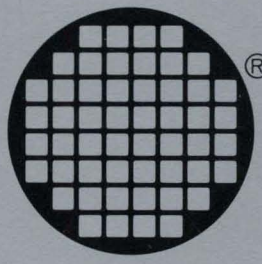

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Static RAMs 1

SRAM Selection Guide

Device	Organization	Access Times (ns)	Maximum Current (mW)		Power Supply Volts	Number of Pins	Package Type	Process	Page No.
			Active	Standby					
IMS1400P IMS1400S IMS1400W	16K x 1 16K x 1 16K x 1	35,45,55 35,45,55 35,45,55	660 660 660	110 110 110	+5 +5 +5	20 20 20	P S W	NMOS NMOS NMOS	1-3 1-3 1-3
IMS1400P-L	16K x 1	70,100	495	83	+5	20	P	NMOS	1-11
IMS1420P IMS1420S IMS1420W	4K x 4 4K x 4 4K x 4	45,55 45,55 45,55	605 605 605	165 165 165	+5 +5 +5	20 20 20	P S W	NMOS NMOS NMOS	1-19 1-19 1-19
IMS1421S	4K x 4	40,50	605	165	+5	20	S	NMOS	1-19
IMS1420P-L	4K x 4	70,100	495	83	+5	20	P	NMOS	1-27
IMS1423P IMS1423S IMS1423W	4K x 4 4K x 4 4K x 4	25,35,45 25,35,45 25,35,45	660 660 660	33 CMOS 33 CMOS 33 CMOS	+5 +5 +5	20 20 20	P S W	CMOS CMOS CMOS	1-35 1-35 1-35
IMS1424P IMS1424S IMS1424W	4K x 4 4K x 4 4K x 4	35,45 35,45 35,45	550 550 550	33 CMOS 33 CMOS 33 CMOS	+5 +5 +5	22 22 22	P S W	CMOS CMOS CMOS	1-43 1-43 1-43
IMS1403P IMS1403S IMS1403W	16K x 1 16K x 1 16K x 1	35,45,55 35,45,55 35,45,55	660 660 660	33 CMOS 33 CMOS 33 CMOS	+5 +5 +5	20 20 20	P S W	CMOS CMOS CMOS	1-44 1-44 1-44
IMS1600P IMS1600S IMS1600W	64K x 1 64K x 1 64K x 1	45,55,70 45,55,70 45,55,70	440 440 440	77 CMOS 77 CMOS 77 CMOS	+5 +5 +5	22 22 22	P S W	CMOS CMOS CMOS	1-45 1-45 1-45
IMS1620S IMS1620W	16K x 4 16K x 4	45,55,70 45,55,70	440 440	77 CMOS 77 CMOS	+5 +5	22 22	S W	CMOS CMOS	1-53 1-53
IMS1624S IMS1624W	16K x 4 16K x 4	45,55,70 45,55,70	440 440	77 CMOS 77 CMOS	+5 +5	24 28	S W	CMOS CMOS	1-61 1-61
IMS1601S IMS1601W	64K x 1 64K x 1	55,70 55,70	440 440	28 CMOS 28 CMOS	+5 +5	22 22	S W	CMOS CMOS	1-62 1-62

NOTES:
P = Plastic DIP
S = Ceramic DIP
W = Ceramic Chip Carrier

IMS1400

High Performance 16Kx1 Static RAM

FEATURES

- 35, 45 and 55ns Chip Enable access
- Maximum active power 660mW
- Maximum standby power 110mW
- Single 5 volt ± 10% supply
- $\overline{E}$ ($\overline{CE}$) power down function
- TTL compatible inputs and output
- Fully static—no clocks for timing
- Three-state output

DESCRIPTION

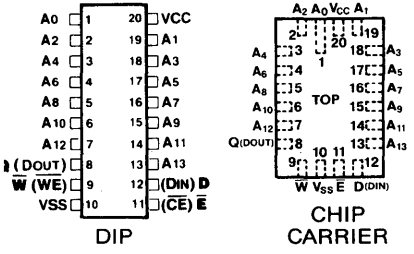
The INMOS IMS1400 is a high performance 16K x 1 bit static RAM having access times of 35, 45 and 55ns and a maximum power consumption of 660mW. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary N-MOS technology.

The IMS1400 features fully static operation requiring no external clocks or timing strobes, equal access and cycle times, full TTL compatibility and operation from a single +5V ± 10% power supply. Additionally, a Chip Enable ($\overline{E}$) function is provided that can be used to place the IMS1400 into a low power standby mode, reducing power consumption to less than 110mW.

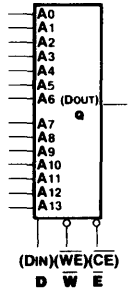
The IMS1400 is packaged in a 20-pin, 300 mil DIP, and is also available in a 20-pin chip carrier, making possible high system packing densities.

The IMS1400 is a high speed VLSI RAM intended for applications that demand superior performance and reliability.

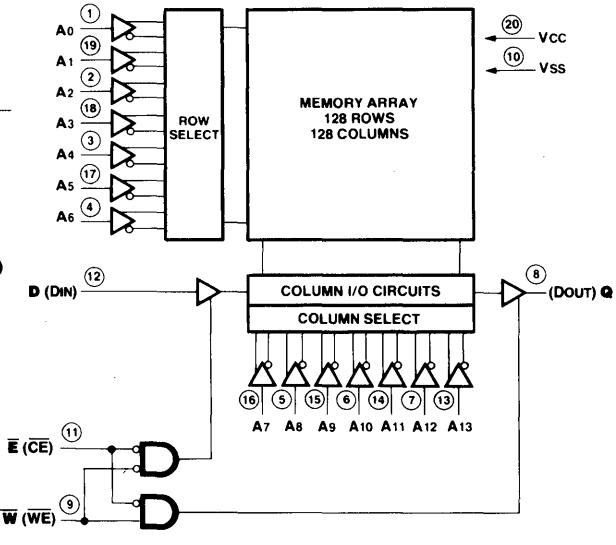
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

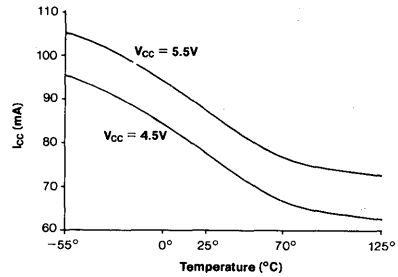
A0 - A13 ADDRESS INPUTS	VCC POWER (+5V)
W (WE) WRITE ENABLE	VSS GROUND
E (CE) CHIP ENABLE	
D (DIN) DATA INPUT	
Q (DOUT) DATA OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temp. (Ceramic Package) . . . . −65°C to 150°C
Storage Temp. (Plastic Package) . . . . −55°C to 125°C
Power Dissipation 1W
DC Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TYPICAL DYNAMIC I_{CC} VS TEMPERATURE



DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		6.0	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−2.5		0.8	V	All Inputs
T_A	Ambient Operating Temperature	0		70	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

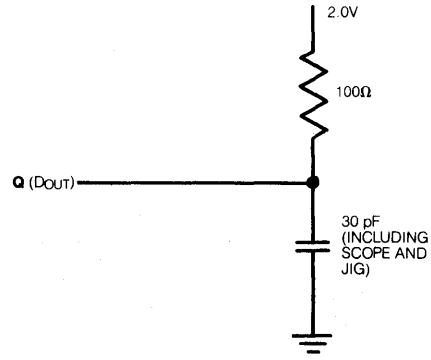
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC		120	mA	$t_C = t_C$ min
I_{CC2}	V_{CC} Power Supply Current (Standby)		20	mA	$\overline{E} \geq V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)	−10	10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 16mA$		0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

FIGURE 1. OUTPUT LOAD



CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV_i = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

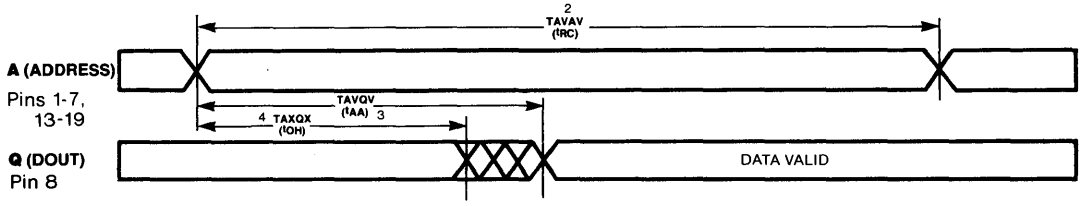
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

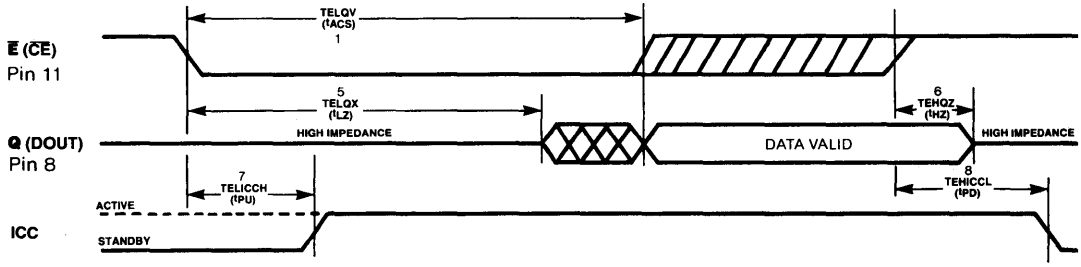
NO.	SYMBOL		PARAMETER	1400-35		1400-45		1400-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	35		40		50		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		35		40		50	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		3		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Disable	0	25	0	25	0	30	ns	f
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	
8	t_{EHICCL}	t_{PD}	Chip Disable to Power Down	0	45	0	45	0	55	ns	
		t_T	Input Rise and Fall Times		50		50		50	ns	e

Note c: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage.

READ CYCLE 1 [c, d]



READ CYCLE 2 [c]



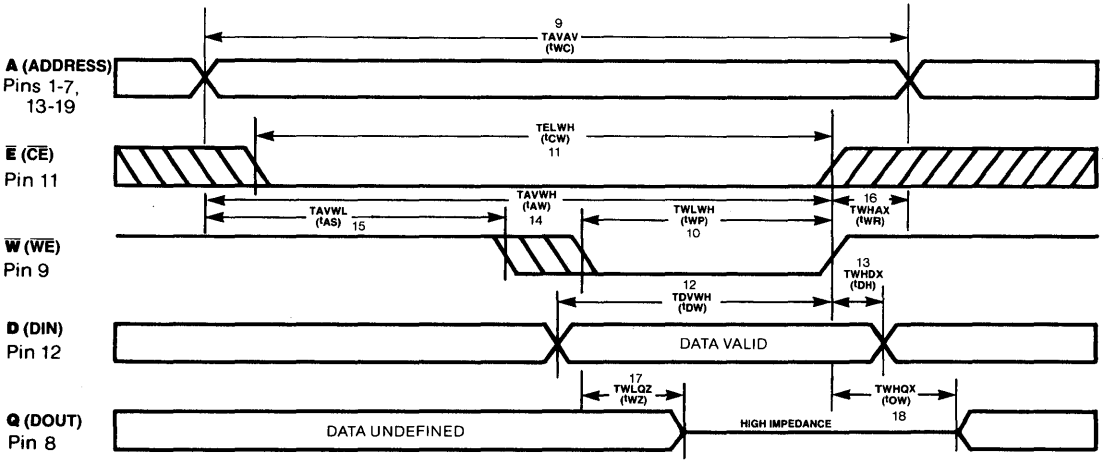
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400-35		1400-45		1400-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	35		40		50		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		20		25		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	35		40		50		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		15		20		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	35		40		50		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	10		10		15		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	25	ns	f
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0	25	0	25	0	30	ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{E}$ goes low with $\overline{W}$ low, output remains in high impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transition.

WRITE CYCLE 1



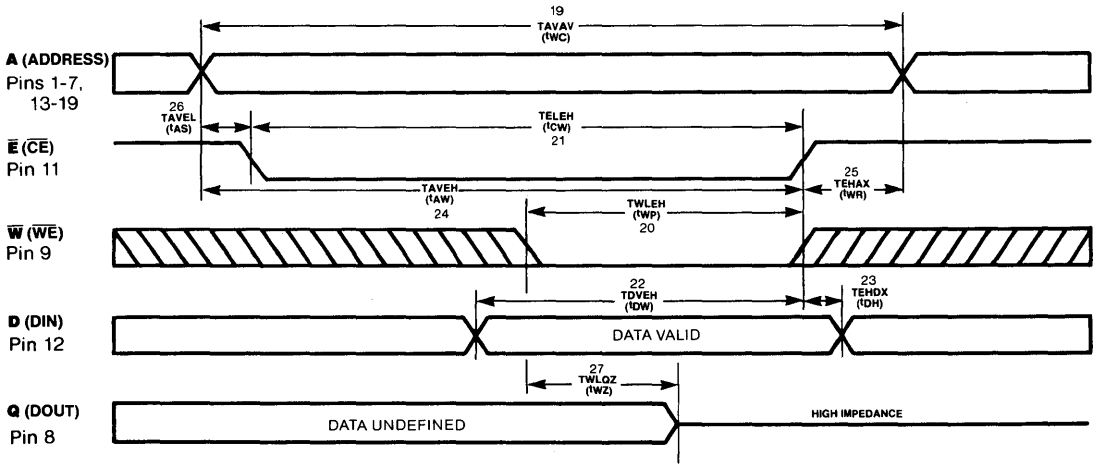
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400-35		1400-45		1400-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	35		40		50		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	35		40		50		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		15		20		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	5		5		5		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	35		40		50		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	−5		−5		−5		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	25	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1400 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), fourteen address inputs, a data in (D_{IN}) and a data out (D_{OUT}).

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms, the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the 14 address inputs are decoded to select one memory cell out of 16,385. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than 1/6 of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout a READ CYCLE 1 and is valid at the specified address access time. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the input (D_{IN}) is written into the selected cell, and the output (D_{OUT}) is in high impedance.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, D_{OUT} becomes active.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, D_{OUT} remains in the high impedance state.

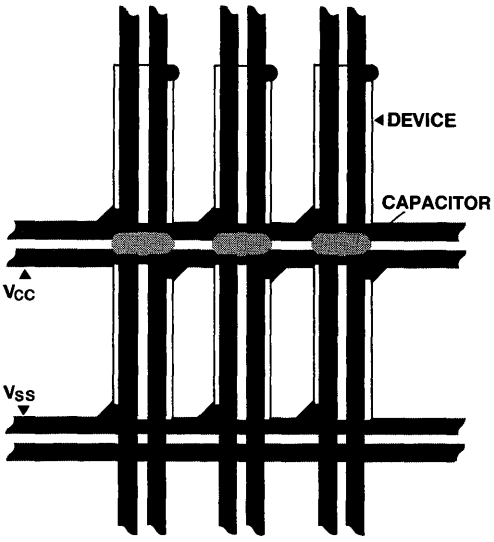
APPLICATION

To ensure proper operation of the IMS1400 in a system environment, it is recommended that the following guidelines on board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor, to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

Also, to prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

The use of proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are some of the most important, yet basic rules to be followed.

The rules are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1400	35ns	PLASTIC DIP	IMS1400P-35
	35ns	CERAMIC DIP	IMS1400S-35
	35ns	CHIP CARRIER	IMS1400W-35
	45ns	PLASTIC DIP	IMS1400P-45
	45ns	CERAMIC DIP	IMS1400S-45
	45ns	CHIP CARRIER	IMS1400W-45
	55ns	PLASTIC DIP	IMS1400P-55
	55ns	CERAMIC DIP	IMS1400S-55
	55ns	CHIP CARRIER	IMS1400W-55

IMS1400L
Low Power 16Kx1 Static RAM

FEATURES

- 70 and 100ns Chip Enable access
- Maximum active power 495mW
- Maximum standby power 83mW
- Single 5 volt ± 10% supply
- $\overline{E}$ power down function
- TTL compatible inputs and output
- Fully static—no clocks for timing
- Three-state output

DESCRIPTION

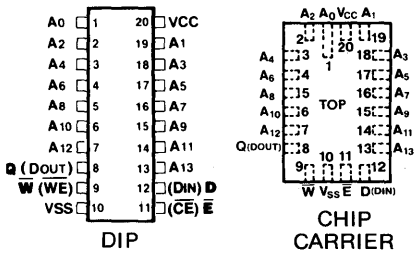
The INMOS IMS1400L is a high performance 16K x 1 bit static RAM having access time of 70 and 100ns and a maximum power consumption of 495mW. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary N-MOS technology.

The IMS1400L features fully static operation requiring no external clocks or timing strobes, equal access and cycle times, full TTL compatibility and operation from a single +5V ± 10% power supply. Additionally, a Chip Enable ($\overline{E}$) function is provided that can be used to place the IMS1400L into a low power standby mode, reducing power consumption to less than 83mW.

The IMS1400L is packaged in a 20-pin, 300-mil plastic DIP, making possible high system packing densities.

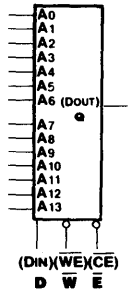
The IMS1400L is a high speed VLSI RAM intended for low power applications that demand superior performance and reliability.

PIN CONFIGURATION

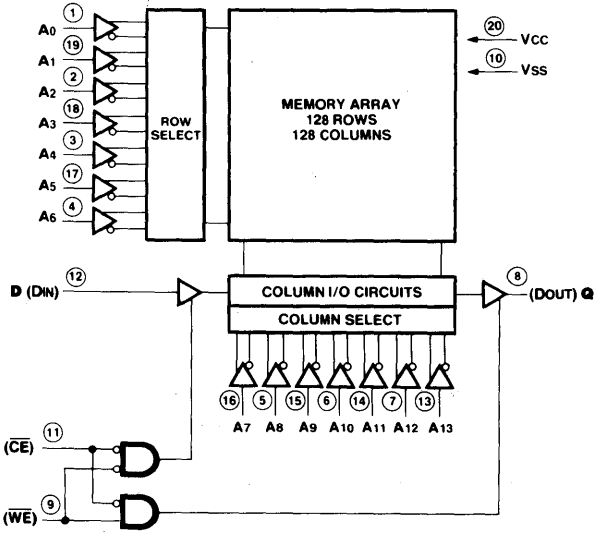


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

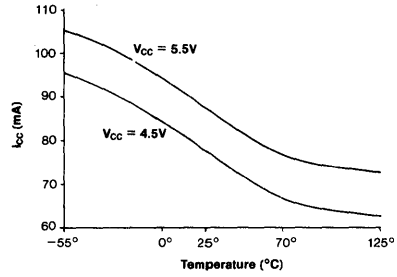
A0 - A13 ADDRESS INPUTS	VCC POWER (+5V)
W (WE) WRITE ENABLE	VSS GROUND
E (CE) CHIP ENABLE	
D (DIN) DATA INPUT	
Q (DOUT) DATA OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TYPICAL DYNAMIC I_{CC} VS TEMPERATURE



DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		6.0	V	
V_{IL}	Input Logic "0" Voltage	−2.0		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

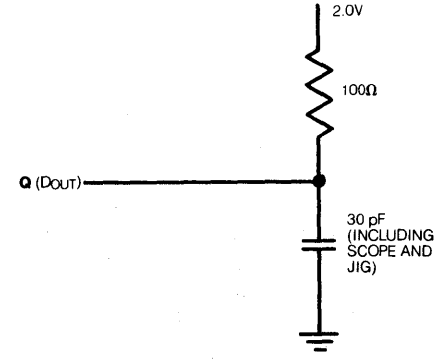
SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC	0°C		90	mA	$t_C = t_C$ min
		25°C		85		
		70°C		75		
I_{CC2}	V_{CC} Power Supply Current (Standby)	0°C-70°C		15	mA	$\overline{E} \ge V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)		−10	10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		−50	50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$		2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 16mA$			0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

FIGURE 1. OUTPUT LOAD



CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

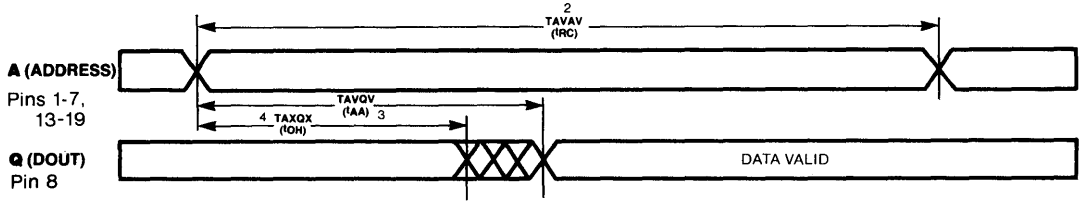
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

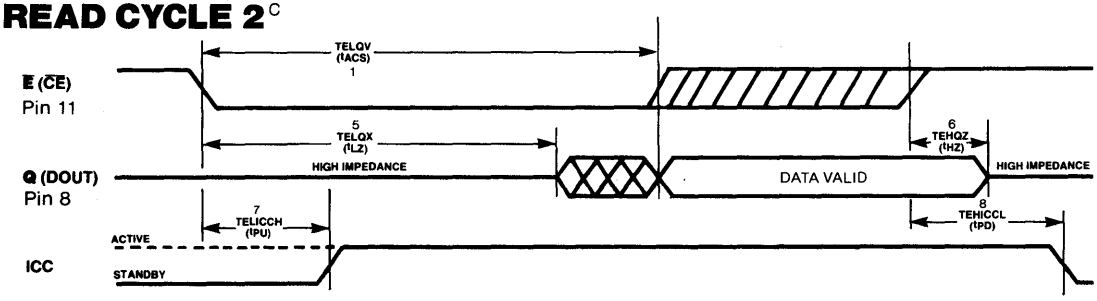
NO.	SYMBOL	PARAMETER	1420L-70		1420L-10		UNITS	NOTES
			MIN	MAX	MIN	MAX		
1	t_{ACS}	Chip Enable Access Time		70		100	ns	
2	t_{RC}	Read Cycle Time	65		95		ns	c
3	t_{AA}	Address Access Time		65		95	ns	d
4	t_{OH}	Output Hold After Address Change	5		5		ns	
5	t_{LZ}	Chip Enable to Output Active	20		20		ns	
6	t_{HZ}	Chip Disable to Output Disable		25		25	ns	f
7	t_{PU}	Chip Enable to Power Up	0		0		ns	
8	t_{PD}	Chip Disable to Power Down		70		70	ns	
9	t_{RCS}	Read Command Set-up Time	−5		−5		ns	
10	t_{RCH}	Read Command Hold Time	−5		−5		ns	
	t_T	Input Rise and Fall Times		50		50	ns	e

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



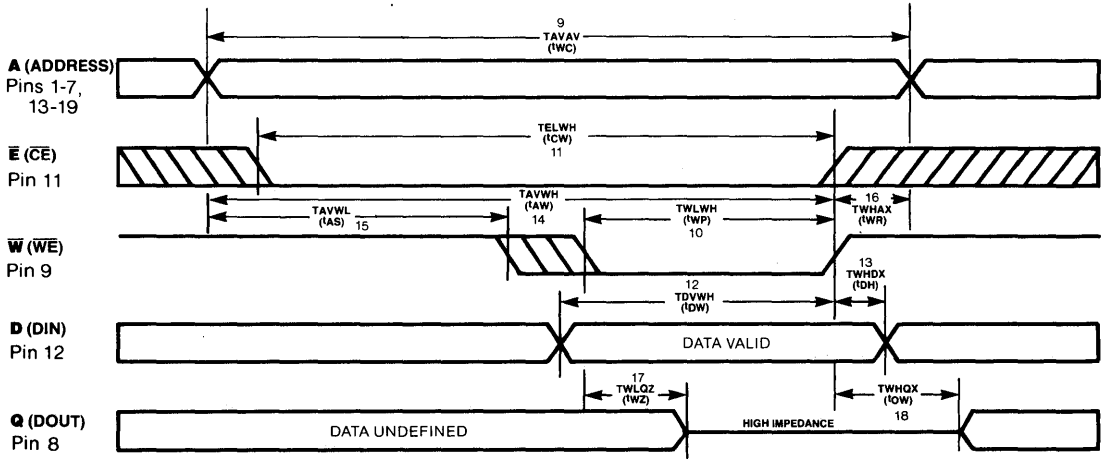
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	1420L-70		1420L-10		UNITS	NOTES
			MIN	MAX	MIN	MAX		
11	t_{WC}	Write Cycle Time	70		100		ns	
12	t_{WP}	Write Pulse Width	65		70		ns	
13	t_{CW}	Chip Enable to End of Write	65		70		ns	
14	t_{DW}	Data Set-up to End of Write	30		35		ns	
15	t_{DH}	Data Hold After End of Write	5		5		ns	
16	t_{AW}	Address Set-up to End of Write	65		70		ns	
17	t_{AS}	Address Set-up to Beginning of Write	0		0		ns	
18	t_{WR}	Address Hold After End of Write	5		5		ns	
19	t_{WZ}	Write Enable to Output Disable		35		40	ns	f
20	t_{OW}	Output Active After End of Write	0		0		ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{E}$ goes low with $\overline{W}$ low, output remains in high impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 1



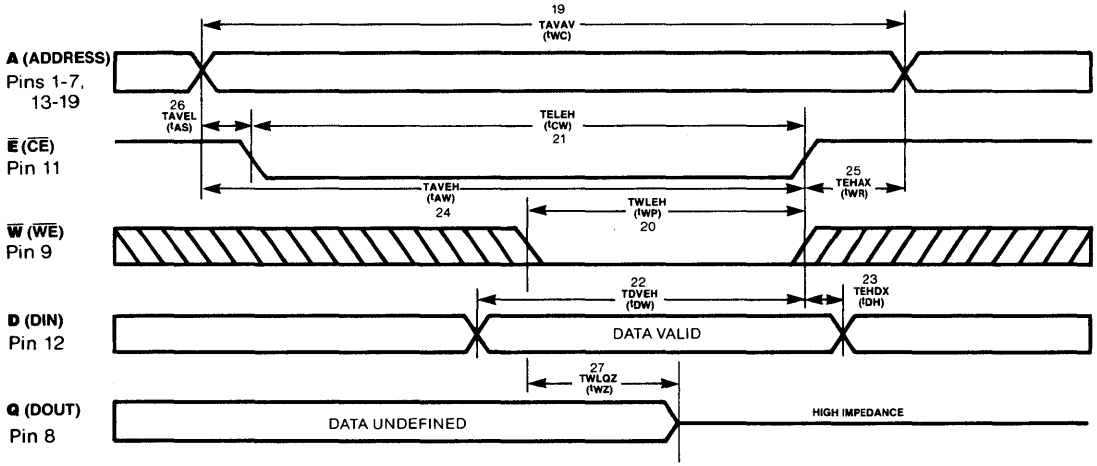
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	1420L-70		1420L-10		UNITS	NOTES
			MIN	MAX	MIN	MAX		
21	t_{WC}	Write Cycle Time	70		100		ns	
22	t_{WP}	Write Pulse Width	65		70		ns	
23	t_{CW}	Chip Enable to End of Write	65		70		ns	
24	t_{DW}	Data Set-up to End of Write	30		35		ns	
25	t_{DH}	Data Hold After End of Write	5		5		ns	
26	t_{AW}	Address Set-up to End of Write	60		65		ns	
27	t_{WR}	Address Hold After End of Write	5		5		ns	
28	t_{AS}	Address Set-up to Beginning of Write	−5		−5		ns	
29	t_{WZ}	Write Enable to Output Disable		35		40	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1400L has two control inputs: Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), 14 address inputs, a data in (D_{IN}) and a data out (D_{OUT}).

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms, the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the 14 address inputs are decoded to select one memory cell out of 16,385. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-fifth of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout a READ CYCLE 1 and is valid at the specified address access time. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the input (D_{IN}) is written into the selected cell, and the output (D_{OUT}) is in high impedance.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, D_{OUT} becomes active.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, D_{OUT} remains in the high impedance state.

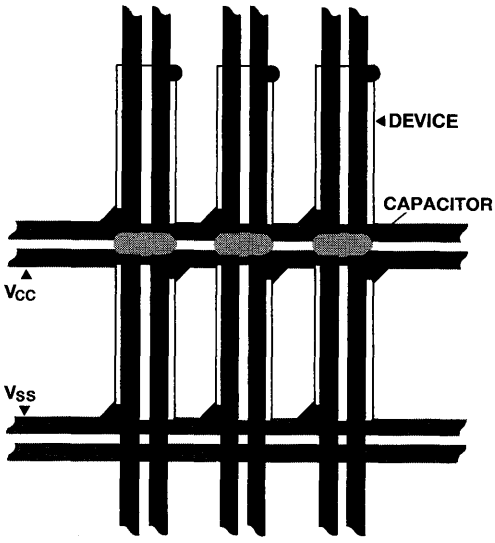
APPLICATION

To ensure proper operation of the IMS1400L in a system environment, it is recommended that the following guidelines on board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor, to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

Also, to prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

The use of proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are some of the most important, yet basic rules to be followed.

The rules are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1400L	70ns	PLASTIC DIP	IMS1400P-70L
	100ns	PLASTIC DIP	IMS1400P-10L

IMS1420
IMS1421
High Performance 4K x 4 Static RAM

FEATURES

- 4K x 4 Bit Organization
- 40nsec and 50nsec Address Access Times
- 605mW Maximum Power Dissipation
- Fully TTL Compatible
- Common Data Inputs & Outputs
- 20-Pin, 300-mil DIP
- Single +5 volt ± 10% Operation

IMS1420
- 45nsec and 55nsec Chip Enable Access Times
- Power Down Function
- 165mW Maximum Standby Power

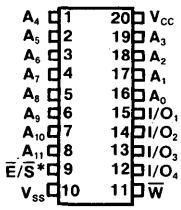
IMS1421
- High Speed Chip Select Function
- 30nsec and 40nsec Chip Select Access Times

DESCRIPTION

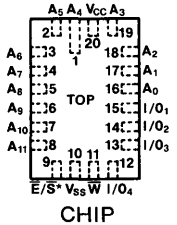
The IMS1420 and IMS1421 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1420 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode, thus reducing power to 165mW. In place of the Chip Enable function, the IMS1421 provides a high speed Chip Select ($\overline{S}$) function which allows faster access times to be achieved. With these two options, the designer can select the device which better fits his particular application.

The IMS1420 is packaged in a 20-pin 300-mil plastic DIP, and both the IMS1420 and IMS1421 are available in ceramic DIPs and ceramic chip carriers.

PIN CONFIGURATION

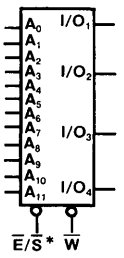


DIP

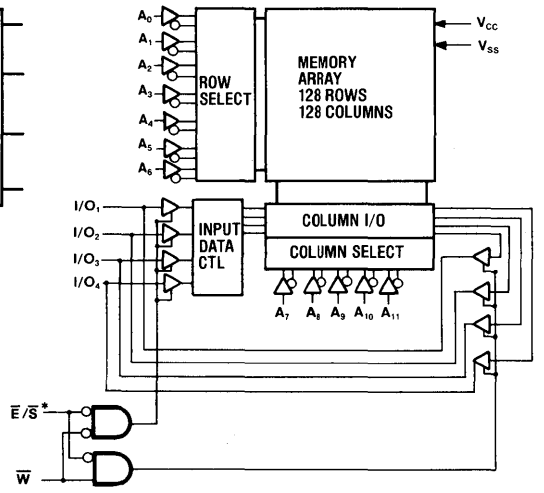


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{11} ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{W}$ WRITE ENABLE	V_{SS} GROUND
$\overline{E}$* CHIP ENABLE	
$\overline{S}$* CHIP SELECT	
I/O DATA IN/OUT	

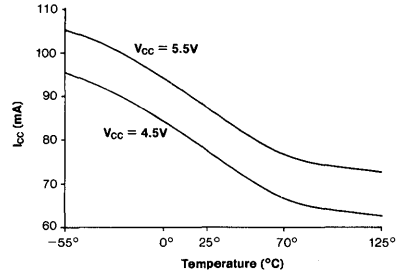
* $\overline{E}$ IMS1420 ONLY
$\overline{S}$ IMS1421 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TYPICAL DYNAMIC I_{CC} VS TEMPERATURE



DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		6.0	V	
V_{IL}	Input Logic "0" Voltage	−2.5		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = 5.0V \pm 10\%$)

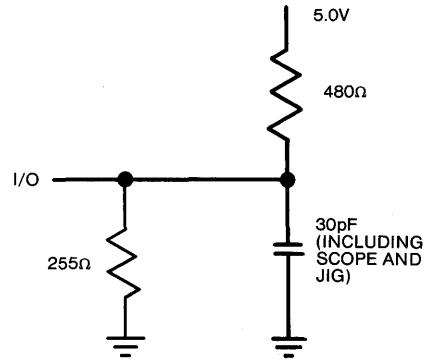
SYMBOL	PARAMETER	1420		1421		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}	Average V_{CC} Power Supply Current AC		110		110	mA	$t_C = t_C$ (min)
I_{CC2}	V_{CC} Power Supply Current (Stdby)		30		NA	mA	$\overline{E} \geq V_{IH}$ (min)
I_{IN}	Input Leakage Current (Any Input)		10		10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		50		50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 8mA$		.4		.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

FIGURE 1. OUTPUT LOAD



CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}/\overline{S}}$	$\overline{E}/\overline{S}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

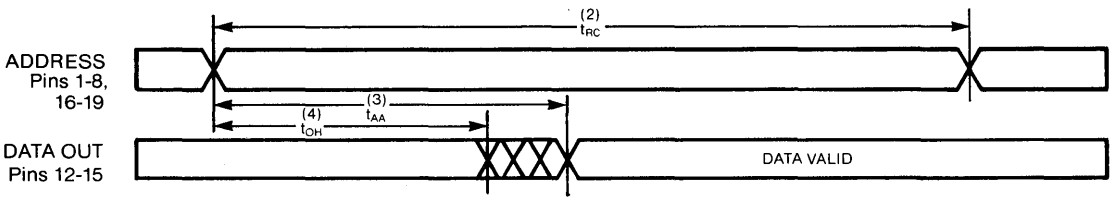
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

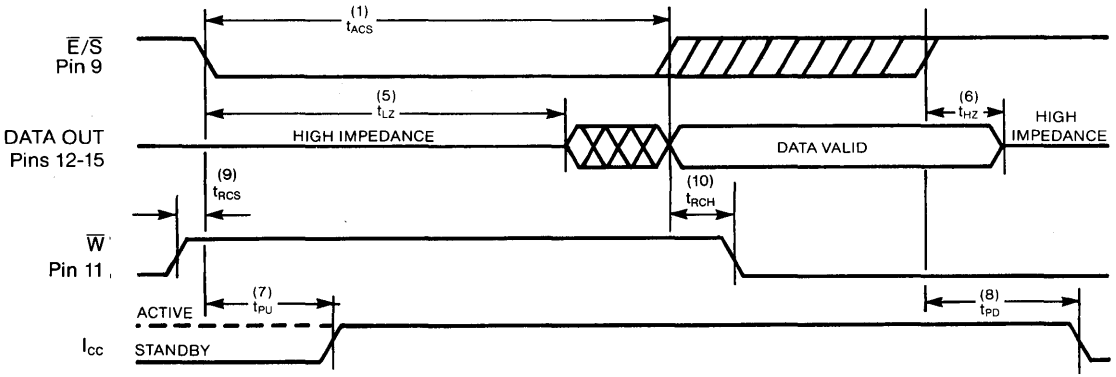
NO.	SYMBOL	PARAMETER	1420-45		1420-55		1421-40		1421-50		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ACS}	Chip Enable/Select Access Time		45		55		30		40	ns	
2	t_{RC}	Read Cycle Time	40		50		40		50		ns	c
3	t_{AA}	Address Access Time		40		50		40		50	ns	d
4	t_{OH}	Output Hold After Address Change	3		3		3		3		ns	
5	t_{LZ}	Chip Enable/Select to Output Active	20		20		20		20		ns	
6	t_{HZ}	Chip Disable/Select to Output Disable		20		25		20		25	ns	f
7	t_{PU}	Chip Enable to Power Up	0		0		NA		NA		ns	
8	t_{PD}	Chip Disable to Power Down		45		55		NA		NA	ns	
9	t_{RCS}	Read Command Set-Up Time	−5		−5		−5		−5		ns	
10	t_{RCH}	Read Command Hold Time	−5		−5		−5		−5		ns	
	t_T	Input Rise and Fall Times		50		50		50		50	ns	e

Note c: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected $\overline{E}/\overline{S}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



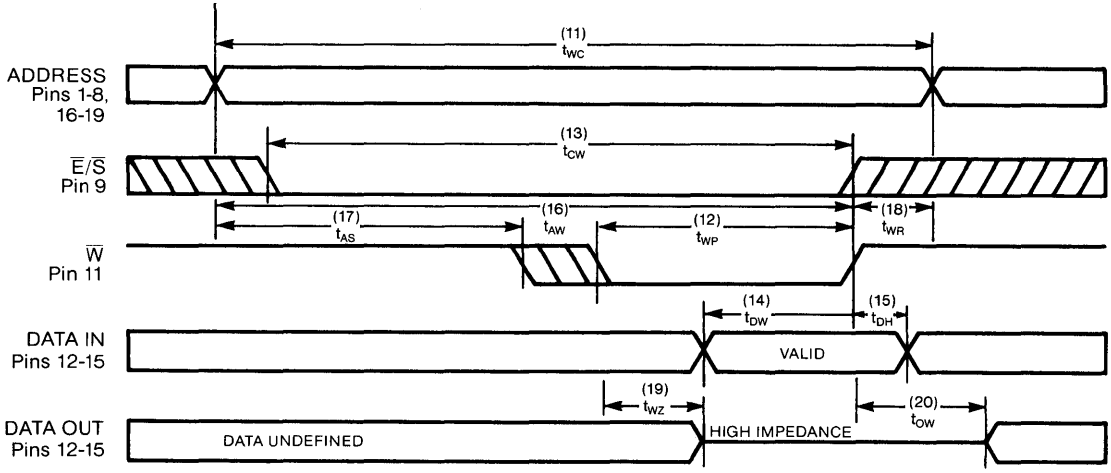
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	1420-45		1420-55		1421-40		1421-50		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
11	t_{WC}	Write Cycle Time	40		50		40		50		ns	
12	t_{WP}	Write Pulse Width	35		45		35		45		ns	
13	t_{CW}	Chip Enable/Select to End of Write	35		45		30		40		ns	
14	t_{DW}	Data Set-up to End of Write	15		20		15		20		ns	
15	t_{DH}	Data Hold After End of Write	3		3		3		3		ns	
16	t_{AW}	Address Set-up to End of Write	35		45		40		50		ns	
17	t_{AS}	Address Set-up to Beginning of Write	0		0		0		0		ns	
18	t_{WR}	Address Hold After End of Write	5		5		0		0		ns	
19	t_{WZ}	Write Enable to Output Disable		20		25		20		25	ns	f
20	t_{OW}	Output Active After End of Write	8		8		8		8		ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{E}/\overline{S}$ goes low with $\overline{W}$ low, output remains in high impedance state.
Note h: $\overline{E}/\overline{S}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 1



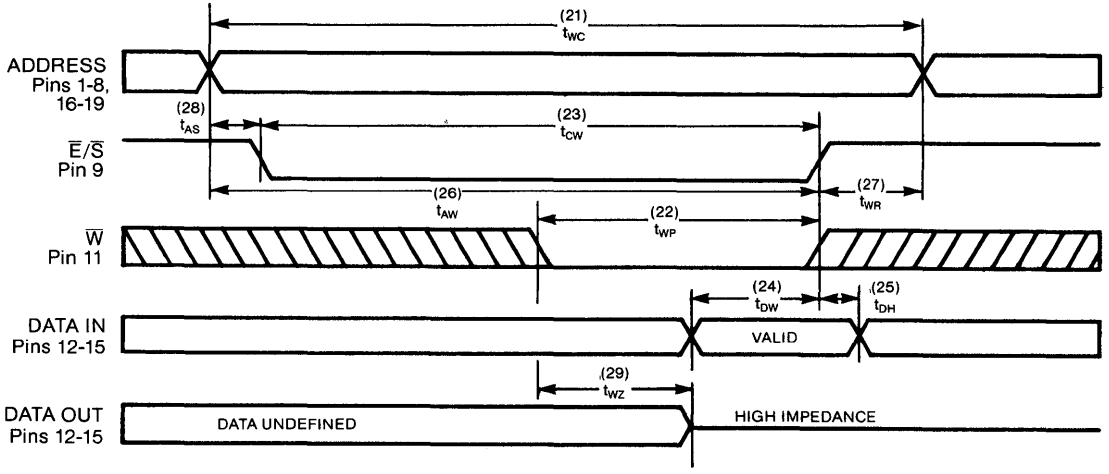
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}/\overline{S}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	1420-45		1420-55		1421-40		1421-50		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
21	t_{WC}	Write Cycle Time	40		50		40		50		ns	
22	t_{WP}	Write Pulse Width	35		45		35		45		ns	
23	t_{CW}	Chip Enable/Select to End of Write	35		45		30		40		ns	
24	t_{DW}	Data Set-up to End of Write	15		20		15		20		ns	
25	t_{DH}	Data Hold After End of Write	5		5		5		5		ns	
26	t_{AW}	Address Set-up to End of Write	30		40		35		45		ns	
27	t_{WR}	Address Hold After End of Write	5		5		5		5		ns	
28	t_{AS}	Address Set-up to Beginning of Write	−5		−5		0		0		ns	
29	t_{WZ}	Write Enable to Output Disable		20		25		20		25	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}/\overline{S}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 2



DEVICE OPERATION (IMS1420)

The IMS1420 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs, and four Data I/O lines.

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms, the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one 4-bit word out of 4096. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-third of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of 3ns. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the inputs is written into the selected cells, and the outputs are floating.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address need not be stable until a maximum of 5ns after $\overline{E}$ goes low. The address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, the outputs become active. When $\overline{W}$ goes high at the end of a write cycle and the outputs of the memory go active, the data from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high the outputs remain in the high impedance state.

DEVICE OPERATION (IMS1421)

The operation of the IMS1421 is similar to the operation of the IMS1420 except that the Chip Enable ($\overline{E}$) function on the IMS1420 is replaced by a high speed Chip Select ($\overline{S}$) for the IMS1421. The $\overline{S}$ function controls chip selection but there is no power down function on the IMS1421. The IMS1421 is designed to allow even higher system performance than is possible with the IMS1420 by removing the Chip Select decoder delay from the critical access delay path.

With $\overline{S}$ high, the device is deselected and the outputs are disabled

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{S} \leq V_{IL}$ max. Read access time is measured from either $\overline{S}$ going low or from valid address. If $\overline{S}$ goes low within 10ns of address valid, access time is equal to address access time. If $\overline{S}$ goes low later than 10ns after address valid, then access time is equal to Chip Select access time.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{S}$ going low and is terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{S}$ (WRITE CYCLE 2) going high. During a write cycle, the outputs are floated and the data on the inputs are written into the addressed memory cells.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the specified WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{S}$ going low, the address must be stable for the specified WRITE CYCLE 2 set-up time. WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high and $\overline{S}$ low, the outputs become active.

WRITE CYCLE 2 on page 5 shows a write cycle terminated by the rising edge of $\overline{S}$. Data set-up and hold times are referenced to the rising edge of $\overline{S}$ and the outputs remain in the high impedance state.

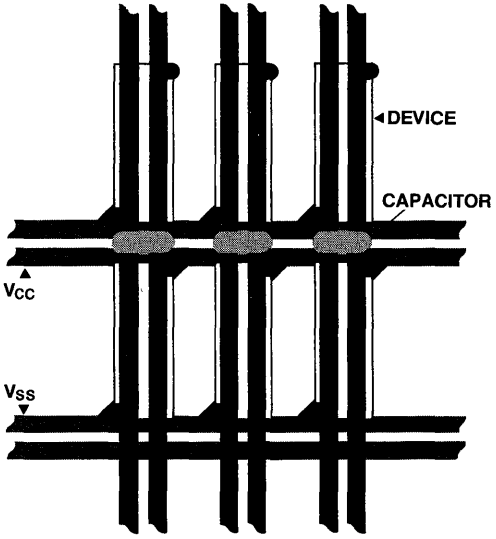
APPLICATION

Fundamental rules in regard to memory board layout should be followed to ensure maximum benefit from the features offered by the IMS1420/21 Static RAM.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1420/21. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1420/21 are high frequency, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor acts as a low impedance power supply located near the memory device. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the back-plane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board providing a quiet environment free of noise spikes and signal reflections.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1420	45ns	PLASTIC DIP	IMS1420P-45
	45ns	CERAMIC DIP	IMS1420S-45
	45ns	CHIP CARRIER	IMS1420W-45
	55ns	PLASTIC DIP	IMS1420P-55
	55ns	CERAMIC DIP	IMS1420S-55
	55ns	CHIP CARRIER	IMS1420W-55
IMS1421	40ns	CERAMIC DIP	IMS1421S-40
	40ns	CHIP CARRIER	IMS1421W-40
	50ns	CERAMIC DIP	IMS1421S-50
	50ns	CHIP CARRIER	IMS1421W-50

IMS1420L
Low Power 4Kx4 Static RAM

FEATURES

- 4K x 4 Bit Organization
- 70 and 100ns Chip Enable Access Times
- 65 and 95ns Address Access Times
- 495mW Maximum Power Dissipation
- 83mW Maximum Standby Power
- Fully TTL Compatible
- Common Data Inputs and Outputs
- 20-pin, 300-mil Plastic DIP
- Single 5 volt ± 10% Operation
- Power Down Function

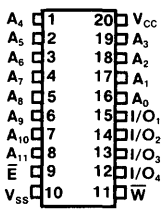
DESCRIPTION

The INMOS IMS1420L features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1420L provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode, thus reducing power to 83mW.

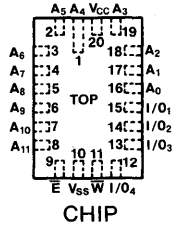
The IMS1420L is packaged in a 20-pin, 300 mil plastic DIP. This makes possible high system packing densities.

The IMS1420L is a high speed VLSI RAM intended for applications that demand superior performance and reliability.

PIN CONFIGURATION



DIP

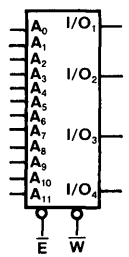


CHIP CARRIER

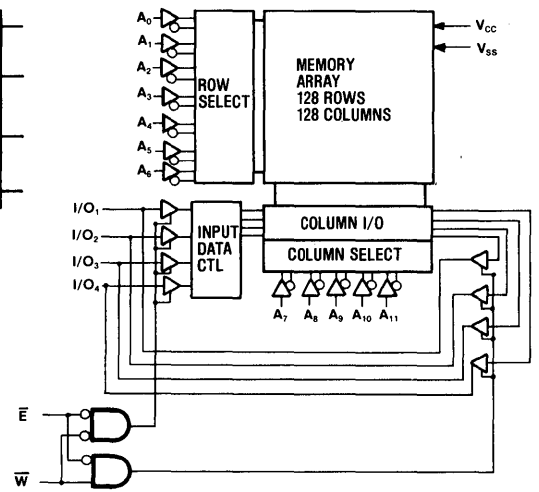
PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$	CHIP ENABLE		
I/O	DATA IN/OUT		

LOGIC SYMBOL



BLOCK DIAGRAM

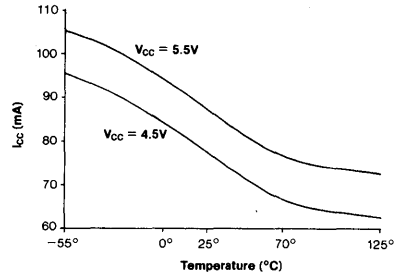


ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TYPICAL DYNAMIC I_{CC} VS TEMPERATURE



DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		6.0	V	
V_{IL}	Input Logic "0" Voltage	−2.5		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

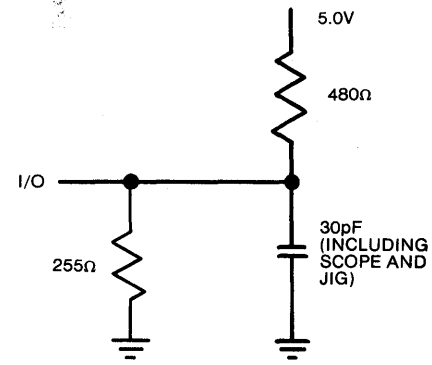
SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC	0°C		90	mA	$t_C = t_C$ min
		25°C		85		
		70°C		75		
I_{CC2}	V_{CC} Power Supply Current (Standby)	0°C-70°C		15	mA	$\overline{E} \geq V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)			10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current			50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$		2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 8mA$			0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

FIGURE 1. OUTPUT LOAD



CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

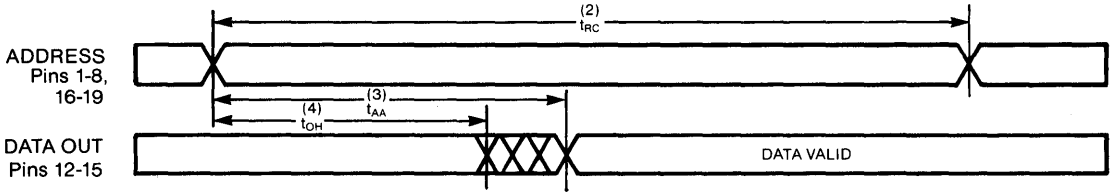
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

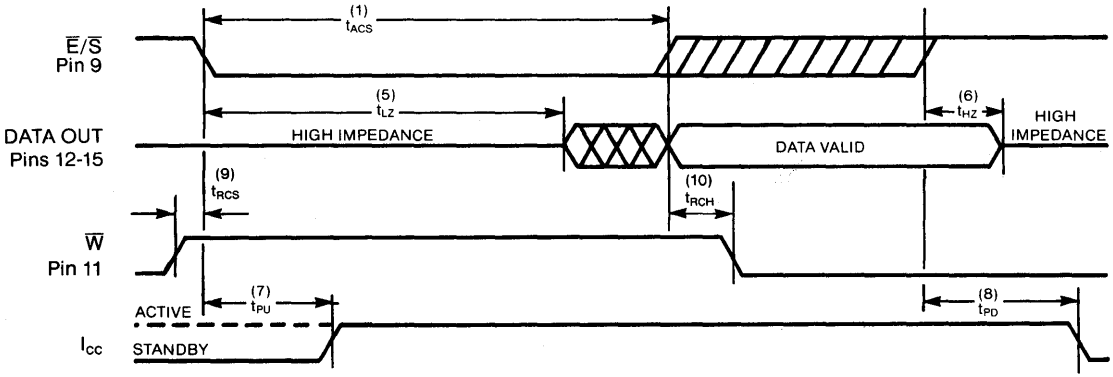
NO.	SYMBOL		PARAMETER	1400L-70		1400L-10		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		70		100	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	65		95		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		65		95	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Disable	0	30	0	40	ns	f
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		ns	
8	t_{EHICCL}	t_{PD}	Chip Disable to Power Down	0	65	0	65	ns	
		t_T	Input Rise and Fall Times		50		50	ns	e

Note c: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage.

READ CYCLE 1 [c, d]



READ CYCLE 2 [c]



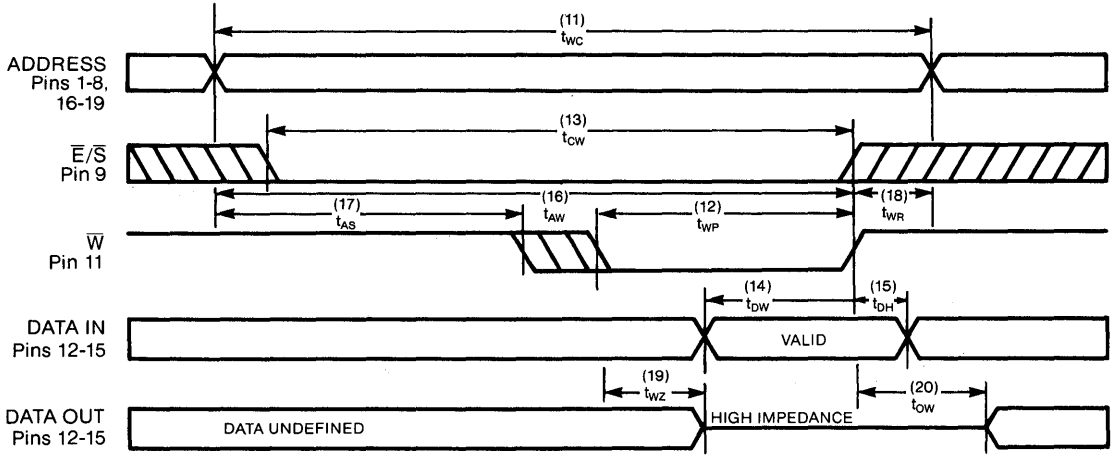
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400L-70		1400L-10		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	65		95		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	40		45		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	55		60		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	30		35		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		5		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	55		60		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	5		10		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		5		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	35	ns	f
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0	40	0	40	ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{E}$ goes low with $\overline{W}$ low, output remains in high impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 1



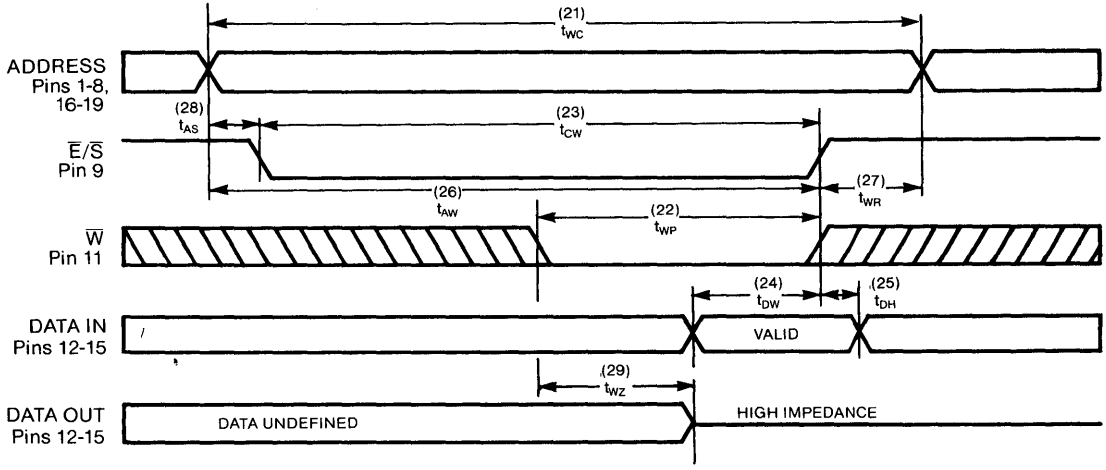
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400L-70		1400L-10		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	65		95		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	30		35		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	55		60		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	30		35		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	5		5		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	55		60		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		5		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	30	0	30	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1420L has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs, and four Data I/O lines.

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms, the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one 4-bit word out of 4096. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-fifth of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout a READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of 3ns. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the inputs is written into the selected cells and the outputs are floating.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address need not be stable until a maximum of 5ns after $\overline{E}$ goes low. The address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, the outputs become active. When $\overline{W}$ goes high at the end of a write cycle and the outputs of the memory go active, the data from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

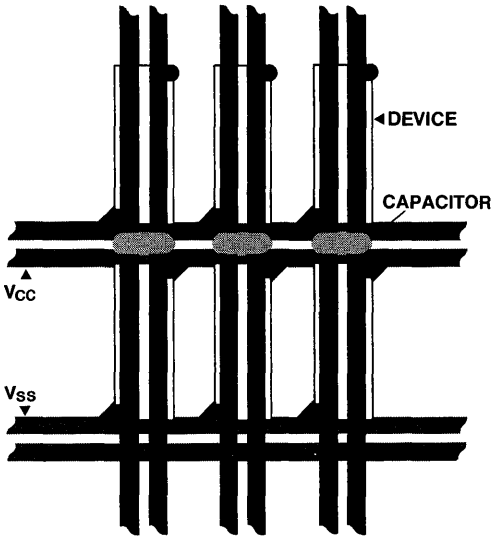
APPLICATION

Fundamental rules in regard to memory board layout should be followed to ensure maximum benefit from the features offered by the IMS1420L Static RAM.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1420L. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1420L are high frequency, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor acts as a low impedance power supply located near the memory device. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board providing a quiet environment free of noise spikes and signal reflections.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1420L	70ns	PLASTIC DIP	IMS1420P-70L
	100ns	PLASTIC DIP	IMS1420P-10L

IMS1423
High Performance 4K x 4 CMOS Static RAM

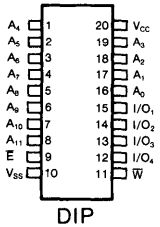
FEATURES

- INMOS Very High Speed CMOS
- Advanced Process—2 Micron Design Rules
- 4K x 4 Bit Organization
- 25nsec, 35nsec and 40nsec Address Access Times
- 25nsec, 35nsec and 45nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- Power Down Function
- 660mW Maximum Power Dissipation
- 100mW Maximum Standby Power
- 33mW Maximum Standby Power (Stable CMOS levels)
- 20 Pin, 300-mil DIP (JEDEC Standard)
- Pin Compatible with IMS1420

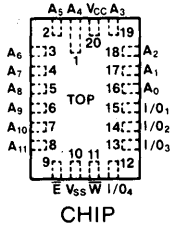
DESCRIPTION

The IMS1423 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1423 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode, thus reducing power to 100mW. By using CMOS levels, the standby power may be reduced to an even lower 33mW.

PIN CONFIGURATION

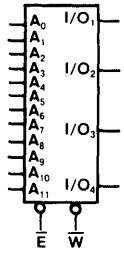


DIP

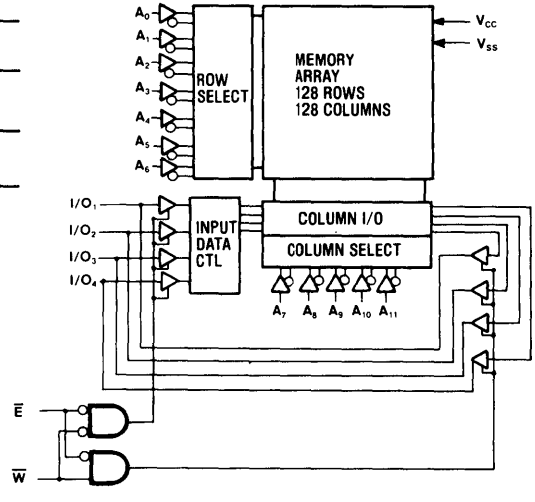


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{11} ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{W}$ WRITE ENABLE	V_{SS} GROUND
$\overline{E}$ CHIP ENABLE	
I/O DATA IN/OUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −2.0 to 7.0V
Voltage on I/O (Pins 13-16) . . . . . −1.0 to (V_{CC} + .5V)
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current . . . . . 25mA (One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC} + .5	V	
V_{IL}	Input Logic "0" Voltage	−1.0		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	400 Linear ft./min. transverse air flow

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current AC		120 110 100	mA mA mA	t_{AVAV} = 25ns, j t_{AVAV} = 35ns, j t_{AVAV} = 45ns, j
I_{CC_2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		18	mA	$\overline{E} \geq 2.0V$ All Other Inputs 2.0V $\leq V_{IN} \leq 0.8V$
I_{CC_3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		6	mA	$\overline{E} \geq (V_{CC} - 0.3V)$ All Other Inputs $V_{CC} - .3V \leq V_{IN} \leq 0.3V$
I_{CC_4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels) $\overline{E} \geq (V_{CC} - .3V)$		13 12 11	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns All Other Inputs Cycling from 0.3V to V_{CC} −.3V
I_{IN}	Input Leakage Current (Any Input)		±10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = −4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

Note j: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS[a]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

Note a: Operation to specifications guaranteed 500μS after $V_{CC} \geq 4.5$.

CAPACITANCE[b] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

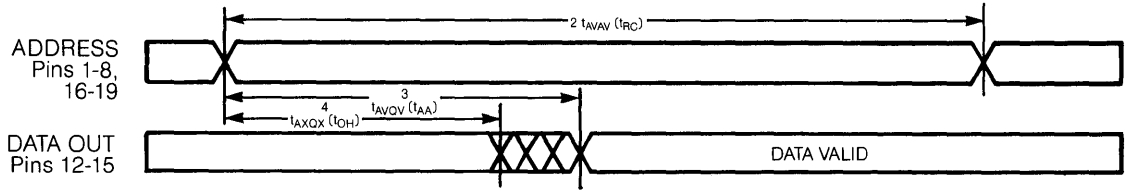
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE [i]

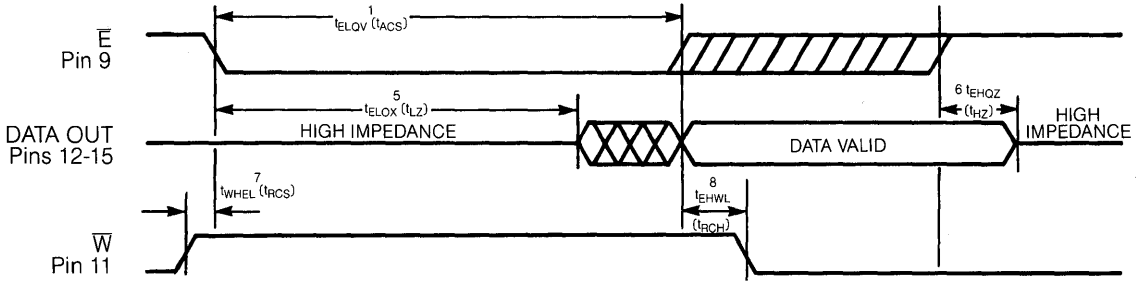
NO.	SYMBOL Standard	SYMBOL Alternate	PARAMETER	1423-25 MIN	1423-25 MAX	1423-35 MIN	1423-35 MAX	1423-45 MIN	1423-45 MAX	UNITS	NOTES
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		40		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		40	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		3		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	15	0	20	0	20	ns	f
7	t_{WHEL}	t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
8	t_{EHWL}	t_{RCH}	Read Command Hold Time	0		0		0		ns	
9	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	
10	t_{EHICCL}	t_{PD}	Chip Enable To Power Down		25		35		45	ns	
		t_T	Input Rise and Fall Times		50		50		50	ns	e

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage.
Note i: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.

READ CYCLE 1 [c,d]



READ CYCLE 2 [c]



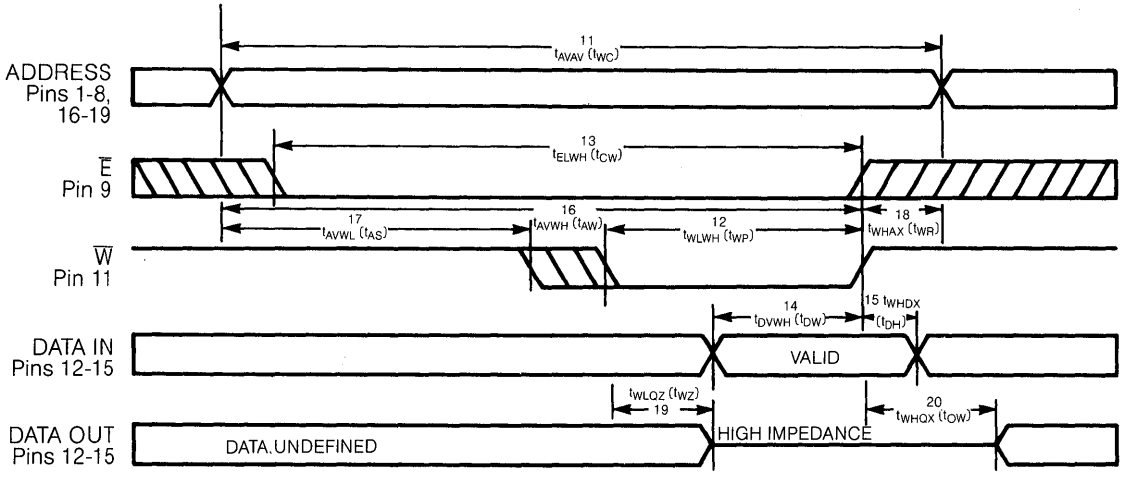
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h, i]

NO.	SYMBOL		PARAMETER	1423-25		1423-35		1423-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
11	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		40		ns	
12	t_{WLWH}	t_{WP}	Write Pulse Width	20		25		35		ns	
13	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		25		35		ns	
14	t_{DVWH}	t_{DW}	Data Set-up to End of Write	10		13		15		ns	
15	t_{WHDX}	t_{DH}	Data Hold After End of Write	2		2		5		ns	
16	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		25		35		ns	
17	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
18	t_{WHAX}	t_{WR}	Address Hold After End of Write	2		3		5		ns	
19	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	10	0	12	0	20	ns	f
20	t_{WHQX}	t_{OW}	Output Active After End of Write	6		6		6		ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{W}$ is low when $\overline{E}$ goes low, output remains in the high impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.

WRITE CYCLE 1



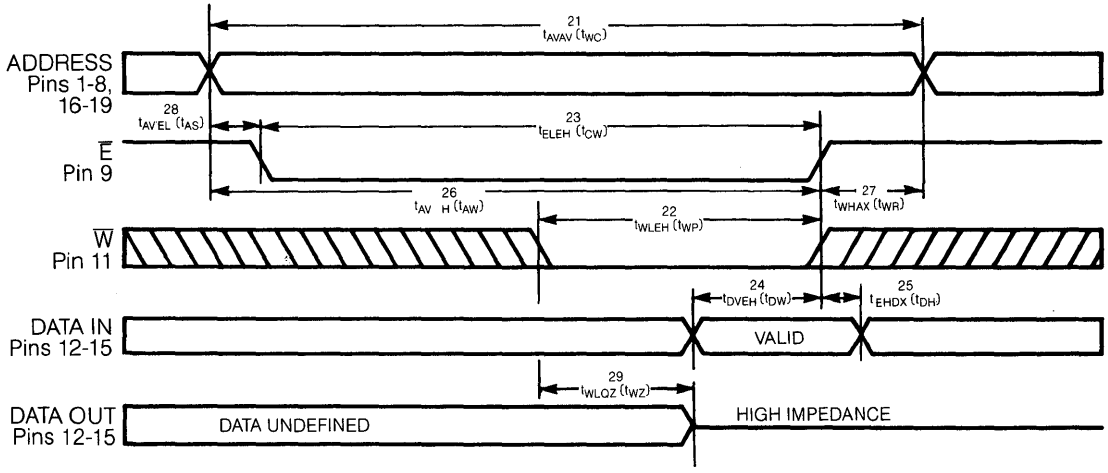
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h, i]

NO.	SYMBOL Standard	SYMBOL Alternate	PARAMETER	1423-25 MIN	1423-25 MAX	1423-35 MIN	1423-35 MAX	1423-45 MIN	1423-45 MAX	UNITS	NOTES
21	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		40		ns	
22	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		35		ns	
23	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		35		ns	
24	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		13		15		ns	
25	t_{EHDX}	t_{DH}	Data Hold After End of Write	2		2		5		ns	
26	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		35		ns	
27	t_{EHAX}	t_{WR}	Address Hold After End of Write	2		3		5		ns	
28	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
29	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	10	0	12	0	20	ns	f, g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1423 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs (A_0-A_{11}), and four Data I/O lines.

The IMS1423 becomes active immediately after V_{CC} is applied, but proper operation is not assured until 500 microseconds after V_{CC} reaches 4.5 volts.

With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one 4-bit word out of 4096. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-fourth of the active mode power with TTL input levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from the latter of either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of t_{AXQV}. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

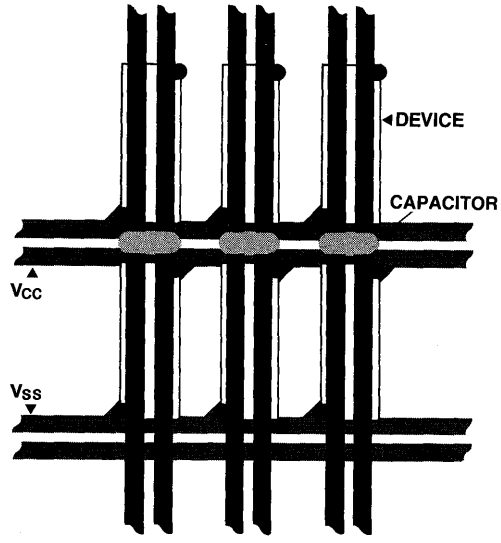
WRITE CYCLE

The write cycle of the IMS1423 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high level to a low level. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common input/output connections. Therefore input data should not be active until after t_{WLQZ} to avoid bus contention. During a write cycle, data on the inputs is written into the selected cells and the outputs are floating.

If a write cycle is initiated by $\overline{E}$ going low, the address must be stable for t_{AVEL} referenced to $\overline{E}$. If the write cycle is initiated by $\overline{W}$ going low, then the address must be valid for t_{AVWL} referenced to $\overline{W}$. The address must be held stable for the entire write cycle. After either $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If the set-up and hold times are not met, for either address or data, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high while $\overline{E}$ is low, the outputs become active. When $\overline{W}$ goes high at the end of a write cycle and the outputs of the memory go active, the data from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1423, that the fundamental rules of good engineering practice be followed in areas such as board layout and signal fidelity to ensure proper system operation.

TTL VS. CMOS INPUT LEVELS

The IMS1423 is fully compatible with TTL input levels. The input circuitry of the IMS1423 is designed for maximum speed and also for conversion of TTL level signals to the CMOS levels required for internal operation. The IMS1423 consumes less power when CMOS levels (.3/ V_{CC} −.3 volts) are used than TTL levels (.8/2.0 volts) are applied. The lower CMOS I_{CC} specifications, I_{CC3} and I_{CC4}, may be achieved by using CMOS levels. The power consumption will be lower at typical TTL levels than at the worst case levels.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the wide operating margins of the IMS1423. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1423 have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as near the memory as possible, with the shortest lead lengths practical. The high frequency decoupling capacitor should have a minimum value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor, for low frequency current transients, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The termination resistor should be placed as close to the driver package as possible. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33ohm range will be required. Because the characteristic impedance of each layout will be different, it is necessary to select the proper value of this resistor by trial and error. A resistor of predetermined value may not properly terminate the transmission line.

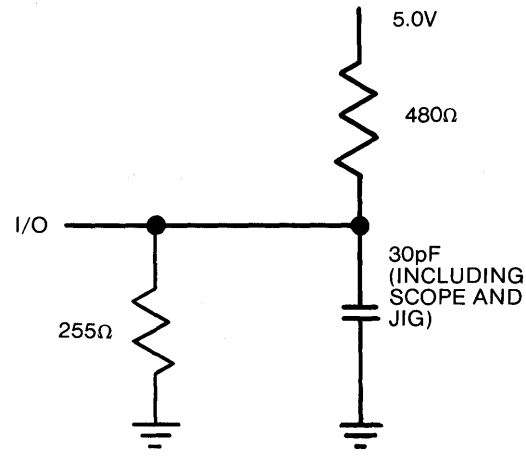
Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilizing a wideband oscilloscope and probe. When using WRITE CYCLE 1, care should be taken to avoid bus contention. When $\overline{W}$ goes high, with $\overline{E}$ low, the output buffers will be active t_{WHQX} after the rising edge of $\overline{W}$. Data out will be the same as the data just written, unless the address changes. If data-in from the previous cycle is still valid after the address changes, contention may result. Contention may also result if $\overline{E}$ goes low before $\overline{W}$, with Data-in valid early in the cycle. INMOS Application Note #5, "Bus Contention Considerations," provides a detailed analysis of contention and methods used to control bus contention.

ASYNCHRONOUS VS. SYNCHRONOUS OPERATION

Fast, high density Static RAMs have a finite probability of encountering transient (non-catastrophic) errors[1] particularly when operated in a totally asynchronous manner. Therefore, in applications where extremely low error rates are essential, it is recommended that synchronous operation be considered. Synchronous operation is accomplished by allowing address changes during device deselect intervals ($\overline{E}$ high) only.

[1]Chappell, Schuster, Sai-Halasz, "Stability and Soft Error Rates of SRAM Cells," ISSCC Digest of Technical Papers, p. 162-163; Feburary 1984.

FIGURE 1. OUTPUT LOAD



ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1423	25ns	PLASTIC DIP	IMS1423P-25
	25ns	CERAMIC DIP	IMS1423S-25
	25ns	CHIP CARRIER	IMS1423W-25
	35ns	PLASTIC DIP	IMS1423P-35
	35ns	CERAMIC DIP	IMS1423S-35
	35ns	CHIP CARRIER	IMS1423W-35
	45ns	PLASTIC DIP	IMS1423P-45
	45ns	CERAMIC DIP	IMS1423S-45
	45ns	CHIP CARRIER	IMS1423W-45

IMS1424

High Performance 4K x 4 CMOS Static RAM

with Output Enable

New Product Preview

FEATURES

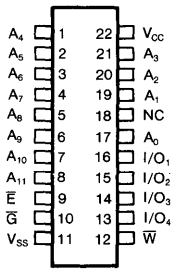
- INMOS Very High Speed CMOS
- Advanced Process—2 Micron Design Rules
- 4K x 4 Bit Organization
- 35nsec and 40nsec Address Access Times
- 35nsec and 45nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- Power Down Function
- 22 Pin, 300-mil DIP (Proposed JEDEC Standard)
- Output Enable Control to Eliminate Bus Contention

DESCRIPTION

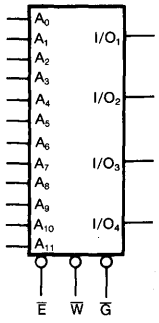
The IMS1424 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1424 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode. The IMS1424 also includes an Output Enable ($\overline{G}$) to eliminate bus contention. The IMS1424 is functionally equivalent to the IMS1423, with the addition of the $\overline{G}$ control function as a bonding option.

* JEDEC Standard Notation	Alternate Notation	Function
$\overline{E}$	$\overline{CE}$	Chip Enable
$\overline{W}$	$\overline{WE}$	Write Enable
$\overline{G}$	$\overline{OE}$	Output Enable

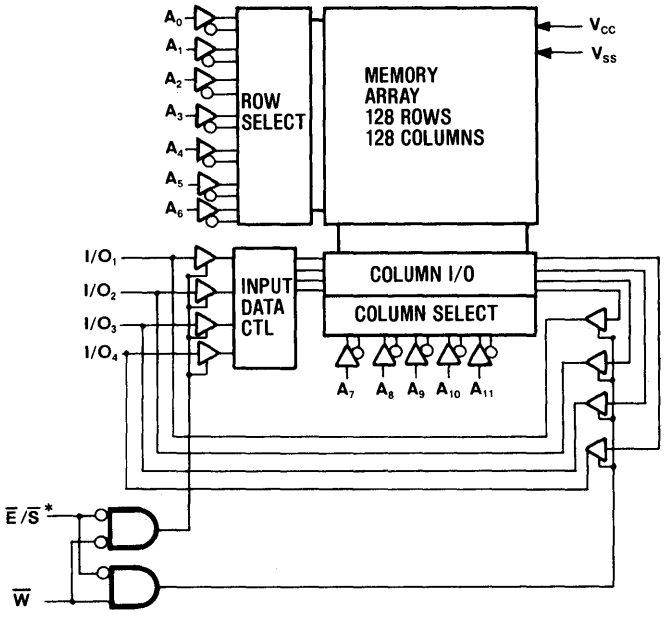
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$	CHIP ENABLE	$\overline{G}$	OUTPUT ENABLE
I/O	DATA IN/OUT		

IMS1403

High Performance 16K x 1 CMOS Static RAM

Preliminary

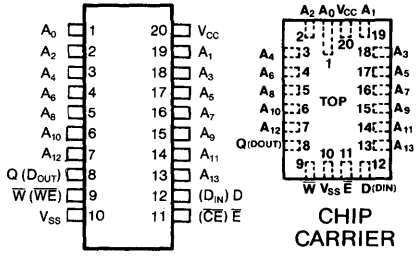
FEATURES

- INMOS Very High Speed CMOS
- Advanced Process—2 Micron Design Rules
- 16K x 1 Bit Organization
- 35, 45 and 55nsec Address Access Times
- 35, 45 and 55nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- 20-Pin, 300-mil DIP (JEDEC Standard Pinout)
- Single 5 volt ± 10% Operation
- Power Down Function
- Pin Compatible with IMS1400

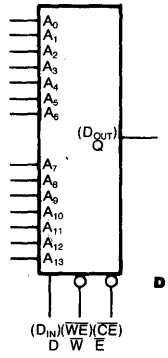
DESCRIPTION

The INMOS IMS1403 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1403 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode.

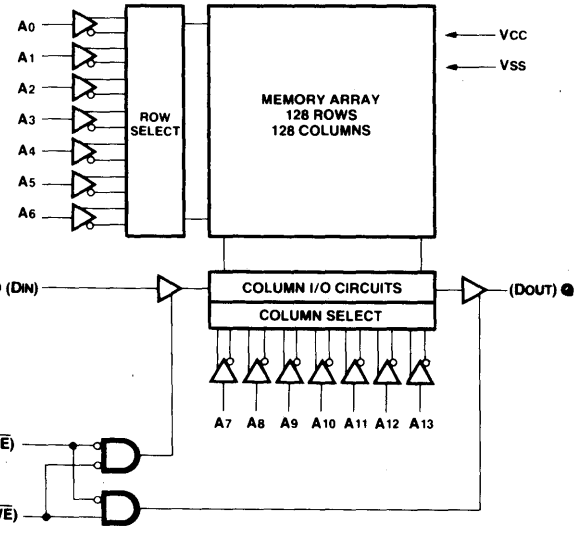
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{13} ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{W}$ ($\overline{WE}$) WRITE ENABLE	V_{SS} GROUND
$\overline{E}$ ($\overline{CE}$) CHIP ENABLE	
D (D_{IN}) DATA INPUT	
Q (D_{OUT}) DATA OUTPUT	

IMS1600

High Performance 64K x 1 CMOS Static RAM

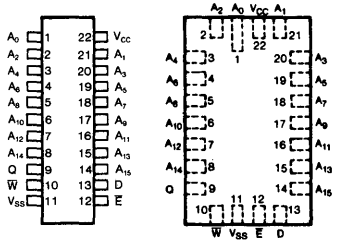
FEATURES

- INMOS Very High Speed CMOS
- Advanced Process—2 Micron Design Rules
- 64K x 1 Bit Organization
- 45, 55 and 70nsec Address Access Times
- 45, 55 and 70nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Output
- Three-state Output
- 22-Pin, 300-mil DIP (JEDEC Standard Pinout)
- Single +5V ± 10% Operation
- Power Down Function
- 440mW Maximum Power Dissipation
- 140mW Maximum Standby Power (Stable TTL Input Levels)
- 77mW Maximum Standby Power (Stable CMOS Input Levels)

DESCRIPTION

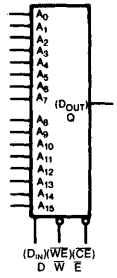
The IMS1600 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1600 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode, thus reducing power to 140mW. By using stable CMOS levels, the standby power may be reduced to an even lower 77mW.

PIN CONFIGURATION

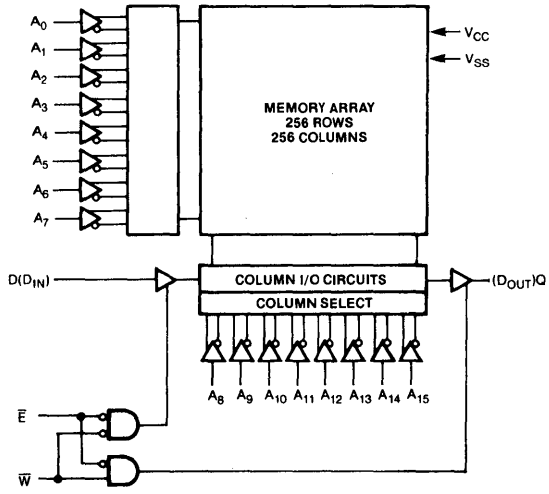


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{15}	ADDRESS INPUTS
$\overline{W}$	WRITE ENABLE
$\overline{E}$	CHIP ENABLE
D	DATA INPUT
Q	DATA OUTPUT
V_{CC}	POWER (+5V)

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −2.0 to 7.0V
Voltage on Q (Pin 9) . . . . . −1.0 to (V_{CC} + 0.5)
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temp. (Ceramic Package) . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current . . . . . 25mA (One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating onl and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification i not implied. Exposure to absolute maximum rating conditions for extende periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC} +.5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−1.0		0.8	V	All Inputs
T_A	Ambient Operating Temperature	0		70	°C	400 Linear ft./min. transverse air flow

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current AC		80 75 70	mA mA mA	t_{AVAV} = 45ns, a t_{AVAV} = 55ns, a t_{AVAV} = 70ns, a
I_{CC_2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		25	mA	$\overline{E} \geq 2.0V$ All Other Inputs 2.0V $\leq V_{IN} \leq 0.8V$
I_{CC_3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\overline{E} \geq (V_{CC} - 0.3V)$ All Other Inputs V_{CC} $-.3V \leq V_{IN} \leq 0.3V$
I_{CC_4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels) $\overline{E} \geq (V_{CC} - .3V)$		19 17 15	mA mA mA	t_{AVAV} = 45ns t_{AVAV} = 55ns t_{AVAV} = 70ns All Other Inputs Cycling from 0.3V to V_{CC} −.3V
I_{ILK}	Input Leakage		±10	µA	
I_{OLK}	Output Leakage		±50	µA	
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = −8mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

Note a: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with output unloaded.

AC TEST CONDITIONS[b]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

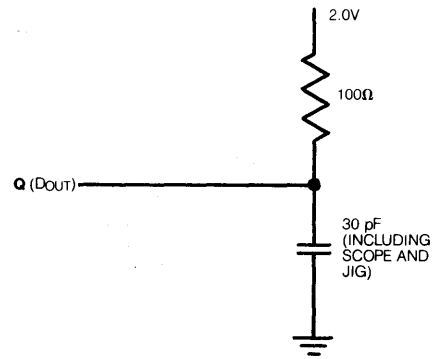
Note b: Operation to specifications guaranteed 500µS after $V_{CC} \geq 4.5$.

CAPACITANCE[c] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note c: This parameter is sampled and not 100% tested.

FIGURE 1. OUTPUT LOAD



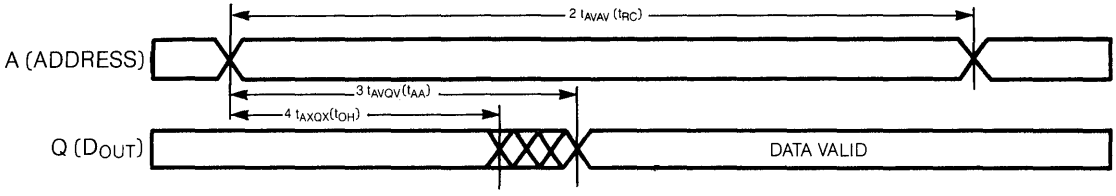
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE [h]

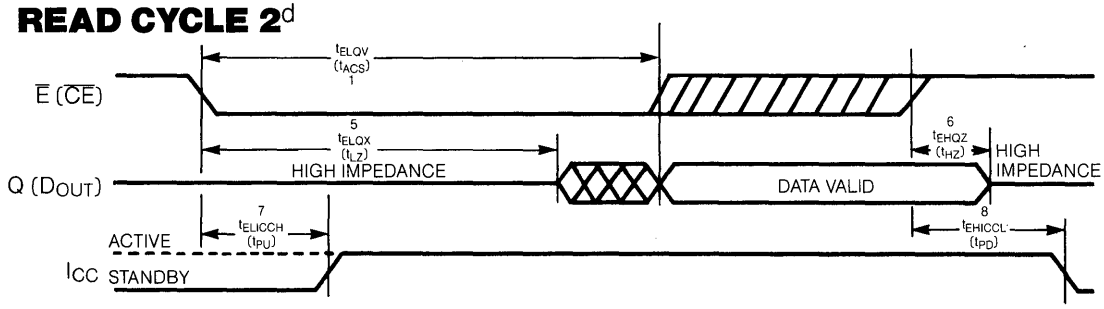
NO.	SYMBOL		PARAMETER	1600-45		1600-55		1600-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	45		55		70		ns	d
3	t_{AVQV}	t_{AA}	Address Access Time		45		55		70	ns	e
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	f
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Disable	0	25	0	30	0	30	ns	g
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	c
8	t_{EHICCL}	t_{PD}	Chip Disable To Power Down	0	45	0	55	0	70	ns	c
		t_T	Input Rise and Fall Times		50		50		50	ns	f

Note d: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note e: Device is continuously selected, $\overline{E}$ low.
Note f: Measured between reference levels of $V_{IL} = 0.8V$ and $V_{IH} = 2.0V$.
Note g: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.

READ CYCLE 1 [d,e]



READ CYCLE 2 [d]



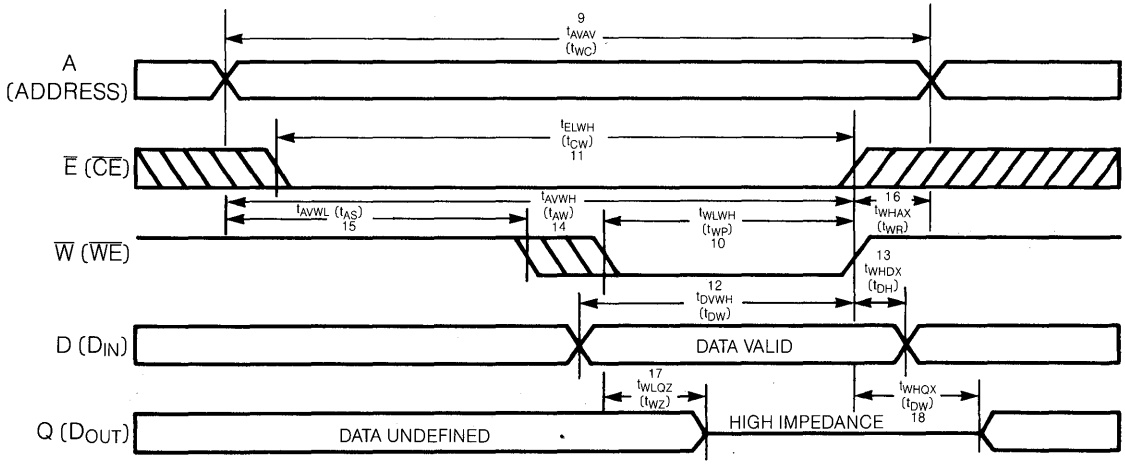
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ± 10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h, j]

NO.	SYMBOL		PARAMETER	1600-45		1600-55		1600-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		70		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		25		30		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		30		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	5		5		5		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		35		40		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	10		10		10		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	5		5		5		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	30	ns	g
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0	25	0	30	0	40	ns	i

Note g: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note i: If $\overline{E}$ goes high with $\overline{W}$ low, output remains in high impedance state.
Note j: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transition.

WRITE CYCLE 1



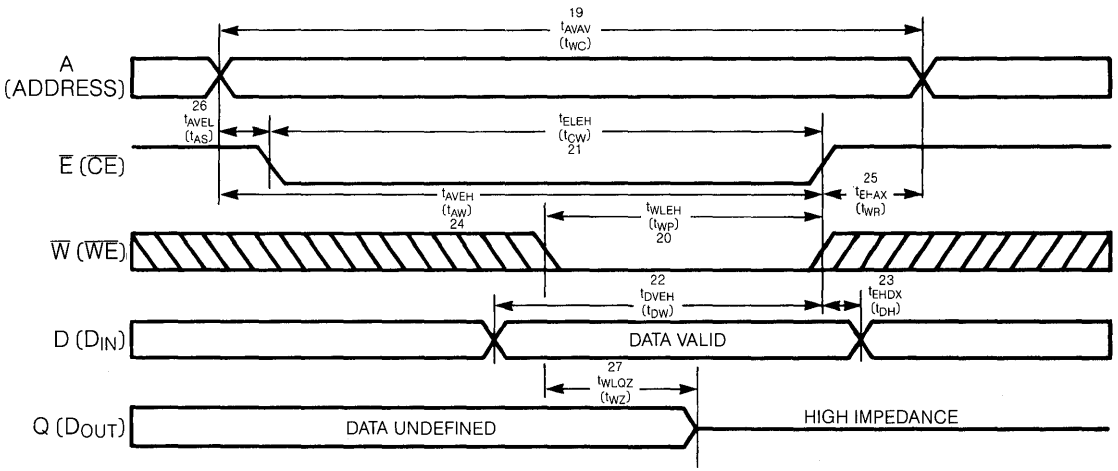
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h, j]

NO.	SYMBOL Standard	SYMBOL Alternate	PARAMETER	1600-45 MIN	1600-45 MAX	1600-55 MIN	1600-55 MAX	1600-70 MIN	1600-70 MAX	UNITS	NOTES
19	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		70		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		20		30		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	5		5		5		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	40		50		60		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	5		5		5		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	30	ns	g

Note g: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note j: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transition.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1600 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), sixteen address inputs (A_0-A_{15}), a data in (D_{IN}) and a data out (D_{OUT}).

The IMS1600 becomes active immediately after V_{CC} is applied, but proper operation is not guaranteed until after 500 microseconds after V_{CC} reaches 4.5 volts. The $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the sixteen address inputs are decoded to select one memory cell out of 65,536. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-third of the active mode power with TTL input levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from the latter of either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of t_{AXQX}. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

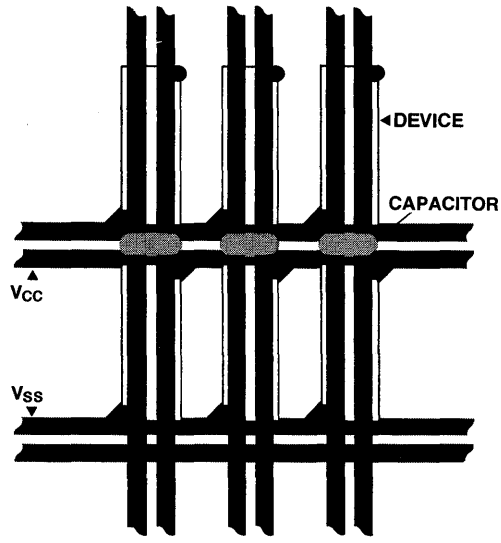
WRITE CYCLE

The write cycle of the IMS1600 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to fall. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Contention can be avoided in a carefully designed system. During a write cycle, data on the inputs is written into the selected cells and the outputs are floating.

If a write cycle is initiated by $\overline{W}$ going low, then the address must be valid for t_{AVWL} referenced to $\overline{W}$. If a write cycle is initiated by $\overline{E}$ going low, the address must be stable for t_{AVEL} referenced to $\overline{E}$. The address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If the set-up and hold times are not met, for either address or data, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of the memory becomes active. The data from the memory will be the same as the input data, unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1600, that the fundamental rules of good engineering practice be followed in areas such as board layout and signal fidelity to ensure proper system operation.

TTL VS. CMOS INPUT LEVELS

The IMS1600 is fully compatible with TTL input levels. The input circuitry of the IMS1600 is designed for maximum speed and also for conversion of TTL level signals to the CMOS levels required for internal operation. The IMS1600 consumes less power when CMOS levels (.3/V_{CC} −.3 volts) are used than TTL levels (.8/2.0 volts) are applied. The lower CMOS I_{CC} specifications, I_{CC3} and I_{CC4}, may be achieved by using CMOS levels, i.e., inputs within .3 volts of either supply. The power consumption will be lower at typical TTL levels than at the worst case levels.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1600. The impedance in the decoupling path from the power pin (22) through the decoupling capactor to the ground pin (11) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1600 have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients, therefore should be located as near the device and with as short lead lengths as practical. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing.

ASYNCHRONOUS VS. SYNCHRONOUS OPERATION

Fast, high density memory devices have a finite probability of encountering transient (non-catastrophic) errors[1] particularly when operated in a totally asynchronous manner. Therefore, in applications where extremely low error rates are essential, it is recommended that synchronous operation be considered. Synchronous operation is accomplished by allowing address changes during device deselect intervals ($\overline{E}$ high) only.

[1]Chappell, Schuster, Sai-Halasz, "Stability and Soft Error Rates of SRAM Cells," ISSCC Digest of Technical Papers, p. 162-163; Feburary 1984.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1600	45ns	CERAMIC DIP	IMS1600S-45
	45ns	CHIP CARRIER	IMS1600W-45
	55ns	CERAMIC DIP	IMS1600S-55
	55ns	CHIP CARRIER	IMS1600W-55
	70ns	CERAMIC DIP	IMS1600S-70
	70ns	CHIP CARRIER	IMS1600W-70

IMS1620
High Performance 16K x 4 CMOS Static RAM

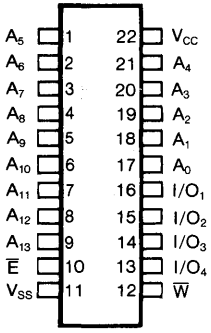
FEATURES

- INMOS Very High Speed CMOS
- Advanced Process—2 Micron Design Rules
- 16K x 4 Bit Organization
- 45, 55 and 70nsec Address Access Times
- 45, 55 and 70nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Single 5 volt ± 10% Operation
- Power Down Function
- 22-Pin, 300-mil DIP (JEDEC Standard)

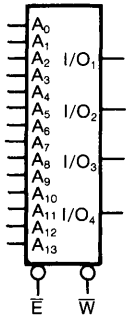
DESCRIPTION

The IMS1620 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1620 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode.

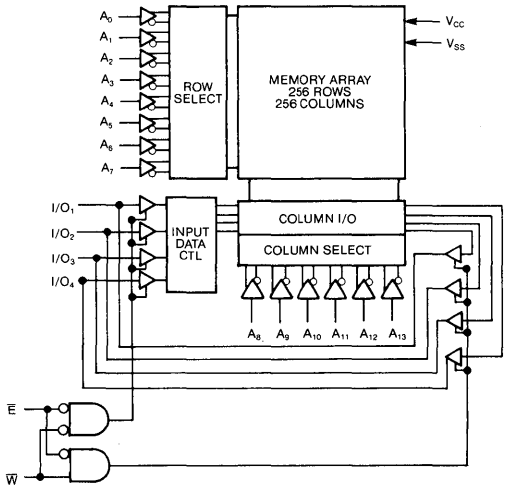
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
I/O	DATA IN/OUT		
$\overline{E}$	CHIP ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −2.0 to 7.0V
Voltage on I/O (Pins 13-16) . . . . . −1.0 to (V_{CC} + .5V)
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current . . . . . 25mA (One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC} + .5	V	
V_{IL}	Input Logic "0" Voltage	−1.0		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	400 Linear ft./min. transverse air flow

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC		80 75 70	mA mA mA	t_{AVAV} = 45ns, a t_{AVAV} = 55ns, a t_{AVAV} = 70ns, a
I_{CC2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		25	mA	$\overline{E} \geq 2.0V$ All Other Inputs $2.0V \leq V_{IN} \leq 0.8V$
I_{CC3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\overline{E} \geq (V_{CC} - 0.3V)$ All Other Inputs $V_{CC} - .3V \leq V_{IN} \leq .3V$
I_{CC4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels) $\overline{E} \geq (V_{CC} - .3V)$		19 17 15	mA mA mA	t_{AVAV} = 45ns, a t_{AVAV} = 55ns, a t_{AVAV} = 70ns, a All Other Inputs Cycling from 0.3V to V_{CC} −.3V
I_{IN}	Input Leakage Current (Any Input)	−10	10	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	µA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = −4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS[a]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

Note a: Operation to specifications guaranteed 500µs after $V_{CC} \geq 4.5$.

CAPACITANCE[b] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

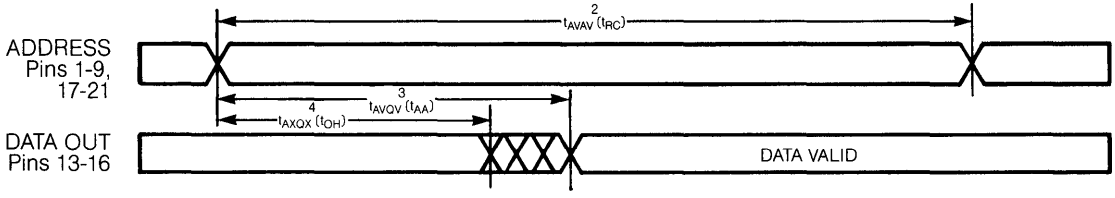
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[h]

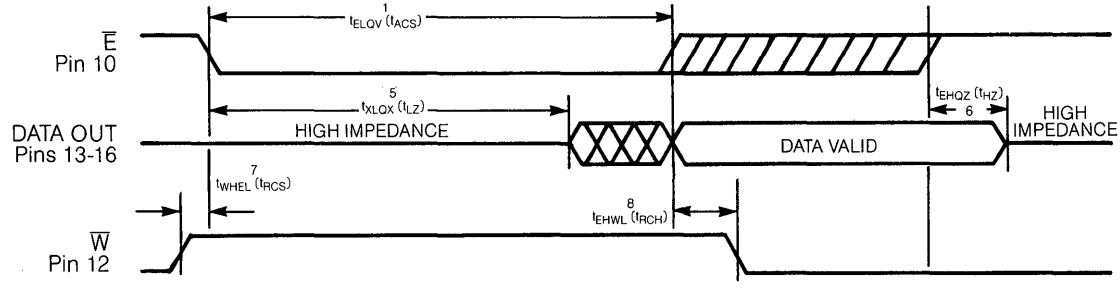
NO.	SYMBOL		PARAMETER	1620-45		1620-55		1620-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	45		55		70		ns	d
3	t_{AVQV}	t_{AA}	Address Access Time		45		55		70	ns	e
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		3		ns	f
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	3		3		3		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	25	0	25	ns	g
7	t_{WHEL}	t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
8	t_{EHWL}	t_{RCH}	Read Command Hold Time	0		0		0		ns	
9	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0			
10	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		45		55		70		
		t_T	Input Rise and Fall Times		50		50		50	ns	f

Note d: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note e: Device is continuously selected $\overline{E}$ low.
Note f: Measured between V_{IL} max and V_{IH} min.
Note g: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



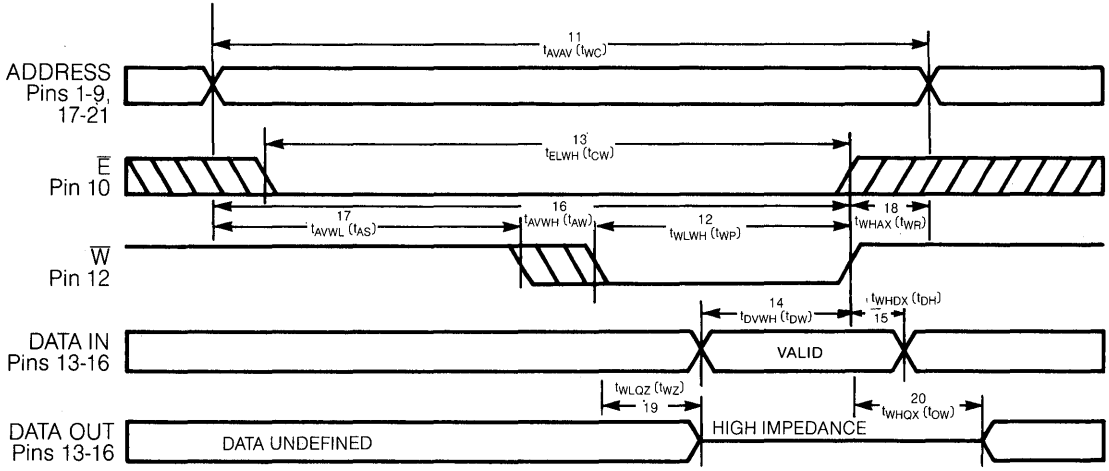
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ± 10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h, i]

NO.	SYMBOL		PARAMETER	1620-45		1620-55		1620-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
11	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		70		ns	
12	t_{WLWH}	t_{WP}	Write Pulse Width	40		50		60		ns	
13	t_{ELWH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
14	t_{DVWH}	t_{DW}	Data Set-up to End of Write	20		25		25		ns	
15	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
16	t_{AVWH}	t_{AW}	Address Set-up to End of Write	35		45		50		ns	
17	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
18	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
19	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	25	ns	g
20	t_{WHQX}	t_{OW}	Output Active After End of Write	0		0		0		ns	j

Note g: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note i: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note j: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.

WRITE CYCLE 1



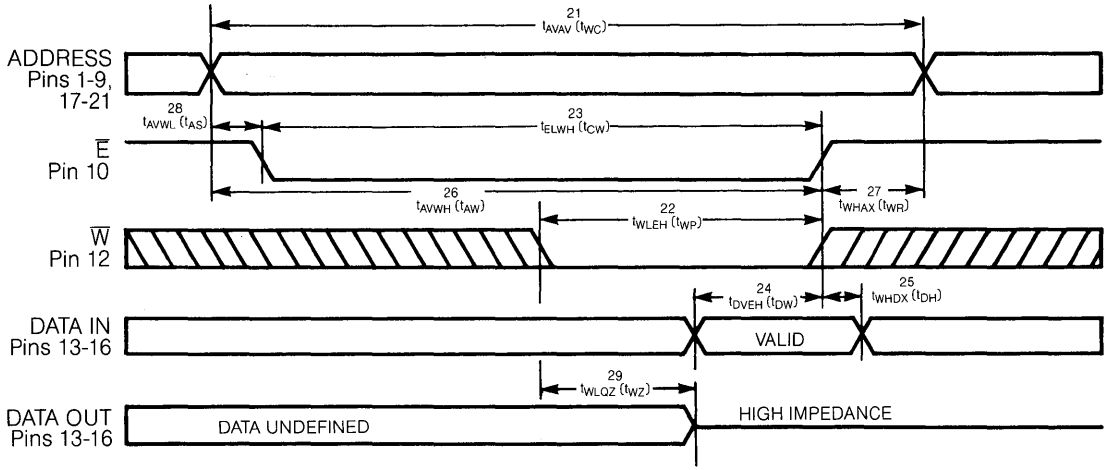
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h, i]

NO.	SYMBOL		PARAMETER	1620-45		1620-55		1620-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
21	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		70		ns	
22	t_{WLEH}	t_{WP}	Write Pulse Width	40		50		60		ns	
23	t_{ELEH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
24	t_{DVEH}	t_{DW}	Data Set-up to End of Write	20		25		25		ns	
25	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
26	t_{AVEH}	t_{AW}	Address Set-up to End of Write	35		45		50		ns	
27	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
28	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
29	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	25	ns	g

Note g: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note i: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1620 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), fourteen address inputs (A_0 - A_{13}), and four Data I/O lines.

The IMS1620 becomes active immediately after V_{CC} is applied, with proper operation assured 500 microseconds after V_{CC} reaches 4.5 volts. With $\overline{E}$ low, the device is selected and the fourteen address inputs are decoded to select one 4-bit word out of 16,384. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min. with $\overline{E} \leq V_{IL}$ max. Read access time is measured from the latter of either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of t_{AXQV}. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

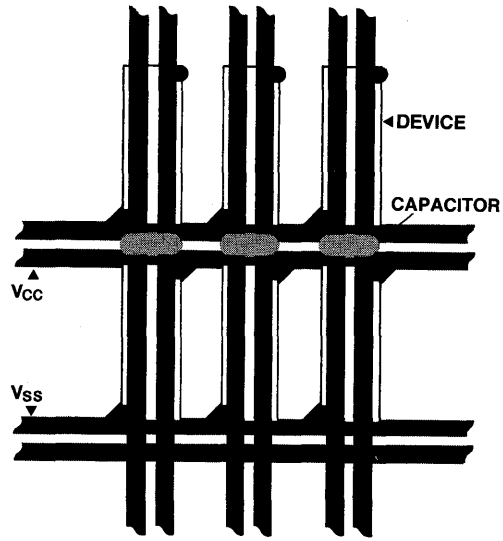
WRITE CYCLE

The write cycle of the IMS1620 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high level to a low level. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common input/output connections. Therefore input data should not be active until after t_{WLQZ} to avoid bus contention. During a write cycle, data on the inputs is written into the selected cells and the outputs are floating.

If a write cycle is initiated by $\overline{E}$ going low, the address must be stable for t_{AVEL} referenced to $\overline{E}$. If the write cycle is initiated by $\overline{W}$ going low, then the address must be valid for t_{AVWL} referenced to $\overline{W}$. The address must be held stable for the entire write cycle. After either $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If set-up and hold times are not met, for either address or data, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high while $\overline{E}$ is low, the outputs become active. When $\overline{W}$ goes high at the end of a write cycle and the outputs of the memory go active, the data from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high the outputs remain in the high impedance state.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1620, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

TTL VS. CMOS INPUT LEVELS

The IMS1620 is fully compatible with TTL input levels. The input circuitry of the IMS1620 is designed for maximum speed and also for conversion of TTL level signals to the CMOS levels required for internal operation. The IMS1620 consumes less power when CMOS levels (.3/V_{CC} −.3 volts) are used than TTL levels (.8/2.0 volts) are applied. The lower CMOS I_{CC} specifications, I_{CC3} and I_{CC4}, may be achieved by using CMOS levels. The power consumption will be lower at typical TTL levels than at the worst case levels.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the wide operating margins of the IMS1620. The impedance in the decoupling path from the power pin (22) through the decoupling capacitor to the ground pin (11) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1620 have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as near the memory as possible, with the shortest lead lengths practical. The high frequency decoupling capacitor should have a minimum value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor, for low frequency current transients, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The termination resistor should be placed as close to the driver package as possible. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33ohm range will be required. Because the characteristic impedance of each layout will be different, it is necessary to select the proper value of this resistor by trial and error. A resistor of predetermined value may not properly terminate the transmission line.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilizing a wideband oscilloscope and probe.

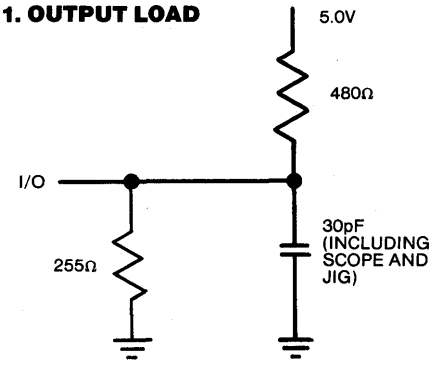
When using WRITE CYCLE 1, care should be taken to avoid bus contention. When $\overline{W}$ goes high, with $\overline{E}$ low, the output buffers will be active t_{WHQX} after the rising edge of $\overline{W}$. Data out will be the same as the data just written, unless the address changes. If Data-in from the previous cycle is still valid after the address changes, contention may result. Contention may also result if $\overline{E}$ goes low before $\overline{W}$, with Data-in valid early in the cycle. INMOS Application Note #5, "Bus Contention Considerations," provides a detailed analysis of contention and methods used to control bus contention.

ASYNCHRONOUS VS. SYNCHRONOUS OPERATION

Fast, high density Static RAMs have a finite probability of encountering transient (non-catastrophic) errors[1] particularly when operated in a totally asynchronous manner. Therefore, in applications where extremely low error rates are essential, it is recommended that synchronous operation be considered. Synchronous operation is accomplished by allowing address changes during device deselect intervals ($\overline{E}$ high) only.

[1]Chappell, Schuster, Sai-Halasz, "Stability and Soft Error Rates of SRAM Cells," ISSCC Digest of Technical Papers, p. 162-163; Feburary 1984.

FIGURE 1. OUTPUT LOAD



ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1620	45ns	CERAMIC DIP	IMS1620S-45
	45ns	CHIP CARRIER	IMS1620W-45
	55ns	CERAMIC DIP	IMS1620S-55
	55ns	CHIP CARRIER	IMS1620W-55
	70ns	CERAMIC DIP	IMS1620S-70
	70ns	CHIP CARRIER	IMS1620W-70

IMS1624

High Performance 16K x 4 CMOS Static RAM

with Output Enable

Also available screened to MIL-STD-883C

New Product Preview

FEATURES

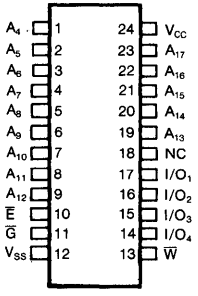
- INMOS Very High Speed CMOS
- Advanced Process—2 Micron Design Rules
- 16K x 4 Bit Organization
- 45, 55 and 70nsec Address Access Times
- 45, 55 and 70nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- Power Down Function
- 24 Pin, 300-mil DIP (Proposed JEDEC Standard)
- Output Enable Control to Eliminate Bus Contention

DESCRIPTION

The IMS1624 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1624 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode. The IMS1624 also includes an Output Enable ($\overline{G}$) to eliminate bus contention. The IMS1624 is functionally equivalent to the IMS1620, with the addition of the $\overline{G}$ control function as a bonding option.

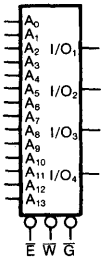
* JEDEC Standard Notation	Alternate Notation	Function
$\overline{E}$	$\overline{CE}$	Chip Enable
$\overline{W}$	$\overline{WE}$	Write Enable
$\overline{G}$	$\overline{OE}$	Output Enable

PIN CONFIGURATION

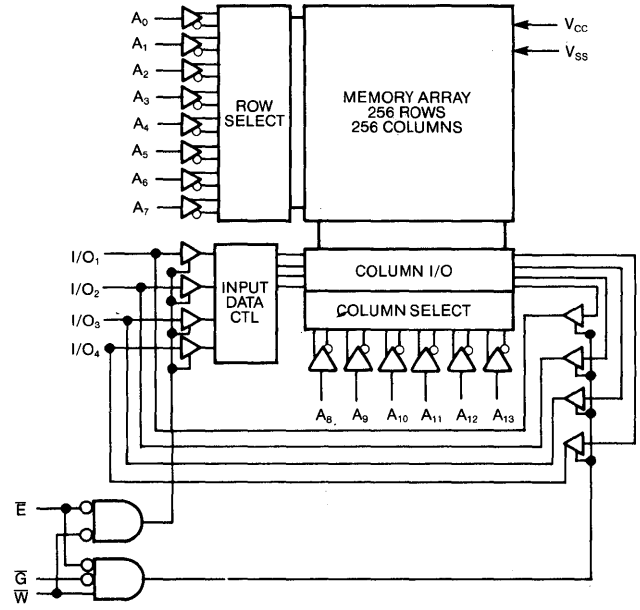


DIP

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$	CHIP ENABLE	$\overline{G}$	OUTPUT ENABLE
I/O	DATA IN/OUT		

IMS1601

High Performance Low Power/Data Retention 64K x 1 CMOS Static RAM

Also available screened to MIL-STD-883C

New Product Preview

FEATURES

- INMOS Very High Speed CMOS
- Advanced Process—2 Micron Design Rules
- 64K x 1 Bit Organization
- 55 and 70nsec Address Access Times
- 55 and 70nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Output
- Three-state Output
- 22-Pin, 300-mil DIP (JEDEC Standard Pinout)
- Single +5V ± 10% Operation
- Power Down Function at 5V
- 2V (Min) battery back up/data retention mode
- 30μW (Max) power dissipation with a 3V battery

DESCRIPTION

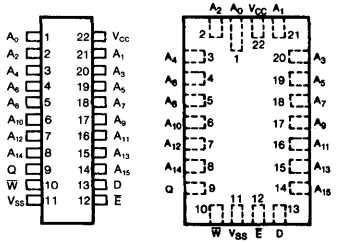
The IMS1601 is a high performance 64K x 1 static RAM with a battery back up/low power mode and guaranteed data retention to 2 volts.

The IMS1601 features fully static operation requiring no external clocks or strobes, and equal access and cycle times of 55 or 70 nanoseconds. The device is also fully TTL compatible and operates from a single 5 volt supply in its standard mode. For systems requiring battery back-up operation, the IMS1601 has been optimized to provide the user with ultra low power. When using a 3 volt battery the device has a maximum standby current of 10 micro amps at room temperature. Additionally, the Chip Enable function is provided to place the IMS1601 into a normal supply (V_{CC}=5V) low power standby mode.

The IMS1601 is packaged in a 22-pin, 300-mil CDIP and also available in a 22-pin leadless ceramic chip carrier, for high board density applications.

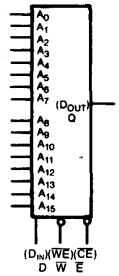
The IMS1601 is a VLSI RAM intended for battery back-up/low power applications in additon to providing superior performance under normal operating conditions.

PIN CONFIGURATION

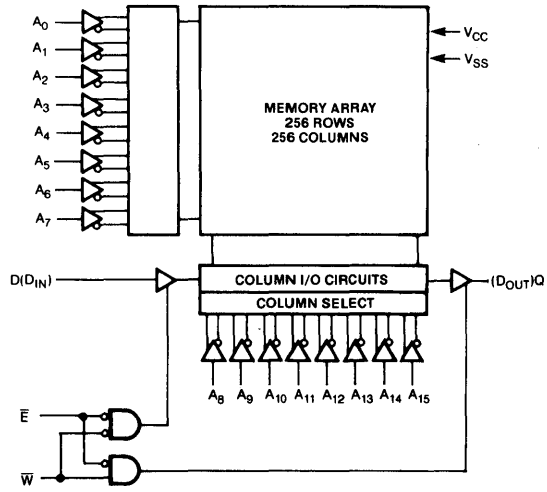


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{15} ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{W}$ WRITE ENABLE	
$\overline{E}$ CHIP ENABLE	
D DATA INPUT	
Q DATA OUTPUT	

Dynamic RAMs 2

DRAM Selection Guide

Device	Organization	Access Times (ns)	Maximum Current (mW)		Power Supply Volts	Number of Pins	Package Type	Process	Page No.
			Active	Standby					
IMS2600P	64K x 1	80,100,120	303	22	+5	16	P	NMOS	2-3
IMS2600S	64K x 1	100,120	303	22	+5	16	S	NMOS	2-3
IMS2600W	64K x 1	100,120	303	22	+5	18	W (A)	NMOS	2-3
IMS2620P	16K x 4	100,120,150	330	28	+5	18	P	NMOS	2-15
IMS2630P	8K x 8	120,150,200	275	42	+5	28	P	NMOS	2-23
IMS2800P	256K x 1	60,80,100,120,150	350	10 CMOS	+5	16	P	CMOS	2-31
IMS2800S	256K x 1	60,80,100,120,150	350	10 CMOS	+5	16	S	CMOS	2-31
IMS2800W	256K x 1	60,80,100,120,150	350	10 CMOS	+5	18	W (B)	CMOS	2-31
IMS2800J	256K x 1	60,80,100,120,150	350	10 CMOS	+5	18	J	CMOS	2-31
IMS2801P	256K x 1	60,80,100,120,150	350	10 CMOS	+5	16	P	CMOS	2-43
IMS2801S	256K x 1	60,80,100,120,150	350	10 CMOS	+5	16	S	CMOS	2-43
IMS2801W	256K x 1	60,80,100,120,150	350	10 CMOS	+5	18	W (B)	CMOS	2-43
IMS2801J	256K x 1	60,80,100,120,150	350	10 CMOS	+5	18	J	CMOS	2-43

NOTES:
P = Plastic DIP
J = Plastic Chip Carrier
S = Ceramic DIP
W = Ceramic Chip Carrier

IMS2600

High Performance 64Kx1 Dynamic RAM

inmos®

FEATURES

- High Speed, $\overline{RAS}$ Access of 80, 100, 120 and 150ns
- Cycle Times of 130, 160, 190 and 230ns
- Low Power:
  22mW Standby
  303mW Active (350ns Cycle Time)
  413mW Active (190ns Cycle Time)
- Single +5V ± 10% Power Supply
- On-Chip refresh using $\overline{CAS}$-before-$\overline{RAS}$, Pin 1 left as N/C for 256K expansion
- Indefinite D_{OUT} Hold Under $\overline{CAS}$ Control
- Industry Standard 16 Pin Configuration
- Nibble-Mode Capability (High Speed 4 Bit Serial Mode)
- 4ms/256 Cycle Refresh
- All Inputs and Output TTL Compatible
- Read, Write, Read-Modify-Write Capability both on Single Bit and in Nibble Mode Operation
- $\overline{RAS}$-Only Refresh Capability
- Common I/O Capability using "Early-Write"

DESCRIPTION

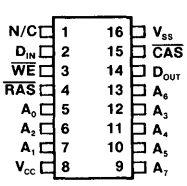
The IMS2600 64K x 1 bit dynamic RAM is fabricated with INMOS' advanced N-MOS technology and utilizes innovative circuit techniques to achieve high performance, low power and wide operating margins. Multiplexed addressing allows the IMS2600 to be packaged in a standard 16-pin DIP. Additionally, the IMS2600 features new functional enhancements that make it more versatile than previous dynamic RAMs. $\overline{CAS}$-before-$\overline{RAS}$ refresh provides an on-chip refresh mechanism that is upward compatible to 256K dynamic RAMs because pin 1 is left as a no-connect. The IMS2600 also features "nibble mode" which allows high speed serial access of up to 4 bits of data, thus providing the system equivalent of 4-way interleaving on chip.

The output of the IMS2600 can be held valid for an indefinite period by holding $\overline{CAS}$ low. This facilitates hidden-refresh operations and, when used with $\overline{CAS}$-before-$\overline{RAS}$ refresh, can greatly reduce the number of memory interface circuits.

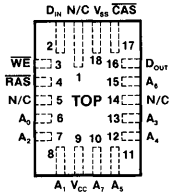
The IMS2600 is fully TTL compatible on all inputs and the output, and operates from a single +5V ± 10% power supply.

The IMS2600 is a cost-effective VLSI RAM intended for applications that demand high density as well as superior performance and reliability.

PIN CONFIGURATION

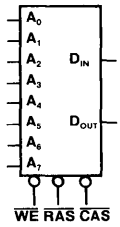


DIP

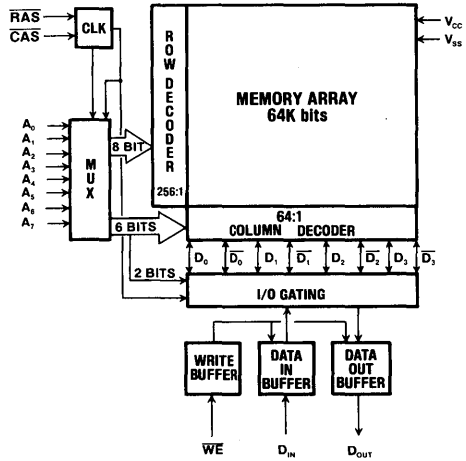


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5 VOLT SUPPLY INPUT
V_{SS}	GROUND

DEVICE OPERATION

The IMS2600 contains 65536 (2^{16}) bits of information as 256 (2^8) rows by 256 (2^8) columns. The sixteen addresses for unique bit selection are time-division multiplexed over eight adress lines under control of the Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$) clocks. The normal sequence of $\overline{RAS}$ and $\overline{CAS}$ requires that $\overline{CAS}$ is high as $\overline{RAS}$ goes low. This causes the eight address inputs to be latched and decoded for selection of one of the 256 rows. The row addresses must be held for the specified period [t_{RAH} (min)] and then they may be switched to the appropriate column address. After the column addresses are stable for the specified column address setup time, $\overline{CAS}$ may be brought low. This causes the eight address inputs to be latched and used to select a single column in the specified row. The cycle is terminated by bringing $\overline{RAS}$ high. A new cycle may be initiated after $\overline{RAS}$ has been high for the specified precharge interval [(t_{RP} (min)]. $\overline{RAS}$ and $\overline{CAS}$ must be properly overlapped and once brought low they must remain low for their specified pulse widths.

READ CYCLE

A read cycle is performed by sequencing $\overline{RAS}$ and $\overline{CAS}$ as described above while holding the $\overline{WE}$ input high during the period when $\overline{RAS}$ and $\overline{CAS}$ are both low. The read access time will be determined by the actual timing relationship between $\overline{RAS}$ and $\overline{CAS}$. If $\overline{CAS}$ goes low within the specified $\overline{RAS}$-to-$\overline{CAS}$ delay [t_{RCD} (max)], then the access time will be determined by $\overline{RAS}$ and be equal to t_{RAC} (max). If $\overline{CAS}$ occurs later than t_{RCD} (max) then the access time is measured from $\overline{CAS}$ and will be equal to t_{CAC} (max).

WRITE CYCLE

The IMS2600 will perform three types of write cycles: Early-Write, Late-Write or Read-Modify-Write. The difference between these cycles is that on an Early-Write D_{OUT} will remain open and on a Late-Write or Read-Modify-Write D_{OUT} will reflect the contents of the addressed cell before it was written.

The type of write cycle that is performed is determined by the relationship between $\overline{CAS}$ and $\overline{WE}$. For Early-Write cycles $\overline{WE}$ occurs before $\overline{CAS}$ goes low, and D_{IN} setup is referenced to the falling edge of $\overline{CAS}$. For Late-Write or Read-Modify-Write cycles $\overline{WE}$ occurs after $\overline{CAS}$, and D_{IN} setup is referenced to the falling edge of $\overline{WE}$.

The choice of write cycle timing is usually very system dependent and the different modes are made available to accommodate these differences. In general, the Early-Write timing is most appropriate for systems that have a bidirectional data bus. Because D_{OUT} remains inactive during Early-Write cycles, the D_{IN} and D_{OUT} pins may be tied together without bus contention.

DEVICE SELECTION AND OUTPUT CONTROL

Selection of a memory device for a read or write operation requres that both $\overline{RAS}$ and $\overline{CAS}$ be sequenced. A device is not selected if $\overline{RAS}$ is sequenced while $\overline{CAS}$ remains high or if $\overline{CAS}$ is sequenced while $\overline{RAS}$ remains high. The device must receive a properly overlapped $\overline{RAS}/\overline{CAS}$ sequence to be selected.

Once a device is selected the state of D_{OUT} becomes entirely controlled by $\overline{CAS}$. As long as $\overline{CAS}$ remains low D_{OUT} will remain in the state that it had when $\overline{RAS}$ went high at the end of the cycle in which it was selected. This is true even if a $\overline{RAS}$ sequence occurs while $\overline{CAS}$ is held low.

REFRESH

The IMS2600 remembers data by storing charge on a capacitor. Because the charge will leak away over a period of time it is necessary to access the data in the cell (capacitor) periodically in order to fully restore the stored charge while it is still at a sufficiently high level to be properly detected. For the IMS2600 any $\overline{RAS}$ sequence will fully refresh an entire row of 256 bits. To ensure that all cells remain sufficiently refreshed, all 256 rows must be refreshed every 4 ms.

The addressing of the rows for refresh may be sourced either externally or internally. If the row refresh addresses are to be provided from an external source, $\overline{CAS}$ must be high when $\overline{RAS}$ goes low. If $\overline{CAS}$ is high when $\overline{RAS}$ goes low, any type of cycle (Read, Write, Read-Modify-Write or $\overline{RAS}$ only) will cause the addressed row to be refreshed.

If $\overline{CAS}$ is low when $\overline{RAS}$ falls, the IMS2600 will use an internal 8-bit counter as the source of the row addresses and will ignore the address inputs. This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh-only mode and no data access is allowed. Also, $\overline{CAS}$-before-$\overline{RAS}$ refresh does not cause device selection and the state of D_{OUT} will remain unchanged.

NIBBLE MODE

The IMS2600 is designed to allow high-speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during Nibble Mode are determined by the eight row addresses and the most significant 6 bits of the column address. The low-order 2 bits of the column address (A_3, A_6) are used to select one of the 4 nibble bits for initial access. After the first bit is accessed the remaining nibble bits may be accessed by bringing $\overline{CAS}$ high then low (toggle) while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes A_3 and A_6 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for read, write and/or read-modify-write access (See Table 1 for example). If more than 4 bits are accessed during Nibble Mode, the address sequence will begin to repeat. If any bit is written during an access, the new value will be read on any subsequent accesses.

In Nibble Mode, read, write and read-modify-write operations may be performed in any desired combination. (e.g., first bit read, second bit write, third bit read-modify-write, etc.)

Table 1
NIBBLE MODE ADDRESSING SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	ROW ADDRESSES	COLUMN ADDRESSES (A_3, A_6)	
$\overline{RAS}/\overline{CAS}$	1	10101010	10101010	generated externally
toggle $\overline{CAS}$	2	10101010	10101010	generated internally
toggle $\overline{CAS}$	3	10101010	10101010	
toggle $\overline{CAS}$	4	10101010	10101010	
toggle $\overline{CAS}$	1	10101010	10101010	sequence repeats

ABSOLUTE MAXIMUM RATINGS*[a]

Voltage on V_{CC} Relative to V_{SS} . . . . . −1.0V to +7.0V
Storage Temp. (Ceramic Package) −65°C to +150°C
Storage Temp. (Plastic Package) . −55°C to +125°C
Power Dissipation. 1W
Short Circuit Output Current. 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS[a, b]

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage		0		V	
V_{IH}	Logic "1" Voltage	2.4		V_{CC} + 1	V	
V_{IL}	Logic "0" Voltage	−2.0		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	Still Air

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current (Operating)	IMS2600-80		95	mA	t_{RC} = 130ns, t_{RAS} = 80ns (c)
		IMS2600-10		85		t_{RC} = 160ns, t_{RAS} = 100ns
		IMS2600-10		55		t_{RC} = 350ns, t_{RAS} = 100ns
		IMS2600-12		75		t_{RC} = 190ns, t_{RAS} = 120ns
		IMS2600-12		55		t_{RC} = 350ns, t_{RAS} = 120ns
		IMS2600-15		65		t_{RC} = 230ns, t_{RAS} = 150ns
		IMS2600-15		55		t_{RC} = 350ns, t_{RAS} = 150ns
I_{CC_2}	V_{CC} Power Supply Current (Active)			20	mA	$RAS \leq V_{IL}$ (max), $CAS \leq V_{IL}$ (max)
I_{CC_3}	Standby Current			4.0	mA	$RAS \geq V_{IH}$ (min), $CAS \geq V_{IH}$ (min)
I_{IN}	Input Leakage Current (Any Input)		−10	10	µA	$0V \leq V_{IN} \leq 5.5V$, others = 0V
I_{OLK}	Output Leakage Current		−10	10	µA	D_{OUT} = Hi Z, $0V \leq V_{OUT} \leq 5.5V$
V_{OH}	Output High Voltage		2.4		V	$I_O = -5.0mA$
V_{OL}	Output Low Voltage			0.4	V	$I_O = 5.0mA$

Note a: All voltage values in this data sheet are with respect to V_{SS}.
b: After power-up, a pause of 500 µs followed by eight initialization memory cycles is required to achieve proper device operation. Any interval greater than 4ms with $\overline{RAS}$ inactivity requires eight reinitialization cycles to achieve proper device operation.
c: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with output open.

AC TEST CONDITIONS

Input Pulse Levels. . . . . 0 to 3V
Input Rise and Fall Times. . . . . 5ns between 0.8 and 2.4V
Input Timing Reference Levels. . . . . 0.8 and 2.4V
Output Timing Reference Levels. . . . . 0.8 and 2.4V
Output Load. . . . . Equivalent to 2 TTL Loads and 50pF

CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS	COND.
C_{IN}	Input Cap. $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	6	pF	d
C_{IN}	Input Cap. Addresses	5	pF	d
C_{OUT}	Output Cap.	7	pF	d o

Note d: Capacitance measured with BOONTON METER.
o: $\overline{CAS} = V_{IH}$ to disable D_{OUT}

AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2600-80		2600-10		2600-12		2600-15		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{RC}	Random Read Cycle Time	130		160		190		230		ns	
2	t_{RAC}	Access Time from $\overline{RAS}$		80		100		120		150	ns	h
3	t_{CAC}	Access Time from $\overline{CAS}$		50		60		75		75	ns	i
4	t_{RAS}	$\overline{RAS}$ Pulse Width		80	100	10K	120	10K	150	10K	ns	
5	t_{RSH}	$\overline{RAS}$ Hold Time	50		60		75		75		ns	
6	t_{CAS}	$\overline{CAS}$ Pulse Width	50		60		75		75		ns	
7	t_{CSH}	$\overline{CAS}$ Hold Time	80		100		120		150		ns	
8	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	12	30	15	40	17	45	20	75	ns	e j
9	t_{CRS}	$\overline{CAS}$ to $\overline{RAS}$ Set-up Time	0		0		0		0		ns	
10	t_{RP}	$\overline{RAS}$ Precharge Time	40		50		60		70		ns	
11	t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
12	t_{RAH}	Row Address Hold Time	8		10		12		15		ns	
13	t_{ASC}	Column Address Set-up Time	−5		−5		−5		−5		ns	
14	t_{CAH}	Column Address Hold Time (Ref. $\overline{CAS}$)	20		25		35		45		ns	
15	t_{AR}	Column Address Hold Time (Ref. $\overline{RAS}$)	45		55		75		95		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		0		ns	
17	t_{RCH}	Read Command Hold Time (Ref. $\overline{CAS}$)	0		0		0		0		ns	k
18	t_{RRH}	Read Command Hold Time (Ref. $\overline{RAS}$)	0		0		0		0		ns	k
19	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	25	0	25	0	30	ns	f
20	t_{WCS}	Write Command Set-up Time	0		0		0		0		ns	m
21	t_{WCH}	Write Command Hold Time (Ref. $\overline{CAS}$)	20		25		30		35		ns	
22	t_{WCR}	Write Command Hold Time (Ref. $\overline{RAS}$)	45		55		70		85		ns	
23	t_{WP}	Write Pulse Width	18		20		25		30		ns	
24	t_{DS}	Data-in Set-up Time	0		0		0		0		ns	l
25	t_{DH}	Data-in Hold Time (Ref. $\overline{CAS}$)	20		25		30		35		ns	l
26	t_{DHR}	Data-in Hold Time (Ref. $\overline{RAS}$)	45		55		70		85		ns	
27	t_{RW}	Read-Write Cycle Time	150		180		215		260		ns	
27	t_{RMW}	Read-Modify-Write Cycle Time	155		190		255		270		ns	
28	t_{RRW}	Read-Write Cycle $\overline{RAS}$ Pulse Width	100		120		145		180		ns	
28	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	105		130		155		190		ns	
29	t_{CRW}	Read-Write Cycle $\overline{CAS}$ Pulse Width	75		90		105		130		ns	

AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2600-80		2600-10		2600-12		2600-15		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
29	t_{CRW}	Read-Modify-Write Cycle $\overline{CAS}$ Pulse Width	75		100		115		140		ns	
30	t_{RWD}	$\overline{RAS}$ to Write Delay	75		90		110		140		ns	m
31	t_{CWD}	$\overline{CAS}$ to Write Delay	50		60		70		75		ns	m
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		30		35		ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		30		35		ns	
34	t_{NC}	Nibble Mode Read Cycle Time	48		55		65		75		ns	
35	t_{NCAC}	Nibble Mode Access Time from $\overline{CAS}$		20		25		30		35	ns	
36	t_{NCAS}	Nibble Mode $\overline{CAS}$ Pulse Width	20		25		30		35		ns	
37	t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	18		20		25		30		ns	
38	t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	23		25		30		35		ns	
39	t_{NRMW}	Nibble Mode Read-Modify-Write Cycle Time	64		80		95		110		ns	
40	t_{NCRW}	Nibble Mode R-M-W $\overline{CAS}$ Pulse Width	36		45		60		70		ns	
41	t_{NCWD}	Nibble Mode $\overline{CAS}$ to Write Delay	18		20		25		30		ns	
42	t_{FCS}	Refresh Set-up for $\overline{CAS}$ (Ref. $\overline{RAS}$)	0		0		0		0		ns	
43	t_{FCH}	Refresh Hold Time (Ref. $\overline{RAS}$)	12		15		17		20		ns	
	t_{REF}	Refresh Period		4		4		4		4	ms	
	t_T	Input Rise and Fall Times	3	50	3	50	3	50	3	50	ns	n

NOTES:

e: t_{RCD} (max) is a derived parameter; t_{RCD} (max) = t_{RAC} (max) − t_{CAC} (max); t_{RCD} (min) is a restrictive parameter due to $\overline{CAS}$-before-$\overline{RAS}$ refresh.

f: t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition.

h: Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).

i: Assumes that $t_{RCD} \geq t_{RCD}$ (max).

j: Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is determined exclusively by t_{CAC}.

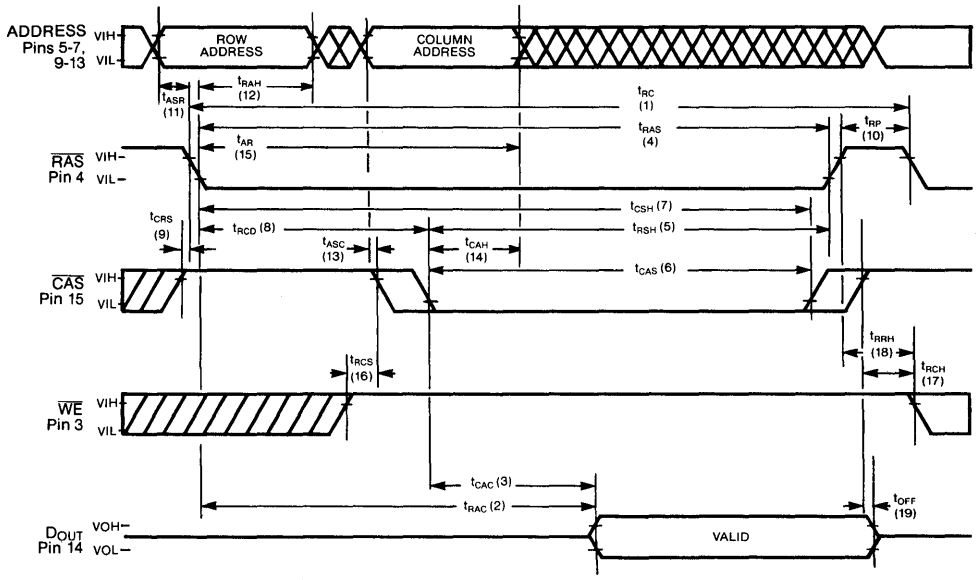
k: Either t_{RRH} or t_{RCH} must be satisfied for a Read cycle.

l: These parameters are referenced to $\overline{CAS}$ leading edge in Early-Write cycles, and to $\overline{WE}$ leading edge in Read-Write or Read-Modify-Write cycles.

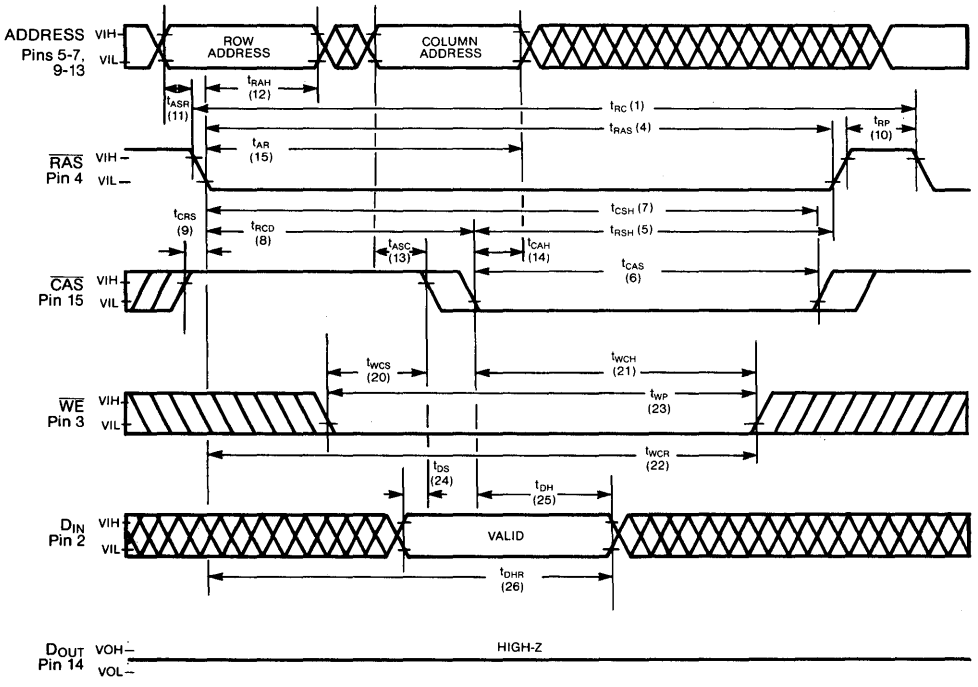
m: t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an Early-Write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a Read-Write and the data output will contain data read from the selected cell. If neither of the above conditions is met the condition of the data out is indeterminate at access time and remains so until $\overline{CAS}$ returns to V_{IH}.

n: The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Transition time measured between V_{IL} (max) and V_{IH} (min).

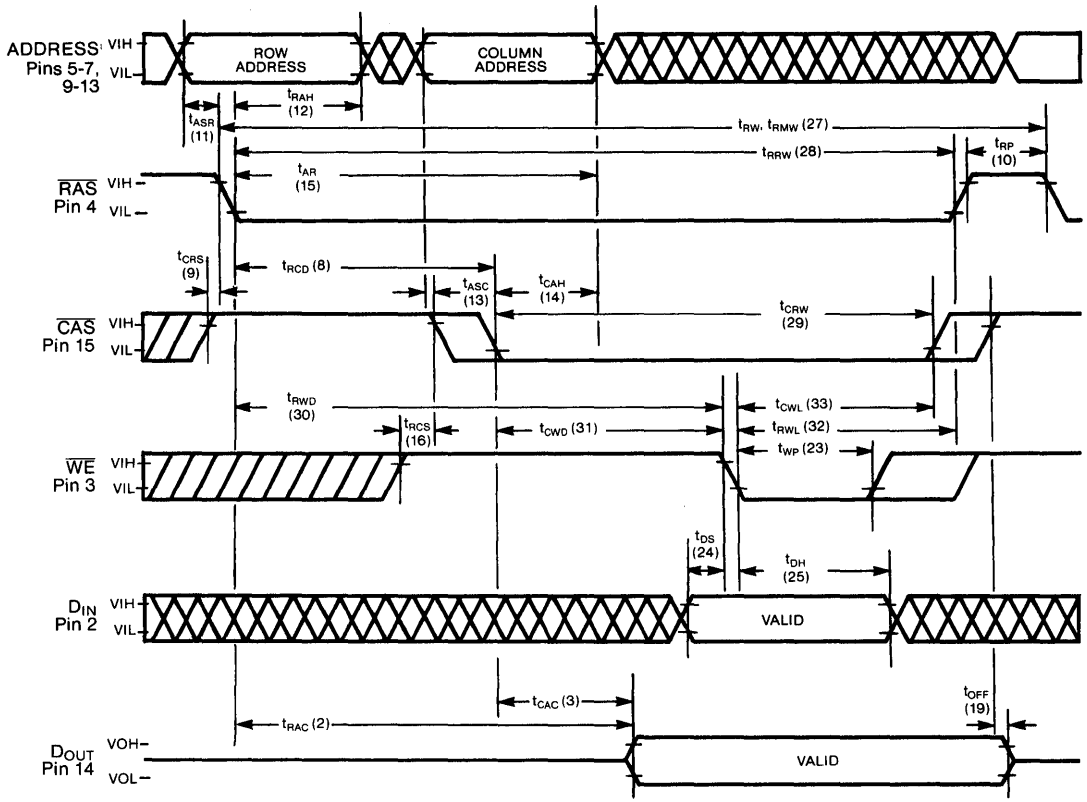
READ CYCLE



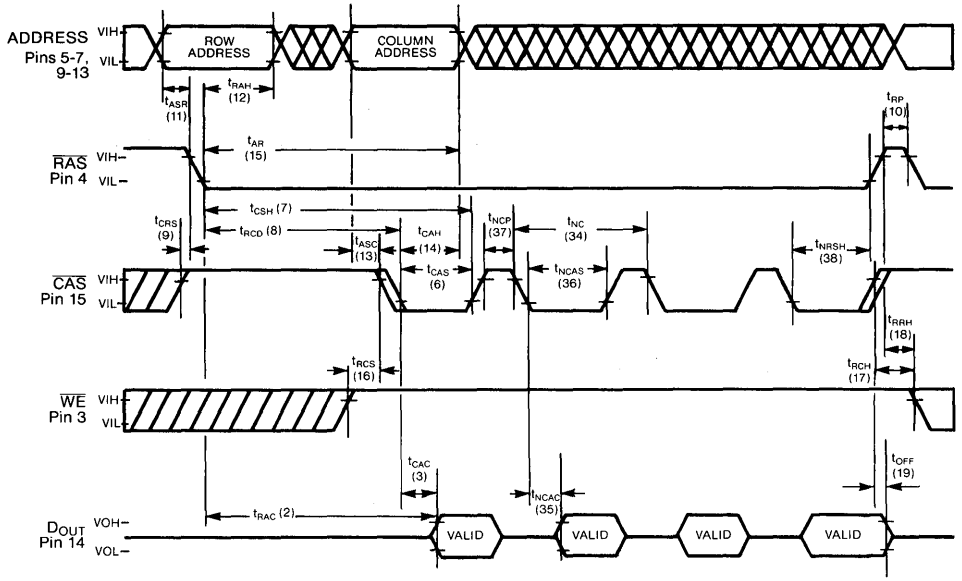
WRITE CYCLE



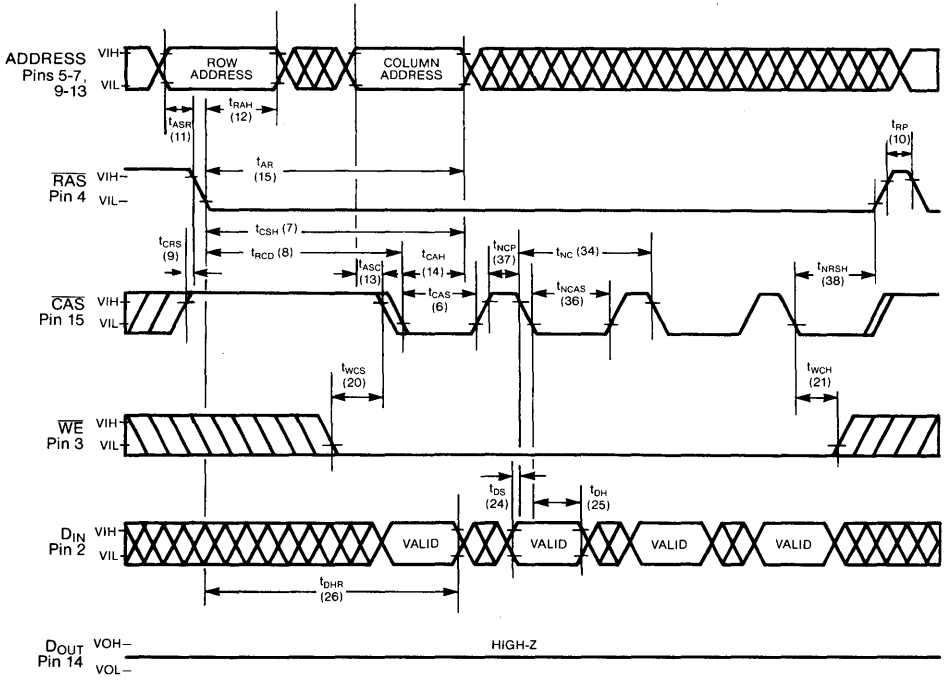
READ-WRITE/READ-MODIFY-WRITE CYCLE



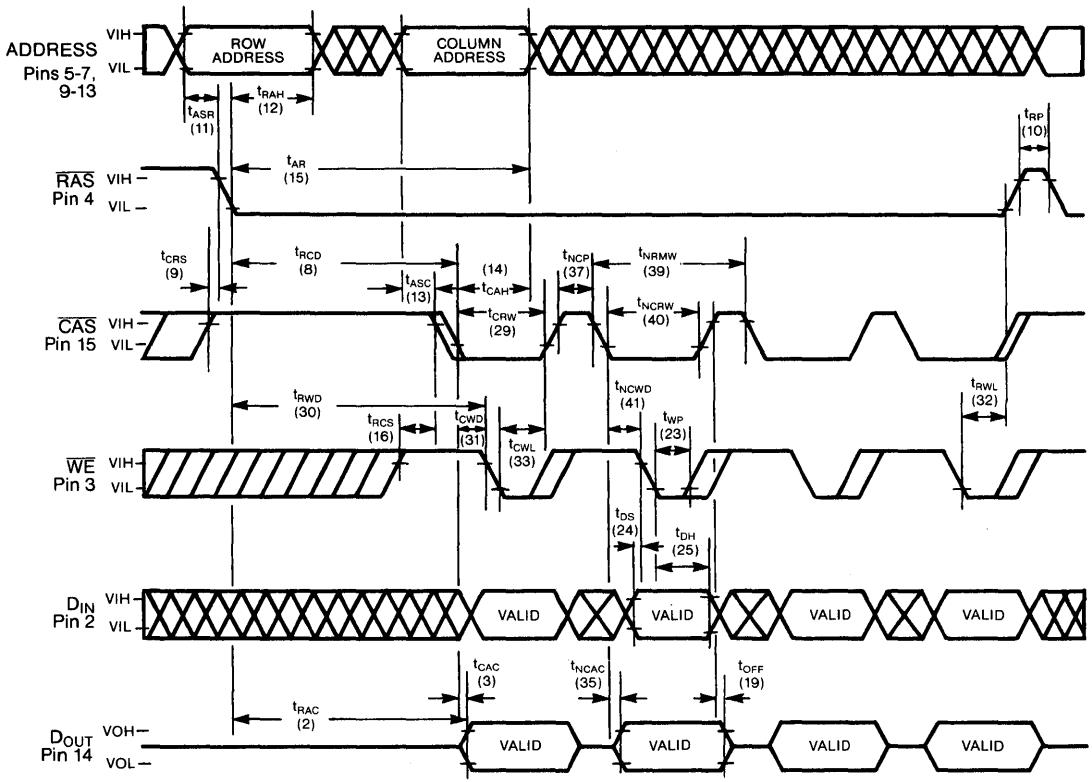
NIBBLE MODE READ CYCLE



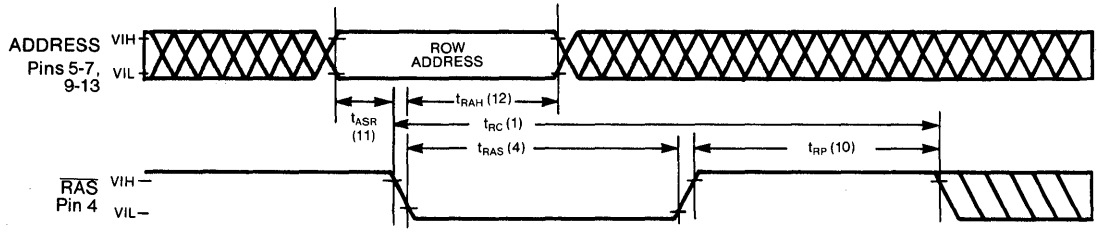
NIBBLE MODE WRITE CYCLE



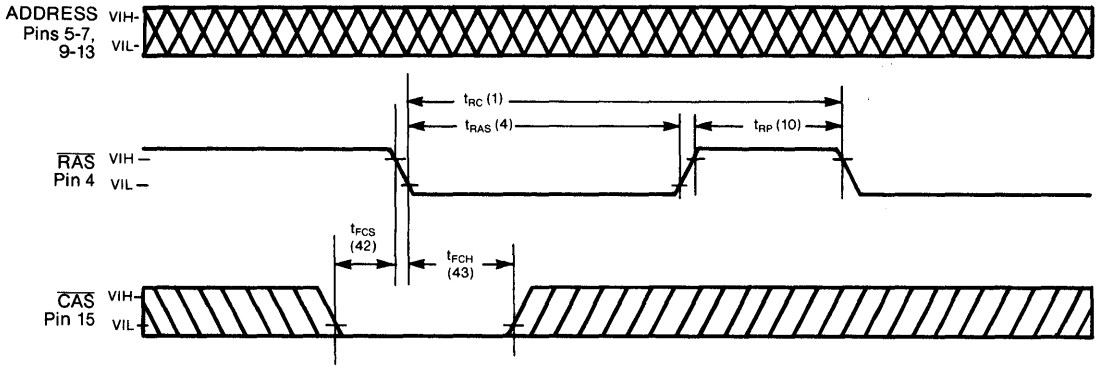
NIBBLE MODE READ-MODIFY-WRITE CYCLE



$\overline{\text{RAS}}$-ONLY REFRESH [$\overline{\text{CAS}} \geq V_{IH}$ (min)]



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH



APPLICATION

To ensure proper operation of the IMS2600 in a system environment it is recommended that the following guidelines and board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (8) through the decoupling capacitor, to the ground pin (16) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line and the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. To prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry. A high-frequency decoupling capacitor with a value of 0.1μF, should be placed between the rows of memory devices in the array. A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propogating down the lines, especially low-going TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver/termination combination close to the memory array. Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are among the most important, yet basic guidelines to be followed. These guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

AVERAGE CURRENT CALCULATIONS

In a system, the average current used by the IMS2600 can be calculated using:

$$I_{CC(avg)} = \frac{[t_{RAS(min)} + t_{RP(min)}]\, I_{CC_1} + [t_{RAS(s)} - t_{RAS(min)}]\, I_{CC_2} + [t_{RP(s)} - t_{RP(min)}]\, I_{CC_3}}{[t_{RAS(s)} + t_{RP(s)}]}$$

where $t_{RAS(s)}$ = System $\overline{RAS}$ pulse width

$t_{RP(s)}$ = System $\overline{RAS}$ precharge pulse width

$t_{RAS(min)}$ = $\overline{RAS}$ minimum pulse width from data sheet

$t_{RP(min)}$ = $\overline{RAS}$ precharge minimum pulse width from data sheet

I_{CC1} = the operating current from data sheet

I_{CC2} = the active current from data sheet

I_{CC3} = the standby current from data sheet

An I_{CC} average value can be found for any cycle rate and duty cycle using the above formula. For example, at the maximum cycle rate of the IMS2600-12:

$t_{RAS(s)} = t_{RAS(min)} = 120ns$

$t_{RP(s)} = t_{RP(min)} = 60ns$

then by substitution into the above formula,

$$I_{CC(avg)} = \frac{(120ns + 60ns)\, I_{CC_1} + (120ns - 120\ ns)\, I_{CC_2} + (60ns - 60ns)\, I_{CC_3}}{(120ns + 60ns)}$$

$$= \frac{(180ns)\, I_{CC_1} + (0ns)\, I_{CC_2} + (0ns)\, I_{CC_3}}{180ns}$$

$$= I_{CC_1} = 75mA$$

The $I_{CC(avg)}$ is equal to the maximum operating current as given in the data sheet (with outputs not loaded).

As another example, the minimum $I_{CC(avg)}$ occurs during refresh-only operation at the minimum required refresh cycle rate and minimum $\overline{RAS}$ pulse width. For the IMS2600-12, this would give:

$t_{RAS(s)} = t_{RAS(min)} = 120ns$

$$t_{RP(s)} = \frac{4ms}{256} - t_{RAS(min)} = 15\,505ns$$

then by substitution into the above formula,

$$I_{CC(avg)} = \frac{[120ns + 60ns]\, I_{CC_1} + [120ns - 120ns]\, I_{CC_2} + [15\,505ns - 60ns]\, I_{CC_3}}{[120ns + 15\,505ns]}$$

$$I_{CC(avg)} = \frac{180ns\ (75mA) + 15\,445ns\ (4.0mA)}{15\,625ns} = 4.82mA$$

This current represents the minimum current that one IMS2600-12 would use in a system. When the IMS2600 is operated within the data sheet specifications and timing limits, all other $I_{CC(avg)}$ calculations will fall between Example 1 and Example 2 values.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS2600	80ns	PLASTIC DIP	IMS2600P-80
	100ns	PLASTIC DIP	IMS2600P-10
	100ns	CERAMIC DIP	IMS2600S-10
	100ns	CHIP CARRIER	IMS2600W-10
	120ns	PLASTIC DIP	IMS2600P-12
	120ns	CERAMIC DIP	IMS2600S-12
	120ns	CHIP CARRIER	IMS2600W-12
	150ns	PLASTIC DIP	IMS2600P-15

IMS2620

High Performance 16Kx4 Dynamic RAM

No Page Mode Operation

FEATURES

- 16K x 4 Organization
- High Speed, $\overline{RAS}$ Access of 100, 120 and 150ns
- Cycle Times of 160, 190, and 240ns
- Low Power:
  28mW Standby
  495mW Active (160ns Cycle Time)
  330mW Active (350ns Cycle Time)
- Common I/O
- Single +5V ± 10% Power Supply
- On-Chip Refresh Assist using $\overline{CAS}$-before-$\overline{RAS}$
- Multiplexed Addresses 8 Row, 6 Column
- 18-Pin Package—JEDEC Standard Pinout
- All Inputs and Outputs TTL Compatible
- Output Enable ($\overline{OE}$) Control for Greater Timing Flexibility
- 4ms/256 Cycle Refresh
- Read, Write and Read-Modify-Write Capability
- 25 MBit Data Rate

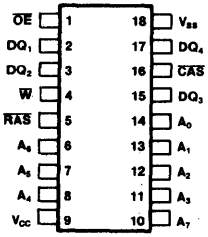
DESCRIPTION

The IMS2620 16K x 4 bit dynamic RAM is fabricated with INMOS' advanced Double Poly N-MOS technology and utilizes advanced circuit techniques to achieve high performance, low power and wide operating margins. Multiplexed addressing and common data I/O allow the IMS2620 to be packaged in an 18-pin, 300-mil wide plastic DIP with JEDEC standard Pinout.

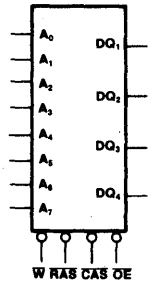
The IMS2620 has several features that help simplify system interfacing. $\overline{CAS}$-before-$\overline{RAS}$ refresh assist eliminates the need for a refresh counter and an extra level of address multiplexing. The Output Enable ($\overline{OE}$) function gives an extra level of output control that allows common I/O in both early-write and read-modify-write cycles.

For applications requiring very high speeds, the IMS2620 offers the equivalent data rate of 25 MBits, without Page Mode.

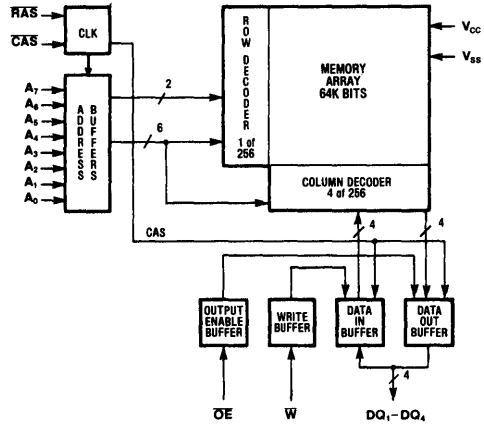
PIN CONFIGURATION *



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_7	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
DQ_1 - DQ_4	DATA IN/DATA OUT
$\overline{OE}$	OUTPUT ENABLE
$\overline{W}$	WRITE ENABLE
V_{CC}	+5V SUPPLY
V_{SS}	GROUND

*Row Addresses A0-A7
Column Addresses A1-A6

DEVICE OPERATION

The IMS2620 contains 65,536 bits of information. Fourteen address bits are required to decode 4 of 65,536 storage locations. The fourteen addresses for unique nibble (4 bits) selection are time division multiplexed under control of the Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$) clocks. The normal sequence of $\overline{RAS}$ and $\overline{CAS}$ requires that $\overline{CAS}$ is high as $\overline{RAS}$ goes low. This causes the eight address inputs (A0-A7) to be latched and decoded for selection of one of the 256 rows. The row addresses must be held for the specified period [t_{RAH} (min)] and then they may be switched to the appropriate column addresses. After the six column addresses (A1-A6) are stable for the specified setup time, $\overline{CAS}$ may be brought low. This causes the six column addresses to be latched and used to select 4 of the 256 bits within the specified row. The cycle is terminated by bringing $\overline{RAS}$ high. A new cycle may be initiated after $\overline{RAS}$ has been high for the specified precharge interval [t_{RP} (min)]. $\overline{RAS}$ and $\overline{CAS}$ must be properly overlapped and once brought low they must remain low for their specified pulse widths.

READ CYCLE

A read cycle is performed by sequencing $\overline{RAS}$ and $\overline{CAS}$ as described above while holding the $\overline{WE}$ input high and $\overline{OE}$ low when $\overline{RAS}$ and $\overline{CAS}$ are both low. During a read cycle, the read access time is determined by the actual timing relationship between $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$. If $\overline{CAS}$ goes low within the specified $\overline{RAS}$ to $\overline{CAS}$ delay [t_{RCD} (max)] and $\overline{OE}$ goes low within the output enable access time [t_{OEA} (max)], then the access time is determined by $\overline{RAS}$ and is equal to t_{RAC} (max). If $\overline{CAS}$ occurs later than t_{RCD} (max) and output enable access time [t_{OEA} (max)] is satisfied, then access time is determined by $\overline{CAS}$ and is equal to t_{CAC} (max). If t_{OEA} (max) is not satisfied within either the t_{RAC} (max) or t_{CAC} (max), then the access time is determined by $\overline{OE}$ and is equal to t_{OEA} (max).

WRITE CYCLE

The IMS2620 will perform three types of write cycles: Early-Write, Late-Write, and Read-Modify-Write. The difference between these cycles is that with an Early-Write cycle the data out remains open regardless of the state of $\overline{OE}$ and with a Late-Write cycle or Read-Modify-Write cycle the data out is controlled by $\overline{OE}$.

DEVICE SELECTION AND OUTPUT CONTROL

A device is not selected if $\overline{RAS}$ is sequenced while $\overline{CAS}$ remains high or if $\overline{CAS}$ is sequenced while $\overline{RAS}$ remains high. The device must receive a properly overlapped $\overline{RAS}$/$\overline{CAS}$ sequence to be selected and to perform read or write operations.

Once the device is selected the state of the data out buffers is controlled by $\overline{CAS}$ and $\overline{OE}$. If $\overline{CAS}$ and $\overline{OE}$ both remain low after $\overline{RAS}$ goes high, the data out will remain in the state it was when $\overline{RAS}$ went high. The output will remain unchanged even if a $\overline{RAS}$ sequence occurs while $\overline{CAS}$ and $\overline{OE}$ are held low. Either $\overline{CAS}$ or $\overline{OE}$ going high disables the output buffer. Whenever the data output buffers are turned off by $\overline{OE}$ making a low-to-high transition, re-asserting $\overline{OE}$ will not turn the output buffers back on unless another $\overline{RAS}$/$\overline{CAS}$ read sequence is executed.

REFRESH

The IMS2620 remembers data by storing charge on a capacitor. Because the charge will leak away over a period of time it is necessary to access the data in the cell (capacitor) periodically in order to fully restore the stored charge while it is still at a sufficiently high level to be properly detected. For the IMS2620 any $\overline{RAS}$ sequence will fully refresh an entire row of 256 bits (64 nibbles). To ensure that all cells remain sufficiently refreshed, all 256 rows must be refreshed every 4ms. The addressing of the rows for refresh may be sourced either externally or internally.

If the row refresh addresses are sourced externally, $\overline{CAS}$ must be high when $\overline{RAS}$ goes low. If $\overline{CAS}$ is high when $\overline{RAS}$ goes low, any type of cycle (Read, Write, Read-modify-write, $\overline{RAS}$/$\overline{CAS}$ only, or $\overline{RAS}$ only) will cause the addressed row to be refreshed.

If $\overline{CAS}$ is low when $\overline{RAS}$ falls, the IMS2620 will use an internal 8-bit counter as the source of the row addresses and will ignore the external addresses. This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh-only mode and no data is accessed from this location. $\overline{CAS}$-before-$\overline{RAS}$ refresh does not cause device selection and the state of the data out buffers remains unchanged. If the output buffers were in a high impedance state at the start of the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle, they will remain in the high impedance state regardless of the state of the $\overline{OE}$ control. If $\overline{OE}$ and $\overline{CAS}$ are still low from a preceding read cycle, the output data buffers will remain valid through the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle as long as both $\overline{OE}$ and $\overline{CAS}$ remain active. When data out is held valid through a refresh cycle in this fashion it is referred to as a Hidden Refresh cycle.

ABSOLUTE MAXIMUM RATINGS*[a]

Voltage on V_{CC} Relative to V_{SS} . . . . . −1.0V to +7.0V
Storage Temp. (Plastic Package). . . . −55°C to +125°C
Power Dissipation 1W
Short Circuit Output Current/Output 50mA
(One output at a time)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS[a, b]

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage		0		V	
V_{IH}	Logic "1" Voltage	2.4		V_{CC} + 1	V	
V_{IL}	Logic "0" Voltage	−2.0		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	Still Air

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current (Operating)	IMS2620-10		90	mA	t_{RC} = 160ns, t_{RAS} = 100ns (c)
		IMS2620-10		60		t_{RC} = 350ns, t_{RAS} = 100ns
		IMS2620-12		80		t_{RC} = 190ns, t_{RAS} = 120ns
		IMS2620-12		60		t_{RC} = 350ns, t_{RAS} = 120ns
		IMS2620-15		70		t_{RC} = 240ns, t_{RAS} = 150ns
		IMS2620-15		60		t_{RC} = 350ns, t_{RAS} = 150ns
I_{CC_2}	V_{CC} Power Supply Current (Active)			20	mA	$RAS \leq V_{IL}$(max), $CAS \leq V_{IL}$(max)
I_{CC_3}	Standby Current			5.0	mA	$RAS \geq V_{IH}$(min), $CAS \geq V_{IH}$(min)
I_{IN}	Input Leakage Current (Any Input)		−10	10	μA	$0V \leq V_{IN} \leq 5.5V$, others = 0V
I_{OLK}	Output Leakage Current		−10	10	μA	D_{OUT} = Hi Z, $0V \leq V_{OUT} \leq 5.5V$
V_{OH}	Output High Voltage		2.4		V	I_O = −2.0mA
V_{OL}	Output Low Voltage			0.4	V	I_O = 4.2mA

Note a: All voltage values in this data sheet are with respect to V_{SS}.
b: After power-up, a pause of 500 μs followed by eight initialization memory cycles is required to achieve proper device operation. Any interval greater than 4ms with $\overline{RAS}$ inactivity requires eight reinitialization cycles to achieve proper device operation and data must be reloaded.
c: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with output open.

AC TEST CONDITIONS

Input Pulse Levels. . . . . 0 to 3V
Input Rise and Fall Times. . . . . 5ns between 0.8 and 2.4V
Input Timing Reference Levels. . . . . 0.8 and 2.4V
Output Timing Reference Levels. . . . . 0.8 and 2.4V
Output Load. . . . . Equivalent to 2 TTL Loads and 50pF

CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS	COND.
C_{IN}	Input Cap. $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	6	pF	d
C_{IN}	Input Cap. Addresses	5	pF	d
C_{OUT}	Output Cap.	7	pF	d o

Note d: Capacitance measured with BOONTON METER.
o: Disabled by output buffers, $\overline{CAS} = V_{IH}$ or $\overline{OE} = V_{IH}$.

AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL STD	SYMBOL JEDEC	PARAMETER	-10 MIN	-10 MAX	-12 MIN	-12 MAX	-15 MIN	-15 MAX	UNITS	NOTES
1	t_{RAH}	t_{RLAX}	Row Address Hold Time	10		12		15		ns	
2	t_{ASR}	t_{AVRL}	Row Address Set-Up Time	0		0		0		ns	
3	t_{RC}	t_{RLRL}	Read Cycle Time	160		190		240		ns	
4	t_{RAS}	t_{RLRH}	$\overline{RAS}$ Pulse Width	100	10K	120	10K	150	10K	ns	h
5	t_{RP}	t_{RHRL}	$\overline{RAS}$ Precharge Time	50		60		80		ns	
6	t_{AR}	$t_{RLA(C)X}$	Column Address Hold Time (Ref. $\overline{RAS}$)	65		80		110		ns	
7	t_{CSH}	t_{RLCH}	$\overline{CAS}$ Hold Time	100		120		150		ns	
8	t_{RSH}	t_{CLRH}	$\overline{RAS}$ Hold Time	65		70		80		ns	
9	t_{CRS}	t_{CHRL}	$\overline{CAS}$ to $\overline{RAS}$ Set-Up Time	0		0		0		ns	
10	t_{RCD}	t_{RLCL}	$\overline{RAS}$ to $\overline{CAS}$ Delay	15	40	17	50	20	70	ns	e j
11	t_{ASC}	t_{AVCL}	Column Address Set-Up Time	0		−5		−5		ns	
12	t_{CAH}	t_{CLAX}	Column Address Hold Time	25		30		40		ns	
13	t_{CAS}	t_{CLCH}	$\overline{CAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	t_{RCS}	t_{WHCL}	Read Command Set-Up Time	0		0		0		ns	
15	t_{RRH}	t_{RHWL}	Read Command Hold Time (Ref. $\overline{RAS}$)	0		0		0		ns	k
16	t_{RCH}	t_{CHWL}	Read Command Hold Time (Ref. $\overline{CAS}$)	0		0		0		ns	k
17	t_{CAC}	t_{CLQV}	Access Time From $\overline{CAS}$		60		70		80	ns	i
18	t_{RAC}	t_{RLQV}	Access Time from $\overline{RAS}$		100		120		150	ns	h
19	t_{OFF}	t_{CHQZ}	Output Buffer Turn-Off Delay From $\overline{CAS}$	0	20	0	25	0	30	ns	f
20	t_{OEA}	t_{GLQV}	Access Time From $\overline{OE}$		25		30		40	ns	
21	t_{OEZ}	t_{GHQZ}	Output Buffer Turn-Off Delay From $\overline{OE}$	0	20	0	25	0	30	ns	
22	t_{WCS}	t_{WLCL}	Write Command Set-Up Time (Early Write)	−5		−5		−5		ns	m
23	t_{WCH}	t_{CLWH}	Write Command Hold Time (Ref. $\overline{CAS}$)	20		30		40		ns	
24	t_{WP}	t_{WLWH}	$\overline{WE}$ Pulse Width	25		30		40		ns	

NOTES:

e: t_{RCD} (max) is a derived parameter; t_{RCD} (max) = t_{RAC} (max) − t_{CAC} (max); t_{RCD} (min) is a restrictive parameter due to $\overline{CAS}$-before-$\overline{RAS}$ refresh.

f: t_{OFF} (max) and t_{OEZ} (max) are defined as the time at which the output achieves the open circuit condition.

h: Assumes that $t_{RCD} \leq t_{RCD}$ (max).If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).

i: Assumes that $t_{RCD} \geq t_{RCD}$ (max).

j: Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is determined exclusively by t_{CAC}.

k: Either t_{RRH} or t_{RCH} must be satisfied for a Ready cycle.

l: These parameters are referenced to $\overline{CAS}$ leading edge in Early-Write cycles, and to $\overline{WE}$ leading edge in Read-Write or Read-Modify-Write cycles.

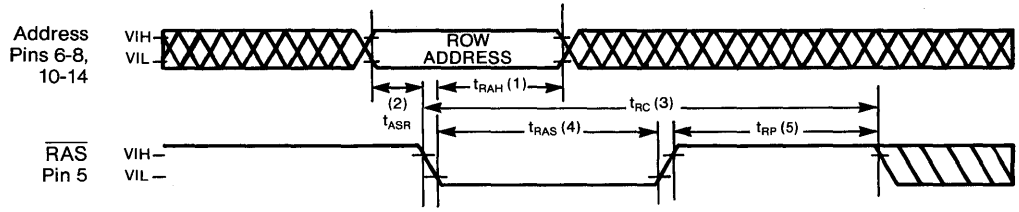
m: t_{WCS} is a restrictive operating parameter in Read-Write and Read-Modify-Write cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an Early-Write cycle and the data output will remain open circuit throughout the entire cycle regardless of the state of $\overline{OE}$.

n: The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Transition time measured between V_{IL} (max) and V_{IH} (min).

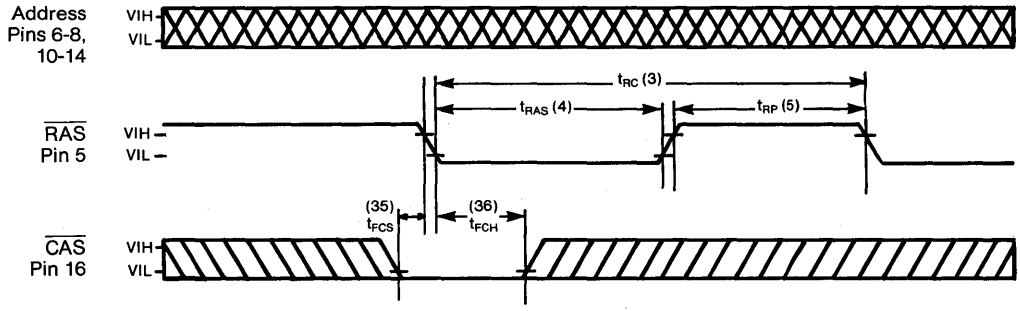
AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL STD	SYMBOL JEDEC	PARAMETER	-10 MIN	-10 MAX	-12 MIN	-12 MAX	-15 MIN	-15 MAX	UNITS	NOTES
25	t_{WCR}	t_{RLWH}	Write Command Hold Time (Ref. $\overline{RAS}$)	55		80		110		ns	
26	t_{DS}	t_{DVCL} t_{DVWL}	Data-In Set-Up Time	0		0		0		ns	l
27	t_{DH}	t_{CLDX} t_{WLDX}	Data-In Hold Time	25		30		40		ns	l
28	t_{DHR}	t_{RLDX}	Data-In Hold Time (Ref. $\overline{RAS}$)	65		80		110		ns	
29	t_{CWL}	t_{WLCH}	Write Command To $\overline{CAS}$ Lead Time	25		30		40		ns	
30	t_{OCS}	t_{GHCL}	$\overline{OE}$ Set-Up To $\overline{CAS}$ For Output Hi-Z	−5		−5		−5		ns	
31	t_{OED}	t_{GHDX}	$\overline{OE}$ High To Data-In	20		25		30		ns	
32	t_{RWL}	t_{WLRH}	Write Command To $\overline{RAS}$ Lead	35		45		60		ns	
33	t_{OCH}	t_{CHGX}	$\overline{OE}$ High Hold Time After $\overline{CAS}$ High	5		5		5		ns	
34	t_{ORH}	t_{RHGX}	$\overline{OE}$ Hold Time After $\overline{RAS}$	0		0		0		ns	
35	t_{FCS}	t_{CLRL}	Refresh Set-Up Time For $\overline{CAS}$ (Ref. $\overline{RAS}$)	0		0		0		ns	
36	t_{FCH}	t_{RLCH}	Refresh Hold Time (Ref. $\overline{RAS}$)	15		20		25		ns	
	t_{REF}	t_{REF}	Refresh Period		4		4		4	ms	b
	t_T	t_T	Input Rise And Fall Times	3	50	3	50	3	50	ns	n

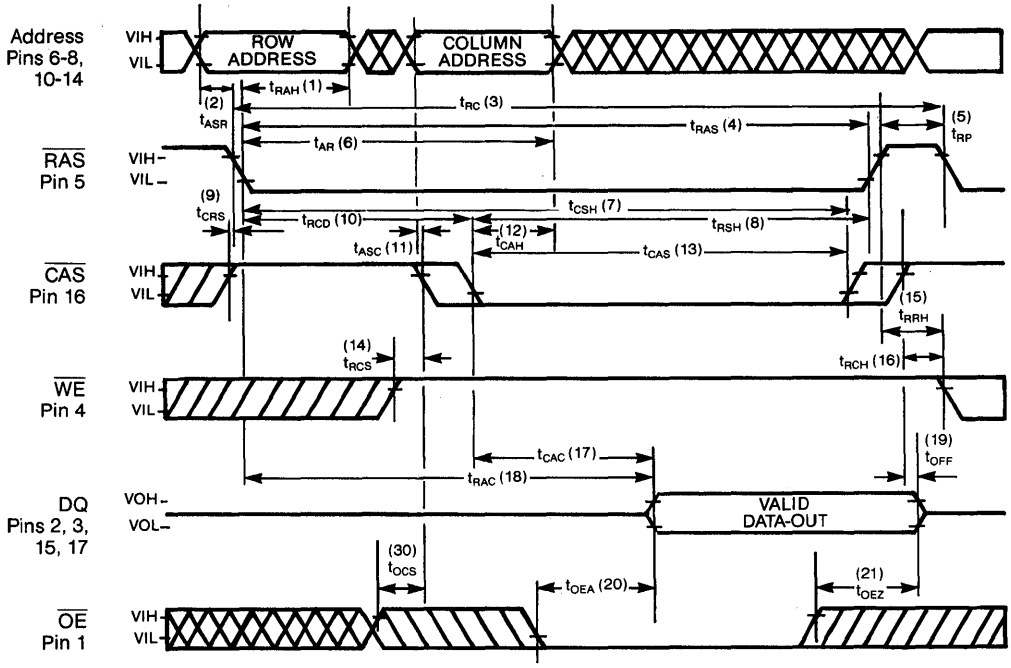
$\overline{RAS}$-ONLY REFRESH [$\overline{CAS} \geq V_{IH}$ (min)]



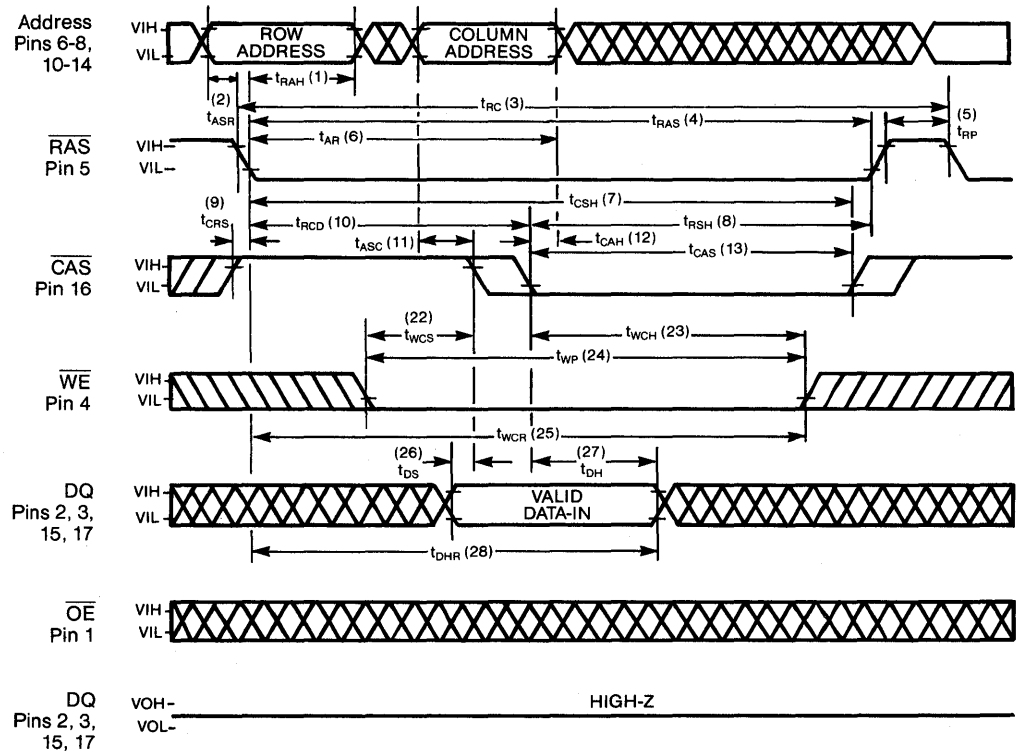
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH



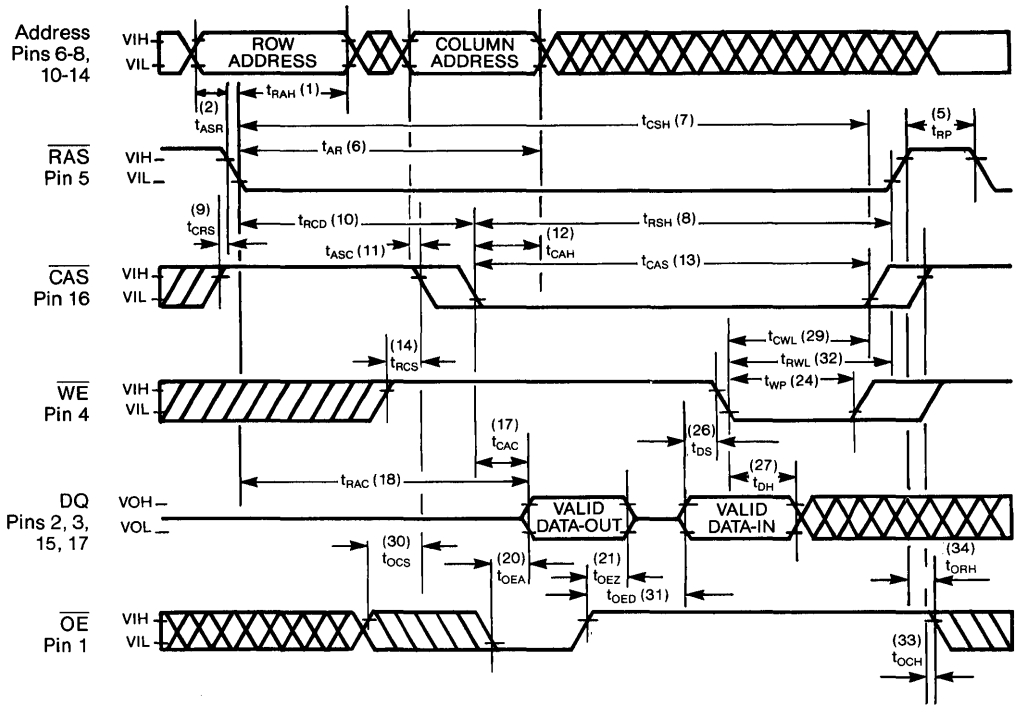
READ CYCLE



EARLY WRITE CYCLE



READ-WRITE/READ-MODIFY-WRITE CYCLE



APPLICATION

To ensure proper operation of the IMS2620 in a system environment it is recommended that the following guidelines for board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (9) through the decoupling capacitor, to the ground pin (18) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line and the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. To prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry. A high-frequency decoupling capacitor with a value of 0.1μF should be placed between the rows of memory devices in the array. A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propogating down the lines, especially low-going TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver/termination combination close to the memory array. Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are among the most important, yet basic guidelines to be followed. These guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS2620	100ns	PLASTIC DIP	IMS2620P-10
	120ns	PLASTIC DIP	IMS2620P-12
	150ns	PLASTIC DIP	IMS2620P-15

IMS2630

High Performance 8Kx8 Dynamic RAM

FEATURES

- 8Kx8 Byte-Wide Organization
- High Speed Chip Enable Access of 120, 150 and 200ns
- 28-Pin Package—JEDEC Standard Pinout
- 256 Cycle/4ms Refresh
- On-Chip Refresh Counter
- Hidden Refresh Using Pin 1 Refresh
- Single +5V ± 10% Supply
- Latched Chip Select and Address
- High Speed Output Enable Control
- Low Power
  - 42mW Standby
  - 358mW Max @ 190ns cycle
  - 275mW Max @ 240ns cycle
  - 220mW Max @ 310ns cycle

DESCRIPTION

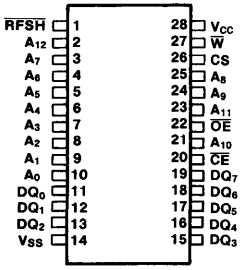
The IMS2630 8Kx8 bit dynamic RAM is fabricated with INMOS' advanced double-poly N-MOS technology and utilizes advanced circuit techniques to achieve high performance while providing low power and wide operating margins. The IMS2630 is packaged in a 28-pin, 600-mil wide DIP and features the JEDEC standard pinout.

On-chip refresh circuitry simplifies system interfacing and eliminates the need for an external refresh counter. Pulsing Pin 1 ($\overline{RFSH}$) activates an on-chip refresh cycle.

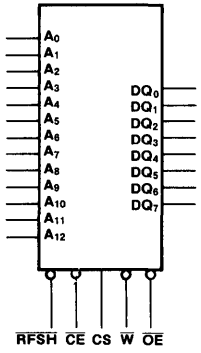
The IMS2630 is fully TTL compatible and operates from a single +5V ± 10% power supply.

The IMS2630 is a cost-effective VLSI dynamic RAM intended for high-performance byte-wide applications as well as applications requiring high data rates exceeding 42 MBits/sec.

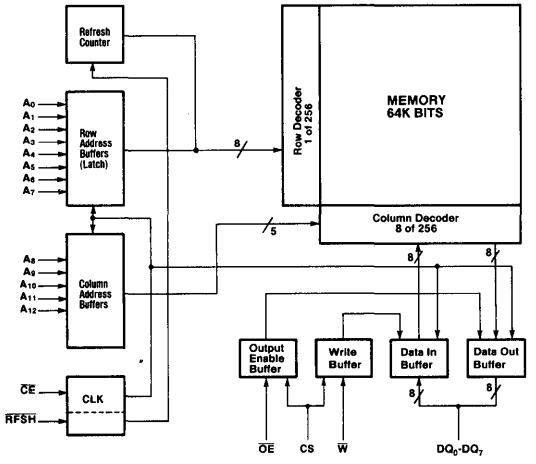
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESS INPUTS		
$\overline{CE}$	CHIP ENABLE	DQ_0-DQ_7	DATA IN/DATA OUT
CS	CHIP SELECT	V_{CC}	+5V SUPPLY
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{OE}$	OUTPUT ENABLE	$\overline{RFSH}$	REFRESH ENABLE

READ CYCLE

A read cycle is performed by sequencing $\overline{CE}$, CS, and $\overline{OE}$ while holding $\overline{W}$ input high (inactive). The addresses (A0-A12) and CS are latched by the falling edge of $\overline{CE}$. When the data output becomes valid, an automatic precharge cycle is executed. Even though the device executes an automatic precharge, the data output remains valid until either $\overline{CE}$ or $\overline{OE}$ goes high (inactive).

The read access time is determined by either $\overline{CE}$ or $\overline{OE}$. Data output will be valid at Chip Enable Access time (t_{CEA}) provided that $\overline{OE}$ has been valid at least (t_{OEA}) (Output Enable Access time) prior to the maximum Chip Enable Access time. If $\overline{OE}$ has not been asserted early enough to guarantee the Chip Enable Access (t_{CEA}), data output will not appear until t_{OEA} (Output Enable Access time) after $\overline{OE}$ goes low.

WRITE CYCLE

A write cycle is performed by sequencing $\overline{CE}$, CS and $\overline{W}$ while holding $\overline{OE}$ input high (inactive). Identical to the read cycle, the address (A0-A12) and CS are latched by the falling edge of $\overline{CE}$. After data is written into the memory location within the device, an automatic precharge cycle is executed by the RAM.

The IMS2630 will perform two types of write cycles: Early-Write or Late-Write. The type of write cycle performed is determined by the relationship between $\overline{CE}$ and $\overline{W}$. If $\overline{W}$ is brought low prior to $\overline{CE}$, an Early-Write cycle is executed and the data-in (DQ0-DQ7) is strobed into the RAM by the falling edge of $\overline{CE}$. If $\overline{W}$ is brought low after $\overline{CE}$, a Late-Write cycle is executed and the data-in (DQ0-DQ7) is strobed into the RAM by the falling edge of $\overline{W}$.

REFRESH

The IMS2630 dynamic RAM remembers data by charge storage in capacitive cells. Because the charge leaks away over a period of time it is necessary to access the data in each cell (capacitor) periodically in order to fully restore the stored charge while it is still at a sufficiently high level to be properly detected. In order to restore all memory locations, all 256 row locations (every binary combination of A0-A7) must be accessed each 4 ms interval. Refresh cycles may be performed in either distributed or burst mode as long as the 4ms requirement is met.

The refresh addresses, A0-A7, may be supplied either externally or internally. If the row addresses are provided externally, any $\overline{CE}$ type memory cycle will refresh the row location defined by the address field during the high-to-low transition of $\overline{CE}$. Read, Write, or $\overline{CE}$-Only type cycles are sufficient for the purpose of refreshing.

System interfacing requirements can be simplified and system refresh support logic can be reduced by using $\overline{RFSH}$-type (Pin 1) refreshing. During $\overline{RFSH}$ cycles, an on-chip address counter provides the necessary refresh address. This eliminates the need for providing refresh addresses externally. After each $\overline{RFSH}$ initiated cycle has been executed, the on-chip refresh address counter is incremented in preparation for the next $\overline{RFSH}$ initiated cycle. The on-chip refresh circuitry can be activated by strobing $\overline{RFSH}$ low when $\overline{CE}$ is high (inactive). Also, hidden refresh cycles can be executed when $\overline{CE}$ is low provided that $\overline{RFSH}$ is not asserted until after sufficient time has elapsed for the completion of automatic precharging as specified by t_{CFD} and t_{OFD} for a hidden refresh during a read cycle or by t_{CFD} and t_{WFD} for a hidden refresh during a write cycle. Hidden $\overline{RFSH}$ cycles can't be executed during $\overline{CE}$-Only type cycles since the above automatic precharge requirements would not be met.

ABSOLUTE MAXIMUM RATINGS*[a]

Voltage on V_{CC} Relative to V_{SS} . . . . . −1.0V to +7.0V
Storage Temp. (Plastic Package) . . −55°C to +125°C
Power Dissipation. 1W
Short Circuit Output Current/Output. 30mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS[a, b]

SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage		0		V	
V_{IH}	Logic "1" Voltage	2.4		$V_{CC}+1$	V	
V_{IL}	Logic "0" Voltage	−2.0		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	Still Air

DC ELECTRICAL CHARACTERISTICS ($-0°C \leq T_A \leq 70°C$, $V_{CC} = 5V \pm 10\%$)

SYMBOL	PARAMETER		MIN	MAX	UNIT	CONDITIONS
I_{CC_1}	Average V_{CC} Power Supply Current (Operating)	IMS2630-12		65	mA	$t_C = 190ns$
		IMS2630-15		50	mA	$t_C = 240ns$ (C)
		IMS2630-20		40	mA	$t_C = 310ns$
I_{CC_2}	V_{CC} Power Supply Current (Active)			20	mA	$\overline{CE} \leq V_{IL}$ (max), $\overline{OE}$ & $\overline{W} \geq V_{IH}$ (min)
I_{CC_3}	Standby Current			7.5	mA	$\overline{CE} \geq V_{IH}$ (min)
I_{ILK}	Input Leakage Current (Any Input)		−10	10	μA	$0V \leq V_{IN} \leq 5.5V$, others = 0V
I_{OLK}	Output Leakage Current		−10	10	μA	D_{OUT} = Hi Z, $0V \leq V_{OUT} \leq 5.5V$ (d)
V_{OH}	Output High Voltage		2.4		V	$I_O = -1.0mA$
V_{OL}	Output Low Voltage			0.4	V	$I_O = 4.0mA$

AC TEST CONDITIONS

Input Pulse Levels. . . . . 0 to 3V
Input Rise and Fall Times. . . . . 5ns between 0.8 and 2.4V
Input Timing Reference Levels. . . . . 0.8 and 2.4V
Output Timing Reference Levels. . . . . 0.8 and 2.4V
Output Load. . . . . Equivalent to 2 TTL Loads and 50pF

CAPACITANCE

SYMBOL	PARAMETER	MAX	COND.
C_{IN}	Input Cap. $\overline{RFSH}$, $\overline{CE}$, $\overline{WE}$ $\overline{OE}$	8pF	e
C_{IN}	Input Cap. Addresses CS	7pF	e
C_{OUT}	Output Cap.	10pF	e f

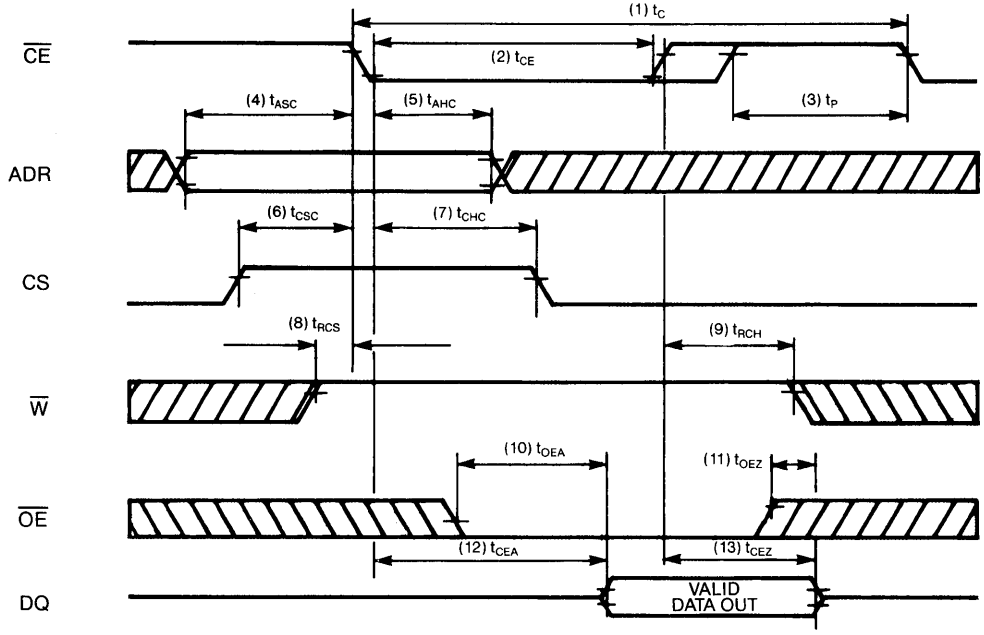
NOTES:

a: All voltage values in this data sheet are with respect to V_{SS}.
b: After power-up, a pause of 500μs followed by eight $\overline{CE}$ or $\overline{RFSH}$ initialization memory cycles is required to achieve proper device operation. Any interval greater than 4ms with $\overline{CE}$ or $\overline{RFSH}$ inactivity requires eight reinitialization cycles to achieve proper device operation and stored data must be reloaded.
c: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with output open.
d: I_{OLK} for DQ0-DQ7 measured with output open circuit $^2V_{CE} \geq V_{IH}$ (min)[3].
e: Capacitance measured with BOONTON METER.
f: $\overline{CE}$ or $\overline{OE}$ = V_{IH} to disable D_{OUT}.
g: The transition time specification applies for all control signals. In addition to meeting the transition rate specification, all control signals must transit between measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Transition time measured between V_{IL} (max) and V_{IH} (min).

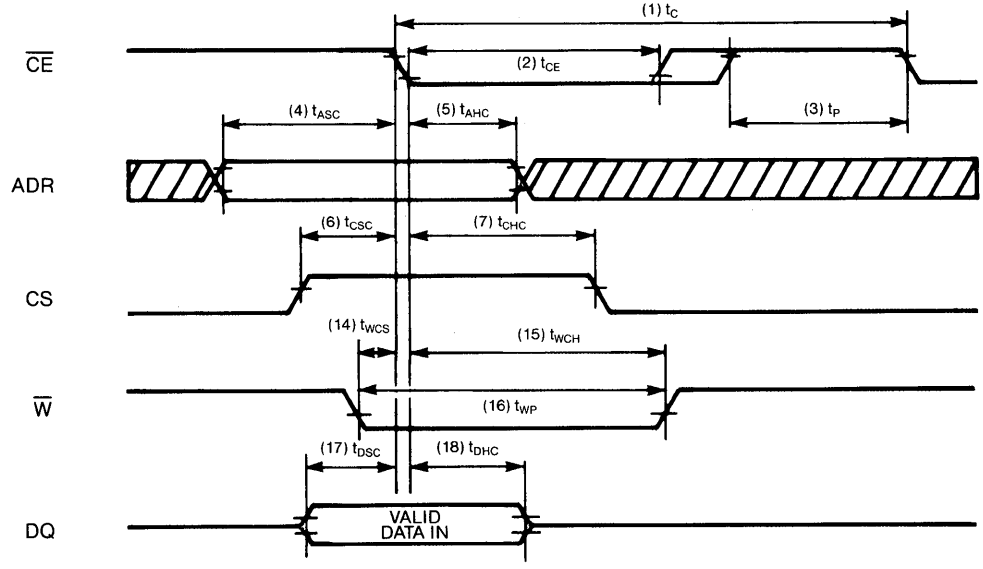
AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL		PARAMETER	2630–12		2630–15		2630–20		NOTES
	STD	JEDEC		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_C	t_{ELEL}	Random Read Or Write Cycle Time	190		240		310		
2	t_{CE}	t_{ELEH}	$\overline{CE}$ Pulse Width	120	10K	150	10K	200	10K	
3	t_P	t_{EHEL}	$\overline{CE}$ Precharge Time	60		80		100		
4	t_{ASC}	t_{AVEL}	Address Set-Up Time (Ref. $\overline{CE}$)	0		0		0		
5	t_{AHC}	t_{ELAX}	Address Hold Time (Ref. $\overline{CE}$)	30		35		40		
6	t_{CSC}	t_{SVEL}	Chip Select Set-Up Time (Ref. $\overline{CE}$)	0		0		0		
7	t_{CHC}	t_{ELSX}	Chip Select Hold Time (Ref. $\overline{CE}$)	30		35		40		
8	t_{RCS}	t_{WHEL}	Read Command Set-Up Time (Ref. $\overline{CE}$)	0		0		0		
9	t_{RCH}	t_{EHWL}	Read Command Hold Time (Ref. $\overline{CE}$)	0		0		0		
10	t_{OEA}	t_{GLQV}	Access Time From $\overline{OE}$	0	35	0	40	0	50	
11	t_{OEZ}	t_{GHQZ}	Output Buffer Turn-Off Delay (Ref. $\overline{OE}$)	0	30	0	40	0	50	
12	t_{CEA}	t_{ELQV}	Access Time From $\overline{CE}$		120		150		200	
13	t_{CEZ}	t_{EHQZ}	Output Buffer Turn Off Delay (Ref. $\overline{CE}$)	0	30	0	40	0	50	
14	t_{WCS}	t_{WLEL}	Write Command Set-Up Time (Ref. $\overline{CE}$)	−50		−60		−80		
15	t_{WCH}	t_{ELWH}	Write Command Hold Time (Ref. $\overline{CE}$)	50		60		80		
16	t_{WP}	t_{WLWH}	Write Pulse Width	30		40		50		
17	t_{DSC}	t_{DVEL}	Data-In Set-Up Time (Ref. $\overline{CE}$)	−5		−5		−5		
18	t_{DHC}	t_{ELDX}	Data-In Hold From $\overline{CE}$ (Early-Write)	50		60		80		
19	t_{WDC}	t_{ELWL}	Write Enable Delay From $\overline{CE}$	50		60		80		
20	t_{CHW}	t_{WLEH}	Chip Enable Hold Time After $\overline{W}$ (Late-Write)	30		40		50		
21	t_{DSW}	t_{DVWL}	Data-In Set-Up Time (Ref. $\overline{W}$)	0		0		0		
22	t_{DHW}	t_{WLDX}	Data-In Hold Time From $\overline{W}$ (Late-Write)	30		40		50		
23	t_{FE}	t_{FLFH}	$\overline{RFSH}$ Pulse Width	120	10K	150	10K	200	10K	
24	t_{FLD}	t_{FHEL}	$\overline{RFSH}$ To $\overline{CE}$ Precharge Time	60		80		100		
25	t_{FP}	t_{FHFL}	$\overline{RFSH}$ Precharge Time	60		80		100		
26	t_{CFP}	t_{EHFL}	$\overline{CE}$ To $\overline{RFSH}$ Precharge Time	60		80		100		
27	t_{CFD}	t_{ELFL}	$\overline{CE}$ To $\overline{RFSH}$ Delay (Hidden-Refresh)	180		230		300		
28	t_{WFD}	t_{WLFL}	$\overline{W}$ To $\overline{RFSH}$ Delay (Hidden-Refresh)	100		130		150		
29	t_{REF}	(t_{REF})	Refresh Period		4ms		4ms		4ms	
30	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	g
31	t_{OFD}	t_{GLFL}	$\overline{OE}$ To $\overline{RFSH}$ Delay (Hidden-Refresh)	105		130		150		

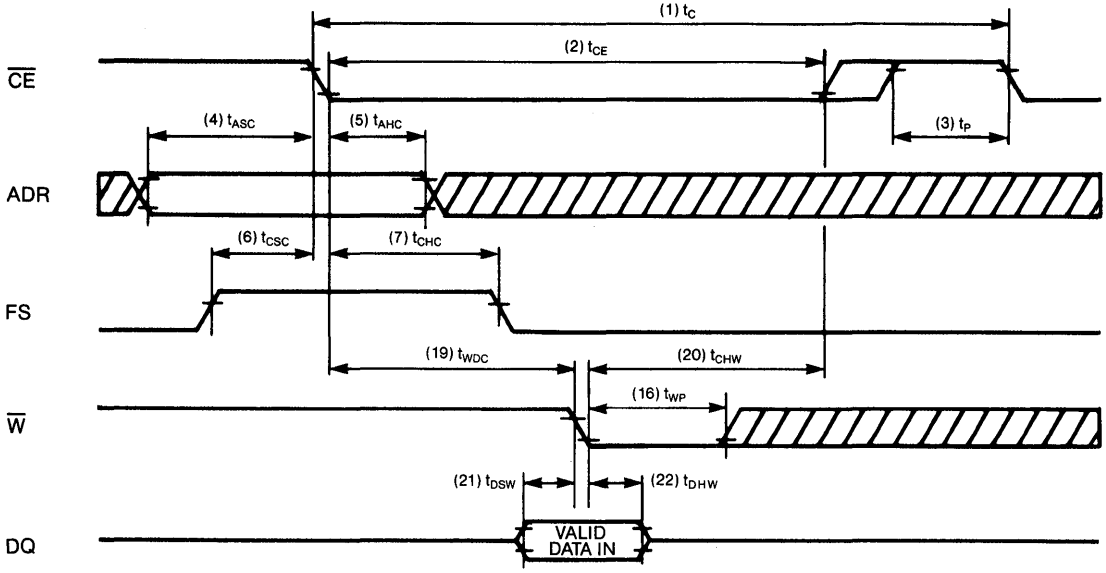
READ CYCLE ($\overline{RFSH} \geq V_{IH}$)



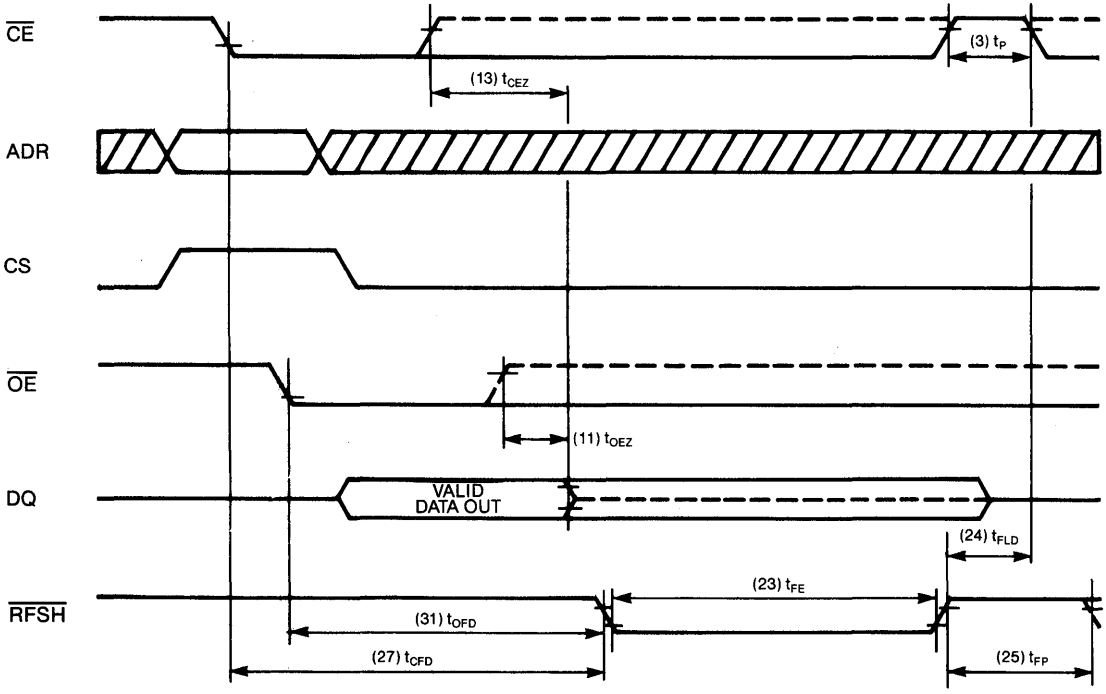
EARLY-WRITE CYCLE ($\overline{OE} \geq V_{IH}$, $\overline{RFSH} \geq V_{IH}$)



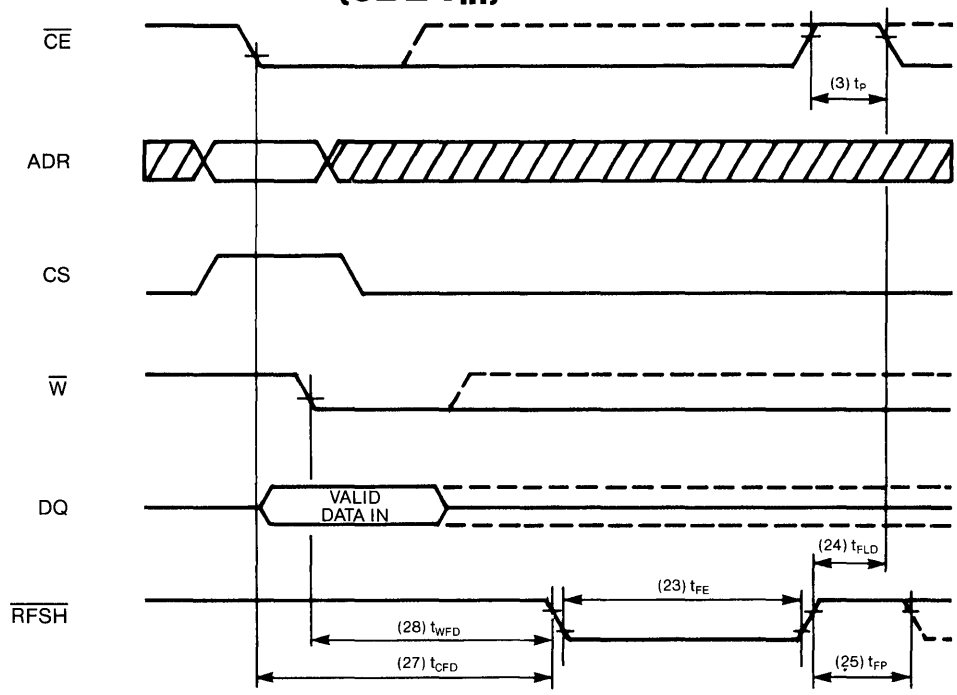
LATE-WRITE CYCLE ($\overline{OE} \geq V_{IH}$, $\overline{RFSH} \geq V_{IH}$)



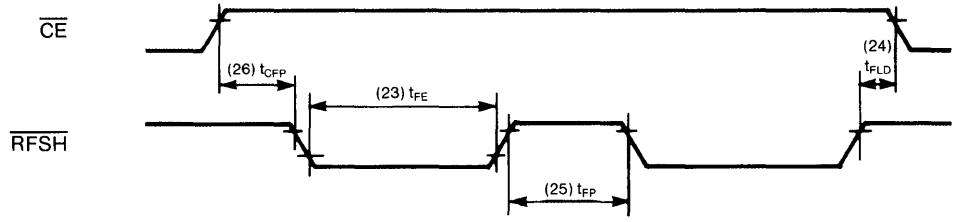
HIDDEN REFRESH CYCLE AFTER READ CYCLE COMPLETE ($\overline{W} \geq V_{IH}$)



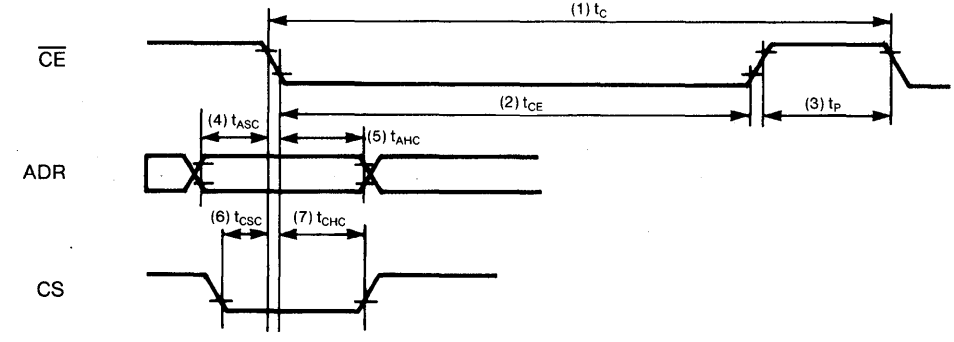
HIDDEN REFRESH CYCLE AFTER WRITE CYCLE COMPLETE ($\overline{OE} \geq V_{IH}$)



RFSH REFRESH CYCLE ($\overline{OE}$, $\overline{W}$, CS = DON'T CARE)



CE REFRESH CYCLE CS $\leq V_{IL}$, RFSH $\geq V_{IH}$, $\overline{OE}$, $\overline{W}$ = DON'T CARE (UNSELECTED CYCLE)



ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS2630	120ns	PLASTIC DIP	IMS2630P-12
	150ns	PLASTIC DIP	IMS2630P-15
	200ns	PLASTIC DIP	IMS2630P-20

IMS2800
High Performance 256K x 1 CMOS Dynamic RAM

FEATURES

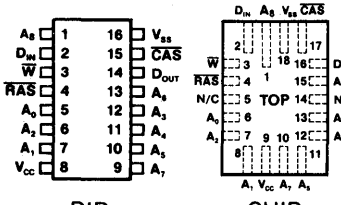
- Ultra High Speed—60, 80, 100, 120 and 150ns $\overline{RAS}$ Access Times Over Full V_{CC} (4.5V to 5.5V) and Temperature (0°C to 70°C) Ranges
- Eliminates Traditional DRAM Multiplexed Address Timing Constraints
- Inmos Advanced Field Shield Isolated CMOS Process Optimized for Speed
- All Inputs and Outputs are CMOS as Well as TTL Compatible
- Low Power (CMOS Input Levels)
  Standby—10mW
  Active—350mW at 120ns Cycle Times
- JEDEC Standard Pinout
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh as Well as $\overline{RAS}$ Only Refresh
- 4.4ms, 256 Cycle Refresh
- Single 5V ± 10% Supply
- Extended $\overline{RAS}$ Active Time to Facilitate Multiple Accesses Within a Row

DESCRIPTION

The IMS2800 is a 256K x 1 dynamic RAM that has been designed and processed for ultra high performance. The IMS2800 is fabricated with INMOS' advanced CMOS process resulting in low power while providing extremely wide operating margins as well as ultra high speed. The use of a Pseudo P-Well CMOS approach results in considerably lower soft error rates (Better than 64K dynamic RAMs). Furthermore, the use of $V_{CC/2}$ bit line precharging reduces on-chip internal noise, lowers average operating supply current, and reduces transient currents.

Innovative features as well as standard functional options on the IMS2800 provide the system designer with unprecedented DRAM memory design flexibility. With previous generations of DRAM products, the system designer was unable to take full advantage of the device performance of high speed DRAMs because of timing overhead associated with time division multiplexing the addresses. The IMS2800 chip design relieves this con-

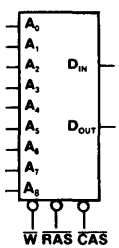
PIN CONFIGURATION



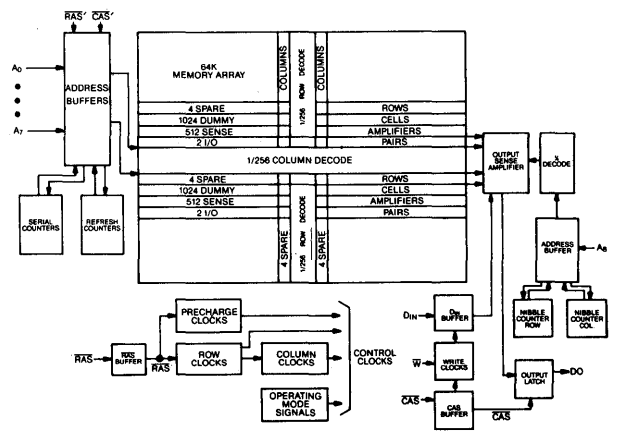
DIP CHIP CARRIER†

†Available in ceramic and plastic.

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_8	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{W}$	WRITE ENABLE
V_{CC}	+5 VOLT SUPPLY INPUT
V_{SS}	GROUND

straint by using asynchronous column address decoding in combination with on-chip transparent row address latches which allows a short (4ns; 2ns set-up and 2ns hold) row address capture window. This results in the performance limiting constraints associated with multiplexing the addresses being virtually eliminated. Now, it is possible to achieve system $\overline{RAS}$ access times as fast as 60ns which allows interfacing to the next generation of high speed microprocessors with no wait state penalty. Furthermore, systems that can take advantage of the asynchronous column address accessing (Static Column Decode) via page mode operations can achieve performance levels previously impossible without the use of high speed static RAMs.

The IMS2800 is a cost effective VLSI DRAM for applications that demand high density, reliability, high performance, and extremely wide operating margins. Inmos' improved address multiplexing technique utilizing Static Column Decoding (SCD) provides high density and ultra high performance without paying the power and cost penalties of using static RAM.

GENERAL

All cycles of the IMS2800 are initiated by a high-to-low transition of $\overline{RAS}$. For Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only refresh cycles, the high to low transition of $\overline{RAS}$ causes the state of the 9 external address lines (A0 through A8) to be latched. Eight of the nine address bits are decoded to select one of 256 rows. The ninth row address bit (A8) is saved and becomes part of the ten bit column address which selects one of the 1024 column locations. The IMS2800 uses a transparent latch to capture the row addresses which permits an extremely short capture time for the row addresses with only a 2ns set-up and 2ns hold required. After the short row address capture time has been satisfied, the 9 external address lines can be changed to the column address. Since column address decoding on the IMS2800 is static (asynchronous or ripple-through), no address strobes are required to select 1 bit location out of the 512 column locations within the selected row address field. However, after the high-to-low transition of $\overline{RAS}$, the state of $\overline{CAS}$ and $\overline{W}$ determine whether the cycle is a Read, Write, Read-Modify-Write, or a $\overline{RAS}$-Only refresh cycle.

READ CYCLE

A read cycle is performed on one or more memory locations if $\overline{W}$ is high while both $\overline{RAS}$ and $\overline{CAS}$ are low. With $\overline{RAS}$ and $\overline{CAS}$ low while $\overline{W}$ is high, the output will reflect the contents of the cell addressed by the 9 latched row addresses and the current 9 column addresses provided that all read cycle (or Write-Verify/Write-Read cycle) timing conditions have been satisfied. Asynchronous page operations, where more than one location can be accessed during a single $\overline{RAS}$ active cycle, can be executed by simply changing the column address whenever a new bit within the present page (defined by the 9 latched row addresses) is being accessed. It is not necessary to toggle $\overline{CAS}$ in order to perform page mode read operations, but $\overline{CAS}$ can be toggled, if desired, for the purpose of enabling or disabling the data output buffers.

WRITE CYCLES

The IMS2800 will perform three types of write cycles: Early-Write, Late-Write, and Read-Modify-Write. A write cycle is initiated when $\overline{W}$, $\overline{CAS}$, and $\overline{RAS}$ are low.

If $\overline{W}$ goes low prior to $\overline{CAS}$ going low, an Early-Write cycle is executed. Early-Write cycles are initiated by the falling edge of $\overline{CAS}$ with set-up and hold times for both data-in and column addresses (Column addresses latched during Write cycles to provide additional noise immunity as well as allow pipelined write operations.) being referenced to the falling edge of $\overline{CAS}$. During Early-Write cycles, the data out will remain open (high impedance state) as long as $\overline{W}$ remains low. If $\overline{W}$ goes high following an Early-Write cycle, while $\overline{RAS}$ and $\overline{CAS}$ both remain low, the IMS2800 will execute a Write-Verify or a Write-Read cycle (See timing diagram).

If $\overline{CAS}$ goes low prior to $\overline{W}$ going low, a Late-Write is executed. Late-Write cycles are intiated by the falling edge of $\overline{W}$ with the set-up and hold times for both data-in and column addresses being referenced to the falling edge of $\overline{W}$. Prior to the $\overline{W}$ control input being asserted for a Late-Write cycle, all the input conditions for a read operation are satisfied ($\overline{RAS}$ and $\overline{CAS}$ are both low and $\overline{W}$ is high). If $\overline{W}$ is asserted after a valid read access occurs, the operation is called a Read-Modify-Write cycle. During a Read-Modify-Write cycle, the Data-out will reflect the contents of the addressed cell before it was written until $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ go high. A Late-Write cycle where $\overline{W}$ is brought low prior to output data accessing will result in an indeterminate data output state, but whatever state was present at the time $\overline{W}$ goes low will be latched until $\overline{RAS}$, $\overline{CAS}$, or $\overline{W}$ go high.

REFRESH CYCLES

Dynamic RAMs retain data by storing charge on a capacitor. Since the charge will leak away over a period of time, it is necessary to access the data in the cell (capacitor) periodically in order to fully restore the stored charge while it is still at a sufficiently high level to be properly detected. For the IMS2800, any $\overline{RAS}$ sequence will fully refresh all storage cells within the single row addressed. To ensure that all cells remain sufficiently refreshed, all 256 rows (all binary combinations of address bits A0 through A7 must be refreshed every 4.4 mS.)

The addressing of the rows for refresh may be sourced either externally or internally. If the refresh row addresses are to be provided from an external source, $\overline{CAS}$ must be high when $\overline{RAS}$ goes low. If $\overline{CAS}$ is high when $\overline{RAS}$ goes low, any type of cycle (Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only) will cause the externally addressed row to be refreshed.

If $\overline{CAS}$ is low when $\overline{RAS}$ falls, the IMS2800 will use an internal 8-bit counter as the source of the row addresses and will ignore the $\overline{W}$ (Write Enable) and the external address inputs. $\overline{CAS}$-Before-$\overline{RAS}$ refresh mode is a refresh-only mode. Also, $\overline{CAS}$-Before-$\overline{RAS}$ refresh does not cause device selection and the state of the data-out will remain unchanged as long as $\overline{CAS}$ remains low.

ABSOLUTE MAXIMUM RATINGS*[a]

Voltage on V_{CC} Relative to V_{SS} . . . . . −1.0V to +7.0V
Storage Temp. (Ceramic Package) . . −65°C to +150°C
Storage Temp. (Plastic Package) . . . . −55°C to +125°C
Power Dissipation. 1W
Short Circuit Output Current. 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS[a, b]

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage		0		V	
V_{IH}	Logic "1" Voltage	2.4		V_{CC} + 1	V	
V_{IL}	Logic "0" Voltage	−1.0V		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	Still Air

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current (Operating)		70 60 45	mA mA mA	t_{RL2RL2} = 121ns t_{RL2RL2} = 150ns (c) t_{RL2RL2} = 200ns
I_{CC_2}	V_{CC} Power Supply Current (Active)		15	mA	$\overline{RAS} \leq V_{IL}$ (max), $\overline{CAS} \leq V_{IL}$ (max) (d)
I_{CC_3}	Standby Current		2.5 4.5 4.0 5.5	mA mA mA mA	All inputs stable at CMOS levels, $\overline{RAS} \geq (V_{CC} - .4V)$. All inputs stable at TTL levels $\overline{RAS} \geq 2.4V$. All inputs toggling between CMOS levels at 6.25MHZ, $\overline{RAS} \geq (V_{CC} - .4V)$. (e) All inputs (except $\overline{RAS}$) toggling between TTL levels at 6.25MHZ.
I_{IN}	Input Leakage Current (Any Input)	−10	10	μA	$0V \leq V_{IN} \leq 5.5V$, others = 0V
I_{OLK}	Output Leakage Current	−10	10	μA	D_{OUT} = Hi Z, $0V \leq V_{OUT} \leq 5.5V$
V_{OH}	Output High Voltage	2.4		V	$I_O = -5.0mA$
V_{OL}	Output Low Voltage		0.4	V	$I_O = 5.0mA$

Note a: All voltage values in this data sheet are with respect to V_{SS}.
b: After power-up, a pause of 1ms followed by eight initialization memory cycles is required to achieve proper device operation. Any interval greater than 4.4ms with $\overline{RAS}$ inactivity requires eight reinitialization cycles to achieve proper device operation.
c: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with output open.
d: DC current after t_{RLQV} (max), t_{CLQV} (max), and t_{AVQV} delay.
e: CMOS levels are defined as V_{IH} (min) $\geq (V_{CC} - .4V)$ and V_{IL} (max) $\leq 0.4V$. TTL levels are defined as V_{IH} (min) $\geq 2.4V$ and V_{IL} (max) $\leq 0.8V$.

AC TEST CONDITIONS

Input Pulse Levels. . . . . 0 to 3V
Input Rise and Fall Times. . . . . 3ns between 0.8 and 2.4V
Input Timing Reference Levels. . . . . 0.8 and 2.4V
Output Timing Reference Levels. . . . . 0.8 and 2.4V
Output Load. . . . . Equivalent to 2 TTL Loads and 50pF

CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS	COND.
C_{IN}	Input Cap. $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	6	pF	d
C_{IN}	Input Cap. Addresses	5	pF	d
C_{OUT}	Output Cap.	7	pF	d o

Note d: Capacitance measured with BOONTON METER.
o: $\overline{CAS} = V_{IH}$ to disable D_{OUT}

AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2800-60		2800-80		2800-100		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{AVAV}	Address Cycle	35		46		56		ns	
2	t_{AVCL2}	Column Address Set-Up (Early Write)	0		0		0		ns	h
3	t_{AVQV}	Column Address Access		32		43		53	ns	
4	t_{AVRL2}	Row Address Set-Up	2		2		2		ns	
5	t_{AVWL2}	Column Address Set-Up (Late Write)	0		0		0		ns	h
6	t_{AXQX}	Output Hold	5		5		5		ns	
7	t_{CH1QZ}	Output Hold	2		2		2		ns	f
8	t_{CH2CL2}	$\overline{CAS}$ Precharge	5		5		5		ns	
9	t_{CH2QZ}	Output Turn-Off Delay		15		15		15	ns	f
10	t_{CH2RL2}	$\overline{CAS}$ To $\overline{RAS}$ Set-Up (Non-$\overline{CAS}$ Before $\overline{RAS}$ Refresh)	2		2		2		ns	
11	t_{CH2WX}	Read Command Hold Time (Reference $\overline{CAS}$)	0		0		0		ns	g
12	t_{CL1AX}	Column Address Hold (Early Write)	6		8		9		ns	h
13	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Read)	11		13		16		ns	
14	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Write)	5		5		5		ns	
15	t_{CL1DX}	Data-In Hold (Early Write)	6		8		9		ns	
16	t_{CL1QV}	$\overline{CAS}$ Access		11		13		16	ns	
17	t_{CL1QVN}	$\overline{CAS}$ To Data (Write-Verify/Write-Read)		50		60		70	ns	
18	t_{CL1RH1}	$\overline{CAS}$ To $\overline{RAS}$ Lead	15		20		25		ns	
19	t_{CL1RL2}	$\overline{CAS}$ To $\overline{RAS}$ Set-Up (Refresh)	2		2		2		ns	
20	t_{CL1WH1}	Write Hold (Reference $\overline{CAS}$)	5		5		5		ns	
21	t_{CL1WL2}	$\overline{CAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	11		13		16		ns	i
22	t_{CL2CL2}	Page Read/Write Cycle	35		40		45		ns	
23	t_{CL2QX}	Output Turn-On Delay	0		0		0		ns	
24	t_{DVCL2}	Early Write Data Set-Up (Early Write)	0		0		0		ns	h
25	t_{DVWL2}	Late Write Data Set-Up	0		0		0		ns	
26	t_{RH2AX}	Address Hold Without Data Change	0		0		0		ns	
27	t_{RH2RL2}	$\overline{RAS}$ Precharge	55		65		70		ns	
28	t_{RH2WX}	Read Command Hold Time (Reference $\overline{RAS}$)	0		0		0		ns	g
29	$t_{RL1A(C)X}$	Column Address Hold (Write)	40		45		50		ns	
30	t_{RL1AX}	Row Address Hold	2		2		2		ns	

AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2800-120		2800-150		UNITS	NOTES
			MIN	MAX	MIN	MAX		
1	t_{AVAV}	Address Cycle	63		78		ns	
2	t_{AVCL2}	Column Address Set-Up (Early Write)	0		0		ns	h
3	t_{AVQV}	Column Address Access		60		75	ns	
4	t_{AVRL2}	Row Address Set-Up	2		2		ns	
5	t_{AVWL2}	Column Address Set-Up (Late Write)	0		0		ns	h
6	t_{AXQX}	Output Hold	5		5		ns	
7	t_{CH1QZ}	Output Hold	2		2		ns	f
8	t_{CH2CL2}	$\overline{CAS}$ Precharge	5		5		ns	
9	t_{CH2QZ}	Output Turn-Off Delay		15		20	ns	f
10	t_{CH2RL2}	$\overline{CAS}$ To $\overline{RAS}$ Set-Up (Non-$\overline{CAS}$ Before $\overline{RAS}$ Refresh)	2		2		ns	
11	t_{CH2WX}	Read Command Hold Time (Reference $\overline{CAS}$)	0		0		ns	g
12	t_{CL1AX}	Column Address Hold (Early Write)	11		15		ns	h
13	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Read)	19		25		ns	
14	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Write)	5		10		ns	
15	t_{CL1DX}	Data-In Hold (Reference $\overline{CAS}$)	11		15		ns	
16	t_{CL1QV}	$\overline{CAS}$ Access		19		25	ns	
17	t_{CL1QVN}	$\overline{CAS}$ To Data Write-Read		80		100	ns	
18	t_{CL1RH1}	$\overline{CAS}$ To $\overline{RAS}$ Lead	30		40		ns	
19	t_{CL1RL2}	$\overline{CAS}$ To $\overline{RAS}$ Set-Up (Refresh)	2		2		ns	
20	t_{CL1WH1}	Write Hold (Reference $\overline{CAS}$)	5		10		ns	
21	t_{CL1WL2}	$\overline{CAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	19		25		ns	i
22	t_{CL2CL2}	Page Read/Write Cycle	50		65		ns	
23	t_{CL2QX}	Output Turn-On Delay	0		0		ns	
24	t_{DVCL2}	Early Write Data Set-Up (Early Write)	0		0		ns	h
25	t_{DVWL2}	Late Write Data Set-Up	0		0		ns	
26	t_{RH2AX}	Address Hold Without Data Change	0		0		ns	
27	t_{RH2RL2}	$\overline{RAS}$ Precharge	75		90		ns	
28	t_{RH2WX}	Read Command Hold Time (Reference $\overline{RAS}$)	0		0		ns	g
29	$t_{RL1A(C)X}$	Column Address Hold (Write)	55		75		ns	
30	t_{RL1AX}	Row Address Hold	2		2		ns	

AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2800-60		2800-80		2800-100		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
31	t_{RL1CH1}	$\overline{CAS}$ Hold ($\overline{CAS}$-Before-$\overline{RAS}$)	2		2		2		ns	
32	t_{RL1CH1}	$\overline{CAS}$ Hold (Early Write)	40		45		50		ns	
33	t_{RL1CL2}	$\overline{CAS}$ Hold (Non Refresh)	2		2		2		ns	
34	t_{RL1DX}	Data Hold (Early Write)	8		10		12		ns	
35	t_{RL1QV}	$\overline{RAS}$ Access		60		80		100	ns	
36	t_{RL1RH1}	$\overline{RAS}$ Pulse Width	60	10^5	80	10^5	100	10^5	ns	
37	t_{RL1WH1}	Write Command Hold (Reference $\overline{RAS}$)	40		45		50		ns	
38	t_{RL1WL2}	$\overline{RAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	60		80		100		ns	i
39	t_{RL2RL2}	Random Read/Write Cycle	121		151		176		ns	
40	t_{WH1QX}	Output Hold	0		0		0		ns	
41	t_{WH2CL2}	Read Command Set-Up	0		0		0		ns	
42	t_{WH2QVN}	$\overline{W}$ High to Data (Write-Verify or Write-Read Cycle)		11		13		16	ns	
43	t_{WH2WL2}	Write Precharge	5		5		5		ns	
44	t_{WL1AX}	Column Address Hold (Late Write)	5		5		5		ns	h
45	t_{WL1CH1}	Write To $\overline{CAS}$ Delay	5		5		5		ns	
46	t_{WL1CL2}	Early Write $\overline{W}$ Set-Up	0		0		0		ns	i
47	t_{WL1DX}	Data-In Hold (Late Write)	5		7		8		ns	h
48	t_{WL1QV}	$\overline{W}$ To Data After Late Write		35		40		45	ns	
49	t_{WL1QVN}	Write/Read Cycle (Write-Verfiy/Write-Read Access)		55		74		92	ns	
50	t_{WL1RH1}	Write To $\overline{RAS}$ Lead	15		15		15		ns	
51	t_{WL1WH1}	Write Pulse	5		5		5		ns	
52	t_{REF}	Refresh Period		4.4		4.4		4.4	ms	
53	t_T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	j, k

NOTES:

f. Q_Z is defined as the time at which the output achieves the open circuit condition.

g. Either t_{CH2WX} or t_{RH2WX} must be satisfied for a Read cycle.

h. Address and data set-up and hold times referenced to $\overline{CAS}$ (t_{AVCL2}, t_{CL1AX}, t_{DVCL2}, and t_{CL1DX}) are restrictive parameters for Early-Write operations only. Address and data set-up times referenced to $\overline{W}$ (t_{AVWL2}, t_{WL1AX}, t_{DVWL2}, and t_{WL1DX}) are restrictive parameters for Late-Write and Read-Modify-Write cycle operations only.

i. t_{WH2CL2}, t_{CL1WL2}, and t_{RL1WL2} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only. If $t_{WL1CL2} \geq t_{WL1CL2}$ (min) the cycle is an Early-Write cycle and data will remain open circuit unless $\overline{W}$ goes high while $\overline{CAS}$ and $\overline{RAS}$ are both low. If $t_{WH2CL2} \geq t_{WH2CL2}$ (min), $t_{RL1WL2} \geq t_{RL1WL2}$ (min), and $t_{AVQV} \geq t_{AVQV}$ (min) the cycle is a Read-Write and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out is indeterminate at access time and remains so until either $\overline{CAS}$ or $\overline{W}$ returns to V_{IH}.

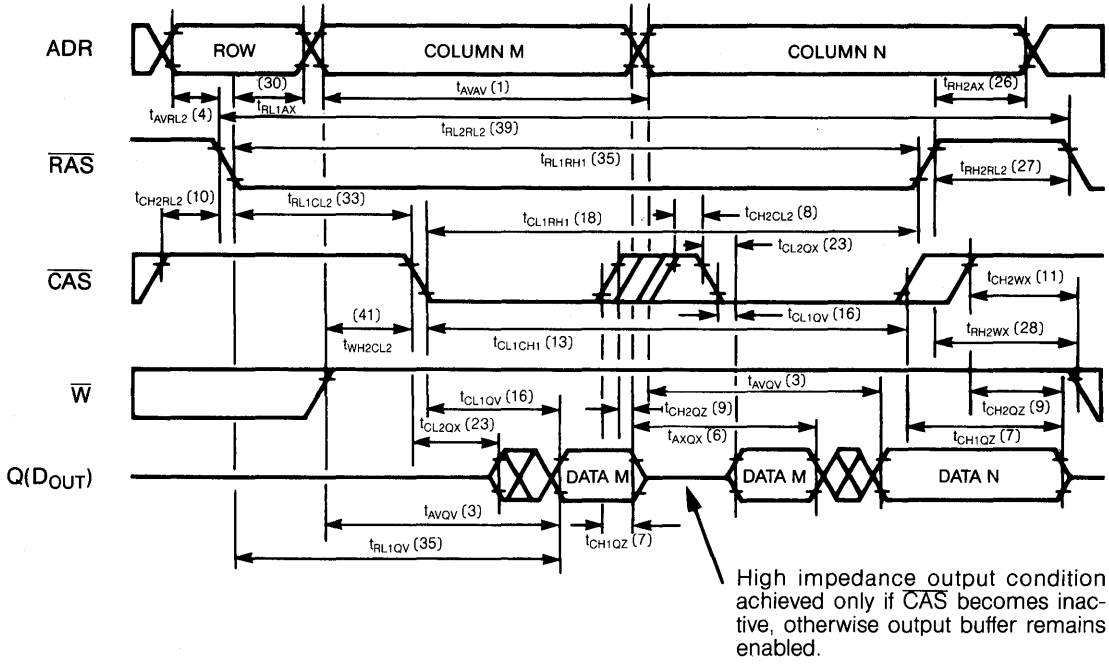
j. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Transition time is measured between V_{IL} (max) and V_{IH} (min).

k. 3ns rise and fall times (t_T) are used for cycle time specifications.

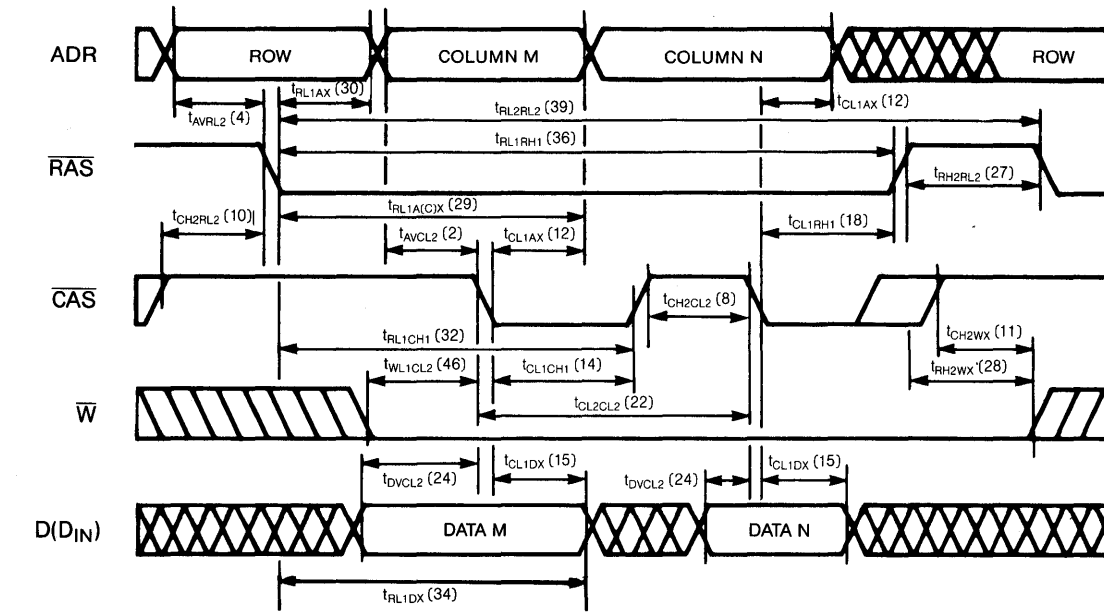
AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2800-120		2800-150		UNITS	NOTES
			MIN	MAX	MIN	MAX		
31	t_{RL1CH1}	$\overline{CAS}$ Hold ($\overline{CAS}$-Before-$\overline{RAS}$)	2		2		ns	
32	t_{RL1CH1}	$\overline{CAS}$ Hold (Early Write)	55		70		ns	
33	t_{RL1CL2}	$\overline{CAS}$ Hold (Non Refresh)	2		2		ns	
34	t_{RL1DX}	Data Hold (Early Write)	15		25		ns	
35	t_{RL1QV}	$\overline{RAS}$ Access		120		150	ns	
36	t_{RL1RH1}	$\overline{RAS}$ Pulse Width	120	10^5	150	10^5	ns	
37	t_{RL1WH1}	Write Command Hold (Reference $\overline{RAS}$)	55		70		ns	
38	t_{RL1WL2}	$\overline{RAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	120		150		ns	i
39	t_{RL2RL2}	Random Read/Write Cycle	201		246		ns	
40	t_{WH1QX}	Output Hold	0		0		ns	
41	t_{WH2CL2}	Read Command Set-Up	0		0		ns	
42	t_{WH2QVN}	$\overline{WE}$ High To D. (Write-Verify or Write-Read Cycle)		19		25	ns	
43	t_{WH2WL2}	Write Precharge	5		10		ns	
44	t_{WL1AX}	Column Address Hold (Late Write)	5		10		ns	h
45	t_{WL1CH1}	Write To $\overline{CAS}$ Delay	5		10		ns	
46	t_{WL1CL2}	Early Write $\overline{WE}$ Set-Up	0		0		ns	i
47	t_{WL1DX}	Data-In Hold (Late Write)	10		15		ns	h
48	t_{WL1QV}	$\overline{WE}$ To Data After Late Write		50		65	ns	
49	t_{WL1QVN}	Write/Read Cycle		110		140	ns	
50	t_{WL1RH1}	Write To $\overline{RAS}$ Lead	15		20		ns	
51	t_{WL1WH1}	Write Pulse	5		10		ns	
52	t_{REF}	Refresh Period		4.4		4.4	ms	
53	t_T	Transition Time (Rise and Fall)	2	50	2	50	ns	j, k

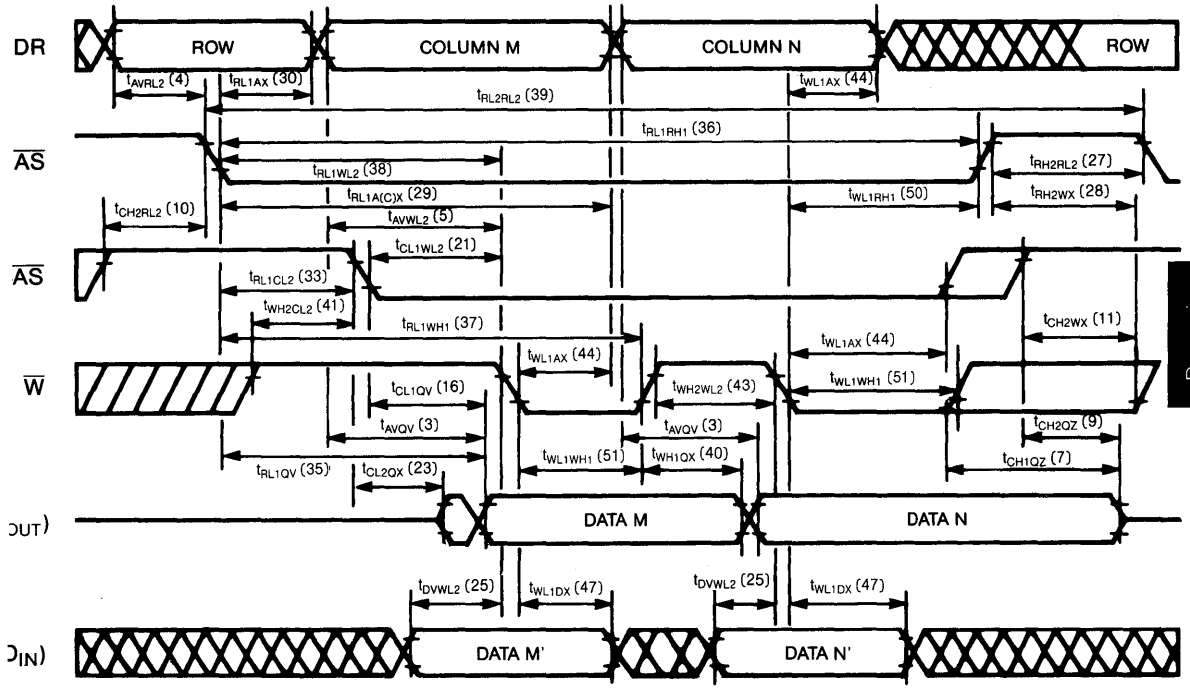
READ CYCLE



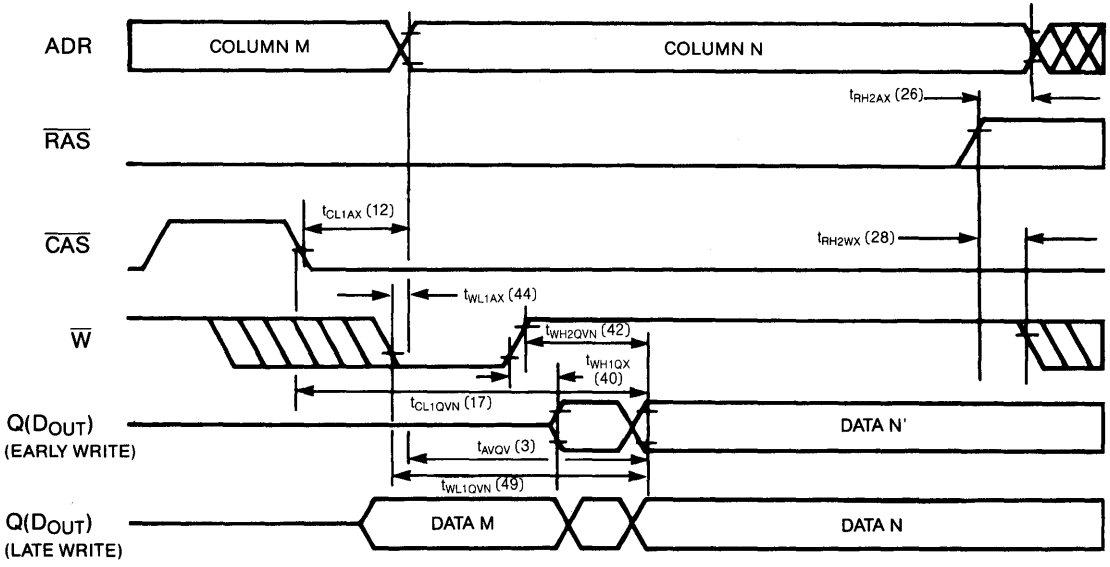
EARLY-WRITE CYCLE



.ATE-WRITE/READ-MODIFY-WRITE CYCLE

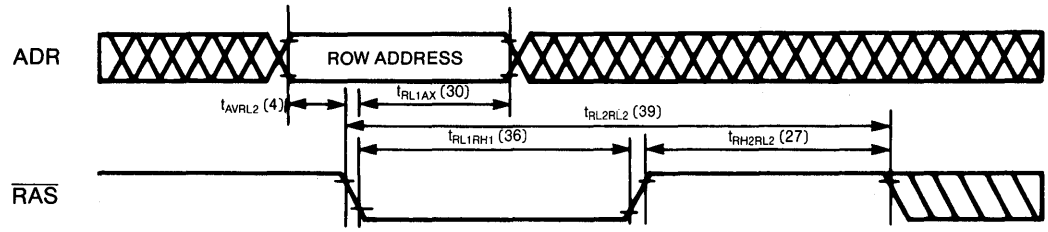


WRITE-VERIFY/WRITE-READ CYCLE

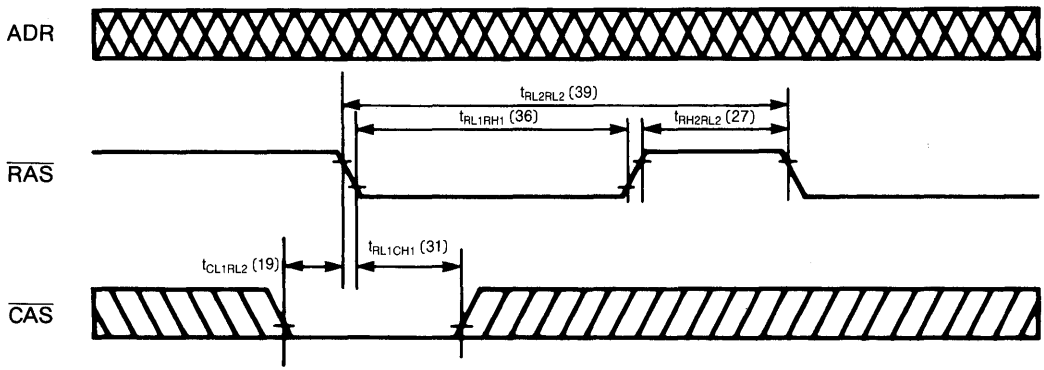


If Column Address N = Column Address M, Cycle is Write-Verify.

$\overline{RAS}$ ONLY REFRESH [$\overline{CAS} \geq V_{IH}$ (MIN)]



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH



APPLICATION

To ensure proper operation of the IMS2800 in a system environment it is recommended that the following guidelines be followed.

POWER DISTRIBUTION

Transient currents are required by dynamics RAMs. These transient current spikes can cause significant power supply and ground noise unless adequate power distribution and decoupling is used. The recommended power distribution scheme combines proper trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (8) through the decoupling capacitor, to the ground pin (16) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line and the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. To prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry. A high-frequency decoupling capacitor with a value of 0.1μF, should be placed between the rows of memory devices in the array. A larger tantalum capacitor with a value beteween 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propogating down the lines, especially low-going TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver/termination combination close to the memory array. Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are among the most important, yet basic guidelines to be followed. These guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS2800	60ns	PLASTIC DIP	IMS2800P-60
	60ns	CERAMIC DIP	IMS2800S-60
	60ns	CERAMIC CHIP CARRIER	IMS2800W-60
	60ns	PLASTIC CHIP CARRIER	IMS2800J-60
	80ns	PLASTIC DIP	IMS2800P-80
	80ns	CERAMIC DIP	IMS2800S-80
	80ns	CERAMIC CHIP CARRIER	IMS2800W-80
	80ns	PLASTIC CHIP CARRIER	IMS2800J-80
	100ns	PLASTIC DIP	IMS2800P-100
	100ns	CERAMIC DIP	IMS2800S-100
	100ns	CERAMIC CHIP CARRIER	IMS2800W-100
	100ns	PLASTIC CHIP CARRIER	IMS2800J-100
	120ns	PLASTIC DIP	IMS2800P-120
	120ns	CERAMIC DIP	IMS2800S-120
	120ns	CERAMIC CHIP CARRIER	IMS2800W-120
	120ns	PLASTIC CHIP CARRIER	IMS2800J-120
	150ns	PLASTIC DIP	IMS2800P-150
	150ns	CERAMIC DIP	IMS2800S-150
	150ns	CERAMIC CHIP CARRIER	IMS2800W-150
	150ns	PLASTIC CHIP CARRIER	IMS2800J-150

IMS2801
High Performance 256K x 1 CMOS Dynamic RAM

Preliminary

FEATURES

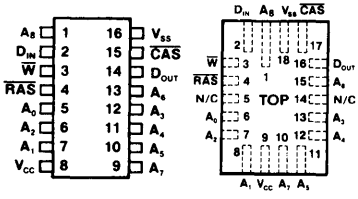
- Ultra High Speed—60, 80, 100, 120 and 150ns $\overline{RAS}$ Access Times Over Full V_{CC} (4.5V to 5.5V) and Temperature (0°C to 70°C) Ranges
- Eliminates Traditional DRAM Multiplexed Address Timing Constraints
- Inmos Advanced Field Shield Isolated CMOS Process Optimized for Speed
- All Inputs and Outputs are CMOS as Well as TTL Compatible
- Low Power (CMOS Input Levels)
  Standby—10mW
  Active—350mW at 120ns Cycle Times
- JEDEC Standard Pinout
- $\overline{CAS}$-Before-$\overline{RAS}$ Refresh as Well as $\overline{RAS}$ Only Refresh
- 4.4ms, 256 Cycle Refresh
- Single 5V ± 10% Supply
- Extended $\overline{RAS}$ Active Time to Facilitate Multiple Accesses Within a Row

DESCRIPTION

The IMS2801 is a 256K x 1 dynamic RAM that has been designed and processed for ultra high performance. The IMS2801 is fabricated with INMOS' advanced CMOS process resulting in low power while providing extremely wide operating margins as well as ultra high speed. The use of a pseudo P-Well CMOS approach results in considerably lower soft error rates (Better than 64K RAMs). Furthermore, the use of $V_{CC/2}$ bit line precharging reduces on-chip internal noise, lowers average operating supply current, and reduces transient currents.

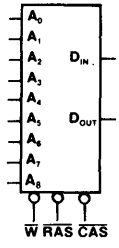
Innovative features as well as standard functional options on the IMS2801 provide the system designer with unprecedented DRAM memory design flexibility. With previous generations of DRAM products, the system designer was unable to take full advantage of the device performance of high speed DRAMs because of the timing overhead associated with address multiplexing.

PIN CONFIGURATION

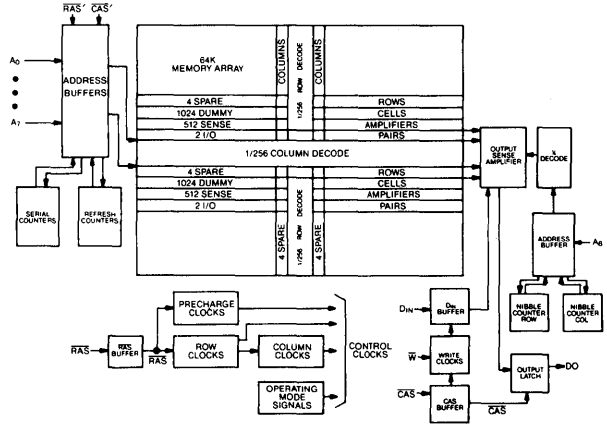


†Available in ceramic and plastic.

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_8	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{W}$	WRITE ENABLE
V_{CC}	+5 VOLT SUPPLY INPUT
V_{SS}	GROUND

DESCRIPTION (continued)

The IMS2801 uses on-chip high speed transparent address latches to capture both Row and Column addresses. This results in the performance limiting constraints associated with multiplexing the addresses being virtually eliminated. Now, it is possible to achieve system access times as fast as 60nS which allows interfacing to the next generation of high speed microprocessors with no wait state penalty. Furthermore, systems that can take advantage of fast page mode operations can achieve performance levels previously impossible without the use of high speed static RAMs.

The IMS2801 is a cost effective VLSI DRAM for applications that demand high density, reliability, high performance, and extremely wide operating margins. Inmos' improved address multiplexing technique utilizing fast capture transparent row and column address latches provides high density and ultra high performance without paying the power and cost penalties of using static RAM.

GENERAL

All cycles of the IMS2801 are initiated by a high-to-low transition of $\overline{RAS}$. For Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only refresh cycles, the high to low transition of $\overline{RAS}$ causes the state of the 9 external address lines (A0 through A8) to be latched. Eight of the nine address bits are decoded to select one of 256 rows. The ninth row address bit (A8) is saved and becomes part of the ten bit column address which selects one of the 1024 column locations. The IMS2801 uses transparent latches to capture the row addresses which permits an extremely short capture time for the row addresses with only a 2nS set-up and 2nS hold required. After the short row address capture time has been satisfied, the 9 external address lines can be changed to the column address. Column address decoding on the IMS2801 is static (asynchronous or ripple-through; Static Column Decoded) whenever $\overline{CAS}$ is high but the column addresses are latched when $\overline{CAS}$ is low. This provides the advantages of statically decoded column accessing while maintaining compatibility with conventional DRAMs. After the high-to-low transition of $\overline{RAS}$, the state of $\overline{CAS}$ and $\overline{W}$ determine whether the cycle is a Read, Write, Read-Modify-Write, or a $\overline{RAS}$-Only refresh cycle. The cycle is terminated by bringing $\overline{RAS}$ high. A new cycle may be initiated after $\overline{RAS}$ has been high for the specified precharge interval [t_{RH2RL2} (min)]. $\overline{RAS}$ and $\overline{CAS}$ must be properly overlapped and once brought low they must remain low for their specified pulse widths.

READ CYCLE

A read cycle is performed on one or more memory locations if $\overline{W}$ is high while both $\overline{RAS}$ and $\overline{CAS}$ are low. During a read cycle, at access time the output will reflect the contents of the cell addressed by the 9 latched row and column addresses. The read access time is determined by t_{RL1QV}, t_{AVQV}, or t_{CL1QV}, whichever is greatest. When data is accessed, the data output is entirely under the control of $\overline{CAS}$; accessed data will remain valid as long as $\overline{CAS}$ remains active even if a $\overline{RAS}$ sequence occurs while $\overline{CAS}$ is held low.

WRITE CYCLES

A write cycle is initiated when $\overline{W}$, $\overline{CAS}$, and $\overline{RAS}$ are low. The IMS2801 will perform three types of write cycles: write cycles supported are Early-Write, Late-Write, and Read-Modify-Write.

During a $\overline{RAS}$ active cycle, if $\overline{W}$ goes low prior to $\overline{CAS}$ going low, an Early-Write cycle is executed. Early-Write cycles are initiated by the falling edge of $\overline{CAS}$ with set-up and hold times for both data-in and column addresses referenced to the falling edge of $\overline{CAS}$. With Early-Write cycles, the data out will remain open (high impedance state).

If $\overline{CAS}$ goes low prior to $\overline{W}$ going low, a Late-Write cycle is executed. Late-Write cycles are initiated by the falling edge of $\overline{W}$ with set-up and hold times for both data-in and column addresses referenced to the falling edge of $\overline{W}$. If $\overline{W}$ is asserted after a valid read access occurs, the operation is called a Read-Modify-Write cycle. During a Read-Modify-Write cycle, the data-out will reflect the contents of the addressed cell before it was written until the output is turned off (high impedance state) by bringing $\overline{CAS}$ high.

The choice of write cycle timing is usually very system dependent and the different modes are made available to accommodate these differences. In general, the Early-Write timing is most appropriate for systems that have a bidirectional data bus. Because Q (data-out) remains inactive during Early-Write cycles, the D (data-in) and the Q (data-out) pins may be tied together without bus contention.

PAGE MODE CYCLES

Page mode operation permits access of up to 512 locations within a single $\overline{RAS}$ active cycle. The multiple locations in the same page can be randomly accessed by simply changing the column address inputs and cycling $\overline{CAS}$. Within a page mode cycle, any combination of Read, Write, Early Write or Late Write, or Read-Modify-Write cycles can be executed. Unlike traditional address multiplexed dynamic RAMs, the IMS2801 transparently latches the column addresses (column addresses are ripple-through decoded whenever $\overline{CAS}$ is high and latched when $\overline{CAS}$ is low) which permits column decoding to occur independently of the assertion of $\overline{CAS}$. Additionally, the falling edge of $\overline{CAS}$ acts as a high speed output enable for read cycles and performs a gating function during write cycles. Transparent column address latching allows high speed page mode accesses to be performed by simply changing the column address inputs whenever a new bit in the current page (defined by the 9 bit address field latched by the falling edge of $\overline{RAS}$) is to be accessed and toggling $\overline{CAS}$ high and then low. When $\overline{CAS}$ goes high the data-out buffers are turned off (high impedance) and when $\overline{CAS}$ is active the data-out drivers are turned on. Access during the page mode operation is determined by t_{RL1QV}, t_{AVQV}, and t_{CL1QV}, whichever is greatest.

ABSOLUTE MAXIMUM RATINGS*[a]

Voltage on V_{CC} Relative to V_{SS} . . . . . −1.0V to +7.0V
Storage Temp. (Ceramic Package) . . −65°C to +150°C
Storage Temp. (Plastic Package) . . . . −55°C to +125°C
Power Dissipation. 1W
Short Circuit Output Current. 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS[a, b]

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage		0		V	
V_{IH}	Logic "1" Voltage	2.4		V_{CC} + 1	V	
V_{IL}	Logic "0" Voltage	−1.0V		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	Still Air

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current (Operating)		70 60 45	mA mA mA	t_{RL2RL2} = 121ns t_{RL2RL2} = 150ns (c) t_{RL2RL2} = 200ns
I_{CC_2}	V_{CC} Power Supply Current (Active)		15	mA	$\overline{RAS} \leq V_{IL}$ (max), $\overline{CAS} \leq V_{IL}$ (max) (d)
I_{CC_3}	Standby Current		2.5 4.5 4.0 5.5	mA mA mA mA	All inputs stable at CMOS levels, $\overline{RAS} \geq (V_{CC} - .4V)$. All inputs stable at TTL levels, $\overline{RAS} \geq 2.4V$. All inputs toggling between CMOS levels at 6.25MHZ, $\overline{RAS} \geq (V_{CC} - .4V)$. (e) All inputs (except $\overline{RAS}$) toggling between TTL levels at 6.25MHZ.
I_{IN}	Input Leakage Current (Any Input)	−10	10	μA	$0V \leq V_{IN} \leq 5.5V$, others = 0V
I_{OLK}	Output Leakage Current	−10	10	μA	D_{OUT} = Hi Z, $0V \leq V_{OUT} \leq 5.5V$
V_{OH}	Output High Voltage	2.4		V	$I_O = -5.0mA$
V_{OL}	Output Low Voltage		0.4	V	$I_O = 5.0mA$

Note a: All voltage values in this data sheet are with respect to V_{SS}.
b: After power-up, a pause of 1ms followed by eight initialization memory cycles is required to achieve proper device operation. Any interval greater than 4.4ms with $\overline{RAS}$ inactivity requires eight reinitialization cycles to achieve proper device operation.
c: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with output open.
d: DC current after t_{RLQV} (max), t_{CLQV} (max), and t_{AVQV} delay.
e: CMOS levels are defined as V_{IH} (min) ≥ (V_{CC} −.4V) and V_{IL} (max) ≤ 0.4V. TTL levels are defined as V_{IH} (min) ≥ 2.4V and V_{IL} (max) ≤ 0.8V.

AC TEST CONDITIONS

Input Pulse Levels. . . . . 0 to 3V
Input Rise and Fall Times. . . . . 3ns between 0.8 and 2.4V
Input Timing Reference Levels. . . . . 0.8 and 2.4V
Output Timing Reference Levels. . . . . 0.8 and 2.4V
Output Load. . . . . Equivalent to 2 TTL Loads and 50pF

CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS	COND.
C_{IN}	Input Cap. $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	6	pF	d
C_{IN}	Input Cap. Addresses	5	pF	d
C_{OUT}	Output Cap.	7	pF	d o

Note d: Capacitance measured with BOONTON METER.
o: $\overline{CAS} = V_{IH}$ to disable D_{OUT}

AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2801-60		2801-80		2801-100		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{AVCL2}	Column Address Set-Up	0		0		0		ns	h
2	t_{AVQV}	Column Address Access		32		43		53		ns
3	t_{AVRL2}	Row Address Set-Up	2		2		2		ns	
4	t_{AVWL2}	Address Valid to $\overline{W}$ Active	0		0		0		ns	h, l
5	t_{CH1QZ}	Output Hold		2		2		2	ns	f
6	t_{CH2CL2}	$\overline{CAS}$ Precharge	5		5		5		ns	
7	t_{CH2QV}	Access from $\overline{CAS}$ High		32		43		53	ns	f
8	t_{CH2QZ}	Output Turn-Off Delay		15		15		15	ns	
9	t_{CH2RL2}	$\overline{CAS}$ Set-Up (Non-$\overline{CAS}$ Before $\overline{RAS}$ Refresh)	2		2		2		ns	
10	t_{CH2WX}	Read Command Hold (Reference $\overline{CAS}$)	0		0		0		ns	g
11	t_{CL1AX}	Column Address Hold	6		8		9		ns	h
12	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Read)	11		14		16		ns	
13	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Write)	5		5		5		ns	
14	t_{CL1DX}	Data-In Hold (Early Write)	6		8		9		ns	
15	t_{CL1QV}	$\overline{CAS}$ Access		11		13		16	ns	
16	t_{CL1RH1}	$\overline{CAS}$ To $\overline{RAS}$ Lead	15		20		25		ns	
17	t_{CL1RL2}	$\overline{CAS}$ Set-Up ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	2		2		2		ns	
18	t_{CL1WH1}	Write Hold (Reference $\overline{CAS}$)	5		5		5		ns	
19	t_{CL1WL2}	$\overline{CAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	11		13		16		ns	i
20	t_{CL2CL2}	Page Read/Write Cycle	35		40		45		ns	
21	t_{CL2QX}	Output Turn-On Delay	0		0		0		ns	
22	t_{DVCL2}	Data Set-Up (Early Write)	0		0		0		ns	h
23	t_{DVWL2}	Data Set-Up (Late Write)	0		0		0		ns	
24	t_{RH2RL2}	$\overline{RAS}$ Precharge	55		65		70		ns	
25	t_{RH2WX}	Read Command Hold Time (Reference $\overline{RAS}$)	0		0		0		ns	g
26	$t_{RL1A(C)X}$	Column Address Hold (Reference $\overline{RAS}$)	40		45		50		ns	
27	t_{RL1AX}	Row Address Hold	2		2		2		ns	
28	t_{RL1CH1}	$\overline{CAS}$ Hold (Early Write)	40		45		50		ns	
29	t_{RL1CH1}	$\overline{CAS}$ Hold ($\overline{CAS}$-Before-$\overline{RAS}$)	2		2		2		ns	
30	t_{RL1CL2}	$\overline{CAS}$ Hold (Non Refresh)	2		2		2		ns	

AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2801-120		2801-150		UNITS	NOTES
			MIN	MAX	MIN	MAX		
1	t_{AVCL2}	Column Address Set-Up (Early Write)	0		0		ns	h
2	t_{AVQV}	Column Address Access		60		75	ns	
3	t_{AVRL2}	Row Address Set-Up	2		2		ns	
4	t_{AVWL2}	Address Valid To $\overline{W}$ Active	60		75		ns	h
5	t_{CH1QZ}	Output Hold	2		2		ns	f
6	t_{CH2CL2}	$\overline{CAS}$ Precharge	5		5		ns	
7	t_{CH2QV}	Access from $\overline{CAS}$ High		60		75	ns	f
8	t_{CH2QZ}	Output Turn-Off Delay		15		20	ns	
9	t_{CH2RL2}	$\overline{CAS}$ Set-Up (Non-$\overline{CAS}$ Before $\overline{RAS}$ Refresh)	2		2		ns	
10	t_{CH2WX}	Read Command Hold (Reference $\overline{CAS}$)	0		0		ns	g
11	t_{CL1AX}	Column Address Hold	11		15		ns	h
12	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Read)	19		25		ns	
13	t_{CL1CH1}	$\overline{CAS}$ Pulse Width (Write)	5		10		ns	
14	t_{CL1DX}	Data-In Hold (Early Write)	11		15		ns	
15	t_{CL1QV}	$\overline{CAS}$ Access		19		25	ns	
16	t_{CL1RH1}	$\overline{CAS}$ To $\overline{RAS}$ Lead	30		40		ns	
17	t_{CL1RL2}	$\overline{CAS}$ Set-Up ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	2		2		ns	
18	t_{CL1WH1}	Write Hold (Reference $\overline{CAS}$)	5		10		ns	
19	t_{CL1WL2}	$\overline{CAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	19		25		ns	i
20	t_{CL2CL2}	Page Read/Write Cycle	50		65		ns	
21	t_{CL2QX}	Output Turn-On Delay	0		0		ns	
22	t_{DVCL2}	Data Set-Up (Early Write)	0		0		ns	h
23	t_{DVWL2}	Data Set-Up (Late Write)	0		0		ns	
24	t_{RH2RL2}	$\overline{RAS}$ Precharge	75		90		ns	
25	t_{RH2WX}	Read Command Hold Time (Reference $\overline{RAS}$)	0		0		ns	g
26	$t_{RL1A(C)X}$	Column Address Hold (Reference $\overline{RAS}$)	55		75		ns	
27	t_{RL1AX}	Row Address Hold	2		2		ns	
28	t_{RL1CH1}	$\overline{CAS}$ Hold (Early Write)	55		70		ns	
29	t_{RL1CH1}	$\overline{CAS}$ Hold ($\overline{CAS}$-Before-$\overline{RAS}$)	2		2		ns	
30	t_{RL1CL2}	$\overline{CAS}$ Hold (Non Refresh)	2		2		ns	

AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2801-60		2801-80		2801-100		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
31	t_{RL1DX}	Data-In Hold (Reference $\overline{RAS}$)	8		10		12		ns	
32	t_{RL1QV}	$\overline{RAS}$ Access		60		80		100	ns	
33	t_{RL1RH1}	$\overline{RAS}$ Pulse Width	60	10^5	80	10^5	100	10^5	ns	
34	t_{RL1WH1}	Write Command Hold (Reference $\overline{RAS}$)	40		45		50		ns	
35	t_{RL1WL2}	$\overline{RAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	60		80		100		ns	i
36	t_{RL2RL2}	Random Read/Write Cycle	111		146		176		ns	
37	t_{WH2CL2}	Read Command Set-Up	0		0		0		ns	
38	t_{WH2WL2}	Write Precharge	5		5		5		ns	
39	t_{WL1CH1}	Write To $\overline{CAS}$ Delay	5		5		5		ns	
40	t_{WL1CL2}	Early Write $\overline{W}$ Set-Up	0		0		0		ns	i
41	t_{WL1DX}	Data-In Hold (Late Write)	5		7		8		ns	h
42	t_{WL1RH1}	Write Command Lead ($\overline{RAS}$)	15		15		15		ns	
43	t_{WL1WH1}	Write Pulse	5		5		5		ns	
44	t_{WL2CL2}	Write To $\overline{CAS}$ Cycle	35		40		45		ns	
45	t_{REF}	Refresh Period		4.4		4.4		4.4	ms	
46	t_T	Transition Time	2	50	2	50	2	50	ns	j, k

NOTES:

f: Q_Z is defined as the time at which the output achieves the open circuit condition.

g. Either t_{CH2WX} or t_{RH2WX} must be satisfied for a Read cycle.

h. Address and data set-up and hold times referenced to $\overline{CAS}$ (t_{AVCL2}, t_{CL1AX}, t_{DVCL2}, and t_{CL1DX}) are restrictive parameters for Early-Write operations only. Address and data set-up times referenced to $\overline{W}$ (t_{AVWL2}, t_{WL1AX}, t_{DVWL2}, and t_{WL1DX}) are restrictive parameters for Late-Write and Read-Modify-Write cycle operations only.

i. t_{WH2CL2}, t_{CL1WL2}, and t_{RL1WL2} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only. If $t_{WL1CL2} \geq t_{WL1CL2}$ (min) the cycle is an Early-Write cycle and data will remain open circuit unless $\overline{CAS}$ makes a subsequent high-to-low transition while $\overline{W}$ is high and $\overline{RAS}$ is low. If $t_{WH2CL2} \geq t_{WH2CL2}$ (min), $t_{RL1WL2} \geq t_{RL1WL2}$ (min), and $t_{AVQV} \geq t_{AVQV}$ (min) the cycle is a Read-Write and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data out is indeterminate at access time.

j. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Transition time is measured between V_{IL} (max) and V_{IH} (min).

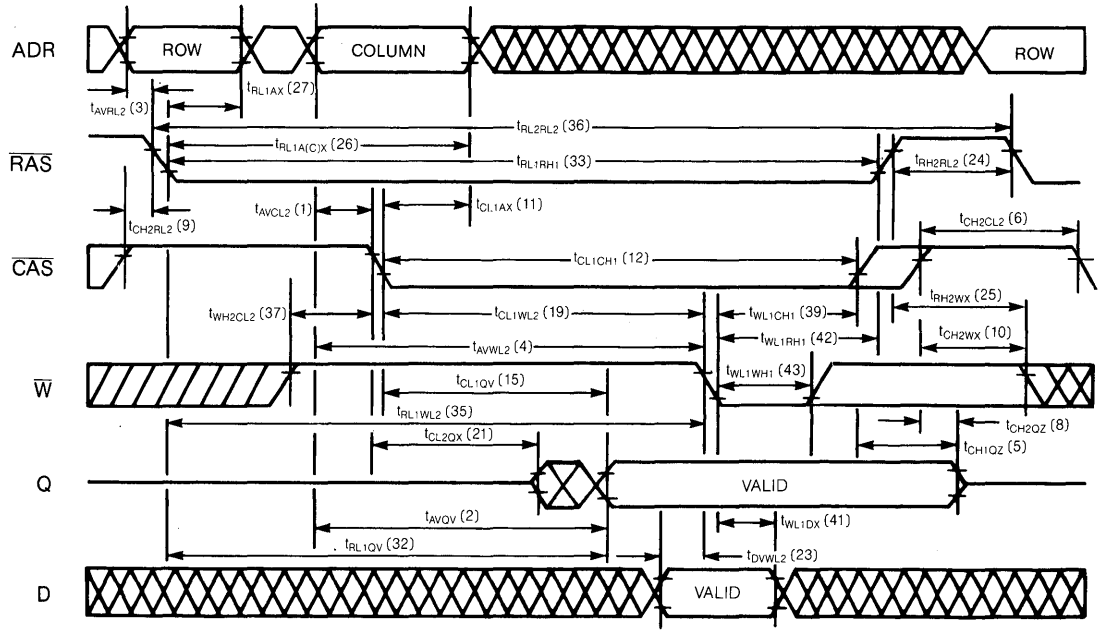
k. 3ns rise and fall times (t_T) are used for cycle time specifications.

l. t_{AVWL2} is a restrictive parameter for Late-Write or Read-Modify-Write cycles when Read Access prior to Write is required.

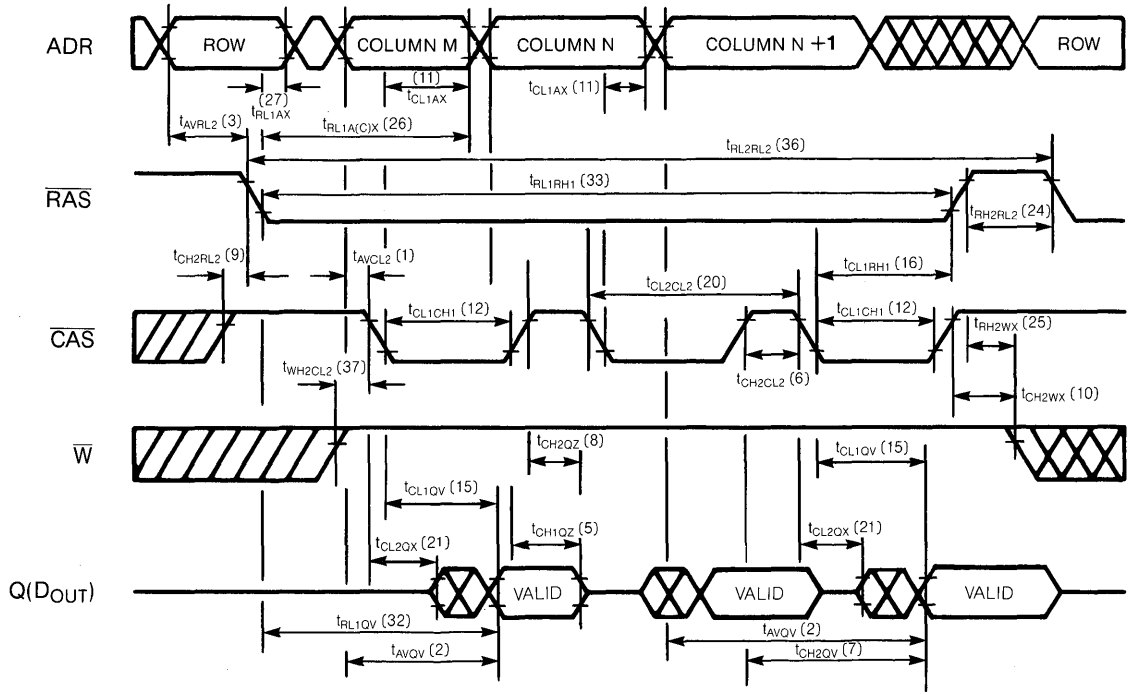
AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2801-120		2801-150		UNITS	NOTES
			MIN	MAX	MIN	MAX		
31	t_{RL1DX}	Data-In Hold (Reference $\overline{RAS}$)	15		25		ns	
32	t_{RL1QV}	$\overline{RAS}$ Access		120		150	ns	
33	t_{RL1RH1}	$\overline{RAS}$ Pulse Width	120	10^5	150	10^5	ns	
34	t_{RL1WH1}	Write Command Hold (Reference $\overline{RAS}$)	55		70		ns	
35	t_{RL1WL2}	$\overline{RAS}$ to $\overline{W}$ Delay (Read/Modify/Write)	120		150		ns	i
36	t_{RL2RL2}	Random Read/Write Cycle	201		246		ns	
37	t_{WH2CL2}	Read Command Set-Up	0		0		ns	
38	t_{WH2WL2}	Write Precharge	5		10		ns	
39	t_{WL1CH1}	Write To $\overline{CAS}$ Delay	5		10		ns	
40	t_{WL1CL2}	Early Write $\overline{W}$ Set-Up	0		0		ns	i
41	t_{WL1DX}	Data-In Hold (Late Write)	10		15		ns	h
42	t_{WL1QVN}	Write/Read Cycle		110		140	ns	
43	t_{WL1RH1}	Write Command Lead ($\overline{RAS}$)	15		20		ns	
44	t_{WL2CL2}	Write To $\overline{CAS}$ Cycle	50		65		ns	
45	t_{WL1WH1}	Write Pulse	5		10		ns	
46	t_{REF}	Refresh Period		4.4		4.4	ms	
47	t_T	Transition Time	2	50	2	50	ns	j, k

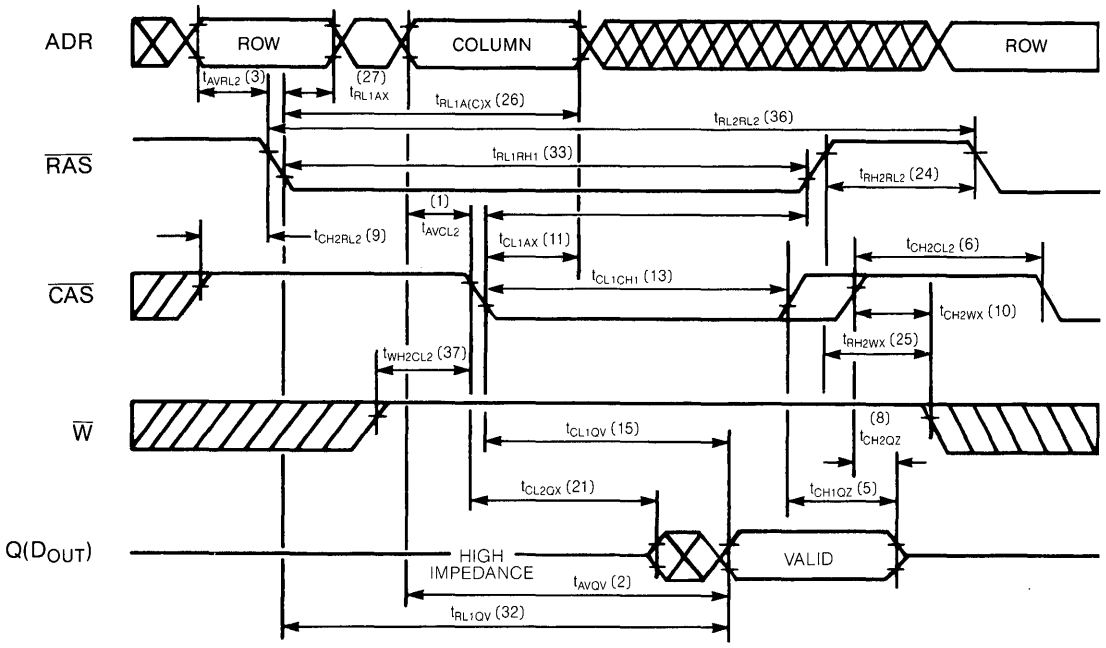
LATE-WRITE/READ-MODIFY-WRITE CYCLE



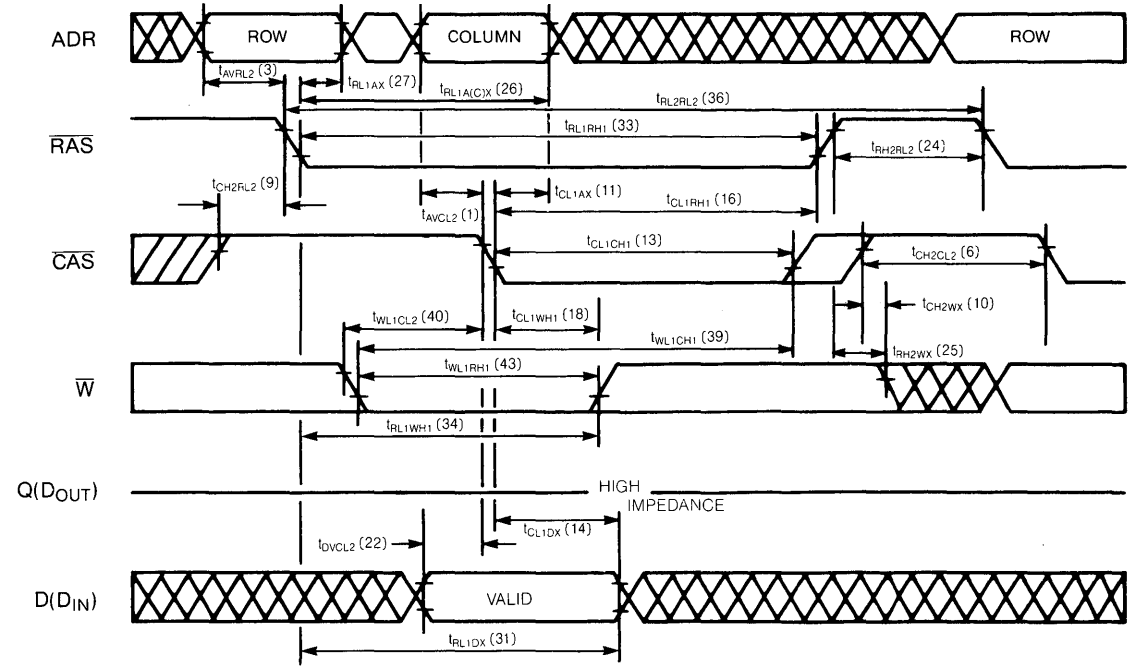
PAGE MODE READ CYCLE



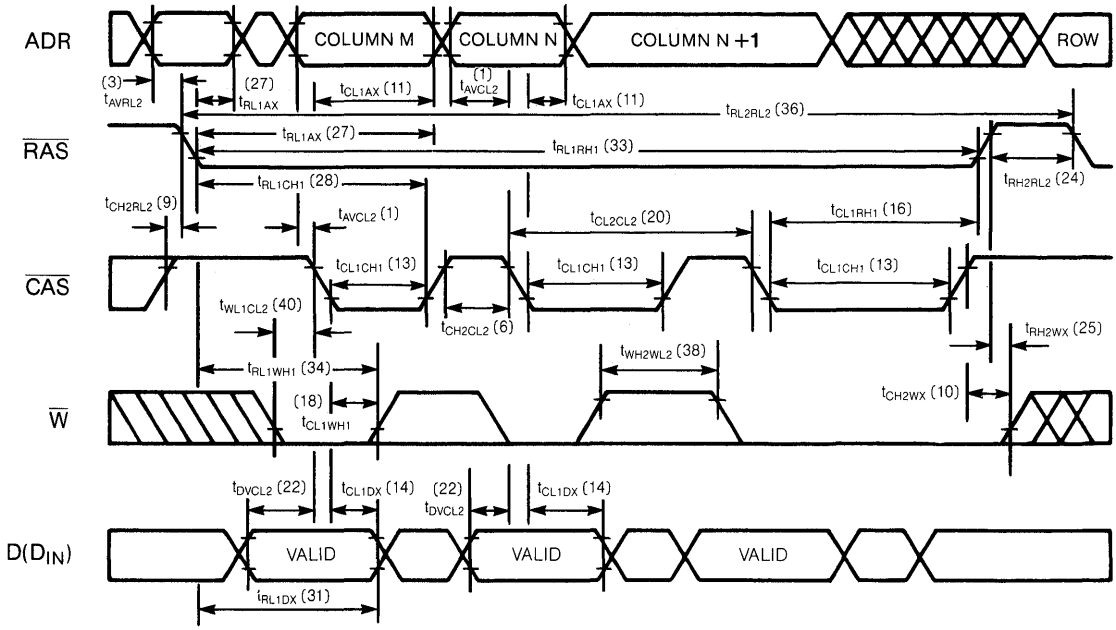
READ CYCLE



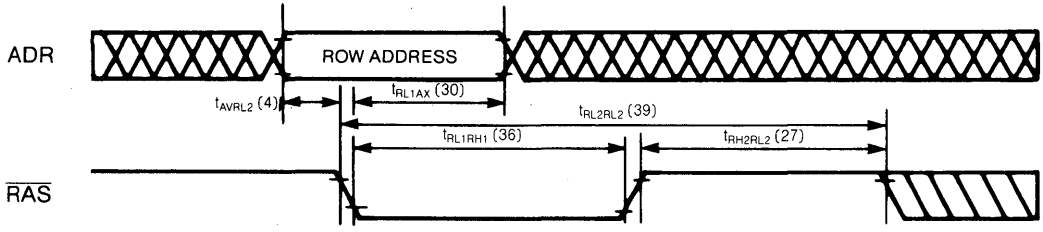
EARLY-WRITE CYCLE



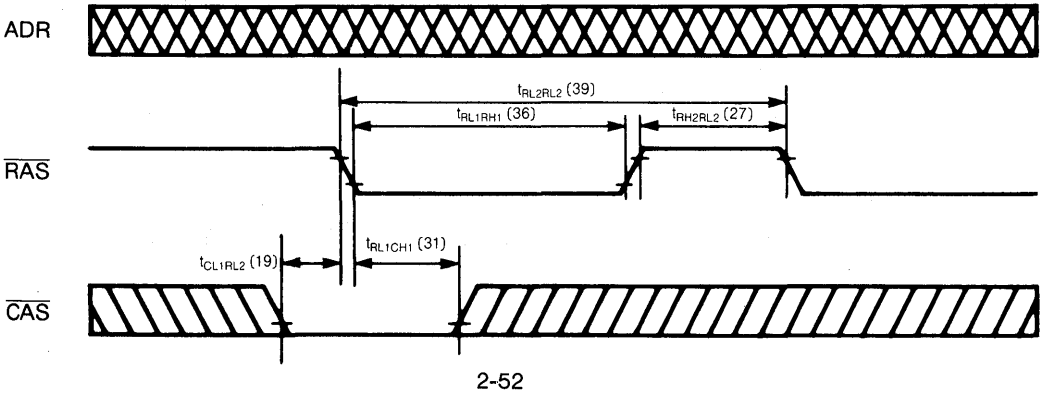
PAGE MODE EARLY WRITE CYCLE



RAS ONLY REFRESH [CAS ≥ VIH (MIN)]



CAS-BEFORE-RAS REFRESH



REFRESH

The IMS2801 remembers data by storing charge on a capacitor. Because the charge will leak away over a period of time it is necessary to access the data in the cell (capacitor) periodically in order to fully restore the stored charge while it is still at a sufficiently high level to be properly detected. For the IMS2801 any $\overline{RAS}$ sequence will fully refresh an entire row of 1024 bits. To ensure that all cells remain sufficiently refreshed, all 256 rows must be refreshed during every 4.4 mS interval.

The addressing of the rows for refresh may be sourced either externally or internally. If the refresh address is provided from an external source, $\overline{CAS}$ must be high when $\overline{RAS}$ goes low and the row address set-up and hold times must be satisfied. If $\overline{CAS}$ is high when $\overline{RAS}$ goes low, any type of cycle (Read, Write, Read-Modify-Write, or $\overline{RAS}$-Only) will cause the externally addressed row to be refreshed.

If $\overline{CAS}$ is low when $\overline{RAS}$ falls, the IMS2801 will use an internal 8-bit encounter as the source of the row addresses and will ignore the $\overline{W}$ (Write Enable) and the external address inputs. $\overline{CAS}$-Before-$\overline{RAS}$ refresh does not cause the device to be selected and the state of the data-out will remain unchanged as long as $\overline{CAS}$ remains low.

APPLICATION

To ensure proper operation of the IMS2801 in a system environment it is recommended that the following guidelines be followed.

POWER DISTRIBUTION

Transient currents are required by dynamics RAMs. These transient current spikes can cause significant power supply and ground noise unless adequate power distribution and decoupling is used. The recommended power distribution scheme combines proper trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (8) through the decoupling capacitor, to the ground pin (16) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line and the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. To prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry. A high-frequency decoupling capacitor with a value of 0.1μF, should be placed between the rows of memory devices in the array. A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low-going TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver/termination combination close to the memory array. Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are among the most important, yet basic guidelines to be followed. These guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS2801	60ns	PLASTIC DIP	IMS2801P-60
	60ns	CERAMIC DIP	IMS2801S-60
	60ns	CERAMIC CHIP CARRIER	IMS2801W-60
	60ns	PLASTIC CHIP CARRIER	IMS2801J-60
	80ns	PLASTIC DIP	IMS2801P-80
	80ns	CERAMIC DIP	IMS2801S-80
	80ns	CERAMIC CHIP CARRIER	IMS2801W-80
	80ns	PLASTIC CHIP CARRIER	IMS2801J-80
	100ns	PLASTIC DIP	IMS2801P-100
	100ns	CERAMIC DIP	IMS2801S-100
	100ns	CERAMIC CHIP CARRIER	IMS2801W-100
	100ns	PLASTIC CHIP CARRIER	IMS2801J-100
	120ns	PLASTIC DIP	IMS2801P-120
	120ns	CERAMIC DIP	IMS2801S-120
	120ns	CERAMIC CHIP CARRIER	IMS2801W-120
	120ns	PLASTIC CHIP CARRIER	IMS2801J-120
	150ns	PLASTIC DIP	IMS2801P-150
	150ns	CERAMIC DIP	IMS2801S-150
	150ns	CERAMIC CHIP CARRIER	IMS2801W-150
	150ns	PLASTIC CHIP CARRIER	IMS2801J-150

Military 3

Military Selection Guide

Device Static RAMs	Organization	Access Times (NS)	Maximum Current (mW)		Power Supply Volts	Number of Pins	Package Type	Process	Page No.
			Active	Standby					
IMS1400S-M IMS1400W-M	16K x 1 16K x 1	45,55,70 45,55,70	660 660	165 165	+5 +5	20 20	S W	NMOS NMOS	3-3 3-3
IMS1420S-M IMS1420W-M	4K x 4 4K x 4	55,70 55,70	660 660	165 165	+5 +5	20 20	S W	NMOS NMOS	3-11 3-11
IMS1423S-M IMS1423W-M	4K x 4 4K x 4	45,55 45,55	660 660	33 CMOS 33 CMOS	+5 +5	20 20	S W	CMOS CMOS	3-19 3-19
IMS1600S-M IMS1600W-M	64K x 1 64K x 1	55,70 55,70	440 440	77 CMOS 77 CMOS	+5 +5	22 22	S W	CMOS CMOS	3-27 3-27
IMS1620S-M	16K x 4	55,70	440	77 CMOS	+5	22	S	CMOS	3-35
Dynamic RAMs									
IMS2600S-M	64K x 1	120,150	468	28	+5	16	S	NMOS	3-43

NOTES:
S = Ceramic DIP
W = Ceramic Chip Carrier

Military Standard Program

The INMOS military standard program was developed to provide MIL-STD-883 processing of memory products. This includes screening to Class B of Method 5004 and quality conformance to Method 5005.

MIL-STD-883, Method 5004, Class B, defines the procedures for total lot screening over the full military temperature range. At INMOS, this range has been defined as: −55°C to +125°C.

MIL-STD-883, Method 5005, Class B, defines the quality conformance inspections and tests required to insure that each lot consistently meets specified quality and reliability levels. Method 5005 consists of Group A (electrical tests), Group B (package integrity tests), Group C (die-related tests), and Group D (package integrity tests) lot inspection procedures.

By specifying an INMOS military product, the user is assured of not only superior performance but also a component capable of meeting stringent military requirements.

IMS1400M

High Performance 16K Static RAM (MIL-STD-883C)

FEATURES

- Specifications guaranteed over full military temperature range (−55°C to +125°C)
- MIL-STD-883C Processing
- 55 and 70nsec Chip Enable Access Times
- Maximum Active Power 660mW
- Maximum Standby Power 165mW
- Single +5V ± 10% Supply
- $\overline{E}$ Power Down Function
- TTL Compatible Inputs and Output
- Fully Static—No Clocks for Timing
- Three-State Output

DESCRIPTION

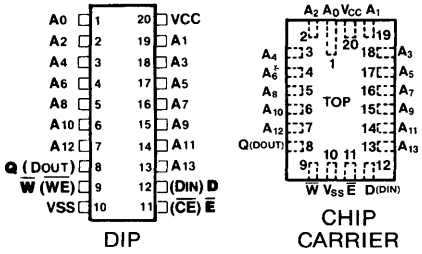
The INMOS Extended Temperature IMS1400M is a high performance 16K x 1 bit static RAM processed in full compliance to MIL-STD-883C, with access times of 55 and 70nsec and maximum power consumption of 660mW. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary N-MOS technology.

The IMS1400M features fully static operation requiring no external clocks or timing strobes, equal access and cycle times, full TTL compatibility and operation from a single +5V ± 10% power supply. Additionally, a Chip Enable function is provided that can be used to place the IMS1400M into a low power standby mode, reducing power consumption to less than 165mW.

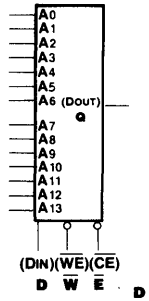
The IMS1400M is packaged in a 20-pin, 300 mil DIP and is also available in a 20-pin chip carrier, making possible high system packing densities.

The IMS1400M is a high speed VLSI RAM intended for Military Temperature applications that demand superior performance and reliability.

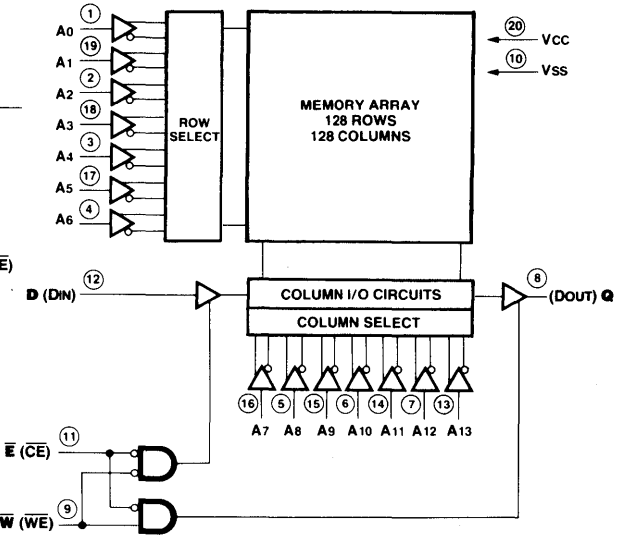
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0 - A13 ADDRESS INPUTS	VCC POWER (+5V)
W (WE) WRITE ENABLE	VSS GROUND
E (CE) CHIP ENABLE	
D (DIN) DATA INPUT	
Q (DOUT) DATA OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias . . . . . −65°C to 135°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		6.0	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−2.0		0.8	V	All Inputs
T_A	Ambient Operating Temperature	−55		125	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC		120	mA	$t_C = t_C$ min
I_{CC2}	V_{CC} Power Supply Current (Standby)		30	mA	$\overline{E} \geq V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)	−10	10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 16mA$		0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

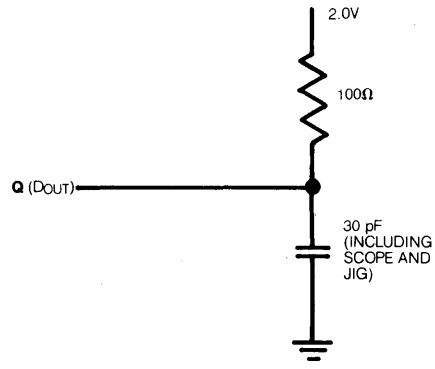
Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

FIGURE 1. OUTPUT LOAD



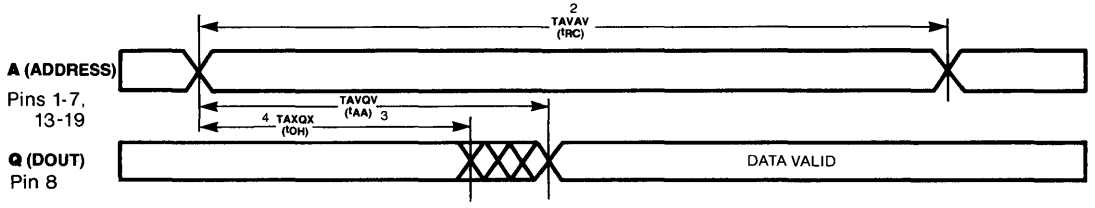
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

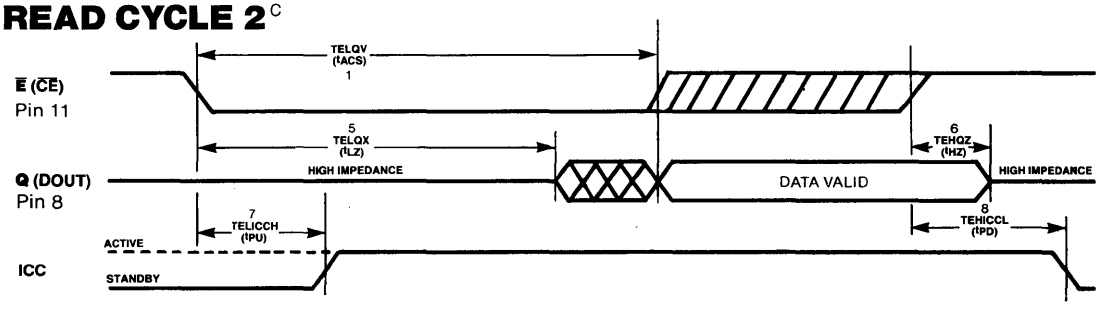
NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	40		50		65		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		40		50		65	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		0		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
6	t_{EHQX}	t_{HZ}	Chip Disable to Output Disable	0	25	0	30	0	40	ns	f
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	
8	t_{EHICCL}	t_{PD}	Chip Disable to Power Down	0	45	0	55	0	70	ns	
		t_T	Input Rise and Fall Times		50		50		50	ns	e

Note c: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage.

READ CYCLE 1 [c, d]



READ CYCLE 2 [c]



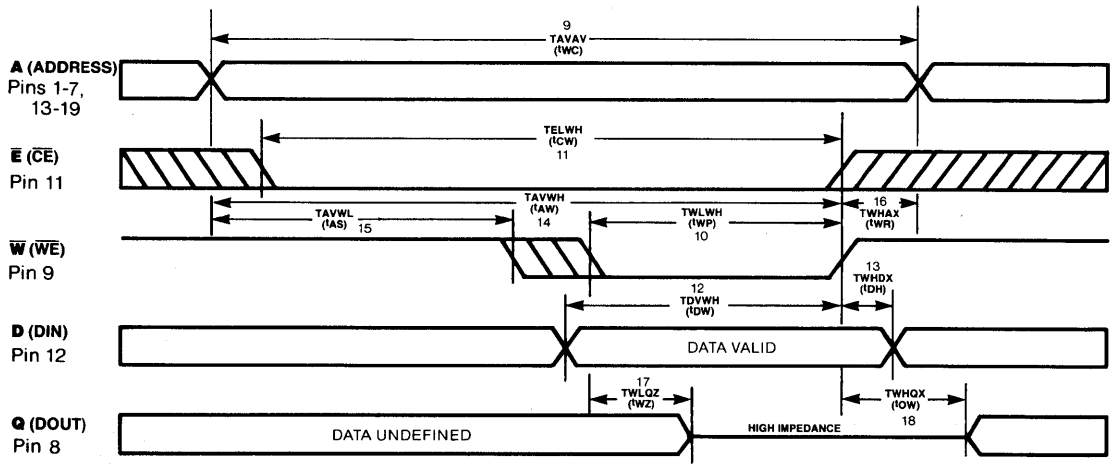
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	40		50		65		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		25		30		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		23		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		8		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	40		50		55		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	8		8		8		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		10		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	28	ns	f
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0	25	0	30	0	40	ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{E}$ goes high with $\overline{W}$ low, Output remains in HIGH impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transition.

WRITE CYCLE 1



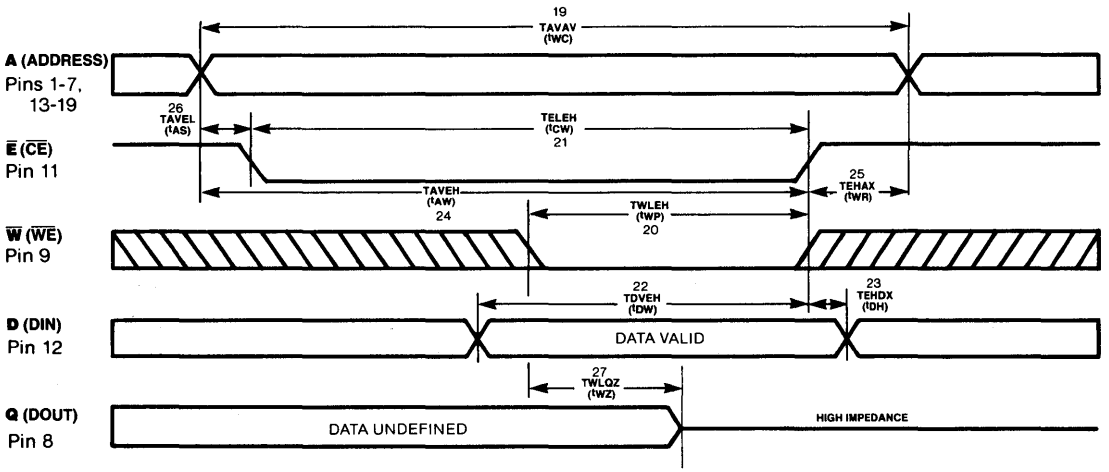
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC}$ = 5.0V ± 10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	40		50		65		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		20		23		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	5		5		10		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	40		50		55		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		10		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	−5		−5		−5		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	28	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transition.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1400M has two control inputs: Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), 14 address inputs, a data in (D_{IN}) and a data out (D_{OUT}).

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the 14 address inputs are decoded to select one memory cell out of 16,385. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than ¼ of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout a READ CYCLE 1 and is valid at the specified address access time. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the input (D_{IN}) is written into the selected cell, and the output (D_{OUT}) is in high impedance.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, D_{OUT} becomes active.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, D_{OUT} remains in the high impedance state.

APPLICATION

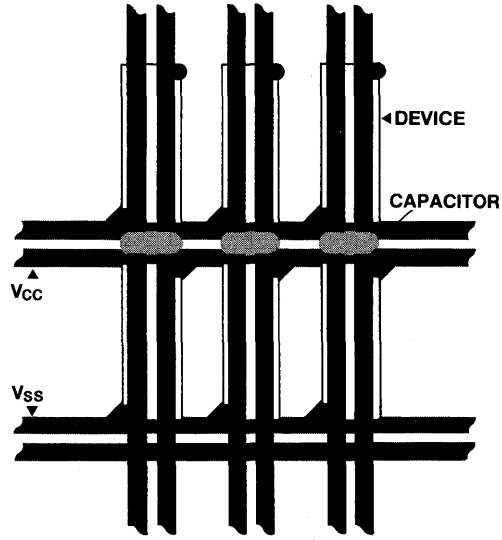
To ensure proper operation of the extended temperature IMS1400M in a system environment, it is recommended that the following guidelines on board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor, to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see Figure 2). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

Also, to prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

The use of proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are some of the most important, yet basic rules to be followed.

The rules are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

INMOS MILITARY STANDARD PROGRAM*

The INMOS military program is designed to provide full compliance to MIL-STD-883C. This includes screening per Method 5004, quality conformance testing per method 5005, and the applicable provisions of MIL-M-38510. The IMS1400M is processed for general applications where component quality and reliability must conform to the guidelines and objectives of military procurement. Suitability for use in specific applications should be determined using the guidelines of MIL-STD-454.

Component screening, as depicted in Table 1, defines the sequence used for production of INMOS military products. This sequence assures compliance with methods 5004, 5005, and their applicable sub-methods. All electrical testing is performed at military temperatures of −55°C, +25°C, and +125°C with applicable quality conformance testing per the requirements of MIL-M-38510. Additionally, INMOS includes as standard screening, the requirements of method 5004 paragraph 3.3 on all military grade products.

All INMOS military grade components are hermetically sealed in metal to ceramic packages and contain an organic RTV silicon alpha particle overcoat. Dual in line packages are per MIL-M-38510 appendix C case outline D8 configuration 3. The 20 pin rectangular leadless chip carrier has not been designated in MIL-M-38510 and is supplied to the INMOS case outline defined herein.

By specifying the IMS1400M the user can be assured of receiving a product manufactured, tested and inspected in full compliance with MIL-STD-883C and one with superior performance for those applications where quality and reliability are of the essence.

TABLE I

100 PERCENT PROCESS STEP	MIL-STD-883C METHOD	TEST CONDITION	COMMENT
INTERNAL VISUAL	2010	B	
STABILIZATION BAKE	1008	C	
TEMPERATURE CYCLE	1010	C	
CONSTANT ACCELERATION	2001	E	Y-1 AXIS
SEAL TEST	1014	B	
SEAL TEST	1014	C	
VISUAL INSPECTION			INMOS 80-1001
PRE BURN IN ELECTRICAL			+25°C DATA SHEET
BURN IN	1015	D	
POST BURN ELECTRICAL			+25°C DATA SHEET
PDA			5% MAX
FINAL ELECTRICAL			+125°C DATA SHEET
GROUP A	5005	3.5.1	A2, A5, A8, A10
FINAL ELECTRICAL			−55°C DATA SHEET
GROUP A	5005	3.5.1	A3, A6, A8, A11
EXTERNAL VISUAL	2009		
GROUP A	5005	3.5.1	A1, A4, A7, A9
GROUP B	5005	3.5.2	
GROUP C	5005		MIL-STD-883C 1.2.1.b.17
GROUP D	5005		

*See Inmos Document 41-9047 "Military General Processing Specification" for full details.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1400M	45ns	DIP	IMS1400S-45M
	45ns	CHIP CARRIER	IMS1400W-45M
	55ns	DIP	IMS1400S-55M
	55ns	CHIP CARRIER	IMS1400W-55M
	70ns	DIP	IMS1400S-70M
	70ns	CHIP CARRIER	IMS1400W-70M

IMS1420M

High Performance 4Kx4 Static RAM (MIL-STD-883C)

FEATURES

- Specifications guaranteed over full military temperature range (−55°C to +125°C)
- MIL-STD-883C Processing
- 4K x 4 Bit Organization
- 55 and 70ns Address Access
- 660mW Maximum Power Dissipation
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Single +5V ± 10% Operation
- 55 and 70nsec Chip Enable Access
- Power Down Function
- 165mW Maximum Standby Power

DESCRIPTION

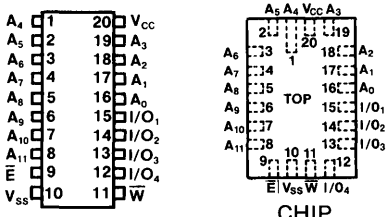
The INMOS Extended Temperature IMS1420M is a high performance 4K x 4 bit static RAM processed in full compliance to MIL-STD-883C. This includes screening over the full −55°C to +125°C temperature range, as defined in Method 5004 Class B and qualification to Method 5005 Class B. The device features access times of 55 and 70nsec and maximum power consumption of 660mW. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary N-MOS technology.

The IMS1420M features fully static operation requiring no external clocks or timing strobes, equal access and cycle times, full TTL compatibility and operation from a single +5V ± 10% power supply. Additionally, a Chip Enable function is provided that can be used to place the IMS1420M into a low power standby mode, reducing power consumption to less than 165mW.

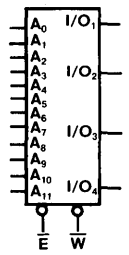
The IMS1420M is packaged in a 20-pin, 300-mil DIP, and is also available in a 20-pin chip carrier, making possible high system packing densities.

The IMS1420M is a high speed VLSI RAM intended for Military Temperature applications that demand superior performance and reliability.

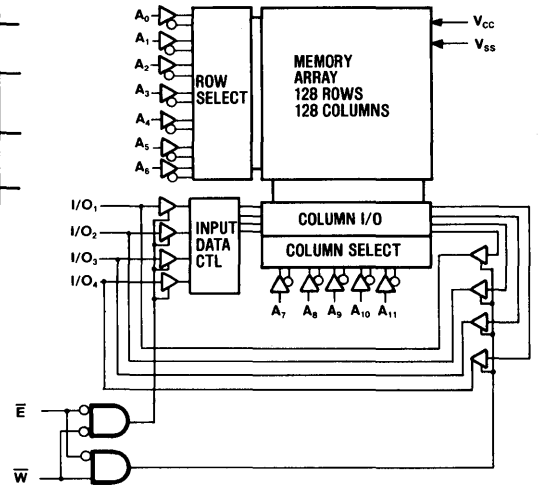
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$	CHIP ENABLE		
I/O	DATA IN/OUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias . . . . . −65°C to 135°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.4		6.0	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−2.0		0.8	V	All Inputs
T_A	Ambient Operating Temperature	−55		125	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC		120	mA	$t_C = t_C$ min
I_{CC2}	V_{CC} Power Supply Current (Standby)		30	mA	$\overline{E} \geq V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)	−10	10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 8mA$		0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

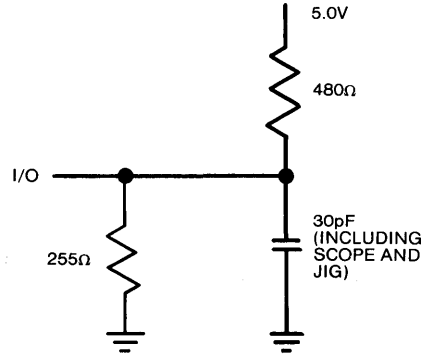
Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

FIGURE 1. OUTPUT LOAD



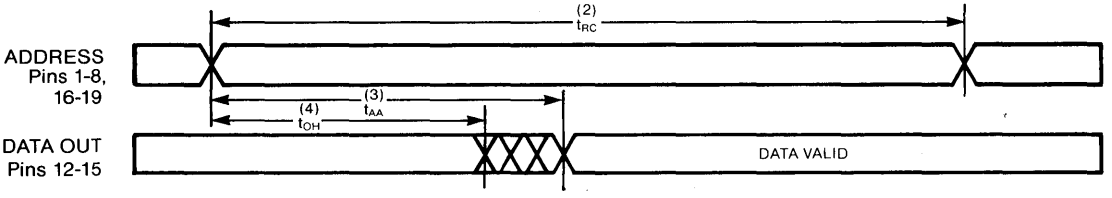
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

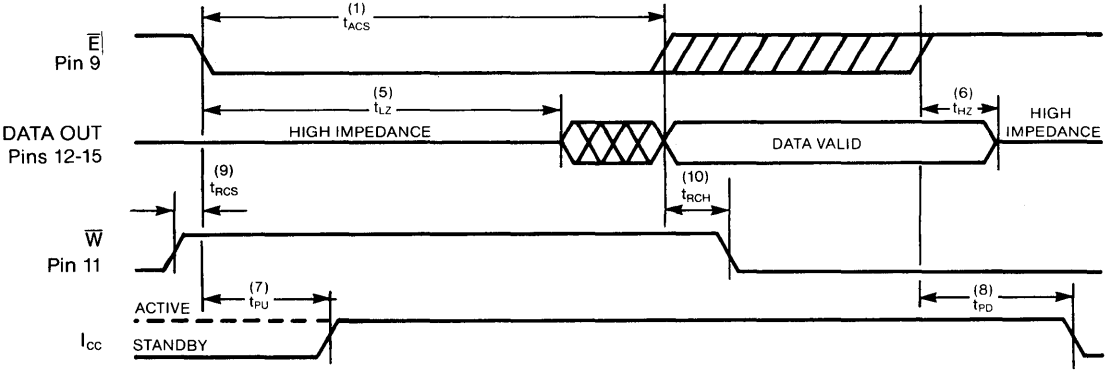
NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
1	t_{ACS}	Chip Enable Access Time		55		70	ns	
2	t_{RC}	Read Cycle Time	55		70		ns	c
3	t_{AA}	Address Access Time		55		70	ns	d
4	t_{OH}	Output Hold After Address Change	3		3		ns	
5	t_{LZ}	Chip Enable to Output Active	15		15		ns	
6	t_{HZ}	Chip Disable to Output Disable		25		30	ns	f
7	t_{PU}	Chip Enable to Power Up	0		0		ns	
8	t_{PD}	Chip Disable to Power Down	0	55	0	70	ns	
9	t_{RCS}	Read Command Set-up Time	−5		−5		ns	
10	t_{RCH}	Read Command Hold Time	−5		−5		ns	
	t_T	Input Rise and Fall Times		50		50	ns	e

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage.

READ CYCLE 1 [c, d]



READ CYCLE 2 [c]



Military

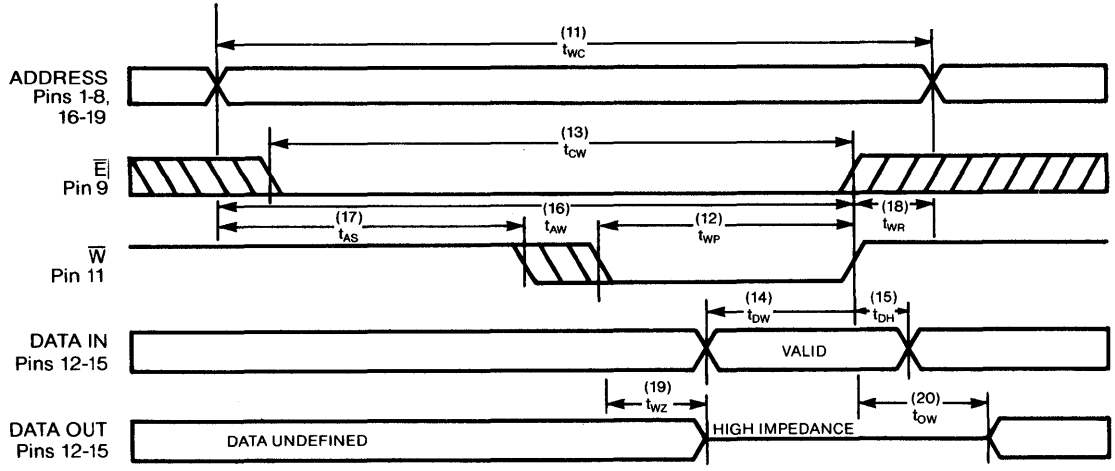
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
11	t_{WC}	Write Cycle Time	55		70		ns	
12	t_{WP}	Write Pulse Width	45		65		ns	
13	t_{CW}	Chip Enable to End of Write	45		65		ns	
14	t_{DW}	Data Set-up to End of Write	25		30		ns	
15	t_{DH}	Data Hold After End of Write	3		5		ns	
16	t_{AW}	Address Set-up to End of Write	45		65		ns	
17	t_{AS}	Address Set-up to Beginning of Write	0		0		ns	
18	t_{WR}	Address Hold After End of Write	5		5		ns	
19	t_{WZ}	Write Enable to Output Disable	0	25	0	30	ns	f
20	t_{OW}	Output Active After End of Write	0		0		ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{E}$ goes high with $\overline{W}$ low, Output remains in HIGH impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 1



RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

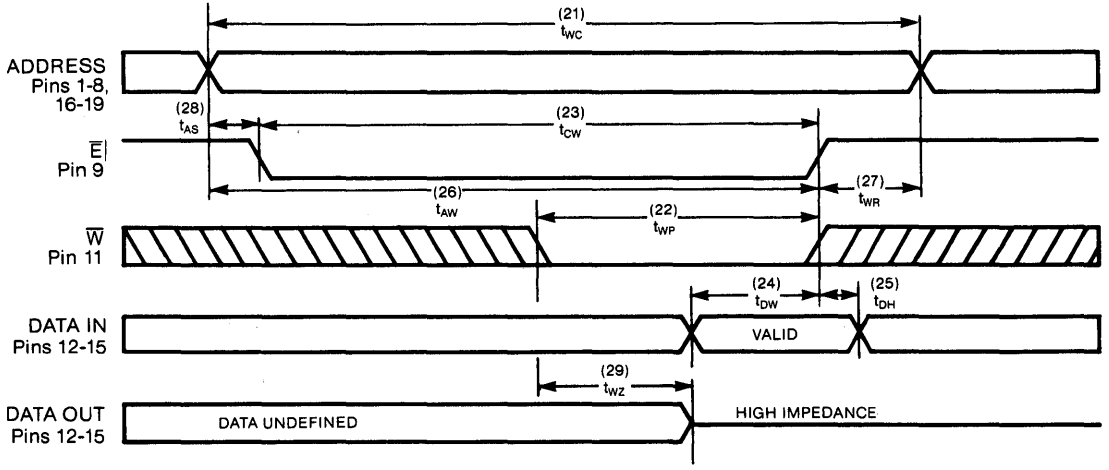
WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
21	t_{WC}	Write Cycle Time	55		70		ns	
22	t_{WP}	Write Pulse Width	45		65		ns	
23	t_{CW}	Chip Enable to End of Write	45		65		ns	
24	t_{DW}	Data Set-up to End of Write	25		30		ns	
25	t_{DH}	Data Hold After End of Write	5		5		ns	
26	t_{AW}	Address Set-up to End of Write	40		60		ns	
27	t_{WR}	Address Hold After End of Write	5		5		ns	
28	t_{AS}	Address Set-up to Beginning of Write	−5		−5		ns	
29	t_{WZ}	Write Enable to Output Disable	0	25	0	30	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

Military

WRITE CYCLE 2



DEVICE OPERATION

The IMS1420M has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs, and four Data I/O lines.

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one 4-bit word out of 4096. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-third of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of 3ns. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the inputs is written into the selected cells, and the outputs are floating.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address need not be stable until a maximum of 5ns after $\overline{E}$ goes low. The address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, the outputs become active. When $\overline{W}$ goes high at the end of a write cycle and the outputs of the memory go active, the data from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

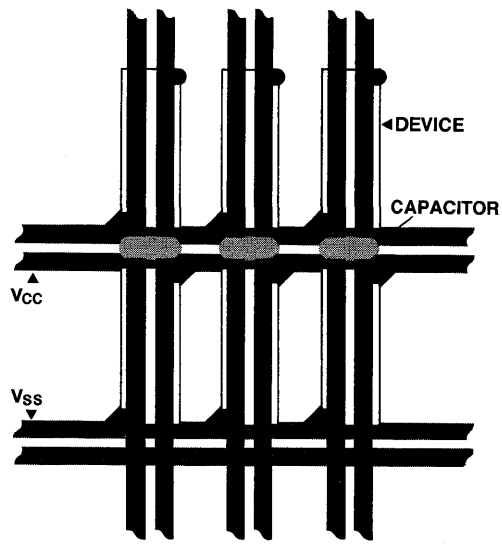
Fundamental rules in regard to memory board layout should be followed to ensure maximum benefit from the features offered by the IMS1420M Static RAM.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1420M. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor, to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1420M are high frequency, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor acts as a low impedance power supply located near the memory device. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs, are some of the most important, yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes and signal reflections.

INMOS MILITARY STANDARD PROGRAM*

The INMOS military program is designed to provide full compliance to MIL-STD-883C. This includes screening per Method 5004, quality conformance testing per method 5005, and the applicable provisions of MIL-M-38510. The IMS1420M is processed for general applications where component quality and reliability must conform to the guidelines and objectives of military procurement. Suitability for use in specific applications should be determined using the guidelines of MIL-STD-454.

Component screening, as depicted in Table 1, defines the sequence used for production of INMOS military products. This sequence assures compliance with methods 5004, 5005, and their applicable sub-methods. All electrical testing is performed at military temperatures of −55°C, +25°C, and +125°C with applicable quality conformance testing per the requirements of MIL-M-38510. Additionally, INMOS includes as standard screening, the requirements of method 5004 paragraph 3.3 on all military grade products.

All INMOS military grade components are hermetically sealed in metal to ceramic packages and contain an organic RTV silicon alpha particle overcoat. Dual in line packages are per MIL-M-38510 appendix C case outline D8 configuration 3. The 20 pin rectangular leadless chip carrier has not been designated in MIL-M-38510 and is supplied to the INMOS case outline defined herein.

By specifying the IMS1420M the user can be assured of receiving a product manufactured, tested and inspected in full compliance with MIL-STD-883C and one with superior performance for those applications where quality and reliability are of the essence.

TABLE I

100 PERCENT PROCESS STEP	MIL-STD-883C METHOD	TEST CONDITION	COMMENT
INTERNAL VISUAL	2010	B	
STABILIZATION BAKE	1008	C	
TEMPERATURE CYCLE	1010	C	
CONSTANT ACCELERATION	2001	E	Y-1 AXIS
SEAL TEST	1014	B	
SEAL TEST	1014	C	
VISUAL INSPECTION			INMOS 80-1001
PRE BURN IN ELECTRICAL			+25°C DATA SHEET
BURN IN	1015	D	
POST BURN ELECTRICAL			+25°C DATA SHEET
PDA			5% MAX
FINAL ELECTRICAL			+125°C DATA SHEET
GROUP A	5005	3.5.1	A2, A5, A8, A10
FINAL ELECTRICAL			−55°C DATA SHEET
GROUP A	5005	3.5.1	A3, A6, A8, A11
EXTERNAL VISUAL	2009		
GROUP A	5005	3.5.1	A1, A4, A7, A9
GROUP B	5005	3.5.2	
GROUP C	5005		MIL-STD-883C 1.2.1.b.17
GROUP D	5005		

*See Inmos Document 41-9047 "Military General Processing Specification" for full details.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1420M	55ns	DIP	IMS1420S-55M
	55ns	CHIP CARRIER	IMS1420W-55M
	70ns	DIP	IMS1400S-70M
	70ns	CHIP CARRIER	IMS1400W-70M

IMS1423M
CMOS High Performance 4K x 4 Static RAM (MIL-STD-883C)

FEATURES

- Specifications guaranteed over full military temperature range (−55°C to +125°C)
- MIL-STD-883C Processing
- INMOS Very High Speed CMOS
- Advanced Process—2 Micron Design Rules
- 4K x 4 Bit Organization
- 35, 45 and 55nsec Address Access Times
- 35, 45 and 55nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- Power Down Function
- 20 Pin, 300-mil DIP (JEDEC Standard)

DESCRIPTION

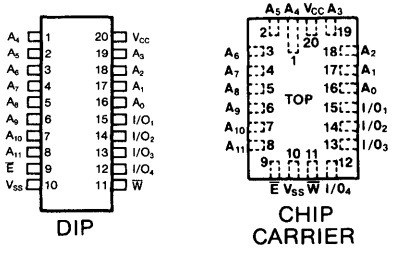
The IMS1423M is a high performance 4K x 4 static RAM guaranteed to operate over the full temperature range. This includes screening over the full −55°C to +125°C temperature range, as defined in Method 5004 Class B and qualification to Method 5005 Class B. The devices feature access times of 35, 45 and 55 nanoseconds.

The IMS1423M features fully static operation requiring no external clocks or strobes, equal access and cycle times, full TTL compatibility and operation from a single 5 volt supply. Additionally, a Chip Enable function is provided to place the IMS1423M into a low power stand-by mode.

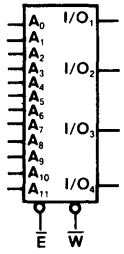
The IMS1423M is packaged in a 20 pin, 300 mil DIP and is also available in a 20 pin chip carrier, making possible high system packing densities.

The IMS1423M is a VLSI RAM intended for Military temperature applications that demand superior performance and reliability.

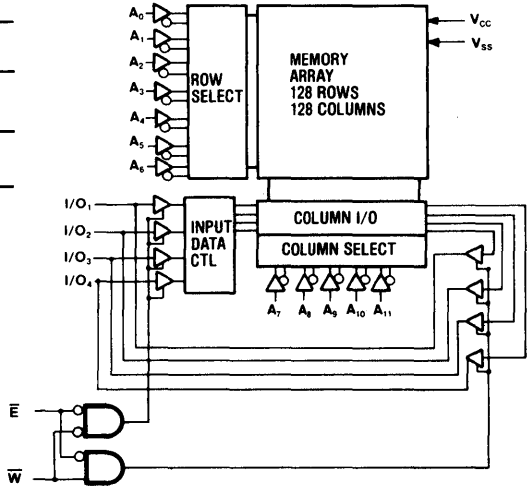
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$	CHIP ENABLE		
I/O	DATA IN/OUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −2.0 to 7.0V
Voltage on I/O (Pins 13-16) . . . . . −1.0 to (V_{CC} + .5V)
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current . . . . . 25mA (One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC} + .5	V	
V_{IL}	Input Logic "0" Voltage	−1.0		0.8	V	
T_A	Ambient Operating Temperature	−55		125	°C	400 Linear ft./min. transverse air flow

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current AC		120 110	mA mA	t_{AVAV} = 45ns, a t_{AVAV} = 55ns, a
I_{CC_2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		18	mA	$\overline{E} \geq 2.0V$ All Other Inputs 2.0V $\leq V_{IN} \leq 0.8V$
I_{CC_3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		6	mA	$\overline{E} \geq (V_{CC} - 0.3V)$ All Other Inputs $V_{CC} - .3V \leq V_{IN} \leq 0.3V$
I_{CC_4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels) $\overline{E} \geq (V_{CC} - .3V)$		14 13	mA mA	t_{AVAV} = 45ns t_{AVAV} = 55ns All Other Inputs Cycling from 0.3V to V_{CC} −.3V
I_{IN}	Input Leakage Current (Any Input)		±10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = −4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS[b]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

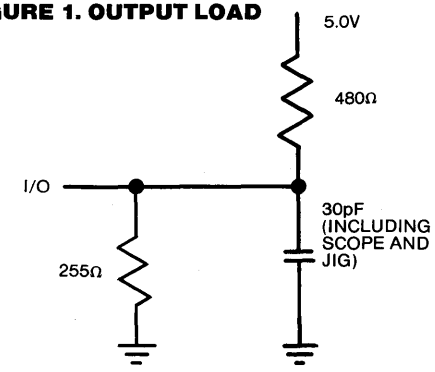
Note b: Operation to specifications guaranteed 500μS after $V_{CC} \geq 4.5$.

CAPACITANCE[c] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note c: This parameter is sampled and not 100% tested.

FIGURE 1. OUTPUT LOAD



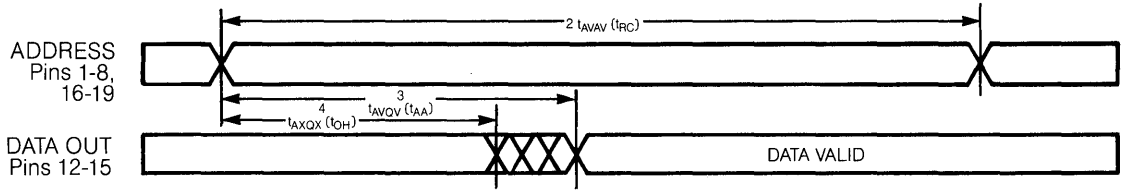
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[j]

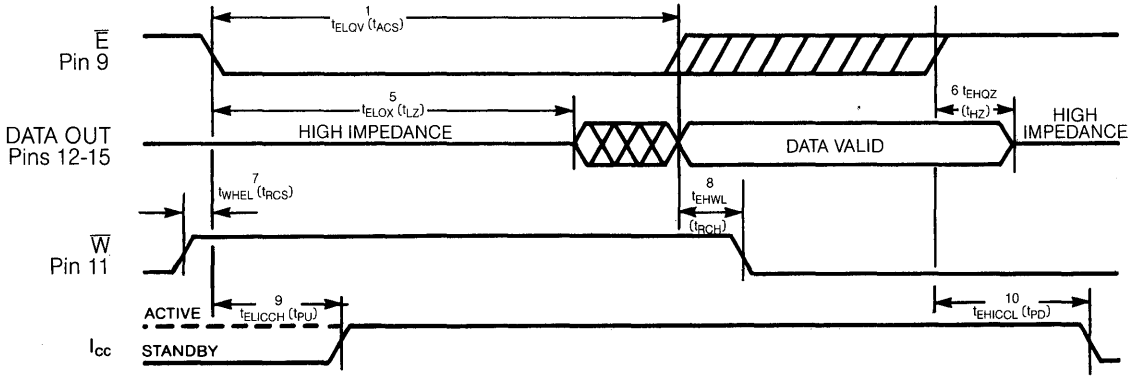
NO.	SYMBOL		PARAMETER	1423M-45		1423M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	45		55		ns	d
3	t_{AVQV}	t_{AA}	Address Access Time		45		55	ns	e
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	20	ns	g
7	t_{WHEL}	t_{RCS}	Read Command Set-Up Time	0		0		ns	
8	t_{EHWL}	t_{RCH}	Read Command Hold Time	0		0		ns	
9	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		ns	
10	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		45		55	ns	
		t_T	Input Rise and Fall Times	3	50	3	50	ns	f

Note d: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note e: Device is continuously selected, $\overline{E}$ low.
Note f: Measured between V_{IL} max and V_{IH} min.
Note g: Measured ± 200mV from steady state output voltage.
Note j: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



Military

RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[i, j]

NO.	SYMBOL		PARAMETER	1423M-45		1423M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
11	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		ns	
12	t_{WLWH}	t_{WP}	Write Pulse Width	45		50		ns	
13	t_{ELWH}	t_{CW}	Chip Enable to End of Write	40		50		ns	
14	t_{DVWH}	t_{DW}	Data Set-up to End of Write	20		25		ns	
15	t_{WHDX}	t_{DH}	Data Hold After End of Write	3		3		ns	
16	t_{AVWH}	t_{AW}	Address Set-up to End of Write	40		30		ns	
17	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		ns	
18	t_{WHAX}	t_{WR}	Address Hold After End of Write	5		5		ns	
19	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	ns	g
20	t_{WHQX}	t_{OW}	Output Active After End of Write	5		5		ns	h

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[i, j]

NO.	SYMBOL		PARAMETER	1423M-45		1423M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
21	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		ns	
22	t_{WLEH}	t_{WP}	Write Pulse Width	40		50		ns	
23	t_{ELEH}	t_{CW}	Chip Enable to End of Write	40		50		ns	
24	t_{DVEH}	t_{DW}	Data Set-up to End of Write	20		25		ns	
25	t_{EHDX}	t_{DH}	Data Hold After End of Write	2		2		ns	
26	t_{AVEH}	t_{AW}	Address Set-up to End of Write	40		25		ns	
27	t_{EHAX}	t_{WR}	Address Hold After End of Write	5		5		ns	
28	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	3		3		ns	
29	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	ns	g,h

Note g: Measured ± 200mV from steady state output voltage.
Note h: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note i: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note j: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.

DEVICE OPERATION

The IMS1423M has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs (A_0-A_{11}), and four Data I/O lines.

The IMS1423M becomes active immediately after V_{CC} is applied, but proper operation is not assured until 500 microseconds after V_{CC} reaches 4.5 volts.

With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one 4-bit word out of 4096. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-fourth of the active mode power with TTL input levels and even lower with CMOS levels.

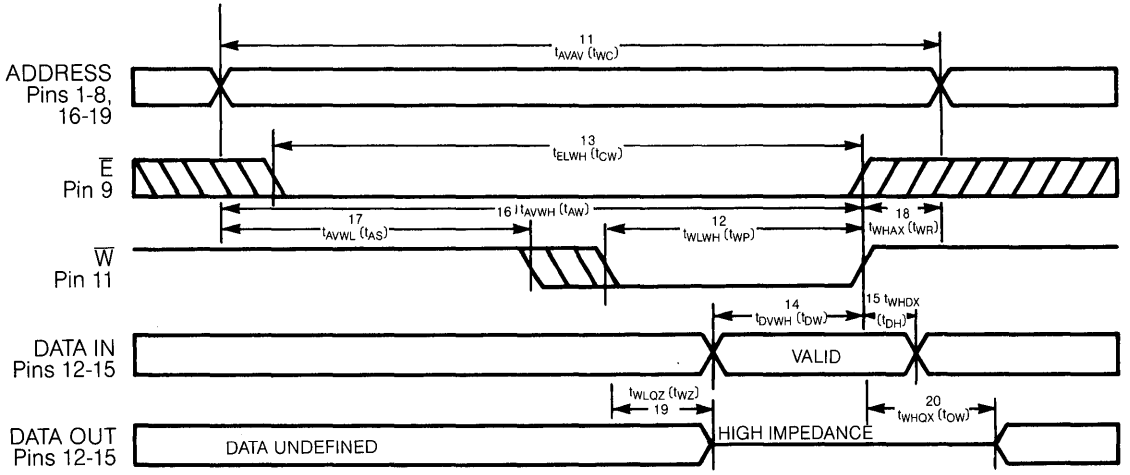
READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from the latter of either $\overline{E}$ going low or from valid address.

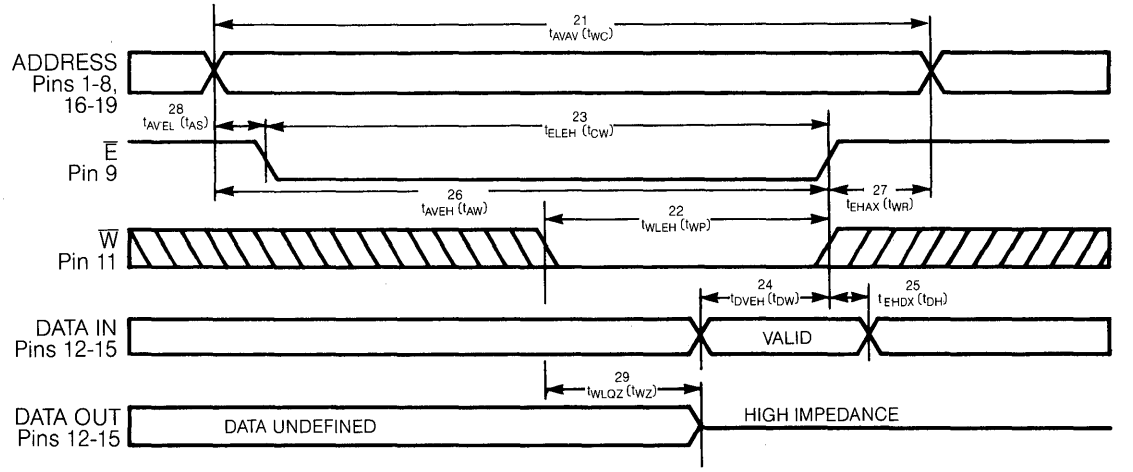
The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of t_{AXQV}. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE 1



WRITE CYCLE 2



WRITE CYCLE

The write cycle of the IMS1423M is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high level to a low level. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common input/output connections. Therefore input data should not be active until after t_{WLQZ} to avoid bus contention. During a write cycle, data on the inputs is written into the selected cells and the outputs are floating.

If a write cycle is initiated by $\overline{E}$ going low, the address must be stable for t_{AVEL} referenced to $\overline{E}$. If the write cycle is initiated by $\overline{W}$ going low, then the address must be valid for t_{AVWL} referenced to $\overline{W}$. The address must be held stable for the entire write cycle. After either $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If the set-up and hold times are not met, for either address or data, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high while $\overline{E}$ is low, the outputs become active. When $\overline{W}$ goes high at the end of a write cycle and the outputs of the memory go active, the data from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1423M, that the fundamental rules of good engineering practice be followed in areas such as board layout and signal fidelity to ensure proper system operation.

TTL VS. CMOS INPUT LEVELS

The IMS1423M is fully compatible with TTL input levels. The input circuitry of the IMS1423M is designed for maximum speed and also for conversion of TTL level signals to the CMOS levels required for internal operation. The IMS1423M consumes less power when CMOS levels (.3/V_{CC} −.3 volts) are used than TTL levels (.8/2.0 volts) are applied. The lower CMOS I_{CC} specifications, I_{CC3} and I_{CC4}, may be achieved by using CMOS levels. The power consumption will be lower at typical TTL levels than at the worst case levels.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the wide operating margins of the IMS1423M. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1423M have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as near the memory as possible, with the shortest lead lengths practical. The high frequency decoupling capacitor should have a minimum value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor, for low frequency current transients, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

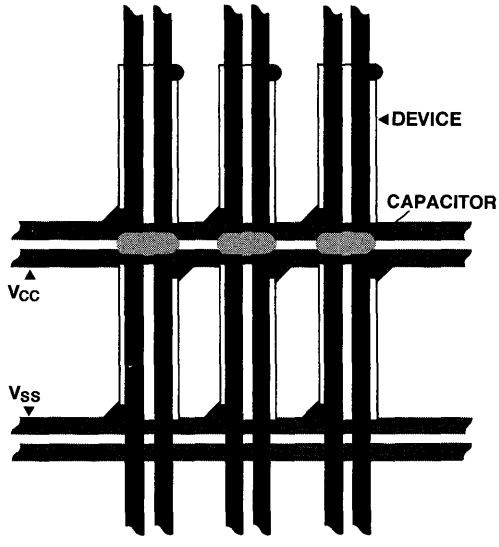
TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The termination resistor should be placed as close to the driver package as possible. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33ohm range will be required. Because the characteristic impedance of each layout will be different, it is necessary to select the proper value of this resistor by trial and error. A resistor of predetermined value may not properly terminate the transmission line.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilizing a wideband oscilloscope and probe. When using WRITE CYCLE 1, care should be taken to avoid bus contention. When $\overline{W}$ goes high, with $\overline{E}$ low, the output buffers will be active t_{WHQX} after the rising edge of $\overline{W}$. Data out will be the same as the data just written, unless the address changes. If data-in from the previous cycle is still valid after the address changes, contention may result. Contention may also result if $\overline{E}$ goes low before $\overline{W}$, with Data-in valid early in the cycle. INMOS Application Note #5, "Bus Contention Considerations," provides a detailed analysis of contention and methods used to control bus contention.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

ASYNCHRONOUS VS. SYNCHRONOUS OPERATION

Fast, high density Static RAMs have a finite probability of encountering transient (non-catastrophic) errors[1] particularly when operated in a totally asynchronous manner. Therefore, in applications where extremely low error rates are essential, it is recommended that synchronous operation be considered. Synchronous operation is accomplished by allowing address changes during device deselect intervals ($\overline{E}$ high) only.

[1]Chappell, Schuster, Sai-Halasz, "Stability and Soft Error Rates of SRAM Cells," ISSCC Digest of Technical Papers, p. 162-163; Feburary 1984.

INMOS MILITARY STANDARD PROGRAM*

The INMOS military program is designed to provide compliance to MIL-STD-883C. This includes screening per Method 5004, quality conformance testing per method 5005, and the applicable provisions of MIL-M-38510. The IMS1423M is processed for general applications where component quality and reliability must conform to the guidelines and objectives of military procurement. Suitability for use in specific applications should be determined using the guidelines of MIL-STD-454.

Component screening, as depicted in Table 1, defines the sequence used for production of INMOS military products. This sequence assures compliance with methods 5004, 5005, and their applicable sub-methods. All electrical testing is performed to guarantee operation at −55°C, +25°C, and +125°C T_A, with applicable quality conformance testing per the requirements of MIL-M-38510. Additionally, INMOS includes as standard screening, the requirements of method 5004 paragraph 3.3 on all military grade products.

All INMOS military grade components are hermetically sealed in metal to ceramic packages and contain an organic RTV silicon alpha particle overcoat. Dual in line packages are per MIL-M-38510 appendix C case outline D8 configuration 3. The 20 pin rectangular leadless chip carrier has not been designated in MIL-M-38510 and is supplied to the INMOS case outline defined herein.

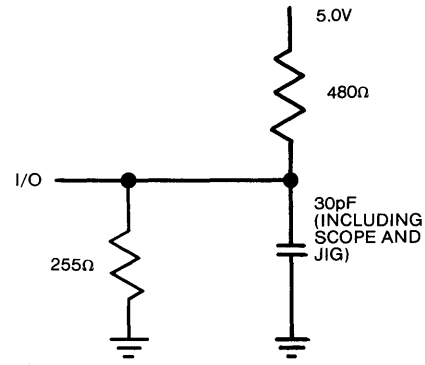
By specifying the IMS1423M the user can be assured of receiving a product manufactured, tested and inspected in compliance with MIL-STD-883C and one with superior performance for those applications where quality and reliability are of the essence.

TABLE I

100 PERCENT PROCESS STEP	MIL-STD-883C METHOD	TEST CONDITION	COMMENT
INTERNAL VISUAL	2010	B	
STABILIZATION BAKE	1008	C	
TEMPERATURE CYCLE	1010	C	
CONSTANT ACCELERATION	2001	E	Y-1 AXIS
SEAL TEST	1014	B	
SEAL TEST	1014	C	
VISUAL INSPECTION			INMOS 80-1001
PRE BURN IN ELECTRICAL			+25°C DATA SHEET
BURN IN	1015	D	
POST BURN ELECTRICAL			+25°C DATA SHEET
PDA			5% MAX
FINAL ELECTRICAL			+125°C DATA SHEET
FINAL ELECTRICAL			−55°C DATA SHEET
EXTERNAL VISUAL	2009		
GROUP A	5005	3.5.1	A1-A11
GROUP B	5005	3.5.2	
GROUP C	5005		MIL-STD-883C 1.2.1.b.17
GROUP D	5005		

*See Inmos Document 41-9047 "Military General Processing Specification" for full details.

FIGURE 1. OUTPUT LOAD



ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1423M	45ns	CERAMIC DIP	IMS1423S-45M
	45ns	CHIP CARRIER	IMS1423W-45M
	55ns	CERAMIC DIP	IMS1423S-55M
	55ns	CHIP CARRIER	IMS1423W-55M

IMS1600M

CMOS High Performance 64K x 1 Static RAM (MIL-STD-883C)

FEATURES

- Specifications guaranteed over full military temperature range (−55°C to +125°C)
- MIL-STD-883C Processing
- INMOS Very High Speed CMOS
- Advanced Process—2 Micron Design Rules
- 64K x 1 Bit Organization
- 55 and 70nsec Address Access Times
- 55 and 70nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- Power Down Function
- 22 Pin, 300-mil DIP (JEDEC Standard)

DESCRIPTION

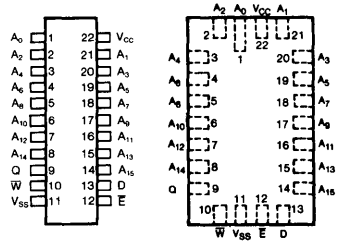
The IMS1600M is a high performance 64K x 1 static RAM guaranteed to operate over the full temperature range. This includes screening over the full −55°C to +125°C temperature range, as defined in Method 5004 Class B and qualification to Method 5005 Class B. The devices feature access times of 55 and 70 nanoseconds.

The IMS1600M features fully static operation requiring no external clocks or strobes, equal access and cycle times, full TTL compatibility and operation from a single 5 volt supply. Additionally, a Chip Enable function is provided to place the IMS1600M into a low power stand-by mode.

The IMS1600M is packaged in a 22 pin, 300 mil DIP and is also available in a 22 pin chip carrier, making possible high system packing densities.

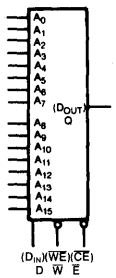
The IMS1600M is a VLSI RAM intended for Military temperature applications that demand superior performance and reliability.

PIN CONFIGURATION

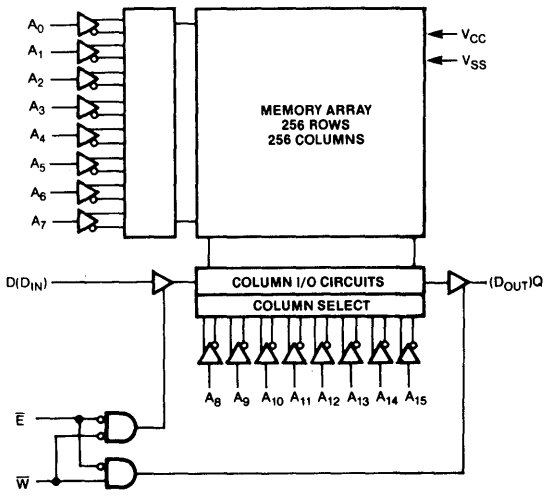


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{15}	ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{W}$	WRITE ENABLE	
$\overline{E}$	CHIP ENABLE	
D	DATA INPUT	
Q	DATA OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −2.0 to 7.0V
Voltage on Q (Pin 9) . . . . . −1.0 to (V_{CC} + 0.5)
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temp. (Ceramic Package) . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current . . . . . 25mA (One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC} + .5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−1.0		0.8	V	All Inputs
T_A	Ambient Operating Temperature	−55		125	°C	400 Linear ft./min. transverse air flow

DC ELECTRICAL CHARACTERISTICS (−55°C ≤ T_A ≤ +125°C) (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current AC		110 100	mA mA	t_{AVAV} = 55ns, a t_{AVAV} = 70ns, a
I_{CC_2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		25	mA	$\overline{E} \geq 2.0V$ All Other Inputs 2.0V ≤ V_{IN} ≤ 0.8V
I_{CC_3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\overline{E} \geq (V_{CC} - 0.3V)$ All Other Inputs V_{CC} −.3V ≤ V_{IN} ≤ 0.3V
I_{CC_4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels) $\overline{E} \geq (V_{CC} - .3V)$		17 15	mA mA	t_{AVAV} = 55ns t_{AVAV} = 70ns All Other Inputs Cycling from 0.3V to V_{CC} −.3V
I_{ILK}	Input Leakage		±10	µA	
I_{OLK}	Output Leakage		±50	µA	
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = −8mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

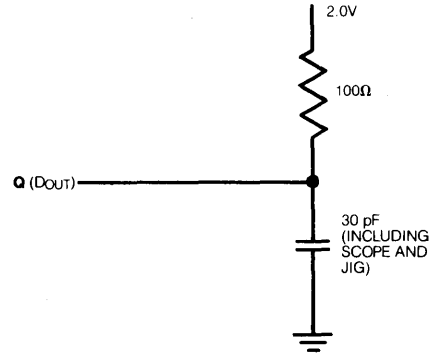
Note a: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with output unloaded.

AC TEST CONDITIONS[b]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

Note b: Operation to specifications guaranteed 500µS after $V_{CC} \geq 4.5$.

FIGURE 1. OUTPUT LOAD



CAPACITANCE[c] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note c: This parameter is sampled and not 100% tested.

RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

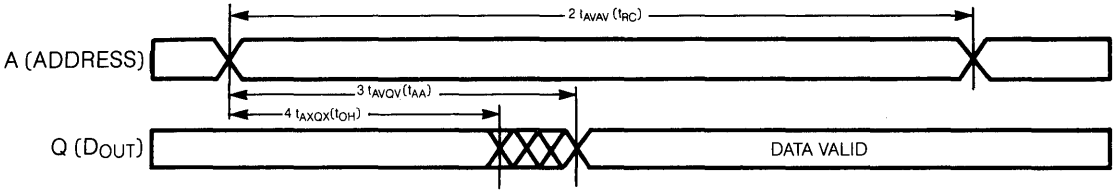
READ CYCLE [h]

NO.	SYMBOL		PARAMETER	IMS1600M-55		1600M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	55		70		ns	d
3	t_{AVQV}	t_{AA}	Address Access Time		55		70	ns	e
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		ns	f
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Disable	0	30	0	30	ns	g
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		ns	c
8	t_{EHICCL}	t_{PD}	Chip Disable To Power Down	0	55	0	50	ns	c
		t_T	Input Rise and Fall Times		50		50	ns	f

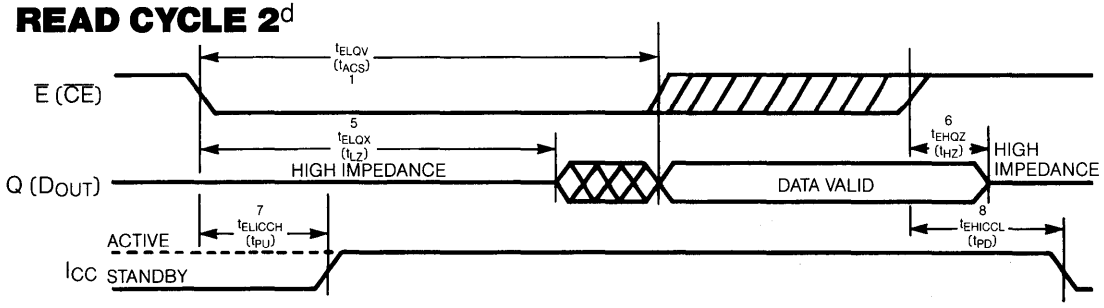
Note d: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note e: Device is continuously selected, $\overline{E}$ low.
Note f: Measured between reference levels of $V_{IL} = 0.8V$ and $V_{IH} = 2.0V$.
Note g: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.

Military

READ CYCLE 1 [d,e]



READ CYCLE 2 [d]



RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h, j]

NO.	SYMBOL		PARAMETER	IMS1600M-55		IMS1600M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	55		70		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	25		30		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	50		65		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	20		30		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	5		5		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	33		38		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	8		8		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	5		5		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	25	0	30	ns	g
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0	30	0	40	ns	i

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1600M-55		1600M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	55		70		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	25		30		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	25		30		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	20		30		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	5		5		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	25		30		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	5		5		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	3		3		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	25	0	30	ns	g

Note g: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note i: If $\overline{E}$ goes low with $\overline{W}$ low, the output remains in high impedance state.
Note j: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transition.

DEVICE OPERATION

The IMS1600M has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), sixteen address inputs (A_0-A_{15}), a data in (D_{IN}) and a data out (D_{OUT}).

The IMS1600M becomes active immediately after V_{CC} is applied, but proper operation is not guaranteed until after 500 microseconds after V_{CC} reaches 4.5 volts. The $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the sixteen address inputs are decoded to select one memory cell out of 65,536. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-third of the active mode power with TTL input levels and even lower with CMOS levels.

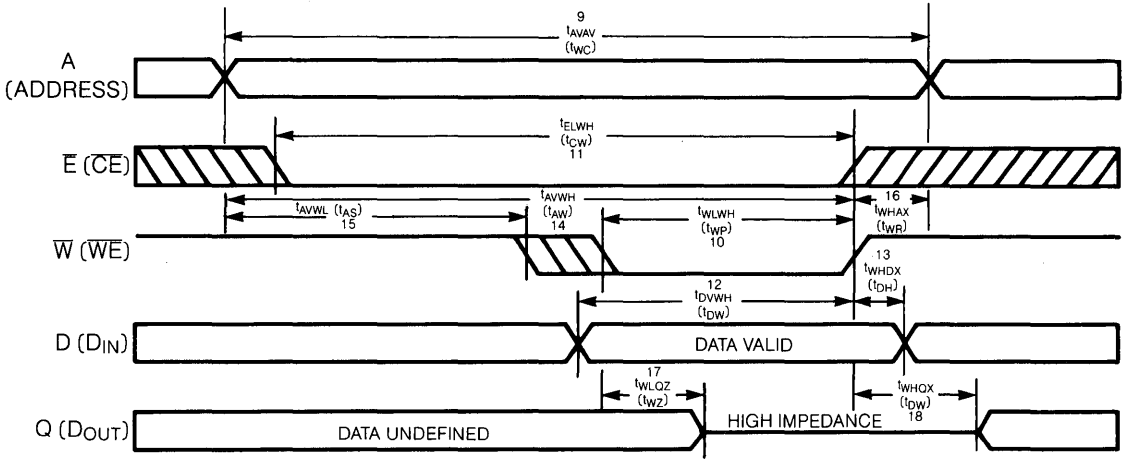
READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from the latter of either $\overline{E}$ going low or from valid address.

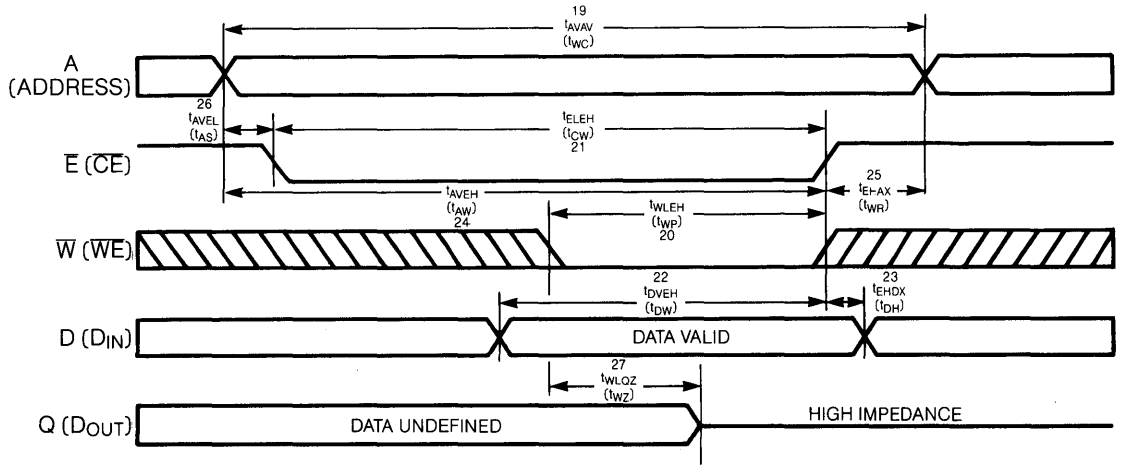
The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of t_{AXQX}. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ

WRITE CYCLE 1



WRITE CYCLE 2



CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1600M is initiated by the latter of $\overline{E}$ or $\overline{W}$ to fall. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Contention can be avoided in a carefully designed system. During a write cycle, data on the inputs is written into the selected cells and the outputs are floating.

If a write cycle is initiated by $\overline{W}$ going low, then the address must be valid for t_{AVWL} referenced to $\overline{W}$. If a write cycle is initiated by $\overline{E}$ going low, the address must be stable for t_{AVEL} referenced to $\overline{E}$. The address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If the set-up and hold times are not met, for either address or data, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of the memory becomes active. The data from the memory will be the same as the input data, unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1600M, that the fundamental rules of good engineering practice be followed in areas such as board layout and signal fidelity to ensure proper system operation.

TTL VS. CMOS INPUT LEVELS

The IMS1600M is fully compatible with TTL input levels. The input circuitry of the IMS1600 is designed for maximum speed and also for conversion of TTL level signals to the CMOS levels required for internal operation. The IMS1600 consumes less power when CMOS levels (.3/ V_{CC} −.3 volts) are used than TTL levels (.8/2.0 volts) are applied. The lower CMOS I_{CC} specifications, I_{CC3} and I_{CC4}, may be achieved by using CMOS levels, i.e., inputs within .3 volts of either supply. The power consumption will be lower at typical TTL levels than at the worst case levels.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1600M. The impedance in the decoupling path from the power pin (22) through the decoupling capacitor to the ground pin (11) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1600M have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients, therefore should be located as near the device and with as short lead lengths as practical. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

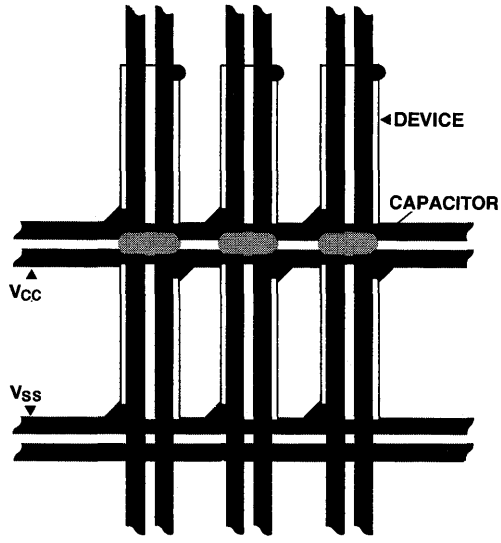
The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing.

ASYNCHRONOUS VS. SYNCHRONOUS OPERATION

Fast, high density memory devices have a finite probability of encountering transient (non-catastrophic) errors[1] particularly when operated in a totally asynchronous manner. Therefore, in applications where extremely low error rates are essential, it is recommended that synchronous operation be considered. Synchronous operation is accomplished by allowing address changes during device deselect intervals ($\overline{E}$ high) only.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

[1]Chappell, Schuster, Sai-Halasz, "Stability and Soft Error Rates of SRAM Cells," ISSCC Digest of Technical Papers, p. 162-163; Feburary 1984.

INMOS MILITARY STANDARD PROGRAM*

The INMOS military program is designed to provide compliance to MIL-STD-883C. This includes screening per Method 5004, quality conformance testing per method 5005, and the applicable provisions of MIL-M-38510. The IMS1600M is processed for general applications where component quality and reliability must conform to the guidelines and objectives of military procurement. Suitability for use in specific applications should be determined using the guidelines of MIL-STD-454.

Component screening, as depicted in Table 1, defines the sequence used for production of INMOS military products. This sequence assures compliance with methods 5004, 5005, and their applicable sub-methods. All electrical testing is performed to guarantee operation at −55°C, +25°C, and +125°C T_A, with applicable quality conformance testing per the requirements of MIL-M-38510. Additionally, INMOS includes as standard screening, the requirements of method 5004 paragraph 3.3 on all military grade products.

All INMOS military grade components are hermetically sealed in metal to ceramic packages and contain an organic RTV silicon alpha particle overcoat. Dual in line packages are per MIL-M-38510 appendix C case outline D7 configuration 3. The 20 pin rectangular leadless chip carrier has not been designated in MIL-M-38510 and is supplied to the INMOS case outline defined herein.

By specifying the IMS1600M the user can be assured of receiving a product manufactured, tested and inspected in compliance with MIL-STD-883C and one with superior performance for those applications where quality and reliability are of the essence.

TABLE I

100 PERCENT PROCESS STEP	MIL-STD-883C METHOD	TEST CONDITION	COMMENT
INTERNAL VISUAL	2010	B	
STABILIZATION BAKE	1008	C	
TEMPERATURE CYCLE	1010	C	
CONSTANT ACCELERATION	2001	E	Y-1 AXIS
SEAL TEST	1014	B	
SEAL TEST	1014	C	
VISUAL INSPECTION			INMOS 80-1001
PRE BURN IN ELECTRICAL			+25°C DATA SHEET
BURN IN	1015	D	
POST BURN ELECTRICAL			+25°C DATA SHEET
PDA			5% MAX
FINAL ELECTRICAL			+125°C DATA SHEET
FINAL ELECTRICAL			−55°C DATA SHEET
EXTERNAL VISUAL	2009		
GROUP A	5005	3.5.1	A1-A11
GROUP B	5005	3.5.2	
GROUP C	5005		MIL-STD-883C 1.2.1.b.17
GROUP D	5005		

*See Inmos Document 41-9047 "Military General Processing Specification" for full details.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1600M	55ns	CERAMIC DIP	IMS1600S-55M
	55ns	CHIP CARRIER	IMS1600W-55M
	70ns	CERAMIC DIP	IMS1600S-70M
	70ns	CHIP CARRIER	IMS1600W-70M

IMS1620M

CMOS High Performance 16Kx4 Static RAM (MIL-STD-883C)

Preliminary

FEATURES

- Specifications guaranteed over full military temperature range (−55°C to +125°C)
- MIL-STD-883C Processing
- INMOS Very High Speed CMOS
- Advanced Process−2 Micron Design Rules
- 16K x 4 Bit Organization
- 55 and 70nsec Address Access Times
- 55 and 70nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Single +5V ± 10% Operation
- Power Down Function
- 22 Pin, 300-mil DIP (JEDEC Standard)

DESCRIPTION

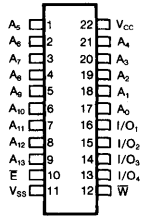
The IMS1620M is a high performance 16K x 4 static RAM guaranteed to operate over the full temperature range. This includes screening over the full −55°C to +125°C temperature range, as defined in Method 5004 Class B and qualification to Method 5005 Class B. The devices feature access times of 55 and 70 nanoseconds.

The IMS1620M features fully static operation requiring no external clocks or strobes, equal access and cycle times, full TTL compatability and operation from a single 5 volt supply. Additionally, a Chip Enable function is provided to place the IMS1620M into a low power standby mode.

The IMS1620M is packaged in a 22 pin, 300 mil dip, and is also available in a 22 pin chip carrier, making possible high system packing densities.

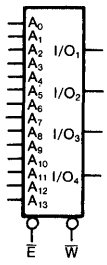
The IMS1620M is a VLSI RAM intended for Military temperature applications that demand superior performance and reliability.

PIN CONFIGURATION

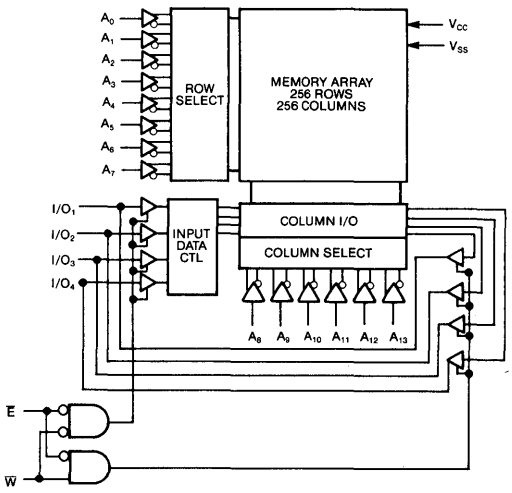


DIP

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{13} ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{W}$ WRITE ENABLE	V_{SS} GROUND
I/O DATA IN/OUT	
$\overline{E}$ CHIP ENABLE	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −2.0 to 7.0V
Voltage on I/O (Pins 13-16) . . . . . −1.0 to (V_{CC} + 1.0V)
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current . . . . . 25mA (One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0.	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC} + .5	V	
V_{IL}	Input Logic "0" Voltage	−1.0		0.8	V	
T_A	Ambient Operating Temperature	−55		125	°C	400 Linear ft./min. transverse air flow

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$) ($V_{CC}$ = 5.0V ± 10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC		TBD TBD	mA mA	t_{AVAV} = 55ns, a t_{AVAV} = 70ns, a
I_{CC2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		TBD	mA	$\overline{E} \geq 2.0V$ All Other Inputs $2.0V \leq V_{IN} \leq 0.8V$
I_{CC3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		TBD	mA	$\overline{E} \geq (V_{CC} - 0.3V)$ All Other Inputs $V_{CC} - .3V \leq V_{IN} \leq 0.3V$
I_{CC4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels) $\overline{E} \geq (V_{CC} - .3V)$		TBD TBD	mA mA	t_{AVAV} = 55ns, a t_{AVAV} = 70ns, a All Other Inputs Cycling from 0.3V to V_{CC} −.3V
I_{IN}	Input Leakage Current (Any Input)	−10	10	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	µA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = −4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS[b]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

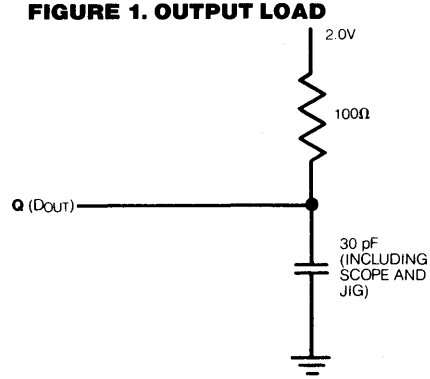
Note b: Operation to specifications guaranteed 500µS after $V_{CC} \geq 4.5$.

CAPACITANCE[c] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note c: This parameter is sampled and not 100% tested.

FIGURE 1. OUTPUT LOAD



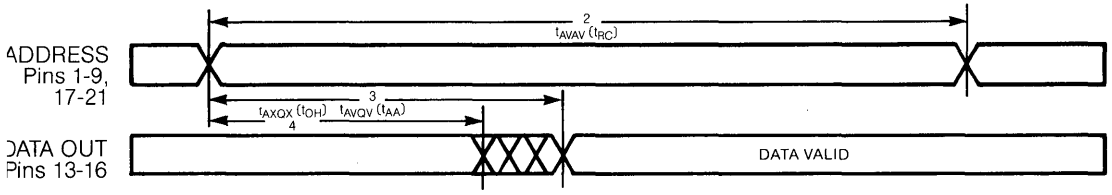
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[h]

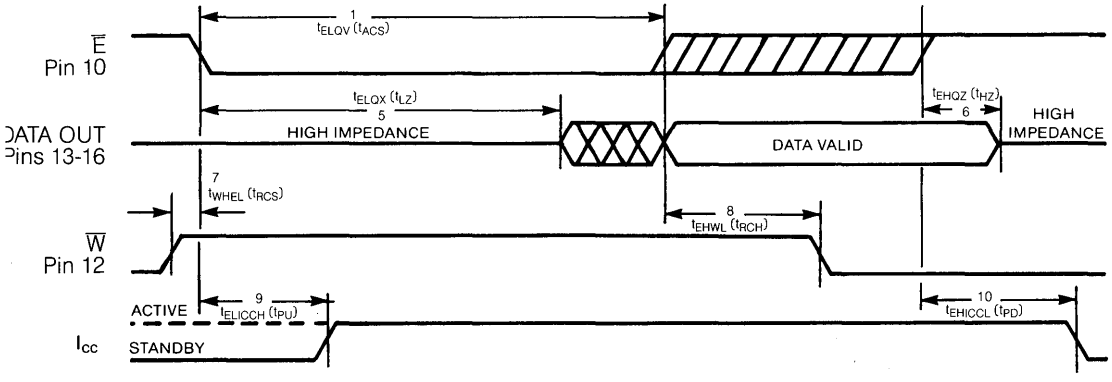
NO.	SYMBOL		PARAMETER	1620M-55		1620M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	55		70		ns	d
3	t_{AVQV}	t_{AA}	Address Access Time		55		70	ns	e
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		ns	f
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	3		3		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	25	0	30	ns	g
7	t_{WHEL}	t_{RCS}	Read Command Set-Up Time	0		0		ns	
8	t_{EHWL}	t_{RCH}	Read Command Hold Time	0		0		ns	
9	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0			
10	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		55		70		
		t_T	Input Rise and Fall Times	3	50	3	50	ns	f

Note d: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note e: Device is continuously selected, $\overline{E}$ low.
Note f: Measured between V_{IL} max and V_{IH} min.
Note g: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.

READ CYCLE 1[d, e]



READ CYCLE 2[d]



Military

RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h, i]

NO.	SYMBOL		PARAMETER	1620M-55		1620M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
11	t_{AVAV}	t_{WC}	Write Cycle Time	55		70		ns	
12	t_{WLWH}	t_{WP}	Write Pulse Width	50		60		ns	
13	t_{ELWH}	t_{CW}	Chip Enable to End of Write	50		60		ns	
14	t_{DVWH}	t_{DW}	Data Set-up to End of Write	25		30		ns	
15	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		ns	
16	t_{AVWH}	t_{AW}	Address Set-up to End of Write	50		60		ns	
17	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		ns	
18	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		ns	
19	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	25	0	25	ns	g
20	t_{WHQX}	t_{OW}	Output Active After End of Write	0		0		ns	j

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h, i]

NO.	SYMBOL		PARAMETER	1620M-55		1620M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX		
21	t_{AVAV}	t_{WC}	Write Cycle Time	55		70		ns	
22	t_{WLEH}	t_{WP}	Write Pulse Width	50		60		ns	
23	t_{ELEH}	t_{CW}	Chip Enable to End of Write	50		60		ns	
24	t_{DVEH}	t_{DW}	Data Set-up to End of Write	25		30		ns	
25	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		ns	
26	t_{AVEH}	t_{AW}	Address Set-up to End of Write	50		60		ns	
27	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		ns	
28	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		ns	
29	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	25	0	30	ns	g

Note g: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} (min) to V_{IL} (max) or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note i: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note j: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.

DEVICE OPERATION

The IMS1620M has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), fourteen address inputs (A_0 - A_{13}), and four Data I/O lines.

The IMS1620M becomes active immediately after V_{CC} is applied, with proper operation assured 500 microseconds after V_{CC} reaches 4.5 volts. With $\overline{E}$ low, the device is selected and the fourteen address inputs are decoded to select one 4-bit word out of 16,384. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

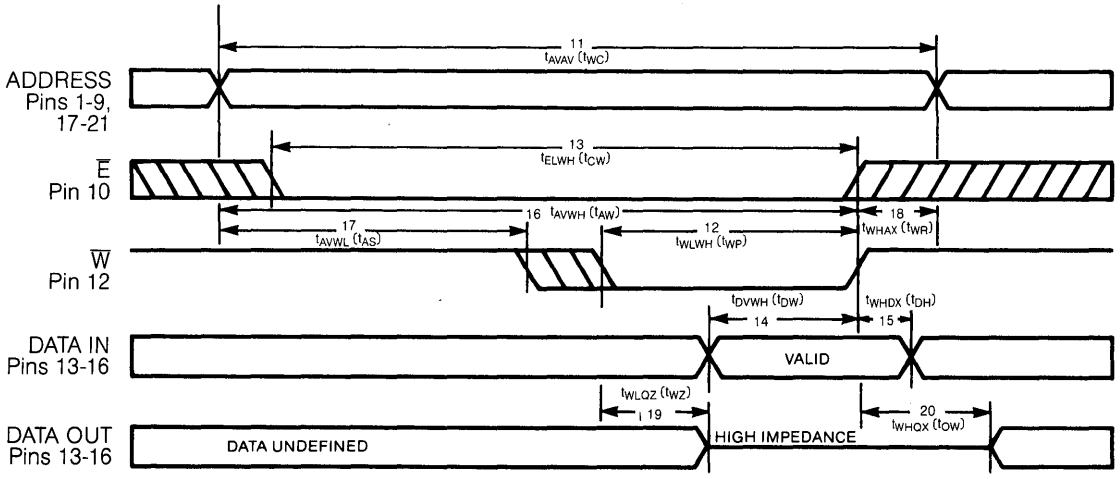
READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min. with $\overline{E} \leq V_{IL}$ max. Read access time is measured from the latter of either $\overline{E}$ going low or from valid address.

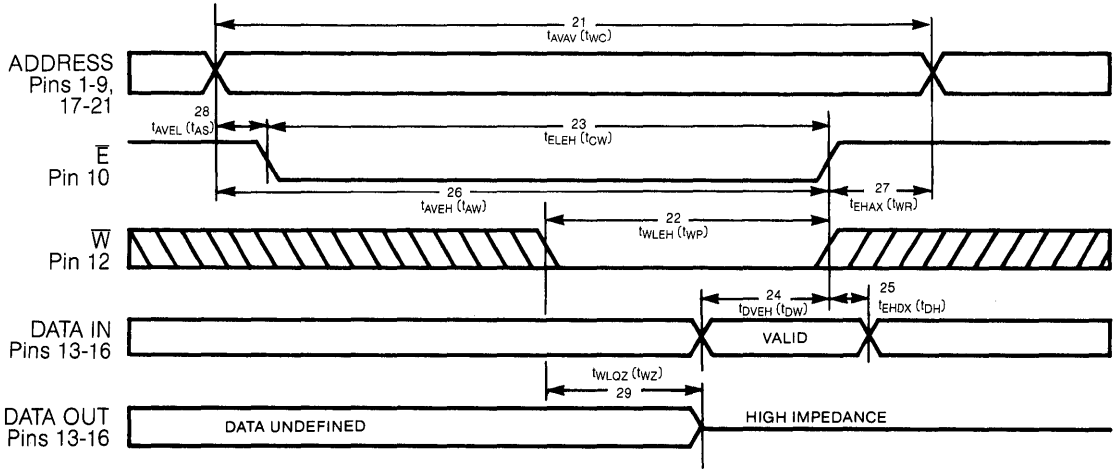
The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of t_{AXQV}. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE 1



WRITE CYCLE 2



WRITE CYCLE

The write cycle of the IMS1620M is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high level to a low level. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common input/output connections. Therefore input data should not be active until after t_{WLQZ} to avoid bus contention. During a write cycle, data on the inputs is written into the selected cells and the outputs are floating.

If a write cycle is initiated by $\overline{E}$ going low, the address must be stable for t_{AVEL} referenced to $\overline{E}$. If the write cycle is initiated by $\overline{W}$ going low, then the address must be valid for t_{AVWL} referenced to $\overline{W}$. The address must be held stable for the entire write cycle. After either $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If set-up and hold times are not met, for either address or data, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high while $\overline{E}$ is low, the outputs become active. When $\overline{W}$ goes high at the end of a write cycle and the outputs of the memory go active, the data from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

It is imperative, when designing with any very high speed memory such as the IMS1620M, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

TTL VS. CMOS INPUT LEVELS

The IMS1620M is fully compatible with TTL input levels. The input circuitry of the IMS1620M is designed for maximum speed and also for conversion of TTL level signals to the CMOS levels required for internal operation. The IMS1620M consumes less power when CMOS levels (.3/V_{CC} −.3 volts) are used than TTL levels (.8/2.0 volts) are applied. The lower CMOS I_{CC} specifications, I_{CC3} and I_{CC4}, may be achieved by using CMOS levels. The power consumption will be lower at typical TTL levels than at the worst case levels.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the wide operating margins of the IMS1620M. The impedance in the decoupling path from the power pin (22) through the decoupling capacitor to the ground pin (11) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1620M have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as near the memory board as possible, with the shortest lead lengths practical. The high frequency decoupling capacitor should have a minimum value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor, for low frequency current transients, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

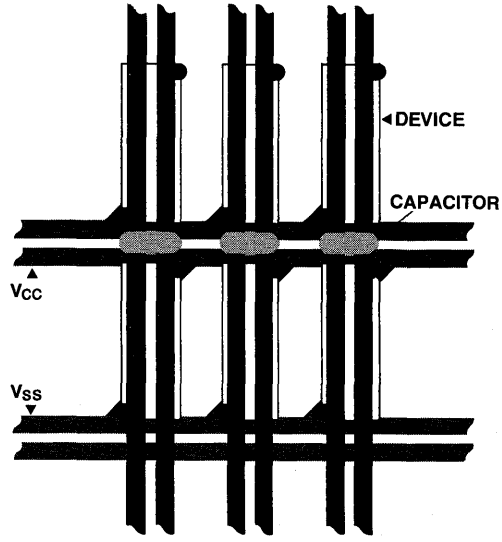
Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The termination resistor should be placed as close to the driver package as possible. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33ohm range will be required. Because the characteristic impedance of each layout will be different, it is necessary to select the proper value of this resistor by trial and error. A resistor of predetermined value may not properly terminate the transmission line.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilizing a wideband oscilloscope and probe.

When using WRITE CYCLE 1, care should be taken to avoid bus contention. When $\overline{W}$ goes high, with $\overline{E}$ low, the output buffers will be active t_{WHQX} after the rising edge of $\overline{W}$. Data out will be the same as the data just written, unless the address changes. If Data-in from the previous cycle is still valid after the address changes, contention may result. Contention may also result if $\overline{E}$ goes low before $\overline{W}$, with Data-in valid early in the cycle. INMOS Application Note #5, "Bus Contention Considerations," provides a detailed analysis of contention and methods used to control bus contention.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

ASYNCHRONOUS VS. SYNCHRONOUS OPERATION

Fast, high density Static RAMs have a finite probability of encountering transient (non-catastrophic) errors[1] particularly when operated in a totally asynchronous manner. Therefore, in applications where extremely low error rates are essential, it is recommended that synchronous operation be considered. Synchronous operation is accomplished by allowing address changes during device deselect intervals ($\overline{E}$ high) only.

[1]Chappell, Schuster, Sai-Halasz, "Stability and Soft Error Rates of SRAM Cells," ISSCC Digest of Technical Papers, p. 162-163; Feburary 1984.

INMOS MILITARY STANDARD PROGRAM*

The INMOS military program is designed to provide compliance to MIL-STD-883C. This includes screening per Method 5004, quality conformance testing per method 5005, and the applicable provisions of MIL-M-38510. The IMS1620M is processed for general applications where component quality and reliability must conform to the guidelines and objectives of military procurement. Suitability for use in specific applications should be determined using the guidelines of MIL-STD-454.

Component screening, as depicted in Table 1, defines the sequence used for production of INMOS military products. This sequence assures compliance with methods 5004, 5005, and their applicable sub-methods. All electrical testing is performed to guarantee operation at −55°C, +25°C, and +125°C T_A, with applicable quality conformance testing per the requirements of MIL-M-38510. Additionally, INMOS includes as standard screening, the requirements of method 5004 paragraph 3.3 on all military grade products.

All INMOS military grade components are hermetically sealed in metal to ceramic packages and contain an organic RTV silicon alpha particle overcoat. Dual in line packages are per MIL-M-38510 appendix C case outline D7 configuration 3. The 22 pin rectangular leadless chip carrier has not been designated in MIL-M-38510 and is supplied to the INMOS case outline defined herein.

By specifying the IMS1620M the user can be assured of receiving a product manufactured, tested and inspected in compliance with MIL-STD-883C and one with superior performance for those applications where quality and reliability are of the essence.

TABLE I

100 PERCENT PROCESS STEP	MIL-STD-883C METHOD	TEST CONDITION	COMMENT
INTERNAL VISUAL	2010	B	
STABILIZATION BAKE	1008	C	
TEMPERATURE CYCLE	1010	C	
CONSTANT ACCELERATION	2001	E	Y-1 AXIS
SEAL TEST	1014	B	
SEAL TEST	1014	C	
VISUAL INSPECTION			INMOS 80-1001
PRE BURN IN ELECTRICAL			+25°C DATA SHEET
BURN IN	1015	D	
POST BURN ELECTRICAL			+25°C DATA SHEET
PDA			5% MAX
FINAL ELECTRICAL			+125°C DATA SHEET
FINAL ELECTRICAL			−55°C DATA SHEET
EXTERNAL VISUAL	2009		
GROUP A	5005	3.5.1	A1-A11
GROUP B	5005	3.5.2	
GROUP C	5005		MIL-STD-883C 1.2.1.b.17
GROUP D	5005		

*See Inmos Document 41-9047 "Military General Processing Specification" for full details.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1620M	55ns	CERAMIC DIP	IMS1620S-55M
	70ns	CERAMIC DIP	IMS1620S-70M

Also available in Ceramic Chip Carrier, specifications not available at time of publication.

IMS2600M

High Performance 64Kx1 Dynamic RAM (MIL-STD-883C)

Military

FEATURES

- Specifications guaranteed over full military DRAM temperature range (−55°C to +110°C)
- MIL-STD-883C Processing
- High Speed, $\overline{RAS}$ Access of 120 and 150ns
- Cycle Times of 190 and 230ns
- Low Power:
  28mW Standby
  358mW Active (350ns Cycle Time)
  468mW Active (190ns Cycle Time)
- Single +5V ± 10% Power Supply
- On-Chip refresh using $\overline{CAS}$-before-$\overline{RAS}$, Pin 1 left as N/C for 256K expansion
- Indefinite D_{OUT} Hold Under $\overline{CAS}$ Control
- Industry Standard 16 Pin Configuration
- Nibble-Mode Capability (High Speed 4 Bit Serial Mode)
- 4ms/256 Cycle Refresh
- All Inputs and Output TTL Compatible
- Read, Write, Read-Modify-Write Capability both on Single Bit and in Nibble Mode Operation
- $\overline{RAS}$-Only Refresh Capability
- Common I/O Capability using "Early-Write"

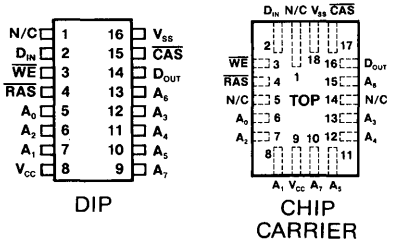
DESCRIPTION

The Extended Temperature IMS2600M 64K x 1 bit dynamic RAM is processed 100% in full compliance to MIL-STD-883C with access times of 120 and 150ns. The RAM is fabricated with INMOS' advanced N-MOS technology and utilizes innovative circuit techniques to achieve high performance, low power and wide operating margins. Multiplexed addressing allows the IMS2600M to be packaged in a standard 16-pin DIP. Additionally, the IMS2600M features new functional enhancements that make it more versatile than previous dynamic RAMs. $\overline{CAS}$-before-$\overline{RAS}$ refresh provides an on-chip refresh mechanism that is upward compatible to 256K dynamic RAMs because pin 1 is left as a no-connect. The IMS-2600M also features "nibble mode" which allows high speed serial access of up to 4 bits of data, thus providing the system equivalent of 4-way interleaving on chip.

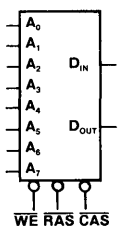
The IMS2600M is fully TTL compatible on all inputs and the output, and operates from a single +5V ± 10% power supply.

The IMS2600M is a cost-effective VLSI RAM intended for military temperature applications that demand high density as well as superior performance and reliability.

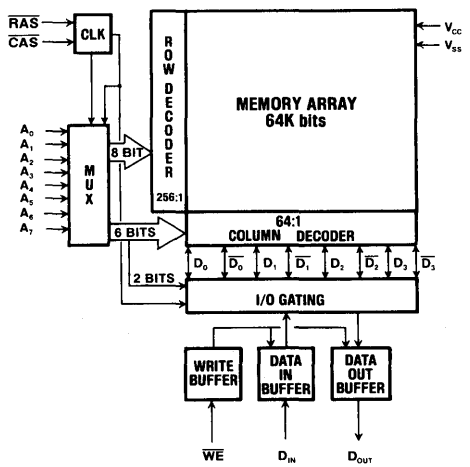
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5 VOLT SUPPLY INPUT
V_{SS}	GROUND

DEVICE OPERATION

The IMS2600M contains 65536 (2^{16}) bits of information as 256 (2^8) rows by 256 (2^8) columns. The sixteen addresses for unique bit selection are time-division multiplexed over eight address lines under control of the Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$) clocks. The normal sequence of $\overline{RAS}$ and $\overline{CAS}$ requires that $\overline{CAS}$ is high as $\overline{RAS}$ goes low. This causes the eight address inputs to be latched and decoded for selection of one of the 256 rows. The row addresses must be held for the specified period [t_{RAH} (min)] and then they may be switched to the appropriate column address. After the column addresses are stable for the specified column address setup time, $\overline{CAS}$ may be brought low. This causes the eight address inputs to be latched and used to select a single column in the specified row. The cycle is terminated by bringing $\overline{RAS}$ high. A new cycle may be initiated after $\overline{RAS}$ has been high for the specified precharge interval [t_{RP} (min)]. $\overline{RAS}$ and $\overline{CAS}$ must be properly overlapped and once brought low they must remain low for their specified pulse widths.

READ CYCLE

A read cycle is performed by sequencing $\overline{RAS}$ and $\overline{CAS}$ as described above while holding the $\overline{WE}$ input high during the period when $\overline{RAS}$ and $\overline{CAS}$ are both low. The read access time will be determined by the actual timing relationship between $\overline{RAS}$ and $\overline{CAS}$. If $\overline{CAS}$ goes low within the specified $\overline{RAS}$-to-$\overline{CAS}$ delay [t_{RCD} (max)], then the access time will be determined by $\overline{RAS}$ and be equal to t_{RAC} (max). If $\overline{CAS}$ occurs later than t_{RCD} (max) then the access time is measured from $\overline{CAS}$ and will be equal to t_{CAC} (max).

WRITE CYCLE

The IMS2600M will perform three types of write cycles: Early-Write, Late-Write or Read-Modify-Write. The difference between these cycles is that on an Early-Write D_{OUT} will remain open and on a Late-Write or Read-Modify-Write D_{OUT} will reflect the contents of the addressed cell before it was written.

The type of write cycle that is performed is determined by the relationship between $\overline{CAS}$ and $\overline{WE}$. For Early-Write cycles $\overline{WE}$ occurs before $\overline{CAS}$ goes low, and D_{IN} setup is referenced to the falling edge of $\overline{CAS}$. For Late-Write or Read-Modify-Write cycles $\overline{WE}$ occurs after $\overline{CAS}$, and D_{IN} setup is referenced to the falling edge of $\overline{WE}$.

The choice of write cycle timing is usually very system dependent and the different modes are made available to accommodate these differences. In general, the Early-Write timing is most appropriate for systems that have a bidirectional data bus. Because D_{OUT} remains inactive during Early-Write cycles, the D_{IN} and D_{OUT} pins may be tied together without bus contention.

DEVICE SELECTION AND OUTPUT CONTROL

Selection of a memory device for a read or write operation requires that both $\overline{RAS}$ and $\overline{CAS}$ be sequenced. A device is not selected if $\overline{RAS}$ is sequenced while $\overline{CAS}$ remains high or if $\overline{CAS}$ is sequenced while $\overline{RAS}$ remains high. The device must receive a properly overlapped $\overline{RAS}$/$\overline{CAS}$ sequence to be selected.

Once a device is selected the state of D_{OUT} becomes entirely controlled by $\overline{CAS}$. If $\overline{CAS}$ remains low when $\overline{RAS}$ goes high, D_{OUT} will remain in the state it was in when $\overline{RAS}$ went high. The output will remain unchanged even if a $\overline{RAS}$ sequence occurs while $\overline{CAS}$ is held low.

REFRESH

The IMS2600M remembers data by storing charge on a capacitor. Because the charge will leak away over a period of time it is necessary to access the data in the cell (capacitor) periodically in order to fully restore the stored charge while it is still at a sufficiently high level to be properly detected. For the IMS2600M any $\overline{RAS}$ sequence will fully refresh an entire row of 256 bits. To ensure that all cells remain sufficiently refreshed, all 256 rows must be refreshed every 4 ms.

The addressing of the rows for refresh may be sourced either externally or internally. If the row refresh addresses are to be provided from an external source, $\overline{CAS}$ must be high when $\overline{RAS}$ goes low. If $\overline{CAS}$ is high when $\overline{RAS}$ goes low, any type of cycle (Read, Write, Read-Modify-Write or $\overline{RAS}$ only) will cause the addressed row to be refreshed.

If $\overline{CAS}$ is low when $\overline{RAS}$ falls, the IMS2600M will use an internal 8-bit counter as the source of the row addresses and will ignore the address inputs. This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh-only mode and no data access is allowed. Also, $\overline{CAS}$-before-$\overline{RAS}$ refresh does not cause device selection and the state of D_{OUT} will remain unchanged.

NIBBLE MODE

The IMS2600M is designed to allow high-speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during Nibble Mode are determined by the eight row addresses and the most significant 6 bits of the column address. The low-order 2 bits of the column address (A_3, A_6) are used to select one of the 4 nibble bits for initial access. After the first bit is accessed the remaining nibble bits may be accessed by bringing $\overline{CAS}$ high then low (toggle) while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes A_3 and A_6 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for read, write and/or read-modify-write access (See Table 1 for example). If more than 4 bits are accessed during Nibble Mode, the address sequence will begin to repeat. If any bit is written during an access, the new value will be read on any subsequent accesses.

In Nibble Mode, read, write and read-modify-write operations may be performed in any desired combination. (e.g., first bit read, second bit write, third bit read-modify-write, etc.)

Table 1

NIBBLE MODE ADDRESSING SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	ROW ADDRESSES	COLUMN ADDRESSES A_3, A_6	
$\overline{RAS}$/$\overline{CAS}$	1	10101010	10101010	generated externally
toggle $\overline{CAS}$	2	10101010	10101011	
toggle $\overline{CAS}$	3	10101010	10101000	generated internally
toggle $\overline{CAS}$	4	10101010	10101001	
toggle $\overline{CAS}$	1	10101010	10101010	sequence repeats

ABSOLUTE MAXIMUM RATINGS*[a]

Voltage on V_{CC} Relative to V_{SS} . . . . . −1.0V to +7.0V
Storage Temp. (Ceramic Package) . . . −65°C to +150°C
Power Dissipation. 1W
Short Circuit Output Current. 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS[a, b]

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage		0		V	
V_{IH}	Logic "1" Voltage	2.4		V_{CC} + 1	V	
V_{IL}	Logic "0" Voltage	−2.0		0.8	V	
T_A	Ambient Operating Temperature	−55°		110	°C	Still Air

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 110°C$, $V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current (Operating) IMS2600M-12		85	mA	t_{RC} = 190ns, t_{RAS} = 120ns (C)
	IMS2600M-12		65		t_{RC} = 350ns, t_{RAS} = 120ns
	IMS2600M-15		75		t_{RC} = 230ns, t_{RAS} = 150ns
	IMS2600M-15		65		t_{RC} = 350ns, t_{RAS} = 150ns
I_{CC_2}	V_{CC} Power Supply Current (Active)		20	mA	RAS ≤ V_{IL} (max), CAS ≤ V_{IL} (max)
I_{CC_3}	Standby Current		5.0	mA	RAS ≥ V_{IH} (min), CAS ≥ V_{IH} (min)
I_{IN}	Input Leakage Current (Any Input)	−10	10	μA	0V ≤ V_{IN} ≤ 5.5V, others = 0V
I_{OLK}	Output Leakage Current	−10	10	μA	D_{OUT} = Hi Z, 0V ≤ V_{OUT} ≤ 5.5V
V_{OH}	Output High Voltage	2.4		V	I_O = −5.0mA
V_{OL}	Output Low Voltage		0.4	V	I_O = 5.0mA

Note a: All voltage values in this data sheet are with respect to V_{SS}.
b: After power-up, a pause of 500 μs followed by eight initialization memory cycles is required to achieve proper device operation. Any interval greater than 4ms with $\overline{RAS}$ inactivity requires eight reinitialization cycles to achieve proper device operation.
c: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with output open.

AC TEST CONDITIONS

Input Pulse Levels. . . . . 0 to 3V
Input Rise and Fall Times. . . . . 5ns between 0.8 and 2.4V
Input Timing Reference Levels. . . . . 0.8 and 2.4V
Output Timing Reference Levels. . . . . 0.8 and 2.4V
Output Load. . . . . Equivalent to 2 TTL Loads and 50pF

CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS	COND.
C_{IN}	Input Cap. $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	6	pF	d
C_{IN}	Input Cap. Addresses	5	pF	d
C_{OUT}	Output Cap.	7	pF	d o

Note d: Capacitance measured with BOONTON METER.
o: $\overline{CAS}$ = V_{IH} to disable D_{OUT}

AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2600M-12		2600M-15		UNITS	NOTES
			MIN	MAX	MIN	MAX		
1	t_{RC}	Random Read Cycle Time	190		230		ns	
2	t_{RAC}	Access Time from $\overline{RAS}$		120		150	ns	h
3	t_{CAC}	Access Time from $\overline{CAS}$		75		90	ns	i
4	t_{RAS}	$\overline{RAS}$ Pulse Width	120	10K	150	10K	ns	
5	t_{RSH}	$\overline{RAS}$ Hold Time	75		90		ns	
6	t_{CAS}	$\overline{CAS}$ Pulse Width	75		90		ns	
7	t_{CSH}	$\overline{CAS}$ Hold Time	120		150		ns	
8	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	17	45	20	60	ns	e j
9	t_{CRS}	$\overline{CAS}$ to $\overline{RAS}$ Set-up Time	0		0		ns	
10	t_{RP}	$\overline{RAS}$ Precharge Time	60		70		ns	
11	t_{ASR}	Row Address Set-up Time	0		0		ns	
12	t_{RAH}	Row Address Hold Time	12		15		ns	
13	t_{ASC}	Column Address Set-up Time	−0		−0		ns	
14	t_{CAH}	Column Address Hold Time (Ref. $\overline{CAS}$)	35		45		ns	
15	t_{AR}	Column Address Hold Time (Ref. $\overline{RAS}$)	75		95		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		ns	
17	t_{RCH}	Read Command Hold Time (Ref. $\overline{CAS}$)	0		0		ns	k
18	t_{RRH}	Read Command Hold Time (Ref. $\overline{RAS}$)	0		0		ns	k
19	t_{OFF}	Output Buffer Turn-off Delay	0	25	0	30	ns	f
20	t_{WCS}	Write Command Set-up Time	0		0		ns	m
21	t_{WCH}	Write Command Hold Time (Ref. $\overline{CAS}$)	30		35		ns	
22	t_{WCR}	Write Command Hold Time (Ref. $\overline{RAS}$)	70		85		ns	
23	t_{WP}	Write Pulse Width	25		30		ns	
24	t_{DS}	Data-in Set-up Time	0		0		ns	l
25	t_{DH}	Data-in Hold Time (Ref. $\overline{CAS}$)	30		35		ns	l
26	t_{DHR}	Data-in Hold Time (Ref. $\overline{RAS}$)	70		85		ns	
27	t_{RW}	Read-Write Cycle Time	215		260		ns	
27	t_{RMW}	Read-Modify-Write Cycle Time	225		270		ns	
28	t_{RRW}	Read-Write Cycle $\overline{RAS}$ Pulse Width	145		180		ns	
28	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	155		190		ns	
29	t_{CRW}	Read-Write Cycle $\overline{CAS}$ Pulse Width	105		130		ns	
29	t_{CRW}	Read-Modify-Write Cycle $\overline{CAS}$ Pulse Width	115		140		ns	
30	t_{RWD}	$\overline{RAS}$ to Write Delay	110		140		ns	m
31	t_{CWD}	$\overline{CAS}$ to Write Delay	70		90		ns	m
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35		ns	

AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYMBOL	PARAMETER	2600M-12		2600M-15		UNITS	NOTES
			MIN	MAX	MIN	MAX		
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		35		ns	
34	t_{NC}	Nibble Mode Read Cycle Time	65		75		ns	
35	t_{NCAC}	Nibble Mode Access Time from $\overline{CAS}$		30		35	ns	
36	t_{NCAS}	Nibble Mode $\overline{CAS}$ Pulse Width	30		35		ns	
37	t_{NCP}	Nibble Mode $\overline{CAS}$ Precharge Time	25		30		ns	
38	t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	30		35		ns	
39	t_{NRMW}	Nibble Mode Read-Modify-Write Cycle Time	95		110		ns	
40	t_{NCRW}	Nibble Mode R-M-W $\overline{CAS}$ Pulse Width	60		70		ns	
41	t_{NCWD}	Nibble Mode $\overline{CAS}$ to Write Delay	25		30		ns	
42	t_{FCS}	Refresh Set-up for $\overline{CAS}$ (Ref. $\overline{RAS}$)	0		0		ns	
43	t_{FCH}	Refresh Hold Time (Ref. $\overline{RAS}$)	17		20		ns	
	t_{REF}	Refresh Period		4		4	ms	
	t_T	Input Rise and Fall Times	3	50	3	50	ns	n

NOTES:

e: t_{RCD} (max) is a derived parameter; t_{RCD} (max) = t_{RAC} (max) − t_{CAC} (max); t_{RCD} (min) is a restrictive parameter due to CAS-before-RAS refresh.

f: t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition.

h: Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).

i: Assumes that $t_{RCD} \geq t_{RCD}$ (max).

j: Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is determined exclusively by t_{CAC}.

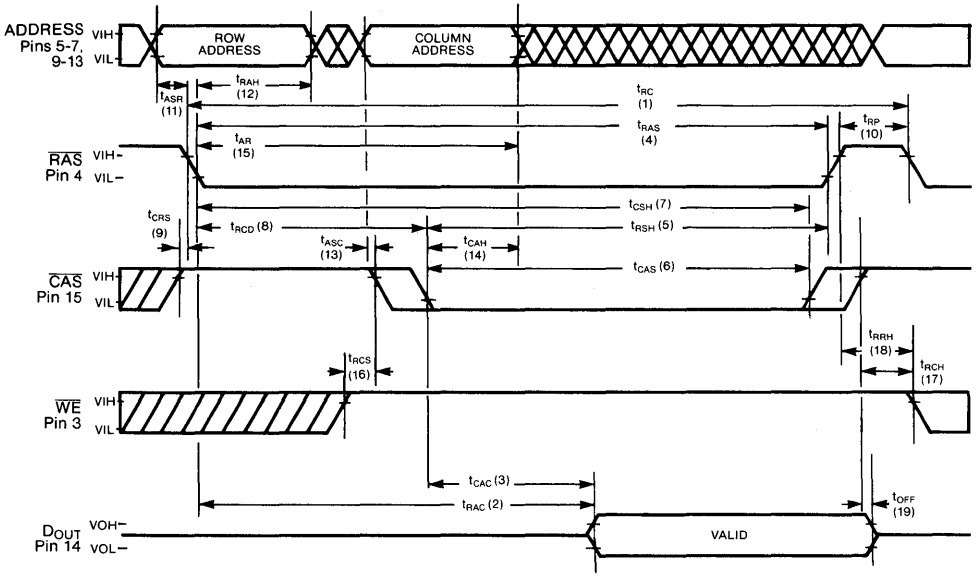
k: Either t_{RRH} or t_{RCH} must be satisfied for a Read cycle.

l: These parameters are referenced to CAS leading edge in Early-Write cycles, and to WE leading edge in Read-Write or Read-Modify-Write cycles.

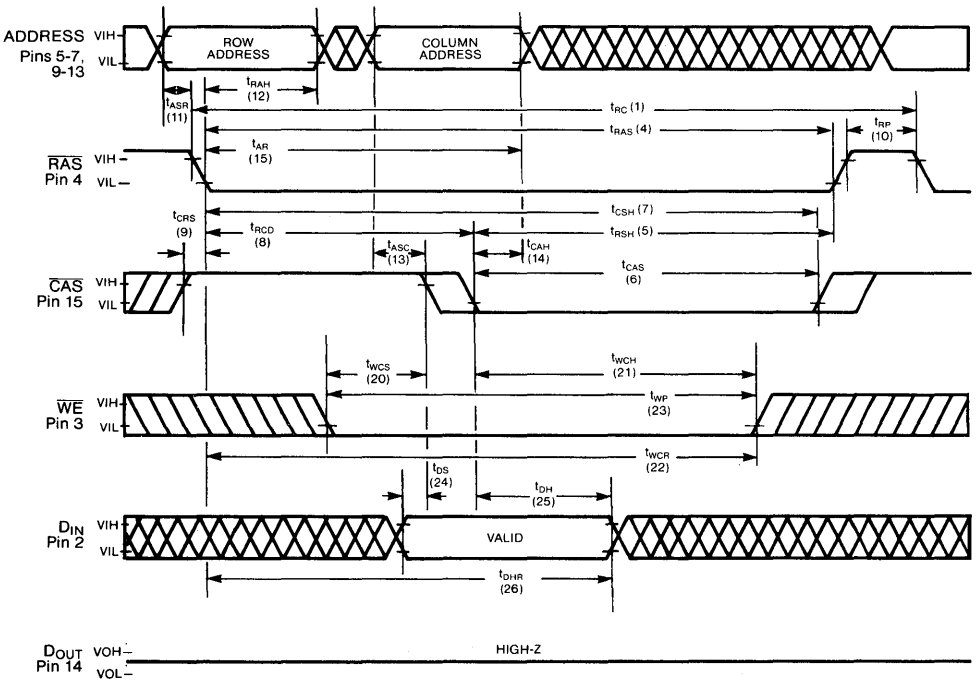
m: t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an Early-Write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a Read-Write and the data output will contain data read from the selected cell. If neither of the above conditions is met the condition of the data out is indeterminate at access time and remains so until CAS returns to V_{IH}.

n: The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Transition time measured between V_{IL} (max) and V_{IH} (min).

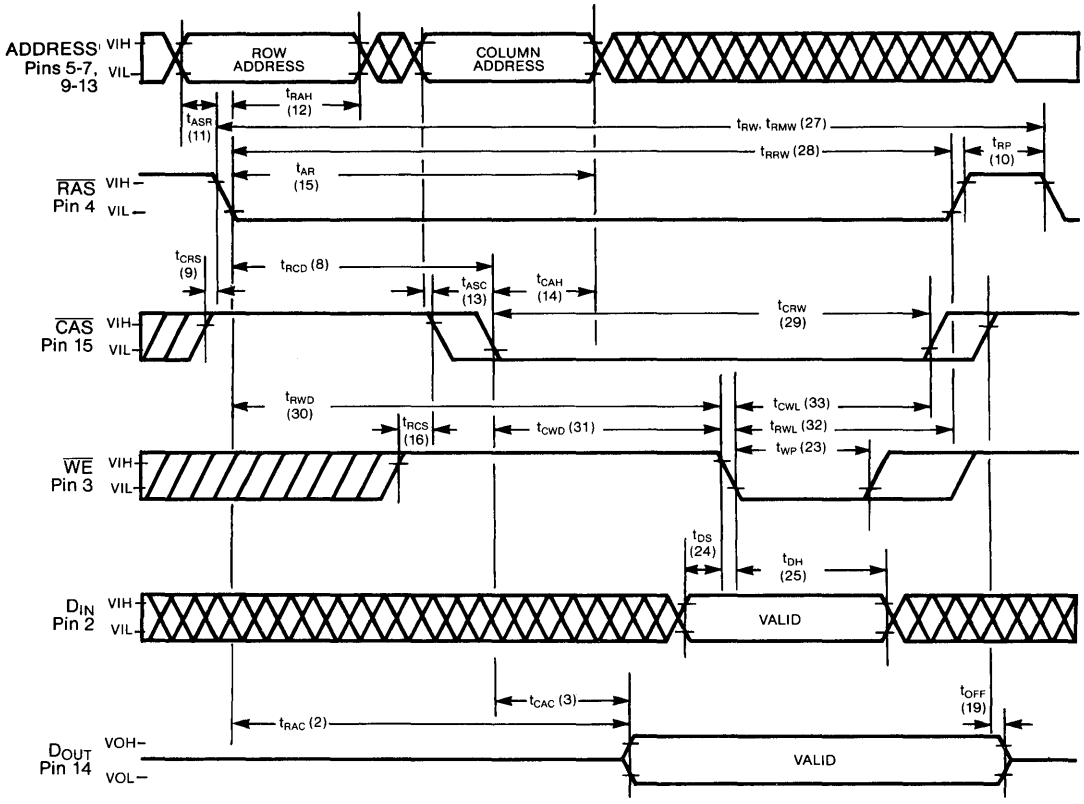
READ CYCLE



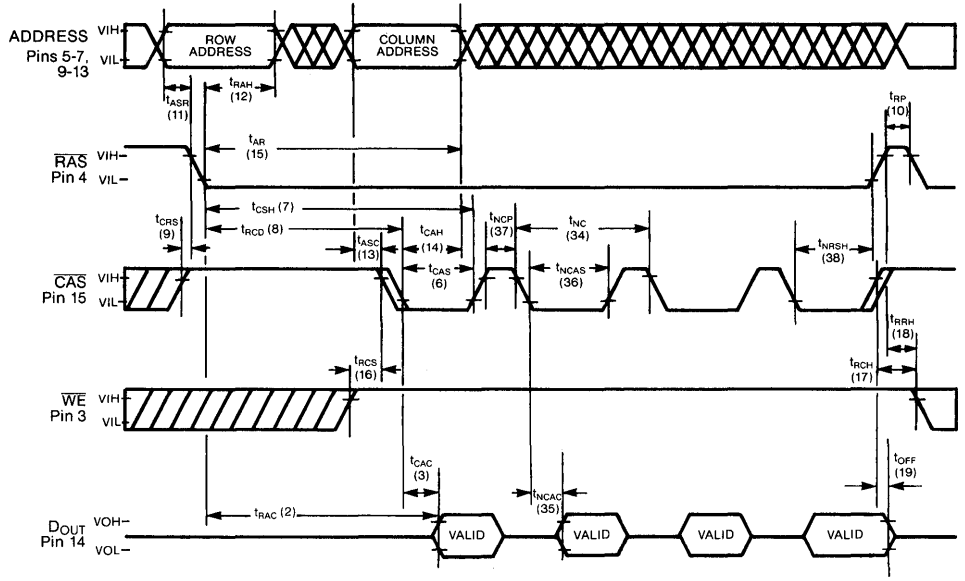
WRITE CYCLE



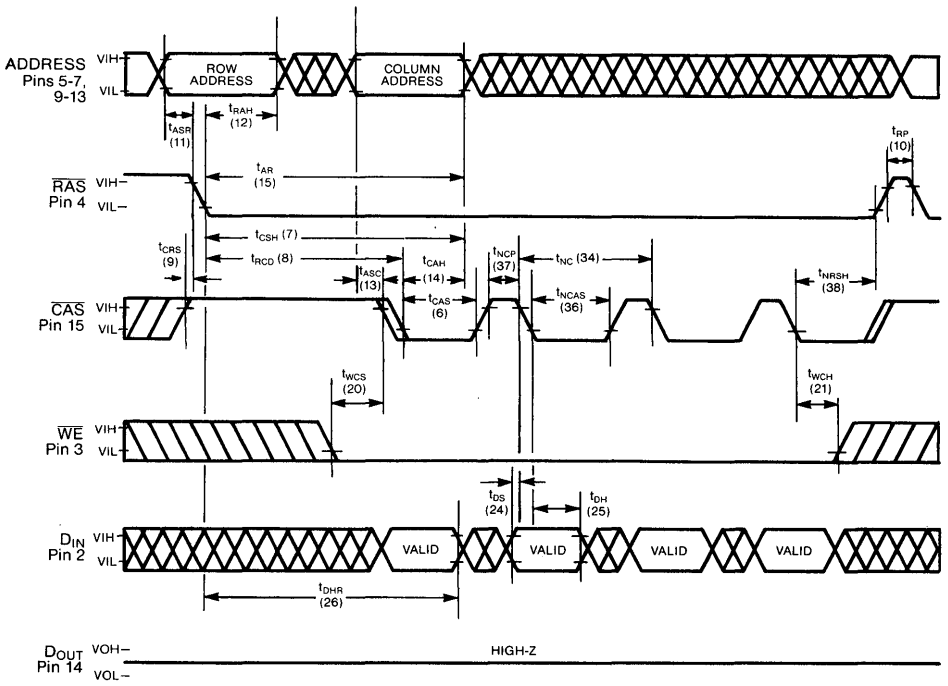
READ-WRITE/READ-MODIFY-WRITE CYCLE



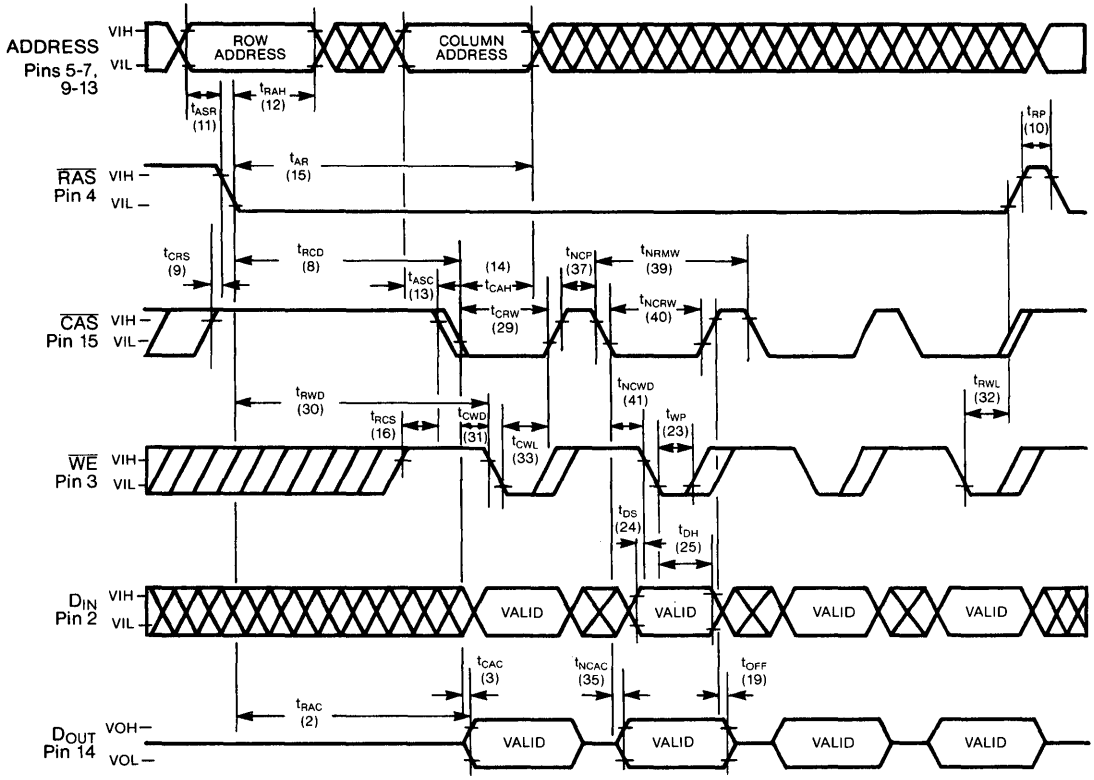
NIBBLE MODE READ CYCLE



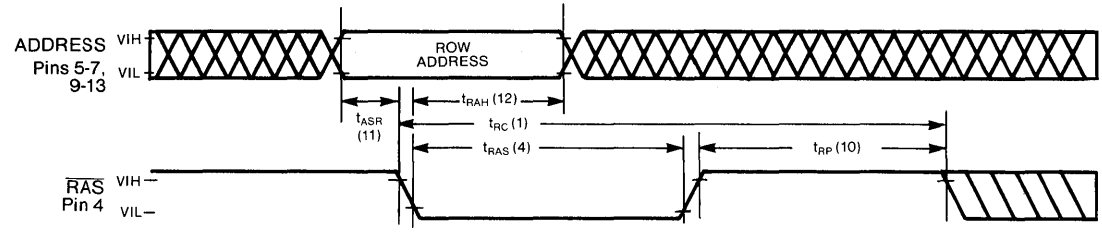
NIBBLE MODE WRITE CYCLE



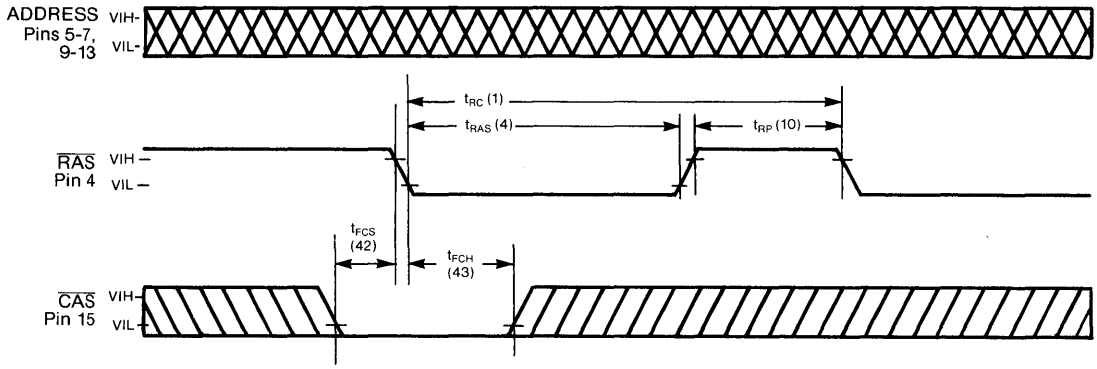
NIBBLE MODE READ-MODIFY-WRITE CYCLE



$\overline{\text{RAS}}$-ONLY REFRESH [$\overline{\text{CAS}} \geq V_{IH}$ (min)]



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH



APPLICATION

To ensure proper operation of the IMS2600M in a system environment it is recommended that the following guidelines on board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (8) through the decoupling capacitor, to the ground pin (16) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line and the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. To prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry. A high-frequency decoupling capacitor with a value of 0.1μF should be placed between the rows of memory devices in the array. A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propogating down the lines, especially low-going TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver/termination combination close to the memory array. Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are among the most important, yet basic guidelines to be followed. These guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

INMOS MILITARY STANDARD PROGRAM*

The INMOS military program is designed to provide full compliance to MIL-STD 883C. This includes screening per Method 5004, quality conformance testing per Method 5005, and the applicable provisions of MIL-M-38510. The IMS2600M is processed for general applications where component quality and reliability must conform to the guidelines and objectives of military procurement. Suitability for use in specific applications should be determined using the quidelines of MIL-STD-454.

Component screening, as depicted in Table 1, defines the sequence used for production of INMOS military products. This sequence assures compliance with methods 5004, 5005, and their applicable sub-methods. All electrical testing is performed at military temperatures of −55°C, +25°C, and +110°C with applicable quality conformance testing per the requirements of MIL-M-38510. Additionally, INMOS includes as standard screening, the requirements of method 5004 paragraph 3.3 on all military grade products.

All INMOS military grade components are hermetically sealed in metal to ceramic packages and contain an organic RTV silicon alpha particle overcoat. Dual in line packages are per MIL-M-38510 appendix C case outline D8 configuration 3.

By specifying the IMS2600M, the user can be assured of receiving a product manufactured, tested and inspected in full compliance with MIL-STD-883C and one with superior performance for those applications where quality and reliability are of the essence.

TABLE I

100 PERCENT PROCESS STEP	MIL-STD-883C METHOD	TEST CONDITION	COMMENT
INTERNAL VISUAL	2010	B	
STABILIZATION BAKE	1008	C	
TEMPERATURE CYCLE	1010	C	
CONSTANT ACCELERATION	2001	E	Y-1 AXIS
SEAL TEST	1014	B	
SEAL TEST	1014	C	
VISUAL INSPECTION			INMOS 80-1001
PRE BURN IN ELECTRICAL			+25°C DATA SHEET
BURN IN	1015	D	
POST BURN ELECTRICAL			+25°C DATA SHEET
PDA			5% MAX
FINAL ELECTRICAL			+110°C DATA SHEET
GROUP A	5005	3.5.1	A2, A5, A8, A10
FINAL ELECTRICAL			−55°C DATA SHEET
GROUP A	5005	3.5.1	A3, A6, A8, A11
EXTERNAL VISUAL	2009		
GROUP A	5005	3.5.1	A1, A4, A7, A9
GROUP B	5005	3.5.2	
GROUP C	5005		MIL-STD-883C 1.2.1.b.17
GROUP D	5005		

*See Inmos Document 41-9047 "Military General Processing Specification" for full details.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS2600M	120ns	CERAMIC DIP	IMS2600S-12M
	150ns	CERAMIC DIP	IMS2600S-15M

Video 4

Video Selection Guide

Device	Pixel Rates (MHz)	Power Supply Volts	Video Compatible	Signal Output	Possible Colors	DAC	Number of Pins	Package	Process
IMSG170	20,35,50	+5	RS170A	75Ω	256K	3 (6-bit)	28	S	CMOS

NOTES:
S = Ceramic DIP

IMSG170

High Performance CMOS Color look-up table

Preliminary

FEATURES

- Compatible with the RS 170A video standard
- Pixel rates up to 50 MHz
- 256K possible colors
- Single monolithic, high performance CMOS
- Pixel address mask
- RGB analog output, 6 bit DAC per gun, composite blank + sync
- Low DAC glitch energy
- Video signal output into 75 ohms
- TTL compatible inputs
- Microprocessor compatible write interface
- Single +5V ± 10% power supply
- Low power dissipation, 750mW max at maximum pixel rate
- Standard 600 mil 28 pin DIP package

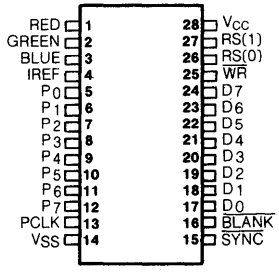
DESCRIPTION

The IMSG170 integrates the function of a color look-up table (or color palette), digital-analog convertors (with 75Ω outputs) and microprocessor interface into a single 28 pin package.

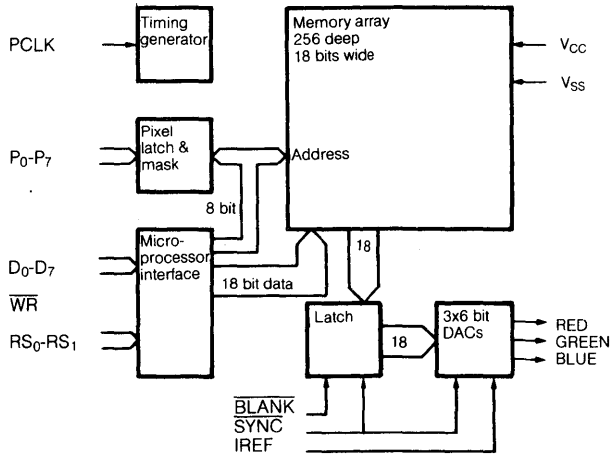
At any time, a set of up to 256 colors may be selected for display from a palette of 256K. The IMSG170 significantly reduces component cost, board area, and power consumption.

The pixel word mask allows displayed colors to be changed in a single write cycle rather than by modifying the look-up table.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES	
P_0-P_7	Pixel address inputs
D_0-D_7	Program data inputs
RS_0-RS_1	Register select
RED, GREEN, BLUE	Analog video outputs
PCLK	Pixel clock
$\overline{WR}$	Write enable
$\overline{BLANK}$	Video blanking input
$\overline{SYNC}$	Video sync input
IREF	Reference current
V_{CC}	+5 volt supply input
V_{SS}	Ground

FUNCTIONAL DESCRIPTION

PIXEL INTERFACE

SIGNAL	PIN	INPUT/ OUTPUT	SIGNAL NAME	DESCRIPTION
PCLK	13	Input	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address, Blanking and Sync inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the Color Look-Up Table to the analog outputs.
P_0-P_7	5-12	Input	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel Mask Register and then used as the address into the Color Look-Up Table. This causes an internal 18 bit wide color value to be produced.
$\overline{BLANK}$	16	Input	Blanking	A low value on this input, when sampled, will cause a color value of zero to be applied to the inputs of the DACs regardless of the color value of the current pixel.
$\overline{SYNC}$	15	Input	Sync	The value on this input, when sampled, controls an offset on the analog outputs, the offset being 30% of the full scale analog output. If $\overline{SYNC}$ is low there is no offset, if $\overline{SYNC}$ is high the offset is active.

ANALOG INTERFACE

SIGNAL	PIN	INPUT/ OUTPUT	SIGNAL NAME	DESCRIPTION
RED, GREEN, BLUE	1 2 3	Output Output Output	Red, Green, Blue,	These three signals are the outputs of three 6 bit DACs. Each DAC is composed of 90 current sources whose outputs are summed. 63 of the current sources are controlled by the binary input to the DACs, 27 are controlled by the $\overline{SYNC}$ signal.
IREF	4	Input	Reference Current	The Reference Current drawn from V_{CC} via the IREF pin determines the current sourced by each of the current sources in the DACs. Each current source producing 1/30 of IREF when turned on.

MICROPROCESSOR INTERFACE

SIGNAL	PIN	INPUT/ OUTPUT	SIGNAL NAME	DESCRIPTION
$\overline{WR}$	25	Input	Write Enable	The Write Enable signal controls the timing of write operations to the microprocessor interface. A minimum high period for the Write Enable signal is specified in terms of the Pixel Clock period allowing the two signals to be asynchronous.
RS_0-RS_1	26-27	Input	Register Select	The values on these inputs are sampled on the falling edge of the Write Enable signal, they specify which one of the three internal registers is to be written to next. See internal Register description for the function of these three registers.
D_0-D_7	17-24	Input	Program Data	On the rising edge of Write Enable the byte value on the Program Data inputs is written to the specified register.

INTERNAL REGISTERS

RS_1	RS_0	SIZE (BITS)	REGISTER NAME	DESCRIPTION
0	0	8	Pixel Address	The Pixel Address register is written with an 8 bit value to address a location within the Color Look-Up Table.
0	1	18	Color Value	The Color Value register is internally an 18 bit wide register. The 18 bit value is formed by the concatenation of the least significant 6 bits from each of 3 bytes written to the Color Value register. The first value written will be applied to the red DAC, the second to the green DAC and the third to the blue DAC. After the third byte is written to the Color Value register the 18 bit word will be written to the location in the Color Look-Up Table specified by the current contents of the Pixel Address register. The Pixel Address register is then incremented.
1	Don't Care	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P_0-P_7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, a zero setting that bit to zero. The Pixel Mask register does not affect the Pixel Address generated by the Microprocessor Interface when the look-up table is being modified.

DEVICE DESCRIPTION

The IMSG170 is intended for use as the output stage of raster scan video systems. It contains a high speed random access store of 256 x 18 bit words, three 6 bit high speed DAC's, a microprocessor interface and a pixel word mask.

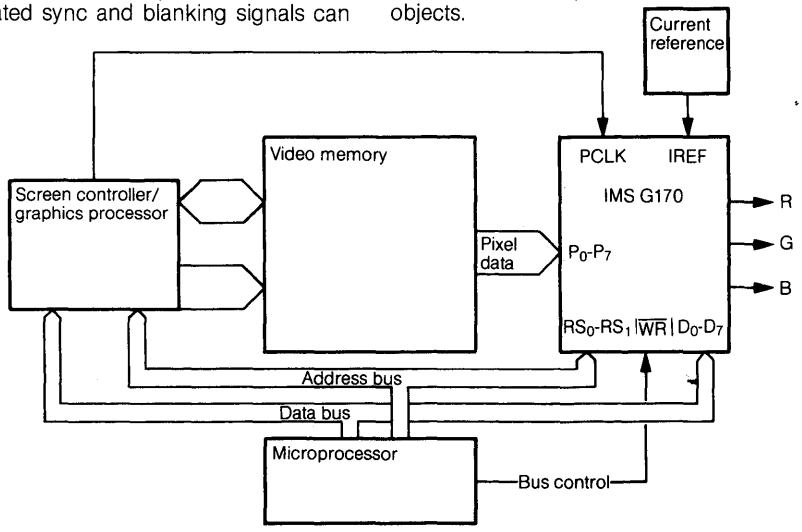
An 8 bit value read in on the Pixel Address input is used as a read address for the store and results in an 18 bit data word. This data is partitioned as three fields of 6 bits, with each field being applied to the inputs of a 6 bit DAC.

Pixel rates of up to 50 MHz are achieved by pipelining the memory access over two clock periods.

Externally generated sync and blanking signals can be input to the IMSG170, these signals act on all three of the analog outputs. The $\overline{SYNC}$ and $\overline{BLANK}$ signals are delayed internally by pipelining so that they appear at the analog outputs with the correct relationship to the pixel address stream.

The contents of the look up table can be modified via an 8 bit wide microprocessor interface. The use of an internal synchronizing circuit allows operations on the interface to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes of the effective contents of the Color Look-Up Table to facilitate such operations as animation and flashing objects.



VIDEO PATH

Pixel Address, $\overline{SYNC}$ and $\overline{BLANK}$ inputs are sampled on the rising edge of Pixel Clock and appear at the analog outputs after two further rising edges of Pixel Clock.

ANALOG OUTPUTS

The outputs of the DACs are intended to produce 1 volt peak white amplitude (i.e., 0.7 volts swing and 0.3 volts sync as specified by RS170A) when driving a 75 ohm load and when a 4.44 mA IREF is supplied.

The $\overline{BLANK}$ and $\overline{SYNC}$ inputs to the IMSG170 act on all three of the analog outputs. When the $\overline{BLANK}$ input is low a binary zero is applied to the inputs of the DACs. When the $\overline{SYNC}$ input is low an offset on the analog outputs of 30% of the full scale output current is removed. The $\overline{BLANK}$ and $\overline{SYNC}$ inputs can be operated independently of each other.

The expressions for peak white voltage/output loading combinations are given below:

1) Composite sync ($\overline{SYNC}$ going low to generate sync pulses on the analog outputs)

$$\text{V peak white} = \frac{\text{IREF} \times 90 \times \text{Rload}}{30}$$

$$\text{V black level} = \frac{\text{IREF} \times 27 \times \text{Rload}}{30}$$

2) Separate sync ($\overline{SYNC}$ continuously low)

$$\text{V peak white} = \frac{\text{IREF} \times 63 \times \text{Rload}}{30}$$

V black level = 0

MICROPROCESSOR INTERFACE

There are three internal registers in the IMSG170. These are:

RS1	RS0	Register
0	0	Pixel Address
0	1	Color Value
1	0	Pixel Mask

The Pixel Address register is used to specify the location in the look-up table to be written with a color value. The Color Value register contains the data used to update the contents of the location specified by the Pixel Address register. The Pixel Mask register is an 8 bit register. The value in the mask register is bitwise ANDed with the incoming pixel address to give a masked pixel address.

The microprocessor interface is asynchronous with the video path, the timing of operations on the interface registers being controlled by the Write Enable signal ($\overline{WR}$). On the falling edge of this signal the register select lines are sampled, and on the rising edge the values on the data bus are sampled. To allow for the internal synchronization of the written data with the video path, Write Enable must be high for at least three Pixel Clock cycles between write operations. Each time a new color value is written to the Look-Up Table to modify its contents the write cycle will replace the color value read cycle for one pixel.

To write a new color value to the table a pixel address must be specified and then an 18 bit data word written to that location in the Table.

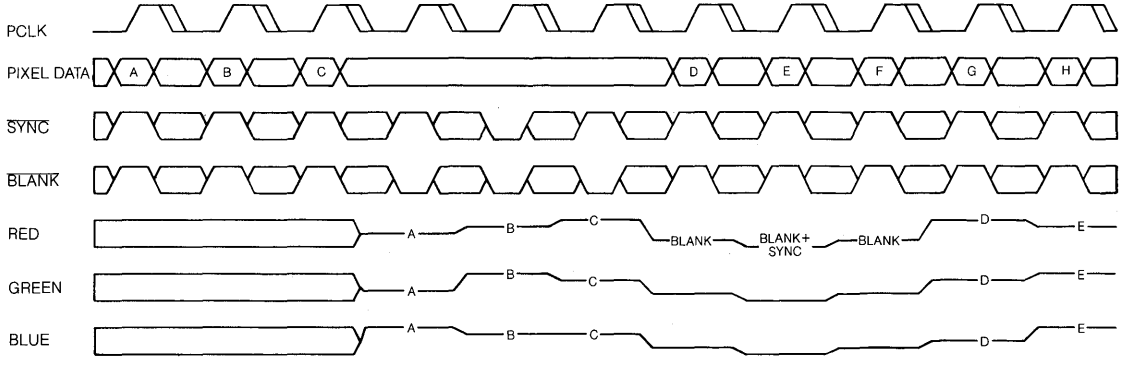
Locations in the Look-Up Table can be specified in two ways. The first is to write a pixel address and then perform a color value write sequence. The second method is to write an initial pixel address and then (as the Pixel Address register increments after every color value write sequence) write a succession of new color values for the range of pixel addresses to be written.

A color value write sequence is three successive byte writes to the Color Value register. The least significant 6 bits are taken from each byte written and concatenated into an 18 bit word. The first byte written will define the red intensity, the second the green and the last the blue.

The pixel address used to access the Color Look-Up Table is the result of the bitwise ANDing of the incoming pixel address and contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colors without altering the video memory or the look-up table contents. Thus, by partitioning the color definitions by one or more bits in the pixel address rapid animation and flashing objects can be produced.

In the event that the Pixel Address register is modified during a color value write sequence the Color Value register is initialized, aborting any unfinished write sequence.

The Pixel Mask register is independent of the Pixel Address and Color Value registers.



ABSOLUTE MAXIMUM RATINGS[a]

Voltage on V_{CC} 7.0V
Voltage on Other Pin . . . . . V_{SS} −0.5V to V_{CC} +0.5V
Temperature Under Bias . . . . . −40°C to 85°C
Storage Temperature (Ambient) . . . . −65°C to 150°C
Power Dissipation 1W
Reference Current . . . . . −15mA
Analog Output Current (Per Output) 45mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS[a]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	Volts	
V_{SS}	Ground		0		Volts	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC} +0.5	Volts	
V_{IL}	Input Logic "0" Voltage	−0.5		0.8	Volts	−2.0 V min for 20 ns pulse width
T_A	Ambient Operating Temperature	0		70	°C	

DC ELECTRICAL CHARACTERISTICS[a, b] (0°C ≤ T_A ≤ +70°C) (V_{CC} = 5.0V ± 10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	Average Power Supply Current		150	mA	c
IREF	Reference Current	−1.5	−7	mA	d
V_O max	Maximum Output Voltage	2		V	e, $I_O \leq$ 10mA
I_O max	Maximum Output Current	21		mA	e, $V_O \leq$ 1V
	Full Scale Accuracy	±5		%	e
	Sync Accuracy	29	31	%	g
	Differential Accuracy	±1		%	h
	Linearity	±0.5		LSB	i

AC TEST CONDITIONS

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 2.5ns
Input Timing Reference Level 1.5V

AC ELECTRICAL CHARACTERISTICS[a]

(0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ± 10%)

PARAMETER	MIN	MAX	UNITS	NOTES
Rise Time (10% to 90%)		8	ns	j
Full Scale Settling Time		20	ns	j,k,f
Glitch Energy		400	pVsec	f

Note a: All voltages in this data sheet are with respect to V_{SS} unless specified otherwise.
Note b: The Pixel Clock frequency must be stable for a period of at least 20μS after power-up (or after a change in Pixel Clock frequency) before proper device operation is achieved.
Note c: Pixel Clock frequency = 50 MHz. Io = Io (max)
Note d: Reference currents below the minimum specified may cause the analog outputs to become invalid.
Note e: $\overline{SYNC} \geq V_{IH}$ (min).
Note f: This parameter is sampled, not 100% tested.
Note g: Sync current is nominally 30% of peak white current.
Note h: Between different analog outputs on the same device.
Note i: Monotonicity guaranteed.
Note j: Load = 75 Ω + 30 pF.
Note k: To within 1% of full scale voltage.

NOTE: device characterization is underway. The values given here represent a design goal and are subject to change.

Note: device characterization is underway. The values given here represent a design goal and are subject to change.

Video

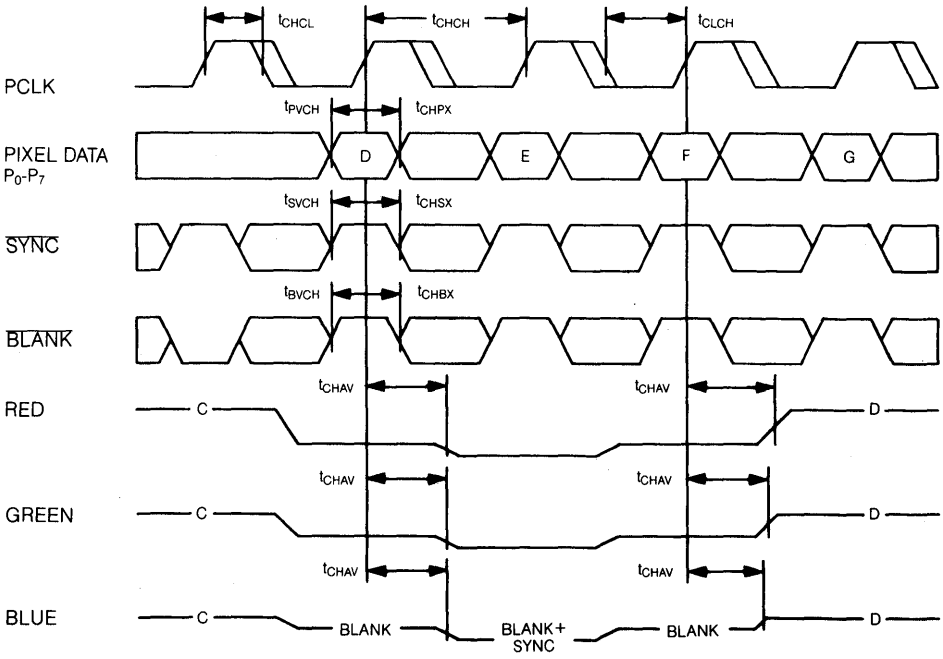
VIDEO OPERATION

AC OPERATING CONDITIONS: V_{CC} = +5.0V ± 10%, 0°C ≤ T_A ≤ 70°C[b]

SYMBOL	PARAMETER	IMSG170-50		IMSG170-35		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{CHCH}	PCLK Period	20	10000	28	10000	ns	
Δt_{CHCH}	PCLK Jitter		±2.5		±2.5	%	n
t_{CLCH}	PCLK Width Low	6	10000	9	10000	ns	
t_{CHCL}	PCLK Width High	6	10000	9	10000	ns	
t_{PVCH}	Pixel Word Setup Time	3		4		ns	
t_{CHPX}	Pixel Word Hold Time	3		4		ns	
t_{SVCH}	$\overline{SYNC}$ Setup Time	3		4		ns	
t_{BVCH}	$\overline{BLANK}$ Setup Time	3		4		ns	
t_{CHSX}	$\overline{SYNC}$ Hold Time	3		4		ns	
t_{CHBX}	$\overline{BLANK}$ Hold Time	3		4		ns	
t_{CHAV}	PCLK to Valid DAC Output	15	30	15	45	ns	o
Δt_{CHAV}	Differential Output Delay		1		1	ns	p
	Pixel Clock Transition Time		50		50	ns	

Note n: This parameter for allowed variation in the Pixel Clock frequency does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (t_{CHCH}) period specified above.
Note o: A valid analog output is defined as when the changing analog signal is half way between its successive values.
Note p: Between different analog outputs on the same device.

VIDEO TIMING



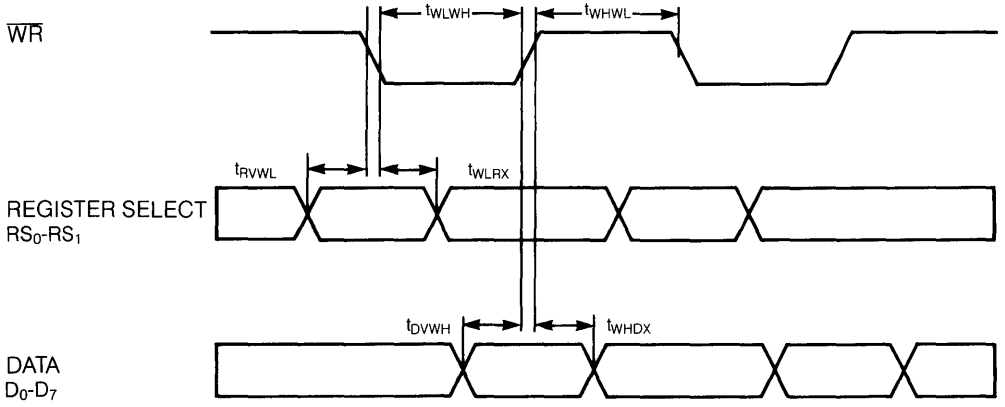
MICROPROCESSOR INTERFACE: WRITE CYCLE TIMING

AC OPERATING CONDITIONS: V_{CC} = +5.0V ± 10%, 0°C ≤ T_A ≤ 70°C

SYMBOL	PARAMETER	IMSG170-50		IMSG170-35		UNITS	NOTES
		MIN	MAX	MIN	MAX		
t_{WLWH}	$\overline{WR}$ Pulse Width Low	50		50		ns	
t_{WHWL}	$\overline{WR}$ Pulse Width High	3*t_{CHCH}		3*t_{CHCH}		ns	m
t_{RVWL}	Register Select Setup Time	10		15		ns	
t_{WLRX}	Register Select Hold Time	10		15		ns	
t_{DVWH}	Data Setup Time	10		15		ns	
t_{WHDX}	Data Hold Time	10		15		ns	
	Write Enable Transition Time		50		50	ns	

Notes: m The parameter t_{WHWL} allows for the write data to be synchronized with the pixel clock, hence this parameter is expressed in terms of the pixel clock period t_{CHCH}.

WRITE CYCLE TIMING



Note: device charaterization is underway. The values given here represent a design goal and are subject to change.

APPLICATION

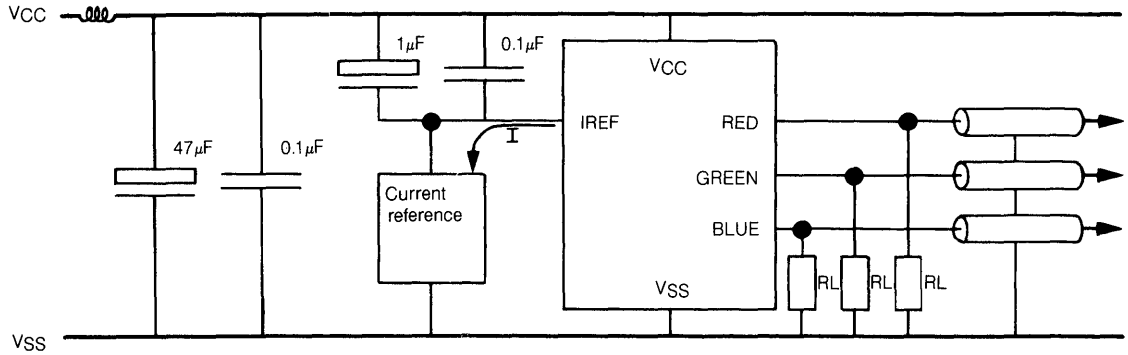
The IMSG170 has no on chip power supply rejection to analog outputs. To ensure proper operation in a system environment it is recommended that the following guidelines are followed.

POWER DISTRIBUTION

Transient currents are required by high speed CMOS circuitry such as the IMSG170. These transient current spikes can cause significant power supply and ground noise unless adequate power distribution and decoupling is used. The recommended power distribution scheme combines proper layout and placement of decoupling capacitors. A ground plane and locally isolated V_{CC} supply, as shown below, will help to minimize V_{CC} noise generated by external circuitry. A high frequency decoupling capacitor with value of 0.1μF and a larger tantalum capacitor with a value of 47μF should be placed in parallel between V_{CC} and V_{SS} as close as possible to the device.

CURRENT REFERENCE

The current reference (IREF) input to the IMSG170 provides an onboard voltage reference by sourcing a current from the V_{CC} supply. To prevent noise modulating the analog outputs the current reference should be as stable as possible and decoupled to V_{CC}. To minimize cross-talk onto IREF the current source should be sited as close as possible to the IMSG170 and a ground plane should be used.



Transputer Products 5

Transputer Selection Guide

Device	Processor Wordlength (bits)	Onchip RAM (Kbytes)	Number of Links	Speed Selection (MHz)	Power Supply (Volts)	Number of Pins	Package Type	Process	Page No.
IMS T414C IMS T414G	32 32	2 2	4 4	12,15,20 12,15,20	+5 +5	84 84	C G	CMOS CMOS	5-3 5-3
IMS T212C IMS T212G	16 16	2 2	4 4	12,15,20 12,15,20	+5 +5	68 68	C G	CMOS CMOS	5-19 5-19
IMS C001P IMS C002P	Link Adapter Link Adapter	Link Adapter Link Adapter	1 1	10 10	+5 +5	28 24	S S	CMOS CMOS	5-31 5-35

NOTES:
C = J-lead Ceramic Chip Carrier
G = Ceramic Pin Grid Array
S = Ceramic DIP
P = Plastic DIP

Transputer Evaluation Board Selection Guide

Part Number	Processor	Onboard Memory (bytes)	Number of Links	Connection	Power Supply (Volts)	Physical Dimensions	Page No.
IMS B001-1	T414A-12	64K(SRAM)	4	2xRS232	+5	Double Extended Eurocard	5-39
IMS B002-1 IMS B002-2	T414A-12 T414A-12	1M(DRAM) 2M(DRAM)	4 4	2xRS232 2xRS232	+5 +5	Double Extended Eurocard Double Extended Eurocard	5-43 5-43
IMS B004-1 IMS B004-2	T414A-12 T414A-12	1M(DRAM) 2M(DRAM)	4 4	IBM PC BUS IBM PC BUS	– –	PC Plug in Card PC Plug in Card	5-47 5-47

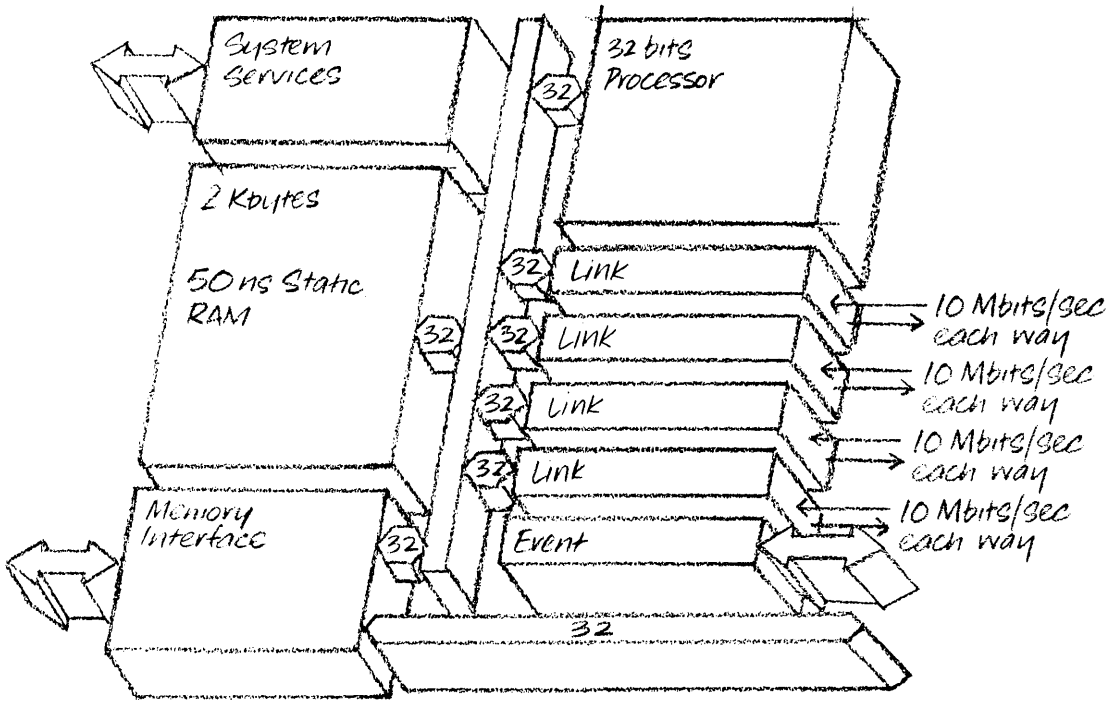
Software Selection Guide

Part Number	Description	Host Machine	Target System	Format	Page No.
IMS D100 IMS D600 IMS D700	Transputer Development System Transputer Development System Transputer Development System	Stride 440 VAX/VMS IBM PC (XT or AT)	Transputers Transputers Transputers	Floppy Disks 1600 bpi Mag Tape Floppy Disks	5-51 5-55 5-59
IMS S001 IMS P600	Portakit Occam Programming System	Any VAX/VMS	Any VAX Code	1600 bpi Mag Tape 1600 bpi Mag Tape	5-63 5-63

IMS T414 transputer

Features

- 32 bit 10 MIPS processor
- 4 Gigabyte linear address space
- 32 bit wide 25 MByte/sec memory interface
- Configurable on-chip memory controller
- 2K bytes high speed on chip RAM
- 4 inter-transputer links, each with full duplex DMA transfer capability at 10 Mbits/sec
- Advanced 1.5 micron CMOS technology
- Low power dissipation (less than 500mW)


System Services
32 bits Processor
32
2 Kbytes
50 ns Static RAM
32
32
Link
32
Link
32
Link
32
Link
10 Mbits/sec each way
10 Mbits/sec each way
10 Mbits/sec each way
10 Mbits/sec each way
Memory Interface
32
Event
32

IMS T414	32 bit transputer providing 10 MIPS (millions of instructions per second) processing power with memory and communication capability, all on a single CMOS chip in an 84 pin package. Totally compatible at program and interface level with all transputer products.
Processor	Reduced instruction set for compact programs, efficient high level language implementation and direct support for the occam model of concurrency. Sub–microsecond procedure call, process switching and interrupt latency. High performance arithmetic with direct support for floating point operations.
Memory	2K bytes of static memory giving a maximum data rate of 80 Mbytes/s. Multiport access for processor and each link.
Memory interface	Provides direct address space up to 4 Gbytes with a maximum data rate of 25 MBytes/s. 32 bits wide with mutiplexed data and address. Configurable memory controller provides all timing, control and DRAM refresh signals for a wide variety of mixed memory systems.
Peripheral interface	Memory controller supports memory mapped peripherals, including DMA. Links may be interfaced to byte wide peripherals via an INMOS Link Adapter. Peripheral can request attention via the Event input.
Links	Four INMOS standard 10 Mbits/sec, full duplex, serial links providing concurrent message passing capability to other transputer devices. DMA block transfer capability provided on each link.
Technology	200 000 devices fabricated in an advanced 1.5 micron twin tub CMOS process with polycide gates and interconnect.
Engineering	High frequency on chip clocks are generated from a single TTL level 5 MHz clock input. Memory and communications timing are derived from this clock. Communications are independent of the phase of the clock input so that interconnected transputers may use separate or common clocks without regard to timing skews.
Programming	Designed for efficient execution of high level languages. Languages provided by INMOS include C, Pascal, Fortran and occam. Programming in occam provides maximum performance and allows exploitation of concurrency. Interactive program development using occam as the lowest level image of the system.

The processor is designed to execute high level languages efficiently, and will normally be programmed using occam or an industry standard language such as C, Fortran or Pascal.

Concurrent processing

The processor shares its time between any number of concurrent processes. A process which is waiting for communication or a timeout does not consume any processor time.

Priority processes

The T414 supports two levels of priority – in occam notation, a **PRI PAR** (priority parallel) process may have two components. The priority 1 (low priority) processes are executed whenever there are no active priority 0 (high priority) processes.

Priority 0 processes are expected to execute for a short time. Priority 1 processes are periodically timesliced to provide an even distribution of processor time between computationally intensive tasks.

Interrupt latency

If a priority 0 process is waiting for an external channel to become ready, and if there are no active priority 0 processes, then the interrupt latency (from when the channel becomes ready to when the process starts executing) is typically 12 processor cycles, maximum 58 cycles (assuming use of on chip RAM).

Time

The processor includes timers for both high and low priority processes.

Error handling

High–level language execution is made secure with array bounds checking, arithmetic overflow detection etc. A flag is set when an error is detected. The error can be handled internally by software or externally by sensing the error pin. System state is preserved for subsequent analysis.

Performance

The performance of the transputer is measured in terms of the number of bytes to hold the program, and the number of internal processor cycles to execute it. The number of internal processor cycles per microsecond is given in the transputer designation, e.g., the IMS T414–20 executes 20 processor cycles per microsecond.

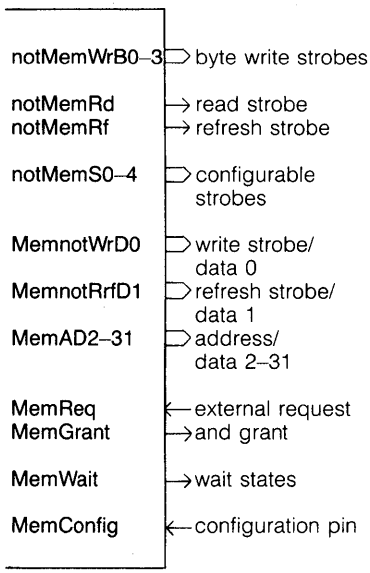
All timings are averages. The time taken to execute a program is given by the sum of the times to execute the individual program elements.

External memory

Extra processor cycles may be needed when program and/or data are held in external memory, depending both on the operation being performed, and on the speed of the external memory. The number of extra processor cycles required for each memory access is denoted as **e**. The value of **e** is 2 for the fastest external memory, and values of **e** for the pre–configured memory systems are given later.

If the program is stored in external memory, and **e** >= 4, then the number of extra cycles required for program execution may be estimated at (**e** – 3) / 4.

		Size *bytes*	**Time** *cycles*	**Data off chip** *cycles*
Arithmetic operators	+, –	1	1	
	* (multiplication)	2	39	
	/ (division)	2	40	
	\ (remainder)	2	38	
Comparison operators	= constant	0	1	
	>, =, <>, <, <=, >=	2	3	
Logical operators	AND	1	2	
	OR	4	8	
	/\, \/, ><(xor), ~	2	2	
Shift operators	<<n, >>n	2	3+n	
Expression evaluation	constant	1.3	1.3	
	variable	1.1	2.1	e
	error check	4	6	
	expression as subscript	1.3	1.3	
Constructs	SEQ	0	0	
	IF n components	1.3+3n	1.4+4.3n	en
	ALT n components	8+10.2n	31+19.7n	(2e–2)n+(10e–8)
	PAR n components	4+7.5n	30.5n–11	3en+4
	WHILE	4	12	
	SEQ i = 0 FOR n	7.3	15n–4	(4e–2)n
	PAR i = 0 FOR n	39	71n–6	16en–12
Procedure call	n parameters	1.4+1.1n	15.4+1.1n	en
Primitives	assignment to variable	1.1	1.1	e
	n word array assignment	4.2	2n+4	2en
	channel input and output	3.6	28.5	e
	n word array communication	2.1	n+21	en



The memory interface uses a 32–bit wide address/data bus and its controller may be configured, on reset, to suit a wide variety of different memory systems. One of 13 preset configurations may be selected or the configuration may be supplied externally.

The T414 memory interface cycle has six states, referred to as 'Tstates'. The duration of each Tstate is chosen to suit the memory used.

Tstate

T1	address setup time before address valid strobe
T2	address hold time after address valid strobe
T3	read cycle tristate/write cycle data setup
T4	read or write data
T5	read or write data
T6	end tristate/data hold

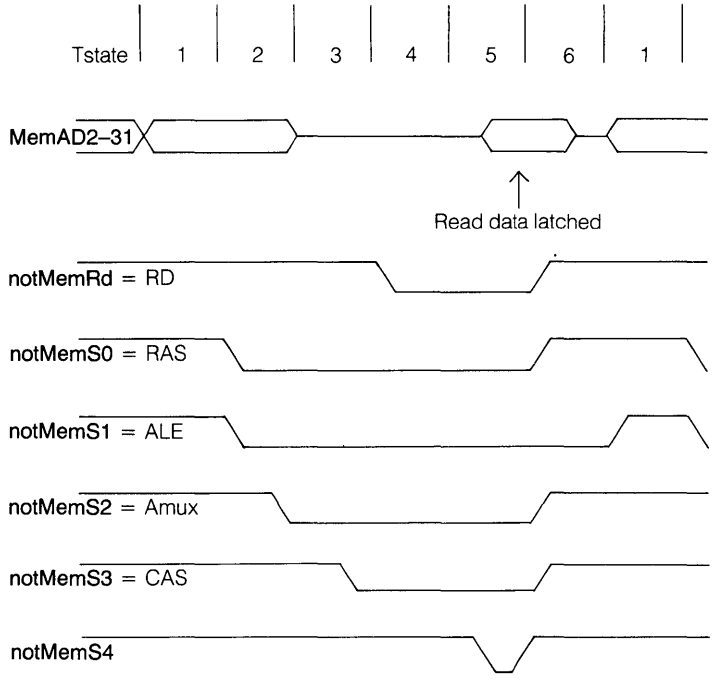
Each Tstate is configured to have a duration of one to four periods **Tm**. One period **Tm** is half the processor cycle time. In addition, **T4** may be extended by wait states.

The use of the strobes **notMemS0** to **notMemS4** will depend upon the memory system. The durations of the signals on each of **notMemS1** to **notMemS4** are denoted respectively as **s1** to **s4**, and are configurable to be between 0 and 31 periods **Tm**.

Signal	Starts	Ends
notMemS0	T2	T6
notMemS1	T2	T2+(Tm*s1)
notMemS2	T2+(Tm*s2)	T6
notMemS3	T2+(Tm*s3)	T6
notMemS4	T2+(Tm*s4)	T6

Read cycles

Read cycles generate **notMemS0** to **notMemS4** and **notMemRd** signals. Input data is latched at the end of T5. Byte reads are performed as word reads, with byte selection performed inside the processor.



Read cycle for dynamic RAM

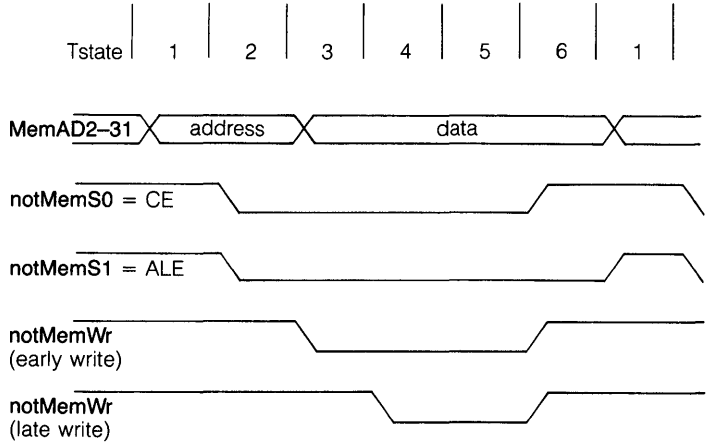
Write cycles

Write cycles generate **notMemS0** to **notMemS4** and the **notMemWrB** write data strobe signals. Separate **notMemWrB** signals are provided for each byte. A word write uses all the **notMemWrB** signals; if a particular byte is not to be written the relevant **notMemWrB** signal is not generated, and the corresponding data outputs are tristated.

Early indication of a write cycle is provided by a low signal on **MemnotWrD0** while the address is valid.

Write cycles may be configured to be either early or late. In late write cycles, write data is valid before the leading edge of **notMemWrB**, and held valid until after the trailing edge of **notMemWrB**.

Early write cycles provide a wide **notMemWrB** pulse, with data valid at the trailing edge of **notMemWrB**.



Write cycles, early and late

Refresh

Refresh can be configured to be enabled or disabled. If Refresh is enabled, the interval between refresh cycles can be configured to be 18, 36, 54 or 72 periods of the input clock signal **ClockIn**.

Refresh cycles generate all the strobes **notMemS1** to **notMemS4**, but neither **notMemRd** nor the **notMemWrB** signals. **notMemRf** goes low during **T1** and remains low until the end of **T6**. Refresh is also indicated by **MemnotRfD1** going low during **T1** and **T2** with the same timing as address signals.

A refresh cycle outputs a 10 Mbits/sec refresh address, on **MemAD2–10**. It is decremented after each refresh cycle. The remaining address bits are held high during a refresh cycle.

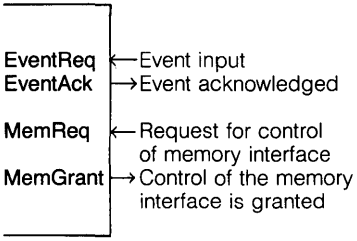
Wait states

An interface cycle may be extended by holding the **MemWait** input high. This may be done by connecting **MemWait** to one of the configurable strobes, **notMemS1** to **notMemS4**, or to an external signal.

Memory interface initialisation

An external configuration may be loaded from a PAL or ROM, or one of the following internal settings may be selected. A program is provided with the transputer development system to assist the verification of the actual interface timings for a particular configuration.

Purpose	**Duration of each Tstate** periods Tm						**Strobe duration**				**Write cycle** type	**Refresh interval** input clocks	**Cycle time** proc cycles	**Extra cycles** e
	T1	T2	T3	T4	T5	T6	s1	s2	s3	s4				
Byte	1	1	1	1	1	1	30	1	3	5	late	72	3	2
wide	1	2	1	1	1	2	30	1	2	7	late	72	4	3
dynamic	1	2	1	1	2	3	30	1	2	7	late	72	5	4
RAM	2	3	1	1	2	3	30	1	3	8	late	72	6	5
Multiplexed	1	1	1	1	1	1	3	1	2	3	early	72	3	2
address	1	1	2	1	2	1	5	1	2	3	early	72	4	3
dynamic	2	1	2	1	3	1	6	1	2	3	early	72	5	4
RAM	2	2	2	1	3	2	7	1	3	4	early	72	6	5
Static	1	1	1	1	1	1	30	1	2	3	early	–	3	2
RAM	1	1	2	1	2	1	30	2	5	9	early	–	4	3
General	2	2	2	2	4	2	30	2	3	8	late	72	7	6
purpose	3	3	3	3	3	3	30	2	4	13	late	72	9	8
Slowest	4	4	4	4	4	4	31	31	31	31	late	72	12	11



An interrupt request from a peripheral may be signalled via the **EventReq** pin, which is handshaken using **EventAck**. This will normally be used to trigger a high priority process. The request appears to the process as an input on a hardware channel.

Peripheral controllers may access the whole of the external memory address space for DMA transfers, using the transputer signals **MemReq** and **MemGrant**. The processor and links can continue operating to internal memory while DMA proceeds to external memory.

Byte wide peripherals can be interfaced to the links using Link Adapters.

T414 timer

At the standard **ClockIn** cycle rate of 5 MHz, the timer has a resolution of one microsecond.

Floating point operations

Floating point operations are provided by a run–time package. Typical floating point operations require approximately 240 processor cycles.

Standard arithmetic procedures

The T414 transputer provides a number of special purpose instructions to support multiple length and floating point arithmetic. A library of predefined procedures is provided to access these instructions.

Reset and Analyse

On reset, the T414 configures the memory interface, generating refresh cycles to initialize dynamic RAM. All state information is lost, and the transputer commences to bootstrap itself.

The T414 is analysed by taking and holding the **Analyse** pin high, then pulsing the **Reset** pin, then taking the **Analyse** pin low. The effect is to stop operation in a way which preserves much of the internal state, and then to bootstrap. The memory interface is not reconfigured, and refresh cycles continue, preserving the contents of dynamic RAM. The T414 can be bootsrapped with software to aid in debugging a failed program.

Suitable bootstrap and analysis software is provided as part of the transputer development system.

Bootstrap

The T414 can be bootstrapped either from a link, or by executing code in external ROM. If the **BootFromROM** pin is low the processor waits for the first message to arrive on any link, and interprets it as a bootstrap program to be read into memory and executed.

Link speed selection

The speed of the links is directly proportional to the frequency supplied on the **ClockIn** signal. The universal speed for all transputer products is twice **ClockIn**, i.e., 10 MBits/sec. The T414 also supports a slower speed equal to the **ClockIn** (5MHz). This option is selected for link 0 by holding the **Link0Special** pin high, and for the other links by holding the **Link123Special** pin high.

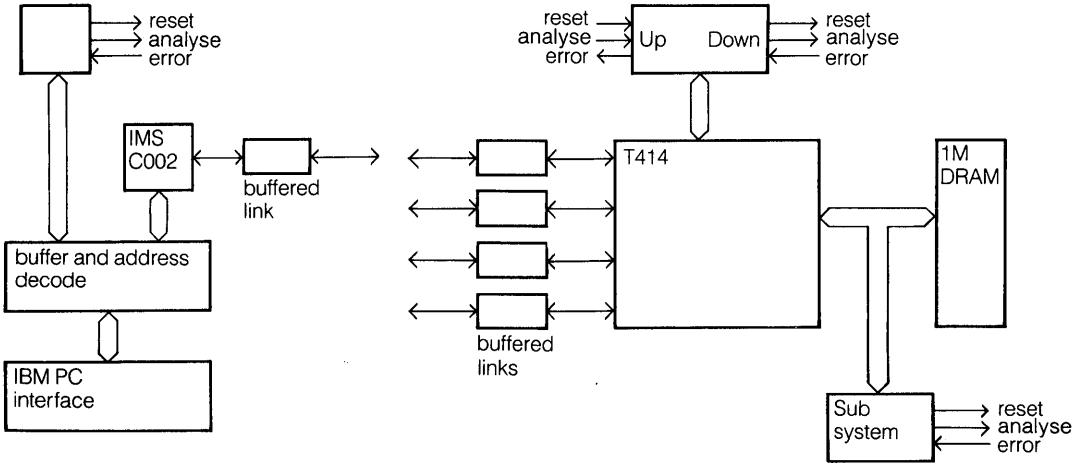
The transputer is a high performance component when used in single transputer configurations. The separation of the communications system from the memory interface enables both interfaces to be optimised for their individual functions. In particular, the T414 is readily interfaced to current day systems by means of a Link Adaptor, without compromising the flexibility or efficiency of its external memory interface.

IBM PC add–in board

This typical configuration can be the basis for a performance accelerator for the popular IBM Personal Computer. A single add–in board holds two modules. One is a T414 with a megabyte of memory and four buffered links. The other is an interface connecting a single buffered link to the PC. Both modules provide Reset, Analyse and Error signals (system services).

The buffered links enable the board to be connected to other transputer boards, in networks of arbitrary size. A small amount of logic around the system services enables the board to act as a master or as a daisy chained slave in the network.

The two modules on the board are connected via the links and the system services.

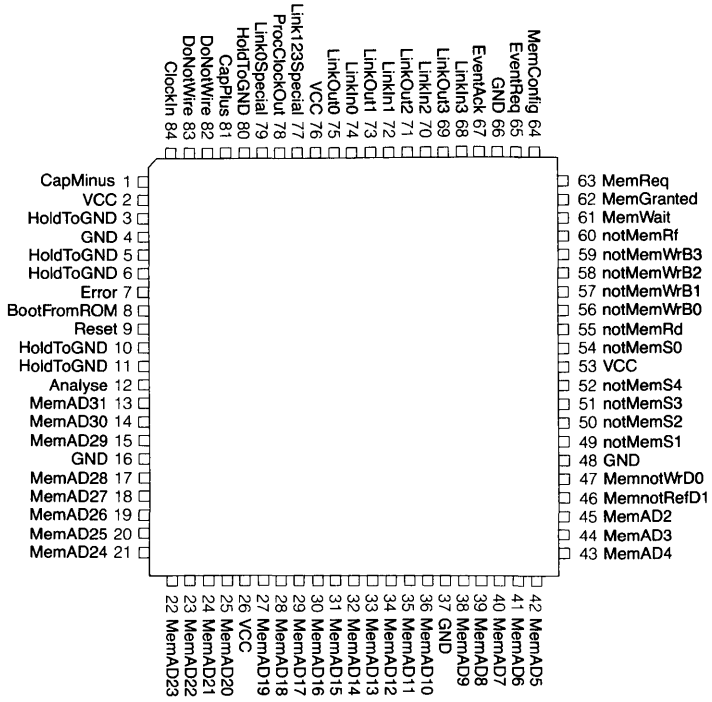


The following tables give the target parameters for the T414 transputer.

	Parameter		Conditions	Min	Max	Unit
Absolute maximum ratings	VCC	DC supply voltage		0	7.0	V
	VI,VO	Input or output voltage on any pin		–0.5	VCC+0.5	V
	TS	Storage temperature		–65	150	degC
	TA	Ambient temperature under bias		–55	125	degC
	PD	Power dissipation rating			2	W
Recommended operating conditions	VCC	DC supply voltage		4.5	5.5	V
	VI,VO	Input or output voltage		0	VCC	V
	IO	Output current drawn from pin			+– 25	mA
	TA	Operating temperature range		0	70	degC
DC characteristics			4.5 V < VCC < 5.5 V 0 degC < TA < 70 degC input clock frequency = 5 MHz All voltages are with respect to GND			
	VIH	High level input voltage		2.0	VCC+0.5	V
	VIL	Low level input voltage		–0.5	0.8	V
	II	Input current	GND < VI< VCC		+–200	uA
	VOH	Output high voltage	IOH = 2mA	VCC–1		V
	VOL	Output low voltage	IOL = 4mA		0.4	V
	IOZ	Tristate output current	GND < VI < VCC		+–200	uA
	PD	Power dissipation			0.9	W

The T414 is available in an 84 pin J–lead ceramic chip carrier.

84 pin J–lead chip carrier

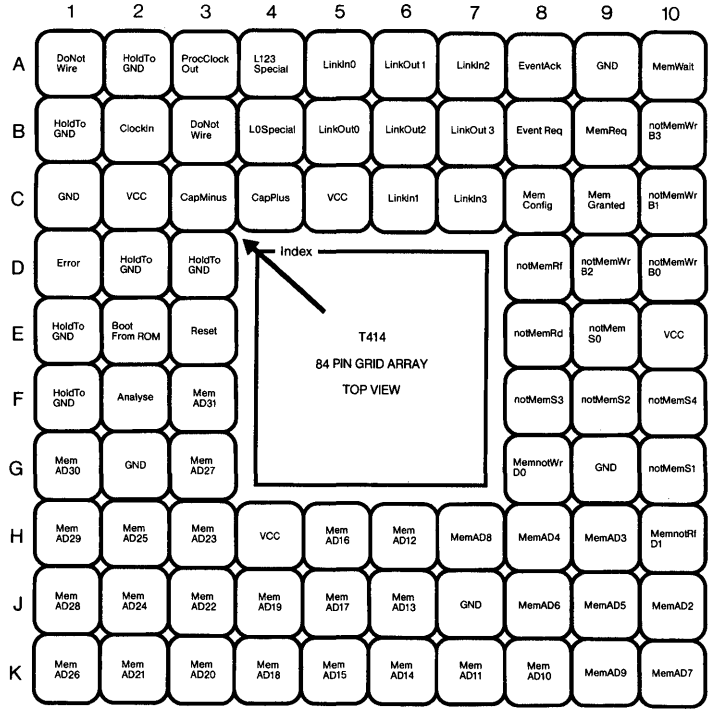


T414 speed selections

The T414 is produced in various speed selections. Inclusion of a speed selection in the table does not imply immediate availability.

Product parameters			Part number
Instruction throughput	Processor cycle time	Input clock frequency	
6 MIPS	80 ns	5 MHz	IMS T414-12
7.5 MIPS	67 ns	5 MHz	IMS T414-15
10 MIPS	50 ns	5 MHz	IMS T414-20

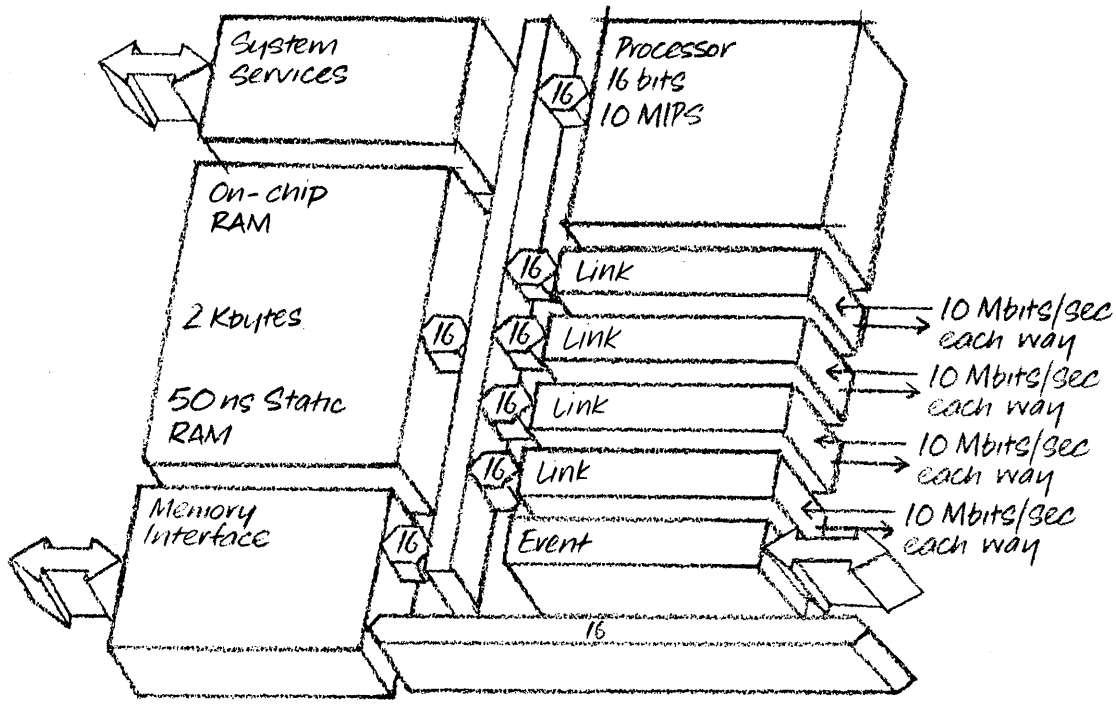
84 pin grid array



IMS T212 transputer

Features

- 16 bit 10 MIPS processor
- Non multiplexed 20 MByte/sec interface
- 2K bytes high speed on chip RAM
- 4 inter-transputer links, each with full duplex DMA transfer capability at 10 Mbits/sec
- Advanced 1.5 micron CMOS technology
- Low power dissipation (less than 400mW)


System
Services
Processor
16 bits
10 MIPS
16
On-chip
RAM
2 Kbytes
50 ns Static
RAM
16
Link
16
Link
16
Link
16
Link
Memory
Interface
16
Event
16
10 Mbits/sec
each way
10 Mbits/sec
each way
10 Mbits/sec
each way
10 Mbits/sec
each way

IMS T212	16 bit transputer providing 10 MIPS (millions of instructions per second) processing power with memory and communication capability, all on a single CMOS chip in an 68 pin package. Totally compatible at program and interface level with all transputer products.
Processor	Reduced instruction set for compact programs, efficient high level language implementation and direct support for the occam model of concurrency. Sub–microsecond procedure call, process switching and interrupt latency. High performance arithmetic with direct support for floating point operations.
Memory	2K bytes of static memory giving a maximum data rate of 40 Mbytes/s. Multiport access for processor and each link.
Memory interface	Provides direct address space up to 64 Kbytes with a maximum data rate of 20 MBytes/s. 16 bits data and 16 bits address non–multiplexed. Optimized for fast static RAM, word organized or byte organized.
Peripheral interface	Memory interface supports memory mapped peripherals. Links may be interfaced to byte wide peripherals via an INMOS Link Adapter. Peripheral can request attention via the Event input.
Links	Four INMOS standard 10 Mbits/sec, full duplex, serial links providing concurrent message passing capability to other transputer devices. DMA block transfer capability provided on each link.
Technology	200 000 devices fabricated in an advanced 1.5 micron twin tub CMOS process with polycide gates and interconnect.
Engineering	High frequency on chip clocks are generated from a single TTL level 5 MHz clock input. Memory and communications timing are derived from this clock. Communications are independent of the phase of the clock input so that interconnected transputers may use separate or common clocks without regard to timing skews.
Programming	Designed for efficient execution of high level languages. Languages provided by INMOS include C, Pascal, Fortran and occam. Programming in occam provides maximum performance and allows exploitation of concurrency. Interactive program development using occam as the lowest level image of the system.

The processor is designed to execute high level languages efficiently, and will normally be programmed using occam or an industry standard language such as C, Fortran or Pascal.

Concurrent processing

The processor shares its time between any number of concurrent processes. A process which is waiting for communication or a timeout does not consume any processor time.

Priority processes

The T212 supports two levels of priority – in occam notation, a **PRI PAR** (priority parallel) process may have two components. The priority 1 (low priority) processes are executed whenever there are no active priority 0 (high priority) processes.

Priority 0 processes are expected to execute for a short time. Priority 1 processes are periodically timesliced to provide an even distribution of processor time between computationally intensive tasks.

Interrupt latency

If a priority 0 process is waiting for an external channel to become ready, and if there are no active priority 0 processes, then the interrupt latency (from when the channel becomes ready to when the process starts executing) is typically 12 processor cycles, maximum 58 cycles (assuming use of on chip RAM).

Time

The processor includes timers for both high and low priority processes.

Error handling

High–level language execution is made secure with array bounds checking, arithmetic overflow detection etc. A flag is set when an error is detected. The error can be handled internally by software or externally by sensing the error pin. System state is preserved for subsequent analysis.

Performance

The performance of the transputer is measured in terms of the number of bytes to hold the program, and the number of internal processor cycles to execute it. The number of internal processor cycles per microsecond is given in the transputer designation, e.g., the IMS T212–20 executes 20 processor cycles per microsecond.

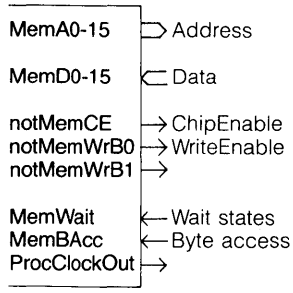
All timings are averages. The time taken to execute a program is given by the sum of the times to execute the individual program elements.

External memory

Extra processor cycles may be needed when program and/or data are held in external memory, depending both on the operation being performed. The figures given below assume no wait states and word organized memory, i.e., all off chip accesses are completed in two processor cycles.

The effect of storing program in external memory is a performance degradation of typically less than 10%

		Size *bytes*	**Time** *cycles*	**Data off chip** *cycles*
Arithmetic operators	+, -	1	1	
	* (multiplication)	2	23	
	/ (division)	2	24	
	\ (remainder)	2	22	
Comparison operators	= constant	0	1	
	>, =, <>, <, <=, >=	2	3	
Logical operators	AND	1	2	
	OR	4	8	
	/\, \/, ><(xor), ~	2	2	
Shift operators	<<n, >>n	2	3+n	
Expression evaluation	constant	1.3	1.3	
	variable	1.1	2.1	1
	error check	4	6	
	expression as subscript	1.3	1.3	
Constructs	SEQ	0	0	
	IF n'th branch	1.3+3n	1.4+4.3n	n
	ALT n components	8+10.2n	31+19.7n	10
	PAR n components	4+7.5n	30.5n–11	
	WHILE	4	12	
	SEQ i = 0 FOR n	7.3	15n–4	2n+2
	PAR i = 0 FOR n	39	71n–6	16n
Procedure call	n parameters	1.4+1.1n	15.4+1.1n	n
Primitives	assignment to variable	1.1	1.1	1
	n word array assignment	4.2	2n+4	2n
	channel input and output	3.6	28.5	1
	n word array communication	2.1	n+21	n

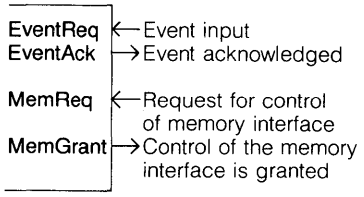


The memory interface consists of a 16 bit address bus and a 16 bit data bus. It performs word reads and word writes in 2 processor cycles. A processor cycle is identified by **ProcClockOut**.

The **MemWait** signal is sampled during the second half of the first processor cycle, and is defined with a setup and hold time after the falling edge of **ProcClockOut**. A wait state may last for any number of processor cycles.

The **MemBAcc** pin can be set at the start of a memory interface cycle to cause the memory interface to perform two byte access cycles. The timing allows **MemBAcc** to be derived directly from the address lines, so that it is generated when the byte organized memory or peripheral chip is accessed. **MemA0** is held low during the first byte access, and set high during the second byte access.

Peripheral interfacing

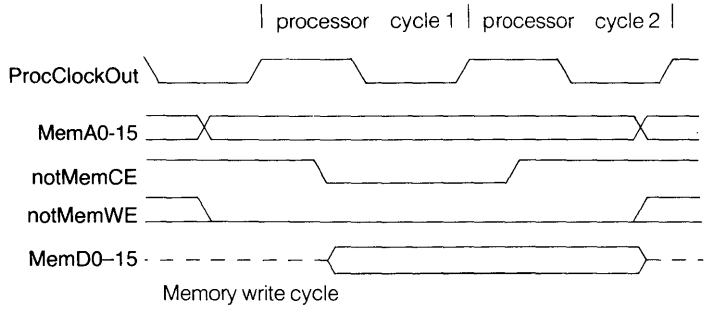


An interrupt request from a peripheral may be signalled via the **EventReq** pin, which is handshaken using **EventAck**. This will normally be used to trigger a high priority process. The request appears to the process as an input on a hardware channel.

Peripheral controllers may access the whole of the external memory address space for DMA transfers, using the transputer signals **MemReq** and **MemGrant**. The processor and links can continue operating to internal memory while DMA proceeds to external memory.

Byte wide peripherals can be interfaced to the links using Link Adapters.

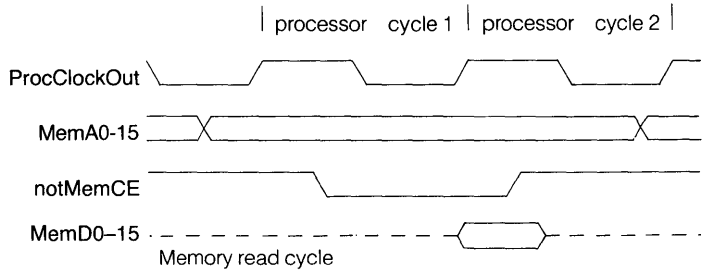
Read cycles



Memory write cycle

The address is valid at the falling edge of **notMemCE**, and the interface strobes the data from **MemD0–15** on the rising edge of **NotMemCE**.

Write cycles



Memory read cycle

The signal **notMemWE** is held low before the beginning of the cycle. The address is valid at the falling edge of **notMemCE**. The interface presents the data on **MemD0–15**, which is strobed on the rising edge of **notMemCE**.

T212 timer

At the standard **ClockIn** cycle rate of 5 MHz, the timer has a resolution of one microsecond. The timer for low priority processes has a resolution of 64 microseconds.

Standard arithmetic procedures

The T212 transputer provides a number of special purpose instructions to support multiple length and floating point arithmetic. A library of predefined procedures is provided to access these instructions.

Reset and Analyse

On reset, all state information is lost, and the transputer commences to bootstrap itself.

The T212 is analysed by taking and holding the **Analyse** pin high, then pulsing the **Reset** pin, then taking the **Analyse** pin low. The effect is to stop operation in a way which preserves much of the internal state, and then to bootstrap. The T212 can be bootsrapped with software to aid in debugging a failed program.

Suitable bootstrap and analysis software is provided as part of the transputer development system.

Bootstrap

The T212 can be bootstrapped either from a link, or by executing code in external ROM. If the **BootFromROM** pin is low the processor waits for the first message to arrive on any link, and interprets it as a bootstrap program to be read into memory and executed.

Link speed selection

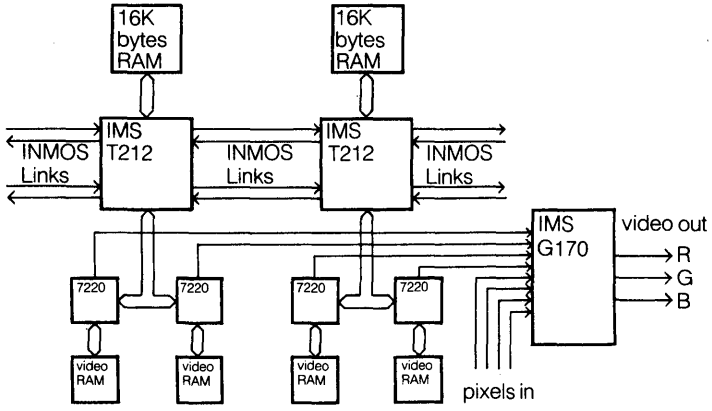
The speed of the links is directly proportional to the frequency supplied on the **ClockIn** signal. The universal speed for all transputer products is twice **ClockIn**, i.e., 10 MBits/sec. The T212 also supports a slower speed equal to the **Clockin** (5MHz). This option is selected for link 0 by holding the **Link0Special** pin high, and for the other links by holding the **Link123Special** pin high.

The transputer is a high performance component when used in single transputer configurations. The separation of the communications system from the memory interface enables both interfaces to be optimised for their individual functions. In particular, the T212 is readily interfaced to current day systems by means of a Link Adaptor, without compromising the performance of its external memory interface. It is ideally suited to applications requiring distributed control or array processing.

Animated graphics

This configuration provides an animated graphics capability on a double extended Eurocard. A system can comprise a single board, or boards may be ganged to provide higher resolution, more colours and higher performance. Each board contains two IMS T212 transputers. The transputers receive drawing commands and synchronize their operations via INMOS links.

Each transputer controls two 7220 graphics controllers providing two picture planes. The system is arranged so that each transputer provides either two bits per pixel, or two frames for animation. Whilst one frame is being displayed, the T212 is free to draw in the other. The animation is provided by a single write to the mask register of the IMS G170 colour lookup table to select the new frame.

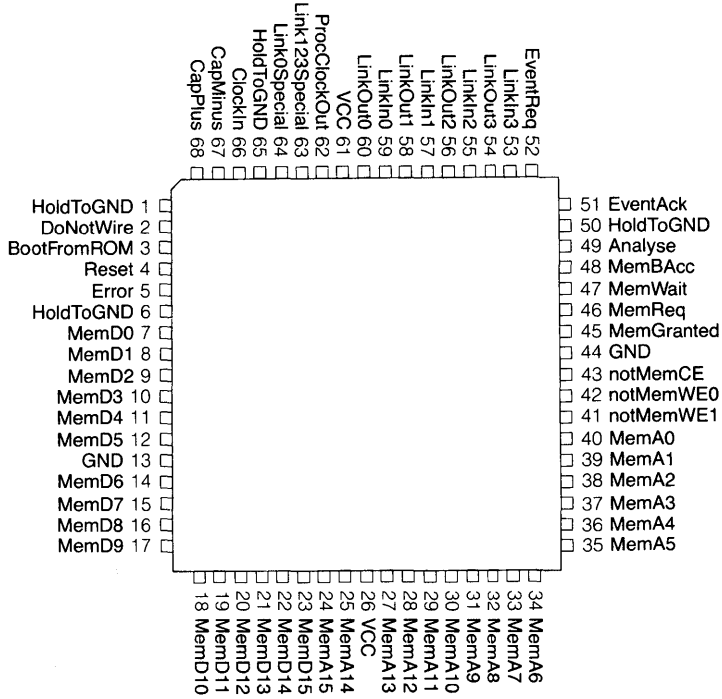


The following tables give the target parameters for the T212 transputer.

	Parameter		Conditions	Min	Max	Unit
Absolute maximum ratings	VCC	DC supply voltage		0	7.0	V
	VI,VO	Input or output voltage on any pin		–0.5	VCC+0.5	V
	TS	Storage temperature		–65	150	degC
	TA	Ambient temperature under bias		–55	125	degC
	PD	Power dissipation rating			2	W
Recommended operating conditions	VCC	DC supply voltage		4.5	5.5	V
	VI,VO	Input or output voltage		0	VCC	V
	IO	Output current drawn from pin			+– 25	mA
	TA	Operating temperature range		0	70	degC
DC characteristics			4.5 V < VCC < 5.5 V 0 degC < TA < 70 degC input clock frequency = 5 MHz All voltages are with respect to GND			
	VIH	High level input voltage		2.0	VCC+0.5	V
	VIL	Low level input voltage		–0.5	0.8	V
	II	Input current	GND < VI< VCC		+–200	uA
	VOH	Output high voltage	IOH = 2mA	VCC–1		V
	VOL	Output low voltage	IOL = 4mA		0.4	V
	IOZ	Tristate output current	GND < VI < VCC		+–200	uA
	PD	Power dissipation			0.7	W

The 212 is available in a 68 pin J-Lead chip carrier or a 68 pin grid array.

68 pin J-lead chip carrier



T212 speed selections

The T212 is produced in various speed selections. Inclusion of a speed selection in the table does not imply immediate availability.

Product parameters			Part number
Instruction throughput	Processor cycle time	Input clock frequency	
6 MIPS	80 ns	5 MHz	IMS T212-12
7.5 MIPS	67 ns	5 MHz	IMS T212-15
10 MIPS	50 ns	5 MHz	IMS T212-20

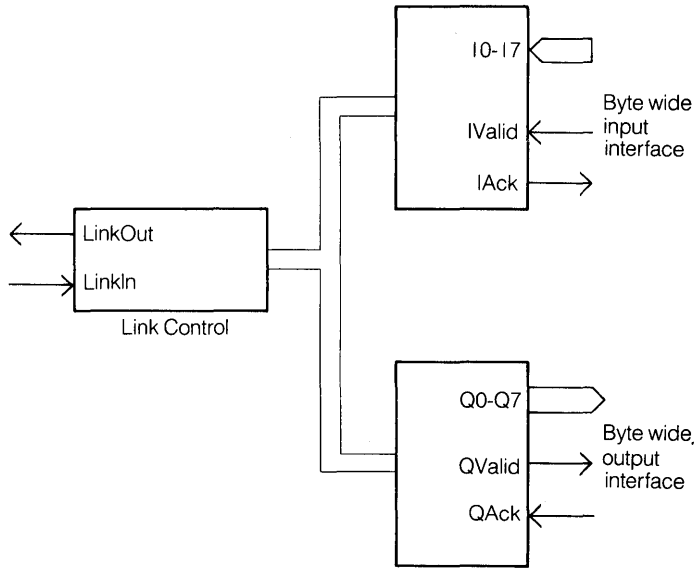
IMS C001 link adaptor

Features

- High performance system interconnect
- Two handshaken byte-wide interfaces
- INMOS serial link
- 10M bits/sec data rate
- Advanced 1.5 micron CMOS technology
- Standard 600 mil 28 pin DIP

Applications

- Programmable I/O pins for a transputer
- High performance handshaken serial link between microprocessor systems
- Link between transputers running at different clock frequencies



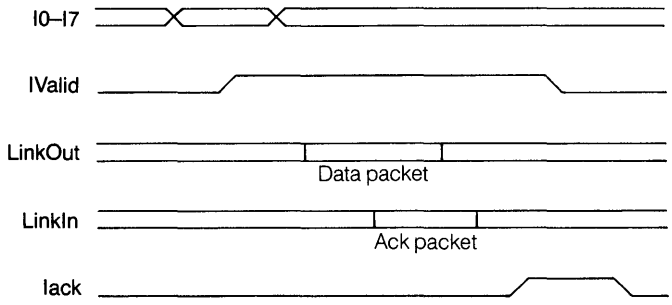
The IMS C001 link adaptor converts between an INMOS serial link and two fully handshaken byte–wide interfaces. One interface is for data coming from the serial link and one for data going to the serial link.

The serial link enables the link adaptor to communicate with another link adaptor, a transputer or an INMOS peripheral processor. Two link adaptors, directly connected via their byte–wide interfaces, inserted into an INMOS serial link will correctly maintain the handshaken protocol of the INMOS serial link.

Data reception is asynchronous which allows communication to be independent of clock phase. Transfers may proceed in both directions at the same time.

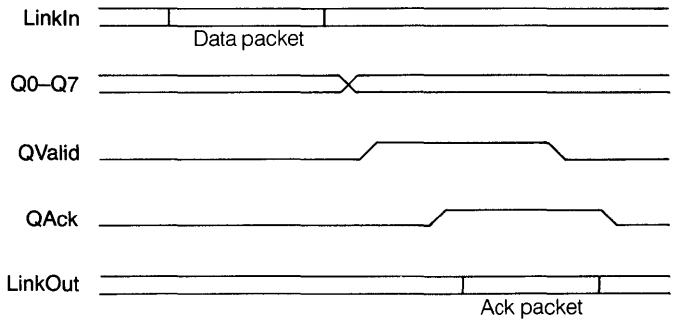
Output to link

Data is presented to the link adaptor on **I0–I7**, and **IValid** is taken high to commence the handshake. The adaptor transmits the data through the serial link, and acknowledges receipt of the data on **IAck** when it has received the acknowledgment from the serial link and all the data bits have been transmitted.

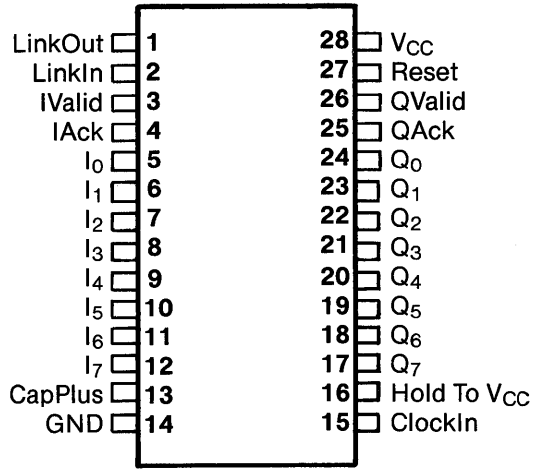


Input from link

The link adaptor receives data from the serial link, presents it on **Q0–Q7**, and takes **QValid** high to commence the handshake. Receipt of the data is acknowledged on **QAck**, and the link adaptor then transmits an acknowledgement on the serial link.



The C001 is available in a 600 mil 28 pin DIP package.



Ordering details

Product	Part number
Link adaptor	IMS C001

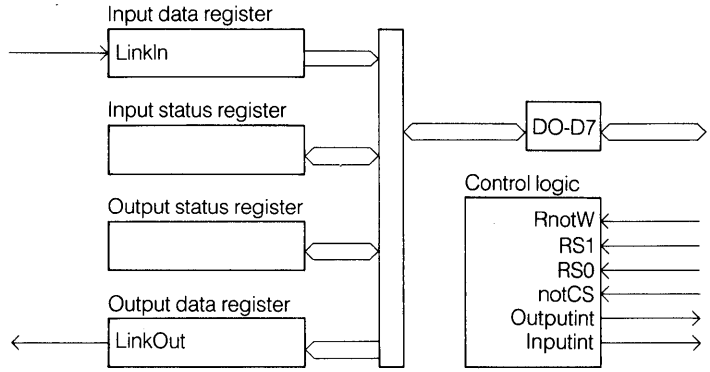
IMS C002 link adaptor

Features

- High performance system interconnect
- Bi-directional handshaken byte-wide interface
- INMOS serial link
- 10M bits/sec data rate
- Interrupt control for microprocessor buses
- Advanced 1.5 micron CMOS technology
- Standard 300 mil 24 pin DIP

Applications

- Interface between transputers and industry standard peripherals
- High performance handshaken link between standard microprocessor buses



The IMS C002 link adaptor provides an interface between an INMOS serial link and a microprocessor system bus, via an 8–bit bidirectional interface.

The C002 has status/control and data registers for both input and output. Any of these can be accessed at the byte wide interface at any time. Two interrupt lines are provided, each gated by an interrupt enable flag. One presents an interrupt on output ready, and the other on data present.

Data reception is asynchronous which allows communication to be independent of clock phase. Transfers may proceed in both directions at the same time.

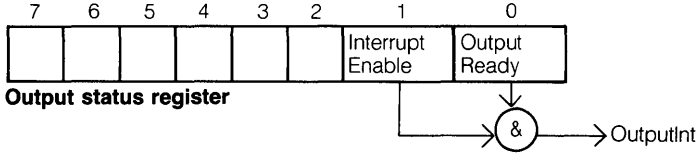
The C002 enables transputers to communicate with peripherals designed for conventional microprocessor systems. The C002 also makes it possible to build arrays with conventional microprocessors, and to link microprocessors from different families.

Parallel interface

One of the four registers is selected by **RS0** and **RS1**. If a new value is to be written into the selected registers, it is set up on **D0–D7** and **RnotW** is taken low. **notCS** is then taken low. On read cycles, the C002 places the current value of the selected register on **D0–D7**.

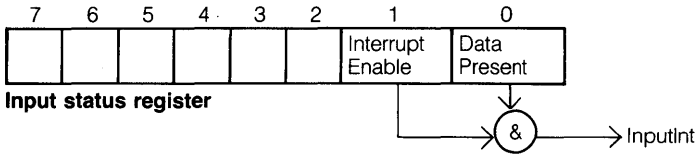
RS1	RS0	RnotW	**Function**
0	0	1	**D0–D7** := input data register
0	1	0	output data register := **D0–D7**
1	0	1	**D0–D7** := input status register
1	0	0	input status register := **D0–D7**
1	1	1	**D0–D7** := output status register
1	1	0	output status register := **D0–D7**

Output to link



The **output ready** status bit indicates that the serial link is able to receive a byte of data. It is set on reset, and when the C002 receives an acknowledgement from the serial link. It is reset when a data byte is written to the output data register on the parallel interface. **Outputint** is set if both **output ready** and **interrupt enable** are set.

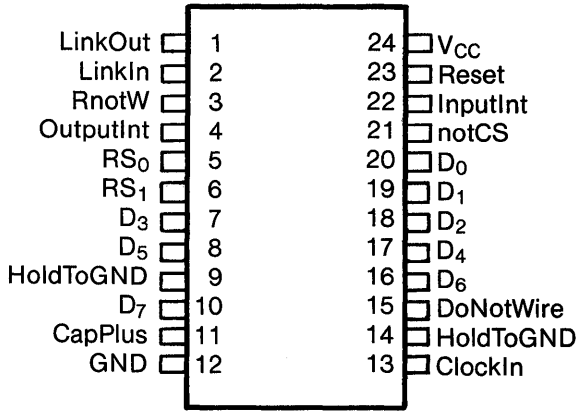
nput from link



The **data present** status bit indicates that the serial link has received a byte of data. It is reset when the data byte is read from the input data register on the parallel interface, this causes an acknowledgement to be transmitted on the serial link. **Inputint** is set if both **data present** and **interrupt enable** are set.

C002 signal list

The C002 is available in a 300 mil 24 pin DIP package.



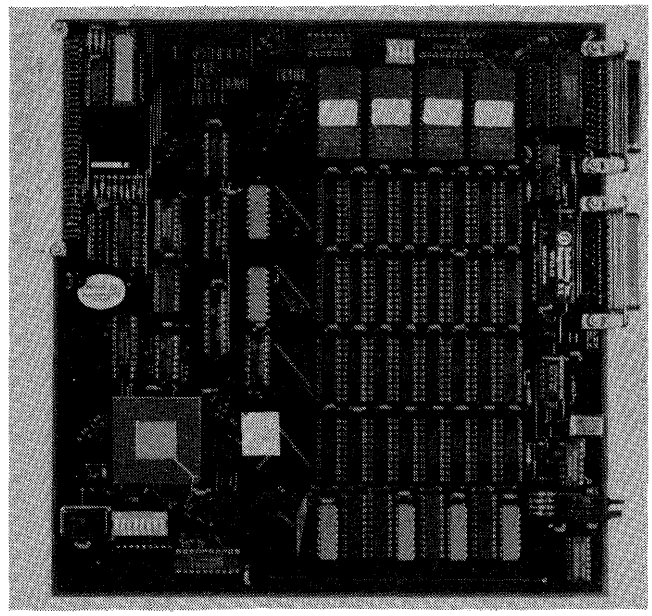
Ordering details

Product	Part number
Link adaptor	IMS C002

IMS B001 transputer evaluation board

Features

- 32 bit transputer
- 64K bytes of static RAM (IMS 1400)
- 128K bytes of ROM
- Bootstrap Loader
- Buffered INMOS serial links
- Two RS232 ports



The IMS B001 evaluation board enables users to evaluate and demonstrate the use of transputers. The board is the first of a family of compatible evaluation boards. It provides standard buffered INMOS link connections and external control of the transputer's Reset and Analyse functions. This allows it to control a subsystem consisting of other compatible boards, or to be a component of such a subsystem.

An occam program, designed and debugged within an INMOS transputer development system, is compiled and configured for either a single IMS B001 board or a network of interconnected compatible boards. The resulting code is then downloaded into the corresponding system and executed.

Double Extended Eurocard (233.4mm x 220mm)

32 bit transputer

10Mbits/sec INMOS link transmission speed with user selectable TTL buffering

64K bytes static RAM (32 x IMS 1400–45)

128K bytes EPROM (4 x 27256) contains bootstrap loader, memory test and terminal to host transparent mode software

RS232 serial input/output (SCN 2681 DUART) via D–type 25 way connectors

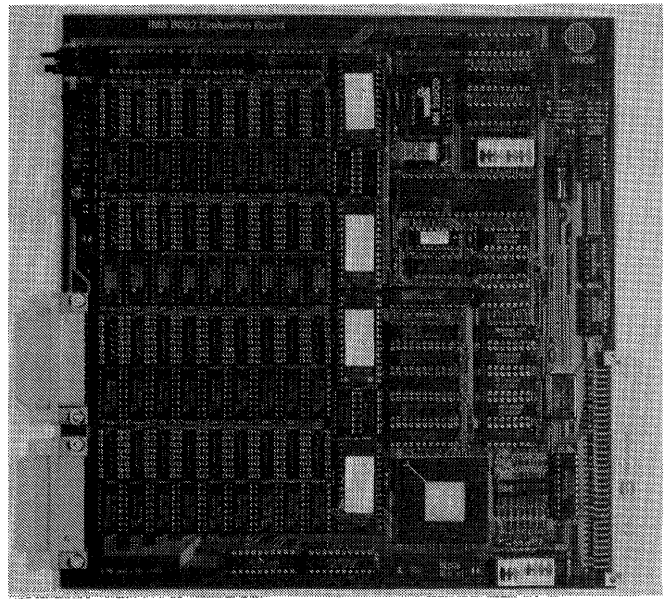
64 way a/c DIN connector	4 buffered/unbuffered INMOS links Master/Slave Resets Master/Slave Analyses Power supply
Switches	Boot from ROM Reset (push button) Analyse (biased toggle)
LED indicators	Error Power A16
Cables	power supply links transputer development system
Power supply	+5V (3 amps)

Product	Part number
Evaluation board	IMS B001

IMS B002 transputer evaluation board

Features

- 32 bit transputer
- 1M byte or 2M byte dynamic RAM with parity
- 128K bytes of ROM
- Bootstrap Loader
- Buffered INMOS serial links
- Two RS232 ports



The IMS B002 evaluation board enables users to evaluate and demonstrate the use of transputers. The board is one of a family of compatible evaluation boards. It provides standard buffered INMOS link connections and external control of the transputer's Reset and Analyse functions. This allows it to control a subsystem consisting of other compatible boards, or to be a component of such a subsystem.

An occam program, designed and debugged within an INMOS transputer development system, is compiled and configured for either a single IMS B002 board or a network of interconnected compatible boards. The resulting code is then downloaded into the corresponding system and executed.

Double Extended Eurocard (233.4mm x 220mm)

32 bit transputer

10M bits/sec INMOS link transmission speed with TTL buffering

1M byte or 2M byte dynamic RAM with parity

128K bytes EPROM (4 x 27256) contains bootstrap loader, memory test and terminal to host transparent mode software

RS232 serial input/output (SCN 2681 DUART) via D–type 25 way connectors

8 bit program readable/writable I/O available on edge connector and coding switch

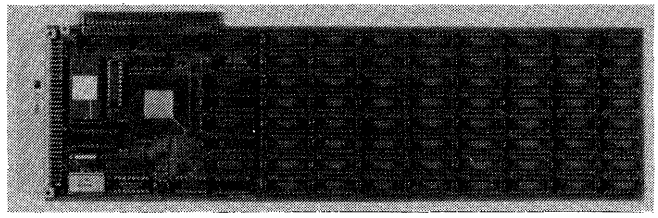
64 way a/c DIN connector	4 buffered INMOS links Master/Slave Resets Master/Slave Analyses Programmable I/O Boot from ROM control Power supply
Switches	Boot from ROM Reset (push button) Analyse (biased toggle)
LED indicators	Error Parity error Power 5 program writable
Cables	power supply links transputer development system
Power supply	+5V (3.5 amps) +0V

Product			Part number
	Transputer	Memory	
Evaluation board	T414	1M byte	IMS B002-1
Evaluation board	T414	2M byte	IMS B002-2
Evaluation board	T404	1M byte	IMS B002-3

IMS B004 transputer evaluation board

Features

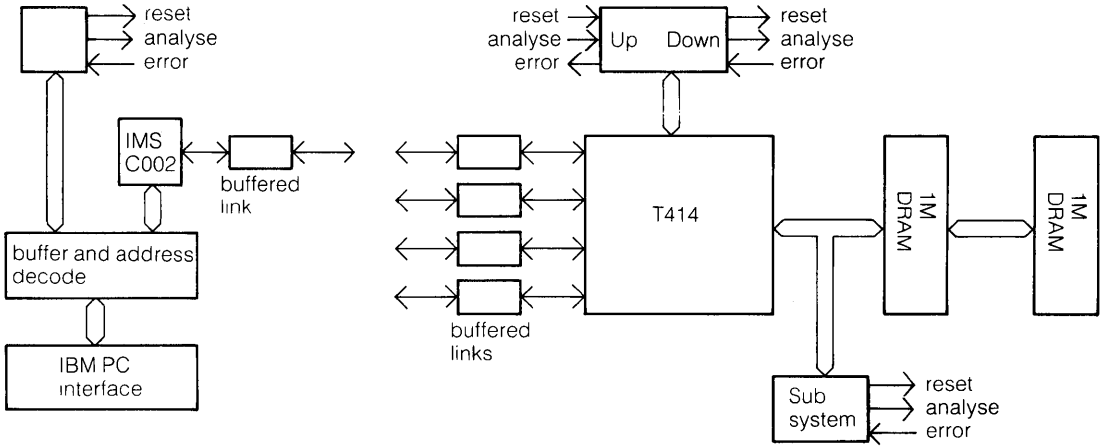
- 32 bit transputer
- 1M byte or 2M byte dynamic RAM with parity
- Buffered INMOS serial links
- IBM PC add-in card



The IMS B004 IBM PC add–in board enables users to evaluate and demonstrate the use of transputers. Containing a 32 bit transputer, the board provides a powerful upgrade to the IBM PC. The board is one of a family of compatible evaluation boards. It provides standard buffered INMOS link connections and external control of the transputer's Reset and Analyse functions. This allows it to control a subsystem consisting of other compatible boards, or to be a component of such a subsystem.

An occam program, designed and debugged within an INMOS transputer development system, is compiled and configured for either a single IMS B004 board or a network of interconnected compatible boards. The resulting code is then downloaded into the corresponding system and executed. The development system may be run on the IBM PC under DOS or on a separate computer.

The IBM PC I/O channel is interfaced to an INMOS link by the on–board IMS C002 link adaptor, and logic is provided for the transputer's external reset control and monitoring. Simple external connections complete the communication and control route between the IBM PC and the transputer system.



Board ready for installation in an IBM PC system unit expansion slot

32 bit transputer

10M bits/sec INMOS link transmission speed with TTL buffering

1M byte or 2M byte dynamic RAM with parity

62 pin I/O channel connector	IMS C002 link adaptor Reset/Analyse/Error Power supply
Connectors	5 buffered INMOS links Master/Slave Resets Master/Slave Analyses
Cables	INMOS links Reset/Analyse/Error cables
Power supply	+5V (1.75 amps) +0V

Product			Part number
	Transputer	Memory	
Evaluation board	T414	1M byte	IMS B004-1
Evaluation board	T414	2M byte	IMS B004-2

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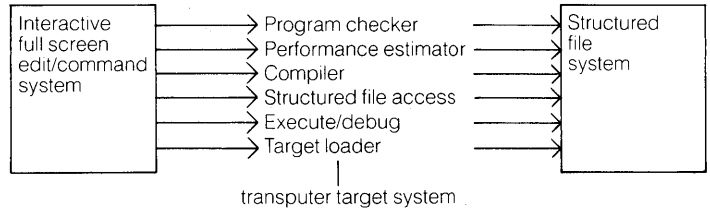
IMS D100 transputer development station

Features

- Fully integrated editor and development toolset
- Single user 10 MHz M68000 based workstation
  Fifteen megabyte Winchester disk
  One megabyte RAM
  640K byte floppy disk drive
  VDU terminal
- Compiles occam for:
  Execution on development station
  Interconnected transputers
- All application development at occam source level
- Hierarchical program structure with separate compilation



The transputer development station provides all the facilities of the occam programming system on a self contained workstation. Within the system the user edits, compiles and debugs occam programs, exploiting the full screen text editing facilities and using function keys to access the capabilities of the toolset provided by the system.

The user's program may also be compiled for a single transputer or an array of transputers. The compiled code can then be downloaded via an RS232 port or transmitted to an EPROM programmer.

Licence terms and conditions -- permits internal use for any purpose

Workstation	10 MHz M68000 1 Mbyte RAM with parity 15 Mbyte Winchester disk 5 1/4" 640K byte floppy disk Monochrome vdu terminal Cables for power and terminal connection

Integrated occam editor/compiler

Targets supported	T414 transputer system T212 transputer system M68000

Occam kernel for M68000

Floating point and I/O library

Utilities for file conversion and copying

Tutorial file

Documentation	System installation manual Transputer development system manual Occam programming manual M68000 implementation manual Transputer implementation manual Maintenance documentation

Software supplied installed on Winchester and on floppy disk

The transputer development station can be purchased directly from INMOS and its franchised distributors. Specify supply voltage required when ordering.

Product	Part number
Transputer development station	IMS D100

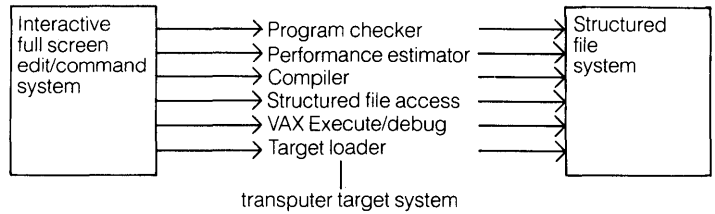
Warranty

The transputer development system is supplied with 90 days warranty from both INMOS and its franchised systems distributors. Details of suitable maintenance companies for extending hardware cover are included in the system documentation.

IMS D600 transputer development system VAX/VMS

Features

- Fully integrated editor and development toolset
- Compiles occam for:
  VAX under VMS
  Interconnected transputers
- All application development at occam source level
- Hierarchical program structure with separate compilation
- Runs on VAX/VMS 11/7xx computers including MicroVAX



The transputer development system runs on any VAX computer (including MicroVAX) under versions 3 and 4 of VMS. It provides all the facilities of the occam programming system, and is entered by a simple VMS command. Within the system the user edits, compiles and debugs occam programs, exploiting the full screen text editing facilities and using function keys to access the capabilities of the toolset provided by the system.

The user's program may also be compiled for a single transputer or a network of transputers. The compiled code can then be downloaded via the RS232 terminal line or transmitted to an EPROM programmer.

Licence terms and conditions – permits internal use for any purpose

Integrated occam editor/compiler

Targets supported	T414 transputer system T212 transputer system VAX

Occam kernel (in VAX/VMS object format)

Floating point and I/O library

Utilities for file conversion and copying

Tutorial file

VMS installation commands

Terminal capability	VT100 and TVI–920C Table driven terminal driver Terminal driver source
Documentation	System installation manual Transputer development system manual Occam programming manual VAX implementation manual Transputer implementation manual

Software supplied on 1600bpi VAX format magnetic tape.

The transputer development system can be purchased directly from INMOS and its franchised distributors:

Product	Part number
Transputer development system VAX/VMS	IMS D600

VAX and VMS are trademarks of Digital Equipment Corporation.

IMS D700 transputer development system IBM PC

Features

- Fully integrated editor and development toolset
- Compiles occam for:
  IBM Personal Computer under DOS
  Interconnected transputers
- All application development at occam source level
- Hierarchical program structure with separate compilation
- Runs on IBM Personal Computer XT and AT

Licence terms and conditions – permits internal use for any purpose

Integrated occam editor/compiler

Targets supported
- T414 transputer system
- T212 transputer system
- 8088/8086

Occam kernel (in DOS object format)

Floating point and I/O library

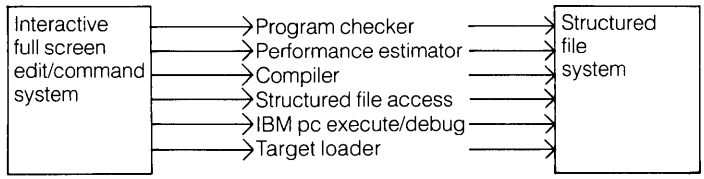
Utilities for file conversion and copying

Tutorial file

DOS installation commands

Documentation
- System installation manual
- Transputer development system manual
- Occam programming manual
- IBM PC implementation manual
- Transputer implementation manual

Software supplied on a set of floppy disks



transputer target system

The transputer development system runs on an IBM Personal Computer with 640K bytes of RAM and hard disk under DOS. It provides all the facilities of the occam programming system, and is entered by a simple DOS command. Within the system the user edits, compiles and debugs occam programs, exploiting the full screen text editing facilities and using function keys to access the capabilities of the toolset provided by the system.

The user's program may also be compiled for a single transputer or a network of transputers. The compiled code can then be loaded via an add–on board, downloaded via an RS232 line, or transmitted to an EPROM programmer.

The size of each separate compilation unit is limited by the segmentation constraints of the 8086.

The transputer development system can be purchased directly from INMOS and its franchised distributors:

Product	Part number
Transputer development system IBM PC	IMSD700

IBM is a registered trademark of International Business Machines Corporation.

occam®

Occam

Occam is a simple programming language, based on the concepts of concurrency and communication.

These concepts are central to today's applications of microprocessors and computers, and will play an even more important role in the future when multitudes of computers are connected to form intelligent systems.

Occam is intended for the professional design engineer/programmer.

It is simple, easy to learn and is oriented to interactive work-station based use. Occam's keywords and operators can exactly mirror system structure, enabling complex applications to be designed and programmed in a concise and readable form. As a result, design and implementation costs and times are reduced.

Occam may be used as a combination design, simulation and implementation language.

Complete hardware/software systems may be described in occam. Executing the program provides an efficient system simulation tool. The program describing the hardware components of the system can act as a formal design description for any new hardware design, while the program describing the software components may be used as the actual software for the final product.

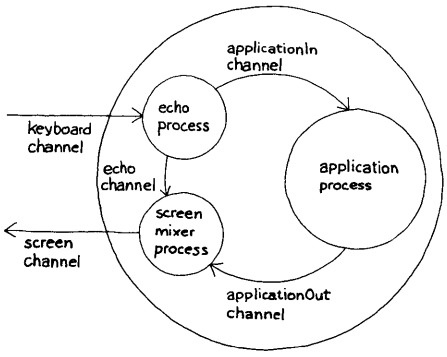
Occam related products

Occam programming manual

A tutorial introduction and reference manual for the first release of the language.

Occam development software

For development of applications in occam, a range of support products is provided. These include compilers, together with appropriate tools, optimised for occam program development, which are intended to run on a variety of widely available hosts, generating target code for a variety of processors.




```
CHAN keyboard AT 2:
CHAN screen AT 1:
CHAN echo,applicationIn,applicationOut:

DEF endbuffer = -3:

PAR

  -- echo process
  VAR ch:
  WHILE TRUE
    SEQ
      keyboard?ch
      echo!ch
      applicationIn!ch

  ...-- screen mixer process
  ...-- application process
```

Model

Systems are described as a collection of concurrent processes, which communicate using channels.

Implementation

An occam program may be executed on a network of interconnected computers, each executing one of the concurrent processes. However, with no changes except to configuration details it may be implemented on any smaller network or a single computer, with each computer sharing its time between its set of concurrent processes.

Structure

Programs are constructed from processes combined together using constructors. The primitive processes of input, output and assignment form the lowest level of processes in a program.

Input and output

A channel provides communication between two concurrent processes. The communication is synchronised. One process must be an input process and the other an output process. The communication takes place only when both processes are ready, when the values are copied from the output process to the input process.

```
InputChannel ? char
```

```
OutputChannel ! char
```

Sequence

The sequence constructor defines a process whose component processes are executed one after the other in the order in which they appear. A sequence construct terminates after the last of its component processes has terminated.

```
SEQ
  InputChannel ? char
  OutputChannel ! char
```

Parallel

The parallel constructor defines a process whose component processes are executed concurrently. A parallel construct terminates only when all its component processes have terminated.

```
PAR
  out1 ! 'a'
  out2 ! 'b'
```

Alternative

The alternative constructor defines a process, each component of which has an input process as its first component. The first process able to complete its input is chosen for execution. The alternative construct terminates when the chosen process terminates.

```
ALT
  in1 ? char
    out ! char
  in2 ? char
    out ! char
```

Conditional

The conditional constructor defines a process, each component of which has a condition as its first component. The conditions are tested in sequence. If a condition is found that evaluates to true that process is chosen for execution. The conditional construct terminates when the chosen process terminates.

```
IF
  x < 0
    x:= -x
  x >=0
    SKIP
```

Repetition

The repetition constructor defines a condition and a process which will be repeatedly executed until the result of evaluating the condition is false.

```
WHILE x > 0
  SEQ
    in ? x
    out ! x
```

Time

A clock local to each computer is maintained and may be accessed via the special channel **TIME** and used to control the execution of a process.

```
TIME ? AFTER e
```

Abstraction

A name can be given to the text of a process. The text will be substituted for all occurences of the name in textually subsequent processes. Channels, variables and other names may be used as parameters when textual substitution takes place.

```
PROC echo(CHAN in,out)=
  WHILE TRUE
    VAR x:
    SEQ
      in ? x
      out ! x:
```

Application Notes 6

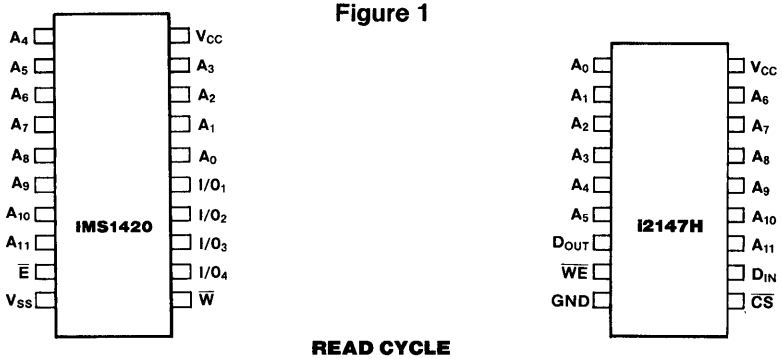
IMS1420
4Kx4 vs 4Kx1
Application Note #1

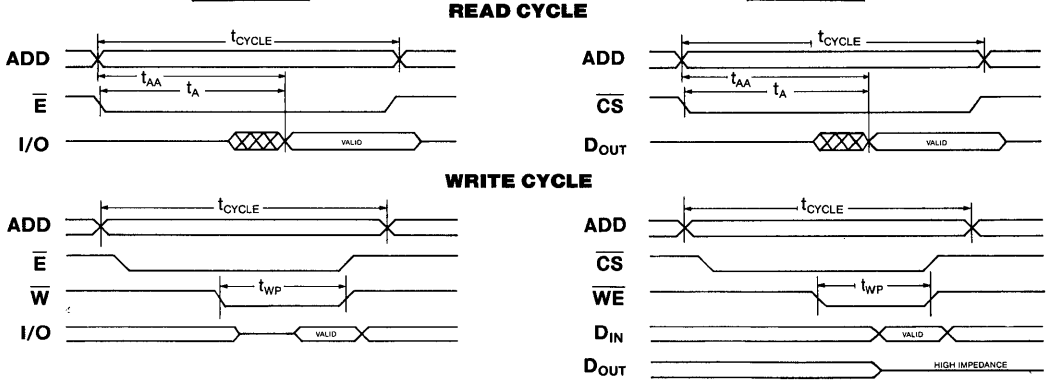
IMS1420 Tops 2147H with Less Board Space and Reduced Power Consumption!

INTRODUCTION

Bipolar memory devices have traditionally been used in memory designs requiring high speed, but at a high cost in power dissipation. Recently, MOS memory devices (2147H) have met the speed requirement, while providing lower power dissipation, thus encroaching on the bipolar applications. Some of these applications include memory systems which use wide words. The INMOS IMS1420 provides the speed with a considerable reduction in power dissipation and directly reduces the number of memory devices necessary to meet wide word requirements.

Figure 1





t_{AA} = 40ns
t_{cycle} = 40ns
t_A = 45ns
t_{WP} = 30ns

t_{AA} = 45ns
t_{cycle} = 45ns
t_A = 45ns
t_{WP} = 25ns

Figure 2

DEVICE DESCRIPTION

The IMS1420 is a high performance 4K x 4 static RAM having maximum Chip Enable ($\overline{E}$) access times of 45 and 55nsec, with a maximum power dissipation of only 66mW. The use of innovative design techniques as well as the latest VLSI technology have combined to produce these characteristics. The IMS1420 features fully static operation requiring no external clocks or timing strobes, equal Address access and cycle times, full TTL compatibility and operation from a single +5 volt supply. A Chip Enable function provides standby operation reducing power consumption to less than 165mW maximum. The device is housed in a 20-pin,300-mil DIP.

The Intel 2147H is a 4K x 1 static RAM, having maximum Address and Chip Select ($\overline{CS}$) access times of 45 and 55nsec. The maximum power dissipation is 990mW with a standby power dissipation of 165mW. As with the IMS1420, the device is fully TTL compatible and operates from a +5 volt power supply. The 2147H is packaged in an 18-pin, 300-mil DIP*.

When comparing the memory devices (see Figure 1), the similarities in the pinouts show that both devices are identical in the number of address pins, and both have WRITE ($\overline{W}$, $\overline{WE}$) and SELECT ($\overline{E}$, $\overline{CS}$) control input functions. The differences in the pinouts show that the IMS1420 has 4 common I/O data pins while the 2147H has separate data-in and data-out pins. Comparison of the READ and WRITE cycles of the devices shows equivalent Chip Enable access times, but shorter Address access and cycle times for the IMS1420. (See Figure 2.)

INTERFACING

The CPU systems shown in Figure 3 show the main busses as Address, Control and Data. System A has a common I/O data bus, while System B has separate data-in and data-out busses.

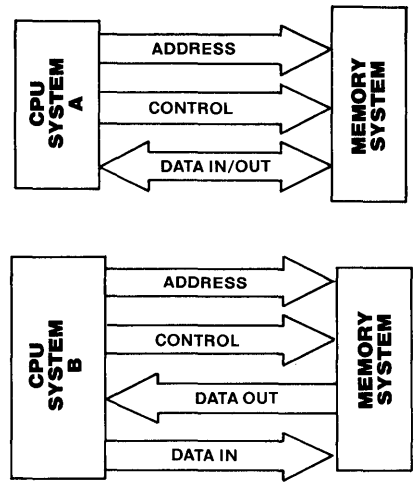
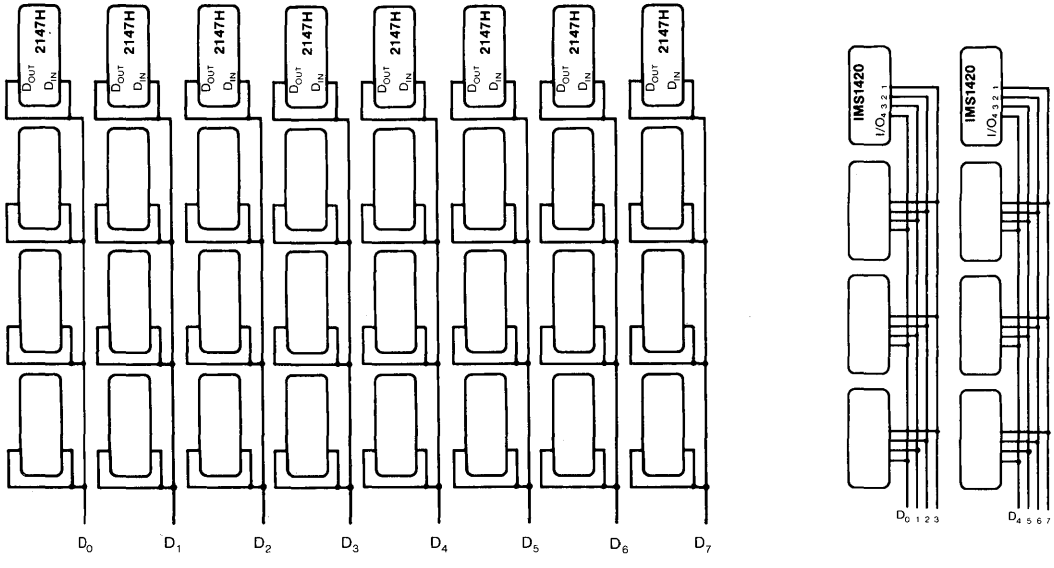


Figure 3

Interfacing to the address and control bus connections for both systems is straightforward and identical for the 2147H and the IMS1420, with one exception. The 2147H requires the use of a pullup resistor to V_{CC} on the chip select pin, to prevent the device from powering up in the select mode when V_{CC} is first applied. † With the IMS1420, when V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input.



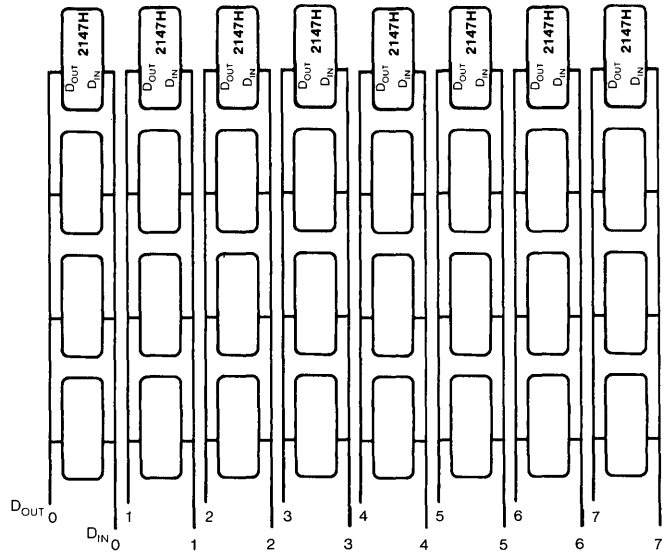
(a.) (b.)

Figure 4

* 1980 Intel Component Data Catalog, pg. 1-65 to 1-68.

† 1980 Intel Component Data Catalog, pg. 1-66, Note #3.

(a.)



(b.)

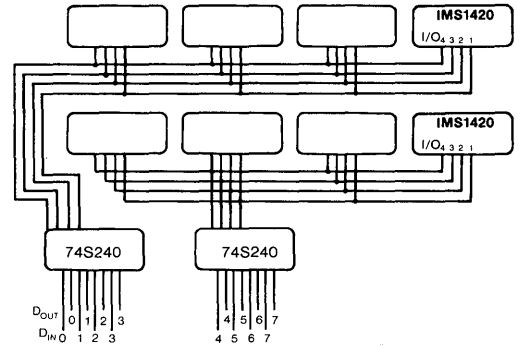


Figure 5

Therefore a pullup resistor from $\overline{E}$ to V_{CC} is unnecessary. After V_{CC} is applied for 2ms, the $\overline{E}$ input controls device selections as well as standby and active modes.

Interfacing to CPU System A is almost the same for the IMS1420 or the 2147H. The data-in and data-out pins of the 2147H are tied together, and then tied to a bi-directional data line of the data bus. The data input/output pins of the IMS1420 are each tied directly to a bidirectional data line of the data bus. (Figure 4a and 4b.)

Bus contention between data coming into a memory device and data going out of a memory device is only a problem during the WRITE cycle. If $\overline{CS}$ goes low a period of time before $\overline{WE}$ goes low, the device output driver could become active during the time that the input data is placed on the bus. Since both the CPU system and the memory device would try to drive the same data bus line, large current transients can occur. To prevent bus contention, the $\overline{CS}$ must go low after $\overline{WE}$ goes low, keeping the memory output driver in high impedance. Thus when the input data is placed on the bus, no contention occurs between the output driver of the device and the ouput driver of the CPU system. This is called a Chip Enable controlled WRITE cycle. (See Figure 6.)

The most direct approach to interface 2147H memory devices to CPU System B is shown in Figure 5a. Four rows of eight 2147H memory devices are each connected directly to separate data-in and data-out lines. Because the data input and output lines are separate, no special timing during the WRITE cycle is necessary to prevent bus contention.

Four rows of two IM1420's each can interface to CPU System B, using two 74S240's (or similar bus driver) to interface to the separate data-in and data-out busses. This can be accomplished as shown in Figure 5b. The timing for the READ cycle would remain the same but in the WRITE cycle (see Figure 6), only a Chip Enable

WRITE CYCLE : $\overline{CS}/\overline{E}$ CONTROLLED

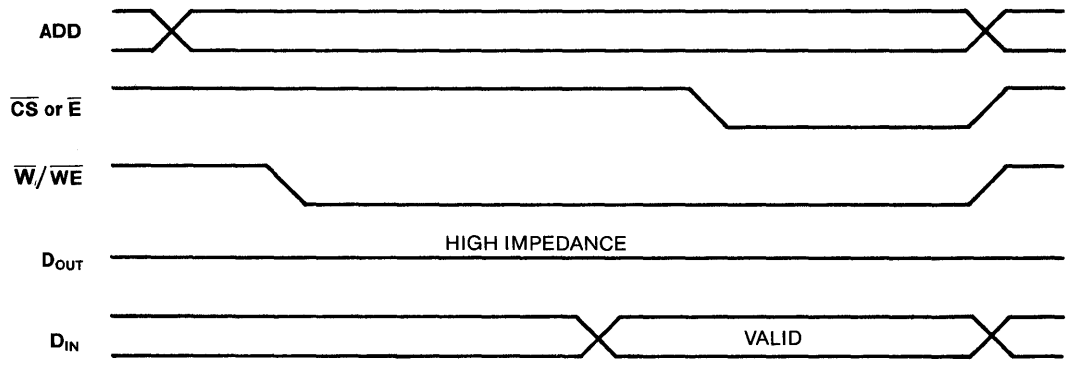


Figure 6

controlled WRITE cycle could be used. This would keep the data-out drivers of the IMS1420's in the high impedance state during the WRITE cycle, preventing any data bus contention with input data.

SAVINGS

With CPU System A each IMS1420 could replace four 2147H memory devices. The following calculations show the savings in PC board area, memory chip count, and power consumption. These calculations include 0.2 in. horizontal and vertical spacing between packages to more accurately represent actual layouts.

	2147H	IMS1420	NET SAVINGS
No. of Packages	32	8	24
Area	17.6in²	4.8in²	12.8in²
Power	11.88W	2.2W	9.68W

With CPU System B, each IMS1420 could replace four 2147H memory devices, but two data bus drivers must be added. Still, a net savings can be seen.

	2147H	IMS1420	74S240	NET SAVINGS
No. of Packages	32	8	2	22
Area	17.6in²	4.8in²	1.2in²	11.6in²
Power	11.88W	2.2W	1.6W	8.6W

CONCLUSION

By replacing every four 2147H memory devices with one IMS1420 memory device, a 4-to-1 memory chip count reduction, as well as a 5-to-1 reduction in power dissipation of the memory system occurs. This could directly increase the overall system reliability and efficiency, while using less PC board space for the same amount of memory capacity.

IMS1420
4Kx4 vs 2Kx8
Application Note #2

Use the IMS1420 in Place of 2K x 8's and Cut Board Space in Half.

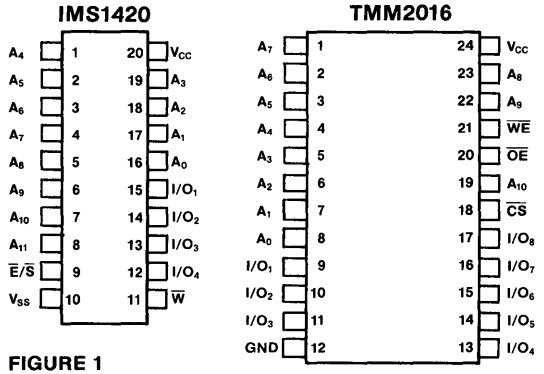


FIGURE 1

The new 2K x 8 static RAMs have definite applications in microprocessor systems where small amounts of RAMs are required. When the total amount of RAM exceeds 2K bytes, however, the 4K x 4 static RAM becomes a cost-effective alternative.

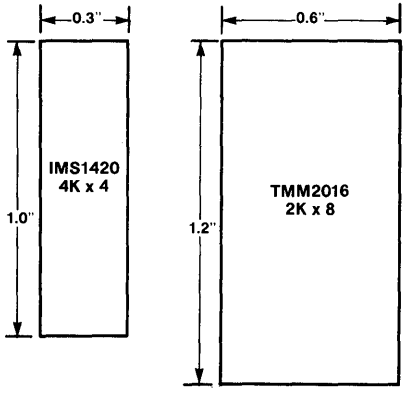


FIGURE 2a

A comparison between a typical 2K x 8 static RAM (Toshiba TMM2016) and a 4K x 4 static RAM (INMOS IMS1420) yields results which should be of particular interest to the design engineer.

Figure 1 shows package outlines for each device. Although the 2K x 8 has only 4 more pins than the 4K x 4, its package is twice the size of the 4K x 4 device. Figure 2a shows the package comparison.

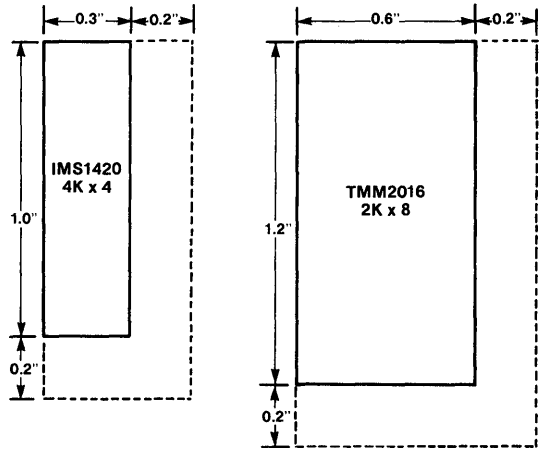


FIGURE 2b

The 4K x 4 is 0.3 square inches while the 2K x 8 is 0.72 square inches. When mounted on a printed circuit board, there must be room added for spacing purposes (assume 0.2" per side). Thus, the effective space required for each device is shown in Figure 2b. The 4K x 4 requires only 0.6 square inches, while the 2K x 8 needs 1.12 square inches.

The advantages of this can be demonstrated using a real-world example. Assume a memory board for the

Memory Word Size	No. of 24 Pin Devices	Total Area	No. of 20 Pin Devices	Total Area
4K x 8	2	2.24 sq. in.	2	1.2 sq. in.
8K x 8	4	4.48 sq. in.	4	2.4 sq. in.
16K x 8	8	8.96 sq. in.	8	4.8 sq. in.
24K x 8	12	13.44 sq. in.	12	7.2 sq. in.
32K x 8	16	17.92 sq. in.	16	9.6 sq. in.
48K x 8	24	26.88 sq. in.	24	14.4 sq. in.
64K x 8	32	35.84 sq. in.	32	19.2 sq. in.

TABLE 1

Standard BUS (STD BUS) is to be designed with the maximum amount of static RAM memory on it. With a typical STD card size of 4.5" x 6.5" (29.25 square inches), careful attention must be paid to efficiently use the relatively small space at hand. In addition to the memory devices, allowance for TTL interface circuitry and PC traces must also be included. The final area for the memory devices alone may be as small as 15 square inches.

Table 1 shows the total area required by the 4K x 4 and 2K x 8 devices in various memory sizes. With 15 square inches of board space available for the memory devices, the chart shows that only 12 2K x 8 chips would fit on the STD board, yielding a memory size of 24K x 8. On the other hand, 24 4K x 4 devices could be used in the same area for a 48K x 8 memory, or double the size of the 2K x 8 system.

In the case of deep memories (greater than 16K bytes), it may be advantageous to go to a 16K x 1 static RAM such as the IMS1400. The amount of decode logic is reduced for the 16K, and separate input and output data lines are available. Where low power is critical, however, the 2K x 8 and 4K x 4 are better choices, since fewer chips are powered-up at any given time.

Overall, the 4K x 4 device is a better choice than the 2K x 8 in systems requiring a memory greater than 2K bytes deep. Board space savings make the 4K x 4 a natural in such systems.

IMS1400
IMS1420
BITMAPS

Application Note #3

In the course of evaluating a memory IC, various tests are often performed which check for potential weaknesses which may be inherent in the device. These tests include voltage stress tests, fine and gross leak tests, life tests, pattern-sensitivity tests, etc. This Application Note discusses bitmaps for the IMS1400 (16Kx1) and the IMS1420 (4Kx4) static RAMs. Bitmaps describe the internal addressing topology and are necessary for thorough characterization of the devices.

In a static memory device bits are stored in cells. The cells are arranged in a two-dimensional array, which is made up of rows and columns. During RAM accessing, cell selection within the array is done by on-chip row and column address decoders. Optimum design of these

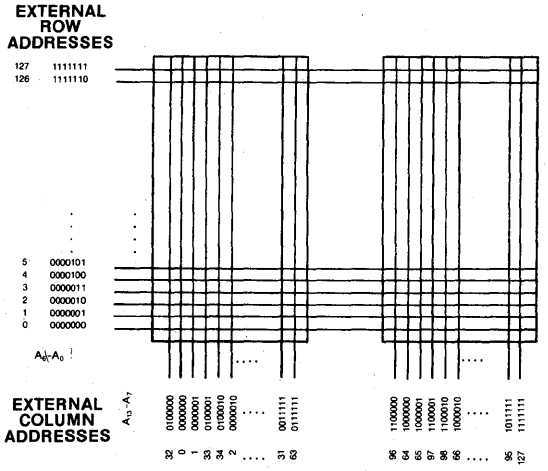


Figure 1: IMS1400 BITMAP

address decoders often results in a scrambling of the relationship between the externally applied address and the internal physical storage cell location.

THE IMS1400 BITMAP

In order to perform meaningful address sensitivity test sequences, it is necessary to determine the physical location of the cell (within the array) that is being addressed. Since the key to investigating pattern sensitivities is knowing how to address a specific cell, a bitmap (sometimes called a topographical memory map) is required to accomplish this. The bitmap for the IMS1400 is shown in Figure 1.

The IMS1400 has 14 address lines (A_0-A_{13}); A_0-A_6 are Row Addresses and A_7-A_{13} are Column Addresses. As shown in Figure 1, the Row Address begins at the bottom of the arrays with 0000000 and increments sequentially upwards to 1111111. Column Addresses are different, however, in that the columns they address "jump around" from left to right. For example, the leftmost column is 0100000, followed by 0000000, 0000001, 0100010, 0000010, etc.

A simple encoder circuit (see Figure 2) can take sequential logical Column Addresses (LA_7-LA_{13}) and convert them to the external addresses (A_7-A_{13}) required to access the columns in a left-to-right fashion. Rather than having to supply column addresses of 0100000, 0000000, 0100010, 0000010, . . . 1111111 to move left to right, the user would simply address 0000000, 0000001, 0000010, 0000011, . . . 1111111 and the encoder circuit would do the proper translations. This is a convenience tool for the software writer.

THE IMS1420 BITMAP

The bitmap for the IMS1420 appears in Figure 3. Since the IMS1420 is organized 4Kx4, only 12 address lines are required (A_0-A_{11}). These are organized as A_0-A_6 (Row Addresses) and A_7-A_{11} (Column Addresses). As with the IMS1400, the Row Addresses of the IMS1420

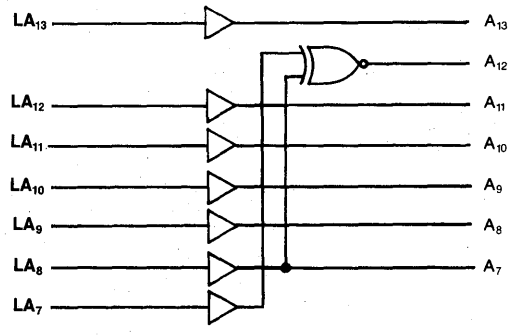


Figure 2: IMS1400 Address Encoder Circuit

sequence start at 0000000, 0000001, 0000010, and continue upwards to 1111111.

At this point, however, the similarity ends. One Column Address accesses four separate columns. As a result, one address applied to the IMS1420 accesses *four* distinct memory cells. The device is actually made up of two arrays—one for I/O_1 and I/O_2 and the other for I/O_3 and I/O_4. When an address is supplied to the device, it goes to both arrays, at which time two memory locations in each array are accessed.

The Column Addresses of the bitmap in Figure 3 are numbered sequentially left to right (from 00000 to 11111)

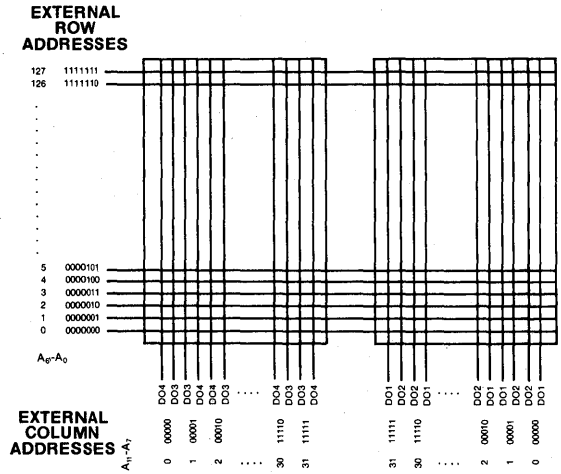


Figure 3: IMS1420 BITMAP

for the left array (I/O_3 and I/O_4) and right to left for the right array I/O_1 and I/O_2). Note that the order of the bits is flip-flopped with each successive address. Again, it is up to the test engineer to decide how these address lines are sequenced to test for pattern sensitivity.

REDUNDANCY

INMOS' static RAMs utilize redundancy to make the product more easily manufacturable. Since spare columns are used to replace defective columns, the bitmap accuracy may be slightly reduced. That is, by providing an address to access a given physical location, the test engineer may actually access a physical location that is quite different.

In the case of the IMS1400, zero, one or two columns may be utilized. This translates to a bitmap accuracy of 100%, 99.2% or 98.4% respectively. The IMS1420 utilizes zero, four or eight spare columns, yielding a bitmap accuracy of 100%, 96.9% or 93.8% respectively. Since any pattern sensitivity testing is a statistical evaluation, the very high percentage of bits which are topologically correct (even in "repaired" parts) gives the test engineer confidence that the traditional approach to pattern sensitivity testing is still valid.

IMS2600
Nibble Mode
Application Note #4

Nibble Mode Operation Simplifies High-Bandwidth Memory Applications

INTRODUCTION

For the past decade the semiconductor industry has put a great deal of emphasis on increasing the density of memories to decrease the cost per bit of memory. Unfortunately, in concentrating on reducing the cost per bit they have generally ignored the opportunity to, at the same time, increase the value of each bit of memory. One way to increase the value of memory is by incorporating functional enhancements that attack well-defined system problems while ensuring that the solution can be implemented in a silicon-efficient manner.

"Nibble mode" is one of the few fundamental functional enhancements to be incorporated into multiplexed dynamic RAMs since their introduction in the early 70's. It is one of the few enhancements that not only adds value by addressing a well defined system problem but, when properly implemented, can actually reduce component manufacturing and testing costs.

The system solution that "nibble mode" provides results in a significant improvement in memory bandwidth. It takes advantage of the fact that in a very large number of applications, data is transfered to and from memory in blocks or packets. The previous offerings from the semiconductor industry provided "page mode" as an attempt to solve this problem. However, as implemented on these devices, page mode did not offer a significant bandwidth improvement over totally random accesses. Also, for each bit read in page mode a new address must be supplied. This adds unnecessary complexity in terms of address generation and distribution in systems that do move data in well-defined packets.

These block oriented and other types of high bandwidth applications are addressed by "nibble mode" in a very straightforward way. The IMS2600 is organized like many other DRAMs such that internally four bits of information are accessed each cycle. Two bits of the column address are used to decode one of these four bits, the result being an apparent single bit access. On other multiplexed DRAMs any further accesses require that a new address be loaded (either a column address for page mode or a row and column address for another random bit). On the IMS2600, however, the other three bits may be accessed simply by taking $\overline{CAS}$ high and then low (toggling). Toggling $\overline{CAS}$ while $\overline{RAS}$ is low causes the IMS2600 to make the next bit in the group of four available for read and/or write access by the "outside world." The four bit "nibble" is defined by the row address and the 6 most significant bits of the column address. (Column addresses 3 and 6 are the two lowest order column address bits.) Thus, as bits are accessed in "nibble mode" the internally generated address will wrap around on the four-bit boundary. This boundary "restriction" very often turns into a system advantage. In many cache-oriented systems a cache miss causes a four word packet to be read from memory. The four word block consists of the addressed word and the other three words in the "vicinity" of the addressed word (not the addressed word and the "next" three). It is desirable in this type of system to fetch the addressed word *first* so that the CPU can continue and then fetch the other three neighbors. "Nibble mode" supports this type of operation because the address boundary for a packet of four cache words is the same (or can be made the same) as the address boundaries for a packet of four memory words.

This application note will not deal with the block or packet oriented type of system, which is an obvious 'nibble mode" application area, but will instead deal with how "nibble mode" can be used in applications requiring high bandwidths and a continuous data rate.

THE APPLICATION

The circuitry described in this application note uses eight IMS2600-12's operated in nibble mode to provide pixel data to a color monitor. Because the circuit is designed to interface to the IBM Personal Computer, the display format was chosen to be resolution compatible with the 640 pixel by 200 line format of the IBM Color Graphics Monitor Adapter. The IMS2600 is used to allow 4 bits/pixel at the 640x200 resolution rather than the 1 bit per pixel that is available on the current IBM color board. (See IBM Personal Computer Technical Reference manual.) As the primary intention of this application note is to demonstrate the use of "nibble mode," none of the alphanumeric or low resolution graphics modes of the IBM PC are implemented. However, the resolution and color selection are sufficient to allow implementation of a full 80 column by 25 line alphanumeric display with

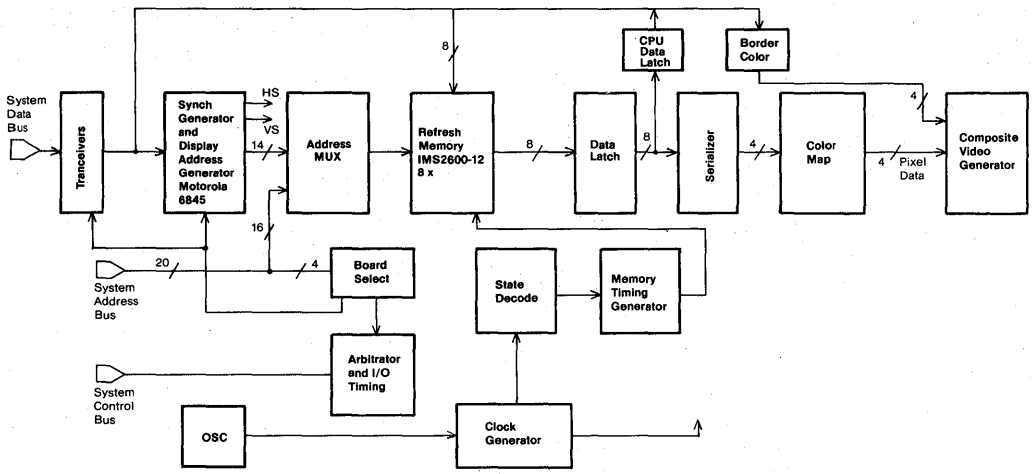


Figure 1. Block Diagram of Display Board

cursor, reverse character video, and blinking. Also, the circuitry to generate a vertical interval interrupt is included to facilitate updating on the screen in such a way as to eliminate the hashing of the display that would occur if screen updates were made during the scan interval.

Figure 1 shows the basic block diagram. The Motorola 6845 CRT Controller was chosen as the synch generator and display address generator mainly because it is used in the IBM PC. It has some quirks, but its ability to generate linear addressing of the refresh memory minimizes the amount of display refresh memory required when the display format is not a power of 2. The 6845 also has an intial address register that can be used to pan and scroll through the display memory, which is handy.

The 6845 generates a series of sequential addresses, one per clock period. The clock period for the 6845 is equal to eight pixel times. For each address from the 6845, four bits are read from each of the 2600's, giving 32 bits of 8 pixels. As the data is read from the 2600's, it is loaded into an 8 bit data latch. The output of this data latch is then transferred to the serializer so that the sequence of bytes from the memory is converted to a sequence of 4 bit pixels that are used to drive the display. The color mapping RAM between the data serializer and the video output circuit is used to convert the 4 bit codes from the display memory into 4 bit color information for the display. The color mapping memory makes it easy to implement some of the special functions. (More on this later.)

The clock generator, state decode, and the memory timing generator combination make the whole thing go. (Refer to the timing diagram in Figure 2a and the detailed schematics in Figure 3.) The timing generator is driven by an oscillator that runs at two times the pixel rate. In this particular instance the pixel rate as used by the PC is 14.31818 MHz, giving a pixel period of 69.84ns. To engineering accuracy, this is 70ns (0.2% error). The timing generator divides the oscillator frequency by 2, 4, 8 and 16 to give the pixel clock, two control clocks, and the 6845 clock respectively. The state decoder uses the outputs of the timing generator and decodes 1-of-16 states. The state decode outputs are used to condition the J-K flip-flops in the memory timing generator circuits, the outputs of which are used to drive the memory. The timing diagrams in Figure 2a and 2b show that the number of bytes accessed during each memory cycle is determined by the type of memory access being performed. An active display access fetches 4 bytes (8 pixels), a CPU access to memory accesses 1 byte, and a 6845 access during retrace accesses one byte. This last type of access causes no data to be output to the display and is used only to ensure continuous memory refresh during retrace intervals.

During a series of active display accesses, the Memory Timing Generator generates four $\overline{\text{CAS}}$ pulses every 560ns (8 pixel times). The rising edge of each $\overline{\text{CAS}}$ causes the accessed data to be strobed into the data latch. The $\overline{\text{CAS}}$ pulses do not occur on even pixel times so there is some skew between the data coming out of the memory and the data going to the display. The data serializer (Figure 4) acts like a 2 byte FIFO and deskews the data. The combination of the 74S374 and 74S257 in the data serializer "empties" the data latch once every two pixel times and breaks the byte stream into a stream of nibbles that goes at the pixel rate. Figure 5 shows the interaction of transfers between the data latch and the serializer. The letter "L" is used to indicate the time when the Memory Data Latch (74S374 Octal D-Flip-Flop) is loaded from the memory and "D" indicates that the serializer has

dumped the data from the Memory Data Latch so that the Memory Data Latch may be loaded again.

During a CPU read cycle, the output data latch is loaded with the data from the location addressed by the CPU. Since there is only one transition of $\overline{CAS}$ during a CPU access, the data is available until the first low-to-high transition of $\overline{CAS}$ during the next memory cycle (560ns minimum). Even if this is not enough time for the CPU to take the data, there is no problem as the data is captured in the CPU Data Latch (a transparent latch) and is available there until the next CPU memory access.

ARBITRATION

The circuit shown in Figure 6 is the type of arbitration that is necessary when synchronizing completely asynchronous signals. The CPU and display are each being driven by their own local oscillators so any activity on the system bus is completely asynchronous with respect to the memory on the display board. A memory access to the display board causes an immediate deassertion of IOREADY, causing the processor to wait for the memory to respond. The asynchronous request is then synchronized to the local clock with the two cascade flip-

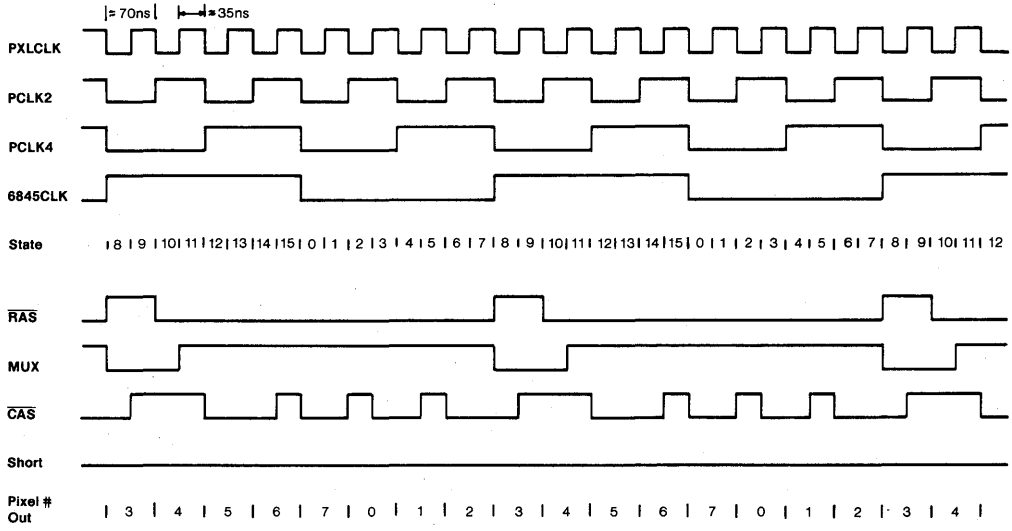


Figure 2a. Continuous Active Display Accesses

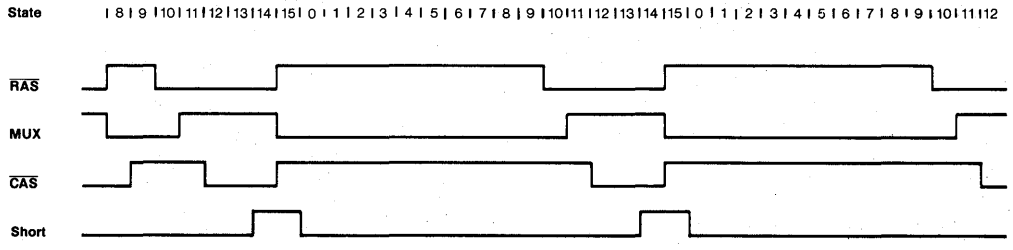


Figure 2b. CPU Access or Retrace Interval Memory Timing

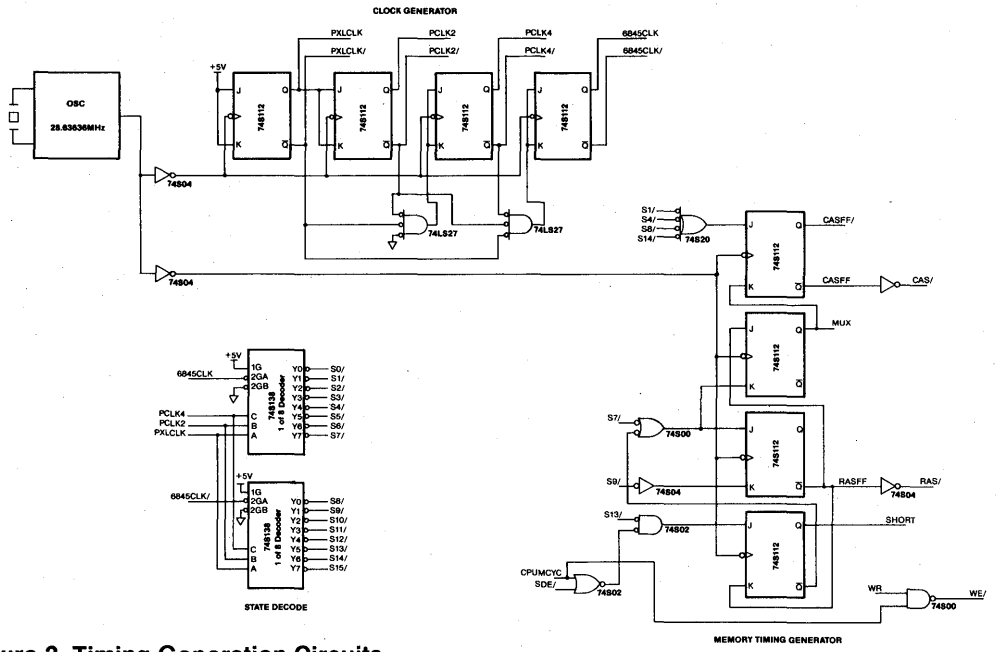


Figure 3. Timing Generation Circuits

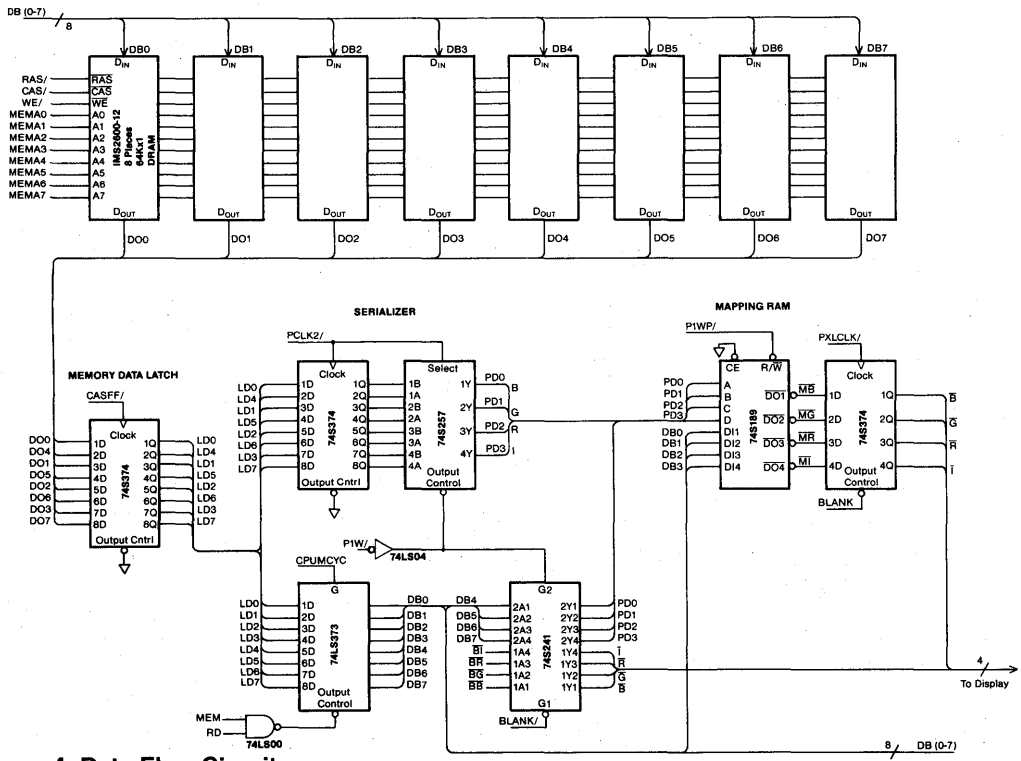


Figure 4. Data Flow Circuits

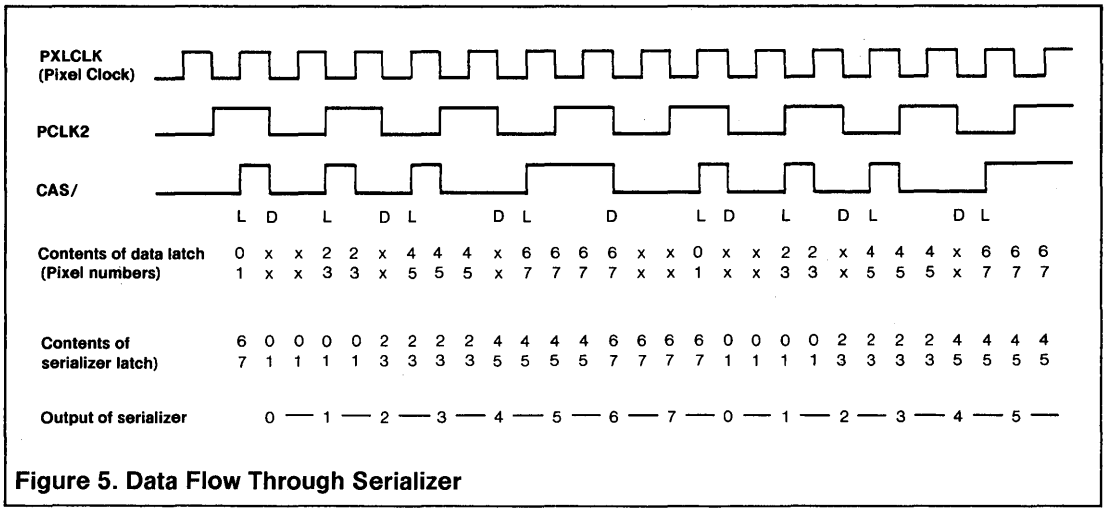


Figure 5. Data Flow Through Serializer

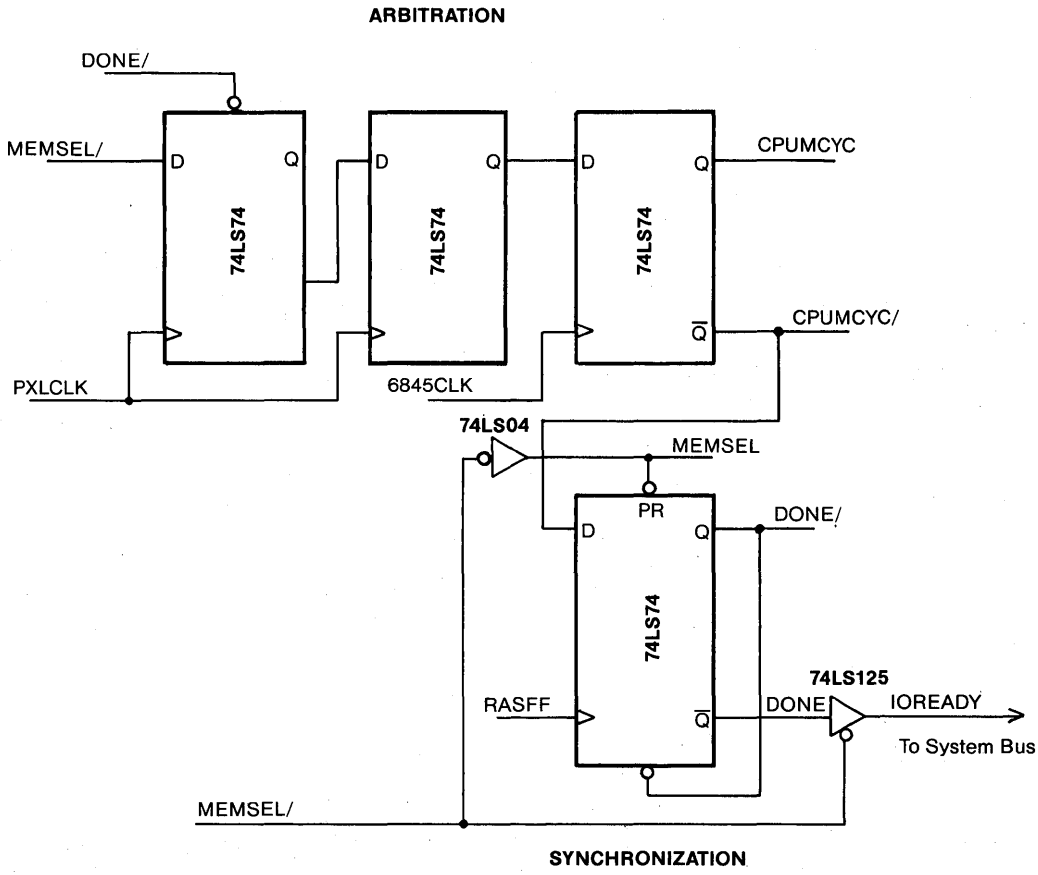


Figure 6. Arbitration and Synchronization

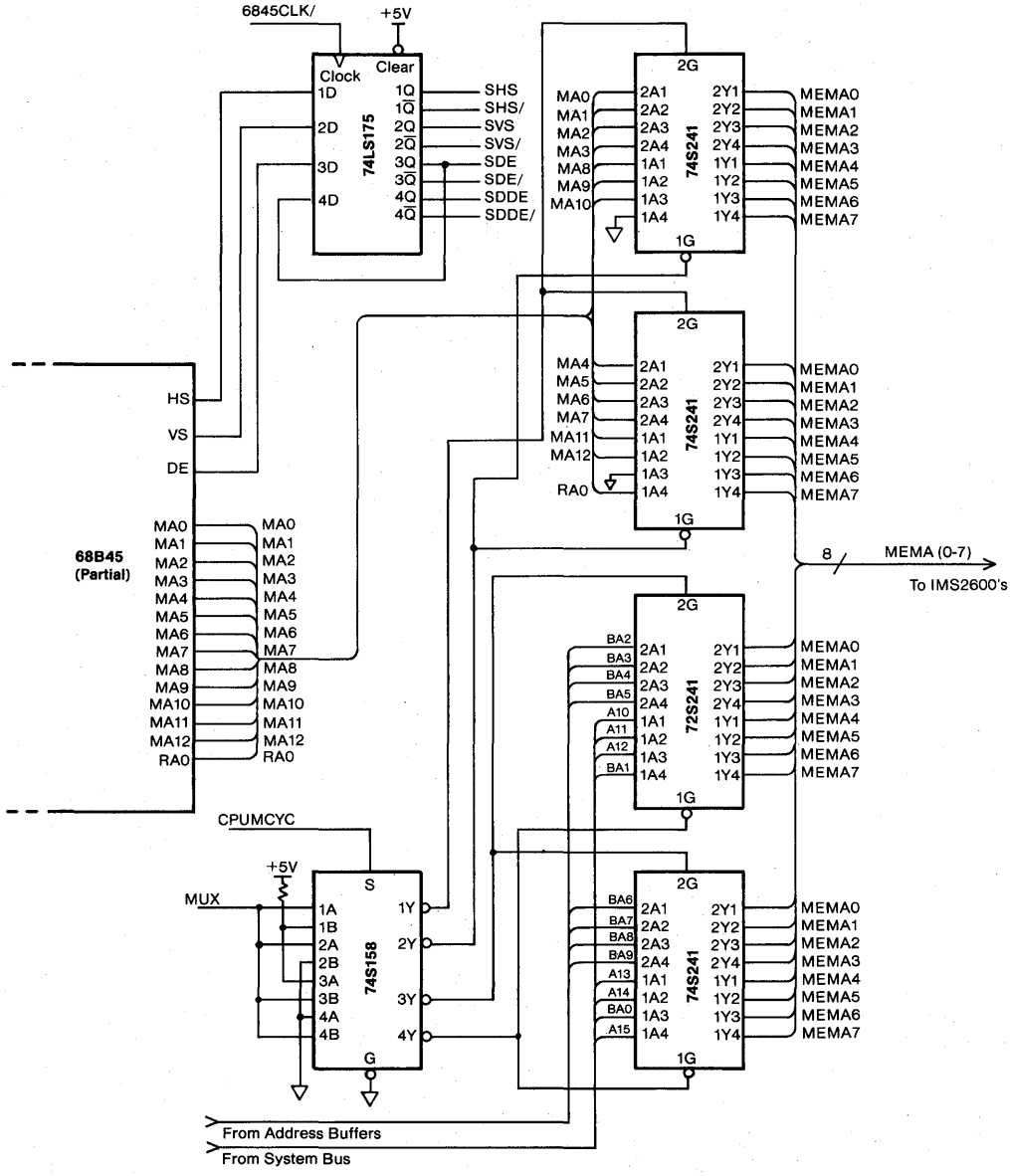


Figure 7. Address Multiplexing Circuits

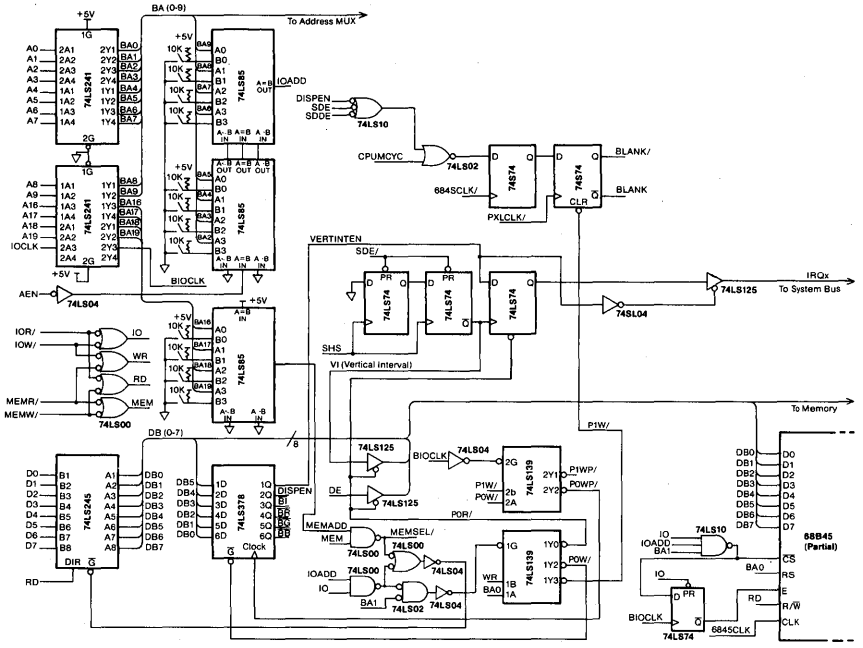


Figure 8. Misc. Control and Interface Circuits

flops. The synchronized CPU memory request then is synchronized to the start of the next memory cycle (3rd level of synchronization). Once the requested memory cycle starts ($\overline{RAS}$ goes low) IOREADY is asserted and the accessed data is made available or the data to the memory is written within 209ns.

TABLE 1. Address Correspondence

6845 Address	CPU Address	Memory Address
"0"	A0	COLUMN 6
"0"	A1	COLUMN 3
MA0	A2	ROW 0
MA1	A3	ROW 1
MA2	A4	ROW 2
MA3	A5	ROW 3
MA4	A6	ROW 4
MA5	A7	ROW 5
MA6	A8	ROW 6
MA7	A9	ROW 7
MA8	A10	COLUMN 0
MA9	A11	COLUMN 1
MA10	A12	COLUMN 2
MA11	A13	COLUMN 4
MA12	A14	COLUMN 5
RA0	A15	COLUMN 7

ADDRESS MULTIPLEXING

The address multiplexing (Figure 7) is accomplished by controlling the output enables of four 74S241's. The 74S241's multiplex the 16 CPU addresses or the fourteen 6845 display refresh addresses onto the eight IMS2600 address lines at the appropriate time. CPU display multiplexing is controlled by the CPUMCYC flip-flop and row/column addressing is controlled by the MUX signal from the memory Timing Generator. Only fourteen 6845 addresses are used because the 6845 always accesses 4 successive bytes in "nibble mode," so column addresses 3 and 6 are always "0" during a display refresh access. Table 1 shows the correspondence between 6845 addressing and CPU addressing of the memory. There are some details of the memory addressing that must be comprehended when the CPU computes the address of a pixel in the display memory.

```
      FUNCTION IADD (LINE, PIXEL)
c     Returns the address of a pixel in display relative to
c     the base address of the display memory. The ad-
c     dress is not a byte address.
      INTEGER LINE, PIXEL
c     Line is the raster line number in the range 0 to
c     199. 0 is the top line. Pixel is the pixel number
c     along the line in the range 0 to 639. 0 is the left
c     most pixel.
      IADD=(LINE/2)*648+PIXEL+8
      IF[MOD(LINE,2). EQ.1]IADD=IADD+65536
      RETURN
      END
```

The byte address containing this pixel is:

BYTE=IADD/2

The low order four bits of the byte contain even numbered pixels and the high order four bits contain the odd numbered pixels.

Figure 9. Pixel Address Computation

The display format, as mentioned earlier, is 640 pixels/line by 200 lines. When setting up the 6845, the number of displayed "characters" per row should be set to 81 characters. This gives 648 pixels positions/line, but only the last 640 pixels are displayed. (Display of the first "character" position in each line is suppressed by the blanking logic.) The blanked character position is used for left and right panning. The data is to be displayed after the pan is placed in the blanked area of each line and then the starting address register in the 6845 is incremented for pan right or decrimented for pan left.

The 200 line format of the display is somewhat of a problem. The Vertical Displayed (R6) and Vertical Total (R4) registers in the 6845 are only 7 bits. This does not give enough range to cover the 200 displayed scan lines if R9 (Max Scan Line Address) in the 6845 is set to "0." Therefore, to get enough range R6 must be set to 100 (decimal) and R9 must be set to 1. This will cause the RA0 output to be low on all even-numbered scan lines (count starts at 0) and high for all odd-numbered scan lines.

As an example of how the software can accommodate these addressing quirks, a FORTRAN routine that computes the address of a pixel is shown in Figure 9.

USE OF THE MAPPING RAM

As mentioned earlier, the stream of pixel codes coming from the serializer are fed through a 16x4 RAM to transform the codes to the final color information for the display. The CPU can therefore change the "color" that any code will display by modifying the mapping in the RAM. For example, if code "0000" is assigned the color value "0000" (black) and code "0001" is assigned the color value of "1111" (white) then white characters on a black background can be generated by storing codes "0000" and "0001" in the appropraite locations in the refresh memory (the IMS2600's). If it is then desired to blink the characters, then all that is required is that the CPU periodically change the mapping of code "0001" from "1111" to "0000" to "1111," etc. The set of 16 codes can be allocated in any manner to achieve a wide variety of visual effects with very little CPU intevention.

MISCELLANEOUS CIRCUITRY

A detailed description of the circuitry to deal with bus protocol is not presented in this application note even though the circuitry is included in the schematics. The circuitry for converting the synchronous signals and the color signals into properly modulated video is not included as it is readily available from other sources.

POSSIBLE EMBELLISHMENTS

The approach shown in this application note is capable of sustaining a continuous data rate from the memory of over 14M nibbles/second when accessed byte parallel. The serializer circuitry could be reversed to provide a similar data rate to the memory. Also, by going to a wider data path to the memory even higher data rates could be achieved. (A bit wide memory could run at over 14Mbytes/second.) These higher bandwidths can be achieved with little if any increase in the complexity of the control circuitry and minimal increase in the cost of the data buffering. Also, the bandwidth obtained with the approach shown was limited by the display requirements and not by the IMS2600 or the control circuitry. It is worth noting that a new address is loaded into the IMS2600 every 560ns, and that this address could be any random address and the data rate would be maintained.

ANALYSIS OF THE ALTERNATIVES

There are two methods that might be considered as alternatives to "nibble mode" that are worth looking at here. Page mode is one of these alternatives. However, there are several problems that are encountered when trying to use eight 64Kx1 DRAMs with page mode in this design:

1) None of the currently available 64K DRAMs have a "page mode" cycle time that is fast enough to allow the necessary data rate.
2) The 640x200 screen format is not compatible with "page mode" because only 512 pixels can be accessed before a new page must be accessed. The only alternative would be to add four more memory devices and access them 12 bits at a time. But,
3) "page mode" is not compatible with the linear addressing generated by the 6845, and
4) 12 bit accesses create a problem when accessing from the CPU, and
5) the spec. limit for $\overline{RAS}$ active is usually 10μs but the display requires that $\overline{RAS}$ be active for 44.8μs if "page mode" is used, and
6) the RAMs would not automatically be refreshed by display accesses so a special refresh circuit would have to be added, and
7) the control gets more complicated, the data flow gets more complicated, etc.

The other approach that might be tried is to use 16Kx4 DRAMs. There are two methods that could be used and both of them would "work." The first method would be to access all eight 16Kx4's in parallel. This would give 8 pixels at a time so they would only have to cycle once every 500ns (no problem). However, if 32 bits are fetched at a time the serialization problem gets *much* more complex. There is also a problem with demultiplexing the 8 bits of CPU data onto the 32 bit memory data bus. So even though this technique "works" it is a very costly solution.

The problems with the wide data path can be overcome by interleaving the 16Kx4's as four rows of two memories each. This allows the data path to be no more complex than the one shown in this design. However, the interleaving requires a much more complex memory timing control in that it would be necessary to generate four $\overline{RAS}$'s and four $\overline{CAS}$'s and four $\overline{OE}$'s. It would also be likely that the address multiplexing could not be shared among all the memories because there is a high probability that one row of memories would be strobing in its row addresses while another row of memories would be strobing in its column addresses. Even though all of this is "practical" it does seem kind of ridiculous to spend a lot of effort trying to make eight 16Kx4's look like eight IMS2600's.

CONCLUSION

This application note has demonstrated that "nibble mode" is a useful feature of the IMS2600 and can be easily applied to solving real problems. It has also shown that in high bandwidth applications, the design solution achieved with "nibble mode" can be much more efficient than the "solutions" afforded by other commonly used approaches.

IMS1420
IMS1421
Bus Contention Considerations

Application Note #5

Utilization of IMS1420/21 on a Common I/O Bus

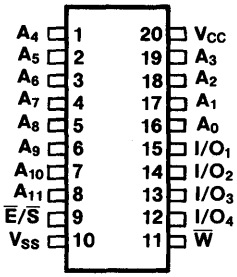


Figure 1: IMS1420/1421 Pin Configuration

The IMS1420/1421 conforms to the industry standard 20-pin package configuration for 4Kx4 static RAMs (See Figure 1). This pinout uses a common I/O data bus and like all common I/O devices, contention problems may occur unless the bus is carefully managed. Bus contention occurs when two (or more) devices with opposing output states are simultaneously enabled on the same line. If one device is attempting to output a high level (sourcing) and the other is attempting to output a low level (sinking), high current levels can flow during the driver conflict. Even short intervals of contention can cause system problems. This is due to the system noise resulting from the large peak transient currents associated with the multiple devices driving the same bus. Contention currents can be destructive and even if immediate destruction does not occur, extended periods of bus contention can impact long-term device reliability. Therefore, to avoid unpredictable system behavior due to high noise levels or damage to the system components, bus contention should be avoided whenever possible.

IMS1420/1421 OUTPUT CONTROL

Common I/O data bus contention can be avoided with the IMS1420/1421 static RAM by using the two control functions, Chip Enable ($\overline{E}/S$) and Write Enable ($\overline{W}$). The output data buffers are enabled only when $\overline{E}/S$ is low (active) and $\overline{W}$ is high (inactive). Under all other conditions the output buffers are disabled (See Figure 2). This

TRUTH TABLE

$\overline{E}/S$	$\overline{W}$	OUTPUT BUFFER
0	0	DISABLED
0	1	ENABLED
1	0	DISABLED
1	1	DISABLED

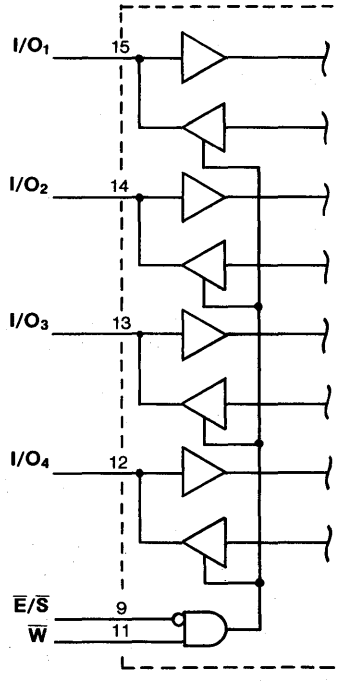
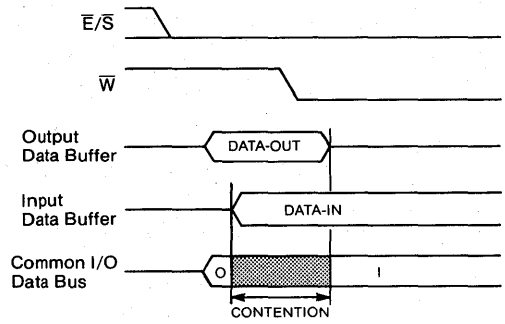
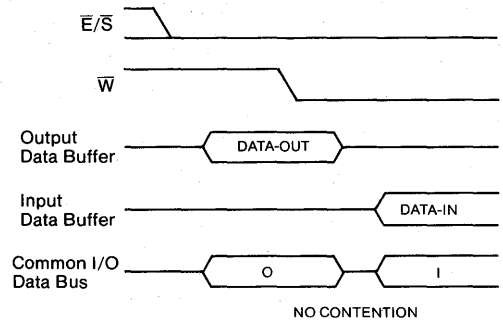


Figure 2: IMS1420/1421 I/O Buffer Enable Conditions



(a) Data-In Enabled Prior to Disabling Data-Out



(b) Data-In Enabled After Disabling Data-Out

Figure 3

two-line control provides considerable versatility to the system designer and allows several different write cycle modes of operation.

IMS1420/1421 DATA-IN SETUP CONTENTION CONSIDERATIONS

Bus contention can exist during a write cycle where $\overline{E}/\overline{S}$ has been low for some time prior to the falling edge of $\overline{W}$. In this case, the falling edge of $\overline{W}$ is used to turn off the data-out buffers of the RAM ($\overline{W}$-initiated write cycle). As shown in Figure 3, contention can occur unless sufficient time is allowed for the data-out buffers to be turned off. This must occur prior to the earliest time that the data-in buffers start driving the common I/O data bus. The time delay for safe operation between turning off the RAM output buffer and the turning on of the data-in buffer is dependent on the specification of the device used, system timing, and system design.

Bus contention can be avoided by asserting the $\overline{W}$ control signal prior to the $\overline{E}/\overline{S}$ signal ($\overline{E}/\overline{S}$-initiated write cycle) as shown in Figure 4. If $\overline{E}/\overline{S}$ goes low after $\overline{W}$ goes low, the memory output buffer will remain in the high impedance state during the write cycle.

IMS1420/1421 DATA-HOLD CONTENTION CONSIDERATIONS

Data contention can also occur at the end of the write cycle as shown in Figure 5. A contention condition exists if $\overline{W}$ goes high (inactive) while $\overline{E}/\overline{S}$ is still low ($\overline{W}$-terminated write cycle) and the addresses are changed when the data-in is still enabled (See Figure 5a). Contention can also exist if $\overline{W}$ goes high (inactive), $\overline{E}/\overline{S}$ remains low (active), addresses remain stable, and data-in changes

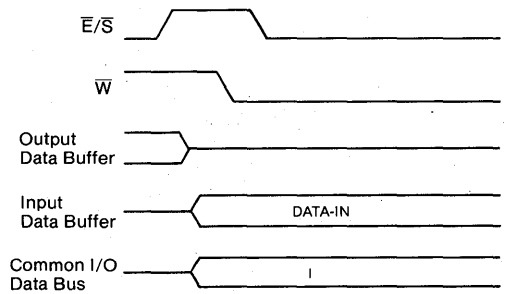


Figure 4: $\overline{E}/\overline{S}$ Used to Control Output Buffer (No Contention)

after the specified hold time. This condition is shown in Figure 5b. If the addresses and data-in do not change, contention will not occur at the end of the write cycle, since the data being read out is identical to the data-in on the bus. If a write cycle is terminated by pulling $\overline{E}/\overline{S}$ high (inactive) prior to $\overline{W}$ going high (inactive), the data output buffer of the IMS1420/1421 will remain in the high impedance state. This eliminates contention concerns during data-in hold time (See Figure 5c).

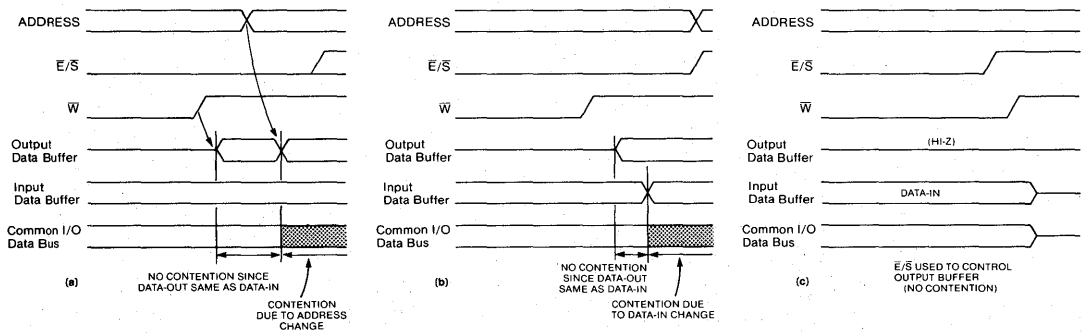
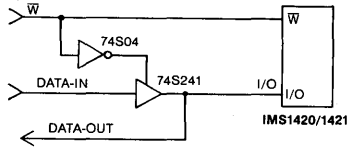


Figure 5



(One of Four I/O Drivers Shown)

Timing Calculations

Time to Disable RAM (t_{WZ})	Maximum 1420-45 −55 −70 20ns 25ns 35ns
Time to Enable Data-In Buffer $\overline{W}\downarrow$ to 74S04↑ 74S04↑ to D(ON)	Minimum 1.5ns 4.0ns 5.5ns
Maximum Contention Duration Max. Disable RAM Min. Enable 74S241	Maximum 1420-45 −55 −70 20.0ns 25.0ns 35.0ns 5.5ns 5.5ns 5.5ns 14.5ns 19.5ns 29.5ns

Figure 6: Typical Application Illustrating I/O Bus Contention

UNAVOIDABLE CONTENTION CONSIDERATIONS

Although the IMS1420/1421 offers sufficient control of the data-out buffers, bus contention is unavoidable in many speed critical applications. This is particularly true when system timing is tight and the device is continuously enabled ($\overline{E}/\overline{S}$ grounded) or when the system write strobe is valid late in the memory cycle. Under such conditions, the write cycle is controlled by the $\overline{W}$ control function ($\overline{W}$-initiated write cycle). Additionally, there may not be adequate time to delay the enabling of the data-in buffer in order to avoid bus contention.

In this type of application, a variation of the circuit shown in Figure 6 is commonly used. As shown in the figure, worst-case contention intervals from 15 to 30ns (or more) are common. Even though the contention duration is short, current per I/O line can be extremely high (See Figure 7). The worst-case current magnitude is dependent on the short circuit characteristics of the driver used. Regardless, contention current levels can cause undesirable effects if not limited.

Figure 8 illustrates a technique that can be used to limit contention currents to approximately 30mA. The contention duty cycle should be minimized even when the current is limited to 30mA per I/O line. Use of the series limiting resistors on each I/O line has an insignificant impact on the data-in levels since the input buffers of the IMS1420/1421 are high impedance with input

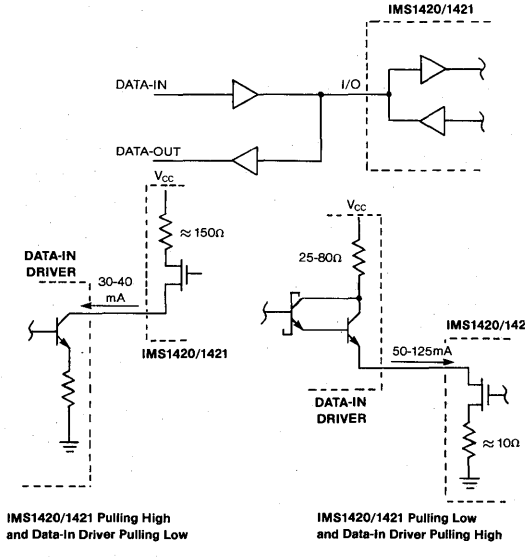


Figure 7: High Contention Current During Driver Conflict

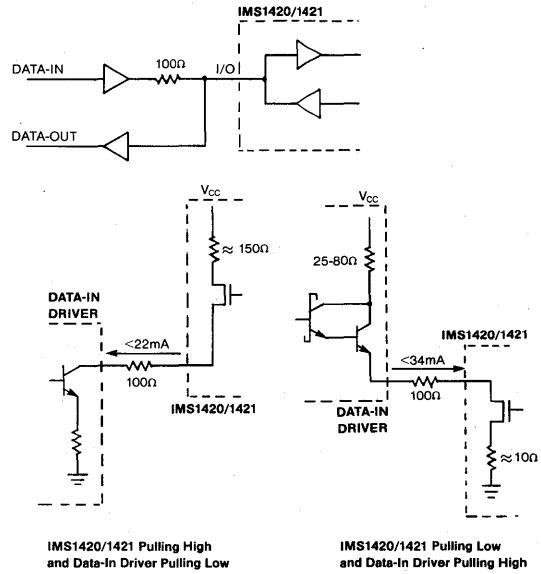


Figure 8: Current Limited During Driver Conflict

current limited to leakage current (10μA maximum). However, since the I/O terminals have capacitance (7pF maximum) and board interconnect traces also have capacitance, the use of the series current-limiting resistor forms an RC network and has a small impact on data-in valid time. Figure 9 and 10 show the worst-case calculations of speed loss due to the RC components. The time penalties shown must be added to the point that bus contention ceases. Calculations are shown for system organizations as deep as 16K (4 IMS1420/1421 connected to a common I/O Bus).

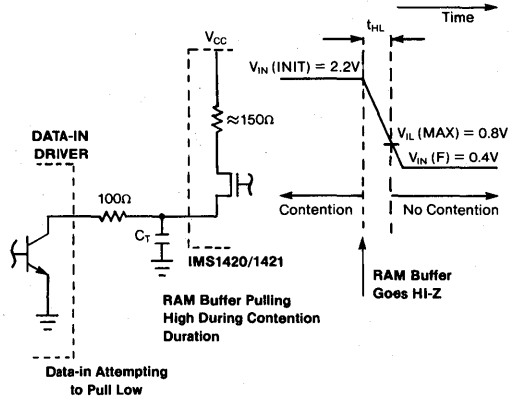
IMS1420/1421 POWER-UP FAIL-SAFE CIRCUITRY

When power is first applied to the IMS1420/1421, an on-chip circuit forces the device into a low power standby mode and the $\overline{E}/\overline{S}$ control signal is inhibited. This power-up disable sequence not only limits start-up currents by forcing a standby condition, but also, via the

$\overline{E}/\overline{S}$ inhibit, prevents bus contention caused by the IMS1420/1421 output buffers turning on during system power-up.

SUMMARY

Bus contention can occur with devices using common I/O. The IMS1420/1421 provides control functions such that bus contention can be avoided. Bus contention should always be avoided whenever possible; but if it can't be avoided, the duration of multiple driver overlap should be minimized and current should be limited to a safe level.



$$t_{HL} = \tau\, ln\left[\frac{V_{IN}(INIT) - V_{IN}(F)}{V_{IL}(MAX) - V_{IN}(F)}\right]$$

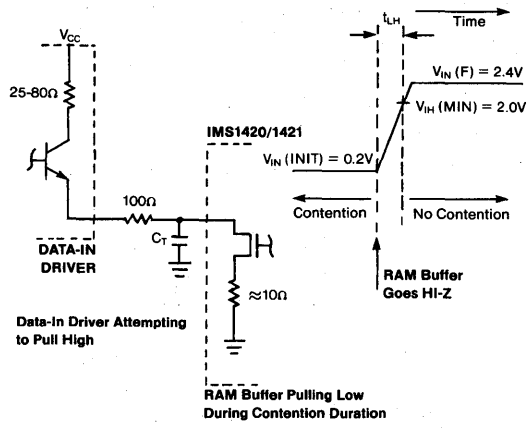
$$t_{HL} = \tau\, ln\left[\frac{2.2 - 0.4}{0.8 - 0.4}\right] = \tau\, ln\ [4.5]$$

$$t_{HL} = 1.5\tau$$

Time Penalty	
1 RAM	1.4ns
2 RAMS	2.7ns
3 RAMS	4.0ns
4 RAMS	5.4ns

Using: $C_{I/O}$ (RAM) = 7pF & C (Board)/RAM = 2pF, C_T = 9pF/RAM

Figure 9: Time Penalty (t_{HL}) Due to Limiting Resistor



$$t_{LH} = \tau\, ln\left[\frac{V_{IN}(F) - V_{IN}(INIT)}{V_{IN}(F) - V_{IH}(MIN)}\right]$$

$$t_{LH} = \tau\, ln\left[\frac{2.4 - 0.2}{2.4 - 2.0}\right] = \tau\, ln\ [5.5]$$

$$t_{LH} = 1.7\tau$$

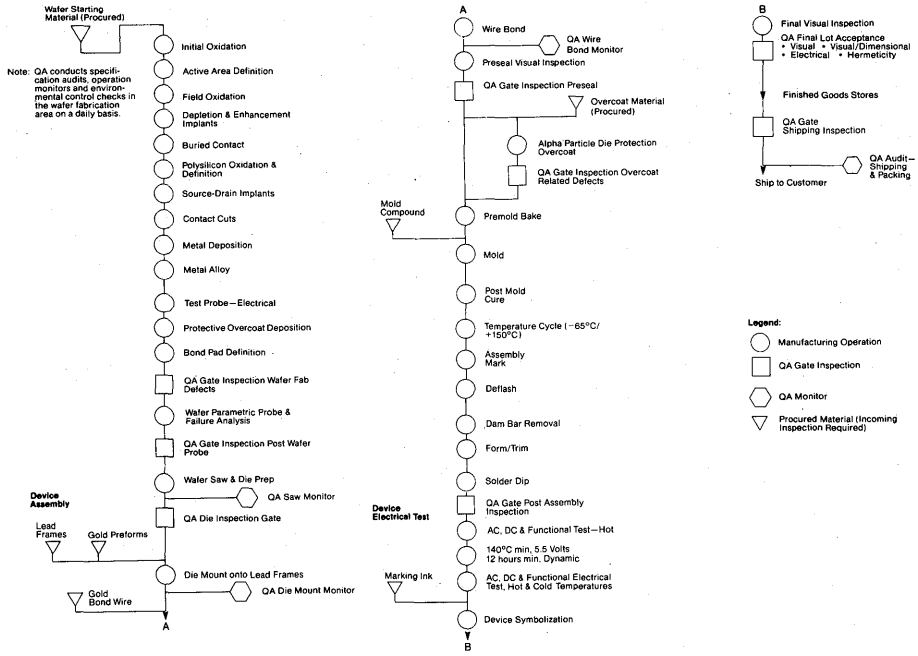
Time Penalty	
1 RAM	1.5ns
2 RAMS	3.1ns
3 RAMS	4.6ns
4 RAMS	6.1ns

Using: $C_{I/O}$ (RAM) = 7pF & C (Board)/RAM = 2pF, C_T = 9pF /RAM

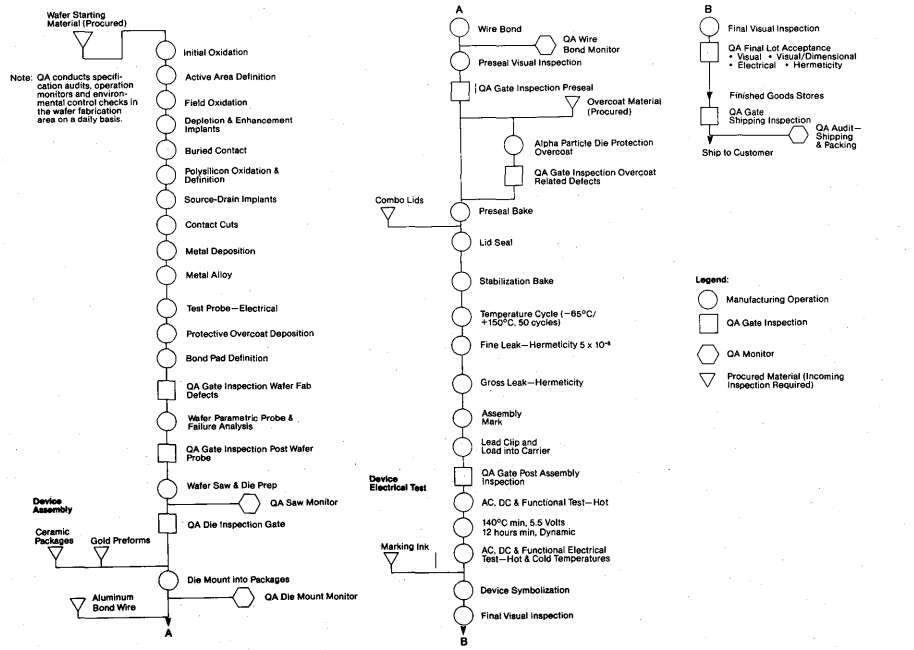
Figure 10: Time Penalty (t_{LH}) Due to Limiting Resistor

Quality/Reliability 7

FLOW DIAGRAM—STANDARD PLASTIC



FLOW DIAGRAM—STANDARD CERAMIC



INMOS quality & reliability

The INMOS Quality Program is set up to be attentive to every phase of the semiconductor product life cycle. This includes specific programs in each of the following areas:

- Design in quality
- Document control
- Incoming inspection
- Comprehensive new product qualification
- Ongoing quality and reliability monitors
- Thorough production testing and quality monitor procedure
- Continual quality and reliability improvement

In this section these programs will be discussed in some detail.

Design in quality & reliability

The INMOS Quality Program begins with the design of new INMOS products. The following procedures are examples from the INMOS program to design quality and reliability into every product.

INMOS products are designed to have parametric margins beyond the product target specifications. The design performance is verified using simulations of circuit performance over voltage and temperature values beyond those of specified product operation, including verification beyond the military performance range. In addition, the device models are chosen to ensure tolerance to wide variations in process parameters beyond those expected in manufacture.

The design process includes consideration of quality issues such as signal levels available for sensing, reduction of internal noise levels, stored data integrity (i.e., cell capacitance in DRAMs and stability of SRAM cells), and testability of all device functions. Electrostatic damage protection techniques are included in the design with input protection goals of 2K volts for MIL-STD-883 testing methods. Specific customer requirements can be met by matching their detailed specifications against INMOS designed-in margins.

Document control

The Document Control Department maintains control over all manufacturing specifications, lot travelers, procurement specifications and drawings, reticle tapes and test programs. New specifications and changes are subject to approval by the Engineering and Manufacturing managers.

Document Control also has responsibility for controlling in-line documentation in all manufacturing areas which includes distribution of specifications, control of changes and liaison with production control and manufacturing in introducing changed procedures into the line.

Incoming material inspection

Vendors wishing to supply materials used in the manufacture of INMOS products are screened to ensure that their product meets the INMOS specification. Only those that meet INMOS requirements are included in the Qualified Vendors List. All direct materials including wafers, packages, lids, bond wire, eutectics, chemicals, masks and reticles received at each location are passed to the QA Incoming Inspection department.

Stringent testing is done on all memory materials. Tests on wafers include visual, dimensional, resistivity, topography, polarity and crystal defect. Tests on packages include plating characteristics, leakage, bake and solderability.

The QA Analytical Chemistry Laboratory checks incoming acids, solvents, gasses and photoresists using the latest analytical techniques and equipment. Incoming chemicals for use in the fabrication area, the incoming water and the deionized water supplies are characterized daily.

Reticles and masks are inspected on high resolution photomask inspection systems designed to meet the needs of VLSI circuits. Reticles and masks passing initial QA inspection are then subjected to an in-line qualification procedure before being released for use on production wafers.

Internal product qualification

INMOS performs a thorough internal product qualification prior to the delivery of any new product, other than engineering samples or prototypes, to customers.

Care is taken to select a representative sample from the final prototype material. This typically consists of 300 units from a minimum of three different production lots. Testing is then done to assure the initial product reliability levels that are required. Product qualifications are done in accordance with MIL-STD-883, methods 5004 and 5005, or CECC/BS9000.

Product monitors

Product monitors

To ensure the PAM and Failure Rate levels required by today's users, a statistically significant sample needs to be taken continuously over time. Two of the programs that INMOS uses to accomplish this are the Finished Goods Audit (FGA) and the Product Monitoring Program (PMP).

In the FGA program, random samples are pulled from finished goods, that is, products that have passed all test and QA points. Any rejected lots are 100% retested. But, more importantly, each failure is analyzed and corrective actions identified to prevent recurrence of that specific problem.

The Product Monitoring Program is a comprehensive ongoing program of reliability testings. A small sample is pulled from production lots of a particular part type. Tests run in this program include: extended temperature operating life, EMG testing, soft error rate testing, 85°C/85% R.H./5.5V temperature/humidity/bias (THB), and SEM monitoring temperature cycle.

Device testing

Device testing

Electrical testing at INMOS begins while the devices are still in wafer form before being divided into individual die.

Defective circuits are identified so they may be later discarded after the wafer has been separated into individual die. This test fully exercises the circuits for all AC and DC datasheet parameters in addition to verifying functionality.

After the passing circuits have been assembled into packages they are again tested in our Final Test operation. In a mature product the typical flow is:

Preburn-In testing
Burn-In
Final testing (Hot)
Final testing (Cold)

Quality improvement programs

In order to achieve its goal as an industry leader in the quality and reliability of its products, INMOS has put in place specific programs to address quality issues throughout the company. Strategic quality and reliability objectives are established for the company by a Quality Steering Committee which includes representatives from the executive offices. A tops-down program for the education of all levels of management and staff in the techniques of management for quality has been put in place.

Failure analysis

Failure analysis

The role of Failure Analysis is to determine the cause-and-effect relationship in rejects and to affect corrective actions and/or appropriate controls. Tools used by Failure Analysis include component testers with both schmoo plot and real time bit map capabilities, in-circuit microprobers, standard electrical bench equipment (curve tracers, oscilloscopes, pulse generators, digital power supplies, break-out boxes, etc.), optical microscopes, scanning electron microscopes, electron beam chemical analysis (e.g., EDX, scanning auger), wet chemical and plasma techniques for "deprocessing" devices, and metallurgical sectioning equipment.

Two of the most powerful tools used in the analysis of functional failures are real time bit mapping and schmoo plots. Real time bit mapping allows an analyst to see an image of the device, displays the dependence of the functional failure with respect to the memory array's layout (topological bit map) or with respect to the electrical addresses applied to the device (electrical bit map).

Scanning electron microscopes (SEMs) are primarily employed to visualize the artifacts of a failure mechanism.

Advancing fabrication and assembly technology is forcing the application and development of plasma techniques in deprocessing assembled devices. Depending on the desired end, the combinations and types of materials being put into use in the manufacture of components today may be unyielding to the traditional wet chemical methods of deprocessing and/or disassembly needed for component failure analysis.

General Information 8

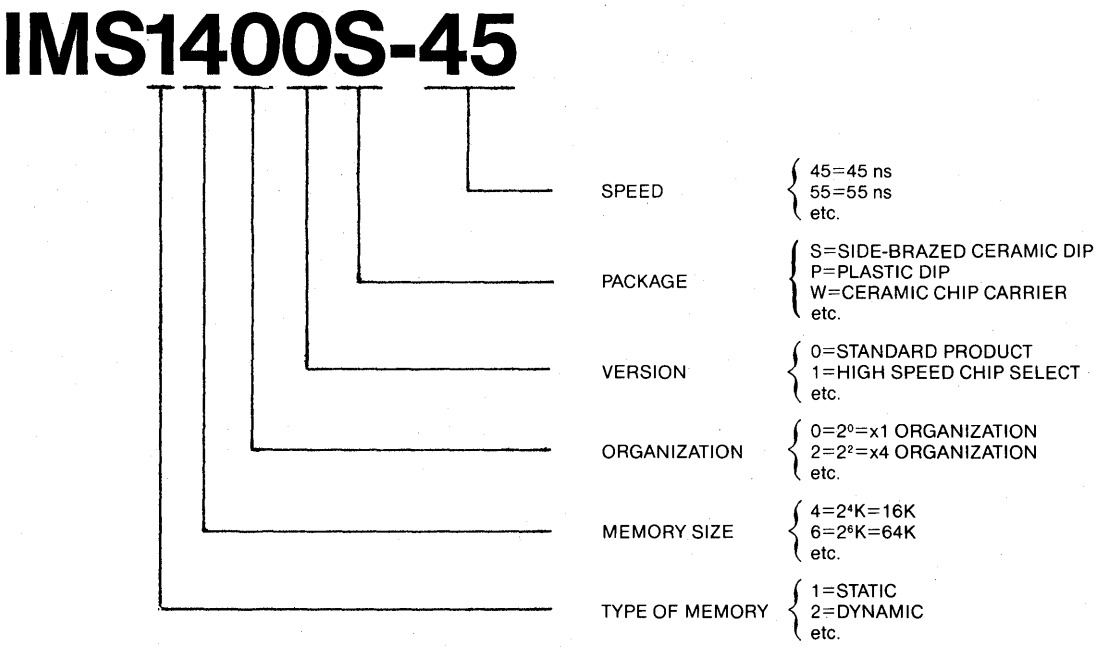
Numbering Scheme

INMOS MEMORIES NUMBERING SCHEME

In an industry plagued by part numbers that don't make a lot of sense, Inmos offers a numbering scheme that makes it easy to identify its memory products.

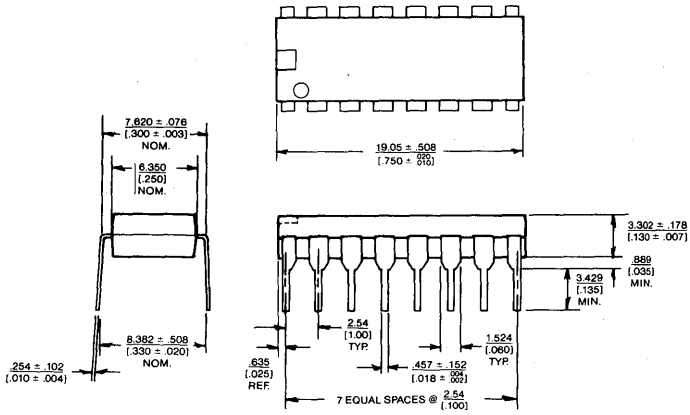
Other static rams include the IMS1420 and IMS1423. The "2" indicates a "x 4" organization. Since the memory size is 16K (2^4), the devices are 4K x 4. The difference between the two devices is the high-speed chip-select feature. Dynamic memory begins with a "2", as demonstrated by the IMS2600. Its memory size is 2^6K, or 64K. Since its organization digit is a "0", it is a 2^0, or "x 1" organization. Its last digit is a "0", designating it as the standard version.

Speed is specified by the dash number. For statics, the two-digit number is the chip-enable access time in nanoseconds. For dynamics, the chip access time is indicated by the two most significant digits. Thus, the IMS2600-12 would have an access time of 120 nanoseconds.

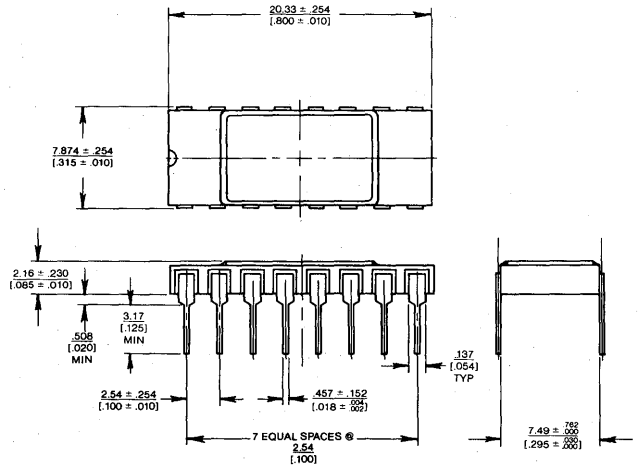


Packaging Information

16 PIN PLASTIC DUAL-IN-LINE

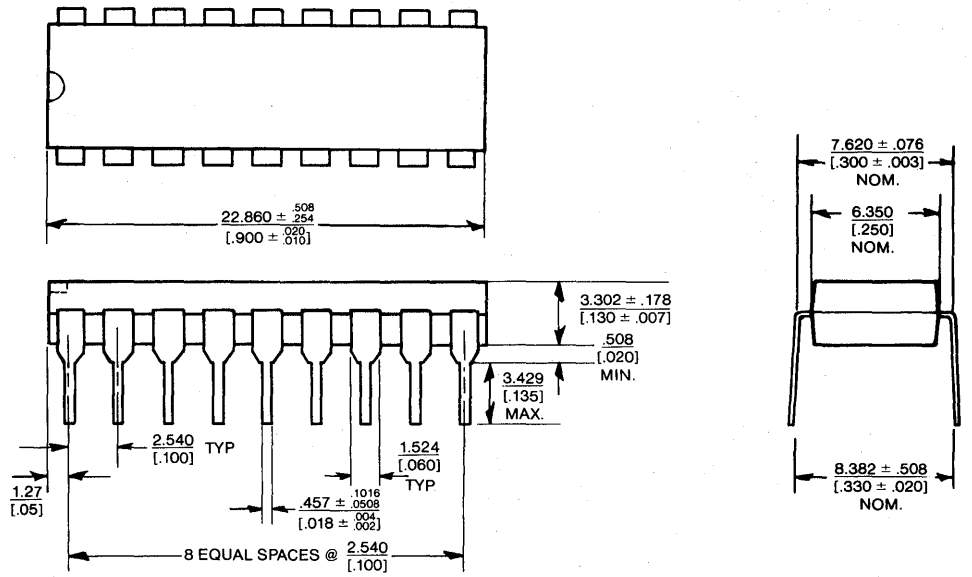


16 PIN CERAMIC DUAL-IN-LINE

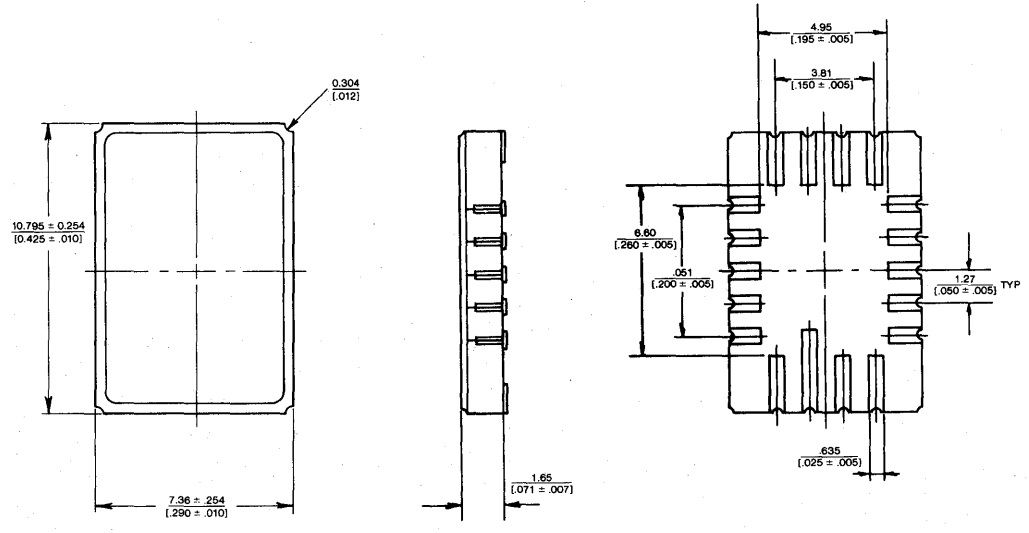


General Information

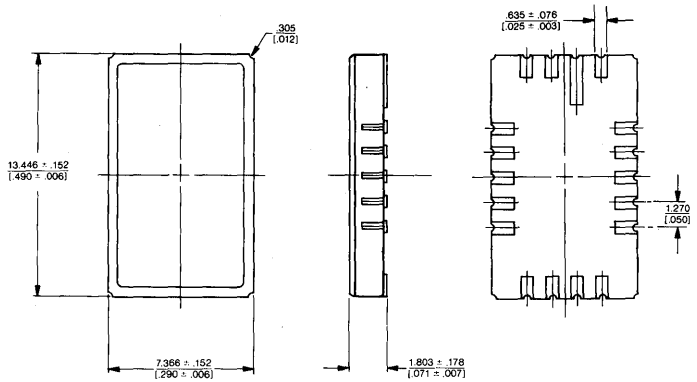
18 PIN PLASTIC DUAL-IN-LINE



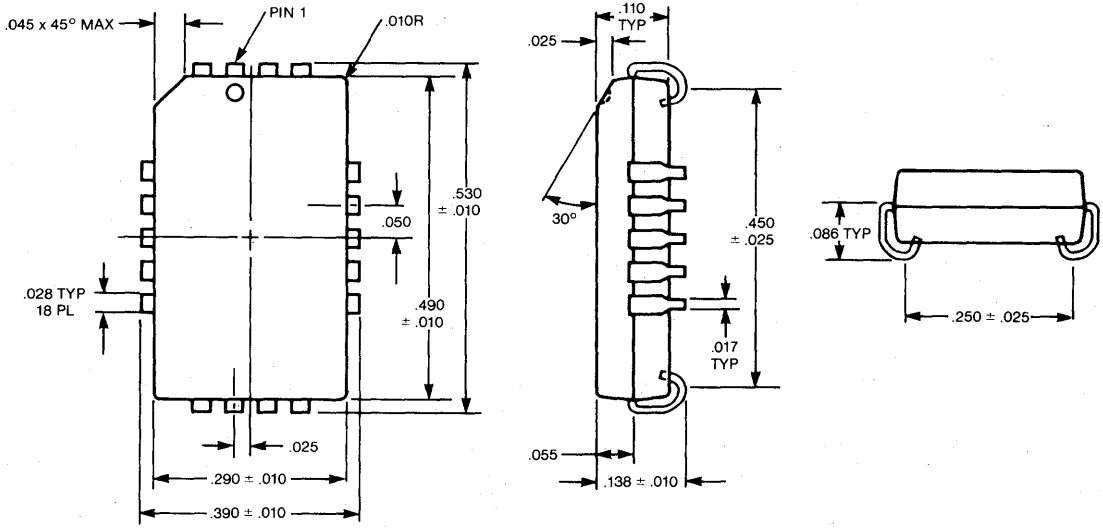
18 PIN CERAMIC LEADLESS CHIP CARRIER (A)



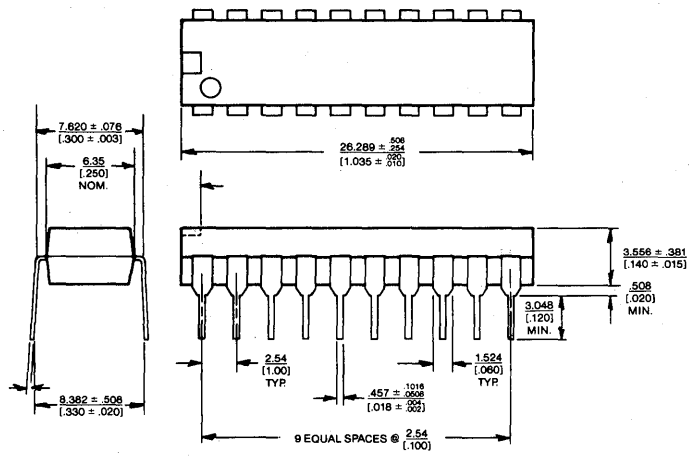
18 PIN CERAMIC LEADLESS CHIP CARRIER (B)



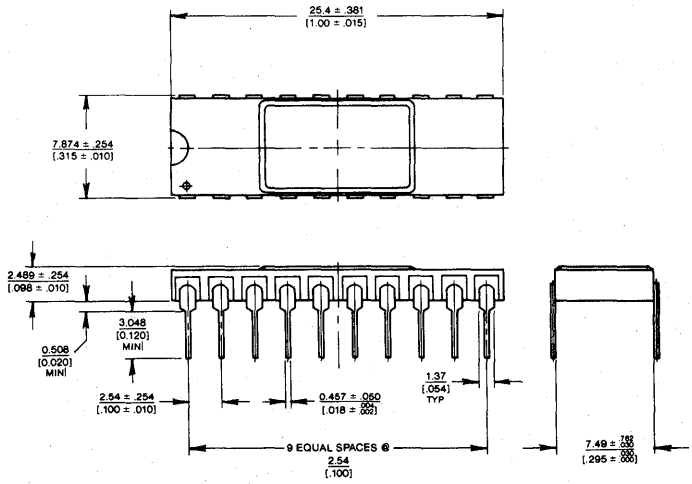
18 PIN PLASTIC CHIP CARRIER



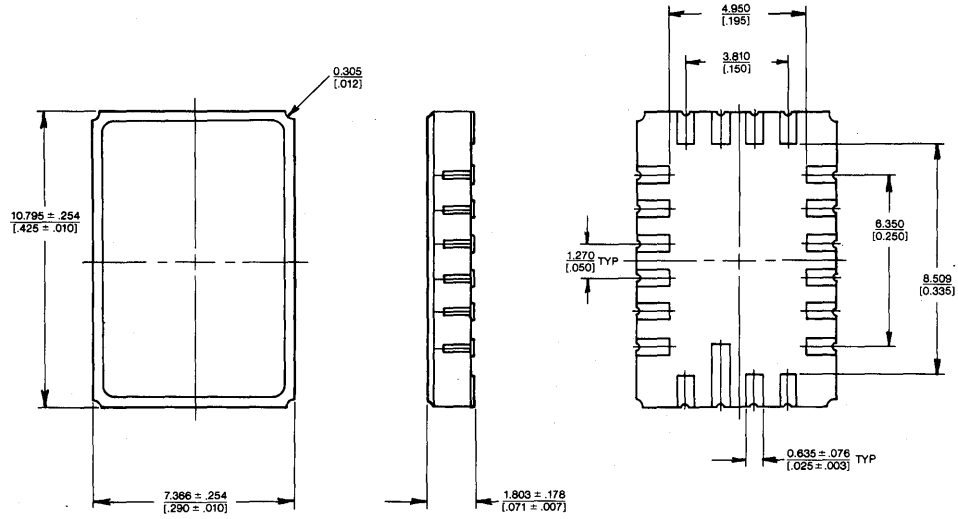
20 PIN PLASTIC DUAL-IN-LINE



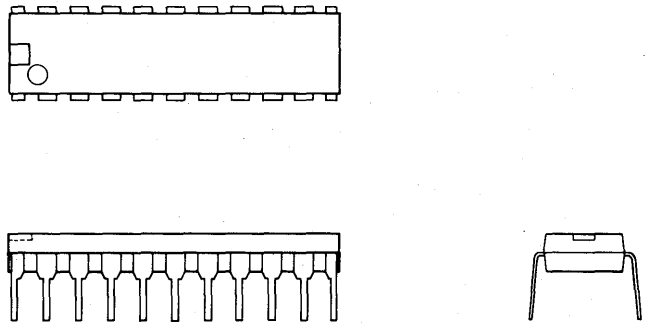
20 PIN CERAMIC DUAL-IN-LINE



20 PIN CHIP CARRIER

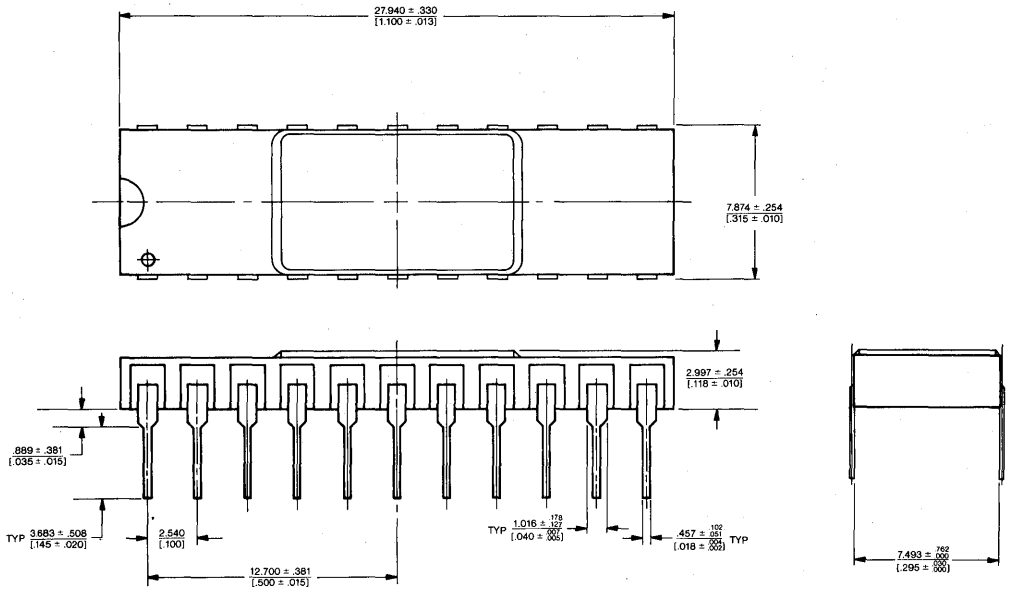


22 PIN PLASTIC DUAL-IN-LINE

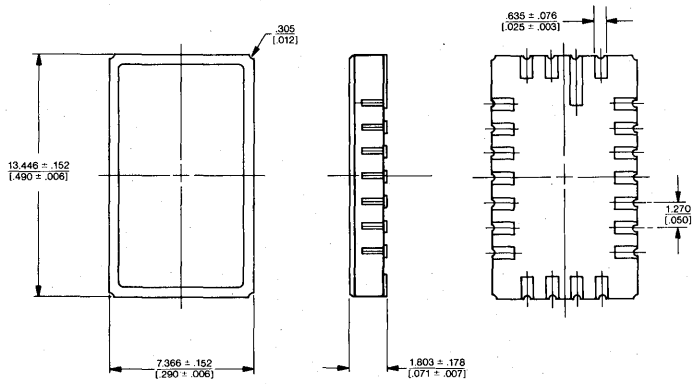


Specifications not available at time of publication.

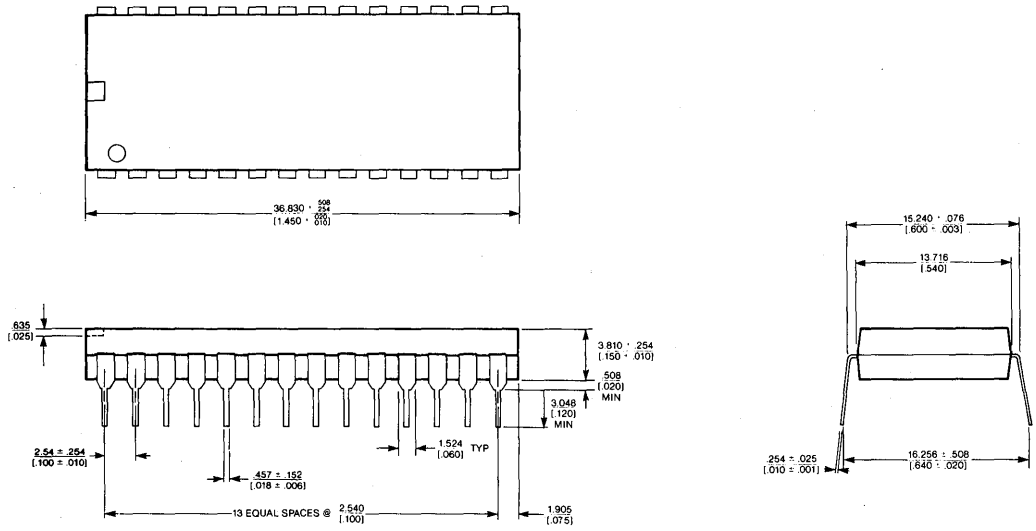
22 PIN CERAMIC DUAL-IN-LINE



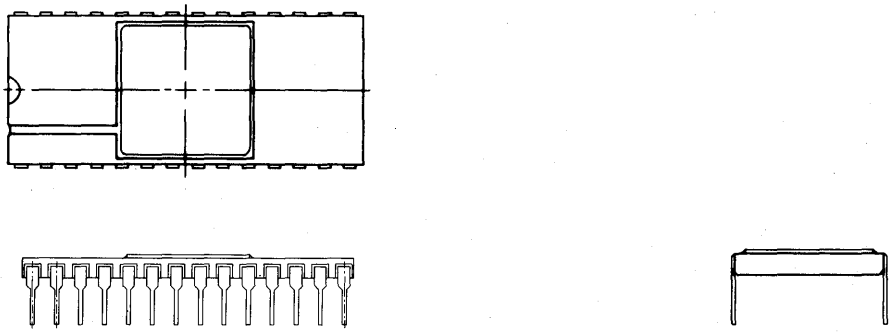
22 PIN CHIP CARRIER



28 PIN PLASTIC DUAL-IN-LINE



28 PIN CERAMIC DUAL-IN-LINE



Specifications not available at time of publication.

Conversion Tables

1. Convert Hexadecimal to Decimal

$1AF6_{16} = 1 \times 16^3 + A \times 16^2 + F \times 16^1 + 6 \times 16^0 = 4096 + 2560 + 240 + 6 = 6902_{10}$

2. Convert Octal to Decimal

$2147_8 = 2 \times 8^3 + 1 \times 8^2 + 4 \times 8^1 + 7 \times 8^0 = 1024 + 64 + 32 + 7 = 1127$

3. Convert Binary to Decimal

$101101_2 = 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 32 + 0 + 8 + 4 + 1 = 45_{10}$

4. Convert Decimal to Hexadecimal

1207_{10} → $16^3 \mid 1207$ quotient 0, remainder 1207 → $16^2 \mid 1207$ quotient 4, remainder 183 → $16^1 \mid 183$ quotient B, remainder 7 → $16^0 \mid 7$ quotient 7, remainder 0 = $4B7_{16}$

5. Convert Decimal to Octal

153_{10} → $8^2 \mid 153$ quotient 2, remainder 25 → $8^1 \mid 25$ quotient 3, remainder 1 → $8^0 \mid 1$ quotient 1, remainder 0 = 231_8

6. Convert Decimal to Binary

53_{10} → $2^5 \mid 53$ quotient 1, remainder 21 → $2^4 \mid 21$ quotient 1, remainder 5 → $2^3 \mid 5$ quotient 0, remainder 5 → $2^2 \mid 5$ quotient 1, remainder 1 → $2^1 \mid 1$ quotient 0, remainder 1 → $2^0 \mid 1$ quotient 1, remainder 0 = 110101_2

Recommended Decimal Multiples and Submultiples

Multiples and Submultiples	Prefixes	Symbols
10^{18}	exa	E
10^{15}	pecta	P
10^{12}	tera	T
10^{9}	giga	G
10^{6}	mega	M
10^{3}	kilo	k
10^{2}	hecto	h
10	deca	da
10^{-1}	deci	d
10^{-2}	centi	c
10^{-3}	milli	m
10^{-6}	micro	μ (greek mu)
10^{-9}	nano	n
10^{-12}	pico	p
10^{-15}	femto	f
10^{-18}	atto	a

Conversion Tables (cont.)

Constants and Conversion Factors

Conversion Factors—General

To Obtain	Multiply	By
Degree (angle)	Radians	57.2958
Ergs	Foot-pounds	1.356×10^{7}
Feet	Miles	**5280.**
Feet of water @ 4°C	Atmospheres	33.90
Foot-pounds	Hosepower-hours	1.98×10^{6}
Foot-pounds	Kilowatt-hours	2.655×10^{6}
Foot-pounds per min.	Horsepower	3.3×10^{4}
Horsepower	Foot-pounds per sec.	1.818×10^{-3}
Inches of mercury @ 0°C	Pounds per square inch	2.036
Joules	BTU	1054.8
Joules	Foot-pounds	1.35582
Kilowatts	BTU per min.	1.758×10^{-2}
Kilowatts	Foot-pounds per min.	2.26×10^{-5}
Kilowatts	Horsepower	0.745712
Knots	Miles per hour	0.86897624
Miles	Feet	1.894×10^{-4}
Nautical miles	Miles	0.86897624
Radians	Degrees	1.745×10^{-2}
Square feet	Acres	**43560.**
Watts	BTU per min.	17.5796

Temperature Factors

$°F = 9/5(°C) + 32$

Fahrenheit temperature -1.8 (temperature in kelvins) -459.67

$°C = 5/9\ [(°F) - 32]$

Celsius temperature = temperature in kelvins -273.15

Fahrenheit temperature = 1.8 (Celsius temperature) $+32$

***Boldface numbers are exact; others are given to ten significant figures where so indicated by the multiplier factor.**

Conversion Factors—Metric to English

To Obtain	Multiply	By
Inches	Centimeters	0.3937007874
Feet	Meters	3.280839895
Yards	Meters	1.093613298
Miles	Kilometers	0.6213711922
Ounces	Grams	$3.527396195 \times 10^{-2}$
Pounds	Kilograms	2.204622622
Gallons (U.S. Liquid)	Liters	0.2641720524
Fluid ounces	Milliliters (cc)	$3.381402270 \times 10^{-2}$
Square inches	Square centimeters	0.1550003100
Square feet	Square meters	10.76391042
Square yards	Square meters	1.195990046
Cubic inches	Mililiters (cc)	$6.102374409 \times 10^{-2}$
Cubic feet	Cubic meters	35.31466672
Cubic yards	Cubic meters	1.307950619

Conversion Tables (cont.)

Conversion Factors—English to Metric*

To Obtain	Multiply	By
Microns	Mils	**25.4**
Centimeters	Inches	**2.54**
Meters	Feet	**0.3048**
Meters	Yards	**0.9144**
Kilometers	Miles	**1.609344**
Grams	Ounces	28.34952313
Kilograms	Pounds	**0.45359237**
Liters	Gallons (U.S. Liquid)	**3.785411784**
Mililiters (cc)	Fluid ounces	29.57352956
Square centimeters	Square inches	**6.4516**
Square meters	Square feet	**0.09290304**
Square meters	Square yards	**0.83612736**
Mililiters (cc)	Cubic inches	**16.387064**
Cubic meters	Cubic feet	$2.831684659 \times 10^{-2}$
Cubic meters	Cubic yards	0.764554858

Conversion Factors—General*

To Obtain	Multiply	By
Atmospheres	Feet of water @ 4°C	2.950×10^{-2}
Atmospheres	Inches of mercury @ 0°C	3.342×10^{-2}
Atmospheres	Pounds per square inch	6.804×10^{-2}
BTU	Foot-pounds	1.285×10^{-3}
BTU	Joules	9.480×10^{-4}
Cubic feet	Cords	**128.**

***Boldface numbers are exact; others are given to ten significant figures where so indicated by the multiplier factor.**

Miscellaneous Constants

Physical Constants

Equatorial radius of the earth = 6378.388 km = 3963.34 miles (statute).
Polar radius of the earth, 6356.912 km = 3949.99 miles (statute).
1 degree of latitude at 40° = 69 miles.
1 international nautical mile = 1.15078 miles (statute) = 1852 m = 6076.115 ft.
Mean density of the earth = 5.522 g/cm^3 = 344.7 lb./ft.^{3}
Constant of gravitation, $(6.673 \pm 0.003) \times 10^{-8}$ cm^3 gm^{-1} S^{-2}
Acceleration due to gravity at sea level, latitude 45° = 980.665cm/s^2 = 32.1740 ft./sec^2.
Length of seconds pendulum at sea level, latitude 45° = 99.3574 cm = 39.1171 in.
1 knot (international) = 101.269 ft./min. = 1.6878 ft./sec. = 1.1508 miles (statute)/hr.
1 micron = 10^{-4} cm.
1 angstrom = 10^{-8} cm.
Mass of hydrogen atom = $(1.67339 \pm 0.0031) \times 10^{-24}$ g.
Density of mercury at 0°C = 13.5955 g/mi.
Density of water at 3.98°C = 1.000000 g/mi.
Density, maximum, of water, at 3.98°C = 0.999973 g/cm^3.
Density of dry air at 0°C, 760 mm = 1.2929 g/liter.
Velocity of sound in dry air at 0°C = 331.36 m/s—1087.1 ft./sec.
Velocity of light in vacuum = $(2.997925 \pm 0.000002) \times 10^{-10}$ cm/s.
Heat of fusion of water 0°C = 79.71 cal/g.
Heat of vaporization of water 100°C = 539.55 cal/g.
Electrochemical equivalent of silver 0.001118 g/sec. international amp.
Absolute wave length of red cadmium light in air at 15°C, 760 mm pressure = 6438.4696 A.
Wave length of orange-red line of krypton 86 = 6057.802 A.

INMOS Sales Offices

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San Jose
INMOS Sales
408-298-1786

Torrance
INMOS Sales
213-530-7764

GEORGIA
Atlanta
INMOS Sales
404-475-1936

MASSACHUSETTS
Westborough
INMOS Sales
617-366-4020

MARYLAND
Baltimore
INMOS Sales
301-995-0813

MINNESOTA
Minneapolis
INMOS Sales
612-831-5626

INTERNATIONAL
Paris, France
INMOS SARL
(1)-4687-2201

United Kingdom, Bristol
INMOS Limited
02-722-90861

West Germany
INMOS GmbH
Tel: 089-319-1028

INMOS Representatives

ALABAMA
Huntsville
Macro-Marketing Assoc.
205-883-9630

ARIZONA
Phoenix
Compass Marketing & Sales
602-996-0635

Tucson
Compass Marketing & Sales
602-293-1220

CALIFORNIA
Irvine
Centaur Corporation
714-261-2123

Santa Clara
Criterion Sales
408-988-6300

San Diego
Centaur Corporation
619-278-4950

San Diego
Hadden Assoc.
619-565-9444

Woodland Hills
Centaur Corporation
818-704-1655

COLORADO
Denver
Component Sales
303-779-8060

CONNECTICUT
Brookfield
Kanan Assoc.
203-775-0494

FLORIDA
Maitland
E.I.R., Inc.
305-660-9600

N. Lauderdale
E.I.R., Inc.
305-975-8718

GEORGIA
Norcross (Atlanta)
Macro-Marketing Assoc.
205-883-9630

ILLINOIS
Schaumburg (Chicago)
Micro-Tex
312-885-1131

INDIANA
Carmel
Giesting & Associates
317-844-5222

Indianapolis
Elec. Mktg. Consultants, Inc.
317-253-1668

KANSAS
Kansas City
B.C. Electronic Sales
913-342-1211

Wichita
B.C. Electronic Sales
316-722-0104

MASSACHUSETTS
Needham Heights
Kanan Assoc.
617-449-7400

MARYLAND
Severna Park (Baltimore)
New Era Sales
301-544-4100

MICHIGAN
Coloma
Giesting & Associates
616-468-4200

Farmington Hills
Giesting & Associates
313-478-8106

MINNESOTA
Edina (Minneapolis)
Mel Foster Tech Sales
612-941-9790

MISSOURI
St. Louis (Bridgeton)
B.C. Electronic Sales
314-291-1101

NORTH CAROLINA
Raleigh
CSR Electronics, Inc.
919-878-9200

NEW JERSEY
Teaneck (New York City)
R.T. Reid Assoc.
201-692-0200

NEW MEXICO
Albuquerque
Compass Marketing & Sales
505-888-0800

NEW YORK
Melville
R.T. Reid Assoc.
516-351-8833

Rochester
L-Mar Assoc.
716-323-1000

OHIO
Beachwood
E.S.I.
216-831-9555

Cincinnati
Giesting & Associates
513-385-1105

OKLAHOMA
Tulsa
B.P Sales
918-744-9964

OREGON
Portland
Westerberg & Assoc.
503-620-1931

PENNSYLVANIA
Huntingdon Valley (Philadelphia)
Knowles Assoc.
215-322-7100

TEXAS
Austin
B.P Sales
512-346-9186

Houston
B.P Sales
713-531-4144

Richardson (Dallas)
B.P Sales
214-234-8438

UTAH
Salt Lake City
Component Sales
801-268-8440

WASHINGTON
Bellevue (Seattle)
Westerberg & Assoc.
206-453-8881

WISCONSIN
Waukesha (Milwaukee)
Micro-Tex
414-542-5352

CANADA
Downsview, Ontario
Har-Tech Electronics
416-665-7773

Ottawa, Ontario
Har-Tech Electronics
613-230-8431

Pointe Claire (Montreal), Quebec
Har-Tech Electronics
514-694-6110

INTERNATIONAL
Australia
ACE Electronics Pty. Ltd.
02-2111144

Hong Kong
PALIMAX
5-468161
Extn 555

Italy, Milan
Cefra SRL
Tel: 392-235264

Japan, Tokyo
Matsushita Electric
Tel: 03-435-4501

Korea
TESS-KO Enterprises
02-7542454

Singapore
CALTRON (PTE) Ltd.
4567222

Taiwan
Helm Engineering
02-7091888

United Kingdom
Chichester, West Sussex
Hartech Limited
0243-773511

United Kingdom
Kirkmuirhill, Lanarkshire
Stuart Electronics
0555-892-393

United Kingdom
Marple Bridge, Cheshire
TC Electronics
061-427-2020

United Kingdom
Stevenage, Herts
Dexter Electronics
0438-65551

INMOS Distributors

ALABAMA
Huntsville
Arrow Electronics
205-837-6955

Huntsville
Pioneer-Standard
205-837-9300

ARIZONA
Phoenix
Wyle
602-866-2888

Tempe
Anthem Electronics
602-966-6600

Tempe
Arrow Electronics
602-968-4800

CALIFORNIA
Calabasas
Wyle
818-880-9001

Chatsworth
Anthem Electronics
213-700-1000

Chatsworth
Arrow Electronics
818-701-7500

El Segundo
Wyle
213-322-8100

Hayward
Arrow Electronics
415-487-4300

Irvine
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714-768-4444

Irvine
Wyle
714-863-9953

Irvine
Wyle (Military)
714-851-9953

Sacramento
Wyle
916-638-5282

San Diego
Anthem Electronics
619-453-4871

San Diego
Arrow Electronics
619-565-4800

San Diego
Wyle
619-565-9171

San Jose
Anthem Electronics
408-295-4200

Santa Clara
Wyle
408-727-2500

Sunnyvale
Arrow Electronics
408-745-6600

Tustin
Arrow Electronics
714-838-5422

COLORADO
Denver
Arrow Electronics
303-696-1111

Englewood
Anthem Electronics
303-790-4500

Thornton
Wyle
303-457-9953

CONNECTICUT
Milford
Falcon Electronics
203-878-5272

Wallingford
Arrow Electronics
203-265-7741

FLORIDA
Ft. Lauderdale
Arrow Electronics
305-776-7790

Ft. Lauderdale
Pioneer-Standard
305-428-8877

Orlando
Pioneer-Standard
305-834-9090

Palm Bay
Arrow Electronics
305-725-1480

GEORGIA
Norcross
Arrow Electronics
404-449-8252

Norcross
Pioneer-Standard
404-448-1711

IOWA
Cedar Rapids
Arrow Electronics
319-395-7230

Schaumburg
Arrow Electronics
312-397-3440

INDIANA
Indianapolis
Arrow Electronics
317-243-9353

MASSCHUSETTS
Wilmington
Lionex Corp.
617-657-5170

Woburn
Arrow Electronics
617-933-8130

MARYLAND
Columbia
Arrow Electronics
800-842-7769

Columbia
Lionex Corporation
301-964-0040

Gaithersburg
Pioneer-Standard
301-921-0660

MICHIGAN
Ann Arbor
Arrow Electronics
313-971-8220

MINNESOTA
Edina
Arrow Electronics
612-830-1800

Minnetonka
Pioneer-Standard
612-935-5444

MISSOURI
St. Louis
Arrow Electronics
314-567-6888

NORTH CAROLINA
Charlotte
Pioneer-Standard
704-527-8188

Raleigh
Arrow Electronics
919-876-3132

Winston-Salem
Arrow Electronics
919-725-8711

NEW HAMPSHIRE
Manchester
Arrow Electronics
603-668-6968

NEW JERSEY
Fairfield
Arrow Electronics
201-575-5300

Fairfield
Lionex Corp.
201-227-7960

Moorestown
Arrow Electronics
609-596-8000

NEW MEXICO
Albuquerque
Arrow Electronics
505-243-4566

NEW YORK
Hauppauge
Arrow Electronics
516-231-1000

Hauppauge
Lionex Corp.
516-273-1660

Liverpool
Arrow Electronics
315-652-1000

Melville
Arrow Electronics
516-694-6800

Rochester
Arrow Electronics
716-427-0300

OHIO
Centerville
Arrow Electronics
513-435-5563

Solon
Arrow Electronics
216-248-3990

OKLAHOMA
Tulsa
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OREGON
Lake Oswego
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Portland
Arrow Electronics
503-684-1690

Portland
Wyle
503-640-6000

PENNSYLVANIA
Horsham
Lionex Corp.
215-443-5150

Monroeville
Arrow Electronics
412-856-7000

TEXAS
Austin
Arrow Electronics
512-835-4180

Austin
Wyle
512-834-9957

Carrollton (Dallas)
Arrow Electronics
214-380-6464

Houston
Wyle
713-879-9953

Richardson (Dallas)
Wyle
214-235-9953

Stafford (Houston)
Arrow Electronics
713-530-4700

UTAH
Salt Lake City
Anthem Electronics
801-973-8555

Salt Lake City
Arrow Electronics
801-539-1135

Salt Lake City
Wyle
801-974-9953

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Bellevue
Arrow Electronics
206-643-4800

Redmond (Seattle)
Anthem Electronics
206-881-0850

Seattle
Wyle
206-453-8300

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Oak Creek
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414-764-6600

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Future Electronics
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Calgary, Alberta
Future Electronics
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Downsview, Ontario
Future Electronics
416-638-4771

Pointe Claire (Montreal), Quebec
Future Electronics
514-694-7710

Vancouver, B.C.
Future Electronics
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Diode
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Tel: 1-534-7535

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Ireland, Dublin
Micro Marketing Ltd.
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Israel, Tel Aviv
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Tel: 03-3483211-9

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Celdis Italiana SpA
02-6120041

Netherlands, Haaften
Techmation Electronics BV
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Norway, Oslo
Ola Tandberg Elektro A/S
Tel: 02-269955

Portugal, Lisbon
Teleprinta
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Tel: 08-541080

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Datacomp AG
Tel: 01-7302165

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Rapid Recall Ltd.
Tel: 0494-26271

United Kingdom, London
Sunbury on Thames, Middlesex
Hawke Electronics
Tel: 01-1979-7799

United Kingdom
Workingham, Berks
Kudos Electronics Ltd.
Tel: 0734-794515

United States, New York
Arrow Electronics, Export Div.
Tel: 516-293-6363

West Germany, Munich
E2000 A.G.
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