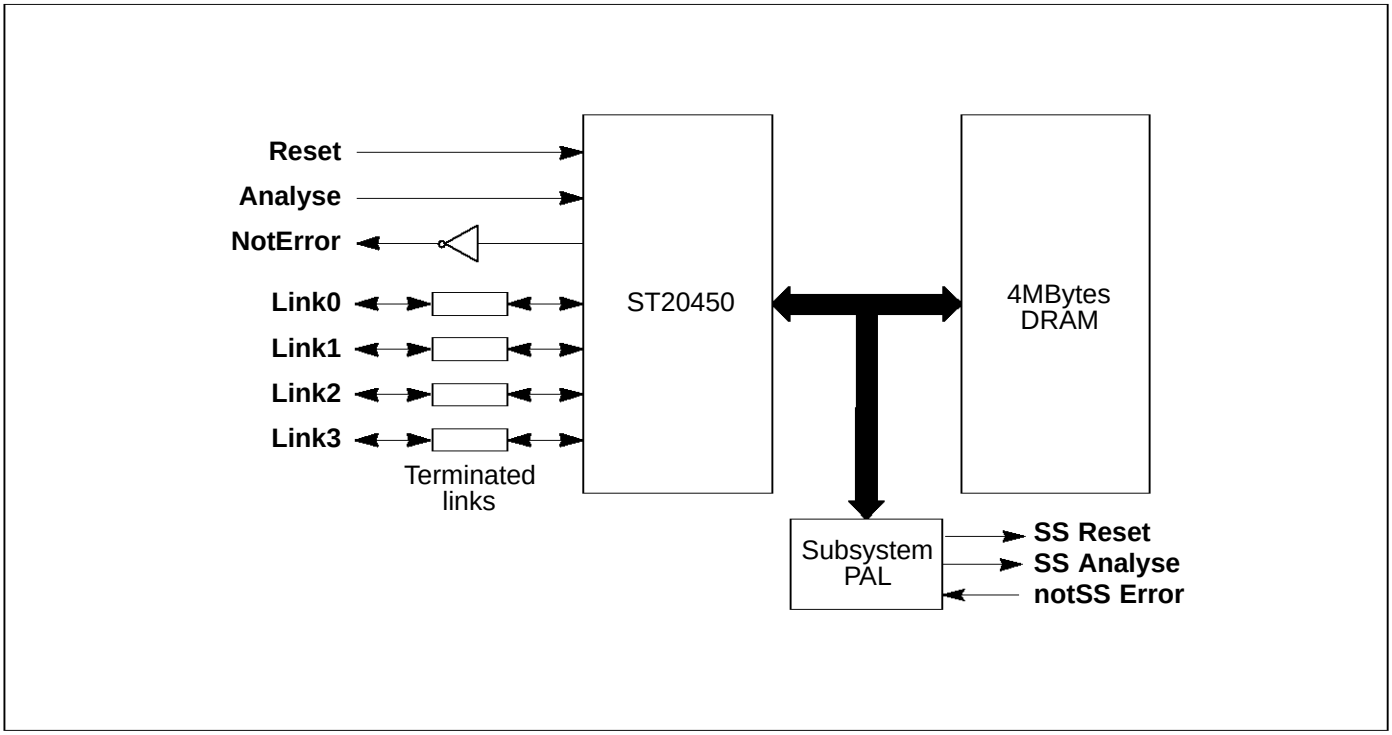
SGS-THOMSON MICROELECTRONICS

IMS B452

4MByte SIZE 2 TRAM

ENGINEERING DATA



FEATURES

- 40MHz ST20450 Transputer
- 4 Mbyte of zero wait-state DRAM (100ns memory cycle time)
- Size 2 TRAM
- Communicates via 4 hardware serial links
- Package has only 16 active pins
- Subsystem control circuitry
- Designed to a published specification (*Technical Note 29*).

DESCRIPTION

The IMS B452 is a compact size 2 TRAM offering 4Mbytes of 4-cycle DRAM and subsystem controller circuitry.

With its 4MBytes of external memory, the B452 is able to run all of the SGS-THOMSON Microelectronics Limited development tools. It is ideally suited for applications using large amounts of memory, allowing progams such as simulation and evaluation to run quickly and efficiently.

1.1 Description

The IMS B452 is an SGS-THOMSON Microelectronics Limited TRAnsputer Module (TRAM) incorporating an ST20450 processor, 4 Mbytes of dynamic RAM and subsystem control circuitry.

TRAMs are board level processors with a simple, standardised interface. They integrate processor, memory and peripheral functions allowing powerful, flexible, processor based systems to be produced with the minimum of design effort. TRAMs may be plugged into motherboards, which provide the necessary electrical signals, mechanical support and usually, an interface to a host machine. A variety of motherboards are available from SGS-THOMSON Microelectronics and from third-party vendors for most of the common computing platforms.

Further details of the TRAM/motherboard philosophy and the full electrical and mechanical specification of TRAMs can be found in [1] and [2].

If a custom motherboard design is intended, then reference to [3] will also be required.

1.2 Pin descriptions

Pin	In/Out	Function	Pin No.
System Services			
VCC, **GND**		Power supply and return	3,14
ClockIn	in	5MHz clock signal	8
Reset	in	Processor reset	10
Analyse	in	Processor error analysis	9
notError	out	Processor error indicator (inverted)	11
Hardware Serial Links			
LinkIn0-3	in	Serial link inputs to processor	13,5,2,16
LinkOut0-3	out	Serial link outputs from processor	12,4,1,15
LinkspeedA,B	in	Link speed selection	6,7
Subsystem services			
Subsystem reset	out	Subsystem reset	1b
Subsystem analyse	out	Subsystem error analysis	1c
Subsystem error	in	Subsystem error indicator	1a

Table 1.1 IMS B452 Pin designations

Notes:

1 Signal names are prefixed by **not** if they are active low; otherwise they are active high.

2 Details of the physical pin locations can be found in Figure 1.3.

1.3 Standard TRAM signals

A TRAM can be regarded as a processor with extra RAM attached but with only 16 signals brought out to the TRAM pins. The majority of the TRAM pins function in exactly

the same way as the corresponding processor signals, which are detailed in [3]. However, a few of these signals are slightly different from the specification as follows:

1.3.1 notError (pin 11)

This is an open collector signal. It is driven low when there is an error; otherwise it is pulled high by a resistor on the motherboard. This enables the **notError** outputs on several TRAMs to be wire-ORed together. (The TRAM specification recommends that no more than 10 **notError** outputs are connected together).

1.3.2 LinkSpeedA and LinkSpeedB (pins 6 and 7)

LinkspeedA and **LinkspeedB** set the speed of processor link 0 and links 1-3 respectively. When the appropriate input is low the link(s) operate at 10 Mbits/s and when high the link(s) operate at 20 Mbits/s.

1.3.3 Hardware serial Link signals

Whilst the hardware serial links obey a protocol identical to that described in [3], there are some differences in the electrical characteristics.

LinkIn0-3

The link inputs have pull-down resistors to ensure that they are disabled when they are not connected.

LinkOut0-3

The link outputs have resistors connected in series for matching to a 100Ω transmission line.

1.3.4 Subsytem signals

The IMS B452 has a subsystem port in addition to the usual TRAM signals. This enables the TRAM to reset or analyse a subsystem of other TRAMs and/or motherboards. The polarity of these signals is the same as that of the **Reset**, **Analyse** and **notError** standard TRAM signals. Therefore, the IMS B452 subsystem can drive other TRAMs on the same motherboard with no intermediate logic. However, **SubSystemReset** and **SubSystemAnalyse** must go through inverting buffers if they are to drive a subsystem off the motherboard.

These subsystem signals are accessed by writing or reading to control registers in the processor memory space.

1.4 Memory configuration

The internal RAM of the IMS ST20450 occupies the first 16Kbytes of address space. The next 4 Mbytes is occupied by the external dynamic RAM present on the TRAM.

Table 1.2 details the start and end addresses of the external memory and Figure 1.1 shows a graphical representation of the memory map (the "#" sign indicating a hexadecimal number).

	Hardware byte address
From:	#80004000
To:	#803FFFFF

Table 1.2 Location of external memory on the IMS B452

Subsystem register locations

The subsystem register addresses start at hardware address #00000000 in all TRAMs that utilize a 32-bit processor, allowing software compatibility between TRAMs. These registers are located as shown in Table 1.3.

Register	Hardware byte address
SubSystemReset (write only)	#00000000
SubSystemAnalyse (write only)	#00000004
notSubSystemError (read only)	#00000000

Table 1.3 Subsystem address locations

Setting bit 0 in either the reset or the analyse registers asserts the corresponding signal. Similarly, clearing bit 0 deasserts the signal. When an error occurs in the subsystem, bit 0 of the error location becomes set.

Byte locations #00000008 and #0000000C are unused. The subsystem registers are repeated at every sixteenth byte location in the positive address space. See Figure 1.1.

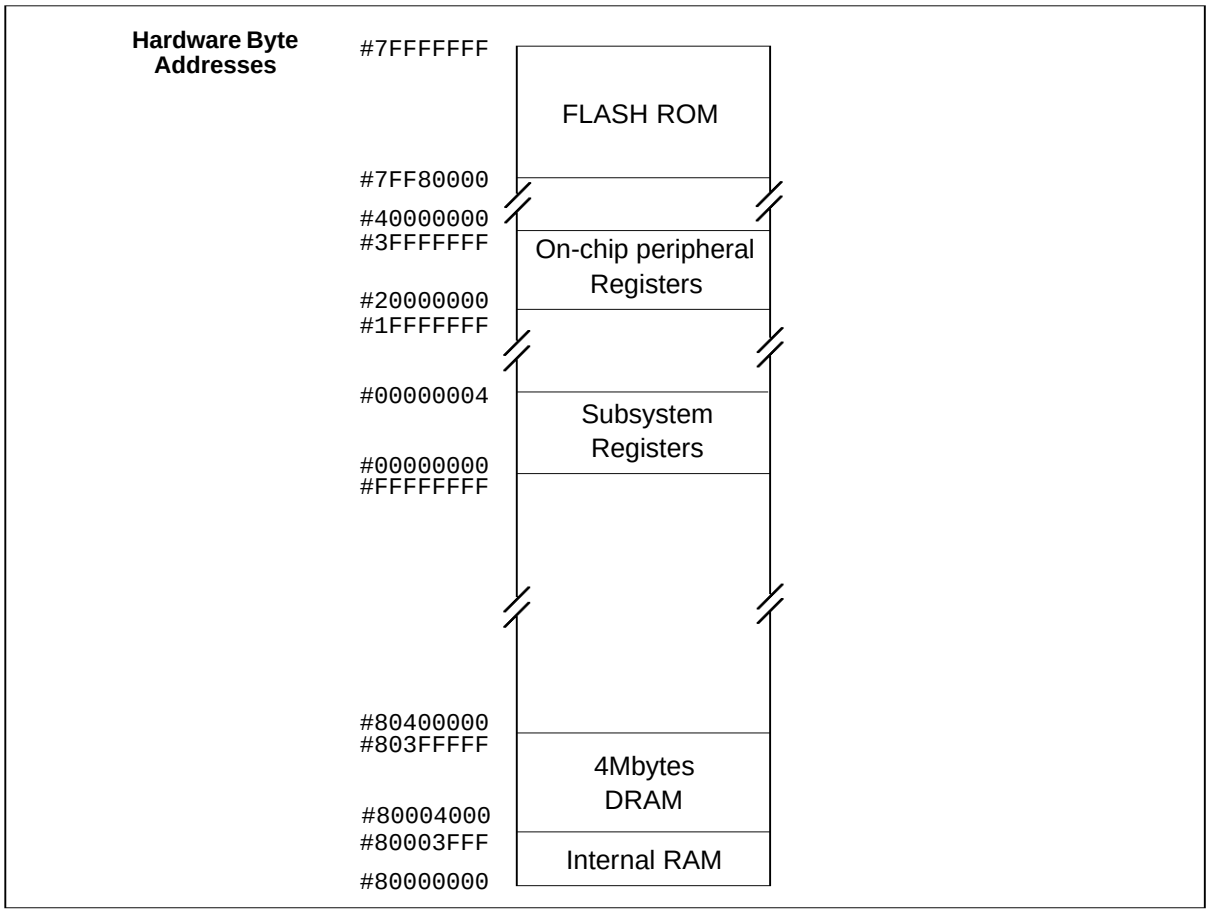


Figure 1.1 Memory map

1.5 Mechanical details

Figure 1.2 indicates the vertical dimensions of a single IMS B452 TRAM and Figure 1.3 shows the outline drawing of the IMS B452.

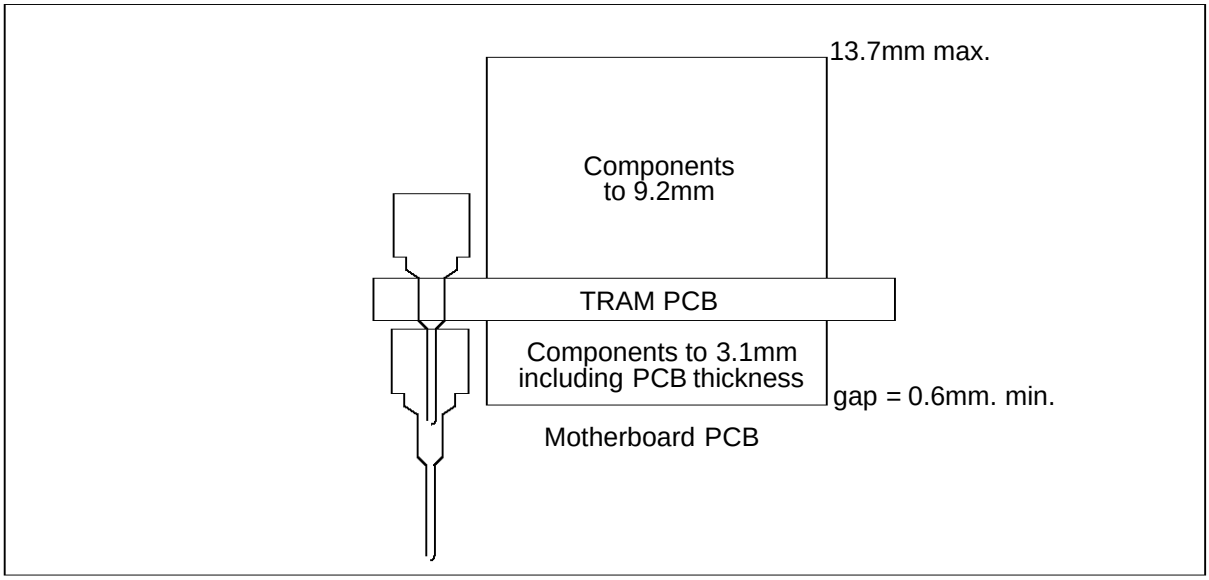


Figure 1.2 IMS B452 height specification

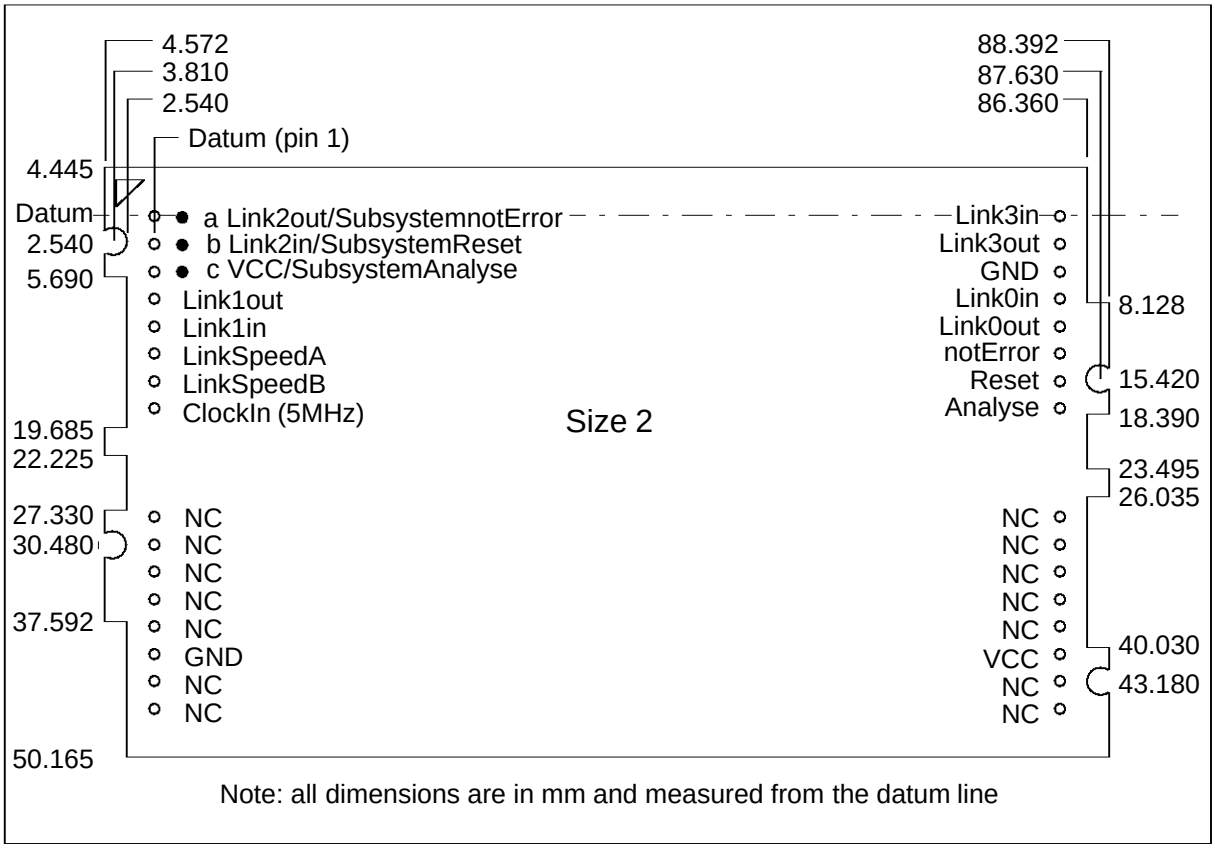


Figure 1.3 PCB profile drawing and pinout

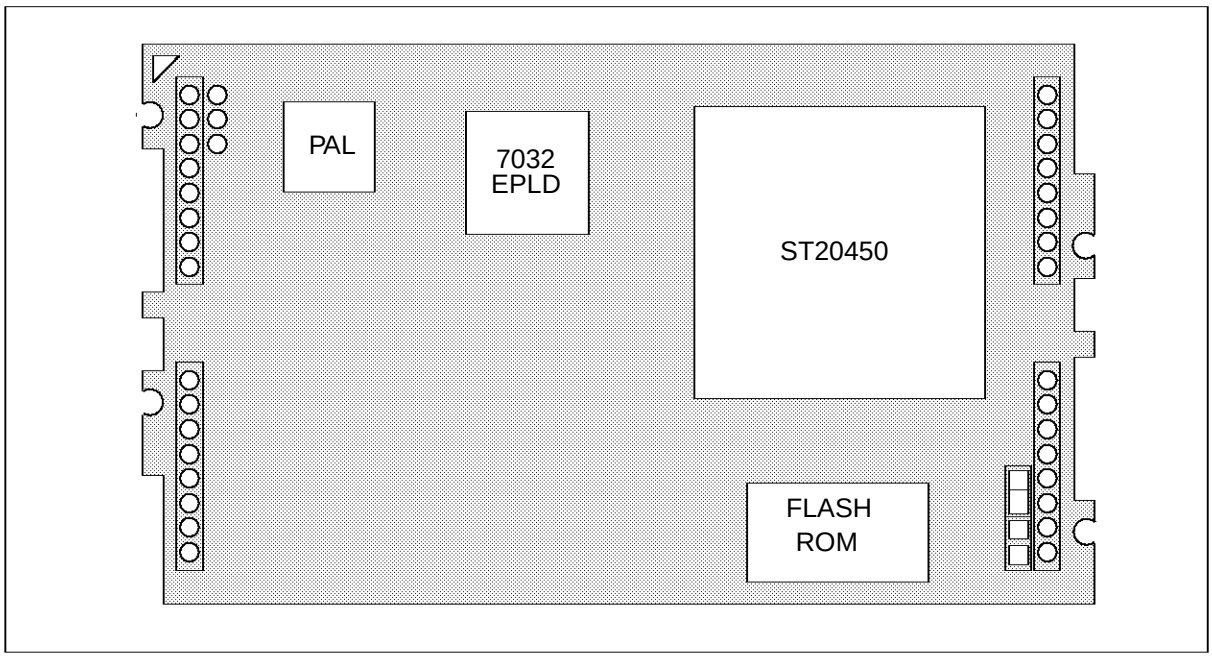


Figure 1.4 TRAM layout

1.6 Installation

Since the IMS B452 contains CMOS components, all normal precautions to prevent static damage should be taken.

The IMS B452 is supplied with spacer pin strips attached to the TRAM pins on the underside of the board. These spacers perform two functions. Firstly, they help to protect the TRAM pins during transit. Secondly, they can be used to space the TRAMs off the motherboard. If there are no components mounted on the motherboard TRAM slot, then the spacer strips should be removed before the TRAM is inserted.

Plug the IMS B452 carefully into the motherboard. Where the IMS B452 is being used with an SGS-THOMSON Microelectronics motherboard, the silk screened triangle marking pin 1 on the IMS B452 (see Figure 1.3) should be aligned with the silk screened triangle that appears in the corner of the appropriate TRAM slot. If it is envisaged that the assembly is likely to be subjected to any vibrations, it is recommended that the TRAM is secured to the motherboard using nylon M3 nuts and bolts. The bolts should be inserted through the fixing holes on the motherboard, and through the castlations on two edges of the TRAM. A number of these nuts and bolts are supplied with each of the SGS-THOMSON Microelectronics motherboards.

Should it be necessary to unplug the IMS B452, it is advised that, having removed any retaining nuts and bolts, it is gently levered out while keeping it as flat as possible. As soon as the IMS B452 is removed, the spacer pin strips should be refitted to the TRAM to protect the pins.

1.7 Specification

TRAM feature	IMS B452	Unit	Notes
Processor type	ST20450		
Number of processors	1		
Number of hardware serial links	4		
Amount of FLASH ROM	256 x 8	Kbyte	
Amount of SRAM	None		
Amount of internal SRAM	16	Kbytes	
SRAM ‘wait -states’	N/A		
Amount of DRAM	4	Mbyte	
DRAM ‘wait -states’	0		
Memory cycle time	100	ns	
Page mode cycle time	50	ns	
Subsystem controller	Yes		
Peripheral circuitry	None		
Parity	No		
Size (TRAM size)	2		
Length	92.96	mm	
Pitch between pins	83.82	mm	
Width	54.61	mm	
Component height above PCB	9.2	mm	
Component height below PCB	3.1	mm	1
Weight	34	g	
Storage temperature	0-70	^{o}C	
Operating temperature	0-50	^{o}C	2
Power supply voltage (VCC)	4.75-5.25	Volt	
Power consumption	3.25	W	3

Table 1.4 IMS B452 specification

Notes

1 This dimension includes the thickness of the PCB which is 1.6mm.

2 The figure quoted refers to the ambient air temperature.

3 Worst case power consumption value obtained when tested at a supply voltage (VCC) of 5.25 V.

1.8 Ordering Information

Description	Order Number
IMS B452 TRAM with ST20450	IMS B452

Table 1.5 Ordering information

1.9 References

1 *Module Motherboard Architecture,* INMOS Technical Note 29.

2 *Dual-In-Line Transputer Modules (TRAMs),* INMOS Technical Note 49.

3 *ST20450 datasheet,* SGS-THOMSON Microelectronics Limited 1995, reference 42 1626 04.