AP-373

APPLICATION NOTE

Replacing the DEC 21140 with the Intel 82557 Controller for LAN Designs

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Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call 1-800-879-4683

CG-041493

1.0. INTRODUCTION

This application note provides information on the differences between the DEC 21140 and the Intel 82557 LAN Controller. This allows Ethernet designers to transition from an existing DEC 21140 design to an Intel 82557 based LAN solution with minimal difficulty. Start Body Text Here--Delete This Line.

NOTE

This document is meant to be used as an overview document only. For detailed information on the DEC 21140, contact Digital. For additional information on the Intel 82557 PCI LAN Controller, contact your local Intel Sales Representative.

2.0. 82557 OVERVIEW

The 82557 is Intel's first highly integrated 32-bit PCI LAN controller for 10 or 100 Mbps Fast Ethernet networks. The 82557 offers a high performance LAN solution while maintaining low-cost through its high-integration. It contains high-performance 32-bit PCI Bus Master interface to fully utilize the high bandwidth available (up to 132 Mbytes per second) to masters on the PCI bus. The 82557 is optimized to support twisted pair Ethernet, the required wiring media for 100BASE-T.

The 82557 contains a number of high-performance networking features that off-load time-critical tasks from the CPU. Its bus master architecture can eliminate the “intermediate copy” step in Receive (RCV) and Transmit (XMT) frame copies, resulting in faster processing of these frames. It maintains a similar memory structure to the Intel 82596 LAN Coprocessor; however, these memory structures have been streamlined for better Network Operating System (NOS) interaction and improved performance.

The 82557 contains two separate RCV and XMT FIFOs, preventing data overruns or underruns while waiting for access to the PCI bus. The FIFOs also enable back to back frame transmission within the minimum interframe spacing. Full support for up to 1 Mbyte of FLASH provides remote Boot capability (a BIOS extension stored in the FLASH which could allow a node to boot itself off of a network drive). For 100 Mbps applications the 82557 contains an IEEE MII compliant interface to any MII compliant physical interface device which provides a complete LAN solution for 10/100 Mbps networks. For 10 Mbps networks, the 82557 can be interfaced to a standard ENDEC interface (such as the Intel 82503 Serial Interface component), while maintaining software compatibility to 100 Mbps solutions.

The 82557 was designed to implement cost effective, high performance PCI add-in adapters, or it can also be designed directly onto a PC motherboard. Its combination of high integration and low cost make it ideal for either application.

2.1. 82557 Feature Summary

- Glueless 32-bit PCI bus master interface (direct drive of bus) - compatible to PCI Specification Rev 2.1
- Intel 82596-like chained memory structure
- Improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- Built-in FLASH interface with addressing up to 1 MByte
- On-chip receive and transmit FIFOs (3 Kbytes each)
- On-chip counters for network management
- Support for back to back transmit interframe spacing (IFS)
- Built in EEPROM interface
- Support for both 10 Mbps and 100 Mbps networks
- Interface to MII Compliant physical layer components for 10/100 Mbps designs (IEEE 802.3u 100BASE-T compatible)
- Standard seven pin ENDEC interface to serial device such as the Intel 82503 for 10 Mbps designs - IEEE 802.3 10BASE-T compatible
- Autodetect and autoswitching for 10 or 100 Mbps network speeds
- Full duplex capable at 10 and 100 Mbps
- 160 Lead QFP package

3.0. DIFFERENCES BETWEEN THE INTEL 82557 AND THE DEC 21140

The following tables list various features for the Intel 82557 LAN Controller and the DEC 21140 LAN Controller.

General Feature Comparison

Feature	Intel 82557	DEC 21140
Bus Interface	PCI	PCI
PCI Clock Range	16-33 MHz	25-33 MHz
Operating Voltage	5V, ± 5%	3.3V
MII Compliant	Yes	Yes
10/100 Mbps Operation	Yes	Yes
Full Duplex	Yes	Yes
Architecture	Bus Master	Bus Master
Integrated 10BASE-T PHY	No	No
On-chip 100BASE-TX PCS/Scrambler	No	Yes
Transmit and Receive FIFO	6K (3K Tx; 3K Rx)	6K (2K Tx; 4K Rx)
MII Management Functions	Yes	Yes
DMA	4-channel, full scatter gather capability	Limited scatter gather capability
Byte Ordering	Little Endian	Little Endian / Big Endian
Testing Features	Software Self Test Internal / External Loopback Software Dump Command	JTAG with Boundary Scan Internal / External Loopback
EEPROM Interface	Yes	Yes
Flash Interface	Yes	No
MDIO Interface	Yes	Yes
Bursting	256 Dword	256 Dword
Pin Compatible to Each Other	No	No
Packaging	160-Pin QFP	144-pin PQFP

Software Interface Comparisons

Feature	Intel 82557	DEC 21140
Memory Structure	Shared	Shared
Memory Addressing	32-bit Enhanced Linear	Long-Word Aligned
Descriptor Format	Array / Linked List	Ring / Chain
Max. # of buffers pointed to by descriptor	Unlimited	2
Statistical Information	Yes (on-chip counters)	Yes (per transmit/receive descriptor)
General Purpose Timer	No	Yes
Transmit Threshold Support	Yes	Yes
On-chip Jabber	No	Yes

4.0. INTEL 82557 AND DEC 21140 SIGNAL GROUPING DIFFERENCES

4.1. Parallel Interface

The Parallel Interface consists of the PCI Bus interface and the Local Memory Interface.

Signal Grouping	Intel 82557 Signal Name	DEC 21140 Signal Name
PCI Interface		
Address / Data	AD0-31	AD0-31
Bus Command and Byte Enables	CBE#0-3	CBE#0-3
Parity	PAR, SERR#, PERR#	PAR, SERR#, PERR#
Interface Control	FRAME#, IRDY#, TRDY#, STOP#, IDSEL#, DEVSEL#	FRAME#, IRDY#, TRDY#, STOP#, IDSEL#, DEVSEL#
Interrupt	INTA#	INT#
Arbitration	REQ#, GNT#	REQ#, GNT#
System	CLK, RST#	PCICLK, RST#
Local Memory Interface		
	EEPROM (EECS, FLF0EESK, FLD1EEDO, FLD2EEDI)	Serial ROM (SRCK, SRCS, SRDI, SRDO)
	FLASH (FLF0EESK, FLD1EEDO, FLD2EED1, FLD3-7, FLADDR0-11, FLCS#, FLOE#, FLWE#)	N/A

4.2. PCI Interface

The glueless PCI interface connects to the PCI bus and provides control, address, and data information to and from the host. Both the Intel 82557 and DEC 21140 operate as both a master and as a slave on the PCI bus. As masters, the 82557 and 21140 interact with the system memory to access data for transmission, or receive data for reception. As a slave, various control structures are accessed by the host CPU, which reads or

writes to on-chip registers. The CPU provides the 82557 and 21140 with the necessary receive and transmit data. The PCI bus interface also provides the means for configuring PCI parameters in the 82557 and the 21140.

4.3. Local Memory Interface

The Local Memory Interface provides a glueless connection between a particular LAN controller and non-volatile memory.

The 82557 can be connected to an external FLASH and/or EEPROM. The FLASH interface, which could also be used to connect to any standard 8-bit EPROM device, provides up to 1 Mbyte of addressing to the FLASH. It utilizes a multiplexed address scheme that works in conjunction with a LS373 or compatible latch to demultiplex the address. Both Read and Write accesses are supported. The FLASH may be used for remote boot functions and network statistics / diagnostics functions. The FLASH is mapped into host system memory (anywhere within the 32-bit memory space) for software accesses. It is also mapped into an available expansion ROM location during boot time of the system. The EEPROM interface is used to store configuration data for the 82557 (i.e. Node Address, board manufacturing ID, etc.). Both read and write accesses to the EEPROM are supported by the 82557.

The DEC 21140 contains an interface to a MicroWire* Serial EPROM. The EPROM interface is used to store configuration data for the 21140 (i.e. Node Address, board manufacturing ID, etc.). Both read and write accesses to the EEPROM are supported by the 21140.

4.4. Serial Interface

The Serial Interface consists of the MII Interface and the Serial (ENDEC) interface.

Signal Grouping	Intel 82557* Signal Name	DEC 21140** Signal Name
MII Interface		
Input Clocks	RXCLK, TXCLK	RCLK, TCLK
Receive Data	RXD0-3	RXD0-3
Receive Info.	RXDV, RXER	DV, ERR
Transmit Data	TXD0-3	TXD0-3
Transmit Info.	TXEN	TXEN
Link	CRS, COL	CRS, CLSN
Management	MDIO, MDC	MDIO, MDC
Serial (ENDEC) Interface		
Input Clocks	RXCLK, TXCLK	RCLK, TCLK
Receive Data	RXD0	RXD
Transmit Data	TXD0	TXD
Transmit Info.	RTS	TXEN
Link	CRS, COL	CRS, CLSN,
Other		

Signal Grouping	Intel 82557* Signal Name	DEC 21140** Signal Name
Misc. DEC 21140 pins	N/A	RXD4, TXD4, LINK, GEP0-7, SRL, MATCH, SD, TCK, TDI, TDO, TMS, RXEN
Misc. Intel 82557 pins	FDX#, FULHAL, RSTOUT, LPBCK	N/A

NOTES:

* Serial (ENDEC) interface pins are a subset of the MII pins. For example, when the 82557 is programmed in serial mode (i.e., with the 82503), the pins used for serial mode are the same as the MII pins (with the exception of TXD and RXD on the 21140—the 82557 uses TXD0 and RXD0 only for the transmit and receive data pins).

** The DEC 21140 Serial (ENDEC) Interface pins are different than the MII Interface pins, with the exception of CRS.

4.5. MII Interface

The MII Interface for both the DEC 21140 and the Intel 82557 provides the functional interface to any MII compatible PHY. The data path consists of a separate nibble-wide stream for both transmit and receive activities. Data transfers are clocked by the 25 MHz transmit and receive clocks in the 100Mbps operation or by 2.5 MHz clocks in the 10 Mbps operation. These clock inputs are driven by the PHY.

4.6. Serial (ENDEC) Interface

The 82557 Serial Interface for both the DEC 21140 and the Intel 82557 provides the functional interface to any 10Mbps (ENDEC) compatible PHY (such as the Intel 82503). The 10Mbps serial-side interface is bit wide. Transmission is performed on the TXD0 pin and reception on RXD0 for the Intel 82557. For the DEC 21140, separate TXD and RXD pins are used (from the MII interface) to transmit and receive bit wide data. These clocks operate at 10 MHz and are both driven by the PHY.

5.0. ADDITIONAL INFORMATION

For additional literature on the Intel 82557, please contact your local Intel sales office. For additional information on the DEC 21140, please contact Digital.