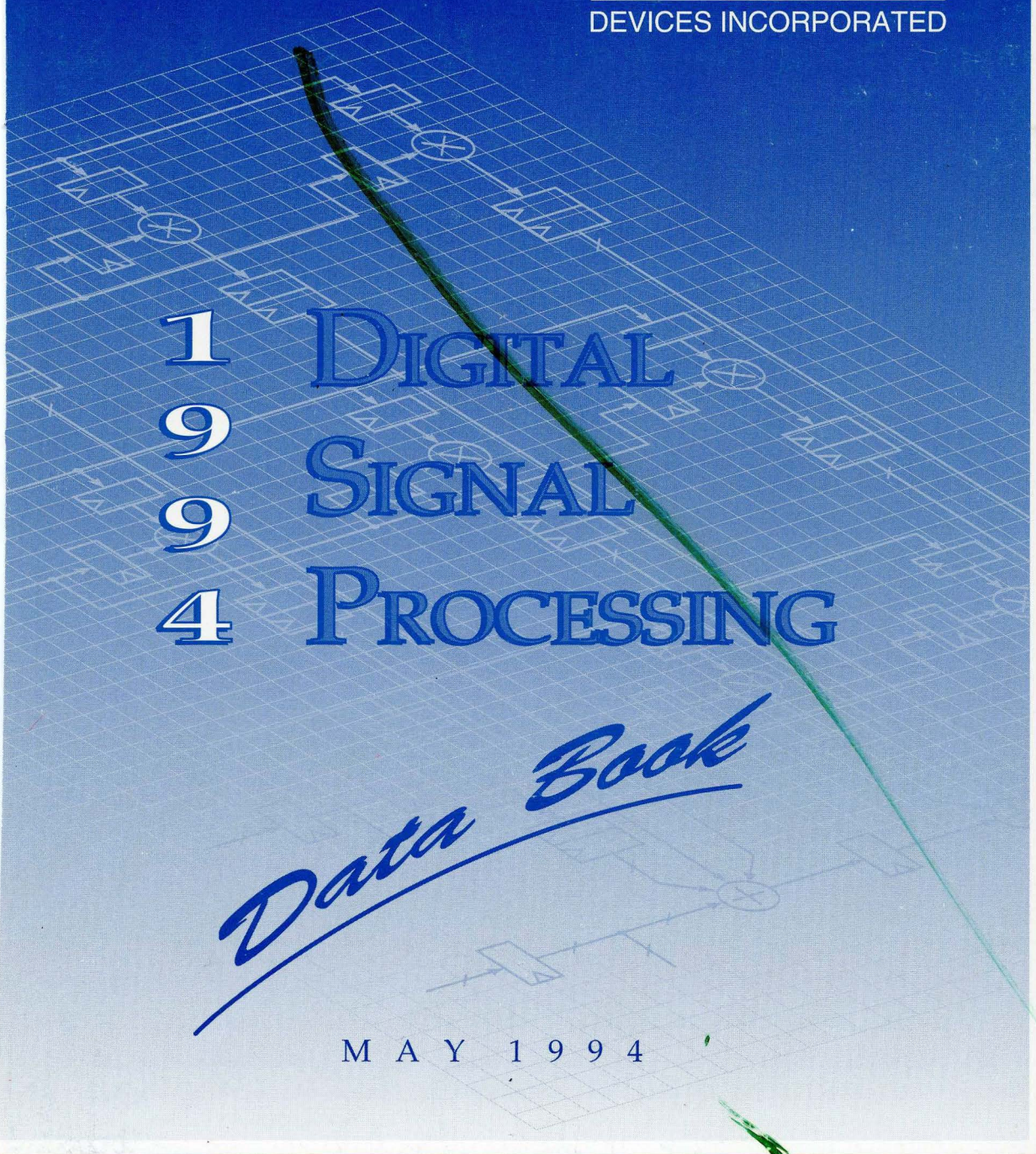
LOGIC

DEVICES INCORPORATED



1994 Digital Signal Processing

Data Book

MAY 1994

LOGIC
DEVICES INCORPORATED

1994 DIGITAL SIGNAL PROCESSING

Data Book

MAY 1994

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Ordering Information 1

Video Imaging Products 2

Arithmetic Logic Units & Special Arithmetic Functions 3

Multipliers & Multiplier-Accumulators 4

Register Products 5

Peripheral Products 6

Quality and Reliability 7

Technology and Design Features 8

Package Information 9

Product Listing 10

Sales Offices 11

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Table of Contents

1. ORDERING INFORMATION 1-1

2. VIDEO IMAGING PRODUCTS 2-1
   - LF2242 12/16-bit Half-Band Digital Filter 2-3
   - LF2246 11 x 10-bit Image Filter 2-11
   - LF2249 12 x 12-bit Digital Mixer 2-19
   - LF2250 12 x 10-bit Matrix Multiplier 2-27
   - LF2272 Colorspace Converter/Corrector (3 x 12-bits) 2-43
   - LF43881 8 x 8-bit Digital Filter 2-51
   - LF43891 9 x 9-bit Digital Filter 2-63

3. ARITHMETIC LOGIC UNITS & SPECIAL ARITHMETIC FUNCTIONS 3-1
   - **Arithmetic Logic Units**
   - L4C381 16-bit Cascadable ALU 3-3
   - L29C101 16-bit ALU Slice (Quad 2901) 3-15
   - **Special Arithmetic Functions**
   - LSH32 32-bit Cascadable Barrel Shifter 3-27
   - LSH33 32-bit Cascadable Barrel Shifter with Registers 3-37
   - L10C23 64 x 1 Digital Correlator 3-45

4. MULTIPLIERS & MULTIPLIER-ACCUMULATORS 4-1
   - **Multipliers**
   - LMU08 8 x 8-bit Parallel Multiplier, Signed 4-3
   - LMU8U 8 x 8-bit Parallel Multiplier, Unsigned 4-3
   - LMU557 8 x 8-bit Parallel Multiplier, Latched Output 4-11
   - LMU558 8 x 8-bit Parallel Multiplier, Unregistered 4-11
   - LMU12 12 x 12-bit Parallel Multiplier 4-19
   - LMU112 12 x 12-bit Parallel Multiplier, Reduced Pinout 4-25
   - LMU16 16 x 16-bit Parallel Multiplier 4-31
   - LMU216 16 x 16-bit Parallel Multiplier, Surface Mount 4-31
   - LMU17 16 x 16-bit Parallel Multiplier, Microprogrammable 4-39
   - LMU217 16 x 16-bit Parallel Multiplier, Microprogrammable, Surface Mount 4-39
   - LMU18 16 x 16-bit Parallel Multiplier, 32 Outputs 4-47
   - **Multiplier-Accumulators**
   - LMA1009 12 x 12-bit Multiplier-Accumulator 4-55
   - LMA2009 12 x 12-bit Multiplier-Accumulator, Surface Mount 4-55
   - LMA1010 16 x 16-bit Multiplier-Accumulator 4-63
   - LMA2010 16 x 16-bit Multiplier-Accumulator, Surface Mount 4-63
   - **Multiplier-Summers**
   - LMS12 12 x 12 + 26-bit Cascadable Multiplier-Summer, FIR 4-71

Table of Contents

5. REGISTER PRODUCTS 5-1

Pipeline Registers

L29C520 4 x 8-bit Multilevel Pipeline Register (1-4 Stages) 5-3
L29C521 4 x 8-bit Multilevel Pipeline Register (1-4 Stages) 5-3
LPR520 4 x 16-bit Multilevel Pipeline Register (1-4 Stages) 5-11
LPR521 4 x 16-bit Multilevel Pipeline Register (1-4 Stages) 5-11
LPR200 8 x 16-bit Multilevel Pipeline Register (1-8 Stages) 5-17
LPR201 7 x 16-bit Multilevel Pipeline Register (1-7 Stages) 5-17
L29C524 14 x 8-bit Dual 7-Deep Pipeline Register (1-14 Stages) 5-27
L29C525 16 x 8-bit Dual 8-Deep Pipeline Register (1-16 Stages) 5-27
L10C11 4/8-bit Variable Length Shift Register (3-18 Stages) 5-37

Register Files

LRF07 8 x 8-bit Register File (3-Port) 5-43

Shadow Registers

L29C818 8-bit Serial Scan Shadow Register 5-49

6. PERIPHERAL PRODUCTS 6-1

L5380 SCSI Bus Controller 6-3
L53C80 SCSI Bus Controller 6-3

7. QUALITY AND RELIABILITY 7-1

8. TECHNOLOGY AND DESIGN FEATURES 8-1

Latchup and ESD Protection 8-3
Power Dissipation in LOGIC Devices Products 8-7

9. PACKAGE INFORMATION 9-1

LOGIC Devices/MIL-STD-1835 Package Code Cross-Reference 9-3
Thermal Considerations 9-5
Package Marking Guide 9-7
Mechanical Drawings 9-9

10. PRODUCT LISTING 10-1

11. SALES OFFICES 11-1

Numeric Table of Contents

L10C11	18 x 8-bit Variable Length Shift Register	5-37
L10C23	64 x 1 Digital Correlator	3-45
L29C101	16-bit ALU Slice (Quad 2901)	3-15
L29C520	4 x 8-bit Multilevel Pipeline Register (1-4 Stages)	5-3
L29C521	4 x 8-bit Multilevel Pipeline Register (1-4 Stages)	5-3
L29C524	14 x 8-bit Dual 7-Deep Pipeline Register (1-14 Stages)	5-27
L29C525	16 x 8-bit Dual 8-Deep Pipeline Register (1-16 Stages)	5-27
L29C818	8-bit Serial Scan Shadow Register	5-49
L4C381	16-bit Cascadable ALU	3-3
L5380	SCSI Bus Controller	6-3
L53C80	SCSI Bus Controller	6-3
LF2242	12/16-bit Half-Band Digital Filter	2-3
LF2246	11 x 10-bit Image Filter	2-11
LF2249	12 x 12-bit Digital Mixer	2-19
LF2250	12 x 10-bit Matrix Multiplier	2-27
LF2272	Colorspace Converter/Corrector (3 x 12-bits)	2-43
LF43881	8 x 8-bit Digital Filter	2-51
LF43891	9 x 9-bit Digital Filter	2-63
LMA1009	12 x 12-bit Multiplier-Accumulator	4-55
LMA1010	16 x 16-bit Multiplier-Accumulator	4-63
LMA2009	12 x 12-bit Multiplier-Accumulator, Surface Mount	4-55
LMA2010	16 x 16-bit Multiplier-Accumulator, Surface Mount	4-63
LMS12	12 x 12 + 26-bit Cascadable Multiplier-Summer, FIR	4-71
LMU08	8 x 8-bit Parallel Multiplier, Signed	4-3
LMU112	12 x 12-bit Parallel Multiplier, Reduced Pinout	4-25
LMU12	12 x 12-bit Parallel Multiplier	4-19
LMU16	16 x 16-bit Parallel Multiplier	4-31
LMU17	16 x 16-bit Parallel Multiplier, Microprogrammable	4-39
LMU18	16 x 16-bit Parallel Multiplier, 32 Outputs	4-47
LMU216	16 x 16-bit Parallel Multiplier, Surface Mount	4-31
LMU217	16 x 16-bit Parallel Multiplier, Microprogrammable, Surface Mount	4-39
LMU557	8 x 8-bit Parallel Multiplier, Latched Output	4-11
LMU558	8 x 8-bit Parallel Multiplier, Unregistered	4-11
LMU8U	8 x 8-bit Parallel Multiplier, Unsigned	4-3
LPR200	8 x 16-bit Multilevel Pipeline Register (1-8 Stages)	5-17
LPR201	7 x 16-bit Multilevel Pipeline Register (1-7 Stages)	5-17
LPR520	4 x 16-bit Multilevel Pipeline Register (1-4 Stages)	5-11
LPR521	4 x 16-bit Multilevel Pipeline Register (1-4 Stages)	5-11
LRF07	8 x 8-bit Register File (3-Port)	5-43
LSH32	32-bit Cascadable Barrel Shifter	3-27
LSH33	32-bit Cascadable Barrel Shifter with Registers	3-37

Ordering Information 1
Video Imaging Products 2
Arithmetic Logic Units & Special Arithmetic Functions 3
Multipliers & Multiplier-Accumulators 4
Register Products 5
Peripheral Products 6
Quality and Reliability 7
Technology and Design Features 8
Package Information 9
Product Listing 10
Sales Offices 11

Ordering Information

TO CONSTRUCT A VALID PART NUMBER:

In order to construct a valid LOGIC Devices part number, begin with the generic number obtained from the data sheet header. To this number, append two or three characters from the tables below indicating the desired package code, temperature range, and screening. Finally, append one or two digits indicating the performance grade desired. Most devices are offered in several speed grades with the part number suffix indicating a critical path delay in nanoseconds.

FOR MORE INFORMATION ON AVAILABLE PART NUMBERS:

All products are not offered with all combinations of package styles, temperature ranges, and screening. The Ordering Information table on the last page of each data sheet indicates explicitly all valid combinations of package, temperature, screening, and performance codes for a given product.

L	7C108	C	M	B	20	L
(1)	(2)	(3)	(4)	(5)	(6)	(7)

Key:

(1) Prefix, LOGIC Devices Inc.
(2) Device number
(3) Package code
(4) Temperature range
(5) Screening
(6) Performance/speed grade
(7) Low power designation

Package Codes

Suffix	Description
C, I*	CerDIP
D, H*	Sidebraze, Hermetic DIP
E	Commercial Pin Grid Array
G	Ceramic Pin Grid Array
J	Plastic J-Lead Chip Carrier
K, T*	Ceramic Leadless Chip Carrier
M	CerFlat
P, N*	Plastic DIP
Q	Plastic Quad Flatpack
W	Plastic SOJ (J-Lead)

*Some devices are available in packages of two widths. For devices available in a single width, C, D, K, and P are used.

Temperature Range

Suffix	Description
C	Commercial 0°C to +70°C
M	Military –55°C to +125°C

Screening

Suffix	Description
No Designator	Commercial Flow
B	MIL-STD-883 Class B Compliant

Ordering Information 1
Video Imaging Products 2
Arithmetic Logic Units & Special Arithmetic Functions 3
Multipliers & Multiplier-Accumulators 4
Register Products 5
Peripheral Products 6
Quality and Reliability 7
Technology and Design Features 8
Package Information 9
Product Listing 10
Sales Offices 11

Video Imaging Products

VIDEO IMAGING PRODUCTS 2-1

LF2242	12/16-bit Half-Band Digital Filter	2-3
LF2246	11 x 10-bit Image Filter	2-11
LF2249	12 x 12-bit Digital Mixer	2-19
LF2250	12 x 10-bit Matrix Multiplier	2-27
LF2272	Colorspace Converter/Corrector (3 x 12-bits)	2-43
LF43881	8 x 8-bit Digital Filter	2-51
LF43891	9 x 9-bit Digital Filter	2-63

LOGIC DEVICES INCORPORATED

LF2242
12/16-bit Half-Band Interpolating/ Decimating Digital Filter

FEATURES

- 66 MHz Clock Rate
- Passband (0 to $0.22f_S$) Ripple: ±0.02 dB
- Stopband ($0.28f_S$ to $0.5f_S$) Rejection: 59.4 dB
- User-Selectable 2:1 Decimation or 1:2 Interpolation
- 12-bit Two's Complement Input and 16-bit Output with User-Selectable Rounding to 9 through 16 Bits
- User-Selectable Two's Complement or Inverted Offset Binary Output Formats
- Three-State Outputs
- Replaces TRW/Raytheon TMC2242
- Package Styles Available:
  - 44-pin Plastic LCC, J-Lead

DESCRIPTION

The **LF2242** is a linear-phase, half-band (low pass) interpolating/ decimating digital filter that, unlike intricate analog filters, requires no tuning. The LF2242 can also significantly reduce the complexity of traditional analog anti-aliasing pre-filters without compromising the signal bandwidth or attenuation. This can be achieved by using the LF2242 as a decimating post-filter with an A/D converter and by sampling the signal at twice the rate needed. Likewise, by using the LF2242 as an interpolating pre-filter with a D/A converter, the corresponding analog reconstruction post-filter circuitry can be simplified.

The coefficients of the LF2242 are fixed, and the only user programming required is the selection of the mode (interpolate, decimate, or pass-through) and rounding. The asynchronous three-state output enable control simplifies interfacing to a bus.

Data can be input into the LF2242 at a rate of up to 66 million samples per second. Within the 66 MHz I/O limit, the output sample rate can be one-half, equal to, or two times the input sample rate. Once data is clocked in, the 55-value output response begins after 6 clock cycles and ends after 60 clock cycles. The pipeline latency from the input of an impulse response to its corresponding output peak is 33 clock cycles.

The output data may be in either two's complement format or inverted offset binary format. To avoid truncation errors, the output data is always internally rounded before it is latched into the output register. Rounding is user-selectable, and the output data can be rounded from 16 bit values down to 9 bit values.

DC gain of the LF2242 is 1.0015 (0.0126 dB) in pass-through and decimate modes and 0.5007 (–3.004 dB) in interpolate mode. Passband ripple does not exceed ±0.02 dB from 0 to $0.22f_S$ with stopband attenuation greater than 59.4 dB from $0.28f_S$ to $0.5f_S$ (Nyquist frequency). The response of the filter is –6 dB at $0.25f_S$. Full compliance with CCIR Recommendation 601 (–12 dB at $0.25f_S$) can be achieved by cascading two devices serially.

LF2242 BLOCK DIAGRAM

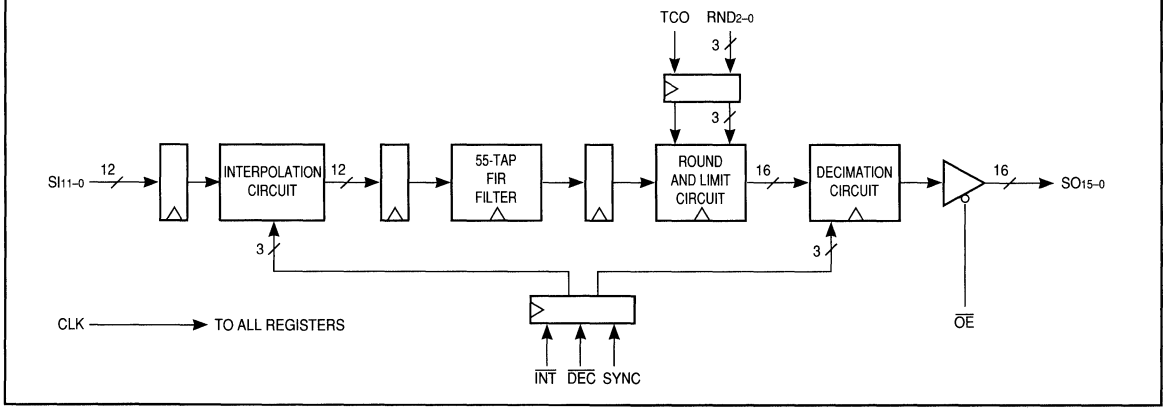
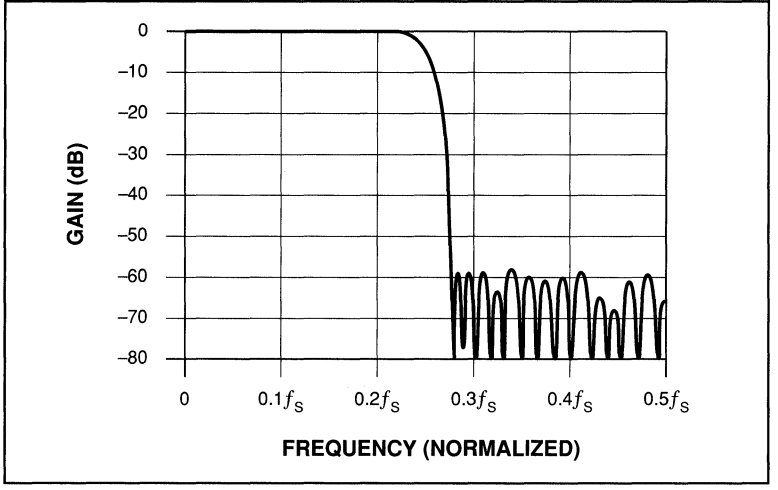


FIGURE 1. FREQUENCY RESPONSE OF FILTER



SIGNAL DEFINITIONS

Power

V_{CC} and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers. All timing specifications are referenced to the rising edge of CLK.

SYNC — Synchronization Control

Incoming data is synchronized by holding SYNC HIGH on CLK_N, and then by bringing SYNC LOW on CLK_{N+1} with the first word of input data. SYNC is held LOW until resynchronization is desired, or it can be toggled at half the clock rate. For interpolation ($\overline{INT}$ = LOW), input data should be presented at the first rising edge of CLK for which SYNC is LOW and then at every alternate rising edge of CLK thereafter. SYNC is inactive if $\overline{DEC}$ and $\overline{INT}$ are equal (pass-through mode).

Inputs

SI_{11-0} — Data Input

12-bit two's complement data input port. Data is latched into the register on the rising edge of CLK. The LSB is SI_0 (Figure 2).

Outputs

SO_{15-0} Data Output

The current 16-bit result is available on the SO_{15-0} outputs. The LF2242's limiter ensures that a valid full-scale (7FFF positive or 8000 negative) output will be generated in the event of an internal overflow. The LSB is SO_0 (Figure 2).

Controls

$\overline{INT}$ — Interpolation Control

When $\overline{INT}$ is LOW and $\overline{DEC}$ is HIGH (Table 1), the device internally forces every other incoming data sample to zero. This effectively halves the input data rate and the output amplitude.

$\overline{DEC}$ — Decimation Control

When $\overline{DEC}$ is LOW and $\overline{INT}$ is HIGH (Table 1), the output register is strobed on every other rising edge of CLK (driven at half the clock rate), decimating the output data stream.

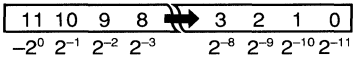
TABLE 1. MODE SELECTION

$\overline{INT}$	$\overline{DEC}$	MODE
0	0	Pass-through*
0	1	Interpolate
1	0	Decimate
1	1	Pass-through*

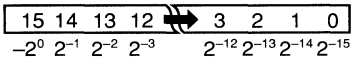
*Input and output registers run at full clock rate

FIGURE 2. INPUT AND OUTPUT FORMATS

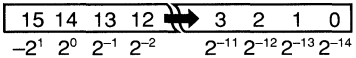
Two's Complement Input Format



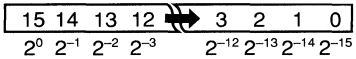
Two's Complement Output Format (TCO = 1, Non-interpolate)



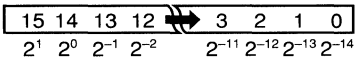
Two's Complement Output Format (TCO = 1, Interpolate)



Inverted Offset Binary Output Format (TCO = 1, Non-interpolate)



Inverted Offset Binary Output Format (TCO = 1, Interpolate)



RND2-0 — Rounding Control

The rounding control inputs set the position of the effective LSB of the output data by adding a rounding bit to the internal bit position that is one below that specified by RND2-0. All bits below the effective LSB position are subsequently zeroed (Table 2).

TCO — Two's Complement Format Control

The TCO input determines the format of the output data. When TCO is HIGH, the output data is presented in two's complement format. When TCO is LOW, the data is in inverted offset binary format (all output bits are inverted except the MSB — the MSB is unchanged).

$\overline{OE}$ — Output Enable

When the $\overline{OE}$ signal is LOW, the current data in the output register is available on the SO15-0 pins. When $\overline{OE}$ is HIGH, the outputs are in a high-impedance state.

TABLE 2. ROUNDING FORMAT

RND2-0	SO15	SO14	SO13	SO12	...	SO8	SO7	SO6	SO5	SO4	SO3	SO2	SO1	SO0
000	X	X	X	X	...	X	X	X	X	X	X	X	X	R
001	X	X	X	X	...	X	X	X	X	X	X	X	R	0
010	X	X	X	X	...	X	X	X	X	X	X	R	0	0
011	X	X	X	X	...	X	X	X	X	X	R	0	0	0
100	X	X	X	X	...	X	X	X	X	R	0	0	0	0
101	X	X	X	X	...	X	X	X	R	0	0	0	0	0
110	X	X	X	X	...	X	X	R	0	0	0	0	0	0
111	X	X	X	X	...	X	R	0	0	0	0	0	0	0

'R' indicates the half-LSB rounded bit (effective LSB position)

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			140	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			10	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

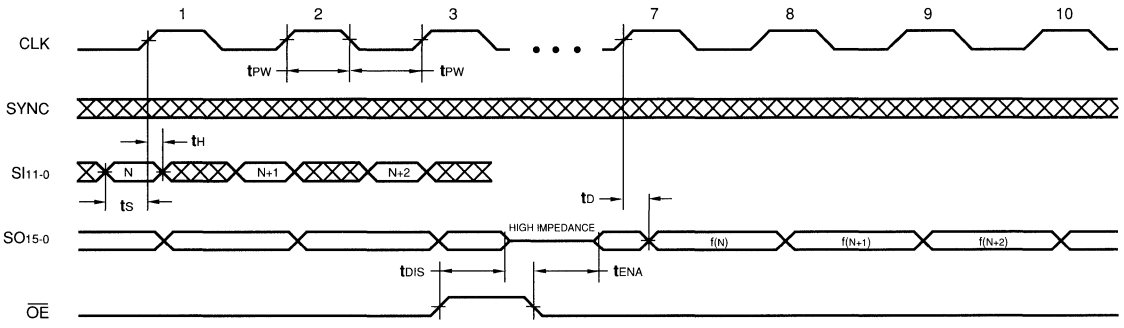
SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

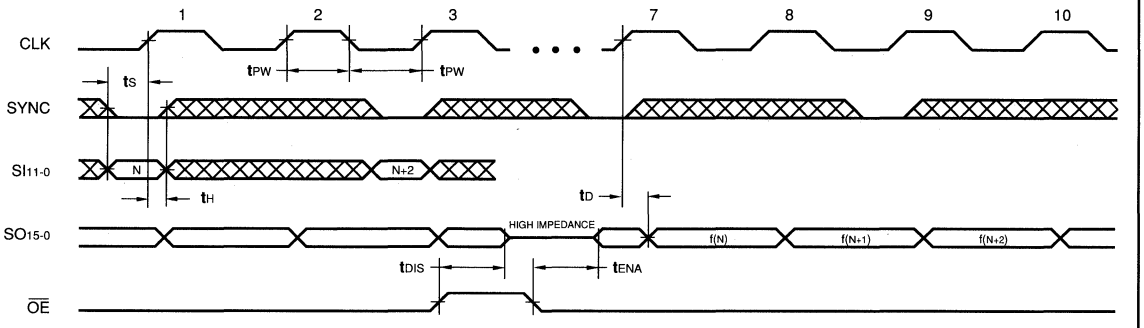
		LF2242–					
		33		25		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25		15	
t_{PW}	Clock Pulse Width	10		10		7	
t_S	Input Setup Time	10		8		6	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		20		16		12
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15		12
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15		12

PRELIMINARY

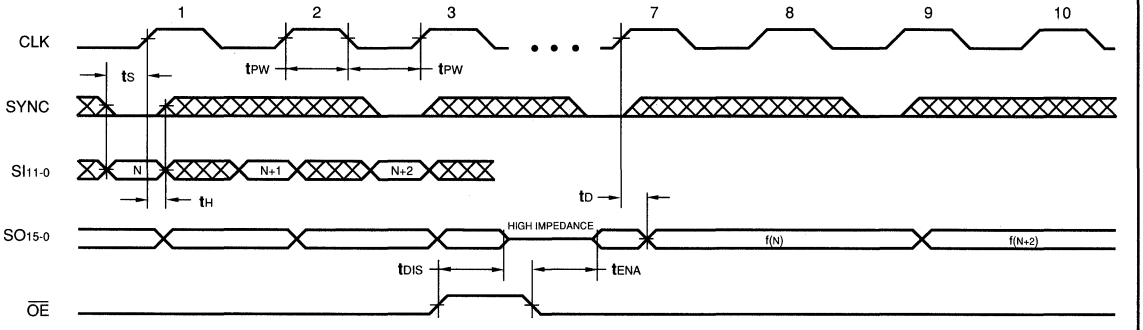
SWITCHING WAVEFORMS: PASS-THROUGH MODE ($\overline{INT}$ = $\overline{DEC}$)



SWITCHING WAVEFORMS: INTERPOLATE MODE ($\overline{INT}$ = 0, $\overline{DEC}$ = 1)



SWITCHING WAVEFORMS: DECIMATE MODE ($\overline{INT}$ = 1, $\overline{DEC}$ = 0)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 3. INPUT CIRCUIT

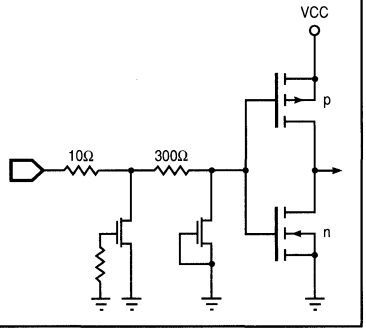


FIGURE 4. OUTPUT CIRCUIT

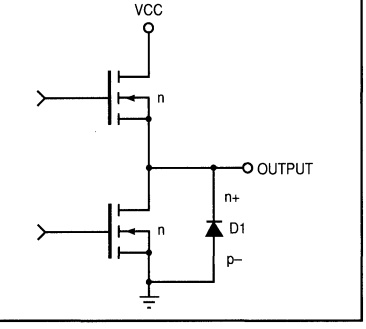
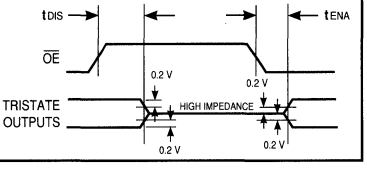
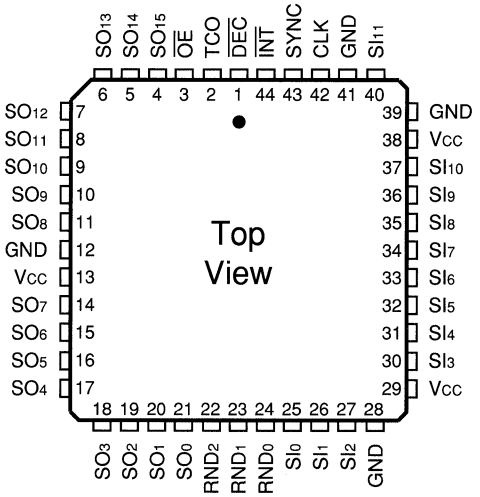


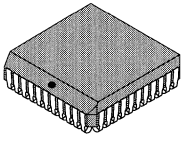
FIGURE 5. THRESHOLD LEVELS



ORDERING INFORMATION

44-pin





Speed	Plastic J-Lead Chip Carrier (J1)	
	0°C to +70°C — COMMERCIAL SCREENING	
33 ns	LF2242JC33	
25 ns	LF2242JC25	
15 ns	LF2242JC15	

LF2246
11 x 10-bit Image Filter

FEATURES

- 40 MHz Data and Coefficient Input and Computation Rate
- Four 11 x 10-bit Multipliers with Individual Data and Coefficient Inputs and a 25-bit Accumulator
- User-Selectable Fractional or Integer Two's Complement Data Formats
- Fully Registered, Pipelined Architecture
- Input and Output Data Registers, with User-Configurable Enables
- Three-State Outputs
- Fully TTL Compatible
- Ideally Suited for Image Processing and Filtering Applications
- Replaces TRW/Raytheon TMC2246
- Package Styles Available:
  - 120-pin Pin Grid Array
  - 120-pin Plastic Quad Flatpack

DESCRIPTION

The **LF2246** consists of an array of four 11 x 10-bit registered multipliers followed by a summer and a 25-bit accumulator. All multiplier inputs are user accessible and can be updated every clock cycle with either fractional or integer two's complement data. The pipelined architecture has fully registered input and output ports and an asynchronous three-state output enable control to simplify the design of complex systems. The pipeline latency for all inputs is five clock cycles.

Storage for mixing and filtering coefficients can be accomplished by holding the data or coefficient inputs over multiple clock cycles. A 25-bit accumulator path allows cumulative word growth which may be internally rounded to 16 bits. Output data is updated every clock cycle and may be held under user control. All inputs, outputs, and controls are registered on the rising edge of clock, except for $\overline{OEN}$. The LF2246 operates at a clock rate of 40 MHz over the full temperature and supply voltage ranges.

The LF2246 is applicable for performing pixel interpolation in image manipulation and filtering applications. The LF2246 can perform a bilinear interpolation of an image (4-pixel kernels) at real-time video rates when used with an image resampling sequencer. Larger kernels or more complex functions can be realized by utilizing multiple devices.

Unrestricted access to all data and coefficient input ports provides the LF2246 with considerable flexibility in applications such as digital filters, adaptive FIR filters, mixers, and other similar systems requiring high-speed processing.

LF2246 Block Diagram

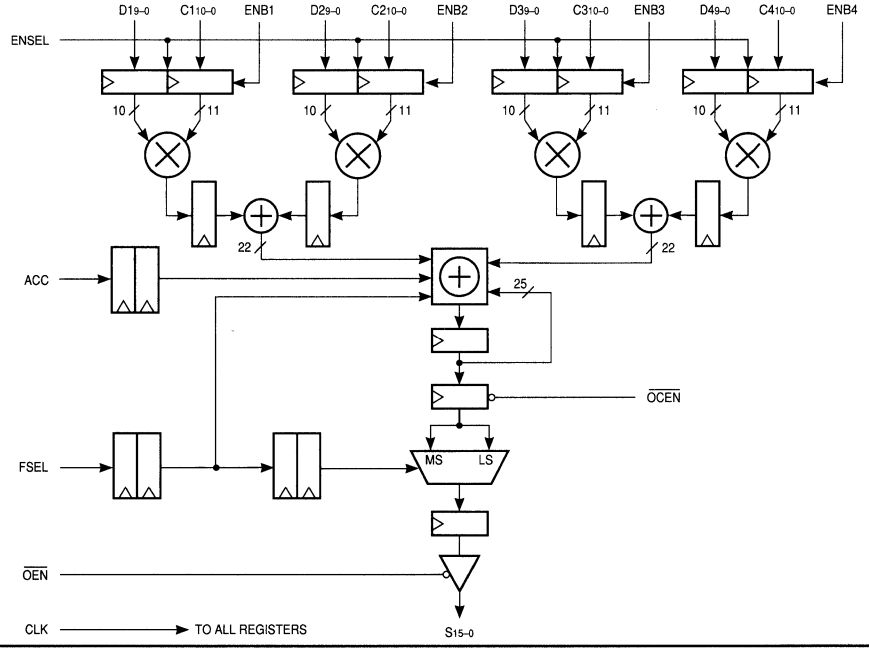


FIGURE 1A. INPUT FORMATS

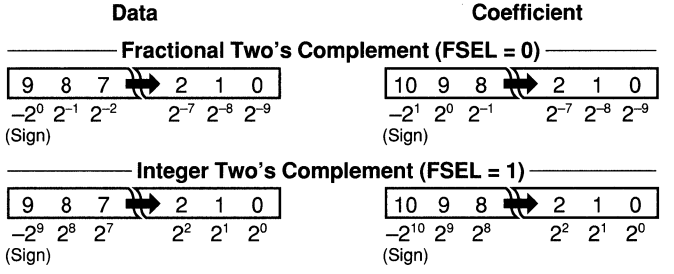


FIGURE 1B. OUTPUT FORMATS

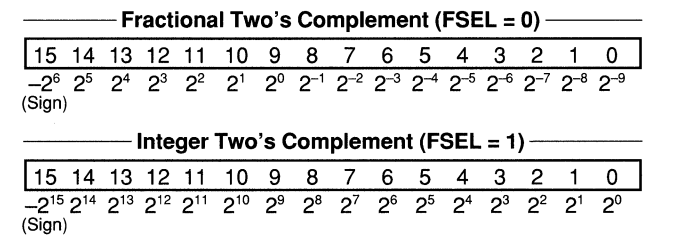


TABLE 1. INPUT REGISTER CONTROL

ENB1-4	ENSEL	INPUT REGISTER HELD
1	1	Data 'N'
1	0	Coefficient 'N'
0	X	None

X = "Don't Care"
'N' = 1, 2, 3, or 4

SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

D19-0–D49-0 — Data Input

D1–D4 are 10-bit data input registers. The LSB is DN0 (Figure 1a).

C110-0–C410-0 — Coefficient Input

C1–C4 are 11-bit coefficient input registers. The LSB is CN0 (Figure 1a).

Outputs

S15-0 — Data Output

The current 16-bit result is available on the S15-0 outputs (Figure 1b).

Controls

ENB1–ENB4 — Input Enable

The ENBN (N = 1, 2, 3, or 4) input allows either or both the DN and CN registers to be updated on each clock cycle. When ENBN is LOW, registers DN and CN are both strobed by the next rising edge of CLK. When ENBN is HIGH and ENSEL is LOW, register DN is strobed while register CN is held. If both ENBN and ENSEL are HIGH, register DN is held, and register CN is strobed (Table 1).

ENSEL — Enable Select

The ENSEL input in conjunction with the individual input enables ENB1–ENB4 determines whether the data or the coefficient input registers will be held on the next rising edge of CLK (Table 1).

$\overline{OEN}$ — Output Enable

When the $\overline{OEN}$ signal is LOW, the current data in the output register is available on the S15-0 pins. When $\overline{OEN}$ is HIGH, the outputs are in a high-impedance state.

$\overline{OCEN}$ — Clock Enable

When the $\overline{OCEN}$ input is LOW, the accumulator output is stored in the output register on the next rising edge of CLK. When $\overline{OCEN}$ is HIGH, the contents of the output register is held. Accumulation continues internally as long as ACC is HIGH, despite the state of $\overline{OCEN}$.

FSEL — Format Select

When the FSEL input is LOW, the data input during the current clock cycle is assumed to be in fractional two's complement format, and the upper 16 bits of the accumulator are presented at the output. Rounding of the accumulator result to 16 bits is performed if the accumulator control input ACC is LOW. When FSEL is HIGH, the data input is assumed to be in integer two's complement format, and the lower 16 bits of the accumulator are presented at the output. No rounding is performed when FSEL is HIGH.

ACC — Accumulator Control

The ACC input determines whether internal accumulation is performed on the data input during the current clock cycle. If ACC is LOW, no accumulation is performed, the prior accumulated sum is cleared, and the current sum of products is output. If FSEL is also LOW, one-half LSB rounding to 16 bits is performed on the result. This allows summations without propagating roundoff errors. When ACC is HIGH, the emerging product is added to the sum of the previous products, without additional rounding.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

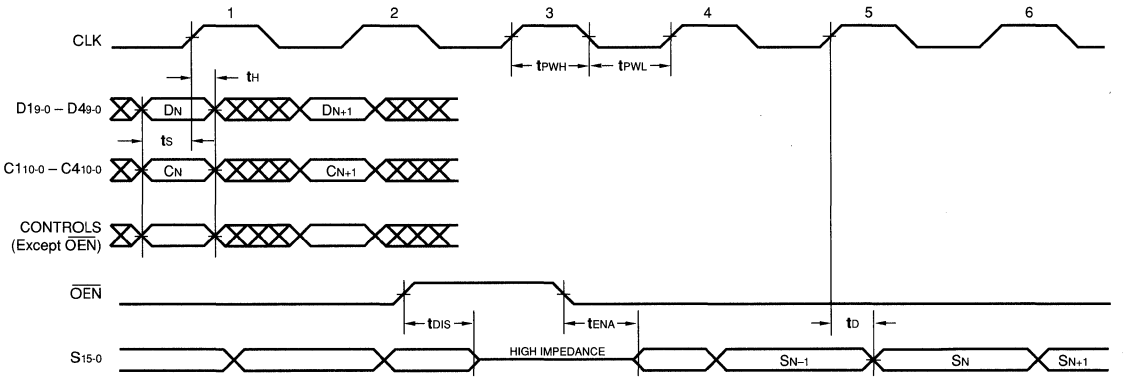
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			6	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2246–			
		33		25	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25	
t_{PWL}	Clock Pulse Width, LOW	15		10	
t_{PWH}	Clock Pulse Width, HIGH	10		10	
t_S	Input Setup Time	10		8	
t_H	Input Hold Time	0		0	
t_D	Output Delay		15		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 30 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 2. INPUT CIRCUIT

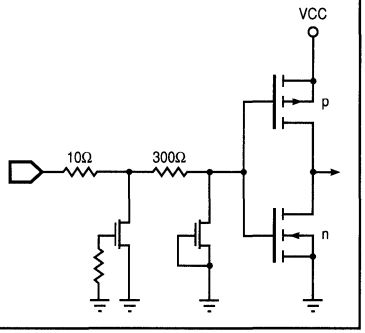


FIGURE 3. OUTPUT CIRCUIT

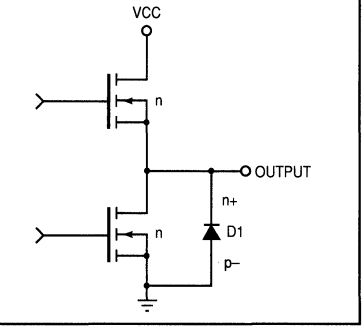
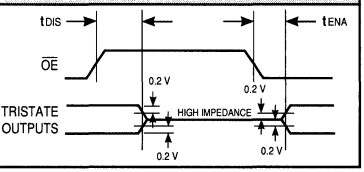
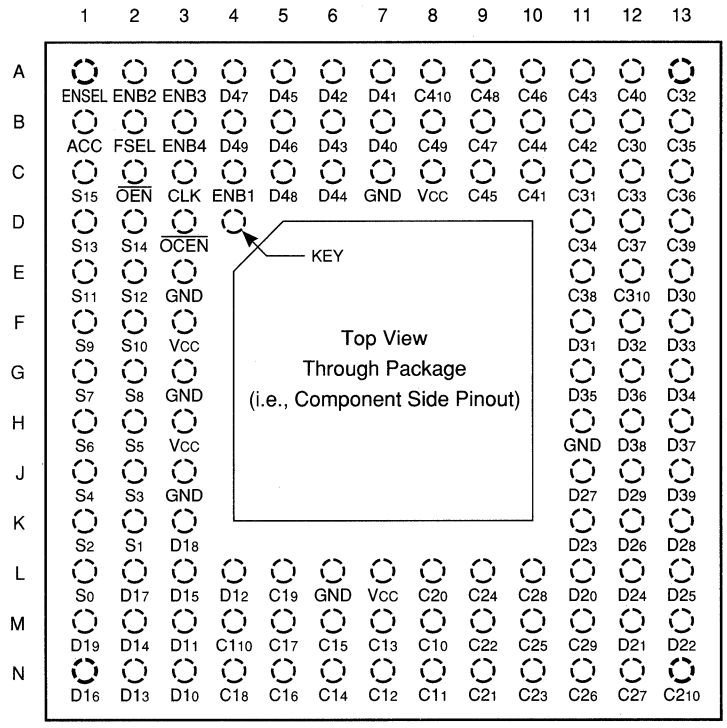


FIGURE 4. THRESHOLD LEVELS



ORDERING INFORMATION

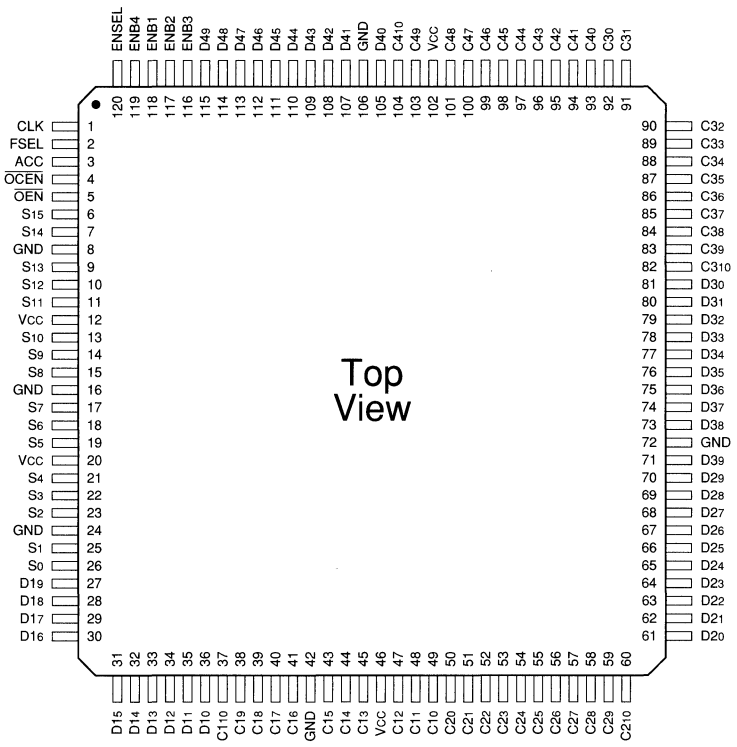
120-pin



Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2246GC33
25 ns	LF2246GC25

ORDERING INFORMATION

120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2246QC33
25 ns	LF2246QC25

FEATURES

- 40 MHz Data and Computation Rate
- Two 12 x 12-bit Multipliers with Individual Data Inputs
- Separate 16-bit Input Port for Cascading Devices
- Independent, User-Selectable 1–16 Clock Pipeline Delay for Each Data Input
- User-Selectable Rounding of Products
- Fully Registered, Pipelined Architecture
- Three-State Outputs
- Fully TTL Compatible
- Replaces TRW/Raytheon TMC2249
- Package Styles Available:
  - 120-pin Pin Grid Array
  - 120-pin Plastic Quad Flatpack

DESCRIPTION

The **LF2249** is a high-speed digital mixer comprised of two 12-bit multipliers and a 24-bit accumulator. All multiplier inputs are user accessible, and each can be updated on every clock cycle. The LF2249 utilizes a pipelined architecture with fully registered inputs and outputs and an asynchronous three-state output enable control for optimum flexibility.

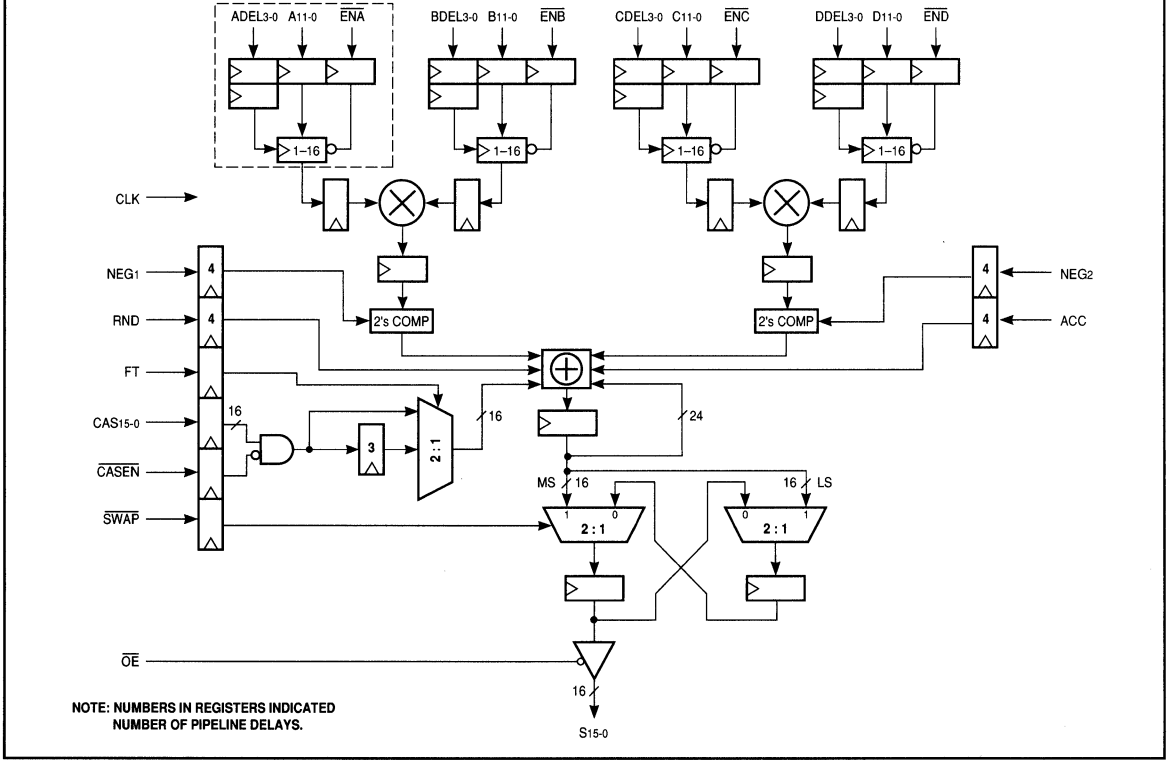
Independent input register clock enables allow the user to hold the data inputs over multiple clock cycles. Each multiplier input also includes a user-selectable 1-16 clock pipeline delay. The output of each multiplier can be independently negated under user control for subtraction of products. The sum of the products can also be internally rounded to 16 bits during the accumulation process.

A separate 16-bit input port connected to the accumulator is included to allow cascading of multiple LF2249s. Access to all 24 bits of the accumulator is gained by switching between upper or lower 16-bit words. The accumulated output data is updated on every clock cycle.

All inputs and outputs of the LF2249 are registered on the rising edge of clock, except for $\overline{OE}$. Internal pipeline registers for all data and control inputs are provided to maintain

2

LF2249 Block Diagram



synchronous operation between the incoming data and all available control functions. The LF2249 operates at a clock rate of 40 MHz over the full commercial temperature and supply voltage ranges.

Because of its flexibility, the LF2249 is ideally suited for applications such as image switching and mixing, digital quadrature mixing and modulating, FIR filtering, and arithmetic function and waveform synthesis.

SIGNAL DEFINITIONS

Power

V_{CC} and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

$A_{11\text{-}0}$–$D_{11\text{-}0}$ — Data Inputs

$A_{11\text{-}0}$–$D_{11\text{-}0}$ are 12-bit data input registers. Data is latched into the input registers on the rising edge of CLK. The contents of the input registers are clocked into the top of the corresponding 16-stage pipeline delay (pushing the contents of the register stack down one register position) on the next clock cycle if the pipeline register stack is enabled. The LSBs are A_0-D_0 (Figure 1a).

$CAS_{15\text{-}0}$ — Cascade Data Input

$CAS_{15\text{-}0}$ is the 16-bit cascade data input port. Data is latched into the register on the rising edge of CLK. The LSB is CAS_0 (Figure 1a).

DETAILED VIEW OF BLOCK DIAGRAM OUTLINED AREA

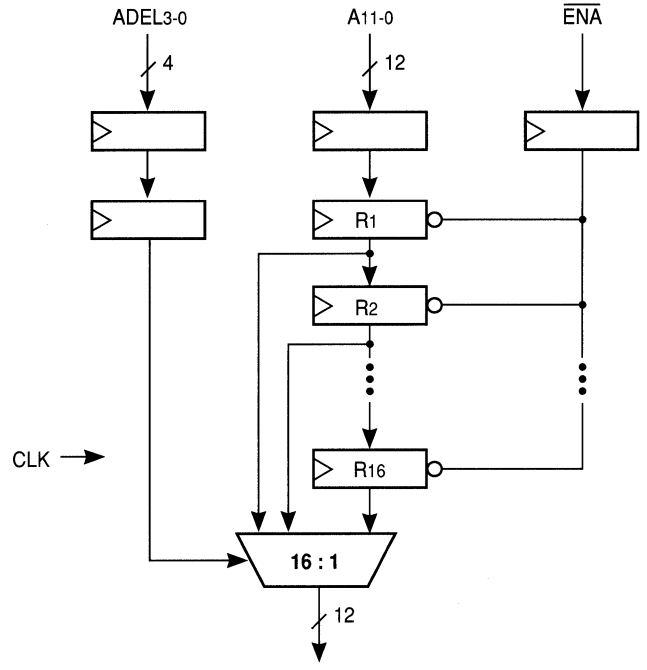


FIGURE 1A. INPUT FORMATS

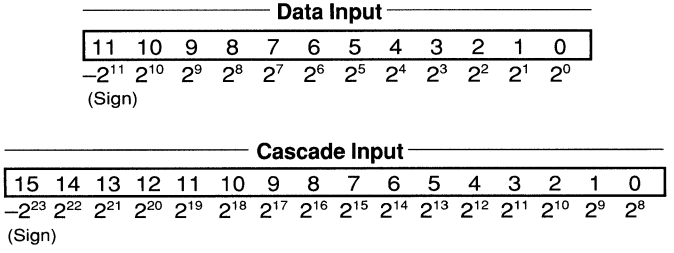
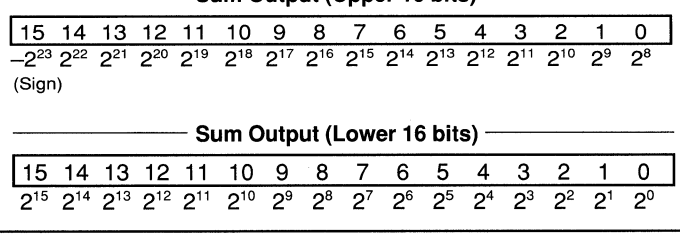


FIGURE 1B. OUTPUT FORMATS



Outputs

S15-0 — Data Output

The current 16-bit result is available on the S15-0 outputs. The output data may be either the upper or lower 16 bits of the accumulator output, depending on the state of $\overline{SWAP}$. The LSB is S0 (Figure 1b).

Controls

$\overline{ENA}$–$\overline{END}$ — Pipeline Register Enable

Input data in the N (N = A, B, C, or D) input register is latched into the corresponding pipeline register stack on each rising edge of CLK for which $\overline{EN}_N$ is LOW. Data already in the N register stack is pushed down one register position. When $\overline{EN}_N$ is HIGH, the data in the N pipeline register stack does not change, and the data in the N input register will not be stored in the register stack.

ADEL3-0–DDEL3-0 — Pipeline Delay Select

NDEL (N = A, B, C, or D) is the 4-bit registered pipeline delay select word. NDEL determines which stage of the N pipeline register stack is routed to the multiplier inputs. The minimum delay is one clock cycle (NDEL = 0000), and the maximum delay is 16 clock cycle (NDEL = 1111). Upon power up, the values of ADEL–DDEL and the contents of the pipeline register stacks are unknown and must be initialized by the user.

NEG1–NEG2 — Negate Control

The NEG1 and NEG2 controls determine whether a subtraction or accumulation of products is performed. When NEG1 is HIGH, the product *A x B* is negated, causing the product to be subtracted from the accumulator contents. Likewise, when NEG2 is HIGH, the product *C x D* is negated, causing the product to be subtracted as well. NEG1 and NEG2 determine the operation to be performed on the data input during the current clock cycle when ADEL–DDEL = 0000.

$\overline{CASEN}$ — Cascade Enable

When $\overline{CASEN}$ is LOW, data being input on the CAS15-0 inputs during that clock cycle will be registered and accumulated internally. When $\overline{CASEN}$ is HIGH, the CAS15-0 inputs are ignored.

FT — Feedthrough Control

When FT is LOW and ADEL–DDEL = 0000, data being input on the CAS15-0 inputs is delayed three clock cycles to align the data with the data being input on the A11-0–D11-0 inputs. When FT is HIGH, the cascade data being input is routed around the three delay registers to simplify the cascading of multiple devices.

ACC — Accumulator Control

The ACC input determines whether internal accumulation is performed on the data input during the current clock cycle. If ACC is LOW, no accumulation is performed, the prior accumulated sum is cleared, and the current sum of products is output. When ACC is HIGH, the emerging products are added to the sum of the previous products.

RND — Rounding Control

When RND is HIGH, the sum of the products of the data being input on the current clock cycle will be rounded to 16 bits. To avoid the accumulation of roundoff errors, rounding is only performed during the first cycle of each accumulation process.

$\overline{SWAP}$ — Output Select

The $\overline{SWAP}$ control allows the user to access all 24 bits of the accumulator output by switching between upper and lower 16-bit words. When $\overline{SWAP}$ is HIGH, the upper 16 bits of the accumulator are always output. When $\overline{SWAP}$ is LOW, the lower 16 bits of the accumulator are output on every other clock cycle. As long as $\overline{SWAP}$ remains LOW, new output data will not be clocked into the output registers.

$\overline{OE}$ — Output Enable

When the $\overline{OE}$ signal is LOW, the current data in the output registers is available on the S15-0 pins. When $\overline{OE}$ is HIGH, the outputs are in a high-impedance state.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
V_{CC} supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output ..... –0.5 V to V_{CC} + 0.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

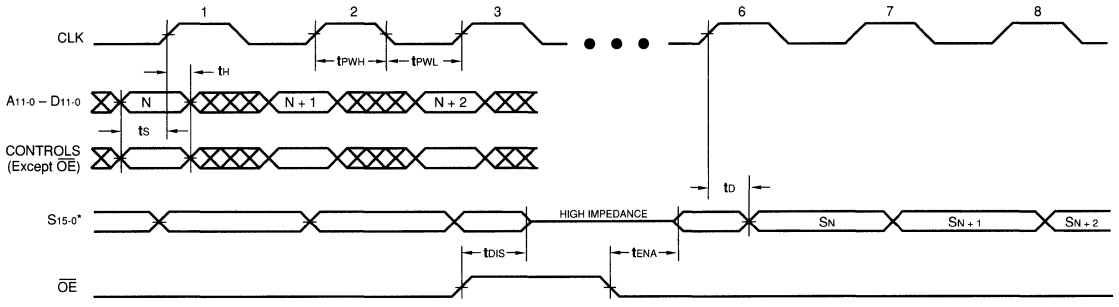
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			6	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2249-					
		40		33		25	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	40		33		25	
t_{PWL}	Clock Pulse Width, LOW	15		15		10	
t_{PWH}	Clock Pulse Width, HIGH	10		10		10	
t_S	Input Setup Time	8		8		7	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		17		15		14
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15		15

SWITCHING WAVEFORMS



*Assumes ADEL–DDEL = 0000

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 25 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 2. INPUT CIRCUIT

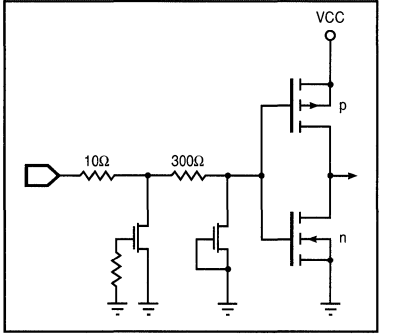


FIGURE 3. OUTPUT CIRCUIT

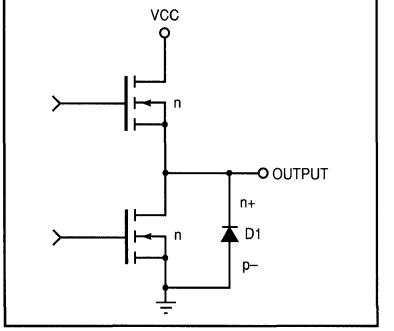
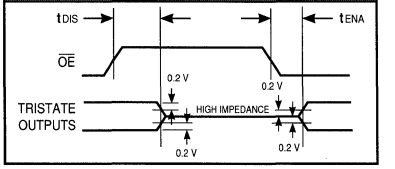
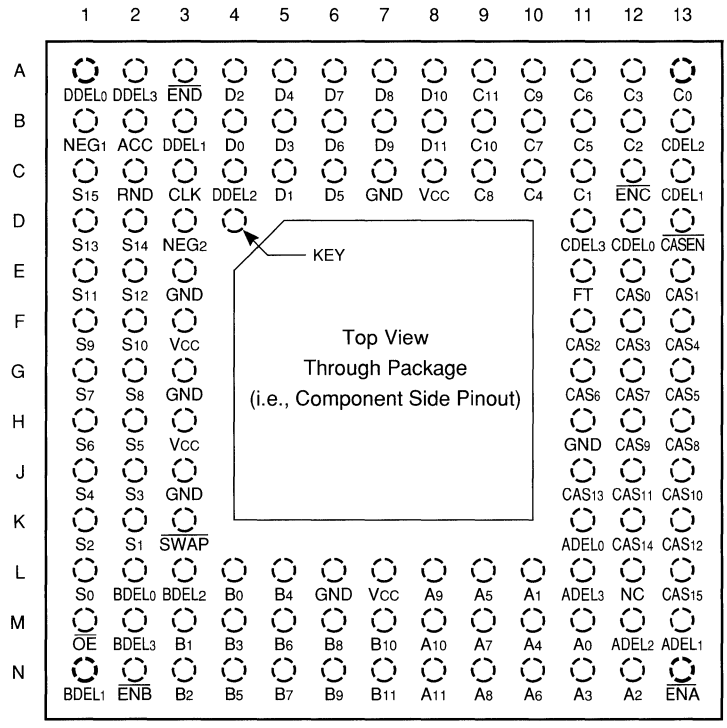


FIGURE 4. THRESHOLD LEVELS



ORDERING INFORMATION

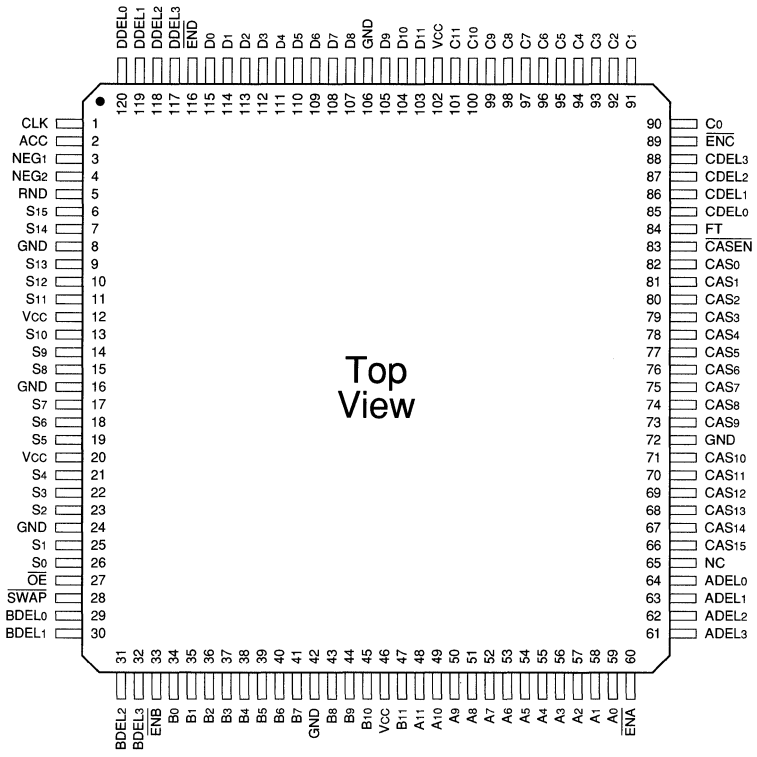
120-pin



Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — COMMERCIAL SCREENING
40 ns	LF2249GC40
33 ns	LF2249GC33
25 ns	LF2249GC25

ORDERING INFORMATION

120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — COMMERCIAL SCREENING
40 ns	LF2249QC40
33 ns	LF2249QC33
25 ns	LF2249QC25

LF2250
12 x 10-bit Matrix Multiplier

FEATURES

- 40 MHz Data and Computation Rate
- Nine Multiplier Array with 12-bit Data and 10-bit Coefficient Inputs
- Separate 16-bit Cascade Input and Output Ports
- On-board Coefficient Storage
- Four User-Selectable Filtering and Transformation Functions:
  - 3 x 3 Matrix Multiplier
  - Cascadable 9-Tap FIR Filter
  - Cascadable 3 x 3 Convolver
  - Cascadable 4 x 2 Convolver
- Replaces TRW/Raytheon TMC2250
- DESC SMD No. 5962-93260
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 120-pin Pin Grid Array
  - 120-pin Plastic Quad Flatpack

DESCRIPTION

The **LF2250** is a high-speed matrix multiplier consisting of an array of nine 12 x 10-bit multipliers. Internal summing adders are also included to provide the configurations needed to implement matrix multiplications, cascadable FIR filters, and pixel convolvers.

The 3 x 3 matrix multiplier (triple dot product) configuration of the LF2250 allows users to easily perform three-dimensional perspective translations or video format conversions at real-time video rates. By using the LF2250 in this configuration, conversions can be made from the RGB (color component) format to the YIQ (quadrature encoded chrominance) or YUV (color difference) formats and vice versa (YIQ or YUV to RGB).

In addition to color space conversions, the LF2250 offers a range of selectable configurations designed for filtering applications. When configured as a 9-tap FIR filter, the LF2250 automatically selects the necessary internal bus structure and inserts the appropriate data path delay elements. In addition, a 16-bit cascade input port allows for the creation of larger filters without a reduction in throughput.

Real-time video image filtering using the convolver modes of the LF2250 can provide edge detection, texture enhancement, and detail smoothing. Both pixel convolver configurations, 3 x 3 and 4 x 2, deliver high-speed data manipulation in a single chip solution. By using the 16-bit cascade input port to cascade two devices, cubic convolutions (4 x 4-pixel) can be easily accommodated with no decrease in throughput rates.

All inputs and outputs, as well as all control lines, are registered on the rising edge of clock. The LF2250 operates at clock rates up to 40 MHz over the full commercial temperature and supply voltage ranges.

LF2250 Block Diagram

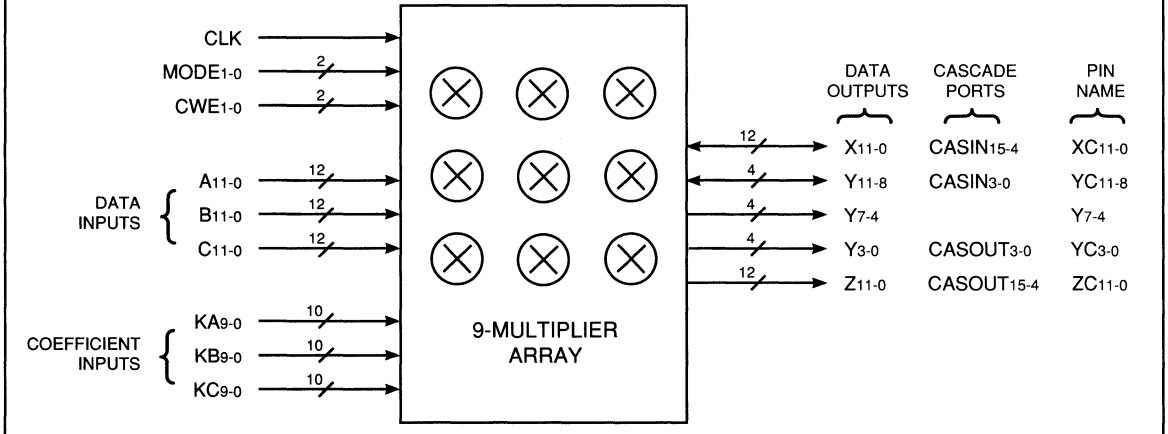


TABLE 1. MODE SELECTION	
MODE1-0	OPERATING MODE
00	3 x 3 Matrix Multiplier
01	9-Tap FIR Filter
10	3 x 3 Convolver
11	4 x 2 Convolver

OPERATING MODES

The LF2250 can realize four different user-selectable digital filtering architectures as determined by the state of the mode (MODE1-0) inputs. Upon selection of the desired function, the LF2250 automatically chooses the appropriate internal data paths and input/output bus structure. Table 1 details the modes of operation.

DATA FORMATTING

The coefficient input ports (KA, KB, KC) are 10-bit fractional two's complement format regardless of the operating mode. The data input ports (A, B, C) are 12-bit integer two's complement format regardless of the operating mode.

In the matrix multiplier mode (Mode 00), the data output ports (X, Y, Z) are 12-bit integer two's complement format. In the FIR filter and convolver modes (Modes 01, 10, 11), the X, Y, and Z ports are configured as the cascade-in (CASIN15-0) and cascade-out (CASOUT15-0) ports. These ports assume 16-bit (12-bit integer, 4-bit fractional) two's complement data on both the inputs and outputs. Table 2 shows the data port formatting for each of the four operating modes.

BIT WEIGHTING

The internal sum of products of the LF2250 can grow to 23 bits. However, in order to keep the output format of the matrix multiply mode (Mode 00) identical to the input format, the X, Y, and Z outputs are truncated to 12-bit integer words. In the filter modes (Modes 01, 10, 11), the cascade output is always half-LSB rounded to 16 bits (12 integer bits and 4 fractional bits). The user may half-LSB round the output to any size less than 16 bits by simply forcing a "1" into the bit position of the cascade input immediately below the desired LSB. For example, if half-LSB rounding to 12 bits is desired, then a "1" must be forced into the CASIN3 bit position (CASOUT4 would then be the LSB).

In all four modes, the user may adjust the bit weighting, by applying an identical scaling correction factor to both the input and output data streams. If the coefficients are re-scaled, then the relative weightings of the cascade-in and cascade-out ports will differ accordingly. Figure 1 illustrates the input and output bit weightings for all four modes.

DATA OVERFLOW

Because the LF2250's matched input and output data formats accommodate unity gain (0 dB), input conditions that could lead to numeric overflow may exist. To ensure that no overflow conditions occur, the user must be aware of the maximum input data and coefficient word sizes allowable for each specific algorithm being performed.

SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

A11-0, B11-0, C11-0 — Data Inputs

A, B, and C are the 12-bit registered data input ports. Data presented to these ports is latched into the multiplier input registers for the current operating mode (Table 1). In the filter modes (Modes 01, 10, 11), the rising edge of CLK internally right-shifts new data to the next filter tap.

KA9-0, KB9-0, KC9-0 — Coefficient Inputs

KA, KB, and KC are the 10-bit registered coefficient input ports. Data presented to these ports is latched into the corresponding internal coefficient register set defined by CWE1-0 (Table 4) on the next rising edge of CLK. Table 3 shows which coefficient registers are available for each coefficient input port.

TABLE 2. DATA PORT FORMATTING											
	PIN NAMES										
MODE1-0	A11-0	B11-0	C11-0	KA9-0	KB9-0	KC9-0	XC11-0	YC11-8	Y7-4	YC3-0	ZC11-0
00	A11-0	B11-0	C11-0	KA9-0	KB9-0	KC9-0	X11-0	Y11-8	Y7-4	Y3-0	Z11-0
01	A11-0	A11-0	NC	KA9-0	KB9-0	KC9-0	CASIN15-4	CASIN3-0	NC	CASOUT3-0	CASOUT15-4
10	A11-0	B11-0	C11-0	KA9-0	KB9-0	KC9-0	CASIN15-4	CASIN3-0	NC	CASOUT3-0	CASOUT15-4
11	A11-0	B11-0	NC	KA9-0	KB9-0	KC9-0	CASIN15-4	CASIN3-0	NC	CASOUT3-0	CASOUT15-4

FIGURE 1A. INPUT FORMATS

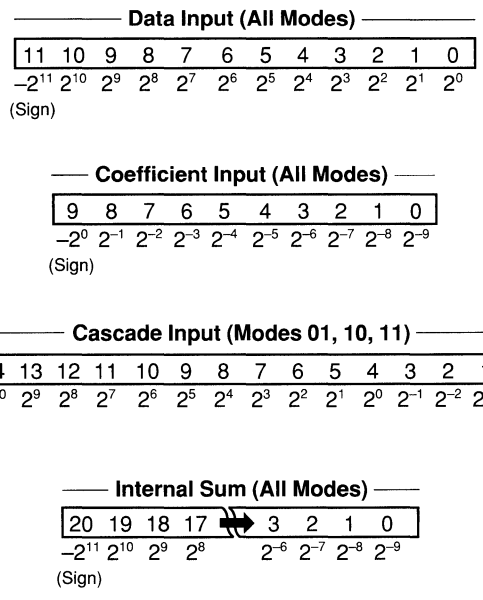
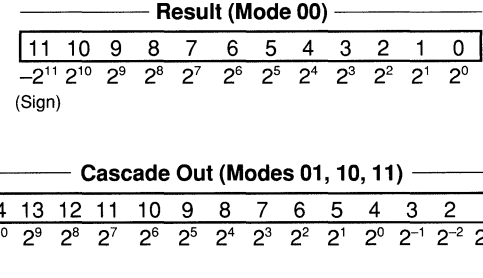


FIGURE 1B. OUTPUT FORMATS



CASIN15-0 — Cascade Input

In the filter modes (Modes 01, 10, 11), the 12-bit X port and four bits of the Y port are internally reconfigured as the 16-bit registered cascade input port. Data presented to this port will be added to the internal sum of products.

Outputs

X11-0, Y11-0, Z11-0 — Data Outputs

X, Y, and Z are the 12-bit registered output ports for the matrix multiply mode (Mode 00). These ports are automatically reconfigured for the filter modes (Modes 01, 10, 11) as the cascade-in and cascade-out ports.

CASOUT15-0 — Cascade Output

In the filter modes (Modes 01, 10, 11), the 12-bit Z port and four bits of the Y port are internally reconfigured as the 16-bit registered cascade output port.

NOTE: *The X, Y, and Z ports are automatically reconfigured by the LF2250 as the cascade-in and cascade-out ports as required for each operating mode. Because both the X and Z ports are used for the cascade ports, all X port pins and all Z port pins are labelled as XC and ZC, respectively. All Y port pins that are used for the cascade ports are labelled as YC. Those Y port pins which are not used for the cascade ports are labelled as Y.*

Controls

MODE1-0 — Mode Select

The registered mode select inputs determine the operating mode of the LF2250 (Table 1) for data being input on the next clock cycle. When switching between modes, the internal pipeline latencies of the device must be observed. After switching operating modes, the user must allow enough clock cycles to pass to flush the internal registers before valid data will appear on the outputs.

CWE1-0 — Coefficient Write Enable

The registered coefficient write enable inputs determine which internal coefficient register set to update (Table 4) on the next clock cycle.

TABLE 3. COEFFICIENT INPUTS

INPUT PORT	REG. AVAILABLE
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

TABLE 4. COEFF. REG. UPDATE	
CWE1-0	COEFFICIENT SET
00	Hold All Registers
01	KA1, KB1, KC1
10	KA2, KB2, KC2
11	KA3, KB3, KC3

DETAILS OF OPERATION

3 x 3 Matrix Multiplier — Mode 00

In this mode, all three input ports (A, B, C) and all three output ports (X, Y, Z) are utilized to implement a 3 x 3 matrix multiplication (triple dot product). Each truncated 12-bit output is the sum of all three input words multiplied by the appropriate coefficients (Table 5). The pipeline latency for this mode is five clock cycles. Therefore, the sum of products will be output five clock cycles after the input data has been latched. New output data is subsequently available every clock cycle thereafter.

9-Tap FIR Filter — Mode 01

This mode utilizes the 12-bit A and B data input ports as well as the 16-bit CASIN port. The input data should be presented to the A and B ports simultaneously. The resulting 9-sample response, which is half-LSB rounded to 16 bits, begins after five clock cycles and ends after 13 clock cycles (Table 5). The pipeline latency from the input of an impulse response to the center of the output response is nine clock cycles. The latency from the CASIN port to the CASOUT port is four clock cycles. New output data is available every clock cycle.

3 x 3-Pixel Convolver — Mode 10

When configured in this mode, line delayed data is loaded through the A, B, and C input ports. During each cycle, a new rounded 16-bit output (comprising of the summation of the multiplications of the last nine data inputs with their related coefficients) becomes available (Table 5). The CASIN term is also added to each new output. The internal bus structure and pipeline delays allow new input data to be added every cycle while maintaining the structure of the filtering operation. This addition of new data every cycle produces the effect of the convolution window moving to the next pixel column.

4 x 2-Pixel Convolver — Mode 11

Using the A and B ports, input data is loaded and multiplied by the on-board coefficients. These products are then summed with the CASIN data and rounded to create the 16-bit output. The cascade ports allow multiple devices to be used together for use with larger kernels. As with Mode 10, each cycle results in a 16-bit output created from the products and summations performed.

TABLE 5. LATENCY EQUATIONS

3 x 3 Matrix Multiplier — Mode 00

$$X(n+4) = A(n)KA1(n) + B(n)KB1(n) + C(n)KC1(n)$$
$$Y(n+4) = A(n)KA2(n) + B(n)KB2(n) + C(n)KC2(n)$$
$$Z(n+4) = A(n)KA3(n) + B(n)KB3(n) + C(n)KC3(n)$$

9-Tap FIR Filter — Mode 01

$$\begin{aligned} CASOUT(n+12) = {} & A(n+8)KA3(n+8) + A(n+7)KA2(n+7) + A(n+6)KA1(n+6) \\ & + B(n+5)KB3(n+8) + B(n+4)KB2(n+7) + B(n+3)KB1(n+6) \\ & + B(n+2)KC3(n+8) + B(n+1)KC2(n+7) + B(n)KC1(n+6) \\ & + CASIN(n+9) \end{aligned}$$

3 x 3-Pixel Convolver — Mode 10

$$\begin{aligned} CASOUT(n+6) = {} & A(n+2)KA3(n+2) + A(n+1)KA2(n+1) + A(n)KA1(n) \\ & + B(n+2)KB3(n+2) + B(n+1)KB2(n+1) + B(n)KB1(n) \\ & + C(n+2)KC3(n+2) + C(n+1)KC2(n+1) + C(n)KC1(n) \\ & + CASIN(n+3) \end{aligned}$$

4 x 2-Pixel Convolver — Mode 11

$$\begin{aligned} CASOUT(n+7) = {} & A(n+3)KA3(n+3) + A(n+2)KA2(n+2) + A(n+1)KA1(n+1) \\ & + A(n)KC3(n+3) + B(n+3)KB3(n+3) + B(n+2)KB2(n+2) \\ & + B(n+1)KB1(n+1) + B(n)KC1(n+1) \\ & + CASIN(n+4) \end{aligned}$$

FIGURE 2. 3 x 3 MATRIX MULTIPLIER — MODE 00

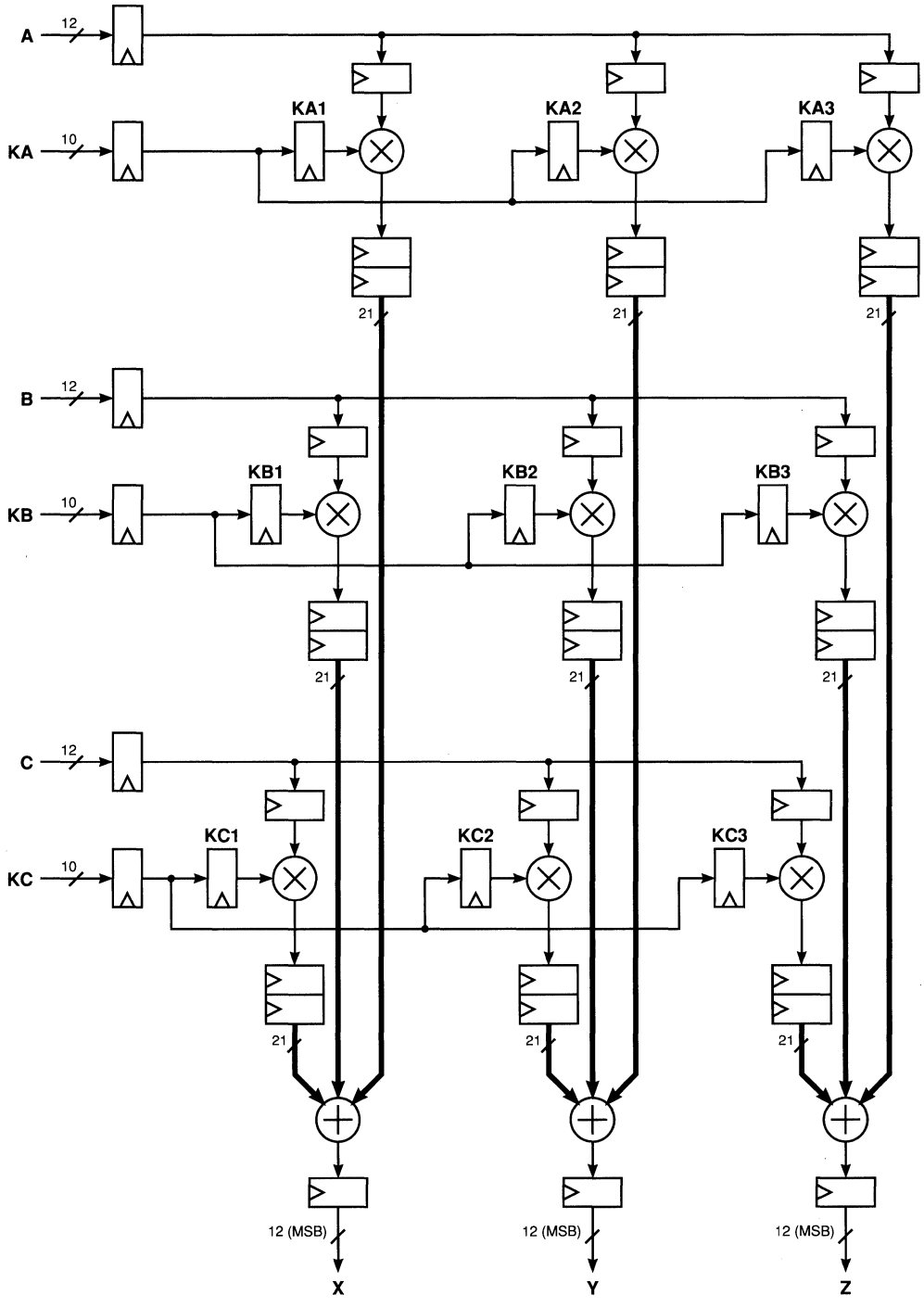


FIGURE 3. 9-TAP FIR FILTER — MODE 01

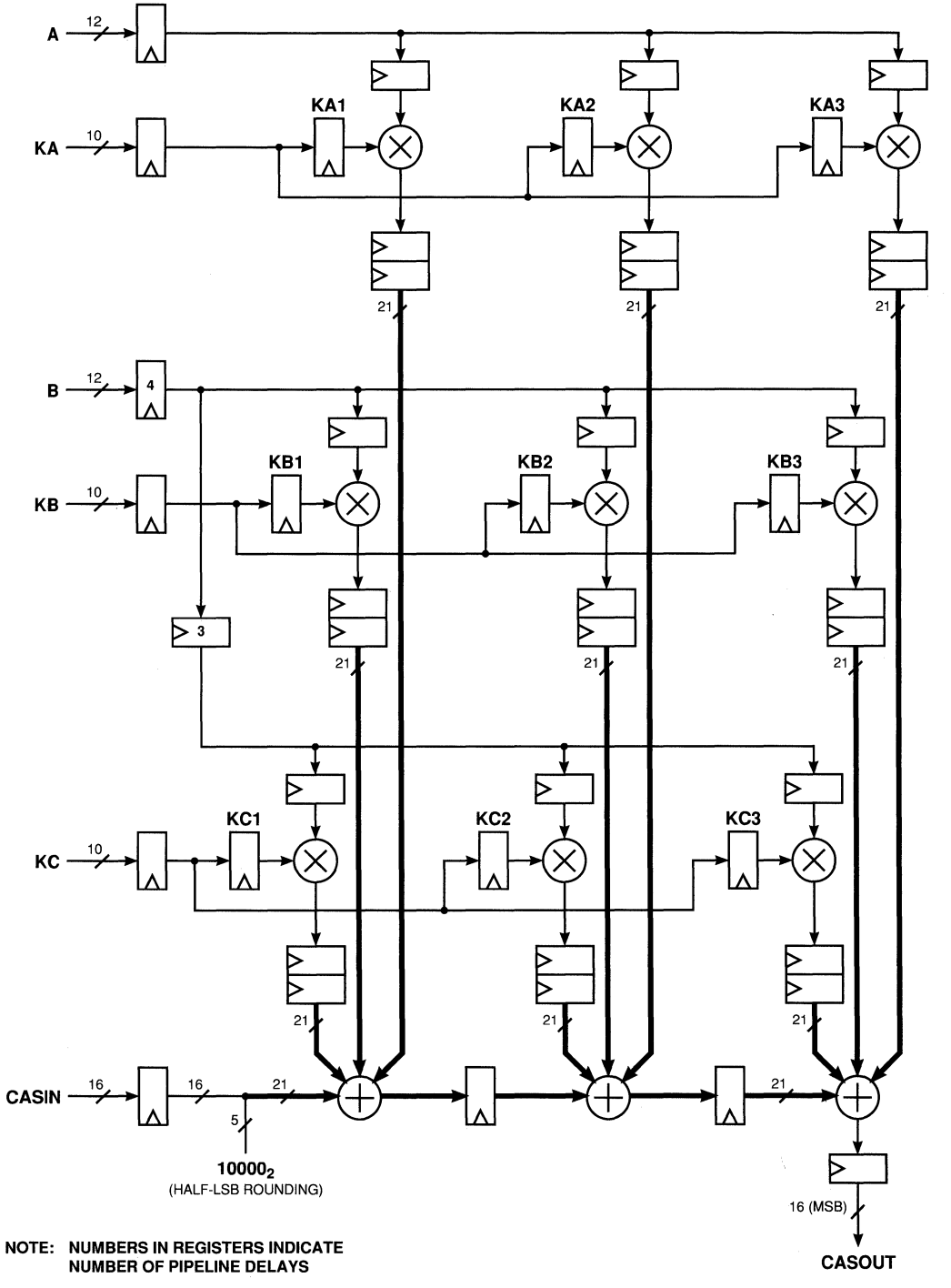


FIGURE 4. 3 x 3-PIXEL CONVOLVER — MODE 10

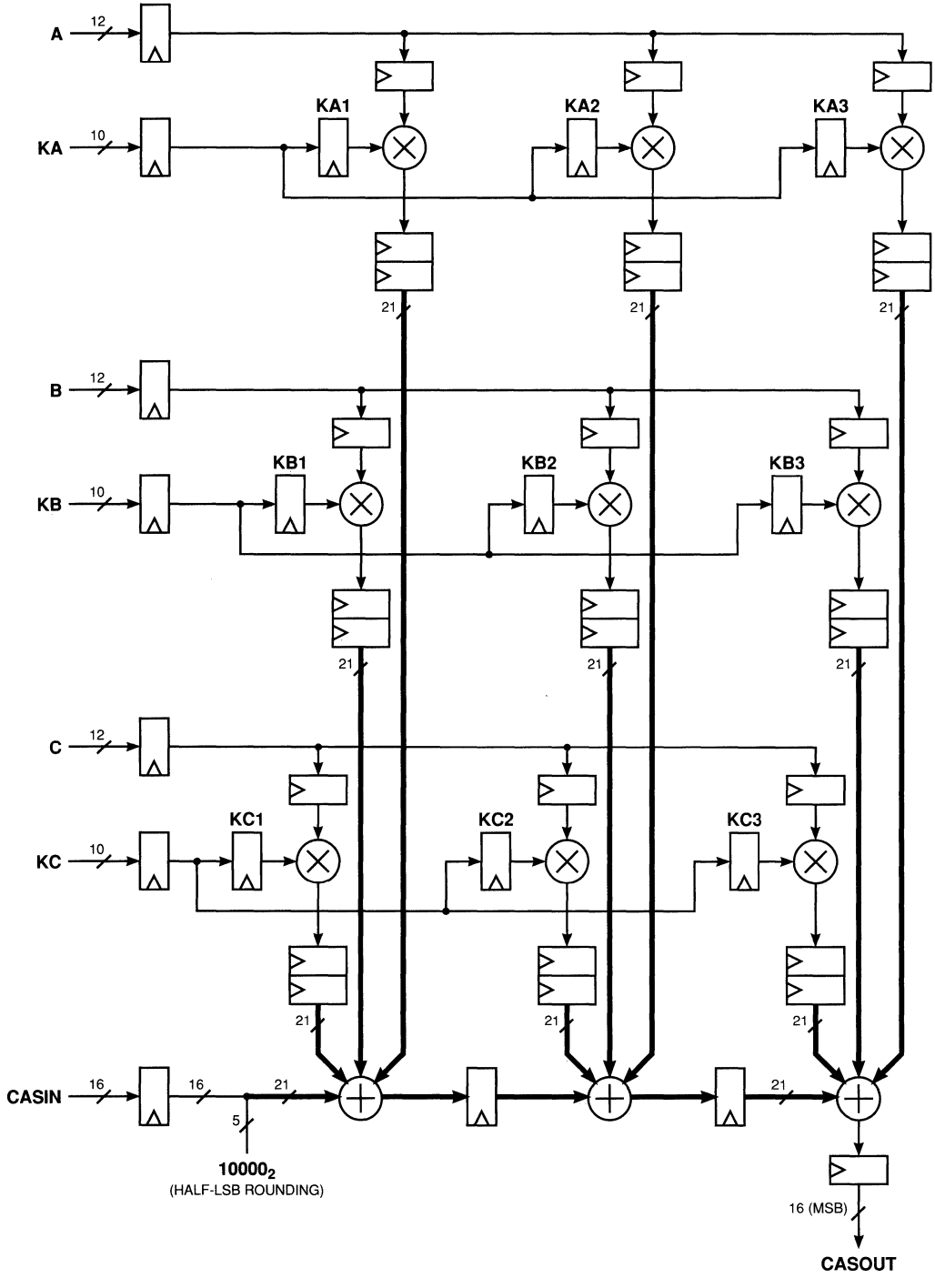
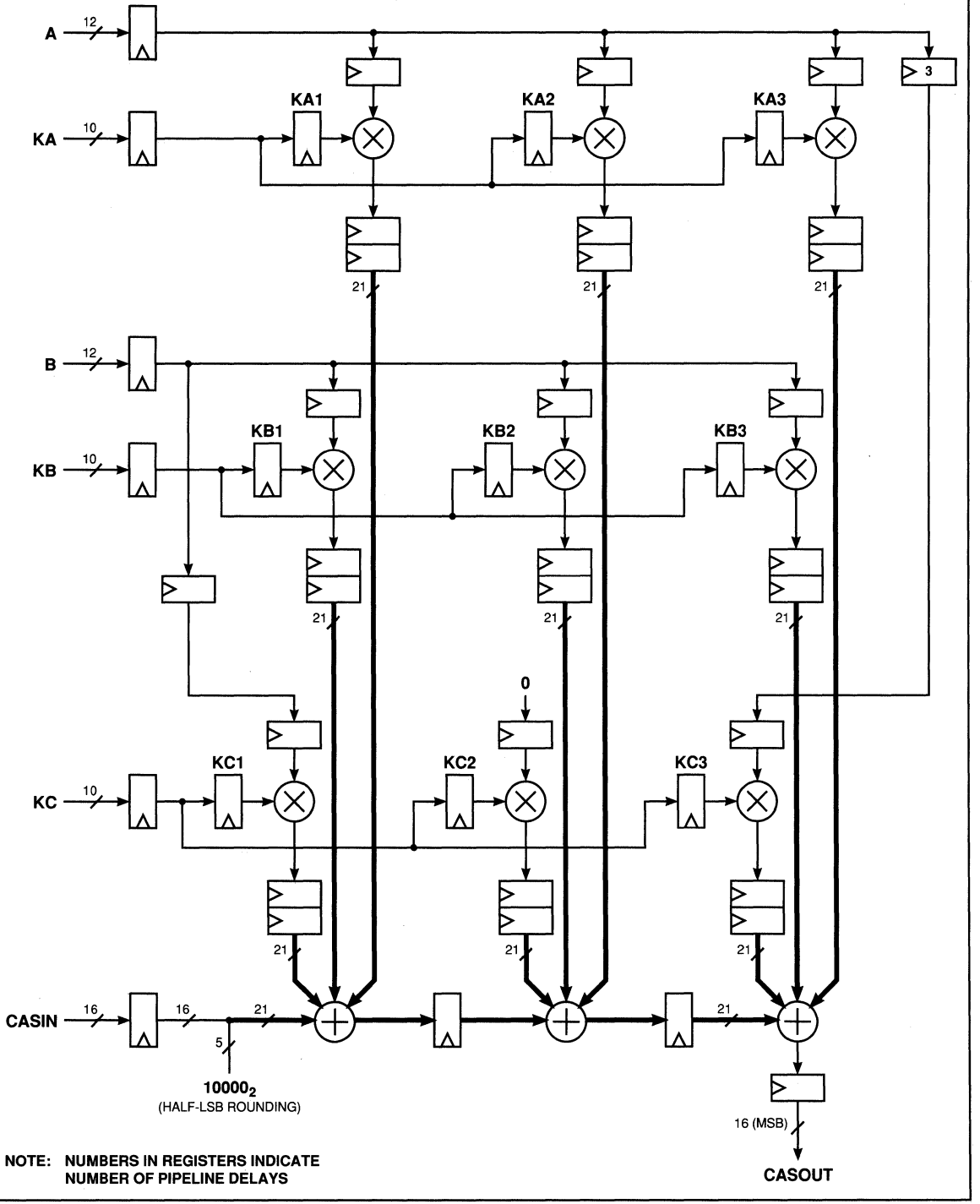


FIGURE 5. 4 X 2-PIXEL CONVOLVER — MODE 11



NOTE: NUMBERS IN REGISTERS INDICATE NUMBER OF PIPELINE DELAYS

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	−0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

2

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			160	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			12	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

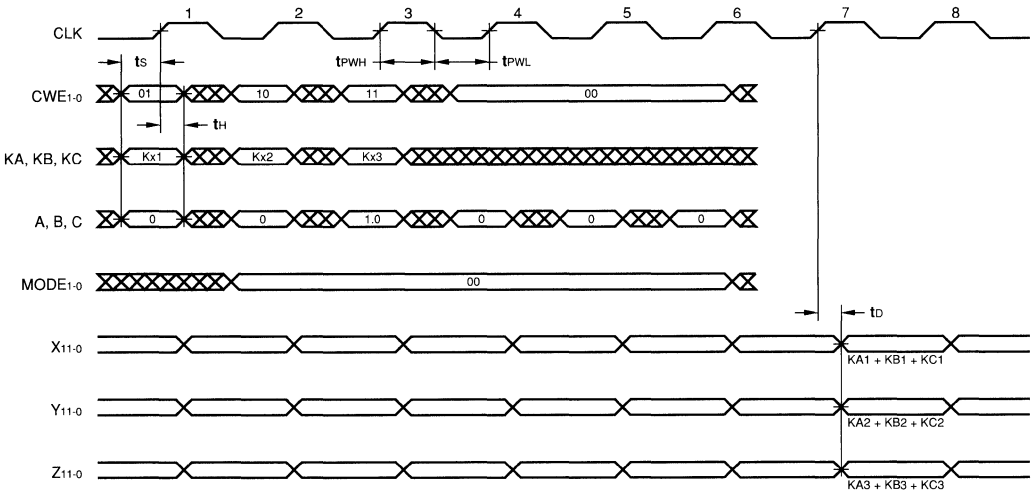
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2250–			
		33		25	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25	
t_{PWL}	Clock Pulse Width, LOW	15		10	
t_{PWH}	Clock Pulse Width, HIGH	10		10	
t_S	Input Setup Time	8		6	
t_H	Input Hold Time	0		0	
t_D	Output Delay		18		16

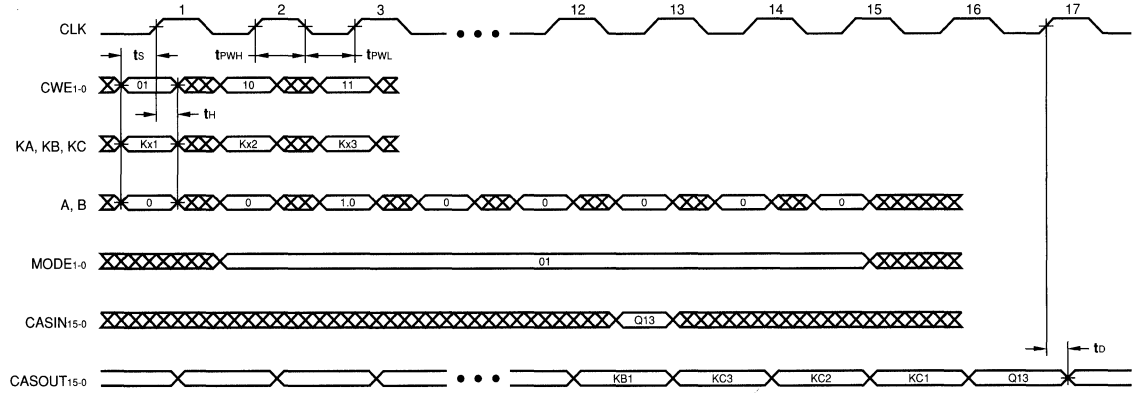
MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2250–			
		33		25	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25	
t_{PWL}	Clock Pulse Width, LOW	15		10	
t_{PWH}	Clock Pulse Width, HIGH	10		10	
t_S	Input Setup Time	12		9	
t_H	Input Hold Time	0		0	
t_D	Output Delay		25		20

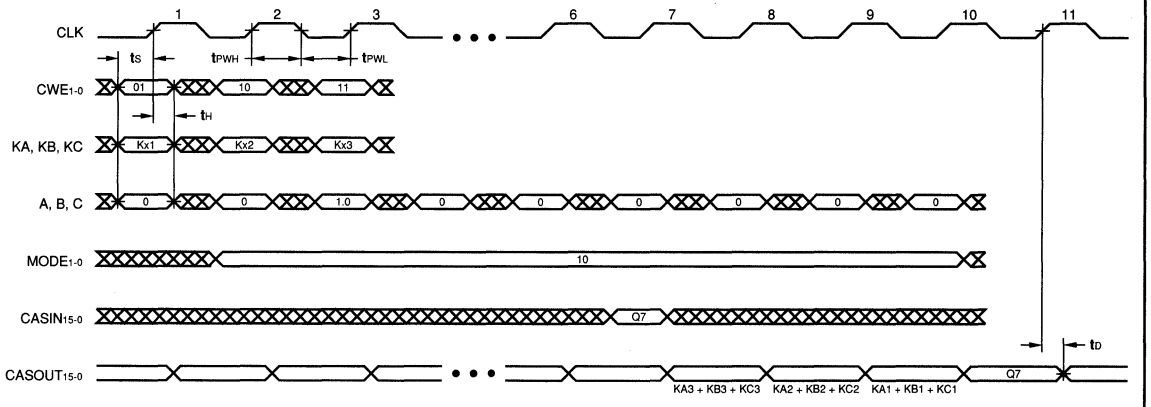
SWITCHING WAVEFORMS: 3 x 3 MATRIX MULTIPLIER — MODE 00



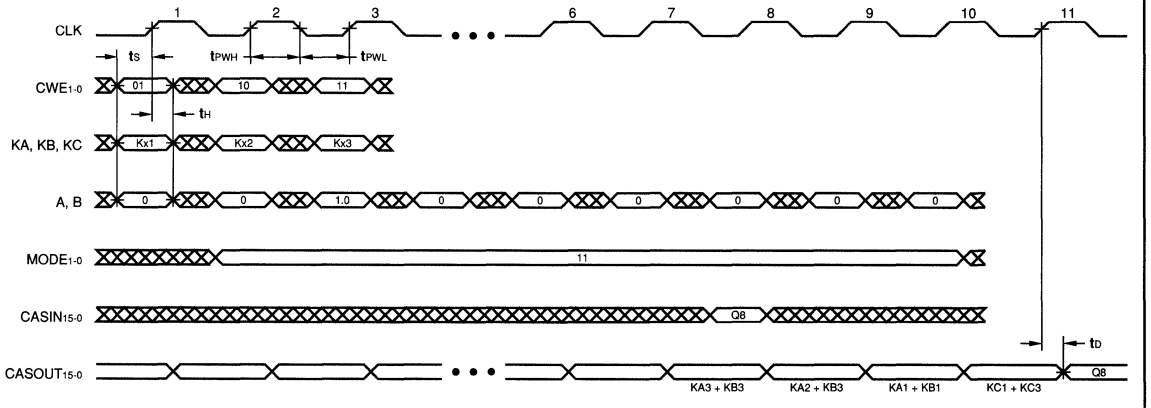
SWITCHING WAVEFORMS: 9-TAP FIR FILTER — MODE 01



Switching Waveforms: 3 x 3-Pixel Convolver — Mode 10



Switching Waveforms: 4 x 2-Pixel Convolver — Mode 11



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 6. INPUT CIRCUIT

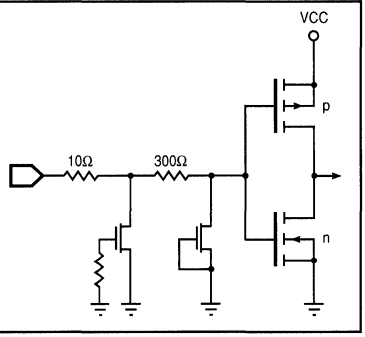


FIGURE 7. OUTPUT CIRCUIT

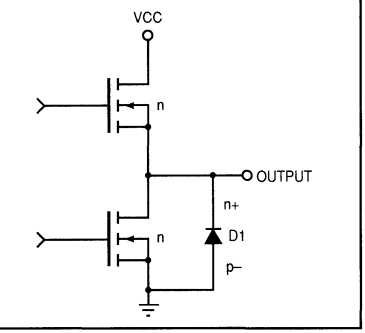
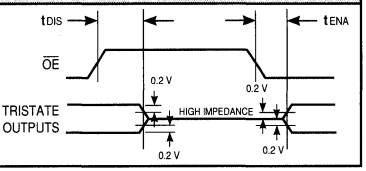
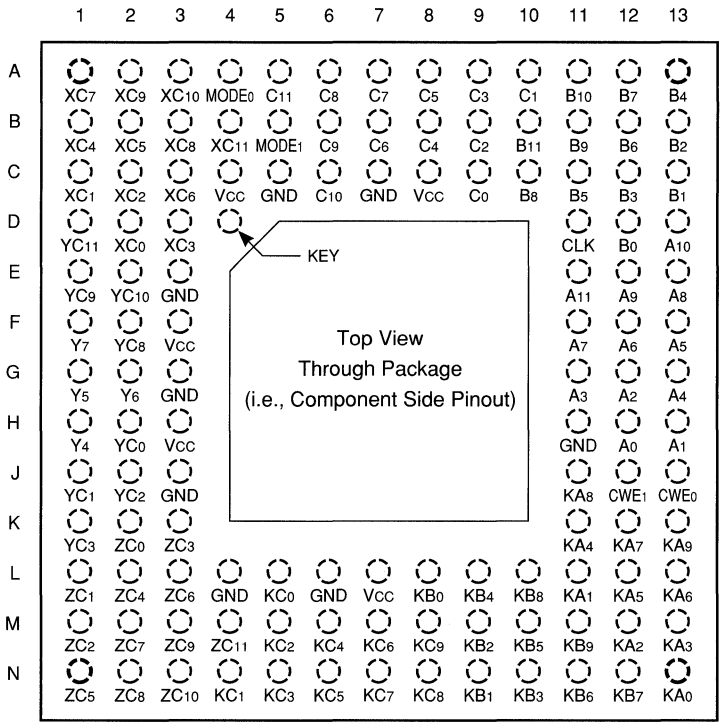


FIGURE 8. THRESHOLD LEVELS



ORDERING INFORMATION

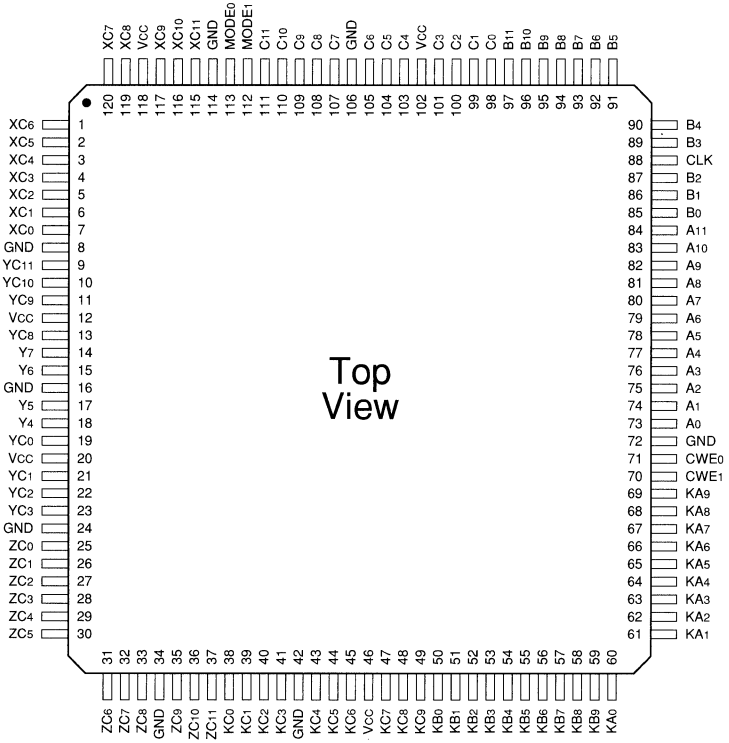
120-pin



Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2250GC33
25 ns	LF2250GC25
	–55°C to +125°C — COMMERCIAL SCREENING
33 ns	LF2250GM33
25 ns	LF2250GM25
	–55°C to +125°C — MIL-STD-883 COMPLIANT
33 ns	LF2250GMB33
25 ns	LF2250GMB25

ORDERING INFORMATION

120-pin



Speed	Plastic Quad Flatpack (Q1)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2250QC33
25 ns	LF2250QC25

LOGIC DEVICES INCORPORATED

LF2272
Colorspace Converter/ Corrector (3 x 12-bits)

FEATURES

- 40 MHz Data and Computation Rate
- Full Precision Internal Calculations with Output Rounding
- On-board 10-bit Coefficient Storage
- Overflow Capability in Low Resolution Applications
- Two's Complement Input and Output Data Format
- 3 Simultaneous 12-bit Channels (64 Giga Colors)
- Applications:
  - Component Color Standards Translations (RGB, YIQ, YUV)
  - Color-Temperature Conversion
  - Image Capturing and Manipulation
  - Composite Color Encoding/ Decoding
  - Three-Dimensional Perspective Translation
- Replaces TRW/Raytheon TMC2272
- 120-pin Pin Grid Array

DESCRIPTION

The **LF2272** is a high-speed digital colorspace converter/corrector consisting of three simultaneous 12-bit input and output channels for functionality up to 64 Giga (2^{36}) colors. Some of the applications the LF2272 can be used for include phosphor colorimetry correction, image capturing and manipulation, composite color encoding/decoding, color matching, and composite color standards conversion/transcoding.

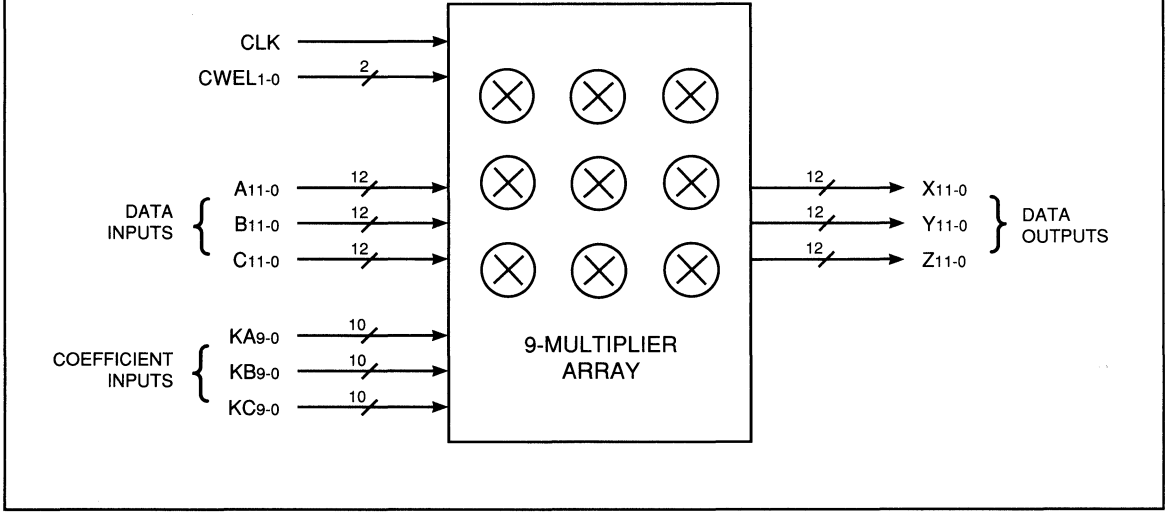
The 3 x 3 matrix multiplier (triple dot product) allows users to easily perform three-dimensional perspective translations or video format conversions at real-time video rates. By using the LF2272, conversions can be made from the RGB (color component) format to the YIQ (quadrature encoded chrominance) or YUV (color difference) formats and vice versa (YIQ or YUV to RGB). Differing signal formats in each stage of a system can be disregarded. For example, using an LF2272 at each format interface allows each stage of a system to operate on the data while in the appropriate format.

All inputs and outputs, as well as all control lines, are registered on the rising edge of clock. The LF2272 operates at clock rates up to 40 MHz over the full commercial temperature and supply voltage ranges. A narrower data path can be used to allow the LF2272 to work with many different imaging applications.

DETAILS OF OPERATION

All three input ports (A, B, C) and all three output ports (X, Y, Z) are utilized to implement a 3 x 3 matrix multiplication (triple dot product). Each truncated 12-bit output is the sum of all three input words multiplied by the appropriate coefficients (Table 1). The pipeline latency is five clock cycles. Therefore, the sum of

LF2272 BLOCK DIAGRAM



products will be output five clock cycles after the input data has been registered. New output data is subsequently available every clock cycle thereafter.

DATA FORMATTING

The data input ports (A, B, C) and data output ports (X, Y, Z) are 12-bit integer two's complement format.

The coefficient input ports (KA, KB, KC) are 10-bit fractional two's complement format. Refer to Figures 1a and 1b.

BIT WEIGHTING

The internal sum of products of the LF2272 can grow to 23 bits. However, in order to keep the output format identical to the input format, the X, Y, and Z outputs are rounded to 12-bit integer words. The rounding is done only at the final output stage to allow accuracy, with correct rounding and overflow, for applications requiring less than 12-bit integer words. The user may adjust the bit weighting by applying an identical scaling correction factor to both the input and output data streams.

TABLE 1. LATENCY EQUATIONS

$$X(n+4) = A(n)KA1(n) + B(n)KB1(n) + C(n)KC1(n)$$
$$Y(n+4) = A(n)KA2(n) + B(n)KB2(n) + C(n)KC2(n)$$
$$Z(n+4) = A(n)KA3(n) + B(n)KB3(n) + C(n)KC3(n)$$

DATA OVERFLOW

Because the LF2272's matched input and output data formats accommodate unity gain (0 dB), input conditions that could lead to numeric overflow may exist. To ensure that no overflow conditions occur, the user must be aware of the maximum input data and coefficient word sizes allowable for each specific algorithm being performed.

SYSTEMS SMALLER THAN 12-BITS

Using a data path less than 12-bits requires the input data to be right justified and sign extended to 12-bits because the LF2272 carries out all calculations to full precision. Since all least-significant bits are used, the desired X, Y, and Z outputs are rounded correctly and upper-order output bits are used for overflow.

FIGURE 1A. INPUT FORMATS

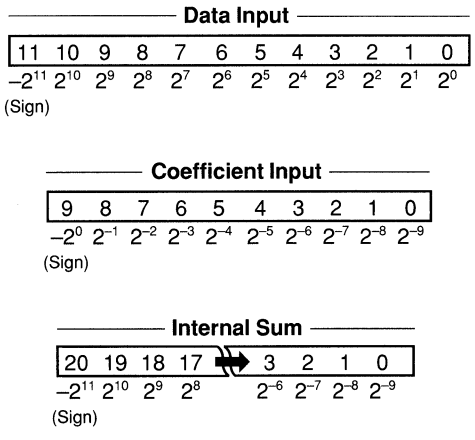
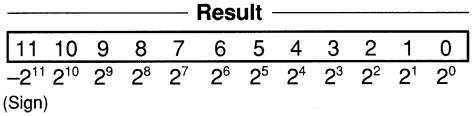


FIGURE 1B. OUTPUT FORMAT



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

A11-0, B11-0, C11-0 — Data Inputs

A, B, and C are the 12-bit registered data input ports. Data presented to these ports is latched into the multiplier input registers.

KA9-0, KB9-0, KC9-0 — Coefficient Inputs

KA, KB, and KC are the 10-bit registered coefficient input ports. Data presented to these ports is latched into the corresponding internal coefficient register set defined by CWEL1-0 (Table 3) on the next rising edge of CLK. Table 2 shows which coefficient registers are available for each coefficient input port.

TABLE 2. COEFFICIENT INPUTS

INPUT PORT	REG. AVAILABLE
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

Outputs

X11-0, Y11-0, Z11-0 — Data Outputs

X, Y, and Z are the 12-bit registered data output ports.

Controls

CWEL1-0 — Coefficient Write Enable

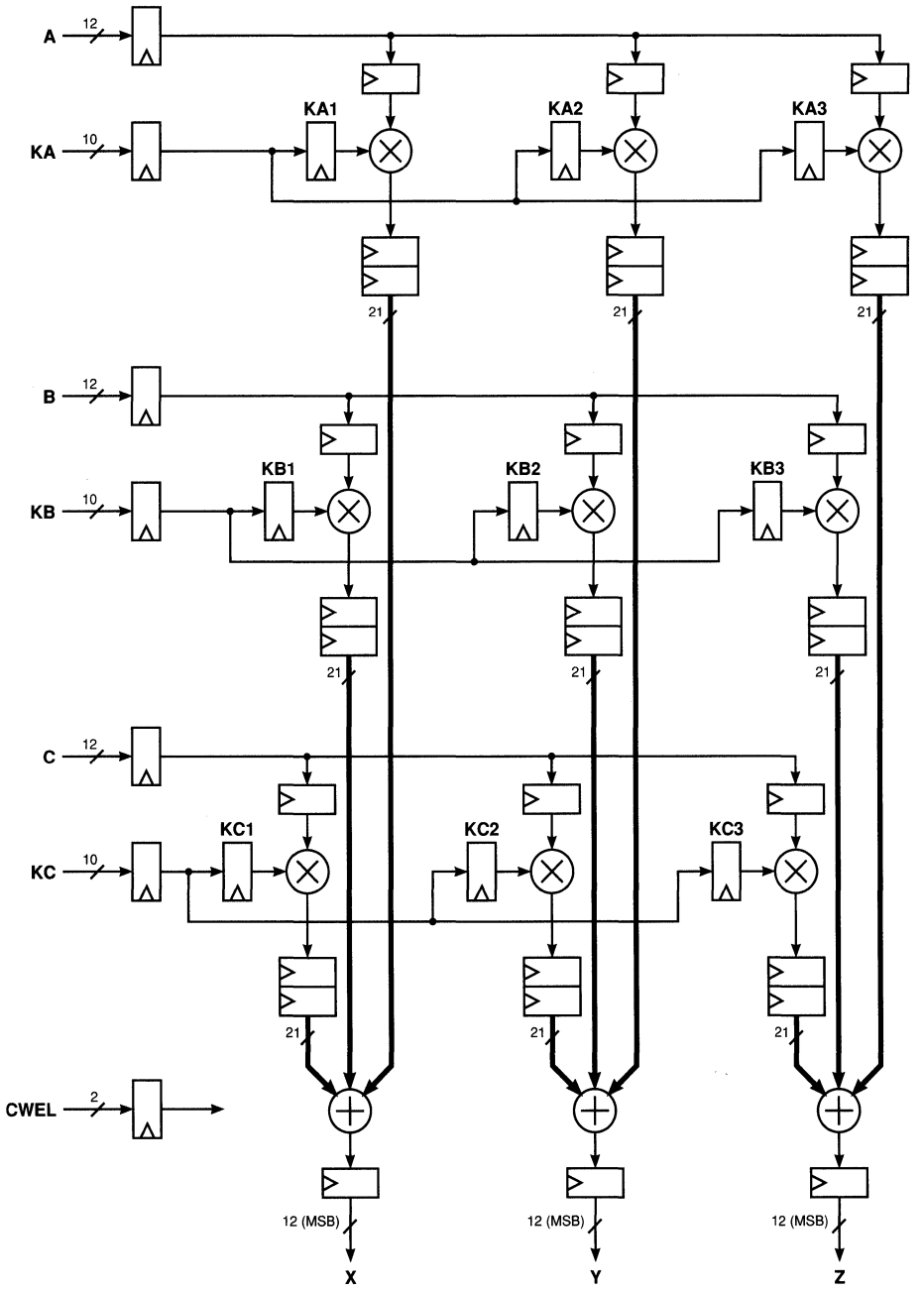
The registered coefficient write enable inputs determine which internal coefficient register set to update (Table 3) on the next clock cycle.

TABLE 3. COEFF. REG. UPDATE

CWEL1-0	COEFFICIENT SET
00	Hold All Registers
01	KA1, KB1, KC1
10	KA2, KB2, KC2
11	KA3, KB3, KC3

2

FIGURE 2. DETAILED FUNCTIONAL DIAGRAM



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	−0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

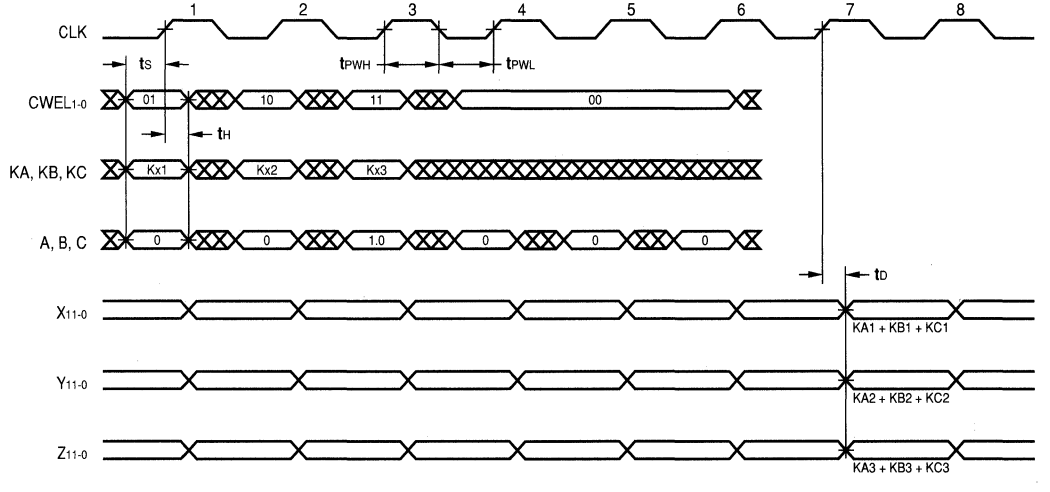
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			160	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			12	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2272–			
		33		25	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**
tCYC	Cycle Time	33		25	
tPWL	Clock Pulse Width, LOW	15		10	
tPWH	Clock Pulse Width, HIGH	10		10	
tS	Input Setup Time	8		6	
tH	Input Hold Time	0		0	
tD	Output Delay		18		16

SWITCHING WAVEFORM



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 3. INPUT CIRCUIT

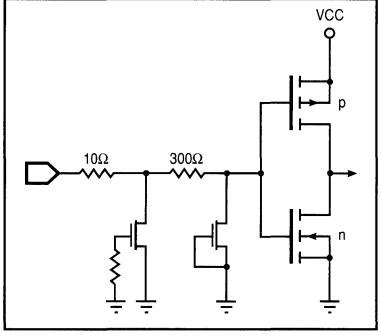


FIGURE 4. OUTPUT CIRCUIT

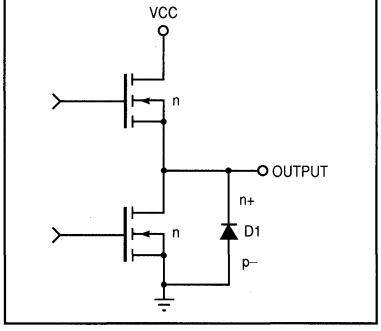
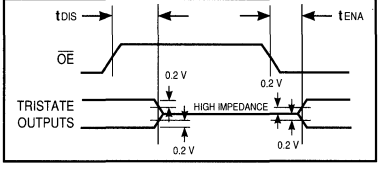
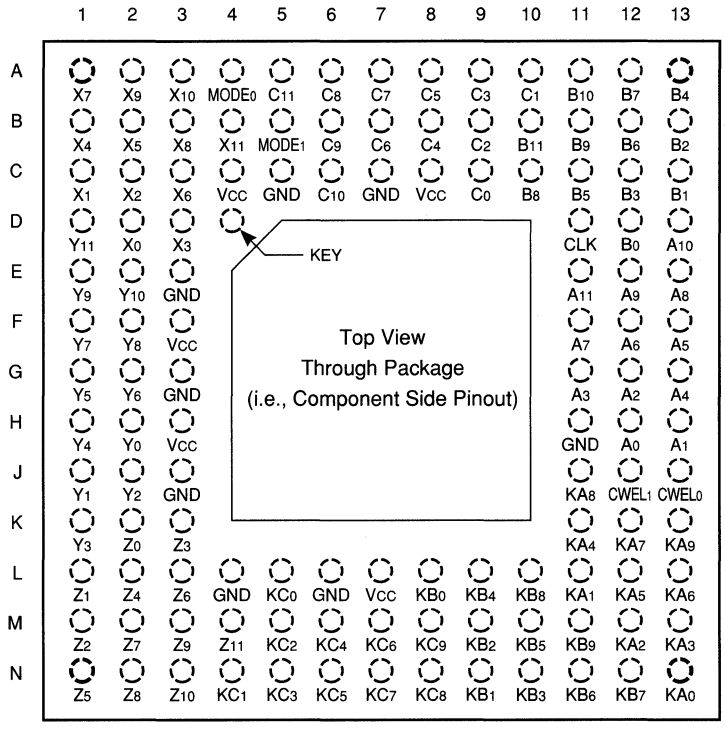


FIGURE 5. THRESHOLD LEVELS



ORDERING INFORMATION

120-pin



Speed	Ceramic Pin Grid Array (G4)
	0°C to +70°C — COMMERCIAL SCREENING
33 ns	LF2272GC33
25 ns	LF2272GC25

FEATURES

- 30 MHz Maximum Sampling Rate
- 240 MHz Multiply-Accumulate Rate
- 8 Filter Cells
- 8-bit Unsigned or Two's Complement Data
- 8-bit Unsigned or Two's Complement Coefficients
- 26-bit Data Outputs
- Shift-and-Add Output Stage for Combining Filter Outputs
- Expandable Data Size, Coefficient Size, and Filter Length
- User-Selectable 2:1, 3:1, or 4:1 Decimation
- Available 100% Screened to MIL-STD-883, Class B
- Replaces Harris HSP43881 and HSP43881/883
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 100-pin Plastic Quad Flatpack
  - 84-pin Ceramic PGA

DESCRIPTION

The **LF43881** is a video-speed digital filter that contains eight filter cells (taps) cascaded internally and a shift-and-add output stage. An 8 x 8 multiplier, three decimation registers, and a 26-bit accumulator are contained in each filter cell. The output stage of the LF43881 contains a 26-bit accumulator which can add the contents of any filter stage to the output stage accumulator shifted right by 8 bits. 8-bit unsigned or two's complement format for data and coefficients can be independently selected.

Expanded coefficients and word sizes can be processed by cascading multiple LF43881s to implement larger filter lengths without affecting the sample rate. By reducing the sample rate, a single LF43881 can process larger filter lengths by using multiple passes. The sampling rate can range from 0 to 30 MHz. Over 1000 taps may be processed without overflows due to the architecture of the device.

The output sample rate can be reduced to one-half, one-third, or one-fourth the input sample rate by using the three decimation registers contained in every filter cell. Matrix multiplication, N x N spatial correlations/convolutions, and other 2-D operations for image processing can also be achieved using these registers.

2

LF43881 BLOCK DIAGRAM

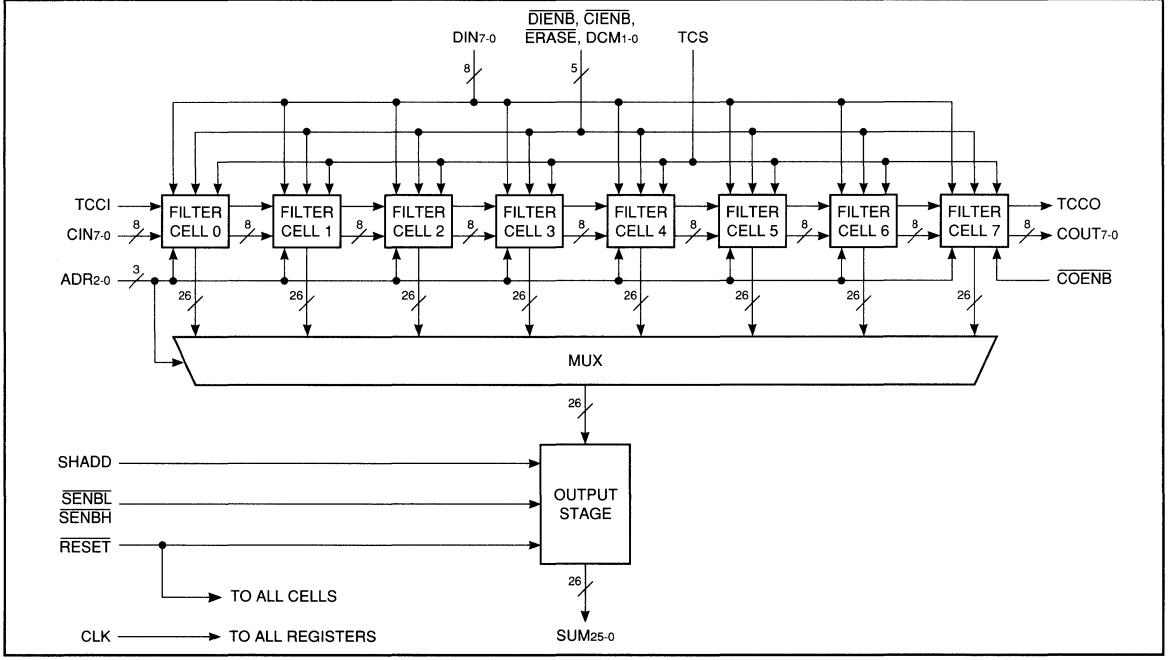
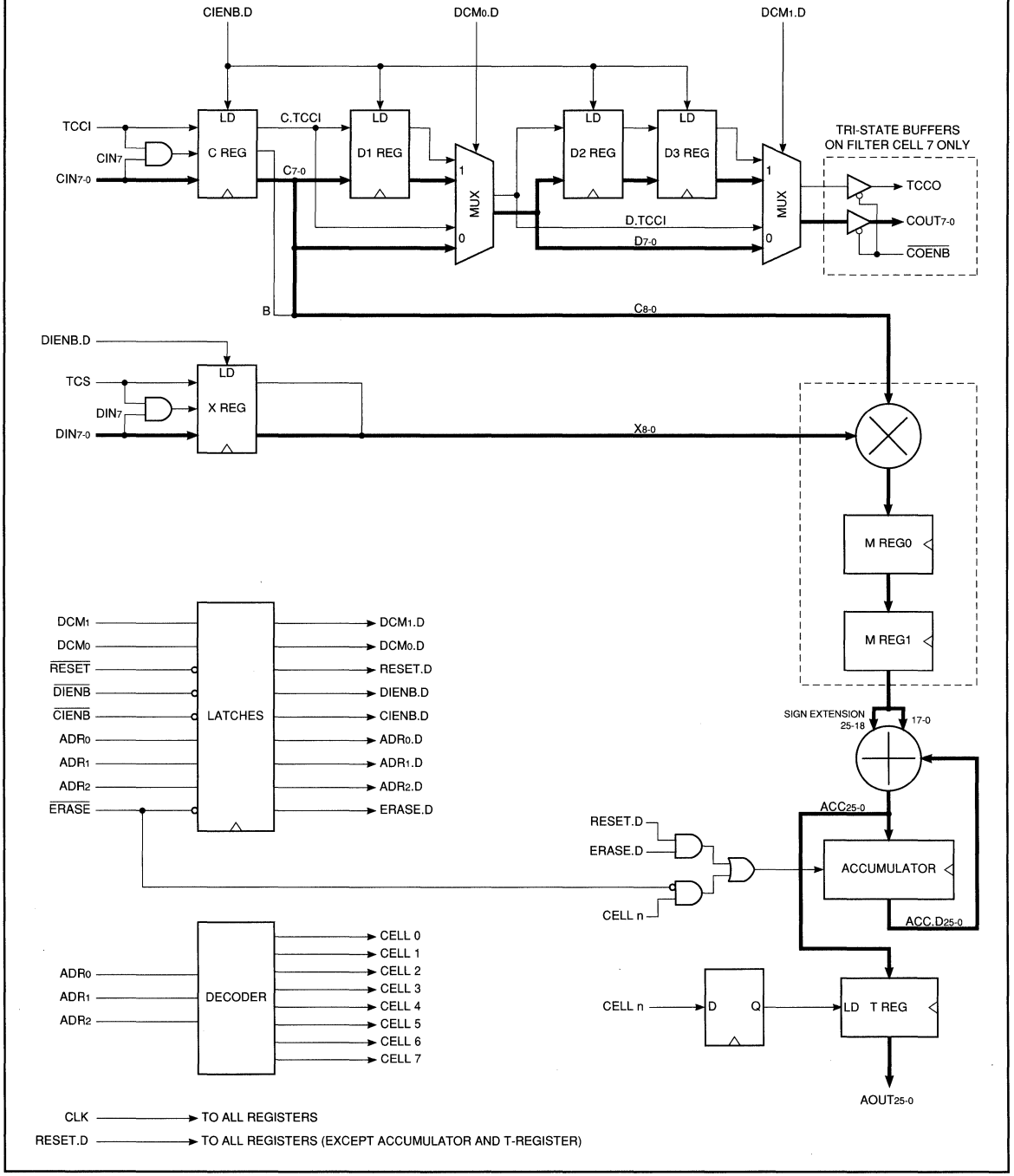


FIGURE 1. FILTER CELL DIAGRAM



FILTER CELL DESCRIPTION

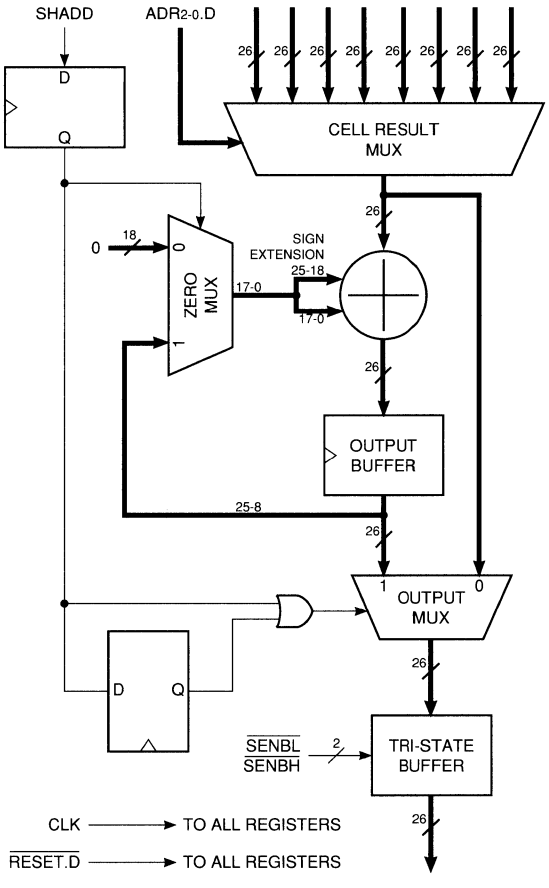
8-bit coefficients are loaded into the C register (CIN7-0) and are output as COUT7-0 (the $\overline{\text{COENB}}$ signal enables the COUT7-0 outputs). The path taken by the coefficients varies according to the decimation mode chosen. With no decimation, the coefficients move directly from the C register, bypassing all decimation registers, and are available at the output on the following clock cycle. When decimation is chosen, the coefficient output is delayed by 1, 2, or 3 clock cycles depending on how many decimation registers the coefficients pass through (D1, D2, or D3). The number of decimation registers the coefficients pass through is determined by DCM1-0. Refer to Table 1 for choosing a decimation mode.

$\overline{\text{CIENB}}$ enables the C and D registers for coefficient loading. The registers are loaded on the rising edge of CLK when $\overline{\text{CIENB}}$ is LOW. $\overline{\text{CIENB}}$ is latched and delayed internally which enables the registers for loading one clock cycle after $\overline{\text{CIENB}}$ goes active (loading takes place on the second rising edge of CLK after $\overline{\text{CIENB}}$ goes LOW). Therefore, $\overline{\text{CIENB}}$ must be LOW one clock cycle before the coefficients are placed on the CIN7-0 inputs. The coefficients are held when $\overline{\text{CIENB}}$ is HIGH.

$\overline{\text{DIENB}}$ enables the X register for the loading of data. The X register is loaded on the rising edge of CLK when $\overline{\text{DIENB}}$ is LOW. $\overline{\text{DIENB}}$ is latched and delayed internally (loading takes place on the second rising edge of CLK after $\overline{\text{DIENB}}$ goes LOW). Therefore, $\overline{\text{DIENB}}$ must be LOW one clock cycle before the data is placed on the DIN7-0 inputs. The X register is loaded with all zeros when $\overline{\text{DIENB}}$ is HIGH.

The output of the C register (C8-0) and X register (X8-0) provide the inputs of the 8 x 8 multiplier. The multiplier is followed by two pipeline registers, M REG0 and M REG1. The output of the multiplier is sign extended and is used as one of the inputs to the 26-bit adder. The output of the 26-bit accumulator provides the second input to the adder. Both the accumulator and T register are loaded simultaneously with the output of the adder.

FIGURE 2. OUTPUT STAGE DIAGRAM



The accumulator is loaded with the output of the adder on every clock cycle unless cleared. Clearing the accumulator can be achieved using two methods. The first method, when both $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are LOW, causes all accumulators and all registers in the device to be cleared together. $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are latched and delayed internally causing the clearing to occur on the second clock cycle after $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ go active.

The second method, when only $\overline{\text{ERASE}}$ is LOW, clears a single accumulator of a selected cell. The cell is selected using the ADR2-0 inputs (decoded to Cell n). $\overline{\text{ERASE}}$ is latched and delayed internally causing the clearing to occur on the second clock cycle after $\overline{\text{ERASE}}$ goes active. Refer to Table 2 for clearing registers and accumulators.

TABLE 1. DECIMATION MODE SELECTION

DCM1	DCM0	Decimation Function
0	0	Decimation registers not used
0	1	One decimation register used (decimation by one-half)
1	0	Two decimation registers used (decimation by one-third)
1	1	Three decimation registers used (decimation by one-fourth)

TABLE 2. REGISTER AND ACCUMULATOR CLEARING

$\overline{ERASE}$	$\overline{RESET}$	Clearing Effect
0	0	All accumulators and all registers are cleared
0	1	Only the accumulator addressed by ADR2-0 is cleared
1	0	All registers are cleared (accumulators are not cleared)
1	1	No clearing occurs, internal state remains the same

OUTPUT STAGE DESCRIPTION

The 26-bit adder contained in the output stage can add the contents of any filter cell accumulator (selected by ADR2-0) with the 18 most significant bits of the output buffer. The result is stored back into the output buffer. The complete operation takes only one clock cycle. The eight least significant bits of the output buffer are lost.

The Zero multiplexer is controlled by the SHADD input signal. This allows selection of either the 18 most significant bits of the output buffer or all zeros for the adder input. When SHADD is LOW, all zeros will be selected. When SHADD is HIGH, the 18 most significant bits of the output buffer are selected enabling the shift-and-add operation. SHADD is latched and delayed internally by one clock cycle.

The output multiplexer is also controlled by the SHADD input signal. This allows selection of either a filter cell accumulator, selected by ADR2-0, or the output buffer to be output to the SUM25-0 bus. Only the 26 least significant bits from either a filter cell accumulator or the output buffer are output on SUM25-0. If SHADD is LOW during two consecutive clock cycles (low during the current and previous clock cycle), the output multiplexer selects the contents of a filter cell accumulator addressed by ADR2-0. Otherwise, the output multiplexer selects the contents of the output buffer.

If the same address remains on the ADR2-0 inputs for more than one clock cycle, SUM25-0 will not change to reflect any updates to the addressed cell accumulator. Only the result from the first selection of the cell (first clock cycle) will be output. This allows the interface of slow memory devices where the output needs to be active for more than one clock cycle. Normal FIR operation is not affected because ADR2-0 is changed sequentially.

NUMBER SYSTEMS

Data and coefficients can be represented as either unsigned or two's complement numbers. The TCS and TCCI inputs determine which of the two formats is to be used. All values are represented as 9-bit two's complement numbers internally. The value of the ninth bit is determined by the number system selected. The ninth bit is a sign extended bit when the two's complement mode is chosen. When the unsigned mode is chosen, the ninth bit is zero.

SIGNAL DEFINITIONS

Power

V_{CC} and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

DIN7-0 — Data Input

8-bit data is latched into the X register of each filter cell simultaneously. The TCS signal selects the appropriate data format type. The $\overline{DIENB}$ signal enables loading of the data.

CIN7-0 — Coefficient Input

8-bit coefficients are latched into the C register of Filter Cell 0. The TCCI signal selects the appropriate coefficient format type. The $\overline{CIENB}$ signal enables loading of the coefficients.

Outputs

SUM25-0 — Data Output

The 26-bit result from an individual filter cell will appear when ADR2-0 is used to select the filter cell result. SHADD in conjunction with ADR2-0 is used to select the output from the shift-and-add output stage.

COUT7-0 — Coefficient Output

The 8-bit coefficient output from Filter Cell 7 can be connected to the CIN7-0 coefficient input of the same LF43881 to recirculate the coefficients. COUT7-0 can also be connected to the CIN7-0 of another LF43881 to cascade the devices. The $\overline{COENB}$ signal enables the output of the coefficients.

Controls

TCS — Data Format Control

The TCS input determines the interpretation of the input data. When TCS is HIGH, two's complement arithmetic is used. When TCS is LOW, unsigned arithmetic is used.

TCCI — Coefficient Input Format Control

The TCCI input determines the interpretation of the coefficients. When TCCI is HIGH, two's complement arithmetic is used. When TCCI is LOW, unsigned arithmetic is used.

TCCO — Coefficient Output Format

The TCCO output shows the format of the COUT7-0 coefficient output. TCCO follows the TCCI input. When cascading multiple LF43881s, the TCCO output of one device should be connected to the TCCI input of another device. The $\overline{\text{COENB}}$ signal enables TCCO.

$\overline{\text{DIENB}}$ — Data Input Enable

The $\overline{\text{DIENB}}$ input enables the X register of every filter cell. While $\overline{\text{DIENB}}$ is LOW, the X registers are loaded with the data present at the DIN7-0 inputs on the rising edge of CLK. While $\overline{\text{DIENB}}$ is HIGH, all bits of DIN7-0 are forced to zero and a rising edge of CLK will load the X register of every filter cell with all zeros. $\overline{\text{DIENB}}$ must be low one clock cycle prior to presenting the input data on the DIN7-0 input since it is latched and delayed internally.

$\overline{\text{CIENB}}$ — Coefficient Input Enable

The $\overline{\text{CIENB}}$ input enables the C and D registers of every filter cell. While $\overline{\text{CIENB}}$ is LOW, the C and appropriate D registers are loaded with the coefficient data on the rising edge of CLK. While $\overline{\text{CIENB}}$ is HIGH, the contents of the C and D registers are held and the CLK signal is ignored. By using $\overline{\text{CIENB}}$ in its active state, coefficient data can be shifted from cell to cell. $\overline{\text{CIENB}}$ must be low one clock cycle prior to presenting the coefficient data on the CIN7-0 input since it is latched and delayed internally.

$\overline{\text{COENB}}$ — Coefficient Output Enable

The $\overline{\text{COENB}}$ input enables the COUT7-0 and TCCO outputs. When $\overline{\text{COENB}}$ is LOW, the outputs are enabled. When $\overline{\text{COENB}}$ is HIGH, the outputs are placed in a high-impedance state.

DCM1-0 — Decimation Control

The DCM1-0 inputs select the number of decimation registers to use (Table 1). Coefficients are passed from one cell to another at a rate determined by DCM1-0. When no decimation registers are selected, the coefficients are passed from cell to cell on every rising edge of CLK (no decimation). When one decimation register is selected, the coefficients are passed from cell to cell on every other rising edge of CLK (2:1 decimation). When two decimation registers are selected, the coefficients are passed from cell to cell on every third rising edge of CLK (3:1 decimation) and so on. DCM1-0 is latched and delayed internally.

ADR2-0 — Cell Accumulator Select

The ADR2-0 inputs select which cell's accumulator will available at the SUM25-0 output or added to the output stage accumulator. In both cases, ADR2-0 is latched and delayed by one clock cycle. If the same address remains on the ADR2-0 inputs for more than one clock cycle, SUM25-0 will not change if the contents of the accumulator changes. Only the result from the first selection of the cell (first clock cycle) by ADR2-0 will be available. ADR2-0 is also used to select which accumulator to clear when $\overline{\text{ERASE}}$ is LOW.

$\overline{\text{SENBH}}$ — MSB Output Enable

When $\overline{\text{SENBH}}$ is LOW, SUM25-16 is enabled. When $\overline{\text{SENBH}}$ is HIGH, SUM25-16 is placed in a high-impedance state.

$\overline{\text{SENBL}}$ — LSB Output Enable

When $\overline{\text{SENBL}}$ is LOW, SUM15-0 is enabled. When $\overline{\text{SENBL}}$ is HIGH, SUM15-0 is placed in a high-impedance state.

$\overline{\text{RESET}}$ — Register Reset Control

When $\overline{\text{RESET}}$ is LOW, all registers are cleared simultaneously except the cell accumulators. $\overline{\text{RESET}}$ can be used with $\overline{\text{ERASE}}$ to clear all cell accumulators. $\overline{\text{RESET}}$ is latched and delayed internally. Refer to Table 2.

$\overline{\text{ERASE}}$ — Accumulator Erase Control

When $\overline{\text{ERASE}}$ is LOW, the cell accumulator specified by ADR2-0 is cleared. When $\overline{\text{RESET}}$ is LOW in conjunction with $\overline{\text{ERASE}}$, all cell accumulators are cleared. Refer to Table 2.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –400 µA	2.6			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			160	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			500	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

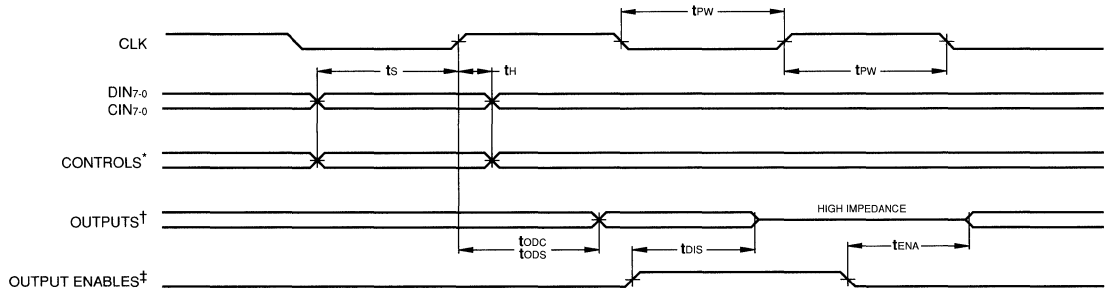
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF43881–					
		50		40		33	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		39		33	
t_{PW}	Clock Pulse Width	20		16		13	
t_S	Input Setup Time	16		14		13	
t_H	Input Hold Time	0		0		0	
t_{ODC}	Coefficient Output Delay		24		20		18
t_{ODS}	Sum Output Delay		27		25		21
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		15		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		20		15		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF43881–			
		50		40	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		39	
t_{PW}	Clock Pulse Width	20		16	
t_S	Input Setup Time	20		17	
t_H	Input Hold Time	0		0	
t_{ODC}	Coefficient Output Delay		24		20
t_{ODS}	Sum Output Delay		31		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		20		15

SWITCHING WAVEFORMS



*includes $\overline{DIENB}$, $\overline{CIENB}$, $\overline{ERASE}$, $\overline{RESET}$, TCS, TCCI, SHADD, DCM_{1-0}, and ADR_{2-0}.
†includes TCCO, SUM_{25-0}, and $COUT_{7-0}$.
‡includes $\overline{SENBL}$, $\overline{SENBH}$, and $\overline{COENB}$.

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 3. INPUT CIRCUIT

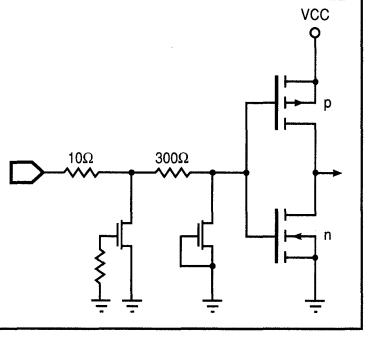


FIGURE 4. OUTPUT CIRCUIT

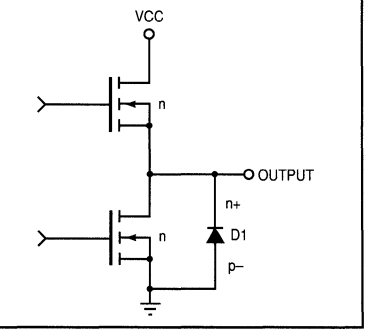
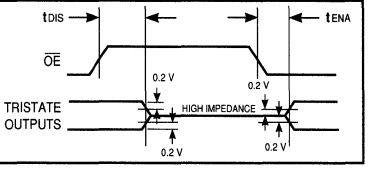
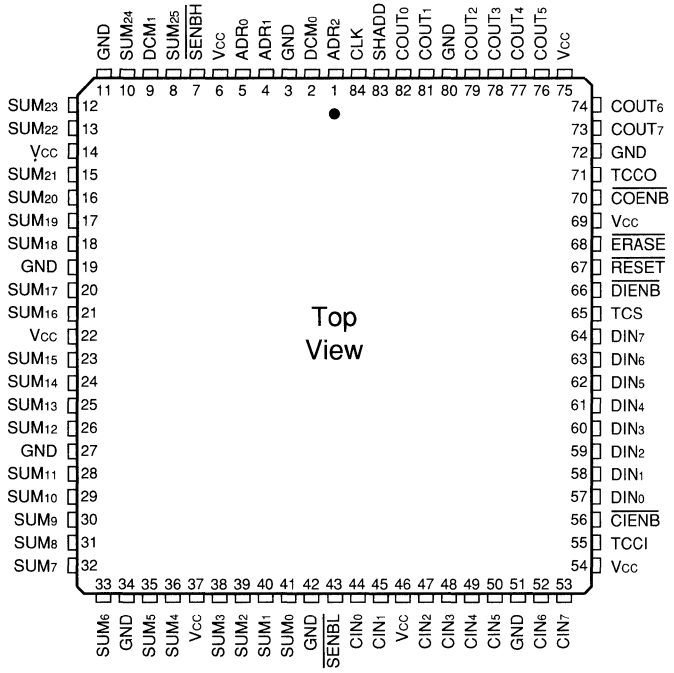


FIGURE 5. THRESHOLD LEVELS



ORDERING INFORMATION

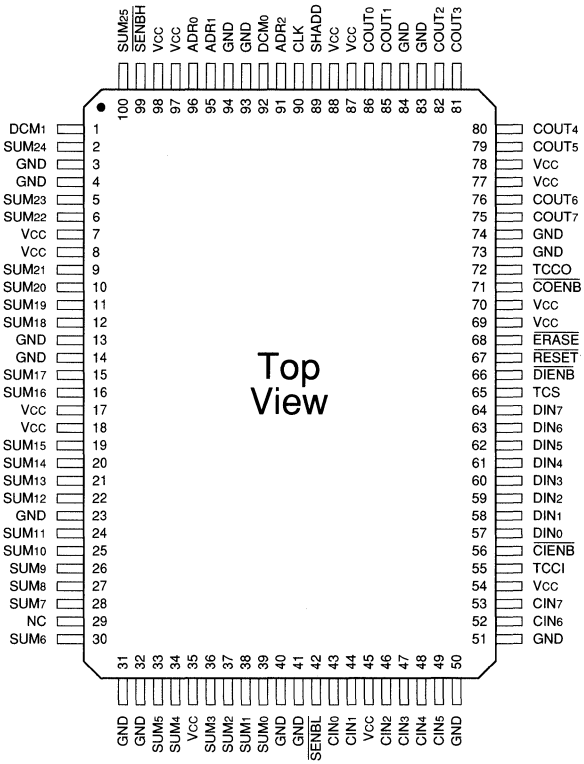
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43881JC50
40 ns	LF43881JC40
33 ns	LF43881JC33

ORDERING INFORMATION

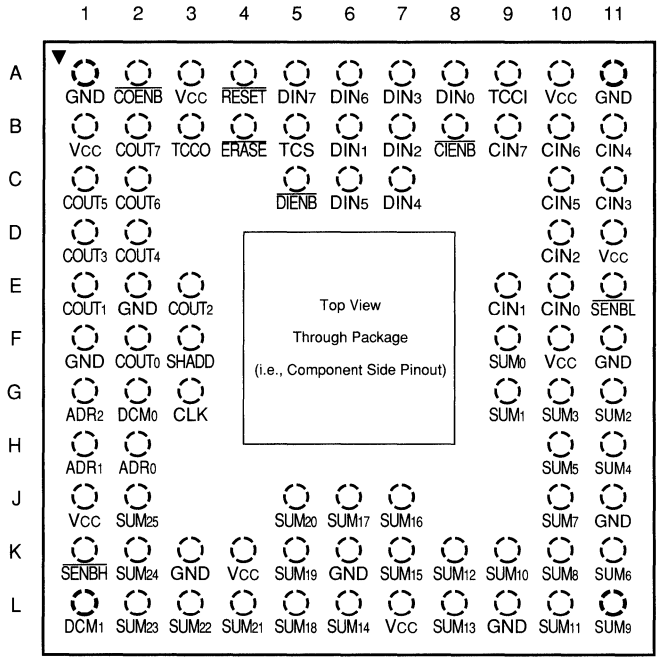
100-pin



Speed	Plastic Quad Flatpack (Q2)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43881QC50
40 ns	LF43881QC40
33 ns	LF43881QC33

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — Commercial Screening
50 ns	LF43881GC50
40 ns	LF43881GC40
33 ns	LF43881GC33
	–55°C to +125°C — Commercial Screening
50 ns	LF43881GM50
40 ns	LF43881GM40
	–55°C to +125°C — MIL-STD-883 Compliant
50 ns	LF43881GMB50
40 ns	LF43881GMB40

LF43891
9 x 9-bit Digital Filter

FEATURES

- 30 MHz Maximum Sampling Rate
- 240 MHz Multiply-Accumulate Rate
- 8 Filter Cells
- 8-bit Unsigned or 9-bit Two's Complement Data
- 8-bit Unsigned or 9-bit Two's Complement Coefficients
- 26-bit Data Outputs
- Shift-and-Add Output Stage for Combining Filter Outputs
- Expandable Data Size, Coefficient Size, and Filter Length
- User-Selectable 2:1, 3:1, or 4:1 Decimation
- Available 100% Screened to MIL-STD-883, Class B
- Replaces Harris HSP43891 and HSP43891/883
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 100-pin Plastic Quad Flatpack
  - 84-pin Ceramic PGA

DESCRIPTION

The **LF43891** is a video-speed digital filter that contains eight filter cells (taps) cascaded internally and a shift-and-add output stage. A 9 x 9 multiplier, three decimation registers, and a 26-bit accumulator are contained in each filter cell. The output stage of the LF43891 contains a 26-bit accumulator which can add the contents of any filter stage to the output stage accumulator shifted right by 8 bits. 8-bit unsigned or 9-bit two's complement format for data and coefficients can be independently selected.

Expanded coefficients and word sizes can be processed by cascading multiple LF43891s to implement larger filter lengths without affecting the sample rate. By reducing the sample rate, a single LF43891 can process larger filter lengths by using multiple passes. The sampling rate can range from 0 to 30 MHz. Over 1000 taps may be processed without overflows due to the architecture of the device.

The output sample rate can be reduced to one-half, one-third, or one-fourth the input sample rate by using the three decimation registers contained in every filter cell. Matrix multiplication, N x N spatial correlations/convolutions, and other 2-D operations for image processing can also be achieved using these registers.

LF43891 BLOCK DIAGRAM

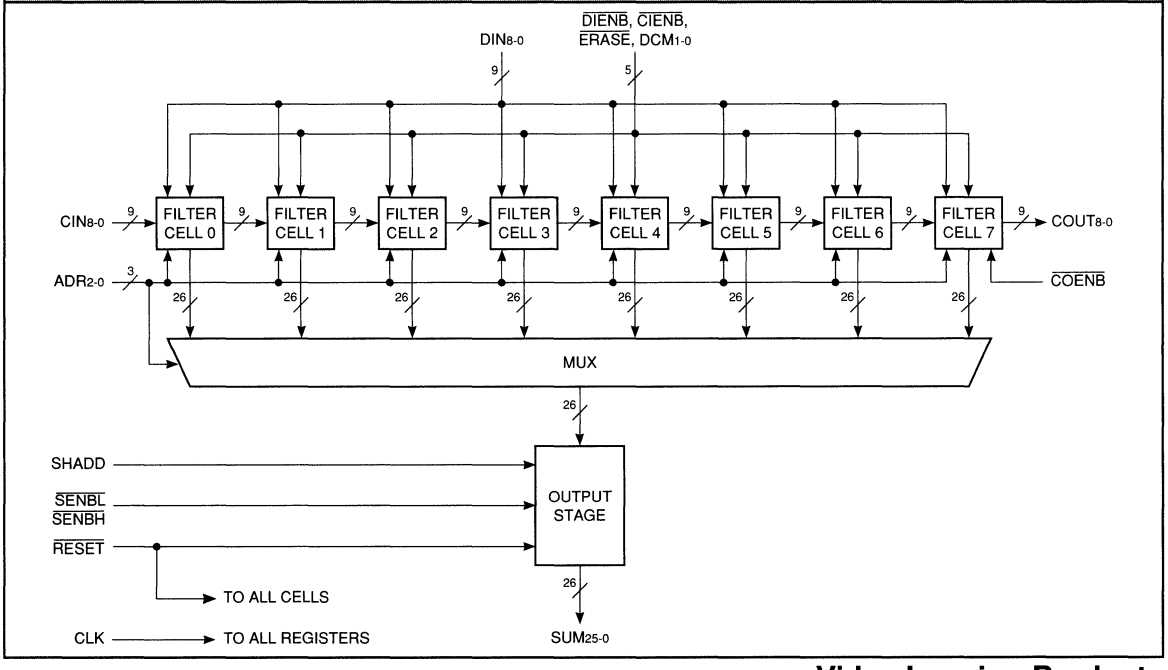
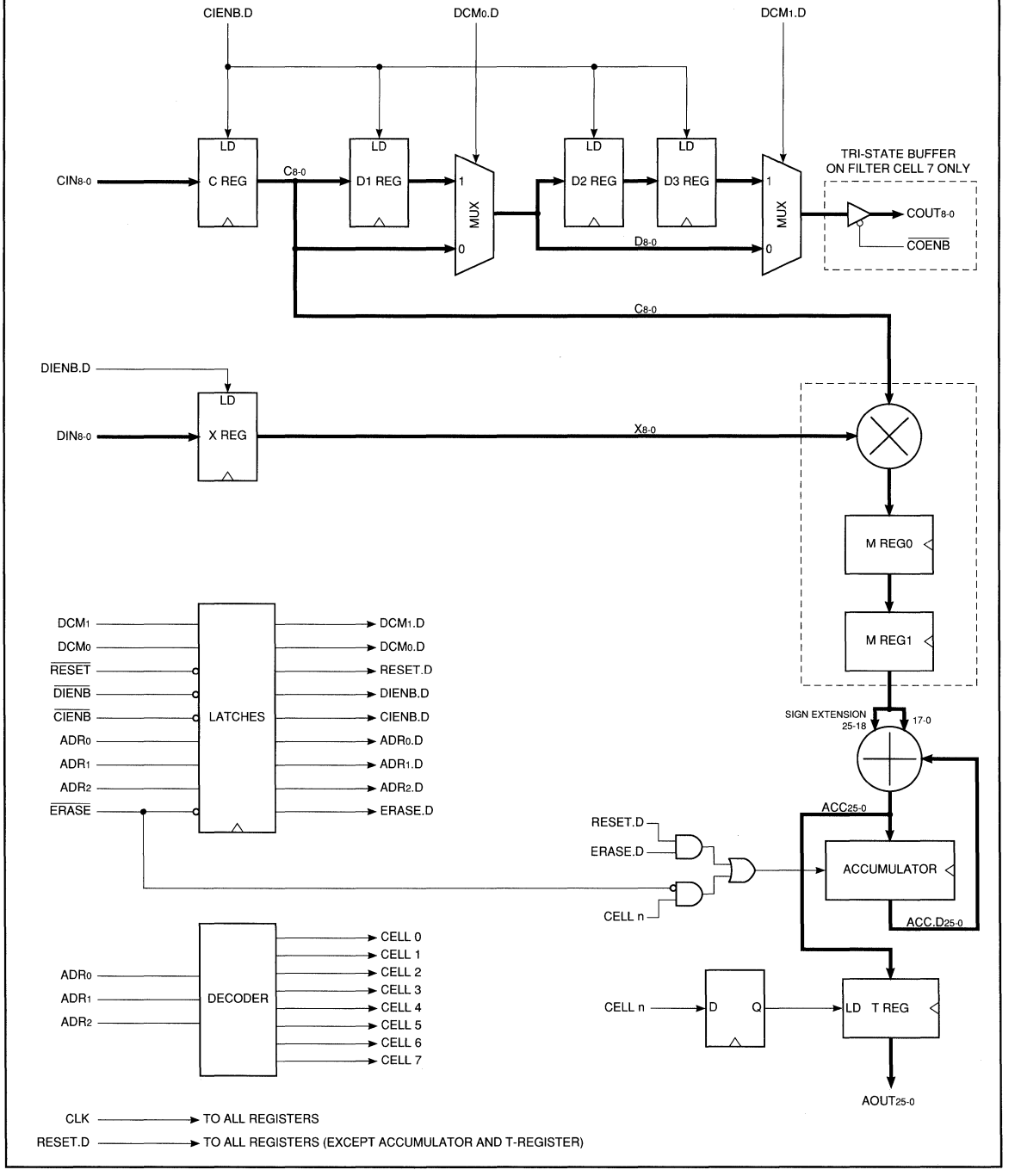


FIGURE 1. FILTER CELL DIAGRAM



FILTER CELL DESCRIPTION

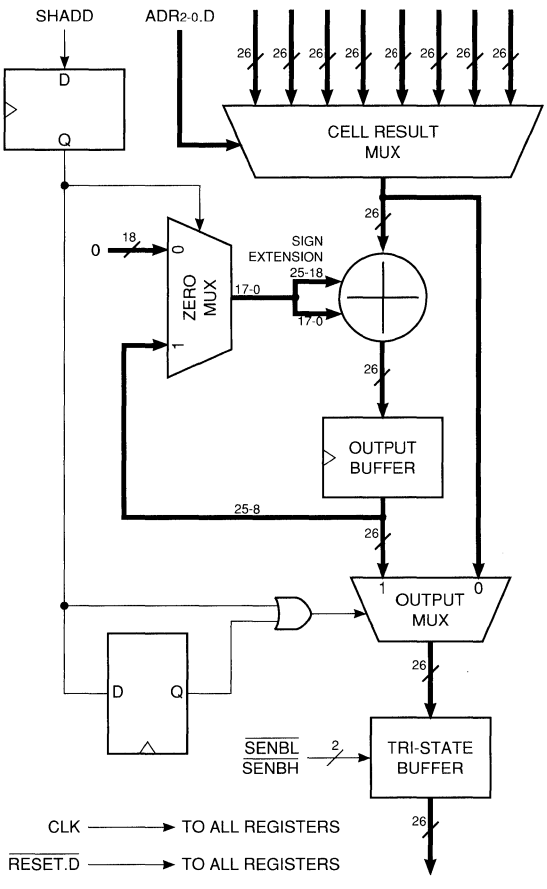
9-bit coefficients are loaded into the C register (CIN8-0) and are output as COUT8-0 (the $\overline{\text{COENB}}$ signal enables the COUT8-0 outputs). The path taken by the coefficients varies according to the decimation mode chosen. With no decimation, the coefficients move directly from the C register, bypassing all decimation registers, and are available at the output on the following clock cycle. When decimation is chosen, the coefficient output is delayed by 1, 2, or 3 clock cycles depending on how many decimation registers the coefficients pass through (D1, D2, or D3). The number of decimation registers the coefficients pass through is determined by DCM1-0. Refer to Table 1 for choosing a decimation mode.

$\overline{\text{CIENB}}$ enables the C and D registers for coefficient loading. The registers are loaded on the rising edge of CLK when $\overline{\text{CIENB}}$ is LOW. $\overline{\text{CIENB}}$ is latched and delayed internally which enables the registers for loading one clock cycle after $\overline{\text{CIENB}}$ goes active (loading takes place on the second rising edge of CLK after $\overline{\text{CIENB}}$ goes LOW). Therefore, $\overline{\text{CIENB}}$ must be LOW one clock cycle before the coefficients are placed on the CIN8-0 inputs. The coefficients are held when $\overline{\text{CIENB}}$ is HIGH.

$\overline{\text{DIENB}}$ enables the X register for the loading of data. The X register is loaded on the rising edge of CLK when $\overline{\text{DIENB}}$ is LOW. $\overline{\text{DIENB}}$ is latched and delayed internally (loading takes place on the second rising edge of CLK after $\overline{\text{DIENB}}$ goes LOW). Therefore, $\overline{\text{DIENB}}$ must be LOW one clock cycle before the data is placed on the DIN8-0 inputs. The X register is loaded with all zeros when $\overline{\text{DIENB}}$ is HIGH.

The output of the C register (C8-0) and X register (X8-0) provide the inputs of the 9 x 9 multiplier. The multiplier is followed by two pipeline registers,

FIGURE 2. OUTPUT STAGE DIAGRAM



M REG0 and M REG1. The output of the multiplier is sign extended and is used as one of the inputs to the 26-bit adder. The output of the 26-bit accumulator provides the second input to the adder. Both the accumulator and T register are loaded simultaneously with the output of the adder.

The accumulator is loaded with the output of the adder on every clock cycle unless cleared. Clearing the accumulator can be achieved using two methods. The first method, when both $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are LOW, causes all accumulators and all registers in the device to be cleared together. $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ are latched and delayed internally causing the clearing to occur on the second clock cycle after $\overline{\text{RESET}}$ and $\overline{\text{ERASE}}$ go active.

The second method, when only $\overline{\text{ERASE}}$ is LOW, clears a single accumulator of a selected cell. The cell is selected using the ADR2-0 inputs (decoded to Cell n). $\overline{\text{ERASE}}$ is latched and delayed internally causing the clearing to occur on the second clock cycle after $\overline{\text{ERASE}}$ goes active. Refer to Table 2 for clearing registers and accumulators.

TABLE 1. DECIMATION MODE SELECTION

DCM1	DCM0	Decimation Function
0	0	Decimation registers not used
0	1	One decimation register used (decimation by one-half)
1	0	Two decimation registers used (decimation by one-third)
1	1	Three decimation registers used (decimation by one-fourth)

TABLE 2. REGISTER AND ACCUMULATOR CLEARING

$\overline{ERASE}$	$\overline{RESET}$	Clearing Effect
0	0	All accumulators and all registers are cleared
0	1	Only the accumulator addressed by ADR2-0 is cleared
1	0	All registers are cleared (accumulators are not cleared)
1	1	No clearing occurs, internal state remains the same

OUTPUT STAGE DESCRIPTION

The 26-bit adder contained in the output stage can add the contents of any filter cell accumulator (selected by ADR2-0) with the 18 most significant bits of the output buffer. The result is stored back into the output buffer. The complete operation takes only one clock cycle. The eight least significant bits of the output buffer are lost.

The Zero multiplexer is controlled by the SHADD input signal. This allows selection of either the 18 most significant bits of the output buffer or all zeros for the adder input. When SHADD is LOW, all zeros will be selected. When SHADD is HIGH, the 18 most significant bits of the output buffer are selected enabling the shift-and-add operation. SHADD is latched and delayed internally by one clock cycle.

The output multiplexer is also controlled by the SHADD input signal. This allows selection of either a filter cell accumulator, selected by ADR2-0, or the output buffer to be output to the SUM25-0 bus. Only the 26 least significant bits from either a filter cell accumulator or the output buffer are output on SUM25-0. If SHADD is LOW during two consecutive clock cycles (low during the current and previous clock cycle), the output multiplexer selects the contents of a filter cell accumulator addressed by ADR2-0. Otherwise, the output multiplexer selects the contents of the output buffer.

If the same address remains on the ADR2-0 inputs for more than one clock cycle, SUM25-0 will not change to reflect any updates to the addressed cell accumulator. Only the result from the first selection of the cell (first clock cycle) will be output. This allows the interface of slow memory devices where the output needs to be active for more than one clock cycle. Normal FIR operation is not affected because ADR2-0 is changed sequentially.

NUMBER SYSTEMS

Data and coefficients can be represented as either 8-bit unsigned or 9-bit two's complement numbers. All values are represented as 9-bit two's complement numbers internally. If the most significant or sign bit is a zero, the multiplier can multiply 8-bit unsigned numbers.

SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers. All timing specifications are referenced to the rising edge of CLK.

Inputs

DIN8-0 — Data Input

9-bit data is latched into the X register of each filter cell simultaneously. The $\overline{DIENB}$ signal enables loading of the data.

CIN8-0 — Coefficient Input

9-bit coefficients are latched into the C register of Filter Cell 0. The $\overline{CIENB}$ signal enables loading of the coefficients.

Outputs

SUM25-0 — Data Output

The 26-bit result from an individual filter cell will appear when ADR2-0 is used to select the filter cell result. SHADD in conjunction with ADR2-0 is used to select the output from the shift-and-add output stage.

COUT8-0 — Coefficient Output

The 9-bit coefficient output from Filter Cell 7 can be connected to the CIN8-0 coefficient input of the same LF43891 to recirculate the coefficients. COUT8-0 can also be connected to the CIN8-0 of another LF43891 to cascade the devices. The $\overline{COENB}$ signal enables the output of the coefficients.

Controls

$\overline{DIENB}$ — Data Input Enable

The $\overline{DIENB}$ input enables the X register of every filter cell. While $\overline{DIENB}$ is LOW, the X registers are loaded with the data present at the DIN8-0 inputs on the rising edge of CLK. While $\overline{DIENB}$ is HIGH, all bits of DIN8-0 are forced to zero and a rising edge of CLK will load the X register of every filter cell with all zeros. $\overline{DIENB}$ must be low one clock cycle prior to presenting the input data on the DIN8-0 input since it is latched and delayed internally.

$\overline{CIENB}$ — Coefficient Input Enable

The $\overline{CIENB}$ input enables the C and D registers of every filter cell. While $\overline{CIENB}$ is LOW, the C and appropriate D registers are loaded with the coefficient data on the rising edge of CLK. While $\overline{CIENB}$ is HIGH, the contents of the C and D registers are held and the CLK signal is ignored. By using $\overline{CIENB}$ in its active state, coefficient data can be shifted from cell to cell. $\overline{CIENB}$ must be low one clock cycle prior to presenting the coefficient data on the CIN8-0 input since it is latched and delayed internally.

$\overline{COENB}$ — Coefficient Output Enable

The $\overline{COENB}$ input enables the COUT8-0 output. When $\overline{COENB}$ is LOW, the outputs are enabled. When $\overline{COENB}$ is HIGH, the outputs are placed in a high-impedance state.

DCM1-0 — Decimation Control

The DCM1-0 inputs select the number of decimation registers to use (Table 1). Coefficients are passed from one cell to another at a rate determined by DCM1-0. When no decimation registers are selected, the coefficients are passed from cell to cell on every rising edge of CLK (no decimation). When one decimation register is selected, the coefficients are passed from cell to cell on every other rising edge of CLK (2:1 decimation). When two decimation registers are selected, the coefficients are passed from cell to cell on every third rising edge of CLK (3:1 decimation) and so on. DCM1-0 is latched and delayed internally.

ADR2-0 — Cell Accumulator Select

The ADR2-0 inputs select which cell's accumulator will available at the SUM25-0 output or added to the output stage accumulator. In both cases, ADR2-0 is latched and delayed by one clock cycle. If the same address remains on the ADR2-0 inputs for more than one clock cycle, SUM25-0 will not change if the contents of the accumulator changes. Only the result from the first selection of the cell (first clock cycle) by ADR2-0 will be available. ADR2-0 is also used to select which accumulator to clear when $\overline{ERASE}$ is LOW.

$\overline{SENBH}$ — MSB Output Enable

When $\overline{SENBH}$ is LOW, SUM25-16 is enabled. When $\overline{SENBH}$ is HIGH, SUM25-16 is placed in a high-impedance state.

$\overline{SENBL}$ — LSB Output Enable

When $\overline{SENBL}$ is LOW, SUM15-0 is enabled. When $\overline{SENBL}$ is HIGH, SUM15-0 is placed in a high-impedance state.

$\overline{RESET}$ — Register Reset Control

When $\overline{RESET}$ is LOW, all registers are cleared simultaneously except the cell accumulators. $\overline{RESET}$ can be used with $\overline{ERASE}$ to clear all cell accumulators. $\overline{RESET}$ is latched and delayed internally. Refer to Table 2.

$\overline{ERASE}$ — Accumulator Erase Control

When $\overline{ERASE}$ is LOW, the cell accumulator specified by ADR2-0 is cleared. When $\overline{RESET}$ is LOW in conjunction with $\overline{ERASE}$, all cell accumulators are cleared. Refer to Table 2.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –400 µA	2.6			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	(Note 12)			±10	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			160	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			500	µA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

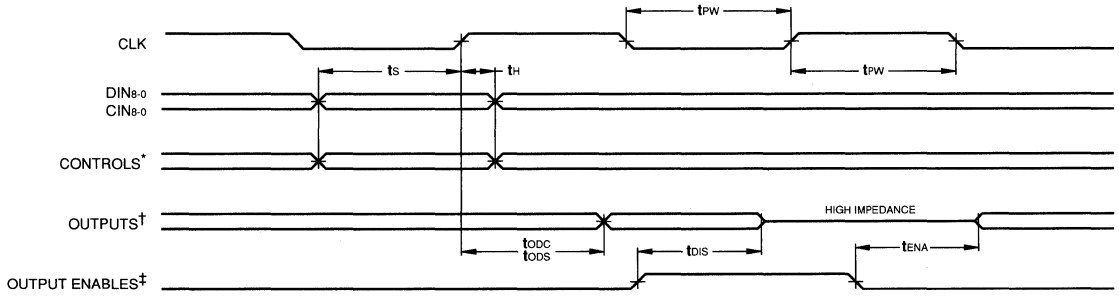
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF43891–					
		50		40		33	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		39		33	
t_{PW}	Clock Pulse Width	20		16		13	
t_S	Input Setup Time	16		14		13	
t_H	Input Hold Time	0		0		0	
t_{ODC}	Coefficient Output Delay		24		20		18
t_{ODS}	Sum Output Delay		27		25		21
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		15		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		20		15		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF43891–			
		50		40	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	50		39	
t_{PW}	Clock Pulse Width	20		16	
t_S	Input Setup Time	20		17	
t_H	Input Hold Time	0		0	
t_{ODC}	Coefficient Output Delay		24		20
t_{ODS}	Sum Output Delay		31		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		20		15

SWITCHING WAVEFORMS



*includes $\overline{DIENB}$, $\overline{CIENB}$, $\overline{ERASE}$, $\overline{RESET}$, SHADD, DCM_{1-0}, and ADR_{2-0}.
†includes SUM_{25-0} and $COUT_{8-0}$.
‡includes $\overline{SENBL}$, $\overline{SENBH}$, and $\overline{COENB}$.

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 20 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 3. INPUT CIRCUIT

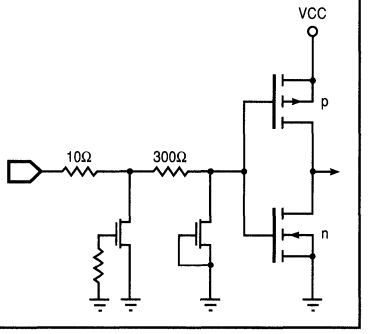


FIGURE 4. OUTPUT CIRCUIT

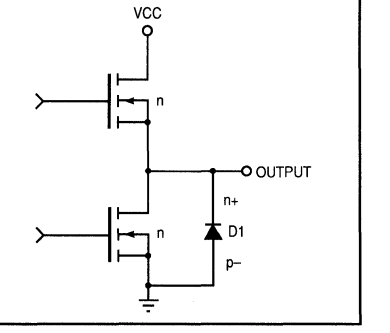
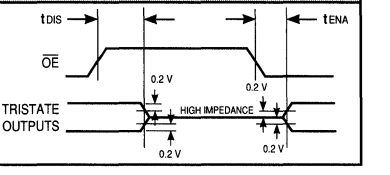
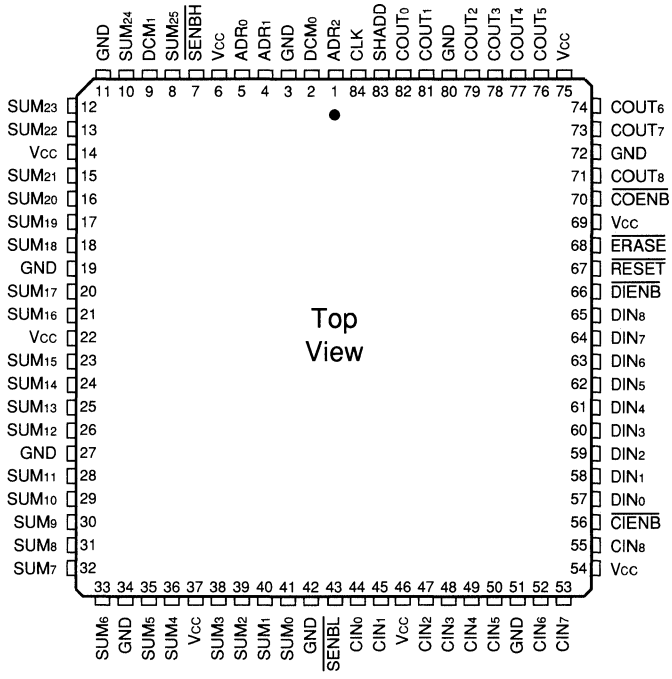


FIGURE 5. THRESHOLD LEVELS



ORDERING INFORMATION

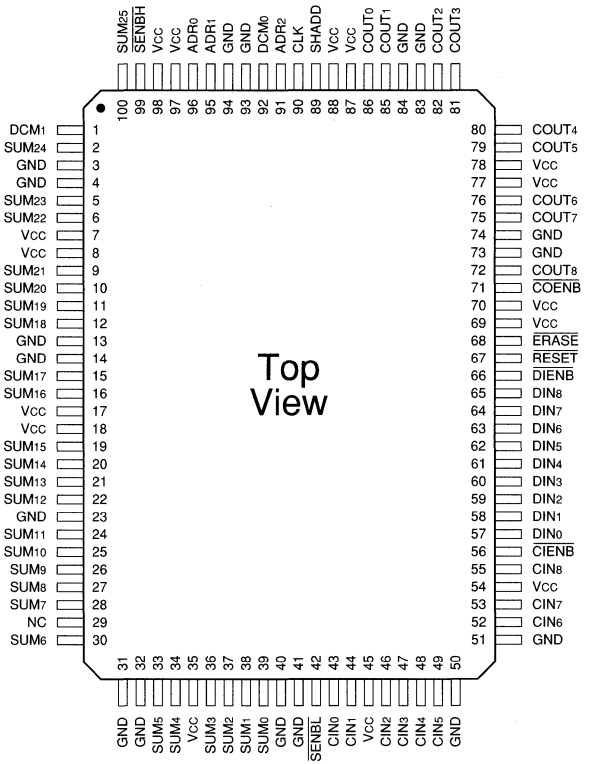
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43891JC50
40 ns	LF43891JC40
33 ns	LF43891JC33

ORDERING INFORMATION

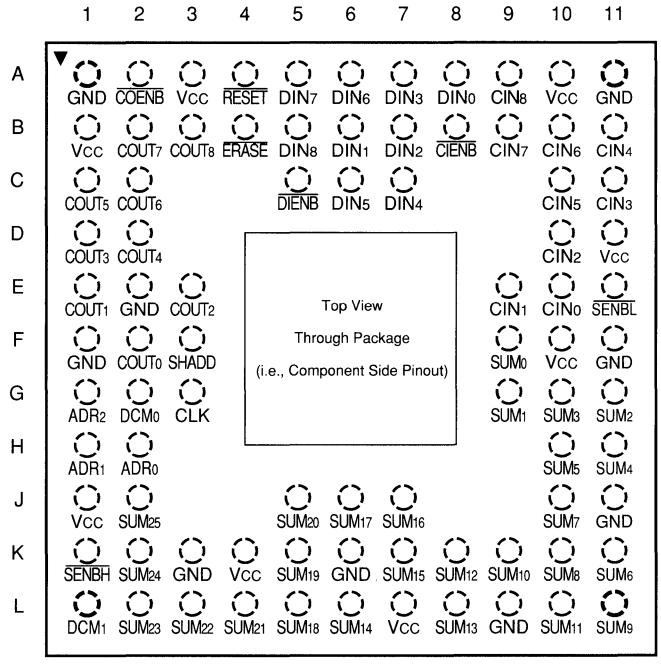
100-pin



Speed	Plastic Quad Flatpack (Q2)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43891QC50
40 ns	LF43891QC40
33 ns	LF43891QC33

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — COMMERCIAL SCREENING
50 ns	LF43891GC50
40 ns	LF43891GC40
33 ns	LF43891GC33
	–55°C to +125°C — COMMERCIAL SCREENING
50 ns	LF43891GM50
40 ns	LF43891GM40
	–55°C to +125°C — MIL-STD-883 COMPLIANT
50 ns	LF43891GMB50
40 ns	LF43891GMB40

Ordering Information 1
Video Imaging Products 2
Arithmetic Logic Units & Special Arithmetic Functions 3
Multipliers & Multiplier-Accumulators 4
Register Products 5
Peripheral Products 6
Quality and Reliability 7
Technology and Design Features 8
Package Information 9
Product Listing 10
Sales Offices 11

Arithmetic Logic Units & Special Arithmetic Functions

ARITHMETIC LOGIC UNITS & SPECIAL ARITHMETIC FUNCTIONS 3-1

Arithmetic Logic Units

L4C381 16-bit Cascadable ALU 3-3

L29C101 16-bit ALU Slice (Quad 2901) 3-15

Special Arithmetic Functions

LSH32 32-bit Cascadable Barrel Shifter 3-27

LSH33 32-bit Cascadable Barrel Shifter with Registers 3-37

L10C23 64 x 1 Digital Correlator 3-45

FEATURES

- High-Speed (15ns), Low Power 16-bit Cascadable ALU
- Implements Add, Subtract, Accumulate, Two's Complement, Pass, and Logic Operations
- All Registers Have a Bypass Path for Complete Flexibility
- DESC SMD No. 5962-89959
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC
  - 68-pin Commercial PGA
  - 68-pin Ceramic PGA

DESCRIPTION

The **L4C381** is a flexible, high speed, cascadable 16-bit Arithmetic and Logic Unit. It combines four 381-type 4-bit ALUs, a look-ahead carry generator, and miscellaneous interface logic — all in a single 68-pin package. While containing new features to support high speed pipelined architectures and single 16-bit bus configurations, the L4C381 retains full performance and functional compatibility with the bipolar '381 designs.

The L4C381 can be cascaded to perform 32-bit or greater operations. See "Cascading the L4C381" toward the end of this data sheet for more information.

ARCHITECTURE

The L4C381 operates on two 16-bit operands (A and B) and produces a 16-bit result (F). Three select lines control the ALU and provide 3 arithmetic, 3 logical, and 2 initialization functions. Full ALU status is provided to support cascading to longer word lengths. Registers are provided on both the ALU inputs and the output, but these may be bypassed under user control. An internal feedback path allows the registered ALU output to be routed to one of the ALU inputs, accommodating chain operations and accumulation. Furthermore, the A or B input can be forced to Zero allowing unary functions on either operand.

ALU OPERATIONS

The S_2–S_0 lines specify the operation to be performed. The ALU functions and their select codes are shown in Table 1.

The two functions, B minus A and A minus B, can be achieved by setting the carry input of the least significant slice and selecting codes 001 and 010 respectively.

L4C381 BLOCK DIAGRAM

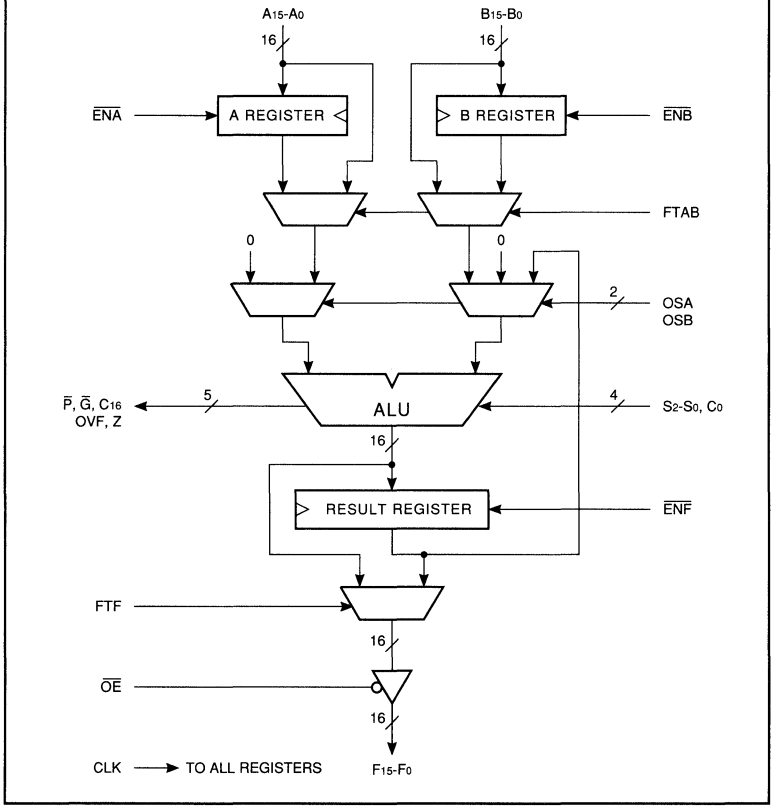


TABLE 1. ALU FUNCTIONS

S_2-S_0	FUNCTION
000	CLEAR (F = 00 ••• 00)
001	NOT(A) + B
010	A + NOT(B)
011	A + B
100	A XOR B
101	A OR B
110	A AND B
111	PRESET (F = 11 ••• 11)

ALU STATUS

The ALU provides Overflow and Zero status bits. Carry, Propagate, and Generate outputs are also provided for cascading. These outputs are defined for the three arithmetic functions only. The ALU sets the Zero output when all 16 output bits are zero. The Generate, Propagate, C_{16}, and OVF flags for the A + B operation are defined in Table 2. The status flags produced for NOT(A) + B and A + NOT(B) can be found by complementing A_i and B_i respectively in Table 2.

TABLE 2. ALU STATUS FLAGS

Bit Carry Generate $= g_i = A_iB_i$	for i = 0 ... 15
Bit Carry Propagate $= p_i = A_i + B_i$	for i = 0 ... 15
$P_0 = p_0$	
$P_i = p_i (P_{i-1})$	for i = 1 ... 15
and	
$G_0 = g_0$	
$G_i = g_i + p_i (G_{i-1})$	for i = 1 ... 15
$C_i = G_{i-1} + P_{i-1} (C_0)$	for i = 1 ... 15
then	
$\bar{G} = \text{NOT}(G_{15})$	
$\bar{P} = \text{NOT}(P_{15})$	
$C_{16} = G_{15} + P_{15}C_0$	
$\text{OVF} = C_{15} \text{ XOR } C_{16}$	

OPERAND REGISTERS

The L4C381 has two 16-bit wide input registers for operands A and B. These registers are rising edge triggered by a common clock. The A register is enabled for input by setting the $\overline{\text{ENA}}$ control LOW, and the B register is enabled for input by setting the $\overline{\text{ENB}}$ control LOW. When either the $\overline{\text{ENA}}$ control or $\overline{\text{ENB}}$ control is HIGH, the data in the corresponding input register will not change.

This architecture allows the L4C381 to accept arguments from a single 16-bit data bus. For those applications that do not require registered inputs, both the A and B operand registers can be bypassed with the FTAB control line. When the FTAB control is asserted (FTAB = HIGH), data is routed around the A and B input registers; however, they continue to function normally via the $\overline{\text{ENA}}$ and $\overline{\text{ENB}}$ controls. The contents of the input registers will again be available to the ALU if the FTAB control is released.

OUTPUT REGISTER

The output of the ALU drives the input of a 16-bit register. This rising-edge-triggered register is clocked by the same clock as the input registers. When the $\overline{\text{ENF}}$ control is LOW, data from the ALU will be clocked into the output register. By disabling the output register, intermediate results can be held while loading new input operands. Three-state drivers controlled by the $\overline{\text{OE}}$ input allow the L4C381 to be configured in a single bidirectional bus system.

The output register can be bypassed by asserting the FTF control signal (FTF = HIGH). When the FTF control is asserted, output data is routed around the output register, however, it continues to function normally via the $\overline{\text{ENF}}$ control. The contents of the output register will again be available on the output pins if FTF is released. With both FTAB and FTF true (HIGH) the L4C381 is functionally identical to four cascaded 54S381-type devices.

OPERAND SELECTION

The two operand select lines, OSA and OSB, control multiplexers that precede the ALU inputs. These multiplexers provide an operand force-to-zero function as well as F register feedback to the B input. Table 3 shows the inputs to the ALU as a function of the operand select inputs. Either the A or B operands may be forced to zero.

TABLE 3. OPERAND SELECTION

OSB	OSA	OPERAND B	OPERAND A
0	0	F	A
0	1	0	A
1	0	B	0
1	1	B	A

When both operand select lines are low, the L4C381 is configured as a chain calculation ALU. The registered ALU output is passed back to the B input to the ALU. This allows accumulation operations to be performed by providing new operands via the A input port. The accumulator can be preloaded from the A input by setting OSA true. By forcing the function select lines to the CLEAR state (000), the accumulator may be cleared. Note that this feedback operation is not affected by the state of the FTF control. That is, the F outputs of the L4C381 may be driven directly by the ALU. The output register continues to function, however, and provides the ALU B operand source.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

3

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		15	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

From Input \ To Output	L4C381-55				L4C381-40				L4C381-26			
	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}
FTAB = 0, FTF = 0												
Clock	32	38	53	36	26	30	44	32	22	22	26	22
C_0	—	—	34	22	—	—	28	20	—	—	18	18
S_2-S_0, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 0, FTF = 1												
Clock	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_2-S_0, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22
FTAB = 1, FTF = 0												
A_{15}-A_0, B_{15}-B_0	—	36	46	37	—	30	40	32	—	22	22	22
Clock	32	—	—	—	26	—	—	—	22	—	—	—
C_0	—	—	34	22	—	—	28	20	—	—	18	18
S_2-S_0, OSA, OSB	—	42	42	42	—	32	34	35	—	22	22	22
FTAB = 1, FTF = 1												
A_{15}-A_0, B_{15}-B_0	55	36	46	37	40	30	40	32	26	22	22	22
Clock (OSA, OSB = 0)	56	38	53	36	46	30	44	32	28	22	26	22
C_0	37	—	34	22	30	—	28	20	22	—	18	18
S_2-S_0, OSA, OSB	55	42	42	42	40	32	34	35	26	22	22	22

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C381-55				L4C381-40				L4C381-26			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{15}-A_0, B_{15}-B_0	8	2	35	2	8	2	28	2	8	2	16	2
C_0	21	0	21	0	16	0	16	0	8	0	8	0
S_2-S_0, OSA, OSB	44	0	44	0	32	0	32	0	18	0	18	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	10	2	10	2	10	2	10	2	8	2	8	2

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C381-55	L4C381-40	L4C381-26
t_{ENA}	20	18	16
t_{DIS}	20	18	16

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C381-55	L4C381-40	L4C381-26
Minimum Cycle Time	43	34	20
Highgoing Pulse	15	10	10
Lowgoing Pulse	15	10	10

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

From Input \ To Output	L4C381-20				L4C381-15			
	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}
FTAB = 0, FTF = 0								
Clock	11	20	20	20	11	15	15	15
C_0	—	—	14	14	—	—	13	13
S_2-S_0, OSA, OSB	—	18	20	18	—	14	15	14
FTAB = 0, FTF = 1								
Clock	20	20	20	20	15	15	15	15
C_0	18	—	14	14	14	—	13	13
S_2-S_0, OSA, OSB	20	18	20	18	15	14	15	14
FTAB = 1, FTF = 0								
A_{15}-A_0, B_{15}-B_0	—	16	20	17	—	14	15	14
Clock	11	—	—	—	11	—	—	—
C_0	—	—	14	14	—	—	13	13
S_2-S_0, OSA, OSB	—	18	20	18	—	14	15	14
FTAB = 1, FTF = 1								
A_{15}-A_0, B_{15}-B_0	20	16	20	17	15	14	15	14
Clock (OSA, OSB = 0)	20	20	20	20	15	15	15	15
C_0	18	—	14	14	14	—	13	13
S_2-S_0, OSA, OSB	20	18	20	18	15	14	15	14

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C381-20				L4C381-15			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{15}-A_0, B_{15}-B_0	5	0	14	0	5	0	12	0
C_0	12	0	12	0	10	0	10	0
S_2-S_0, OSA, OSB	15	0	15	0	12	0	12	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	5	0	5	0	5	0	5	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C381-20	L4C381-15	
t_{ENA}	8	6	
t_{DIS}	8	6	

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C381-20	L4C381-15	
Minimum Cycle Time	18	14	
Highgoing Pulse	5	4	
Lowgoing Pulse	5	4	

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

From Input \ To Output	L4C381-65				L4C381-45				L4C381-30			
	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}
FTAB = 0, FTF = 0												
Clock	37	44	63	45	28	34	50	34	26	28	34	28
C_0	—	—	42	25	—	—	32	23	—	—	22	22
S_2-S_0, OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 0, FTF = 1												
Clock	68	44	63	45	56	34	50	34	34	28	34	28
C_0	42	—	42	25	32	—	32	23	26	—	22	22
S_2-S_0, OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28
FTAB = 1, FTF = 0												
A_{15}-A_0, B_{15}-B_0	—	44	56	44	—	32	46	36	—	28	28	28
Clock	37	—	—	—	28	—	—	—	26	—	—	—
C_0	—	—	42	25	—	—	32	23	—	—	22	22
S_2-S_0, OSA, OSB	—	48	48	48	—	38	38	38	—	28	28	28
FTAB = 1, FTF = 1												
A_{15}-A_0, B_{15}-B_0	65	44	56	44	45	32	46	36	30	28	28	28
Clock (OSA, OSB = 0)	68	44	63	45	56	34	50	34	34	28	34	28
C_0	42	—	42	25	32	—	32	23	26	—	22	22
S_2-S_0, OSA, OSB	66	48	48	48	46	38	38	38	30	28	28	28

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C381-65				L4C381-45				L4C381-30			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{15}-A_0, B_{15}-B_0	10	3	43	3	8	3	33	3	8	3	20	3
C_0	25	0	25	0	20	0	20	0	12	0	12	0
S_2-S_0, OSA, OSB	50	0	50	0	36	0	36	0	20	0	20	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	12	2	12	2	10	2	10	2	10	2	10	2

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C381-65	L4C381-45	L4C381-30
t_{ENA}	22	20	18
t_{DIS}	22	20	18

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C381-65	L4C381-45	L4C381-30
Minimum Cycle Time	52	38	26
Highgoing Pulse	20	15	12
Lowgoing Pulse	20	15	12

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

From Input \ To Output	L4C381-25				L4C381-20			
	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}	F_{15}-F_0	$\overline{P}$, $\overline{G}$	OVF, Z	C_{16}
FTAB = 0, FTF = 0								
Clock	14	24	24	24	14	20	20	20
C_0	—	—	18	18	—	—	16	16
S_2-S_0, OSA, OSB	—	22	24	22	—	18	20	18
FTAB = 0, FTF = 1								
Clock	25	24	24	24	20	20	20	20
C_0	21	—	18	18	17	—	16	16
S_2-S_0, OSA, OSB	25	22	24	22	20	18	20	18
FTAB = 1, FTF = 0								
A_{15}-A_0, B_{15}-B_0	—	20	25	22	—	17	20	17
Clock	14	—	—	—	14	—	—	—
C_0	—	—	18	18	—	—	16	16
S_2-S_0, OSA, OSB	—	22	24	22	—	18	20	18
FTAB = 1, FTF = 1								
A_{15}-A_0, B_{15}-B_0	25	20	25	22	20	17	20	17
Clock (OSA, OSB = 0)	25	24	24	24	20	20	20	20
C_0	21	—	18	18	17	—	16	16
S_2-S_0, OSA, OSB	25	22	24	22	20	18	20	18

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	L4C381-25				L4C381-20			
	FTAB = 0		FTAB = 1		FTAB = 0		FTAB = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
A_{15}-A_0, B_{15}-B_0	7	0	14	0	6	0	12	0
C_0	14	0	14	0	12	0	12	0
S_2-S_0, OSA, OSB	19	0	19	0	16	0	16	0
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	7	0	7	0	6	0	6	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	L4C381-25	L4C381-20
t_{ENA}	14	10
t_{DIS}	14	10

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	L4C381-25	L4C381-20
Minimum Cycle Time	20	18
Highgoing Pulse	8	6
Lowgoing Pulse	8	6

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 1. INPUT CIRCUIT

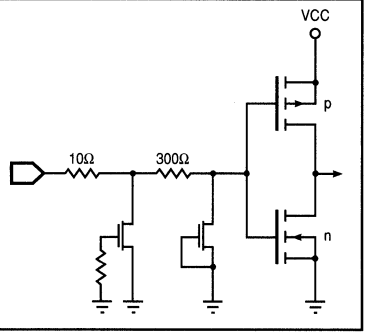


FIGURE 2. OUTPUT CIRCUIT

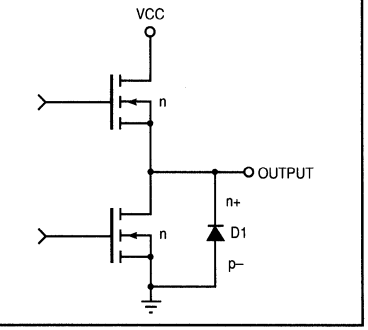
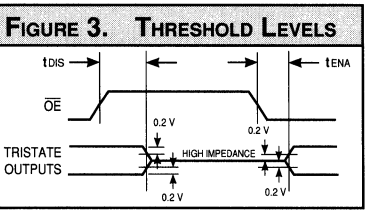


FIGURE 3. THRESHOLD LEVELS



CASCADING THE L4C381

Cascading the L4C381 to 32 bits is accomplished simply by connecting the C_{16} output of the least significant slice to the C_0 input of the most significant slice. The S_2-S_0, OSA, OSB, $\overline{ENA}$, $\overline{ENB}$, and $\overline{ENF}$ lines are common to both devices. The Zero output flags should be logically ANDed to produce the Zero flag for the 32-bit result. The OVF and C_{16} outputs of the most significant slice are valid for the 32-bit result.

Propagation delay calculations for this configuration require two steps: First determine the propagation delay from the input of interest to the C_{16} output of the lower slice. Add this number to the delay from the C_0 input of the upper slice to the output of interest (of the C_0 setup time, if the F register is used). The sum gives the overall input-to-output delay (or setup time) for the 32-bit configuration. This method gives a conservative result, since the C_{16} output is very lightly loaded. Formulas for calculation of all critical delays for a 32-bit system are shown in Figures 4A through 4D.

Cascading to greater than 32 bits can be accomplished in two ways: The simplest (but slowest) method is to simply connect the C_{16} output of each slice to the C_0 input of the next more significant slice. Propagation delays are calculated as for the 32-bit case, except that the C_0 to C_{16} delays for all intermediate slices must be added to the overall delay for each path. A faster method is to use an external carry-lookahead generator. The $\overline{P}$ and $\overline{G}$ outputs of each slice are connected as inputs to the CLA generator, which in turn produces the C_0 inputs for each slice except the least significant. The C_{16} outputs are not used in this case, except for the most significant one, which is the carry out of the overall system. The carry in to the system is connected to the C_0 input of the least significant slice, and also to the carry lookahead generator. Propagation delays for this configuration are the sum of the time to $\overline{P}$, $\overline{G}$, for the least significant slice, the propagation delay of the carry lookahead generator, and the C_0 to output time of the most significant slice.

3

FIGURE 4A. FTAB = 0, FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
Clock	→ Other	=	(Clock → C_{16}) + (C_0 → Out)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_2-S_0, OSA, OSB	→ Other	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 → Out)
A, B	Setup time	=	Same as 16-bit case
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
S_2-S_0, OSA, OSB	Setup time	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C_{16}) + (C_0 Setup time)

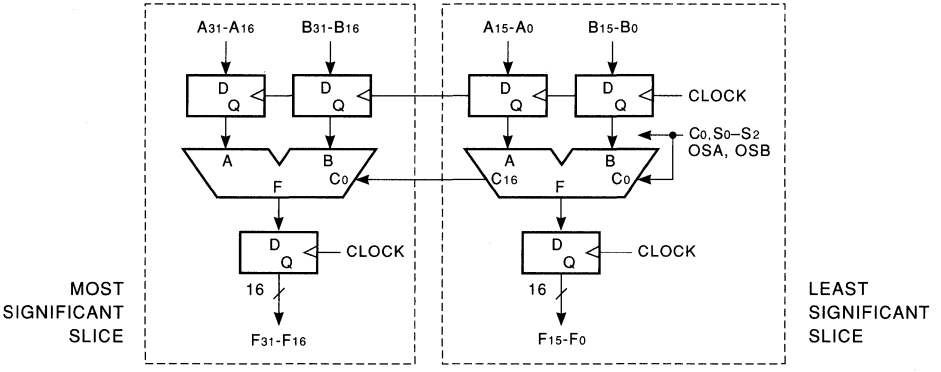


FIGURE 4B. FTAB = 0, FTF = 1

From	To		Calculated Specification Limit
Clock	→ F	=	(Clock → C_{16}) + (C_0 → F)
Clock	→ Other	=	(Clock → C_{16}) + (C_0 → Out)
C_0	→ F	=	(C_0 → C_{16}) + (C_0 → F)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_2-S_0, OSA, OSB	→ F	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 → F)
S_2-S_0, OSA, OSB	→ Other	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 → Out)
A, B	Setup time	=	Same as 16-bit case
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
S_2-S_0, OSA, OSB	Setup time	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time		=	(Clock → C_{16}) + (C_0 Setup time)

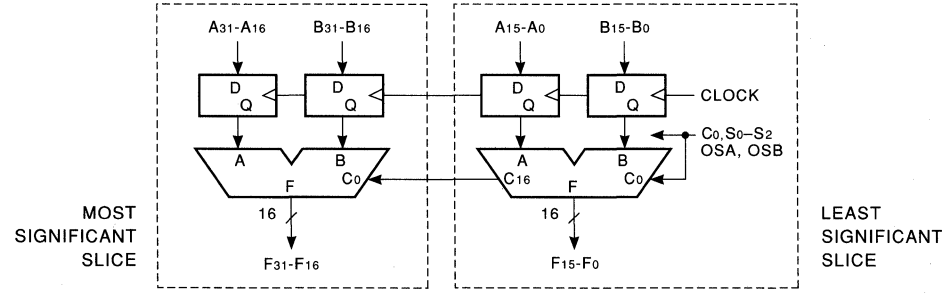


FIGURE 4C. FTAB = 1, FTF = 0

From	To		Calculated Specification Limit
Clock	→ F	=	Same as 16-bit case
A, B	→ Other	=	(A, B → C_{16}) + (C_0 → Out)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_2-S_0, OSA, OSB	→ Other	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 → Out)
A, B	Setup time	=	(A, B → C_{16}) + (C_0 Setup time)
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
S_2-S_0, OSA, OSB	Setup time	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C_{16}) + (C_0 Setup time)

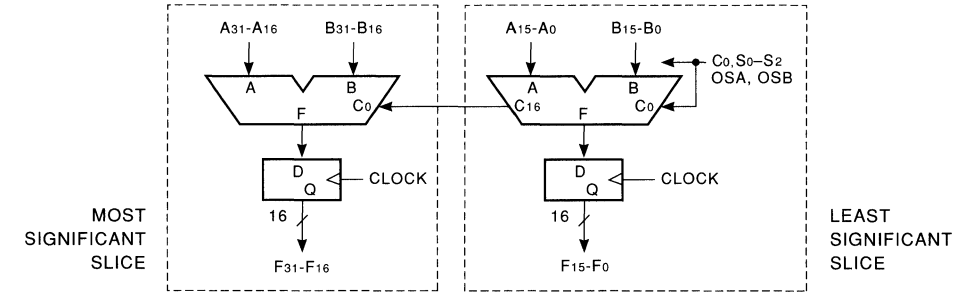
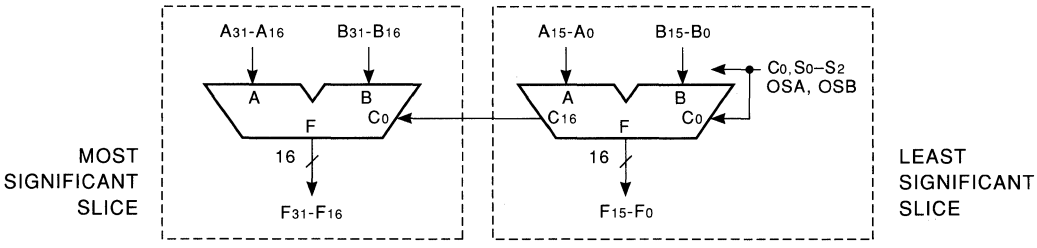


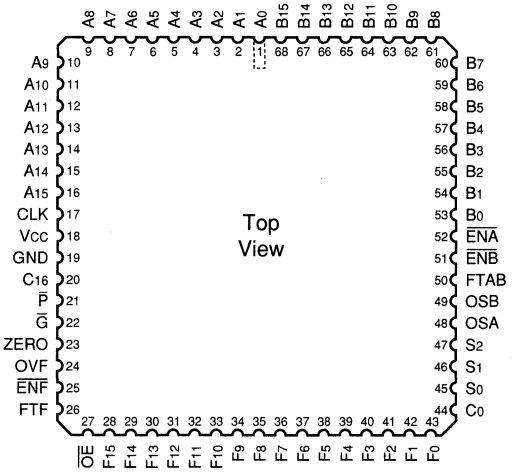
FIGURE 4D. FTAB = 1, FTF = 1

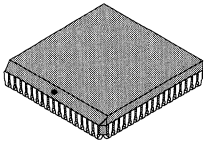
From	To		Calculated Specification Limit
A, B	→ F	=	(A, B → C_{16}) + (C_0 → F)
A, B	→ Other	=	(A, B → C_{16}) + (C_0 → Out)
C_0	→ F	=	(C_0 → C_{16}) + (C_0 → F)
C_0	→ Other	=	(C_0 → C_{16}) + (C_0 → Out)
S_2-S_0, OSA, OSB	→ F	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 → F)
S_2-S_0, OSA, OSB	→ Other	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 → Out)
A, B	Setup time	=	(A, B → C_{16}) + (C_0 Setup time)
C_0	Setup time	=	(C_0 → C_{16}) + (C_0 Setup time)
S_2-S_0, OSA, OSB	Setup time	=	(S_2-S_0, OSA, OSB → C_{16}) + (C_0 Setup time)
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	Setup time	=	Same as 16-bit case
Minimum cycle time (F register accumulate loop)		=	(Clock → C_{16}) + (C_0 Setup time)

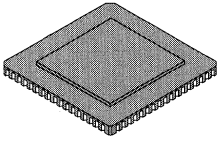


ORDERING INFORMATION

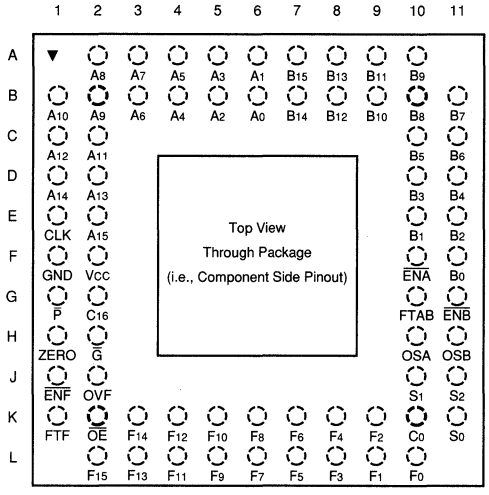
68-pin

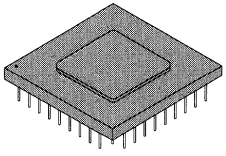


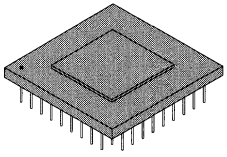




68-pin







Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Commercial Pin Grid Array (E1)	Ceramic Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening			
55 ns	L4C381JC55	L4C381KC55	L4C381EC55	L4C381GC55
40 ns	L4C381JC40	L4C381KC40	L4C381EC40	L4C381GC40
26 ns	L4C381JC26	L4C381KC26	L4C381EC26	L4C381GC26
20 ns	L4C381JC20	L4C381KC20	L4C381EC20	L4C381GC20
15 ns	L4C381JC15	L4C381KC15	L4C381EC15	L4C381GC15
	–55°C to +125°C — Commercial Screening			
65 ns		L4C381KM65		L4C381GM65
45 ns		L4C381KM45		L4C381GM45
30 ns		L4C381KM30		L4C381GM30
25 ns		L4C381KM25		L4C381GM25
20 ns		L4C381KM20		L4C381GM20
	–55°C to +125°C — MIL-STD-883 Compliant			
65 ns		L4C381KMB65		L4C381GMB65
45 ns		L4C381KMB45		L4C381GMB45
30 ns		L4C381KMB30		L4C381GMB30
25 ns		L4C381KMB25		L4C381GMB25
20 ns		L4C381KMB20		L4C381GMB20

L29C101
16-bit ALU Slice

FEATURES

- Four-Wide 2901 ALUs Plus Carry Look-Ahead Logic and Full 16-bit Data Paths
- High Speed, Low Power CMOS Technology
- Fast Clock Period: 35 ns Commercial, 45 ns Military
- DESC SMD No. 5962-89517
- Available 100% Screened to MIL-STD-883, Class B
- Pin and Functionally Equivalent to AMD Am29C101 and Cypress CY7C9101
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Ceramic Pin Grid Array

DESCRIPTION

The **L29C101** is a high-performance, expandable, 16-bit Arithmetic Logic Unit slice manufactured using CMOS technology. Completely code compatible with its 4-bit predecessors, the part can be used to implement the arithmetic section of central processors or many types of programmable controllers.

The microinstruction set of the L29C101 is straightforward, yet versatile enough so that the part can be used to emulate the ALU operations of most digital computers.

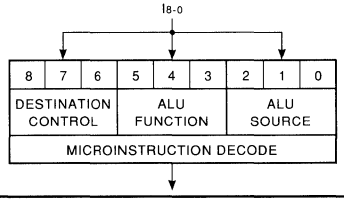
The L29C101 is comprised of functions equivalent to four 2901 bit-slice ALUs plus the 2902 carry look-ahead logic, all in a single 64-pin device.

Included are a 16-word by 16-bit dual-port register file, a 16-bit 8-function ALU, 16-bit shifters, and all the necessary decoding and control logic.

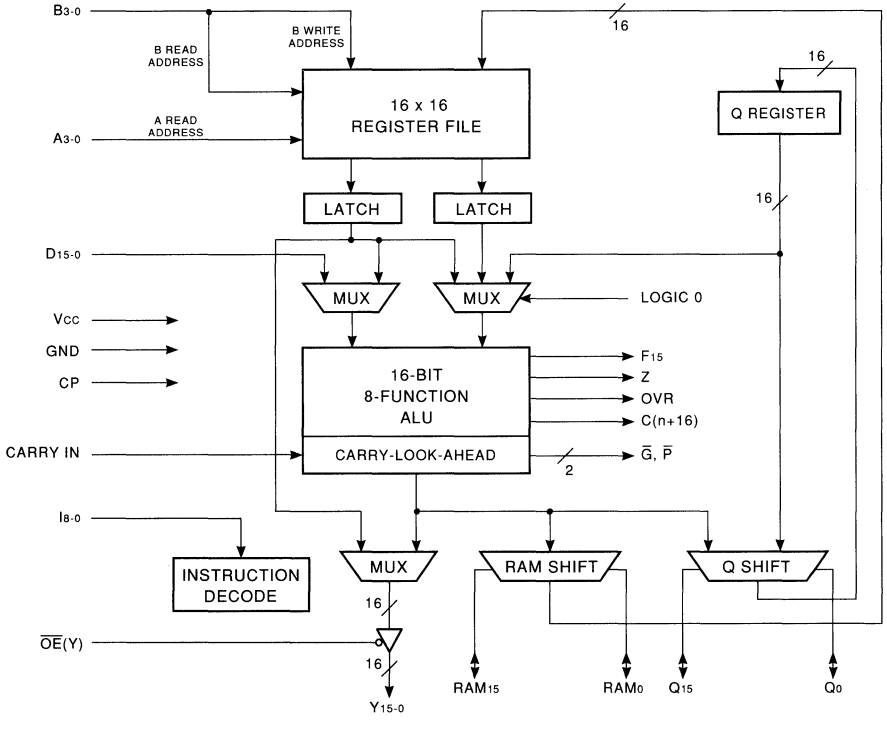
All status, shift linkage, and carry functions are cascadable to allow construction of architectures wider than 16-bits if desired. Expanded

3

L29C101 Instruction Decoding



L29C101 Block Diagram



designs can take advantage of full carry-look-ahead for improved performance.

The L29C101 is fully pin and function compatible with the Am29C101. The L29C101 is available in High-Rel versions that are fully compliant with MIL-STD-883, Class B.

L29C101 ARCHITECTURE

A typical execution cycle for the L29C101 consists of reading two operands simultaneously from the two-port register file, performing an ALU operation on these operands, and returning the result to the register file. This entire operation can be completed in a single clock cycle, providing high performance and simple microcode. Optionally, the ALU operands may be sourced by the external data port, an auxiliary register denoted the Quotient or "Q" register, or forced to zero under instruction control. Also, the data returned to the register file and the Q register may be shifted one bit in either direction to aid multiplication and division operations.

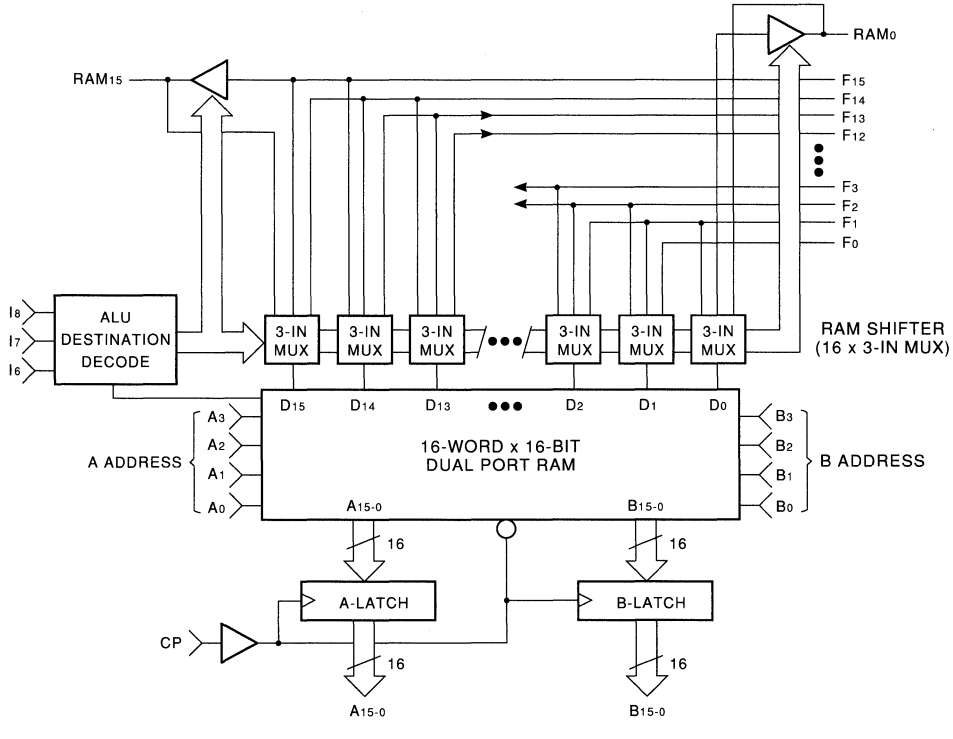
REGISTER FILE

The two-port register file has a capacity of 16 words of 16 bits each. The A-port address, A_{3-0}, specifies the register to be read from the A-port, and the B-port address, B_{3-0}, specifies the register to the read from the B-port. Both A and B addresses may be the same, in which case identical data will appear at both A and B ports. In addition, the B-port address can specify a register location for writing. Data from the locations indicated by the A and B addresses are read from the register file during the low period of the clock. The data is applied to two latches which are transparent during the clock low period, and hold their state during the clock high period. The purpose of these latches is to hold the A and B ALU operands constant while a computation result is written back to the register file at the B address. This allows for a read-modify-write cycle, which is useful in applications such as accumulation. Under control of the Result Destination Field (I_{8-6}), data to be written to the register file is stored into the register addressed by the B field on the rising edge of the clock.

ALU CONTROL

The ALU is capable of performing eight operations. These functions are described in Table 2. The control inputs, I_{5-3}, select one of three arith-

FIGURE 1. REGISTER FILE



metic or five logical operations to be performed on the input operands. The integral carry-look-ahead circuitry across all 16 ALU bits is functionally equivalent to the 2902 carry-look-ahead unit and provides significant speed advantages.

In the arithmetic mode, the ALU result is also a function of the Carry-In input. When executing ALU Add or Subtract instructions, setting the C(n) input to '1' causes the addition of '1' to the result. Thus for two's complement operations, C(n) of the least significant slice would be set to zero for addition, and to '1' for subtraction. This is because the L29C101 ALU naturally implements one's complement subtraction, that is, a bitwise complement of one of the operands. In order to achieve a two's complement result, a '1' must be added in the least significant position. This is accomplished by using C(n). PASS and Negate operations are also available by combining arithmetic instructions (Add, Subtract) with any of the operand source options which set one operand to zero. Tables 5 and 6 show the detailed ALU logic and arithmetic functions and the operands selected. Table 5 includes ALU function selection.

OPERAND SOURCE CONTROL

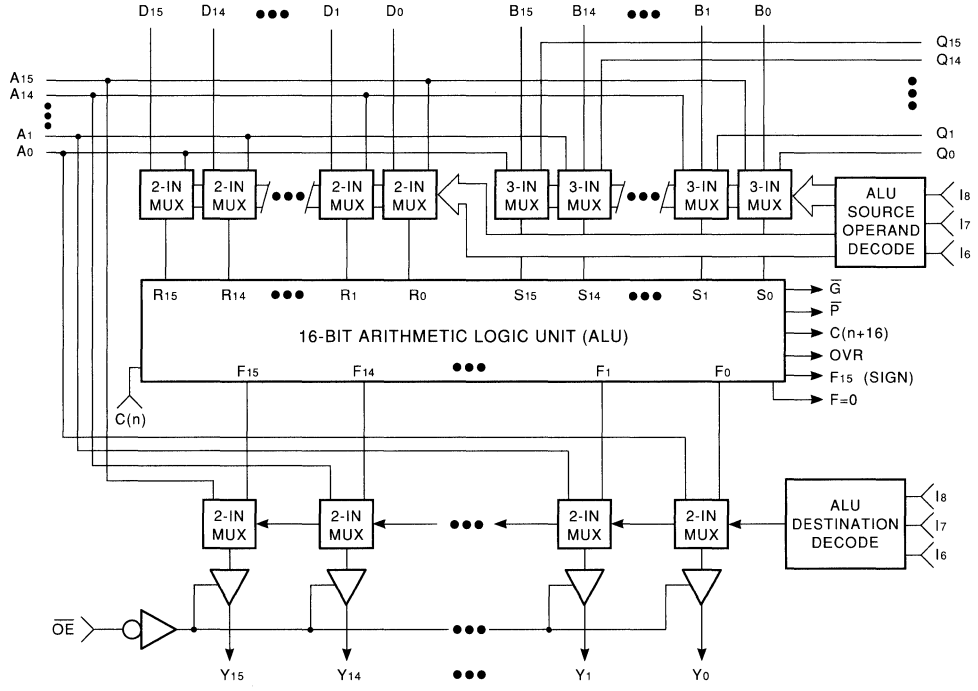
As shown in the figure below, each of the ALU operands is supplied by a multiplexer, which allows significant flexibility in the selection of the operand source. The two 16-bit ALU inputs are denoted R and S. The R operand may be sourced by the A read port of the register file, from the D input pins, or may be forced to zero. The S operand may be sourced by the B read port of the register file, the A read port (when the R operand is D or zero), the Q register, or forced to zero. Control of the operand selection multiplexers is encoded into control field I_{2-0}, as described in Table 1.

RESULT DESTINATION CONTROL

The instruction field, I_{8-6}, is encoded to control the routing of the ALU result field, denoted F, and the Q register contents. The encoding is defined in Table 3. Under instruction control, the ALU result can be stored in the register file, the Q register, or both. A No Operation capability is also provided during which the result is not stored in either location. This field also controls the value presented at the Y_{15-0} outputs. These outputs generally reflect the ALU result F, but for one of the instruction decodes, the outputs are

3

FIGURE 2. ALU



driven by the A port value read from the register file. This provides the capability to read data from the register file while simultaneously performing an ALU operation. This is useful in applications such as postincrement address generation.

In addition to destination control, up or down shifting of both the register file and Q register load values are controlled by the I8-6 field. Each can be up or down shifted one position prior to storing in the destination register. The RAM0 or Q0 pins output the least significant bit of the value being stored for downshifts, and accept the bit to be stored in the least signficant position for upshifts. Similarly, the RAM15 or Q15 pins output the most significant bit for upshifts, and accept the bit to be stored in the most significant position for downshifts. Table 3 gives the various shift actions and data destinations controlled by the I8-6 inputs.

Q REGISTER

The Q register is intended primarily for use as a separate working register for multiplication and division routines but it also serves as an accumulator or for temporary storage. The Q register is loaded via a multiplexer, which allows either up or downshift of the Q register contents, or an unshifted load of the Q register with the ALU result.

STATUS OUTPUTS

The $\overline{G}$ and $\overline{P}$ outputs are low-true Carry-Generate and Carry-Propagate signals. They are used in conjunction with an external carry-look-ahead generator when cascading L29C101 slices beyond 32 bits. The C(n+16) is the Carry-Out signal, which can be directly connected to the C(n) input of another L29C101 to implement a 32-bit system. The OVR output indicates two's complement overflow for addition and subtraction. The logical definitions of the $\overline{G}$, $\overline{P}$, C(n+16), and OVR signals are given in Table 7.

The MSB of the ALU result (F15) is provided so that the sign bit may be examined easily. The Z output is used for zero detection and is high when all of the F output bits are low. It is an open drain output which may be wire OR'ed across multiple slices.

FIGURE 3. Q REGISTER

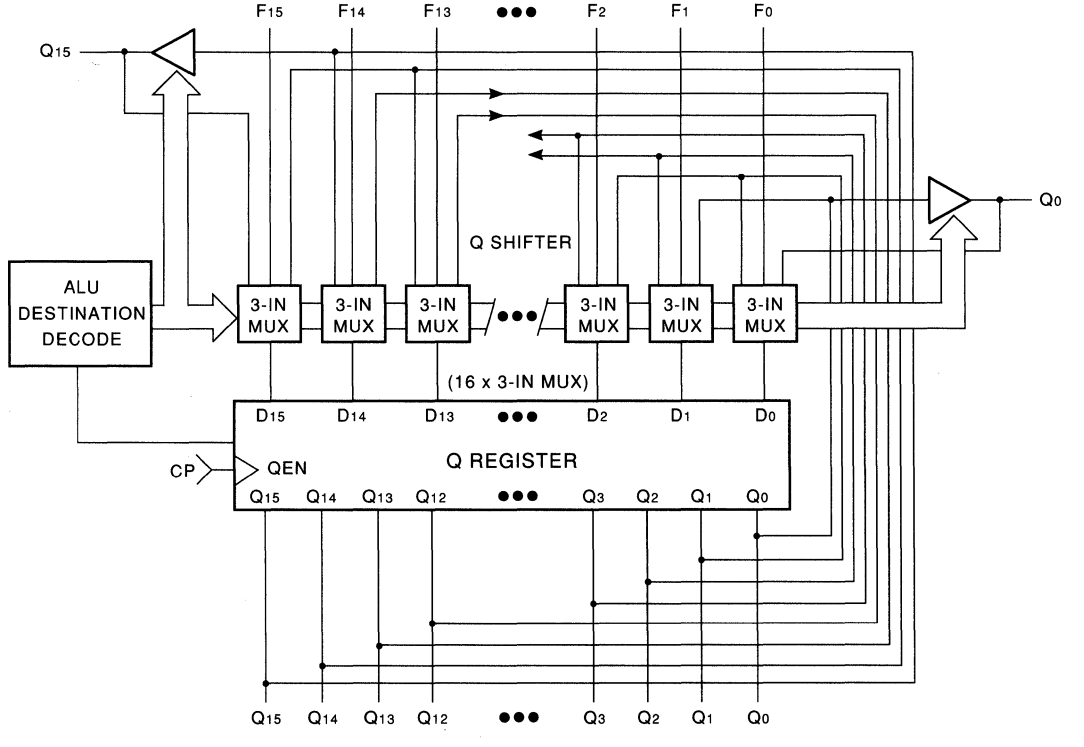


TABLE 1. ALU SOURCE OPERAND CONTROL

Mnemonic	Micro Code I_2	I_1	I_0	Octal Code	ALU Source Operands R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	O	Q
ZB	L	H	H	3	O	B
ZA	H	L	L	4	O	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	O

TABLE 2. ALU FUNCTION CONTROL

Mnemonic	Micro Code I_5	I_4	I_3	Octal Code	ALU Function	Symbol
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S – R
SUBS	L	H	L	2	R Minus S	R – S
OR	L	H	H	3	R OR S	
AND	H	L	L	4	R AND S	
NOTRS	H	L	H	5	$\overline{R}$ AND S	
EXOR	H	H	L	6	R EX-OR S	
EXNOR	H	H	H	7	R EX-NOR S	

TABLE 3. ALU DESTINATION CONTROL

Mnemonic	Micro Code I_8	I_7	I_6	Octal Code	RAM Function Shift	Load	Q-Reg. Function Shift	Load	Y Output	RAM Shifter RAM_0	RAM_{15}	Q Shifter Q_0	Q_{15}
QREG	L	L	L	0	X	None	None	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	None	X	None	F	X	X	X	X
RAMA	L	H	L	2	None	F → B	X	None	A	X	X	X	X
RAMF	L	H	H	3	None	F → B	X	None	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2 → B	X	None	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F → B	X	None	F	IN_0	F_{15}	X	Q_{15}

TABLE 4. SOURCE OPERAND AND ALU FUNCTION MATRIX

Octal I_{5-3}	I_{2-0} → ALU Function	0 A, Q	1 A, B	2 O, Q	3 O, B	4 O, A	5 D, A	6 D, Q	7 D, O
		ALU Source							
0	C(n) = L R plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	C(n) = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	C(n) = L S minus R	Q – A – 1	B – A – 1	Q – 1	B – 1	A – 1	A – D – 1	Q – D – 1	– D – 1
	C(n) = H	Q – A	B – A	Q	B	A	A – D	Q – D	– D
2	C(n) = L R minus S	A – Q – 1	A – B – 1	– Q – 1	– B – 1	– A – 1	D – A – 1	D – Q – 1	D – 1
	C(n) = H	A – Q	A – B	– Q	– B	– A	D – A	D – Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	$\overline{A}$ ∧ Q	0	0	0	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	A ∧ B	Q	B	A	D ∧ A	D ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

Table 5. ALU Logic Mode Functions

Octal I_{5-3}, I_{2-0}	Group	Function
40	AND	$A \wedge Q$
41		$A \wedge B$
45		$D \wedge A$
46		$D \wedge Q$
30	OR	$A \vee Q$
31		$A \vee B$
35		$D \vee A$
36		$D \vee A$
60	EX – OR	$A \forall Q$
61		$A \forall B$
65		$D \forall A$
66		$D \forall Q$
70	EX – NOR	$\overline{A \forall Q}$
71		$\overline{A \forall B}$
75		$\overline{D \forall A}$
76		$\overline{D \forall Q}$
72	INVERT	$\overline{Q}$
73		$\overline{R}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	ZERO	0
43		0
44		0
47		0
50	MASK	$\overline{A} \wedge Q$
51		$\overline{A} \wedge B$
55		$\overline{D} \wedge A$
56		$\overline{D} \wedge Q$

Table 6. ALU Arithmetic Mode Functions

Octal I_{5-3}, I_{2-0}	C(n) = 0 (Low)		C(n) = 1 (High)	
	Group	Function	Group	Function
00	ADD	A + Q	ADD Plus One	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q – 1	PASS	Q
13		B – 1		B
14		A – 1		A
27		D – 1		D
22	1's Comp.	– Q –1	2's Comp. (Negate)	– Q
23		– B – 1		– B
24		– A – 1		– A
17		– D – 1		– D
10	Subtract (1's Comp.)	Q – A –1	Subtract (2's Comp.)	Q – A
11		B – A – 1		B – A
15		A – D – 1		A – D
16		Q – D – 1		Q – D
20		A – Q –1		A – Q
21		A – B – 1		A – B
25		D – A – 1		D – A
26		D – Q – 1		D – Q

Table 7. Logic Functions for Carry and Overflow Conditions

I_{5-3}	Function	P	G	C (n+16)	OVR
0	R + S	$\overline{P_0 \cdot P_1 \cdots P_{15}}$	$\overline{G_{15} + P_{15} G_{14} + P_{15} P_{14} G_{13} + \cdots}$	C_{16}	$C_{16} \forall C_{15}$
1	S – R	Same as R + S equations, but substitute $\overline{Ri}$ for Ri in definitions			
2	R – S	Same as R + S equations, but substitute $\overline{Si}$ for Si in definitions			
3	$R \vee S$	HIGH	HIGH	LOW	LOW
4	$R \wedge S$				
5	$R \wedge \overline{S}$				
6	$\overline{R} \forall S$				
7	$\overline{R \forall S}$				

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

3

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		15	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			5.0	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C) *Note 9 (ns)*

OUTPUT ENABLE/DISABLE TIMES *(Note 11)*

Device	Input	Output	tENA	tDIS
L29C101-35	$\overline{OE}$	Y	20	17

CYCLE TIME AND CLOCK CHARACTERISTICS

Read – Modify – Write Cycle (from selection of A, B registers to end of cycle)	35 ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	30 MHz
Minimum Clock LOW Time	15 ns
Minimum Clock HIGH Time	20 ns

COMBINATIONAL PROPAGATION DELAYS *(Note 13)*

From Input \ To Output	Y	F_{15}	C (n16)	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM_0 RAM_{15}	Q_0 Q_{15}
A,B Address	46	43	35	37	49	41	40	—
D	34	34	27	27	40	29	33	—
C(n)	27	24	20	—	28	23	28	—
I_0, I_1, I_2	40	40	33	30	42	32	35	—
I_3, I_4, I_5	41	38	32	28	40	36	38	—
I_6, I_7, I_8	20	—	—	—	—	—	26	26
A bypass ALU (I = 2XX)	26	—	—	—	—	—	—	—
Clock	38	34	30	30	36	32	34	25

SETUP AND HOLD TIMES RELATIVE TO CLOCK INPUT *(Note 13)*

Input	Setup Time Before H → L	Hold Time After H → L	Setup Time Before L → H	Hold Time After L → H
A,B Source Address (Notes 15, 16)	24	3	35	—
B Destination Address (Note 14)	24	Do Not Change		0
D	—	—	26	0
C(n)	—	—	16	0
I_0, I_1, I_2	—	—	30	0
I_3, I_4, I_5	—	—	31	0
I_6, I_7, I_8 (Note 14)	10	Do Not Change		0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	12	0

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (-55°C to +125°C) *Note 9 (ns)*

OUTPUT ENABLE/DISABLE TIMES *(Note 11)*

Device	Input	Output	tENA	tDIS
L29C101-45	$\overline{OE}$	Y	23	20

CYCLE TIME AND CLOCK CHARACTERISTICS

Read – Modify – Write Cycle (from selection of A, B registers to end of cycle)	45ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	25 MHz
Minimum Clock LOW Time	20 ns
Minimum Clock HIGH Time	20 ns

COMBINATIONAL PROPAGATION DELAYS *(Note 13)*

From Input \ To Output	Y	F_{15}	C (n16)	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM_0 RAM_{15}	Q_0 Q_{15}
A,B Address	52	50	40	38	48	46	43	—
D	37	36	30	32	40	32	35	—
C(n)	30	28	24	—	29	27	30	—
I_0, I_1, I_2	44	43	36	34	46	38	41	—
I_3, I_4, I_5	47	44	35	35	45	44	45	—
I_6, I_7, I_8	22	—	—	—	—	—	30	30
A bypass ALU (I = 2XX)	27	—	—	—	—	—	—	—
Clock	44	39	32	32	40	36	34	28

SETUP AND HOLD TIMES RELATIVE TO CLOCK INPUT *(Note 13)*

Input	Setup Time Before H → L	Hold Time After H → L	Setup Time Before L → H	Hold Time After L → H
A,B Source Address (Notes 15, 16)	22	3	40	—
B Destination Address (Note 14)	22	Do Not Change		0
D	—	—	30	0
C(n)	—	—	20	0
I_0, I_1, I_2	—	—	37	0
I_3, I_4, I_5	—	—	36	0
I_6, I_7, I_8 (Note 14)	10	Do Not Change		0
RAM_0, RAM_{15}, Q_0, Q_{15}	—	—	12	0

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

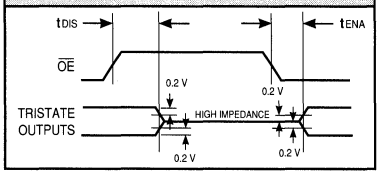
13. A dash indicates a propagation delay or setup time constraint that does not exist.

14. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change."

15. Source addresses must be stable prior to the clock H→L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.

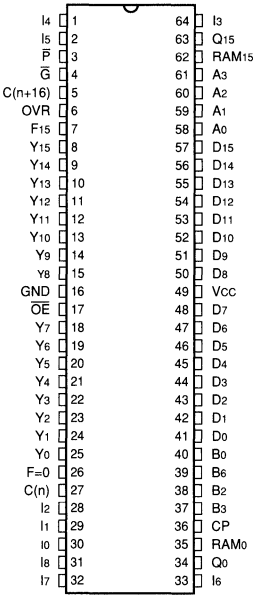
16. The setup time prior to the clock L→H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes all the time from stable A and B addresses to the clock L→H transition, regardless of when the clock H→L transition occurs.

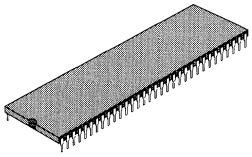
FIGURE 4. THRESHOLD LEVELS



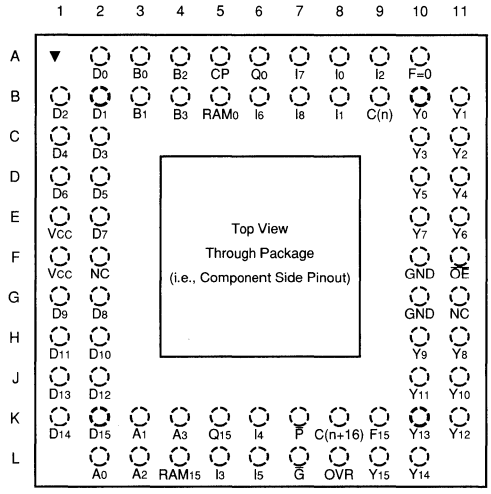
ORDERING INFORMATION

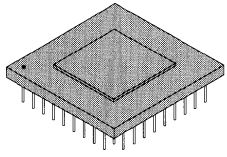
64-pin





68-pin





Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G1)
	0°C to +70°C — COMMERCIAL SCREENING	
35 ns	L29C101DC35	L29C101GC35
	–55°C to +125°C — COMMERCIAL SCREENING	
45 ns	L29C101DM45	L29C101GM45
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
45 ns	L29C101DMB45	L29C101GMB45

LSH32
32-bit Cascadable Barrel Shifter

FEATURES

- 32-bit Input, 32-bit Output Multiplexed to 16 Lines
- Full 0-31 Position Barrel Shift Capability
- Integral Priority Encoder for 32-bit Floating Point Normalization
- Sign-Magnitude or Two's Complement Mantissa Representation
- 32-bit Linear Shifts with Sign or Zero Fill
- Independent Priority Encoder Outputs for Block Floating Point
- DESC SMD No. 5962-89717
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC
  - 68-pin Commercial PGA
  - 68-pin Ceramic PGA

DESCRIPTION

The **LSH32** is a 32-bit high speed shifter designed for use in floating point normalization, word pack/unpack, field extraction, and similar applications. It has 32 data inputs, and 16 output lines. Any shift configuration of the 32 inputs, including circular (barrel) shifting, left shifts with zero fill, and right shift with sign extend are possible. In addition, a built-in priority encoder is provided to aid floating point normalization.

SHIFT ARRAY

The 32 inputs to the LSH32 are applied to a 32-bit shift array. The 32 outputs of this array are multiplexed down to 16 lines for presentation at the device outputs. The array may be configured such that any contiguous 16-bit field (including wraparound of the 32 inputs) may be presented to the output pins under control of the shift code field (wrap mode). Alternatively, the wrap feature may be disabled, resulting in zero or sign bit fill, as appropriate (fill mode). The shift code control assignments and the resulting input to output mapping for the wrap mode are shown in Table 1.

Essentially the LSH32 is configured as a left shift device. That is, a shift code of 00000_2 results in no shift of the input field. A code of 00001_2 provides an effective left shift of 1 position, etc. When viewed as a right shift, the shift code corresponds to the two's complement of the shift distance, i.e., a shift code of 11111_2 (-1_{10}) results in a right shift of one position, etc.

When not in the wrap mode, the LSH32 fills bit positions for which there is no corresponding input bit. The fill value and the positions filled depend on the RIGHT/$\overline{\text{LEFT}}$ (R/$\overline{\text{L}}$) direction pin. This pin is a don't care input when in wrap mode. For left shifts in fill mode, lower bits are filled with zero as shown in Table 2. For right shifts, however, the SIGN input is used as the fill value. Table 3 depicts the bits to be filled as a function of shift code for the right shift case. Note that the R/$\overline{\text{L}}$ input changes only the fill convention, and does not affect the definition of the shift code.

In fill mode, as in wrap mode, the shift code input represents the number of shift positions directly for left shifts, but the two's complement of the shift code results in the equivalent right shift. However, for fill mode the R/$\overline{\text{L}}$ input can be viewed as the most

LSH32 BLOCK DIAGRAM

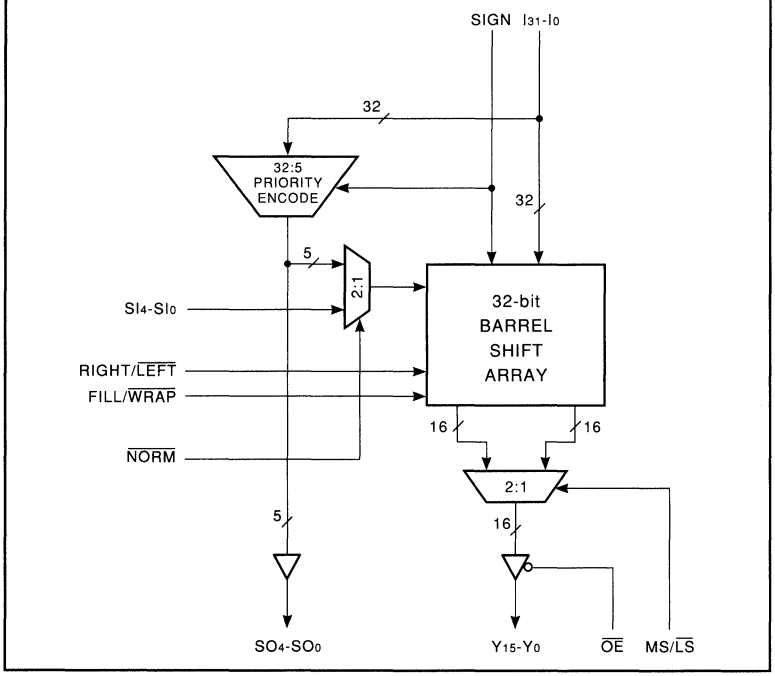


TABLE 1. WRAP MODE SHIFT CODE DEFINITIONS

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0
00001	I_{30}	I_{29}	I_{28}	•••	I_{15}	I_{14}	•••	I_1	I_0	I_{31}
00010	I_{29}	I_{28}	I_{27}	•••	I_{14}	I_{13}	•••	I_0	I_{31}	I_{30}
00011	I_{28}	I_{27}	I_{26}	•••	I_{13}	I_{12}	•••	I_{31}	I_{30}	I_{29}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I_{16}	I_{15}	I_{14}	•••	I_1	I_0	•••	I_{19}	I_{18}	I_{17}
10000	I_{15}	I_{14}	I_{13}	•••	I_0	I_{31}	•••	I_{18}	I_{17}	I_{16}
10001	I_{14}	I_{13}	I_{12}	•••	I_{31}	I_{30}	•••	I_{17}	I_{16}	I_{15}
10010	I_{13}	I_{12}	I_{11}	•••	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I_3	I_2	I_1	•••	I_{20}	I_{19}	•••	I_6	I_5	I_4
11101	I_2	I_1	I_0	•••	I_{19}	I_{18}	•••	I_5	I_4	I_3
11110	I_1	I_0	I_{31}	•••	I_{18}	I_{17}	•••	I_4	I_3	I_2
11111	I_0	I_{31}	I_{30}	•••	I_{17}	I_{16}	•••	I_3	I_2	I_1

TABLE 2. FILL MODE SHIFT CODE DEFINITIONS — LEFT SHIFT

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0
00001	I_{30}	I_{29}	I_{28}	•••	I_{15}	I_{14}	•••	I_1	I_0	0
00010	I_{29}	I_{28}	I_{27}	•••	I_{14}	I_{13}	•••	I_0	0	0
00011	I_{28}	I_{27}	I_{26}	•••	I_{13}	I_{12}	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I_{16}	I_{15}	I_{14}	•••	I_1	I_0	•••	0	0	0
10000	I_{15}	I_{14}	I_{13}	•••	I_0	0	•••	0	0	0
10001	I_{14}	I_{13}	I_{12}	•••	0	0	•••	0	0	0
10010	I_{13}	I_{12}	I_{11}	•••	0	0	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I_3	I_2	I_1	•••	0	0	•••	0	0	0
11101	I_2	I_1	I_0	•••	0	0	•••	0	0	0
11110	I_1	I_0	0	•••	0	0	•••	0	0	0
11111	I_0	0	0	•••	0	0	•••	0	0	0

significant bit of a 6-bit two's complement shift code, comprised of $R/\overline{L}$ concatenated with the SI_4–SI_0 lines. Thus a positive shift code ($R/\overline{L} = 0$) results in a left shift of 0–31 positions, and a negative code ($R/\overline{L} = 1$) a right shift of up to 32 positions. The LSH32 can thus effectively select any contiguous 32-bit field out of a (sign extended and zero filled) 96-bit "input."

OUTPUT MULTIPLEXER

The shift array outputs are applied to a 2:1 multiplexer controlled by the $MS/\overline{LS}$ select line. This multiplexer makes available at the output pins either the most significant or least significant 16 outputs of the shift array.

PRIORITY ENCODER

The 32-bit input bus drives a priority encoder which is used to determine the first significant position for purposes of normalization. The priority encoder produces a five-bit code representing the location of the first non-zero bit in the input word. Code assignment is such that the priority encoder output represents the number of shift positions required to left align the first non-zero bit of the input word. Prior to the priority encoder, the input bits are individually exclusive OR'ed with the SIGN input. This allows normalization in floating point systems using two's complement mantissa representation. A negative value in two's complement representation will cause the exclusive OR gates to invert the input data to the encoder. As a result the leading significant digit will always be "1." This affects only the encoder inputs; the shift array always operates on the raw input data. The priority encoder function table is shown in Table 4.

TABLE 3. FILL MODE SHIFT CODE DEFINITIONS — RIGHT SHIFT

Shift Code	Y_{31}	Y_{30}	Y_{29}	...	Y_{16}	Y_{15}	...	Y_2	Y_1	Y_0
00000	S	S	S	...	S	S	...	S	S	S
00001	S	S	S	...	S	S	...	S	S	I_{31}
00010	S	S	S	...	S	S	...	S	I_{31}	I_{30}
00011	S	S	S	...	S	S	...	I_{31}	I_{30}	I_{29}
.	.	.	.	...	.	.	...	.	.	.
.	.	.	.	...	.	.	...	.	.	.
.	.	.	.	...	.	.	...	.	.	.
01111	S	S	S	...	S	S	...	I_{19}	I_{18}	I_{17}
10000	S	S	S	...	S	I_{31}	...	I_{18}	I_{17}	I_{16}
10001	S	S	S	...	I_{31}	I_{30}	...	I_{17}	I_{16}	I_{15}
10010	S	S	S	...	I_{30}	I_{29}	...	I_{16}	I_{15}	I_{14}
.	.	.	.	...	.	.	...	.	.	.
.	.	.	.	...	.	.	...	.	.	.
.	.	.	.	...	.	.	...	.	.	.
11100	S	S	S	...	I_{20}	I_{19}	...	I_6	I_5	I_4
11101	S	S	S	...	I_{19}	I_{18}	...	I_5	I_4	I_3
11110	S	S	I_{31}	...	I_{18}	I_{17}	...	I_4	I_3	I_2
11111	S	I_{31}	I_{30}	...	I_{17}	I_{16}	...	I_3	I_2	I_1

TABLE 4. PRIORITY ENCODER FUNCTION TABLE

I_{31}	I_{30}	I_{29}	...	I_{16}	I_{15}	...	I_2	I_1	I_0	Shift Code
1	X	X	...	X	X	...	X	X	X	00000
0	1	X	...	X	X	...	X	X	X	00001
0	0	1	...	X	X	...	X	X	X	00010
.	.	.	...	.	.	...	.	.	.	.
.	.	.	...	.	.	...	.	.	.	.
0	0	0	...	1	X	...	X	X	X	01111
0	0	0	...	0	1	...	X	X	X	10000
0	0	0	...	0	0	...	X	X	X	10001
.	.	.	...	.	.	...	.	.	.	.
.	.	.	...	.	.	...	.	.	.	.
0	0	0	...	0	0	...	0	1	X	11110
0	0	0	...	0	0	...	0	0	1	11111
0	0	0	...	0	0	...	0	0	0	11111

NORMALIZE MULTIPLXER

The $\overline{NORM}$ input, when asserted results in the priority encoder output driving the internal shift code inputs directly. It is exactly equivalent to routing the SO_4–SO_0 outputs back to the SI_4–SI_0 inputs. The $\overline{NORM}$ input provides faster normalization of 32-bit data by avoiding the delay associated with routing the shift code off chip. When using the $\overline{NORM}$ function, the LSH32 should be placed in fill mode, with the R/$\overline{L}$ input low.

APPLICATIONS EXAMPLES

Normalization of mantissas up to 32 bits can be accomplished directly by a single LSH32. The $\overline{NORM}$ input is asserted, and fill mode and left shift are selected. The normalized mantissa is then available at the device output in two 16-bit segments, under the control of the output data multiplexer select, the MS/$\overline{LS}$.

If it is desirable to avoid the necessity of multiplexing output data in 16-bit segments, two LSH32 devices can be used in parallel. Both devices receive the same input word, with the MS/$\overline{LS}$ select line of one wired high, and the other low. Each device will then independently determine the shift distance required for normalization, and the full 32 bits of output data will be available simultaneously.

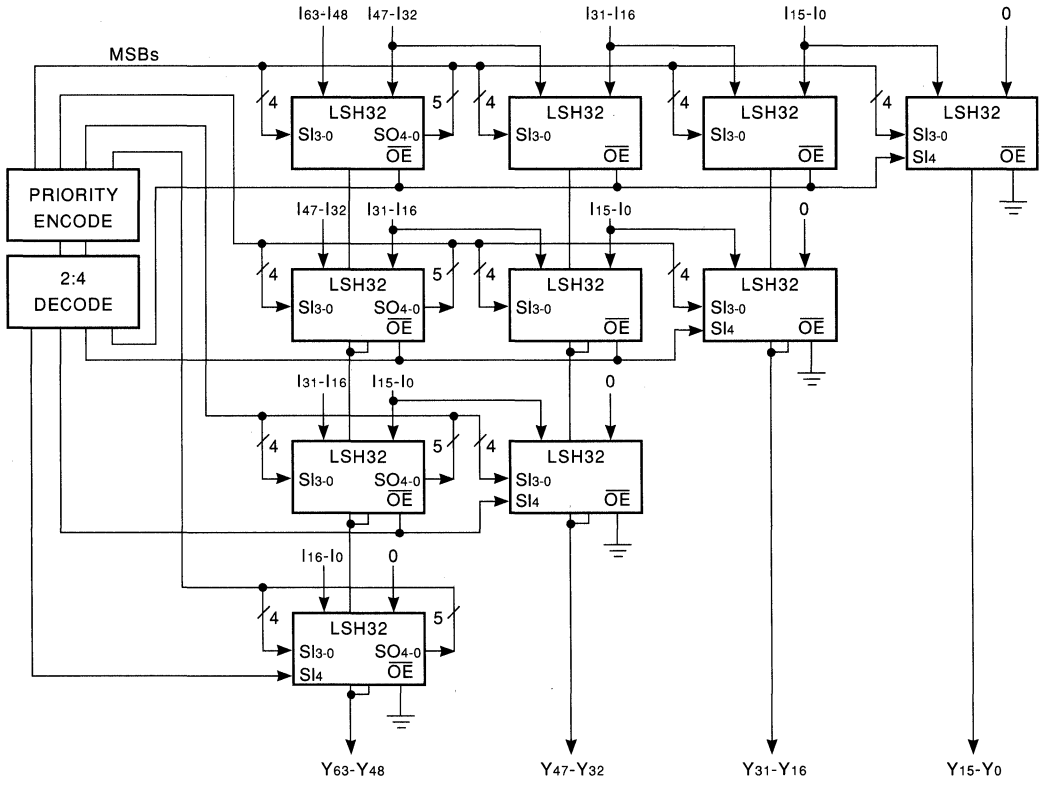
LONG-WORD NORMALIZATION (MULTIPLE CYCLES)

Normalization of floating point mantissas longer than 32 bits can be accomplished by cascading LSH32 units. When cascading for normalization, the device inputs are overlapped such that each device lower in priority than the first shares 16 inputs with its more significant neighbor. Fill mode and left shift are selected, however, internal normalization ($\overline{NORM}$) is not used. The most significant result half of each device is enabled to the output. The shift out (SO_4–SO_0) lines of the most significant slice are connected to the shift in lines of all slices, including the first. The exception is that all SI_4 lines are grounded, limiting the shift distance to 16 positions. The shift distance required for normalization is produced by the priority encoder in the most significant slice. The priority encoder will produce the shift code necessary to normalize the input word if the leading non-zero digit is found in the upper 16 bits. If this is the case, the number of shift positions necessary to accomplish normalization is placed on the SO_4–SO_0 outputs for use by all slices, and the appropriate 0–15 bit shift is accomplished. If the upper 16 bits are all zero, then the maximum shift of 15 places is executed. Single clock normalization requiring shifts longer than 16 bits can be accomplished by a bank-select technique described below.

SINGLE CYCLE LONG-WORD NORMALIZATION

An extension of the above concept is a single clock normalization of long words (potentially requiring shifts of more than 15 places). The arrangement of LSH32s required is shown in Figure 1. Cascading of LSH32 units is accomplished by connecting the SI_3–SI_0 input lines of each unit to the SO_3–SO_0 outputs of the most significant device in the row as before. Essen-

FIGURE 1. SINGLE CYCLE LONG-WORD NORMALIZATION USING LSH32S



tially the LSH32s are arranged in multiple rows or banks such that the inputs to successive rows are left-shifted by 16 positions. The outputs of each row are multiplexed onto a three-state bus. The normalization problem then reduces to selecting from among the several banks that one which has the first non-zero bit of the input value among its 16 most significant positions. If the most significant one in the input file was within the upper 16 locations of a given bank, the SO_4 output of the most significant slice in that bank will be low. Single clock normalization can thus be accomplished simply by enabling onto the three-state output bus the highest priority bank in which this condition is met. In this way the input word will be normalized regardless of the number of shift positions required to accomplish this.

The number of shift positions can be determined simply by concatenation of the SO_3–SO_0 outputs of the most significant slice in the selected row with the encoded Output Enable-bits determining the row number. Note that lower rows need not be fully populated. This is because they represent left shifts in multiples of 16 positions, and the lower bits of the output word will be zero filled. In order to accomplish this zero fill, the least significant device in each row is always enabled, and the row select is instead connected to the SI_4 input. This will force the shift length of the least significant device to a value greater than 15 whenever the row containing that device is not selected. This results in zero fill being accomplished by the equivalently positioned slice in a higher bank, as shown in the diagram.

BLOCK FLOATING POINT

With a small amount of external logic, block floating point operations are easily accomplished by the LSH32. Data resulting from a vector operation are applied to the LSH32 with the $\overline{NORM}$-input deasserted. The SO_4–SO_0 outputs fill then represent the normalization shift distance for each vector element in turn. By use of an external latch and comparator, the maximum shift distance encountered across all elements in the vector is saved for use in the next block operation (or block normalization). During this subsequent pass through the data, the shift code saved from the previous pass is applied uniformly across all elements of the vector. Since the LSH32 is not used in the internal normalize mode, this operation can be pipelined, thereby obtaining the desired shift distance for the next pass while simultaneously applying the normalization required from the previous pass.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS

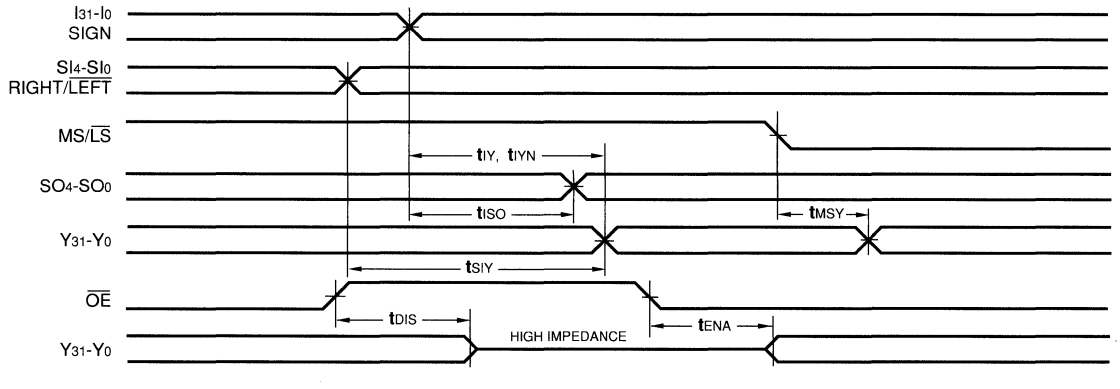
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LSH32–					
		42		32		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{IY}	I, SIGN Inputs to Y Outputs		42		32		20
t_{IYN}	I, SIGN Inputs to Y Outputs, Normalize Mode		75		60		20
t_{ISO}	I, SIGN Inputs to SO Outputs		55		42		20
t_{SIY}	SI, RIGHT/$\overline{\text{LEFT}}$ to Y Outputs		52		40		20
t_{MSY}	MS/$\overline{\text{LS}}$ Select to Y Outputs		28		24		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		20		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		20		20		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LSH32–					
		50		40		30	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{IY}	I, SIGN Inputs to Y Outputs		50		40		30
t_{IYN}	I, SIGN Inputs to Y Outputs, Normalize Mode		85		75		58
t_{ISO}	I, SIGN Inputs to SO Outputs		65		52		42
t_{SIY}	SI, RIGHT/$\overline{\text{LEFT}}$ to Y Outputs		62		52		40
t_{MSY}	MS/$\overline{\text{LS}}$ Select to Y Outputs		32		26		24
t_{DIS}	Three-State Output Disable Delay (Note 11)		22		20		17
t_{ENA}	Three-State Output Enable Delay (Note 11)		22		20		17

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 2. INPUT CIRCUIT

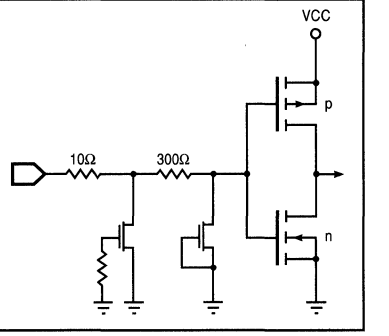


FIGURE 3. OUTPUT CIRCUIT

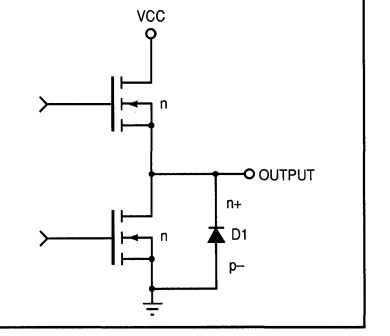
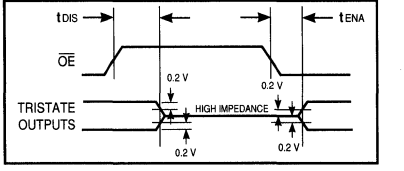
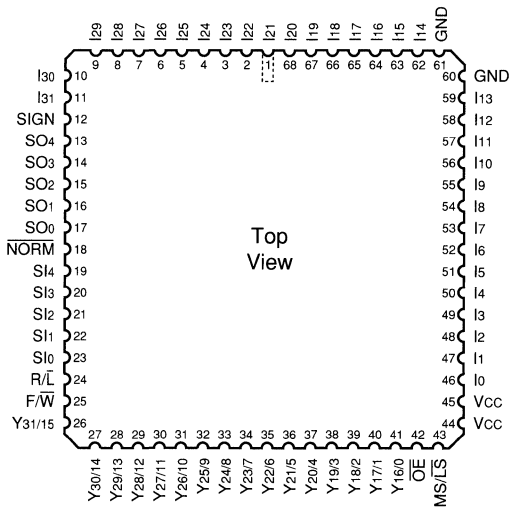


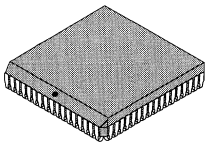
FIGURE 4. THRESHOLD LEVELS

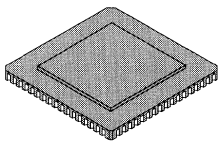


ORDERING INFORMATION

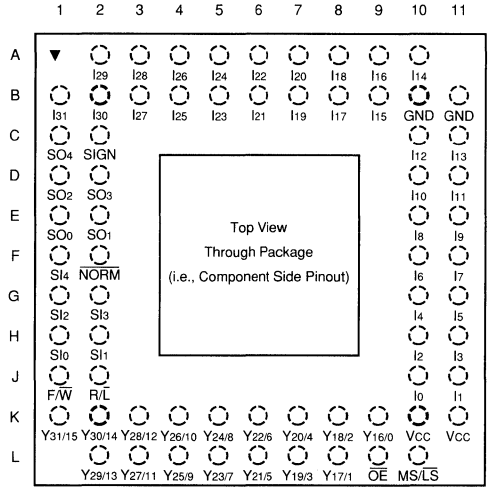
68-pin

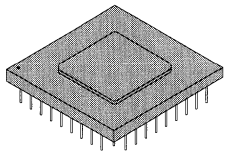


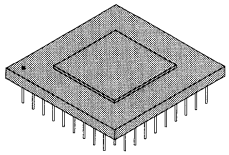




68-pin







Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Commercial Pin Grid Array (E1)	Ceramic Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening			
42 ns	LSH32JC42	LSH32KC42	LSH32EC42	LSH32GC42
32 ns	LSH32JC32	LSH32KC32	LSH32EC32	LSH32GC32
20 ns	LSH32JC20	LSH32KC20	LSH32EC20	LSH32GC20
	–55°C to +125°C — Commercial Screening			
50 ns		LSH32KM50		LSH32GM50
40 ns		LSH32KM40		LSH32GM40
30 ns		LSH32KM30		LSH32GM30
	–55°C to +125°C — MIL-STD-883 Compliant			
50 ns		LSH32KMB50		LSH32GMB50
40 ns		LSH32KMB40		LSH32GMB40
30 ns		LSH32KMB30		LSH32GMB30

LSH33
32-bit Barrel Shifter with Registers

FEATURES

- 32-bit Input, 32-bit Output Multiplexed to 16 Lines
- Full 0-31 Position Barrel Shift Capability
- Integral Priority Encoder for 32-bit Floating Point Normalization
- Sign-Magnitude or Two's Complement Mantissa Representation
- 32-bit Linear Shifts with Sign or Zero Fill
- Independent Priority Encoder Outputs for Block Floating Point
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC
  - 68-pin Commercial PGA
  - 68-pin Ceramic PGA

DESCRIPTION

The **LSH33** is a 32-bit high speed shifter designed for use in floating point normalization, word pack/unpack, field extraction, and similar applications. It has 32 data inputs, and 16 output lines. Any shift configuration of the 32 inputs, including circular (barrel) shifting, left shifts with zero fill, and right shifts with sign extension are possible. In addition, a built-in priority encoder is provided to aid floating point normalization.

Input/Output registers provide complete pipelined operation. Both have independent bypass paths for complete flexibility. When FTI = 1, the input registers are bypassed. Likewise, when FTO= 1, the output registers are bypassed.

SHIFT ARRAY

The 32 inputs, which can be registered, to the LSH33 are applied to a 32-bit shift array. The 32 outputs, which can also be registered, of this array are then multiplexed down to 16 lines for presentation at the device outputs. The array may be configured such that any contiguous 16-bit field (including wraparound of the 32 inputs) may be presented to the output pins under control of the shift code field (wrap mode). Alternatively, the wrap feature may be disabled, resulting in zero or sign bit fill, as appropriate (fill mode). The shift code control assignments and the resulting input to output mapping for the wrap mode are shown in Table 1.

Essentially the LSH33 is configured as a left shift device. That is, a shift code of 00000_2 results in no shift of the input field. A code of 00001_2 provides an effective left shift of 1 position, etc. When viewed as a right shift, the shift code corresponds to the two's complement of the shift distance, i.e., a shift code of 11111_2 (-1_{10}) results in a right shift of one position, etc.

When not in the wrap mode, the LSH33 fills bit positions for which there is no corresponding input bit. The fill value and the positions filled depend on the RIGHT/$\overline{\text{LEFT}}$ (R/$\overline{\text{L}}$) direction pin. This pin is a don't care input when in wrap mode. For left shifts in fill mode, lower bits are filled with zero as shown in Table 2. For right shifts, however, the SIGN input is used as the fill value. Table 3 depicts the bits to be filled as a function of shift code for the right shift case. Note that the R/$\overline{\text{L}}$ input changes only the fill convention, and does not affect the definition of the shift code.

LSH33 BLOCK DIAGRAM

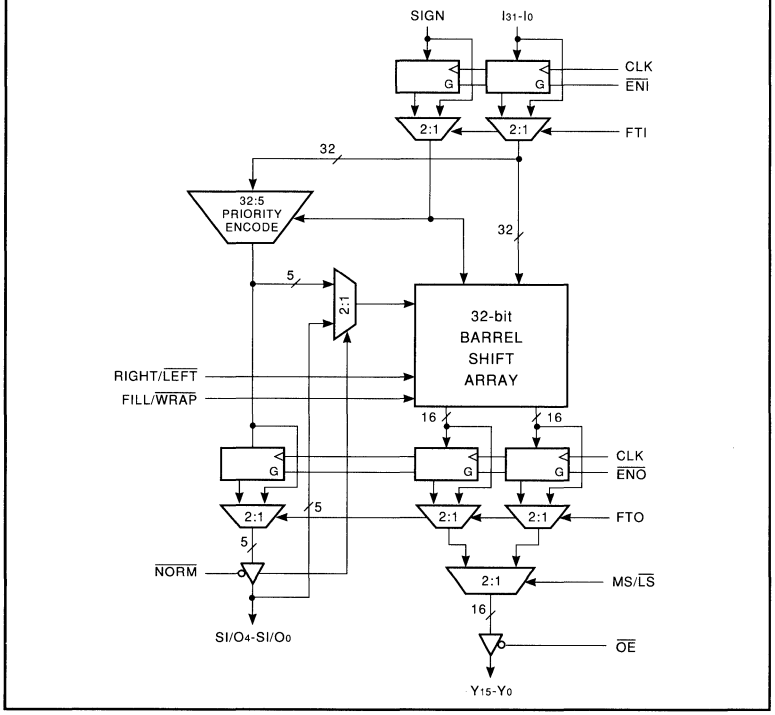


TABLE 1. WRAP MODE SHIFT CODE DEFINITIONS

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0
00001	I_{30}	I_{29}	I_{28}	•••	I_{15}	I_{14}	•••	I_1	I_0	I_{31}
00010	I_{29}	I_{28}	I_{27}	•••	I_{14}	I_{13}	•••	I_0	I_{31}	I_{30}
00011	I_{28}	I_{27}	I_{26}	•••	I_{13}	I_{12}	•••	I_{31}	I_{30}	I_{29}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I_{16}	I_{15}	I_{14}	•••	I_1	I_0	•••	I_{19}	I_{18}	I_{17}
10000	I_{15}	I_{14}	I_{13}	•••	I_0	I_{31}	•••	I_{18}	I_{17}	I_{16}
10001	I_{14}	I_{13}	I_{12}	•••	I_{31}	I_{30}	•••	I_{17}	I_{16}	I_{15}
10010	I_{13}	I_{12}	I_{11}	•••	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I_3	I_2	I_1	•••	I_{20}	I_{19}	•••	I_6	I_5	I_4
11101	I_2	I_1	I_0	•••	I_{19}	I_{18}	•••	I_5	I_4	I_3
11110	I_1	I_0	I_{31}	•••	I_{18}	I_{17}	•••	I_4	I_3	I_2
11111	I_0	I_{31}	I_{30}	•••	I_{17}	I_{16}	•••	I_3	I_2	I_1

TABLE 2. FILL MODE SHIFT CODE DEFINITIONS — LEFT SHIFT

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0
00001	I_{30}	I_{29}	I_{28}	•••	I_{15}	I_{14}	•••	I_1	I_0	0
00010	I_{29}	I_{28}	I_{27}	•••	I_{14}	I_{13}	•••	I_0	0	0
00011	I_{28}	I_{27}	I_{26}	•••	I_{13}	I_{12}	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	I_{16}	I_{15}	I_{14}	•••	I_1	I_0	•••	0	0	0
10000	I_{15}	I_{14}	I_{13}	•••	I_0	0	•••	0	0	0
10001	I_{14}	I_{13}	I_{12}	•••	0	0	•••	0	0	0
10010	I_{13}	I_{12}	I_{11}	•••	0	0	•••	0	0	0
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	I_3	I_2	I_1	•••	0	0	•••	0	0	0
11101	I_2	I_1	I_0	•••	0	0	•••	0	0	0
11110	I_1	I_0	0	•••	0	0	•••	0	0	0
11111	I_0	0	0	•••	0	0	•••	0	0	0

In fill mode, as in wrap mode, the shift code input represents the number of shift positions directly for left shifts, but the two's complement of the shift code results in the equivalent right shift. However, for fill mode the R/$\overline{L}$ input can be viewed as the most significant bit of a 6-bit two's complement shift code, comprised of R/$\overline{L}$ concatenated with the SI_4–SI_0 lines. Thus, a positive shift code (R/$\overline{L}$ = 0) results in a left shift of 0–31 positions, and a negative code (R/$\overline{L}$ = 1) a right shift of up to 32 positions. The LSH33 can thus effectively select any contiguous 32-bit field out of a (sign extended and zero filled) 96-bit "input."

OUTPUT MULTIPLEXER

The shift array outputs can be registered and then applied to a 2:1 multiplexer controlled by the MS/$\overline{LS}$ select line. This multiplexer makes available at the output pins either the most significant or least significant 16 outputs of the shift array.

PRIORITY ENCODER

The 32-bit input bus drives a priority encoder which is used to determine the first significant position for purposes of normalization. The priority encoder produces a five-bit code representing the location of the first non-zero bit in the input word. Code assignment is such that the priority encoder output represents the number of shift positions required to left align the first non-zero bit of the input word. Prior to the priority encoder, the input bits are individually exclusive OR'ed with the SIGN input. This allows normalization in floating point systems using two's complement mantissa representation. A negative value in two's complement representation will cause the exclusive OR gates to invert the input data to the encoder. As a result, the leading significant digit will always be "1."

TABLE 3. FILL MODE SHIFT CODE DEFINITIONS — RIGHT SHIFT

Shift Code	Y_{31}	Y_{30}	Y_{29}	•••	Y_{16}	Y_{15}	•••	Y_2	Y_1	Y_0
00000	S	S	S	•••	S	S	•••	S	S	S
00001	S	S	S	•••	S	S	•••	S	S	I_{31}
00010	S	S	S	•••	S	S	•••	S	I_{31}	I_{30}
00011	S	S	S	•••	S	S	•••	I_{31}	I_{30}	I_{29}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
01111	S	S	S	•••	S	S	•••	I_{19}	I_{18}	I_{17}
10000	S	S	S	•••	S	I_{31}	•••	I_{18}	I_{17}	I_{16}
10001	S	S	S	•••	I_{31}	I_{30}	•••	I_{17}	I_{16}	I_{15}
10010	S	S	S	•••	I_{30}	I_{29}	•••	I_{16}	I_{15}	I_{14}
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
•	•	•	•	•••	•	•	•••	•	•	•
11100	S	S	S	•••	I_{20}	I_{19}	•••	I_6	I_5	I_4
11101	S	S	S	•••	I_{19}	I_{18}	•••	I_5	I_4	I_3
11110	S	S	I_{31}	•••	I_{18}	I_{17}	•••	I_4	I_3	I_2
11111	S	I_{31}	I_{30}	•••	I_{17}	I_{16}	•••	I_3	I_2	I_1

TABLE 4. PRIORITY ENCODER FUNCTION TABLE

I_{31}	I_{30}	I_{29}	•••	I_{16}	I_{15}	•••	I_2	I_1	I_0	Shift Code
1	X	X	•••	X	X	•••	X	X	X	00000
0	1	X	•••	X	X	•••	X	X	X	00001
0	0	1	•••	X	X	•••	X	X	X	00010
•	•	•	•••	•	•	•••	•	•	•	•
•	•	•	•••	•	•	•••	•	•	•	•
0	0	0	•••	1	X	•••	X	X	X	01111
0	0	0	•••	0	1	•••	X	X	X	10000
0	0	0	•••	0	0	•••	X	X	X	10001
•	•	•	•••	•	•	•••	•	•	•	•
•	•	•	•••	•	•	•••	•	•	•	•
0	0	0	•••	0	0	•••	0	1	X	11110
0	0	0	•••	0	0	•••	0	0	1	11111
0	0	0	•••	0	0	•••	0	0	0	11111

This affects only the encoder inputs; the shift array always operates on the raw input data. The priority encoder function table is shown in Table 4.

NORMALIZE MULTIPLEXER

The $\overline{\text{NORM}}$ input, when asserted, results in the priority encoder output driving the internal shift code inputs directly. When using the $\overline{\text{NORM}}$ function, the LSH33 should be placed in fill mode, with the R/$\overline{\text{L}}$ input low.

When $\overline{\text{NORM}}$ is high (not asserted), the SI/O_4–SI/O_0 port acts as the shift code input to the shifter.

APPLICATIONS EXAMPLES

Normalization of mantissas up to 32 bits can be accomplished directly by a single LSH33. To do this, the $\overline{\text{NORM}}$ input is asserted, and fill mode and left shift are selected. The normalized mantissa is then available at the device output in two 16-bit segments, under the control of the output data multiplexer select, the MS/$\overline{\text{LS}}$ signal.

If it is desirable to avoid the necessity of multiplexing output data in 16-bit segments, two LSH33 devices can be used in parallel. Both devices receive the same input word, with the MS/$\overline{\text{LS}}$ select line of one wired high, and the other low. Each device will then independently determine the shift distance required for normalization, and the full 32 bits of output data will be available simultaneously.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS — COMMERCIAL OPERATING RANGE (0°C to +70°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

From Input \ To Output	LSH33-40		LSH33-30		LSH33-20	
	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0
FTI = 0, FTO = 0						
CLK	28	28	24	24	15	15
MS/$\overline{LS}$	28	—	24	—	15	—
FTI = 0, FTO= 1						
CLK ($\overline{NORM}$ = 0/1)	73/40	55/—	58/30	42/—	20/20	20/—
SI_4-SI_0	52	—	40	—	20	—
R/$\overline{L}$, F/$\overline{W}$	52	—	40	—	20	—
MS/$\overline{LS}$	28	—	24	—	15	—
FTI = 1, FTO = 0						
CLK	28	28	24	24	15	15
MS/$\overline{LS}$	28	—	24	—	15	—
FTI = 1, FTO = 1						
I_{31}-I_0, SIGN ($\overline{NORM}$ = 0/1)	73/40	55/—	58/30	42/—	20/20	20/—
SI_4-SI_0	52	—	40	—	20	—
R/$\overline{L}$, F/$\overline{W}$	52	—	40	—	20	—
MS/$\overline{LS}$	28	—	24	—	15	—

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

Input	LSH33-40				LSH33-30				LSH33-20			
	FTI = 0		FTI = 1		FTI = 0		FTI = 1		FTI = 0		FTI = 1	
	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
I_{31}-I_0, SIGN	12	3	20	2	10	3	15	2	8	0	8	2
SI_4-SI_0	17	0	17	0	15	0	15	0	8	0	8	0
R/$\overline{L}$, F/$\overline{W}$	12	0	12	0	10	0	10	0	8	0	8	0
$\overline{ENI}$, $\overline{ENO}$	12	0	12	0	10	0	10	0	8	0	8	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	LSH33-40	LSH33-30	LSH33-20
t_{ENA}	20	17	15
t_{DIS}	20	17	15

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	LSH33-40	LSH33-30	LSH33-20
Minimum Cycle Time	30	20	15
Highgoing Pulse	12	9	7
Lowgoing Pulse	12	9	7

SWITCHING CHARACTERISTICS — MILITARY OPERATING RANGE (–55°C to +125°C)

GUARANTEED MAXIMUM COMBINATIONAL DELAYS *Notes 9, 10 (ns)*

To Output / From Input	LSH33-50		LSH33-40		LSH33-30	
	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0	Y_{15}-Y_0	SO_4-SO_0
FTI = 0, FTO = 0						
CLK	32	32	28	28	24	24
MS/$\overline{LS}$	32	—	28	—	24	—
FTI = 0, FTO= 1						
CLK ($\overline{NORM}$ = 0/1)	80/50	65/—	73/40	55/—	58/30	42/—
SI_4-SI_0	62	—	52	—	40	—
R/$\overline{L}$, F/$\overline{W}$	62	—	52	—	40	—
MS/$\overline{LS}$	32	—	28	—	24	—
FTI = 1, FTO = 0						
CLK	32	32	28	28	24	24
MS/$\overline{LS}$	32	—	28	—	24	—
FTI = 1, FTO = 1						
I_{31}-I_0, SIGN ($\overline{NORM}$ = 0/1)	80/50	65/—	73/40	55/—	58/30	42/—
SI_4-SI_0	62	—	52	—	40	—
R/$\overline{L}$, F/$\overline{W}$	62	—	52	—	40	—
MS/$\overline{LS}$	62	—	28	—	24	—

GUARANTEED MINIMUM SETUP AND HOLD TIMES WITH RESPECT TO CLOCK RISING EDGE *Notes 9, 10 (ns)*

	LSH33-50				LSH33-40				LSH33-30			
	FTI = 0		FTI = 1		FTI = 0		FTI = 1		FTI = 0		FTI = 1	
Input	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold	Setup	Hold
I_{31}-I_0, SIGN	15	3	20	2	12	3	20	2	10	0	15	2
SI_4-SI_0	20	0	20	0	17	0	17	0	15	0	15	0
R/$\overline{L}$, F/$\overline{W}$	15	0	15	0	12	0	12	0	10	0	10	0
$\overline{ENI}$, $\overline{ENO}$	15	0	15	0	12	0	12	0	10	0	10	0

TRI-STATE ENABLE/DISABLE TIMES *Notes 9, 10, 11 (ns)*

	LSH33-50	LSH33-40	LSH33-30
t_{ENA}	22	20	17
t_{DIS}	22	20	17

CLOCK CYCLE TIME AND PULSE WIDTH *Notes 9, 10 (ns)*

	LSH33-50	LSH33-40	LSH33-30
Minimum Cycle Time	35	30	20
Highgoing Pulse	15	12	9
Lowgoing Pulse	15	12	9

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

3

FIGURE 1. INPUT CIRCUIT

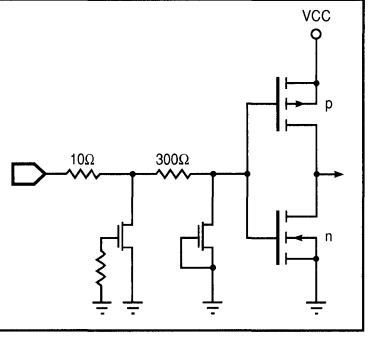


FIGURE 2. OUTPUT CIRCUIT

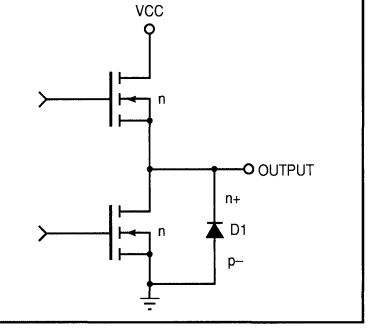
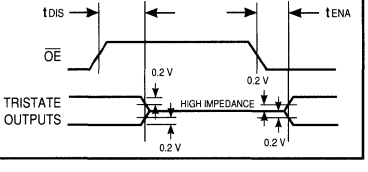
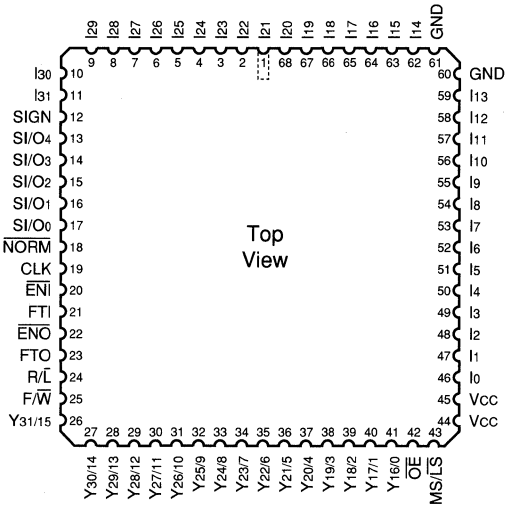


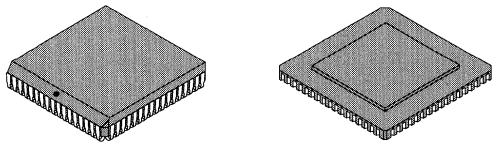
FIGURE 3. THRESHOLD LEVELS



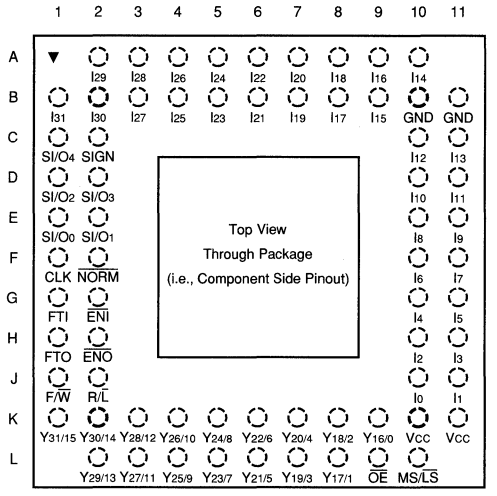
ORDERING INFORMATION

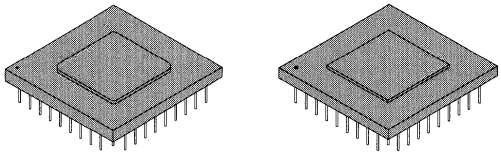
68-pin





68-pin





Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	Commercial Pin Grid Array (E1)	Ceramic Pin Grid Array (G1)
	0°C to +70°C — Commercial Screening			
40 ns	LSH33JC40	LSH33KC40	LSH33EC40	LSH33GC40
30 ns	LSH33JC30	LSH33KC30	LSH33EC30	LSH33GC30
20 ns	LSH33JC20	LSH33KC20	LSH33EC20	LSH33GC20
	–55°C to +125°C — Commercial Screening			
50 ns		LSH33KM50		LSH33GM50
40 ns		LSH33KM40		LSH33GM40
30 ns		LSH33KM30		LSH33GM30
	–55°C to +125°C — MIL-STD-883 Compliant			
50 ns		LSH33KMB50		LSH33GMB50
40 ns		LSH33KMB40		LSH33GMB40
30 ns		LSH33KMB30		LSH33GMB30

FEATURES

- High Speed (50 MHz), Low Power (125 mW), CMOS 64-bit Digital Correlator
- Replaces TRW/Raytheon TDC1023/TMC2023
- Bit Can be Selectively Masked
- Three-State Outputs
- DESC SMD No. 5962-89711
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Ceramic DIP
  - 28-pin Ceramic LCC

DESCRIPTION

The **L10C23** is a high speed CMOS 64-bit digital correlator. It is pin-for-pin equivalent to the TRW/Raytheon TDC1023/TMC2023. The L10C23 operates over the full military ambient temperature range using advanced CMOS technology.

The L10C23 produces the 7-bit correlation score of two input words of up to 64 bits, denoted A and B. The A and B inputs are serially shifted into two independently clocked 64-bit registers. The A register is clocked on the rising edge of CLK A, and the B register is clocked on the rising edge of CLK B.

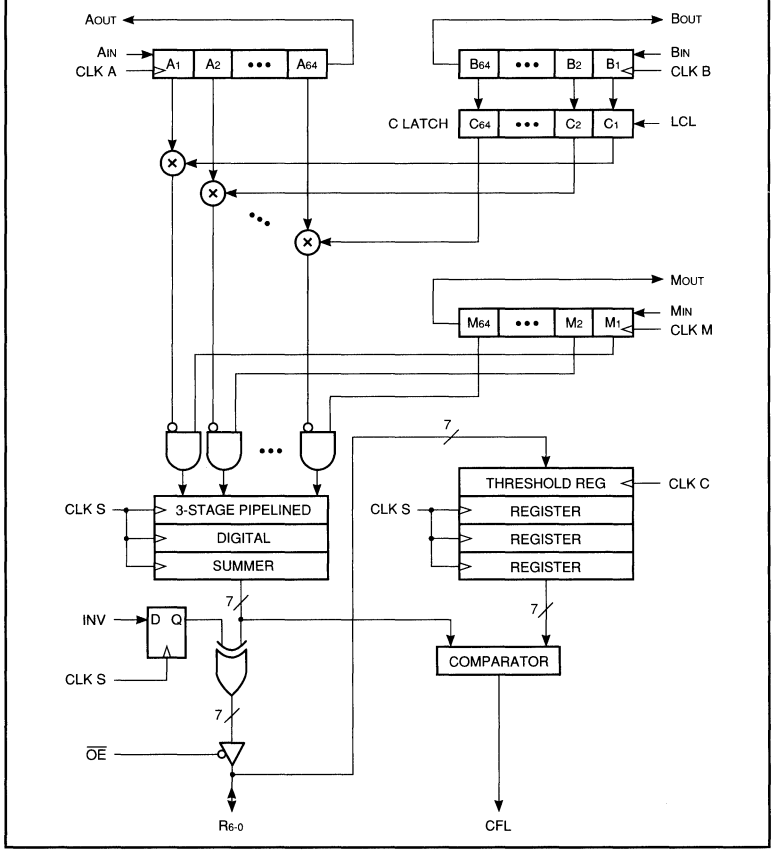
The outputs of the B register drive a 64-bit transparent latch, denoted the C latch. The C latch is controlled by the LCL (Load C Latch) input. A HIGH level on the LCL input causes the C latch to be transparent, allowing the contents of the B register to be applied directly to the correlator array. When the LCL input is LOW, the data in the C latch is held, so that the B input may be loaded with a new correlation reference without affecting the current reference value stored in C.

Each bit in the A register is exclusive NOR'ed with the corresponding bit in the C latch, implementing a single bit multiplication at each bit position.

The mask register, denoted by M, is a third 64-bit register, which is serially loaded from the M input on the rising edge of CLK M. Bit positions in the M register which are set to zero mask the corresponding bits in the A and C registers from participating in the correlation score. This can be used to reduce the effective length of the correlation, or to correlate against only one channel of a bit-multiplexed datastream without deinterleaving the data.

The output of the masking process is a 64-bit vector which contains ones in the locations in which A and B data match, and which are unmasked (M register contains a '1'). This 64-bit vector is applied to a pipelined digital summer which calculates the total number of ones in the vector (the correlation score). The summer network contains three pipeline stages, which are clocked on the rising edge of CLK S. Calculation of a

L10C23 Block Diagram



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edge of CLK S. Calculation of a correlation score therefore requires three clock cycles, but a new result can be obtained on each cycle once the pipeline is filled.

Because a portion of the summer logic is located between the input registers and the first pipeline register, some timing restrictions exist between CLK S and CLK A, CLK B, or CLK M. CLK S may be tied to an input clock (usually CLK A) to obtain a continuously updated correlation score, delayed by three cycles from the data. Under this condition, CLK S may be skewed later than CLK A by no more than t_{SK} to assure that the A register outputs have not changed before the S clock occurs.

Alternatively, CLK S may be asynchronous to the input clocks, as long as data is stable at the pipeline register inputs prior to the CLK S rising edge. This condition can be met by assuring that CLK S occurs at least t_{PS} after the input clock.

The summer output represents a count of the number of matching positions in the input data streams. This 7-bit result can be inverted (one's complemented) by loading a '1' into the INV register.

Correlation values which exceed a predetermined threshold can be detected via the Threshold register and Comparator. The Threshold register is loaded with a 7-bit value via the R_{6-0} pins at the rising edge of CLK C and while $\overline{OE}$ is HIGH. To achieve synchronization with the digital summer, the Threshold register contents are fed into pipeline registers clocked by CLK S. The compare flag output (CFL) goes HIGH when the summer output is equal to or greater than the contents of the Threshold register.

Cascading the L10C23 devices for longer correlation lengths and more bits of reference or data precision is easily accomplished. The A, B, and M registers have serial outputs to directly drive the corresponding inputs of succeeding devices. The correlation scores of multiple devices in such a system should be added together to obtain the overall correlation score.

Correlation on data exceeding one bit of precision can be accomplished by first calculating single-bit correlation scores at each bit position, then adding the results after weighting them appropriately. Thus, one L10C23 would be used for each bit of precision in the data.

Logic Devices' L4C381 16-bit ALU can be used to assist in adding the outputs of several L10C23 correlators. When adding several 7-bit correlation scores, advantage can be taken of the fact that the sum of two 7-bit numbers will not exceed 8 bits. Thus the L4C381 can simultaneously perform two 7-bit additions. The first two operands are applied to A_{6-0} and B_{6-0}, with the result appearing on F_{7-0}. The second pair of operands are applied to A_{14-8} and B_{14-8}, with the result appearing in F_{15-8}. The unused inputs are tied to ground. If it can be guaranteed that at least one of the input scores will not reach its maximum value of 64, then this technique can also be applied in the second tier of adders. In this case, while the inputs have 8 bits of precision, the maximum value that their sum can assume is 255, which is expressable in 8 bits.

Alternatively, when performing long correlations on relatively slow datastreams, one L4C381 can be configured using its feedback mode to accumulate the correlation scores of a number of L10C23s. To accomplish this, the outputs of all the correlators are tied together on a three-state bus. Each one is sequentially enabled and clocked into the L4C381, which accumulates the total resulting score.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

3

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

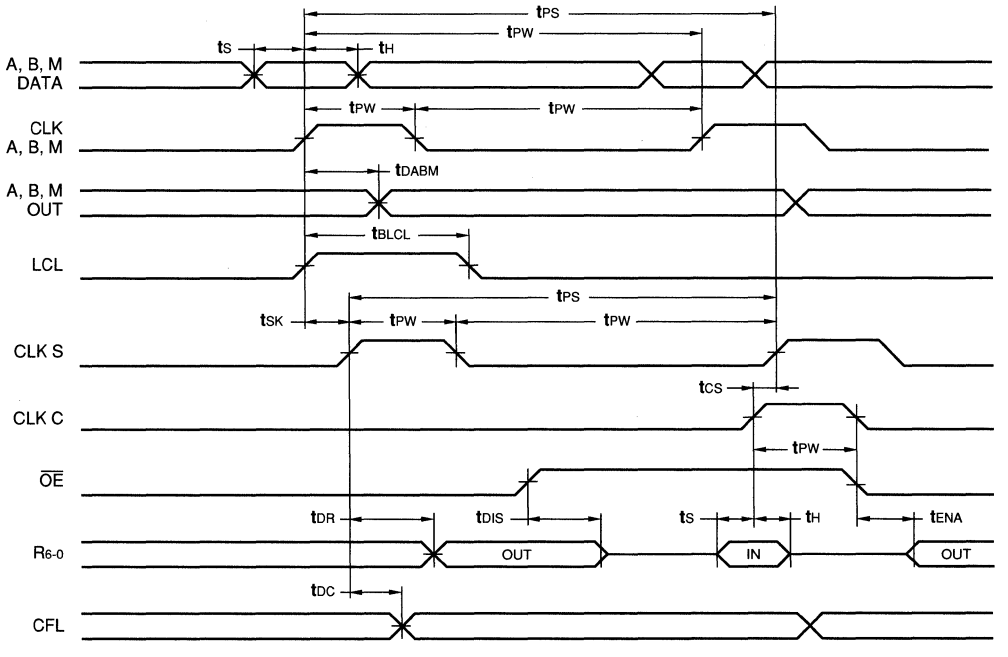
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		25	100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			0.5	mA

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L10C23–					
		50		30		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PABM}	A, B, M Clock Period	50		28		20	
t_{PW}	A, B, M, S, C Clock Pulse Width	20		12		8	
t_S	Input Setup Time	20		10		10	
t_H	Input Hold Time	0		0		0	
t_{BLCL}	B Clock to LCL Hold	20		12		8	
t_{CS}	C Clock to S Clock	50		28		20	
t_{DABM}	A, B, M Clock to A, B, M Out		25		20		18
t_{PS}	S Clock Period, A, B, M Clock to S Clock Delay	50		28		20	
t_{SK}	A, B, M Clock to S Clock Skew (Note 8)		3		3		3
t_{DR}	S Clock to R_{6-0}		35		30		22
t_{DC}	S Clock to CFL		25		20		18
t_{ENA}	Output Enable Time (Note 11)		30		18		16
t_{DIS}	Output Disable Time (Note 11)		35		16		14

SWITCHING WAVEFORMS

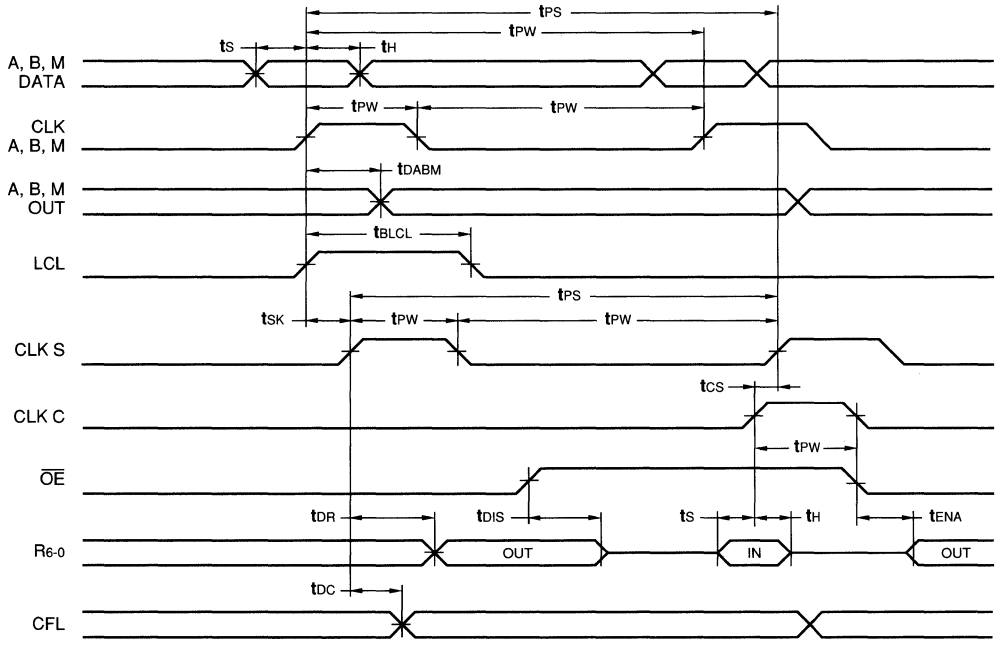


SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE (-55°C to +125°C) *Notes 9, 10 (ns)*

		L10C23–					
		60		35		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PABM}	A, B, M Clock Period	58		33		20	
t_{PW}	A, B, M, S, C Clock Pulse Width	20		14		8	
t_S	Input Setup Time	22		12		12	
t_H	Input Hold Time	0		0		0	
t_{BLCL}	B Clock to LCL Hold	20		14		8	
t_{CS}	C Clock to S Clock	58		33		20	
t_{DABM}	A, B, M Clock to A, B, M Out		30		23		20
t_{PS}	S Clock Period, A, B, M Clock to S Clock Delay	58		33		20	
t_{SK}	A, B, M Clock to S Clock Skew (Note 8)		3		3		3
t_{DR}	S Clock to R_{6-0}		40		35		27
t_{DC}	S Clock to CFL		30		23		18
t_{ENA}	Output Enable Time (Note 11)		35		20		18
t_{DIS}	Output Disable Time (Note 11)		40		18		16

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

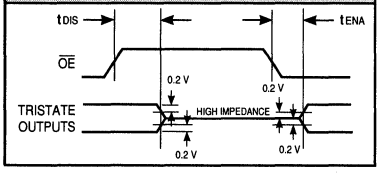
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

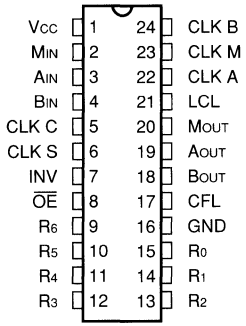
12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 1. THRESHOLD LEVELS

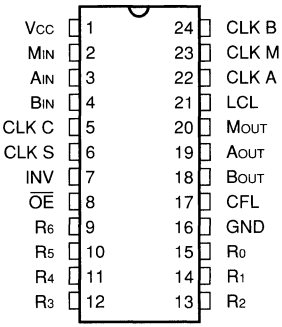


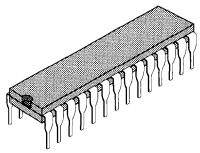
ORDERING INFORMATION

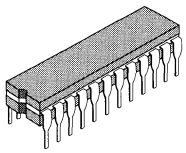
24-pin — 0.3" wide

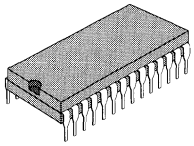


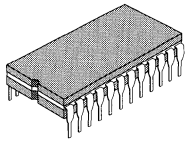
24-pin — 0.6" wide







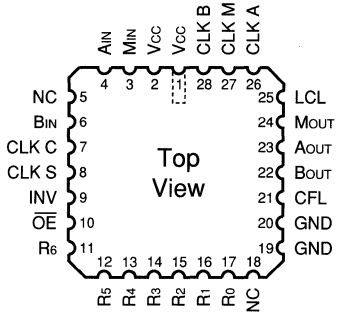


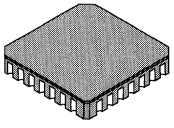


Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic DIP (P1)	Ceramic DIP (C4)
	0°C to +70°C — COMMERCIAL SCREENING			
50 ns	L10C23NC50	L10C23IC50	L10C23PC50	L10C23CC50
30 ns	L10C23NC30	L10C23IC30	L10C23PC30	L10C23CC30
20 ns	L10C23NC20	L10C23IC20	L10C23PC20	L10C23CC20
	–55°C to +125°C — COMMERCIAL SCREENING			
60 ns		L10C23IM60		L10C23CM60
35 ns		L10C23IM35		L10C23CM35
20 ns		L10C23IM20		L10C23CM20
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
60 ns		L10C23IMB60		L10C23CMB60
35 ns		L10C23IMB35		L10C23CMB35
20 ns		L10C23IMB20		L10C23CMB20

ORDERING INFORMATION

28-pin





Speed	Ceramic Leadless Chip Carrier (K1)		
	0°C to +70°C — COMMERCIAL SCREENING		
50 ns	L10C23KC50		
30 ns	L10C23KC30		
20 ns	L10C23KC20		
	–55°C to +125°C — COMMERCIAL SCREENING		
60 ns	L10C23KM60		
35 ns	L10C23KM35		
20 ns	L10C23KM20		
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
60 ns	L10C23KMB60		
35 ns	L10C23KMB35		
20 ns	L10C23KMB20		

Ordering Information 1
Video Imaging Products 2
Arithmetic Logic Units & Special Arithmetic Functions 3
Multipliers & Multiplier-Accumulators 4
Register Products 5
Peripheral Products 6
Quality and Reliability 7
Technology and Design Features 8
Package Information 9
Product Listing 10
Sales Offices 11

Multipliers & Multiplier-Accumulators

MULTIPLIERS & MULTIPLIER-ACCUMULATORS 4-1

Multipliers

LMU08 8 x 8-bit Parallel Multiplier, Signed 4-3
LMU8U 8 x 8-bit Parallel Multiplier, Unsigned 4-3
LMU557 8 x 8-bit Parallel Multiplier, Latched Output 4-11
LMU558 8 x 8-bit Parallel Multiplier, Unregistered 4-11
LMU12 12 x 12-bit Parallel Multiplier 4-19
LMU112 12 x 12-bit Parallel Multiplier, Reduced Pinout 4-25
LMU16 16 x 16-bit Parallel Multiplier 4-31
LMU216 16 x 16-bit Parallel Multiplier, Surface Mount 4-31
LMU17 16 x 16-bit Parallel Multiplier, Microprogrammable 4-39
LMU217 16 x 16-bit Parallel Multiplier, Microprogrammable, Surface Mount 4-39
LMU18 16 x 16-bit Parallel Multiplier, 32 Outputs 4-47

Multiplier-Accumulators

LMA1009 12 x 12-bit Multiplier-Accumulator 4-55
LMA2009 12 x 12-bit Multiplier-Accumulator, Surface Mount 4-55
LMA1010 16 x 16-bit Multiplier-Accumulator 4-63
LMA2010 16 x 16-bit Multiplier-Accumulator, Surface Mount 4-63

Multiplier-Summers

LMS12 12 x 12 + 26-bit Cascadable Multiplier-Summer, FIR 4-71

LMU08/8U
8 x 8-bit Parallel Multiplier

FEATURES

- 35 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- LMU08 Replaces TRW TMC208K
- LMU8U Replaces TRW TMC28KU
- Two's Complement (LMU08), or Unsigned Operands (LMU8U)
- Three-State Outputs
- DESC SMD No. 5962-88739
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Ceramic DIP
  - 44-pin Plastic LCC, J-Lead
  - 44-pin Ceramic LCC

DESCRIPTION

The **LMU08** and **LMU8U** are high-speed, low power 8-bit parallel multipliers. They are pin-for-pin equivalents with TRW TMC208K and TMC28KU type multipliers. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

Both the LMU08 and the LMU8U produce the 16-bit product of two 8-bit numbers. The LMU08 accepts operands in two's complement format, and produces a two's complement result. The product is provided in two halves with the sign bit replicated as the most significant bit of both halves. This facilitates use of the LMU08 product as a double precision operand in 8-bit systems. The LMU8U operates on unsigned data, producing an unsigned magnitude result.

Both the LMU08 and the LMU8U feature independently controlled registers for both inputs and the product, which along with three-state outputs allows easy interfacing with microprocessor busses. Provision is made in the LMU08 and LMU8U for proper rounding of the product to 8-bit precision. The round input is loaded at the rising edge of the logical OR of CLK A and CLK B for the LMU08. The LMU8U latches RND on the rising edge of CLK A only. In either case, a '1' is added in the most significant position of the lower product byte when RND is asserted. Subsequent truncation of the least significant product byte results in a correctly rounded 8-bit result.

LMU08/8U Block Diagram

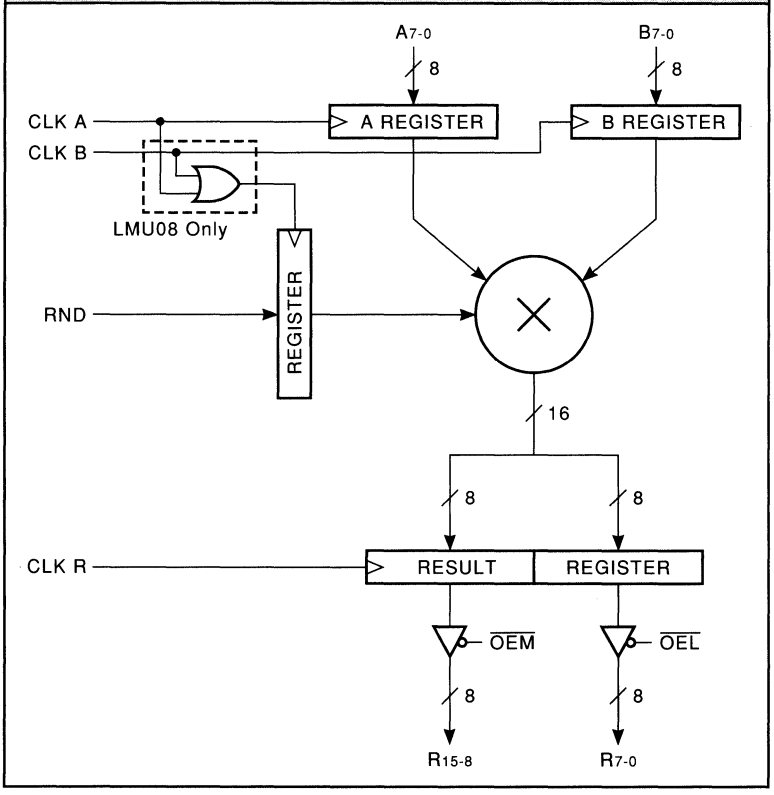


FIGURE 1A. INPUT FORMATS

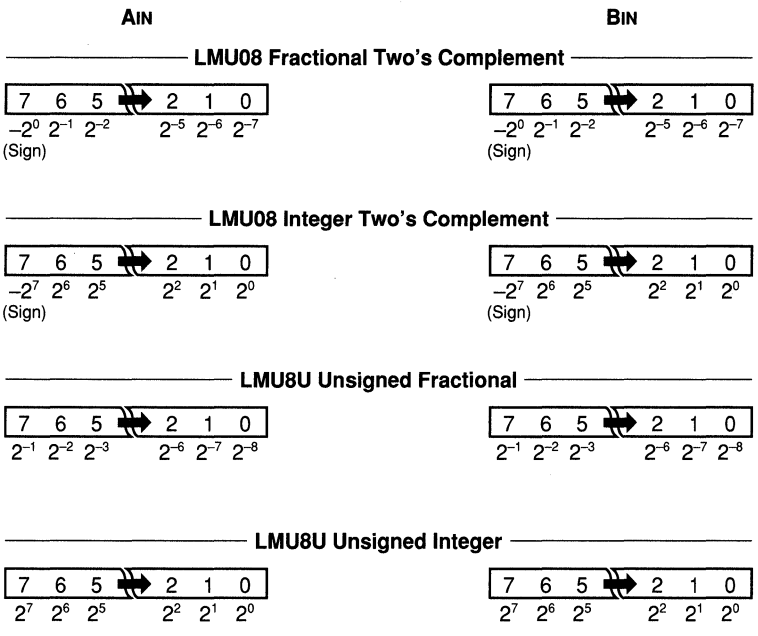
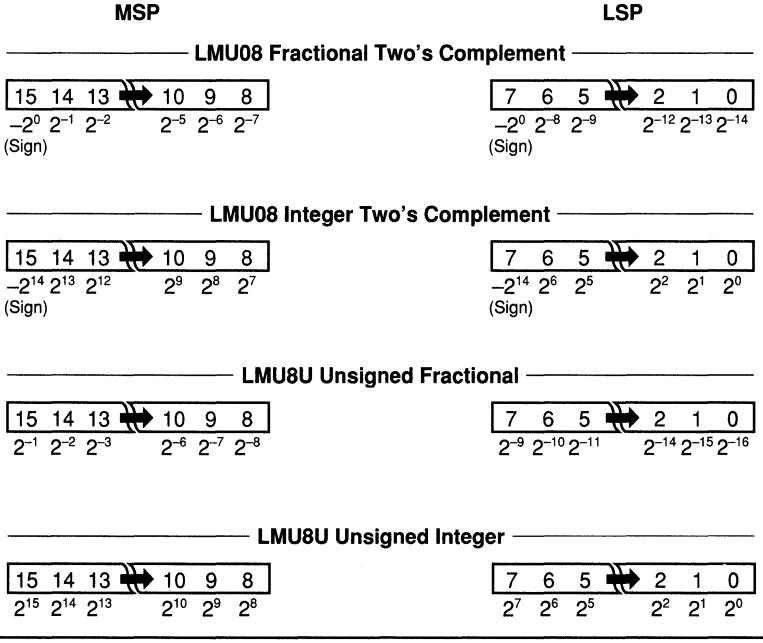


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		8	24	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

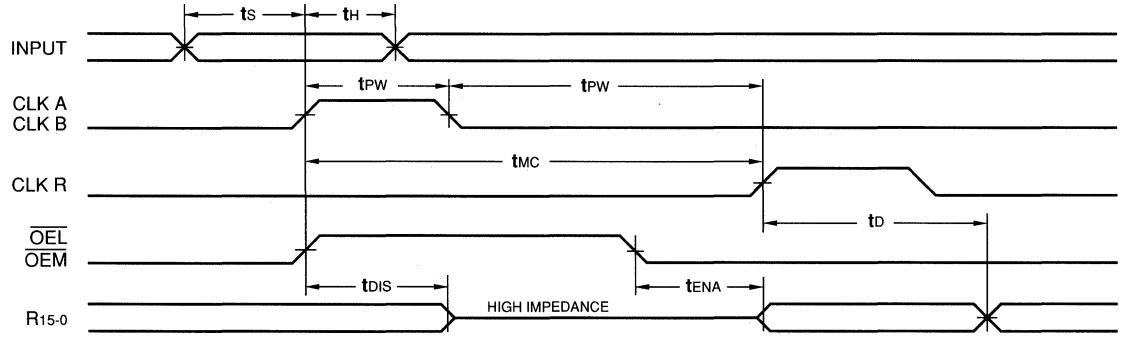
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU08/8U–					
		70		50		35	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		70		50		35
t_{PW}	Clock Pulse Width	20		20		10	
t_S	Input Register Setup Time	14		14		14	
t_H	Input Register Hold Time	4		0		0	
t_D	Output Delay		25		20		20
t_{ENA}	Three-State Output Enable Delay (Note 11)		24		22		22
t_{DIS}	Three-State Output Disable Delay (Note 11)		22		20		20

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU08/8U–					
		90		60		45	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		90		60		45
t_{PW}	Clock Pulse Width	25		20		15	
t_S	Input Register Setup Time	20		15		15	
t_H	Input Register Hold Time	5		0		0	
t_D	Output Delay		35		22		22
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		24		24
t_{DIS}	Three-State Output Disable Delay (Note 11)		35		22		22

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

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b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

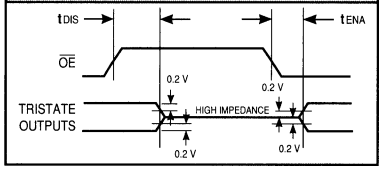
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

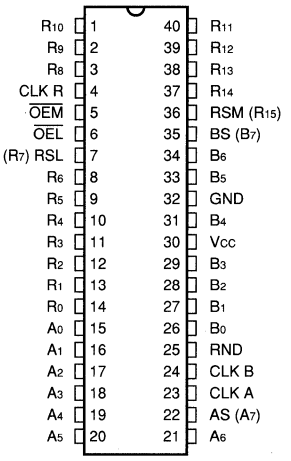
FIGURE 2. THRESHOLD LEVELS

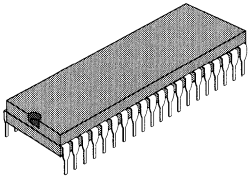


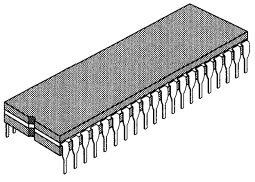
4

LMU08 — ORDERING INFORMATION

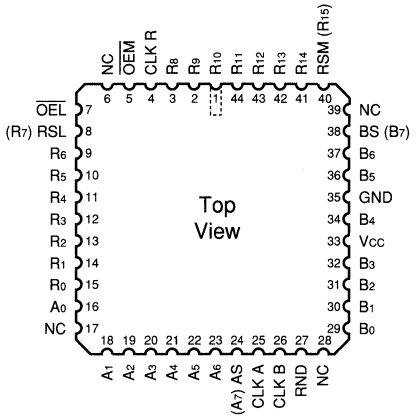
40-pin — 0.6" wide

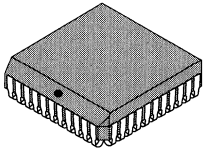


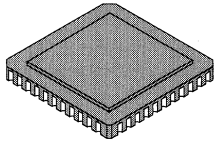




44-pin



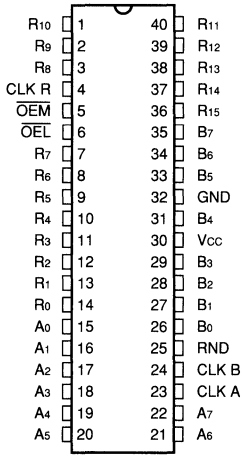


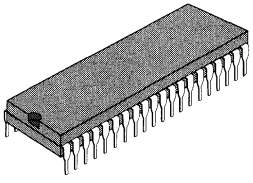


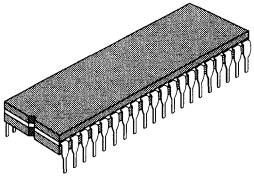
Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — COMMERCIAL SCREENING			
70 ns	LMU08PC70	LMU08CC70	LMU08JC70	LMU08KC70
50 ns	LMU08PC50	LMU08CC50	LMU08JC50	LMU08KC50
35 ns	LMU08PC35	LMU08CC35	LMU08JC35	LMU08KC35
	–55°C to +125°C — COMMERCIAL SCREENING			
90 ns		LMU08CM90		LMU08KM90
60 ns		LMU08CM60		LMU08KM60
45 ns		LMU08CM45		LMU08KM45
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
90 ns		LMU08CMB90		LMU08KMB90
60 ns		LMU08CMB60		LMU08KMB60
45 ns		LMU08CMB45		LMU08KMB45

LMU8U — ORDERING INFORMATION

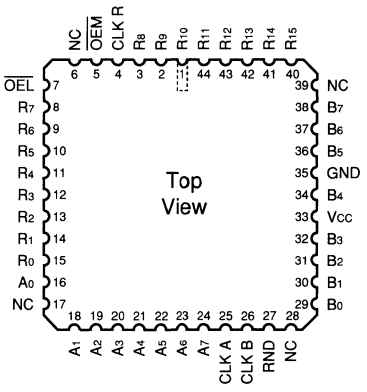
40-pin — 0.6" wide

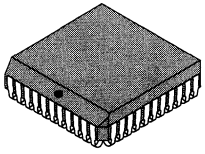


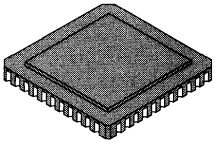




44-pin







Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — COMMERCIAL SCREENING			
70 ns	LMU8UPC70	LMU8UCC70	LMU8UJC70	LMU8UKC70
50 ns	LMU8UPC50	LMU8UCC50	LMU8UJC50	LMU8UKC50
35 ns	LMU8UPC35	LMU8UCC35	LMU8UJC35	LMU8UKC35
	–55°C to +125°C — COMMERCIAL SCREENING			
90 ns		LMU8UCM90		LMU8UKM90
60 ns		LMU8UCM60		LMU8UKM60
45 ns		LMU8UCM45		LMU8UKM45
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
90 ns		LMU8UCMB90		LMU8UKMB90
60 ns		LMU8UCMB60		LMU8UKMB60
45 ns		LMU8UCMB45		LMU8UKMB45

4

LMU557/558
8 x 8-bit Parallel Multiplier

FEATURES

- 60 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces Am25S557/558, 54S557/558
- Fully Combinatorial, No Clocks Required
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Ceramic DIP

DESCRIPTION

The **LMU557** and **LMU558** are high-speed, low power 8-bit parallel multipliers. They are pin for pin equivalents with 54S557 and 54S558 type multipliers. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

Both the LMU557 and LMU558 produce the 16-bit product of two 8-bit signed or unsigned numbers in a single unclocked operation. Assertion of control inputs TCA and TCB indicate that the corresponding input value is in two's complement notation.

Provision is made for proper rounding for any combination of signed or unsigned inputs. The RU input to the LMU558 causes the product to be rounded to 8 bits of precision for unsigned or mixed mode multiplication. For multiplication of two signed operands, the RS input is used for rounding, and the most significant bit of the product is discarded. [It will be identical to the sign bit for all except the $(-2^8)\bullet(-2^8)$ case, which will cause overflow if the result MSB is not considered.]

The LMU557 internally produces the RU and RS controls from a single round input, denoted R. With R asserted, RS rounding occurs if either TCA or TCB is asserted, while RU rounding is implemented for TCA and TCB not asserted. This implementation frees a pin for control of the transparent output latch in the LMU557 via the G input.

Both the LMU557 and LMU558 offer three-state output buffers controlled by the $\overline{OE}$ input. The LMU557 has a 16-bit transparent latch between the multiplier array and the output drivers for flexibility in implementing pipelined systems. This latch is transparent when G is HIGH, and holds its state when G is LOW. In addition, both polarities of the result MSB (R_{15}) are available as separate output pins to allow simple expansion to longer word lengths in signed multiplication.

LMU557/558 Block Diagram

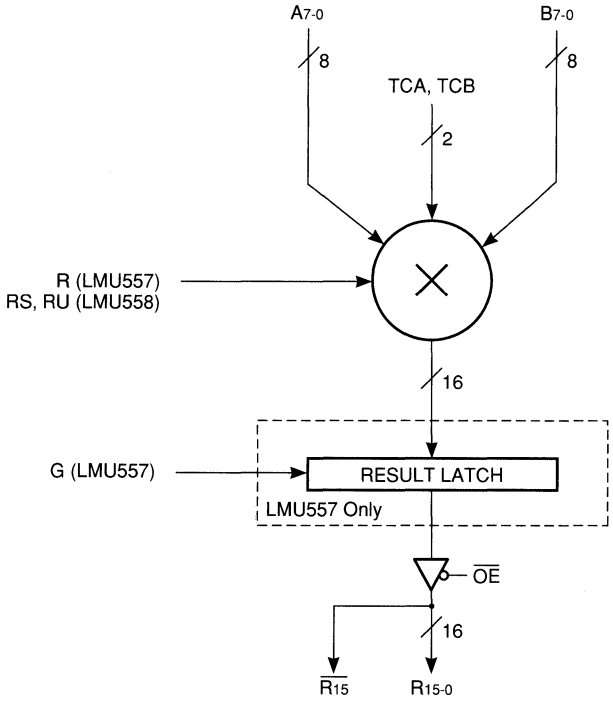


FIGURE 1A. INPUT FORMATS

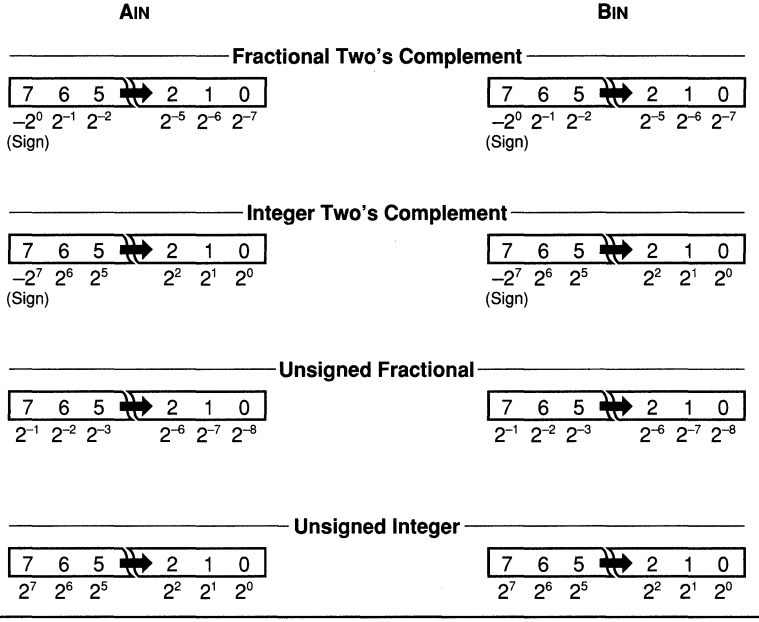
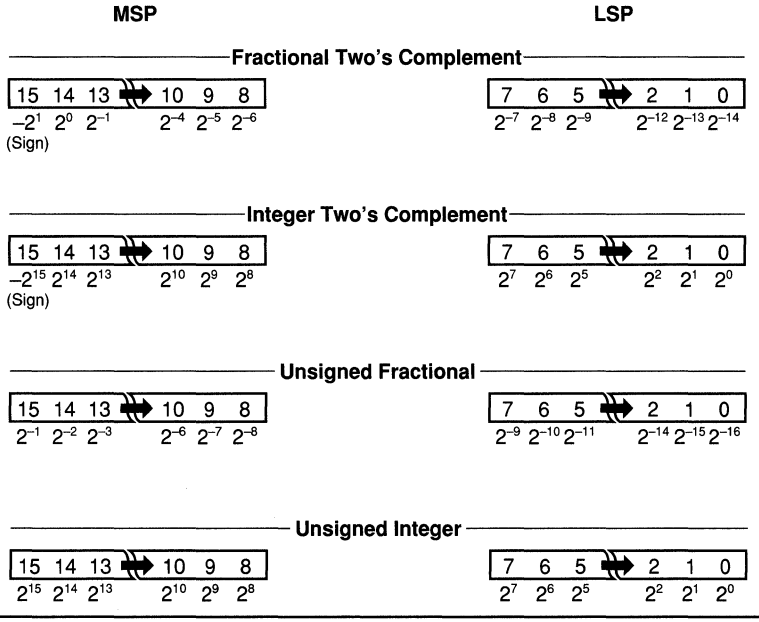


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		17	35	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

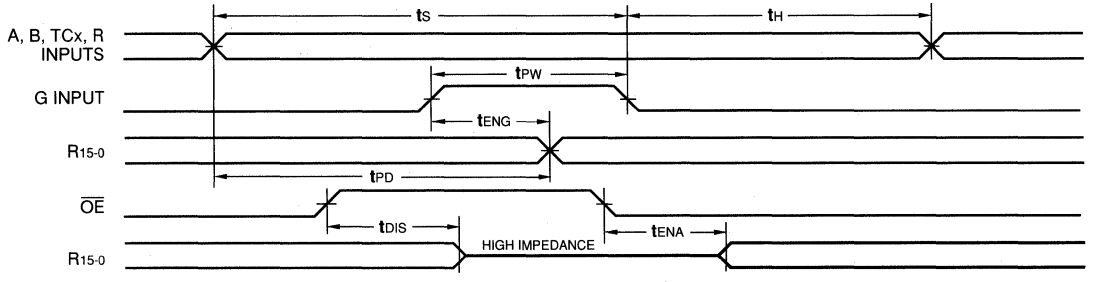
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMU557/558–60 Min	LMU557/558–60 Max
t_{PD}	A, B, TCx, R Inputs to R_{15-8}, $\overline{R_{15}}$		60
t_{PD}	A, B, TCx, R Inputs to R_{7-0}		55
t_{PW}	G Pulse Width	15	
t_S	A, B, TCx, R Inputs to G Setup Time	45	
t_H	G to A, B, TCx, R Hold Time	0	
t_{ENG}	G Enable to Result		30
t_{ENA}	Three-State Output Enable Delay (Note 11)		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		20

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	LMU557/558–70 Min	LMU557/558–70 Max
t_{PD}	A, B, TCx, R Inputs to R_{15-8}, $\overline{R_{15}}$		70
t_{PD}	A, B, TCx, R Inputs to R_{7-0}		60
t_{PW}	G Pulse Width	20	
t_S	A, B, TCx, R Inputs to G Setup Time	55	
t_H	G to A, B, TCx, R Hold Time	0	
t_{ENG}	G Enable to Result		35
t_{ENA}	Three-State Output Enable Delay (Note 11)		30
t_{DIS}	Three-State Output Disable Delay (Note 11)		25

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

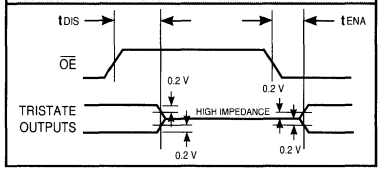
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

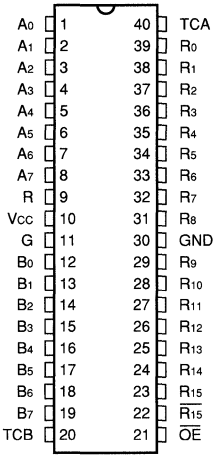
FIGURE 2. THRESHOLD LEVELS

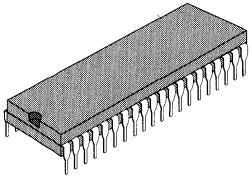


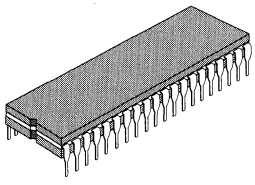
4

LMU557 — ORDERING INFORMATION

40-pin — 0.6" wide



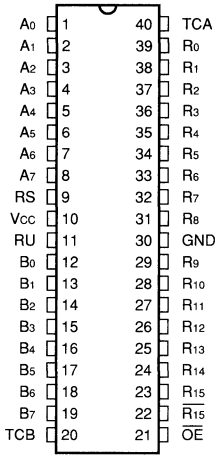


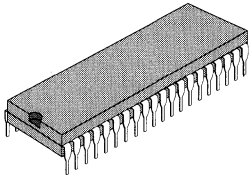


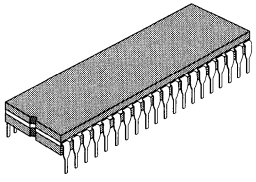
Speed	Plastic DIP (P3)	Ceramic DIP (C11)		
	0°C to +70°C — COMMERCIAL SCREENING			
60 ns	LMU557PC60	LMU557CC60		
	–55°C to +125°C — COMMERCIAL SCREENING			
70 ns		LMU557CM70		
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
70 ns		LMU557CMB70		

LMU558 — ORDERING INFORMATION

40-pin — 0.6" wide







Speed	Plastic DIP (P3)	Ceramic DIP (C11)		
	0°C to +70°C — Commercial Screening			
60 ns	LMU558PC60	LMU558CC60		
	–55°C to +125°C — Commercial Screening			
70 ns		LMU558CM70		
	–55°C to +125°C — MIL-STD-883 Compliant			
70 ns		LMU558CMB70		

LMU12
12 x 12-bit Parallel Multiplier

FEATURES

- 35 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces TRW MPY012H
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Commercial PGA
  - 68-pin Ceramic PGA

DESCRIPTION

The **LMU12** is a high-speed, low power 12-bit parallel multiplier. It is pin and functionally compatible with TRW MPY012H devices. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU12 produces the 24-bit product of two 12-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control bit are similarly loaded by CLK B.

The TCA and TCB controls specify the A and B operands as two's complement when HIGH, or unsigned magnitude when LOW.

RND is loaded on the rising edge of the logical OR of CLK A and CLK B. RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 12 least significant bits produces a result correctly rounded to 12-bit precision.

At the output, the Right Shift control (RS) selects either of two output formats. RS LOW produces a 23-bit product with a copy of the sign bit inserted in the MSB position of the least significant half. RS HIGH gives a full 24-bit product. Two 12-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK M and CLK L respectively. For asynchronous output, these registers may be made transparent by setting the feed through control (FT) HIGH.

LMU12 Block Diagram

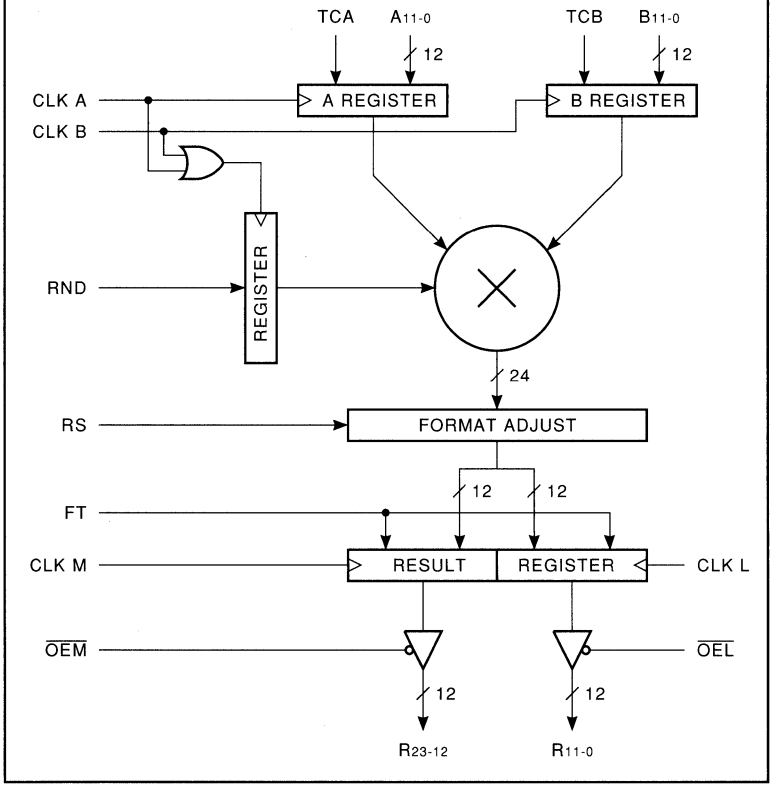


FIGURE 1A. INPUT FORMATS

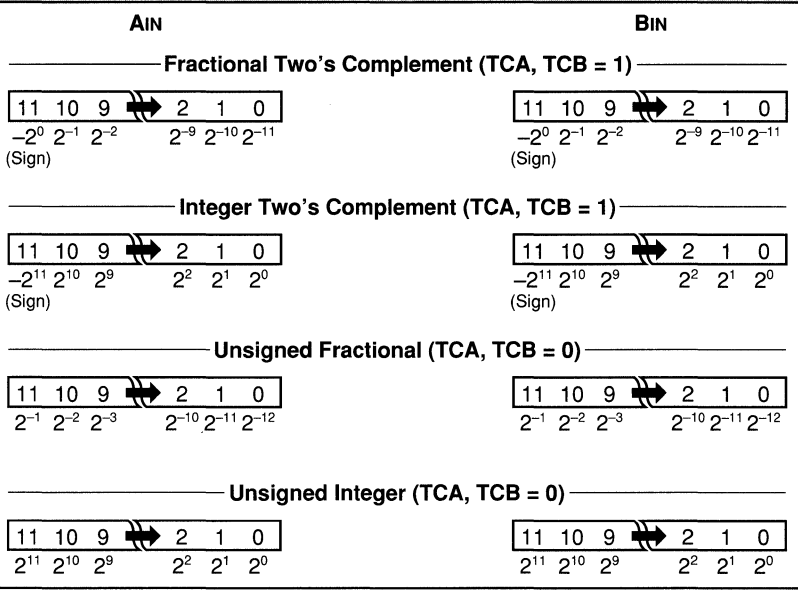
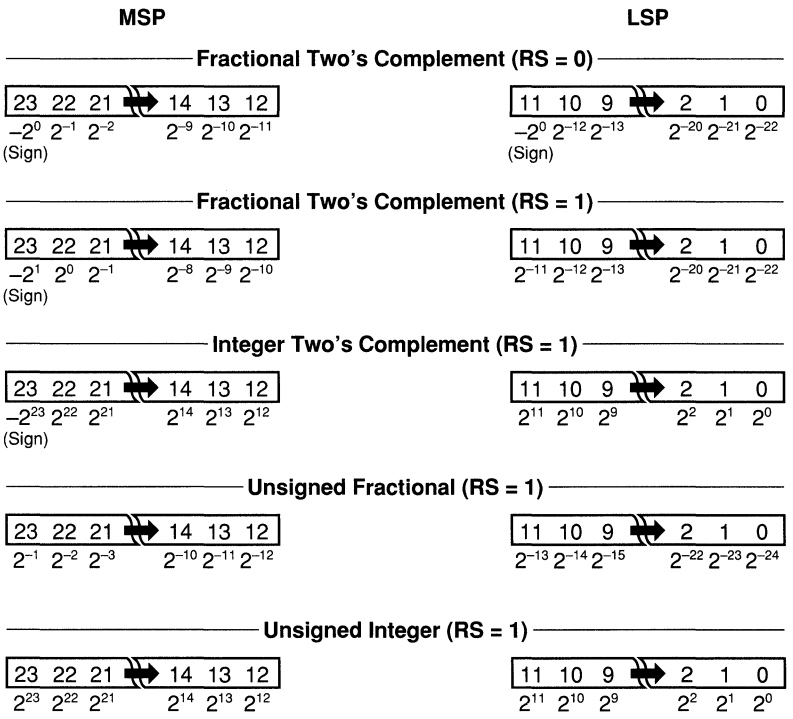


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

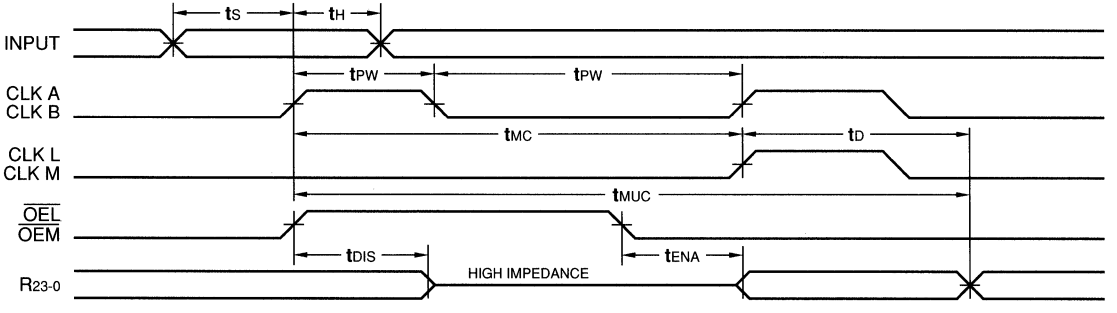
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU12–					
		65		45		35	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		45		35
t_{MUC}	Unclocked Multiply Time		95		65		55
t_{PW}	Clock Pulse Width	25		15		15	
t_S	Input Register Setup Time	18		15		12	
t_H	Input Register Hold Time	2		2		2	
t_D	Output Delay		26		25		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		22		22		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		20		18

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU12–					
		75		55		45	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		55		45
t_{MUC}	Unclocked Multiply Time		110		75		65
t_{PW}	Clock Pulse Width	25		20		15	
t_S	Input Register Setup Time	18		15		15	
t_H	Input Register Hold Time	2		2		2	
t_D	Output Delay		30		30		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		26		26		24
t_{DIS}	Three-State Output Disable Delay (Note 11)		24		24		22

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

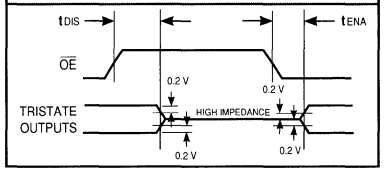
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

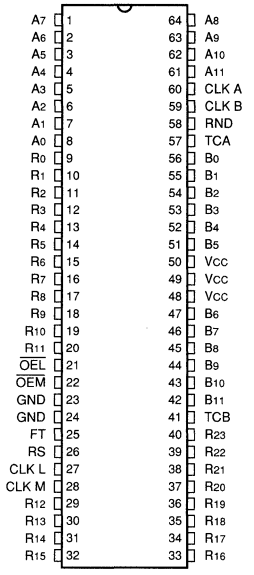
FIGURE 2. THRESHOLD LEVELS

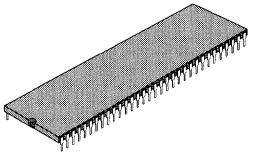


4

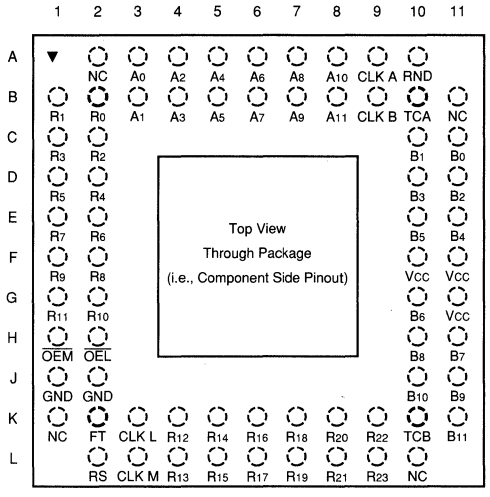
ORDERING INFORMATION

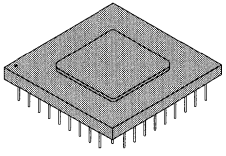
64-pin

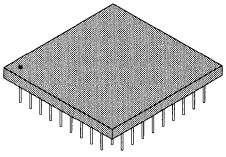




68-pin







Speed	Sidebraze Hermetic DIP (D6)	Commercial Pin Grid Array (E2)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — Commercial Screening		
65 ns	LMU12DC65	LMU12EC65	LMU12GC65
45 ns	LMU12DC45	LMU12EC45	LMU12GC45
35 ns	LMU12DC35	LMU12EC35	LMU12GC35
	–55°C to +125°C — Commercial Screening		
75 ns	LMU12DM75		LMU12GM75
55 ns	LMU12DM55		LMU12GM55
45 ns	LMU12DM45		LMU12GM45
	–55°C to +125°C — MIL-STD-883 Compliant		
75 ns	LMU12DMB75		LMU12GMB75
55 ns	LMU12DMB55		LMU12GMB55
45 ns	LMU12DMB45		LMU12GMB45

LMU112
12 x 12-bit Parallel Multiplier

FEATURES

- 50 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces TRW MPY112K
- Two's Complement or Unsigned Operands
- Three-State Outputs
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 52-pin Plastic LCC, J-Lead

DESCRIPTION

The **LMU112** is a high-speed, low power 12-bit parallel multiplier built using advanced CMOS technology. The LMU112 is pin and functionally compatible with TRW's MPY112K.

The A and B input operands are loaded into their respective registers on the rising edge of the separate clock inputs (CLK A and CLK B). Two's complement or unsigned magnitude operands are accommodated via the operand control bit (TC) which is loaded along with the B operands. The operands are specified to be in two's complement format when TC is asserted and unsigned magnitude when TC is deasserted. Mixed mode operation is not allowed.

For two's complement operands, the 17 most significant bits at the output of the asynchronous multiplier array are shifted one bit position to the left. This is done to discard the redundant copy of the sign-bit, which is in the most significant bit position, and extend the bit precision by one bit. The result is then truncated to the 16 MSB's and loaded into the output register on the rising edge of CLK B.

The contents of the output register are made available via three-state buffers by asserting $\overline{OE}$. When $\overline{OE}$ is de-asserted, the outputs (R_{23-8}) are in the high impedance state.

4

LMU112 Block Diagram

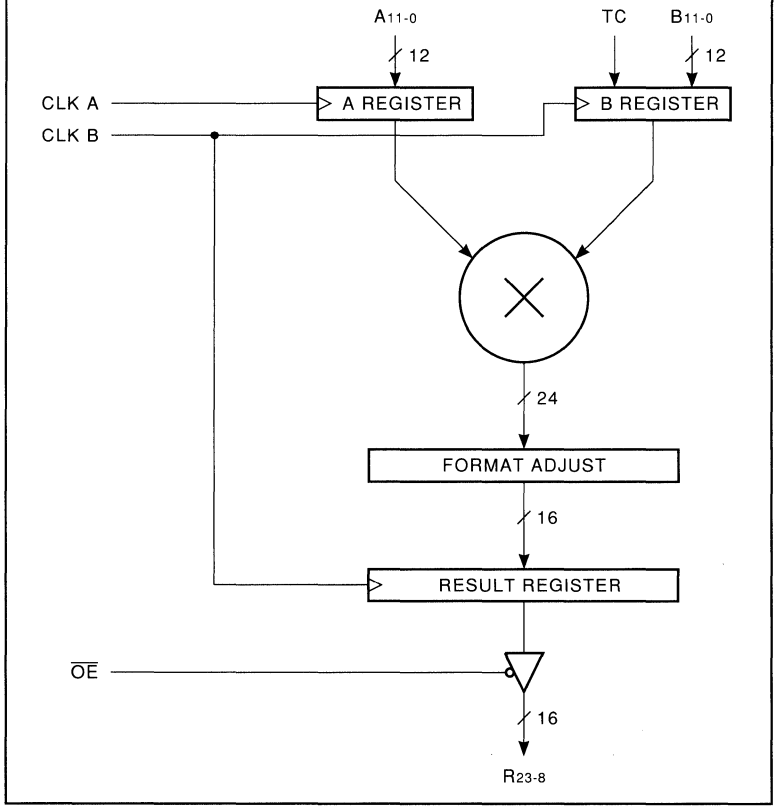


FIGURE 1A. INPUT FORMATS

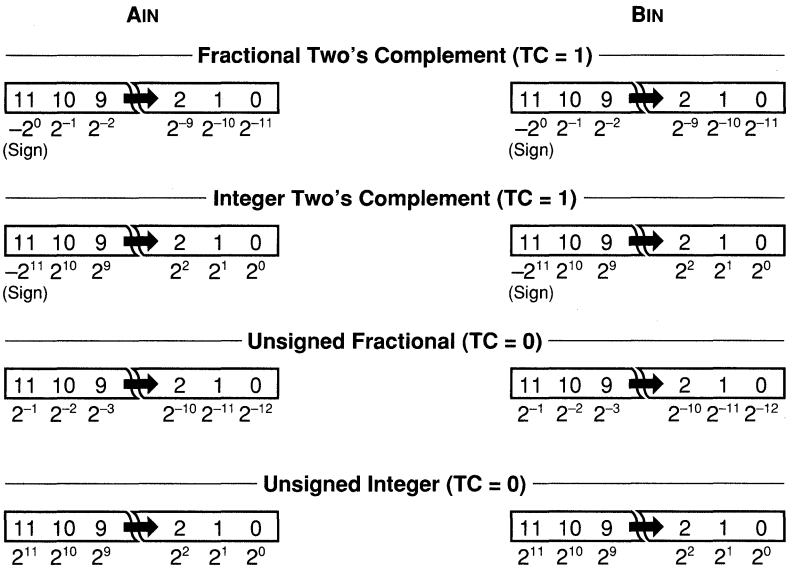
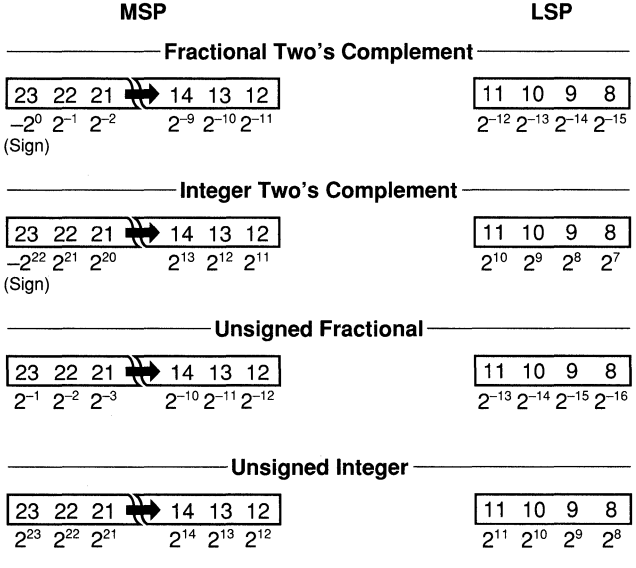


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

4

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	20	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

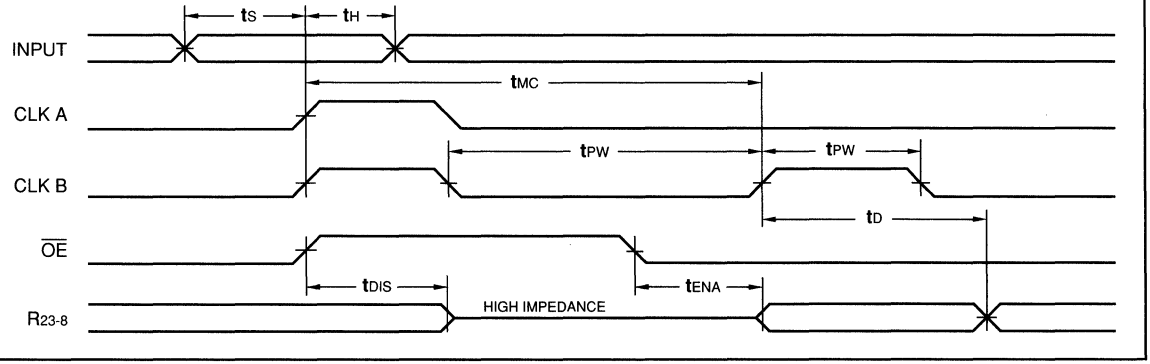
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU112–			
		60		50	
Symbol	Parameter	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		60		50
t_{PW}	Clock Pulse Width	15		15	
t_S	Input Register Setup Time	15		15	
t_H	Input Register Hold Time	3		3	
t_D	Output Delay		25		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU112–			
		65		55	
Symbol	Parameter	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		55
t_{PW}	Clock Pulse Width	20		20	
t_S	Input Register Setup Time	15		15	
t_H	Input Register Hold Time	3		3	
t_D	Output Delay		30		30
t_{ENA}	Three-State Output Enable Delay (Note 11)		30		30
t_{DIS}	Three-State Output Disable Delay (Note 11)		30		30

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

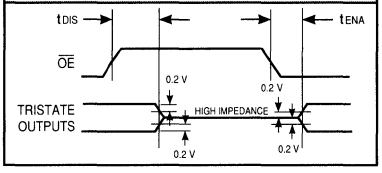
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

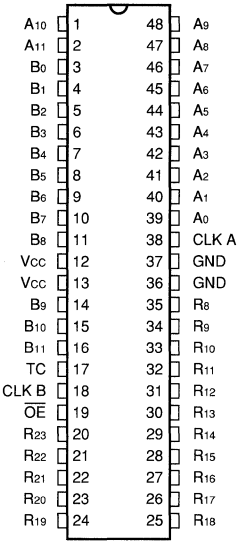
FIGURE 2. THRESHOLD LEVELS

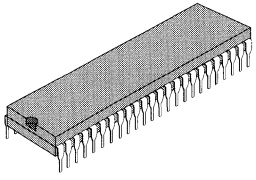


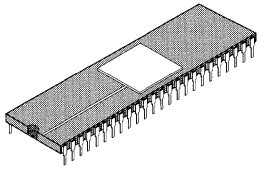
4

ORDERING INFORMATION

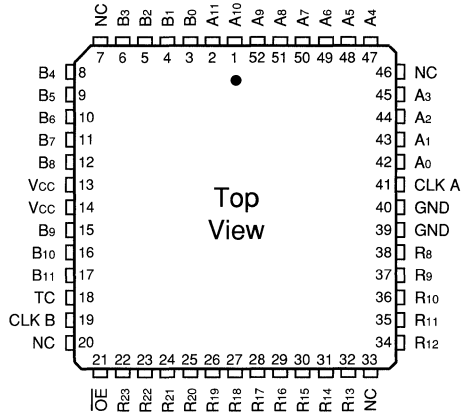
48-pin

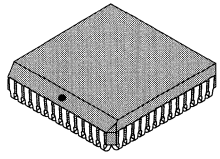






52-pin





Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic J-Lead Chip Carrier (J5)
	0°C to +70°C — Commercial Screening		
60 ns	LMU112PC60	LMU112DC60	LMU112JC60
50 ns	LMU112PC50	LMU112DC50	LMU112JC50
	–55°C to +125°C — Commercial Screening		
65 ns		LMU112DM65	
55 ns		LMU112DM55	
	–55°C to +125°C — MIL-STD-883 Compliant		
65 ns		LMU112DMB65	
55 ns		LMU112DMB55	

LMU16/216
16 x 16-bit Parallel Multiplier

FEATURES

- 45 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces TRW MPY016/TMC216, Cypress CY7C516, IDT 7216L, and AMD Am29516
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- DESC SMD No. 5962-86873
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Commercial PGA
  - 68-pin Ceramic PGA
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC

DESCRIPTION

The **LMU16** and **LMU216** are high-speed, low power 16-bit parallel multipliers. The LMU16 and LMU216 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU16 and LMU216 produce the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK A. B data and the TCB control bit are similarly loaded by CLK B. The TCA and TCB controls specify the A and B operands as two's complement when HIGH, or unsigned magnitude when LOW.

RND is loaded on the rising edge of the logical OR of CLK A and CLK B. RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the Right Shift control (RS) selects either of two output formats. RS LOW produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS HIGH gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK M and CLK L respectively. For asynchronous output, these registers may be made transparent by setting the feed through control (FT) HIGH.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{\text{MSPSEL}}$ LOW causes the MSP outputs to be driven by the most significant half of the result. $\overline{\text{MSPSEL}}$ HIGH routes the least significant half of the result to the MSP outputs. In addition, the LSP is available via the B port through a separate three-state buffer.

The output multiplexer control $\overline{\text{MSPSEL}}$ uses a pin which is a supply ground in the TRW MPY016H/TMC216H. When this control is LOW (GND), the function is that of the MPY016H/TMC216H, thus allowing full compatibility.

LMU16/216 BLOCK DIAGRAM

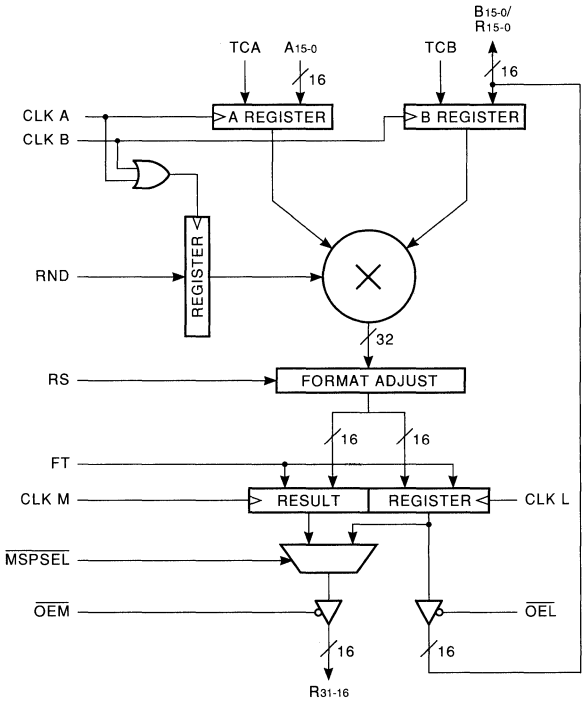


FIGURE 1A. INPUT FORMATS

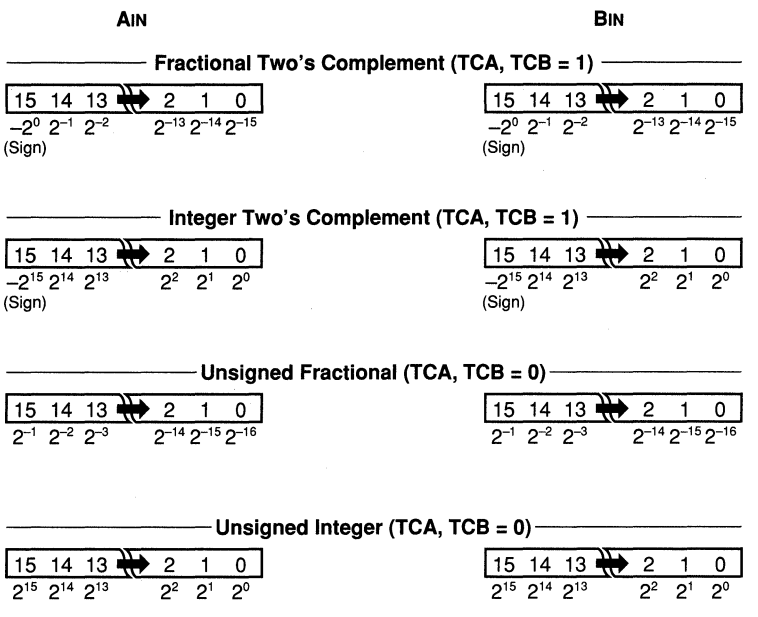
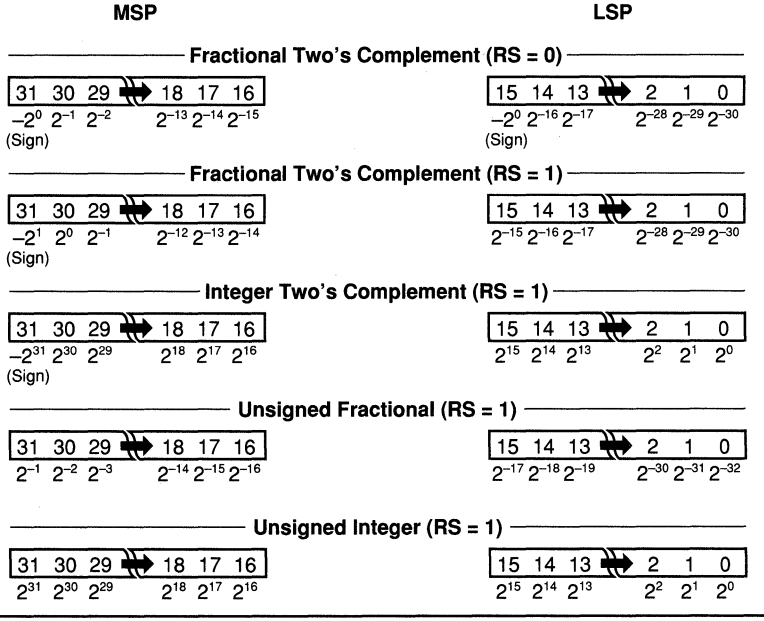


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

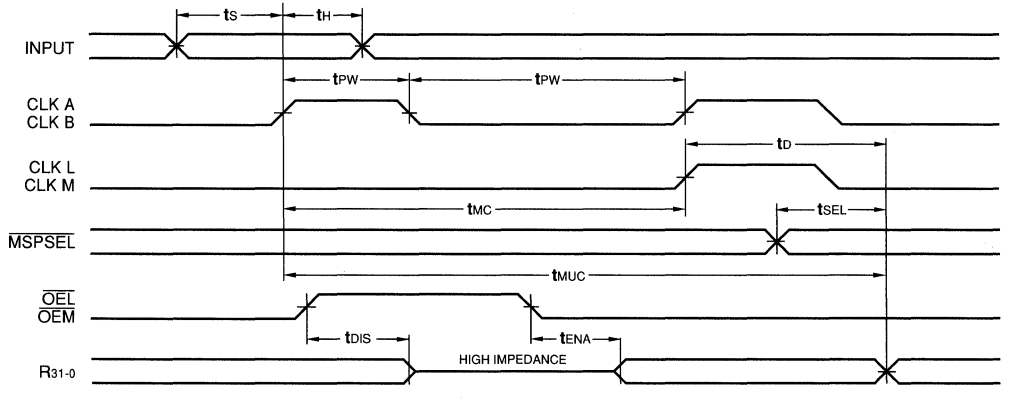
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU16/216–					
		65		55		45	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{MC}	Clocked Multiply Time		65		55		45
t_{MUC}	Unclocked Multiply Time		85		75		65
t_{PW}	Clock Pulse Width	15		15		15	
t_S	Input Setup Time	15		15		15	
t_H	Input Hold Time	1		1		1	
t_D	Output Delay		30		30		30
t_{SEL}	Output Select Delay		25		25		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU16/216–					
		75		65		55	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{MC}	Clocked Multiply Time		75		65		55
t_{MUC}	Unclocked Multiply Time		95		85		75
t_{PW}	Clock Pulse Width	20		15		15	
t_S	Input Setup Time	15		15		15	
t_H	Input Hold Time	2		2		2	
t_D	Output Delay		35		30		30
t_{SEL}	Output Select Delay		30		30		30
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

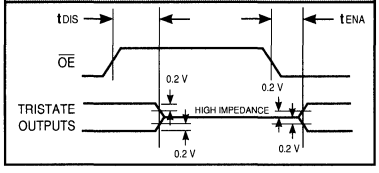
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

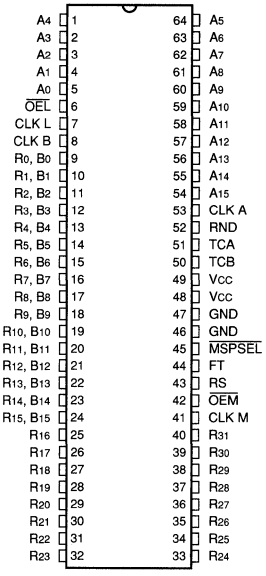
FIGURE 2. THRESHOLD LEVELS

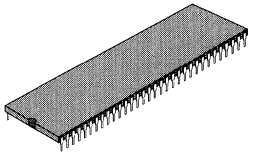


4

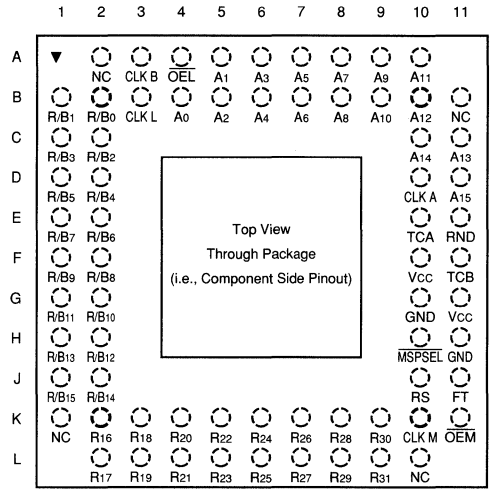
LMU16 — ORDERING INFORMATION

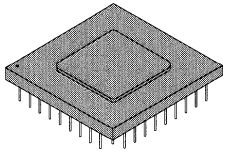
64-pin

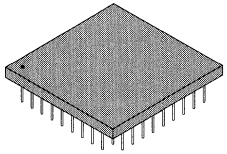




68-pin



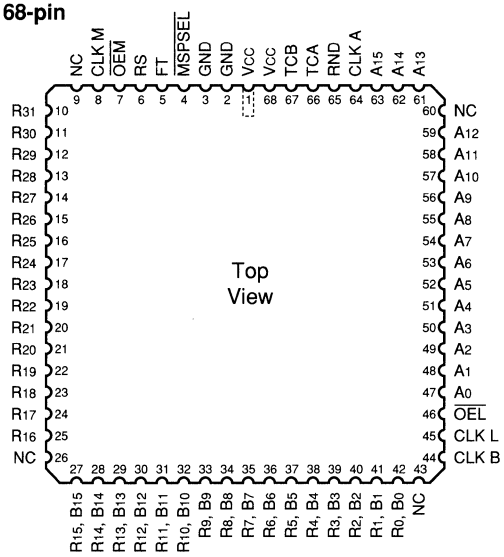


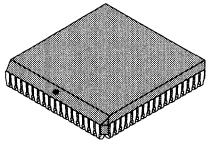


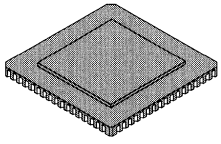
Speed	Sidebraze Hermetic DIP (D6)	Commercial Pin Grid Array (E2)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — COMMERCIAL SCREENING		
65 ns	LMU16DC65	LMU16EC65	LMU16GC65
55 ns	LMU16DC55	LMU16EC55	LMU16GC55
45 ns	LMU16DC45	LMU16EC45	LMU16GC45
	–55°C to +125°C — COMMERCIAL SCREENING		
75 ns	LMU16DM75		LMU16GM75
65 ns	LMU16DM65		LMU16GM65
55 ns	LMU16DM55		LMU16GM55
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
75 ns	LMU16DMB75		LMU16GMB75
65 ns	LMU16DMB65		LMU16GMB65
55 ns	LMU16DMB55		LMU16GMB55

LMU216 — ORDERING INFORMATION

68-pin







Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
	0°C to +70°C — COMMERCIAL SCREENING			
65 ns	LMU216JC65	LMU216KC65		
55 ns	LMU216JC55	LMU216KC55		
45 ns	LMU216JC45	LMU216KC45		
	–55°C to +125°C — COMMERCIAL SCREENING			
75 ns		LMU216KM75		
65 ns		LMU216KM65		
55 ns		LMU216KM55		
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
75 ns		LMU216KMB75		
65 ns		LMU216KMB65		
55 ns		LMU216KMB55		

4

LMU17/217
16 x 16-bit Parallel multiplier

FEATURES

- 45 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Replaces Cypress CY7C517, IDT 7217L, and AMD Am29517
- Single Clock Architecture with Register Enables
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- DESC SMD No. 5962-87686
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic PGA
  - 68-pin Ceramic LCC

DESCRIPTION

The **LMU17** and **LMU217** are high-speed, low power 16-bit parallel multipliers. The LMU17 and LMU217 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU17 and LMU217 produce the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK. B data and the TCB control bit are similarly loaded. Loading of the A and B registers is controlled by the $\overline{ENA}$ and $\overline{ENB}$ controls. When HIGH, these controls prevent application of the clock to the respective register. The TCA and TCB controls specify the operands as two's complement when HIGH, or unsigned magnitude when LOW.

RND is loaded on the rising edge of CLK, provided either $\overline{ENA}$ or $\overline{ENB}$ are LOW. RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the Right Shift control (RS) selects either of two output formats. RS LOW produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS HIGH gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK, subject to the $\overline{ENR}$ control. When $\overline{ENR}$ is HIGH, clocking of the result registers is prevented. For asynchronous output, these registers may be made transparent by setting the feed through control (FT) HIGH.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{MSPSEL}$ LOW causes the MSP outputs to be driven by the most significant half of the result. $\overline{MSPSEL}$ HIGH routes the least significant half of the result to the MSP pins. In addition, the LSP is available via the B port through a separate three-state buffer.

LMU17/217 Block Diagram

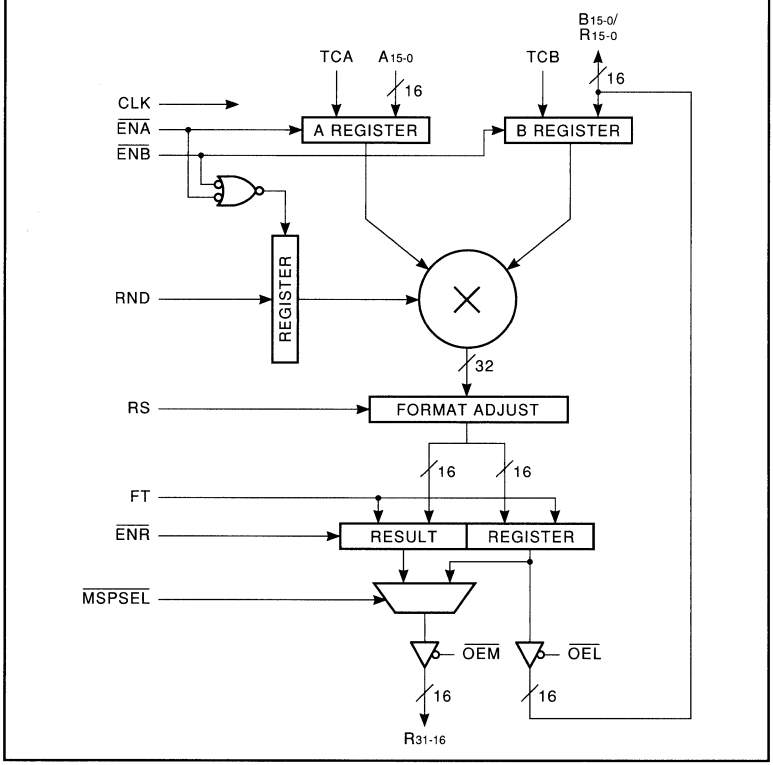


FIGURE 1A. INPUT FORMATS

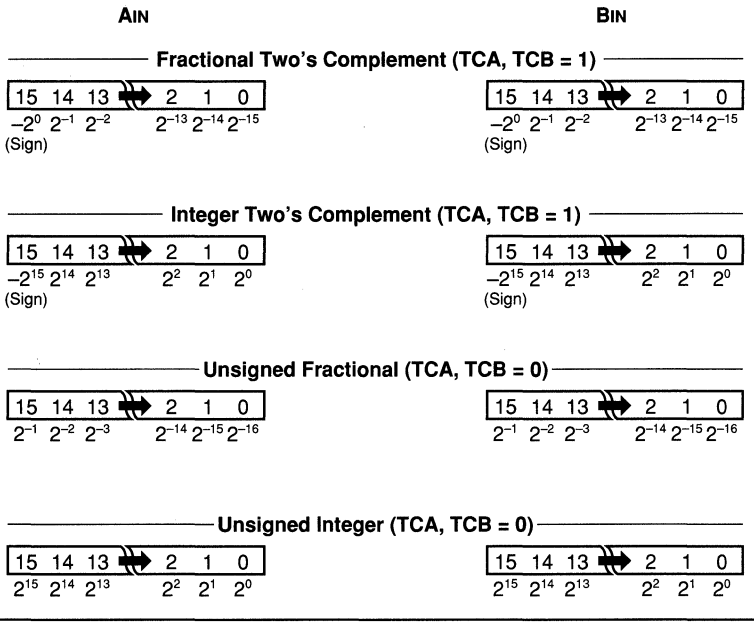
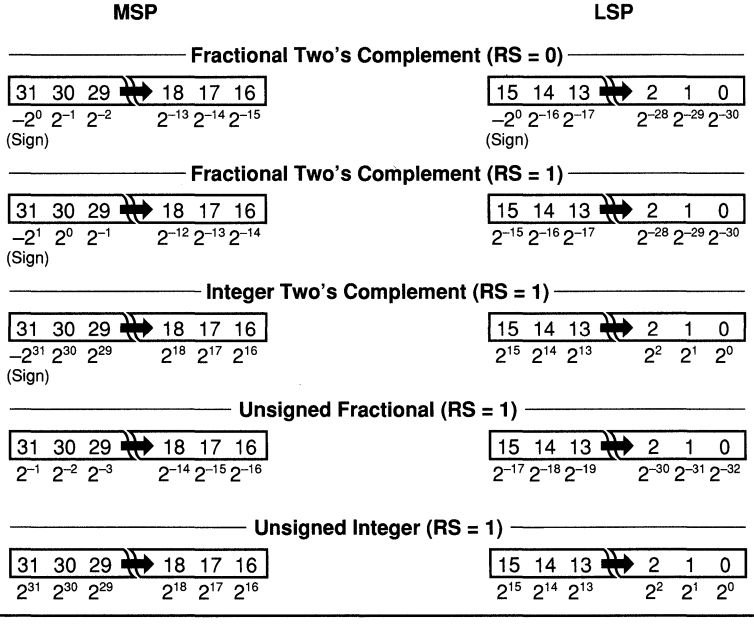


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

4

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

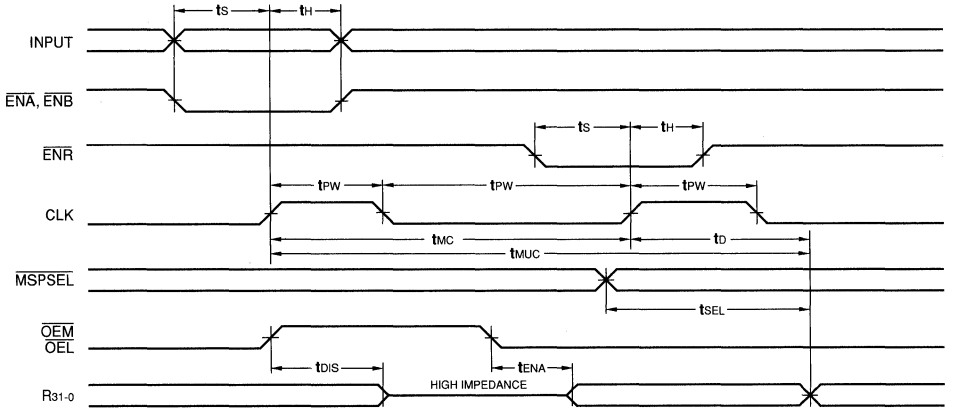
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU17/217–					
		65		55		45	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{MC}	Clocked Multiply Time		65		55		45
t_{MUC}	Unclocked Multiply Time		85		75		65
t_{PW}	Clock Pulse Width	15		15		15	
t_S	Input Setup Time	15		15		15	
t_H	Input Hold Time	3		3		3	
t_D	Output Delay		30		30		30
t_{SEL}	Output Select Delay		25		25		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU17/217–					
		75		65		55	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{MC}	Clocked Multiply Time		75		65		55
t_{MUC}	Unclocked Multiply Time		95		85		75
t_{PW}	Clock Pulse Width	20		15		15	
t_S	Input Setup Time	15		15		15	
t_H	Input Hold Time	3		3		3	
t_D	Output Delay		35		30		30
t_{SEL}	Output Select Delay		30		30		30
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

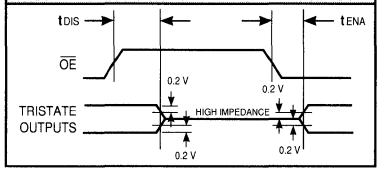
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

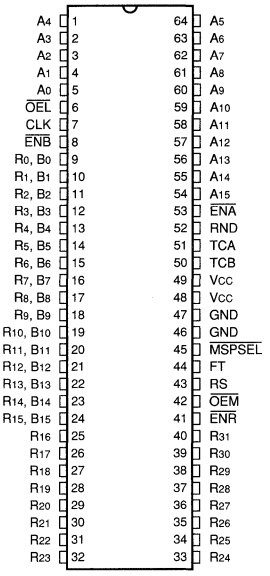
FIGURE 2. THRESHOLD LEVELS

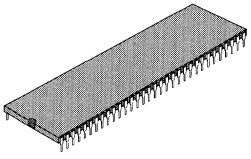


4

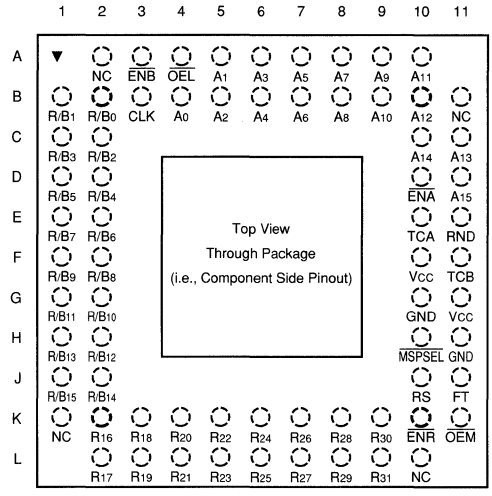
LMU17 — ORDERING INFORMATION

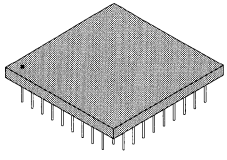
64-pin





68-pin

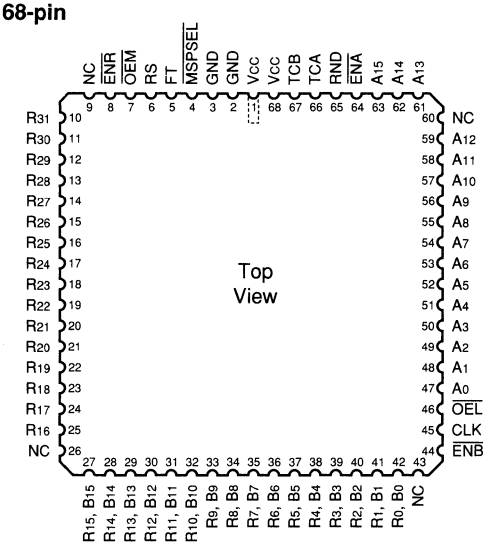


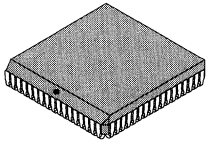


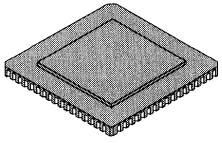
Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — COMMERCIAL SCREENING	
65 ns	LMU17DC65	LMU17GC65
55 ns	LMU17DC55	LMU17GC55
45 ns	LMU17DC45	LMU17GC45
	–55°C to +125°C — COMMERCIAL SCREENING	
75 ns	LMU17DM75	LMU17GM75
65 ns	LMU17DM65	LMU17GM65
55 ns	LMU17DM55	LMU17GM55
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
75 ns	LMU17DMB75	LMU17GMB75
65 ns	LMU17DMB65	LMU17GMB65
55 ns	LMU17DMB55	LMU17GMB55

LMU217 — ORDERING INFORMATION

68-pin







Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
	0°C to +70°C — COMMERCIAL SCREENING			
65 ns	LMU217JC65	LMU217KC65		
55 ns	LMU217JC55	LMU217KC55		
45 ns	LMU217JC45	LMU217KC45		
	–55°C to +125°C — COMMERCIAL SCREENING			
75 ns		LMU217KM75		
65 ns		LMU217KM65		
55 ns		LMU217KM55		
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
75 ns		LMU217KMB75		
65 ns		LMU217KMB65		
55 ns		LMU217KMB55		

4

LMU18
16 x 16-bit Parallel Multiplier

FEATURES

- 35 ns Worst-Case Multiply Time
- Low Power CMOS Technology
- Full 32-bit Output Port — No Multiplexing Required
- Two's Complement, Unsigned, or Mixed Operands
- Three-State Outputs
- DESC SMD No. 5962-94523
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 84-pin Ceramic PGA

DESCRIPTION

The **LMU18** is a high-speed, low power 16-bit parallel multiplier. The LMU18 is an 84-pin device which provides simultaneous access to all outputs. Full military ambient temperature range operation is attained by the use of advanced CMOS technology.

The LMU18 produces the 32-bit product of two 16-bit numbers. Data present at the A inputs, along with the TCA control bit, is loaded into the A register on the rising edge of CLK. B data and the TCB control bit are similarly loaded. Loading of the A and B registers is controlled by the $\overline{ENA}$ and $\overline{ENB}$ controls. When HIGH, these controls prevent application of the clock to the respective register. The TCA and TCB controls specify the operands as two's complement when HIGH, or unsigned magnitude when LOW.

RND is loaded on the rising edge of CLK, providing either $\overline{ENA}$ or $\overline{ENB}$ are LOW. RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

At the output, the Right Shift control (RS) selects either of two output formats. RS LOW produces a 31-bit product with a copy of the sign bit inserted in the MSB postion of the least significant half. RS HIGH gives a full 32-bit product. Two 16-bit output registers are provided to hold the most and least significant halves of the result (MSP and LSP) as defined by RS. These registers are loaded on the rising edge of CLK, subject to the $\overline{ENR}$ control. When $\overline{ENR}$ is HIGH, clocking of the result registers is prevented. For asynchronous output these registers may be made transparent by setting the feed through control (FT) HIGH.

The two halves of the product may be routed to a single 16-bit three-state output port (MSP) via a multiplexer. $\overline{MSPSEL}$ LOW causes the MSP outputs to be driven by the most significant half of the result. $\overline{MSPSEL}$ HIGH routes the least significant half of the result to the MSP pins. The MSB of the result is available in both true and complemented form to aid implementation of higher precision multipliers.

LMU18 Block Diagram

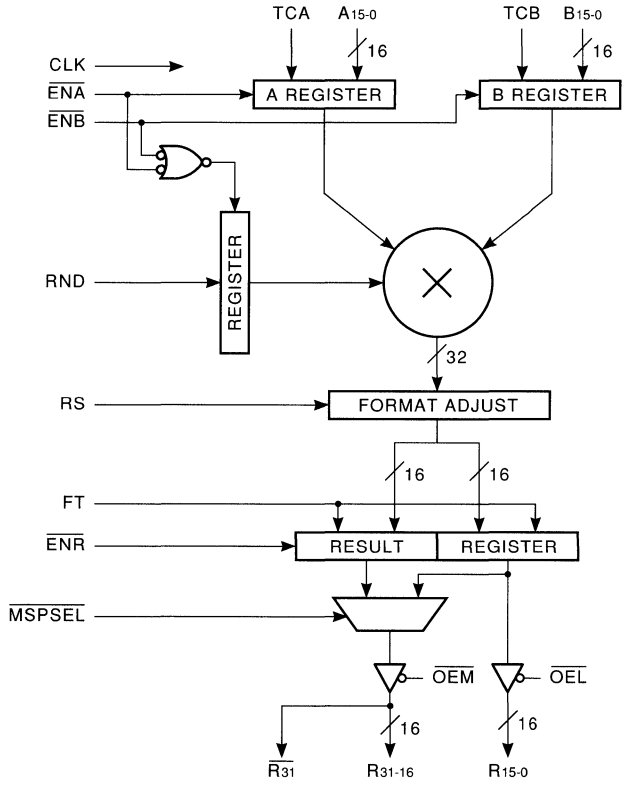


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FIGURE 1A. INPUT FORMATS

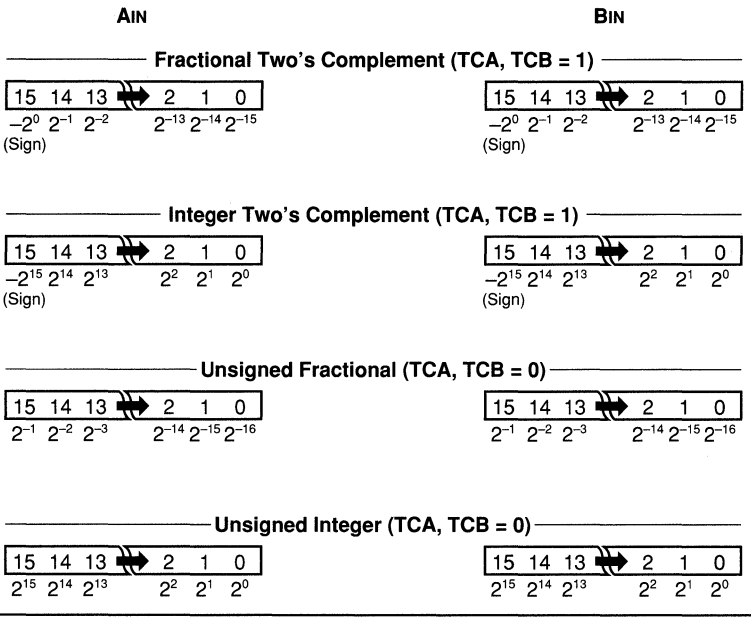
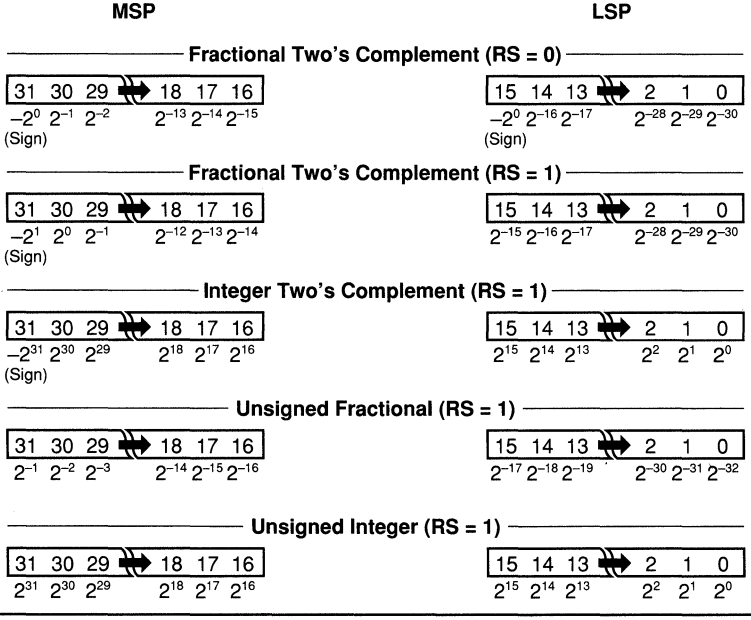


FIGURE 1B. INPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		25	45	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

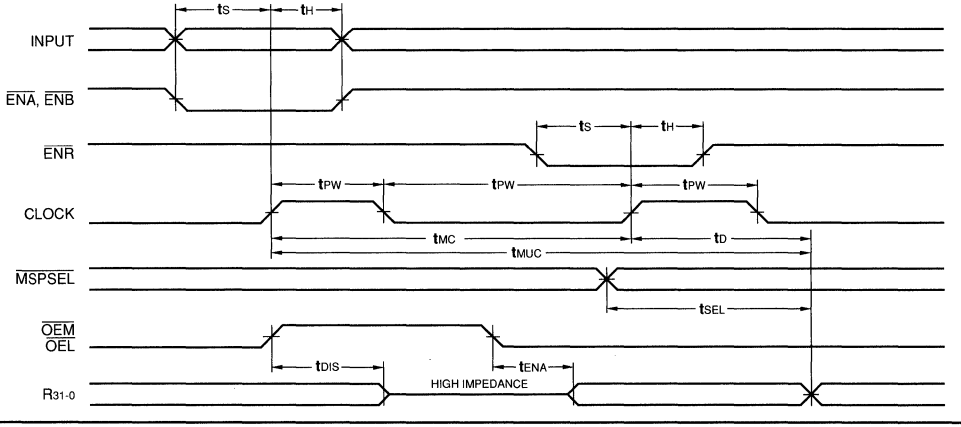
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMU18–					
		65		45		35	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		45		35
t_{MUC}	Unclocked Multiply Time		85		65		55
t_{PW}	Clock Pulse Width	15		15		15	
t_S	Input Setup Time	15		15		12	
t_H	Input Hold Time	5		5		5	
t_D	Output Delay		30		30		28
t_{SEL}	Output Select Delay		25		25		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		20		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		24		20		20

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMU18–					
		75		55		45	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		55		45
t_{MUC}	Unclocked Multiply Time		95		85		65
t_{PW}	Clock Pulse Width	20		15		15	
t_S	Input Setup Time	15		15		12	
t_H	Input Hold Time	5		5		5	
t_D	Output Delay		35		35		33
t_{SEL}	Output Select Delay		30		30		30
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		20		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		24		20		20

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

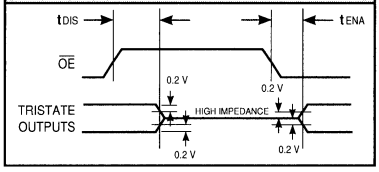
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 2. THRESHOLD LEVELS



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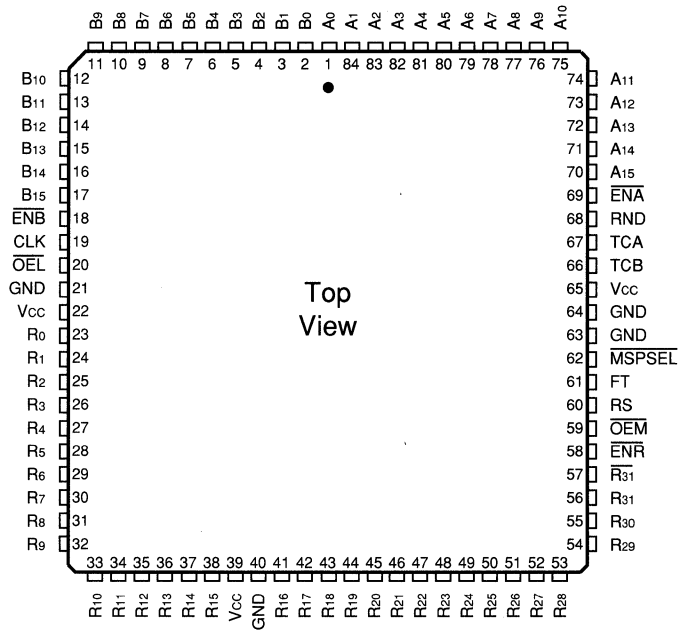
ORDERING INFORMATION

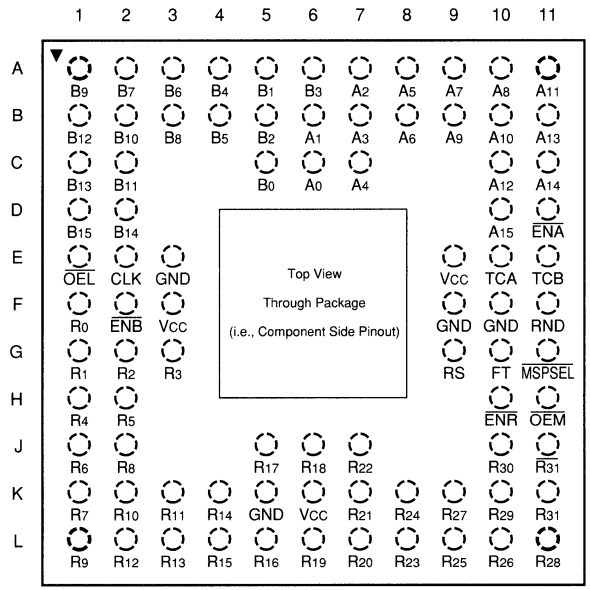
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
65 ns	LMU18JC65
45 ns	LMU18JC45
35 ns	LMU18JC35
	–55°C to +125°C — COMMERCIAL SCREENING
75 ns	
55 ns	
45 ns	
	–55°C to +125°C — MIL-STD-883 COMPLIANT
75 ns	
55 ns	
45 ns	

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — Commercial Screening
65 ns	LMU18GC65
45 ns	LMU18GC45
35 ns	LMU18GC35
	–55°C to +125°C — Commercial Screening
75 ns	LMU18GM75
55 ns	LMU18GM55
45 ns	LMU18GM45
	–55°C to +125°C — MIL-STD-883 Compliant
75 ns	LMU18GMB75
55 ns	LMU18GMB55
45 ns	LMU18GMB45

LMA1009/2009
12 x 12-bit Multiplier-Accumulator

FEATURES

- 45 ns Multiply-Accumulate Time
- Low Power CMOS Technology
- Replaces TRW TDC1009/TMC2009
- Two's Complement or Unsigned Operands
- Accumulator Performs Preload, Accumulate, and Subtract
- Three-State Outputs
- DESC SMD No. 5962-90996
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Ceramic PGA
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC

DESCRIPTION

The **LMA1009** and **LMA2009** are high-speed, low power 12-bit multiplier-accumulators. They are pin-for-pin equivalent to the TRW TDC1009/TMC2009 multiplier-accumulators. The LMA1009 and LMA2009 are functionally identical; they differ only in packaging. Full ambient temperature range operation is achieved by the use of advanced CMOS technology.

The LMA1009/2009 produces the 24-bit product of two 12-bit numbers. The results of a series of multiplications may be accumulated to form the sum of products. Accumulation is performed to 27-bit precision with the multiplier product sign extended as appropriate.

Data present at the A and B input registers is latched on the rising edges of CLK A and CLK B respectively. RND, TC, ACC, and SUB controls are latched on the rising edge of the logical OR of CLK A and CLK B. TC specifies the input as two's complement (TC HIGH) or unsigned magnitude (TC LOW). RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 12 least significant bits produces a result correctly rounded to 12-bit precision.

The ACC and SUB inputs control accumulator operation. ACC HIGH results in addition of the multiplier product and the accumulator contents, with the result stored in the accumulator register on the rising edge of CLK R. ACC and SUB HIGH results in subtraction of the accumulator contents from the multiplier product, with the result stored in the accumulator register. With ACC LOW, no accumulation occurs and the next product is loaded directly into the accumulator register.

The LMA1009/2009 output register (accumulator register) is divided into three independently controlled sections. The least significant result (LSR) and most significant result (MSR) registers are 12 bits in length. The extended result register (XTR) is 3 bits long.

Each output register has an independent output enable control. In addition to providing control of the three-state output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are HIGH and PREL is HIGH, data can be preloaded via the bidirectional output pins into the respective output registers. Data present on the output pins is latched on the rising edge of CLK R. The interrelation of PREL and the enable controls is summarized in Table 1.

LMA1009/2009 Block Diagram

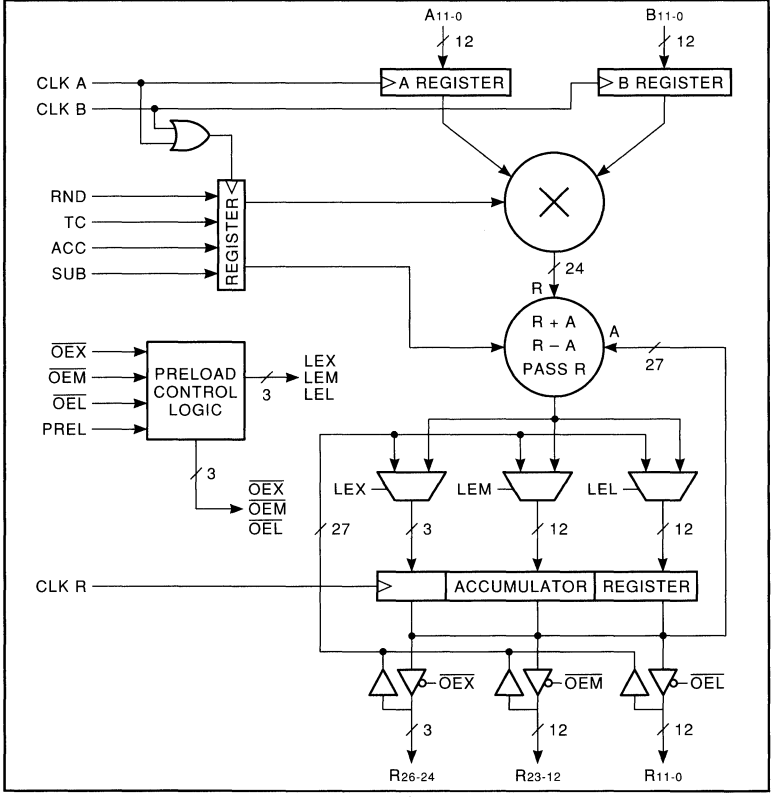


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Table 1. Preload Truth Table

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

PREL = Preload data to appropriate register
OUT = Register available on output pins
Z = High impedance state

Figure 1a. Input Formats

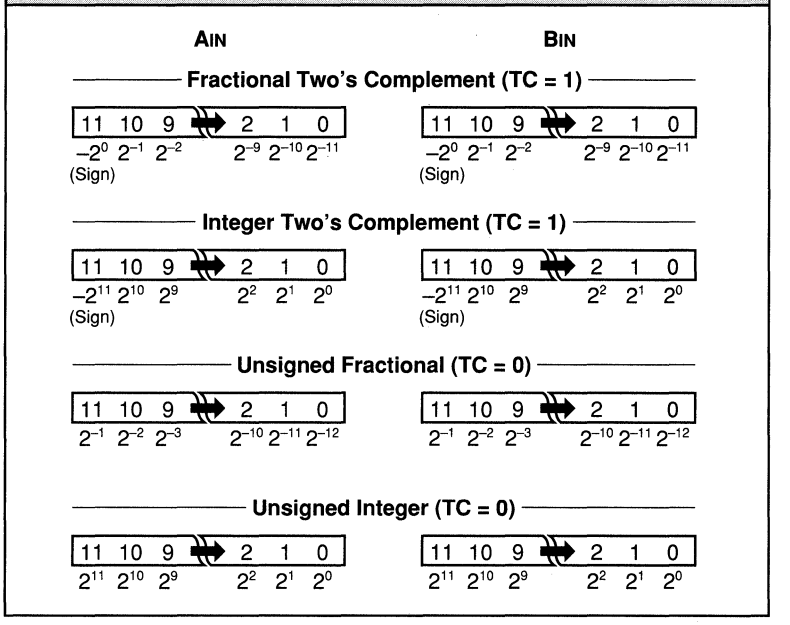
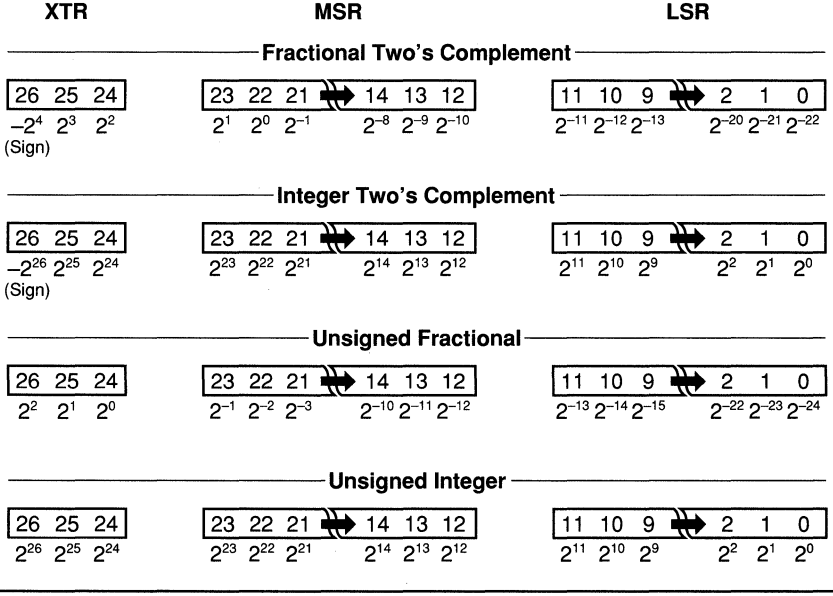


Figure 1b. Output Formats



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

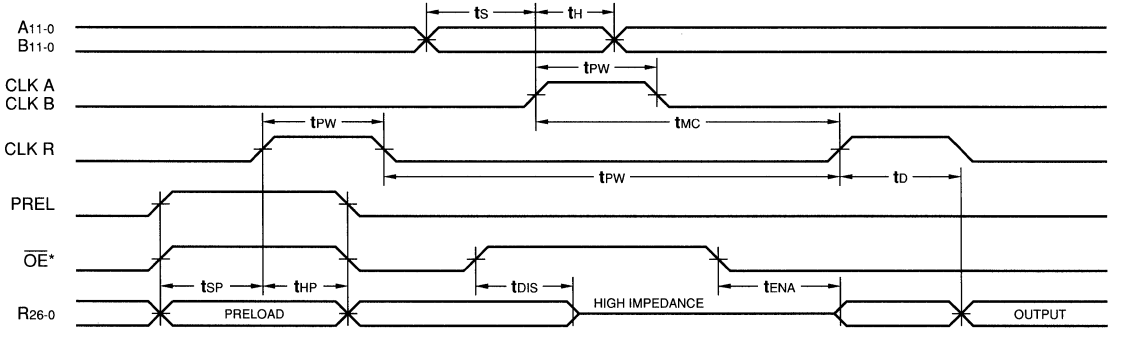
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMA1009/2009–					
		75		55		45	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		55		45
t_{PW}	Clock Pulse Width	15		15		15	
t_S	Input Register Setup Time	15		15		12	
t_H	Input Register Hold Time	2		2		2	
t_{SP}	Preload Setup Time	15		15		12	
t_{HP}	Preload Hold Time	2		2		2	
t_D	Output Delay		30		25		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		30		30		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		25		25

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMA1009/2009–					
		95		65		55	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		95		65		55
t_{PW}	Clock Pulse Width	20		20		15	
t_S	Input Register Setup Time	20		20		15	
t_H	Input Register Hold Time	2		2		2	
t_{SP}	Preload Setup Time	20		20		15	
t_{HP}	Preload Hold Time	2		2		2	
t_D	Output Delay		35		30		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		35		30
t_{DIS}	Three-State Output Disable Delay (Note 11)		30		30		30

SWITCHING WAVEFORMS



*includes $\overline{OEX}$, $\overline{OEM}$, $\overline{OEL}$

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

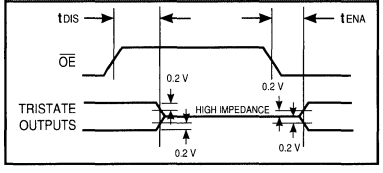
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 2. THRESHOLD LEVELS



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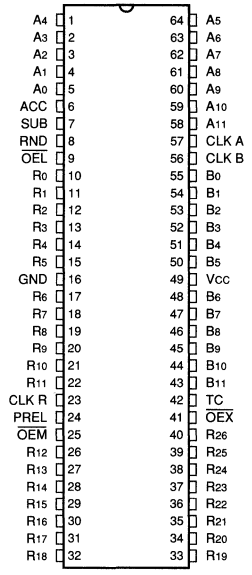
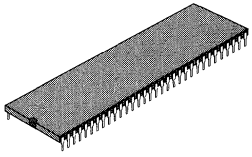
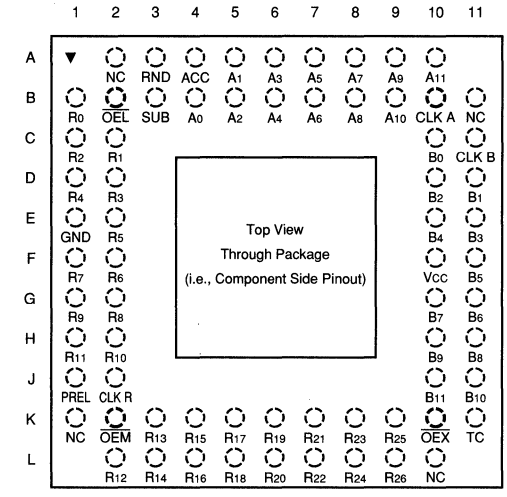
LMA1009 — ORDERING INFORMATION

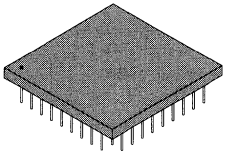
64-pin





68-pin

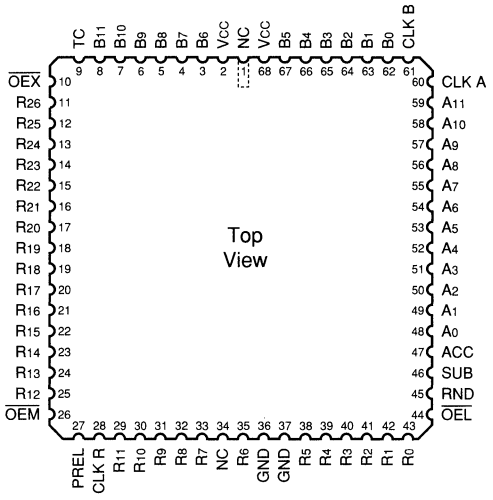


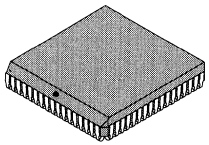


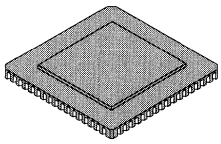
Speed	Sidebraze Hermetic DIP (D6)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — Commercial Screening	
75 ns	LMA1009DC75	LMA1009GC75
55 ns	LMA1009DC55	LMA1009GC55
45 ns	LMA1009DC45	LMA1009GC45
	–55°C to +125°C — Commercial Screening	
95 ns	LMA1009DM95	LMA1009GM95
65 ns	LMA1009DM65	LMA1009GM65
55 ns	LMA1009DM55	LMA1009GM55
	–55°C to +125°C — MIL-STD-883 Compliant	
95 ns	LMA1009DMB95	LMA1009GMB95
65 ns	LMA1009DMB65	LMA1009GMB65
55 ns	LMA1009DMB55	LMA1009GMB55

LMA2009 — ORDERING INFORMATION

68-pin







Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)	
	0°C to +70°C — COMMERCIAL SCREENING		
75 ns	LMA2009JC75	LMA2009KC75	
55 ns	LMA2009JC55	LMA2009KC55	
45 ns	LMA2009JC45	LMA2009KC45	
	–55°C to +125°C — COMMERCIAL SCREENING		
95 ns		LMA2009KM95	
65 ns		LMA2009KM65	
55 ns		LMA2009KM55	
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
95 ns		LMA2009KMB95	
65 ns		LMA2009KMB65	
55 ns		LMA2009KMB55	

LMA1010/2010
16 x 16-bit Multiplier-Accumulator

FEATURES

- 45 ns Multiply-Accumulate Time
- Replaces TRW TMC2210, Cypress CY7C510, IDT 7210L, and AMD Am29510
- Two's Complement or Unsigned Operands
- Accumulator Performs Preload, Accumulate, and Subtract
- Three-State Outputs
- DESC SMD No. 5962-88733
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 64-pin Sidebraze, Hermetic DIP
  - 68-pin Commercial PGA
  - 68-pin Ceramic PGA
  - 68-pin Plastic LCC, J-Lead
  - 68-pin Ceramic LCC

DESCRIPTION

The **LMA1010** and **LMA2010** are high-speed, low power 16-bit multiplier-accumulators. The LMA1010 and LMA2010 are functionally identical; they differ only in packaging. Full military ambient temperature range operation is achieved with advanced CMOS technology.

The LMA1010 and LMA2010 produce the 32-bit product of two 16-bit numbers. The results of a series of multiplications may be accumulated to form the sum of products. Accumulation is performed to 35-bit precision with the multiplier product sign extended as appropriate.

Data present at the A and B input registers is latched on the rising edges of CLK A and CLK B respectively. RND, TC, ACC, and SUB controls are latched on the rising edge of the logical OR of CLK A and CLK B. TC specifies the input as two's complement (TC HIGH) or unsigned magnitude (TC LOW). RND, when HIGH, adds '1' to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

ACC and SUB control accumulator operation. ACC HIGH results in addition of the multiplier product and the accumulator contents, with the result stored in the accumulator register on the rising edge of CLK R. ACC and SUB HIGH results in subtraction of the accumulator contents from the multiplier product, with the result stored in the accumulator register. With ACC LOW, no accumulation occurs and the next product is loaded directly into the accumulator register.

The LMA1010/2010 output register (accumulator register) is divided into three independently controlled sections. The least significant result (LSR) and most significant result (MSR) registers are 16 bits in length. The extended result register (XTR) is 3 bits long. The output signals R15-0 and input signals B15-0 share the same bidirectional pins.

Each output register has an independent output enable control. In addition to providing three-state control of the output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are HIGH and PREL is HIGH, data can be preloaded via the bidirectional output pins into the respective output registers. Data present on the output pins is latched on the rising edge of CLK R. The interrelation of PREL and the enable controls is summarized in Table 1.

LMA1010/2010 Block Diagram

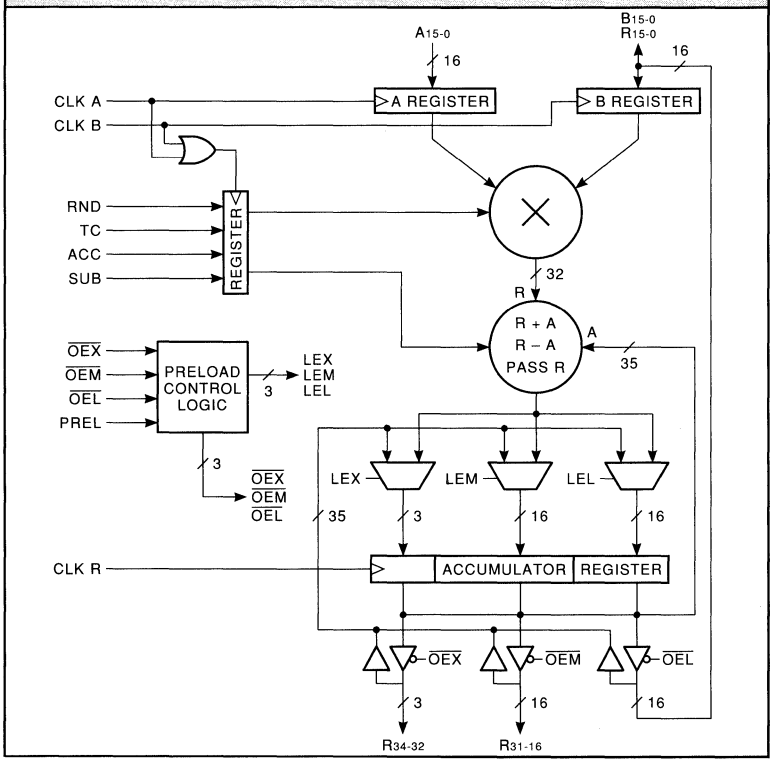


TABLE 1. PRELOAD TRUTH TABLE

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

PREL = Preload data to appropriate register
OUT = Register available on output pins
Z = High impedance state

FIGURE 1A. INPUT FORMATS

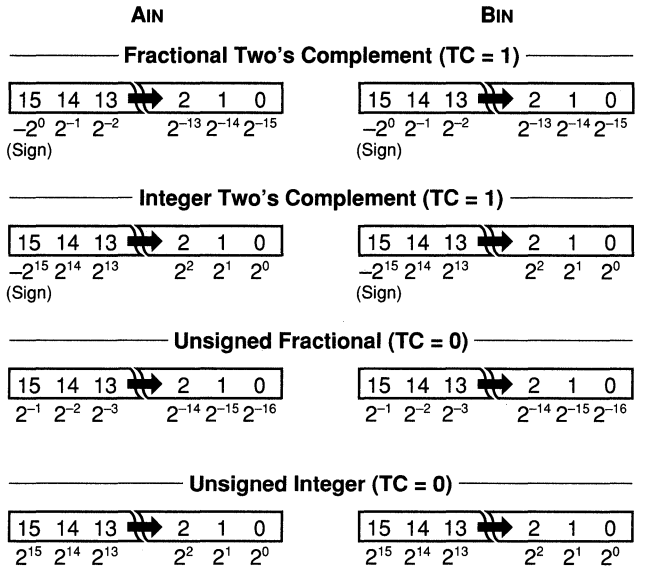
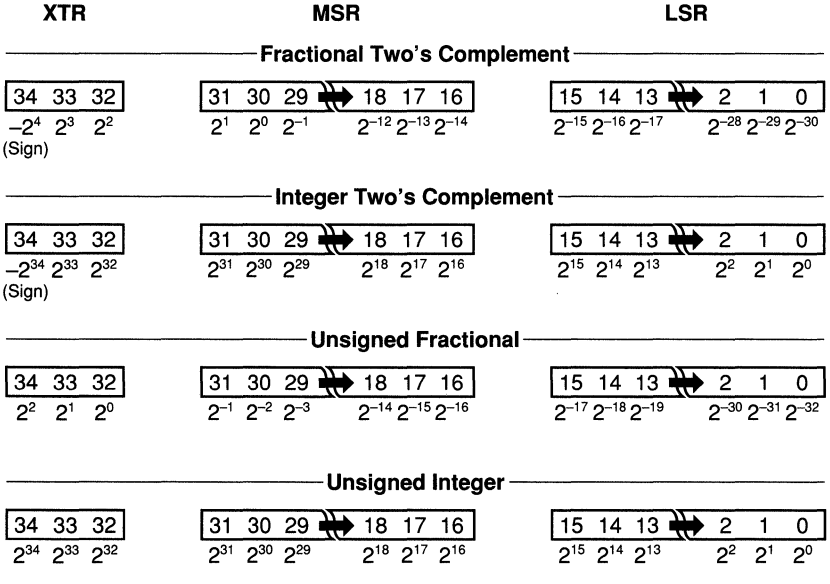


FIGURE 1B. OUTPUT FORMATS



MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		12	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

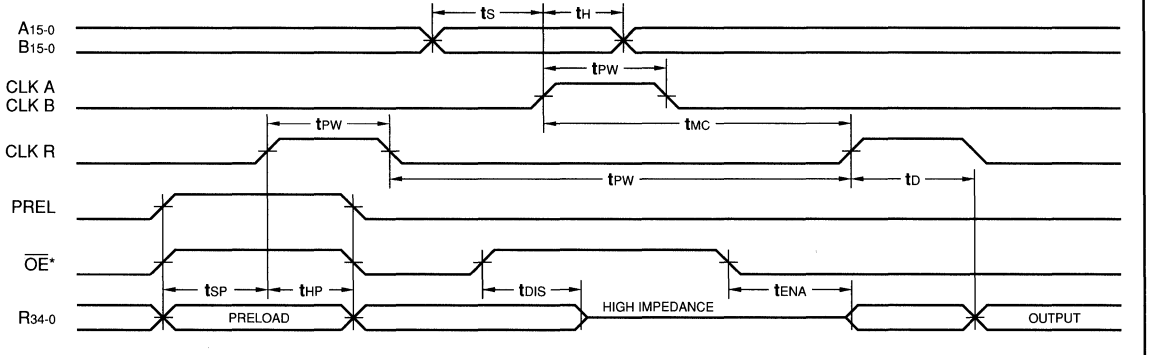
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMA1010/2010–					
		65		55		45	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		65		55		45
t_{PW}	Clock Pulse Width	15		15		15	
t_S	Input Register Setup Time	15		15		12	
t_H	Input Register Hold Time	2		2		2	
t_{SP}	Preload Setup Time	15		15		12	
t_{HP}	Preload Hold Time	2		2		2	
t_D	Output Delay		30		25		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		30		30		30
t_{DIS}	Three-State Output Disable Delay (Note 11)		30		25		25

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMA1010/2010–					
		75		65		55	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{MC}	Clocked Multiply Time		75		65		55
t_{PW}	Clock Pulse Width	20		15		15	
t_S	Input Register Setup Time	20		15		15	
t_H	Input Register Hold Time	2		2		2	
t_{SP}	Preload Setup Time	20		15		15	
t_{HP}	Preload Hold Time	2		2		2	
t_D	Output Delay		35		30		30
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		30		30
t_{DIS}	Three-State Output Disable Delay (Note 11)		35		25		25

SWITCHING WAVEFORMS



*includes $\overline{OEX}$, $\overline{OEM}$, $\overline{OEL}$

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

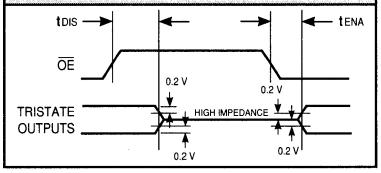
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

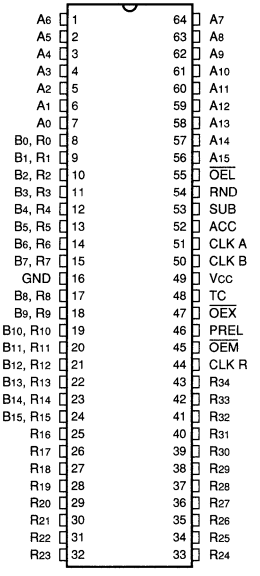
FIGURE 2. THRESHOLD LEVELS

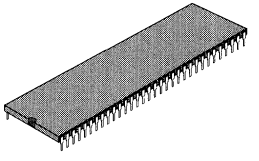


4

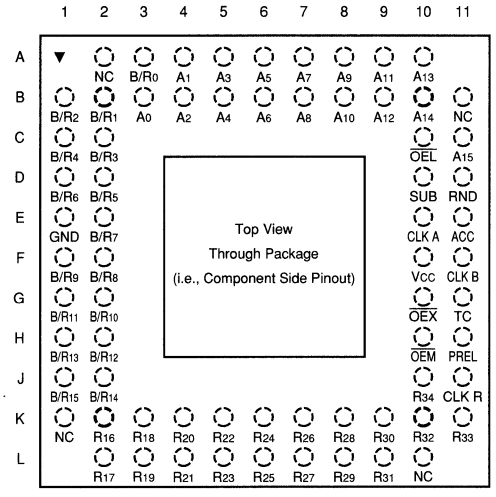
LMA1010 — ORDERING INFORMATION

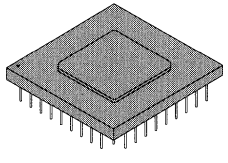
64-pin

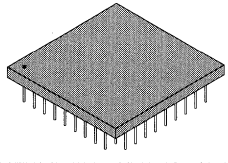




68-pin



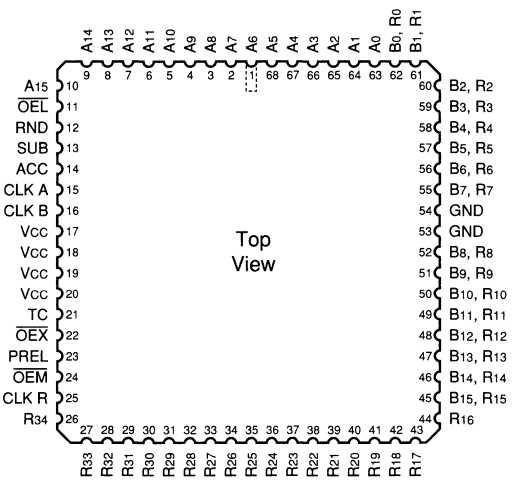


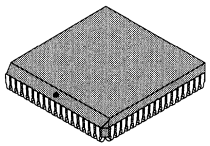


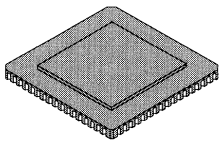
Speed	Sidebraze Hermetic DIP (D6)	Commercial Pin Grid Array (E2)	Ceramic Pin Grid Array (G2)
	0°C to +70°C — COMMERCIAL SCREENING		
65 ns	LMA1010DC65	LMA1010EC65	LMA1010GC65
55 ns	LMA1010DC55	LMA1010EC55	LMA1010GC55
45 ns	LMA1010DC45	LMA1010EC45	LMA1010GC45
	–55°C to +125°C — COMMERCIAL SCREENING		
75 ns	LMA1010DM75		LMA1010GM75
65 ns	LMA1010DM65		LMA1010GM65
55 ns	LMA1010DM55		LMA1010GM55
	–55°C to +125°C — MIL-STD-883 COMPLIANT		
75 ns	LMA1010DMB75		LMA1010GMB75
65 ns	LMA1010DMB65		LMA1010GMB65
55 ns	LMA1010DMB55		LMA1010GMB55

LMA2010 — ORDERING INFORMATION

68-pin







Speed	Plastic J-Lead Chip Carrier (J2)	Ceramic Leadless Chip Carrier (K3)		
	0°C to +70°C — COMMERCIAL SCREENING			
65 ns	LMA2010JC65	LMA2010KC65		
55 ns	LMA2010JC55	LMA2010KC55		
45 ns	LMA2010JC45	LMA2010KC45		
	–55°C to +125°C — COMMERCIAL SCREENING			
75 ns		LMA2010KM75		
65 ns		LMA2010KM65		
55 ns		LMA2010KM55		
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
75 ns		LMA2010KMB75		
65 ns		LMA2010KMB65		
55 ns		LMA2010KMB55		

LMS12
12-bit Cascadable Multiplier-Summer

FEATURES

- 12 x 12-bit Multiplier with Pipelined 26-bit Output Summer
- Summer has 26-bit Input Port Fully Independent from Multiplier Inputs
- Cascadable to Form Video Rate FIR Filter with 3-bit Headroom
- A, B, and C Input Registers Separately Enabled for Maximum Flexibility
- 25 MHz Data Rate for FIR Filtering Applications
- High Speed, Low Power CMOS Technology
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 84-pin Plastic LCC, J-Lead
  - 84-pin Ceramic PGA

DESCRIPTION

The **LMS12** is a high-speed 12 x 12-bit combinatorial multiplier integrated with a 26-bit adder in a single 84-pin package. It is an ideal building block for the implementation of very high-speed FIR filters for video, RADAR, and other similar applications. The LMS12 implements the general form (A•B) + C. As a result, it is also useful in implementing polynomial approximations to transcendental functions.

ARCHITECTURE

A block diagram of the LMS12 is shown below. Its major features are discussed individually in the following paragraphs.

MULTIPLIER

The $A_{11\text{-}0}$ and $B_{11\text{-}0}$ inputs to the LMS12 are captured at the rising edge of the clock in the 12-bit A and B input registers, respectively. These registers are independently enabled by the $\overline{ENA}$ and $\overline{ENB}$ inputs. The registered input data are then applied to a 12 x 12-bit multiplier array, which produces a 24-bit result. Both the inputs and outputs of the multiplier are in two's complement format. The multiplication result forms the input to the 24-bit product register.

SUMMER

The $C_{25\text{-}0}$ inputs to the LMS12 form a 26-bit two's complement number which is captured in the C register at the rising edge of the clock. The C register is enabled by assertion of the $\overline{ENC}$ input. The summer is a 26-bit adder which operates on the C register data and the sign extended contents of the product register to produce a 26-bit sum. This sum is applied to the 26-bit S register.

OUTPUT MULTIPLEXER

The FTS input controls a multiplexer which selects the data to be output on the $S_{25\text{-}0}$ lines. When FTS is asserted, the summer result is applied directly to the S output port. When FTS is deasserted, the multiplexer selects the S register for output on the S port, effecting a one-cycle delay of the summer result. The S output port can be forced to a high-impedance state by driving the $\overline{OE}$ control line high. FTS would be asserted for conventional FIR filter applications, however the insertion of zero-coefficient filter taps may be accomplished by negating FTS. Negating FTS also allows application of the same filter transfer function to two interleaved datastreams with successive input and output sample points occurring on alternate clock cycles.

LMS12 BLOCK DIAGRAM

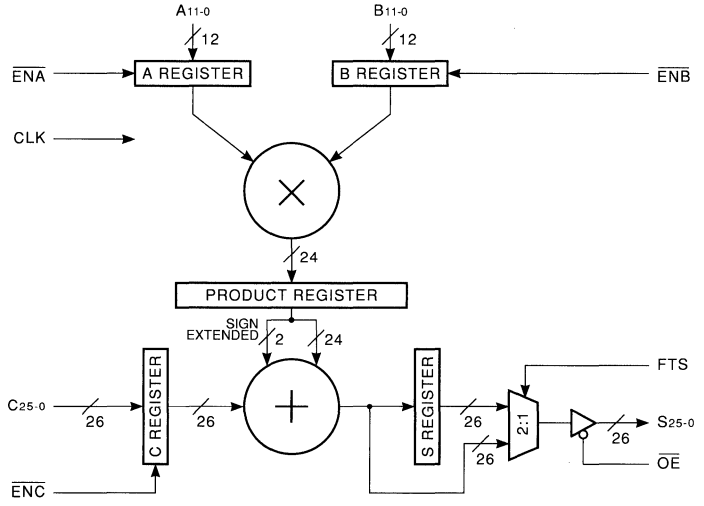
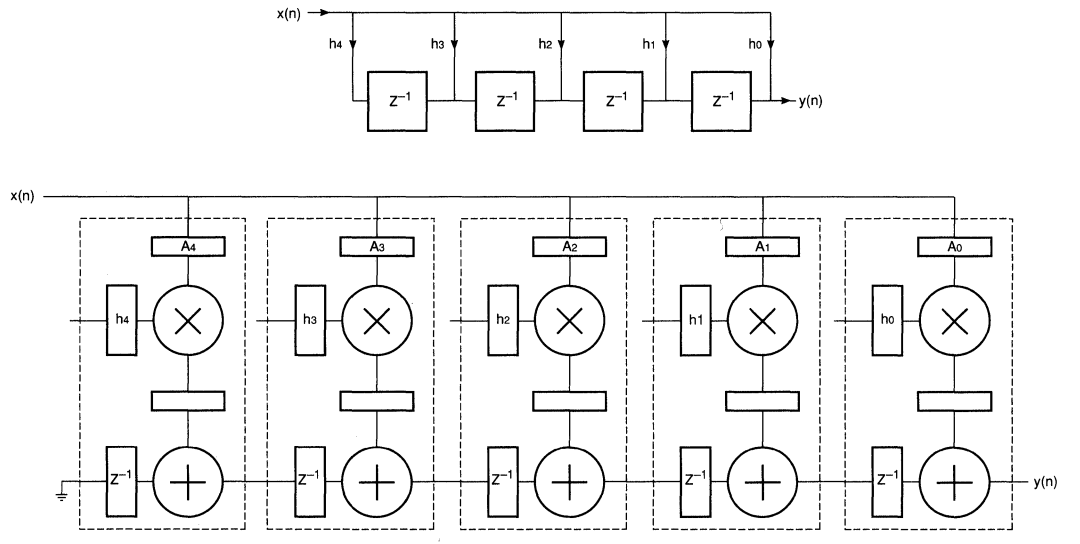


FIGURE 1. FLOW DIAGRAM FOR 5-TAP FIR FILTER



APPLICATIONS

The LMS12 is designed specifically for high-speed FIR filtering applications requiring a throughput rate of one output sample per clock period. By cascading LMS12 units, the transpose form of the FIR transfer function is implemented directly, with each of the LMS12 units supplying one of the filter weights, and the cascaded summers accumulating the results. The signal flow graph for a 5-tap FIR filter and the equivalent implementation using LMS12's is shown in Figure 1.

The operation of the 5-tap FIR filter implementation of Figure 1 is depicted in Table 1. The filter weights h4 - h0 are assumed to be latched in the B input registers of the LMS12 units. The x(n) data is applied in parallel to the A input registers of all devices. For descriptive purposes in the table, the A register contents and sum output data of each device is labelled according to the index of the weight applied by that device; i.e., S0 is produced by the rightmost device, which has h0 as its filter weight and A0 as its input register contents. Each column represents one clock cycle, with the data passing a particular point in the system illustrated across each row.

TABLE 1. TIMING EXAMPLE FOR 5-TAP NONDECIMATING FIR FILTER

CLK Cycle	1	2	3	4	5	6	7	8	9
$X_{(n)}$	X_n	X_{n+1}	X_{n+2}	X_{n+3}	X_{n+4}	X_{n+5}	X_{n+6}	X_{n+7}	X_{n+8}
A_4 Register Sum 4		X_n	X_{n+1} h_4X_n	X_{n+2} h_4X_{n+1}	X_{n+3} h_4X_{n+2}	X_{n+4} h_4X_{n+3}	X_{n+5} h_4X_{n+4}	X_{n+6} h_4X_{n+5}	X_{n+7} h_4X_{n+6}
A_3 Register Sum 3		X_n	X_{n+1} h_3X_n + h_4X_{n-1}	X_{n+2} h_3X_{n+1} + h_4X_n	X_{n+3} h_3X_{n+2} + h_4X_{n+1}	X_{n+4} h_3X_{n+3} + h_4X_{n+2}	X_{n+5} h_3X_{n+4} + h_4X_{n+3}	X_{n+6} h_3X_{n+5} + h_4X_{n+4}	X_{n+7} h_3X_{n+6} + h_4X_{n+5}
A_2 Register Sum 2		X_n	X_{n+1} h_2X_n + h_3X_{n-1} + h_4X_{n-2}	X_{n+2} h_2X_{n+1} + h_3X_n + h_4X_{n-1}	X_{n+3} h_2X_{n+2} + h_3X_{n+1} + h_4X_n	X_{n+4} h_2X_{n+3} + h_3X_{n+2} + h_4X_{n+1}	X_{n+5} h_2X_{n+4} + h_3X_{n+3} + h_4X_{n+2}	X_{n+6} h_2X_{n+5} + h_3X_{n+4} + h_4X_{n+3}	X_{n+7} h_2X_{n+6} + h_3X_{n+5} + h_4X_{n+4}
A_1 Register Sum 1		X_n	X_{n+1} h_1X_n + h_2X_{n-1} + h_3X_{n-2} + h_4X_{n-3}	X_{n+2} h_1X_{n+1} + h_2X_n + h_3X_{n-1} + h_4X_{n-2}	X_{n+3} h_1X_{n+2} + h_2X_{n+1} + h_3X_n + h_4X_{n-1}	X_{n+4} h_1X_{n+3} + h_2X_{n+2} + h_3X_{n+1} + h_4X_n	X_{n+5} h_1X_{n+4} + h_2X_{n+3} + h_3X_{n+2} + h_4X_{n+1}	X_{n+6} h_1X_{n+5} + h_2X_{n+4} + h_3X_{n+3} + h_4X_{n+2}	X_{n+7} h_1X_{n+6} + h_2X_{n+5} + h_3X_{n+4} + h_4X_{n+3}
A_0 Register Sum 0		X_n	X_{n+1} h_0X_n + h_1X_{n-1} + h_2X_{n-2} + h_3X_{n-3} + h_4X_{n-4}	X_{n+2} h_0X_{n+1} + h_1X_n + h_2X_{n-1} + h_3X_{n-2} + h_4X_{n-3}	X_{n+3} h_0X_{n+2} + h_1X_{n+1} + h_2X_n + h_3X_{n-1} + h_4X_{n-2}	X_{n+4} h_0X_{n+3} + h_1X_{n+2} + h_2X_{n+1} + h_3X_n + h_4X_{n-1}	X_{n+5} h_0X_{n+4} + h_1X_{n+3} + h_2X_{n+2} + h_3X_{n+1} + h_4X_n	X_{n+6} h_0X_{n+5} + h_1X_{n+4} + h_2X_{n+3} + h_3X_{n+2} + h_4X_{n+1}	X_{n+7} h_0X_{n+6} + h_1X_{n+5} + h_2X_{n+4} + h_3X_{n+3} + h_4X_{n+2}

4

FIGURE 2A. INPUT FORMATS

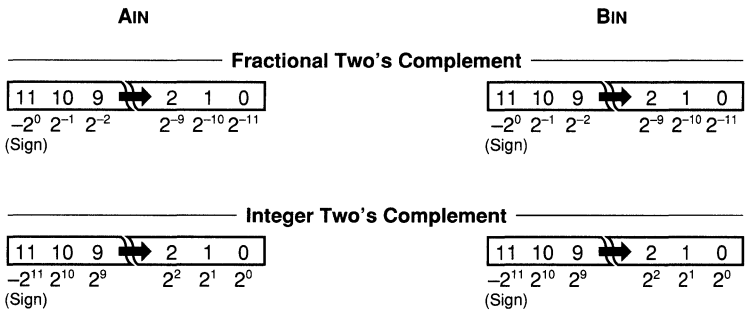
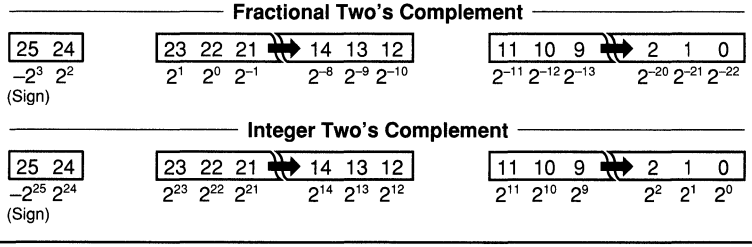


FIGURE 2B. OUTPUT FORMATS



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

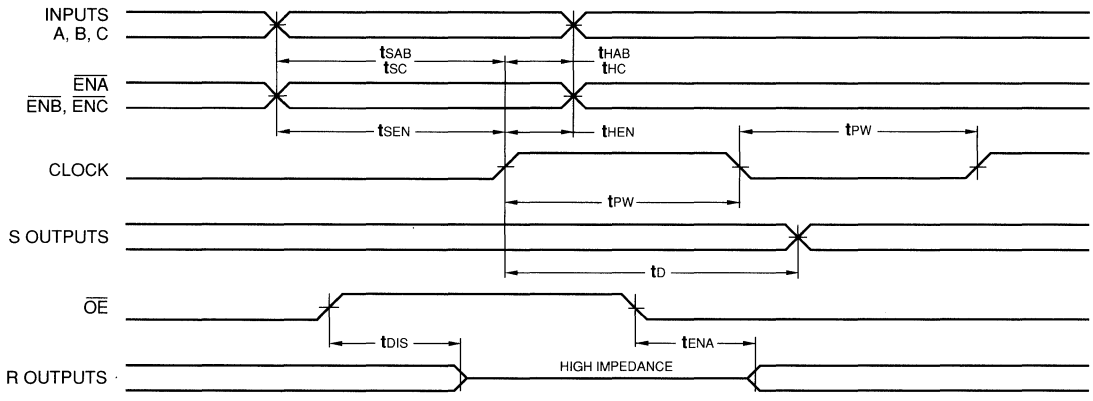
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	3.5			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		15	25	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LMS12–					
		65		50		40	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CP}	Clock Period	40		35		30	
t_{PW}	Clock Pulse Width	15		15		12	
t_{SAB}	A, B, Data Setup Time	15		12		12	
t_{SC}	C Data Setup Time	15		10		7	
t_{SEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		12		12	
t_{HAB}	A, B, Data Hold Time	5		5		5	
t_{HC}	C Data Hold Time	5		5		5	
t_{HEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5		5	
t_D	Clock to S–FT = 1		50		40		35
	Clock to S–FT = 0		25		25		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		22		22		22

SWITCHING WAVEFORMS

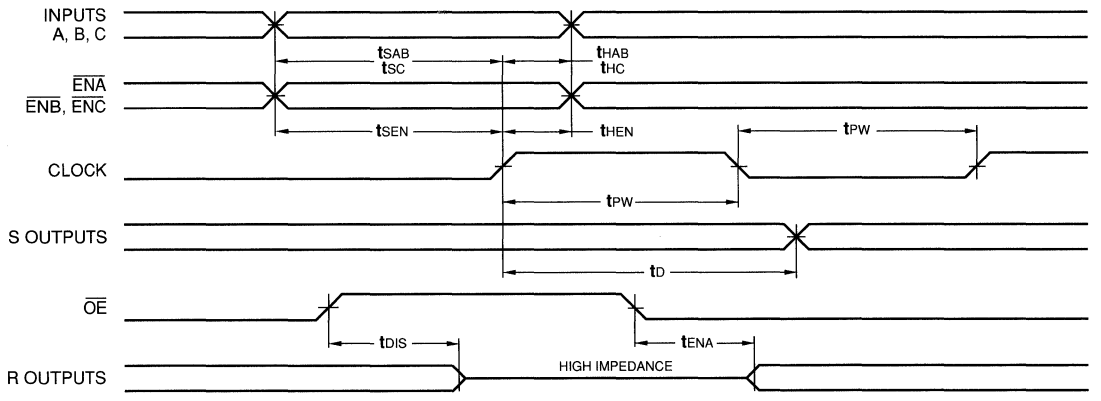


SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LMS12–			
		65		50	
Symbol	Parameter	Min	Max	Min	Max
t_{CP}	Clock Period	40		35	
t_{PW}	Clock Pulse Width	15		15	
t_{SAB}	A, B, Data Setup Time	15		15	
t_{SC}	C Data Setup Time	15		15	
t_{SEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Setup Time	15		15	
t_{HAB}	A, B, Data Hold Time	5		5	
t_{HC}	C Data Hold Time	5		5	
t_{HEN}	$\overline{ENA}$, $\overline{ENB}$, $\overline{ENC}$ Hold Time	5		5	
t_D	Clock to S–FT = 1		50		45
	Clock to S–FT = 0		25		25
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		22		22

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

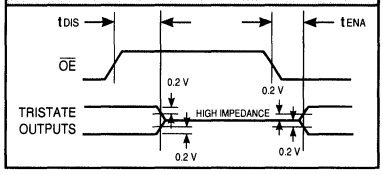
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 3. THRESHOLD LEVELS



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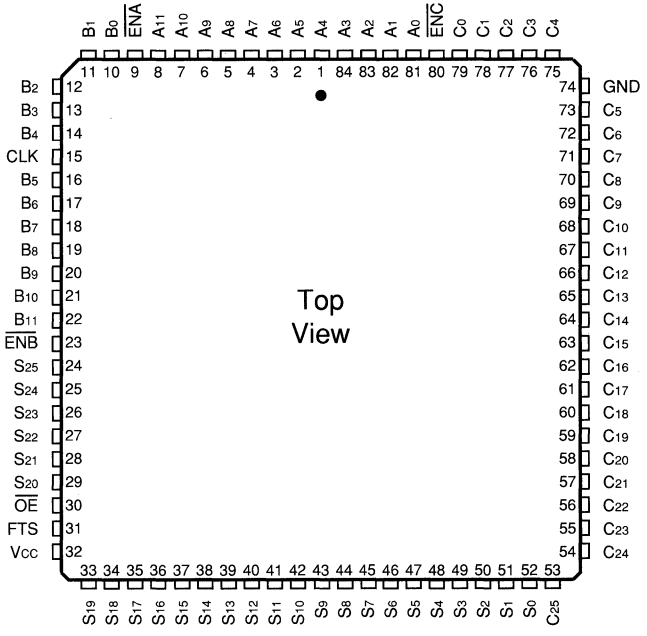
ORDERING INFORMATION

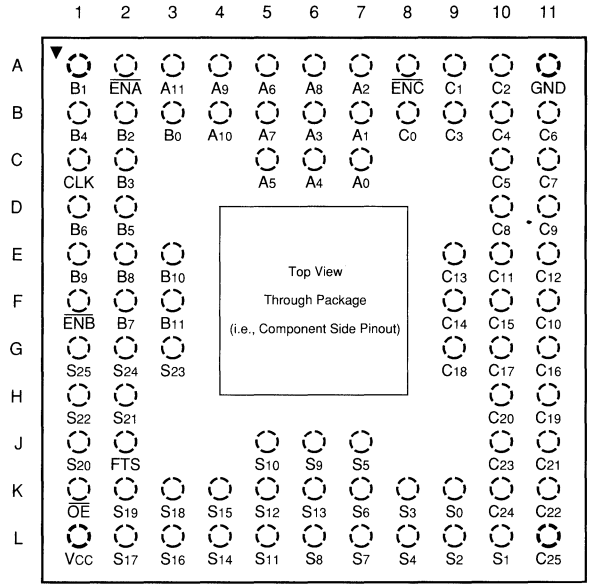
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
65 ns	LMS12JC65
50 ns	LMS12JC50
40 ns	LMS12JC40
	–55°C to +125°C — COMMERCIAL SCREENING
65 ns	
50 ns	
	–55°C to +125°C — MIL-STD-883 COMPLIANT
65 ns	
50 ns	

ORDERING INFORMATION

84-pin



Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — Commercial Screening
65 ns	LMS12GC65
50 ns	LMS12GC50
40 ns	LMS12GC40
	–55°C to +125°C — Commercial Screening
65 ns	LMS12GM65
50 ns	LMS12GM50
	–55°C to +125°C — MIL-STD-883 Compliant
65 ns	LMS12GMB65
50 ns	LMS12GMB50

Ordering Information 1
Video Imaging Products 2
Arithmetic Logic Units & Special Arithmetic Functions 3
Multipliers & Multiplier-Accumulators 4
Register Products 5
Peripheral Products 6
Quality and Reliability 7
Technology and Design Features 8
Package Information 9
Product Listing 10
Sales Offices 11

Register Products

5

REGISTER PRODUCTS 5-1

Pipeline Registers

L29C520 4 x 8-bit Multilevel Pipeline Register (1-4 Stages) 5-3
L29C521 4 x 8-bit Multilevel Pipeline Register (1-4 Stages) 5-3
LPR520 4 x 16-bit Multilevel Pipeline Register (1-4 Stages) 5-11
LPR521 4 x 16-bit Multilevel Pipeline Register (1-4 Stages) 5-11
LPR200 8 x 16-bit Multilevel Pipeline Register (1-8 Stages) 5-17
LPR201 7 x 16-bit Multilevel Pipeline Register (1-7 Stages) 5-17
L29C524 14 x 8-bit Dual 7-Deep Pipeline Register (1-14 Stages) 5-27
L29C525 16 x 8-bit Dual 8-Deep Pipeline Register (1-16 Stages) 5-27
L10C11 4/8-bit Variable Length Shift Register (3-18 Stages) 5-37

Register Files

LRF07 8 x 8-bit Register File (3-Port) 5-43

Shadow Registers

L29C818 8-bit Serial Scan Shadow Register 5-49

L29C520/521
4 x 8-bit Multilevel Pipeline Register

FEATURES

- Four 8-bit Registers
- Implements Double 2-Stage Pipeline or Single 4-Stage Pipeline Register
- Hold, Shift, and Load Instructions
- Separate Data In and Data Out Pins
- High-Speed, Low Power CMOS Technology
- Three-State Outputs
- DESC SMD No. 5962-91762
- Available 100% Screened to MIL-STD-883, Class B
- Replaces IDT29FCT520/IDT29FCT521 and AMD Am29520/Am29521
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Ceramic DIP
  - 28-pin Plastic LCC, J-Lead
  - 28-pin Ceramic LCC
  - 24-pin Ceramic Flatpack

DESCRIPTION

The **L29C520** and **L29C521** are pin-for-pin compatible with the IDT29FCT520/IDT29FCT521 and AMD Am29520/Am29521, implemented in low power CMOS.

The L29C520 and L29C521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I_{1-0}, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R1 and shifted sequentially through R2, R3, and R4. Also, for the L29C520, data may be loaded from the inputs into either R1 or R3 with only R2 or R4 shifting. The L29C521 differs from the L29C520 in that R2 and R4 remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I_{1-0} may be set to prevent any register from changing.

The S_{1-0} select lines control a 4-to-1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

TABLE 1. L29C520 INSTRUCTION TABLE

I_1	I_0	Description			
L	L	D→R1	R1→R2	R2→R3	R3→R4
L	H	HOLD	HOLD	D→R3	R3→R4
H	L	D→R1	R1→R2	HOLD	HOLD
H	H	ALL REGISTERS ON HOLD			

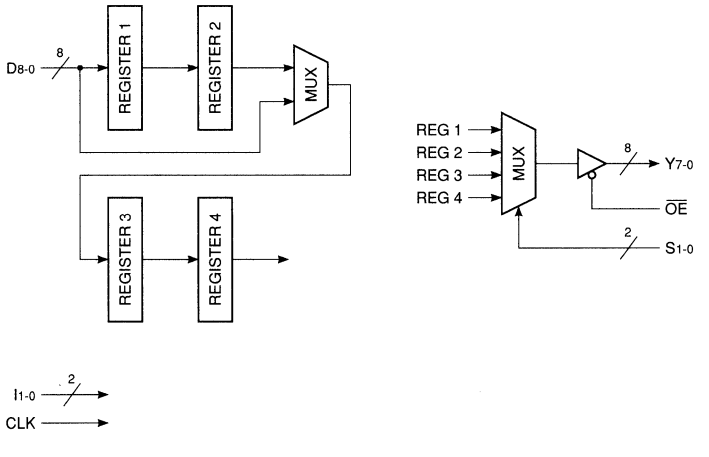
TABLE 2. L29C521 INSTRUCTION TABLE

I_1	I_0	Description			
L	L	D→R1	R1→R2	R2→R3	R3→R4
L	H	HOLD	HOLD	D→R3	HOLD
H	L	D→R1	HOLD	HOLD	HOLD
H	H	ALL REGISTERS ON HOLD			

TABLE 3. OUTPUT SELECT

S_1	S_0	Register Selected
L	L	Register 4
L	H	Register 3
H	L	Register 2
H	H	Register 1

L29C520/521 BLOCK DIAGRAM



5

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –15.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.5	mA

SWITCHING CHARACTERISTICS

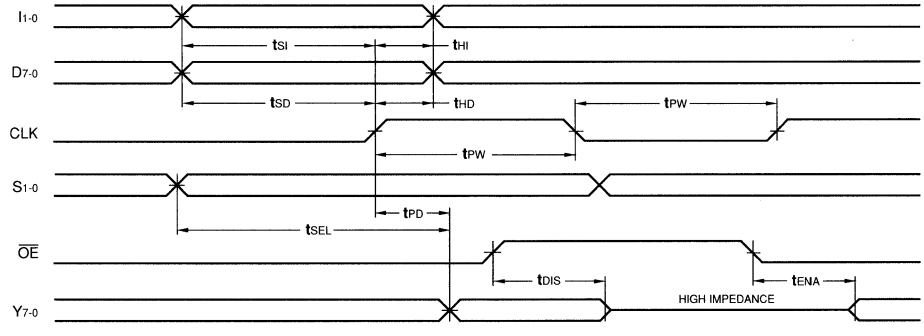
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C520/521–			
		22		14	
Symbol	Parameter	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		22		14
t_{SEL}	Select to Output Delay		20		13
t_{PW}	Clock Pulse Width	10		7	
t_{SI}	Instruction Setup Time	10		5	
t_{HI}	Instruction Hold Time	3		1	
t_{SD}	Data Setup Time	10		5	
t_{HD}	Data Hold Time	3		1	
t_{ENA}	Three-State Output Enable Delay (Note 11)		21		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		12

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C520/521–					
		30		24		16	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		30		24		16
t_{SEL}	Select to Output Delay		30		22		15
t_{PW}	Clock Pulse Width	15		10		8	
t_{SI}	Instruction Setup Time	15		10		6	
t_{HI}	Instruction Hold Time	5		3		2	
t_{SD}	Data Setup Time	15		10		6	
t_{HD}	Data Hold Time	5		3		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		22		16
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		16		13

SWITCHING WAVEFORMS



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7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

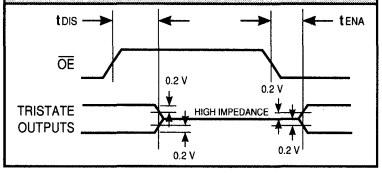
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

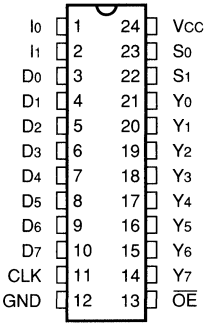
12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 1. THRESHOLD LEVELS

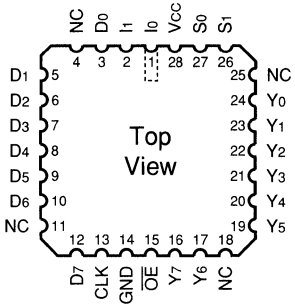


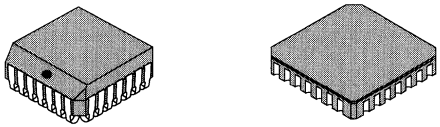
L29C520 — ORDERING INFORMATION

24-pin — 0.3" wide



28-pin



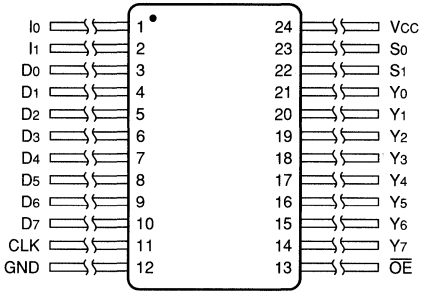


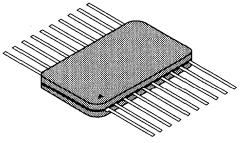
Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — COMMERCIAL SCREENING			
22 ns	L29C520PC22	L29C520CC22	L29C520JC22	L29C520KC22
14 ns	L29C520PC14	L29C520CC14	L29C520JC14	L29C520KC14
	–55°C to +125°C — COMMERCIAL SCREENING			
30 ns		L29C520CM30		L29C520KM30
24 ns		L29C520CM24		L29C520KM24
16 ns		L29C520CM16		L29C520KM16
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
30 ns		L29C520CMB30		L29C520KMB30
24 ns		L29C520CMB24		L29C520KMB24
16 ns		L29C520CMB16		L29C520KMB16

5

L29C520 — ORDERING INFORMATION

24-pin

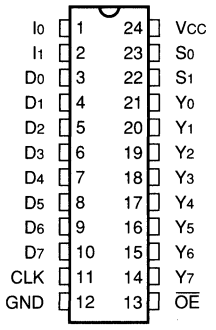




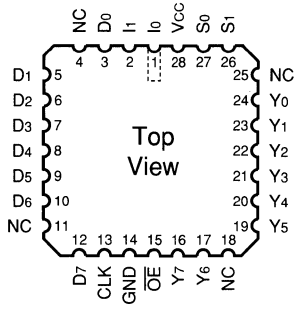
Speed	Ceramic Flatpack (M1)	
	0°C to +70°C — Commercial Screening	
22 ns	L29C520MC22	
14 ns	L29C520MC14	
	–55°C to +125°C — Commercial Screening	
30 ns	L29C520MM30	
24 ns	L29C520MM24	
16 ns	L29C520MM16	
	–55°C to +125°C — MIL-STD-883 Compliant	
30 ns	L29C520MMB30	
24 ns	L29C520MMB24	
16 ns	L29C520MMB16	

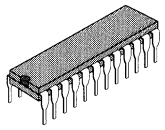
L29C521 — ORDERING INFORMATION

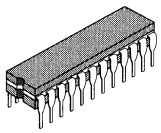
24-pin — 0.3" wide

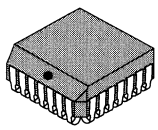


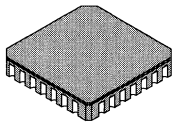
28-pin







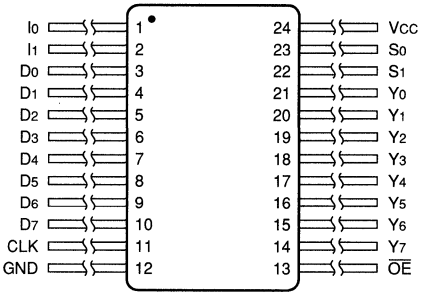


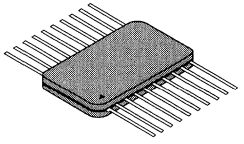


Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic J-Lead Chip Carrier (J4)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — Commercial Screening			
22 ns	L29C521PC22	L29C521CC22	L29C521JC22	L29C521KC22
14 ns	L29C521PC14	L29C521CC14	L29C521JC14	L29C521KC14
	–55°C to +125°C — Commercial Screening			
30 ns		L29C521CM30		L29C521KM30
24 ns		L29C521CM24		L29C521KM24
16 ns		L29C521CM16		L29C521KM16
	–55°C to +125°C — MIL-STD-883 Compliant			
30 ns		L29C521CMB30		L29C521KMB30
24 ns		L29C521CMB24		L29C521KMB24
16 ns		L29C521CMB16		L29C521KMB16

L29C521 — ORDERING INFORMATION

24-pin





Speed	Ceramic Flatpack (M1)	
	0°C to +70°C — Commercial Screening	
22 ns	L29C521MC22	
14 ns	L29C521MC14	
	–55°C to +125°C — Commercial Screening	
30 ns	L29C521MM30	
24 ns	L29C521MM24	
16 ns	L29C521MM16	
	–55°C to +125°C — MIL-STD-883 Compliant	
30 ns	L29C521MMB30	
24 ns	L29C521MMB24	
16 ns	L29C521MMB16	

LPR520/521
4 x 16-bit Multilevel Pipeline Register

FEATURES

- Four 16-bit Registers
- Implements Double 2-Stage Pipeline or Single 4-Stage Pipeline Register
- Hold, Shift, and Load Instructions
- Separate Data In and Data Out Pins
- High-Speed, Low Power CMOS Technology
- Three-State Outputs
- DESC SMD No. 5962-89716
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Ceramic DIP
  - 44-pin Plastic LCC, J-Lead
  - 44-pin Ceramic LCC

DESCRIPTION

The **LPR520** and **LPR521** are functionally compatible with the IDT29FCT520/IDT29FCT521 and AMD Am29520/Am29521 but have 16-bit inputs and outputs. They are implemented in low power CMOS.

The LPR520 and LPR521 contain four registers which can be configured as two independent, 2-level pipelines or as one 4-level pipeline.

The Instruction pins, I_{1-0}, control the loading of the registers. For either device, the registers may be configured as a four-stage delay line, with data loaded into R1 and shifted sequentially through R2, R3, and R4. Also, for the LPR520, data may be loaded from the inputs into either R1 or R3 with only R2 or R4 shifting. The LPR521 differs from the LPR520 in that R2 and R4 remain unchanged during this type of data load, as shown in Tables 1 and 2. Finally, I_{1-0} may be set to prevent any register from changing.

The S_{1-0} select lines control a 4-to-1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allows simultaneous write and read operations on different registers.

LPR520/521 Block Diagram

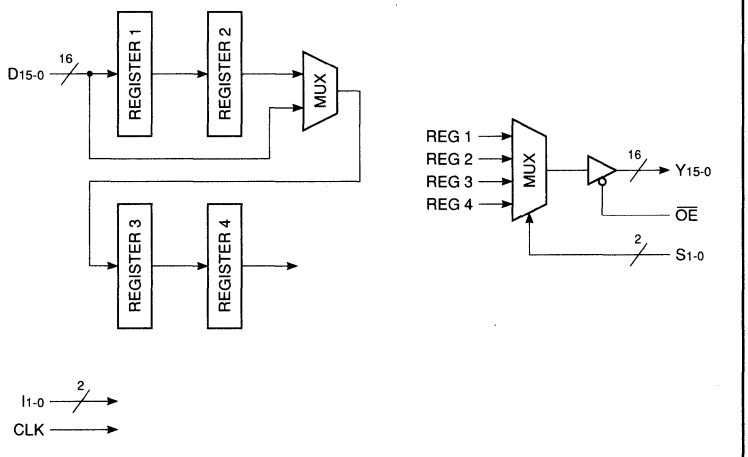


Table 1. LPR520 Instruction Table

I_1	I_0	Description			
L	L	D→R1	R1→R2	R2→R3	R3→R4
L	H	HOLD	HOLD	D→R3	R3→R4
H	L	D→R1	R1→R2	HOLD	HOLD
H	H	ALL REGISTERS ON HOLD			

Table 2. LPR521 Instruction Table

I_1	I_0	Description			
L	L	D→R1	R1→R2	R2→R3	R3→R4
L	H	HOLD	HOLD	D→R3	HOLD
H	L	D→R1	HOLD	HOLD	HOLD
H	H	ALL REGISTERS ON HOLD			

Table 3. Output Select

S_1	S_0	Register Selected
L	L	Register 4
L	H	Register 3
H	L	Register 2
H	H	Register 1

5

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	40	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

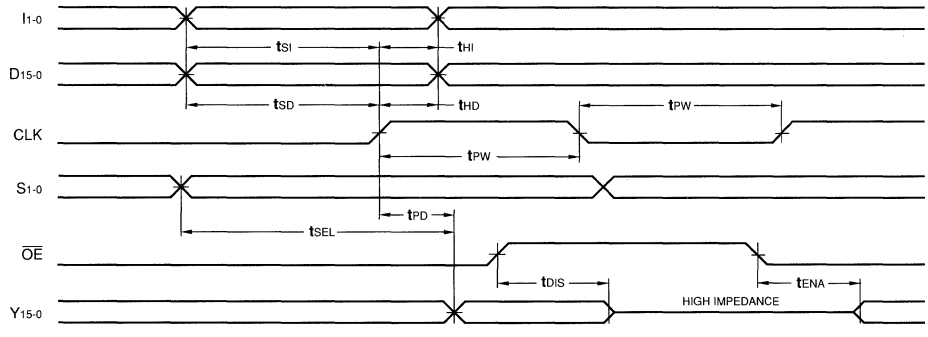
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LPR520/521–					
		25		22		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		25		22		15
t_{SEL}	Select to Output Delay		25		20		15
t_{PW}	Clock Pulse Width	10		10		8	
t_{SI}	Instruction Setup Time	13		10		6	
t_{HI}	Instruction Hold Time	3		3		1	
t_{SD}	Data Setup Time	13		10		6	
t_{HD}	Data Hold Time	3		3		1	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		21		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		15		12

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LPR520/521–					
		30		24		18	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		30		24		18
t_{SEL}	Select to Output Delay		30		22		18
t_{PW}	Clock Pulse Width	15		10		9	
t_{SI}	Instruction Setup Time	15		10		8	
t_{HI}	Instruction Hold Time	5		3		2	
t_{SD}	Data Setup Time	15		10		8	
t_{HD}	Data Hold Time	5		3		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		22		16
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		16		13

SWITCHING WAVEFORMS



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NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

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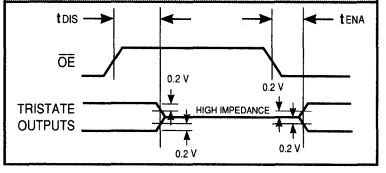
11. Transition is measured ±200 mV from steady-state voltage with specified loading.

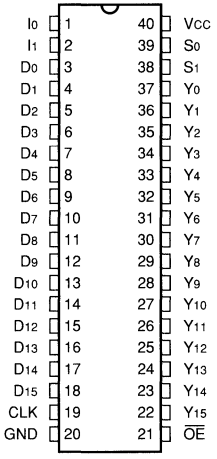
12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

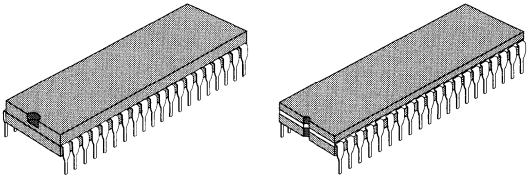
FIGURE 1. THRESHOLD LEVELS



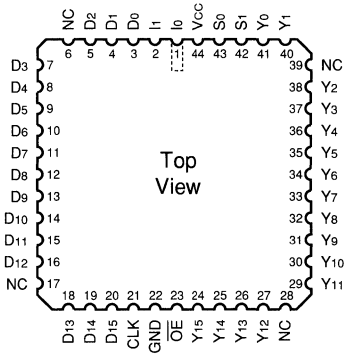
LPR520 — ORDERING INFORMATION

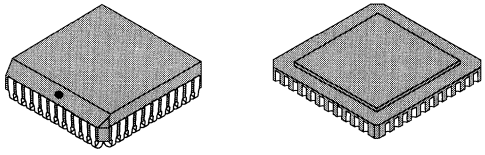
40-pin — 0.6" wide





44-pin





Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — Commercial Screening			
25 ns	LPR520PC25	LPR520CC25	LPR520JC25	LPR520KC25
22 ns	LPR520PC22	LPR520CC22	LPR520JC22	LPR520KC22
15 ns	LPR520PC15	LPR520CC15	LPR520JC15	LPR520KC15
	–55°C to +125°C — Commercial Screening			
30 ns		LPR520CM30		LPR520KM30
24 ns		LPR520CM24		LPR520KM24
18 ns		LPR520CM18		LPR520KM18
	–55°C to +125°C — MIL-STD-883 Compliant			
30 ns		LPR520CMB30		LPR520KMB30
24 ns		LPR520CMB24		LPR520KMB24
18 ns		LPR520CMB18		LPR520KMB18

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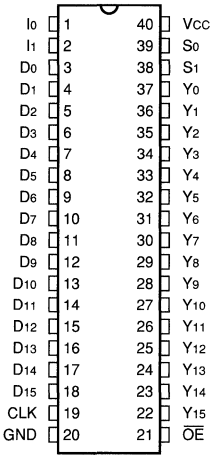
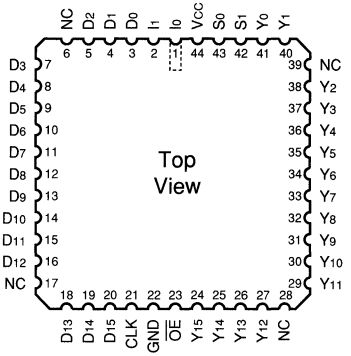
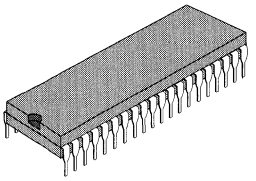
LPR521 — ORDERING INFORMATION

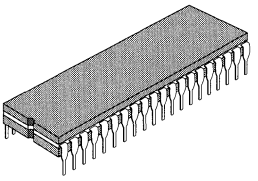
40-pin — 0.6" wide

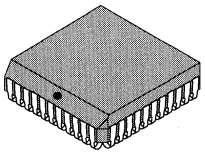


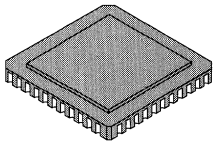
44-pin











Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — Commercial Screening			
25 ns	LPR521PC25	LPR521CC25	LPR521JC25	LPR521KC25
22 ns	LPR521PC22	LPR521CC22	LPR521JC22	LPR521KC22
15 ns	LPR521PC15	LPR521CC15	LPR521JC15	LPR521KC15
	–55°C to +125°C — Commercial Screening			
30 ns		LPR521CM30		LPR521KM30
24 ns		LPR521CM24		LPR521KM24
18 ns		LPR521CM18		LPR521KM18
	–55°C to +125°C — MIL-STD-883 Compliant			
30 ns		LPR521CMB30		LPR521KMB30
24 ns		LPR521CMB24		LPR521KMB24
18 ns		LPR521CMB18		LPR521KMB18

LPR200/201
16-bit Multilevel Pipeline Register

FEATURES

- Pipeline Registers — Eight 16-bit High-Speed (LPR200) or Seven 16-bit High-Speed with a Direct Feed-Through Path (LPR201)
- Programmable Multilevel Register Configurations
- Access time of 10 ns
- Hold, Shift, and Load Instructions
- Replaces IDT73200 and IDT73201
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 48-pin Plastic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 52-pin Plastic LCC, J-Lead
  - 52-pin Ceramic LCC

DESCRIPTION

The **LPR200** and **LPR201** are programmable multilevel pipeline registers. Both devices are pin-for-pin compatible with the IDT73200 and IDT73201.

The LPR200 contains eight 16-bit high-speed pipeline registers which can be configured as eight independent, 1-level pipelines; four independent, 2-level pipelines; two independent, 4-level pipelines; or as one 8-level pipeline.

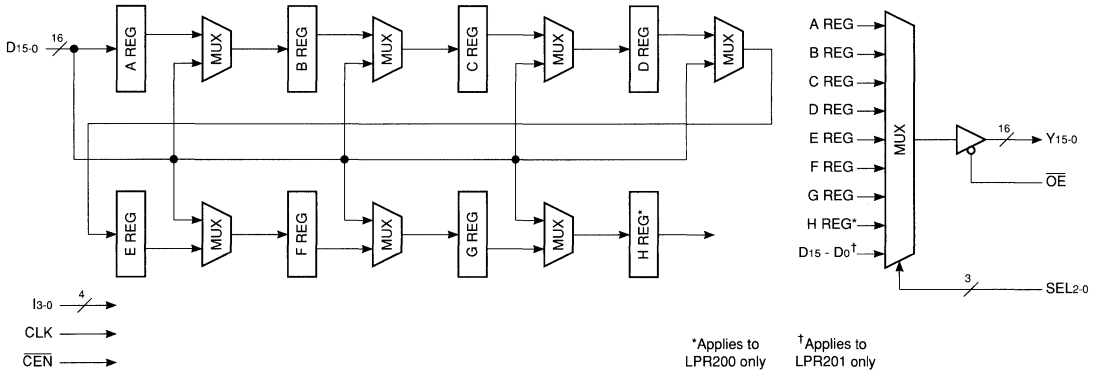
The LPR201 contains seven 16-bit high-speed pipeline registers which can be configured as seven independent, 1-level pipelines; three independent, 2-level plus one 1-level pipelines; one 4-level plus one 3-level pipeline; or as one 7-level pipeline.

The Instruction pins, I_{3-0}, control the loading of the registers. The registers can be configured as a seven-stage delay line (eight-stage in the case of the LPR200) with data loaded into A and shifted sequentially through B, C, D, E, F, and G (and H in the case of the LPR200) as shown in Table 1. The Instruction pins may also be set to prevent any register from changing.

The Select lines, S_{2-0}, control an 8-to-1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allow simultaneous write and read operations on different registers.

5

LPR200/201 Block Diagram



SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers.

Inputs

D15-0 — Data Input

16-bit data input port. Data is latched into the registers on the rising edge of CLK.

Outputs

Y15-0 — Data Output

16-bit data output port.

Controls

I3-0 — Instruction Control

The instruction control pins select which register operation will be carried out. Refer to Tables 2 and 3.

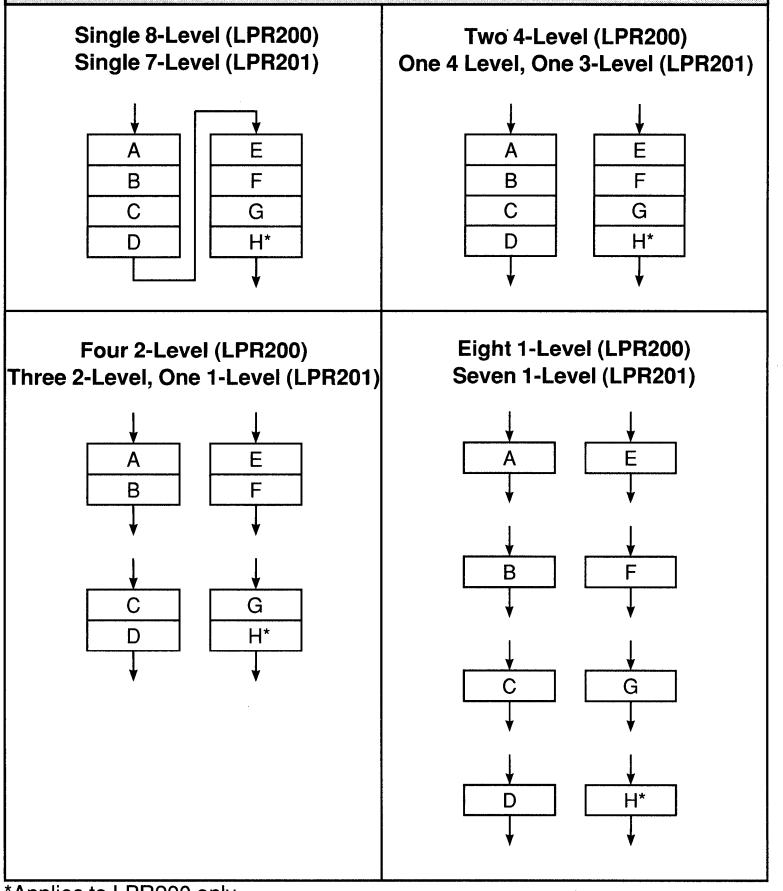
SEL2-0 — Output Select

The output select pins control which register contents will appear at the Y15-0 output pins. Refer to Tables 4 and 5.

$\overline{CEN}$ — Clock Enable

When $\overline{CEN}$ is LOW, the instruction designated by I3-0 is performed on the registers. When $\overline{CEN}$ is HIGH, no register operations are performed.

TABLE 1. REGISTER LOAD OPERATIONS



*Applies to LPR200 only

$\overline{OE}$ — Output Enable

When $\overline{OE}$ is LOW, the register data specified by SEL2-0 is available on the Y15-0 output pins. When $\overline{OE}$ is HIGH, the output port is in a high-impedance state.

TABLE 2. LPR200 INSTRUCTION TABLE

Mnemonics	Inputs I_3	I_2	I_1	I_0	Description
LDA	0	0	0	0	$D_{15-0} \rightarrow A$
LDB	0	0	0	1	$D_{15-0} \rightarrow B$
LDC	0	0	1	0	$D_{15-0} \rightarrow C$
LDD	0	0	1	1	$D_{15-0} \rightarrow D$
LDE	0	1	0	0	$D_{15-0} \rightarrow E$
LDF	0	1	0	1	$D_{15-0} \rightarrow F$
LDG	0	1	1	0	$D_{15-0} \rightarrow G$
LDH	0	1	1	1	$D_{15-0} \rightarrow H$
LSHAH	1	0	0	0	$D_{15-0} \rightarrow A$ $A \rightarrow B$ $B \rightarrow C$ $C \rightarrow D$ $D \rightarrow E$ $E \rightarrow F$ $F \rightarrow G$ $G \rightarrow H$
LSHAD	1	0	0	1	$D_{15-0} \rightarrow A$ $A \rightarrow B$ $B \rightarrow C$ $C \rightarrow D$
LSHEH	1	0	1	0	$D_{15-0} \rightarrow E$ $E \rightarrow F$ $F \rightarrow G$ $G \rightarrow H$
LSHAB	1	0	1	1	$D_{15-0} \rightarrow A$ $A \rightarrow B$
LSHCD	1	1	0	0	$D_{15-0} \rightarrow C$ $C \rightarrow D$
LSHEF	1	1	0	1	$D_{15-0} \rightarrow E$ $E \rightarrow F$
LSHGH	1	1	1	0	$D_{15-0} \rightarrow G$ $G \rightarrow H$
HOLD	1	1	1	1	ALL REGISTERS ON HOLD

TABLE 4. LPR200 OUTPUT SELECT

SEL_2	SEL_1	SEL_0	Y_{15-0}
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	H

TABLE 3. LPR201 INSTRUCTION TABLE

Mnemonics	Inputs I_3	I_2	I_1	I_0	Description
LDA	0	0	0	0	$D_{15-0} \rightarrow A$
LDB	0	0	0	1	$D_{15-0} \rightarrow B$
LDC	0	0	1	0	$D_{15-0} \rightarrow C$
LDD	0	0	1	1	$D_{15-0} \rightarrow D$
LDE	0	1	0	0	$D_{15-0} \rightarrow E$
LDF	0	1	0	1	$D_{15-0} \rightarrow F$
LDG	0	1	1	0	$D_{15-0} \rightarrow G$
HOLD	0	1	1	1	ALL REGISTERS ON HOLD
LSHAG	1	0	0	0	$D_{15-0} \rightarrow A$ $A \rightarrow B$ $B \rightarrow C$ $C \rightarrow D$ $D \rightarrow E$ $E \rightarrow F$ $F \rightarrow G$
LSHAD	1	0	0	1	$D_{15-0} \rightarrow A$ $A \rightarrow B$ $B \rightarrow C$ $C \rightarrow D$
LSHEG	1	0	1	0	$D_{15-0} \rightarrow E$ $E \rightarrow F$ $F \rightarrow G$
LSHAB	1	0	1	1	$D_{15-0} \rightarrow A$ $A \rightarrow B$
LSHCD	1	1	0	0	$D_{15-0} \rightarrow C$ $C \rightarrow D$
LSHEF	1	1	0	1	$D_{15-0} \rightarrow E$ $E \rightarrow F$
LDG	1	1	1	0	$D_{15-0} \rightarrow G$
HOLD	1	1	1	1	ALL REGISTERS ON HOLD

TABLE 5. LPR201 OUTPUT SELECT

SEL_2	SEL_1	SEL_0	Y_{15-0}
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	D_{15-0}

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +155°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output	–0.5 V to V_{CC} + 0.5 V
Output current into low outputs	50 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

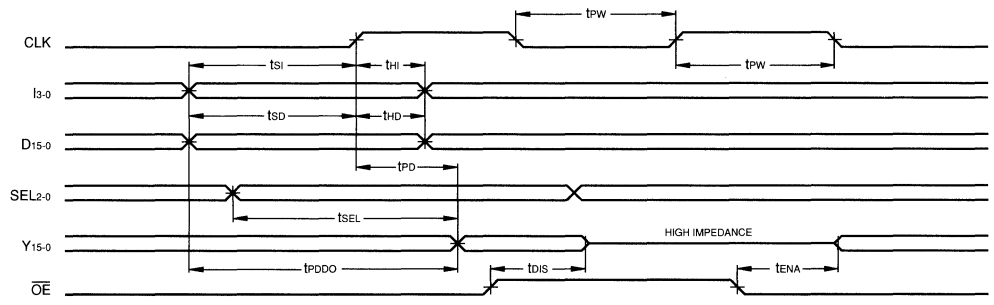
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –8.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 16 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	(Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)		2.0	10	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			12	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LPR200/201–							
		20		15		12		10	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
t_{CYC}	Cycle Time	20		15		12		10	
t_{PW}	Clock Pulse Width	5		5		5		5	
t_{PD}	Clock to Output Delay		20		15		12		10
t_{SEL}	Select to Output Delay		20		15		12		10
t_{PDDO}	Data In to Data Out Flowthrough Delay (LPR201)		20		15		12		10
t_{SI}	Instruction Setup Time	5		5		4		3	
t_{HI}	Instruction Hold Time	2		2		2		1.5	
t_{SD}	Data Setup Time	4		4		3		3	
t_{HD}	Data Hold Time	2		2		1		0	
t_{SC}	Clock Enable Setup Time	5		5		4		3	
t_{HC}	Clock Enable Hold Time	2		2		2		1.5	
t_{DIS}	Three-State Output Disable Delay (Note 11)		10		9		8		6
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		10		9		7

SWITCHING WAVEFORMS

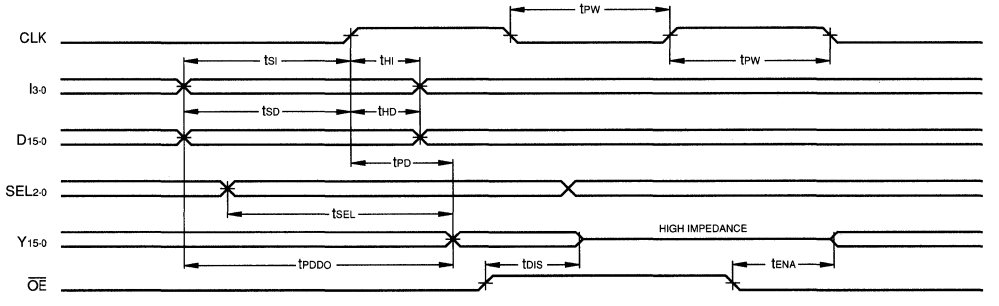


SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE (-55°C to +125°C) *Notes 9, 10 (ns)*

		LPR200/201–					
		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	20		15		12	
t_{PW}	Clock Pulse Width	6		5		5	
t_{PD}	Clock to Output Delay		20		15		12
t_{SEL}	Select to Output Delay		20		15		12
t_{PDDO}	Data In to Data Out Flowthrough Delay (LPR201)		20		15		12
t_{SI}	Instruction Setup Time	6		5		4	
t_{HI}	Instruction Hold Time	3		2		2	
t_{SD}	Data Setup Time	5		4		3	
t_{HD}	Data Hold Time	3		2		1	
t_{SC}	Clock Enable Setup Time	6		5		4	
t_{HC}	Clock Enable Hold Time	6		5		4	
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		9		8
t_{ENA}	Three-State Output Enable Delay (Note 11)		13		10		9

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 10 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 1. INPUT CIRCUIT

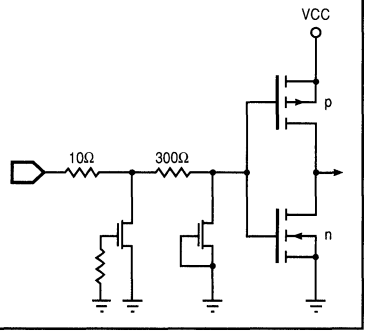


FIGURE 2. OUTPUT CIRCUIT

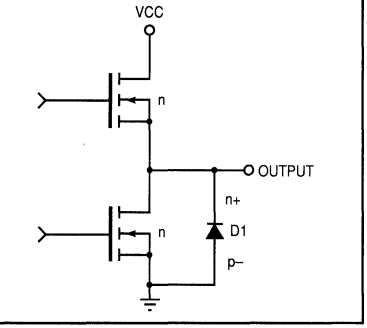
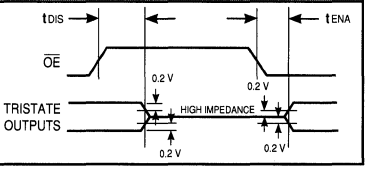
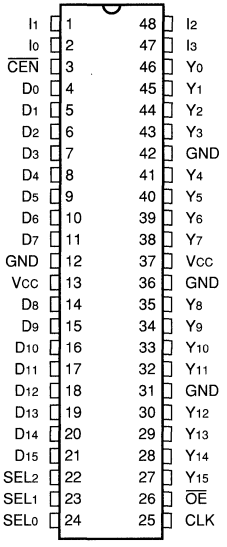


FIGURE 3. THRESHOLD LEVELS

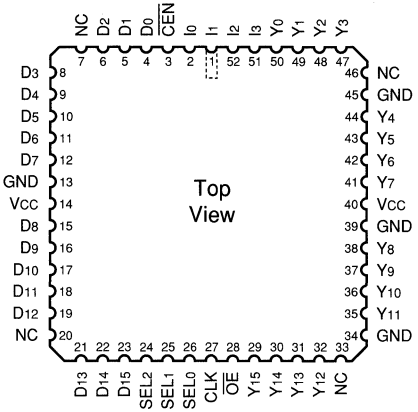


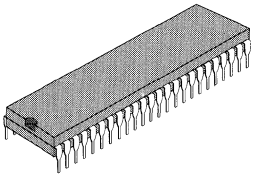
LPR200 — ORDERING INFORMATION

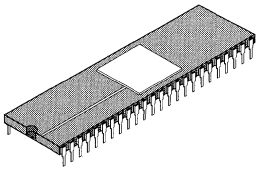
48-pin

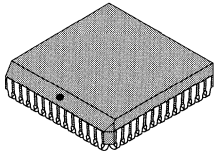


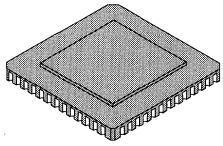
52-pin







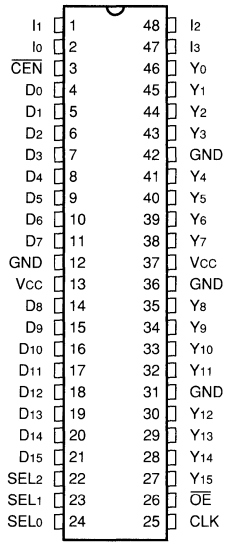




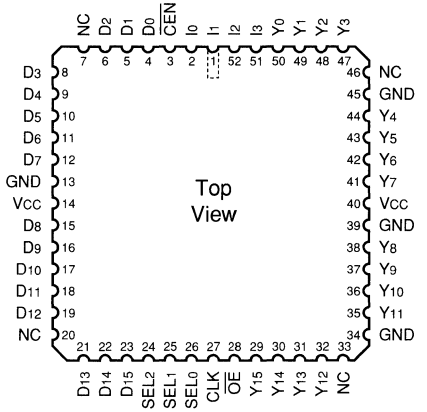
Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic Leaded Chip Carrier (J5)	Ceramic Leadless Chip Carrier (K10)
	0°C to +70°C — Commercial Screening			
20 ns	LPR200PC20	LPR200DC20	LPR200JC20	LPR200KC20
15 ns	LPR200PC15	LPR200DC15	LPR200JC15	LPR200KC15
12 ns	LPR200PC12	LPR200DC12	LPR200JC12	LPR200KC12
10 ns	LPR200PC10	LPR200DC10	LPR200JC10	LPR200KC10
	–55°C to +125°C — Commercial Screening			
20 ns		LPR200DM20		LPR200KM20
15 ns		LPR200DM15		LPR200KM15
12 ns		LPR200DM12		LPR200KM12
	–55°C to +125°C — MIL-STD-883 Compliant			
20 ns		LPR200DMB20		LPR200KMB20
15 ns		LPR200DMB15		LPR200KMB15
12 ns		LPR200DMB12		LPR200KMB12

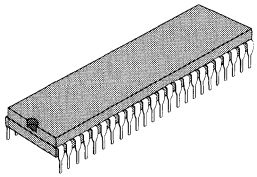
LPR201 — ORDERING INFORMATION

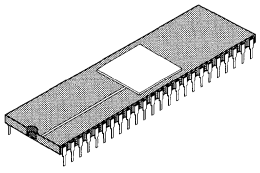
48-pin

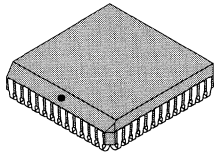


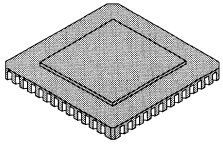
52-pin











Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic Leaded Chip Carrier (J5)	Ceramic Leadless Chip Carrier (K10)
	0°C to +70°C — Commercial Screening			
20 ns	LPR201PC20	LPR201DC20	LPR201JC20	LPR201KC20
15 ns	LPR201PC15	LPR201DC15	LPR201JC15	LPR201KC15
12 ns	LPR201PC12	LPR201DC12	LPR201JC12	LPR201KC12
10 ns	LPR201PC10	LPR201DC10	LPR201JC10	LPR201KC10
	–55°C to +125°C — Commercial Screening			
20 ns		LPR201DM20		LPR201KM20
15 ns		LPR201DM15		LPR201KM15
12 ns		LPR201DM12		LPR201KM12
	–55°C to +125°C — MIL-STD-883 Compliant			
20 ns		LPR201DMB20		LPR201KMB20
15 ns		LPR201DMB15		LPR201KMB15
12 ns		LPR201DMB12		LPR201KMB12

5

L29C524/525
Dual Pipeline Register

FEATURES

- Pipeline Registers — Dual 7-Deep (L29C524) or Dual 8-Deep (L29C525)
- Configurable to Single 14-Deep and Single 16-Deep
- Low Power CMOS Technology
- Replaces AMD Am29524 and Am29525
- Load, Shift, and Hold Instructions
- Separate Data In and Data Out Pins
- Three-State Outputs
- DESC SMD No. 5962-91696
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Sidebraze, Hermetic DIP
  - 28-pin Ceramic Flatpack
  - 28-pin Plastic LCC, J-Lead

DESCRIPTION

The **L29C524** and **L29C525** are high-speed, low power CMOS pipeline registers. They are pin-for-pin compatible with the AMD Am29524 and Am29525. The products can be configured as two independent 7-level (or 8-level) pipelines or as single 14-level (or 16-level) pipeline. The configuration implemented is determined by the instruction code (I_{1-0}) as shown in Table 2.

The I_{1-0} instruction code controls the internal routing of data and loading of each register. For instruction I_{1-0} = 00 (Push A and B), data applied at the D_{7-0} inputs is latched into register A0 on the rising edge of CLK. The contents of A0 simultaneously move to register A1, A1 moves to A2, and so on. The contents of the last register on the A side (A6 for the L29C524, A7 for the L29C525) are wrapped back to register B0. The registers on the B side are similarly shifted, with the contents of the last register on the B side (B6 for the L29C524, B7 for the L29C525) lost.

Instruction I_{1-0} = 01 (Push B) acts similarly to the Push A and B instruction, except that only the B side registers are shifted. The input data is applied to register B0, and the contents of the last register on the B side (B6 for the L29C524, B7 for the L29C525) are lost. The contents of the A side registers are unaffected. Instruction I_{1-0} = 10 (Push A) is identical to the Push B instruction, except that the A side registers are shifted and the B side registers are unaffected.

Instruction I_{1-0} = 11 (Hold) causes no internal data movement. It is equivalent to preventing the application of a clock edge to any internal register.

The contents of any of the registers is selectable at the output through the use of the S_{3-0} control inputs. On the L29C524, the input pins D_{7-0} may also be selected to drive the output, and all output pins may be forced to zero. The independence of the I and S control lines allows simultaneous reading and writing. Encoding for the S_{3-0} controls is given in Table 3.

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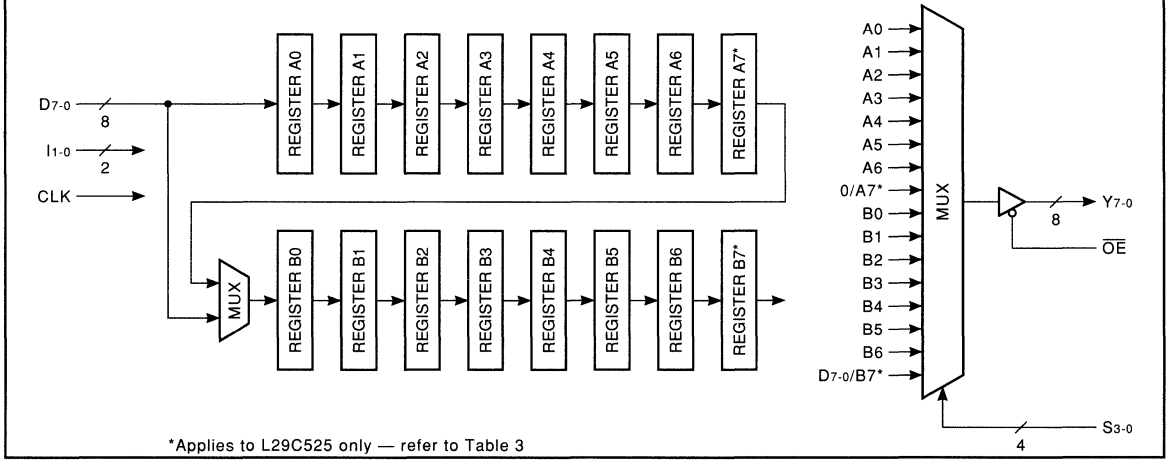
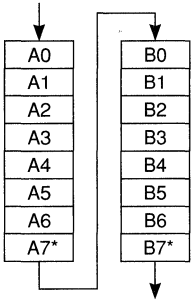
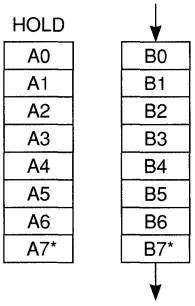
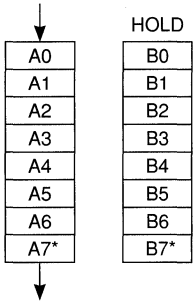
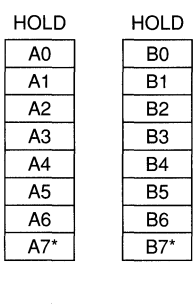
L29C524/525 Block Diagram



*Applies to L29C525 only — refer to Table 3

TABLE 1. REGISTER LOAD OPERATIONS

Single 14/16 Level	Dual 7/8 Level		
Push A and B	**Push B**	**Push A**	**Hold All Registers**
			

*Applies to L29C525 only

TABLE 2. INSTRUCTION SET

	Inputs		
Mnemonics	**I_1**	**I_0**	**Description**
Shift	0	0	Push A and B
LDB	0	1	Push B
LDA	1	0	Push A
HLD	1	1	Hold All Registers

TABLE 3. OUTPUT SELECT

S_3	S_2	S_1	S_0	Y_{7-0}
0	0	0	0	A0
0	0	0	1	A1
0	0	1	0	A2
0	0	1	1	A3
0	1	0	0	A4
0	1	0	1	A5
0	1	1	0	A6
0	1	1	1	0 (L29C524) A7 (L29C525)
1	0	0	0	B0
1	0	0	1	B1
1	0	1	0	B2
1	0	1	1	B3
1	1	0	0	B4
1	1	0	1	B5
1	1	1	0	B6
1	1	1	1	D_{7-0} (L29C524) B7 (L29C525)

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –12 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	35	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

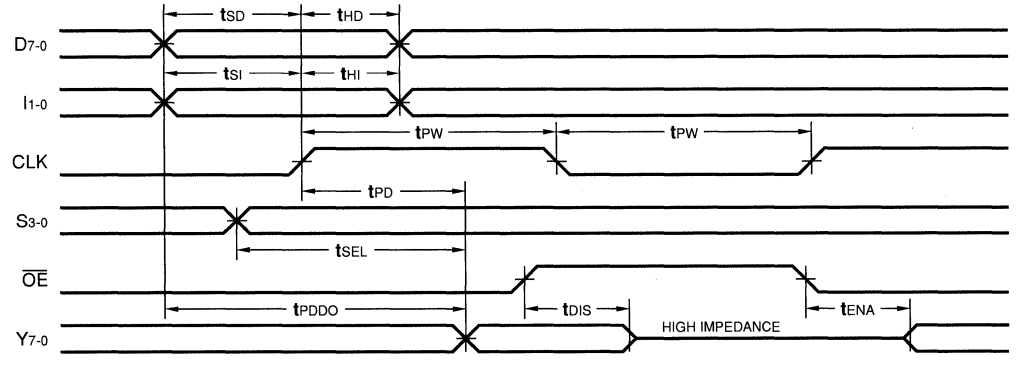
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C524/525–			
		20		15	
Symbol	Parameter	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		20		15
t_{SEL}	Select to Output Delay		20		15
t_{PDDO}	Data to Output Delay (L29C524)		20		15
t_{PW}	Clock Pulse Width	12		10	
t_{SD}	Data Setup Time	7		5	
t_{HD}	Data Hold Time	0		0	
t_{SI}	Instruction Setup Time	7		5	
t_{HI}	Instruction Hold Time	2		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		13

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C524/525–			
		25		20	
Symbol	Parameter	Min	Max	Min	Max
t_{PD}	Clock to Output Delay		25		20
t_{SEL}	Select to Output Delay		25		20
t_{PDDO}	Data to Output Delay (L29C524)		25		20
t_{PW}	Clock Pulse Width	12		12	
t_{SD}	Data Setup Time	7		7	
t_{HD}	Data Hold Time	2		2	
t_{SI}	Instruction Setup Time	7		7	
t_{HI}	Instruction Hold Time	2		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15
t_{DIS}	Three-State Output Disable Delay (Note 11)		13		13

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

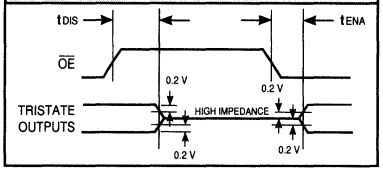
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 1. THRESHOLD LEVELS



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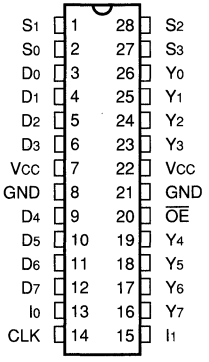
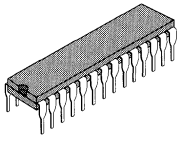
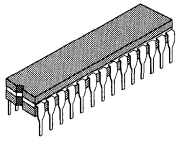
L29C524 — ORDERING INFORMATION

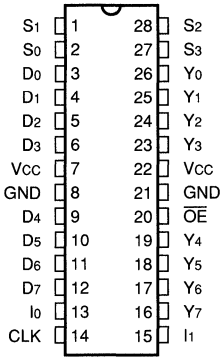
28-pin — 0.3" wide

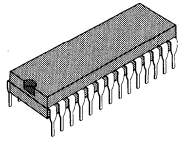


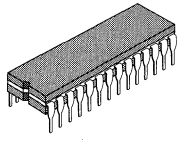




28-pin — 0.4" wide



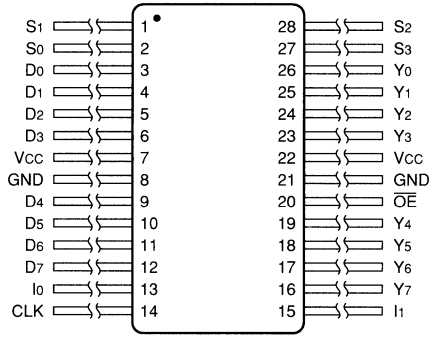


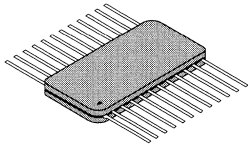


Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic DIP (P11)	Ceramic DIP (C10)
	0°C to +70°C — COMMERCIAL SCREENING			
20 ns	L29C524PC20	L29C524CC20	L29C524NC20	L29C524IC20
15 ns	L29C524PC15	L29C524CC15	L29C524NC15	L29C524IC15
	–55°C to +125°C — COMMERCIAL SCREENING			
25 ns		L29C524CM25		L29C524IM25
20 ns		L29C524CM20		L29C524IM20
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
25 ns		L29C524CMB25		L29C524IMB25
20 ns		L29C524CMB20		L29C524IMB20

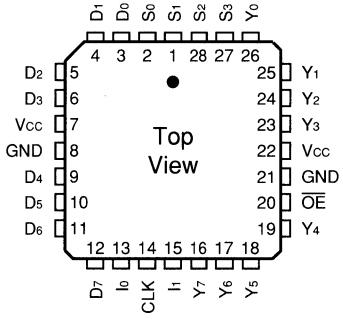
L29C524 — ORDERING INFORMATION

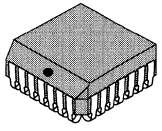
28-pin





28-pin





Speed	Ceramic Flatpack (M2)	Plastic J-Lead Chip Carrier (J4)
	0°C to +70°C — COMMERCIAL SCREENING	
20 ns	L29C524MC20	L29C524JC20
15 ns	L29C524MC15	L29C524JC15
	–55°C to +125°C — COMMERCIAL SCREENING	
25 ns	L29C524MM25	
20 ns	L29C524MM20	
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
25 ns	L29C524MMB25	
20 ns	L29C524MMB20	

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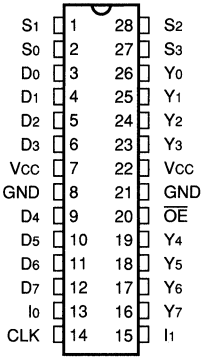
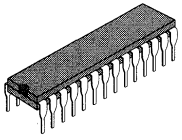
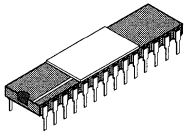
L29C525 — ORDERING INFORMATION

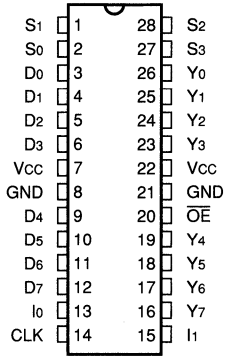
28-pin — 0.3" wide

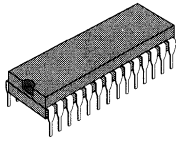


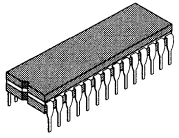




28-pin — 0.4" wide



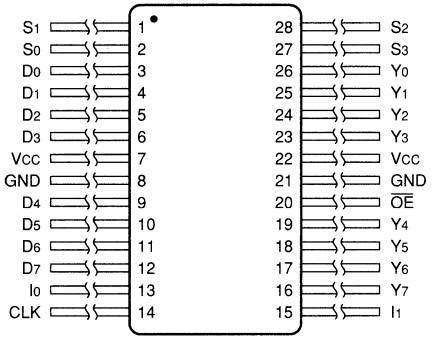


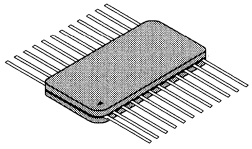


Speed	Plastic DIP (P10)	Sidebraze Hermetic DIP (D10)	Plastic DIP (P11)	Ceramic DIP (C10)
	0°C to +70°C — COMMERCIAL SCREENING			
20 ns	L29C525PC20	L29C525DC20	L29C525NC20	L29C525IC20
15 ns	L29C525PC15	L29C525DC15	L29C525NC15	L29C525IC15
	–55°C to +125°C — COMMERCIAL SCREENING			
25 ns		L29C525DM25		L29C525IM25
20 ns		L29C525DM20		L29C525IM20
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
25 ns		L29C525DMB25		L29C525IMB25
20 ns		L29C525DMB20		L29C525IMB20

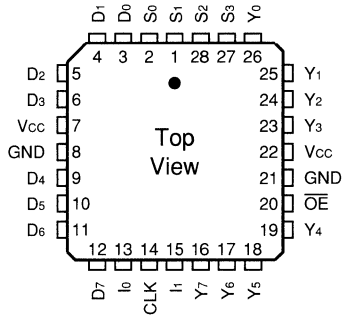
L29C525 — ORDERING INFORMATION

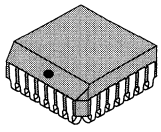
28-pin





28-pin





Speed	Ceramic Flatpack (M2)	Plastic J-Lead Chip Carrier (J4)
	0°C to +70°C — COMMERCIAL SCREENING	
20 ns	L29C525MC20	L29C525JC20
15 ns	L29C525MC15	L29C525JC15
	–55°C to +125°C — COMMERCIAL SCREENING	
25 ns	L29C525MM25	
20 ns	L29C525MM20	
	–55°C to +125°C — MIL-STD-883 COMPLIANT	
25 ns	L29C525MMB25	
20 ns	L29C525MMB20	

5

LOGIC DEVICES INCORPORATED

L10C11
4/8-bit Variable Length Shift Register

FEATURES

- Variable Length 4 or 8-bit Wide Shift Register
- Selectable Delay Length from 3 to 18 Stages
- Low Power CMOS Technology
- Replaces TRW/Raytheon TMC2011
- Load, Shift, and Hold Instructions
- Separate Data In and Data Out Pins
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Ceramic DIP
  - 28-pin Plastic LCC, J-Lead

DESCRIPTION

The **L10C11** is a high-speed, low power CMOS variable length shift register. The L10C11 consists of two 4-bit wide, adjustable length shift registers. These registers share control signals and a common clock. Both shift registers can be programmed together to any length from 3 to 18 stages inclusive, or one register can be fixed at 18 stages of delay while the other is variable. The configuration implemented is determined by the Length Code (L_{3-0}) and the MODE control line as shown in Table 1.

Each input is applied to a chain of registers which are clocked on the rising edge of the common CLK input. These registers are numbered R1 through R17 and R1′ through R17′, corresponding to the D_{3-0} and D_{7-4} data fields respectively. A multiplexer serves to route the contents of any of registers R2 through R17 to the output register, denoted R18. A similar multiplexer operates on the contents of R2′ through R17′ to load R18′. Note that the minimum-length path from data inputs to outputs is R1 to R2 to R18, consisting of three stages of delay.

The MODE input determines whether one or both of the internal shift registers have variable length. When MODE = 0, both D_{3-0} and D_{7-4} are delayed by an amount which is controlled by L_{3-0}. When MODE = 1, the D_{7-4} field is delayed by 18 stages independent of L_{3-0}.

The Length Code (L_{3-0}) controls the number of stages of delay applied to the D inputs as shown in Table 1. When the Length Code is 0, the inputs are delayed by 3 clock periods. When the Length Code is 1, the delay is 4 clock periods, and so forth. The Length Code and MODE inputs are latched on the rising edge of CLK. Both the Length Code and MODE values may be changed at any time without affecting the contents of registers R1 through R17 or R1′ through R17′.

5

L10C11 Block Diagram

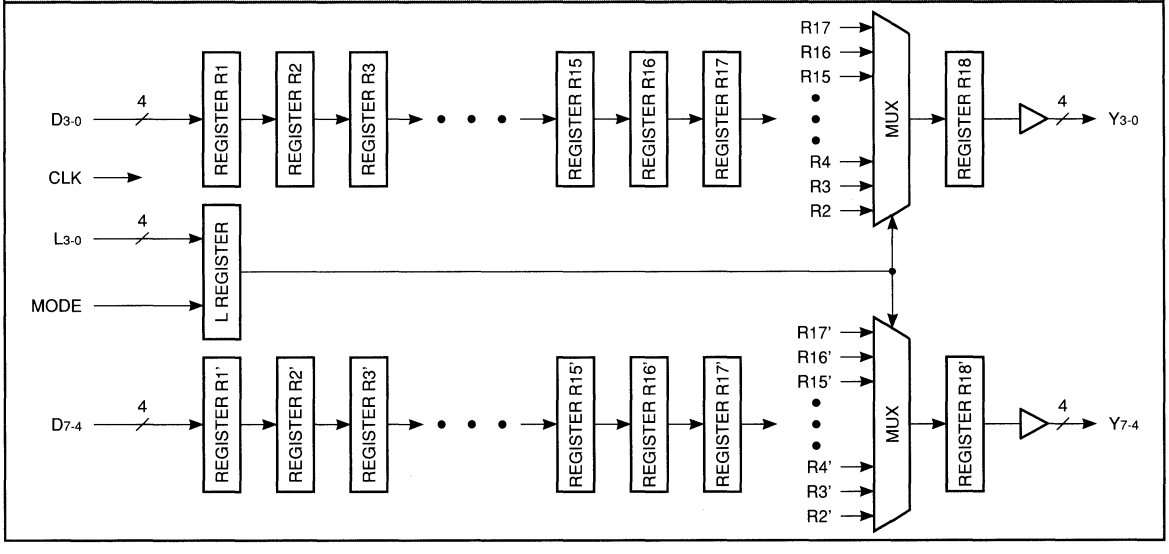


Table 1. Control Encoding

Length Code				Mode = 0		Mode = 1	
				Delay		Delay	
L_3	L_2	L_1	L_0	Y_{3-0}	Y_{7-4}	Y_{3-0}	Y_{7-4}
0	0	0	0	3	3	3	18
0	0	0	1	4	4	4	18
0	0	1	0	5	5	5	18
0	0	1	1	6	6	6	18
0	1	0	0	7	7	7	18
0	1	0	1	8	8	8	18
0	1	1	0	9	9	9	18
0	1	1	1	10	10	10	18
1	0	0	0	11	11	11	18
1	0	0	1	12	12	12	18
1	0	1	0	13	13	13	18
1	0	1	1	14	14	14	18
1	1	0	0	15	15	15	18
1	1	0	1	16	16	16	18
1	1	1	0	17	17	17	18
1	1	1	1	18	18	18	18

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2, 3, 8)

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions

To meet specified electrical and switching characteristics

Mode	Temperature Range	Supply Voltage
Active Operation, Com.	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Mil.	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = −12 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	20	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS

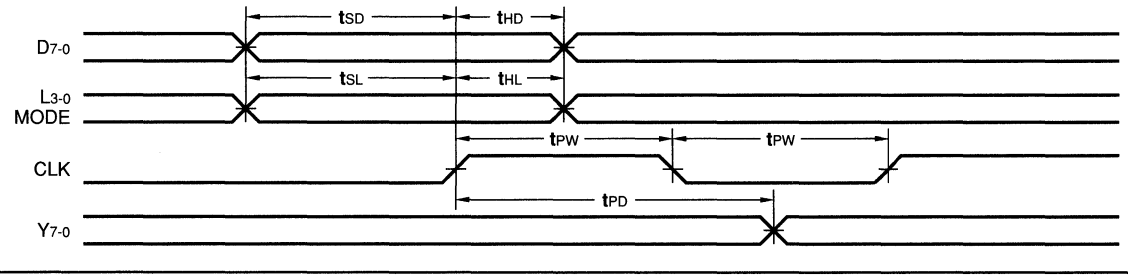
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L10C11–					
		25		20		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Output Delay		25		20		15
t_{PW}	Clock Pulse Width	15		12		10	
t_{SD}	Data Setup Time	20		10		8	
t_{HD}	Data Hold Time	2		0		0	
t_{SL}	L_{3-0}, MODE Setup Time	20		10		8	
t_{HL}	L_{3-0}, MODE Hold Time	2		0		0	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L10C11–					
		30		25		20	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{PD}	Output Delay		30		25		20
t_{PW}	Clock Pulse Width	15		12		12	
t_{SD}	Data Setup Time	25		10		10	
t_{HD}	Data Hold Time	2		2		0	
t_{SL}	L_{3-0}, MODE Setup Time	25		10		10	
t_{HL}	L_{3-0}, MODE Hold Time	2		2		0	

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

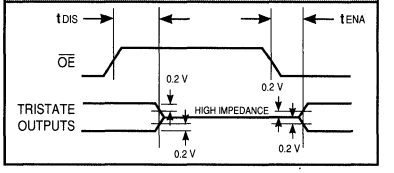
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

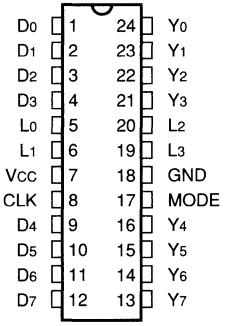
12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

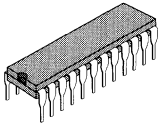
FIGURE 1. THRESHOLD LEVELS

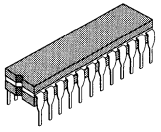


ORDERING INFORMATION

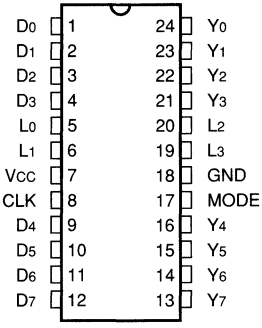
24-pin — 0.3" wide

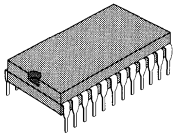


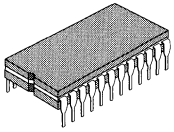




24-pin — 0.6" wide





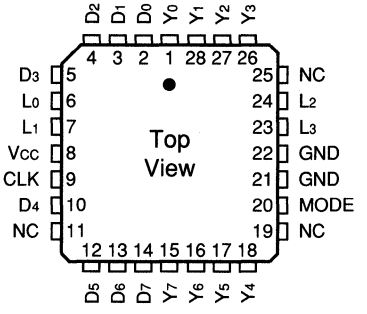


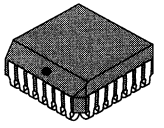
Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Plastic DIP (P1)	Ceramic DIP (C4)
	0°C to +70°C — Commercial Screening			
25 ns	L10C11PC25	L10C11CC25	L10C11NC25	L10C11IC25
20 ns	L10C11PC20	L10C11CC20	L10C11NC20	L10C11IC20
15 ns	L10C11PC15	L10C11CC15	L10C11NC15	L10C11IC15
	–55°C to +125°C — Commercial Screening			
30 ns		L10C11CM30		L10C11IM30
25 ns		L10C11CM25		L10C11IM25
20 ns		L10C11CM20		L10C11IM20
	–55°C to +125°C — MIL-STD-883 Compliant			
30 ns		L10C11CMB30		L10C11IMB30
25 ns		L10C11CMB25		L10C11IMB25
20 ns		L10C11CMB20		L10C11IMB20

5

ORDERING INFORMATION

28-pin





Speed	Plastic J-Lead Chip Carrier (J4)	
	0°C to +70°C — COMMERCIAL SCREENING	
25 ns	L10C11JC25	
20 ns	L10C11JC20	
15 ns	L10C11JC15	
	–55°C to +125°C — COMMERCIAL SCREENING	
	–55°C to +125°C — MIL-STD-883 COMPLIANT	

LRF07
8 x 8-bit Register File (3-Port)

FEATURES

- 8-word x 8-bit Three-Port Memory
- Independently Addressable Ports: 1 Input, 1 Output, 1 Bidirectional
- Low Power CMOS Technology
- Internally Latched Control Bits
- High-Speed Scratchpad Memory with Overlapped Data Fetch/Store
- Fully TTL Compatible
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40-pin Plastic DIP
  - 40-pin Ceramic DIP
  - 44-pin Ceramic LCC

DESCRIPTION

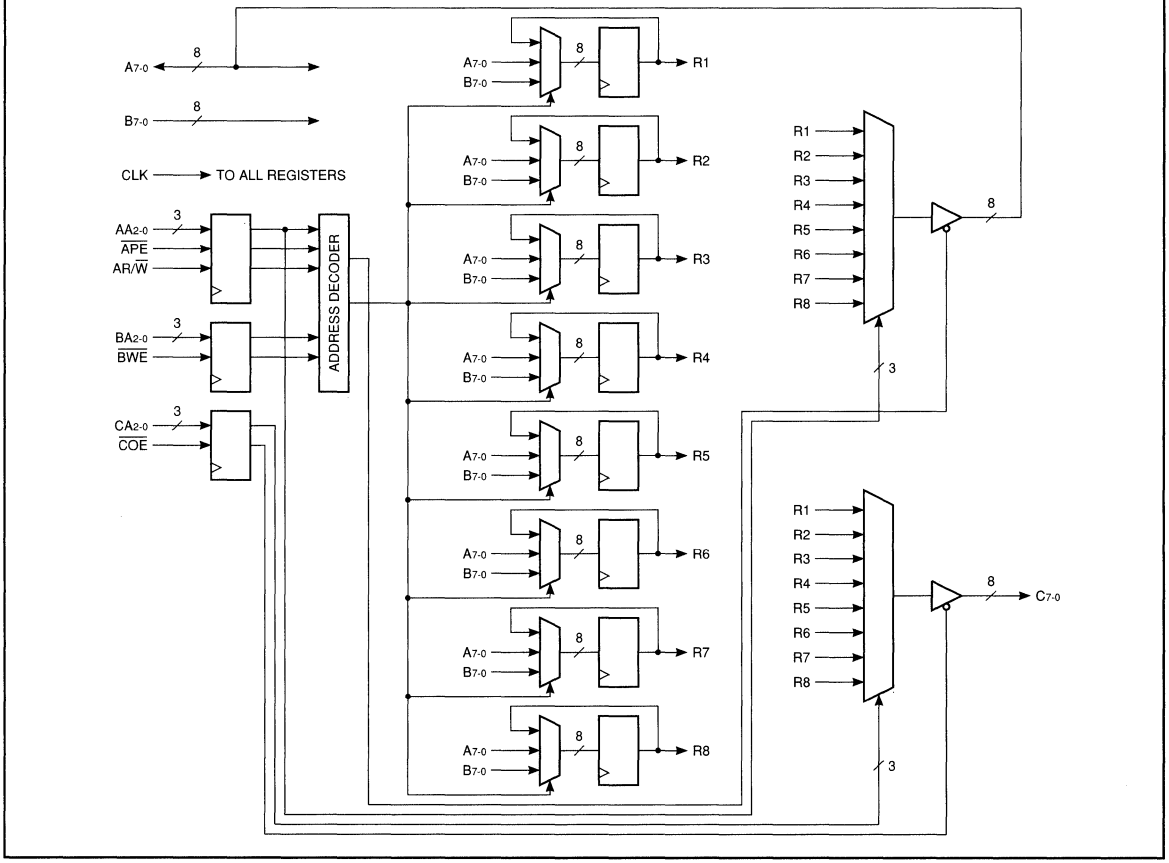
The **LRF07** is an 8-word x 8-bit expandable register file with three independently addressable ports, designated A, B, and C. Each port has eight data lines, three address lines, and a port enable control. All address and control lines are registered to facilitate instruction pipelining in microprogrammed systems. All ports may be used simultaneously in any clock cycle.

The C port is a read only port. C port address lines (CA_{2-0}) are latched on the rising edge of CLK. The data indicated by the port address will be presented on the output lines one t_{ACC} following the rising clock edge on which the address is latched. If the same register is simultaneously addressed for writing from a different port, the data presented to the outputs is the contents of the register prior to the write operation.

The B port is a write port. B port address lines (BA_{2-0}) are latched on the rising edge of CLK. The contents of the B address register are decoded to control data routing multiplexers.

5

LRF07 Block Diagram



These supply data from the input pins to the desired register. The input data is latched into the addressed register on the rising clock edge following the one which latched the address.

The A port is a bidirectional port. The A READ/$\overline{\text{WRITE}}$ (AR/$\overline{\text{W}}$) control is latched along with the address lines (AA_{2-0}) and determines whether the A port acts as an input or an output during any clock period. When AR/$\overline{\text{W}}$ is HIGH at the rising clock edge, the A port presents the addressed data on the A_{7-0} data lines.

Read operations on the A port are performed identically to C port reads. When AR/$\overline{\text{W}}$ is LOW at the rising clock edge, an A port write operation is executed in the same manner as a B port write. The input data is latched on the rising clock edge following the one which latched the address.

All ports have associated port enable inputs. These inputs are internally registered and are applied simultaneously with the corresponding port address. In the case of the C port, the $\overline{\text{COE}}$ input is a three-state output control. A HIGH latched in this input places C_{7-0} in a high impedance state beginning one t_{DIS} following the rising clock edge that latched $\overline{\text{COE}}$. The B port enable $\overline{\text{BWE}}$ serves as a registered write enable input. A HIGH latched in this input disables write operations from the port on the following rising clock edge. The A port enable $\overline{\text{APE}}$, serves the dual function of write enable or three-state enable depending on the direction of the A port.

Maximum Ratings *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

Electrical Characteristics *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			2.0	mA

SWITCHING CHARACTERISTICS

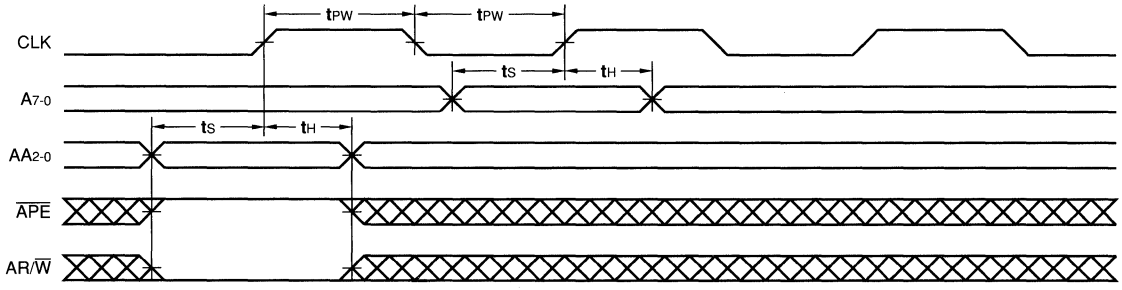
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LRF07–			
		35		20	
Symbol	Parameter	Min	Max	Min	Max
t_{ACC}	Output Delay		35		20
t_{PW}	Clock Pulse Width	25		12	
t_S	Input Setup Time	15		7	
t_H	Input Hold Time	5		0	
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		20
t_{DIS}	Three-State Output Disable Delay (Note 11)		25		15

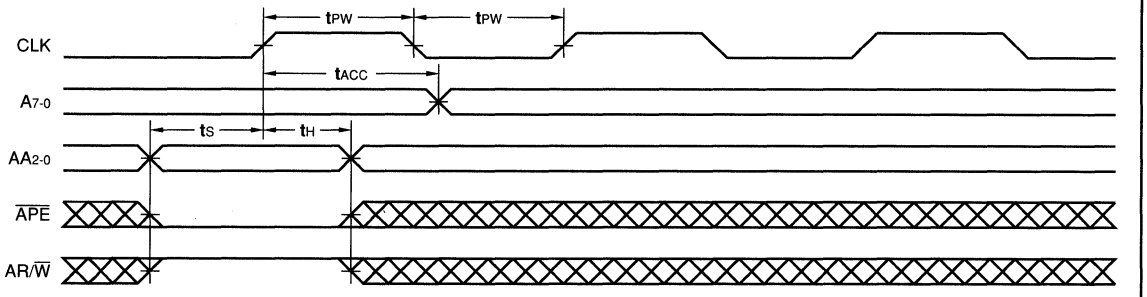
MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LRF07–			
		40		25	
Symbol	Parameter	Min	Max	Min	Max
t_{ACC}	Output Delay		40		25
t_{PW}	Clock Pulse Width	25		15	
t_S	Input Setup Time	15		10	
t_H	Input Hold Time	5		0	
t_{ENA}	Three-State Output Enable Delay (Note 11)		35		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		30		20

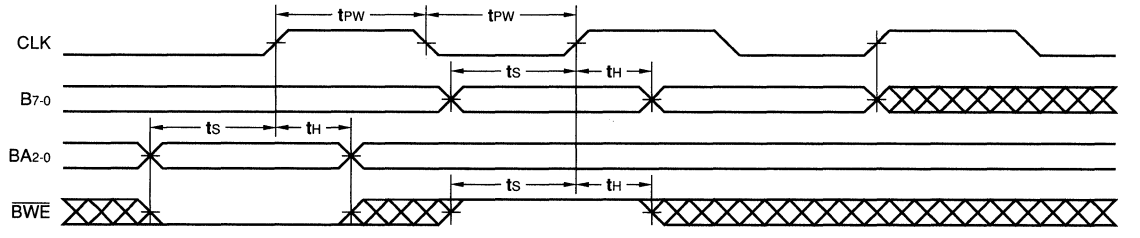
SWITCHING WAVEFORMS: PORT A WRITE OPERATION



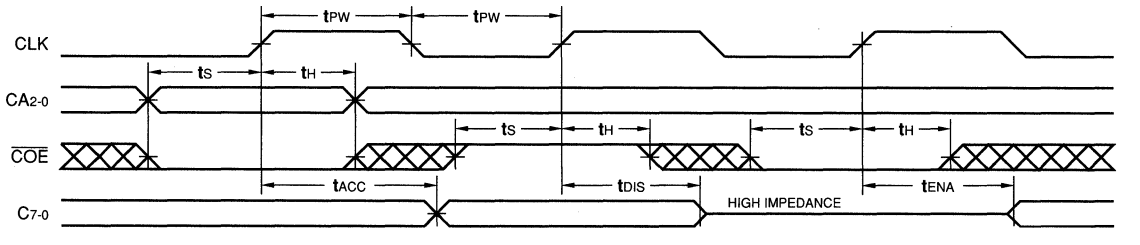
Switching Waveforms: Port A Read Operation



Switching Waveforms: Port B Write Operation



Switching Waveforms: Port C Read Operation



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

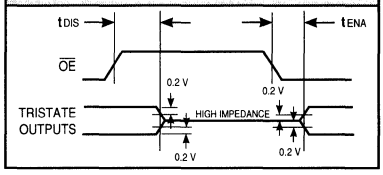
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 1. THRESHOLD LEVELS



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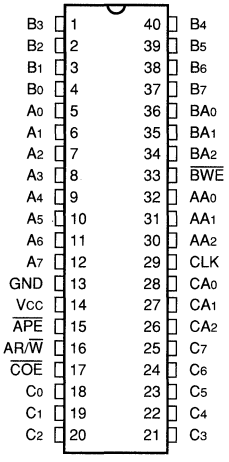
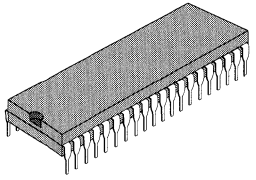
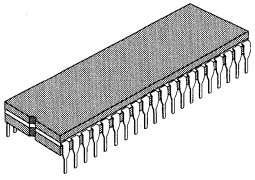
ORDERING INFORMATION

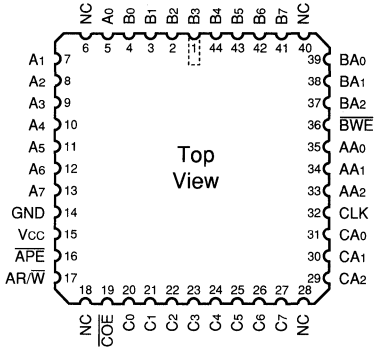
40-pin — 0.6" wide

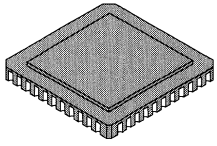






44-pin





Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — Commercial Screening		
35 ns	LRF07PC35	LRF07CC35	LRF07KC35
20 ns	LRF07PC20	LRF07CC20	LRF07KC20
	–55°C to +125°C — Commercial Screening		
40 ns		LRF07CM40	LRF07KM40
25 ns		LRF07CM25	LRF07KM25
	–55°C to +125°C — MIL-STD-883 Compliant		
40 ns		LRF07CMB40	LRF07KMB40
25 ns		LRF07CMB25	LRF07KMB25

L29C818
8-bit Serial Scan Shadow Register

FEATURES

- Octal Register with Additional 8-bit Shiftable Shadow Register
- Serial Load/Verify of Writable Control Store RAM
- Serial Stimulus/Observation of Sequential Logic
- High-Speed, Low Power CMOS Technology
- Replaces AMD Am29818
- DESC SMD No. 5962-90515
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Ceramic DIP
  - 28-pin Ceramic LCC

DESCRIPTION

The **L29C818** is a high-speed octal register designed especially for applications using serial-scan diagnostics or writable control store. It is pin and functionally compatible with the AMD Am29818 bipolar device.

The L29C818 consists of an octal register, the P register, internally connected to an 8-bit shift register, the S register. Each has its own corresponding clock pin and the P register has a three-state output control.

An input control signal, MODE, in combination with the S register serial data input (SDI) pin controls data routing within the L29C818. When the MODE input is LOW, indicating normal operation, data present on the D_{7-0} pins is loaded into the P register on the rising edge of CLK P. The contents of the P register are visible on the output pins Y_{7-0} when the $\overline{OE}$ control line is LOW.

Also, data present on the SDI pin is loaded into the least significant position of the S register on the rising edge of CLK S. In this mode, the S register performs a right-shift operation with the contents of each bit position replaced by the value in the next least significant location. The value in S_7 is shifted out on the serial data output (SDO) pin. The SDI and SDO pins allow serial connection of multiple L29C818 devices into a diagnostic loop. When MODE is LOW, the operation of the P and S registers are completely independent and no timing relationship is enforced between CLK P and CLK S.

When MODE is HIGH, the internal multiplexers route data between the S and P registers and the Y port. The contents of the S register are loaded into the P register on the rising edge of

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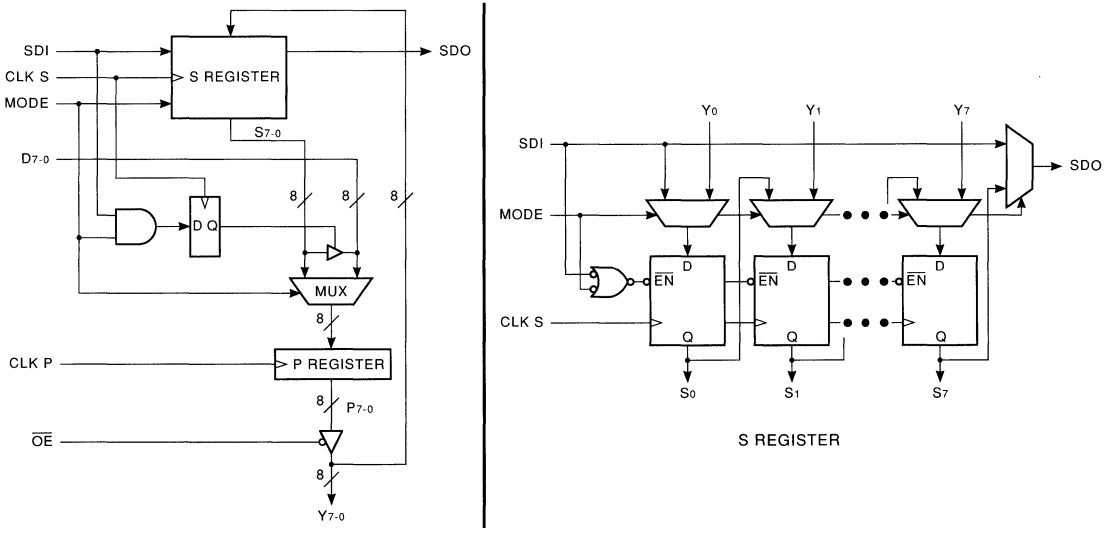
L29C818 Block Diagram



CLK P. In diagnostic applications, this allows a data value input via serial scan to be loaded into the active data path of the machine.

When the MODE pin is HIGH, CLK S causes a parallel, rather than serial, load of the S register. In this mode, the S register is loaded from the Y_{7-0} pins at the rising edge of CLK S. This is useful in writable control store applications for read-back of the control store via the serial path.

When MODE is HIGH, the SDI pin is used as a control input to enable or disable the loading of the S register. It also affects routing of the S register contents onto the D_{7-0} outputs. When SDI is LOW, the S register is enabled for loading as above. When SDI is HIGH however, CLK S is prevented from reaching the S register and no load occurs. In order to allow the SDI pin to serve as an enable signal for all L29C818 devices in a serial configuration, special handling of the SDI input is required. When MODE is HIGH, the SDI input drives the SDO output directly, bypassing the S register. This means that the SDI value will apply simultaneously to all L29C818s in a serial loop. However, to ensure proper operation of a given device, the user must ensure that the SDI setup time to CLK S is extended by the sum of the SDI to SDO delays of all previous devices in the serial path.

The D_{7-0} port is normally used as the input port to the D register. For writable control store applications however, this port is connected to the I/O pins of the RAM used as a control store. In order to load this RAM through the serial path, it is necessary to drive the S register contents onto the D_{7-0} pins. This is accomplished when MODE and SDI are HIGH and a CLK S rising edge occurs. Note from above that with SDI HIGH, no loading of the S register occurs. However, a flip-flop is set which synchronously enables the D port output buffer. The D output remains enabled until the first rising edge of CLK S during which either SDI or MODE is LOW. Thus to load a control store RAM, data would be shifted in with MODE LOW. When an entire control store word is present in the serial S registers, the SDI and MODE pins are brought HIGH for one or more cycles, preventing further shifting of the S registers and enabling the contents onto the D port for writing into the RAM.

To verify the contents of a control store RAM, the RAM is read into the D register in the normal fashion. Then, the D contents are transferred in parallel to the S register by driving MODE HIGH with SDI LOW. The S register contents are then scanned out serially by returning MODE LOW and applying CLK S pulses.

TABLE 1. FUNCTION TABLE

Inputs				Outputs		Action		
MODE	SDI	CLK S	CLK P	P REG	S REG	Y_{7-0}	D_{7-0}	SDO
0	X	⎍	X	N/A	SHIFT	Normal	HI-Z	S_7
0	X	X	⎍	LOAD D	N/A	Normal	Input	S_7
1	0	⎍	X	N/A	LOAD Y	Input*	HI-Z	SDI
1	1	⎍	X	N/A	HOLD	Normal	Output	SDI
1	X	X	⎍	LOAD S	N/A	Normal	HI-Z	SDI

*If $\overline{OE}$ is LOW, the P register value will be loaded into the S register. If $\overline{OE}$ is HIGH, a value may be applied externally to the Y_{7-0} pins.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

5

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –12.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±20	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	15	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS — NORMAL REGISTER OPERATION

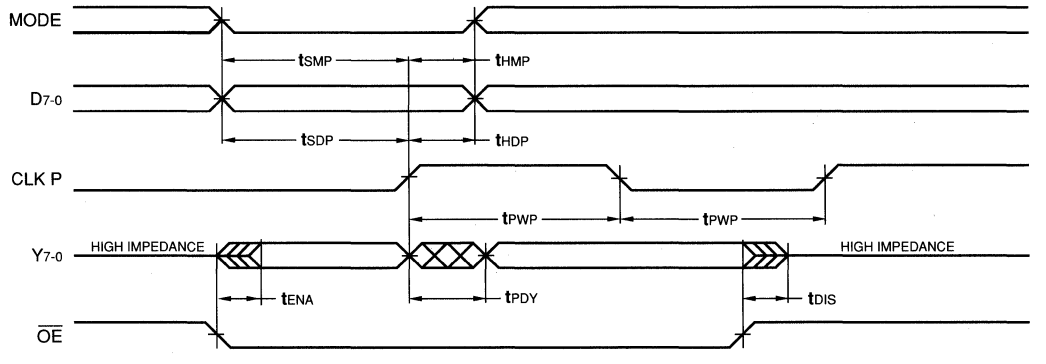
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C818–			
		25		15	
Symbol	Parameter	Min	Max	Min	Max
t_{PWP}	CLK P Pulse Width	15		10	
t_{PDY}	CLK P to Y_{7-0}		13		9
t_{SDP}	D_{7-0} to CLK P Setup Time	8		6	
t_{HDP}	CLK P to D_{7-0} Hold Time	2		2	
t_{SMP}	MODE to CLK P Setup Time	15		15	
t_{HMP}	CLK P to MODE Hold Time	2		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		25		25
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C818–			
		30		24	
Symbol	Parameter	Min	Max	Min	Max
t_{PWP}	CLK P Pulse Width	15		15	
t_{PDY}	CLK P to Y_{7-0}		18		12
t_{SDP}	D_{7-0} to CLK P Setup Time	10		8	
t_{HDP}	CLK P to D_{7-0} Hold Time	2		2	
t_{SMP}	MODE to CLK P Setup Time	15		15	
t_{HMP}	CLK P to MODE Hold Time	2		2	
t_{ENA}	Three-State Output Enable Delay (Note 11)		30		30
t_{DIS}	Three-State Output Disable Delay (Note 11)		20		20

SWITCHING WAVEFORMS — NORMAL REGISTER OPERATION



SWITCHING CHARACTERISTICS — SERIAL SHIFT OPERATION

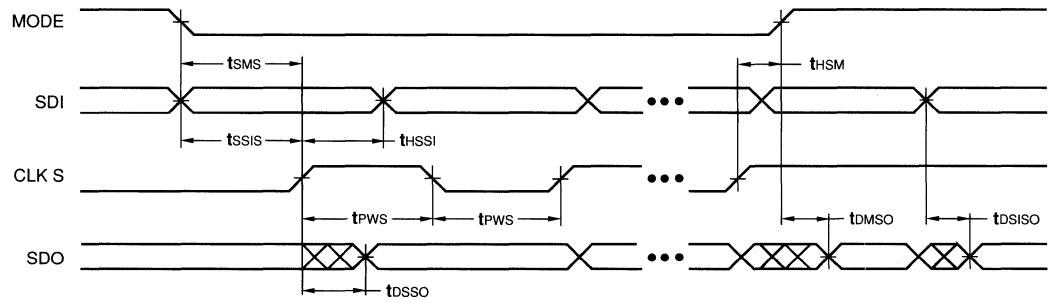
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C818–			
		25		15	
Symbol	Parameter	Min	Max	Min	Max
t_{PWS}	CLK S Pulse Width	25		15	
t_{DSSO}	CLK S to SDO		25		25
t_{SSIS}	SDI to CLK S Setup Time	10		10	
t_{HSSI}	CLK S to SDI Hold Time	0		0	
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	2		2	
t_{DMSO}	MODE to SDO	16		16	
t_{DSISO}	SDI to SDO	16		15	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C818–			
		30		24	
Symbol	Parameter	Min	Max	Min	Max
t_{PWS}	CLK S Pulse Width	25		25	
t_{DSSO}	CLK S to SDO		30		30
t_{SSIS}	SDI to CLK S Setup Time	12		12	
t_{HSSI}	CLK S to SDI Hold Time	0		0	
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	5		5	
t_{DMSO}	MODE to SDO	18		18	
t_{DSISO}	SDI to SDO	18		18	

SWITCHING WAVEFORMS — SERIAL SHIFT OPERATION



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SWITCHING CHARACTERISTICS — PIPELINE LOAD FROM SHADOW

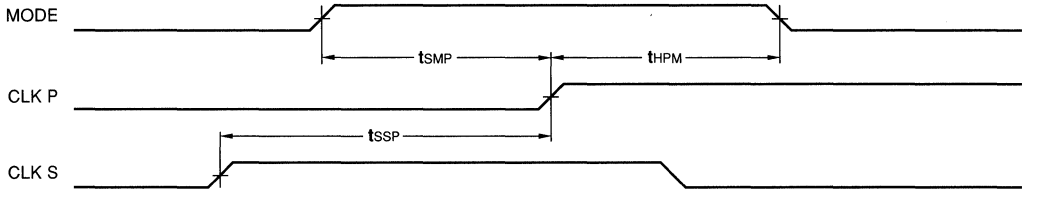
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C818–			
		25		15	
Symbol	Parameter	Min	Max	Min	Max
t_{SMP}	MODE to CLK P	15		15	
t_{HPM}	CLK P to MODE Hold Time	2		2	
t_{SSP}	CLK S to CLK P	10		10	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C818–			
		30		24	
Symbol	Parameter	Min	Max	Min	Max
t_{SMP}	MODE to CLK P	15		15	
t_{HPM}	CLK P to MODE Hold Time	2		2	
t_{SSP}	CLK S to CLK P	15		15	

SWITCHING WAVEFORMS — PIPELINE LOAD FROM SHADOW



SWITCHING CHARACTERISTICS — SHADOW LOAD FROM Y PORT

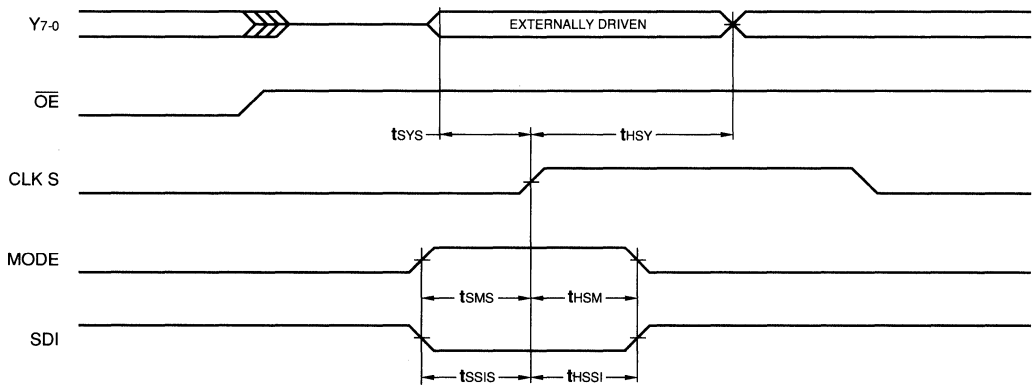
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C818–			
		25		15	
Symbol	Parameter	Min	Max	Min	Max
t_{SYS}	Y_{7-0} to CLK S Setup Time	5		5	
t_{HSY}	CLK S to Y_{7-0} Hold Time	5		5	
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	2		2	
t_{SSIS}	SDI to CLK S Setup Time	10		10	
t_{HSSI}	CLK S to SDI Hold Time	0		0	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C818–			
		30		24	
Symbol	Parameter	Min	Max	Min	Max
t_{SYS}	Y_{7-0} to CLK S Setup Time	5		5	
t_{HSY}	CLK S to Y_{7-0} Hold Time	5		5	
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	5		5	
t_{SSIS}	SDI to CLK S Setup Time	12		12	
t_{HSSI}	CLK S to SDI Hold Time	0		0	

SWITCHING WAVEFORMS — SHADOW LOAD FROM Y PORT



SWITCHING CHARACTERISTICS — SHADOW READ VIA D PORT

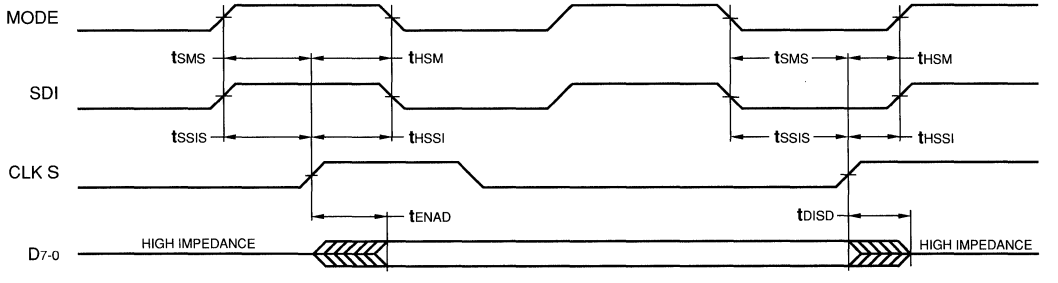
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		L29C818–			
		25		15	
Symbol	Parameter	Min	Max	Min	Max
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	2		2	
t_{SSIS}	SDI to CLK S Setup Time	10		10	
t_{HSSI}	CLK S to SDI Hold Time	0		0	
t_{ENAD}	CLK S to D_{7-0} Enable Delay (Note 11)	85		80	
t_{DISD}	CLK S to D_{7-0} Disable Delay (Note 11)	30		25	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		L29C818–			
		30		24	
Symbol	Parameter	Min	Max	Min	Max
t_{SMS}	MODE to CLK S Setup Time	12		12	
t_{HSM}	CLK S to MODE Hold Time	5		5	
t_{SSIS}	SDI to CLK S Setup Time	12		12	
t_{HSSI}	CLK S to SDI Hold Time	0		0	
t_{ENAD}	CLK S to D_{7-0} Enable Delay (Note 11)	90		90	
t_{DISD}	CLK S to D_{7-0} Disable Delay (Note 11)	35		35	

SWITCHING WAVEFORMS — SHADOW READ VIA D PORT



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

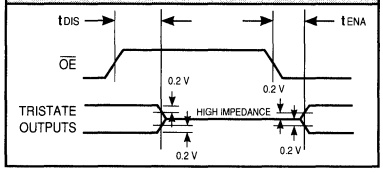
c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

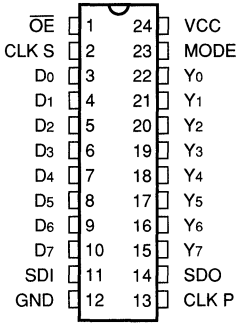
FIGURE 1. THRESHOLD LEVELS

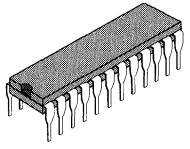


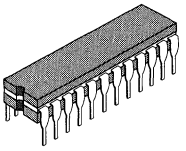
5

ORDERING INFORMATION

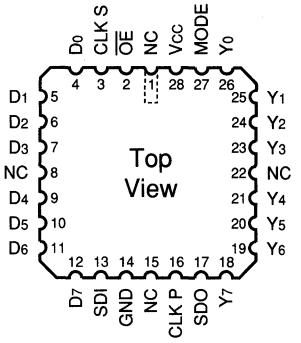
24-pin — 0.3" wide

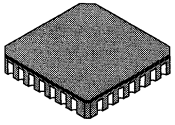






28-pin





Speed	Plastic DIP (P2)	Ceramic DIP (C1)	Ceramic Leadless Chip Carrier (K1)
	0°C to +70°C — Commercial Screening		
25 ns	L29C818PC25	L29C818CC25	L29C818KC25
15 ns	L29C818PC15	L29C818CC15	L29C818KC15
	–55°C to +125°C — Commercial Screening		
30 ns		L29C818CM30	L29C818KM30
24 ns		L29C818CM24	L29C818KM24
	–55°C to +125°C — MIL-STD-883 Compliant		
30 ns		L29C818CMB30	L29C818KMB30
24 ns		L29C818CMB24	L29C818KMB24

Ordering Information 1
Video Imaging Products 2
Arithmetic Logic Units & Special Arithmetic Functions 3
Multipliers & Multiplier-Accumulators 4
Register Products 5
Peripheral Products 6
Quality and Reliability 7
Technology and Design Features 8
Package Information 9
Product Listing 10
Sales Offices 11

Peripheral Products

PERIPHERAL PRODUCTS 6-1
L5380 SCSI Bus Controller 6-3
L53C80 SCSI Bus Controller 6-3

LOGIC DEVICES INCORPORATED

L5380/53C80
SCSI Bus Controller

FEATURES

- Asynchronous Transfer Rate Up to 4 Mbytes/sec
- Low Power CMOS Technology
- Replaces NCR 5380/53C80/53C80-40 and AMD Am5380/53C80
- On-Chip SCSI Bus Drivers
- Supports Arbitration, Selection/Reselection, Initiator or Target Roles
- Programmed or DMA I/O, Handshake or Wait State DMA Interlock
- DESC SMD No. 5962-90548
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
  - 40/48-pin Plastic DIP
  - 40-pin Ceramic DIP
  - 48-pin Sidebraze, Hermetic DIP
  - 44-pin Plastic LCC, J-Lead
  - 44-pin Ceramic LCC

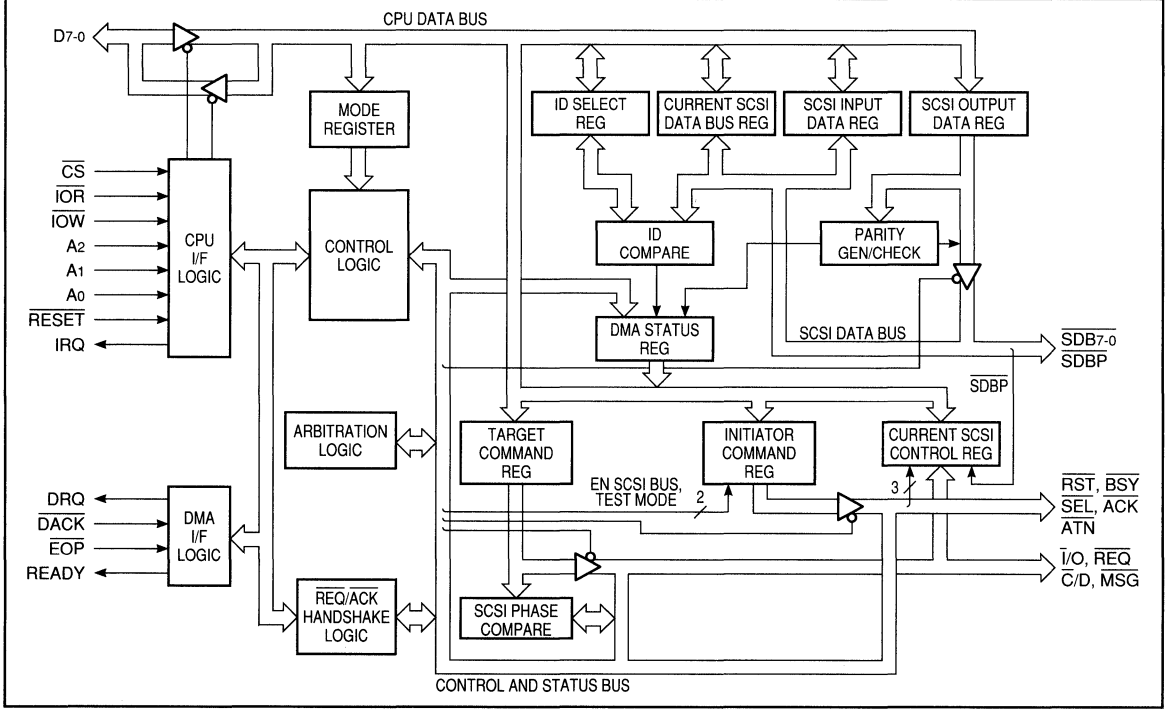
DESCRIPTION

The **L5380/53C80** are high performance SCSI bus controllers which support the physical layer of the SCSI (Small Computer System Interface) bus as defined by the ANSI X3T9.2 committee. It is pin and functionally compatible with the NMOS NCR5380, while offering up to a 2.5x performance improvement, 10x power reduction, and lower cost. Replacement of the NMOS 5380 by the LOGIC Devices L5380/53C80 will result in an immediate transfer rate improvement due to $\overline{REQ}/\overline{ACK}$ and $DRQ/\overline{DACK}$ handshake response times up to 5 times faster than previous devices. While remaining firmware compatible with the NCR5380, the L5380/53C80 provides bug fixes and state machine enhancements allowing even larger throughput gains for new designs.

The L5380/53C80 supports asynchronous data transfer between initiator and target at up to 4 Mbytes/sec. It operates in either initiator or target roles and offers a choice of programmed I/O (direct microprocessor manipulation of handshake) or any of several DMA modes (autonomous handshake and data transfer operations). The L5380/53C80 has internal hardware to support arbitration and can monitor and generate interrupts for a variety of error conditions. It provides extensive bus status monitoring features and includes buffers capable of directly driving a terminated SCSI bus for a compact implementation.

6

L5380/53C80 BLOCK DIAGRAM



PIN DEFINITIONS

A. SCSI Bus

$\overline{SDB7\text{–}0}$ — SCSI DATA BUS 7–0

Bidirectional/Active low. The 8-bit SCSI data bus is defined by these pins. $\overline{SDB7}$ is the most significant bit. During arbitration phase, these lines contain the SCSI ID numbers of all initiators arbitrating for the SCSI bus; $\overline{SDB7}$ represents the initiator with the highest priority. During the selection/reselection phase, these lines contain the ID number of the device that won the arbitration along with the ID number of the device to be selected/reselected.

$\overline{SDBP}$ — SCSI DATA BUS PARITY

Bidirectional/Active low. $\overline{SDBP}$ is the parity bit of the SCSI data bus. Odd parity is used, meaning that the total number of ones on the bus, including the parity bit, is odd. Parity is always generated when sending information, however checking for parity errors when receiving information is a user option. Parity is not valid during arbitration phase.

$\overline{SEL}$ — SELECT

Bidirectional/Active low. $\overline{SEL}$ is asserted by the initiator to select a target. It is also asserted by the target when reselecting it as an initiator.

$\overline{BSY}$ — BUSY

Bidirectional/Active low. $\overline{BSY}$ is asserted to indicate that the SCSI bus is active.

$\overline{ACK}$ — ACKNOWLEDGE

Bidirectional/Active low. $\overline{ACK}$ is asserted by the initiator during any information transfer phase in response to assertion of $\overline{REQ}$ by the target. Similarly, $\overline{ACK}$ is deasserted after $\overline{REQ}$ becomes inactive. These two signals form the data transfer handshake between the initiator and target. Data is latched by the target on the lowgoing edge of $\overline{ACK}$ for target receive operations.

$\overline{ATN}$ — ATTENTION

Bidirectional/Active low. $\overline{ATN}$ is asserted by the initiator after successful selection of a target, to indicate an intention to send a message to the target. The target responds to $\overline{ATN}$ by entering the MESSAGE OUT phase.

$\overline{RST}$ — SCSI BUS RESET

Bidirectional/Active low. $\overline{RST}$ when active indicates a SCSI bus reset condition.

$\overline{I}/O$ — INPUT/OUTPUT

Bidirectional/Active low. $\overline{I}/O$ is controlled by the target and specifies the direction of information transfer. When $\overline{I}/O$ is asserted, the direction of transfer is to the initiator. $\overline{I}/O$ is also asserted by the target during RESELECTION phase to distinguish it from SELECTION phase.

$\overline{C}/D$ — CONTROL/DATA

Bidirectional/Active low. $\overline{C}/D$ is controlled by the target and when asserted, indicates CONTROL (command or status) information is on the SCSI data bus. DATA is specified when $\overline{C}/D$ is deasserted.

$\overline{MSG}$ — MESSAGE

Bidirectional/Active low. $\overline{MSG}$ is controlled by the target, and when asserted indicates MESSAGE phase.

$\overline{REQ}$ — REQUEST

Bidirectional/Active low. $\overline{REQ}$ is asserted by the target to begin the handshake associated with transfer of a byte over the SCSI data bus. $\overline{REQ}$ is deasserted upon receipt of $\overline{ACK}$ from the initiator. Data is latched by the initiator on the lowgoing edge of $\overline{REQ}$ for initiator receive operations.

B. Microprocessor Bus

$\overline{CS}$ — CHIP SELECT

Input/Active low. This signal enables reading or writing of the internal registers by the microprocessor, using memory mapped I/O. An alternate method for reading selected registers is available for DMA.

DRQ — DMA REQUEST

Output/Active high. This signal is used to indicate that the L5380/53C80 is ready to execute the next cycle of a DMA transfer on the microprocessor bus. For send operations, it indicates that the output data register is ready to receive the next byte from the DMA controller or CPU. For receive operations, it indicates that the input data register contains the next byte to be read by the DMA controller or CPU.

IRQ — INTERRUPT REQUEST

Output/Active high. The L5380/53C80 asserts this signal to indicate to the microprocessor that one of the several interrupt conditions have been met. These include SCSI bus fault conditions as well as other events requiring microprocessor intervention. Most interrupt types are individually maskable.

$\overline{IOR}$ — I/O READ

Input/Active low. $\overline{IOR}$ is used in conjunction with $\overline{CS}$ and A2–0 to execute a memory mapped read of a L5380/53C80 internal register. It is also used in conjunction with $\overline{DACK}$ to execute a DMA read of the SCSI Input Data Register.

READY — READY

Output/Active high. Ready is used rather than DRQ as an alternate method for controlling DMA data transfer. This DMA type is termed blockmode DMA and must be specifically enabled by the CPU. In block-

mode DMA, data is throttled by treating the L5380/53C80 as wait state memory. I/O (DMA) cycles are initiated at the maximum rate sustainable by the DMA controller/memory subsystem, but all cycles are extended (wait-states inserted) until READY is asserted by the L5380/53C80. This is generally the fastest DMA method since memory subsystem addressing can be overlapped with SCSI operations (flyby mode).

$\overline{DACK}$ — DMA ACKNOWLEDGE

Input/Active low. $\overline{DACK}$ is used in conjunction with $\overline{IOR}$ or $\overline{IOW}$ to enable reading or writing of the SCSI Input and Output Data Registers when in DMA mode. $\overline{DACK}$ resets DRQ and must not occur simultaneously with $\overline{CS}$.

$\overline{EOP}$ — END OF PROCESS

Input/Active low. This input is used to indicate to the L5380/53C80 that a DMA transfer is to be concluded. The L5380/53C80 can automatically generate an interrupt in response to receiving $\overline{EOP}$ from the DMA controller.

$\overline{RESET}$ — CPU BUS RESET

Input/Active low. This input clears all internal registers and state machines. It does not result in assertion of the $\overline{RST}$ signal on the SCSI bus and therefore affects only the local L5380/53C80 and not other devices on the bus.

$\overline{IOW}$ — I/O WRITE

Input/Active low. $\overline{IOW}$ is used in conjunction with $\overline{CS}$ and A_{2-0} to execute a memory mapped write of a L5380/53C80 internal register. It is also used in conjunction with $\overline{DACK}$ to execute a DMA write of the SCSI Output Data Register.

A_{2-0} — ADDRESS 2-0

Inputs/Active high. These signals, in conjunction with $\overline{CS}$, $\overline{IOR}$, and $\overline{IOW}$, address the L5380/53C80 internal registers for CPU read/write operations.

D_{7-0} — DATA 7-0

Bidirectional/Active high. These signals are the microprocessor data bus. D_7 is the most significant bit.

L5380/53C80 INTERNAL REGISTERS

Overview

The L5380/53C80 contains registers that are directly addressed by the microprocessor. These registers allow for monitoring of SCSI bus activity, controlling the operation of the L5380/53C80, and determining the cause of interrupts. In many cases, a read-only and a write-only register are mapped to the same address. Some addresses are dummy registers which are used to implement a control operation but do not correspond to a physical register. The state of the CPU data bus when writing or reading these dummy registers is 'don't care'. Tables 1 and 3 show the address and name of each register as well as bit definitions.

Register Descriptions

A. Write Operations

The following paragraphs give detailed descriptions of the function of each bit in the L5380/53C80 internal registers for write operations as shown in Table 1.

WRITE ADDRESS 0
Output Data Register

The Output Data Register is a write-only register used for sending information to the SCSI data bus. During arbitration, the arbitrating SCSI device asserts its ID via this register. The device which wins arbitration also asserts the "OR" of its ID and the ID of the target/initiator to be selected/reselected. In programmed I/O mode this register is written using $\overline{CS}$ and $\overline{IOW}$ with A_{2-0} = 000. In DMA mode, it is written when $\overline{IOW}$ and $\overline{DACK}$ are simultaneously active, irrespective of the state of the address lines. Note that a "1" written to the Output Data Register becomes a low state when asserted on the active-low SCSI bus.

WRITE ADDRESS 1
Initiator Command Register

The Initiator Command Register is a read/write register which allows CPU control of the SCSI signals asserted by the initiator. Some bits in this register are not readable, and these positions are mapped to status bits useful in monitoring the progress of arbitration. These, along with the initiation of system-wide reset and test functions, may also be of use to the target.

R1 Bit 7 — Assert $\overline{RST}$

When this bit is set, the L5380/53C80 asserts the $\overline{RST}$ line on the SCSI bus, initializing all devices on the bus to the reset condition. All logic and internal registers of the L5380/53C80 are reset, except for the Assert RST bit itself, the Testmode bit (R1 bit 6) and the IRQ (interrupt request) latch. The IRQ pin becomes active indicating a SCSI bus reset interrupt. This interrupt is not maskable.

R1 Bit 6 — Testmode

When this bit is set, the L5380/53C80 places all outputs, including both SCSI and CPU signals, in a high impedance state. This effectively removes the device from the system as an aid to system diagnostics. Note that internal registers may still be written to while in Testmode. The L5380/53C80 returns to normal operation when Testmode is reset. The Testmode bit is reset by either writing a "0" to R1 bit 6

or via the RESET (CPU reset) pin. Testmode is not affected by the RST (SCSI bus reset) signal, or by the Assert RST bit in the Initiator Command Register (R1 bit 7).

R1 Bit 5 — Not Used

R1 Bit 4 — Assert ACK

When this bit is set, ACK is asserted on the SCSI bus. Resetting this bit deasserts ACK. Note that ACK will be asserted only if the Targetmode bit (R2 bit 6) is reset, indicating that the L5380/53C80 is acting as an initiator.

R1 Bit 3 — Assert BSY

When this bit is set, BSY is asserted on the SCSI bus. Resetting this bit deasserts BSY. BSY is asserted to indicate that the device has been selected or reselected, and deasserting BSY causes a bus free condition.

R1 Bit 2 — Assert SEL

When this bit is set, SEL is asserted on the SCSI bus. Resetting this bit deasserts SEL. SEL is normally asserted after a successful arbitration.

R1 Bit 1 — Assert ATN

When this bit is set, ATN is asserted on the SCSI bus. Resetting this bit deasserts ATN. ATN is asserted by the initiator to request message out phase. Note that ATN will be asserted only if the Targetmode bit (R2 bit 6) is reset, indicating that the L5380/53C80 is acting as an initiator.

R1 Bit 0 — Assert Data Bus

When this bit is set, the open drain SCSI data bus and parity drivers are enabled and the contents of the Output Data Register are driven onto the SCSI data lines. In addition to the Assert Data Bus bit, enabling of the SCSI bus drivers requires one of the following two sets of conditions:

When the L5380/53C80 is operating as an initiator, the Targetmode bit (R2 bit 6) must be reset, the I/O pin must be negated (initiator to target transfer) and no phase mismatch condition can exist. A phase mismatch occurs when the MSG, C/D, and I/O bits of the Target Command Register (R3) do not match the corresponding SCSI control lines.

When the L5380/L53C80 is operating as a target, the Targetmode bit will be set, and in this case Assert Data Bus will enable the outputs unconditionally.

The Assert Data Bus bit need not be set for arbitration to occur; when the Arbitrate bit (R2 bit 0) is set, and a bus free condition is detected, the data bus will be enabled for arbitration regardless of the state of the Assert Data Bus bit.

Finally, note that the Testmode bit (R1 bit 6) overrides all other controls, including Assert Data Bus and Arbitrate, and disables all outputs.

WRITE ADDRESS 2
Mode Register

The Mode register is a read/write register which provides control over several aspects of L5380/53C80 operation. Programmed I/O or two different types of DMA transfer may be selected, initiator or target device operation is accommodated, and parity checking and interrupts may be enabled via this register. The function of each individual bit is described as follows:

R2 Bit 7 — Blockmode

This bit must be used in conjunction with DMA Mode (R2 bit 1). It is used to select the type of handshake desired between the L5380/53C80 and the external DMA controller. See "L5380/53C80 Data Transfers" for a complete discussion of the transfer types supported.

R2 Bit 6 — Targetmode

When this bit is set, the L5380/53C80 will operate as a SCSI target device. This enables the SCSI signals I/O, C/D, MSG, and REQ to be asserted.

When Targetmode is reset, the device will operate as an initiator. This enables the SCSI signals ATN and ACK to be asserted. Targetmode also affects state machine operation for DMA transfers and the conditions necessary for enabling the SCSI Data bus drivers. (See Assert Databus, R1 bit 0).

R2 Bit 5 — Enable Parity Check

When this bit is set, information received on the SCSI data bus is checked for odd parity. The Parity Error latch will be set whenever data is received under DMA control or the Current SCSI Data Register (Read Register 0) is read by the CPU. The state of the Parity Error latch can be determined by reading R5 bit 5, and it can be reset by a read to Address 7. Note that ENABLE PARITY CHECK must be set if parity error interrupts are to be generated. This interrupt can be separately masked by the Enable Parity Interrupt bit (R2 bit 4) while retaining the state of the Parity Error latch for later examination by the CPU.

R2 Bit 4 — Enable Parity Interrupt

When this bit is set, the L5380/53C80 will set the interrupt request latch, and assert IRQ (interrupt request) if it detects a parity error. Enable Parity Check (R2 bit 5) must also be set if parity error interrupts are desired.

R2 Bit 3 — Enable End Of DMA Interrupt

When this bit is set, the L5380/53C80 will set the interrupt request latch, and assert IRQ (interrupt request) if it detects a valid EOP (End of Process) signal. EOP is normally generated by a DMA controller to indicate the end of a DMA transfer. EOP is valid only when coincident with IOR or IOW and DACK.

R2 Bit 2 — Monitor Busy

When this bit is set, the L5380/53C80 continuously monitors the state of the $\overline{BSY}$ signal. Absence of $\overline{BSY}$ for a period longer than 400 ns (but less than 1200 ns) will cause the L5380/53C80 to set the BSYERR and IRQ (interrupt request) latches. In addition, the six least significant bits of the Initiator Command Register are reset, and all SCSI data and control outputs are disabled until the BSYERR latch is reset. This effectively disconnects the L5380/53C80 from the SCSI bus in response to an unexpected disconnect by another device. It also allows the CPU to be interrupted when the SCSI bus becomes free in systems where arbitration is not used and an $\overline{EOP}$ signal is not available.

R2 Bit 1 — DMA Mode

When this bit is set, the L5380/53C80's internal state machines automatically control the SCSI signals $\overline{REQ}$ and $\overline{ACK}$ (as appropriate for initiator or target operation) and the CPU signals DRQ and READY. DMA Mode must be set prior to starting a DMA transfer in either direction. The DMA Mode bit is reset whenever a bus free condition is detected ($\overline{BSY}$ is not active). This aborts DMA operations when a loss of $\overline{BSY}$ occurs, regardless of the state of the Monitor Busy bit (R2 bit 2.) The DMA Mode bit is not reset when $\overline{EOP}$ is received, but must be specifically reset by the CPU. $\overline{EOP}$ does, however, inhibit additional DMA cycles from occurring.

R2 Bit 0 — Arbitrate

This bit is set to indicate a desire to arbitrate for use of the SCSI bus. Before setting the Arbitrate bit, the SCSI Output Data Register (Write Register 0) must be written with the SCSI ID assigned to the arbitrating SCSI device. The bit position of register R0 which is set represents the priority number of the SCSI device, with bit 7 the highest priority. See the section on "Arbitration" for a full discussion of the L5380/53C80 arbitration procedure.

TABLE 1. WRITE REGISTERS

Address 0 — Output Data Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 1 — Initiator Command Register

7	6	5	4	3	2	1	0
ASSERT $\overline{RST}$	TEST MODE		ASSERT $\overline{ACK}$	ASSERT $\overline{BSY}$	ASSERT $\overline{SEL}$	ASSERT $\overline{ATN}$	ASSERT DATA BUS

Address 2 — Mode Register

7	6	5	4	3	2	1	0
BLOCK MODE	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT'RPT	ENABLE EODMA INT'RPT	MONI-TOR BUSY	DMA MODE	ARBI-TRATE

Address 3 — Target Command Register

7	6	5	4	3	2	1	0
LAST BYTE SENT				ASSERT $\overline{REQ}$	ASSERT $\overline{MSG}$	ASSERT $\overline{C}$/D	ASSERT $\overline{I}$/O

Address 4 — ID Select Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 5 — Start DMA Send

7	6	5	4	3	2	1	0

Address 6 — Start DMA Target Receive

7	6	5	4	3	2	1	0

Address 7 — Start DMA Initiator Receive

7	6	5	4	3	2	1	0

6

WRITE ADDRESS 3
Target Command Register

The Target Command Register is a read/write register which allows CPU control of the SCSI signals asserted by the target. In addition, this register contains a read-only status flag useful in unambiguously determining when the last byte of a DMA transfer has actually been sent over the SCSI bus.

When operating as an initiator with DMA mode set, the Assert $\overline{MSG}$, Assert $\overline{C}/D$, and Assert $\overline{I}/O$ bits are used as a template to compare against the corresponding SCSI control signals provided by the target. A phase mismatch interrupt will be generated on the falling edge of the $\overline{REQ}$ input if the template does not match the state of the signals. Therefore the CPU should initialize these bits to the phase of the expected data transfer. An interrupt, then, will signal an intent by the target to change to a new phase. The SCSI information transfer phases and their associated direction of data transfer are given in Table 2.

R3 Bits 7-4 — Not Used

R3 Bit 3 — Assert $\overline{REQ}$

When this bit is set, $\overline{REQ}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{REQ}$. Note that $\overline{REQ}$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target.

R3 Bit 2 — Assert $\overline{MSG}$

When this bit is set, $\overline{MSG}$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{MSG}$. Note that $\overline{MSG}$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{MSG}$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

R3 Bit 1 — Assert $\overline{C}/D$

When this bit is set, $\overline{C}/D$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{C}/D$. Note that $\overline{C}/D$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{C}/D$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

R3 Bit 0 — Assert $\overline{I}/O$

When this bit is set, $\overline{I}/O$ is asserted on the SCSI bus. Resetting this bit deasserts $\overline{I}/O$. Note that $\overline{I}/O$ will be asserted only if the Targetmode bit (R2 bit 6) is set, indicating that the L5380/53C80 is acting as a target. When operating as an initiator, this bit is compared against the $\overline{I}/O$ input, and an interrupt is generated if they differ at the falling edge of $\overline{REQ}$.

WRITE ADDRESS 4
ID Select Register

The ID Select Register is a write-only register which is used to monitor selection or reselection attempts to the L5380/53C80. In arbitrating systems, an ID number is assigned to each SCSI device by setting a single bit position of the ID Select Register. Each SCSI data pin is inverted and compared with the corresponding bit in the ID Select Register. If any matches are found while a bus free condition exists and $\overline{SEL}$ is active, the L5380/53C80 will generate an interrupt to indicate a selection or reselection. During selection or reselection, parity checking may be enabled by setting the Enable Parity Check bit (R2 bit 5). This interrupt may be masked by resetting all bits in this register.

WRITE ADDRESS 5
Start DMA Send

This is a dummy register. Writes to this location are detected and cause the L5380/53C80 internal state machine to execute a DMA send operation. This location is used for either initiator or target DMA send. The DMAMODE bit (R2 bit 1) must be set prior to writing this location.

WRITE ADDRESS 6
Start DMA Target Receive

This is a dummy register. Writes to this location are detected and cause the L5380/53C80 internal state machine to execute a target DMA receive operation. The DMAMODE bit (R2 bit 1) and the Targetmode bit (R2 bit 6) must be set prior to writing this location.

WRITE ADDRESS 7
Start DMA Initiator Receive

This is a dummy register. Writes to this location are detected and cause the L5380/53C80 internal state machine to execute an initiator DMA

TABLE 2. SCSI INFORMATION TRANSFER PHASES

$\overline{MSG}$	$\overline{C}/D$	$\overline{I}/O$	Phase	Direction		
0	0	0	Message In	Target	→	Initiator
0	0	1	Message Out	Initiator	→	Target
0	1	0	Unused			
0	1	1	Unused			
1	0	0	Status In	Target	→	Initiator
1	0	1	Command	Initiator	→	Target
1	1	0	Data In	Target	→	Initiator
1	1	1	Data Out	Initiator	→	Target

receive operation. The DMAMODE bit (R2 bit 1) must be set and the Targetmode bit (R2 bit 6) must be reset prior to writing this location.

B. READ OPERATIONS

The following paragraphs give detailed descriptions of the function of each bit in the L5380/53C80 internal registers for read operations as shown in Table 3.

READ ADDRESS 0
Current SCSI Data Bus

The Current SCSI Data Bus Register allows the microprocessor to monitor the SCSI data bus at any time, by asserting $\overline{CS}$ and $\overline{IOR}$ with address lines $A_{2-0} = 000$. The SCSI data lines are not actually registered, but gated directly onto the CPU bus whenever Address 000 is read by the CPU. Therefore, reads of this location should only be done when the SCSI data lines are guaranteed to be stable by the SCSI protocol. For systems which implement SCSI bus arbitration, this location is read to determine whether devices having higher priorities are also arbitrating. Programmed I/O data transfer uses this location for reading data transferred on the SCSI data bus. With parity checking enabled, SCSI data bus parity checking is done at the beginning of the read cycle for fast error detection. Note that the SCSI data bus is inverted to become active high when presented to the CPU.

READ ADDRESS 1
Initiator Command Register

Reading bit 7 or bits 4–0 of the Initiator Command Register simply reflects the status of the corresponding bit in the register. Bits 6 and 5 are mapped to other signals as discussed below:

R1 Bit 6 — Arbitration In Progress

For this bit to be active, the Arbitrate bit (R2 bit 0) must be set. When ARBITRATION IN PROGRESS is set, it indicates that the L5380/53C80 has detected a bus free condition and is currently arbitrating for control of the bus. See the section on "Arbitration" for a complete discussion of the L5380/53C80 arbitration mechanism. Resetting the Arbitrate bit will reset ARBITRATION IN PROGRESS.

R1 Bit 5 — Lost Arbitration

For this bit to be active, the Arbitrate bit (R2 bit 0) must be set. When LOST ARBITRATION is set, it indicates that the L5380/53C80 has arbitrated for the SCSI bus (see R1 bit 6 above) and has detected the assertion of $\overline{SEL}$ by another (higher priority) device. The L5380/53C80 responds to loss of arbitration by immediately discontinuing the arbitration attempt. Resetting the Arbitrate bit will reset LOST ARBITRATION.

READ ADDRESS 2
Mode Register

Reading the Mode Register simply reflects the status of the bits in that register.

READ ADDRESS 3
Target Command Register

Reading the Target Command Register simply reflects the status of the bits in that register, except for bit 7, LAST BYTE SENT.

R3 bit 7 — Last Byte Sent

This read only bit indicates that the last byte of data loaded into the L5380/53C80 during a DMA send operation has actually been transferred over the SCSI bus. Note that the end of process flag and the corresponding interrupt occur when this byte is loaded into the L5380/53C80, but do not reflect whether it has actually been sent. This bit is not present in the NCR5380, but is present in the NCR53C80. Last Byte Sent is reset when the DMAMODE bit (R2 bit 1) is reset.

READ ADDRESS 4
Current SCSI Control Register

The Current SCSI Control Register provides a means for the CPU to directly monitor the state of the SCSI bus control signals. The SCSI control lines are not actually registered, but gated directly onto the CPU bus whenever Address 100 is read by the CPU. The value of each bit position represents the complement of the corresponding (low true) SCSI Signal Pin.

READ ADDRESS 5
DMA Status Register

The DMA Status Register provides a means for the CPU to determine the status of a DMA transfer and to determine the cause of an interrupt. It also makes available the final two SCSI bus signals which are not included in the Current SCSI Control Register. The function of each individual bit is defined as follows:

R5 Bit 7 — End of DMA

When this bit is set, it indicates that a valid $\overline{EOP}$ has been received during a DMA transfer. A valid $\overline{EOP}$ occurs when $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are simultaneously active for the minimum specified time. End of DMA is reset when the DMAMODE bit (R2 bit 1) is reset.

Note that for DMA send operations, an END OF DMA status indicates only that the last byte of the transfer is loaded into the Output Data Register of the sending device, not that it has actually been transferred over the SCSI bus. For this reason, the L5380/53C80 provides an additional status bit; Last Byte Sent (R3 bit 7) which indicates that this final byte has been transferred to the receiving end. This bit is not present in the NCR5380.

Also, note that the DMAMODE bit is reset automatically whenever a loss of busy condition is detected, which in turn resets END OF DMA. Therefore

the DMA Status Register should be read prior to resetting the Assert $\overline{BSY}$ bit (R1 bit 3) at the conclusion of a DMA transfer.

R5 Bit 6 — DMA Request

This bit reflects the state of the DRQ (DMA Request) signal. In programmed I/O, this bit can be polled by the CPU to determine whether there is a pending request for byte transfer. For DMA send operations, DMA REQUEST is reset when $\overline{DACK}$ and $\overline{IOW}$ are simultaneously asserted. For DMA receive operations, simultaneous $\overline{DACK}$ and $\overline{IOR}$ will reset DMA REQUEST. DMA REQUEST is reset unconditionally when the DMAMODE bit (R2 bit 1) is reset.

R5 Bit 5 — Parity Error

This bit can only be set if Enable Parity Check (R2 bit 5) is set. When enabled, the Parity Error bit is set if incoming SCSI data in either initiator or target mode, or during selection phase, does not correctly reflect odd parity. PARITY ERROR can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bit 4 — Interrupt Request

This bit reflects the state of the IRQ signal. The L5380/53C80 asserts IRQ to generate an interrupt to the CPU. See the section on "Interrupts" for further information on the possible sources of interrupts in the L5380/53C80. INTERRUPT REQUEST can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bit 3 — Phase Match

When this bit is set, it indicates that the $\overline{MSG}$, $\overline{C}/D$, and $\overline{I}/O$ lines match the state of the Assert $\overline{MSG}$, Assert $\overline{C}/D$, and Assert $\overline{I}/O$ bits in the Target Command Register. PHASEMATCH is not actually registered, but represents a continuous comparison of these three phase bits to the corresponding internal register locations. This bit is intended for use by the

TABLE 3. READ REGISTERS

Address 0 — Current SCSI Data Bus

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 1 — Initiator Command Register

7	6	5	4	3	2	1	0
ASSERT $\overline{RST}$	ARB. IN PRO-GRESS	LOST ARB.	ASSERT $\overline{ACK}$	ASSERT $\overline{BSY}$	ASSERT $\overline{SEL}$	ASSERT $\overline{ATN}$	ASSERT DATA BUS

Address 2 — Mode Register

7	6	5	4	3	2	1	0
BLOCK MODE	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT'RPT	ENABLE EODMA INT'RPT	MONI-TOR BUSY	DMA MODE	ARBI-TRATE

Address 3 — Target Command Register

7	6	5	4	3	2	1	0
LAST BYTE SENT				ASSERT $\overline{REQ}$	ASSERT $\overline{MSG}$	ASSERT $\overline{C}/D$	ASSERT $\overline{I}/O$

Address 4 — Current SCSI Control Register

7	6	5	4	3	2	1	0
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C}/D$	$\overline{I}/O$	$\overline{SEL}$	$\overline{PARITY}$

Address 5 — DMA Status Register

7	6	5	4	3	2	1	0
END OF DMA	DMA REQ.	PARITY ERROR	INTER-RUPT REQ.	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$

Address 6 — Input Data Register

7	6	5	4	3	2	1	0
$\overline{SDB7}$	$\overline{SDB6}$	$\overline{SDB5}$	$\overline{SDB4}$	$\overline{SDB3}$	$\overline{SDB2}$	$\overline{SDB1}$	$\overline{SDB0}$

Address 7 — Reset Error/Interrupt Register

7	6	5	4	3	2	1	0

initiator to detect that the target device has changed to a different information transfer phase. When the L5380/53C80 detects a phase mismatch, PHASEMATCH is reset, and information transfer to or from the SCSI bus is inhibited.

R5 Bit 2 — Busy Error

This bit can only be set if the Monitor Busy bit (R2 bit 2) is set. When set, Busy Error indicates that the BSY pin has been false for a period at least equal to a bus settle delay (400 ns). When the Busy Error condition is detected, all SCSI signal pins are disabled, and the DMAMODE bit (R2 bit 1) and bits 5-0 of the Initiator Command Register are reset. Busy Error can be reset by a read to the Reset Error/Interrupt Register (Register 7).

R5 Bits 1, 0 — $\overline{ATN}$, $\overline{ACK}$

Like the Current SCSI Control Register, these bits provide a means for the CPU to directly monitor the state of the SCSI bus control signals. The SCSI control lines are not actually registered, but gated directly onto the CPU bus whenever Address 5 is read by the CPU. The value of each bit position represents the complement of the corresponding (low true) SCSI Signal Pin.

READ ADDRESS 6
Input Data Register

This register acts as a temporary holding register for information received from the SCSI data bus during DMA transfers (DMAMODE bit, R2 bit 1 is set). In the initiator mode, the L5380/53C80 latches the SCSI data when $\overline{REQ}$ goes active. In the target mode, data is latched when $\overline{ACK}$ goes active. The contents of this register represent the negation of the low-true SCSI data. The contents of the SCSI Input Data Register are gated onto the CPU data bus when $\overline{DACK}$ and $\overline{IOR}$ are simultaneously true, or by a CPU read of location 6. Note that $\overline{DACK}$ and $\overline{CS}$ must never be active simultaneously in order to prevent conflicting read operations. Parity may optionally be checked on the data as it is loaded into this register.

READ ADDRESS 7
Reset Error/Interrupt Register

This is a dummy register. Reads to this location are detected and used to reset the Interrupt Request Latch (IRQ signal) and the PARITY ERROR, INTERRUPT REQUEST, and BUSY ERROR latches (visible as bits 5, 4, and 2 of Register 5).

INTERRUPTS

The L5380/53C80 generates interrupts to the CPU by setting the Interrupt Request Latch, which directly drives the IRQ (Interrupt Request) line. The IRQ output will reflect the state of the Interrupt Request Latch under all conditions except when Testmode (R1 bit 6) is active, when it is in a high impedance state. The Interrupt Request Latch may be reset by reading Address 7, the Reset Error/Interrupt Register. A read of this location also resets several error condition latches as discussed in the section on "Internal Registers".

Interrupts may be caused by any of six conditions, most of which may be masked by resetting enable bits in the appropriate registers. The following sections describe each interrupt type, its cause, and how it may be reset. Upon receiving an interrupt, the CPU may read the Current SCSI Control Register (R4) and the DMA Status Register (R5) to determine the cause of the interrupt. While the following discussions indicate the expected values of these registers following an interrupt, it is recommended that bits in these registers which are not germane to determining the cause of an interrupt be masked off in firmware prior to implementing a comparison. A typical operational sequence for an interrupt service routine is given at the end of this section.

SCSI Bus Reset Interrupt

A SCSI Bus Reset Interrupt occurs when the SCSI $\overline{RST}$ signal becomes active. This may be due to another SCSI device driving the $\overline{RST}$ line, or because the Assert $\overline{RST}$ bit (R1 bit 7) has been set, causing the L5380/53C80 to drive the SCSI $\overline{RST}$ line. The value of the SCSI $\overline{RST}$ line is visible as R4 bit 7; however, this line is not latched and therefore may have changed state by the time the CPU responds to the interrupt and polls this location. For this reason, a SCSI Bus Reset Interrupt should be assumed if no other interrupt condition is active when reading Registers 4 and 5.

The SCSI Bus Reset Interrupt is nonmaskable. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Selection/Reselection Interrupt

A Selection/Reselection Interrupt occurs when the SCSI $\overline{SEL}$ signal becomes active, the SCSI bus matches the bit set in the ID Select Register, and $\overline{BSY}$ has been false for at least a bus settle delay. When the $\overline{I}/O$ pin is asserted, the interrupt should be interpreted as a reselection. The Selection/Reselection Interrupt may be masked by resetting all bits in the ID Select Register. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Loss of Busy Interrupt

A Loss of Busy Interrupt occurs when the SCSI $\overline{BSY}$ signal has been inactive for at least a bus settle delay (400 ns). The Loss of Busy Interrupt may be masked by resetting the Monitor Busy bit (R2 bit 2). Resetting Monitor Busy also prevents the Busy Error latch (Read R5 bit 2) from being set. The expected read values for the Current

SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Phase Mismatch Interrupt

A Phase Mismatch Interrupt occurs when the DMAMODE bit (R2 bit 1) is set, $\overline{REQ}$ is active on the SCSI bus, and the SCSI phase signals $\overline{MSG}$, $\overline{C}/D$, and $\overline{I}/O$ do not match the corresponding bits in the Target Command Register. This interrupt is intended for use by the initiator to detect a change of phase by the target during a DMA transfer. When operating as a target, the SCSI phase lines will normally be asserted via the Target Command Register, so no phase mismatch will be generated unless another SCSI device is erroneously driving the phase lines to an unintended state.

The result of the continuous comparison of the SCSI phase lines to the Target Command Register contents is visible as the Phase Match bit (Read R5 bit 3). This flag operates irrespective of the state of DMAMODE and $\overline{REQ}$. As long as a phase mismatch condition persists, the L5380/53C80 is prevented from recognizing active $\overline{REQ}$ inputs, and SCSI output data drivers are disabled.

The Phase Mismatch Interrupt is nonmaskable, however it will only occur when operating in DMAMODE. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

Parity Error Interrupt

A Parity Error Interrupt occurs when incorrect parity is detected during a read of the SCSI bus. Parity checking occurs under the following conditions: Parity is checked during a programmed I/O read of the Current SCSI Data Register (Read R0), when $\overline{CS}$ and $\overline{IOR}$ are active and the $A_{2\text{-}0}$ lines are 000. Parity is also checked during DMA read operations (DMAMODE bit, R2 bit 1 is set) when $\overline{ACK}$ is active for target receive, or $\overline{REQ}$ is active for initiator receive.

The Parity Error latch is set when parity error checking is enabled and one of the above parity error conditions is encountered. This latch is

TABLE 4. INTERRUPT READ VALUES

Read Address 4 — Current SCSI Control Register

7	6	5	4	3	2	1	0
$\overline{RST}$	$\overline{BSY}$	$\overline{REQ}$	$\overline{MSG}$	$\overline{C}/D$	$\overline{I}/O$	$\overline{SEL}$	$\overline{PARITY}$
SCSI Bus Reset Interrupt							
X	0	0	0	0	0	0	0
Selection/Reselection Interrupt							
0	0	0	X	X	1=RESEL	1	X
Loss of Busy Interrupt							
0	0	0	0	0	0	0	0
Phase Mismatch Interrupt							
0	1	1	X	X	X	0	X
Parity Error Interrupt							
0	X	X	X	X	X	X	X
End of DMA Interrupt							
0	1	X	X	X	X	0	X

Read Address 5 — DMA Status Register

7	6	5	4	3	2	1	0
END OF DMA	DMA REQ	PARITY ERROR	INTER-RUPT REQ	PHASE MATCH	BUSY ERROR	$\overline{ATN}$	$\overline{ACK}$
SCSI Bus Reset Interrupt							
0	0	0	1	1	0	0	0
Selection/Reselection Interrupt							
0	0	0	1	X	0	X	0
Loss of Busy Interrupt							
0	0	0	1	X	1	0	0
Phase Mismatch Interrupt							
0	0	0	1	0	X	X	0
Parity Error Interrupt							
X	X	1	1	X	X	X	X
End of DMA Interrupt							
1	0	0	1	X	0	0	X

visible as bit 5 of the DMA Status Register (Read R5). The Parity Error Interrupt may be masked and setting of the Parity Error latch prevented by resetting the Enable Parity Check bit (Write R2 bit 5). The Parity Error latch can be reset by reading the Reset Error/Interrupt Register (Read R7). The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

End of DMA Interrupt

An End of DMA Interrupt occurs when a valid $\overline{EOP}$ (End of Process) signal is detected during a DMA transfer. $\overline{EOP}$ is valid when $\overline{EOP}$, $\overline{DACK}$, and either $\overline{IOR}$ or $\overline{IOW}$ are simultaneously asserted for the minimum specified time. $\overline{EOP}$ inputs not occurring during I/O read or write operations are ignored.

The End of DMA latch is set whenever the DMAMODE bit (R2 bit 1) is set and a valid $\overline{EOP}$ is received. This latch is visible as bit 7 of the DMA Status Register (Read R5). The End of DMA Interrupt may be masked by resetting the Enable EODMA Interrupt bit (Write R2 bit 3). This bit does not affect the End of DMA latch, however. The End of DMA latch can be reset by resetting the DMAMODE bit in the Mode Register. The expected read values for the Current SCSI Control Register and the DMA Status Register upon encountering this interrupt are given in Table 4.

DATA TRANSFERS

The L5380/53C80 supports programmed I/O under CPU control or DMA transfer via a DMA controller when transferring information to and from the SCSI data bus. Programmed I/O can be implemented entirely in firmware or using minimum external logic for accessing the appropriate registers. Under DMA control, the L5380/53C80's DMA interface logic and internal state machines provide the necessary control of the $\overline{REQ}$-$\overline{ACK}$ handshake. Each type of transfer is fully described in the following sections.

Programmed I/O

Two forms of programmed I/O are supported by the L5380/53C80. For normal programmed I/O, the SCSI handshake is accomplished by setting bits in the Initiator or Target Command registers to assert SCSI control lines, and polling the Current SCSI Control and DMA Control registers for the appropriate responses. Since for this method the control is contained in firmware, the cycle times are relatively slow. It is most appropriate for transferring small blocks of data such as SCSI command blocks or messages, where the overhead of setting up a DMA controller could be significant.

Pseudo DMA

An alternate method of programmed I/O allows the state machines of the L5380/53C80 to handle the SCSI handshake, thereby improving performance in systems which do not employ a hardware DMA controller. To implement Pseudo DMA, the DMAMODE bit is set. The CPU polls the DRQ bit in the DMA Control Register to determine when a byte should be written to or read from the

TABLE 5. TYPICAL INTERRUPT SERVICE ROUTINE POLLING SERVICE

Read Address 5 > TEMP	: Read DMA Status Reg to variable TEMP
IF TEMP "AND" HEX (10) = 0 THEN GO TO NEXT DEVICE	: IRQ not active, so L5380/L53C80 was not the source of this interrupt
TEMP "AND" HEX (AC) → TEMP	: Mask off irrevelant bits
IF TEMP > HEX (7F) THEN GO TO EODMA	: End of DMA Interrupt
IF TEMP > HEX (1F) THEN GO TO PARERR	: Parity Error Interrupt
IF TEMP > HEX (03) THEN GO TO BYSERR	: Loss of Busy Interrupt
IF TEMP = HEX (00) THEN GO TO PHASERR	: Phase Mismatch Interrupt
Read Address 4 → TEMP	: Read Current SCSI Control Reg to variable TEMP
TEMP "AND" HEX (06) → TEMP	: Mask off irrevelant bits
IF TEMP = HEX (06) THEN GO TO RESEL	: Reselection Interrupt
IF TEMP = HEX (02) THEN GO TO SEL	: Selection Interrupt
IF TEMP = HEX (00) THEN GO TO RESET	: SCSI Bus Reset Interrupt

6

L5380/53C80. When reading or writing, external logic must be used to decode the L5380/53C80 location and produce $\overline{DACK}$, since it is used by the internal state machines. Also, $\overline{CS}$ must be suppressed since it may not be asserted simultaneously with $\overline{DACK}$.

Normal DMA Mode

Normal DMA mode is obtained when the DMAMODE bit is set but the Blockmode bit is reset. The DMA process is started by writing to the Start DMA Send, Start DMA Initiator Receive, or Start DMA Target Receive locations as appropriate. Once started, the internal state machines of the L5380/53C80 manage the $\overline{REQ}$ - $\overline{ACK}$ handshake protocol, as well as the DRQ-$\overline{DACK}$ handshake with the DMA controller.

The L5380/53C80 will assert DRQ whenever it is ready to transfer a byte to or from the DMA controller. In response to DRQ, the controller asserts $\overline{DACK}$ and $\overline{IOR}$ to read the byte, or $\overline{DACK}$ and $\overline{IOW}$ to write a byte to the L5380/53C80. For write operations, the byte is latched at the rising edge of the logical AND of $\overline{DACK}$ and $\overline{IOW}$. The transfer can be terminated by asserting $\overline{EOP}$ during a read or write operation, or by resetting the DMAMODE bit.

Block DMA Mode

When the Blockmode bit is set, the DMA handshake is no longer dependent on interlocked DRQ-$\overline{DACK}$ cycles. Instead, the DMA controller may be allowed to free-run, with data flow throttled by inserting "wait-states" in the DMA transfer to or from the L5380/53C80. Wait-states, which are idle clock cycles inserted during the I/O read or write operation, are inserted by the DMA controller until the READY output of the L5380/53C80 goes true, allowing the bus cycle to conclude.

The READY output will be deasserted under the following conditions: For send operations, READY will be false whenever the Output Data Register contains a byte which has not been transferred over the SCSI bus. This allows the DMA controller to access RAM to fetch the next byte, but postpones the end of the CPU bus cycle until the previous byte has been transferred, freeing the Output Data Register to receive it.

For receive operations, READY will be false whenever the Input Data Register is empty. This allows the DMA controller to address the RAM for a write operation, but postpones the end of the CPU bus cycle until the incoming byte is stored in the Input Data Register and is available on the CPU bus.

Note that when blockmode is employed, $\overline{DACK}$ may optionally remain asserted throughout the DMA transfer, since it is not used in an interlocked DMA handshake (Its interlock function is replaced by $\overline{IOR}$ or $\overline{IOW}$). Also, DRQ will be asserted in the normal way when operating in blockmode. To gain the abovementioned performance benefits, it should be used only to initiate the first byte transfer, with READY used to throttle succeeding transfers. This methodology is compatible with DMA controllers such as the Intel 8237 and AMD Am9516/9517.

In summary, blockmode operation offers the potential for improved transfer rates by overlapping the DMA memory access with the SCSI transfer. This is of particular value when used with DMA controllers capable of "flyby" operation, where the data is transferred directly from memory to the peripheral, and does not pass through the DMA controller itself. This transfer rate gain is achieved at the expense of locking up the CPU bus for a time equal to the SCSI transit time of the entire block. This may be strongly preferable in some systems where net disk access time is a crucial performance factor. Also, the time required to arbitrate for the CPU bus on a byte-by-byte basis may well be longer than the cycles wasted waiting for SCSI transfers to take place, especially with fast peripherals which operate from a high speed sector buffer.

Terminating DMA Transfers

DMA transfers, either normal or blockmode, may be terminated in a number of ways. The following sections describe these methods, along with providing information about correct sequencing of various signals to effect a clean exit from a DMA process.

$\overline{EOP}$ Signal

The $\overline{EOP}$ signal is usually generated by a DMA controller to indicate that its transfer counter has decremented to zero. In order to be recognized by the L5380/53C80, it should be asserted simultaneously with the $\overline{DACK}$ and $\overline{IOR}$ or $\overline{IOW}$ signals corresponding to the last byte in the transfer. Note that in the case of send operations, asserting $\overline{EOP}$ indicates to the L5380/53C80 that SCSI transfers should cease after transmission of the byte loaded while $\overline{EOP}$ is asserted. In order to determine when this last byte has actually been sent, the Last Byte Sent flag in the Target Command Register may be examined. This flag is not present in the NCR implementation of the 5380, but is available in the 53C80, a non-pin-compatible variant. The $\overline{EOP}$ input does not reset the DMAMODE bit, but after transmission of the last byte causes the internal state machine to return to an idle condition, so that no further SCSI handshaking will occur until another transmission is explicitly initiated. Note that the NCR version of the 5380, upon receiving an $\overline{EOP}$, will stop asserting DRQ, but will continue to issue $\overline{ACK}$ in response to additional $\overline{REQ}$ inputs,

potentially causing data loss if the target initiates another data transmission without an intervening phase change. The L5380/53C80 prevents this spurious DMA handshake from occurring.

DMA Mode Bit

Resetting the DMAMODE bit in the Mode Register causes a hard reset of the internal DMA state machines, and thus an effective termination of a DMA transfer. Since unlike the $\overline{EOP}$ case the state machine is not allowed to exit gracefully, care must be taken in the timing of DMAMODE reset.

For receive operations, the DMAMODE bit should be reset after the last $\overline{DRQ}$ is received, but prior to asserting $\overline{DACK}$ to prevent an additional $\overline{REQ}$ or $\overline{ACK}$ from occurring. For normal DMA mode, resetting this bit will cause DRQ to go inactive. However, the last byte received remains in the SCSI Input Data Register and may be read either by the normal $\overline{DACK}$ and $\overline{IOR}$ DMA read or using a CPU read of Address 6. For blockmode DMA, READY will remain asserted when DMAMODE is reset, allowing the DMA controller to retrieve the last byte in the normal fashion. The NCR version of the 5380 fails to keep READY asserted when DMAMODE is reset, potentially causing deadlock on the CPU bus.

Bus Phase Mismatch

When operating in DMAMODE as an initiator, a bus phase mismatch can be used to terminate a data transfer. If the $\overline{C}/D$, $\overline{I}/O$, and $\overline{MSG}$ lines fail to match the corresponding bits in the Target Command Register, it will prevent recognition of $\overline{REQ}$, and will disable the SCSI data and parity output drivers. Also, when $\overline{REQ}$ becomes active, an interrupt will be generated. Because $\overline{REQ}$ is not recognized, the effect is to stop the DMA transfer, although the state machine does not return to idle until either DMAMODE is reset or a valid $\overline{EOP}$ is received.

One caution should be observed when using phase changes to end DMA transfers: While this method does not require the initiator to keep a transfer counter, it depends on the target causing a phase change between any two consecutive information transfer phases. Since this is not required by the protocol, it must be guaranteed by the target software. Otherwise the target may begin a new information transfer without the initiator recognizing the boundary between the two.

ARBITRATION

The L5380/53C80 contains on-chip hardware to assist in arbitrating for the SCSI bus. This arbitration logic cooperates with the host firmware to effect SCSI arbitration, as described in the following paragraphs:

The SCSI arbitration timeline begins with detection of a bus free condition at time t_0. Bus free is defined as $\overline{BSY}$ and $\overline{SEL}$ inactive for at least a bus settle delay (400 ns). Following the bus settle delay, the SCSI device must wait an additional bus free delay of 800 ns, for a total of 1200 ns after t_0, prior to driving any signal. Thus a minimum of 1200 ns must elapse from initial deassertion of $\overline{BSY}$ to the beginning of an arbitration attempt. A final constraint is that arbitration may not begin if more than a bus set delay (1800 ns) has elapsed since $\overline{BSY}$ became active (arbitration began), corresponding to 2200 ns after t_0.

The CPU indicates a desire to arbitrate by setting the Arbitrate bit (R2 bit 0). When Arbitrate is set, the L5380/53C80 will monitor the state of $\overline{BSY}$ and $\overline{SEL}$ to detect a bus free condition. The actual implementation uses an internal delay line to provide a time reference for detection of a bus free condition. This delay is nominally 800 ns during which $\overline{BSY}$ and $\overline{SEL}$ must be inactive. This time represents the center of the window between the Bus Settle Delay (400 ns) and the Bus Free Delay (400 + 800 = 1200 ns). When Bus Free is detected, the L5380/53C80 waits for an additional time of nominally 900 ns (1700 ns nominal since t_0) and asserts $\overline{BSY}$ and the contents of the Output Data Register. This time represents the center of the 1200 ns–2200 ns window between the earliest and latest legal arbitration attempt. Since the actual delays are process and temperature dependent, they will vary in practice, but will always remain well within the specified limits.

Once arbitration has begun ($\overline{BSY}$ and the Output Data Register asserted,) the Arbitration In Progress bit (R1 bit 6) will be set, allowing the CPU to detect the fact that arbitration has begun. The CPU should then wait one arbitration delay (2.2 µs) before reading the bus to determine whether arbitration has been won or lost. The Lost Arbitration bit (R2 bit 7) will be active if the L5380/53C80 has detected $\overline{SEL}$ active on the SCSI bus, indicating that another SCSI device has declared itself the winner of the arbitration. $\overline{SEL}$ active also disables the SCSI output drivers, allowing the winning arbitrator to proceed with its transfer.

BUG FIXES/ENHANCMENTS

The NCR5380 and the Am5380 have some architectural bugs, both published and unpublished. The **LOGIC Devices L5380/53C80** was designed to eliminate these bugs while maintaining pin and architectural compatibility. A list of these errors along with solutions implemented in the L5380/53C80 is itemized below.

1. When executing blockmode DMA send operations, the READY signal is intended to insert memory wait states as a mechanism to throttle data transfer, with the DMA controller in a free-running loop. The NCR/Am5380 erroneously allows the contents of the Output Data Register to be overwritten by subsequent bytes prior to acknowledgment of the

current byte by the SCSI receiver. This causes loss of data when operating in blockmode if the sender's DMA cycle is faster than the receiver's.

2. Assertion of $\overline{EOP}$ during blockmode DMA transfers fails to cause assertion of READY in the NCR/Am5380. This may prevent the CPU from becoming bus master and can result in lockup of the CPU bus in a not-ready state. In block DMA send mode when $\overline{EOP}$ is received, the L5380/53C80 reasserts READY immediately after transmitting the final byte. For receive mode, READY is asserted immediately.

3. When a valid $\overline{EOP}$ is detected, the NCR/Am5380 prevents assertion of additional DRQ's, but continues to respond to SCSI handshakes. This means that additional data transmitted without phase change may be lost. The L5380/53C80, like the NCR/Am5380 remains in DMAMODE after an $\overline{EOP}$. However, the internal state machine returns to an idle condition and does not respond to additional SCSI handshake attempts until another data transfer is explicitly initiated.

4. When operating as an initiator in DMAMODE, the NCR/Am5380 leaves $\overline{ACK}$ asserted after receipt of a valid $\overline{EOP}$, requiring the CPU to deassert it. When a valid $\overline{EOP}$ is detected, the L5380/53C80 deasserts $\overline{ACK}$ properly.

5. If the NCR/Am5380 is not terminated on the SCSI side, the floating $\overline{RST}$ pin will cause spurious interrupts. The L5380/53C80 contains internal high value pullups to set unterminated SCSI pins to the inactive state.

6. During DMA send operations, when a valid $\overline{EOP}$ signal is received by the NCR/Am5380, no convenient indication exists to indicate that the last byte of data (loaded simultaneously with $\overline{EOP}$) has in fact been successfully transmitted. The L5380/53C80 provides Last Byte status bit mapped to bit 7 of the Target Command Register. This bit will be set after a valid $\overline{EOP}$ has occurred, and the final byte has been transmitted successfully.

7. During the reselection phase, the NCR/AM5380 may reset the reselection interrupt if the contents of the Target Command Register do not match the current SCSI bus phase. The L5380/53C80 does not spuriously reset this interrupt.

8. In the NCR/Am5380, the phase mismatch interrupt is captured in an edge triggered fashion on the active edge of $\overline{REQ}$. During reselection, this interrupt might not be generated even though a phase change has occurred. The reason for this is as follows:

- The initiator DMAMODE bit must be set in order to receive a phase-match interrupt.
- However, the DMAMODE bit cannot be set unless $\overline{BSY}$ is active.
- $\overline{BSY}$ will be driven active by the target only after the relesection has occurred.
- Once $\overline{BSY}$ has been asserted by the target, it may then assert $\overline{REQ}$ before the initiator has set the DMAMODE bit, and the initiator will then fail to generate an interrupt.

The L5380/53C80 interrupt latch will be set if a phase mismatch condition exists when the later of $\overline{REQ}$ or DMAMODE become active. In this way, the mismatch will always be detected, even if the target asserts $\overline{REQ}$ before the initiator sets DMAMODE.

MAXIMUM RATINGS *Above which useful life may be impaired*

Storage temperature	–65°C to +150°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Output voltage	0.0 V to V_{CC}
Input voltage	0.0 V to +5.5 V
I_{OL} Low Level Output Current (SCSI Bus)	48 mA
I_{OL} Low Level Output Current (other pins)	8 mA
I_{OH} High Level Output Current (other pins)	–4 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

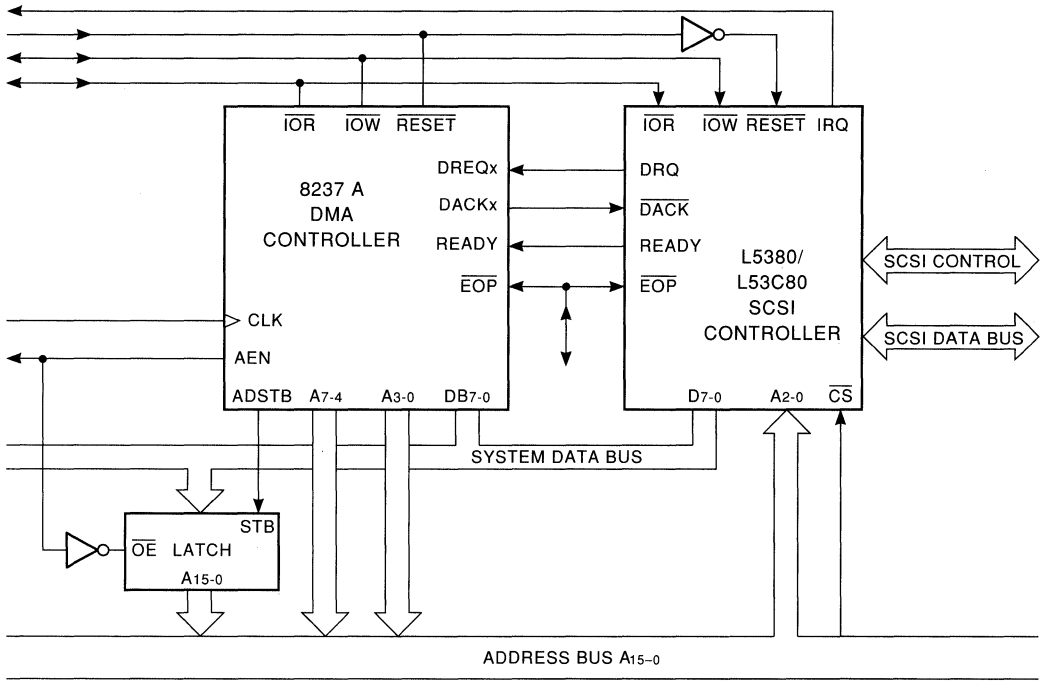
6

ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		0.0		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{OL}	Output Low Voltage (SCSI bus)	V_{CC} = Min, I_{OL} = 48 mA			0.5	V
V_{OL}	Output Low Voltage (other pins)	V_{CC} = Min, I_{OL} = 8 mA			0.5	V
V_{OH}	Output High Voltage (other pins)	V_{CC} = Min, I_{OH} = –4 mA	3.5			V
I_{IN}	Input Current*	V_{CC} = Max, V_{IN} = 0 – V_{CC} (SCSI bus)			65	µA
I_{IN}	Input Current*	V_{CC} = Max, V_{IN} = 0 – V_{CC} (other pins)			20	µA
I_{CC}	Supply Current	V_{CC} = Max, V_{IH} = 2.4, VIL = 0.4, 4 MHz cycle, No Load, No Termination		10	20	mA
I_{CC}	Supply Current Quiescent	Same as above, inputs stable			1.0	mA

*Not tested at low temperature extreme.

DMA Interface with 8237 A

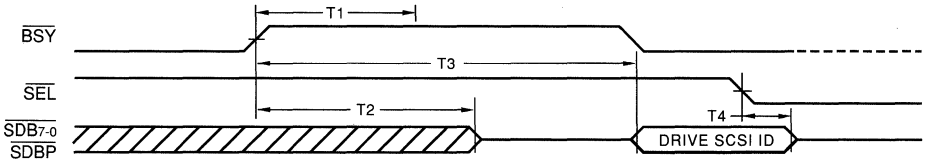


SWITCHING CHARACTERISTICS

Arbitration Timing *(ns — except where noted)*

Symbol	Parameter	L5380/53C80– Commercial Min	Commercial Max	Military Min	Military Max
T1	$\overline{BSY}$ False Duration to Detect Bus Free Condition	0.4 µs	1.2 µs	0.4 µs	1.2 µs
T2	SCSI Bus Clear (High Z) from $\overline{BSY}$ False		1.2 µs		1.2 µs
T3	Arbitrate ($\overline{BSY}$ and SCSI ID Asserted) from $\overline{BSY}$ False (Bus Free Detected)	1.2 µs	2.2 µs	0.8 µs	2.4 µs
T4	SCSI Bus Clear (High Z) from $\overline{SEL}$ True (Lost Arbitration)		60		60

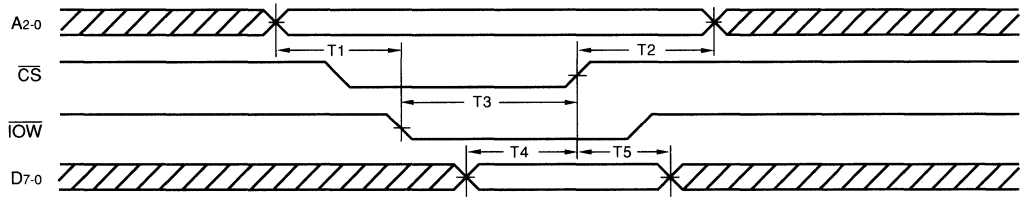
Arbitration Waveforms



CPU Write Cycle Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max	Military 2 Mbytes/sec Min	Military 2 Mbytes/sec Max
T1	Address Setup to Write Enable	10		5		10	
T2	Address Hold from End of Write Enable	5		5		5	
T3	Width of Write Enable	40		20		40	
T4	Data Setup to End of Write Enable	20		5		20	
T5	Data Hold from End of Write Enable	10		5		10	

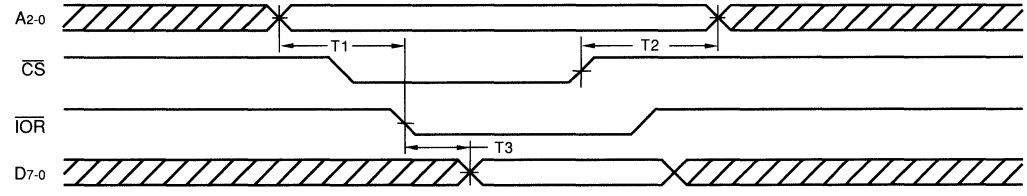
CPU Write Cycle Waveforms



CPU Read Cycle Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max	Military 2 Mbytes/sec Min	Military 2 Mbytes/sec Max
T1	Address Setup to Read Enable	10		5		10	
T2	Address Hold from End of Read Enable	5		5		5	
T3	Data Access Time from Read Enable		50		20		50

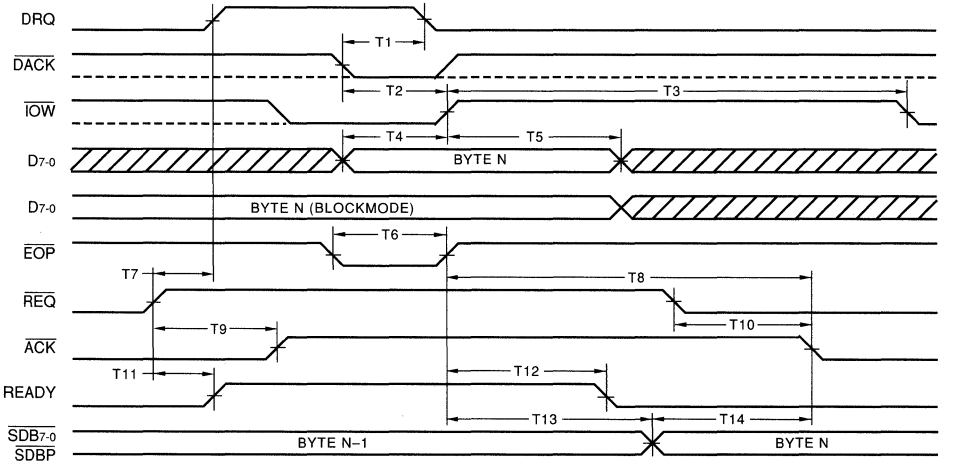
CPU Read Cycle Waveforms



DMA Write Initiator Send Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max	Military 2 Mbytes/sec Min	Military 2 Mbytes/sec Max
	The following apply for all DMA Modes						
T1	DRQ False from Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)		60		30		60
T2	Width of Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)	60		20		60	
T4	Data Setup to End of Write Enable	20		5		20	
T5	Data Hold from End of Write Enable	15		5		15	
T6	Concurrent Width of $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$	50		20		50	
T9	$\overline{REQ}$ False to $\overline{ACK}$ False		90		45		90
T13	End of Write Enable to Valid SCSI Data		65		45		65
T14	SCSI Data Setup Time to $\overline{ACK}$ True	60		65		60	
	The following apply for Normal DMA Mode only						
T7	$\overline{REQ}$ False to DRQ True		60		30		60
T8	$\overline{DACK}$ False to $\overline{ACK}$ True ($\overline{REQ}$ True)		140		140		140
T10	$\overline{REQ}$ True to $\overline{ACK}$ True ($\overline{DACK}$ False)		70		35		70
	The following apply for Blockmode DMA only						
T3	$\overline{IOW}$ Recovery Time	40		20		40	
T8	$\overline{IOW}$ False to $\overline{ACK}$ True ($\overline{REQ}$ True)		140		140		140
T10	$\overline{REQ}$ True to $\overline{ACK}$ True ($\overline{IOW}$ False)		70		35		70
T11	$\overline{REQ}$ False to READY True		60		30		60
T12	$\overline{IOW}$ False to READY False		70		35		70

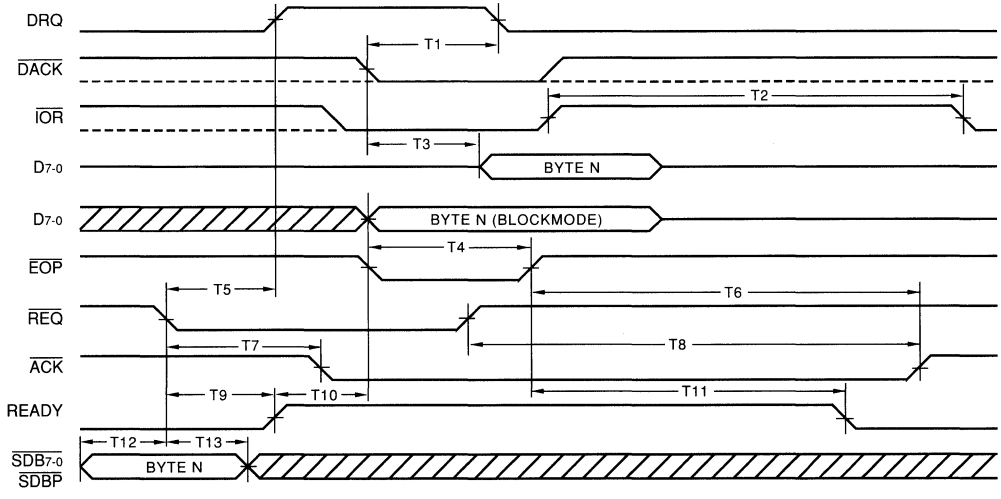
DMA Write Initiator Send Waveforms



DMA Read Initiator Receive Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max	Military 2 Mbytes/sec Min	Military 2 Mbytes/sec Max
	The following apply for all DMA Modes						
T1	DRQ False from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		30		60
T3	Data Access Time from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		20		60
T4	Concurrent Width of $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$	50		20		50	
T7	$\overline{REQ}$ True to $\overline{ACK}$ True		70		35		70
T12	SCSI Data Setup Time to $\overline{REQ}$ True	20		5		20	
T13*	SCSI Data Hold Time from $\overline{REQ}$ True	15		10		15	
	The following apply for Normal DMA Mode only						
T5	$\overline{REQ}$ True to DRQ True		60		30		60
T6	$\overline{DACK}$ False to $\overline{ACK}$ False ($\overline{REQ}$ False)		90		55		90
T8	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{DACK}$ False)		80		55		80
	The following apply for Blockmode DMA only						
T2	$\overline{IOR}$ Recovery Time	40		20		40	
T6	$\overline{IOR}$ False to $\overline{ACK}$ False ($\overline{REQ}$ False)		90		45		90
T8	$\overline{REQ}$ False to $\overline{ACK}$ False ($\overline{IOR}$ False)		80		45		80
T9	$\overline{REQ}$ True to READY True		60		30		60
T10	READY True to CPU Data Valid		15		15		15
T11	$\overline{IOR}$ False to READY False		70		35		70

DMA Read Initiator Receive Waveforms

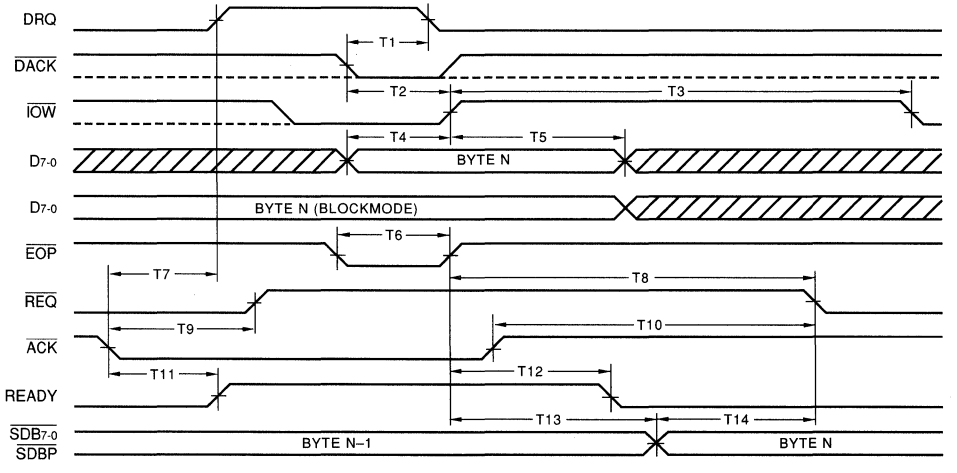


*Data must be held on the SCSI bus until $\overline{ACK}$ becomes True

DMA Write Target Send Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max	Military 2 Mbytes/sec Min	Military 2 Mbytes/sec Max
	The following apply for all DMA Modes						
T1	DRQ False from Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)		60		30		60
T2	Width of Write Enable (concurrence of $\overline{IOW}$ and $\overline{DACK}$)	60		20		60	
T4	Data Setup to End of Write Enable	20		5		20	
T5	Data Hold from End of Write Enable	15		5		15	
T6	Concurrent Width of $\overline{EOP}$, $\overline{IOW}$, and $\overline{DACK}$	50		20		50	
T9	$\overline{ACK}$ True to $\overline{REQ}$ False		90		45		90
T13	End of Write Enable to Valid SCSI Data		60		45		60
T14	SCSI Data Setup Time to $\overline{REQ}$ True	60		65		60	
	The following apply for Normal DMA Mode only						
T7	$\overline{ACK}$ True to DRQ True		60		30		60
T8	$\overline{DACK}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		130		130		140
T10	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{DACK}$ False)		70		35		70
	The following apply for Blockmode DMA only						
T3	$\overline{IOW}$ Recovery Time	40		20		40	
T8	$\overline{IOW}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		130		130		140
T10	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{IOW}$ False)		70		35		70
T11	$\overline{ACK}$ True to READY True		60		30		60
T12	$\overline{IOW}$ False to READY False		70		35		70

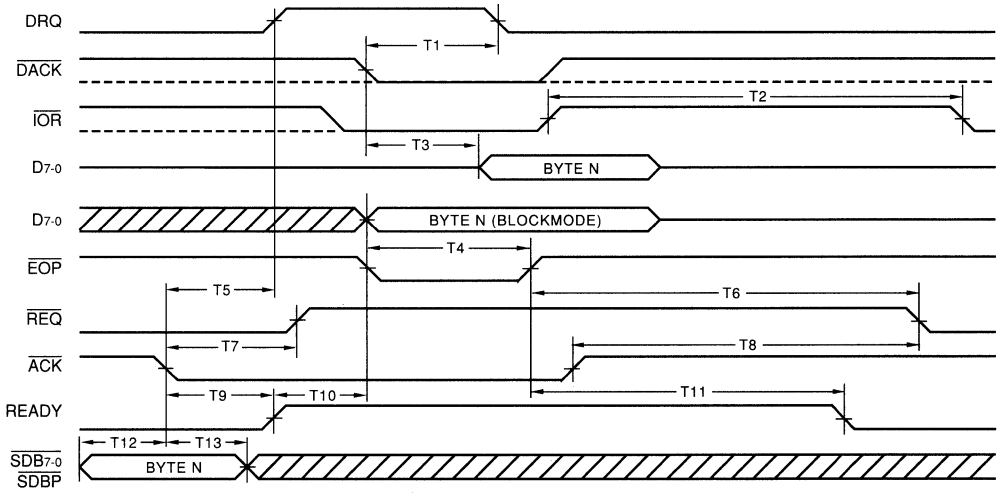
DMA Write Target Send Waveforms



DMA Read Target Receive Timing *(ns)*

Symbol	Parameter	Commercial 2 Mbytes/sec Min	Commercial 2 Mbytes/sec Max	Commercial 4 Mbytes/sec Min	Commercial 4 Mbytes/sec Max	Military 2 Mbytes/sec Min	Military 2 Mbytes/sec Max
	The following apply for all DMA Modes						
T1	DRQ False from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		30		60
T3	Data Access Time from Concurrence of $\overline{IOR}$ and $\overline{DACK}$		60		20		60
T4	Concurrent Width of $\overline{EOP}$, $\overline{IOR}$, and $\overline{DACK}$	50		20		50	
T7	$\overline{ACK}$ True to $\overline{REQ}$ False		70		45		70
T12	SCSI Data Setup Time to $\overline{ACK}$ True	20		10		20	
T13*	SCSI Data Hold Time from $\overline{ACK}$ True	15		10		15	
	The following apply for Normal DMA Mode only						
T5	$\overline{ACK}$ True to DRQ True		60		30		60
T6	$\overline{DACK}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		90		45		90
T8	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{DACK}$ False)		80		45		80
	The following apply for Blockmode DMA only						
T2	$\overline{IOR}$ Recovery Time	40		20		40	
T6	$\overline{IOR}$ False to $\overline{REQ}$ True ($\overline{ACK}$ False)		90		45		90
T8	$\overline{ACK}$ False to $\overline{REQ}$ True ($\overline{IOR}$ False)		80		45		80
T9	$\overline{ACK}$ True to READY True		60		30		60
T10	READY True to CPU Data Valid		15		15		15
T11	$\overline{IOR}$ False to READY False		70		35		70

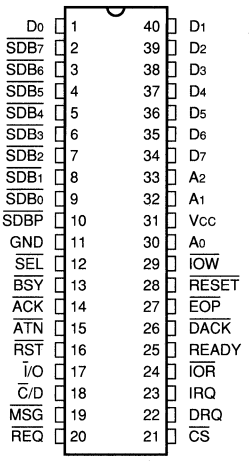
DMA Read Target Receive Waveforms

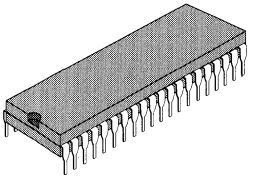


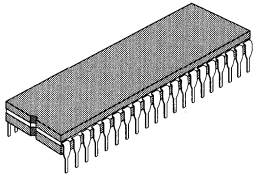
*Data must be held on the SCSI bus until $\overline{REQ}$ becomes False

L5380 — ORDERING INFORMATION

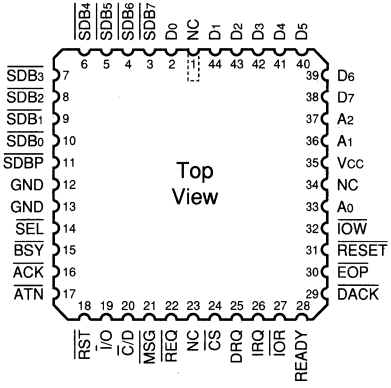
40-pin — 0.6" wide

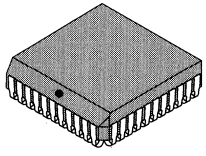


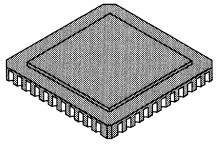




44-pin



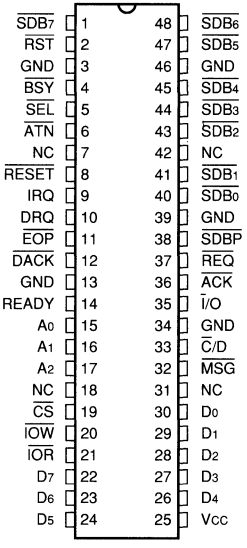




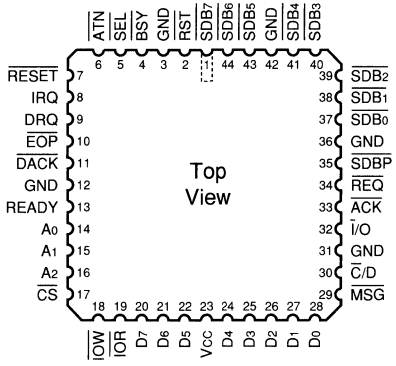
Speed	Plastic DIP (P3)	Ceramic DIP (C11)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — COMMERCIAL SCREENING			
4	L5380PC4	L5380CC4	L5380JC4	L5380KC4
2	L5380PC2	L5380CC2	L5380JC2	L5380KC2
	–55°C to +125°C — COMMERCIAL SCREENING			
2		L5380CM2		L5380KM2
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
2		L5380CMB2		L5380KMB2

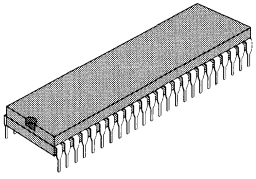
L53C80 — ORDERING INFORMATION

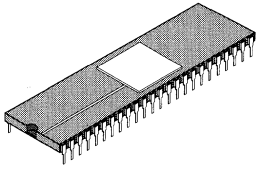
48-pin

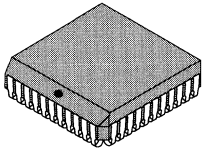


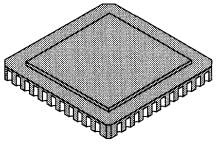
44-pin











Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic J-Lead Chip Carrier (J1)	Ceramic Leadless Chip Carrier (K2)
	0°C to +70°C — COMMERCIAL SCREENING			
4	L53C80PC4	L53C80DC4	L53C80JC4	L53C80KC4
2	L53C80PC2	L53C80DC2	L53C80JC2	L53C80KC2
	–55°C to +125°C — COMMERCIAL SCREENING			
2		L53C80DM2		L53C80KM2
	–55°C to +125°C — MIL-STD-883 COMPLIANT			
2		L53C80DMB2		L53C80KMB2

6

Ordering Information 1
Video Imaging Products 2
Arithmetic Logic Units & Special Arithmetic Functions 3
Multipliers & Multiplier-Accumulators 4
Register Products 5
Peripheral Products 6
Quality and Reliability 7
Technology and Design Features 8
Package Information 9
Product Listing 10
Sales Offices 11

Quality and Reliability

Copies of the LOGIC Devices **"Quality Assurance Program Manual"** and **"Reliability Manual"** may be obtained from LOGIC Devices by contacting our applications group at (408) 737-3346 between 8:00 AM and 6:00 PM Pacific time, Monday through Friday.

Ordering Information 1
Video Imaging Products 2
Arithmetic Logic Units & Special Arithmetic Functions 3
Multipliers & Multiplier-Accumulators 4
Register Products 5
Peripheral Products 6
Quality and Reliability 7
Technology and Design Features 8
Package Information 9
Product Listing 10
Sales Offices 11

Technology and Design Features

TECHNOLOGY AND DESIGN FEATURES 8-1
Latchup and ESD Protection 8-3
Power Dissipation in LOGIC Devices Products 8-7

Latchup and ESD Protection

Latchup is a destructive phenomenon which was once common in CMOS circuits but has now been largely eliminated by improved circuit design techniques. Latchup takes place because of the existence in CMOS of an inherent PNPN or NPNP structure between VCC and ground. Either of these two can form a pair of transistors connected so as to form a positive feedback loop, with the collector of one transistor driving the base of the other. The result is a low-impedance path from VCC to ground, which cannot be interrupted except by the removal of power. This condition can be destructive if the area involved is sufficiently large to dissipate excessive power. One example of the formation of such a structure is shown in Figure 1. The equivalent circuit is shown in Figure 2.

As shown in Figure 1, the N+ regions which form the source and drain of an N-channel MOS transistor also act as the emitters of a parasitic NPN transistor. The P-well forms the base region and the N-substrate is the collector. The current gain of this transistor is relatively high because it is formed vertically and therefore the base width is quite small. This is especially true of fine-geometry CMOS processes which tend to have very shallow wells to reduce sidewall capacitance. The P+ region in the well is called a "well tap" and is present to form a low-resistance connection between the well and ground. The source region cannot serve this function because it forms a diode between the N+ source and the P-well.

Also shown in Figure 1 is an additional parasitic PNP transistor. The source and drain regions of the P-channel MOS device form the emitters, the N-substrate is the base, and the P-well is the collector. This transistor is a PNP, and generally has a beta (β) much less than 1 since it is formed laterally and the gate region is relatively large. Like the vertical NPN, it can have multiple emitters. The N+ region tied to VCC in the substrate functions similarly to the well tap discussed above.

Note that the base of the NPN and the collector of the PNP are a common region (the P-well), and similarly the base of the PNP and the collector of the NPN are common (the N-substrate). Thus, the PNPN structure necessary for latchup is formed. Also, due to the the physical distance between the well and substrate taps and the base regions which they attempt to contact, a small resistance exists between the base regions and their respective well taps, denoted RS (substrate) and RW (well).

Latchup begins when a perturbation causes one of the bipolar transistors to turn on. An example would be excursion of the output pad below ground or above VCC due to transmission-line ringing. If the pad goes more than 0.7 V below ground, the NPN will turn on since its base is at approximately ground potential. The NPN's collector current will cause a voltage drop across RS, the bulk substrate resistance. This voltage drop turns on the PNP.

The PNP transistor's collector current forces a similar voltage drop across RW, the well resistance. This raises the base voltage of the NPN above ground and can cause the NPN to continue to conduct even after the output pad returns to a normal voltage range. In this case, the current path shifts to the grounded emitter.

Note that any effect which can cause a transient turn-on of either transistor can cause the latchup process. Common causes include:

1. Ringing of unprotected I/O pins outside the ground to VCC region.
2. Radiation-induced carriers generated in the base of the bipolar transistors.
3. Hot-powerup of the device, with inputs driven HIGH before VCC is applied.
4. Electrostatic discharge.

PROTECTING AGAINST LATCHUP

Latchup, while once a severe problem for CMOS, is now a relatively well-understood phenomenon. In order for latchup to occur, the product of the current gains of the two parasitic transistors must exceed 1. Thus, the primary means for avoiding latchup is the insertion of structures known as "guard rings" around all MOS transistors (and other structures) likely to be subjected to latchup-causing transients. This includes output buffer transistors and any devices which form a part of the ESD protection network. These guard rings absorb current which would otherwise drive the base of the lateral device, and thus dramatically reduce its gain.

Since external electrical perturbations are the dominant cause of latchup in non-radiation environments, protecting the "periphery" of the chip is most important. Therefore, since guard rings require a lot of area, they are generally used only in critical areas such as those mentioned above.

As an additional protective measure, strict rules are enforced in the layout regarding the positioning of the substrate and well taps. They are spaced closely together throughout

FIGURE 1. PARASITIC TRANSISTOR STRUCTURES IN PARALLEL CMOS

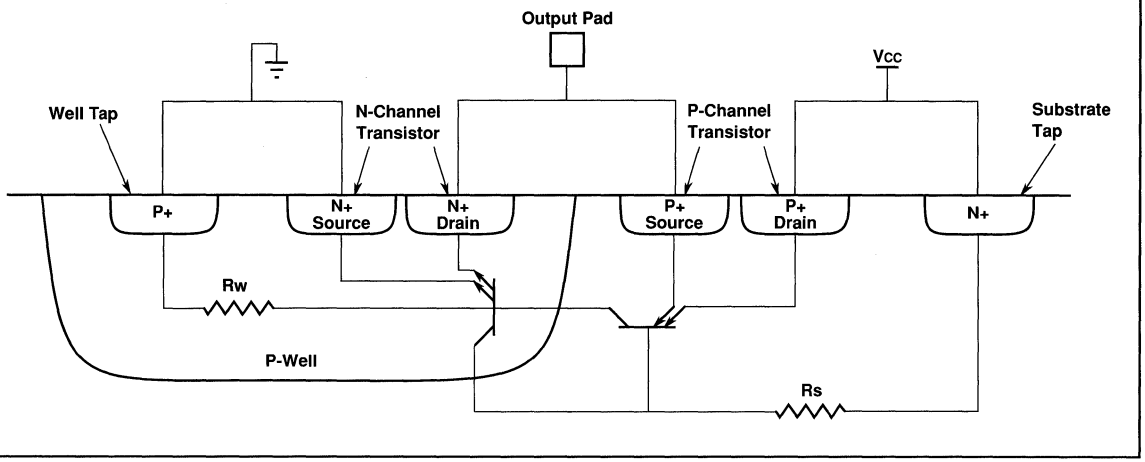
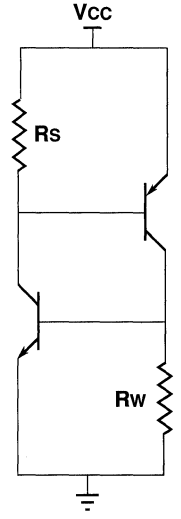


FIGURE 2. EQUIVALENT CIRCUIT FOR LATCHUP PATH



the die, reducing the values of RS and RW. This makes it more difficult to develop the base drive necessary to regenerate the latchup condition.

Measurement of susceptibility to latchup is done by connecting a current source to an input or output of the device under test. By increasing the current forced to flow into the pin and noting the point at which latchup occurs, a measure of the device's ability to resist latchup-inducing carrier injection is obtained. Note that depending on the device, the current source may require a rather large voltage compliance in order to provide an adequate test.

While early CMOS devices had a latchup trigger current of a few tens of milliamps, most current LOGIC Devices products typically can withstand more than 1 amp without latching. As a result, latchup is no longer a practical concern, except for extreme conditions such as driving multiple inputs HIGH with a low-impedance source during powerup of the device.

ELECTROSTATIC DISCHARGE

Input protection structures on CMOS devices are used to protect against damage to the gate oxides of input transistors when accumulated static charge is discharged through a device. This charge can often reach potentials of several thousand volts. The input protection network is designed to shunt this charge safely to ground or VCC, bypassing the delicate MOS transistors.

Several features are required of a good input protection network. Since static discharge pulses exhibit very fast rise-times, it must have a very fast turn-on time. It must be capable of carrying large instantaneous currents without damage. It must prevent the voltage

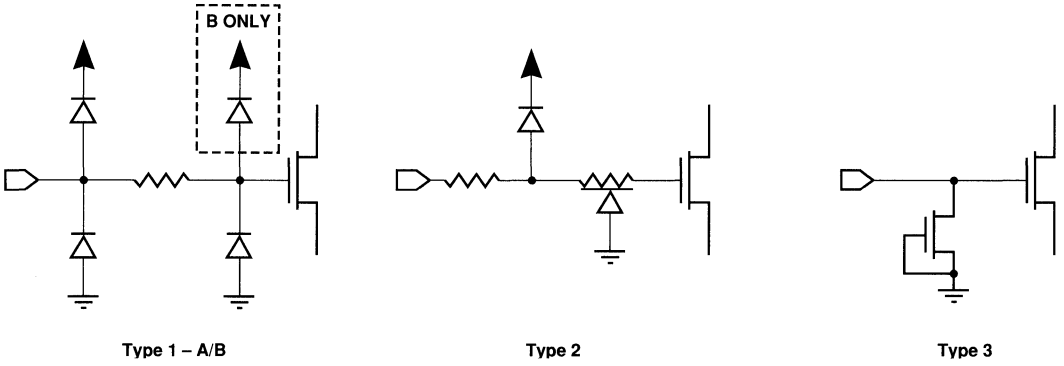
at the circuit input from rising above approximately 10 V during the time when the several-thousand-volt discharge is shunted to ground. It must not create appreciable delay for fast edges which are within the 0–5 V input range. And finally, it must be well protected against latchup caused by inputs which are driven beyond the supply rails, injecting current into the substrate. Much research and experimentation has been devoted to optimizing the tradeoffs between these conflicting goals.

All LOGIC Devices products employ one of the three input protection structures shown in Figure 3. Most devices currently use the Type 1 input protection. This structure is designed to absorb very high static discharge energies and will draw substantial current from the input pin if driven beyond either supply rail. Hence, it provides a "hard" clamp. Besides its advantages for static protection, this clamp can effectively reduce undershoot energy, preventing oscillation of an unterminated input back above the 0.8 V V_{IL} MAX level. This makes the circuit ideal for noisy environments and ill-behaved signals. This input structure may not be driven to a high level without power applied to the device, however. To do so would result in current flowing through the diode connected to the device's V_{CC} rail, and supplying power to the entire board or system backward through the device V_{CC} pin. This may overstress the bond wire or device metallization, resulting in failure.

The Type 2 structure employs a series resistor prior to the two clamp diodes. This results in a "soft" clamping effect. This structure will withstand the transient application of voltages outside the supply rails for brief periods without drawing excessive current. In contrast to the Type 1 structure, this circuit will provide only a modest reduction of the energy in an undershoot pulse. However, it is somewhat more tolerant of power-up sequences which cause the inputs to be driven before V_{CC} is applied. In the course of routine product upgrades, devices employing this structure are being redesigned to use a Type 1 input protection.

The Type 3 structure uses a large area N-channel transistor (part of an open-drain output buffer) to protect the input. The drain-well junction of this device serves the function of a diode connected between the input and ground, protecting against negative excursions of the input. The avalanche breakdown of the output device serves to protect against positive pulses, giving the effect of a zener diode between the input and ground. This circuit is used only for inputs which are designed to have their inputs driven without power applied. The lack of a diode to V_{CC} prevents sourcing of power from the inputs to the V_{CC} supply.

FIGURE 3. INPUT PROTECTION DEVICES



8

Power Dissipation in LOGIC Devices Products

In calculating the power dissipation of LOGIC Devices products, attention must be given to a number of formerly second-order effects which were generally ignored when dealing with bipolar and NMOS technologies. By far the dominant contributor to power dissipation in most CMOS devices is the effective current path from the supply to ground, created by the repetitive charging and discharging of the load capacitance. This is distinct from DC loading effects, which may also consume power. The power dissipated in the load capacitance is proportional to CV^2F, where C is the load capacitance, V is the voltage swing, and F is the switching frequency. This mechanism can frequently contribute 80% or more of the total device dissipation of a truly complementary device operating at a high clock rate.

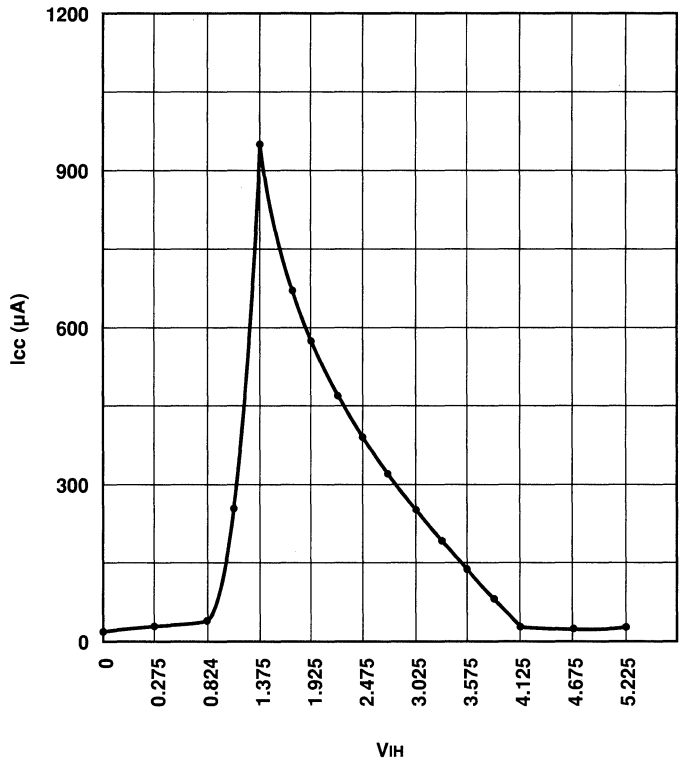
The second contributor to the power dissipation of a CMOS device is the DC current path between V_{CC} and ground present in the input level translators. These circuits are voltage amplifiers which are designed to convert worst case 0.8–2.0 V TTL-compatible input levels to 0 and 5 V internal levels. With 2.0 V applied to the input of most level translator circuits, about 1 mA will flow from the power supply to ground. A floating input will at best have similar results, and may result in oscillations which can dissipate orders of magnitude more power and cause malfunctioning of the device.

The power dissipation of input level translators exhibits a strong peak at about 1.4 V but is reduced substantially when the input voltage exceeds 3.0 V (see Figure 1). Fortunately, this voltage is easy to achieve in practice, even for bipolar devices with TTL I/O structures. These generally will produce a V_{OH} of at least 3.5 V if not fully loaded. As a result, dissipation in the input structures is usually negligible compared to other sources.

Two further sources of power dissipation in CMOS come from the core logic. The sources of internal power dissipation are the same as those discussed for external nodes, namely repetitive charging of the parasitic load capacitances on each gate output, and the power drawn due to a direct current path to ground when gate input voltage levels transition through the linear region. In practice, the internal voltage waveforms are characterized by high edge rates and rail-to-rail swings. For this reason, the latter source of dissipation is usually negligible, unless NMOS or other non-complementary logic design techniques have been used.

The capacitance of typical internal nodes in CMOS logic circuits are a few femtofarads. However, there can be thousands, or tens of thousands of such nodes. As a result, the core

FIGURE 1.



8

power dissipation is strongly dependent on the average rate at which these nodes switch (the "F" in CV^2F). Fortunately, for most complex logic circuits, with non-pathological external stimulus only a small fraction of the logic nodes switch on any given cycle. For this reason, internal power is generally quite small for these device types. Exceptions include devices containing long shift registers or other structures which can exhibit high duty cycles on most internal nodes. These devices can dissipate significant power in the core logic if stimulated with alternating data patterns and clocked at a high rate.

To summarize, of the several contributors to power dissipation, the CV^2F power of the outputs is usually dominant. Because output loading is system-dependent, it is not possible for the manufacturer to accurately predict total power dissipation in actual use. As a result, LOGIC Devices extrapolates measured power dissipation values to a zero-load environment and publishes the resulting value. This value includes the effects of worst-case input and power-supply voltages, temperature, and stimulus pattern, but not CV^2F. This value is weakly frequency dependent, and the frequency at which it is measured is published in the device data sheet. The maximum value is for worst-case pattern, and the typical is for a more random pattern and is therefore more representative of what would be experienced in actual practice.

A good estimate of total power dissipation in a particular system under worst-case conditions can be obtained by adding the calculated output power to the *typical* published figure. The output power is given by:

$$\frac{NCV^2F}{4}$$

where:

N = the number of device outputs (divided by 2 to account for the assumption that on average, half of the outputs switch on any given cycle)

C = the output load capacitance, per pin, given in Farads

V = the power supply voltage

F = the clock frequency (divided by 2 to account for the fact that a registered output can at most switch at only half the clock rate).

A less pessimistic estimate, appropriate for complex devices when reasonable input voltage levels and non-pathological patterns can be expected, would neglect the published value and use only the calculated value as given above.

Ordering Information 1
Video Imaging Products 2
Arithmetic Logic Units & Special Arithmetic Functions 3
Multipliers & Multiplier-Accumulators 4
Register Products 5
Peripheral Products 6
Quality and Reliability 7
Technology and Design Features 8
Package Information 9
Product Listing 10
Sales Offices 11

Package Information

PACKAGE INFORMATION 9-1

LOGIC Devices/MIL-STD-1835 Package Code Cross-Reference 9-3

Thermal Considerations 9-5

Package Marking Guide 9-7

Mechanical Drawings

Ceramic DIP (Ordering Code: C, I) 9-10

C1 24-pin, 0.3" wide 9-10

C2 20-pin, 0.3" wide 9-10

C3 22-pin, 0.3" wide 9-11

C4 24-pin, 0.6" wide 9-11

C5 28-pin, 0.3" wide 9-12

C6 28-pin, 0.6" wide 9-12

C7 16-pin, 0.3" wide 9-13

C8 18-pin, 0.3" wide 9-13

C9 32-pin, 0.6" wide 9-14

C10 28-pin, 0.4" wide 9-14

C11 40-pin, 0.6" wide 9-15

Sidebraze, Hermetic DIP (Ordering Code: D, H) 9-16

D1 24-pin, 0.6" wide 9-16

D2 24-pin, 0.3" wide 9-16

D3 40-pin, 0.6" wide 9-17

D4 64-pin, 0.9" wide, cavity up 9-17

D5 48-pin, 0.6" wide 9-18

D6 64-pin, 0.9" wide, cavity down 9-18

D7 20-pin, 0.3" wide 9-19

D8 22-pin, 0.3" wide 9-19

D9 28-pin, 0.6" wide 9-20

D10 28-pin, 0.3" wide 9-20

D11 28-pin, 0.4" wide 9-21

Commercial PGA (Ordering Code: E) 9-22

E1 68-pin, cavity up 9-22

E2 68-pin, cavity down 9-22

E3 120-pin 9-23

Ceramic PGA (Ordering Code: G) 9-24

G1 68-pin, cavity up 9-24

G2 68-pin, cavity down 9-24

G3 84-pin 9-25

G4 120-pin 9-25

Plastic J-Lead Chip Carrier (Ordering Code: J) 9-26

J1 44-pin, 0.690" x 0.690" 9-26

J2 68-pin, 0.990" x 0.990" 9-26

J3 84-pin, 1.190" x 1.190" 9-27

J4 28-pin, 0.490" x 0.490" 9-27

Package Information

Plastic J-Lead Chip Carrier (Continued)

J5 52-pin, 0.790" x 0.790" 9-28
J6 32-pin, 0.490" x 0.590" 9-28
J7 20-pin, 0.390" x 0.390" 9-29

Ceramic Leadless Chip Carrier (Ordering Code: K, T) 9-30

K1 28-pin, 0.450" x 0.450" 9-30
K2 44-pin, 0.650" x 0.650" 9-30
K3 68-pin, 0.950" x 0.950" 9-31
K4 22-pin, 0.290" x 0.490" 9-31
K5 28-pin, 0.350" x 0.550" 9-32
K6 20-pin, 0.290" x 0.425" 9-32
K7 32-pin, 0.450" x 0.550" 9-33
K8 20-pin, 0.350" x 0.350" 9-33
K9 48-pin, 0.550" x 0.550" 9-34

Ceramic Flatpack (Ordering Code: M) 9-35

M1 24-pin 9-35
M2 28-pin 9-35

Plastic DIP (Ordering Code: P, N) 9-36

P1 24-pin, 0.6" wide 9-36
P2 24-pin, 0.3" wide 9-36
P3 40-pin, 0.6" wide 9-37
P4 64-pin, 0.9" wide 9-37
P5 48-pin, 0.6" wide 9-38
P6 20-pin, 0.3" wide 9-38
P7 32-pin, 0.3" wide 9-39
P8 22-pin, 0.3" wide 9-39
P9 28-pin, 0.6" wide 9-40
P10 28-pin, 0.3" wide 9-40
P11 28-pin, 0.4" wide 9-41
P12 16-pin, 0.3" wide 9-41
P13 18-pin, 0.3" wide 9-42
P14 32-pin, 0.6" wide 9-42
P15 32-pin, 0.4" wide 9-43

Plastic Quad Flatpack (Ordering Code: Q) 9-44

Q1 120-pin 9-44
Q2 100-pin 9-45

Plastic SOJ (Ordering Code: W) 9-46

W1 24-pin, 0.3" wide 9-46
W2 28-pin, 0.3" wide 9-46
W3 20-pin, 0.3" wide 9-47
W4 16-pin, 0.3" wide 9-47
W5 18-pin, 0.3" wide 9-48
W6 32-pin, 0.4" wide 9-48

LOGIC Devices/MIL-STD-1835 Package Code Cross-Reference

LOGIC DEVICES PACKAGE CODE	DESCRIPTION	MIL-STD-1835 PACKAGE DESIGNATOR	MIL-STD-1835 DIMENSION REFERENCE
CERAMIC DIP			
C1	24-pin, 0.3" wide	GDIP3-T24	D-9
C2	20-pin, 0.3" wide	GDIP1-T20	D-8
C3	22-pin, 0.3" wide	N/A	N/A
C4	24-pin, 0.6" wide	GDIP1-T24	D-3
C5	28-pin, 0.3" wide	GDIP4-T28	D-15
C6	28-pin, 0.6" wide	GDIP1-T28	D-10
C7	16-pin, 0.3" wide	GDIP1-T16	D-2
C8	18-pin, 0.3" wide	GDIP1-T18	D-6
C9	32-pin, 0.6" wide	GDIP1-T32	D-16
C10	28-pin, 0.4" wide	N/A	N/A
C11	40-pin, 0.6" wide	GDIP1-T40	D-5
SIDEBRAZE, HERMETIC DIP			
D1	24-pin, 0.6" wide	CDIP2-T24	D-3
D2	24-pin, 0.3" wide	CDIP4-T24	D-9
D3	40-pin, 0.6" wide	CDIP2-T40	D-5
D4	64-pin, 0.9" wide, cavity up	CDIP1-T64	D-13
D5	48-pin, 0.6" wide	CDIP2-T48	D-14
D6	64-pin, 0.9" wide, cavity down	CDIP1-T64	D-13
D7	20-pin, 0.3" wide	CDIP2-T20	D-8
D8	22-pin, 0.3" wide	N/A	N/A
D9	28-pin, 0.6" wide	CDIP2-T28	D-10
D10	28-pin, 0.3" wide	CDIP3-T28	D-15
D11	28-pin, 0.4" wide	N/A	N/A
CERAMIC PGA			
G1	68-pin, cavity up	CMGA3-P68	P-AC
G2	68-pin, cavity down	CMGA3-P68	P-AC
G3	84-pin	CMGA15-P84	P-BC
G4	120-pin	CMGA3-P121	P-AC
CERAMIC LEADLESS CHIP CARRIER			
K1	28-pin, 0.450" x 0.450"	CQCC1-N28	C-4
K2	44-pin, 0.650" x 0.650"	CQCC1-N44	C-5
K3	68-pin, 0.950" x 0.950"	CQCC1-N68	C-7
K4	22-pin, 0.290" x 0.490"	N/A	N/A
K5	28-pin, 0.350" x 0.550"	CQCC4-N28	C-11A
K6	20-pin, 0.290" x 0.425"	CQCC3-N20	C-13
K7	32-pin, 0.450" x 0.550"	CQCC1-N32	C-12
K8	20-pin, 0.350" x 0.350"	CQCC1-N20	C-2
K9	48-pin, 0.550" x 0.550"	N/A	N/A
CERAMIC FLATPACK			
M1	24-pin	GDFP2-F24	F-6
M2	28-pin	GDFP2-F28	F-11

Thermal Considerations

The temperature at which a semiconductor device operates is one of the primary determinants of its reliability. This temperature is often referred to as the "junction temperature", although this term is more appropriate for bipolar than MOS technologies. Heat dissipated in the device during operation escapes through a path consisting of one or more series thermal impedances terminating in the surrounding air (see Figure. 1).

The presence of this nonzero thermal impedance causes the temperature of the device to rise above that of the air. Each of the components of the overall thermal impedance causes a rise in temperature which is linearly dependent on the power dissipated in the device. The coefficient is called θ, and has the units °C/W. The θ value for each thermal impedance represents the amount of temperature rise across the impedance as a function of the power dissipation. Usually, θ is given a subscript indicating the two points between which the impedance is measured. Thus the junction temperature of an operating device is given by:

$$T_j = T_{AMB} + (Pd \bullet \theta_{JA})$$

where:

T_j = junction temperature of the device, °C,

T_{AMB} = ambient air temperature, in°C

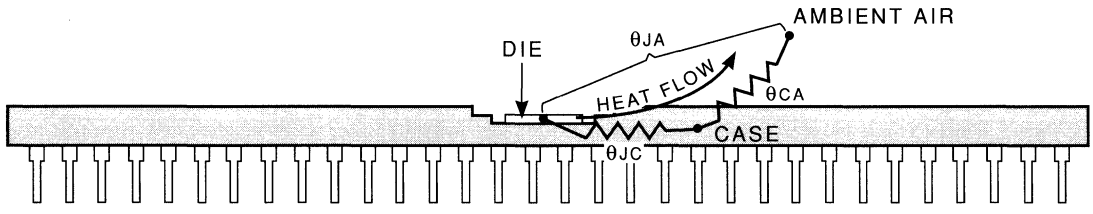
Pd = power dissipation of the device, in W,

θ_{JA} = sum of all thermal impedances between the die and the ambient air, in °C/W.

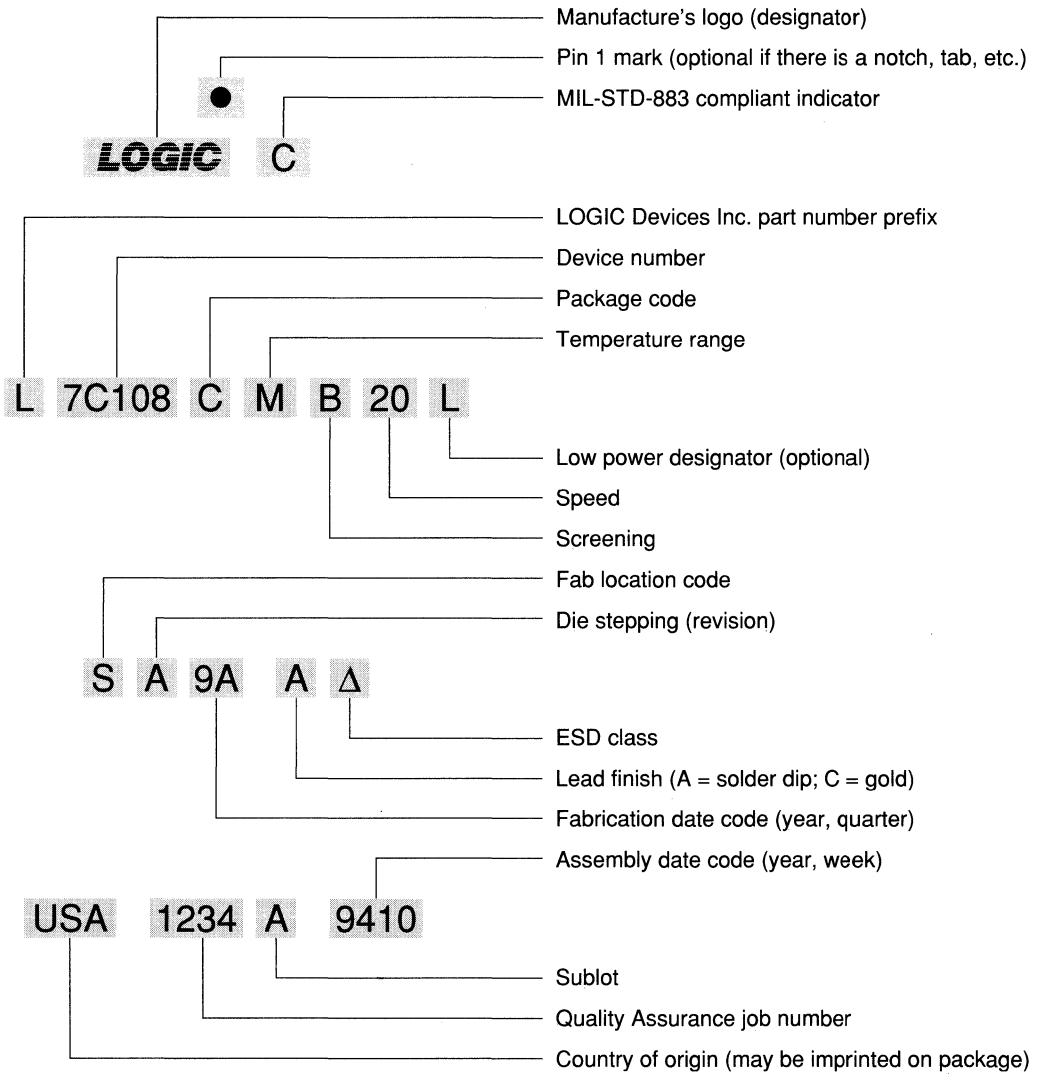
The thermal impedance of a given device is dependent on several factors. The package type is the predominant effect; ceramic packages have much lower thermal impedances than plastic, and packages with large surface areas tend to dissipate heat faster. Another factor which is beyond the control of the device manufacturer but which is nonetheless important is the temperature and flow rate of the cooling air. Secondary effects include the size of the die, the method of attaching the die to the package, and the organization of high power dissipation elements on the die.

Because all LOGIC Devices products are built with low-power CMOS technology, thermal impedance is less of a concern than it would be for higher power technologies. As an example, consider a typical NMOS multiplier similar to the LMU16, packaged in a 64-pin plastic DIP. Assuming 1 W power dissipation and θ_{JA} of 50°C/W, the actual die temperature would be 50°C above the surrounding air. By contrast, the LOGIC Devices LMU16 has a typical power dissipation of only 60 mW. This device in the same package would operate at only 3° above the ambient air temperature. Since operating temperature has an exponential relationship to device failure rate (see Quality and Reliability Manuals), the reduction of die temperature available with LOGIC Devices low-power CMOS translates to a marked increase in expected reliability.

FIGURE 1.



Package Marking Guide



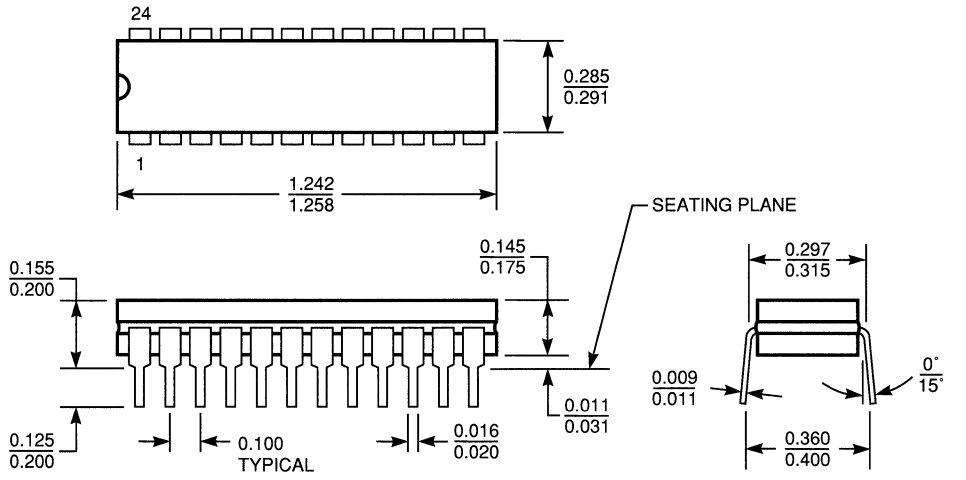
NOTE: Package marking may occur on top and bottom of package due to space limitations

Mechanical Drawings

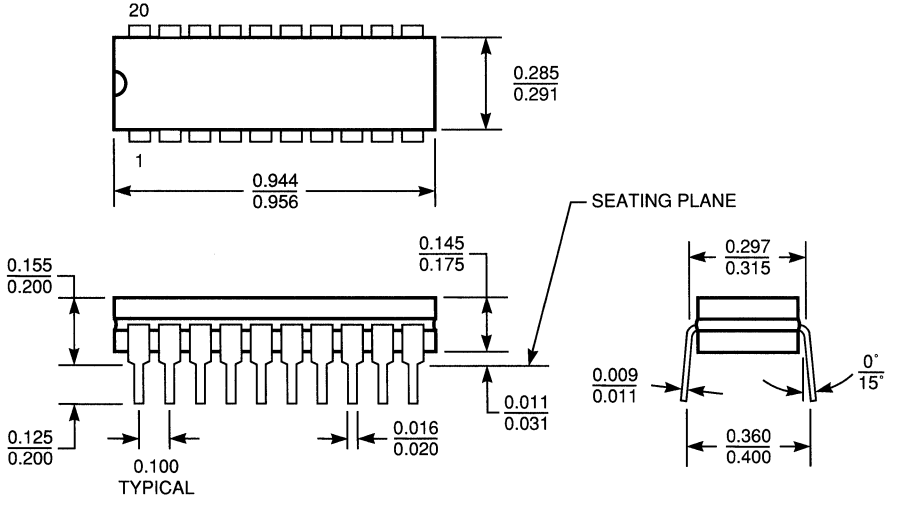
- Ceramic Dual In-line Package
- Sidebraze, Hermetic Dual In-line Package
- Commercial Pin Grid Array
- Ceramic Pin Grid Array
- Plastic J-Lead Chip Carrier
- Ceramic Leadless Chip Carrier
- Ceramic Flatpack
- Plastic Dual In-line Package
- Plastic Quad Flatpack
- Plastic Small Outline J-Lead

CERAMIC DIP (ORDERING CODE: C, I)

C1 — 24-pin, 0.3" wide

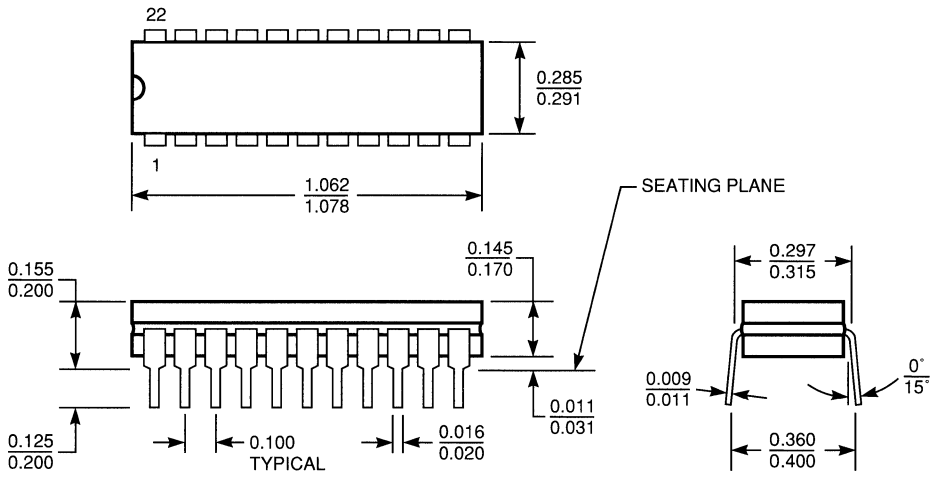


C2 — 20-pin, 0.3" wide

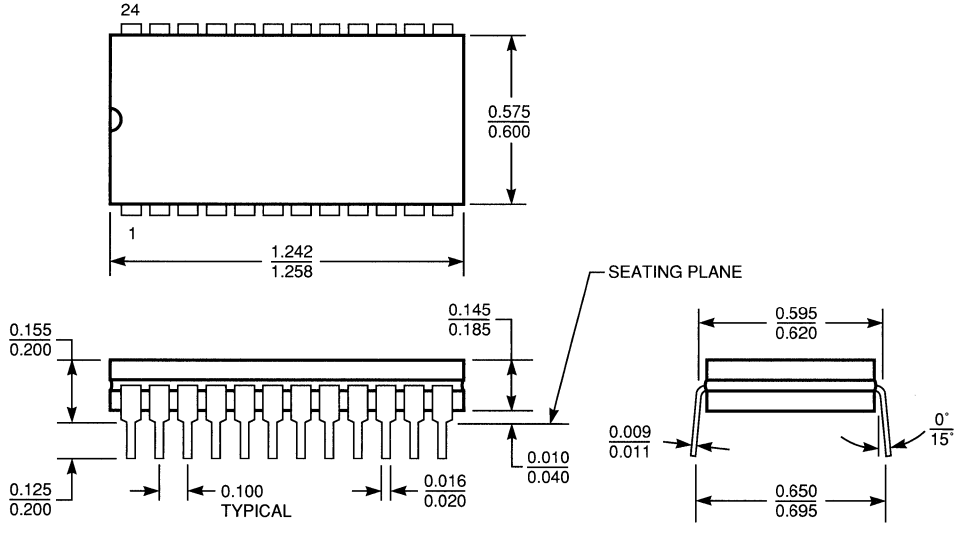


CERAMIC DIP (ORDERING CODE: C, I)

C3 — 22-pin, 0.3" wide



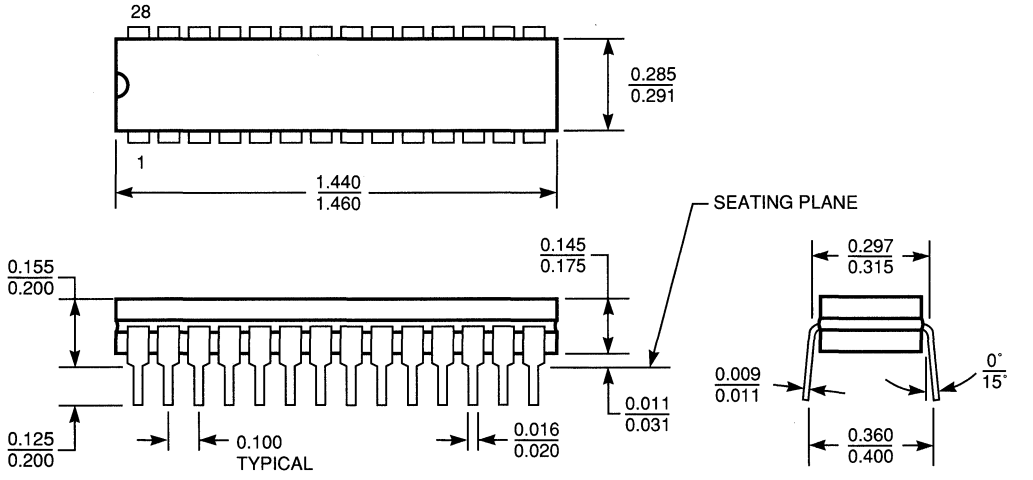
C4 — 24-pin, 0.6" wide



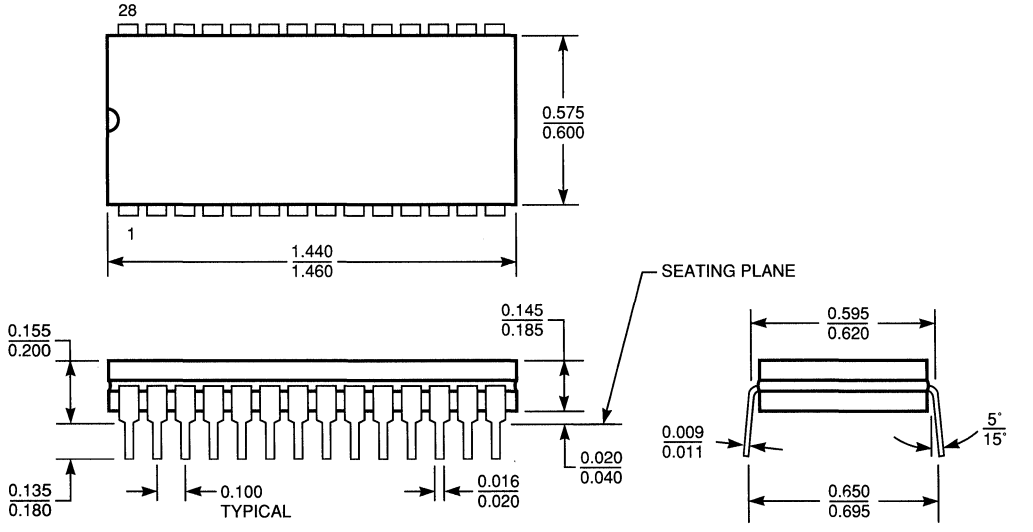
9

CERAMIC DIP (ORDERING CODE: C, I)

C5 — 28-pin, 0.3" wide

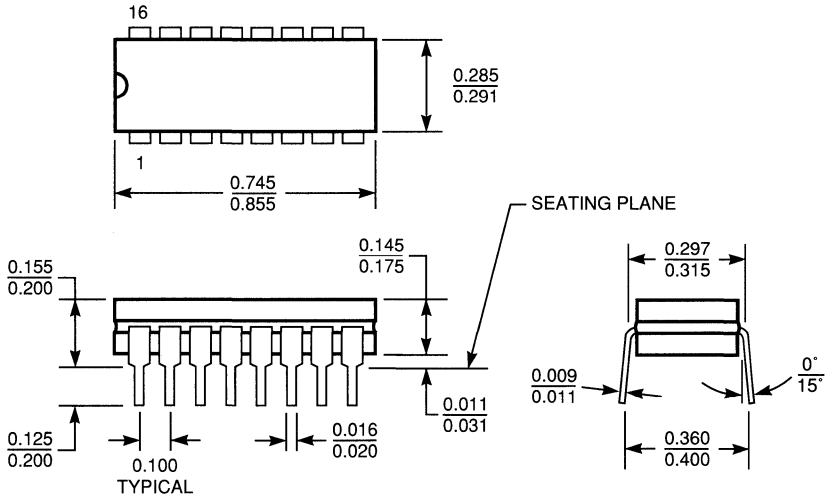


C6 — 28-pin, 0.6" wide

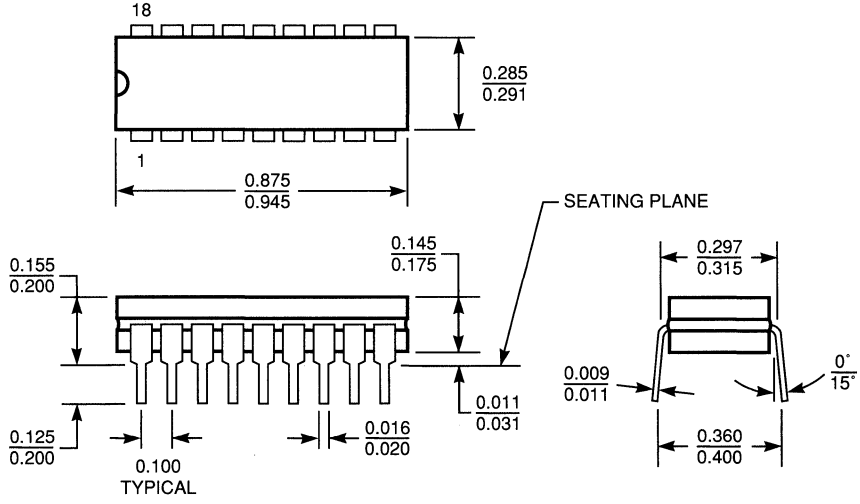


CERAMIC DIP (ORDERING CODE: C, I)

C7 — 16-pin, 0.3" wide



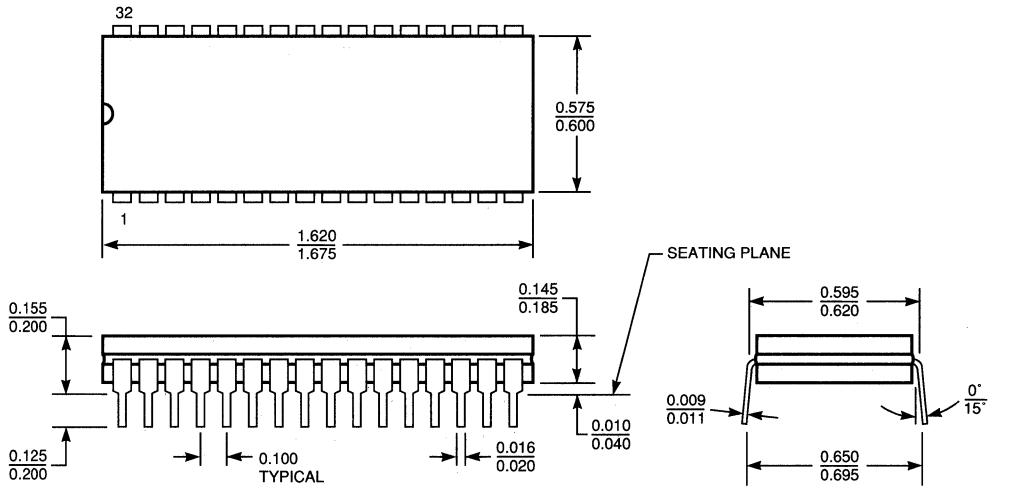
C8 — 18-pin, 0.3" wide



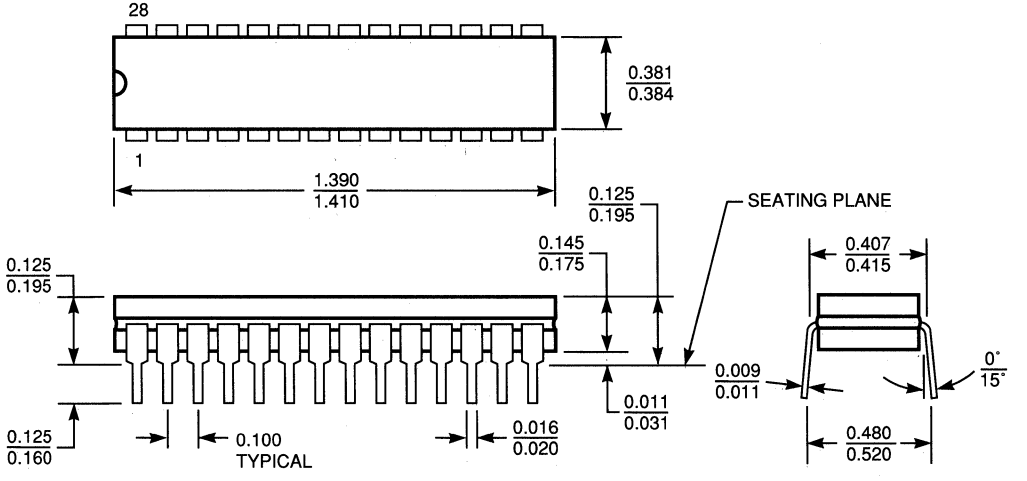
9

CERAMIC DIP (ORDERING CODE: C, I)

C9 — 32-pin, 0.6" wide

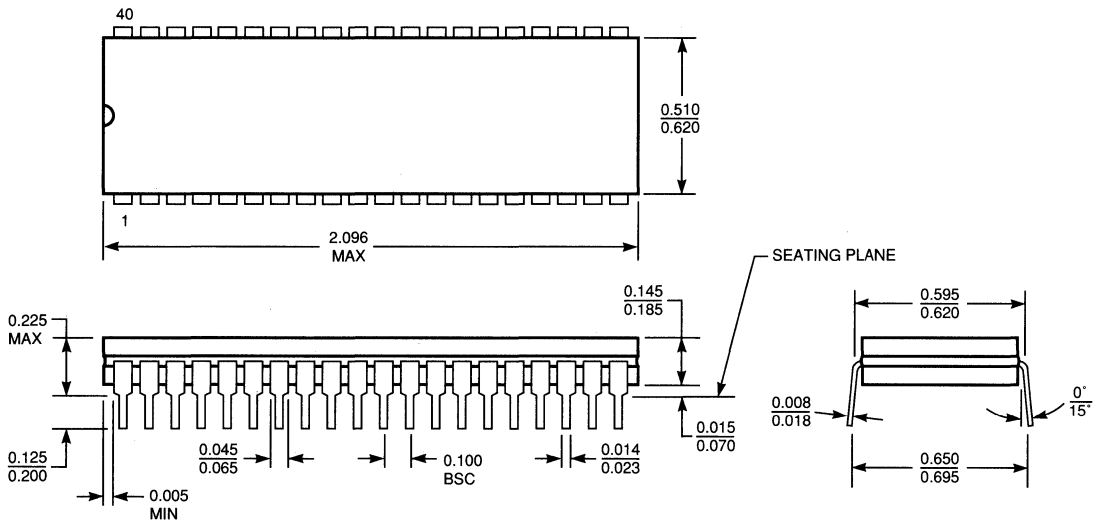


C10 — 28-pin, 0.4" wide



Ceramic DIP (Ordering Code: C, I)

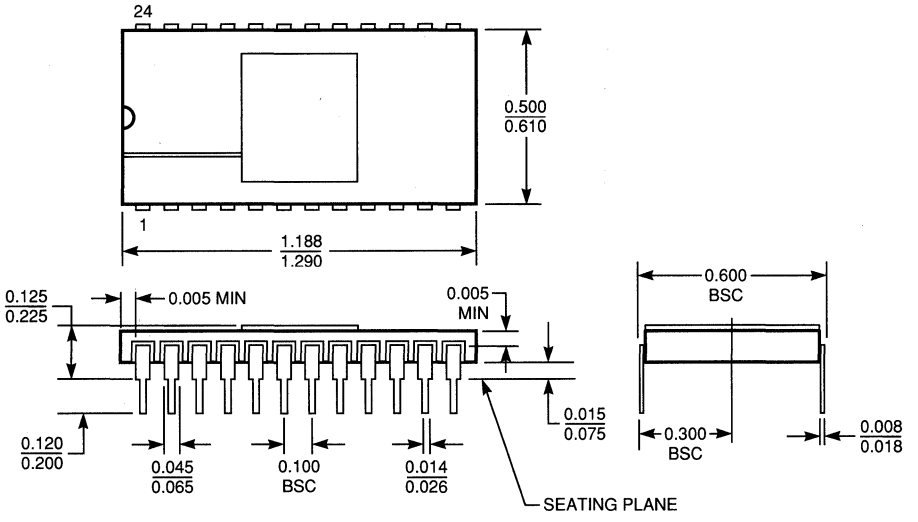
C11 — 40-pin, 0.6" wide



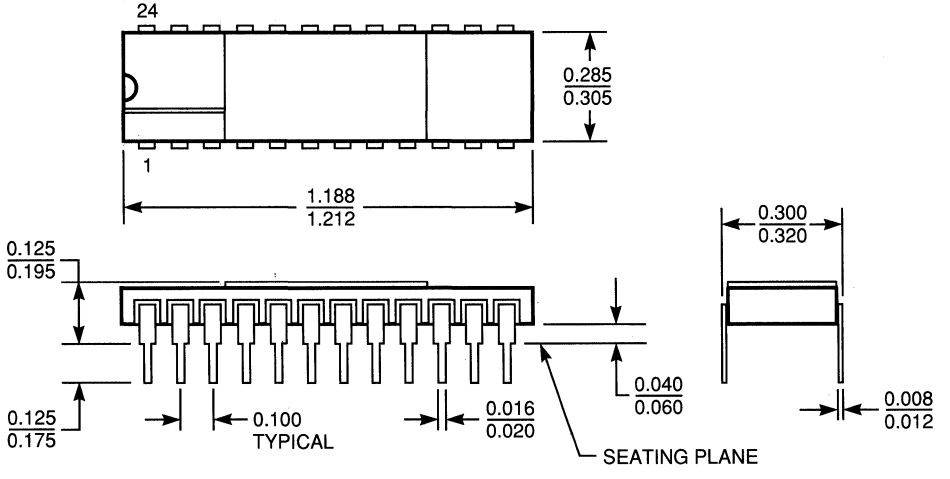
9

SIDEBRAZE, HERMETIC DIP (ORDERING CODE: D, H)

D1 — 24-pin, 0.6" wide

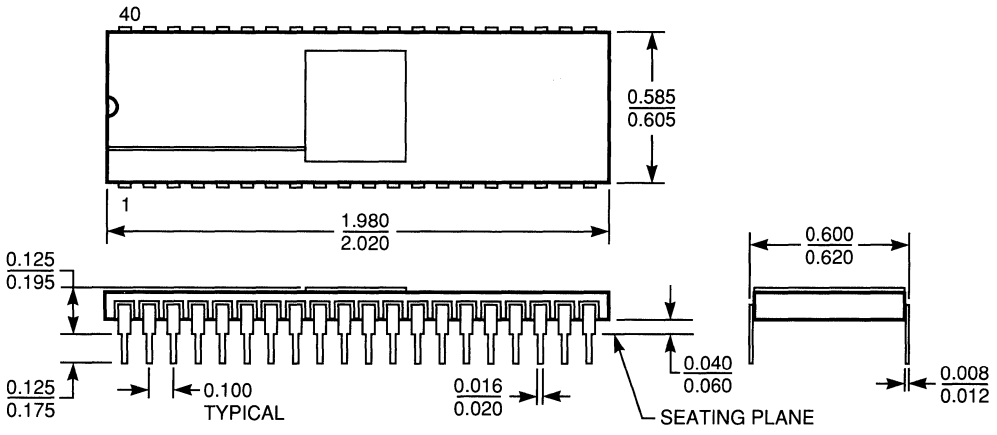


D2 — 24-pin, 0.3" wide

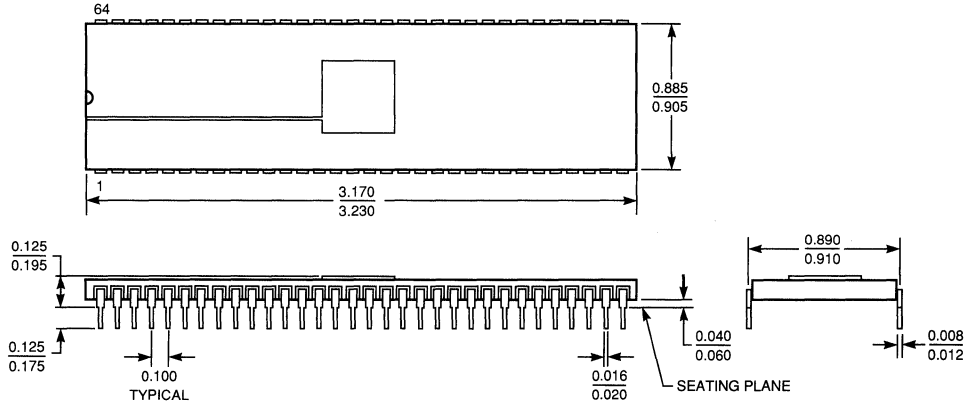


SIDEBRAZE, HERMETIC DIP (ORDERING CODE: D, H)

D3 — 40-pin, 0.6" wide



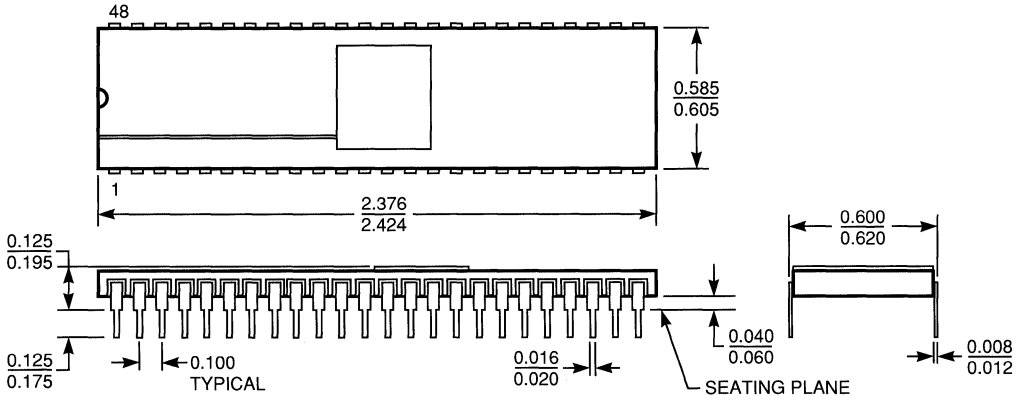
D4 — 64-pin, 0.9" wide, cavity up



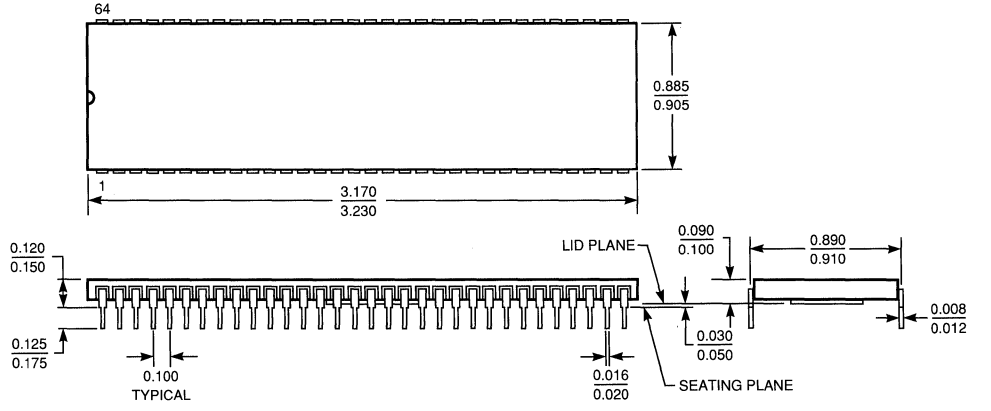
9

SIDEBRAZE, HERMETIC DIP (ORDERING CODE: D, H)

D5 — 48-pin, 0.6" wide

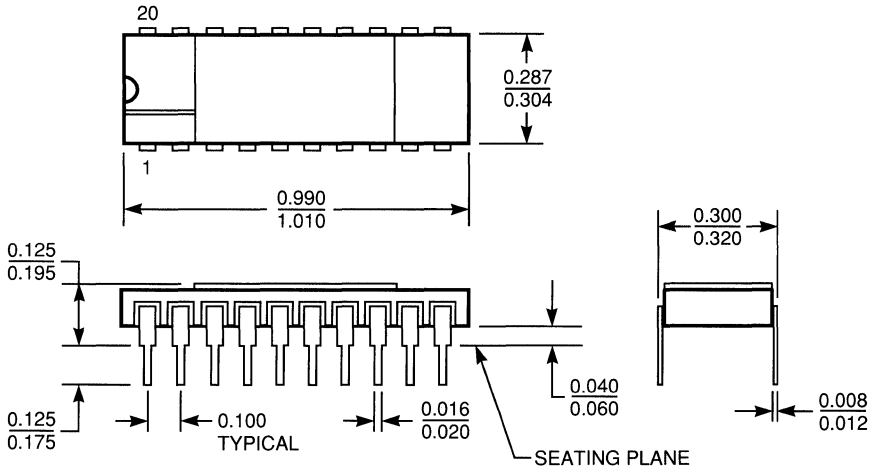


D6 — 64-pin, 0.9" wide, cavity down

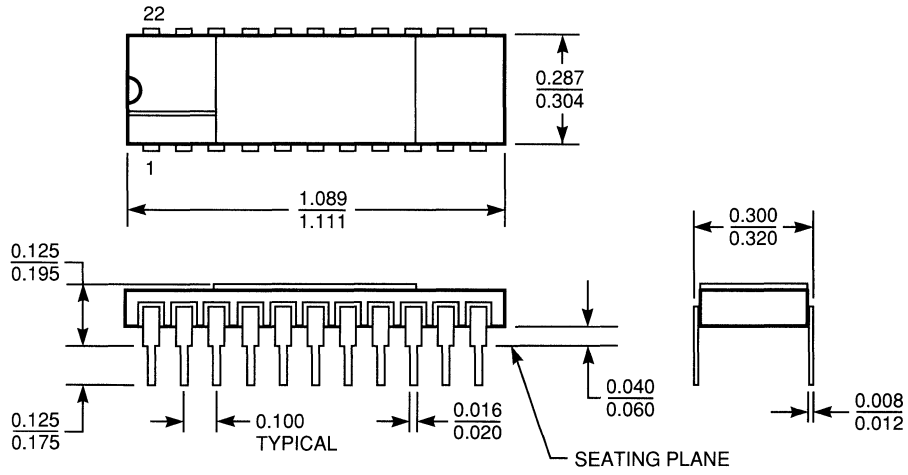


SIDEBRAZE, HERMETIC DIP (ORDERING CODE: D, H)

D7 — 20-pin, 0.3" wide



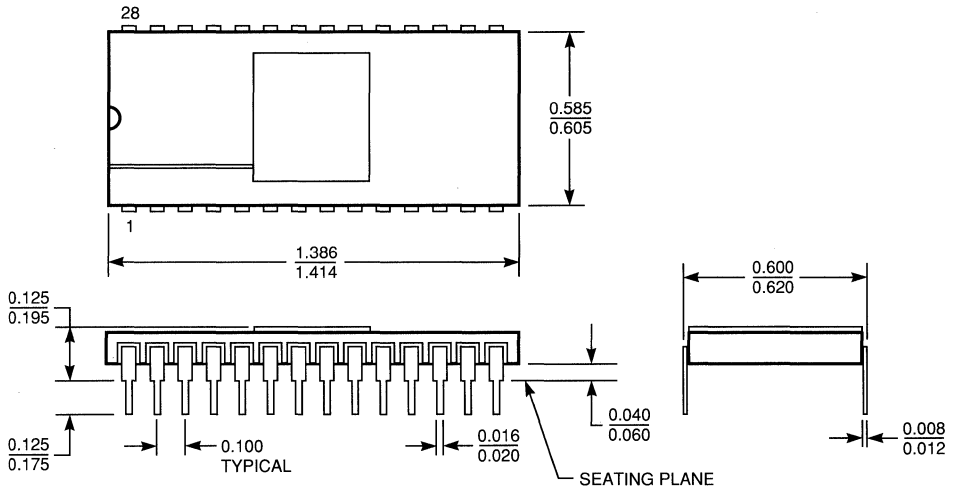
D8 — 22-pin, 0.3" wide



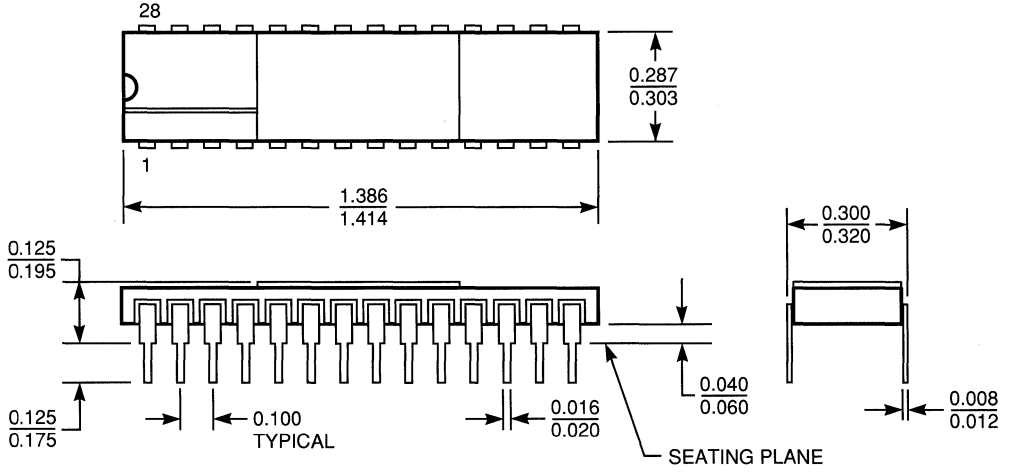
9

SIDEBRAZE, HERMETIC DIP (ORDERING CODE: D, H)

D9 — 28-pin, 0.6" wide

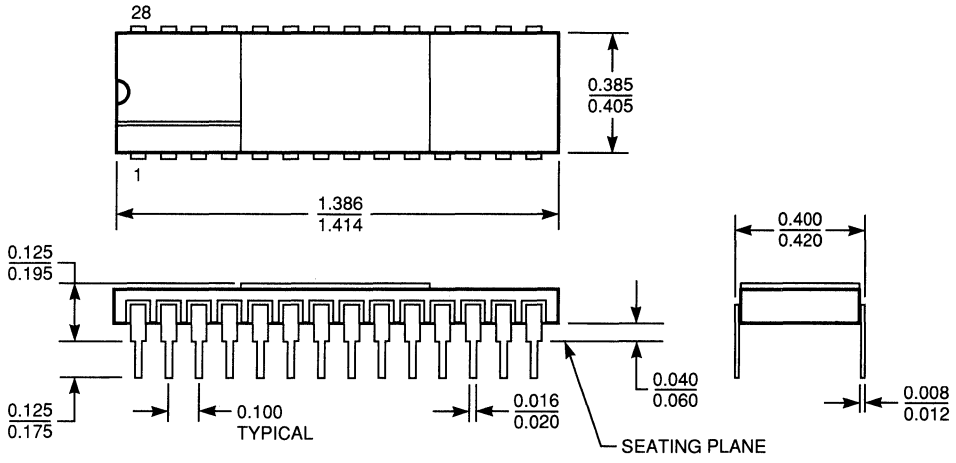


D10 — 28-pin, 0.3" wide



SIDEBRAZE, HERMETIC DIP (ORDERING CODE: D, H)

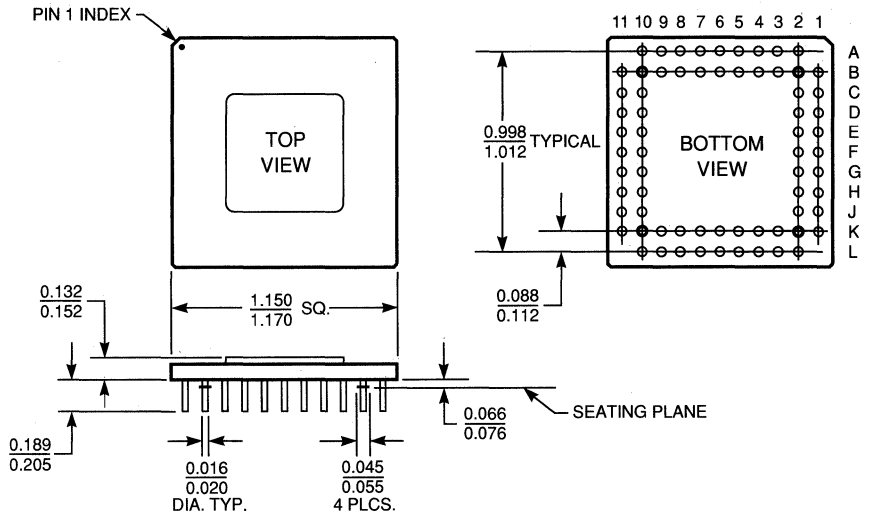
D11 — 28-pin, 0.4" wide



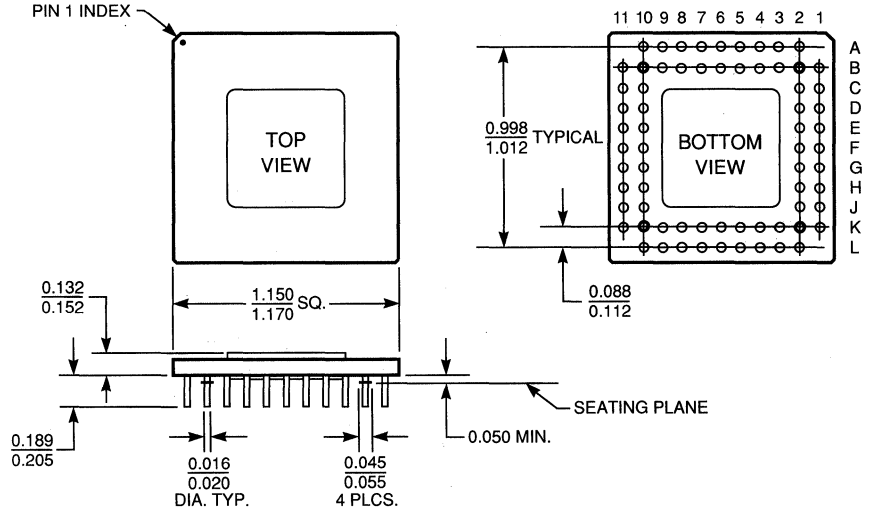
9

COMMERCIAL PGA (ORDERING CODE: E)

E1 — 68-pin, cavity up

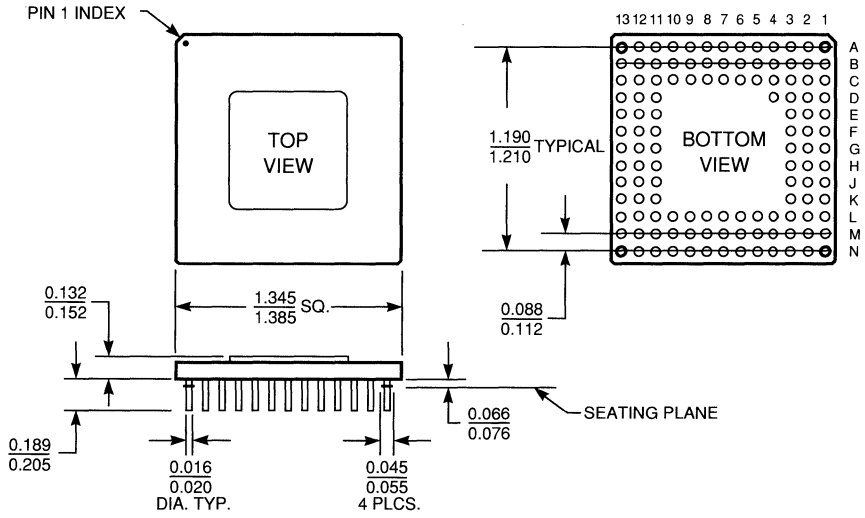


E2 — 68-pin, cavity down



Commercial PGA (Ordering Code: E)

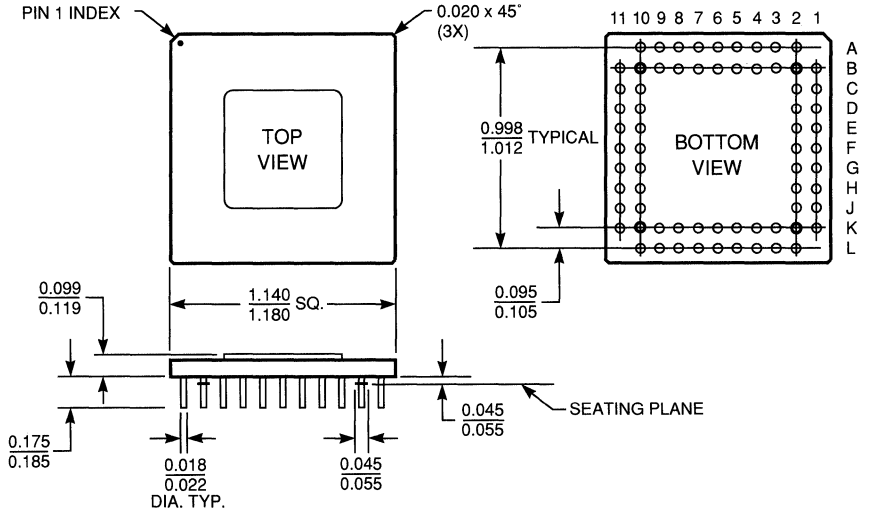
E3 — 120-pin



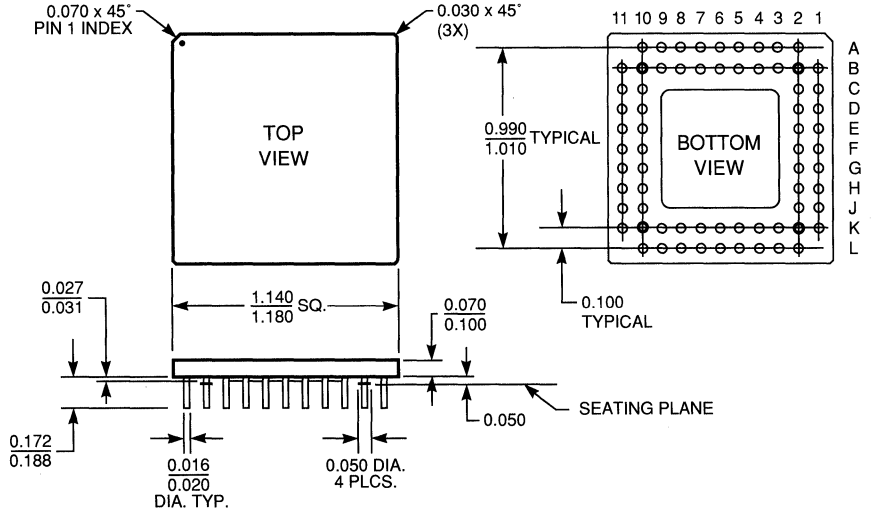
9

Ceramic PGA (Ordering Code: G)

G1 — 68-pin, cavity up

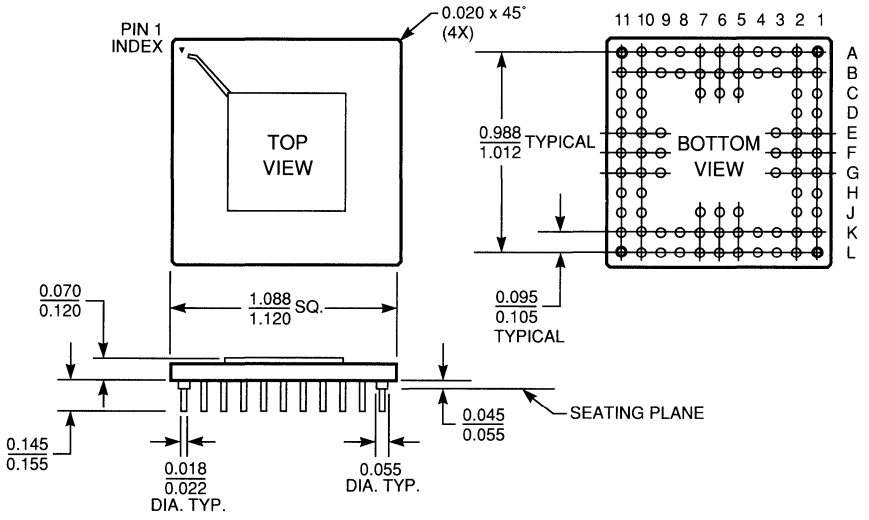


G2 — 68-pin, cavity down

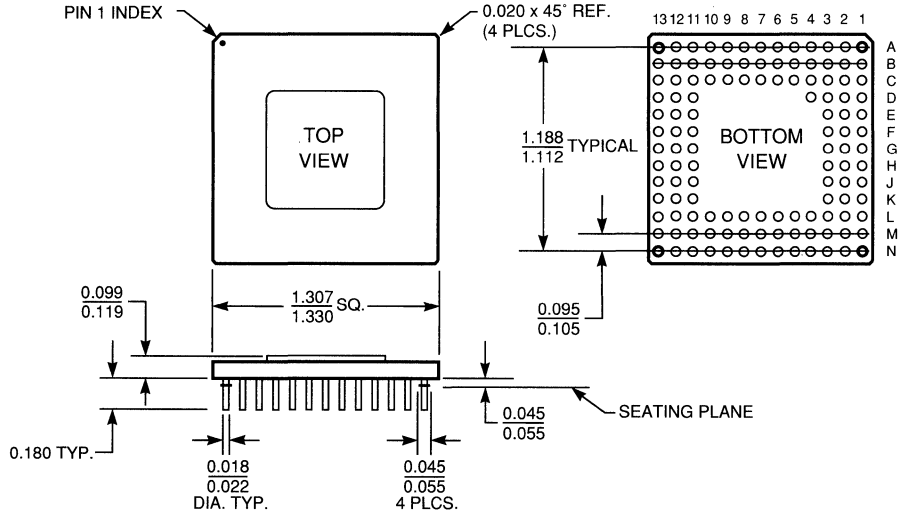


Ceramic PGA (Ordering Code: G)

G3 — 84-pin



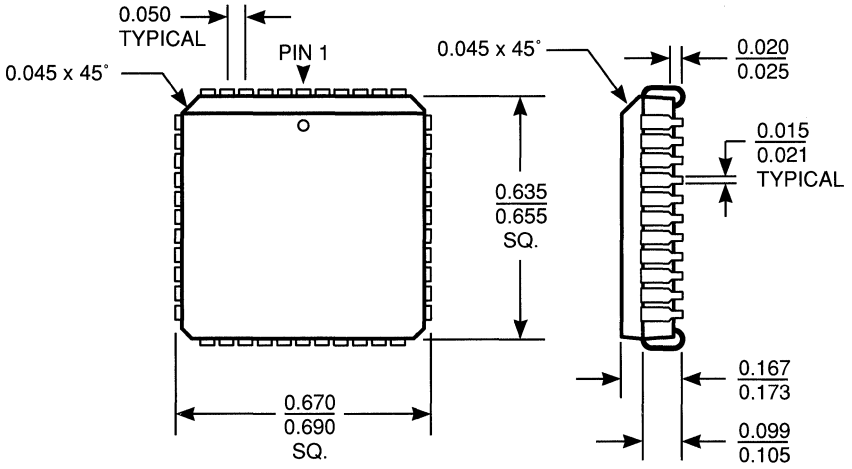
G4 — 120-pin



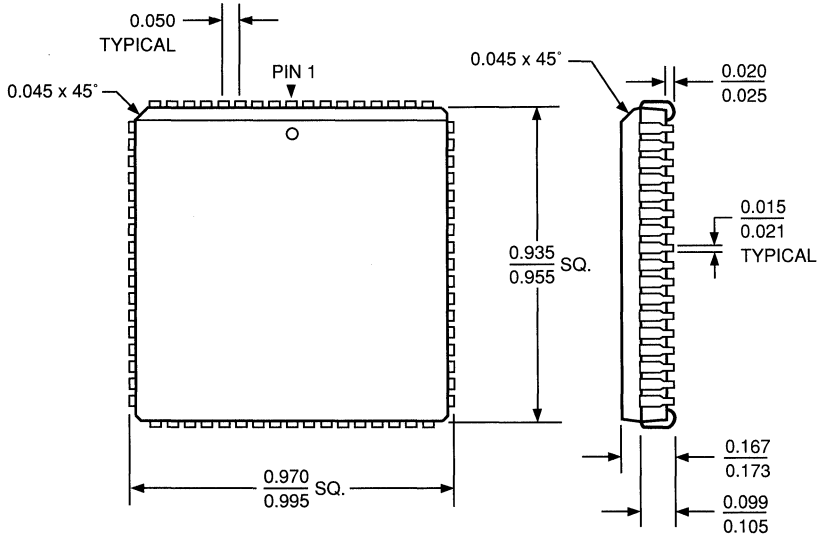
9

Plastic J-Lead Chip Carrier (Ordering Code: J)

J1 — 44-pin, 0.690" x 0.690"

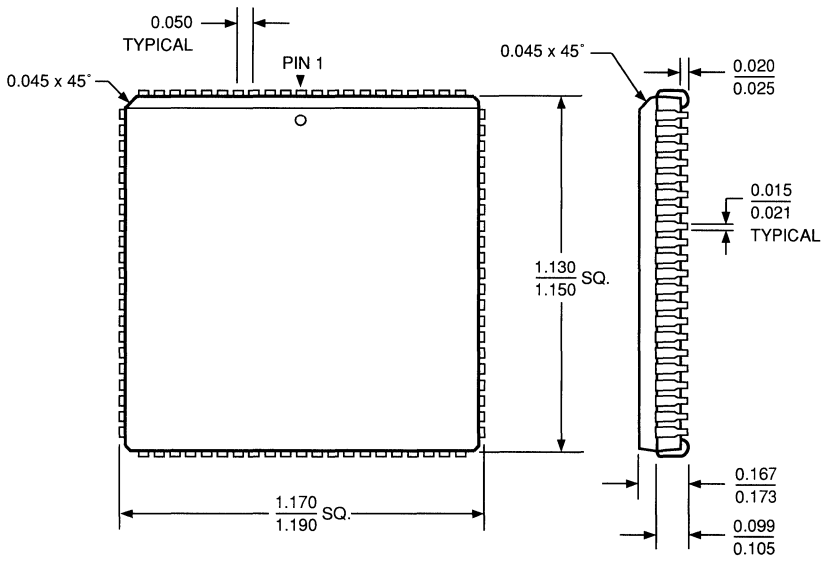


J2 — 68-pin, 0.990" x 0.990"

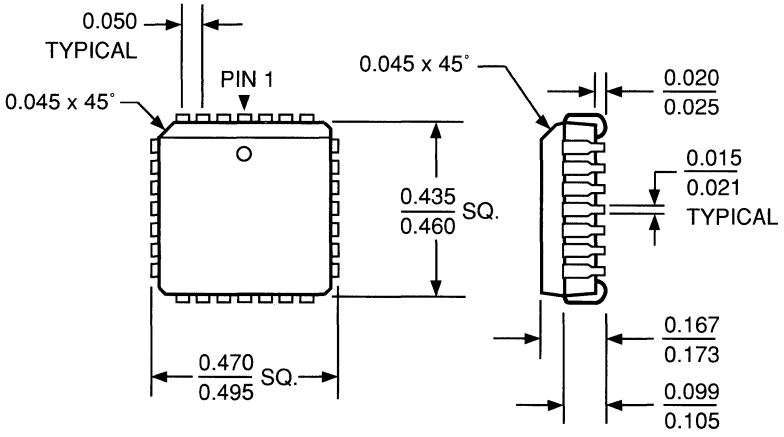


Plastic J-Lead Chip Carrier (Ordering Code: J)

J3 — 84-pin, 1.190" x 1.190"



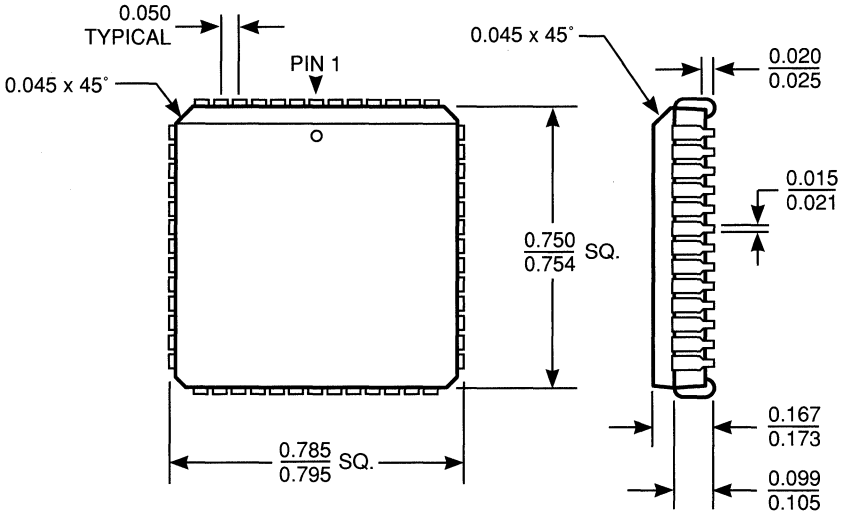
J4 — 28-pin, 0.490" x 0.490"



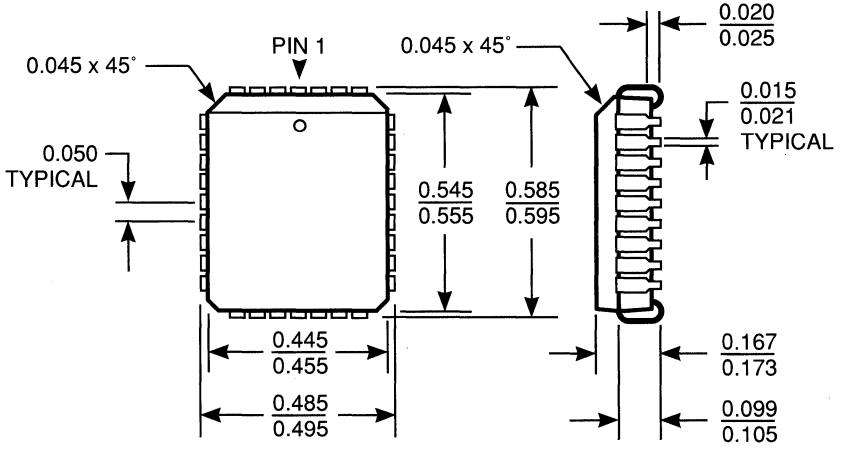
9

Plastic J-Lead Chip Carrier (Ordering Code: J)

J5 — 52-pin, 0.790" x 0.790"

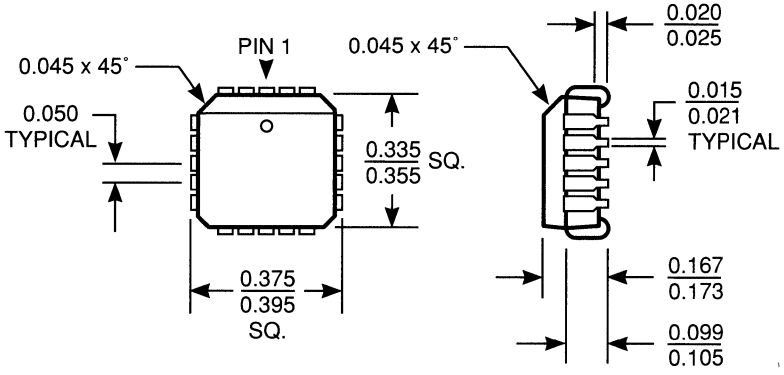


J6 — 32-pin, 0.490" x 0.590"



Plastic J-Lead Chip Carrier (Ordering Code: J)

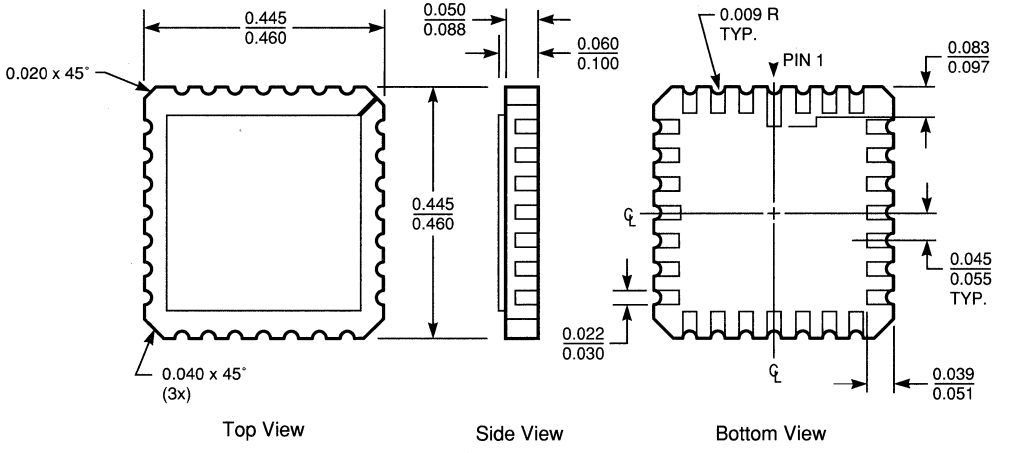
J7 — 20-pin, 0.390" x 0.390"



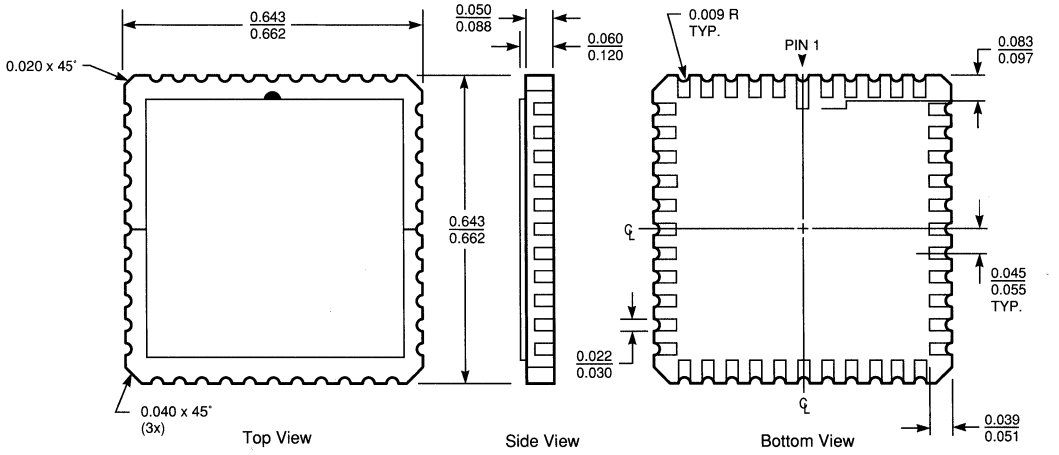
9

Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K1 — 28-pin, 0.450" x 0.450"

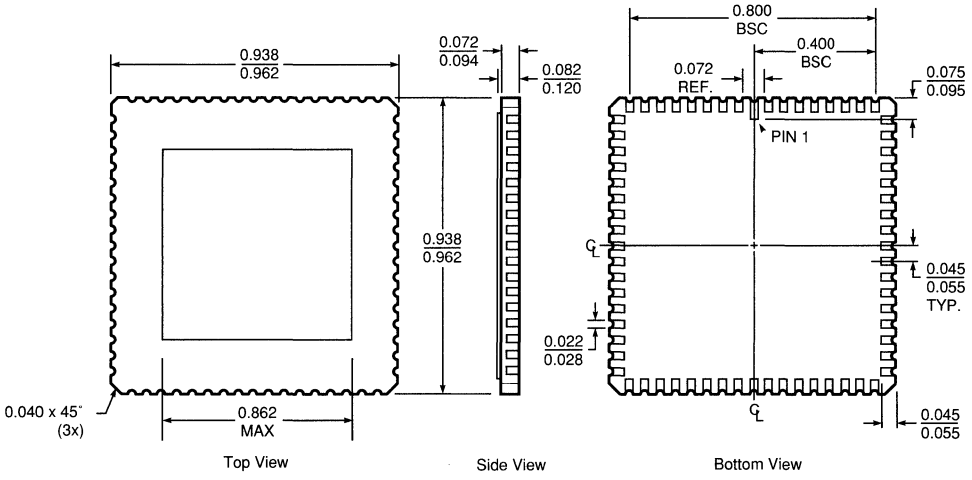


K2 — 44-pin, 0.650" x 0.650"

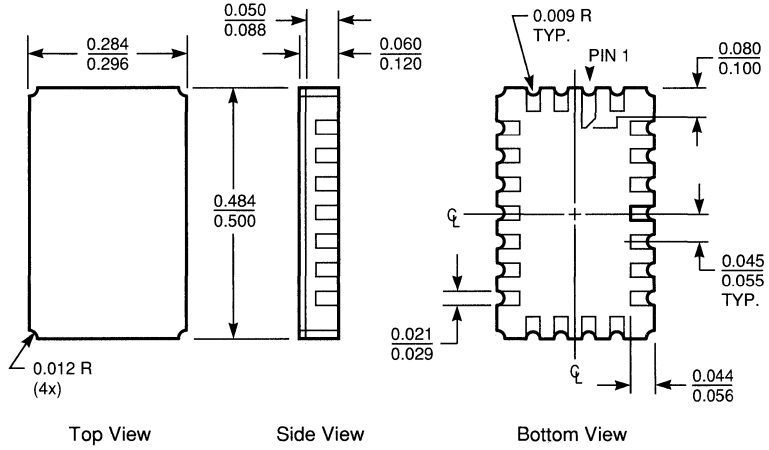


Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K3 — 68-pin, 0.950" x 0.950"



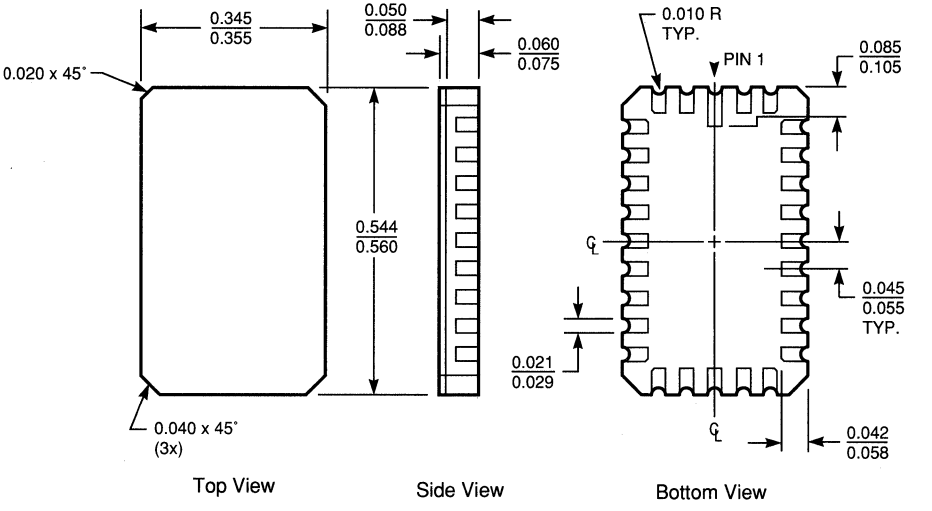
K4 — 22-pin, 0.290" x 0.490"



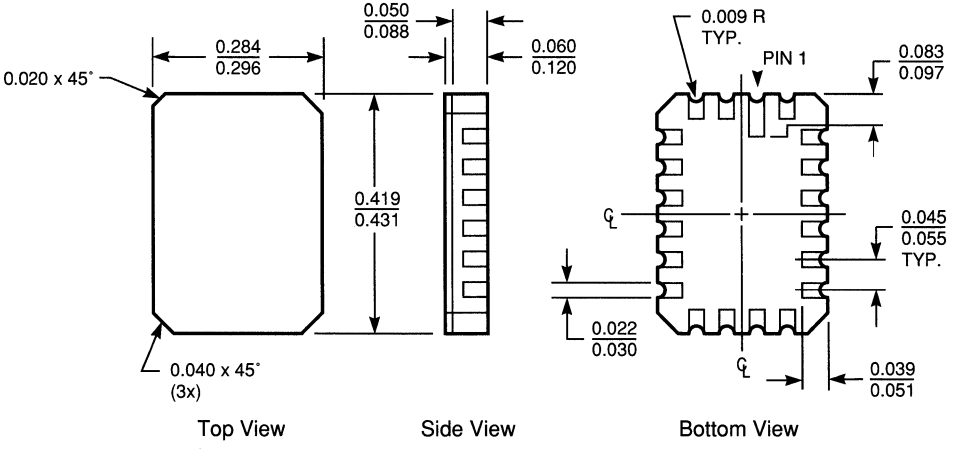
9

Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K5 — 28-pin, 0.350" x 0.550"

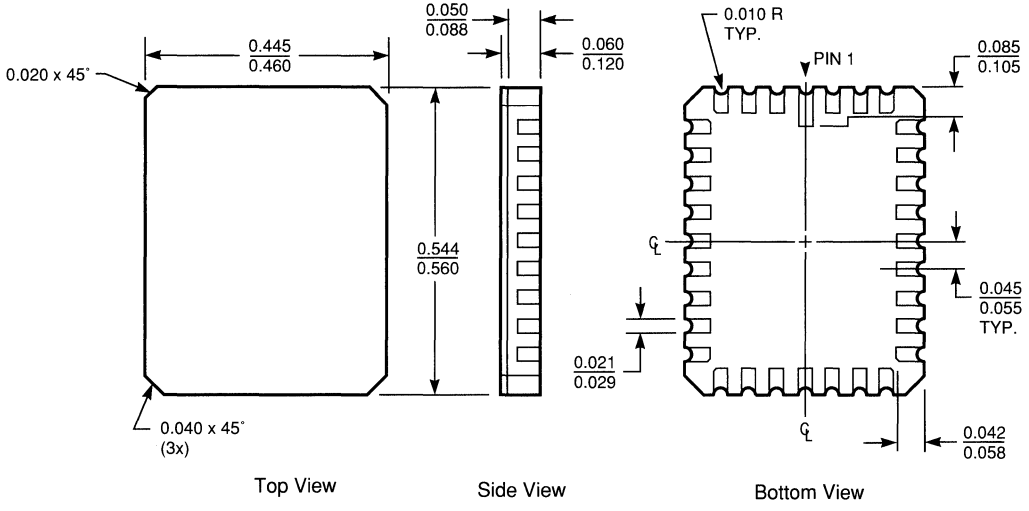


K6 — 20-pin, 0.290" x 0.425"

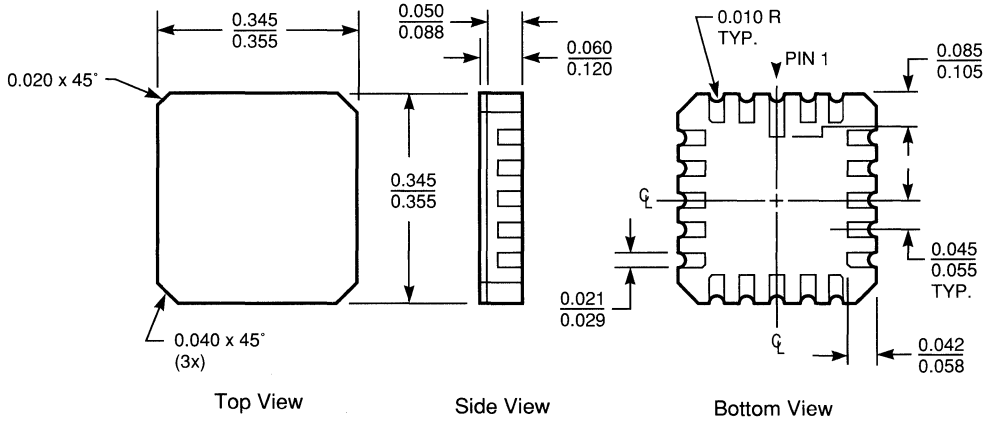


Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K7 — 32-pin, 0.450" x 0.550"



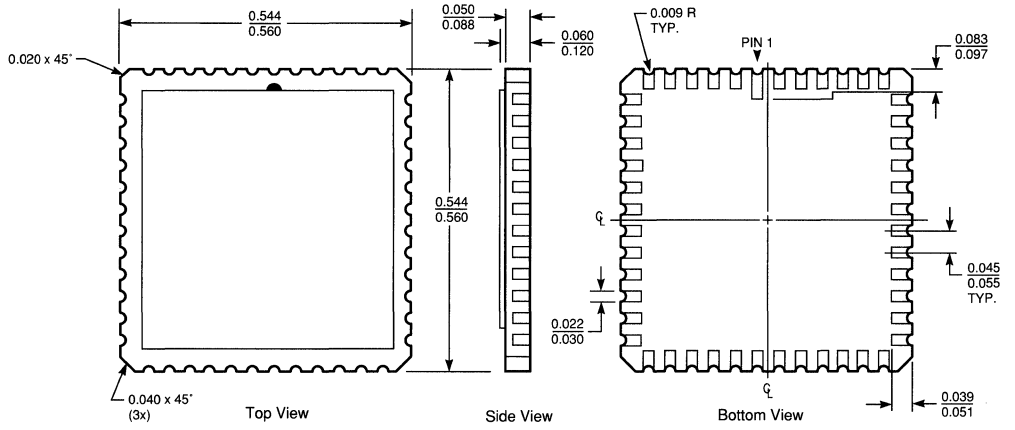
K8 — 20-pin, 0.350" x 0.350"



9

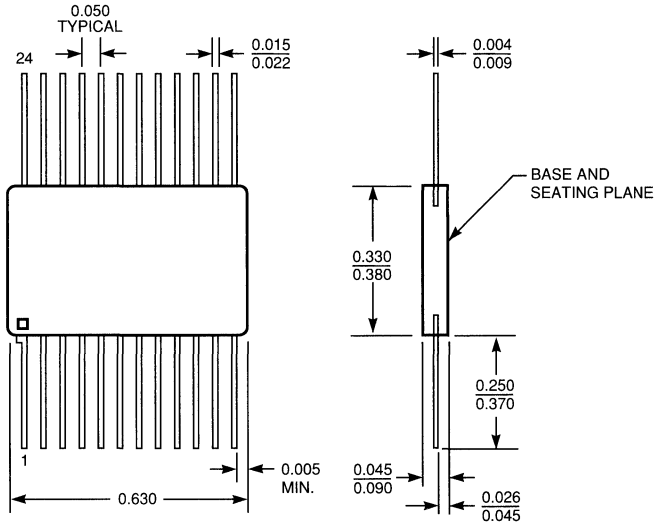
Ceramic Leadless Chip Carrier (Ordering Code: K, T)

K9 — 48-pin, 0.550" x 0.550"

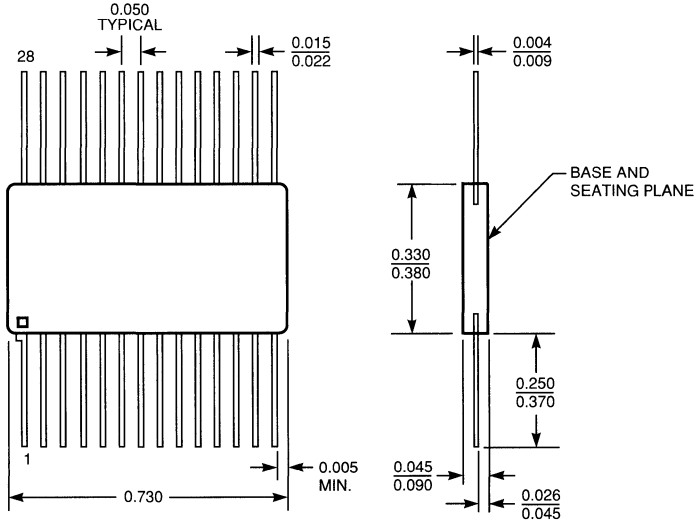


Ceramic Flatpack (Ordering Code: M)

M1 — 24-pin

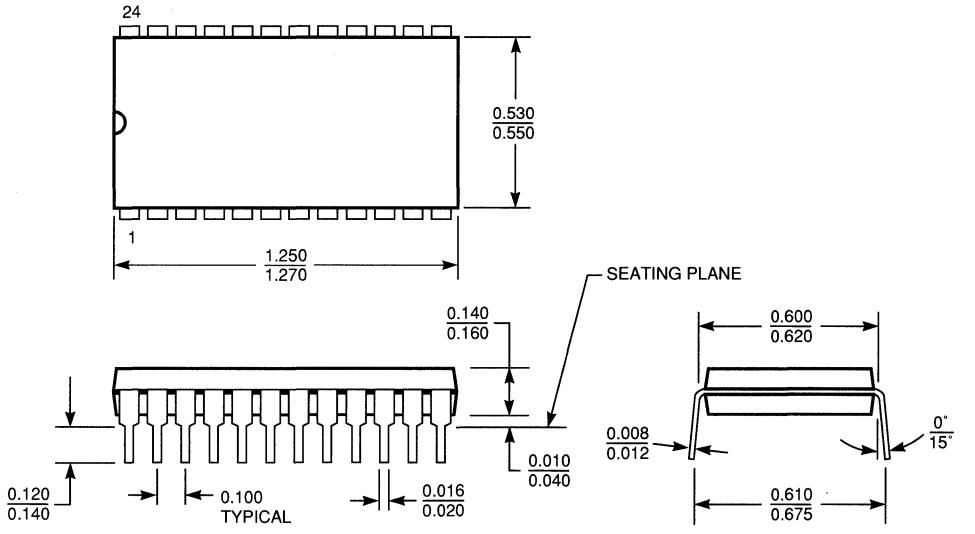


M2 — 28-pin

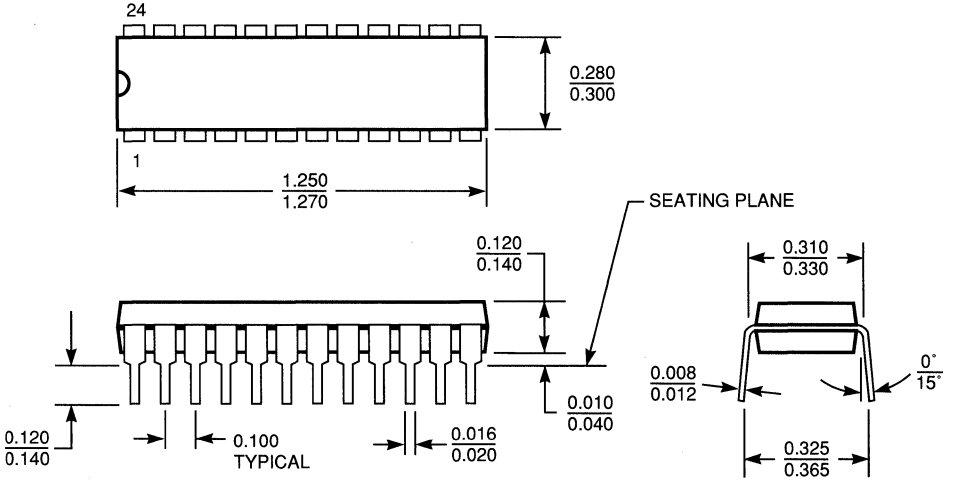


PLASTIC DIP (ORDERING CODE: P, N)

P1 — 24-pin, 0.6" wide

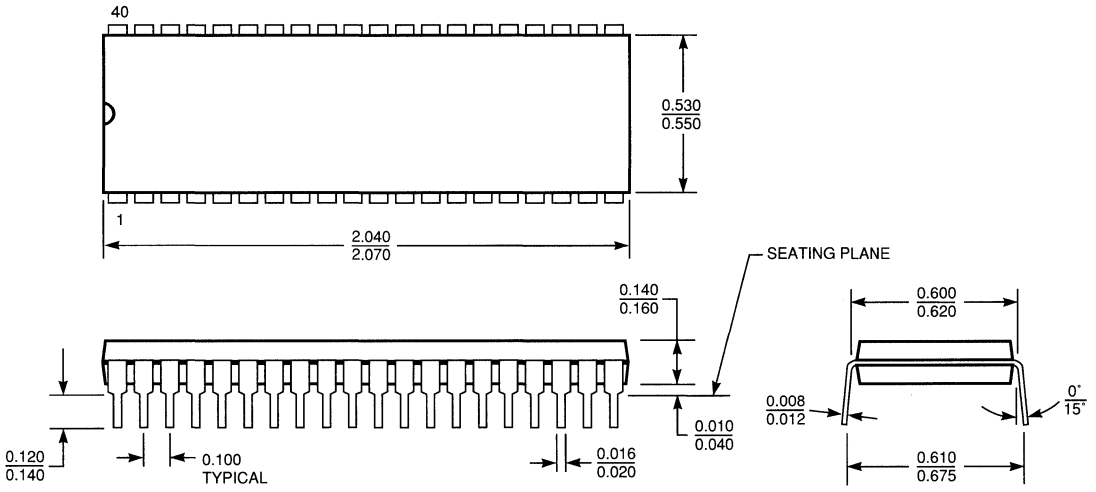


P2 — 24-pin, 0.3" wide

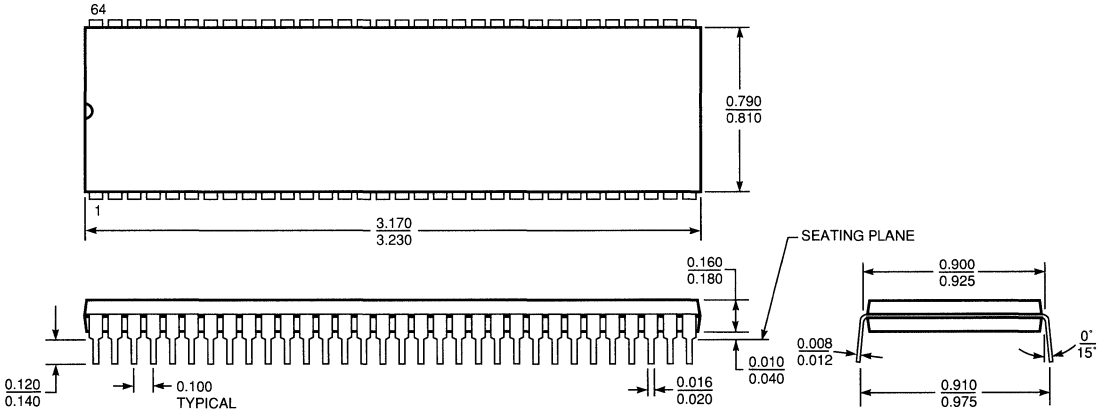


PLASTIC DIP (ORDERING CODE: P, N)

P3 — 40-pin, 0.6" wide



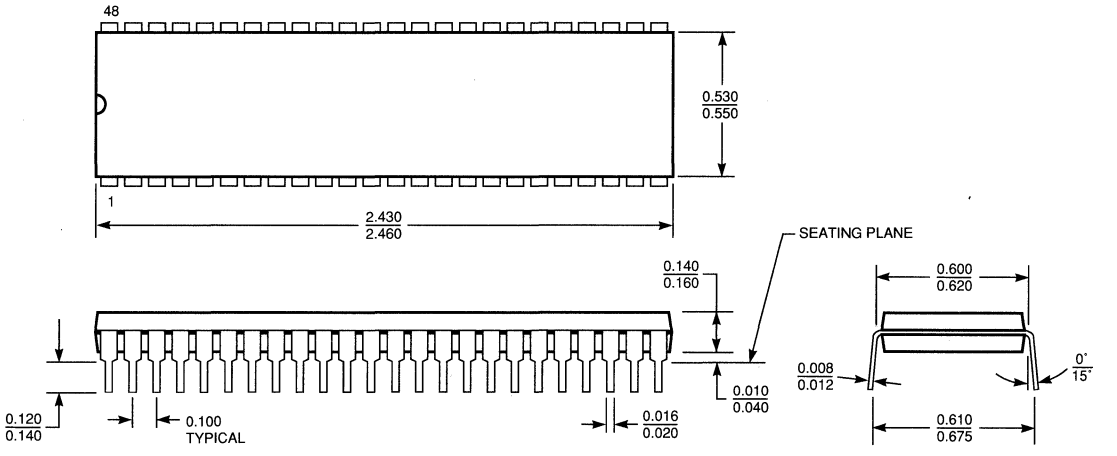
P4 — 64-pin, 0.9" wide



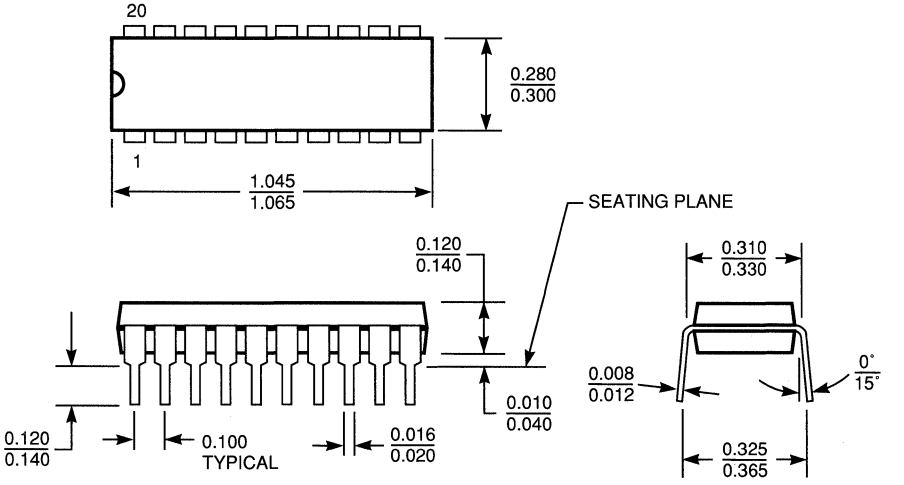
9

Plastic DIP (Ordering Code: P, N)

P5 — 48-pin, 0.6" wide

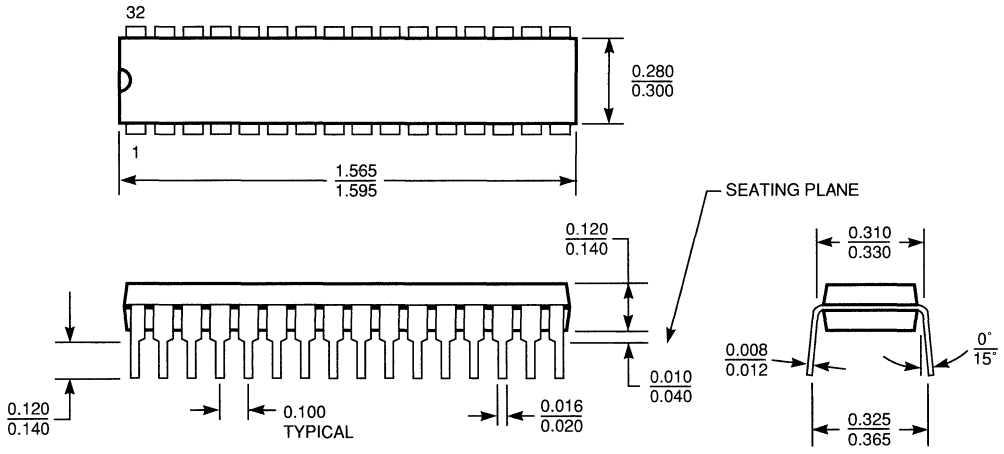


P6 — 20-pin, 0.3" wide

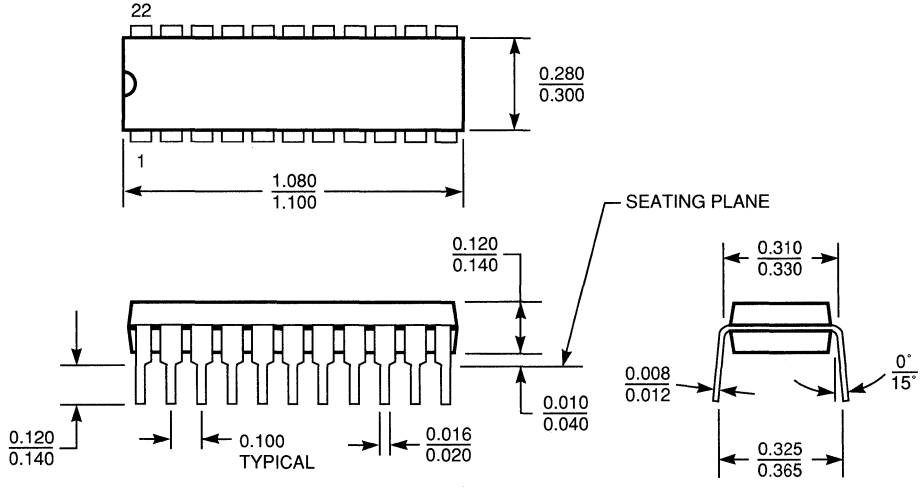


Plastic DIP (Ordering Code: P, N)

P7 — 32-pin, 0.3" wide



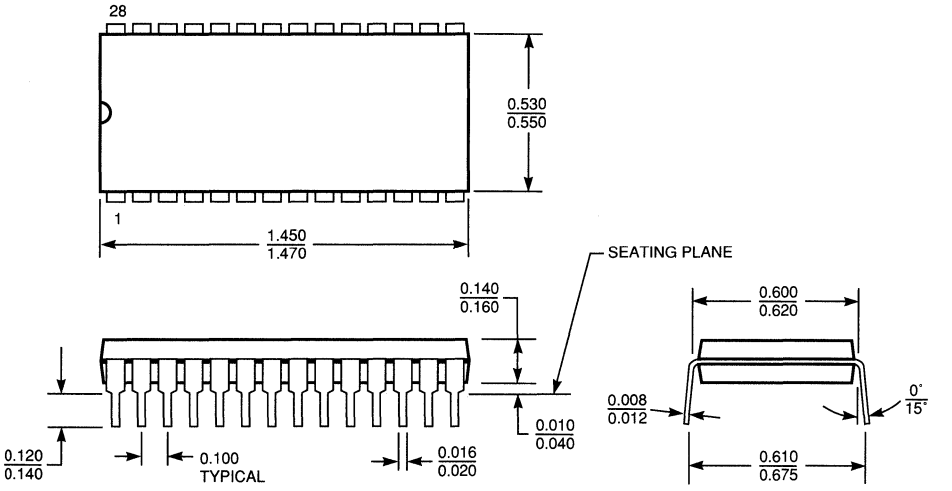
P8 — 22-pin, 0.3" wide



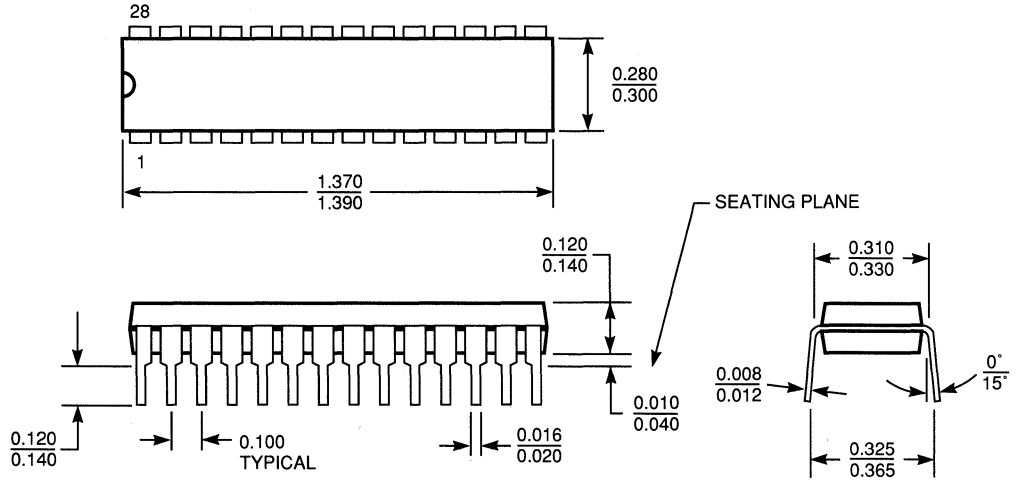
9

PLASTIC DIP (ORDERING CODE: P, N)

P9 — 28-pin, 0.6" wide

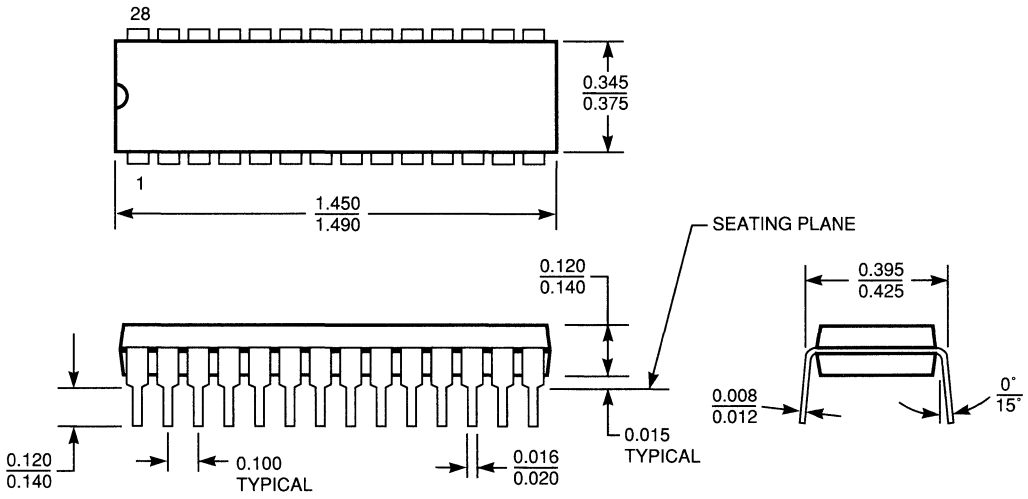


P10 — 28-pin, 0.3" wide

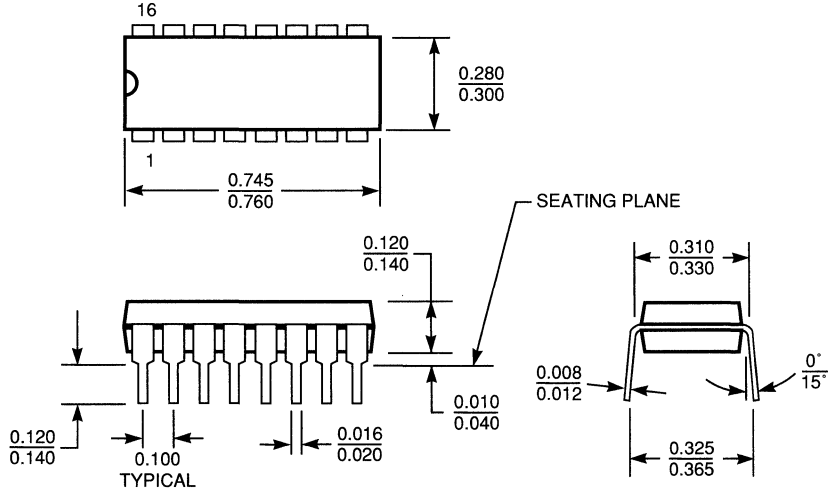


Plastic DIP (Ordering Code: P, N)

P11 — 28-pin, 0.4" wide



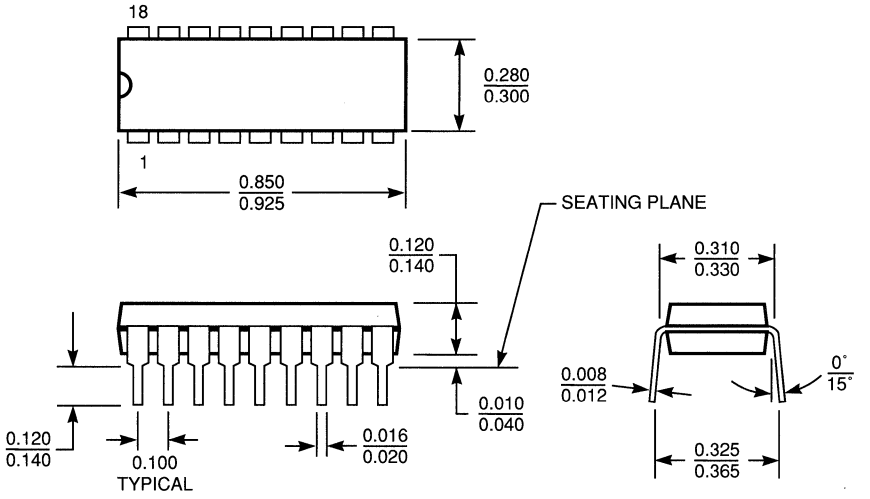
P12 — 16-pin, 0.3" wide



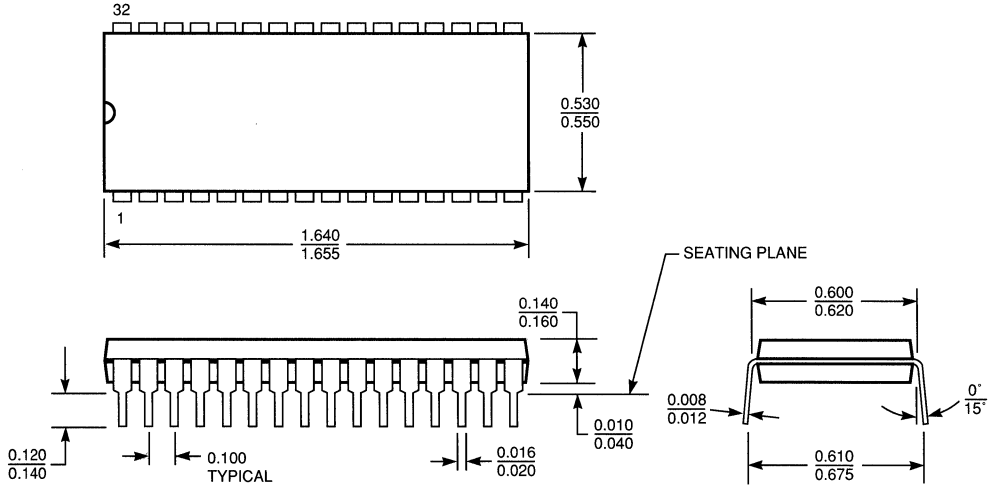
9

PLASTIC DIP (ORDERING CODE: P, N)

P13 — 18-pin, 0.3" wide

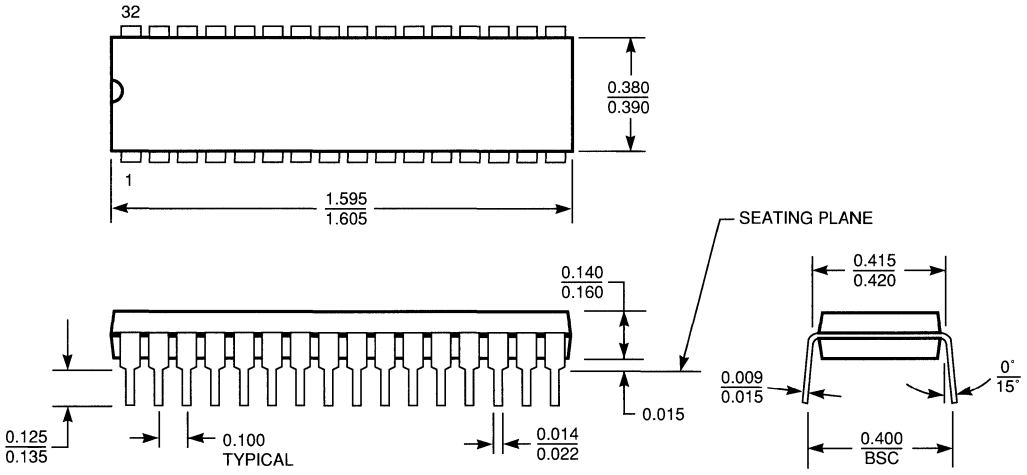


P14 — 32-pin, 0.6" wide



Plastic DIP (Ordering Code: P, N)

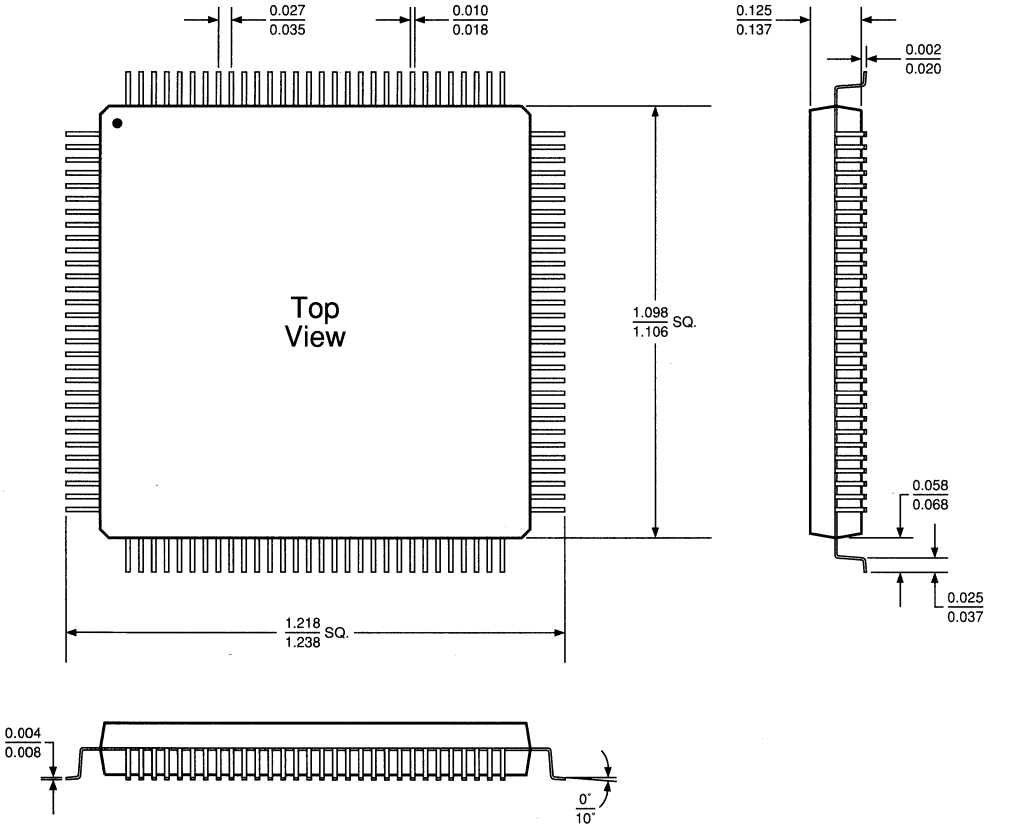
P15 — 32-pin, 0.4" wide



9

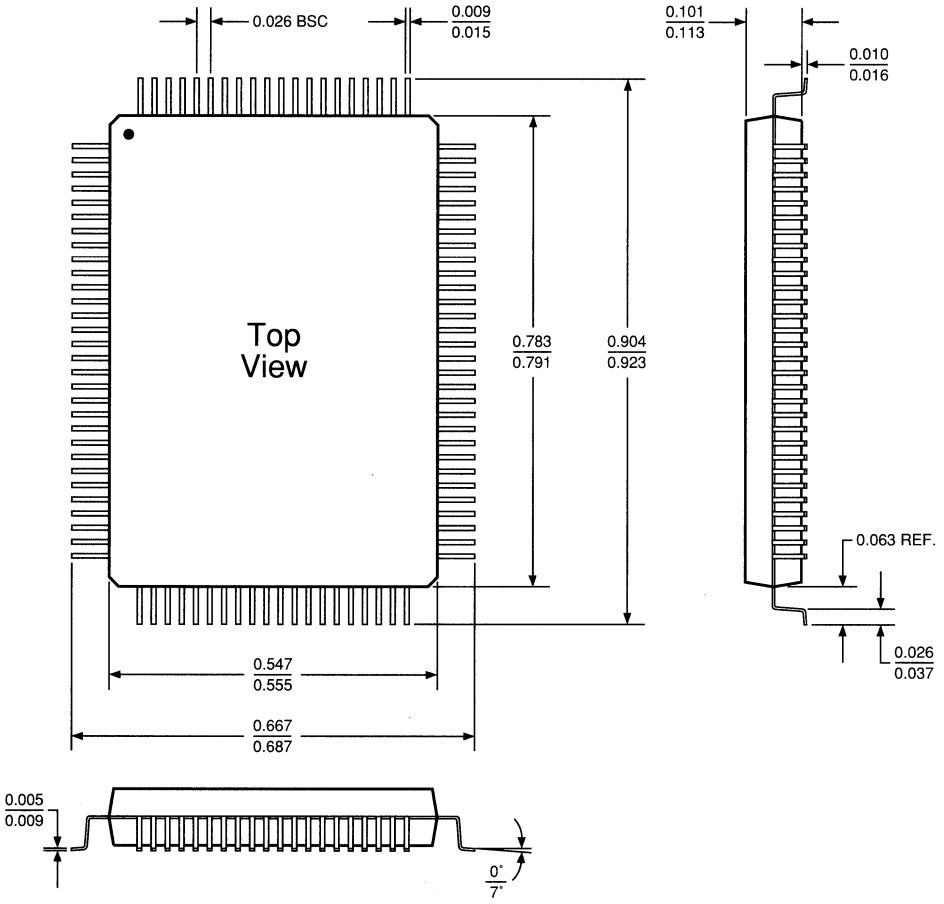
Plastic Quad Flatpack (Ordering Code: Q)

Q1 — 120-pin



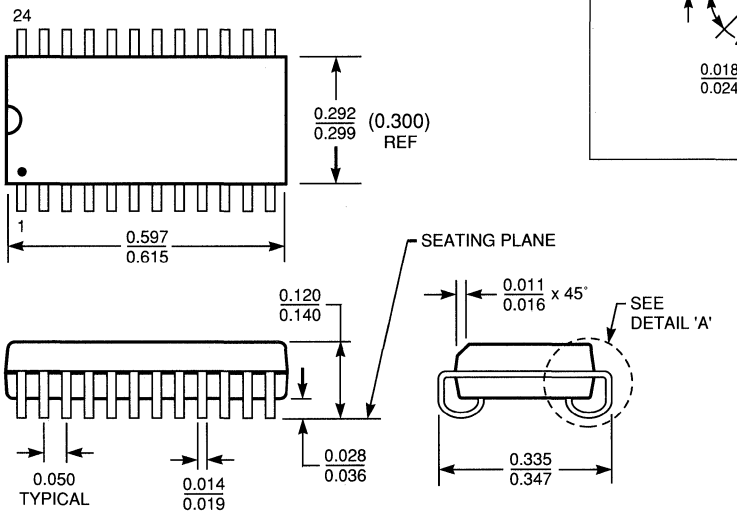
Plastic Quad Flatpack (Ordering Code: Q)

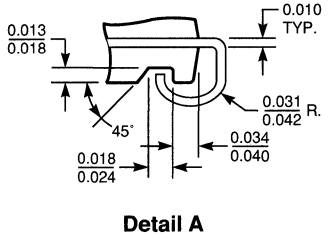
Q2 — 100-pin



PLASTIC SOJ (ORDERING CODE: W)

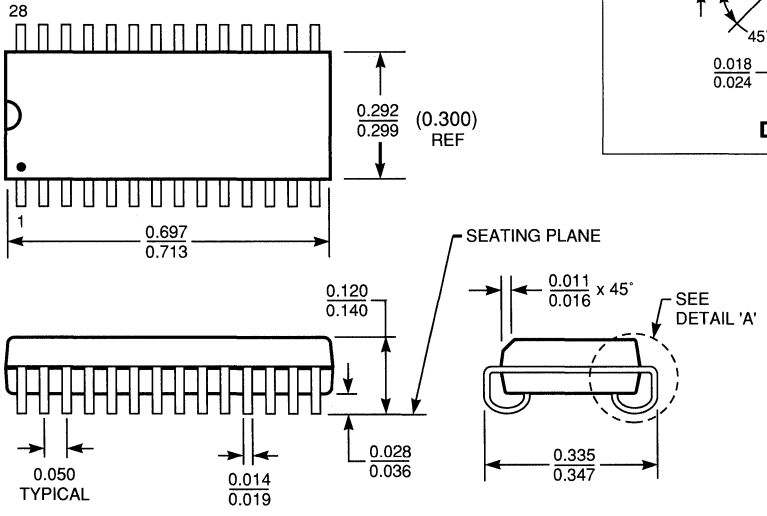
W1 — 24-pin, 0.3" wide

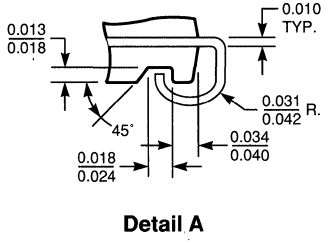




Detail A

W2 — 28-pin, 0.3" wide

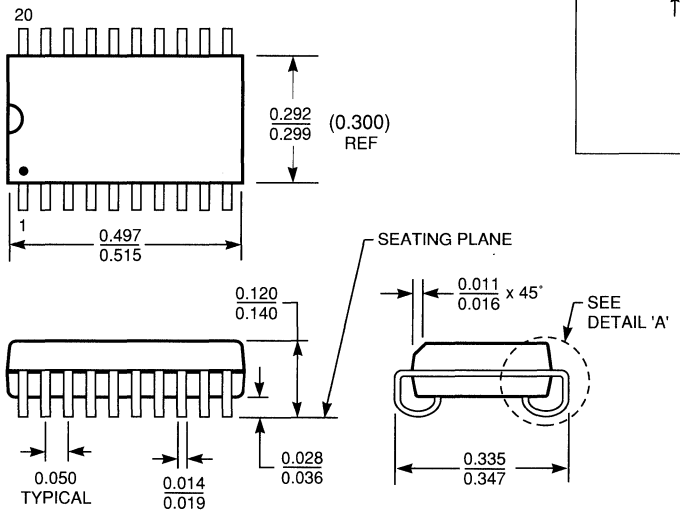


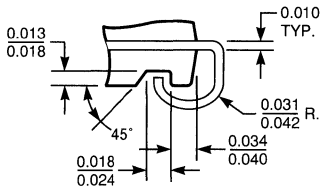


Detail A

Plastic SOJ (Ordering Code: W)

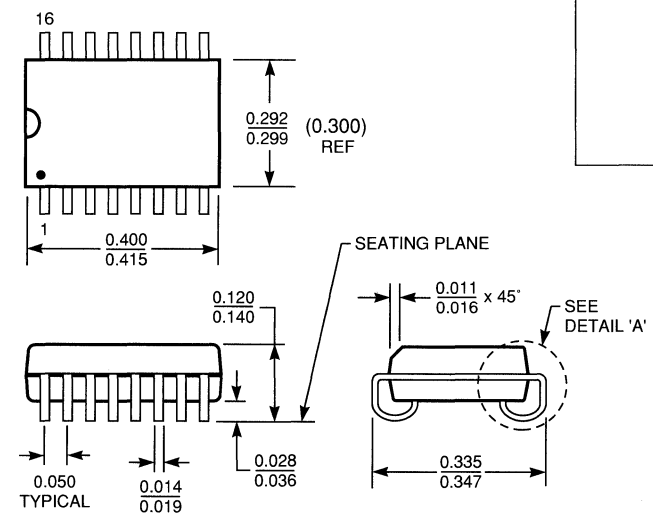
W3 — 20-pin, 0.3" wide

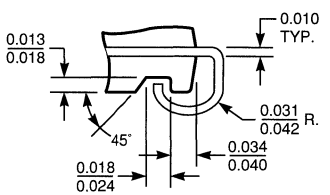




Detail A

W4 — 16-pin, 0.3" wide



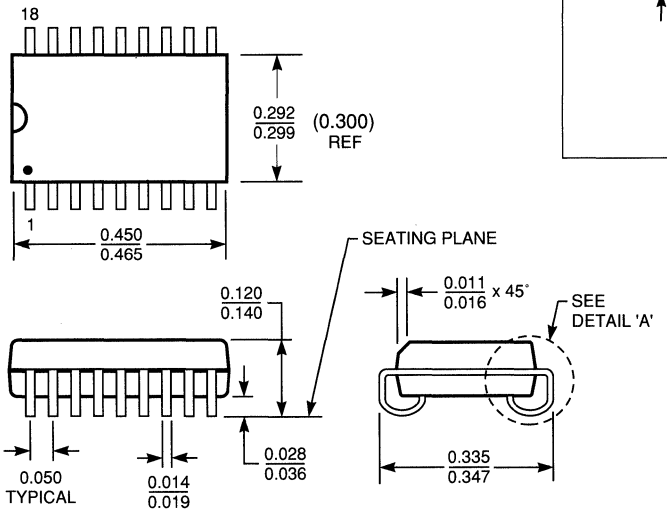


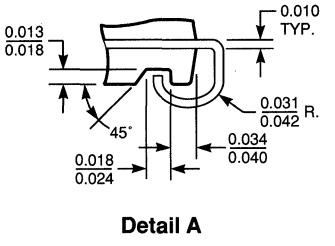
Detail A

9

PLASTIC SOJ (ORDERING CODE: W)

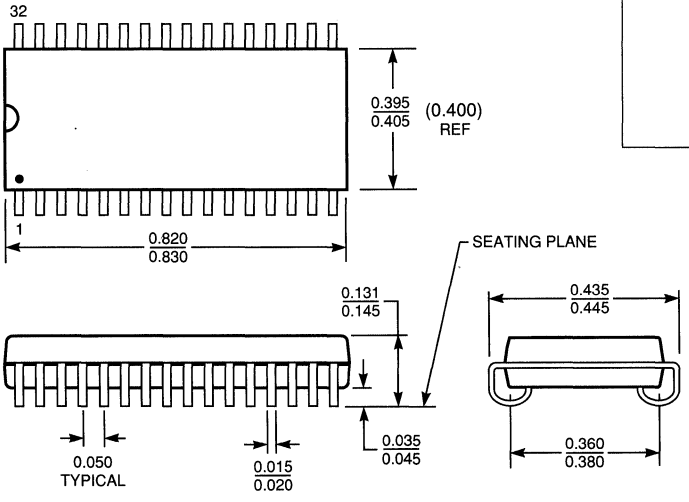
W5 — 18-pin, 0.3" wide

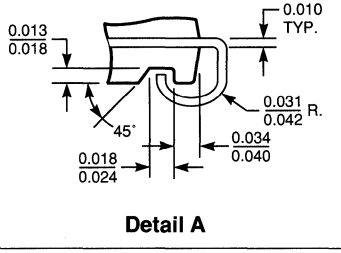




Detail A

W6 — 32-pin, 0.4" wide





Detail A

Ordering Information 1
Video Imaging Products 2
Arithmetic Logic Units & Special Arithmetic Functions 3
Multipliers & Multiplier-Accumulators 4
Register Products 5
Peripheral Products 6
Quality and Reliability 7
Technology and Design Features 8
Package Information 9
Product Listing 10
Sales Offices 11

Product Listing

10

DSP PRODUCTS

PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	SPEED (ns) MIL.	POWER (mW)	PACKAGE AVAILABILITY
VIDEO IMAGING PRODUCTS					
LF2242	12/16-bit Half-Band Digital Filter	15	TBA	—	44-lead PLCC
LF2246	11 x 10-bit Image Filter	25	TBA	—	120-pin PGA, 120-pin PQFP
LF2249	12 x 12-bit Digital Mixer	25	TBA	—	120-pin PGA, 120-pin PQFP
LF2250	12 x 10-bit Matrix Multiplier	25	TBA	—	120-pin PGA, 120-pin PQFP
LF2272	Colorspace Converter (3 x 12-bits)	25	TBA	—	120-pin PGA
LF43881	8 x 8-bit Digital Filter	33	40	—	84-pin PGA/PLCC, 100-pin PQFP
LF43891	9 x 9-bit Digtial Filter	33	40	—	84-pin PGA/PLCC, 100-pin PQFP
ARITHMETIC LOGIC UNITS					
L4C381	16-bit Cascadable ALU	15	20	75	68-lead LCC/PLCC, 68-pin PGA
L29C101	16-bit ALU Slice (Quad 2901)	35	45	75	64-pin DIP, 68-pin PGA
BARREL SHIFTERS					
LSH32	32-bit Barrel Shifter	20	30	50	68-lead LCC/PLCC, 68-pin PGA
LSH33	32-bit Barrel Shifter w/Registers	20	30	50	68-lead LCC/PLCC, 68-pin PGA
CORRELATORS					
L10C23	64 x 1 Digital Correlator	20	20	125	24-pin DIP, 28-lead LCC
MULTIPLIERS					
LMU08	8 x 8-bit, Signed	35	45	40	40-pin DIP, 44-lead LCC/PLCC
LMU8U	8 x 8-bit, Unsigned	35	45	40	40-pin DIP, 44-lead LCC/PLCC
LMU557	8 x 8-bit, Latched Output	60	70	85	40-pin DIP
LMU558	8 x 8-bit, Unregistered	60	70	85	40-pin DIP
LMU12	12 x 12-bit	35	45	60	64-pin DIP. 68-pin PGA
LMU112	12 x 12-bit, Reduced Pinout	50	55	50	48-pin DIP, 52-lead PLCC
LMU16	16 x 16-bit	45	55	60	64-pin DIP, 68-pin PGA
LMU216	16 x 16-bit, Surface Mount	45	55	60	68-lead LCC/PLCC
LMU17	16 x 16-bit, Microprogrammable	45	55	60	64-pin DIP, 68-pin PGA
LMU217	16 x 16-bit, Microprog., Surf. Mount	45	55	60	68-lead LCC/PLCC
LMU18	16 x 16-bit, 32 Outputs	35	45	125	84-pin PGA, 84-lead PLCC
MULTIPLIER-ACCUMULATORS					
LMA1009	12 x 12-bit	45	55	60	64-pin DIP, 68-pin PGA
LMA2009	12 x 12-bit, Surface Mount	45	55	60	68-lead LCC/PLCC
LMA1010	16 x 16-bit	45	55	60	64-pin DIP, 68-pin PGA
LMA2010	16 x 16-bit, Surface Mount	45	55	60	68-lead LCC/PLCC
MULTIPLIER-SUMMERS					
LMS12	12 x 12 + 26-bit, FIR	40	50	75	84-pin PGA, 84-lead PLCC

DSP PRODUCTS (CONTINUED)					
PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	SPEED (ns) MIL.	POWER (mW)	PACKAGE AVAILABILITY
PIPELINE REGISTERS					
L29C520	4 x 8-bit Multilevel (1-4 Stages)	14	16	50	24-pin DIP/FP, 28-lead LCC/PLCC
L29C521	4 x 8-bit Multilevel (1-4 Stages)	14	16	50	24-pin DIP/FP, 28-lead LCC/PLCC
LPR520	4 x 16-bit Multilevel (1-4 Stages)	15	18	50	40-pin DIP, 44-lead LCC/PLCC
LPR521	4 x 16-bit Multilevel (1-4 Stages)	15	18	50	40-pin DIP, 44-lead LCC/PLCC
LPR200	8 x 16-bit Multilevel (1-8 Stages)	10	12	50	48-pin DIP, 52-lead LCC/PLCC
LPR201	7 x 16-bit Multilevel (1-7 Stages)	10	12	50	48-pin DIP, 52-lead LCC/PLCC
L29C524	14 x 8-bit Dual 7-Deep (1-14 Stages)	15	20	50	28-pin DIP/FP, 28-lead PLCC
L29C525	16 x 8-bit Dual 8-Deep (1-16 Stages)	15	20	50	28-pin DIP/FP, 28-lead PLCC
L10C11	4/8-bit Var. Length (3-18 Stages)	15	20	50	24-pin DIP, 28-lead PLCC
REGISTER FILES					
LRF07	8 x 8-bit Register File (3-Port)	20	25	50	40-pin DIP, 44-lead LCC
SHADOW REGISTERS					
L29C818	8-bit Serial Scan Shadow Register	15	24	50	24-pin DIP, 28-lead LCC

PERIPHERAL PRODUCTS					
PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	SPEED (ns) MIL.	POWER (mW)	PACKAGE AVAILABILITY
L5380	SCSI Bus Controller	4 Mb/s	2 Mb/s	50	40-pin DIP, 44-lead LCC/PLCC
L53C80	SCSI Bus Controller	4 Mb/s	2 Mb/s	50	48-pin DIP, 44-lead LCC/PLCC

MEMORY PRODUCTS						
PART NO.	PRODUCT DESCRIPTION	SPEED (ns) COM.	SPEED (ns) MIL.	POWER (mW) OPER.	POWER (mW) INACTIVE	PACKAGE AVAILABILITY
16K STATIC RAMS						
L6116	2K x 8, Common I/O + OE	12	15	250	75	24-pin DIP/SOJ, 28/32-lead LCC
64K STATIC RAMS						
L7C187	64K x 1, Separate I/O	12	15	135	75	22-pin DIP, 24-pin SOJ
L7C162	16K x 4, Separate I/O	12	15	210	75	28-pin DIP/SOJ/LCC
L7C164	16K x 4, Common I/O	12	15	210	75	22-pin DIP, 24-pin SOJ
L7C166	16K x 4, Common I/O + OE	12	15	210	75	24-pin DIP/SOJ, 28-lead LCC
L7C185	8K x 8, Common I/O	12	15	320	75	28-pin DIP/FP/SOJ, 28/32-lead LCC
256K STATIC RAMS						
L7C197	256K x 1, Separate I/O	15	20	165	100	24-pin DIP/SOJ, 28-lead LCC
L7C194	64K x 4, Common I/O	15	20	210	100	24-pin DIP/SOJ, 28-lead LCC
L7C195	64K x 4, Common I/O + OE	15	20	210	100	28-pin DIP/SOJ
L7C199	32K x 8, Common I/O + OE	15	20	490	100	28-pin DIP/FP/SOJ, 28/32-lead LCC
1M STATIC RAMS						
L7C108	128K x 8, Common I/O, 1 CE + OE	15	20	550	50	32-pin DIP/SOJ, 32-lead LCC
L7C109	128K x 8, Common I/O, 2 CE + OE	15	20	550	50	32-pin DIP/SOJ, 32-lead LCC
SPECIAL ARCHITECTURE STATIC RAMS						
L7C174	8K x 8, Cache-Tag	12	15	320	0.5	28-pin DIP/SOJ, 32-lead LCC

DESC SMD PRODUCTS (LISTED BY LOGIC DEVICES PART NUMBER)

PART NO.	DESC SMD NUMBER	AVAILABILITY	PRODUCT DESCRIPTION
DSP PRODUCTS			
L10C23	5962-89711	Released	64 x 1 Digital Correlator
L29C101	5962-89517	Released	16-bit ALU Slice (Quad 2901)
L29C520	5962-91762	Released	4 x 8-bit Multilevel Pipeline Register
L29C521	5962-91762	Released	4 x 8-bit Multilevel Pipeline Register
L29C525	5962-91696	Released	16 x 8-bit Dual 8-Deep Pipeline Register
L29C818	5962-90515	Released	8-bit Serial Scan Shadow Register
L4C381	5962-89959	Released	16-bit Cascadable ALU
LF2250	5962-93260	Released	12 x 10-bit Matrix Multiplier
LMA1009	5962-90996	Released	12 x 12-bit Multiplier-Accumlator
LMA2009	5962-90996	Released	12 x 12-bit Multiplier-Accumlator
LMA1010	5962-88733	Released	16 x 16-bit Multiplier-Accumlator
LMA2010	5962-88733	Released	16 x 16-bit Multiplier-Accumlator
LMS12	TBA	Future	12 x 12 + 26-bit Multiplier-Summer, FIR
LMU08	5962-88739	Released	8 x 8-bit Parallel Multiplier
LMU8U	5962-88739	Released	8 x 8-bit Parallel Multiplier
LMU16	5962-86873	Released	16 x 16-bit Parallel Multiplier
LMU216	5962-86873	Released	16 x 16-bit Parallel Multiplier
LMU17	5962-87686	Released	16 x 16-bit Parallel Multiplier
LMU217	5962-87686	Released	16 x 16-bit Parallel Multiplier
LMU18	5962-94523	Released	16 x 16-bit Parallel Multiplier w/32 outputs
LPR520	5962-89716	Released	4 x 16-bit Multilevel Pipeline Register
LPR521	5962-89716	Released	4 x 16-bit Multilevel Pipeline Register
LSH32	5962-89717	Released	32-bit Barrel Shifter
PERIPHERAL PRODUCTS			
L5380	5962-90548	Released	SCSI Bus Controller
L53C80	5962-90548	Released	SCSI Bus Controller
MEMORY PRODUCTS			
L6116	5962-84036	Released	2K x 8 Static RAM
L6116	5962-89690	Released	2K x 8 Static RAM
L6116	5962-88740	Released	2K x 8 Static RAM, Low Power
L7C108	5962-89598	Released	128K x 8 Static RAM
L7C109	5962-89598	Released	128K x 8 Static RAM
L7C162	5962-89712	Released	16K x 4 Static RAM
L7C164	5962-89692	Future	16K x 4 Static RAM
L7C166	5962-89892	Future	16K x 4 Static RAM
L7C168	5962-86705	Released	4K x 4 Static RAM
L7C174	TBA	Pending	8K x 8 Static RAM, Cache-Tag
L7C185	5962-38294	Released	8K x 8 Static RAM
L7C191	5962-90664	Consult Factory	64K x 4 Static RAM
L7C192	5962-89935	Consult Factory	64K x 4 Static RAM
L7C194	5962-88681	Consult Factory	64K x 4 Static RAM
L7C197	5962-88544	Consult Factory	256K x 1 Static RAM
L7C199	5962-88552	Released	32K x 8 Static RAM, Low Power
L7C199	5962-88662	Released	32K x 8 Static RAM

DESC SMD PRODUCTS (LISTED BY SMD NUMBER)			
DESC SMD NO.	**LOGIC PART NO.**	**AVAILABILITY**	**PRODUCT DESCRIPTION**
DSP PRODUCTS			
5962-86873	LMU16/LMU216	Released	16 x 16-bit Parallel Multiplier
5962-87686	LMU17/LMU217	Released	16 x 16-bit Parallel Multiplier
5962-88733	LMA1010/LMA2010	Released	16 x 16-bit Multiplier-Accumlator
5962-88739	LMU08/8U	Released	8 x 8-bit Parallel Multiplier
5962-89517	L29C101	Released	16-bit ALU Slice (Quad 2901)
5962-89711	L10C23	Released	64 x 1 Digital Correlator
5962-89716	LPR520/LPR521	Released	4 x 16-bit Multilevel Pipeline Register
5962-89717	LSH32	Released	32-bit Barrel Shifter
5962-89959	L4C381	Released	16-bit Cascadable ALU
5962-90515	L29C818	Released	8-bit Serial Scan Shadow Register
5962-90996	LMA1009/LMA2009	Released	12 x 12-bit Multiplier-Accumlator
5962-91696	L29C525	Released	16 x 8-bit Dual 8-Deep Pipeline Register
5962-91762	L29C520/L29C521	Released	4 x 8-bit Multilevel Pipeline Register
5962-93260	LF2250	Released	12 x 10-bit Matrix Multiplier
5962-94523	LMU18	Released	16 x 16-bit Parallel Multiplier w/32 outputs
PERIPHERAL PRODUCTS			
5962-90548	L5380/L53C80	Released	SCSI Bus Controller
MEMORY PRODUCTS			
5962-38294	L7C185	Released	8K x 8 Static RAM
5962-84036	L6116	Released	2K x 8 Static RAM
5962-86705	L7C168	Released	4K x 4 Static RAM
5962-88544	L7C197	Consult Factory	256K x 1 Static RAM
5962-88552	L7C199	Released	32K x 8 Static RAM, Low Power
5962-88662	L7C199	Released	32K x 8 Static RAM
5962-88681	L7C194	Consult Factory	64K x 4 Static RAM
5962-88740	L6116	Released	2K x 8 Static RAM, Low Power
5962-89598	L7C108/L7C109	Released	128K x 8 Static RAM
5962-89690	L6116	Released	2K x 8 Static RAM
5962-89692	L7C164	Future	16K x 4 Static RAM
5962-89712	L7C162	Released	16K x 4 Static RAM
5962-89892	L7C166	Future	16K x 4 Static RAM
5962-89935	L7C192	Consult Factory	64K x 4 Static RAM
5962-90664	L7C191	Consult Factory	64K x 4 Static RAM

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Arithmetic Logic Units & Special Arithmetic Functions 3
Multipliers & Multiplier-Accumulators 4
Register Products 5
Peripheral Products 6
Quality and Reliability 7
Technology and Design Features 8
Package Information 9
Product Listing 10
Sales Offices 11

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11

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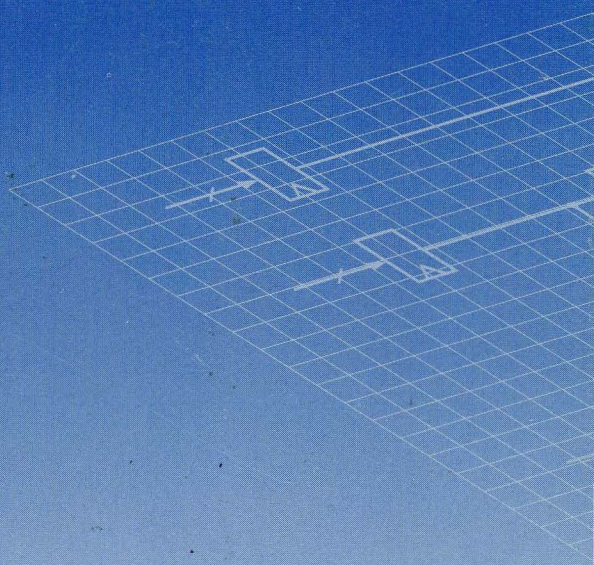

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