MITSUBISHI SEMICONDUCTORS 1988

BIPOLAR DIGITAL IC
LSTTL

DATA BOOK

MITSUBISHI ELECTRIC

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INDEX BY FUNCTION (Recommended operating conditions $V_{CC} = 5V \pm 5\%$, $T_{opr} = -20 \sim +75°C$)

INVERTERS, NAND GATES

Circuit function	Type of output: Active pull-up	Type of output: Open collector	Type	Typical electrical characteristics: Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)	Package Outlines	Interchangeable products	Page
Hex Inverter	○	—	M74LS04P	6	12	8	0.4	14P4	74LS04	2-15
	—	○	M74LS05P	10	12	8	—	14P4	74LS05	2-17
Quadruple 2-Input Positive NAND Gate	○	—	M74LS00P	6	8	8	0.4	14P4	74LS00	2-9
	—	○	M74LS03P	10	8	8	—	14P4	74LS03	2-13
Triple 3-Input Positive NAND Gate	○	—	M74LS10P	8	6	8	0.4	14P4	74LS10	2-23
	—	○	M74LS12P	13	6.3	8	—	14P4	74LS12	2-27
Dual 4-Input Positive NAND Gate	○	—	M74LS20P	10	4	8	0.4	14P4	74LS20	2-39
	—	○	M74LS22P	18	4	8	—	14P4	74LS22	2-43
Single 8-Input Positive NAND Gate	○	—	M74LS30P	11	2.4	8	0.4	14P4	74LS30	2-49
Single 13-Input Positive NAND Gate	○	—	M74LS133P	11	2.4	8	0.4	16P4	74LS133	2-143

AND GATES

Quadruple 2-Input Positive AND Gate	○	—	M74LS08P	10	17	8	0.4	14P4	74LS08	2-19
	—	○	M74LS09P	13	17	8	—	14P4	74LS09	2-21
Triple 3-Input Positive AND Gate	○	—	M74LS11P	10	12.8	8	0.4	14P4	74LS11	2-25
	—	○	M74LS15P	13	12.8	8	—	14P4	74LS15	2-33
Dual 4-Input Positive AND Gate	○	—	M74LS21P	10	8.5	8	0.4	14P4	74LS21	2-41

NOR GATES

Quadruple 2-Input Positive NOR Gate	○	—	M74LS02P	6	10	8	0.4	14P4	74LS02	2-11
Triple 3-Input Positive NOR Gate	○	—	M74LS27P	6	13.5	8	0.4	14P4	74LS27	2-47

OR GATE

Quadruple 2-Input Positive OR Gate	○	—	M74LS32P	7	20	8	0.4	14P4	74LS32	2-51

EXCLUSIVE OR GATES

Quadruple 2-Input Exclusive OR Gate	○	—	M74LS86P	10	30.5	8	0.4	14P4	74LS86	2-90
	—	○	M74LS136P	13	30.5	8	—	14P4	74LS136	2-145
	○	—	M74LS386P	10	30.5	8	0.4	14P4	74LS386	2-366

EXCLUSIVE NOR GATE

Quadruple 2-Input Exclusive NOR Gate	—	○	M74LS266P	15	40	8	—	14P4	74LS266	2-302

AND-OR-INVERT GATE

Dual 2-Wide 2-Input AND-OR-INVERT Gate	○	—	M74LS51P	7	5.5	8	0.4	14P4	74LS51	2-69

BUFFERS/LINE DRIVERS

Circuit function	Type of output: Active pull-up	Type of output: Open collector	Type of output: 3-state	Type	Typical electrical characteristics: Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)	Hysteresis (V_{T+}-V_{T-}) (V)	Package Outlines	Interchangeable products	Page
Octal Buffer/Line Driver			I	**M74LS240P**	8	120	24	15	0.4	20P4	74LS240	2-256
	—	—	N	**M74LS241P**	9	126.7	24	15	0.4	20P4	74LS241	2-259
			N	**M74LS244P**	9	126.7	24	15	0.4	20P4	74LS244	2-269
	—	—	I	**M74LS540P**	10	111.7	24	15	0.4	20P4	74LS540	2-385
	—	—	N	**M74LS541P**	10	133.3	24	15	0.4	20P4	74LS541	2-388
Octal Bus Transceiver	—	—	N	**M74LS245P**	10	290	24	15	0.4	20P4	74LS245	2-272
	—	—	I	**M74LS620P**	10	290	24	15	0.4	20P4	74LS620	2-399
	—	—	I	**M74LS640P**	10	290	24	15	0.4	20P4	74LS640	2-402
	—	—	I	**M74LS640-1P**	10	290	48	15	0.4	20P4	74LS640-1	2-405
	—	N	—	**M74LS641P**	18	290	24	—	0.4	20P4	74LS641	2-408
	—	N	—	**M74LS641-1P**	18	290	48	—	0.4	20P4	74LS641-1	2-411
	—	I	—	**M74LS642P**	15	290	24	—	0.4	20P4	74LS642	2-414
	—	I	—	**M74LS642-1P**	15	290	48	—	0.4	20P4	74LS642-1	2-417
	—	—	I·N	**M74LS643P**	10	290	24	15	0.4	20P4	74LS643	2-420
	—	—	I·N	**M74LS643-1P**	10	290	48	15	0.4	20P4	74LS643-1	2-423
	—	I·N	—	**M74LS644P**	16	290	24	—	0.4	20P4	74LS644	2-426
	—	I·N	—	**M74LS644-1P**	16	290	48	—	0.4	20P4	74LS644-1	2-429
	—	—	N	**M74LS645P**	12	290	24	15	0.4	20P4	74LS645	2-432
	—	—	N	**M74LS645-1P**	12	290	48	15	0.4	20P4	74LS645-1	2-435
Hex Bus Driver	—	—	N	**M74LS365AP**	9	67.5	24	2.6	—	16P4	74LS365A	2-341
	—	—	I	**M74LS366AP**	7	59	24	2.6	—	16P4	74LS366A	2-344
	—	—	N	**M74LS367AP**	9	67.5	24	2.6	—	16P4	74LS367A	2-347
	—	—	I	**M74LS368AP**	7	59	24	2.6	—	16P4	74LS368A	2-350
Quadruple 2-Input Positive NAND Buffer	I	—	—	**M74LS37P**	10	17.3	24	1.2	—	14P4	74LS37	2-53
	—	I	—	**M74LS38P**	14	17.3	24	—	—	14P4	74LS38	2-55
Quadruple Bus Buffer Gate	—	—	N	**M74LS125AP**	9	51.8	24	2.6	—	14P4	74LS125A	2-137
	—	—	N	**M74LS126AP**	9	59	24	2.6	—	14P4	74LS126A	2-139
Quadruple Bus Transceiver	—	—	I	**M74LS242P**	8	133.3	24	15	0.4	14P4	74LS242	2-263
	—		N	**M74LS243P**	9	138.3	24	15	0.4	14P4	74LS243	2-266
Dual 4-Input Positive NAND Buffer	I	—	—	**M74LS40P**	14	8.6	24	1.2	—	14P4	74LS40	2-57

I : With inverted output N : With noninverted output I·N : With both inverted and noninverted output

SCHMITT TRIGGER NAND GATES/INVERTERS

Circuit function	Type of output: Active pull-up	Type of output: Open collector	Type	Typical electrical characteristics: Propagation time (ns)	Power dissipation (mW)	Positive-going threshold voltage (V)	Negative-going threshold voltage (V)	Package Outlines	Interchangeable products	Page
Hex Schmitt Trigger Inverter	I	—	**M74LS14P**	12	51.5	1.6	0.8	14P4	74LS14	2-31
	I	—	**M74LS19P**	13	67	1.9	1.0	14P4	74LS19	2-37
Quadruple 2-Input Positive NAND Schmitt Trigger	I	—	**M74LS132P**	13	35.3	1.6	0.8	14P4	74LS132	2-141
	I	—	**M74LS24P**	19	44	1.9	1.0	14P4	74LS24	2-45
Dual 4-Input Positive NAND Schmitt Trigger	I	—	**M74LS13P**	16	17.5	1.6	0.8	14P4	74LS13	2-29
	I	—	**M74LS18P**	25	22.5	1.9	1.0	14P4	74LS18	2-35

I : With inverted output

J-K FLIP-FLOPS

Circuit function	Type	Typical electrical characteristics				Trigger	Preset	Reset	Package Outlines	Interchangeable products	Page
		Operating frequency (MHz)	Setup time (ns)	Hold time (ns)	Power dissipation (mW)						
Dual J-K Negative Edge-Triggered Flip-Flop with Reset	**M74LS73AP**	0~45	20	0	20	↓	—	⊔	14P4	74LS73A	2-71
Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset	**M74LS76AP**	0~45	20	0	20	↓	⊔	⊔	16P4	74LS76A	2-80
Dual J-K Negative Edge-Triggered Flip-Flop with Reset	**M74LS107AP**	0~45	20	0	20	↓	—	⊔	14P4	74LS107A	2-112
Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop with Set and Reset	**M74LS109AP**	0~45	20	5	20	↑	⊔	⊔	16P4	74LS109A	2-115
Dual J-K Negative Edge-Triggered Flip-Flop with Set and Reset	**M74LS112AP**	0~45	20	0	20	↓	⊔	⊔	16P4	74LS112A	2-118
Dual J-K Negative Edge-Triggered Flip-Flop with Set	**M74LS113AP**	0~45	20	0	20	↓	⊔	—	14P4	74LS113A	2-121
Dual J-K Negative Edge-Triggered Flip-Flop with Set Common Reset and Common Clock	**M74LS114AP**	0~45	20	0	20	↓	⊔	⊔	14P4	74LS114A	2-124

↑ : Positive-going edge ↓ : Negative-going edge ⊔ : Active low-level

D-Type FLIP FLOPS

Circuit function	Type	Typical electrical characteristics				Trigger	Preset	Reset	Package Outlines	Interchangeable products	Page
		Operating frequency (MHz)	Setup time (ns)	Hold time (ns)	Power dissipation (mW)						
Dual D-Type Edge-Triggered Flip-Flop with Set and Reset	**M74LS74AP**	0~50	20	5	20	↑	⊔	⊔	14P4	74LS74A	2-74
Hex D-Type Flip-Flop with Reset	**M74LS174P**	0~47	20	5	80	↑	—	⊔	16P4	74LS174	2-214
Quadruple D-Type Flip-Flop with Reset	**M74LS175P**	0~50	20	5	55	↑	—	⊔	16P4	74LS175	2-217
Octal Positive Edge-Triggered D-Type Flip-Flop with Reset	**M74LS273P**	0~40	20	5	85	↑	—	⊔	20P4	74LS273	2-304
Octal Positive Edge-Triggered D-Type Flip-Flop with 3-State Outputs	**M74LS374P**	0~40	20	4	135	↑	—	—	20P4	74LS374	2-356
Octal Positive Edge-Triggered D-Type Flip-Flop with Enable	**M74LS377P**	0~40	25	5	85	↑	—	—	20P4	74LS377	2-363

↑ : Positive-going edge

⊔ : Active low-level

LATCHES, REGISTERS

Circuit function	Type	Typical electrical characteristics				Enable	Reset	Package Outlines	Interchangeable products	Page
		Power dissipation (ns)	Setup time (ns)	Hold time (ns)	Power dissipation (mW)					
4-Bit Bistable Latch	**M74LS75P**	9	20	8	31.5	⊓	—	16P4	74LS75	2-77
	M74LS375P	9	20	8	31.5	⊓	—	16P4	74LS375	2-360
Dual 4-Bit Addresable Latch	**M74LS256P**	13	15	5	100	—	⊔	16P4	74LS256	2-288
8-Bit Addressable Latch	**M74LS259P**	13	15	5	100	—	⊔	16P4	74LS259	2-298
Quadruple R-S Latch	**M74LS279P**	10	—	—	19	—	—	16P4	74LS279	2-307
Octal D-Type Transparent Latch with 3-State Outputs	**M74LS373P**	12	5	20	120	⊓	—	20P4	74LS373	2-353
4-Bit D-Type Register with 3-State Outputs	**M74LS173AP**	23	17	6	85	↑	⊓	16P4	74LS173A	2-210

⊓ : Active high-level

⊔ : Active low-level

↑ : Positive-going edge

SHIFT REGISTERS

Circuit function	Type	Typical electrical characteristics: Operating frequency (MHz)	Typical electrical characteristics: Power dissipation (mW)	Reset	Mode: Right shift	Mode: Left shift	Mode: Parallel load	Mode: Hold (Do nothing)	Package Outlines	Interchangeable products	Page
8-Bit Universal Shift/Storage Register	**M74LS299P**	0~28	165	A	○	○	○	○	20P4	74LS299	2-328
	M74LS323P	0~28	165	S	○	○	○	○	20P4	74LS323	2-332
4-Bit Bidirectional Universal Shift Register	**M74LS194AP**	0~45	75	A	○	○	○	○	16P4	74LS194A	2-236
5-Bit Shift Register	**M74LS96P**	0~45	60	A	○	—	○	—	16P4	74LS96	2-108
4-Bit Cascadable Shift Register with 3-State Outputs	**M74LS395AP**	0~40	83.8	A	○	—	○	—	16P4	74LS395	2-374
4-Bit Parallel Access Shift Register	**M74LS195AP**	0~60	70	A	○	—	○	—	16P4	74LS195A	2-239
4-Bit Parallel Access Shift Register	**M74LS95BP**	0~50	65	—	○	—	○	—	14P4	74LS95B	2-105
4-Bit Shift Register with 3-State Outputs	**M74LS295BP**	0~40	72.5	—	○	—	○	—	14P4	74LS295B	2-322
8-Bit Serial-In Parallel-Out Shift Register	**M74LS164P**	0~50	80	A	○	—	—	—	14P4	74LS164	2-196
8-Bit Shift Register	**M74LS91P**	0~60	60	—	○	—	—	—	14P4	74LS91	2-95
8-Bit Parallel-Load Shift Register	**M74LS165AP**	0~38	105	—	○	—	—	—	16P4	74LS165A	2-199
8-Bit Shift Register	**M74LS166AP**	0~38	100	A	○	—	—	—	16P4	74LS166A	2-203
8-Bit Shift Register/Latch with 3-State Output	**M74LS595P**			A	○	—	—	○	16P4	74LS595	2-391
8-Bit Shift Register/Latch with Open Collector Output	**M74LS596P**			A	○	—	—	○	16P4	74LS596	2-395

A : Asynchronous
S : Synchronous

ASYNCHRONOUS COUNTERS

Circuit function	Organization	Type	Typical electrical characteristics: Clock frequency (MHz)	Typical electrical characteristics: Power dissipation (mW)	Trigger	Parallel load	Reset	Package Outlines	Interchangeable products	Page
Decade Counter	2×5	**M74LS90P**	0~75 0~30	45	↓	"9" set	⊓	14P4	74LS90	2-92
	2×5	**M74LS290P**	0~75 0~30	45	↓	"9" set	⊓	14P4	74LS290	2-316
Presettable Decade Counter/Latch	2×5	**M74LS196P**	0~80 0~25	80	↓	A	⊔	14P4	74LS196	2-242
4-Bit Binary Counter	2×8	**M74LS93P**	0~60 0~35	45	↓	—	⊓	14P4	74LS93	2-101
	2×8	**M74LS293P**	0~60 0~35	45	↓	—	⊓	14P4	74LS293	2-319
Presettable 4-Bit Binary Counter/Latch	2×8	**M74LS197P**	0~80 0~35	80	↓	A	⊔	14P4	74LS197	2-246
Divide-by-Twelve Counter	2×6	**M74LS92P**	0~80 0~30	45	↓	—	⊓	14P4	74LS92	2-98
Dual Decade Counter	2×5	**M74LS390P**	0~80 0~35	100	↓	—	⊓	16P4	74LS390	2-368
Dual 4-Bit Decade Counter	2×5	**M74LS490P**	0~35	75	↓	—	⊓	16P4	74LS490	2-382
Dual 4-Bit Binary Counter	16	**M74LS393P**	0~75	100	↓	—	⊓	14P4	74LS393	2-371

↓ : Negative-going edge
A : Asynchronous
"9" set: Output Q_A and Q_D can be set to high directly, and output Q_B and Q_C to low.

SYNCHRONOUS COUNTERS

Circuit function	Type	Typical electrical characteristics: Clock frequency (MHz)	Typical electrical characteristics: Power dissipation (mW)	Trigger	Parallel load	Reset	Package Outlines	Interchangeable products	Page
Synchronous Presettable Decade Counter with Direct Reset	**M74LS160AP**	0~55	92.5	↓	S	A	16P4	74LS160A	2-180
Fully Synchronous Presettable Decade Counter	**M74LS162AP**	0~55	92.5	↓	S	S	16P4	74LS162A	2-188
Synchronous Presettable Up/Down Decade Counter with Mode Control	**M74LS190P**	0~38	100	↓	A	—	16P4	74LS190	2-220
Synchronous Presettable Up/Down Decade Counter	**M74LS192P**	0~38	95	↓	A	A	16P4	74LS192	2-228
Synchronous Presettable 4-Bit Binary Counter with Direct Reset	**M74LS161AP**	0~55	92.5	↓	S	A	16P4	74LS161A	2-184
Fully Synchronous Presettable 4-Bit Binary Counter	**M74LS163AP**	0~55	92.5	↓	S	S	16P4	74LS163A	2-192
Synchronous Presettable Up/Down 4-Bit Binary Counter with Mode Control	**M74LS191P**	0~40	100	↓	A	—	16P4	74LS191	2-224
Synchronous Presettable Up/Down 4-Bit Binary Counter	**M74LS193P**	0~38	95	↓	A	A	16P4	74LS193	2-232
Synchronous Up/Down Decade Counter	**M74LS668P**	0~45	100	↓	S	—	16P4	74LS668	2-438
Synchronous Up/Down 4-Bit Binary Counter	**M74LS669P**	0~30	100	↓	S	—	16P4	74LS669	2-444

↓ : Positive-going edge
A : Asynchronous
S : Synchronous

MONOSTABLE MULTIVIBRATORS

Circuit function	Type	Typical electrical characteristics: Output pulse width	Typical electrical characteristics: Power dissipation (mW)	Typical electrical characteristics: External timing resistor/capacitor for setting output pulse width	Package Outlines	Interchangeable products	Page
Retriggerable Monostable Multivibrator with Reset	**M74LS122P**	70ns~∞	30	5~260kΩ/No limit	14P4	74LS122	2-127
Dual Retriggerable Monostable Multivibrator with Reset	**M74LS123P**	70ns~∞	60	5~260kΩ/No limit	16P4	74LS123	2-132
Dual Retriggerable Monostable Multivibrator with Reset	**M74LS423P**	70ns~∞	60	5~260kΩ/No limit	16P4	74LS423	2-377
Dual Monostable Multivibrator	**M74LS221P**	33ns~∞	62.5	1.4~100kΩ/0~1000μF	16P4	74LS221	2-250

DATA SELECTORS/MULTIPLEXERS

Circuit function	Type	Typical power dissipation (mW)	Typical propagation time (ns): From strobe (enable) input to output	Typical propagation time (ns): From data input to output	Typical propagation time (ns): From data input to inverted output	Package Outlines	Interchangeable products	Page
8-Line to 1-Line Data Selector/Multiplexer with Strobe	**M74LS151P**	30	15	15	8	16P4	74LS151	2-165
8-Line to 1-Line Data Selector/Multiplexer with 3-State Output	**M74LS251P**	33	13	15	7	16P4	74LS251	2-281
Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe	**M74LS153P**	31	12	10	—	16P4	74LS153	2-168
Dual 4-Line to 1-Line Data Selector/Multiplexer with 3-State Output	**M74LS253P**	38.8	12	10	—	16P4	74LS253	2-285
Dual 4-Line to 1-Line Data Selector/Multiplexer with Strobe(Inverted)	**M74LS352P**	31	11	—	7	16P4	74LS352	2-336
Dual 4-Line to 1-Line Data Selector/Multiplexer with 3-State Output (Inverted)	**M74LS353P**	38.8	13	—	8	16P4	74LS353	2-338
Quadruple 2-Line to 1-Line Data Selector/Multiplexer	**M74LS157P**	48.5	12	8	—	16P4	74LS157	2-176
Quadruple 2-Line to 1-Line Data Selector/Multiplexer (Inverted)	**M74LS158P**	24	8	—	5	16P4	74LS158	2-178
Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output	**M74LS257AP**	47	9	7	—	16P4	74LS257A	2-292
Quadruple 2-Line to 1-Line Data Selector/Multiplexer with 3-State Output (Inverted)	**M74LS258AP**	42.2	10	—	7	16P4	74LS258A	2-295
Quadruple 2-Input Multiplexer with Storage	**M74LS298P**	65	12 From clock input	—	—	16P4	74LS298	2-325

DISPLAY DECODERS/DRIVERS

Circuit function	Output active level	Type	Typical electrical characteristics: Power dissipation (mW)	Typical electrical characteristics: Low-level current output (mA)	Typical electrical characteristics: Output break-down voltage (V)	Package Outlines	Interchangeable products	Page
BCD-to-Decimal Decoder/Driver	"L"	**M74LS145P**	35	24	15	16P4	74LS145	2-156
BCD-to-7-Segment Decoder/Driver	"L"	**M74LS47P**	35	24	15	16P4	74LS47	2-62
BCD-to-7-Segment Decoder/Driver	"H"	**M74LS48P**	125	6	V_{CC}	16P4	74LS48	2-66
BCD-to-7-Segment Decoder/Driver	"L"	**M74LS247P**	35	24	15	16P4	74LS247	2-275
BCD-to-7-Segment Decoder/Driver	"H"	**M74LS248P**	125	6	V_{CC}	16P4	74LS248	2-278

Segment Identification of M74LS47P, M74LS48P

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Segment identification																

Segment Identification of M74LS247P, M74LS248P

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Segment identification																

DECODERS/DEMULTIPLEXERS

Circuit function	Type	Typical power dissipation (mW)	Typical propagation time (ns): From strobe (enable) input to output	Typical propagation time (ns): From data input to output	Package Outlines	Interchangeable products	Page
BCD-to-Decimal Decoder	**M74LS42P**	35	—	12	16P4	74LS42	2-59
3-Line to 8-Line Decoder/Demultiplexer with Address Latch	**M74LS137P**	55	10	12	16P4	74LS137	2-147
3-Line to 8-Line Decoder/Demultiplexer	**M74LS138P**	31.5	12	14	16P4	74LS138	2-151
Dual 2-Line to 4-Line Decoder/Demultiplexer	**M74LS139P**	34	10	13	16P4	74LS139	2-154
Dual 2-Bit Binary to 4-Line Decoder/Demultiplexer with Strobe	**M74LS155P**	30.5	16	13	16P4	74LS155	2-170
Dual 2-Bit Binary to 4-Line Decoder/Demultiplexer with Open Collector Outputs	**M74LS156P**	30.5	23	19	16P4	74LS156	2-173

ENCODER

Circuit function	Type	Typical electrical characteristics: Propagation time (ns)	Typical electrical characteristics: Power dissipation (mW)	Typical electrical characteristics: Low-level output current (mA)	Typical electrical characteristics: High-level output current (mA)	Package Outlines	Interchangeable products	Page
10-Line to 4-Line Priority Encoder	**M74LS147P**	16	55	8	0.4	16P4	74LS147	2-159
8-Line to 3-Line Priority Encoder	**M74LS148P**	15	55	8	0.4	16P4	74LS148	2-162

COMPARATOR

Circuit function	Type	Typical electrical characteristics				Package Outlines	Interchangeable products	Page
		Propagation time (ns)	Power dissipation (mW)	Low-level output current (mA)	High-level output current (mA)			
4-Bit Magnitude Comparator	**M74LS85P**	13	55	8	0.4	16P4	74LS85	2-86
8-Bit Magnitude Comparator	**M74LS682P**	20	210	24	0.4	20P4	74LS682	2-452
	M74LS683P	24	210	24	—	20P4	74LS683	2-456
	M74LS684P	20	200	24	0.4	20P4	74LS684	2-459
	M74LS685P	24	200	24	—	20P4	74LS685	2-462
	M74LS688P	14	200	24	0.4	20P4	74LS688	2-465
	M74LS689P	22	200	24	—	20P4	74LS689	2-468

PARITY GENERATOR/CHECKER

9-Bit Odd/Even parity Generator/Checker	**M74LS280P**	18	80	8	0.4	14P4	74LS280	2-310

ADDER

Circuit function	Type	Typical power dissipation (mW)	Typical propagation time (ns)		Package Outlines	Interchangeable products	Page
			Carry time	Add time			
4-Bit Binary Full Adder with Fast Carry	**M74LS83AP**	102.5	8	12	16P4	74LS83A	2-83
4-Bit Binary Full Adder with Fast Carry	**M74LS283P**	102.5	8	12	16P4	74LS283	2-313

REGISTER FILES

Circuit function	Type	Typical power dissipation (mW)	Typical propagation time (ns)		Package Outlines	Interchangeable products	Page
			Write time	Read time			
4-By-4 Register File with Open Collector Outputs	**M74LS170P**	125	15	16	16P4	74LS170	2-207
4-By-4 Register File with 3-State Output	**M74LS670P**	150	12	13	16P4	74LS670	2-449
4-Bit D-Type Register with 3-State Output	**M74LS173AP**	85	—	—	16P4	74LS173A	2-210

Refer to LATCH and REGISTER sections for M74LS173AP specifications.

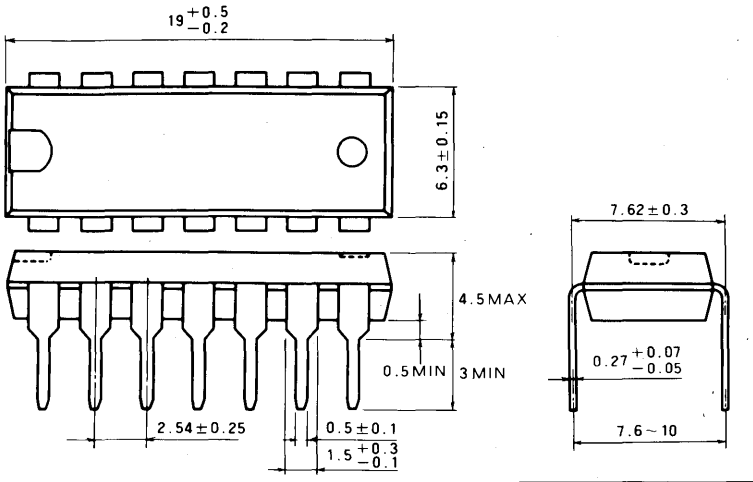
SYMBOLOGY

Symbol	Descriptions	
C_L	Load capacitance	Extenally connected load capacitance
f_{max}	Maximum clock frequency	Maximum input repetition frequency for normal IC operation.
F_I	Fan-in	Number of similar inputs
F_O	Fan-out	Number of similar ICs which can be driven by an output
H	Indicates the high logic level	Used in voltage and current suffixes to indicate the high potential level
I	Indicates current or input	Currents flowing into ICs are taken to be positive and those flowing out as negative
I_{CC}	Supply current	The current flowing into the V_{CC} supply terminal of a circuit
I_{CCL}	Low-level supply current	V_{CC} current when the inputs are such that the output is low.
I_{CCH}	High-level supply current	V_{CC} current when the inputs are such that the output is high.
I_{CCZ}	High-impedance supply current	V_{CC} current when the inputs are such that the output is in the high-impedance state.
I_F	Forward current	Forward diode current
I_I	Input current	Input current flowing into the IC pin when a voltage is applied.
I_{IH}	High-level input current	The current flowing into an input when a specified high voltage is applied.
I_{IL}	Low-level input current	The current flowing out of an input when a specified low voltage is applied.
I_{OH}	High-level output current	Current flowing in the load when the output is high or current flowing when a high level is applied
I_{OL}	Low-level output current	The current flowing into an output which is in the low state
I_{OS}	Short-circuit output current	The current flowing out of an output which is in the high state when that output is short circuit to ground.
I_{OZH}	Off-state high-level output current	The current flowing into a disabled 3-state output with a specified high output voltage applied
I_{OZL}	Off-state low-level output current	The current flowing out of a disabled 3-state output with a specified low output voltage applied
I_T	Threshold current	Current which flows when the threshold voltage is applied to the input
I_{T+}	Positive threshold current	Current which flows when the positive threshold voltage is applied to the input
I_{T-}	Negative threshold current	Current which flows when the negative threshold voltage is applied to the input
L	Indicates the low logic level	Used in voltage and current suffixes to indicate the low potential level
O	Indicates output	
Pd	Power dissipation	Product of the supply voltage and the supply current
PRR	Pulse repetition rate	The rate of repetition of an applied pulse train
Ta	Operating free-air temperature	The temperature of the environment surrounding an IC
t_f	Falltime	Time required to fall from the high to the low logic level
t_h	Hold time	The required hold time for a specified input after an input has changed
t_{latch}	Latch time	The time from the latching action of input data until the data appears in the output
Topr	Operating temperature	The ambient temperature range for normal IC operation
t_{pd}	Propagation delay time	Amount of time required from a change of input signal until the corresponding change in output, expressed as the average propagation time.
t_{PHL}	Propagation delay time, high-to-low-level output	Amount of time required from a change of input signal until the output changes from high to low.
t_{PHZ}	Output disable time from High level	Amount of time required from a change of input signal until the output changes from high to high-impedance.
t_{PLH}	Propagation delay time, low-to-high-level output	Amount of time required from a change of input signal until the output changes from low to high.
t_{PLZ}	Output disable time from Low level	Amount of time required from a change of input signal until the output changes from low to high-impedance.
t_W	Pulse width	The time required for a pulse to change from one specified level to another.
t_{WQ}	Output pulse width	The width of the pulse appearing in the output of a monostable multivibrator
t_{PZH}	Output enable time to a High level	Amount of time required from a change of input signal until the output changes from high-impedance to high.
t_{PZL}	Output enable time to a Low level	Amount of time required from a change of input signal until the output changes from high-impedance to low.
tr	Risetime	Time required to rise from the low to the high logic level
trec	Recovery time	Time from the point at which the input states are cancelled until the next clock pulse may be applied.
Tstg	Storage temperature	The range of surrounding storage temperature for an IC.
t_{SU}	Setup time	The required hold time for other inputs before a particular input may be changed.
V_{CC}	Supply voltage	The voltage of power supply voltage over which the device is guaranteed to operate within the specified limits.

Symbol	Descriptions	
V_{BE}	Base-emitter voltage	
V_F	Forward voltage	Forward voltage applied to a diode
V_I	Input voltage	Voltage applied to an input
V_{IC}	Input clamp diode voltage	The forward voltage applied to an input clamping diode.
V_{IE}	Input emitter-emitter voltage	The emitter-to-emitter voltage for a multi-emitter transistor input.
V_{IH}	High-level input voltage	The range of input voltages that represents a logic high in the system.
V_{IL}	Low-level input voltage	The range of input voltages that represents a logic low in the system.
V_O	Output voltage	Voltage applied to or appearing at an output
V_{OH}	High-level output voltage	Voltage at an output in the high state
V_{OL}	Low-level output voltage	Voltage at an output in the low state
V_P	Pulse amplitude	The difference between the low level and high level of a pulse.
V_T	Threshold voltage	The input voltage beyond at which the output changes
V_{T+}	Positive-going threshold voltage	The threshold voltage at which the output changes when the input is changing from low to high.
V_{T-}	Negative-going threshold voltage	The threshold voltage at which the output changes when the input is changing from high to low.
Z	Indicates the off-state	Indicates that the output is in the high-impedance state.
Z_O	Output impedance	The load impedance which should be connected to such devices as pulse generators.

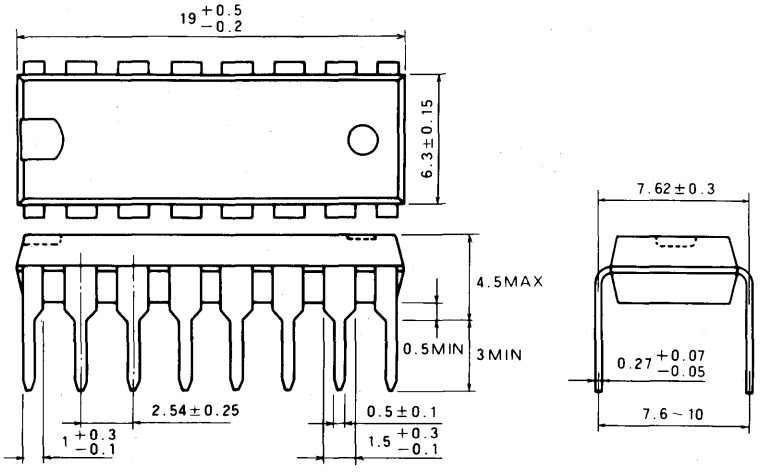
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



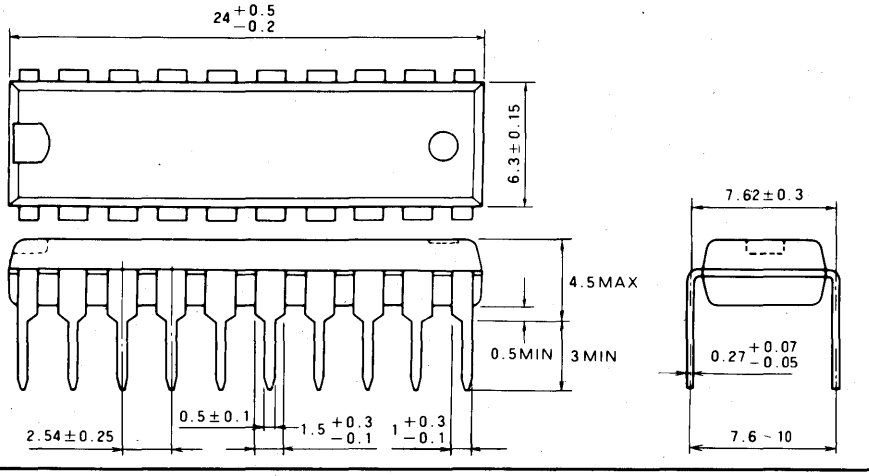
TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm



DATA SHEETS

SCHEMATICS OF INPUTS AND OUTPUTS

INDIVIDUAL DATA

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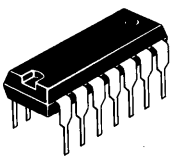
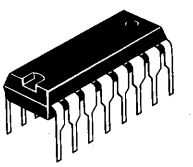
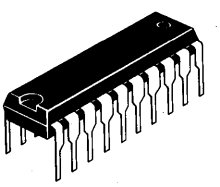






SCHEMATICS OF INPUTS AND OUTPUTS

Schematics of inputs and outputs of the M74LS00P series are shown in I-1 ~ I-11 and in 0-1 ~ 0-17, respectively, for devices whose circuit diagrams are not given in the individual data. Reference should be made when circuitry is being designed.

SCHEMATICS OF INPUTS AND OUTPUTS

Type designation	Schematics of inputs			Schematics of outputs		
	Fig.	R (Ω)	Pin	Fig.	R (equivalent resistance) Ω	
M74LS42P	I-1	17k	All inputs	0-1	120	
M74LS47P	I-1	25k	D_A~D_D	0-2	—	
	I-1	20k	$\overline{LT}$, $\overline{RBI}$			
	I-2	R_{IN}=10k	$\overline{BI}/\overline{RBO}$	I-2	R_{OUT}=20k	$\overline{BI}/\overline{RBO}$
M74LS48P	I-1	25k	D_A~D_D	0-3	2k	
	I-1	20k	$\overline{LT}$, $\overline{RBI}$			
	I-2	R_{IN}=10k	$\overline{BI}/\overline{RBO}$	I-2	R_{OUT}=20k	$\overline{BI}/\overline{RBO}$
M74LS73AP	I-1	26k	J, K	0-14	120	
	I-1	9k	$\overline{T}$			
	I-3	9k	$\overline{R_D}$			
M74LS74AP	I-3	8k	$\overline{S_D}$, $\overline{R_D}$	0-14	120	
	I-4	18k	T			
	I-5	31k	D			
M74LS75P	I-1	18k	D	0-15	120	
	I-1	4.5k	E			
M74LS76AP	I-1	26k	J, K	0-14	120	
	I-1	9k	$\overline{T}$			
	I-3	9k	$\overline{S_D}$, $\overline{R_D}$			
M74LS83AP	I-1	18k	C_0	0-1	120	
	I-1	9k	A_1~A_4, B_1~B_4			
M74LS85P	I-6	17k	$I_{A<B}$, $I_{A>B}$	0-1	120	
	I-7	R_1=15k, R_2=8.5k	$I_{A=B}$			
	I-7	R_1=8.5k, R_2=17k	A_0~A_3, B_0~B_3			
M74LS90P	I-1	17k	$S_{D(9)1}$, $S_{D(9)2}$, R_{D1}, R_{D2}	0-13	R=120, R_1=17k R_2=17k, R_3=9k	Q_B
	I-8	R_1=8.5k, R_2=8.5k, R_3=8.5k	$\overline{T_1}$			
	I-8	R_1=5.8k, R_2=5.8k, R_3=4.4k	$\overline{T_2}$	0-15	120	Q_A, Q_C, Q_D
M74LS91P	I-1	26k	D_{S1}, D_{S2}	0-15	120	
	I-1	19k	T			
M74LS92P	I-1	17k	R_{D1}, R_{D2}	0-13	R=120, R_1=17k R_2=17k, R_3=9k	Q_C
	I-8	R_1=8.5k, R_2=8.5k, R_3=8.5k	$\overline{T_1}$			
	I-8	R_1=5.8k, R_2=5.8k, R_3=4.4k	$\overline{T_2}$	0-15	120	Q_A, Q_B, Q_D
M74LS93P	I-1	17k	R_{D1}, R_{D2}	0-15	120	Q_A, Q_D
	I-8	R_1=8.5k, R_2=8.5k R_3=8.5k	$\overline{T_1}$	0-13	R=120, R_1=17k R_2=17k, R_3=9k	Q_B
	I-8	R_1=13k, R_2=13k R_3=9k	$\overline{T_2}$		R=120, R_1=10k R_2=10k, R_3=9k	Q_C
M74LS95BP	I-1	17k	$\overline{T_R}$, $\overline{T_L}$	0-15	120	
	I-1	9k	M/C			
	I-1	20k	D_S, D_0~D_3			

Note: All resistances given are typical values.

SCHEMATICS OF INPUTS AND OUTPUTS

Type designation	Schematics of inputs			Schematics of outputs	
	Fig.	R (Ω)	Pin	Fig.	R (equivalent resistance) Ω
M74LS96P	I-1	26k	D_S	0-15	120
	I-1	18k	$\overline{R_D}$, T, S_{D0}~S_{D4}		
	I-1	3.4k	LOAD		
M74LS107AP	I-1	26k	J, K	0-14	120
	I-1	9k	$\overline{T}$		
	I-3	9k	$\overline{R_D}$		
M74LS109AP	I-3	8k	$\overline{S_D}$, $\overline{R_D}$	0-14	120
	I-4	18k	T		
	I-5	31k	J, $\overline{K}$		
M74LS112AP	I-1	24k	J, K	0-14	120
	I-1	9k	$\overline{T}$		
	I-3	9k	$\overline{S_D}$, $\overline{R_D}$		
M74LS113AP	I-1	24k	J, K	0-14	120
	I-1	9k	$\overline{T}$		
	I-3	9k	$\overline{S_D}$		
M74LS114AP	I-1	24k	J, K	0-14	120
	I-1	4.8k	$\overline{T}$		
	I-3	9k	$\overline{S_D}$		
	I-3	4.5k	$\overline{R_D}$		
M74LS122P	I-1	17k	All inputs	0-1	120
M74LS123P	I-1	17k	All inputs	0-1	120
M74LS137P	I-9	15k	D_0~D_3	0-5	120
	I-1	20k	E_1, $\overline{E_2}$, $\overline{E_L}$		
M74LS138P	I-9	10k	D_0~D_3	0-5	120
	I-1	20k	E_1, $\overline{E_2}$, $\overline{E_3}$	0-5	120
M74LS139P	I-1	17k	All inputs	0-1	120
M74LS145P	I-1	17k	All inputs	0-6	—
M74LS147P	I-1	17k	All inputs	0-5	120
M74LS148P	I-1	17k	$\overline{D_0}$, $\overline{E}$	0-5	120
	I-1	9k	$\overline{D_1}$~$\overline{D_7}$		
M74LS151P	I-1	17k	All inputs	0-1	120
M74LS153P	I-1	17k	All inputs	0-1	120
M74LS155P	I-1	17k	All inputs	0-1	120
M74LS156P	I-1	17k	All inputs	0-7	—
M74LS157P	I-1	17k	$1D_0$~$4D_0$, $1D_1$~$4D_1$	0-1	120
	I-1	8.5k	S_A, $\overline{G}$		
M74LS158P	I-1	17k	$1D_0$~$4D_0$, $1D_1$~$4D_1$	0-1	120
	I-1	8.5k	S_A, $\overline{G}$		
M74LS160AP	I-1	20k	D_A~D_D, T, E_P, $\overline{R_D}$	0-15	120
	I-1	9k	E_T, $\overline{LOAD}$		
M74LS161AP	I-1	20k	D_A~D_D, T, E_P, $\overline{R_D}$	0-15	120
	I-1	9k	E_T, $\overline{LOAD}$		
M74LS162AP	I-1	20k	D_A~D_D, T, E_P	0-15	120
	I-1	9k	E_T, $\overline{R}$, $\overline{LOAD}$		
M74LS163AP	I-1	20k	D_A~D_D, T, E_P	0-15	120
	I-1	9k	E_T, $\overline{R}$, $\overline{LOAD}$		

SCHEMATICS OF INPUTS AND OUTPUTS

Type designation	Schematics of inputs			Schematics of outputs		
	Fig.	R (Ω)	Pin	Fig.	R (equivalent resistance) Ω	
M74LS164P	I-1	20k	All inputs	0-15	120	
M74LS165AP	I-9	9k	T, T_{INH}, $\overline{LOAD}$	0-8	120	
	I-1	18k	D_0~D_7			
	I-1	22k	D_S			
M74LS166AP	I-9	9k	$\overline{R_D}$, $\overline{LOAD}$, T, T_{INH}	0-8	120	
	I-1	18k	D_0~D_7			
	I-9	12k	$\overline{LOAD}$	0-8	120	
	I-1	22k	D_S			
M74LS170P	I-1	8.5k	$\overline{E_R}$, $\overline{E_W}$	0-2	—	
	I-1	17k	D_0~D_3, R_A, R_B, W_A, W_B			
M74LS173AP	I-1	19k	All inputs	0-9	100	
M74LS174P	I-1	17k	T, $\overline{R_D}$	0-15	120	
	I-1	30k	D_0~D_5			
M74LS175P	I-1	17k	T, $\overline{R_D}$	0-15	120	
	I-1	30k	D_0~D_3			
M74LS190P	I-1	5.7k	$\overline{E}$	0-15	120	
	I-1	17k	All inputs except $\overline{E}$			
M74LS191P	I-1	5.7k	$\overline{E}$	0-15	120	
	I-1	17k	All inputs except $\overline{E}$			
M74LS192P	I-1	23k	D_A~D_D	0-15	120	
	I-1	17k	T_U, T_D, R_D, $\overline{LOAD}$			
M74LS193P	I-1	23k	D_A~D_D	0-15	120	
	I-1	17k	T_U, T_D, R_D, $\overline{LOAD}$			
M74LS194AP	I-1	25k	D_{SR}, D_{SL}, D_0~D_3	0-15	120	
	I-1	17k	T, $\overline{R_D}$, M/C_1, M/C_2			
M74LS195AP	I-1	20k	J, $\overline{K}$, D_0~D_3, M/C	0-15	120	
	I-1	17k	T, $\overline{R_D}$			
M74LS196P	I-1	17k	D_A~D_D, $\overline{LOAD}$	0-15	120	
	I-1	8.5k	$\overline{R_D}$			
	I-8	R_1=5.7k, R_2=6.5k, R_3=7k	$\overline{T_1}$			
	I-8	R_1=5.7k, R_2=5.7k, R_3=5.7k	$\overline{T_2}$			
M74LS197P	I-1	17k	D_A~D_D, $\overline{LOAD}$	0-15	120	
	I-1	8.5k	$\overline{R_D}$			
	I-8	R_1=5.7k, R_2=6.5k, R_3=7k	$\overline{T_1}$			
	I-8	R_1=14k, R_2=13k, R_3=13k	$\overline{T_2}$			
M74LS221P	I-1	24k	$\overline{A}$	0-1	120	
	I-11	R_1=45k, R_2=24k, R_3=9.5k R_4=14k, R_5=1.7k	B			
	I-10	R_1=12k, R_2=9.5k R_3=14k, R_4=1.7k	$\overline{R_D}$			
M74LS247P	I-1	25k	D_A~D_D	0-2	—	
	I-1	20k	$\overline{LT}$, $\overline{RBI}$			
	I-2	R_{IN}=10k	$\overline{BI}/\overline{RBO}$	I-2	R_{OUT}=20k	$\overline{BI}/\overline{RBO}$
M74LS248P	I-1	25k	D_A~D_D	0-3	2k	
	I-1	20k	$\overline{LT}$, $\overline{RBI}$			
	I-2	R_{IN}=10k	$\overline{BI}/\overline{RBO}$	I-2	R_{OUT}=20k	$\overline{BI}/\overline{RBO}$

SCHEMATICS OF INPUTS AND OUTPUTS

Type designation	Schematics of inputs			Schematics of outputs		
	Fig.	R (Ω)	Pin	Fig.	R (equivalent resistance) Ω	
M74LS251P	I-1	17k	All inputs	O-11	100	
M74LS253P	I-1	19k	S_A, S_B, $1\overline{OC}$, $2\overline{OC}$	O-4	100	
	I-1	17k	$1D_0$~$1D_3$, $2D_0$~$2D_3$	O-12	100	
M74LS256P	I-1	17k	S_A, S_B, 1D, 2D, $\overline{R}$	O-16	120	
	I-9	9.5k	M/C			
M74LS257AP	I-1	8.5k	S_A	O-9	100	
	I-1	17k	$\overline{OC}$, $1D_0$~$4D_0$, $1D_1$~$4D_1$			
M74LS258AP	I-1	8.5k	S_A	O-9	100	
	I-1	17k	$\overline{OC}$, $1D_0$~$4D_0$, $1D_1$~$4D_1$			
M74LS259P	I-1	17k	S_A~S_C, D, $\overline{R}$	O-16	120	
	I-9	9.5k	M/C			
M74LS273P	I-1	17k	T, $\overline{R_D}$	O-15	120	
	I-5	28k	1D~8D			
M74LS280P	I-1	20k	All inputs	O-1	120	
M74LS283P	I-1	18k	C_0	O-1	120	
	I-1	9k	A_1~A_4, B_1~B_4			
M74LS290P	I-1	17k	$S_{D(9)1}$, $S_{D(9)2}$ R_{D1}, R_{D2}	O-13	R=120, R_1=17k R_2=17k, R_3=9k	Q_B
	I-8	R_1=8.5k, R_2=8.5k, R_3=8.5k	$\overline{T_1}$			
	I-8	R_1=5.8k, R_2=5.8k, R_3=4.4k	$\overline{T_2}$	O-15	120	Q_A, Q_C, Q_D
M74LS293P	I-1	17k	R_{D1}, R_{D2}	O-15	120	Q_A, Q_D
	I-8	R_1=8.5k, R_2=8.5k R_3=8.5k	$\overline{T_1}$	O-13	R=120, R_1=17k R_2=17k, R_3=9k	Q_B
	I-8	R_1=13k, R_2=13k R_3=9k	$\overline{T_2}$		R=120, R_1=10k R_2=10k, R_3=9k	Q_C
M74LS295BP	I-1	18k	$\overline{T}$	O-9	100	
	I-1	20k	OC, M/C			
	I-5	30k	D_S			
	I-5	20k	D_0~D_3			
M74LS298P	I-1	17k	$\overline{T}$	O-15	120	
	I-1	20k	S_A, $1D_0$~$4D_0$, $1D_1$~$4D_1$			
M74LS299P	I-1	10k	M/C_1, M/C_2	O-9	100	Q_0~Q_7
	I-1	20k	$\overline{OC_1}$, $\overline{OC_2}$, $\overline{R_D}$, T			
	I-5	20k	D_{SR}, D_{SL}, D_0~D_7	O-1	120	Q'_0, Q'_7
M74LS323P	I-1	10k	M/C_1, M/C_2	O-9	100	Q_0~Q_7
	I-1	20k	$\overline{OC_1}$, $\overline{OC_2}$, $\overline{R_D}$, T			
	I-5	20k	D_{SR}, D_{SL}, D_0~D_7	O-1	120	Q'_0, Q'_7
M74LS352P	I-1	19k	S_A, S_B, $\overline{1G}$, $\overline{2G}$	O-1	120	
	I-1	17k	$1D_0$~$1D_3$, $2D_0$~$2D_3$			
M74LS353P	I-1	19k	S_A, S_B, $1\overline{OC}$, $2\overline{OC}$	O-12	100	
	I-1	17k	$1D_0$~$1D_3$, $2D_0$~$2D_3$			
M74LS373P	I-1	17k	1D~8D	O-9	100	
	I-9	9k	E, $\overline{OC}$			
M74LS374P	I-1	30k	1D~8D	O-9	100	
	I-9	9k	T, $\overline{OC}$			

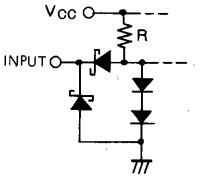
SCHEMATICS OF INPUTS AND OUTPUTS

Type designation	Schematics of inputs			Schematics of outputs		
	Fig.	R (Ω)	Pin	Fig.	R (equivalent resistance) Ω	
M74LS375P	I-1	18k	1D～4D	0-15	120	
	I-1	4.5k	1-2E, 3-4E			
M74LS377P	I-1	17k	$\overline{E}$, $\overline{E}$	0-15	120	
	I-5	28k	1D～8D			
M74LS390	I-1	17k	R_D	0-17	120	
	I-8	R_1=14k, R_2=14k, R_3=14k	$\overline{T_1}$			
	I-8	R_1=8.5k, R_2=8.5k, R_3=8k	$\overline{T_2}$			
M74LS393P	I-1	17k	R_D	0-17	120	
	I-8	R_1=14k, R_2=14k, R_3=14k	$\overline{T}$			
M74LS395AP	I-1	18k	$\overline{T}$	0-9	100	Q_0～Q_3
	I-1	20k	$\overline{OC}$, M/C, $\overline{R_D}$			
	I-5	30k	D_S			
	I-5	20k	D_0～D_3	0-17	120	Q'_3
M74LS423P	I-1	17k	All inputs	0-1	120	
M74LS490P	I-1	17k	$S_{D(9)}$, R_D	0-17	120	
	I-8	R_1=14k, R_2=14k, R_3=14k	$\overline{T}$			
M74LS595P	I-1	19k	D_S	0-9	Q_0～Q_7	
	I-9	13k	その他	0-8	Q_7'	
M74LS596P	I-1	19k	D_S	0-2	Q_0～Q_7	
	I-9	13k	その他	0-8	Q_7'	
M74LS668P	I-1	8.5k	$\overline{LOAD}$	0-15	120	Q_A, Q_B Q_C, Q_D
	I-1	17k	U/$\overline{D}$, T, $\overline{EP}$, $\overline{ET}$			
	I-5	20k	D_A～D_D	0-1	120	RCO
M74LS669P	I-1	8.5k	$\overline{LOAD}$	0-15	120	Q_A, Q_B, Q_C, Q_D
	I-1	17k	U/$\overline{D}$, T, $\overline{EP}$, $\overline{ET}$			
	I-5	20k	D_A～D_D	0-1	120	RCO
M74LS670P	I-1	8.5k	$\overline{Ew}$	0-10	120	
	I-7	R_1=8.5k, R_2=17k	$\overline{OC}$			
	I-1	17k	R_A, R_B, W_A, W_B, D_0～D_3			
M74LS682P	I-9	14k	P_0～P_7	0-5	100	
	I-12	R_1=14k, R_2=24k	Q_0～Q_7			
M74LS683P	I-9	14k	P_0～P_7	0-7	—	
	I-12	R_1=14k, R_2=24k	Q_0～Q_7			
M74LS684P	I-9	14k	全入力	0-5	100	
M74LS685P	I-9	14k	全入力	0-7	—	
M74LS688P	I-9	14k	全入力	0-5	100	
M74LS689P	I-9	14k	全入力	0-7	—	

SCHEMATICS OF INPUTS AND OUTPUTS

Schematics of inputs

I-1



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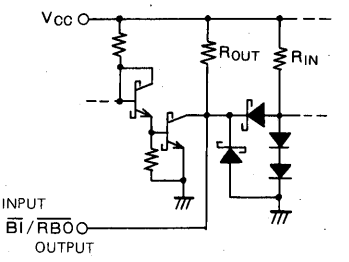

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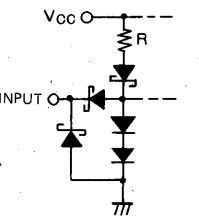

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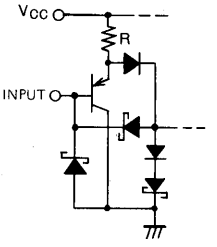

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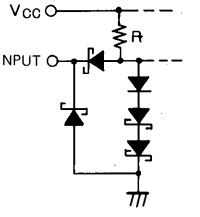

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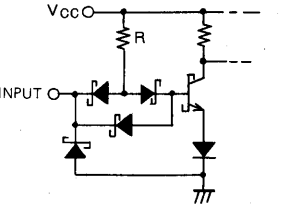

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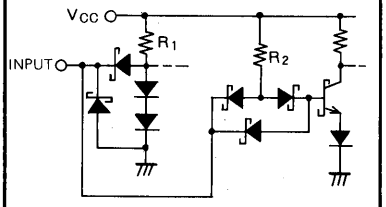

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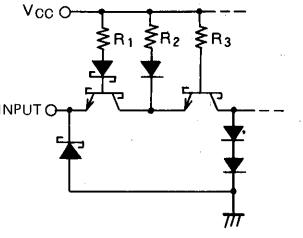

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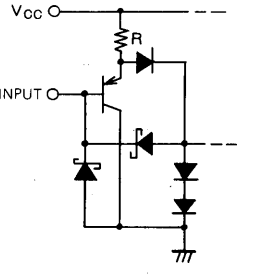

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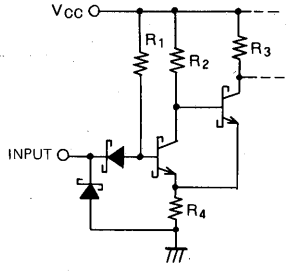

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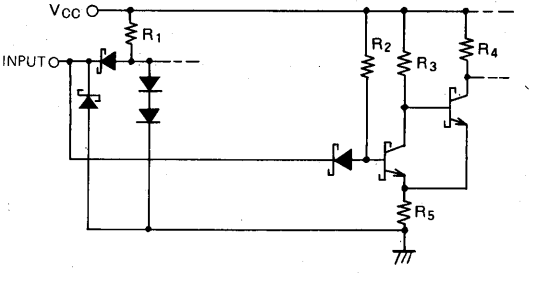
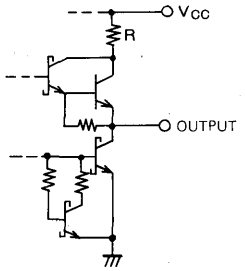


SCHEMATICS OF INPUTS AND OUTPUTS

Schematics of outputs

0-1



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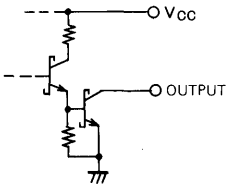

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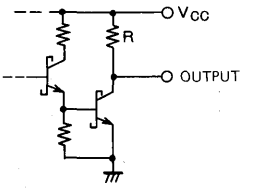

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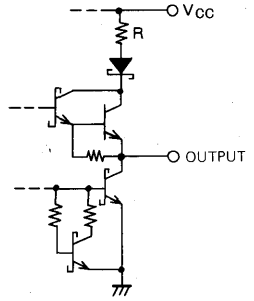

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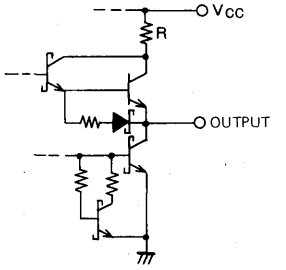

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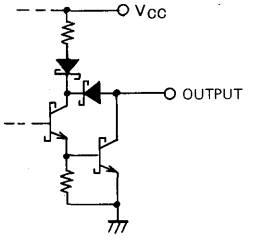

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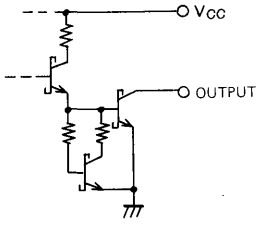

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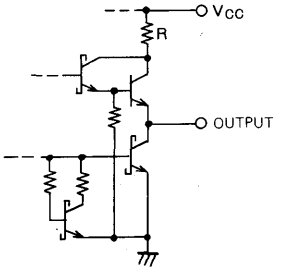

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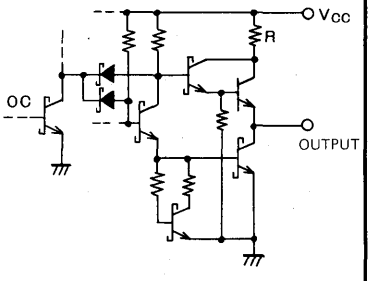

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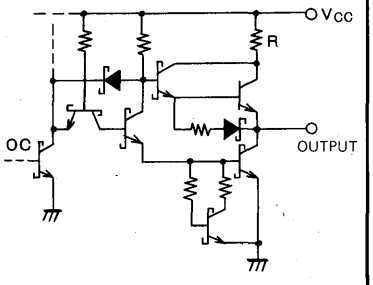

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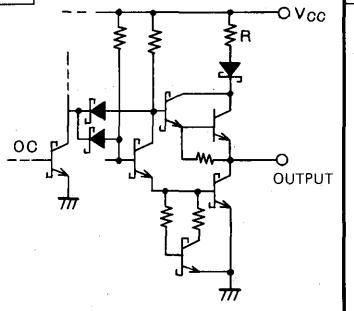

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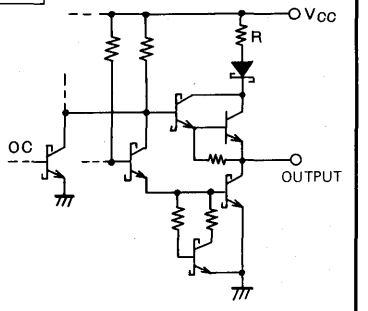
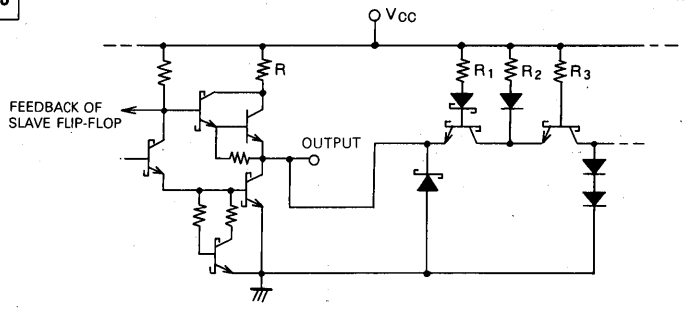


SCHEMATICS OF INPUTS AND OUTPUTS

0-13



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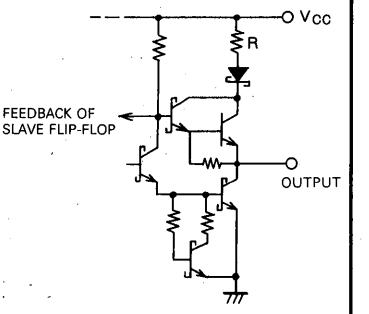

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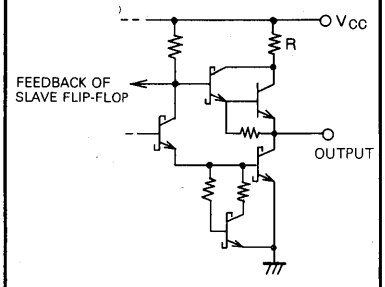

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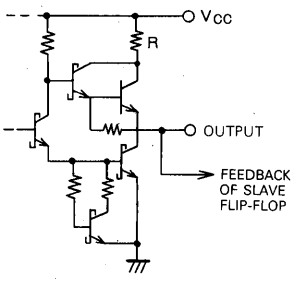

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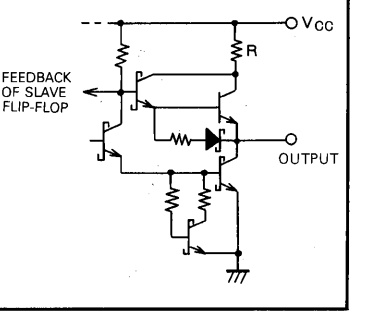


M74LS00P

QUADRUPLE 2-INPUT POSITIVE NAND GATES

DESCRIPTION

The M74LS00P is semiconductor integrated circuit containing four dual-input positive-logic NAND gates, usable as negative-logic NOR gates.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 8mW typical)
- High speed (t_{pd} = 6ns typical)
- Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATIONS

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

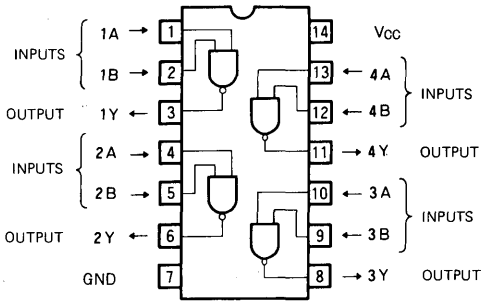
The use of Schottky TTL technology enables the achievement of input high breakdown voltage, high speed, and low power consumption as well as high fan-out.

When both A and B inputs are high the output Y is low. When either A or B input is low the output Y is high.

FUNCTION TABLE

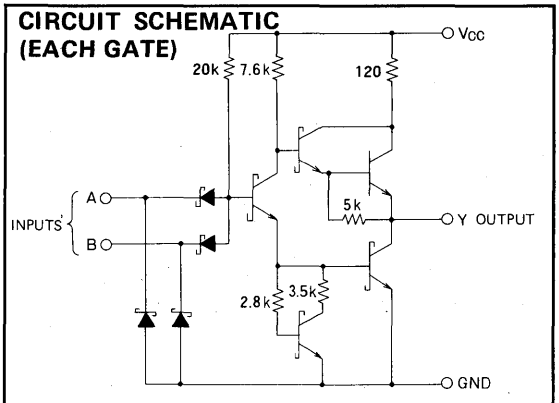
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	℃
T_{stg}	Storage temperature range		−65 ~ +150	℃

QUADRUPLE 2-INPUT POSITIVE NAND GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

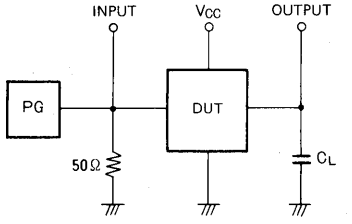
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$, $V_I = 0.8V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$, $V_I = 2V$	$I_{OL} = 4mA$		0.25	0.4	V
			$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC} = 5.25V$, $V_O = 0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC} = 5.25V$, $V_I = 0V$			0.8	1.6	mA
I_{CCL}	Supply current, all outputs low	$V_{CC} = 5.25V$, $V_I = 4.5V$			2.4	4.4	mA

* : All typical values are at $V_{CC} = 5V$, $Ta = 25°C$.
Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25°C$, unless otherwise noted)

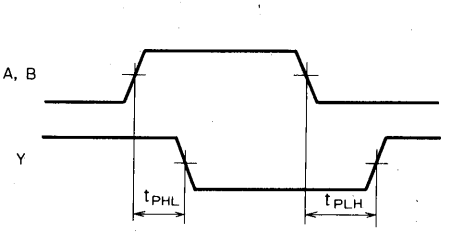
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	$C_L = 15pF$ (Note 2)		6	15	ns
t_{PHL}	High-to-low-level output propagation time			6	15	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS02P

QUADRUPLE 2-INPUT POSITIVE NOR GATES

DESCRIPTION

The M74LS02P is a semiconductor integrated circuit containing 4 dual-input positive NOR and negative NAND gates.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 10mW typical)
- High speed (t_{pd} = 6ns typical)
- Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

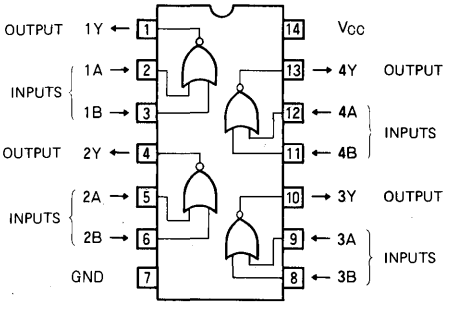
The use of Schottky TTL technology, enables the achievement of high input voltage, high speed, low power dissipation, and high fan-out.

When at least input A or input B is high, output Y is low, and when both A and B are low, Y is high.

FUNCTION TABLE

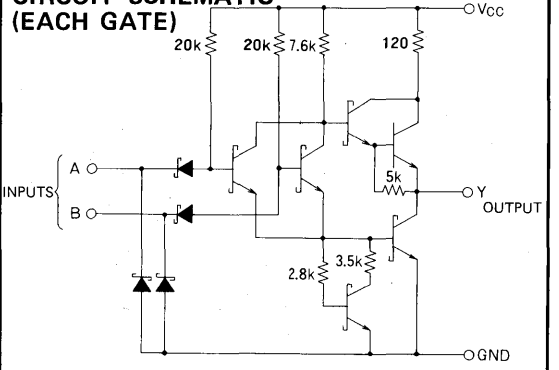
A	B	Y
L	L	H
H	L	L
L	H	L
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

QUADRUPLE 2-INPUT POSITIVE NOR GATES

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

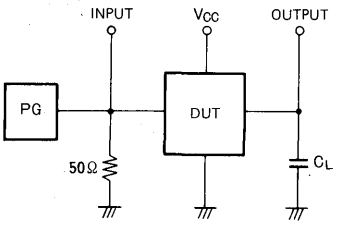
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
		V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.25V, V_I=0V			1.6	3.2	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.25V, V_I=4.5V			2.8	5.4	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

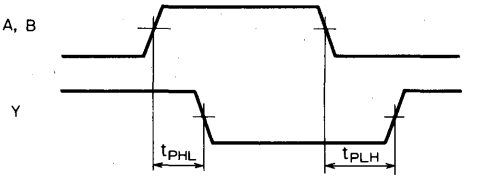
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	C_L=15pF		6	15	ns
t_{PHL}	High-to-low-level output propagation time	(Note 2)		6	15	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P\text{-}P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS03P

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS03P is a semiconductor integrated circuit containing four dual-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

FEATURES

- Usable in AND-Tie connection
- High breakdown input voltage ($V_I \geqq 15V$)
- High breakdown output voltage ($V_O \geqq 7V$)
- Low power dissipation (P_d = 8mW typical)
- High speed (t_{pd} = 10ns typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

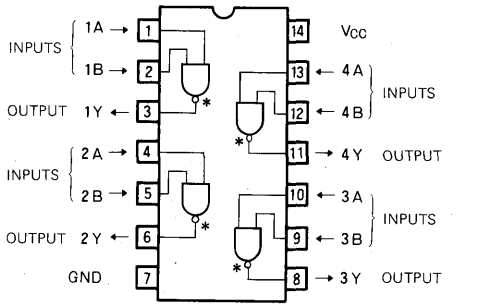
With use of open collector outputs and SBD inputs featuring a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

When inputs A and B are high, output Y is low and when one or both inputs are low, the output Y is high.

FUNCTION TABLE

A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

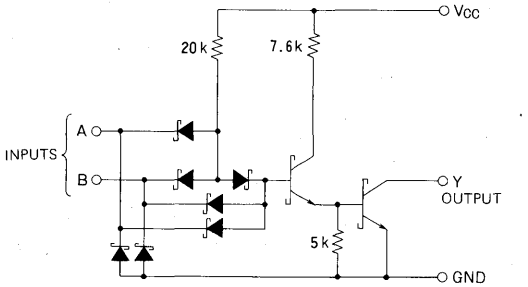
PIN CONFIGURATION (TOP VIEW)



* : OPEN COLLECTOR OUTPUT

Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

QUADRUPLE 2-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O = 5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL} ≦ 0.4V	0		4	mA
		V_{OL} ≦ 0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

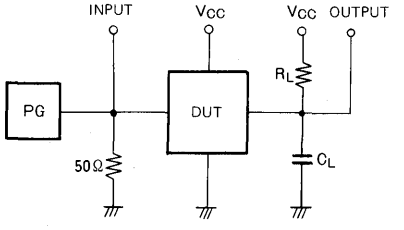
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75V, V_I = 0.8V, V_O = 5.5V				100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, V_I = 2V	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{CCH}	Supply current, all inputs high	V_{CC} = 5.25V, V_I = 0V			0.8	1.6	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = 5.25V, V_I = 4.5V			2.4	4.4	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

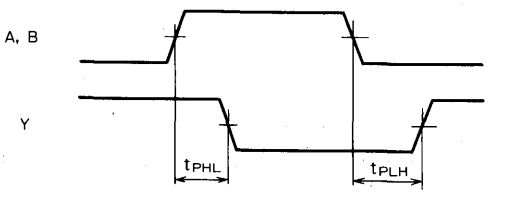
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level/high-to-low-level output propagation time	R_L = 2 kΩ, C_L = 15 pF (Note 1)		10	32	ns
t_{PHL}				10	28	ns

Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS04P

HEX INVERTERS

DESCRIPTION

The M74LS04P is a semiconductor integrated circuit containing 6 inverter circuits.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 12mW typical)
- High speed (t_{pd} = 6ns typical)
- Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

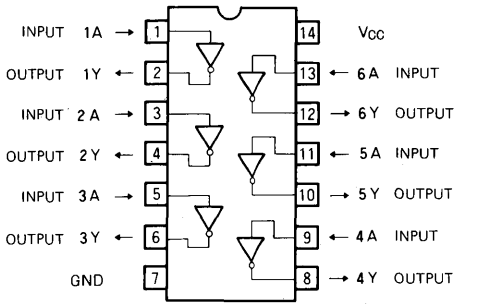
The use of Schottky TTL technology enables the achievement of high input voltage, high speed, low power dissipation and high fan-out.

When input A is high, output Y is low, and when A is low, Y is high.

FUNCTION TABLE

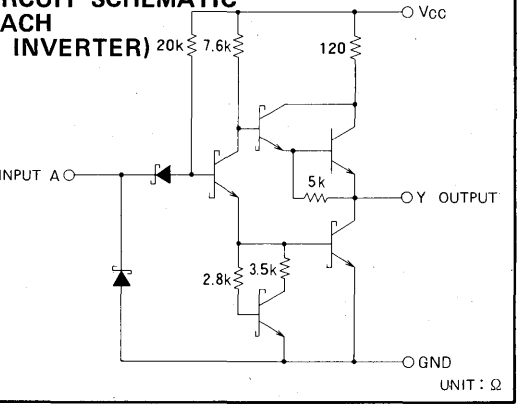
A	Y
L	H
H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH INVERTER)



ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=0V$			1.2	2.4	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=4.5V$			3.6	6.6	mA

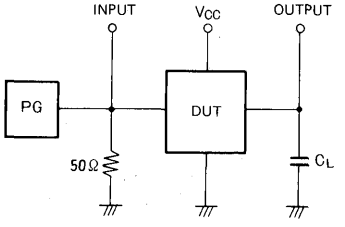
* : All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	High-to-low-level output propagation time	$C_L=15pF$ (Note 2)		6	15	ns
t_{PHL}	Low-to-high-level output propagation time			6	15	ns

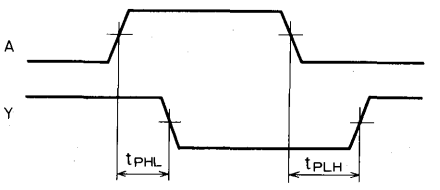
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



MITSUBISHI ELECTRIC

M74LS05P

HEX INVERTERS WITH OPEN COLLECTOR OUTPUTS

DESCRIPTION

The M74LS05P is a semiconductor integrated circuit containing 6 open collector output inverter circuits.

FEATURES

- Usable in AND-Tie connection.
- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 12mW typical)
- High speed (t_{pd} = 10ns typical)
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

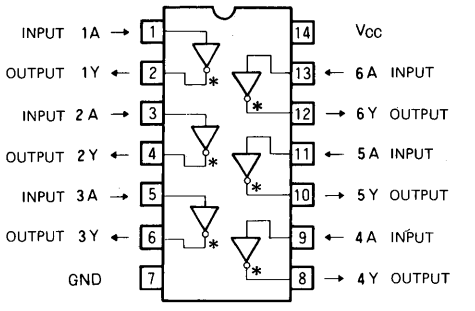
With the use of Schottky barrier diodes for the inputs and open-collector outputs, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection, which has been impossible with conventional gates.

When input A is high, output Y is low, and when A is low, Y is high.

FUNCTION TABLE

A	Y
L	H
H	L

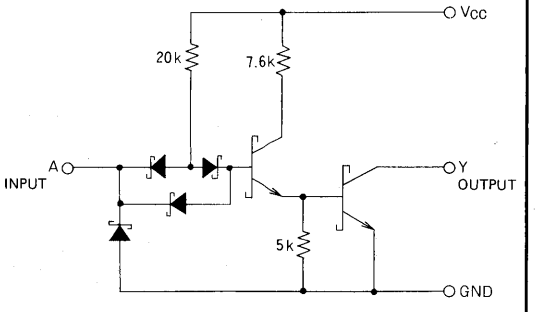
PIN CONFIGURATION (TOP VIEW)



*: OPEN COLLECTOR OUTPUT

Outline 14P4

CIRCUIT SCHEMATIC (EACH INVERTER)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

HEX INVERTERS WITH OPEN COLLECTOR OUTPUTS

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O = 5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL} ≦ 0.4V	0		4	mA
		V_{OL} ≦ 0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

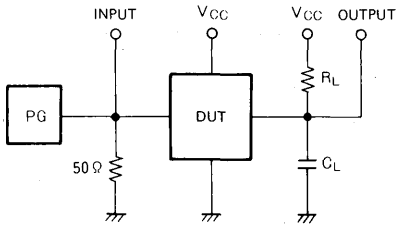
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75V, V_I = 0.8V, V_O = 5.5V				100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, V_I = 2V	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = 5.25V, V_I = 0V			1.2	2.4	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = 5.25V, V_I = open			3.6	6.6	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

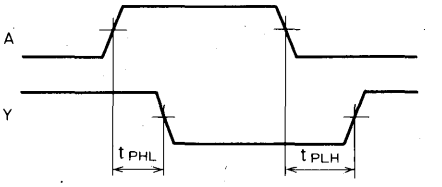
SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	R_L = 2 kΩ, C_L = 15pF (Note 1)		10	32	ns
t_{PHL}	High-to-low-level output propagation time			10	28	ns

Note 1: Measurement circuit



TIMING DIAGRAM (Reference level = 1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = 3V_{P-P}, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

M74LS08P

QUADRUPLE 2-INPUT POSITIVE AND GATES

DESCRIPTION

The M74LS08P is a semiconductor integrated circuit containing 4 dual input-positive AND and negative OR gates.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 17mW typical)
- High speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

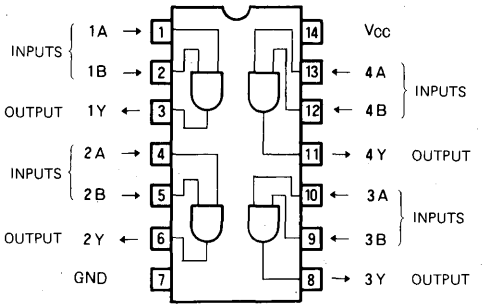
The use of Schottky TTL technology, enables the achievement of high input voltage, high speed, low power dissipation, and high fan-out.

When both inputs A and B are high, output Y is high, and when either or both of the inputs are low, Y is low.

FUNCTION TABLE

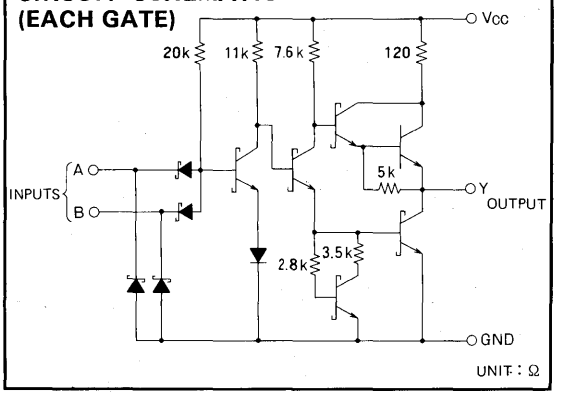
A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

QUADRUPLE 2-INPUT POSITIVE AND GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

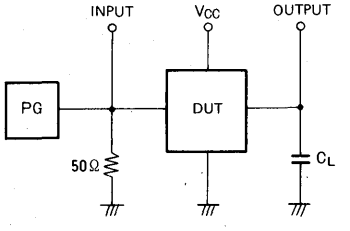
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=0.8V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=4.5V$			2.4	4.8	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=0V$			4.4	8.8	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 1: All measurement should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

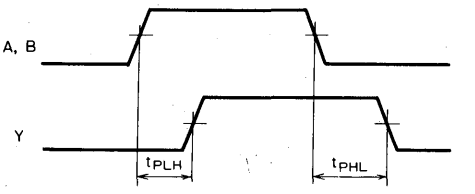
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	$C_L=15pF$		9	15	ns
t_{PHL}	High-to-low-level output propagation time	(Note 2)		10	20	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS09P

QUADRUPLE 2-INPUT POSITIVE AND GATES WITH OPEN COLLECTOR OUTPUTS

DESCRIPTION

The M74LS09P is a semiconductor integrated circuit containing 4 dual-input positive AND and negative OR gates with open collector output.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage ($V_I \geqq 15V$)
- High breakdown output voltage ($V_O \geqq 7V$)
- Low power consumption (P_d = 17mW typical)
- High speed (t_{pd} = 13ns typical)
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

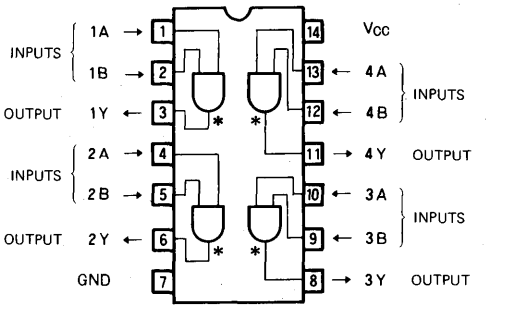
With the use of open collector output, the high-level output impedance can be freely selected by means of an external load resistor. This enables use in wire-AND, which has been impossible with conventional gates.

When both inputs A and B are high, output Y is high and when either or both of them are low, Y is low.

FUNCTION TABLE

A	B	Y
L	L	L
H	L	L
L	H	L
H	H	H

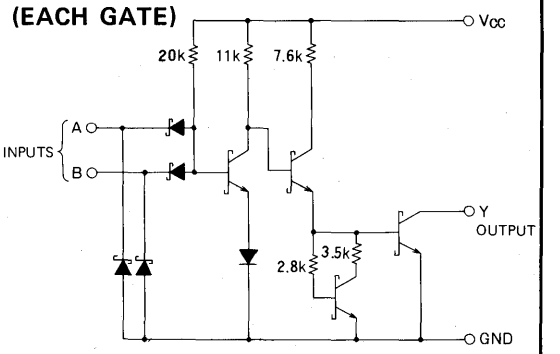
PIN CONFIGURATION (TOP VIEW)



*: OPEN COLLECTOR OUTPUT

Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

QUADRUPLE 2-INPUT POSITIVE AND GATES WITH OPEN COLLECTOR OUTPUTS

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_O = 5.5V$	0		100	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

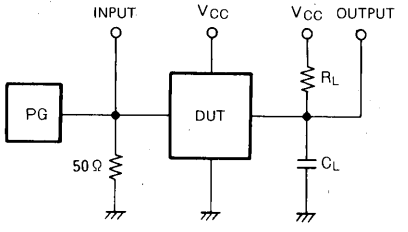
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$				−1.5	V
I_{OH}	High-level output current	$V_{CC} = 4.75V$, $V_I = 2V$, $V_O = 5.5V$				100	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$, $V_I = 0.8V$	$I_{OL} = 4mA$		0.25	0.4	V
			$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.4	mA
I_{CCH}	Supply current, all outputs high	$V_{CC} = 5.25V$, $V_I = 0V$			2.4	4.8	mA
I_{CCL}	Supply current, all outputs low	$V_{CC} = 5.25V$, $V_I = 4.5V$			4.4	8.8	mA

* : All typical values are at $V_{CC} = 5V$, $Ta = 25°C$.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	High-to-low-level output propagation time	$R_L = 2 k\Omega$, $C_L = 15pF$ (Note 1)		15	35	ns
t_{PHL}	Low-to-high-level output propagation time			10	35	ns

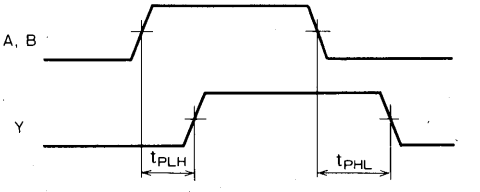
Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



MITSUBISHI ELECTRIC

M74LS10P

TRIPLE 3-INPUT POSITIVE NAND GATES

DESCRIPTION

The M74LS10P is a semiconductor integrated circuit containing three triple-input positive NAND and negative NOR gates.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 8mW typical)
- High speed (t_{pd} = 6ns typical)
- Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use Schottky TTL technology has enabled the achievement of high input voltage, high speed, low power dissipation and high fan-out.

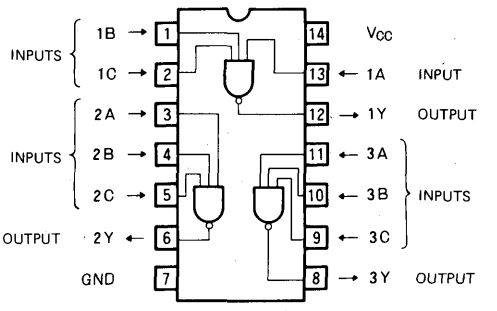
When all inputs A, B and C are high, output Y is low, and when one or more of the inputs is low, Y is high.

FUNCTION TABLE

A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

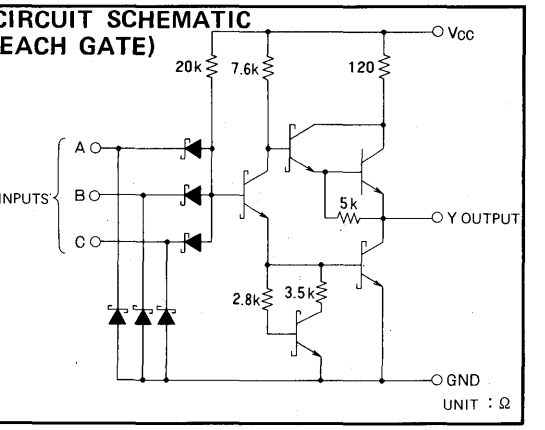
N=B・C

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

TRIPLE 3-INPUT POSITIVE NAND GATES

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$, $V_I = 0.8V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$	$I_{OL} = 4mA$		0.25	0.4	V
		$V_I = 2V$	$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC} = 5.25V$, $V_O = 0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC} = 5.25V$, $V_I = 0V$			0.6	1.2	mA
I_{CCL}	Supply current, all outputs low	$V_{CC} = 5.25V$, $V_I = 4.5V$			1.8	3.3	mA

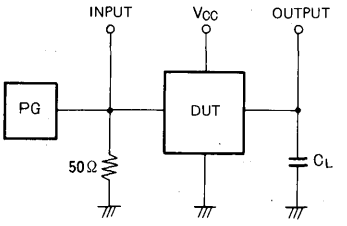
* : All typical values are at $V_{CC} = 5V$, $T_a = 25°C$.

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	$C_L = 15pF$ (Note 2)		6	15	ns
t_{PHL}	High-to-low-level output propagation time			9	15	ns

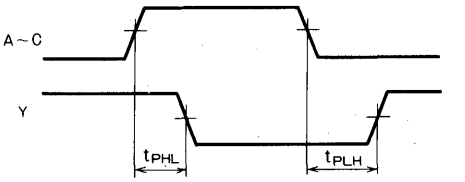
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



MITSUBISHI ELECTRIC

M74LS11P

TRIPLE 3-INPUT POSITIVE AND GATE

DESCRIPTION

The M74LS11P is a semiconductor integrated circuit containing three triple-input positive AND and negative OR gates.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 13mW typical)
- High speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of Schottky TTL technology and active output pullups enables the achievement of input high breakdown voltage, high speed, lower power dissipation and high fan-out.

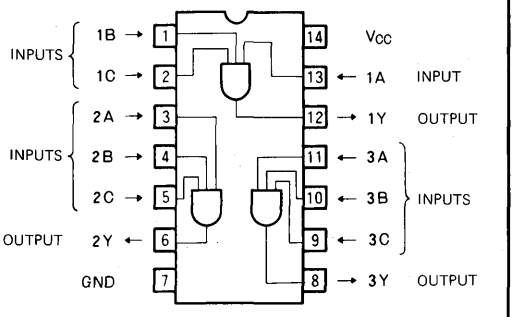
When inputs A, B and C are high, output Y is high and when one or more of the inputs is low, Y is low.

FUNCTION TABLE

A	N	Y
L	L	L
H	L	L
L	H	L
H	H	H

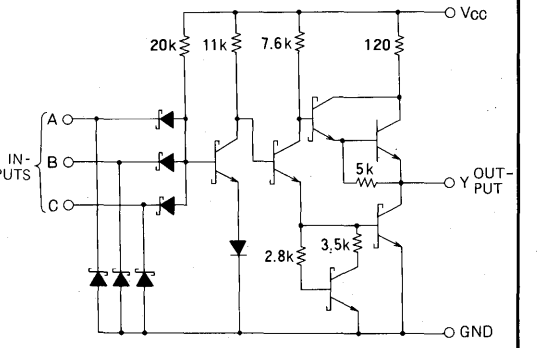
N=B·C

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=0.8V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=4.5V$			1.8	3.6	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=0V$			3.3	6.6	mA

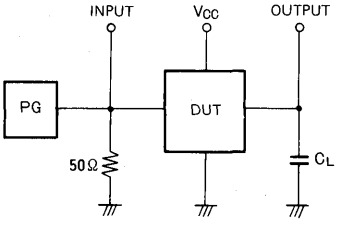
* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high output level propagation time	$C_L=15pF$ (Note 2)		9	15	ns
t_{PHL}	High-to-low output level propagation time			10	20	ns

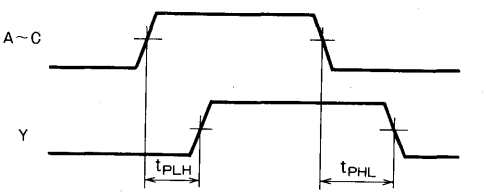
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS12P

TRIPLE 3-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS12P is a semiconductor integrated circuit containing three triple-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 6mW typical)
- High speed (t_{pd} = 13ns typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

With the use of Schottky barrier diodes for the inputs and open-collector outputs, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

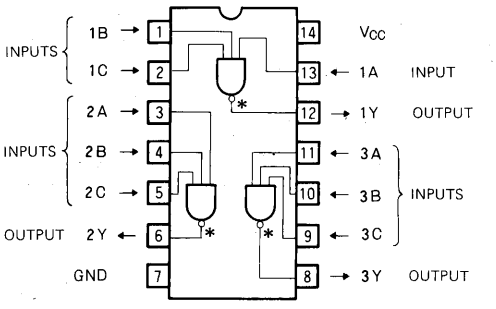
When inputs A, B and C are high, output Y is low and when one or more of the inputs is low, the output Y is high.

FUNCTION TABLE

A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

N = B・C

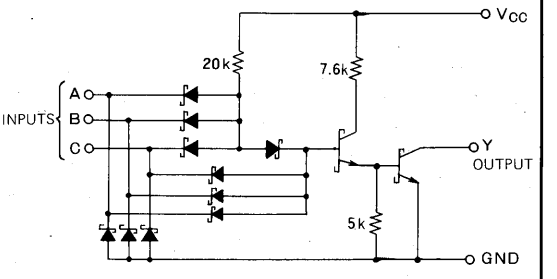
PIN CONFIGURATION (TOP VIEW)



*: OPEN COLLECTOR OUTPUT

Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

TRIPLE 3-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O = 5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL} ≦ 0.4V	0		4	mA
		V_{OL} ≦ 0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

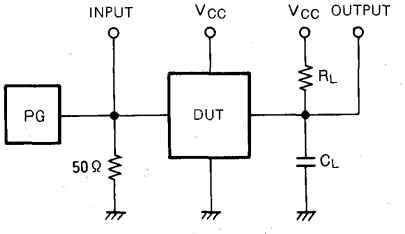
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75V, V_I = 0.8V, V_O = 5.5V				100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, V_I = 2V	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{CCH}	Supply current, all inputs high	V_{CC} = 5.25V, V_I = 0V			0.7	1.4	mA
I_{CCL}	Supply current, all inputs low	V_{CC} = 5.25V, V_I = 4.5V			1.8	3.3	mA

* : All typical vlaues are at V_{CC} = 5V, T_a = 25°C

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level/high-to-low level output propagation time	R_L = 2 kΩ, C_L = 15pF (Note)		10	32	ns
t_{PHL}				15	28	ns

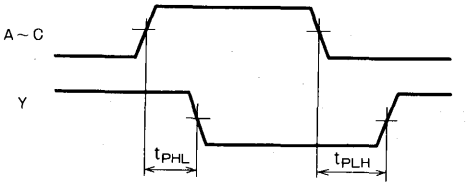
Note: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω.

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS13P

DUAL 4-INPUT NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS13P is a semiconductor integrated circuit containing two 4-input positive-logic NAND gates having a Schmitt trigger function and negative-logic NOR gates.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.8V typical) and high noise margin
- High breakdown input voltage ($V_I \geqq 15V$) ($V_I \geqq 15V$, $V_O \geqq 7V$)
- Low power dissipation ($P_d = 17.5mW$ typical)
- High speed (t_{pd} = 16ns typical)
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

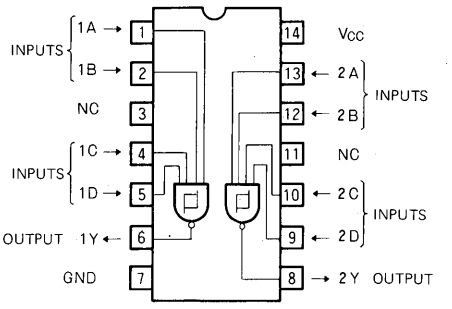
FUNCTIONAL DESCRIPTION

The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.8V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in a shaped waveform output without causing oscillation.

When inputs A, B, C and D are high, output Y is low, and when one or more of the inputs are low, Y is high.

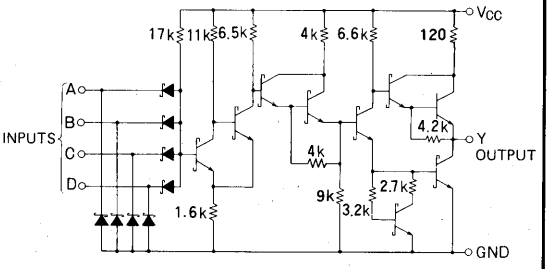
Refer to M74LS14P for the typical characteristics.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC : NO CONNECTION

CIRCUIT SCHEMATIC (EACH SCHMITT TRIGGER)



UNIT : Ω

FUNCTION TABLE

A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

N = B・C・D

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

DUAL 4-INPUT NAND SCHMITT TRIGGER

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{T+}	Positive-going threshold voltage	$V_{CC}=5V$		1.4	1.6	1.9	V
V_{T-}	Negative-going threshold voltage	$V_{CC}=5V$		0.5	0.8	1	V
$V_{T+}-V_{T-}$	Hysteresis width	$V_{CC}=5V$		0.4	0.8		V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.5V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $V_I=1.9V$	$I_{OL}=4mA$		0.25	0.4	V
			$I_{OL}=8mA$		0.35	0.5	V
I_{T+}	Input current at positive-going threshold	$V_{CC}=5V$, $V_I=V_{T+}$			−0.14		mA
I_{T-}	Input current at negative-going threshold	$V_{CC}=5V$, $V_I=V_{T-}$			−0.18		mA
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=0V$			2.9	6	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=4.5V$			4.1	7	mA

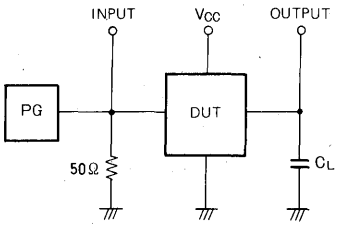
* : All typical values are at $V_{CC}=5V$, $Ta=25°C$

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	$C_L=15pF$ (Note 2)		12	22	ns
t_{PHL}	High-to-low-level output propagation time			20	27	ns

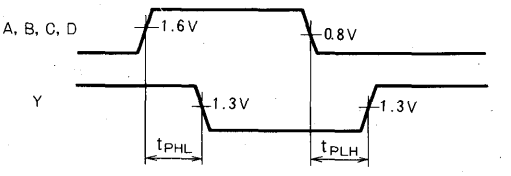
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.

(2) C_L includes probe and jig capacitance

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74LS14P

HEX SCHMITT TRIGGER INVERTERS

DESCRIPTION

The M74LS14P is a semiconductor integrated circuit containing 6 Schmitt trigger inverter circuits.

FEATURES

- Suitable for waveform shaping applications
- Wide hysterisis width (0.8V typical) and high noise margin
- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 51mW typical)
- High speed (tpd = 12ns typical)
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

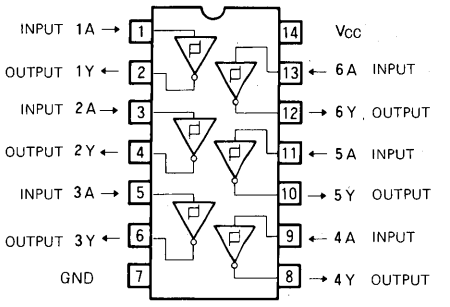
The use Schottly TTL technology has enabled the achievement of high input voltage, high speed, low power dissipation, and high fan-out. With positive feedback applied in the circuit, the hysterisis width is 0.8V (typical). Accordingly, noise margin is high. Even slow changing input signals result in a shaped waveform output without casing oscillation.

When input A is high, output Y is low, and when A is low, Y is high.

FUNCTION TABLE

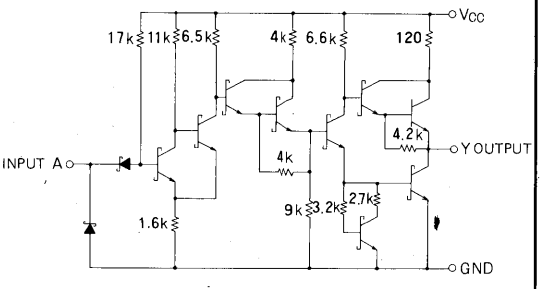
A	Y
L	H
H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH CIRCUIT)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

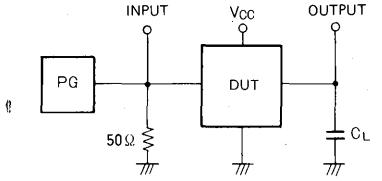
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{T+}	Positive-going threshold voltage	$V_{CC}=5V$		1.4	1.6	1.9	V
V_{T-}	Negative-going threshold voltage	$V_{CC}=5V$		0.5	0.8	1	V
$V_{T+}-V_{T-}$	Hysteresis	$V_{CC}=5V$		0.4	0.8		V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.5V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $V_I=1.9V$	$I_{OL}=4mA$		0.25	0.4	V
			$I_{OL}=8mA$		0.35	0.5	V
I_{T+}	Input current at positive-going threshold	$V_{CC}=5V$, $V_I=V_{T+}$			−0.14		mA
I_{T-}	Input current at negative-going threshold	$V_{CC}=5V$, $V_I=V_{T-}$			−0.18		mA
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=0V$			8.6	16	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=4.5V$			12	21	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

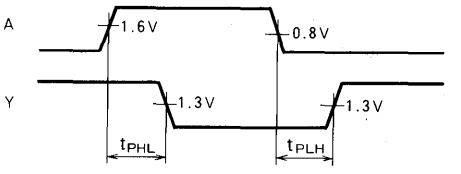
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	$C_L=15pF$ (Note 2)		12	22	ns
t_{PHL}	High-to-low-level output propagation time			12	22	ns

Note 2: Measurement circuit



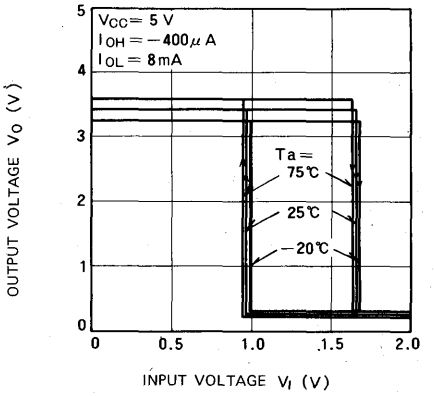
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM

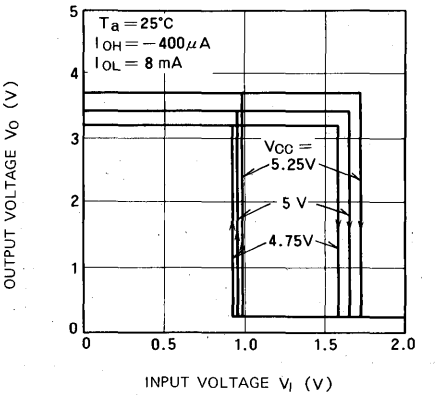


TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE VS INPUT VOLTAGE



OUTPUT VOLTAGE VS INPUT VOLTAGE



M74LS15P

TRIPLE 3-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS15P is a semiconductor integrated circuit containing 3 triple-input positive AND and negative OR gates with open collector outputs.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage ($V_I \geqq 15V$)
- High breakdown output voltage ($V_O \geqq 7V$)
- Low power dissipation (P_d = 13mW typical)
- High speed (t_{pd} = 13ns typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

With the use of Schottky TTL Technology and open collector outputs with a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

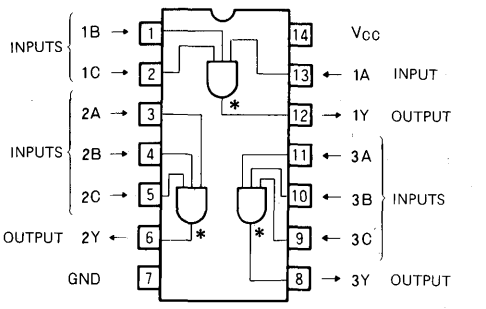
When inputs A, B and C are high, output Y is high and when one or more of the inputs is low, Y is low.

FUNCTION TABLE

A	N	Y
L	L	L
H	L	L
L	H	L
H	H	H

N = B · C

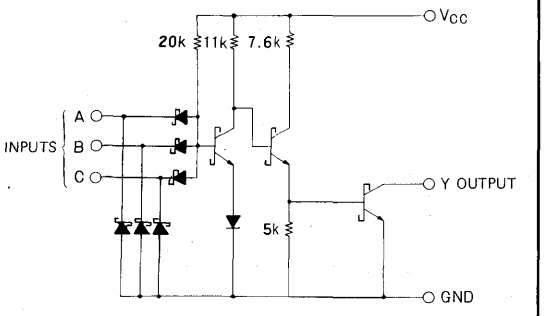
PIN CONFIGURATION (TOP VIEW)



* : OPEN COLLECTOR OUTPUT

Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

TRIPLE 3-INPUT POSITIVE AND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O=5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		4	mA
		V_{OL}≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

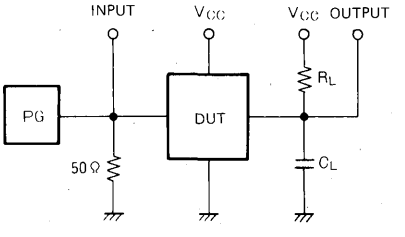
Symbol	Parameter	Conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
I_{OH}	High-level output current	V_{CC}=4.75V, V_I=2V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage	V_{CC}=4.75V, V_I=0.8V	I_{OL}= 4mA		0.25	0.4	V
			I_{OL}= 8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.25V, V_I=4.5V			1.8	3.6	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.25V, V_I= 0			3.3	6.6	mA

* : All typical values are at V_{CC}=5V, Ta=25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

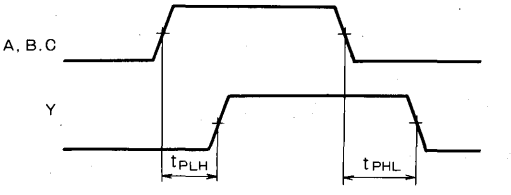
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	R_L=2KΩ		15	35	ns
t_{PHL}	High-to-low-level output propagation time	C_L=15pF (Note)		10	35	ns

Note: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS18P

DUAL 4-INPUT NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS18P is a semiconductor integrated circuit containing two 4-input positive-logic NAND gates having a schmitt trigger function and negative-logic NOR gates.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.9V typical) and high noise margin
- Reduce low-level input current (PNPTr input)
- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 22mW typical)
- High speed (t_{pd} = 24ns typical)
- Wide operating temperature range (T_a = –20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

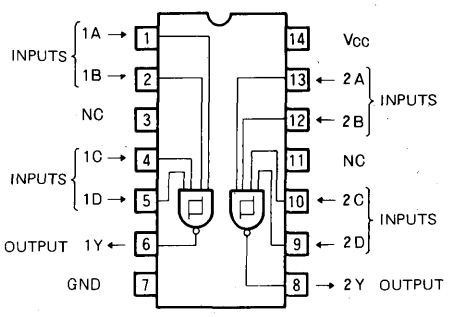
It is an IC with PNPTr inputs, active pull-up in the outputs, input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.9V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in shaped waveform output without causing oscillation.

When A, B, C and D inputs are high, output Y is low, and when more than one is low, Y is high.

M74LS13P can be replaced with M74LS18P without any changes as pin connections, functions, are interchangeable. Depending on PNPTr input usage, loading on the transmission can be reduced. Depending on the high level of the threshold voltage setting, low level noise margin can be improved.

For typical characteristics see M74LS19P.

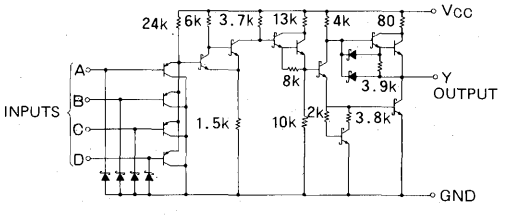
PIN CONFIGURATION (TOP VIEW)



Outline 14P4

NC: NO CONNECTION

CIRCUIT SCHEMATIC (Each schmitt trigger)



UNIT: Ω

FUNCTION TABLE

A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

N = B·C·D

ABSOLUTE MAXIMUM RATINGS (Ta = –20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		–0.5 ~ +7	V
V_I	Input voltage		–0.5 ~ +15	V
V_O	Output voltage	High-level state	–0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		–20 ~ +75	°C
Tstg	Storage temperature range		–65 ~ +150	°C

DUAL 4-INPUT NAND SCHMITT TRIGGER

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

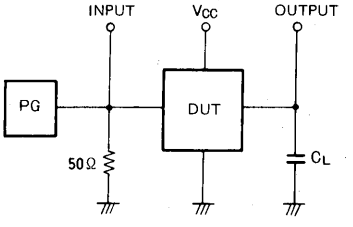
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{T+}	Positive-going threshold voltage	V_{CC}=5V		1.65	1.9	2.15	V
V_{T-}	Negative-going threshold voltage	V_{CC}=5V		0.75	1.0	1.25	V
$V_{T+}-V_{T-}$	Hysteresis width	V_{CC}=5V		0.4	0.9		V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.5V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V, V_I=1.9V	I_{OL}=4mA		0.25	0.4	V
			I_{OL}=8mA		0.35	0.5	V
I_{T+}	Input current at positive-going threshold	V_{CC}=5V, V_I=V_{T+}			−2		μA
I_{T-}	Input current at negative-going threshold	V_{CC}=5V, V_I=V_{T-}			−5		μA
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.05	mA
I_{OS}	Short-circuit output current (Note 1)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.25V, V_I=0V			3.3	6	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.25V, V_I=4.5V			5.7	10	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

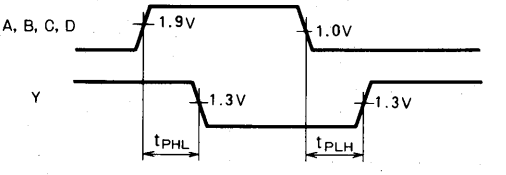
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	C_L=15pF (Note 2)		12	20	ns
t_{PHL}	High-to-low-level output propagation time			37	55	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74LS19P

HEX SCHMITT TRIGGER INVERTER

DESCRIPTION

The M74LS19P is a semiconductor integrated circuit containing 6 schmitt trigger inverter circuits.

FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.9V typical) and high noise margin
- Reduce low-level input current (PNPTr input)
- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 67mW typical)
- High speed (t_{pd} = 13ns typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

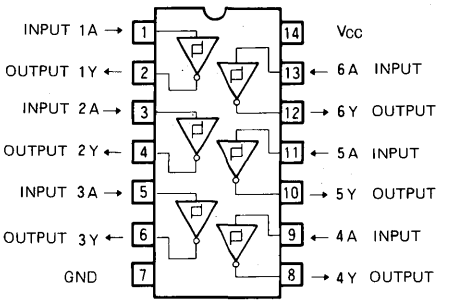
FUNCTIONAL DESCRIPTION

It is an IC with PNPTr inputs, active pull-up in the outputs, input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.9V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in shaped waveform output without causing oscillation.

When input A is high, output Y is low, and when A is low, Y is high.

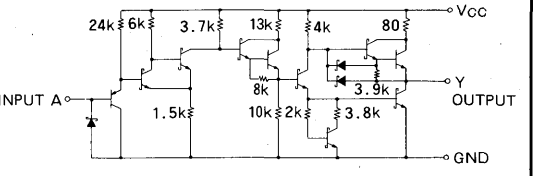
M74LS14P can be replaced with M74LS19P without any changes as pin connections, functions, are interchangeable. Depending on PNPTr input usage, loading on the transmission can be reduced. Depending on the high level of the threshold voltage setting, low level noise margin can be improved.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC



UNIT: Ω

FUNCTION TABLE

A	Y
L	H
H	L

ABSOLUTE MAXIMUM RATINGS

(Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

HEX SCHMITT TRIGGER INVERTER

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75℃$, unless otherwise noted)

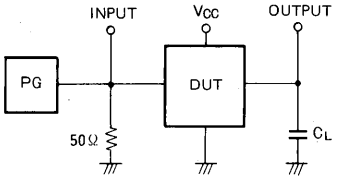
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{T+}	Positive-going threshold voltage	$V_{CC}=5V$		1.65	1.9	2.15	V
V_{T-}	Negative-going threshold voltage	$V_{CC}=5V$		0.75	1.0	1.25	V
$V_{T+}-V_{T-}$	Hysteresis width	$V_{CC}=5V$		0.4	0.9		V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.5V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=1.9V$	$I_{OL}=8mA$		0.35	0.5	V
I_{T+}	Input current at positive-going threshold	$V_{CC}=5V$, $V_I=V_{T+}$			−2		μA
I_{T-}	Input current at negative-going threshold	$V_{CC}=5V$, $V_I=V_{T-}$			−5		μA
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.05	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=0V$			9.9	18	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=4.5V$			17	30	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25℃$, unless otherwise noted)

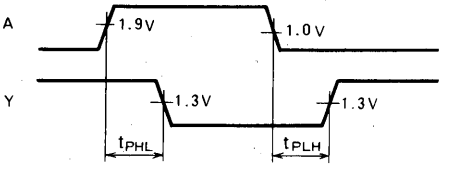
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	$C_L=15pF$ (Note 2)		11	20	ns
t_{PHL}	High-to-low-level output propagation time			15	30	ns

Note 2: Measurement circuit



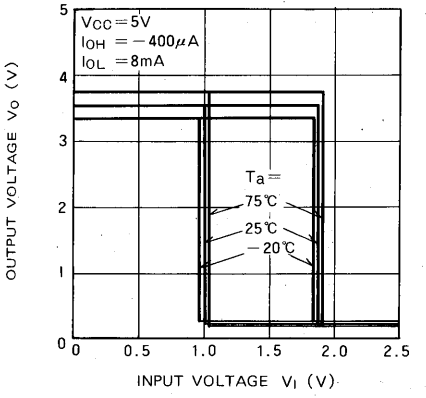
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM

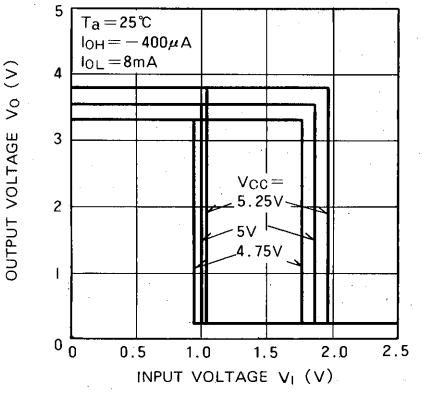


TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE VS. INPUT VOLTAGE



OUTPUT VOLTAGE VS. INPUT VOLTAGE



MITSUBISHI ELECTRIC

M74LS20P

DUAL 4-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74LS20P is a semiconductor integrated circuit containing two 4-input positive NAND gates, usable as negative-logic NOR gates.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 4mW typical)
- High speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of Schottky TTL technolgoy enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

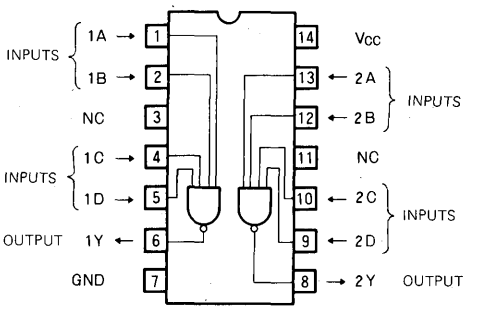
When inputs A, B and C are high, output Y is low, and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

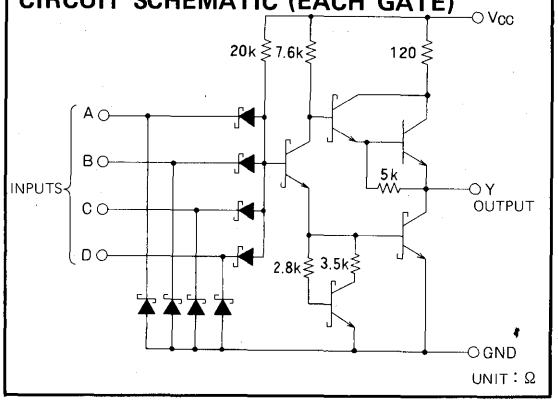
N=B・C・D

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC: NO CONNECTION

CIRCUIT SCHEMATIC (EACH GATE)



ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

DUAL 4-INPUT POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
		V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CCH}	Supply current, all inputs high	V_{CC}=5.25V, V_I=0V			0.4	0.8	mA
I_{CCL}	Supply current, all inputs low	V_{CC}=5.25V, V_I=4.5V			1.2	2.2	mA

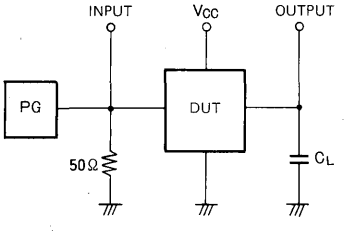
* : All typical values are at V_{CC}=5V, Ta=25°C

Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level/high-to-low-level output propagation time	C_L=15pF (Note 2)		6	15	ns
t_{PHL}				13	15	ns

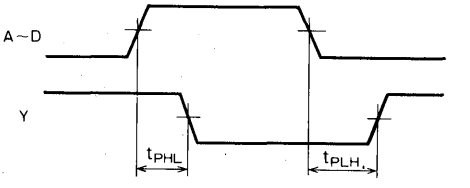
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
V_P = $3V_{P\text{-}P}$, Z_O = 50Ω.

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



MITSUBISHI ELECTRIC

M74LS21P

DUAL 4-INPUT POSITIVE AND GATE

DESCRIPTION

The M74LS21P is a semiconductor integrated circuit containing two 4-input positive AND and negative OR gates.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (Pd = 8.5mW typical)
- High speed (t_{pd} = 9ns typical)
- Low output impedance
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of Schottky TTL technology and active output pullups enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

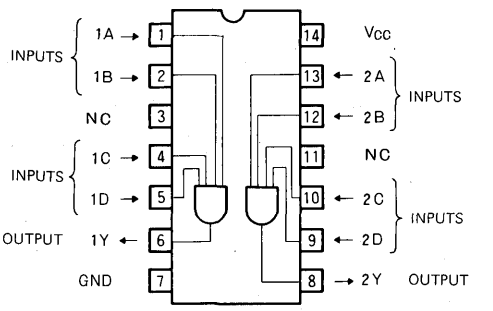
When inputs A, B, C and D are high, output Y is high, and when one or more of the inputs is low, Y is low.

FUNCTION TABLE

A	N	Y
L	L	L
H	L	L
L	H	L
H	H	H

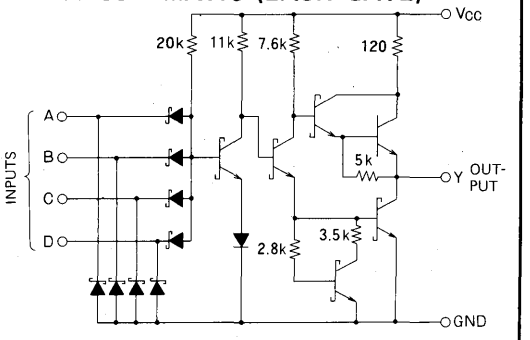
N = B・C・D

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC : NO CONNECTION

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

DUAL 4-INPUT POSITIVE AND GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
			$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=4.5V$			1.2	2.4	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=0V$			2.2	4.4	mA

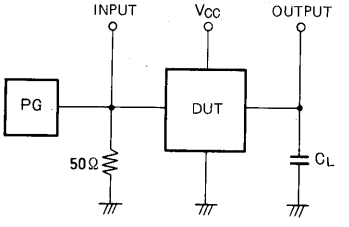
* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.

Note 1: All measurements must be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-output level propagation time	$C_L=15pF$ (Note 2)		9	15	ns
t_{PHL}	High-to-low-output level propagation time			10	20	ns

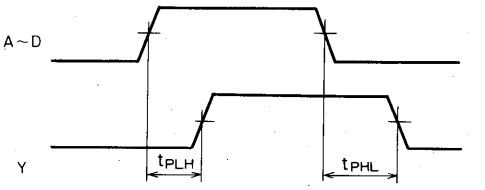
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS22P

DUAL 4-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS22P is a semiconductor integrated circuit containing two 4-input positive-logic NAND gates with open collector outputs, usable as negative-logic NOR gates.

FEATURES

- Usable in wire-AND connection
- High breakdown input voltage ($V_I \geqq 15V$)
- High breakdown output voltage ($V_O \geqq 7V$)
- Low power dissipation (P_d = 4mW typical)
- High speed (t_{pd} = 18ns typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

With the use of open collector outputs and SBD inputs featuring a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection which has been impossible with conventional gates.

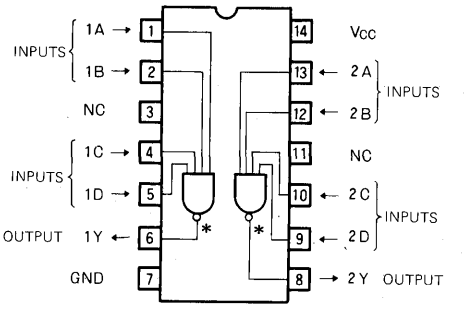
When inputs A, B, C and D are high, output Y is low and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

N=B・C・D

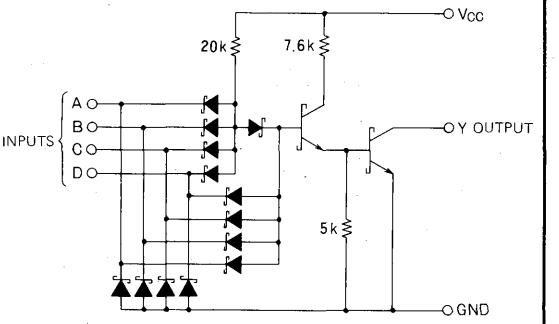
PIN CONFIGURATION (TOP VIEW)



* : OPEN COLLECTOR OUTPUT
NC : NO CONNECTION

Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

DUAL 4-INPUT POSITIVE NAND GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING OCNDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O = 5.5V	0		100	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

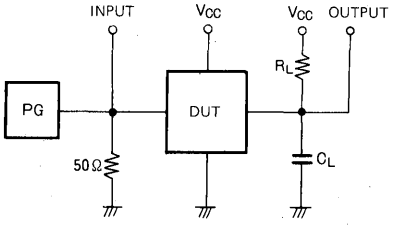
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75V, V_I = 0.8V, V_O = 5.5V				100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, V_I = 2V	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{CCH}	Supply current, all inputs high	V_{CC} = 5.25V, V_I = 0V			0.4	0.8	mA
I_{CCL}	Supply current, all inputs low	V_{CC} = 5.25V, V_I = 4.5V			1.2	2.2	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C

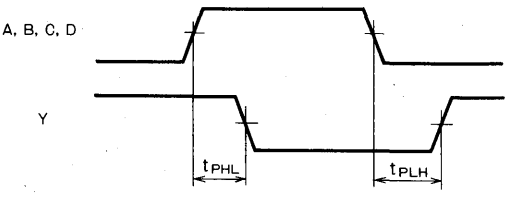
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level/high-to-low-level output propagation time	R_L = 2kΩ, C_L = 15pF (Note 1)		10	32	ns
t_{PHL}				25	28	ns

Note 1: Measurement circuit



TIMING DIAGRAM (Reference level = 1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns;
V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

M74LS24P

QUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS24P is a semiconductor integrated circuit containing four 2-input positive-logic NAND gates having a schmitt trigger function and negative-logic NOR gates.

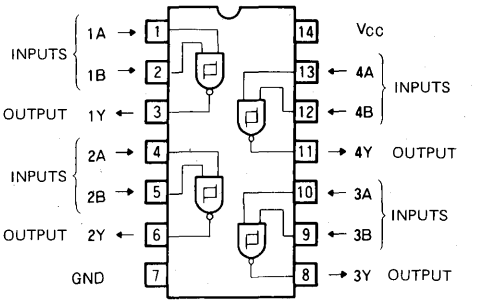
FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.9V typical) and high noise margin
- Reduce low-level input current (PNPTr input)
- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 44mW typical)
- High speed (t_{pd} = 18ns typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

FUNCTIONAL DESCRIPTION

It is an IC with PNPTr inputs, active pull-up in the outputs, input high breakdown voltage, high speed, low power dissipation and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.9V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in shaped waveform output without causing oscillation.

When A and B inputs are high, output Y is low, and when more than one is low, output Y is high.

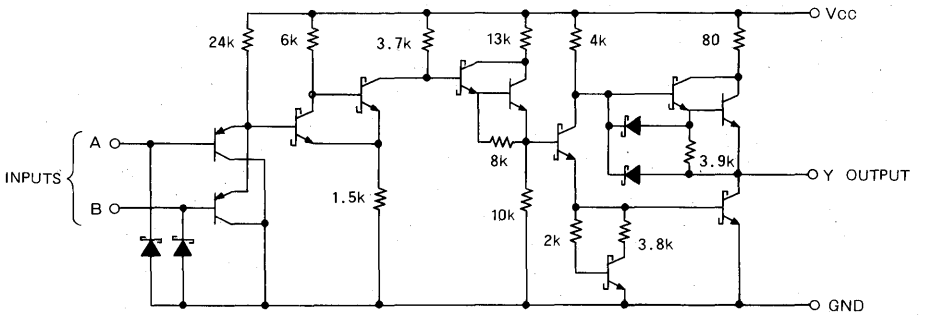
M74LS132P can be replaced with M74LS24P without any changes as pin connections, functions, are interchangeable. Depending on PNPTr input usage, loading on the transmission can be reduced. Depending on the high level of the threshold voltage setting, low level noise margin can be improved.

For typical characteristics see M74LS19P.

FUNCTION TABLE

A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

CIRCUIT SCHEMATIC (Each schmitt trigger)



UNIT: Ω

QUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

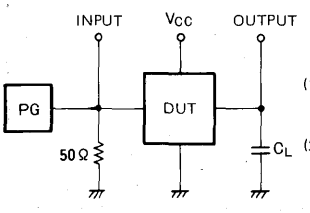
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{T+}	Positive-going threshold voltage	V_{CC} = 5V		1.65	1.9	2.15	V
V_{T-}	Negative-going threshold voltage	V_{CC} = 5V		0.75	1.0	1.25	V
$V_{T+} - V_{T-}$	Hysteresis width	V_{CC} = 5V		0.4	0.9		V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V, V_I = 0.5V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, V_I = 1.9V	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5V, $V_I = V_{T+}$			−2		μA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5V, $V_I = V_{T-}$			−5		μA
I_{IH}	High-level input current	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.05	mA
I_{OS}	Short-circuit output current (Note 1)	V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = 5.25V, V_I = 0V			6.6	12	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = 5.25V, V_I = 4.5V			11	20	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25℃, unless otherwise noted)

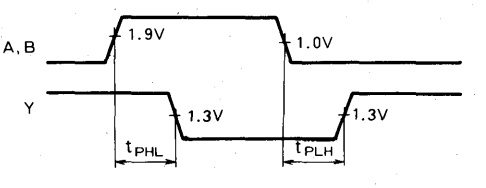
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	C_L = 15pF (Note 2)		13	20	ns
t_{PHL}	High-to-low-level output propagation time			24	40	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74LS27P

TRIPLE 3-INPUT POSITIVE NOR GATE

DESCRIPTION

The M74LS27P is a semiconductor integrated circuit containing three triple-input positive NOR and negative NAND gates.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 13.5mW typical)
- High speed (t_{pd} = 6ns typical)
- Low output impedance
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of Schottky TTL technology and active output pullups enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

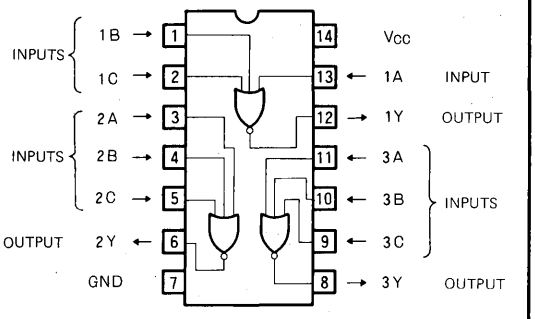
When one or more of the A, B and C inputs are high, output Y is low and when all inputs are low, Y is high.

FUNCTION TABLE

A	N	Y
L	L	H
H	L	L
L	H	L
H	H	L

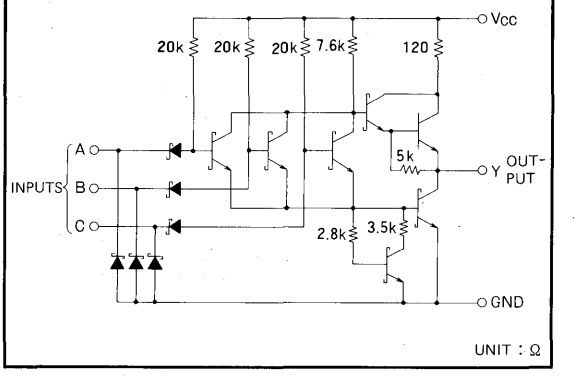
N=B+C

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

TRIPLE 3-INPUT POSITIVE NOR GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
			$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=0V$			2	4	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=4.5V$			3.4	6.8	mA

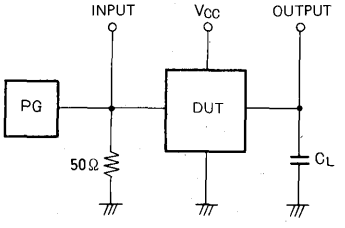
* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.

Note 1: All measurements must be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

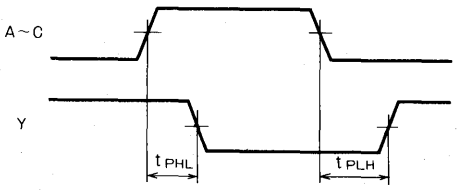
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	$C_L=15pF$		6	15	ns
t_{PHL}	High-to-low-level output propagation time	(Note 2)		6	15	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, $t_r \approx 6ns$, $t_f = 6ns$, $t_W = 500ns$,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS30P

SINGLE 8-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74LS30P is a semiconductor integrated circuit containing one 8-input positive-logic NAND gate, usable as a negative-logic NOR gate.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 2.4mW typical)
- High speed (t_{pd} = 11ns typical)
- Low output impedance
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of Schottky TTL technology enables the achievement of input high breakdown voltage, high speed, low power dissipation and high fan-out.

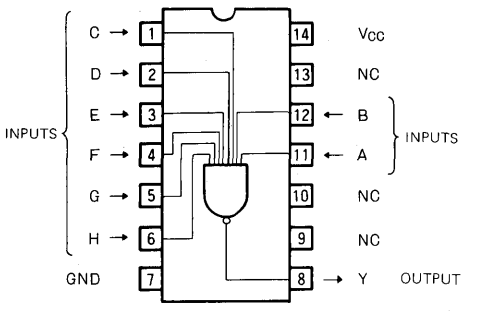
When inputs A, B, C, D, E, F and G are high, output Y is low and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

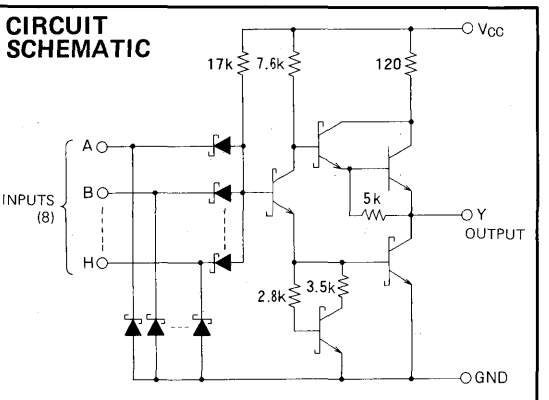
N=B・C・D・E・F・G・H

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC: NO CONNECTION

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +V_{CC}	V
T_{opr}	Operating free-air ambinet temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

SINGLE 8-INPUT POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output circuit (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all inputs high	$V_{CC}=5.25V$, $V_I=0V$			0.35	0.5	mA
I_{CCL}	Supply current, all inputs low	$V_{CC}=5.25V$, $V_I=4.5V$			0.6	1.1	mA

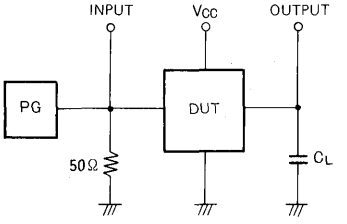
* : All typical values are at $V_{CC}=5V$, $T_a=25°C$

Note 1: All measurements should be done quickly.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level/high-to-low-level output propagation time	$C_L=15pF$ (Note 2)		6	15	ns
t_{PHL}				16	20	ns

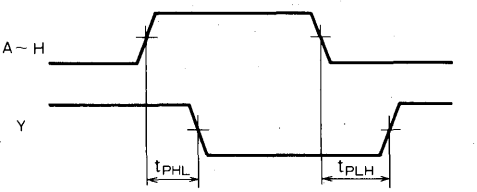
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characterisitcs:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns;
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.

(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



PRECAUTION FOR USE

Connect pins not being used to the V_{CC} supply voltage.

M74LS32P

QUADRUPLE 2-INPUT POSITIVE OR GATES

DESCRIPTION

The M74LS32P is a semiconductor integrated circuit containing 4 dual-input positive OR and negative AND gates.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 20mW typical)
- High speed (t_{pd} = 7ns typical)
- Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

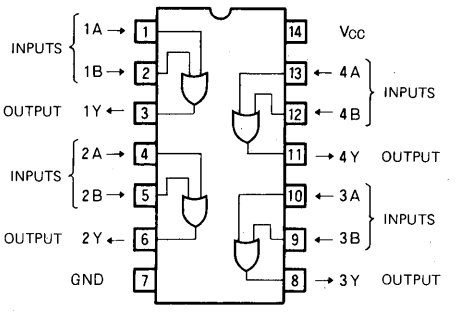
The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

When either or both of the inputs A and B is/are high, output Y is high, and when both A and B are low, Y is low.

FUNCTION TABLE

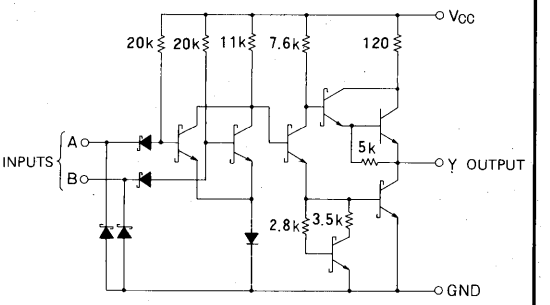
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	℃
T_{stg}	Storage temperature range		−65 ~ +150	℃

QUADRUPLE 2-INPUT POSITIVE OR GATES

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_{OH}≧2.7V	0		−400	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		4	mA
		V_{OL}≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

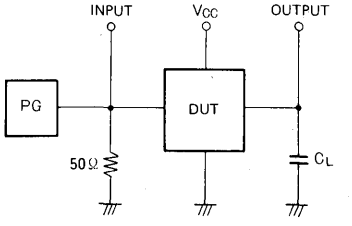
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
		V_I=0.8V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.25V, V_I=4.5V			3.1	6.2	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.25V, V_I=0V			4.9	9.8	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

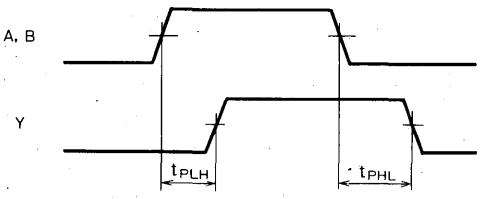
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	C_L=15pF (Note 2)		7	22	ns
t_{PHL}	High-to-low-level output propagation time			7	22	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characterstics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS37P

QUADRUPLE 2-INPUT POSITIVE NAND BUFFER

DESCRIPTION

The M74LS37P is a semiconductor integrated circuit containing four 2-input positive NAND and negative NOR buffer gates.

FEATURES

- High fan-out (I_{OL} = 24mA, I_{OH} = −1.2mA)
- High breakdown input voltabe ($V_I \geqq 15V$)
- Low power dissipation (P_d = 17.5mW typical)
- High speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

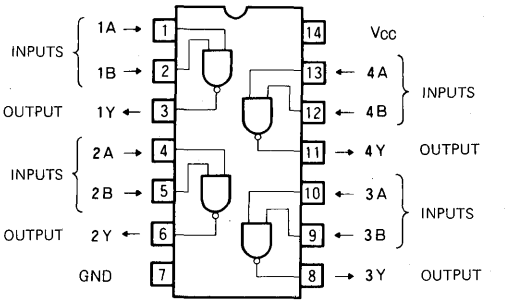
The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

When inputs A and B are high, output Y is low, and when one or both inputs are low, Y is high.

FUNCTION TABLE

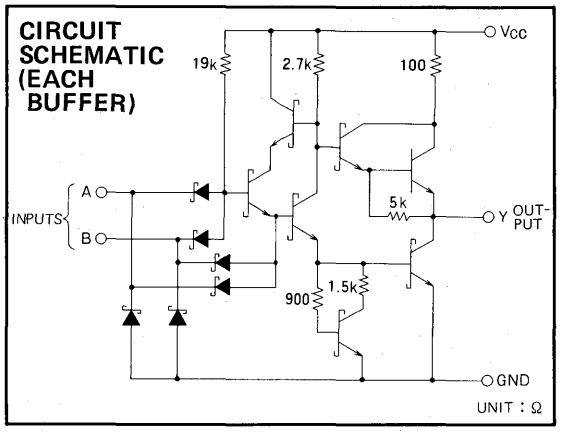
A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH BUFFER)



MAXIMUM ABSOLUTE RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

QUADRUPLE 2-INPUT POSITIVE NAND BUFFER

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−1.2	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

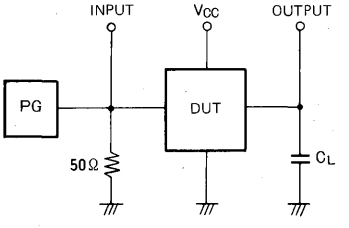
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $I_{OH}=-1.2mA$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=12mA$		0.25	0.4	V
		$V_I=2V$	$I_{OL}=24mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−30		−130	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=0V$			0.9	2	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=4.5V$			6	12	mA

* : All typical values are at $V_{CC}=5V$, $Ta=25°C$.
Note 1: All measurement should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$, unless otherwise noted)

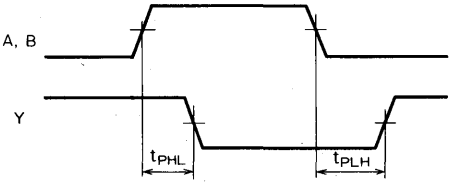
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	$C_L=45pF$		7	24	ns
t_{PHL}	High-to-low-level output propagation time	(Note 2)		12	24	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50Ω$.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS38P

QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS38P is a semiconductor integrated circuit containing four 2-input positive NAND and negative NOR buffer gates with open collector outputs.

FEATURES

- Usable in wire-AND connection
- High fan-out (I_{OL} = 24mA max)
- High breakdown input voltage ($V_I \geqq 15V$)
- High breakdown output voltage ($V_O \geqq 7V$)
- Low power dissipation (P_d = 17.5mW typical)
- High speed (t_{pd} = 14ns typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

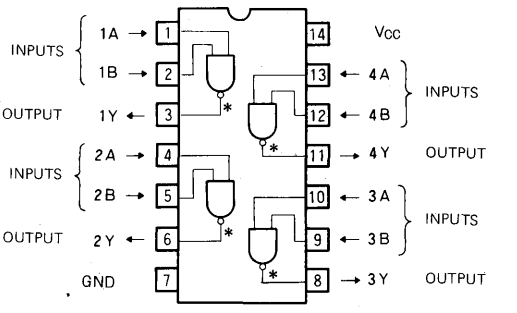
FUNCTIONAL DESCRIPTION

With the use of open collector outputs and SBD inputs having a high breakdown voltage, the high-level output impedance can be selected freely by use of an external load resistor. This permits wire-AND connection, which has been impossible with conventional gates. The maximum low-level output current (I_{OL}) of 24mA makes this device suitable as a buffer gate. When inputs A and B are high, output Y is low and when one or both inputs are low, Y is high.

FUNCTION TABLE

A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

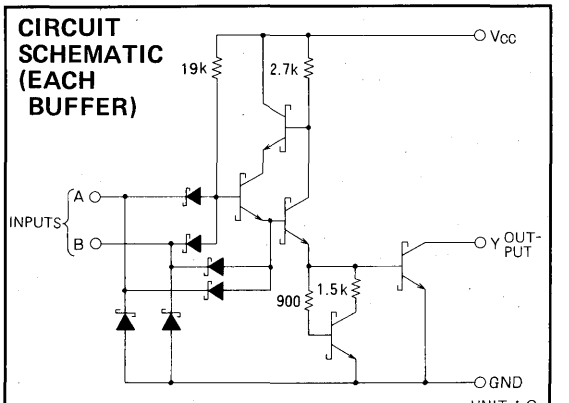
PIN CONFIGURATION (TOP VIEW)



∗ : OPEN COLLECTOR OUTPUT

Outline 14P4

CIRCUIT SCHEMATIC (EACH BUFFER)



ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

QUADRUPLE 2-INPUT POSITIVE NAND BUFFER WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_O = 5.5V$	0		250	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

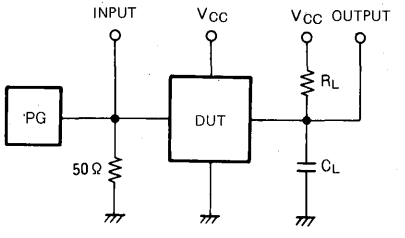
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$				−1.5	V
I_{OH}	High-level output current	$V_{CC} = 4.75V$, $V_I = 0.8V$, $V_O = 5.5V$				250	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$	$I_{OL} = 12mA$		0.25	0.4	V
		$V_I = 2V$	$I_{OL} = 24mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.4	mA
I_{CCH}	Supply current, all outputs high	$V_{CC} = 5.25V$, $V_I = 0V$			0.9	2	mA
I_{CCL}	Supply current, all outputs low	$V_{CC} = 5.25V$, $V_I = Open$			6	12	mA

* : All typical values are at $V_{CC} = 5V$, $T_a = 25°C$.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	$R_L = 667\Omega$		13	32	ns
t_{PHL}	High-to-low-level output propagation time	$C_L = 45pF$ (Note 1)		14	28	ns

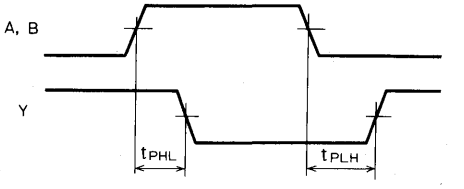
Note 1: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS40P

DUAL 4-INPUT POSITIVE NAND BUFFER

DESCRIPTION

The M74LS40P is a semiconductor integrated circuit containing 2 built-in quadruple-input positive NAND and negative NOR buffer gates.

FEATURES

- High fan-out (I_{OL} = 24mA, I_{OH} = −1.2mA)
- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d =9mW typical)
- High speed (t_{pd} = 14ns typical)
- Low output impedance
- Wide operating temperature range (Ta = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

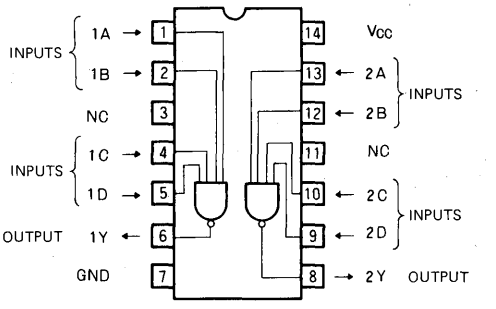
When all inputs A, B, C and D are high, output Y is low and when one or more of the inputs is low, Y is high.

FUNCTION TABLE

A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

N=B·C·D

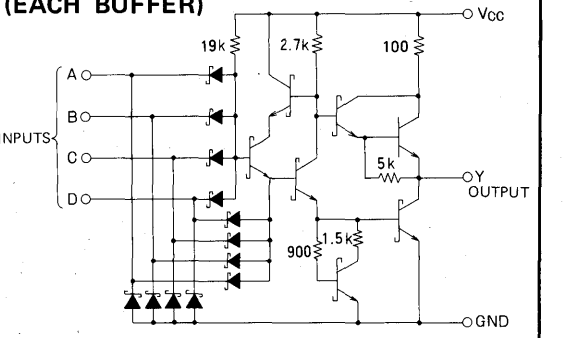
PIN CONFIGURATION (TOP VIEW)



NC : NO CONNECTION

Outline 14P4

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

DUAL 4-INPUT POSITIVE NAND BUFFER

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−1.2	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $I_{OH}=-1.2mA$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=12mA$		0.25	0.4	V
		$V_I=2V$	$I_{OL}=24mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−30		−130	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=0V$			0.45	1	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=$ Open			3	6	mA

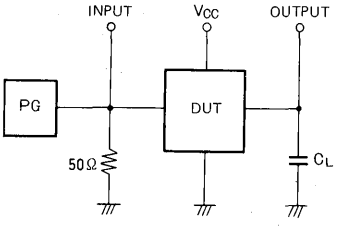
* : All typical values are at $V_{CC}=5V$, $T_a=25°C$

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	$C_L=45pF$		7	24	ns
t_{PHL}	High-to-low-level output propagation time	(Note 2)		20	24	ns

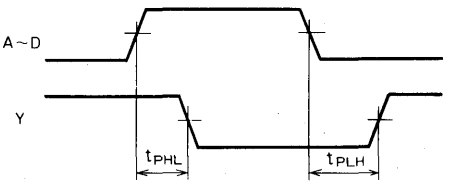
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS42P

BCD-TO-DECIMAL DECODER

DESCRIPTION

The M74LS42P is a semiconductor integrated circuit provided with a BCD-to-decimal decoder function.

FEATURES

- All outputs set high with reactive input
- Usable as a 3-bit binary/octal decoder
- Wide operating temperature range (T_a=−20~+75°C)

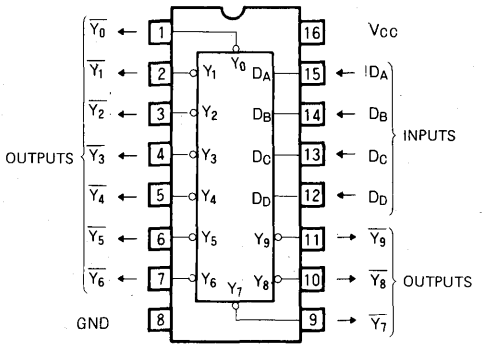
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

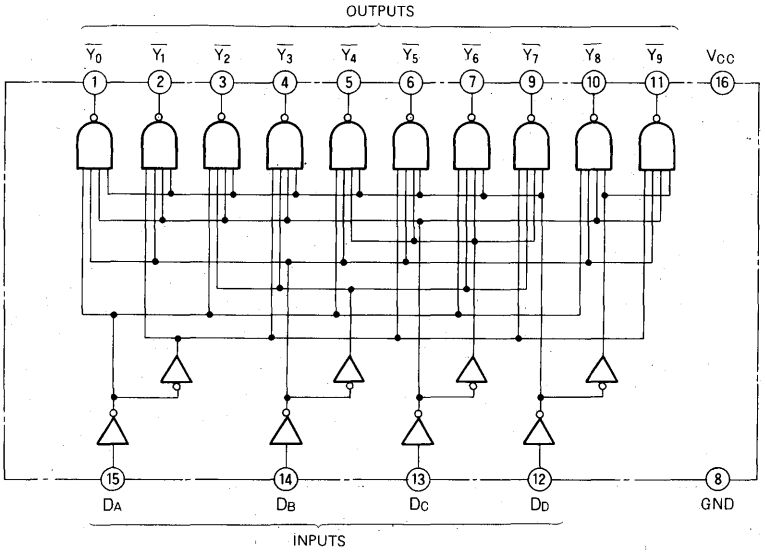
When inputs D_A, D_B, D_C and D_D are specified in BCD code, the output corresponding to the number among $\overline{Y_0}$~$\overline{Y_9}$ is set low and all the other 9 outputs are set high. When a binary number of 10 or more is applied to D_A~D_D, all the outputs are set high.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



BCD-TO-DECIMAL DECODER

FUNCTION TABLE

Decimal number	D_D	D_C	D_B	D_A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$	$\overline{Y_8}$	$\overline{Y_9}$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	H	L	H	L	H	H	H	H	H	H	H	H	H	H
11	H	L	H	H	H	H	H	H	H	H	H	H	H	H
12	H	H	L	L	H	H	H	H	H	H	H	H	H	H
13	H	H	L	H	H	H	H	H	H	H	H	H	H	H
14	H	H	H	L	H	H	H	H	H	H	H	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75V	I_{OL} = 4mA		0.25	0.4	V
		V_I = 0.8V, V_I = 2V	I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC}	Supply current	V_{CC} = 5.25V (Note 2)			7	13	mA

* : All typical values are at V_{CC} = 5V, Ta = 25℃

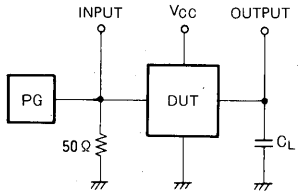
Note 1: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 2: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

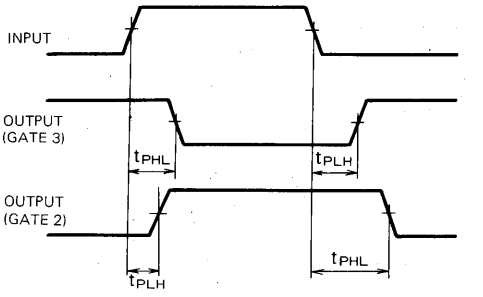
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, gate 2	C_L=15pF (Note 3)		8	25	ns
t_{PHL}				14	25	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, gate 3			12	30	ns
t_{PHL}				12	30	ns

Note 3: Measurement circuit



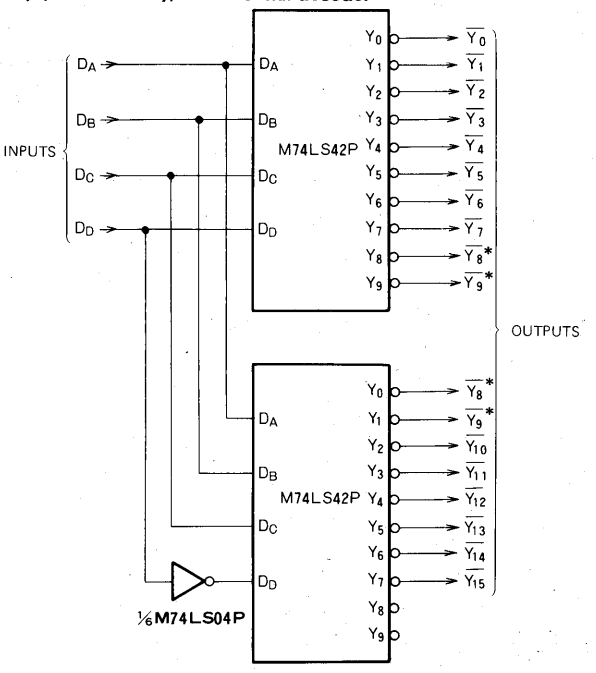
(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Z_O=50Ω
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



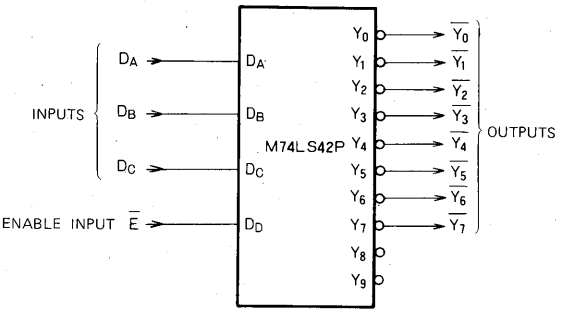
APPLICATION EXAMPLES

(1) 4-bit binary/hexadecimal decoder



Outputs marked with * are provided from both decoders.

(2) 3-bit binary/octal decoder with enable input



M74LS47P

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-LOW OUTPUT)

DESCRIPTION

The M74LS47P is a semiconductor integrated circuit provided with BCD-to-7-segment decoder/driver function and open collector outputs.

FEATURES

- Suitable for 7-segment display element lighting
- $\overline{RBI}$ input and $\overline{BI}/\overline{RBO}$ outputs for zero suppression
- $\overline{LT}$ input for lamp testing
- $\overline{BI}/\overline{RBO}$ input for extinguishing all segments
- Open collector outputs
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When a number is designed in BCD code for BCD inputs D_A, D_B, D_C and D_D, segment outputs $\overline{a}$~$\overline{g}$ are set low in accordance with that number. By connecting the 7-segment display element to each of the outputs, the character indicated on the display character can be displayed. $\overline{a}$~$\overline{g}$ are open collector outputs with a breakdown voltage of not less than 15V and a low-level output current of 24mA, thereby making it possible to directly drive a 7-segment LED for the display of anode-common numbers.

Suppression of the high-order unnecessary zeroes is possible by setting the highest order $\overline{RBI}$ ripple blanking input low and connecting ripple blanking output $\overline{BI}/\overline{RBO}$ to the next-order $\overline{RBI}$ for each of the digits. (Refer to the application example.)

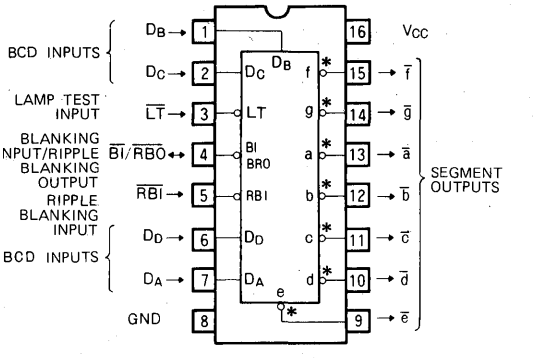
By setting blanking input $\overline{BI}/\overline{RBO}$ low, outputs $\overline{a}$~$\overline{g}$ are set high and the display element is extinguished irrespective of the status of the other inputs. The luminous intensity can be controlled by applying pulses.

Since $\overline{BI}/\overline{RBO}$ serves as both an input and output pin, only ICs with open collector outputs can be connected to this pin.

By setting lamp test input $\overline{LT}$ low, $\overline{a}$~$\overline{g}$ are set low irrespective of the status of $\overline{BI}/\overline{RBO}$, D_A, D_B, D_C and D_D, all the segments in the display element are lighted and each segment can be tested.

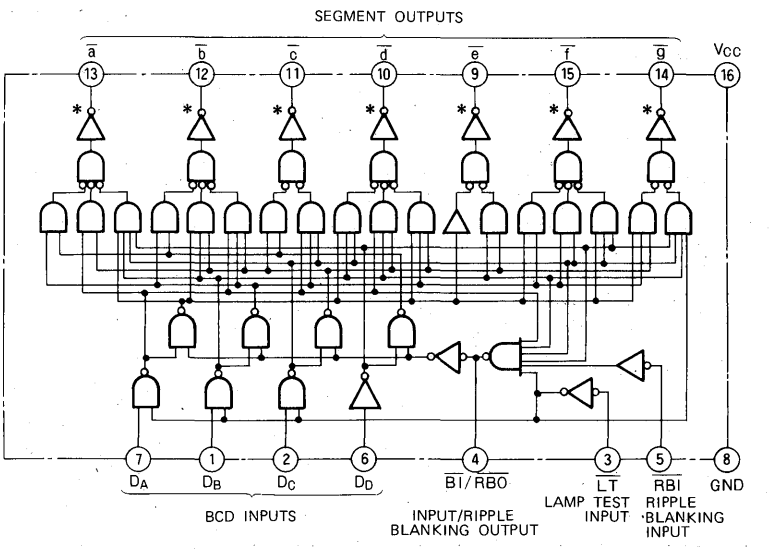
Except for that pins 6 and 9 differ in character from the M74LS47P has exactly the same functions, pin connections and characteristics as the M75LS247P.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

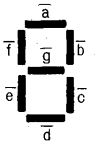
BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-LOW OUTPUT)

FUNCTION TABLE (Note 1)

Decimal number or function	$\overline{LT}$	$\overline{RBI}$	D_D	D_C	D_B	D_A	$\overline{BI}/\overline{RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	Note
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(1)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
Blanking	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(2)
Ripple blanking	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(3)
Lamp test	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(4)

Note 1. (1) $\overline{LT}$ is normally kept in high
$\overline{RBI}$ is kept open or in high with a decimal 0 output.
(2) When $\overline{BI}/\overline{RBO}$ is low, all the segment outputs are high irrespective of the status of the other inputs.
(3) All the segment outputs are set high and $\overline{BI}/\overline{RBO}$ is set low when $\overline{LT}$ is high and $\overline{RBI}$, D_A, D_B, D_C and D_D are low.
(4) When $\overline{LT}$ is low, all the segment outputs are low.
X: Irrelevant

DEFINITION OF SEGMENTS



CHARACTERS DISPLAYED

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Character	0	1	2	3	4	5	6	7	8	9	c	ɔ	u	⊆	t	

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	Input $\overline{BI}/\overline{RBO}$		−0.5 ~ V_{CC}	V
		Other inputs		−0.5 ~ +15	V
V_O	Output voltage	Output $\overline{BI}/\overline{RBO}$	High-level state	−0.5 ~ V_{CC}	V
		Other outputs		−0.5 ~ +15	V
$I_{O(peak)}$	Output current		tw ≦ 1ms, dutycycle ≦ 10%	200	mA
I_O	Output current		High-level state	1	mA
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-LOW OUTPUT)

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current, outputs $\overline{a} \sim \overline{g}$	V_{OH} = 15 V	0		250	μA
I_{OH}	High-level output current, output $\overline{BI}/\overline{RBO}$	$V_{OH} \geqq 2.4$ V	0		−50	μA
I_{OL}	Low-level output current, outputs $\overline{a} \sim \overline{g}$	$V_{OL} \leqq 0.4$ V	0		12	mA
		$V_{OL} \leqq 0.5$ V	0		24	mA
I_{OL}	Low-level output current, output $\overline{BI}/\overline{RBO}$	$V_{OL} \leqq 0.4$ V	0		1.6	mA
		$V_{OL} \leqq 0.5$ V	0		3.2	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75 V, I_{IC} = −18 mA				−1.5	V
V_{OH}	High-level output voltage, output $\overline{BI}/\overline{RBO}$		V_{CC} = 4.75 V	I_{OH} = −50 μA	2.4	4.2		V
I_{OH}	High-level output current, outputs $\overline{a} \sim \overline{g}$		V_I = 0.8 V, V_I = 2 V	V_O = 15 V			250	μA
V_{OL}	Low-level output voltage	Outputs $\overline{a} \sim \overline{g}$	V_{CC} = 4.75 V, V_I = 0.8 V, V_I = 2 V	I_{OL} = 12 mA		0.25	0.4	V
				I_{OL} = 24 mA		0.35	0.5	
		Outputs $\overline{BI}/\overline{RBO}$		I_{OL} = 1.6 mA		0.25	0.4	
				I_{OL} = 3.2 mA		0.35	0.5	
I_{IH}	High-level input voltage, except input $\overline{BI}/\overline{RBO}$		V_{CC} = 5.25 V, V_I = 2.7 V				20	μA
			V_{CC} = 5.25 V, V_I = 10 V				0.1	mA
I_{IL}	Low-level input current	Input $\overline{BI}/\overline{RBO}$	V_{CC} = 5.25 V, V_I = 0.4 V				−1.2	mA
		Other inputs					−0.4	mA
I_{OS}	Short-circuit output current, output $\overline{BI}/\overline{RBO}$		V_{CC} = 5.25 V, V_O = 0 V		−0.3		−2	mA
I_{CC}	Supply current		V_{CC} = 5.25 V (Note 2)			7	13	mA

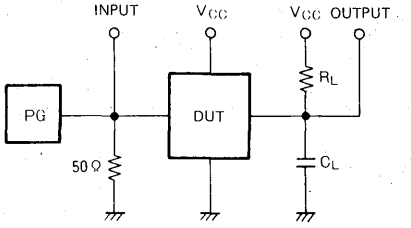
* : All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2: I_{CC} is measured with all inputs at 4.5V.

SWITCHING CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D_A to outputs $\overline{a} \sim \overline{g}$	R_L = 665Ω, C_L = 15 pF (Note 3)		35	100	ns
t_{PHL}				30	100	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{RBI}$ to outputs $\overline{a} \sim \overline{f}$			50	100	ns
t_{PHL}				45	100	ns

Note 3: Measurement circuit

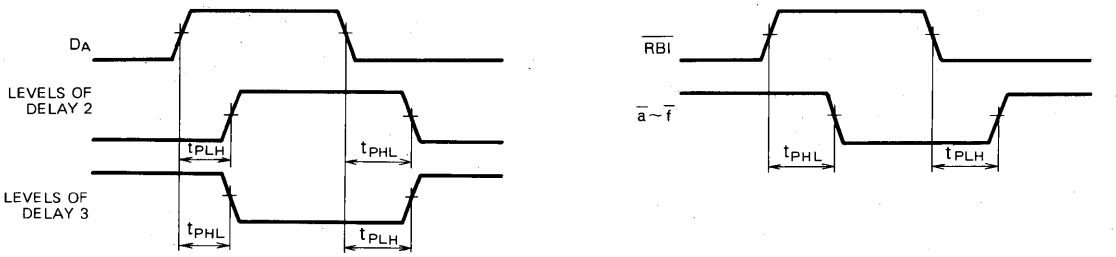


(1) *The pulse generator (PG) has the following characteristics:*
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω.

(2) C_L includes probe and jig capacitance.

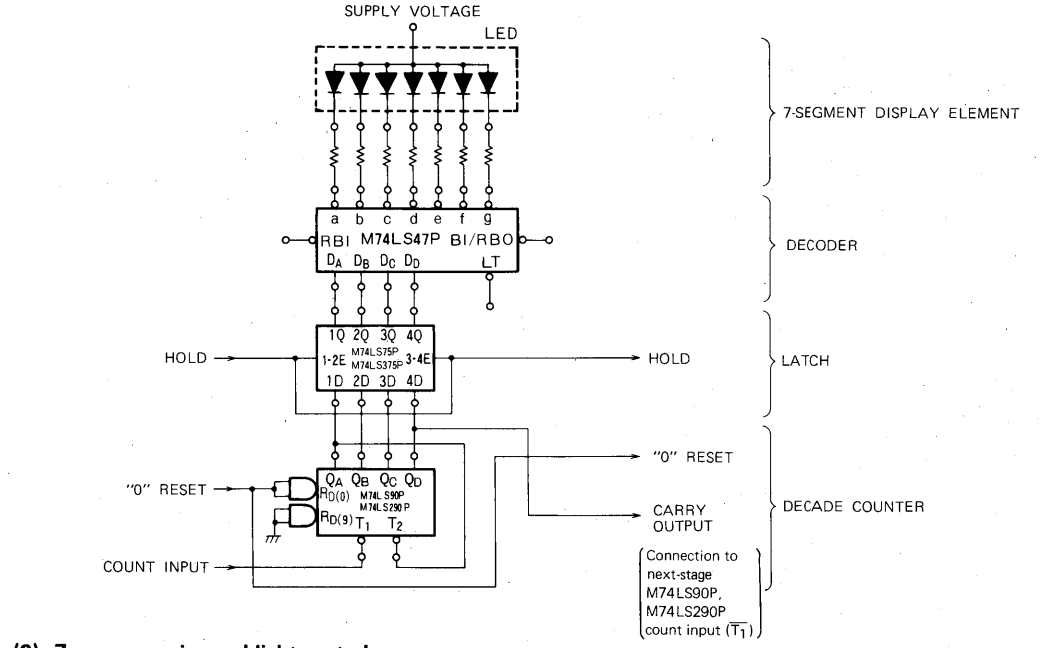
BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-LOW OUTPUT)

TIMING DIAGRAM (Reference level = 1.3V)

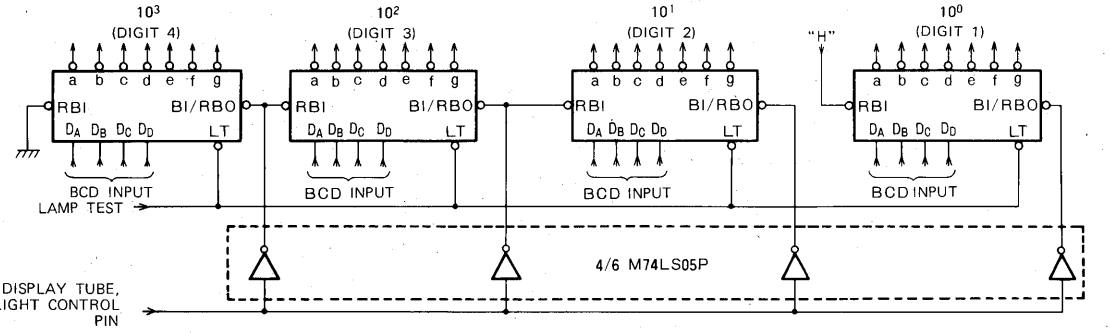


APPLICATION EXAMPLES

(1) Counter using M74LS47P



(2) Zero suppression and light control



M74LS48P

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

DESCRIPTION

The M74LS48P is a semiconductor integrated circuit provided with BCD-to-7-segment decoder/driver function.

FEATURES

- Suitable for 7-segment display element lighting
- $\overline{RBI}$ input and $\overline{BI}/\overline{RBO}$ output for zero suppression
- $\overline{LT}$ input for lamp testing
- $\overline{BI}/\overline{RBO}$ input for extinguishing all segments
- NPN transistor can be externally mounted for High-current drive.
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

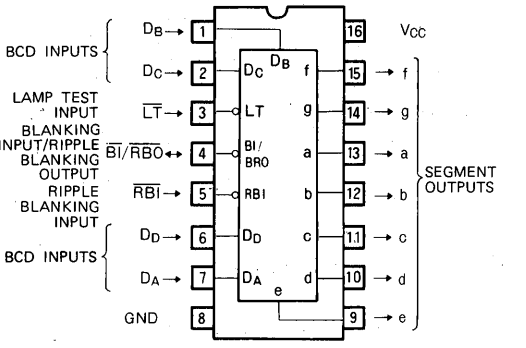
This device resembles the M74LS47P without the output transistors and when a number is specified in BCD code for BCD inputs D_A, D_B, D_C and D_D, segment outputs a~g are set high in accordance with that number. Outputs a~g contain 2Ω pull-up resistors which are suitable for driving common-cathode LEDs. By connecting an NPN transistor to these outputs, it is possible to drive high current display elements.

The ripple blanking, blanking and lamp test functions are the same as those for the M74LS47P.

Refer to the M74LS47P for the application example.

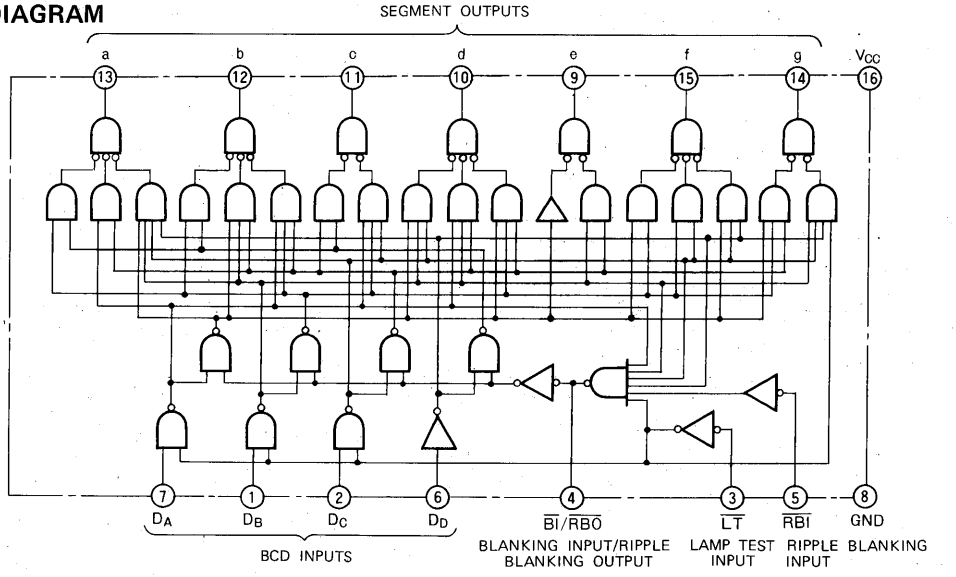
Except for that pins 6 and 9 differ in character form the M74LS48P has exactly the same functions, pin connections and characteristics as the M74LS248P.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

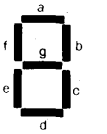
BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

FUNCTION TABLE (Note 1)

Decimal number or function	$\overline{LT}$	$\overline{RBI}$	D_D	D_C	D_B	D_A	$\overline{BI}/\overline{RBO}$	a	b	c	d	e	f	g	Note
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	(1)
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
Blanking	X	X	X	X	X	X	L	L	L	L	L	L	L	L	(2)
Ripple blanking	H	L	L	L	L	L	L	L	L	L	L	L	L	L	(3)
Lamp test	L	X	X	X	X	X	H	H	H	H	H	H	H	H	(4)

Note 1: (1) $\overline{LT}$ is normally kept in high.
$\overline{RBI}$ is kept open or in high with a decimal 0 output.
(2) When $\overline{BI}/\overline{RBO}$ is low, all the segment outputs are low irrespective of the status of the other inputs.
(3) All the segment outputs are set high and $\overline{BI}/\overline{RBO}$ is set low when $\overline{LT}$ is high and $\overline{RBI}$, D_A, D_B, D_C and D_D are low.
(4) When $\overline{LT}$ is low, all the segment outputs are high.
X: Irrelevant

DEFINITION OF SEGMENTS



CHARACTERS DISPLAYED

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Character	0	1	2	3	4	5	6	7	8	9	c	ɔ	u	⊆	t	

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	Input $\overline{BI}/\overline{RBO}$		−0.5 ~ V_{CC}	V
		Other inputs		−0.5 ~ +15	V
V_O	Output voltage	Output $\overline{BI}/\overline{RBO}$	High-level state	−0.5 ~ V_{CC}	V
		Other outputs		−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current, outputs a ~ g	$V_{OH} \geqq 2.4V$	0		−100	μA
I_{OH}	High-level output current, output $\overline{BI}/\overline{RBO}$	$V_{OH} \geqq 2.4V$	0		−50	μA
I_{OL}	Low-level output current, outputs a ~ g	$V_{OL} \leqq 0.4V$	0		2	mA
		$V_{OL} \leqq 0.5V$	0		6	mA
I_{OL}	Low-level output current, output $\overline{BI}/\overline{RBO}$	$V_{OL} \leqq 0.4V$	0		1.6	mA
		$V_{OL} \leqq 0.5V$	0		3.2	mA

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +70°C$, unless otherwise noted)

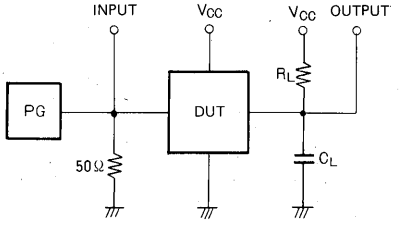
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	Outputs a ~ g	$V_{CC}=4.75V$	$I_{OH}=-100\mu A$	2.4	4.2		V
		Output $\overline{BI}/\overline{RBO}$	$V_I=0.8V$, $V_I=2V$	$I_{OH}=-50\mu A$	2.4	4.2		V
I_{OH}	High-level output current	Outputs a ~ g	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $V_O=0.85V$		−1.3	−2		mA
V_{OL}	Low-level output voltage	Outputs a ~ g	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=2mA$		0.25	0.4	V
				$I_{OL}=6mA$		0.35	0.5	V
		Output $\overline{BI}/\overline{RBO}$		$I_{OL}=1.6mA$		0.25	0.4	V
				$I_{OL}=3.2mA$		0.35	0.5	V
I_{IH}	High-level input current	Inputs other than $\overline{BI}/\overline{RBO}$	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
			$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	Input $\overline{BI}/\overline{RBO}$	$V_{CC}=5.25V$, $V_I=0.4V$				−1.2	mA
		Other inputs					−0.4	mA
I_{OS}	Short-circuit output current	Output $\overline{BI}/\overline{RBO}$	$V_{CC}=5.25V$, $V_O=0V$		−0.3		−2	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 2)			25	38	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.
Note 2: I_{CC} is measured with all inputs at 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

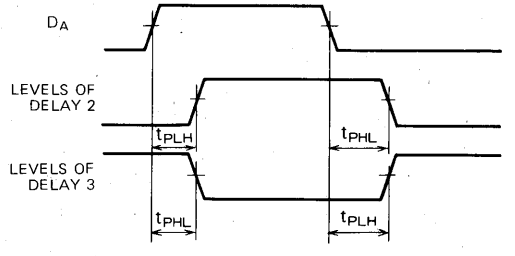
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D_A to outputs a ~ g	$R_L=4k\Omega$, $C_L=15pF$ (Note 3)		30	100	ns
t_{PHL}				30	100	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{RBI}$ to outputs a ~ f	$R_L=6k\Omega$, $C_L=15pF$ (Note 3)		40	100	ns
t_{PHL}				45	100	ns

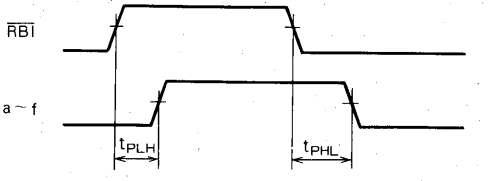
Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, $V_P=3V_{P\text{-}P}$, $Z_O=50\Omega$.
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)





M74LS51P

DUAL 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE

DESCRIPTION

The M74LS51P is a semiconductor integrated circuit containing dual 2-wide 2-input/3-input AND-OR-INVERT gates.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d=5.5mW typical)
- High speed (t_{pd}=7ns typical)
- Low output impedance
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

Schottky TTL technology enables input high breakdown voltage, high speed, low power dissipation and high fan-out.

This device consists of a NOR gate with two 2-input AND gates as the inputs and a NOR gate with two 3-input AND gates as the inputs, and the following logical expressions are yielded:

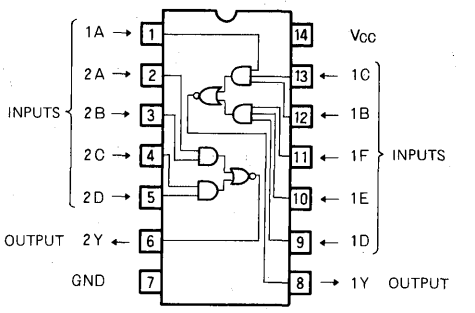
$$1Y = \overline{1A \cdot 1B \cdot 1C + 1D \cdot 1E \cdot 1F}$$
$$2Y = \overline{2A \cdot 2B + 2C \cdot 2D}$$

FUNCTION TABLE

M	N	Y
L	L	H
H	L	L
L	H	L
H	H	L

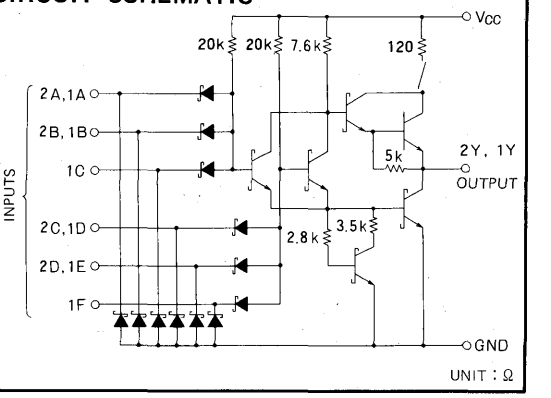
M=1A·1B·1C
N=1D·1E·1F
AND-OR
M=2A·2B
N=2C·2D

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

DUAL 2-WIDE 2-INPUT/3-INPUT AND-OR-INVERT GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

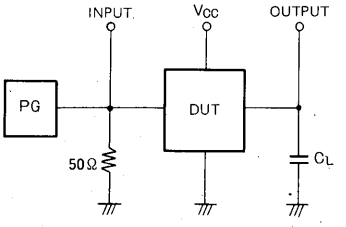
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
			$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=0V$			0.8	1.6	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=4.5V$			1.4	2.8	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25°C$).
Note 1: All measurements must be done quickly and not more than one output should be shorted at a time.

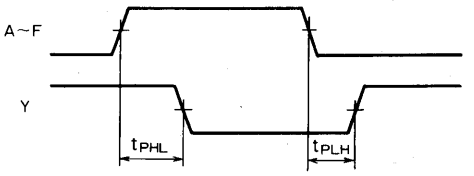
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	$C_L=15pF$		6	20	ns
t_{PHL}	High-to-low-level output propagation time	(Note 2)		8	20	ns

Note 2: Measurement circuit



TIMING DIAGRAM (Reference level = 1.3V)



(1) The pulse generator (PG) has the following characteristics:
PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance.

M74LS73AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH RESET

DESCRIPTION

The M74LS73AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input $\overline{T}$, inputs J and K and direct reset input $\overline{R_D}$.

FEATURES

- Negative edge-triggering
- Each flip-flop can be used independently
- Direct reset input
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

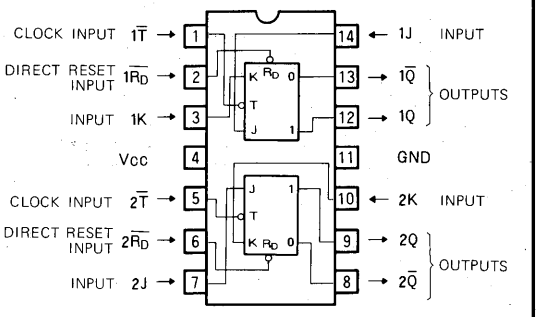
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While $\overline{T}$ is high, signals J and K are put in the read-in state, and when $\overline{T}$ changes from high to low, the J and K signals immediately before the change emerge in outputs Q and $\overline{Q}$ in accordance with the function table. By setting $\overline{R_D}$ low, Q and $\overline{Q}$ are set low and high respectively irrespective of the status of the other input signals. For use as a J-K flip-flop, $\overline{R_D}$ must be kept high.

Also available is M74LS107AP with the same functions and electrical characteristics. This offers easy mounting with V_{CC} positioned at pin 14 and GND at pin 7.

PIN CONFIGURATION (TOP VIEW)



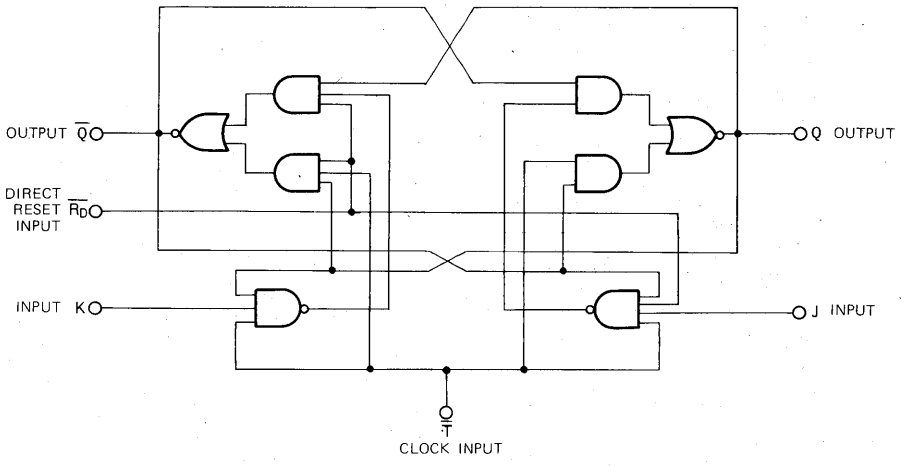
Outline 14P4

FUNCTIONAL TABLE (Note 1)

$\overline{T}$	$\overline{R_D}$	J	K	Q	$\overline{Q}$
X	L	X	X	L	H
↓	H	H	H	Toggle	
↓	H	L	H	L	H
↓	H	H	L	H	L
↓	H	L	L	Q^0	$\overline{Q^0}$
H	H	X	X	Q^0	$\overline{Q^0}$

Note 1 ↓ : Transition from high to low-level (negative edge trigger)
X : Irrelevant
Q^0 : level of Q before the indicated steady-state input conditions were established.
$\overline{Q^0}$: level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Toggle : complement of previous state with ↓ transition of outputs

BLOCK DIAGRAM (EACH FLIP-FLOP)



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH RESET

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V, V_I = 0.8V, V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V, V_I = 0.8V, V_I = 2V	I_{OL} = 4mA		0.25	0.4	V
				I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	J, K	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		$\overline{R_D}$					60	μA
		$\overline{T}$					80	μA
		J, K	V_{CC} = 5.25V, V_I = 10V				0.1	mA
		$\overline{R_D}$					0.3	mA
		$\overline{T}$					0.4	mA
I_{IL}	Low-level input current	J, K	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
		$\overline{R_D}$ $\overline{T}$					−0.8	mA
I_{OS}	Short-circuit output current (Note 2)		V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25V (Note 3)			4	6	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

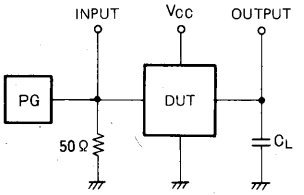
Note 3: Supply current measurements should be done with Q and $\overline{Q}$ set alternately high and $\overline{T}$ should be set low during actual measurement.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L = 15pF (Note 4)	30	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{T}$ to Q, $\overline{Q}$			8	20	ns
t_{PHL}				6	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{R_D}$ to Q, $\overline{Q}$			10	20	ns
t_{PHL}				7	20	ns

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH RESET

Note 4: Measurement circuit

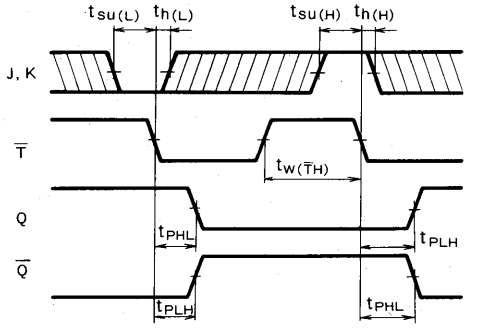


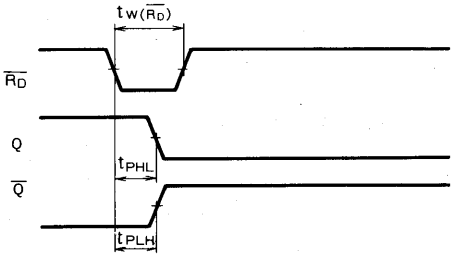
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = 3V_{P-P}, Z_o = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T}H)}$	Clock input $\overline{T}$ high pulse width		20	12		ns
$t_{w(\overline{R_D})}$	Direct reset input pulse width		25	4		ns
t_r	Clock rise time			650	100	ns
t_f	Clock fall time			900	100	ns
$t_{su(H)}$	Setup time high $\overline{T}$ to J, K		20	9		ns
$t_{su(L)}$	Setup time low $\overline{T}$ to J, K		20	10		ns
$t_{h(H)}$	Hold time high $\overline{T}$ to J, K		0	− 8		ns
$t_{h(L)}$	Hold time low $\overline{T}$ to J, K		0	− 5		ns

TIMING DIAGRAM (Reference level = 1.3V)

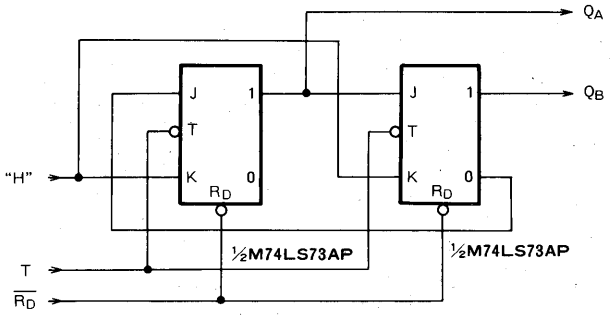


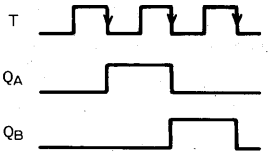


Note: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

High-speed 1/3 divider





M74LS74AP

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

DESCRIPTION

The M74LS74AP is a semiconductor intergrated circuit containing 2 D-type positive edge-triggered flip-flop circuits with discrete terminals for clock input T, data input D and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Each flip-flop can be used independently.
- Direct set and reset inputs
- Positive edge-triggering
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20 ~ +75°C)

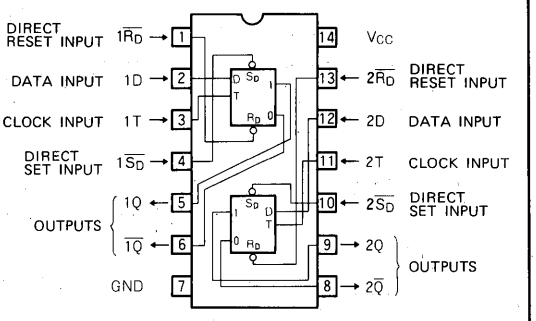
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

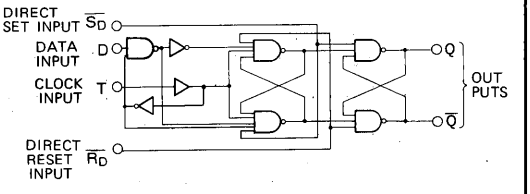
When T changes from low to high, the D signal immediately before the change emerges in outputs Q and $\overline{Q}$ in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$, this IC can be made into a direct R-S flip-flop. When both S_D and R_D are low, Q = $\overline{Q}$ = high. However, when both of them change to high at the same time, the status of Q and $\overline{Q}$ cannot be anticipated. For use as a D-type filip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

LOGIC DIAGRAM (EACH FLIP-FLOP)



FUNCTION TABLE

$\overline{S_D}$	$\overline{R_D}$	T	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H *	H *
H	H	L	X	Q^0	$\overline{Q}^0$
H	H	↑	H	H	L
H	H	↑	L	L	H

Note 1: ↑ : Transition from low to high-level

Q^0 : level of Q before the indicated steady-state input conditions were established.

$\overline{Q}^0$: level of $\overline{Q}$ before the indicated steady-state input conditions were established.

X : Irrelevant

* : Nonstable; it will not persist when $\overline{R_D}$, $\overline{S_D}$ inputs return to their inactive (high) level.

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +5.5	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	D, T	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{S_D}$, $\overline{R_D}$					40	
		D, T	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{S_D}$, $\overline{R_D}$					0.2	
I_{IL}	Low-level input current	D, T	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$\overline{S_D}$, $\overline{R_D}$					−0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$, (Note 3)			4	8	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

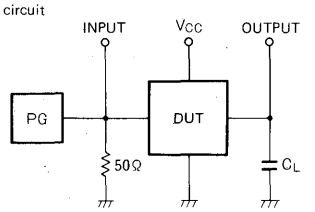
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: Measurement circuit

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L=15pF$ (Note 4)	25	50		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from T to Q, $\overline{Q}$			11	25	ns
t_{PHL}				11	40	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{S_D}$, $\overline{R_D}$ to Q, $\overline{Q}$			8	25	ns
t_{PHL}				11	40	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$

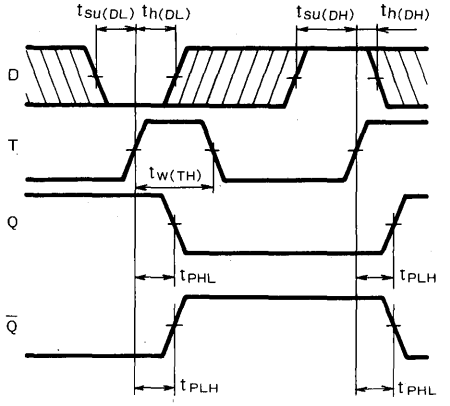
(2) C_L includes probe and jig capacitance.

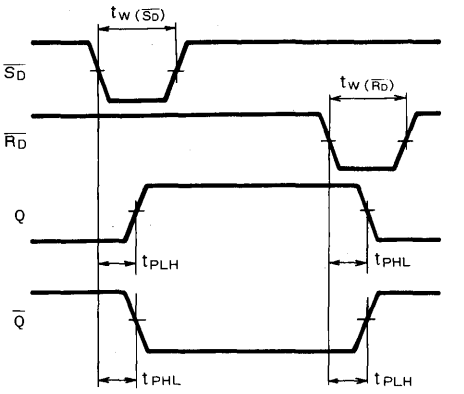
DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOPS WITH SET AND RESET

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(TH)}$	Clock input T high pulse width		25	4		ns
$t_{w(\overline{SD},\overline{RD})}$	Direct set and reset inputs $\overline{S_D}$, $\overline{R_D}$ pulse width		25	4		ns
$t_{su(DH)}$	Setup time high D to T		20	10		ns
$t_{su(DL)}$	Setup time low D to T		20	8		ns
$t_{h(DH)}$	Hold time high D to T		5	− 5		ns
$t_{h(DL)}$	Hold time low D to T		5	− 5		ns

TIMING DIAGRAM (Reference level = 1.3V)

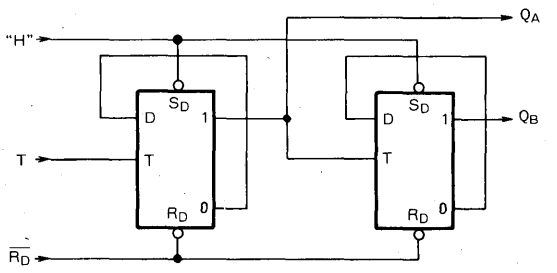


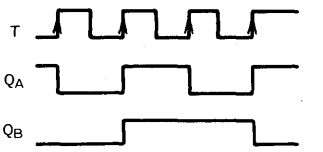


Note 4: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

¼divider





MITSUBISHI ELECTRIC

M74LS75P

4-BIT BISTABLE LATCH

DESCRIPTION

The M74LS75P is a semiconductor integrated circuit containing 4 bistable latch circuits and is provided with outputs Q and $\overline{Q}$.

FEATURES

- Enable inputs common to two circuits each
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

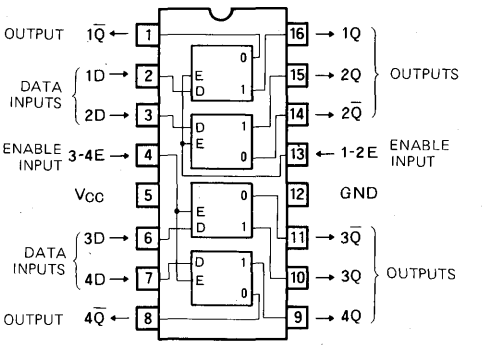
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 4 D-type latch circuits and is provided with enable inputs E common to 2 circuits each. When E is high, the information from the data input D appears in the outputs Q and $\overline{Q}$. When the D signal changes, the signal that appears in outputs Q and $\overline{Q}$ also changes. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q and $\overline{Q}$ does not change even if D is changed.

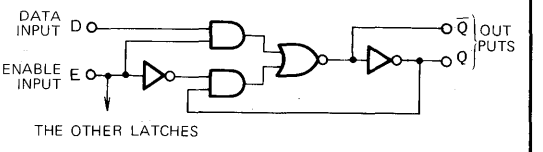
Also provided is the M74LS375P with the same functions and electrical characteristics. With the V_{CC} positioned at pin 16 and GND at pin 8, this device makes for easy mounting.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM (EACH LATCH)



FUNCTION TABLE (Note 1)

E	D	Q	$\overline{Q}$
H	H	H	L
H	L	L	H
L	X	Q^0	$\overline{Q^0}$

Note 1 Q^0, $\overline{Q^0}$: Level of Q and $\overline{Q}$ before the indicated steady-state input conditions were established.

X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V, I_{OH}=−400μA		2.7	3.5		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V	I_{OL}=4mA		0.25	0.4	V
				I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	D	V_{CC}=5.25V, V_I=2.7V				20	μA
		E					80	
		D	V_{CC}=5.25V, V_I=10V				0.1	mA
		E					0.4	
I_{IL}	Low-level input current	D	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
		E					−1.6	
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 3)			6.3	12	mA

* : All typical values are at V_{CC}=5V, Ta=25℃

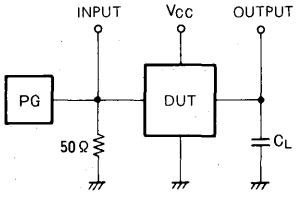
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output Q	C_L=15pF (Note 4)		12	27	ns
t_{PHL}				8	17	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output $\overline{Q}$			10	20	ns
t_{PHL}				6	15	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output Q			13	27	ns
t_{PHL}				12	25	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output $\overline{Q}$			12	30	ns
t_{PHL}				6	15	ns

Note 4: Measurement circuit



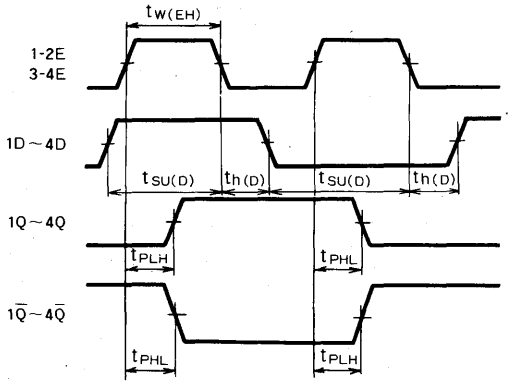
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = 3V_{P-P}, Z_O = 50Ω.

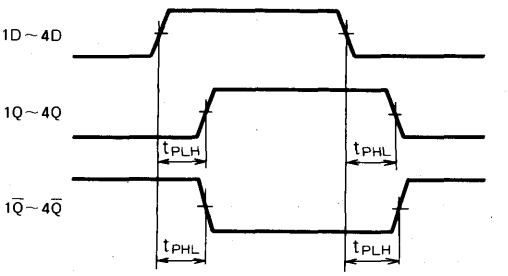
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(EH)}$	Enable input E high pulse width		20	7		ns
$t_{SU(D)}$	Setup time 1D ~ 4D to E		20	12		ns
$t_{h(D)}$	Hold time 1D ~ 4D to E		8	5		ns

TIMING DIAGRAM (Reference level = 1.3V)





High-level 3-4E, 1-2E

M74LS76AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

DESCRIPTION

The M74LS76AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input $\overline{T}$, inputs J and K and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Negative edge-triggering
- Each fli-flop can be used independently
- Direct set and reset inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

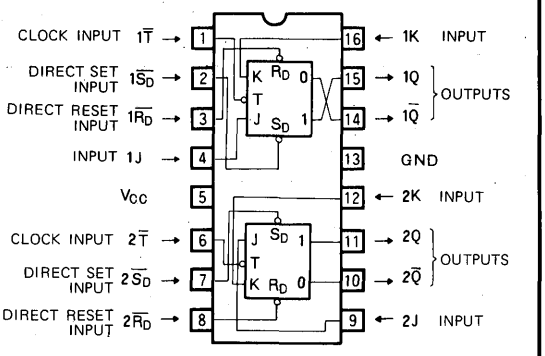
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While $\overline{T}$ is high, signals J and K are put in the read-in state, and when $\overline{T}$ changes from high to low, the J and K signals immmediately before the change emerge in outputs Q and $\overline{Q}$ in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$ this IC can be made into a direct R-S flip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, Q = $\overline{Q}$ = high. However, when both of them change to high at the same time, the status of Q and $\overline{Q}$ cannot be anticipated. For use as a J-K flip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high.

Also available is M74LS112AP with the same functions and electrical characteristics. This offers easy mounting with V_{CC} positioned at pin 16 and GND at pin 8.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{T}$	$\overline{S_D}$	$\overline{R_D}$	J	K	Q	$\overline{Q}$
X	L	H	X	X	H	L
X	H	L	X	X	L	H
X	L	L	X	X	H*	H*
↓	H	H	H	H	Toggle	
↓	H	H	L	H	L	H
↓	H	H	H	L	H	L
↓	H	H	L	L	Q^0	$\overline{Q^0}$
H	H	H	X	X	Q^0	$\overline{Q^0}$

Note 1 ↓ : Transition from high to low-level (negative edge trigger)

X : Irrelevant

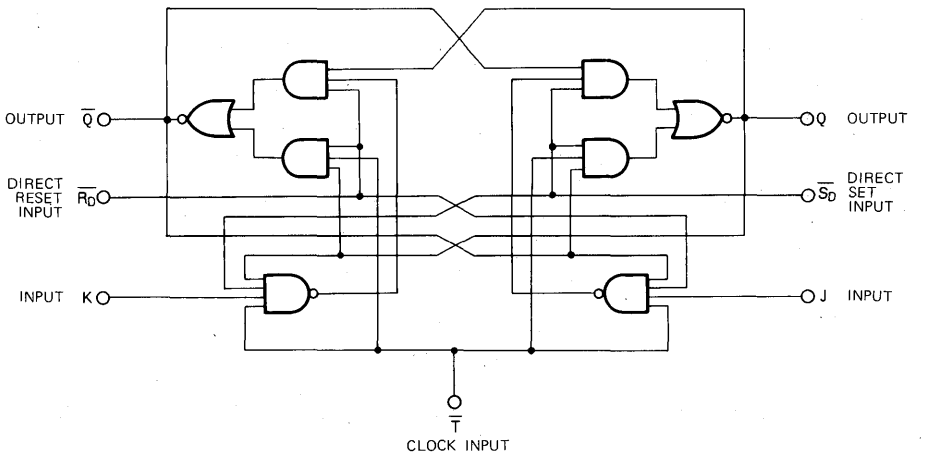
* : Q = $\overline{Q}$ = high when $\overline{S_D}$ = $\overline{R_D}$ = low and so when both $\overline{S_D}$ and $\overline{R_D}$ are set high, the status of Q and $\overline{Q}$ cannot be anticipated.

Q^0: level of Q before the indicated steady-state input conditions were established.

$\overline{Q^0}$: level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Toggle : Complement of previous state with ↓ transition of outputs

BLOCK DIAGRAM (EACH FLIP-FLOP)



MITSUBISHI ELECTRIC

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	High-level input current		V_{CC} = 4.75V	I_{OL} = 4mA		0.25	0.4	V
			V_I = 0.8V, V_I = 2V	I_{OL} = 8mA		0.35	0.5	V
I_{IH}	Low-level input current	J, K	V_{CC} = 5.25V V_I = 2.7V				20	μA
		$\overline{S_D}$, $\overline{R_D}$					60	
		$\overline{T}$					80	
		J, K	V_{CC} = 5.25V V_I = 10V				0.1	mA
		$\overline{S_D}$, $\overline{R_D}$					0.3	
		$\overline{T}$					0.4	
I_{IL}	Low-level output voltage	J, K	V_{CC} = 5.25V				−0.4	mA
		$\overline{S_D}$, $\overline{R_D}$, $\overline{T}$	V_I = 0.4V (Note 2)				−0.8	
I_{OS}	Short-circuit output current (note 3)		V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25V (Note 4)			4	6	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C

Note 2: $\overline{S_D}$ and $\overline{R_D}$ should not both be set to 0.4V simultaneously.

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: Supply current measurements should be done with Q and $\overline{Q}$ set alternately high and $\overline{T}$ should be set low during actual measurement.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

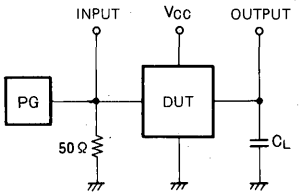
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L = 15pF (Note 5)	30	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{T}$ to Q, $\overline{Q}$			6	20	ns
t_{PHL}				7	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{S_D}$, $\overline{R_D}$ to Q, $\overline{Q}$			7	20	ns
t_{PHL}				7	20	ns

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

TIMING REQUIREMENTS (V_{CC}= 5 V, Ta=25℃, unless otherwise noted)

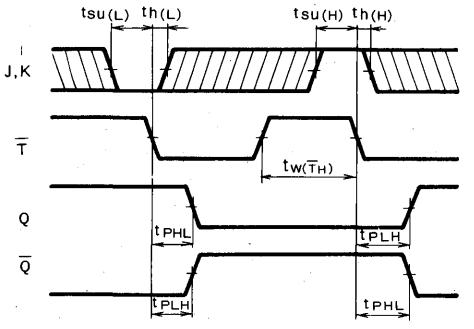
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T}H)}$	Clock input $\overline{T}$ high pulse width		20	12		ns
$t_{w(\overline{S}D,\overline{R}D)}$	Direct set, reset pulse width		25	4		ns
t_r	Clock rise time			650	100	ns
t_f	Clock fall time			900	100	ns
$t_{su(H)}$	Setup time high J, K to $\overline{T}$		20	12		ns
$t_{su(L)}$	Setup time low J, K to $\overline{T}$		20	12		ns
$t_{h(H)}$	Hold time high J, K to $\overline{T}$		0	− 10		ns
$t_{h(L)}$	Hold time low J, K to $\overline{T}$		0	− 6		ns

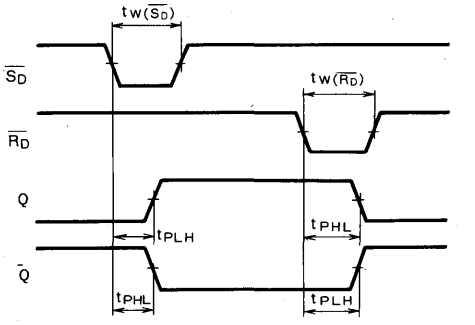
Note 5: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)





Note: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS83AP

4-BIT BINARY FULL ADDER WITH FAST CARRY

DESCRIPTION

The M74LS83AP is a semiconductor integrated circuit containing a 4-bit binary look ahead carry type full adder.

FEATURES

- High speed with look-ahead carry addition
- Possible configuration of systems with partial look-ahead carry
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

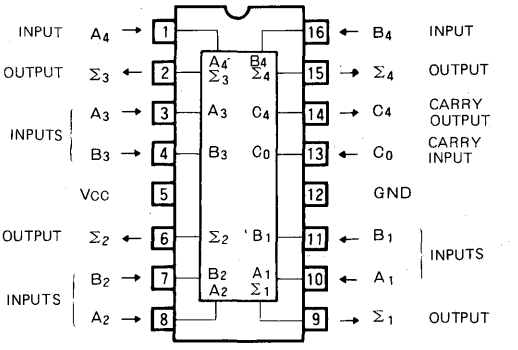
FUNCTIONAL DESCRIPTION

This device performs the addition of two 4-bit binary numbers. When a 4-bit binary number is applied to inputs A_1~A_4 and B_1~B_4 and the carry signal from the previous digit is applied to input C_0, the respective bit sum output and carry outputs for the next upper digit appear in outputs Σ_1~Σ_4 and C_4.

This adder features full internal look ahead across all four bits generating the carry term in 8ns typically. Therefor, the carry output can be obtained in a delay time of 8Nns when N-stages are connected and a 4N-bit parallel adder is configured. (Refer to application example.)

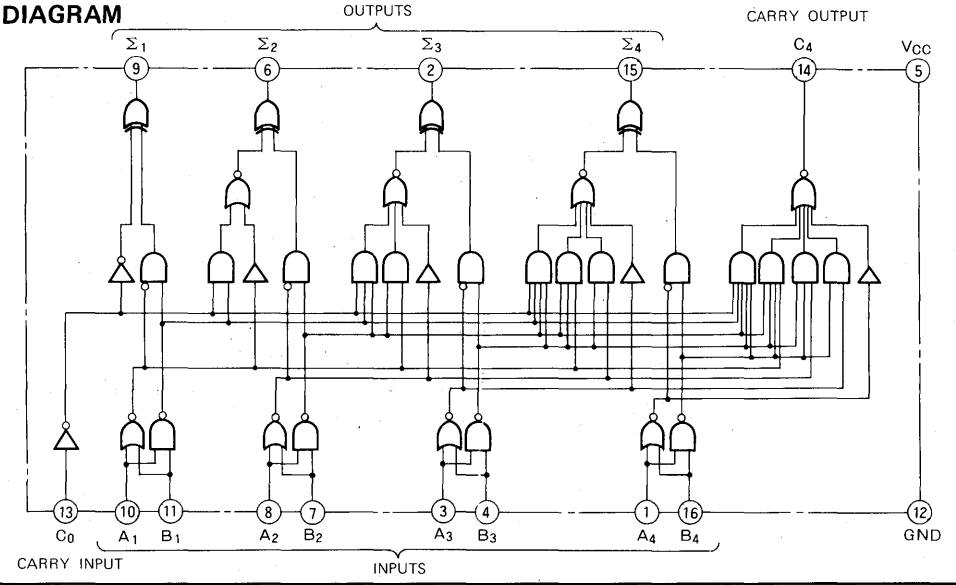
Also available is the M74LS283P with the same functions and electrical characteristics and with a pin 16 V_{CC} and 8 GND configuration.

PIN CONFIGURATION (TOP VIEW)



Outline 16 P4

BLOCK DIAGRAM



4-BIT BINARY FULL ADDER WITH FAST CARRY

FUNCTION TABLE (Note 1)

C_{k-1}	A_k	B_k	Σ_k	C_k
L	L	L	L	L
L	H	L	H	L
L	L	H	H	L
L	H	H	L	H
H	L	L	H	L
H	H	L	L	H
H	L	H	L	H
H	H	H	H	H

Note 1 C_k and Σ_k are the carry output and sum output obtained by adding A_k, B_k and C_{k-1} (carry input), and they are expressed in the following logical expression.

$\Sigma_k = A_k \oplus B_k \oplus C_{k-1}$

$C_k = A_k \cdot B_k + (A_k + B_k) \cdot C_{k-1}$

Where $k = 1 \sim 4$

$\oplus$ = Exclusive OR

$+$ = OR

$\cdot$ = AND

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20 \sim +75$	°C
Tstg	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC} = 4.75V$, $I_{IC} = -18mA$				-1.5	V
V_{OH}	High-level output voltage		$V_{CC} = 4.75V$, $V_I = 0.8V$ $V_I = 2V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = 4.75V$	$I_{OL} = 4mA$		0.25	0.4	V
			$V_I = 0.8V$, $V_I = 2V$	$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	C_0	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$A_1 \sim A_4$, $B_1 \sim B_4$					40	
		C_0	$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
		$A_1 \sim A_4$, $B_1 \sim B_4$					0.2	
I_{IL}	Low-level input current	C_0	$V_{CC} = 5.25V$, $V_I = 0.4V$				-0.4	mA
		$A_1 \sim A_4$, $B_1 \sim B_4$					-0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC} = 5.25V$, $V_O = 0V$		-20		-100	mA
I_{CC}	Supply current		$V_{CC} = 5.25V$, $V_I = 0V$			22	39	mA
			$V_{CC} = 5.25V$, $V_I = 0V$, $V_I = 4.5V$ (Note 3)			19	34	mA
			$V_{CC} = 5.25V$, $V_I = 4.5V$			19	34	mA

* : All typical values are at $V_{CC} = 5V$, $T_a = 25°C$.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

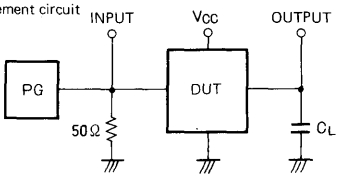
Note 3: Measurement should be conducted with inputs $B_1 - B_4$ at 0V and the other inputs at 4.5V.

4-BIT BINARY FULL ADDER WITH FAST CARRY

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

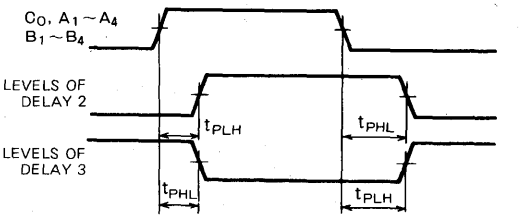
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input C_0 to outputs $\Sigma_1 \sim \Sigma_4$	C_L=15pF (Note 4)		12	24	ns
t_{PHL}				13	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $A_1 \sim A_4$, $B_1 \sim B_4$ to outputs $\Sigma_1 \sim \Sigma_4$			9	24	ns
t_{PHL}				11	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input C_0 to output C_4			8	17	ns
t_{PHL}				8	22	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $A_1 \sim A_4$, $B_1 \sim B_4$ to output C_4			8	17	ns
t_{PHL}				8	17	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3$V_{P\text{-}P}$, Z_O=50Ω.
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)

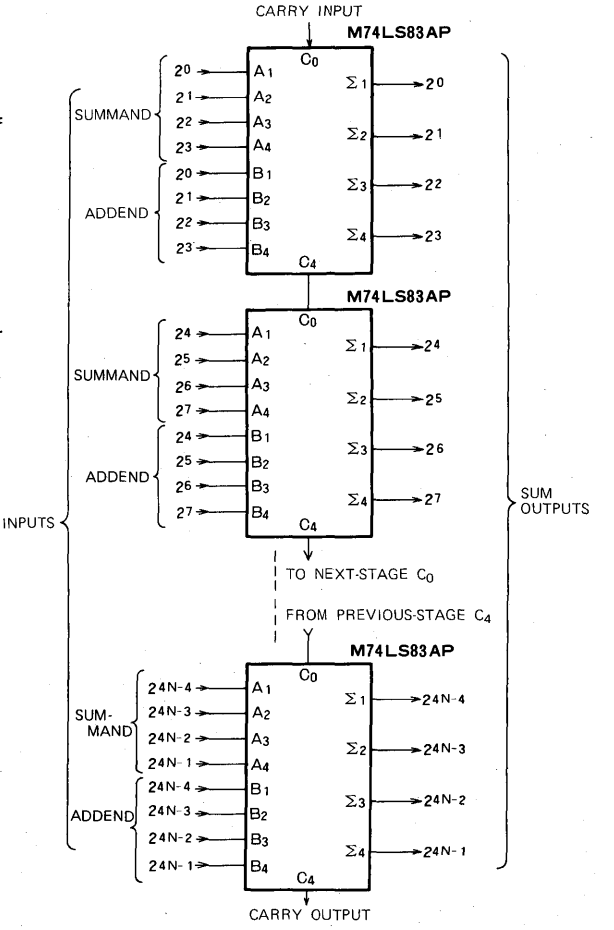


APPLICATION EXAMPLE

Shown on the right is a 4N-bit binary parallel adder using N number of M74LS83AP devices. The typical delay times of the carry output in this circuit are:

N = 1 (4 bits)	10.5ns
N = 2 (8 bits)	21ns
N = 3 (12 bits)	31.5ns
N = 4 (16 bits)	42ns
N = 8 (32 bits)	84ns

This allows a high-speed ripple carry adder to be configured.



M74LS85P

4-BIT MAGNITUDE COMPARATOR

DESCRIPTION

The M74LS85P is a semiconductor integrated circuit containing a 4-bit digital comparator.

FEATURES

- Easy expansion of number of bits
- Binary or BCD comparison
- Wide operating temperature range (T_a=−20~+75°C)

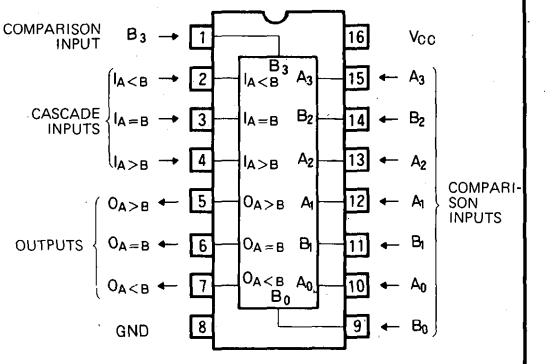
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

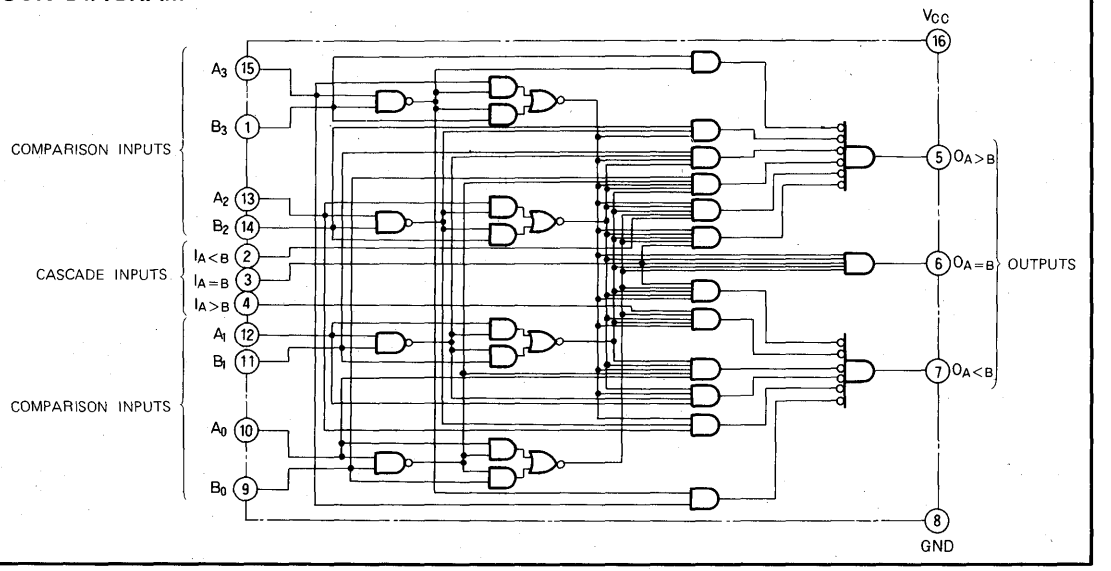
By applying two sets of 4-bit binary numbers A and B to be compared to comparison inputs A_0~A_3 and B_0~B_3 and by setting cascade input $I_{A=B}$ high, high appears in outputs $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ in accordance with the magnitude. This is used for connecting cascade inputs $I_{A>B}$, $I_{A<B}$ and $I_{A=B}$ and increasing the number of bits.
(Refer to application example)

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

4-BIT MAGNITUDE COMPARATOR

FUNCTION TABLE (Note 1)

A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

Note 1. X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta=-20\sim+75℃$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5\sim+7$	V
V_I	Input voltage		$-0.5\sim+15$	V
V_O	Output voltage	High-level state	$-0.5\sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20\sim+75$	℃
Tstg	Storage temperature range		$-65\sim+150$	℃

RECOMMENDED OPERATING CONDITIONS ($Ta=-20\sim+75℃$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH}\geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL}\leqq 0.4V$	0		4	mA
		$V_{OL}\leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
			$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$I_{A<B}$, $I_{A>B}$	$V_{CC}=5.25V$				20	μA
		$A_0\sim A_3, B_0\sim B_3, I_{A=B}$	$V_I=2.7V$				60	
		$I_{A<B}$, $I_{A>B}$	$V_{CC}=5.25V$				0.1	mA
		$A_0\sim A_3, B_0\sim B_3, I_{A=B}$	$V_I=10V$				0.3	
I_{IL}	Low-level input current	$I_{A<B}$, $I_{A>B}$	$V_{CC}=5.25V$				−0.4	mA
		$A_0\sim A_3, B_0\sim B_3, I_{A=B}$	$V_I=0.4V$				−1.2	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 3)			11	20	mA

*: All typical values are at $V_{CC}=5V$, $T_a=25°C$.

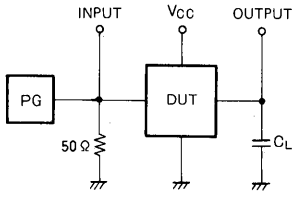
Note 2: All measurements must be done quickly and not more than output should be shorted at a time.

Note 3: I_{CC} is measured with $I_{A=B}$ at 0V and with all other inputs at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs, $A_0 \sim A_3$, $B_0 \sim B_3$ to outputs $O_{A<B}$, $O_{A=B}$, $O_{A>B}$	Number of delay gate steps 1	C_L = 15pF (Note 4)		6		ns
t_{PHL}					11		ns
t_{PLH}		Number of delay gate steps 2			10		ns
t_{PHL}					18		ns
t_{PLH}		Number of delay gate steps 3			12	36	ns
t_{PHL}					20	30	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $A_0 \sim A_3$, $B_0 \sim B_3$ to outputs $O_{A<B}$, $O_{A=B}$, $O_{A>B}$				16	45	ns
t_{PHL}					20	45	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $I_{A=B}$ to outputs $O_{A<B}$, $O_{A>B}$				6	22	ns
t_{PHL}					12	17	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $I_{A=B}$ to output $O_{A=B}$				7	20	ns
t_{PHL}					13	26	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $I_{A<B}$, $I_{A>B}$ to outputs $O_{A<B}$, $O_{A=B}$, $O_{A>B}$				9	22	ns
t_{PHL}					15	17	ns

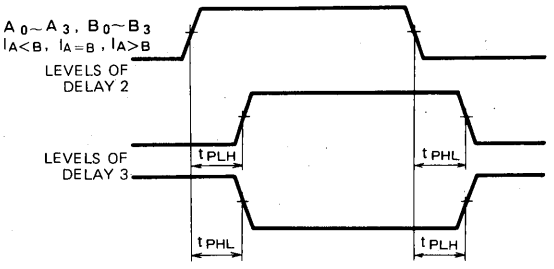
Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P=3V_{P-P}, Z_O = 50Ω.

(2) C_L includes probe and jig capacitance.

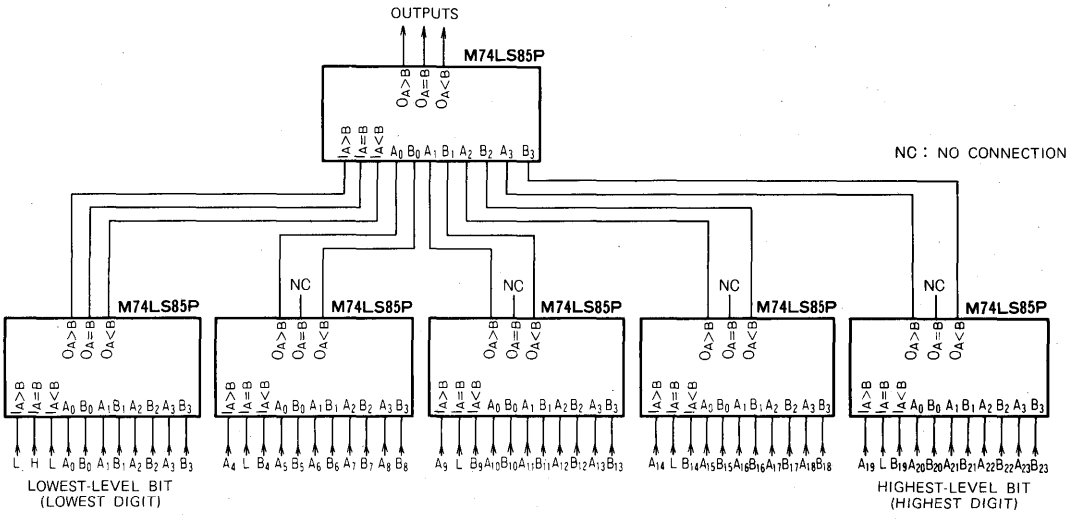
TIMING DIAGRAM (Reference level = 1.3V)



MITSUBISHI ELECTRIC

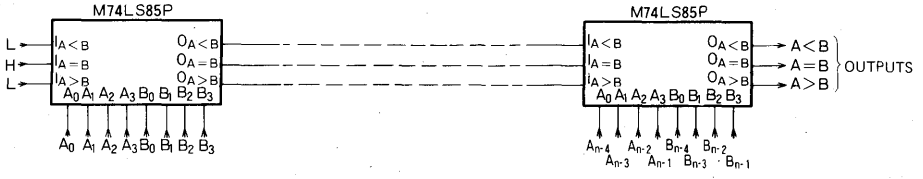
APPLICATION EXAMPLES

(1) Shown below is a 24-bit (digital) comparator using the M74LS85P. Expansion is possible up to n bits using this type of cascade connection.



NC : NO CONNECTION

(2) Shown below is an n-bit comparator using the M74LS85P. The speed is decreases as the number of bits in the configuration below increases. configuration below.



M74LS86P

QUADRUPLE 2-INPUT EXCLUSIVE OR GATES

DESCRIPTION

The M74LS86P is a semiconductor integrated circuit containing 4 dual-input exclusive-OR gates.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation ($P_d = 30.5mW$ typical)
- High speed ($t_{pd} = 10ns$ typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

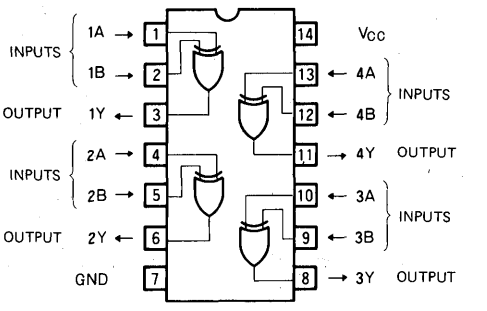
The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out.

When both inputs A and B either low or high, output Y is low, and when A and B are high and low or low and high respectively, Y is high.

FUNCTION TABLE

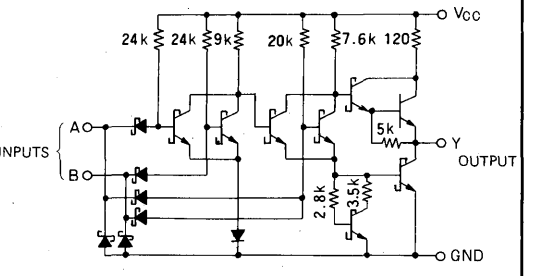
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

MITSUBISHI ELECTRIC

QUADRUPLE 2-INPUT EXCLUSIVE OR GATES

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

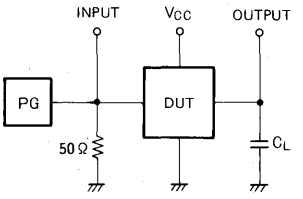
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
		V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				40	μA
		V_{CC}=5.25V, V_I=10V				0.2	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.8	mA
I_{OS}	Short-circuit output current (Note 1)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 2)			6.1	10	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.
Note 2: I_{CC} is measured with all inputs grounded.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

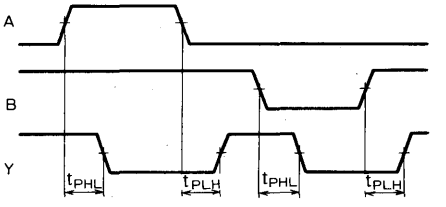
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time	C_L = 15pF, Other input low (Note 3)		8	23	ns
t_{PHL}				12	17	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time	C_L = 15pF, Other input high (Note 3)		8	30	ns
t_{PHL}				10	22	ns

Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = 3V_{P-P}, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS90P

DECADE COUNTER

DESCRIPTION

The M74LS90P is a semiconductor integrated circuit containing an asynchronous decade counter function with direct reset inputs and direct 9-set inputs.

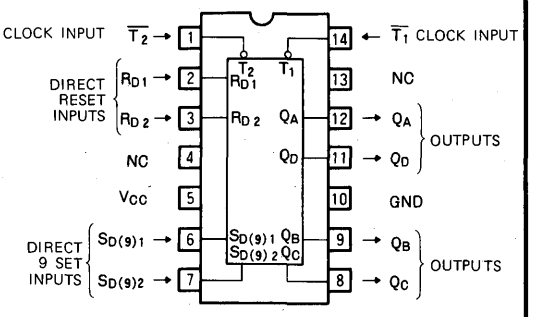
FEATURES

- Direct reset inputs provided
- Direct 9 set inputs provided
- Usable independently as binary and divide-by-five counter
- High-speed counting (f_{max}=75MHz typical)
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC : NO CONNECTION

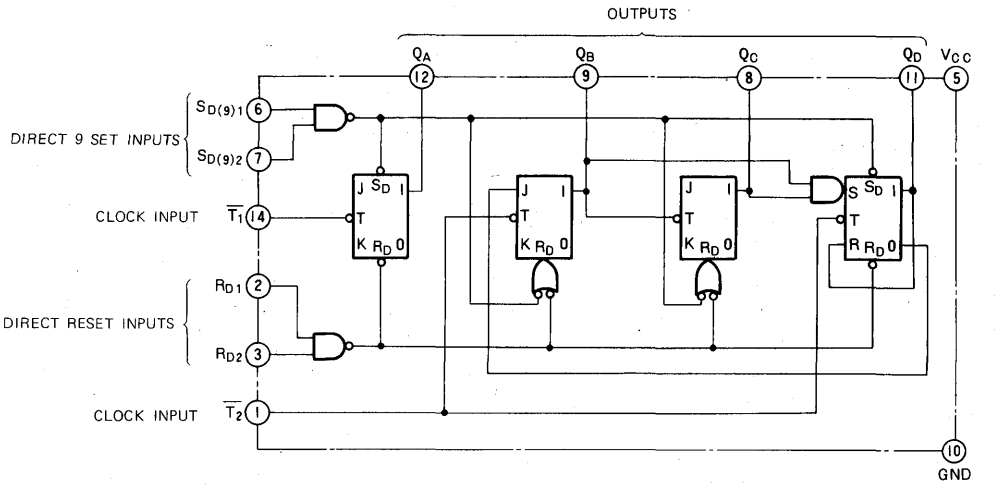
FUNCTIONAL DESCRIPTION

This device consists of independent binary and divide-by-five counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B, Q_C and Q_D are employed for use as a divide-by-five counter. When employed as a decade counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the BCD code output appears in outputs Q_A, Q_B, Q_C and Q_D. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The binary and divide-by-five counters can be reset or set to 9 simultaneously by setting direct reset inputs R_{D1} and R_{D2} high or direct 9 set inputs $S_{D(9)1}$ and $S_{D(9)2}$ high. For use as a counter, R_{D1} and/or R_{D2}, and $S_{D(9)1}$ and/or $S_{D(9)2}$, are set low.

Also provided is the M74LS290P with the same functions and electrical characteristics. Its GND positioning at pin 7 and V_{CC} at pin 14 makes for easy mounting.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

DECADE COUNTER

FUNCTION TABLE (Note 1)

$\overline{T}$	R_{D1}	R_{D2}	$S_{D(9)1}$	$S_{D(9)2}$	Q_A	Q_B	Q_C	Q_D
X	H	H	L	X	L	L	L	L
X	H	H	X	L	L	L	L	L
X	X	X	H	H	H	L	L	H
↓	L	X	L	X	Count			
↓	X	L	X	L	Count			
↓	L	X	X	L	Count			
↓	X	L	L	X	Count			

Note 1 ↓ : Transition from high to low
X : Irrelevant

Count	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

(1) Output Q_A is connected to input B for BCD count.

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	−0.5 ~ +5.5	V
		Inputs R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	−0.5 ~ +15	
V_O	Output voltage	High level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V	I_{OL} = 4mA (Note 2)		0.25	0.4	V
			V_I = 0.8V, V_I = 2V	I_{OL} = 8mA (Note 3)		0.35	0.5	V
I_{IH}	High-level input current	R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	V_{CC} = 5.25V V_I = 2.7V				20	μA
		$\overline{T_1}$					40	
		$\overline{T_2}$					80	
		$\overline{T_1}$	V_{CC} = 5.25V V_I = 5.5V				0.2	mA
		$\overline{T_2}$					0.4	
		R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	V_{CC} = 5.25V V_I = 0.4V				−0.4	mA
		$\overline{T_1}$					−2.4	
		$\overline{T_2}$					−3.2	
I_{OS}	Short-circuit output current (Note 3)		V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25V (Note 4)			9	15	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2: Testing of output QA should be conducted with input T_2 connected to output Q_A.

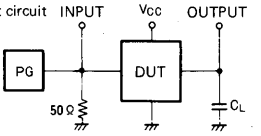
Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with R_{D1}, R_{D2} inputs grounded following momentary connection to 4.5V, and T_1, T_2, $S_{D(9)1}$ and $S_{D(9)2}$ inputs grounded

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A	C_L=15pF (Note 5)	32	75		MHz
fmax	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	30		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_A			7	16	ns
t_{PHL}				8	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_D			15	48	ns
t_{PHL}				16	50	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_B			7	16	ns
t_{PHL}				8	21	ns
t_{PLH}	Low-to-high-output, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_C			15	32	ns
t_{PHL}				15	35	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_D			7	32	ns
t_{PHL}				8	35	ns
t_{PHL}	High-to-low-level output propagation time, from inputs R_{D1}, R_{D2} to outputs Q_A, Q_B, Q_C, Q_D			17	40	ns
t_{PLH}	Low-to-high-level output propagation time, from inputs $S_{D(9)1}$, $S_{D(9)2}$ to outputs Q_A, Q_D			10	30	ns
t_{PHL}	High-to-low-level output propagation time, from inputs $S_{D(9)1}$, $S_{D(9)2}$ to outputs Q_B, Q_C			14	40	ns

Note 5: Measurement circuit

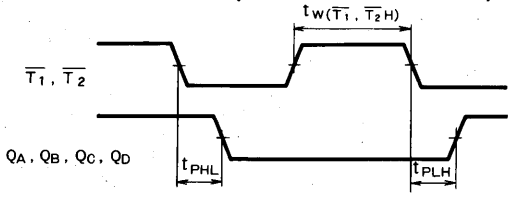


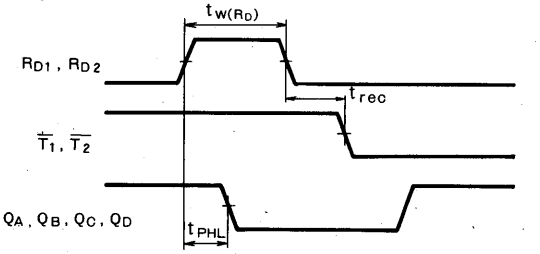
(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance

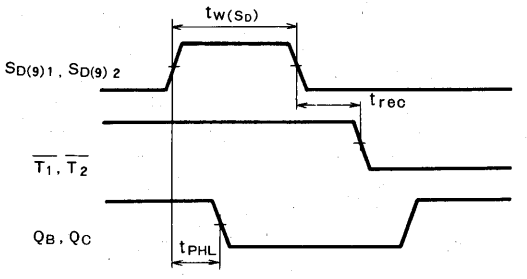
TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

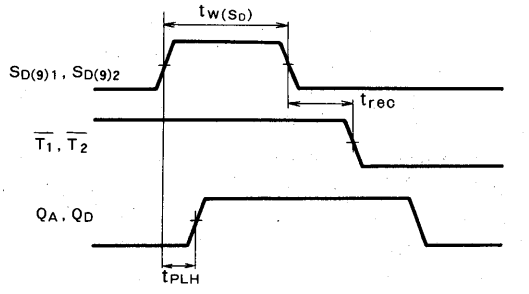
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T_1}H)}$	Clock input $\overline{T_1}$ high pulse width		15	6		ns
$t_{w(\overline{T_2}H)}$	Clock input $\overline{T_2}$ high pulse width		30	17		ns
$t_{w(R_D)}$	Direct reset R_{D1}, R_{D2} pulse width		15	6		ns
$t_{w(S_D)}$	Direct 9 set $S_{D(9)1}$, $S_{D(9)2}$ pulse width		15	8		ns
t_r	Clock pulse rise time			500	100	ns
t_f	Clock pulse fall time			200	100	ns
$t_{rec(R_D)}$	Recovery time R_{D1}, R_{D2} to $\overline{T_1}$, $\overline{T_2}$		25	8		ns
$t_{rec(S_D)}$	Recovery time $S_{D(9)1}$, $S_{D(9)2}$ to $\overline{T_1}$, $\overline{T_2}$		25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)









MITSUBISHI ELECTRIC

M74LS91P

8-BIT SHIFT REGISTER

DESCRIPTION

The M74LS91P is a semiconductor integrated circuit containing an 8-bit serial input-serial output shift register function.

FEATURES

- Synchronous serial input-serial ouptut
- Positive edge-triggering
- Q_7 and $\overline{Q_7}$ outputs provided
- Wide operating temperature range (T_a=−20~75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

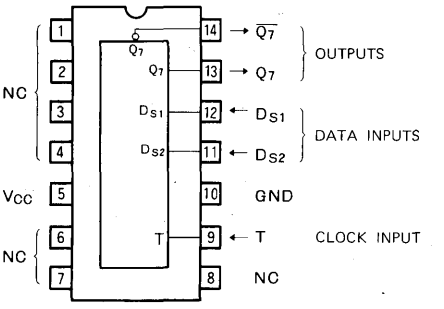
This device contains 8 edge-triggered R-S-T flip-flops and the serial data input D_{S1}, D_{S2} and $D_{S1} \cdot D_{S2}$ represents the first-stage flip-flop data input.

When D_{S1} and D_{S2} are both high and eight clock pulses are applied to clock input T, the high signal appears in Q_7 and the low signal in $\overline{Q_7}$. When one or more of the inputs is low and the eight clock pulses are applied to T, the low signal appears in $\overline{Q_7}$ and the high signal in $\overline{Q_7}$.

Data reading and shifting operations are performed when T changes from low to high.

Either D_{S1} and D_{S2} should be set low and eight or more clock pulses should be applied to T in order for all the 8 flip-flops to be set low.

PIN CONFIGURATION (TOP VIEW)



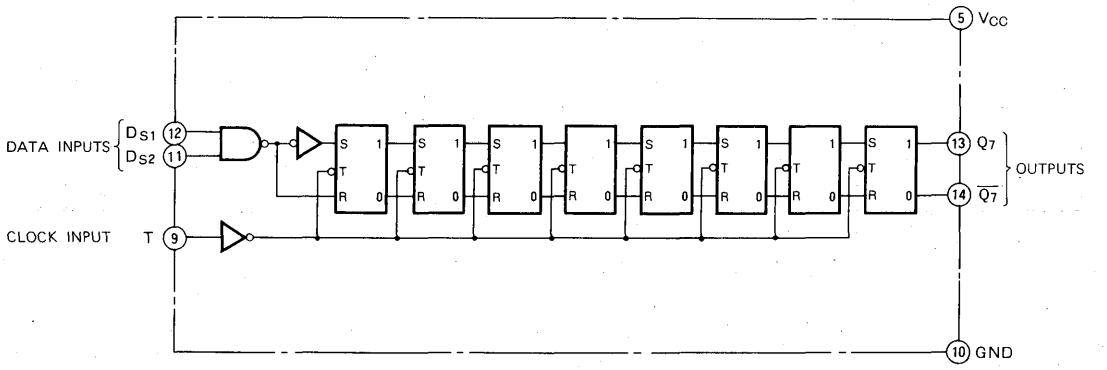
Outline 14P4 NC: NO CONNECTION

FUNCTION TABLE (Note 1)

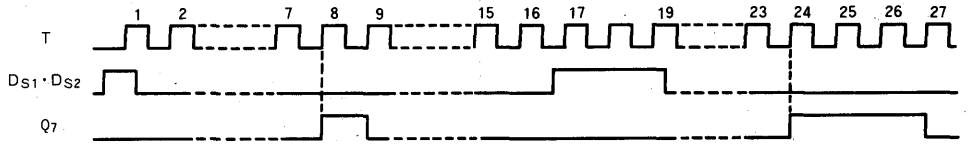
t_n		t_{n+8}	
D_{S1}	D_{S2}	Q_7	$\overline{Q_7}$
L	L	L	H
L	H	L	H
H	L	L	H
H	H	H	L

Note 1 t_n : Bit time before clock
t_{n+8} : Bit time after 8 clock pulses have been applied

BLOCK DIAGRAM



OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75V	I_{OL} = 4mA		0.25	0.4	V
		V_I = 0.8V, V_I = 2V	I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current	V_{CC} = 5.25V, V_O = 0V (Note 2)		−20		−100	mA
I_{CC}	Supply current	V_{CC} = 5.25V (Note 3)			12	20	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C

Note 2: All measurements should be done quickly.

Note 3: I_{CC} is measured with D_{S1} and D_{S2} at 0V after 8 clock pulses have been applied to T

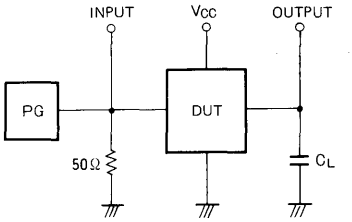
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L = 15pF (Note 4)	10	60		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_7, $\overline{Q_7}$			12	40	ns
t_{PHL}				15	40	ns

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

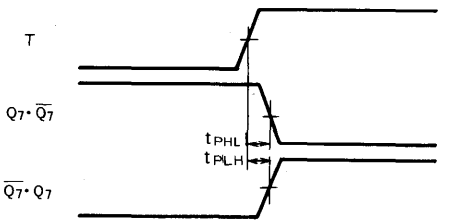
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(T)}$	Clock input pulse width		25	6		ns
$t_{su(Ds)}$	Setup time D_{S1}, D_{S2} to T		25	7		ns
$t_{h(Ds)}$	Hold time D_{S1}, D_{S2} to T		6	0		ns

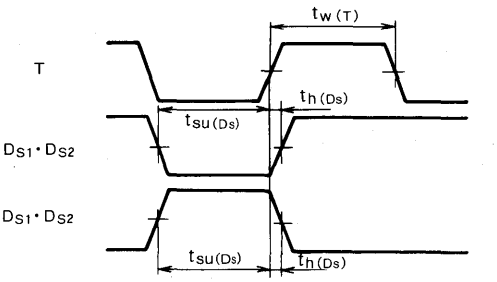
Note 4: *Measurement circuit*



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r= 6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Z_O=50Ω.
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)





M74LS92P

DIVIDE-BY-TWELVE COUNTER

DESCRIPTION

The M74LS92P is a semiconductor integrated circuit containing an asynchronous divide-by-twelve counter function with direct reset inputs.

FEATURES

- Direct reset input provided
- Usable independently as binary and divide-by-six counter
- High-speed counting (f_{max} = 80MHz typical)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

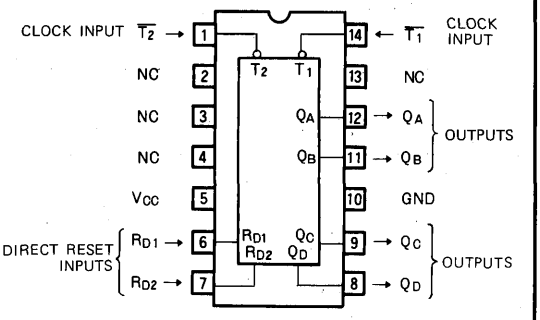
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-6 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B, Q_C and Q_D are employed for use as a divide-by-6 counter. When employed as a divide-by-12 counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the output appears in outputs Q_A, Q_B, Q_C and Q_D in accordance with the function table. The code appearing in the output is not pure binary code. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

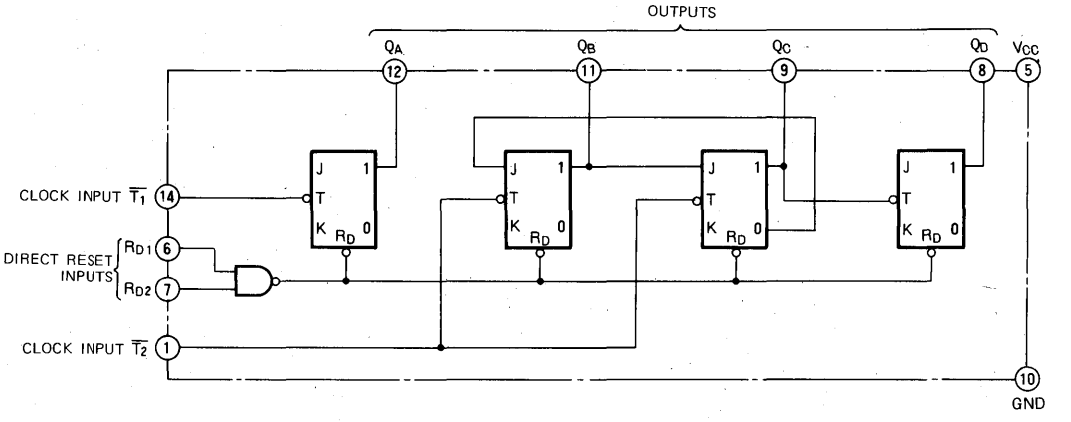
The binary and divide-by-6 counters can be reset simultaneously by setting direct reset inputs R_{D1} and R_{D2} high. For use as a counter, either R_{D1} or R_{D2} or both set low.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC : NO CONNECTION

BLOCK DIAGRAM



DIVIDE-BY-TWELVE COUNTER

FUNCTION TABLE (Note 1)

$\overline{T}$	R_{D1}	R_{D2}	Q_A	Q_B	Q_C	Q_D
X	H	H	L	L	L	L
↓	L	H	Count			
↓	H	L	Count			
↓	L	L	Count			

Note 1 ↓ : Transition from high to low
X : Irrelevant

Count number	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

(1) Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS
($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	$-0.5 \sim +5.5$	V
		Inputs R_{D1}, R_{D2}	$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	°C
T_{stg}	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDTIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				-1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=4mA$ (Note 2)		0.25	0.4	V
			$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$ (Note 2)		0.35	0.5	V
I_{IH}	High-level input current	R_{D1}, R_{D2}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{T_1}$					40	
		$\overline{T_2}$					80	
		$\overline{T_1}$	$V_{CC}=5.25V$, $V_I=5.5V$				0.2	mA
		$\overline{T_2}$					0.4	
		R_{D1}, R_{D2}	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	R_{D1}, R_{D2}	$V_{CC}=5.25V$, $V_I=0.4V$				-0.4	mA
		$\overline{T_1}$					-2.4	
		$\overline{T_2}$					-3.2	
I_{OS}	Short-circuit output current (Note 3)		$V_{CC}=5.25V$, $V_O=0V$		-20		-100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 4)			9	15	mA

* : All typical values are at $V_{CC}=5V$; $Ta=25°C$.

Note 2: Testing of output Q_A should be conducted with input $\overline{T_2}$ connected to output Q_A.

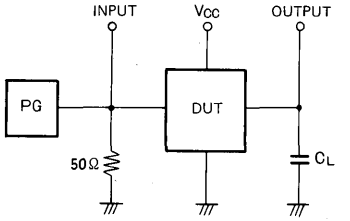
Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with $\overline{T_1}$ and $\overline{T_2}$ at 0V after R_{D1} and R_{D2} have been set to 0V from 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A	C_L=15pF (Note 4)	32	80		MHz
f_{max}	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	30		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation fime, from input $\overline{T_1}$ to output Q_A			7	16	ns
t_{PHL}				8	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_D			25	48	ns
t_{PHL}				25	50	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_B			7	16	ns
t_{PHL}				8	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation fime, from input $\overline{T_2}$ to output Q_C			8	16	ns
t_{PHL}				10	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_D			15	32	ns
t_{PHL}				15	35	ns
t_{PHL}	High-to-low-level output propagation time, from inputs R_{D1}, R_{D2} to outputs Q_A, Q_B, Q_C, Q_D			17	40	ns

Note 4: Measurement circuit



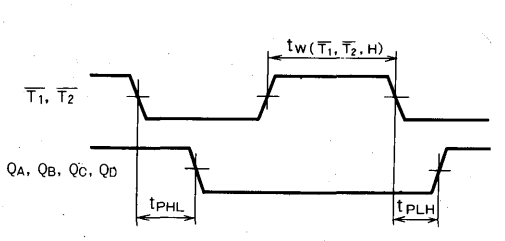
(1) The pulse generator (PG) has the following characteristics: PRR = 1MNz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω.

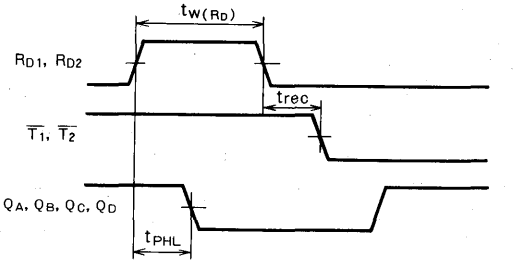
(2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{T_1}H)}$	Clock input $\overline{T_1}$ high pulse width		15	6		ns
$t_{W(\overline{T_2}H)}$	Clock input $\overline{T_2}$ high pulse width		30	17		ns
$t_{W(R_D)}$	Direct reset R_{D1}, R_{D2} pulse width		15	5		ns
t_r	Clock pulse rise time			500	100	ns
t_f	Clock pulse fall time			200	100	ns
$t_{rec(R_D)}$	Recovery time R_{D1}, R_{D2} to $\overline{T_1}$, $\overline{T_2}$		25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)





MITSUBISHI ELECTRIC

M74LS93P

4-BIT BINARY COUNTER

DESCRIPTION

The M74LS93P is a semiconductor integrated circuit containing an asynchronous 4-bit binary (hexadecimal) counter function with direct reset inputs.

FEATURES

- Direct reset inputs provided
- Usable independently as binary and octal counter
- High-speed counting (f_{max} = 60MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

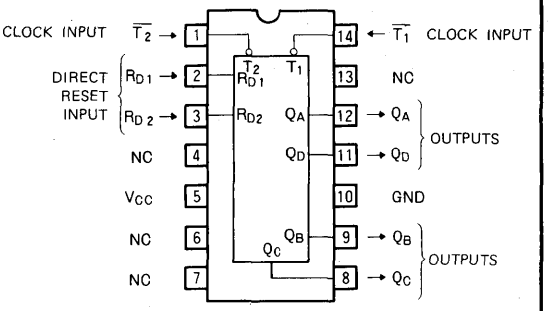
FUNCTIONAL DESCRIPTION

This device is composed of independent binary and octal counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B, Q_C and Q_D are employed for use as an octal counter. When employed as a hexadecimal counter, the pure binary code output appears in the Q_A, Q_B, Q_C and Q_D outputs by connecting Q_A and $\overline{T_2}$ and making $\overline{T_1}$ the input. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ change from high to low.

The binary and octal counters can be reset simultaneously by setting direct reset inputs R_{D1} or R_{D2}, high. For use as a counter, either R_{D1} or R_{D2}, or both, is set low.

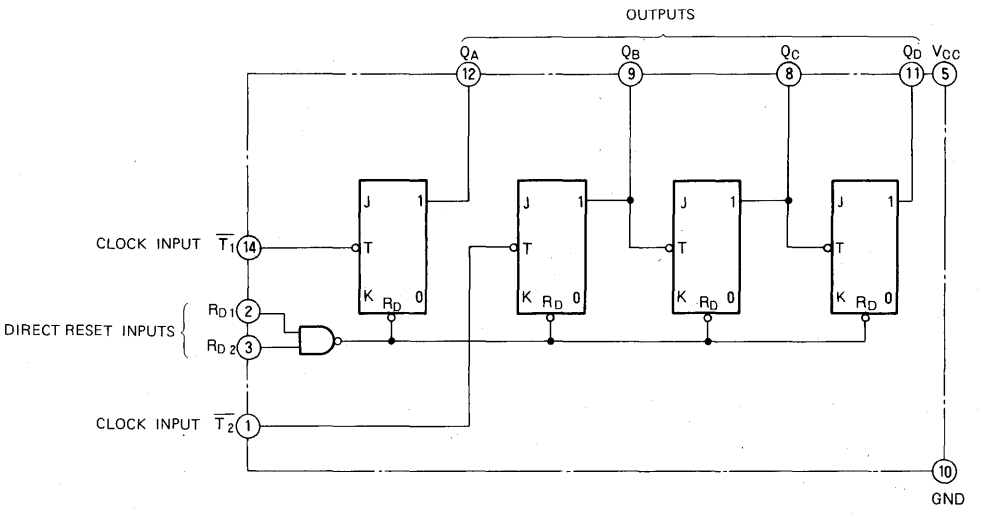
Also provided is the M74LS293P with the same functions and electrical characteristics. Its GND positioning at pin 7 enables easy mounting.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC : NO CONNECTION

BLOCK DIAGRAM



FUNCTION TABLE (Note 1)

$\overline{T}$	R_{D1}	R_{D2}	Q_A	Q_B	Q_C	Q_D
X	H	H	L	L	L	L
↓	L	H	Count			
↓	H	L	Count			
↓	L	L	Count			

Note 1 ↓ : Transition from high to low
X : Irrelevant

Count number	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	−0.5 ~ +5.5	V
		Inputs R_{D1}, R_{D2}	−0.5 ~ +15	
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

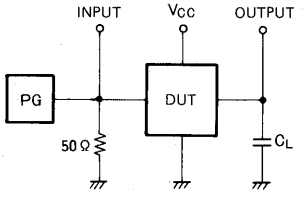
Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V	I_{OL}=4mA (Note 2)		0.25	0.4	V
				I_{OL}=8mA (Note 2)		0.35	0.5	V
I_{IH}	High-level input current	R_{D1}, R_{D2}	V_{CC}=5.25V, V_I=2.7V				20	μA
		$\overline{T_1}$, $\overline{T_2}$					40	
		$\overline{T_1}$, $\overline{T_2}$	V_{CC}=5.25V, V_I=5.5V				0.2	mA
		R_{D1}, R_{D2}	V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	R_{D1}, R_{D2}	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
		$\overline{T_1}$					−2.4	
		$\overline{T_2}$					−1.6	
I_{OS}	Short-circuit output current (Note 3)		V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 4)			9	15	mA

* : All typical values are at V_{CC} = 5V, Ta=25°C.
Note 2: Testing of output Q_A should be conducted with input T_2 connected to output Q_A
Note 3: All measurements should be done quickly and not more than one output shoudl be shorted at a time.
Note 4: I_{CC} is measured with $\overline{T_1}$ and $\overline{T_2}$ at 0V after R_{D1} and R_{D2} have been set to 0V from 4.5 V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits typ	Limits Max	Unit
f_{max}	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A	C_L=15pF (Note 5)	32	60		MHz
f_{max}	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	35		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_A			7	16	ns
t_{PHL}				8	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_B			28	70	ns
t_{PHL}				28	70	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_C			7	16	ns
t_{PHL}				8	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_D			15	32	ns
t_{PHL}				15	35	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_D			22	51	ns
t_{PHL}				22	51	ns
t_{PHL}	High-to-low-level output propagation time, from inputs R_{D1}, R_{D2} to outputs Q_A, Q_B, Q_C, Q_D			17	40	ns

Note 5: Measurement circuit

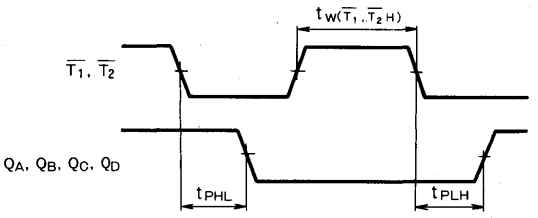


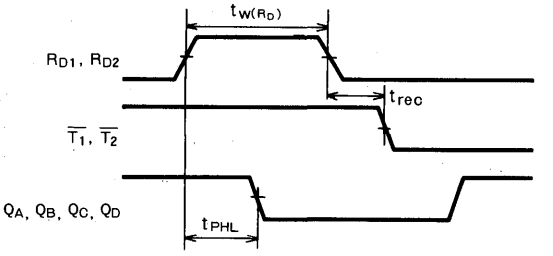
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MNz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Zo = 50Ω.
(2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T_1}H)}$	Clock input $\overline{T_1}$ high pulse width		15	6		ns
$t_{w(\overline{T_2}H)}$	Clock input $\overline{T_2}$ high pulse width		30	15		ns
$t_{w(R_D)}$	Direct reset R_{D1}, R_{D2} Pulse width		15	5		ns
t_r	Clock pulse rise time			500	100	ns
t_f	Clock pulse fall time			200	100	ns
$t_{rec(R_D)}$	Recovery time R_{D1}, R_{D2} to $\overline{T_1}$, $\overline{T_2}$		25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)





M74LS95BP

4-BIT PARALLEL-ACCESS SHIFT REGISTER

DESCRIPTION

The M74LS95BP is a semiconductor integrated circuit containing a 4-bit serial/parallel input-serial/parallel output shift register function.

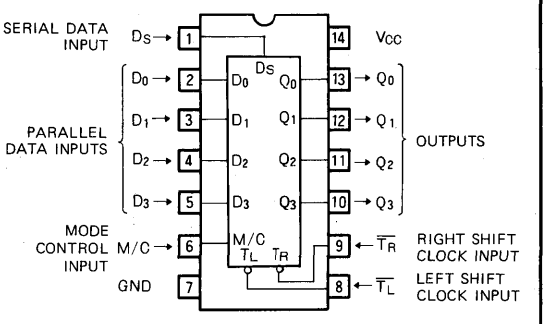
FEATURES

- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection
- Mode control input provided
- Special right and left shift inputs provided
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)

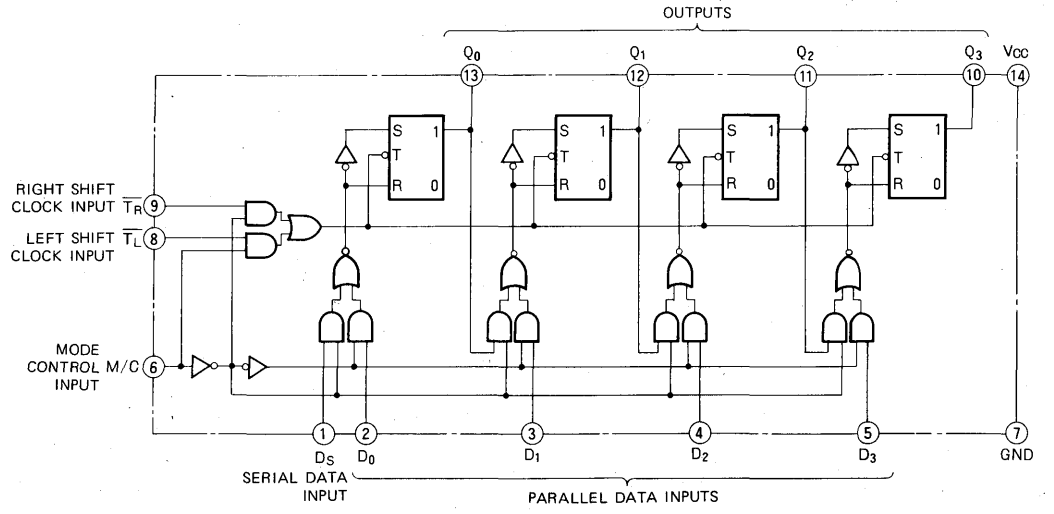


Outline 14P4

FUNCTIONAL DESCRIPTION

This device is usable as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept at low, the serial data are applied to serial data input D_S and the clock pulse is applied to right shift clock input $\overline{T_R}$, the serial data are shifted sequentially into outputs Q_0~Q_3 in synchronization with the clock pulse. When M/C is kept at high, the parallel data are applied to parallel data inputs D_0~D_3 and the 1-bit clock pulse is applied to left shift clock input $\overline{T_L}$, the signals D_0~D_3 appear in outputs Q_0~Q_3 respectively. When $\overline{T_R}$ and $\overline{T_L}$ change from high to low, the right shift or parallel data reading operation is performed. When M/C is kept in high, Q_3 is connected to D_2, Q_2 to D_1 and Q_1 and D_0, the serial data are applied to D_3 and the clock pulse is applied to $\overline{T_L}$, the device functions as a left shift register. Care should be taken when switching the M/C signal since the output changes in accordance with the status of $\overline{T_R}$ and $\overline{T_L}$. Refer to the function table.

BLOCK DIAGRAM



4-BIT PARALLEL-ACCESS SHIFT REGISTER

FUNCTION TABLE (Note 1)

Operational mode	M/C	$\overline{T_R}$	$\overline{T_L}$	D_S	$D_0 \sim D_3$	Q_0	Q_1	Q_2	Q_3
Right shift	L	↓	X	L	X	L	Q_0^0	Q_1^0	Q_2^0
	L	↓	X	H	X	H	Q_0^0	Q_1^0	Q_2^0
Parallel reading	H	X	↓	X	$D_0 \sim D_3$	D_0	D_1	D_2	D_3
M/C switching	↓	L	L	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0
	↑	L	L	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0
	↓	H	L	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0
	↑	H	L	X	X	*	*	*	*
	↓	L	H	X	X	*	*	*	*
	↑	L	H	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0
	↓	H	H	X	X	*	*	*	*
	↑	H	H	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0

Note 1. ↓ : Transition from high to low (negative edge trigger)
↑ : Transition from low to high (positive edge trigger)
Q^0 : Level of Q before the indicated steady-state input conditions were established
* : Cannot be predicted
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20 \sim +75$	°C
Tstg	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

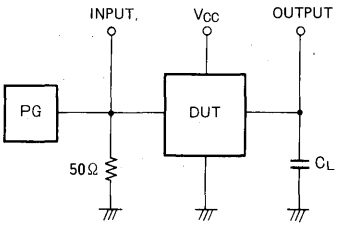
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC} = 4.75V$, $I_{IC} = -18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC} = 4.75V$, $V_I = 0.8V$, $V_I = 2V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = 4.75V$, $V_I = 0.8V$, $V_I = 2V$	$I_{OL} = 4mA$		0.25	0.4	V
				$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	M/C	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		M/C					40	
		M/C	$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
		M/C					0.2	
I_{IL}	Low-level input current	M/C	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.4	mA
		M/C					−0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC} = 5.25V$, $V_O = 0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC} = 5.25V$ (Note 3)			13	21	mA

* : All typical values are at V_{CC}=5V, Ta=25°C.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with $D_0 \sim D_3$ at 0V, D_S open and M/C at 4.5V after $\overline{T_R}$ and $\overline{T_L}$ have been set from 3V to 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
f_{max}	Maximum clock frequency	C_L=15pF (Note 4)	25	50		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $\overline{T}_R$, $\overline{T}_L$ to outputs $Q_0 \sim Q_3$			14	27	ns
t_{PHL}				14	32	ns

Note 4: Measurement circuit

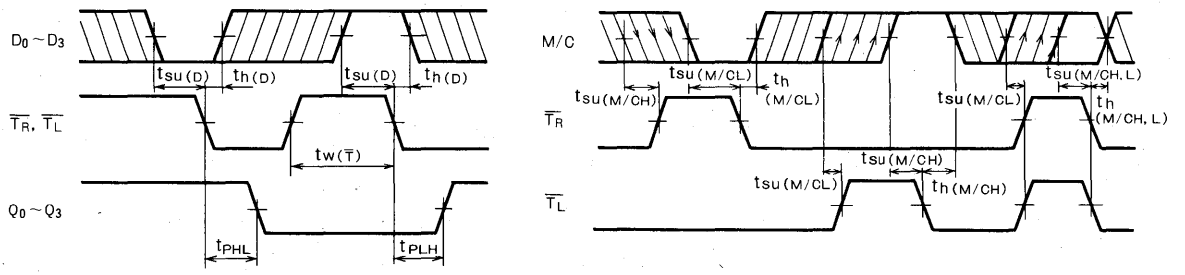


(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{T})}$	Clock input $\overline{T}$ high pulse width		25	8		ns
t_f	Clock input $\overline{T}$ falltime			350	100	ns
$t_{SU(D)}$	Setup time D to $\overline{T}$		20	0		ns
$t_{SU(M/CL)}$	Setup time M/C low to $\overline{T}$		20	14		ns
$t_{SU(M/CH)}$	Setup time M/C high to $\overline{T}$		20	0		ns
$t_{h(D)}$	D hold time to $\overline{T}$		10	2		ns
$t_{h(M/CL)}$	Hold time M/C low to $\overline{T}$		10	2		ns
$t_{h(M/CH)}$	Hold time M/C high to $\overline{T}$		10	−13		ns

TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.
The arrows on the shaded areas indicate the direction for when the input is permitted to change.

M74LS96P

5-BIT SHIFT REGISTER

DESCRIPTION

The M74LS96P is a semiconductor integrated circuit containing a 5-bit serial/parallel input-serial/parallel output shift register function.

FEATURES

- Positive edge-triggering
- Right shift function
- Asynchronous parallel input provided
- Direct reset input provided
- Wide operating temperature range (T_a= –20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

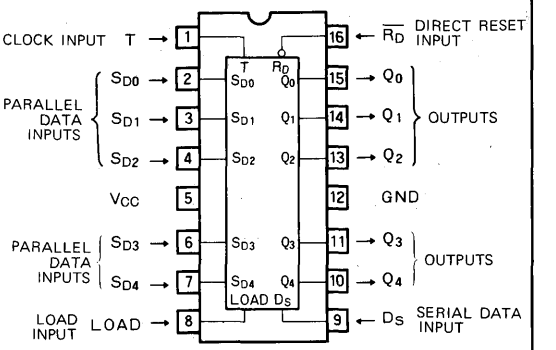
This 5-bit shift register is composed with 4 R-S-T flip-flops and it functions as a serial/parallel inpput-serial/parallel output shift register.

For use as a serial input-serial/parallel output shift register, the load input LOAD or parallel data inputs S_{D0}~S_{D4} are kept in high and the data are applied to the serial data input D_S. When a clock pulse is applied to clock input T with D_S in high, the high signal is shifted sequentially to Q_0, Q_1 ... Q_4. Shifting is performed when T changes from low to high. When the serial data are applied to D_{S0}~S_{D4} and LOAD is set high, the S_{D0}~S_{D4} signals appear in Q_0~Q_4 respectively irrespective of T.

When direct reset input $\overline{R_D}$ is set low, Q_0~Q_4 are set low if LOAD is low irrespective of the other input signals.

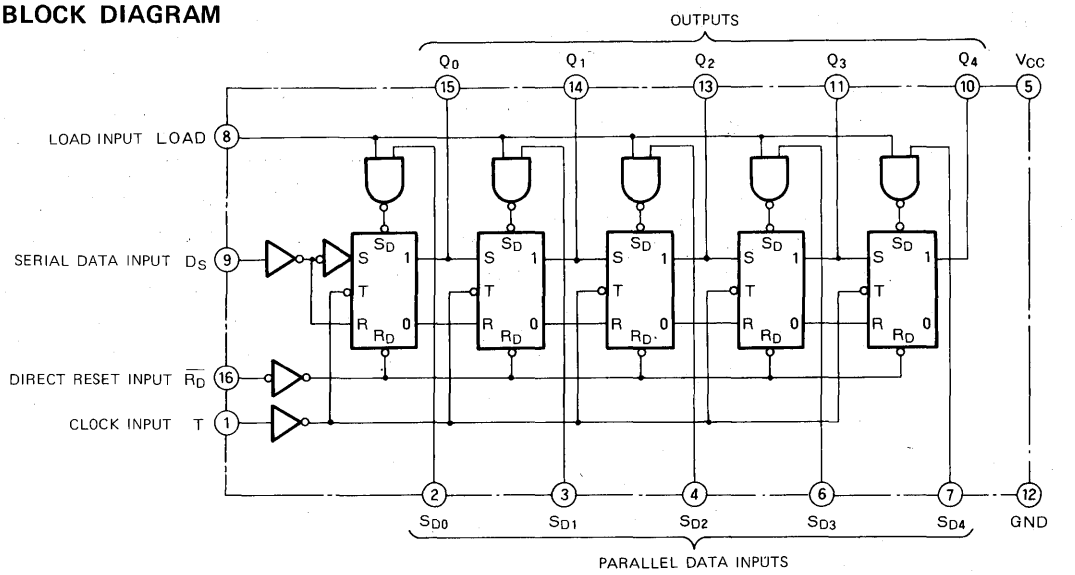
When LOAD is high, parallel reading takes precedence, and the S_{D0}~S_{D4} signals appear in Q_0~Q_4.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



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FUNCTION TABLE (Note 1)

SERIAL INPUT-PARALLEL OUTPUT

	t_n	t_{n+1}	t_{n+2}	t_{n+3}	t_{n+4}	t_{n+5}	t_{n+6}
D_S	L	H	L	H	L	H	L
Q_0	*	L	H	L	H	L	H
Q_1	*	*	L	H	L	H	L
Q_2	*	*	*	L	H	L	H
Q_3	*	*	*	*	L	H	L
Q_4	*	*	*	*	*	L	H

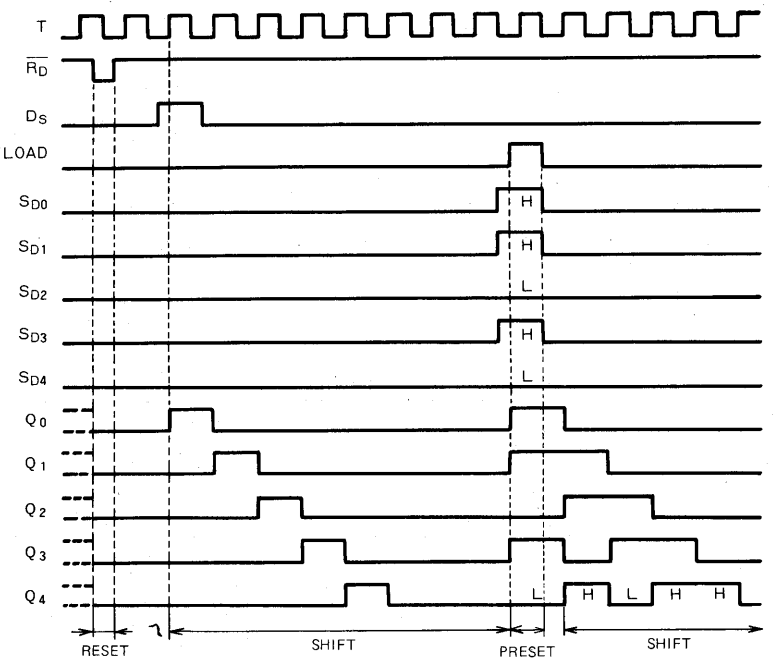
Note 1: For use as a serial input-parallel output, LOAD, S_{D0}, S_{D1}, S_{D2}, S_{D3} and S_{D4} are all kept at low and $\overline{RD}$ is kept at high.
tn: Bit time prior to clock
tn+1: Bit time after application of 1 clock pulse
tn+6: Bit time after application of 6 clock pulses
* : Cannot be predicted

PARALLEL INPUT-PARALLEL OUTPUT

LOAD	$S_{D(N)}$	$\overline{R_D}$	$Q_{(N)}$
L	L	L	L
L	L	H	Q^0
L	H	L	L
L	H	H	Q^0
H	L	L	L
H	L	H	Q^0
H	H	L	H
H	H	H	H

Note 2: For use as a parallel input-parallel output, $\overline{R_D}$ is first set low and kept at high.
The parallel input data are input into S_{D0}~S_{D4}.
The data are read when LOAD is high and they simultaneously appear in the outputs. $\overline{R_D}$ is usually kept at high and LOAD at low.
The "N" in $S_{D(N)}$ refers to 0, 1, 2, 3, 4.
Q^0 is the level of Q before the indicated steady-state input conditions were established.

OPERATION TIMING DIAGRAM



5-BIT SHIFT REGISTER

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level output	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

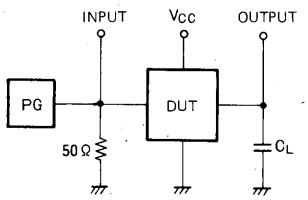
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
			V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	LOAD	V_{CC}=5.25V				100	μA
		Other inputs	V_I=2.7V				20	
		LOAD	V_{CC}=5.25V				0.5	mA
		Other inputs	V_I=10V				0.1	
I_{IL}	Low-level input current	LOAD	V_{CC}=5.25V				−2.0	mA
		Other inputs	V_I=0.4V				−0.4	
I_{OS}	Short-circuit output current (Note 3)		V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 4)			12	20	mA

* : All typical values are at V_{CC}=5V, Ta=25°C.
Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 4: I_{CC} is measured with $\overline{R_D}$ at 0V and all the other inputs at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L=15pF (Note 5)	25	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs $Q_0 \sim Q_4$			12	40	ns
t_{PHL}				12	40	ns
t_{PLH}	Low-to-high-level output propagation time, from input S_D, LOAD to outputs $Q_0 \sim Q_4$			11	35	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to outputs $Q_0 \sim Q_4$			11	35	ns

Note 5: Measurement circuit

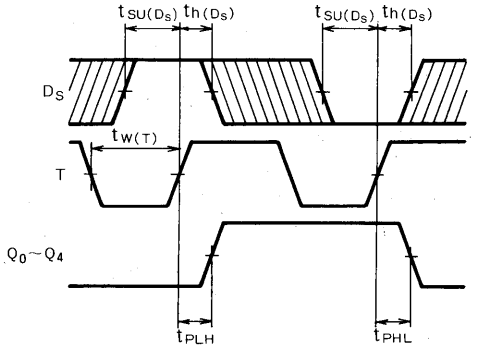


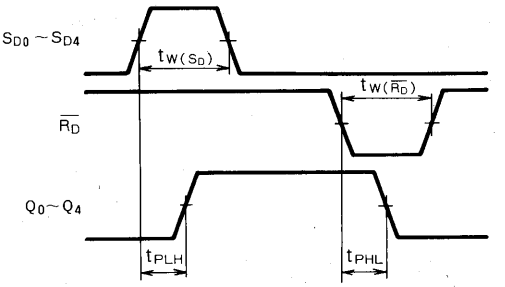
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(T)}$	Clock input T pulse width		20	5		ns
$t_{w(S_D)}$	Parallel data input pulse width		30	5		ns
$t_{w(\overline{R_D})}$	Direct reset pulse width		30	5		ns
$t_{su(D_S)}$	Setup time D_S to T		30	3		ns
$t_{h(D_S)}$	Hold time D_S to T		5	−1		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS107AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH RESET

DESCRIPTION

The M74LS107AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input $\overline{T}$, J and K inputs and direct reset input R_D.

FEATURES

- Negative edge-triggering
- Independent input/output terminals for each flip-flop.
- Direct reset input
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = -20 ~ +75°C)

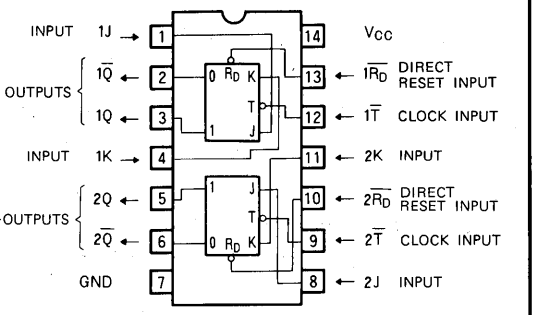
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

J and K signals are read when $\overline{T}$ is "H". When $\overline{T}$ changes from "H" to "L", Q and $\overline{Q}$ transit with the J and K signals to the states described in the function table. By setting $\overline{R_D}$ in "L" state, Q and $\overline{Q}$ become "L" and "H", respectively, irrespective of the states of the other input signals. For use as a J-K flio-flop, keep $\overline{R_D}$ in the "H" state. M74LS107AP is the same as M74LS73AP except for pin configuration.

PIN CONFIGURATION (TOP VIEW)



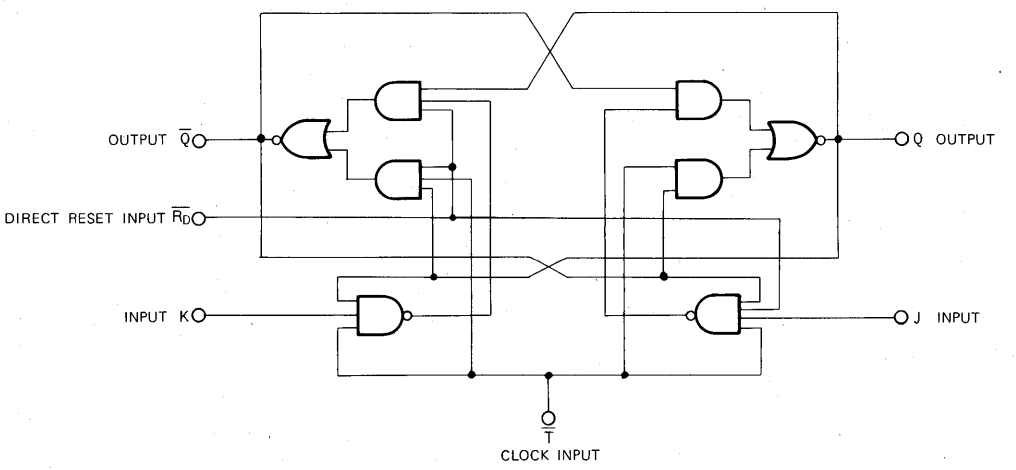
Outline 14P4

FUNCTION TABLE (Note 1)

$\overline{T}$	$\overline{R_D}$	J	K	Q	$\overline{Q}$
X	L	X	X	L	H
↓	H	H	H	Toggle	
↓	H	L	H	L	H
↓	H	H	L	H	L
↓	H	L	L	Q^0	$\overline{Q^0}$
H	H	X	X	Q^0	$\overline{Q^0}$

Note 1: ↓ : transition from high to low-level
X : irrelevant
Q^0 : level of Q before the indicated steady-state input conditions were established.
$\overline{Q^0}$: level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Toggle : complement of previous state with ↓ transition of outputs

BLOCK DIAGRAM (EACH FLIP-FLOP)



MITSUBISHI ELECTRIC

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH RESET

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400 μA		2.7	3.4		V
V_{OL}	Low-level output current		V_{CC} = 4.75V	I_{OL} = 4mA		0.25	0.4	V
			V_I = 0.8V, V_I = 2V	I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	J, K	V_{CC} = 5.25V V_I = 2.7V				20	μA
		$\overline{R_D}$					60	
		$\overline{T}$					80	
		J, K	V_{CC} = 5.25V V_I = 10V				0.1	mA
		$\overline{R_D}$					0.3	
		$\overline{T}$					0.4	
I_{IL}	Low-level input current	J, K	V_{CC} = 5.25V V_I = 0.4V				−0.4	mA
		$\overline{R_D}$ $\overline{T}$					−0.8	
I_{OS}	Short-circuit output current (Note 2)		V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25V (Note 3)			4	6	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

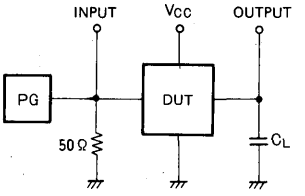
Note 2: I_{CC} is measured with Q and $\overline{Q}$ outputs high in turn. At the time of measurement, $\overline{T}$ input is grounded.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L = 15pF (Note 4)	30	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T}$ to output Q, $\overline{Q}$			8	20	ns
t_{PHL}				6	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{R_D}$ to output Q, $\overline{Q}$			10	20	ns
t_{PHL}				7	20	ns

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH RESET

Note 4: Measurement circuit

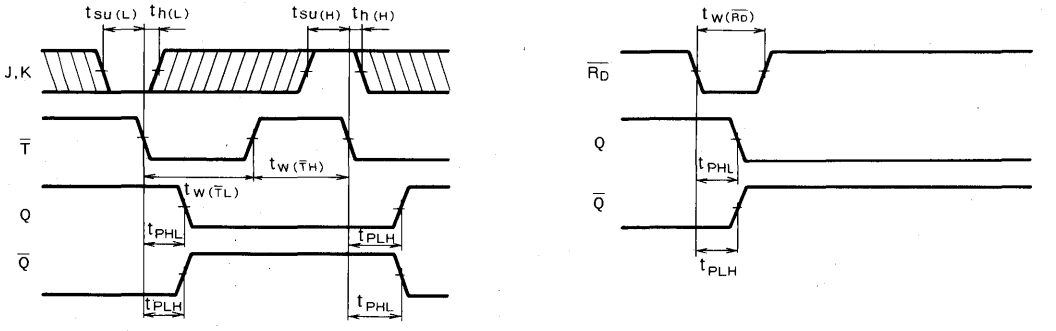


(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5 V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{T}H)}$	Clock input $\overline{T}$ high pulse width		20	12		ns
$t_{W(\overline{RD})}$	Direct reset input $\overline{R_D}$ pulse width		25	4		ns
tr	Clock rise time			650	100	ns
tf	Clock pulse fall time			900	100	ns
$t_{SU(H)}$	Setup time high J, K to $\overline{T}$		20	9		ns
$t_{SU(L)}$	Setup time low J, K to T		20	10		ns
$t_{h(H)}$	Hold time high J, K to T		0	− 8		ns
$t_{h(L)}$	Hold time low J, K to $\overline{T}$		0	− 5		ns

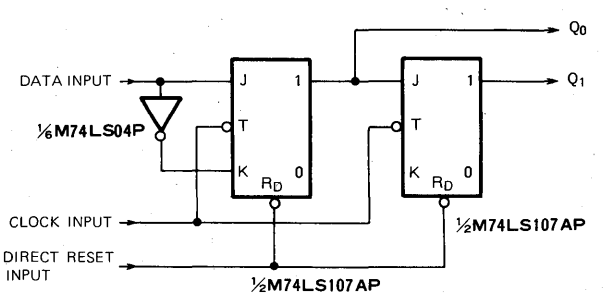
TIMING DIAGRAM (Reference level = 1.3V)

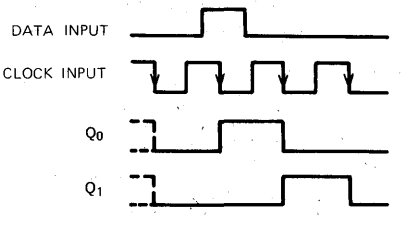


Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

2bit shift register





Note 6: Output switching characteristics may not satisfy the ratings if the clock signal is applied without observing the set-up time.

M74LS109AP

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

DESCRIPTION

The M74LS109AP is a semiconductor integrated circuit containing 2 J-$\overline{K}$ positive edge-triggered flip-flop circuits with discrete terminals for clock input T, inputs J and $\overline{K}$, and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Positive edge-triggering
- Each flip-flop can be used independently
- Direct set and reset inputs
- J and $\overline{K}$ inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20~+75°C)

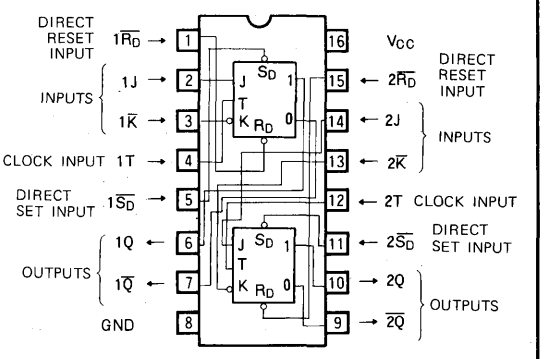
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

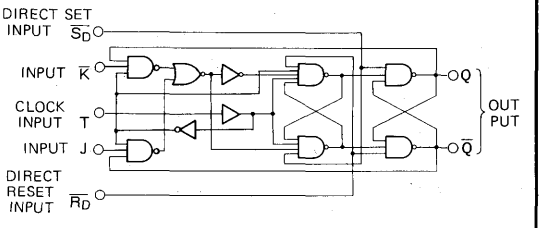
When T changes from low to high, the J and $\overline{K}$ signals immediately before the change emerge in outputs Q and $\overline{Q}$ in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$, this IC can be made into a direct R-S flip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, Q = $\overline{Q}$ = high. However, when both of them change to high at the same time, the status of Q and $\overline{Q}$ cannot be anticipated. For use as a J-K flip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high. By connecting J and $\overline{K}$, this IC can be used as a D-type flip-flop.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

LOGIC DIAGRAM (EACH FLIP-FLOP)



FUNCTION TABLE (Note 1)

$\overline{S_D}$	$\overline{R_D}$	T	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	L	X	X	Q^0	$\overline{Q^0}$
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q^0	$\overline{Q^0}$
H	H	↑	H	H	H	L

Note 1 ↑ : Transition from low to high-level (positive edge trigger)

Q^0 : Level of Q before the indicated steady-state input conditions were established.

$\overline{Q^0}$: Level of $\overline{Q}$ before the indicated steady-state input conditions were established.

Toggle : complement of previous state with ↑ transition of output

X : Irrelevant

* : Q = $\overline{Q}$ = high when $\overline{S_D}$ = $\overline{R_D}$ = low and so when both $\overline{S_D}$ and $\overline{R_D}$ are set high, the status of Q and $\overline{Q}$ cannot be anticipated.

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +5.5	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75℃$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75℃$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
			$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	J, $\overline{K}$, T	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{S_D}$, $\overline{R_D}$					40	
		J, $\overline{K}$, T	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{S_D}$, $\overline{R_D}$					0.2	
I_{IL}	Low-level input current	J, $\overline{K}$, T	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$\overline{S_D}$, $\overline{R_D}$					−0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$, (Note 3)			4	8	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25℃$

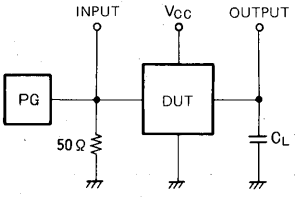
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: The supply current should be measured with Q and $\overline{Q}$ alternately set high and with T set low during actual measurement.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25℃$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	$C_L=15pF$ (Note 4)	25	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from T to Q, $\overline{Q}$			10	25	ns
t_{PHL}				12	40	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{S_D}$, $\overline{R_D}$ to Q, $\overline{Q}$			11	25	ns
t_{PHL}				10	40	ns

Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.

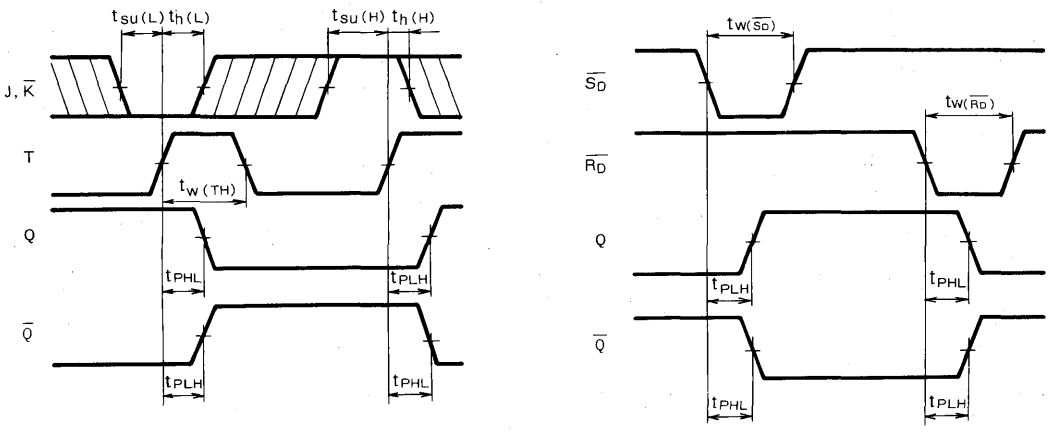
(2) C_L includes probe and jig capacitance.

DUAL J-K POSITIVE EDGE-TRIGGERED FLIP FLOP WITH SET AND RESET

TIMING REQUIREMENTS (V_{CC}= 5 V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(TH)}$	Clock input T high pulse width		25	11		ns
$t_{w(\overline{SD},\overline{RD})}$	Direct set, reset pulse width		25	4		ns
$t_{su(H)}$	Setup time high to T		20	19		ns
$t_{su(L)}$	Setup time low to T		20	7		ns
$t_{h(H)}$	Hold time high to T		5	−2		ns
$t_{h(L)}$	Hold time low to T		5	−16		ns

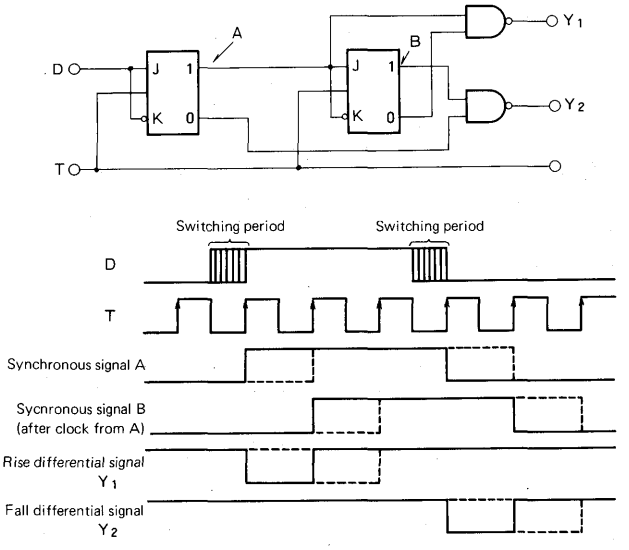
TIMING DIAGRAM (Reference level = 1.3V)



Note 4: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Typical circuit for converting asynchronous signal into synchronous signal and rise/fall differential circuit



Note 5: The waveforms indicated by the dotted lines apply when reading with the next clock without observing the set-up time to T.

M74LS112AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

DESCRIPTION

The M74LS112AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input $\overline{T}$, J and K inputs and direct set and reset inputs $\overline{S_D}$ and $\overline{R_D}$.

FEATURES

- Negative edge-triggering
- Independent input/output terminals for each flip-flop.
- Direct set and reset inputs
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = -20 ~ +75°C)

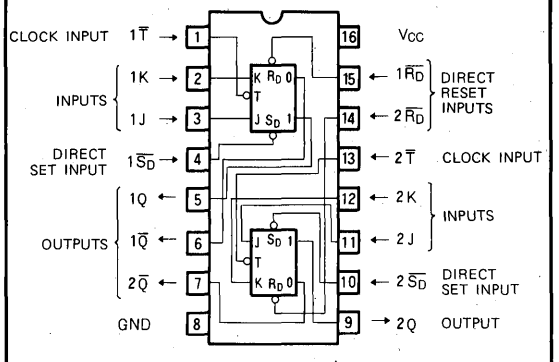
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

J and K signals of are read, while $\overline{T}$ is high. When $\overline{T}$ changes from high to low, the signals of J and K immediately before the change appear in outputs Q and $\overline{Q}$ in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$, this IC can be made into an direct R-S flip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, Q = $\overline{Q}$ = high. However, when both of them changed to high at the same time, the status of Q and $\overline{Q}$ cannot be anticipated. For use as a J-K flip-flop, keep $\overline{S_D}$ and $\overline{R_D}$ high. M74LS112AP is the same as M74LS76AP except for pin configuration.

PIN CONFIGURATION (TOP VIEW)



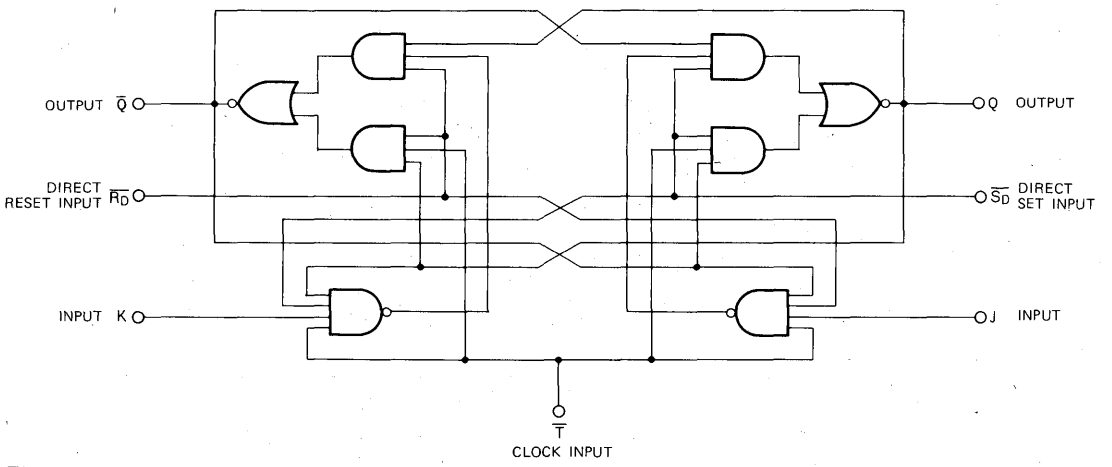
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{T}$	$\overline{S_D}$	$\overline{R_D}$	J	K	Q	$\overline{Q}$
X	L	H	X	X	H	L
X	H	L	X	X	L	H
X	L	L	X	X	H*	H*
↓	H	H	H	H	Toggle	
↓	H	H	L	H	L	H
↓	H	H	H	L	H	L
↓	H	H	L	L	Q^0	$\overline{Q^0}$
H	H	H	X	X	Q^0	$\overline{Q^0}$

Note 1: ↓ : transition from high to low-level
X : irrelevant
* : Q = $\overline{Q}$ = high when $\overline{S_D}$ = $\overline{R_D}$ = low and so when both $\overline{S_D}$ and $\overline{R_D}$ are set high, the status of Q and $\overline{Q}$ cannot be anticipated.
Q^0 : level of Q before the indicated steady-state input conditions were established.
$\overline{Q^0}$: level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Toggle : complement of previous state with ↓ transition of outputs

BLOCK DIAGRAM (EACH FLIP FLOP)



MITSUBISHI ELECTRIC

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	°C
T_{stg}	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC} = 4.75V$, $I_{IC} = -18mA$				-1.5	V
V_{OH}	High-level output voltage		$V_{CC} = 4.75V$, $V_I = 0.8V$, $V_I = 2V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = 4.75V$, $V_I = 0.8V$, $V_I = 2V$	$I_{OL} = 4mA$		0.25	0.4	V
				$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	J, K	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$\overline{S_D}$, $\overline{R_D}$					60	
		$\overline{T}$					80	
		J, K	$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
		$\overline{S_D}$, $\overline{R_D}$					0.3	
		$\overline{T}$					0.4	
I_{IL}	Low-level input current	J, K	$V_{CC} = 5.25V$, $V_I = 0.4V$				-0.4	mA
		$\overline{S_D}$, $\overline{R_D}$ $\overline{T}$					-0.8	
I_{OS}	Short-circuit output current (Note 3)		$V_{CC} = 5.25V$, $V_O = 0V$		-20		-100	mA
I_{CC}	Supply current		$V_{CC} = 5.25V$ (Note 4)			4	6	mA

* : All typical values are at $V_{CC} = 5V$, $Ta = 25°C$.

Note 2: S_D and R_D should not both be set to 0.4V simultaneously.

Note 3: All measurements should be done quickly, and not more than one output should be shorted at a time.

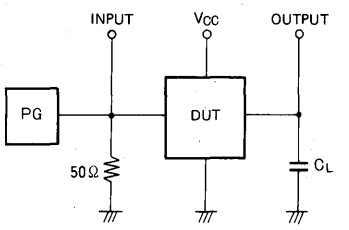
Note 4: I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, $\overline{T}$ input is grounded.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L = 15pF$ (Note 5)	30	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time from input $\overline{T}$ to output Q, $\overline{Q}$			6	20	ns
t_{PHL}				7	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{S_D}$, $\overline{R_D}$ to output Q, $\overline{Q}$			7	20	ns
t_{PHL}				7	20	ns

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOPS WITH SET AND RESET

Note 4: Measurement circuit

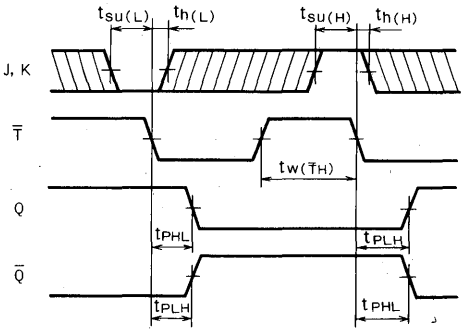


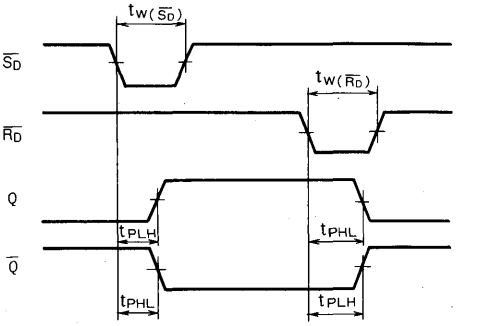
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
V_P=3V_{P-P}, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{T}H)}$	Clock input $\overline{T}$ high pulse width		20	12		ns
$t_{W(\overline{S_D}.\overline{R_D})}$	Direct set and reset inputs $\overline{S_D}$, $\overline{R_D}$ pulse width		25	4		ns
t_r	Clock rise time			650	100	ns
t_f	Clock pulse fall time			900	100	ns
$t_{SU(H)}$	Setup time high J, K to $\overline{T}$		20	12		ns
$t_{SU(L)}$	Setup time low J, K to $\overline{T}$		20	12		ns
$t_{h(H)}$	Hold time high J, K to $\overline{T}$		0	−10		ns
$t_{h(L)}$	Hold time low J, K to $\overline{T}$		0	− 6		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS113AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET

DESCRIPTION

The M74LS113AP is a semiconductor integrated circuit containing 2 J-K negative edge-triggered flip-flop circuits with discrete terminals for clock input $\overline{T}$, inputs J and K and direct set input $\overline{S_D}$.

FEATURES

- Negative edge-triggering
- Each flip-flop can be used independently
- Direct set input
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

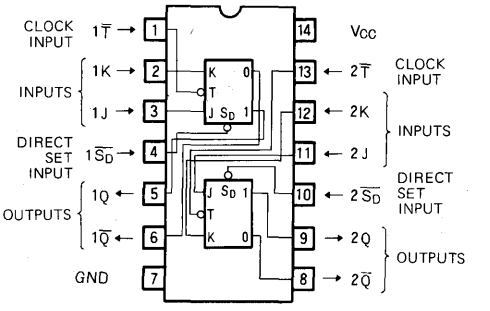
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While $\overline{T}$ is high, signals J and K are put in the read-in state, and when $\overline{T}$ changes from high to low, the J and K signals immediately before the change emerge in outputs Q and $\overline{Q}$ in accordance with the function table. By setting $\overline{S_D}$ low, Q and $\overline{Q}$ are set low and high respectively irrespective of the status of the other input signals. For use as a J-K flip-flop, $\overline{S_D}$ must be kept high.

The only difference in functions from M74LS112AP is that this IC has no $\overline{RD}$ input.

PIN CONFIGURATION (TOP VIEW)



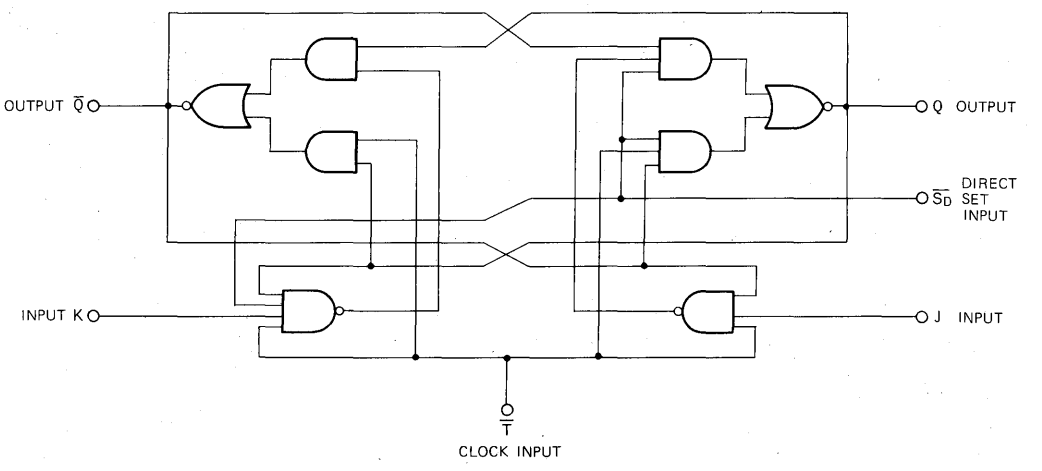
Outline 14P4

FUNCTION TABLE (Note 1)

$\overline{T}$	$\overline{S_D}$	J	K	Q	$\overline{Q}$
X	L	X	X	H	L
↓	H	H	H	Toggle	
↓	H	L	H	L	H
↓	H	H	L	H	L
↓	H	L	L	Q^0	$\overline{Q^0}$
H	H	X	X	Q^0	$\overline{Q^0}$

Note 1 ↓ : Transition from high to low-level (negative edge trigger)
X : Irrelevant
Q^0: level of Q before the indicated steady-state input conditions were established.
$\overline{Q^0}$: level of $\overline{Q}$ before the indicated steady-state input conditions were established.
Toggle : complement of previous state with ↓ transition of outputs

BLOCK DIAGRAM (EACH FLIP-FLOP)



DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	°C
T_{stg}	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				-1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	J, K	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{S_D}$					60	
		$\overline{T}$					80	
		J, K	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{S_D}$					0.3	
		$\overline{T}$					0.4	
I_{IL}	Low-level input current	J, K	$V_{CC}=5.25V$, $V_I=0.4V$				-0.4	mA
		$\overline{S_D}$ $\overline{T}$					-0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		-20		-100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 3)			4	6	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25°C$

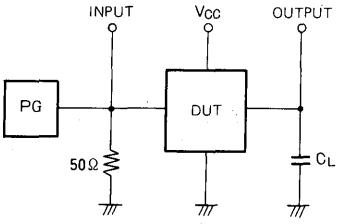
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: Supply current measurements should be done with Q and $\overline{Q}$ set alternately high and $\overline{T}$ should be set low during actual measurement.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L=15pF$ (Note 4)	30	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{T}$ to Q, $\overline{Q}$			8	20	ns
t_{PHL}				7	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{S_D}$ to Q, $\overline{Q}$			8	20	ns
t_{PHL}				7	20	ns

Note 4: Measurement circuit



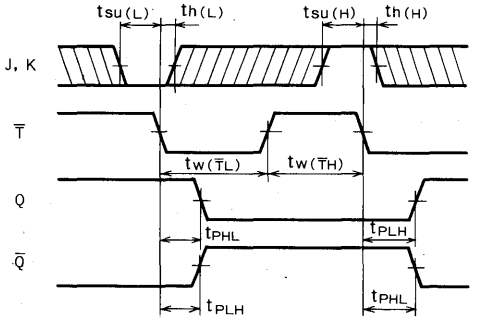
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.

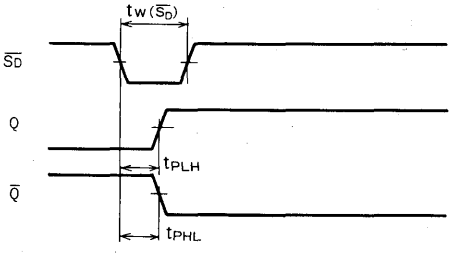
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T}H)}$	Clock input $\overline{T}$ high pulse width		20	13		ns
$t_{w(\overline{S_D})}$	Direct set pulse width		25	10		ns
t_r	Clock rise time			650	100	ns
t_f	Clock fall time			900	100	ns
$t_{SU(H)}$	Setup time high J, K to $\overline{T}$		20	9		ns
$t_{SU(L)}$	Setup time low J, K to $\overline{T}$		20	12		ns
$t_{h(H)}$	Hold time high J, K to $\overline{T}$		0	−10		ns
$t_{h(L)}$	Hold time low J, K to $\overline{T}$		0	−5		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS114AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET, COMMON RESET, AND COMMON CLOCK

DESCRIPTION

The M74LS114AP is a semiconductor integrated circuit containing 2 J-K flip-flop circuits with common terminals for clock input T and direct reset input $\overline{R_D}$ and discrete terminals for inputs J and K and direct set inputs $\overline{S_D}$.

FEATURES

- Negative edge-triggering
- Common clock input and direct reset input
- Discrete direct set input
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20~+75°C)

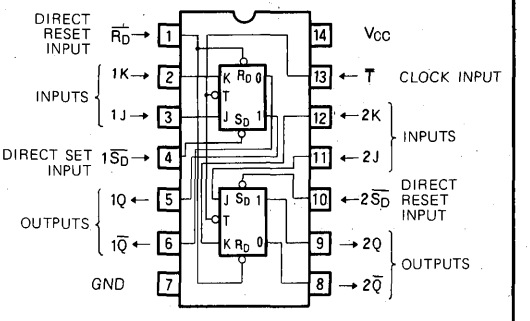
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

While $\overline{T}$ is high, signals J and K are put in the read-in state, and when $\overline{T}$ changes from high to low, the J and K signals immediately before the change emerge in outputs Q and $\overline{Q}$ in accordance with the function table. By using $\overline{S_D}$ and $\overline{R_D}$ this IC can be made into a direct R-S clip-flop. When both $\overline{S_D}$ and $\overline{R_D}$ are low, Q = $\overline{Q}$ = high. However, when both of them change to high at the same time, the status of Q and $\overline{Q}$ cannot be anticipated. For use as a J-K flip-flop, $\overline{S_D}$ and $\overline{R_D}$ must be kept in high.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

FUNCTION TABLE (Note 1)

$\overline{T}$	$\overline{S_D}$	$\overline{R_D}$	J	K	Q	$\overline{Q}$
X	L	H	X	X	H	L
X	H	L	X	X	L	H
X	L	L	X	X	H*	H*
↓	H	H	H	H	Toggle	
↓	H	H	L	H	L	H
↓	H	H	H	L	H	L
↓	H	H	L	L	Q^0	$\overline{Q^0}$

Note 1 ↓ : Transition from high to low-level (negative edge trigger)

X : Irrelevant

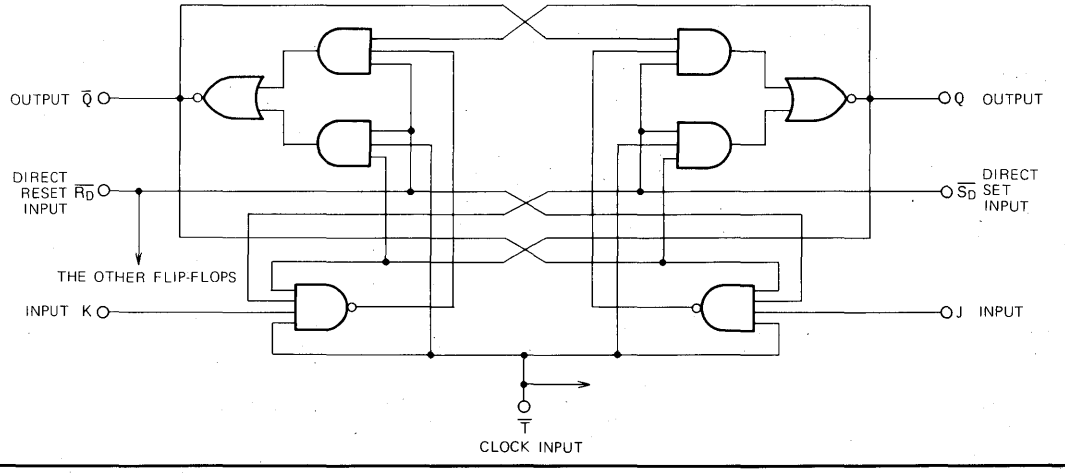
* : Q = $\overline{Q}$ = high when $\overline{S_D}$ = $\overline{R_D}$ = low and so when both $\overline{S_D}$ and $\overline{R_D}$ are set high, the status of Q and $\overline{Q}$ cannot be anticipated.

Q^0 : Status of output before ↓ change.

$\overline{Q^0}$: level of Q before the indicated steady-state input conditions were established.

Toggle : complement of previous state with ↓ transition of outputs

BLOCK DIAGRAM (EACH FLIP-FLOP)



MITSUBISHI ELECTRIC

M74LS114AP

DUAL J-K NEGATIVE EDGE-TRIGGERED FLIP FLOP WITH SET, COMMON RESET, AND COMMON CLOCK

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20 \sim +75$	°C
Tstg	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				-1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$ $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$ $I_{OL}=8mA$		0.25 0.35	0.4 0.5	V V
I_{IH}	High-level input current	J, K	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{S_D}$					60	
		$\overline{R_D}$					120	
		$\overline{T}$					160	
		J, K	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{S_D}$					0.3	
		$\overline{R_D}$					0.6	
		$\overline{T}$					0.8	
I_{IL}	Low-level input current	J, K	$V_{CC}=5.25V$, $V_I=0.4V$ (Note 2)				-0.4	mA
		$\overline{S_D}$					-0.8	
		$\overline{R_D}$ $\overline{T}$					-1.6	
I_{OS}	Short-circuit output current (Note 3)		$V_{CC}=5.25V$, $V_O=0V$		-20		-100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 4)			4	6	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25°C$

Note 2: $\overline{S_D}$ and $\overline{R_D}$ should not both be set to 0.4V simultaneously.

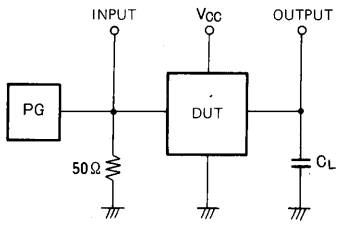
Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: Supply current measurements should be done with Q and $\overline{Q}$ set alternately high and $\overline{T}$ should be set low during actual measurement.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L=15pF$ (Note 4)	30	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{T}$ to Q, $\overline{Q}$			7	20	ns
t_{PHL}				7	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{S_D}$, $\overline{R_D}$ to Q, $\overline{Q}$			8	20	ns
t_{PHL}				7	20	ns

Note 4: Measurement circuit

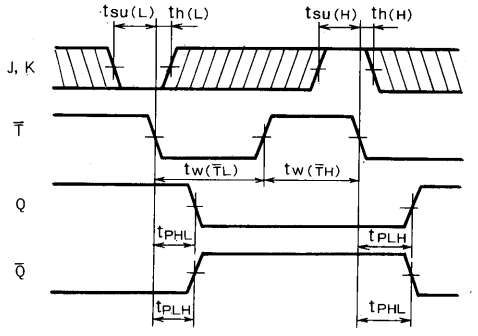


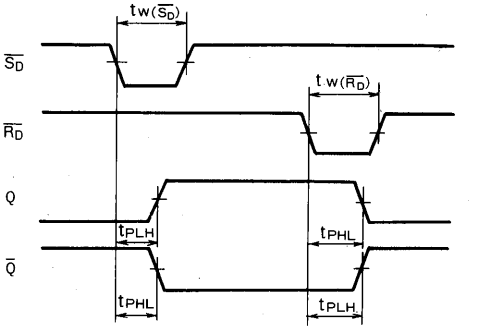
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Type	Max	
$t_{w(\overline{T}H)}$	Clock input $\overline{T}$ high pulse width		20	12		ns
$t_{w(\overline{S_D}.\overline{R_D})}$	Direct set, reset pulse width		25	4		ns
t_r	Clock rise time			650	100	ns
t_f	Clock fall time			900	100	ns
$t_{SU(H)}$	Setup time high J, K to $\overline{T}$		20	11		ns
$t_{SU(L)}$	Setup time low J, K to $\overline{T}$		20	13		ns
$t_{h(H)}$	Hold time high J, K to $\overline{T}$		0	−11		ns
$t_{h(L)}$	Hold time low J, K to $\overline{T}$		0	− 6		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS122P

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

DESCRIPTION

The M74LS122P is a semiconductor integrated circuit containing a retriggerable monostable multivibrator circuits with a direct reset input.

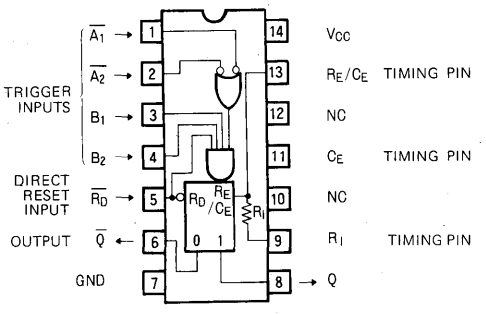
FEATURES

- Long pulse widths can be generated using the retriggerable function.
- Output pulses can be stopped at any time with direct reset inputs.
- $\overline{A}$, B complementary inputs provided.
- High breakdown input voltage ($V_I \geqq 15V$)
- Q and $\overline{Q}$ outputs provided
- Wide operating temperature range ($T_a = -20 \sim +75°C$)
- Internal timing resistance provided ($R_I = 10k\Omega$)

APPLICATION

General purpose, for use in industrial and consumer equipment

PIN CONFIGURATION (TOP VIEW)



$R_I = 10k\Omega$

NC: NO CONNECTION

Outline 14P4

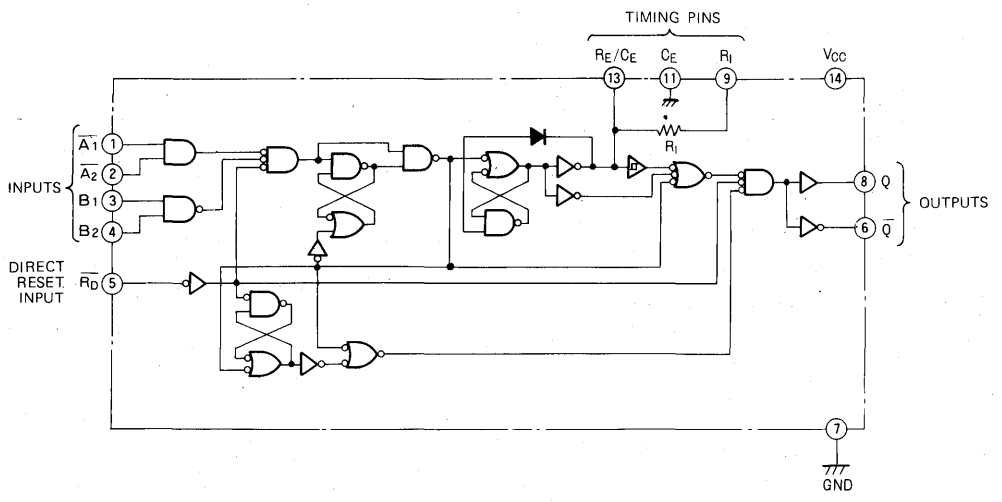
FUNCTIONAL DESCRIPTION

As shown in Fig. 1, the timing pins R_E/C_E and C_E are connected to the external resistance R_T and static capacitance C_T, and when a triggering pulse is applied to inputs $\overline{A_1}$, $\overline{A_2}$ and B_1 or B_2, a positive pulse appears at output Q, with a negative pulse appearing at $\overline{Q}$. When the internal timing resistance is used (Fig. 2 (a)), the static capacitance C_T is connected to the C_E and R_E/C_E pins. Thus, connecting the R_I and V_{CC} pins causes the device to function as a monostable multivibrator and eliminates the need for an external resistance. The width of the pulse (t_w) appearing at output can be controlled by the values for R_T and C_T. (When the internal timing resistance is used, the setting is made with C_T). The trigger is affected by $\overline{A_1}$ or $\overline{A_2}$ switching from high to low-level, or by B_1 or B_2 switching from low to high.

The retriggering function is used when a wide output pulse width is desired. It is obtained by triggering $\overline{A_1}$ or $\overline{A_2}$, or B_1 or B_2 prior to the pulse being fully output, thus extending its length (See Fig. 2 (b)).

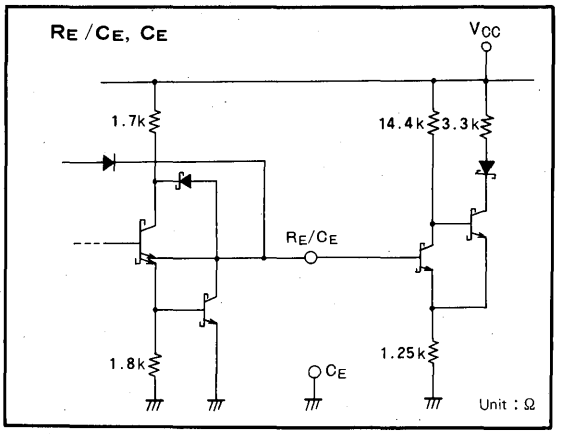
Dropping the direct reset input $\overline{R_D}$ to low-level immediately causes Q to go low-level and $\overline{Q}$ to be set high, regardless of the present output status. This allows the $\overline{R_D}$ signal to be used to shorten the output pulse width to the desired length (See Fig. 2 (c)). A precaution worth noting is that when $\overline{A_1}$ or $\overline{A_2}$ is low-level and $B_1 = B_2$ = high, and $\overline{R_D}$ is switched from low to high-level, the trigger will be activated changing the status of Q and $\overline{Q}$.

BLOCK DIAGRAM (Monostable multivibrator)



RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

TIMING PIN EQUIVALENT CIRCUIT



FUNCTION TABLE (Note 1)

$\overline{R_D}$	$\overline{A_1}$	$\overline{A_2}$	B_1	B_2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

Note 1. ↑ : Transition from low to high (positive edge trigger)
↓ : Transition from high to low (negative edge trigger)
⎍ : Positive-going one-shot trigger
⎎ : Negative-going one-shot trigger
X : Irrelevant

OPERATIONAL DESCRIPTION

1. Using the timing pins

Figure 1 shows the timing pins R_E/C_E and C_E connected to the external resistance R_T and static capacitance C_T respectively. An alternate method to connecting R_T is to connect the R_1 and V_{CC} Pins together. When a electrolytic capacitor is used as C_T, connect R_E/C_E to the positive (+) side and C_E to the negative (-) side. In this case, the device functions as a TTL IC, and eliminates the requirement for a switching diode. Where noise causes operational problems, connect the C_E pin to GND (located near the 7 pin) as shown by the dashed line in the diagram.

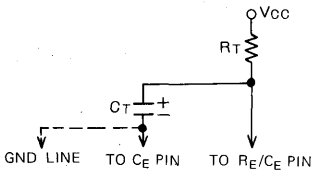


Fig. 1 Connecting External Resistance R_T and Static Capacitance C_T to Timing Pins R_E/C_E and C_E

2. Output Pulse Width t_w

Output pulse width t_w is set by the values of R_T and C_T as shown below. When R_1 is used, R_T should equal 10kΩ.

2-1. When $C_T > 1000pF$, $t_w = K \cdot R_T \cdot C_T \cdot (1 \pm 0.1)$(ns).
For the value for K, also refer to Typical Characteristics, K — C_T characteristics. (The value for R_T does not affect K.)
Units for R_T and C_T are kΩ and pF respectively.

2-2. When $C_T \leqq 1000pF$, refer to the output pulse width vs. C_T, R_T shown in the Typical Characteristics section in back of this specification sheet.

3. Controlling Output Pulse Width

The width of the output pulse can be controlled using three methods, based on the presence or absence of the trigger signal and $\overline{R_D}$ signal.

3-1. Used as conventional device
Figure 2(a) shows the device used in the normal monostable multivibrator mode. Here, output pulse width t_w is set using the equations and diagram shown in the above section.

3-2. Extending the width of the output pulse by retriggering
Figure 2(b) shows that the output pulse can be extended to any width desired by triggering again before the pulse is fully output.

3-3. Shortening the width of the output pulse by signal $\overline{R_D}$
Figure 2(c) shows that the $\overline{R_D}$ signal can be used to terminate the output pulse initiated by the trigger. The output pulse can be shortened to any width desired.

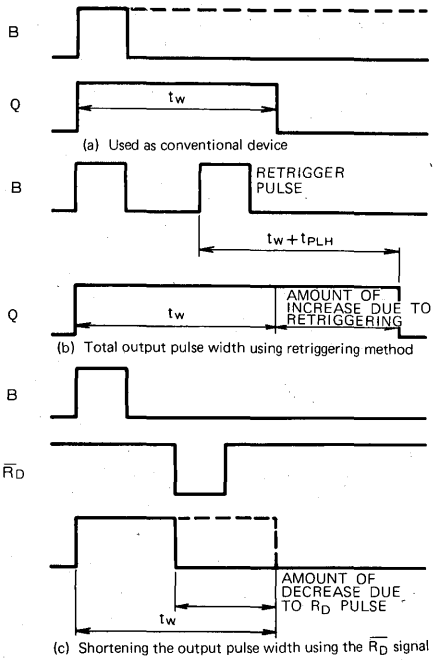


Fig. 2 Output Pulse Width Control

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RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

4. Precautions

4-1. The retriggering pulse should follow the trigger by $0.22C_T$ (ns), where the unit for C_T is picofarads. During this interval, the retriggering pulse will be ineffective.

4-2. The wiring used to connect the external C_T and R_T should be shielded from noise, and be as short as possible (less than 3cm) to minimize line capacitance and noise-induced errors.

4-3. Use a capacitor with good high-frequency characteristics and a value of 0.01 to 0.1μF to connect V_{CC} and GND.

4-4. Note that an output pulse will be produced when the power to the device is turned on.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA
R_T	External timing resistance		5		260	kΩ
C_T	External timing capacitance		No limits			
C_R	R_E/C_E pin line capacitance				50	pF

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.5		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 2)			6	11	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

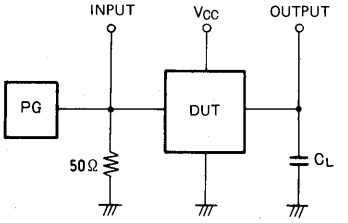
Note 2. I_{CC} is measured with R_E/C_E, C_E open. 4.5V is applied to $\overline{R_D}$, $\overline{A_1}$, $\overline{A_2}$, B_1 and B_2, with the measurement taken after $\overline{A_1}$ and $\overline{A_2}$ are momentarily dropped to 0V, then raised to 4.5V.

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time, from input $\overline{A_1}$, $\overline{A_2}$ to output Q	C_T=0pF R_T=5kΩ C_L=15pF (Note 3)		19	33	ns
t_{PLH}	Low-to-high-level output propagation time, from input B_1, B_2 to output Q			20	44	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{A_1}$, $\overline{A_2}$ to output $\overline{Q}$			21	45	ns
t_{PHL}	High-to-low level output propagation time, from input B_1, B_2 to output $\overline{Q}$			23	56	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q			18	27	ns
t_{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output Q			23	45	ns
$t_{WQ(min)}$	Minimum output pulse width, from inputs $\overline{A_1}$, $\overline{A_2}$, B_1 and B_2 to output Q			70	200	ns
t_{WQ}	Output pulse width, from input $\overline{A}$, B to output Q	C_T=1000pF, R_T=10kΩ C_L=15pF (Note 3)	4	4.55	5	μs

Note 3. Measurement Circuit

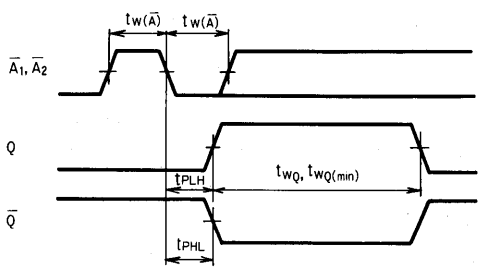


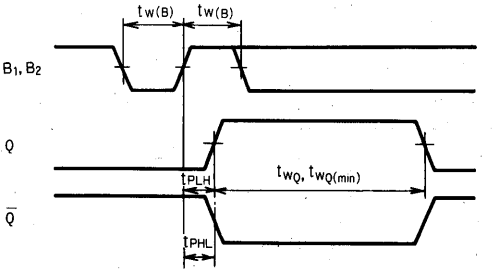
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz (t_{WQ} measurement: 100kHz), t_r = 6ns,
t_f = 6ns, t_w = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

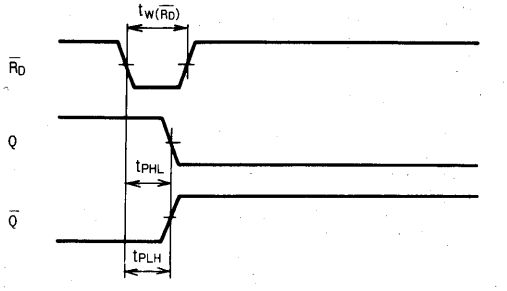
TIMING REQUIREMENTS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{A_1}, \overline{A_2})}$	Trigger $\overline{A}$ pulse width		40	15		ns
$t_{W(B_1, B_2)}$	Trigger B pulse width		40	10		ns
$t_{W(\overline{R_D})}$	Direct reset $\overline{R_D}$ pulse width		40	15		ns

TIMING DIAGRAM (Reference level = 1.3V)







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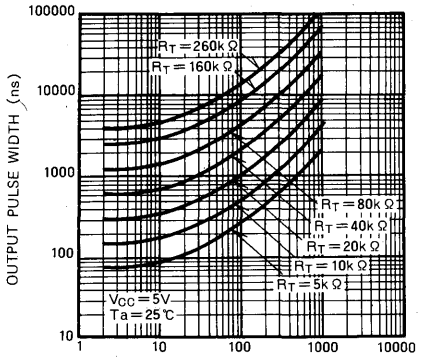
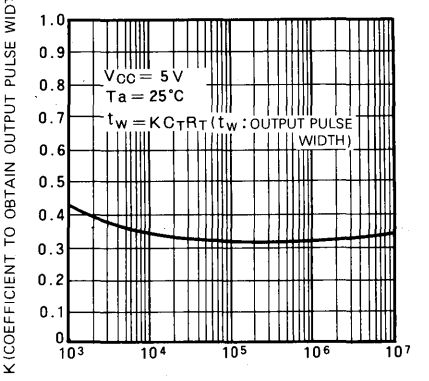
RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

TYPICAL CHARACTERISTICS

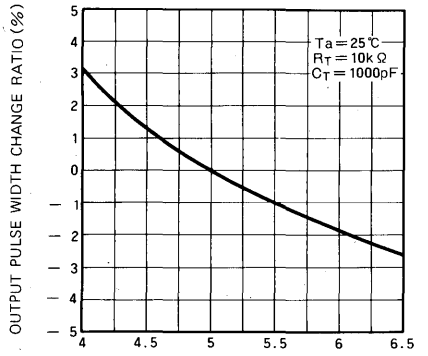
OUTPUT PULSE WIDTH vs C_T, R ($C_T \leqq 1000$ pF)



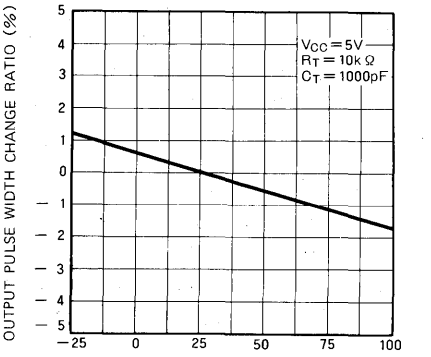
K VS C_T ($C > 1000$ pF)



CHANGE RATIO OF OUTPUT PULSE vs POWER SUPPLY VOLTAGE



CHANGE RATIO OF OUTPUT PULSE vs AMBIENT TEMPERATURE



M74LS123P

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

DESCRIPTION

The M74LS123P is a semiconductor integrated circuit containing two retriggerable monostable multivibrator circuits with direct reset inputs.

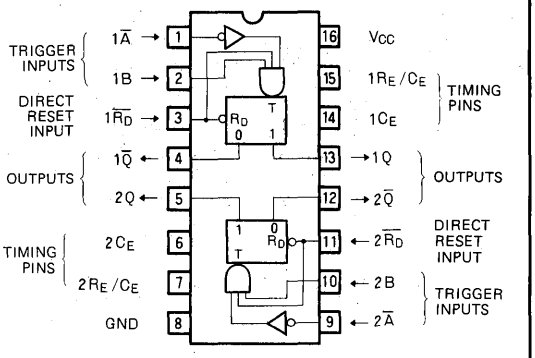
FEATURES

- Long pulse widths can be generated using the retriggerable function
- Output pulses can be stopped at any time with direct reset inputs
- $\overline{A}$, B complementary inputs provided
- High breakdown input voltage ($V_I \geqq 15V$)
- Q and $\overline{Q}$ outputs provided
- Wide operating temperature range (T_a=–20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

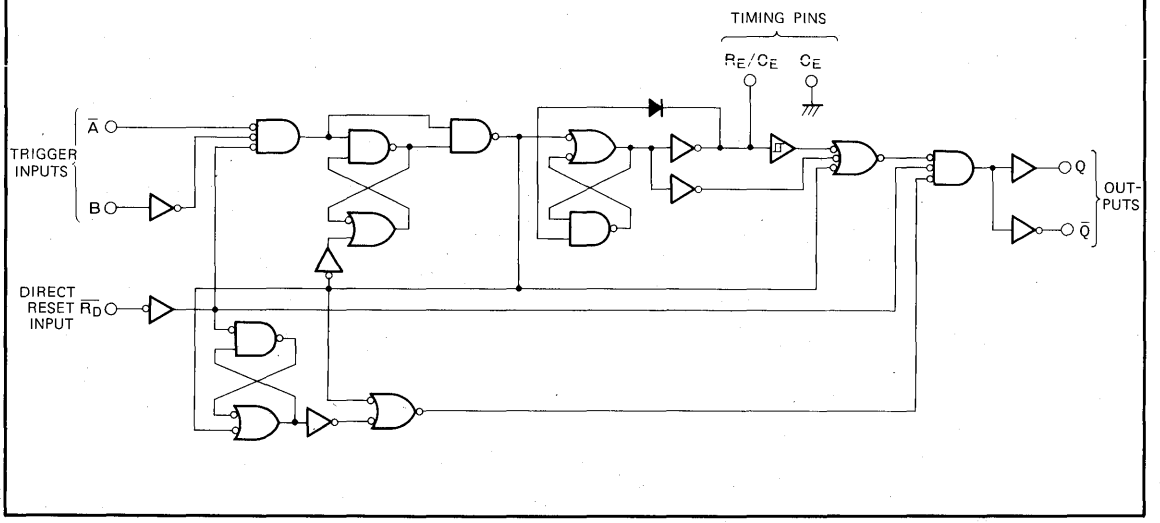
FUNCTIONAL DESCRIPTION

Positive pulses appear in output Q and negative pulses in output $\overline{Q}$ by connecting external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E, as shown in Fig. 1 on the next page, and by applying a trigger from input $\overline{A}$ or B. (Fig. 2(a)) The width tw of the pulses appearing in the outputs is set by R_T and C_T. When $\overline{A}$ changes from high to low or when B changes from low to high, the trigger is applied.

The retriggerable function is used to obtain long output pulse widths and when the trigger is applied from $\overline{A}$ or B immediately before the output pulse is completed, the output pulse width can be extended. (Fig. 2(b))

Q can be reset immediately low and $\overline{Q}$ high by setting direct reset input $\overline{R_D}$ low irrespective of the status of the outputs. The output pulse width can therefore be made as short as preferred by the $\overline{R_D}$ signal. (Fig. 2(c)) When $\overline{R_D}$ changes from low to high with $\overline{A}$ at low and B at high, the trigger is applied and the status of Q and $\overline{Q}$ changes.

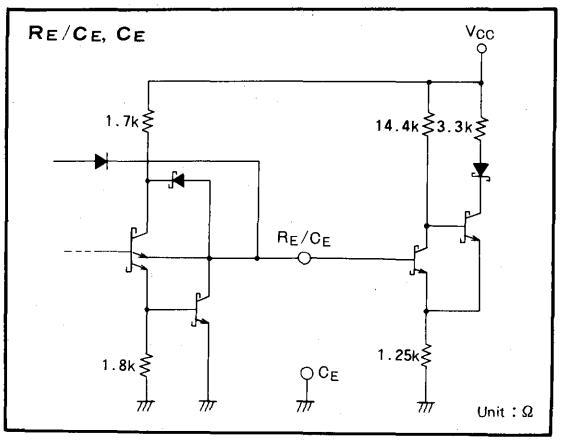
BLOCK DIAGRAM (EACH MONOSTABLE MULTIVIBRATOR)



MITSUBISHI ELECTRIC

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

TIMING PIN EQUIVALENT CIRCUIT



FUNCTION TABLE (Note 1)

$\overline{R_D}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

Note 1. ↑ : Transition from low to high. (positive edge triggering)
↓ : Transition from high to low. (negative edge triggering)
⎍ : Positive one-shot operation.
⎍ : Negative one-shot operation.
X : Irrelevant

OPERATION DESCRIPTION

1. How to use the timing pins

As shown in Fig. 1, external resistor R_T and capacitor C_T are connected to timing pins R_E/C_E and C_E. Connect the positive to the R_E/C_E side and the negative to the C_E side when using C_T with polarity. In this case, it is not necessary to connect a switching diode required with the same type of TTL IC. With malfunctions caused by noise, connect C_E to the GND line (neighboring on pin 8) as shown by the dotted line in Fig. 1.

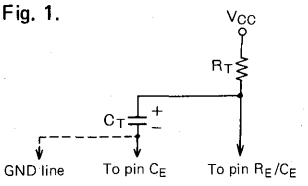


Fig. 1 Connection of external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E

2. Output pulse width t_w

The output pulse width t_w is set by R_T and C_T

2-1. When CT is greater than 1000pF

$t_W = 0.45 \cdot R_T \cdot C_T$ (ns) $\times (1 \pm 0.1)$

Refer to K-C_T characteristics indicated in TYPICAL CHARACTERISTICS for value of K. (No change is brought to K by value of R_T.)

R_T is measured in kilohms and C_T in picofarads

Depending on the product, fluctuations in the order of 3/-10%may occur.

R_T is measured in kilohms and C_T in picofarads

2-2. When CT is equal to or less than 1000pF

Refer to the output pulse width versus–C_T, R_T given in the typical characteristics.

3. Output pulse width control

The output pulse width can be controlled in 3 ways by using, or not using, the trigger signal and $\overline{R_D}$ signal.

3-1. Normal use

This is the normal method of use as a regular monostable multivibrator such as that shown in Fig. 2(a) and the output pulse width t_w can be set as for the formula and figure in section 2 above.

3-2. Extension of output pulse width with retrigger function

As shown in Fig. 2(b), the output pulse width can be extended as desired by applying a trigger pulse before the output pulse is completed.

3-3. Shortening of the output pulse width with $\overline{R_D}$ signal

As shown in Fig. 2(c), the output pulse which has been generated by the trigger signal can be terminated with the $\overline{R_D}$ signal and it is possible to shorten its width as required.

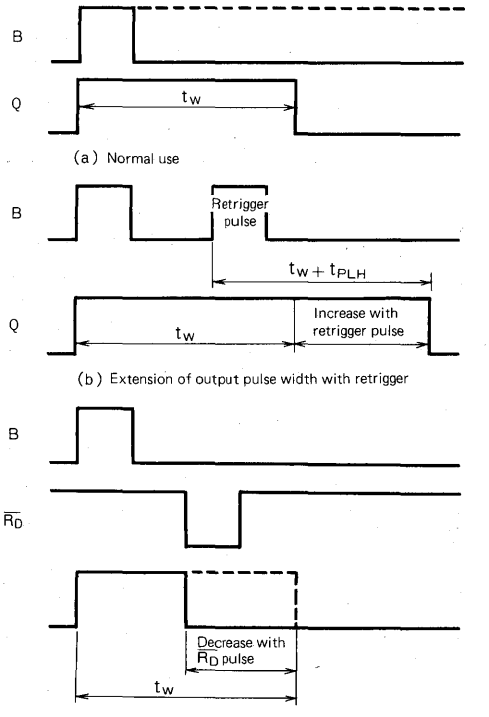


Fig. 2 Output pulse width control

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

4. Precautions with use

4-1. Apply the retrigger pulse after a wait of $0.22C_T$ (ns) upon application of the trigger pulse. C_T is measured in picofarads. The retrigger pulse during this period is ineffective.

4-2. In order to minimize the floating capacitance and to safeguard against malfunction caused by noise, make the R_T and C_T wiring as short as possible and avoid signal wires which may be conducive to noise.

4-3. Connect an external capacitor of 0.01~0.1μF with good high-frequency characteristics between pins V_{CC} and GND.

4-4. The output pulse is generated when the power is switched on.

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA
R_T	External timing resistance		5		260	kΩ
C_T	External timing capacitance		None			
C_R	R_E/C_E pin wiring capacitance				50	pF

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}= 4 mA		0.25	0.4	V
		V_I=0.8V, V_I=2V	I_{OL}= 8 mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 3)			12	20	mA

* : All typical values are at V_{CC}=5V, T_a=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

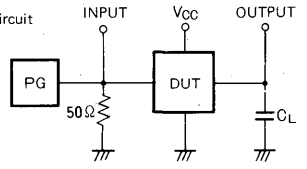
Note 3: I_{CC} is measured with R_E/C_E and C_E open, 4.5V applied to $\overline{R_D}$, $\overline{A}$ and B and $\overline{A}$ set from 0V momentarily to 4.5V.

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time, from input $\overline{A}$ to output Q	C_T = 0 pF R_T = 5 kΩ C_L = 15 pF (Note 4)		19	33	ns
t_{PLH}	Low-to-high-level output propagation time, from input B to output Q			20	44	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{A}$ to output $\overline{Q}$			21	45	ns
t_{PHL}	High-to-low-level output propagation time, from input B to output $\overline{Q}$			23	56	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q			18	27	ns
t_{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output $\overline{Q}$			23	45	ns
$t_{WQ(min)}$	Minimum output pulse width, from inputs $\overline{A}$, B to output Q			66	200	ns
t_{WQ}	Output pulse width, from inputs $\overline{A}$, B to output Q	C_T = 1000 pF, R_T = 10 kΩ C_L = 15 pF (Note 4)	4	4.55	5	μs

Note 4: Measurement circuit

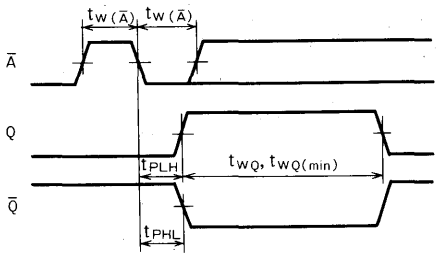


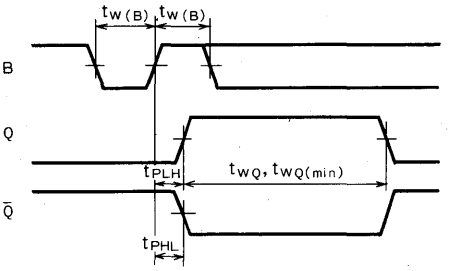
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz (100kHz with t_{WQ} measurement), t_r = 6ns, t_f = 6ns, $t_w \geqq 40$ns, V_P = 3V_{P-P}, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance

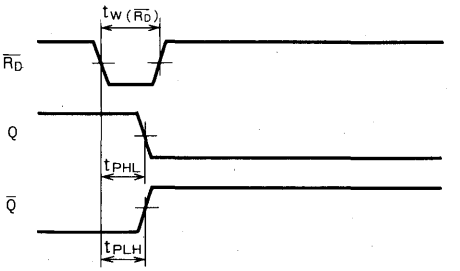
TIMING REQUIREMENTS (V_{CC} = 5 V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{A})}$	Trigger input $\overline{A}$ pulse width		40	15		ns
$t_{W(B)}$	Trigger input B pulse width		40	10		ns
$t_{W(\overline{R_D})}$	Direct reset input pulse width $\overline{R_D}$		40	15		ns

TIMING DIAGRAM (Reference level = 1.3V)



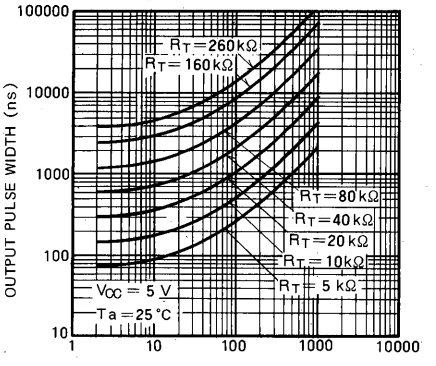




DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

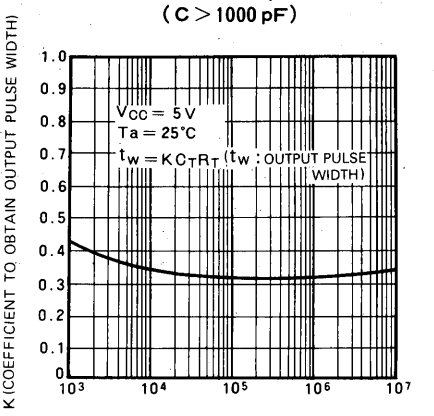
TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH VS C_T, R_T ($C_T \leqq 1000$ pF)

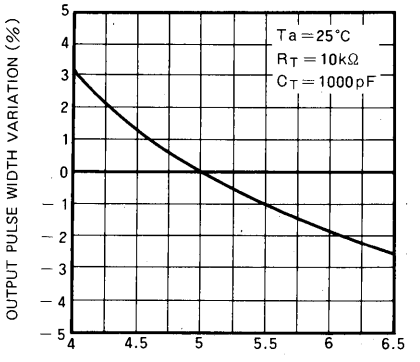


Note 5. Error within ±20% of output width given in the figure above.

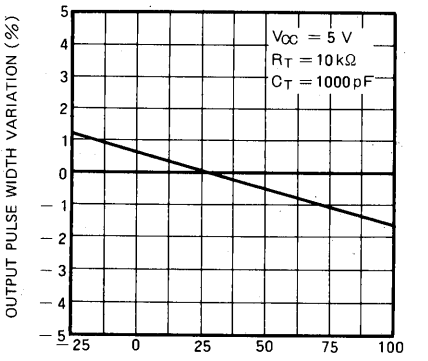
K VS C_T ($C > 1000$ pF)



OUTPUT PULSE WIDTH VARIATION VS SUPPLY VOLTAGE



OUTPUT PULSE WIDTH VARIATION VS AMBIENT TEMPERATURE



M74LS125AP

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS125AP is a semiconductor integrated circuit containing 4 buffers with 3-state outputs and is provided with an output control input $\overline{OC}$ which is independent for each buffer.

FEATURES

- Provided with output control input independent for each of 4 circuits
- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 52mW typical)
- High speed (t_{pd} = 8ns typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

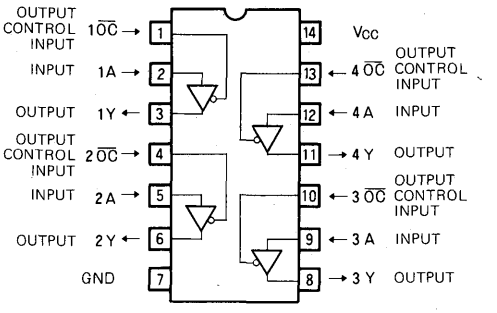
When $\overline{OC}$ is low, high appears in the output Y if input A is high and low appears if A is low. When $\overline{OC}$ is high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

FUNCTION TABLE (Note 1)

$\overline{OC}$	A	Y
L	L	L
L	H	H
H	X	Z

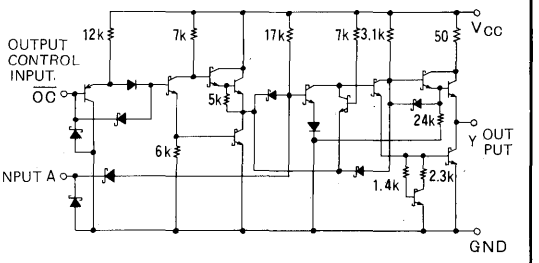
Note 1: X : irrelevant
Z : high-impedance

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ*	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$			−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-2.6mA$	2.4	3.1		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $I_{OL}=12mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$, $I_{OL}=24mA$		0.35	0.5	V
I_{OZH}	Off-state high-level output current	$V_{CC}=5.25V$, $V_{I(\overline{OC})}=2V$, $V_O=2.4V$			20	μA
I_{OZL}	Off-state low-level output current	$V_{CC}=5.25V$, $V_{I(\overline{OC})}=2V$, $V_O=0.4V$			−20	μA
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$			20	μA
		$V_{CC}=5.25V$, $V_I=10V$			0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$			−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$	−40		−225	mA
I_{CCZ}	Supply current, all outputs off	$V_{CC}=5.25V$, $V_I=0V$, $V_{I(\overline{OC})}=4.5V$		11	20	mA

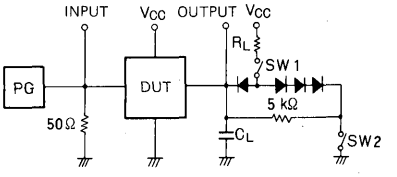
* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input A to output Y	$C_L=45pF$ (Note 3)		7	15	ns
t_{PHL}				10	18	ns
t_{PZH}	Output enable time to high-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		12	20	ns
t_{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		15	25	ns
t_{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		13	20	ns
t_{PLZ}	Output disable time from low-level	$R_L=667\Omega$ $C_L=5pF$ (Note 3)		13	20	ns

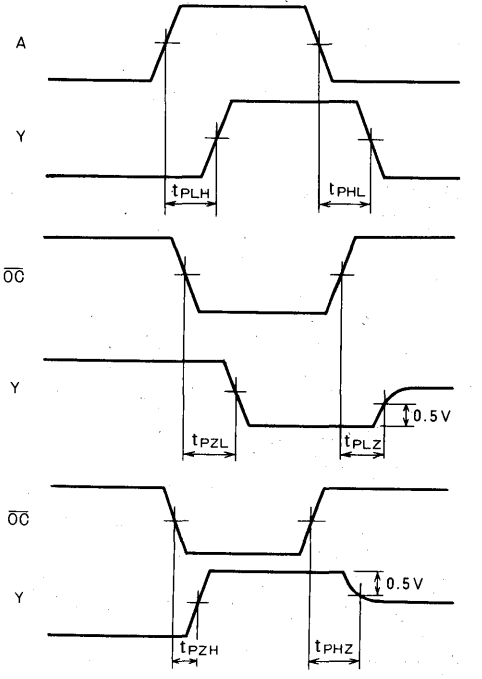
Note 3: Measurement circuit



Parameter	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, $V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.
(2) All diodes are switching diodes ($t_{rr} \leqq 4ns$)
(3) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



MITSUBISHI ELECTRIC

M74LS126AP

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS126AP is a semiconductor integrated circuit containing 4 buffers with 3-state outputs and is provided with an output control input OC which is independent for each buffer.

FEATURES

- Provided with output control input independent for each of 4 circuits
- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 59mW typical)
- High speed (t_{pd} = 10ns typical)
- Wide operating temperature range (T_a = 20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

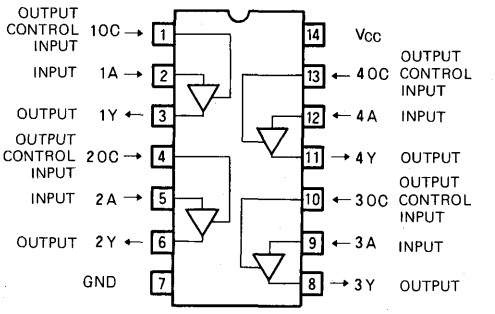
When OC is high, high appears in the output Y if input A is high and low appears if A is low. When OC is low, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

FUNCTION TABLE (Note 1)

OC	A	Y
H	L	L
H	H	H
L	X	Z

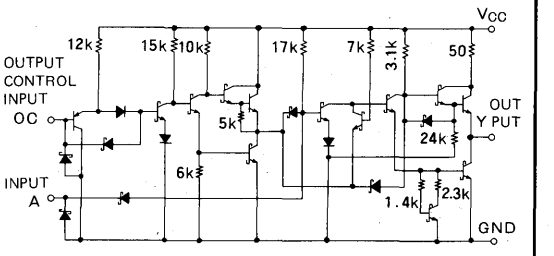
Note 1: X : irrelevant
Z : high-impedance

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

QUADRUPLE BUS BUFFER GATE WITH 3-STATE OUTPUT

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$			−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-2.6mA$	2.4	3.1		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$ $I_{OL}=12mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$ $I_{OL}=24mA$		0.35	0.5	V
I_{OZH}	Off-state high-level output current	$V_{CC}=5.25V$, $V_{I(OC)}=0.8V$, $V_O=2.4V$			20	μA
I_{OZL}	Off-state low-level output current	$V_{CC}=5.25V$, $V_{I(OC)}=0.8V$, $V_O=0.4V$			−20	μA
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$			20	μA
		$V_{CC}=5.25V$, $V_I=10V$			0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$			−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$	−40		−225	mA
I_{CCZ}	Supply current, all outputs off	$V_{CC}=5.25V$, $V_I=0V$		12	22	mA

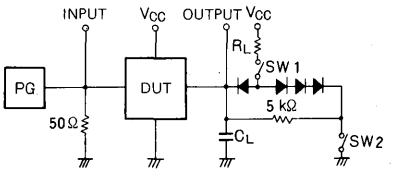
* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input A to output Y	$C_L=45pF$ (Note 3)		7	15	ns
t_{PHL}				10	18	ns
t_{PZH}	Output enable time to high-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		14	25	ns
t_{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		16	35	ns
t_{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		16	25	ns
t_{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		12	25	ns

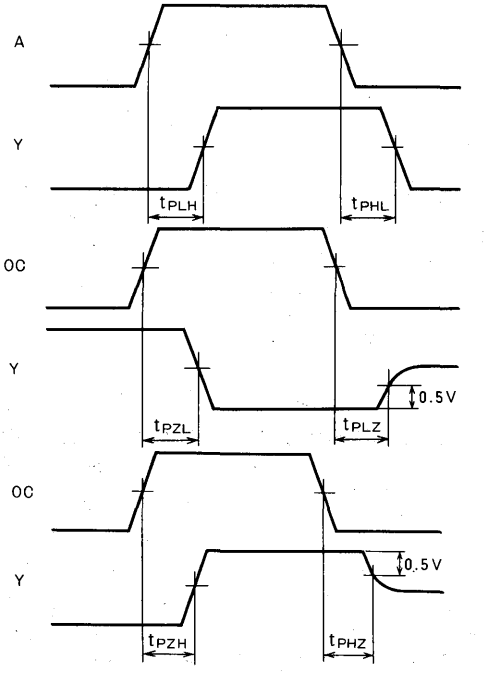
Note 3: Measurement circuit



Parameter	SW 1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) All diodes are switching diodes ($t_{rr} \leqq 4ns$)
(3) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



M74LS132P

QUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

DESCRIPTION

The M74LS132P is a semiconductor integrated circuit containing four 2-input positive-logic NAND gates having a Schmitt trigger function and negative-logic NOR gates.

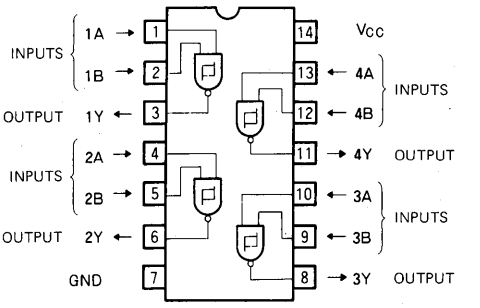
FEATURES

- Suitable for waveform shaping applications
- Wide hysteresis width (0.8V typical) and high noise margin
- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 35.2mW typical)
- High speed (t_{pd} = 13ns typical)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

FUNCTIONAL DESCRIPTION

The use of Schottky TTL technology has enabled the achievement of input high breakdown voltage, high speed, low power dissipation, and high fan-out. With positive feedback applied in the circuit, the hysteresis width is 0.8V (typical). Accordingly, the noise margin is high. Even slow changing input signals result in a shaped waveform output without causing oscillation.

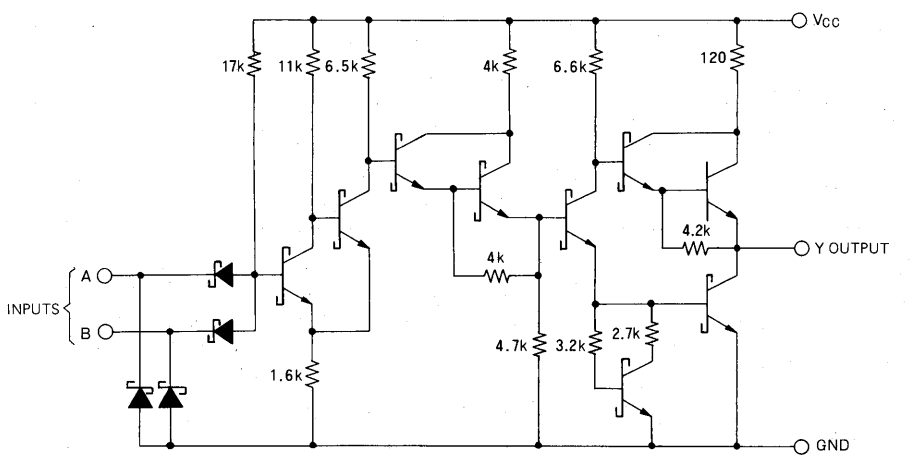
When inputs A and B are high, output Y is low, and when either or both inputs are low, Y is high.

Refer to M74LS14P for the typical characteristics.

FUNCTION TABLE

A	B	Y
L	L	H
H	L	H
L	H	H
H	H	L

CIRCUIT SCHEMATIC (EACH SCHMITT TRIGGER)



UNIT : Ω

QUADRUPLE 2-INPUT POSITIVE NAND SCHMITT TRIGGER

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{T+}	Positive-going threshold voltage	V_{CC} = 5V		1.4	1.6	1.9	V
V_{T-}	Negative-going threshold voltage	V_{CC} = 5V		0.5	0.8	1	V
$V_{T+} - V_{T-}$	Hysteresis width	V_{CC} = 5V		0.4	0.8		V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V, V_I = 0.5V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, V_I = 1.9V	I_{OL} = 4mA		0.25	0.4	V
			I_{OL} = 8mA		0.35	0.5	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5V, $V_I = V_{T+}$			−0.14		mA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5V, $V_I = V_{T-}$			−0.18		mA
I_{IH}	High-level input current	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = 5.25V, V_I = 0V			5.9	11	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = 5.25V, V_I = 4.5V			8.2	14	mA

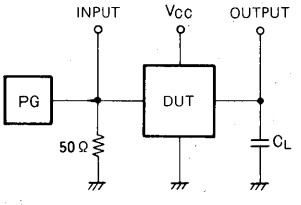
* : All typical values are at V_{CC} = 5V, Ta = 25℃

Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	C_L = 15pF (Note 2)		12	22	ns
t_{PHL}	High-to-low-level output propagation time			14	22	ns

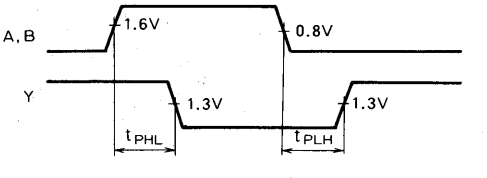
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω.

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM



MITSUBISHI ELECTRIC

M74LS133P

SINGLE 13-INPUT POSITIVE NAND GATE

DESCRIPTION

The M74LS133P is a semiconductor integrated circuit containing one 13-input positive-logic NAND gate, usable as a negative logic NOR gate.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- Low power dissipation (P_d = 2.5mW typical)
- High speed (t_{pd} = 11ns typical)
- Low output impedance
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The use of PNP transistors for the inputs and active pull-up transistors for the outputs enables input high breakdown voltage, high speed, low power dissipation and high fan-out.

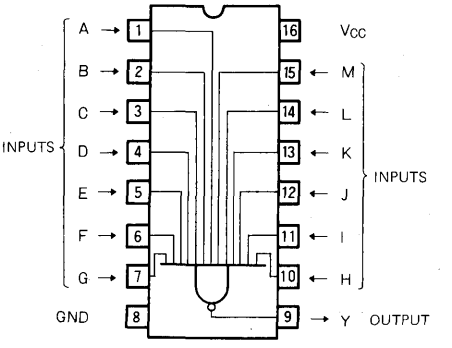
When inputs A through M are high, output Y is low and when one or more of the inputs is low, output Y is high.

FUNCTION TABLE

A	N	Y
L	L	H
H	L	H
L	H	H
H	H	L

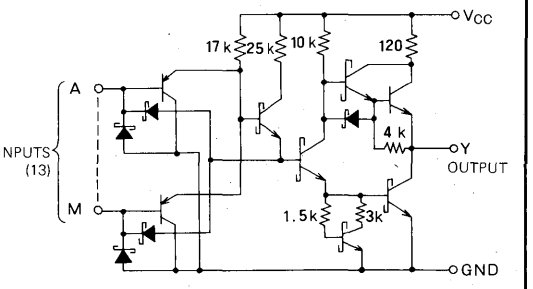
N=B・C・D・E・F・G・H・I ・J・K・L・M

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

SINGLE 13-INPUT POSITIVE NAND GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$, $V_I = 0.8V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$, $V_I = 2V$	$I_{OL} = 4mA$		0.25	0.4	V
			$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC} = 5.25V$, $V_O = 0V$		−20		−100	mA
I_{CCH}	Supply current, all inputs high	$V_{CC} = 5.25V$, $V_I = 0V$			0.35	0.5	mA
I_{CCL}	Supply current, all inputs low	$V_{CC} = 5.25V$, V_I = Open			0.6	1.1	mA

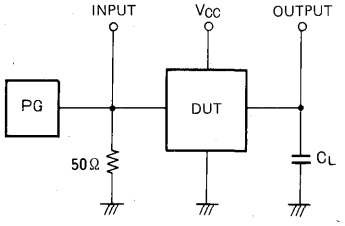
* : All typical values are at $V_{CC} = 5V$, $T_a = 25°C$

Note 1: All measurements should be done quickly.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level/high-to-low-level output propagation time	$C_L = 15pF$ (Note 2)		6	15	ns
t_{PHL}				16	38	ns

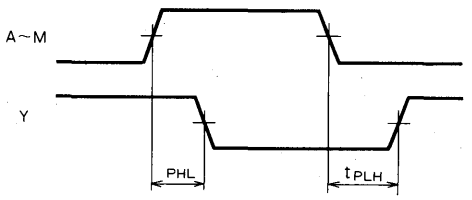
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



PRECAUTION FOR USE

Connect pins not being used to the V_{CC} supply voltage.

M74LS136P

QUADRUPLE 2-INPUT EXCLUSIVE OR GATES WITH OPEN COLLECTOR OUTPUTS

DESCRIPTION

The M74LS136P is a semiconductor integrated circuit containing 4 dual-input exclusive-OR gates with open collector output.

FEATURES

- Usable in wire-AND connection
- High breakdown output voltage ($V_O \geqq 7V$)
- Low power dissipation (P_d = 30.5mW typical)
- High speed (t_{pd} = 13ns typical)
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

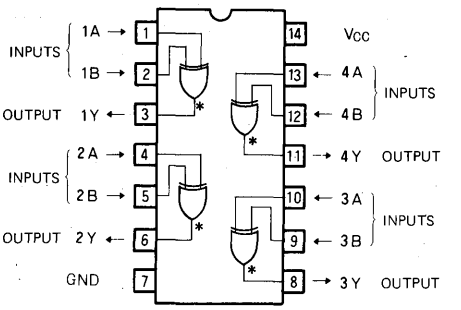
With the use of open collector output, the high-level output impedance can be freely selected by means of an external resistor. This make possible use in the wire-AND, which has been impossible with conventional gates.

When both inputs A and B are high or both low, output Y is low, and when A and B are high and low or low and high respectively, Y is high.

FUNCTION TABLE

A	B	Y
L	L	L
H	L	H
L	H	H
H	H	L

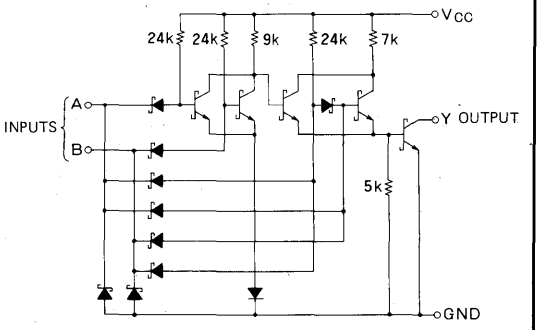
PIN CONFIGURATION (TOP VIEW)



* : OPEN COLLECTOR OUTPUT

Outline 14P4

CIRCUIT SCHEMATIC (EACH GATE)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, *unless otherwise noted*)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

QUADRUPLE 2-INPUT EXCLUSIVE OR GATES WITH OPEN COLLECTOR OUTPUTS

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_O = 5.5V$	0		100	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

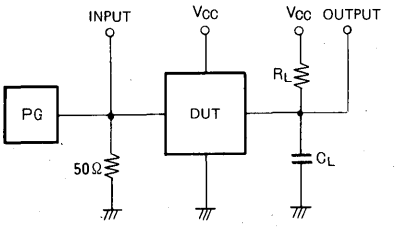
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$				−1.5	V
I_{OH}	High-level output current	$V_{CC} = 4.75V$, $V_I = 0.8V$ $V_I = 2V$, $V_O = 5.5V$				100	μA
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$	$I_{OL} = 4mA$		0.25	0.4	V
		$V_I = 0.8V$, $V_I = 2V$	$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				40	μA
		$V_{CC} = 5.25V$, $V_I = 10V$				0.2	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.8	mA
I_{CC}	Supply current	$V_{CC} = 5.25V$ (Note 1)			6.1	10	mA

* : All typical values are at $V_{CC} = 5V$, $Ta = 25°C$.
Note 1: I_{CC} is measured with all inputs grounded.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $Ta = 25°C$, unless otherwise noted)

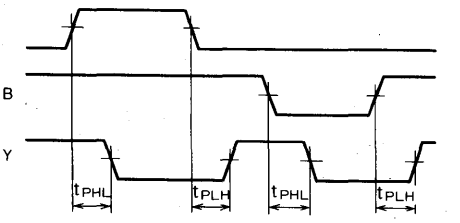
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time,	$R_L = 2 k\Omega$ $C_L = 15pF$ Other input low (Note 2)		14	30	ns
t_{PHL}				14	30	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time,	$R_L = 2 k\Omega$ $C_L = 15pF$ Other input high (Note 2)		12	30	ns
t_{PHL}				12	30	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS137P

3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

DESCRIPTION

The M74LS137P is a semiconductor integrated circuit containing a 3-line-to-8-line decoder/multiplexer function with address latch.

FEATURES

- Address latch capability with latch enable input
- Easy cascade connection with two enable inputs
- Wide operating temperature range (Ta: −20 − +75°C)

APPLICATIONS

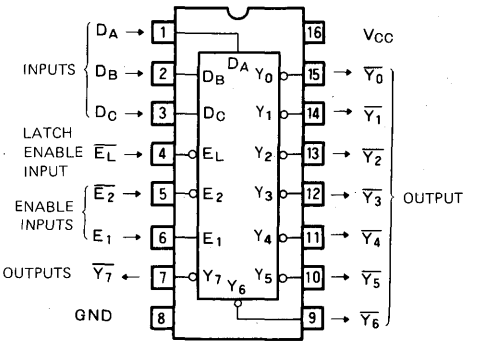
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTIONS

When latch enable input $\overline{E_L}$ is low, the data applied to inputs D_A−D_C are read into the latch; when it is high, the device operates as a decoder/demultiplexer with a function that retains the data

When the device is used as a decoder and inputs D_A−D_C are designated with a 3-bit binary code, one output among outputs $\overline{Y_0}$−$\overline{Y_7}$ corresponding to the numerical value is set low and the other seven outputs are all set high. In this case, enable input E_1 is set high and enable input $\overline{E_2}$ is set low. When E_1 and $\overline{E_2}$ are subject to any other conditions, the outputs are set high regardless of the status of D_A−D_C. (Refer to application examples)

PIN CONFIGURATION (TOP VIEW)

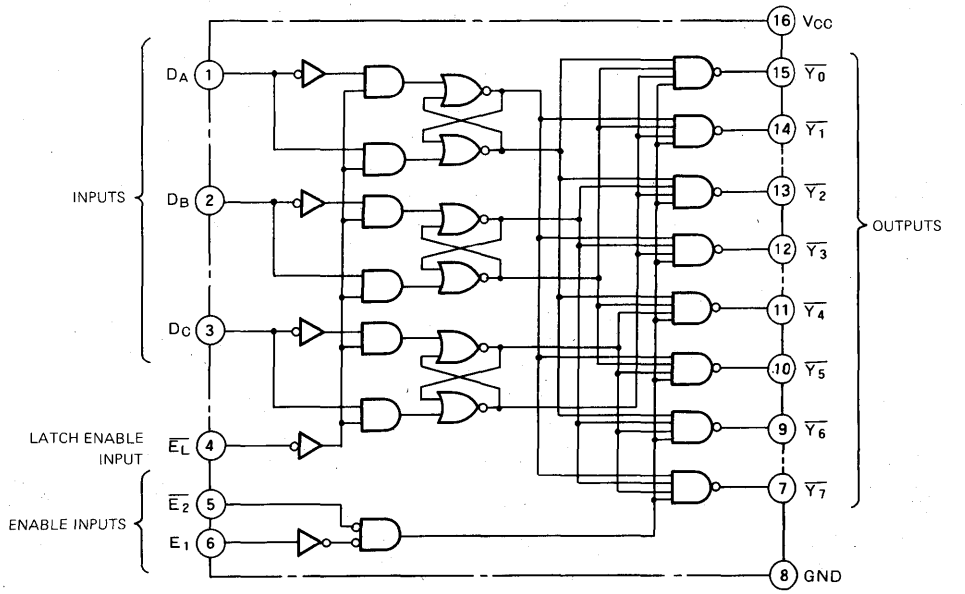


Outline 16P4

When the device is used as a demultiplexer, it functions as a 1-line-to-8-line demultiplexer by making E_1 and $\overline{E_2}$ the data inputs and D_A−D_C the selection inputs.

This IC is the same as the M74LS138P except that it features a latch function in inputs D_A−D_C.

BLOCK DIAGRAM



3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

FUNCTION TABLE

$\overline{E_L}$	E_1	$\overline{E_2}$	D_C	D_B	D_A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all other, H.							

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	°C
T_{stg}	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				-1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current		$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
			$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$\overline{E_L}$, E_1, $\overline{E_2}$	$V_{CC}=5.25V$, $V_I=0.4V$				-0.4	mA
		D_A, D_B, D_C					-0.2	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		-20		-100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 3)			11	18	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

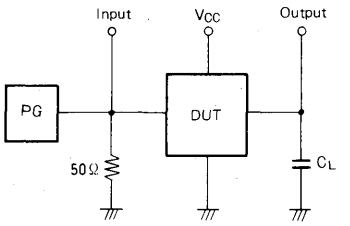
Note 3: Supply current should be measured with all inputs grounded.

3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Number of delay gate stages		Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{PLH}	Low-to-high, high-to-low output propagation time, from inputs D_A, D_B, D_C to outputs $\overline{Y_0} - \overline{Y_7}$		2	C_L=15pF (Note 4)		8	17	ns
t_{PHL}			4			15	38	
t_{PLH}	Low-to-high, high-to-low output propagation time, from inputs D_A, D_B, D_C to outputs $\overline{Y_0} - \overline{Y_7}$		3			10	24	ns
t_{PHL}			3			13	29	
t_{PLH}	Low-to-high, high-to-low output propagation time, from input $\overline{E_2}$ to outputs $\overline{Y_0} - \overline{Y_7}$		2			9	21	ns
t_{PHL}			2			10	27	
t_{PLH}	Low-to-high, high-to-low output propagation time, from input E_1 to outputs $\overline{Y_0} - \overline{Y_7}$		3			10	21	ns
t_{PHL}			3			12	27	
t_{PLH}	Low-to-high, high-to-low output propagation time, from input $\overline{E_L}$ to outputs $\overline{Y_0} - \overline{Y_7}$		3			13	27	ns
t_{PHL}			4			18	38	

Note 4: Measurement circuit

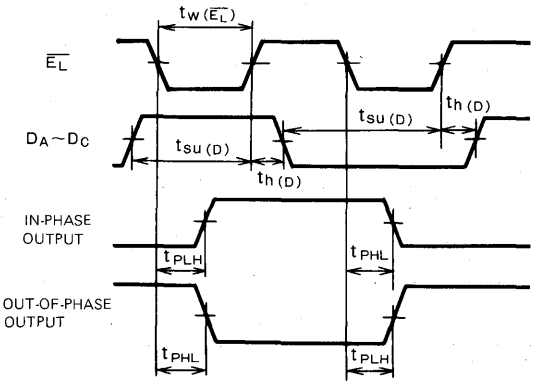


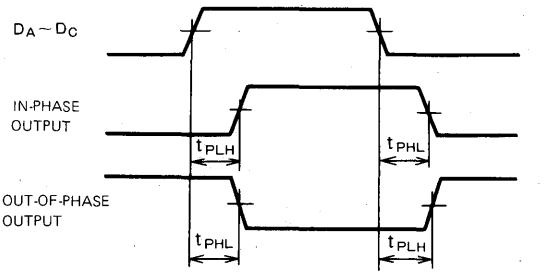
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_o = 50 ohms.
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{w(\overline{E_L})}$	Latch enable $\overline{E_L}$ pulse width		15	4		ns
$t_{su(D)}$	Setup time D_A – D_C to $\overline{E_L}$		10	3		ns
$t_{h(D)}$	Hold time D_A – D_C to $\overline{E_L}$		10	0		ns

TIMING DIAGRAMS (Reference level = 1.3V)

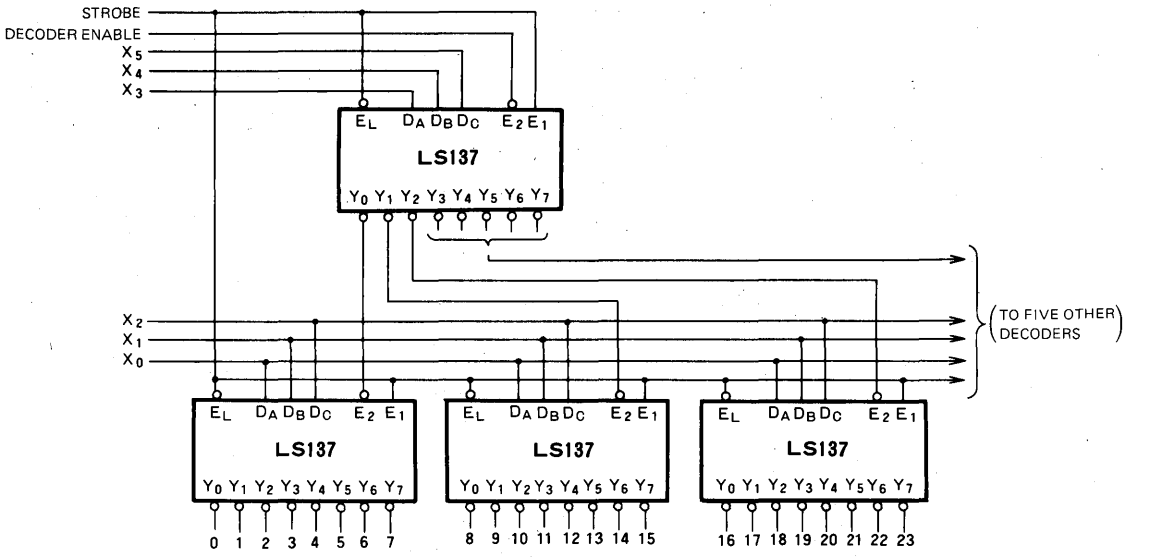




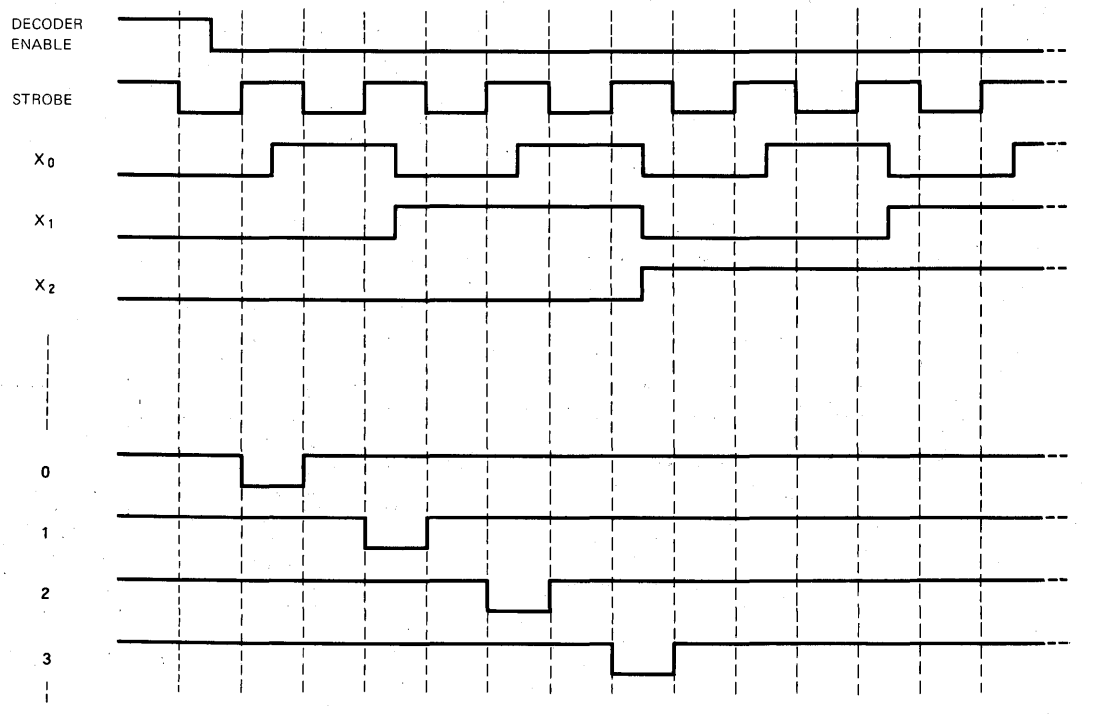
3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER WITH ADDRESS LATCH

APPLICATION EXAMPLES (6-bit 2-line-to-64-line decoder with address latch)

(a) CIRCUIT DIAGRAM



(b) FUNCTION WAVEFORM



MITSUBISHI ELECTRIC

M74LS138P

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

DESCRIPTION

The M74LS138P is a semiconductor integrated circuit consisting of a 3-bit binary-octal decoder/demultiplexer with enable inputs.

FEATURES

- 3 classes of enable inputs
- 4 to 16 decorder/demultiplexer functions are provided without use of external components.
- Wide operating temperature range (T_a = -20 ~ +75°C)

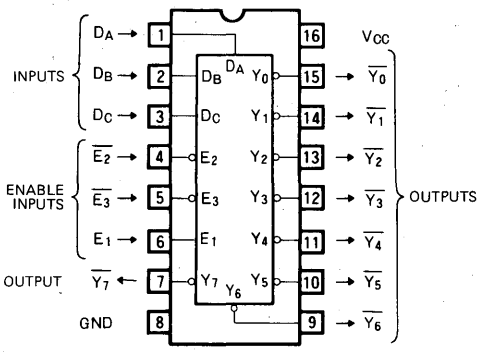
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

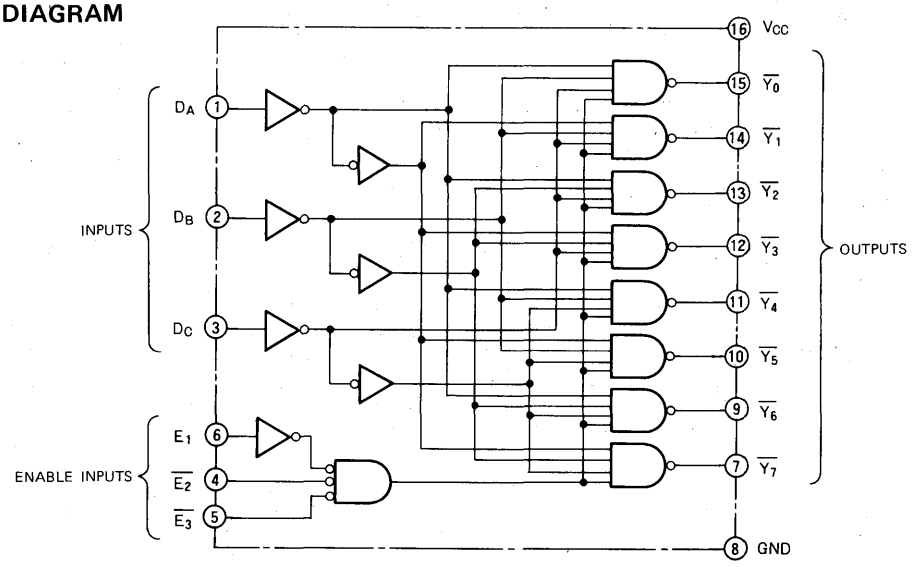
For use as a decoder, specify inputs D_A, D_B, and D_C in 3-bit binary code. In the case of decoding function, the E_1 is kept in high state while $\overline{E_2}$ and $\overline{E_3}$ are kept low. If E_1, $\overline{E_2}$ and $\overline{E_3}$ are not in these conditions, all the outputs become high, irrespective of the status of D_A~D_C. For use as a demultiplexer, $\overline{E_1}$, $\overline{E_2}$ and E_3 are used as data inputs and D_A, D_B, and D_C as selection inputs. This forms a 1-line to 8-line demultiplexer.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

FUNCTION TABLE (Note 1)

E_1	$\overline{E_X}$	D_C	D_B	D_A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Note 1: $\overline{E_X}=\overline{E_2}+\overline{E_3}$
X : irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a=-20\sim+75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5\sim+7$	V
V_I	Input voltage		$-0.5\sim+15$	V
V_O	Output voltage	High-level state	$-0.5\sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20\sim+75$	℃
T_{stg}	Storage temperature range		$-65\sim+150$	℃

RECOMMENDED OPERATING CONDITIONS ($T_a=-20\sim+75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH}\geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL}\leqq 0.4V$	0		4	mA
		$V_{OL}\leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a=-20\sim+75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				-0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$		-20		-100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 3)			6.3	10	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

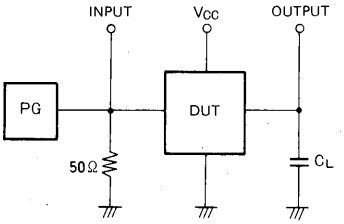
Note 3: I_{CC} is measured with all output off-state.

3-LINE TO 8-LINE DECODER/DEMULTIPLEXER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

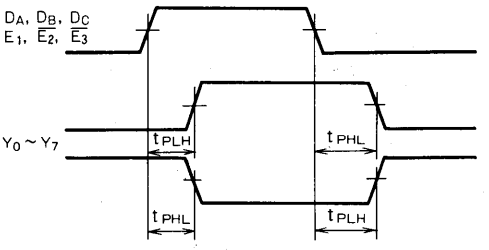
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B, D_C to output $\overline{Y_0}$–$\overline{Y_7}$	delay gate stages 2	C_L = 15pF (Note 4)		9	20	ns
t_{PHL}					12	41	ns
t_{PLH}		delay gate stages 3			16	27	ns
t_{PHL}					14	39	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $\overline{E_2}$, $\overline{E_3}$ to outputs $\overline{Y_0}$–$\overline{Y_7}$	delay gate stages 2			10	18	ns
t_{PHL}					15	32	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E_1 to outputs $\overline{Y_0}$–$\overline{Y_7}$	delay gate stages 3			8	26	ns
t_{PHL}					15	38	ns

Note 4: Measurement circuit



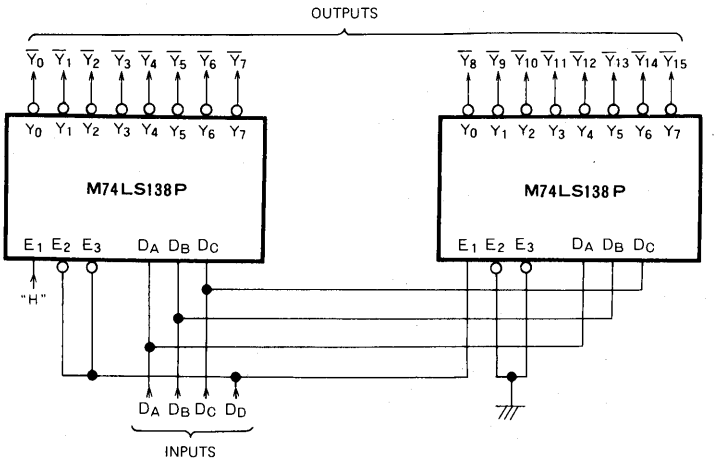
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

4-line to 16-line decorder/demultiplexer



M74LS139P

DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

DESCRIPTION

The M74LS139P is a semiconductor integrated circuit containing two 2-bit 2-line-to-4-line decoders/demultiplexers with separate enable inputs.

FEATURES

- Enable inputs provided
- Two circuits completely separate
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

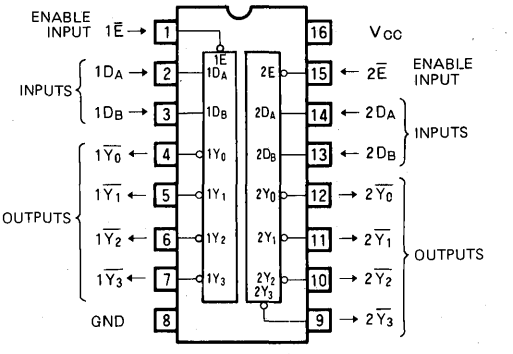
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

For use as a decoder, when inputs D_A and D_B are specified in 2-bit binary code, the output corresponding to the number among $\overline{Y_0}$~$\overline{Y_3}$ is set low and all the other 3 outputs are set high. The enable inputs $\overline{E}$ are kept low. When inputs $\overline{E}$ are high, all the outputs are set high irrespective of the status of D_A and D_B.

For use as a 1-line-4-line demultiplexer, make inputs $\overline{E}$ the data inputs and D_A and D_B the selection inputs.

PIN CONFIGURATION (TOP VIEW)



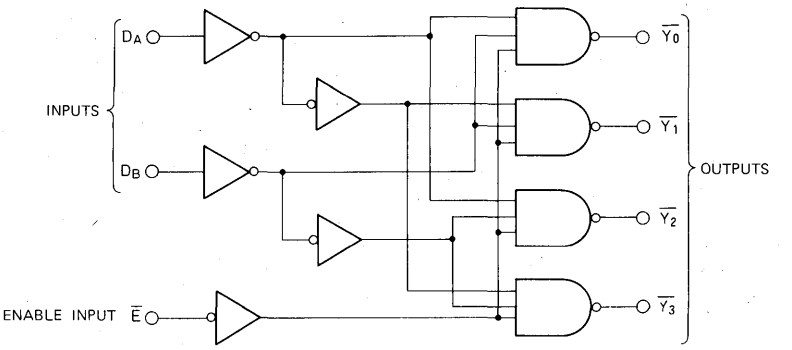
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{E}$	D_B	D_A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Note 1: X : Irrelevant

BLOCK DIAGRAM (EACH DECODER)



DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise ntoed)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

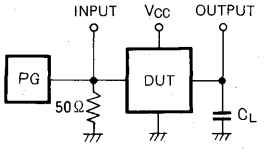
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$, $V_I = 0.8V$, $V_I = 2V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$, $V_I = 0.8V$, $V_I = 2V$	$I_{OL} = 4mA$		0.25	0.4	V
			$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC} = 5.25V$, $V_O = 0V$		−20		−100	mA
I_{CC}	Supply current	$V_{CC} = 5.25V$ (Note 3)			6.8	11	mA

* : All typical values are at $V_{CC} = 5V$, $T_a = 25°C$.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with the outputs in the enable state.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25°C$, unless otherwise noted)

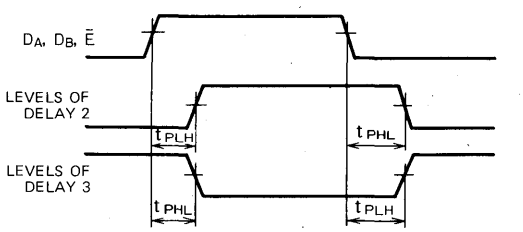
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B to outputs $\overline{Y_0}$–$\overline{Y_7}$	dealy gate stages 2	$C_L = 15pF$ (Note 4)		8	20	ns
t_{PHL}					15	33	ns
t_{PLH}		delay gate stages 3			10	29	ns
t_{PHL}					15	38	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E}$ to outputs $\overline{Y_0}$–$\overline{Y_7}$				8	24	ns
t_{PHL}					12	32	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, $t_r = 6ns$, $t_f = 6ns$, $t_w = 500ns$, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



M74LS145P

BCD-TO-DECIMAL DECODER/DRIVER

DESCRIPTION

The M74LS145P is a semiconductor integrated circuit provided with BCD-to-decimal decoder/driver function and open collector outputs.

FEATURES

- High output current (I_O=80mA with $V_{OL} \leqq 3V$; I_O = 24mA with $V_O \leqq 0.5V$)
- High output breakdown voltage ($V_O \geqq 15V$)
- All outputs high with reactive input
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

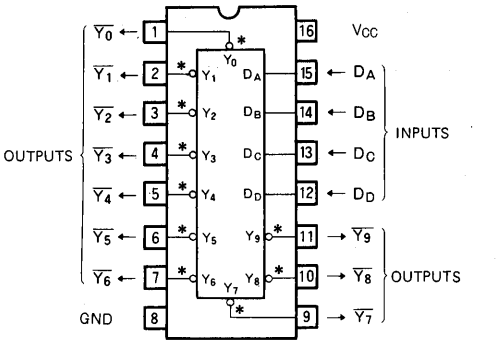
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When inputs D_A, D_B, D_C and D_D are designated with a BCD code in this decoder/driver, the $\overline{Y_0} \sim \overline{Y_9}$ output corresponding to the number is set low while the other 9 outputs are set high. When a binary number of 10 or more is applied to $D_A \sim D_D$., all the outputs are set high.

The outputs are open collector types with a breakdown voltage of 15V and an I_{OL} of 80mA (with $V_{OL} \leqq 3V$) This device is therefore suitable for use as an LSTTL/MOS interface, display tube and relay driver.

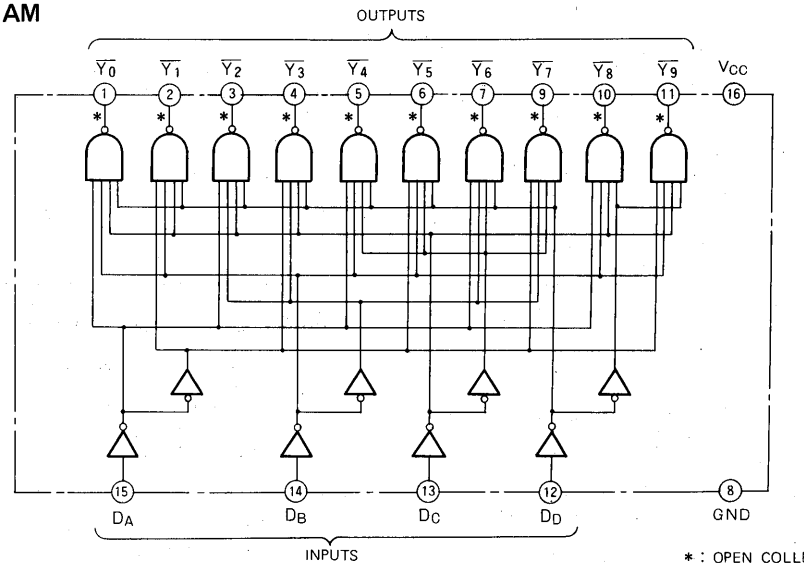
PIN CONFIGURATION (TOP VIEW)



* : OPEN COLLECTOR OUTPUTS

Outline 16P4

BLOCK DIAGRAM



* : OPEN COLLECTOR OUTPUTS

MITSUBISHI ELECTRIC

BCD-TO-DECIMAL DECODER/DRIVER

FUNCTION TABLE

Decimal number	D_D	D_C	D_B	D_A	$\overline{Y_0}$	$\overline{Y_1}$	$\overline{Y_2}$	$\overline{Y_3}$	$\overline{Y_4}$	$\overline{Y_5}$	$\overline{Y_6}$	$\overline{Y_7}$	$\overline{Y_8}$	$\overline{Y_9}$
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	H	L	H	L	H	H	H	H	H	H	H	H	H	H
11	H	L	H	H	H	H	H	H	H	H	H	H	H	H
12	H	H	L	L	H	H	H	H	H	H	H	H	H	H
13	H	H	L	H	H	H	H	H	H	H	H	H	H	H
14	H	H	H	L	H	H	H	H	H	H	H	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	H	H	H

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim +15$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	°C
T_{stg}	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH}=15V$	0		250	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
I_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $V_O=15V$				250	μA
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=12mA$		0.25	0.4	V
			$I_{OL}=24mA$		0.35	0.5	V
			$I_{OL}=80mA$		2.3	3	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 1)			7	13	mA

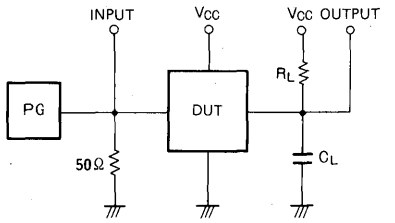
* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.

Note 1: I_{CC} is measured with $D_A \sim D_D$ at 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

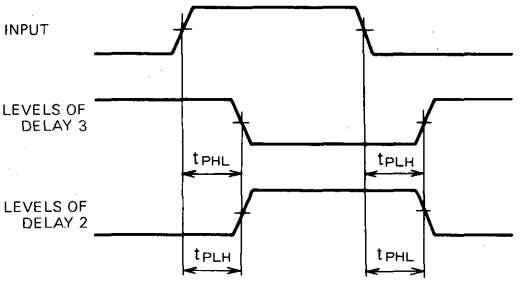
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time	delay gate stages 2	R_L=665Ω, C_L=45pF (Note 2)		27	50	ns
t_{PHL}					17	50	ns
t_{PLH}		delay gate stages 3			27	50	ns
t_{PHL}					17	50	ns

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Z_O=50Ω.
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference=1.3V)



M74LS147P

10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

DESCRIPTION

The M74LS147P is a semiconductor integrated circuit containing a 10-line BCD encoder with a priority function.

FEATURES

- Priority decoding of the data inputs
- Data inputs and outputs both active-low
- Wide operating temperature range (T_a = -20 ~ +75°C)

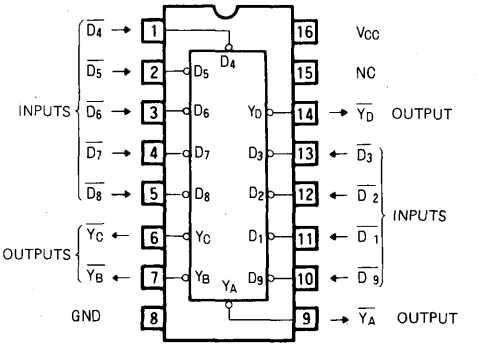
APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

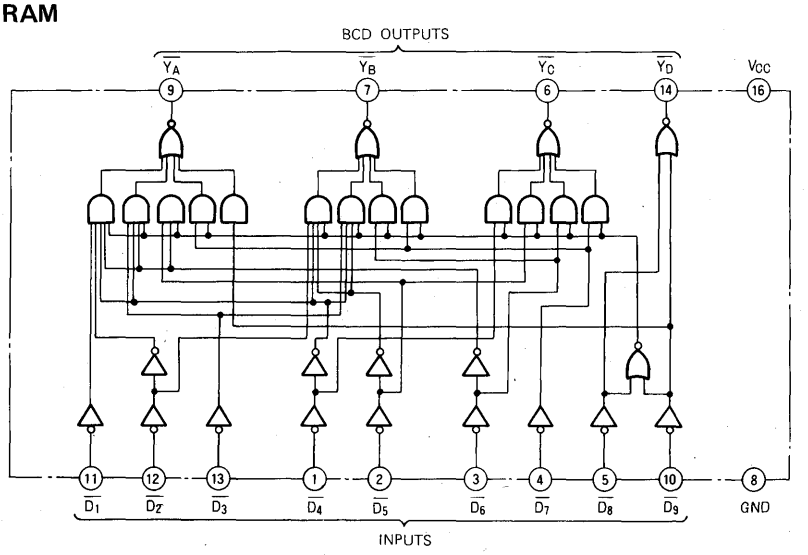
This device functions to encode a pulse entered through one of the nine input pins ($\overline{D_1}$ ~ $\overline{D_9}$) into a BCD code by producing an inverted signal (based on input) at output $\overline{Y_A}$ ~ $\overline{Y_D}$. The encoder handles all inputs in a priority sequence, so that when two or more are present at input at the same time, the signal present at the highest priority pin will be encoded. $\overline{D_0}$ does not exist as an input, and when all inputs are at high-level, all outputs will also be high-level, yielding a 0 output. Ideally suited for use as a keyboard encoder or range selector.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4 NC: NO CONNECTION

BLOCK DIAGRAM



10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

FUNCTION TABLE (Note 1)

$\overline{D_1}$	$\overline{D_2}$	$\overline{D_3}$	$\overline{D_4}$	$\overline{D_5}$	$\overline{D_6}$	$\overline{D_7}$	$\overline{D_8}$	$\overline{D_9}$	$\overline{Y_D}$	$\overline{Y_C}$	$\overline{Y_B}$	$\overline{Y_A}$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

Note 1. X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level output	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75V	I_{OL} = 4mA		0.25	0.4	V
		V_I = 0.8V, V_I = 2V	I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC1}	Supply current	V_{CC} = 5.25V (Note 3)			12	20	mA
I_{CC2}	Supply current	V_{CC} = 5.25V (Note 4)			10	17	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

3. I_{CC1} is measured with $\overline{D_7}$ at 0V, and all other inputs open.

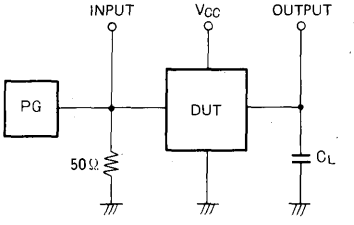
4. I_{CC2} is measured with all inputs open.

10-LINE DECIMAL TO 4-LINE BCD PRIORITY ENCODER

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

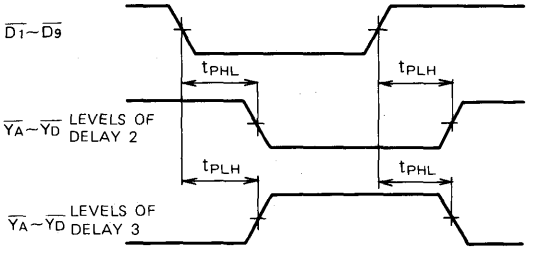
Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{D_1} \sim \overline{D_9}$ to output $\overline{Y_A} \sim \overline{Y_D}$ (levels of delay 2)	C_L=15pF (Note 5)		9	18	ns
t_{PHL}				14	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{D_1} \sim \overline{D_9}$ to output $\overline{Y_A} \sim \overline{Y_D}$ (levels of delay 3)			25	33	ns
t_{PHL}				15	23	ns

Note 5. Measurement Circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS148P

8-LINE TO 3-LINE PRIORITY ENCODER

DESCRIPTION

The M74LS148P is a semiconductor integrated circuit provided with an 8-line to 3-line priority encoder function and priority sequence function.

FEATURES

- Priority decoding of the data input
- Easy expansion of the number of input bit
- Wide operating temperature range (T_a=−20~+75°C)

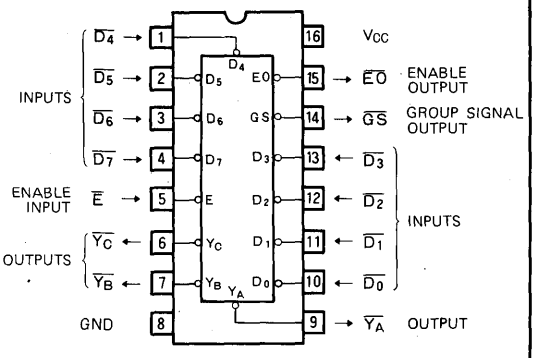
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

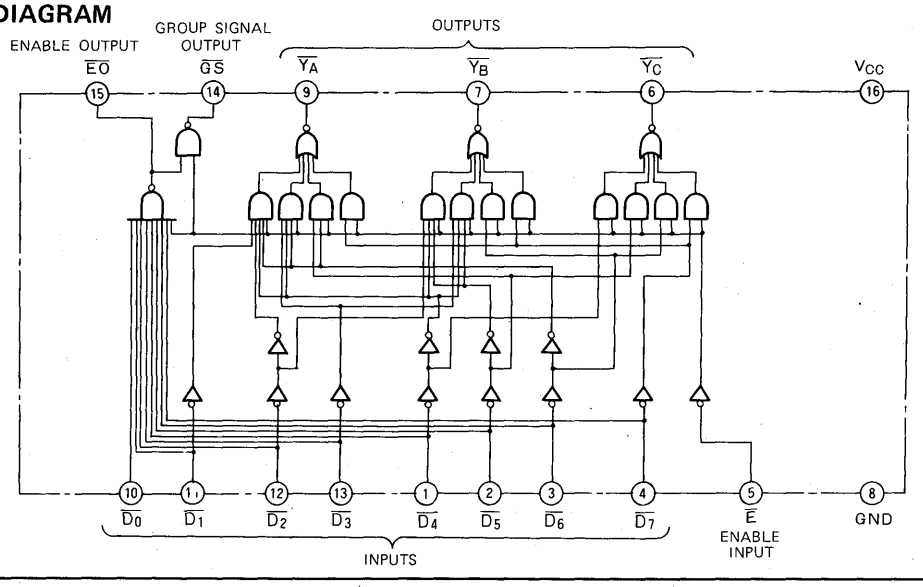
When signals are applied to one of this encoder's eight inputs $\overline{D_0}$~$\overline{D_7}$, the 3-bit binary number corresponding to the input pin appears at outputs $\overline{Y_A}$~$\overline{Y_C}$. Since priority is given to each input, the highest-level input pin signal is encoded when more than one signals are applied simultaneously. The number of input data can easily be increased as shown in the application example using the enable input $\overline{E}$, enable output $\overline{EO}$ and group signal output $\overline{GS}$. This device is suitable for use as a keyboard encoder or for range selection.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

8-LINE TO 3-LINE PRIORITY ENCODER

FUNCTION TABLE (Note 1)

$\overline{E}$	$\overline{D_0}$	$\overline{D_1}$	$\overline{D_2}$	$\overline{D_3}$	$\overline{D_4}$	$\overline{D_5}$	$\overline{D_6}$	$\overline{D_7}$	$\overline{Y_C}$	$\overline{Y_B}$	$\overline{Y_A}$	$\overline{GS}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

Note 1 X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20 \sim +75$	°C
Tstg	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				-1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	I_{OL} 4mA		0.25	0.4	V
			$V_I=0.8V$, $V_I=2V$	I_{OL} 8mA		0.35	0.5	V
I_{IH}	High-level input current	$\overline{D_0}$, $\overline{E}$	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{D_1} \sim \overline{D_7}$					40	
		$\overline{D_0}$, $\overline{E}$	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{D_1} \sim \overline{D_7}$					0.2	
I_{IL}	Low-level input current	$\overline{D_0}$, $\overline{E}$	$V_{CC}=5.25V$, $V_I=0.4V$				-0.4	mA
		$\overline{D_1} \sim \overline{D_7}$					-0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		-20		-100	mA
I_{CC1}	Supply current		$V_{CC}=5.25V$ (Note 3)			12	20	mA
I_{CC2}	Supply current		$V_{CC}=5.25V$ (Note 4)			10	17	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC1} is measured with $\overline{D_7}$ and $\overline{E}$ at 0V and with all other inputs open.

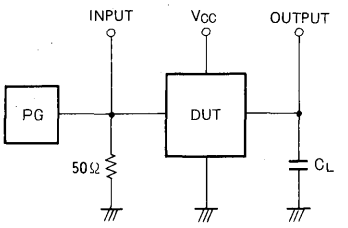
Note 4: I_{CC2} is measured with all inputs open.

8-LINE TO 3-LINE PRIORITY ENCODER

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

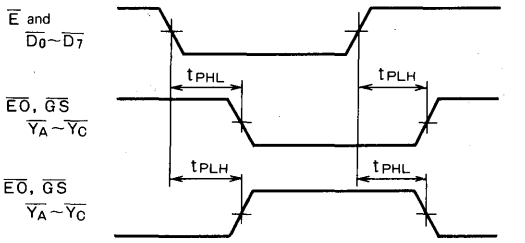
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $\overline{D_1}$~$\overline{D_7}$ to outputs $\overline{Y_A}$~$\overline{Y_C}$ (levels of delay 2)	C_L=15pF (Note 5)		11	18	ns
t_{PHL}				14	25	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $\overline{D_1}$~$\overline{D_7}$ to outputs $\overline{Y_A}$~$\overline{Y_C}$ (levels of delay 3)			15	36	ns
t_{PHL}				18	29	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $\overline{D_0}$~$\overline{D_7}$ to output $\overline{EO}$ (levels of delay 3)			7	18	ns
t_{PHL}				24	40	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $\overline{D_0}$~$\overline{D_7}$ to output $\overline{GS}$ (levels of delay 2)			31	55	ns
t_{PHL}				8	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E}$ to outputs $\overline{Y_A}$~$\overline{Y_C}$ (levels of delay 2)			11	25	ns
t_{PHL}				14	25	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E}$ to output $\overline{GS}$ (levels of delay 2)			8	17	ns
t_{PHL}				13	36	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E}$ to output $\overline{EO}$ (levels of delay 2)			11	21	ns
t_{PHL}				27	35	ns

Note 5: Measurement circuit



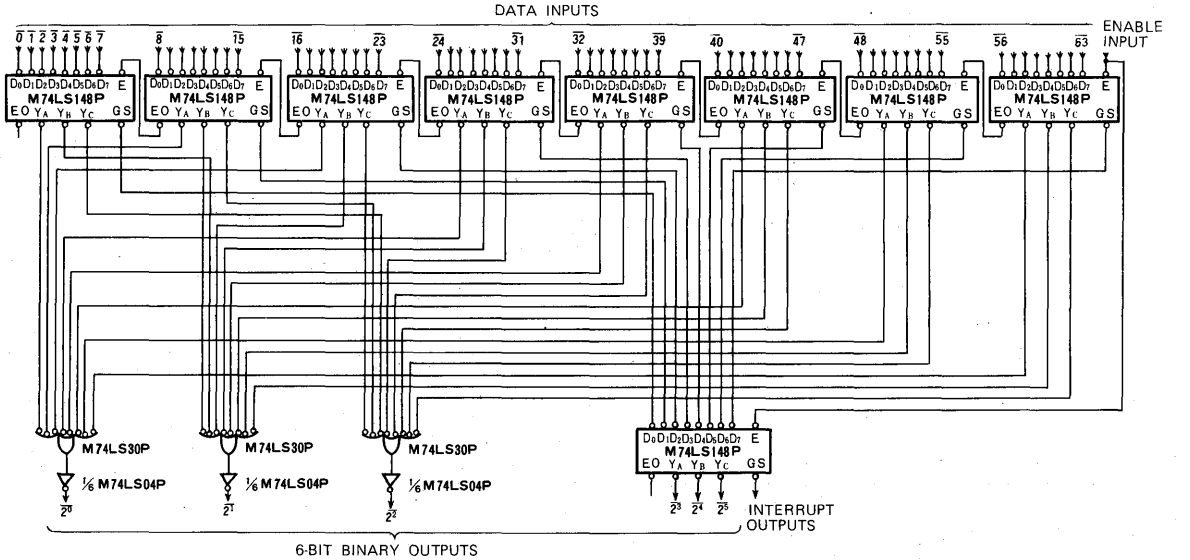
(1) The pulse generator (PG) has the following characteristics:
PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Z_O=50Ω.
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

64-line/4-bit binary encoder



Expansion is possible up to 2^n bits in accordance with the above application example.

M74LS151P

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

DESCRIPTION

The M74LS151P is a semiconductor integrated circuit containing an 8-line to 1-line data selector/multiplexer function.

FEATURES

- Strobe input provided
- Complementary output provided
- Low output impedance
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

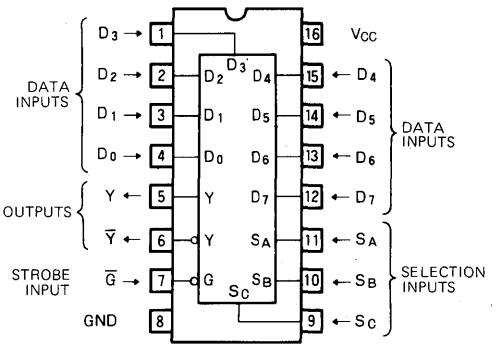
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has a data selector function which provides 1-line selection of 8 input signals and a multiplexer function which converts the 8-bit parallel data into serial data. When 8-line signals are applied to the data inputs and 1 data is specified from among the 8 data from selection inputs S_A, S_B and S_C, the input signal is output at Y and the inverted signal from output $\overline{Y}$. By applying 8-bit parallel data to D_0~D_7 and connecting a synchronous octal counter output to S_A, S_B and S_C, the data appear in Y in D_0~D_7 order and in $\overline{Y}$ in $\overline{D_0}$~$\overline{D_7}$ order as synchronized with the clock pulse. When strobe input $\overline{G}$ is set high, Y is set low and $\overline{Y}$ high.

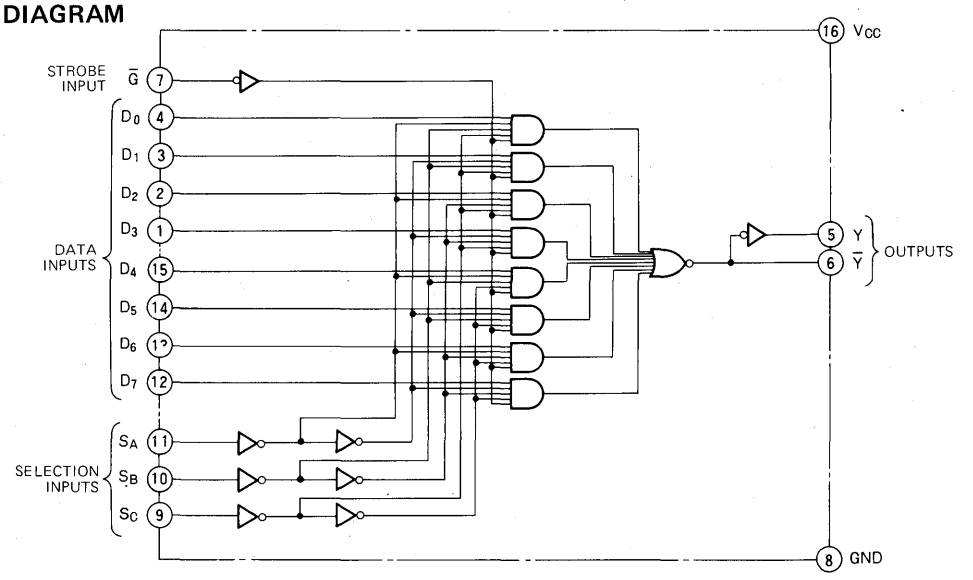
M74LS151P has the same functions and pin connections as M74LS251P but the latter is provided with 3-state outputs.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

FUNCTION TABLE (Note 1)

S_C	S_B	S_A	$\overline{G}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	$\overline{Y}$
X	X	X	H	X	X	X	X	X	X	X	X	L	H
L	L	L	L	L	X	X	X	X	X	X	X	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L
L	L	H	L	X	L	X	X	X	X	X	X	L	H
L	L	H	L	X	H	X	X	X	X	X	X	H	L
L	H	L	L	X	X	L	X	X	X	X	X	L	H
L	H	L	L	X	X	H	X	X	X	X	X	H	L
L	H	H	L	X	X	X	L	X	X	X	X	L	H
L	H	H	L	X	X	X	H	X	X	X	X	H	L
H	L	L	L	X	X	X	X	L	X	X	X	L	H
H	L	L	L	X	X	X	X	H	X	X	X	H	L
H	L	H	L	X	X	X	X	X	L	X	X	L	H
H	L	H	L	X	X	X	X	X	H	X	X	H	L
H	H	L	L	X	X	X	X	X	X	L	X	L	H
H	H	L	L	X	X	X	X	X	X	H	X	H	L
H	H	H	L	X	X	X	X	X	X	X	L	L	H
H	H	H	L	X	X	X	X	X	X	X	H	H	L

Note 1 X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	°C
T_{stg}	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

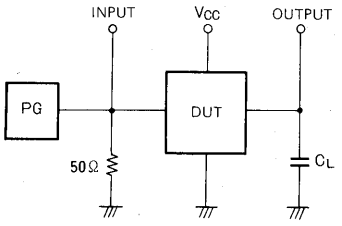
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$			−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$	2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OL}=4mA$		0.25	0.4	V
		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$			20	μA
		$V_{CC}=5.25V$, $V_I=10V$			0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$			−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$	−20		−100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 3)		6	10	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.
Note 2: All measurements should be done quickly.
Note 3: I_{CC} is measured with all inputs at 4.5V

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs S_A, S_B, S_C to output $\overline{Y}$	$C_L=15pF$ (Note 4)		10	23	ns
t_{PHL}				15	32	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs S_A, S_B, S_C to output Y			22	43	ns
t_{PHL}				16	30	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{G}$ to output $\overline{Y}$			10	24	ns
t_{PHL}				14	30	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{G}$ to output Y			21	42	ns
t_{PHL}				16	32	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $D_0 \sim D_7$ to output $\overline{Y}$			7	21	ns
t_{PHL}				8	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $D_0 \sim D_7$ to output Y			17	32	ns
t_{PHL}				12	26	ns

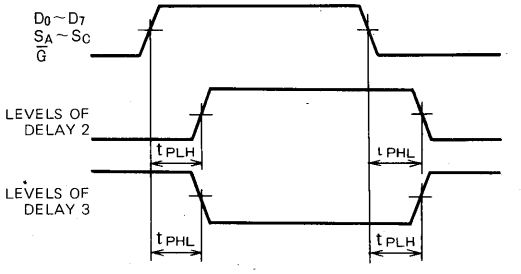
Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference=1.3V)



M74LS153P

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

DESCRIPTION

The M74LS153P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits.

FEATURES

- Strobe inputs provided independently for each circuit
- Selection inputs common to both circuits
- Low output impedance
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

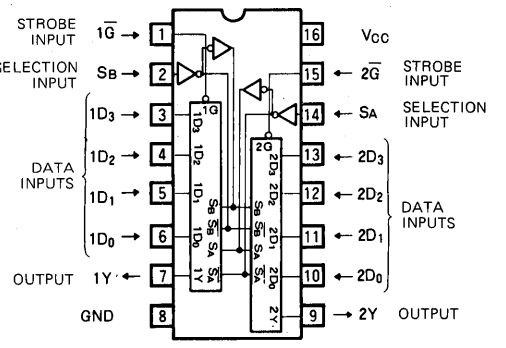
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has two data selector circuits which provide 2-line to 1-line selection of 4 pairs of input signal using two multiplexer circuits which convert the 4-bit parallel data into serial data with time-sharing. When 4-line signals are applied to the data inputs D_0, D_1, D_2 and D_3 and 1 data is specified from among the data by selection inputs S_A and S_B, the input signal is output at Y. By applying 4-bit parallel data to D_0, D_1, D_2 and D_3, and connecting a synchronous divide-by-4 counter output to S_A and S_B, the D_0, D_1, D_2 and D_3 data appear in the order of D_0, D_1, D_2 and D_3 synchronized with the clock pulse. S_A and S_B are common to both circuits while strobe inputs $1\overline{G}$ and $2\overline{G}$ are independent. When $1\overline{G}$ and $2\overline{G}$ are set high, 1Y and 2Y are set low irrespective of the status of the input.

M74LS153P has the same functions and pin connections as M74LS253P but the latter is provided with 3-state outputs.

PIN CONFIGURATION (TOP VIEW)



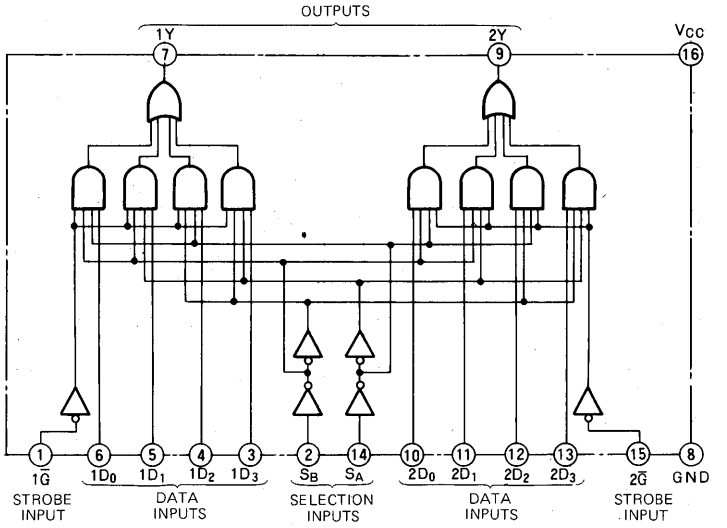
Outline 16P4

FUNCTION TABLE (Note 1)

S_B	S_A	D_0	D_1	D_2	D_3	$\overline{G}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Note 1 X : Irrelevant

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

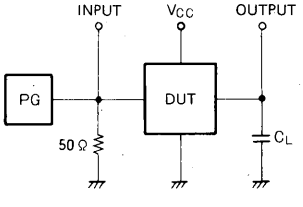
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75V	I_{OL} = 4 mA		0.25	0.4	V
		V_I = 0.8V, V_I = 2V	I_{OL} = 8 mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC}	Supply current	V_{CC} = 5.25V (Note 3)			6.2	10	mA

* : All typical values are at V_{CC}=5V, T_a=25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25℃, unless otherwise noted)

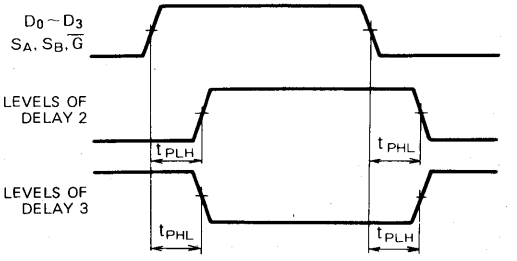
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_0 ~ D_3 to output Y	C_L = 15pF (Note 4)		8	15	ns
t_{PHL}				12	26	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs S_A, S_B to output Y			12	29	ns
t_{PHL}				13	38	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{G}$ to output Y			12	24	ns
t_{PHL}				12	32	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS155P

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH STROBE

DESCRIPTION

The M74LS155P is a semiconductor integrated circuit containing two 2-bit binary to 4-line decoders/demultiplexers.

FEATURES

- Low output impedance
- Enable inputs provided
- 8-bit output decoder/demultiplexer functions are provided without the use of external components
- Wide operating temperature range (T_a=−20~+75°C)

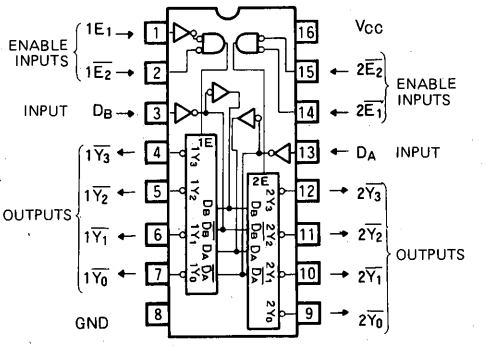
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When a 2-bit binary number is decoded in quaternary numbers and the 2-bit binary number is applied to inputs D_A and D_B, the corresponding $\overline{Y_0}$~$\overline{Y_3}$ output is set low and all the other 3 outputs are set high. In this case, enable inputs $1E_1$ and $2\overline{E_1}$ are kept high and low, respectively, and enable inputs $1\overline{E_2}$ and $2\overline{E_2}$ are kept low. When $1\overline{E_2}$ and $2\overline{E_2}$ are set high, all the outputs are set high. When decoding a 3-bit binary number in octal numbers, $1E_1$ and $2\overline{E_2}$ are connected and by applying the third bit binary number, the outputs appear in $2\overline{Y_0}$~$2\overline{Y_3}$ and $1\overline{Y_0}$~$1\overline{Y_3}$, in accordance with the function table.

PIN CONFIGURATION (TOP VIEW)

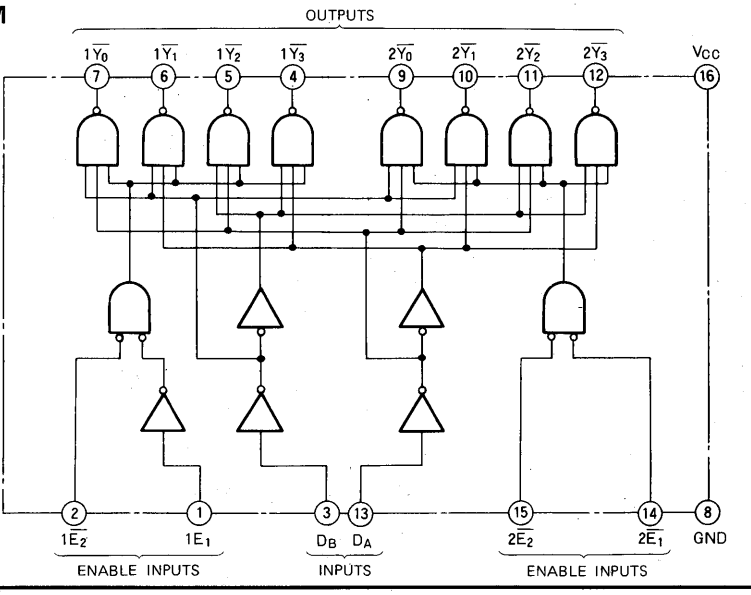


Outline 16P4

For use as a 1-line to 4-line demultiplexer, the outputs appear in $\overline{Y_0}$~$\overline{Y_3}$ by making $1E_1$ and $2\overline{E_1}$ the data inputs and D_A and D_B the selection inputs. For use as a 1-line to 8-line demultiplexer, $1E_1$ and $2\overline{E_1}$ are connected to make them the third bit selection input and $1\overline{E_2}$ and $2\overline{E_2}$ are connected to make the data inputs so that the outputs appear in $2\overline{Y_0}$~$2\overline{Y_3}$ and $1\overline{Y_0}$~$1\overline{Y_3}$.

M74LS155P has the same functions and pin connections as M74LS255P but the latter is provided with open collector outputs.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH STROBE

FUNCTION TABLE (Note 1)

(2-bit binary to 4-line decoder/1 line to 4-line demultiplexer)

D_B	D_A	$1\overline{E_2}$	$1E_1$	$1\overline{Y_0}$	$1\overline{Y_1}$	$1\overline{Y_2}$	$1\overline{Y_3}$
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

D_B	D_A	$2\overline{E_2}$	$2\overline{E_1}$	$2\overline{Y_0}$	$2\overline{Y_1}$	$2\overline{Y_2}$	$2\overline{Y_3}$
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

(3-bit binary to 8-line decoder/1 line to 8-line demultiplexer)

D_C	D_B	D_A	$\overline{E}$	$2\overline{Y_0}$	$2\overline{Y_1}$	$2\overline{Y_2}$	$2\overline{Y_3}$	$1\overline{Y_0}$	$1\overline{Y_1}$	$1\overline{Y_2}$	$1\overline{Y_3}$
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Note 1 X : Irrelevant
D_C : Pin connecting $1E_1$ and $2\overline{E_1}$
$\overline{E}$: Pin connecting $1\overline{E_2}$ and $2\overline{E_2}$

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75V	I_{OL} = 4mA		0.25	0.4	V
		V_I = 0.8V, V_I = 2V	I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.25V V_I = 2.7V				20	μA
		V_{CC} = 5.25V V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC}	Supply current	V_{CC} = 5.25V (Note 3)			6.1	10	mA

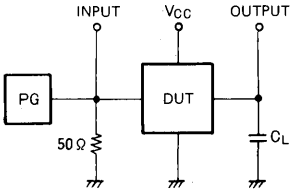
* : All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time
Note 3: I_{CC} is measured with inputs $1\overline{E_2}$, $2\overline{E_1}$ and $2\overline{E_2}$ at 0V and with D_A, D_B and $1E_1$ at 4.5V

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH STROBE

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

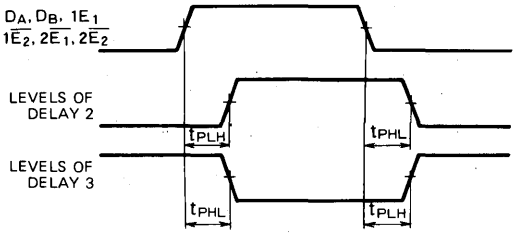
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B to outputs $\overline{Y_0}$~$\overline{Y_3}$	delay gate stages 2	C_L=15pF (Note 4)		8	15	ns
t_{PHL}					15	30	ns
t_{PLH}		delay gate stages 3			10	26	ns
t_{PHL}					15	30	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $1\overline{E_2}$, $2\overline{E_1}$, $2\overline{E_2}$ to outputs $\overline{Y_0}$~$\overline{Y_3}$				8	15	ns
t_{PHL}					11	30	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $1E_1$ to outputs $1\overline{Y_0}$~$1\overline{Y_3}$				17	27	ns
t_{PHL}					15	27	ns

Note 4: Measurement circuit



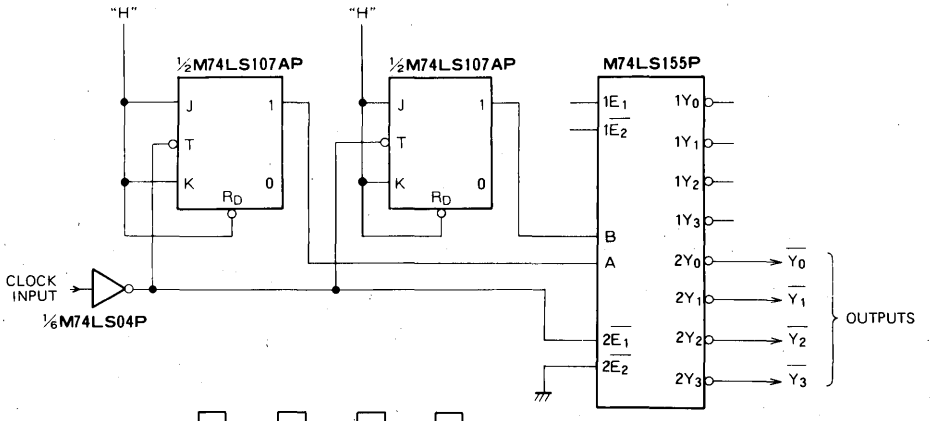
(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_{P-P}=3V, Z_O=50Ω.
(2) C_L includes probe and jig capacitance

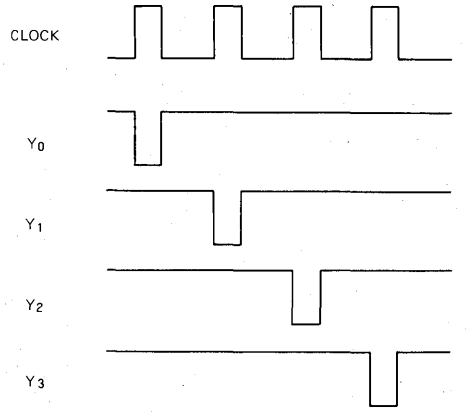
TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

4-phase clock pulse generator





M74LS156P

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS156P is a semiconductor integrated circuit containing two 2-bit binary to 4-line decoders/demultiplexers with open collector outputs

FEATURES

- Usable in AND Tie connection
- Enable inputs provided
- 8-bit output decoder/demultiplexer function is provided without the use of external components
- Wide operating temperature range (T_a=−20~+75°C)

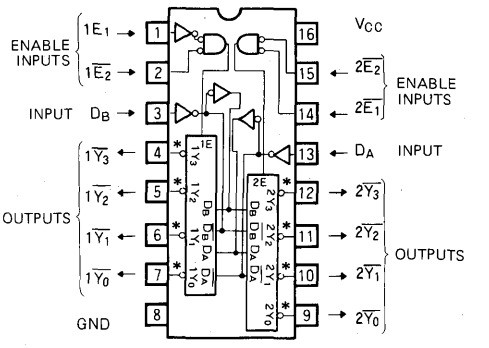
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When a 2-bit binary number is decoded as a quaternary number and the 2-bit binary number is applied to inputs D_A and D_B, the corresponding $\overline{Y_0}$~$\overline{Y_3}$ output is set low and all the other 3 outputs are set high. In this case, enable inputs $1E_1$ and $2\overline{E_1}$ are kept high and low, respectively, and enable inputs $1\overline{E_2}$ and $2\overline{E_2}$ are kept low. When $1\overline{E_2}$ and $2\overline{E_2}$ are set high, all the outputs are set high. When decoding a 3-bit binary number in octal numbers, $1E_1$ and $2\overline{E_2}$ are connected and by applying the third bit binary number to them, the outputs appear in $2\overline{Y_0}$~$2\overline{Y_3}$ and $1\overline{Y_0}$~$1\overline{Y_3}$, in accordance with the function table.

PIN CONFIGURATION (TOP VIEW)



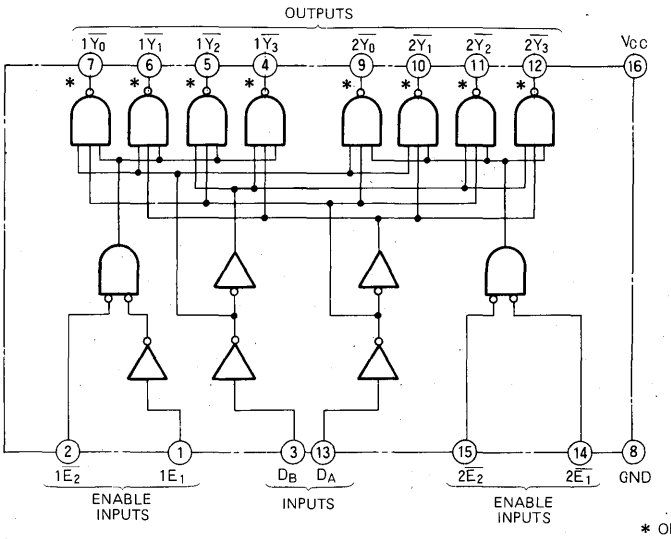
* OPEN COLLECTOR OUTPUT

Outline 16P4

For use as a 1-line to 4-line demultiplexer, the outputs appear in $\overline{Y_0}$~$\overline{Y_3}$ by making $1E_1$ and $2\overline{E_1}$ the data inputs and D_A and D_B the selection inputs. For use as a 1-line to 8-line demultiplexer, $1E_1$ and $1\overline{E_1}$ are connected to to be made the third bit selection input and $1\overline{E_2}$ and $2\overline{E_2}$ are connected to be made the data inputs so that the outputs appear in $2\overline{Y_0}$~$2\overline{Y_3}$ and $1\overline{Y_0}$~$1\overline{Y_3}$.

M74LS156P has the same functions and pin connections as M74LS155P but the latter is provided with active pull-up resistor outputs.

BLOCK DIAGRAM



* OPEN COLLECTOR OUTPUT

M74LS156P

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

(2-bit binary to 4-line decoder/1 line to 4-line demultiplexer)

D_B	D_A	$1\overline{E}_2$	$1E_1$	$1\overline{Y}_0$	$1\overline{Y}_1$	$1\overline{Y}_2$	$1\overline{Y}_3$
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

D_B	D_A	$2\overline{E}_2$	$2\overline{E}_1$	$2\overline{Y}_0$	$2\overline{Y}_1$	$2\overline{Y}_2$	$2\overline{Y}_3$
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

(3-bit binary to 8-line decoder/1 line to 8 line demultiplexer)

D_C	D_B	D_A	$\overline{E}$	$2\overline{Y}_0$	$2\overline{Y}_1$	$2\overline{Y}_2$	$2\overline{Y}_3$	$1\overline{Y}_0$	$1\overline{Y}_1$	$1\overline{Y}_2$	$1\overline{Y}_3$
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Note 1 X : Irrelevant
D_C : Pin connecting $1E_1$ and $2\overline{E}_1$
$\overline{E}$: Pin connecting $1\overline{E}_2$ and $2\overline{E}_2$

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O=5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		4	mA
		V_{OL}≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
I_{OH}	High-level output current	V_{CC}=4.75V, V_I=0.8V V_I=2V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
		V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 2)			6.1	10	mA

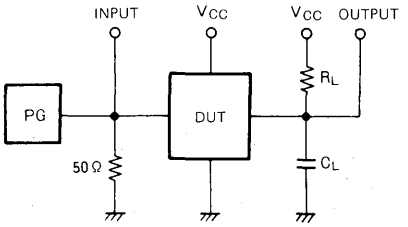
* : All typical values are at V_{CC}= 5V, T_a= 25°C.
Note 2: I_{CC} is measured with inputs $1\overline{E}_2$, $2\overline{E}_1$ and $2\overline{E}_2$ at 0V and with D_A, D_B and $1E_1$ at 4.5V

DUAL 2-BIT BINARY TO 4-LINE DECODER/DEMULTIPLEXER WITH OPEN COLLECTOR OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, *unless otherwise noted*)

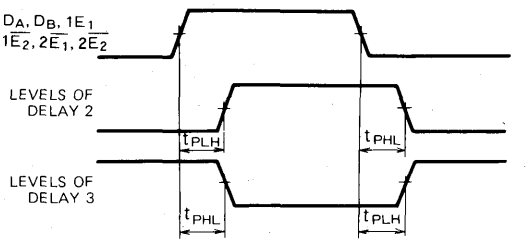
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B to outputs $\overline{Y_0}$~$\overline{Y_3}$	delay gate stages 2	R_L=2kΩ, C_L=15pF (Note 3)		18	40	ns
t_{PHL}					18	51	ns
t_{PLH}		delay gate stages 3			20	46	ns
t_{PHL}					18	51	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $1\overline{E_2}$, $2\overline{E_1}$, $2\overline{E_2}$ to outputs $\overline{Y_0}$~$\overline{Y_3}$				16	40	ns
t_{PHL}					20	51	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $1E_1$ to outputs $1\overline{Y_0}$ ~$1\overline{Y_3}$				20	48	ns
t_{PHL}					25	48	ns

Note 3: Measurement circuit



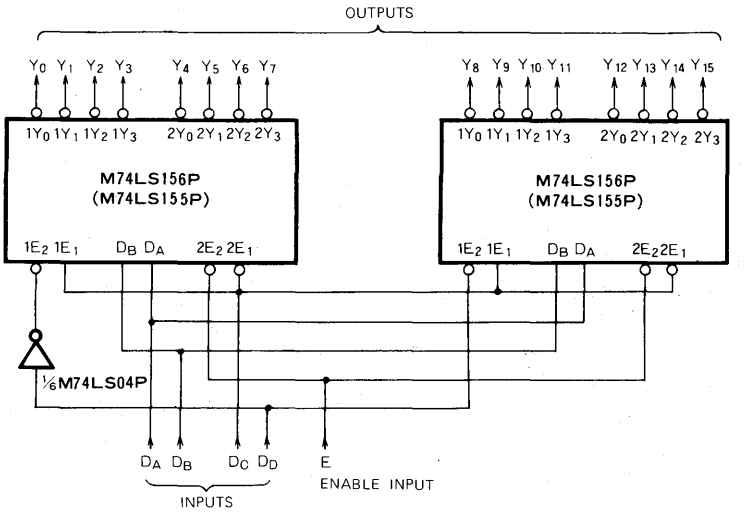
(1) The pulse generator (PG) has the following characteristics:
PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P = $3V_{P-P}$, Z_O=50Ω.
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

4-bit binary/hexadecimal decoder/demultiplexer



M74LS157P

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

DESCRIPTION

The M74LS157P is a semiconductor integrated circuit containing four 1-line to 2-line data selector/multiplexer circuits.

FEATURES

- Common strobe input for all 4 circuits
- Common select input for all 4 circuits
- Low output impedance
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

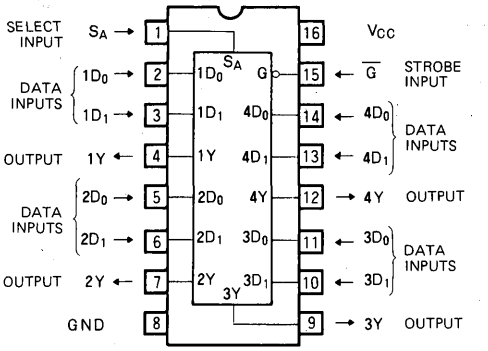
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has 4 circuits, each of which has a data selection function which selects one-line out of a 2-line signal and a multiplexing function to convert 2-bit parallel data into serial data by time sharing. When 2-line signals are fed to at inputs D_0 and D_1 and one of these is specified by the selection input S_A, the specified input signal is selected taken from output Y. The S_A and strobe inputs are common to all 4 circuits. When $\overline{G}$ is high, all the outputs, 1Y, 2Y, 3Y, and 4Y are low, regardless of the inputs.

M74LS157P has the same functions and pin connections as M74LS257P but the latter is provided with 3-state outputs.

PIN CONFIGURATION (TOP VIEW)



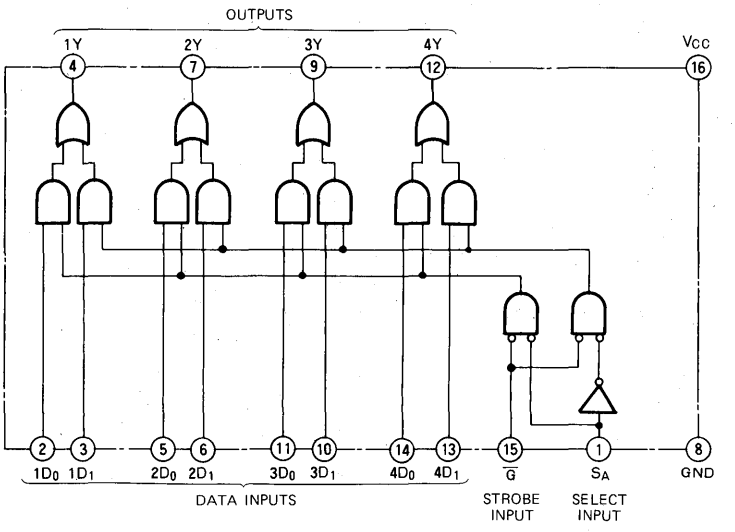
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{G}$	S_A	D_0	D_1	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Note 1: X : irrelevant

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

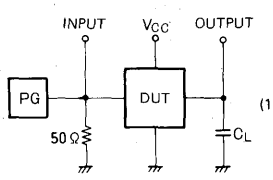
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V	I_{OL} = 4mA		0.25	0.4	V
			V_I = 0.8V, V_I = 2V	I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	D_0, D_1	V_{CC} = 5.25V				20	μA
		S_A, $\overline{G}$	V_I = 2.7V				40	
		D_0, D_1	V_{CC} = 5.25V				0.1	mA
		S_A, $\overline{G}$	V_I = 10V				0.2	
I_{IL}	Low-level input current	D_0, D_1	V_{CC} = 5.25V				−0.4	mA
		S_A, $\overline{G}$	V_I = 0.4V				−0.8	
I_{OS}	Short-circuit output current (Note 2)		V_{CC} = 5.25V, V_O = 0 V		−20		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25V (Note 3)			9.7	16	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with all inputs at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25℃, unless otherwise noted)

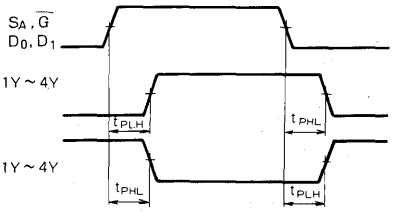
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D_0, D_1 to output Y	C_L = 15pF (Note 4)		7	14	ns
t_{PHL}				9	14	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input S_A to output Y			11	23	ns
t_{PHL}				14	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{G}$ to output Y			12	20	ns
t_{PHL}				12	21	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS158P

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (INVERTED)

DESCRIPTION

The M74LS158P is a semiconductor integrated circuit containing four 2-line to 1-line data selector/multiplexer circuits.

FEATURES

- Converted outputs provided
- Strobe inputs provided independently for each circuits
- Selection inputs common to four circuits
- Low output impedance
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

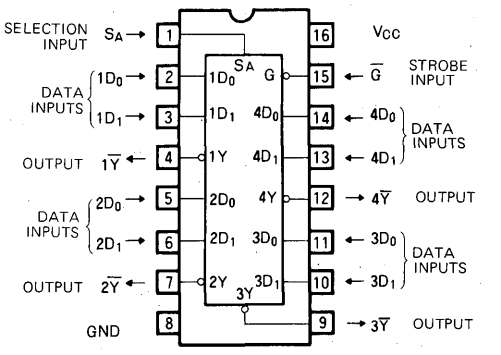
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has four data selector circuits which provide 2-line to 1-line selection for 4 pairs of signals using four multiplexer circuits which convert the 2-bit parallel data into serial data with time-sharing. When 2-line signals are applied to the data inputs D_0 and D_1 and 1 data is specified from among the data from selection input S_A, the input signal is inverted and can be output at $\overline{Y}$. By applying 2-bit parallel data to D_0 and D_1, and connecting a binary counter output to S_A, the D_0 and D_1 data are inverted and appear in the order to D_0 and D_1 synchronized with the clock pulse. S_A and strobe input $\overline{G}$ are common to all four circuits. When $\overline{G}$ is set high, $1\overline{Y}$, $2\overline{Y}$, $3\overline{Y}$ and $4\overline{Y}$ are set high irrespective of the status of the inputs.

M74LS158P has the same functions and pin connections as M74LS258P but the latter is provided with 3-state outputs.

PIN CONFIGURATION (TOP VIEW)



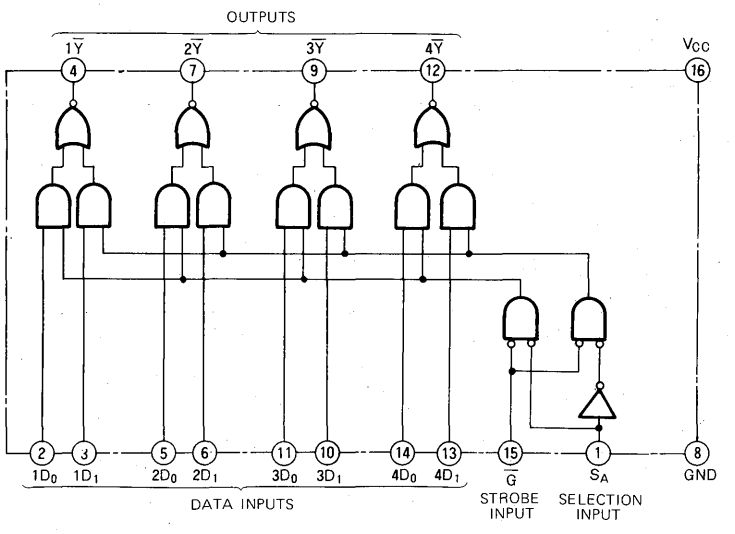
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{G}$	S_A	D_0	D_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Note 1 X : Irrelevant

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER (INVERTED)

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

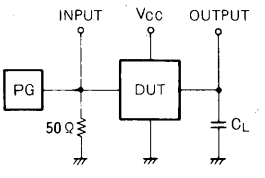
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
			V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	D_0, D_1	V_{CC}=5.25V				20	μA
		S_A, $\overline{G}$	V_I=2.7V				40	
		D_0, D_1	V_{CC}=5.25V				0.1	mA
		S_A, $\overline{G}$	V_I=10V				0.2	
I_{IL}	Low-level input current	D_0, D_1	V_{CC}=5.25V				−0.4	mA
		S_A, $\overline{G}$	V_I=0.4V				−0.8	
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O= 0 V		−20		−100	mA
I_{CCH}	High level Supply current		V_{CC}=5.25V (Note 3)			4.8	8	mA
I_{CCL}	Low-level supply current		V_{CC}=5.25V (Note 4)			6.5	11	mA

* : All typical values are at V_{CC}=5V, T_a=25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time. Note 3: I_{CC} is measured with all inputs at 4.5V.
Note 4: The supply current should be measured with $1D_0$~$4D_0$ at 4.5V and the other inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

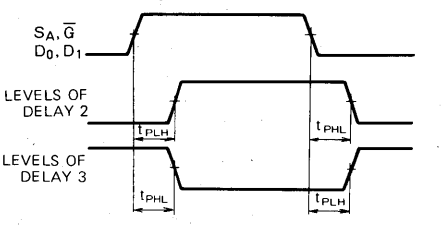
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_0, D_1 to output $\overline{Y}$	C_L=15pF (Note 5)		5	12	ns
t_{PHL}				5	12	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input S_A to output $\overline{Y}$			9	20	ns
t_{PHL}				10	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{G}$ to output $\overline{Y}$			8	17	ns
t_{PHL}				8	18	ns

Note 5: Measurement circuit



(1) The pulse generator (GP) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P\text{-}P}$, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS160AP

SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH DIRECT RESET

DESCRIPTION

The M74LS160AP is a semiconductor integrated circuit containing a presettable synchronous decade counter function with a direct reset input.

FEATURES

- Direct reset and synchronous preset inputs
- Carry output and enable input for cascade connection
- High-speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

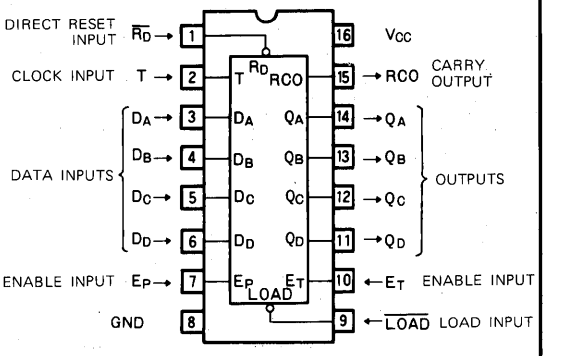
When the count pulse is applied to clock input T, the number of count pulses appears as a BCD code in the outputs Q_A, Q_B, Q_C and Q_D synchronized with the count pulse. Counting is done when T changes from low to high.

Presetting is performed to synchronize the count pulse. When data are applied to the data inputs D_A, D_B, D_C and D_D, the load input $\overline{LOAD}$ is made low and T is changed from low to high, the signals D_A, D_B, D_C and D_D appear at the Q_A, Q_B, Q_C and Q_D outputs, respectively, regardless of the status of enable inputs E_P and E_T, thereby presetting the counter.

When the counter is preset to a numerical value of 10 or more, counting proceeds in accordance with the status transition diagram.

Resetting is asynchronous. Q_A, Q_B, Q_C and Q_D are set low by setting direct reset input $\overline{R_D}$ low, regardless of the status of the other inputs.

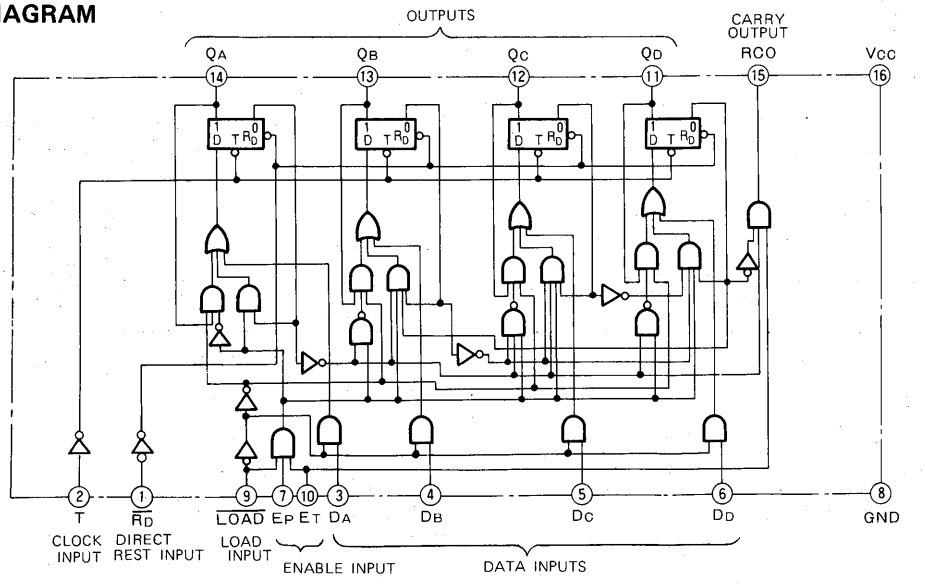
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

Carry output RCO is high only when Q_A is high, Q_B is low, Q_C is low, Q_D is high and E_T is high. E_P, E_T and RCO are used for synchronous counter cascade connection and for configuration of a divide-by-10^n counter. (Refer to the application examples.)

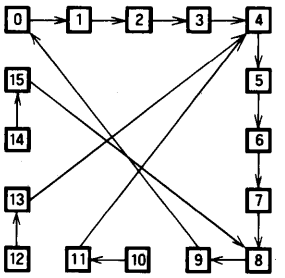
BLOCK DIAGRAM



MITSUBISHI ELECTRIC

SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH DIRECT RESET

STATE DIAGRAM

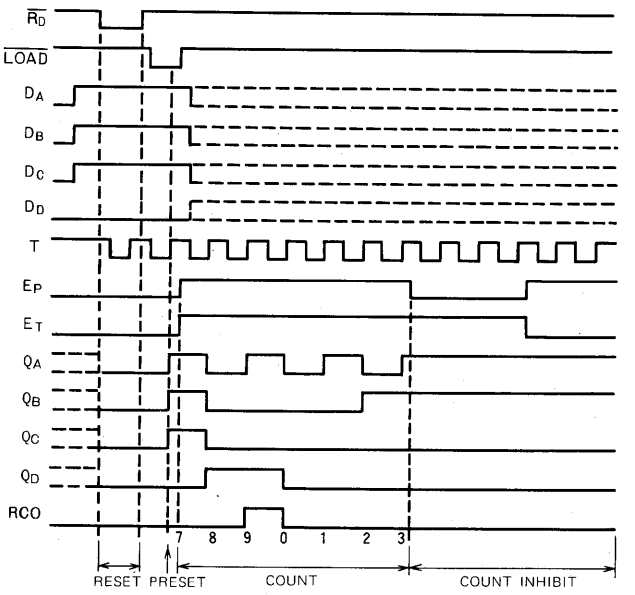


FUNCTION TABLE (Note 1)

$\overline{R_D}$	$\overline{LOAD}$	E_T	E_P	T	Q_A	Q_B	Q_C	Q_D	RCO
L	X	X	X	X	L	L	L	L	L
H	L	L	X	↑	D_A	D_B	D_C	D_D	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Inhibit				L
H	H	H	L	X	Inhibit				L*

Note 1. ↑ : Transition from low to high (positive edge trigger)
* : RCO is normally low but is high when Q_A is high, Q_B is low, Q_C is low, Q_D is high and E_T is high. Therefore, RCO = $Q_A \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot Q_D \cdot E_T$
X : Irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_O \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH DIRECT RESET

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ*	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{LOAD}, T, E_T$					40	μA
		$\overline{R_D}$					20	μA
		D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{LOAD}, T, E_T$					0.2	mA
		$\overline{R_D}$					0.1	mA
I_{IL}	Low-level input current	D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$\overline{LOAD}, T, E_T$					−0.8	mA
		$\overline{R_D}$					−0.4	mA
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high		$V_{CC}=5.25V$ (Note 3)			18	31	mA
I_{CCL}	Supply current, all outputs low		$V_{CC}=5.25V$ (Note 4)			19	32	mA

* : All typical values are at $V_{CC}=5V$, $Ta=25°C$.
Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3. I_{CCH} is measured with $D_A, D_B, D_C, D_D, E_P, E_T$, and $\overline{R_D}$ at 4.5V, $\overline{LOAD}$ at 0V, and T set from 0V to 4.5VA
Note 4. I_{CCL} is measured with $D_A, D_B, D_C, D_D, E_P, E_T$ and $\overline{R_D}$, $\overline{LOAD}$ at 0V and T set from 0V to 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

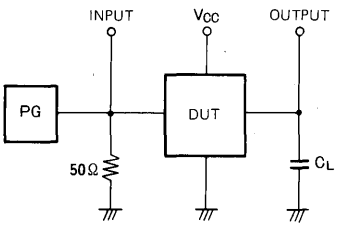
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum clock frequency	$C_L=15pF$ (Note 5)	25	55		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output RCO			20	35	ns
t_{PHL}				20	35	ns
t_{PLH}	Lwo-to-high-level, high-to-low-level output propagation time (when $\overline{LOAD}$ is high), from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				16	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time (when $\overline{LOAD}$ is low), from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				16	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E_T to output RCO			8	14	ns
t_{PHL}				8	14	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ outputs Q_A, Q_B, Q_C, Q_D			15	28	ns

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{W(TH)}$	Clock input T high pulse width		25	7		ns
$t_{W(TL)}$	Clock input T low pulse width		25	6		ns
$t_{W(\overline{R_D})}$	Direct reset $\overline{R_D}$ pulse width		20	6		ns
t_r	Clock pulse rise time			400	100	ns
$t_{SU(D)}$	Setup time $D_A \sim D_D$ to T		20	3		ns
$t_{SU(\overline{LOAD})}$	Setup time $\overline{LOAD}$ to T (Note 8)		20	6		ns
$t_{SU(E)}$	Setup time E_P, E_T to T		20	8		ns
$t_{h(D)}$	Hold time $D_A \sim D_D$ to T		3	0		ns
$t_{h(\overline{LOAD})}$	Hold time $\overline{LOAD}$ to T (Note 8)		3	−3		ns
$t_{h(E)}$	Hold time E_P, E_T to T		3	−3		ns
$t_{rec(\overline{R_D})}$	Recovery time $\overline{R_D}$ to T		15	6		ns

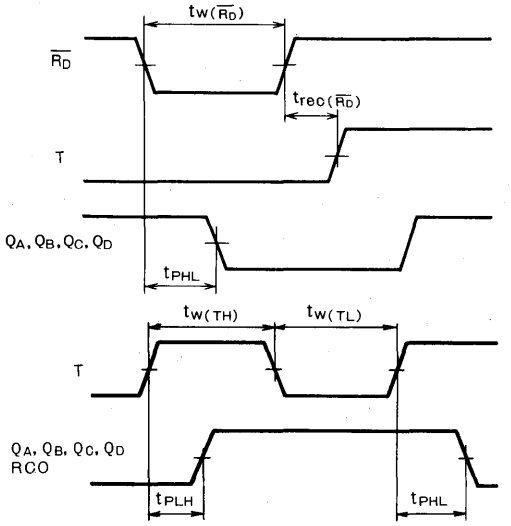
SYNCHRONOUS PRESETTABLE DECADE COUNTER WITH DIRECT RESET

Note 5. Measurement circuit



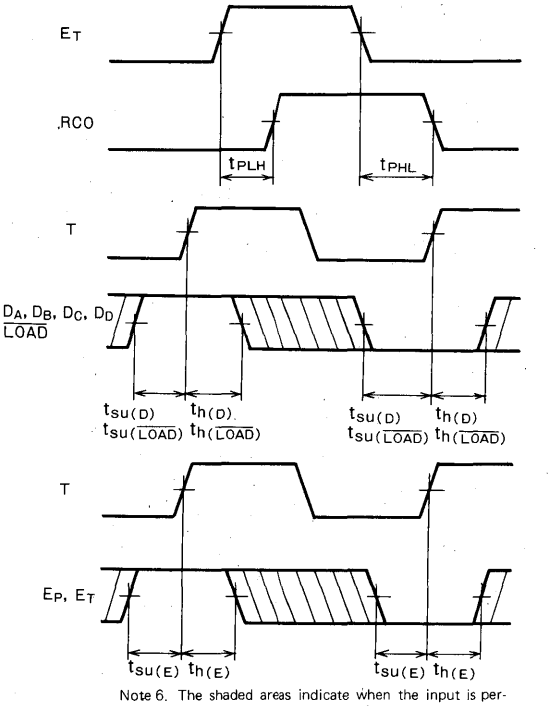
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Zo = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



Note 7. When the clock input T does not satisfy these standards, an incorrect counting operation may result.

Note 8. When the load input $\overline{LOAD}$ setup time and hold time are not satisfied, the incorrect data may be preset. (When LOAD changes within ± 5ns of the $\overline{LOAD}$ input transition from low to high, presetting may be made to low when the data input is high.)

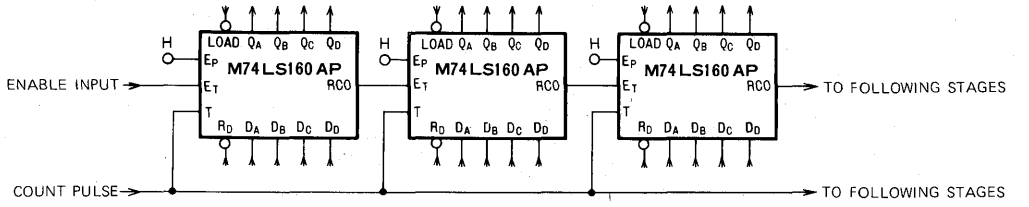


Note 6. The shaded areas indicate when the input is permited to change for predictable output performance.

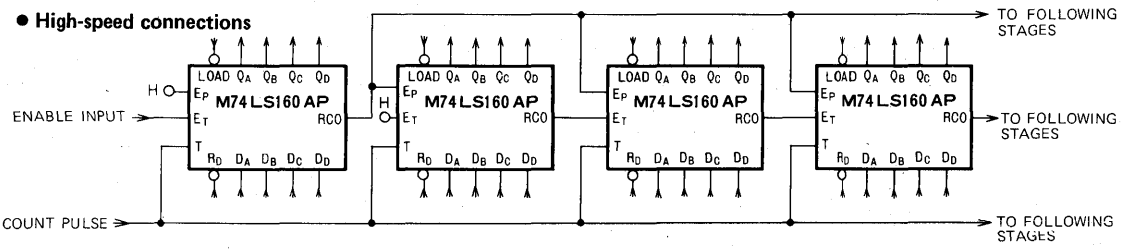
APPLICATION EXAMPLE

Cascade-connected divided-by-10^n counter

- **Low-speed connections**



- **High-speed connections**



M74LS161AP

SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

DESCRIPTION

The M74LS161AP is a semiconductor integrated circuit containing a synchronous presettable 4-bit binary (hexadecimal) counter with direct reset input.

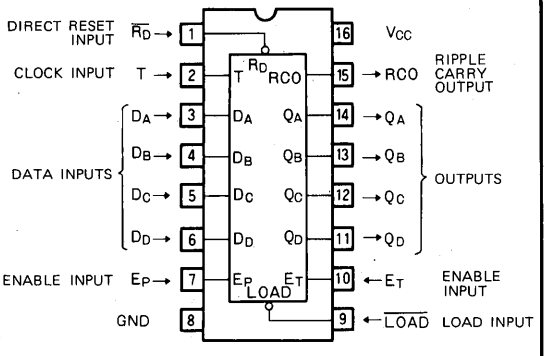
FEATURES

- Direct reset and synchronous preset inputs
- Enable input and carry output for cascaded operation
- High-speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range (T_a = -20 ~ 75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPITON

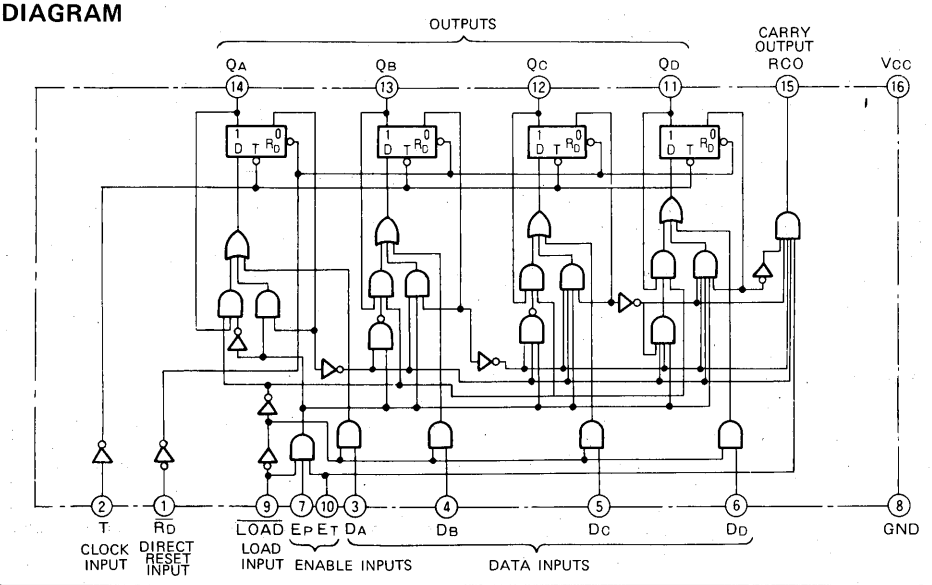
When a counting pulse is applied to the T input, the 4-bit binary representation of the count is output at Q_A, Q_B, Q_C and Q_D in synchronization with the count pulse. Counting is done on the transition of the T input signal from low to high.

Presetting is accomplished in synchronization with the counting pulse. When preset data is applied to the D_A, D_B, D_C and D_D inputs, the load input $\overline{LOAD}$ is made low, and T is changed from low to high, this data will appear in the Q_A, Q_B, Q_C and Q_D outputs, respectively regardless of the status of the enable inputs E_P and E_T, thereby presetting counter.

Resetting is performed asynchronously by setting the direct reset input $\overline{R_D}$ to low at which time the Q_A, Q_B, Q_C and Q_D outputs go to low-level regardless of the states of the other inputs.

The ripple carry output RCO is high only when all Q outputs and E_T are high. The two enable inputs E_P and E_T and the RCO carry output can be used to form an n-bit synchronous counter by means of cascade connection of several ICs (refer to the application example for the M74LS160AP).

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

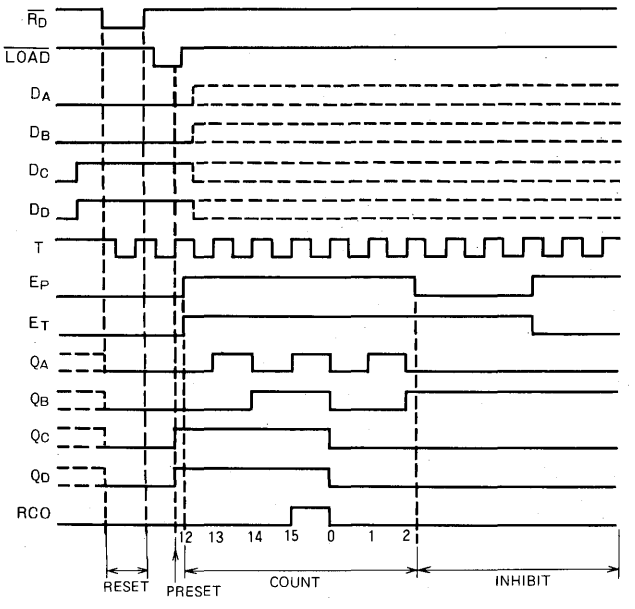
SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

FUNCTION TABLE (Note 1)

$\overline{R_D}$	$\overline{LOAD}$	E_T	E_P	T	Q_A	Q_B	Q_C	Q_D	RCO
L	X	X	X	X	L	L	L	L	L
H	L	L	X	↑	D_A	D_B	D_C	D_D	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Inhibit				L
H	H	H	L	X	Inhibit				L*

Note 1: ↑ : Indicates a transition from low to high (positive edge triggering).
* : RCO is normally low but is high when all Q outputs and E_T are high simultaneously, i.e., $RCO = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot E_T$
X : irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
			$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{LOAD}, T, E_T$					40	
		$\overline{R_D}$					20	
		D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{LOAD}, T, E_T$					0.2	
		$\overline{R_D}$					0.1	
I_{IL}	Low-level input current	D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$\overline{LOAD}, T, E_T$					−0.8	
		$\overline{R_D}$					−0.4	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high		$V_{CC}=5.25V$ (Note 3)			18	31	mA
I_{CCL}	Supply current, all outputs low		$V_{CC}=5.25V$ (Note 4)			19	32	mA

* : Typical values are for $V_{CC}=5V$ and $T_a=25°C$

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

3: Measurement of the high-level power supply current is performed with all data inputs, E_P, E_T and $\overline{R_D}$ at 4.5V and the $\overline{LOAD}$ input at 0V, changing the T input from 0V to 4.5V.

4: Measurement of the high-level power supply current is performed with all data inputs, E_P, E_T, $\overline{R_D}$ and $\overline{LOAD}$ at 0V, changing the T input from 0V to 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

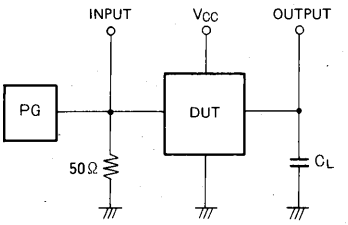
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L=15pF$ (Note 5)	25	55		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output RCO			20	35	ns
t_{PHL}				20	35	ns
t_{PLH}	Lwo-to-high-level, high-to-low-level output propagation time (when $\overline{LOAD}$ is high), from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				16	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time (when $\overline{LOAD}$ is low), from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				16	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E_T to output RCO			8	14	ns
t_{PHL}				8	14	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ outputs Q_A, Q_B, Q_C, Q_D			15	28	ns

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(TH)}$	Clock input T high pulse width		25	7		ns
$t_{W(TL)}$	Clock input T low pulse width		25	6		ns
$t_{W(\overline{R_D})}$	Direct reset $\overline{R_D}$ pulse width		20	6		ns
t_r	Clock pulse rise time			400	100	ns
$t_{SU(D)}$	Setup time $D_A \sim D_D$ to T		20	3		ns
$t_{SU(\overline{LOAD})}$	Setup time $\overline{LOAD}$ to T (Note 8)		20	6		ns
$t_{SU(E)}$	Setup time E_P, E_T to T		20	8		ns
$t_{h(D)}$	Hold time $D_A \sim D_D$ to T		3	0		ns
$t_{h(\overline{LOAD})}$	Hold time $\overline{LOAD}$ to T (Note 8)		3	−3		ns
$t_{h(E)}$	Hold time E_P, E_T to T		3	−3		ns
$t_{rec(\overline{R_D})}$	Recovery time $\overline{R_D}$ to T		15	6		ns

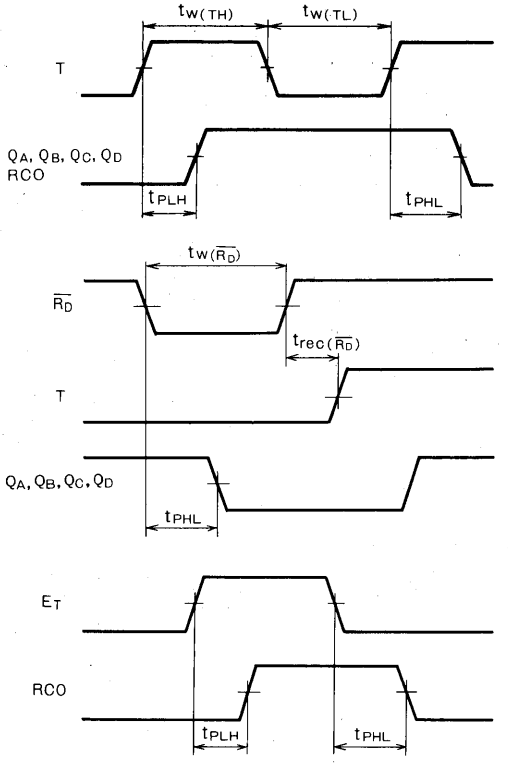
SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER WITH DIRECT RESET

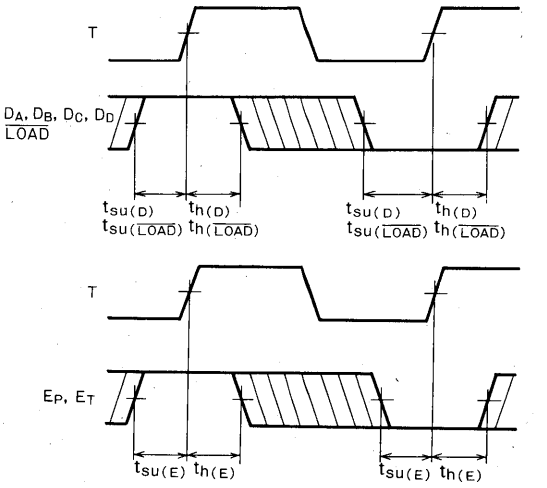
Note 5: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
V_P = 3V_{P-P}, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

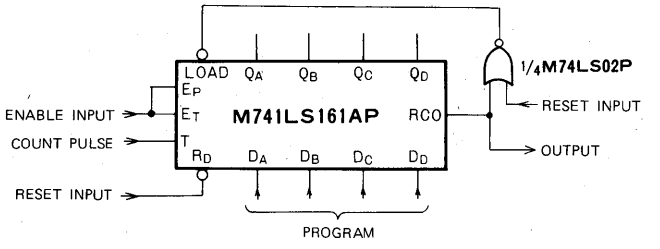




Note 6. The shaded area indicates the period within which switching may take place.

APPLICATION EXAMPLE

Programmable divider



Note 7: Reset is performed by applying countpulse with reset input high. $\overline{R_D}$ pin cannot be used since Q_A~Q_D should be set low.

DA	DB	DC	DD	Divide rate
L	L	L	L	1/16
H	L	L	L	1/15
L	H	L	L	1/14
H	H	L	L	1/13
L	L	H	L	1/12
H	L	H	L	1/11
L	H	H	L	1/10
H	H	H	L	1/9
L	L	L	H	1/8
H	L	L	H	1/7
L	H	L	H	1/6
H	H	L	H	1/5
L	L	H	H	1/4
H	L	H	H	1/3
L	H	H	H	1/2

M74LS162AP

FULLY SYNCHRONOUS PRESETTABLE DECADE COUNTER

DESCRIPTION

The M74LS162AP is a semiconductor integrated circuit containing a synchronous presettable decade counter function with a synchronous reset input.

FEATURES

- Synchronous reset and preset inputs
- Carry output and enable input for cascade connection
- High-speed counting (f_{max}= 55MHz typical)
- Wide operating temperature range (T_a= -20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

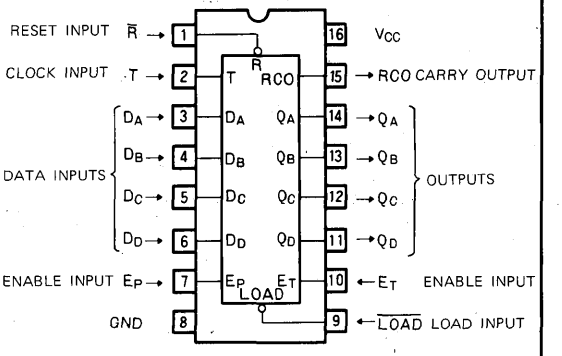
When the count pulses are applied to clock input T, the number of count pulses appears as a BCD code in the outputs Q_A, Q_B, Q_C, Q_D synchronized with the count pulses. Counting is done when T changes from low to high.

Presetting is performed to synchronize the count pulse. When data are applied to the data inputs D_A, D_B, D_C and D_D, the load input $\overline{LOAD}$ is made low and T is changed from low to high, the signals D_A, D_B, D_C and D_D appear at the Q_A, Q_B, Q_C and Q_D outputs, respectively, regardless of the status of enable inputs E_P and E_T, thereby presetting the counter. When the counter is preset to a numerical value of 10 or more, counting proceeds in accordance with the status transition diagram.

Resetting is synchronized with the count pulses. Q_A, Q_B, Q_C and Q_D are set low by setting reset input $\overline{R}$ low and by changing T from low to high.

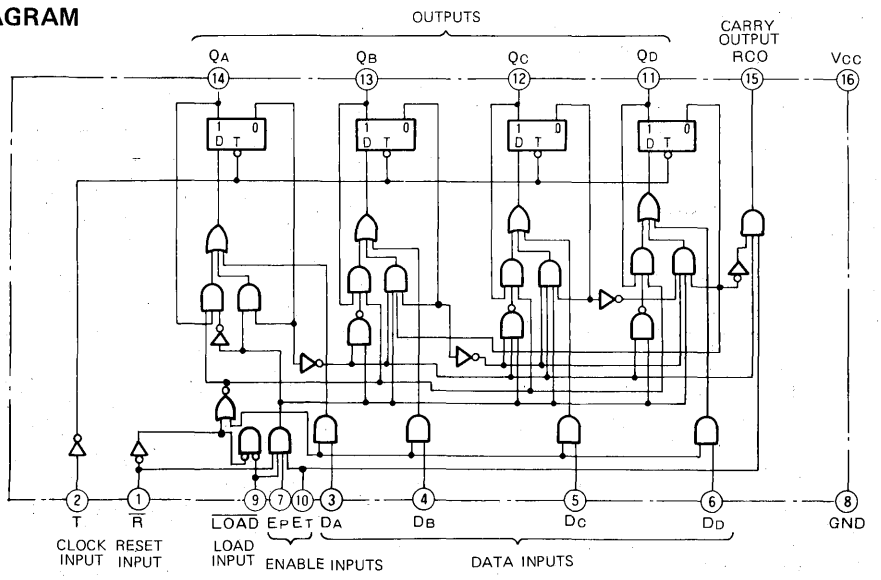
Carry output RCO is high only when Q_A is high, Q_B is low, Q_C is low, Q_D is high and E_T is high. E_P, E_T and RCO are used for synchronous counter cascade connection and for configuration of an n-bit counter. (Refer to the application examples of the M74LS160AP.)

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



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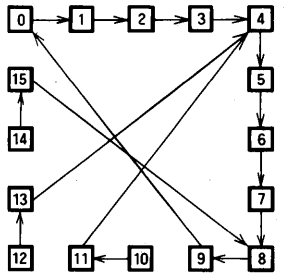
FULLY SYNCHRONOUS PRESETTABLE DECADE COUNTER

STATE DIAGRAM



FUNCTION TABLE (Note 1)

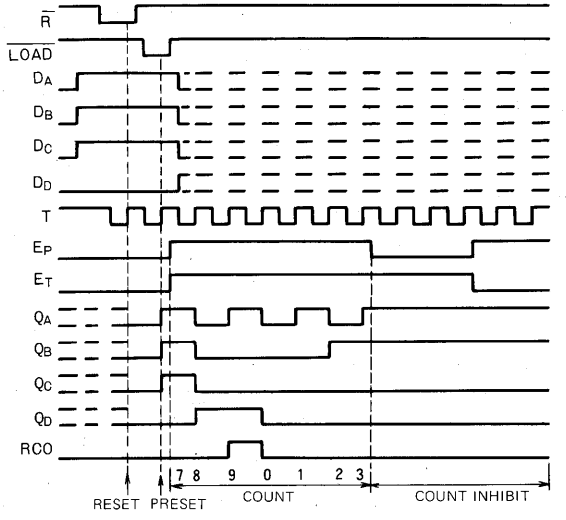
$\overline{R}$	$\overline{LOAD}$	E_T	E_P	T	Q_A	Q_B	Q_C	Q_D	RCO
L	X	X	X	↑	L	L	L	L	L
H	L	L	X	↑	D_A	D_B	D_C	D_D	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Inhibit				L
H	H	H	L	X	Inhibit				L*

Note 1 ↑ : Transition from low to high (positive edge trigger)

* : RCO is normally low but is high when Q_A is high, Q_B is low, Q_C is low, Q_D is high and E_T is high. Therefore, RCO = $Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot E_T$

X : Irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 20 ~ + 75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

FULLY SYNCHRONOUS PRESETTABLE DECADE COUNTER

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ*	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{LOAD}, T, E_T$					40	μA
		$\overline{R}$					40	μA
		D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{LOAD}, T, E_T$					0.2	mA
		$\overline{R}$					0.2	mA
I_{IL}	Low-level input current	D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$\overline{LOAD}, T, E_T$					−0.8	mA
		$\overline{R}$					−0.8	mA
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high		$V_{CC}=5.25V$ (Note 3)			18	31	mA
I_{CCL}	Supply current, all outputs low		$V_{CC}=5.25V$ (Note 4)			19	32	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3. I_{CCH} is measured with $D_A, D_B, D_C, D_D, E_P, E_T$, and $\overline{R}$ at 4.5V, $\overline{LOAD}$ at 0V, then 4.5V applied to T input.
Note 4. I_{CCL} is measured with $D_A, D_B, D_C, D_D, E_P, E_T$ and $\overline{R}$, $\overline{LOAD}$ at 0V and T set from 0V to 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5 V, Ta=25°C, unless otherwise noted)

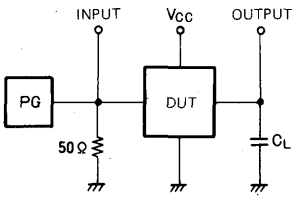
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum clock frequency	$C_L = 15pF$ (Note 5)	25	55		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output RCO			20	35	ns
t_{PHL}				20	35	ns
t_{PLH}	Lwo-to-high-level, high-to-low-level output propagation time (when LOAD is high), from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				16	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time (when LOAD is low), from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				16	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E_T to output RCO			8	14	ns
t_{PHL}				8	14	ns

TIMING REQUIREMENT (V_{CC}= 5 V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{w(TH)}$	Clock input T high pulse width		25	7		ns
$t_{w(TL)}$	Clock input T low pulse width		25	6		ns
t_r	Clock pulse rise time			400	100	ns
$t_{su(D)}$	Setup time $D_A \sim D_D$ to T		20	3		ns
$t_{su(\overline{LOAD})}$	Setup time $\overline{LOAD}$ to T (Note 8)		20	6		ns
$t_{su(\overline{R})}$	Setup time $\overline{R}$ to T		20	11		ns
$t_{su(E)}$	Setup time E_P, E_T to T		20	8		ns
$t_{h(D)}$	Hold time $D_A \sim D_D$ to T		3	0		ns
$t_{h(\overline{LOAD})}$	Hold time $\overline{LOAD}$ to T (Note 8)		3	−3		ns
$t_{h(\overline{R})}$	Hold time $\overline{R}$ to T		3	−8		ns
$t_{h(E)}$	Hold time E_P, E_T to T		3	−5		ns

FULLY SYNCHRONOUS PRESETTABLE DECADE COUNTER

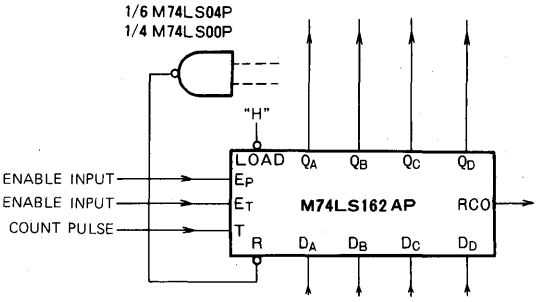
Note 5. Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f ≈ 6ns, t_W = 500ns, VP = $3V_{P-P}$, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance

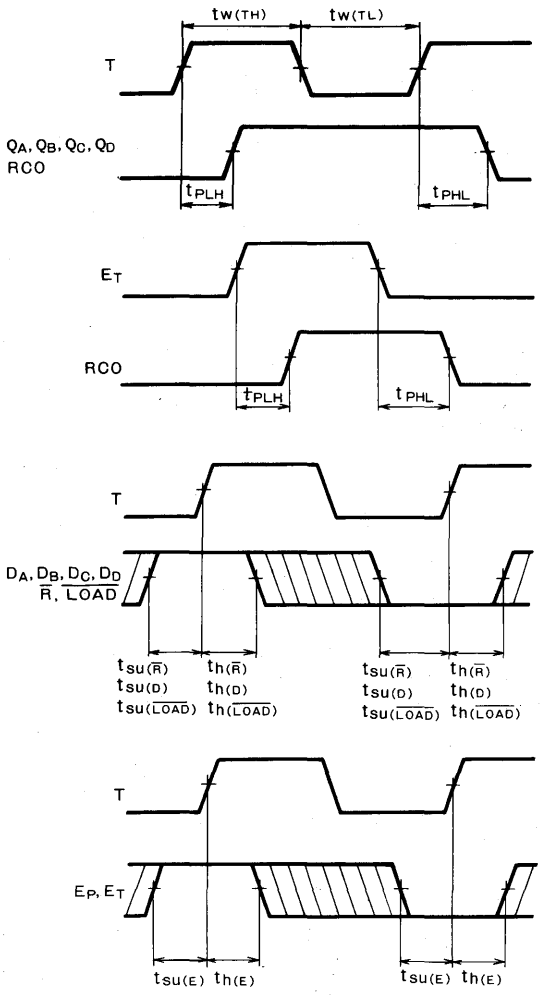
APPLICATION EXAMPLES

Divide-by-n counter configuration



Divide-by-n counter	Pins connected to gate input
Ternary counter	Q_B
Divide-by 5 counter	Q_C
Divide-by-6 counter	Q_A, Q_C
Divide-by-7 counter	Q_B, Q_C
Divide-by-9 counter	Q_D

TIMING DIAGRAM (Reference level = 1.3V)



Note 6. The shaded areas indicate when the input is permited to change for predictable output performance.

M74LS163AP

FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

DESCRIPTION

The M74LS163AP is a semiconductor integrated circuit containing a synchronous presettable 4-bit binary (hexadecimal) counter with a synchronous reset input.

FEATURES

- Synchronous reset and preset inputs.
- Cascade connected enable input and carry output.
- High speed counting (f_{max} = 55MHz typical)
- Wide operating temperature range (T_a = -20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

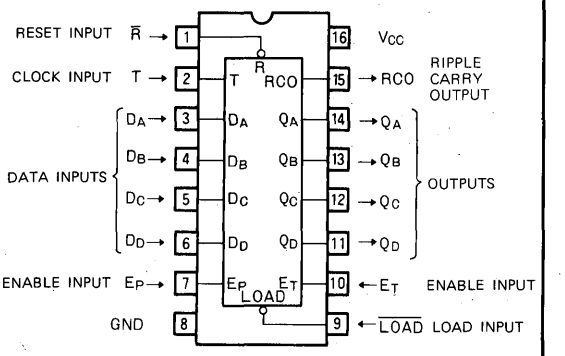
FUNCTIONAL DESCRIPTION

When count pulses are applied to the clock input T, the number of count pulses appears as a 4-bit binary code in the outputs Q_A, Q_B, Q_C, and Q_D synchronized with the count pulses. Counting is done when T changes from low to high.

Presetting is performed to synchronize the count pulse. When data is applied to the data inputs D_A, D_B, D_C and D_D, the load input $\overline{LOAD}$ is made low, and T is changed from low to high, the signals D_A, D_B, D_C, and D_D appear at the Q_A, Q_B, Q_C, and Q_D outputs, respectively, regardless of the status of the enable inputs E_P and E_T, thereby presetting the counter.

Reset is performed, synchronized with the count pulse. When the reset input $\overline{R}$ is made low, and T is changed from low to high, Q_A, Q_B, Q_C, and Q_D will be low.

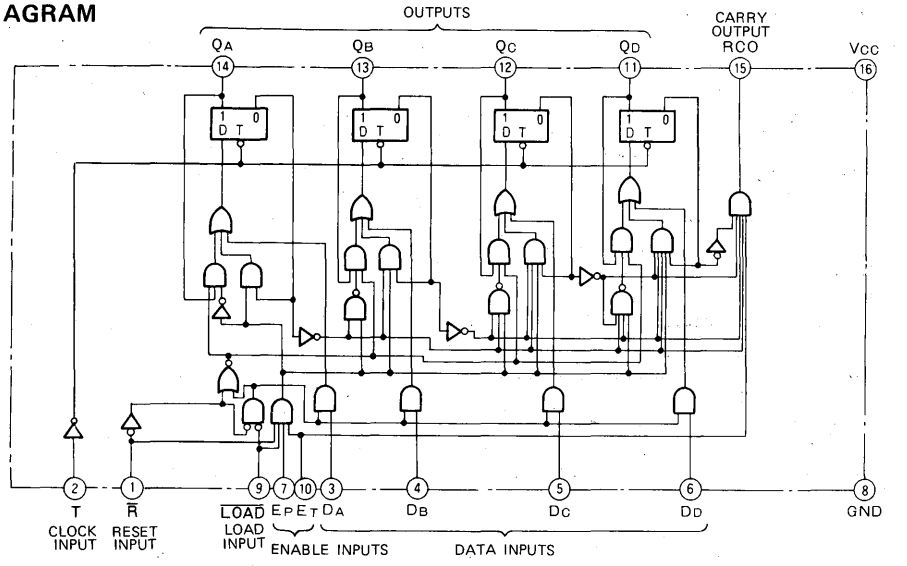
PIN CONFIGURATION (TOP VIEW)



Outline 16P4

The ripple carry output RCO is high only when $Q_A = Q_B = Q_C = Q_D$ = high and E_T = high. E_P, E_T and RCO are used when the counter is cascade connected in a synchronous manner to from an n-bit counter. (See the M74LS160AP application example).

BLOCK DIAGRAM



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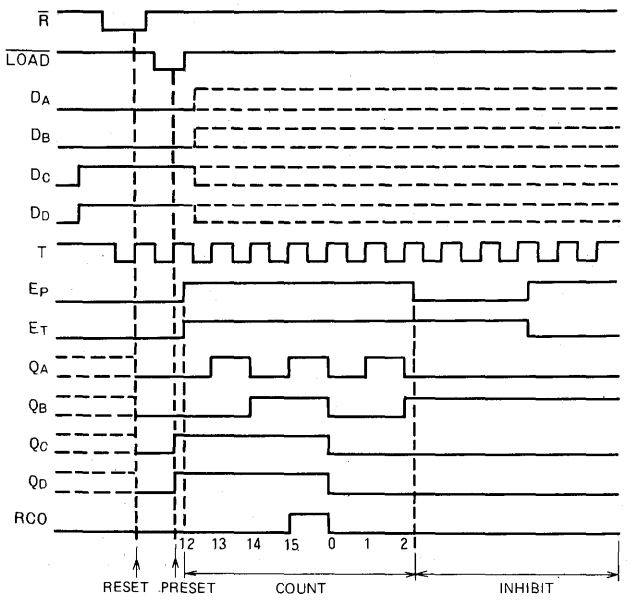
FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

FUNCTION TABLE (Note 1)

$\overline{R}$	$\overline{LOAD}$	E_T	E_P	T	Q_A	Q_B	Q_C	Q_D	RCO
L	X	X	X	↑	L	L	L	L	L
H	L	L	X	↑	D_A	D_B	D_C	D_D	L
H	L	H	X	↑					L*
H	H	H	H	↑	Count				L*
H	H	L	X	X	Inhibit				L
H	H	H	L	X	Inhibit				L*

Note 1: ↑ : transition from low to high level
* : RCO output is normally low-level, but RCO output is high-level when E_T input is high-level while the counter is in its maximum count state (HHHH).
X : irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ*	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
			$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{LOAD}, T, E_T$					40	
		$\overline{R}$					40	
		D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{LOAD}, T, E_T$					0.2	
		$\overline{R}$					0.2	
I_{IL}	Low-level input current	D_A, D_B, D_C, D_D, E_P	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$\overline{LOAD}, T, E_T$					−0.8	
		$\overline{R}$					−0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	Supply current, all outputs high		$V_{CC}=5.25V$ (Note 3)			18	31	mA
I_{CCL}	Supply current, all outputs low		$V_{CC}=5.25V$ (Note 4)			19	32	mA

* : All typical values are at $V_{CC}=5V$, $Ta=25°C$.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

3: I_{CCH} is measured with $D_A, D_B, D_C, D_D, E_T, \overline{R}$ inputs at 4.5V, $\overline{LOAD}$ inputg rounded and a momentary ground, then 4.5V, applied to T input.

4: I_{CCL} is measured with $D_A, D_B, D_C, D_D, E_T, \overline{R}$, $\overline{LOAD}$ inputs grounded and a momentary ground, then 4.5V, applied to T input.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

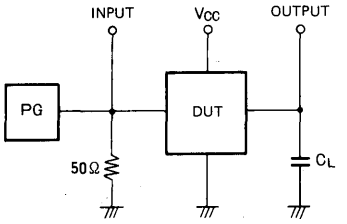
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum clock frequency	$C_L=15pF$ (Note 5)	25	55		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output RCO			20	35	ns
t_{PHL}				20	35	ns
t_{PLH}	Lwo-to-high-level, high-to-low-level output propagation time (when LOAD is high), from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				16	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time (when LOAD is low), from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				16	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E_T to output RCO			8	14	ns
t_{PHL}				8	14	ns

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{W(TH)}$	Clock input T high pulse width		25	7		ns
$t_{W(TL)}$	Clock input T low pulse width		25	6		ns
t_r	Clock pulse rise time			400	100	ns
$t_{SU(D)}$	Setup time $D_A \sim D_D$ to T		20	3		ns
$t_{SU(\overline{LOAD})}$	Setup time $\overline{LOAD}$ to T (Note 7)		20	6		ns
$t_{SU(\overline{R})}$	Setup time $\overline{R}$ to T		20	11		ns
$t_{SU(E)}$	Setup time E_P, E_T to T		20	8		ns
$t_{h(D)}$	Hold time $D_A \sim D_D$ to T		3	0		ns
$t_{h(\overline{LOAD})}$	Hold time $\overline{LOAD}$ to T (Note 7)		3	−3		ns
$t_{h(\overline{R})}$	Hold time $\overline{R}$ to T		3	−8		ns
$t_{h(E)}$	Hold time E_P, E_T to T		3	−5		ns

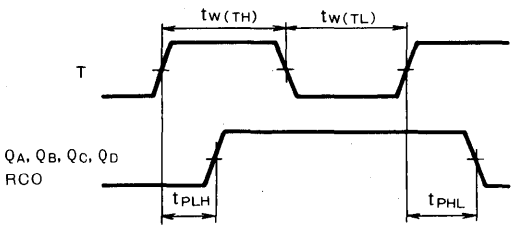
FULLY SYNCHRONOUS PRESETTABLE 4-BIT BINARY COUNTER

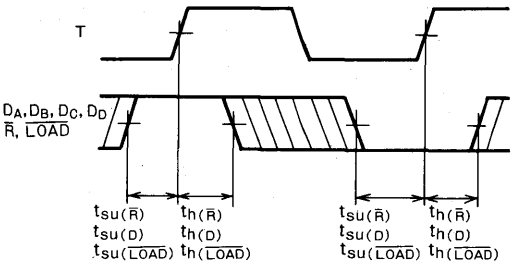
Note 5: Measurement circuit

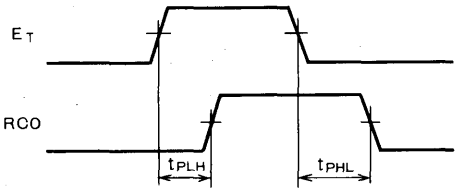


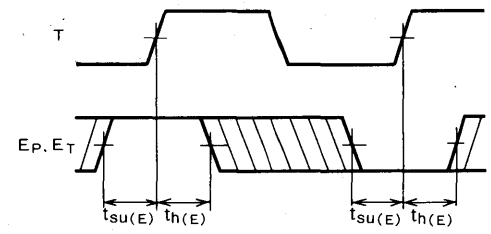
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)





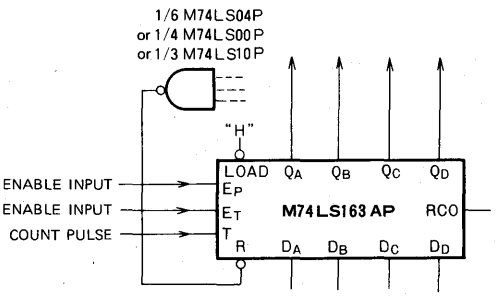




Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Variable modulo counter



Divide rate	Outputs connect to inputs of GATE
3	Q_B
5	Q_C
6	Q_A, Q_C
7	Q_B, Q_C
9	Q_D
10	Q_A, Q_D
11	Q_B, Q_D
12	Q_A, Q_B, Q_D
13	Q_C, Q_D
14	Q_A, Q_C, Q_D
15	Q_B, Q_C, Q_D

M74LS164P

8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER

DESCRIPTION

The M74LS164P is a semiconductor integrated circuit containing an 8-bit serial input-serial/parallel output shift register function with direct reset input.

FEATURES

- Serial input-serial/parallel output
- Direct reset input provided
- 8-bit for high space factor
- Input load factor of 1 for each input
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

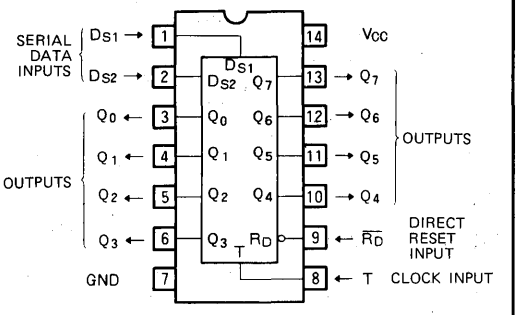
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is configured with 9 D-type edge-triggered flip-flops and the serial data inputs D_{S1} and D_{S2} logic product D_{S1} x D_{S2} represents the first-stage flip-flop data input. Outputs Q_0~Q_7 are taken out from the flip-flop Q outputs. When D_{S1} and D_{S2} are both high and the clock pulse is applied to T, the high signal is shifted in sequence into Q_0, Q_1 ... Q_7. When either D_{S1} or D_{S2} or both are low and the clock pulse is applied to T, the low signal is shifted into Q_0, Q_1 ... Q_7 in sequence. Shifting is performed when T changes from low to high.

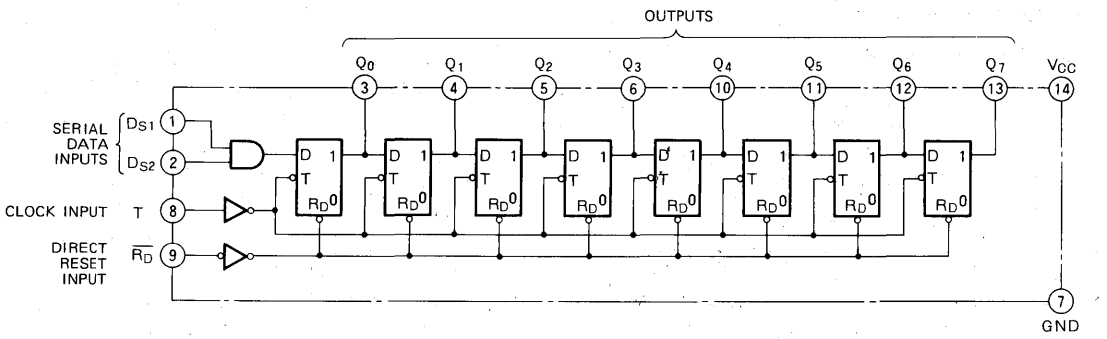
When the direct reset input R_D is set low, all the outputs are reset low irrespective of the other input signals. $\overline{R_D}$ should be kept at high when using this device as a shift register.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

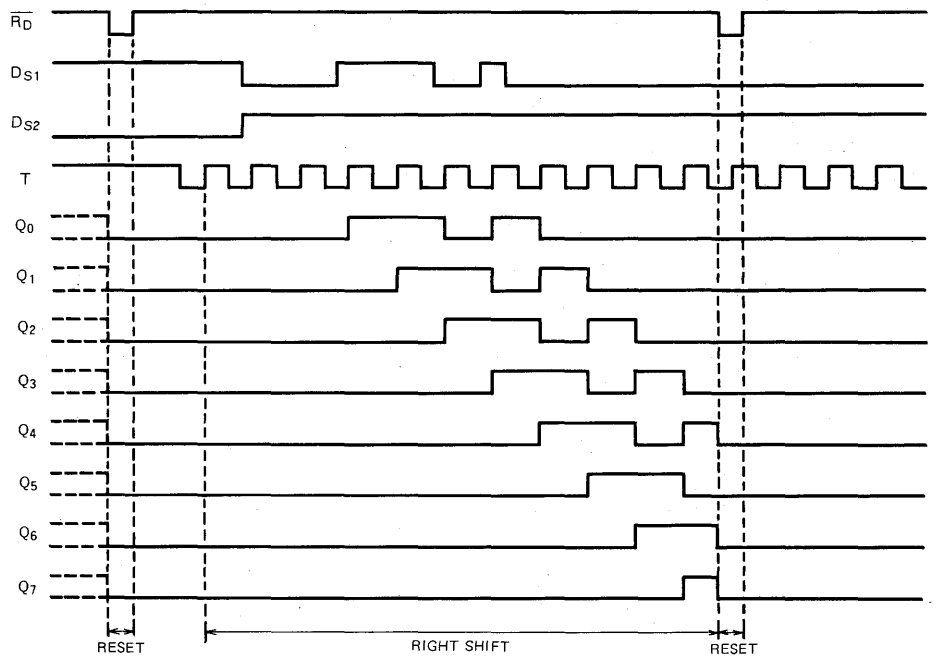
8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER

FUNCTION TABLE (Note 1)

Operational mode	$\overline{R_D}$	T	D_{S1}	D_{S2}	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Reset	L	X	X	X	L	L	L	L	L	L	L	L
Right shift	H	↑	L	L	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0
	H	↑	H	L	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0
	H	↑	L	H	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0
	H	↑	H	H	H	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0

Note 1 ↑ : Transition from low to high (positive edge trigger)
Q^0 : Level of output before the change from low to high
X : Irrelevant

OPERATION TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

8-BIT SERIAL-IN PARALLEL-OUT SHIFT REGISTER

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

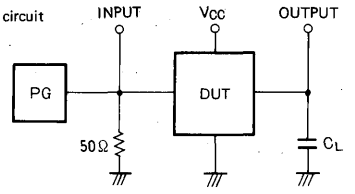
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$			−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$	2.7	3.5		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $I_{OL}=4mA$		0.25	0.4	V
		$V_I=0.8V, V_I=2V$, $I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$			20	μA
		$V_{CC}=5.25V$, $V_I=10V$			0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$			−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$	−20		−100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 3)		16	27	mA

* : All typical values are at V_{CC}=5V, Ta=25°C.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with D_{S1} and D_{S2} at 0V, 4.5V applied to T after $\overline{R_D}$ has been set from 0V to 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L=15pF$ (Note 4)	25	50		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs $Q_0 \sim Q_7$			13	27	ns
t_{PHL}				14	32	ns
t_{PHL}	Low-to-high-level, high-to-low-level output propagation time, input $\overline{R_D}$ to outputs $Q_0 \sim Q_7$			18	36	ns

Note 4: Measurement circuit

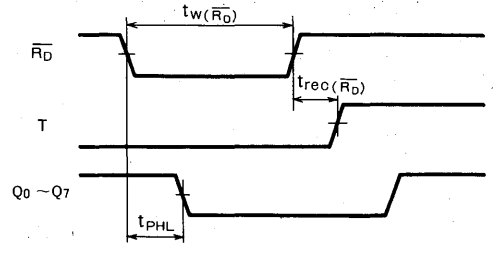


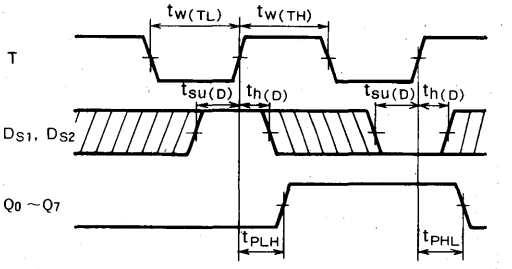
(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Zo=50Ω.
(2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(TH)}$	Clock input T high pulse width		20	8		ns
$t_{W(TL)}$	Clock input T low pulse width		20	10		ns
$t_{W(\overline{R_D})}$	Direct reset $\overline{R_D}$ pulse width		20	9		ns
$t_{SU(D)}$	Setup time D_{S1}, D_{S2} to T		15	3		ns
$t_{h(D)}$	Hold time D_{S1}, D_{S2} to T		5	2		ns
$t_{rec(\overline{R_D})}$	Recovery time $\overline{R_D}$ to T		20	−1		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

MITSUBISHI ELECTRIC

M74LS165AP

8-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER

DESCRIPTION

The M74LS165AP is a semiconductor integrated circuit containing an 8-bit serial/parallel input – serial output shift register function.

FEATURES

- Parallel-to-serial data conversion
- Complementary output (Q_7 and $\overline{Q_7}$)
- Direct overriding load (data) input
- Clock inhibit input
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

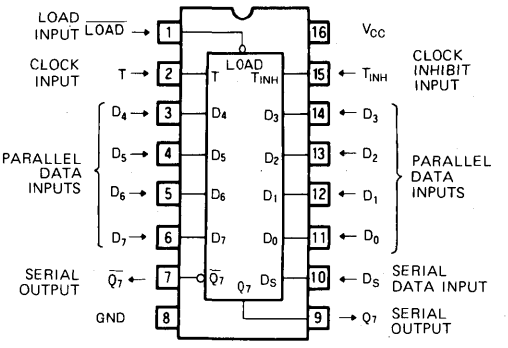
This device is configured from eight R-S-T flip-flop circuits and is designed to accept serial data input through D_S, or parallel data input through D_0 ~ D_7.

When D_S is used as the input, a clock pulse is applied to clock input T when load input $\overline{LOAD}$ is high-level and the clock inhibit input T_{INH} is low-level.

Shift operations are initiated upon T transiting from low to high, and the data present at D_S appears as an output pulse from Q_7, $\overline{Q_7}$ of the 8th flip-flop circuit. The output at $\overline{Q_7}$ is always an inverted value of that present at Q_7.

When D_0 ~ D_7 is used as the input, $\overline{LOAD}$ is active-low. Since D_0 ~ D_7 are entered at the direct-set, direct-reset input of each flip-flop, read is executed regardless of the status of other inputs.

PIN CONFIGURATION (TOP VIEW)

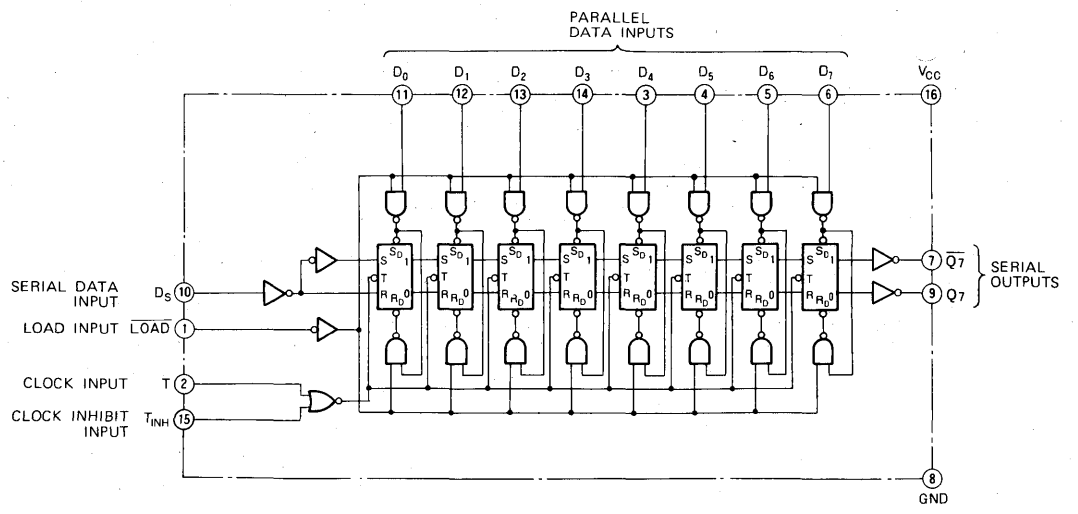


Outline 16P4

Care should be exercised to prevent the recording of erroneous data caused by a change in the value of D_0 ~ D_7 when $\overline{LOAD}$ switches from low to high-value. Also, when T_{INH} is high, a shift operation will not be effected with clock pulse input. When T is low-level, and T_{INH} transits from low to high, a 1-bit shift operation will be executed.

M74LS165AP is an enhanced-performance version of M74LS165P having modified switching characteristics.

BLOCK DIAGRAM



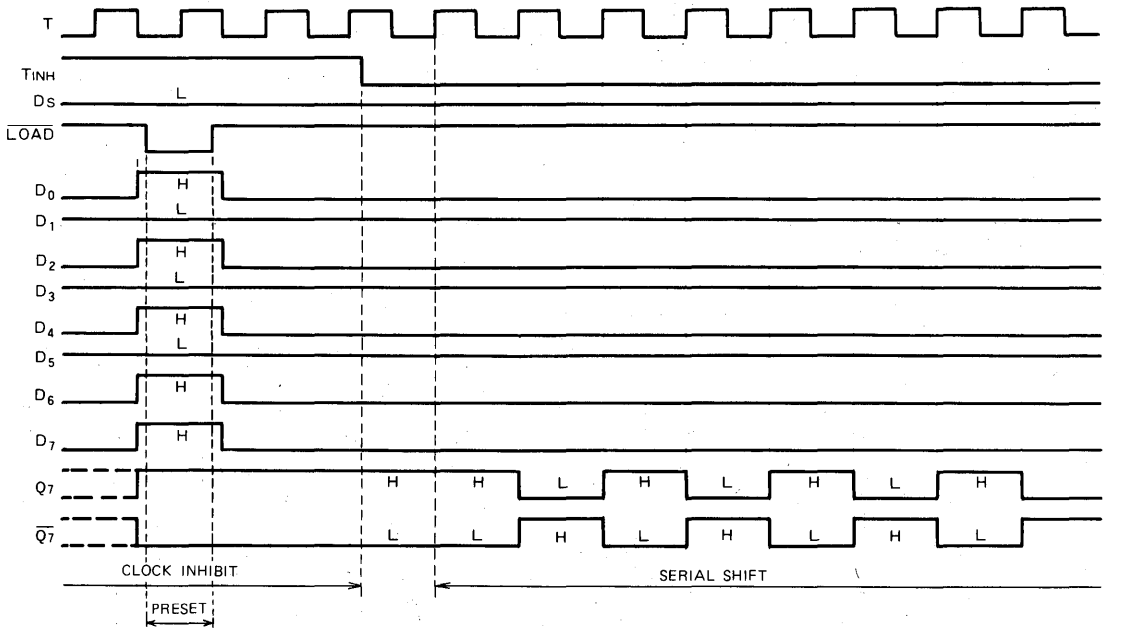
8-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER

FUNCTION TABLE (Note 1)

Inputs					Internal Outputs		Output
$\overline{LOAD}$	T_{INH}	T	D_S	$D_0 \cdots D_7$	Q_0	Q_1	Q_7
L	X	X	X	$D_0 \cdots D_7$	D_0	D_1	D_7
H	L	L	X	X	Q_0^0	Q_1^0	Q_7^0
H	L	↑	H	X	H	Q_0^0	Q_6^0
H	L	↑	L	X	L	Q_0^0	Q_6^0
H	H	X	X	X	Q_0^0	Q_1^0	Q_7^0

Note 1. X : Irrelevant
↑ : Transition from low to high (positive edge trigger)
Q^0 : Status of output before ↑ of T

TIMING DIAGRAM



MITSUBISHI ELECTRIC

8-BIT PARALLEL-IN SERIAL-OUT SHIFT REGISTER

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20 \sim +75$	°C
Tstg	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.5		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				-0.4	mA
I_{OS}	Short-circuit output current (Note 3)	$V_{CC}=5.25V$, $V_O=0V$		-20		-100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 4)			18	30	mA

* : All typical values are at $V_{CC} = 5V$, $T_a = 25°C$.

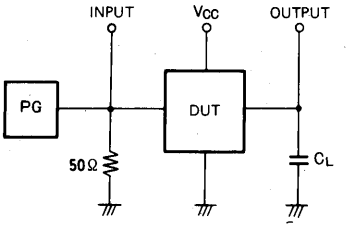
Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

3. With the outputs open, clock inhibit and clock at 4.5V, and a clock pulse applied to the $\overline{LOAD}$ input, I_{CC} is measured first with the parallel inputs at 4.5V, then with the parallel inputs grounded.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	$C_L = 15pF$ (Note 4)	25	38		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{LOAD}$ to outputs Q_7 and $\overline{Q_7}$			17	35	ns
t_{PHL}				20	35	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_7 and $\overline{Q_7}$			14	25	ns
t_{PHL}				13	25	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D_7 to output Q_7			9	25	ns
t_{PHL}				20	30	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D_7 to output $\overline{Q_7}$			16	30	ns
t_{PHL}				12	25	ns

Note 4. Measurement Circuit

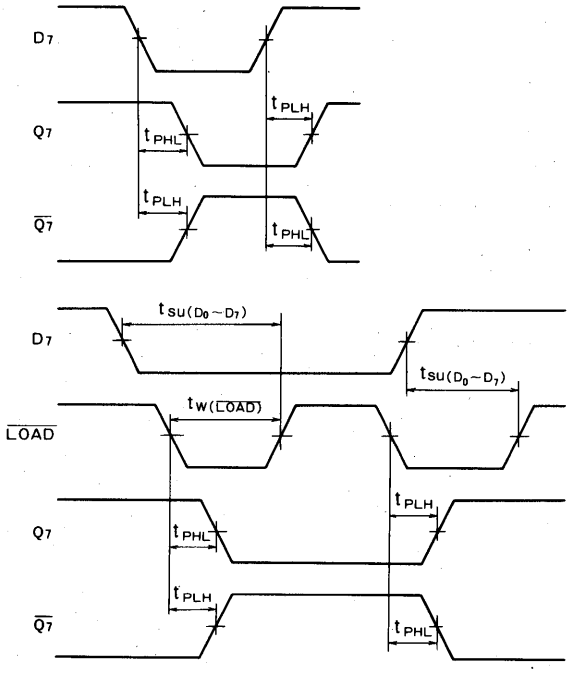


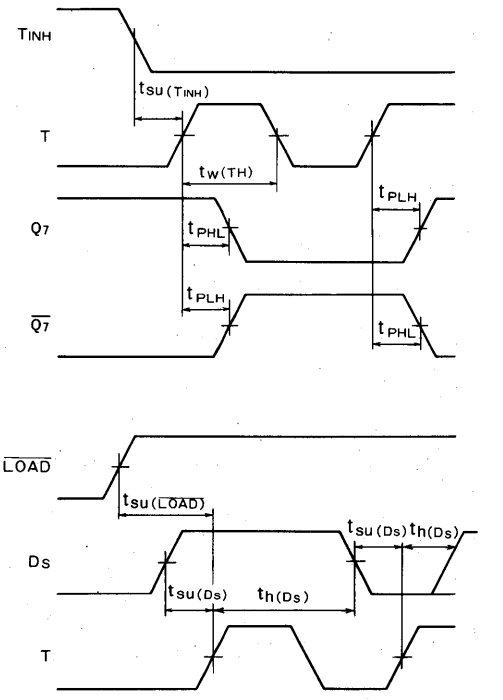
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_o = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (Vcc=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(T)}$	Clock pulse width		25	13		ns
$t_{w(\overline{LOAD})}$	$\overline{LOAD}$ low-level pulse width		15	12		ns
$t_{su(T_{INH})}$	Setup time T_{INH} to T		30	13		ns
$t_{su(D_0 \sim D_7)}$	Setup time $D_0 \sim D_7$ to $\overline{LOAD}$		10	9		ns
$t_{su(D_S)}$	Setup time D_S to T		20	8		ns
$t_{su(\overline{LOAD})}$	Setup time $\overline{LOAD}$ to T		45	0		ns
t_h	Hold time		0	0		ns

TIMING DIAGRAM (Reference level = 1.3V)





M74LS166AP

8-BIT SHIFT REGISTER

DESCRIPTION

The M74LS166AP is a semiconductor integrated circuit containing an 8-bit serial/parallel input – serial output shift register function.

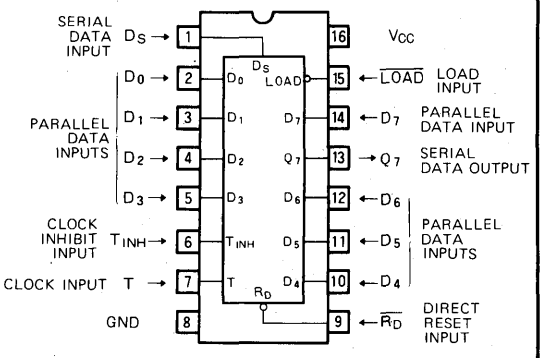
FEATURES

- Parallel-to-serial conversion
- Clock inhibit input
- Direct overriding reset
- Wide operating temperature range (T_a = –20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment

PIN CONFIGURATION (TOP VIEW)



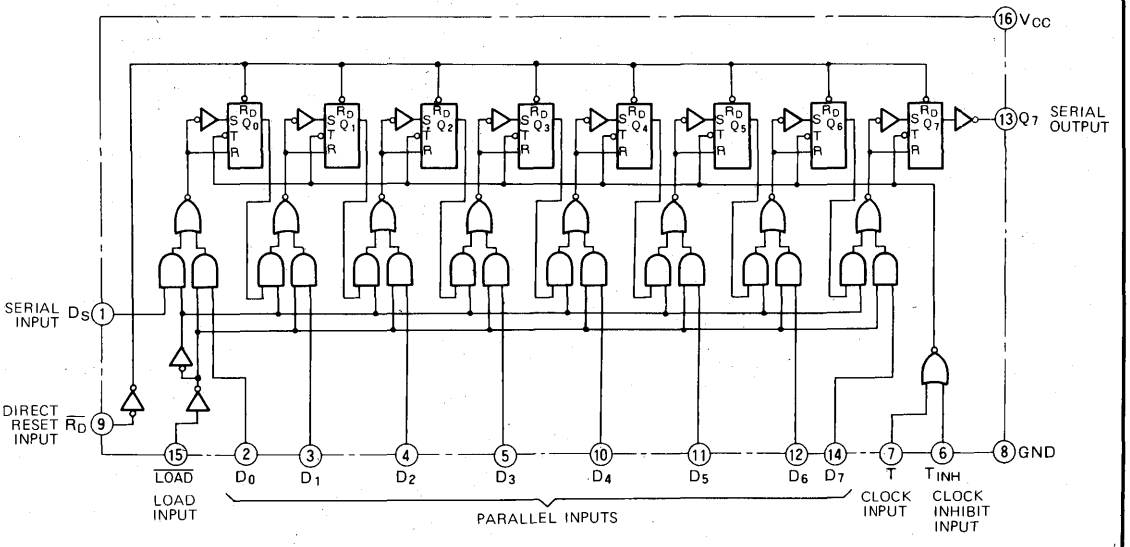
Outline 16P4

FUNCTIONAL DESCRIPTION

Parallel or serial input mode is selected via the load input $\overline{LOAD}$ signal. When $\overline{LOAD}$ is high-level, serial input enables the serial data input and couples the eight flip-flop for serial shifting with each clock pulse. Conversely, when $\overline{LOAD}$ is low-level, parallel data inputs D_0~D_7 are enabled and synchronous loading occurs on the next clock pulse. While during parallel loading, serial data flow in inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enable the clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock-inhibit input should be change to the high level only while the clock input is high. The buffered, direct reset input $\overline{R_D}$ overrides all other inputs, including the clock, and sets all flip-flop to zero.

M74LS166AP has been improved to resolve timing problems on $\overline{LOAD}$ input signal switching that occurred in the M74LS166P. Serial output Q7 has also been provided with a buffer to reduce noise, resulting in a change in specifications.

BLOCK DIAGRAM



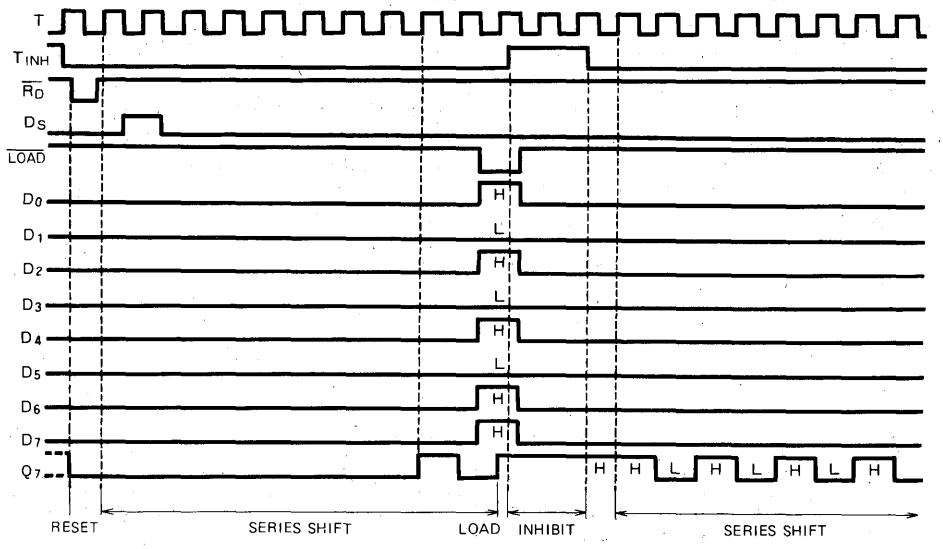
8-BIT SHIFT REGISTER

FUNCTION TABLE (Note 1)

t_n						t_{n+1}		
$\overline{R_D}$	$\overline{LOAD}$	T_{INH}	T	Ds	Parallel Inputs	Internal outputs		Q_7
					$D_0 \cdots D_7$	Q_0	Q_1	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{00}	Q_{10}	Q_{70}
H	L	L	↑	X	$D_0 \cdots D_7$	D_0	D_1	D_7
H	H	L	↑	H	X	H	Q_{0n}	Q_{6n}
H	H	L	↑	L	X	L	Q_{0n}	Q_{6n}
H	X	H	↑	X	X	Q_{00}	Q_{1n}	Q_{70}

Note 1. X : Irrelevant
↑ : Transition from low to high (positive edge trigger)
$D_0 \sim D_7$: Indicates status prior to clock pulse at input D_0 thru D_7.
$Q_{00} \ldots Q_{70}$: Indicates initial status of output Q_0 thru Q_7.
$Q_{0n} \ldots Q_{7n}$: Indicates status of Q_0 thru Q_7 immediately prior to clock input
t_{n+1} : Bit time after one clocking transition.

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level output	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.5		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
			$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$		− 20		−100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 3)			20	32	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

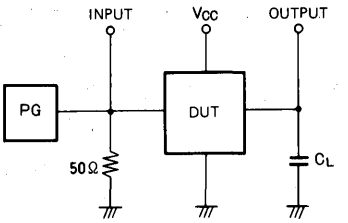
Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

3. With all outputs open, 4.5V applied to the serial input and all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to clock.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L=15pF$ (Note 5)	25	38		MHz
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q_7			18	30	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output Q_7			10	20	ns
t_{PHL}				12	25	ns

Note 4. Measurement circuit

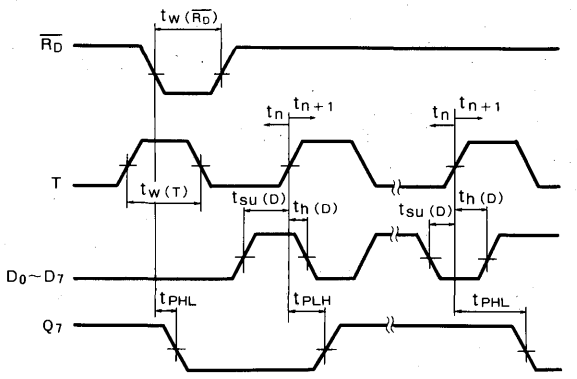


(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) C_L includes jig and probe capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(T)}$	Clock pulse width		20	14		ns
$t_{w(\overline{R_D})}$	Reset pulse width		20	8		ns
$t_{su(D)}$	Setup time D_S, D_0~D_7 to T		20	12		ns
$t_{su(\overline{LOAD})}$	Setup time $\overline{LOAD}$ to T		30	12		ns
t_h	Hold time all inputs to T		0	−10		ns

TIMING DIAGRAM (Reference level = 1.3V)



TEST CONDITION TABLE

Data input for test	$\overline{LOAD}$	Output tested	Bit time
D_7	0V	Q_7	t_{n+1}
D_S	4.5V	Q_7	t_{n+8}

MITSUBISHI ELECTRIC

M74LS170P

4-BY-4 REGISTER FILE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS170P is a semiconductor integrated circuit containing a 4-word by 4-bit register file function with open collector outputs.

FEATURES

- Separate read and write addresses for simultaneous data
- Read and write enable inputs provided
- Easy expansion of memory capacity using enable inputs
- Usable in AND-Tie connection (open collector outputs)
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

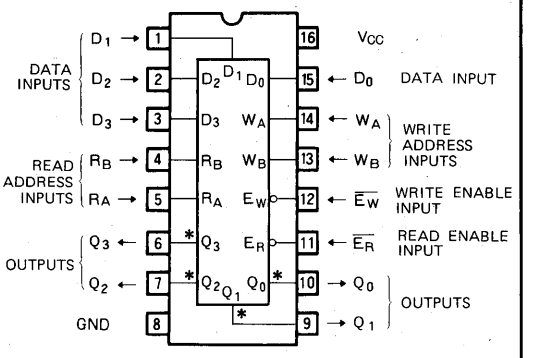
FUNCTIONAL DESCRIPTION

This device contains 16 D-type latches as memory elements. Separate read and write inputs, both address and enable, allow simultaneous read and write operation, thereby enabling readout of other word contents during writing and writing into other words during readout resulting in increased speed. Open collector outputs make it possible to

The open collector outputs permit wire-AND connections for 256 outputs and expansion up to 1024 words.

M74LS170P has the same functions and pin connections as M74LS670P but the latter is provided with 3-state outputs.

PIN CONFIGURATION (TOP VIEW)



* : OPEN COLLECTOR OUTPUT

Outline 16 P4

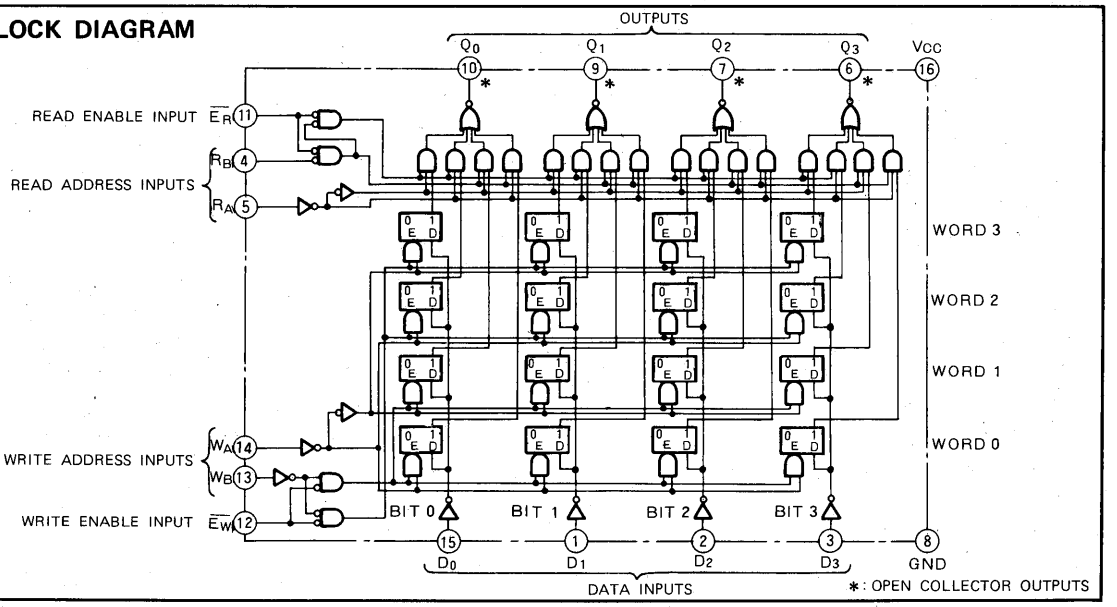
Writing Method

Writing into the bits is performed by specifying the words with address inputs W_A and W_B and by applying the data to data inputs D_0, D_1, D_2 and D_3. The write enable input $\overline{E_W}$ is set low. No writing is performed when $\overline{E_W}$ is set high.

Readout Method

When the words are specified by read address inputs R_A and R_B, the contents of the stored bits appear in outputs Q_0, Q_1, Q_2 and Q_3. Read enable input $\overline{E_R}$ is set low. When $\overline{E_R}$ is set high, all the outputs are set high.

BLOCK DIAGRAM



*: OPEN COLLECTOR OUTPUTS

4-BY-4 REGISTER FILE WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

Writing Method

W_A	W_B	$\overline{E_W}$	Word 0	Word 1	Word 2	Word 3
X	X	H	Q^0	Q^0	Q^0	Q^0
L	L	L	Q=D	Q^0	Q^0	Q^0
H	L	L	Q^0	Q=D	Q^0	Q^0
L	H	L	Q^0	Q^0	Q=D	Q^0
H	H	L	Q^0	Q^0	Q^0	Q=D

Readout Method

R_A	R_B	$\overline{E_R}$	Q_0	Q_1	Q_2	Q_3
X	X	H	H	H	H	H
L	L	L	W_0B_0	W_0B_1	W_0B_2	W_0B_3
H	L	L	W_1B_0	W_1B_1	W_1B_2	W_1B_3
L	H	L	W_2B_0	W_2B_1	W_2B_2	W_2B_3
H	H	L	W_3B_0	W_3B_1	W_3B_2	W_3B_3

Note 1 Q^0 : No change in word contents.
Q=D : Data input contents are written into specified word.
W_XB_Y : Indicates word X and bit Y contents
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O = 5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		4	mA
		V_{OL}≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
I_{OH}	High-level output current		V_{CC}=4.75V, V_I=0.8V, V_I=2V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V	I_{OL}=4mA		0.25	0.4	V
				I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	$\overline{E_R}$, $\overline{E_W}$	V_{CC}=5.25V, V_I=2.7V				40	μA
		Other inputs					20	
		$\overline{E_R}$, $\overline{E_W}$	V_{CC}=5.25V, V_I=10V				0.2	mA
		Other inputs					0.1	
I_{IL}	Low-level input current	$\overline{E_R}$, $\overline{E_W}$	V_{CC}=5.25V, V_I=0.4V				−0.8	mA
		Other inputs					−0.4	
I_{CC}	Supply current		V_{CC}=5.25V (Note 2)			25	40	mA

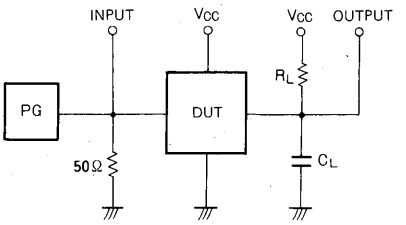
* : All typical values are at V_{CC}=5V, T_a=25°C.
Note 2: I_{CC} is measured with W_A, W_B, R_A and R_B at 0V and with D_0~D_4, $\overline{E_R}$ and $\overline{E_W}$ at 4.5V.

4-BY-4 REGISTER FILE WITH OPEN COLLECTOR OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E_R}$ to outputs Q_0, Q_1, Q_2, Q_3	R_L = 2 kΩ, C_L = 15 pF (Note 3)		13	30	ns
t_{PHL}				11	30	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs R_A, R_B to outputs Q_0, Q_1, Q_2, Q_3			16	40	ns
t_{PHL}				15	40	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E_W}$ to outputs Q_0, Q_1, Q_2, Q_3			16	45	ns
t_{PHL}				16	40	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_0, D_1, D_2, D_3 to outputs Q_0, Q_1, Q_2, Q_3			15	45	ns
t_{PHL}				15	35	ns

Note 3: Measurement circuit



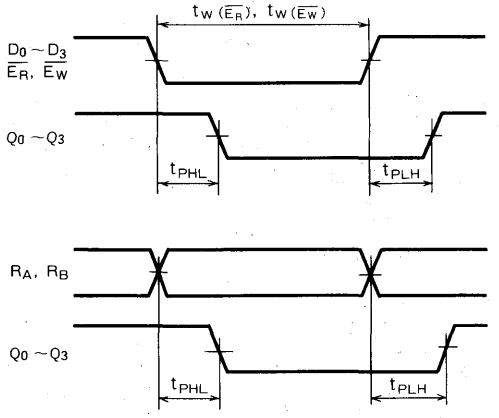
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance

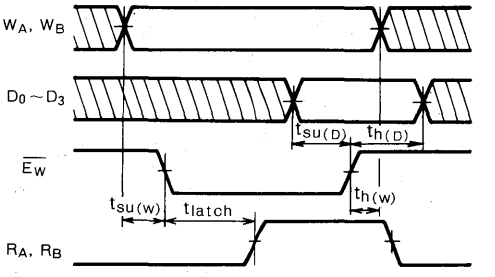
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{E_R})}$	Read enable input $\overline{E_R}$ pulse width		25	9		ns
$t_{W(\overline{E_W})}$	Wright enable input $\overline{E_W}$ pulse width		25	9		ns
$t_{su(D)}$	D_0~D_3 setup time with respect to $\overline{E_W}$		10	5		ns
$t_{su(W)}$	W_A, W_B setup time with respect to $\overline{E_W}$		15	− 2		ns
$t_{h(D)}$	D_0~D_3 hold time with respect to $\overline{E_W}$		15	0		ns
$t_{h(W)}$	W_A, W_B hold time with respect to $\overline{E_W}$		5	− 2		ns
t_{latch}	D_0~D_3 latch time (note 4)		25	5		ns

Note 4: t_{LATCH} is the time required for storage when data is changed.

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS173AP

4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS173AP is a semiconductor integrated circuit containing a 4-bit register with 3-state outputs.

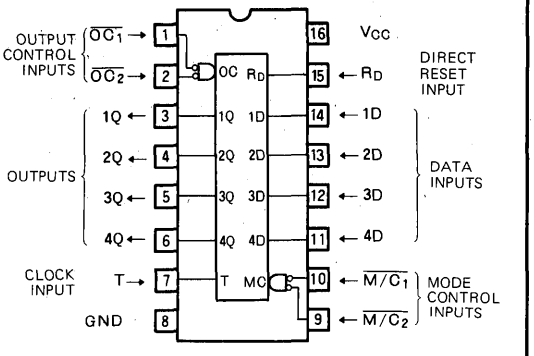
FEATURES

- Data can be held irrespective of number of clock pulses
- Data are non-destructible with 3-state outputs
- Positive edge-triggering
- Direct reset input provided
- Easy bit expansion
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



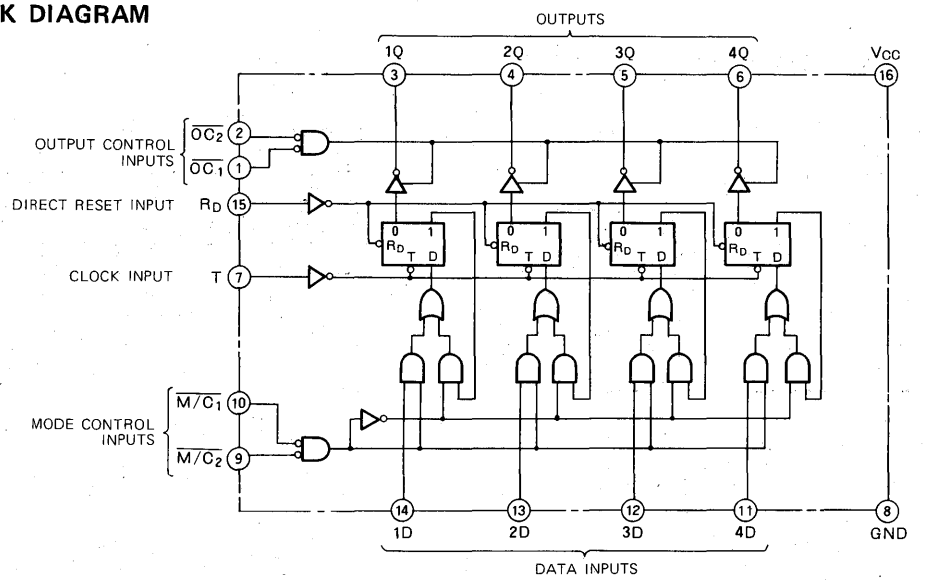
Outline 16P4

FUNCTIONAL DESCRIPTION

This device contains 4 edge-triggered D-type flip-flop circuits and direct reset input R_D and clock input T common to all circuits. When T changes from low to high, the information of data inputs 1D ~ 4D immediately before the change appears in outputs 1Q ~ 4Q respectively in accordance with the function table.

When R_D is set high with mode control inputs $\overline{M/C_1}$ and $\overline{M/C_2}$ low, all the flip-flop outputs are low irrespective of the other inputs. When $\overline{M/C_1}$ or $\overline{M/C_2}$ is high, 1Q ~ 4Q hold the status established when $\overline{M/C_1}$ and $\overline{M/C_2}$ are low, irrespective of the other signals. When $\overline{OC_1}$ or $\overline{OC_2}$ is high, 1Q ~ 4Q are all put in the high-impedance state. In this case, the internal flip-flop status does not change because of the $\overline{OC_1}$ and $\overline{OC_2}$ input change. For use as a D-type flip-flop, set $\overline{M/C_1}$, $\overline{M/C_2}$, $\overline{OC_1}$ and $\overline{OC_2}$ all low.

BLOCK DIAGRAM



4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

R_D	T	$\overline{M/C_1}$	$\overline{M/C_2}$	D	Q
H	X	X	X	X	L
L	L	X	X	X	Q^0
L	↑	H	X	X	Q^0
L	↑	X	H	X	Q^0
L	↑	L	L	L	L
L	↑	L	L	H	H

Note 1 High-impedance state when $\overline{OC_1}$ and/or $\overline{OC_2}$ are high.
↑ : Transition from low to high (positive edge trigger)
X : Irrelevant
Q^0 : Level of Q before the indicated steady-state input conditions were established

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-2.6mA$		2.4	3.1		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=12mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$	$I_{OL}=24mA$		0.35	0.5	V
I_{OZH}	Off-state high-level output current	$V_{CC}=5.25V$, $V_I=2V$, $V_O=2.7V$				20	μA
I_{OZL}	Off-state low-level output current	V_{CC} 5.25V, $V_I=2V$, $V_O=0.4V$				−20	μA
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$		−30		−130	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 3)			17	30	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25°C$
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured after $\overline{M/C_1}$, $\overline{M/C_2}$, 1D 4D and $\overline{OC_2}$ have been set to 0V, T and $\overline{OC_1}$ to 4.5V and R_D from 0V to 4.5V.

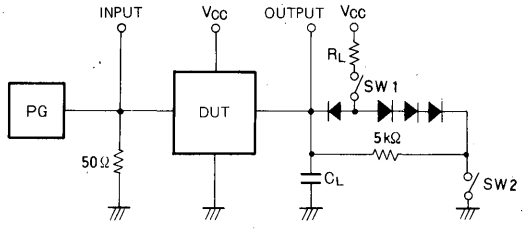
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L=45pF (Note 4)	30	35		MHz
t_{PHL}	High-to-low-level output propagation time, from input R_D to output Q			21	35	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time from input T to output			20	25	ns
t_{PHL}				26	30	ns
t_{PZH}	Output enable time to high-level	C_L=45pF, R_L=667Ω (Note 4)		14	23	ns
t_{PZL}	Output enable time to low-level			15	27	ns
t_{PHZ}	Output disable time from high-level	C_L=5pF, R_L=667Ω (Note 4)		11	17	ns
t_{PLZ}	Output disable time from low-level			9	17	ns

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(T)}$	Clock input T pulse width		20	4		ns
$t_{su(D)}$	Setup time 1D~4D to T		17	3		ns
$t_{h(D)}$	Hold time 1D~4D to T		6	3		ns
$t_{su(\overline{M/C})}$	Setup time $\overline{M/C_1}$, $\overline{M/C_2}$ to T		35	20		ns
$t_{h(\overline{M/C})}$	Hold time $\overline{M/C_1}$, $\overline{M/C_2}$ to T		0	−12		ns
$t_{w(R_D)}$	Direct reset R_D pulse width		20	10		ns
t_{rec}	Recovery time R_D to T		15	12		ns

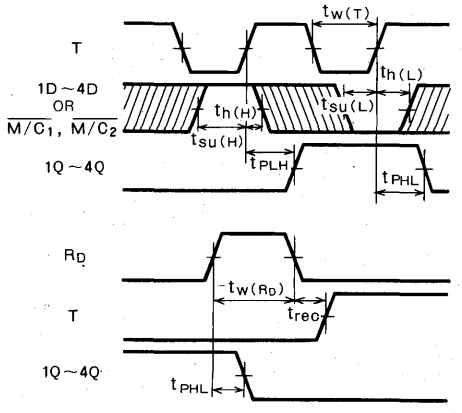
Note 4: Measurement circuit

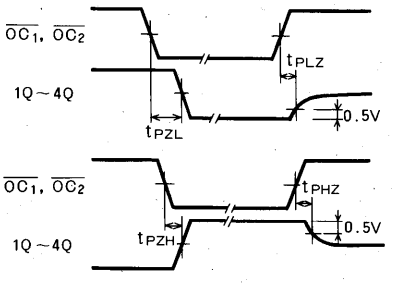


Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = 3V_{P-P}, Z_O = 50Ω.
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns).
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

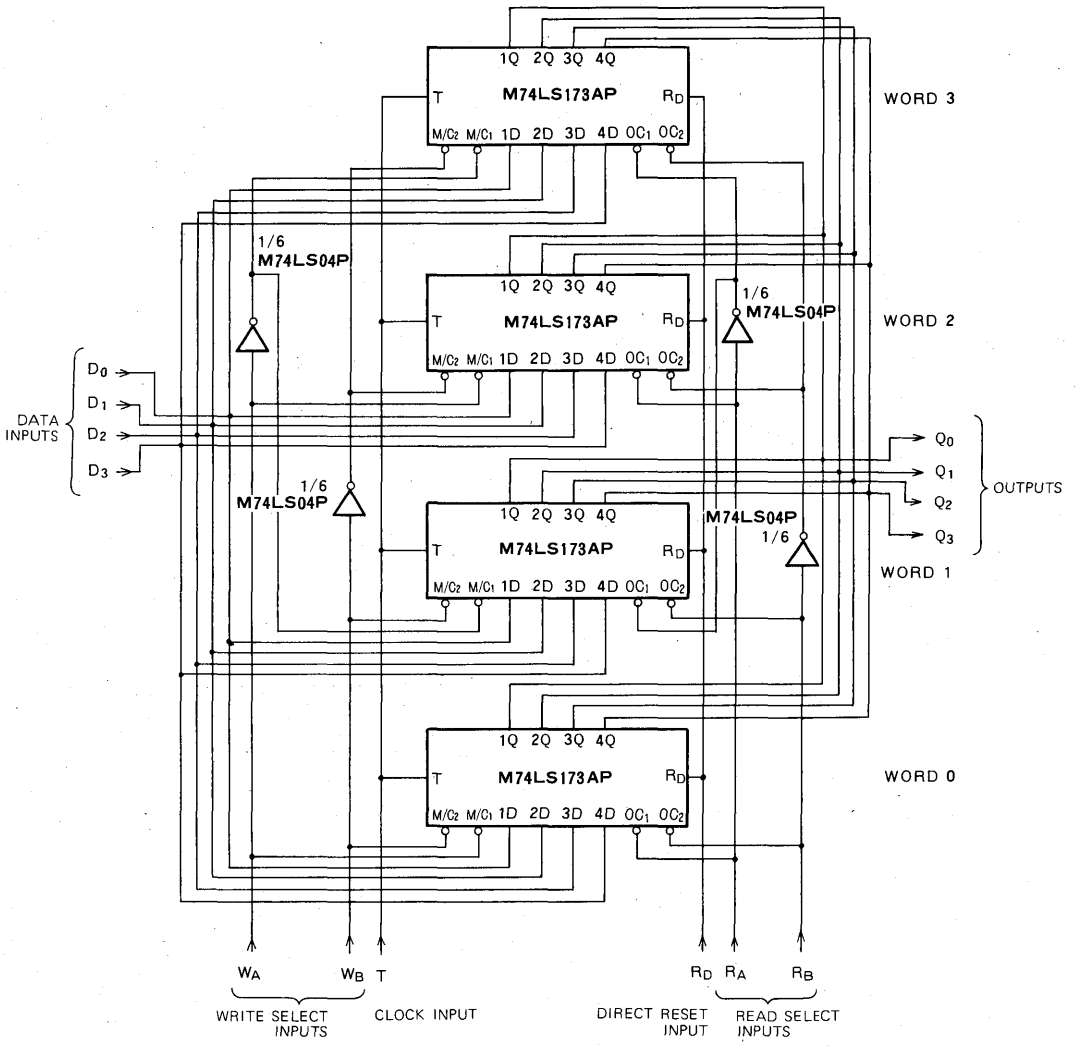




4-BIT D-TYPE REGISTER WITH 3-STATE OUTPUT

APPLICATION EXAMPLE

Shown below is a schematic of a 4-bit x 4-word register file using the M74LS173AP.



Writing method

W_B	W_A	WORD			
		0	1	2	3
L	L	Q=D	Q^0	Q^0	Q^0
L	H	Q^0	Q=D	Q^0	Q^0
H	L	Q^0	Q^0	Q=D	Q^0
H	H	Q^0	Q^0	Q^0	Q=D

Readout method

R_B	R_A	Q_0	Q_1	Q_2	Q_3
L	L	W_0D_0	W_0D_1	W_0D_2	W_0D_3
L	H	W_1D_0	W_1D_1	W_1D_2	W_1D_3
H	L	W_2D_0	W_2D_1	W_2D_2	W_2D_3
H	H	W_3D_0	W_3D_1	W_3D_2	W_3D_3

M74LS174P

HEX D-TYPE FLIP FLOPS WITH RESET

DESCRIPTION

The M74LS174P is a semiconductor integrated circuit containing 6 D-type edge-triggered flip-flop circuits with common clock input T and direct reset input $\overline{R_D}$ as well as discrete data input D.

FEATURES

- Positive edge-triggering
- Common clock and direct reset inputs for all 6 circuits
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = -20 ~ +75°C)

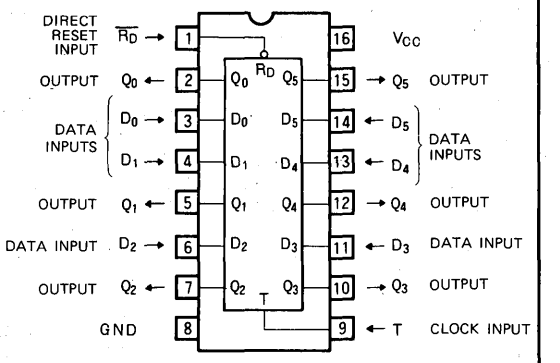
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When T changes from low to high, the D signal immediately before the change appears in the output Q in accordance with the function table. When $\overline{R_D}$ is low, all Q are low, regardless of the status of the other input signals. For use as a D-type flip-flop, keep $\overline{R_D}$ high.

PIN CONFIGURATION (TOP VIEW)



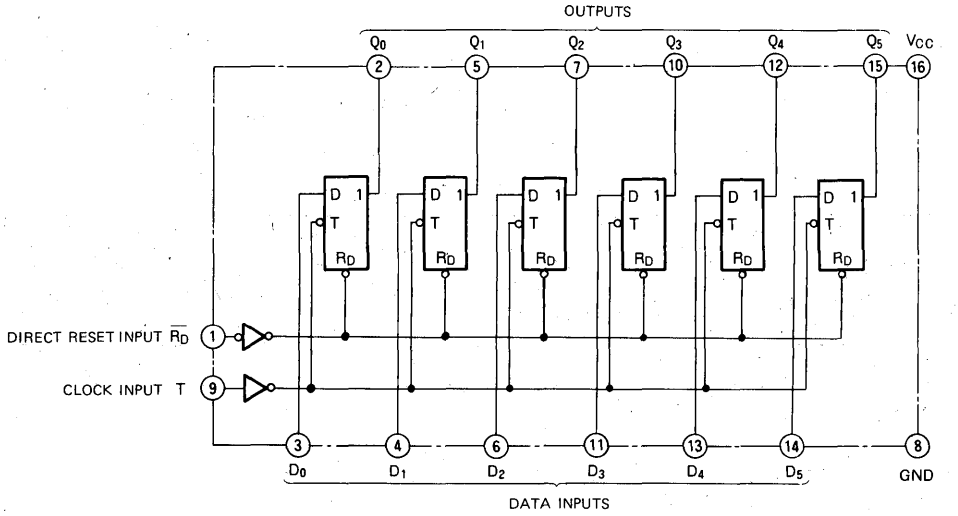
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{R_D}$	T	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q^0

Note 1: ↑ : transition from low to high level
Q^0 : level of Q before the indicated steady-state input conditions were established
X : irrelevant

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

HEX D-TYPE FLIP FLOPS WITH RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75℃$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20 \sim +75$	℃
Tstg	Storage temperature range		$-65 \sim +150$	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75℃$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75℃$, unless otherwise noted)

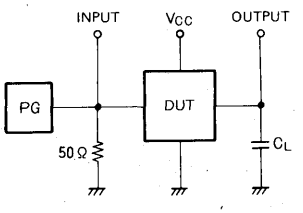
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current Note 2	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 3)			16	26	mA

* : All typical values are at $V_{CC}=5V$, $Ta=25°C$.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with D, $\overline{R_D}$ inputs at 4.5V and a momentary ground, then 4.5V, applied to T input

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25℃$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	$C_L=15pF$ (Note 4)	30	47		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output Q			10	30	ns
t_{PHL}				10	30	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q			11	35	ns

Note 4: Measurement circuit

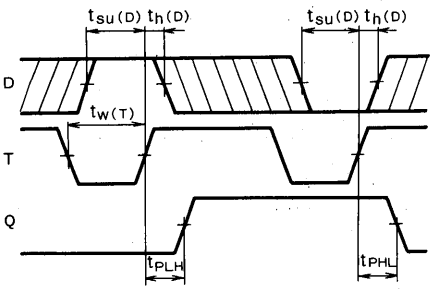


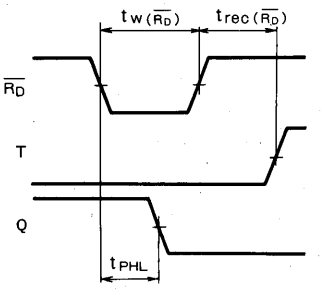
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}= 5 V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(T)}$	Clock input T pulse width		20	4		ns
$t_{w(\overline{RD})}$	Reset input $\overline{R_D}$ pulse width		20	6		ns
$t_{su(D)}$	Setup time D to T		20	2		ns
$t_{h(D)}$	Hold time D to T		5	0		ns
$t_{rec(\overline{RD})}$	Recovery time $\overline{R_D}$ to T		25	5		ns

TIMING DIAGRAM (Reference level = 1.3V)

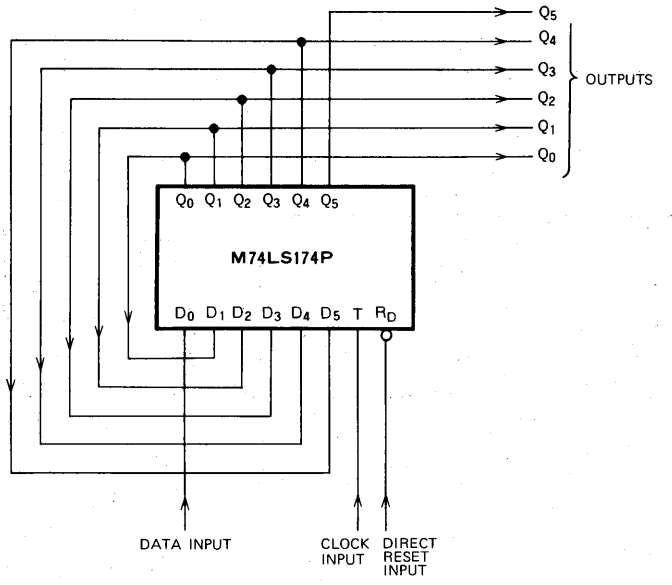




Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

6-bit shift register



MITSUBISHI ELECTRIC

M74LS175P

QUADRUPLE D-TYPE FLIP FLOP WITH RESET

DESCRIPTION

The M74LS175P is a semiconductor integrated circuit containing 4 positive edge-triggered D-type flip-flops with common clock input T and direct reset input $\overline{R_D}$ and discrete data inputs D.

FEATURES

- Positive edge-triggering
- Clock and direct reset inputs common to 4 circuits
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a = −20~+75°C)

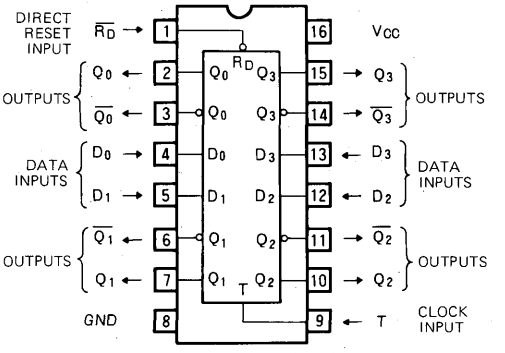
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When T changes from low to high, the D signal immediately before the change emerges in outputs Q and $\overline{Q}$ in accordance with the function table. By setting $\overline{R_D}$ low, all the Q and $\overline{Q}$ outputs are set low and high, respectively, irrespective of the status of the other inputs signals. For use as a D-type flip-flop, $\overline{R_D}$ must be kept in high.

PIN CONFIGURATION (TOP VIEW)



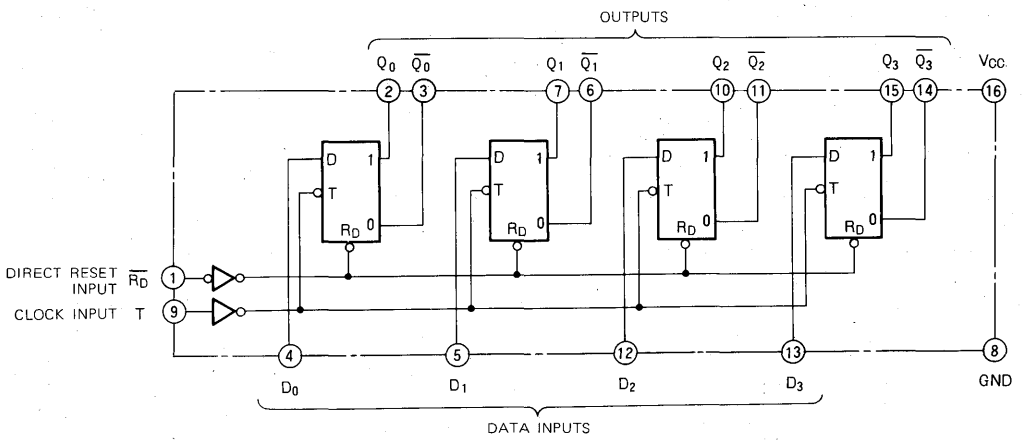
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{R_D}$	T	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

Note 1 X : Irrelevant
↑ : Transition from low to high level (positve edge trigger)
Q_0 : Level of Q before the indicated steady-state input conditions were established.

BLOCK DIAGRAM



QUADRUPLE D-TYPE FLIP FLOP WITH RESET

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_{OH}≧2.7V	0		−400	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		4	mA
		V_{OL}≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
		V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 3)			11	18	mA

* : All typical values are at V_{CC}=5V, T_a=25°C

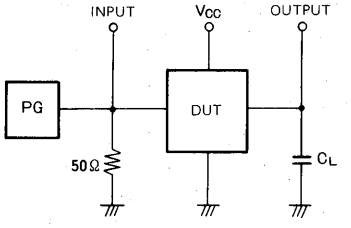
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with 4.5V applied to D and $\overline{R_D}$ after T is set to 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L=15pF (Note 4)	30	50		ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from T to Q, $\overline{Q}$			10	25	ns
t_{PHL}				12	25	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from $\overline{R_D}$ to Q, $\overline{Q}$			15	30	ns
t_{PHL}				19	30	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω.

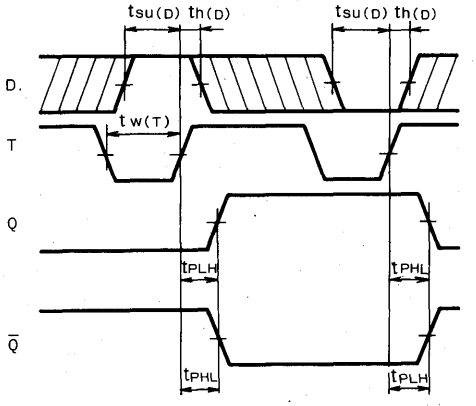
(2) C_L includes probe and jig capacitance.

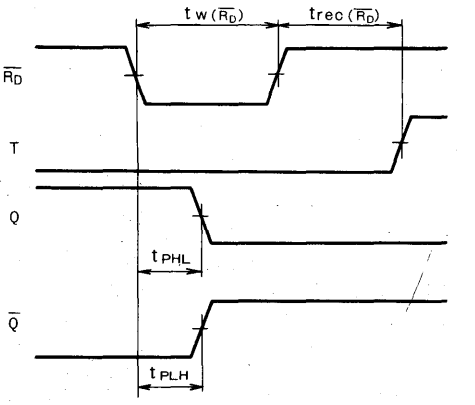
QUADRUPLE D-TYPE FLIP FLOP WITH RESET

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(T)}$	Clock input T pulse width		20	4		ns
$t_{W(\overline{R_D})}$	Direct reset input pulse width		20	7		ns
$t_{SU(D)}$	Setup time high to T		20	2		ns
$t_{h(D)}$	Hold time high to T		5	0		ns
$t_{rec(\overline{R_D})}$	Recovery time for direct reset input		25	5		ns

TIMING DIAGRAM (Reference level = 1.3V)

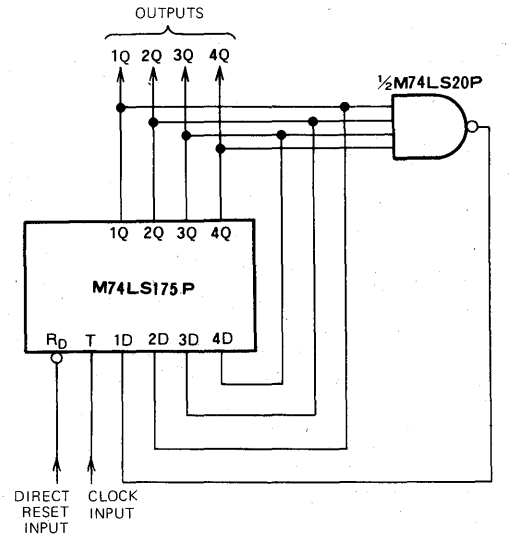


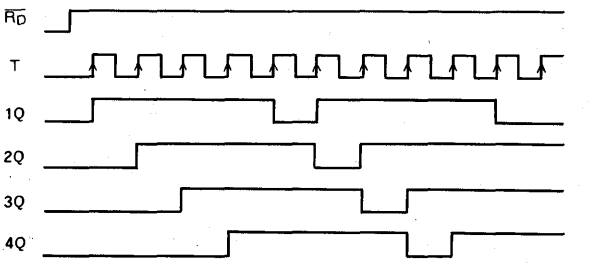


Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Timing pulse generator





M74LS190P

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

DESCRIPTION

The M74LS190P is a semiconductor integrated circuit containing a decade up/down counter function with up/down control and preset inputs.

FEATURES

- Up/down switching with up/down control input
- Asynchronous preset input provided
- Enable input provided
- Easy cascade connection possible
- High-speed counting (f_{max}= 38MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

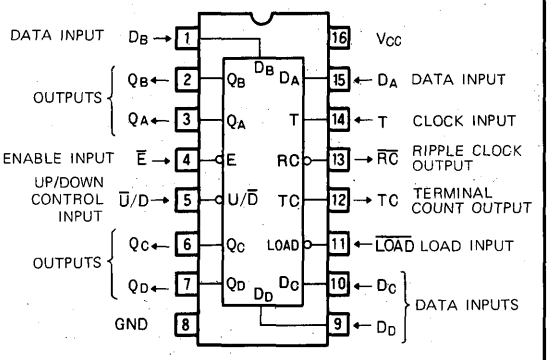
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When enable input $\overline{E}$ is low, load input $\overline{LOAD}$ is high and the count pulses are applied to clock input T, the number of count pulses appear as a BCD code in the outputs Q_A, Q_B, Q_C and Q_D in synchronization with the count pulses. When the up/down control input $\overline{U}/D$ is made low, count-up begins and when made high, count-down begins. Counting is performed when T changes from low to high.

Presetting is performed regardless of the count pulses and by applying the data to data inputs D_A, D_B, D_C and D_D and by setting $\overline{LOAD}$ low, the D_A, D_B, D_C and D_D signals appear in outputs Q_A, Q_B, Q_C and Q_D irrespective of the status of the other inputs and the count can be preset. Counting proceeds as per the status transition diagram with presetting to a numerical value of 10_2 or higher.

PIN CONFIGURATION (TOP VIEW)

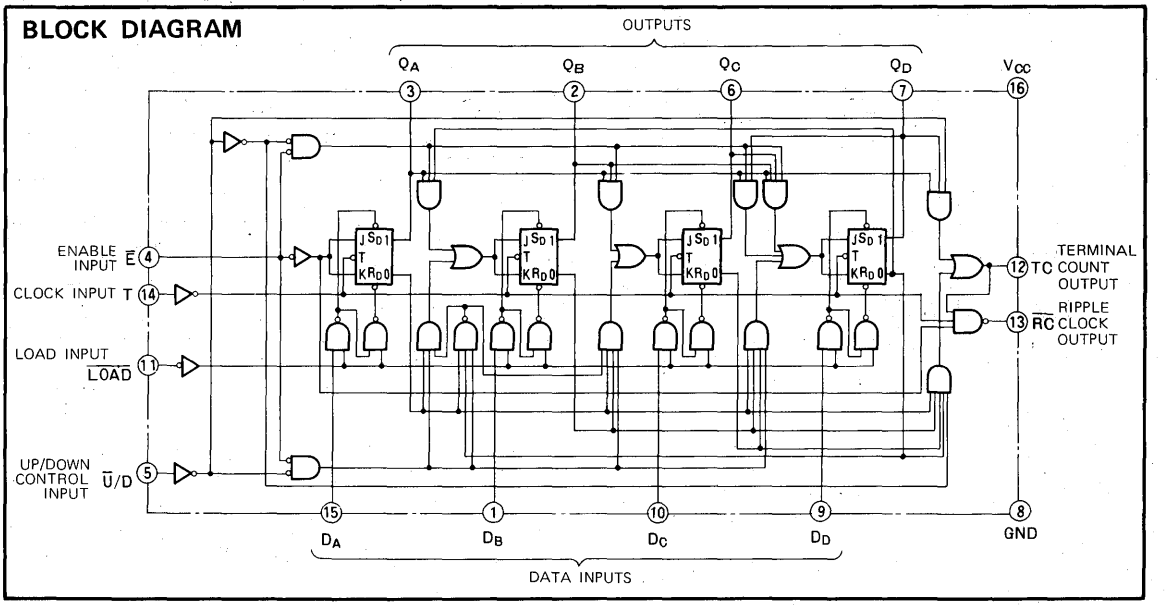


Outline 16P4

High appears in the terminal count output TC during count-up while 9_2 appears in Q_A, Q_B, Q_C and Q_D and during count-down while 0_2 appears. Low appears in the ripple clock output $\overline{RC}$ only when $\overline{E}$ and T are low and 9_2 appears in outputs Q_A, Q_B, Q_C and Q_D during count-up or 0_2 appears in the outputs during count-down. $\overline{E}$, TC and $\overline{RC}$ are used when cascade-connecting the counter. (Refer to application examples.)

$\overline{E}$ can be changed from high to low irrespective of the status of T but when changed from low to high, T must be high. Perform the change for $\overline{U}/D$ when T is high.

BLOCK DIAGRAM



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SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

FUNCTION TABLE (Note 1)

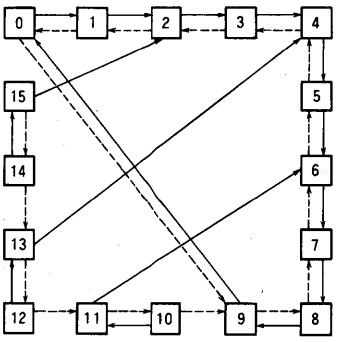
$\overline{LOAD}$	$\overline{E}$	$\overline{U}/D$	T	Q_A	Q_B	Q_C	Q_D
L	X	X	X	D_A	D_B	D_C	D_D
H	L	L	↑	Count-up			
H	L	H	↑	Count-down			
H	H	X	X	Inhibit			

Note 1. ↑ : Transition from low to high
X : Irrelevant

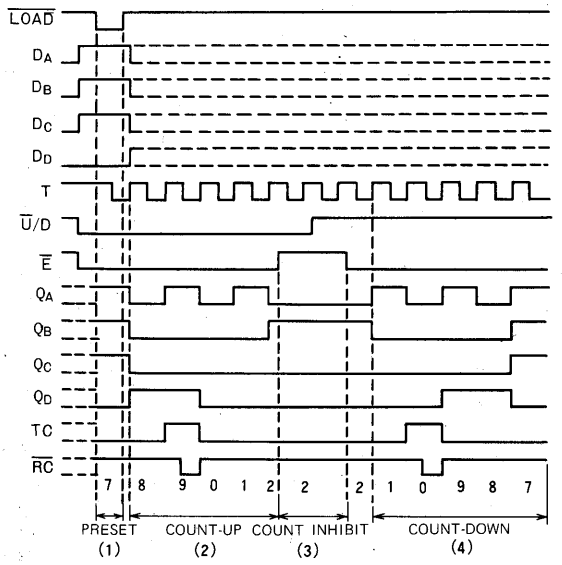
$\overline{E}$	TC(1)	T	$\overline{RC}$
L	H	L	L
L	H	H	H
H	X	X	H
X	L	X	H

TC is the output but the signal generated internally by the following logical expression.
$TC = Q_A \cdot Q_D \cdot (\overline{U}/D)$ ..... Count-up
$TC = \overline{Q_A} \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot \overline{Q_D} \cdot (\overline{U}/D)$ ..... Count-down

STATE DIAGRAM



OPERATION TIMING DIAGRAM



Details of timing diagram
(1) Preset to 13
(2) Count-up 8, 9, 0, 1, 2
(3) Count inhibit
(4) Count-down 1, 0, 9, 8, 7

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

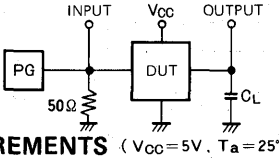
Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$T, \overline{LOAD}, \overline{U}/D, D_A \sim D_D$	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{E}$					60	
		$T, \overline{LOAD}, \overline{U}/D, D_A \sim D_D$	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{E}$					0.3	
I_{IL}	Low-level input current	$T, \overline{LOAD}, \overline{U}/D, D_A \sim D_D$	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$\overline{E}$					−1.2	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 3)			20	35	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3. I_{CC} is measured with all the inputs at 0V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum clock freqency	$C_L=15pF$ (Note 4)	20	40		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, input $\overline{LOAD}$ to outputs Q_A, Q_B, Q_C, Q_D			19	33	ns
t_{PHL}				25	50	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B, D_C, D_D to outputs Q_A, Q_B, Q_C, Q_D			11	32	ns
t_{PHL}				25	40	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output $\overline{RC}$			11	20	ns
t_{PHL}				11	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				14	36	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output TC			20	42	ns
t_{PHL}				24	52	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{U}/D$ to output $\overline{RC}$			22	45	ns
t_{PHL}				20	45	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{U}/D$ to output TC			15	33	ns
t_{PHL}				15	33	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E}$ to output $\overline{RC}$			10	33	ns
t_{PHL}				11	33	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$
(2) C_L includes probe and jig capacitance

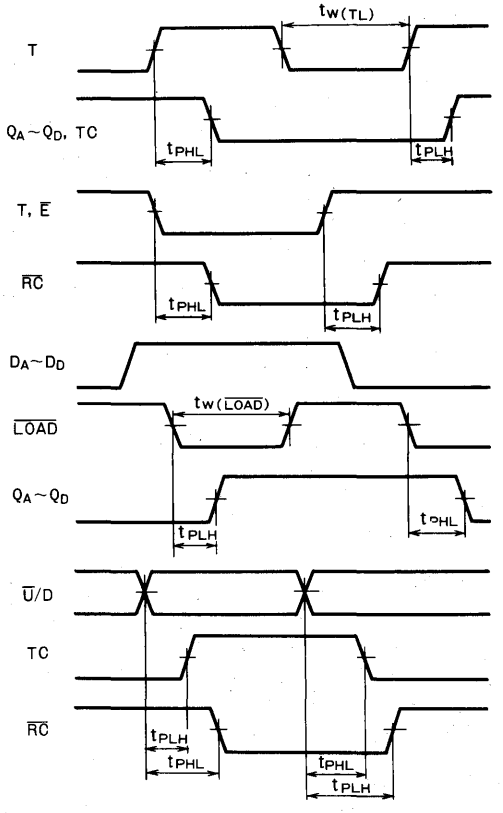
TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

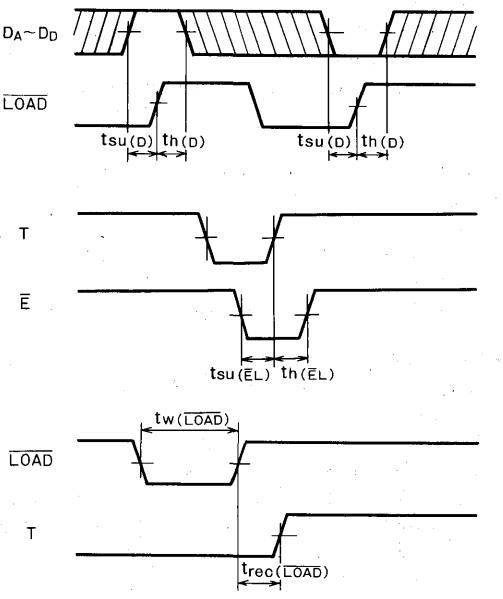
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{W(TL)}$	Clock input T low pulse width		25	9		ns
$t_{W(\overline{LOAD})}$	Load $\overline{LOAD}$ pulse width		35	10		ns
tr	Clock pulse rise time			2000	100	ns
$t_{SU(D)}$	Setup time $D_A \sim D_D$ to $\overline{LOAD}$		20	9		ns
$t_{SU(\overline{EL})}$	Setup time $\overline{E}$ low to T		40	24		ns
$t_{h(D)}$	Hold time $D_A \sim D_D$ to $\overline{LOAD}$		5	0		ns
$t_{h(\overline{EL})}$	Hold time $\overline{E}$ low to T		5	2		ns
$t_{rec(\overline{LOAD})}$	Recovery time $\overline{LOAD}$ to T		20	16		ns

MITSUBISHI ELECTRIC

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

TIMING DIAGRAM (Reference level = 1.3V)



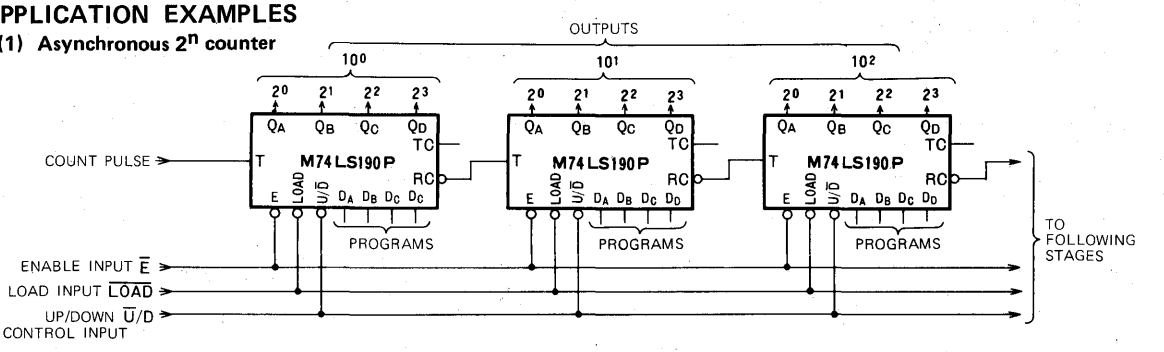


Note 5. The shaded areas indicate when the input is permitted to change for predictable output performance.

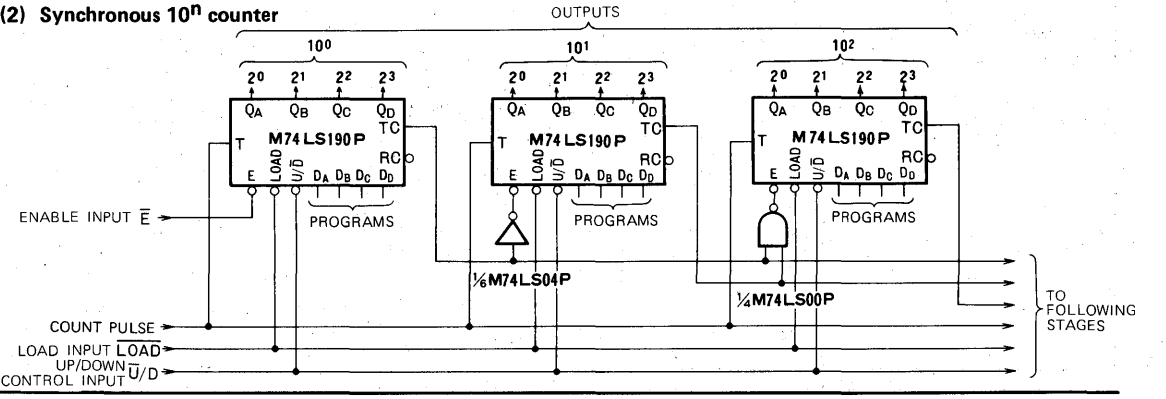
Note 6. The shaded area with the arrows indicate the direction of when the input is permitted to change.

APPLICATION EXAMPLES

(1) Asynchronous 2^n counter



(2) Synchronous 10^n counter



M74LS191P

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

DESCRIPTION

The M74LS191P is a semiconductor integrated circuit containing a synchronous 4-bit binary (hexadecimal) counter function with up/down control and preset inputs.

FEATURES

- Up/down switching with up/down control inputs
- Asynchronous preset input provided
- Enable input provided
- Easy cascade connection possible
- High-speed counting (f_{max}= 40MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

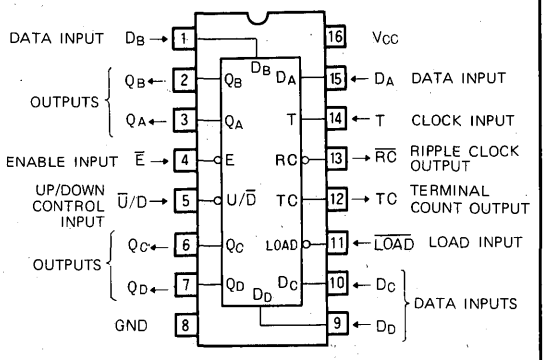
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When enable input E is low, load input $\overline{LOAD}$ is high and the count pulses are applied to clock input T, the number of count pulses appears as 4-bit pure binary code in the outputs Q_A, Q_B, Q_C and Q_D in synchronization with the count pulses. When the up/down control input $\overline{U}/D$ is made low, count-up begins and when made high, count-down begins. Counting is performed when T changes from low to high.

Presetting is performed regardless of the count pulses and by applying the data to data inputs D_A, D_B, D_C and D_D and by setting $\overline{LOAD}$ low, the D_A, D_B, D_C and D_D signals appear in outputs Q_A, Q_B, Q_C and Q_D irrespective of the status of the other inputs and the counter can be preset.

PIN CONFIGURATION (TOP VIEW)

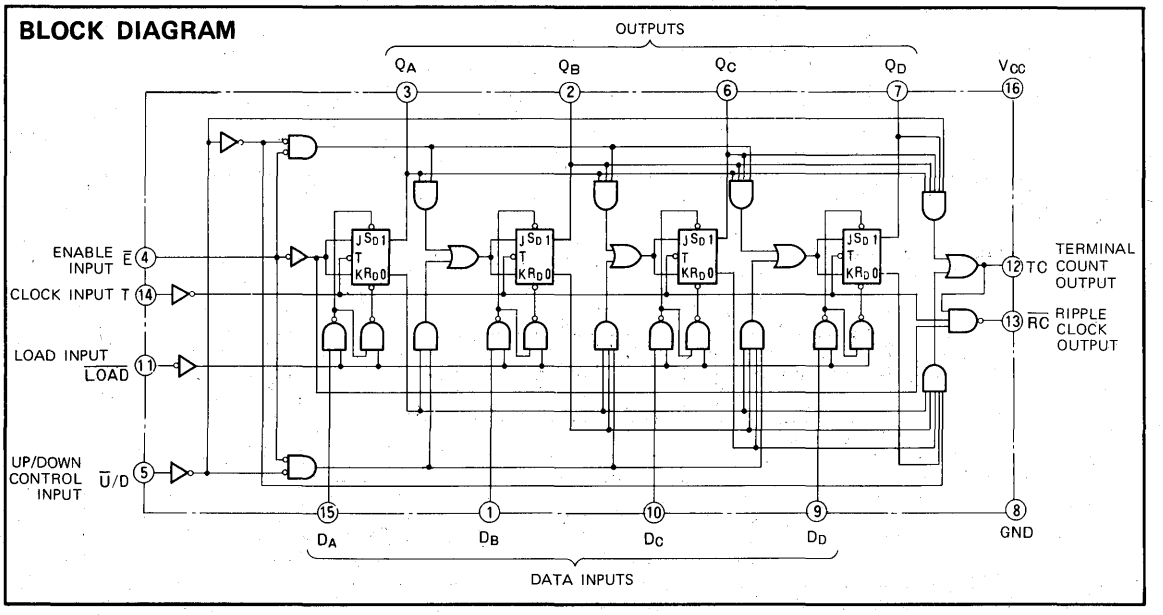


Outline 16P4

High appears in the terminal count output TC during count-up while 15_2 appears in Q_A, Q_B, Q_C and Q_D and during count-down while 0_2 appears. Low appears in the ripple clock output $\overline{RC}$ only when $\overline{E}$ and T are low and 15_2 appears in outputs Q_A, Q_B, Q_C and Q_D during count-up or 0_2 appears in the outputs during count-down. $\overline{E}$, TC and $\overline{RC}$ are used when cascade-connecting the counter. (Refer to application example.)

$\overline{E}$ can be changed from high to low irrespective of the status of T but when changed from low to high, T must be high. Perform the change for $\overline{U}/D$ when T is high.

BLOCK DIAGRAM



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SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

FUNCTION TABLE (Note 1)

$\overline{LOAD}$	$\overline{E}$	$\overline{U}/D$	T	Q_A	Q_B	Q_C	Q_D
L	X	X	X	D_A	D_B	D_C	D_D
H	L	L	↑	Count-up			
H	L	H	↑	Count-down			
H	H	X	X	Inhibit			

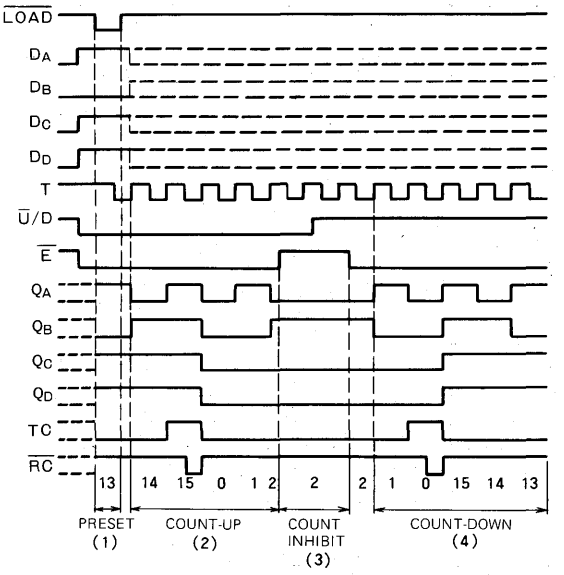
Note 1 ↑ : Transition from low to high level

X : Irrelevant

$\overline{E}$	TC(1)	T	$\overline{RC}$
L	H	L	L
L	H	H	H
H	X	X	H
X	L	X	H

(1) TC is the output but the signal generated internally by the following logical expression.;
$TC = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot (\overline{U}/D)$ ····· Count-up
$TC = \overline{Q}_A \cdot \overline{Q}_B \cdot \overline{Q}_C \cdot \overline{Q}_D \cdot (\overline{U}/D)$ ····· Count-down

OPERATION TIMING DIAGRAM



Details of timing diagram
(1) Preset to 13 (2) Count-up 14, 15, 0, 1, 2
(3) Count inhibit (4) Count-down 1, 0, 15, 14, 13

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
			$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	T, $\overline{LOAD}$, $\overline{U}/D$, $D_A \sim D_D$	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{E}$					60	μA
		T, $\overline{LOAD}$, $\overline{U}/D$, $D_A \sim D_D$	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{E}$					0.3	mA
I_{IL}	Low-level input current	T, $\overline{LOAD}$, $\overline{U}/D$, $D_A \sim D_D$	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$\overline{E}$					−1.2	mA
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 3)			20	35	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3. I_{CC} is measured with all the inputs at 0V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

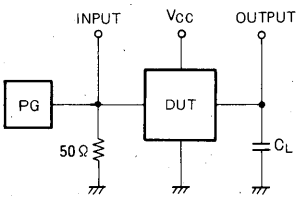
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
fmax	Maximum clock freqency	$C_L=15pF$ (Note 4)	20	40		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{LOAD}$ to outputs Q_A, Q_B, Q_C, Q_D			19	33	ns
t_{PHL}				25	50	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B, D_C, D_D to outputs Q_A, Q_B, Q_C, Q_D			11	32	ns
t_{PHL}				25	40	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output $\overline{RC}$			11	20	ns
t_{PHL}				11	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				14	36	ns
t_{PLH}	Low-to-high-output, high-to-low-level output propagation time, from input T to output TC			20	42	ns
t_{PHL}				24	52	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{U}/D$ to output $\overline{RC}$			22	45	ns
t_{PHL}				20	45	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{U}/D$ to output TC			15	33	ns
t_{PHL}				15	33	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E}$ to output $\overline{RC}$			10	33	ns
t_{PHL}				11	33	ns

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

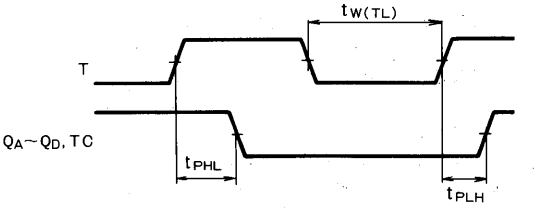
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{W(TL)}$	Clock input T low pulse width		25	9		ns
$t_{W(\overline{LOAD})}$	Load $\overline{LOAD}$ pulse width		35	10		ns
t_r	Clock pulse rise time			2000	100	ns
$t_{SU(D)}$	Setup time $D_A \sim D_D$ to $\overline{LOAD}$		20	9		ns
$t_{SU(\overline{EL})}$	Setup time $\overline{E}$ low to T		40	24		ns
$t_{h(D)}$	Hold time $D_A \sim D_D$ to $\overline{LOAD}$		5	0		ns
$t_{h(\overline{EL})}$	Hold time $\overline{E}$ low to T		5	2		ns
$t_{rec(\overline{LOAD})}$	Recovery time $\overline{LOAD}$ to T		20	16		ns

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER WITH MODE CONTROL

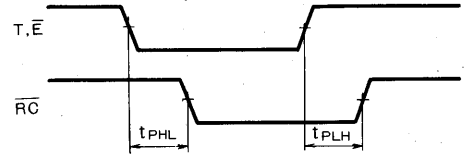
Note 4: Measurement circuit

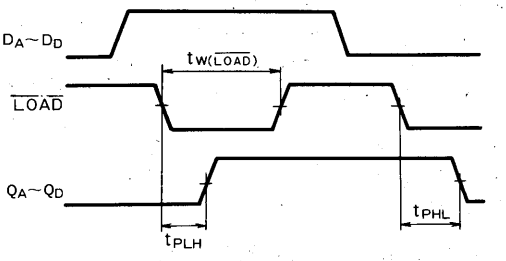


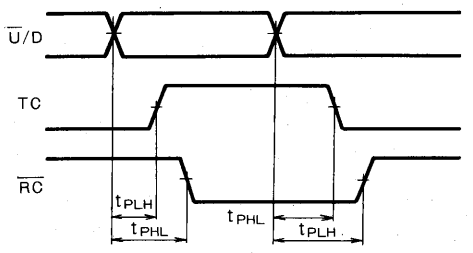
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Zo = 50Ω.
(2) C_L includes probe and jig capacitance

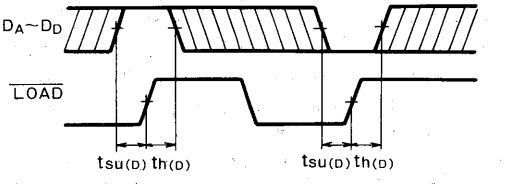


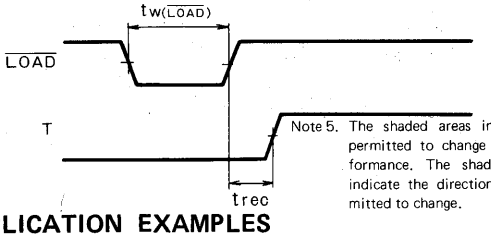
TIMING DIAGRAM (Reference level = 1.3V)



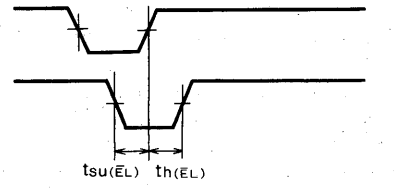






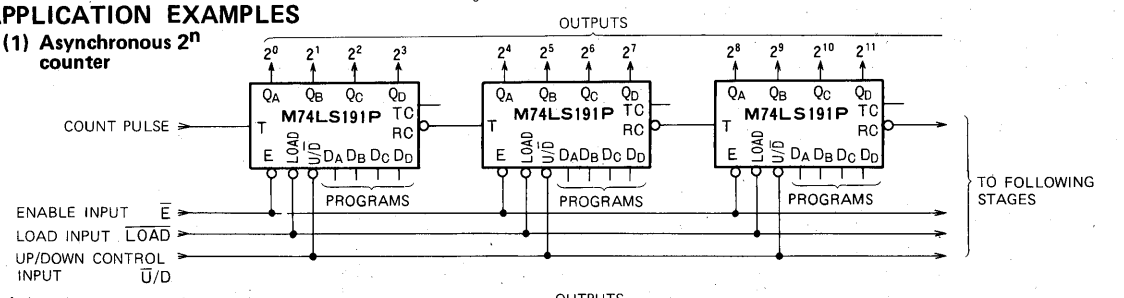


Note 5. The shaded areas indicate when the input is permitted to change for predictable output performance. The shaded areas with the arrows indicate the direction of when the input is permitted to change.

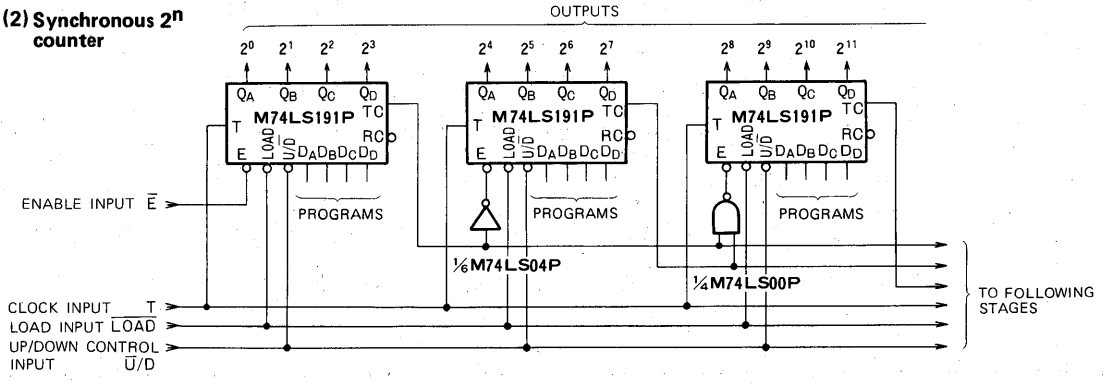


APPLICATION EXAMPLES

(1) Asynchronous 2^n counter



(2) Synchronous 2^n counter



M74LS192P

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

DESCRIPTION

The M74LS192P is a semiconductor integrated circuit containing a synchronous decade up/down counter function with direct reset and preset inputs.

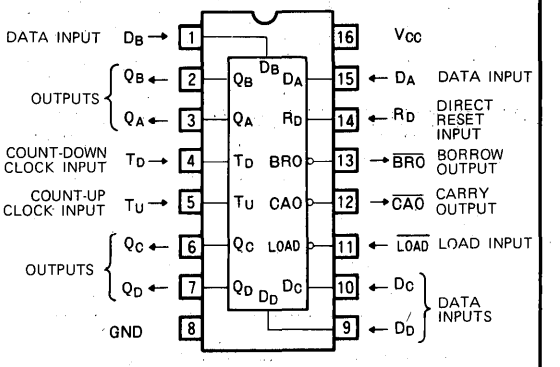
FEATURES

- Special up count, down count clock inputs
- Asynchronous preset input provided
- Direct reset input provided
- Easy cascade connection possible
- High-speed counting (f_{max}= 38MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

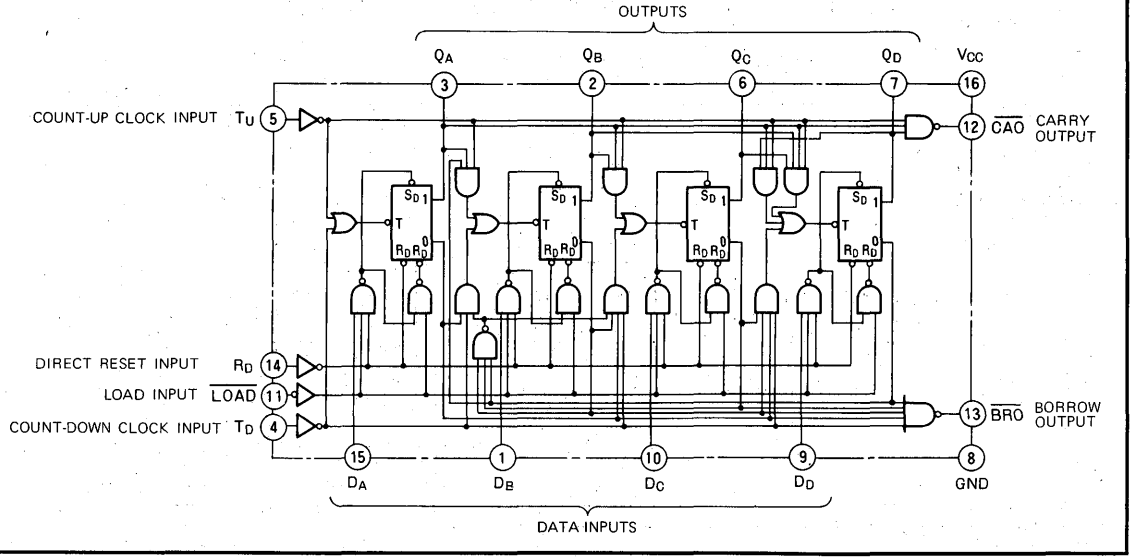
This device comes with special count-up clock input T_U and count-down clock input T_D used independently for count-up and count-down applications. For count-up, the number of count pulses appears as a BCD code in outputs Q_A, Q_B, Q_C and Q_D in synchronization with the count pulses by setting load input $\overline{LOAD}$ and T_D high, applying the count pulses to T_U while for count-down, $\overline{LOAD}$ and T_U are set high and the count pulses are applied to T_D. Counting is performed when T_U or T_D changes from low to high.

Presetting is performed independently of the count pulse. When data are applied to data inputs D_A, D_B, D_C and D_D and $\overline{LOAD}$ is set low, the D_A, D_B, D_C and D_D signals appear in the Q_A, Q_B, Q_C and Q_D outputs, respectively, regardless of the status of the T_U and T_D signals, thereby presetting the counter. Counting proceeds as per the status transition diagram with presetting to a numerical value of 10 or more.

Reset can be performed by setting the direct reset input R_D high which sets $Q_A = Q_B = Q_C = Q_D$ low irrespective of the status of the other inputs.

Low appears in the carry output $\overline{CAO}$ during count-up when 9 appears in Q_A, Q_B, Q_C and Q_D and when T_U is low while low appears in output $\overline{BRO}$ when 0 appears in the outputs $\overline{CAO}$ and $\overline{BRO}$ should be connected to the next stage T_U and T_D for counter cascade connection. (Refer to the application examples.)

BLOCK DIAGRAM



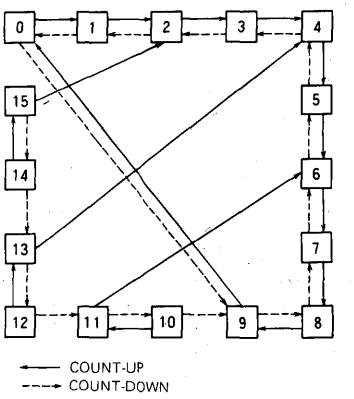
SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

FUNCTION TABLE (Note 1)

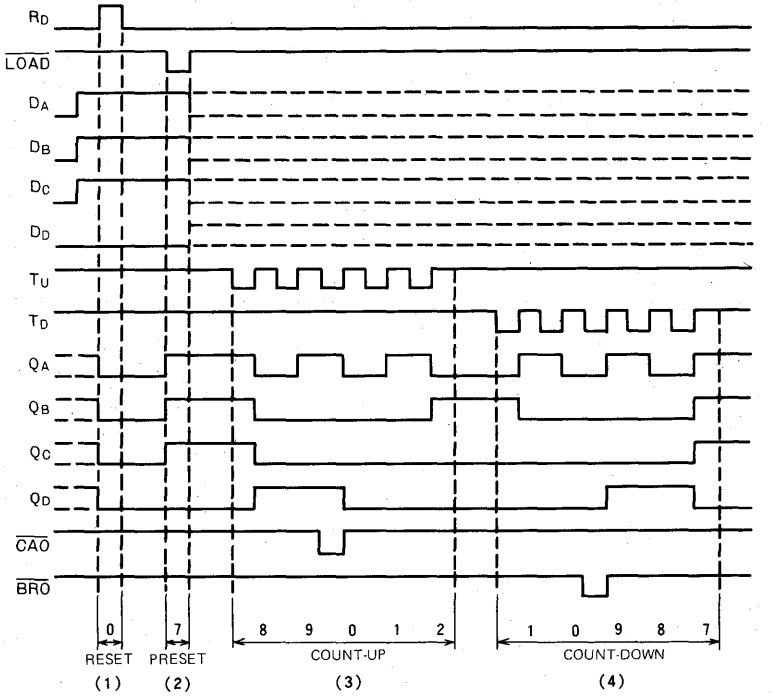
R_D	$\overline{LOAD}$	T_U	T_D	Q_A	Q_B	Q_C	Q_D	$\overline{CAO}$	$\overline{BRO}$
H	X	X	X	L	L	L	L	H	H*
L	L	X	X	D_A	D_B	D_C	D_D	H*	H*
L	H	H	H	Inhibit				H*	H*
L	H	↑	H	Count-up				H*	H*
L	H	H	↑	Count-down				H*	H*

Note 1. ↑ : Transition from low to high
* : Normally high but low appears in accordance with the following logical expressions:
$\overline{CAO} = \overline{Q_A \cdot Q_D \cdot T_U}$ ..... Count-up
$\overline{BRO} = \overline{Q_A \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot \overline{Q_D} \cdot \overline{T_D}}$ ..... Count-down
X : Irrelevant

STATE DIAGRAM



OPERATION TIMING DIAGRAM



Details of timing diagram
(1) Reset
(2) Preset to 7
(3) Count-up 8, 9, 0, 1, 2
(4) Count-down 1, 0, 9, 8, 7

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

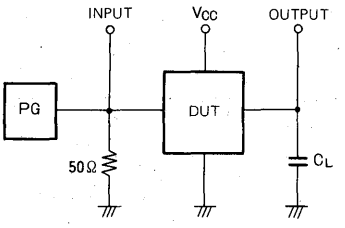
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$, $V_I = 0.8V$ $V_I = 2V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$	$I_{OL} = 4mA$		0.25	0.4	V
		$V_I = 0.8V, V_I = 2V$	$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC} = 5.25V$, $V_O = 0V$		−20		−100	mA
I_{CC}	Supply current	$V_{CC} = 5.25V$ (Note 3)			19	34	mA

* : All typical values are at $V_{CC} = 5V$, $Ta = 25°C$.
Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3. I_{CC} is measured with R_D and $\overline{LOAD}$ at 0V and T_U, T_D, $D_A \sim D_D$ at 4.5V

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L = 15pF$ (Note 4)	25	38		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T_U to output $\overline{CAO}$			7	26	ns
t_{PHL}				14	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T_D to output $\overline{BRO}$			7	24	ns
t_{PHL}				19	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T_U, T_D to outputs Q_A, Q_B, Q_C, Q_D			20	38	ns
t_{PHL}				17	47	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{LOAD}$ to outputs Q_A, Q_B, Q_C, Q_D			24	40	ns
t_{PHL}				20	40	ns
t_{PHL}	High-to-low-level output propagation time, from input R_D to outputs Q_A, Q_B, Q_C, Q_D			12	35	ns

Note 4. Measurement circuit



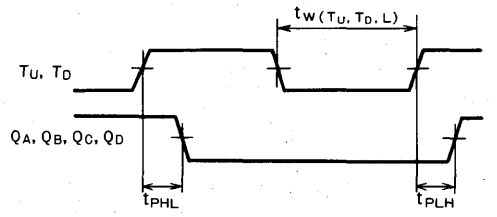
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance

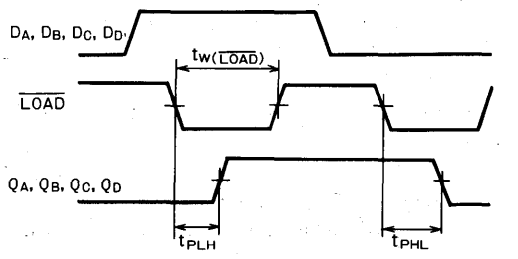
SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

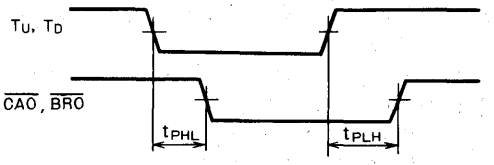
TIMING REQUIREMENTS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

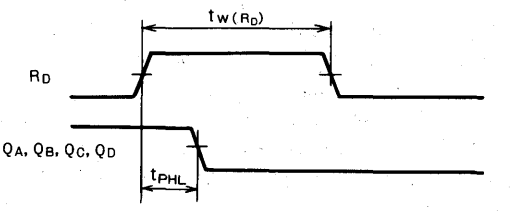
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(T_UL)}$	Clock input T_U low pulse width		20	14		ns
$t_{W(T_DL)}$	Clock input T_D low pulse width		20	18		ns
$t_{W(\overline{LOAD})}$	Load $\overline{LOAD}$ pulse width		20	11		ns
$t_{W(R_D)}$	Direct reset R_D pulse width		20	4		ns
$t_{SU(D)}$	Setup time D_A~D_D to $\overline{LOAD}$		20	4		ns
$t_{h(D)}$	Hold time D_A~D_D to $\overline{LOAD}$		5	−3		ns

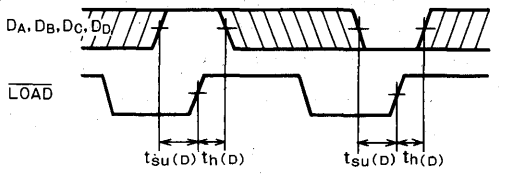
TIMING DIAGRAM (Reference level = 1.3V)







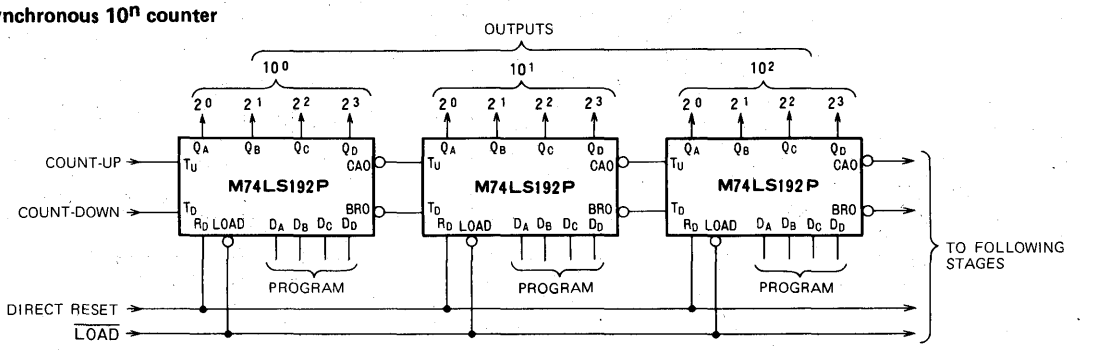




Note 5. The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Asynchronous 10^n counter



M74LS193P

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

DESCRIPTION

The M74LS193P is a semiconductor integrated circuit containing a synchronous hexadecimal (4-bit binary) up/down counter with direct reset and preset.

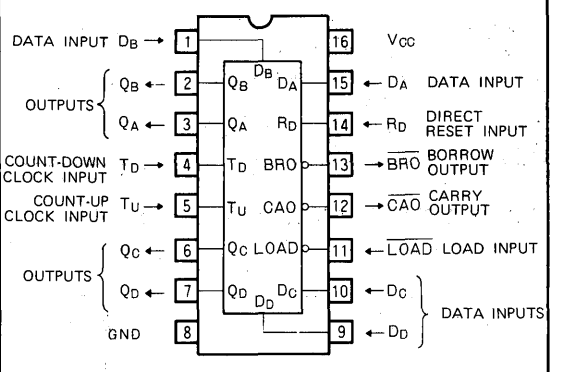
FEATURES

- Special clock for up count, down count
- Asynchronous preset input provided
- Direct reset input provided
- Cascade connection easily made
- High-speed counting (f_{max}=38MHz typical)
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

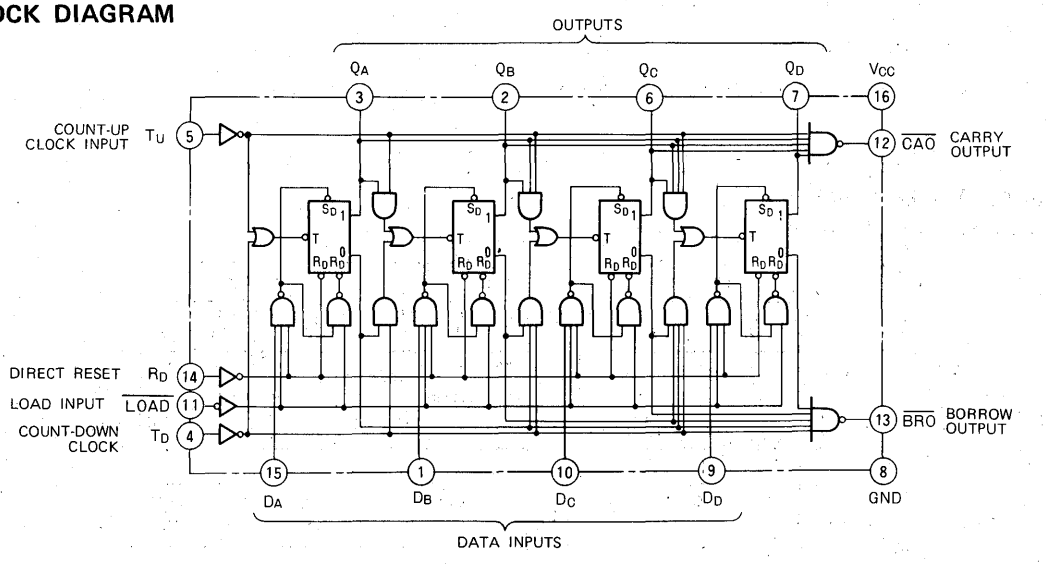
This device comes with special count-up clock input T_U and count-down clock input T_D used independently for count-up and count-down applications. For count-up, the count pulse number appears as a 4-bit pure binary code in outputs Q_A, Q_B, Q_C and Q_D in synchronization with the count pulses by setting load input $\overline{LOAD}$ and T_D to high, applying the count pulses to T_U while for count-down, $\overline{LOAD}$ and T_U are set high and the count pulses are applied to T_D. Counting is performed when T_U or T_D changes from low to high.

Presetting is performed regardlessly of the count pulse. When data are applied to data inputs D_A, D_B, D_C and D_D and $\overline{LOAD}$ is set low, the D_A, D_B, D_C and D_D signals appear in the Q_A, Q_B, Q_C, and Q_D outputs, respectively, regardless of the status of the T_U and T_D signals, thereby presetting the counter.

Reset can be performed by setting the direct reset input RD high which sets $Q_A = Q_B = Q_C = Q_D$ low irrespective of the status of the other inputs.

Low appears is the carry output $\overline{CAO}$ during count-up when 15 appears in Q_A, Q_B, Q_C and Q_D and when T_U is low, while low appears in output $\overline{BRO}$ when 0 appears in the outputs and when T_D is low. $\overline{CAO}$ and $\overline{BRO}$ should be connected to T_U and T_D of the next stage for cascade connection. (Refer to the application example.)

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

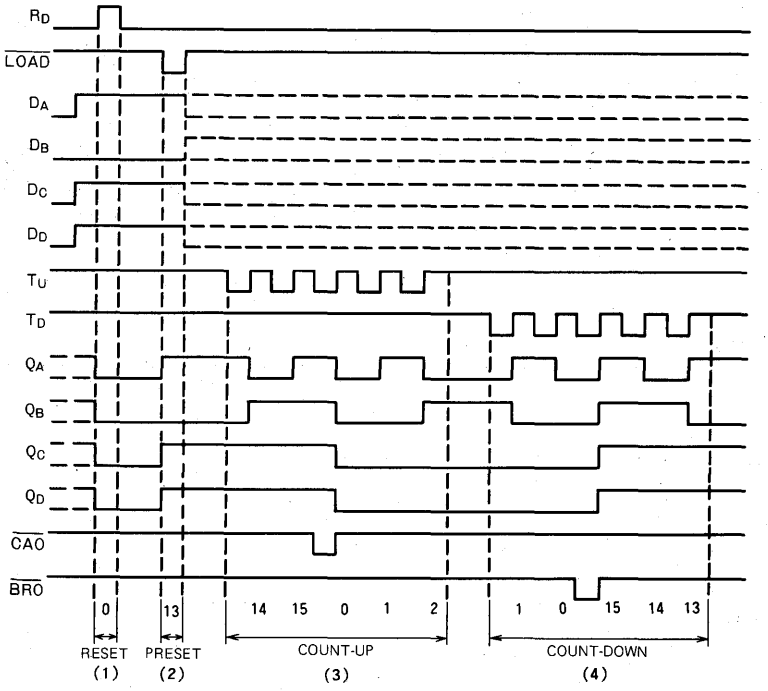
SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

FUNCTION TABLE (Note 1)

R_D	$\overline{LOAD}$	T_U	T_D	Q_A	Q_B	Q_C	Q_D	$\overline{CAO}$	$\overline{BRO}$
H	X	X	X	L	L	L	L	H	H*
L	L	X	X	D_A	D_B	D_C	D_D	H*	H*
L	H	H	H	Inhibit				H*	H*
L	H	↑	H	Count-up				H*	H*
L	H	H	↑	Count-down				H*	H*

Note 1 ↑ : Transition from low to high
* : Normally high but low appears in accordance with the following
$CAO = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot T_U$ ..... Count-up
$BRO = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot T_D$ ..... Count-down
X : Irrelevant

OPERATION TIMING DIAGRAM



Details of timing diagram
(1) Reset
(2) Preset to 13
(3) Count-up 14, 15, 0, 1, 2
(4) Count-down 1, 0, 15, 14, 13

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

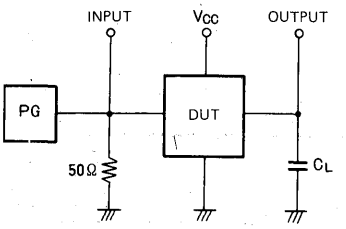
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 3)			19	34	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with R_D and $\overline{LOAD}$ at 0V and T_U, T_D, $D_A \sim D_D$ at 4.5V

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L=15pF$ (Note 4)	25	38		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T_U to output $\overline{CAO}$			7	26	ns
t_{PHL}				14	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T_D to output $\overline{BRO}$			7	24	ns
t_{PHL}				19	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs T_U, T_D to outputs Q_A, Q_B, Q_C, Q_D			20	38	ns
t_{PHL}				17	47	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{LOAD}$ to outputs Q_A, Q_B, Q_C, Q_D			24	40	ns
t_{PHL}				20	40	ns
t_{PHL}	High-to-low-level output propagation time, from input R_D to outputs Q_A, Q_B, Q_C, Q_D			12	35	ns

Note 4: Measurement circuit



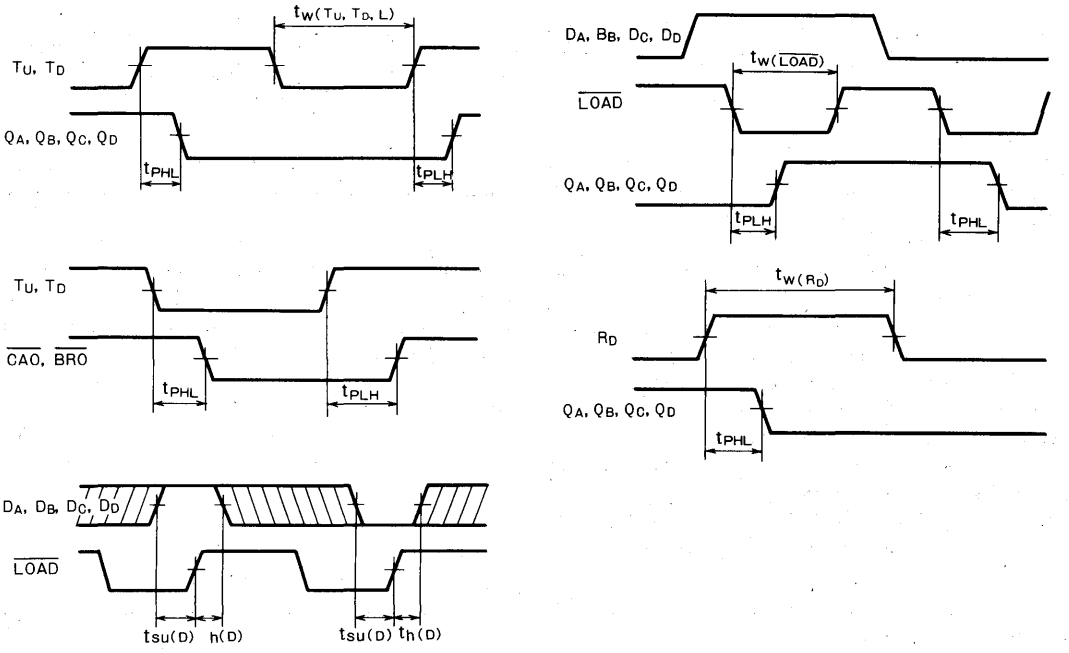
(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Z_O=50Ω.
(2) C_L includes probe and jig capacitance

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(T_UL)}$	Clock input T_U low pulse width		20	14		ns
$t_{W(T_DL)}$	Clock input T_D low pulse width		20	18		ns
$t_{W(\overline{LOAD})}$	Load $\overline{LOAD}$ pulse width		20	11		ns
$t_{W(R_D)}$	Direct reset R_D pulse width		20	4		ns
$t_{SU(D)}$	Setup time D_A~D_D to $\overline{LOAD}$		20	4		ns
$t_{h(D)}$	Hold time D_A~D_D to $\overline{LOAD}$		5	−3		ns

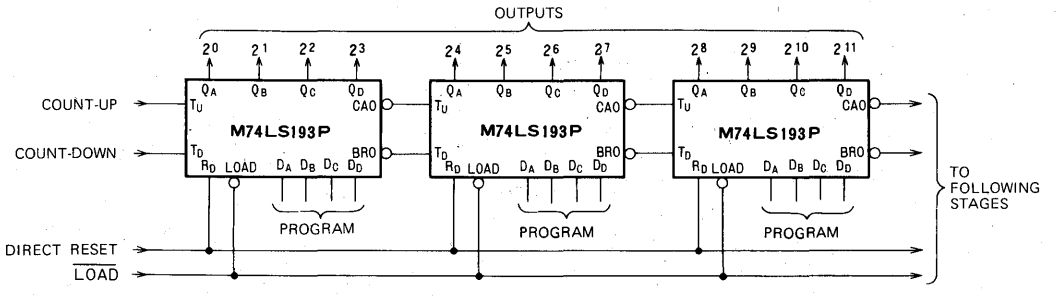
TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

Asynchronous 2^n counter



M74LS194AP

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH RESET

DESCRIPTION

The M74LS194AP is a semiconductor integrated circuit with a 4-bit bidirectional serial/parallel input-serial/parallel output shift register functions.

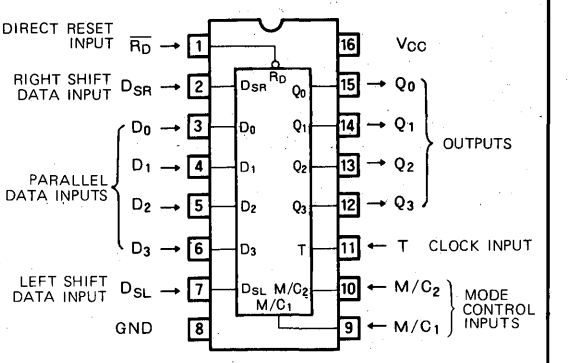
FEATURES

- Synchronous serial/parallel input-serial/parallel/output
- Right shift and left shift functions
- Mode control input provided
- Direct reset input provided
- Hold mode function
- Wide operating temperature range (T_a= –20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



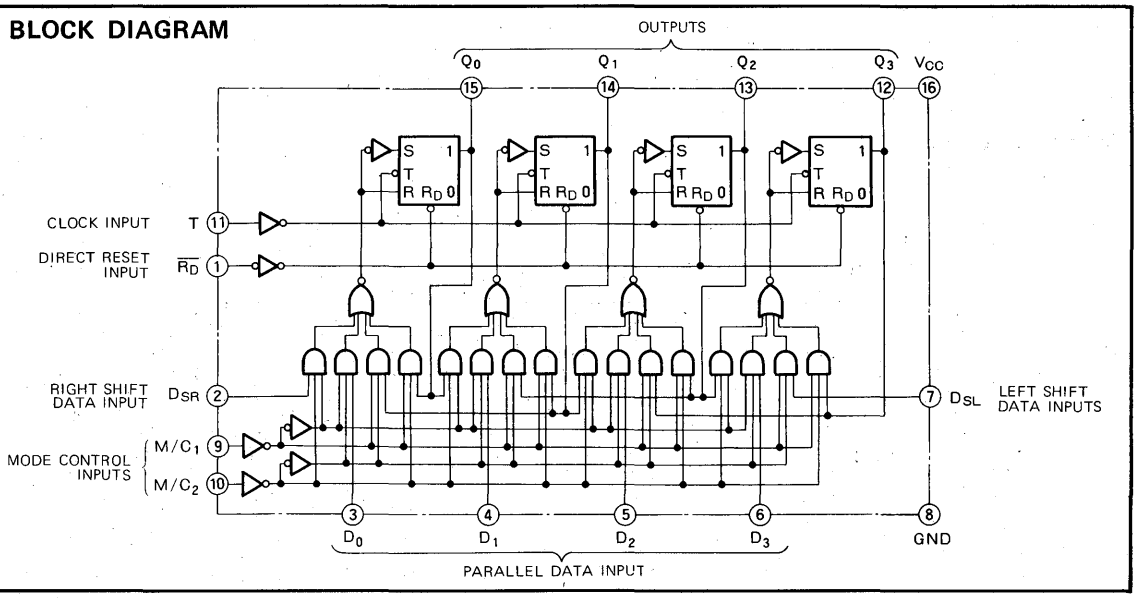
Outline 16P4

FUNCTIONAL DESCRIPTION

This device is usable as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the modes control inputs M/C_1 and M/C_2. When M/C_1 is kept in high and M/C_2 in low, the serial data are applied to right shift data input D_{SR} and the clock pulse is applied to clock input T, the serial data are shifted sequentially to outputs Q_0~Q_3 in synchronization with the clock pulse. When M/C_1 is kept in low and M/C_2 in high the serial data are applied to left shift data input D_{SL} and clock pulse is applied to clock input T, the serial data are shifted sequentially in synchronization with the clock pulse. The D_0~D_3 signal appears in Q_0~Q_3 by keeping M/C_1 and M/C_2 in high, applying the parallel data to parallel data inputs D_0~D_3 and applying a 1-bit clock pulse to clock input T. When both M/C_1 and M/C_2 are kept in low, the status of the flip-flops does not change even if the clock pulse is applied to the clock input T.

When T changes from low to high, the right shift, left shift or parallel data are read in. Q_0~Q_3 are set low by setting direct reset input $\overline{R_D}$ low irrespective of the status of the other input signals.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH RESET

FUNCTION TABLE (Note 1)

Operational mode	$\overline{R_D}$	M/C_1	M/C_2	T	D_{SR}	D_{SL}	$D_0 \sim D_3$	Q_0	Q_1	Q_2	Q_3
Direct reset	L	X	X	X	X	X	X	L	L	L	L
Right shift	H	H	L	↑	L	X	X	L	Q_0^0	Q_1^0	Q_2^0
	H	H	L	↑	H	X	X	H	Q_0^0	Q_1^0	Q_2^0
Left shift	H	L	H	↑	X	L	X	Q_1^0	Q_2^0	Q_3^0	L
	H	L	H	↑	X	H	X	Q_1^0	Q_2^0	Q_3^0	H
Parallel read	H	H	H	↑	X	X	$D_0 \sim D_3$	D_0	D_1	D_2	D_3
Clock inhibit	H	L	L	X	X	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0

Note 1. ↑ : Transition from low to high (positive edge trigger)
Q^0 : Level of Q before the indicated steady-state input conditions were established
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($Ta = -20 \sim +75℃$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20 \sim +75$	℃
Tstg	Storage temperature range		$-65 \sim +150$	℃

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75℃$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75℃$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ ✱	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 3)			15	23	mA

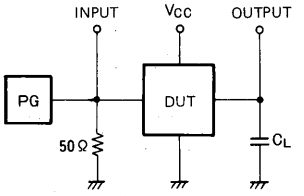
✱ : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2: All measurements must be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured after $D_0 \sim D_3$ have been set to 0V, D_{SR}, D_{SL}, M/C_1, M/C_2 and $\overline{R_D}$ to 4.5V and T to 4.5V from 0V.

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER WITH RESET

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L=15pF (Note 4)	25	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs $Q_0 \sim Q_3$			10	22	ns
t_{PHL}				12	26	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to outputs $Q_0 \sim Q_3$			8	30	ns

Note 4: Measurement circuit

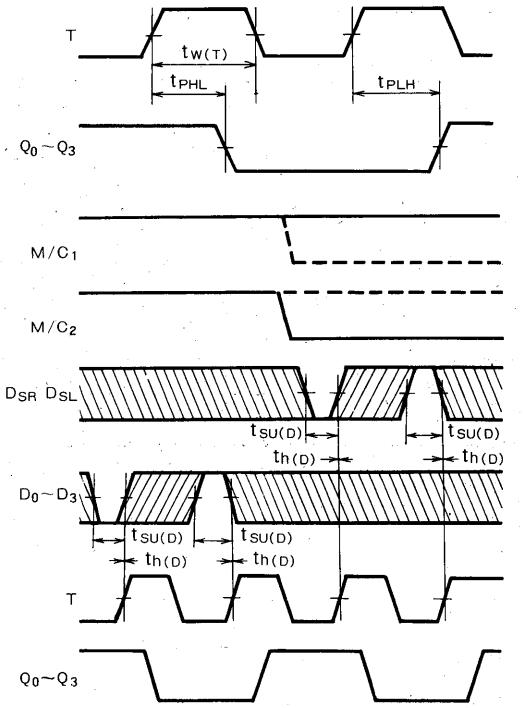


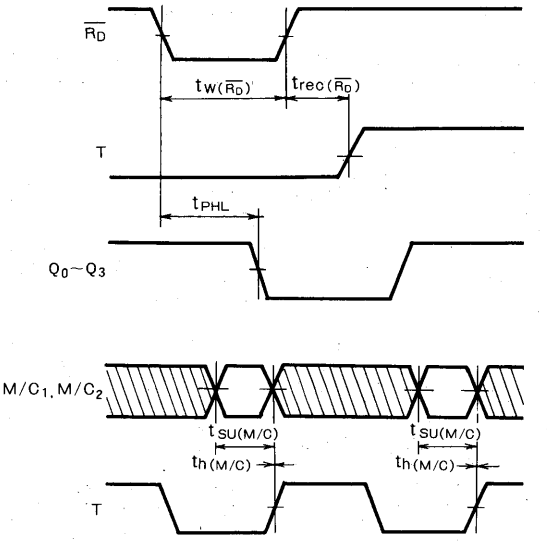
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(T)}$	Clock input T high pulse width		20	5		ns
$t_{w(\overline{R_D})}$	Direct reset input $\overline{R_D}$ pulse width		20	6		ns
$t_{su(D)}$	Setup time D to T		20	7		ns
$t_{su(M/C)}$	Setup time M/C_1, M/C_2 to T		30	12		ns
$t_{h(D)}$	Hold time D to T		0	− 3		ns
$t_{h(M/C)}$	Hold time M/C_1, M/C_2 to T		0	− 6		ns
$t_{rec(\overline{R_D})}$	Recovery time to direct reset		25	3		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance. The broken liners for M/C_1 and M/C_2 indicate three timings for left shifting. Setup time D_{SR} is for Q_0 only; setup time D_{SL} is for Q_3 only

MITSUBISHI ELECTRIC

M74LS195AP

4-BIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

DESCRIPTION

The M74LS195AP is a semiconductor integrated circuit containing a 4-bit serial/parallel input-serial/parallel output shift register function with a direct reset input.

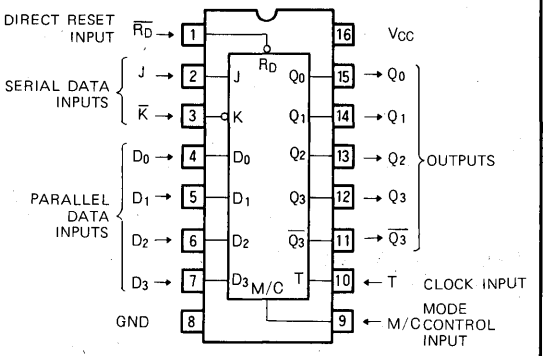
FEATURES

- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection
- Mode control input provided
- Serial inputs J and $\overline{K}$ provided
- Direct reset input provided
- Q_3 and $\overline{Q_3}$ outputs provided
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



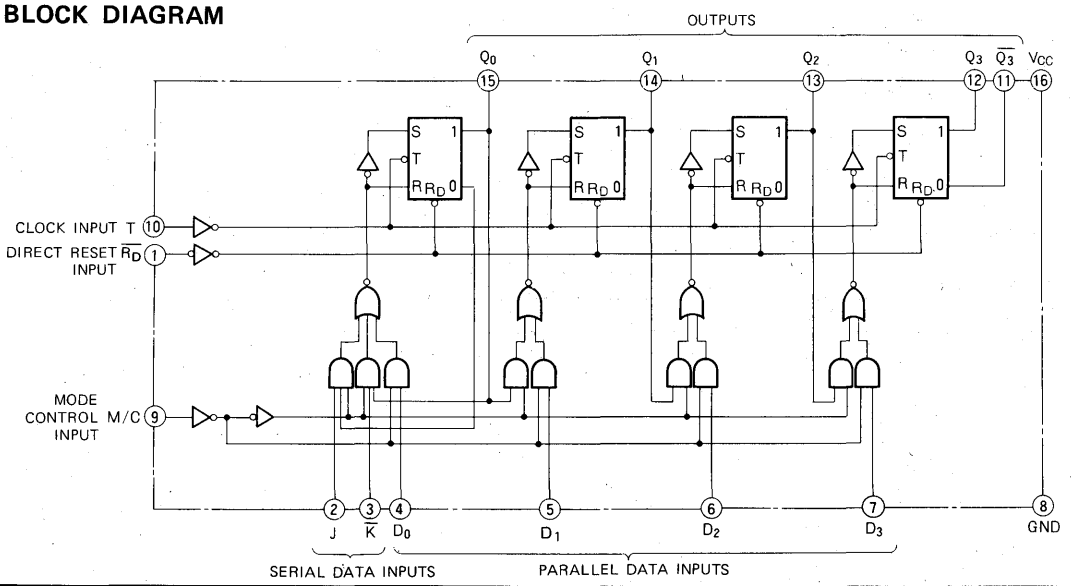
Outline 16P4

FUNCTIONAL DESCRIPTION

This device can be used as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept in high, the serial data are applied to serial data inputs J and $\overline{K}$ and the clock pulse is applied to clock input T, the serial data are shifted sequentially into outputs Q_0~$\overline{Q_3}$ in synchronization with the clock pulse. The first stage flip-flop with J and $\overline{K}$ functions as a J-K flip-flop. When serial data are applied from line 1, J and $\overline{K}$ are mutually connected and used as serial input pins. When M/C is kept in low, the parallel data are applied to parallel data inputs D_0~D_3 and a 1-bit clock pulse is applied to T, the D_0~D_3 signals appears in Q_0~$\overline{Q_3}$. When T changes from low to high, the shift or parallel reading operation is performed.

The last stage flip-flop output has mutually complementary outputs Q_3 and $\overline{Q_3}$. Q_0~Q_3 are reset low and $\overline{Q_3}$ high by setting direct reset input $\overline{R_D}$ low irrespective of all the other input signals.

BLOCK DIAGRAM



4-BIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

FUNCTION TABLE (Note 1)

Operational mode	T	$\overline{R_D}$	M/C	J	$\overline{K}$	$D_0 \sim D_3$	Q_0	Q_1	Q_2	Q_3	$\overline{Q_3}$
Direct reset	X	L	X	X	X	X	L	L	L	L	H
Right shift	↑	H	H	H	H	X	H	Q_0^0	Q_1^0	Q_2^0	$\overline{Q_2^0}$
	↑	H	H	L	L	X	L	Q_0^0	Q_1^0	Q_2^0	$\overline{Q_2^0}$
	↑	H	H	H	L	X	$\overline{Q_0^0}$	Q_0^0	Q_1^0	Q_2^0	$\overline{Q_2^0}$
	↑	H	H	L	H	X	Q_0^0	Q_0^0	Q_1^0	Q_2^0	$\overline{Q_2^0}$
Parallel read	↑	H	L	X	X	$D_0 \sim D_3$	D_0	D_1	D_2	D_3	$\overline{D_3}$

Note 1. ↑ : Transition from low to high (positive edge triggering)
Q^0: Level of Q before the indicated steady-state input conditions were established
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level output	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20 \sim +75$	℃
Tstg	Storage temperature range		$-65 \sim +150$	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				-1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=0.8V, V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				-0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$		-20		-100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 3)			14	21	mA

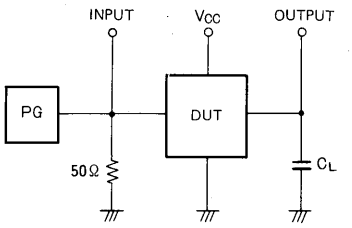
* : All typical values are at V_{CC}=5V, Ta=25°C.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with M/C at 0V, J, $\overline{K}$ and $D_0 \sim D_3$ at 4.5V, with $\overline{R_D}$ kept at 4.5V after changing from 0V and after changing T from 0V to 4.5V.

4-BIT PARALLEL-ACCESS SHIFT REGISTER WITH RESET

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L=15pF (Note 4)	30	60		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs $Q_0 \sim Q_3$, $\overline{Q_3}$			12	22	ns
t_{PHL}				12	26	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output $Q_0 \sim Q_3$			14	30	ns
t_{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output $\overline{Q_3}$			12	30	ns

Note 4: Measurement circuit

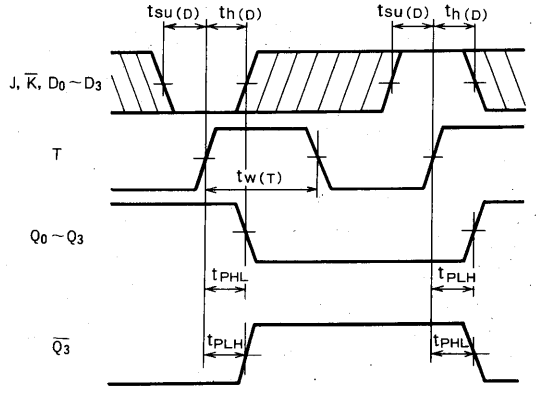


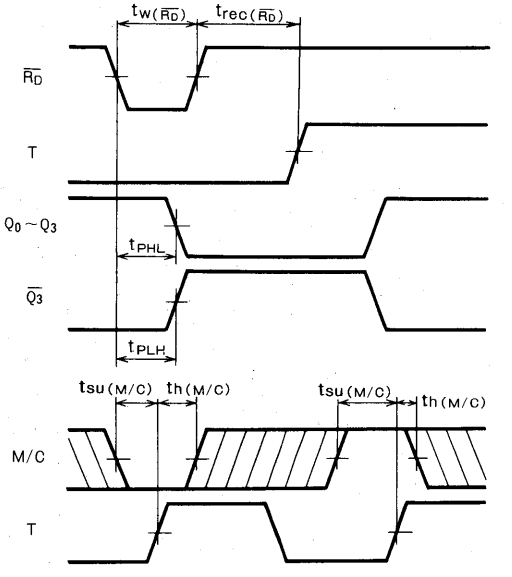
(1) The pulse generator has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(T)}$	Clock input T high pulse width		16	10		ns
$t_{W(\overline{R_D})}$	Direct reset $\overline{R_D}$ pulse width		12	6		ns
$t_{SU(D)}$	Setup time input data to T		15	3		ns
$t_{SU(M/C)}$	Setup time M/C to T		25	10		ns
$t_{h(D)}$	Hold time input data to T		3	−1		ns
$t_{h(M/C)}$	M/C hold time to T		0	−7		ns
$t_{rec(\overline{R_D})}$	Direct reset recovery time to T		25	5		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS196P

PRESETTABLE DECADE COUNTER/LATCH

DESCRIPTION

The M74LS196P is a semiconductor integrated circuit containing an asynchronous decade counter function with direct reset input and preset input.

FEATURES

- Direct reset input and asynchronous preset input provided
- Usable independently as binary and divide-by-five counter
- High-speed counting (f_{max} = 80MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

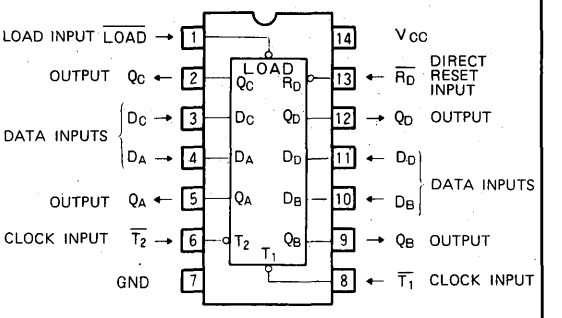
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-5 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B, Q_C and Q_D are employed for use as a divide-by-5 counter. When employed as a decade counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the count number as a BCD code appears in outputs Q_A, Q_B, Q_C and Q_D. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

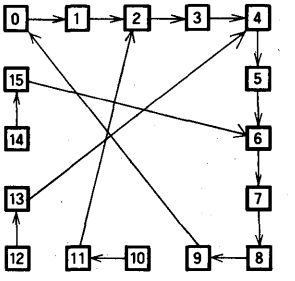
The counter can be preset by applying data to data inputs D_A, D_B, D_C and D_D and by setting $\overline{LOAD}$ input low, and the D_A, D_B, D_C and D_D signals appear in Q_A, Q_B, Q_C, Q_D outputs irrespective of the $\overline{T_1}$ and $\overline{T_2}$ inputs. When preset to a numerical value of 10 or above, the count proceeds in accordance with the status transition figure.

PIN CONFIGURATION (TOP VIEW)

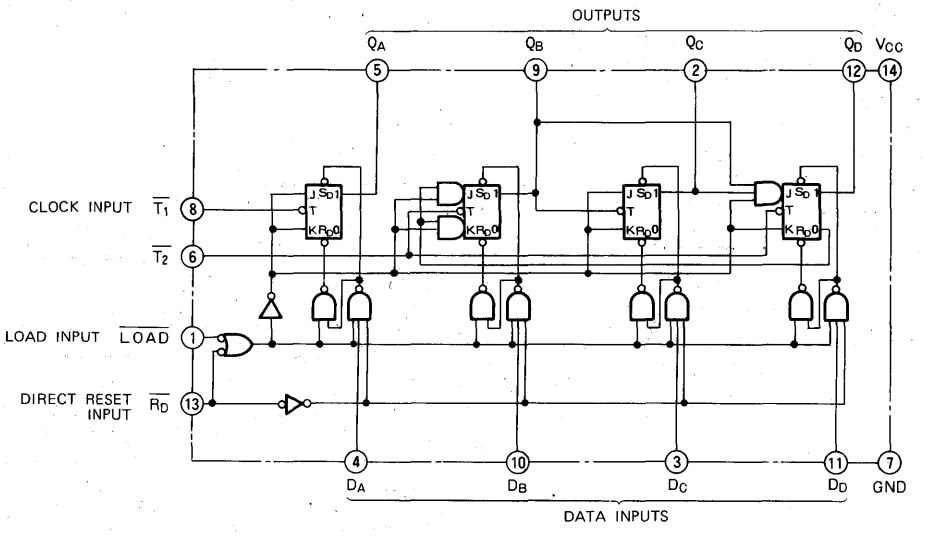


Outline 14P4

STATE DIAGRAM



BLOCK DIAGRAM



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PRESETTABLE DECADE COUNTER/LATCH

For resetting, it is possible to set $Q_A = Q_B = Q_C = Q_D$ = low by setting direct reset input R_D low irrespective of the status of the other inputs.

FUNCTION TABLE (Note 1)

$\overline{T}$	$\overline{R_D}$	$\overline{LOAD}$	Q_A	Q_B	Q_C	Q_D
X	L	X	L	L	L	L
X	H	L	D_A	D_B	D_C	D_D
↓	H	H	Count			

Note 1 ↓ : Transition from high to low (negative edge trigger)
X : Irrelevant

Count number	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

(1) Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS

($T_a = -20 \sim +75℃$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	−0.5 ~ +5.5	V
		Inputs $\overline{LOAD}$, $\overline{R_D}$, $D_A \sim D_D$	−0.5 ~ +15	
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75℃$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75℃$, unless otherwise noted)

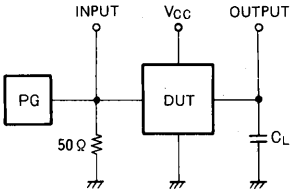
Symbol	Parameter		Test condtions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
			V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	$\overline{LOAD}$, D_A, D_B, D_C, D_D	V_{CC}=5.25V, V_I=2.7V				20	μA
		$\overline{T_1}$, $\overline{R_D}$					40	
		$\overline{T_2}$					80	
		$\overline{T_1}$	V_{CC}=5.25V, V_I=5.5V				0.2	mA
		$\overline{T_2}$					0.4	
		$\overline{LOAD}$, D_A, D_B, D_C, D_D	V_{CC}=5.25V, V_I=10V				0.1	
		$\overline{R_D}$					0.2	
I_{IL}	Low-level input current	$\overline{LOAD}$, D_A, D_B, D_C, D_D	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
		$\overline{R_D}$					−0.8	
		$\overline{T_1}$					−2.4	
		$\overline{T_2}$					−2.8	
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 3)			16	27	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A	C_L = 15pF (Note 4)	30	80		MHz
f_{max}	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B			25		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time from input $\overline{T_1}$ to output Q_A			9	15	ns
t_{PHL}				8	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_B			10	24	ns
t_{PHL}				10	33	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_C			20	57	ns
t_{PHL}				17	62	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_D			10	18	ns
t_{PHL}				9	45	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B, D_C, D_D to outputs Q_A, Q_B, Q_C, Q_D			9	30	ns
t_{PHL}				11	44	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input input $\overline{LOAD}$ to outputs Q_A, Q_B, Q_C, Q_D			14	41	ns
t_{PHL}				10	45	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to outputs Q_A, Q_B, Q_C, Q_D			14	51	ns

Note 4: Measurement circuit



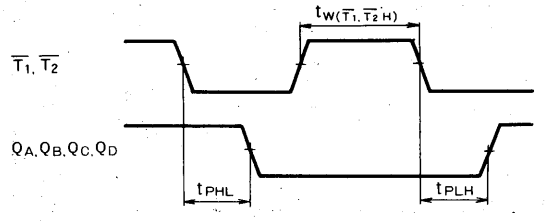
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_{P-P}, Zo = 50Ω.

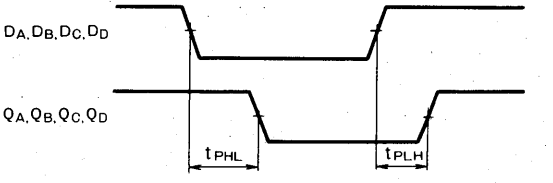
(2) C_L includes probe and jig capacitance

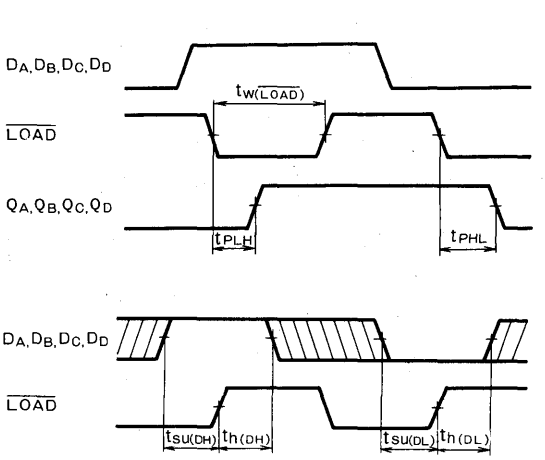
TIMING REQUIREMENTS (V_{CC} = 5 V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{T_1}H)}$	Clock input $\overline{T_1}$ high pulse width		20	5		ns
$t_{W(\overline{T_2}H)}$	Clock input $\overline{T_2}$ high pulse width		30	17		ns
$t_{W(\overline{LOAD})}$	Load $\overline{LOAD}$ input pulse width		20	8		ns
$t_{W(\overline{R_D})}$	Direct reset $\overline{R_D}$ pulse width		15	4		ns
$t_{SU(DL)}$	Setup time D_A~D_D low to $\overline{LOAD}$		15	3		ns
$t_{SU(DH)}$	Setup time D_A~D_D high to $\overline{LOAD}$		10	0		ns
$t_{h(DL)}$	Hold time D_A~D_D low to $\overline{LOAD}$		6	0		ns
$t_{h(DH)}$	Hold time D_A~D_D high to $\overline{LOAD}$		3	−1		ns
$t_{rec(\overline{LOAD})}$	Recovery time $\overline{LOAD}$ to $\overline{T}$		30	7		ns
$t_{rec(\overline{R_D})}$	Recovery time $\overline{R_D}$ to $\overline{T}$		30	7		ns

TIMING DIAGRAM (Reference level = 1.3V)



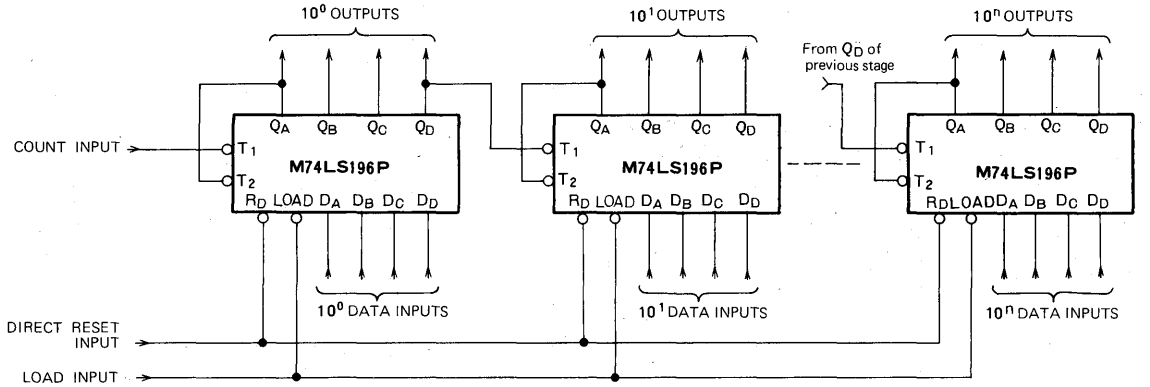




Note 5: *The shaded areas indicate when the input is permitted to change for predictable output performance.*

APPLICATION EXAMPLES

(1) Divide-by-10^n presettable counter

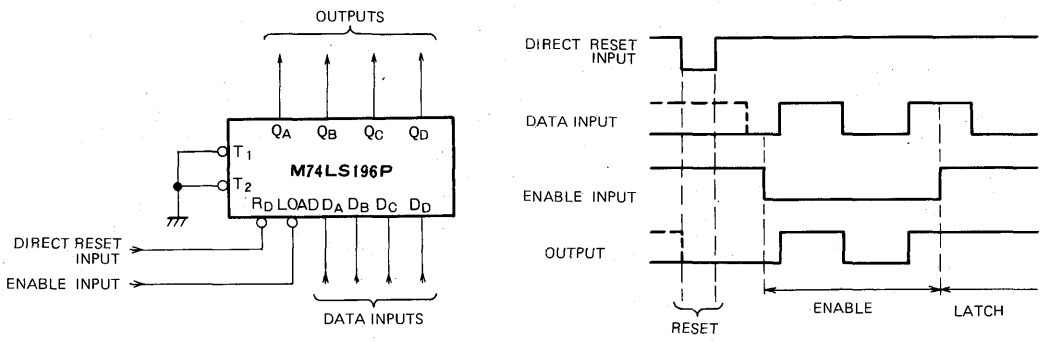


The above counter can be configured by connecting n + 1 M74LS196P devices. It operates at a high speed (60MHz typical) but since the system is synchronous, the time during which the output changes with respect to the input is delayed in accordance with the following formula.

The delay time (typical) of each output at the Mth stage is:

Q_A	20 (M−1) + 8 ns	Q_C	20 (M−1) +31 ns
Q_B	20 (M−1) +17 ns	Q_D	20 (M−1) +20 ns

(2) Use as a latch



M74LS197P

PRESETTABLE 4-BIT BINARY COUNTER/LATCH

DESCRIPTION

The M74LS197P is a semiconductor integrated circuit containing an asynchronous hexadecimal (4-bit binary) counter function with direct reset and preset inputs.

FEATURES

- Direct reset input and asychronous preset input provided
- Usable independently as binary and octal counter
- High-speed counting (f_{max}= 80MHz typical)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

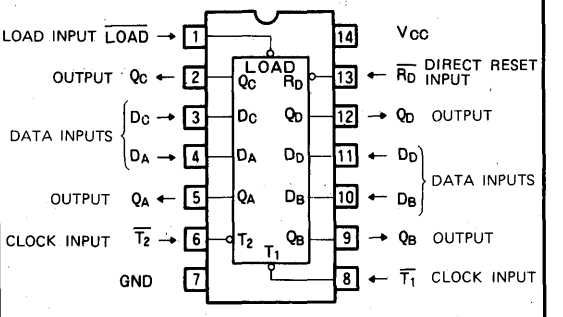
FUNCTIONAL DESCRIPTION

This device is composed of independent binary and octal counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B, Q_C and Q_D are employed for use as an octal counter. When employed as a hexadecimal counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the count number as a 4-bit pure binary code appears in outputs Q_A, Q_B, Q_C and Q_D. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The counter can be preset by applying data to data inputs D_A, D_B, D_C and D_D and by setting $\overline{LOAD}$ input low, and the D_A, D_B, D_C and D_D signals appear in Q_A, Q_B, Q_C, Q_D outputs irrespective of the $\overline{T_1}$ and $\overline{T_2}$ inputs.

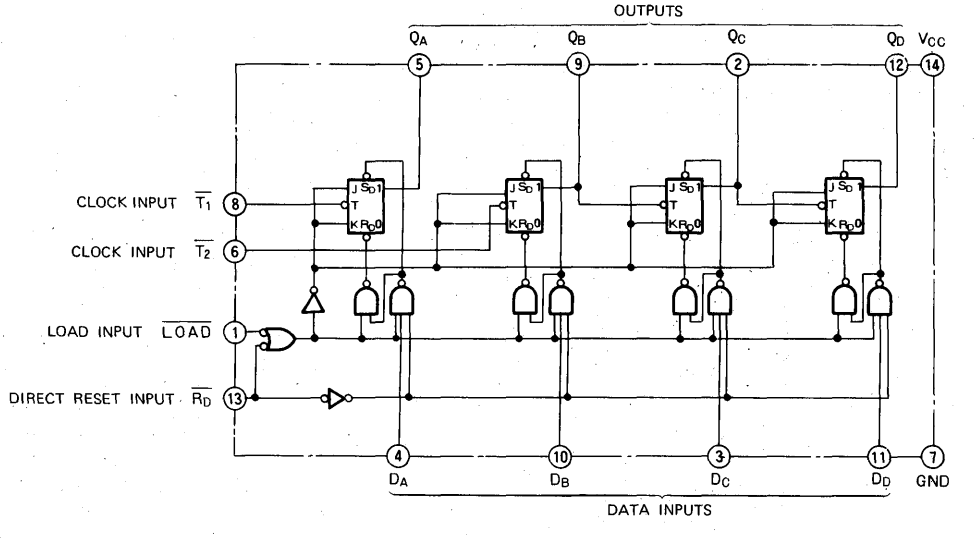
For resetting, it is possible to set Q_A = Q_B = Q_C = Q_D = low by setting direct reset input $\overline{R_D}$ low irrespective of the status of the other inputs.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

BLOCK DIAGRAM



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PRESETTABLE 4-BIT BINARY COUNTER/LATCH

FUNCTION TABLE (Note 1)

$\overline{T}$	$\overline{R_D}$	$\overline{LOAD}$	Q_A	Q_B	Q_C	Q_D
X	L	X	L	L	L	L
X	H	L	D_A	D_B	D_C	D_D
↓	H	H	Count			

Note 1 ↓ : Transition from high to low (negative trigger)
X : Irrelevant

Count number	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

(1) Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	−0.5 ~ +5.5	V
		Inputs $\overline{LOAD}$, $\overline{R_D}$, D_A ~ D_D	−0.5 ~ +15	
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
			$V_I=0.8V$, $V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$\overline{LOAD}$, D_A, D_B, D_C, D_D	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{R_D}$, $\overline{T_1}$, $\overline{T_2}$					40	μA
		$\overline{T_1}$, $\overline{T_2}$	$V_{CC}=5.25V$, $V_I=5.5V$				0.2	mA
		$\overline{LOAD}$, D_A, D_B, D_C, D_D	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{R_D}$					0.2	mA
I_{IL}	Low-level input current	$\overline{LOAD}$, D_A, D_B, D_C, D_D	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$\overline{R_D}$					−0.8	mA
		$\overline{T_1}$					−2.4	mA
		$\overline{T_2}$					−1.3	mA
I_{OS}	Short-circuit output current (note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 3)			16	27	mA

* : All typical values are at $V_{CC}=5V$, $Ta=25°C$.

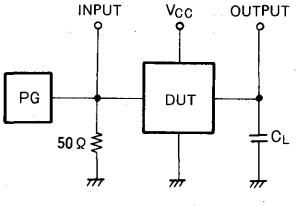
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditons	Limits Min	Limits Typ	Limits Max	Unit
fmax	Maximum clock frequency ($\overline{T_1}$)	$C_L=15pF$ (Note 4)	30	80		MHz
fmax	Maximum clock frequency ($\overline{T_2}$)			35		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_A			6	15	ns
t_{PHL}				7	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_B			8	19	ns
t_{PHL}				8	35	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_C			15	51	ns
t_{PHL}				15	63	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_D			22	78	ns
t_{PHL}				24	95	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B, D_C, D_D to outputs Q_A, Q_B, Q_C, Q_D			8	27	ns
t_{PHL}				10	44	ns
t_{PLH}	Low-to-high-level output propagation time, from input $\overline{LOAD}$ to outputs Q_A, Q_B, Q_C, Q_D			13	39	ns
t_{PHL}				10	45	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to outputs Q_A, Q_B, Q_C, Q_D			13	51	ns

Note 4: Measurement circuit



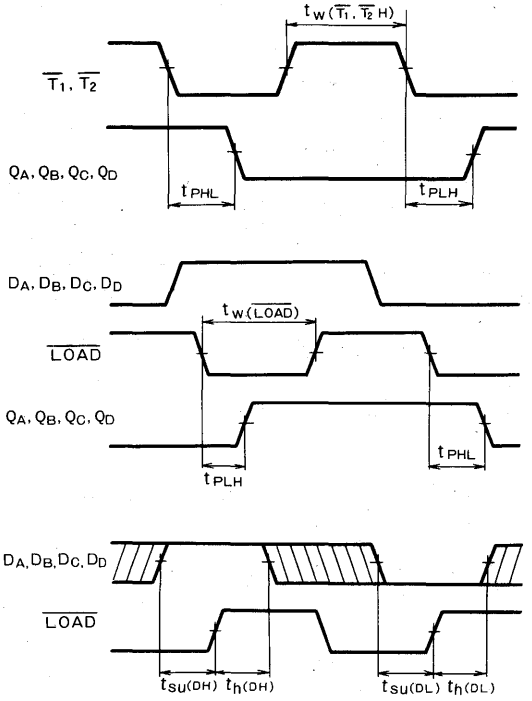
(1) The pusle generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.

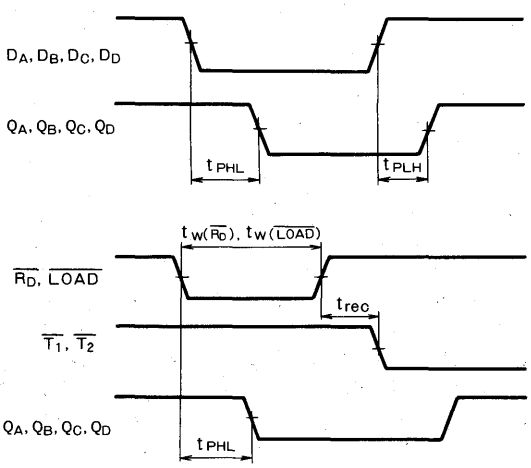
(2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}= 5 V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T_1H})}$	Clock input $\overline{T_1}$ high pulse width		20	5		ns
$t_{w(\overline{T_2H})}$	Clock input $\overline{T_2}$ high pulse width		30	14		ns
$t_{w(\overline{LOAD})}$	Load $\overline{LOAD}$ input pulse width		20	8		ns
$t_{w(\overline{RD})}$	Direct reset $\overline{R_D}$ pulse width		15	4		ns
$t_{su(DL)}$	Setup time D_A~D_D low to $\overline{LOAD}$		15	3		ns
$t_{su(DH)}$	Setup time D_A~D_D high to $\overline{LOAD}$		10	0		ns
$t_{h(DL)}$	Hold time D_A~D_D low to $\overline{LOAD}$		6	0		ns
$t_{h(DH)}$	Hold time D_A~D_D high to $\overline{LOAD}$		3	−1		ns
$t_{rec(\overline{LOAD})}$	Recovery time $\overline{LOAD}$ to $\overline{T}$		30	7		ns
$t_{rec(\overline{RD})}$	Recovery time $\overline{R_D}$ to $\overline{T}$		30	7		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS221P

DUAL MONOSTABLE MULTIVIBRATOR

DESCRIPTION

The M74LS221P is a semiconductor integrated circuit containing two monostable multivibrator circuits with direct reset inputs.

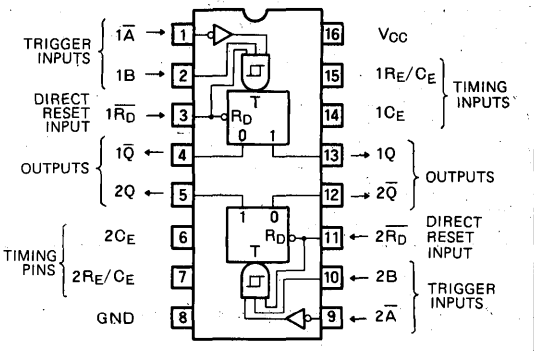
FEATURES

- Pulse width excellent temperature characteristics and supply voltage
- Schmidt trigger inputs (B inputs) provided
- Wide output pulse width range (t_w = 47ns ~ 1s)
- Operation possible with duty cycle up to 90% (R_T=100kΩ)
- Direct reset inputs provided
- $\overline{A}$, B complementary inputs provided
- Q and $\overline{Q}$ outputs
- High input breakdown voltage ($V_I \geqq 15V$)
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



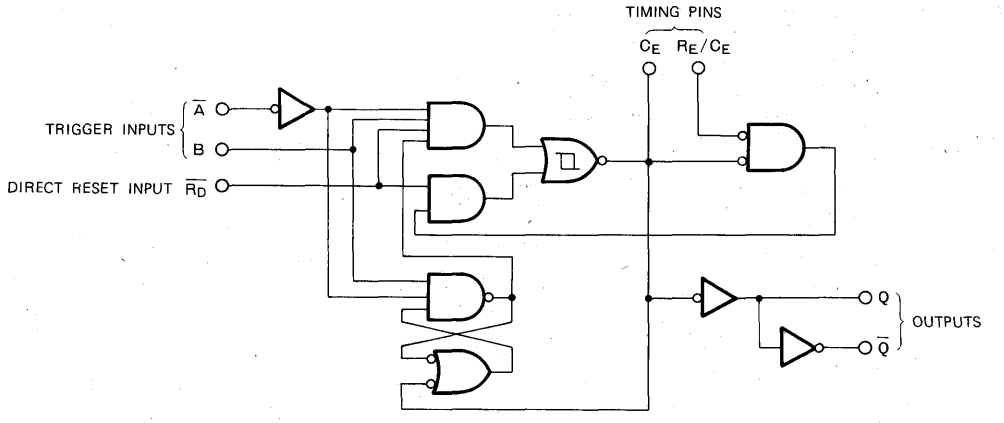
Outline 16P4

FUNCTIONAL DESCRIPTION

Positive pulses appear in output Q and negative pulses in output $\overline{Q}$ by connecting external resistor R_T and electrostatic capacitor C_T to timing pins R_E/C_E and C_E, as shown in Fig. 1, and by applying a trigger from input $\overline{A}$ or B. The width t_w of the pulses appearing in the outputs is set by R_T and C_T. When $\overline{A}$ changes from high to low or when B changes from low to high, the trigger is applied. This IC is able to obtain an output pulse width with excellent supply voltage and temperature characteristics since both its supply voltage and temperature are assured.

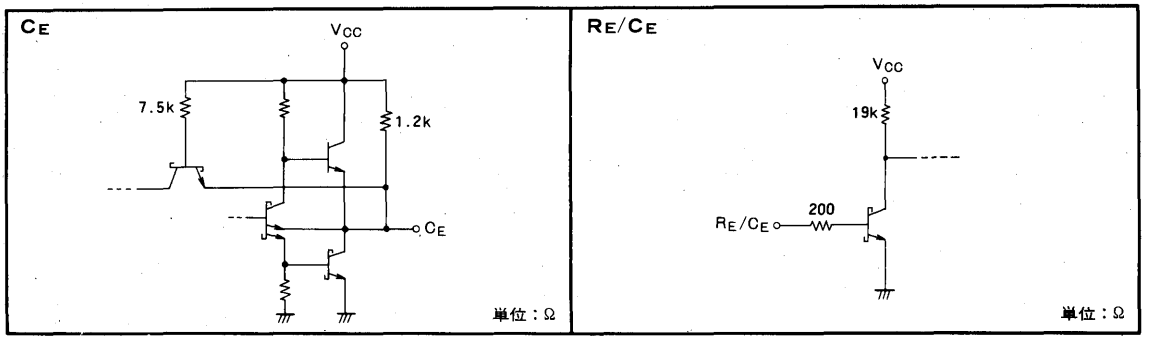
Q can be reset immediately low and $\overline{Q}$ high by setting direct reset input $\overline{R_D}$ low irrespective of the status of the outputs. If $\overline{R_D}$ changes from low to high when $\overline{A}$ is low and B is high, the trigger is applied and the pulse appears in the output.

BLOCK DIAGRAM (EACH MONOSTABLE MULTIVIBRATOR)



MITSUBISHI ELECTRIC

TIMING PIN EQUIVALENT CIRCUIT



FUNCTION TABLE (Note 1)

$\overline{R_D}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

Note 1. ↑ : Transition from low to high.
↓ : Transition from high to low.
⎍: Positive one-shot operation.
⎎: Negative one-shot operation.
X : Irrelevant

OPERATION DESCRIPTION

1. How to use the timing pins

As shown in Fig. 1, external resistor R_T and electrostatic capacitor C_T are connected to timing pins R_E/C_E and C_E. Connect the negative to the R_E/C_E side and the positive to the C_E side when using C_T with polarity.

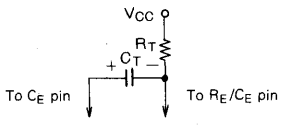


Fig. 1 Connection of external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E

2. Output pulse width t_w

The output pulse width t_w is set using R_T and C_T by the following formula:

$$t_w = C_T \cdot R_T \cdot \ln 2 \ (ns) \times (1 \pm 0.1)$$
$$\simeq 0.7 C_T \cdot R_T \ (ns) \times (1 \pm 0.1)$$

R_T is measured in kiloohms and C_T in picofarads. Individual fluctuations of +10% may occur in products.

Depending on the product, fluctuations in the order of 3/-10% may occur.

3. Precautions with use

In order to minimize the floating capacitance and to safeguard against malfunction caused by noise, make the R_T and C_T wiring as short as possible and avoid signal wires which may be conducive to noise.

Connect a capacitor of 0.01~0.1μF with good high-frequency characteristics between pins V_{CC} and GND. Mount this capacitor as close as possible to the IC.

ABSOLUTE MAXIMUM RATINGS (Ta = −20~+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5~+7	V
V_I	Input voltage		−0.5~+15	V
V_O	Output voltage	High-level state	−0.5~V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20~+75	℃
T_{stg}	Storage temperature range		−65~+150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20~+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA
R_T	External timing resistance		1.4		100	kΩ
C_T	External timing capacitance		0		1000	μF

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage	$\overline{A}$, B					0.8	V
		$\overline{R_D}$					0.5	
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.5, 0.8V$ $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
			$V_I=0.5V, 0.8V, V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current		$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
			$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$\overline{A}$	$V_{CC}=5.25V$				−0.4	mA
		B, $\overline{R_D}$	$V_I=0.4V$				−0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current (static state)		$V_{CC}=5.25V$			4.7	11	mA
	Supply current (one-shot state)		$V_{CC}=5.25V$			19	27	mA

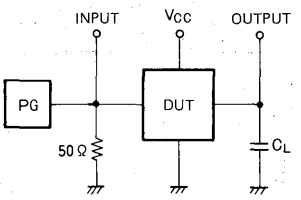
* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
t_{PLH}	Low-to-high-level output propagation time, from input $\overline{A}$ to output Q	$C_T=80pF$ $R_T=2k\Omega$ $C_L=15pF$ (Note 3)			27	70	ns
t_{PLH}	Low-to-high-level output propagation time, from input B to output Q				24	55	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{A}$ to output $\overline{Q}$				30	80	ns
t_{PHL}	High-to-low-level output propagation time, from input B to output $\overline{Q}$				26	65	ns
t_{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output $\overline{Q}$				23	65	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q				18	55	ns
$t_{WQ(min)}$	Minimum output pulse width, from inputs $\overline{A}$, B to outputs Q, $\overline{Q}$	$C_T=0pF$, $R_T=2k\Omega$ $C_L=15pF$ (Note 3)		20	30	70	ns
t_{WQ}	Output pulse width, from inputs $\overline{A}$, B to outputs Q, $\overline{Q}$	$C_L=15pF$ (Note 3)	$C_T=80pF$, $R_T=2k\Omega$	70	120	150	ns
			$C_T=100pF$, $R_T=10k\Omega$	600	670	750	ns
			$C_T=1\mu F$, $R_T=10k\Omega$	6	6.9	7.5	ms

Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR=1MHz, t_r=6ns, t_f=6ns, t_w=40ns,
$V_P=3V_{P\text{-}P}$, $Z_O=50\Omega$

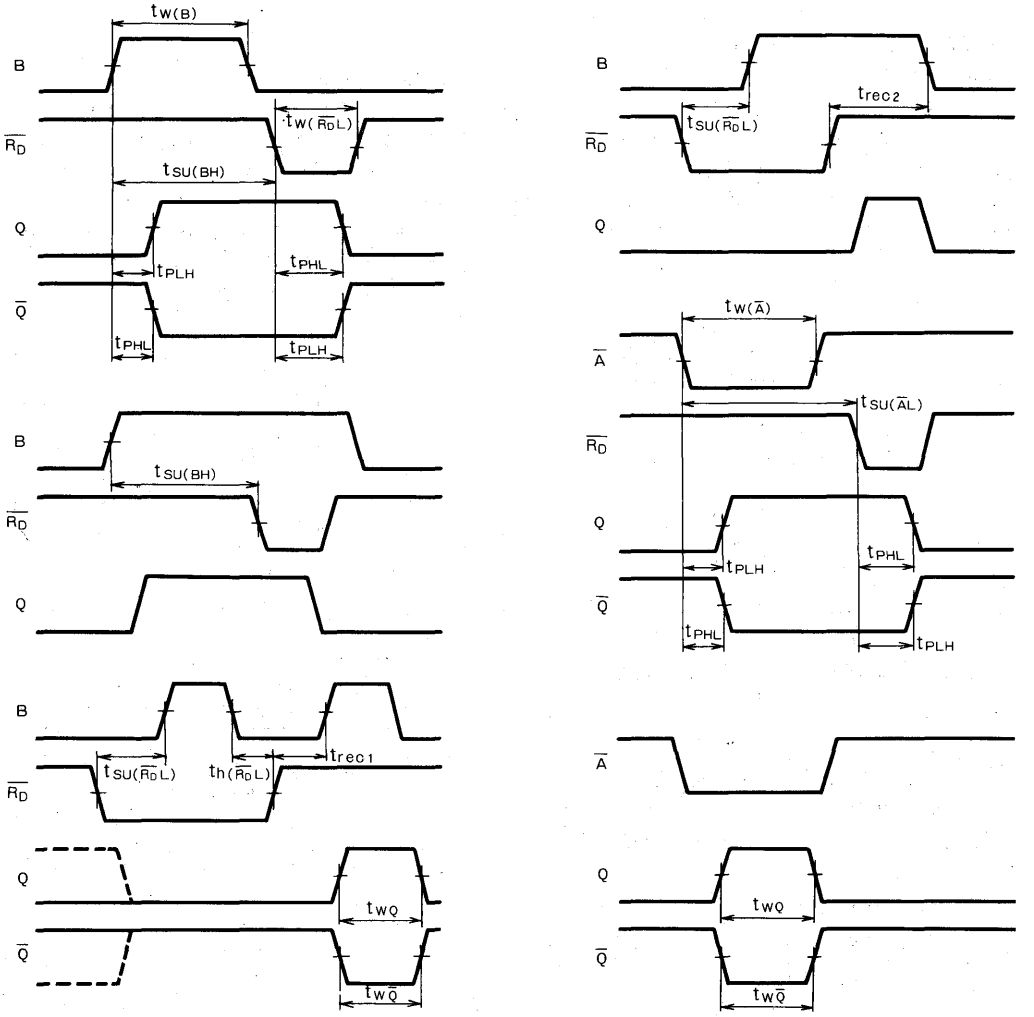
(2) C_L includes probe and jig capacitance

DUAL MONOSTABLE MULTIVIBRATOR

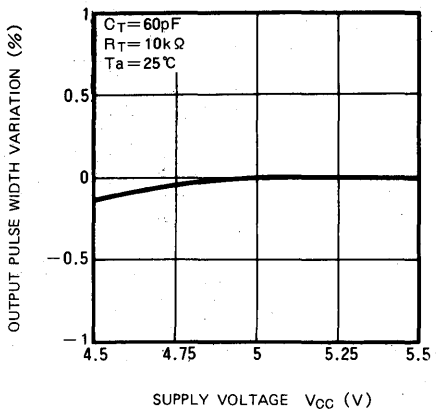
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_r, t_f	Maximum rise, fall voltage rate of input pulse	$\overline{A}$		1			V/μs
		B		1			V/s
$t_{w(\overline{A})}$	Trigger $\overline{A}$ pulse width			40	35		ns
$t_{w(B)}$	Trigger B pulse width			40	35		ns
$t_{w(\overline{R_D})}$	Direct reset input pulse width			40	9		ns
O.D.C	Output duty cycle	R_T=2kΩ	(Note 3)			50	%
		R_T=100kΩ				90	%
$t_{su(\overline{AL})}$	Setup time $\overline{A}$ low to $\overline{R_D}$			60	33		ns
$t_{su(BH)}$	Setup time B high to $\overline{R_D}$			60	25		ns
$t_{su(\overline{R_D}L)}$	Setup time $\overline{R_D}$ low to B			50	15		ns
t_{rec1}	Recovery time			15	−5		ns
t_{rec2}	Recovery time (when B is superimposed onto $\overline{R_D}$)			50	30		ns
$t_{h(\overline{R_D}L)}$	Hold time $\overline{R_D}$ low to B			0	−15		ns

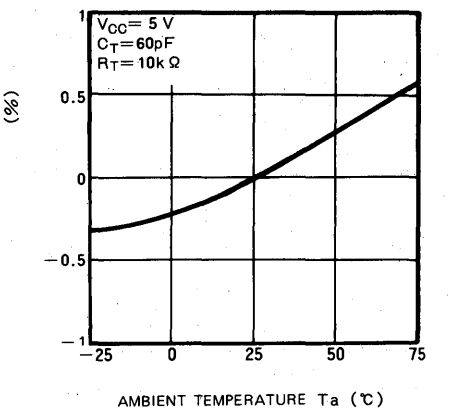
TIMING DIAGRAM (Reference level = 1.3V)



OUTPUT PULSE WIDTH VARIATION VS SUPPLY VOLTAGE



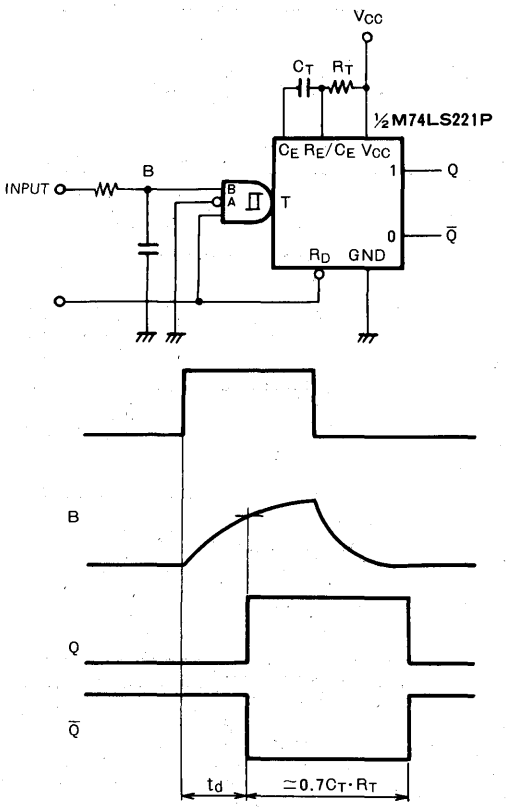
OUTPUT PULSE WIDTH VARIATION VS AMBIENT TEMPERATURE



APPLICATION EXAMPLES

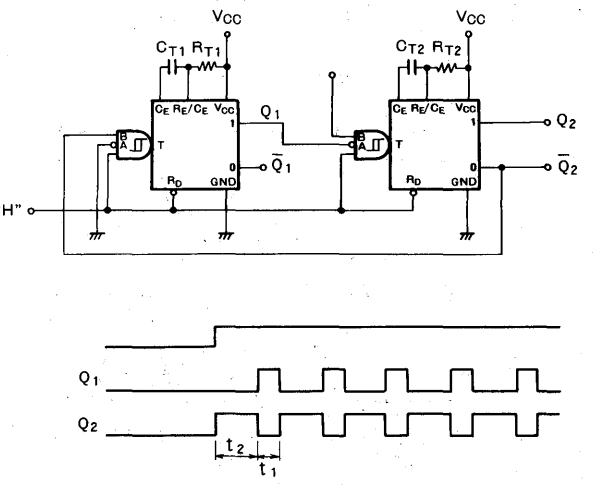
(1) Delay circuit

By connecting an integration circuit to the B input, a rectangular waveform applied to the input is changed to the waveform shown at B and delayed by time t_d. The width of the pulse output at Q and $\overline{Q}$ is determined as usual by the values of C_T, R_T connected externally to the circuit.



(2) Pulse generator

Using the fact that the output pulse width of the M74LS221P varies only slightly with changes in supply voltage and ambient temperature, a pulse generator with good supply voltage and temperature stability can be implemented. By choosing the values of externally connected components C_T and R_T, the duty cycle and frequency can be freely selected.

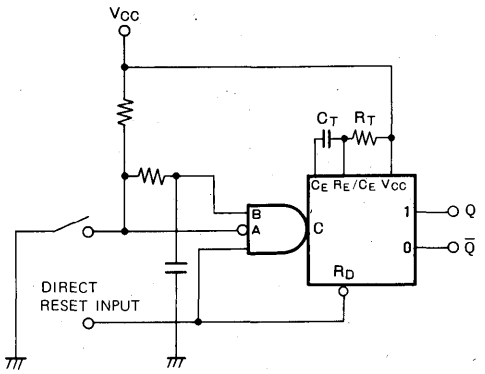


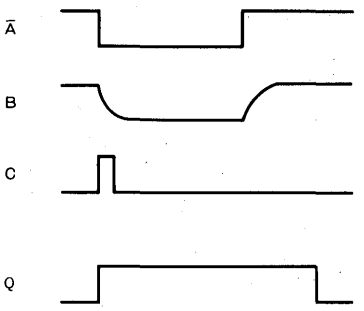
$t_1 \fallingdotseq 0.7C_{T1} \cdot R_{T1}$

$t_2 \fallingdotseq 0.7C_{T2} \cdot R_{T2}$

MITSUBISHI ELECTRIC

(3) ANTI-CHATTERING CIRCUIT





M74LS240P

OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(INVERTED)

DESCRIPTION

The M74LS240P is a semiconductor integrated circuit containing 2 blocks of buffers with 3-state inverted output and common output control input for all 4 discrete circuits.

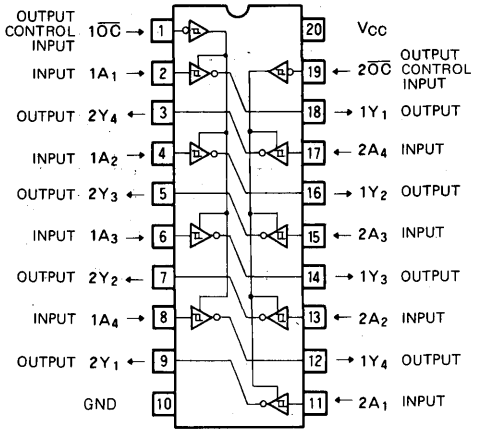
FEATURES

- Small input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High breakdown input voltage ($V_I \geqq 5V$)
- Output control input having same phase for 2 circuits. ($1\overline{OC}$, $2\overline{OC}$)
- High fan-out, 3-state output. (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range. (T_a = −20~ + 75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTIONAL DESCRIPTION

The use of pnp transistors in the input circuits has enabled the achievement of small input load factor and high breakdown input voltage. With hysteresis characteristics, the buffer has a 3-state inverted output with high noise margin. When the output control input $\overline{OC}$ is low, high appears in the output Y if input A is low, and low appears in the Y if A is high. If, on the other hand, $\overline{OC}$ is high, all the outputs Y_1, Y_2, Y_3, and Y_4 are in a high-impedance state, irrespective of the status of A.

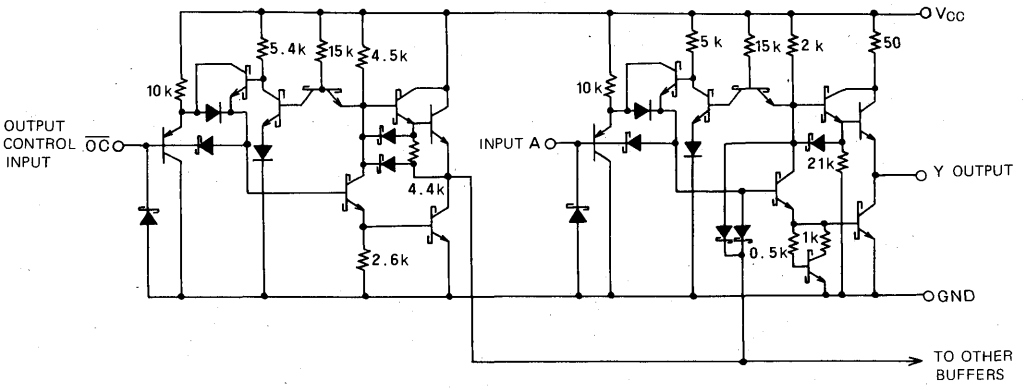
By connecting $1\overline{OC}$ with $2\overline{OC}$, it becomes possible to control the output of the 8 circuits. The output can be terminated with load resistor of 133Ω or over.

FUNCTION TABLE (Note 1)

A	$\overline{OC}$	Y
L	L	H
H	L	L
X	H	Z

Note 1: Z : high-impedance
X : irrelevant

CIRCUIT DIAGRAM (EACH BUFFER)



UNIT: Ω

MITSUBISHI ELECTRIC

OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(INVERTED)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
$V_{T+}-V_{T-}$	Hysteresis	$V_{CC}=4.75V$		0.2	0.4		V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$	$V_I=0.8V$, $I_{OH}=-3mA$	2.4	3.4		V
		$V_I=2V$	$V_I=0.5V$, $I_{OH}=-15mA$	2			V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=12mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$	$I_{OL}=24mA$		0.35	0.5	V
I_{OZH}	Off-state high-level output current	$V_{CC}=5.25V$, $V_I=2V$, $V_O=2.7V$				20	μA
I_{OZL}	Off-state low-level output current	$V_{CC}=5.25V$, $V_I=2V$, $V_O=0.4V$				−20	μA
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.2	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$		−40		−225	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=0V$			17	27	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$			26	44	mA
I_{CCZ}	Supply current, all outputs off	$V_{CC}=5.25V$, $V_I=4.5V$			29	50	mA

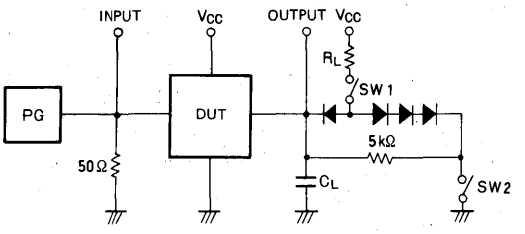
* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input A to output Y	$C_L=45pF$ (Note 3)		7	14	ns
t_{PHL}				9	18	ns
t_{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		15	30	ns
t_{PZH}	Output enable time to high-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		12	40	ns
t_{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		11	25	ns
t_{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		12	18	ns

OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(INVERTED)

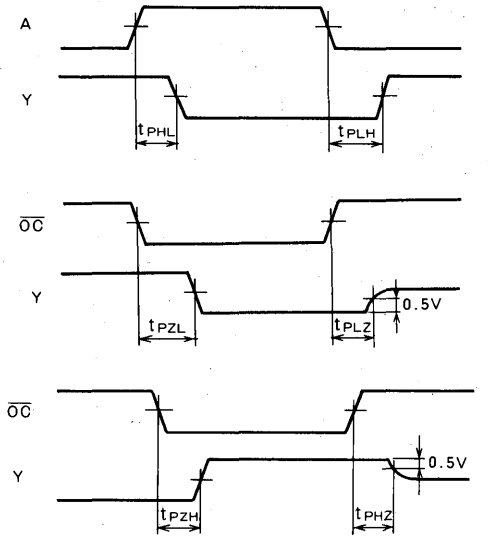
Note 3: Measurement circuit



Parameter	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

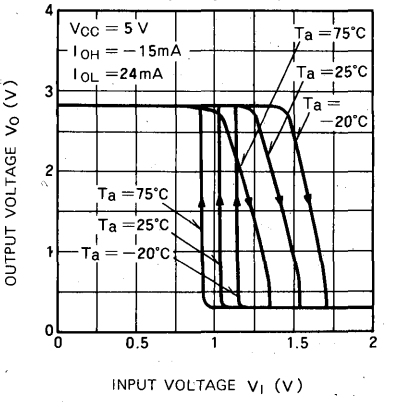
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

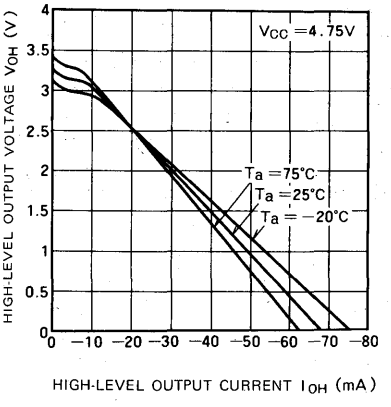


TYPICAL CHARACTERISITCS

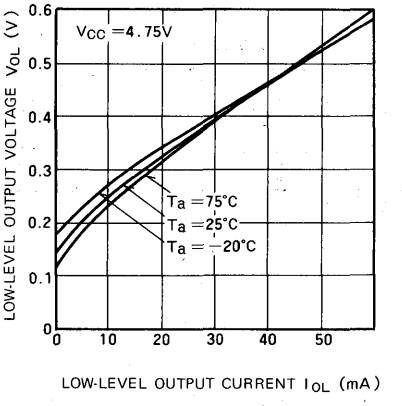
OUTPUT VOLTAGE VS INPUT VOLTAGE



HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



M74LS241P

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74LS241P is a semiconductor integrated circuit containing 2 buffer blocks with 3-state non-inverted outputs and is provided with output control inputs which are common to 4 circuits and which are independent.

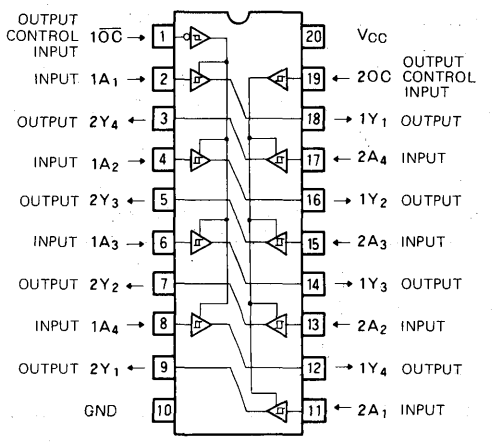
FEATURES

- Small input load factor (pnp input)
- Hysteresis provided (=400mV typical)
- High breakdown input voltage ($V_I \geqq 15V$)
- Complementary output control inputs ($1\overline{OC}$, 2OC)
- High fan-out 3-state outputs (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

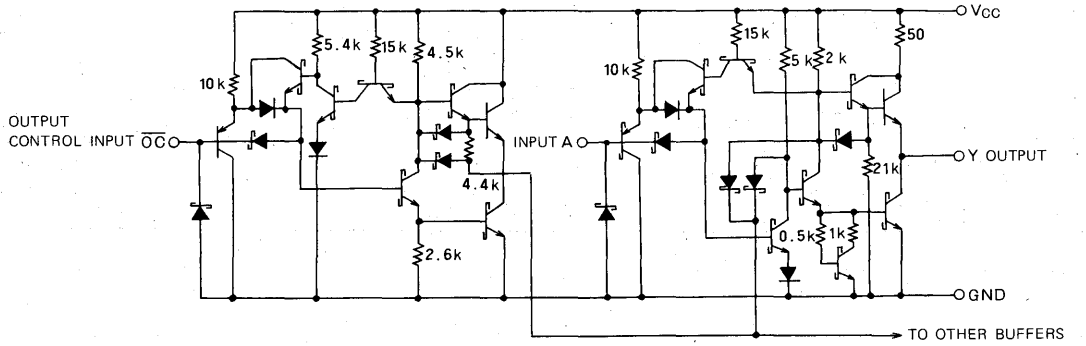
FUNCTIONAL DESCRIPTION

Since pnp transistors are used for the input circuits, the input load factor is small and a high breakdown input voltage is provided. The 3-state non-inverted output buffers have a high noise margin due to hysteresis.

When $1\overline{OC}$ is low, low appears in output Y if input 1A is low, and high appears in Y if 1A is high. When 2OC is high, low appears in output 2Y if input 2A is low and high appears in 2Y if 2A is high. All the outputs are put in a high-impedance state when $1\overline{OC}$ and 2OC are high and low, respectively.

The device can be used as a 4-bit two-way bus driver by connecting $1\overline{OC}$ and 2OC, 1A and 2Y and also 2A and 1Y. The outputs can be terminated with load resistors of not less than 133 ohms.

CIRCUIT DIAGRAM (EACH BUFFER)



UNIT: Ω

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

1A	$1\overline{OC}$	1Y
L	L	L
H	L	H
X	H	Z

2A	2OC	2Y
L	H	L
H	H	H
X	L	Z

Note 1 Z : High-impedance
X : irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
$V_{T+}-V_{T-}$	Hysteresis width	$V_{CC}=4.75V$	0.2	0.4		V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$			−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $I_{OH}=-3mA$	2.4	3.1		V
		$V_I=2V$, $V_I=0.5V$, $I_{OH}=-15mA$	2			V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $I_{OL}=12mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$, $I_{OL}=24mA$		0.35	0.5	V
I_{OZH}	Off-state high-level output current	$V_{CC}=5.25V$, $V_I=2V$, $V_O=2.7V$			20	μA
I_{OZL}	Off-state low-level output current	$V_{CC}=5.25V$, $V_I=2V$, $V_O=0.4V$			−20	μA
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$			20	μA
		$V_{CC}=5.25V$, $V_I=10V$			0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$			−0.2	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$	−40		−225	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$		17	27	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$		27	46	mA
I_{CCZ}	Supply current, all outputs disabled	$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$		32	54	mA

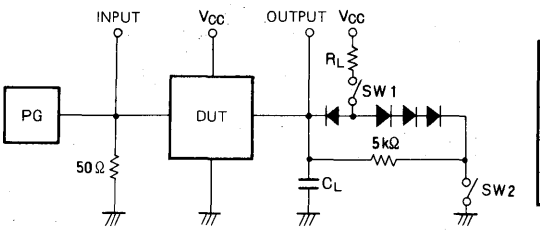
* : All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input A to output Y	C_L=45pF (Note 3)		8	18	ns
t_{PHL}				9	18	ns
t_{PZL}	Output enable time to low-level	R_L=667Ω, C_L=45pF (Note 3)		15	30	ns
t_{PZH}	Output enable time to high-level	R_L=667Ω, C_L=45pF (Note 3)		12	40	ns
t_{PLZ}	Output disable time from low-level	R_L=667Ω, C_L= 5 pF (Note 3)		11	25	ns
t_{PHZ}	Output disable time from high-level	R_L=667Ω C_L= 5 pF (Note 3)		12	18	ns

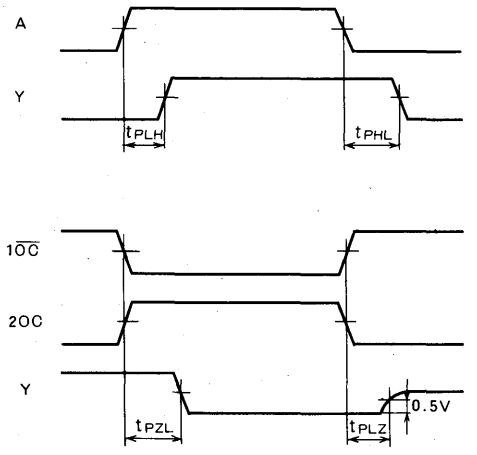
Note 3: Measurement circuit

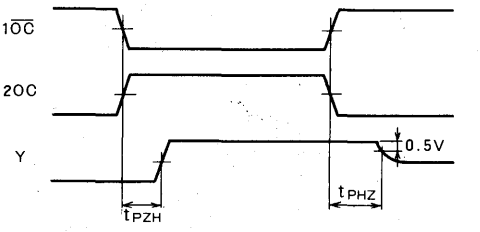


Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P\text{-}P}$, Z_o = 50Ω.
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

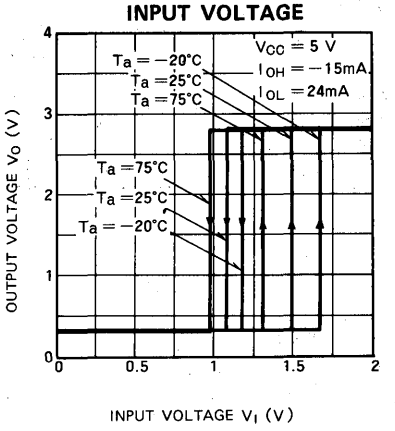




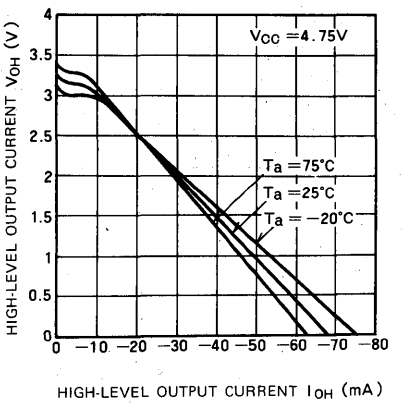
OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

TYPICAL CHARACTERISTICS

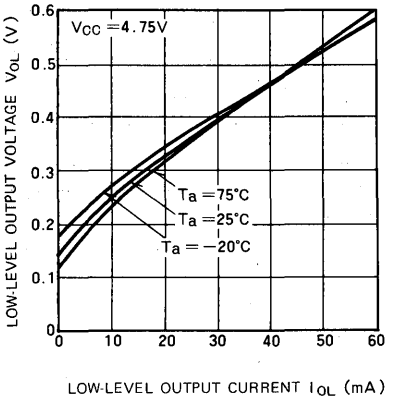
OUTPUT VOLTAGE VS INPUT VOLTAGE



HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



M74LS242P

QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS242P is a semiconductor integrated circuit containing 4 bus transmitters/receivers circuit with 3-state inverted outputs.

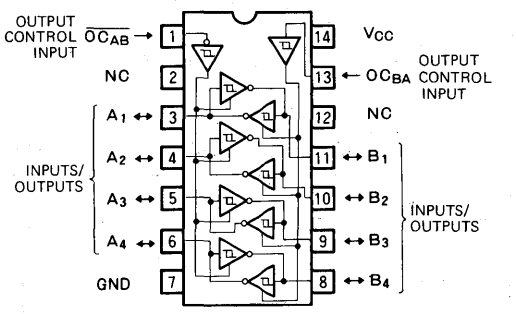
FEATURES

- Two-way transmission for, or isolation from, two 4-bit data words
- Low input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High fan-out (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC : NO CONNECTION

FUNCTIONAL DESCRIPTION

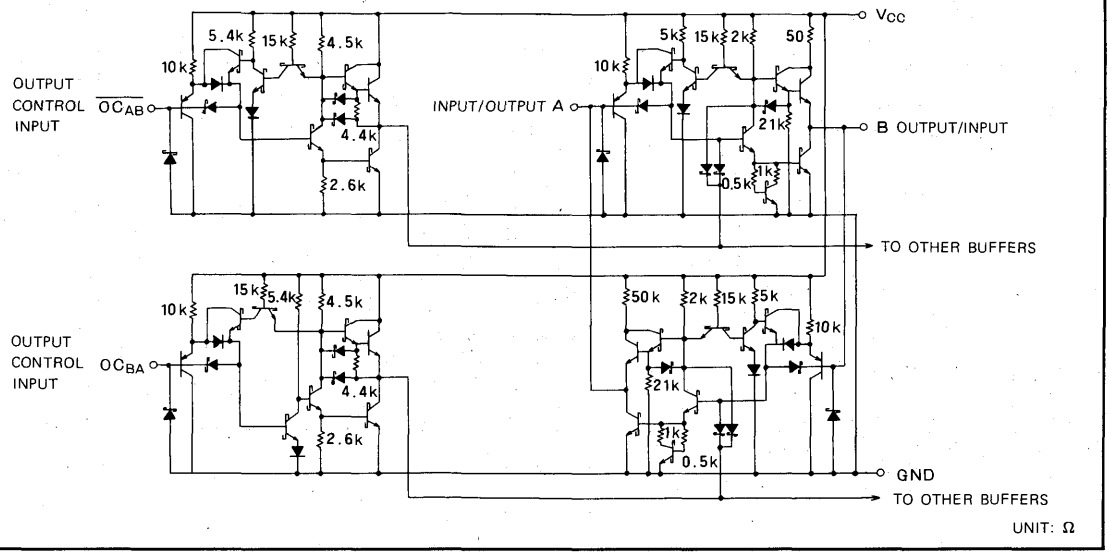
In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with the 3-state inverted outputs are made two-way buffers.

Since the input section is provided with hysteresis, the noise margin is increased and the use of pnp transistors in the inputs reduces the input load factor.

The input/output direction is controlled by $\overline{OC_{AB}}$ and OC_{BA}. When $\overline{OC_{AB}}$ and OC_{BA} are low, input/output pins A are made the input pins and the output/input pins B are made the output pins. When $\overline{OC_{AB}}$ and OC_{BA} are high, pins B are made the input pins and A the output pins. When $\overline{OC_{AB}}$ is high and OC_{BA} is high and OC_{BA} is low, both A and B are put in the high-impedance state and A and B are isolated. When $\overline{OC_{AB}}$ is low and OC_{BA} is high, both A and B are put to the output state resulting in the possibility of oscillation and damage to the IC. Use in this state must therefore be avoided. This state resulting from the $\overline{OC_{AB}}$ and OC_{BA} signals should be kept as short as possible. Termination is possible with a load resistor of not less than 133 ohms.

Refer to M74LS240P for the typical characteristics.

CIRCUIT DIAGRAM (EACH BUFFER)



QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

$\overline{OC_{AB}}$	OC_{BA}	A	B
H	H	$\overline{O}$	I
L	H	*	*
H	L	Z	Z
L	L	I	$\overline{O}$

Note 1: I : Input pin
$\overline{O}$: Output pin (inverted)
* : Inhibited (A and B are made output pins)
Z : High-impedance (A, B are isolated)

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +5.5	V
		$\overline{OC_{AB}}$, OC_{BA}		−0.5 ~ +15	V
V_O	Output voltage		Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
$V_{T+}-V_{T-}$	Hysteresis width		V_{CC}=4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V, I_{OH}=−3mA		2.4	3.1		V
			V_{CC}=4.75V, V_I=2V, I_{OH}=−15mA		2			V
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V	I_{OL}=12mA		0.25	0.4	V
				I_{OL}=24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.25V, V_I=0.8V, V_I=2V, V_O=2.7V				40	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.25V, V_I=0.8V, V_I=2V, V_O=0.4V				−200	μA
I_{IH}	High-level input current	A, B	V_{CC}=5.25V, V_I=2.7V				20	μA
		$\overline{OC_{AB}}$, OC_{BA}					20	
		A, B	V_{CC}=5.25V, V_I=5.5V				0.1	mA
		$\overline{OC_{AB}}$, OC_{BA}	V_{CC}=5.25V, V_I=10V				0.1	
I_{IL}	Low-level input current	$\overline{OC_{AB}}$, OC_{BA}	V_{CC}=5.25V, V_I=0.4V				−0.2	mA
		A		$\overline{OC_{AB}}$=OC_{BA}=0V			−0.2	
		B		$\overline{OC_{AB}}$=OC_{BA}=4.5V			−0.2	
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−40		−225	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.25V, V_I=0V, V_I=4.5V			22	38	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.25V, V_I=0V, V_I=4.5V			29	50	mA
I_{CCZ}	Supply current, all outputs off		V_{CC}=5.25V, V_I=0V, V_I=4.5V			29	50	mA

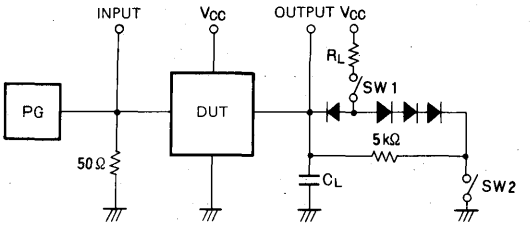
* : All typical values are at V_{CC}=5V, Ta=25°C.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs A, B to outputs B, A	C_L=45pF (Note 3)		7	14	ns
t_{PHL}				9	18	ns
t_{PZL}	Output disable time from low-level	R_L=667Ω, C_L=45pF (Note 3)		15	40	ns
t_{PZH}	Output enable time to high-level	R_L=667Ω, C_L=45pF (Note 3)		12	40	ns
t_{PLZ}	Output enable time to low-level	R_L=667Ω, C_L= 5 pF (Note 3)		11	25	ns
t_{PHZ}	Output disable time from high-level	R_L=667Ω C_L= 5 pF (Note 3)		12	18	ns

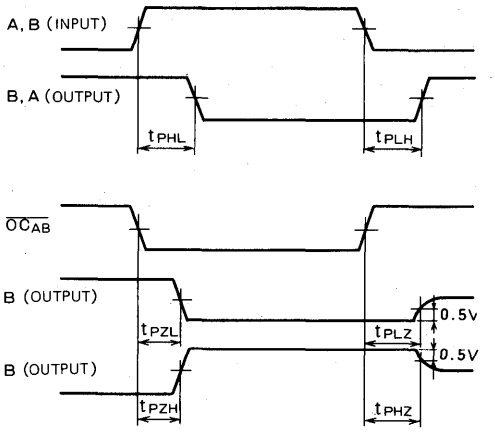
Note 3: Measurement circuit

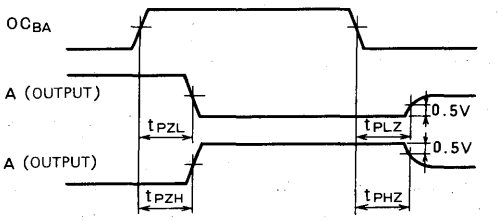


Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)





M74LS243P

QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74LS243P is a semiconductor integrated circuit containing 4 bus transmitters/receivers with 3-state non-inverted outputs.

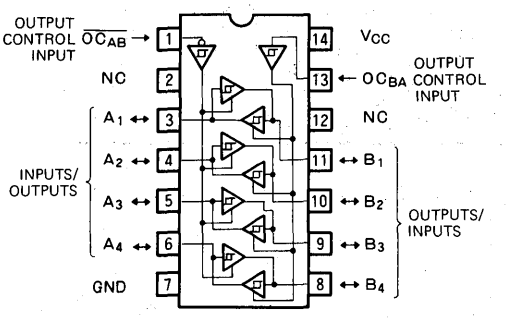
FEATURES

- Two-way transmission for, or isolation from, two 4-bit data words
- Low input load factor (pnp input)
- Hysteresis provided (= 400 mV typical)
- High fan-out (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC : NO CONNECTION

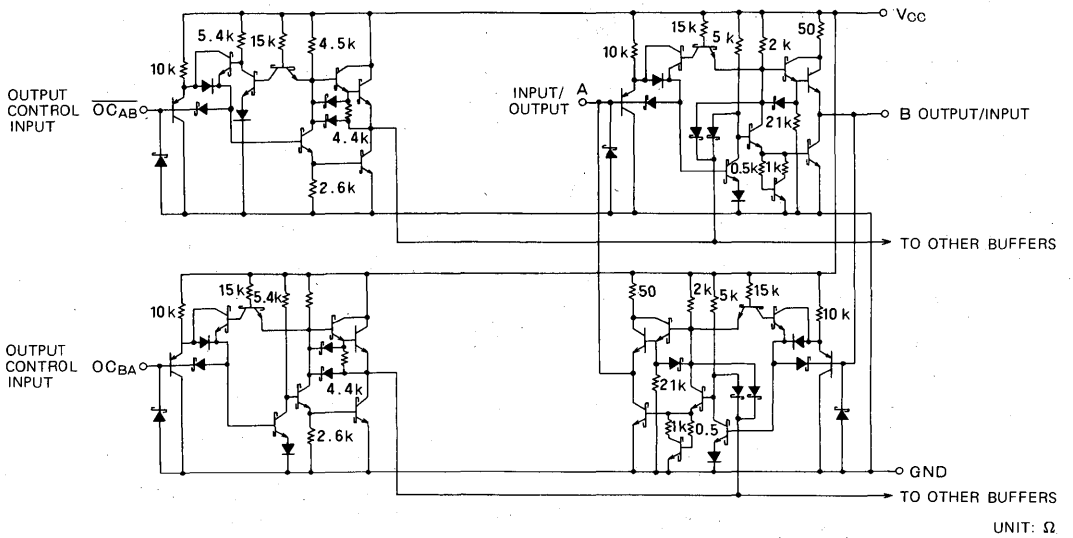
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with the 3-state non-inverted outputs are made two-way buffers.

Since the input section is provided with hysteresis, the noise margin is increased and the use of pnp transistors in the inputs reduces the input load factor.

The input/output direction is controlled by $\overline{OC_{AB}}$ and OC_{BA}. When $\overline{OC_{AB}}$ and OC_{BA} are low, input/output pins A are made the input pins and the output/input pins B are made the output pins. When $\overline{OC_{AB}}$ and OC_{BA} are high, pins B are made the input pins and A the output pins. When $\overline{OC_{AB}}$ is high and OC_{BA} is low, both A and B are put in the high-impedance state and A and B are isolated. When $\overline{OC_{AB}}$ is low and OC_{BA} is high, both A and B are put to the output state resulting in the possibility of oscillation and damage to the IC. Use in this state must therefore be avoided. This state resulting from the $\overline{OC_{AB}}$ and OC_{BA} signals should be kept as short as possible. Termination is possible with a load resistor of not less than 133 ohms. Refer to M74LS241P for the typical characteristics.

CIRCUIT DIAGRAM (EACH BUFFER)



MITSUBISHI ELECTRIC

QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

$\overline{OC_{AB}}$	OC_{BA}	A	B
H	H	O	I
L	H	*	*
H	L	Z	Z
L	L	I	O

Note 1: I : Input pin
O : Output (non-inverted) pin
* : Inhibited (A and B are made output pins)
Z : High-impedance (A, B are isolated)

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +5.5	V
		$\overline{OC_{AB}}$, OC_{BA}		−0.5 ~ +15	V
V_O	Output voltage		Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
$V_{T+}-V_{T-}$	Hysteresis width		$V_{CC}=4.75V$		0.2	0.4		V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$	$I_{OH}=-3mA$	2.4	3.1		V
			$V_I=2V$	$I_{OH}=-15mA$	2			V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=12mA$		0.25	0.4	V
			$V_I=0.8V$, $V_I=2V$	$I_{OL}=24mA$		0.35	0.5	V
I_{OZH}	Off-stage high-level output current		$V_{CC}=5.25V$, $V_I=0.8V$, $V_I=2V$, $V_O=2.7V$				40	μA
I_{OZL}	Off-state low-level output current		$V_{CC}=5.25V$, $V_I=0.8V$, $V_I=2V$, $V_O=0.4V$				−200	μA
I_{IH}	High-level input current	A, B	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{OC_{AB}}$, OC_{BA}					20	
		A, B	$V_{CC}=5.25V$, $V_I=5.5V$				0.1	mA
		$\overline{OC_{AB}}$, OC_{BA}	$V_{CC}=5.25V$, $V_I=10V$				0.1	
I_{IL}	Low-level input current	$\overline{OC_{AB}}$, OC_{BA}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.2	mA
		A		$\overline{OC_{AB}}=OC_{BA}=0V$			−0.2	
		B		$\overline{OC_{AB}}=OC_{BA}=4.5V$			−0.2	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−40		−225	mA
I_{CCH}	Supply current, all output high		$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$			22	38	mA
I_{CCL}	Supply current, all outputs low		$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$			29	50	mA
I_{CCZ}	Supply current, all outputs off		$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$			32	54	mA

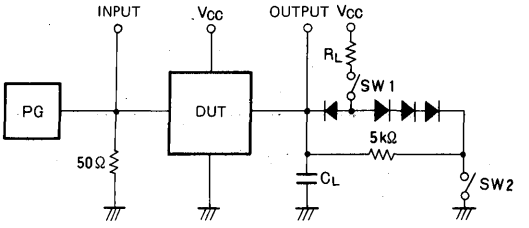
* : All typical values are at $V_{CC}=5V$, $Ta=25°C$.
Note 2: All measurements should be done quickly and not more than one outputs should be shorted at a time.

QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs A, B to outputs B, A	C_L = 45pF (Note 3)		8	18	ns
t_{PHL}				9	18	ns
t_{PZH}	Output enable time to high-level	R_L = 667Ω, C_L = 45pF (Note 3)		15	40	ns
t_{PZL}	Output enable time to low-level	R_L = 667Ω, C_L = 45pF (Note 3)		12	40	ns
t_{PLZ}	Output disable time from low-level	R_L = 667Ω, C_L = 5 pF (Note 3)		11	25	ns
t_{PHZ}	Output disable time from high-level	R_L = 667Ω C_L = 5 pF (Note 3)		12	18	ns

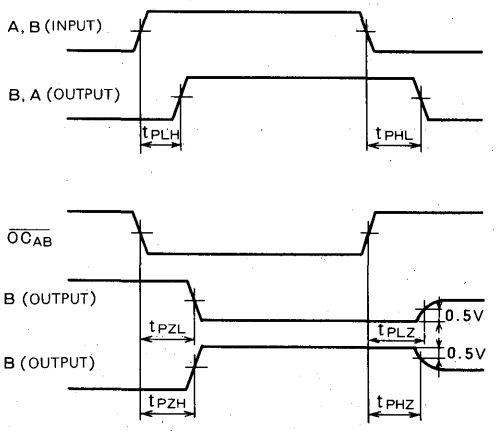
Note 3: Measurement circuit

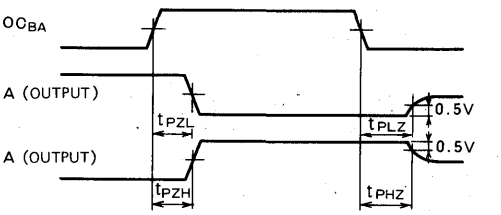


Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, Z_O = 50Ω
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns).
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)





M74LS244P

OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

DESCRIPTION

The M74LS244P is a semiconductor integrated circuit containing 2 blocks of buffers with 3-state non-inverted output and common output controlling input for all 4 discrete circuits.

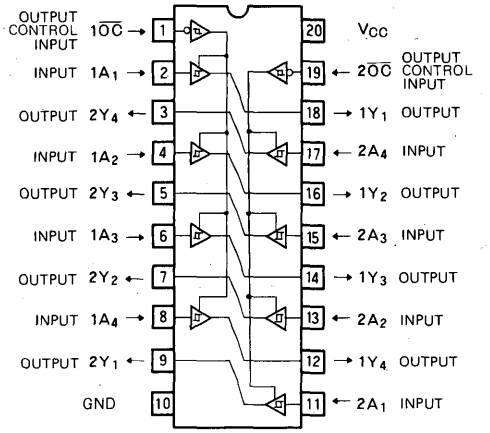
FEATURES

- Low input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High breakdown input voltage ($V_I \geqq 15V$)
- Output control input having same phase for 2 circuits
- High fan-out, 3-state output
  (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTIONAL DESCRIPTION

The use of pnp transistors in the input circuit has enabled the achievement of small input load factor. With hysteresis characteristics, the buffer has a 3-state noninverted output with high noise margin.

When output control input $\overline{OC}$ is low, the output Y is low if input A is low and Y is high if A is high. When $\overline{OC}$ is high, all of Y_1, Y_2, Y_3, and Y_4 are in the high-impedance state, irrespective of the status of A.

By connecting $1\overline{OC}$ with $2\overline{OC}$, it becomes possible to control the output of all 8 circuits simultaneously. Output can be terminated by a load resistor of 133Ω or over.

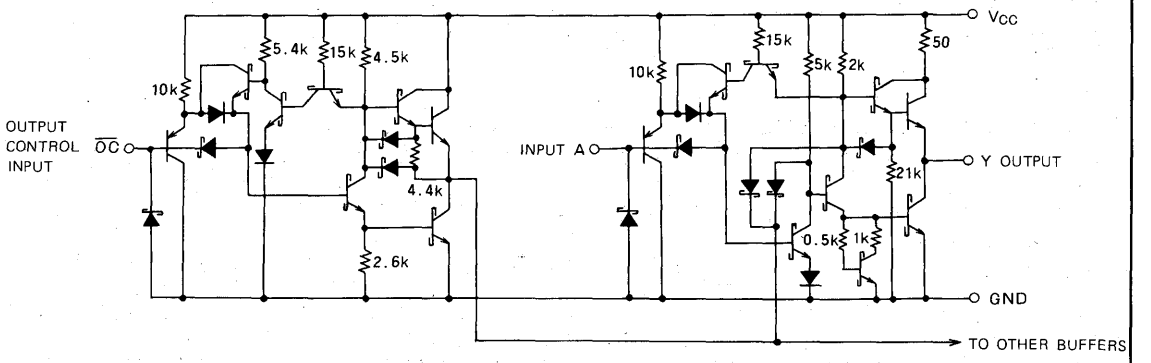
For standard characteristics, see M74LS241P.

FUNCTION TABLE (Note 1)

A	$\overline{OC}$	Y
L	L	L
H	L	H
X	H	Z

Note 1: Z : high-impedance
X : irrelevant

CIRCUIT DIAGRAM (EACH BUFFER)



UNIT: Ω

OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$			−3	mA
		$V_{OH} \geqq 2V$			−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$			12	mA
		$V_{OL} \leqq 0.5V$			24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC}=4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V	V_I=0.8V, I_{OH}=−3mA	2.4	3.4		V
		V_I=2V	V_I=0.5V, I_{OH}=−15mA	2			V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}=12mA		0.25	0.4	V
		V_I=0.8V, V_I=2V	I_{OL}=24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current	V_{CC}=5.25V, V_I=2V, V_O=2.7V				20	μA
I_{OZL}	Off-state low-level output current	V_{CC}=5.25V, V_I=2V, V_O=0.4V				−20	μA
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.2	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC}=5.25V, V_O=0V		−40		−225	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.25V, V_I=0V, V_I=4.5V			17	27	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.25V, V_I=0V			27	46	mA
I_{CCZ}	Supply current, all outputs off	V_{CC}=5.25V, V_I=4.5V			32	54	mA

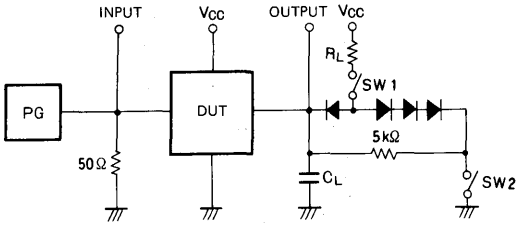
* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input A to output Y	C_L=45pF (Note 3)		8	18	ns
t_{PHL}				9	18	ns
t_{PZH}	Output enable time to high-level	R_L=667Ω, C_L=45pF (Note 3)		15	30	ns
t_{PZL}	Output enable time to low-level	R_L=667Ω, C_L=45pF (Note 3)		12	40	ns
t_{PLZ}	Output disable time from low-level	R_L=667Ω, C_L= 5 pF (Note 3)		11	25	ns
t_{PHZ}	Output disable time from high-level	R_L=667Ω, C_L= 5 pF (Note 3)		12	18	ns

OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

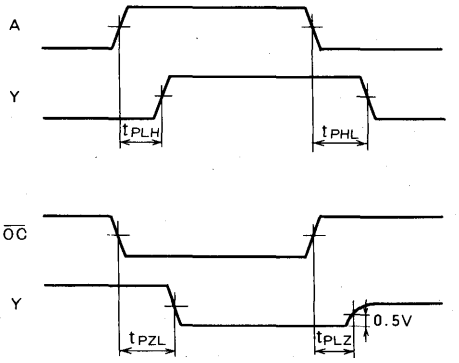
Note 3: Measurement circuit

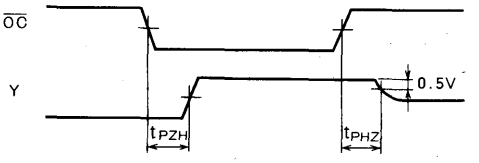


Symbol	SW 1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, $V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)





M74LS245P

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

DESCRIPTION

The M74LS245P is a semiconductor integrated circuit containing of 8 bus transmitter/receiver circuits with non-inverted outputs.

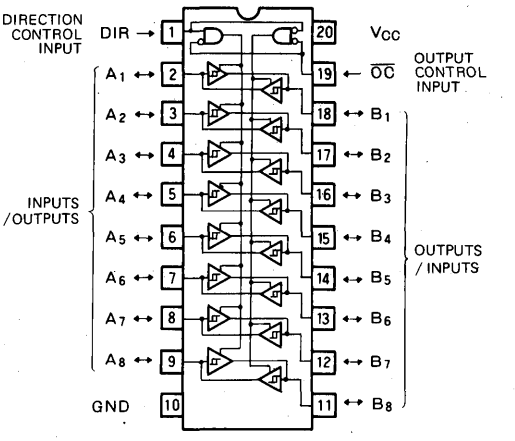
FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Low input load factor (pnp input)
- Input/output A and output/input B have hysteresis characteristics (Hysteresis = 400mV typical)
- High fan-out (I_{OL} = 24mA, I_{OH} = -15mA)
- Wide operating temperature range. (T_a = -20 ~ +75°C)

APPLICATION

General digital equipment for industrial and consumer use

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTIONAL DESCRIPTION

The inputs and outputs of the two buffer circuits with 3-state non-inverted outputs are connected alternately to form a bi-directional buffer.

With hysterisis characteristics in the input section of input/output A and output/input B, noise margin is high. The use of a pnp transistor input has made the input load factor small. The data direction control input DIR controls the direction of input and output. When DIR is high, A is the input terminal and B is the output terminal. On the contrary, when DIR is low, B is the input terminal and A is the output terminal.

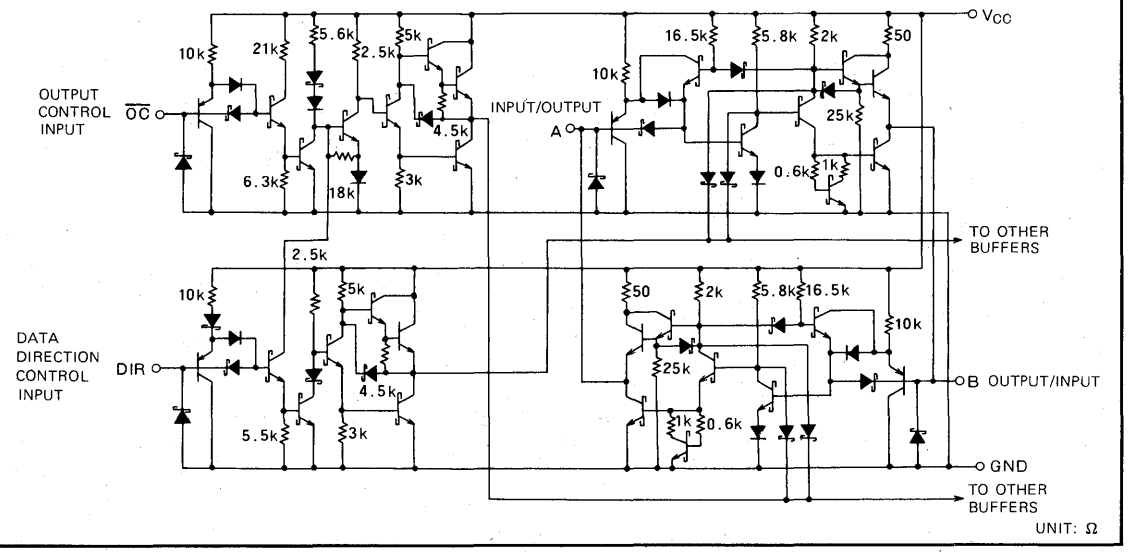
When the output control input $\overline{OC}$ is high, both A and B, in a high-impedance state, are separated.

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

Note 1: I : input
O : output (noninverted output)
Z : high-impedance
X : irrelevant

CIRCUIT DIAGRAM (EACH BUFFER)



MITSUBISHI ELECTRIC

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +5.5	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	℃
Tstg	Storage temperature range			−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
$V_{T+} - V_{T-}$	Hystersis		V_{CC} = 4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V	I_{OH} = −3mA	2.4	3.4		V
			V_I = 0.8V, V_I = 2V	I_{OH} = −15mA	2			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V	I_{OL} = 12mA			0.4	V
			V_I = 0.8V, V_I = 2V	I_{OL} = 24mA			0.5	V
I_{OZH}	Off-state high-level output current		V_{CC} = 5.25V, V_I = 0.8V, V_I = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC} = 5.25V, V_I = 0.8V, V_I = 2V, V_O = 0.4V				−200	μA
I_{IH}	High-level input current	A, B	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC} = 5.25V, V_I = 5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current		V_{CC} = 5.25V, V_I = 0.4V				−0.2	mA
I_{OS}	Short-circuit output current (Note 2)		V_{CC} = 5.25V, V_O = 0 V		−40		−225	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.25V, V_I = 0 V, V_I = 4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = 5.25V, V_I = 0 V, V_I = 4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC} = 5.25V, V_I = 0 V, V_I = 4.5V			64	95	mA

∗ : All typical values are at V_{CC} = 5V, Ta = 25°C.

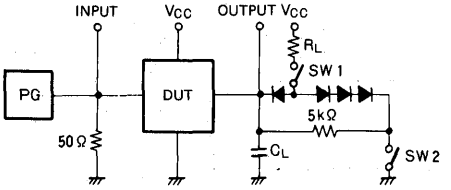
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25℃ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input A, B to output B, A	C_L = 45pF (Note 3)		10	15	ns
t_{PHL}				10	15	ns
t_{PZL}	Output enable time to low-level	R_L = 667Ω, C_L = 45pF (Note 3)		25	40	ns
t_{PZH}	Output enable time to high-level	R_L = 667Ω, C_L = 45pF (Note 3)		23	40	ns
t_{PLZ}	Output disable time from low-level	R_L = 667Ω, C_L = 5pF (Note 3)		15	25	ns
t_{PHZ}	Output disable time from high-level	R_L = 667Ω, C_L = 5pF (Note 3)		14	25	ns

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS(NONINVERTED)

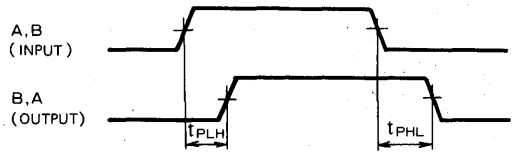
Note 3: Measurement circuit

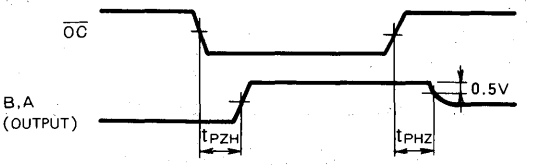


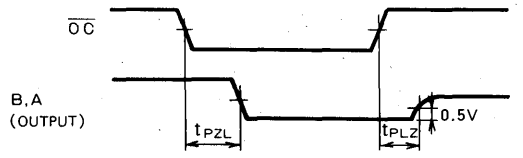
Symbol	SW 1	SW 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

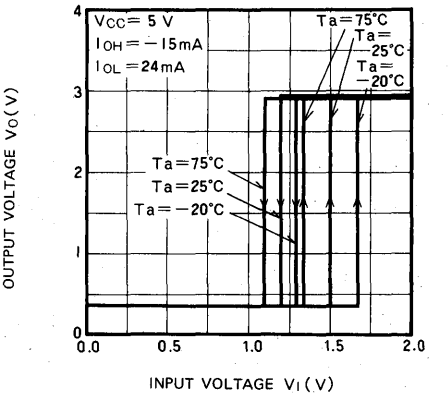




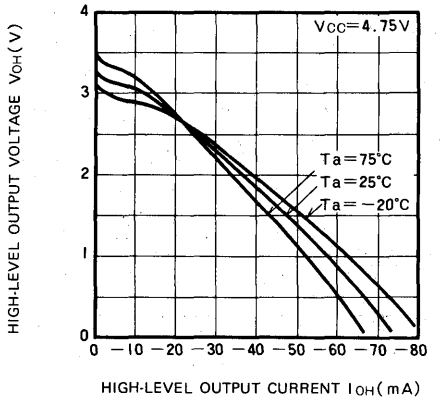


TYPICAL CHARACTERISTICS

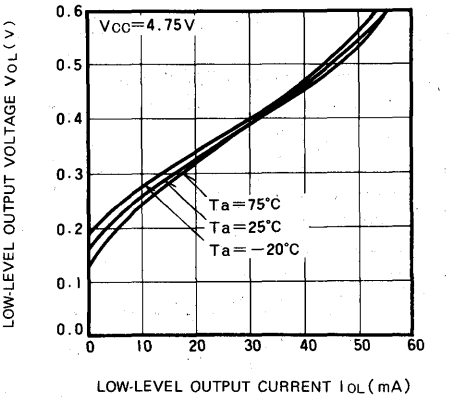
OUTPUT VOLTAGE VS INPUT VOLTAGE



HIGH-LEVEL OUTPUT VOLTAGE VS HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE VS LOW-LEVEL OUTPUT CURRENT



M74LS247P

BCD-TO-7-SEGMENT DECODER/DRIVER(ACTIVE-LOW OUTPUT)

DESCRIPTION

The M74LS247P is a semiconductor integrated circuit provided with BCD-to-7-segment decoder/driver function and open collector outputs.

FEATURES

- Suitable for 7-segment display element lighting
- $\overline{RBI}$ input and $\overline{BI}/\overline{RBO}$ outputs for zero suppression
- $\overline{LT}$ input for lamp testing
- $\overline{BI}/\overline{RBO}$ input for extinguishing all segments
- Open collector outputs
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

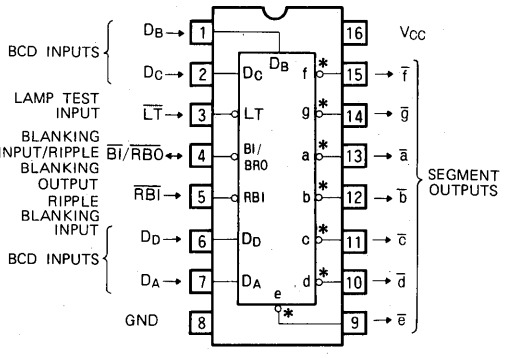
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When a number is specified in BCD code for BCD inputs D_A, D_B, D_C and D_D, segment ouputs $\overline{a}$~$\overline{g}$ are set low in accordance with that number. By connecting the 7-segment display element to each of the outputs, the character indicated on the display character can be displayed. $\overline{a}$~$\overline{g}$ are open collector outputs with a breakdown voltage of not less than 15V and a low-level output current of 24mA, therby making it possible to drive directly a 7-segment LED for the display of anode-common numbers.

Suppression of the unnecessary high-order zeroes is possible by setting the highest order $\overline{RBI}$ ripple blanking input low and connecting ripple blanking output $\overline{BI}/\overline{RBO}$ to the next-level $\overline{RBI}$ for each of the digits. Refer to the M74LS47P for the application example.

PIN CONFIGURATION (TOP VIEW)



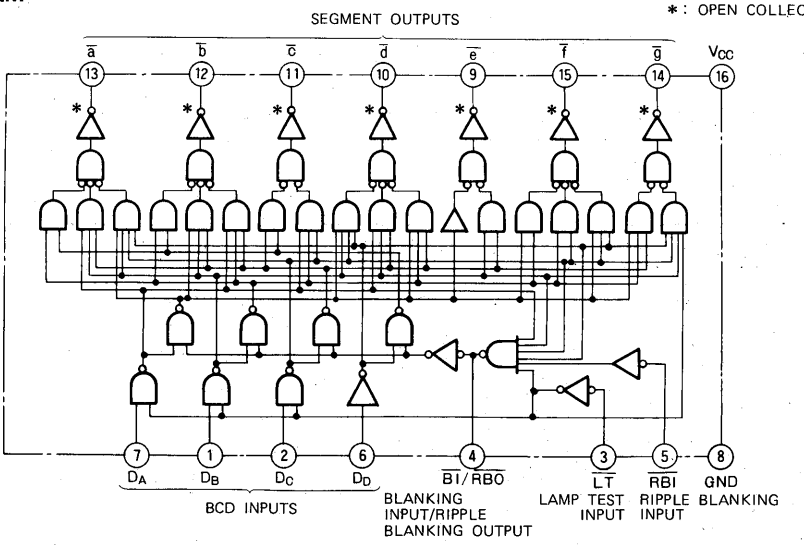
Outline 16P4

By setting blanking input $\overline{BI}/\overline{RBO}$ low, outputs $\overline{a}$~$\overline{g}$ are set high and the display element is extinguished irrespective of the status of the other inputs. Since $\overline{BI}/\overline{RBO}$ serves as both an input and output pin, only ICs with open collector outputs can be connected to this pin.

By setting lamp test input $\overline{LT}$ low, $\overline{a}$~$\overline{g}$ are set low irrespective of the status of $\overline{BI}/\overline{RBO}$, D_A, D_B, D_C and D_D, all the segments in the display element are lighted and each segment can be tested. Refer to M74LS47P for the $\overline{BI}/\overline{RBO}$ and a~g circuits.

The only difference between the M74LS247P and M74LS47P is the configuration of the 6 and 9 numerals.

BLOCK DIAGRAM



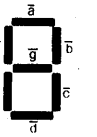
BCD-TO-7-SEGMENT DECODER/DRIVER(ACTIVE-LOW OUTPUT)

FUNCTION TABLE (Note 1)

Decimal number or function	$\overline{LT}$	$\overline{RBI}$	D_D	D_C	D_B	D_A	$\overline{BI}/\overline{RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	Note
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(1)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	L	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	L	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
Blanking	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(2)
Ripple blanking	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(3)
Lamp test	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(4)

Note 1. (1) $\overline{LT}$ is normally kept in high.
$\overline{RBI}$ is kept open or in high with a decimal 0 output.
(2) When $\overline{BI}/\overline{RBO}$ is low, all the segment outputs are high irrespective of the status of the other inputs.
(3) All the segment outputs are set high and $\overline{BI}/\overline{RBO}$ is set low when $\overline{RBI}$, D_A, D_B, D_C and D_D are set low with $\overline{LT}$ high.
(4) When $\overline{LT}$ is low, all the segment outputs are low.
X: Irrelevant

DEFINITION OF SEGMENTS



CHARACTERS DISPLAYED

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Character	0	1	2	3	4	5	6	7	8	9	c	ɔ	u	⊆	t	

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5~+7	V
V_I	Input voltage	Input $\overline{BI}/\overline{RBO}$		−0.5~V_{CC}	V
		Other inputs		−0.5 ~ +15	V
V_O	Output voltage	Output $\overline{BI}/\overline{RBO}$	High-level state	−0.5~V_{CC}	V
		Other outputs		−0.5 ~ +15	V
$I_{O(peak)}$	Output current		tw≦1ms, dutycycle≦10%	200	mA
I_O	Output current		High-level state	1	mA
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current, outputs $\overline{a}$ ~ $\overline{g}$	V_{OH} = 15V	0		250	μA
I_{OH}	High-level output current, output $\overline{BI}/\overline{RBO}$	V_{OH}≧2.4V	0		−50	μA
I_{OL}	Low-level output current, outputs $\overline{a}$~$\overline{g}$	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		24	mA
I_{OL}	Low-level output current, output $\overline{BI}/\overline{RBO}$	V_{OL}≦0.4V	0		1.6	mA
		V_{OL}≦0.5V	0		3.2	mA

BCD-TO-7-SEGMENT DECODER/DRIVER(ACTIVE-LOW OUTPUT)

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +70°C$, unless otherwise noted)

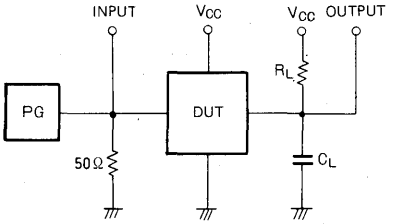
Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage, output $\overline{BI}/\overline{RBO}$		$V_{CC}=4.75V$	$I_{OH}=-50\mu A$	2.4	4.2		V
I_{OH}	High-level output current, outputs $\bar{a} \sim \bar{g}$		$V_I=0.8V$, $V_I=2V$	$V_O=15V$			250	μA
V_{OL}	Low-level output voltage	Outputs $\bar{a} \sim \bar{g}$	$V_{CC}=4.75V$ $V_I=0.8V$, $V_I=2V$	$I_{OL}=12mA$		0.25	0.4	V
				$I_{OL}=24mA$		0.35	0.5	V
		Output $\overline{BI}/\overline{RBO}$		$I_{OL}=1.6mA$		0.25	0.4	V
				$I_{OL}=3.2mA$		0.35	0.5	V
I_{IH}	High-level input voltage, except input $\overline{BI}/\overline{RBO}$		$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
			$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	Input $\overline{BI}/\overline{RBO}$	$V_{CC}=5.25V$, $V_I=0.4V$				−1.2	mA
		Other inputs					−0.4	mA
I_{OS}	Short-circuit output current, output $\overline{BI}/\overline{RBO}$		$V_{CC}=5.25V$, $V_O=0V$		−0.3		−2	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 2)			7	13	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.
Note 2. I_{CC} is measured with all inputs at 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

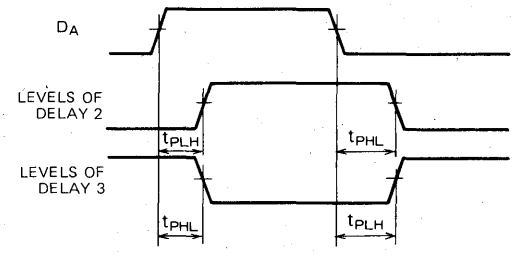
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D_A to outputs $\bar{a} \sim \bar{g}$	$R_L=665\Omega$, $C_L=15pF$ (Note 3)		35	100	ns
t_{PHL}				30	100	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{RBI}$ to outputs $\bar{a} \sim \bar{f}$			50	100	ns
t_{PHL}				45	100	ns

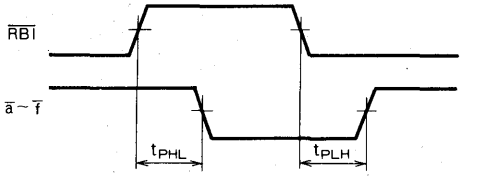
Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Z_O=50Ω.
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)





M74LS248P

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

DESCRIPTION

The M74LS248P is a semiconductor integrated circuit provided with a BCD-to-7-segment decoder/driver function and 2kohm (typ) pull-up resistor outputs.

FEATURES

- Suitable for lighting 7-segment display element
- $\overline{RBI}$ input and $\overline{BI}/\overline{RBO}$ output for zero suppression
- $\overline{LT}$ input for lamp testing
- $\overline{BI}/\overline{RBO}$ input for blanking all segments
- NPN transistor can be externally mounted for high-current drive.
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

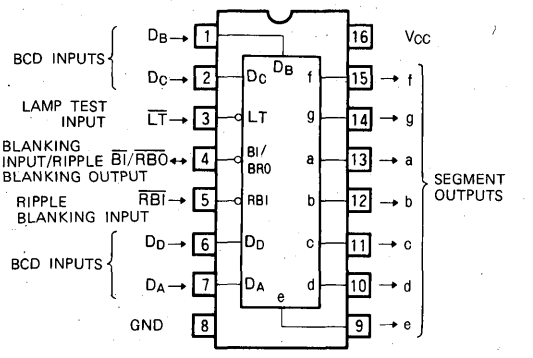
This IC is a version of the M74LS247P without the output transistors. When numbers are specified in BCD code for BCD inputs D_A, D_B, D_C and D_D, segment outputs a~g are set high in accordance with those numbers. These outputs have built-in 2kΩ pull-up resistors suited to driving common-cathode LEDs. High-current display elements can be driven by connecting NPN transistors to the outputs.

The ripple blanking, blanking and lamp test functions are the same as those for the M74LS247P.

Refer to the M74LS47P for the application example.

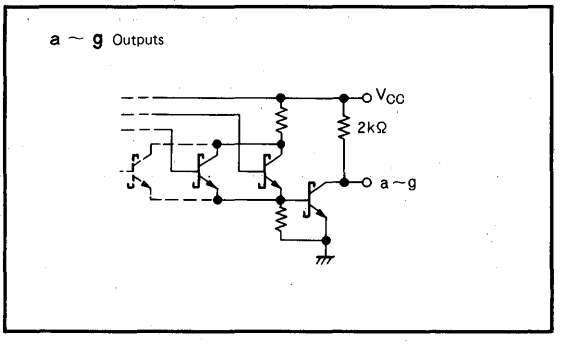
The only difference from the M74LS48P is the configuration of the 6 and 9 numerals.

PIN CONFIGURATION (TOP VIEW)

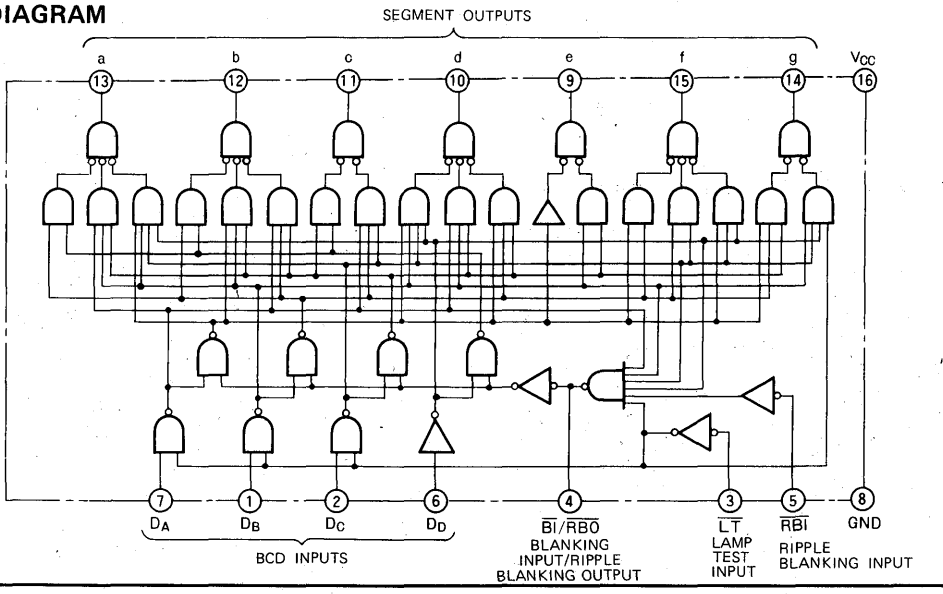


Outline 16P4

OUTPUT CIRCUIT SCHEMATIC



BLOCK DIAGRAM



MITSUBISHI ELECTRIC

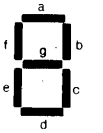
BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

FUNCTION TABLE (Note 1)

Decimal number or function	$\overline{LT}$	$\overline{RBI}$	D_D	D_C	D_B	D_A	$\overline{BI}/\overline{RBO}$	a	b	c	d	e	f	g	Note
0	H	H	L	L	L	L		H	H	H	H	H	H	H	L	(1)
1	H	X	L	L	L	H		H	L	H	H	L	L	L	L	
2	H	X	L	L	H	L		H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H		H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L		H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H		H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L		H	H	L	H	H	H	H	H	
7	H	X	L	H	H	H		H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L		H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H		H	H	H	H	H	L	H	H	
10	H	X	H	L	H	L		H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H		H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L		H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H		H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L		H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H		H	L	L	L	L	L	L	L	
Blanking	X	X	X	X	X	X	L		L	L	L	L	L	L	L	(2)
Ripple blanking	H	L	L	L	L	L		L	L	L	L	L	L	L	L	(3)
Lamp test	L	X	X	X	X	X		H	H	H	H	H	H	H	H	(4)

Note 1. (1) $\overline{LT}$ is normally kept in high.
$\overline{RBI}$ is kept open or in high in case of a decimal 0 output.
(2) When $\overline{BI}/\overline{RBO}$ is low, all the segment outputs are low irrespective of the status of the other inputs.
(3) All the segment outputs are set low and $\overline{BI}/\overline{RBO}$ is set low when $\overline{RBI}$, D_A, D_B, D_C and D_D are set low with $\overline{LT}$ high.
(4) When $\overline{LT}$ is low, all the segment outputs are high.
X: Irrelevant

DEFINITION OF SEGMENTS



CHARACTERS DISPLAYED

Decimal number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Character	0	1	2	3	4	5	6	7	8	9	c	ɔ	u	⊆	t	

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	Input $\overline{BI}/\overline{RBO}$		−0.5 ~ V_{CC}	V
		Other inputs		−0.5 ~ +15	V
V_O	Output voltage	Output $\overline{BI}/\overline{RBO}$	High-level state	−0.5 ~ V_{CC}	V
		Other outputs		−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current, outputs a ~ g	$V_{OH} \geqq 2.4V$	0		−100	μA
I_{OH}	High-level output current, output $\overline{BI}/\overline{RBO}$	$V_{OH} \geqq 2.4V$	0		−50	μA
I_{OL}	Low-level output current, outputs a ~ g	$V_{OL} \leqq 0.4V$	0		2	mA
		$V_{OL} \leqq 0.5V$	0		6	mA
I_{OL}	Low-level output current, output $\overline{BI}/\overline{RBO}$	$V_{OL} \leqq 0.4V$	0		1.6	mA
		$V_{OL} \leqq 0.5V$	0		3.2	mA

BCD-TO-7-SEGMENT DECODER/DRIVER (ACTIVE-HIGH OUTPUT)

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +70°C$, unless otherwise noted)

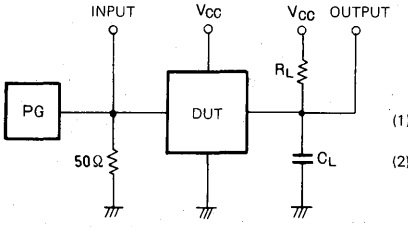
Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	Outputs a~g	$V_{CC}=4.75V$	$I_{OH}=-100\mu A$	2.4	4.2		V
		Output $\overline{BI}/\overline{RBO}$	$V_I=0.8V$, $V_I=2V$	$I_{OH}=-50\mu A$	2.4	4.2		V
I_{OH}	High-level output current	Outputs a~g	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $V_O=0.85V$		−1.3	−2		mA
V_{OL}	Low-level output voltage	Outputs a~g	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=2mA$		0.25	0.4	V
				$I_{OL}=6mA$		0.35	0.5	V
		Output $\overline{BI}/\overline{RBO}$		$I_{OL}=1.6mA$		0.25	0.4	V
				$I_{OL}=3.2mA$		0.35	0.5	V
I_{IH}	High-level input current	Except input $\overline{BI}/\overline{RBO}$	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
			$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	Input $\overline{BI}/\overline{RBO}$	$V_{CC}=5.25V$, $V_I=0.4V$				−1.2	mA
		Other inputs					−0.4	mA
I_{OS}	Short-circuit output current	Output $\overline{BI}/\overline{RBO}$	$V_{CC}=5.25V$, $V_O=0V$		−0.3		−2	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 2)			25	38	mA

* : All typical values are at $V_{CC}=5V$, $T_a=25°C$.
Note 2. I_{CC} is measured with all inputs at 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

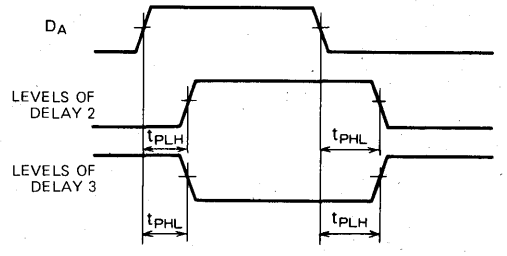
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D_A to outputs a~g	$R_L=4k\Omega$, $C_L=15pF$ (Note 3)		30	100	ns
t_{PHL}				30	100	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{RBI}$ to outputs a~f	$R_L=6k\Omega$, $C_L=15pF$ (Note 3)		40	100	ns
t_{PHL}				45	100	ns

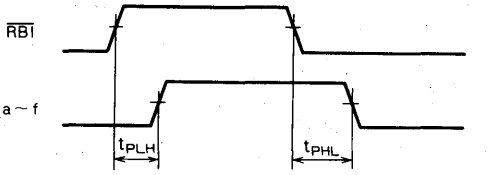
Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Z_O=50Ω.
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)





M74LS251P

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS251P is a semiconductor integrated circuit containing an 8-line to 1-line data selector/multiplexer function and 3-state outputs.

FEATURES

- 3-state outputs
- Complementary output provided
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

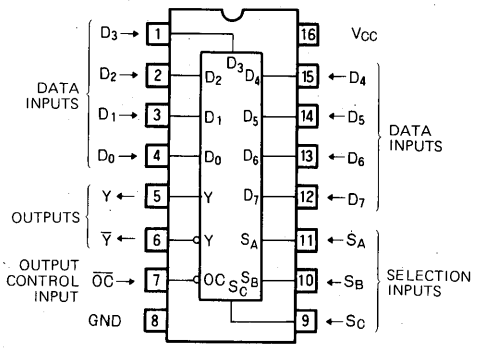
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has a data selector function which provides 1-line selection of 8 input signals and using a multiplexer function which converts the 8-bit parallel data into serial data by time-sharing. When 8-line signals are applied to the data inputs and 1 data is specified from among the 8 data from selection inputs S_A, S_B and S_C, the input signal is at output Y and the inverted signal from output $\overline{Y}$. When output control input $\overline{OC}$ is set high, Y and $\overline{Y}$ are put in the high-impedance state and the outputs are completely isolated.

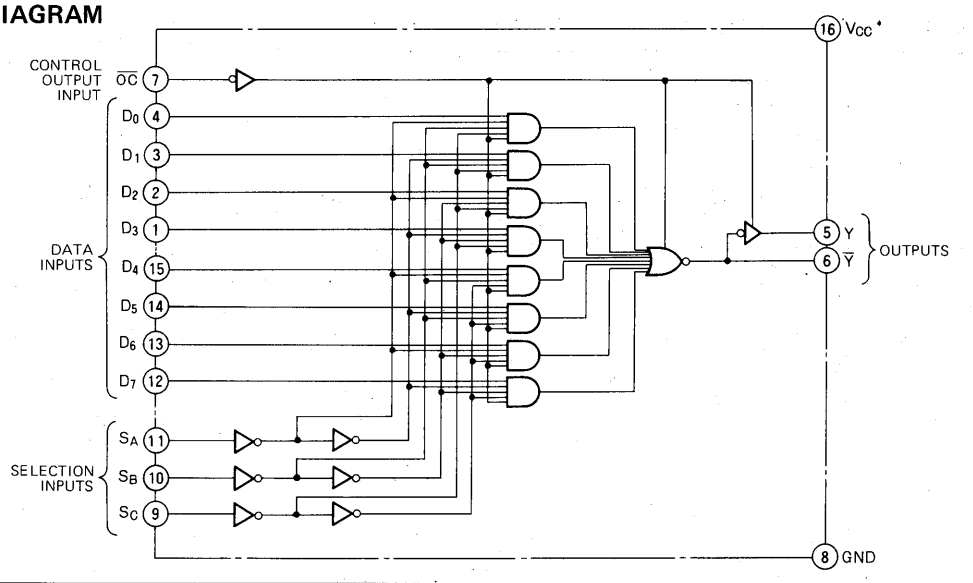
M74LS251P has the same functions and pin connections as M74LS151P but the latter is provided with active pull-up resistor outputs.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

S_C	S_B	S_A	$\overline{OC}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	$\overline{Y}$
X	X	X	H	X	X	X	X	X	X	X	X	Z	Z
L	L	L	L	L	X	X	X	X	X	X	X	L	H
L	L	L	L	H	X	X	X	X	X	X	X	H	L
L	L	H	L	X	L	X	X	X	X	X	X	L	H
L	L	H	L	X	H	X	X	X	X	X	X	H	L
L	H	L	L	X	X	L	X	X	X	X	X	L	H
L	H	L	L	X	X	H	X	X	X	X	X	H	L
L	H	H	L	X	X	X	L	X	X	X	X	L	H
L	H	H	L	X	X	X	H	X	X	X	X	H	L
H	L	L	L	X	X	X	X	L	X	X	X	L	H
H	L	L	L	X	X	X	X	H	X	X	X	H	L
H	L	H	L	X	X	X	X	X	L	X	X	L	H
H	L	H	L	X	X	X	X	X	H	X	X	H	L
H	H	L	L	X	X	X	X	X	X	L	X	L	H
H	H	L	L	X	X	X	X	X	X	H	X	H	L
H	H	H	L	X	X	X	X	X	X	X	L	L	H
H	H	H	L	X	X	X	X	X	X	X	H	H	L

Note 1 X : Irrelevant
Z : High-impedance state

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

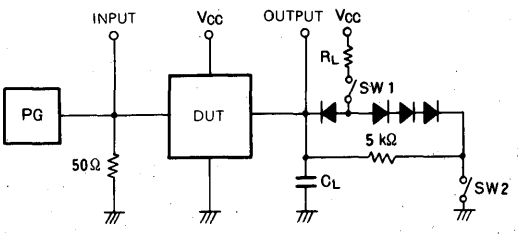
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V, V_I=2V, I_{OH}=−2.6mA	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V, V_I=0.8V, V_I=2V, I_{OL}= 4 mA		0.25	0.4	V
		V_{CC}=4.75V, V_I=0.8V, V_I=2V, I_{OL}= 8 mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current	V_{CC}=5.25V, V_I=2V, V_O=2.7V			20	μA
I_{OZL}	Off-state low-level output current	V_{CC}=5.25V, V_I=2V, V_O=0.4V			−20	μA
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V			20	μA
		V_{CC}=5.25V, V_I=10V			0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V			−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC}=5.25V, V_O=0V	−30		−130	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 3)		6.1	10	mA
I_{CCZ}	Supply current, all outputs off	V_{CC}=5.25V (Note 4)		7.1	12	mA

* : All typical values are at V_{CC}=5V, T_a=25°C.
Note 2: All measurements should be done quickly.
Note 3: I_{CC} is measured with $\overline{OC}$ at 0V and all other inputs at 4.5V
Note 4: I_{CCZ} is measured with all inputs at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs S_A, S_B, S_C to output Y	C_L=15pF (Note 5)		22	45	ns
t_{PHL}				18	45	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs S_A, S_B, S_C to output $\overline{Y}$			10	33	ns
t_{PHL}				15	33	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_0~D_7 to output Y			15	28	ns
t_{PHL}				14	28	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_0~D_7 to output $\overline{Y}$			7	15	ns
t_{PHL}				7	15	ns
t_{PZH}	High-level output enable time, from input $\overline{OC}$ to output Y	R_L=2kΩ, C_L=15pF (Note 5)		11	45	ns
t_{PZL}	Low-level output enable time, from input $\overline{OC}$ to output Y			16	40	ns
t_{PZH}	High-level output enable time, from input $\overline{OC}$ to output $\overline{Y}$	R_L=2kΩ, C_L=15pF (Note 5)		11	27	ns
t_{PZL}	Low-level output enable time, from input $\overline{OC}$ to output $\overline{Y}$			13	40	ns
t_{PHZ}	High-level outpout disable time, from input $\overline{OC}$ to output Y	R_L=2kΩ, C_L= 5 pF (Note 5)		16	45	ns
t_{PLZ}	Low-level output disable time, from input $\overline{OC}$ to output Y			8	25	ns
t_{PHZ}	High-level output disable time, from input $\overline{OC}$ to output $\overline{Y}$	R_L=2kΩ, C_L= 5 pF (Note 5)		18	55	ns
t_{PLZ}	Low-level output disable time, from input $\overline{OC}$ to output $\overline{Y}$			9	25	ns

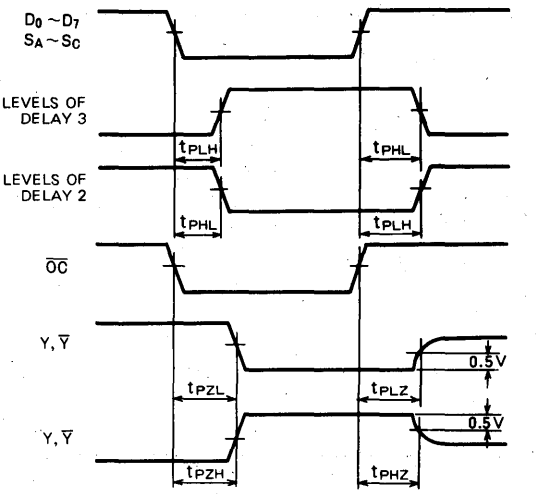
Note 5: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Z_o=50Ω.
(2) All diodes are switching diodes. ($t_{rr} \leq 4ns$)
(3) C_L includes probe and jig capacitance

Symbol	SW 1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

TIMING DIAGRAM (Reference level = 1.3V)



M74LS253P

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS253P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits and 3-state outputs.

FEATURES

- Selection inputs common to both circuits
- Output control inputs separate for each circuit
- 3-state outputs
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

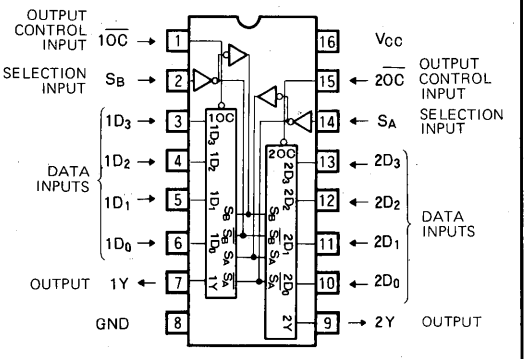
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has two data selector circuits which provide 1-line selection of 4 input signal using two multiplexer circuits which convert the 4-bit parallel data into serial data by time-sharing. When 4-line signals are applied to the data inputs D_0, D_1, D_2 and D_3, and 1 data is specifed from among the data input by selection inputs S_A and S_B, the input signal is output at Y. By applying 4-bit parallel data to data inputs D_0, D_1, D_2 and D_3 and by connecting the output of a synchronous divide-by-four counter to S_A and S_B, data D_0, D_1, D_2 and D_3 appear in the order of D_0, D_1, D_2 and D_3, synchronized with the clock pulse. S_A and S_B are common to both circuits while output control inputs $1\overline{OC}$ and $2\overline{OC}$ are separate. When $1\overline{OC}$ and $2\overline{OC}$ are set high, 1Y and 2Y are put in the high-impedance state ("Z") irrespective of the status of the inputs.

M74LS253P has the same functions and pin connections as M74LS153P but the latter is provided with active pull-up resistor outputs.

PIN CONFIGURATION (TOP VIEW)



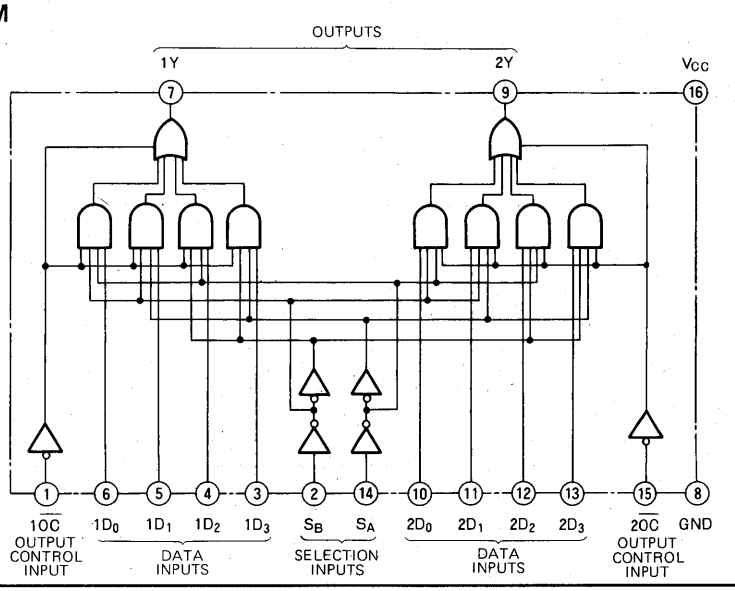
Outline 16P4

FUNCTION TABLE (Note 1)

S_B	S_A	D_0	D_1	D_2	D_3	$\overline{OC}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Note 1 X : Irrelevant
Z : High-impedance state

BLOCK DIAGRAM



DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V V_I= 2 V, I_{OH}=−2.6mA		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}= 4 mA		0.25	0.4	V
		V_I=0.8V, V_I= 2 V	I_{OL}= 8 mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current	V_{CC}=5.25V, V_I= 2 V, V_O=2.7V				20	μA
I_{OZL}	Off-state low-level output current	V_{CC}=5.25V, V_I= 2 V, V_O=0.4V				−20	μA
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC}=5.25V, V_O= 0 V		−30		−130	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.25V (Note 3)			7	12	mA
I_{CCZ}	Supply current, all outputs off	V_{CC}=5.25V (Note 4)			8.5	14	mA

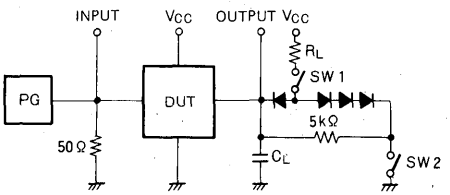
* : All typical values are at V_{CC}=5V, T_a=25°C.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CCL} is measured with all inputs at 0V.
Note 4: I_{CCZ} is measured with $1\overline{OC}$ and $2\overline{OC}$ at 4.5V and all other inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $D_0 \sim D_3$ to output Y	C_L=15pF (Note 5)		8	25	ns
t_{PHL}				12	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs S_A, S_B to output Y			12	45	ns
t_{PHL}				12	32	ns
t_{PZH}	Output enable time to high-level	R_L=2kΩ, C_L=15pF (Note 5)		11	28	ns
t_{PZL}	Output enable time to low-level	R_L=2kΩ, C_L=15pF (Note 5)		12	23	ns
t_{PHZ}	Output disable time from high-level	R_L=2kΩ, C_L=5pF (Note 5)		15	41	ns
t_{PLZ}	Output disable time from low-level	R_L=2kΩ, C_L=5pF (Note 5)		9	27	ns

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

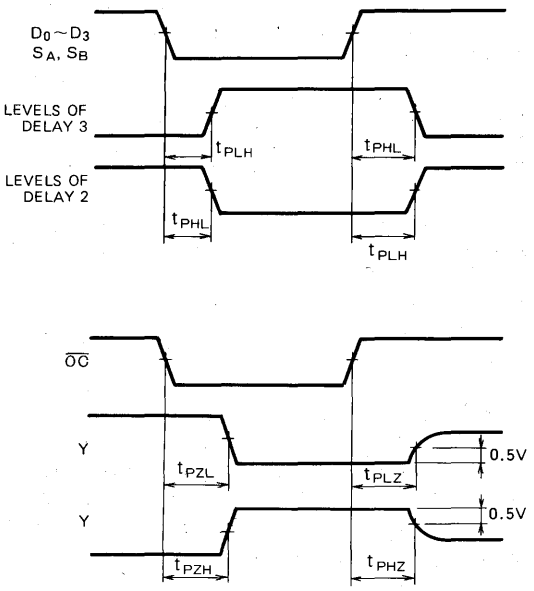
Note 5: Measurement circuit



Symbol	SW 1	SW 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR-1MHz, t_r=6ns, t_f=6ns, t_w=500ns, $V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.
(2) All diodes are switching diodes. ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS256P

DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION

The M74LS256P is a semiconductor integrated circuit containing a dual demultiplexer circuit configured into a 4-bit latch addressable in 2-bit binary code.

FEATURES

- Easily expandable
- May be used as a 2-bit binary-to-quaternary decoder/demultiplexer
- Active low common reset
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment

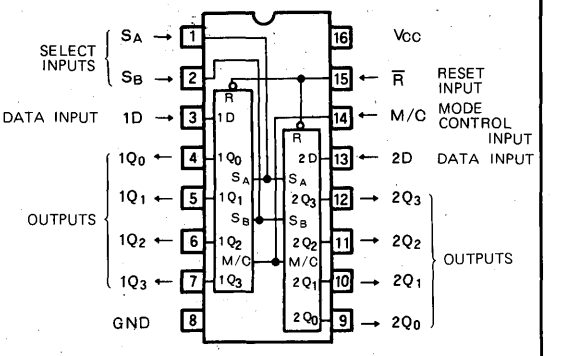
FUNCTIONAL DESCRIPTION

This device is configured from two circuits providing the capability to function as a 2- bit binary-to-quaternary demultiplexer or as a 4-bit latch. The operational modes listed below are selectable using mode control input M/C (common to both circuits) and reset input $\overline{R}$ in combination.

(1) 2-bit binary-to-quaternary decoder/demultiplexer
(2) Addressable latch
(3) Data input inhibit
(4) Reset

When used as a 2-bit binary-to-quaternary decoder/demultiplexer and a 2-bit binary number is applied to select inputs S_A and S_B, one of the $Q_0 \sim Q_3$ outputs will correspond to that number, and the signal appearing at its output will be the same as the one present at data input D. All other outputs will remain low-level at this time; and latch operations are not performed in this mode.

PIN CONFIGURATION (TOP VIEW)



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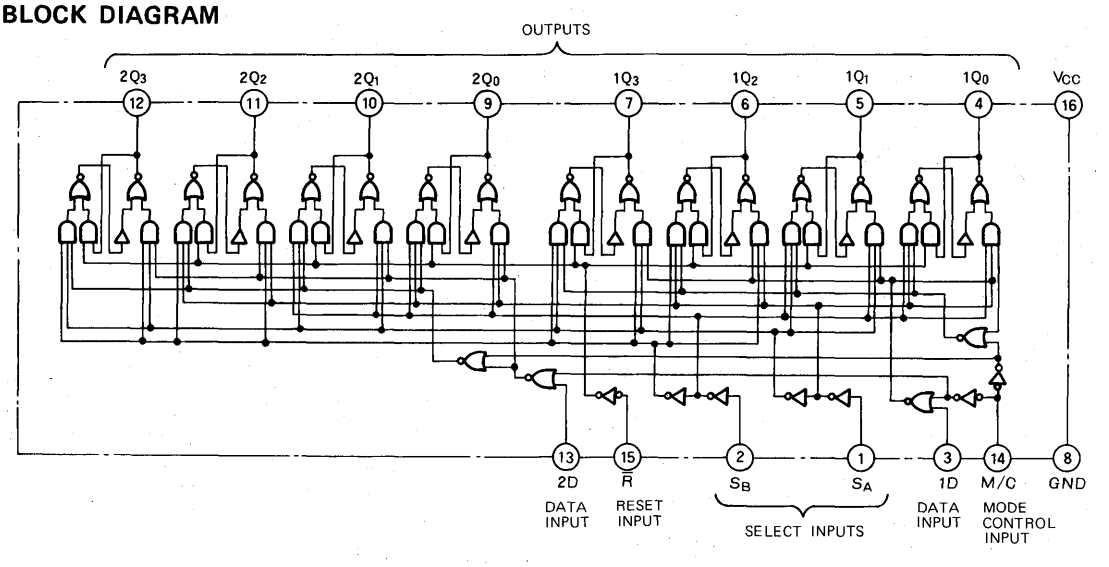
When used as an addressable latch, S_A and S_B will be ıecified as in the above operation, with the corresponding tch being selected. The signal present at data input D will then appear at output. When M/C transits from low to high (data inhibit mode), the information present at D immediately prior to that event will be latched. When M/C is low-level, changing the signal at D will also change the signal present at Q.

During the data input inhibit mode, changes applied to D will not affect $Q_0 \sim Q_3$, and the status prior to M/C transiting high will be held.

Direct reset is activated by all outputs at low-level, regardless of the status of D, S_A, and S_B.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTION TABLE (Note 1)

Operational mode	$\overline{R}$	M/C	D	S_A	S_B	Q_0	Q_1	Q_2	Q_3
Reset	L	H	X	X	X	L	L	L	L
Active high 4-channel demultiplexers	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	H	L	L	L
	L	L	L	H	L	L	L	L	L
	L	L	H	H	L	L	H	L	L
	L	L	L	L	H	L	L	L	L
	L	L	H	L	H	L	L	H	L
	L	L	L	H	H	L	L	L	L
	L	L	H	H	H	L	L	L	H
Memory	H	H	X	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0
Addressable latch	H	L	L	L	L	L	Q_1^0	Q_2^0	Q_3^0
	H	L	H	L	L	H	Q_1^0	Q_2^0	Q_3^0
	H	L	L	H	L	Q_0^0	L	Q_2^0	Q_3^0
	H	L	H	H	L	Q_0^0	H	Q_2^0	Q_3^0
	H	L	L	L	H	Q_0^0	Q_1^0	L	Q_3^0
	H	L	H	L	H	Q_0^0	Q_1^0	H	Q_3^0
	H	L	L	H	H	Q_0^0	Q_1^0	Q_2^0	L
	H	L	H	H	H	Q_0^0	Q_1^0	Q_2^0	H

Note 1. X : Irrelevant
Q^0 : Indicates output status prior to input conditions being set.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
			V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	M/C	V_{CC}=5.25V, V_I=2.7V				40	μA
		Exclusive of M/C					20	
		M/C	V_{CC}=5.25V, V_I=10V				0.2	mA
		Exclusive of M/C					0.1	
I_{IL}	Low-level input current	M/C	V_{CC}=5.25V, V_I=0.4V				−0.8	mA
		Exclusive of M/C					−0.4	
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 3)			20	36	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

3. I_{CC} is measured with all inputs at 0V.

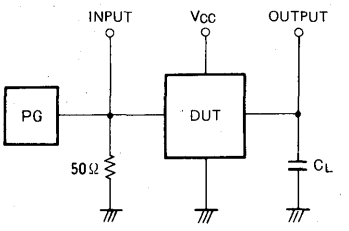
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R}$ to output Q_0~Q_3	C_L=15pF (Note 4)		9	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output Q_0~Q_3			15	32	ns
t_{PHL}				11	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input S_A, S_B to output Q_0~Q_3			15	38	ns
t_{PHL}				11	29	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input M/C to output Q_0~Q_3			14	35	ns
t_{PHL}				13	24	ns

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(DH)}$	D high-level setup time to M/C		15	10		ns
$t_{h(DH)}$	D high-level hold time to M/C		5	− 5		ns
$t_{su(DL)}$	D low-level setup time to M/C		15	8		ns
$t_{h(DL)}$	D low-level hold time to M/C		5	− 7		ns
$t_{su(S)}$	S_A, S_B setup time to M/C		15	7		ns
$t_{h(S)}$	S_A, S_B hold time to M/C		5	− 5		ns
$t_{w(M/C)}$	M/C pulse width		15	8		ns
$t_{w(\overline{R})}$	$\overline{R}$ pulse width		15	7		ns

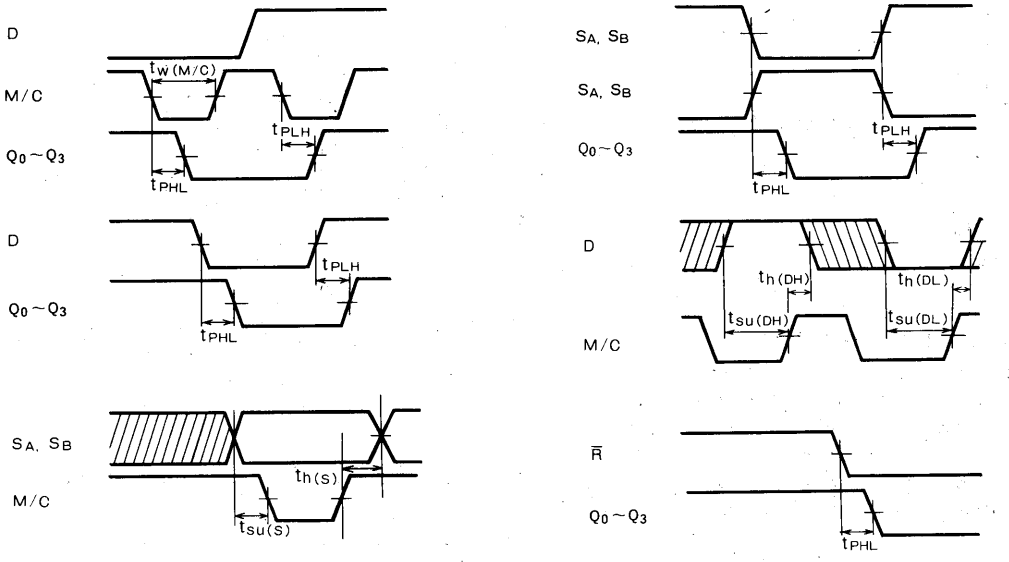
Note 4. Measurement Circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω.

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



Note 5. Shaded area denotes the time period in which switching is possible.

M74LS257AP

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS257AP is a semiconductor integrated circuit containing four 2-line to 1-line data selector/multiplexer circuits and 3-state outputs.

FEATURES

- Output control input common to all four circuits
- 3-state outputs
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

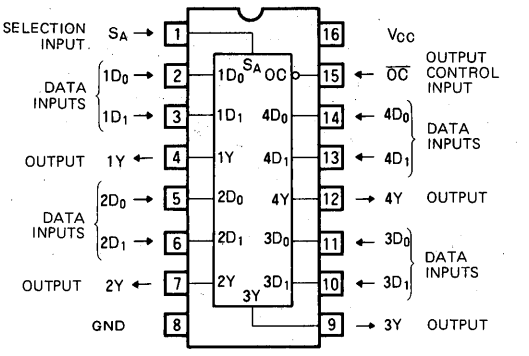
FUNCTIONAL DESCRIPTION

This IC has four data selector circuits which provide 1-line selection of 2 input signals using four multiplexer circuits which convert the 2-bit parallel data into serial data by time-sharing. When 2-line signals are applied to the data inputs D_0 and D_1, and 1 data is specified from among the data input from selection input S_A, the input signal is output at Y.

S_A and output control $\overline{OC}$ are common to all four circuits. When $\overline{OC}$ is set high, 1Y, 2Y, 3Y and 4Y are put in the high-impedance state irrespective of the status of the other inputs.

M74LS257AP has the same functions and pin connections as M74LS157P but the latter is provided with active pull-up resistor outputs.

PIN CONFIGURATION (TOP VIEW)



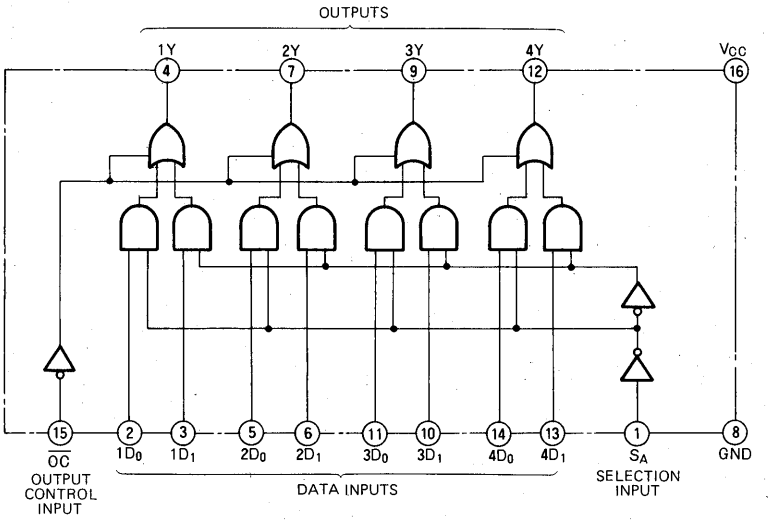
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{OC}$	S_A	D_0	D_1	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Note 1 X : Irrelevant
Z : High-impedance state

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

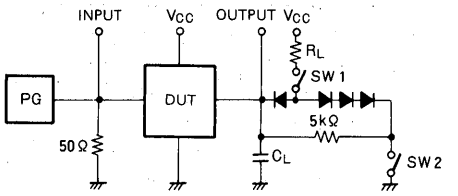
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−2.6mA		2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=12mA		0.25	0.4	V
			V_I=0.8V, V_I=2V	I_{OL}=24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.25V, V_I=2V, V_O=2.4V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.25V, V_I=2V, V_O=0.4V				−20	μA
I_{IH}	High-level input current	D_0, D_1, $\overline{OC}$	V_{CC}=5.25V				20	μA
		S_A	V_I=2.7V				40	
		D_0, D_1, $\overline{OC}$	V_{CC}=5.25V				0.1	mA
		S_A	V_I=10V				0.2	
I_{IL}	Low-level input current	D_0, D_1, $\overline{OC}$	V_{CC}=5.25V				−0.4	mA
		S_A	V_I=0.4V				−0.8	
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−30		−130	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.25V (Note 3)			6.2	10	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.25V (Note 4)			10	16	mA
I_{CCZ}	Supply current, all outputs off		V_{CC}=5.25V (Note 5)			12	19	mA

* : All typical values are at V_{CC}=5V, T_a=25°C.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CCH} is measured with $\overline{OC}$, S_A, D_1 at 0V and D_0 at 4.5V
Note 4: I_{CCL} is measured with all inputs at 0V.
Note 5: I_{CCZ} is measured with $\overline{OC}$ at 4.5V and all other inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_0, D_1 to output Y	C_L=45pF (Note 6)		6	18	ns
t_{PHL}				8	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input S_A to output Y			11	28	ns
t_{PHL}				11	35	ns
t_{PZH}	Output enable time to high-level	R_L=667Ω C_L=45pF (Note 6)		7	22	ns
t_{PZL}	Output enable time to low-level	R_L=667Ω, C_L=45pF (Note 6)		9	35	ns
t_{PLZ}	Output disable time from low-level	R_L=667Ω, C_L=5 pF (Note 6)		11	26	ns
t_{PHZ}	Output disable time from high-level	R_L=667Ω, C_L=5 pF (Note 6)		8	35	ns

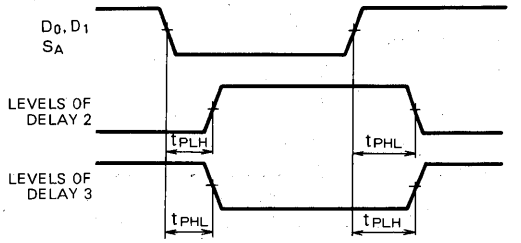
Note 6: Measurement circuit

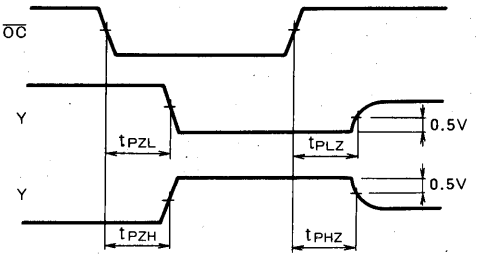


Symbol	SW 1	SW 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance.

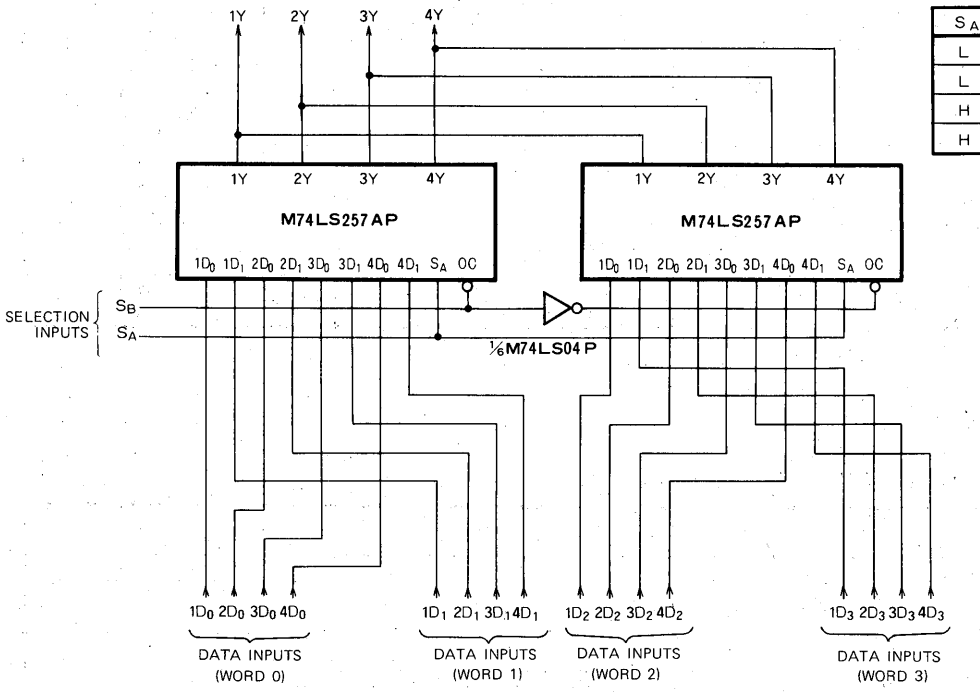
TIMING DIAGRAM (Reference level = 1.3V)





APPLICATION EXAMPLE

4-line to 1-line data selector (multiplexer)



SA	SB	OUTPUT
L	L	WORD 0
L	H	WORD 1
H	L	WORD 2
H	H	WORD 3

M74LS258AP

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS258AP is a semiconductor integrated circuit containing four 2-line to 1-line data selector/multiplexer circuits with 3-stage outputs.

FEATURES

- Inverted outputs
- Output control input common to all four circuits
- Select input common to all four circuits
- 3-state outputs
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

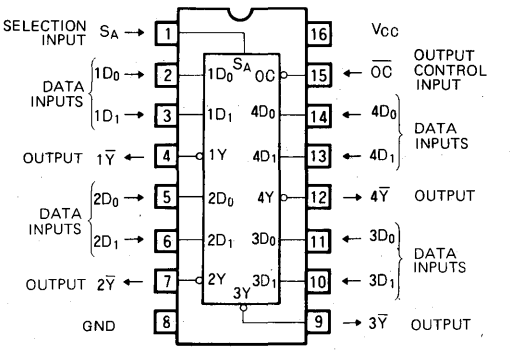
FUNCTIONAL DESCRIPTION

This IC contains four sets of circuits which are used 1-line selection 2 input signals and as both data selectors, selecting 1-line out of 2 input signals, and multiplexers which convert the 2-bit parallel data into serial data by time-sharing. When one out of 2-line signals, which are applied to the data inputs D_0 and D_1, is specified by select from input S_A, inverted signal of that appears at output $\overline{Y}$.

S_A and output control $\overline{OC}$ are common to all four circuits. When $\overline{OC}$ is set high, $1\overline{Y}$, $2\overline{Y}$, $3\overline{Y}$ and $4\overline{Y}$ are put in the high-impedance state irrespective of the status of the other inputs.

M74LS258AP has the same functions and pin connections as M74LS158P but the latter is provided with active pull-up resistor outputs.

PIN CONFIGURATION (TOP VIEW)



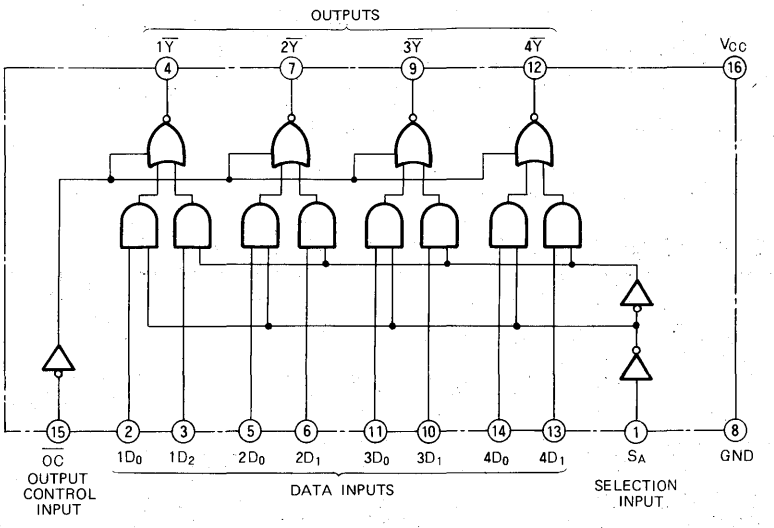
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{OC}$	S_A	D_0	D_1	$\overline{Y}$
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

Note 1 X : Irrelevant
Z : High-impedance state

BLOCK DIAGRAM



QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−2.6 mA		2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=12mA		0.25	0.4	V
			V_I=0.8V, V_I=2V	I_{OL}=24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.25V, V_I=2V, V_O=2.7V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.25V, V_I=2V, V_O=0.4V				−20	μA
I_{IH}	High-level input current	D_0, D_1, $\overline{OC}$	V_{CC}=5.25V				20	μA
		S_A	V_I=2.7V				40	
		D_0, D_1, $\overline{OC}$	V_{CC}=5.25V				0.1	mA
		S_A	V_I=10V				0.2	
I_{IL}	Low-level input current	D_0, D_1, $\overline{OC}$	V_{CC}=5.25V				−0.4	mA
		S_A	V_I=0.4V				−0.8	
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−30		−130	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.25V (Note 3)			4.5	7	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.25V (Note 4)			8.8	14	mA
I_{CCZ}	Supply current, all outputs off		V_{CC}=5.25V (Note 5)			12	19	mA

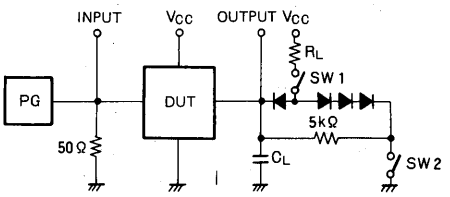
*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CCH} is measured with all inputs at 0V.
Note 4: I_{CCL} is measured with $\overline{OC}$, S_A and D_1 at 0V and D_0 at 4.5V.
Note 5: I_{CCZ} is measured with $\overline{OC}$ at 4.5V and all other inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_0, D_1 to output $\overline{Y}$	C_L=45pF (Note 6)		5	18	ns
t_{PHL}				8	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input S_A to output $\overline{Y}$			9	28	ns
t_{PHL}				16	35	ns
t_{PZH}	Output enable time to high-level	R_L=667Ω, C_L=45pF (Note 6)		7	22	ns
t_{PZL}	Output enable time to low-level	R_L=667Ω, C_L=45pF (Note 6)		12	35	ns
t_{PLZ}	Output disable time from low-level	R_L=667Ω, C_L= 5 pF (Note 6)		11	26	ns
t_{PHZ}	Output disable time from high-level	R_L=667Ω, C_L= 5 pF (Note 6)		8	35	ns

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

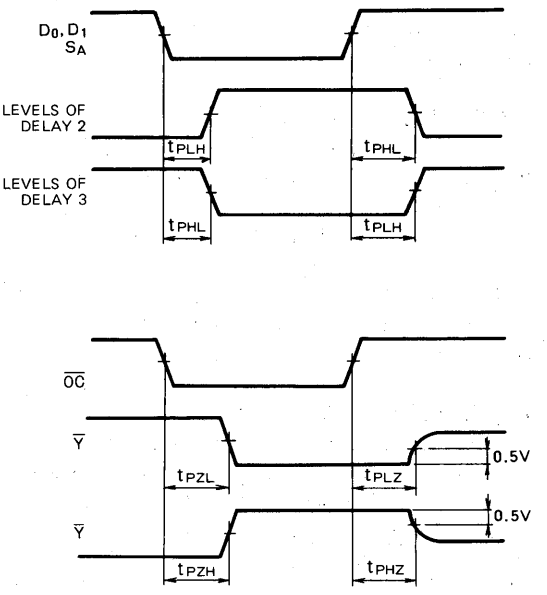
Note 6: Measurement circuit



Symbol	SW 1	SW 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Z_O=50Ω.
(2) All diodes are switching diodes.
(3) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



M74LS259P

8-BIT ADDRESSABLE LATCH

DESCRIPTION

The M74LS259P is a semiconductor integrated circuit containing 8 latch circuits and a demultiplexer which designates the latches with a 3-bit binary code.

FEATURES

- Easy bit expansion
- Usable as 3-bit binary/octal decoder/demultiplexer
- Direct reset input provided
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of a 3-bit binary/octal demultiplexer and 8 latch circuits. The following operational modes can be selected by combining the mode control input M/C with the reset input $\overline{R}$

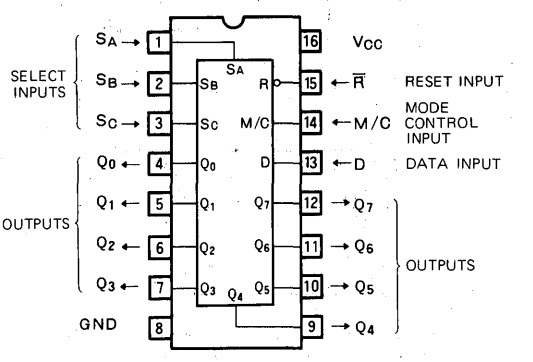
(1)	3-bit binary/octal decoder/demultiplexer	M/C: Low; $\overline{R}$: Low
(2)	Addressable latch	M/C: Low; $\overline{R}$: High
(3)	Data input inhibit	M/C: High $\overline{R}$: High
(4)	Reset	M/C: High; $\overline{R}$: Low

When this device is used as a 3-bit binary/octal decoder/demultiplexer and the select inputs S_A ~ S_C are designated by a 3-bit binary number, the same signal as the data input D appears in one of the outputs Q_0 ~ Q_7 corresponding to that number and all the other outputs are set low. There is no latch operation in this mode.

When used as an addressable latch and inptus S_A ~ S_C are designated as above, the corresponding latch is selected and the same signal as D appears in the output. When M/C changes from low to high (data inhibit mode), the information from the data input D immediately before the change is latched. When M/C is low, the signal appearing in Q is also changed if the signal D is changed.

In the data input inhibit mode Q_0 ~ Q_7 do not change

PIN CONFIGURATION (TOP VIEW)



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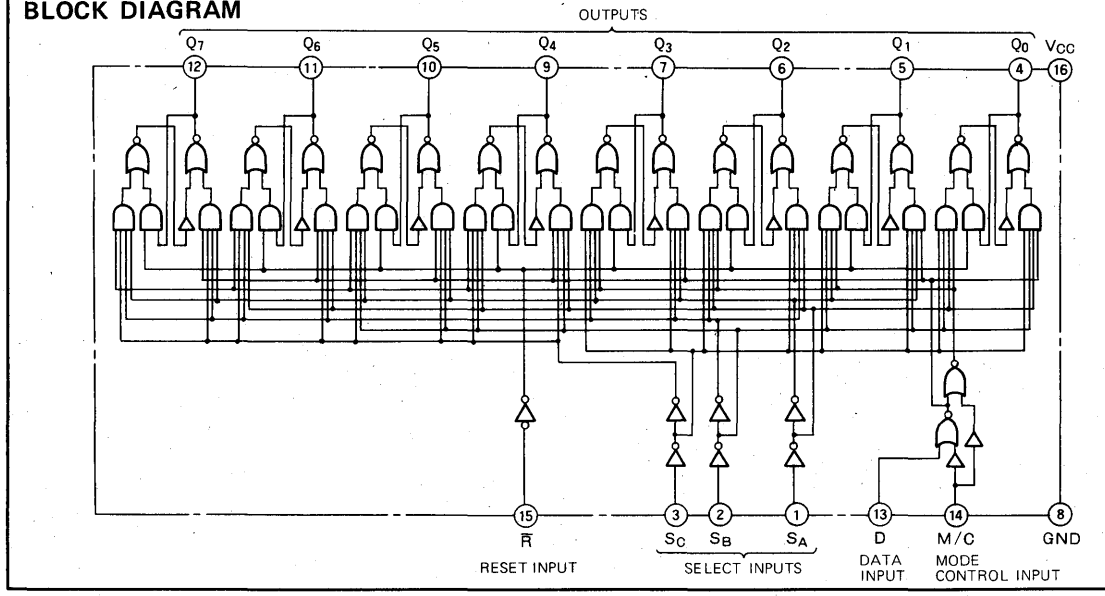
BLOCK DIAGRAM



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even if D is changed and the status before M/C is set high is held.

With direct resetting, all the outputs are reset low irrespective of the status of D and $S_A \sim S_C$.

FUNCTION TABLE (Note 1)

Operational mode	$\overline{R}$	M/C	D	S_A	S_B	S_C	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
3-bit binary/octal decoder/demultiplexer	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	H	L	L	L	L	L	L	L	L	L	L
	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	L	L	L	H	H	H	L	L	L	L	L	L	L	L
	L	L	H	H	H	H	L	L	L	L	L	L	L	H
Data input inhibit	H	H	X	X	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0
Addressable latch	H	L	L	L	L	L	L	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0
	H	L	H	L	L	L	H	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0
	H	L	L	H	L	L	Q_0^0	L	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0
	H	L	H	H	L	L	Q_0^0	H	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	H	L	L	H	H	H	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	L
	H	L	H	H	H	H	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	H

Note 1 X : Irrelevant

Q^0 : Level of Q before the indicated steady-state input conditions were established.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
		V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 3)			22	36	mA

* : All typical values are at V_{CC}=5V, T_a=25°C

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at 0V.

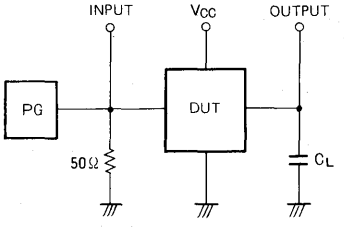
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R}$ to outputs Q_0~Q_7	C_L=15pF		9	27	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to outputs Q_0~Q_7			15	32	ns
t_{PHL}				12	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs S_A, S_B, S_C to outputs Q_0~Q_7			15	38	ns
t_{PHL}				12	29	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time from input M/C to outputs Q_0~Q_7			14	35	ns
t_{PHL}				13	24	ns

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(DH)}$	Setup time D high to M/C		15	10		ns
$t_{h(DH)}$	Hold time D high to M/C		5	−5		ns
$t_{su(DL)}$	Setup time D low to M/C		15	8		ns
$t_{h(DL)}$	Hold time D low to M/C		5	−7		ns
$t_{su(S)}$	Setup time S_A, S_B to M/C		15	7		ns
$t_{h(S)}$	Hold time S_A, S_B, to M/C		5	−5		ns
$t_{w(M/C)}$	M/C input pulse width		15	8		ns
$t_{w(\overline{R})}$	$\overline{R}$ input pulse width		15	7		ns

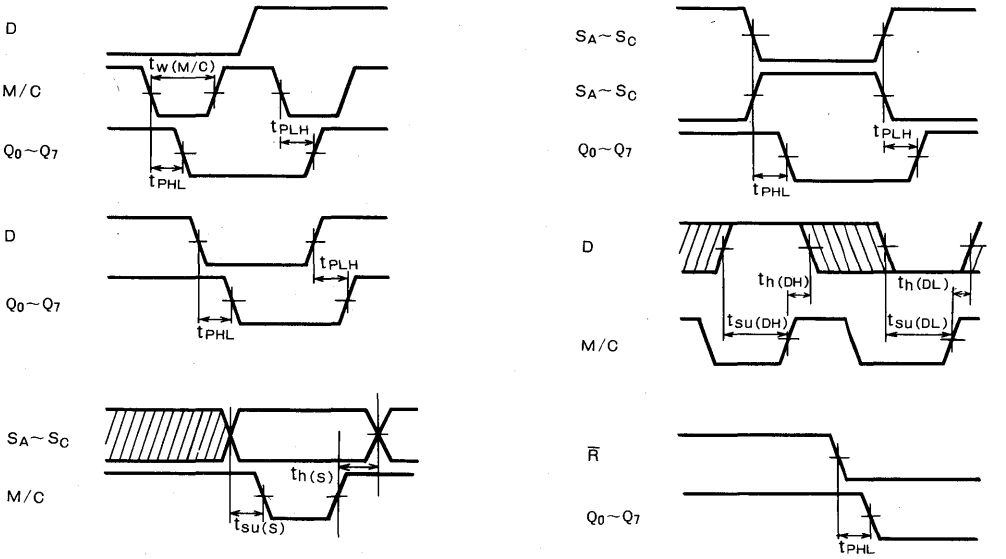
Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω.

(2) C_L includes probe and jig capacitance.

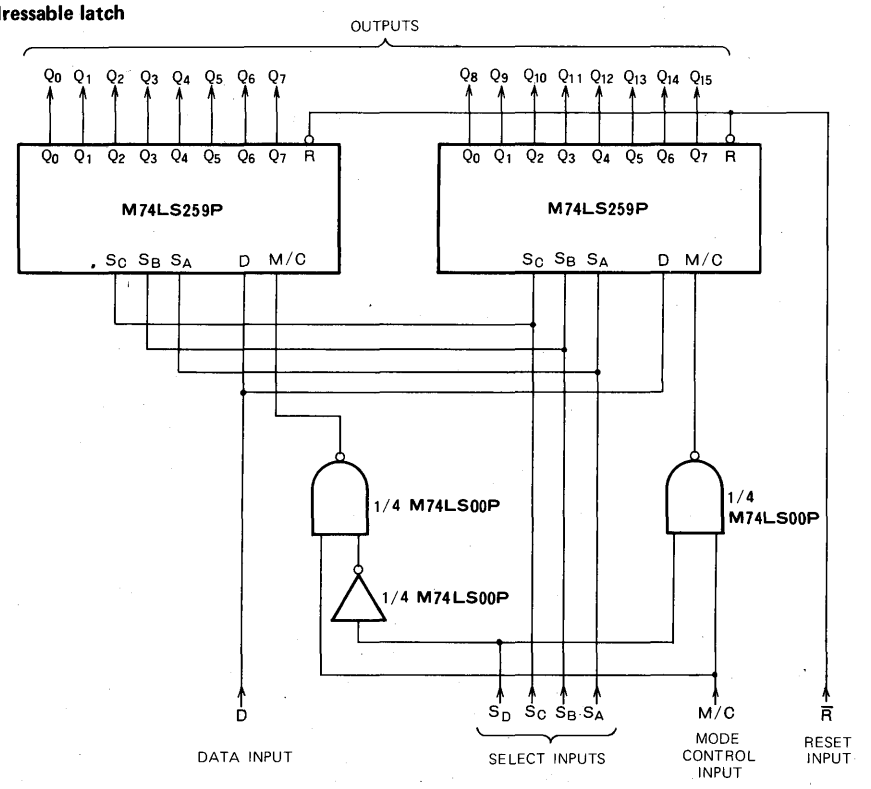
TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

16-bit addressable latch



M74LS266P

QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS266P is a semiconductor integrated circuit containing four integral open-collector output circuits configured into dual input exclusive NOR gates.

FEATURES

- "wire-AND" capability
- Capable of gating high output voltages ($V_O \geqq 7V$)
- Low power dissipation (Pd = 40mW typical)
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

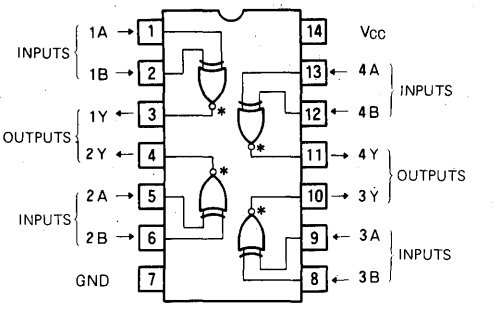
The use of open-collector output circuits in this device gives the user the option of varying high-level output impedance via an external resistance. It is thus possible to implement an AND tie which is not possible in conventional gates.

When both inputs A and B are either high or low-level, output Y goes high-level. Conversely, when A and B are high – low, or low – high with respect to each other, Y will be low-level.

FUNCTION TABLE

A	B	Y
L	L	H
H	L	L
L	H	L
H	H	H

PIN CONFIGURATION (TOP VIEW)



* : OPEN COLLECTOR OUTPUT

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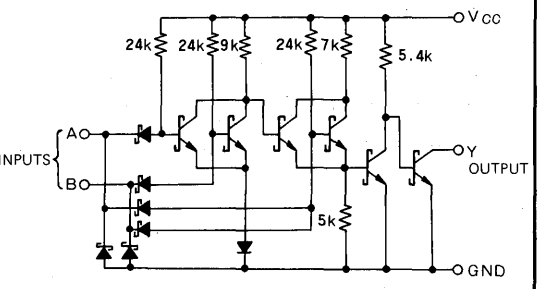
CIRCUIT DIAGRAM (Applicable to each gate)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ +7	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

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QUADRUPLE 2-INPUT EXCLUSIVE NOR GATE WITH OPEN COLLECTOR OUTPUT

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_O = 5.5V$	0		100	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

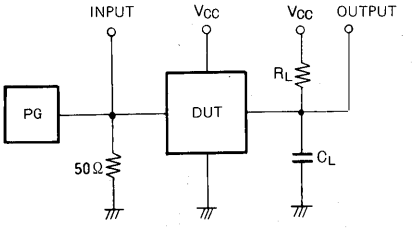
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
I_{OH}	High-level output current	$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $V_O=5.5V$				100	μA
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=4mA$		0.25	0.4	V
		$V_I=0.8V, V_I=2V$	$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				40	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.2	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.8	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 1)			8	13	mA

* : All typical values are at $V_{CC} = 5V$, $T_a = 25°C$.
Note 1. I_{CC} is measured with one input of each gate at 4.5V, the other inputs grounded, and the outputs open.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

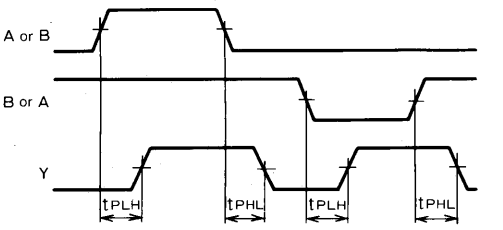
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time	$R_L = 2 k\Omega$, $C_L = 15pF$	Other input low-level (Note 2)		16	30	ns
t_{PHL}					16	30	ns
t_{PLH}		$R_L = 2 k\Omega$, $C_L = 15pF$	Other input high-level (Note 2)		14	30	ns
t_{PHL}					14	30	ns

Note 2. Measurement Circuit



(1) The pulse generator has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS273P

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH RESET

DESCRIPTION

The M74LS273P is a semiconductor integrated circuit containing 8 D-type positive edge-triggered flip-flop circuits with common direct reset and clock inputs.

FEATURES

- Positive edge-triggering
- High mounting density with 8 circuits contained
- Direct reset and clock inputs common to all 8 circuits
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

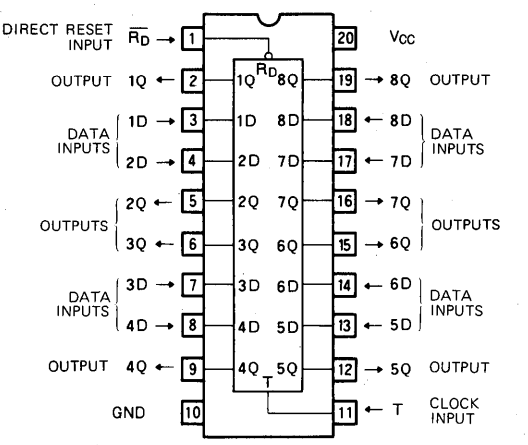
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 8 edge-triggered D-type flip-flop circuits and it is provided with direct reset $\overline{R_D}$ input and clock input T common to all 8 circuits. When T changes in each flip-flop from low to high, the data input signal D immediately before the change appears in output Q.

When $\overline{R_D}$ is set low, 1Q through 8Q are all set low irrespective of the status of the ID through 8D and T signals. For use as a D-type flip-flop, $\overline{R_D}$ must be kept in high.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTION TABLE (Note 1)

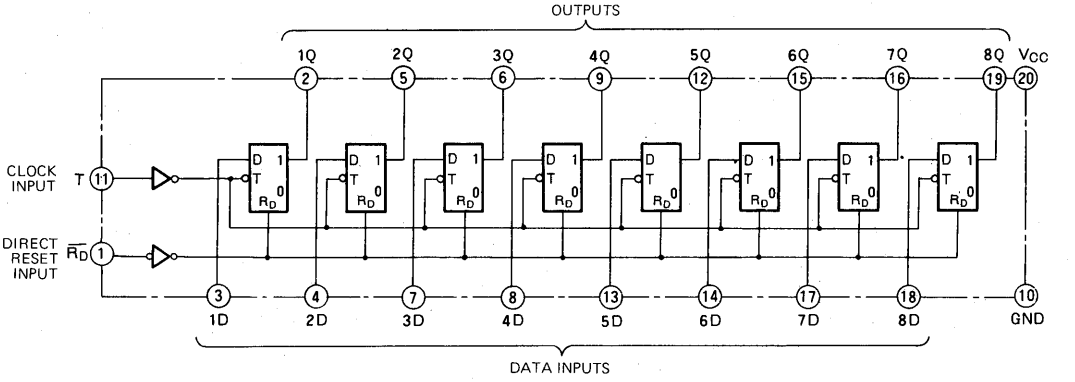
$\overline{R_D}$	T	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

Note 1 ↑ : Transition from low to high (positive edge trigger)

Q_0: Level of Q before the indicated steady-state input conditions were established.

X : Irrelevant

BLOCK DIAGRAM



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OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH RESET

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$, $V_I = 0.8V$ $V_I = 2V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$	$I_{OL} = 4mA$		0.25	0.4	V
		$V_I = 0.8V, V_I = 2V$	$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC} = 5.25V$, $V_O = 0V$		−20		−100	mA
I_{CC}	Supply current	$V_{CC} = 5.25V$ (Note 3)			17	27	mA

* : All typical values are at $V_{CC} = 5V$, $T_a = 25°C$

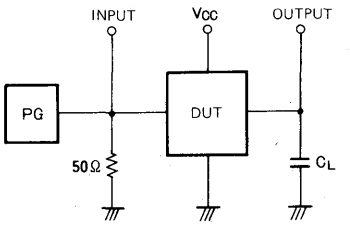
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured after 1D ~ 8D and $\overline{R_D}$ are made 4.5V and T has been changed from 0V to 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L = 15pF$ (Note 4)	30	40		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from T to 1Q~8Q			12	27	ns
t_{PHL}				13	27	ns
t_{PHL}	High-to-low-level output propagation time, from $\overline{R_D}$ to 1Q~8Q			15	27	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.

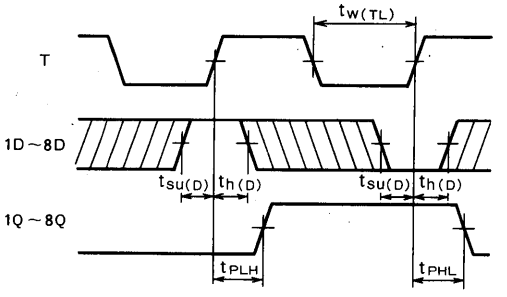
(2) C_L includes probe and jig capacitance.

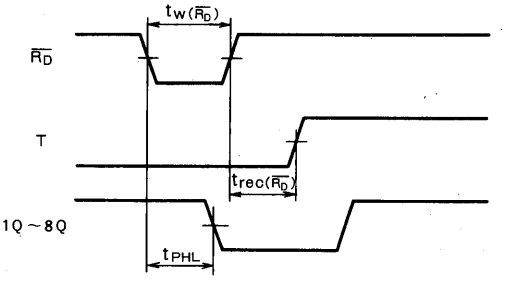
OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH RESET

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(TL)}$	Clock input T low pulse width		20	7		ns
$t_{W(\overline{RD})}$	Direct reset pulse width		20	6		ns
$t_{SU(D)}$	Setup time 1D~8D to T		20	7		ns
$t_{h(D)}$	Hold time 1D~8D to T		5	−3		ns
$t_{rec(\overline{RD})}$	Recovery time $\overline{RD}$ to T		25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS279P

QUADRUPLE R-S LATCH

DESCRIPTION

The M74LS279P is a semiconductor integrated circuit containing 4 R-S flip-flop circuits.

FEATURES

- High breakdown input voltage ($V_I \geqq 15V$)
- High breakdown output voltage ($V_O \geqq 7V$)
- Low power dissipation (P_d = 19mW typical)
- Low output impedance
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

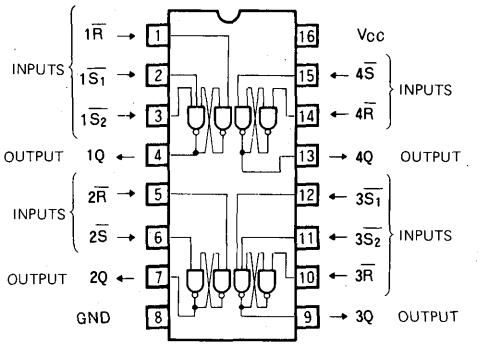
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

Two of the 4 circuits have set inputs $\overline{S}_1$ and $\overline{S}_2$ and reset input $\overline{R}$ and the other 2 circuits have $\overline{S}$ and $\overline{R}$ inputs.

When $\overline{S_1}$ or $\overline{S_2}$ or both are low or $\overline{S}$ is low, high appears in output Q, and when R is low, low appears in output Q. When $\overline{S_1}$ or $\overline{S_2}$ or both are low and $\overline{R}$ is low, high appears in the output but when each of the inputs is set high at the same time, the status of Q cannot be anticipated.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTION TABLE (Note 1)

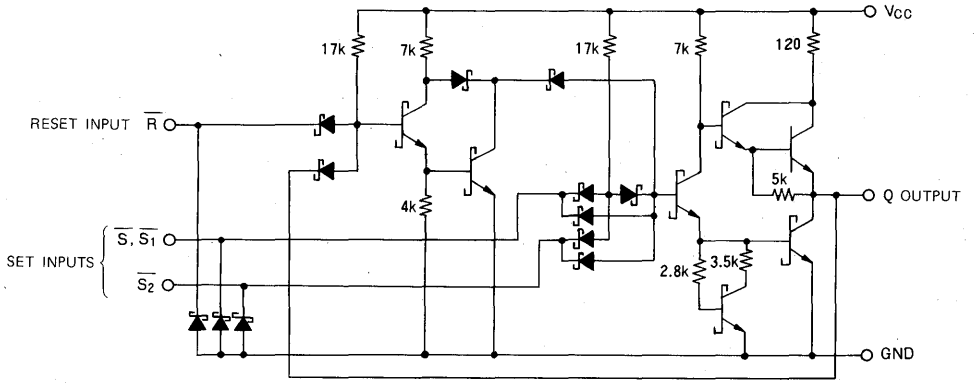
$\overline{S}_1$	$\overline{S_2}$	$\overline{R}$	Q
L	X	L	H*
X	L	L	H*
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	Q^0

Note 1 Q^0 : Level of Q before the indicated steady-state input conditions were established

X : Irrelevant

* : Nonstable, it will not persist when $\overline{R}$, $\overline{S_1}$ and $\overline{S_2}$ return to their inactive (high) level

CIRCUIT SCHEMATIC (EACH LATCH)



UNIT: Ω

QUADRUPLE R-S LATCH

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted.)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	℃
T_{stg}	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75V	I_{OL} = 4mA		0.25	0.4	V
		V_I = 0.8V, V_I = 2V	I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.25V V_I = 2.7V				20	μA
		V_{CC} = 5.25V V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC}	Supply current	V_{CC} = 5.25V (Note 3)			3.8	7	mA

* : All typical values are at V_{CC} = 5V, Ta = 25℃

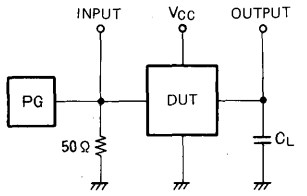
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all $\overline{R}$ inputs at 0V and all $\overline{S}$ inputs at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25℃, unless otherwise noted)

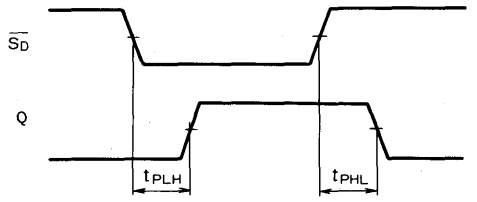
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{S}$ to output Q	C_L = 15pF (Note 4)		6	22	ns
t_{PHL}				12	21	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R}$ to output Q			12	27	ns

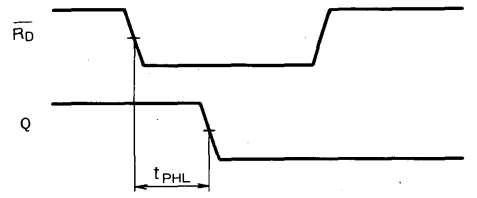
Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2). C_L includes probe and jig capacitance

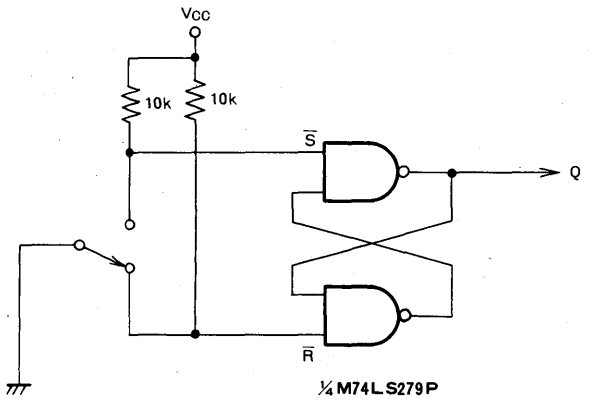
TIMING DIAGRAM (Reference level = 1.3V)





APPLICATION EXAMPLE

Chattering prevention circuit



¼M74LS279P

M74LS280P

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

DESCRIPTION

The M74LS280P is a semiconductor integrated circuit containing a 9-bit parity generator/checker function.

FEATURES

- Easy expansion of bits with cascade connection
- Wide operating temperature range (T_a=–20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

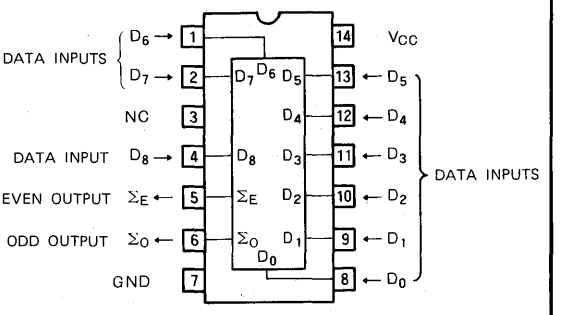
This device is provided with both a 9-bit parity generator and checker functions. For use as a parity generator, parity outputs in even output Σ_E and odd output Σ_O are obtained in accordance with the function table, depending on whether the number of high-level data in the inputs is even or odd when 9-bit data are applied to data inputs D_0~D_8.

For use as a parity checker, one of the 9-bit data inputs is used for the even or odd parity designation and the remaining 8 bits are used as the data.

FUNCTION TABLE

Number of high-level data in input data.	Σ_E	Σ_O
Even number	H	L
Odd number	L	H

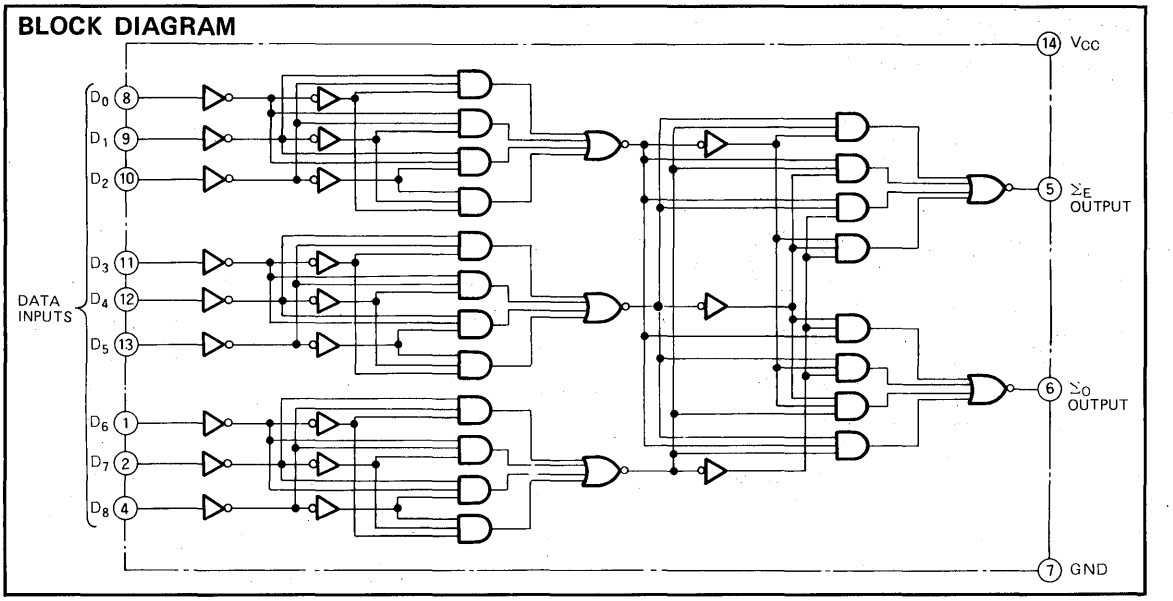
PIN CONFIGURATION (TOP VIEW)



NC : NO CONNECTION

Outline 14P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

9-BIT ODD/EVEN PARITY GENERATOR/CHECKER

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

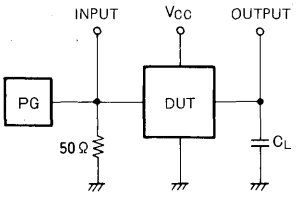
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
		V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 2)			16	27	mA

* : All typical values are at V_{CC}=5V, Ta=25°C.
Note 1: All measurements should be done quickly.
Note 2: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

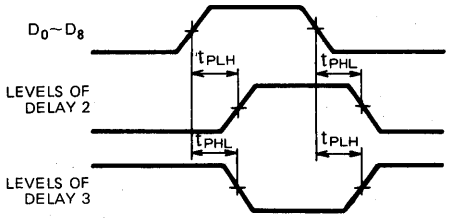
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_0 ~ D_8 to output Σ_E	C_L=15pF (Note 3)		22	50	ns
t_{PHL}				17	45	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_0 ~ D_8 to output Σ_O			16	35	ns
t_{PHL}				17	50	ns

Note 3: Measurement circuit



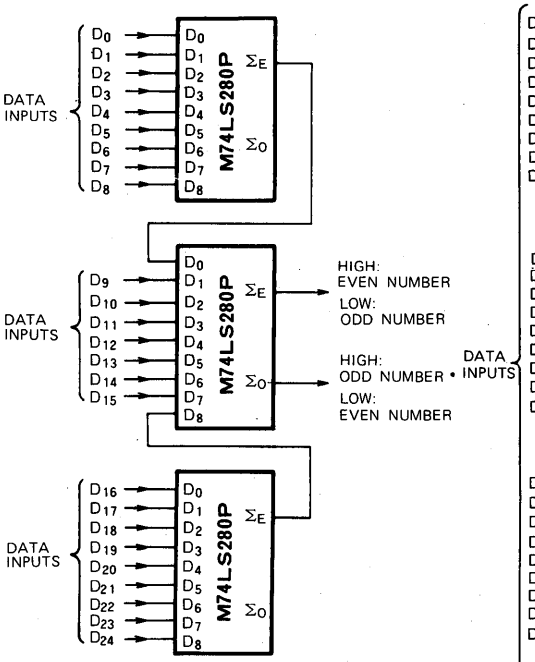
(1) The pulse generator (PG) has the following characteristics:
PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Z_O=50Ω.
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)

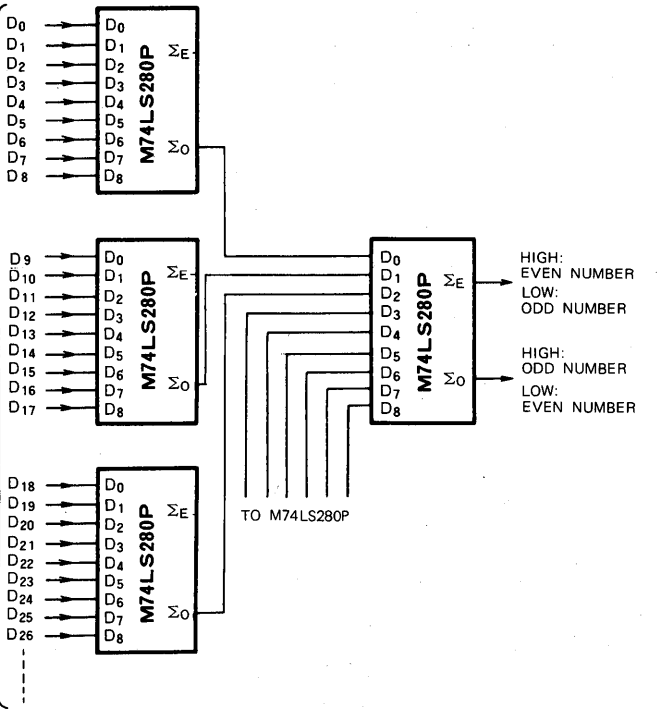


APPLICATIONS EXAMPLES

(1) 25-line parity generator/checker



(2) 81-line parity generator/checker



M74LS283P

4-BIT BINARY FULL ADDER WITH FAST CARRY

DESCRIPTION

The M74LS283P is a semiconductor integrated circuit containing a 4-bit full adder function using the look-ahead carry method of operation.

FEATURES

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Wide operating temperature range (Ta = −20 ~ +75°C)

APPLICATION

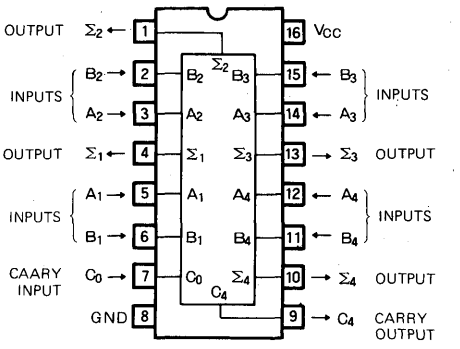
General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

This device functions as a 2-group, 4-bit binary adder with full adder capability. When a 4-bit binary number is applied to input A_1 thru A_4 or B_1 thru B_4 and a carry signal from the previous column is applied to input C_0, the sum output for the respective bits will appear at output $\Sigma_1 \sim \Sigma_4$; and carry output to the following column will appear at C_4.

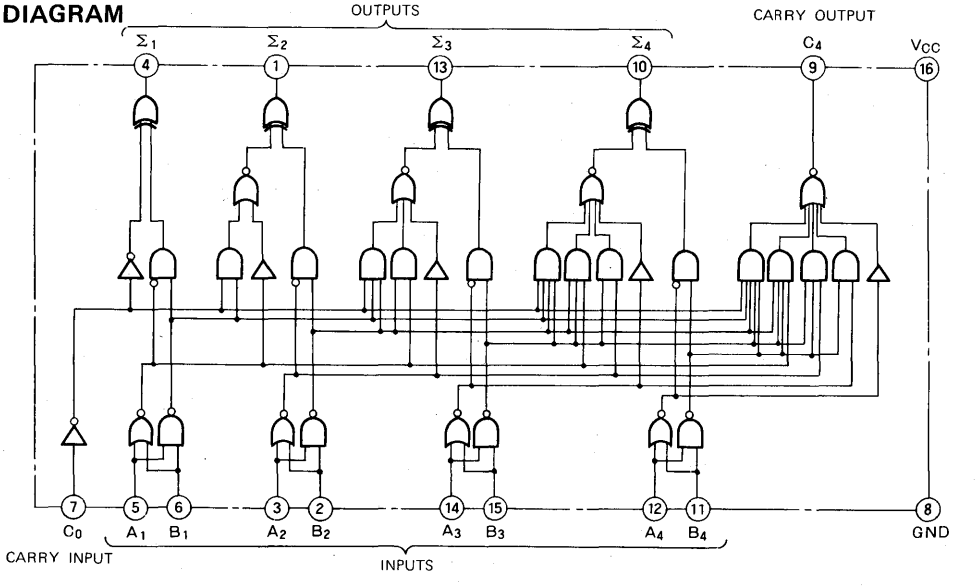
The full adder capability of this device is also complete with full look-ahead carry operations, and its high speed means that a 4-bit carry output is produced at an average rate of 8ns (typical). Thus, when N-stages are configured for parallel addition of an N-number of 4-bit inputs, a carry output can be obtained with a 8Nns delay time. (See the application example provided in the back of this specification sheet.) Also provided is the M74LS83AP with the same functions and electrical characteristics. This device differs only in its pin configuration.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



4-BIT BINARY FULL ADDER WITH FAST CARRY

FUNCTION TABLE (Note 1)

C_{k-1}	A_k	B_k	Σ_k	C_k
L	L	L	L	L
L	H	L	H	L
L	L	H	H	L
L	H	H	L	H
H	L	L	H	L
H	H	L	L	H
H	L	H	L	H
H	H	H	H	H

Note 1. Σ_K and C_K are the sum and carry output calculated in response to input at A_K, B_K, and C_{K-1} (carry input), derived from the following logical equation.

$\Sigma_K = A_K \oplus B_K \oplus C_{K-1}$

$C_K = A_K \cdot B_K + (A_K + B_K) \cdot C_{K-1}$

(Where K = 1~4; $\oplus$ = Exclusive OR; + = OR; · = AND)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	°C
T_{stg}	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	C_0	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$A_1 \sim A_4$, $B_1 \sim B_4$					40	
		C_0	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$A_1 \sim A_4$, $B_1 \sim B_4$					0.2	
I_{IL}	Low-level input current	C_0	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$A_1 \sim A_4$, $B_1 \sim B_4$					−0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$, $V_I=0V$			22	39	mA
			$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$ (Note 3)			19	34	
			$V_{CC}=5.25V$, $V_I=4.5V$			19	34	

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

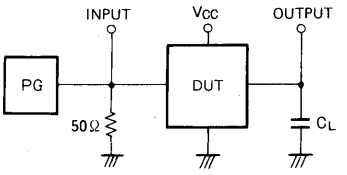
Note 3. I_{CC} is measured with $B_1 \sim B_4$ at 0V and with all other inputs 4.5V.

4-BIT BINARY FULL ADDER WITH FAST CARRY

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

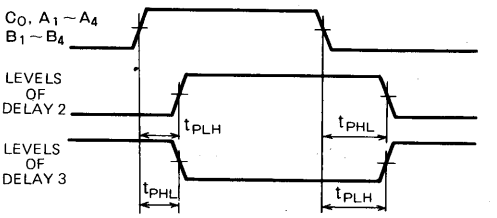
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input C_0 to outputs Σ_1~Σ_4	C_L=15pF (Note 4)		12	24	ns
t_{PHL}				13	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs A_1~A_4 or B_1~B_4 to outputs Σ_1~Σ_4			9	24	ns
t_{PHL}				11	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs C_0 to output C_4			8	17	ns
t_{PHL}				8	22	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs A_1~A_4 or B_1~B_4 to output C_4			8	17	ns
t_{PHL}				8	17	ns

Note 4. Measurement Circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

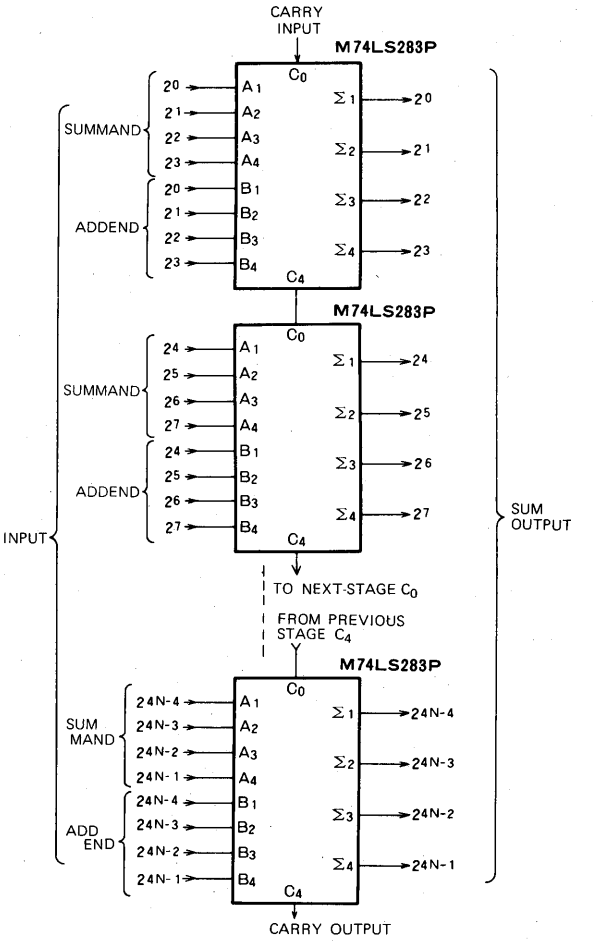
TIMING DIAGRAM (Reference level = 1.3V)



APPLICATION EXAMPLE

The accompanying diagram shows an N-number of M74LS283P devices connected in parallel for addition of an N-number of 4-bit inputs. Typical delay times for carry output in this circuit configuration are listed below. This figures indicates the suitability of this device for use in a high-speed adder employing the ripple-carry method.

N=1	(4 bits)	10.5ns
N=2	(8 bits)	21ns
N=3	(12 bits)	31.5ns
N=4	(16 bits)	42ns
N=8	(32 bits)	84ns



M74LS290P

DECADE COUNTER

DESCRIPTION

The M74LS290P is a semiconductor integrated cirucit containing an asynchronous decade counter function with direct reset and direct 9-set inputs.

FEATURES

- Direct reset inputs provided
- Direct 9-set inputs provided
- Usable independently as binary and divide-by-5 counter
- High-speed counting (f_{max}= 75MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

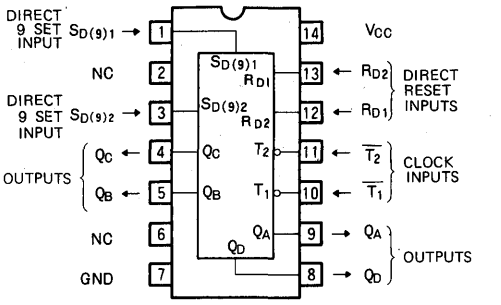
FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-5 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B, Q_C and Q_D are employed for use as a divide-by-5 counter. When employed as a decade counter, Q_A and $\overline{T_2}$ are connected and by making $\overline{T_1}$ the input, the BCD code output appears in outputs Q_A, Q_B, Q_C and Q_D. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ are changed from high to low.

The binary and divide-by-5 counters can be reset or set to 9 simultaneously by setting direct reset inputs R_{D1} and R_{D2} and direct 9 set inputs $S_{D(9)1}$ and $S_{D(9)2}$ high. For use as a counter, either R_{D1} or R_{D2}, or both, and $S_{D(9)1}$ or $S_{D(9)2}$, or both, are set low.

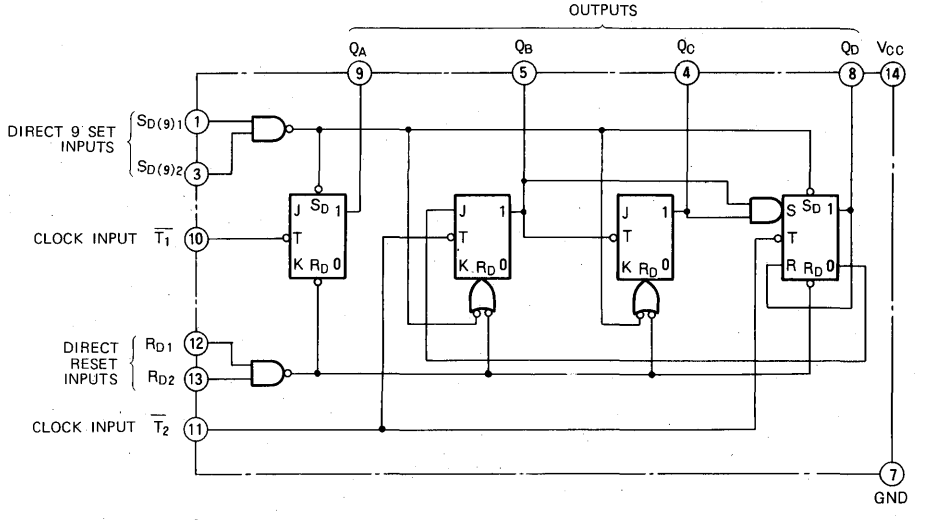
Also provided is the M74LS90P with the same functions and electrical characteristics. This device differs only in its pin configuration.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC : NO CONNECTION

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

DECADE COUNTER

FUNCTION TABLE (Note 1)

$\overline{T}$	R_{D1}	R_{D2}	$S_{D(9)1}$	$S_{D(9)2}$	Q_A	Q_B	Q_C	Q_D
X	H	H	L	X	L	L	L	L
X	H	H	X	L	L	L	L	L
X	X	X	H	H	H	L	L	H
↓	L	X	L	X	Count			
↓	X	L	X	L	Count			
↓	L	X	X	L	Count			
↓	X	L	L	X	Count			

Note 1: ↓ : Transition from high to low
X : Irrelevant

Count number	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

(1) Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75℃, unless other wise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltae	Inputs $\overline{T_1}$, $\overline{T_2}$	−0.5 ~ +5.5	V
		Inputs R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	−0.5 ~ +15	
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	HIgh-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltate		V_{CC}=4.75V	I_{OL}=4 mA (Note 2)		0.25	0.4	V
			V_I=0.8V, V_I=2V	I_{OL}=8 mA (Note 2)		0.35	0.5	V
I_{IH}	High-level input current	R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	V_{CC}=5.25V, V_I=2.7V				20	μA
		$\overline{T_1}$					40	
		$\overline{T_2}$					80	
		$\overline{T_1}$	V_{CC}=5.25V, V_I=5.5V				0.2	mA
		$\overline{T_2}$					0.4	
		R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	R_{D1}, R_{D2}, $S_{D(9)1}$, $S_{D(9)2}$	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
		$\overline{T_1}$					−2.4	
		$\overline{T_2}$					−3.2	
I_{OS}	Short-circuit output current (Note 3)		V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 4)			9	15	mA

* : All typical values are at V_{CC}=5V, T_a=25℃.

Note 2: Output Q_A should be tested with input $\overline{T_2}$ connected to output Q_A.

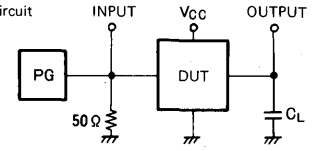
Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 4: I_{CC} is measured with $\overline{T_1}$, $\overline{T_2}$, $S_{D(9)1}$ and $S_{D(9)2}$ at 0V after R_{D1} and R_{D2} have been set to 0V after 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A	C_L= 15pF (Note 5)	32	75		MHz
fmax	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	30		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_A			7	16	ns
t_{PHL}				8	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_B			15	48	ns
t_{PHL}				16	50	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_C			7	16	ns
t_{PHL}				8	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_D			15	32	ns
t_{PHL}				15	35	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_D			7	32	ns
t_{PHL}				8	35	ns
t_{PHL}	Low-to-high-level output propagation time, from inputs $S_{D(9)1}$, $S_{D(9)2}$ to outputs Q_A, Q_D			17	40	ns
t_{PLH}	High-to-low-level output propagation time, from inputs $S_{D(9)1}$, $S_{D(9)2}$ to outputs Q_B, Q_C			10	30	ns
t_{PHL}	High-to-low-level output propagation time, from inputs R_{D1}, R_{D2} to outputs Q_A, Q_B, Q_C, Q_D			14	40	ns

Note 5: Measurement circuit

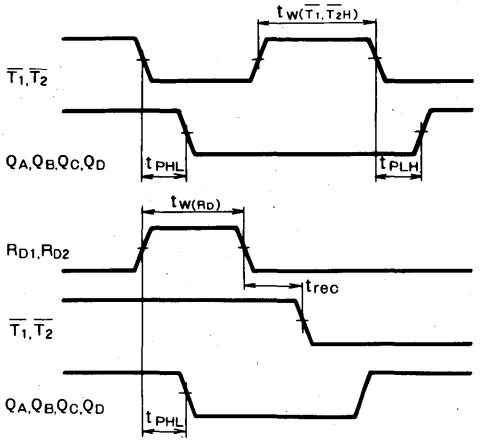


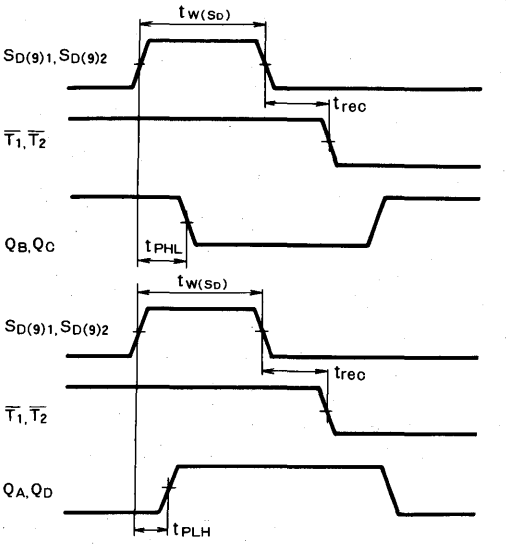
(1) The pusle generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Zo = 50Ω.
(2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}= 5 V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T_1}H)}$	Clock input $\overline{T_1}$ high pulse width		15	6		ns
$t_{w(\overline{T_2}H)}$	Clock input $\overline{T_2}$ high pulse width		30	17		ns
$t_{w(R_D)}$	Direct reset R_{D1}, R_{D2} pulse width		15	5		ns
$t_{w(S_D)}$	Direct 9 set $S_{D(9)1}$, $S_{D(9)2}$ pulse width		15	5		ns
t_r	Clock pulse rise time			500	100	ns
t_f	Clock pulse fall time			200	100	ns
$t_{rec(R_D)}$	Recovery time R_{D1}, R_{D2} to $\overline{T_1}$, $\overline{T_2}$		25	8		ns
$t_{rec(S_D)}$	Recovery time $S_{D(9)1}$, $S_{D(9)2}$ to $\overline{T_1}$, $\overline{T_2}$		25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)





MITSUBISHI ELECTRIC

M74LS293P

4-BIT BINARY COUNTER

DESCRIPTION

The M74LS293P is a semiconductor integrated circuit containing an asynchronous 4-bit binary (hexademical) counter function with direct reset inputs.

FEATURES

- Direct reset inputs provided
- Usable independently as binary and octal counter
- High-speed counting (f_{max}= 60MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

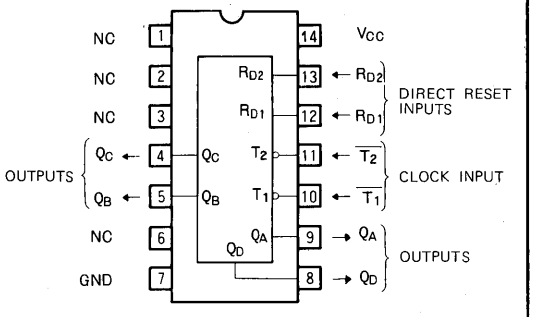
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of independent binary and octal counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and Q_B, Q_C and Q_D are employed for use as an octal counter. When employed as a hexadecimal counter, the pure binary code output appears in the Q_A, Q_B, Q_C and Q_D outputs by connecting Q_A and $\overline{T_2}$ and making $\overline{T_1}$ the input. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ change from high to low.

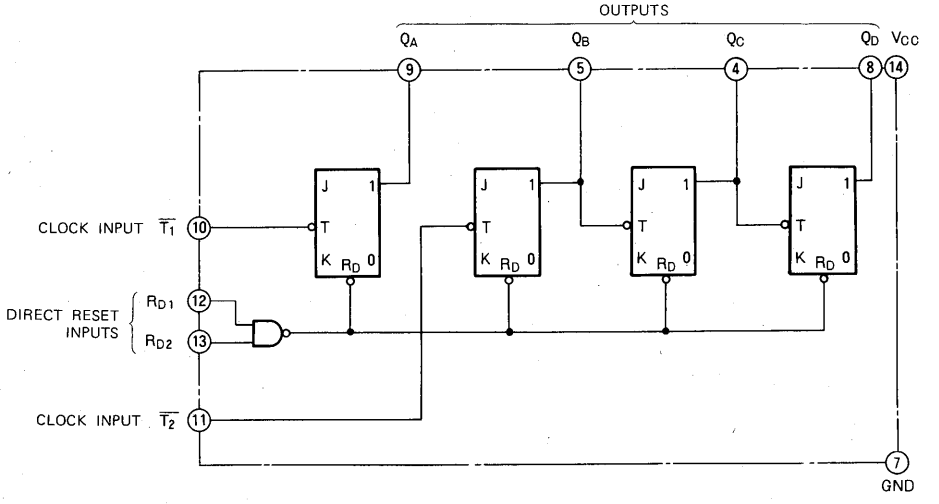
The binary and octal counters can be reset simultaneously by setting direct reset inputs R_{D1} and R_{D2} high. For use as a counter, either R_{D1} or R_{D2}, or both, is set low. This pin has the same functions and electrical characteristics as the M74LS93P; only its pin configuration is different.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC : NO CONNECTION

BLOCK DIAGRAM



4-BIT BINARY COUNTER

FUNCTION TABLE (Note 1)

$\overline{T}$	R_{D1}	R_{D2}	Q_A	Q_B	Q_C	Q_D
X	H	H	L	L	L	L
↓	L	H	Count			
↓	H	L	Count			
↓	L	L	Count			

Note 1 ↓ : Transition from high to low
X : Irrelevant

Count number	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS
(T_a = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	−0.5 ~ +5.5	V
		Inputs R_{D1}, R_{D2}	−0.5 ~ +15	
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	HIgh-level output voltage		V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V	I_{OL} = 4mA (Note 2)		0.25	0.4	V
			V_I = 0.8V, V_I = 2V	I_{OL} = 8mA (Note 2)		0.35	0.5	V
I_{IH}	High-level input current	R_{D1}, R_{D2}	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		$\overline{T_1}$, $\overline{T_2}$					40	
		$\overline{T_1}$, $\overline{T_2}$	V_{CC} = 5.25V, V_I = 5.5V				0.2	mA
		R_{D1}, R_{D2}	V_{CC} = 5.25V, V_I = 10V				0.1	
I_{IL}	Low-level input current	R_{D1}, R_{D2}	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
		$\overline{T_1}$					−2.4	
		$\overline{T_2}$					−1.6	
I_{OS}	Short-circuit output current (Note 3)		V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25V (Note 4)			9	15	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2: Output Q_A should be tested with input T_2 connected to output Q_A.
Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 4: I_{CC} is measured with $\overline{T_1}$ and $\overline{T_2}$ at 0V after R_{D1} and R_{D2} have been set to 0V after 4.5V.

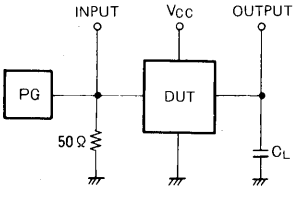
SWITCHING CHARACTERISTICS (V_{CC}= 5 V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A	C_L=15pF (Note 5)	32	60		MHz
f_{max}	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		16	35		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_A			7	16	ns
t_{PHL}				8	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_D			28	70	ns
t_{PHL}				28	70	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_B			7	16	ns
t_{PHL}				8	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_C			15	32	ns
t_{PHL}				15	35	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_D			22	51	ns
t_{PHL}				22	51	ns
t_{PHL}	High-to-low-level output propagation time, from inputs R_{D1}, R_{D2} to outputs Q_A, Q_B, Q_C, Q_D			17	40	ns

TIMING REQUIREMENTS (V_{CC}= 5 V, T_a=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T_1}H)}$	Clock input $\overline{T_1}$ high pulse width		15	6		ns
$t_{w(\overline{T_2}H)}$	Clock input $\overline{T_2}$ high pulse width		30	15		ns
$t_{w(RD)}$	Direct reset R_{D1}, R_{D2} pulse width		15	5		ns
t_r	Clock pulse rise time			500	100	ns
t_f	Clock pulse fall time			200	100	ns
$t_{rec(RD)}$	Recovery time R_{D1}, R_{D2} to $\overline{T_1}$, $\overline{T_2}$		25	8		ns

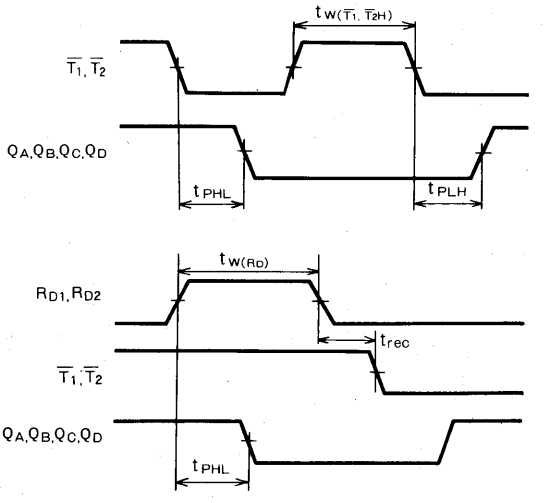
Note 5: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_{P-P}, Zo = 50Ω.

(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



M74LS295BP

4-BIT SHIFT REGISTER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS295BP is a semiconductor integrated circuit containing a 3-state output 4-bit serial/parallel input serial/parallel output shift register function.

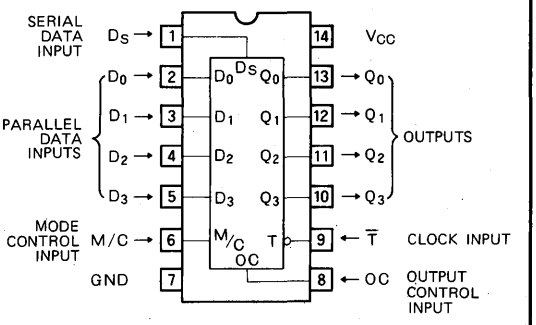
FEATURES

- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection
- Mode control input provided
- Output control input provided
- Usable in AND-Tie connection (3-state output provided)
- Wide operating temperature range (T_a= −20~+75°C)
- High fan-out (I_{OL} = 24mA, I_{OH} = −2.6mA)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)

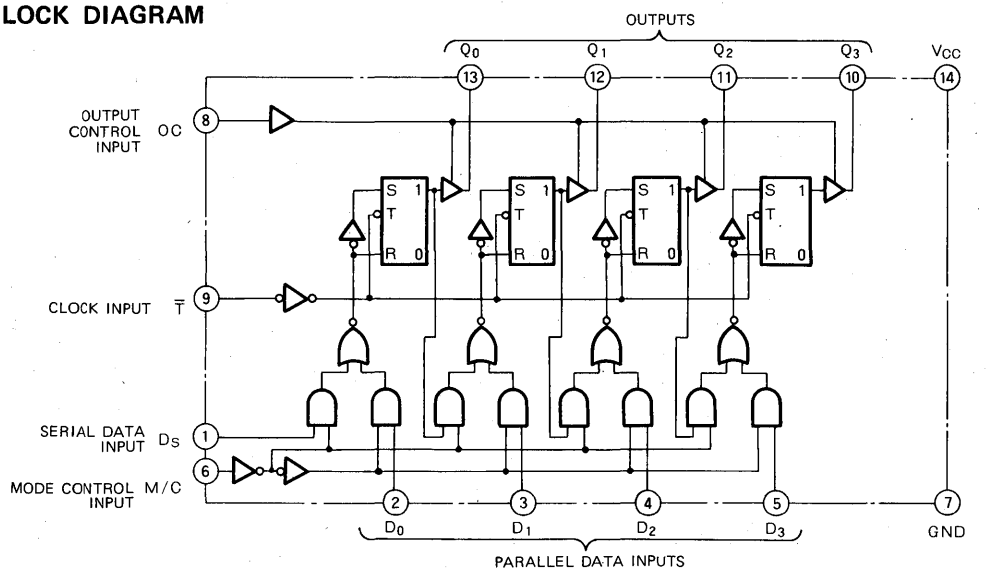


Outline 14P4

FUNCTIONAL DESCRIPTION

This device is usable as a serial input-serial/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept in low, the serial data are applied to serial data input D_S and the clock pulse is applied to clock input $\overline{T}$, the serial data are shifted into outputs Q_0~Q_3 sequentially in synchronization with the clock pulse. When M/C is kept in high, the parallel data are applied to parallel data inputs D_0~D_3 and the 1-bit clock pulse is applied to clock input $\overline{T}$, the signals D_0~D_3 appear in Q_0~Q_3 respectively. When $\overline{T}$ changes from high to low, the right shift or parallel data reading operation is performed. When M/C is kept in high, Q_3 is connected with D_2, Q_2 with D_1 and Q_1 with D_0, the serial data are applied to D_3 and the clock pulse applied to $\overline{T}$, the left shift operation is performed. When low is applied to output control input OC, Q_0~Q_3 are put in the high-impedance state and AND-tie connection is enabled. Even when OC is changed, there are no effects on the shift and parallel data reading operations. When a low-level signal is applied to OC with an expansion in the bit number due to the high-impedance state and so shifting is disabled. In cases like this, the M74LS395AP with cascade output Q_3' is recommended.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

4-BIT SHIFT REGISTER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

Function mode	Input							Output			
	M/C	$\overline{T}$	D_S	Parallel Data				Q_0	Q_1	Q_2	Q_3
				D_0	D_1	D_2	D_3				
Output hold	H	H	X	X	X	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0
Parallel read	H	↓	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3
Left shift	H	↓	X	Q_1^+	Q_2^+	Q_3^+	D_3	Q_1^0	Q_2^0	Q_3^0	D_3
Output hold	L	H	X	X	X	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0
Right shift	L	↓	H	X	X	X	X	H	Q_0^0	Q_1^0	Q_2^0
	L	↓	L	X	X	X	X	L	Q_0^0	Q_1^0	Q_2^0

Note 1: ↑ : transition from low to high level (negative edge trigger)
Q^0 : level of Q before the indicated steady-state input conditions were established
X : irrelevant
Q^+ : D_0 and Q_1, D_1 and Q_2, and D_2 and Q_3 are connected externally and serial data are applied to D3
High-impedance state when OC is low.

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

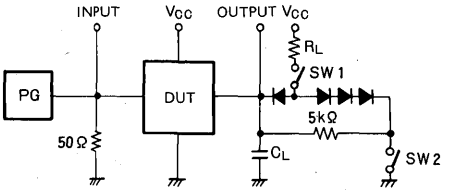
Symbol	Parameter	Test condotions	Limits			Unit
			Min	Typ *	Max	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−2.6mA	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V, I_{OL}=12mA		0.25	0.4	V
		V_I=0.8V, V_I=2V, I_{OL}=24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current	V_{CC}=5.25V, V_I=0.8V, V_O=2.7V			20	μA
I_{OZL}	Off-state low-level output current	V_{CC}=5.25V, V_I=0.8V, V_O=0.4V			−20	μA
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V			20	μA
		V_{CC}=5.25V, V_I=10V			0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V			−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC}=5.25V, V_O= 0 V	−30		−130	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 3)		20	29	mA
I_{CCZ}	Supply current, all outputs off	V_{CC}=5.25V (Note 4)		22	33	mA

* : All typical values are at V_{CC}=5V, Ta=25°C.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with D_0~D_3 at 0V, D_S, M/C and 0C at 4.5V after $\overline{T}$ has been set from 3V to 0V.
Note 4: I_{OCZ} is measured with D_0~D_3, 0C and $\overline{T}$ at 0V and D_S and M/C at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency		30	40		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T}$ to outputs $Q_0 \sim Q_3$	C_L=15pF (Note 5)		15	20	ns
t_{PHL}				18	30	ns
t_{PZH}	Output enable time to high-level	R_L=2kΩ, C_L=15pF (Note 5)		14	26	ns
t_{PZL}	Output enable time to low-level	R_L=2kΩ, C_L=15pF (Note 5)		16	30	ns
t_{PHZ}	Output disable time from high-level	R_L=2kΩ, C_L=5pF (Note 5)		14	20	ns
t_{PLZ}	Output disable time from low-level	R_L=2kΩ, C_L=5pF (Note 5)		14	20	ns

Note 5: Measurement circuit



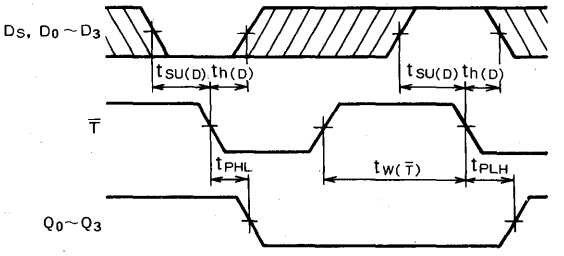
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

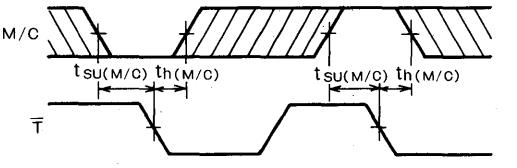
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_o = 50Ω
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns)
(3) C_L includes probe and jig capacitance

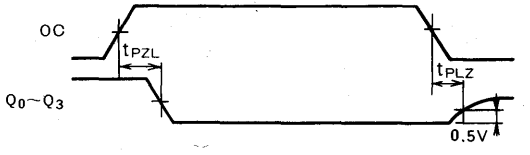
TIMING REQUIREMENTS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

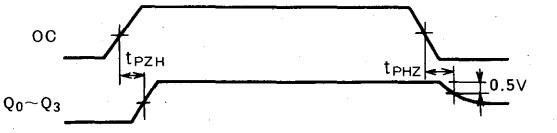
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T})}$	Clock input $\overline{T}$ high pulse width		25	10		ns
$t_{su(D)}$	Setup time D to $\overline{T}$		20	3		ns
$t_{su(M/C)}$	Setup time M/C to $\overline{T}$		40	20		ns
$t_{h(D)}$	Hold time D to $\overline{T}$		20	−1		ns
$t_{h(M/C)}$	M/C hold time to $\overline{T}$		0	−10		ns

TIMING DIAGRAM (Reference level = 1.3V)









Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS298P

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

DESCRIPTION

The M74LS298P is a semiconductor integrated circuit which containing four 2-line to 1-line multiplexers provided with a temporary storage circuit with common selection input and clock input.

FEATURES

- One line data can be selected from 2-line data.
- Equipped with D-type negative edge-triggered flip-flop.
- Wide operating temperature range (T_a = -20 ~ +75°C)

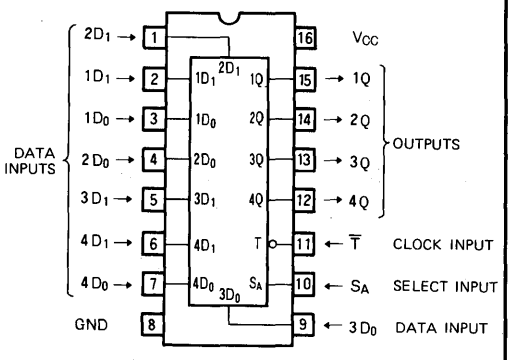
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When the select input S_A is low, data input D_0 is selected, and when it is high, data input D_1 is selected. When the clock input $\overline{T}$ changes from high to low, the selected data appears in the output Q. Since a D-type negative edge-triggered flip-flop is used as a temporary storage circuit, the status of Q does not change even if D is changed, whether $\overline{T}$ is high or low.

PIN CONFIGURATION (TOP VIEW)



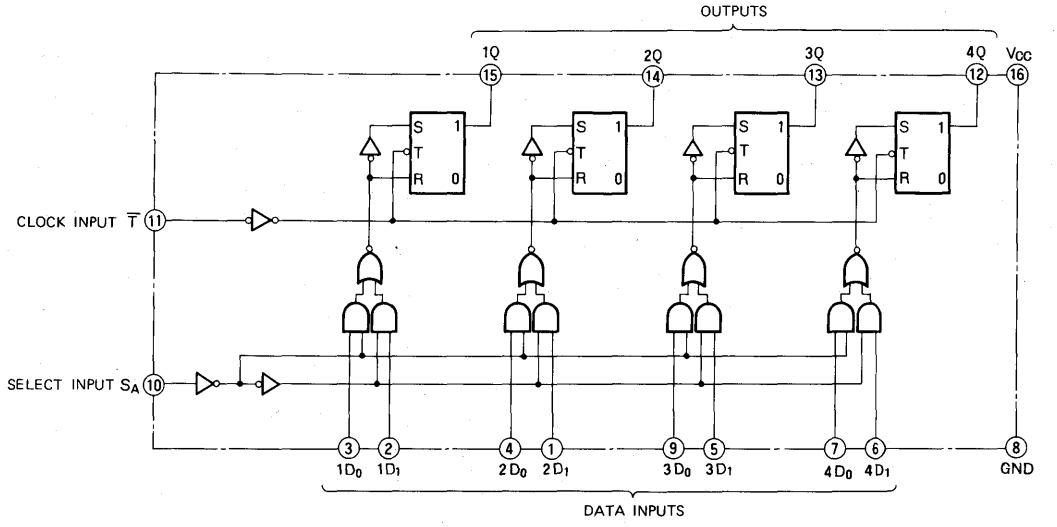
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{T}$	S_A	D_0	D_1	Q
↓	L	L	X	L
↓	L	H	X	H
↓	H	X	L	L
↓	H	X	H	H

Note 1: ↓ : transition from high to low-level
X : irrelevant

BLOCK DIAGRAM



QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V, V_I = 0.8V V_I = 2V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75V	I_{OL} = 4mA		0.25	0.4	V
		V_I = 0.8V, V_I = 2V	I_{OL} = 8mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current	V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC} = 5.25V, V_O = 0V		−20		−100	mA
I_{CC}	Supply current	V_{CC} = 5.25V (Note 3)			13	21	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

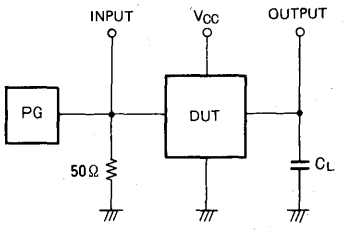
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

3: I_{CC} is measured with S_A, $1D_0$ ~ $4D_1$ inputs grounded and a momentary 4.5V, then grounded, applied $\overline{T}$ input.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T}$ to outputs 1Q ~ 4Q	C_L = 15pF (Note 4)		12	27	ns
t_{PHL}				11	32	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
V_P = 3V_{P-P}, Z_O = 50Ω

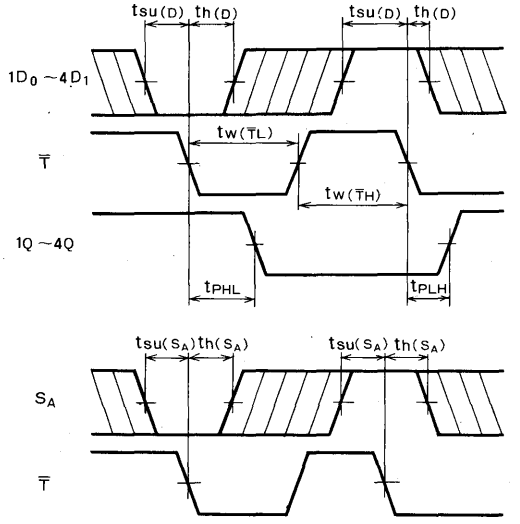
(2) C_L includes probe and jig capacitance.

QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T}H)}$	Clock input $\overline{T}$ high pulse width		20	7		ns
$t_{w(\overline{T}L)}$	Clock input $\overline{T}$ low pulse width		20	4		ns
t_f	Clock pulse fall time		15	0		ns
$t_{SU(D)}$	Setup time data input to $\overline{T}$		15	0		ns
$t_{SU(S_A)}$	Setup time S_A to $\overline{T}$		25	5		ns
$t_{h(D)}$	Hold time data input to $\overline{T}$		5	0		ns
$t_{h(S_A)}$	Hold time S_A to $\overline{T}$		0	−2		ns

TIMING DIAGRAM (Reference level = 1.3V)



Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS299P

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

DESCRIPTION

The M74LS299P is a semiconductor integrated circuit containing an 8-bit serial/parallel input-parallel output shift register function equipped with 3-state outputs and direct reset input.

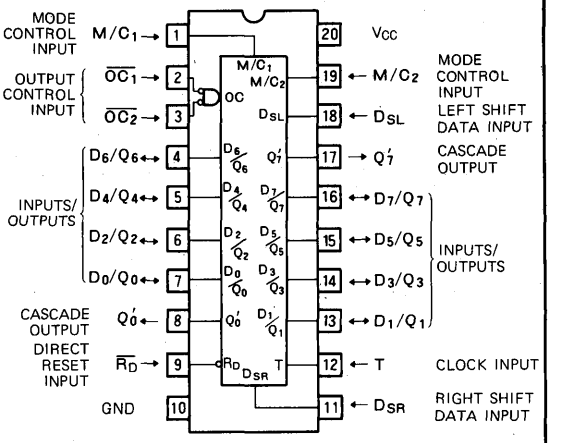
FEATURES

- Synchronous serial/parallel input-serial/parallel input
- Right shift and left shift functions
- Possible expansion of bit number
- 3-state outputs
- Common parallel input and output pins
- Direct reset input
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTIONAL DESCRIPTION

The operational modes listed below can be selected by combining the mode control inputs M/C_1 and M/C_2.

(1) Parallel read	M/C_1:	High;	M/C_2:	High
(2) Right shift	M/C_1:	High;	M/C_2:	Low
(3) Left shift	M/C_1:	Low;	M/C_2:	High
(4) Clock inhibit	M/C_1:	Low;	M/C_2:	Low

With parallel read, the 8-bit parallel data are applied to inputs/outputs D_0/Q_0~D_7/Q_7 and when the clock input T changes from low to high, the data are stored in each of the respective flip-flops.

With right shift, when the parallel data are applied to the right shift data input DSR, a shift is made one bit at a time from D_0/Q_0 to D_7/Q_7 every time the clock input T changes from low to high.

With left shift, when the parallel data are applied to the left shift data input D_{SL}, a shift is made one bit at a time from D_7/Q_7 to D_0/Q_0 every time the clock input T changes from low to high.

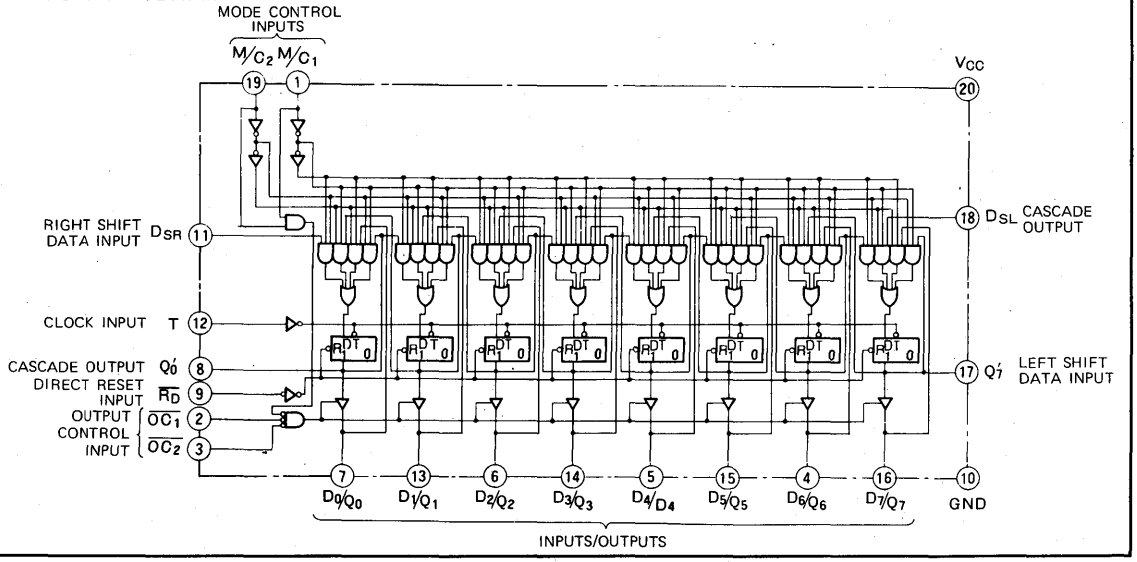
With clock inhibit, the flip-flop status does not change since the clock pulses are inhibited from being applied to the flip-flop.

When one or both $\overline{OC_1}$ and $\overline{OC_2}$ are set high, all D_0/Q_0~D_7/Q_7 outputs are put in the high-impedance mode "Z." The contents of the flip-flop do not change even if $\overline{OC_1}$ and $\overline{OC_2}$ are changed.

When $\overline{R_D}$ is set low, all the flip-flops are set low irrespective of the status of the other inputs.

Cascade outputs Q'_0 and Q'_7 are used for expansion of the respective bit numbers. Reference should be made to the typical application.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

FUNCTION TABLE (Note 1)

Operational mode	$\overline{R_D}$	T	M/C_1	M/C_2	D_{SR}	D_{SL}	$\overline{OC_1}$	$\overline{OC_2}$	D_0/Q_0	D_1/Q_1	D_2/Q_2	D_3/Q_3	D_4/Q_4	D_5/Q_5	D_6/Q_6	D_7/Q_7	Q'_0	Q'_7
Direct reset	L	X	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L
	L	X	X	L	X	X	L	L	L	L	L	L	L	L	L	L	L	L
Right shift	H	↑	H	L	L	X	L	L	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	L	Q_6^0
	H	↑	H	L	H	X	L	L	H	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	H	Q_6^0
Left shift	H	↑	L	H	X	L	L	L	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	L	Q_1^0	L
	H	↑	L	H	X	H	L	L	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_4^0	Q_6^0	Q_7^0	H	Q_1^0	H
Parallel read	H	↑	H	H	X	X	L	L	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_7
Clock inhibit	H	X	L	L	X	X	L	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	Q_0^0	Q_7^0
	H	L	X	X	X	X	L	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	Q_0^0	Q_7^0
Output inhibit ($D_0/Q_0 \sim D_7/Q_7$ are put in the high-impedance state)	X	X	X	X	X	X	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Q_0^0	Q_7^0
	X	X	X	X	X	X	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Q_0^0	Q_7^0
	X	X	X	X	X	X	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Q_0^0	Q_7^0

Note 1. Q_n^0 : level of Q before the indicated steady-state input conditions were established
X : Irrelevant
↑ : Transition from low to high (positive edge trigger)
Dn : $D_0/Q_0 \sim D_7/Q_7$ function as inputs. Q'_0 and Q'_7 are set to the same status as D_0 and D_7, respectively.
Z : High-impedance state. Status of flip-flops before $D_0/Q_0 \sim D_7/Q_7$ were put in the high-impedance mode is held.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage			−0.5 ~ +15	V
V_O	Output voltage	$D_0/Q_0 \sim D_7/Q_7$	Off-state	−0.5 ~ +5.5	V
		Q'_0, Q'_7	High-level state	−0.5 ~ +V_{CC}	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage			4.75	5	5.25	V
I_{OH}	High-level output current	$D_0/Q_0 \sim D_7/Q_7$	$V_{OH} \geqq 2.4V$	0		−2.6	mA
		Q'_0, Q'_7	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$D_0/Q_0 \sim D_7/Q_7$	$V_{OL} \leqq 0.4V$	0		12	mA
			$V_{OL} \leqq 0.5V$	0		24	mA
		Q'_0, Q'_7	$V_{OL} \leqq 0.4V$	0		4	mA
			$V_{OL} \leqq 0.5V$	0		8	mA

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	$D_0/Q_0 \sim D_7/Q_7$	V_{CC}=4.75V	I_{OH}=−2.6mA	2.4	3.1		V
		Q_0', Q_7'	V_I=0.8V, V_I=2V	I_{OH}=−400μA	2.7	3.4		V
V_{OL}	Low-level output voltage	$D_0/Q_0 \sim D_7/Q_7$	V_{CC}=4.75V, V_I=0.8V	I_{OL}=12mA		0.25	0.4	V
				I_{OL}=24mA		0.35	0.5	V
		Q_0', Q_7'	V_I= 2 V	I_{OL}= 4 mA		0.25	0.4	V
				I_{OL}= 8 mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current	$D_0/Q_0 \sim D_7/Q_7$	V_{CC}=5.25V, V_I=2V, V_O=2.7V				40	μA
I_{OZL}	Off-state low-level output current	$D_0/Q_0 \sim D_7/Q_7$	V_{CC}=5.25V, V_I=2V, V_O=0.4V				−400	μA
I_{IH}	High-level input current	$D_0/Q_0 \sim D_7/Q_7$, M/C_1, M/C_2	V_{CC}=5.25V, V_I=2.7V				40	μA
		Onputs other then $D_0/Q_0 \sim D_7/Q_7$, M/C_1, M/C_2					20	μA
		$D_0/Q_0 \sim D_7/Q_7$	V_{CC}=5.25V	V_I=5.5V			100	μA
		M/C_1, M/C_2		V_I=10V			200	μA
		Onputs other then $D_0/Q_0 \sim D_7/Q_7$, M/C_1, M/C_2					100	μA
I_{IL}	Low-level input current	M/C_1, M/C_2	V_{CC}=5.25V				−0.8	mA
		Onput other then M/C_1, M/C_2	V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current	$D_0/Q_0 \sim D_7/Q_7$	V_{CC}=5.25V		−30		−130	mA
		Q_0', Q_7'	V_O=0V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V			33	53	mA

* : All typical values are at V_{CC} = 5V, Ta ≈ 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with inputs T and OC at 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L=15pF (Note 4)	25	28		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time from input T to outputs Q_0', Q_7'			20	33	ns
t_{PHL}				20	39	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to outputs Q_0', Q_7'			18	40	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$	C_L=45pF (Note 4)		17	25	ns
t_{PHL}				23	39	ns
t_{PHL}	High-to-low-level output propagation time, from inputs $\overline{R_D}$ to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$			20	40	ns
t_{PZH}	Output enable time to high-level	R_L=665Ω, C_L=45pF (Note 4)		12	21	ns
t_{PZL}	Output enable time to low-level	R_L=665Ω, C_L=45pF (Note 4)		15	30	ns
t_{PHZ}	Output disable time from high-level.	R_L=665Ω, C_L= 5pF (Note 4)		12	15	ns
t_{PLZ}	Output disable time from low-level	R_L=665Ω, C_L= 5pF (Note 4)		12	15	ns

TIMING REQUIREMENTS (V_{CC}= 5 V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(TH)}$	Clock input T high pulse width		20	13		ns
$t_{w(TL)}$	Clock input T low pulse width		20	17		ns
$t_{w(\overline{R_D}L)}$	Direct reset input low pulse width		20	7		ns
$t_{su(M/C)}$	Setup time M/C_1, M/C_2 to T		35	18		ns
$t_{su(D)}$	Setup time D_{SR}, D_{SL}, $D_0/Q_0 \sim D_7/Q_7$ to T		20	10		ns
$t_{h(M/C)}$	Hold time M/C_1, M/C_2 to T		10	−12		ns
$t_{h(D)}$	Hold time D_{SR}, D_{SL}, $D_0/Q_0 \sim D_7/Q_7$ to T		0	− 5		ns
$t_{rec(\overline{R_D})}$	Recovery time $\overline{R_D}$ to T		20	15		ns

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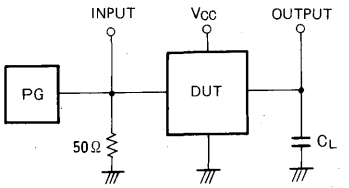
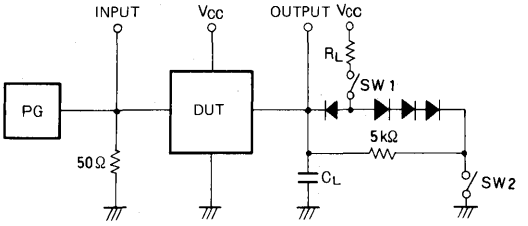
Note 4: Measurement circuit

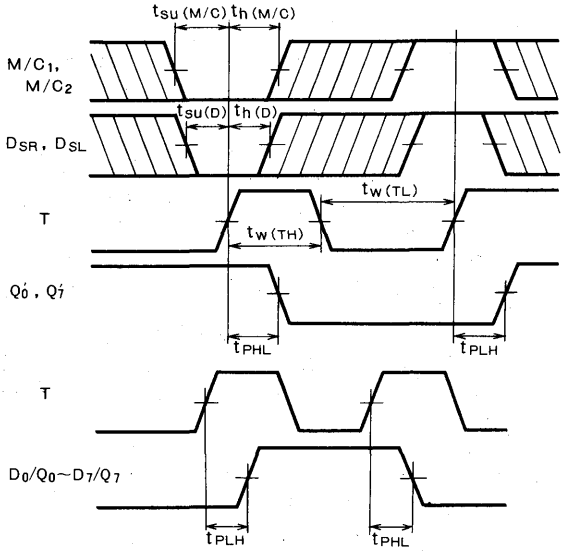


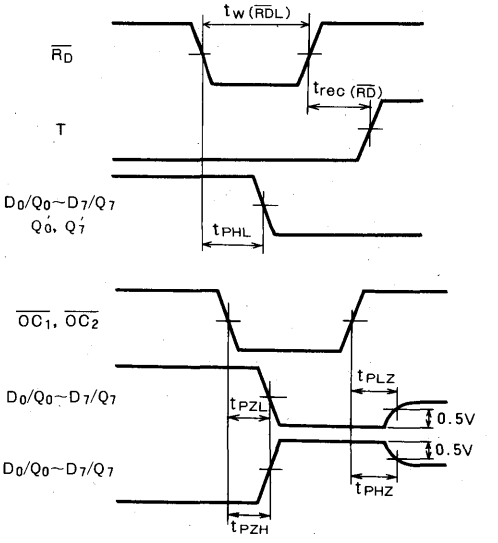


Symbol	SW 1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P=3V_{P-P}, Z_O=50Ω
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns)
(3) C_L includes probe and jig capacitance

TIMING DIAGRAM

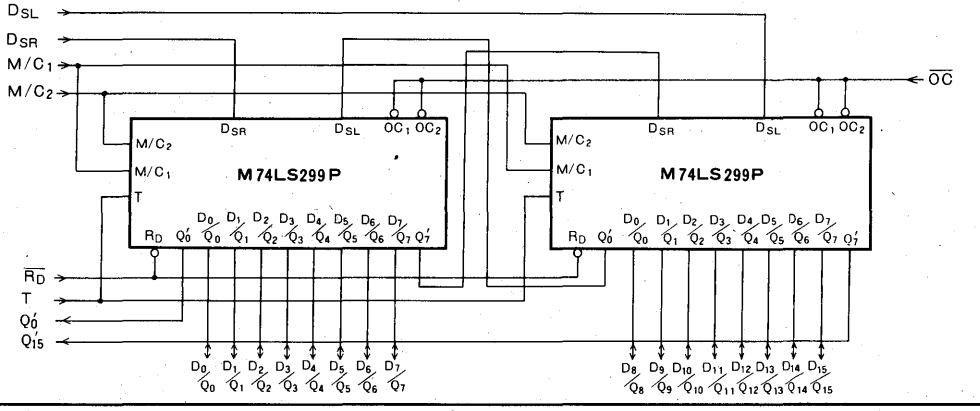




Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

The figure below shows the configuration of a 16-bit shift register using two M74LS299P devices.
Similarly, an 8n-bit shift register can be configured with n ICs.



M74LS323P

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

DESCRIPTION

The M74LS323P is a semiconductor integrated circuit containing an 8-bit serial/parallel input/parallel output shift register function equipped with 3-state outputs and synchronous reset input.

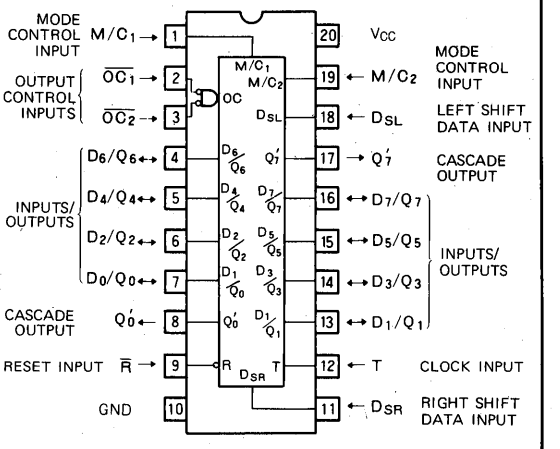
FEATURES

- Synchronous serial/parallel input/serial/parallel input
- Right shift and left shift functions
- Possible expansion of bit number
- 3-state outputs
- Common parallel input and output pins
- Synchronous reset input
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTIONAL DESCRIPTION

The operational modes listed below can be selected by combining the mode control inputs M/C_1 and M/C_2.

(1)	Parallel read	M/C_1:	High;	M/C_2: High
(2)	Right shift	M/C_1:	High;	M/C_2: Low
(3)	Left shift	M/C_1:	Low;	M/C_2: High
(4)	Clock inhibit	M/C_1:	Low;	M/C_2: Low

With parallel read, the 8-bit parallel data are applied to inputs/outputs D_0/Q_0~D_7/Q_7 and when the clock input T changes from low to high, the data are stored in each of the respective flip-flops.

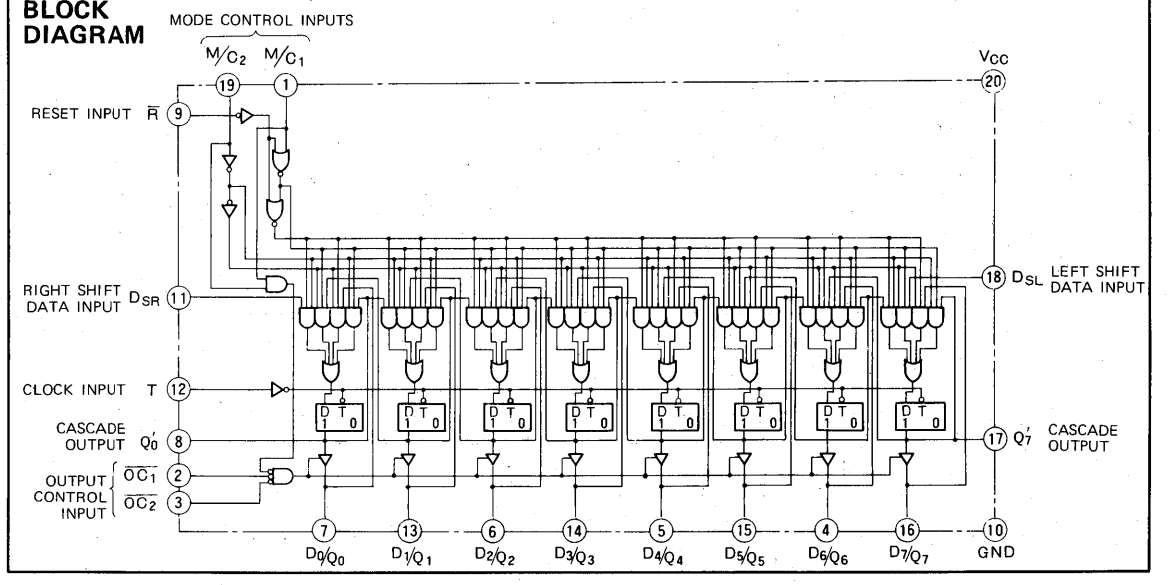
With right shift, when the parallel data are applied to the right shift data input D_{SR}, a shift is made one bit at a time from D_0/Q_0 to D_7/Q_7 every time the clock input T changes from low to high.

With left shift, when the parallel data are applied to the left shift data input D_{SL}, a shift is made one bit at a time from D_0/Q_0 to D_7/Q_7 every time the clock input T changes from low to high.

With clock inhibit, the flip-flop status does not change since the clock pulses are inhibited from being applied to the flip-flop.

When one or both $\overline{OC_1}$ and $\overline{OC_2}$ are set high, all D_0/Q_0~D_7/Q_7 outputs are put in the high-impedance mode "Z." The contents of the flip-flop do not change even if $\overline{OC_1}$ and $\overline{OC_2}$ are changed.

BLOCK DIAGRAM



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8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

When $\overline{R}$ is set low if $\overline{T}$ is changed from low to high, all the flip-flops are set low.

Cascade outputs Q'_0 and Q'_7 are used for expansion of the respective bit numbers. Reference should be made to the application example.

FUNCTION TABLE (Note 1)

Operational mode	$\overline{R}$	T	M/C_1	M/C_2	D_{SR}	D_{SL}	$\overline{OC_1}$	$\overline{OC_2}$	D_0/Q_0	D_1/Q_1	D_2/Q_2	D_3/Q_3	D_4/Q_4	D_5/Q_5	D_6/Q_6	D_7/Q_7	Q'_0	Q'_7
Reset	L	↑	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L
	L	↑	X	L	X	X	L	L	L	L	L	L	L	L	L	L	L	L
Right shift	H	↑	H	L	L	X	L	L	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	L	Q_6^0
	H	↑	H	L	H	X	L	L	H	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	H	Q_6^0
Left shift	H	↑	L	H	X	L	L	L	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	L	Q_1^0	L
	H	↑	L	H	X	H	L	L	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	Q	Q_1^0	H
Parallel read	H	↑	H	H	X	X	L	L	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_0	D_7
Clock inhibit	H	X	L	L	X	X	L	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	Q_0^0	Q_7^0
	H	L	X	X	X	X	L	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	Q_0^0	Q_7^0
Output inhibit ($D_0/Q_0 \sim D_7/Q_7$ are put in the high-impedance state	X	X	X	X	X	X	H	L	Z	Z	Z	Z	Z	Z	Z	Z	Q_0^0	Q_7^0
	X	X	X	X	X	X	L	H	Z	Z	Z	Z	Z	Z	Z	Z	Q_0^0	Q_7^0
	X	X	X	X	X	X	H	H	Z	Z	Z	Z	Z	Z	Z	Z	Q_0^0	Q_7^0

Note 1 Q_n^0 : level of Q before the indicated steady-state input conditions were established
X : Irrelevant
↑ : transition from low to high (positive edge trigger)
Dn : $D_0/Q_0 \sim D_7/Q_7$ were put in the high-impedance mode is held.
Z : High-impedance state. Status of flip-flops before $D_0/Q_7 \sim D_7/Q_7$ were put in the high-impedance mode is held.

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			$-0.5 \sim +7$	V
V_I	Input voltage			$-0.5 \sim +15$	V
V_O	Output voltage	$D_0/Q_0 \sim D_7/Q_7$	Off-state	$-0.5 \sim +5.5$	V
		Q'_0, Q'_7	High-level state	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range			$-20 \sim +75$	°C
Tstg	Storage temperature range			$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage			4.75	5	5.25	V
I_{OH}	High-level output current	$D_0/Q_0 \sim D_7/Q_7$	$V_{OH} \geqq 2.4V$	0		−2.6	mA
		Q'_0, Q'_7	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$D_0/Q_0 \sim D_7/Q_7$	$V_{OL} \leqq 0.4V$	0		12	mA
			$V_{OL} \leqq 0.5V$	0		24	mA
		Q'_0, Q'_7	$V_{OL} \leqq 0.4V$	0		4	mA
			$V_{OL} \leqq 0.5V$	0		8	mA

8-BIT UNIVERSAL SHIFT/STORAGE REGISTER

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$D_0/Q_0 \sim D_7/Q_7$	$V_{CC}=4.75V$	$I_{OH}=-2.6mA$	2.4	3.1		V
		Q_0', Q_7'	$V_I=0.8V$, $V_I=2V$	$I_{OH}=-400\mu A$	2.7	3.4		V
V_{OL}	Low-level output voltage	$D_0/Q_0 \sim D_7/Q_7$	$V_{CC}=4.75V$	$I_{OL}=12mA$		0.25	0.4	V
			$V_I=0.8V$	$I_{OL}=24mA$		0.35	0.5	V
		Q_0', Q_7'	$V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{OZH}	Off-state high-level output current	$D_0/Q_0 \sim D_7/Q_7$	$V_{CC}=5.25V$, $V_I=2V$, $V_O=2.7V$				40	μA
I_{OZL}	Off-state low-level output current	$D_0/Q_0 \sim D_7/Q_7$	$V_{CC}=5.25V$, $V_I=2V$, $V_O=0.4V$				−400	μA
I_{IH}	High-level input current	$D_0/Q_0 \sim D_7/Q_7$, M/C_1, M/C_2	$V_{CC}=5.25V$, $V_I=2.7V$				40	μA
		Input other then $D_0/Q_0 \sim D_7/Q_7$, M/C_1, M/C_2					20	μA
		$D_0/Q_0 \sim D_7/Q_7$	$V_{CC}=5.25V$	$V_I=5.5V$			100	μA
		M/C_1, M/C_2		$V_I=10V$			200	μA
		Inputs other then $D_0/Q_0 \sim D_7/Q_7$, M/C_1, M/C_2					100	μA
I_{IL}	Low-level input current	M/C_1, M/C_2	$V_{CC}=5.25V$				−0.8	mA
		Inputs other then M/C_1, M/C_2	$V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 1)	$D_0/Q_0 \sim D_7/Q_7$	$V_{CC}=5.25V$		−30		−130	mA
		Q_0', Q_7'	$V_O=0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 2)			33	53	mA

* : All typical values are at $V_{CC}=5V$, $Ta=25°C$.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with inputs T and $\overline{OC}$ at 4.5V..

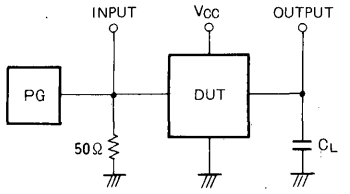
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$, unless otherwise noted)

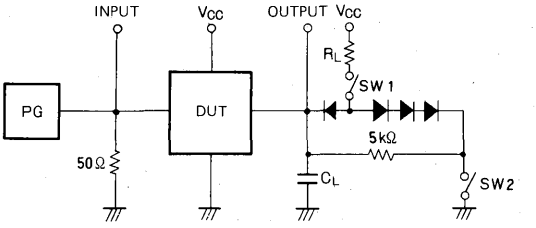
Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
fmax	Maximum clock frequency	$C_L=15pF$ (Note 4)	25	28		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_0', Q_7'			20	33	ns
t_{PHL}				20	39	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to inputs/outputs $D_0/Q_0 \sim D_7/Q_7$	$C_L=45pF$ (Note 4)		17	25	ns
t_{PHL}				23	39	ns
t_{PZH}	Output enable time to high-level	$R_L=665\Omega$, $C_L=45pF$ (Note 4)		12	21	ns
t_{PZL}	Output enable time to low-level	$R_L=665\Omega$, $C_L=45pF$ (Note 4)		15	30	ns
t_{PHZ}	Output disable time from high-level	$R_L=665\Omega$, $C_L=5pF$ (Note 4)		12	15	ns
t_{PLZ}	Output disable time from low-level	$R_L=665\Omega$, $C_L=5pF$ (Note 4)		12	15	ns

TIMING REQUIREMENTS ($V_{CC}=5V$, $Ta=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
$t_{w(TH)}$	Clock input T high pulse width		30	13		ns
$t_{w(TL)}$	Clock input T low pulse width		30	17		ns
$t_{su(M/C)}$	Setup time M/C_1, M/C_2 to T		35	18		ns
$t_{su(D)}$	Setup time D_{SR}, D_{SL}, $D_0/Q_0 \sim D_7/Q_7$ to T		20	10		ns
$t_{su(\overline{R})}$	Setup time $\overline{R}$ to T		30	23		ns
$t_{h(M/C)}$	Hold time M/C_1, M/C_2 to T		10	−12		ns
$t_{h(D)}$	Hold time D_{SR}, D_{SL}, $D_0/Q_0 \sim D_7/Q_7$ to T		0	−5		ns
$t_{h(\overline{R})}$	Recovery time $\overline{R}$ to T		0	−8		ns

Note 4: Measurement circuit

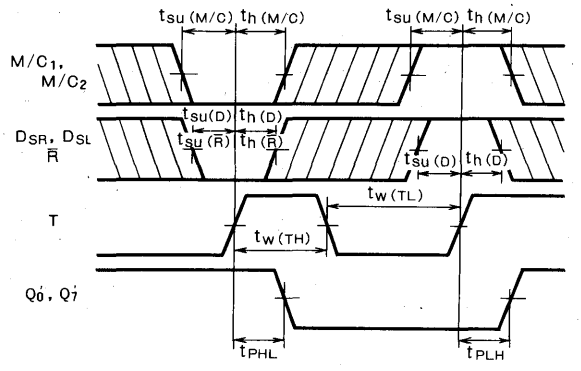


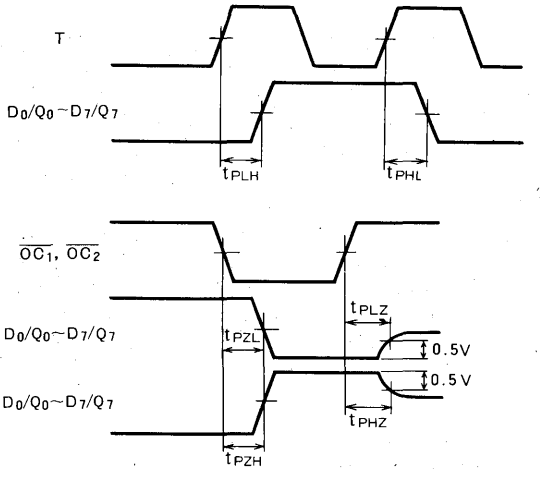


Symbol	SW 1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)

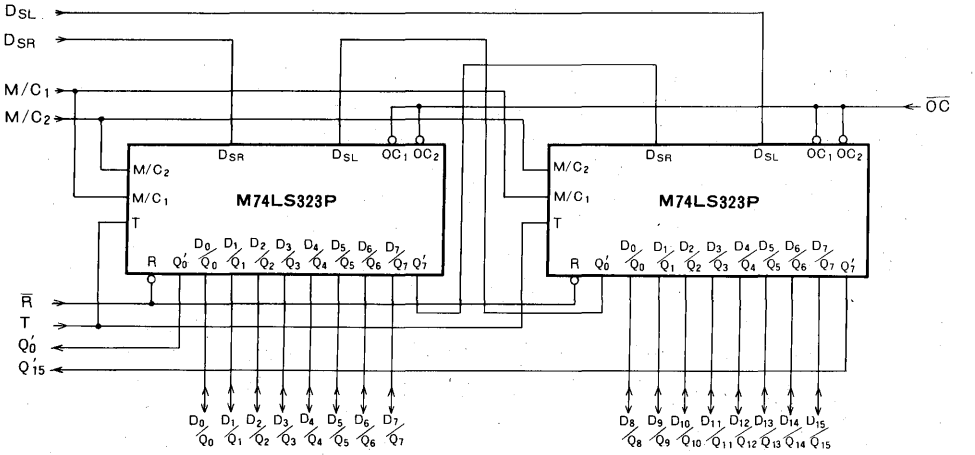




Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION EXAMPLE

The figure below shows the configuration of a 16-bit shift register using two M74LS323P devices. Similarly, an 8n-bit shift register can be configured with n ICs.



M74LS352P

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE (INVERTED)

DESCRIPTION

The M74LS352P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits.

FEATURES

- Inverted outputs provided
- Strobe inputs provided independently for each circuit
- Selection inputs common to both circuits
- Low output impedance
- Wide operating temperature range (T_a=−20~+75°C)

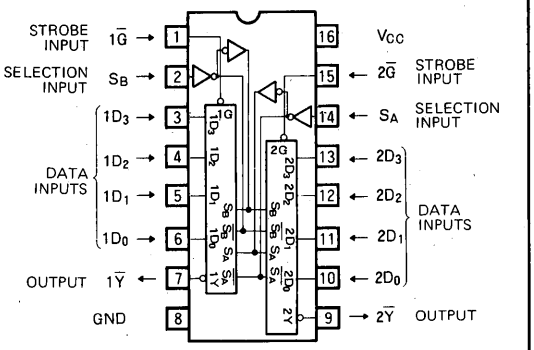
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has two data selector circuits which provide 1-line selection of 4 input signals and two multiplexer circuits which convert the 4-bit parallel data into serial data with time-sharing. When 4-line signals are applied to the data inputs D_0, D_1, D_2 and D_3 and 1 data is specified from among the data by selection inputs S_A and S_B, the input signal is output at $\overline{Y}$. By applying 4-bit parallel data to D_0, D_1, D_2 and D_3, and connecting a synchronous divide-by-4 counter output to S_A and S_B, the D_0, D_1, D_2 and D_3 data appear in the order of D_0, D_1, D_2 and D_3 synchronized with the clock pulse. S_A and S_B are common to both circuits while strobe inputs $1\overline{G}$ and $2\overline{G}$ are independent. When $1\overline{G}$ and $2\overline{G}$ are set high, $1\overline{Y}$ and $2\overline{Y}$ are set high irrespective of the status of the input.

PIN CONFIGURATION (TOP VIEW)



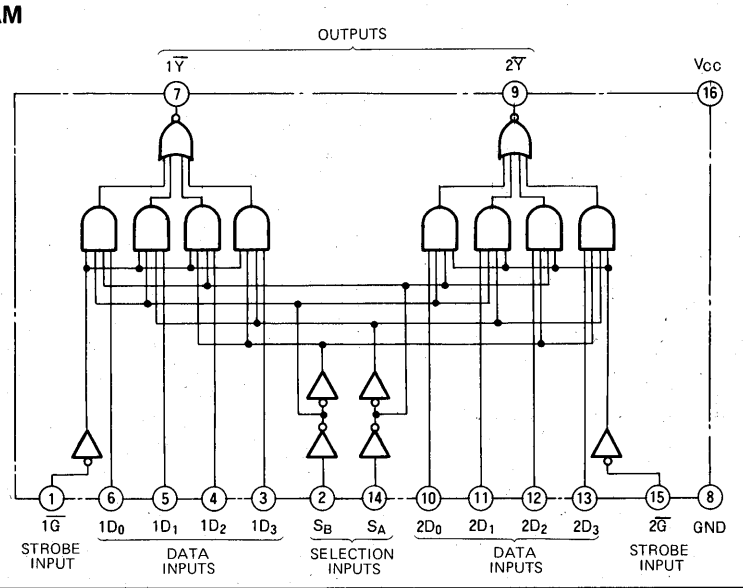
Outline 16P4

FUNCTION TABLE (Note 1)

S_B	S_A	D_0	D_1	D_2	D_3	$\overline{G}$	$\overline{Y}$
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Note 1 X : Irrelevant

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

M74LS352P

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH STROBE (INVERTED)

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

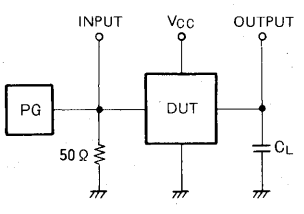
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V V_I= 2 V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}= 4 mA		0.25	0.4	V
		V_I=0.8V, V_I= 2 V	I_{OL}= 8 mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC}=5.25V, V_O= 0 V		−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 3)			6.2	10	mA

* : All typical values are at V_{CC}=5V, T_a=25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.
Note 3: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}= 5 V, Ta = 25°C, unless otherwise noted)

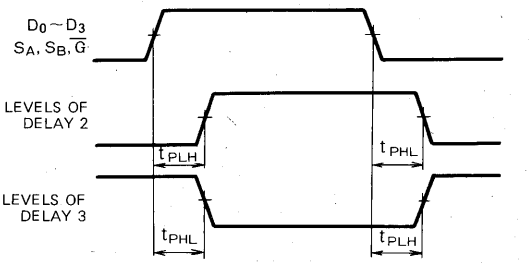
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_0 ~ D_3 to output	C_L= 15pF (Note 4)		7	20	ns
t_{PHL}				7	26	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs S_A, S_B to output $\overline{Y}$			9	29	ns
t_{PHL}				14	38	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{G}$ to output $\overline{Y}$			8	24	ns
t_{PHL}				13	32	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



M74LS353P

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS353P is a semiconductor integrated circuit containing two 4-line to 1-line data selector/multiplexer circuits and 3-state outputs.

FEATURES

- Inverted outputs provided
- Output control inputs separate for each circuit
- Selection inputs common to both circuits
- 3-state outputs
- Wide operating temperature range (T_a=−20~+75°C)

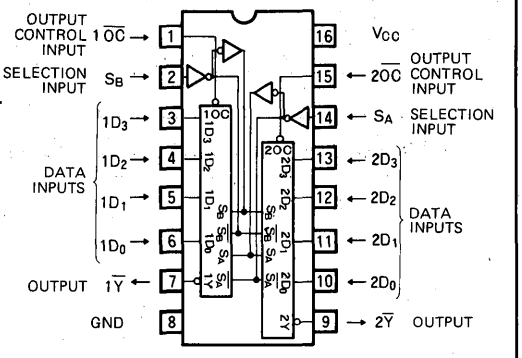
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This IC has two data selector circuits which provide 1-line selection of 4 input signals two multiplexer circuits which convert the 4-bit parallel data into serial data by time-sharing. When 4-line signals are applied to the data inputs D_0, D_1, D_2 and D_3, and 1 data is specified from among the data input by selection inputs S_A and S_B, the input signal is output at $\overline{Y}$. By applying 4-bit parallel data to data inputs D_0, D_1, D_2 and D_3 and by connecting the output of a synchronous divide-by-four counter to S_A and S_B, data D_0, D_1, D_2 and D_3 appear in the order of D_0, D_1, D_2 and D_3, synchronized with the clock pulse. S_A and S_B are common to both circuits while output control inputs $1\overline{OC}$ and $2\overline{OC}$ are separate. When $1\overline{OC}$ and $2\overline{OC}$ are set high, $1\overline{Y}$ and $2\overline{Y}$ are put in the high-impedance state ("Z") irrespective of the status of the inputs.

PIN CONFIGURATION (TOP VIEW)



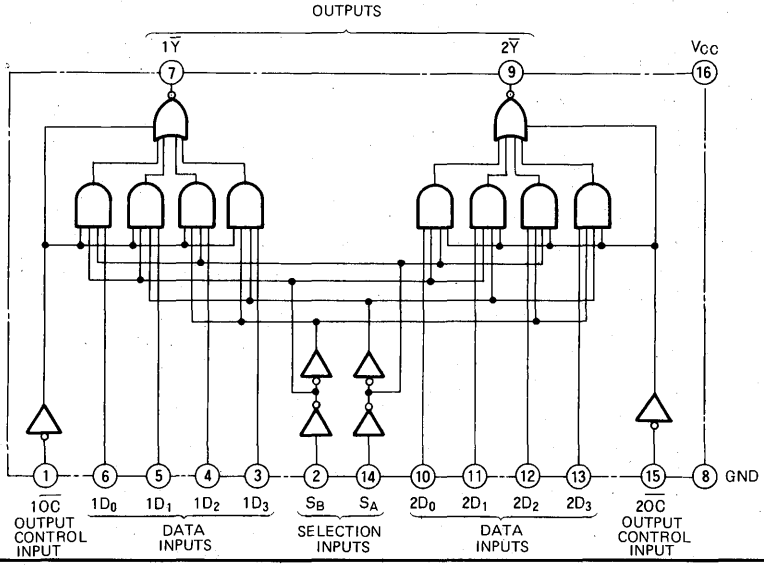
Outline 16P4

FUNCTION TABLE (Note 1)

S_B	S_A	D_0	D_1	D_2	D_3	$\overline{OC}$	$\overline{Y}$
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Note 1 X : Irrelevant
Z : High-impedance state

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−2.6mA		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
		V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current	V_{CC}=5.25V, V_I=2V, V_O=2.7V				20	μA
I_{OZL}	Off-state low-level output current	V_{CC}=5.25V, V_I=2V, V_O=0.4V				−20	μA
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC}=5.25V, V_O=0V		−30		−130	mA
I_{CCL}	Supply current, all inputs low	V_{CC}=5.25V (Note 3)			7	12	mA
I_{CCZ}	Supply current, all outputs off	V_{CC}=5.25V (Note 4)			8.5	14	mA

* : All typical values are at V_{CC}=5V, Ta=25℃

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CCL} is measured with all inputs at 0V.

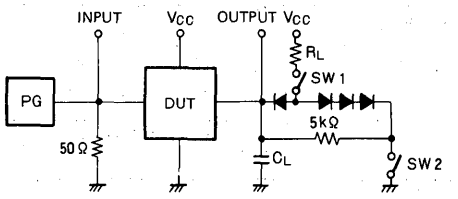
Note 4: I_{CCZ} is measured with $1\overline{OC}$ and $2\overline{OC}$ at 4.5V and all other inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs $D_0 \sim D_3$ to output $\overline{Y}$	C_L=15pF (Note 5)		9	25	ns
t_{PHL}				6	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs S_A, S_B to output $\overline{Y}$			14	45	ns
t_{PHL}				14	32	ns
t_{PZH}	Output enable time to high-level	R_L=2kΩ, C_L=15pF (Note 5)		14	23	ns
t_{PZL}	Output enable time to low-level	R_L=2kΩ, C_L=15pF (Note 5)		15	23	ns
t_{PHZ}	Output disable time from high-level	R_L=2kΩ, C_L=5pF (Note 5)		14	41	ns
t_{PLZ}	Output disable time from low-level	R_L=2kΩ, C_L=5pF (Note 5)		9	27	ns

DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER WITH 3-STATE OUTPUT (INVERTED)

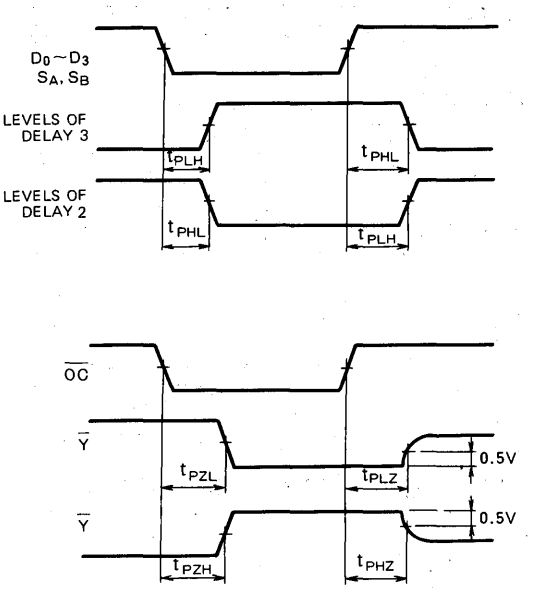
Note 5: Measurement circuit



Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR=1MHz, t_r=6ns, t_f=6ns, t_w=500ns, V_P=3V_{P-P}, Z_O = 50Ω.
(2) All diodes are switching diodes.
(3) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



MITSUBISHI ELECTRIC

M74LS365AP

HEX BUS DRIVER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS365AP is a semiconductor integrated circuit containing 6 buffers with 3-state outputs and is provided with output control inputs $\overline{OC_1}$ and $\overline{OC_2}$, which are common to six circuits.

FEATURES

- Provided with output control inputs common to 6 circuits
- High fan-out (I_{OL} = 24mA, I_{OH} = −2.6mA)
- High breakdown input voltage ($V_I \geqq 15V$)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

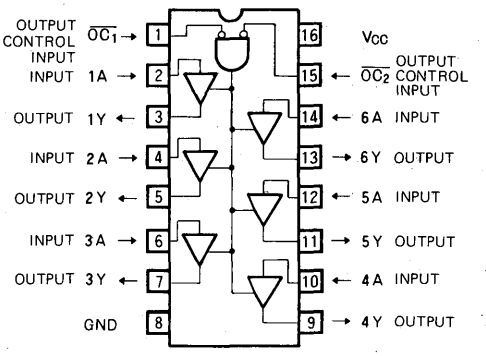
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When $\overline{OC_1}$ and $\overline{OC_2}$ are both low, high appears at the output Y if input A is high and low appears if A is low.

When either $\overline{OC_1}$ or $\overline{OC_2}$ or both are high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

PIN CONFIGURATION (TOP VIEW)



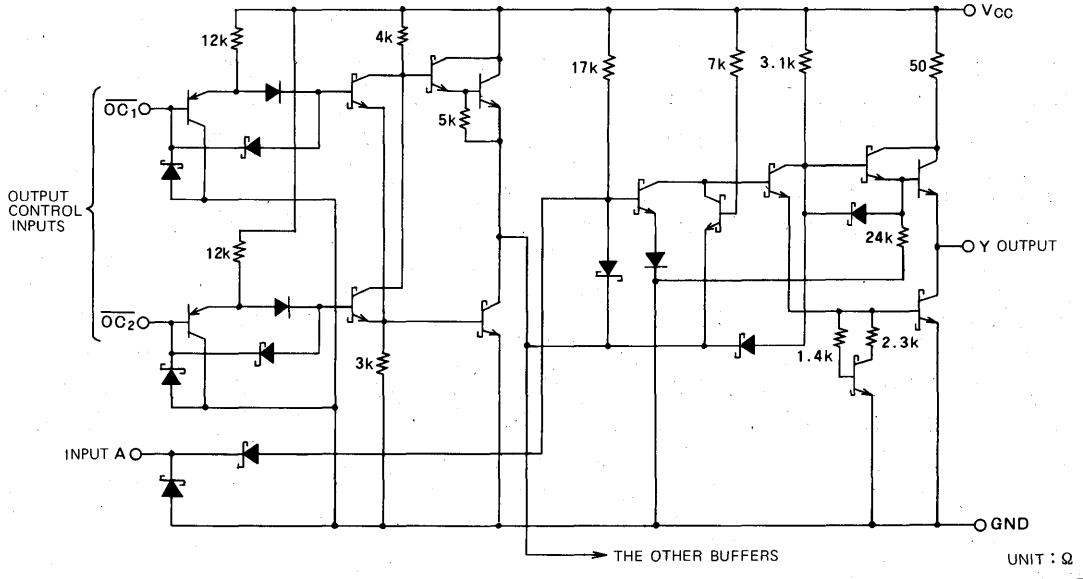
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{OC_1}$	$\overline{OC_2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Note 1: X : irrelevant
Z : high-impedance

CIRCUIT SCHEMATIC (EACH BUFFER)



HEX BUS DRIVER WITH 3-STATE OUTPUT

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-2.6mA$		2.4	3.1		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$	$I_{OL}=12mA$		0.25	0.4	V
			$V_I=0.8V$	$I_{OL}=24mA$		0.35	0.5	V
I_{OZH}	Off-state high-level output current		$V_{CC}=5.25V$, $V_I(\overline{OC})=2V$, $V_O=2.4V$				20	μA
I_{OZL}	Off-state low-level output current		$V_{CC}=5.25V$, $V_I(\overline{OC})=2V$, $V_O=0.4V$				−20	μA
I_{IH}	High-level input current		$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
			$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$\overline{OC}$	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		A	$V_{CC}=5.25V$	$V_I(\overline{OC})=0.4V$ $V_I=0.4V$			−0.4	mA
				$V_I(\overline{OC})=2V$ $V_I=0.5V$			−20	μA
I_{OS}	Short circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−40		−225	mA
I_{CC}	Supply current		$V_{CC}=5.25V$, $V_I=0V$, $V_I(\overline{OC})=4.5V$			14	24	mA

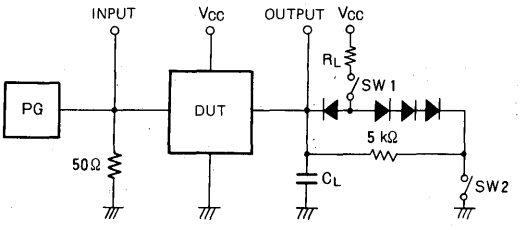
* : All values are at $V_{CC}=5V$, $T_a=25°C$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input A to output Y	$C_L=45pF$ (Note 3)		7	16	ns
t_{PHL}				10	22	ns
t_{PZH}	Output enable time to high-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		13	35	ns
t_{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		15	40	ns
t_{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		13	30	ns
t_{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		16	35	ns

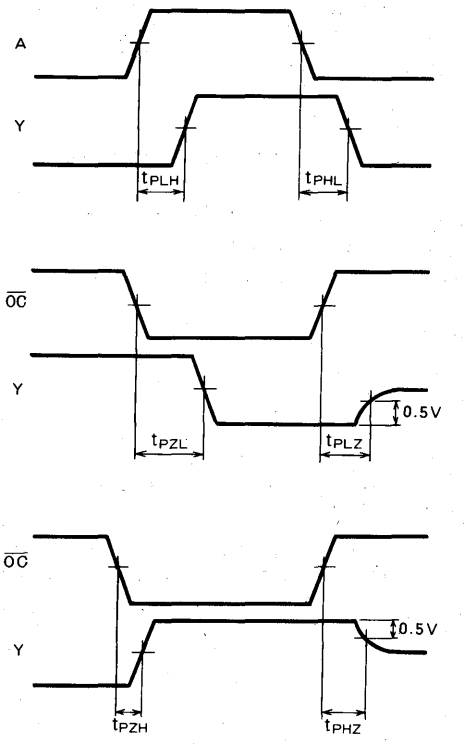
Note 3: Measurement circuit



Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance

TIMING DIAGRAM (Reference level = 1.3V)



M74LS366AP

HEX BUS DRIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS366AP is a semiconductor integrated circuit containing 6 buffers with 3-state outputs and is provided with output control inputs $\overline{OC_1}$ and $\overline{OC_2}$, which are common to six circuits.

FEATURES

- Provided with output control inputs common to 6 circuits
- High fan-out (I_{OL} = 24mA, I_{OH} = −2.6mA)
- High breakdown input voltage ($V_I \geqq 15V$)
- Wide operating temperature range (T_a = −20~+75°C)

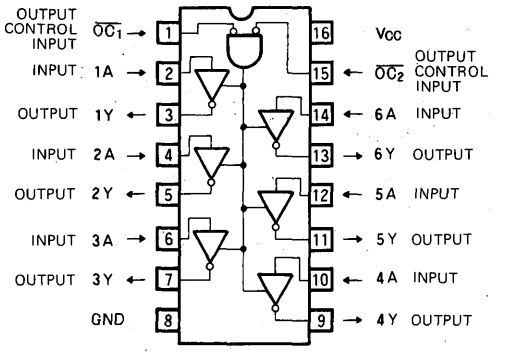
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When OC_1 and OC_2 are both low, low appears in the output Y if input A is high and high appears if A is low. When either $\overline{OC_1}$ or $\overline{OC_2}$ both are high, all outputs Y are put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

PIN CONFIGURATION (TOP VIEW)



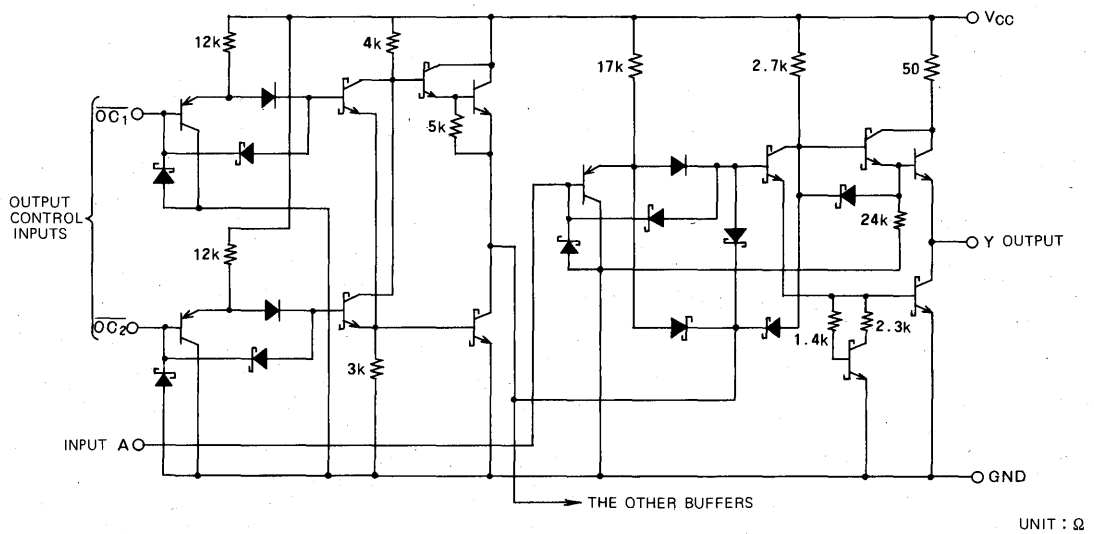
Outline 16P4

FUNCTION TABLE (Note 1)

$\overline{OC_1}$	$\overline{OC_2}$	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

Note 1: X : irrelevant
Z : high-impedance

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

MITSUBISHI ELECTRIC

HEX BUS DRIVER WITH 3-STATE OUTPUT (INVERTED)

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V, I_{OH}=−2.6mA		2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=12mA		0.25	0.4	V
			V_I=0.8V, V_I=2V	I_{OL}=24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.25V, $V_I(\overline{OC})$=2V, V_O=2.4V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.25V, $V_I(\overline{OC})$=2V, V_O=0.4V				−20	μA
I_{IH}	High-level input current		V_{CC}=5.25V, V_I=2.7V				20	μA
			V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	$\overline{OC}$	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
		A	V_{CC}=5.25V	$V_I(\overline{OC})$=0.4V, V_I=0.4V			−0.4	mA
				$V_I(\overline{OC})$=2V, V_I=0.5V			−20	μA
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−40		−225	mA
I_{CC}	Supply current		V_{CC}=5.25V, V_I=0V, $V_I(\overline{OC})$=4.5V			12	21	mA

* : All values are at V_{CC}=5V, T_a=25°C

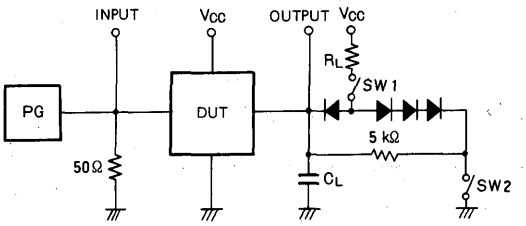
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input A to output Y	C_L=45pF (Note 3)		7	15	ns
t_{PHL}				7	18	ns
t_{PZH}	Output enable time to high-level	R_L=667Ω, C_L=45pF (Note 3)		10	35	ns
t_{PZL}	Output enable time to low-level	R_L=667Ω, C_L=45pF (Note 3)		18	45	ns
t_{PHZ}	Output disable time from high-level	R_L=667Ω, C_L= 5 pF (Note 3)		13	32	ns
t_{PLZ}	Output disable time from low-level	R_L=667Ω, C_L= 5 pF (Note 3)		14	14	ns

HEX BUS DRIVER WITH 3-STATE OUTPUT (INVERTED)

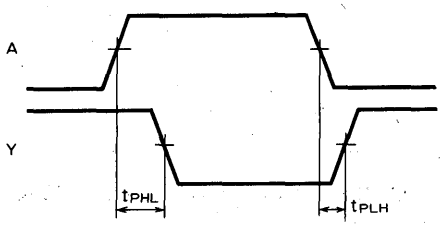
Note 3: Measurement circuit

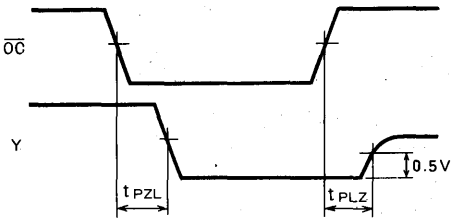


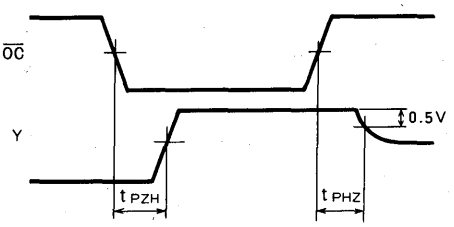
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)







M74LS367AP

HEX BUS DRIVERS WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS367AP is a semiconductor integrated circuit constaining 6 buffers with 3-state output and is provided with output control inputs $1\overline{OC}$ and $2\overline{OC}$, which are common to 4 circuits and 2 circuits, respectively.

FEATURES

- Provided with output control inputs common to 4 circuits and 2 circuits.
- High fan-out
- High breakdown input voltage
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

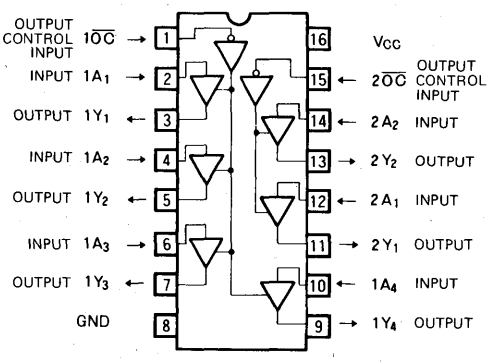
When $\overline{OC}$ is low, high appears in the output Y if input A is high, and low appears if A is low. When $\overline{OC}$ is high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

FUNCTION TABLE (Note 1)

$\overline{OC}$	A	Y
L	L	L
L	H	H
H	X	Z

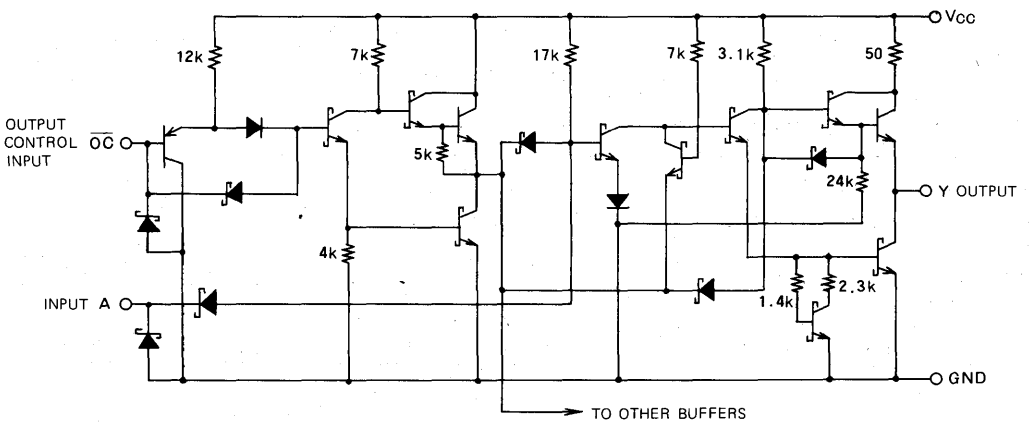
Note 1: X : irrelevant
Z : high-impedance

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

HEX BUS DRIVERS WITH 3-STATE OUTPUTS

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

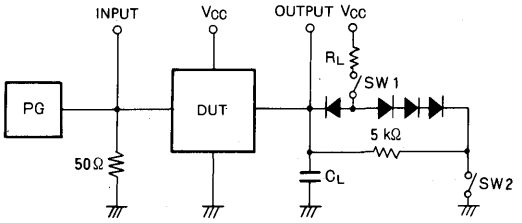
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-2.6mA$		2.4	3.1		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$ $V_I=0.8V$	$I_{OL}=12mA$ $I_{OL}=24mA$		0.25 0.35	0.4 0.5	V V
I_{OZH}	Off-state high-level output current		$V_{CC}=5.25V$, $V_I(\overline{OC})=2V$, $V_O=2.4V$				20	μA
I_{OZL}	Off-state low-level output current		$V_{CC}=5.25V$, $V_I(\overline{OC})=2V$, $V_O=0.4V$				−20	μA
I_{IH}	High-level input current		$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
			$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$\overline{OC}$	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		A	$V_{CC}=5.25V$	$V_I(\overline{OC})=0.4V$ $V_I=0.4V$			−0.4	mA
				$V_I(\overline{OC})=2V$ $V_I=0.5V$			−20	μA
I_{OS}	Short-circuit output current		$V_{CC}=5.25V$, $V_O=0V$		−40		−225	mA
I_{CC}	Supply current		$V_{CC}=5.25V$, $V_I=0V$, $V_I(\overline{OC})=4.5V$			14	24	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Lwo-to-high-level, high-to-low-level output propagation time, from input A to output Y	$C_L=45pF$ (Note 3)		7	16	ns
t_{PHL}				10	22	ns
t_{PZH}	Output enable time to high-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		13	35	ns
t_{PZL}	Output enable time to low-level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		15	40	ns
t_{PHZ}	Output disable time from high-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		13	30	ns
t_{PLZ}	Output disable time from low-level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		16	35	ns

Note 3: Measurement circuit



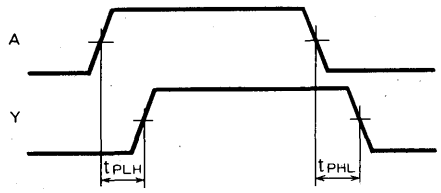
Symbol	SW 1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

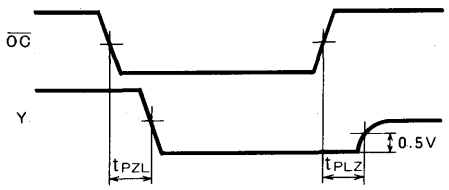
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, $V_P = 3V_{P-P}$, $Z_O = 50\Omega$

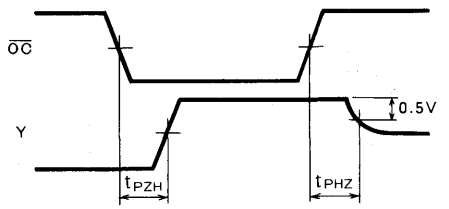
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)

(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)







M74LS368AP

HEX BUS DRIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS368AP is a semiconductor integrated circuit containing 6 buffers with 3-state outputs and is provided with output control inputs $1\overline{OC}$ and $2\overline{OC}$, which are common to 4 circuits and 2 circuits respectively.

FEATURES

- Provided with output control inputs common to 4 circuits and 2 circuits
- High fan-out (I_{OL} = 24mA, I_{OH} = −2.6mA)
- High breakdown input voltage ($V_I \geqq 15V$)
- Wide operating temperature range (T_a = −20~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

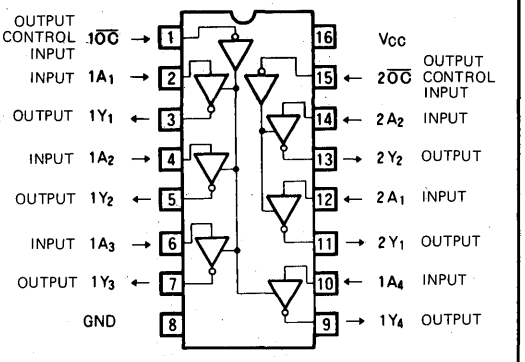
When $\overline{OC}$ is low, low appears in the output Y if input A is high and high appears if A is low. When $\overline{OC}$ is high, Y is put in the high-impedance state irrespective of the status of A. For this reason, this device is most suitable for use as a bus line driver.

FUNCTION TABLE (Note 1)

$\overline{OC}$	A	Y
L	L	H
L	H	L
H	X	Z

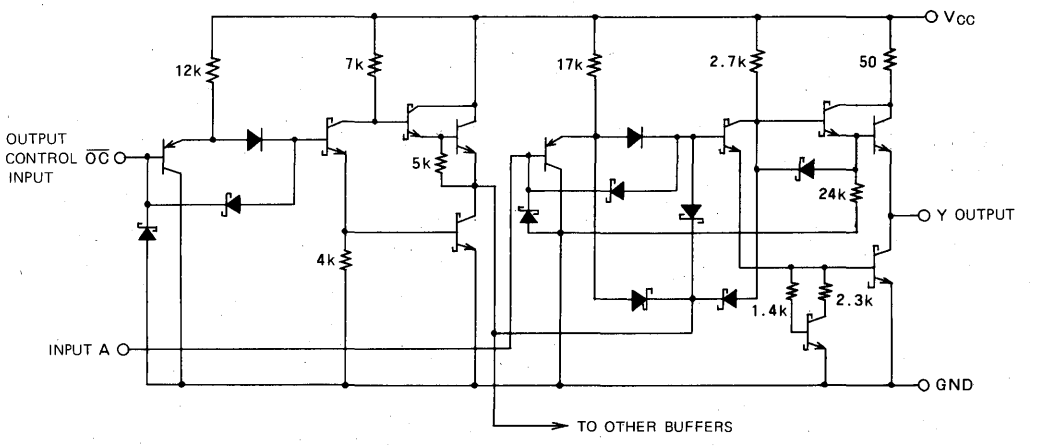
Note 1: X : irrelevant
Z : high-impedance

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

CIRCUIT SCHEMATIC (EACH BUFFER)



UNIT : Ω

MITSUBISHI ELECTRIC

HEX BUS DRIVER WITH 3-STATE OUTPUT (INVERTED)

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	°C
T_{stg}	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V, I_{OH}=−2.6mA		2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=12mA		0.25	0.4	V
			V_I=0.8V, V_I=2V	I_{OL}=24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.25V, $V_I(\overline{OC})$=2V, V_O=2.4V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.25V, $V_I(\overline{OC})$=2V, V_O=0.4V				−20	μA
I_{IH}	High-level input current		V_{CC}=5.25V, V_I=2.7V				20	μA
			V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	$\overline{OC}$	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
		A	V_{CC}=5.25V	$V_I(\overline{OC})$=0.4V, V_I=0.4V			−0.4	mA
				$V_I(\overline{OC})$=2V, V_I=0.5V			−20	μA
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−40		−225	mA
I_{CC}	Supply current		V_{CC}=5.25V, V_I=0V, $V_I(\overline{OC})$=4.5V			12	21	mA

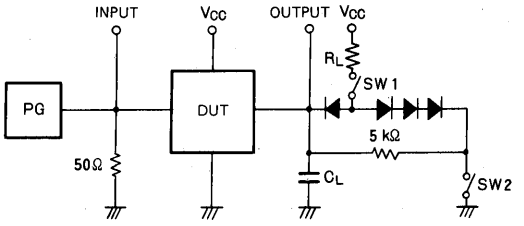
* : All values are at V_{CC}=5V, T_a=25°C, unless otherwise noted

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high level, high-to-low-level output propagation time, from input A to output Y	C_L=45pF (Note 3)		7	15	ns
t_{PHL}				7	18	ns
t_{PZH}	Output enable time to high-level	R_L=667Ω, C_L=45pF (Note 3)		16	35	ns
t_{PZL}	Output enable time to low-level	R_L=667Ω, C_L=45pF (Note 3)		18	45	ns
t_{PHZ}	Output disable time from high-level	R_L=667Ω, C_L= 5 pF (Note 3)		13	32	ns
t_{PLZ}	Output disable time from low-level	R_L=667Ω, C_L= 5 pF (Note 3)		18	35	ns

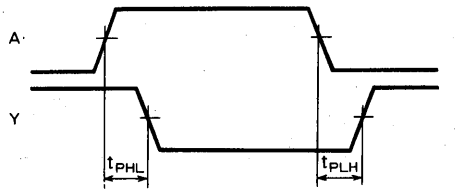
Note 3: Measurement circuit

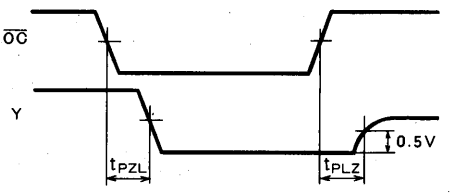


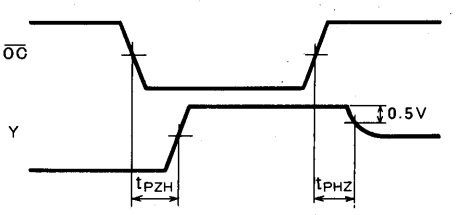
Symbol	SW 1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P\text{-}P}$, Z_O = 50Ω.
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)







M74LS373P

OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS373P is a semiconductor integrated circuit containing 8 D-type latch circuits with 3-state output and is provided with an output controlling input and an enable input common to all circuits.

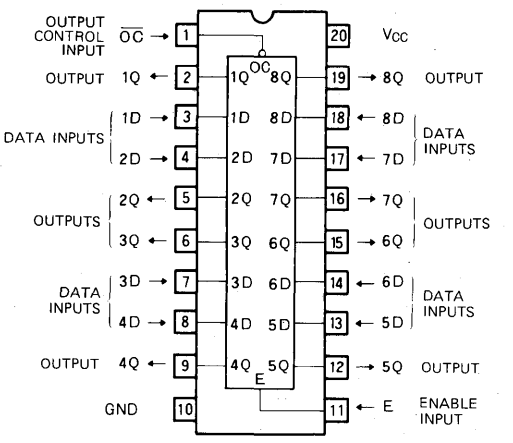
FEATURES

- 3-state, high fan-out output
- Since pnp transistor input is used in output control and enable inputs, the input load factor is small
- The enable input has high noise margin (Hysterisis = 400mV typical)
- Package density is high with 8 circuits in one package
- Provided with output control and enable inputs which are common to all 8 circuits.
- Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTIONAL DESCRIPTION

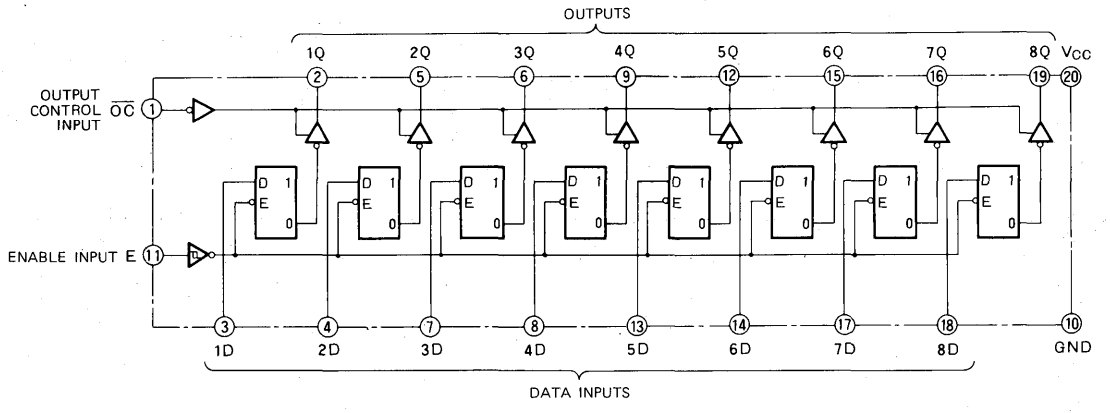
Since the 8 D-type latches use pnp transistor input for the output control input $\overline{OC}$ and enable input E, which are common to all 8 circuits, the input load factor is small. With a hysteretis of 400mV (typical) specially given to the input circuit E, noise margin is high.

When E is high, the information from the data input D appears in the output Q.

When the D signal changes, the signal that appears in Q also changes. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q does not change even if the D is changed.

When $\overline{OC}$ is high, 1Q – 8Q are all put in the high-impedance state irrespective of other input signals. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bi-directional bus driver. For application, see M74LS374P.

BLOCK DIAGRAM



OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

$\overline{OC}$	E	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q^0
H	X	X	Z

Note 1: Q^0 : level of Q before the indicated steady-state input conditions were established
Z : high-impedance
X : irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage	E					0.75	V
		D, $\overline{OC}$					0.8	
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-2.6mA$		2.4	3.1		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=12$ mA		0.25	0.4	V
				$I_{OL}=24$mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		$V_{CC}=5.25V$, $V_I=2V$, $V_O=2.7V$				20	μA
I_{OZL}	Off-state low-level output current		$V_{CC}=5.25V$, $V_I=2V$, $V_O=0.4V$				−20	μA
I_{IH}	High-level input current		$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
			$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current		$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−30		−130	mA
I_{CCZ}	Supply current, all outputs off		$V_{CC}=5.25V$ (Note 3)			24	40	mA

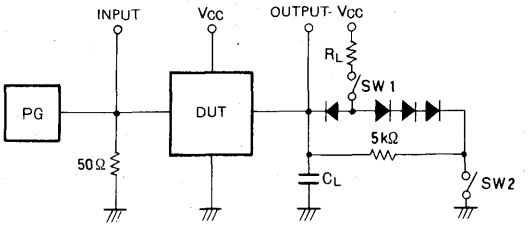
* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.
3: I_{CCZ} is measured with $\overline{OC}$ input at 4.5V.

OCTAL D-TYPE TRANSPARENT LATCHS WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input 1D~8D to output 1Q~8Q	C_L=45pF (Note 4)		9	18	ns
t_{PHL}				11	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output 1Q~8Q			14	30	ns
t_{PHL}				13	30	ns
t_{PZH}	Output enable time to high-level	R_L=667Ω, C_L=45pF (Note 4)		13	28	ns
t_{PZL}	Output enable time to low-level	R_L=667Ω, C_L=45pF (Note 4)		14	36	ns
t_{PHZ}	Output disable time from high-level	R_L=667Ω, C_L= 5pF (Note 4)		16	20	ns
t_{PLZ}	Output disable time from low-level	R_L=667Ω, C_L= 5pF (Note 4)		8	25	ns

Note 4: Measurme Measurement circuit



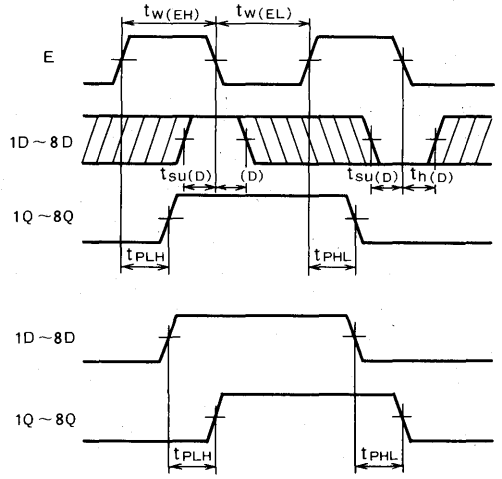
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

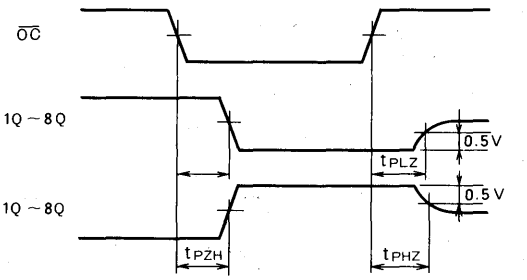
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns)
(3) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(EH)}$	Enable input E high pulse width		15	11		ns
$t_{W(EL)}$	Enable input E low pulse width		15	10		ns
t_{SU}	Setup time 1D~8D to E		5	−2		ns
t_h	Hold time 1D~8D to E		20	7		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS374P

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS WITH 3-STATE OUTPUTS

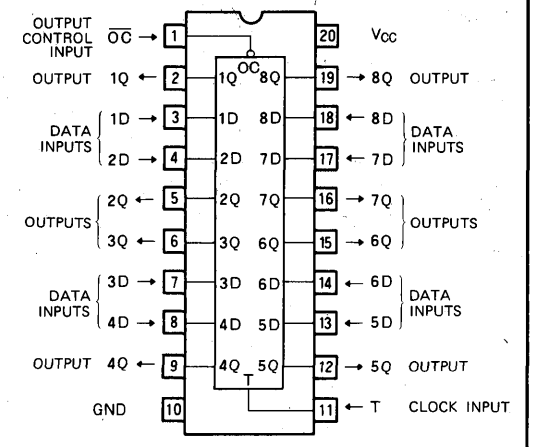
DESCRIPTION

The M74LS374P is a semiconductor integrated circuit containing 8 D-type positive edge-triggered flipflop circuits with 3-state output, and is provided with an output control input and a clock input, which are common to all the circuits.

FEATURES

- Positive edge triggering
- 3-state, high fan-out output
- The use of pnp transistor input for the output control and clock inputs has made the input load factor small
- The clock input has high noise margin. (Hysterisis = 400mV typical)
- Package density is high with 8 circuits in one package
- Provided with output control and clock inputs which are common to all 8 circuits.
- Wide operating temperature range (T_a = -20 ~ +75°C)

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

APPLICATION

General purpose, for use in industrial and consumer equipment.

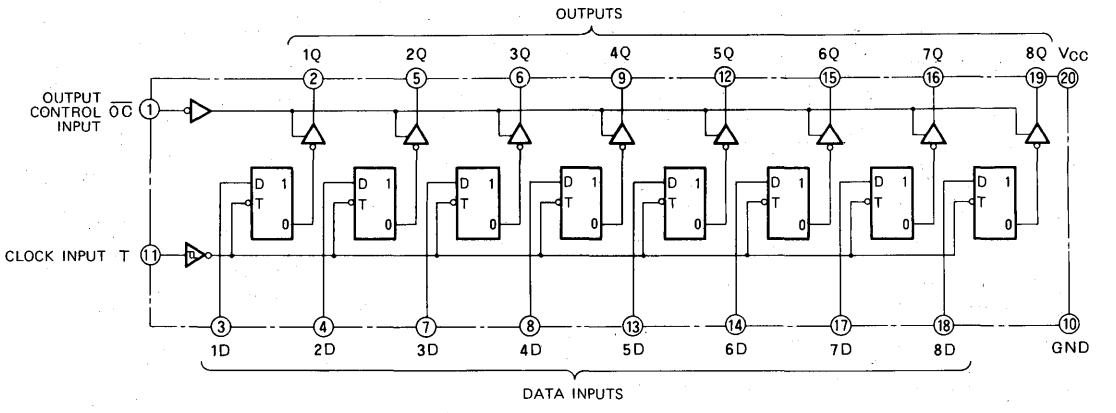
FUNCTIONAL DESCRIPTION

Since the 8 D-type ege-triggered flip-flop circuits use a pnp transistor input for the output control input $\overline{OC}$ and clock input T, which are common to all 8 circuits, the input load factor is small. With a hysterisis of 400mV (typical) specially given to the input circuit T, noise margin is high.

When T changes from low to high, the information of data input D immediately before the change appears in the output Q in accordance with the function table.

When $\overline{OC}$ is high, 1Q – 8Q are all put into the high-inpedance state, irrespective of other input signals. Since all outputs have high fan-out, this device is suitable for use as a buffer register, I/O port, or bi-directional bus driver.

BLOCK DIAGRAM



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M74LS374P

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

$\overline{OC}$	T	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q^0
H	X	X	Z

Note 1: ↑ : transition from low to high level
Q^0 : level of Q before the indicated steady-state input conditions were established
Z : high-impedance
X : irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +7	V
T_{opr}	Operating free-air ambient temperature range		−20 ~ +75	℃
T_{stg}	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−2.6	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$ $V_I=2V$, $I_{OH}=-2.6mA$		2.4	3.1		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=12mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$	$I_{OL}=24mA$		0.35	0.5	V
I_{OZH}	Off-state high-level output current	$V_{CC}=5.25V$, $V_I=2V$, $V_O=2.7V$				20	μA
I_{OZL}	Off-state low-level output current	$V_{CC}=5.25V$, $V_I=2V$, $V_O=0.4V$				−20	μA
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$		−30		−130	mA
I_{CCZ}	Supply current, all outputs off	$V_{CC}=5.25V$ (Note 3)			27	45	mA

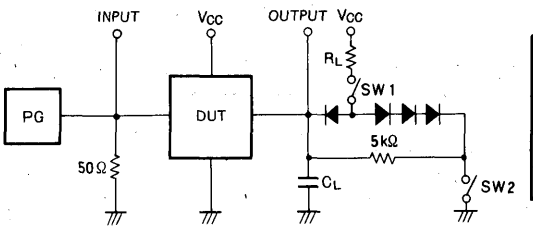
* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.
3: I_{CCZ} is measured with OC input at 4.5V.

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L=45pF (Note 4)	35	40		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output 1Q~8Q			10	28	ns
t_{PHL}				13	28	ns
t_{PZH}	Output enable time to high-level	R_L=667Ω, C_L=45pF (Note 4)		14	28	ns
t_{PZL}	Output enable time to low-level	R_L=667Ω, C_L=45pF (Note 4)		14	28	ns
t_{PHZ}	Output disable time from high-level	R_L=667Ω, C_L= 5pF (Note 4)		16	20	ns
t_{PLZ}	Output disable time from low-level	R_L=667Ω, C_L= 5pF (Note 4)		8	25	ns

Note 4: Measurement circuit



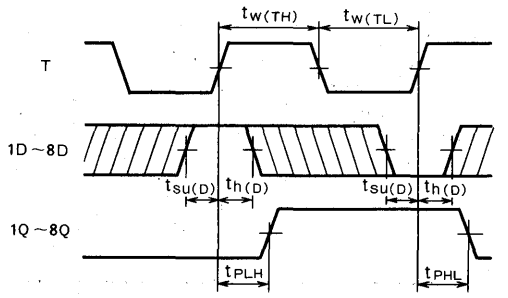
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

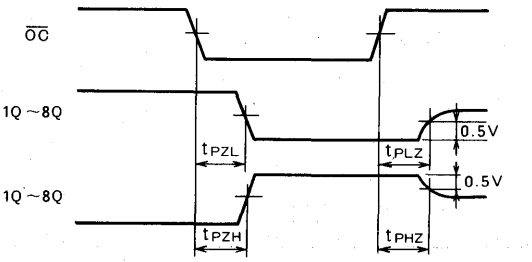
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns)
(3) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(TH)}$	Clock input T high pulse width		15	5		ns
$t_{W(TL)}$	Clock input T low pulse width		18	15		ns
$t_{SU(D)}$	Setup time 1D~8D to T		20	6		ns
$t_{h(D)}$	Hold time 1D~8D to T		4	1		ns

TIMING DIAGRAM (Reference level = 1.3V)



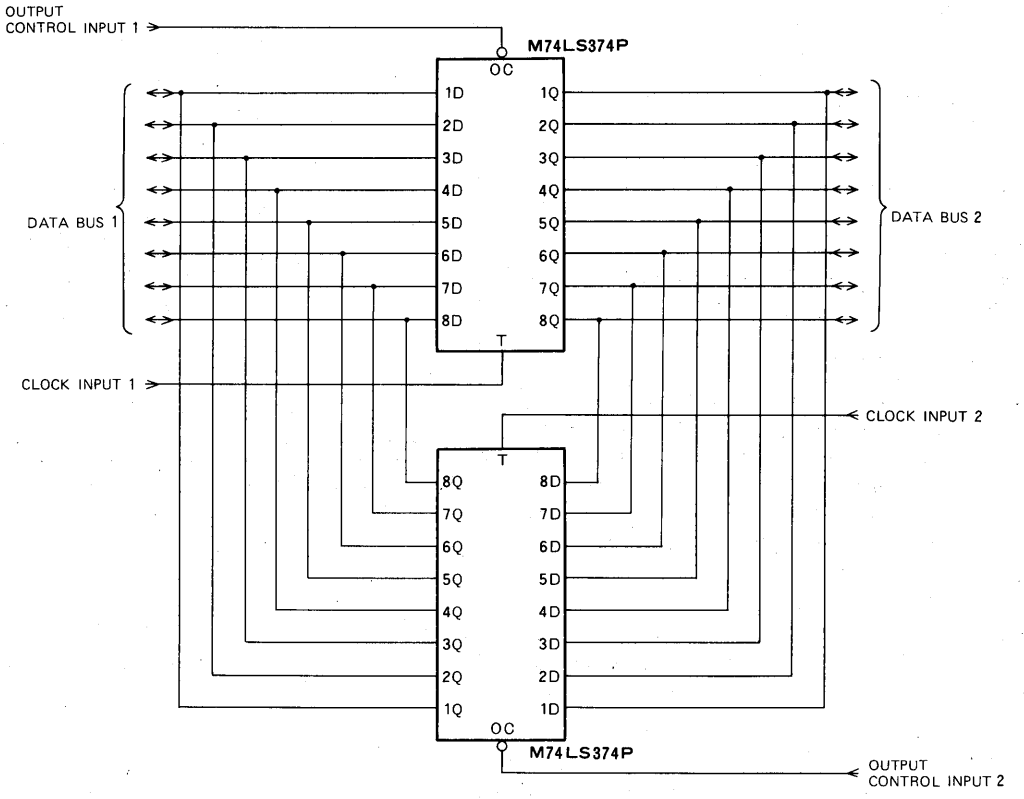


Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOPS WITH 3-STATE OUTPUTS

APPLICATION EXAMPLE

8-Bit shift register



M74LS375P

4-BIT BISTABLE LATCH

DESCRIPTION

The M74LS375P is a semiconductor integrated circuit containing 4 bistable latch circuits and is provided with outputs Q and $\overline{Q}$.

FEATURES

- Enable inputs common to two circuits each
- Q and $\overline{Q}$ outputs
- pin 8 GND, pin 16 V_{CC}
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 4 D-type latch circuits and is provided with enable inputs E common to 2 circuits each. When E is high, the information from the data input D appears in the outputs Q and $\overline{Q}$. When the D signal changes, the signal that appears in outputs Q and $\overline{Q}$ also changes. When E changes from high to low, the status of D immediately before the change is latched. While E is low, the status of Q and $\overline{Q}$ does not change even if D is changed.

This IC has the same functions and electrical characteristics as M74LS75P and differs only in its pin configuration.

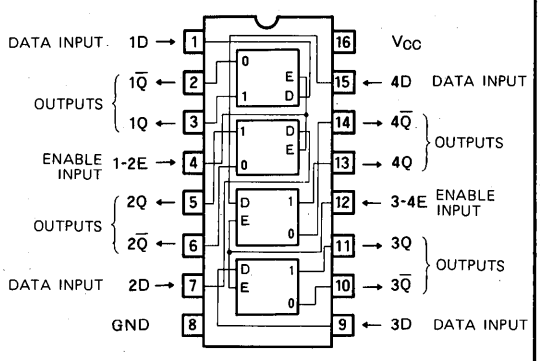
FUNCTION TABLE (Note 1)

E	D	Q	$\overline{Q}$
H	H	H	L
H	L	L	H
L	X	Q^0	$\overline{Q^0}$

Note 1 Q^0, $\overline{Q^0}$: Level of Q and $\overline{Q}$ before the indicated steady-state input conditions were established.

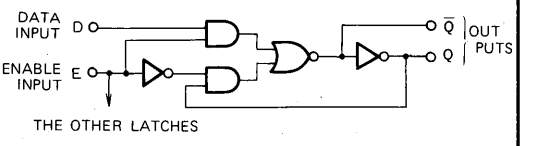
X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM (EACH LATCH)



ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	℃
Tstg	Storage temperature range		−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.5		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
			V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	D	V_{CC}=5.25V				20	μA
		E	V_I=2.7V				80	
		D	V_{CC}=5.25V				0.1	mA
		E	V_I=10V				0.4	
I_{IL}	Low-level input current	D	V_{CC}=5.25V				−0.4	mA
		E	V_I=0.4V				−1.6	
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 3)			6.3	12	mA

* : All typical values are at V_{CC}=5V, Ta=25℃

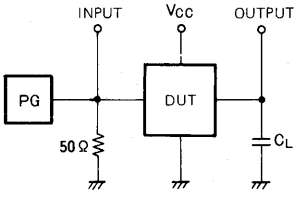
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs at 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output Q	C_L=15pF (Note 4)		12	27	ns
t_{PHL}				8	17	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D to output $\overline{Q}$			10	20	ns
t_{PHL}				6	15	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output Q			13	27	ns
t_{PHL}				12	25	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input E to output $\overline{Q}$			12	30	ns
t_{PHL}				6	15	ns

Note 4: Measurement circuit



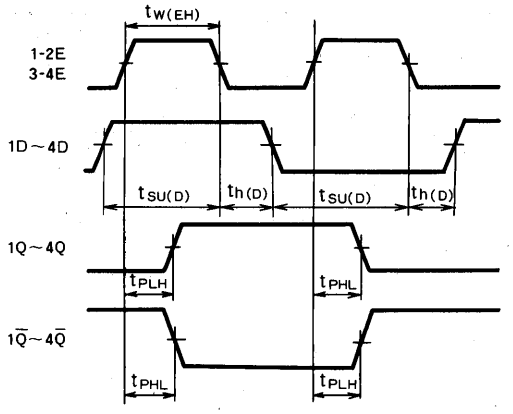
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω.

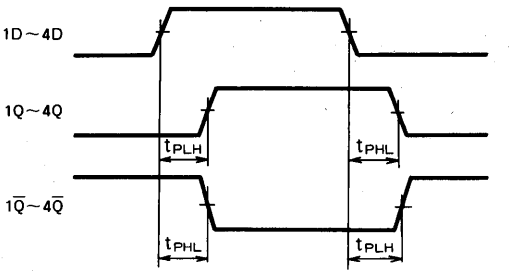
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(EH)}$	Enable input E high pulse width		20	7		ns
$t_{SU(D)}$	Setup time 1D～4D to E		20	12		ns
$t_{h(D)}$	Hold time 1D～4D to E		8	5		ns

TIMING DIAGRAM (Reference level = 1.3V)





High-level 3-4E, 1-2E

M74LS377P

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH ENABLE

DESCRIPTION

The M74LS377P is a semiconductor integrated circuit containing 8 D-type positive edge-triggered flip-flop circuits with common clock input and enable input.

FEATURES

- Positive edge-triggering
- High mounting density with 8 circuits contained
- Enable and clock inputs common to all 8 circuits
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

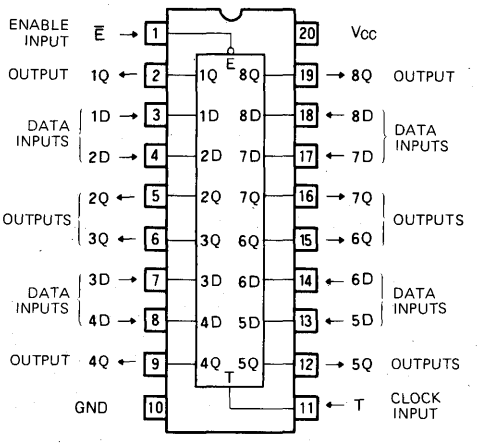
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device contains 8 edge-triggered D-type flip-flop circuits and it is provided with clock input T and enable input $\overline{E}$ common to all 8 circuits. When T changes in each flip-flop from low to high, the data input signal D immediately before the change appears in output Q.

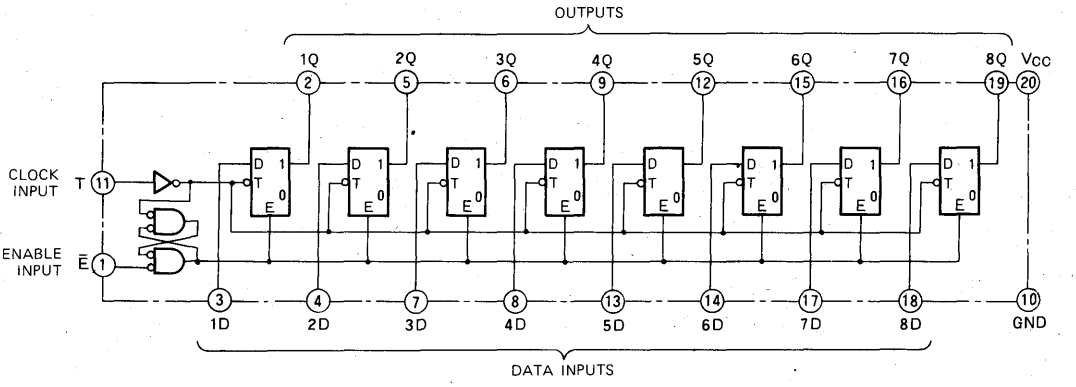
When $\overline{E}$ is set high, the output status does not change irrespective of the status of the other input signals. Malfunctioning does not result even if $\overline{E}$ is set from high to low or from low to high.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

BLOCK DIAGRAM



OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH ENABLE

FUNCTION TABLE (Note 1)

$\overline{E}$	T	D	Q
H	X	X	Q^0
L	↑	H	H
L	↑	L	L
X	L	X	Q^0

Note 1 ↑ : Transition form low to high (positive edge trigger)
Q^0 : Level of Q before the indicated steady-state input conditions were established.
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC} = 4.75V$, $I_{IC} = -18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC} = 4.75V$, $V_I = 0.8V$ $V_I = 2V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = 4.75V$	$I_{OL} = 4mA$		0.25	0.4	V
		$V_I = 0.8V, V_I = 2V$	$I_{OL} = 8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC} = 5.25V$, $V_I = 0.4V$				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC} = 5.25V$, $V_O = 0V$		−20		−100	mA
I_{CC}	Supply current	$V_{CC} = 5.25V$ (Note 3)			17	28	mA

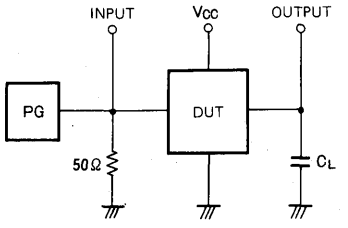
* : All typical values are at $V_{CC} = 5V$, $T_a = 25°C$
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: Supply current is measured after 1D ~ 8D are set to 0V and T has been changed from 0V to 4.5V.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	$C_L = 15pF$ (Note 4)	30	40		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from T to 1Q ~ 8Q			11	27	ns
t_{PHL}				11	27	ns

OCTAL POSITIVE EDGE-TRIGGERED D-TYPE FLIP FLOP WITH ENABLE

Note 4: Measurement circuit

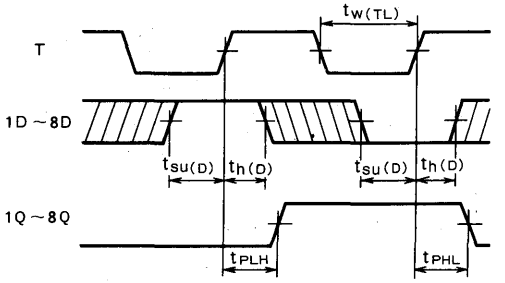


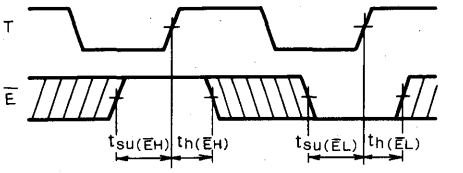
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns.
$V_P = 3V_{P-P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(TL)}$	Clock input T low pulse width		20	8		ns
$t_{SU(D)}$	Setup time 1D~8D to T		20	6		ns
$t_{SU(\overline{E}H)}$	Setup time high $\overline{E}$ to T		10	0		ns
$t_{SU(\overline{E}L)}$	Setup time low $\overline{E}$ to T		25	9		ns
$t_{h(D)}$	Hold time 1D~8D to T		5	− 5		ns
$t_{h(\overline{E}H)}$	Hold time high $\overline{E}$ to T		5	− 5		ns
$t_{h(\overline{E}L)}$	Hold time low $\overline{E}$ to T		5	1		ns

TIMING DIAGRAM (Reference level = 1.3V)





Note 5: The shaded areas indicate when the input is permitted to change for predictable output performance.

M74LS386P

QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

DESCRIPTION

The M74LS386P is a semiconductor circuit containing four integral circuits configured into dual input exclusive OR gates.

FEATURES

- Capable of withstanding high input voltages ($V_I \geqq 15V$)
- Low power dissapation (P_d = 30.5mW typical)
- High operating speed (t_{pd} = 10ns typical)
- Low output impedance
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

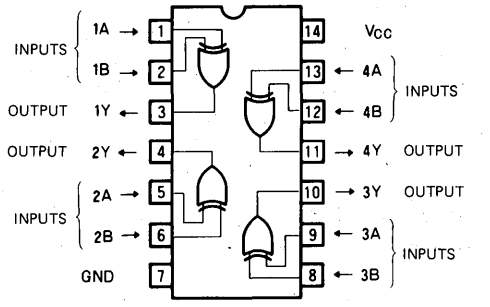
The use of Shottky TTL technology has enabled the achievement of high input voltages, high speed, low power dissipation, and high fan-out.

When both inputs A and B either low or high, output Y is low, and when A and B are high and low or low and high respectively, Y is high.

FUNCTION TABLE

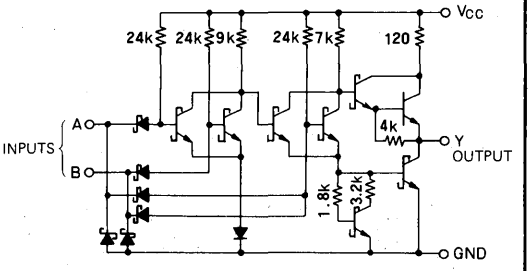
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	L

PIN CONFIGURATION (TOP VIEW)



Outline 14P4

CIRCUIT DIAGRAM (Applicable to each gate)



UNIT : Ω

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

MITSUBISHI ELECTRIC

QUADRUPLE 2-INPUT EXCLUSIVE OR GATE

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
			$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				40	μA
		$V_{CC}=5,25V$, $V_I=10V$				0.2	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.8	mA
I_{OS}	Short-circuit output current (Note 1)	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current	$V_{CC}=5.25V$ (Note 2)			6.1	10	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

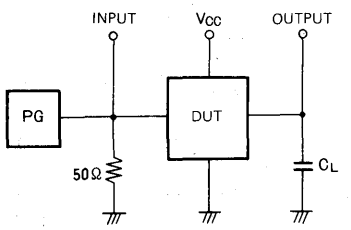
Note 1. All measurements should be done quickly, and not more than one output should be shorted at a time.

2. I_{CC} is measured with all inputs grounded.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time	$C_L=15pF$, Other inputs low (Note 3)		8	23	ns
t_{PHL}				12	17	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time	$C_L=15pF$, Other inputs high (Note 3)		8	30	ns
t_{PHL}				10	22	ns

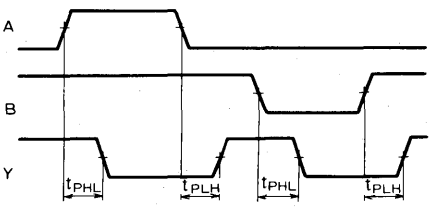
Note 3. Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.

(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS390P

DUAL DECADE COUNTER

DESCRIPTION

The M74LS390P is a semiconductor integrated circuit containing two asynchronous decade counters with direct reset inputs

FEATURES

- High mounting density with 2 circuits equivalent to LS90 and LS290
- Direct reset inputs independent for both circuits
- Usable independently as binary and divide-by-5 counters
- High-speed counting (f_{max}= 80MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

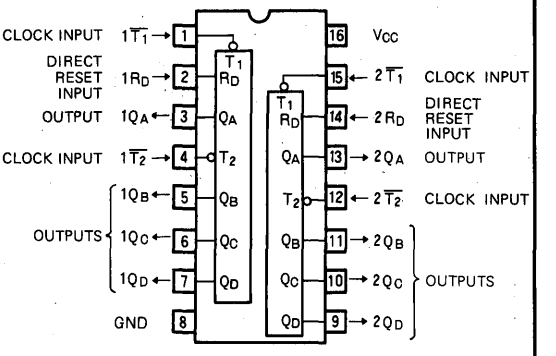
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-5 counters. Clock input $\overline{T_1}$ and output Q_A are employed for use as a binary counter while clock input $\overline{T_2}$ and outputs Q_B, Q_C and Q_D are employed for use as a divide-by-5 counter. When employed as a decade counter, the pure binary code output appears in the Q_A, Q_B, Q_C and Q_D outputs by connecting Q_A and $\overline{T_2}$ and making $\overline{T_1}$ the input. Counting is performed when $\overline{T_1}$ and $\overline{T_2}$ change from high to low.

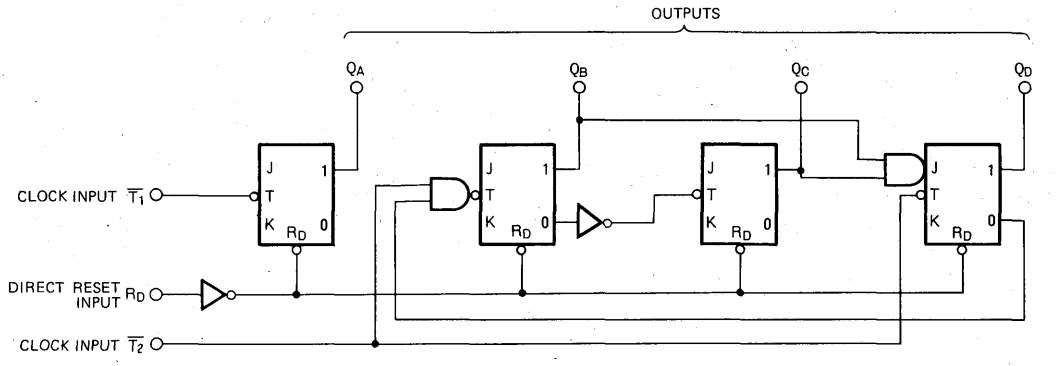
The binary and divide-by-5 counters can be reset simultaneously by setting direct reset input R_D high. For use as a counter, R_D is set low.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

DUAL DECADE COUNTER

FUNCTION TABLE (Note 1)

$\overline{T}$	R_D	Q_A	Q_B	Q_C	Q_D
X	H	L	L	L	L
↓	L	Count			

Note 1 ↓ : Transition from high to low (negative trigger)
X : Irrelevant

Count number	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Valid when Q_A and $\overline{T_2}$ are connected and $\overline{T_1}$ is made the input

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage	Inputs $\overline{T_1}$, $\overline{T_2}$	$-0.5 \sim +5.5$	V
		Input R_D	$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20 \sim +75$	°C
Tstg	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

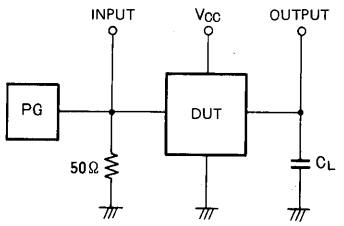
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC} = 4.75V$, $I_{IC} = -18mA$				-1.5	V
V_{OH}	High-level output voltage		$V_{CC} = 4.75V$, $V_I = 0.8V$ $V_I = 2V$, $I_{OH} = -400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC} = 4.75V$	$I_{OL} = 4mA$ (Note 2)		0.25	0.4	V
			$V_I = 0.8V$, $V_I = 2V$	$I_{OL} = 8mA$ (Note 2)		0.35	0.5	V
I_{IH}	High-level input current	R_D	$V_{CC} = 5.25V$, $V_I = 2.7V$				20	μA
		$\overline{T_1}$					100	μA
		$\overline{T_2}$					200	μA
		R_D	$V_{CC} = 5.25V$, $V_I = 10V$				0.1	mA
		$\overline{T_1}$	$V_{CC} = 5.25V$, $V_I = 5.5V$				0.2	mA
		$\overline{T_2}$					0.4	mA
I_{IL}	Low-level input current	R_D	$V_{CC} = 5.25V$, $V_I = 0.4V$				-0.4	mA
		$\overline{T_1}$					-1.6	mA
		$\overline{T_2}$					-2.4	mA
I_{OS}	Short-circuit output current (Note 3)		$V_{CC} = 5.25V$, $V_O = 0V$		-20		-100	mA
I_{CC}	Supply current		$V_{CC} = 5.25V$ (Note 4)			15	26	mA

* : All typical values are at $V_{CC} = 5V$, $Ta = 25°C$.
Note 2: Output Q_A should be tested with input $\overline{T_2}$ connected to output Q_A.
Note 3: All measurements should be done quickly not more than one output should be shorted at a time.
Note 4: I_{CC} is measured with $\overline{T_1}$ and $\overline{T_2}$ at 0V after R_D has been set from 4.5V to 0V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency, from input $\overline{T_1}$ to output Q_A	C_L=15pF (Note 5)	25	80		MHz
fmax	Maximum clock frequency, from input $\overline{T_2}$ to output Q_B		12.5	35		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_A			8	20	ns
t_{PHL}				8	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_1}$ to output Q_C			24	60	ns
t_{PHL}				24	60	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_B			10	21	ns
t_{PHL}				10	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_C			17	39	ns
t_{PHL}				17	39	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T_2}$ to output Q_D			10	21	ns
t_{PHL}				10	21	ns
t_{PHL}	High-to-low-level output propagation time, from input R_D to outputs Q_A, Q_B, Q_C, Q_D			11	39	ns

Note 5: Measurement circuit



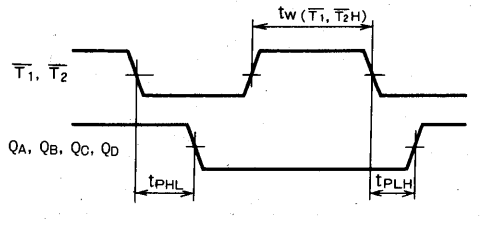
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, T_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P\text{-}P}$, Z_O = 50Ω

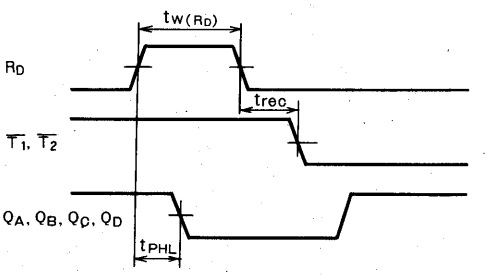
(2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{T_1}H)}$	Clock input $\overline{T_1}$ high pulse width		20	4		ns
$t_{W(\overline{T_2}H)}$	Clock input $\overline{T_2}$ high pulse width		40	12		ns
$t_{W(R_D)}$	Direct reset R_D pulse width		20	4		ns
t_r	Clock pulse rise time			400	100	ns
t_f	Clock pulse fall time			300	100	ns
$t_{rec(R_D)}$	Recovery time R_D to $\overline{T_1}$, $\overline{T_2}$		25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)





MITSUBISHI ELECTRIC

M74LS393P

DUAL 4-BIT BINARY COUNTERS

DESCRIPTION

The M74LS393P is a semiconductor integrated circuit containing two 4-bit binary (hexadecimal) asynchronous counter circuits with direct reset inputs

FEATURES

- High package density with 2 circuits equivalent to LS93 or LS293
- 2 discrete direct reset inputs
- High-speed counting (f_{max} = 75MHz typical)
- Wide operating temperature range (T_a = -20 ~ +75°C)

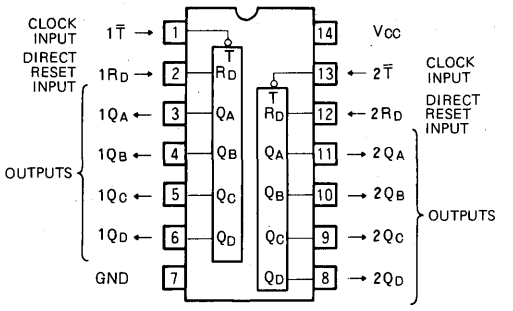
APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When a count pulse is fed to the clock input $\overline{T}$, pure binary code appear in at outputs Q_A, Q_B, Q_C, and Q_D. Counting is performed when $\overline{T}$ changes from high to low. Reset is affected by making the direct reset input R_D high. For use as a counter, hold R_D low.

PIN CONFIGURATION (TOP VIEW)



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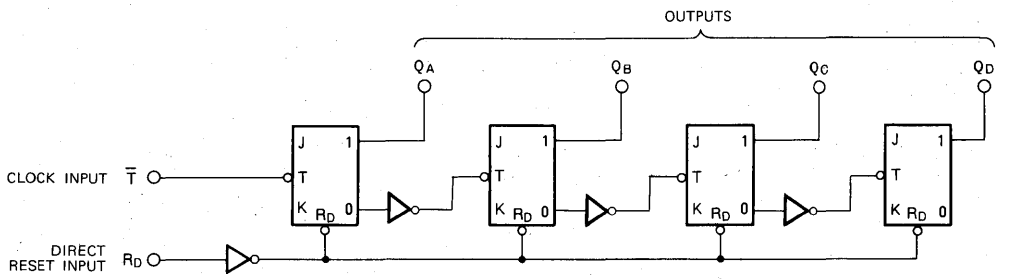
BLOCK DIAGRAM (EACH BLOCK)



DUAL 4-BIT BINARY COUNTERS

FUNCTION TABLE (Note 1)

$\overline{T}$	R_D	Q_A	Q_B	Q_C	Q_D
X	H	L	L	L	L
↓	L	Count			

Note 1: ↓ : transition from high to low-level
X : irrelevant

Count	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

ABSOLUTE MAXIMUM RATINGS
($Ta = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage	$\overline{T}$ input	$-0.5 \sim +5.5$	V
		R_D input	$-0.5 \sim +15$	
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
Topr	Operating free-air ambient temperature range		$-20 \sim +75$	°C
Tstg	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($Ta = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$, unless otherwise noted)

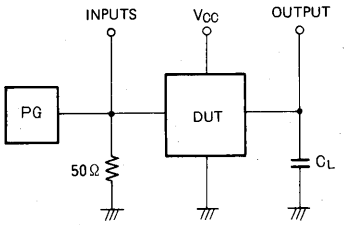
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ*	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				-1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	R_D	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{T}$					100	
		R_D	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{T}$	$V_{CC}=5.25V$, $V_I=5.5V$				0.2	mA
I_{IL}	Low-level input current	R_D	$V_{CC}=5.25V$, $V_I=0.4V$				-0.4	mA
		$\overline{T}$					-1.6	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		-20		-100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 3)			15	26	mA

* : All typical values are at $V_{CC} = 5V$, $Ta = 25°C$.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.
3: I_{CC} is measured with $\overline{T}$ input grounded and a momentary 4.5V, then grounded, applied R_D input.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L=15pF (Note 4)	25	75		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T}$ to output Q_A			8	20	ns
t_{PHL}				8	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T}$ to output Q_D			36	60	ns
t_{PHL}				36	60	ns
t_{PHL}	High-to-low-level output propagation time, from input R_D to output Q_A, Q_B, Q_C, Q_D			11	39	ns

Note 4: Measurement circuit

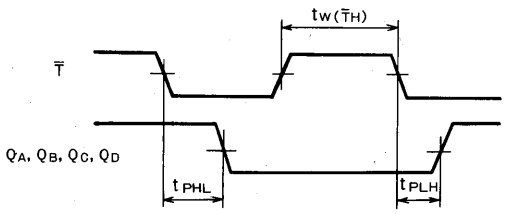


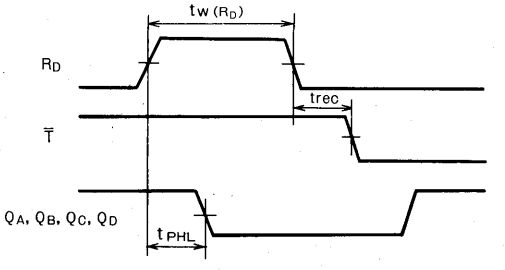
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
V_P = 3V_{P-P}, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{T}H)}$	Clock input $\overline{T}$ high pulse width		20	4		ns
$t_{W(R_D)}$	Direct reset input R_D pulse width		20	4		ns
t_r	Clock pulse rise time			400	100	ns
t_f	Clock pulse fall time			300	100	ns
$t_{rec(R_D)}$	Recovery time R_D to $\overline{T}$		25	7		ns

TIMING DIAGRAM (Reference level = 1.3V)





M74LS395AP

4-BIT CASCADABLE SHIFT REGISTER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS395AP is a semiconductor integrated circuit containing a 3-state output 4-bit serial/parallel input-serial/parallel output shift register function.

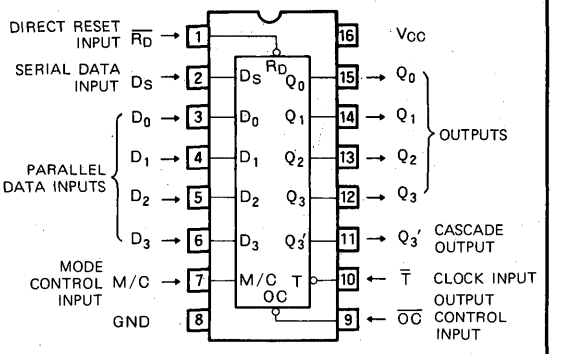
FEATURES

- Synchronous serial/parallel input-serial/parallel output
- Right shift function
- Left shift function available with external connection
- Mode control input provided
- Output control input provided
- $Q_0 \sim Q_3$ usable in AND-Tie connection (3-state output provided)
- Bit number can be expanded
- Wide operating temperature range (T_a = −20~+75°C)
- High fan-out (I_{OL} = 24mA, I_{OH} = −2.6mA)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)

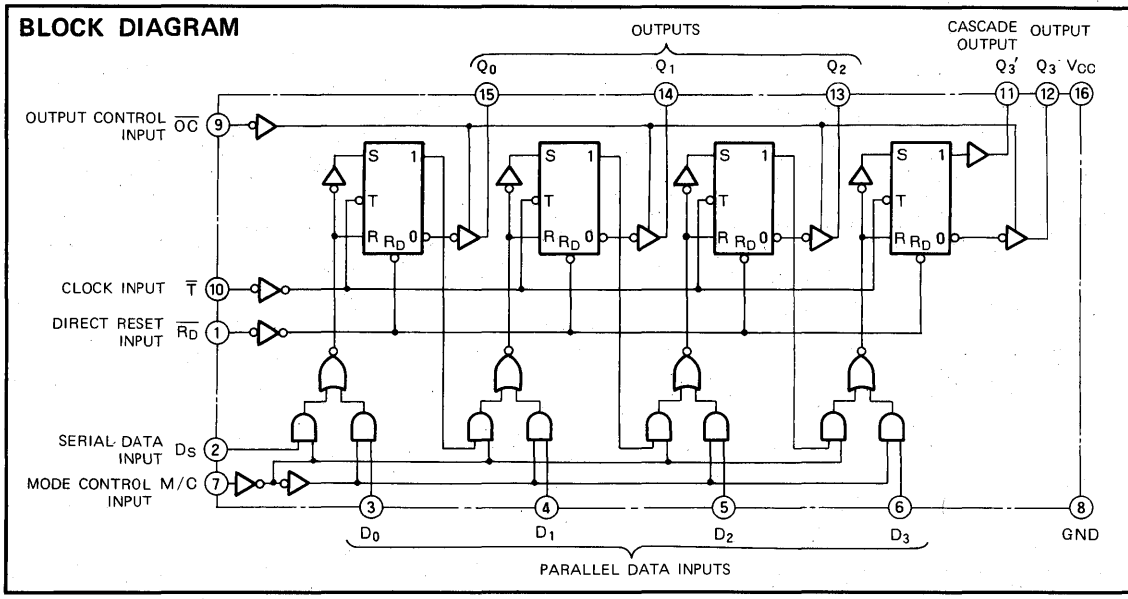


Outline 16P4

FUNCTIONAL DESCRIPTION

This device can be used as a serial input-series/parallel output and parallel input-serial/parallel output shift register with the mode control input M/C signal. When M/C is kept in low, the serial data are applied to the serial data input D_S and the clock pulse is applied to the clock input $\overline{T}$, the serial data are shifted sequentially to outputs $Q_0 \sim Q_3$ and Q_3' in synchronization with the clock pulse. When M/C is kept in high, the parallel data are applied to parallel data inputs $D_0 \sim D_3$ and the 1-bit clock pulse is applied to the $\overline{T}$, signals $D_0 \sim D_3$ appear in outputs $Q_0 \sim Q_3$ and Q_3'. When $\overline{T}$ changes from high to low, the right shift or parallel data read operation is performed. When M/C is kept in high, Q_3 is connected to D_2, Q_2 to D_1 and Q_1 to D_0, the serial data are applied to D_3, and the clock pulse is applied to $\overline{T}$, the left shift operation is performed. When a high-level state is applied to output control input $\overline{OC}$, $Q_0 \sim Q_3$ are put in a high-impedance state and AND-Tie connection is made possible. There will be no effect on the shift and parallel data reading operations even when $\overline{OC}$ is changed. Cascade output Q_3' is used for bit number expansion. Even if $\overline{OC}$ is changed in this state, there is no effect on the shifting and parallel data reading. By setting direct reset input $\overline{R_D}$ and $\overline{OC}$ low, $Q_0 \sim Q_3'$ are reset low irrespective of the status of the other input signals.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

4-BIT CASCADABLE SHIFT REGISTER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

Function mode	Input								3-state output				Cascade output
	$\overline{R_D}$	M/C	$\overline{T}$	D_S	Parallel input				Q_0	Q_1	Q_2	Q_3	Q_3'
					D_0	D_1	D_2	D_3					
Direct reset	L	X	X	X	X	X	X	X	L	L	L	L	L
Output hold	H	H	H	X	X	X	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_3^0
Parallel output	H	H	↓	X	D_0	D_1	D_2	D_3	D_0	D_1	D_2	D_3	D_3
Output hold	H	L	H	X	X	X	X	X	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_3^0
Right shift	H	L	↓	H	X	X	X	X	H	Q_0^0	Q_1^0	Q_2^0	Q_2^0
	H	L	↓	L	X	X	X	X	L	Q_0^0	Q_1^0	Q_2^0	Q_2^0

Note 1. ↓ : Transition from high to low (negative edge trigger)
Q^0 : Level of Q before the indicated steady-state input conditions were established
X : Irrelevant
Output impedance state is high when $\overline{OC}$ is high.

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage			−0.5 ~ +15	V
V_O	Output voltage	$Q_0 \sim Q_3$	Off-state	−0.5 ~ +5.5	V
		Q_3'	High-level output	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	℃
Tstg	Storage temperature range			−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage			4.75	5	5.25	V
I_{OH}	High-level output current	$Q_0 \sim Q_3$	$V_{OH} \geqq 2.4V$	0		−2.6	mA
		Q_3'	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$Q_0 \sim Q_3$	$V_{OL} \leqq 0.4V$	0		12	mA
			$V_{OL} \leqq 0.5V$	0		24	mA
		Q_3'	$V_{OL} \leqq 0.4V$	0		4	mA
			$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage	$Q_0 \sim Q_3$	V_{CC} = 4.75V, V_I = 0.8V	I_{OH} = −2.6mA	2.4	3.1		V
		Q_3'	V_I = 2V	I_{OH} = −400μA	2.7	3.4		V
V_{OL}	Low-level output voltage	$Q_0 \sim Q_3$	V_{CC} = 4.75V, V_I = 0.8V, V_I = 2V	I_{OL} = 12mA		0.25	0.4	V
				I_{OL} = 24mA		0.35	0.5	V
		Q_3'		I_{OL} = 4 mA		0.25	0.4	V
				I_{OL} = 8 mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current	$Q_0 \sim Q_3$	V_{CC} = 5.25V, V_I = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-state low-level output current	$Q_0 \sim Q_3$	V_{CC} = 5.25V, V_I = 2V, V_O = 0.4V				−20	μA
I_{IH}	High-level input current		V_{CC} = 5.25V, V_I = 2.7V				20	μA
			V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current		V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	$Q_0 \sim Q_3$	V_{CC} = 5.25V, V_O = 0 V		−30		−130	mA
		Q_3'			−20		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25V (Note 3)			21	31	mA
I_{CCZ}	Supply current, all outputs off		V_{CC} = 5.25V (Note 4)			22	34	mA

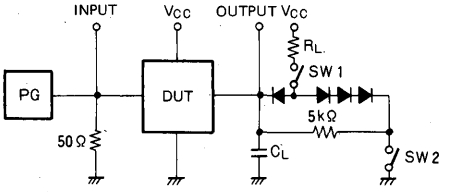
All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3: Supply current I_{CC} should be measured with $\overline{RD}$, D_S and M/C at 4.5V and $D_0 \sim D_3$, $\overline{OC}$ and $\overline{T}$ at 0V.
Note 4: I_{OCZ} is measured with $\overline{RD}$, D_S, M/C and $\overline{OC}$ at 4.5V, and $D_0 \sim D_3$ at 0V after $\overline{T}$ has been set from 3V to 0V.

4-BIT CASCADABLE SHIFT REGISTER WITH 3-STATE OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L=15pF (Note 5)	30	40		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T}$ to outputs $Q_0 \sim Q_3$, Q_3'			14	30	ns
t_{PHL}				16	30	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output $Q_0 \sim Q_3$, Q_3'			20	35	ns
t_{PZH}	Output enable time to high-level	R_L=2kΩ, C_L=15pF (Note 5)		13	25	ns
t_{PZL}	Output enable time to low-level	R_L=2kΩ, C_L=15pF (Note 5)		15	25	ns
t_{PHZ}	Output disable time from high-level	R_L=2kΩ, C_L=5pF (Note 5)		11	17	ns
t_{PLZ}	Output disable time from low-level	R_L=2kΩ, C_L=5pF (Note 5)		10	20	ns

Note 5: Measurement circuit



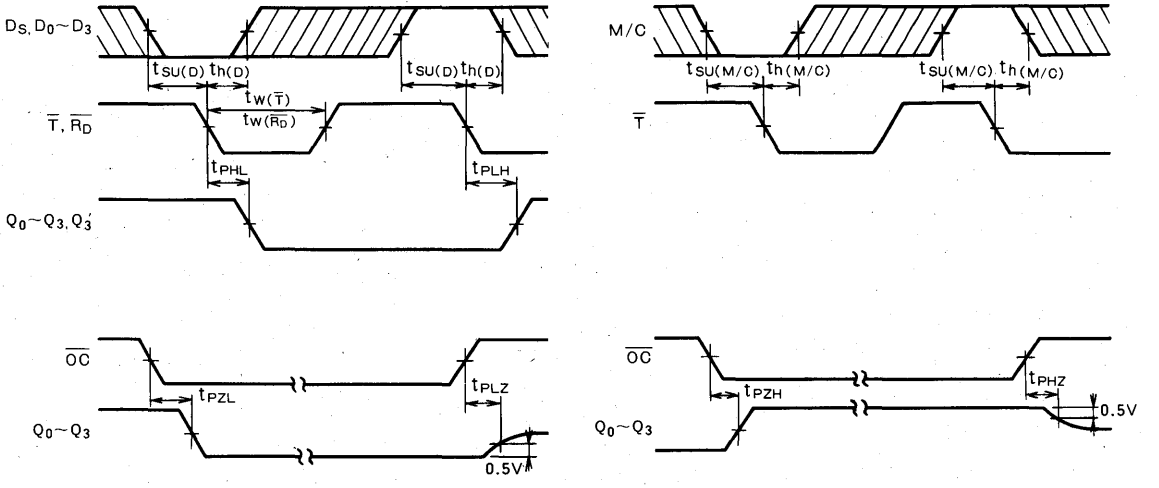
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{T})}$	Clock input $\overline{T}$ high pulse width		25	10		ns
$t_{w(\overline{R_D})}$	Direct reset $\overline{R_D}$ pulse width		20	5		ns
$t_{su(D)}$	Setup time D to $\overline{T}$		20	9		ns
$t_{su(M/C)}$	Setup time M/C to $\overline{T}$		40	16		ns
$t_{h(D)}$	Hold time D to $\overline{T}$		10	−1		ns
$t_{h(M/C)}$	M/C hold time to $\overline{T}$		10	−12		ns

TIMING DIAGRAM (Reference level = 1.3V)



Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.

NEW PRODUCT

M74LS423P

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

DESCRIPTION

The M74LS423P is a semiconductor integrated circuit containing two retriggerable monostable multivibrator circuits with direct reset inputs.

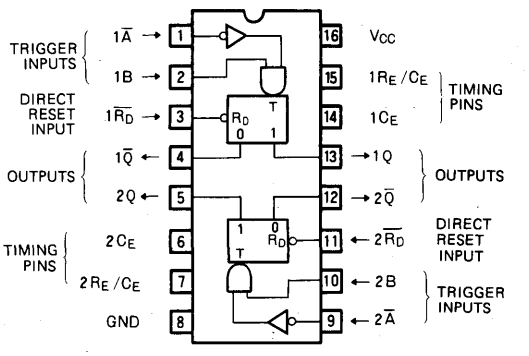
FEATURES

- Long pulse widths can be generated using the retriggerable function
- Output pulses can be stopped at any time with direct reset inputs
- $\overline{A}$, B complementary inputs provided
- Direct reset pulses with no one-shot operation.
- High input breakdown voltage ($V_I \geqq 15V$)
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (T_a=–20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

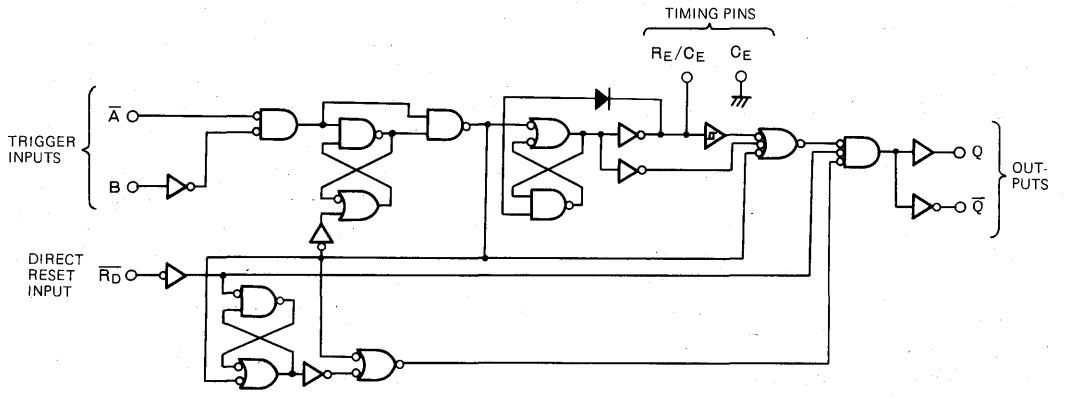
Positive pulses appear in output Q and negative pulses in output $\overline{Q}$ by connecting external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E, as shown in Fig. 1 on the next page, and by applying a trigger from input $\overline{A}$ or B. (Fig. 2(a)) The width tw of the pulses appearing in the outputs is set by R_T and C_T. When $\overline{A}$ changes from high to low or when B changes from low to high, the trigger is applied.

The retriggerable function is used to obtain long output pulse widths and when the trigger is applied from $\overline{A}$ or B immediately before the output pulse is completed, the output pulse width can be extended. (Fig. 2(b))

Q can be reset immediately low and $\overline{Q}$ high by setting direct reset input $\overline{R_D}$ low irrespective of the status of the outputs. The output pulse width can therefore be made as short as preferred by the $\overline{R_D}$ signal. (Fig. 2(c))

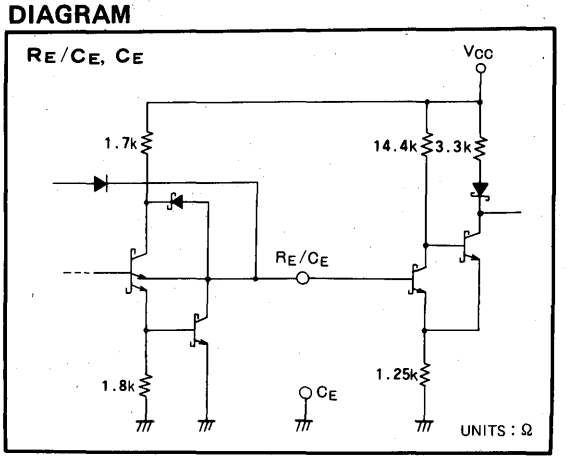
The above functions are the same as for the M74LS123P. However, when $\overline{R_D}$ changes from low to high with $\overline{A}$ at low and B at high for the M74LS123P, the trigger is applied and one-shot operation takes place, whereas with the M74LS423P one-shot operation does not take place for the same change in $\overline{R_D}$.

BLOCK DIAGRAM (EACH MONOSTABLE MULTIVIBRATOR)



DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

TIMING TERMINAL EQUIVALENT CIRCUIT DIAGRAM



FUNCTION TABLE (Note 1)

$\overline{R_D}$	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

Note 1. ↑ : Transition from low to high. (positive edge triggering)
↓ : Transition from high to low. (negative edge triggering)
⎍ : Positive one-shot operation.
⎎ : Negative one-shot operation.
X : Irrelevant

OPERATION DESCRIPTION

1. How to use the timing pins

As shown in Fig. 1, external resistor R_T and capacitor C_T are connected to timing pins R_E/C_E and C_E. Connect the positive to the R_E/C_E side and the negative to the C_E side when using C_T with polarity. In this case, it is not necessary to connect a switching diode required with the same type of TTL IC. With malfunctions caused by noise, connect C_E to the GND line (neighboring on pin 8) as shown by the dotted line in Fig. 1.

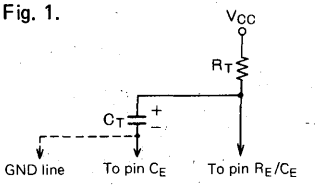


Fig. 1 Connection of external resistor R_T and capacitor C_T to timing pins R_E/C_E and C_E

2. Output pulse width t_w

The output pulse width t_w is set by R_T and C_T

2-1. When CT is greater than 1000pF

$t_w = K \cdot R_T \cdot C_T$ (ns) $\times (1 + 0.1)$

Depending on the product, fluctuations of about ±10% may arise.

Refer to K-C_T characteristics indicated in TYPICAL CHARACTERISTICS for value of K. (No change is brought to K by value of R_T.)

R_T is measured in kilohms and C_T in picofarads

Depending on the product, fluctuations in the order of 3/-10%may occur.

R_T is measured in kilohms and C_T in picofarads

2-2. When CT is equal to or less than 1000pF

Refer to the output pulse width versus–C_T, R_T given in the typical characteristics.

3. Output pulse width control

The output pulse width can be controlled in 3 ways by using, or not using, the trigger signal and $\overline{R_D}$ signal.

3-1. Normal use

This is the normal method of use as a regular monostable multivibrator such as that shown in Fig. 2(a) and the output pulse width t_w can be set as for the formula and figure in section 2 above.

3-2. Extension of output pulse width with retrigger function

As shown in Fig. 2(b), the output pulse width can be extended as desired by applying a trigger pulse before the output pulse is completed.

3-3. Shortening of the output pulse width with $\overline{R_D}$ signal

As shown in Fig. 2(c), the output pulse which has been generated by the trigger signal can be terminated with the $\overline{R_D}$ signal and it is possible to shorten its width as required.

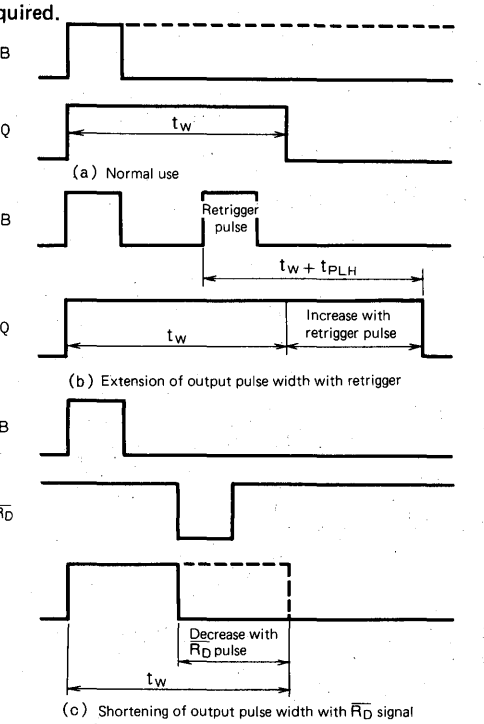


Fig. 2 Output pulse width control

MITSUBISHI ELECTRIC

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

4. Precautions with use

4-1. Apply the retrigger pulse after a wait of $0.22C_T$ (ns) upon application of the trigger pulse. C_T is measured in picofarads. The retrigger pulse during this period is ineffective.

4-2. In order to minimize the floating capacitance and to safeguard against malfunction caused by noise, make the R_T and C_T wiring as short as possible (less than 3cm) and avoid signal wires which may be conducive to noise.

4-3. Connect an external capacitor of 0.01~0.1μF with good high-frequency characteristics between pins V_{CC} and GND.

4-4. The output pulse is generated when the power is switched on.

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level stage	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA
R_T	External timing resistance		5		260	kΩ
C_T	External timing capacitance		None			
C_R	R_E/C_E pin wiring capacitance				50	pF

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}= 4 mA		0.25	0.4	V
		V_I=0.8V, V_I=2V	I_{OL}= 8 mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 3)			12	20	mA

* : All typical values are at V_{CC}=5V, T_a=25°C.

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

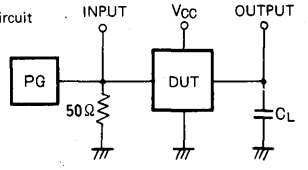
Note 3: I_{CC} is measured with R_E/C_E and C_E open, 4.5V applied to $\overline{R_D}$, $\overline{A}$ and B and $\overline{A}$ set from 0V momentarily to 4.5V.

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time, from input $\overline{A}$ to output Q	C_T = 0 pF, R_T = 5 kΩ, C_L = 15 pF (Note 4)			33	ns
t_{PLH}	Low-to-high-level output propagation time, from input B to output Q				44	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{A}$ to output $\overline{Q}$				45	ns
t_{PHL}	High-to-low-level output propagation time, from input B to output $\overline{Q}$				56	ns
t_{PHL}	High-to-low-level output propagation time, from input $\overline{R_D}$ to output Q				27	ns
t_{PLH}	Low-to-high-level output propagation time, from input $\overline{R_D}$ to output $\overline{Q}$				45	ns
$t_{WQ\,(min)}$	Minimum output pulse width, from inputs $\overline{A}$, B to output Q				200	ns
t_{WQ}	Output pulse width, from inputs $\overline{A}$, B to output Q	C_T = 1000 pF, R_T = 10 kΩ, C_L = 15 pF (Note 4)	4		5	μs

Note 4: Measurement circuit

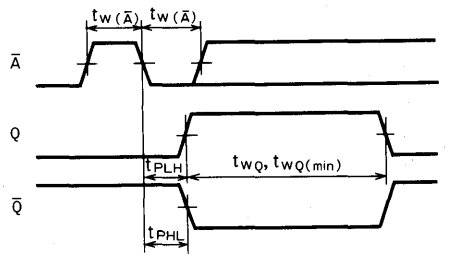


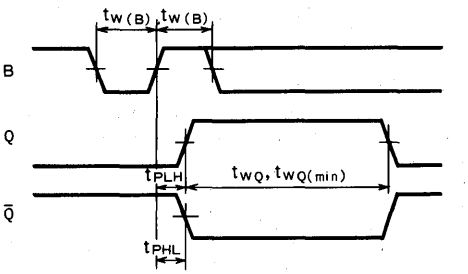
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz (100kHz with t_{WQ} measurement), t_r = 6ns, t_f = 6ns, $t_w \geqq 40$ns, $V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$.
(2) C_L includes probe and jig capacitance

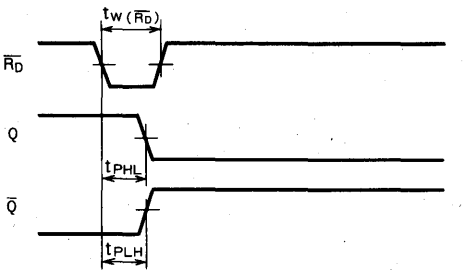
TIMING REQUIREMENTS (V_{CC} = 5 V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{A})}$	Trigger input $\overline{A}$ pulse width		40			ns
$t_{W(B)}$	Trigger input B pulse width		40			ns
$t_{W(\overline{R_D})}$	Direct reset input pulse width $\overline{R_D}$		40			ns

TIMING DIAGRAM (Reference level = 1.3V)







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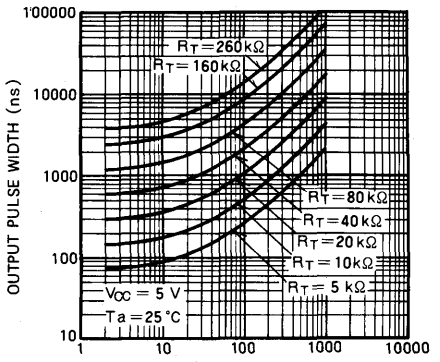
DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH RESET

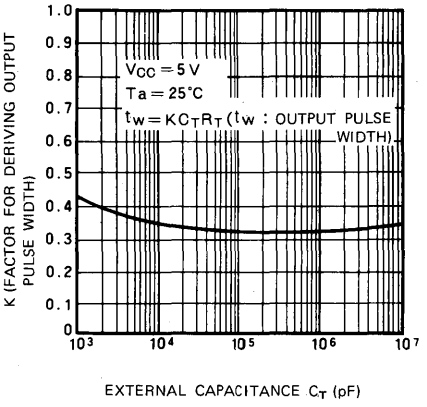
TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH VS C_T, R_T ($C_T \leqq 1000$ pF)

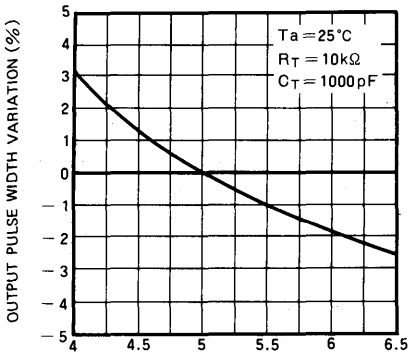


Note 5: The error of the output pulse width in the above graph is within ±20%.

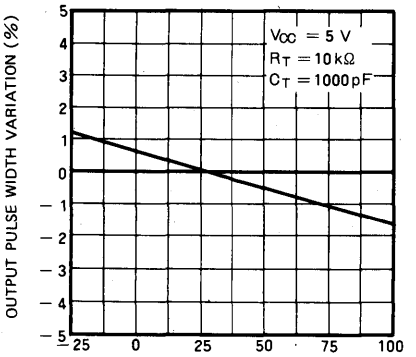
K VS C_T ($C_T > 1000$ pF)



OUTPUT PULSE WIDTH VARIATION VS SUPPLY VOLTAGE



OUTPUT PULSE WIDTH VARIATION VS AMBIENT TEMPERATURE



M74LS490P

DUAL 4-BIT DECADE COUNTER

DESCRIPTION

The M74LS490P is a semiconductor integrated circuit containing a dual circuit asynchronous decade counter with direct reset input and direct 9-set input.

FEATURES

- Two integral circuits (the functional equivalent of LS90 and LS290) provide high mounting density capability
- Individual clock, direct clear, and set-to-9 inputs for each decade counter
- High-speed counting (f_{max} = 35MHz typical)
- Wide operating temperature range (T_a = −20 ~ +75°C)

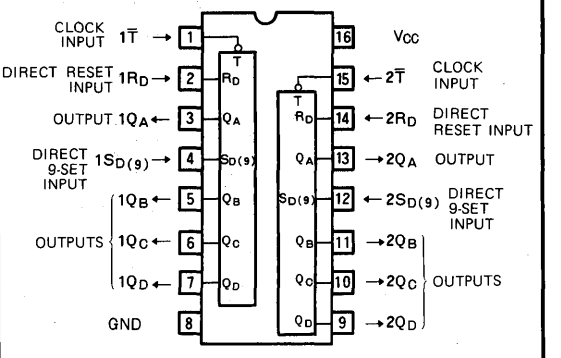
APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

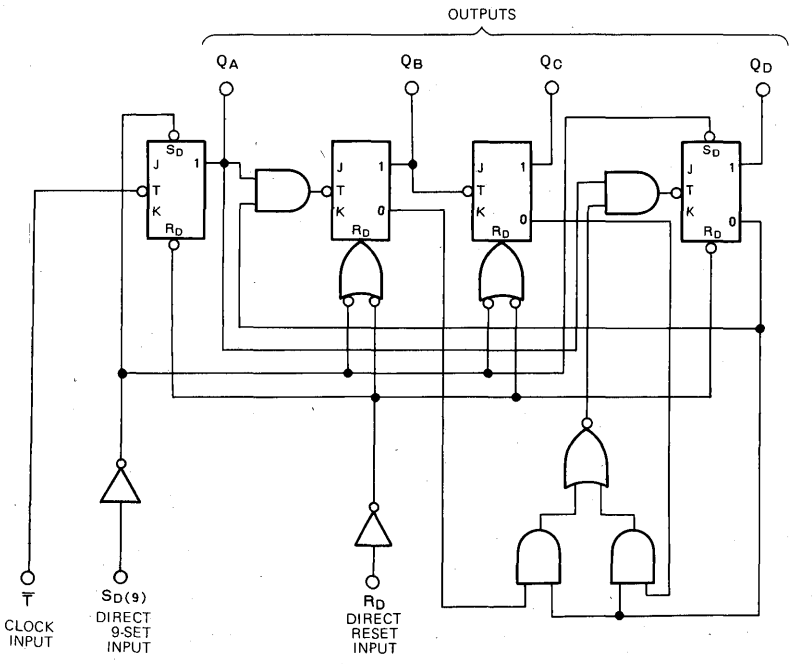
This device functions to produce binary-coded decimal output at Q_A, Q_B, Q_C, and Q_D in response to count pulse input at clock input $\overline{T}$. Counting occurs when $\overline{T}$ transits from high to low-level. A high-level status at direct reset input R_D or direct 9-set input $S_{D(9)}$ initiates reset or a setting to 9 respectively. When operated as a counter, R_D and $S_{D(9)}$ are set low-level.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

BLOCK DIAGRAM (Applicable to each circuits)



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DUAL 4-BIT DECADE COUNTER

FUNCTION TABLE (Note 1)

$\overline{T}$	R_D	$S_{D(9)}$	Q_A	Q_B	Q_C	Q_D
X	H	L	L	L	L	L
X	L	H	H	L	L	H
↓	L	L	Count			

Note 1. ↓ : Transition from high to low (negative edge trigger)
X : Irrelevant

Count	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage	INPUT $\overline{T}$	−0.5 ~ +5.5	V
		INPUT R_D, $S_{D(9)}$	−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

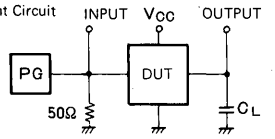
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V	I_{OL}=4mA		0.25	0.4	V
				I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	R_D, $S_{D(9)}$	V_{CC}=5.25V, V_I=2.7V				20	μA
		$\overline{T}$					100	
		R_D, $S_{D(9)}$	V_{CC}=5.25V, V_I=10V				0.1	mA
		$\overline{T}$	V_{CC}=5.25V, V_I=5.5V				0.2	
I_{IL}	Low-level input current	R_D, $S_{D(9)}$	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
		$\overline{T}$					−1.6	
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 3)			15	26	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.
3. I_{CC} is measured with all outputs open, both R_D and $S_{D(9)}$ inputs grounded following momentary connection to 4.5V; all other inputs grounded.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency (from input $\overline{T}$ to output Q_A)	C_L=15pF (Note 4)	25	35		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T}$ to output Q_A			8	20	ns
t_{PHL}				8	20	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T}$ to outputs Q_B, Q_D			20	39	ns
t_{PHL}				22	39	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{T}$ to output Q_C			30	54	ns
t_{PHL}				30	54	ns
t_{PHL}	High-to-low-level output propagation time, from input R_D to outputs Q_A, Q_B, Q_C, Q_D			11	39	ns
t_{PLH}	Low-to-high-level output propagation time, from input $S_{D(9)}$ to outputs Q_A, Q_D			11	39	ns
t_{PHL}	High-to-low-level output propagation time, from input $S_{D(9)}$ to outputs Q_B, Q_C			12	36	ns

Note 4. Measurement Circuit

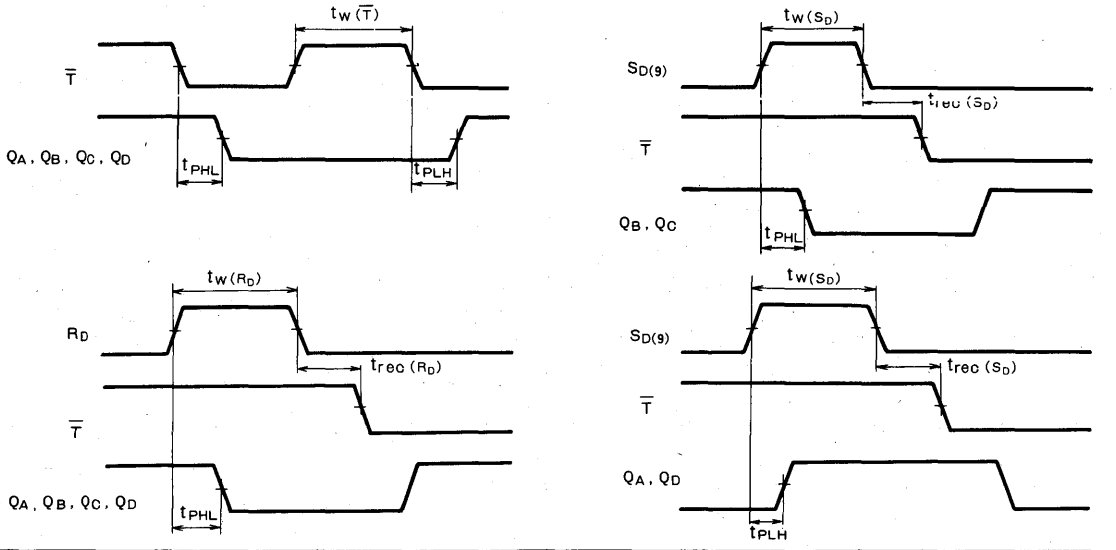


(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{T})}$	Clock input $\overline{T}$ pulse width		20	5		ns
$t_{W(R_D)}$	Direct reset R_D pulse width		20	4		ns
$t_{W(S_D)}$	Direct 9-set $S_{D(9)}$ pulse width		20	4		ns
t_r	Clock pulse rise time			400	100	ns
t_f	Clock pulse fall time			300	100	ns
$t_{rec(R_D)}$	R_D recovery time to $\overline{T}$		25	8		ns
$t_{rec(S_D)}$	$S_{D(9)}$ recovery time to $\overline{T}$		25	8		ns

TIMING DIAGRAM (Reference level = 1.3V)



MITSUBISHI ELECTRIC

M74LS540P

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS540P is a semiconductor integrated circuit containing 1 block of buffer with 3-state inverted output and common output control input for all 8 discrete circuits.

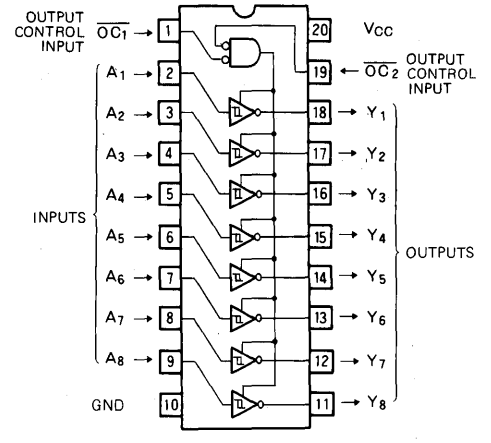
FEATURES

- Small input load factor (pnp input)
- Hysteresis provided (= 400mV typical)
- High breakdown input voltage ($V_I \geqq 5V$)
- Output control inputs provided ($\overline{OC_1}$, $\overline{OC_2}$)
- High fan-out, 3-state output (I_{OL} = 24mA, I_{OH} = −15mA)
- Data flow-thru pin out
- Wide operating temperature range. (T_a = −20~ + 75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTIONAL DESCRIPTION

The use of pnp transistors in the input circuits has enabled the achievement of small input load factor and input high break-down voltage. With hysteresis characteristics, the buffer has a 3-state inverted output with high noise margin. When output control inputs $\overline{OC_1}$ and $\overline{OC_2}$ are low, a high-level signal appears at output Y if input A is low and a low-level signal appears if it is high.

All outputs are set to the high-impedance state regardless of the status of A when $\overline{OC_1}$ and $\overline{OC_2}$ are in any other state.

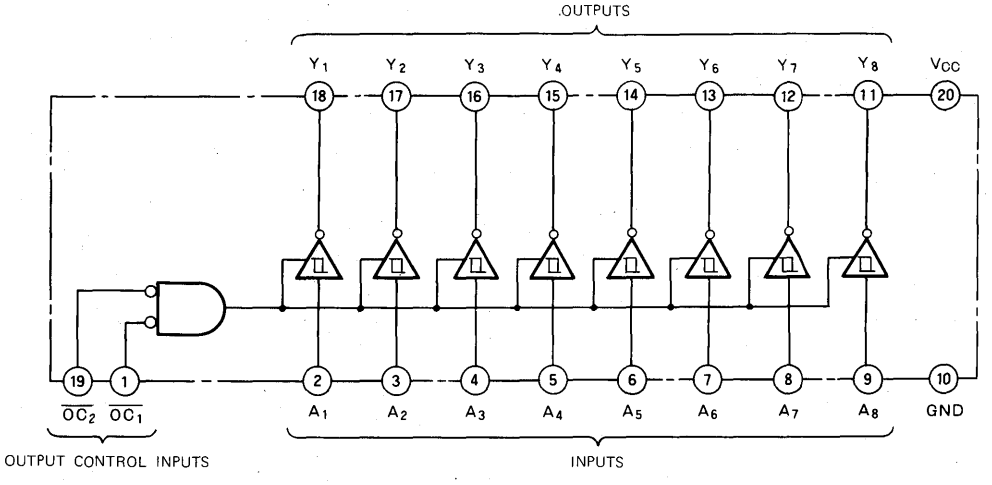
The input and output pins are arranged for facilitated board layout (data flow-thru pin out).

FUNCTION TABLE (Note 1)

A	$\overline{OC_1}$	$\overline{OC_2}$	Y
L	L	L	H
H	L	L	L
X	L	H	Z
X	H	L	Z
X	H	H	Z

Note 1: Z : high-impedance
X : irrelevant

CIRCUIT DIAGRAM (EACH BUFFER)



OCTAL BUFFER/LINE DRIVERS WITH 3-STATE OUTPUTS(INVERTED)

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ*	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
$V_{T+} - V_{T-}$	Hysteresis	$V_{CC}=4.75V$		0.2	0.4		V
V_{IC}	Input clamp voltage	$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$V_{CC}=4.75V$	$V_I=0.8V$, $I_{OH}=-3mA$	2.4	3.4		V
		$V_I=2V$	$V_I=0.5V$, $I_{OH}=-15mA$	2			V
V_{OL}	Low-level output voltage	$V_{CC}=4.75V$	$I_{OL}=12mA$		0.25	0.4	V
		$V_I=0.8V$, $V_I=2V$	$I_{OL}=24mA$		0.35	0.5	V
I_{OZH}	Off-state high-level output current	$V_{CC}=5.25V$, $V_I=2V$, $V_O=2.7V$				20	μA
I_{OZL}	Off-state low-level output current	$V_{CC}=5.25V$, $V_I=2V$, $V_O=0.4V$				−20	μA
I_{IH}	High-level input current	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
I_{IL}	Low-level input current	$V_{CC}=5.25V$, $V_I=0.4V$				−0.2	mA
I_{OS}	Short-circuit output current (Note 2)	$V_{CC}=5.25V$, $V_O=0V$		−40		−225	mA
I_{CCH}	Supply current, all outputs high	$V_{CC}=5.25V$, $V_I=0V$			13	25	mA
I_{CCL}	Supply current, all outputs low	$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$			24	45	mA
I_{CCZ}	Supply current, all outputs off	$V_{CC}=5.25V$, $V_I=4.5V$			30	52	mA

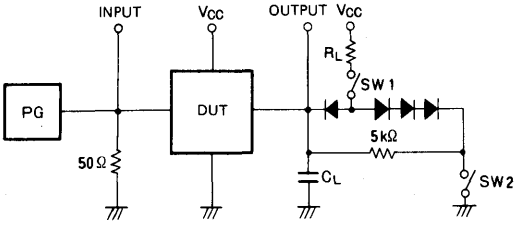
* : All typical values are at $V_{CC}=5V$, $Ta=25°C$.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input A to output Y	$C_L=45pF$ (Note 3)			15	ns
t_{PHL}					15	ns
t_{PZL}	Output enable time to low-level	$R_L=667Ω$, $C_L=45pF$ (Note 3)			38	ns
t_{PZH}	Output enable time to high-level	$R_L=667Ω$, $C_L=45pF$ (Note 3)			25	ns
t_{PLZ}	Output disable time from low-level	$R_L=667Ω$, $C_L=5pF$ (Note 3)			25	ns
t_{PHZ}	Output disable time from high-level	$R_L=667Ω$ $C_L=5pF$ (Note 3)			18	ns

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (INVERTED)

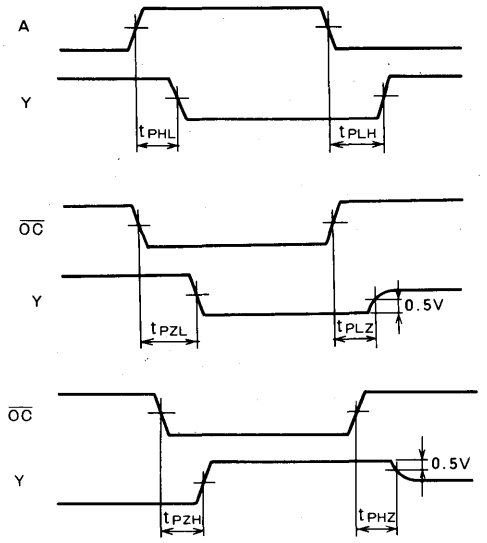
Note 3: Measurement circuit



Parameter	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, $V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS541P

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74LS541P is a semiconductor integrated circuit containing 1 buffer block with 3-state non-inverted outputs and is provided with output control inputs which are common to 8 circuits and which are independent.

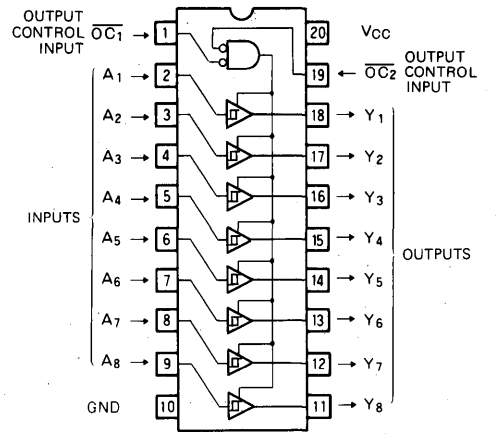
FEATURES

- Small input load factor (pnp input)
- Hysteresis provided (=400mV typical)
- High breakdown input voltage ($V_I \geqq 15V$)
- Output control inputs provided ($\overline{OC_1}$, $\overline{CO_2}$)
- High fan-out 3-state outputs (I_{OL} = 24mA, I_{OH} = −15mA)
- Data flow-thru pin out
- Wide operating temperature range (T_a=−20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTION TABLE (Note 1)

A	$\overline{OC_1}$	$\overline{OC_2}$	Y
L	L	L	L
H	L	L	H
X	L	H	Z
X	H	L	Z
X	H	H	Z

Note 1 Z : High-impedance
X : irrelevant

FUNCTIONAL DESCRIPTION

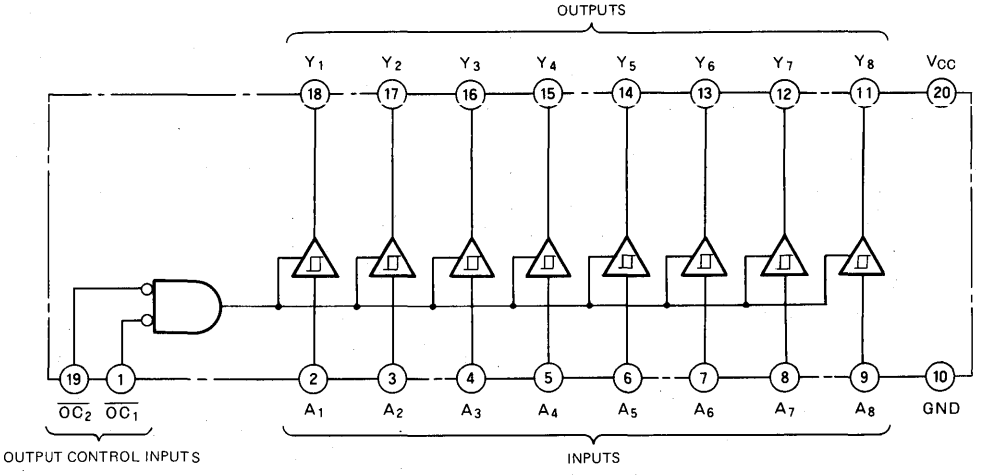
Since pnp transistors are used for the input circuits, the input load factor is small and a input high breakdown voltage is provided. The 3-state non-inverted output buffers have a high noise margin due to hysteresis.

When $\overline{OC_1}$ or $\overline{OC_2}$ is low, low appears in output Y if input A is low, and high appears in Y if A is high.

All outputs are set to the high-impedance state when $\overline{OC_1}$ and $\overline{OC_2}$ are in any other state.

The input and output pins are arranged for facilitated board layout (data flow-thru pin out).

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
$V_{T+}-V_{T-}$	Hysteresis width	V_{CC}=4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V	V_I=0.8V, I_{OH}=−3mA	2.4	3.4		V
		V_I=2V	V_I=0.5V, I_{OH}=−15mA	2			V
V_{OL}	Low-level output voltage	V_{CC}=4.75V	I_{OL}=12mA		0.25	0.4	V
		V_I=0.8V, V_I=2V	I_{OL}=24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current	V_{CC}=5.25V, V_I=2V, V_O=2.7V				20	μA
I_{OZL}	Off-state low-level output current	V_{CC}=5.25V, V_I=2V, V_O=0.4V				−20	μA
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.2	mA
I_{OS}	Short-circuit output current (Note 2)	V_{CC}=5.25V, V_O=0V		−40		−225	mA
I_{CCH}	Supply current, all outputs high	V_{CC}=5.25V, V_I=0V, V_I=4.5V			18	32	mA
I_{CCL}	Supply current, all outputs low	V_{CC}=5.25V, V_I=0V, V_I=4.5V			30	52	mA
I_{CCZ}	Supply current, all outputs disabled	V_{CC}=5.25V, V_I=0V, V_I=4.5V			32	55	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

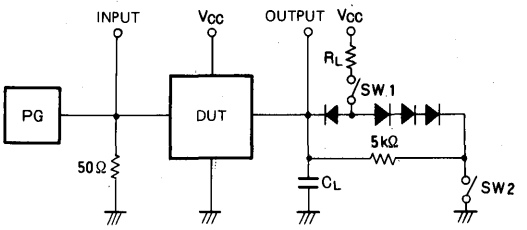
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input A to output Y	C_L=45pF (Note 3)			15	ns
t_{PHL}					18	ns
t_{PZL}	Output enable time to low-level	R_L=667Ω, C_L=45pF (Note 3)			38	ns
t_{PZH}	Output enable time to high-level	R_L=667Ω, C_L=45pF (Note 3)			32	ns
t_{PLZ}	Output disable time from low-level	R_L=667Ω, C_L= 5 pF (Note 3)			29	ns
t_{PHZ}	Output disable time from high-level	R_L=667Ω C_L= 5 pF (Note 3)			18	ns

OCTAL BUFFER/LINE DRIVER WITH 3-STATE OUTPUT (NONINVERTED)

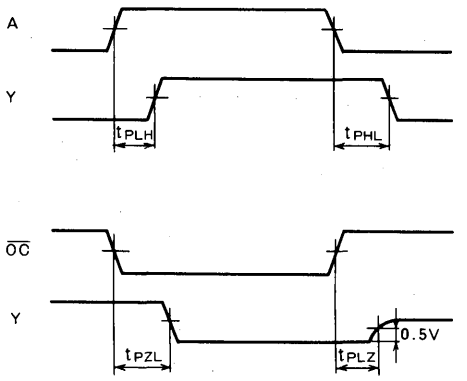
Note 3: Measurement circuit



Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
$V_P = 3V_{P-P}$, $Z_o = 50\Omega$.
(2) All diodes are switching diodes ($t_{rr} \leq 4$ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS595P

8-BIT SHIFT REGISTER/LATCH WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS595P is a semiconductor integrated circuit containing an 8-bit serial input/parallel output shift register function with a 3-state output latch.

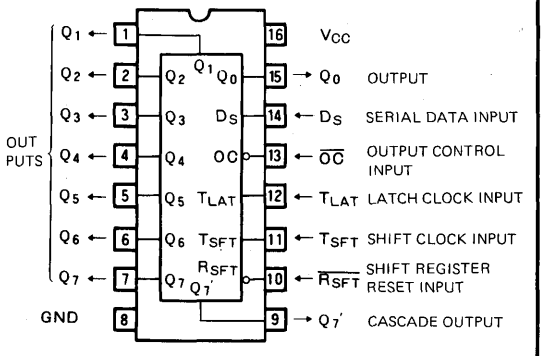
FEATURES

- 8-bit serial in, parallel out shift register with latch
- Shift register has direct reset ($\overline{R_{SFT}}$)
- Independent clock input pins (T_{SFT}, T_{LAT})
- 3-state, high fan-out outputs ($Q_0 \sim Q_7$) (I_{OL} = 24 mA, I_{OH} = −2.6mA)
- Cascade output pin provided (Q_7')
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATIONS

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

The shift register bits are each composed of two flip-flops. Separate clocks are used for shifting and latching.

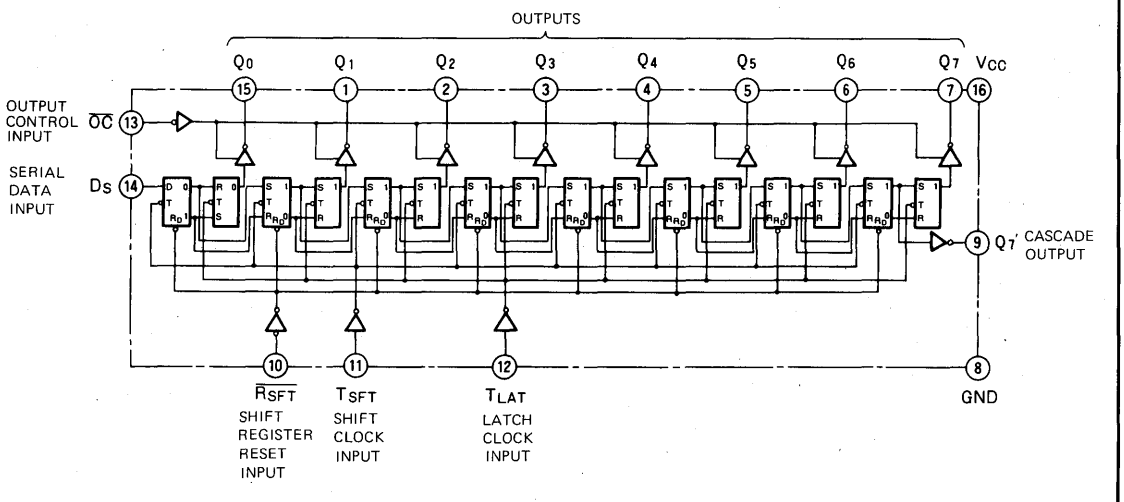
The shift clock input T_{SFT} and latch clock input T_{LAT} are independent, and the shift or latch operation is performed when the respective pin changes from low to high,

Serial data input D_s is the data input of the first stage shift register and when it is high and a pulse is applied to T_{SFT}, the high signal enters the shift register in sequence. When D_s is low and a pulse is applied to T_{SFT}, the low signal enters the shift register in sequence.

When the pulse is applied to T_{LAT}, the contents of the shift register are stored in the latch register and appear at $Q_0 \sim Q_7$. $Q_0 \sim Q_7$ are 3-state outputs with buffers. Cascade output Q_7' at which the output of the eighth shift register appears is used for expanding the number of bits.

When T_{SFT} and T_{LAT} are connected for use, the shift register state with a 1 clock delay is output to $Q_0 \sim Q_7$.

BLOCK DIAGRAM



8-BIT SHIFT REGISTER/LATCH WITH 3-STATE OUTPUT

When shift register reset input $\overline{R_{SFT}}$ is set low, the shift register and Q_7' are reset. In order to reset $Q_0 \sim Q_7$, the state of T_{LAT} must be changed from low to high after the shift register has been reset by $\overline{R_{SFT}}$.

When a high signal is applied to output control input $\overline{OC}$, $Q_0 \sim Q_7$ are put in a high-impedance state but Q_7' does not change. $\overline{OC}$ status changes have no effect on the shift operation.

FUNCTION TABLE (Note 1)

Operating mode		Input					3-state output								Cascade output Q'_7
		$\overline{R_{SFT}}$	T_{SFT}	T_{LAT}	D_S	$\overline{OC}$	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
Reset	Shift t_1	L	X	X	X	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	L
	Latch t_2	X	X	↑	X	L	L	L	L	L	L	L	L	L	L
Shift/latch operation	Shift t_1	H	↑	X	H	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	q_6^0
	Latch t_2	H	X	↑	X	L	H	q_0^0	q_1^0	q_2^0	q_3^0	q_4^0	q_5^0	q_6^0	q_6^0
	Shift t_1	H	↑	X	L	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	q_6^0
	Latch t_2	H	X	↑	X	L	L	q_0^0	q_1^0	q_2^0	q_3^0	q_4^0	q_5^0	q_6^0	q_6^0
3-state		X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	q_7

Note 1. ↑ : transition from low to high level (positive edged trigger)
Q^0 : level of Q before the indicated steady-state input conditions were established
X : Irrelevant
q^0 : contents of shift register before T_{SFT} is applied
q : shift register contents
t_1, t_2 : t_2 is set after t_1 has been set
Z : high-impedance state

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage			−0.5 ~ +15	V
V_O	Output voltage	$Q_0 \sim Q_7$	High-level state	−0.5 ~ +5.5	V
		Q_7'	Off-state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage			4.75	5	5.25	V
I_{OH}	High-level output current	$Q_0 \sim Q_7$	$V_{OH} \geqq 2.4V$	0		−2.6	mA
		Q_7'	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$Q_0 \sim Q_7$	$V_{OL} \leqq 0.4V$	0		12	mA
			$V_{OL} \leqq 0.5V$	0		24	mA
		Q_7'	$V_{OL} \leqq 0.4V$	0		4	mA
			$V_{OL} \leqq 0.5V$	0		8	mA

8-BIT SHIFT REGISTER/LATCH WITH 3-STATE OUTPUT

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

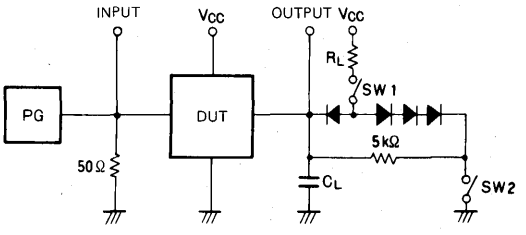
Symbol	Parameter		Test conditions		Limits Min	Limits Typ *	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	$Q_0 \sim Q_7$	$V_{CC}=4.75V$	$I_{OH}=-2.6mA$	2.4	3.1		V
		Q_7'	$V_I=0.8V$, $V_I=2V$	$I_{OH}=-400\mu A$	2.7	3.4		V
V_{OL}	Low-level output voltage	$Q_0 \sim Q_7$	$V_{CC}=4.75V$	$I_{OL}=12mA$		0.25	0.4	V
			$V_I=0.8V$	$I_{OL}=24mA$		0.35	0.5	V
		Q_7'	$V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{OZH}	Off-state high-level output current	$Q_0 \sim Q_7$	$V_{CC}=5.25V$, $V_I=0.8V$, $V_I=2V$, $V_O=2.7V$				20	μA
I_{OZL}	Off-state low-level output current	$Q_0 \sim Q_7$	$V_{CC}=5.25V$, $V_I=0.8V$, $V_I=2V$, $V_O=0.4V$				−20	μA
I_{IH}	High-level input current		$V_{CC}=5.25V$	$V_I=2.7V$			20	μA
				$V_I=10V$			0.1	mA
I_{IL}	Low-level input current	Ds	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		Input except Ds					−0.2	mA
I_{OS}	Short-circuit output current (Note 2)	$Q_0 \sim Q_7$	$V_{CC}=5.25V$, $V_O=0V$		−30		−130	mA
		Q_7'			−20		−100	mA
I_{CCH}	High-level supply current		$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$			29	50	mA
I_{CCL}	Low-level supply current		$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$			39	65	mA
I_{CCZ}	Off-state supply current		$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$			41	65	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum repeat frequency	$C_L=15pF$ (Note 3)	20	25		MHz
t_{PLH}	Low-to-high, high-to-low output propagation time, from input T_{SFT} to output Q'_7			11	18	ns
t_{PHL}				16	25	
t_{PHL}	High-to-low output propagation time from input $\overline{R_{SFT}}$ to output Q'_7			19	35	ns
t_{PLH}	Low-to-high, high-to-low output propagation time, from input T_{LAT} to outputs $Q_0 \sim Q_7$	$C_L=45pF$ (Note 3)		12	18	ns
t_{PHL}				22	35	
t_{PZH}	Output enable time to high level	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		16	30	ns
t_{PZL}	Output enable time to low level			20	38	ns
t_{PHZ}	Output disable time to high level	$R_L=667\Omega$, $C_L=5pF$ (Note 3)		22	30	ns
t_{PLZ}	Output disable time to low level			17	38	ns

Note 3. Measurement circuit



Parameter	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

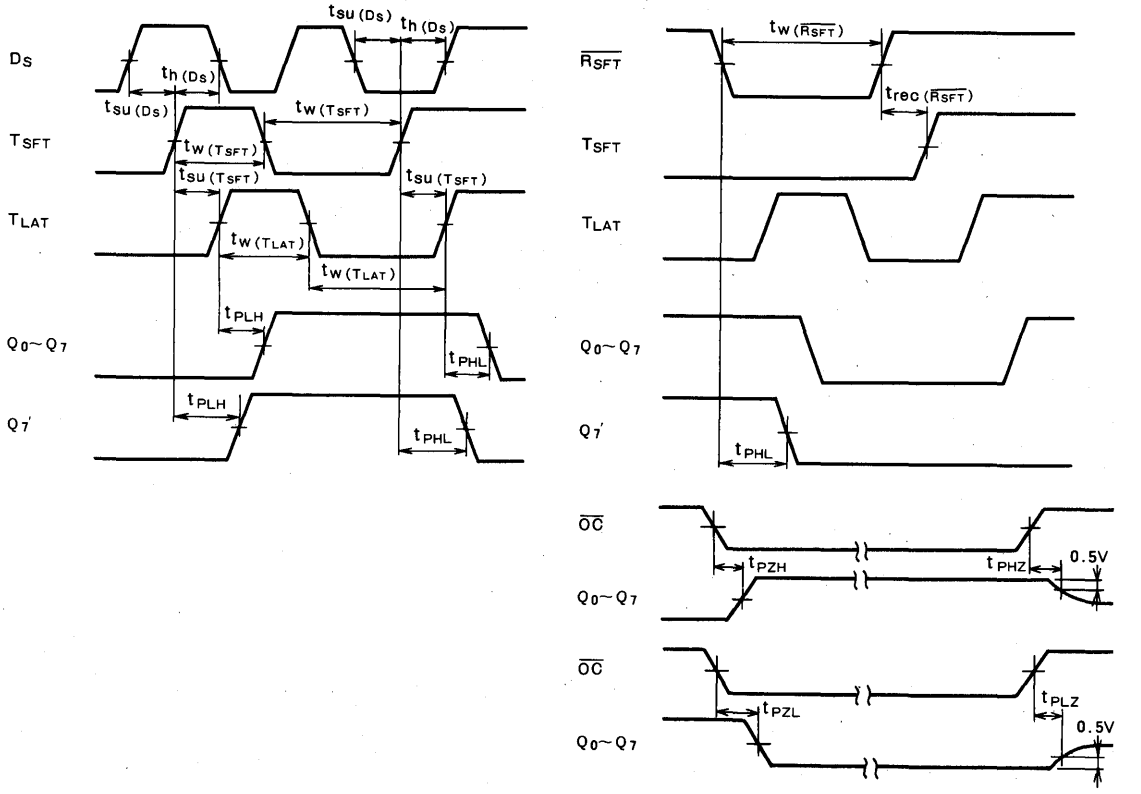
(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P-P}$, Z_o = 50 ohms.
(2) All diodes are switching diodes ($t_{rr} \leqq 4ns$).
(3) C_L includes probe and jig capacitance.

8-BIT SHIFT REGISTER/LATCH WITH 3-STATE OUTPUT

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(T_{SFT})}$	Shift clock input pulse width		25	22		ns
$t_{w(T_{LAT})}$	Latch clock input pulse width		20	12		ns
$t_{w(\overline{R_{SFT}})}$	Shift register reset pulse width		20	10		ns
$t_{su(Ds)}$	Setup time D_s to T_{SFT}		20	12		ns
$t_{h(Ds)}$	Hold time D_s to T_{SFT}		2	−1		ns
$t_{rec(\overline{R_{SFT}})}$	Recovery time $\overline{R_{SFT}}$ to T_{SFT}		20	12		ns
$t_{su(T_{SFT})}$	Setup time T_{SFT} to T_{LAT}		40	12		ns

TIMING DIAGRAMS (Reference level = 1.3V)



MITSUBISHI ELECTRIC

M74LS596P

8-BIT SHIFT REGISTER/LATCH WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS596P is a semiconductor integrated circuit containing an 8-bit serial input/parallel output shift register function with an open collector output latch.

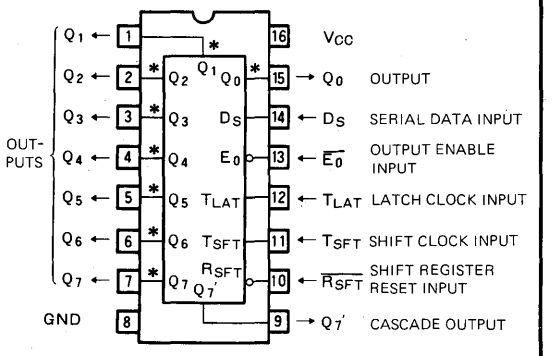
FEATURES

- 8-bit serial in parallel out shift register with latch.
- Shift register has direct reset ($\overline{R_{SFT}}$)
- Independent clock input pins (T_{SFT}, T_{LAT})
- Open-collector, high fan-out outputs ($Q_0 \sim Q_7$) (I_n= 24mA)
- Cascade output pin provided (Q'_7)
- Wide operating temperature range ($T_a = -20 \sim +75°C$)

APPLICATIONS

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

The shift register bits are each composed of two flip-flops Separate clocks are used for shifting and latching.

The shift clock input T_{SFT} and latch clock input T_{LAT} are independent, and the shift or latch operation is performed when the respective pin changes from low to high.

Serial data input D_s is the data input of the first stage shift register and when it is high and the pulse is applied to T_{SFT}, the high signal enters the shift register in sequence. When D_s is low and a pulse is applied to T_{SFT}, the low signal enters a shift register in sequence.

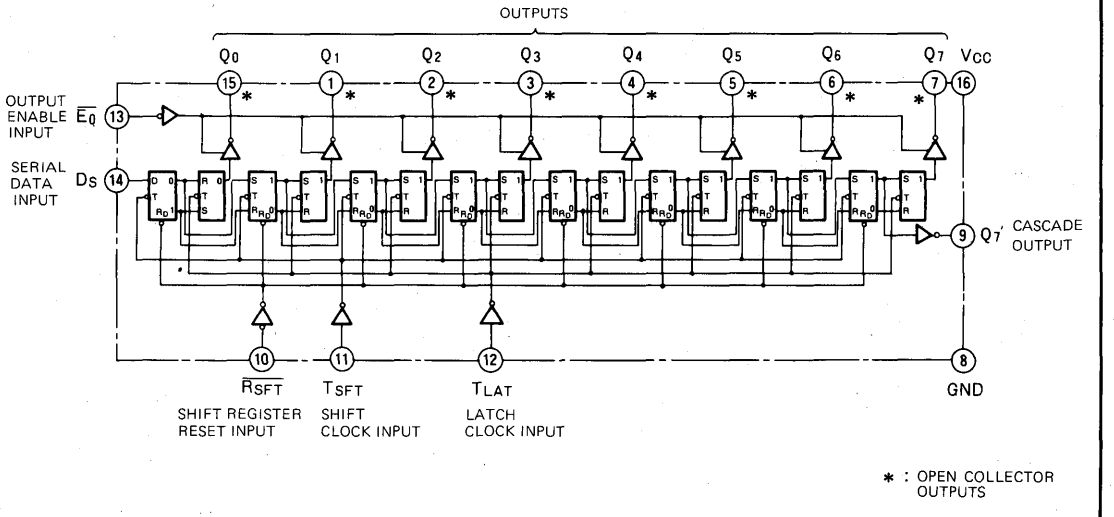
When a pulse is applied to T_{LAT}, the contents of the shift register are stored in the latch register and appear at $Q_0 \sim Q_7$. $Q_0 \sim Q_7$ are open collector outputs with buffers.

Cascade output Q_7' at which the output of the eighth shift register appears is used for expanding the number of bits.

When T_{SFT} and T_{LAT} are connected for use, the shift register state with a 1 clock delay is output to $Q_0 \sim Q_7$.

When shift register reset input $\overline{R_{SFT}}$ is set low, the shift

BLOCK DIAGRAM



8-BIT SHIFT REGISTER/LATCH WITH OPEN COLLECTOR OUTPUT

register and Q'_7 are reset. In order to reset $Q_0 \sim Q_7$, the state of T_{LAT} must be changed from low to high after the shift register has been reset by $\overline{R_{SFT}}$.

When a high signal is applied to output enable input $\overline{E_0}$, $Q_0 \sim Q_7$ are set high but Q_7' does not change. $\overline{E_0}$ status changes have no effect on the shift operation.

FUNCTION TABLE (Note 1)

Operating mode		Input					Open collector output								Cascade output Q'_7
		$\overline{R_{SFT}}$	T_{SFT}	T_{LAT}	D_S	$\overline{E_0}$	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
Reset	Shift t_1	L	X	X	X	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	L
	Latch t_2	X	X	↑	X	L	L	L	L	L	L	L	L	L	L
Shift/latch operation	Shift t_1	H	↑	X	H	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	q_6^0
	Latch t_2	H	X	↑	X	L	H	q_0^0	q_1^0	q_2^0	q_3^0	q_4^0	q_5^0	q_6^0	q_6^0
	Shift t_1	H	↑	X	L	L	Q_0^0	Q_1^0	Q_2^0	Q_3^0	Q_4^0	Q_5^0	Q_6^0	Q_7^0	q_6^0
	Latch t_2	H	X	↑	X	L	L	q_0^0	q_1^0	q_2^0	q_3^0	q_4^0	q_5^0	q_6^0	$q^0{}_6$
Output disable		X	X	X	X	H	H	H	H	H	H	H	H	H	q_7

Note . ↑ : transition from low to high level (positive edged trigger)

Q^0: level of Q before the indicated steady-state input conditions were established

X : irrelevant

q^0: contents of shift register before T_{SFT} is applied

q : shift register contents

t_1, t_2 : t_2 is set after t_1 has been set

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage			−0.5 ~ +15	V
V_O	Output voltage	$Q_0 \sim Q_7$	High-level state	−0.5 ~ +7	V
		Q_7'		−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min	Typ	Max	
V_{CC}	Supply voltage			4.75	5	5.25	V
I_{OH}	High-level output current	$Q_0 \sim Q_7$	V_O=5.5V	0		100	μA
		Q_7'	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$Q_0 \sim Q_7$	$V_{OL} \leqq 0.4V$	0		12	mA
			$V_{OL} \leqq 0.5V$	0		24	mA
		Q_7'	$V_{OL} \leqq 0.4V$	0		4	mA
			$V_{OL} \leqq 0.5V$	0		8	mA

8-BIT SHIFT REGISTER/LATCH WITH OPEN COLLECTOR OUTPUT

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage	Q'_7	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
I_{OH}	High-level output voltage	$Q_0 \sim Q_7$	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $V_O=5.5V$				100	μA
V_{OL}	Low-level output voltage	$Q_0 \sim Q_7$	$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=12mA$		0.25	0.4	V
				$I_{OL}=24mA$		0.35	0.5	V
		Q'_7		$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current		$V_{CC}=5.25V$	$V_I=2.7V$			20	μA
				$V_I=10V$			0.1	mA
I_{IL}	Low-level input current	D_S	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		Input except D_S					−0.2	mA
I_{OS}	Short-circuit output current (Note 2)	Q'_7	$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CCH}	High-level supply current		$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$					mA
I_{CCL}	Low-level supply current		$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$					mA
I_{CCZ}	Off-state supply current		$V_{CC}=5.25V$, $V_I=0V$, $V_I=4.5V$					mA

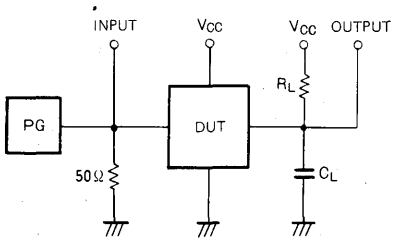
∗ : All values are at $V_{CC}=5V$, $T_a=25°C$

Note 2: All measurements should be done quickly and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
f_{max}	Maximum repeat frequency from input T_{SFT} to output Q'_7	$R_L=2k\Omega$, $C_L=15pF$ (Note 3)	20	25		MHz
t_{PLH}	Low-to-high, high-to-low output propagation time, from input T_{SFT} to output Q'_7			16	21	ns
t_{PHL}				12	30	
t_{PHL}	High-to-low output propagation time from input $\overline{R_{SFT}}$ to output Q'_7			19	35	ns
t_{PLH}	Low-to-high, high-to-low output propagation time, from input T_{LAT} to outputs $Q_0 - Q_7$	$R_L=667\Omega$, $C_L=45pF$ (Note 3)		24	42	ns
t_{PHL}				23	35	
t_{PLH}	Low-to-high, high-to-low output propagation time, from input $\overline{E_0}$ to output $Q_0 - Q_9$			30	60	ns
t_{PHL}				12	38	

Note 3. Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r 6ns, t_f = 6ns, t_w = 500ns, $V_P = 3V_{P-P}$, Z_o = 50 ohms.

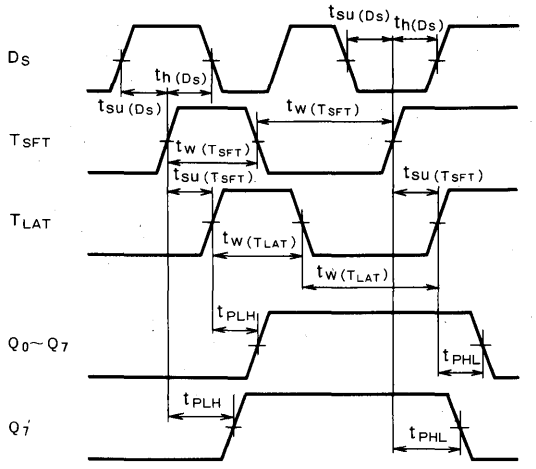
(2) C_L includes probe and jig capacitance.

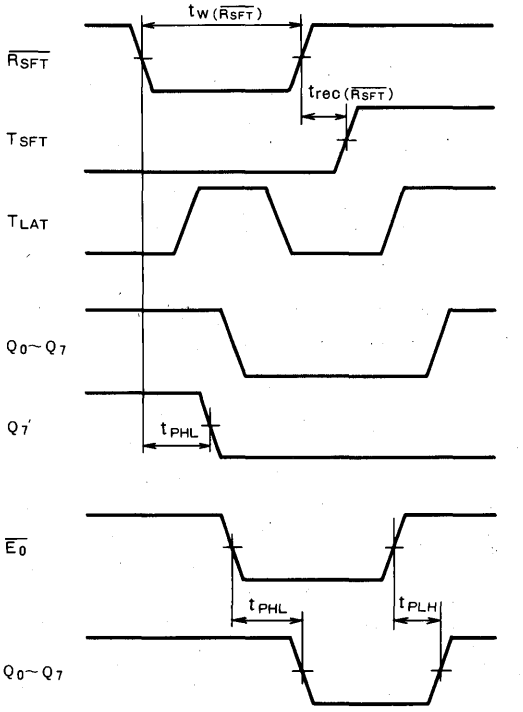
8-BIT SHIFT REGISTER/LATCH WITH OPEN COLLECTOR OUTPUT

TIMING REQUIREMENTS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(T_{SFT})}$	Shift clock input pulse width		25	22		ns
$t_{W(T_{LAT})}$	Latch clock input pulse width		20	12		ns
$t_{W(\overline{R_{SFT}})}$	Shift register reset pulse width		20	9		ns
$t_{SU(D_S)}$	Setup time D_s to T_{SFT}		20	12		ns
$t_{h(D_S)}$	Hold time D_s to T_{SFT}		2	−1		ns
$t_{REC(\overline{R_{SFT}})}$	Recovery time $\overline{R_{SFT}}$ to T_{SFT}		20	12		ns
$t_{SU(T_{SFT})}$	Setup time T_{SFT} to T_{LAT}		40	12		ns

TIMING DIAGRAMS (Reference level = 1.3V)





MITSUBISHI ELECTRIC

M74LS620P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS620P is a semiconductor integrated circuit containing an octal bus transmitter/receiver with a tri-state inverted output.

FEATURES

- Two 8-bit data trains can be transmitted bidirectionally or as unidirectional pulses
- Input/output A and output/input B each exhibit hysteresis characteristics (Hysteresis width = 400mV typ)
- High fan-out capability (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment

FUNCTIONAL DESCRIPTION

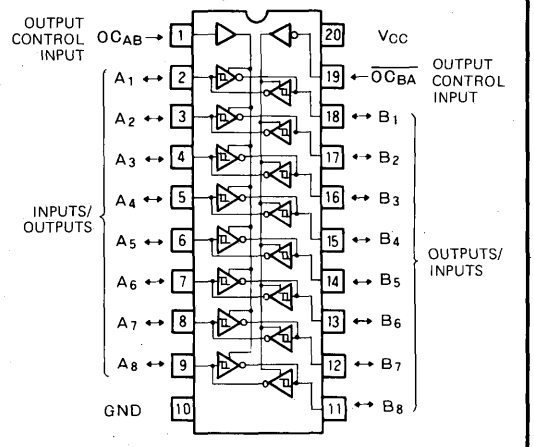
In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with 3-state inverted outputs are made two-way buffers.

The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin.

The input/output direction is controlled by OC_{AB} and $\overline{OC_{BA}}$.

When OC_{AB} and $\overline{OC_{BA}}$ are high, A becomes the input pin, with output obtained at pin B. Conversely, when OC_{AB} are $\overline{OC_{BA}}$ are low, B is the input and A is the output.

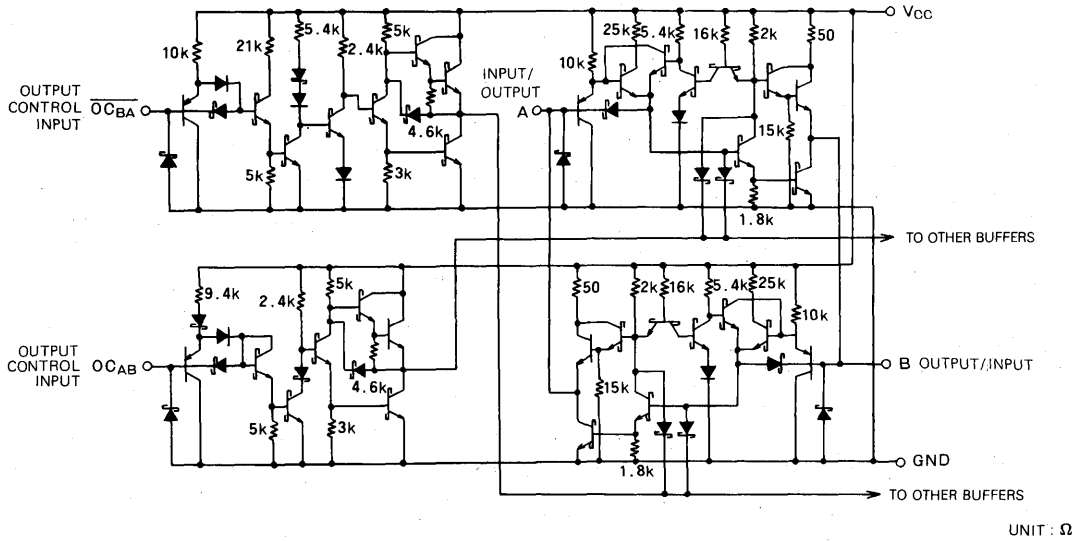
PIN CONFIGURATION (TOP VIEW)



Outline 20P4

A high impedance status is initiated at both pin A and B when OC_{AB} is low and $\overline{OC_{BA}}$ is high, isolating A from B. Precautions should be taken to guard against OC_{AB} being at a high while $\overline{OC_{BA}}$ is low. This condition will result in output from both A and B, and could result in the IC being destroyed.

CIRCUIT DIAGRAM (EACH BUFFER)



UNIT : Ω

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

$\overline{OC_{BA}}$	OC_{AB}	A	B
L	L	O	I
H	H	I	O
H	L	Z	Z
L	H	*	*

Note 1. I : Input pin
O : Output pin
Z : High-impedance (A and B isolated)
* : Inhibit (No output from either A or B)

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +5.5	V
		OC_{AB}, $\overline{OC_{BA}}$		−0.5 ~ +15	V
V_O	Output voltage		Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+}-V_{T-}$	Hysteresis width		V_{CC}=4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V	I_{OH}=−3mA	2.4	3.4		V
			V_I=0.6V, V_{IH}=2V	I_{OH}=−15mA	2			V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=12mA		0.25	0.4	V
			V_I=0.6V, V_{IH}=2V	I_{OL}=24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.25V, V_I=0.6V, V_{IH}=2V, V_O=2.7V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.25V, V_I=0.6V, V_{IH}=2V, V_O=0.4V				−400	μA
I_{IH}	High-level input current	A, B	V_{CC}=5.25V, V_I=2.7V				20	μA
		$\overline{OC_{BA}}$, OC_{AB}					20	μA
		A, B	V_{CC}=5.25V, V_I=5.5V				0.1	mA
		$\overline{OC_{BA}}$, OC_{AB}	V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current		V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−40		−225	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.25V, V_I=0V, V_{IH}=4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.25V, V_I=0V, V_{IH}=4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC}=5.25V, V_I=0V, V_{IH}=4.5V			64	95	mA

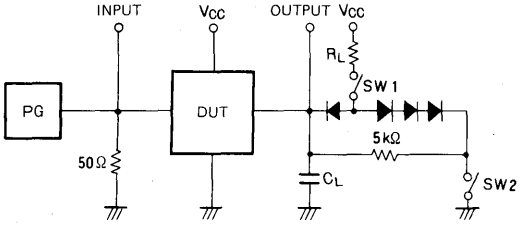
* : All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	From input A to output B	C_L=45pF (Note 3)		8	10	ns
		From input B to output A			8	10	
t_{PHL}	High-to-low level output propagation time	From input A to output B			12	15	ns
		From input B to output A			12	15	
t_{PZL}	Output enable time to low-level	From input $\overline{OC_{BA}}$ to output A	R_L=667Ω, C_L=45pF (Note 3)		25	40	ns
		From input OC_{AB} to output B			25	40	
t_{PZH}	Output enable time to high-level	From input $\overline{OC_{BA}}$ to output A			23	40	ns
		From input OC_{AB} to output B			23	40	
t_{PLZ}	Output disable time from low-level	From input $\overline{OC_{BA}}$ to output A	R_L=667Ω, C_L=5pF (Note 3)		17	25	ns
		From input OC_{AB} to output B			17	25	
t_{PHZ}	Output disable time from high-level	From input $\overline{OC_{BA}}$ to output A			19	25	ns
		From input OC_{AB} to output B			19	25	

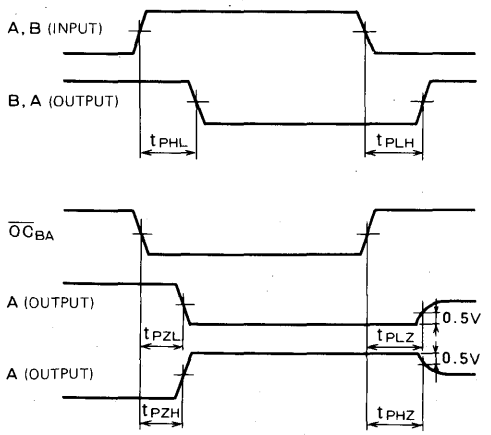
Note 3: Measurement Circuit

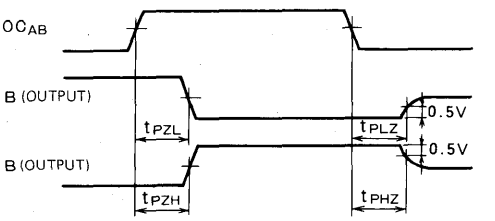


Parameter	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) All diodes have high-speed switching characteristics ($t_{rr} \leq$ 4ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)





M74LS640P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS640P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Hysteresis provided (width = 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 24mA, I_{OH} = –15mA)
- Wide operating temperature range. (T_a = –20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

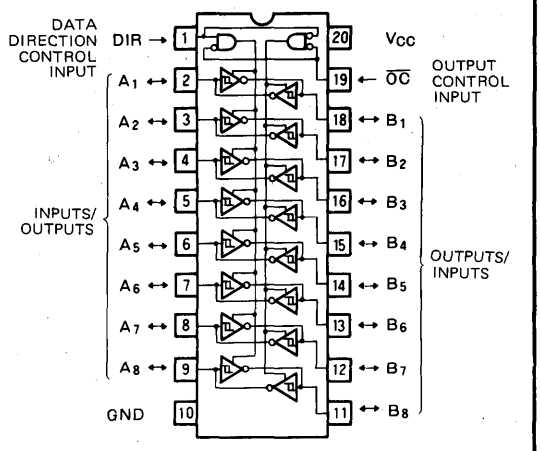
The inputs and outputs of the two buffer circuits with 3-state inverted outputs are connected together to form bi-directional buffers. Having hysteresis characteristics in the input section of input/output A and output/input B, noise margin is high.

The data direction control input DIR controls the direction of input and output. When DIR is high, A is the input terminal and B is the output terminal and when DIR is low, A is the output terminal and B is the input terminal.

When the output control input $\overline{OC}$ is high, both A and B are put in the high-impedance state so the buffers are isolated.

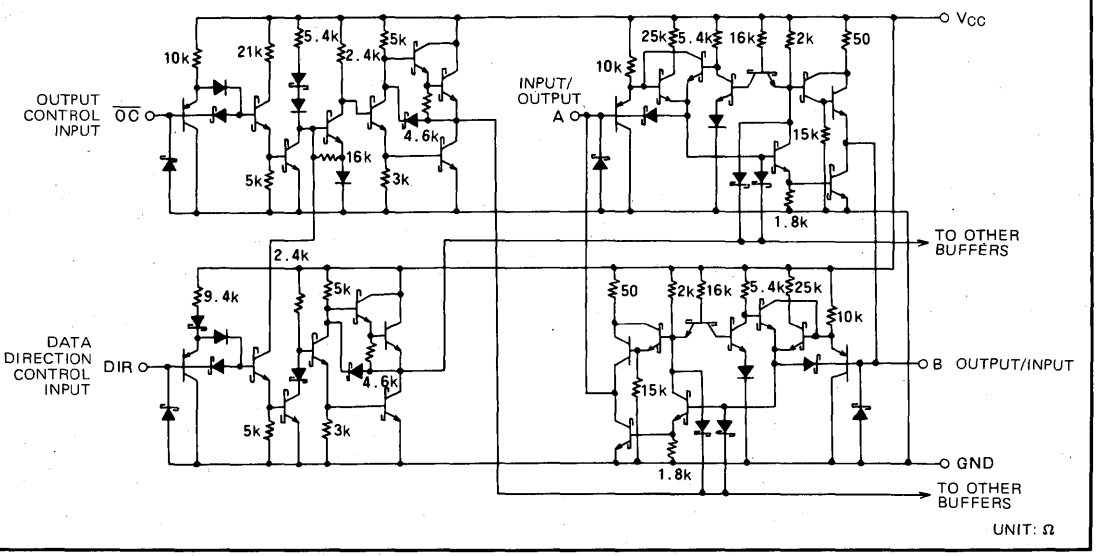
A device, M74LS640-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

CIRCUIT DIAGRAM (Each buffer)



MITSUBISHI ELECTRIC

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1: I: Input pin
$\overline{O}$: Output (inverted output) pin
Z: High impedance (A and B separated)
X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +5.5	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		Off state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+}-V_{T-}$	Hysteresis width		V_{CC} = 4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V	I_{OH} = −3 mA	2.4	3.4		V
			V_I = 0.6V, V_I = 2V	I_{OH} = −15mA	2			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V	I_{OL} = 12mA		0.25	0.4	V
			V_I = 0.6V, V_I = 2V	I_{OL} = 24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC} = 5.25V, V_I = 0.6V, V_I = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC} = 5.25V, V_I = 0.6V, V_I = 2V, V_O = 0.4V				−400	μA
I_{IH}	High-level input current	A, B	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC} = 5.25V, V_I = 5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current		V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)		V_{CC} = 5.25V, V_O = 0V		−40		−225	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			48	70	mA
I_{CCL}	Supply current, all outpus low		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			64	95	mA

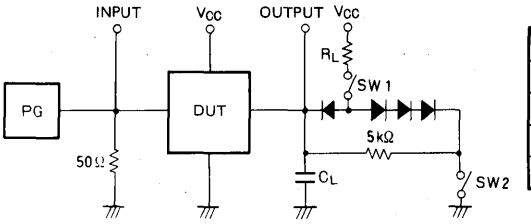
*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high level output propagation time	From input A to output B	C_L=45pF (Note 3)		8	10	ns
		From input B to output A			8	10	
t_{PHL}	High-to-low level output propagation time	From input A to output B			12	15	ns
		From input B to output A			12	15	
t_{PZL}	Low output enable time	From input $\overline{OC}$ to output A	R_L=667Ω C_L=45pF (Note 3)		25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PZH}	High output enable time	From input $\overline{OC}$ to output A			23	40	ns
		From input $\overline{OC}$ to output B			23	40	
t_{PLZ}	Low output disable time	From input $\overline{OC}$ to output A	R_L=667Ω C_L=5pF (Note 3)		17	25	ns
		From input $\overline{OC}$ to output B			17	25	
t_{PHZ}	High output disable time	From input $\overline{OC}$ to output A			19	25	ns
		From input $\overline{OC}$ to output B			19	25	

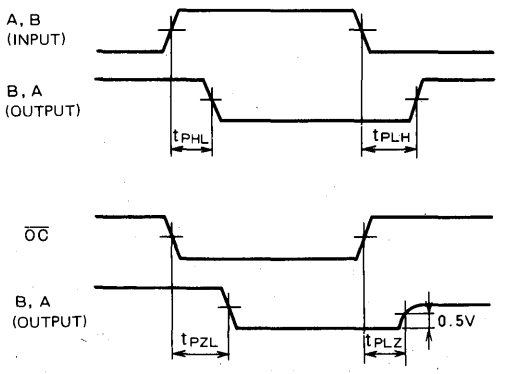
Note 3: Measurement circuit



Parameter	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω
(2) All diodes are high speed switching diodes ($t_{rr} \leq$ 4ns).
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS640-1P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

DESCRIPTION

The M74LS640-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 48mA, I_{OH} = −15mA)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

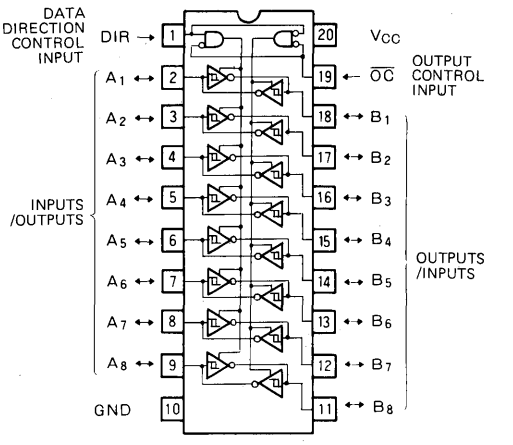
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with 3-state inverted outputs are made two-way buffers.

The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

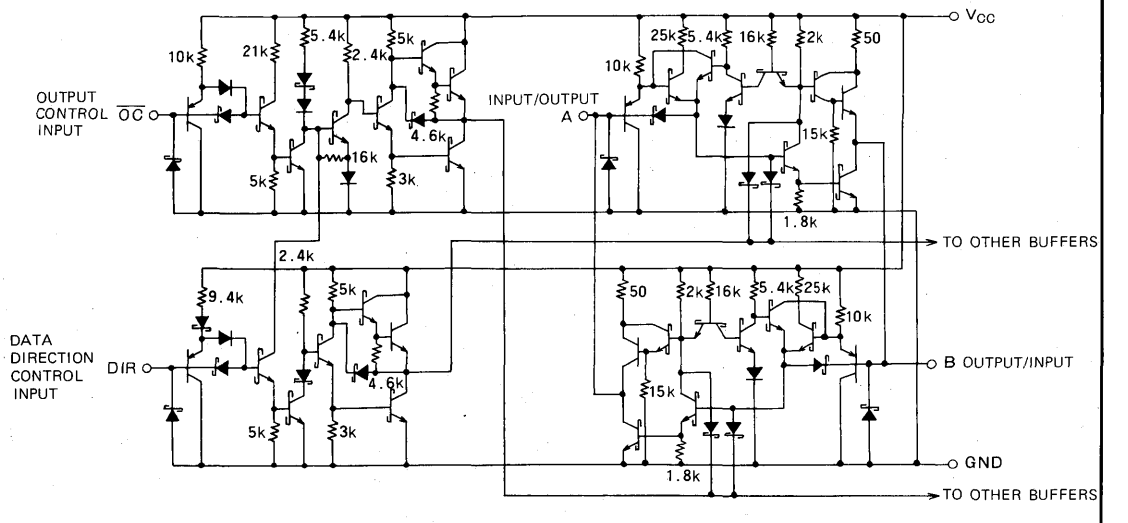
When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When $\overline{OC}$ is high, both A and B are put in the high-impedance state and A and B are isolated.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

CIRCUIT DIAGRAM (EACH BUFFER)



OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1: I : Input pin
$\overline{O}$: Output (inverted) pin
Z : High-impedance (A, B isolated)
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +5.5	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		48	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+}-V_{T-}$	Hysteresis width		V_{CC}=4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V	I_{OH}=−3mA	2.4	3.4		V
			V_I=0.6V, V_I=2V	I_{OH}=−15mA	2			V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=12mA		0.25	0.4	V
			V_I=0.6V, V_I=2V	I_{OL}=24mA		0.35	0.5	V
				I_{OL}=48mA		0.4	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.25V, V_I=0.6V, V_I=2V, V_O=2.7V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.25V, V_I=0.6V, V_I=2V, V_O=0.4V				−400	μA
I_{IH}	High-level input current	A, B	V_{CC}=5.25V, V_I=2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC}=5.25V, V_I=5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current		V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−40		−225	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.25V, V_I=0V, V_I=4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.25V, V_I=0V, V_I=4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC}=5.25V, V_I=0V, V_I=4.5V			64	95	mA

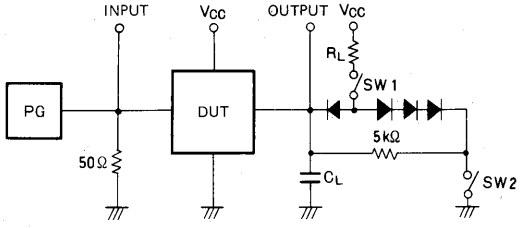
* : All typical values are at V_{CC}=5V, Ta=25°C
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (INVERTED)

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	From input A to output B	C_L=45pF (Note 3)		8	10	ns
		From input B to output A			8	10	
t_{PHL}	High-to-low level output propagation time	From input A to output B			12	15	ns
		From input B to output A			12	15	
t_{PZL}	Low-level output enable time	From input $\overline{OC}$ to output A	R_L = 667Ω C_L = 45pF (Note 3)		25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PZH}	High-level output enable time	From input $\overline{OC}$ to output A			23	40	ns
		From input $\overline{OC}$ to output B			23	40	
t_{PLZ}	Low-level output disable time	From input $\overline{OC}$ to output A	R_L = 667Ω C_L = 5pF (Note 3)		17	25	ns
		From input $\overline{OC}$ to output B			17	25	
t_{PHZ}	High-level output disable time	From input $\overline{OC}$ to output A			19	25	ns
		From input $\overline{OC}$ to output B			19	25	

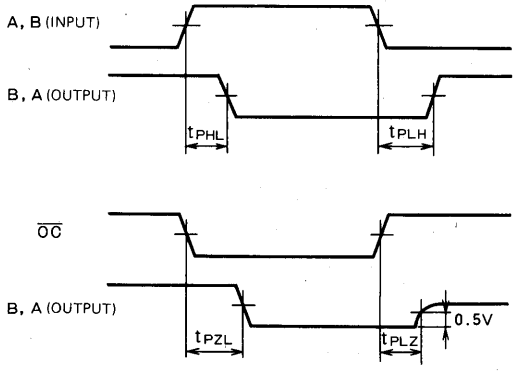
Note 3: Measurement circuit



Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω.
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns).
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS641P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

DESCRIPTION

The M74LS641P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with non-inverted open collector outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Open collector outputs
- Hysteresis provided (width = 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 24mA)
- Wide operating temperature range. (T_a = –20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

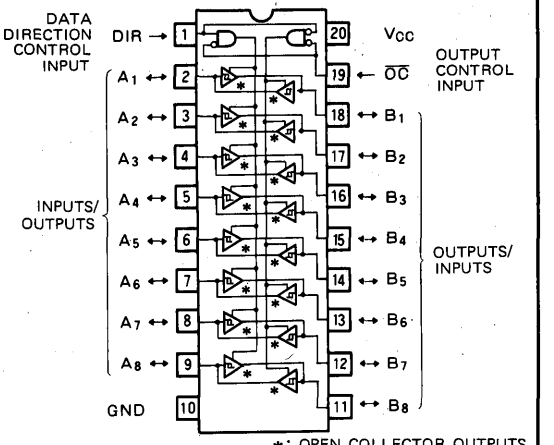
The inputs and outputs of the two buffer circuits with 3-state non-inverted outputs are connected together to form bi-directional buffers. The input sections of input/output A and output/input B have been designed with hysteresis characteristics giving increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is the input pin and B is the output pin. When DIR is low then B is input terminal and A is the output terminal. When output control input OC is high, A and B become high so the buffers are isolated.

Open collector outputs are provided, so the high-level output impedance can be freely selected with external load resistors.

The functions and pin connections of this IC are identical to those of M74LS645P.

PIN CONFIGURATION (TOP VIEW)

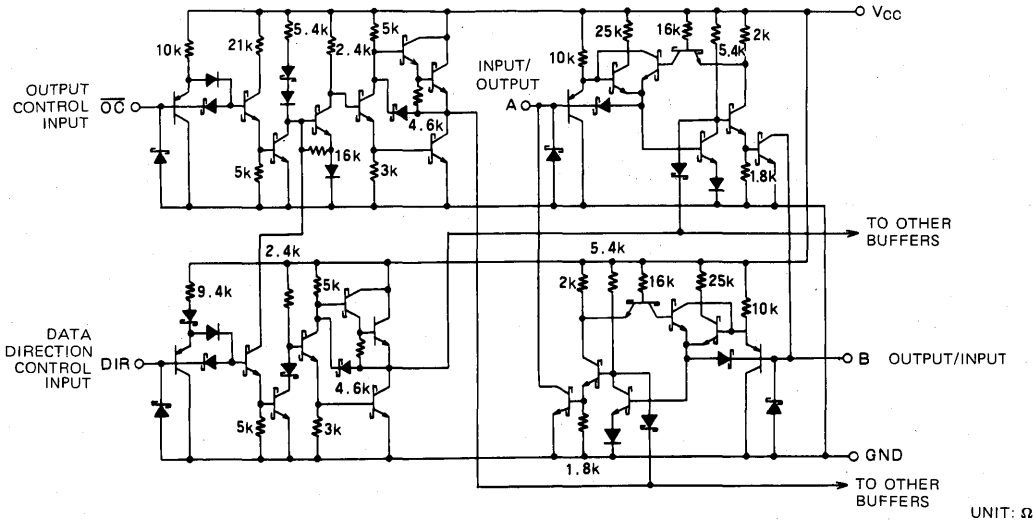


*: OPEN COLLECTOR OUTPUTS

Outline 20P4

A device, M74LS641-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.

CIRCUIT DIAGRAM (Each buffer)



MITSUBISHI ELECTRIC

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	H	H

Note 1: I: Input pin
O: Output (non-inverted output) pin
X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +7	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		High-level state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	℃
Tstg	Storage temperature range			−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O=5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+}-V_{T-}$	Hysteresis width		V_{CC}=4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
I_{OH}	High-level output current		V_{CC}=4.75V, V_I=0.6V, V_I'=2V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.6V, V_I=2V	I_{OL}=12mA		0.25	0.4	V
				I_{OL}=24mA		0.35	0.5	V
I_{IH}	High-level input current	A, B	V_{CC}=5.25V, V_I=2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC}=5.25V, V_I=5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current		V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.25V, V_I=0V, V_I=4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.25V, V_I=0V, V_I=4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC}=5.25V, V_I=0V, V_I=4.5V			64	95	mA

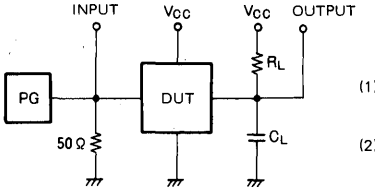
* : All typical values are at V_{CC} = 5V, T_a = 25°C.

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

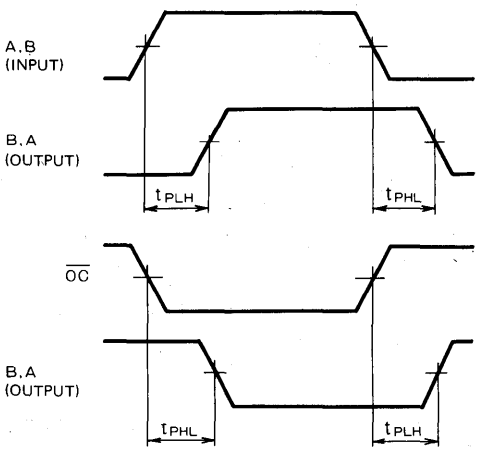
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high level output propagation time	From input A to output B	C_L=45pF, R_L=667Ω (Note 2)		20	25	ns
		From input B to output A			20	25	
t_{PHL}	High-to-low level output propagation time	From input A to output B			15	25	ns
		From input B to output A			15	25	
t_{PLH}	Low-to-high level output propagation time	From input $\overline{OC}$ to output A			25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PHL}	High-to-low level output propagation time	From input $\overline{OC}$ to output A			30	50	ns
		From input $\overline{OC}$ to output B			30	50	

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS641-1P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

DESCRIPTION

The M74LS641-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with non-inverted outputs.

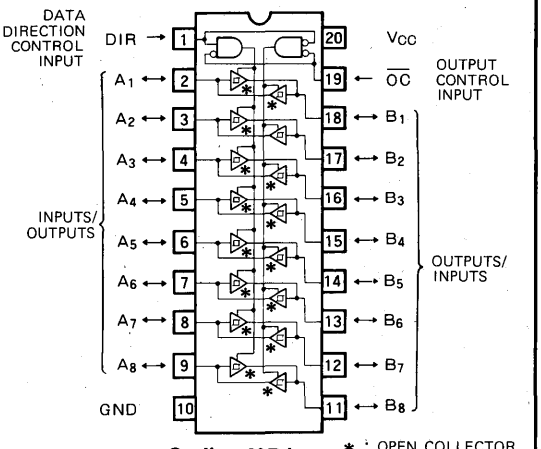
FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Open collector outputs
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 48mA)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

* : OPEN COLLECTOR OUTPUTS

FUNCTIONAL DESCRIPTION

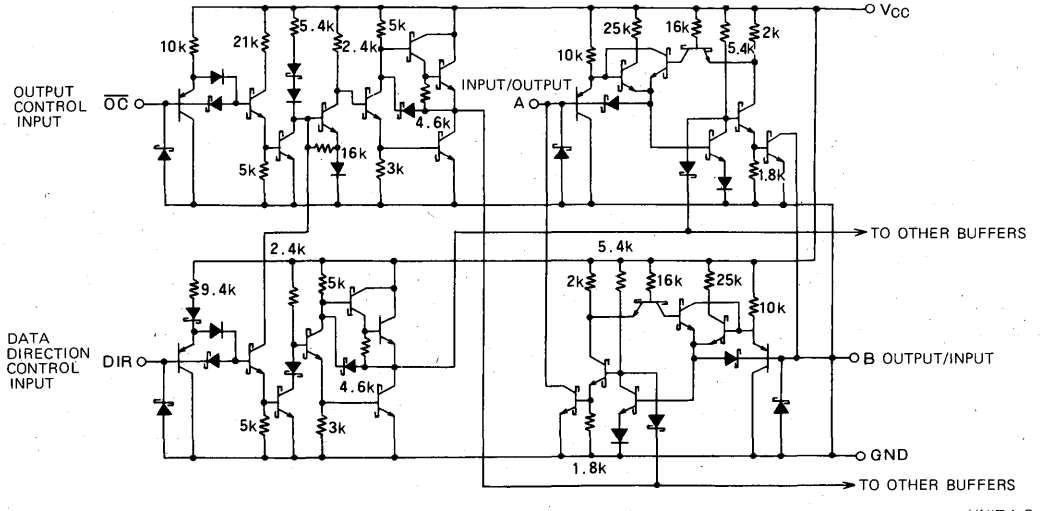
In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with open collector non-inverted outputs are made two-way buffers.

The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When output control input $\overline{OC}$ is high, both A and B go to high and are isolated.

The functions and pin connections of this device are identical to those of M74LS645-1P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

CIRCUIT DIAGRAM (EACH BUFFER)



OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	H	H

Note 1: I : Input pin
O : Output (non-inverted) pin
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +7	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		High-level state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	℃
Tstg	Storage temperature range			−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O=5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		48	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+}-V_{T-}$	Hysteresis width		V_{CC}=4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
I_{OH}	High-level output current		V_{CC}=4.75V, V_I=0.6V, V_I=2V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.6, V_I=2V	I_{OL}=12mA		0.25	0.4	V
				I_{OL}=24mA		0.35	0.5	V
				I_{OL}=48mA		0.4	0.5	V
I_{IH}	High-level input current	A, B	V_{CC}=5.25V, V_I=2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC}=5.25V, V_I=5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current		V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.25V, V_I=0V, V_I=4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.25V, V_I=0V, V_I=4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC}=5.25V, V_I=0V, V_I=4.5V			64	95	mA

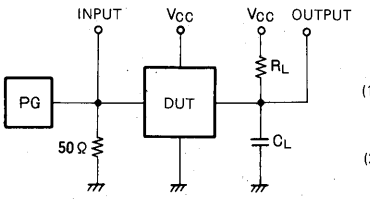
* : All typical values are at V_{CC}=5V, Ta=25℃

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT(NONINVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

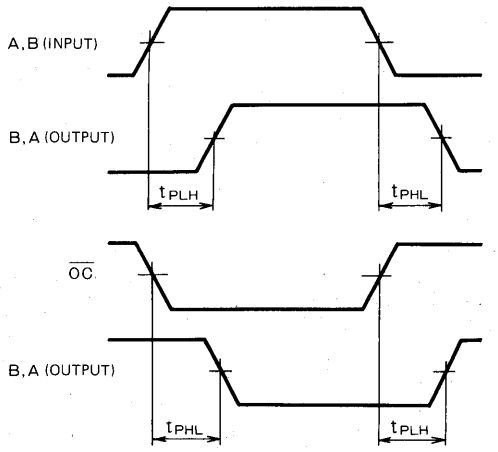
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	From input A to output B	C_L=45pF, R_L=667Ω (Note 2)		20	25	ns
		From input B to output A			20	25	
t_{PHL}	High-to-low level output propagation time	From input A to output B			15	25	ns
		From input B to output A			15	25	
t_{PLH}	Low-to-high level output propagation time	From input $\overline{OC}$ to output A			25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PHL}	High-to-low-level output propagation time	From input $\overline{OC}$ to output A			30	50	ns
		From input $\overline{OC}$ to output B			30	50	

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_o = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS642P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

DESCRIPTION

The M74LS642P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted open collector outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Open collector outputs
- Hysteresis provided (width = 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 24mA)
- Wide operating temperature range. (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

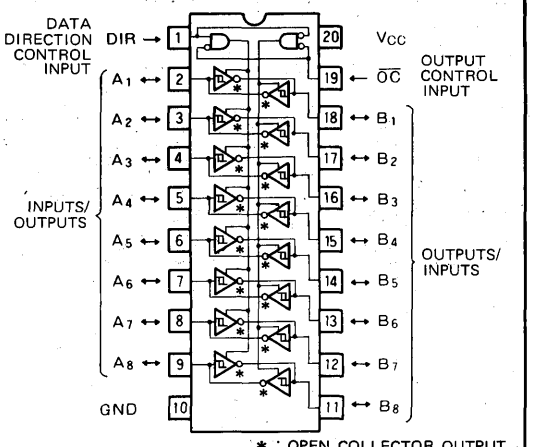
The inputs and outputs of the two buffer circuits with inverted output open collectors are connected together to form bi-directional buffers.

The input sections of input/output A and output/input B have been designed with hysteresis characteristics for increased noise margin. The input/output direction is controlled by DIR.

When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin. When output control input $\overline{OC}$ is high, A and B become high so the buffers are isolated.

Open collector outputs are provided, so the high-level output impedance can be freely selected with external load resistors.

PIN CONFIGURATION (TOP VIEW)

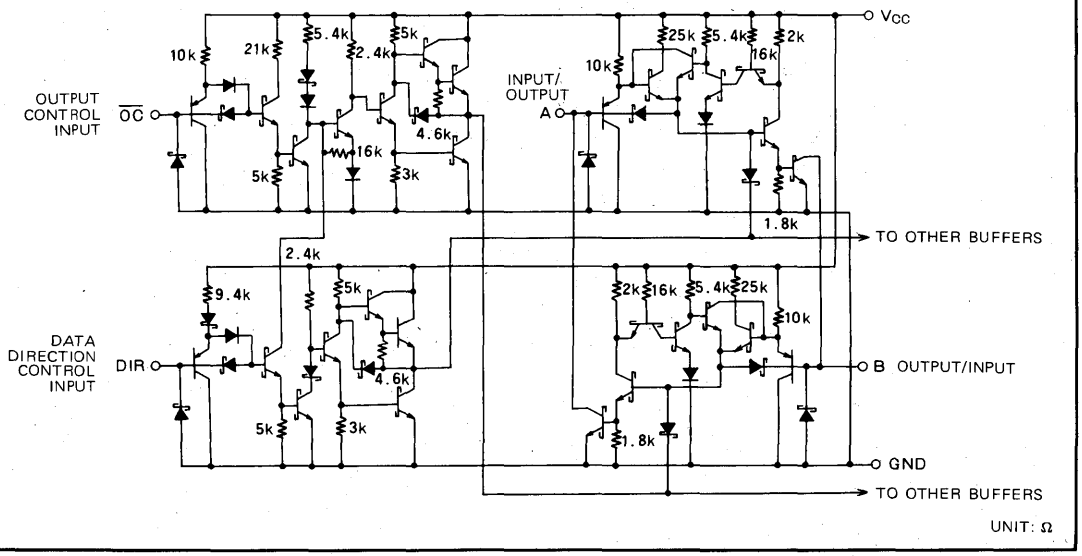


Outline 20P4

The functions and pin connections of this IC are identical to those of M74LS640P.

A device, M74LS642-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.

CIRCUIT DIAGRAM (Each buffer)



MITSUBISHI ELECTRIC

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	H	H

Note 1: I: Input pin
$\overline{O}$: Output (inverted output) pin
X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +7	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		High-level state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	℃
Tstg	Storage temperature range			−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O = 5.5V	0		100	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+} - V_{T-}$	Hysteresis width		V_{CC} = 4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
I_{OH}	High-level output current		V_{CC} = 4.75V, V_I = 0.6V, V_I = 2V, V_{OH} = 5.5V				100	μA
V_{OL}	Low-level output voltage		V_{CC} = 4.75V	I_{OL} = 12mA		0.25	0.4	V
			V_I = 0.6V, V_I = 2V	I_{OL} = 24mA		0.35	0.5	V
I_{IH}	High-level input current	A, B	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC} = 5.25V, V_I = 5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current		V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			64	95	mA

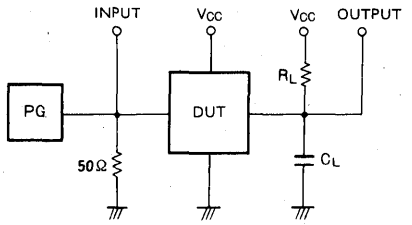
* : All typical values are at V_{CC} = 5V, T_a = 25°C.

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

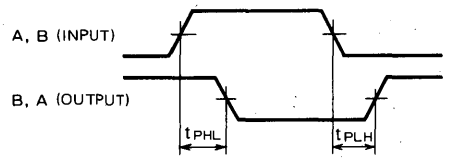
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high level output propagation time	From input A to output B	C_L=45pF, R_L=667Ω (Note 2)		16	25	ns
		From input B to output A			16	25	
t_{PHL}	High-to-low level output propagation time	From input A to output B			14	25	ns
		From input B to output A			14	25	
t_{PLH}	Low-to-high level output propagation time	From input $\overline{OC}$ to output A			25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PHL}	High-to-low level output propagation time	From input $\overline{OC}$ to output A			30	60	ns
		From input $\overline{OC}$ to output B			30	60	

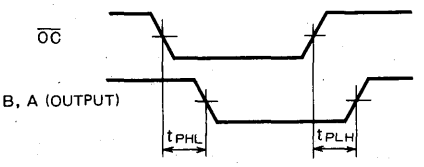
Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)





M74LS642-1P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

DESCRIPTION

The M74LS642-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with open collector inverted outputs.

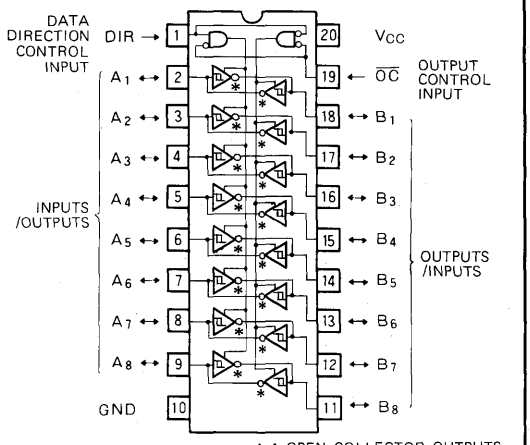
FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Open collector outputs
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 48mA)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

FUNCTIONAL DESCRIPTION

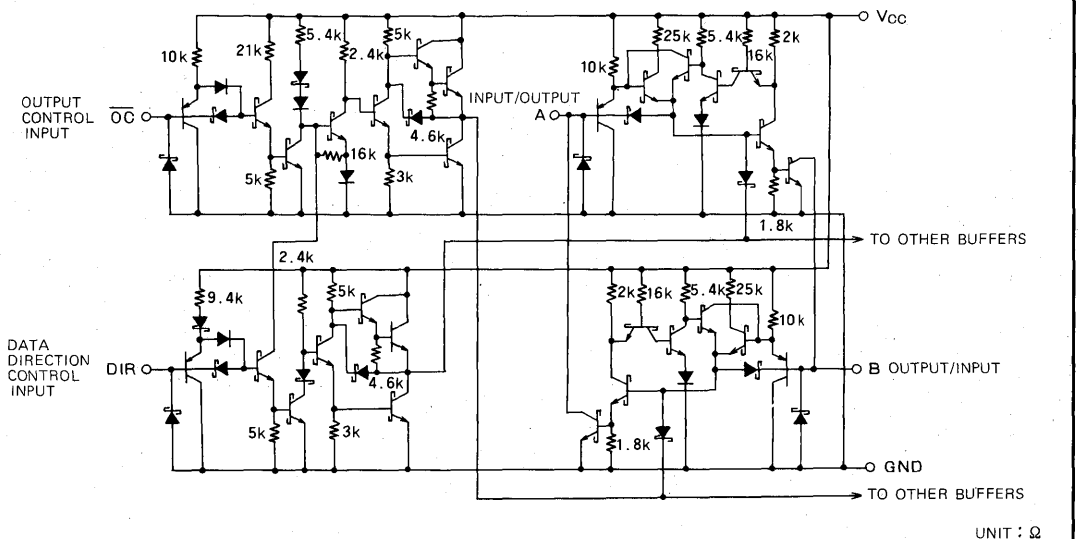
In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with open collector inverted outputs are made two-way buffers.

The input/output A and output/input B sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When $\overline{OC}$ is high, both A and B are high and A and B are isolated.

The functions and pin connections of this device are identical to those of M74LS640-1P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

CIRCUIT DIAGRAM (EACH BUFFER)



OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	$\overline{O}$	I
L	H	I	$\overline{O}$
H	X	H	H

Note 1: I : Input pin
$\overline{O}$: Output (inverted) pin
X : Irrelevant

MAXIMUM ABSOLUTE RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +7	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		High-level state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	℃
Tstg	Storage temperature range			−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O=5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		48	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+}-V_{T-}$	Hysteresis width		V_{CC}=4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
I_{OH}	High-level output current		V_{CC}=4.75V, V_I=0.6V, V_I=2V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.6V, V_I=2V	I_{OL}=12mA		0.25	0.4	V
				I_{OL}=24mA		0.35	0.5	V
				I_{OL}=48mA		0.4	0.5	V
I_{IH}	High-level input current	A, B	V_{CC}=5.25V, V_I=2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC}=5.25V, V_I=5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current		V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.25V, V_I=0V, V_I=4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.25V, V_I=0V, V_I=4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC}=5.25V, V_I=0V, V_I=4.5V			64	95	mA

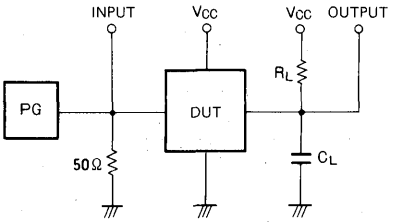
* : All typical values are at V_{CC}=5V, Ta=25℃

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT (INVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

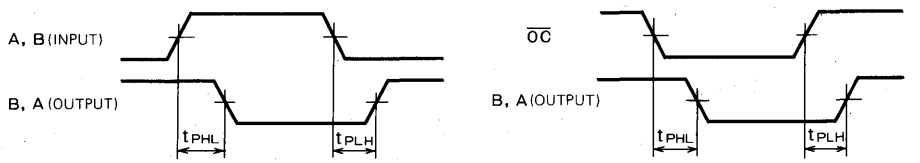
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	From input A to output B	C_L=45pF, R_L=667Ω (Note 2)		16	25	ns
		From input B to output A			16	25	
t_{PHL}	High-to-low level outpout propagation time	From input A to output B			14	25	ns
		From input B to output A			14	25	
t_{PLH}	Low-to-high level output propagation time	From input $\overline{OC}$ to output A			25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PHL}	High-to-low-level output propagation time	From input $\overline{OC}$ to output A			30	60	ns
		From input $\overline{OC}$ to output B			30	60	

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_o = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS643P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS643P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted and non-inverted outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Hysteresis provided (width = 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 24mA, I_{OH} = −15mA)
- Wide operating temperature range. (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

The inputs and outputs of the two buffer circuits with 3-state outputs are connected together to form bi-directional buffers.

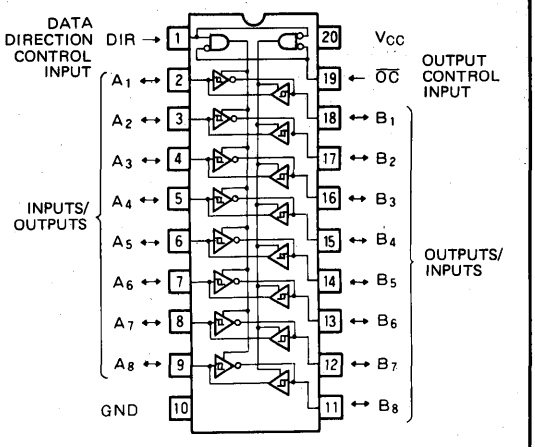
The input sections of input/output A and output/input B have been designed with hysteresis characteristics for increased noise margin. The input/output direction is controlled by DIR.

When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin.

When output control input $\overline{OC}$ is high, both A and B are put in the high-impedance state so the buffers are isolated.

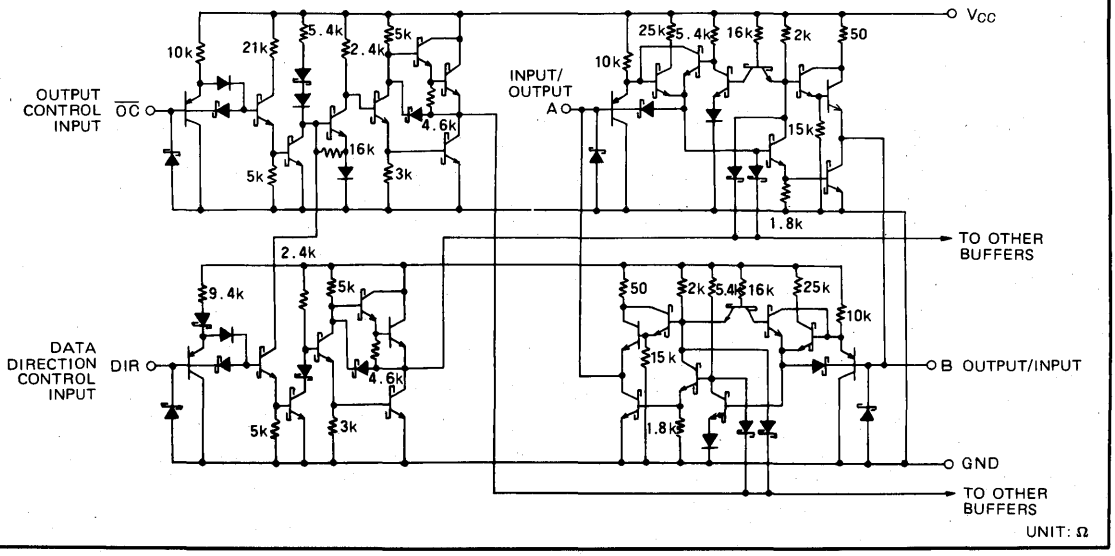
A device, M74LS643-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

CIRCUIT DIAGRAM (Each buffer)



MITSUBISHI ELECTRIC

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	O	I
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1: I: Input pin
O: Output (non-inverted output) pin
$\overline{O}$: Output (inverted output) pin
Z: High impedance (A, B separated)
X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +5.5	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		Off state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

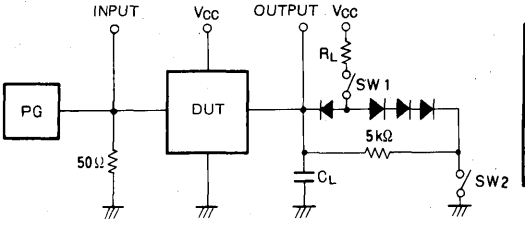
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+} - V_{T-}$	Hysteresis width		V_{CC} = 4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V	I_{OH} = −3 mA	2.4	3.4		V
			V_I = 0.6V, V_I = 2V	I_{OH} = −15mA	2			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V	I_{OL} = 12mA		0.25	0.4	V
			V_I = 0.6V, V_I = 2V	I_{OL} = 24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC} = 5.25V, V_I = 0.6V, V_I = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC} = 5.25V, V_I = 0.6V, V_I = 2V, V_O = 0.4V				−400	μA
I_{IH}	High-level input current	A, B	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC} = 5.25V, V_I = 5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current		V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)		V_{CC} = 5.25V, V_O = 0V		−40		−225	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			64	95	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, Ta = 25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high level output propagation time	From input A to output B	C_L = 45pF (Note 3)		8	10	ns
		From input B to output A			8	10	
t_{PHL}	High-to-low level output propagation time	From input A to output B			12	15	ns
		From input B to output A			12	15	
t_{PZL}	Low output enable time	From input $\overline{OC}$ to output A	R_L = 667Ω C_L = 45pF (Note 3)		25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PZH}	High output enable time	From input $\overline{OC}$ to output A			23	40	ns
		From input $\overline{OC}$ to output B			23	40	
t_{PLZ}	Low output disable time	From input $\overline{OC}$ to output A	R_L = 667Ω C_L = 5pF (Note 3)		17	25	ns
		From input $\overline{OC}$ to output B			17	25	
t_{PHZ}	High output disable time	From input $\overline{OC}$ to output A			19	25	ns
		From input $\overline{OC}$ to output B			19	25	

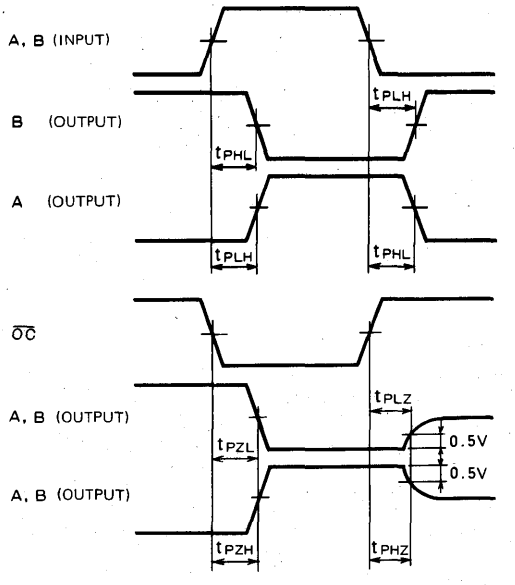
Note 3: Measurement circuit



Parameter	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) All diodes are high speed switching diodes ($t_{rr} \leq 4$ns).
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS643-1P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

DESCRIPTION

The M74LS643-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with inverted and non-inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 48mA, I_{OH} = −15mA)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

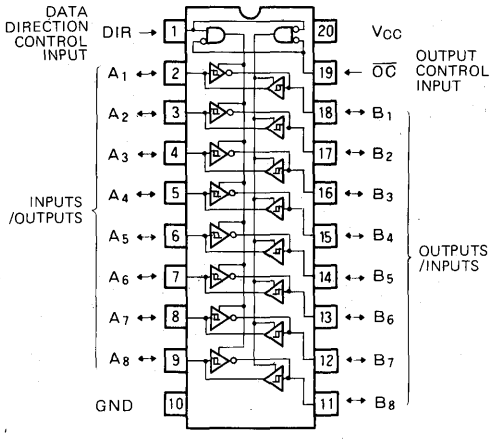
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are mutually connected and the buffers with non-inverted outputs and the buffers with 3-state inverted outputs are made two-way buffers.

The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

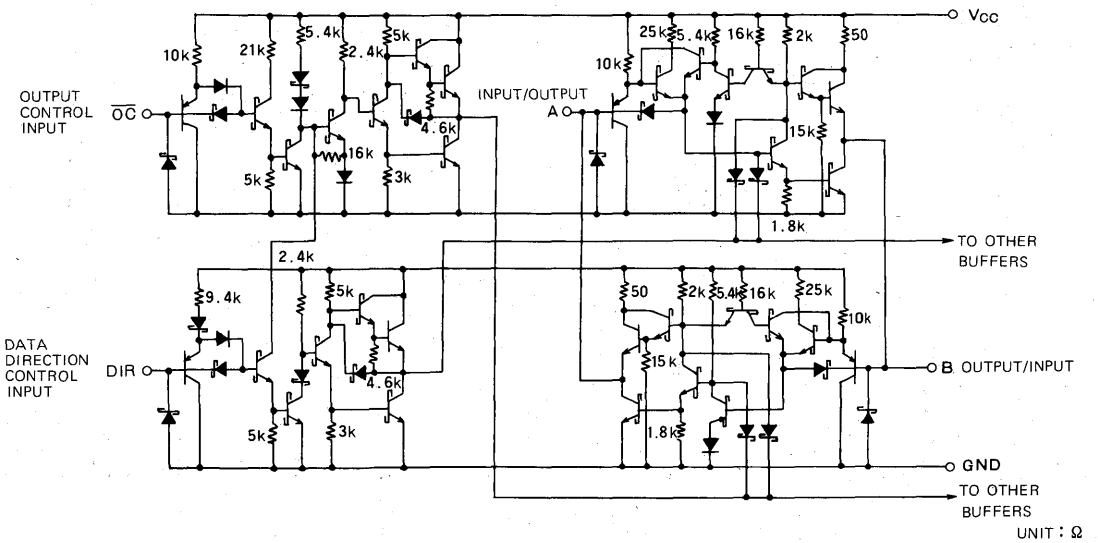
When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When output control input $\overline{OC}$ is high, both A and B are put in the high-impedance state and A and B are isolated.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

CIRCUIT DIAGRAM (EACH BUFFER)



OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	O	I
L	H	I	$\overline{O}$
H	X	Z	Z

Note 1: I : Input pin
O : Output (non-inverted) pin
$\overline{O}$: Output (inverted) pin
Z : High-impedance (A, B are isolated)
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +5.5	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		48	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+} - V_{T-}$	Hysteresis width		V_{CC} = 4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V, V_I = 0.6V, V_I = 2V	I_{OH} = −3mA	2.4	3.4		V
				I_{OH} = −15mA	2			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V, V_I = 0.6V, V_I = 2V	I_{OL} = 12mA		0.25	0.4	V
				I_{OL} = 24mA		0.35	0.5	V
				I_{OL} = 48mA		0.4	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC} = 5.25V, V_I = 0.6V, V_I = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC} = 5.25V, V_I = 0.6V, V_I = 2V, V_O = 0.4V				−400	μA
I_{IH}	High-level input current	A, B	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC} = 5.25V, V_I = 5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current		V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)		V_{CC} = 5.25V, V_O = 0V		−40		−225	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC} = 5.25V, V_I = 0V, V_I = 4.5V			64	95	mA

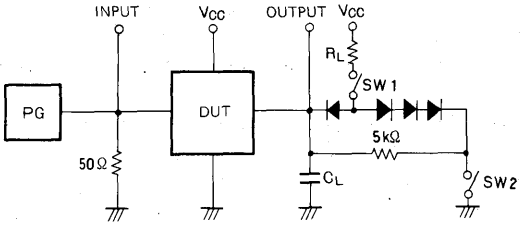
*: All typical values are at V_{CC} = 5V, Ta = 25°C

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	From input A to output B	C_L=45pF (Note 3)		8	10	ns
		From input B to output A			8	10	
t_{PHL}	High-to-low level output propagation time	From input A to output B			12	15	ns
		From input B to output A			12	15	
t_{PZL}	Low-level output enable time	From input $\overline{OC}$ to output A	R_L=667Ω C_L=45pF (Note 3)		25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PZH}	High-level output enable time	From input $\overline{OC}$ to output A			23	40	ns
		From input $\overline{OC}$ to output B			23	40	
t_{PLZ}	Low-level output disable time	From input $\overline{OC}$ to output A	R_L=667Ω C_L=5pF (Note 3)		17	25	ns
		From input $\overline{OC}$ to output B			17	25	
t_{PHZ}	High-level output disable time	From input $\overline{OC}$ to output A			19	25	ns
		From input $\overline{OC}$ to output B			19	25	

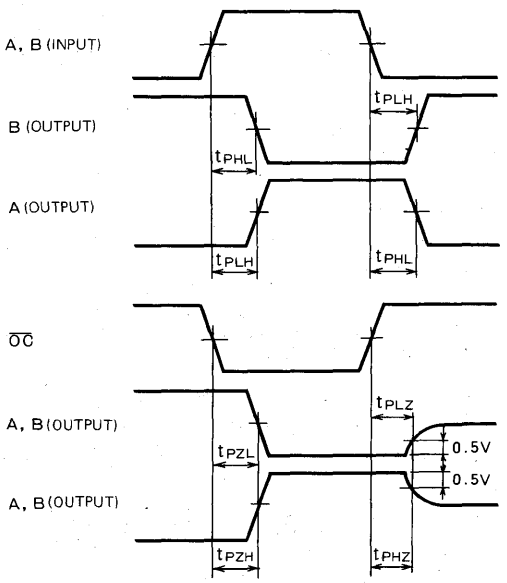
Note 3: Measurement circuit



Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) All diodes are switching diodes ($t_{rr} \lesssim 4$ns).
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS644P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS644P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with inverted, non-inverted open collector outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Open collector outputs
- Hysteresis provided (width = 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 24mA)
- Wide operating temperature range. (T_a = –20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

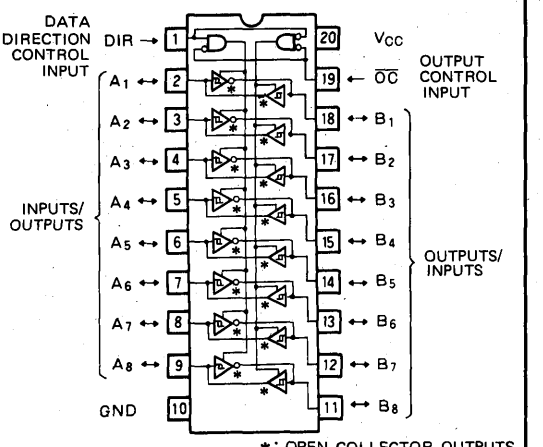
FUNCTIONAL DESCRIPTION

The inputs and outputs of the buffer circuits with open collector outputs are connected together to form bi-directional buffers. The input sections of input/output A and output/input B have been designed with hysteresis characteristics giving increased noise margin. The input/output direction is controlled by DIR.

When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin. When output control input $\overline{OC}$ is high, A and B become high so the buffers are isolated.

Open collector outputs are provided, so the high-level output impedance can be freely selected with external load resistors.

PIN CONFIGURATION (TOP VIEW)

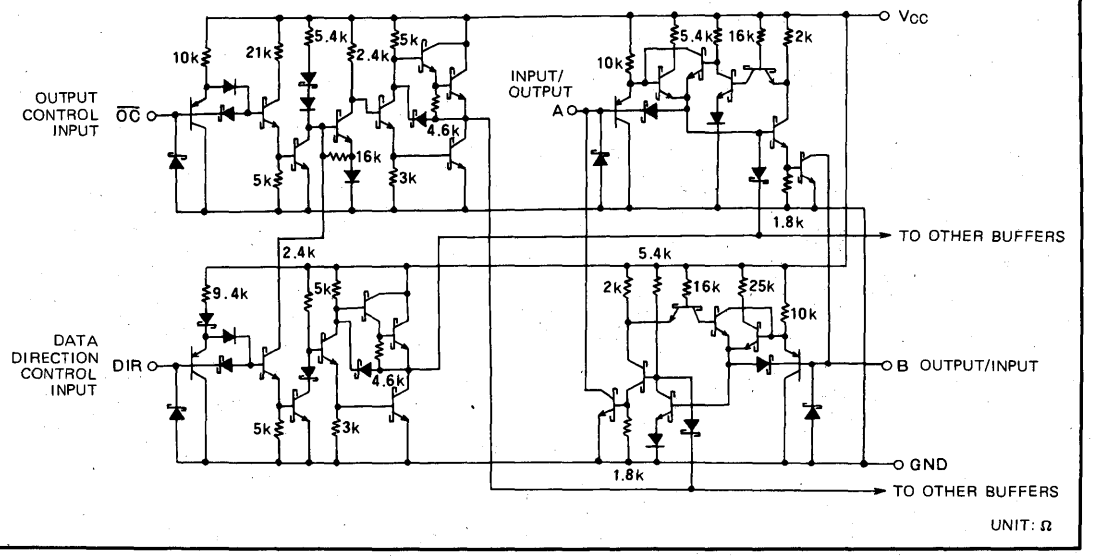


Outline 20P4

The functions and pin connections of this IC are identical to those of M74LS643P.

A device, M74LS644-1P, having the same pin connections and functions except the value of I_{OL} (= 48mA) has been provided.

CIRCUIT DIAGRAM (Each buffer)



MITSUBISHI ELECTRIC

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	O	I
L	H	I	$\overline{O}$
H	X	H	H

Note 1: I: Input pin
O: Output (non-inverted output) pin
$\overline{O}$: Output (inverted output) pin
X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +7	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		High-level state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O=5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75°C, unless otherwise noted)

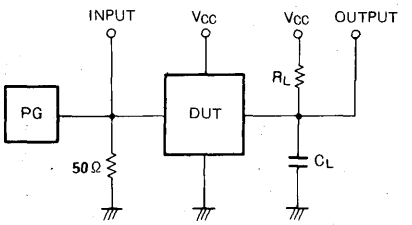
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level output voltage				2			V
V_{IL}	Low-level output voltage						0.6	V
$V_{T+}-V_{T-}$	Hysteresis width		V_{CC}=4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
I_{OH}	High-level output current		V_{CC}=4.75V, V_I=0.6V, V_I=2V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.6V, V_I=2V	I_{OL}=12mA		0.25	0.4	V
				I_{OL}=24mA		0.35	0.5	V
I_{IH}	High-level input current	A, B	V_{CC}=5.25V, V_I=2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC}=5.25V, V_I=5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current		V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.25V, V_I=0V, V_I=4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.25V, V_I=0V, V_I=4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC}=5.25V, V_I=0V, V_I=4.5V			64	95	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

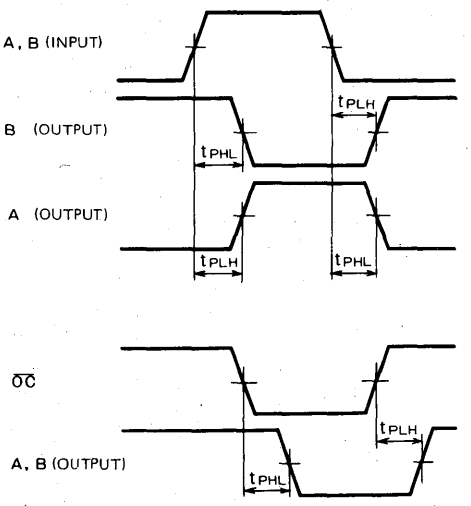
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high level output propagation time	From input A to output B	C_L=45pF, R_L=667Ω (Note 2)		16	25	ns
		From input B to output A			20	25	
t_{PHL}	High-to-low level output propagation time	From input A to output B			14	25	ns
		From input B to output A			15	25	
t_{PLH}	Low-to-high level output propagation time	From input $\overline{OC}$ to output A			25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PHL}	High-to-low level output propagation time	From input $\overline{OC}$ to output A			30	60	ns
		From input $\overline{OC}$ to output B			30	50	

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS644-1P

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS644-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with open collector inverted and non-inverted outputs.

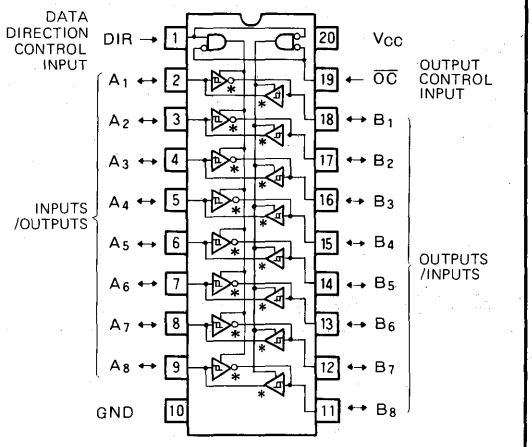
FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Open collector outputs
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 48mA)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

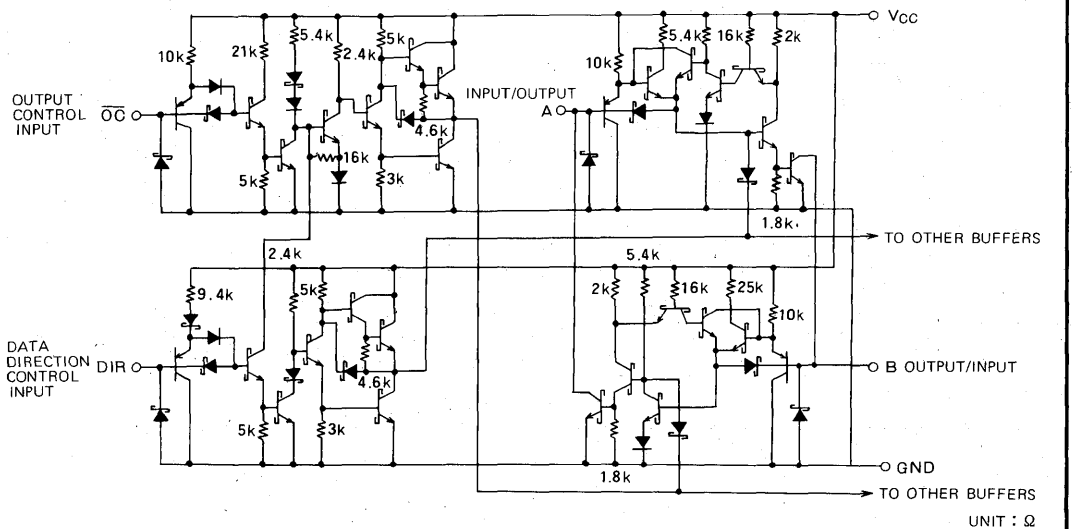
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually and the buffers with open collectors inverted outputs and the buffers with the non-inverted outputs are made two-way buffers. the input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When $\overline{OC}$ is high, both A and B are high, and A and B are isolated.

The functions and pin connections of this device are identical to those of M74LS643-1P but since open collector outputs are provided, the high-level output impedance can be freely selected with an external load resistor.

CIRCUIT DIAGRAM (EACH BUFFER)



UNIT : Ω

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	O	I
L	H	I	$\overline{O}$
H	X	H	H

Note 1: I : Input pin
O : Output (non-inverted) pin
$\overline{O}$: Output (inverted) pin
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +7	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		High-level state	−0.5 ~ +7	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	°C
Tstg	Storage temperature range			−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O=5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		48	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+}-V_{T-}$	Hysteresis width		V_{CC}=4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
I_{OH}	High-level output current		V_{CC}=4.75V, V_I=0.6V, V_I=2V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.6V, V_I=2V	I_{OL}=12mA		0.25	0.4	V
				I_{OL}=24mA		0.35	0.5	V
				I_{OL}=48mA		0.4	0.5	V
I_{IH}	High-level input current	A, B	V_{CC}=5.25V, V_I=2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC}=5.25V, V_I=5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current		V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.25V, V_I=0V, V_I=4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.25V, V_I=0V, V_I=4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC}=5.25V, V_I=0V, V_I=4.5V			64	95	mA

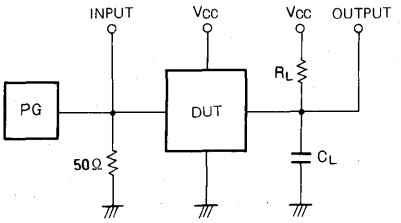
* : All typical values are at V_{CC}=5V, T_a=25°C

OCTAL BUS TRANSCEIVER WITH OPEN COLLECTOR OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

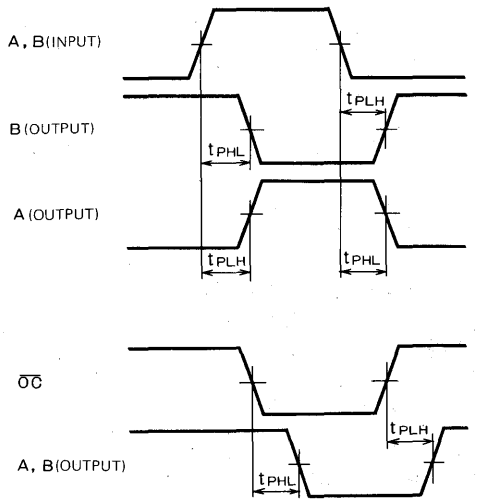
Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	From input A to output B	C_L=45pF, R_L=667Ω (Note 2)		16	25	ns
		From input B to output A			20	25	
t_{PHL}	High-to-low level output propagation time	From input A to output B			14	25	ns
		From input B to output A			15	25	
t_{PLH}	Low-to-high level outpout propagation time	From input $\overline{OC}$ to output A			25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PHL}	High-to-low-level outpout propagation time	From input $\overline{OC}$ to output A			30	60	ns
		From input $\overline{OC}$ to output B			30	50	

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = 3V_{P-P}, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



M74LS645P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74LS645P is a semiconductor integrated circuit containing 8 bus transmitter/receiver circuits with non-inverted outputs.

FEATURES

- Bi-directional transmission or separation of two 8 bit data is possible.
- Hysteresis provided (width = 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 24mA, I_{OH} = –15mA)
- Wide operating temperature range (T_a = –20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

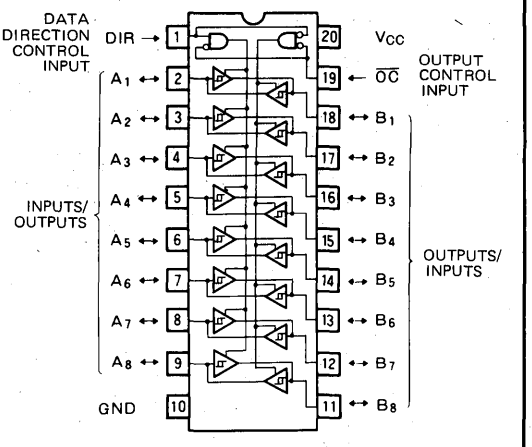
The inputs and outputs of the buffer circuits with 3-state outputs are connected together to form bi-directional buffers.

The input sections of input/output A and output/input B have been designed with hysteresis characteristics for increased noise margin. The input/output direction is controlled by DIR.

When DIR is high then A is the input pin and B is the output pin. When DIR is low then B is input pin and A is the output pin.

When output control input $\overline{OC}$ is high, both A and B are put in the high-impedance state so the buffers are isolated.

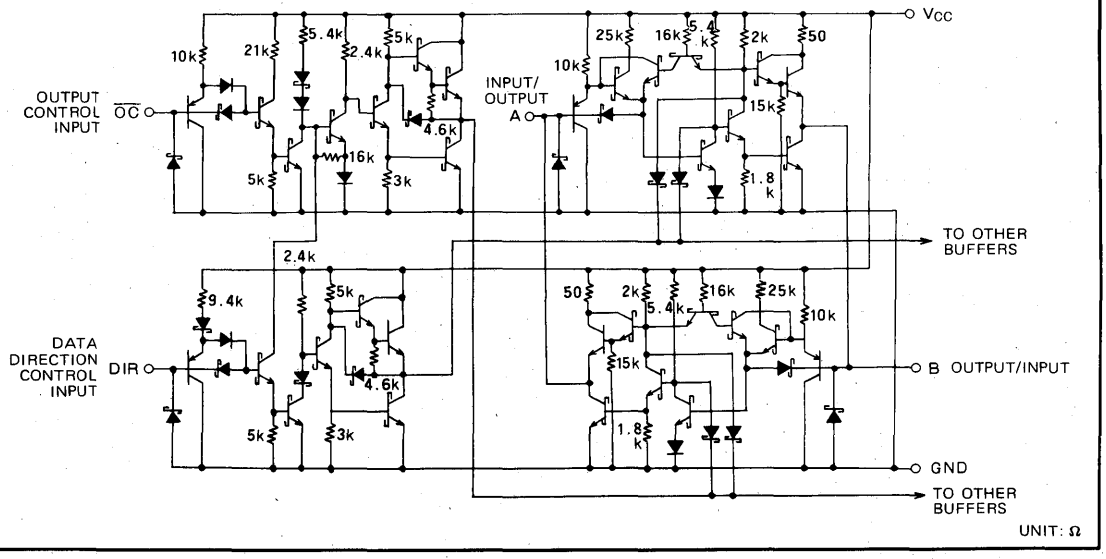
PIN CONFIGURATION (TOP VIEW)



Outline 20P4

A device, M74LS645-1P, having the same pin connections and functions except the value of I_{OL} (=48mA) has been provided.

CIRCUIT DIAGRAM (Each buffer)



MITSUBISHI ELECTRIC

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

Note 1: I: Input pin
O: Output (non-inverted output) pin
Z: High impedance (A, B separated)
X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +5.5	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		Off state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	℃
Tstg	Storage temperature range			−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+} - V_{T-}$	Hysteresis width		V_{CC} = 4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC} = 4.75V, I_{IC} = −18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = 4.75V	I_{OH} = −3mA	2.4	3.4		V
			V_I = 0.6V, V_I = 2V	I_{OH} = −15mA	2			V
V_{OL}	Low-level output voltage		V_{CC} = 4.75V	I_{OL} = 12mA		0.25	0.4	V
			V_I = 0.6V, V_I = 2V	I_{OL} = 24mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC} = 5.25V, V_I = 0.6V, V_I = 2V, V_O = 2.7V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC} = 5.25V, V_I = 0.6V, V_I = 2V, V_O = 0.4V				−400	μA
I_{IH}	High-level input current	A, B	V_{CC} = 5.25V, V_I = 2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC} = 5.25V, V_I = 5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC} = 5.25V, V_I = 10V				0.1	mA
I_{IL}	Low-level input current		V_{CC} = 5.25V, V_I = 0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)		V_{CC} = 5.25V, V_O = 0 V		−40		−225	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5.25V, V_I = 0 V, V_I = 4.5V			48	70	mA
I_{CCL}	Supply current, all outpus low		V_{CC} = 5.25V, V_I = 0 V, V_I = 4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC} = 5.25V, V_I = 0 V, V_I = 4.5V			64	95	mA

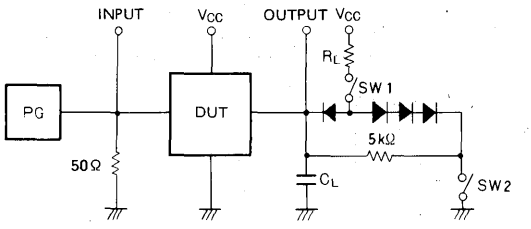
*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high level output propagation time	From input A to output B	C_L=45pF (Note 3)		12	15	ns
		From input B to output A			12	15	
t_{PHL}	High-to-low level output propagation time	From input A to output B			12	15	ns
		From input B to output A			12	15	
t_{PZL}	Low output enable time	From input $\overline{OC}$ to output A	R_L=667Ω, C_L=45pF (Note 3)		25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PZH}	High outputenable time	From input $\overline{OC}$ to output A			23	40	ns
		From input $\overline{OC}$ to output B			23	40	
t_{PLZ}	Low output disable time	From input $\overline{OC}$ to output A	R_L=667Ω, C_L=5pF (Note 3)		17	25	ns
		From input $\overline{OC}$ to output B			17	25	
t_{PHZ}	High output disable time	From input $\overline{OC}$ to output A			19	25	ns
		From input $\overline{OC}$ to output B			19	25	

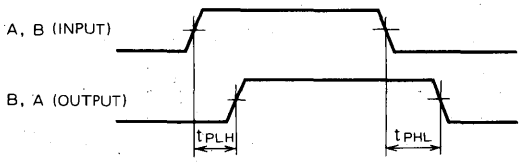
Note 3: Measurement circuit

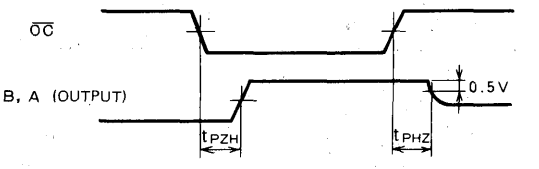


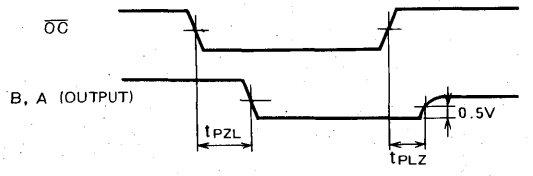
Parameter	SW 1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω
(2) All diodes are high speed switching diodes ($t_{rr} \leqq$ 4ns).
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)







M74LS645-1P

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

DESCRIPTION

The M74LS645-1P is a semiconductor integrated circuit containing 8 bus transmitters/receivers with non-inverted outputs.

FEATURES

- Bi-directional transmission, or separation, of two 8-bit data is possible.
- Hysteresis provided (= 400mV typical) for input/output A and output/input B
- High fan-out (I_{OL} = 48mA, I_{OH} = −15mA)
- Wide operating temperature range (T_a = −20~+75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

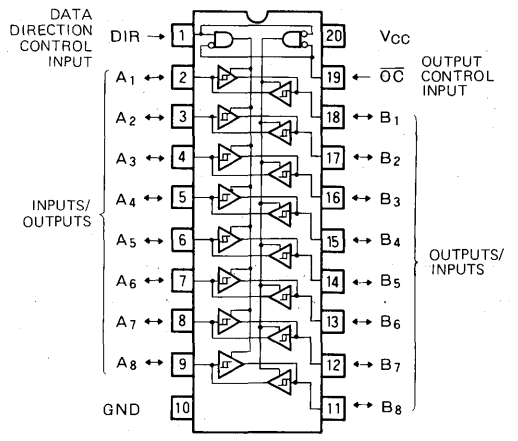
FUNCTIONAL DESCRIPTION

In this device the inputs and outputs are connected mutually to 2 circuits and the buffers with 3-state non-inverted outputs are made two-way buffers.

The input/output A and output/input B input sections are provided with hysteresis for an increased noise margin. The input/output direction is controlled by DIR.

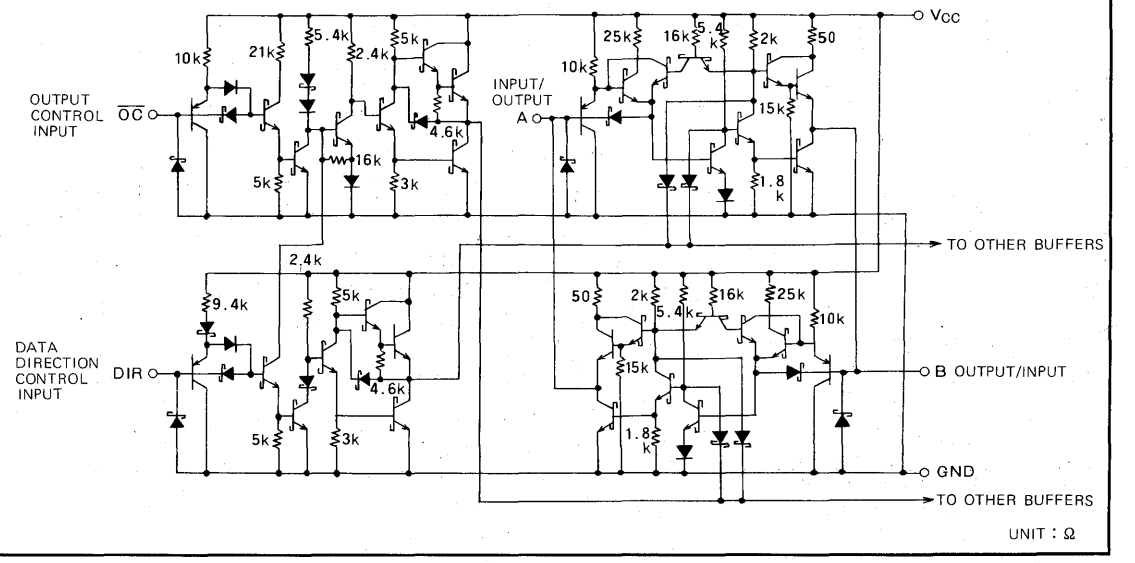
When DIR is high, A is made the input pin and B the output pin. When DIR is low, B is made the input pin and A the output pin. When $\overline{OC}$ is high, both A and B are put in the high-impedance state and A and B are isolated.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4

CIRCUIT DIAGRAM (EACH BUFFER)



UNIT : Ω

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

FUNCTION TABLE (Note 1)

$\overline{OC}$	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

Note 1: I : Input pin
O : Output (non-inverted output) pin
Z : High impedance (A and B are isolated)
X : Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Conditions	Limits	Unit
V_{CC}	Supply voltage			−0.5 ~ +7	V
V_I	Input voltage	A, B		−0.5 ~ +5.5	V
		DIR, $\overline{OC}$		−0.5 ~ +15	V
V_O	Output voltage		Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range			−20 ~ +75	℃
Tstg	Storage temperature range			−65 ~ +150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.4V$	0		−3	mA
		$V_{OH} \geqq 2V$	0		−15	mA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		12	mA
		$V_{OL} \leqq 0.5V$	0		48	mA

ELECTRICAL CHARACTERISTICS (Ta = −20 ~ +75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.6	V
$V_{T+} - V_{T-}$	Hysteresis width		V_{CC}=4.75V		0.2	0.4		V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V	I_{OH}=−3mA	2.4	3.4		V
			V_I=0.6V, V_I=2V	I_{OH}=−15mA	2			V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=12mA		0.25	0.4	V
			V_I=0.6V, V_I=2V	I_{OL}=24mA		0.35	0.5	V
				I_{OL}=48mA		0.4	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.25V, V_I=0.6V, V_I=2V, V_O=2.7V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.25V, V_I=0.6V, V_I=2V, V_O=0.4V				−400	μA
I_{IH}	High-level input current	A, B	V_{CC}=5.25V, V_I=2.7V				20	μA
		DIR, $\overline{OC}$					20	μA
		A, B	V_{CC}=5.25V, V_I=5.5V				0.1	mA
		DIR, $\overline{OC}$	V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current		V_{CC}=5.25V, V_I=0.4V				−0.4	mA
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−40		−225	mA
I_{CCH}	Supply current, all outputs high		V_{CC}=5.25V, V_I=0V, V_I=4.5V			48	70	mA
I_{CCL}	Supply current, all outputs low		V_{CC}=5.25V, V_I=0V, V_I=4.5V			62	90	mA
I_{CCZ}	Supply current, all outputs off		V_{CC}=5.25V, V_I=0V, V_I=4.5V			64	95	mA

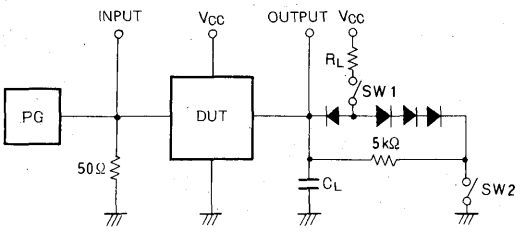
* : All typical values are at V_{CC}=5V, Ta=25℃
Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

OCTAL BUS TRANSCEIVER WITH 3-STATE OUTPUT (NONINVERTED)

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
t_{PLH}	Low-to-high-level output propagation time	From input A to output B	C_L=45pF (Note 3)		12	15	ns
		From input B to output A			12	15	
t_{PHL}	High-to-low level output propagation time	From input A to output B			12	15	ns
		From input B to output A			12	15	
t_{PZL}	Low-level output enable time	From input $\overline{OC}$ to output A	R_L=667Ω, C_L=45pF (Note 3)		25	40	ns
		From input $\overline{OC}$ to output B			25	40	
t_{PZH}	High-level output enable time	From input $\overline{OC}$ to output A			23	40	ns
		From input $\overline{OC}$ to output B			23	40	
t_{PLZ}	Low-level output disable time	From input $\overline{OC}$ to output A	R_L=667Ω, C_L=5pF (Note 3)		17	25	ns
		From input $\overline{OC}$ to output B			17	25	
t_{PHZ}	High-level outpout disable time	From input $\overline{OC}$ to output A			19	25	ns
		From input $\overline{OC}$ to output B			19	25	

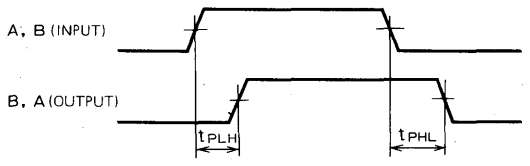
Note 3: Measurement circuit

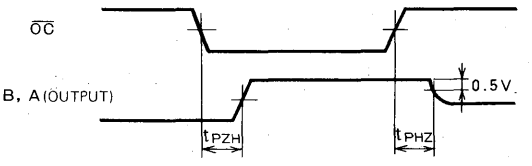


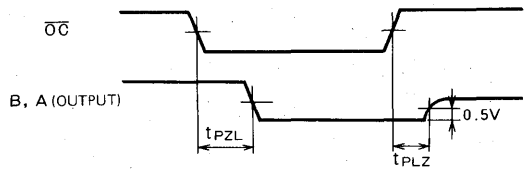
Symbol	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns,
V_P = 3V_{P-P}, Z_O = 50Ω.
(2) All diodes are switching diodes ($t_{rr} \leqq$ 4ns)
(3) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)







M74LS668P

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

DESCRIPTION

The M74LS668P is a semiconductor integrated circuit containing a synchronous decade counter function with an up/down control input and preset input.

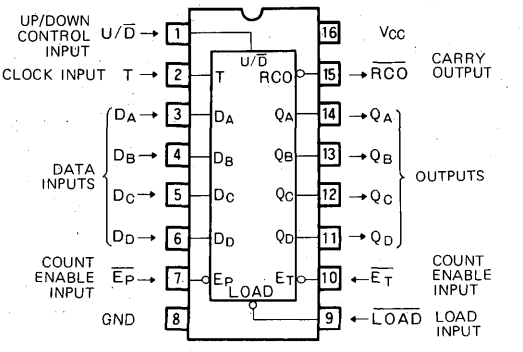
FEATURES

- Fully synchronous operation for counting and programming
- Integral look-ahead for counting
- Carry output for n bit cascading
- Fully independent clock circuit
- Up/down control input provided
- Preset input provided

APPLICATION

General purpose, for use in industrial and consumer equipment

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

This device operates with the preset, up/down control and enable function synchronized to the rising edge of the clock pulse.

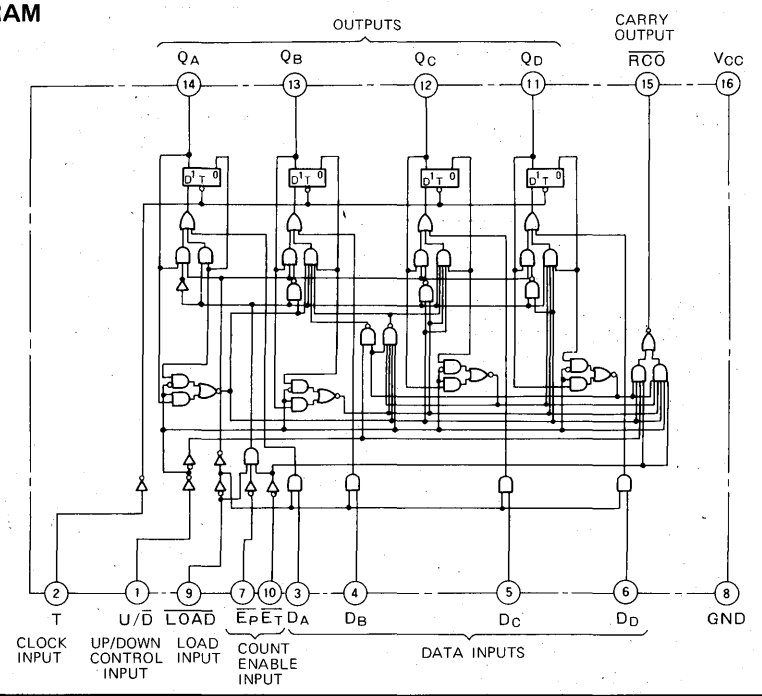
Data is also acquisitioned from outputs Q_A thru Q_D on the rising edge of clock input T, synchronized with (and in response to) data input at D_A thru D_D; and occurs after preset is initiated by dropping load input ($\overline{LOAD}$) to a low-level.

Up/down counter operations are initiated when $\overline{LOAD}$ is high-level, and the count enable input ($\overline{E_P}$ and $\overline{E_T}$) is low-level. The counter increments (up) when control input U/$\overline{D}$ is high-level, and decrements (down) at low-level.

Carry output ($\overline{RCO}$) goes low-level (active) at 9_2 during up counting operations and at 0_2 while the count is going down. The synchronous feature of the counter permits it to be cascaded for use as a decade counter. (See the application example provided in the back of this specification sheet.)

Counter operations are inhibited when $\overline{LOAD}$ and ($\overline{E_P}$ or $\overline{E_T}$) are all high-level.

BLOCK DIAGRAM



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SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

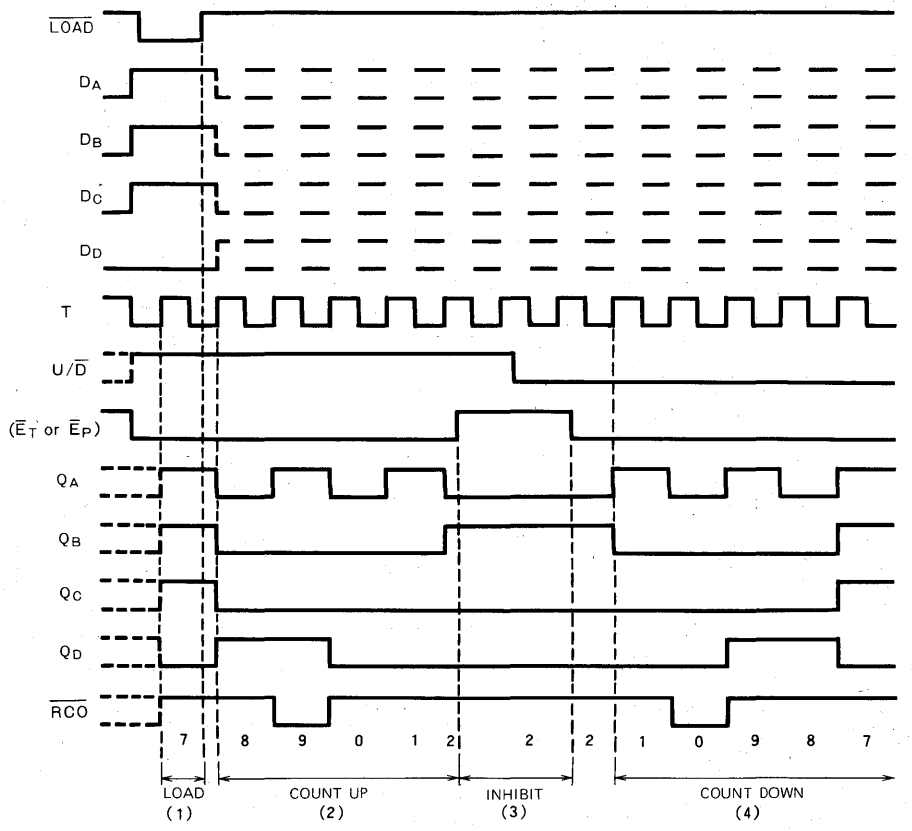
FUNCTION TABLE (Note 1)

$\overline{LOAD}$	$\overline{E_P}$	$\overline{E_T}$	U/$\overline{D}$	T	Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$*
L	X	X	X	↑	D_A	D_B	D_C	D_D	H
H	L	L	H	↑	COUNT UP				H
H	L	L	L	↑	COUNT DOWN				H
H	H	X	X	X	COUNT INHIBIT				H
H	X	H	X	X					

Note 1. ↑ : Transition from low to high
X : Irrelevant
* : $\overline{RCO}$ is normally at high-level, however, when $\overline{E_T}$ is low and the counter is incrementing, Q_A is high-level, Q_B is center-level, Q_C is low-level, and Q_D is high-level, and $\overline{RCO}$ will go low-level. Also, when the counter is decrementing, Q_A, Q_B, Q_C and Q_D will be low, and $\overline{RCO}$ will also be low.

$$\overline{RCO} = Q_A \cdot Q_D \cdot (U/\overline{D}) \cdot \overline{E_T}$$
$$\overline{RCO} = \overline{Q}_A \cdot \overline{Q}_B \cdot \overline{Q}_C \cdot \overline{Q}_D \cdot (\overline{U/D}) \cdot \overline{E_T}$$

TIMING DIAGRAM



Timing diagram notes:
(1) Preset at 7
(2) Increment at 8, 9, 0, 1, 2
(3) Count inhibit
(4) Decrement at 1, 0, 9, 8, 7

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

ABSOLUTE MAXIMUM RATINGS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7$	V
V_I	Input voltage*		$-0.5 \sim +15$	V
V_O	Output voltage	High-level state	$-0.5 \sim V_{CC}$	V
T_{opr}	Operating free-air ambient temperature range		$-20 \sim +75$	°C
T_{stg}	Storage temperature range		$-65 \sim +150$	°C

RECOMMENDED OPERATING CONDITIONS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		-400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				-1.5	V
V_{OH}	*High-level output voltage*		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$T, \overline{E_T}$					20	
		$\overline{LOAD}$					40	
		$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$T, \overline{E_T}$					0.1	
		$\overline{LOAD}$					0.2	
I_{IL}	Low-level input current	$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$	$V_{CC}=5.25V$, $V_I=0.4V$				-0.4	mA
		$T, \overline{E_T}$					-0.4	
		$\overline{LOAD}$					-0.8	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		-20		-100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 3)			20	34	mA

* : All typical values are at $V_{CC} = 5V$, $T_a = 25°C$.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

3. I_{CC} is measured after applying a momentary 4.5V, then ground, to clock input with other inputs grounded and the outputs open.

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

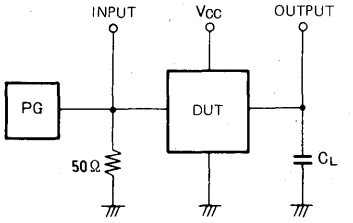
SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
fmax	Maximum clock frequency	C_L=15pF (Note 4)	25	45		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output $\overline{RCO}$			24	40	ns
t_{PHL}				30	60	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_A, Q_B, Q_C, and Q_D			18	27	ns
t_{PHL}				15	27	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E_T}$ to output $\overline{RCO}$			10	17	ns
t_{PHL}				24	45	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input U/$\overline{D}$ to output $\overline{RCO}$			20	35	ns
t_{PHL}				20	40	

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_w	Clock T pulse width		25	10		ns
$t_{su(D)}$	Setup time D_A~D_D to T		20	18		ns
$t_{su(\overline{E})}$	Setup time $\overline{E_T}$, $\overline{E_P}$ to T		35	26		ns
$t_{su(\overline{LOAD})}$	Setup time $\overline{LOAD}$ to T		25	15		ns
$t_{su(U/\overline{D})}$	Setup time U/$\overline{D}$ to T		30	20		ns
t_h	Setup time of all inputs to T		0	−15		ns

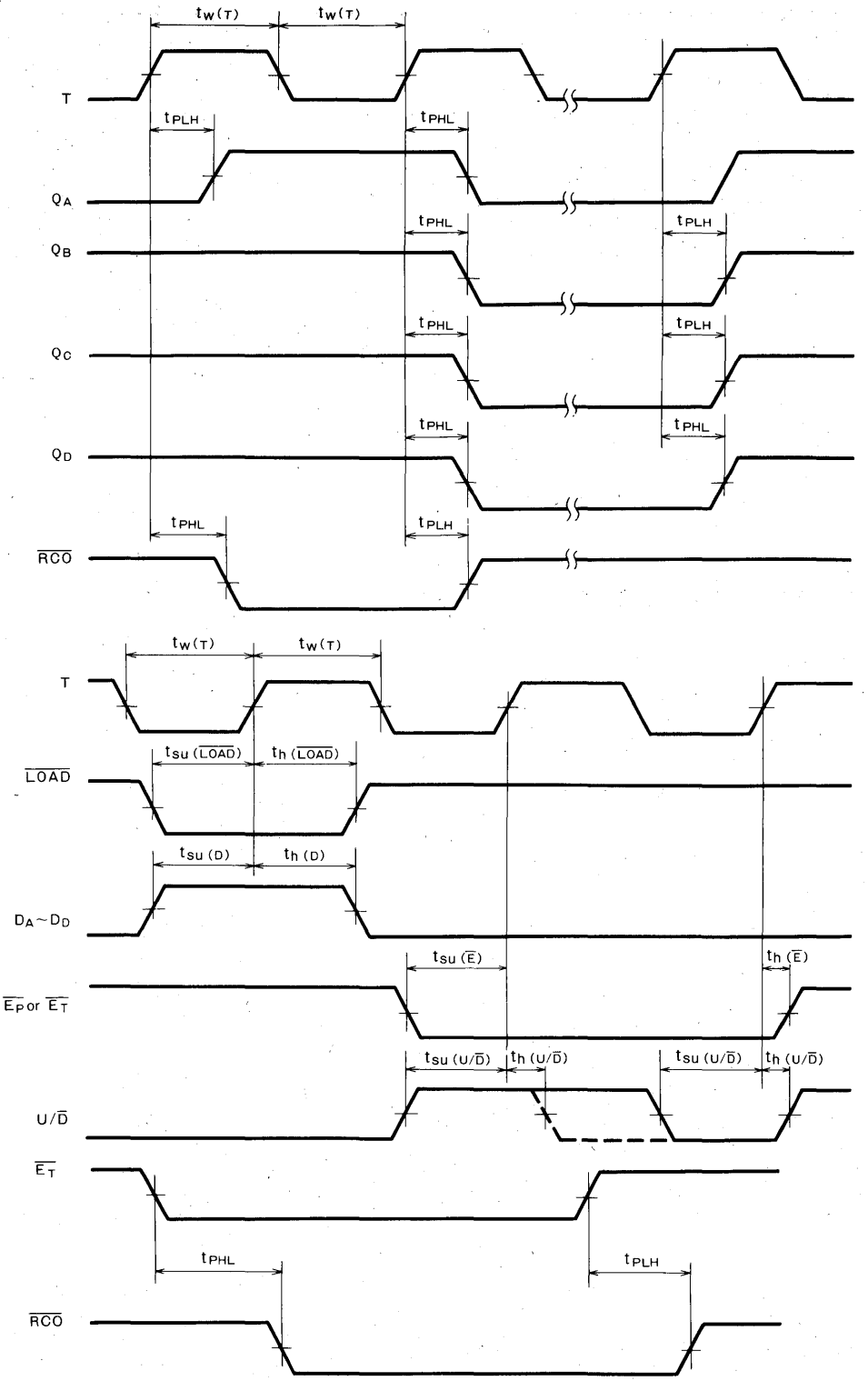
Note 4. Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

TIMING DIAGRAM (Reference level = 1.3V)



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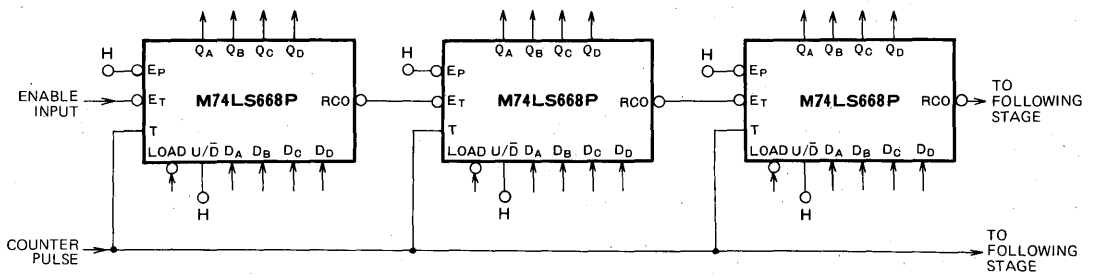
SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER

APPLICATION EXAMPLE

10^n counter with cascade connection



M74LS669P

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

DESCRIPTION

The M74LS669P is a semiconductor integrated circuit containing a synchronous 4-bit binary counter function with an up/down control input and preset input.

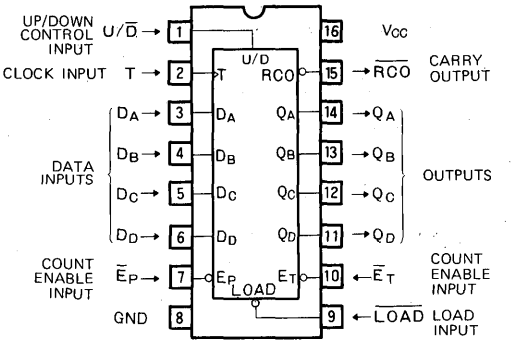
FEATURES

- Fully synchronous operation for counting and programming
- Integral look-ahead for counting
- Carry output for n bit cascading
- Fully independent clock circuit
- Up/down control input provided
- Preset input provided

APPLICATION

General purpose, for use in industrial and consumer equipment

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTIONAL DESCRIPTION

This device operates with the preset, up/down control and enable function synchronized to the rising edge of the clock pulse.

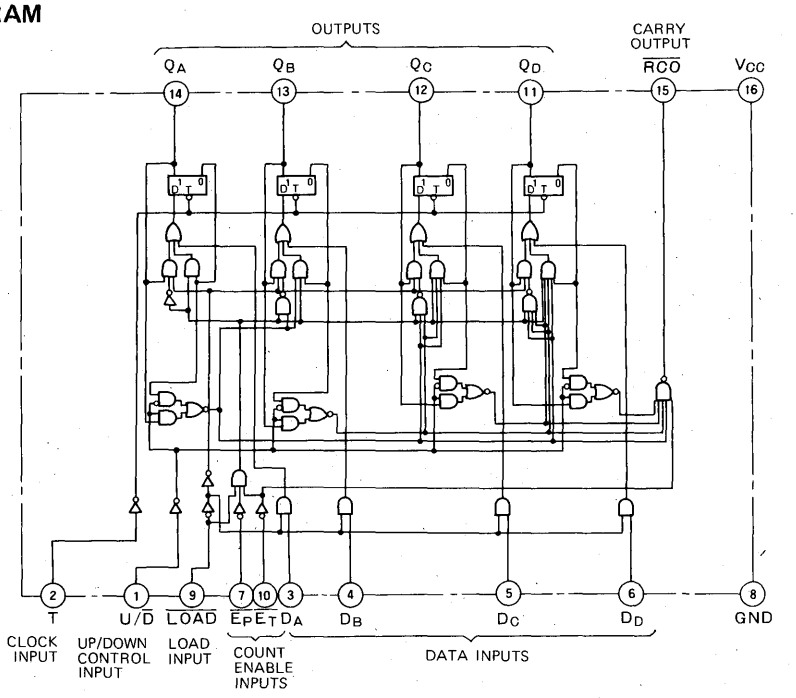
Data is acquisitioned from outputs Q_A thru Q_D on the rising edge of clock input T, synchronized with (and in response to) data input at D_A thru D_D; and occurs after preset is initiated by dropping load input ($\overline{LOAD}$) to a low-level.

Up/down counter operations are initiated when $\overline{LOAD}$ is high-level, and the count enable input ($\overline{E_P}$ and $\overline{E_T}$) is low-level. The counter increments (up) when control input U/$\overline{D}$ is high-level, and decrements (down) at low-level.

Carry output ($\overline{RCO}$) goes low-level (active) at 15_2 during up operations, and at 0_2 while the count is going down. The synchronous feature of the counter permits it to be cascaded for use as a binary counter. (See the application example given for M74LS668P.)

Counter operations are inhibited when $\overline{LOAD}$ and ($\overline{E_P}$ or $\overline{E_T}$) are all high-level.

BLOCK DIAGRAM



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SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

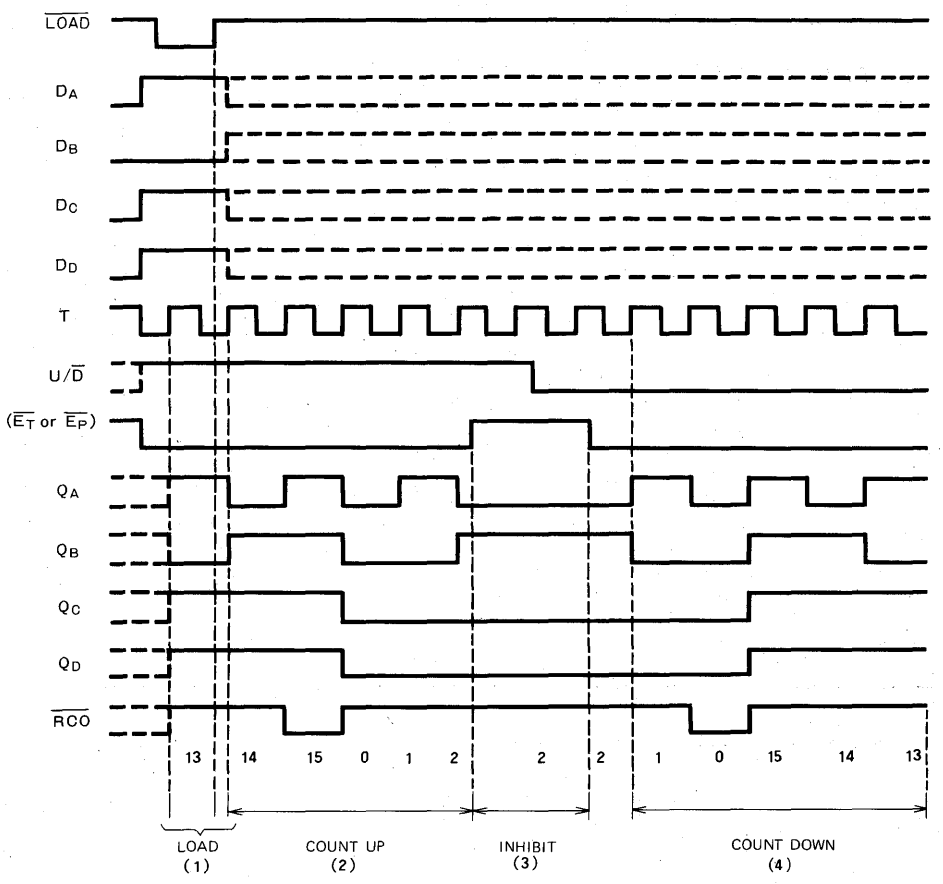
FUNCTION TABLE (Note 1)

$\overline{LOAD}$	$\overline{E_P}$	$\overline{E_T}$	$U/\overline{D}$	T	Q_A	Q_B	Q_C	Q_D	$\overline{RCO}$*
L	X	X	X	↑	D_A	D_B	D_C	D_D	H
H	L	L	H	↑	COUNT UP				H
H	L	L	L	↑	COUNT DOWN				H
H	H	X	X	X	COUNT INHIBIT				H
H	X	H	X	X					

Note 1. ↑ : Transition from low to high
X : Irrelevant
* : $\overline{RCO}$ is normally at high-level, however, when $\overline{E_T}$ is low and the counter is incrementing, Q_A, Q_B, Q_C and Q_D will be high, and $\overline{RCO}$ will be low. Also, when the counter is decrementing, Q_A, Q_B, Q_C and Q_D will be low, and $\overline{RCO}$ will also be low.

$$\overline{RCO} = Q_A \cdot Q_B \cdot Q_C \cdot Q_D \cdot (U/\overline{D}) \cdot \overline{E_T}$$
$$\overline{RCO} = \overline{Q}_A \cdot \overline{Q}_B \cdot \overline{Q}_C \cdot \overline{Q}_D (U/\overline{D}) \cdot \overline{E_T}$$

TIMING DIAGRAM



Timing diagram notes:
(1) Preset at 13
(2) Increment at 14, 15, 0, 1, 2
(3) Count inhibit
(4) Decrement at 1, 0, 15, 14, 13

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V V_I=2V, I_{OH}=−400μA		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
			V_I=0.8V, V_I=2V	I_{OL}=8mA		0.35	0.5	V
I_{IH}	High-level input current	$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$	V_{CC}=5.25V, V_I=2.7V				20	μA
		$T, \overline{E_T}$					20	
		$\overline{LOAD}$					40	
		$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$	V_{CC}=5.25V, V_I=10V				0.1	mA
		$T, \overline{E_T}$					0.1	
		$\overline{LOAD}$					0.2	
I_{IL}	Low-level input current	$D_A, D_B, D_C, D_D, \overline{E_P}, U/\overline{D}$	V_{CC}=5.25V, V_I=0.4V				−0.4	mA
		$T, \overline{E_T}$					−0.4	
		$\overline{LOAD}$					−0.8	
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 3)			20	34	mA

* All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2. All measurements should be done quickly, and not more than one output should be shorted at a time.

3. I_{CC} is measured after applying a momentary 4.5V, then ground, to the clock input with all other inputs grounded.

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

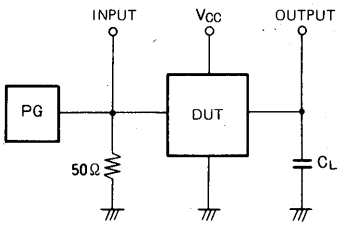
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency	C_L=15pF (Note 4)	25	30		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output $\overline{RCO}$			24	40	ns
t_{PHL}				32	60	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_A, Q_B, Q_C, and Q_D			20	27	ns
t_{PHL}				15	27	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E_T}$ to output $\overline{RCO}$			10	17	ns
t_{PHL}				28	45	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input U/$\overline{D}$ to output $\overline{RCO}$			25	35	ns
t_{PHL}				20	40	

TIMING REQUIREMENTS (V_{CC}=5V, T_a=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_w	Clock T pulse width		25	12		ns
$t_{su\,(D)}$	Setup time D_A~D_D to T		20	18		ns
$t_{su\,(E)}$	Setup time $\overline{E_T}$, $\overline{E_P}$ to T		35	26		ns
$t_{su\,(\overline{LOAD})}$	Setup time $\overline{LOAD}$ to T		25	15		ns
$t_{su\,(U/\overline{D})}$	Setup time U/$\overline{D}$ to T		30	20		ns
t_h	Setup time of all inputs to T		0	−15		ns

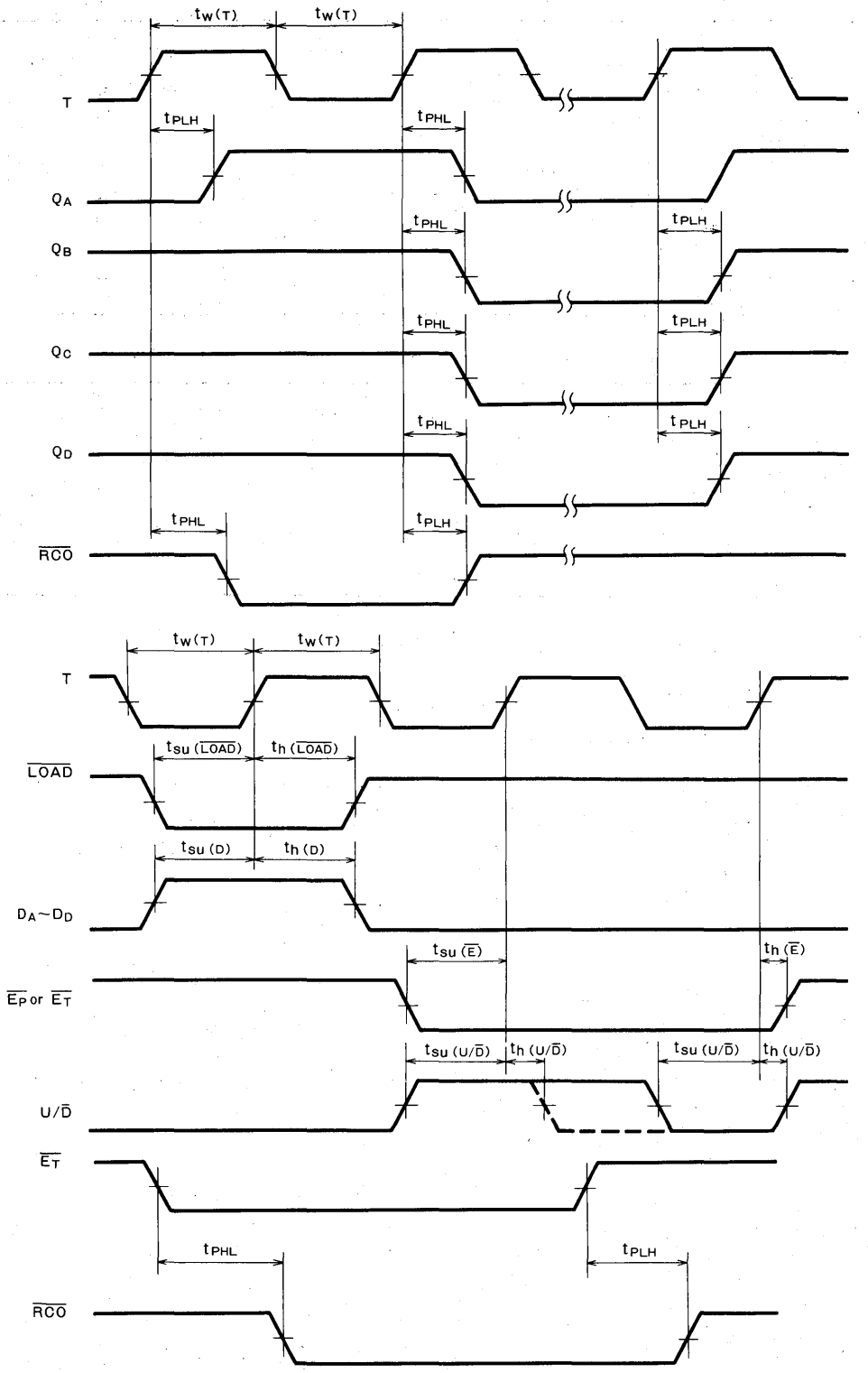
Note 4. Measurement Circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω.
(2) C_L includes probe and jig capacitance.

SYNCHRONOUS PRESETTABLE UP/DOWN 4-BIT BINARY COUNTER

TIMING DIAGRAM (Reference level = 1.3V)



MITSUBISHI ELECTRIC

M74LS670P

4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

DESCRIPTION

The M74LS670P is a semiconductor integrated circuit containing a 4 word x 4 bit register file circuit with 3-state outputs.

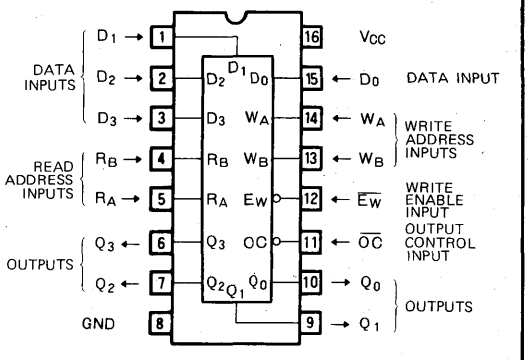
FEATURES

- Since read address and write address are independent, simultaneous writing and reading of data is possible.
- Provided with read enable input and output control inputs
- Storage capacity can be easily expanded with the aid of the enable input.
- AND-tie may be used (With 3-state output)
  Wide operating temperature range (T_a = -20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 16 P4

FUNCTIONAL DESCRIPTION

16 flip-flops are used as storage devices, and a discrete enable input, address input, and output controlling input are provided for reading and writing. Accordingly, during writing, the contents of other words can be read, and during reading, other words can be written, thereby enhansing to high-speed operation.

The 3-state output permits 128-output AND-tie even in the worst condition. Expansion of up to 512 words is possible. possible.

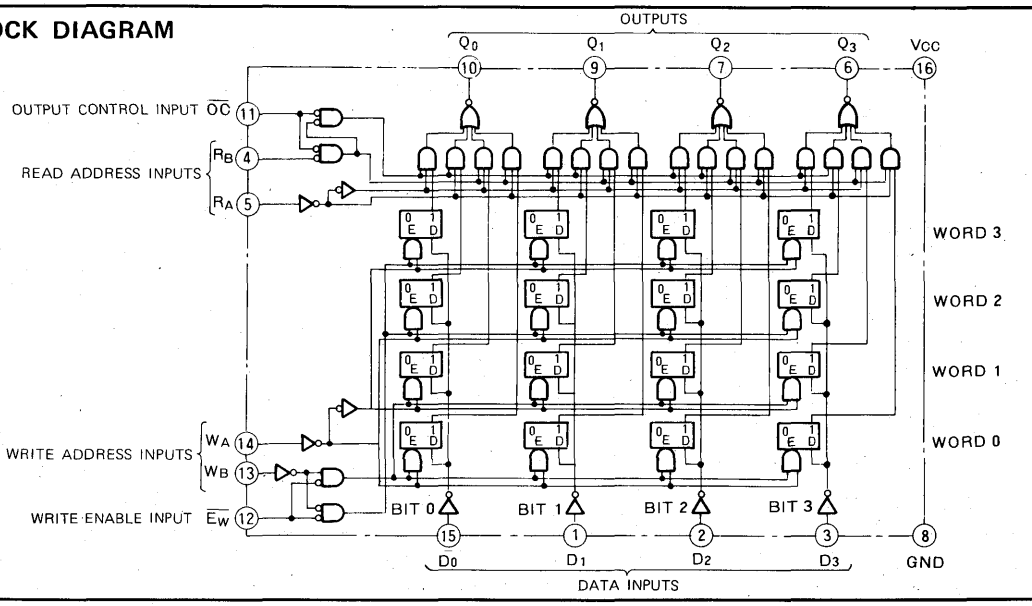
Writing Method

By designating a word using write address inputs W_A and W_B and applying data to the data inputs D_0, D_1, D_2, and D_3, writing into each bit is performed. For writing the write enable input $\overline{E_W}$ is held low (Writing will not be performed if $\overline{E_W}$ is high)

Readout Method

When a word is designated by read address inputs R_A and R_B, the contents of each bit appear in the outputs Q_0, Q_1, Q_2, and Q_3. For reading the output control input $\overline{OC}$ is held low. (when $\overline{OC}$ is high, all the outputs are in the high-impedance state).

BLOCK DIAGRAM



4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

FUNCTION TABLE (Note 1)

Writing Method

W_A	W_B	$\overline{E_W}$	Word 0	Word 1	Word 2	Word 3
X	X	H	Q^0	Q^0	Q^0	Q^0
L	L	L	Q=D	Q^0	Q^0	Q^0
H	L	L	Q^0	Q=D	Q^0	Q^0
L	H	L	Q^0	Q^0	Q=D	Q^0
H	H	L	Q^0	Q^0	Q^0	Q=D

Readout Method

R_A	R_B	$\overline{OC}$	Q_0	Q_1	Q_2	Q_3
X	X	H	Z	Z	Z	Z
L	L	L	W_0B_0	W_0B_1	W_0B_2	W_0B_3
H	L	L	W_1B_0	W_1B_1	W_1B_2	W_1B_3
L	H	L	W_2B_0	W_2B_1	W_2B_2	W_2B_3
H	H	L	W_3B_0	W_3B_1	W_3B_2	W_3B_3

Note 1: Q^0 : The level of Q before the indicated steady-state input conditions were established.

Q=D : The four selected internal latch outputs will assume the states applied to the four external data inputs.

W_XB_Y : The Yth bit of word X. X : irrelevant Z : high-impedance

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C,)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	Off-state	−0.5 ~ +5.5	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_{OH}≧2.4V	0		−2.6	mA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		4	mA
		V_{OL}≦0.5V	0		8	mA

ELECTRICAL CHARACTERISTICS (T_a = −20 ~ +70°C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min	Limits Typ*	Limits Max	Unit
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V, I_{OH}=−2.6mA		2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=0.8V, V_I=2V	I_{OL}=4mA		0.25	0.4	V
				I_{OL}=8mA		0.35	0.5	V
I_{OZH}	Off-state high-level output current		V_{CC}=5.25V, V_I=2V, V_I=2.7V				20	μA
I_{OZL}	Off-state low-level output current		V_{CC}=5.25V, V_I=2V, V_I=0.4V				−20	μA
I_{IH}	High-level input current	$\overline{E_W}$	V_{CC}=5.25V, V_I=2.7V				40	μA
		$\overline{OC}$					60	
		Other input					20	
		$\overline{E_W}$	V_{CC}=5.25V, V_I=10V				0.2	mA
		$\overline{OC}$					0.3	
		Other input					0.1	
I_{IL}	Low-level input current	$\overline{E_W}$	V_{CC}=5.25V, V_I=0.4V				−0.8	mA
		$\overline{OC}$					−1.2	
		Other input					−0.4	
I_{OS}	Short-circuit output current (Note 2)		V_{CC}=5.25V, V_O=0V		−30		−130	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 3)			30	50	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.

Note 2: All measurements should be done quickly, and not more than one output should be shorted at a time.

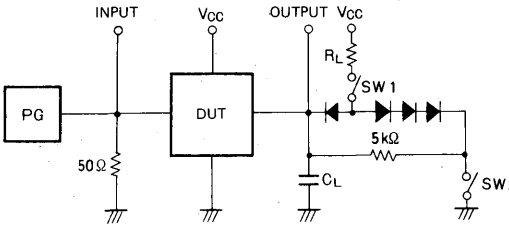
3: Icc is measured with W_A, W_B, R_A, R_B inputs grounded and D_0 ~ D_3, $\overline{E_W}$, $\overline{OC}$ inputs at 4.5V.

4-BY-4 REGISTER FILE WITH 3-STATE OUTPUTS

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input R_A, R_B to output Q_0, Q_1, Q_2, Q_3	C_L=15pF (Note 4)		11	40	ns
t_{PHL}				14	45	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E_W}$ to output Q_0, Q_1, Q_2, Q_3			11	45	ns
t_{PHL}				16	50	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input D_0, D_1, D_2, D_3 to output Q_0, Q_1, Q_2, Q_3			9	45	ns
t_{PHL}				14	40	ns
t_{PZH}	Output enable time to high-level	R_L=2kΩ, C_L=15pF (Note 4)		6	35	ns
t_{PZL}	Output enable time to low-level	R_L=2kΩ, C_L=15pF (Note 4)		10	40	ns
t_{PHZ}	Output disable time from high-level	R_L=2kΩ, C_L=5pF (Note 4)		16	50	ns
t_{PLZ}	Output disable time from low-level	R_L=2kΩ, C_L=5pF (Note 4)		7	35	ns

Note 4: Measurement circuit



Symbol	SW 1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

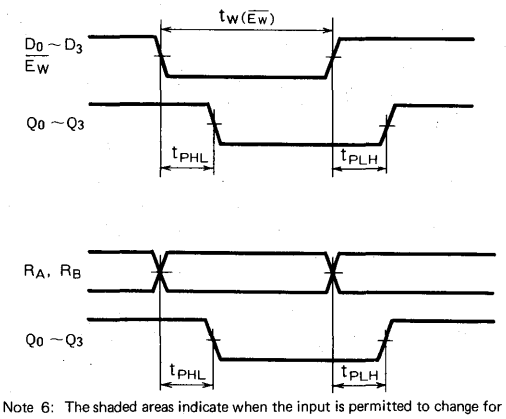
(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P\text{-}P}$, Z_O = 50Ω
(2) All diodes are switching diodes ($t_{rr} \leqq 4$ns)
(3) C_L includes probe and jig capacitance.

TIMING REQUIREMENTS (V_{CC}=5V, Ta=25°C, unless otherwise noted)

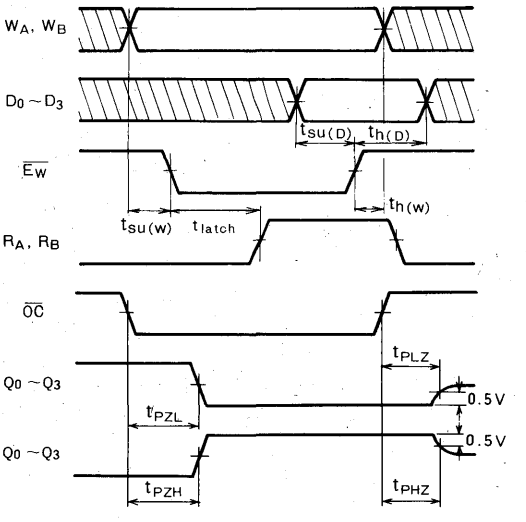
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{E_W})}$	Write enable input $\overline{E_W}$ pulse width		25	9		ns
$t_{W(\overline{OC})}$	Output control input $\overline{OC}$ pulse width		25	9		ns
$t_{SU(D)}$	Setup time D_0~D_3 to $\overline{E_W}$		10	5		ns
$t_{SU(W)}$	Setup time W_A, W_B to $\overline{E_W}$		15	−2		ns
$t_{h(D)}$	Hold time D_0~D_3 to $\overline{E_W}$		15	1		ns
$t_{h(W)}$	Hold time W_A, W_B to $\overline{E_W}$		5	0		ns
t_{latch}	Latch time for new date (Note 5)		25	5		ns

Note 5: Latch time is the time allowed for the internal output of the latch to assume the state of new data.

TIMING DIAGRAM (Reference level = 1.3V)



Note 6: The shaded areas indicate when the input is permitted to change for predictable output performance.



NEW PRODUCT

M74LS682P

8-BIT MAGNITUDE COMPARATOR

DESCRIPTION

The M74LS682P is a semiconductor integrated circuit containing two 8-bit words comparator functions.

FEATURES

- Hysteresis at inputs (width = 400mV typical)
- Internal 24kΩ pull-up resistors on the Q inputs
- Active pull-up outputs
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

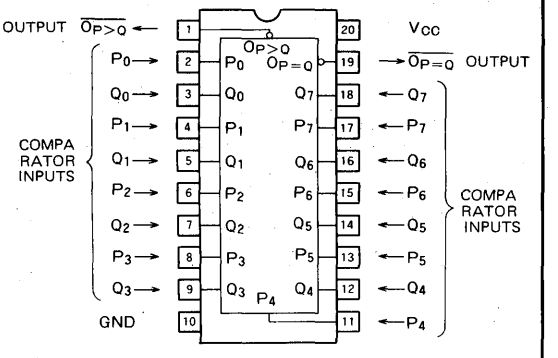
Two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

$Q_0 \sim Q_7$ have internal pull-up resistors (=24kΩ), so that misoperation due to noise is reduced on condition that $Q_0 \sim Q_7$ are open.

Beside the IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application.

PIN CONFIGURATION (TOP VIEW)

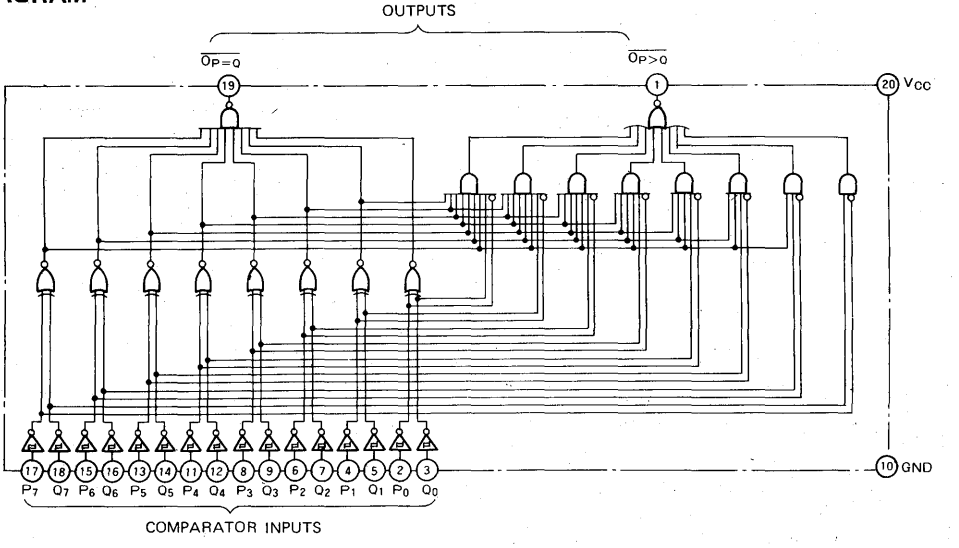


Outline 20P4

8-BIT MAGNITUDE COMPARATORS TABLE

Type designation	Inputs		Outputs		
	Q 24kΩ pull-up	$\overline{E}$	$\overline{O_{P=Q}}$	$\overline{O_{P>Q}}$	Format
M74LS682P	Yes	No	Yes	Yes	Active pull-up
M74LS683P	Yes	No	Yes	Yes	Open collector
M74LS684P	No	No	Yes	Yes	Active pull-up
M74LS685P	No	No	Yes	Yes	Open collector
M74LS688P	No	Yes	Yes	No	Active pull-up
M74LS689P	No	Yes	Yes	No	Open collector

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

8-BIT MAGNITUDE COMPARATOR

FUNCTION TABLE

P, Q	$\overline{O_{P=Q}}$	$\overline{O_{P>Q}}$
P=Q	L	H
P>Q	H	L
P<Q	H	H

ABSOLUTE MAXIMUM RATINGS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage	Inputs P	−0.5∼+15	V
		Inputs Q	−0.5∼V_{CC}+0.5	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
Topr	Operating free-air ambient temperature range		−20∼+75	℃
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_{OH}≧2.7V	0		−400	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta=−20∼+75℃, unless otherwise noted)

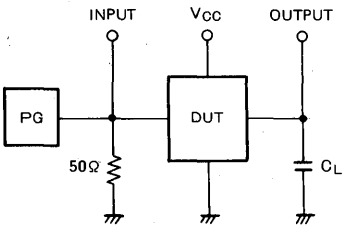
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
$V_{T+}-V_{T-}$	Hysteresis width		V_{CC}=4.75V			0.4		V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC}=4.75V, V_I=2V, V_I=0.8V, I_{OH}=−400μA		2.7			V
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=2V, V_I=0.8V	I_{OL}=12mA		0.25	0.4	V
				I_{OL}=24mA		0.35	0.5	V
I_{IH}	High-level input current	P, Q	V_{CC}=5.25V, V_I=2.7V				20	μA
		P	V_{CC}=5.25V, V_I=10V				0.1	mA
		Q	V_{CC}=5.25V, V_I=5.5V					
I_{IL}	Low-level input current	P	V_{CC}=5.25V, V_I=0.4V				−0.2	mA
		Q					−0.4	mA
I_{OS}	Short-circuit output current (Note 1)		V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 2)			42	70	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.
2: I_{CC} is measured with all inputs at value of 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

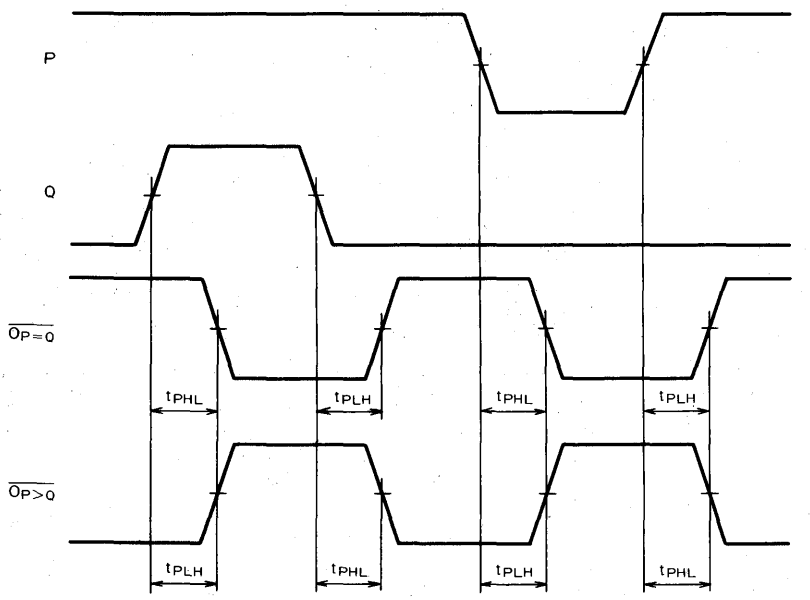
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs P to output $\overline{O_{P=Q}}$	C_L=45pF (Note 3) All other input pins in low-state		13	30	ns
t_{PHL}				16	30	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs Q to output $\overline{O_{P=Q}}$			12	30	ns
t_{PHL}				17	30	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs P to output $\overline{O_{P>Q}}$			24	30	ns
t_{PHL}				21	30	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs Q to output $\overline{O_{P>Q}}$			26	30	ns
t_{PHL}				27	30	

Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

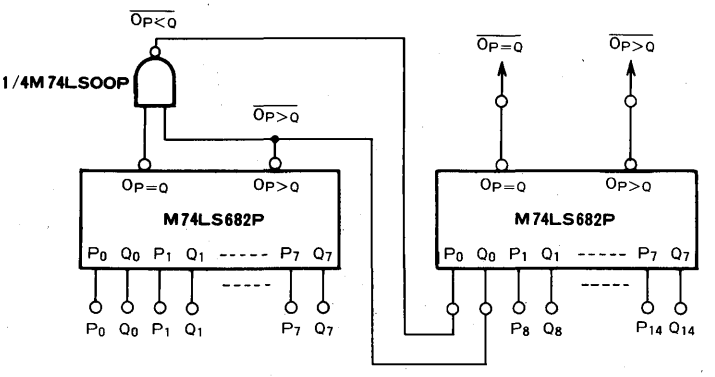
TIMING DIAGRAM (Reference level = 1.3V)



MITSUBISHI ELECTRIC

APPLICATION EXAMPLE

Example of 15-bit comparator



NEW PRODUCT

MITSUBISHI LSTTLs

M74LS683P

8-BIT MAGNITUDE COMPARATOR WITH OPEN COLLECTOR OUTPUT

DESCRIPITON

The M74LS683P is a semiconductor integrated circuit containing two 8-bit words comparator functions with open collector outputs.

FEATURES

- Hysteresis at inputs (width = 400mV typical)
- Internal 24kΩ pull-up resistors on the Q inputs
- Open collector outputs
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

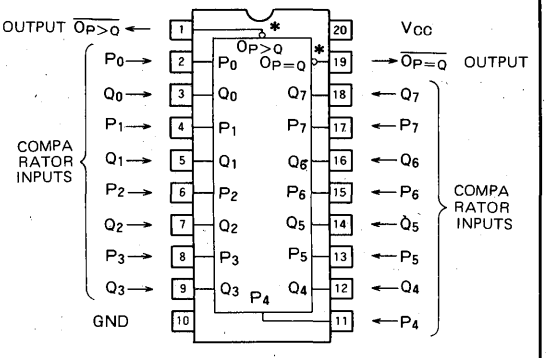
Two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

$Q_0 \sim Q_7$ have internal pull-up resistors (=24kΩ), so that misoperation due to noise is reduced on condition that $Q_0 \sim Q_7$ are open.

Beside this IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application of M74LS682P.

PIN CONFIGURATION (TOP VIEW)



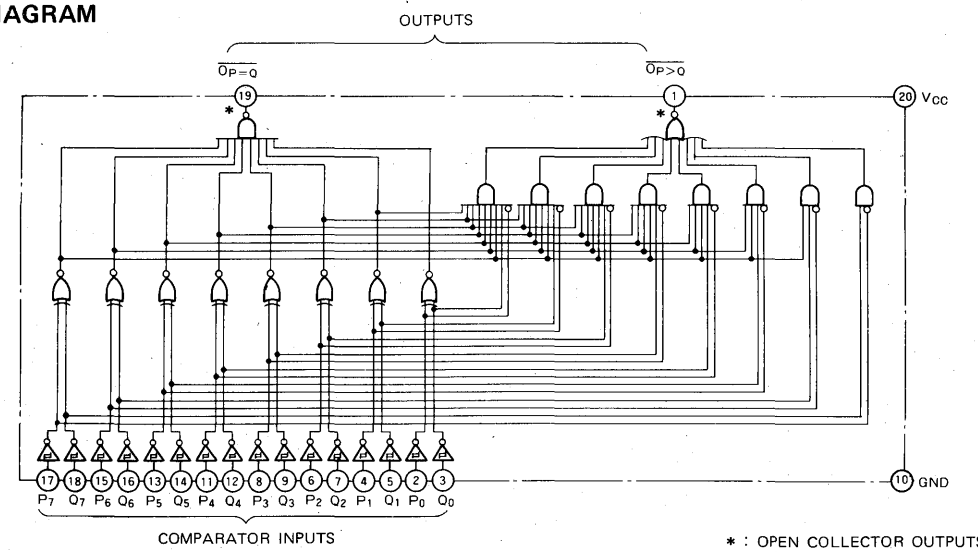
* : OPEN COLLECTOR OUTPUTS

Outline 20P4

8-BIT MAGNITUDE COMPARATORS TABLE

Type designation	Inputs		Outputs		
	Q 24kΩ pull-up	$\overline{E}$	$\overline{O_{P=Q}}$	$\overline{O_{P>Q}}$	Format
M74LS682P	Yes	No	Yes	Yes	Active pull-up
M74LS683P	Yes	No	Yes	Yes	Open collector
M74LS684P	No	No	Yes	Yes	Active pull-up
M74LS685P	No	No	Yes	Yes	Open collector
M74LS688P	No	Yes	Yes	No	Active pull-up
M74LS689P	No	Yes	Yes	No	Open collector

BLOCK DIAGRAM



* : OPEN COLLECTOR OUTPUTS

MITSUBISHI ELECTRIC

8-BIT MAGNITUDE COMPARATOR WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE

P, Q	$\overline{O_{P=Q}}$	$\overline{O_{P>Q}}$
P=Q	L	H
P>Q	H	L
P<Q	H	H

ABSOLUTE MAXIMUM RATINGS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage	Inputs P	−0.5∼+15	V
		Inputs Q	−0.5∼V_{CC}+0.5	V
V_O	Output voltage	High-level state	−0.5∼+7	V
Topr	Operating free-air ambient temperature range		−20∼+75	℃
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O=5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
$V_{T+}-V_{T-}$	Hysteresis width		V_{CC}=4.75V			0.4		V
V_{IC}	Input clamp voltage		V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
I_{OH}	High-level output current		V_{CC}=4.75V, V_I=2V, V_I=0.8V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage		V_{CC}=4.75V, V_I=2V or V_I=0.8V	I_{OL}=12mA		0.25	0.4	V
				I_{OL}=24mA		0.35	0.5	V
I_{IH}	High-level input current	P, Q	V_{CC}=5.25V, V_I=2.7V				20	μA
		P	V_{CC}=5.25V, V_I=10V				0.1	mA
		Q	V_{CC}=5.25V, V_I=5.5V					
I_{IL}	Low-level input current	P	V_{CC}=5.25V, V_I=0.4V				−0.2	mA
		Q					−0.4	mA
I_{CC}	Supply current		V_{CC}=5.25V (Note 1)			42	70	mA

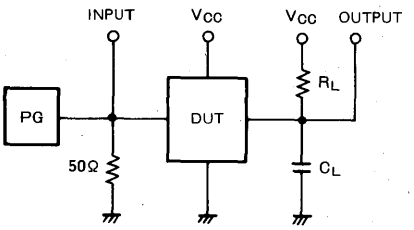
*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 1: I_{CC} is measured with all inputs at value of 4.5V.

8-BIT MAGNITUDE COMPARATOR WITH OPEN COLLECTOR OUTPUT

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

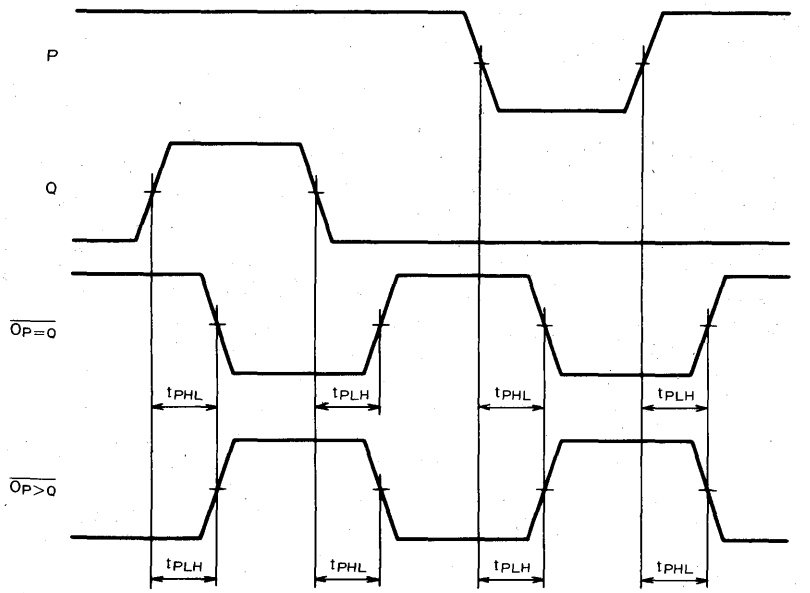
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs P to output $\overline{O_{P=Q}}$	R_L=667Ω, C_L=45pF (Note 2) All other input pins in low-state.		23	45	ns
t_{PHL}				20	30	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs Q to output $\overline{O_{P=Q}}$			21	40	ns
t_{PHL}				20	35	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs P to output $\overline{O_{P>Q}}$			26	45	ns
t_{PHL}				22	30	
t_{PLH}	Low-to-high level high-to-low level output propagation time from inputs Q to output $\overline{O_{P>Q}}$			28	45	ns
t_{PHL}				26	30	

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_w = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



MITSUBISHI ELECTRIC

NEW PRODUCT

M74LS684P

8-BIT MAGNITUDE COMPARATOR

DESCRIPTION

The M74LS684P is a semiconductor integrated circuit containing two 8-bit words comparator functions.

FEATURES

- Hysteresis at inputs (width = 400mV typical)
- Active pull-up outputs.
- Wide operating temperature range (T_a = −20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

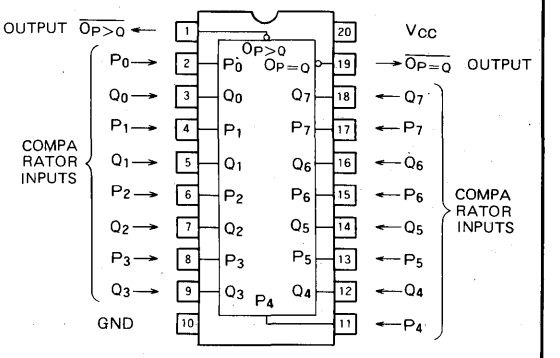
Two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

Note that this IC, in comparison to M74LS682P, does not have internal pull-up resistors on its inputs $Q_0 \sim Q_7$.

Beside this IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application of M74LS682P.

PIN CONFIGURATION (TOP VIEW)

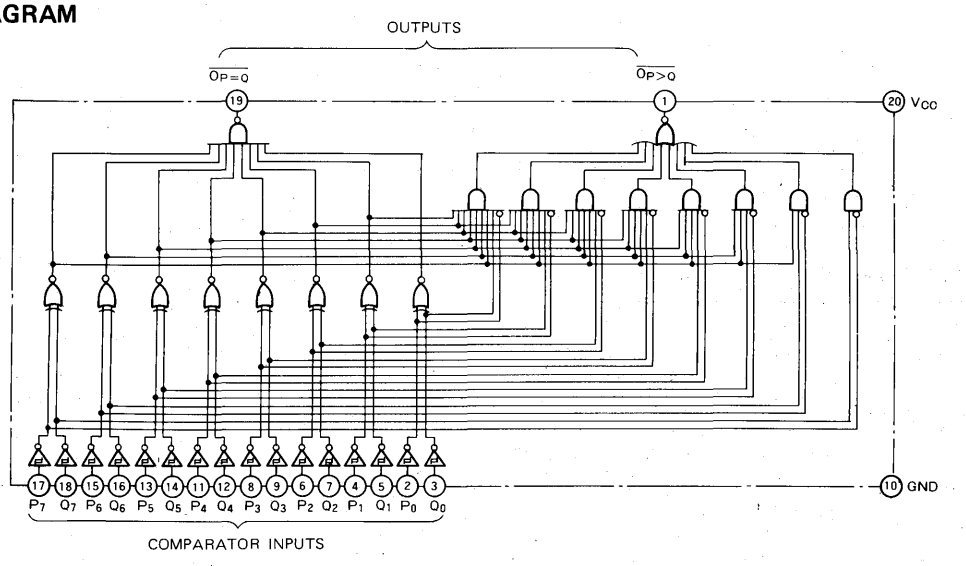


Outline 20P4

8-BIT MAGNITUDE COMPARATORS TABLE

Type designation	Inputs		Outputs		
	Q 24kΩ pull-up	$\overline{E}$	$\overline{O_{P=Q}}$	$\overline{O_{P>Q}}$	Format
M74LS682P	Yes	No	Yes	Yes	Active pull-up
M74LS683P	Yes	No	Yes	Yes	Open collector
M74LS684P	No	No	Yes	Yes	Active pull-up
M74LS685P	No	No	Yes	Yes	Open collector
M74LS688P	No	Yes	Yes	No	Active pull-up
M74LS689P	No	Yes	Yes	No	Open collector

BLOCK DIAGRAM



8-BIT MAGNITUDE COMPARATOR

FUNCTION TABLE

P, Q	$\overline{O_{P=Q}}$	$\overline{O_{P>Q}}$
P=Q	L	H
P>Q	H	L
P<Q	H	H

ABSOLUTE MAXIMUM RATINGS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+15	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
T_{opr}	Operating free-air ambient temperature range		−20∼+75	℃
T_{stg}	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_{OH}≧2.7V	0		−400	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta=−20∼+75℃, unless otherwise noted)

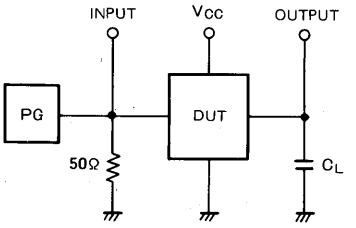
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
$V_{T+}-V_{T-}$	Hysteresis width	V_{CC}=4.75V			0.4		V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=2V, V_I=0.8V, I_{OH}=−400μA		2.7			V
V_{OL}	Low-level output voltage	V_{CC}=4.75V, V_I=2V, V_I=0.8V	I_{OL}=12mA		0.25	0.4	V
			I_{OL}=24mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.2	mA
I_{OS}	Short-circuit output current (Note 1)	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 2)			40	65	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 1: All measurements should be done quickly, and not more than one output should be shorted at a time.
2: I_{CC} is measured with all inputs at value of 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

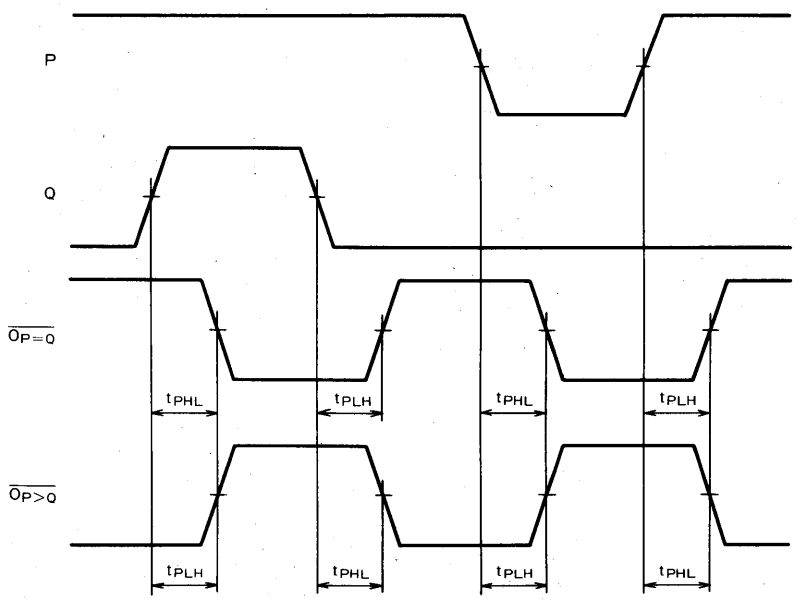
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs P to output $\overline{O_{P=Q}}$	C_L=45pF (Note 3), All other input pins in low-state		13	30	ns
t_{PHL}				16	30	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs Q to output $\overline{O_{P=Q}}$			12	30	ns
t_{PHL}				17	30	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs P to output $\overline{O_{P>Q}}$			24	30	ns
t_{PHL}				21	30	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs Q to output $\overline{O_{P>Q}}$			26	30	ns
t_{PHL}				27	30	

Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



NEW PRODUCT

M74LS685P

8-BIT MAGNITUDE COMPARATOR WITH OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS685P is a semiconductor integrated circuit containing two 8-bit words comparator functions with open collector outputs.

FEATURES

- Hysteresis at inputs (width = 400mW typical)
- Open collector outputs
- Wide operating temperature range (T_a = –20 ~ +75°C)

APPLICATION

General purpose, for use in for industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

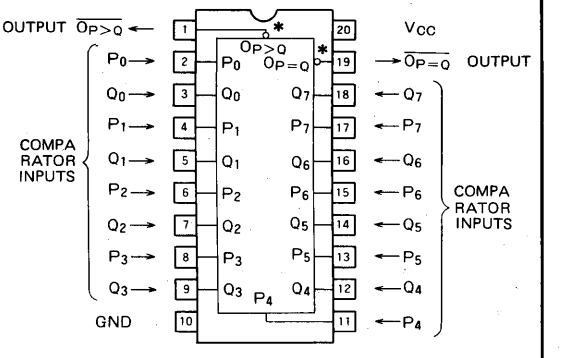
The eight-bit binary or BCD words are applied at inputs P_0 ~ P_7 and Q_0 ~ Q_7. The results as shown in Function Table are expressed at outputs $\overline{O_{P>Q}}$ and $\overline{O_{P=Q}}$.

Note that this IC, in comparison to M74LS683P, does not have internal pull-up resistors on its inputs Q_0 ~ Q_7.

Beside this IC, there are eight-bit digital comparators varying input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application of M74LS682P.

PIN CONFIGURATION (TOP VIEW)



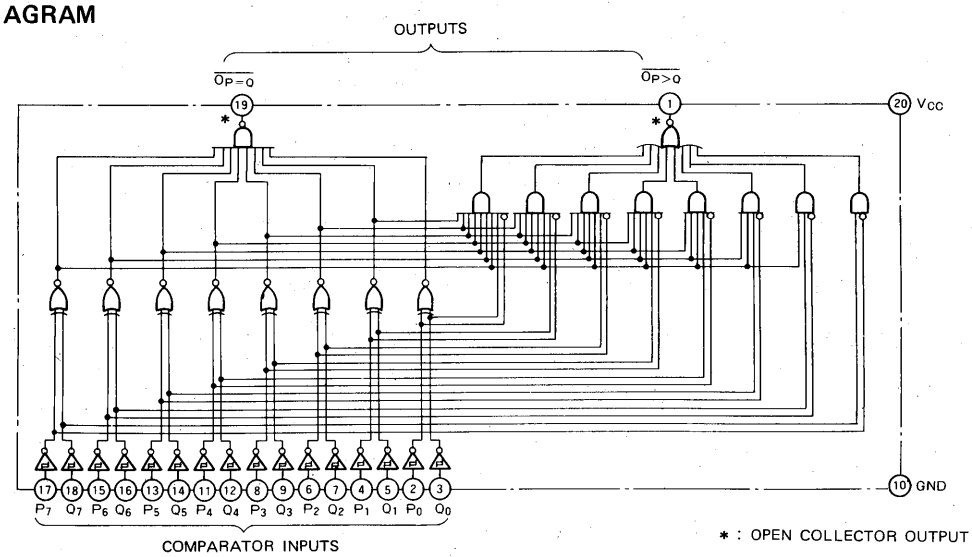
* : OPEN COLLECTOR OUTPUTS

Outline 20P4

8-BIT MAGNITUDE COMPARATORS TABLE

Type designation	Inputs		Outputs		
	Q 24kΩ pull-up	$\overline{E}$	$\overline{O_{P=Q}}$	$\overline{O_{P>Q}}$	Format
M74LS682P	Yes	No	Yes	Yes	Active pull-up
M74LS683P	Yes	No	Yes	Yes	Open collector
M74LS684P	No	No	Yes	Yes	Active pull-up
M74LS685P	No	No	Yes	Yes	Open collector
M74LS688P	No	Yes	Yes	No	Active pull-up
M74LS689P	No	Yes	Yes	No	Open collector

BLOCK DIAGRAM



* : OPEN COLLECTOR OUTPUT

8-BIT MAGNITUDE COMPARATOR WITH OPEN COLLECTOR OUTPUT

FUNCTION TABLE

P, Q	$\overline{O_{P=Q}}$	$\overline{O_{P>Q}}$
P=Q	L	H
P>Q	H	L
P<Q	H	H

ABSOLUTE MAXIMUM RATINGS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+15	V
V_O	Output voltage	High-level state	−0.5∼+7	V
Topr	Operating free-air ambient temperature range		−20∼+75	℃
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O=5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta=−20∼+75℃, unless otherwise noted)

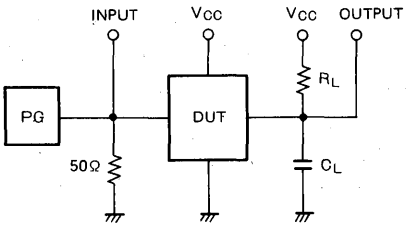
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
$V_{T+}-V_{T-}$	Hysteresis width	V_{CC}=4.75V			0.4		V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
I_{OH}	High-level output current	V_{CC}=4.75V, V_I=2V, V_I=0.8V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage	V_{CC}=4.75V, V_I=2V, V_I=0.8V	I_{OL}=12mA		0.25	0.4	V
			I_{OL}=24mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.2	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 1)			40	65	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 1: I_{CC} is measured with all inputs at value of 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

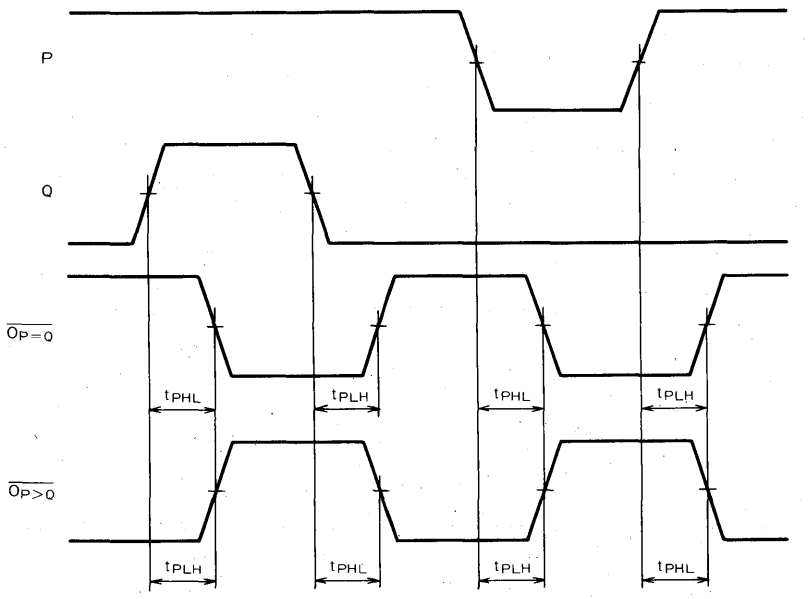
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs P to output $\overline{O_{P=Q}}$	R_L=667Ω, C_L=45pF (Note 2) All other input pins in low-state		23	45	ns
t_{PHL}				20	35	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs Q to output $\overline{O_{P=Q}}$			21	45	ns
t_{PHL}				20	35	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs P to output $\overline{O_{P>Q}}$			26	45	ns
t_{PHL}				22	35	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs Q to output $\overline{O_{P>Q}}$			28	45	ns
t_{PHL}				26	35	

Note 2: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



NEW PRODUCT

M74LS688P

8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT

DESCRIPTION

The M74LS688P is a semiconductor integrated circuit containing two 8-bit words comparator functions with enable input.

FEATURES

- Hysteresis at inputs P and Q (width = 400mV typical)
- Provided with enable input ($\overline{E}$)
- Active pull-up output
- Wide operating temperature range (T_a = –20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

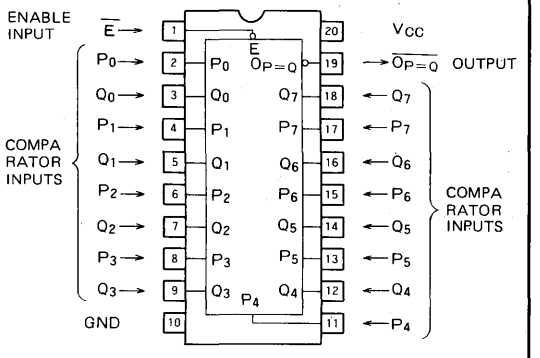
When enable input $\overline{E}$ is low, two eight-bit binary or BCD words are applied at inputs $P_0 \sim P_7$ and $Q_0 \sim Q_7$. The results as shown in Function Table are expressed at output $\overline{O_{P=Q}}$.

When E is high, $\overline{O_{P=Q}}$ is high in spite of $P_0 \sim P_7$ and $Q_0 \sim Q_7$.

Beside this IC, there are eight-bit digital comparators varing input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application.

PIN CONFIGURATION (TOP VIEW)

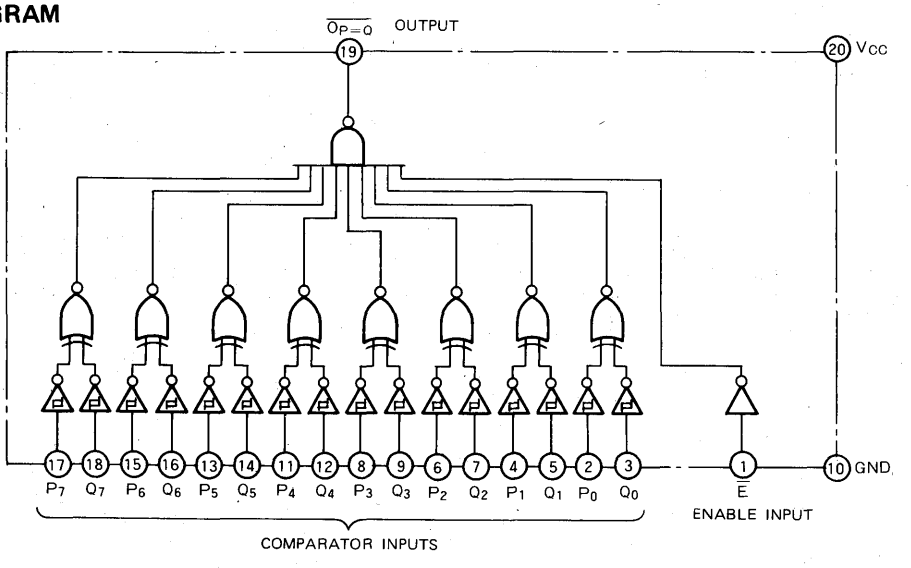


Outline 20P4

8-BIT MAGNITUDE COMPARATORS TABLE

Type designation	Inputs		Outputs		
	Q 24kΩ pull-up	$\overline{E}$	$\overline{O_{P=Q}}$	$\overline{O_{P>Q}}$	Format
M74LS682P	Yes	No	Yes	Yes	Active pull-up
M74LS683P	Yes	No	Yes	Yes	Open collector
M74LS684P	No	No	Yes	Yes	Active pull-up
M74LS685P	No	No	Yes	Yes	Open collector
M74LS688P	No	Yes	Yes	No	Active pull-up
M74LS689P	No	Yes	Yes	No	Open collector

BLOCK DIAGRAM



8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT

FUNCTION TABLE (Note 1)

P, Q	$\overline{E}$	$\overline{O_{P=Q}}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

Note 1: X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+15	V
V_O	Output voltage	High-level state	−0.5∼V_{CC}	V
Topr	Operating free-air ambient temperature range		−20∼+75	℃
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_{OH}≧2.7V	0		400	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta=−20∼+75℃, unless otherwise noted)

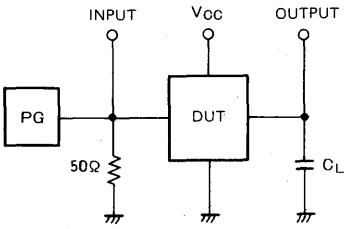
Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
$V_{T+}-V_{T-}$	Hysteresis width	V_{CC}=4.75V			0.4		V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=4.75V, V_I=2V, V_I=0.8V, I_{OH}=−400μA		2.7			V
V_{OL}	Low-level output voltage	V_{CC}=4.75V, V_I=2V, V_I=0.8V	I_{OL}=12mA		0.25	0.4	V
			I_{OL}=24mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.2	mA
I_{OS}	Short-circuit output current	V_{CC}=5.25V, V_O=0V		−20		−100	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 2)			40	65	mA

*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 2: I_{CC} is measured with all other inputs at value of 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

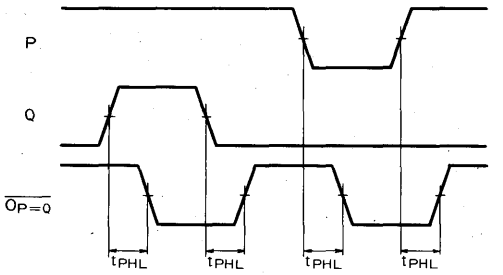
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs P to output $\overline{O_{P=Q}}$	C_L=45pF (Note 3) All other input pins in low-state		12	23	ns
t_{PHL}				18	28	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs Q to output $\overline{O_{P=Q}}$			11	23	ns
t_{PHL}				19	28	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from input $\overline{E}$ to output $\overline{O_{P=Q}}$			10	18	ns
t_{PHL}				16	20	

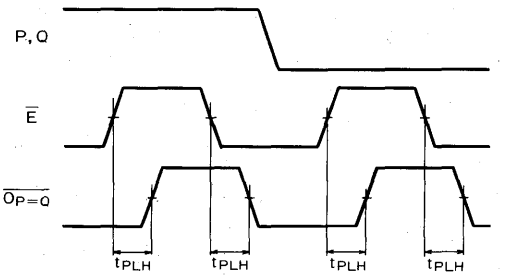
Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = $3V_{P-P}$, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

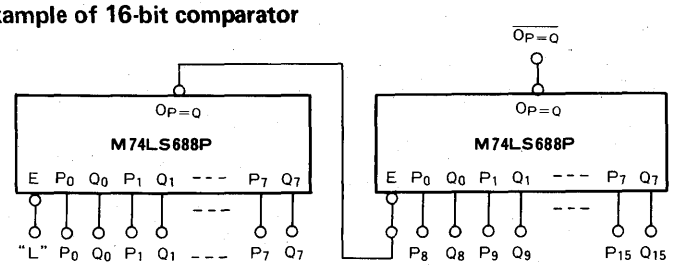
TIMING DIAGRAM (Reference level = 1.3V)





APPLICATION EXAMPLE

Example of 16-bit comparator



NEW PRODUCT

M74LS689P

8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT AND OPEN COLLECTOR OUTPUT

DESCRIPTION

The M74LS689P is a semiconductor integrated circuit contaning two 8-bit words comparator functions with enable input and open collector output.

FEATURES

- Hysteresis at inputs P and Q (width = 400mV typical)
- Provided with enable input ($\overline{E}$)
- Open collector output
- Operating temperature range (T_a = –20 ~ +75°C)

APPLICATION

General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

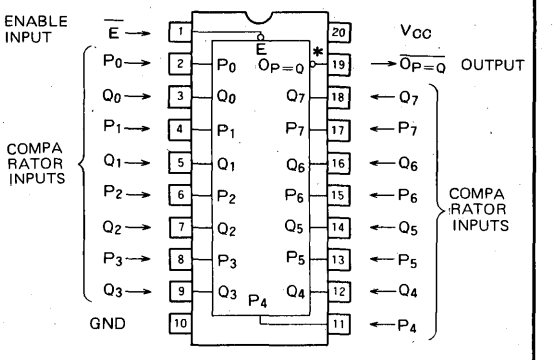
When enable input $\overline{E}$ is low, two eight-bit binary or BCD words are applied at inputs P_0 ~ P_7 and Q_0 ~ Q_7. The results as shown in Function Table are expressed at output $\overline{O_{P=Q}}$.

When E is high, $\overline{O_{P=Q}}$ is high in spite of P_0 ~ P_7 and Q_0 ~ Q_7.

Beside this IC, there are eight-bit digital comparators varing input/output formats. They are shown in the table. The detailed information are shown in individual catalogue.

An example of the extention bits is shown in the application in M74LS688P.

PIN CONFIGURATION (TOP VIEW)



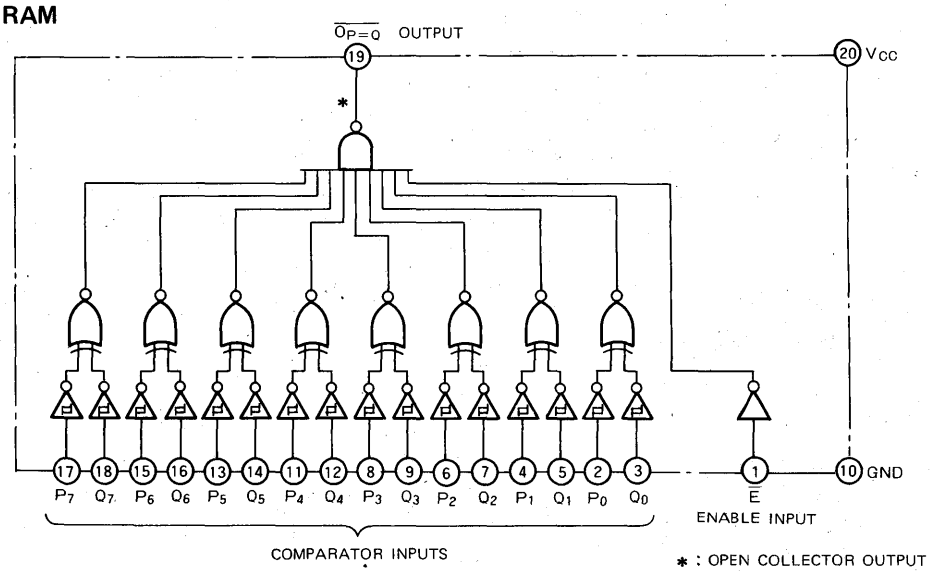
* : OPEN COLLECTOR OUTPUT

Outline 20P4

8-BIT MAGNITUDE COMPARATORS TABLE

Type designation	Inputs		Outputs		
	Q 24kΩ pull-up	$\overline{E}$	$\overline{O_{P=Q}}$	$\overline{O_{P>Q}}$	Format
M74LS682P	Yes	No	Yes	Yes	Active pull-up
M74LS683P	Yes	No	Yes	Yes	Open collector
M74LS684P	No	No	Yes	Yes	Active pull-up
M74LS685P	No	No	Yes	Yes	Open collector
M74LS688P	No	Yes	Yes	No	Active pull-up
M74LS689P	No	Yes	Yes	No	Open collector

BLOCK DIAGRAM



* : OPEN COLLECTOR OUTPUT

MITSUBISHI ELECTRIC

8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT AND OPEN COLLECTOR OUTPUT

FUNCTION TABLE (Note 1)

P, Q	$\overline{E}$	$\overline{O_{P=Q}}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

Note 1: X: Irrelevant

ABSOLUTE MAXIMUM RATINGS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5∼+7	V
V_I	Input voltage		−0.5∼+15	V
V_O	Output voltage	High-level state	−0.5∼+7	V
Topr	Operating free-air ambient temperature range		−20∼+75	℃
Tstg	Storage temperature range		−65∼+150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	V_O=5.5V	0		100	μA
I_{OL}	Low-level output current	V_{OL}≦0.4V	0		12	mA
		V_{OL}≦0.5V	0		24	mA

ELECTRICAL CHARACTERISTICS (Ta=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ *	Max	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
$V_{T+}-V_{T-}$	Hysteresis width	V_{CC}=4.75V			0.4		V
V_{IC}	Input clamp voltage	V_{CC}=4.75V, I_{IC}=−18mA				−1.5	V
I_{OH}	High-level output current	V_{CC}=4.75V, V_I=2V, V_I=0.8V, V_O=5.5V				100	μA
V_{OL}	Low-level output voltage	V_{CC}=4.75V, V_I=2V, V_I=0.8V	I_{OL}=12mA		0.25	0.4	V
			I_{OL}=24mA		0.35	0.5	V
I_{IH}	High-level input current	V_{CC}=5.25V, V_I=2.7V				20	μA
		V_{CC}=5.25V, V_I=10V				0.1	mA
I_{IL}	Low-level input current	V_{CC}=5.25V, V_I=0.4V				−0.2	mA
I_{CC}	Supply current	V_{CC}=5.25V (Note 2)			40	65	mA

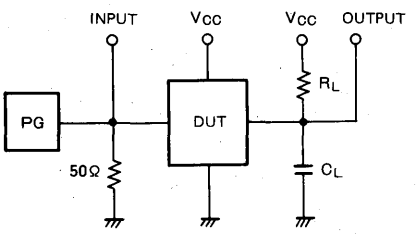
*: All typical values are at V_{CC} = 5V, T_a = 25°C.
Note 2: I_{CC} is measured with all inputs at value of 4.5V.

SWITCHING CHARACTERISTICS (V_{CC}=5V, Ta=25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs P to output $\overline{O_{P=Q}}$	R_L=667Ω, C_L=45pF (Note 3) All other input pins in low-state.		23	40	ns
t_{PHL}				21	35	
t_{PLH}	Low-to-high level, high-to-low level output propagation time from inputs Q to output $\overline{O_{P=Q}}$			23	40	ns
t_{PHL}				21	35	
t_{PLH}	Low-to-high level high-to-low level output propagation time from input $\overline{E}$ to output $\overline{O_{P=Q}}$			22	35	ns
t_{PHL}				20	30	

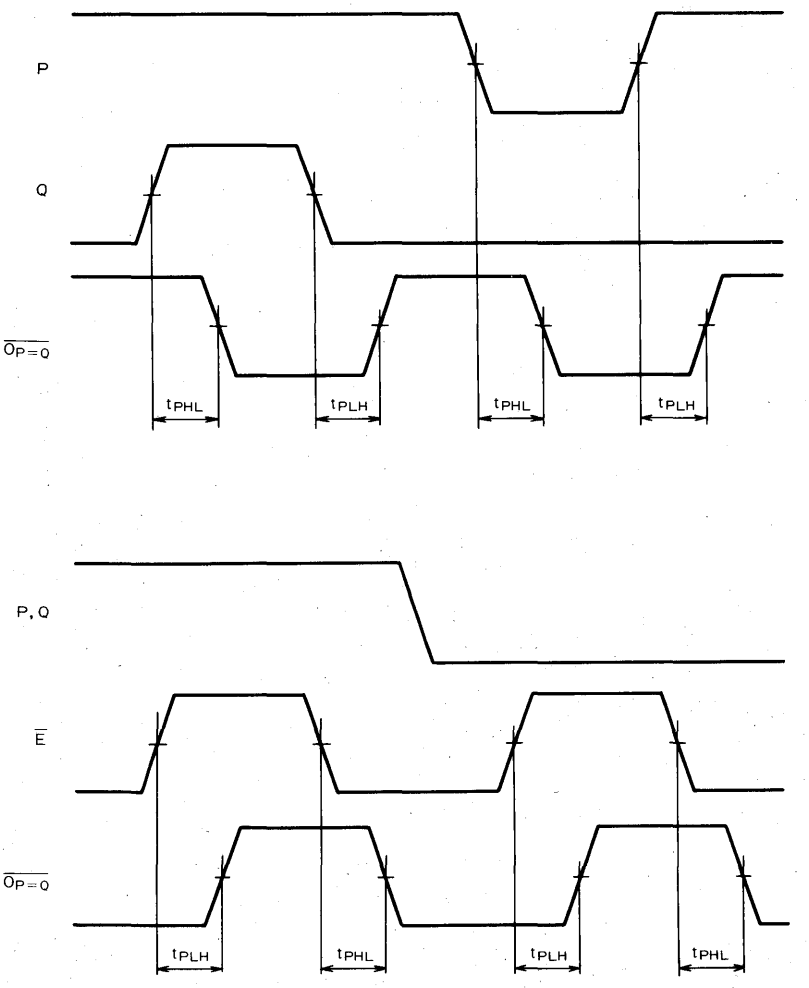
8-BIT MAGNITUDE COMPARATOR WITH ENABLE INPUT AND OPEN COLLECTOR OUTPUT

Note 3: Measurement circuit



(1) The pulse generator (PG) has the following characteristics: PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns, V_P = 3V_{P-P}, Z_O = 50Ω
(2) C_L includes probe and jig capacitance.

TIMING DIAGRAM (Reference level = 1.3V)



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