User's Manual

National Semiconductor

COP400-E02 In-Circuit Emulator Card

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National Semiconductor

420305896-001

1 Introduction

The COP400-E02 enables the user to perform in-circuit emulation of the 410L, 411L, 420L, 420, 421L, and 421 members of the COP400 Microcontroller family. The emulator card may be used stand-alone with PROMs and external power supply, or as a peripheral to the COP400 Product Development System (PDS). When used in conjunction with the PDS, the E02 Emulator gives the user the added capabilities of real-time program tracing, breakpoint/single-stepping, and speedy program updating. The net result is rapid program evolution from conception through debug to final product.

THE USER SHOULD
READ THIS MANUAL THOROUGHLY
BEFORE ATTEMPTING
COP4XX EMULATION.

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2 General Description

2.1 Physical Features

The E02 Emulator is a 5 × 6-inch double-sided printed circuit board mounted on four 0.5-inch nylon stand-offs. Figure 2.1 contains a drawing of the board with its emulator cables removed. The workhorse of the board is the COP402 ROM-less Microcontroller found top-center on the board. To the left of the 402 are 4 single-in-line connectors and one 20-pin socket used as receptacles for the DIP-to-DIP emulator cables. In the center of the board are two MM5204 PROM sockets. The PROM socket labeled "PROM 0" is for COP addresses 0-X'1FF, and the socket labeled "PROM 1" is for addresses X'200-X'3FF. Below the PROM sockets at the bottom of the board is a 50-pin edge connector used to interface to the rear of the Product Development System via the PDS emulator card cable. Pin 1 of this cable should match up with pin 1 of the edge connector which is located in the lower right-hand corner of Figure 2.1.

NEVER CONNECT OR DISCONNECT THE E02 CARD FROM THE PDS EMULATOR CARD CABLE WHILE THE PDS IS TURNED ON; PERMANENT PDS AND/OR E02 DAMAGE MAY RESULT.

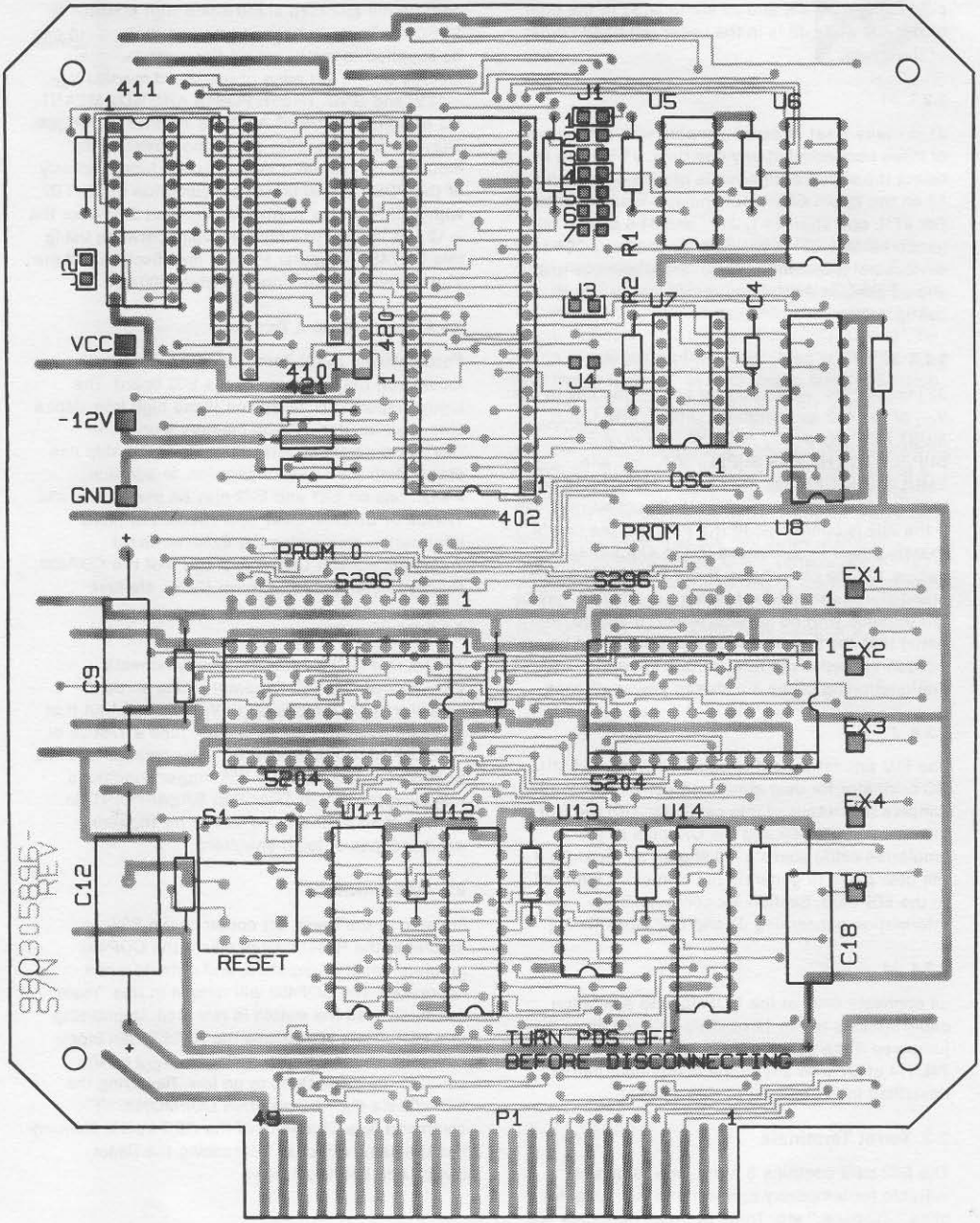

Figure 2.1. COP400-E02 In-Circuit Emulator Layout

2.2 Jumpers

The E02 card is equipped with 4 sets of wire-wrap pin jumpers. J1, J3, and J4 are located to the right of the 402 while J2 is in the upper left-hand corner of the board.

2.2.1 J1

J1 is really a set of seven jumpers with a maximum of three connected at any one time. J1 is used to select the signal assignments of pins 13, 14, and 15 on the 20-pin COP411L emulator cable socket. For 411L operation J1-1, J1-4, and J1-6 should be jumpered. In order to emulate other 20-pin COP400 devices not mentioned in this document, the user should contact the factory for the necessary J1 configuration.

2.2.2 J2

J2 jumpers the +5 volt power bus on the E02 to the V_{CC} of the 402 and emulator cables. THE USER MUST NOT CONNECT HIS SYSTEM POWER SUPPLY TO THE PDS SUPPLY VIA THE 4XX EMULATION CABLES. This could destroy one or both supplies. Consequently, J2 should be removed if the E02 is connected to the PDS and the user's system power is connected to the 4XX emulator cables. On the other hand, if the E02 is being used stand-alone with external power supplies J2 may be left in place with no harmful effect. It should be noted that the target system's power should be adequately bypassed to eliminate spurious malfunctioning of the 402 due to power glitches.

2.2.3 J3

The E02 Emulator Card is supplied with a 3.5 MHz RC oscillator for user emulation convenience. J3 jumpers the output of this oscillator into the CKI input of the COP402 and the CKI pins of the emulation cable sockets. J3 should be removed if the user plans to generate his own clock external to the E02 card. Section 3.2 contains more information concerning J3 and E02 clock timing.

2.2.4 J4

J4 connects CKO of the COP402 and emulation cable sockets to pin 11 of U7. J4 should be jumpered if the user is planning on replacing the 74LS14 of U7 with any of the component carriers described in Section 3.2 of this manual.

2.3 Turret Terminals

The E02 card contains 8 turret-type terminals suitable for temporary connections via "alligator clips," "Q-balls," etc. Three of these terminals are used for E02 power, four are used as logic inputs to the PDS, and the last is a logic output of the PDS.

2.3.1 E02 Emulator Power Terminals

Two supplies (+5 and −12 VDC) are needed to operate the E02 card stand-alone with MM5204 EPROMs. These voltage inputs and their return can be supplied to the board via the three terminals located on the left edge of the board marked V_{CC}, −12V, and GND. THESE POSTS ARE NOT MEANT TO ALLOW THE USER ACCESS TO PDS SUPPLIES. They are to be used for supplying power to the emulator card when it is being used independently of the PDS. Typical power consumption of the E02 with 2 EPROMs is 150 mA for V_{CC} and 30 mA for the −12 volt input. For single +5 volt operation using two DM74S474 bipolar PROMs (see Section 3.3) the V_{CC} current drain is approximately 300 mA.

2.3.2 External Event Terminals

Four External Event Terminals (EX1-EX4) are located on the right side of the E02 board. The logical inputs (TTL levels) on these high impedance pins are stored in TRACE memory along with COP402 program counter values and the skip line status during a TRACE operation. In addition, transitions on EX1 and EX2 may be used to initiate TRACE or BREAKPOINT operations. For more information concerning the External Event Terminals consult Chapters 2 and 9 of the *COP400 Product Development System User's Manual.*

2.3.3 Trigger Out

Trigger Out (TO) is located directly beneath EX1-EX4 on the E02 Emulator. TO is an open-collector (150 ohm pull-up to V_{CC}) PDS output that makes a positive transition each time a TRACE or BREAKPOINT is initiated. TO will continue to make positive transitions every 256 trigger conditions following the actual TRACE or BREAKPOINT. In certain applications TO is useful for triggering oscilloscopes or logic analyzers.

2.4 Reset Switch

Located in the lower left corner of the E02 Emulator, the Reset switch clears the COP402 program counter, registers, and outputs when depressed. The COP402 will remain in this "reset" condition until the switch is released. Depressing this switch will also cause the RESET* pin (open-collector output, 5k ohm pull-up to V_{CC}) on the emulator cable sockets to go low. Resetting the COP402 via the PDS program COPMON's "R" command (see Chapter 9 of the *PDS User's Manual*) has the same effect as depressing the Reset switch and holding it down.

2.5 Edge Connector Assignments

The 50-pin edge connector located at the bottom of the E02 card provides a means of interfacing to the connectors EMULATOR 1 and EMULATOR 2 located on the rear panel of the PDS. Table 2.1 contains the names and a brief description of each signal that passes over the cable between the E02 and PDS.

Table 2.1. Edge Connector Assignments

Connector No.	Name	Description
1	GND	Signal and power return
2	GND	Signal and power return
3	V_{CC}	+5VDC power from PDS
4	V_{CC}	+5VDC power from PDS
5	EX2	Buffered External Event (see 2.3.2)
6	EX1	Buffered External Event
7	EX4	Buffered External Event
8	EX3	Buffered External Event
9	CLK	Buffered AD/DATA* signal from COP402
10	SKIP	COP402 skip status line
11	A8	COP402 program counter address bit
12	A9	Address bit
13	A3	Address bit
14	A7	Address bit
15	A1	Address bit
16	A2	Address bit
17	A4	Address bit
18	A0	Least significant address bit
19	A6	Address bit
20	A5	Address bit
21	Not Used	
22	A10	Most significant address bit
23	Not Used	
24	Not Used	
25	Not Used	
26	Not Used	
27	Not Used	
28	Not Used	
29	Not Used	
30	Not Used	
31	Not Used	
32	Not Used	
33	B0	Least significant COP object code bit
34	B7	Most significant COP object code bit
35	B2	Object code bit
36	B5	Object code bit
37	B3	Object code bit
38	B4	Object code bit
39	B6	Object code bit
40	B1	Object code bit
41	TRIGGER OUT	BREAKPOINT/TRACE indicator (see 2.3.3)
42	Not Used	
43	RST*	Same as RESET* (see 2.4)
44	PROM DISABLE*	Selects PROM or Shared Memory mode
45	−12V	−12VDC from PDS for E02 PROMs
46	−12V	−12VDC from PDS for E02 PROMs
47	V_{CC}	+5VDC power from PDS
48	V_{CC}	+5VDC power from PDS
49	GND	Power and signal return
50	GND	Power and signal return

3 Operating Considerations

3.1 Emulator Cables

The user should take careful note of the orientation of pin 1 on the various emulator cable sockets (see Figure 2.1). The 20-pin socket in the upper left corner of the E02 Emulator is presently used for emulating the COP411L. Pin 1 of the device cable should be oriented away from the center of the board as marked. The four SIPs to the right of this connector are configured as 24- and 28-pin emulator sockets. Pin 1 for both of these sockets is oriented toward the center of the card. The 24-pin socket may be used for emulating the 410L, 421L, and 421. The 28-pin socket is intended to emulate the 420L and 420. Three DIP-to-DIP cables (20-, 24-, and 28-pin) are supplied with the E02 card for user emulation purposes.

ONLY ONE COP400 FAMILY DEVICE MAY BE EMULATED AT A TIME.

3.2 Clock Timing

3.2.1 RC Oscillator

As stated previously, the E02 Emulator is equipped with an on-board 3.5 MHz RC oscillator for user convenience. The frequency of this oscillator may be lowered by replacing the 74LS14 of U7 with a 74C04 and altering the values of R1, R2, and C4 (see Figure 2.1) to the ones shown in Table 3.1. It should be noted that the fastest specified instruction cycle for the 4XXL devices is 16 μs. Although the COP402 has a guaranteed maximum instruction cycle of 10 μs, emulation at somewhat slower speeds is reliable.

Table 3.1. RC Oscillator Component Values

R1 (Ω)	R2 (Ω)	C4 (pF)	Oscillator Frequency (MHz)	Instruction Cycle (μs)
680	680	27	2.0	8
1.7k	1.7k	27	1.5	11
1.0k	3.0k	100	1.0	16
4.0k	4.0k	100	0.5	32

3.2.2 Crystal Oscillator

The COP402 on the E02 Emulator has a crystal option which enables the user to emulate with a crystal controlled clock. Unfortunately, emulator cable capacitance and inductance preclude the use of the crystal on the user's prototype system. This limitation may be circumvented by replacing the 74LS14 (U7) with a 14-pin component carrier containing the circuit shown in Figure 3.1, installing J3, installing J4, and removing pins CKI and CKO of the emulator cable from the emulator cable socket. This last step is necessary because cable capacitance will upset the crystal's stability. Table 3.2 contains the various values of Rx1, Rx2, and Cx needed for 3 standard crystal frequencies.

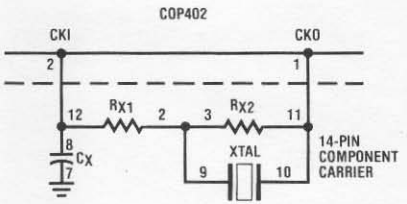

Figure 3.1. Crystal Oscillator Component Carrier Schematic

Table 3.2. Crystal Oscillator Component Values

Rx1 (Ω)	Rx2 (Ω)	Cx (pF)	XTAL Frequency (MHz)	Instruction Cycle (μs)
1.0k	1.0M	27	4.00	4.0
1.0k	1.0M	27	3.58	4.5
1.0k	1.0M	56	2.09	7.7

3.2.3 LC Oscillator

In a similar fashion, U7 may be replaced with a 14-pin carrier containing components for an LC oscillator. Figure 3.2 shows the schematic and Table 3.3 contains sample values for a COP402 LC oscillator.

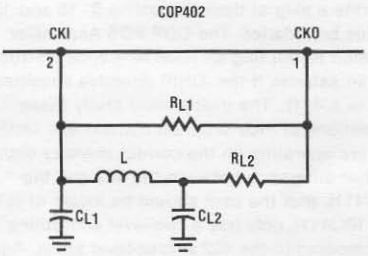

Figure 3.2. LC Oscillator Schematic

Table 3.3. LC Oscillator Component Values

RL1 (Ω)	RL2 (Ω)	CL1 (pF)	CL2 (pF)	L (μH)	Oscillator Frequency (MHz)	Instruction Cycle (μs)
10.0M	511	100	100	22	4.0	4.0
10.0M	511	500	100	22	3.0	5.3
10.0M	511	200	500	22	2.6	6.2
10.0M	511	200	25000	22	1.4	11.4

3.3 Bipolar PROMs

For single supply +5 volt operation, the E02 card may be modified to accept DM74S474 or DM74S475 bipolar PROMs. The holes for these PROMs are located directly above the EPROM sockets on Figure 2.1 and are labeled S296 (the part's previous name). Pin 1 is marked as such.

4 Functional Verification

Correct operation of the COP400-E02 Emulator Card can best be verified by connecting the E02 card to a PDS and emulating a small COP400 family program. Such a program and helps may be found in Section 3.3 of the *PDS User's Manual*. By using the debug routines contained in COPMON and the "coaching" of *PDS User's Manual* Section 3.3, the user should be able to verify correct operation of the emulator's program counter, external event inputs, skip line, and general internal workings. External circuitry, an oscilloscope, or a logic analyzer may be helpful in examining the emulated COP420 output pins. The user may wish to connect several of the 420 outputs in this example to the External Event Terminals (EX1 - EX4) to gain a better understanding of the practical use of these inputs during the COPMON TRACE and BREAKPOINT commands. (See Chapter 9 of the *PDS User's Manual*.)

5 What to Do If . . .

Due to the E02 card's intimate relationship with the user's hardware and physical location external to the PDS, it is extremely vulnerable to misuse and destruction by careless hands. The user should always observe that:

1. Power supplies are adequately bypassed and of the correct voltage.
2. PDS power is not connected to user power.
3. Cables are correctly installed.
4. Device input/output ratings are not exceeded.
5. PROMs are in their correct sockets and properly oriented.
6. The COP402 is receiving a valid clock signal.

If a mishap or malfunction does occur, National Semiconductor's Microcomputer Technical Support Manager will be happy to help you at (408) 737-6803. Questions concerning actual operation of the E02 card or customer use of a COP400 device may be referred to the COPS Application Group at (408) 737-5582.

Alternately, if the E02 should develop a problem and circumstances do not allow sufficient time to send it back to National, there is a series of COPMON commands that may be used to isolate the faulty component(s). Before attempting the following diagnostic aids, the user should study Chapter 9 of the *PDS User's Manual,* Section 2.5 of this manual, and the schematic supplied with the E02 Emulator. The user will also need a functional PDS and PDS emulator card cable.

Step 1

With power turned off, connect the E02 to the PDS.

Step 2

Turn power on, load COPMON, and specify chip number as 440.

Example:

```
(CR)
EXEC, REV:A

X>@COPMON

COPMON, REV:B

CHIP NUMBER (DEFAULT = 420) ? 440

SYSTEM INITIALIZED FOR E04 EMULATOR
```

Specifying the CHIP NUMBER to 440 will allow the E02 to access all of shared memory even though A10 should always be logic low for the E02.

Step 3

Load shared memory with CLRA (object code = X'00) instructions.

```
C>DE 0,0/L
```

Step 4

Specify and perform a TRACE IMMEDIATE.

```
C>TR I

TRACE ENABLED:
IMED OCCUR:      1 PRIOR:          0 GO:N

C>G
```

COPMON should come back with the following message:

```
TRACED ON  IMED  AT A:000
```

If it does not, then the CLK signal described in Section 2.5 is not being generated by the COP402 and/or is not reaching the PDS. Probable faulty circuits:

- COP402 (U4)
- 81LS95 (U8)

The user should also verify that the COP402 is receiving a valid clock input.

Given that COPMON did execute the TRACE properly, the COP program counter should now be examined with the TYPE command.

```
C>TY

 0          0 A:000        E:1111
 1          1 A:000        E:1111
 2          2 A:000        E:1111
 3          3 A:000        E:1111
 4          4 A:000        E:1111
 5          5 A:000        E:1111
 6          6 A:000        E:1111
 7          7 A:000        E:1111
 8          8 A:000        E:1111
 9          9 A:000        E:1111
10         10 A:000        E:1111
11         11 A:000        E:1111
12         12 A:000        E:1111
13         13 A:000        E:1111
14         14 A:000        E:1111
15         15 A:000        E:1111
```

Note all the address values (A:XXX) shown are zero. This is correct because the TRACE operation was begun before COPMON let RST*/RESET* go to a high level. If one or more of the E02 program counter bits are stuck high, the TYPE command might yield the following information:

```
C>TY

 0          0 A:009        E:1111
 1          1 A:009        E:1111
 2          2 A:009        E:1111
 3          3 A:009        E:1111
 4          4 A:009        E:1111
 5          5 A:009        E:1111
 6          6 A:009        E:1111
 7          7 A:009        E:1111
 8          8 A:009        E:1111
 9          9 A:009        E:1111
10         10 A:009        E:1111
11         11 A:009        E:1111
12         12 A:009        E:1111
13         13 A:009        E:1111
14         14 A:009        E:1111
```

With this information the user can generally isolate which address line (A0-A10) is malfunctioning. Probable faulty circuits:

- 81LS95 (U8)
- 81LS95 (U14)
- 74LS373/74C373 (U12)

Step 5

Another TRACE IMMEDIATE command will test RST*/RESET* and proper binary operation of the address lines.

```
C>G

TRACED ON IMED AT A:01B
C>TY

 0          0 A:01B        E:1111
 1          1 A:01C        E:1111
 2          2 A:01D        E:1111
 3          3 A:01E        E:1111
 4          4 A:01F        E:1111
 5          5 A:020        E:1111
 6          6 A:021        E:1111
 7          7 A:022        E:1111
 8          8 A:023        E:1111
 9          9 A:024        E:1111
10         10 A:025        E:1111
11         11 A:026        E:1111
12         12 A:027        E:1111
13         13 A:028        E:1111
14         14 A:029        E:1111
15         15 A:02A        E:1111
C>TY

16         16 A:02B        E:1111
17         17 A:02C        E:1111
18         18 A:02D        E:1111
19         19 A:02E        E:1111
20         20 A:02F        E:1111
21         21 A:030        E:1111
22         22 A:031        E:1111
23         23 A:032        E:1111
24         24 A:033        E:1111
25         25 A:034        E:1111
26         26 A:035        E:1111
27         27 A:036        E:1111
28         28 A:037        E:1111
29         29 A:038        E:1111
30         30 A:039        E:1111
31         31 A:03A        E:1111
```

If the RST*/RESET* line is stuck low, the addresses shown above would have remained at zero. Probable faulty circuits:

- COP402 (U4)
- PDS

The COP addresses from this second TRACE IMMEDIATE operation should be inspected for monotonically increasing binary values from 0 to 3FF and wrap-around from 3FF to 0. This can be done by additional TRACE and TYPE commands.

If several address lines are shorted or nonoperative, a TYPE command might yield program counter values like the following:

```
C>TY

 0      0 A:38B     E:1111
 1      1 A:38B     E:1111
 2      2 A:38D     E:1111
 3      3 A:38D     E:1111
 4      4 A:38F     E:1111
 5      5 A:38F     E:1111
 6      6 A:399     E:1111
 7      7 A:399     E:1111
 8      8 A:39B     E:1111
 9      9 A:39B     E:1111
10     10 A:39D     E:1111
11     11 A:39D     E:1111
12     12 A:39F     E:1111
13     13 A:39F     E:1111
14     14 A:399     E:1111
15     15 A:399     E:1111
C>TY

16     16 A:39B     E:1111
17     17 A:39B     E:1111
18     18 A:39D     E:1111
19     19 A:39D     E:1111
20     20 A:39F     E:1111
21     21 A:39F     E:1111
22     22 A:3A9     E:1111
23     23 A:3A9     E:1111
24     24 A:3AB     E:1111
25     25 A:3AB     E:1111
26     26 A:3AD     E:1111
27     27 A:3AD     E:1111
28     28 A:3AF     E:1111
29     29 A:3AF     E:1111
30     30 A:3A9     E:1111
31     31 A:3A9     E:1111
```

Probable faulty circuits:

- 81LS95 (U14)
- 81LS95 (U8)
- 74LS373/74C373 (U12)

Step 6

Given proper operation of the E02 card to this point, the actual program data bits (B0-B7) will now be tested by inserting various jump commands into memory and using TRACE to verify that the jump occurred. If the E02 fails any of the following tests, the probable faulty circuit is:

- 81LS95 (U11)

Insert a jump to location 0 at address 3E and set up, execute, and list the trace.

```
C>PU 3E, JP 0

C>TR 3E, 1, 0

TRACE ENABLED:
 A:03E OCCUR:  1 PRIOR:  0 GO: N

C>G

TRACED ON  A:03E AT A:03E
C>TY 0/4

0      0 A:03E     E:1111
1      1 A:000     E:1111
2      2 A:001     E:1111
3      3 A:002     E:1111
4      4 A:003     E:1111
```

If the second TRACE memory location does not contain A:000, then the E02 is not recognizing the JP 0 instruction (object code = X'C0) properly. If the JP 0 is working, then high levels on B6 and B7 from the PDS are being recognized by the E02. Proper high levels on B0-B5 may now be tested by successively replacing the JP 0 instruction with the following jumps: JP 1 (X'C1), JP 2 (X'C2), JP 4 (X'C4), JP 8 (X'C8), JP 10 (X'D0), and JP 20 (X'E0). The necessary COPMON commands are:

```
C>PU 3E, JP 1

C>G

TRACED ON  A:03E AT A:03E
C>TY 0/4

0      0 A:03E     E:1111
1      1 A:001     E:1111
2      2 A:002     E:1111
3      3 A:003     E:1111
4      4 A:004     E:1111
```

Note that the contents of trace location 1 should be A:001. If B0 and B1 were shorted or inoperative, the TYPE command might yield the following information:

```
C>G

TRACED ON  A:03E AT A:03E
C>TY
```

0	0	A:03E	E:1111
1	1	A:003	E:1111
2	2	A:004	E:1111
3	3	A:005	E:1111
4	4	A:006	E:1111
5	5	A:007	E:1111
6	6	A:008	E:1111
7	7	A:009	E:1111
8	8	A:00A	E:1111
9	9	A:00B	E:1111
10	10	A:00C	E:1111
11	11	A:00D	E:1111
12	12	A:00E	E:1111
13	13	A:00F	E:1111
14	14	A:010	E:1111
15	15	A:011	E:1111

Continuing the test:

```
C>TR 3E, 1, 0

TRACE ENABLED:
 A:03E OCCUR:  1 PRIOR:  0 GO: N
C>PU 3E, JP 2

C>G

TRACED ON  A:03E AT A:03E
C>TY 0/4
```

0	0	A:03E	E:1111
1	1	A:002	E:1111
2	2	A:003	E:1111
3	3	A:004	E:1111
4	4	A:005	E:1111

```
C>PU 3E, JP 4

C>G

TRACED ON  A:03E AT A:03E
C>TY 0/4
```

0	0	A:03E	E:1111
1	1	A:004	E:1111
2	2	A:005	E:1111
3	3	A:006	E:1111
4	4	A:007	E:1111

```
C>PU 3E, JP 8

C>G

TRACED ON  A:03E AT A:03E
C>TY 0/4
```

0	0	A:03E	E:1111
1	1	A:008	E:1111
2	2	A:009	E:1111
3	3	A:00A	E:1111
4	4	A:00B	E:1111

```
C>PU 3E, JP 10

C>G

TRACED ON  A:03E AT A:03E
C>TY 0/4
```

0	0	A:03E	E:1111
1	1	A:010	E:1111
2	2	A:011	E:1111
3	3	A:012	E:1111
4	4	A:013	E:1111

```
C>PU 3E, JP 20

C>G

TRACED ON  A:03E AT A:03E
C>TY 0/4
```

0	0	A:03E	E:1111
1	1	A:020	E:1111
2	2	A:021	E:1111
3	3	A:022	E:1111
4	4	A:023	E:1111

If the E02 Emulator passes all of the above tests, the supporting circuitry to the COP402 should be functional. It is imperative that all of these tests be performed with a completely operational Product Development System. A malfunctioning E02 card is difficult to discern from a malfunctioning PDS. If the user still experiences difficulties during program emulation, the Microcomputer Technical Support Manager (408-737-6803) should be contacted.

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
Tel: (408) 737-5000
TWX: (910) 339-9240

National Semiconductor
District Sales Office
345 Wilson Avenue, Suite 404
Downsview, Ontario M3H 5W1
Canada
Tel: (416) 635-7260

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Tlacoquemecatl No. 139-401
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Mexico 12, D.F.
Tel: 575-78-68, 575-79-24

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Avda Brigadeiro Faria Lima 844
11 Andar Conjunto 1104
Jardim Paulistano
Sao Paulo, Brasil
Telex: 1121008 CABINE SAO PAULO

National Semiconductor GmbH
Eisenheimerstrasse 61-II
8000 München 21
West Germany
Tel: (089) 576091
Telex: 05-22772

National Semiconductor (UK) Ltd.
301 Harpur Centre
Horne Lane
Bedford MK40 1TR
United Kingdom
Tel: 0234-47147
Telex: 826 209

National Semiconductor
789 Ave. Houba de Strooper
1020 Bruxelles
Belgium
Tel: (02) 4783400
Telex: 61007

National Semiconductor Ltd.
Vodroffsvej 44
1900 Copenhagen V
Denmark
Tel: (01) 356533
Telex: 15179

National Semiconductor France
Expansion 10000
28, rue de la Redoute
92-260 Fontenay aux Roses
France
Tel: 660.81.40
Telex: NSF250956

National Semiconductor SRL
Via Alberto Mario 26
20149 Milano
Italy
Tel: (02) 469 28 64/469 24 31
Telex: 332835

National Semiconductor Sweden
Algrytevagen 23
S-127 32 Skarholmen
Sweden
Tel: (8) 970835
Telex: 10731

NS International Inc., Japan
Miyake Building
1-9 Yotsuya, Shinjuku-ku 160
Tokyo, Japan
Tel: (04) 355-5711
TWX: 232-2015 JSCJ-J

National Semiconductor (Hong Kong) Ltd.
8th Floor,
Cheung Kong Electronic Bldg.
4 Hing Yip Street
Kwun Tong
Kowloon, Hong Kong
Tel: 3-899235
Telex: 73866 NSEHK HX
Cable: NATSEMI

NS Electronics Pty. Ltd.
Cnr. Stud Rd. & Mtn. Highway
Bayswater, Victoria 3153
Australia
Tel: 03-729-6333
Telex: 32096

National Semiconductor (Pty.) Ltd.
No. 1100 Lower Delta Road
Singapore 3
Tel: 2700011
Telex: NAT SEMI RS 21402

National Semiconductor (Taiwan) Ltd.
3rd Floor, Apollo Bldg.,
No. 218-7 Chung Shiao E. Road,
Sec 4, Taipei, Taiwan
P.O. Box 68-332 Taipei
Tel: 7310393-4, 7310465-6
Telex: 22837 NSTW
Cable: NSTW Taipei

National Semiconductor (Hong Kong) Ltd.
Korea Liaison Office
Rm. 607, 615 Seoul Bldg.
6,2 Ka Huehyun-Dong Bldg.
C.P.O. Box 7941
Jung Ku, Seoul 100
Korea
Tel: 28-4746

DA-GP1M39/Printed in U.S.A.