Communication Solutions

SYM92C1000 Ethernet/IEEE 802.3 Media Access Controller with MII, 100Base-TX, and 10Base-T Interface

Release 1.0

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FAST Ethernet Media Access Controller with MII, 100BASE-TX, and 10BASE-T Interfaces

FEATURES

- Supports the EtherCore™ design methodology
- Supports the IEEE 802.3 standards for Media Independent Interface (MII), 100BASE-TX and 10BASE-T
- Supports IEEE 1149.1 standards for JTAG boundary-scan testing
- Accepts broadcast and multicast packets
- Supports automatic re-transmission after collisions without software intervention
- Programmable CRC generation
- Supports half- or full-duplex operation
- Provides statistics vectors for both transmit and receive modes
- 128-pin PQFP package
- Programmable pad insertion
- Programmable interframe spacing (IFS)
- Programmable huge packet support
- Supports programmable late collision retry
- Programmable 100BASE-TX ciphering/deciphering
- 100BASE-TX 4B/5B encoding/decoding
- 10BASE-T serializer/deserializer
- Optimized for hub and switched applications, no address comparison logic
- I/O mux for MII, TP-PMD or 10BASE-T operation
- Separate 8-bit receive and transmit ports, 16-bit host I/O port for I/O and statistics register access

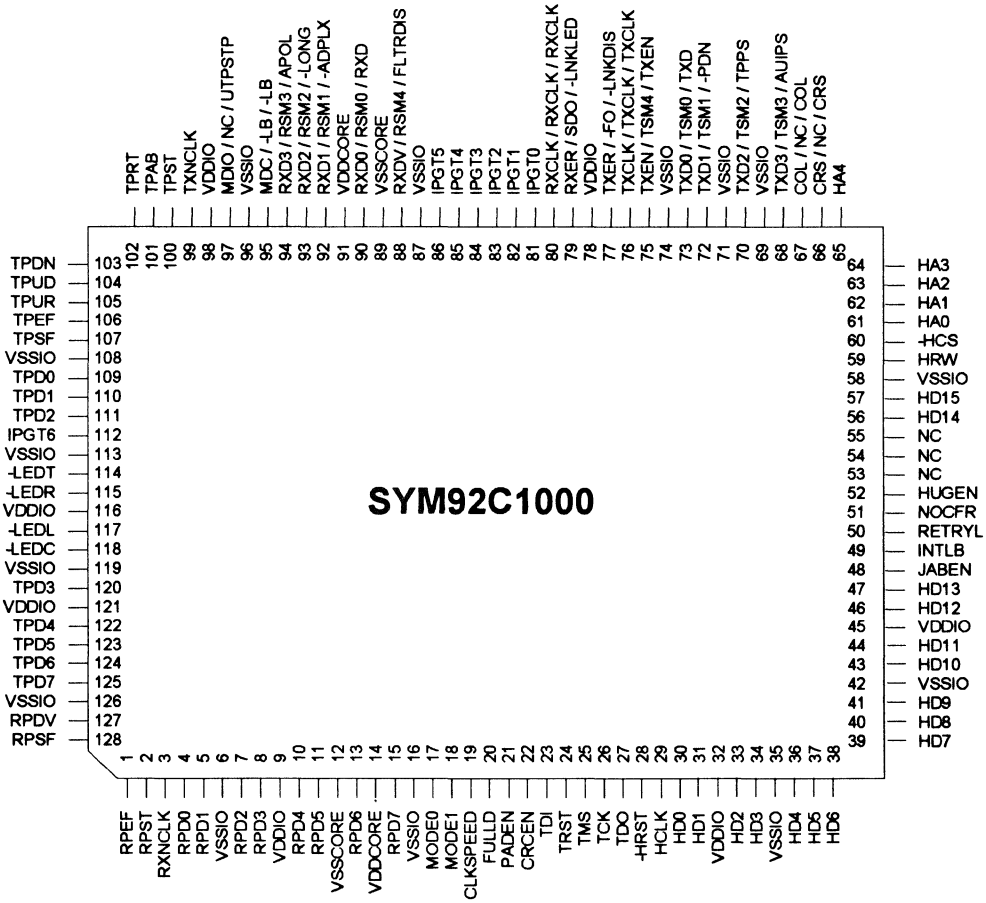


Figure 1 Pinout Diagram

Table 1 Pinout Summary

Pin	Signal Name	Type	Interface	Pin Description
1	RPEF	o	RX	Receive Packet End of Frame
2	RPST	o	RX	Receive Packet Status
3	RXNCLK	o	RX	Receive Nibble Clock (2.5 or 25 MHz)
4	RPD0	o	RX	Receive Data Bit 0
5	RPD1	o	RX	Receive Data Bit 1
6	VSSIO	io/gnd	-	
7	RPD2	o	RX	Receive Data Bit 2
8	RPD3	o	RX	Receive Data Bit 3
9	VDDIO	io/pwr	-	
10	RPD4	o	RX	Receive Data Bit 4
11	RPD5	o	RX	Receive Data Bit 5
12	VSSCORE	c/gnd	-	
13	RPD6	o	RX	Receive Data Bit 6
14	VDDCORE	c/pwr	-	
15	RPD7	o	RX	Receive Data Bit 7
16	VSSIO	io/gnd	-	
17	MODE0	i	CONFIG	Mode Bit 0
18	MODE1	i	CONFIG	Mode Bit 1
19	CLKSPEED	i	CONFIG	Host Clock Speed Select
20	FULLD	i	CONFIG	Full-Duplex Enable
21	PADEN	i	CONFIG	Pad Enable
22	CRCEN	i	CONFIG	CRC Enable
23	TDI	i	JTAG	Test Data In
24	TRST	i	JTAG	Test Reset
25	TMS	i	JTAG	Test Mode Select
26	TCK	i	JTAG	Test Clock
27	TDO	o	JTAG	Test Data Out
28	-HRST	i	HOST	Reset active low
29	HCLK	i	HOST	33 MHz maximum Host Clock
30	HD0	t/s	HOST	Host Data Bit 0
31	HD1	t/s	HOST	Host Data Bit 1
32	VDDIO	io/pwr	-	
33	HD2	t/s	HOST	Host Data Bit 2
34	HD3	t/s	HOST	Host Data Bit 3
35	VSSIO	io/gnd	-	
36	HD4	t/s	HOST	Host Data Bit 4
37	HD5	t/s	HOST	Host Data Bit 5
38	HD6	t/s	HOST	Host Data Bit 6
39	HD7	t/s	HOST	Host Data Bit 7
40	HD8	t/s	HOST	Host Data Bit 8
41	HD9	t/s	HOST	Host Data Bit 9
42	VSSIO	io/gnd	-	
43	HD10	t/s	HOST	Host Data Bit 10
44	HD11	t/s	HOST	Host Data Bit 11
45	VDDIO	io/pwr	-	
46	HD12	t/s	HOST	Host Data Bit 12
47	HD13	t/s	HOST	Host Data Bit 13
48	JABEN	i	CONFIG	Jabber Enable

Pin	Signal Name	Type	Interface	Pin Description
49	INTLB	i	CONFIG	Internal Loopback Enable
50	RETRYL	i	CONFIG	Late Retry Enable
51	NOCFR	i	CONFIG	No Ciphering
52	HUGEN	i	CONFIG	Huge Packet Enable
53	NC	-	-	No Connect
54	NC	-	-	No Connect
55	NC	-	-	No Connect
56	HD14	t/s	HOST	Host Data Bit 14
57	HD15	t/s	HOST	Host Data Bit 15
58	VSSIO	io/gnd	-	
59	HRW	i	HOST	Read Write
60	-HCS	i	HOST	Chip Select active low
61	HA0	i	HOST	Host Address Bit 0
62	HA1	i	HOST	Host Address Bit 1
63	HA2	i	HOST	Host Address Bit 2
64	HA3	i	HOST	Host Address Bit 3
65	HA4	i	HOST	Host Address Bit 4
66	Multimode	-		Refer To Specific Mode Pin Description Table
67	Multimode	-		Refer To Specific Mode Pin Description Table
68	Multimode	-		Refer To Specific Mode Pin Description Table
69	VSSIO	io/gnd	-	
70	Multimode	-		Refer To Specific Mode Pin Description Table
71	VSSIO	io/gnd	-	
72	Multimode	-		Refer To Specific Mode Pin Description Table
73	Multimode	-		Refer To Specific Mode Pin Description Table
74	VSSIO	io/gnd	-	
75	Multimode	-		Refer To Specific Mode Pin Description Table
76	Multimode	-		Refer To Specific Mode Pin Description Table
77	Multimode	-		Refer To Specific Mode Pin Description Table
78	VDDIO	io/pwr	-	
79	Multimode	-		Refer To Specific Mode Pin Description Table
80	Multimode	-		Refer To Specific Mode Pin Description Table
81	IPGT0	i	CONFIG	Back-to-Back IPG Bit 0
82	IPGT1	i	CONFIG	Back-to-Back IPG Bit 1
83	IPGT2	i	CONFIG	Back-to-Back IPG Bit 2
84	IPGT3	i	CONFIG	Back-to-Back IPG Bit 3
85	IPGT4	i	CONFIG	Back-to-Back IPG Bit 4
86	IPGT5	i	CONFIG	Back-to-Back IPG Bit 5
87	VSSIO	io/gnd	-	
88	Multimode	-		Refer To Specific Mode Pin Description Table
89	VSSCORE	c/gnd	-	
90	Multimode	-		Refer To Specific Mode Pin Description Table
91	VDDCORE	c/pwr	-	
92	Multimode	-		Refer To Specific Mode Pin Description Table
93	Multimode	-		Refer To Specific Mode Pin Description Table
94	Multimode	-		Refer To Specific Mode Pin Description Table
95	Multimode	-		Refer To Specific Mode Pin Description Table
96	VSSIO	io/gnd	-	
97	Multimode	-		Refer To Specific Mode Pin Description Table

Pin	Signal Name	Type	Interface	Pin Description
98	VDDIO	io/pwr	-	
99	TXNCLK	o	TX	Transmit Nibble Clock (2.5, 10, or 25 MHz)
100	TPST	o	TX	Transmit Packet Status
101	TPAB	o	TX	Transmit Packet Abort
102	TPRT	o	TX	Transmit Packet Retry
103	TPDN	o	TX	Transmit Packet Done
104	TPUD	o	TX	Transmit Packet Used Data
105	TPUR	i	TX	Transmit Packet Underrun
106	TPEF	i	TX	Transmit Packet End of Frame
107	TPSF	i	TX	Transmit Packet Start of Frame
108	VSSIO	io/gnd	-	
109	TPD0	i/o	TX	Transmit Data bit 0
110	TPD1	i/o	TX	Transmit Data bit 1
111	TPD2	i/o	TX	Transmit Data bit 2
112	IPGT6	i	CONFIG	Back-to-Back IPG Bit 6
113	VSSIO	io/gnd	-	
114	-LEDT	od	LED	Transmit LED
115	-LEDR	od	LED	Receive LED
116	VDDIO	io/pwr	-	
117	-LEDL	od	LED	Link LED
118	-LEDC	od	LED	Collision LED
119	VSSIO	io/gnd	-	
120	TPD3	i/o	TX	Transmit Data bit 3
121	VDDIO	io/pwr	-	
122	TPD4	i/o	TX	Transmit Data bit 4
123	TPD5	i/o	TX	Transmit Data bit 5
124	TPD6	i/o	TX	Transmit Data bit 6
125	TPD7	i/o	TX	Transmit Data bit 7
126	VSSIO	io/gnd	-	
127	RPDV	o	RX	Receive Packet Data Valid
128	RPSF	o	RX	Receive Packet Start of Frame

Table 2 MII Mode Pinout Summary

Pin No.	Signal Name	Type	Pin Description
66	CRS	i	Carrier Sense
67	COL	i	Collision
68	TXD3	o	Transmit Data Bit 3
70	TXD2	o	Transmit Data Bit 2
72	TXD1	o	Transmit Data Bit 1
73	TXD0	o	Transmit Data Bit 0
75	TXEN	o	Transmit Enable
76	TXCLK	i	Transmit Clock
77	TXER	o	Transmit Error
79	RXER	i	Receive Error
80	RXCLK	i	Receive Clock
88	RXDV	i	Receive Data Valid
90	RXD0	i	Receive Data Bit 0
92	RXD1	i	Receive Data Bit 1
93	RXD2	i	Receive Data Bit 2
94	RXD3	i	Receive Data Bit 3
95	MDC	o	Management Data Clock
97	MDIO	i/o	Management Data

Table 3 TP-PMD Mode Pinout Summary

Pin No.	Signal Name	Type	Pin Description
66	NC	-	No Connect (this pin should be tied either high or low)
67	NC	-	No Connect (this pin should be tied either high or low)
68	TSM3	o	Transmit Data Bit 3
70	TSM2	o	Transmit Data Bit 2
72	TSM1	o	Transmit Data Bit 1
73	TSM0	o	Transmit Data Bit 0
75	TSM4	o	Transmit Data Bit 4
76	TXCLK	i	Transmit Clock
77	-FO	o	Fiber Optic Off (active low)
79	SDO	i	Signal Detect
80	RXCLK	i	Receive Clock
88	RSM4	i	Receive Data Bit 4
90	RSM0	i	Receive Data Bit 0
92	RSM1	i	Receive Data Bit 1
93	RSM2	i	Receive Data Bit 2
94	RSM3	i	Receive Data Bit 3
95	-LB	o	Loopback (active low)
97	NC	-	No Connect (this pin should be tied either high or low)

Table 4 10BASE-T Mode Pinout Summary

Pin No.	Signal Name	Type	Pin Description
66	CRS	i	Carrier Sense
67	COL	i	Collision
68	AUIPS	o	AUI Port Select
70	TPPS	o	TP Port Select
72	-PDN	o	Powerdown Enable (active low)
73	TXD	o	Transmit Data
75	TXEN	o	Transmit Enable
76	TXCLK	i	Transmit Clock
77	-LNKDIS	o	Link Disable (active low)
79	-LNKLED	i	Link Pulse (active low)
80	RXCLK	i	Receive Clock
88	FLTRDIS	o	Filter Disable
90	RXD	i	Receive Data
92	-ADPLX	o	Autoduplex Enable (active low)
93	-LONG	o	Long Cable Mode (active low)
94	APOL	o	Autopolarity Enable
95	-LB	o	Loopback Enable (active low)
97	UTPSTP	o	Cable Type Select

Table 5 Pin Type Descriptions

Type	Description
c/pwr	Core Logic Power: a +5 V connection providing power to digital core logic.
c/gnd	Core Logic Ground: a ground connection to the digital core logic.
io/pwr	I/O Driver Power: a +5 V connection providing power to the I/O drivers.
io/gnd	I/O Driver Ground: a ground connection to the I/O drivers.
i	Input: a standard input signal.
o	Output: a standard output signal.
i/o	Input/Output: a standard input/output signal.
od	Open Drain: a switched ground connection for LEDs.
t/s	Tristate: a bi-directional, tristate input/output signal.

GENERAL DESCRIPTION

The SYM92C1000 is a half- or full-duplex, high-performance Local Area Network (LAN) 10 Mbps or 100 Mbps Media Access Controller (MAC) that supports the IEEE 802.3 specifications for Ethernet LANs. The SYM92C1000 MAC controls the network parameters of an IEEE 802.3 network and supports network management with network counters and status vectors. The SYM92C1000 supports 5 volt LAN environments.

The SYM92C1000 is designed to operate in one of three physical layer (PHY) interface modes; 10-100 Mbps Media Independent Interface (MII), 100 Mbps Twisted Pair - Physical Media Dependent (TP-PMD, used for 100BASE-TX or fiber optics), or 10 Mbps 10BASE-T. The SYM92C1000 is optimized for switched applications and does not perform address comparison.

The SYM92C1000 supports a variety of programmable options including; pad insertion for small data packets, huge packet enable to allow transmission and reception of oversize packets, an Inter Packet Gap (IPG) specifier to customize system performance, late collision retry, and 100BASE-TX ciphering and deciphering.

The SYM92C1000 meets the IEEE 802.3 retransmission specifications by automatically retransmiting packets experiencing a collision up to fifteen times without software intervention. After sixteen failed attempts for a single packet the SYM92C1000 aborts the transmission and notifies the host of the failed packet transmission.

In TP-PMD mode, the SYM92C1000 supports 4-bit to 5-bit conversion to provide sufficient transition density to facilitate clock recovery when not in cipher mode. In 10BASE-T mode, the SYM92C1000 performs bit serialization and deserialization to present and receive IEEE 802.3 standard data for an external Manchester encoder/decoder (MENDEC).

The SYM92C1000 supports optional Cyclic Redundancy Checking (CRC) insertion on transmit for data verification. When the SYM92C1000 is used in a node network adapter card application, the CRC is used to ensure the transmitted and received data is valid. When the SYM92C1000 is used in either a hub or a repeater application, the CRC must be disabled, allowing the original CRC to pass through to the destination for the final data check.

The SYM92C1000 supports the Symbios Logic EtherCore design methodology. The block approach to core designs provides the flexibility to develop an Ethernet system to meet specific needs.

Symbios Logic EtherCore products are sold as standard products for quick time-to-market designs. This family of EtherCore products is developed and supported by Symbios Logic ASIC design tools for built-in cost reduction through integration.

SYSTEM OVERVIEW

Figure 2 shows a typical system implementation using the SYM92C1000. The system is comprised of the SYM92C1000, Buffer Management Unit, Host Interface Controller (HIC), and the Physical Layer Device (PHY) .

SYM92C1000 Media Access Controller

The SYM92C1000 performs all the MAC functions of the system, including 100 Mbps transmit and receive, 10 Mbps transmit and receive, collision monitoring and retransmission, pad insertion, CRC generation, CRC verification and IPG management.

Buffer Management Unit

The Buffer Management Unit temporarily stores the LAN data as it passes between the MAC and the Host System Bus and typically consists of a FIFO and control logic.

Host Interface Controller

The Host Interface Controller (HIC) is the communications port between the SYM92C1000 and the host system and receives configuration instructions from the host and returns configuration information as well as transmit and receive status upon request.

Physical Layer Device

The Physical Layer Device (PHY) has three possible configurations; MII, TP-PMD, and 10BASE-T modes. In MII mode, the PHY consists of circuitry to convert 4-bit MII frame data from the SYM92C1000 into serial data that is media-ready. In TP-PMD mode, the PHY converts the frame data from encoded, ciphered 5-bit 25 MHz format presented by the SYM92C1000 to 125 MHz serialized 100BASE-TX data that is media-ready. In 10BASE-T mode, the PHY takes the 10 MHz serial data from the SYM92C1000, Manchester encodes it and makes it media-ready. Typically the PHY requires encoder, transceiver , filters, and magnetics.

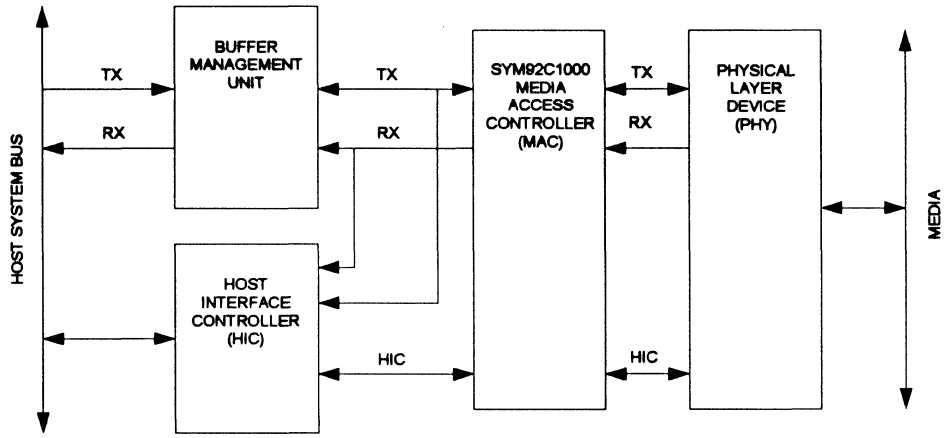


Figure 2 Typical System Implementation

PIN DESCRIPTIONS

FIXED PIN DESCRIPTIONS

On the SYM92C1000, 110 of the 128 pins have a fixed functionality in all three modes of operation (MII, TP-PMD, or 10BASE-T), these pins are listed here. The pin descriptions for the remaining 18 pins from the multiplexed I/O have three different mode options (MII, TP-PMD, or 10BASE-T) depending on configuration and are listed in individual pin description sections related to each mode.

CLKSPEED: Host Clock Speed Select:
This configuration input is tied high to inform the SYM92C1000 that the host clock rate is between 25 MHz and 33 MHz, a low input indicates a clock rate less than or equal to 25 MHz. This pin is valid only in MII mode and has a weak internal pulldown, if left unconnected this function defaults to clock speed less than or equal to 25 MHz. Configuration pins are used to load startup data to the Configuration Register, the contents of the register can be overwritten at any time with new values.

CRCEN: Cyclic Redundancy Check Enable
This configuration input is used to enable CRC error generation. The SYM92C1000 will continuously calculate the CRC and append the result to the end of the transmit packet. If PADEN is set, CRCEN is ignored and a CRC is generated. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset. Configuration pins are used to load startup data to the Configuration Register, the contents of the register can be overwritten at any time with new values.

FULLD: Full Duplex Enable
This configuration input is used to put the SYM92C1000 into full duplex operation. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset. Configuration pins are used to load startup data to the Configuration Register, the contents of the register can be overwritten at any time with new values.

HA(4:0): Host Address Bus
These five input lines are used to address the internal registers of the SYM92C1000.

HCLK: Host Clock
This input is used as the 33 MHz maximum host interface clock.

-HCS: Host Chip Select
This active-low input is driven low to enable the reading and writing of data in the internal registers of the SYM92C1000 in conjunction with HRW.

HD(15:0): Host Data Bus
These sixteen bi-directional lines are used to transfer data between the external host and the internal registers of the SYM92C1000. HD(15:0) is in the tristate condition when not in read mode.

-HRST: Host Reset
This active-low asynchronous input is driven low to force the SYM92C1000 into an idle state and reset all internal registers to default values. -HRST must be held low for a minimum of 20 HCLK cycles and allowed an additional 20 cycles to complete the reset procedure before normal operations resume. For power-on reset with the configuration interface pins unconnected, -HRST must be held low for a minimum of 150 HCLK cycles and then allowed an additional 20 cycles before normal operations begin.

HRW: Host Read/Write Select
This input is used to select read or write operation. Driving HRW high allows read operations and driving HRW low allows write operations.

HUGEN: Huge Packet Enable
This configuration input is used to enable the SYM92C1000 to transmit and receive packets with more than the IEEE maximum of 1518 bytes. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset. Configuration pins are used to load startup data to the Configuration Register, the contents of the register can be overwritten at any time with new values.

INTLB: Internal Loopback Enable
The SYM92C1000 has internal loopback capability, setting this configuration input will cause the MAC to begin internal loopback. The SYM92C1000 does not need to be in full duplex mode to perform internal loopback. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset. Configuration pins are used to load startup data to the Configuration Register, the contents of the register can be overwritten at any time with new values.

IPGT (6:0): Back-To-Back Interpacket Gap
These configuration inputs are used to provide the reset value for the Back-to-Back Interpacket Gap register. IPGT(4:3) have weak internal pullups, the others have weak internal pulldowns. This provides a reset value of 0x18 (960 ns in 100 Mbps mode, 2.4 μs in 10 Mbps mode) when left unconnected. Configuration pins are used to load startup data to the Configuration Register, the contents of the register can be overwritten at any time with new values.

JABEN: Jabber Enable
This configuration input is used to enable the SYM92C1000 jabber logic at reset. If the SYM92C1000 transmits continuously for 20 ms it will abort the transmission and drive TXEN low to block all transmissions for 250 ms. This configuration is valid only in 10BASE-T mode. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset. Configuration pins are used to load startup data to the Configuration Register, the contents of the register can be overwritten at any time with new values.

-LEDC: Collision LED
This open-drain output is driven low when the SYM92C1000 detects a collision. When not active it is in a high impedance state. This output is stretched to 30 ms.

-LEDL: Link LED
This open-drain output is driven low when the SYM92C1000 detects link. When not active it is in a high impedance state. This output is stretched to 30 ms. In MII mode the MII Request Register bit 1 (SCAN) must be set to 1 for this output to be valid.

-LEDR: Receive LED
This open-drain output is driven low when the SYM92C1000 is receiving. When not active it is in a high impedance state. This output is stretched to 30 ms.

-LEDT: Transmit LED
This open-drain output is driven low when the SYM92C1000 is transmitting. When not active it is in a high impedance state. This output is stretched to 30 ms.

MODE(1:0): Mode Select
This configuration input is used to select the reset configuration of the multiplexed I/O interface. 00 selects MII mode, 01 selects TP-PMD mode, and 10 selects 10BASE-T mode. These pins have a weak internal pulldown, if left unconnected the SYM92C1000 defaults to MII mode. Configuration pins are used to load startup data to the Configuration Register, the contents of the register can be overwritten at any time with new values.

NOCFR: No Ciphering
This configuration input disables the ciphering function in TP-PMD mode. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset and ciphering will occur. Configuration pins are used to load startup data to the Configuration Register, the contents of the register can be overwritten at any time with new values.

PADEN: Pad Enable
This configuration input is used to instruct the SYM92C1000 to pad with zeros any short packets out to the IEEE minimum of 64 bytes after reset. It is up to the receive software to read the packet length field and strip off added padding. In the Pad Enable mode, a CRC is generated regardless of CRCEN. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset. Configuration pins are used to load startup data to the Configuration Register, the contents of the register can be overwritten at any time with new values.

RETRYL: Late Collision Retry
This configuration input is used to instruct the SYM92C1000 to allow late collision retries. A late collision occurs more than 512 bit times after the start of a transmission and indicates a mis-configured network topology. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset. Configuration pins are used to load startup data to the Configuration Register, the contents of the register can be overwritten at any time with new values.

RPD(7:0): Receive Packet Data Bus
These eight outputs are used to transfer the receive data byte and the receive status byte from the SYM92C1000 to the external buffer management unit.

RPDV: Receive Packet Data Valid
This output is driven high when a valid receive data byte is on RPD(7:0).

RPEF: Receive Packet End of Frame
This output is driven high at the end of the receive packet.

RPSF: Receive Packet Start of Frame
This output is driven high at the start of the receive packet.

RPST: Receive Packet Status
This output is driven high when a valid receive status byte is on RPD(7:0).

RXNCLK: Receive Nibble Clock
This output is the 25 MHz or 2.5 MHz (depending on 100 Mbps or 10 Mbps data rate) nibble receive clock to synchronize receive data for the external buffer management unit. All receive interface signals from the SYM92C1000 to the Receive Buffer Management Unit are synchronous to RXNCLK.

TCK: Test Clock
This input is the JTAG clock and is limited to 10 MHz maximum. It is used to shift test data and JTAG control information into and out of the SYM92C1000 during JTAG test operations. This pin should not be left floating, if JTAG is not used tie TCK to ground.

TDI: Test Data In
This input is the JTAG serial data input, it is used to shift test data and instructions into the SYM92C1000 during a JTAG test. This pin has a weak internal pullup and may be left unconnected if JTAG is not used.

TDO: Test Data Out
This output is the JTAG serial data output, it is used to shift test data and instructions out of the SYM92C1000 during a JTAG test.

TMS: Test Mode Select
This input is the JTAG mode select, it is used to control the state operation of the SYM92C1000 during a JTAG test. This input has a weak internal pullup and may be left unconnected if JTAG is not used.

TPAB: Transmit Packet Abort
This output is driven high when a normal transmission is aborted due to TPUR being asserted by the buffer management unit. During a retransmit, indicated by TPRT, the transmission may still be aborted by asserting TPUR but TPAB will not be driven high and no abort will be indicated by this pin.

TPD(7:0): Transmit Packet Data Bus
These eight bi-directional lines are used to transfer the transmit data byte from the external buffer management unit to the SYM92C1000. After transmission these lines transfer the transmit status bytes from the SYM92C1000 to the external buffer management unit. TPD(7:0) is in a tristate condition when not driven by the SYM92C1000 or the external buffer management unit.

TPDN: Transmit Packet Done
This output is driven high when the SYM92C1000 has finished a normal packet transmission.

TPEF: Transmit Packet End of Frame
This input is driven high coincident with data loaded into TPD(7:0) to indicate the current byte is the end of a packet.

TPRT: Transmit Packet Retry
This output is driven high when a collision has occurred and retransmission of the packet is required.

TPSF: Transmit Packet Start of Frame
This input is driven high to start a packet transmission.

TPST: Transmit Packet Status
This output is driven high when valid transmit status bytes are on TPD(7:0).

TPUD: Transmit Packet Data Used
This output is driven high when data transmission has begun on the media.

TPUR: Transmit Packet Underrun
This input is driven high to abnormally end a packet transmission. This signal causes TPAB to be asserted except when TPRT is asserted.

-TRST: Test Reset
This active-low input is the JTAG reset. This input has a weak internal pullup, if JTAG is not used or TCK is not clocked then tie -TRST to ground. If JTAG is used then -TRST needs to be held low during chip reset.

TXNCLK: Transmit Nibble Clock
This output is the 25 MHz, 10 MHz, or 2.5 MHz (depending on 100 Mbps or 10 Mbps data rate) nibble transmit clock for synchronizing data from the external buffer management unit. All transmit interface signals between the Transmit Buffer Management Unit and the SYM92C1000 are synchronous to TXNCLK.

VDDCORE: Logic Core Power
These pins provide +5 volts to the digital logic core.

VDDIO: IO Driver Power
These pins provide +5 volts to the I/O drivers.

VSSCORE: Logic Core Ground
These pins provide the ground connection for the digital logic core.

VSSIO: IO Driver Ground
These pins provide the ground connection for the I/O drivers.

MULTIPLEXED PIN DESCRIPTIONS

MII Mode Pin Descriptions

COL: MII Collision
This asynchronous input is driven high for two TXCLK periods minimum when the external MII PHY detects a collision.

CRS: MII Carrier Sense
This asynchronous input is driven high for two TXCLK periods minimum by the external MII PHY when either the transmit or receive medium is active.

MDC: MII Management Clock
This output is the 2.5 MHz or less reference clock for the management data.

MDIO: MII Management Data
This bi-directional line is used to transfer the management data between the SYM92C1000 and the external MII PHY.

RXCLK: MII Receive Clock
This input is the 2.5-25 MHz nibble receive clock from the external MII PHY. All PHY receive signals to the SYM92C1000 are synchronous to RXCLK.

RXD(3:0): MII Receive Data Bus
These four inputs are used to transfer the receive data nibble from the external MII PHY to the SYM92C1000.

RXDV: MII Receive Data Valid
This input is driven high when a valid receive data nibble is on RXD(3:0).

RXER: MII Receive Error
This input is driven high when there is an error on the receive data stream.

TXCLK: MII Transmit Clock
This input is the 2.5-25 MHz nibble transmit clock from the external MII PHY. All PHY transmit signals from the SYM92C1000 are synchronous to TXCLK.

TXD(3:0): MII Transmit Data Bus
These four outputs are used to transfer the transmit data nibble from the SYM92C1000 to the external MII PHY.

TXEN: MII Transmit Enable
This output is driven high when a valid transmit data nibble is on TXD(3:0).

TXER: MII Transmit Error
This output is driven high when there is an error on the transmit data stream.

TP-PMD Mode Pin Descriptions

-FO: TP-PMD Fiber Optic Off
This active-low output is driven low to turn off an external TP-PMD PHY fiber optic transmit circuit. This signal is controlled directly by the TP-PMD Control Register bit -FO.

-LB: TP-PMD Loopback
This active-low output is driven low to perform the loopback function in the external TP-PMD PHY. This signal is controlled directly by the TP-PMD Control Register bit -LB. External loopback can only occur when the SYM92C1000 is in full duplex mode.

RSM(4:0): TP-PMD Receive Data Bus
These five inputs are used to transfer data from the external TP-PMD PHY to the SYM92C1000.

RXCLK: TP-PMD Receive Clock
This input is the 25 MHz symbol receive clock from the external TP-PMD PHY. All PHY receive signals to the SYM92C1000 are synchronous to RXCLK.

SDO: TP-PMD Signal Detect
This input is driven high by the TP-PMD PHY when there is activity on the network.

TSM(4:0): TP-PMD Transmit Data Bus
These five outputs are used to transfer data from the SYM92C1000 to the external TP-PMD PHY.

TXCLK: TP-PMD Transmit Clock
This input is the 25 MHz symbol transmit clock from the external TP-PMD PHY. All PHY transmit signals from the SYM92C1000 are synchronous to TXCLK.

10BASE-T Mode Pin Descriptions

-ADPLX: 10BASE-T Autoduplex Enable/Jabber Disable
This active-low output is typically used to disable an autoduplex function and enable a jabber function on the external 10BASE-T PHY (note, the SYM92C1000

does not support autoduplex). This pin is controlled from the 10BASE-T Control Register bit -ADPLX.

APOL: 10BASE-T Autopolarity Enable
This output is typically driven high to enable an external 10BASE-T PHY autopolarity function. This pin is controlled from the 10BASE-T Control Register bit APOL.

AUIPS: 10BASE-T AUI Port Select
This output is typically used in conjunction with TPPS to select the output port on an external 10BASE-T PHY (see Table 6). This pin is controlled from the 10BASE-T Control Register bit AUIPS.

COL: 10BASE-T Collision
This asynchronuous input is driven high by the 10BASE-T PHY for two TXCLK periods minimum when a collision has been detected on the network.

CRS: 10BASE-T Carrier Sense
This input is driven high by the 10BASE-T PHY when there is activity on the network.

FLTRDIS: 10BASE-T Filter Disable
This output is typically driven high to disable an external 10BASE-T PHY transmit and receive filter function. This pin is controlled from the 10BASE-T Control Register bit -FLTRDIS.

-LB: 10BASE-T Loopback Enable/SQE Disable
This active-low output is typically used to enable the loopback or SQE functions on an external 10BASE-T PHY. This pin is controlled from the 10BASE-T Control Register bit -LB. External loopback can only occur when the SYM92C1000 is in full duplex mode.

-LNKDIS: 10BASE-T Link Disable
This active-low output is typically driven low to disable the external 10BASE-T PHY link pulse function. This pin is controlled from the 10BASE-T Control Register bit -LNKDIS.

-LNKLED: 10BASE-T Link Pulse
This asynchronuous input is driven low by the external 10BASE-T PHY Link LED driver for two TXCLK periods minimum when it detects a link pulse on the twisted pair receive input.

-LONG: 10BASE-T Long Cable Mode
This active-low output is typically driven low to enable a long cable mode in an external 10BASE-T PHY Long cable is defined as cable lengths in excess of 100 meters. This pin is controlled from the 10BASE-T Control Register bit -LONG.

-PDN: 10BASE-T Powerdown Enable
This active-low output is typically driven low to disable all PHY functions and lower power consumption to a minimum. This pin is controlled from the 10BASE-T Control Register bit -PDN.

RXCLK: 10BASE-T Receive Clock
This input is the 10 MHz receive clock from the external 10BASE-T PHY. This clock input must be continuous. All PHY receive signals to the SYM92C1000 are synchronous to RXCLK.

RXD: 10BASE-T Receive Data
This input is used to transfer received data from the external 10BASE-T PHY to the SYM92C1000.

TPPS: 10BASE-T TP Port Select
The outputs TPPS and AUIPS are typically used to select the output port on an external 10BASE-T device as listed in Table 6. These pins are controlled from the 10BASE-T Control Register bits AUIPS and TPPS.

Table 6 Typical AUIPS/TPPS Port Selection

AUIPS	TPPS	Function
0	0	Automatic port selection enabled when -LNKDIS =1
0	1	TP port selected
1	0	AUI port selected
1	1	Invalid

TXCLK: 10BASE-T Transmit Clock
This input is the 10 MHz transmit clock from the external 10BASE-T PHY. All PHY transmit signals from the SYM92C1000 are synchronous to TXCLK.

TXD: 10BASE-T Transmit Data
This output is used to transfer transmit data from the SYM92C1000 to the external 10BASE-T PHY.

TXEN: 10BASE-T Transmit Enable
This output is driven high when valid data is on TXD.

UTPSTP: 10BASE-T Cable Type Select
This output is typically used to adjust the external 10BASE-T PHY transmit output current level to accommodate either 100 Ω UTP cable or 150 Ω STP cable. This signal is driven high to select UTP cable and low to select STP cable. This pin is controlled from the 10BASE-T Control Register bit UTPSTP.

SYSTEM DESCRIPTION

The SYM92C1000 is divided into six primary interfaces: Host Interface, Buffer Interface, JTAG Interface, Configuration Interface, LED Interface, and Multiplexed Input/Output Interface. The Buffer Interface consists of a Transmit and a Receive Interface. The Multiplexed Output interface is user configured into one of three choices: MII Interface, TP-PMD Interface, or 10BASE-T Interface. Figure 3 provides an overview of the signals associated with the six primary interfaces, and Figure 4 details the signals associated with each of the three Multiplexed Output Interface options.

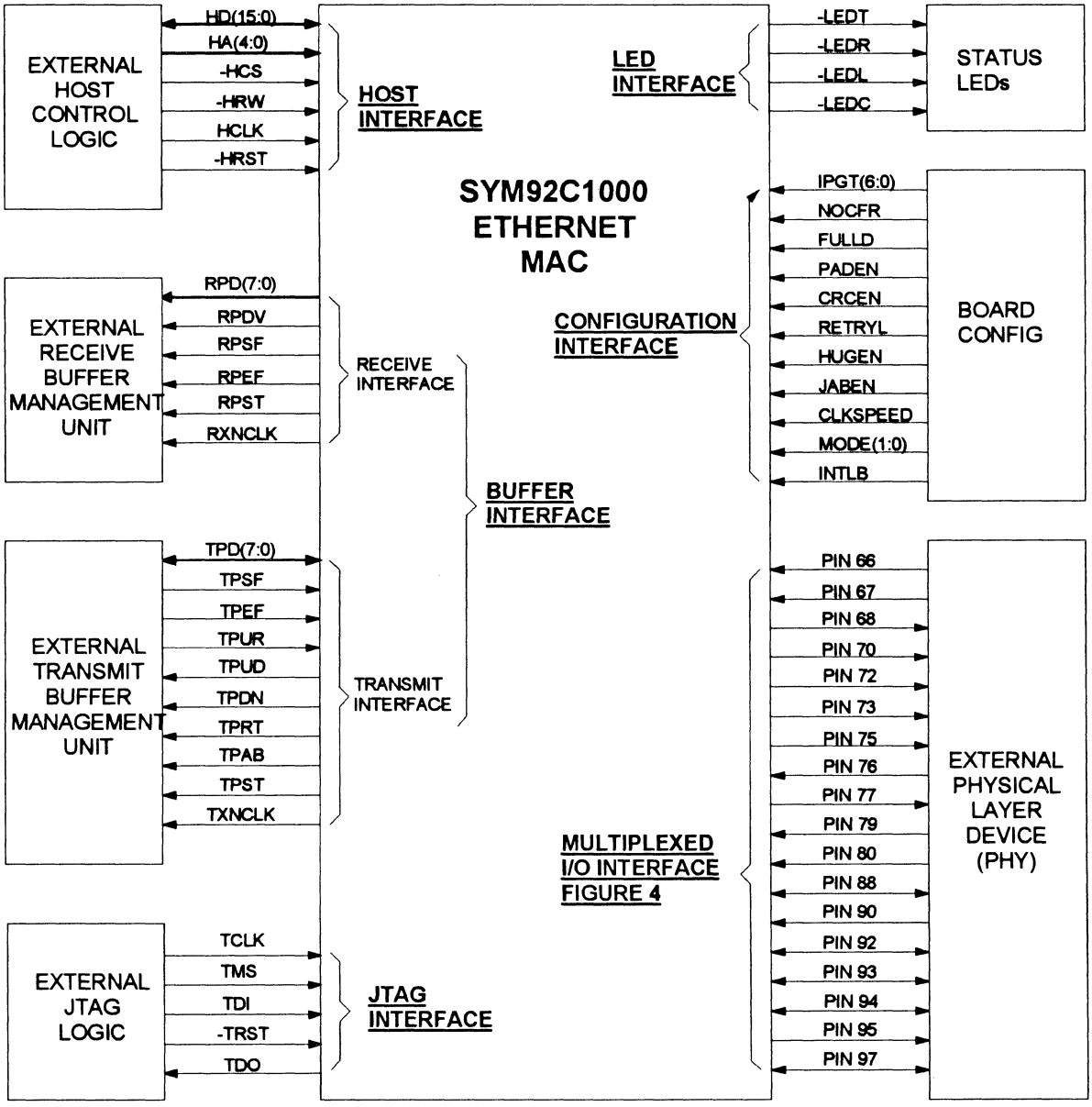


Figure 3 System Block Diagram

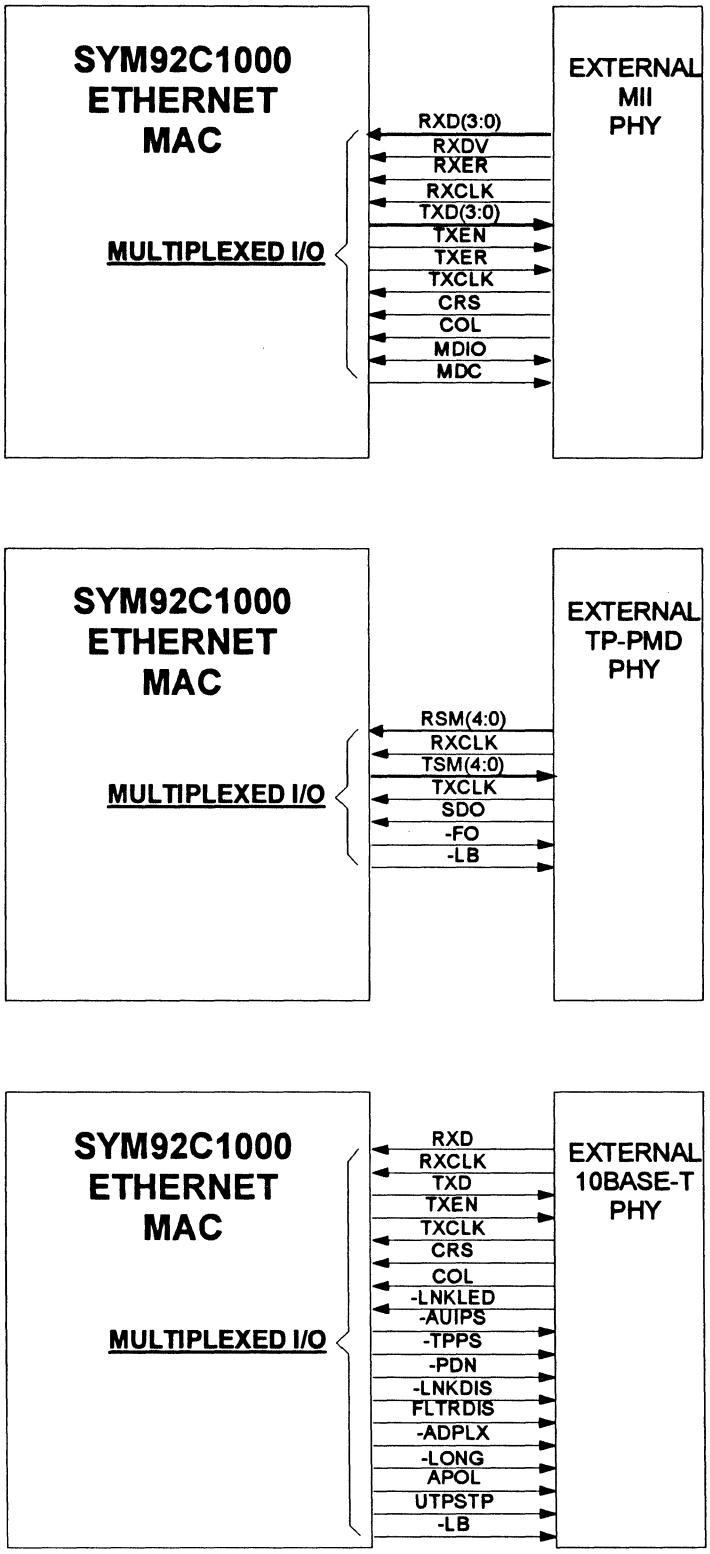


Figure 4 Three Options for Multiplexed I/O

HOST INTERFACE

The following signals are used in the Host Interface

Signal Name	Signal Definition
HA(4:0)	I/O Port Address Bus: These five input lines are used to address the internal registers of the SYM92C1000.
HCLK	Host Clock: This input is used as the 25-33 MHz host interface clock.
-HCS	Host Chip Select: This active-low input is driven low to enable the transfer of data from the internal registers of the SYM92C1000 to the host when HRW is high. When HRW is low, the transition from low to high on -HCS causes the data from the host to be latched into the addressed internal register of the SYM92C1000.
HD(15:0)	I/O Port Data Bus: These sixteen bi-directional lines are used to transfer data between the external host and the internal registers of the SYM92C1000. HD(15:0) is in the tri-state condition when not in read mode.
-HRST	Host Reset: This active-low asynchronous input is driven low to force the SYM92C1000 into an idle state and reset all internal registers to default values. -HRST must be held low for a minimum of 20 HCLK cycles and allowed an additional 20 cycles to complete the reset procedure before normal operations resume. For power-on reset with the configuration interface pins unconnected, -HRST must be held low for a minimum of 150 HCLK cycles and allowed an additional 20 cycles before normal operations begin.
HRW	Host Read/Write Select: This input is used to select read or write operation. Driving HRW high allows read operations and driving HRW low allows write operations.

The SYM92C1000 is controlled by writing to and reading from the 16 bit bi-directional data port HD(15:0). As shown in Table 7, commands, register status, and data are all issued or accessed through the port using the signals -HCS and HRW while the appropriate register address is held on HA(4:0).

Table 7 Read/Write Selection

-HCS	HRW	Operation
0	0	Write Register Port
0	1	Read Register Port
1	X	No Effect

I/O Register Read

For a register read, the External Host Control Logic must: drive the HRW pin high to enable the read function, drive the desired register address onto the HA(4:0) inputs and drive the -HCS input low to read the register contents. HRW, HA(4:0), and -HCS should remain stable through the read cycle (refer to Read Timing Diagrams).

I/O Register Write

For a register write, the External Host Control Logic must: drive the HRW input low to enable the write function, drive the desired register address onto the HA(4:0) inputs, and drive the desired command onto the HD(15:0) bi-directional pins. The register write occurs on the rising transition of the -HCS input, so HRW, HA(4:0), and HD(15:0) must be stable during this transition (refer to Write Timing Diagrams).

HCLK Input

The SYM92C1000 accepts input clock rates up to 33 MHz. For proper operation the Configuration Register bit 6 (CLKSPD) must be set to 0 for HCLK input up to 25 MHz, and set to 1 for clock rate greater than 25 MHz.

BUFFER INTERFACE

The Buffer Interface is subdivided into the Receive Interface and the Transmit Interface

Receive Interface

The following signals are used in the Receive Interface.

Signal Name	Signal Definition
RPD(7:0)	Receive Packet Data Bus: These eight outputs are used to transfer the receive data from the SYM92C1000 to the external buffer management unit, and the receive status byte from the SYM92C1000 to the host interface controller.
RPDV	Receive Packet Data Valid: This output is driven high when a valid receive data byte is on RPD(7:0).
RPEF	Receive Packet End of Frame: This output is driven high at the end of the receive packet
RPSF	Receive Packet Start of Frame: This output is driven high at the start of the receive packet.
RPST	Receive Packet Status: This output is driven high when a valid receive status byte is on RPD(7:0).
RXNCLK	Receive Nibble Clock: This output is the 25/2.5 MHz nibble receive clock to the external buffer management unit. In 10BASE-T mode, RXNCLK is 2.5, in MII mode it may be either 2.5 MHz or 25 MHz, and TP-PMD modes it is a 25 MHz output. All receive signals from the SYM92C1000 to the Receive Buffer Management Unit are synchronous to RXNCLK.

The Receive Interface transfers data and status information to the External Receive Buffer Management Unit. Received packet data is passed on to the External Receive Buffer Management Unit one byte at a time at one half the clock rate of RXNCLK. A packet transmission to the External Receive Buffer Management Unit begins when the Receive Interface asserts RPSF and RPDV along with the first byte of received packet data after the removed preamble and start of frame delimiter (SFD). Subsequent packet data bytes are accompanied by only RPDV until the last byte which is accompanied by RPDV and RPEF. A minimum of three bytes are transmitted to the External Receive Buffer Management Unit if any bytes are emitted for a packet. There is no flow control feedback from the External Receive Buffer Management Unit to the Receive Interface, the External Receive Buffer Management Unit must be able to accept all valid data passed by the SYM92C1000 MAC. Following the last byte of the packet, three bytes of status are appended with RPST asserted, RPDV is not asserted for the status bytes. The Receive Interface passes packets up to and including 1536 bytes long. Longer packets are truncated to 1536 bytes unless Configuration Register bit 5 (HUGEN) is set to one. Collision fragments and other carrier events are passed through as packets if a valid preamble is seen following a valid IPG. Other carrier events are merely noted in the status bytes.

Receive Status Byte

Immediately following the last byte of the packet, three bytes of status are appended to the packet. These bytes are used by the external host interface controller for subsequent data flow control and are detailed in Table 8.

Table 8 Receive Packet Status Bytes

23	22	21	20	19	18	17	16
rsv	CEPS	RXOK	BRDCST	MLTCST	CRCER	DRBNIB	RXVIO
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TOOLNG	TOOSHRT	LNGTH	LNGTH	LNGTH	LNGTH	LNGTH	LNGTH
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LNGTH	LNGTH	LNGTH	LNGTH	LNGTH	LNGTH	LNGTH	LNGTH

Bits	Name	Description
0-13	LNGTH	Packet Length: These bits indicate the length of the packet in bytes.
14	TOOSHRT	Packet too Short: This bit is set when a received packet is less than 64 bytes long.
15	TOOLNG	Packet Too Long: This bit is set when a received packet is greater than 1518 bytes. This bit sets regardless of HUGEN.
16	RXVIO	Receive Code Violation: This bit is set when RXER is asserted.
17	DRBNIB	Dribble Nibble Received: This bit is set if the received data does not end on a byte boundary.
18	CRCER	CRC Error: This bit indicates a packet was received with an invalid Cyclic Redundancy Check field. The CRC of the incoming packet is continuously calculated and checked at the end of the packet. If this value does not match the CRC field of the received packet, a CRC error is reported.
19	MLTCST	Multicast Packet: This bit set indicates a packet with a multicast address.
20	BRDCST	Broadcast Packet: This bit set indicates a packet with a broadcast address.
21	RXOK	Receive OK: This bit set indicates no errors occurred during the packet reception.
22	CEPS	Carrier Event Previously Seen: This bit indicates that between the previous Receive Status Bytes and the current Receive Status Bytes a carrier event was detected, however, the reported carrier event is not associated with the packet to which the current Receive Status Byte is appended. A carrier event is activity on the receive channel that does not result in a packet receive attempt being made.
23	rsv	Reserved.

Transmit Interface

The following signals are used in the Transmit Interface.

Signal Name	Signal Definition
TPAB	Transmit Packet Abort: This output is driven high when the transmission is aborted.
TPD(7:0)	Transmit Packet Data Bus: These eight bi-directional lines are used to transfer the transmit data byte from the External buffer management unit to the SYM92C1000 and to transfer the transmit status byte from the SYM92C1000 to the host interface controller. TPD(7:0) is in the tri-state condition with weak internal pullup when not driven by the SYM92C1000 or the External buffer management unit.
TPDN	Transmit Packet Done: This output is driven high when all packet data has been transmitted.
TPEF	Transmit Packet End of Frame: This input is driven high to end a packet transmission.
TPRT	Transmit Packet Retry: This output is driven high when a collision has occurred and retransmission of the packet is required.
TPSF	Transmit Packet Start of Frame: This input is driven high to start a packet transmission.
TPST	Transmit Packet Status: This output is driven high when valid transmit status byte is on TPD(7:0).
TPUD	Transmit Packet Data Used: This output is driven high when actual data transmission has begun.
TPUR	Transmit Packet Underrun: This input is driven high to abnormally end a packet transmission.
TXNCLK	Transmit Nibble Clock: This output is the 25/10/2.5 MHz nibble transmit clock to the external buffer management unit. In 10BASE-T mode, TXNCLK is 2.5 MHz during transmission and 10 MHz between transmissions, in MII mode it may be either 2.5 MHz or 25 MHz, and TP-PMD modes it is a 25 MHz output. All transmit signals between the SYM92C1000 and the Transmit Buffer Management Unit are synchronous to TXNCLK.

The Transmit Interface takes packet data from the External Transmit Buffer Management Unit in bytes at one half the TXNCLK clock rate and passes it on to the SYM92C1000 on TPD(7:0). A packet transmission begins when the External Transmit Buffer Management Unit asserts TPSF. The External Transmit Buffer Management Unit may also send the first data byte of the packet along with TPSF or delay supplying the first data byte for up to eight periods. The transmit function of the SYM92C1000, after any pending backoff and deference, will generate an eight byte preamble and SFD. After transmitting the SFD, the first data byte is used and TPUD is asserted. TPUD may be asserted in as few as eight byte times, but due to backoff and deferral, may not be asserted for over 500,000 bit times. After seeing TPUD, TPSF is to be dropped and the External Transmit Buffer Management Unit must hold the first packet data byte for two rising clock edges, then supply packet data bytes every other TXNCLK pulse, holding them for the full two periods. The last packet data byte must be accompanied by TPEF for both TXNCLK periods to signal an end of transmission. If the External Transmit Buffer Management Unit fails to supply the first data byte by the time SFD is transmitted, or if at any time during transmission it is unable to supply the next packet data byte, it must recognize an underrun condition and assert TPUR to abort the packet. In addition, if the buffer is overrun causing loss of data, TPUR should be asserted to abort the packet.

TPEF causes the SYM92C1000 MAC to pad a short packet, if necessary and enabled by Configuration Register bit 2 (PADEN), and append the CRC if enabled by Configuration Register bit 3 (CRCEN). With a successful packet transmission, TPDN will be asserted and beginning the following clock period two status bytes will be asserted on TPD(7:0), one period each, with TPST asserted for the two periods. The External Transmit Buffer Management Unit and Host Interface Controller must have tri-stated drivers and accept the status bytes during the time TPST is driven.

Packets longer than 1536 bytes are truncated and aborted unless Configuration Register bit 5 (HUGEN) is set. Collisions will cause the transmission to be truncated and extended with 4 jam bytes consisting of zeros. Collisions other than the sixteenth will cause TPRT to be asserted to direct the External Transmit Buffer Management Unit to restart the packet. Late collisions are treated identically when Configuration Register bit 4 (RETRYL) is set, otherwise they cause an abort, indicated by TPAB. TPAB is also asserted by sixteen collisions on the same packet, excessive deferral, or a transmission underflow. In the event of an aborted transmission, the External Transmit Buffer Management Unit must dump the aborted packet and continue to the next packet.

At the end of a transmission attempt, TPDN, TPRT, and TPAB are held in their current state until the next assertion of TPSF, at which point they are deasserted.

Transmit Status Byte

Immediately following the last byte of the packet, two bytes of status are presented to the External Transmit Buffer Management Unit. These bytes are used by the External Receive Buffer Management Unit for subsequent data flow control and are detailed in Table 9.

Table 9 Transmit Packet Status Bytes

15	14	13	12	11	10	9	8
LNKFAIL	NOCRS	TXOK	TALC	TAED	TAEC	TAUH	PD

7	6	5	4	3	2	1	0
BRDCST	MLTCST	CRCER	LC	COLCNT	COLCNT	COLCNT	COLCNT

Bits	Name	Description
0-3	COLCNT	Collision Count: Bits 3 through 0 give the collision count (0-15) of any successfully transmitted packet. The maximum number of collisions before a packet is aborted is 16, so TAEC set indicates that 16 collisions have occurred.
4	LC	Late Collision Seen: This bit set indicates that a late collision was seen on at least one transmission attempt. A late collision occurs more than 512 bit times after the start of the preamble. Bits 4 and 12 are mutually exclusive, this bit is valid only when Configuration Register bit RETRYL is asserted.
5	CRCER	CRC Error: If CRC is disabled the SYM92C1000 assumes the last four bytes of a packet are an appended CRC and it compare those bytes to its generated CRC. If the assumed CRC and the generated CRC do not match a CRC error is reported in the status bytes.
6	MLTCST	Multicast Packet Transmitted or Attempted: This bit is set if the preceding packet was a multicast packet.
7	BRDCST	Broadcast Packet Transmitted or Attempted: This bit is set if the preceding packet was a broadcast packet.
8	PD	Packet Deferred: This bit indicates that the packet was deferred on at least one transmission attempt.
9	TAUH	Transmit Aborted Due To Underrun or Huge Packet.
10	TAEC	Transmit Aborted Due To Excessive Collisions: After 16 transmit attempts with 16 collisions, the packet is aborted and this bit is set.
11	TAED	Transmit Aborted Due To Excessive Deferral: This bit set means the SYM92C1000 was forced to defer more than 500,000 bit times (125,000 nibble times) during a transmission attempt.
12	TALC	Transmit Aborted Due To Late Collision: This bit set means a transmit packet experienced a late collision and was aborted. A late collision occurs more than 512 bit times after the start of the preamble. Bits 4 and 12 are mutually exclusive, this bit is valid only when Configuration Register bit RETRYL is not asserted.
13	TXOK	Transmit OK: This bit set means the last packet transmitted completely without aborting
14	NOCRS	No Carrier Sense Or SQE Error Seen On Transmit (valid for 10BASE-T mode only)
15	LNKFAIL	Link Failure Or Jabber Condition Detected (valid for 10BASE-T mode only)

JTAG INTERFACE

The following signals are used in the JTAG Interface.

Signal Name	Signal Description
TCK	Test Clock: This input is the JTAG clock and is limited to 10 MHz maximum. It is used to shift test data and JTAG control information into and out of the SYM92C1000 during JTAG test operations. This pin should not be left floating, if JTAG is not used tie TCK to ground.
TDI	Test Data In: This input is the JTAG serial data input, it is used to shift test data and instructions into the SYM92C1000 during a JTAG test. This pin has a weak internal pullup and may be left unconnected if JTAG is not used.
TDO	Test Data Out: This output is the JTAG serial data output, it is used to shift test data and instructions out of the SYM92C1000 during a JTAG test.
TMS	Test Mode Select: This input is the JTAG mode select, it is used to control the state operation of the SYM92C1000 during a JTAG test. This input has a weak internal pullup and may be left unconnected if JTAG is not used.
-TRST	Test Reset: This active-low input is the JTAG reset. This input has a weak internal pullup, if JTAG is not used or TCK is not clocked then tie -TRST to ground. If JTAG is used then -TRST needs to be held low during chip reset..

The JTAG Interface is defined by the IEEE standard 1149.1. This standard defines test logic that can be included in an integrated circuit to provide standardized approaches to:

1. testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate;
2. observing circuit activity during the component's normal operation.

The test logic consists of a boundary-scan register and other building blocks and is accessed through the JTAG Interface

LED INTERFACE

The following signals are used in the LED Interface

Signal Name	Signal Description
-LEDC	Collision LED: This 16 mA open-drain output is driven low when the SYM92C1000 detects a collision. When not active it is in a high impedance state. This output is stretched to 30 ms.
-LEDL	Link LED: This 16 mA open-drain output is driven low when the SYM92C1000 detects link. When not active it is in a high impedance state. This output is stretched to 30 ms. In MII mode the MII Request Register bit 1 (SCAN) must be set to 1 for this output to be valid.
-LEDR	Receive LED: This 16 mA open-drain output is driven low when the SYM92C1000 is receiving. When not active it is in a high impedance state. This output is stretched to 30 ms.
-LEDT	Transmit LED: This 16 mA open-drain output is driven low when the SYM92C1000 is transmitting. When not active it is in a high impedance state. This output is stretched to 30 ms.

The LED interface functions as a switched, 16 mA maximum ground for collision, link, receive, and transmit status LEDs. A typical circuit implementation is shown in Figure 5.

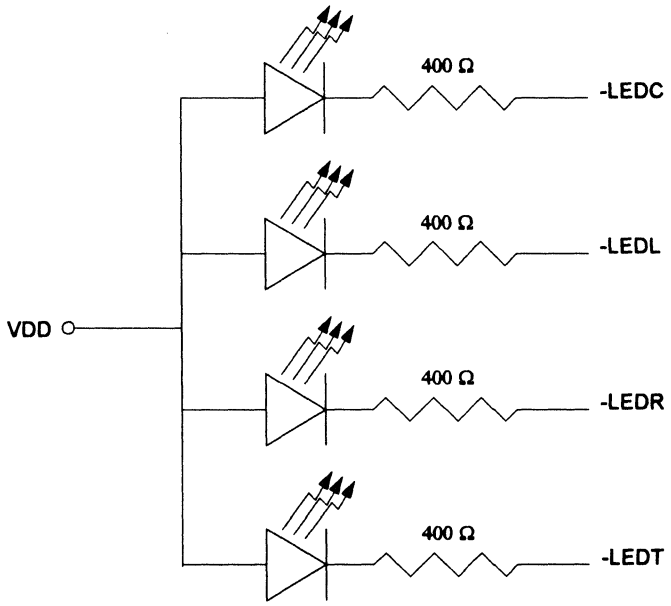


Figure 5 Typical LED Circuit

CONFIGURATION INTERFACE

The following signals are used in the Configuration Interface.

Signal Name	Signal Description
CLKSPEED	Host Clock Speed Select: This configuration input is tied high to inform the SYM92C1000 that the host clock is between 25 MHz and 33 MHz, a low input indicates clock rate is 25 MHz or less. This pin is used only in MII mode to determine MDC clock speed. It has a weak internal pulldown and if left unconnected this function assumes a clock rate of 25 MHz or less
CRCEN	Cyclic Redundancy Check Enable: This configuration input is used to enable CRC error generation. The SYM92C1000 will continuously calculate the CRC and append the result to the end of the transmit packet. If PADEN is set, CRCEN is ignored and a CRC is generated. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset.
FULLD	Full Duplex Enable: This configuration input is used to put the SYM92C1000 into full duplex operation. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset.
HUGEN	Huge Packet Enable: This configuration input is used to enable the SYM92C1000 to transmit or receive packets with more than the IEEE maximum of 1518 bytes. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset.
INTLB	Internal Loopback Enable: The SYM92C1000 has internal loopback capability, setting this configuration input will cause the MAC to begin internal loopback. The SYM92C1000 does not need to be in full duplex mode to perform internal loopback. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset.
IPGT(6:0)	Back-To-Back Interpacket Gap: These configuration inputs are used to provide the reset value for the Back-to-Back Interpacket Gap register. IPGT(4:3) have weak internal pullups, the others have weak internal pulldowns. This provides a reset value of 0x18 when left unconnected.
JABEN	Jabber Enable: This configuration input is used to enable the SYM92C1000 jabber logic at reset. If the SYM92C1000 transmits continuously for 20 ms it will abort the transmission and drive TXEN low to block all transmissions for 250 ms. This configuration is valid only in 10BASE-T mode. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset.
MODE(1:0)	Mode Select: This configuration input is used to select the reset configuration of the multiplexed I/O interface. 00 selects MII mode, 01 selects TP-PMD mode, and 10 selects 10BASE-T mode. These pins have a weak internal pulldown, if left unconnected the SYM92C1000 defaults to MII mode.
NOCFR	No Ciphering: This configuration input disables the ciphering function in TP-PMD mode. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset and ciphering will occur.
PADEN	Pad Enable: This configuration input is used to instruct the SYM92C1000 to pad any short packets out to the IEEE minimum of 64 bytes when reset. In the Pad Enable mode, a CRC is generated regardless of CRCEN. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset.
RETRYL	Late Collision Retry: This configuration input is used to instruct the SYM92C1000 to allow late collision retries. A late collision occurs more than 512 bit times after the start of a transmission and indicates a mis-configured network topology. This pin has a weak internal pulldown, if left unconnected this function is disabled at reset.

These pins are used to establish the reset configuration of the SYM92C1000 by loading the Configuration Interface pin values to the Configuration Register. If a different configuration is desired, the contents of the register can be overwritten with a new configuration value. If these pins are left floating, -HRST must be asserted for 150 HCLK cycles followed by a 20 cycle wait at power-up to put the SYM92C1000 into a known state.

MULTIPLEXED I/O INTERFACE

The Multiplexed I/O Interface allows the user one of three configuration options, a MII Interface, a 100BASE-TX Interface, or a 10BASE-T interface, selected with the Configuration Register bits 8 and 9 (MODE). MODE configures the MII Multiplexer and the I/O Multiplexer to route the packet data through either the 100BASE-TX Module, the 10BASE-T Module, or bypassing both to allow I/O in MII format. Figure 6 depicts the transmit and receive data paths with all three options illustrated.

The transmit data flow originates as the Transmit Byte Stream coming from the External Transmit Buffer Management Unit and enters the Transmit Function block. The Transmit Function block is responsible for converting the Transmit Byte Stream into MII nibble data streams. The Transmit Function performs the IEEE 803.2 specified deference and backoff algorithms, it prepends the data packet with a preamble and SFD, it detects and enforces collisions with jams, it manages and tracks retries, and it reports status to the Host Interface Controller. The Transmit Function block will also pad short packets, implement full or half duplex, append a CRC, retry late collisions, transmit huge packets, and adjust the IPG, according to the user defined configuration registers. The Transmit Function operates on the 2.5 MHz or 25 MHz clock TXCLK in MII mode, the 25 MHz TXCLK in 100BASE-TX modes, or it operates on a 2.5 MHz clock generated from the 10 MHz TXCLK in 10Base-T mode.

After the Transmit Function block the data nibbles enter the MII Multiplexer. The MII Multiplexer routes the data to either the 100BASE-TX, 10BASE-T, or I/O Multiplexer block.

The 100BASE-TX block accepts packet data nibbles from the MII Multiplexer at a clock rate of 25 MHz. The data is then converted from four bit nibbles to five bit format (4B/5B), and presented to the I/O Multiplexer which presents the data to the 100BASE-TX PHY on pins TSM(4:0).

The 10BASE-T block accepts transmit packet data nibbles from the MII Multiplexer at a clock rate of 2.5 MHz. The data is then converted from nibbles to serial data and presented to the I/O Multiplexer at 10 MHz. The I/O Multiplexor then presents the data to the 10BASE-T PHY on pin TXD.

If the MII configuration option is chosen, the MII Multiplexer presents the data nibble directly to the I/O Multiplexer at a clock rate of 2.5 MHz or 25 MHz. The I/O Multiplexer then presents the data to the MII PHY on pins TXD(3:0).

The receive data path originates as a data stream from the PHY. Depending on system configuration, the packet data is received from the PHY as a 10 MHz serial data stream, a 25 MHz five bit data pack, or a 25 MHz or 2.5 MHz four bit nibble. The data is routed through the appropriate module (determined by system configuration) and assembled into 4 bit nibbles. The nibbles are delivered to the Receive Function block at 25 MHz for 100 Mbps transmissions or 2.5 MHz for 10 Mbps transmissions.

The Receive Function block is responsible for: detecting and removing the preamble and SFD, enforcing configuration register options, enforcing the IPG, verifying the CRC, assembling the packet data nibbles into bytes and transmitting them on to the External Receive Buffer Management Unit, and observing any dribble nibbles or receive code violations and reporting them in the appended three status bytes.

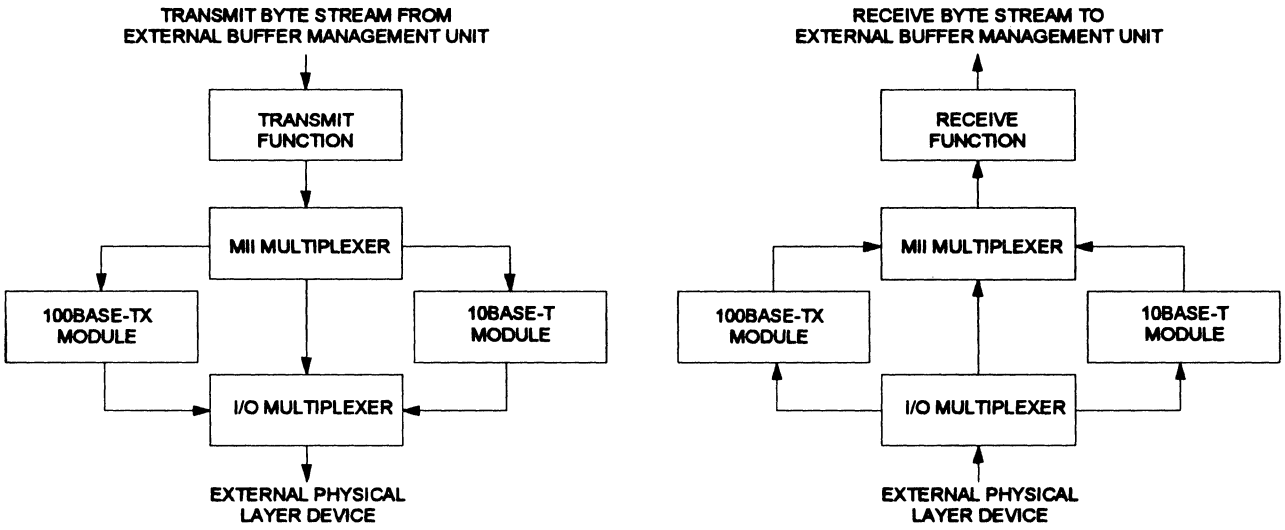


Figure 6 Transmit and Receive Data Paths

MII Interface

The following signals are used in the MII Interface

Signal Name	Signal Description
COL	Collision: This asynchronous input is driven high for a minimum of two TXCLK periods when the external MII PHY detects a collision.
CRS	Carrier Sense: This asynchronous input is driven high for a minimum of two TXCLK periods by the external MII PHY when either the transmit or receive medium is active.
MDC	Management Clock: This output is the 2.5 MHz or less reference clock for the management data.
MDIO	Management Data: This bi-directional line is used to transfer the management data between the SYM92C1000 and the external MII PHY .
RXCLK	Receive Clock: This input is the 2.5 MHz or 25 MHz nibble receive clock from the external MII PHY. All receive signals to the SYM92C1000 are synchronous to RXCLK.
RXD(3:0)	Receive Data: These four inputs are used to transfer the receive data nibble from the external MII PHY to the SYM92C1000.
RXDV	Receive Data Valid: This input is driven high when valid receive data nibble is on RXD(3:0).
RXER	Receive Error: This input is driven high when there is an error on the receive data stream.
TXCLK	Transmit Clock: This input is the 2.5 MHz or 25 MHz nibble transmit clock from the external MII PHY. All transmit signals from the SYM92C1000 are synchronous to TXCLK.
TXD(3:0)	Transmit Data Bus: These four outputs are used to transfer the transmit data nibble from the SYM92C1000 to the external MII PHY .
TXEN	Transmit Enable: This output is driven high when valid transmit data nibble is on TXD(3:0).
TXER	Transmit Error: This output is driven high when there is an error on the transmit data stream.

The MII interface allows access to the internal MII formatted data of the SYM92C1000. The packet data is transmitted on TXD(3:0) and received on RXD(3:0) in nibbles clocked at 2.5 MHz or 25 MHz by either TXCLK and RXCLK respectively. When the SYM92C1000 is attached to a 40 pin MII connector, 45 Ω series resistors should be inserted on pins TXD(3:0), TXEN, TXER, MDC, and MDIO for impedance matching, and a 2 kΩ pulldown resistor should be installed on MDIO (Figure 7).

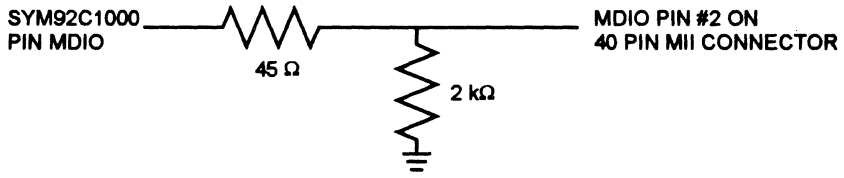


Figure 7 MII Pin MDIO Pulldown

TP-PMD Interface

The following signals are used in the TP-PMD Interface

Signal Name	Signal Description
-FO	Fiber Optic Off: This active-low output is driven low to turn off the external TP-PMD PHY fiber optic transmit circuit. This signal is controlled by an internal register.
-LB	Loopback: This active-low output is driven low to perform the loopback function in the external TP-PMD PHY. The SYM92C1000 must be in full duplex mode to perform loopback. This signal is controlled by an internal register.
RSM(4:0)	Receive Data Bus: These five inputs are used to transfer data from the external TP-PMD PHY to the SYM92C1000.
RXCLK	Receive Clock: This input is the 25 MHz symbol receive clock from the external TP-PMD PHY. All receive signals to the SYM92C1000 are synchronous to RXCLK.
SDO	Signal Detect: This input is driven high when the receive medium is active.
TSM(4:0)	Transmit Data Bus: These five outputs are used to transfer data from the SYM92C1000 to the external TP-PMD PHY.
TXCLK	Transmit Clock: This input is the 25 MHz symbol transmit clock from the external TP-PMD PHY. All transmit signals from the SYM92C1000 are synchronous to TXCLK.

The TP-PMD interface takes the four bit nibbles from the MII output of the Transmit Function, and converts them into encoded and ciphered five bit transmit symbols presented on TSM(4:0) for the TP-PMD PHY. The interface also takes the five bit receive symbols on RSM(4:0) from the TP-PMD, deciphers and decodes them into nibbles and presents them to the Receive Function. The ciphering/deciphering function can be disabled by setting the Configuration Register bit 0 (NOCFR) to one.

TXER and TXEN simultaneously asserted will cause an error symbol to be encoded. If both are asserted during the first two nibbles, the error symbol will be delayed until the third output symbol. Idle symbols are encoded in the absence of an active packet. SDO is driven high by the PHY when there is receive activity on the network (either active packets or idle symbols).

4B/5B Encoding

When transmitting in TP-PMD mode, the SYM92C1000 maps the four bit MII data to five bit data for the external PHY according to IEEE 802.3 standards listed in Table 10. The code (derived from ISO 9314-1 (1989)) is designed to be undetectable and have no meaning outside the 100BASE-TX PHY. It is intended to provide adequate codes for all data code-groups (16) plus control code groups, to have appropriate coding efficiency (80%) to effect 100 Mbps data transmission on a 125 Mbps media, and to provide sufficient transition density to facilitate clock recovery when not in cipher mode.

Table 10 4B/5B Code Group Mapping

PCS Code-Group (4:0) 4 3 2 1 0	Group Name	MII TXD/RXD (3:0) 3 2 1 0	Description
1 1 1 1 0	0	0 0 0 0	Data 0
0 1 0 0 1	1	0 0 0 1	Data 1
1 0 1 0 0	2	0 0 1 0	Data 2
1 0 1 0 1	3	0 0 1 1	Data 3
0 1 0 1 0	4	0 1 0 0	Data 4
0 1 0 1 1	5	0 1 0 1	Data 5
0 1 1 1 0	6	0 1 1 0	Data 6
0 1 1 1 1	7	0 1 1 1	Data 7
1 0 0 1 0	8	1 0 0 0	Data 8
1 0 0 1 1	9	1 0 0 1	Data 9
1 0 1 1 0	A	1 0 1 0	Data 10
1 0 1 1 1	B	1 0 1 1	Data 11
1 1 0 1 0	C	1 1 0 0	Data 12
1 1 0 1 1	D	1 1 0 1	Data 13
1 1 1 0 0	E	1 1 1 0	Data 14
1 1 1 0 1	F	1 1 1 1	Data 15
1 1 1 1 1	I	undefined	IDLE: used as inter-Stream fill code
1 1 0 0 0	J	0 1 0 1	Start-of-Steam Delimiter, Part 1 of 2: always used in pairs with K
1 0 0 0 1	K	0 1 0 1	Start-of Stream Delimiter, Part 2 of 2: always used in pairs with J
0 1 1 0 1	T	undefined	End-of-Stream Delimiter, Part 1 of 2: always used in pairs with R
0 0 1 1 1	R	undefined	End-of-Stream Delimiter, Part 2 of 2: always used in pairs with T
0 0 1 0 0	H	undefined	Invalid code, Transmit Error
0 0 0 0 0	V	undefined	Invalid code
0 0 0 0 1	V	undefined	Invalid code
0 0 0 1 0	V	undefined	Invalid code
0 0 0 1 1	V	undefined	Invalid code
0 0 1 0 1	V	undefined	Invalid code
0 0 1 1 0	V	undefined	Invalid code
0 1 0 0 0	V	undefined	Invalid code
0 1 1 0 0	V	undefined	Invalid code
1 0 0 0 0	V	undefined	Invalid code
1 1 0 0 1	V	undefined	Invalid code

100BASE-T Ciphering

The purpose of ciphering is to spread the transmission spectrum so that electromagnetic coupling with other components is minimized. Ciphering randomizes the data spectrum by XORing a pseudorandom key sequence to the data stream before it is passed on the PHY. The length of the pseudorandom sequence (2047 bits) is chosen to reduce radiated emissions by approximately 20 dB when the SYM92C1000 is transmitting the Idle Line State. In certain applications this reduction may be necessary to meet regulatory requirements. The key sequence is determined with an eleven bit shift register where bit zero is determined by the exclusive OR of bits ten and eight, Figure 8 Illustrates a simplified ciphering circuit.

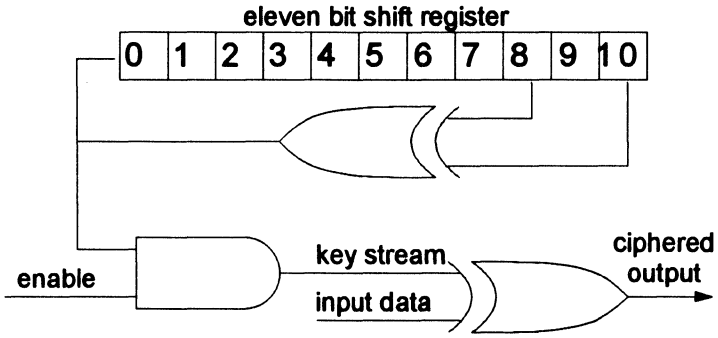


Figure 8 Ciphering Circuit

10BASE-T Interface

The following signals are used in the 10BASE-T Interface

Signal Name	Signal Description
-ADPLX	Autoduplex Enable/Jabber Disable: This active-low output is typically used to enable the autoduplex or jabber functions on the external 10BASE-T PHY. If the twisted pair (TP) port is selected and -LNKDIS = 1, this signal is typically driven low to select autoduplex and high to select half duplex. If the AUI port is selected and -LNKDIS = 0, this signal is typically driven low to disable the jabber function. This signal is controlled from the internal 10BASE-T control register. Note: the SYM92C1000 does not support auto duplex, use this bit to disable that function of the PHY.
APOL	Autopolarity Enable: This output is typically driven high to enable the external 10BASE-T PHY autopolarity function. This signal is controlled from the internal 10BASE-T control register.
AUIPS	AUI Port Select: This output is typically used in conjunction with TPPS to select the port on the 10Base-T device. This signal is controlled from the internal 10BASE-T control register
COL	Collision: This input is driven high for a minimum of two TXCLK periods when there is collision between the transmit and receive data.
CRS	Carrier Sense: This input is driven high when there is data on the receive medium.
FLTRDIS	Filter Disable: This output is typically driven high to disable the external 10BASE-T PHY transmit and receive filter function. This signal is controlled from the internal 10BASE-T control register.
-LB	Loopback Enable/SQE Disable: This active-low output is typically used to enable the loopback or SQE functions on the external 10BASE-T PHY. If TP port is selected and -LNKDIS = 1, this signal is driven low to disable the SQE function. If AUI port is selected and -LNKDIS=0, this signal is driven low to enable the loopback function. The SYM92C1000 must be in full duplex mode to perform loopback. This signal is controlled from the internal 10BASE-T control register.
-LNKDIS	Link Disable: This active-low output is typically driven low to disable the external 10BASE-T PHY link pulse function. This signal is controlled from the internal 10BASE-T control register.
-LNKLED	Link Pulse: This input is driven low for a minimum of two TXCLK periods when the external 10BASE-T PHY detected a link pulse on the twisted pair receive input.
-LONG	Long Cable Mode: This active-low output is typically driven low to enable the external 10BASE-T PHY the capability to accommodate cable lengths in excess of 100 meters. This signal is controlled from the internal 10BASE-T control register.
-PDN	Powerdown Enable: This output is typically driven low to disable all functions and lower power consumption to minimum on the external 10BASE-T PHY. This signal is controlled from the internal 10BASE-T control register.
RXCLK	Receive Clock: This input is the 10 MHz receive clock from the external 10BASE-T PHY. All receive signals to the SYM92C1000 are synchronous to RXCLK.

Signal Name	Signal Description
RXD	Receive Data: This input is used to transfer data from the external 10BASE-T PHY to the SYM92C1000.
TPPS	TP Port Select This output is typically used in conjunction with AUIPS to select the port on the 10Base-T device. This signal is controlled from the internal 10BASE-T control register
TXCLK	Transmit Clock: This active-low input is the 10 MHz transmit clock from the external 10BASE-T PHY. All transmit signals from the SYM92C1000 are synchronous to TXCLK.
TXD	Transmit Data: This output is used to transfer data to the external 10BASE-T PHY.
TXEN	Transmit Enable: This output is driven high when valid data is on TXD.
UTPSTP	Cable Type Select: This output is typically used to adjust the external 10BASE-T PHY transmit output current level to accommodate either 100 Ohm UTP cable or 150 Ohm STP cable. This signal is driven high to select UTP cable and low to select STP cable. This signal is controlled from the internal 10BASE-T control register.

The 10BASE-T interface takes the four bit nibbles from the MII output of the Transmit Function, and converts them into a serial bit stream on TXD for encoding and transmission by the 10BASE-T PHY. The interface also takes the decoded bit stream from the PHY and assembles it into nibbles for the Receive Function. In the event of dribble bits (the bit stream not ending on a byte boundary), the data stream is truncated to the last byte boundary.

The output pins -ADPLX, APOL, -AUIPS, FLTRDIS, -LB, -LNKDIS, -LONG, -PDN, -TPPS, and UTPSTP reflect the contents of the 10BASE-T Control Register

POWER SUPPLY CONSIDERATIONS

The following signals are used to provide power and ground for the SYM92C1000

Signal Name	Signal Description
VDDCORE	Core Power Bus: This is the power for the digital core.
VDDIO	I/O Power Bus: This is the power for the I/O circuitry.
VSSCORE	Core Ground Bus: This is the ground for the digital core.
VSSIO	I/O Ground Bus: This is the ground for the I/O circuitry.

Power and ground layout on the circuit board should be carefully considered to provide proper noise immunity. The VDDCORE, VDDIO, VSSCORE, and VSSIO pins should be connected directly to the primary power and ground planes of the circuit board. A 0.01 µF bypass capacitor should be connected between each VDD pin and the primary ground plane. A single 2.2 µF (tantalum) bypass capacitor should be connected between the primary power and ground planes.

FUNCTIONAL DESCRIPTION

TRANSMIT LOGIC

The transmit logic takes byte-wide data from the Buffer interface and, depending on mode, translates it into 4 bit nibbles (MII mode), 5 bit words (TP-PMD mode) or serializes it (10BASE-T mode). During transmission, the transmit logic appends preamble, optionally inserts CRC (Cyclic Redundancy Check), monitors Collision Detection and Carrier Sense, and reports two status bytes. Functionality is determined by the control bits set in the configuration registers.

CSMA/CD PROTOCOL

The Carrier Sense Multiple Access with Collision Detection (CSMA/CD) media access method is the means by which two or more stations share a common bus. To transmit, a station waits (defers) for a period on the medium when no other station is transmitting, it then sends the message in bit serial form. If a message collides with that of another station, each transmitting station intentionally jams 32 additional bits to ensure propagation of the collision through the system. Each station then remains silent for a random amount of time (back-off) before attempting to transmit again.

The defer logic is used to time the interpacket gap. An interpacket gap of 960 ns (100 Mbps protocol) or 9.6 μs (10 Mbps protocol) is normally required by the 802.3 specification, but this time may be adjusted to a different value using the Interpacket Gap Register. If the SYM92C1000 has just transmitted a packet and starts another packet transmission, it will not defer to an incoming receive packet during the transmission idle time. This causes a collision on the network and the back-off circuitry then resolves the collision between the packets. If the SYM92C1000 has just received a packet and starts a packet transmission, the transmitter defers to an incoming packet if the internal CRS signal goes active within the time specified by the Non-Back-to-Back Interpacket Gap Register. After the configured time, it will transmit the packet with no deferral, causing a collision on the network which is then resolved by the back-off circuitry.

The back-off logic uses the IEEE 802.3 back-off algorithm. The transmit logic allows a packet to be re-transmitted a maximum of 15 times (16 transmission attempts) due to collision.

RECEIVE LOGIC

The receive logic takes data in one of three forms, 4 bit nibbles (MII mode), 5 bit words (TP-PMD mode), or serial (10BASE-T mode). During reception, the receive logic removes the preamble, calculates the CRC and compares it with the incoming CRC, and reports three status bytes at the end of a packet for use by the Receive Buffer Management Unit

ADDRESS RECOGNITION

No address recognition circuitry is present on the SYM92C1000, all address recognition must be performed by the external Host Interface Controller.

CYCLIC REDUNDANCY CHECK

The cyclic Redundancy Check (CRC) is a 32 bit code attached to the packet by the transmit logic and used by the receiving station to check for errors. The receiver calculates a CRC based on the incoming data and compares it to the CRC attached to the packet by the transmit logic. If they are equal, the packet is good. CRC errors are reported in bit 18 of the receive status bytes after the packet is sent to the Receive Buffer Management Unit.

FULL/HALF-DUPLEX OPERATIONS

The SYM92C1000 does not support autoduplex functions of an external 10BASE-T PHY, set the -ADPLX pin accordingly to disable this function. When in half-duplex mode, the receiver function is disabled while a transmission occurs.

When in full-duplex mode, the SYM92C1000 ignores the CRS and COL pins and will not defer packet transmissions. It is recommended that the SYM92C1000 be configured to full-duplex in TP-PMD mode. The external FIFO interface logic must determine which request should be serviced first. It is recommended that transmit operations take precedence over receive operations because transmit underruns leave broken packets on the media but receive overruns cause repeat transmissions from the sending node that leave the media clean.

INTERNAL REGISTERS

Table 11 gives the address assignments and reset values within the register address space for each internal register of the SYM92C1000. All addresses and reset values are given in hexadecimal.

Table 11 Internal Register Address, Reset Value, and Description

Address	Resets to	Mnemonic	Register Name
00h	0000h	CONF	Configuration Register (16 bit read/write)
01h	0018h	BBIPG	Back-to-Back Interpacket Gap Register (16 bit read/write)
02h	1018h (100 Mbps) 4060h (10 Mbps)	NBBIPG	Non-Back-to-Back Interpacket Gap Register (16 bit read/write)
03h	0000h	MIIREQ	MII Request Register (16 bit write only, MII mode only)
04h	061Fh	MIIADD	MII Address Register (16 bit read/write, MII mode only)
04h	061Fh	TPPMD	TP-PMD Control Register (16 bit read/write, TP-PMD mode only)
04h	061Fh	10T	10BASE-T Control Register (16 bit read/write, 10BASE-T mode only)
05h	unknown	MIIWD	MII Write Data Register (16 bit read/write, MII mode only)
06h	unknown	MIIRD	MII Read Data Register (16 bit read only, MII mode only)
07h	0000h	MIIIN	MII Indicators Register (16 bit read only, MII mode only)

CONFIGURATION REGISTER (00h)

The Configuration Register is a read/write register used to configure or indicate status. of the SYM92C1000.

This register defaults to 0000h at reset. When writing to this register, the host must make sure that a transmit operation is not in progress and must ignore data received.

15	14	13	12	11	10	9	8
SRST	rsv	rsv	rsv	rsv	INTLB	MODE	MODE

7	6	5	4	3	2	1	0
CLKSPD	JABEN	HUGEN	RETRYL	CRCEN	PADEN	FULLD	NOCFR

Bits	Name	Description
0	NOCFR	No CFR: With this bit set, the ciphering function of the 100BASE-TX module is disabled for both transmit and received. This bit is only valid in TP-PMD mode.
1	FULLD	Full Duplex: Set this bit to enable full-duplex operation of the SYM92C1000.
2	PADEN	Pad Enable: With this bit set, the SYM92C1000 pads short transmit packets (< 64 bytes). Setting this bit generates a CRC regardless of CRCEN.
3	CRCEN	Cyclic Redundancy Check Enable: With this bit set, the SYM92C1000 continuously calculates the CRC and appends the result to the end of the transmit packet. If PADEN is set, CRCEN is ignored and a CRC is generated.
4	RETRYL	Late Collision Retry: With this bit set, the SYM92C1000 allows late collision retries. A late collision occurs more than 512 bit times after the start of a transmission and indicates a mis-configured network topology.
5	HUGEN	Huge Packet Enable: With this bit set, the SYM92C1000 will receive and transmit packets longer than the IEEE 802.3 standard maximum 1518 bytes.
6	JABEN	Jabber: With this bit set, if the SYM92C1000 transmits continuously for 20 ms it will abort the transmission and drive TXEN low to block all transmissions for 250 ms. This bit is valid in 10BASE-T mode only.

Bits	Name	Description
7	CLKSPD	Clock Speed: This bit must be set when the host clock is faster than 25 MHz. This bit is valid only in MII mode
8-9	MODE	Interface Mode: These two bits are used to configure the SYM92C1000 to the installed External Physical Layer Device (PHY) interface. To configure, set the two bits (8 and 9) by the following table: Bit 9 / Bit 8 / Interface 0 / 0 / MII 0 / 1 / TP-PMD 1 / 0 / 10BASE-T 1 / 1 / Reserved
10	INTLB	Internal Loopback: Set this bit to enable the internal loopback function. In 10BASE-T mode loopback occurs between the serializer and deserializer functions. In TP-PMD mode loopback occurs between 4B/5B transmit conversion and 5B/4B receive conversion. In MII mode loopback occurs after the MII multiplexor and before the I/O multiplexor. The SYM92C1000 does not need to be in full duplex mode to perform internal loopback.
11-14	rsv	Reserved.
15	SRST	Soft Reset: Set this bit to initiate a soft reset of the SYM92C1000, reset this bit to end the soft reset. This bit is write only.

BACK-TO-BACK INTERPACKET GAP REGISTER (01h)

The Back-to-Back Interpacket Gap (IPG) Register is a read/write register used to configure the IPG of a back-to-back transmission by the SYM92C1000. The IPG is determined by multiplying the value in the register by the clock period of TXCLK. This makes the time increment 100 ns for a 10 MHz TXCLK and 40 ns for a 25 MHz TXCLK. For the 10BASE-T interface, the IEEE 802.3 standard IPG is 9.6 µs, this requires the register be set to 0060h (96d). The MII and TP-PMD interface IEEE standard IPG is 960 ns, requiring the register be set to 0018h (24d). This register defaults to 0018h on reset to configure the 100 MHz IPG at 960 ns. For 10BASE-T mode the IPG should be rewritten to the register since it will default to only 2.4 µs. When writing to this register, the host must make sure that a transmit operation is not in progress.

15	14	13	12	11	10	9	8
rsv	rsv	rsv	rsv	rsv	rsv	rsv	rsv

7	6	5	4	3	2	1	0
rsv	IPGT	IPGT	IPGT	IPGT	IPGT	IPGT	IPGT

Bits	Name	Description
0-6	IPGT	Interpacket Gap Time: These seven bits hold a number from 0 to 127. The IPG is determined by multiplying this number by the clock period of TXCLK.
7-15	rsv	Reserved.

NON-BACK-TO-BACK INTERPACKET GAP REGISTER (02h)

The Non-Back-to-Back Interpacket Gap Register is a read/write register used to configure or indicate the two IPG lengths of a non-back-to-back transmission by the SYM92C1000. IPGR1 is the first part of the total IPG length and is typically two thirds of the total time. This is the time when the SYM92C1000 will defer if the carrier sense determines a packet is on the media, after this time the SYM92C1000 will no longer defer to a sensed packet and will transmit after the IPG regardless of activity. IPGR2 is the total IPG length and is typically the same as IPGT in the Back-to-Back Register. The two lengths are determined by multiplying the values in the register by the clock period of TXCLK. This makes the time increment 100 ns for a 10 MHz TXCLK and 40 ns for a 25 MHz TXCLK. This register defaults to 1018h when Mode(1:0) = 0,0 or 0,1. This configures the IPG to the IEEE 802.3 recommended IPGR1 = 640 ns and IPGR2 = 960 ns in 100 MHz modes. The default value when Mode(1:0) = 1,0 is 4060h. This configures the IPG to the IEEE 802.3 recommendations of IPG1 = 6.4 μs and IPGR2 = 9.6 μs for 10BASE-T mode. When writing to this register, the host must make sure that a transmit operation is not in progress.

15	14	13	12	11	10	9	8
rsv	IPGR1	IPGR1	IPGR1	IPGR1	IPGR1	IPGR1	IPGR1

7	6	5	4	3	2	1	0
rsv	IPGR2	IPGR2	IPGR2	IPGR2	IPGR2	IPGR2	IPGR2

Bits	Name	Description
0-6	IPGR2	Interpacket Gap Register 2: These seven bits hold a number from 0 to 127. This is the total non-back-to-back IPG, it is determined by multiplying this number by the clock period of TXCLK.
7	rsv	Reserved.
8-14	IPGR1	Interpacket Gap Register 1: These seven bits hold a number from 0 to 127. This is the first part of the non-back-to-back IPG, it is determined by multiplying this number by the clock period of TXCLK. This period is typically two thirds of IPGR2.
15	rsv	Reserved.

MII REQUEST REGISTER (03h)

The MII Request Register is a write only register used to issue a read or scan command to the MII management function. This register defaults to 0000h. This register is only valid in MII mode

15	14	13	12	11	10	9	8
rsv	rsv	rsv	rsv	rsv	rsv	rsv	rsv

7	6	5	4	3	2	1	0
rsv	rsv	rsv	rsv	rsv	rsv	SCAN	RSTAT

Bits	Name	Description
0	RSTAT	Read Statistics: Set this bit to one to read an MII management register in the external PHY. This bit is reset automatically by hardware.
1	SCAN	Scan Register: Set this bit to 1 to continuously read an external PHY MII management register. Set this bit to 0 to discontinue the scan operation. To continuously detect link in MII mode this bit must be set to 1.
2-15	rsv	Reserved.

CONTROL REGISTER ADDRESS (04h)

This register functions differently in each of the three modes, MII, TP-PMD, or 10BASE-T. In MII mode it is referred to as the MII Address Register, in TP-PMD mode it is the TP-PMD Control Register, and in 10BASE-T mode it is the 10BASE-T Control Register. In all three modes the register resets to 061Fh Descriptions for the three modes follow.

MII Address Register (04h)

In MII mode, the MII Address Register contains the PHY address and management register address. This register resets to 061Fh.

15	14	13	12	11	10	9	8
SQEDIS	rsv	rsv	FIAD	FIAD	FIAD	FIAD	FIAD

7	6	5	4	3	2	1	0
rsv	rsv	rsv	RGAD	RGAD	RGAD	RGAD	RGAD

Bits	Name	Description
0-4	RGAD	Register Address: MII management register address.
5-7	rsv	Reserved.
8-12	FIAD	PHY Address: MII PHY Address
13-14	rsv	Reserved.
15	SQEDIS	Internal SQE Disable: Set this bit to disable the internal SQE check.

TP-PMD Control Register (04h)

In TP-PMD mode, the TP-PMD Control Register contains two control bits for the external PHY. This register resets to 061Fh.

15	14	13	12	11	10	9	8
rsv	rsv	rsv	rsv	rsv	rsv	rsv	rsv

7	6	5	4	3	2	1	0
rsv	rsv	rsv	rsv	rsv	rsv	-FO	-LB

Bits	Name	Description
0	-LB	Loopback: Set this bit low to drive the 100BASE-TX interface pin -LB low. This is used to perform the loopback function in the external PHY. To perform external loopback the SYM92C1000 must be in full duplex mode.
1	-FO	Fiber Optic Off: Set this bit low to drive the 100BASE-TX interface pin -FO low. This is used to turn off the external PHY fiber optic transmit circuit.
2-15	rsv	Reserved.

10BASE-T Control Register (04h)

In 10BASE-T mode, the 10BASE-T Control Register contains ten control bits for the external PHY. This register resets to 061Fh.

15	14	13	12	11	10	9	8
rsv	rsv	rsv	-AUIPS	-TPPS	-PDN	-LNKDIS	FLTRDIS

7	6	5	4	3	2	1	0
rsv	rsv	rsv	-ADPLX	-LONG	APOL	UTPSTP	-LB

Bits	Name	Description
0	-LB	Loopback Enable: Set this bit low to drive the 10BASE-T interface pin -LB low. To perform external loopback the SYM92C1000 must be in full duplex mode.
1	UTPSTP	Select UTP or STP: Set this bit high to drive the 10BASE-T interface pin UTPSTP high.
2	APOL	Autopolarity Enable: Set this bit high to drive the 10BASE-T interface pin APOL high
3	-LONG	Long Cable Mode: Set this bit low to drive the 10BASE-T interface pin -LONG low
4	-ADPLX	Autoduplex Enable: Set this bit low to drive the 10BASE-T interface pin -ADPLX low
5-7	rsv	Reserved.
8	FLTRDIS	Filter Disable: Set this bit high to drive the 10BASE-T interface pin FLTRDIS high.
9	-LNKDIS	Link Disable: Set this bit low to drive the 10BASE-T interface pin -LNKDIS low
11	-TPPS	Twisted Pair Port Select: Set this bit low to drive the 10BASE-T interface pin -TPPS low
12	-AUIPS	AUI Port Select: Set this bit low to drive the 10BASE-T interface pin -AUIPS low
13-15	rsv	Reserved.

MII WRITE DATA REGISTER (05h)

The MII Write Data Register contains the write data to the MII management register. This register is only valid in MII mode. A write to this register will initiate a write operation to the MII management register. On reset, this register is unknown.

15	14	13	12	11	10	9	8
CTLD	CTLD	CTLD	CTLD	CTLD	CTLD	CTLD	CTLD

7	6	5	4	3	2	1	0
CTLD	CTLD	CTLD	CTLD	CTLD	CTLD	CTLD	CTLD

Bits	Name	Description
0-15	CTLD	MII Control Data: This is the control data for the external MII PHY.

MII READ DATA REGISTER (06h)

The MII Read Data Register contains the read data from the MII management register. This register is only valid in MII mode. On reset, this register is unknown.

15	14	13	12	11	10	9	8
STD	STD	STD	STD	STD	STD	STD	STD

7	6	5	4	3	2	1	0
STD	STD	STD	STD	STD	STD	STD	STD

Bits	Name	Description
0-15	STD	MII Status Data: This is the status data from the external MII PHY.

MII INDICATORS REGISTER (07h)

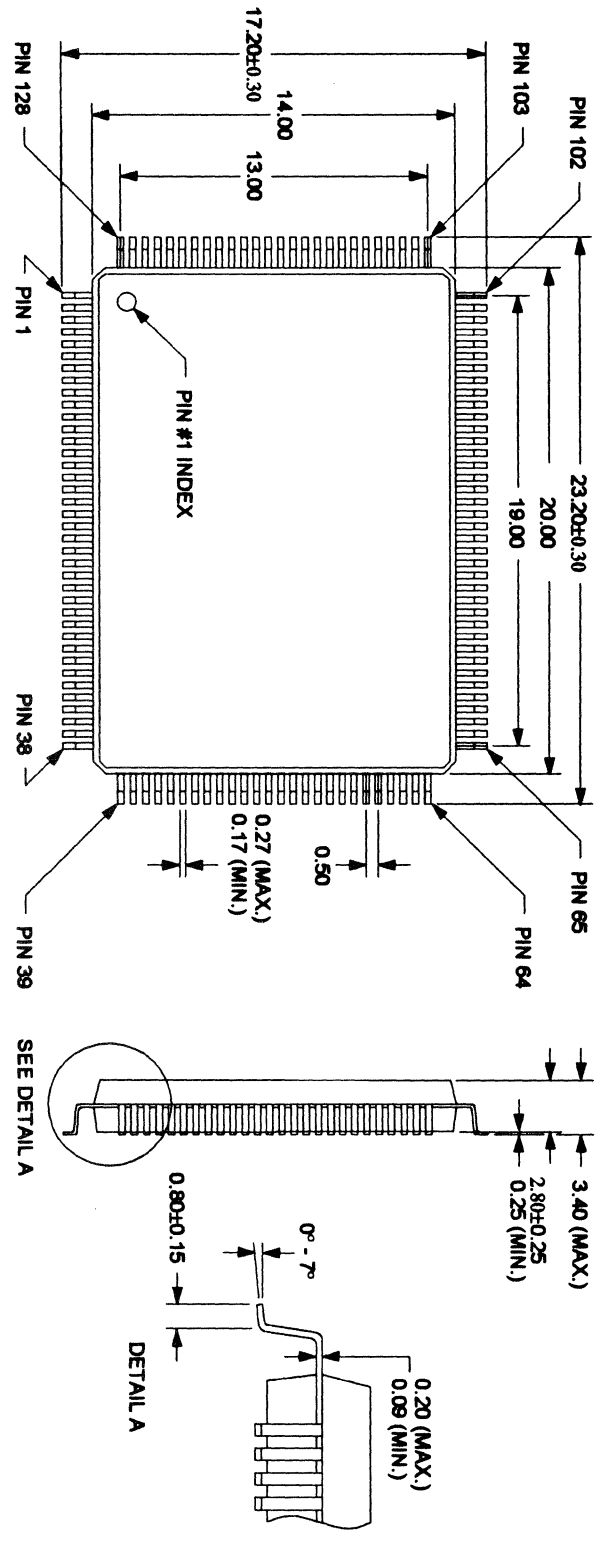
The MII Indicators Register contains the status of the MII management function. This read only register is only valid in MII mode. On reset, this register is 0000h.

15	14	13	12	11	10	9	8
rsv	rsv	rsv	rsv	rsv	rsv	rsv	rsv

7	6	5	4	3	2	1	0
rsv	rsv	rsv	rsv	rsv	NVALID	SCANNING	BUSY

Bits	Name	Description
0	BUSY	MII Management Busy: When this bit is one, the MII management function is busy. The host system must not issue an MII management command until this bit is zero. For a read operation, the MII Read Data Register is not valid until this bit is zero.
1	SCANNING	MII Scan Function Active: When this bit is one, the MII management function is performing the scan operation. The host system must not issue an MII management command until the host system sets this bit to zero by writing a zero to the SCAN bit of the MII Request register.
2	NVALID	Status Data Not Valid: When this bit is one, the MII management function is performing the scan operation and the first data read is not completed. The MII Read Data Register is not valid until this bit is zero.
3-15	rsv	Reserved.

MECHANICAL SPECIFICATIONS



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

ORDERING INFORMATION

The SYM92C1000 is available in a 128-pin Plastic Quad Flat Pack (PQFP). Use the following part number when ordering.

Package Type	Part Number
128-pin PQFP	SYM92C1000PM

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUMS

Symbol	Parameter	Minimum	Maximum	Units
V_{DD}	DC Power Supply Voltage	-0.5	7.0	V
V_{IN}, V_{OUT}	DC Input, Output Voltage	-0.5	V_{DD} + 0.5	V
I	DC Current Drain per VDD and VSS Pin Pairs	-	100	mA
T_{SIG}	Storage Temperature	-55	150	°C
T_L	Lead Temperature (Soldering 10 seconds maximum)	-	250	°C
T_{OPER}	Operating Temperature	0	70	°C

DC CHARACTERISTICS

Symbol	Parameter	Minimum	Maximum	Units
V_{IL}	Input Voltage, Low	-	0.8	V
V_{IH}	Input Voltage, High	2.0	-	V
V_{OL}	Output Voltage, Low	-	0.4	V
V_{OH}	Output Voltage, High	2.4	-	V
C_{IN}	Input Capacitance	10 typical		pF
C_{OUT}	Output Capacitance	10 typical		pF
I_{OLL}	Output Leakage Current	-	±10	µA
I_{IN}	Input Leakage Current	-	±10	µA
I_{DD}	Power Supply Current	-	TBD	mA
I_{OL}	Output Current, Low (4 mA, 0.4 V)	4	-	mA
I_{OL}	Output Current, Low (16 mA, 0.4 V)	16	-	mA
I_{OH}	Output Current, High (4 mA, 2.4 V)	-4	-	mA
I_{OH}	Output Current, High (16 mA, 2.4 V)	-16	-	mA

(V_{DD} = 4.5V to 5.5V, T_{OPER} = 0°C to 70°C)

AC CHARACTERISTICS

Host Interface Read and Host Interface Write Timing

Num	Description	Min.	Max.	Units
1	HCLK Period	30	-	ns
2	-HCS setup time	18	-	ns
3	-HCS hold time	0	-	ns
4	HRW setup time before -HCS asserted	0	-	ns
5	-HCS deasserted to HRW hold time	0	-	ns
6	HA(4:0) setup time before -HCS asserted	0	-	ns
7	-HCS deasserted to HA(4:0) hold time	0	-	ns
8	HD(15:0) propagation delay from -HCS asserted (read only)	0	30	ns
9	-HCS deasserted to HD(15:0) hold time (read only)	0	30	ns
10	HD(15:0) setup time before -HCS asserted (write only)	0	-	ns
11	-HCS deasserted to HD(15:0) hold time (write only)	0	-	ns

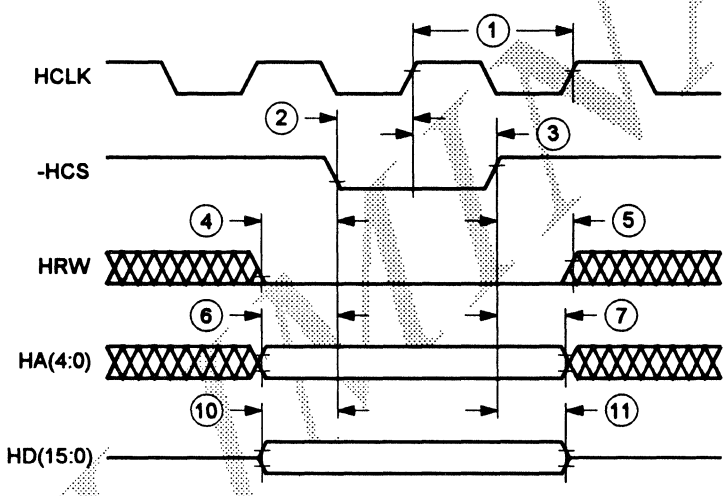


Figure 9 Host Interface Write Timing

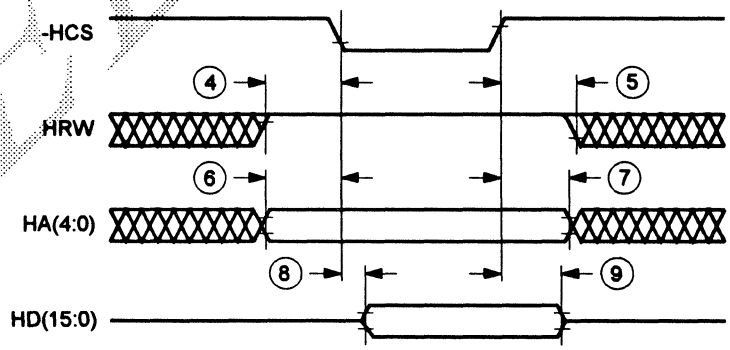


Figure 10 Host Interface Read Timing

Buffer Management Interface Receive Output Timing

Num	Description	Min.	Max.	Units
1	RXNCLK period (100 Mbps modes) RXNCLK period (10 Mbps mode)	39.996 399.96	40.004 400.04	ns
2	RXNCLK to RPSF propagation delay	0	20	ns
3	RPSF output hold time [1]	1 clk + 0	1 clk + 20	ns
4	RXNCLK to RPDV propagation delay	0	20	ns
5	RPDV output hold time [1]	1 clk + 0	1 clk + 20	ns
6	RXNCLK to RPD(7:0) propagation delay	0	20	ns
7	RPD(7:0) output hold time [1]	2 clks + 0	2 clks + 20	ns
8	RXNCLK to RPEF propagation delay	0	20	ns
9	RPEF output hold time [1]	1 clk + 0	1 clk + 20	ns
10	RXNCLK to RPST propagation delay	0	20	ns
11	RPST output hold time [1]	1 clk + 0	1 clk + 20	ns

Note [1]: All Buffer Receive signals are synchronous to RXNCLK, clk refers to one RXNCLK period, clks refers to multiple periods.

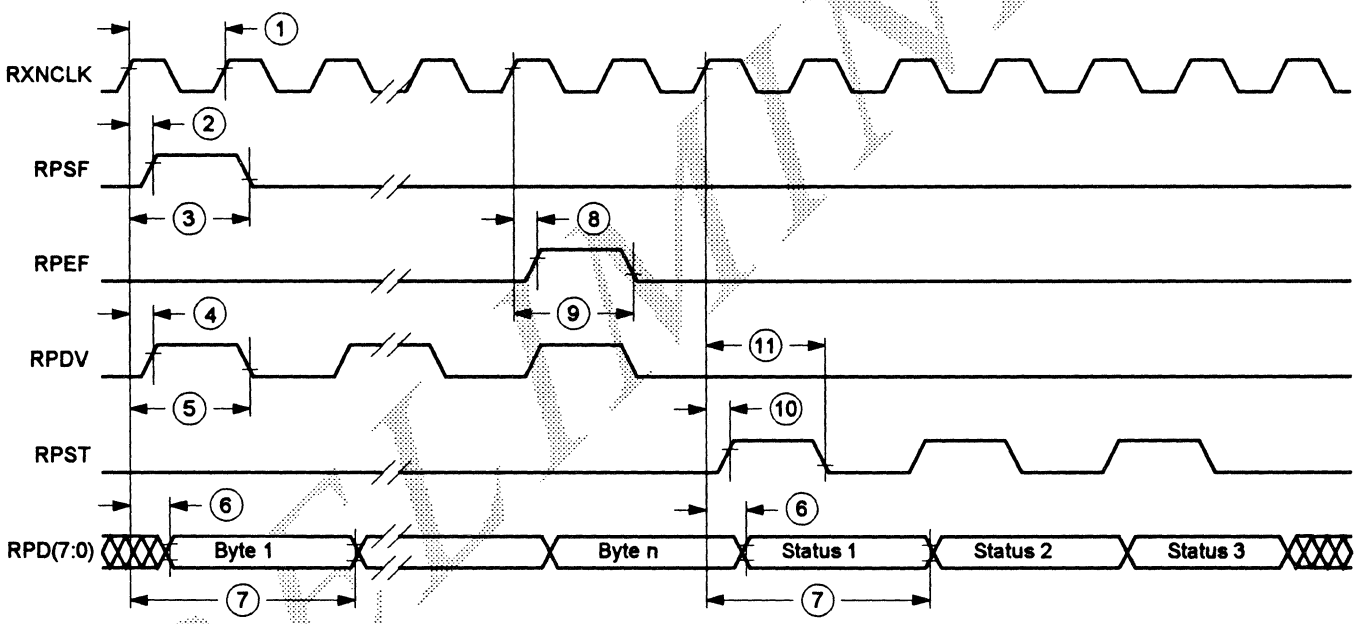


Figure 11 Buffer Management Interface Receive Timing

Buffer Management Interface Begin Normal Transmit

Num	Description	Min.	Max.	Units
1	TXNCLK period (100 Mbps modes) TXNCLK period (10 Mbps mode) TXNCLK period (between transmits, 10BASE-T mode only)	39.996 399.96 99.99	40.004 400.04 100.01	ns
2	TPSF setup time	22	-	ns
3	TPSF assertion to TPUD assertion (this is due to network traffic) [1,2]	16 clks + (2) + (6)	125000 clks + (2) + (6)	
4	TPDN output hold time [1,2]	1 clk + (2) + 0	1 clk + (2) + 15	ns
5	TPAB output hold time [1,2]	1 clk + (2) + 0	1 clk + (2) + 15	ns
6	TXNCLK to TPUD propagation delay	0	15	ns
7	TPSF hold time [1,3]	-	1 clk + 0	ns
8	TPD(7:0) setup time (NOTE: byte one must be asserted and held within sixteen clks of TPSF asserted)	22	-	ns
9	TPD(7:0) hold time [1]	1 clk + 0	-	ns

Note [1]: All Buffer Transmit signals are synchronous to TXNCLK, clk refers to one TXNCLK period, clks refers to multiple periods.

Note [2]: Numbers in parenthesis ( ) in the Min. and Max. columns refer to additional timing values referenced in the Num column

Note [3]: This timing must be met as a result of timing number 6 (TPUD asserted)

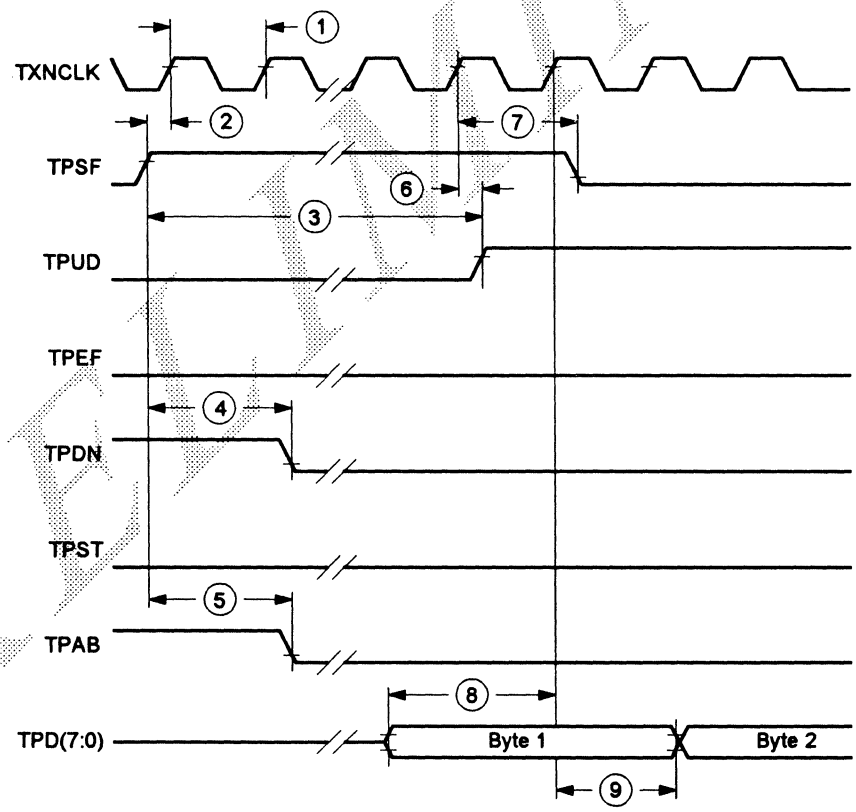


Figure 12 Buffer Management Interface Begin Normal Transmit Timing

Buffer Management Interface End Normal Transmit Timings

Num	Description	Min.	Max.	Units
1	TXNCLK period (100 Mbps modes) TXNCLK period (10 Mbps mode) TXNCLK period (between transmits, 10BASE-T mode only)	39.996 399.96 99.99	40.004 400.04 100.01	ns
2	TPEF asserted to TPUD deasserted [1,2]	2 clks+(3)+(4)	2 clks+(3)+(4)	
3	TPUD output hold time	0	15	ns
4	TPEF setup time	22	-	ns
5	TPEF hold time [1]	1 clk + 0	-	ns
6	TPEF asserted to TPDN asserted (CRC enabled) [1,2] TPEF asserted to TPDN asserted (CRC disabled) [1,2]	10clks+(4)+(9) 2 clks+(4)+(9)	- -	
7	TPD(7:0) setup time (transmit data presented)	22	-	ns
8	TPD(7:0) hold time (transmit data presented) [1]	1 clk + 0	-	ns
9	TXNCLK to TPDN propagation delay	0	15	ns
10	TXNCLK to TPST propagation delay	0	15	ns
11	TPDN asserted to TPST asserted [1,2]	1 clk-(9)+(10)	1 clk-(9)+(10)	
12	TPST output hold time [1]	2 clks + 0	2 clks + 15	ns
13	TXNCLK to TPD(7:0) propagation delay (Status Bytes from SYM92C1000)	0	15	ns
14	TPD(7:0) output hold time (Status Bytes from SYM92C1000) [1]	1 clk + 0	1 clk + 15	ns
15	TPST asserted to TPSF asserted [1]	3 clks	-	

Note [1]: All Buffer Transmit signals are synchronous to TXNCLK, clk refers to one TXNCLK period, clks refers to multiple periods.

Note [2]: Numbers in parenthesis ( ) in the Min. and Max. columns refer to additional timing values referenced in the Num column

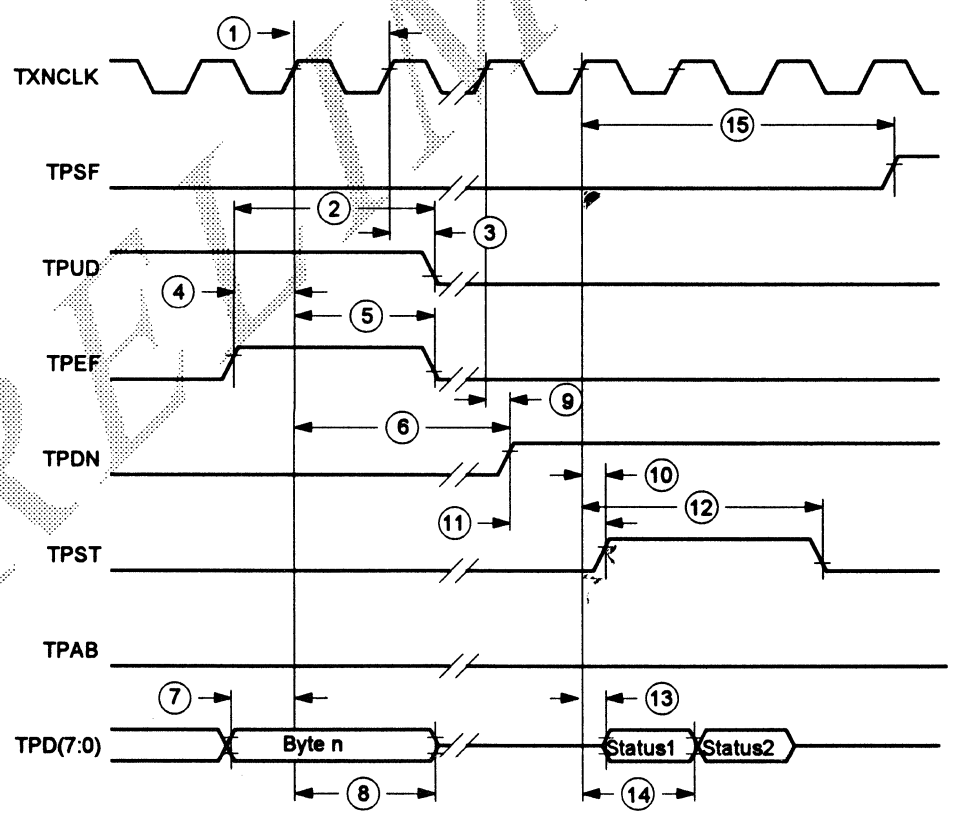


Figure 13 Buffer Management Interface End Normal Transmit Timing

Buffer Management Interface Transmit Underrun Abort Timing

Num	Description	Min.	Max.	Units
1	TXNCLK period (100 Mbps modes) TXNCLK period (10 Mbps mode) TXNCLK period (between transmits, 10BASE-T mode only)	39.996 399.96 99.99	40.004 400.04 100.01	ns
2	TPD(7:0) setup time (transmit data presented)	22	-	ns
3	TPD(7:0) hold time (transmit data presented) [1]	1 clk + 0	-	ns
4	TPUR setup time	22	-	ns
5	TPUR hold time [1]	1 clk + 0	-	ns
6	TPUR asserted to TPUD deasserted [1,2]	2 clks+(4)+(8)	-	-
7	TPUR asserted to TPAB asserted [1,2]	2 clks + (4) + (12)	-	-
8	TPUD output hold time	0	15	ns
9	TPAB asserted to TPST asserted [1,2]	1 clk - (12) + (10)	1 clk - (12) + (10)	
10	TXNCLK to TPST propagation delay	0	15	ns
11	TPST output hold time [1]	2 clks + 0	2 clks + 15	ns
12	TXNCLK to TPAB propagation delay	0	15	ns
13	TXNCLK to TPD(7:0) propagation delay (Status Bytes)	0	15	ns
14	TPD(7:0)output hold time (Status Bytes) [1]	1 clk + 0	1 clk + 15	ns
15	TPST asserted to TPSF asserted [1]	3 clks	-	

Note [1]: All Buffer Transmit signals are synchronous to TXNCLK, clk refers to one TXNCLK period, clks refers to multiple periods.

Note [2]: Numbers in parenthesis ( ) in the Min. and Max. columns refer to additional timing values referenced in the Num column

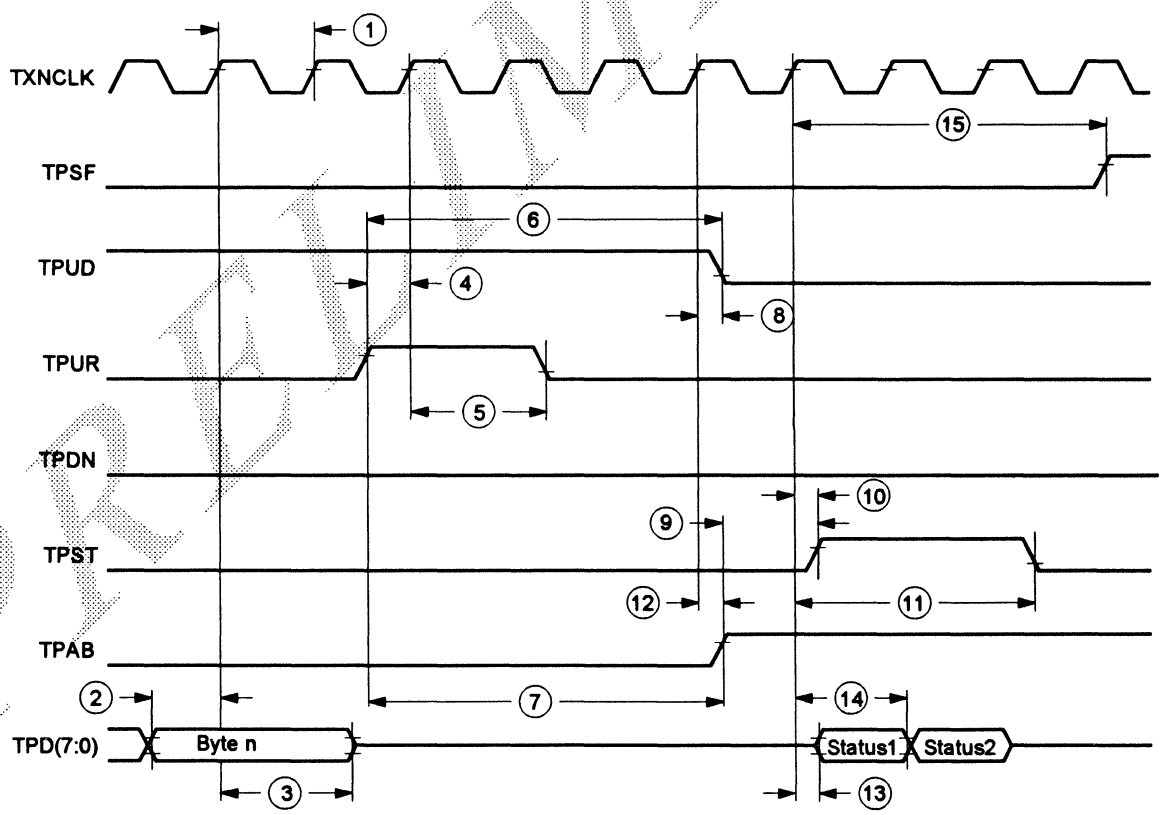


Figure 14 Buffer Management Interface Transmit Underrun Abort Timing

Buffer Management Interface Transmit Retry Timing

Num	Description	Min.	Max.	Units
1	TXNCLK period (100 Mbps modes) TXNCLK period (10 Mbps mode) TXNCLK period (between transmits, 10BASE-T mode only)	39.996 399.96 99.99	40.004 400.04 100.01	ns
2	TPUD output hold time (same clock as TPRT asserted)	0	15	ns
3	TXNCLK to TPRT propagation delay	0	15	ns
4	TPRT asserted to TPSF asserted [1,2]	1 clk - (5)	-	ns
5	TPSF setup time	22	-	ns
6	TPSF asserted to TPRT deasserted [1,2]	1 clk + (5) + 0	1 clk + (5) + 15	ns
7	TPD(7:0) Byte 1 must be presented within 16 TXNCLK periods of TPSF asserted, subject to begin normal transmit setup time	-	-	-

Note [1]: All Buffer Transmit signals are synchronous to TXNCLK, clk refers to one TXNCLK period, clks refers to multiple periods.

Note [2]: Numbers in parenthesis ( ) in the Min. and Max. columns refer to additional timing values referenced in the Num column

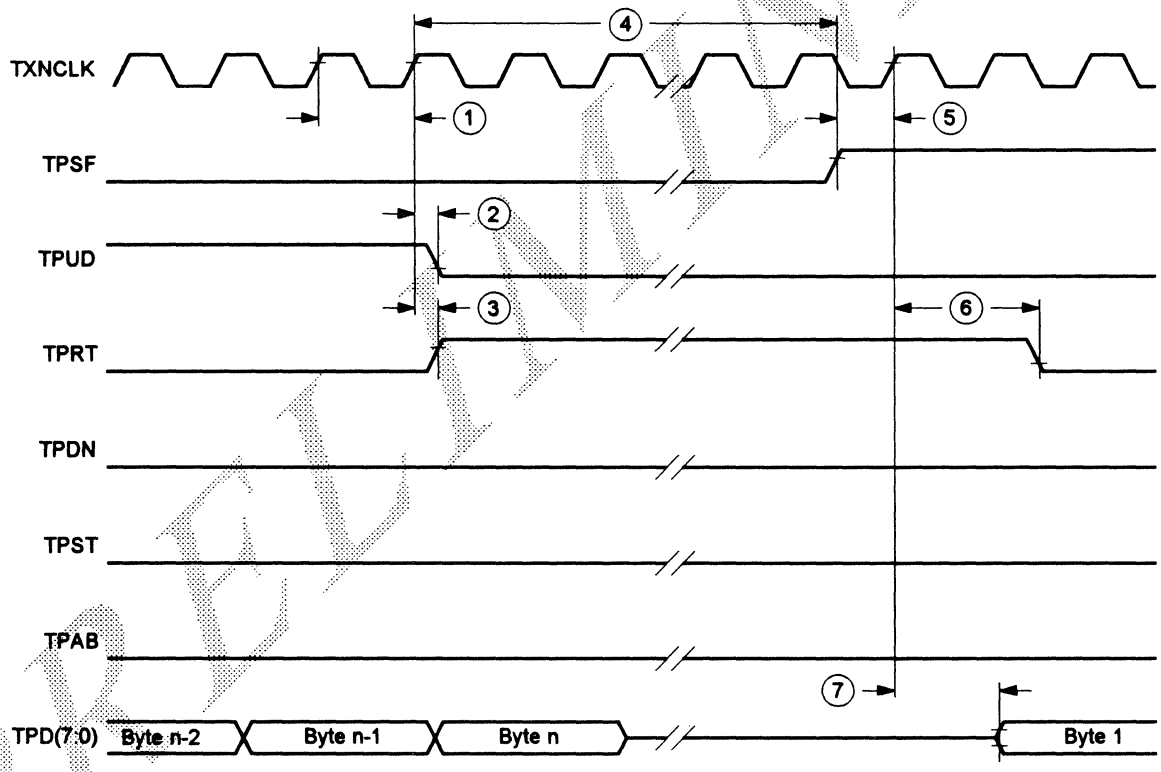


Figure 15 Buffer Management Interface Transmit Retry Timing

MII Receive and MII Transmit Function Timing

Num	Description	Min.	Max.	Units
1	RXCLK period	39.996	-	ns
2	RXDV setup time	10	-	ns
3	RXDV hold time	10	-	ns
4	RXER setup time	10	-	ns
5	RXER hold time	10	-	ns
6	RXD(3:0) setup time	10	-	ns
7	RXD(3:0) hold time	10	-	ns
8	TXCLK period	39.996	-	ns
9	TXCLK to TXEN propagation delay	0	15	ns
10	TXEN output hold time [1]	1 clk + 0	1 clk + 15	ns
11	TXCLK to TXER propagation delay	0	15	ns
12	TXER output hold time [1]	1 clk + 0	1 clk + 15	ns
13	TXCLK to TXD(3:0) propagation delay	0	15	ns
14	TXD(3:0) output hold time [1]	1 clk + 0	1 clk + 15	ns

Note [1]: All MII Transmit and Receive signals are synchronous to TXCLK and RXCLK respectively, clk refers to one TXCLK period

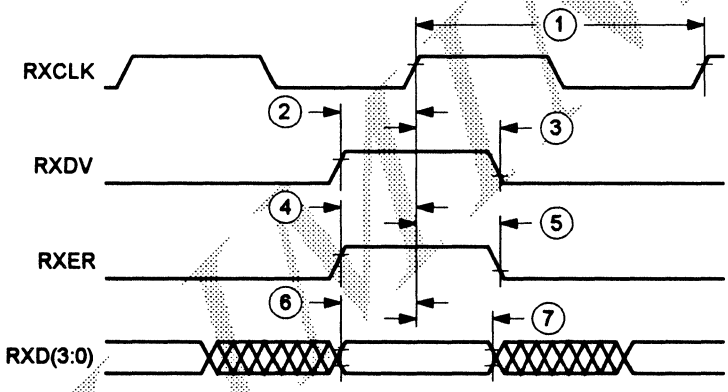


Figure 16 MII Receive Function Timing

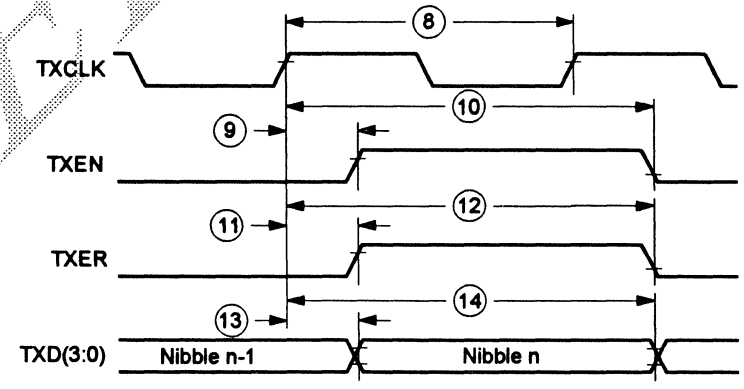


Figure 17 MII Transmit Function Timing

MII Management Input and MII Management Output Timing

Num	Description	Min.	Max.	Units
1	MDC period	399.96	-	ns
2	MDIO setup time (input only)	100	-	ns
3	MDIO hold time (input only)	0	-	ns
4	MDC to MDIO propagation delay (output only)	10	390	ns
5	MDIO output hold time (output only) [1]	1 clk + 10	1 clk + 390	ns

Note [1]: All MII Management Input and Output signals are synchronous to MDC, clk refers to one MDC period

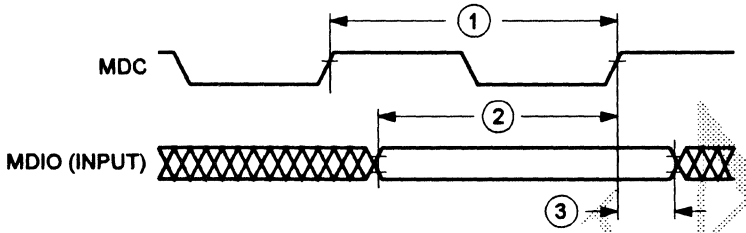


Figure 18 MII Management Input Timing

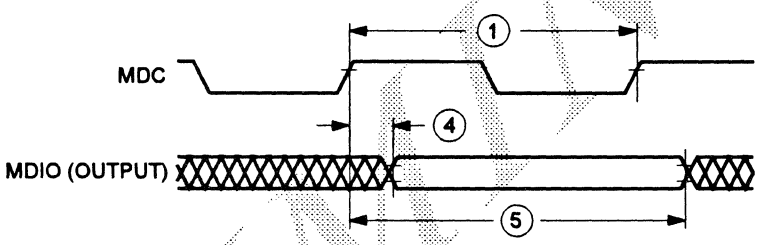


Figure 19 MII Management Output Timing

TP-PMD Receive, TP-PMD Transmit, and TP-PMD Control Function Timing

Num	Description	Min.	Max.	Units
1	RXCLK period	39.996	40.004	ns
2	RSM(4:0) setup time	10	-	ns
3	RSM(4:0) hold time	10	-	ns
4	TXCLK period	39.996	40.004	ns
5	SDO setup time	10	-	ns
6	SDO hold time	0	-	ns
7	TXCLK to TSM(4:0) propagation delay	2.5	15	ns
8	TSM(4:0) output hold time [1]	1 clk + 0	1 clk + 15	ns
9	-HCS pulse width	25	-	ns
10	-HCS to -FO propagation delay	0	25	ns
11	-HCS to -LB propagation delay	0	25	ns

Note [1]: All TP-PMD Transmit and Receive signals are synchronous to TXCLK and RXCLK respectively, clk refers to one TXCLK period

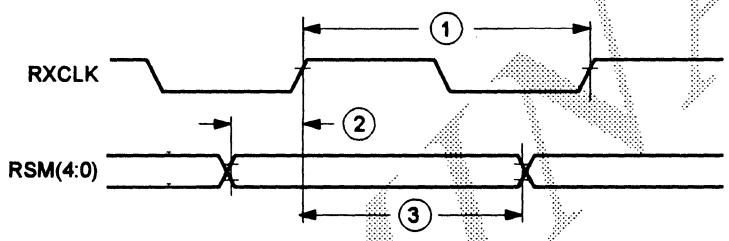


Figure 20 TP-PMD Receive Function Timing

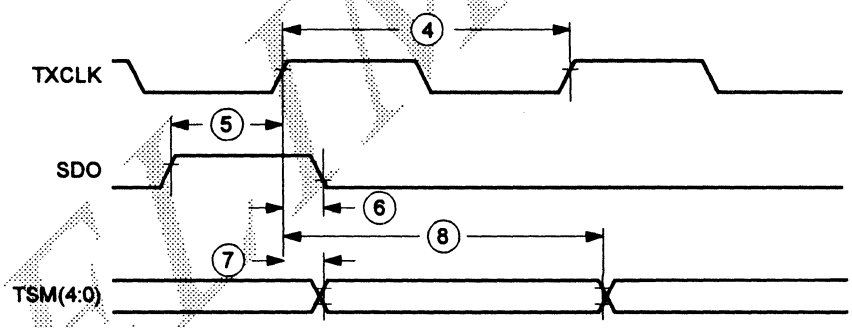


Figure 21 TP-PMD Transmit Function Timing

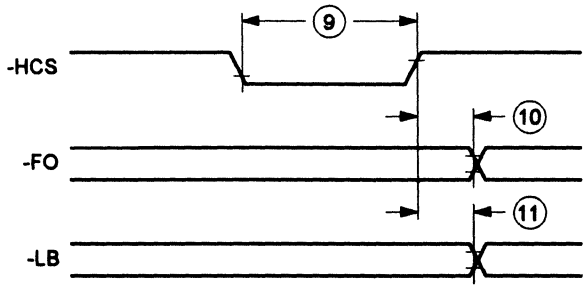


Figure 22 TP-PMD Control Function Timing

10BASE-T Receive, 10BASE-T Transmit, and 10BASE-T Control Function Timing

Num	Description	Min.	Max.	Units
1	RXCLK period	399.96	400.04	ns
2	CRS setup time	10	-	ns
3	CRS hold time	10	-	ns
4	RXD setup time	10	-	ns
5	RXD hold time	10	-	ns
6	TXCLK period	399.96	400.04	ns
7	TXCLK to TXEN propagation delay	0	25	ns
8	TXEN output hold time	0	25	ns
9	TXCLK to TXD propagation delay	0	25	ns
10	TXD output hold time [1]	1 clk + 0	1 clk + 25	ns
11	-HCS pulse width	25	-	ns
12	-HCS to 10BASE-T Control Pins propagation delay	0	25	ns

Note [1]: All 10BASE-T Transmit and Receive signals are synchronous to TXCLK and RXCLK respectively, clk refers to one TXCLK period

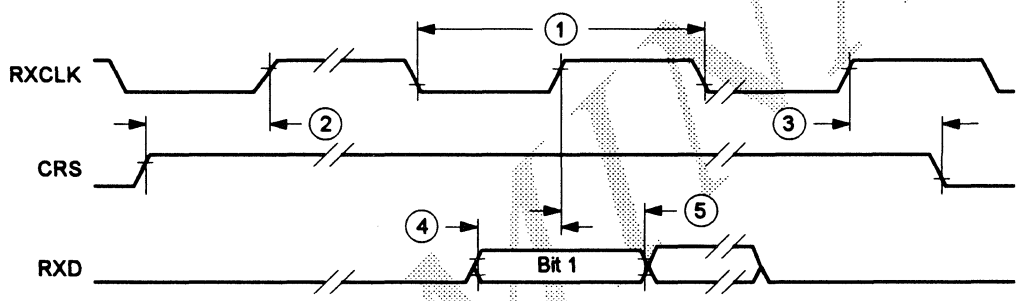


Figure 23 10BASE-T Receive Function Timing

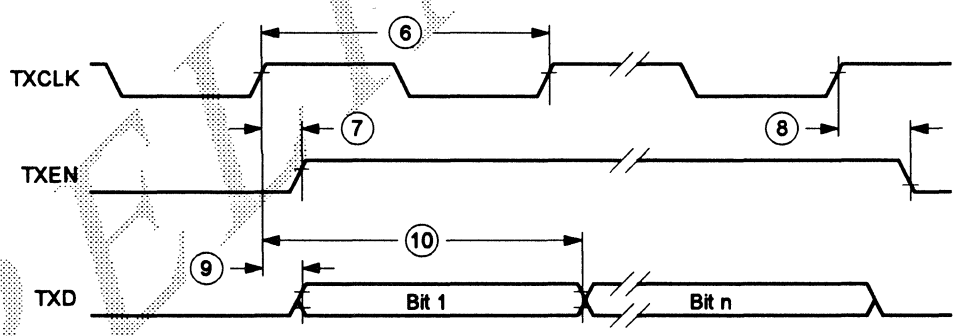


Figure 24 10BASE-T Transmit Function Timing

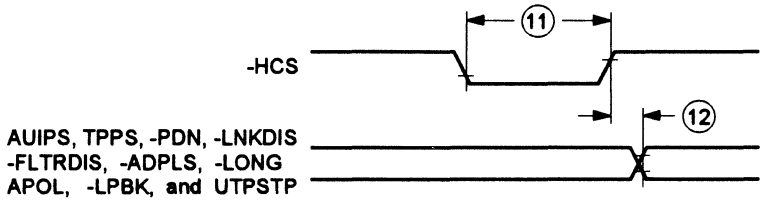


Figure 25 10BASE-T Control Function Timing

JTAG Function Timing

Num	Description	Min.	Max.	Units
1	TCK period	100	-	ns
2	TMS setup time to TCK rising edge	10	-	ns
3	TCK rising edge to TMS hold time	0	-	ns
4	TCK falling edge to TDO propagation delay	-	20	ns
5	TDI setup time to TCK rising edge	10	-	ns
6	TCK rising edge to TDI hold time	25	-	ns
7	Functional output and bi-directional pin propagation delay from TCK falling edge	-	40	ns
8	Functional input and bi-directional pin setup time to TCK rising edge	5	-	ns
9	TCK rising edge to Functional input and bi-directional pin hold time	25	-	ns

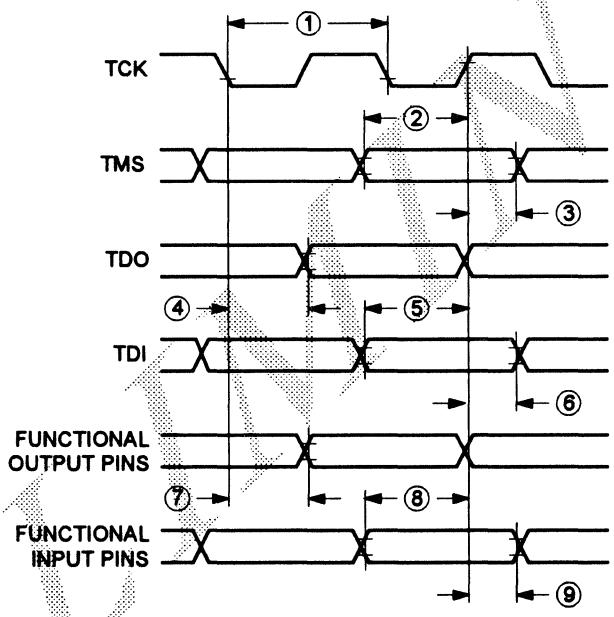


Figure 26 JTAG Function Timing

CLOCK SPECIFICATIONS

HOST AND JTAG CLOCKS

Description	Min.	Typ.	Max.	Units
HCLK Period	30	-	-	ns
HCLK High Time	40	-	60	%
HCLK Low Time	40	-	60	%
TCK Period	100	-	-	ns
TCK High Time	40	-	-	ns
TCK Low Time	40	-	-	ns

TP-PMD CLOCKS

Description	Min.	Typ.	Max.	Units
RXCLK Period	39.996	40	40.004	ns
RXCLK High Time	10	-	-	ns
RXCLK Low Time	20	-	-	ns
RXNCLK Period	39.996	40	40.004	ns
RXNCLK High Time	10	-	-	ns
RXNCLK Low Time	20	-	-	ns
TXCLK Period	39.996	40	40.004	ns
TXCLK High Time	15	-	-	ns
TXCLK Low Time	15	-	-	ns
TXNCLK Period	39.996	40	40.004	ns
TXNCLK High Time	15	-	-	ns
TXNCLK Low Time	15	-	-	ns

10BASE-T CLOCKS

Description	Min.	Typ.	Max.	Units
RXCLK Period	99.99	100	100.01	ns
RXCLK High Time	40	-	200	ns
RXCLK Low Time	40	-	60	ns
RXNCLK Period	-	400	-	ns
RXNCLK High Time	160	-	360	ns
RXNCLK Low Time	160	-	360	ns
TXCLK Period	99.99	100	100.01	ns
TXCLK High Time	40	-	60	ns
TXCLK Low Time	40	-	60	ns
TXNCLK Period during transmission	399.96	400	400.04	ns
TXNCLK High Time during transmission	40	-	60	ns
TXNCLK Low Time during transmission	340	-	360	ns
TXNCLK Period between transmission	99.99	100	100.01	ns
TXNCLK High Time between transmission	40	-	60	ns
TXNCLK Low Time between transmission	40	-	60	ns

MII CLOCKS

Description	Min.	Typ.	Max.	Units
RXCLK Period (25 MHz)	39.996	40	40.004	ns
RXCLK High Time (25 MHz)	14	-	26	ns
RXCLK Low Time (25 MHz)	14	-	26	ns
RXNCLK Period (25 MHz)	39.996	40	40.004	ns
RXNCLK High Time (25 MHz)	14	-	26	ns
RXNCLK Low Time (25 MHz)	14	-	26	ns
TXCLK Period (25 MHz)	39.996	40	40.004	ns
TXCLK High Time (25 MHz)	14	-	26	ns
TXCLK Low Time (25 MHz)	14	-	26	ns
TXNCLK Period (25 MHz)	39.996	40	40.004	ns
TXNCLK High Time (25 MHz)	14	-	26	ns
TXNCLK Low Time (25 MHz)	14	-	26	ns
RXCLK Period (2.5 MHz)	399.96	400	400.04	ns
RXCLK High Time (2.5 MHz)	140	-	260	ns
RXCLK Low Time (2.5 MHz)	140	-	260	ns
RXNCLK Period (2.5 MHz)	399.96	400	400.04	ns
RXNCLK High Time (2.5 MHz)	140	-	260	ns
RXNCLK Low Time (2.5 MHz)	140	-	260	ns
TXCLK Period (2.5 MHz)	399.96	400	400.04	ns
TXCLK High Time (2.5 MHz)	140	-	260	ns
TXCLK Low Time (2.5 MHz)	140	-	260	ns
TXNCLK Period (2.5 MHz)	399.96	400	400.04	ns
TXNCLK High Time (2.5 MHz)	140	-	260	ns
TXNCLK Low Time (2.5 MHz)	140	-	260	ns
MDC Period	400	-	-	ns
MDC High Time	160	-	-	ns
MDC Low Time	160	-	-	ns

NOTES

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