Microelectronic Products Division
Colorado Springs

NCR 86C05

"MEAN" I/O

Data Manual

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MicroChannel is a trademark of IBM
AT is a trademark of IBM
NuBus is a trademark of Texas Instruments

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86C05 Features

- Connects to the following host buses:
    1. IBM MicroChannel Bus
    2. IBM AT (ISA) Bus
    3. EISA Bus
    4. Apple NuBus
- Master mode host bus operation with programmable data transfer width of 8, 16, or 32 bits
- Data transfer rate to 20 MBytes/sec
- Three independent host bus ports and interrupts to support multi-processing environments.
- Programmable host bus parameters; arbitration level, etc.
- On chip 32 word deep by 32 bit FIFO
- Programmable FIFO throttle which produces an extremely high host bus utilization
- 24 bit host bus address counter (32 bit NuBus)
- 24 bit transfer counter
- Six configuration registers
- Six user defined host I/O registers
- 8 or 16 bit DMA interface supports DMA controller or DMA device operation
- Programmable conditions for control microprocessor interrupt
- Connects to a non-multiplexed or multiplexed (address/data) control microprocessor bus
- BIOS PROM support
- Lock host bus and set semaphore command
- Clock rate to 40 MHz
- Built in host bus drivers for control signals
- Internal power on reset and flag
- Single +5 volt supply, CMOS low power consumption

Chapter 1
Functional Description

1.1 INTRODUCTION

1.1.1 General Description

As shown in Figure 1, the NCR 86C05 provides a single chip "master mode" host interface to the MicroChannel, EISA, AT, or NuBus. The 86C05 performs data transfers to 20 MBytes/sec. Eight, sixteen, or thirty two bit data transfers are supported on the host interface. A 32 word deep by 32 bit FIFO is provided to buffer data transfers between the host interface and the DMA or microprocessing unit (MPU).

The DMA interface is programmable to support eight or sixteen bit transfers to a local DMA controller or intelligent peripheral. The 86C05 supports a simple REQ/ACK handshake and it also provides parity for each eight bits on the DMA bus. The DMA interface may be programmed to operate in DMA controller or DMA device mode.

When the DMA interface is configured for 8 bit transfers then the high byte of the DMA interface (bits 8–15) may be used to carry the high byte (bits 8–15) of the MPU interface. This provides the capability for the MPU to transfer 8 or 16 bits of data to the host or DMA interface.

All 86C05 MPU registers are eight bits wide. The 86C05 connects directly to a non-multiplexed or multiplexed (address/data) MPU bus, thus supporting most popular microprocessors including Z8, 8051, and 80188/80186.

To help simplify interface logic even further the 86C05 provides a built in BIOS PROM support logic. The PROM provides the host operating system with initialization parameters for the 86C05 and may also provide routines to communicate with the I/O card.

The 86C05 is available in a 160 pin quad plastic flat pack.

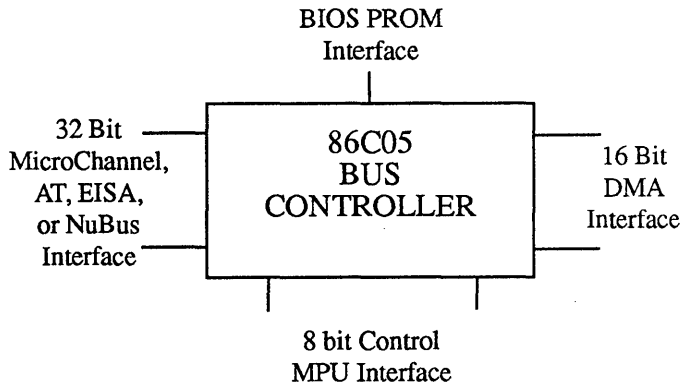


Figure 1. Data Flow through the 86C05

1.1.2 Block Diagram

The block diagram of the 86C05 is shown on the following page. This illustration shows the MicroChannel host interface:

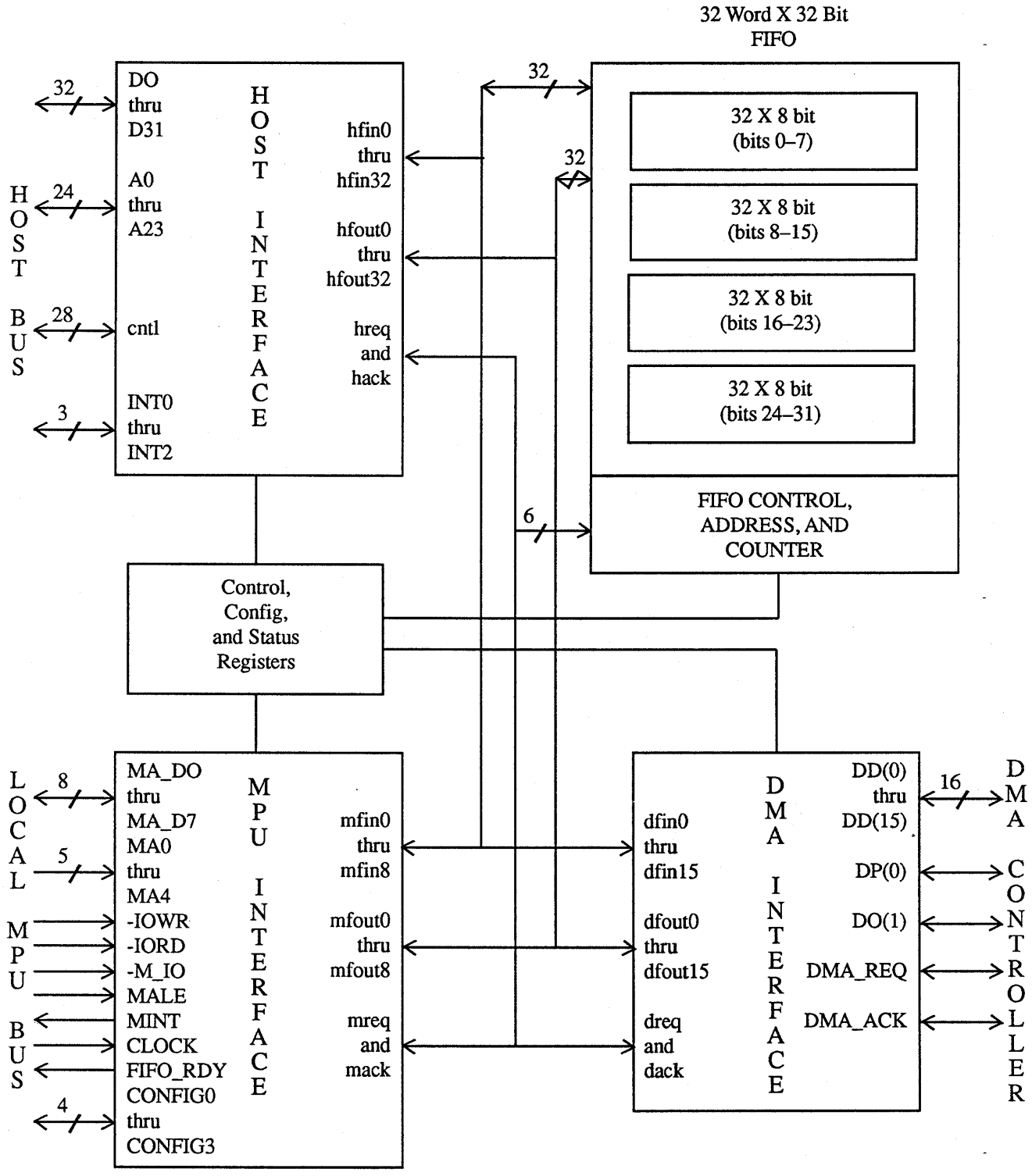


Figure 2. Block diagram of the 86C05

1.2 OVERVIEW

1.2.1 Host Interface

The 86C05 provides all the control and data signals to interface to the MicroChannel, EISA, AT, or NuBus host buses (transceivers required on most lines). Bus selection is made via configuration pins on the 86C05. Host bus parameters are programmable as outlined below:

a. Data Width - The firmware engineer may configure host data transfers in any width combinations (8, 16, or 32). Data is packed and unpacked in the on-chip FIFO. For the MicroChannel and AT host buses the 86C05 transfers to memory sizes smaller then specified. For example, if a 16 bit host transfer was requested but host memory is only 8 bits wide then the 86C05 performs two eight bit transfers. Data transfers can occur to/from I/O or Memory Space.

b. FIFO Throttle - Since the 86C05 operates in bus master mode the maximum number of burst transfers per host bus ownership is programmable from 1 to 64 bus cycles. In addition the 86C05 supports a hog mode which causes the chip to stay on the bus until one of the following events occur:

1. A higher priority device requests the bus

2. The FIFO is full

3. The transfer counter is equal to zero and the FIFO is empty

c. Host Interrupts - To facilitate multiprocessing environments the 86C05 provides three independent host interface interrupts.

d. Arbitration Priority - The host bus arbitration priority is programmable.

e. I/O Registers - Six general purpose I/O registers are provided for communication between the host system and the local MPU.

1.2.2 DMA Interface

The DMA Interface transfers 8 or 16 bit data to logic contained on the I/O card. This logic could be a DMA controller or any device that supports the REQ/ACK handshake. The interface is configurable to act as a DMA controller (8237 handshake with RD / -WRT strobes) or a DMA device. In DMA device mode the 86C05 asserts the DMA_REQ signal and expects to send/receive data when the DMA_ACK signal is received. When the 86C05 is operating as a DMA controller it receives a REQ signal from a device on the I/O card and sends/receives data when it asserts the ACK signal.

When the DMA interface is configured for 8 bit transfers then the high byte of the DMA interface (bits 8–15) may be used to carry the high byte (bits 8–15) of the MPU interface. This provides the capability for the MPU to transfer 8 or 16 bits of data to the host or DMA interface.

In addition, the 86C05 can transfer 8 bit DMA data over either the high or low byte. This feature helps the firmware engineer "clean-up" word transfers with odd transfer counts.

1.2.3 MPU Interface

The microprocessor (MPU) on the I/O card controls all data flow through the card and communicates to the host system via the 86C05. In a typical system, the code contained within the BIOS PROM would communicate an operating system request to the I/O registers on the 86C05. A write to these registers would generate an interrupt to the local MPU on the I/O card. The MPU would then direct the 86C05 to fetch the command block from system memory and transfer it to local MPU memory. The MPU would then decode the command and direct the data flow, for example from the DMA interface to host memory. It should be noted from this example that data can flow through the 86C05 in any direction from the the host, DMA, or MPU interface.

1.2.4 BIOS PROM Interface

The four host buses supported by this product require a BIOS PROM to aid the operating system in configuring and using the I/O card. The code contained within the BIOS PROM is executed by the operating system to initialize the 86C05, the I/O card, and inform the operating system of the I/O card presents. It may also provide the interface routines which communicate between an I/O driver and the I/O card (86C05). It should be noted that when the BIOS PROM interface is 8 data bits wide, any code run directly from this PROM will execute slowly. For higher performance systems the BIOS code should be copied into system RAM and executed from RAM. The method used to

provide the BIOS PROM with a latched address bus is specified below:

a. NuBus - 18 bits of latched memory address bus is provided by the 86C05.

b. MicroChannel - External address latches must be provided when interfacing to this bus. The address range is specified in register 6 and is used by the 86C05 to gate PROM data to the MicroChannel.

c. AT/EISA Bus - Since the lower address bits, SA(0–19), are latched by the AT/EISA Bus these lines connect directly to the address pins of the BIOS PROM. As with MicroChannel explained above, register 6 specifies the address range for the BIOS PROM.

1.3 REGISTERS

1.3.1 86C05 Register Organization

Register numbers 0–13 are shared between the host interface and the MPU interface. They are used for communication between the system processor and the MPU. Registers 15–31 are for the exclusive use on the local MPU and are used to control the operation of the 86C05. In Table 1, the I/O register definitions are proceeded by an access code letter as outlined below:

H = Host Access
M = MPU Access

TABLE 1. REGISTER ASSIGNMENTS AND ADDRESSING

Address					Register	Register Function	
4	3	2	1	0	Number	Write	Read
0	0	0	0	0	0 (00h)	M - Config 0	H - Config 0
0	0	0	0	1	1 (01h)	M - Config 1	H - Config 1
0	0	0	1	0	2 (02h)	HM - Config 2	HM - Config 2
0	0	0	1	1	3 (03h)	HM - Config 3	HM - Config 3
0	0	1	0	0	4 (04h)	HM - Config 4	HM - Config 4
0	0	1	0	1	5 (05h)	HM - Config 5	HM - Config 5
0	0	1	1	0	6 (06h)	HM - Config 6	HM - Config 6
0	0	1	1	1	7 (07h)	HM - I/O Port	HM - I/O Port
0	1	0	0	0	8 (08h)	HM - I/O Cmd 0	HM - I/O Stat 0
0	1	0	0	1	9 (09h)	HM - I/O Cmd 1	HM - I/O Stat 1
0	1	0	1	0	10 (0Ah)	HM - I/O Cmd 2	HM - I/O Stat 2
0	1	0	1	1	11 (0Bh)	H - I/O Data 0	M - I/O Data 0
0	1	1	0	0	12 (0Ch)	H - I/O Data 1	M - I/O Data 1
0	1	1	0	1	13 (0Dh)	H - I/O Data 2	M - I/O Data 2
0	1	1	1	0	14 (0Eh)	Not Defined	Not Defined
0	1	1	1	1	15 (0Fh)	System Control	System Status
1	0	0	0	0	16 (10h)	System Config	Not Defined
1	0	0	0	1	17 (11h)	Host Control 0	Host Status 0
1	0	0	1	0	18 (12h)	Host Control 1	Host Status 1
1	0	0	1	1	19 (13h)	Host Blk Count	Revision Number
1	0	1	0	0	20 (14h)	Host Preempt Time	Not Defined
1	0	1	0	1	21 (15h)	DMA Control	Not Defined
1	0	1	1	0	22 (16h)	Xfer Command	Extended Status
1	0	1	1	1	23 (17h)	Interrupt Mask	Interrupt Status
1	1	0	0	0	24 (18h)	Xfer Count 0–7	Xfer Count 0–7
1	1	0	0	1	25 (19h)	Xfer Count 8–15	Xfer Count 8–15
1	1	0	1	0	26 (1Ah)	Xfer Count 16–23	Xfer Count 16–23
1	1	0	1	1	27 (1Bh)	Host Address 0–7	Host Address 0–7
1	1	1	0	0	28 (1Ch)	Host Address 8–15	Host Address 8–15
1	1	1	0	1	29 (1Dh)	Host Address 16–23	Host Address 16–23
1	1	1	1	0	30 (1Eh)	Host Address 24–31	Host Address 24–31
1	1	1	1	1	31 (1Fh)	MPU Data Buffer	MPU Data Buffer

Register 0, 1 (00h, 01h) - Configuration 0 and 1

WRITE (mpu) / READ (host)

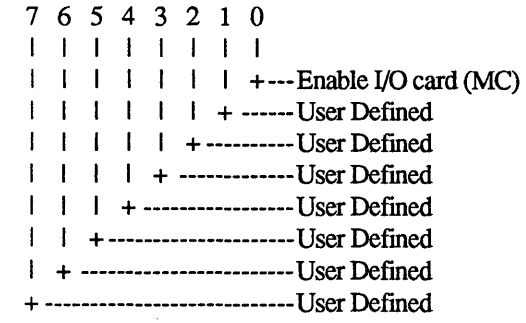
When the host interface is the MicroChannel or EISA buses, these registers must contain a unique card slot ID during I/O card set-up. After this initialization is completed, or for the NuBus or the AT interface these registers are defined by the user. This register is not affected by a firmware or hard reset.

Register 2 (02h) - Configuration 2

This register contains configuration data that is written by the host or local MPU. When the host interface is EISA, this register must contain byte 2 of the card slot ID during I/O card initialization. This register is not affected by a firmware or hard reset.

WRITE (host and mpu) / READ (host and mpu)

REGISTER 2 (02h) FUNCTION



Bit 0 - This bit is pre-defined for MicroChannel operation. It is user defined for all other host buses. For MicroChannel operation this bit is cleared anytime the 86C05 is hard reset. The host processor would typically initialize the I/O registers and then write a one to this bit thus enabling the card (and chip) for normal operation. When this bit is cleared the 86C05 does not respond to any host bus access (except set-up).

Bits 1–7 - User Defined

Register 3 (03h) - Configuration 3

This register contains the I/O address of the 86C05 chip when it is interfaced to the MicroChannel or AT host bus. The reader should note that after a power-up condition the 86C05 does not respond to an I/O address until after this register has been written (MicroChannel or AT bus only).

For EISA bus operation this register must contain byte 3 of the card slot ID during I/O card initialization. Once initialization is completed this register is available for general I/O communications between the host and local MPU. The reader should note that the base I/O address (EISA bus) for this chip is hard wired to ZC80h (where Z is EISA bus slot specific).

When the 86C05 is interfaced to the NuBus this register is used for general purpose configuration. The I/O address space of the NuBus is FSX000II where S is equal to the slot ID bits 3–0, F and 0 are the hexadecimal digits, X is don't care, and I is the 32 I/O register decode. Each card in the NuBus backplane is hardwired for a unique slot ID from 0h to Fh.

WRITE (host and mpu) / READ (host and mpu)

For MicroChannel operation the I/O address placed in this register is compared against address bits 15–8. The I/O address is written by the Host processor during I/O card configuration.

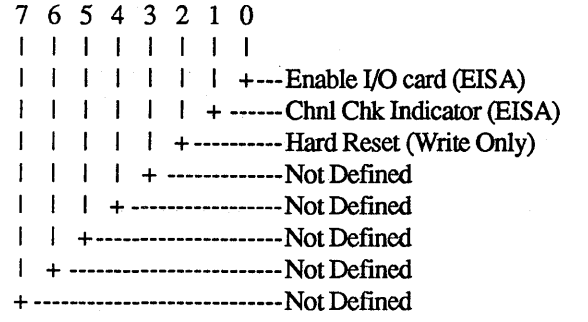
When this chip interfaces to the AT bus the I/O address placed in this register is compared against the AT address bits 9–5. The I/O address is written to this register by the local MPU as soon as possible after power-up.

Register 4 (04h) - Configuration 4

This register provides the capability for the firmware engineer to hard reset the 86C05 chip. Bits 0, 1, and 2 are cleared by a hard reset. Bit 1 is also cleared by a firmware reset.

WRITE (host and mpu) / READ (host and mpu)

REGISTER 4 (04h) FUNCTION



Bit 0 - This bit is pre-defined for EISA operation. It is user defined for all other host buses. This bit is cleared anytime the 86C05 is hard reset. The host processor would typically initialize the I/O registers and then write a one to this bit thus enabling the card for normal operation. This bit does not disable or enable any 86C05 functions.

Bit 1 - When this bit is asserted the EISA bus I/O CHCK signal is asserted. For all other host bus this bit is user defined.

Bit 2 - This latched bit provides a hard reset to the 86C05 chip. This programmable reset is similar to a host or power-up reset with the following exceptions:

1. Registers 2, 3, 5, 6, and 16 are not reset

2. NuBus slave logic is not reset

3. Dual port register control logic is not reset

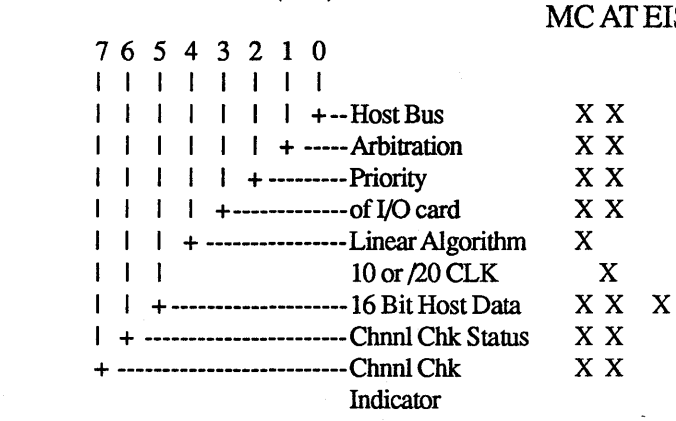
Bits 3–7 - These bits are not defined and should not be used by the firmware engineer.

Register 5 (05h) - Configuration 5

This register is user defined when the host interface is the NuBus and it is pre-defined for MicroChannel, EISA, and AT operation as outlined below. It is cleared by a hard reset.

WRITE (host and mpu) / READ (host and mpu)

REGISTER 5 (05h) FUNCTION DEFINED FOR



Bits 0–3 - These bits indicate the arbitration priority for the MicroChannel and DMA Channel usage for the AT Bus. For MicroChannel operation a hexadecimal value of F (1111) has the lower priority and a hexadecimal value of 0 (0000) has the highest priority.

For AT bus operation the 86C05 asserts the DRQ signal as shown below:

Bits 3 2 1 0	86C05 DMA Request Signal
0 0 0 1	DRQ(0)
0 0 1 0	DRQ(1)
0 1 0 0	DRQ(2)

The slot specific master request signal (-MREQx) is asserted when the 86C05 requires EISA bus access.

The NuBus arbitration priority is set by ID(0–3) pins. Therefore for NuBus operation these bits are user defined.

Bit 4 - For MicroChannel operation, when this bit is deasserted the 86C05 implements the fairness algorithm for host bus arbitration. When this bit is asserted the 86C05 implements the linear priority arbitration algorithm.

For AT operation, this bit indicates the number of 86C05 clocks (25ns) the chip should wait from the time DMA

acknowledge is received until the 86C05 starts to access the AT Bus. When this bit is asserted the 86C05 waits 10 clocks and when it is deasserted it waits 20 clocks. The IBM AT specification states the I/O Card must wait two BCLKs after receiving -DACK and driving MASTER low before it can drive the AT bus command strobes.

Bit 5 - This bit is only defined for MicroChannel, AT, or EISA bus operation. It is user defined for NuBus operation. If the hardware engineer needs only 16 bits of data transferred over the MicroChannel, EISA, or AT bus then the upper data word (bits 15–31) is re-defined as an I/O port (register 7). Data bits 16–23 are for output and data bits 24–31 are input. The host or MPU may read or write this port thru register 7.

Bit 6 - This bit is pre-defined for the MicroChannel host bus and is user defined for all other hosts. It indicates additional check status information.

Bit 7 - When this bit is asserted the MicroChannel CHCK signal is active or the AT signal I/O CHCK is active. For NuBus and EISA operation this pin is user defined. The firmware engineer must exercise care when setting this bit and bit 6. A read operation should first be performed to find the value of bits 0–5. The write operation should then rewrite these bits to their original value.

Register 6 (06h) - Configuration 6

This register contains the BIOS PROM address range when the 86C05 is interfaced to the MicroChannel, EISA, or AT bus. The reader should note that after a reset the 86C05 does not respond to a BIOS PROM address until after this register has been written (MicroChannel, EISA, or AT bus only). When the 86C05 is interfaced to the NuBus all bits in this register, except 6 and 7, are user defined. The contents of this register are not affected by a firmware or hard reset.

The address of the NuBus BIOS PROM is FSXFPPPP where S is equal to the slot ID bits 3–0, F is the hexadecimal digit, X is don't care, and P is 64K BIOS PROM space. Each card in the NuBus backplane is hardwired for a unique slot ID from 0h to Fh.

WRITE (host and mpu) / READ (host and mpu)

When this chip interfaces to the MicroChannel, EISA, or AT bus the BIOS PROM starting address and size information is placed in this register. The BIOS PROM normally resides in the 0C0000h to 0DFFFFh address range. When this chip interfaces to the MicroChannel or EISA bus the BIOS PROM address range is written by the host processor during I/O card configuration. When this chip interfaces to the AT bus the BIOS PROM address range is written by the local MPU as soon as possible after power-up. For IBM BIOS PROM selection, address bits 23–13 are specified as shown below:

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13
0	0	0	0	1	1	0	bit4	bit3	bit2	bit1

For 32 bit addresses (MicroChannel and EISA) the hardware engineer should externally decode address bits A31–A24. For MicroChannel operation when the MADE24 bit is deasserted (32 bit address) and for all EISA operation the -HST_MEM pin (result of external decode) must be asserted to enable a BIOS PROM access.

The BIOS PROM address range is specified below:

REGISTER 6 (06h) FUNCTION

```
7 6 5 4 3 2 1 0
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  +---Not Defined
|  |  |  |  |  |  +------BIOS PROM Addr Bit 13
|  |  |  |  |  +---------BIOS PROM Address Bit 14
|  |  |  |  +------------BIOS PROM Address Bit 15
|  |  |  +---------------BIOS PROM Address Bit 16
|  |  +------------------Not Defined
|  |
0  0 ---------------------- 8K BIOS PROM Size
0  1 ---------------------- 16K BIOS PROM Size
1  0 ---------------------- 32K BIOS PROM Size
1  1 ---------------------- 64K BIOS PROM Size
```

The reader should note that the BIOS PROM starting address must be on a memory boundary equal to the size of the BIOS PROM. For example, a 32K PROM must start on a 32K memory address (i.e. bits 1 and 2 must equal zero).

Register 7 (07h) - I/O Port

This I/O port is always available when the 86C05 is connected to the NuBus. For MicroChannel, EISA, or A bus operation, this port is available only if register 5, bit 5 is asserted. A write to this register sends the data to eight output pins. A read of this register provides eight unlatched bits of data from the input pins (see register 5 for more information). This port is not affected by firmware or hard reset.

Register 8, 9 and 10 (08h, 09h and 0Ah) - I/O Command

These registers can be written or read by both the host processor and the local MPU. In a typical operation the host processor would write a command (with bit 7 asserted) to one of these registers. The local MPU would receive an interrupt and read the command. It would then execute the command, write status information to this register, clear bit 7 in this register, and generate a unique host interrupt for this port. Bit 7 is asserted when the 86C05 is hard reset (a hard reset occurs when the host interface reset pin is asserted) or a firmware reset occurs (a firmware reset takes place when bit 2 of register 4 is asserted). Bits 0–6 are not affected by a firmware or hard reset.

WRITE (host and mpu) / READ (host and mpu)

REGISTER 8, 9, or 10 FUNCTION
(08h, 09h, 0Ah)

```
7 6 5 4 3 2 1 0
| | | | | | | |
| | | | | | | +---User Defined
| | | | | | + ------User Defined
| | | | | +----------User Defined
| | | | + ------------User Defined
| | | +----------------User Defined
| | +--------------------User Defined
| + ----------------------User Defined
+--------------------------Busy
```

Bits 0–6 - User Defined

Bit 7 - This bit is asserted by a hard reset or a write from the host or MPU interface. For example, the host would assert this bit when it issues a new command to the 86C05. When this bit is asserted an interrupt (if not masked) is generated to the local MPU.

Register 11, 12, 13 (0Bh, 0Ch, 0Dh) - I/O Data

WRITE (host) / READ (mpu)

These registers are used to communicate information from the host to the MPU. They could, for example, hold a 24 bit address that points to a host mailbox structure. If the 86C05 is operating as three separate virtual ports these registers could contain unique information about each port. These registers are not affected by a firmware or hard reset.

Register 15 (0Fh) - System Control / System Status

Bits 0–5 of this control register are cleared by a firmware or hard reset.

WRITE (mpu)

REGISTER 15 (0Fh) FUNCTION

```
7 6 5 4 3 2 1 0
| | | | | | | |
| | | | | 0 0 0---Test and Set Bit 0
| | | | | 0 0 1---Test and Set Bit 1
| | | | | 0 1 0---Test and Set Bit 2
| | | | | 0 1 1---Test and Set Bit 3
| | | | | 1 0 0---Test and Set Bit 4
| | | | | 1 0 1---Test and Set Bit 5
| | | | | 1 1 0---Test and Set Bit 6
| | | | | 1 1 1---Test and Set Bit 7
| | | | |
| | | | + ------------Halt State Machines
| | | + ----------------Hard Abort
| | +--------------------Diagnostic Bit
| + ----------------------Simulate Power On Reset
+--------------------------Reset Power on Flag
```

Bits 0–2 - Specifies which bit to test when the Set Semaphore command is executed.

Bit 3 - When this bit is asserted the currently executing command is halted. This bit is normally set by the firmware engineer prior to setting the hard abort bit (bit 4). It forces the chip to release the host bus, halt DMA activity, etc. Asserting this bit terminates the execution of most commands.

Bit 4 - When this bit is asserted the currently executing command is hard aborted.

Bit 5 - This bit allows the MPU to read internal nodes in the 86C05.

Bit 6 - When this bit is asserted its simulates a power-up condition. The power on flag is set and the chip is hard reset.

Bit 7 - Asserting this unlatched bit clears the power on flag (register 15, bit 7)

READ (mpu)

REGISTER 15 (0Fh) FUNCTION

```
7 6 5 4 3 2 1 0
| | | | | | | |
| | | | | | | +---MPU Data Ready
| | | | | | + ------Transfer Counter = 0
| | | | | +----------FIFO Empty
| | | | + ------------FIFO Full
| | | + ----------------Host Operation Done
| | +--------------------DMA Operation Done
| + ----------------------MPU Operation Done
+ --------------------------Power On Flag
```

Bit 0 - When the MPU is transferring data to/from the 86C05 (register 31) this bit indicates the chip is ready to accept more data.

Bit 1 - When this bit is asserted the transfer counter is equal to pseudo zero. The transfer counter may in fact be non-zero but for the transfer size there are zero bytes left to transfer. For example, if performing a 32 bit transfer (four bytes) from the host to the DMA interface and the transfer counter equals 3 (bytes) then this bit is set. The 86C05 can not read anymore data from the host (32 bits at a time) until the firmware changes the transfer size and re-issues the command.

Bit 2 - When asserted the FIFO is pseudo empty.

Bit 3 - When asserted the FIFO is pseudo full.

Bits 4–6 - These bits indicate the corresponding interface has completed its task. For example, when transferring data from the host to the MPU and the transfer counter equals pseudo zero and the 86C05 chip has released the bus, then bit 4 is asserted. These bits are valid only when the corresponding port is transferring data into the 86C05.

Bit 7 - When this bit is asserted a power-on condition is present. This bit can be reset by writing a one to bit 7 of register 15.

Register 16 (10h) - System Configuration

This register is cleared by a hard reset and is not affected by a firmware reset.

WRITE (mpu)

REGISTER 16 (10h) FUNCTION

```
7 6 5 4 3 2 1 0
| | | | | | | |
| | | | | | | +---Polarity MINT pin
| | | | | | + ------Enable FIFO_RDY pin
| | | | | |
| | | | 0 0----------Disable DMA Parity
| | | | 0 1----------Enable DMA Odd Parity
| | | | 1 0----------DMA -RD/-WRT Strobes
| | | | 1 1----------Enable DMA Even Parity
| | | |
| | | + ----------------Upper byte DMA path
| | +--------------------FIFO or /Xfer
| + ----------------------Don't Reset FIFO
+ --------------------------Disable Reset_Out pin
```

Bit 0 - This bit indicates the polarity of the interrupt pin. When this bit is a one the interrupt pin is high true polarity. When this bit is a zero the interrupt pin is low true polarity.

Bit 1 - When this bit is asserted the MPU FIFO_RDY pin is enabled. The FIFO_RDY pin normally connects to a DMA controller on the MPU bus. This allows the firmware engineer to transfer data between MPU memory and the 86C05 under DMA control. Alternately, the firmware engineer may poll bit 0 of register 15 before transferring data between the 86C05 FIFO and local MPU memory.

Bits 2–3 - These bits control the function of the parity bits as outlined above.

Bit 4 - When this bit is asserted and an 8 bit DMA transfer is requested (via register 22) then the 8 bit transfer is performed on the upper data byte.

Bit 5 - This bit affects the definition of registers 24 through 30 as outlined below:

	Reg 24–26	Reg 27–30
Bit 5 = 0	Xfer Counter	Xfer Address
Bit 5 = 1	FIFO Counter	FIFO Address

Bit 6 - When a new 86C05 command is issued the FIFO is reset and data contained within the FIFO is lost. If this bit is asserted the 86C05 does not reset the FIFO when a new command is issued and therefore any data contained in the FIFO is processed. This bit is usually only set for error recovery.

Bit 7 - When asserted the reset out pin can not go low true. This signal is used during a firmware reset to prevent the MPU from being reset.

Register 17 (11h) - Host Control 0 / Host Status 0

This control register is cleared by a firmware or hard reset.

WRITE (mpu)

REGISTER 17 (11h) FUNCTION

```
 7 6 5 4 3 2 1 0
 |  |  |  |  |  |  |  |
 |  |  |  |  |  |  |  +---Block Xfer Mode (NB)
 |  |  |  |  |  |  +------I/O / Memory Space
                            (MC, EISA, AT)
 |  |  |  |  |  +----------Enable Resource Lock
                            (NB, EISA)
 |  |  |  |  +-------------Ignore Access Error
                            (MC, EISA, NB)
 |  |  |  +----------------32 bit Host Address (MC, AT)
 |  |  +-------------------Six Clks between Strobes
                            (MC, AT)
 |  +----------------------Don't Inc Host Address
 +-------------------------Stay on Host bus till FIFO
                            full/empty
```

Bit 0 - When this bit is asserted the 86C05 uses block mode to transfer data to/from NuBus memory. The NuBus memory at the address specified must support block mode. When this bit is deasserted only one transfer is performed per NuBus transaction.

Bit 1 - This bit is only valid for MC, EISA, or AT since all transfers on the NuBus are into memory space. When this bit is asserted the data is transferred to/from host I/O space. This bit allows the 86C05 to transfer data directly to/from an I/O card without using system memory.

Bit 2 - When this bit is asserted the 86C05 performs a resource lock on the NuBus or locks the EISA bus during the requested transfer.

Bit 3 - When this bit is asserted the 86C05 does not halt the currently executing command when an access error occurs. The access error is still reporteD. An access error occurs when the I/O CHCK signal is asserted. In addition, for MicroChannel operation an access error is reported if the accessed slave does not assert the -SD SFDBK signal.

Bit 4 - When asserted a 32 bit MicroChannel or AT address is requested. The hardware engineer must connect the HOST_OWN pin to the output enable of a byte wide MSI driver. This driver gates the address bits 24–31 onto the host bus. All NuBus and EISA bus transfers use a 32 bit address. The reader should note that the AT bus (ISA-16) is only defined for 24 address bits.

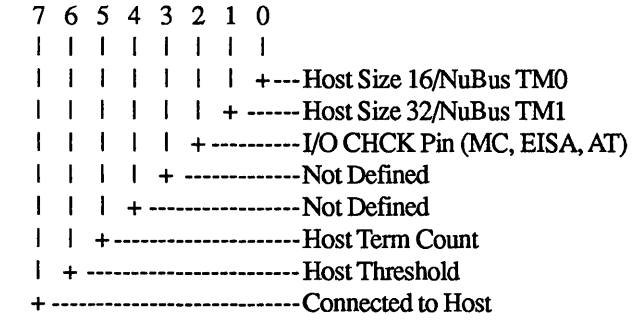
Bit 5 - For MicroChannel and AT operation the 86C05 normally inserts four clocks between the trailing edge of the command strobe and the leading edge of the next command strobe. When this bit is asserted the 86C05 inserts 6 clocks.

Bit 6 - When this bit is asserted the 86C05 performs continuous access to the same host address.

Bit 7 - The 86C05 arbitrated for the host bus access once the FIFO count specified in register 19 has been met. It then transfers the count in register 19 to/from the host and releases the host bus. When this bit is set the 86C05 stays on the bus and transfers data to/from the host until the FIFO is empty/full or the 86C05 is forced off the bus by a higher priority

device (no higher priority device for NuBus interface). READ (mpu)

REGISTER 17 (11h) FUNCTION



Bits 0–1 - These bits are valid after a host access has completed. They indicate the host memory size (MicroChannel, EISA, or AT) or access error (NuBus):

BitBit 1 0	NuBus Function	MC, EISA, or AT Function
0 0	Try Again Later	8 Bit Memory
0 1	Bus Timeout Error	16 Bit Memory
1 0	Error	32 Bit Memory
1 1	Normal Completion	32 Bit Memory

Bit 2 - This unlatched pin provides the firmware engineer with the status of the I/O CHCK pin.

Bit 3 - Not Defined

Bit 4 - Not Defined

Bit 5 - When asserted the 86C05 chip must load the host transfer counter with the count in the FIFO (host write operations) or transfer counter (host read operations). This bit is asserted for the last host transfer before a command completes. This bit is for diagnostic purposes only.

Bit 6 - This bit indicates the FIFO is ready for another block of data. This bit is for diagnostics purposes only.

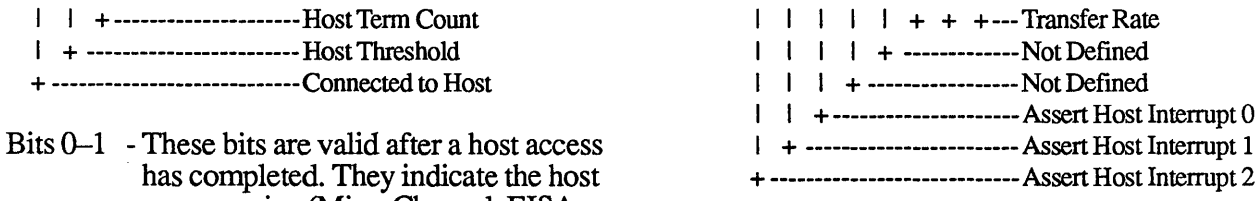
Bit 7 - When this bit is asserted the 86C05 is connected (bus master) to the host bus.

Register 18 (12h) - Host Control 1 / Host Status 1

This control register is cleared by a firmware or hard reset.

WRITE (mpu)

REGISTER 18 (12h) FUNCTION



Bits 0–2 - Regardless of the number of additional clocks inserted into the bus access the 86C05 does not terminate the MicroChannel, EISA, or AT bus cycle until the I/O Channel Ready signal is active. These bits are not defined for NuBus and EISA bus operation.

For MicroChannel operation these bits indicate the number of additional clock (ac) periods to add to the -CMD strobe.

For AT bus operation these bits select a transfer rate. Additional clock periods are added to the access strobes as outlined below (assuming 40 MHz clock input / 2 = 50 ns per additional clock added):

Bits 210	Strobe Pulse Width / ac (ns)	32 Bit Transfer Rate (Mbytes/sec)
000	100 / 0	20
001	150 / 1	16
010	200 / 2	13.4
011	250 / 3	11.4
100	300 / 4	10
101	350 / 5	8.9
110	400 / 6	8.0
111	450 / 7	7.3

Bits 3–4 - Not Defined

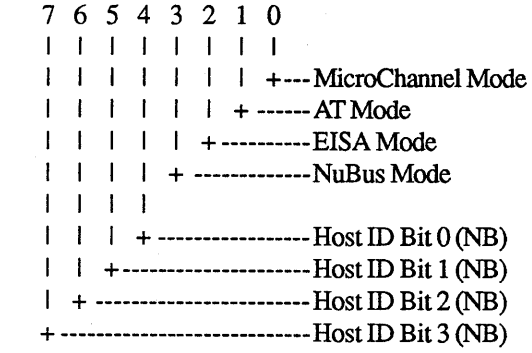
Bits 5–7 - Asserting these unlatched bits produce a host interrupt as shown above. The

interrupt is cleared when the host or MPU writes to the I/O register indicated below:

Interrupt	I/O Register
0	Register 8
1	Register 9
2	Register 10

READ (mpu)

REGISTER 18 (12h) FUNCTION



Bits 0–3 - The host interface of the 86C05 chip is configured (CONFIG2 and CONFIG3 pins) to operate in one of the modes indicated by these bits.

Bits 4–7 - These bits indicate the slot ID for the NuBus.

Register 19 (13h) - Host Blk Count / Revision Number

The Host Block Count register is cleared by a firmware or hard reset.

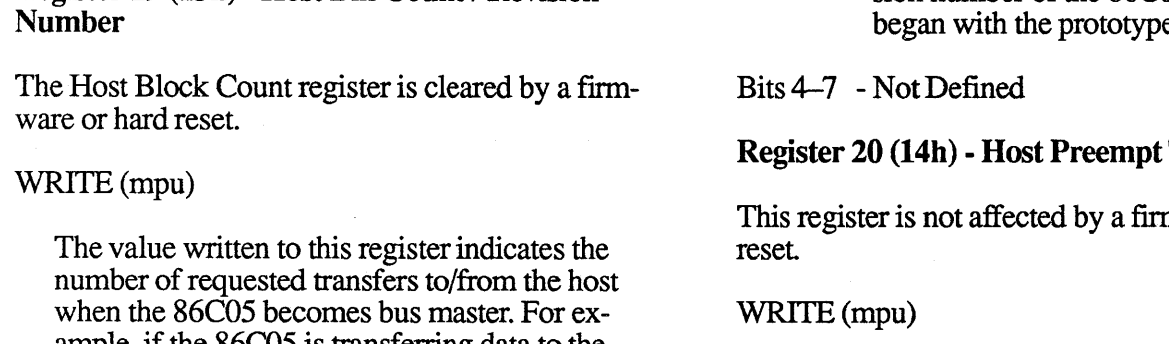
WRITE (mpu)

The value written to this register indicates the number of requested transfers to/from the host when the 86C05 becomes bus master. For example, if the 86C05 is transferring data to the host and 32 bit transfers are enabled and these bits equal 1 (see below), then the 86C05 waits until the FIFO contains at least eight bytes before arbitrating for host bus access. Once bus ownership is obtained the 86C05 attempts to transfer the block count specified in this register before releasing the bus. The transfer terminates early if the 86C05 loses bus priority or is on the bus for too long (register 20). If bit 7 of Register 17 is asserted the 86C05 attempts to stay on the bus until the FIFO is empty/full. For NuBus transfers in block mode, the value in this register must correspond to 2, 4, 8, or 16. The value placed in bits 0, 1, and 2 of this register indicates the block count as shown below:

Bits 2 1 0	Number of Host Transfers
0 0 0	1
0 0 1	2
0 1 0	4
0 1 1	8
1 0 0	16
1 0 1	32
1 1 0	64
1 1 1	64

READ (mpu)

REGISTER 19 (13h) FUNCTION



Bits 0–3 - This number represents the current revision number of the 86C05. The count began with the prototype chip at zero.

Bits 4–7 - Not Defined

Register 20 (14h) - Host Preempt Time

This register is not affected by a firmware or hard reset.

WRITE (mpu)

The value written to this register is the number of clock cycles divided by 4 that the 86C05 can stay on the bus after a bus release condition is present. This register is not used for NuBus operation.

The bus release condition varies for each host bus supported as shown below:
1. MicroChannel - assertion of the -PREMPT signal

2. EISA - deassertion of the -MACKx signal
3. AT - bus release timeout starts immediately after bus ownership begins.

Register 21 (15h) - DMA Control

Bits 0–6 of the DMA Control register are cleared by a firmware or hard reset.

WRITE (mpu)

```
REGISTER 21 (15h)   FUNCTION
  7 6 5 4 3 2 1 0
  |   |   |   |   |   |   |
  |   |   |   |   | 0 0 0---2 clocks DMA REQ pin width
  |   |   |   |   | 0 0 1---3 clocks DMA REQ pin width
  |   |   |   |   | 0 1 0---4 clocks DMA REQ pin width
  |   |   |   |   | 0 1 1---5 clocks DMA REQ pin width
  |   |   |   |   | 1 0 0---6 clocks DMA REQ pin width
  |   |   |   |   | 1 0 1---7 clocks DMA REQ pin width
  |   |   |   |   | 1 1 0---8 clocks DMA REQ pin width
  |   |   |   |   | 1 1 1---9 clocks DMA REQ pin width
  |   |   |   |   |
  |   |   |   | + ------------ DMA /Device or Controller
  |   |   | + ----------------Level or /Edge (DMA Device)
  |   |   |                   ACK Hold Off
  |   |   |                   (DMA Controller)
  |   | + ---------------------DMA REQ high true
  | + -----------------------DMA ACK high true
+ -------------------------Toggle DMA REQ
```

Bits 0–2 - These bits specify the width of the DMA ACK signal when operating as a DMA controller. The 86C05 waits until the DMA REQ signal is asserted and there is data to transfer to/from the FIFO. It then asserts the DMA ACK signal the number of clock pulses specified by these bits.

When the 86C05 is operating as a DMA device, it drives the DMA REQ signal and transfers data when the DMA ACK signal is received. Under this condition, these bits are not used.

Bit 3 - This bit specifies whether the 86C05 is operating as a DMA controller or DMA device. When this bit is asserted DMA controller mode is enabled. See discussion of bits 0–2.

Bit 4 - When the 86C05 DMA interface is operating as a DMA device, this bit specifies whether the DMA REQ pin is level or leading edge asserted. When this bit is asserted edge mode is enabled.

When the 86C05 DMA interface is operating as a DMA controller, this bit specifies a hold off period. That is, after the 86C05 asserts then deasserts DMA ACK it does not re-assert DMA ACK until the time specified by bits 0–2 has passed.

Bit 5 - When this bit is asserted it indicates the 86C05 is operating with a high true DMA REQ signal.

Bit 6 - When this bit is asserted it indicates the 86C05 is operating with a high true DMA ACK signal.

Bit 7 - When this unlatched bit is asserted the DMA REQ signal is toggled. This bit is required to "un-hang" edge asserted DMA controllers.

Register 22 (16h) - Transfer Command / Extended Status

This register is cleared by a firmware or hard reset.

WRITE (mpu)

```
REGISTER 22 (16h)   FUNCTION
  7 6 5 4 3 2 1 0
  |   |   |   |   |   |   |
  |   |   |   |   | 0 0 0---Transfer Host -> DMA
  |   |   |   |   | 0 0 1---Transfer DMA -> Host
  |   |   |   |   | 0 1 0---Transfer HOST -> MPU
  |   |   |   |   | 0 1 1---Transfer MPU -> HOST
  |   |   |   |   | 1 0 0---Transfer DMA -> MPU
  |   |   |   |   | 1 0 1---Transfer MPU -> DMA
  |   |   |   |   | 1 1 0---Set Semaphore
  |   |   |   |   | 1 1 1---No Operation
  |   |   |   |   |
  |   |   |   | 0 0---------- Transfer 8 bit host data
  |   |   |   | 0 1---------- Transfer 8 bit host data
  |   |   |   | 1 0---------- Transfer 16 bit host data
  |   |   |   | 1 1---------- Transfer 32 bit host data
  |   |   |   |
  |   | 0 0---------------------Transfer 8 bit DMA data
  |   | 0 1---------------------Transfer 8 bit DMA data
  |   | 1 0---------------------Transfer 16 bit DMA data
  |   | 1 1---------------------Transfer 16 bit DMA data
  |
+ --------------------------16 bit MPU data
```

Bits 0–2 - When these bits are written the command indicated above begins execution. The firmware engineer must initialize all other registers (transfer count, etc.) before issuing a command to this register. The firmware engineer can poll (register 23) for command complete or receive an interrupt.

The Set Semaphore Command executes on the host bus and performs a read modify write operation. This command first locks host memory, reads a byte from host memory, transfers the byte into the FIFO, sets the indicated bit, writes the byte back to host memory, and unlocks host memory. Once the command has completed the local MPU should read the semaphore (register 31) to determine if it now owns the resource. A bit value of zero indicates the resource is ours. A bit value of one indicates the resource is owned by another processor.

Bits 3–4 - These bits indicate the size of the host transfer. For MicroChannel or AT operation the 86C05 senses the slave device memory width and performs smaller size transfers if required. For example, if these bits request the 86C05 to perform a 32 bit transfer but the memory width is only 16 bits, then the 86C05 performs two 16 bit transfers over host data bus bits 0–15.

For EISA bus operation the 86C05 allows the system board to perform the size translations.

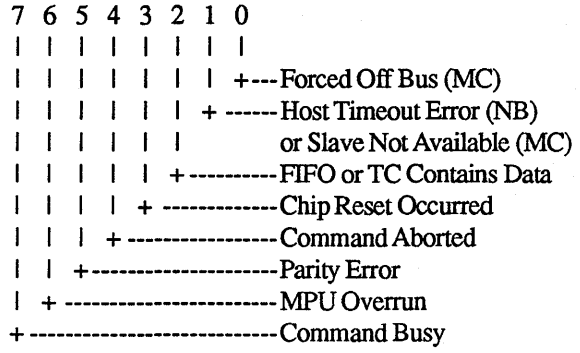
Bits 5–6 - These bits indicate the width of the DMA interface data path.

Bit 7 - When this bit is asserted 16 bits of data is transferred when register 31 (MPU Buffer Data) is accessed. This bit should only be asserted if the hardware engineer has connected the upper byte DD1(0–7) of the DMA interface to the MPU bus

READ (mpu)

This register provides extended status for the firmware engineer. When any error bit (bits 0–6) in this register is asserted, bit 1 (extended status) of register 23 is also asserted.

REGISTER 22 (16h) FUNCTION



Bit 0 - If the 86C05 stays on the MicroChannel longer then 7.5 usec after -PREMPT is asserted it could be forced off by the central arbitration unit, when this occurs this status bit is asserted and the command is aborted.

Bit 1 - If the accessed NuBus memory card does not respond within the 255 clock timeout period this bit is asserted.

When memory or I/O space is accessed on the MicroChannel a signal is returned to indicate if a card is present. When this signal is not returned this bit is set and the data transfer terminated (see register 17,bit 2).

Bit 2 - If the FIFO contains data or the transfer counter is not equal to pseudo zero when a command completes, this bit is set.

Bit 3 - When a chip reset occurs this bit is asserted.

Bit 4 - When the firmware engineer performs a hard abort or halts command execution, this status bit is asserted.

Bit 5 - When this bit is asserted a parity error was detected on data received over the DMA interface.

Bit 6 - This bit indicates an over/underrun condition occurred while transferring data between the 86C05 and the local MPU. The 86C05 needs 12 clocks from the trailing edge of an access to the MPU

Data Buffer (register 31) to the leading edge of the next access. The overrun condition can be avoided by polling register 15, bit 0 before transferring data to/from register 31 or by connecting the FIFO RDY pin to a DMA controller on the MPU bus.

Bit 7 - This bit is asserted while a 86C05 command is executing. The firmware engineer may poll this bit for a command complete condition.

Register 23 (17h) - Interrupt Mask / Status

WRITE (mpu)

When the mask bit in this register is asserted and the corresponding bit is a one for the interrupting condition (listed below) the 86C05 generates an interrupt to the local MPU. This register is cleared by a firmware or hard reset.

READ (mpu)

REGISTER 23 (17h) FUNCTION

```
7 6 5 4 3 2 1 0
| | | | | | | |
| | | | | | | +---86C05 Cmd Completed
| | | | | | +-------86C05 Extended Status
| | | | | +---------Bit 7 of Register 8 asserted
| | | | +-----------Bit 7 of Register 9 asserted
| | | +-------------Bit 7 of Register 10 asserted
| | +-----------------Host Interrupt 0 asserted
| +-------------------Host Interrupt 1 asserted
+-----------------------Host Interrupt 2 asserted
```

Bit 0 - This latched bit indicates the command specified in the Data Flow Control Register (22) completed. Bit 0 is cleared when this register is read.

Bit 1 - If the command specified in the Data Flow Control Register (22) completed with an error, this bit is asserted. Bit 1 is cleared when this register is read. The firmware engineer should note that this bit may be set before the transfer command completes, therefore this bit should not be used to indicate command done status.

Bits 2–4 - When the host issues a command to this chip it should assert bit 7 of register 8, 9, or 10. This asserts the indicated bit in this register. These bits are not latched by this register.

Bits 5–7 - These bits indicate the condition of the three host interrupt pins. The 86C05 has the capability to drive or receive these lines. These bits are not latched.

Register 24, 25, 26 (18h, 19h, 1Ah) - Transfer or FIFO Counter

The 24 bit Transfer Counter is not affected by a firmware or hard reset. The FIFO Up/Down Counter, Host Transfer Counter, and Partial Host Transfer Counter are cleared by a firmware or hard reset.

WRITE (mpu) / READ (mpu)

When register 16 bit 5 is zero, these registers contain the 24 bit data transfer count as shown below:

Register 24 (18h) - Low Byte
Register 25 (19h) - Middle Byte
Register 26 (1Ah) - High Byte

During data transfers this register is decremented on writes to the FIFO. It is used to control the requests for more data into the FIFO. When determining the number of bytes that have been transferred the firmware engineer should consider the transfer counter, and the FIFO counter (contents of register 24 when register 16, bit 5 is one). If the contents of these registers are read during a data transfer they must be debounced.

When register 16 bit 5 is a one, these registers are defined as shown below:

Register 24 (18h) - FIFO Transfer Counter, 8 bits (bit 7 forces FIFO full condition)
Register 25 (19h) - Current Host Transfer Counter, 7 bits
Register 26 (1Ah) - Partial Host Transfer Counter, 2 bits

A write to one of these registers sets the count to any value and a read shows the current contents.

Register 27, 28, 29, 30 (1Bh, 1Ch, 1Dh, 1Eh) - Host Address or FIFO Address

The Host Address register is not affected by a firmware or hard reset. The FIFO Address register is cleared by a firmware or hard reset.

WRITE (mpu) / READ (mpu)

When register 16 bit 5 is a zero, these registers contain the host bus address as shown below:

Register 27 (1Bh) - Bits 0–7
Register 28 (1Ch) - Bits 8–15
Register 29 (1Dh) - Bits 16–23
Register 30 (1Eh) - Bits 24–31 (NB) or Current Preempt Count (MC,EISA,AT)

The address placed in this register is incremented by 0, 1, 2, or 4 after each host bus access. The firmware engineer may read (and debounce) these registers to monitor the progress of the data transfer. The contents of these registers are also useful for error recovery. Register 30 is the upper address byte for NuBus and it is the preempt counter for the MicroChannel, EISA, or AT bus.

When register 16 bit 5 is a one, these registers contain the FIFO In and FIFO Out Transfer Address as shown below:

Register 27 (1Bh) - FIFO In Address, 7 bits
Register 28 (1Ch) - FIFO Out Address, 7 bits

The firmware engineer may read these registers as an aid to error recovery or set their contents for diagnostic or error recovery purposes.

Register 31 (1Fh) - MPU Data Buffer

WRITE (mpu) / READ (mpu)

When data is transferred between the MPU and the FIFO, this register provides a buffer for the data. The MPU should read or write to this register when the FIFO RDY pin is asserted or status bit 0 of register 15 is asserted. This register is not affected by a firmware or hard reset.

Chapter 2
86C05 Pin Definitions

The 86C05 supports four host interfaces; MicroChannel, AT, EISA, and NuBus. The following table defines the pin names and shows the pin cross reference between the four host interfaces:

Table 9. Host Interface - Pin Definition and Cross Reference

MicroChannel Signals	AT Bus Signals	EISA Signals	NuBus Signals
A(0–1)	SA(0–1)	SA(0–1)	NA(0–1)
A(2–17)	SA(2–17)	LA(2–17)	NA(2–17)
A(18–19)	SA(18–19)	LA(18–19)	PO(0–1)
A(20–23)	LA(20–23)	LA(20–23)	PO(2–5)
D(0–31)	SD(0–31)	SD(0–31)	AD(0–31)
ADL	BALE	VDD	-START
DS16RTN	-IOCS16	VDD	-PI(5)
SBHE	-SBHE	no connect	PO(6)
MADE24	MADE24	-LOCK	-ACK
M_-I/O	-SWEN	M-IO	-PO(7)
S1	-IOWR	W-R	-TM1
S0	-IORD	-START	-TM0
CMD	-MEMW	-CMD	SLOT
CDSFBKI	LA17	no connect	PI(0)
CDSFBKO	AEN	AENx	PI(1)
CHRDYRTN	-IOCS32	-EX32	PI(2)
ARB_IN(0)	-DACK(0)	-MACKx	-ARB_IN(0)
ARB_IN(1–2)	-DACK(1–2)	VDD	-ARB_IN(1–2)
ARB_IN(3)	VDD	-EX16	-ARB_IN(3)
ARB_OUT(0)	DRQ(0)	-MREQx	-ARB_OUT(0)
ARB_OUT(1–2)	DRQ(1–2)	no connect	-ARB_OUT(1–2)
ARB_OUT(3)	LA19	no connect	-ARB_OUT(3)
BURST	IOCHRDY	-EXRDY	SSLOT
PREEMPT	-MASTER	no connect	-RQST
ARB/-GNT	-MEMR	no connect	PI(3)
IRQ(0–2)	-IRQ(0–2)	-IRQ(0–2)	-NMRQ(0–2)
CDSETUP	-MEMCS16	VDD	PI(6)
CHCK	-I/O CHCK	-I/O CHCK	PI(4)
CHRESET	RESET DRV	RESET DRV	-RESET
BE(0–2)	VDD	-BE(0–2)	-ID(0–2)
BE3	VDD	-BE(3)	-ID3
DS32RTN	-MEMCS32	BCLK	-CLK
TR32	LA18	-BEOE	PI(7)
HAOE	-HAOE	-HAOE	no connect
HADIR	HADIR	HADIR	RSLOCK
HDOE(0–2)	-HDOE(0–2)	-HDOE(0–2)	-HDOE(0–2)
HDDIR	HDDIR	HDDIR	HDDIR
HOST_OWN	-HOST_OWN	-HOST_OWN	-HOST_OWN
HST_MEM	-HST_MEM	-HST_MEM	-HST_MEM
PROMOE	-PROMOE	-PROMOE	-PROMOE

These host interface pins are common to all four host buses supported by the 86C05 chip. There are 7 common pins. The following abbreviations are used:

I/O = Input and Output Pin
I = Input Pin Only
O = Output Pin Only
TS = Tri-state Pin
OC = Open Collector Pin
TP = Totem Pole Pin

Table 10. Host Interface—Common Pin Summary

Pin(s) Name	Number of Signals	Input/ Output	Pin Type	Pin Drive(ma)
HADIR	1	O	TP	8
HAOE	1	O	TP	8
HDDIR	1	O	TP	8
HDOE(0–2)	1	O	TP	8
HOST_OWN	1	O	TP	8
HST_MEM	1	I	–	–
PROMOE	1	O	TP	8

Table 11. Host Interface—Common

Symbol	Signal Name	I/O	Pin Number	Function
HADIR	Host Address Direction	O	46	This totem pole output signal connects to the DIR pin of the LS245s which gate the address bits to the MicroChannel, EISA, or AT bus. When this pin is low the host address bus is gated to the 86C05 chip. When this pin is high the address bus from the 86C05 is gated to the host address bus. For NuBus operation this pin indicates a Resource Lock condition.
HAOE	Host Address Output Enable	O	47	This active low totem pole output signal connects to the -OE pin of the LS245s which gate the address bus between the 86C05 and the MicroChannel, EISA, or AT bus. This pin is not defined for NuBus operation.

Table 11. Host Interface—Common (continued)

Symbol	Signal Name	I/O	Pin Number	Function
HDDIR	Host Data Direction	O	19	This totem pole output signal connects to the DIR pin of the LS245s which gate the data bus between the 86C05 chip and the Micro-Channel, EISA or AT bus. When this pin is low the host data bus is gated to the 86C05 chip. When this pin is high the data bus from the 86C05 chip is gated to the host data bus. For NuBus operation, this pin connects to the DIR pin of the ALS640s which gate the multi-plexed address/data bus between the 86C05 chip and the NuBus. When this pin is low the NuBus address/data bus is gated to the 86C05 chip. When this pin is high the address/data bus from the 86C05 chip is gated to the host data bus.
HDOE(2) HDOE(1) HDOE(0)	Host Data Output Enable	O	16 17 18	These active low totem poleoutput signals connects tothe -OE pin of the LS245s (Micro-Channel, EISA, or AT) or ALS640s (NuBus) which gate data between the 86C05 and the host bus. These signals pin out as indicated below: Host byte / -HDOE pin 0 / -HDOE(0) 1 / -HDOE(1) 2 / -HDOE(2) 3 / -HDOE(2)
HOST_OWN	Host Own	O	15	When this active low totem pole signal is asserted, the 86C05 is the owner of the host bus. This signal is also discussed under each individual host bus.
HST_MEM	Host Memory Enable	I	80	This active low input signal is used to qualify BIOS PROM access as outlined below a. For AT bus this signal would normally be tied to ground.

Table 11. Host Interface—Common (continued)

Symbol	Signal Name	I/O	Pin Number	Function
				b. For MicroChannel and EISA bus (both support a 32 bit host address), this pin would typically connect to an address comparator for host address bits 24–31. The 86C05 chip compares address bits 13–23. For MicroChannel operation, if the MADE24 pin is high then an active level on this pin is not required. c. The 86C05 chip does not decode address bits 20–23 for the NuBus. This pin could decode these bits.
PROMOE	BIOS PROM Output Enable	O	68	This totem pole active low output signal connects to the -OE pin of a BIOS PROM. When this signal is asserted the 86C05 has detected a BIOS PROM access. The 86C05 also enables the host bus transceiver (byte 0) to gate the BIOS PROM data to the host bus.

The 86C05 MicroChannel Interface consists of 90 signals as outlined below. The 86C05 is configured to operate in the MicroChannel interface mode when CONFIG2 is low and CONFIG3 is high. The following abbreviations are used:

I/O = Input and Output Pin
I = Input Pin Only
O = Output Pin Only
TS = Tri-state Pin
OC = Open Collector Pin
TP = Totem Pole Pin

Table 12. Host Interface—MicroChannel Bus Pin Summary

Pin(s) Name	Number of Signals	Input/ Output	Pin Type	Pin Drive(ma)
A(0–23)	24	I/O	TS	4
ADL	1	I/O	TS	24
ARB_IN(0–3)	4	I	–	–
ARB_OUT(0–3)	4	O	TP	4
ARB/-GNT	1	I	–	–
BE(0–3)	4	O	TP	4
BURST	1	I/O	OC	24

Table 12. Host Interface—MicroChannel Bus Pin Summary (continued)

Pin(s) Name	Number of Signals	Input/ Output	Pin Type	Pin Drive(ma)
CDSETUP	1	I	–	–
CDSFBKI	1	I	–	–
CDSFBKO	1	O	TP	8
CHCK	1	I/O	OC	24
CHRDYRTN	1	I	–	–
CHRESET	1	I	–	–
CMD	1	I/O	TS	24
D(0–31)	32	I/O	TS	4
DS16RTN	1	I	–	–
DS32RTN	1	I	–	–
IRQ(0–2)	3	I/O	OC	4
MADE24	1	I/O	TS	24
M_I/O	1	I/O	TS	24
PREEMPT	1	I/O	OC	24
SBHE	1	O	TS	24
S1	1	I/O	TS	24
S0	1	I/O	TS	24
TR32	1	O	TP	4

Table 13. Host Interface—MicroChannel Bus

Symbol	Signal Name	I/O	Pin Number	Function
A(0–2) A(3–7) A(8–14) A(14–23)	Address Bits	I/O	48–50 55–59 61–67 71–79	These active high tri-statesignals address memory or I/O devices within the system. They connect to the host bus thru LS245s and provide 24 bits of direct addressing capability. Only the lower 16 bits are decoded for I/O operations. These signals are latched (-ADL) by bus slaves. The user may drive 32 bits of address by connecting the HOST_OWN pin to the -OE pin of a byte wide MSI driver.
ADL	Address Decode Latch	I/O	12	This active low, tri-state signal is used to latch the contents of the address bus. The latch is open when this signal is low. Devices on the MicroChannel must latch the address since pipelining is possible. That is, the address may change for the next MicroChannel cycle before the -CMD strobe for the current cycle has been deasserted. This pin connects directly to the MicroChannel.

Table 13. Host Interface—MicroChannel Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
ARB_IN(3) ARB_IN(2) ARB_IN(1) ARB_IN(0)	Arbitration Bus Priority In	I	143 144 145 146	These active high input pins connect directly to the MicroChannel and receive arbitration bus priority levels.
ARB_OUT(3) ARB_OUT(2) ARB_OUT(1) ARB_OUT(0)	Arbitration Bus Priority Out	O	138 139 141 142	These active high totem pole output signals are used to present arbitrating bus participant priority levels. The highest value of (hex Fh) has the lowest priority and the lowest value (hex 0h) has the highest priority. The priority level of the 86C05 is programmed into register 5. These pins should connect to the Micro-Channel through a 7407 open collector driver.
ARB/-GNT	Arbitrate/ Grant	I	149	This active high input signal indicates an arbitration cycle is in process. When this signal is low it is the grant to the winner to access the channel. This pin connects directly to the MicroChannel.
BE(3) BE(2) BE(1) BE(0)	Byte Enable	O	134 135 136 137	These active low totem poleoutputs are used during 32 bit data transfers to indicate which data bytes to placed on the MicroChannel. These signals should connect to the Micro-Channel thru a LS244 driver. The driver is enabled by the -HOST_OWN pin.
BURST	Burst	I/O	148	This active low open collector signal is driven low by arbitrating bus participants to indicate the extended use of the MicroChannel. The 86C05 asserts this signal for all "master mode" transfers. It deasserts -BURST during the last transfer cycle. This pin connects directly to the MicroChannel.
CDSETUP	Card Setup	I	156	This active low input signal is used to force a chip select. When it is active the host processor may read or write registers 0–7. Register

Table 13. Host Interface—MicroChannel Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
				selection is made via the address bits A0, A1, and A2. This pin connects directly to the MicroChannel.
CDSFBKI	Card Select Feedback In	I	158	This active low input signal is used when the 86C05 is the bus master to indicate a slave is present at the address requested.
CDSFBKO	Card Select Feedback Out	O	157	This active low output signal indicates when the 86C05 is being accessed by the MicroChannel. It is generated from an address decode of the I/O registers or BIOS PROM. When the 86C05 is bus master this signal must be return from all addressed slaves. This pin connects directly to the MicroChannel.
CHCK	Channel Check	I/O	151	This active low open collector signal is used to indicate a serious error. It is asserted when the host processor or local MPU writes a one to bit 7 of register 5. A zero written to this register deasserts this signal. The 86C05 terminates the host bus transfer, with an access error, if this signal is asserted. This pin should connect directly to the MicroChannel.
CHRDYRTN	Channel Ready Return	I	159	This active high input indicates that the slave addressed by the 86C05 needs additional time to complete the requested read or write operation. When the slave needs more time it pulls this signal low. The 86C05 inserts wait states until this signal is high. This pin connects directly to the MicroChannel.
CHRESET	Channel Reset	I	154	This active high input provides a hard reset to the 86C05 chip. Internal logic is initialized by this signal and any transfer operations are aborted.

Table 13. Host Interface—MicroChannel Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
CMD	Command	I/O	28	This active low tri-state signal is used to define when data is valid on the data bus. During write operations, the data must be valid on the bus throughout the period -CMD is low. For read operations, the data must be valid before the trailing edge of -CMD and held on the bus (hold time) until after CMD is high. This pin is connected directly to the MicroChannel.
D(4–0) D(14–5) D(20–15) D(30–21) D(31)	Data Bits	I/O	41–45 31–40 21–26 1–10 160	These are active high, tri-state signals. All data transfers between the MicroChannel and the MPU or DMAinterface flows through these pins. These pins connect to the MicroChannel thru LS245 transceivers. When the 86C05 transfers only 16 bits of data to the host, then D(16–31) maybe programmed (register 5, bit 5) as an I/O port.
DS16RTN	Data Size 16 Return	I	153	This active low signal indicates that the slave device which the 86C05 addressed is providing (driving orreceiving) 16 bits of data. If this signal is not returned from the slave device and the 86C05 is programmed for 16 bit transfers, then the 86C05 performs two 8 bit transfers. This pin connects directly to the Micro-Channel.
DS32RTN	Data Size 32 Return	I	152	This active low input signal is driven low by 32 bit slaves. When the firmware engineer requests the 86C05 to perform 32 bit transfers but the slave only supports 8 or 16 bit transfers, then the 86C05 breaks the transfers into the size supported by the slave. This pin connects directly to the MicroChannel.
HOST_OWN	Host Own	O	15	When this totem pole signal isasserted the 86C05 is the owner of the MicroChannel. If 32 bit addressing is specified (register 17, bit 4) then this signal should connect to the output

Table 13. Host Interface—MicroChannel Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
				enable pin of a bus driver (24 ma) that gates address bits 24–31 onto the MicroChannel. It is also required to drive the -BE(0–3) and TR32 signals onto theMicroChannel.
IRQ(2) IRQ(1) IRQ(0)	Interrupt Request	I/O	129 130 133	These active low open collector signals are used to inform a system or concurrent processor of the completion of a task. The86C05 can also monitor these signals and interrupt the local MPU when one or more lines become active (register 23). The 86C05 drives these lines by setting the corresponding bit in register 18. The system or concurrent processor clears the interrupt by writing to the I/O register indicated below: Interrupt I/O Register IRQ(0) Register 8 IRQ(1) Register 9 IRQ(2) Register 10 External selection logic must be added to the I/O card to provide programmability of these signals. For example, if it is required that under program control the -IRQ(0) signal generate an interrupt on one of the MicroChannel pins IRQ 3–7, then -IRQ(0) must be gated through selector logic. These signals are internally pulled high (400 µa). These pins connect to the MicroChannel thru a 7407 open collector driver.
MADE24	Memory Address Enable 24	I/O	13	This active high tri-state signal indicates when an extended (address bits 24–31) address is used on the MicroChannel. When this signal is low a 32 bit memory address is placed on the bus. When this signal is high a 24 bit address is on the bus. When the firmware engineer requests 32 bit transfers, the additional 8 address bits must be provided external to the 86C05. This pin connects directly to the MicroChannel.

Table 13. Host Interface—MicroChannel Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
M_-IO	Memory or I/O	I/O	132	This tri-state signal distinguishes a memory cycle from an I/O cycle. When this signal is high a memory cycle is in progress. When M_-IO is low an I/O cycle is in progress. This pin connects directly to the MicroChannel.
PREEMPT	Preempt	I/O	29	This active low open collector signal is driven low by arbitrating bus participants to request usage of the channel through arbitration. The requesting arbitration bus participant removes it preempt upon being granted the channel. The 86C05 asserts this signal when the use of the channel is needed and the fairness algorithm (if enabled, through register 5) allows the access. This pin connects directly to the MicroChannel.
SBHE	System Byte High Enable	O	69	This active low tri-state signal enables the transfer of data on byte 1 (bits 8–15) of the data bus. It is used with A0 to distinguish between byte 0 (bits 0–7) and byte 1 (bits 8–15) transfers. This pin connects directly to the MicroChannel.
S0	Status Bit 0	I/O	53	These active low tri-state signals indicate the start of a MicroChannel cycle andalso define the type of cycle when used with the M_-IO signal (see above). When the 86C05 is a channel slave it latchs these bits with the trailing edge of ADL. These pins connect directly to the MicroChannel.
S1	Status Bit 1	I/O	52	

M_-I/O	-S0	-S1	Function
0	0	0	Reserved
0	0	1	I/O Write
0	1	0	I/O Read
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Mem Write
1	1	0	Mem Read
1	1	1	Reserved

Table 13. Host Interface—MicroChannel Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
TR32	Translate	O	155	This active high totem pole output is driven low when the 86C05 is performing 32 bit data transfers. When this signal is low, the 86C05 drives MicroChannel signals -BE(0–3) to gate data between 32 bit slaves and the 86C05. This pin connects to the MicroChannel thru a LS244 driver.

The 86C05 EISA Bus Interface consists of 79 signals as outlined below. The 86C05 is configured to operate in the EISA bus host interface mode when CONFIG2 is high and the CONFIG3 pin is low.
The following abbreviations are used:

I/O = Input and Output Pin
I = Input Pin Only
O = Output Pin Only
TS = Tri-state Pin
OC = Open Collector Pin
TP = Totem Pole Pin

Table 14. Host Interface—EISA Bus Pin Summary

Pin(s) Name	Number of Signals	Input/ Output	Pin Type	Pin Drive(ma)
AENx	1	I	–	–
BCLK	1	I	–	–
BE(0–3)	4	O	TS	4
BEOE	1	O	TS	4
CMD	1	I	–	–
EX16	1	I	–	–
EX32	1	I	–	–
EXRDY	1	I	–	–
HOST_OWN	1	O	TP	8
I/O CHCK	1	I/O	OC	24
IRQ(0–2)	3	I/O	OC	4
LA(2–23)	22	I/O	TS	4
LOCK	1	O	TS	24
MACKx	1	I	–	–
M_IO	1	I/O	TS	24
MREQx	1	O	TS	8
SA(0–1)	2	I	–	–
SD(0–31)	32	I/O	TS	4
START	1	I/O	TS	24
RESET DRV	1	I	–	–
W-R	1	I/O	TS	24

Table 15. Host Interface—EISA Bus

Symbol	Signal Name	I/O	Pin Number	Function
AENx	Address Enable	I	157	This active high, slot specificinput signal indicates (when deasserted) that the 86C05 may respond to address and I/O commands. This pin connects directly to the EISA bus.
BCLK	Bus Clock	I	152	This active high input is provided for synchronizing EISA bus events with the main system clock. BCLK operates at a frequency between 8.333 and 6 MHz with a duty cycle of 50 percent. This pin connects directly to the EISA bus.
BE(3) BE(2) BE(1) BE(0)	Byte Enable	O	134 135 136 137	These active low output totempole signals are the byte enables that identify the specific bytes addressed in a double word. These signals and the address lines, LA(2–23), are pipelined from one cycle to the next. -BE(3) enables the high byte (byte 3) of a double word while -BE(0) enables the low byte. These pins connect to the EISA bus through an LS244 driver. The -OE pin of the LS244 must connect to the -BEOE pin.
BEOE	BE Output Enable	O	155	This active low totem pole output is driven low to enable the -BE(0–3) signals onto the EISA bus when the 86C05 is bus master. The -BE(0–3) signals require a separate output enable pin from the address signals since they must be floated while the system board performs data size translation.
CMD	Command Strobe	I	28	This active low input signal provides timing control within the EISA bus cycle. The system board asserts this signal on the rising edge of BCLK, simultaneous with the deassertion of the -START signal. This pin connects directly to the EISA bus.

Table 15. Host Interface—EISA Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
EX16	16 Bit Slave	I	143	This active low input signal indicates an EISA memory or I/O slave is capable of transferring 16 bit size. During 16 bit bus master transfers the 86C05 samples EX16 on the rising edge of BCLK after -START is asserted. If this signal is not asserted the 86C05 floats the -BE(0–3), START, and SD(0–15) lines to allow the system board to perform a size translation. Once completed the system board asserts this signal and the 86C05 completes the cycle. This pin connects directly to the EISA bus.
EX32	32 Bit Slave	I	159	This active low input signal indicates an EISA memory or I/O slave is capable of transferring 32 bit double word size. During 32 bit bus master transfers the 86C05 samples EX32 on the rising edge of BCLK after -START is asserted. If this signal is not asserted the 86C05 floats the -BE(0–3), START, and SD(0–31) lines to allow the system board to perform a size translation. Once completed the system board asserts this signal and the 86C05 completes the cycle. This pin connects directly to the EISA bus.
EXRDY	EISA Channel Ready Input	I	148	This active high input signal lengthen a bus cycle from its standard one BCLK time. It is asserted by a memory or I/O device when it can not respond quickly enough. When EXRDY is low the 86C05 inserts wait cycles (one BCLK) until the device or memory brings it high. This pin connects directly to the EISA bus.
HOST_OWN	Host Own	O	15	When this totem pole signal is asserted the 86C05 is the current owner of the EISA bus. For the EISA bus this signal should connect to the output enable pin of a bus driver (24 ma) that gates address bits 24–31 onto the EISA bus.

Table 15. Host Interface—EISA Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
I/O CHCK	I/O Channel Check	I/O	151	This active low open collector signal is used to indicatea serious error. It is asserted when the host processor or local MPU writes a one to bit 1 of register 4. A zero written to this register deasserts this signal. The 86C05 terminates the host bus transfer, with an access error, if this signal is asserted. This pin should connect directly to the EISA bus.
IRQ(2) IRQ(1) IRQ(0)	Interrupt Request	I/O	129 130 132	These active low open collector signals are used to inform a system or concurrent processor of the completion of a task. The 86C05 can also monitor these signals and interrupt the local MPU when one or more lines become active (register 23). The 86C05 drives these lines by setting the corresponding bit in register 18. The system or concurrent processor clears the interrupt by writing the I/O register indicated below: Interrupt — I/O Register IRQ0 — Register 8 IRQ1 — Register 9 IRQ2 — Register 10 If the user needs the capability to change interrupt lines than external selection jumpers must be added to the I/O card. For example, 86C05 pin IRQ0 could be jumper selectable to EISA bus interrupts IRQ(3–7). These signals are internally pulled high (400 ua). These pins connect to the EISA bus thru a 74LS04 driver.
LA(2) LA(3–7) LA(8–14) LA(15–19) LA(20–23)	Latchable Address	I/O	50 55–59 61–67 71–75 76–79	These active high tri-statesignals address memory or I/O devices within the system. They form bits 2–23 of theaddress bus. These lines are latched by the 86C05 on the deasserting edge of -START. These pins are onnected to the EISA bus thru an LS245 bus transceiver.
LOCK	Bus Lock	O	13	This active low tri-state output pin is asserted by the 86C05 to guarantee exclusive memory

Table 15. Host Interface—EISA Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
				access during the time -LOCK is asserted. This pin is controlled by bit 2 of register 17. It is always asserted during the Set Semaphore command. This pin connects directly to the EISA bus.
MACKx	Master Acknowledge	I	146	This active low slot specific signal is asserted by the system board to grant access to the EISA bus. This signal is in response to the 86C05 asserting the -MREQx signal. The 86C05 must release the EISA bus within 8 usec after this signal is deasserted. Register 20 must be programmed for this preempt time. This pin connects directly to the EISA bus.
M-IO	Memory	I/O	132	This tri-state signal or I/O distinguishes a memory cycle from an I/O cycle. When this signal is high a memory cycle is in progress. When M-IO is low an I/O cycle is in progress. M-IO is pipelined from oneEISA bus cycle to the next. This pin connects directly to the EISA bus.
MREQx	Master Request	O	142	This active low totem pole, slot specific, output signal is asserted by the 86C05 to request EISA bus access. The system board asserts -MACKx in response to this signal. This pin connects to the EISA bus thru a 7407 open collector driver.
SA(0–1)	System	I	48–49	These active high input signals are the lower two bits of the system address bus. They are latched by the system board on the deasserting edge of BALE. The 86C05 uses these signals for address selection and does not generate the lower two address bits from the -BE(0–3) lines. This simplifies 86C05 decode logic. These pins connect directly to the bus.

Table 15. Host Interface—EISA Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
SD(0–4) SD(5–14) Bits SD(15–20) SD(21–30) SD(31)	Data	I/O	45–41 40–31 26–21 10–1 160	These are active high, tri-state signals. All data transfers between the EISA bus and the MPU or DMA interface flow through these signals. These pins connect to the EISA bus thru LS245 transceivers. When the 86C05 only transfers 16 bits of data to the EISA bus, then D(16–31) maybe programmed (register 5, bit 5) as an I/O port.
START	Start Command	I/O	53	This active low tri-state signal indicates the beginning of an EISA bus access. It is asserted for one BCLK period after the address is valid on the bus. This pin connects directly to the EISA bus.
RESET DRV	Bus Reset	I	154	This active high input signal provides a hard reset to the86C05 chip. Internal logic is initialized by this signal and any transfer operations are aborted.
W-R	Write/ Read	I/O	52	This tri-state pin indicates whether to perform an EISA bus write or read operation. When this pin is high a write operation is requested and when low a read. This pin connects directly to the EISA bus.

The 86C05 AT Bus Interface consists of 86 signals as outlined below. The 86C05 is configured to operate in the AT bus host interface mode when CONFIG2 is high and the CONFIG3 pin is high. The following abbreviations are used:

I/O = Input and Output Pin
I = Input Pin Only
O = Output Pin Only
TS = Tri-state Pin
OC = Open Collector Pin
TP = Totem Pole Pin

Table 16. Host Interface—AT Bus Pin Summary

Pin(s) Name	Number of Signals	Input/ Output	Pin Type	Pin Drive(ma)
AEN	1	I	–	–
BALE	1	I/O	TS	24
DACK(0–2)	3	I	–	–
DRQ(0–2)	3	O	TS	8
HOST_OWN	1	O	TP	8
I/O CHCK	1	I/O	OC	24
IOCHRDY	1	I	–	–
IOCS16	1	I	–	–
IOCS32	1	I	–	–
IOWR	1	I/O	TS	24
IORD	1	I/O	TS	24
IRQ(0–2)	3	I/O	OC	4
LA17	1	O	TS	4
LA18	1	O	TS	4
LA19	1	O	TS	4
LA(20–23)	4	I/O	TS	4
MADE24	1	I/O	TS	24
MASTER	1	O	OC	24
MEMCS16	1	I	–	–
MEMCS32	1	I	–	–
MEMR	1	I/O	TS	24
MEMW	1	I/O	TS	24
SA(0–19)	20	I/O	TS	4
SBHE	1	O	TS	24
SWEN	1	I/O	TS	24
SD(0–31)	32	I/O	TS	4
RESET DRV	1	I	–	–

Table 17. Host Interface—AT Bus

Symbol	Signal Name	I/O	Pin Number	Function
AEN	Address Enable	I	157	This active high, input signal indicates a DMA cycle is in progress. The 86C05 uses the low level of this signal to qualify all AT bus access to the internal registers. This pin connects directly to the AT bus.
BALE	Address Latch Enable	I/O	12	This active high, tri-state signal is used to latch the contents of the address bus bits LA(17–23). The address latch is opened when BALE is high and the address is latched on the high to low transition of this signal. This signal is not driven when the 86C05 is bus master in AT mode. BALE connects directly to the AT bus.
DACK(2) DACK(1) DACK(0)	DMA Acknowledge	I	144 145 146	When the 86C05 asserts one of the DRQ lines thecorresponding, active low, DMA acknowledge is returned from the DMA subsystem. This signal indicates the 86C05 now has priority to use the AT bus. For AT bus operation the 86C05 asserts the -MASTER signal and waits 10 clocks or 20 clocks (register 5, bit 4) before asserting an AT bus control signal. These pins connect directly to the AT bus.
DRQ(2) DRQ(1) DRQ(0)	DMA Request	O	139 141 142	These tri-state outputs are used to request ownership of the AT bus. These signals are high true. The 86C05 asserts one of these lines then waits for the corresponding DACK to be returned from the system board. These pins connect directly to the AT bus.
HOST_OWN	Host Own	O	15	When this totem pole signal is asserted the 86C05 is the current owner of the AT bus.
I/O CHCK	I/O Channel Check	I/O	151	This active low totem pole signal is used to indicate a serious error. It is asserted when the host processor or local MPU writes a one to bit

Table 17. Host Interface—AT Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
				7 of register 5. A zero written to this register deasserts this signal. The 86C05 terminates the host bus transfer, with an access error, if this signal is asserted. This pin should connect directly to the AT bus.
IOCHRDY	I/O Channel Ready Input	I	148	This active high input signal lengthens a bus cycle from its standard time when a device or memory cannot respond quickly enough. When IOCHRDY is low the 86C05 inserts wait cycles until the device or memory brings it high. This pin connects directly to the AT bus.
IOCS16	I/O Chip Select 16 bits	I	153	When this active low input signal is asserted it notifies the 86C05 that the addressed I/O device is capable of transferring 16 bits of data at once. When this signal is asserted, the internal 8 bit bus conversion logic is disabled. This signal should be generated by the I/O device from an address decode of the SA bits. This pin connects directly to the AT bus.
IOCS32	I/O Chip Select 32 bits	I	159	When this active low input signal is asserted it notifies the 86C05 that the addressed I/O device is capable of transferring 32 bits of data at once. When this signal is asserted, the internal 8 bit and 16 bit bus conversion logic is disabled. This signal is generated by the I/O device from an address decode of the SA bits. The hardware engineer should connect this pin to VDD when using a 16 bit data bus. The reader should note that this signal is not one of the "standard" AT bus lines.
IORD	I/O Read	I/O	53	This active low tri-state signal indicates when an I/O device is to send data to the data bus. This pin connects directly to the AT bus.

Table 17. Host Interface—AT Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
IOWR	I/O Write	I/O	52	This active low tri-state signal indicates when an I/O device is to accept data from the data bus. This pin connects directly to the AT bus.
IRQ(2) IRQ(1) IRQ(0)	Interrupt Request	I/O	129 130 132	These active low open collector signals are used to inform a system or concurrent completion of a task. The 86C05 can also processor of the monitor these signals and interrupts the local MPU when one or more lines become active (register 23). The 86C05 drives these lines by setting the corresponding bit in register 18. The system or concurrent processor clears the interrupt by writing the I/O register indicated below: Interrupt — I/O Register IRQ0 — Register 8 IRQ1 — Register 9 IRQ2 — Register 10 If the user needs the capability to change interrupt lines than external selection jumpers must be added to the I/O card. For example, 86C05 pin IRQ0 could be jumper selectable to AT bus interrupts IRQ(3–7). These signals are internally pulled high (400 µa). These pins connect to the AT bus thru a 74LS04 driver.
LA17 LA18 LA19 LA20 LA21 LA22 LA23	Latchable Address	O I/O	158 155 138 76 77 78 79	These active high tri-state signals are latchable address bits which are used to decode zero or one wait state memory. They are valid through out the memoryaccess cycle and connect to the AT bus thru an LS245 bus transceiver.
MADE24	Memory Address Enable 24	I/O	13	This active high tri-state signal indicates when an extended (address bits 24 –31) address is used on the AT bus. When this signal is low a 32 bit memory address is placed on the bus. When this signal is high a 24 bit address is on

Table 17. Host Interface—AT Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
				the bus. When the firmware engineer requests 32 bit transfers, the additional 8 bits must be provided external to the 86C05. The reader should note that this signal is not one of the "standard" AT bus control lines.
MASTER	Master	O	29	This active low output signal indicates that the 86C05 is controlling the AT bus. It is asserted when the DRQ0, DRQ1, or DRQ2 is active and the corresponding -DACK signal is received. This pin connects directly to the AT bus.
MEMCS16	Memory Chip Select	I	156	This active low input signal notifies the 86C05 that the addressed memory is capable 16 bits transferring 16 bits of data at once. Asserting this signal prevents the 16 bit to 8 bit bus conversion logic from being activated. This pin connects directly to the AT bus.
MEMCS32	Memory Chip Select 32 bits	I	152	This active low input signal notifies the 86C05 that the addressed memory is capable of transferring 32 bits of data at once. Asserting this signal prevents the 16 bit to 8 bit bus conversion logic and the 32 bit to 16 bit bus conversion logic from being activated. The hardware engineer should tie this input to VDD volts when using a 16 bit data bus. The reader should note that this signal is not one of the "standard" AT interface lines.
MEMR	Memory Read	I/O	149	This active low tri-state signal indicates read memory cycle. This pin connects directly to the AT bus.
MEMW	Memory Write	I/O	28	This active low tri-state signal indicates a memory write cycle. This pin connects directly to the AT bus.

Table 17. Host Interface—AT Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
SA(0–2) SA(3–7) SA(8–14) SA(15–19)	System Address	I/O	48–50 55–59 61–67 71–75	These active high tri-state signals address memory or I/O devices within the system. They form the low-order 20 bits of the 24 bit address bus. These lines are latched on the bus when BALE goes from a high to low state. These pins are connected to the AT bus thru an LS245 bus transceiver.
SBHE	System Byte High Enable	O	69	This active low tri-state signal enables the transfer of data on byte 1 (bits 8–15) of the data bus. It is used with A0 to distinguish between byte 0 (bits 0–7) and byte 1 (bits 8–15) transfers. This pin connects directly to the AT bus.
SD(0–4) SD(5–14) SD(15–20) SD(21–30) SD(31)	Data Bits	I/O	45–41 40–31 26–21 10–1 160	These are active high, tri-state signals. All data transfers between the AT bus and the MPU or DMA interface flow through these signals. These pins connect to the AT bus thru LS245 transceivers. When the 86C05 only transfers 16 bits of data to the bus, then D(16–31) maybe programmed (register 5, bit 5) as an I/O port.
SWEN	System Word High Enable	O	132	This active low tri-state signal enables the transfer of data on bytes 2 and 3 (bits 16–32) of the data bus. It is used with A1 to distinguish between word 0 (bits 0–15) and word 1 (bits 16–31) transfers. The reader should note that this pin is not one of the "standard" AT control signals.
RESET DRV	Bus Reset	I	154	This active high input signal provides a hard reset to the 86C05 chip. Internal logic is initialized by this signal and any transfer operations are aborted.

The 86C05 NuBus Interface consists of 91 signals as outlined below. The 86C05 is configured to operate in the NuBus host interface mode when CONFIG2 is low and the CONFIG3 pin is low. The following abbreviations are used:

I/O = Input and Output Pin
I = Input Pin Only
O = Output Pin Only
TS = Tri-state Pin
OC = Open Collector Pin
TP = Totem Pole Pin

Table 18. Host Interface—NuBus Bus Pin Summary

Pin(s) Name	Number of Signals	Input/ Output	Pin Type	Pin Drive(ma)
ACK	1	I/O	TS	24
AD(0–31)	32	I/O	TS	4
ARB_IN(0–3)	4	I	–	–
ARB_OUT(0–3)	4	O	TP	4
CLK	1	I	–	–
HOST_OWN	1	O	TS	8
ID(0–3)	4	I	–	–
NA(0–17)	18	O	TP	4
NMRQ(0–2)	2	I/O	OC	4
PI(0–7)	8	I	–	–
PO(0–7)	8	O	TP	4
RESET	1	I	–	–
RSLOCK	1	O	TP	4
RQST	1	I/O	TP	24
SLOT	1	O	TP	24
START	1	I/O	TS	24
SSLOT	1	O	TS	24
TM(0–1)	2	I/O	TS	24

Table 19. Host Interface—NuBus Bus

Symbol	Signal Name	I/O	Pin Number	Function
ACK	Ack	I/O	13	This active low tri-state signal indicates the slave has completed the read or write request. During a read operation data is valid when this signal is low. Data is clocked into the bus master on the high to low transition of the CLK. For a write operation the data must be held throughout the Acknowledge cycle. This pin connects directly to the NuBus.

Table 19. Host Interface—NuBus Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
AD(0–4) AD(5–14) AD(15–20) AD(21–30) AD(31)	Address/ Data	I/O	45–41 40–31 26–21 10–1 160	These active high tri-state signals are the multiplexed address and data bus. During the Start cycle of a transaction these lines contain the address of the slave. For a write transaction these signals then carry the write data until the beginning of the next Start cycle. For a read transaction these signals are unknown until the Acknowledge cycle, at which time they hold the data from the slave. These lines connect to the NuBus thru a ALS640 bus transceiver.
ARB_IN(3) ARB_IN(2) ARB_IN(1) ARB_IN(0)	Arb Bus Priority In	I	143 144 145 146	These active low input pins connect directly to the NuBus and receive arbitration bus priority levels.
ARB_OUT(3) ARB_OUT(2) ARB_OUT(1) ARB_OUT(0)	Arb Bus Priority Out	O	138 139 141 142	These active low totem pole output signals are used topresent arbitrating bus participant priority levels. The priority level of the 86C05 is programmed into register 5. These pins are connected to the NuBus by paralleling LS240s inverters. That is, connect the respective -ARB_OUT pin to the OE pin of the LS245. Tie the inputs to the four inverters to ground and connect the outputs from the inverters, in parallel, to the NuBus. Each of the four ARB_OUT lines should be connected in this manner. This type of connection is required to achieve the 60 ma drive current required for NuBus.
CLK	Clock	I	152	This input clock line is used to synchronize all NuBus address, data, control, and arbitration signals. It has a period of 100 ns and a duty cycle of 75% high and 25% low. The low to high transition of this signal is called the driving edge and the high to low transition is called the sampling edge. This pin connects directly to the NuBus.

Table 19. Host Interface—NuBus Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
HOST_OWN Own	Host	O	15	When this totem pole signal is asserted the 86C05 is the current owner of the NuBus.
-ID(3) -ID(2) ID(1) -ID(0)	ID Bits	I	134 135 136 137	These active low inputs signals produce a hexidecimal ID digit between the value 0h and Fh. Each card slot in the NuBus backplane has its own unique ID. This ID is used for arbitration and also defines the card's memory or I/O space. These pins connect directly to the NuBus.
NA(0–2) NA(3–7) NA(8–14) NA(15–17)	NuBus Latched Address	O	48–50 55–59 61–67 71–73	These active high output lines are the latched address for the current NuBus transaction. These lines typically connect to a BIOS PROM and/or other I/O card logic.
NMRQ(2) NMRQ(1) NMRQ(0)	Non- Master Request	I/O	129 130 133	These active low open collector signals are used to indicate a non-master device request interrupt processing. The 86C05 can also monitor these signals and generate an interrupt to the local MPU when they are active (register 23). One of these lines connect to the Apple NuBus thru a driver.
PI(7) PI(6) PI(5) PI(4) PI(3) PI(2) PI(1) PI(0)	Port In	I	155 156 153 154 149 159 157 158	These active high input signals are read by the MPU or Host processor as register 7. These signals are unlatched and therefore could be changing asynchronously with respect to the processor.
PO(0–5) PO(6) PO(7)	Port Out	O	74–79 69 132	These active high totem pole output signals are set or cleared when the MPU or host processor writes to register 7.

Table 19. Host Interface—NuBus Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
RESET	Bus Reset	I	154	This active low input signal provides a hard reset to the 86C05 chip. Internal logic is initialized by this signal and any transfer operations are aborted. This pin connects directly to the NuBus.
RSLOCK	Resource Lock	O	46	When this active high totem pole signal is , assertedthe 86C05 has detected a NuBus resource lock cycle.
RQST	Request	I/O	29	This active low tri-state signal is asserted when a bus master wants to use the NuBus. It may only be asserted if it was not active on the previous cycle. When this signal is asserted the -ARB_IN(0–3) and ARB_OUT (0–3) lines determine which of the arbitrating slots will become the next bus master. Once asserted, this signal stays active until the 86C05 becomes bus master. This pin is connected to the NuBus by paralleling LS240s inverters. That is, connect this pin to the -OE pin of the LS245. Tie the inputs to the four inverters to ground and connect the outputs from the inverters, in parallel, to the NuBus. This type of connection is required to achieve the 60 ma drive current required for NuBus.
SLOT	Slot Space Accessed	O	28	When this active high totem pole signal is asserted, the 86C05 has detected an access to this cards slot space.
START	Start	I/O	12	This active low tri-state signal is asserted to indicate the address cycle of a NuBus transaction. It also initiates an arbitration contest. This pin connects directly to the NuBus.

Table 19. Host Interface—NuBus Bus (continued)

Symbol	Signal Name	I/O	Pin Number	Function
SSLOT	Super Slot Space	O	148	When this active high totem pole signal is asserted, the 86C05 has detected an access to Accessed this cards super slot space.
TM(1) TM(0)	Transfer Mode 0	I/O	52 53	These active low tri-state signals are used at the beginning of a transaction to indicate the type of transaction being initiated. Later in the transaction the responding module uses them to indicate success or failure of of the requested transaction. These pins connect directly to the NuBus.

The 86C05 MPU Interface consists of 18 signals as outlined below. The following abbreviations are used:

I/O = Input and Output Pin
I = Input Pin Only
O = Output Pin Only
TS = Tri-state Pin
TP = Totem Pole Pin

Table 20. MPU Interface—Pin Summary

Pin(s) Name	Number of Signals	Input/ Output	Pin Type	Pin Drive(ma)
MFIFO_RDY	1	O	TP	4
MIORD	1	I	–	–
MIOWR	1	I	–	–
MA(0–2)	3	I	–	–
MA_D(0–7)	8	I/O	TS	4
MALE/MA(3)	1	I	–	–
MINT	1	O	TP	4
MIO_-MEM	1	I	–	–
OSC_D2/MA(4)	1	I/O	TP	4

Table 21. MPU Interface

Symbol	Signal Name	I/O	Pin Number	Function
MFIFO_RDY	FIFO Ready	I	127	This totem pole active high signal is asserted when the FIFO is waiting for a new byte from the MPU, or it has a new byte to send to the MPU. When the MPU FIFO Buffer Register 31 is accessed, this signal is cleared. This pin is enabled by bit 1 of register 16.
MIORD	I/O Read	I	104	When the CONFIG0 pin is low this active low input signal is used by the MPU to read status information from the 86C05. When the CONFIG0 pin is high, this active low input signal is data strobe (-DS). If IOWR is low (R/-W) when this signal is active, a write operation to the 86C05 is initiated. If -IOWR is low when this signal is active, a read operation is initiated.
MIOWR	I/O Write	I	105	When the CONFIG0 pin is low, this active low input signal is used by the MPU to write data to the 86C05. When the CONFIG1 pin is high, this signal determines whether the MPU wants to perform a read operation (-IORD high) or write operation (-IORD low) from/to the 86C05.
OSC_D2/MA(4) MALE/MA(3) MA(2) MA(1) MA(0)	Address Bit 3	I	118 103 123 124 125	When the CONFIG1 signal is low, these active high signals provide address bits 0–4 respectfully. This is used for internal register selection. The reader should note that MA(3) is the MALE pin and MA(4) is the OSC_D2 pin. This implies the OSC_D2 pin is not available when a non- multiplexed bus is specified. When the CONFIG1 pin is low bits MA(0–2) are used for address comparison with de-multiplexed address bits 5, 6, and 7 respectfully. When a comparison is made an internal chip select is generated.

Table 21. MPU Interface (continued)

Symbol	Signal Name	I/O	Pin Number	Function
MA_D(0–4) MA_D(5–7)	Address/ Data Bus	I/O	115–111 109–107	These are active high, tri-state signals. When the CONFIG0 pin is high, these address/data lines interface with the MPU lower 8-bit address/data bus. The addresses are latched into the internal address register by the deasserting edge of MALE. If the address is within the range of the internal chip select, A(0–2), the 8-bit data is written/read to/from a 86C05 register depending on the I/O write or I/O read input control lines.
MD0-MD7	Data Bus	I/O		When CONFIG1 pin is pulled low these lines carry only data.
MALE/MA(3)	Address Latch Enable	I	103	When the CONFIG0 pin is low, this active high input strobe is for latching the address from the multiplexed MA_D(0–7) (Address/ Data) bus. The address is latched into an internal address register on the high to low transition of this signal. The latched address bits are used for internal chip and register selection. When the CONFIG0 pin is high this active low input strobe is for latching the address from the MA_D(0–7) bus. The address is latched into an internal address register on the low to high transition of this signal. When the CONFIG1 pin is low this input provides bit 3 of the demultiplexed address bus.
MINT	MPU Interrupt		128	The active polarity of this signal is determined by bit 0 of register 16. This signal is asserted when an interrupt condition is present and the mask bit for that condition is a one (see register 23). For latched bits, the MPU interrupt is cleared when the MPU reads Interrupt Status Register 23. For unlatched bits, it is cleared when the pass-through interrupt condition disappears.

Table 21. MPU Interface (continued)

Symbol	Signal Name	I/O	Pin Number	Function
MIO_-MEM	I/O or Memory	I	106	When CONFIG0 pin is low this high true input signal enables I/O read and I/O write signals. When this signal is low, 86C05 MPU access is disabled. When CONFIG0 pin is high this low true (-DM) Data Memory signal is used to enable data strobe (-IORD signal). If this signal is high data strobe is disabled.

The 86C05 DMA Interface consists of 20 signals as outlined below. The following abbreviations are used:

I/O = Input and Output Pin
I = Input Pin Only
O = Output Pin Only
TS = Tri-state Pin
TP = Totem Pole Pin

Table 22. DMA Interface—Pin Summary

Pin(s) Name	Number of Signals	Input/ Output	Pin Type	Pin Drive(ma)
DD0(0–7)	8	I/O	TS	4
DD1(0–7)	8	I/O	TS	4
DMA_ACK	1	I	TP	4
DMA_REQ	1	O	TP	4
DP(0)/RD	1	I/O	TS	4
DP(1)/WRT	1	I/O	TS	4

Table 23. DMA Interface

Symbol	Signal Name	I/O	Pin Number	Function
DD0(0–7) DD1(0–7)	DMA Data	I/O	99–92 89–82	These active high, tri-state signals pass 8 or 16 bits of data to/from the internal FIFO and the DMA interface. The DMA interface could be connected to an intelligent peripheral chip (86C05 is a DMA controller) or to a DMA controller (86C05 is a DMA device).

Table 23. DMA Interface (continued)

Symbol	Signal Name	I/O	Pin Number	Function
DMA_ACK	DMA Acknowledge	I	102	The active polarity of this signal is set by register 21, bit 6. When the DMA Interface is programmed to operate as a DMA device, this signal is an acknowledge (in response to DMA_REQ being asserted) from the external DMA controller or device. It indicates the 86C05 may now transfer data between the FIFO and the DMA Interface. When operating as a DMA controller, this signal indicates the peripheral device is requesting a data transfer.
DMA_REQ	DMA Request	O	100	The active polarity of this signal is set by register 21,bit 5. When the DMA Interface is programmed to operate as an DMA device, this signal is a request to transfer data to/from the 86C05 and the external DMA controller or device. It maybe asserted in level or edge mode (register 21, bit 4) when acting as a DMA device. When operating as a DMA controller, the 86C05 waits until the DMA_ACK signal is asserted and there is data to transfer to/from the FIFO. It then asserts this signal and transfers the data as specified (write or read) by the data flow bits (register 22, bits 0–2).
DP(1)/WRT DP(0)/RD	DMA Parity	I/O	81 90	These active high, tri-state signals provide parity for the DMA interface. DP0/RD is the parity bit for DD(0–7) and DP1/ WRT is the parity bit for DD(8–15). Parity is check/ generated at the DMA interface. When the DMA interface is functioning as a DMA controller these bits may be programmed to function as the 8237 -RD and -WRT strobes. See register 21 for more details.

The Utility Interface consists of 24 signals as outlined below. The following abbreviations are used:

I/O = Input and Output Pin
I = Input Pin Only
O = Output Pin Only
TS = Tri-state Pin
TP = Totem Pole Pin

Table 24. Utility Interface—Pin Summary

Pin(s) Name	Number of Signals	Input/ Output	Pin Type	Pin Drive(ma)
CONFIG(0–3)	4	I	–	–
GND	12	I	–	–
OSC_D2/MA(4)	1	I/O	TP	4
OSC_IN	1	I	–	–
OSC_OUT	1	O	–	–
RESET_OUT	1	O	TP	4
VCC	4	I	–	–

Table 25. Utility Interface

Symbol	Signal Name	I/O	Pin Number	Function
CONFIG0	Config0	I	122	This line is pulled up internally and used to select the MPU's strobe inputs. When this signal is low the 86C05 is configured for an 8085/ 8051 type MPU that uses individual read and write strobes. When this signal is left open, the 86C05 chip is configured for a Z8 type MPU that uses separate strobe and read/write signals.
CONFIG1	Config1	I	121	When this internally pulled high input is high, the 86C05 is configured to operate with a multiplexed address and data MPU bus. When this line is low, pins MA(0–4) are used to select internal registers.
CONFIG2 CONFIG3	Config2 Config3	I I	120 119	These internally pulled high inputs specify the host interface as outlined below:

CONFIG3	CONFIG2	Interface
0	0	NuBus
0	1	EISA
1	0	MicroChannel
1	1	AT

Table 25. Utility Interface (continued)

Symbol	Signal Name	I/O	Pin Number	Function
GND	Ground	I	110,131,147 150, 11, 14 27, 30, 51 54, 70, 91	These inputs must all be connected to system ground.
OSC_D2/MA(4)	Osc	O	118	The clock frequency of this output pin is a divide by two of the oscillator input when the CONFIG1 is high.
		I		When the CONFIG1 pin is low this input pin is the non-multiplexed address bus bit 4.
OSC_IN	Osc Input	I	116	The OSC_IN active high input pin is for a 40 MHz crystal or oscillator. The OSC_OUT is for a crystal connection.
OSC_OUT	Osc Output	O	117	
RESET_OUT	Reset Out	O	126	This totem pole output is normally used to reset I/O card logic. It is an "or" of the following signals: a. Host Reset pin b. Power on reset c. Write to register 4 bit 2(firmware reset) Prior to a firmware reset this pin can be disabled by asserting bit 7 of register 16.
VDD	Power	I	101, 140 20, 60	These input pins must connect to I/O card power

Chapter 3
D.C. Characteristics

3.1 ABSOLUTE MAXIMUM RATINGS

- Voltage on all pins with respect to GND range from -0.3 to 7.0 Vdc.
- Ambient operating temperature is 0°C to +70°C.
- Storage temperature is from -65°C to +150°C.

Note that stresses greater than those indicated may cause permanent damage. Operation of the chip at conditions above those shown is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the chip's reliability.

3.2 STANDARD TEST CONDITIONS

The characteristics shown below apply for the following test conditions, unless otherwise noted. Voltages are referenced to GND. Positive current flows into the reference pin. Standard conditions are as follows:

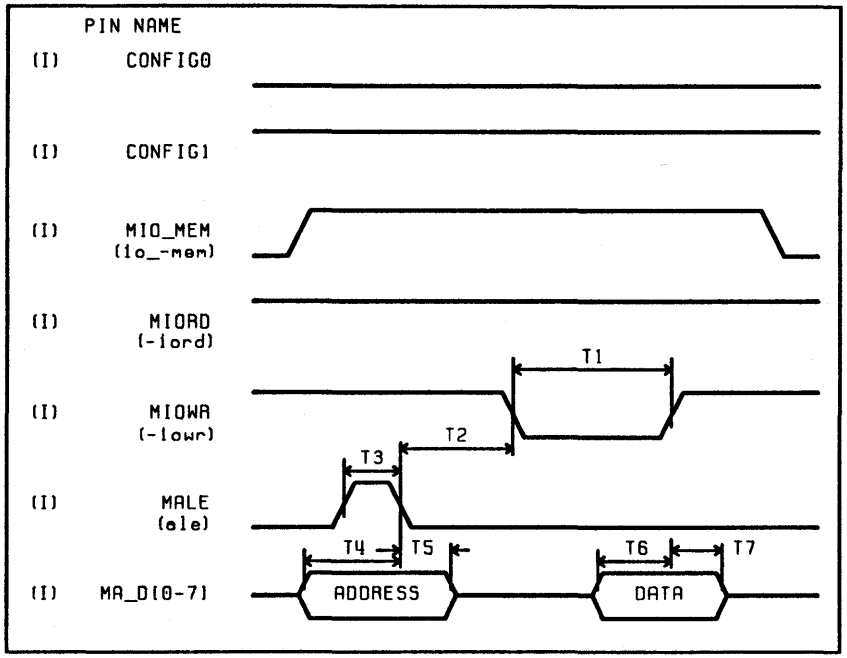
- VCC = 5.0 Vdc +/- 0.25 Vdc.
- GND = 0 Vdc
- 0°C < TA < 70°C

3.3 D.C. VALUES

Parameter	Min	Max	Unit
Input High Voltage	2	VCC	V
Input Low Voltage	-0.3	0.8	V
Output High Voltage	2	VCC	V
Output Low Voltage		0.4	V
Input Leakage	-30	10	µA
Output Leakage		10	µA
VCC Supply Current		50	mA

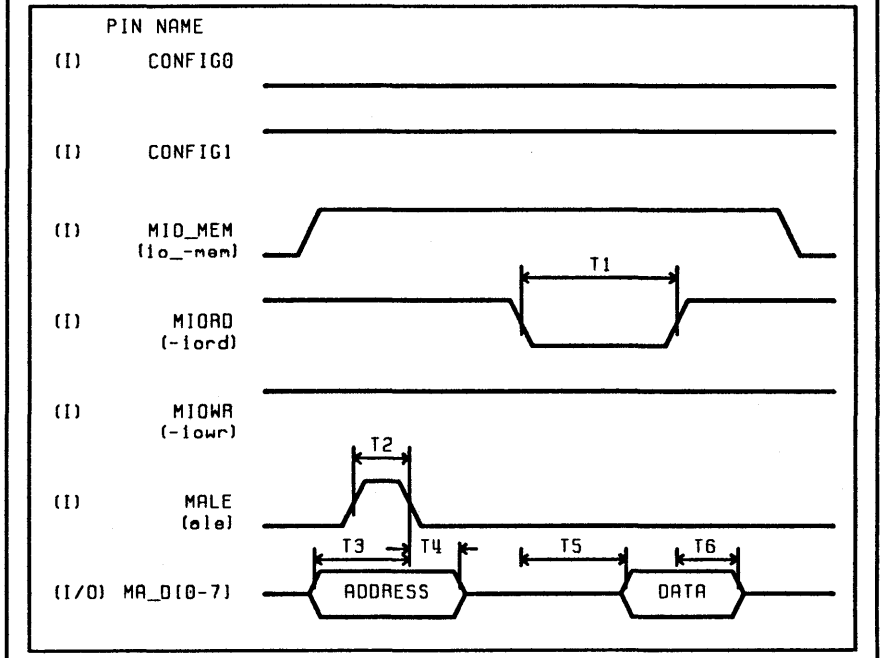
3.4 DRIVERS/RECEIVERS

- Drivers — Sink 24 mA @ 0.4 Vdc asserted
- Receivers — Asserted at input = 0 to 0.8 Vdc
  Non-asserted at input = 2.0 to 5.25 Vdc
  Minimum hysteresis = 0.2 Vdc



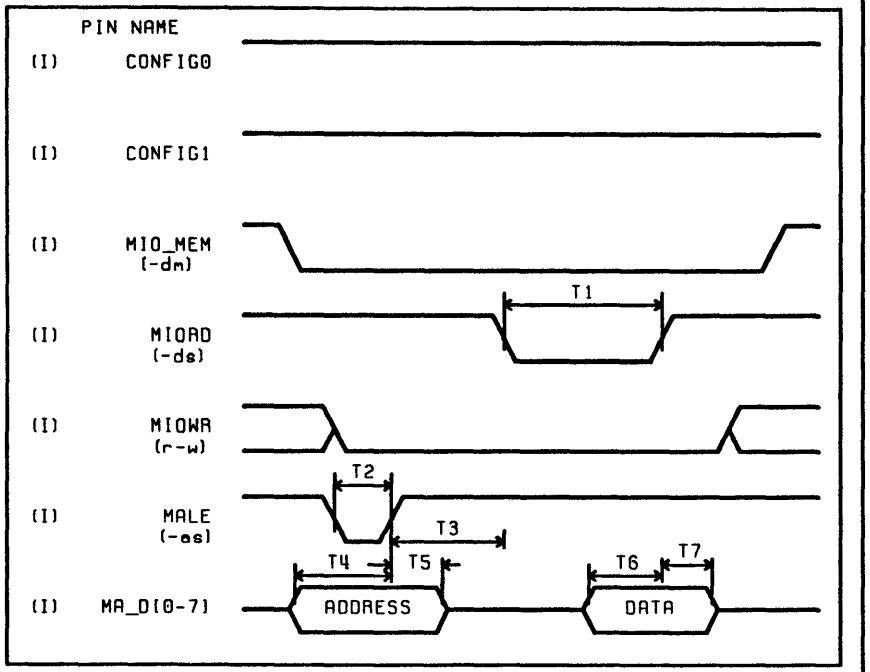
NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	(-iowr) low pulse width	60			ns
T2	(ale) low to (-iowr) low	25			ns
T3	(ale) high pulse width	20			ns
T4	Address setup to (ale) low	15			ns
T5	Address hold from (ale) low	15			ns
T6	Data setup to (-iowr) high	30			ns
T7	Data hold after (-iowr) high	15			ns

Figure 4-1. MPU Write Operation 8085/8051 Mode Timing Characteristics



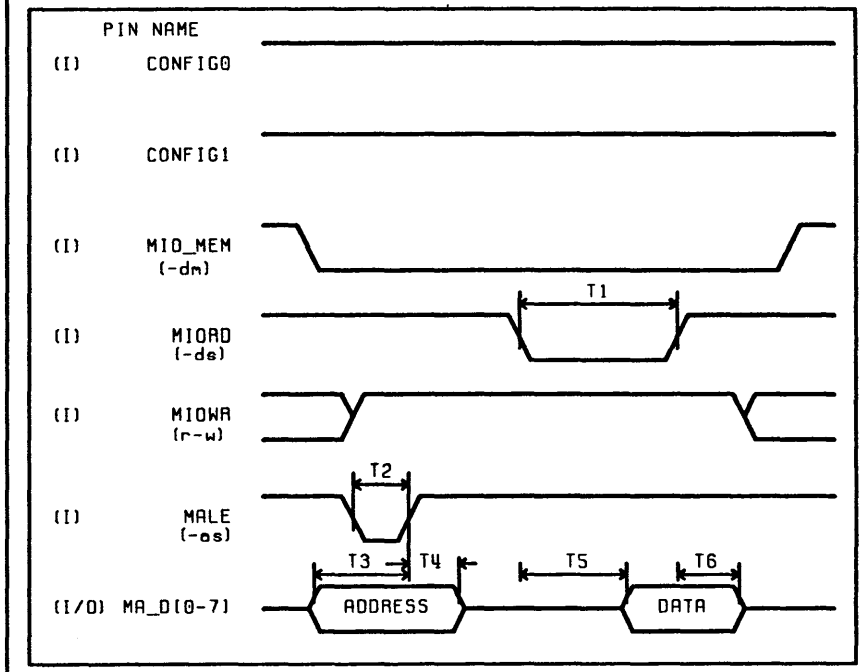
NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	(-iord) low pulse width	60			ns
T2	(ale) high pulse width	20			ns
T3	Address setup to (ale) low	15			ns
T4	Address hold from (ale) low	15			ns
T5	Data valid from (-iord) low			50	ns
T6	Data float from (-iord) high		20		ns

Figure 4-2. MPU Read Operation 8085/8051 Mode Timing Characteristics



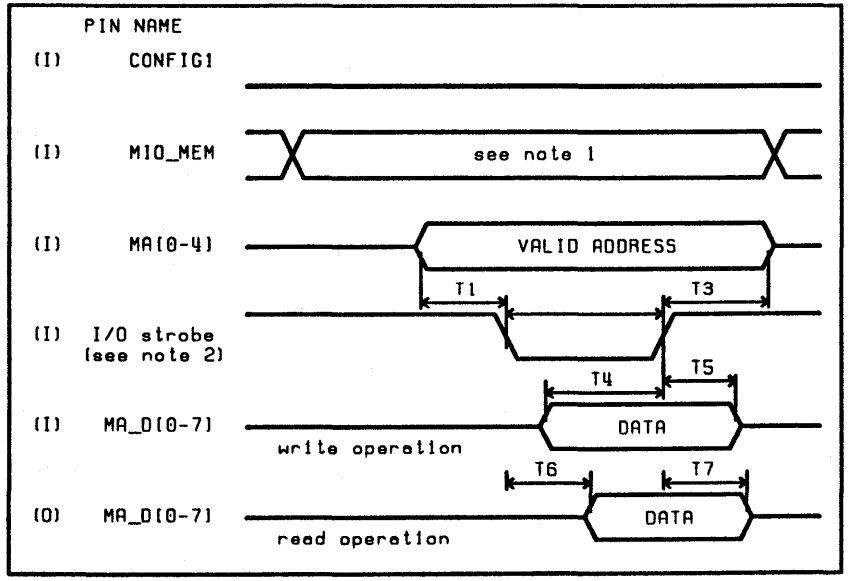
NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	(-ds) low pulse width	60			ns
T2	(-as) low pulse width	20			ns
T3	(-as) high to (-ds) low	25			ns
T4	Address setup to (-as) high	15			ns
T5	Address hold from (-as) low	15			ns
T6	Data setup to (-ds) high	30			ns

Figure 4-3. MPU Write Operation Z8 Mode Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	(-ds) low pulse width	60			ns
T2	(-as) low pulse width	20			ns
T3	Address setup to (-as) high	15			ns
T4	Address hold from (-as) high	15			ns
T5	Data valid from (-ds) low			50	ns
T5	Data valid from (-ds) low			50	ns
T6	Data float from (-ds) high		20		ns

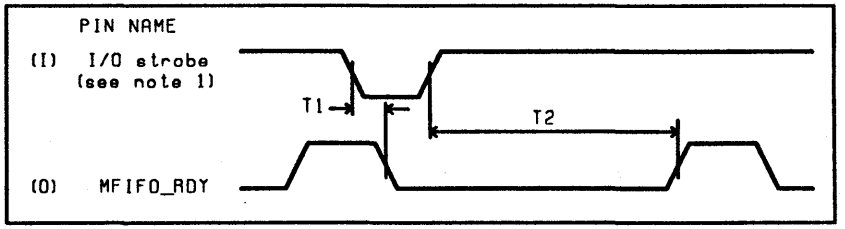
Figure 4-4. MPU Read Operation Z8 Mode Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	Valid address to I/O strobe low	20			ns
T2	I/O strobe low pulse width	60			ns
T3	Address hold from I/O strobe high	20			ns
T4	Write data set-up to I/O strobe high	30			ns
T5	Write data hold from I/O strobe high	15			ns
T6	Read data valid from I/O strobe low			50	ns
T7	Read data float from I/O strobe high		20		ns

Note:
1. Polarity of MIO_MEM signal based on CONFIG0 pin.
2. Actual I/O strobe pin based on polarity of CONFIG0 pin.

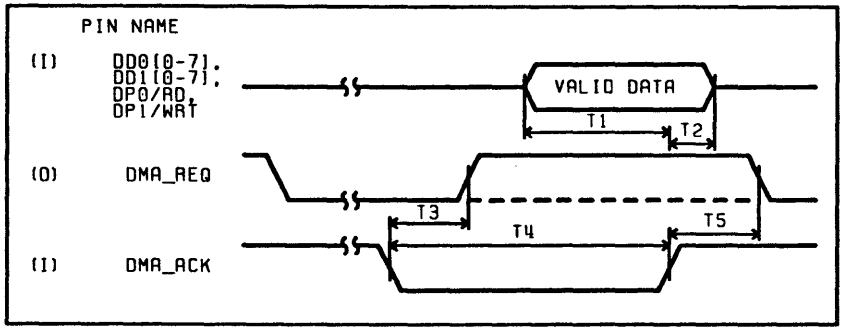
Figure 4-4. MPU Non-multiplexed Address/Data Bus Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	I/O strobe low to MFIFO_RDY low			30	ns
T2	I/O strobe signal high to MFIFO_RDY high	4CP			ns

Note:
1. Actual I/O strobe pin based on polarity of CONFIG0 pin.
2. This figure assumes an MPU I/O access to register 31.
3. CP is clock period (OSC1 pin).
4. Register 16 bit 1 must be equal to one to enable the MFIFO_RDY pin.
5. Status of the MPU MFIFO_RDY pin is read from register 15 bit 0. This bit is independent of the MPU MFIFO_RDY pin being enabled (Register 16 bit 1).

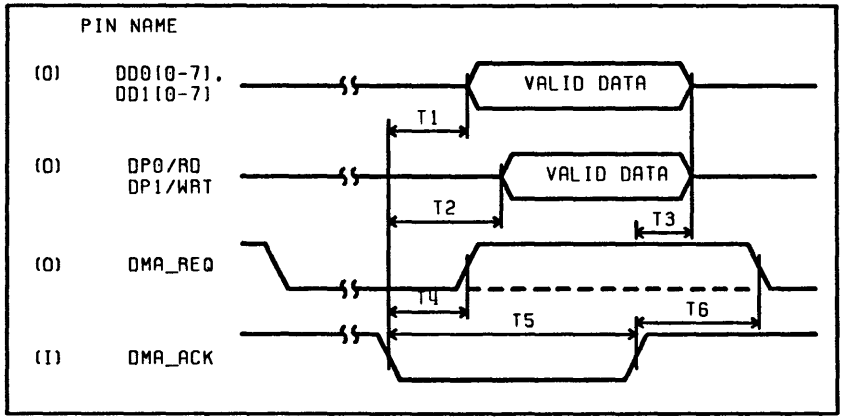
Figure 4-5 MPU MFIFO_RDY Cycle Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	Data valid to DMA_ACK high	10			ns
T2	Data hold from DMA_ACK high	10			ns
T3	DMA_ACK low to DMA_REQ high			25	ns
T4	DMA_ACK pulse width	2CP			ns
T5	DMA_ACK high to DMA_REQ low	0			ns

Note:
1. See registers 16 and 21 for DMA configuration.
2. Device mode set when register 21 bit 3 is zero.
3. This figure assumes DMA_ACK and DMA_REQ are low true.
4. CP is the clock period of the OSCI pin.
5. The 86C05 brings DMA_REQ high only after DMA_ACK is received and the chip is in edge mode or the transfer counter is equal to zero.
6. Parameter T5 is valid only for edge mode, i.e. when register 21 bits 3 and 4 are equal to zero.

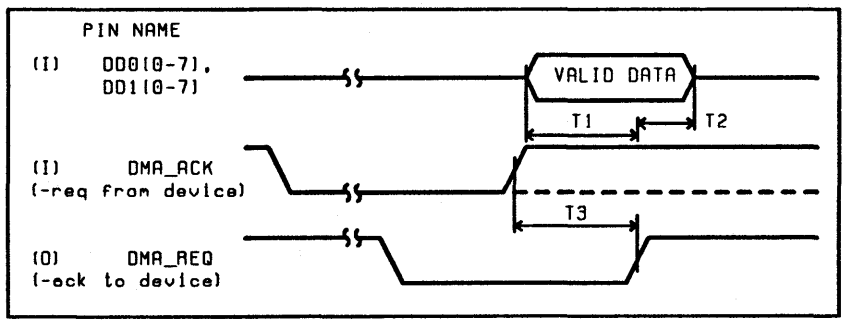
Figure 4-7. DMA Interface, Device Mode Transfer to 86C05 from DMA Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	Data valid from DMA_ACK low			20	ns
T2	Parity valid from DMA_ACK low			35	ns
T3	Bus float from DMA_ACK high		20		ns
T4	DMA_ACK low to DMA_REQ high			25	ns
T5	DMA_ACK pulse width	2CP			ns
T6	DMA_ACK high to DMA_REQ low	0			ns

Note:
1. See registers 16 and 21 for DMA configuration.
2. Device mode set when register 21 bit 3 is zero.
3. This figure assumes DMA_ACK and DMA_REQ are low true.
4. CP is the clock period of the OSCI pin.
5. The 86C05 brings DMA_REQ high only after DMA_ACK is received and the chip is in edge mode or the transfer counter is equal to zero.
6. Parameter T6 is valid only for edge mode, i.e. when register 21 bits 3 and 4 are equal to zero.

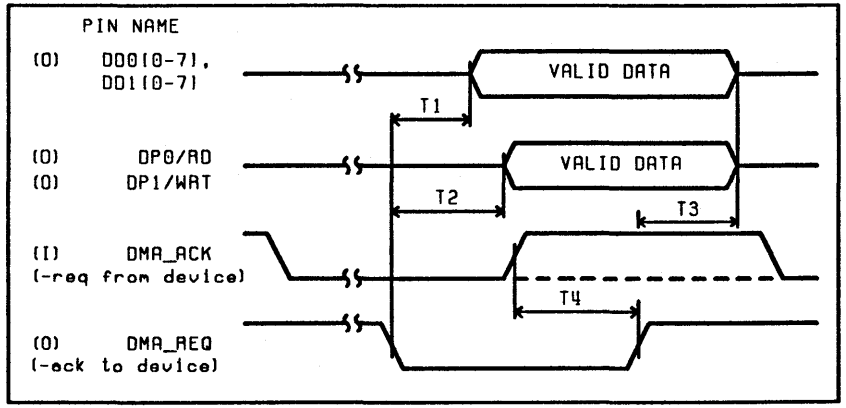
Figure 4-8. DMA Interface, Device Mode Transfer from 86C05 to DMA Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	Data valid to (-ack) high	10			ns
T2	Data hold from (-ack) high	10			ns
T3	(-req) high to (-ack) high (see note 6)	CP+20			ns

Note:
1. See registers 16 and 21 for DMA interface configuration.
2. Controller mode set when register 21 bit 3 is one.
3. The width of the (-ack) pulse is set by register 21 bits 0, 1, and 2.
4. This figure assumes DMA_ACK and DMA_REQ are low true.
5. CP is the clock period of the OSCI pin.
6. The device must deassert its (-req) within parameter T3 time to ensure the 86C05 stops DMA transfer. Parameter T3 is extended if the ack hold-off bit is true (register 21, bit 4). This extension applies to within T3 time of the end of the hold off period.
7. If the device continues to assert (-req) then the 86C05 may begin a new DMA cycle within 2CP of (-ack) going high from the previous cycle.

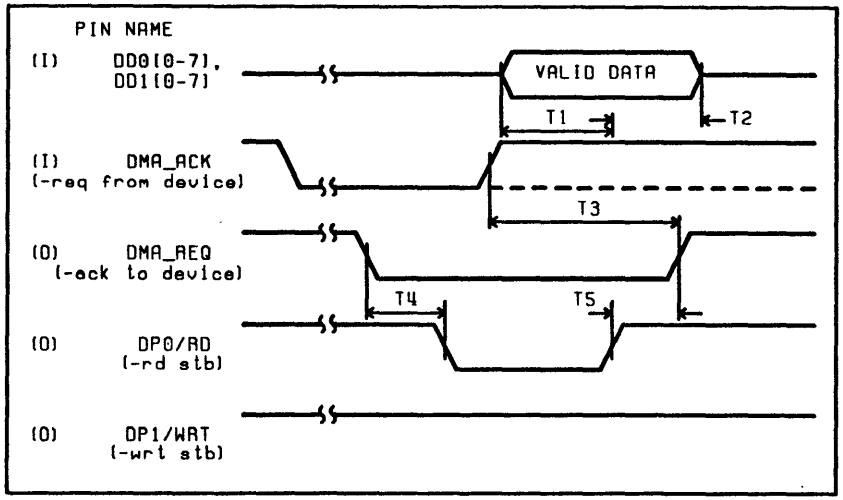
Figure 4-9. DMA Interface, Controller Mode (with parity) Transfer to 86C05 from DMA Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	Data valid from (-ack) low			20	ns
T2	Parity valid from (-ack) low			35	ns
T3	Bus float from (-ack) high		20		ns
T4	(-req) high to (-ack) high (see note 6)	CP+20			ns

Note:
1. See registers 16 and 21 for DMA interface configuration.
2. Controller mode set when register 21 bit 3 is one.
3. The width of the (-ack) pulse is set by register 21 bits 0, 1, and 2.
4. This figure assumes (-req) and (-ack) are low true.
5. CP is the clock period of the OSCI pin.
6. The device must deassert its (-req) within parameter T4 time to ensure the 86C05 stops DMA transfer. Parameter T4 is extended if the ack hold-off bit is true (register 21, bit 4). This extension applies to within T4 time of the end of the hold off period.
7. If the device continues to assert (-req) then the 86C05 may begin a new DMA cycle within 2CP of (-ack) going high from the previous cycle.

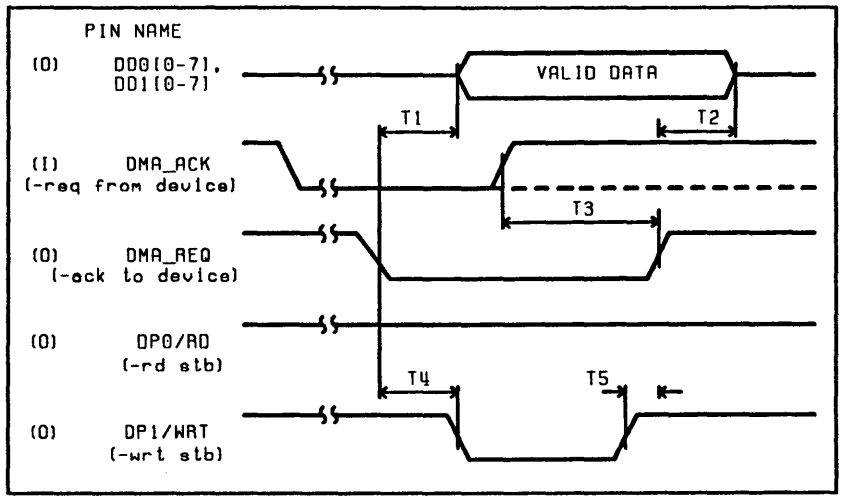
Figure 4-10. DMA Interface, Controller Mode (with parity) Transfer from 86C05 to DMA Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	Data valid to (-rd stb) high	10			ns
T2	Data hold from (-rd stb) high	10			ns
T3	(-req) high to (-ack) high (see note 6)	CP+20			ns
T4	(-ack) low to (-rd stb) low	2CP+10		2CP+10	ns
T5	(-rd stb) high to (-ack) high	CP-10		CP+10	ns

Note:
1. See registers 16 and 21 for DMA interface configuration.
2. Controller mode set when register 21 bit 3 is one.
3. The width of the (-ack) pulse is set by register 21 bits 0, 1, and 2 (must be > 3).
4. This figure assumes (-req) and (-ack) are low true.
5. CP is the clock period of the OSC1 pin.
6. The device must deassert its (-req) within time T3 to ensure the 86C05 stops DMA transfer. Parameter T3 is extended if the ack hold-off bit is true (register 21, bit 4). This extension applies to within T3 time of the end of the hold off period.
7. If the device continues to assert (-req) then the 86C05 may begin a new DMA cycle within 2CP of (-ack) going high from the previous cycle.

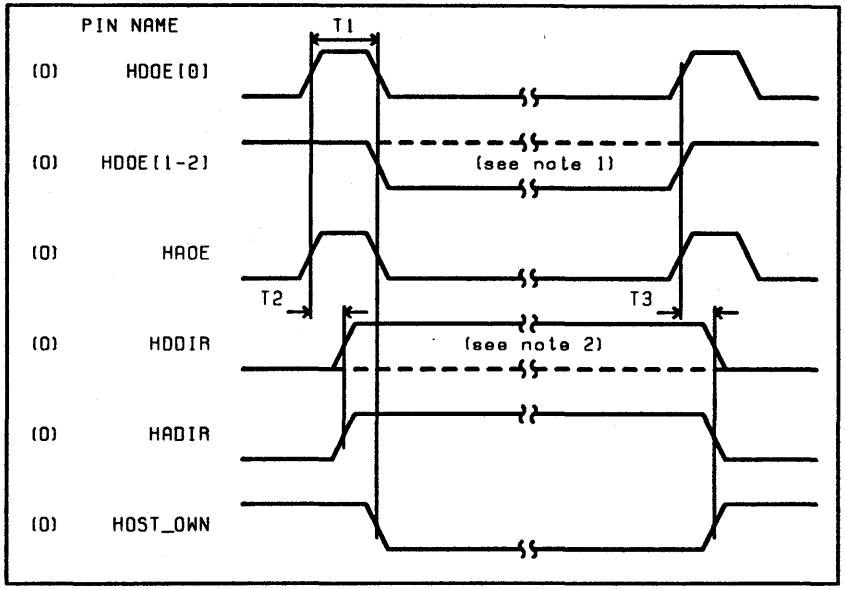
Figure 4-11. DMA Interface, Controller Mode (8237 strobes) Transfer to 86C05 from DMA Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	(-ack) low to valid data			20	ns
T2	Data float from (-ack) high		20		ns
T3	(-req) high to (-ack) high (see note 6)	CP+20			ns
T4	(-ack) low to (-wrt stb) low	2CP-10		2CP+10	ns
T5	(-wrt stb) high to (-ack) high	CP-10		CP+10	ns

Note:
1. See registers 16 and 21 for DMA interface configuration.
2. Controller mode set when register 21 bit 3 is one.
3. The width of the (-ack) pulse is set by register 21 bits 0, 1, and 2 (must be > 3).
4. This figure assumes (-req) and (-ack) are low true.
5. CP is the clock period of the OSC1 pin.
6. The device must deassert its (-req) within time T3 to ensure the 86C05 stops DMA transfer. Parameter T3 is extended if the (-ack) hold-off bit is true (register 21, bit 4). This extension applies to within T3 time of the end of the hold off period.
7. If the device continues to assert (-req) then the the 86C05 may begin a new DMA cycle within 2CP of (-ack) going high from the previous cycle.

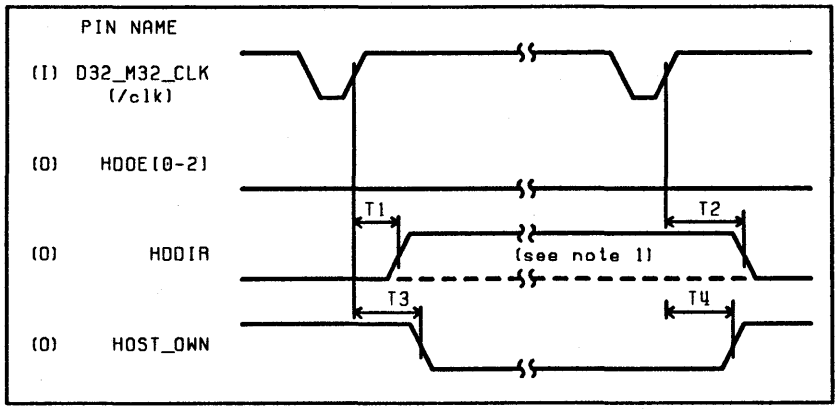
Figure 4-12. DMA Interface, Controller Mode (8237 strobes) Transfer to DMA from 86C05 Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	HDOE[0-2] and HAOE deassert pulse width		2CP		ns
T2	HDOE[0-2] and HAOE high to HDDIR and HADIR high		CP		ns
T3	HAOE high to HADIR low, HDDIR low, and HOST_OWN high		CP		ns

Note:
1. HDOE[1-2] are asserted for 16 and/or 32 bit transfers.
2. HDDIR is high for 86C05 to host data transfer.
3. CP is the clock period of the OSCI pin.
4. HDOE[0-2], HAOE, and HOST_OWN pins are low true signals.

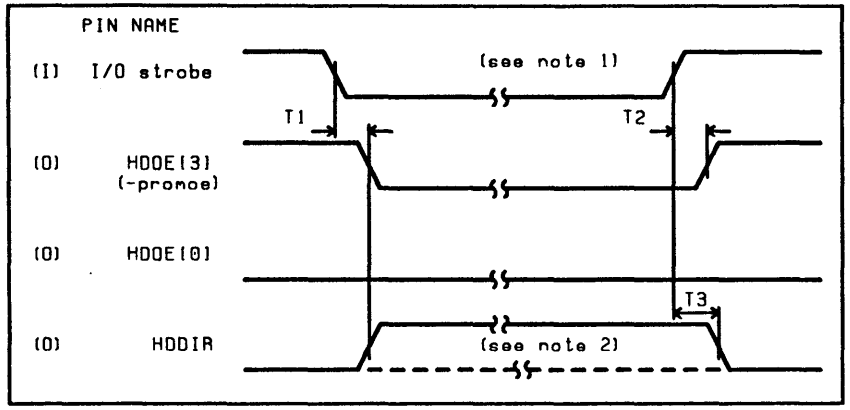
Figure 4-13. Host Transceivers, MicroChannel, EISA, and AT Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	(-clk) high to HDDIR high			21	ns
T2	(-clk) high to HOST_OWN low			24	ns
T3	(-clk) high to HDDIR low			22	ns
T4	(-clk) high to HOST_OWN high			20	ns

Note:
1. HDDIR is high for a 86C05 to host data transfer or 86C05 NuBus start cycle.
2. CP is the clock period of the OSCI pin.
3. HDOE[0-2] and HOST_OWN pins are low true signals.

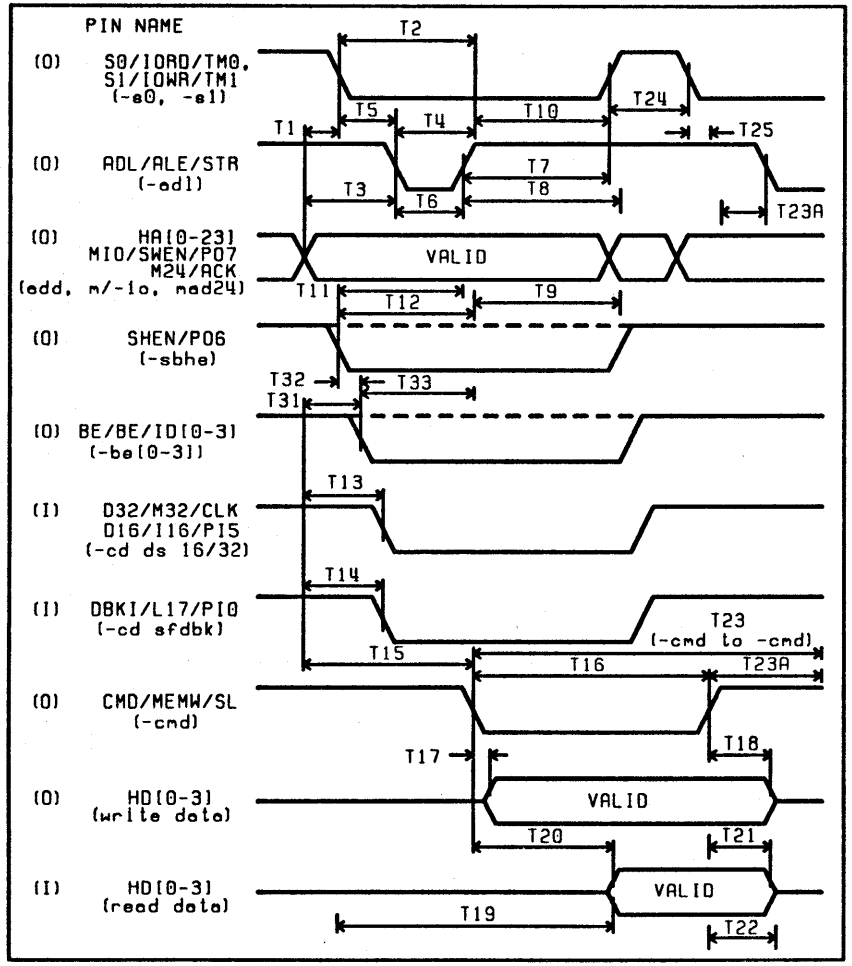
Figure 4-14. Host Transceivers, NuBus Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	I/O strobe low to [-promoe] low, and HDDIR high			27	ns
T2	I/O strobe high to [-promoe] high			22	ns
T3	I/O strobe high to HDDIR low			28	ns

Note:
1. I/O strobe pulse based on host interface;
   a. MicroChannel or EISA --> -CMD
   b. AT --> -IORD or -IOWR
   b. NuBus --> trailing edge of -START to trailing edge of 86C05 -ACK cycle.
2. HDDIR is high for host bus read cycle.
3. HDOE[0] and HDOE[3] are low true signals.

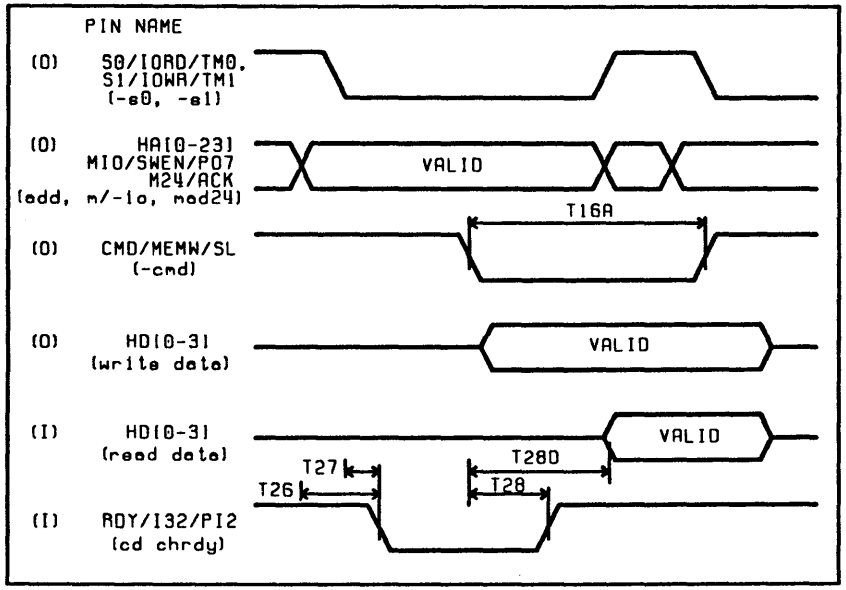
Figure 4-15. BIOS PROM Access Cycle Timing Characteristics



Note:
1. CP is the clock period of the OSCI pin.
2. Default pulse width of (-cmd) is programmable in register 18.

NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	(-s0, -s1) low true from (add, m/-io, mad24) valid	10			ns
T2	(-cmd) low true from (-s0, -s1) low true	4CP-10			ns
T3	(-adl) low true from (add, m/-io, mad24) low true	2CP			ns
T4	(-adl) low true to (-cmd) low true	2CP-10			ns
T5	(-adl) low true from (-s0, -s1) low true	2CP-10			ns
T6	(-adl) pulse width	2CP-10			ns
T7	(-s0, -s1) hold from (-adl) high	2CP-10			ns
T8	(add, m/-io, mad24) and (-sbhe) hold from (-adl) high	2CP-10			ns
T9	(add, m/-io, mad24) and (-sbhe) hold from (-cmd) low true	2CP-10			ns
T10	(-s0, -s1) hold from (-cmd) low	2CP-10			ns
T11	(-sbhe) setup to (-adl) high	2CP-10			ns
T12	(-sbhe) setup to (-cmd) low	2CP-10			ns
T13	(-cd ds 16/32) low from (add) valid			2CP+5	ns
T14	(-cd sfdbk) low from (add) valid			2CP+10	ns
T15	(-cmd) low from (add) valid	4CP-10			ns
T16	(-cmd) pulse width	4CP-15			ns
T17	(write data) setup to (-cmd) low	0			ns
T18	(write data) hold from (-cmd) high	2CP-10			ns
T19	(-s0, -s1) valid to (read data) valid			5CP	ns
T20	(read data) valid from (-cmd) low			2CP+10	ns
T21	(read data) hold from (-cmd) high	0			ns
T22	(-read data) tri-state from (-cmd) high			40	ns
T23	(-cmd) low to next (-cmd) low	8CP-10			ns
T23A	(-cmd) high to next (-cmd) low	4CP-10			ns
T23B	(-cmd) high to next (-adl)	2CP-10			ns
T24	Next (-s0, -s1) low from (-s1, -s0) high	2CP-10			ns
T25	Next (-s0, -s1) low to (-cmd) high			20	ns
T31	(-be[0-3]) low from (add) valid			40	ns
T32	(-be[0-3])) low from (-sbhe) HA[0] HA[1] asserted			30	ns
T33	(-be[0-3]) asserted to (-cmd) low	10			ns

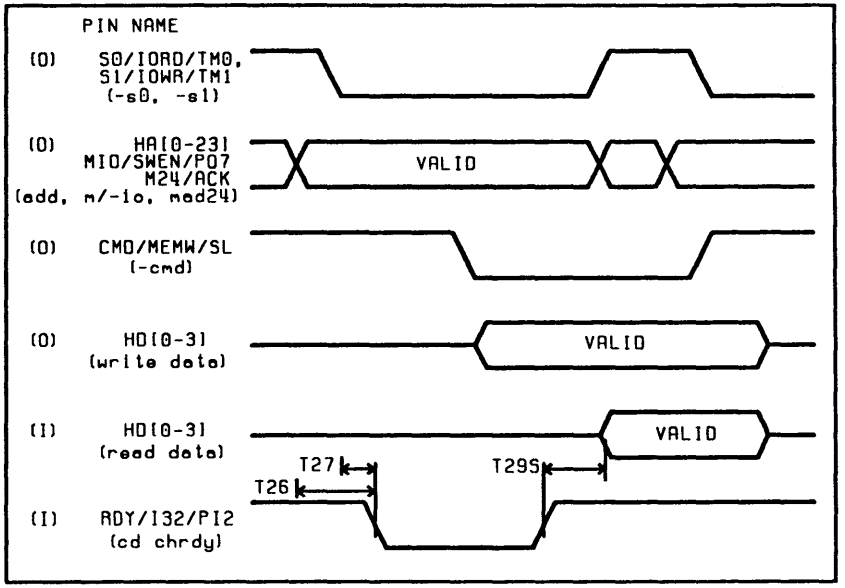
Figure 4-16. MicroChannel Bus Master Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T16A	(-cmd) pulse width	8CP-10			ns
T26	(cd chrdy) low from (add) valid			60	ns
T27	(cd chrdy) low from (-s0, -s1) low			30	ns
T28	(cd chrdy) high from (-cmd) low			30	ns
T28D	(read data) valid from (-cmd) low			8CP-40	ns

Note:
1. CP is the clock period of the OSCI pin
2. Slave must release (cd chrdy) within T28 time of (-cmd) going low for time T28D to be valid.

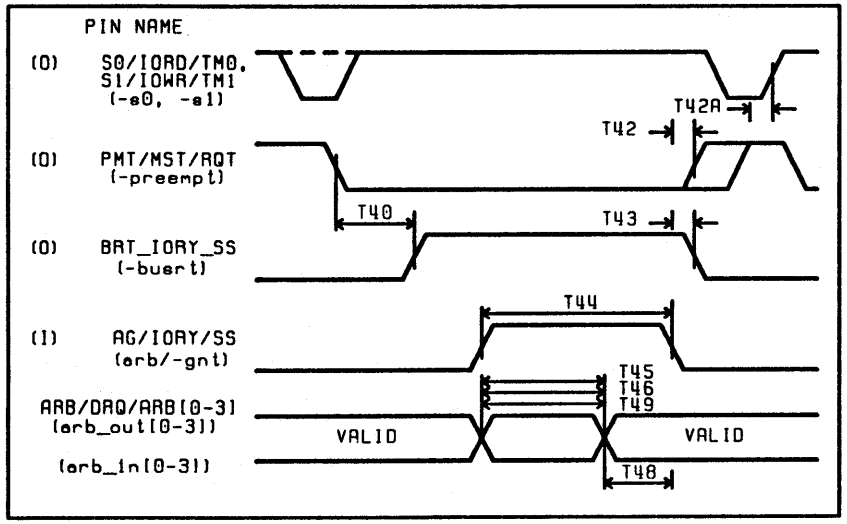
Figure 4-17. MicroChannel Bus Master Synchronous Extended Cycle Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T26	(cd chrdy) low from (add) valid			60	ns
T27	(cd chrdy) low from (-s0, -s1) low			30	ns
T29S	(read data) valid from (cd chrdy) low			6CP-40	ns

Note:
1. CP is the clock period of the OSCI pin
2. Asynchrounous extended cycle occurs when the slave releases (cd chrdy) asynchronously with repect to (-cmd).

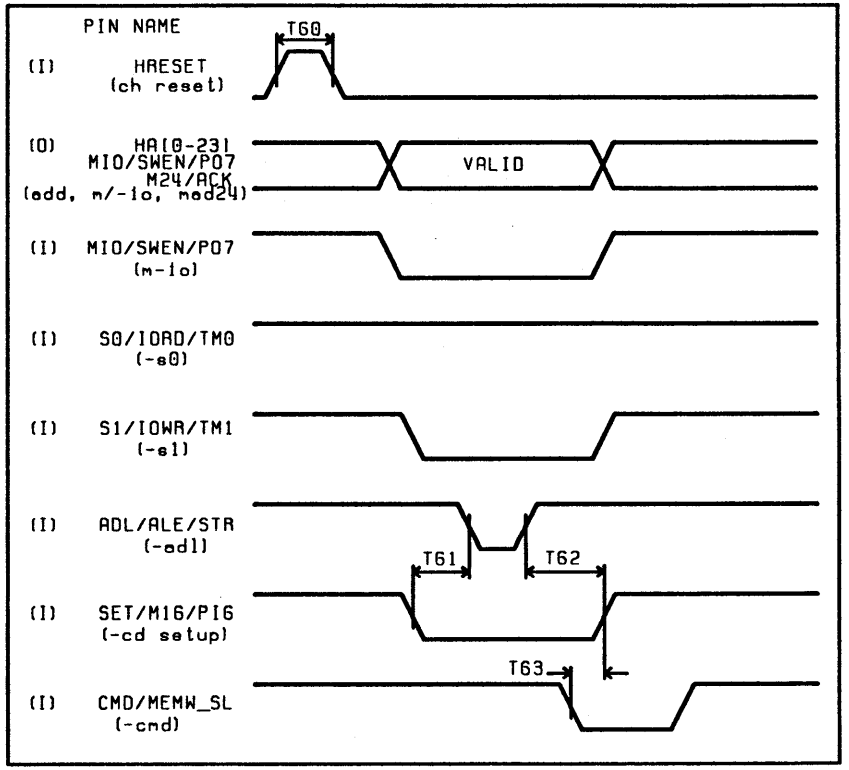
Figure 4-18. MicroChannel Bus Master Asynchronous Extended Cycle Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T40	(-preempt) low to end of xfer			(see note 1)	
T42	(-preempt) high from (arb/-gnt) low			50	ns
T42A	(-preempt) high to (-s0, -s1) high (exiting inactive state)	20			ns
T43	(-busrt) low from (arb/-gnt) low			40	ns
T44	(arb/-gnt) high pulse width	100			ns
T45	Driver turn-on/off delay from (arb/-gnt) low			40	ns
T46	Driver turn-on/off delay from low/higher priority line			40	ns
T48	Arb bus stable before (arb/-gnt) low	10			ns
T49	Tri-state drivers to (arb) high			40	ns

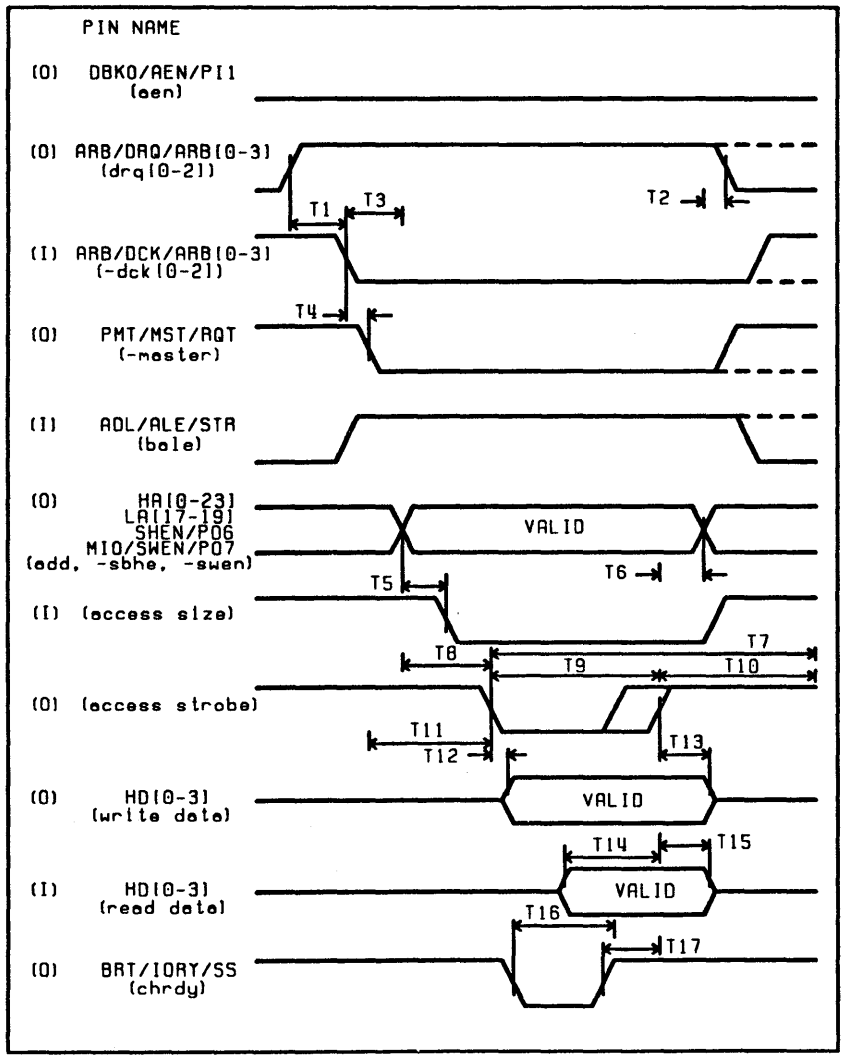
Note:
1. The max time the 86C05 stays on the MicroChannel after (-preempt) has been asserted is programmble in register 20.

Figure 4-19. MicroChannel Bus Arbitration Cycle Cycle Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T60	(ch reset) high pulse width	100			ns
T61	(-cd setup) low to (-adl) low	15			ns
T62	(-cd setup) hold from (-adl) low	25			ns
T63	(-cd setup) hold from (-cmd) low	30			ns

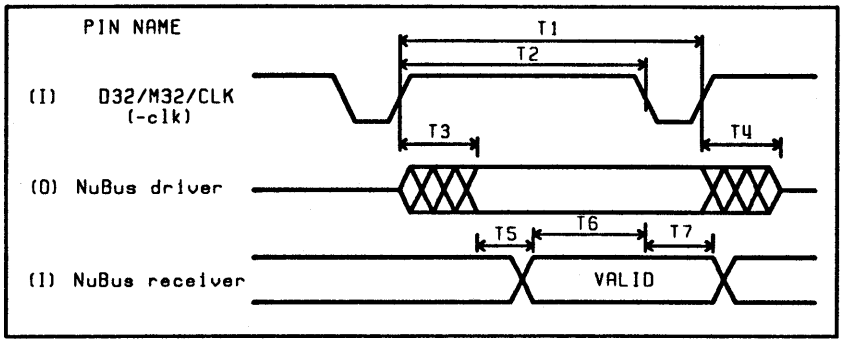
Figure 4-20. MicroChannel Configuration Cycle Cycle Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	(drq[0-2]) high to (-dck[0-2]) low	0			ns
T2	Bus tri-state to drq[0-2] low	2CP-10			ns
T3	(-dck[0-2]) low to bus drivers on	0		4CP+15	ns
T4	(-dck[0-2]) low to (-master) low	0		4CP+15	ns
T5	(access size) returned from (add) valid	0		3CP	ns
T6	(add) hold from (access strobe) high	1CP			ns
T7	(access strobe) to (access strobe)	8CP-10			ns
T8	(add) valid to access strobe	4CP-10			ns
T9	(access strobe) pulse width	4CP-10			ns
T10	(access strobe) high to next (access strobe) low	4CP-10			ns
T11	(access strobe) low from (-dck[0-2]) low	14CP			ns
T12	(write data) setup to (access strobe) low	0			ns
T13	(write data) hold from (access strobe) high	1CP			ns
T14	(read data) valid to (acesss strobe) high	25			ns
T15	(read data) hold from (access strobe) high	0			ns
T16	(chrdy) low from unextended end of (access strobe)			2CP	ns
T17	(chrdy) high to (access strobe) high			5CP	ns

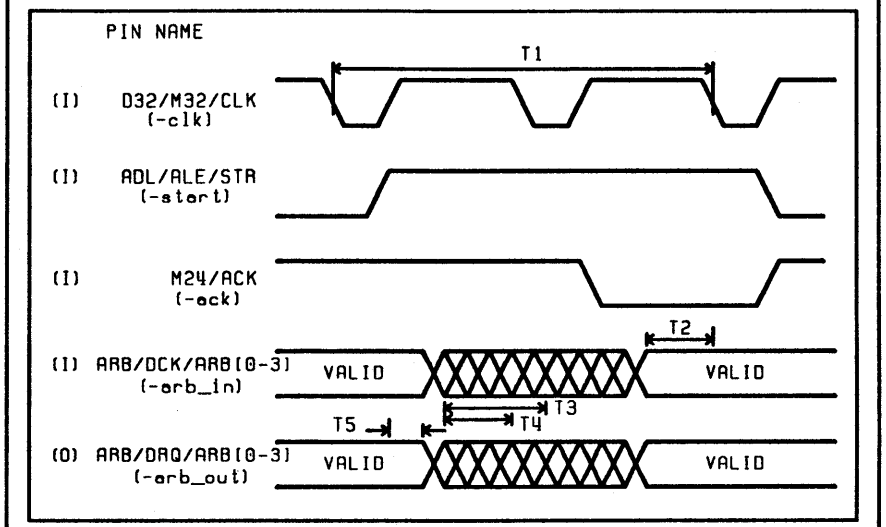
Note:
1. CP is the clock period of the OSCI pin.
2. Default pulse width of (access strobe) is programmable in register 19.
3. The addressed slave must deassert (chrdy) within parameter T16 time of the ended of the normal transfer cycle for the 86C05 to extend the cycle. For example, if resgister 19 is programmed for a 250 ns (access strobe) then (chrdy) must be deasserted 200 ns (CP = 25ns) after the leading edge of the (access strobe).
4. (access strobe) is one of the following pins: S0/IORD/TM0 (-iord), S1/IOWR/TM1 (-iowr), CMD/MEMW/SL (-memw), or AG/MEMR/PI3 (-memr).
5. (access size) is one of the following pins: RDY/I32/PI2, (-io 32) D16/I16/PI5 (-io 16), D32/M32/CLK (-m 32), or SET/M16/PI6 (-m 16).

Figure 4-21. AT (ISA) Bus Master Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	(-clk) period	99.99		100.01	ns
T2	(-clk) width	73		77	ns
T3	Driver turn-on time	0		25	ns
T4	Driver turn-off time	0		25	ns
T5	NuBus prop delay			17	ns
T6	Set-up time to (-clk) high	21			ns
T7	Hold time from (-clk) high	20			ns

Figure 4-22. NuBus Data Transfer Timing Characteristics



NAME	PARAMETER	MIN.	TYP.	MAX.	UNIT
T1	Arbitration time			200	ns
T2	Arbitraton set-up time	25			ns
T3	Driver turn-off time	10		30	ns
T4	Driver turn-on time	10		25	ns
T5	Arbitration hold time			10	ns

Figure 4-23. NuBus Arbitration Timing Characteristics

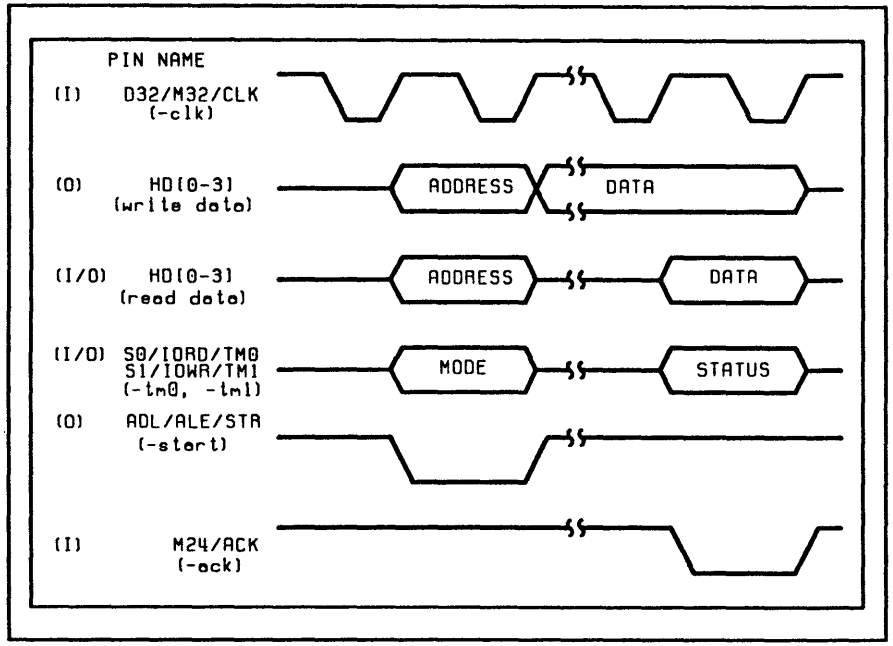


Figure 4-24. NuBus Read/Write Transaction

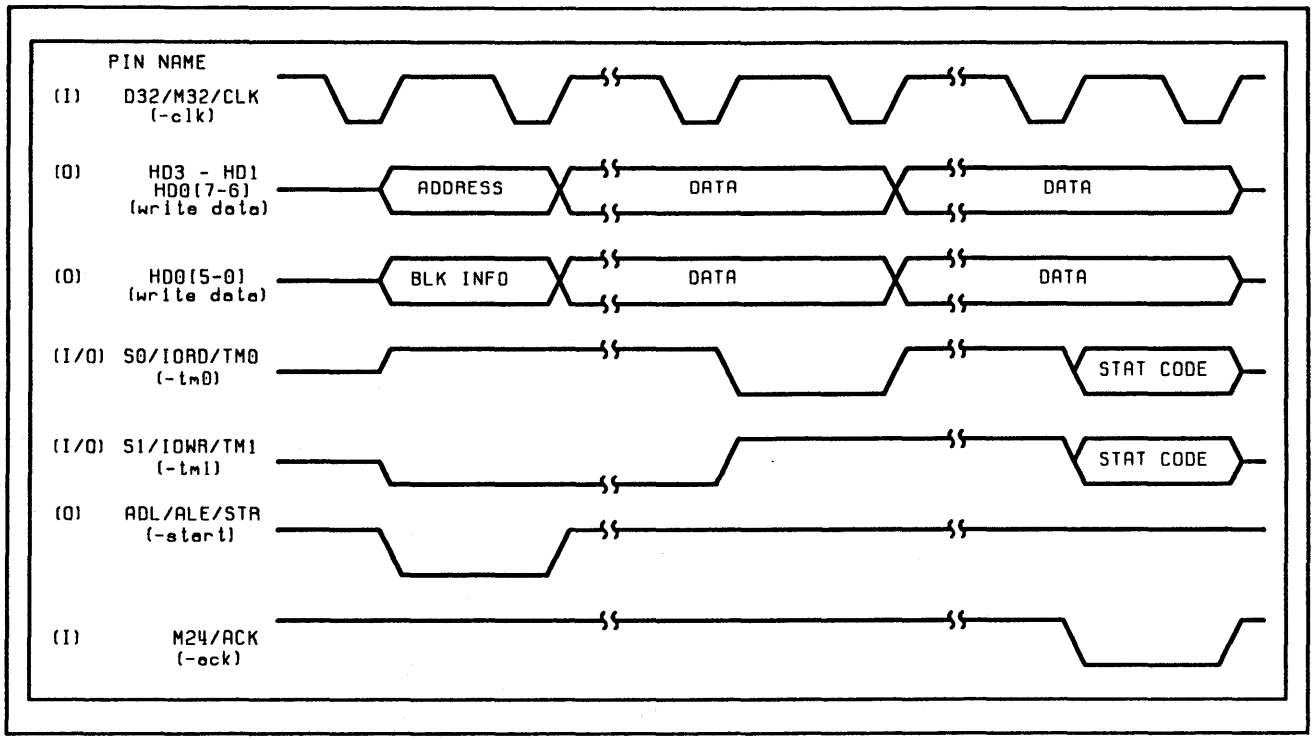


Figure 4-25. NuBus Block Write Transaction

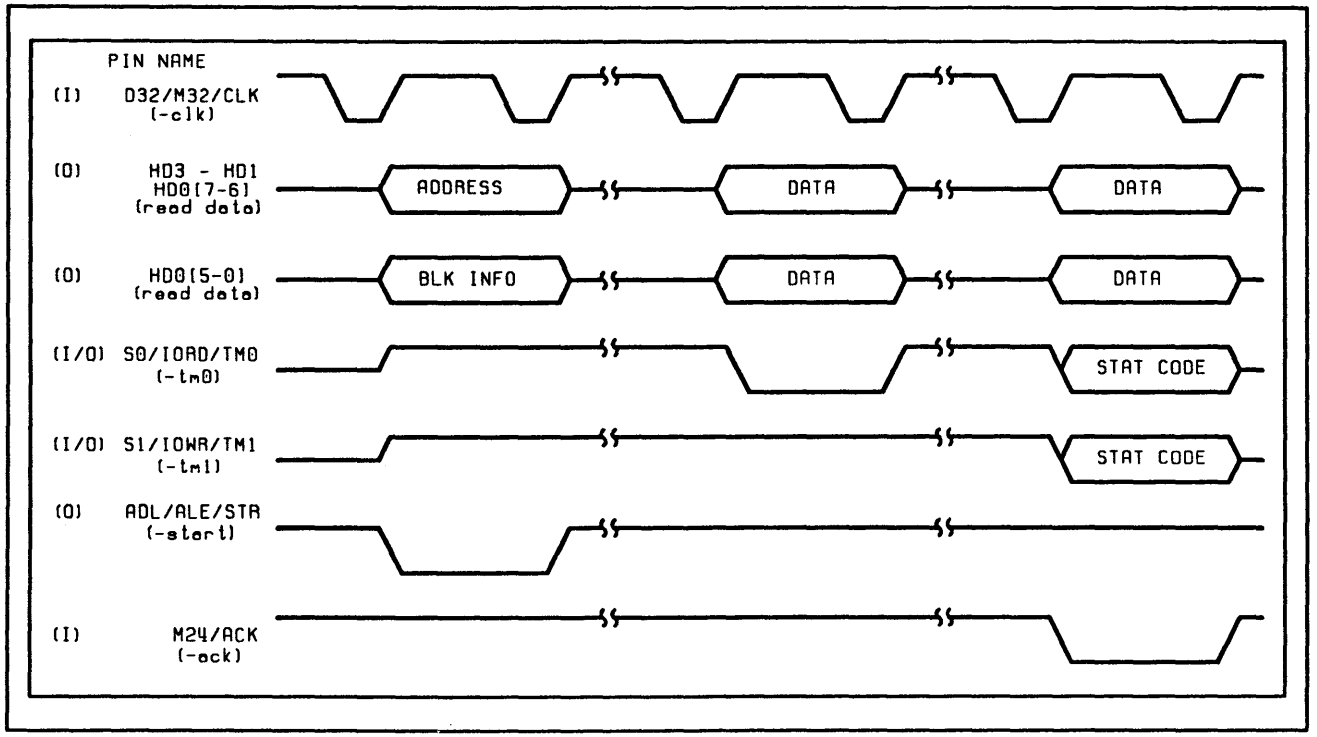
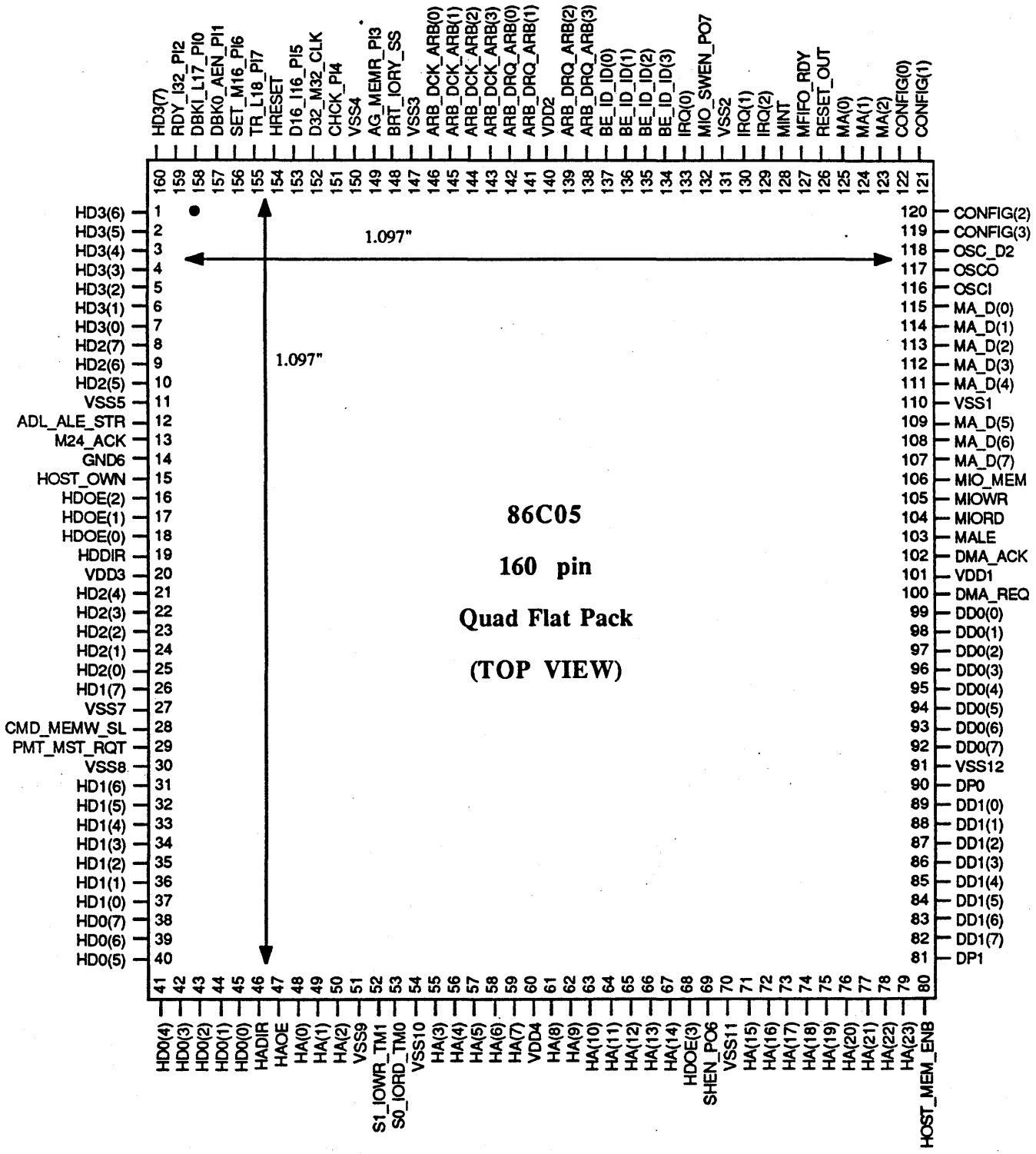


Figure 4-27. NuBus Block Read Transaction

86C05 Pinout



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