PHILIPS

Data handbook

Electronic components and materials

Semiconductors

Part 5 October 1980

Field-effect transistors

SEMICONDUCTORS

PART 5 - OCTOBER 1980

FIELD-EFFECT TRANSISTORS

DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, sub-assemblies and materials; it is made up of four series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

May 1980

ELECTRON TUBES (BLUE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	**February 1980**	**T1 02-80 (ET1a 12-75)**	**Tubes for r.f. heating**
Part 2	**April 1980**	**T2 04-80 (ET1b 08-77)**	**Transmitting tubes for communications**
Part 2b	**May 1978**	**ET2b 05-78**	**Microwave semiconductors and components** Gunn, Impatt and noise diodes, mixer and detector diodes, backward diodes, varactor diodes, Gunn oscillators, sub-assemblies, circulators and isolators.
Part 3	**June 1980**	**T3 06-80 (ET2a 11-77)**	**Klystrons, travelling-wave tubes, microwave diodes**
Part 3	**January 1975**	**ET3 01-75**	**Special Quality tubes, miscellaneous devices**
Part 4	**September 1980**	**T4 09-80 (ET2a 11-77)**	**Magnetrons**
Part 5a	**October 1979**	**ET5a 10-79**	**Cathode-ray tubes** Instrument tubes, monitor and display tubes, C.R. tubes for special applications.
Part 5b	**December 1978**	**ET5b 12-78**	**Camera tubes and accessories, image intensifiers**
Part 6	**July 1980**	**T6 07-80 (ET6 01-77)**	**Geiger-Müller tubes**
Part 7a	**March 1977**	**ET7a 03-77**	**Gas-filled tubes** Thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes.
Part 7b	**May 1979**	**ET7b 05-79**	**Gas-filled tubes** Segment indicator tubes, indicator tubes, switching diodes, dry reed contact units.
Part 8	**July 1979**	**ET8 07-79**	**Picture tubes and components** Colour TV picture tubes, black and white TV picture tubes, monitor tubes, components for colour television, components for black and white television.
Part 9	**June 1980**	**T9 06-80 (ET9 03-78)**	**Photo and electron multipliers** Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates.

SEMICONDUCTORS (RED SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	**March 1980**	**S1 03-80** **(SC1b 05-77)**	**Diodes** Small-signal germanium diodes, small-signal silicon diodes, special diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
Part 2	**May 1980**	**S2 05-80** **(SC1a 08-78)**	**Power diodes, thyristors, triacs** Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs
Part 2	**June 1979**	**SC2 06-79**	**Low-frequency power transistors**
Part 3	**January 1978**	**SC3 01-78**	**High-frequency, switching and field-effect transistors***
Part 3	**April 1980**	**S3 04-80** **(SC2 11-77, partly)** **(SC3 01-78, partly)**	**Small-signal transistors**
Part 4a	**December 1978**	**SC4a 12-78**	**Transmitting transistors and modules**
Part 4b	**September 1978**	**SC4b 09-78**	**Devices for optoelectronics** Photosensitive diodes and transistors, light-emitting diodes, photocouplers, infrared sensitive devices, photoconductive devices
Part 4c	**July 1978**	**SC4c 07-78**	**Discrete semiconductors for hybrid thick and thin-film circuits**
Part 5	**October 1980**	**S5 10-80** **(SC3 01-78)**	**Field-effect transistors**

* Wideband transistors will be transferred to SC3c. The old book SC3 01-78 should be kept until then.

INTEGRATED CIRCUITS (PURPLE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code. Books with the purple cover will replace existing red covered editions as each is revised.

Part 1	**May 1980**	**IC1 04-80 (SC5b 03-77)**	**Bipolar ICs for radio and audio equipment**
Part 2	**May 1980**	**IC2 04-80 (SC5b 03-77)**	**Bipolar ICs for video equipment**
Part 5a	**November 1976**	**SC5a 11-76**	**Professional analogue integrated circuits**
Part 4	**October 1980**	**IC4 10-80 (SC6 10-77)**	**Digital integrated circuits** LOCMOS HE4000B family
Part 6b	**August 1979**	**SC6b 08-79**	**ICs for digital systems in radio and television receivers**
Signetics integrated circuits			Bipolar and MOS memories 1979 Bipolar and MOS microprocessors 1978 Analogue circuits 1979 Logic - TTL 1978

COMPONENTS AND MATERIALS (GREEN SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	July 1979	CM1 07-79	**Assemblies for industrial use** PLC modules, high noise immunity logic FZ/30 series, NORbits 60-series, 61-series, 90-series, input devices, hybrid integrated circuits, peripheral devices
Part 3a	September 1978	CM3a 09-78	**FM tuners, television tuners, surface acoustic wave filters**
Part 3b	October 1978	CM3b 10-78	**Loudspeakers**
Part 4a	November 1978	CM4a 11-78	**Soft Ferrites** Ferrites for radio, audio and television, beads and chokes, Ferroxcube potcores and square cores, Ferroxcube transformer cores
Part 4b	February 1979	CM4b 02-79	**Piezoelectric ceramics, permanent magnet materials**
Part 6	April 1977	CM6 04-77	**Electric motors and accessories** Small synchronous motors, stepper motors, miniature direct current motors
Part 7	September 1971	CM7 09-71	**Circuit blocks** Circuit blocks 100 kHz-series, circuit blocks 1-series, circuit blocks 10-series, circuit blocks for ferrite core memory drive
Part 7a	January 1979	CM7a 01-79	**Assemblies** Circuit blocks 40-series and CSA70 (L), counter modules 50-series, input/output devices
Part 8	June 1979	CM8 06-79	**Variable mains transformers**
Part 9	August 1979	CM9 08-79	**Piezoelectric quartz devices** Quartz crystal units, temperature compensated crystal oscillators
Part 10	October 1980	C10 10-80	**Connectors**
Part 11	December 1979	CM11 12-79	**Non-linear resistors** Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
Part 12	November 1979	CM12 11-79	**Variable resistors and test switches**
Part 13	December 1979	CM13 12-79	**Fixed resistors**
Part 14	April 1980	C14 04-80 (CM2b 02-78)	**Electrolytic and solid capacitors**
Part 15	May 1980	C15 05-80 (CM2b 02-78)	**Film capacitors, ceramic capacitors, variable capacitors**

INDEX OF TYPE NUMBERS
Data Handbooks S1 to S5

The inclusion of a type number in this publication does not necessarily imply its availability.

type no.	part	section	type no.	part	section	type no.	part	section
AA119	S1	PC	BAV18	S1	WD	BB212	S1	T
AAZ13	S1	GB	BAV19	S1	WD	BB405B	S1	T
AAZ15	S1	GB	BAV20	S1	WD	BB405G	S1	T
AAZ17	S1	GB	BAV21	S1	WD	BBY31	4c	Mm
AAZ18	S1	GB	BAV45	S1	Sp	BC107	S3	Sm
BA182	S1	T	BAV70	4c	Mm	BC108	S3	Sm
BA220	S1	WD	BAV99	4c	Mm	BC109	S3	Sm
BA221	S1	WD	BAW56	4c	Mm	BC140	S3	Sm
BA223	S1	T	BAW62	S1	WD	BC141	S3	Sm
BA243	S1	T	BAX12	S1	WD	BC146	S3	Sm
BA244	S1	T	BAX12A	S1	WD	BC147	S3	Sm
BA280	S1	T	BAX13	S1	WD	BC148	S3	Sm
BA314	S1	Vrg	BAX14A	S1	WD	BC149	S3	Sm
BA315	S1	Vrg	BAX16	S1	WD	BC157	S3	Sm
BA316	S1	WD	BAX17	S1	WD	BC158	S3	Sm
BA317	S1	WD	BAX18A	S1	WD	BC159	S3	Sm
BA318	S1	WD	BB105B	S1	T	BC160	S3	Sm
BA379	S1	T	BB105G	S1	T	BC161	S3	Sm
BA482	S1	T	BB106	S1	T	BC177	S3	Sm
BA483	S1	T	BB109G	S1	T	BC178	S3	Sm
BAS11	S1	WD	BB110B	S1	T	BC179	S3	Sm
BAS16	4c	Mm	BB110G	S1	T	BC200	S3	Sm
BAT17	4c	Mm	BB119	S1	T	BC264A	S5	FET
BAT18	4c	Mm	BB204B	S1	T	BC264B	S5	FET
BAV10	S1	WD	BB204G	S1	T	BC264C	S5	FET

FET = Field-effect transistors
GB = Germanium gold bonded diodes
Mm = Discrete semiconductors for hybrid thick and thin-film circuits
PC = Germanium point contact diodes
Sm = Small-signal transistors
Sp = Special diodes
T = Tuner diodes
Vrg = Voltage regulator diodes
WD = Silicon whiskerless diodes

FET = Field-effect transistors

Mm = Discrete semiconductors for hybrid thick and thin-film circuits

type no.	part	section	type no.	part	section	type no.	part	section
BD675	SC2	P	BDT63B	SC2	P	BDX66A	SC2	P
BD676	SC2	P	BDT63C	SC2	P	BDX66B	SC2	P
BD677	SC2	P	BDT91	SC2	P	BDX66C	SC2	P
BD678	SC2	P	BDT92	SC2	P	BDX67	SC2	P
BD679	SC2	P	BDT93	SC2	P	BDX67A	SC2	P
BD680	SC2	P	BDT94	SC2	P	BDX67B	SC2	P
BD681	SC2	P	BDT95	SC2	P	BDX67C	SC2	P
BD682	SC2	P	BDT96	SC2	P	BDX77	SC2	P
BD683	SC2	P	BDV64	SC2	P	BDX78	SC2	P
BD684	SC2	P	BDV64A	SC2	P	BDX91	SC2	P
BD933	SC2	P	BDV64B	SC2	P	BDX92	SC2	P
BD934	SC2	P	BDV65	SC2	P	BDX93	SC2	P
BD935	SC2	P	BDV65A	SC2	P	BDX94	SC2	P
BD936	SC2	P	BDV65B	SC2	P	BDX95	SC2	P
BD937	SC2	P	BDX35	SC2	P	BDX96	SC2	P
BD938	SC2	P	BDX36	SC2	P	BDY20	SC2	P
BD939	SC2	P	BDX37	SC2	P	BDY90	SC2	P
BD940	SC2	P	BDX42	SC2	P	BDY91	SC2	P
BD941	SC2	P	BDX43	SC2	P	BDY92	SC2	P
BD942	SC2	P	BDX44	SC2	P	BDY93	SC2	P
BD943	SC2	P	BDX45	SC2	P	BDY94	SC2	P
BD944	SC2	P	BDX46	SC2	P	BDY96	SC2	P
BD945	SC2	P	BDX47	SC2	P	BDY97	SC2	P
BD946	SC2	P	BDX62	SC2	P	BF115	S3	Sm
BD947	SC2	P	BDX62A	SC2	P	BF180	S3	Sm
BD948	SC2	P	BDX62B	SC2	P	BF181	S3	Sm
BD949	SC2	P	BDX62C	SC2	P	BF182	S3	Sm
BD950	SC2	P	BDX63	SC2	P	BF183	S3	Sm
BD951	SC2	P	BDX63A	SC2	P	BF194	S3	Sm
BD952	SC2	P	BDX63B	SC2	P	BF195	S3	Sm
BD953	SC2	P	BDX63C	SC2	P	BF196	S3	Sm
BD954	SC2	P	BDX64	SC2	P	BF197	S3	Sm
BD955	SC2	P	BDX64A	SC2	P	BF198	S3	Sm
BD956	SC2	P	BDX64B	SC2	P	BF199	S3	Sm
BDT62	SC2	P	BDX64C	SC2	P	BF200	S3	Sm
BDT62A	SC2	P	BDX65	SC2	P	BF240	S3	Sm
BDT62B	SC2	P	BDX65A	SC2	P	BF241	S3	Sm
BDT62C	SC2	P	BDX65B	SC2	P	BF245A	S5	FET
BDT63	SC2	P	BDX65C	SC2	P	BF245B	S5	FET
BDT63A	SC2	P	BDX66	SC2	P	BF245C	S5	FET

P = Low-frequency power transistors Sm = Small-signal transistors

FET = Field-effect transistors
HFSW = High-frequency and switching transistors
Mm = Discrete semiconductors for hybrid thick and thin-film circuits
P = Low-frequency power transistors

type no.	part	section	type no.	part	section	type no.	part	section
BGY32	4a	Tra	BLX68	4a	Tra	BRY39S	S3	Sm
BGY33	4a	Tra	BLX69A	4a	Tra	BRY39T	S2/S3	Th/Sm
BGY35	4a	Tra	BLX91A	4a	Tra	BRY56	S3	Sm
BGY36	4a	Tra	BLX92A	4a	Tra	BRY61	4c	Mm
BGY37	SC3	HFSW	BLX93A	4a	Tra	BSR12;R	4c	Mm
BLV10	4a	Tra	BLX94A	4a	Tra	BSR30	4c	Mm
BLV11	4a	Tra	BLX95	4a	Tra	BSR31	4c	Mm
BLV20	4a	Tra	BLX96	4a	Tra	BSR32	4c	Mm
BLV21	4a	Tra	BLX97	4a	Tra	BSR33	4c	Mm
BLW29	4a	Tra	BLX98	4a	Tra	BSR40	4c	Mm
BLW31	4a	Tra	BLY87A	4a	Tra	BSR41	4c	Mm
BLW32	4a	Tra	BLY87C	4a	Tra	BSR42	4c	Mm
BLW33	4a	Tra	BLY88A	4a	Tra	BSR43	4c	Mm
BLW34	4a	Tra	BLY88C	4a	Tra	BSR50	S3	Sm
BLW60	4a	Tra	BLY89A	4a	Tra	BSR51	S3	Sm
BLW60C	4a	Tra	BLY89C	4a	Tra	BSR52	S3	Sm
BLW64	4a	Tra	BLY90	4a	Tra	BSR56	4c	Mm
BLW75	4a	Tra	BLY91A	4a	Tra	BSR57	4c	Mm
BLW76	4a	Tra	BLY91C	4a	Tra	BSR58	4c	Mm
BLW77	4a	Tra	BLY92A	4a	Tra	BSR60	S3	Sm
BLW78	4a	Tra	BLY92C	4a	Tra	BSR61	S3	Sm
BLW79	4a	Tra	BLY93A	4a	Tra	BSR62	S3	Sm
BLW80	4a	Tra	BLY93C	4a	Tra	BSS38	S3	Sm
BLW81	4a	Tra	BLY94	4a	Tra	BSS50	S3	Sm
BLW82	4a	Tra	BPW22	4b	PDT	BSS51	S3	Sm
BLW83	4a	Tra	BPW34	4b	PDT	BSS52	S3	Sm
BLW84	4a	Tra	BPX25	4b	PDT	BSS60	S3	Sm
BLW85	4a	Tra	BPX29	4b	PDT	BSS61	S3	Sm
BLW86	4a	Tra	BPX40	4b	PDT	BSS62	S3	Sm
BLW87	4a	Tra	BPX41	4b	PDT	BSS63;R	4c	Mm
BLW95	4a	Tra	BPX42	4b	PDT	BSS64;R	4c	Mm
BLW98	4a	Tra	BPX47A	4b	PDT	BSS68	S3	Sm
BLX13	4a	Tra	BPX70	4b	PDT	BSV15	S3	Sm
BLX13C	4a	Tra	BPX71	4b	PDT	BSV16	S3	Sm
BLX14	4a	Tra	BPX72	4b	PDT	BSV17	S3	Sm
BLX15	4a	Tra	BPX94	4b	PDT	BSV52;R	4c	Mm
BLX39	4a	Tra	BPX95B	4b	PDT	BSV64	S3	Sm
BLX65	4a	Tra	BR100/03	S2	Th	BSV78	S5	FET
BLX66	4a	Tra	BR101	S3	Sm	BSV79	S5	FET
BLX67	4a	Tra	BRY39P	S3	Sm	BSV80	S5	FET

PDT = Photodiodes or transistors
Sm = Small-signal transistors
Th = Thyristors
Tra = Transmitting transistors and modules

* = series
FET = Field-effect transistors
GB = Germanium gold bonded diodes
I = Infrared devices
LED = Light-emitting diodes
Mm = Discrete semiconductors for hybrid thick and thin-film circuits
P = Low-frequency power transistors
PC = Germanium point contact diodes
Ph = Photoconductive devices

type no.	part	section
BYX38 *	S2	R
BYX39 *	S2	R
BYX42 *	S2	R
BYX45 *	S2	R
BYX46 *	S2	R
BYX49 *	S2	R
BYX50 *	S2	R
BYX52 *	S2	R
BYX55 *	S1	R
BYX56 *	S2	R
BYX71 *	S2	R
BYX90	S1	R
BYX91 *	S1	R
BYX94	S1	R
BYX96 *	S2	R
BYX97 *	S2	R
BYX98 *	S2	R
BYX99 *	S2	R
BZV10	S1	Vrf
BZV11	S1	Vrf
BZV12	S1	Vrf
BZV13	S1	Vrf
BZV14	S1	Vrf
BZV15 *	S2	Vrg
BZV46	S1	Vrg
BZV85	S1	Vrg
BZW10	S2	TS
BZW70 *	S2	TS
BZW86 *	S2	TS
BZW91 *	S2	TS
BZX61 *	S1	Vrg
BZX70 *	S2	Vrg
BZX79 *	S1	Vrg
BZX84 *	4c	Mm
BZX87 *	S1	Vrg
BZX90	S1	Vrf
BZX91	S1	Vrf
BZX92	S1	Vrf
BZX93	S1	Vrf
BZX94	S1	Vrf
BZY88 *	S1	Vrg
BZY91 *	S2	Vrg
BZY93 *	S2	Vrg
BZY95 *	S2	Vrg
BZY96 *	S2	Vrg
CNY22	4b	PhC
CNY23	4b	PhC
CNY42	4b	PhC
CNY43	4b	PhC
CNY44	4b	PhC
CNY46	4b	PhC
CNY47	4b	PhC
CNY47A	4b	PhC
CNY48	4b	PhC
CQY11B	4b	LED
CQY11C	4b	LED
CQY24A	4b	LED
CQY46A	4b	LED
CQY47A	4b	LED
CQY49B	4b	LED
CQY49C	4b	LED
CQY50	4b	LED
CQY52	4b	LED
CQY54	4b	LED
CQY58	4b	LED
CQY88	4b	LED
CQY89	4b	LED
CQY94	4b	LED
CQY95	4b	LED
CQY96	4b	LED
CQY97	4b	LED
OA47	S1	GB
OA90	S1	PC
OA91	S1	PC
OA95	S1	PC
OA200	S1	WD
OA202	S1	WD
OM931	SC2	P
OM961	SC2	P
ORP10	4b	I
ORP13	4b	I
ORP23	4b	Ph
ORP52	4b	Ph
ORP60	4b	Ph
ORP61	4b	Ph
ORP62	4b	Ph
ORP66	4b	Ph
ORP68	4b	Ph
ORP69	4b	Ph
OSB9110	S2	St
OSB9210	S2	St
OSB9310	S2	St
OSB9410	S2	St
OSM9110	S2	St
OSM9210	S2	St
OSM9310	S2	St
OSM9410	S2	St
OSM9510	S2	St
OSM9511	S2	St
OSM9512	S2	St
OSS9110	S2	St
OSS9210	S2	St
OSS9310	S2	St
OSS9410	S2	St
PH2369	S3	Sm
RPY58A	4b	Ph
RPY71	4b	Ph
RPY76A	4b	I
RPY82	4b	Ph
RPY84	4b	Ph
RPY85	4b	Ph
RPY86	4b	I
RPY87	4b	I
RPY88	4b	I
RPY89	4b	I
SD205	S5	FET
SD210	S5	FET
SD211	S5	FET
SD212	S5	FET
SD213	S5	FET

PhC = Photocouplers
R = Rectifier diodes
Sm = Small-signal transistors
St = Rectifier stacks
Th = Thyristors
Tri = Triacs
TS = Transient suppressor diodes
Vrf = Voltage reference diodes
Vrg = Voltage regulator diodes
WD = Silicon whiskerless diodes

A = Accessories
DH = Diecast heatsinks
FET = Field-effect transistors
HE = Heatsink extrusions
HFSW = High-frequency and switching transistors
I = Infrared devices

type no.	part	section	type no.	part	section	type no.	part	section
56201c	SC2	A	56295	S2	A	56359c	SC2	A
56201d	SC2	A	56312	S2	DH	56359d	SC2	A
56201j	SC2	A	56313	S2	DH	56360a	SC2	A
56230	S2	HE	56314	S2	DH	56363	S2,SC2	A
56231	S2	HE	56315	S2	DH	56364	S2,SC2	A
56233	S2	A	56316	S2	A	56366	S2	A
56234	S2	A	56317	S2	A	56367	S2,SC2	A
56245	S3,4a	A	56318	S2	DH	56368a	SC2	A
56246	S2,S3	A	56319	S2	DH	56368b	SC2	A
56253	S2	DH	56326	SC2	A	56369	S2,SC2	A
56256	S2	DH	56333	SC2	A	56378	SC2	A
56261a	SC2	A	56334	S2	DH	56379	SC2	A
56262A	S2	A	56339	SC2	A			
56264A	S2	A	56348	S2	DH			
56268	S2	DH	56349	S2	DH			
56271	S2	DH	56350	S2	DH			
56278	S2	DH	56352	SC2	A			
56280	S2	DH	56353	SC2	A			
56290	S2	HE	56354	SC2	A			
56293	S2	HE	56359b	SC2	A			

P = Low-frequency power transistors
R = Rectifier diodes
Sm = Small-signal transistors
Tra = Transmitting transistors and modules
Vrf = Voltage reference diodes
WD = Silicon whiskerless diodes

In this alphanumeric list we present all n-channel field-effect transistors mentioned in this handbook except the Signetics D-MOS-FETS.

type number	envelope	± V_{DS} max. V	I_{DSS} mA
BC264A	TO-92 var.	30	2,0-4,5
BC264B			3,5-6,5
BC264C			5,0-8,0
BC264D			7,0-12,0
BF245A	TO-92 var.	30	2,0-6,5
BF245B			6,0-15,0
BF245C			12-25
BF246A	TO-92 var.	25	30-80
BF246B			60-140
BF246C			110-250
BF256A	TO-92 var.	30	3-7
BF256B			6-13
BF256C			11-18
BF410A	TO-92 var.	20*	0,7-3,0
BF410B			2,5-7,0
BF410C			6-12
BF410D			10-18
BF960	SOT-103	20	4-20
BF981	SOT-103	20	4-25
BFQ10	TO-71	30	0,5-10
BFQ11			
BFQ12			
BFQ13			
BFQ14			
BFQ15			
BFQ16			
BFR29	TO-72	30**	10-40
BFR84	TO-72	20	20-55
BFS21	SOT-52	30	> 1
BFS21A			
BFS28	TO-72	20	–

type number	envelope	± V_{DS} max. V	I_{DSS} mA
BFW10	TO-72	30	8-20
BFW11			4-10
BFW12	TO-72	30	1-5
BFW13			0,2-1,5
BFW61	TO-72	25	2-20
BSV78	TO-18	40	> 50
BSV79			> 20
BSV80			> 10
BSV81	TO-72	30**	–
2N3822	TO-72	50	2-10
2N3823	TO-72	30	4-20
2N3966	TO-72	30	> 2
2N4091	TO-18	40	> 30
2N4092			> 15
2N4093			> 8
2N4391	TO-18	40	> 50
2N4392			> 25
2N4393			> 5
2N4856	TO-18	40	> 50
2N4857		40	> 20
2N4858		40	> 8
2N4859		30	> 50
2N4860		30	> 20
2N4861		30	> 8

* Asymmetrical.
** V_{DB}.

CONVERSION LIST

N-channel junction FETS available in SOT-23 envelopes. For full data please refer to Handbook SC4c 07-78 to be superseded by Handbook S7 in the second half of 1980.

type number	marking code	nearest convential type	V_{DS} V	I_{DSS} mA
BF510	S6	BF410A	20	0,7-3,0
BF511	S7	BF410B	20	2,5-7,0
BF512	S8	BF410C	20	6-12
BF513	S9	BF410D	20	10-18
BFR30	M1	BFW11	± 25	4-10
BFR31	M2	BFW12	± 25	1-5
BFT46	M3	BFW13	± 25	0,2-1,5
BSR56	M4	2N4856	± 40	50
BSR57	M5	2N4857	± 40	20-100
BSR58	M6	2N4858	± 40	8-80

N-channel junction field-effect transistors

type number	envelope	RATINGS			CHARACTERISTICS							remarks
		$\pm V_{DS}$	P_{tot} at T_{amb}		$-I_{GSS}$ max.	I_{DSS} min.-max.	$-V_{(P)GS}$ max.	$\lvert y_{fs} \rvert$ min. f = 1 kHz	C_{rs} typ.	F typ.	V_n max.	
		V	mW	°C	nA	mA	V	mA/V	pF	dB	μV	
BC264A BC264B BC264C BC264D	TO-92 var.	30	300	25	10	2,0-4,5 3,5-6,5 5,0-8,0 7,0-12,0	> 0,5	2,5 3,0 3,5 4,0	1,2	0,5	–	hi-fi amplifiers and a.f. equipment
BF245A BF245B BF245C	TO-92 var.	30	300	75	5	2,0-6,5 6-15 12-25	8,0	3,0-6,5	1,1	1,5	–	d.c., l.f. and h.f. amp.
BF246A BF246B BF246C	TO-92	25	300	75	5	30-80 60-140 110-250	0,6-14,5	8	3,5	–	–	v.h.f. and u.h.f. amp. general purpose sw.
BF256A BF256B BF256C	TO-92 var.	30	300	75	5	3-7 6-13 11-18	–	4,5	0,7	7,5	–	v.h.f. and u.h.f. appl.
BF410A BF410B BF410C BF410D	TO-92 var.	20*	300	75	10	0,7-3,0 2,5-7,0 6-12 10-18	typ. 0,8 typ. 1,5 typ. 2,2 typ. 3,0	2,5 4,0 6,0 7,0	0,3	1,5	–	r.f. stages f.m. portables r.f. stages car radios r.f. stages mains radios mixer stages
BFW10 BFW11	TO-72	30	300	25	0,1	8-20 4-10	8 6	3,5-6,5 3,0-6,5	0,6	< 2,5		broad band up to 300 MHz and differential amp.
BFW12 BFW13	TO-72	30	150	110	0,1	1-5 0,2-1,5	2,5 1,2	2,0 1,0	< 0,8	–	0,5	low current-low voltage applications
BFW61	TO-72	25	300	25	1,0	2-20	8	2,0-6,5	< 2,0	–	–	general purpose amp.
2N3822	TO-72	50	300	25	0,1	2-10	6	3,0-6,5	< 3,0	< 5	–	general purpose h.f. amp.
2N3823	TO-72	30	300	25	0,5	4-20	8	3,5-6,5	< 2,0	< 2,5	–	industrial i.f./r.f. amp.

* Asymmetrical.

N-channel MOS-FETS

type number	envelope	RATINGS				CHARACTERISTICS							remarks
		V_{DB} V_{SB}	V_{DS}	P_{tot} at T_{amb}		± I_{GSS} max.	± I_{G1-SS} ± I_{G2-SS} max.	I_{DSS}	$-V_{(P)GS}$ $-V_{(P)G1-S}$	$\|y_{fs}\|$ f = 1 kHz min.	C_{rs} typ.	F max.	
		V	V	mW	°C	pA	nA	mA	V	mA/V	fF	dB	
BF960*	SOT-103	–	20	225	75	–	100	4-20	< 3,5	9	25	2,5	dual gate
BF981*	SOT-103	–	20	225	75	–	100	4-25	< 2,5	10	25	2,0	dual gate
BFR29	TO-72	30	–	200	25	10	–	10-40	< 4	6	< 700	5,0	insulated gate
BFR84*	TO-72	–	20	300	25	–	10	20-55	1,5-3,8	12	30	3,0	dual gate
BFS28	TO-72	–	20	200	25	–	1	–	–	8	25	4,0	dual gate

N-channel junction field-effect transistors for switching

type number	envelope	RATINGS			CHARACTERISTICS						
		± V_{DS}	P_{tot} at T_{amb} (T_{case})		$-I_{GSS}$ (I_{SGO}) max.	I_{DSS} min.	$-V_{(P)GS}$ max.	$r_{ds\ on}$ max.	C_{rs} max.	t_{on} max.	t_{off} max.
		V	mW	°C	pA	mA	V	Ω	pF	ns	ns
BSV78						50	11	25		10	10
BSV79	TO-18	40	350	25	250	20	7,0	40	5	18	16
BSV80						10	5,0	60		30	32
2N3966	TO-72	30	300	25	100	2	6	220	1,5	120	100
2N4091						30	10	30		25	40
2N4092	TO-18	40	1800	(25)	200	15	7,0	50	5	35	60
2N4093						8	5,0	80		60	80
2N4391						50	10	30			20
2N4392	TO-18	40	1800	(25)	100	25	5,0	60	3,5	15	35
2N4393						5	3,0	100			50

* Protected against excessive input voltage surges.

N-channel junction field-effect transistors for switching

type number	envelope	RATINGS			CHARACTERISTICS						
		$\pm V_{DS}$	P_{tot} at T_{amb}		$-I_{GSS}$	I_{DSS}	$-V_{(P)GS}$	$r_{ds\ on}$	C_{rs}	t_{on}	t_{off}
					max.	min.	max.	max.	max.	max.	max.
		V	mW	°C	pA	mA	V	Ω	pF	ns	ns
2N4856	TO-18	40	360	25	250	50	10	25	8	9	25
2N4857		40				20	6	40		10	50
2N4858		40				8	4	60		20	100
2N4859		30				50	10	25		9	25
2N4860		30				20	6	40		10	50
2N4861		30				8	4	60		20	100

N-channel MOS-FET for switching

type number	envelope	RATINGS			CHARACTERISTICS					
		V_{DB} V_{SB}	P_{tot} at T_{amb}		$\pm I_{GSS}$	I_{DSX} I_{SDX}	$r_{ds\ on}$	r_{DSoff}	C_{rs}	C_{rd}
					max.	max.	max.	min.	max.	max.
		V	mW	°C	pA	nA	Ω	GΩ	pF	pF
BSV81	TO-72	30	200	25	10	1	100	10	0,5	0,5

N-channel junction field-effect transistors for differential amplifiers

type number	envelope	RATINGS					CHARACTERISTICS							
		individual transistor			total device		individual transistor			total device				
		$\pm V_{DS}$	P_{tot} at T_{amb}		P_{tot} at T_{amb}		$-I_{GSS}$	I_{DSS}	$-V_{(P)GS}$	$\lvert\Delta V_{GS}\rvert$	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	CMRR
			mW	°C	mW	°C	max. pA	mA	max. V	max. mV	max. μV/K	max. Ω	max. μV/V	min. dB
BFQ10										5	5	6	10	100
BFQ11										10	5	6	30	90
BFQ12										10	10	12	30	90
BFQ13	TO-71	30	250	75	250	75	100	0,5-10	3,5	10	20	12	30	90
BFQ14										15	20	12	30	90
BFQ15										20	40	20	30	90
BFQ16										50	50	30	100	80
BFS21	SOT-52	30	300	25	30	100	–	> 1	6	20	75	15	1000	60
BFS21A										10	40	7,5	500	66

CECC APPROVED TYPES

Products approved to CECC, available on request.

BSV78
BSV79
BSV80
} also available to CECC 50 012-011

BSV81 also available to CECC 50 012-010

GENERAL

Type designation
Rating systems
Letter symbols
s-parameters

PRO ELECTRON TYPE DESIGNATION CODE FOR SEMICONDUCTOR DEVICES

This type designation code applies to discrete semiconductor devices – as opposed to integrated circuits –, multiples of such devices and semiconductor chips.

A basic type number consists of:

TWO LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST LETTER

The first letter gives information about the material used for the active part of the devices.

A. GERMANIUM or other material with band gap of 0,6 to 1,0 eV.
B. SILICON or other material with band gap of 1,0 to 1,3 eV.
C. GALLIUM-ARSENIDE or other material with band gap of 1,3 eV or more.
R. COMPOUND MATERIALS (e.g. Cadmium-Sulphide).

SECOND LETTER

The second letter indicates the function for which the device is primarily designed.

A. DIODE; signal, low power
B. DIODE; variable capacitance
C. TRANSISTOR; low power, audio frequency ($R_{th\ j\text{-}mb} > 15\ ^{o}C/W$)
D. TRANSISTOR; power, audio frequency ($R_{th\ j\text{-}mb} \leqslant 15\ ^{o}C/W$)
E. DIODE; tunnel
F. TRANSISTOR; low power, high frequency ($R_{th\ j\text{-}mb} > 15\ ^{o}C/W$)
G. MULTIPLE OF DISSIMILAR DEVICES – MISCELLANEOUS; e.g. oscillator
H. DIODE; magnetic sensitive
L. TRANSISTOR; power, high frequency ($R_{th\ j\text{-}mb} \leqslant 15\ ^{o}C/W$)
N. PHOTO-COUPLER
P. RADIATION DETECTOR; e.g. high sensitivity phototransistor
Q. RADIATION GENERATOR; e.g. light-emitting diode (LED)
R. CONTROL AND SWITCHING DEVICE; e.g. thyristor, low power ($R_{th\ j\text{-}mb} > 15\ ^{o}C/W$)
S. TRANSISTOR; low power, switching ($R_{th\ j\text{-}mb} > 15\ ^{o}C/W$)
T. CONTROL AND SWITCHING DEVICE; e.g. thyristor, power ($R_{th\ j\text{-}mb} \leqslant 15\ ^{o}C/W$)
U. TRANSISTOR; power, switching ($R_{th\ j\text{-}mb} \leqslant 15\ ^{o}C/W$)
X. DIODE: multiplier, e.g. varactor, step recovery
Y. DIODE; rectifying, booster
Z. DIODE; voltage reference or regulator (transient suppressor diode, with third letter W)

SERIAL NUMBER

Three figures, running from 100 to 999, for devices primarily intended for consumer equipment.
One letter (Z, Y, X, etc.) and two figures, running from 10 to 99, for devices primarily intended for industrial/professional equipment.
This letter has no fixed meaning except W, which is used for transient suppressor diodes.

VERSION LETTER

It indicates a minor variant of the basic type either electrically or mechanically. The letter never has a fixed meaning, except letter R, indicating reverse voltage, e.g. collector to case or anode to stud.

SUFFIX

Sub-classification can be used for devices supplied in a wide range of variants called associated types. Following sub-coding suffixes are in use:

1. VOLTAGE REFERENCE and VOLTAGE REGULATOR DIODES: *ONE LETTER and ONE NUMBER*
   The LETTER indicates the nominal tolerance of the Zener (regulation, working or reference) voltage
   A. 1% (according to IEC 63: series E96)
   B. 2% (according to IEC 63: series E48)
   C. 5% (according to IEC 63: series E24)
   D. 10% (according to IEC 63: series E12)
   E. 20% (according to IEC 63: series E6)
   The number denotes the typical operating (Zener) voltage related to the nominal current rating for the whole range.
   The letter 'V' is used instead of the decimal point.

2. TRANSIENT SUPPRESSOR DIODES: *ONE NUMBER*
   The NUMBER indicates the maximum recommended continuous reversed (stand-off) voltage V_R. The letter 'V' is used as above.

3. CONVENTIONAL and CONTROLLED AVALANCHE RECTIFIER DIODES and THYRISTORS: *ONE NUMBER*
   The NUMBER indicates the rated maximum repetitive peak reverse voltage (V_{RRM}) or the rated repetitive peak off-state voltage (V_{DRM}), whichever is the lower. Reversed polarity is indicated by letter R, immediately after the number.

4. RADIATION DETECTORS: *ONE NUMBER,* preceded by a hyphen (–)
   The NUMBER indicates the depletion layer in μm. The resolution is indicated by a version LETTER.

5. ARRAY OF RADIATION DETECTORS and GENERATORS: *ONE NUMBER,* preceded by a stroke (/).
   The NUMBER indicates how many basic devices are assembled into the array.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

LETTER SYMBOLS FOR TRANSISTORS AND SIGNAL DIODES

based on IEC Publication 148

LETTER SYMBOLS FOR CURRENTS, VOLTAGES AND POWERS

Basic letters

The basic letters to be used are:

I, i = current
V, v = voltage
P, p = power.

Lower-case basic letters shall be used for the representation of instantaneous values which vary with time.
In all other instances upper-case basic letters shall be used.

Subscripts

A, a	Anode terminal
(AV), (av)	Average value
B, b	Base terminal, for MOS devices: Substrate
(BR)	Breakdown
C, c	Collector terminal
D, d	Drain terminal
E, e	Emitter terminal
F, f	Forward
G, g	Gate terminal
K, k	Cathode terminal
M, m	Peak value
O, o	As third subscript: The terminal not mentioned is open circuited
R, r	As first subscript: Reverse. As second subscript: Repetitive. As third subscript: With a specified resistance between the terminal not mentioned and the reference terminal.
(RMS), (rms)	R.M.S. value
S, s	As first or second subscript: Source terminal (for FETS only) As second subscript: Non-repetitive (not for FETS) As third subscript: Short circuit between the terminal not mentioned and the reference terminal
X, x	Specified circuit
Z, z	Replaces R to indicate the actual working voltage, current or power of voltage reference and voltage regulator diodes.

Note: No additional subscript is used for d.c. values.

Upper-case subscripts shall be used for the indication of:

a) continuous (d.c.) values (without signal)
Example I_B

b) instantaneous total values
Example i_B

c) average total values
Example $I_{B(AV)}$

d) peak total values
Example I_{BM}

e) root-mean-square total values
Example $I_{B(RMS)}$

Lower-case subscripts shall be used for the indication of values applying to the varying component alone:

a) instantaneous values
Example i_b

b) root-mean-square values
Example $I_{b(rms)}$

c) peak values
Example I_{bm}

d) average values
Example $I_{b(av)}$

Note: If more than one subscript is used, subscript for which both styles exist shall either be all upper-case or all lower-case.

Additional rules for subscripts

Subscripts for currents

Transistors: If it is necessary to indicate the terminal carrying the current, this should be done by the first subscript (conventional current flow from the external circuit into the terminal is positive).

Examples: I_B, i_B, i_b, I_{bm}

Diodes: To indicate a forward current (conventional current flow into the anode terminal) the subscript F or f should be used; for a reverse current (conventional current flow out of the anode terminal) the subscript R or r should be used.

Examples: I_F, I_R, i_F, $I_{f(rms)}$

Subscripts for voltages

Transistors: If it is necessary to indicate the points between which a voltage is measured, this should be done by the first two subscripts. The first subscript indicates the terminal at which the voltage is measured and the second the reference terminal or the circuit node. Where there is no possibility of confusion, the second subscript may be omitted.

Examples: V_{BE}, v_{BE}, v_{be}, V_{bem}

Diodes: To indicate a forward voltage (anode positive with respect to cathode), the subscript F or f should be used; for a reverse voltage (anode negative with respect to cathode) the subscript R or r should be used.

Examples: V_F, V_R, v_F, V_{rm}

Subscripts for supply voltages or supply currents

Supply voltages or supply currents shall be indicated by repeating the appropriate terminal subscript.

Examples: V_{CC}, I_{EE}

Note: If it is necessary to indicate a reference terminal, this should be done by a third subscript

Example : V_{CCE}

Subscripts for devices having more than one terminal of the same kind

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal followed by a number; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples: I_{B2} = continuous (d.c.) current flowing into the second base terminal

V_{B2-E} = continuous (d.c.) voltage between the terminals of second base and emitter

Subscripts for multiple devices

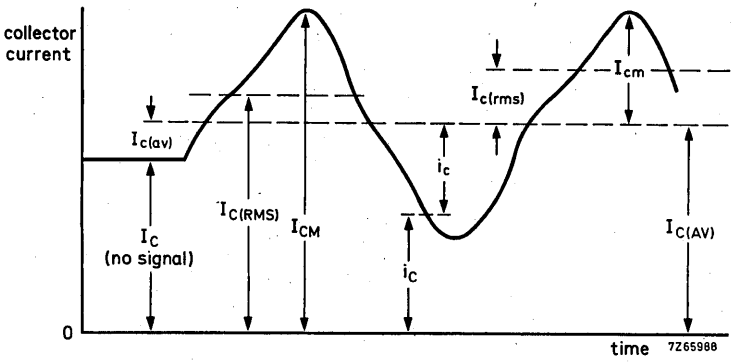
For multiple unit devices, the subscripts are modified by a number preceding the letter subscript; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples: I_{2C} = continuous (d.c.) current flowing into the collector terminal of the second unit

V_{1C-2C} = continuous (d.c.) voltage between the collector terminals of the first and the second unit.

Application of the rules

The figure below represents a transistor collector current as a function of time. It consists of a continuous (d.c.) current and a varying component.



LETTER SYMBOLS FOR ELECTRICAL PARAMETERS

Definition

For the purpose of this Publication, the term "electrical parameter" applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

Basic letters

The following is a list of the most important basic letters used for electrical parameters of semiconductor devices.

B, b = susceptance; imaginary part of an admittance

C = capacitance

G, g = conductance; real part of an admittance

H, h = hybrid parameter

L = inductance

R, r = resistance; real part of an impedance

X, x = reactance; imaginary part of an impedance

Y, y = admittance;

Z, z = impedance;

Upper-case letters shall be used for the representation of:

a) electrical parameters of external circuits and of circuits in which the device forms only a part;

b) all inductances and capacitances.

Lower-case letters shall be used for the representation of electrical parameters inherent in the device (with the exception of inductances and capacitances).

Subscripts

General subscripts

The following is a list of the most important general subscripts used for electrical parameters of semiconductor devices:

F, f = forward; forward transfer
I, i (or 1) = input
L, l = load
O, o (or 2) = output
R, r = reverse; reverse transfer
S, s = source

Examples: Z_S, h_f, h_F

The upper-case variant of a subscript shall be used for the designation of static (d.c.) values.

Examples : h_{FE} = static value of forward current transfer ratio in common-emitter configuration (d.c. current gain)

R_E = d.c. value of the external emitter resistance.

Note: The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript shall be used for the designation of small-signal values.

Examples: h_{fe} = small-signal value of the short-circuit forward current transfer ratio in common-emitter configuration

$Z_e = R_e + jX_e$ = small-signal value of the external impedance

Note: If more than one subscript is used, subscripts for which both styles exist shall either be all upper-case or all lower-case

Examples: h_{FE}, y_{RE}, h_{fe}

Subscripts for four-pole matrix parameters

The first letter subscript (or double numeric subscript) indicates input, output, forward transfer or reverse transfer

Examples: h_i (or h_{11})
h_o (or h_{22})
h_f (or h_{21})
h_r (or h_{12})

A further subscript is used for the identification of the circuit configuration. When no confusion is possible, this further subscript may be omitted.

Examples: h_{fe} (or h_{21e}), h_{FE} (or h_{21E})

Distinction between real and imaginary parts

If it is necessary to distinguish between real and imaginary parts of electrical parameters, no additional subscripts should be used. If basic symbols for the real and imaginary parts exist, these may be used.

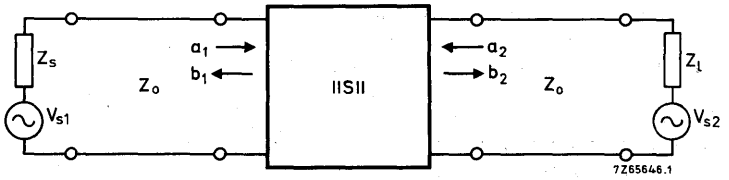
Examples: $Z_i = R_i + jX_i$
$y_{fe} = g_{fe} + jb_{fe}$

If such symbols do not exist or if they are not suitable, the following notation shall be used:

Examples: Re (h_{ib}) etc. for the real part of h_{ib}
Im (h_{ib}) etc. for the imaginary part of h_{ib}

SCATTERING PARAMETERS

In distinction to the conventional h, y and z-parameters, s-parameters relate to travelling wave conditions. The figure below shows a two-port network with the incident and reflected waves a_1, b_1, a_2 and b_2.



$$a_1 = \frac{V_{i1}}{\sqrt{Z_o}} \qquad a_2 = \frac{V_{i2}}{\sqrt{Z_o}} \qquad 1)$$

$$b_1 = \frac{V_{r1}}{\sqrt{Z_o}} \qquad b_2 = \frac{V_{r2}}{\sqrt{Z_o}}$$

Z_o = characteristic impedance of the transmission line in which the two-port is connected.

V_i = incident voltage

V_r = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$
$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, r for 12, f for 21 and o for 22, it follows that:

$$s_i = s_{11} = \frac{b_1}{a_1}\Big|_{a_2 = 0}$$
$$s_r = s_{12} = \frac{b_1}{a_2}\Big|_{a_1 = 0}$$
$$s_f = s_{21} = \frac{b_2}{a_1}\Big|_{a_2 = 0}$$
$$s_o = s_{22} = \frac{b_2}{a_2}\Big|_{a_1 = 0}$$

1) The squares of these quantities have the dimension of power.

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$ = Input reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the input, under the conditions $Z_l = Z_o$ and $V_{s2} = 0$.

$s_r = s_{12}$ = Reverse transmission coefficient.
The complex ratio of the generated wave at the input and the incident wave at the output, under the conditions $Z_s = Z_o$ and $V_{s1} = 0$.

$s_f = s_{21}$ = Forward transmission coefficient.
The complex ratio of the generated wave at the output and the incident wave at the input, under the conditions $Z_l = Z_o$ and $V_{s2} = 0$

$s_o = s_{22}$ = Output reflection coefficient.
The complex ratio of the reflected wave and the incident wave at the output, under the conditions $Z_s = Z_o$ and $V_{s1} = 0$.

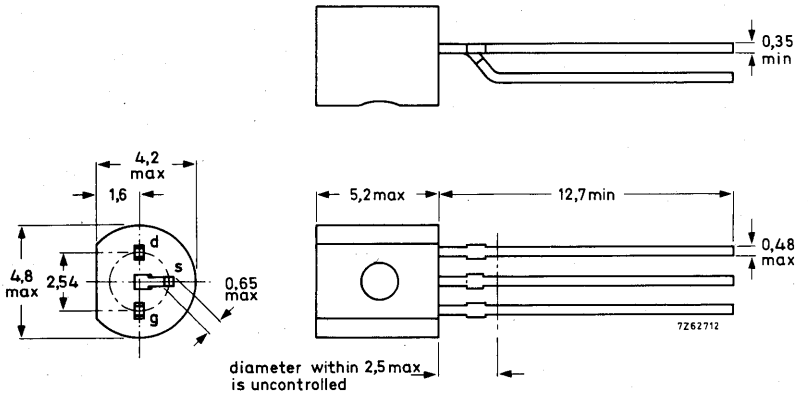
N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for hi-fi amplifiers and other audio frequency equipment.

QUICK REFERENCE DATA				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	150	°C
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 12	mA
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	$\lvert y_{fs} \rvert$	typ.	3,5	mA/V
Noise figure at V_{DS} = 15 V; V_{GS} = 0 f = 1 kHz; R_G = 1 MΩ	F	<	2	dB

MECHANICAL DATA Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Current				
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Temperatures				
Storage temperature	T_{stg}		−65 to +150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

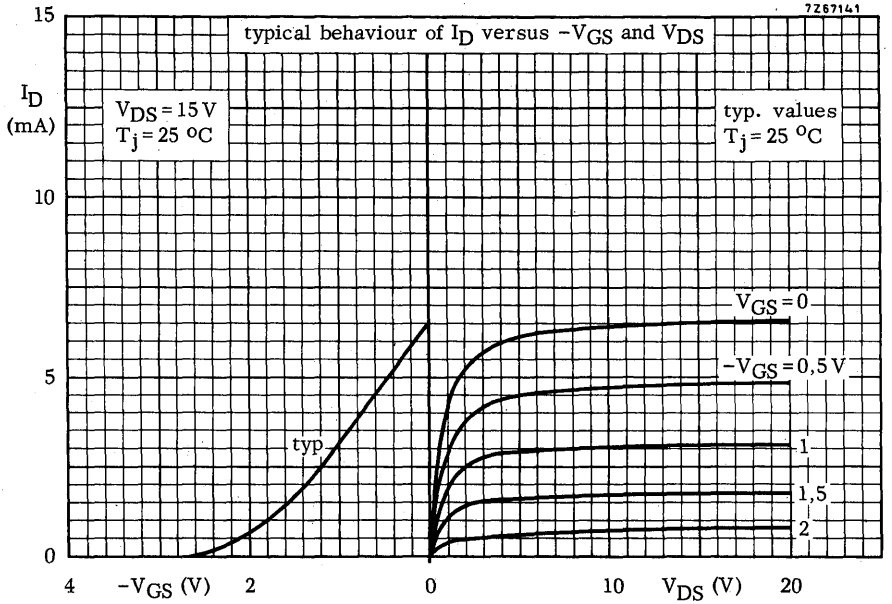
From junction to ambient in free air	$R_{th\ j-a}$	=	0,42	°C/mW

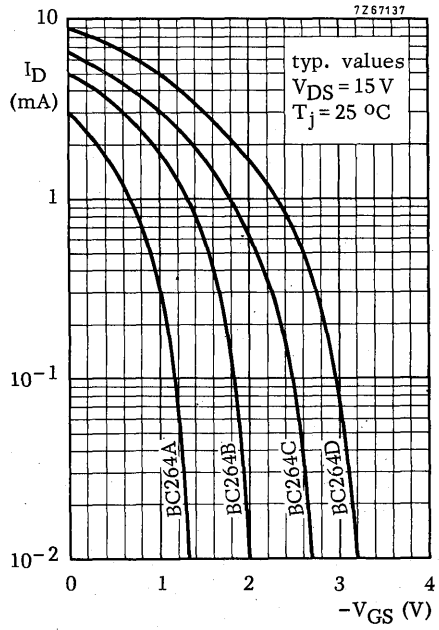
CHARACTERISTICS

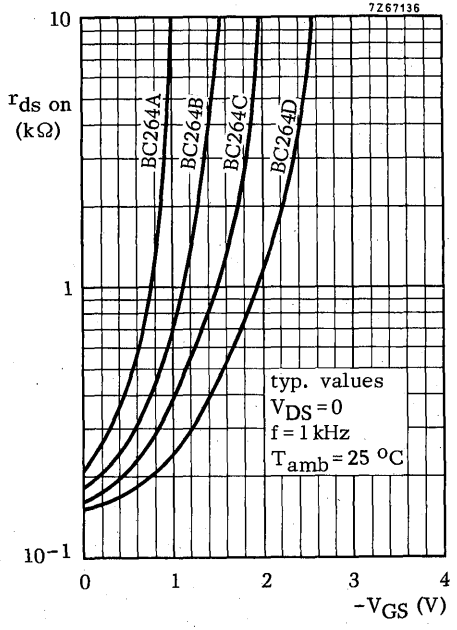
T_j = 25 °C unless otherwise specified

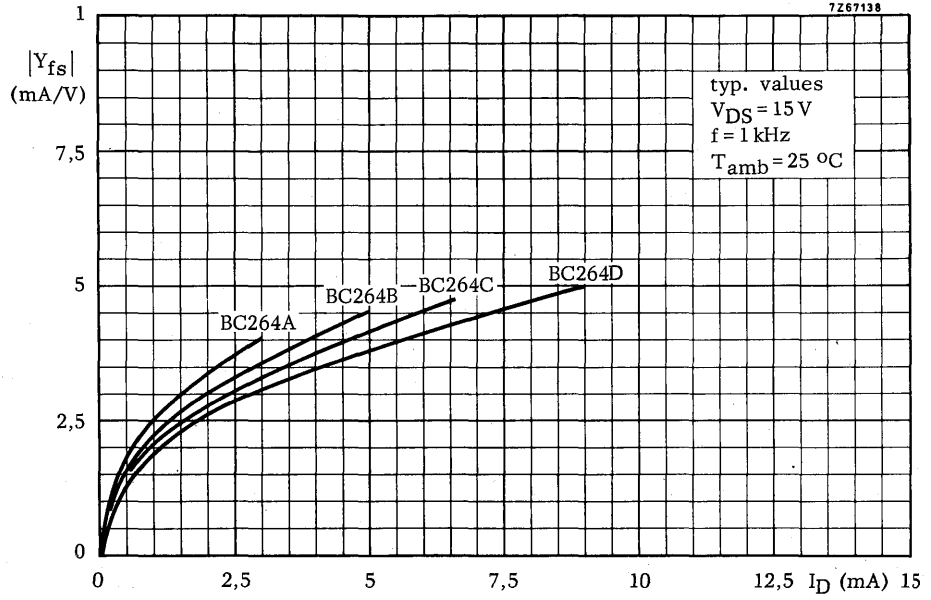
			BC264A	B	C	D	
Gate cut-off current							
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Drain current [1]							
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	2,0	3,5	5,0	7,0	mA
		<	4,5	6,5	8,0	12,0	mA
Gate-source breakdown voltage							
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30	30	30	30	V
Gate-source voltage							
I_D = 200 µA ; V_{DS} = 15 V	$-V_{GS}$	>	0,4	0,4	0,4	0,4	V
I_D = 1,0 mA; V_{DS} = 15 V	$-V_{GS}$	>	0,2	–	–	–	V
		<	1,2	–	–	–	V
I_D = 1,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	0,4	–	–	V
		<	–	1,4	–	–	V
I_D = 2,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	0,5	–	V
		<	–	–	1,5	–	V
I_D = 3,5 mA; V_{DS} = 15 V	$-V_{GS}$	>	–	–	–	0,6	V
		<	–	–	–	1,6	V
Gate-source cut-off voltage							
I_D = 10 nA ; V_{DS} = 15 V	$-V_{(P)GS}$	>	0,5	0,5	0,5	0,5	V
y-parameters at T_{amb} = 25 °C							
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz							
Transfer admittance	$\lvert y_{fs} \rvert$	>	2,5	3,0	3,5	4,0	mA/V
V_{DS} = 15 V; $-V_{GS}$ = 1 V; f = 1 MHz							
Input capacitance	C_{is}	typ.			4,0		pF
Feedback capacitance	C_{rs}	typ.			1,2		pF
Output capacitance	C_{os}	typ.			1,6		pF
Noise figure at f = 1 kHz; R_G = 1 MΩ							
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C	F	typ.			0,5		dB
		<			2		dB
Equivalent noise voltage at T_{amb} = 25 °C							
V_{DS} = 15 V; V_{GS} = 0; f = 10 Hz	$V_n/\sqrt{B}$	typ.			40		$nV/\sqrt{Hz}$

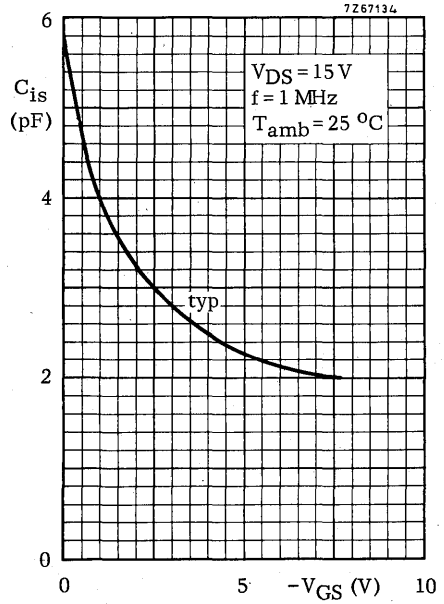
1) Measured under pulse conditions.

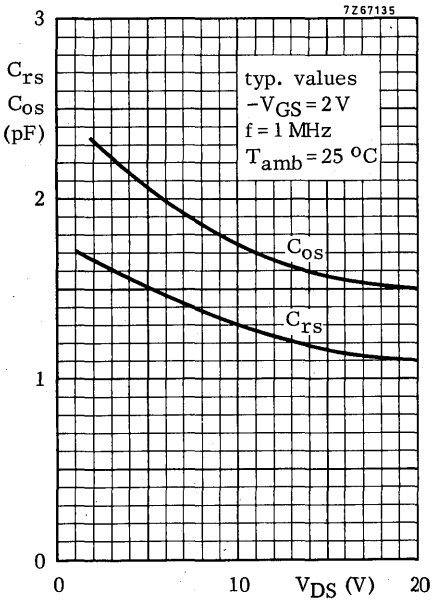

7Z67141
typical behaviour of I_D versus $-V_{GS}$ and V_{DS}
I_D (mA)
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1
1,5
2
typ
15
10
5
0
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

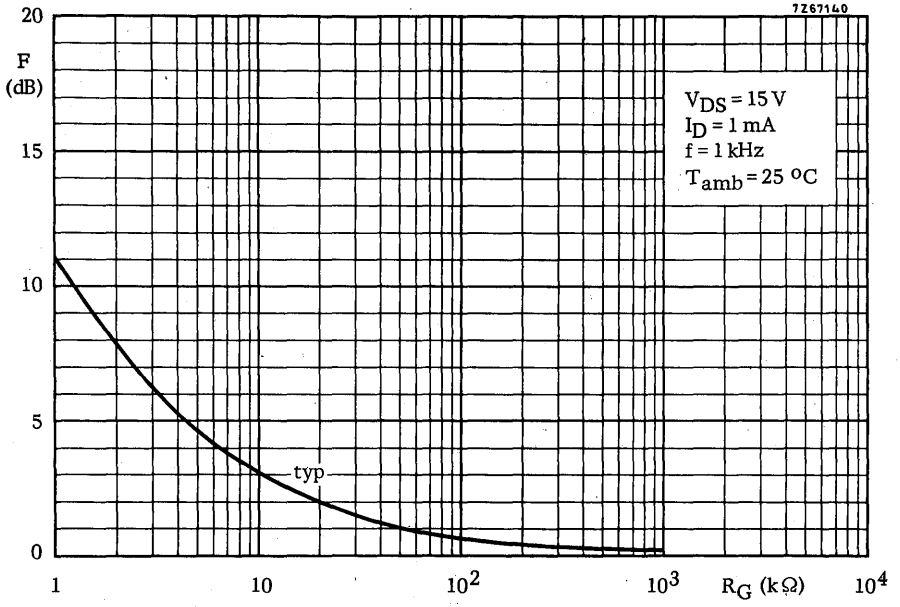

7Z67137
I_D (mA)
typ. values
V_{DS} = 15 V
T_j = 25 °C
BC264A
BC264B
BC264C
BC264D
10
1
10^{-1}
10^{-2}
0
1
2
3
4
$-V_{GS}$ (V)


7Z67136
$r_{ds\ on}$ (kΩ)
BC264A
BC264B
BC264C
BC264D
typ. values
V_{DS} = 0
f = 1 kHz
T_{amb} = 25 °C
10
1
10^{-1}
0
1
2
3
4
$-V_{GS}$ (V)


7Z67138
|Yfs| (mA/V)
typ. values
VDS = 15 V
f = 1 kHz
Tamb = 25 °C
BC264A
BC264B
BC264C
BC264D
1
7,5
5
2,5
0
0
2,5
5
7,5
10
12,5
ID (mA)
15


7Z67134
Cis (pF)
VDS = 15 V
f = 1 MHz
Tamb = 25 °C
typ
6
4
2
0
0
5
-VGS (V)
10


7Z67135
Crs Cos (pF)
typ. values
-VGS = 2 V
f = 1 MHz
Tamb = 25 °C
Cos
Crs
3
2
1
0
0
10
VDS (V)
20


7Z67140
20
F
(dB)
15
10
5
0
1
10
10²
10³
10⁴
R_G (kΩ)
typ
V_DS = 15 V
I_D = 1 mA
f = 1 kHz
T_amb = 25 °C

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

General purpose symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for applications in l.f. and d.c. amplifiers, and in h.f. amplifiers.

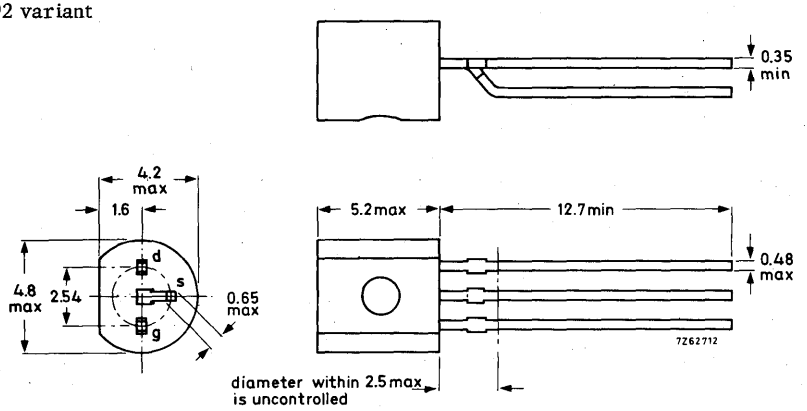
QUICK REFERENCE DATA

Drain-source voltage			$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)			$-V_{GSO}$	max.	30	V
Total power dissipation up to T_{amb} = 75 °C			P_{tot}	max.	300	mW
			BF245A	B	C	
Drain current		>	2	6,0	12	mA
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	<	6,5	15,0	25	mA
Gate-source cut-off voltage						
I_D = 10 nA; V_{DS} = 15 V			$-V_{(P)GS}$	0,5 to 8,0		V
Feedback capacitance						
V_{DS} = 20 V; $-V_{GS}$ = 1 V			C_{rs}	typ.	1,1	pF
Transfer admittance (common source)						
V_{DS} = 15 V; V_{GS} = 0			$\|y_{fs}\|$	3,0 to 6,5		mA/V

MECHANICAL DATA

Dimensions in mm

TO-92 variant



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages					
Drain-source voltage	$\pm V_{DS}$	max.	30	V	
Drain-gate voltage (open source)	V_{DGO}	max.	30	V	
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V	
Currents					
Drain current	I_D	max.	25	mA	
Gate current	I_G	max.	10	mA	
Power dissipation					
Power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW	
up to T_{amb} = 90 °C	P_{tot}	max.	300	mW	1)
Temperatures					
Storage temperature	T_{stg}	−65 to +150		°C	
Junction temperature	T_j	max.	150	°C	

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	0,25	°C/mW
From junction to ambient	$R_{th\ j\text{-}a}$	=	0,20	°C/mW 1)

1) Transistor mounted on printed circuit board, max. lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

		BF245A	B	C	
Gate cut-off current					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	< 5	5	5	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	< 0,5	0,5	0,5	µA
Drain current [1]					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 2	6,0	12	mA
		< 6,5	15,0	25	mA
Gate-source breakdown voltage					
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$	> 30	30	30	V
Gate-source voltage					
I_D = 200 µA; V_{DS} = 15 V	$-V_{GS}$	> 0,4	1,6	3,2	V
		< 2,2	3,8	7,5	V
Gate-source cut-off voltage					
I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$	0,5 to 8,0			V

y-parameters at T_{amb} = 25 °C (common source)

V_{DS} = 15 V; V_{GS} = 0					
f = 1 kHz	Transfer admittance	$\|y_{fs}\|$	3,0 to 6,5		mA/V
	Output admittance	$\|y_{os}\|$	typ.	25	µA/V
f = 200 MHz	Input conductance	g_{is}	typ.	250	µA/V
	Reverse transfer admittance	$\|y_{rs}\|$	typ.	1,4	mA/V
	Transfer admittance	$\|y_{fs}\|$	typ.	6	mA/V
	Output conductance	g_{os}	typ.	40	µA/V
V_{DS} = 20 V; $-V_{GS}$ = 1 V					
f = 1 MHz	Input capacitance	C_{is}	typ.	4,0	pF
	Feedback capacitance	C_{rs}	typ.	1,1	pF
	Output capacitance	C_{os}	typ.	1,6	pF

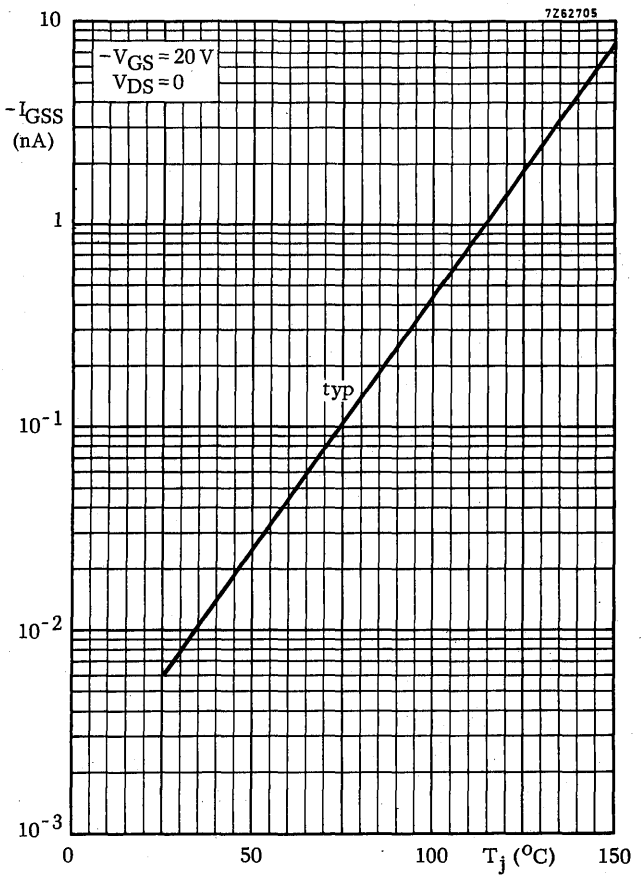
Cut-off frequency [2]

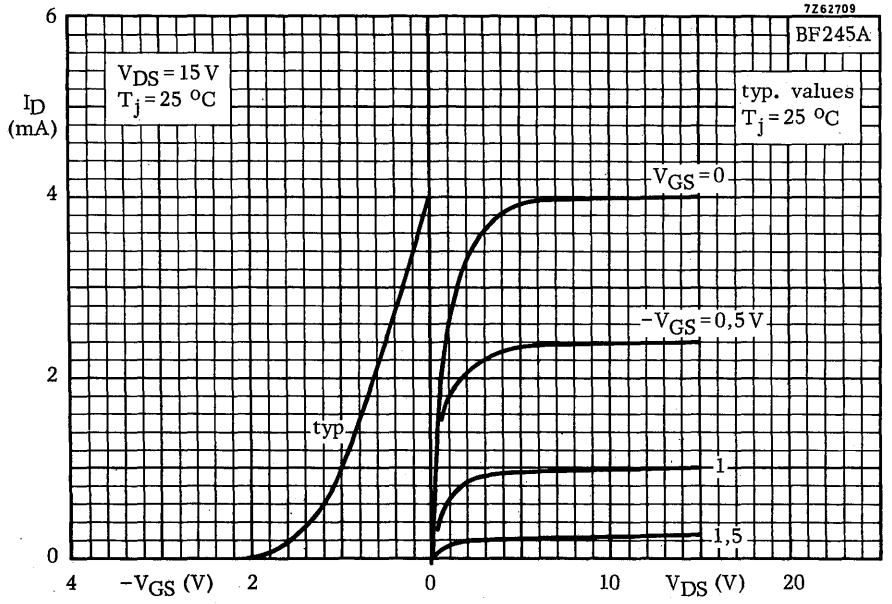
V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.	700	MHz

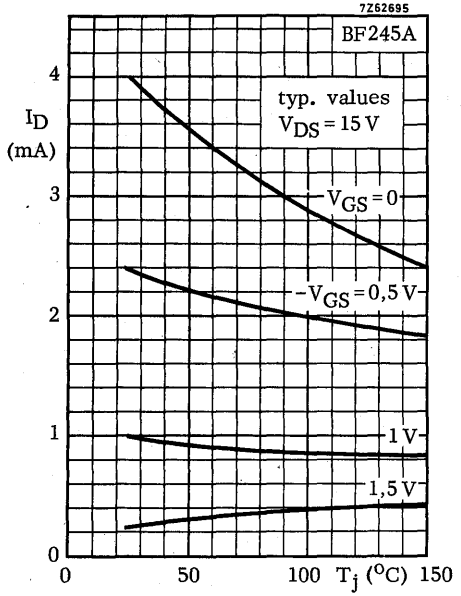
Noise figure at f = 100 MHz; R_G = 1 kΩ (common source)

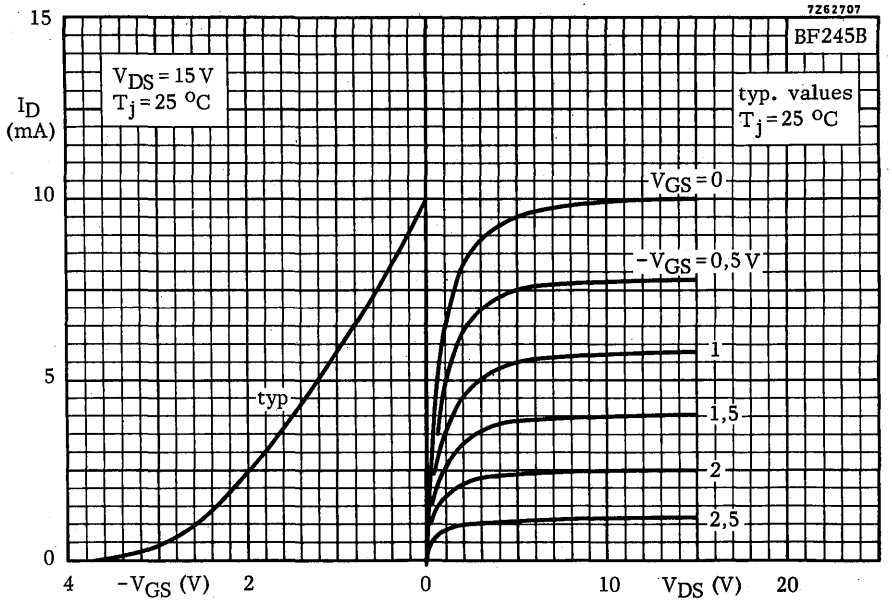
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C input tuned to minimum noise	F	typ.	1,5	dB

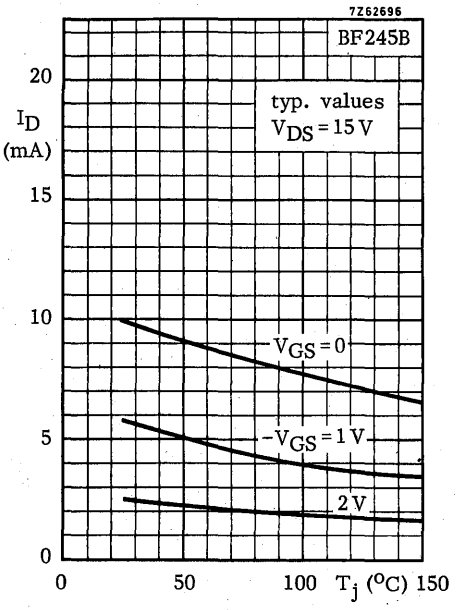
1) Measured under pulse condition: t_p = 300 µs; $\delta \leq 0,02$
2) The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

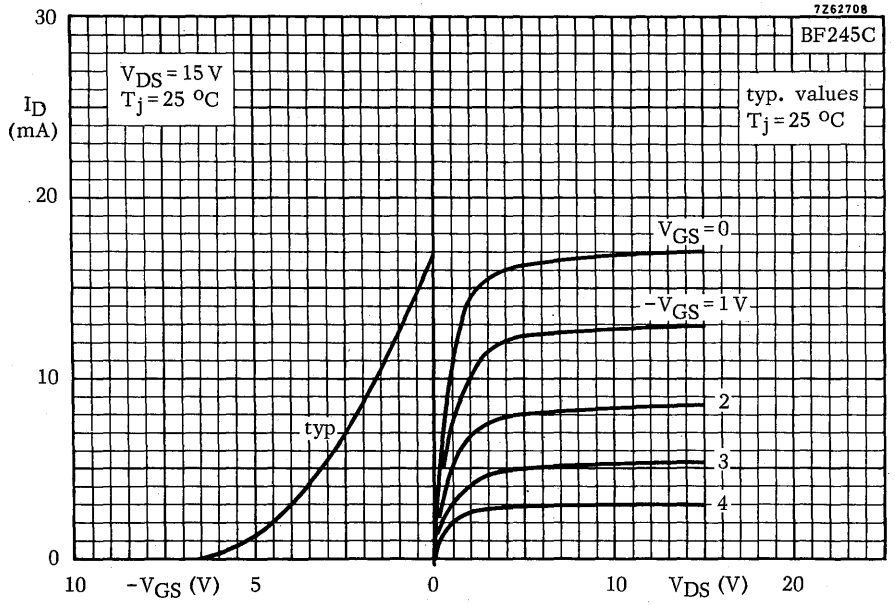

7Z62705
10
$-V_{GS} = 20\ V$
$V_{DS} = 0$
$-I_{GSS}$ (nA)
1
typ
10^{-1}
10^{-2}
10^{-3}
0
50
100
T_j (^oC)
150

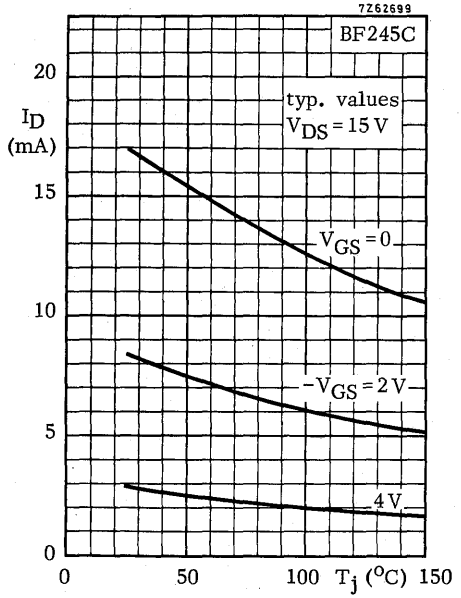

7Z62709
BF245A
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1
1,5
typ
6
4
2
0
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

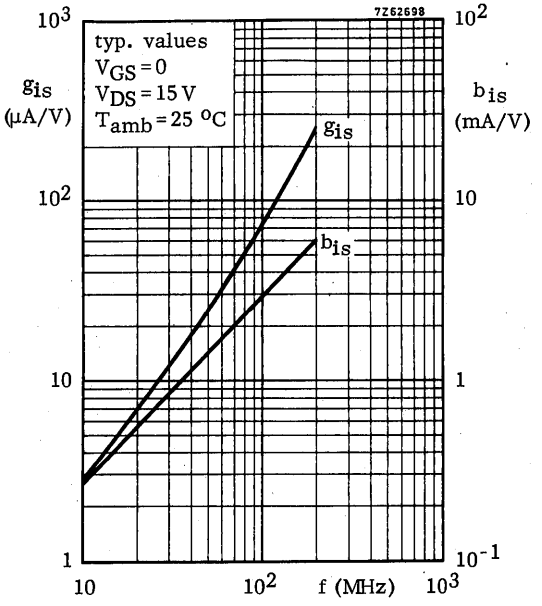

7Z62695
BF245A
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
4
3
2
1
0
0
50
100
T_j (°C)
150

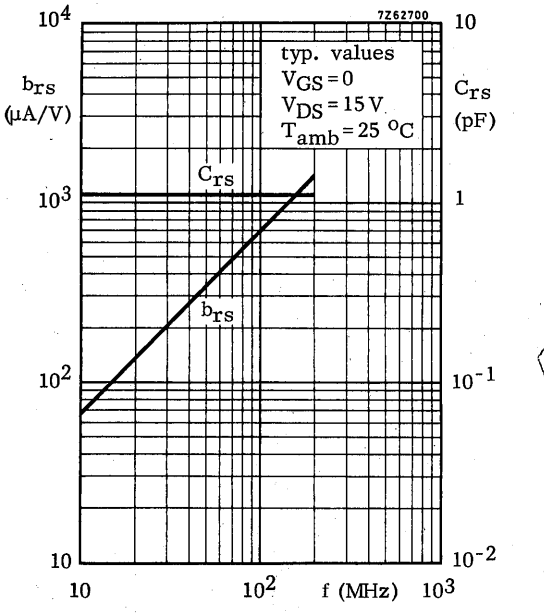

7Z62707
BF245B
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
15
10
5
0
$-V_{GS}$ = 0
$-V_{GS}$ = 0,5 V
1
1,5
2
2,5
typ
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

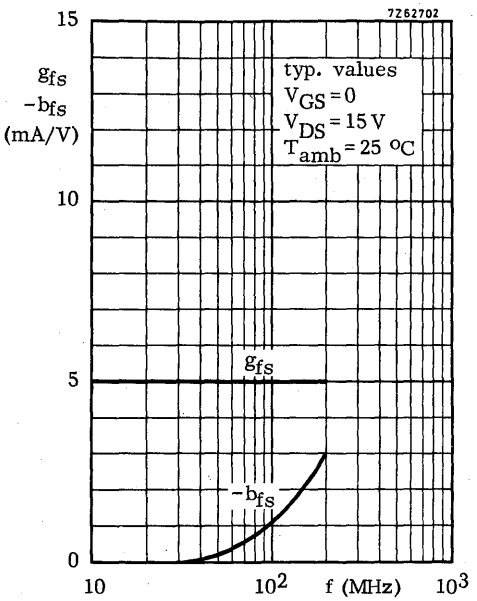

7Z62696
BF245B
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
0
50
100
T_j (°C)
150

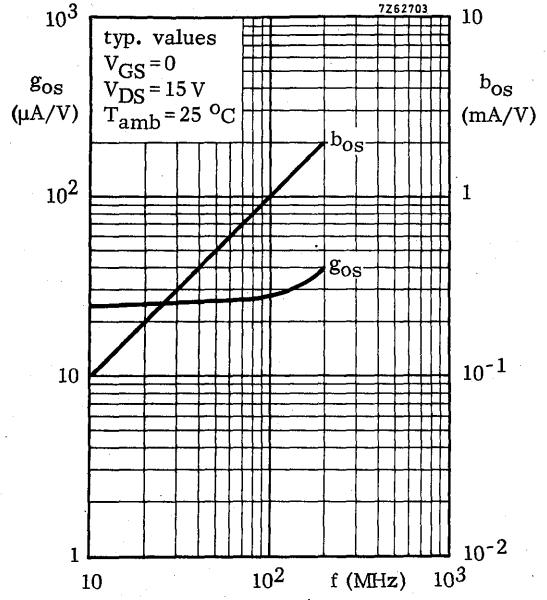

7Z62708
BF245C
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
30
20
10
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2
3
4
typ
10
$-V_{GS}$ (V)
5
0
10
V_{DS} (V)
20

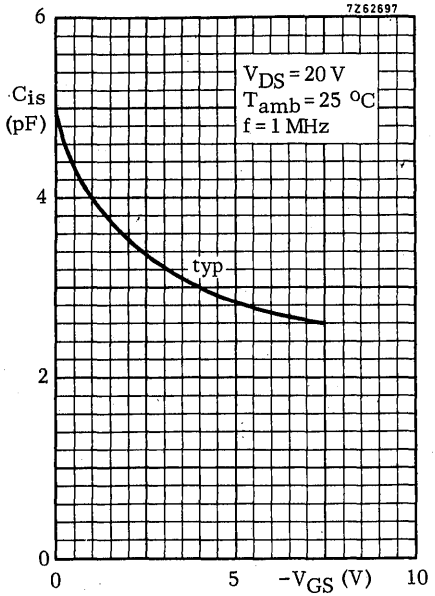

7Z62699
BF245C
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 2 V
4 V
0
50
100
T_j (°C)
150

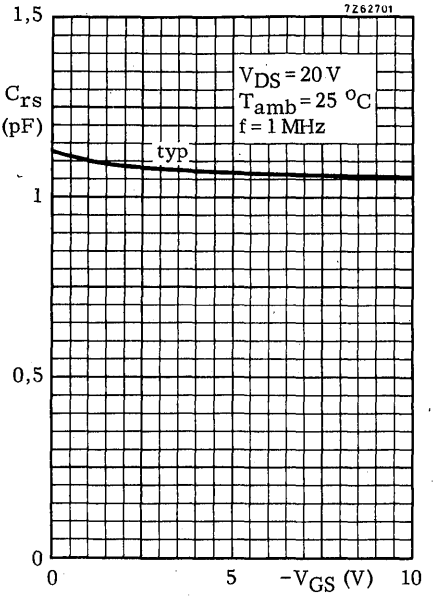

7Z62698
typ. values
$V_{GS} = 0$
$V_{DS} = 15\,V$
$T_{amb} = 25\,^{o}C$
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

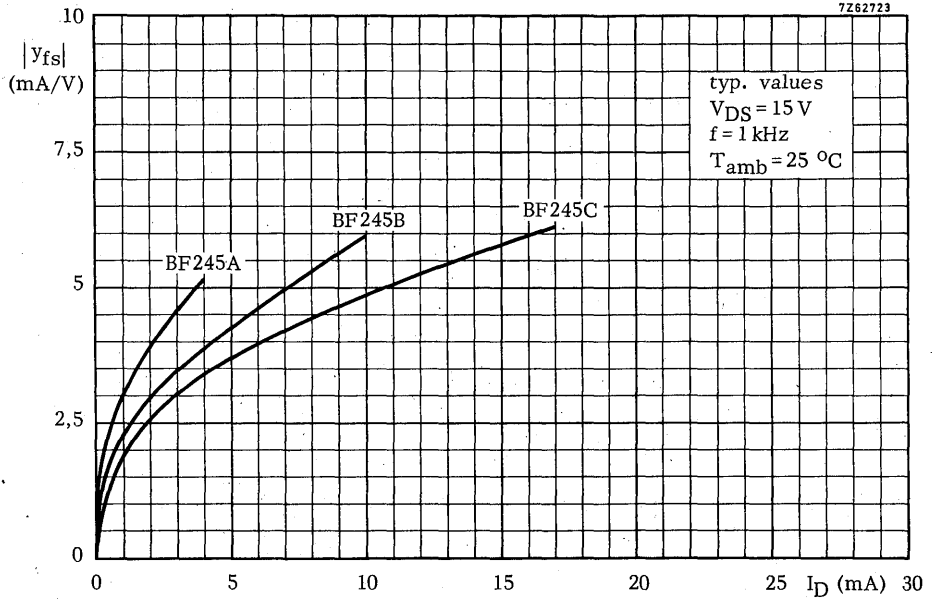

7Z62700
typ. values
$V_{GS} = 0$
$V_{DS} = 15\,V$
$T_{amb} = 25\,^{o}C$
b_{rs} (μA/V)
C_{rs} (pF)
C_{rs}
b_{rs}
10^4
10^3
10^2
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

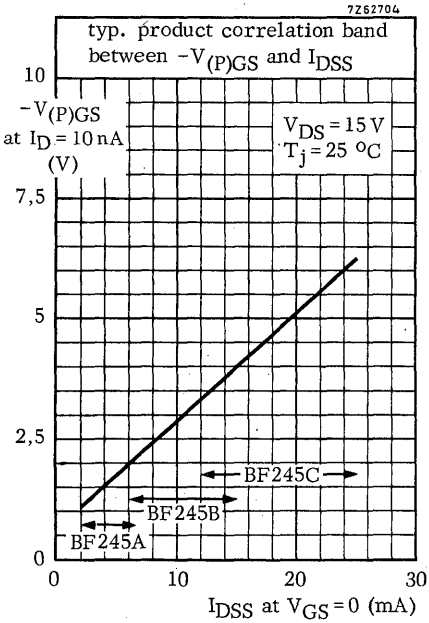

7Z62702
15
g_{fs}
$-b_{fs}$
(mA/V)
10
5
0
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
g_{fs}
$-b_{fs}$
10
10^2
f (MHz)
10^3

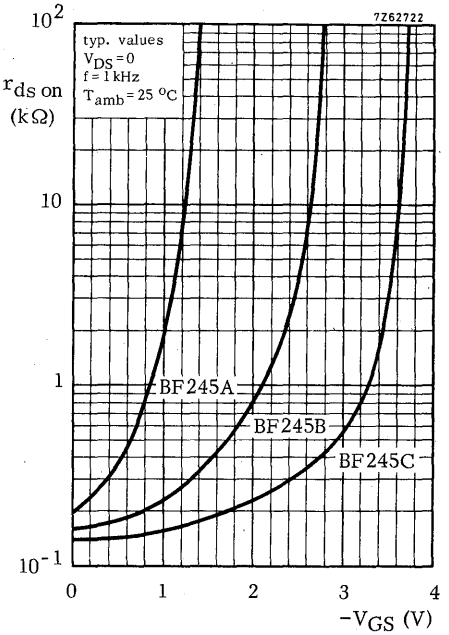

7Z62703
10^3
g_{os}
(μA/V)
10^2
10
1
typ. values
$V_{GS} = 0$
$V_{DS} = 15$ V
$T_{amb} = 25$ °C
b_{os}
g_{os}
10
b_{os}
(mA/V)
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

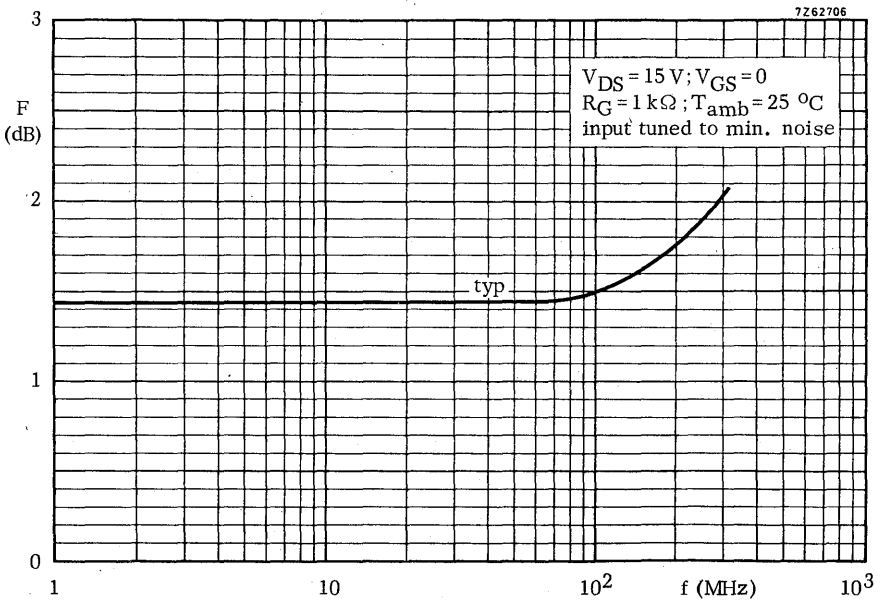

7Z62697
6
4
2
0
C_{is} (pF)
V_{DS} = 20 V
T_{amb} = 25 °C
f = 1 MHz
typ
0
5
$-V_{GS}$ (V)
10


7Z62701
1,5
1
0,5
0
C_{rs} (pF)
V_{DS} = 20 V
T_{amb} = 25 °C
f = 1 MHz
typ
0
5
$-V_{GS}$ (V)
10


7Z62723
10
7,5
5
2,5
0
$|y_{fs}|$ (mA/V)
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
BF245A
BF245B
BF245C
0
5
10
15
20
25
I_D (mA)
30


7Z62704
typ. product correlation band between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ at $I_D = 10$ nA (V)
$V_{DS} = 15$ V
$T_j = 25$ °C
10
7,5
5
2,5
0
BF245C
BF245B
BF245A
0
10
20
30
I_{DSS} at $V_{GS} = 0$ (mA)


7Z62722
typ. values
$V_{DS} = 0$
f = 1 kHz
$T_{amb} = 25$ °C
$r_{ds\ on}$ (kΩ)
10^2
10
1
10^{-1}
BF245A
BF245B
BF245C
0
1
2
3
4
$-V_{GS}$ (V)


7Z62706
$V_{DS} = 15$ V; $V_{GS} = 0$
$R_G = 1$ kΩ; $T_{amb} = 25$ °C
input tuned to min. noise
F (dB)
3
2
1
0
typ
1
10
10^2
f (MHz)
10^3

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical n-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for v.h.f. and u.h.f. amplifiers, mixers, and general purpose switching.

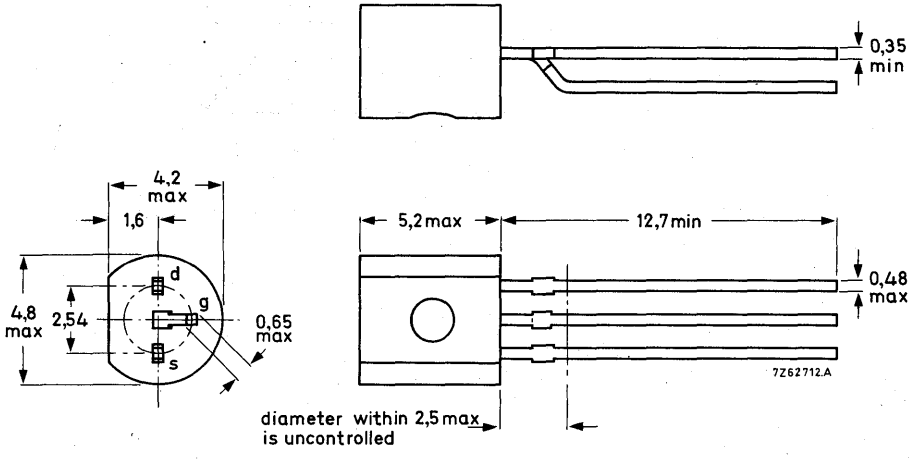
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25		V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300		mW
		BF246A	**B**	**C**	
Drain current					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 30	60	110	mA
		< 80	140	250	mA
Gate-source cut-off voltage					
I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$	0,6 to 14,5			V
Feedback capacitance at f = 1 kHz					
I_D = 10 mA; V_{DS} = 15 V	C_{rs}	typ.	3,5		pF
Transfer admittance (common source)					
I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz	$\|y_{fs}\|$	>	8		mA/V

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	25 V
Drain-gate voltage (open source)	V_{DGO}	max.	25 V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25 V
Gate current	I_G	max.	10 mA
Total power dissipation			
up to T_{amb} = 75 °C	P_{tot}	max.	300 mW
up to T_{amb} = 90 °C*	P_{tot}	max.	300 mW
Storage temperature	T_{stg}	−65 to +	150 °C
Junction temperature	T_j	max.	150 °C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	250 K/W
From junction to ambient*	$R_{th\ j\text{-}a}$	=	200 K/W

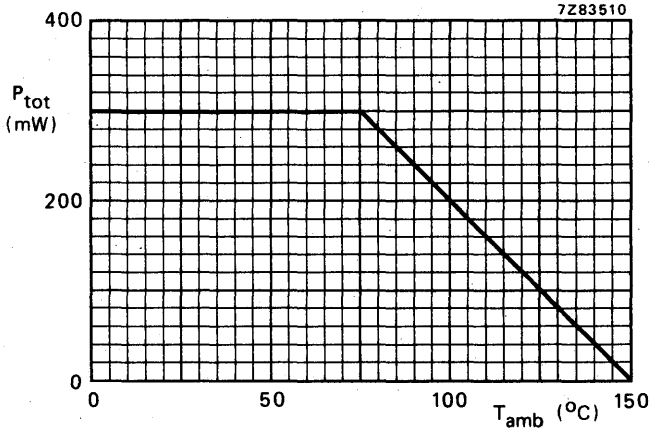


Fig. 2 Maximum permissible power dissipation as a function of ambient temperature.

* Transistor mounted on printed-circuit board, maximum lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

CHARACTERISTICS

T_{amb} = 25 °C

			BF246A	B	C	
Gate cut-off current						
$-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	<	5	5	5	nA
Drain current*						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	30	60	110	mA
		<	80	140	250	mA
Gate-source breakdown voltage						
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	25	25	25	V
Gate-source voltage						
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$	>	1,5	3,0	5,5	V
		<	4,0	7,0	12,0	V
	$-V_{GS}$		0,5 to 14			V
Gate-source cut-off voltage						
I_D = 10 nA; V_{DS} = 15 V	$-V_{(P)GS}$		0,6 to 14,5			V
y-parameters (common source)						
I_D = 10 mA; V_{DS} = 15 V; f = 1 kHz						
Transfer admittance	$\lvert y_{fs} \rvert$	>		8		mA/V
		typ.		23		mA/V
Feedback capacitance	C_{rs}	typ.		3,5		pF
I_D = 10 mA; V_{DS} = 15 V; f = 1 MHz						
Input capacitance	C_{is}	typ.		15		pF
Output capacitance	C_{os}	typ.		15		pF
Cut-off frequency**						
V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.		450		MHz

DEVELOPMENT SAMPLE DATA

* Measured under pulse conditions: t_p = 300 μs; $\delta \leqslant 0{,}02$.

** The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

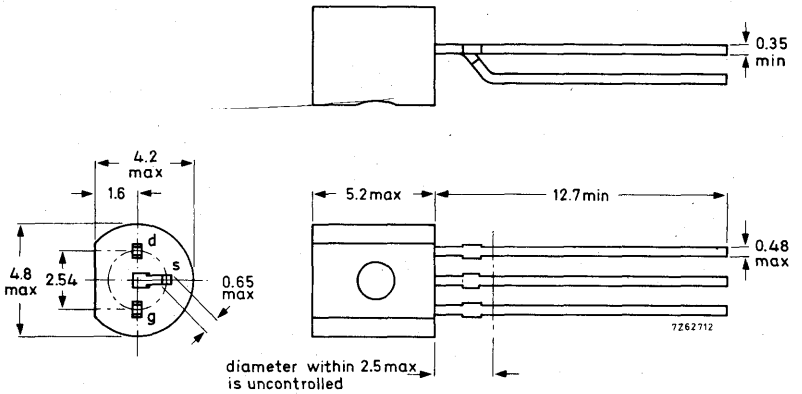
N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Symmetrical N-channel planar epitaxial junction field-effect transistors in a plastic TO-92 variant; intended for v.h.f. and u.h.f. applications.

QUICK REFERENCE DATA					
Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300		mW
		BF256A	B	C	
Drain current					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 3	6	11	mA
		< 7	13	18	mA
Feedback capacitance at f = 1 MHz					
V_{DS} = 20 V; $-V_{GS}$ = 1 V; T_{amb} = 25 °C	C_{rs}	typ.	0,7		pF
Transfer admittance (common source)					
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz; T_{amb} = 25 °C	$\lvert y_{fs} \rvert$	>	4,5		mA/V
Power gain at f = 800 MHz					
V_{DS} = 15 V; R_S = 47 Ω	G_p	typ.	11		dB

MECHANICAL DATA Dimensions in mm

TO-92 variant



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages					
Drain-source voltage	$\pm V_{DS}$	max.	30	V	
Drain-gate voltage (open source)	V_{DGO}	max.	30	V	
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V	
Current					
Gate current	I_G	max.	10	mA	
Power dissipation					
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW	
up to T_{amb} = 90 °C	P_{tot}	max.	300	mW	1)
Temperatures					
Storage temperature	T_{stg}	−65 to +150		°C	
Junction temperature	T_j	max.	150	°C	

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	0,25	°C/mW
From junction to ambient	$R_{th\ j\text{-}a}$	=	0,20	°C/mW 1)

1) Transistor mounted on printed circuit board, max. lead length 3 mm, mounting pad for drain lead minimum 10 mm x 10 mm.

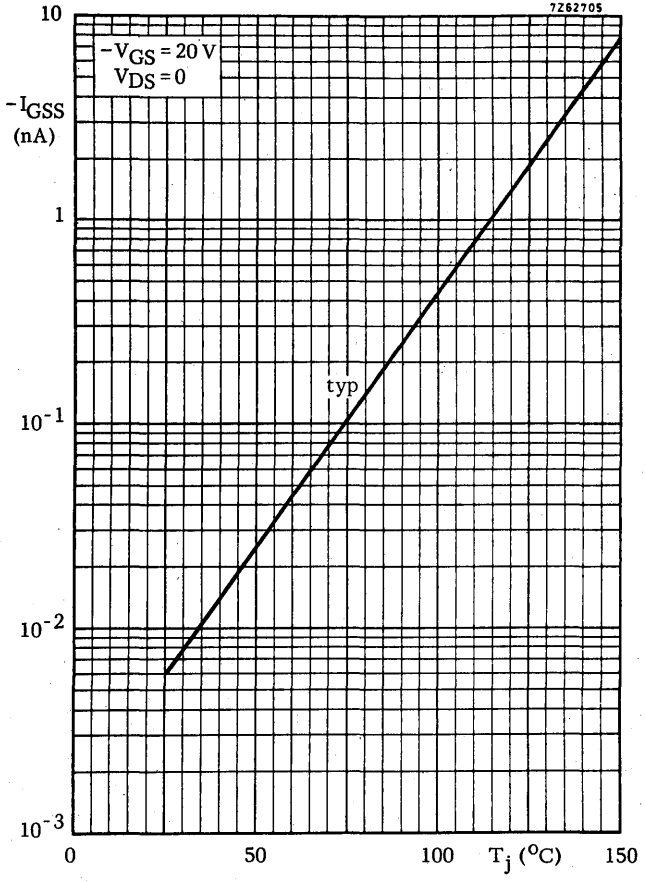
CHARACTERISTICS

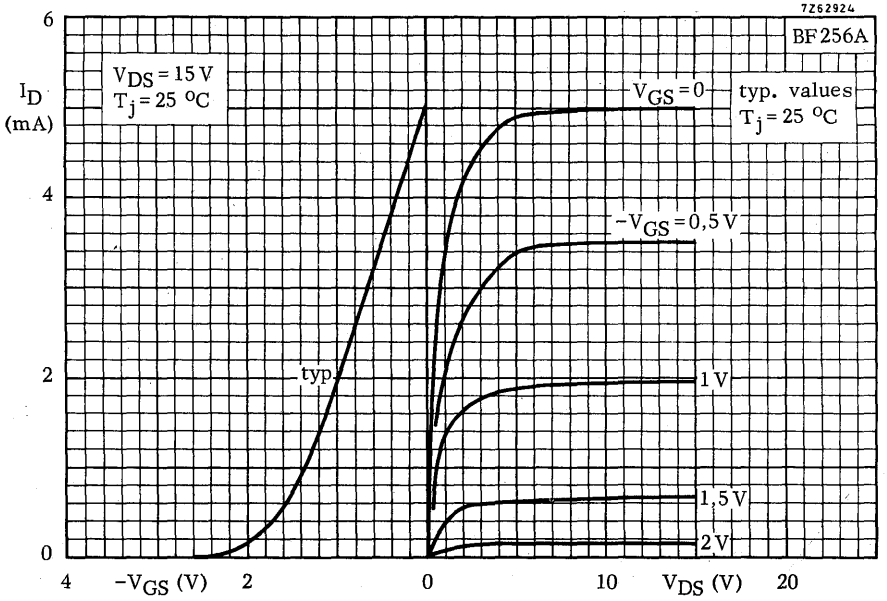
T_{amb} = 25 °C unless otherwise specified

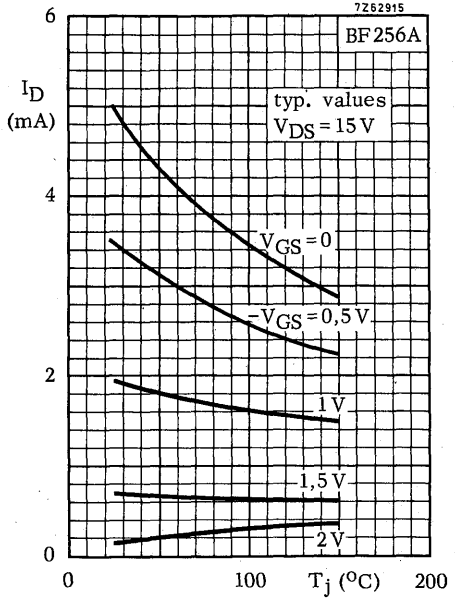
Gate cut-off current						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<		5	nA	
		BF256A	B	C		
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	> 3	6	11	mA	1)
		< 7	13	18	mA	1)
Gate-source breakdown voltage						
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>		30	V	
Gate-source voltage						
I_D = 200 µA; V_{DS} = 15 V	$-V_{GS}$		0,5 to 7,5		V	
y-parameters (common source)						
Transfer admittance at f = 1 kHz						
V_{DS} = 15 V; V_{GS} = 0	$\lvert y_{fs} \rvert$	>		4,5	mA/V	1)
		typ.		5	mA/V	1)
Output capacitance at f = 1 MHz						
V_{DS} = 20 V; V_{GS} = 0	C_{os}	typ.		1,2	pF	
Feedback capacitance at f = 1 MHz						
V_{DS} = 20 V; $-V_{GS}$ = 1 V	C_{rs}	typ.		0,7	pF	
Cut-off frequency						
V_{DS} = 15 V; V_{GS} = 0	f_{gfs}	typ.		1	GHz	2)
Noise figure at f = 800 MHz						
V_{DS} = 10 V; R_S = 47 Ω	F	typ.		7,5	dB	
Power gain at f = 800 MHz						
V_{DS} = 15 V; R_S = 47 Ω	G_p	typ.		11	dB	

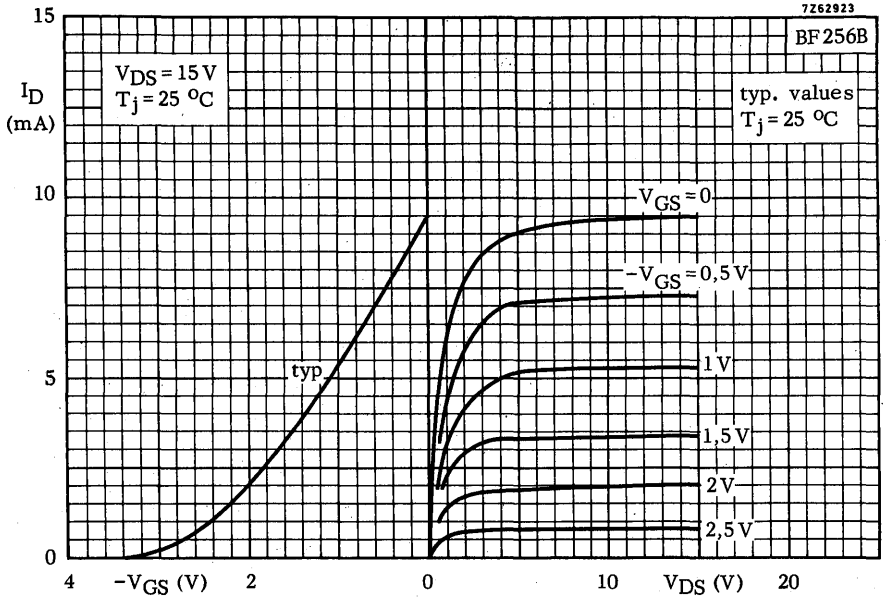
1) Measured under pulse conditions: t_p = 300 µs; $\delta \leq 0{,}02$

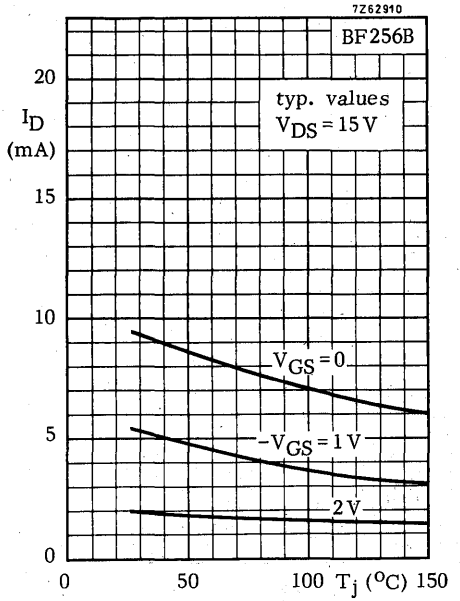
2) The frequency at which g_{fs} is 0,7 of its value at 1 kHz.

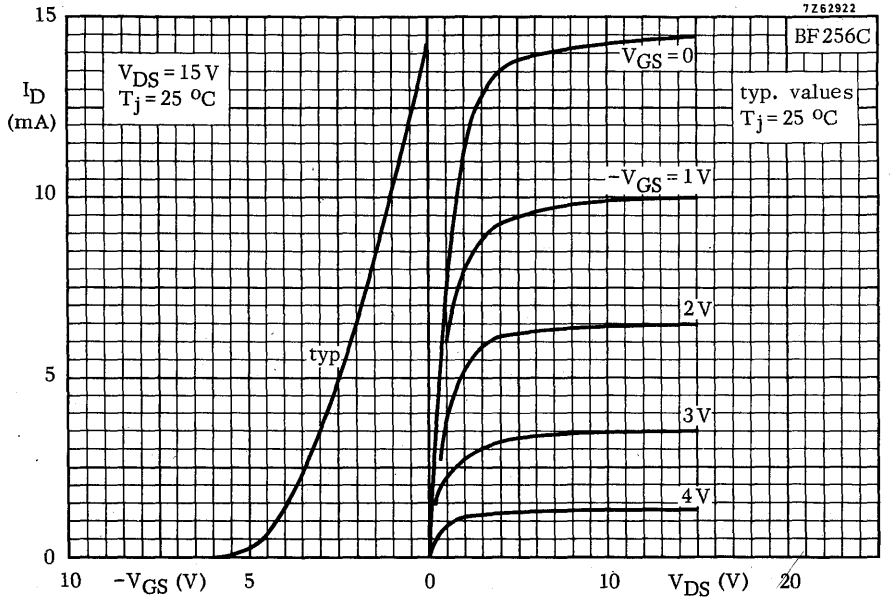

7Z62705
10
$-V_{GS}$ = 20 V
V_{DS} = 0
$-I_{GSS}$ (nA)
1
typ
10^{-1}
10^{-2}
10^{-3}
0
50
100
T_j (°C)
150

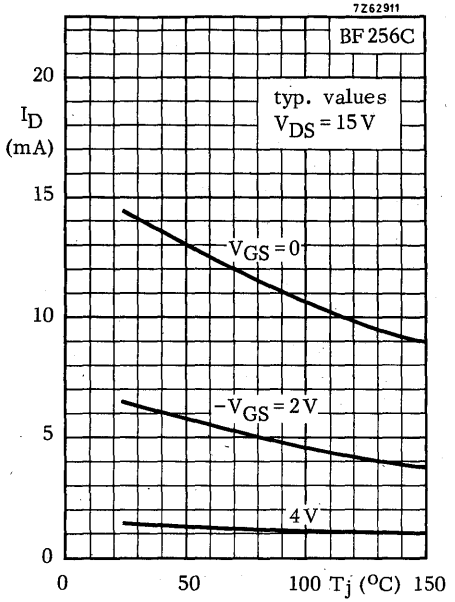

7Z62924
BF256A
V_{DS} = 15 V
T_j = 25 °C
I_D (mA)
typ. values
T_j = 25 °C
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
typ.
6
4
2
0
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

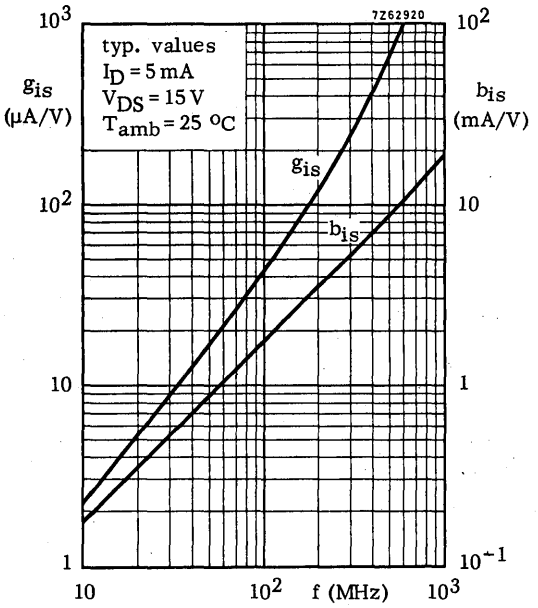

7Z62915
BF256A
I_D (mA)
typ. values
V_{DS} = 15 V
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
6
4
2
0
0
100
T_j (°C)
200

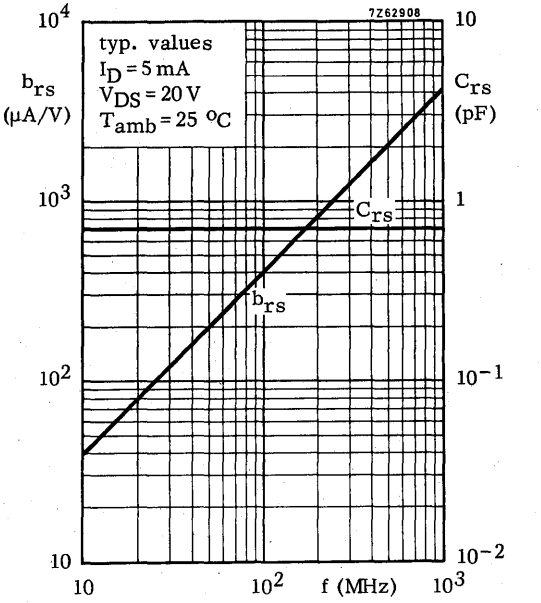

7Z62923
BF256B
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
1,5 V
2 V
2,5 V
typ
4
$-V_{GS}$ (V)
2
0
10
V_{DS} (V)
20

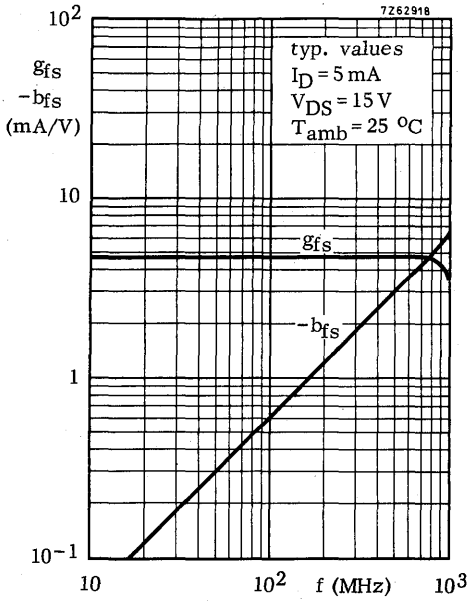

7Z62910
BF256B
typ. values
V_{DS} = 15 V
I_D (mA)
20
15
10
5
0
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
0
50
100
T_j (°C)
150

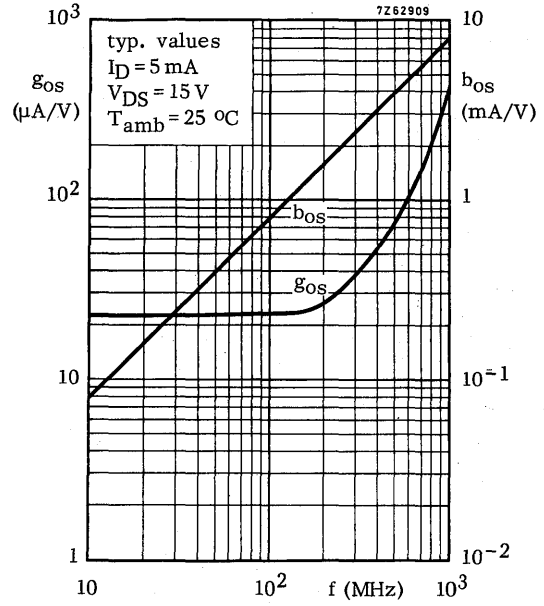

7Z62922
BF256C
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 1 V
2 V
3 V
4 V
typ
15
10
5
0
10
$-V_{GS}$ (V)
5
0
10
V_{DS} (V)
20

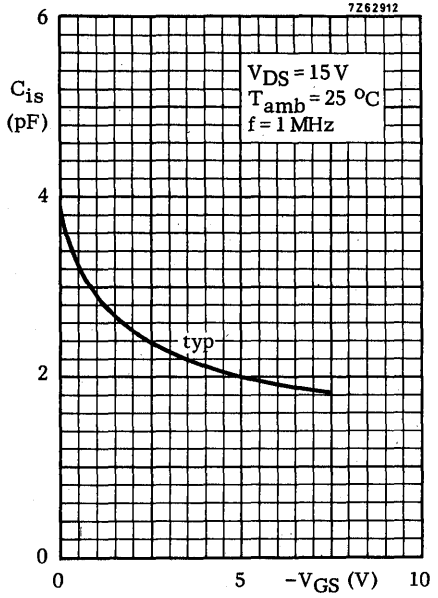

7Z62911
BF256C
typ. values
V_{DS} = 15 V
I_D (mA)
V_{GS} = 0
$-V_{GS}$ = 2 V
4 V
20
15
10
5
0
0
50
100 T_j (°C)
150

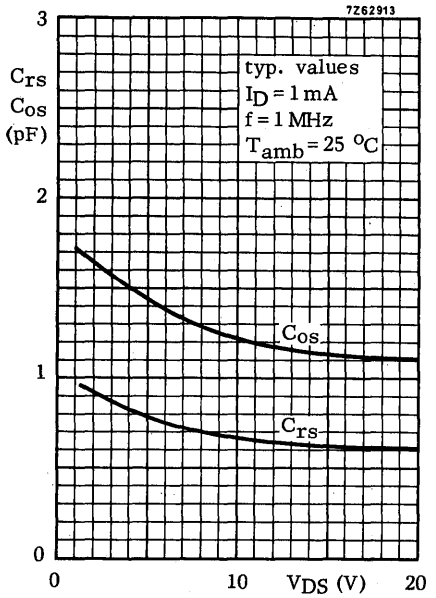

7Z62920
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

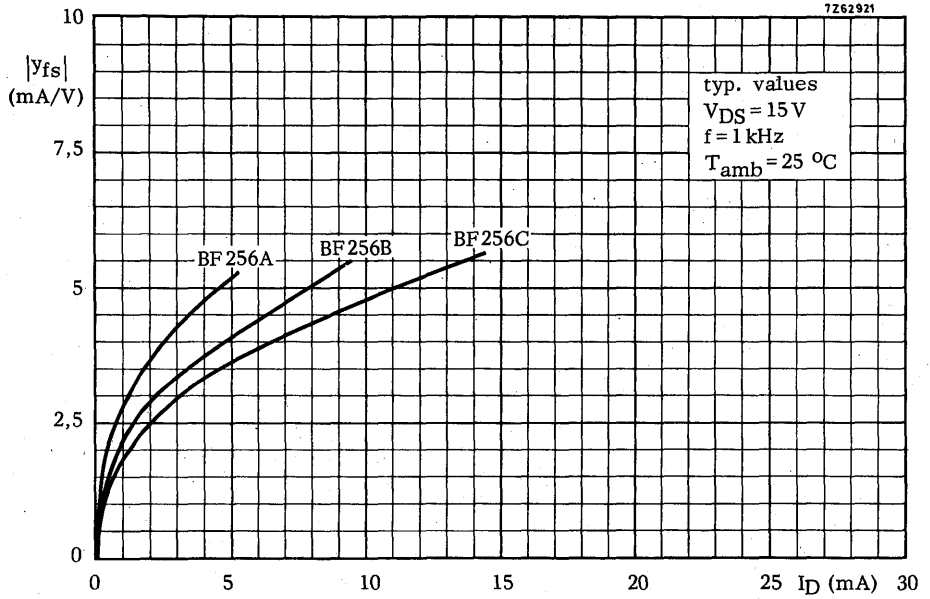

7Z62908
typ. values
I_D = 5 mA
V_{DS} = 20 V
T_{amb} = 25 °C
b_{rs} (μA/V)
C_{rs} (pF)
C_{rs}
b_{rs}
10^4
10^3
10^2
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

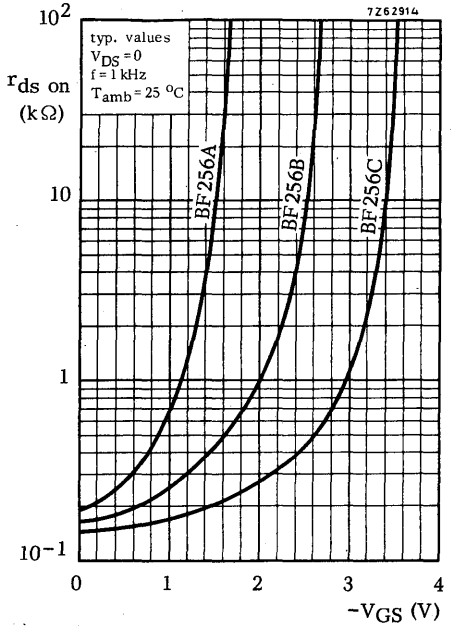

7Z62918
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{fs}
$-b_{fs}$
(mA/V)
10^2
10
1
10^{-1}
g_{fs}
$-b_{fs}$
10
10^2
f (MHz)
10^3

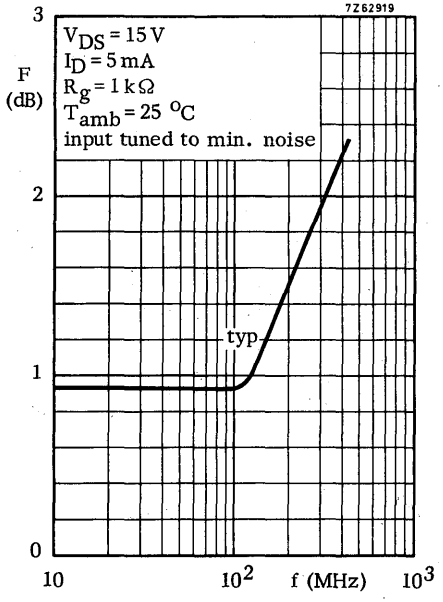

7Z62909
typ. values
I_D = 5 mA
V_{DS} = 15 V
T_{amb} = 25 °C
g_{os}
(μA/V)
b_{os}
(mA/V)
10^3
10^2
10
1
10
1
10^{-1}
10^{-2}
b_{os}
g_{os}
10
10^2
f (MHz)
10^3

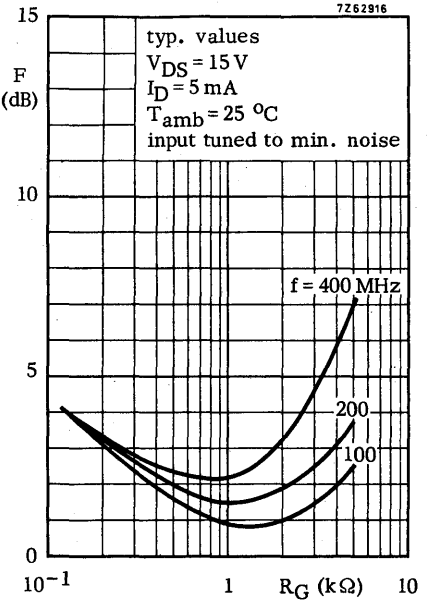

7Z62912
C_{is} (pF)
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
typ
$-V_{GS}$ (V)
0
2
4
6
0
5
10


7Z62913
C_{rs}
C_{os}
(pF)
typ. values
I_D = 1 mA
f = 1 MHz
T_{amb} = 25 °C
C_{os}
C_{rs}
V_{DS} (V)
0
1
2
3
0
10
20


7Z62921
$|y_{fs}|$
(mA/V)
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
BF256A
BF256B
BF256C
I_D (mA)
0
2,5
5
7,5
10
0
5
10
15
20
25
30


7Z62914
typ. values
V_{DS} = 0
f = 1 kHz
T_{amb} = 25 °C
$r_{ds\ on}$ (kΩ)
10^2
10
1
10^{-1}
BF256A
BF256B
BF256C
0
1
2
3
4
$-V_{GS}$ (V)


7Z62919
V_{DS} = 15 V
I_D = 5 mA
R_g = 1 kΩ
T_{amb} = 25 °C
input tuned to min. noise
F (dB)
3
2
1
0
typ
10
10^2
f (MHz)
10^3


7Z62916
typ. values
V_{DS} = 15 V
I_D = 5 mA
T_{amb} = 25 °C
input tuned to min. noise
F (dB)
15
10
5
0
f = 400 MHz
200
100
10^{-1}
1
R_G (kΩ)
10

N-CHANNEL SILICON FIELD-EFFECT TRANSISTORS

Asymmetrical N-channel planar epitaxial junction field-effect transistors in plastic TO-92 variants, intended for applications up to the v.h.f. range.
These FETs can be supplied in four I_{DSS} groups. Special features are the low feedback capacitance and the low noise figure. Thanks to these special features the BF410 is very suitable for applications such as the r.f. stages in f.m. portables (type A), car radios (type B) and mains radios (type C) or the mixer stage (type D).

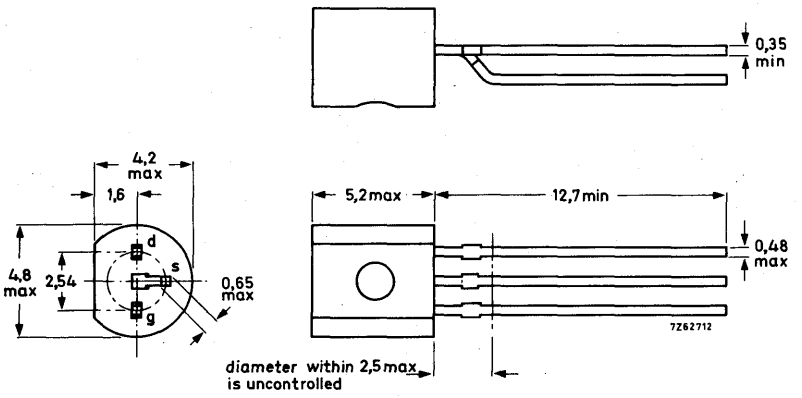
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.		20			V
Drain current (d.c. or average)	I_D	max.		30			mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.		300			mW
			BF410A	B	C	D	
Drain current V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,7	2,5	6	10	mA
		<	3,0	7,0	12	18	mA
Transfer admittance (common source) V_{DS} = 10 V; V_{GS} = 0; f = 1 kHz	$\lvert y_{fs} \rvert$	>	2,5	4	6	7	mA/V
Feedback capacitance V_{DS} = 10 V; V_{GS} = 0	C_{rs}	typ.	0,3	0,3	–	–	pF
V_{DS} = 10 V; I_D = 5 mA	C_{rs}	typ.	–	–	0,3	0,3	pF
Noise figure at optimum source admittance G_S = 1 mA/V; $-B_S$ = 3 mA/V; f = 100 MHz V_{DS} = 10 V; V_{GS} = 0	F	typ.	1,5	1,5	–	–	dB
V_{DS} = 10 V; I_D = 5 mA	F	typ.	–	–	1,5	1,5	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain-gate voltage (open source)	V_{DGO}	max.	20	V
Drain current (d.c. or average)	I_D	max.	30	mA
Gate current	$\pm I_G$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		−65 to + 150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	0,25	°C/mW

STATIC CHARACTERISTICS

T_{amb} = 25 °C

			BF410A	B	C	D	
Gate cut-off current							
$-V_{GS}$ = 0,2 V; V_{DS} = 0	$-I_{GSS}$	<	10	10	10	10	nA
Gate-drain breakdown voltage							
I_S = 0; $-I_D$ = 10 μA	$-V_{(BR)GDO}$	>	20	20	20	20	V
Drain current							
V_{DS} = 10 V; V_{GS} = 0	I_{DSS}	>	0,7	2,5	6	10	mA
		<	3,0	7,0	12	18	mA
Gate-source cut-off voltage							
I_D = 10 μA; V_{DS} = 10 V	$-V_{(P)GS}$	typ.	0,8	1,5	2,2	3	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): V_{DS} = 10 V; V_{GS} = 0; T_{amb} = 25 °C for **BF410A** and **B**
V_{DS} = 10 V; I_D = 5 mA; T_{amb} = 25 °C for **BF410C** and **D**

y-parameters (common source)			BF410A	B	C	D	
Input capacitance at f = 1 MHz	C_{is}	<	5	5	5	5	pF
Input conductance at f = 100 MHz	g_{is}	typ.	100	90	60	50	μA/V
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	0,3	0,3	0,3	0,3	pF
		<	0,4	0,4	0,4	0,4	pF
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	2,5	4,0	4,0	3,5	mA/V
V_{GS} = 0 instead of I_D = 5 mA	$\lvert y_{fs} \rvert$	>	–	–	6,0	7,0	mA/V
Transfer admittance at f = 100 MHz	$\lvert y_{fs} \rvert$	typ.	3,5	5,5	5,0	5,0	mA/V
Output capacitance at f = 1 MHz	C_{os}	<	3	3	3	3	pF
Output conductance at f = 1 MHz	g_{os}	<	60	80	100	120	μA/V
Output conductance at f = 100 MHz	g_{os}	typ.	35	55	70	90	μA/V
Noise figure at optimum source admittance G_S = 1 mA/V; $-B_S$ = 3 mA/V; f = 100 MHz	F	typ.	1,5	1,5	1,5	1,5	dB

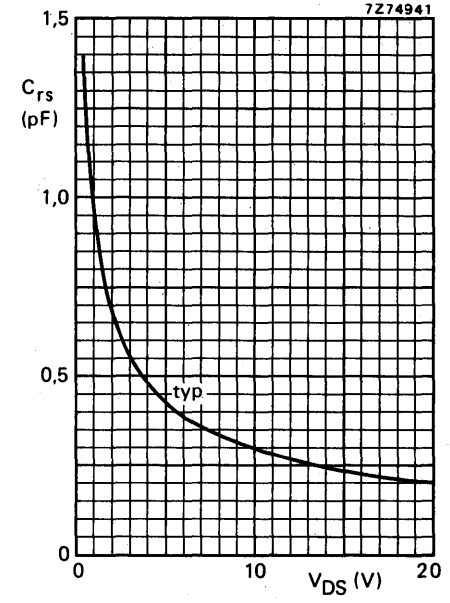


Fig. 2 V_{GS} = 0 for **BF410A** and **BF410B**; I_D = 5 mA for **BF410C** and **BF410D**; f = 1 MHz; T_{amb} = 25 °C.

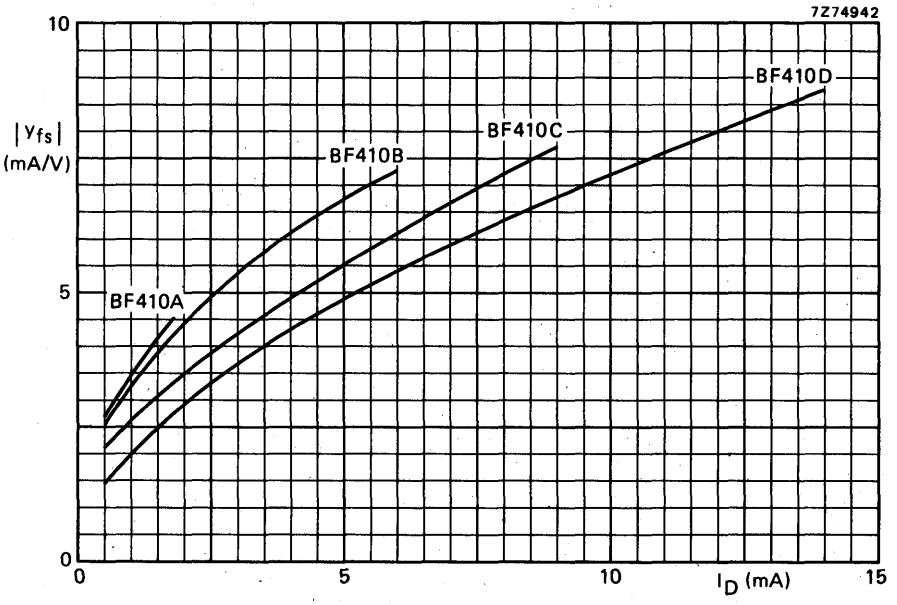


Fig. 3 V_{DS} = 10 V; f = 1 kHz; T_{amb} = 25 °C; typical values.

DUAL N-CHANNEL FETS

Dual symmetrical n-channel silicon planar epitaxial junction field-effect transistors in a TO-71 metal envelope, with electrically insulated gates and a common substrate connected to the envelope; intended for high performance low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 200 μA; V_{DG} = 15 V

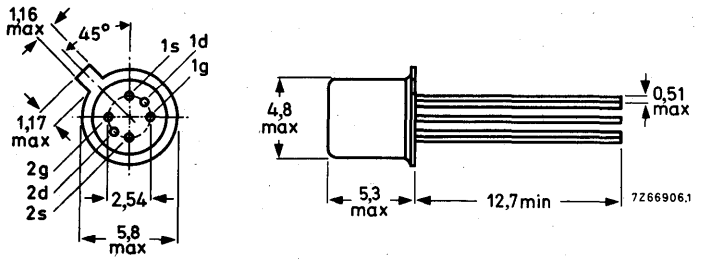
		BFQ10	11	12	13	14	15	16	
Difference in gate current	$\lvert\Delta I_G\rvert$	< 10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\lvert\Delta V_{GS}\rvert$	< 5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	< 5	5	10	20	20	40	50	μV/K
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	> 0,98 < 1,02	0,98 1,02	0,98 1,02	0,98 1,02	0,98 1,02	0,95 1,05	0,95 1,05	
Difference in transfer impedance	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	< 6	6	12	12	12	20	30	Ω
Difference in penetration factor	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	< 10	30	30	30	30	30	100	μV/V
Common mode rejection ratio	CMRR	> 100	90	90	90	90	90	80	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-71.

All leads insulated from the case.



RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Voltage between gate 1 and gate 2	$\pm V_{1G-2G}$	max.	40	V
Currents				
Drain current	I_D	max.	30	mA
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	250	mW
Temperatures				
Storage temperature	T_{stg}	−65 to +200		°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	0,5	°C/mW

CHARACTERISTICS (total device) $T_{amb} = 25\ ^{o}C$ unless otherwise specified

Measured at: $I_D = 200\ \mu A$; $V_{DG} = 15\ V$ except for drain current ratio.

			BFQ10	11	12	13	14	15	16	
Drain current ratio [1]										
$V_{DG} = 15\ V$; $V_{GS} = 0$	$\frac{I_{1D-1SS}}{I_{2D-2SS}}$	>	0,97	0,95	0,95	0,95	0,92	0,90	0,80	
		<	1,03	1,05	1,05	1,05	1,08	1,10	1,20	
Difference in gate current	$\lvert\Delta I_G\rvert$	<	10	10	10	10	10	10	10	pA
Gate-source voltage difference	$\lvert\Delta V_{GS}\rvert$	<	5	10	10	10	15	20	50	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\ \Delta V_{GS}}{dT}\right\rvert$	<	5	5	10	20	20	40	50	$\mu V/^{o}C$
Transfer conductance ratio	$\frac{g_{1fs}}{g_{2fs}}$	>	0,98	0,98	0,98	0,98	0,98	0,95	0,95	
		<	1,02	1,02	1,02	1,02	1,02	1,05	1,05	
Difference in transfer impedance [2]	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	6	6	12	12	12	20	30	Ω
Difference in penetration factor [3]	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	10	30	30	30	30	30	100	μV/V
Common mode rejection ratio [4]	CMRR	>	100	90	90	90	90	90	80	dB

1) Measured under pulse conditions.

2) The difference in transfer impedance is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$\left(\Delta\frac{1}{g_{fs}} = \frac{d\ \Delta V_{GS}}{d\ I_D}\right.$ at $\left.V_{DG} = \text{constant}\right)$

3) The difference in penetration factor is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$\left(\Delta\frac{g_{os}}{g_{fs}} = \frac{d\ \Delta V_{GS}}{d\ V_{DG}}\right.$ at $\left.I_D = \text{constant}\right)$

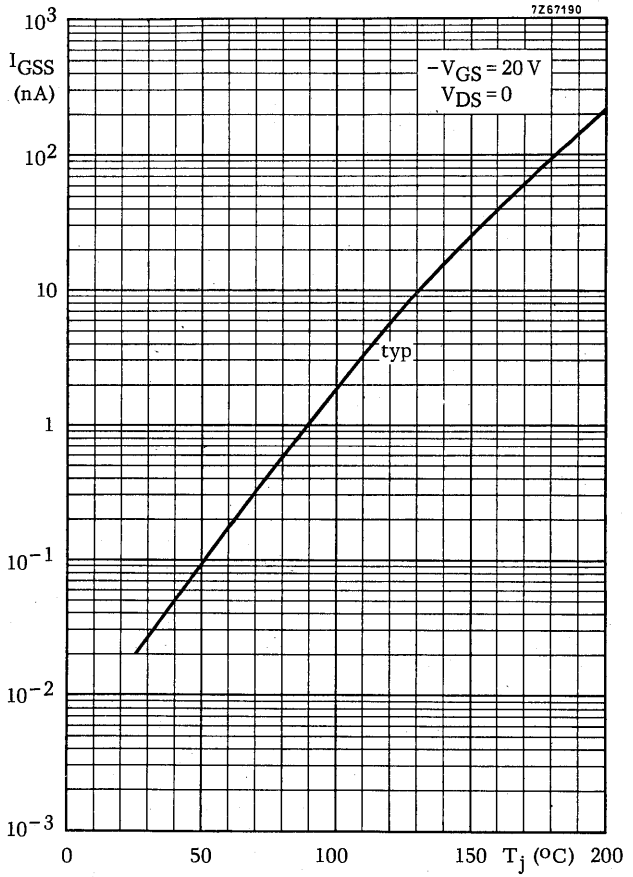
4) Common mode rejection ratio

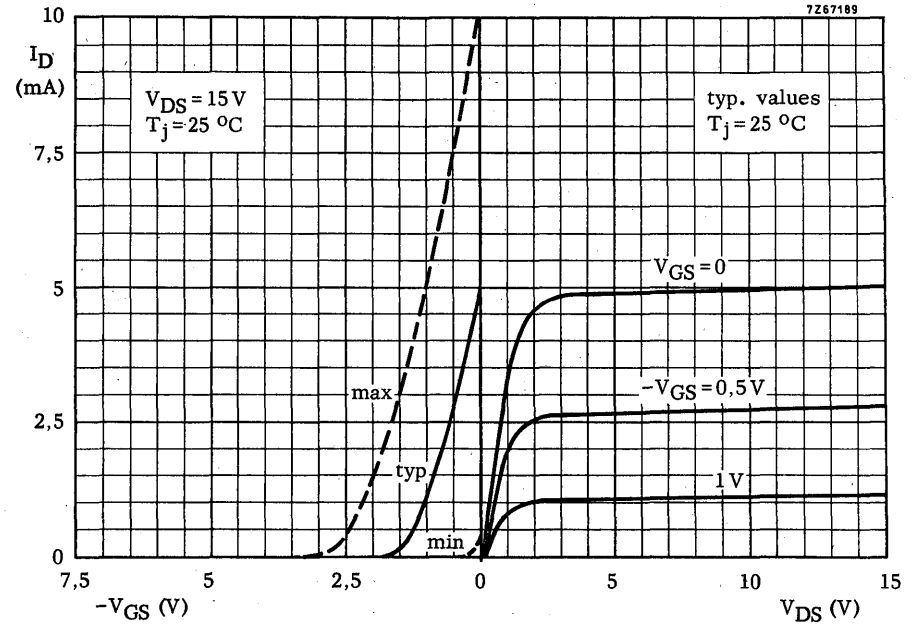
$$\text{CMRR (in dB)} = -20 \log\left|\Delta\frac{g_{os}}{g_{fs}}\right|$$

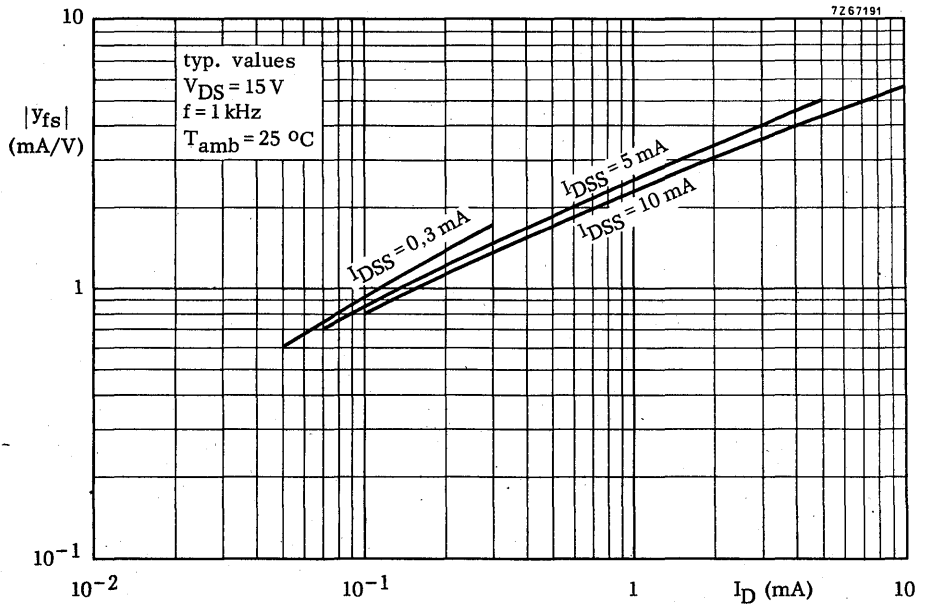
CHARACTERISTICS (Individual transistor) T_{amb} = 25 °C unless otherwise specified

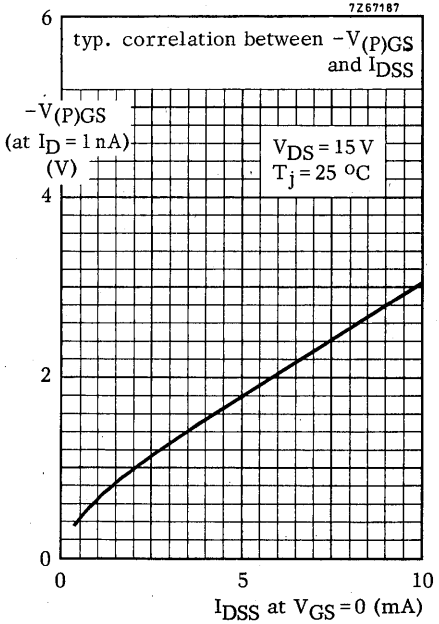
Gate cut-off current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	100	pA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 125 °C	$-I_{GSS}$	<	20	nA
Gate current				
I_D = 200 μA; V_{DG} = 15 V; T_{amb} = 125 °C	I_G	<	10	nA
Drain current				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	0,5 to	10	mA [1]
Gate-source voltage				
I_D = 200 μA; V_{DG} = 15 V	$-V_{GS}$	<	2,7	V
Gate-source cut-off voltage				
I_D = 1 nA; V_{DG} = 15 V	$-V_{(P)GS}$	0,5 to	3,5	V
Transfer conductance at f = 1 kHz				
I_D = 200 μA; V_{DG} = 15 V	g_{fs}	>	1,0	mA/V
Output conductance at f = 1 kHz				
I_D = 200 μA; V_{DG} = 15 V	g_{os}	<	5	μA/V
Input capacitance at f = 1 MHz				
I_D = 200 μA; V_{DG} = 15 V	C_{is}	<	8	pF [2]
Feedback capacitance at f = 1 MHz				
I_D = 200 μA; V_{DG} = 15 V	C_{rs}	<	1,0	pF [2]
Equivalent noise voltage				
I_D = 200 μA; V_{DS} = 15 V B = 0,6 to 100 Hz	V_n	<	0,5	μV

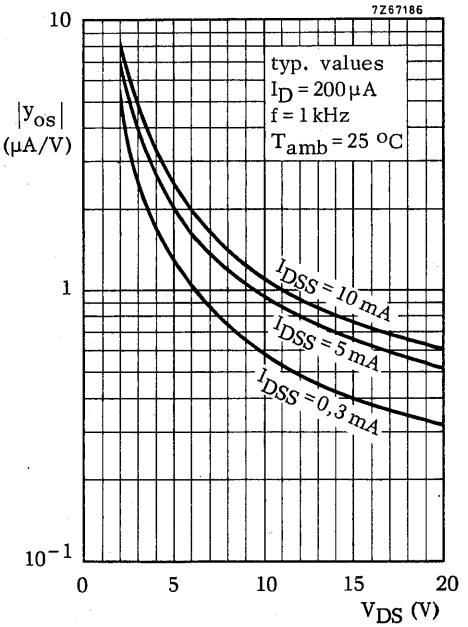
1) Measured under pulse conditions.
2) Measured with case grounded.

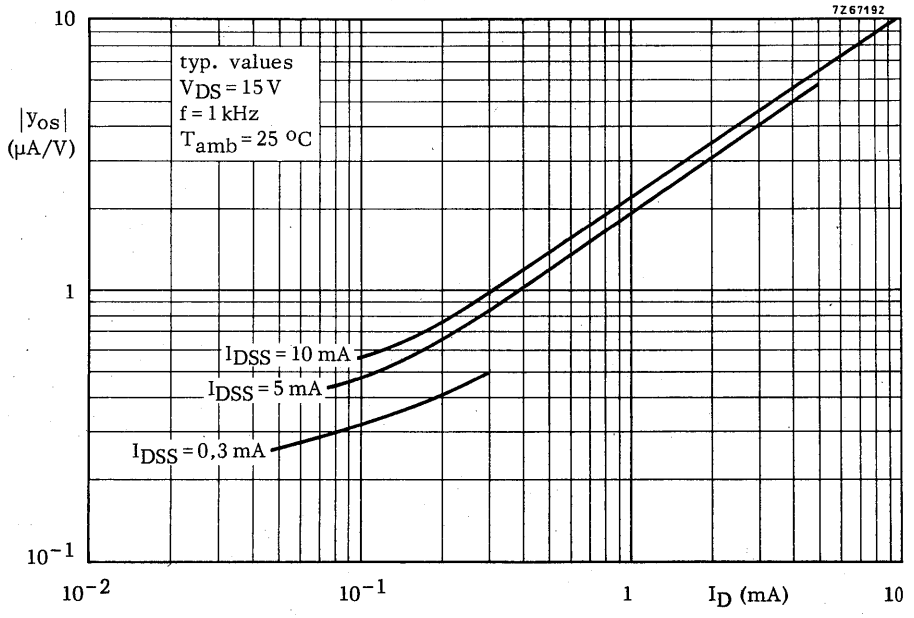

7Z67190
10^3
I_{GSS} (nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS} = 20$ V
$V_{DS} = 0$
typ
0
50
100
150
T_j (°C)
200

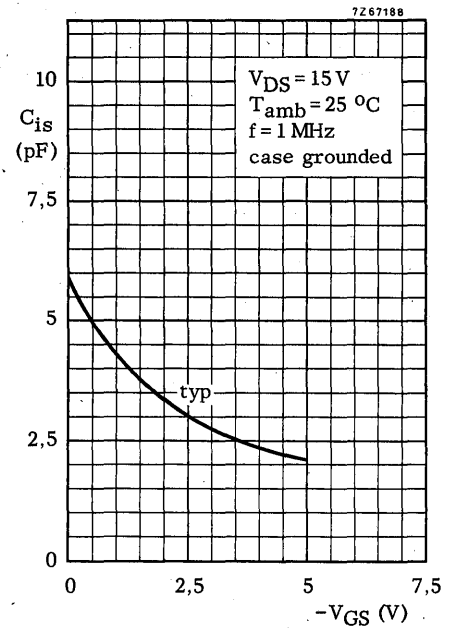

7Z67189
10
I_D (mA)
7,5
5
2,5
0
V_{DS} = 15 V
T_j = 25 °C
typ. values
T_j = 25 °C
V_{GS} = 0
$-V_{GS}$ = 0,5 V
1 V
max
typ
min
7,5
5
2,5
0
5
10
15
$-V_{GS}$ (V)
V_{DS} (V)

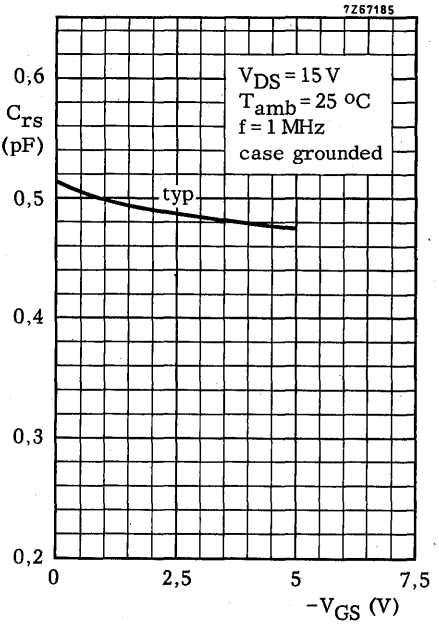

7Z67191
10
$|y_{fs}|$ (mA/V)
1
10^{-1}
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
I_{DSS} = 0,3 mA
I_{DSS} = 5 mA
I_{DSS} = 10 mA
10^{-2}
10^{-1}
1
I_D (mA)
10

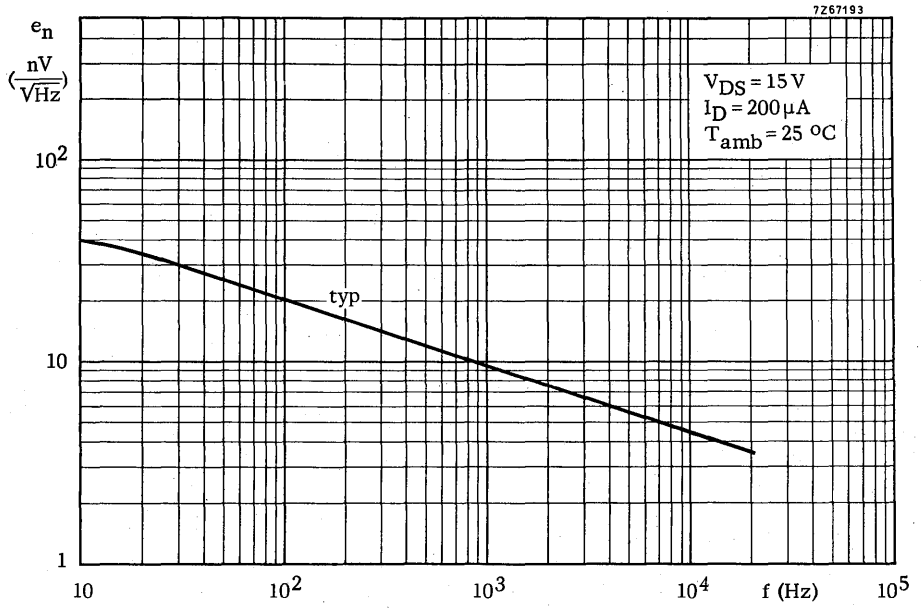

7Z67187
typ. correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ (at I_D = 1 nA) (V)
V_{DS} = 15 V
T_j = 25 °C
6
4
2
0
0
5
10
I_{DSS} at V_{GS} = 0 (mA)


7Z67186
typ. values
I_D = 200 µA
f = 1 kHz
T_{amb} = 25 °C
$|y_{os}|$ (µA/V)
I_{DSS} = 10 mA
I_{DSS} = 5 mA
I_{DSS} = 0,3 mA
10
1
10^{-1}
0
5
10
15
20
V_{DS} (V)


7Z67192
typ. values
V_{DS} = 15 V
f = 1 kHz
T_{amb} = 25 °C
$|y_{os}|$ (µA/V)
I_{DSS} = 10 mA
I_{DSS} = 5 mA
I_{DSS} = 0,3 mA
10
1
10^{-1}
10^{-2}
10^{-1}
1
10
I_D (mA)


7Z67188
10
C_{is} (pF)
7,5
5
2,5
0
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
case grounded
typ
0
2,5
5
7,5
$-V_{GS}$ (V)


7Z67185
0,6
C_{rs} (pF)
0,5
0,4
0,3
0,2
V_{DS} = 15 V
T_{amb} = 25 °C
f = 1 MHz
case grounded
typ
0
2,5
5
7,5
$-V_{GS}$ (V)


7Z67193
e_n ($\frac{nV}{\sqrt{Hz}}$)
10^2
10
1
V_{DS} = 15 V
I_D = 200 µA
T_{amb} = 25 °C
typ
10
10^2
10^3
10^4
f (Hz)
10^5

MATCHED N-CHANNEL FETS

Matched pair of symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes, mounted together in a metal S-clip.

These devices are intended for low level differential amplifiers.

QUICK REFERENCE DATA

Characteristics measured at T_{amb} = 25 °C; I_D = 0,5 mA; V_{DG} = 15 V

			BFS21	BFS21A	
Gate cut-off current	I_G	<	0,5	0,5	nA
Gate -source voltage difference	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
Thermal drift of gate-source voltage difference	$\left\lvert\frac{d\Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/K
Difference in transfer impedance	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	15	7,5	Ω
Difference in penetration factor	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0,5	mV/V
Common mode rejection ratio	CMRR	>	60	66	dB

MECHANICAL DATA

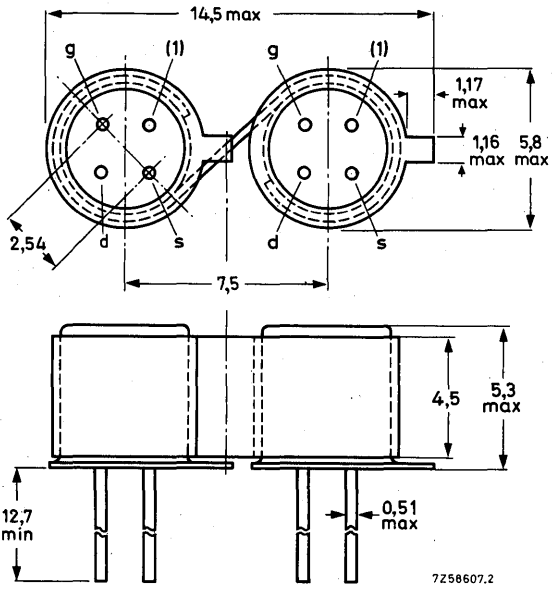
SOT-52 (see page 2)

TOTAL DEVICE

Dimensions in mm

MECHANICAL DATA

SOT-52



(1) = shield lead (connected to case).

Maximum lead diameter is guaranteed only for 12,7 mm.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage between any 2 terminals	V	max.	30 V
Drain current	I_D	max.	4 mA
Gate current	I_G	max.	0,5 mA
Total power dissipation up to T_{amb} = 100 °C	P_{tot}	max.	30 mW
Operating ambient temperature	T_{amb}	−20 to + 100	°C

CHARACTERISTICS (total device) T_{amb} = 25 °C unless otherwise specified

			BFS21	BFS21A	
Drain current ratio					
V_{DG} = 15 V; V_{GS} = 0; T_j = 25 °C	$\frac{I_{D1-S1S}}{I_{D2-S2S}}$	>	0.95	0.95	
		<	1.05	1.05	
Gate-source voltage difference					
I_D = 500 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
I_D = 100 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}\rvert$	<	20	10	mV
Thermal drift of gate-source voltage difference					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\frac{d\ \Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/°C
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\frac{d\ \Delta V_{GS}}{dT}\right\rvert$	<	75	40	μV/°C
Change of gate-source voltage difference with ambient temperature					
T_{amb} = 25 to 100 °C					
I_D = 500 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1})\rvert$	<	6	3	mV
I_D = 100 μA; V_{DG} = 15 V	$\lvert\Delta V_{GS}(T_{amb2}) - \Delta V_{GS}(T_{amb1})\rvert$	<	6	3	mV
Difference of penetration factors [1]					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0.5	10^{-3}
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{g_{os}}{g_{fs}}\right\rvert$	<	1	0.5	10^{-3}
Difference of transfer impedances [2]					
I_D = 500 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	15	7.5	Ω
I_D = 100 μA; V_{DG} = 15 V	$\left\lvert\Delta\frac{1}{g_{fs}}\right\rvert$	<	75	37.5	Ω

1) The difference between the penetration factors is equal to the ratio of the change of the gate-source voltage difference to the change of drain-gate voltage, at constant drain current.

$$\left(\Delta\frac{g_{os}}{g_{fs}} = \frac{d\ \Delta V_{GS}}{d\ V_{DG}} \text{ at } I_D = \text{constant}\right)$$

2) The difference between the transfer impedances is equal to the ratio of the change of the gate-source voltage difference to the change of drain current, at constant drain-gate voltage.

$$\left(\Delta\frac{1}{g_{fs}} = \frac{d\ \Delta V_{GS}}{d\ I_D} \text{ at } V_{DG} = \text{constant}\right)$$

CHARACTERISTICS (continued) (total device)

Common mode rejection ratio [1]			BFS21	BFS21A	
I_D = 500 μA; V_{DG} = 15 V	CMRR	>	60	66	dB
I_D = 100 μA; V_{DG} = 15 V	CMRR	>	60	66	dB

INDIVIDUAL TRANSISTOR

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Currents				
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 25°	P_{tot}	max.	300	mW
Temperatures				
Storage temperature	T_{stg}	−65 to +200		°C
Junction temperature	T_j	max.	200	°C

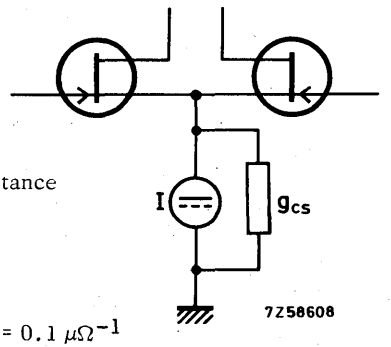
THERMAL RESISTANCE

From junction to ambient in free air (for individual transistor without S-clip) $R_{th\ j\text{-}a}$ = 0.59 °C/mW

[1]) Common mode rejection ratio

$$(CMRR)^{-1} = \Delta\frac{g_{os}}{g_{fs}} + \tfrac{1}{2} g_{cs}\,\Delta\frac{1}{g_{fs}}$$

where g_{cs} in this formula is the output conductance of the summing current source.



The guaranteed values of CMRR apply at g_{cs} = 0.1 μΩ^{-1}

CHARACTERISTICS (individual transistor) T_{amb} = 25 °C unless otherwise specified

Gate cut-off current				
I_D = 500 μA; V_{DS} = 15 V	I_G	<	0.5	nA
I_D = 500 μA; V_{DS} = 15 V; T_{amb} = 100 °C	I_G	<	25	nA
Drain current				
V_{DS} = 15 V, V_{GS} = 0, T_j = 25 °C	I_{DSS}	>	1	mA
Gate-source cut-off voltage				
I_D = 0.5 nA, V_{DS} = 15 V	$-V_{(P)GS}$	<	6	V
Transfer conductance at f = 1 kHz				
I_D = 500 μA; V_{DS} = 15 V	g_{fs}	>	1.0	$m\Omega^{-1}$
Output conductance at f = 1 kHz				
I_D = 500 μA; V_{DS} = 15 V	g_{os}	<	15	$\mu\Omega^{-1}$
Input capacitance at f = 1 MHz				
I_D = 500 μA; V_{DS} = 15 V	C_{is}	<	5	pF
Feedback capacitance at f = 1 MHz				
I_D = 500 μA; V_{DS} = 15 V	C_{rs}	<	0.75	pF
Equivalent noise voltage				
f = 10 Hz				
I_D = 500 μA; V_{DS} = 15 V	$V_n/\sqrt{B}$	<	200	$nV/\sqrt{Hz}$
V_{DS} = 15 V, V_{GS} = 0	$V_n/\sqrt{B}$	<	75	$nV/\sqrt{Hz}$

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are designed for broad band amplifiers (0 to 300 MHz). Their very low noise at low frequencies makes these devices very suitable for differential amplifiers, electro-medical and nuclear detector preamplifiers.

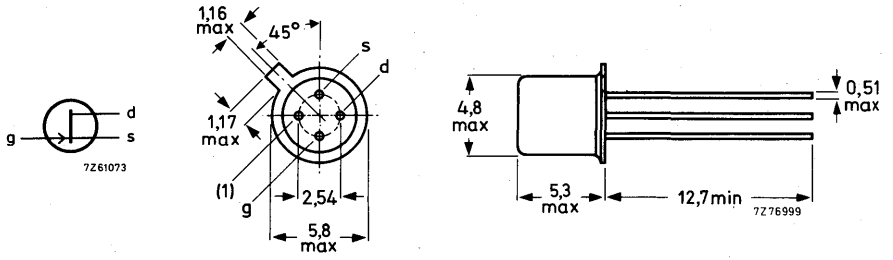
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300		mW
			BFW10	**BFW11**	
Drain current		>	8	4	mA
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	<	20	10	mA
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
Feedback capacitance at f = 1 MHz					
V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	0,80	0,80	pF
Transfer admittance (common source)					
V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	$\lvert y_{fs} \rvert$	>	3,2	3,2	mA/V
Noise figure at V_{DS} = 15 V; V_{GS} = 0					
f = 100 MHz; R_G = 1 kΩ	F	<	2,5	2,5	dB
Equivalent noise voltage					
f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	$nV/\sqrt{Hz}$

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Currents				
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Temperatures				
Storage temperature	T_{stg}	−65 to +200		°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

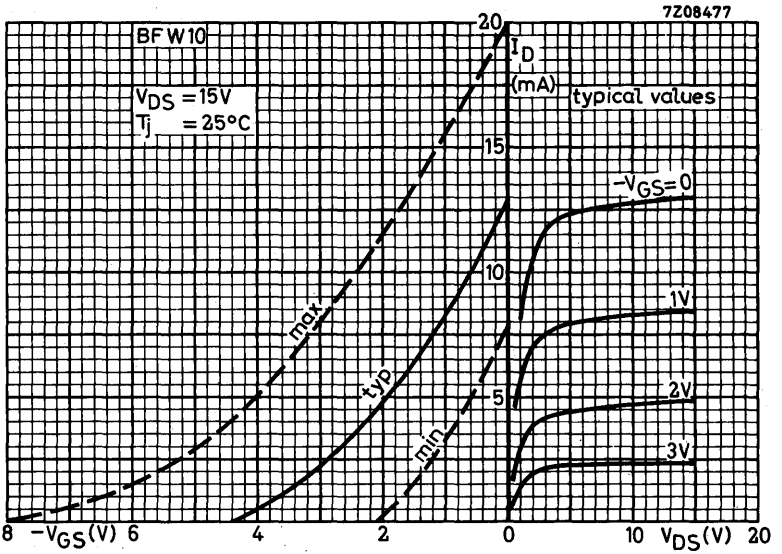
From junction to ambient	$R_{th\ j-a}$	=	0.59	°C/mW

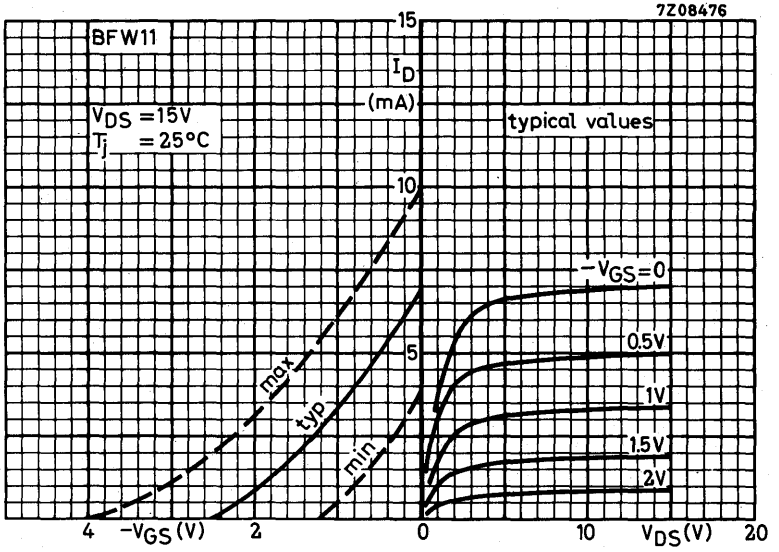
CHARACTERISTICS

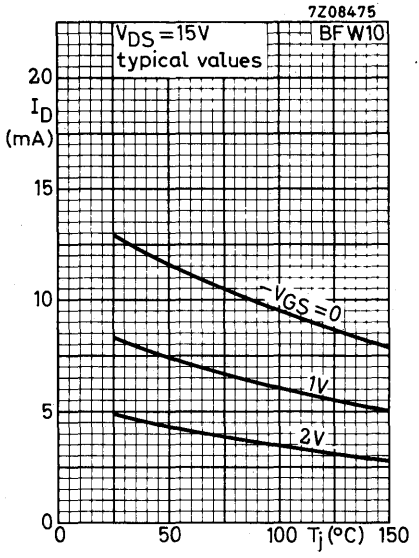
T_j = 25 °C unless otherwise specified

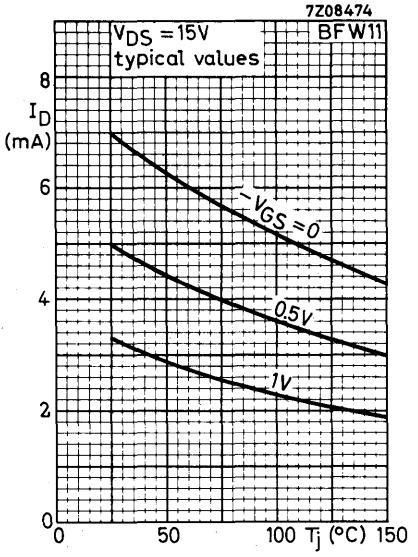
			BFW10	BFW11	
Gate cut-off current					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.5	0.5	μA
Drain current [1]					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	8	4	mA
		<	20	10	mA
Gate-source voltage					
I_D = 400 μA; V_{DS} = 15 V	$-V_{GS}$	>	2.0		V
		<	7.5		V
I_D = 50 μA; V_{DS} = 15 V	$-V_{GS}$	>		1.25	V
		<		4.0	V
Gate-source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	6	V
y parameters					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
f = 1 kHz Transfer admittance	$\lvert y_{fs} \rvert$	>	3.5	3.0	mA/V
		<	6.5	6.5	mA/V
Output admittance	$\lvert y_{os} \rvert$	<	85	50	μA/V
f = 1 MHz Input capacitance	C_{is}	typ.	4	4	pF
		<	5	5	pF
Feedback capacitance	C_{rs}	typ.	0.6	0.6	pF
		<	0.80	0.80	pF
f = 200 MHz Transfer admittance	$\lvert y_{fs} \rvert$	>	3.2	3.2	mA/V
Input conductance	g_{is}	<	800	800	μA/V
Output conductance	g_{os}	<	200	100	μA/V
Noise figure at f = 100 MHz; R_G = 1 kΩ					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C input tuned to minimum noise	F	<	2.5	2.5	dB
Equivalent noise voltage					
V_{DS} = 15 V; V_{GS} = 0; T_{amb} = 25 °C					
f = 10 Hz	$V_n/\sqrt{B}$	<	75	75	nV/$\sqrt{Hz}$

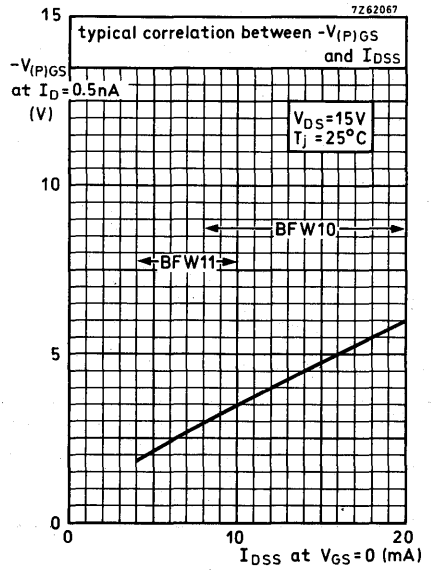
[1] Measured under pulsed conditions.

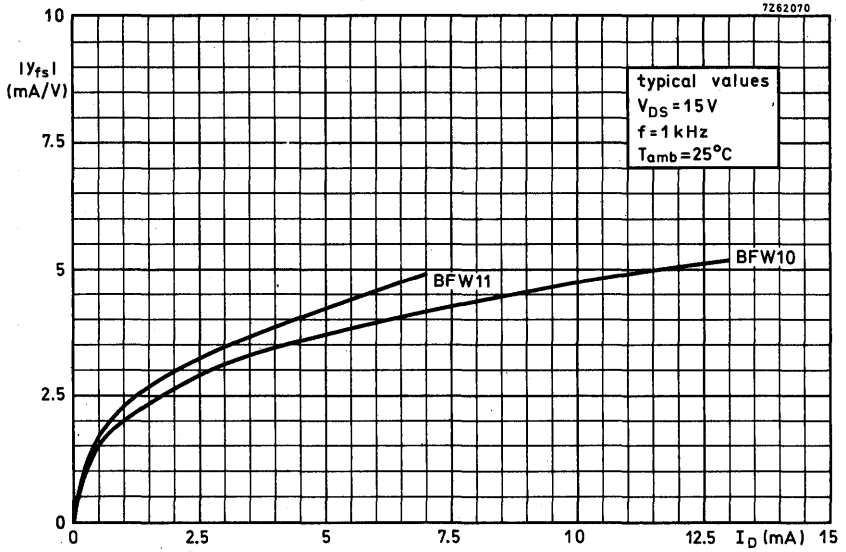

7Z08477
BFW10
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
$-V_{GS}$=0
1V
2V
3V
max
typ
min
20
15
10
5
8 $-V_{GS}$(V) 6
4
2
0
10 V_{DS}(V) 20

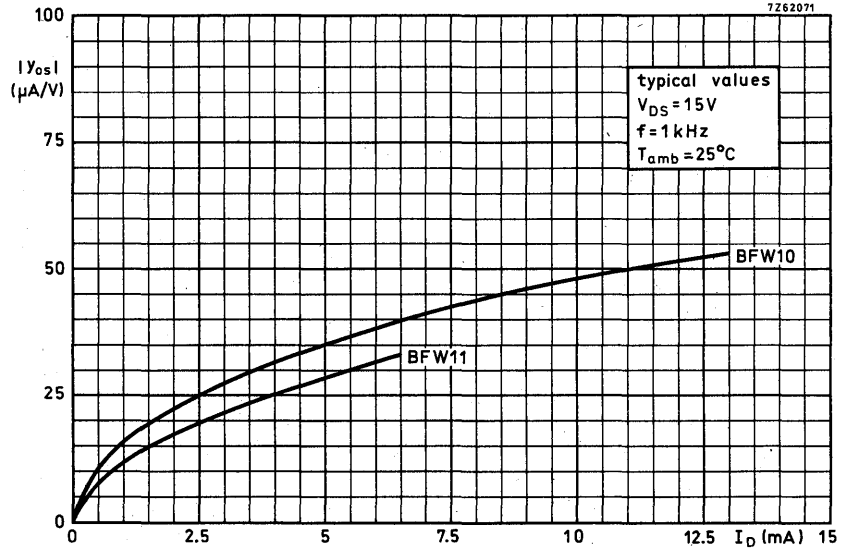

7Z08476
BFW11
V_{DS} = 15V
T_j = 25°C
I_D (mA)
typical values
$-V_{GS}$=0
0.5V
1V
1.5V
2V
max
typ
min
15
10
5
4 $-V_{GS}$(V) 2
0
10 V_{DS}(V) 20

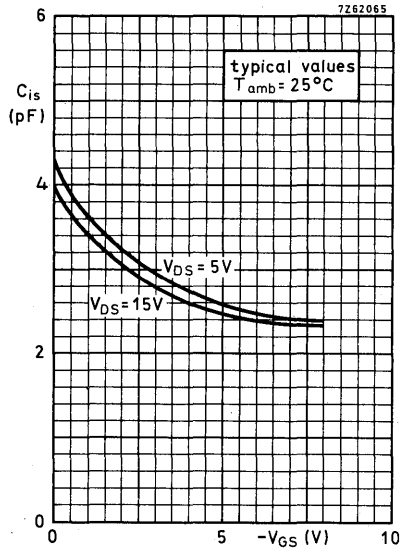

7Z08475
V_{DS} = 15V
typical values
BFW10
I_D (mA)
20
15
10
5
0
$-V_{GS}$ = 0
1V
2V
0
50
100
T_j (°C)
150

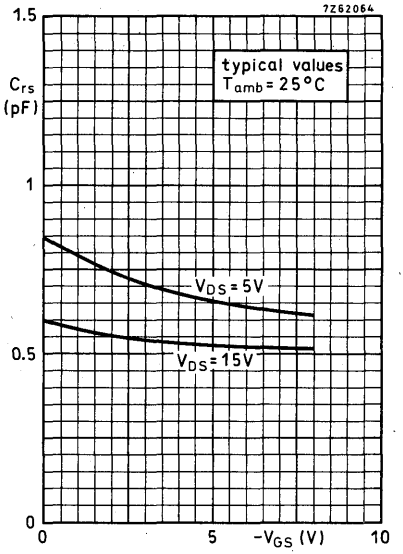

7Z08474
V_{DS} = 15V
typical values
BFW11
I_D (mA)
8
6
4
2
0
$-V_{GS}$ = 0
0.5V
1V
0
50
100
T_j (°C)
150

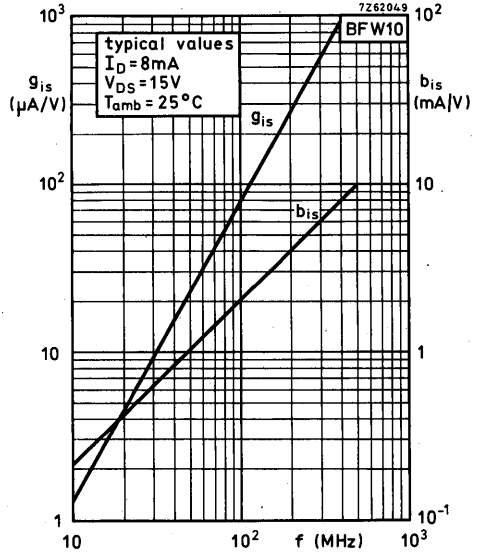

7Z62067
typical correlation between $-V_{(P)GS}$ and I_{DSS}
$-V_{(P)GS}$ at I_D = 0.5nA (V)
V_{DS} = 15V
T_j = 25°C
BFW10
BFW11
15
10
5
0
0
10
20
I_{DSS} at V_{GS} = 0 (mA)

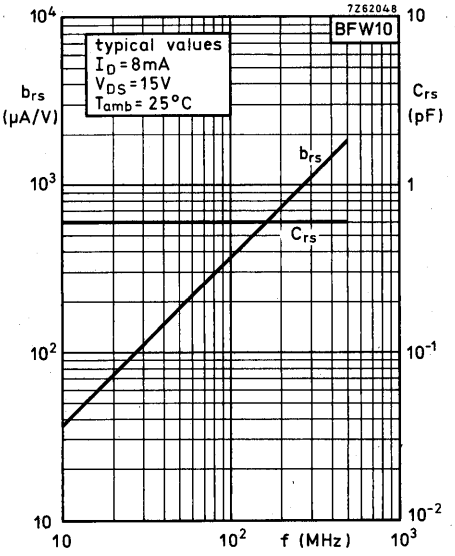

7Z62070
10
|yfs|
(mA/V)
7.5
5
2.5
0
typical values
VDS = 15V
f = 1 kHz
Tamb = 25°C
BFW10
BFW11
0
2.5
5
7.5
10
12.5
ID (mA)
15

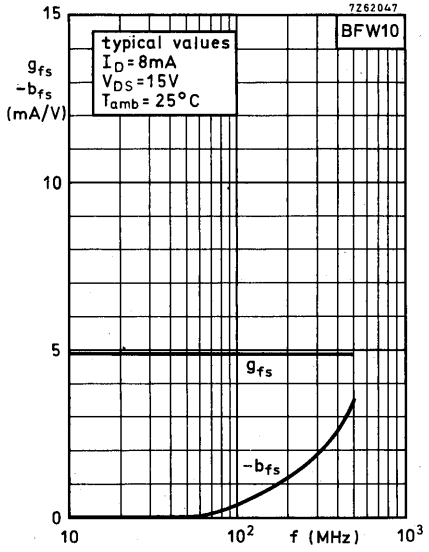

7Z62071
100
|yos|
(μA/V)
75
50
25
0
typical values
VDS = 15V
f = 1 kHz
Tamb = 25°C
BFW10
BFW11
0
2.5
5
7.5
10
12.5
ID (mA)
15

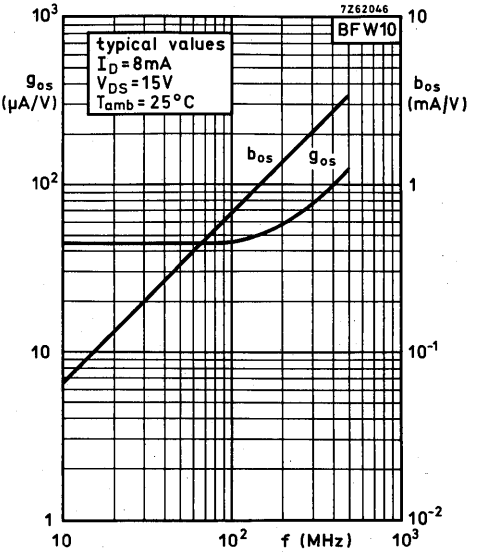

7Z62065
typical values
T_{amb} = 25 °C
C_{is} (pF)
6
4
2
0
V_{DS} = 5V
V_{DS} = 15V
0
5
$-V_{GS}$ (V)
10

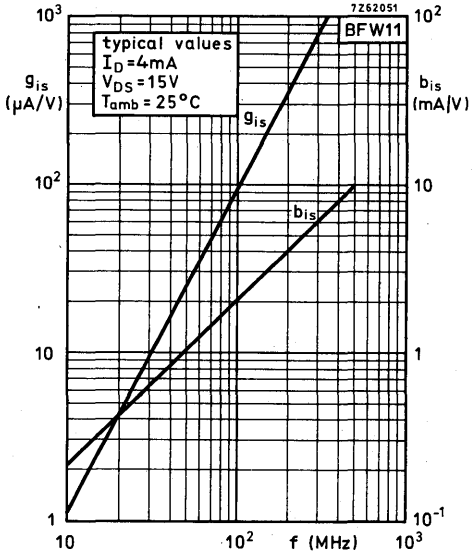

7Z62064
typical values
T_{amb} = 25 °C
C_{rs} (pF)
1.5
1
0.5
0
V_{DS} = 5V
V_{DS} = 15V
0
5
$-V_{GS}$ (V)
10

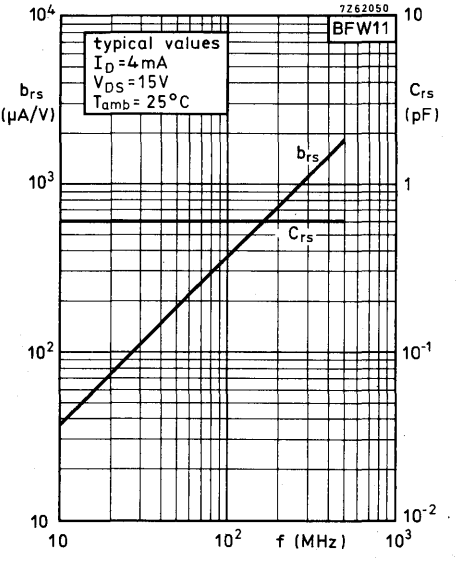

7Z62049
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
10^3
10^2
10
1
10^2
10
1
10^{-1}
10
10^2
f (MHz)
10^3

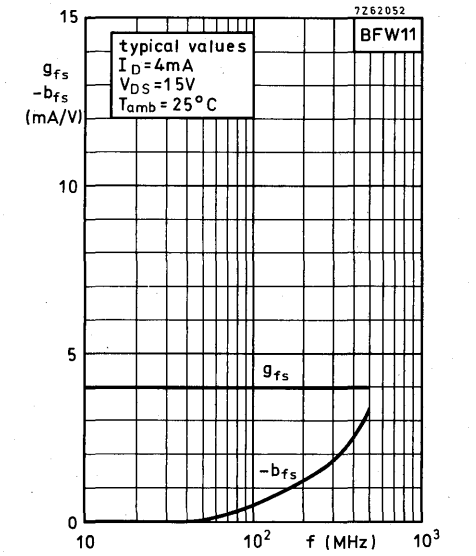

7Z62048
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
C_{rs} (pF)
b_{rs}
C_{rs}
10^4
10^3
10^2
10
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

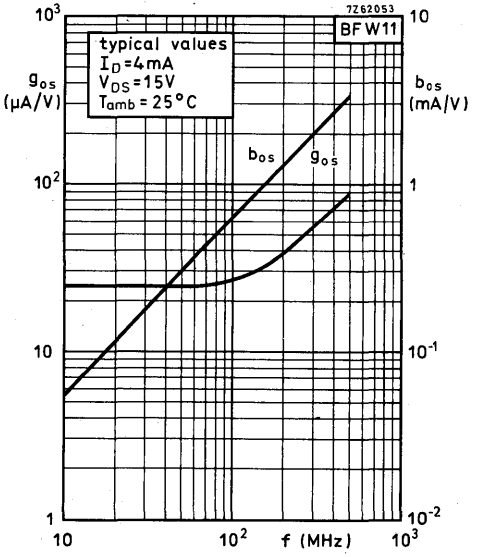

7Z62047
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs} $-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
15
10
5
0
10
10^2
f (MHz)
10^3

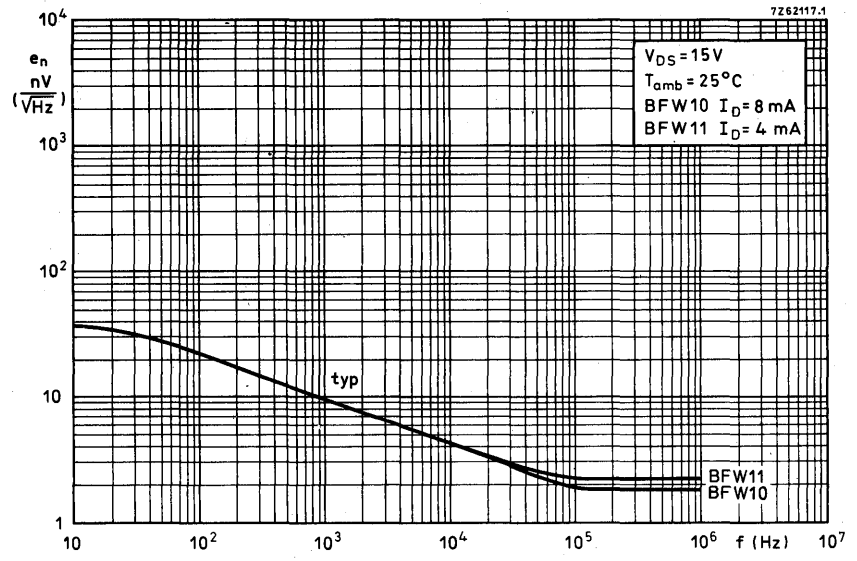

7Z62046
BFW10
typical values
I_D = 8mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
10^3
10^2
10
1
10
1
10^{-1}
10^{-2}
10
10^2
f (MHz)
10^3

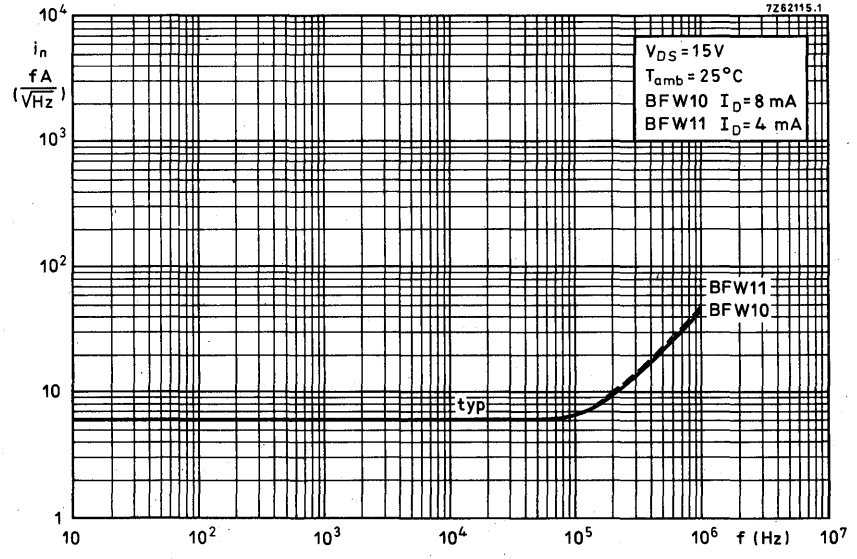

7Z62051
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
f (MHz)

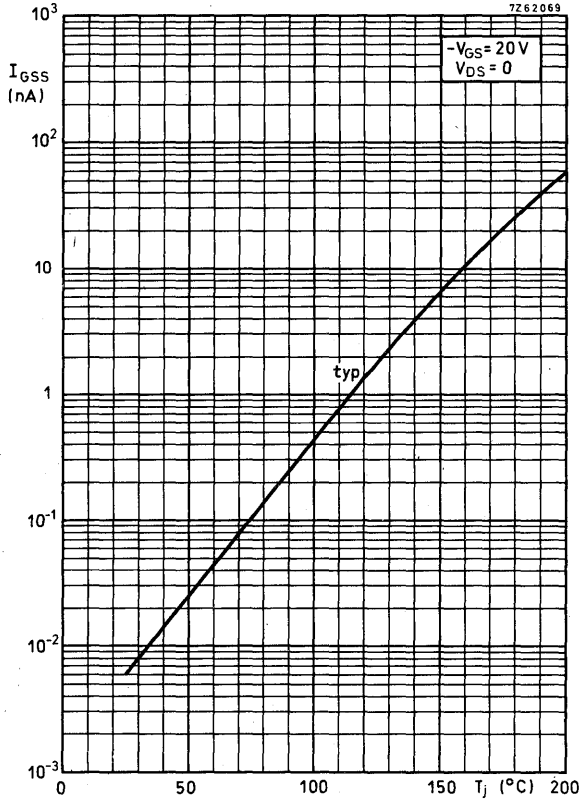

7Z62050
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
b_{rs} (μA/V)
C_{rs} (pF)
b_{rs}
C_{rs}
f (MHz)


7Z62052
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs} $-b_{fs}$ (mA/V)
g_{fs}
$-b_{fs}$
f (MHz)


7Z62053
BFW11
typical values
I_D = 4mA
V_{DS} = 15V
T_{amb} = 25°C
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
f (MHz)


7Z62117.1
10^4
e_n
$\frac{nV}{\sqrt{Hz}}$
10^3
10^2
10
1
V_{DS} = 15V
T_{amb} = 25°C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
typ
BFW11
BFW10
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62115.1
10^4
i_n
$\frac{fA}{\sqrt{Hz}}$
10^3
10^2
10
1
V_{DS} = 15V
T_{amb} = 25°C
BFW10 I_D = 8 mA
BFW11 I_D = 4 mA
BFW11
BFW10
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62069
$-V_{GS}$= 20 V
V_{DS} = 0
I_{GSS} (nA)
10^3
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
typ
0
50
100
150
T_j (°C)
200

N-CHANNEL SILICON FETS

Symmetrical n-channel silicon planar epitaxial junction field-effect transistors in TO-72 metal envelopes with the shield lead connected to the case. The transistors are intended for battery powered equipment and other low current-low voltage applications.

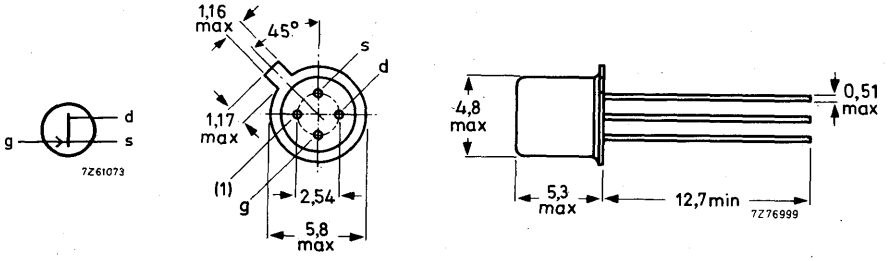
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30		V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30		V
Total power dissipation up to T_{amb} = 110 °C	P_{tot}	max.	150		mW
			BFW12	**BFW13**	
Drain current					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	1	0,2	mA
		<	5	1,5	mA
Gate-source cut-off voltage					
I_D = 0,5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2,5	1,2	V
Feedback capacitance at f = 1 MHz					
V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	0,80	0,80	pF
Transfer admittance (common source)					
V_{DS} = 15 V; I_D = 200 μA; f = 1 kHz	$\lvert y_{fs} \rvert$	>	0,5	0,5	mA/V
Equivalent noise voltage					
V_{DS} = 15 V; I_D = 200 μA					
B = 0,6 to 100 Hz	V_n	<	0,5	0,5	μV

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Currents				
Drain current	I_D	max.	10	mA
Gate current	I_G	max.	5	mA
Power dissipation				
Total power dissipation up to T_{amb} = 110 °C	P_{tot}	max.	150	mW
Temperatures				
Storage temperature	T_{stg}	−65 to	+200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

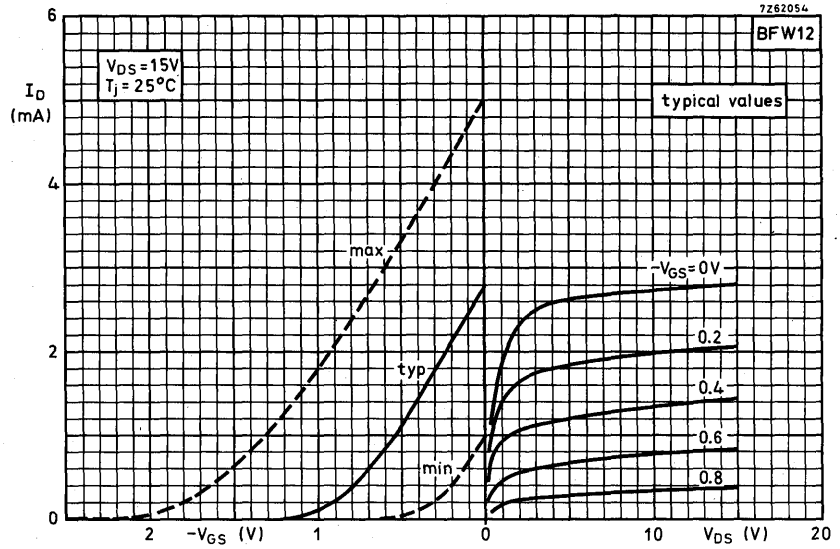
From junction to ambient	$R_{th\ j\text{-}a}$	=	0.59	°C/mW

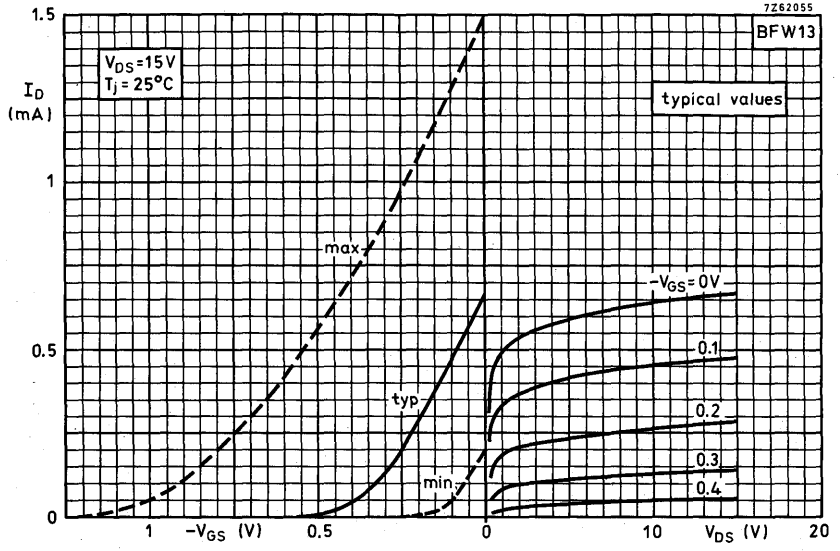
CHARACTERISTICS

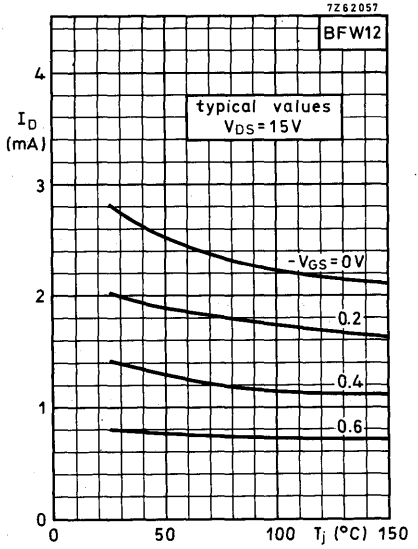
T_j = 25 °C unless otherwise specified

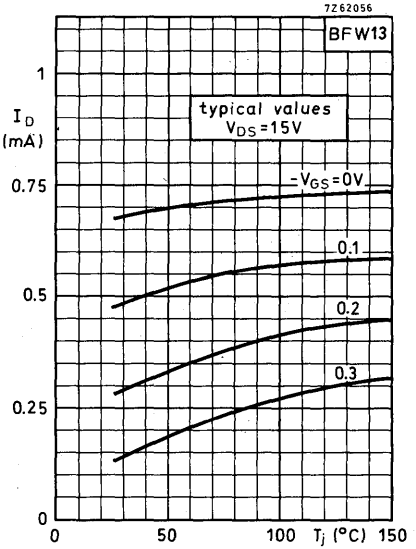
			BFW12	BFW13	
Gate cut-off current					
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	0.1	nA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.1	0.1	µA
Drain current [1]					
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	1	0.2	mA
		<	5	1.5	mA
Gate-source voltage					
I_D = 50 µA; V_{DS} = 15 V	$-V_{GS}$	>	0.5	0.1	V
		<	2.0	1.0	V
Gate-source cut-off voltage					
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	2.5	1.2	V
y parameters at f = 1 kHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Transfer admittance	$\|y_{fs}\|$	>	2.0	1.0	mA/V
Output admittance	$\|y_{os}\|$	<	30	10	µA/V
V_{DS} = 15 V; I_D = 500 µA					
Transfer admittance	$\|y_{fs}\|$	>	1.5	–	mA/V
Output admittance	$\|y_{os}\|$	<	10	–	µA/V
V_{DS} = 15 V; I_D = 200 µA					
Transfer admittance	$\|y_{fs}\|$	>	0.5	0.5	mA/V
Output admittance	$\|y_{os}\|$	<	5	5	µA/V
f = 1 MHz; T_{amb} = 25 °C					
V_{DS} = 15 V; V_{GS} = 0					
Input capacitance	C_{iss}	<	5	5	pF
Feedback capacitance	C_{rs}	<	0.80	0.80	pF
Equivalent noise voltage					
V_{DS} = 15 V; I_D = 200 µA; T_{amb} = 25 °C B = 0.6 to 100 Hz	V_n	<	0.5	0.5	µV

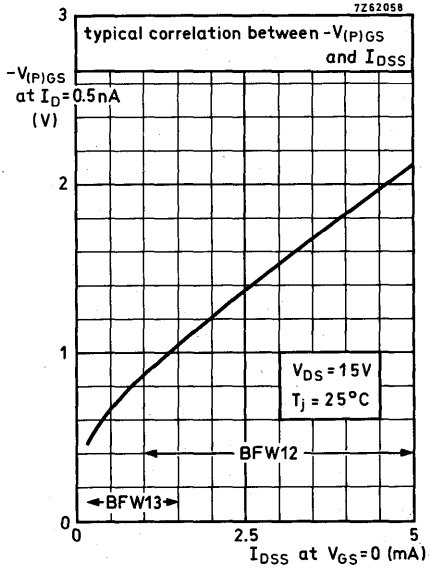
[1]) Measured under pulse conditions.

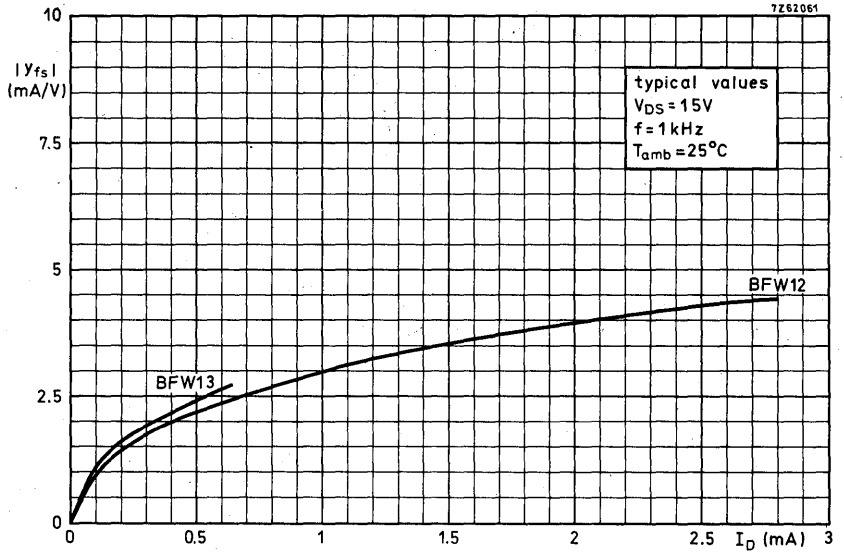

7Z62054
BFW12
V_{DS} = 15V
T_j = 25°C
typical values
I_D (mA)
6
4
2
0
max
typ
min
$-V_{GS}$ = 0V
0.2
0.4
0.6
0.8
2
$-V_{GS}$ (V)
1
0
10
V_{DS} (V)
20

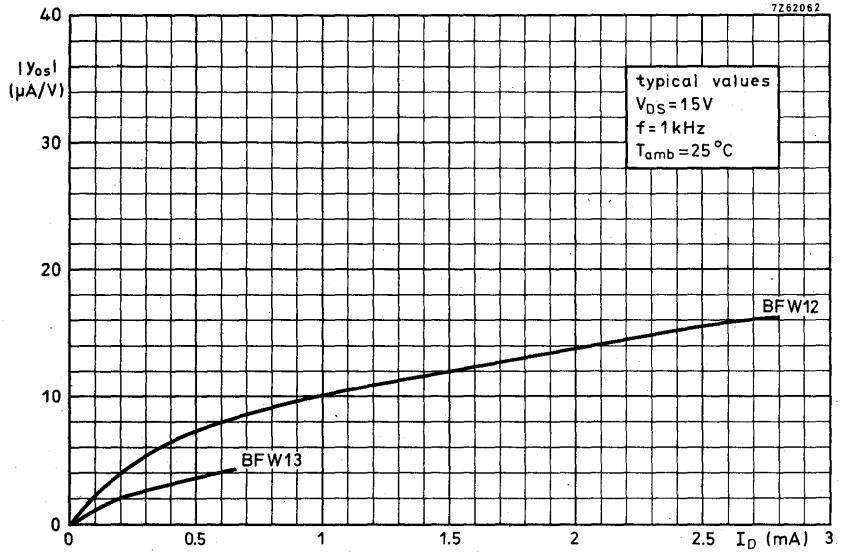

7Z62055
BFW13
V_{DS} = 15V
T_j = 25°C
typical values
I_D (mA)
1.5
1
0.5
0
max
typ
min
$-V_{GS}$ = 0V
0.1
0.2
0.3
0.4
1
$-V_{GS}$ (V)
0.5
0
10
V_{DS} (V)
20

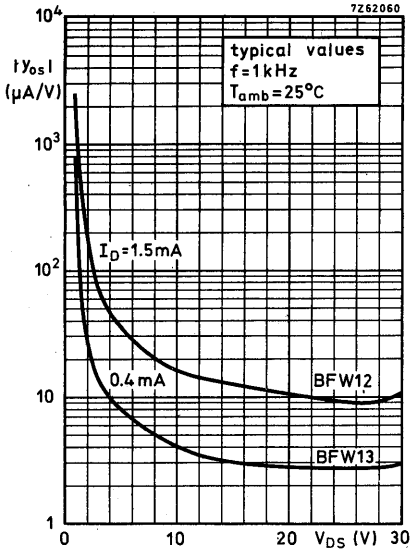

7Z62057
BFW12
typical values
V_{DS}=15V
I_D (mA)
4
3
2
1
0
-V_{GS}=0V
0.2
0.4
0.6
0
50
100
T_j (°C)
150

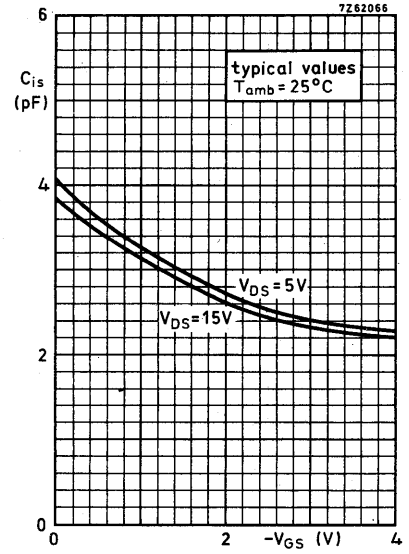

7Z62056
BFW13
typical values
V_{DS}=15V
I_D (mA)
1
0.75
0.5
0.25
0
-V_{GS}=0V
0.1
0.2
0.3
0
50
100
T_j (°C)
150

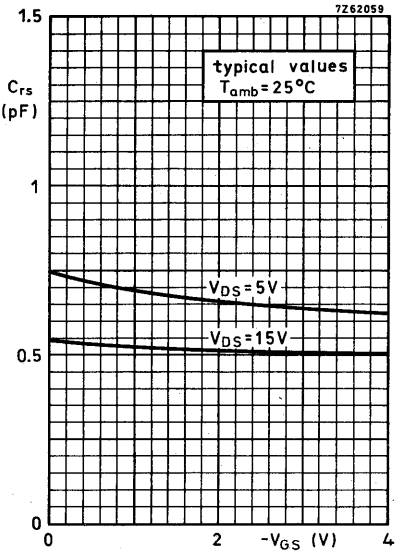

7Z62058
typical correlation between -$V_{(P)GS}$ and I_{DSS}
-$V_{(P)GS}$ at I_D=0.5nA (V)
3
2
1
0
V_{DS} = 15V
T_j = 25°C
BFW12
BFW13
0
2.5
5
I_{DSS} at V_{GS}=0 (mA)

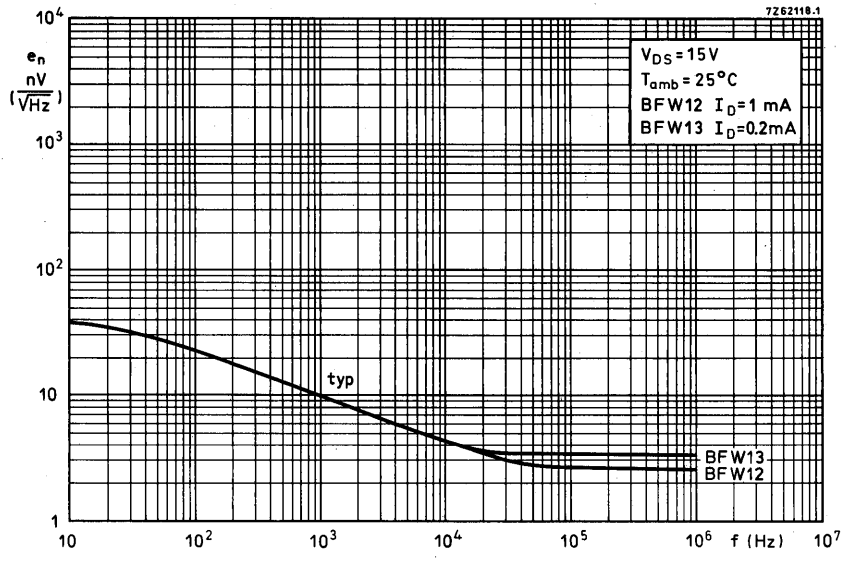

7Z62061
10
|yfs|
(mA/V)
7.5
5
2.5
0
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW12
BFW13
0
0.5
1
1.5
2
2.5
ID (mA)
3

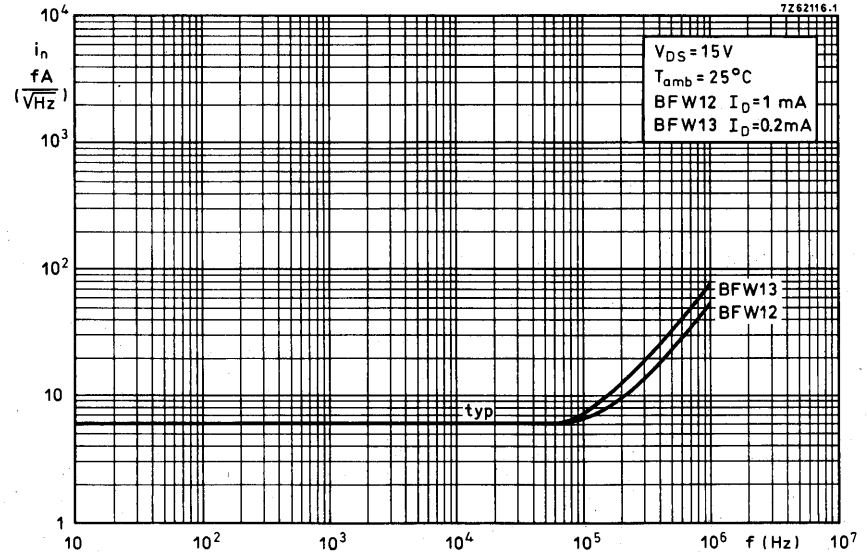

7Z62062
40
|yos|
(μA/V)
30
20
10
0
typical values
VDS = 15V
f = 1kHz
Tamb = 25°C
BFW12
BFW13
0
0.5
1
1.5
2
2.5
ID (mA)
3

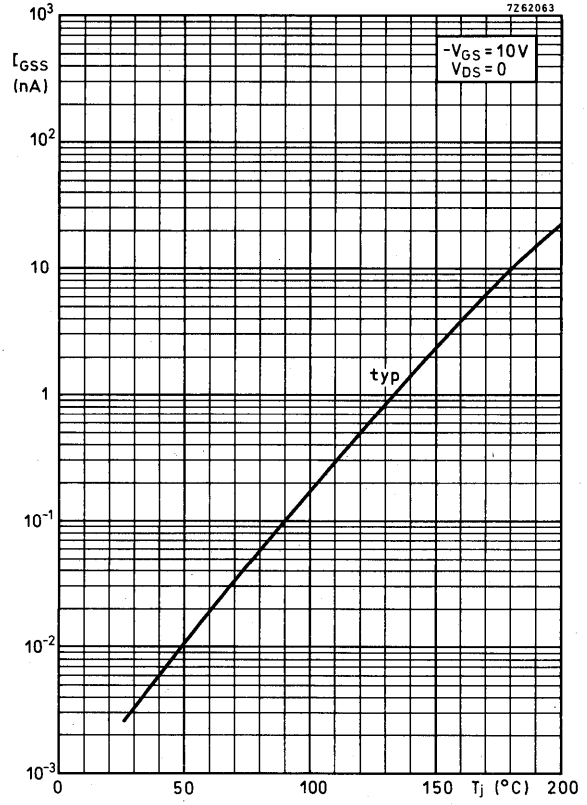

7Z62060
typical values
f=1kHz
T_{amb}=25°C
$|Y_{os}|$
(μA/V)
10^4
10^3
10^2
10
1
I_D=1.5mA
0.4mA
BFW12
BFW13
0
10
20
V_{DS} (V)
30


7Z62066
typical values
T_{amb}=25°C
C_{is}
(pF)
6
4
2
0
V_{DS}=5V
V_{DS}=15V
0
2
$-V_{GS}$ (V)
4


7Z62059
typical values
T_{amb}=25°C
C_{rs}
(pF)
1.5
1
0.5
0
V_{DS}=5V
V_{DS}=15V
0
2
$-V_{GS}$ (V)
4


7Z62118.1
e_n nV ($\sqrt{Hz}$)
10^4
10^3
10^2
10
1
V_{DS} = 15V
T_{amb} = 25°C
BFW12 I_D = 1 mA
BFW13 I_D = 0.2mA
typ
BFW13
BFW12
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62116.1
i_n fA ($\sqrt{Hz}$)
10^4
10^3
10^2
10
1
V_{DS} = 15V
T_{amb} = 25°C
BFW12 I_D = 1 mA
BFW13 I_D = 0.2mA
BFW13
BFW12
typ
10
10^2
10^3
10^4
10^5
10^6
f (Hz)
10^7


7Z62063
10^3
I_{GSS} (nA)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
$-V_{GS}$ = 10 V
V_{DS} = 0
typ
0
50
100
150
T_j (°C)
200

N-CHANNEL SILICON FET

Symmetrical n-channel silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is designed for general purpose amplifiers.

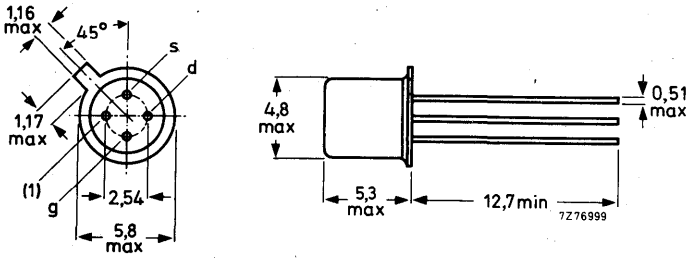
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 20	mA
Gate-source cut-off voltage I_D = 1,0 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	V
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	2,0	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 10 MHz	$\|y_{fs}\|$	>	1,6	mA/V

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	25	V
Drain-gate voltage (open source)	V_{DGO}	max.	25	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	25	V
Currents				
Drain current	I_D	max.	20	mA
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Temperatures				
Storage temperature	T_{stg}	−65 to +200		°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	0.59	°C/mW

CHARACTERISTICS T_j = 25 °C unless otherwise specified

Gate cut-off current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	1.0	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	1.0	μA
Drain current [1]				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	2 to	20	mA
Gate-source voltage				
I_D = 200 μA; V_{DS} = 15 V	$-V_{GS}$	0.5 to	7.5	V
Gate-source cut-off voltage				
I_D = 1.0 nA; V_{DS} = 15 V	$-V_{(P)GS}$	<	8	V
y parameters (common source)				
V_{DS} = 15 V; V_{GS} = 0				
f = 1 kHz Transfer admittance	$\lvert y_{fs} \rvert$	2.0 to	6.5	$m\Omega^{-1}$
Output admittance	$\lvert y_{os} \rvert$	<	85	$\mu\Omega^{-1}$
f = 1 MHz Input capacitance	C_{is}	<	6	pF
Feedback capacitance	C_{rs}	<	2.0	pF
f = 10 MHz Transfer admittance	$\lvert y_{fs} \rvert$	>	1.6	$m\Omega^{-1}$

[1]) Measured under pulsed conditions.

N-CHANNEL FETS

Silicon symmetrical n-channel junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for switching applications. The devices have the feature: low 'on' resistance at zero gate voltage.

QUICK REFERENCE DATA

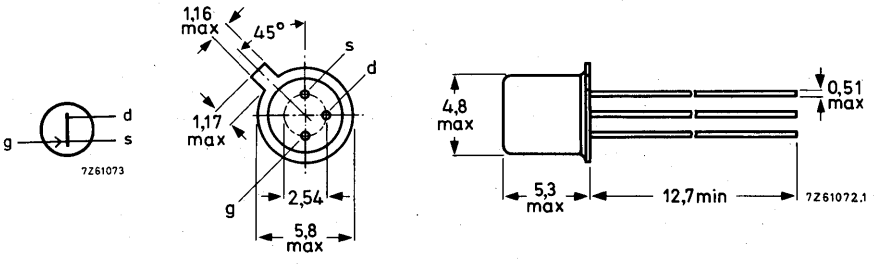
Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.		350		mW
			BSV78	**BSV79**	**BSV80**	
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage I_D = 1 nA; V_{GS} = 15 V	$-V_{(P)GS}$	>	3,75	2,0	1,0	V
		<	11	7,0	5,0	V
Drain-source resistance (on) at f = 1 kHz I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 10 V	C_{rs}	<	5	5	5	pF
Turn-on time	t_{on}	<	10	18	30	ns
Turn-off time	t_{off}	<	10	16	32	ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case



Accessories: 56246 (distance disc).

Products approved to CECC 50 012-011, available on request.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V
Forward gate current	I_G	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	350	mW
Storage temperature	T_{stg}	−65 to +	200	°C
Operating junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	430	K/W

CHARACTERISTICS T_j = 25 °C unless otherwise specified

Gate cut-off current

$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.25	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_j = 150 °C	$-I_{GSS}$	<	0.5	µA

Drain cut-off current

V_{DS} = 15 V; $-V_{GS}$ = 12 V	I_{DSX}	<	0.25	nA
V_{DS} = 15 V; $-V_{GS}$ = 12 V; T_j = 150 °C	I_{DSX}	<	0.5	µA

			BSV78	BSV79	BSV80	
Drain current						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	10	mA
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	3.75	2.0	1.0	V
		<	11	7.0	5.0	V
Gate-source voltage						
I_D = 1.5 µA; V_{DS} = 15 V	$-V_{GS}$	>	3.5	1.75	0.75	V
		<	10	6.0	4.0	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	500			mV
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<		400		mV
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<			325	mV
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$r_{ds\,on}$	<	25	40	60	Ω
y parameters at f = 1 MHz (common source)						
$-V_{GS}$ = 10 V; V_{DS} = 0						
Input capacitance	C_{is}	<	10	10	10	pF
Feedback capacitance	C_{rs}	<	5	5	5	pF

Switching times (see Fig. 2)

Turn-on time when switched from
$-V_{GSMoff}$ = 11 V to I_{Don} = 20 mA; V_{DD} = 10 V **(BSV78)**
$-V_{GSMoff}$ = 7 V to I_{Don} = 10 mA; V_{DD} = 10 V **(BSV79)**
$-V_{GSMoff}$ = 5 V to I_{Don} = 5 mA; V_{DD} = 10 V **(BSV80)**

		BSV78	BSV79	BSV80
delay time	t_d <	5	10	10 ns
rise time	t_r <	5	8	20 ns
turn-on time	t_{on} <	10	18	30 ns

Turn-off time when switched from
I_{Don} = 20 mA to $-V_{GSMoff}$ = 11 V; V_{DD} = 10 V **(BSV78)**
I_{Don} = 10 mA to $-V_{GSMoff}$ = 7 V; V_{DD} = 10 V **(BSV79)**
I_{Don} = 5 mA to $-V_{GSMoff}$ = 5 V; V_{DD} = 10 V **(BSV80)**

		BSV78	BSV79	BSV80
fall time	t_f <	6	11	24 ns
storage time	t_s <	4	5	8 ns
turn-off time	t_{off} <	10	16	32 ns

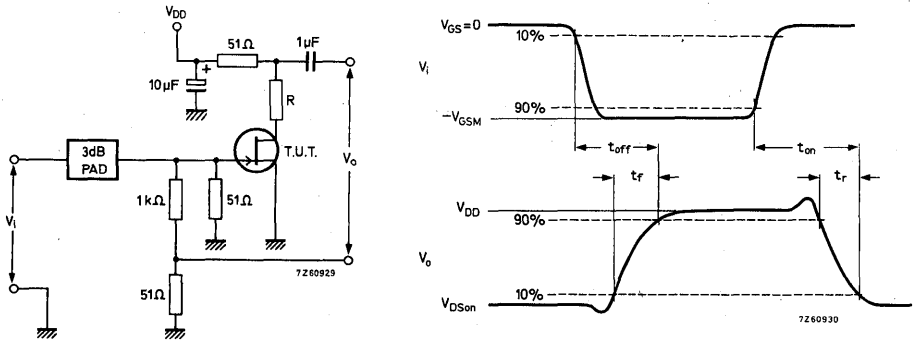


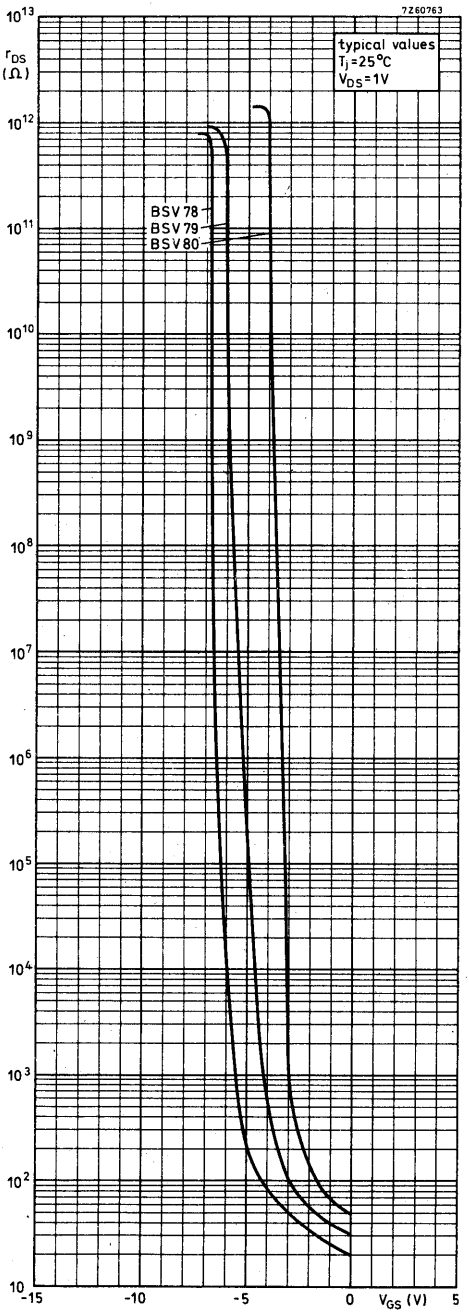
Fig. 2 Switching times test circuit and input and output waveforms.

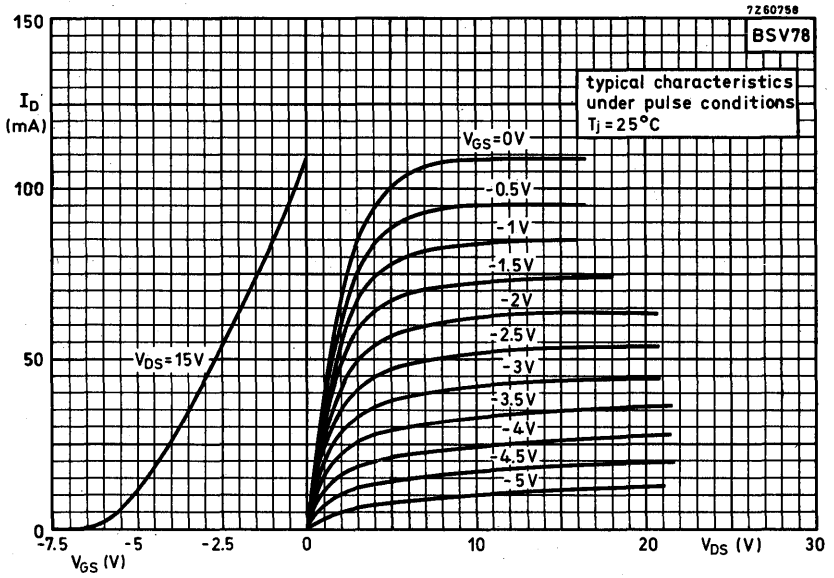
$$R = \frac{10 - V_{DSon}\,(V)}{I_{Don}\,(A)} - 51$$

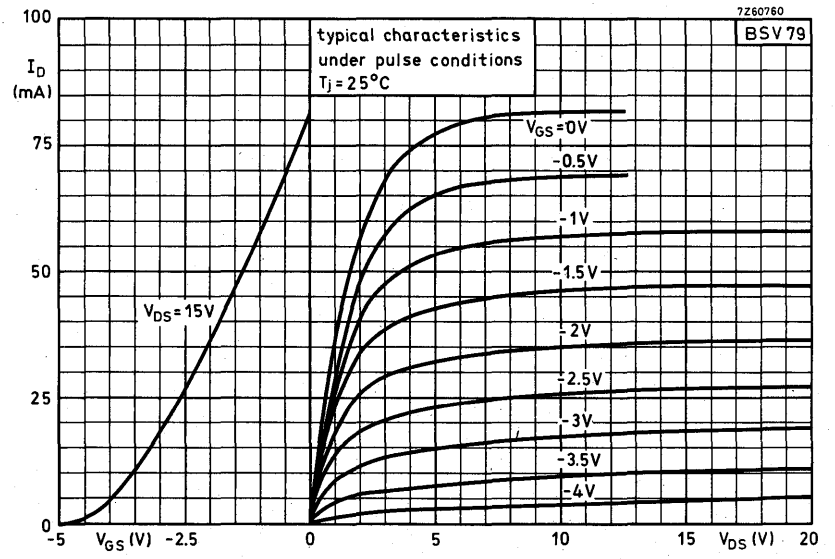
	BSV78	BSV79	BSV80
R =	424	909	1885 Ω

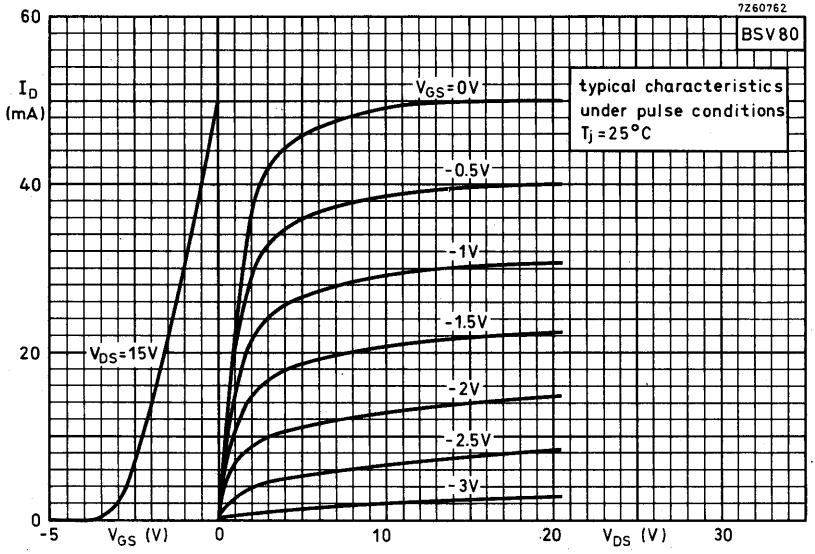
Pulse generator:
R_i = 50 Ω
t_r < 0,5 ns
t_f < 5 ns

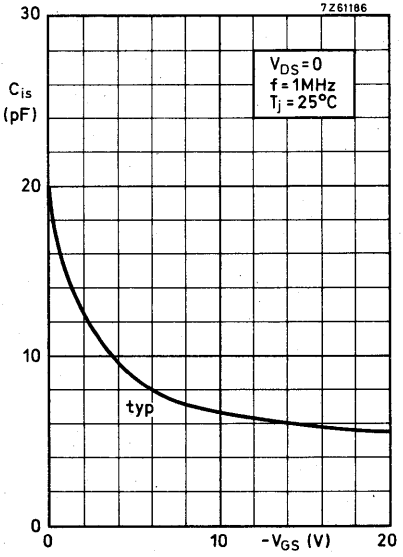
Oscilloscope:
R_i = 50 Ω
t_r < 1 ns
t_f < 1 ns

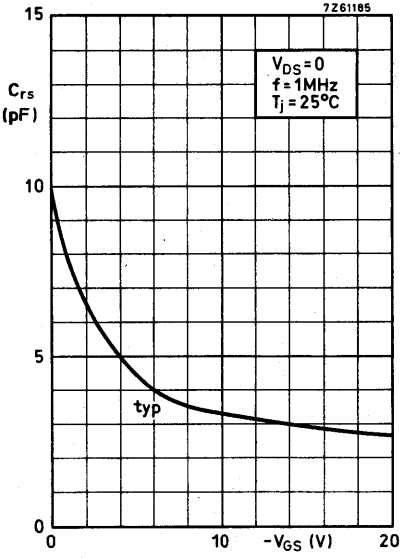

7Z60763
typical values
T_j=25°C
V_{DS}=1V
r_{DS} (Ω)
BSV 78
BSV 79
BSV 80
10^{13}
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
-15
-10
-5
0
V_{GS} (V)
5

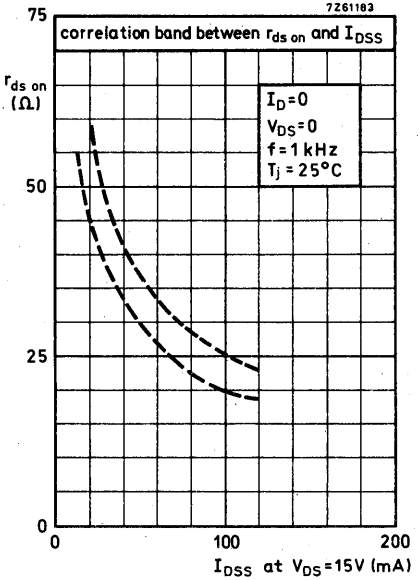

7Z60758
BSV78
typical characteristics
under pulse conditions
Tj = 25°C
ID (mA)
150
100
50
0
VGS=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V
-4.5V
-5V
VDS=15V
-7.5
-5
-2.5
0
10
20
30
VGS (V)
VDS (V)

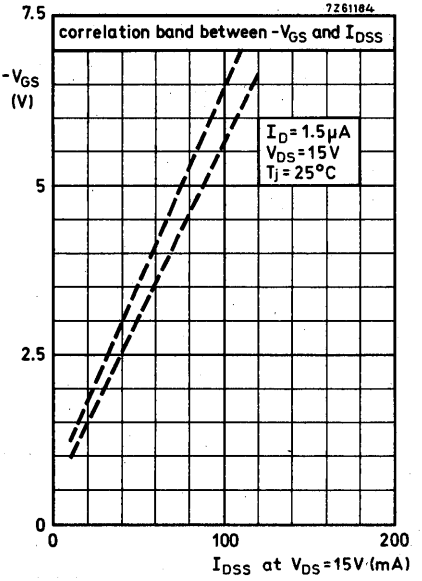

7Z60760
BSV79
typical characteristics
under pulse conditions
Tj = 25°C
ID (mA)
100
75
50
25
0
VGS=0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
-3.5V
-4V
VDS=15V
-5
VGS (V)
-2.5
0
5
10
15
20
VDS (V)


7Z60762
BSV80
typical characteristics
under pulse conditions
Tj = 25°C
ID (mA)
VGS = 0V
-0.5V
-1V
-1.5V
-2V
-2.5V
-3V
VDS = 15V
60
40
20
0
-5
VGS (V)
0
10
20
VDS (V)
30


7Z61186
VDS = 0
f = 1MHz
Tj = 25°C
Cis (pF)
typ
30
20
10
0
0
10
-VGS (V)
20


7Z61185
VDS = 0
f = 1MHz
Tj = 25°C
Crs (pF)
typ
15
10
5
0
0
10
-VGS (V)
20


7Z61183
correlation band between $r_{ds\ on}$ and I_{DSS}
I_D=0
V_{DS}=0
f=1 kHz
T_j=25°C
$r_{ds\ on}$ (Ω)
75
50
25
0
0
100
200
I_{DSS} at V_{DS}=15V (mA)


7Z61184
correlation band between $-V_{GS}$ and I_{DSS}
I_D=1.5μA
V_{DS}=15V
T_j=25°C
$-V_{GS}$ (V)
7.5
5
2.5
0
0
100
200
I_{DSS} at V_{DS}=15V (mA)

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon junction field-effect transistor, designed primarily for small-signal general purpose high-frequency amplifier applications. The 2N3822 features low gate leakage current and low input capacitance.

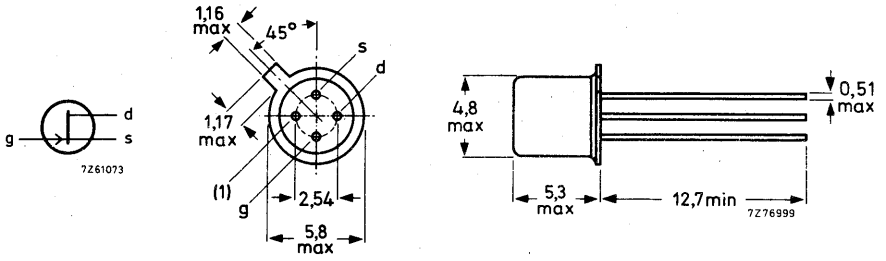
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	50	V
Gate-source voltage	$-V_{GS}$	max.	50	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 10	mA
Transfer admittance (common source)				
V_{DS} = 15 V; V_{GS} = 0; f = 1 kHz	$\|y_{fs}\|$		3,0 to 6,5	mA/V
V_{DS} = 15 V; V_{GS} = 0; f = 100 MHz	$\|y_{fs}\|$	>	3,0	mA/V

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) Shield lead connected to case.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	50	V
Drain-gate voltage	V_{DG}	max.	50	V
Gate-source voltage	$-V_{GS}$	max.	50	V
Gate current (d.c.)	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		−65 to + 200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590	K/W

CHARACTERISTICS with source connected to case for all measurements

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current				
$-V_{GS}$ = 30 V; V_{DS} = 0	$-I_{GSS}$	<	0,1	nA
$-V_{GS}$ = 30 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0,1	μA
Drain current *				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		2 to 10	mA
Gate-source breakdown voltage				
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	50	V
Gate-source voltage				
V_{DS} = 15 V; I_D = 200 μA	$-V_{GS}$		1 to 4	V
Gate-source cut-off voltage				
V_{DS} = 15 V; I_D = 0,5 nA	$-V_{(P)GS}$	<	6	V
Small-signal common source characteristics				
V_{DS} = 15 V; V_{GS} = 0				
Transfer admittance *				
f = 1 kHz	$\|y_{fs}\|$		3,0 to 6,5	mA/V
f = 100 MHz	$\|y_{fs}\|$	>	3,0	mA/V
Output admittance at f = 1 kHz *	$\|y_{os}\|$	<	20	μA/V
Input capacitance at f = 1 MHz	C_{is}	<	6	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	3	pF
Noise figure				
V_{DS} = 15 V; V_{GS} = 0; R_G = 1 MΩ				
f = 10 Hz; B = 5 Hz	F	<	5	dB
Equivalent input noise voltage				
V_{DS} = 15 V; V_{GS} = 0				
f = 10 Hz; B = 5 Hz	V_n	<	200	$nV/\sqrt{Hz}$

* Measured under pulse conditions: t_p = 100 ms; $\delta \leqslant 0{,}1$.

N-CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR

Symmetrical n-channel, depletion type, silicon planar epitaxial junction field-effect transistor in a TO-72 metal envelope, intended for v.h.f. amplifier and mixer applications in industrial service.

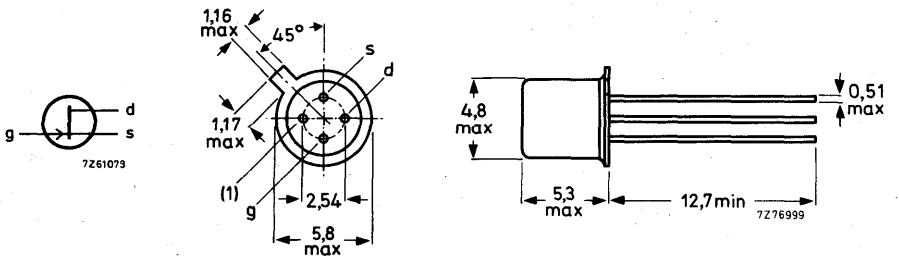
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage	$-V_{GS}$	max.	30	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		4 to 20	mA
Feedback capacitance at f = 1 MHz V_{DS} = 15 V; V_{GS} = 0	C_{rs}	<	2	pF
Transfer admittance (common source) V_{DS} = 15 V; V_{GS} = 0; f = 200 MHz	$\lvert Y_{fs} \rvert$	>	3,2	mA/V
Noise figure at f = 100 MHz V_{DS} = 15 V; V_{GS} = 0; R_G = 1 kΩ	F	<	2,5	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) Shield lead connected to case.

Accessories: 56246 (distance disc).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage	V_{DG}	max.	30	V
Gate-source voltage	$-V_{GS}$	max.	30	V
Gate current (d.c.)	I_G	max.	10	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Storage temperature	T_{stg}		−65 to + 200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	590	K/W

CHARACTERISTICS with source and shield connected to case for all measurements

T_{amb} = 25 °C unless otherwise specified

Gate cut-off current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0,5	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0,5	μA
Drain current *				
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		4 to 20	mA
Gate-source breakdown voltage				
$-I_G$ = 1 μA; V_{DS} = 0	$-V_{(BR)GSS}$	>	30	V
Gate-source voltage				
I_D = 400 μA; V_{DS} = 15 V	$-V_{GS}$		1,0 to 7,5	V
Gate-source cut-off voltage				
V_{DS} = 15 V; I_D = 0,5 nA	$-V_{(P)GS}$	<	8	V

Small-signal common source characteristics

V_{DS} = 15 V; V_{GS} = 0

Transfer admittance *				
f = 1 kHz	$\|y_{fs}\|$		3,5 to 6,5	mA/V
f = 200 MHz	$\|y_{fs}\|$	>	3,2	mA/V
Output admittance at f = 1 kHz *	$\|y_{os}\|$	<	35	μA/V
Input capacitance at f = 1 MHz	C_{is}	<	6	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	2	pF
Real part of input conductance at f = 200 MHz	$Re(y_{is})$	<	0,8	mA/V
Real part of output conductance at f = 200 MHz	$Re(y_{os})$	<	0,2	mA/V
Noise figure at f = 100 MHz				
V_{DS} = 15 V; V_{GS} = 0; R_G = 1 kΩ	F	<	2,5	dB

* Measured under pulse conditions: t_p = 100 ms; $\delta \leqslant 0{,}1$.

N-CHANNEL SILICON FET

Symmetrical n-channel planar epitaxial junction field-effect transistor in a TO-72 metal envelope with the shield lead connected to the case. The transistor is suitable in a variety of low power switching applications, e.g. in multiplexing systems.

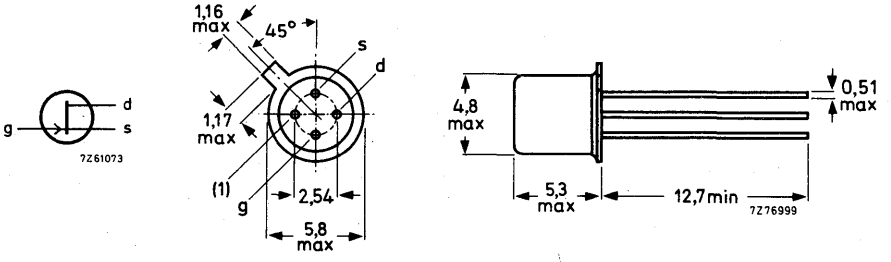
QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	2	mA
Gate-source cut-off voltage I_D = 10 nA; V_{DS} = 10 V	$-V_{(P)GS}$		4 to 6	V
Feedback capacitance at f = 1 MHz V_{DS} = 0; V_{GS} = 7 V	C_{rs}	<	1,5	pF
Drain-source resistance (on) at f = 1 kHz V_{GS} = 0; I_D = 0	$r_{ds\ on}$	<	220	Ω

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = shield lead connected to case

Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	30	V
Current				
Gate current	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Temperatures				
Storage temperature	T_{stg}	−55 to +200		°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	0.59	°C/mW

CHARACTERISTICS T_j = 25 °C unless otherwise specified

Gate cut-off current				
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.1	nA
Drain current				
V_{DG} = 20 V; I_S = 0	I_{DGO}	<	0.1	nA
V_{DG} = 20 V; I_S = 0; T_{amb} = 150 °C	I_{DGO}	<	0.2	µA
Drain current [1])				
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	2	mA
Gate-source breakdown voltage				
$-I_G$ = 1.0 µA; V_{DS} = 0	$-V_{(BR)GS}$	>	30	V
Gate-source voltage				
I_D = 10 nA; V_{DS} = 10 V	$-V_{(P)GS}$		4 to 6	V
Drain-source voltage				
I_D = 1.0 mA; V_{GS} = 0	V_{DS}	<	0.25	V
Drain cut-off current				
V_{DS} = 10 V; $-V_{GS}$ = 7.0 V	I_D	<	1.0	nA
V_{DS} = 10 V; $-V_{GS}$ = 7.0 V; T_{amb} = 150 °C	I_D	<	2.0	µA
Drain-source resistance (on) at f = 1 kHz				
V_{GS} = 0; I_D = 0	$r_{ds\ on}$	<	220	Ω
Input capacitance at f = 1 MHz				
V_{DS} = 20 V; V_{GS} = 0	C_{is}	<	6	pF
Feedback capacitance at f = 1 MHz				
V_{DS} = 0; V_{GS} = 7 V	C_{rs}	<	1.5	pF

CHARACTERISTICS (continued)

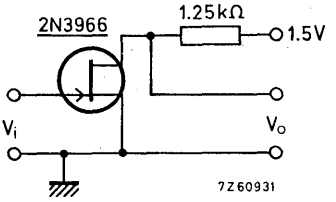
Switching times

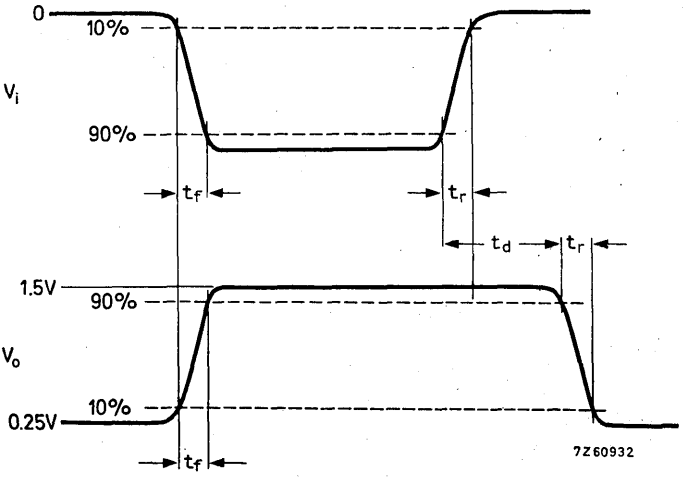
V_{DD} = 1.5 V; $I_{D\,on}$ = 1.0 mA

$V_{GS\,on}$ = 0; $-V_{GS\,off}$ = 6 V

delay time	t_d <	20	ns
rise time	t_r <	100	ns
turn off time	t_{off} <	100	ns

Test circuit:





Pulse generator:

t_r < 1.0 ns
t_f < 1.0 ns
t_p = 1.0 µs
δ < 0.5
R_S = 50 Ω

Oscilloscope:

t_r < 10 ns
R_i > 5 MΩ
C_i < 10 pF

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power switching applications in industrial service.

QUICK REFERENCE DATA

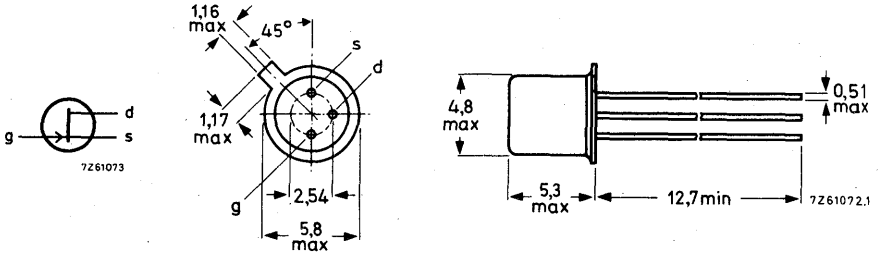
Drain-source voltage		$\pm V_{DS}$	max.	40		V
Total power dissipation up to T_{case} = 25 °C		P_{tot}	max	1,8		W
				2N4091	**2N4092**	**2N4093**
Drain current						
V_{DS} = 20 V; V_{GS} = 0		I_{DSS}	>	30	15	8 mA
Gate-source cut-off voltage			>	5,0	2,0	1,0 V
I_D = 1 nA; V_{DS} = 20 V		$-V_{(P)GS}$	<	10	7,0	5,0 V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0		$r_{ds\ on}$	<	30	50	80 Ω
Feedback capacitance at f = 1 MHz						
V_{DS} = 0; $-V_{GS}$ = 20 V		C_{rs}	<		5,0	pF
Turn-off time						
V_{DD} = 3,0 V; V_{GS} = 0						
I_D = 6,6 mA; $-V_{GSM}$ = 12 V	**2N4091**	t_{off}	<		40	ns
I_D = 4,0 mA; $-V_{GSM}$ = 8 V	**2N4092**	t_{off}	<		60	ns
I_D = 2,5 mA; $-V_{GSM}$ = 6 V	**2N4093**	t_{off}	<		80	ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case



Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	V
Current				
Forward gate current (d.c.)	I_G	max.	10	mA
Power dissipation				
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.8	W
Temperatures				
Storage temperature	T_{stg}	−55 to	+200	°C
Junction temperature	T_j	max.	200	°C

THERMAL RESISTANCE

From junction to case in free air	$R_{th\ j\text{-}c}$	=	0.1	°C/mW

CHARACTERISTICS T_{amb} = 25 °C unless otherwise specified

			2N4091	2N4092	2N4093	
Drain current						
V_{DG} = 20 V; I_S = 0	I_{DGO}	<		0.2		nA
V_{DG} = 20 V; I_S = 0; T_{amb} = 150 °C	I_{DGO}	<		0.4		µA
Source current						
V_{SG} = 20 V; I_D = 0	I_{SGO}	<		0.2		nA
Drain cut-off current						
V_{DS} = 20 V; $-V_{GS}$ = 12 V	I_{DSX}	<	0.2	–	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 8 V	I_{DSX}	<	–	0.2	–	nA
V_{DS} = 20 V; $-V_{GS}$ = 6 V	I_{DSX}	<	–	–	0.2	nA
V_{DS} = 20 V; $-V_{GS}$ = 12 V; T_{amb} = 150 °C	I_{DSX}	<	0.4	–	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 8 V; T_{amb} = 150 °C	I_{DSX}	<	–	0.4	–	µA
V_{DS} = 20 V; $-V_{GS}$ = 6 V; T_{amb} = 150 °C	I_{DSX}	<	–	–	0.4	µA
Gate-source breakdown voltage						
$-I_G$ = 1.0 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Drain current [1]						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	30	15	8	mA
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	5.0	2.0	1.0	V
		<	10	7.0	5.0	V
Drain-source voltage (on)						
I_D = 6.6 mA; V_{GS} = 0	V_{DSon}	<	0.2	–	–	V
I_D = 4.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.2	–	V
I_D = 2.5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.2	V
Drain-source resistance (on)						
I_D = 1.0 mA; V_{GS} = 0	r_{DSon}	<	30	50	80	Ω
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	$r_{ds\ on}$	<	30	50	80	Ω

[1]) Measured under pulsed conditions: $t_p \leq 300$ µs; $\delta \leq 0.03$

CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

y-parameters at f = 1 MHz (common source)

Input capacitance

V_{DS} = 20 V ; V_{GS} = 0	C_{is}	<	16	pF

Feedback capacitance

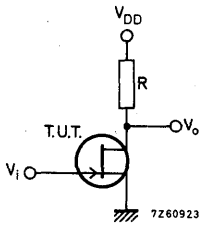
V_{DS} = 0 ; $-V_{GS}$ = 20 V	C_{rs}	<	5	pF

Switching times

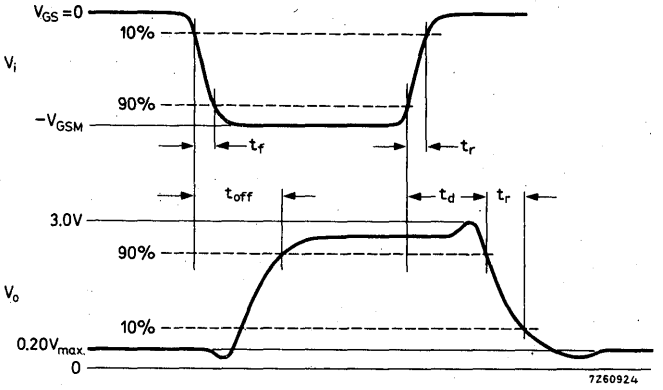
V_{DD} = 3,0 V; V_{GS} = 0

			2N4091	2N4092	2N4093	
	I_D	=	6,6	4,0	2,5	mA
	$-V_{GSM}$	=	12	8	6	V
Delay time	t_d	<	15	15	20	ns
Rise time	t_r	<	10	20	40	ns
Turn-off time	t_{off}	<	40	60	80	ns

Test circuit:



$$R = \frac{2,8}{I_D}$$



Pulse generator:

t_r	<	1	ns
t_f	<	1	ns
t_p	=	1,0	µs
δ	=	0,1	
R_S	=	50	Ω

Oscilloscope:

t_r	<	0,4	ns
R_i	>	9,8	MΩ
C_i	<	1,7	pF

N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, application in industrial service.

QUICK REFERENCE DATA

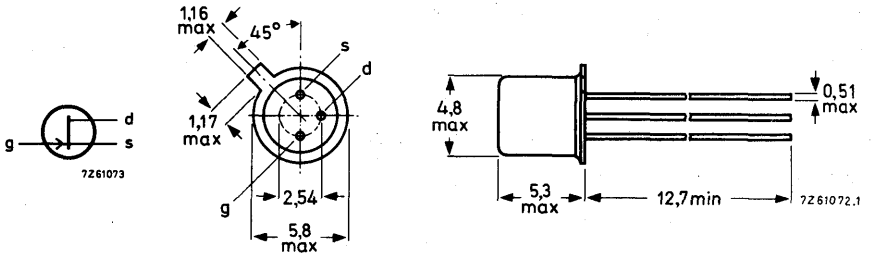
Drain-source voltage	$\pm V_{DS}$	max.		40		V
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.		1,8		W
			2N4391	**2N4392**	**2N4393**	
Drain current V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	25	5	mA
Gate-source cut-off voltage I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4,0	2,0	0,5	V
		<	10	5,0	3,0	V
Drain-source resistance (on) at f = 1 kHz I_D = 1 mA; V_{GS} = 0	$r_{ds\ on}$	<	30	60	100	Ω
Feedback capacitance at f = 1 MHz V_{DS} = 0; $-V_{GS}$ = 12 V **2N4391** V_{DS} = 0; $-V_{GS}$ = 7 V **2N4392** V_{DS} = 0; $-V_{GS}$ = 5 V **2N4393**	C_{rs}	<	3,5	3,5	3,5	pF
Turn-off time V_{DD} = 10 V; V_{GS} = 0						
I_D = 12 mA; $-V_{GSM}$ = 12 V	t_{off}	<	20	–	–	ns
I_D = 6,0 mA; $-V_{GSM}$ = 7 V	t_{off}	<	–	35	–	ns
I_D = 3,0 mA; $-V_{GSM}$ = 5 V	t_{off}	<	–	–	50	ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18.

Gate connected to case



Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages				
Drain-source voltage	$\pm V_{DS}$	max.	40	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	V
Gate-source voltage	$-V_{GSO}$	max.	40	V
Current				
Gate current (d.c.)	I_G	max.	50	mA
Power dissipation				
Total power dissipation up to T_{case} = 25 °C	P_{tot}	max.	1.8	W
Temperatures				
Storage temperature	T_{stg}	−65 to	200	°C
Junction temperature	T_j	max.	200	°C
Thermal resistance				
From junction to case in free air	$R_{th\ j\text{-}c}$	=	0.1	°C/mW

CHARACTERISTICS T_{amb} = 25 °C unless otherwise specified

Gate cut-off current						
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$ <			0.1		nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$ <			0.2		µA
Drain cut-off current		2N4391	2N4392	2N4393		
V_{DS} = 20 V; $-V_{GS}$ = 12 V	I_{DSX} <	0.1	–	–		nA
V_{DS} = 20 V; $-V_{GS}$ = 7 V	I_{DSX} <	–	0.1	–		nA
V_{DS} = 20 V; $-V_{GS}$ = 5 V	I_{DSX} <	–	–	0.1		nA
V_{DS} = 20 V; $-V_{GS}$ = 12 V; T_{amb} = 150 °C	I_{DSX} <	0.2	–	–		µA
V_{DS} = 20 V; $-V_{GS}$ = 7 V; T_{amb} = 150 °C	I_{DSX} <	–	0.2	–		µA
V_{DS} = 20 V; $-V_{GS}$ = 5 V; T_{amb} = 150 °C	I_{DSX} <	–	–	0.2		µA

CHARACTERISTICS (continued) T_{amb} = 25 °C unless otherwise specified

			2N4391	2N4392	2N4393	
Drain current [1]						
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	50	–	–	mA
		<	150	–	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	25	–	mA
		<	–	75	–	mA
V_{DS} = 20 V; V_{GS} = 0	I_{DSS}	>	–	–	5	mA
		<	–	–	30	mA
Gate-source breakdown voltage						
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$	>	40	40	40	V
Gate-source voltage						
I_G = 1 mA; V_{DS} = 0	V_{GSon}	<	1.0	1.0	1.0	V
Gate-source cut-off voltage						
I_D = 1 nA; V_{DS} = 20 V	$-V_{(P)GS}$	>	4.0	2.0	0.5	V
		<	10	5.0	3.0	V
Drain-source voltage (on)						
I_D = 12 mA; V_{GS} = 0	V_{DSon}	<	0.4	–	–	V
I_D = 6.0 mA; V_{GS} = 0	V_{DSon}	<	–	0.4	–	V
I_D = 3.0 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.4	V
Drain-source resistance (on)						
I_D = 1 mA; V_{GS} = 0	r_{DSon}	<	30	60	100	Ω
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	r_{dson}	<	30	60	100	Ω
y parameters at f = 1 MHz (common source)						
Input capacitance						
V_{DS} = 20 V; V_{GS} = 0	C_{is}	<	14	14	14	pF
Feedback capacitance						
$-V_{GS}$ = 12 V; V_{DS} = 0	C_{rs}	<	3.5	–	–	pF
$-V_{GS}$ = 7 V; V_{DS} = 0	C_{rs}	<	–	3.5	–	pF
$-V_{GS}$ = 5 V; V_{DS} = 0	C_{rs}	<	–	–	3.5	pF

[1]) measured under pulsed conditions: t_p = 100 µs; δ = 0.01

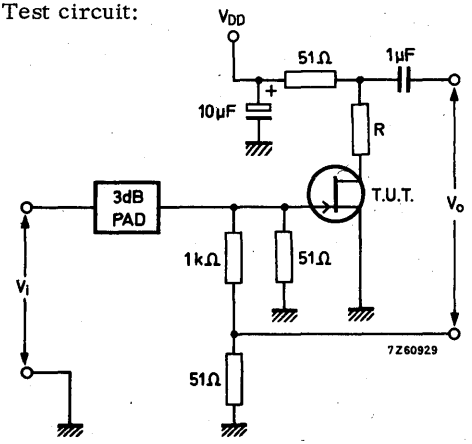
CHARACTERISTICS (continued) $T_{amb} = 25\,^{\circ}C$ unless otherwise specified

Switching times

$V_{DD} = 10\,V$; $V_{GS} = 0$

			2N4391	2N4392	2N4393	
	I_D	=	12	6.0	3.0	mA
	$-V_{GSM}$	=	12	7	5	V
Rise time	t_r	<	5	5	5	ns
Turn on time	t_{on}	<	15	15	15	ns
Fall time	t_f	<	15	20	30	ns
Turn off time	t_{off}	<	20	35	50	ns

Test circuit:



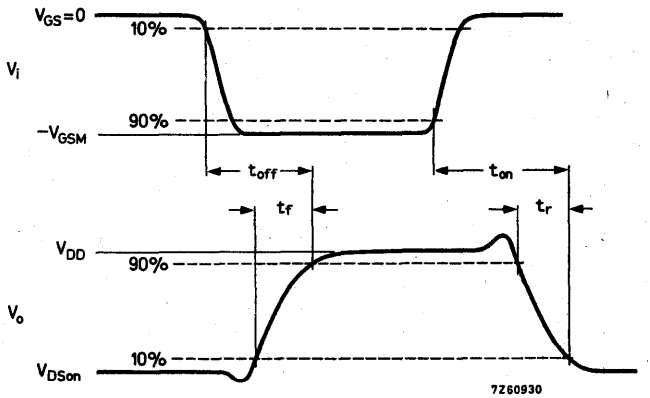
$$R = \frac{9.6}{I_D} - 51\,\Omega$$

Pulse generator:

t_r	<	0.5	ns
t_f	<	0.5	ns
t_p	=	100	μs
δ	=	0.01	

Oscilloscope:

R_i = 50 Ω



N-CHANNEL FETS

Silicon symmetrical n-channel depletion type junction field-effect transistors in TO-18 metal envelopes with the gate connected to the case. The transistors are intended for low power, chopper or switching, applications in industrial service.

QUICK REFERENCE DATA

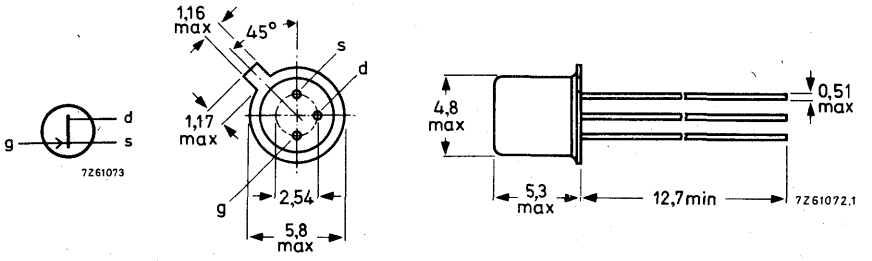
Drain-source voltage	**2N4856 to 2N4858**	$\pm V_{DS}$	max.		40		V
	2N4859 to 2N4861	$\pm V_{DS}$	max.		30		V
Total power dissipation up to T_{amb} = 25 °C		P_{tot}	max.		360		mW
				2N4856 2N4859	**2N4857 2N4860**	**2N4858 2N4861**	
Drain current							
V_{DS} = 15 V; V_{GS} = 0		I_{DSS}	>	50	20	8	mA
Gate-source cut-off voltage			>	4	2	0,8	V
I_D = 0,5 nA; V_{DS} = 15 V		$-V_{(P)GS}$	<	10	6	4	V
Drain-source resistance (on) at f = 1 kHz							
I_D = 0; V_{GS} = 0		$r_{ds\ on}$	<	25	40	60	Ω
Feedback capacitance at f = 1 MHz							
V_{DS} = 0; $-V_{GS}$ = 10 V		C_{rs}	<		8		pF
Turn-off time							
V_{DD} = 10 V; V_{GS} = 0							
I_D = 20 mA; $-V_{GSM}$ = 10 V	**2N4856; 2N4859**	t_{off}	<		25		ns
I_D = 10 mA; $-V_{GSM}$ = 6 V	**2N4857; 2N4860**	t_{off}	<		50		ns
I_D = 5 mA; $-V_{GSM}$ = 4 V	**2N4858; 2N4861**	t_{off}	<		100		ns

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-18

Gate connected to case



Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Voltages					
Drain-source voltage	$\pm V_{DS}$	max.	40	30	V
Drain-gate voltage (open source)	V_{DGO}	max.	40	30	V
Gate-source voltage (open drain)	$-V_{GSO}$	max.	40	30	V
Current					
Gate current (d.c.)	I_G	max.	50		mA
Power dissipation					
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	360		mW
Temperatures					
Storage temperature	T_{stg}		−65 to +200		°C
Junction temperature	T_j	max.	200		°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	0.49	°C/mW

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate cut-off current					
$-V_{GS}$ = 20 V; V_{DS} = 0	$-I_{GSS}$	<	0.25	–	nA
$-V_{GS}$ = 15 V; V_{DS} = 0	$-I_{GSS}$	<	–	0.25	nA
$-V_{GS}$ = 20 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	0.5	–	µA
$-V_{GS}$ = 15 V; V_{DS} = 0; T_{amb} = 150 °C	$-I_{GSS}$	<	–	0.5	µA
Drain cut-off current					
V_{DS} = 15 V; $-V_{GS}$ = 10 V	I_{DSX}	<	0.25	0.25	nA
V_{DS} = 15 V; $-V_{GS}$ = 10 V; T_{amb} = 150 °C	I_{DSX}	<	0.5	0.5	µA

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current [1]						
V_{DS} = 15 V; V_{GS} = 0	I_{DSS}	>	50	20	8	mA
	I_{DSS}	<	–	100	80	mA

			2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	
Gate-source breakdown voltage					
$-I_G$ = 1 µA; V_{DS} = 0	$-V_{(BR)GSS}$		40	30	V

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Gate-source cut-off voltage						
I_D = 0.5 nA; V_{DS} = 15 V	$-V_{(P)GS}$	>	4	2	0.8	V
		<	10	6	4	V
Drain-source voltage (on)						
I_D = 20 mA; V_{GS} = 0	V_{DSon}	<	0.75	–	–	V
I_D = 10 mA; V_{GS} = 0	V_{DSon}	<	–	0.50	–	V
I_D = 5 mA; V_{GS} = 0	V_{DSon}	<	–	–	0.50	V
Drain-source resistance (on) at f = 1 kHz						
I_D = 0; V_{GS} = 0	r_{dson}	<	25	40	60	Ω

[1]) measured under pulsed conditions: t_p = 100 ms; $\delta \leq 0.1$

y-parameters (common source)
$V_{DS} = 0$; $-V_{GS} = 10$ V; f = 1 MHz

Input capacitance	C_{is}	<	18	pF
Feedback capacitance	C_{rs}	<	8	pF

Switching times (see Figs 2 and 3)
$V_{DD} = 10$ V; $V_{GS} = 0$

			2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
Drain current	I_D	=	20	10	5	mA
Gate-source voltage (peak value)	$-V_{GSM}$	=	10	6	4	V
Delay time	t_d	<	6	6	10	ns
Rise time	t_r	<	3	4	10	ns
Turn-off time	t_{off}	<	25	50	100	ns

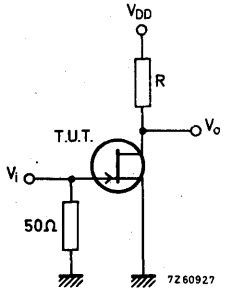


Fig. 2 Switching times test circuit.

	2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	
R =	464	953	1910	Ω

Pulse generator:
$t_r \leqslant$ 1 ns
$t_f \leqslant$ 1 ns
δ = 0,02
Z_o = 50 Ω

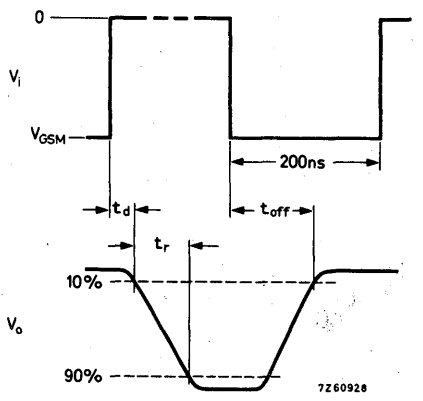


Fig. 3 Input and output waveforms.

Oscilloscope:
$t_r \leqslant$ 0,75 ns
$R_i \geqslant$ 1 MΩ
$C_i \leqslant$ 2,5 pF

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for use in u.h.f. applications in television tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

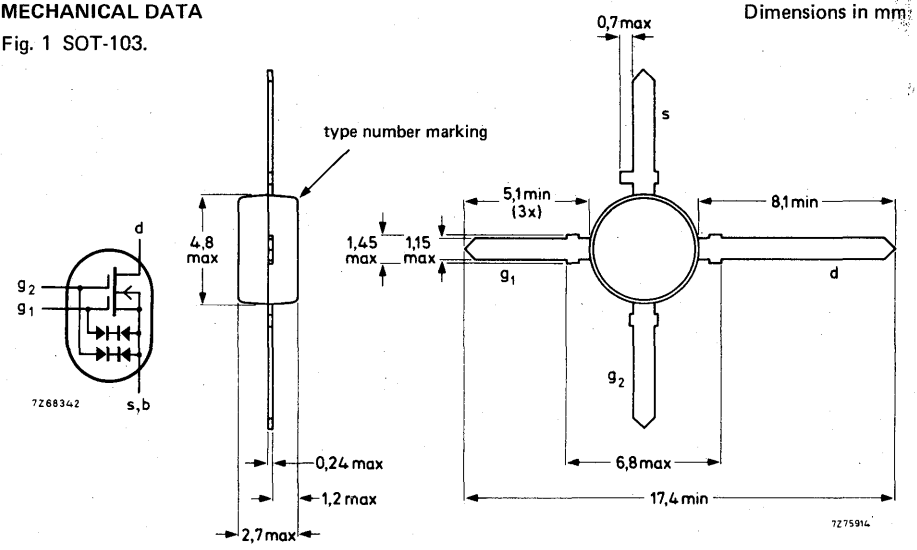
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current (peak value)	I_{DM}	max.	30	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	12	mA/V
Feedback capacitance at f = 1 MHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	25	fF
Noise figure at G_S = 2 mA/V I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; f = 800 MHz	F	typ.	2,8	dB
Power gain at f = 800 MHz I_D = 7 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V; G_S = 2 mA/V; G_L = 1 mA/V	G_p	typ.	16,5	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



RATINGS

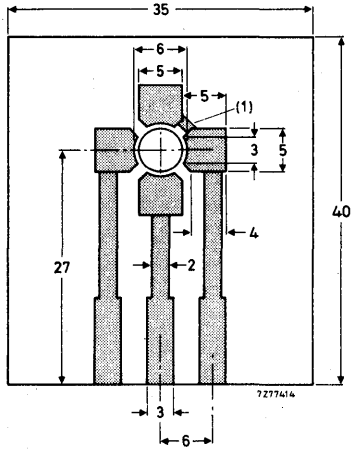
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	20	mA
Drain current (peak value)	I_{DM}	max.	30	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature	T_{stg}	−65 to +150		°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board	$R_{th\ j-a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_{amb} = 25 °C

Gate cut-off currents				
$\pm V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	50	nA
$\pm V_{G2-S} = 5$ V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	50	nA
Gate-source breakdown voltages				
$\pm I_{G1-SS} = 10$ mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$		6,0 to 20	V
$\pm I_{G2-SS} = 10$ mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$		6,0 to 20	V
Drain current*				
$V_{DS} = 10$ V; $V_{G1-S} = 0$; + $V_{G2-S} = 4$ V	I_{DSS}		2 to 20	mA
Gate-source cut-off voltages				
$I_D = 20\ \mu$A; $V_{DS} = 10$ V; + $V_{G2-S} = 4$ V	$-V_{(P)G1-S}$	<	2,7	V
$I_D = 20\ \mu$A; $V_{DS} = 10$ V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	2,7	V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 7$ mA; $V_{DS} = 10$ V; + $V_{G2-S} = 4$ V; T_{amb} = 25 °C

Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	>	9,5	mA/V
		typ.	12	mA/V
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	1,8	pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,0	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	25	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	0,9	pF
Noise figure at $G_S = 2$ mA/V				
f = 200 MHz	F	typ.	1,6	dB
f = 800 MHz	F	typ.	2,8	dB
Power gain at $G_S = 2$ mA/V				
$G_L = 0{,}5$ mA/V; f = 200 MHz	G_p	typ.	23	dB
$G_L = 1$ mA/V; f = 800 MHz	G_p	typ.	16,5	dB

DEVELOPMENT SAMPLE DATA

* Measured under pulse conditions.

SILICON N-CHANNEL DUAL GATE MOS-FET

Depletion type field-effect transistor in a plastic X-package with source and substrate interconnected, intended for v.h.f. applications, such as v.h.f. television tuners, f.m. tuners and professional communication equipment.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

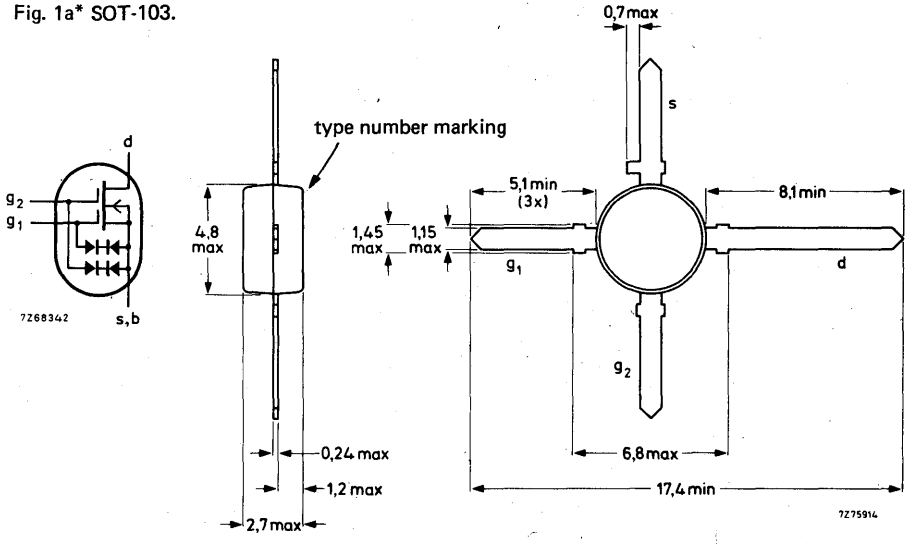
QUICK REFERENCE DATA

Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	20	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Junction temperature	T_j	max.	150	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	typ.	14	mA/V
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	20	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; $+V_{G2\text{-}S}$ = 4 V; f = 200 MHz	F	typ.	0,7	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1a* SOT-103.

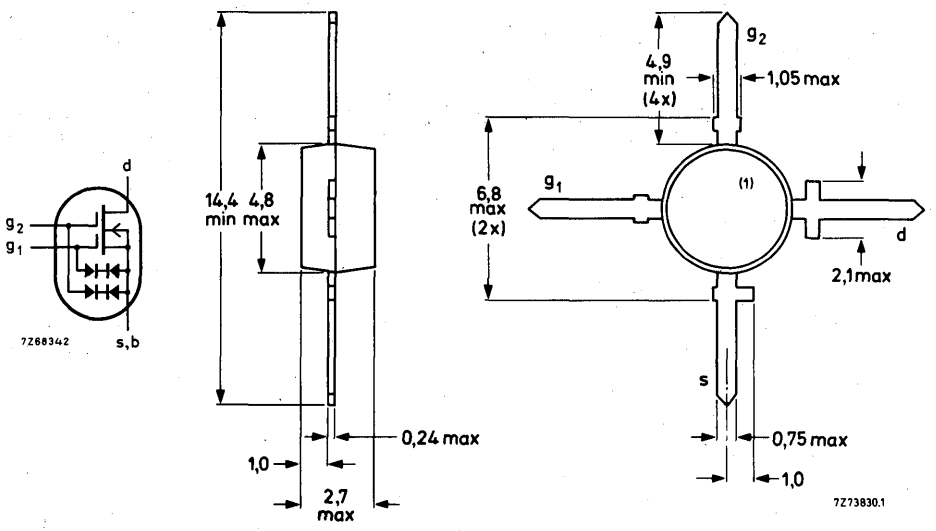


* This envelope will be introduced in the course of 1980, until then the BF981 will be supplied in a symmetrical X-package (Fig. 1b).

MECHANICAL DATA (continued)

Dimensions in mm

Fig. 1b SOT-103.



(1) = type number marking.

RATINGS

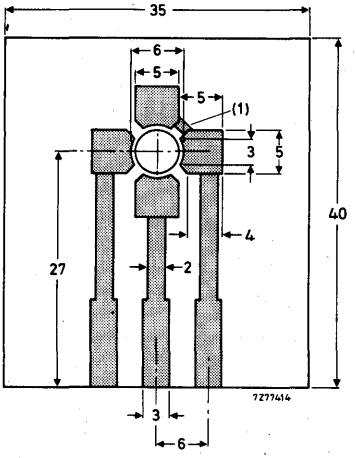
Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DS}	max.	20	V
Drain current (d.c. or average)	I_D	max.	20	mA
Drain current (peak value)	I_{DM}	max.	30	mA
Gate 1 - source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2 - source current	$\pm I_{G2-S}$	max.	10	mA
Total power dissipation up to T_{amb} = 75 °C	P_{tot}	max.	225	mW
Storage temperature	T_{stg}	−65 to +	150	°C
Junction temperature	T_j	max.	150	°C

THERMAL RESISTANCE

From junction to ambient in free air mounted on the printed-circuit board (see Fig. 2)	$R_{th\ j-a}$	=	335	K/W

Dimensions in mm



(1) Connection made by a strip or Cu wire.

Fig. 2 Single-sided 35 μm Cu-clad epoxy fibre-glass printed-circuit board, thickness 1,5 mm. Tracks are fully tin-lead plated. Board in horizontal position for R_{th} measurement.

STATIC CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

Gate cut-off currents			
$\pm V_{G1-S} = 5$ V; $V_{G2-S} = V_{DS} = 0$	$\pm I_{G1-SS}$	<	50 nA
$\pm V_{G2-S} = 5$ V; $V_{G1-S} = V_{DS} = 0$	$\pm I_{G2-SS}$	<	50 nA
Gate-source breakdown voltages			
$\pm I_{G1-SS} = 10$ mA; $V_{G2-S} = V_{DS} = 0$	$\pm V_{(BR)G1-SS}$	>	6 V
$\pm I_{G2-SS} = 10$ mA; $V_{G1-S} = V_{DS} = 0$	$\pm V_{(BR)G2-SS}$	>	6 V
Drain current			
$V_{DS} = 10$ V; $V_{G1-S} = 0$; $+V_{G2-S} = 4$ V; $T_j = 25$ °C	I_{DSS}		4 to 25 mA
Gate-source cut-off voltages			
$I_D = 20$ μA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V	$-V_{(P)G1-S}$	<	2,5 V
$I_D = 20$ μA; $V_{DS} = 10$ V; $V_{G1-S} = 0$	$-V_{(P)G2-S}$	<	2,5 V

DYNAMIC CHARACTERISTICS

Measuring conditions (common source): $I_D = 10$ mA; $V_{DS} = 10$ V; $+V_{G2-S} = 4$ V; $T_{amb} = 25$ °C

Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	10 mA/V
		typ.	14 mA/V
Input capacitance at gate 1; f = 1 MHz	C_{ig1-s}	typ.	2,1 pF
Input capacitance at gate 2; f = 1 MHz	C_{ig2-s}	typ.	1,0 pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	20 fF
Output capacitance at f = 1 MHz	C_{os}	typ.	1,1 pF
Noise figure at f = 100 MHz; $G_S = 1$ mA/V	F	typ.	0,7 dB
		<	1,7 dB
Noise figure at f = 200 MHz; $G_S = 2$ mA/V	F	typ.	1,0 dB
		<	2,0 dB
Transducer gain at f = 100 MHz; $G_S = 1$ mA/V; $G_L = 0{,}5$ mA/V	G_{tr}	typ.	29 dB
Transducer gain at f = 200 MHz; $G_S = 2$ mA/V; $G_L = 0{,}5$ mA/V	G_{tr}	typ.	26 dB

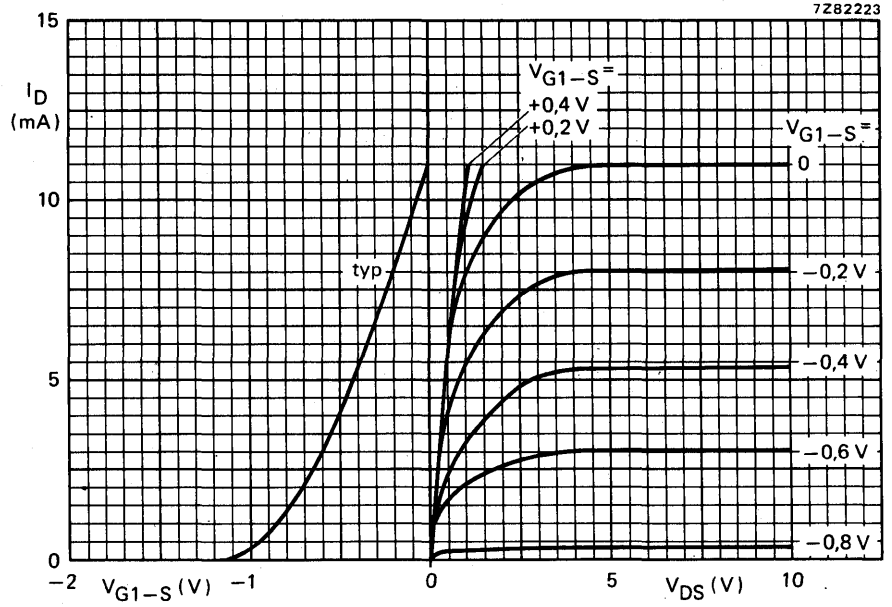


Fig. 3 **Left-hand graph:** V_{DS} = 10 V; V_{G2-S} = + 4 V; T_{amb} = 25 °C. **Right-hand graph:** V_{G2-S} = + 4 V; T_{amb} = 25 °C.

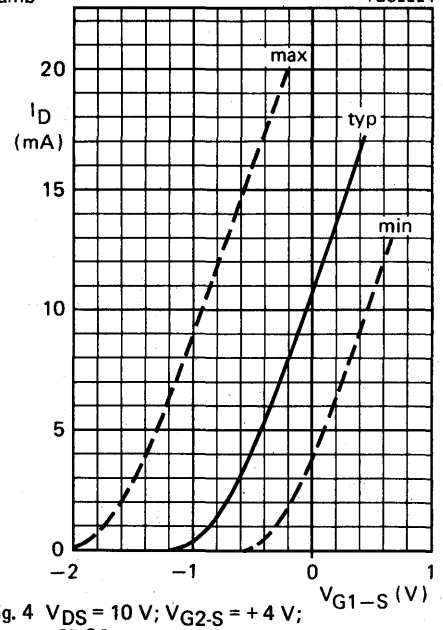


Fig. 4 V_{DS} = 10 V; V_{G2-S} = + 4 V; T_{amb} = 25 °C.

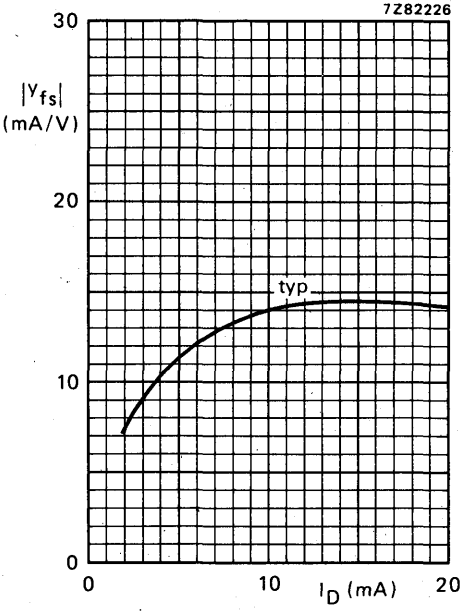


Fig. 5 V_{DS} = 10 V; V_{G2-S} = + 4 V; f = 1 kHz; T_{amb} = 25 °C.

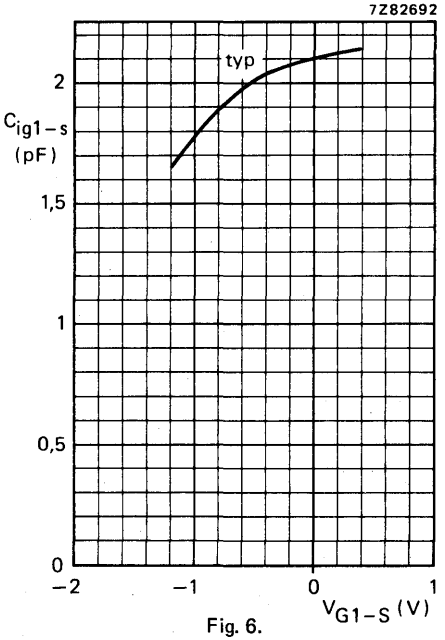


Fig. 6.

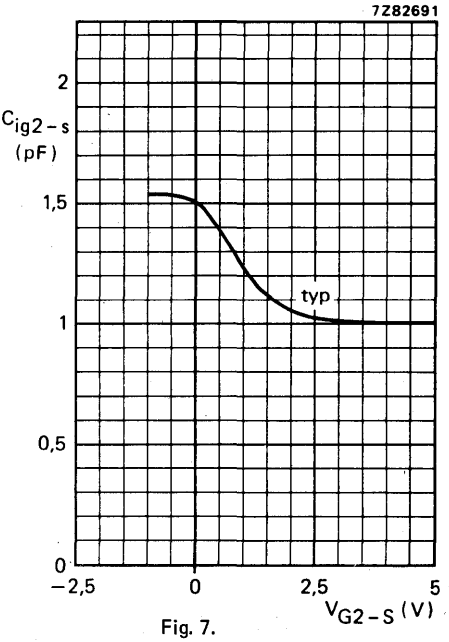


Fig. 7.

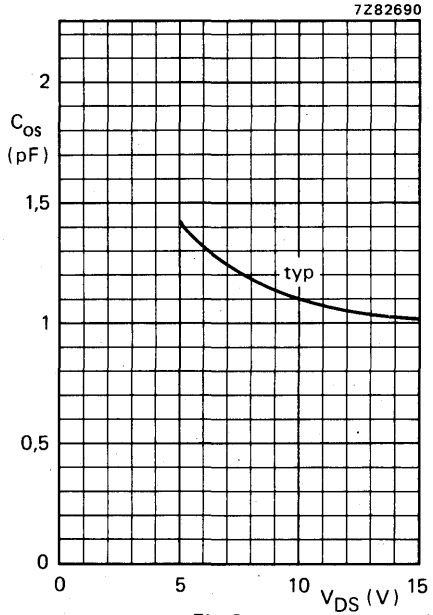


Fig. 8.

Measuring conditions:

Fig. 6 V_{DS} = 10 V; V_{G2-S} = + 4 V; f = 1 MHz; T_{amb} = 25 °C.

Fig. 7 V_{DS} = 10 V; V_{G1-S} = 0; f = 1 MHz; T_{amb} = 25 °C.

Fig. 8 V_{G2-S} = + 4 V; I_D = 10 mA; f = 1 MHz; T_{amb} = 25 °C.

Measuring conditions for Figs 9 to 12: V_{DS} = 10 V; I_D = 10 mA; V_{G2-S} = + 4 V; T_{amb} = 25 °C.

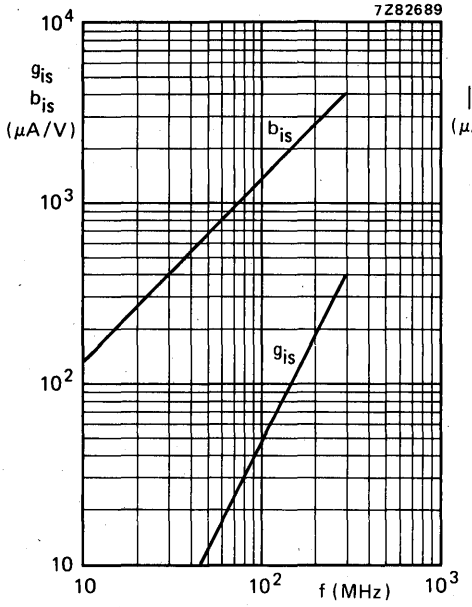


Fig. 9.

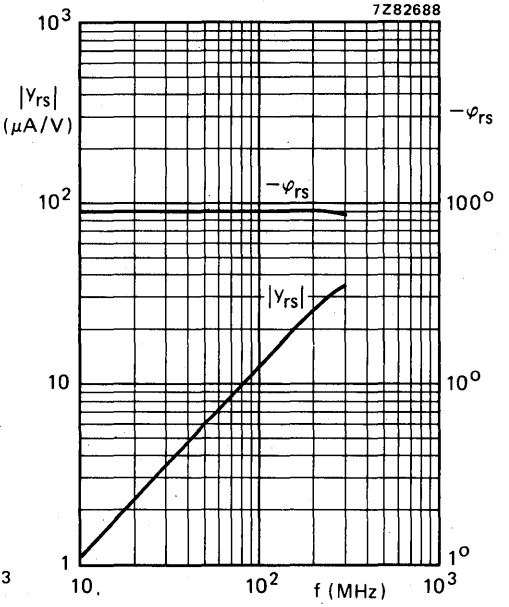


Fig. 10.

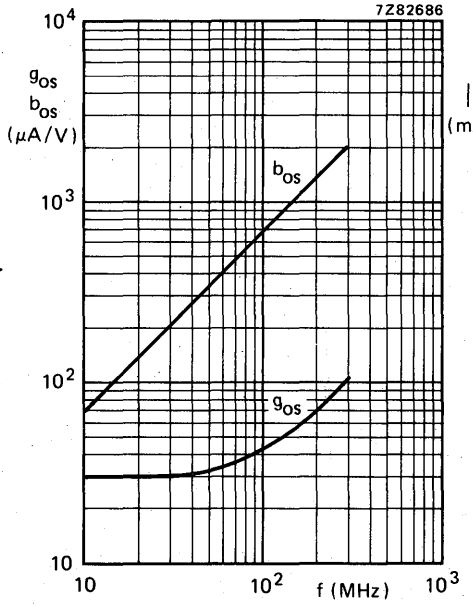


Fig. 11.

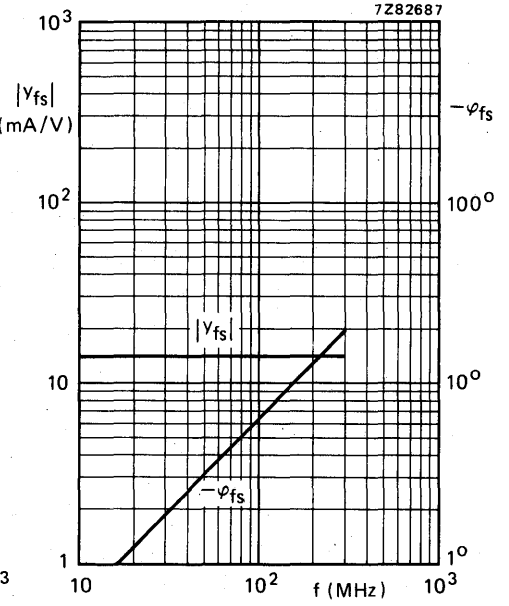


Fig. 12.

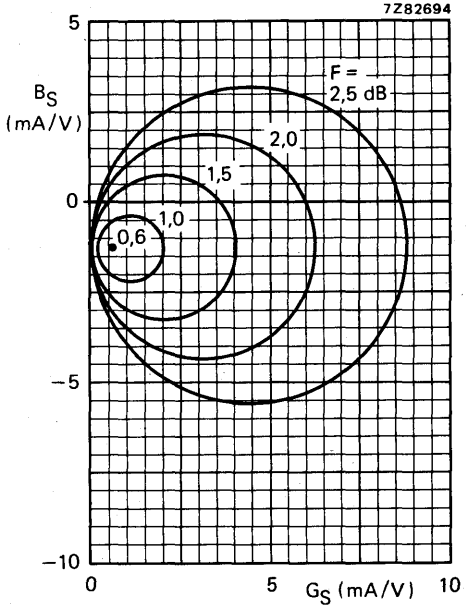


Fig. 13 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 100 MHz; T_{amb} = 25 °C; circles of typical constant noise figures.

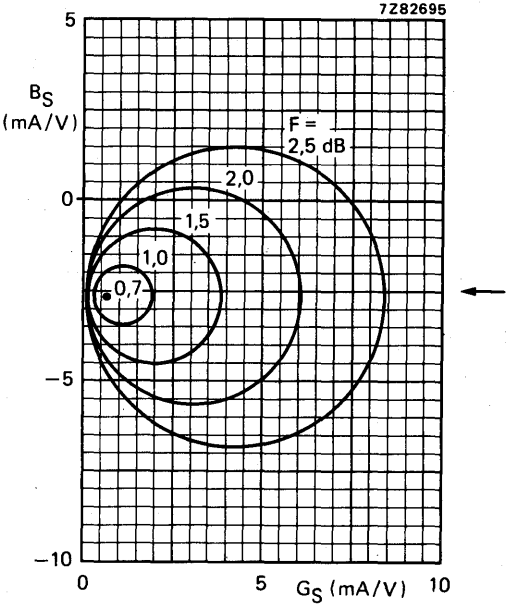


Fig. 14 V_{DS} = 10 V; $V_{G2\text{-}S}$ = + 4 V; I_D = 10 mA; f = 200 MHz; T_{amb} = 25 °C; circles of typical constant noise figures.

Measuring conditions for Figs 9 to 12: V_{DS} = 10 V; I_D = 10 mA; $V_{G2\text{-}S}$ = + 4 V; T_{amb} = 25 °C.

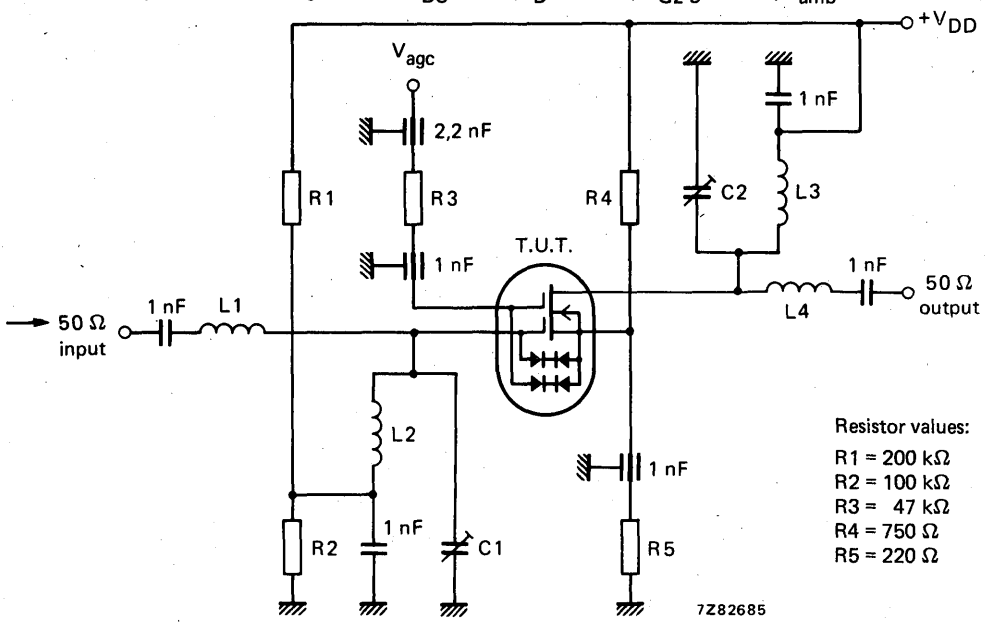


Fig. 15 Automatic gain control test circuit at f = 200 MHz (see also Fig. 16).
V_{DD} = 16 V; G_S = 2 mA/V; G_L = 0,5 mA/V.

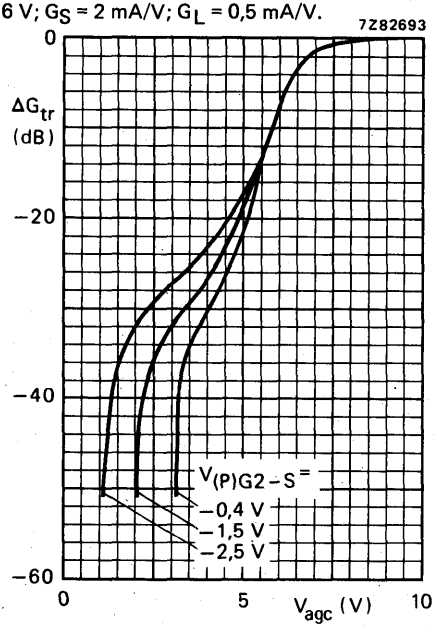


Fig. 16 V_{DD} = 16 V; f = 200 MHz; T_{amb} = 25 °C; typical values; see also Fig. 15.

N-CHANNEL INSULATED GATE MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for linear applications in the audio as well as the i.f. and v.h.f. frequency region, and in cases where high input impedance, low gate leakage currents and low noise figures are of importance.

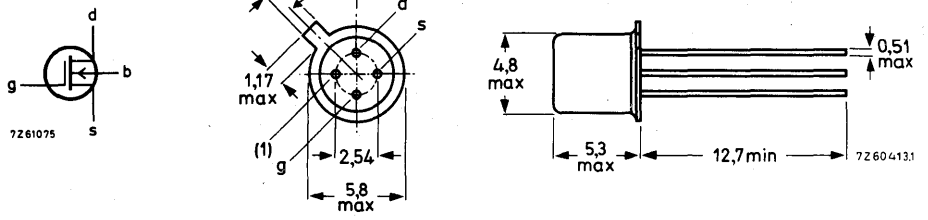
QUICK REFERENCE DATA

Drain-substrate voltage	V_{DB}	max.	30 V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V
Drain current V_{DS} = 15 V; V_{GS} = 0	I_{DSS}		10 to 40 mA
Transfer admittance I_D=5 mA; V_{DS} = 15 V; f = 1 kHz	$\lvert Y_{fs} \rvert$	>	6 mA/V
Feedback capacitance I_D = 5 mA; V_{DS} = 15 V; f = 1 MHz	C_{rs}	<	0,7 pF
Noise figure at f = 200 MHz I_D = 5 mA; V_{DS} = 15 V; T_{amb} = 25 °C G_S = 1 mA/V; B_S = B_{Sopt}	F	<	5 dB
Equivalent noise voltage at f = 1 kHz I_D = 5 mA; V_{DS} = 15 V; T_{amb} = 25 °C	$V_n/\sqrt{B}$	typ.	100 $nV/\sqrt{Hz}$

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = substrate (b) connected to case

Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

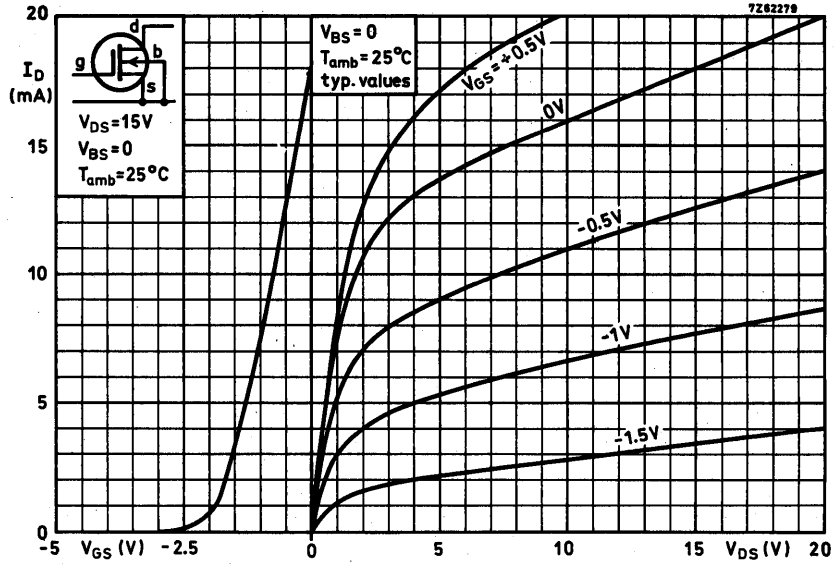
Drain-substrate voltage	V_{DB}	max.	30 V
Source-substrate voltage	V_{SB}	max.	30 V
Gate-substrate voltage (continuous)	$\pm V_{GB}$	max.	10 V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max. min.	15 V −15 V
Drain current (d.c.)	I_D	max.	20 mA
Drain current (peak value) $t_p = 20$ ms; $\delta = 0{,}1$	I_{DM}	max.	50 mA
Total power dissipation up to $T_{amb} = 25$ °C	P_{tot}	max.	200 mW
Storage temperature	T_{stg}		−65 to + 125 °C
Junction temperature	T_j	max.	125 °C

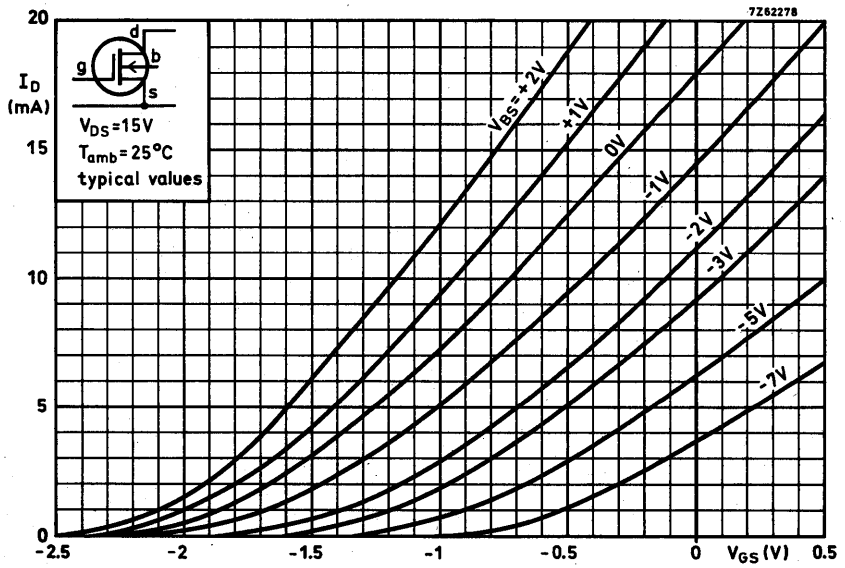
THERMAL RESISTANCE

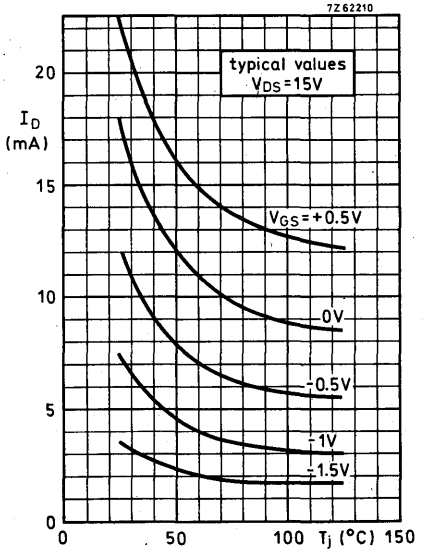
From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	500 K/W

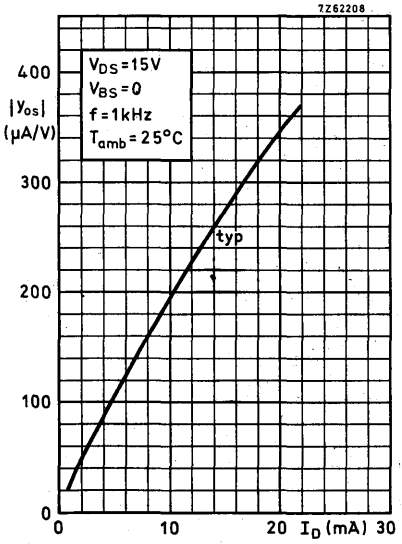
CHARACTERISTICS $T_j = 25\ ^oC$ unless otherwise specified

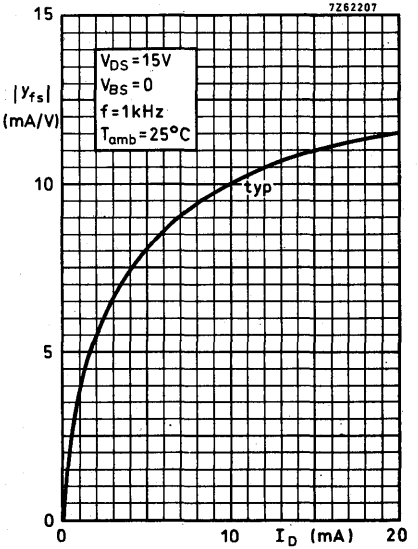
Gate currents; $V_{BS} = 0$				
$-V_{GS} = 10$ V; $V_{DS} = 0$	$-I_{GSS}$	<	10	pA
$V_{GS} = 10$ V; $V_{DS} = 0$	I_{GSS}	<	10	pA
$-V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\ ^oC$	$-I_{GSS}$	<	200	pA
$V_{GS} = 10$ V; $V_{DS} = 0$; $T_j = 125\ ^oC$	I_{GSS}	<	200	pA
Bulk currents; $V_{GB} = 0$				
$-V_{BD} = 30$ V; $I_S = 0$	$-I_{BDO}$	<	10	µA
$-V_{BS} = 30$ V; $I_D = 0$	$-I_{BSO}$	<	10	µA
Drain current				
$V_{DS} = 15$ V; $V_{GS} = 0$	I_{DSS}	10 to	40	mA
Gate-source voltage				
$I_D = 100$ nA; $V_{DS} = 15$ V	$-V_{GS}$	0.5 to	3.5	V
Gate-source cut-off voltage				
$I_D = 100$ nA ; $V_{DS} = 15$ V	$-V_{(P)GS}$	<	4	V
y parameters $T_{amb} = 25\ ^oC$				
$I_D = 5$ mA; $V_{DS} = 15$ V				
Transfer admittance at f = 1 kHz	$\|y_{fs}\|$	>	6	mA/V
Output admittance at f = 1 kHz	$\|y_{os}\|$	<	0.4	mA/V
Input capacitance at f = 1 MHz	C_{is}	<	5	pF
Feedback capacitance at f = 1 MHz	C_{rs}	<	0.7	pF
Output capacitance at f = 1 MHz	C_{os}	<	3	pF
Noise figure at f = 200 MHz $T_{amb} = 25\ ^oC$				
$I_D = 5$ mA; $V_{DS} = 15$ V				
$G_S = 1\ m\Omega^{-1}$; $B_S = B_{Sopt}$	F	<	5	dB
Equivalent noise voltage $T_{amb} = 25\ ^oC$				
$I_D = 5$ mA; $V_{DS} = 15$ V; f = 120 Hz	$V_n/\sqrt{B}$	typ.	300	nV/$\sqrt{Hz}$
f = 1 kHz	$V_n/\sqrt{B}$	typ.	100	nV/$\sqrt{Hz}$
f = 10 kHz	$V_n/\sqrt{B}$	typ.	35	nV/$\sqrt{Hz}$

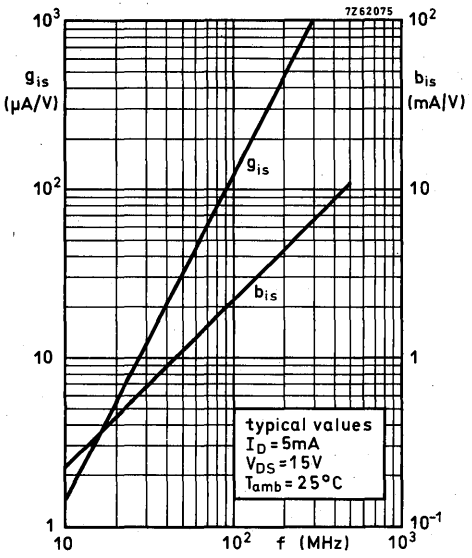

7Z62279
I_D (mA)
V_{DS}=15V
V_{BS}=0
T_{amb}=25°C
V_{BS} = 0
T_{amb} = 25°C
typ. values
V_{GS} = +0.5V
0V
-0.5V
-1V
-1.5V
V_{GS} (V)
V_{DS} (V)

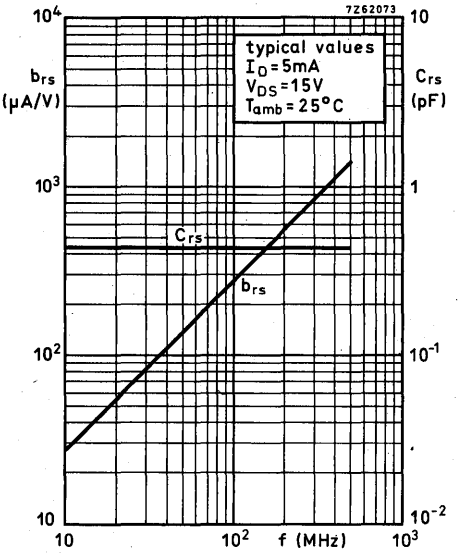

7Z62278
I_D (mA)
V_{DS}=15V
T_{amb}=25°C
typical values
V_{BS} = +2V
+1V
0V
-1V
-2V
-3V
-5V
-7V
V_{GS} (V)

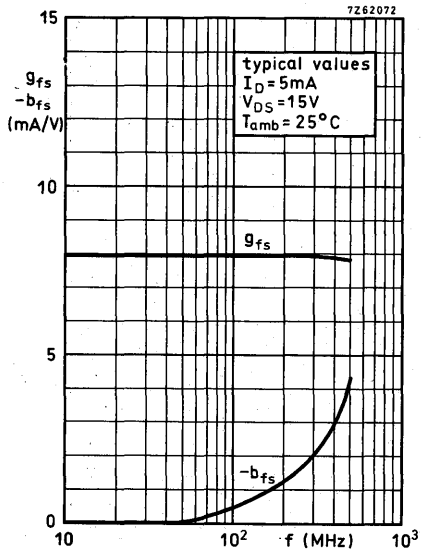

7Z62210
typical values
V_{DS}=15V
I_D (mA)
20
15
10
5
0
V_{GS}=+0.5V
0V
-0.5V
-1V
-1.5V
0
50
100
T_j (°C)
150

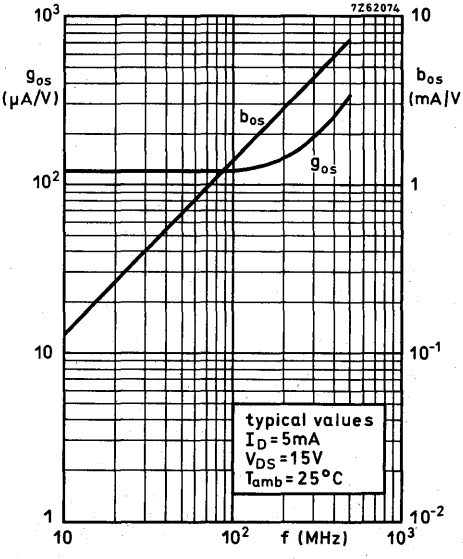

7Z62208
V_{DS}=15V
V_{BS}=0
f=1kHz
T_{amb}=25°C
$|y_{os}|$ (μA/V)
400
300
200
100
0
typ
0
10
20
I_D (mA)
30

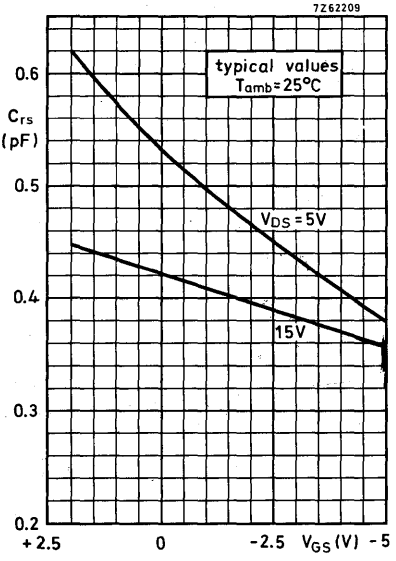

7Z62207
V_{DS}=15V
V_{BS}=0
f=1kHz
T_{amb}=25°C
$|y_{fs}|$ (mA/V)
15
10
5
0
typ
0
10
I_D (mA)
20

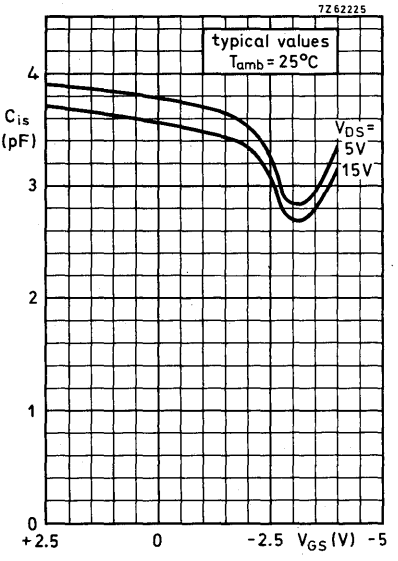

7Z62075
g_{is} (μA/V)
b_{is} (mA/V)
g_{is}
b_{is}
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
f (MHz)


7Z62073
b_{rs} (μA/V)
C_{rs} (pF)
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
C_{rs}
b_{rs}
f (MHz)


7Z62072
g_{fs} $-b_{fs}$ (mA/V)
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
g_{fs}
$-b_{fs}$
f (MHz)


7Z62074
g_{os} (μA/V)
b_{os} (mA/V)
b_{os}
g_{os}
typical values
I_D = 5mA
V_{DS} = 15V
T_{amb} = 25°C
f (MHz)


7Z62209
typical values
Tamb = 25°C
Crs (pF)
0.6
0.5
0.4
0.3
0.2
VDS = 5V
15V
+2.5
0
-2.5
VGS (V)
-5


7Z62225
typical values
Tamb = 25°C
Cis (pF)
4
3
2
1
0
VDS = 5V 15V
+2.5
0
-2.5
VGS (V)
-5

SILICON N-CHANNEL DUAL IG-MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with source and substrate connected to the case, intended for a wide range of v.h.f. applications, such as v.h.f. television tuners, f.m. tuners, as well as for applications in communication, instrumentation and control.

This MOS-FET tetrode is protected against excessive input voltage surges by integrated back-to-back diodes between gates and source.

The tetrode configuration, a series arrangement of two gate controlled channels, offers:

a) very low feedback capacitance providing the possibility of more than 40 dB gain control in r.f. amplifiers requiring negligible a.g.c. power.
b) excellent signal handling capability over the entire gain control range.
c) low noise figure combined with high gain.

QUICK REFERENCE DATA

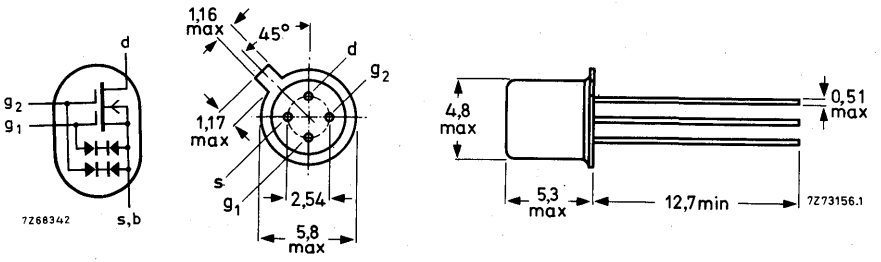
Drain-source voltage	V_{DS}	max.	20	V
Drain current	I_D	max.	50	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Junction temperature	T_j	max.	175	°C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$\lvert y_{fs} \rvert$	typ.	15	mA/V
Feedback capacitance at f = 1 MHz I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	C_{rs}	typ.	30	fF
Noise figure at optimum source admittance I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V G_S = 1,2 mA/V; $-B_S$ = 5,7 mA/V; f = 200 MHz	F	typ.	2,3	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.

Source and substrate connected to the case.



Accessories: 56246 (distance disc).

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage				
Drain-source voltage	V_{DS}	max.	20	V
Currents				
Drain current (d.c. or average)	I_D	max.	50	mA
Drain current (peak value)	I_{DM}	max.	100	mA
Gate 1-source current	$\pm I_{G1-S}$	max.	10	mA
Gate 2-source current	$\pm I_{G2-S}$	max.	10	mA
Power dissipation				
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	300	mW
Temperatures				
Storage temperature	T_{stg}	−65 to + 175		°C
Junction temperature	T_j	max.	175	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j-a}$	=	0,5	°C/mW

STATIC CHARACTERISTICS T_{amb} = 25 °C unless otherwise specified

Gate cut-off currents				
$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0	$\pm I_{G1-SS}$	<	10	nA
$\pm V_{G1-S}$ = 5 V; $V_{G2-S} = V_{DS}$ = 0; T_j = 150 °C	$\pm I_{G1-SS}$	<	10	µA
$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0	$\pm I_{G2-SS}$	<	10	nA
$\pm V_{G2-S}$ = 5 V; $V_{G1-S} = V_{DS}$ = 0; T_j = 150 °C	$\pm I_{G2-SS}$	<	10	µA
Gate-source breakdown voltages				
$\pm I_{G1-SS}$ = 0,1 mA; $V_{G2-S} = V_{DS}$ = 0	$\pm V_{(BR)G1-SS}$	6,0 to 20		V
$\pm I_{G2-SS}$ = 0,1 mA; $V_{G1-S} = V_{DS}$ = 0	$\pm V_{(BR)G2-SS}$	6,0 to 20		V
Drain current				
V_{DS} = 10 V; V_{G1-S} = 0; + V_{G2-S} = 4 V	I_{DSS}	20 to 55		mA [1]
Gate 1-source voltage				
I_D = 10 mA; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{G1-S}$	0,6 to 2,1		V
Gate-source cut-off voltages				
I_D = 10 µA ; V_{DS} = 10 V; + V_{G2-S} = 4 V	$-V_{(P)G1-S}$	1,5 to 3,8		V
I_D = 10 µA ; V_{DS} = 10 V; V_{G1-S} = 0	$-V_{(P)G2-S}$	1,5 to 3,4		V

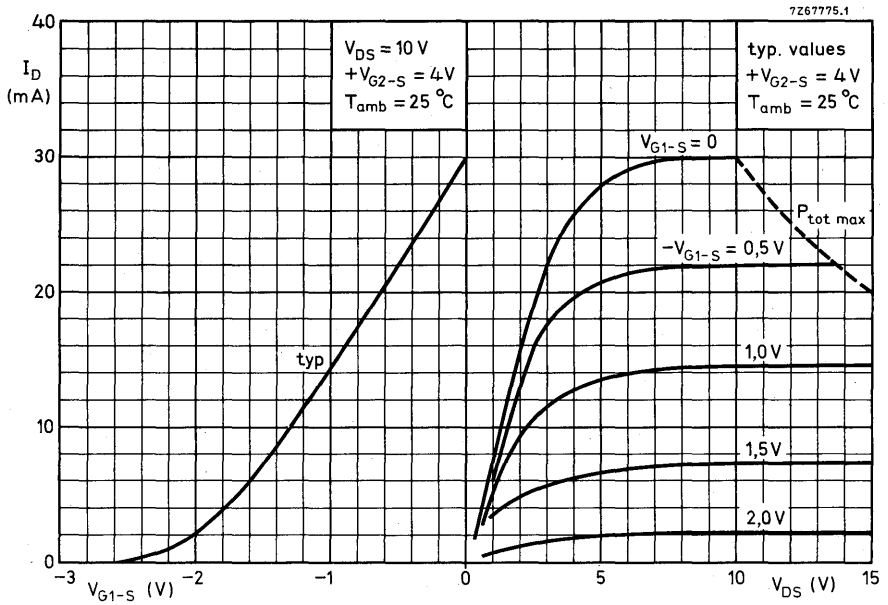
[1] Measured under pulse conditions.

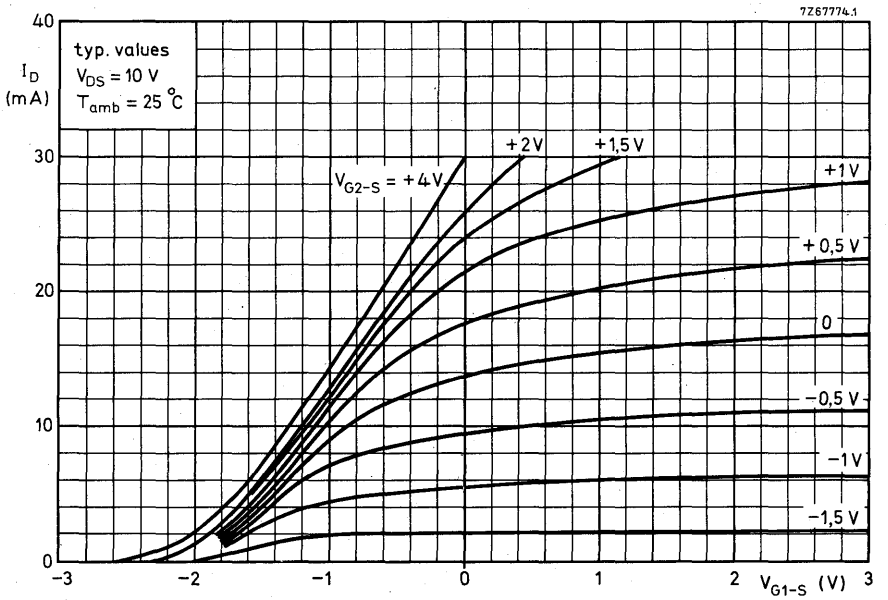
DYNAMIC CHARACTERISTICS

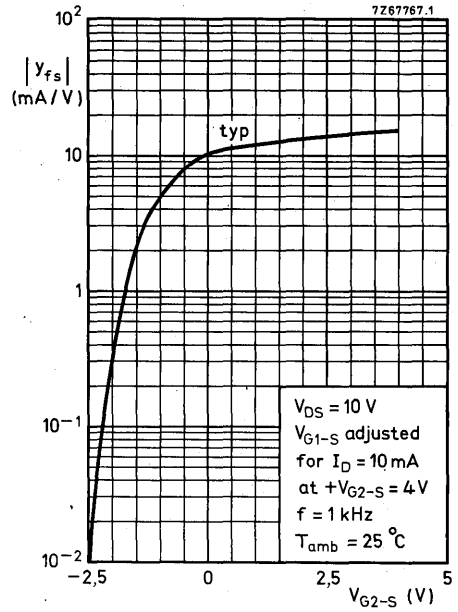
Measuring conditions (common source): I_D = 10 mA; V_{DS} = 10 V; $+V_{G2-S}$ = 4 V; T_{amb} = 25 °C

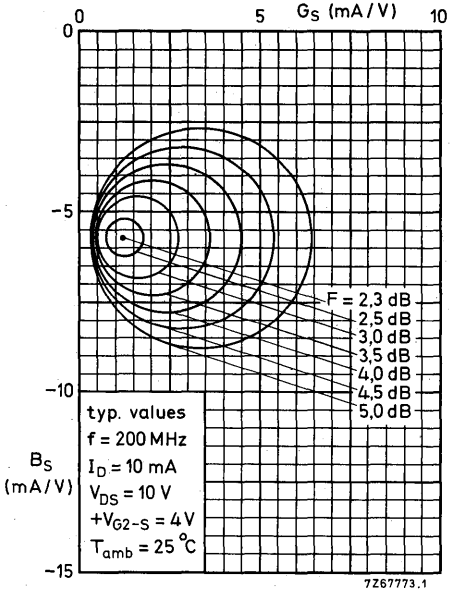
Transfer admittance at f = 1 kHz	$\lvert y_{fs} \rvert$	>	12	mA/V
		typ.	15	mA/V
Input capacitance at f = 1 MHz	C_{is}	typ.	5,5	pF
Feedback capacitance at f = 1 MHz	C_{rs}	typ.	30	fF
Output capacitance at f = 1 MHz	C_{os}	typ.	3,5	pF
Noise figure at optimum source admittance				
G_S = 0,95 mA/V; $-B_S$ = 5,0 mA/V; f = 100 MHz	F	typ.	1,9	dB
G_S = 1,20 mA/V; $-B_S$ = 5,7 mA/V; f = 200 MHz	F	typ.	2,3	dB
		<	3,0	dB
Cross modulation at f = 200 MHz				
Wanted signal at f_o = 197,5 MHz Unwanted signal at f_{int} = 202,5 MHz				
Interference voltage at g_1 for K = 1%	V_{int}	typ.	100	mV [1]

1) Cross modulation is defined here as the voltage at g_1 of an unwanted signal with 80% modulation depth, giving 0,8% modulation depth on the wanted signal (a.m. definition).


7Z67775.1
I_D (mA)
V_{DS} = 10 V
+V_{G2-S} = 4 V
T_{amb} = 25 °C
typ. values
+V_{G2-S} = 4 V
T_{amb} = 25 °C
V_{G1-S} = 0
$P_{tot\ max}$
−V_{G1-S} = 0,5 V
1,0 V
1,5 V
2,0 V
typ
V_{G1-S} (V)
V_{DS} (V)


7Z67774.1
I_D (mA)
typ. values
V_{DS} = 10 V
T_{amb} = 25 °C
+2 V
+1,5 V
V_{G2-S} = +4 V
+1 V
+0,5 V
0
−0,5 V
−1 V
−1,5 V
V_{G1-S} (V)





circles of constant noise figure

SILICON N-CHANNEL DUAL INSULATED-GATE MOS-FET

Depletion type field-effect transistor in a TO-72 metal envelope with source and substrate connected to the case. It is intended for a wide range of applications in communications, instrumentation and control.

QUICK REFERENCE DATA

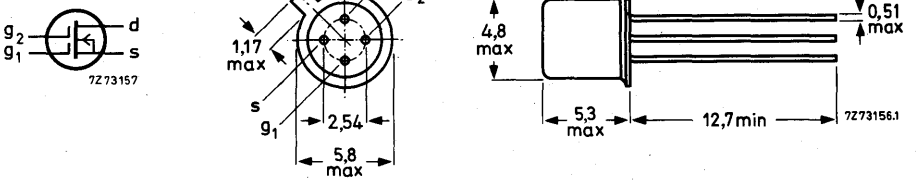
Drain-source voltage	V_{DS}	max.	20 V
Drain current	I_D	max.	20 mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	200 mW
Junction temperature	T_j	max.	135 °C
Transfer admittance at f = 1 kHz I_D = 10 mA; V_{DS} = 13 V; + $V_{G2\text{-}S}$ = 4 V	$\lvert y_{fs} \rvert$	> typ.	8 mA/V 13 mA/V
Feedback capacitance at f = 10 MHz I_D = 10 mA; V_{DS} = 13 V; + $V_{G2\text{-}S}$ = 4 V	C_{rs}	typ.	25 fF

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.

Source and substrate connected to the case



Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	V_{DSX}	max.	20	V
Gate 1-source voltage	$\pm V_{G1-S}$	max.	8	V
Gate 2-source voltage	$\pm V_{G2-S}$	max.	8	V
Non-repetitive peak voltage ($t \leqslant 10$ ms)				
gate 1-source voltage	$\pm V_{G1-SM}$	max.	50	V
gate 2-source voltage	$\pm V_{G2-SM}$	max.	50	V
Drain current	I_D	max.	20	mA
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	200	mW
Storage temperature	T_{stg}	−65 to +	135	°C
Junction temperature	T_j	max.	135	°C

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\ j\text{-}a}$	=	550	K/W

CHARACTERISTICS T_j = 25 °C unless otherwise specified

Gate 1 cut-off current

$\pm V_{G1-S}$ = 8 V; V_{G2-S} = 0; V_{DS} = 0; T_j = 135 °C	$\pm I_{G1-SS}$	<	1	nA

Gate 2 cut-off current

$\pm V_{G2-S}$ = 8 V; V_{G1-S} = 0; V_{DS} = 0; T_j = 135 °C	$\pm I_{G2-SS}$	<	1	nA

Gate 1-source voltage

I_D = 10 mA; V_{DS} = 13 V; + V_{G2-S} = 4 V	$-V_{G1-S}$	0.6 to	2.8	V

Gate 1-source cut-off voltage

I_D = 100 μA; V_{DS} = 20 V; + V_{G2-S} = 4 V	$-V_{G1-S}$	<	5	V

Gate 2-source cut-off voltage

I_D = 50 μA; V_{DS} = 20 V; V_{G1-S} = 0	$-V_{G2-S}$	<	4	V

y parameters (common source)

I_D = 10 mA; V_{DS} = 13 V; + V_{G2-S} = 4 V; T_{amb} = 25 °C

Transfer admittance	f = 1 kHz	$\lvert y_{fs} \rvert$	>	8	mA/V
			typ.	13	mA/V
	f = 200 MHz	$\lvert y_{fs} \rvert$	typ.	12.1	mA/V
	f = 500 MHz	$\lvert y_{fs} \rvert$	typ.	11.2	mA/V
Feedback capacitance	f = 10 MHz	C_{rs}	typ.	25	fF

Transducer gain at f = 200 MHz

I_D = 10 mA; V_{DS} = 13 V; + V_{G2-S} = 4 V

G_S = 1.3 mA/V; G_L = 1 mA/V; T_{amb} = 25 °C

B_S and B_L tuned for maximum gain	G_{tr}	typ.	18	dB

Maximum unilateralised power gain at T_{amb} = 25 °C

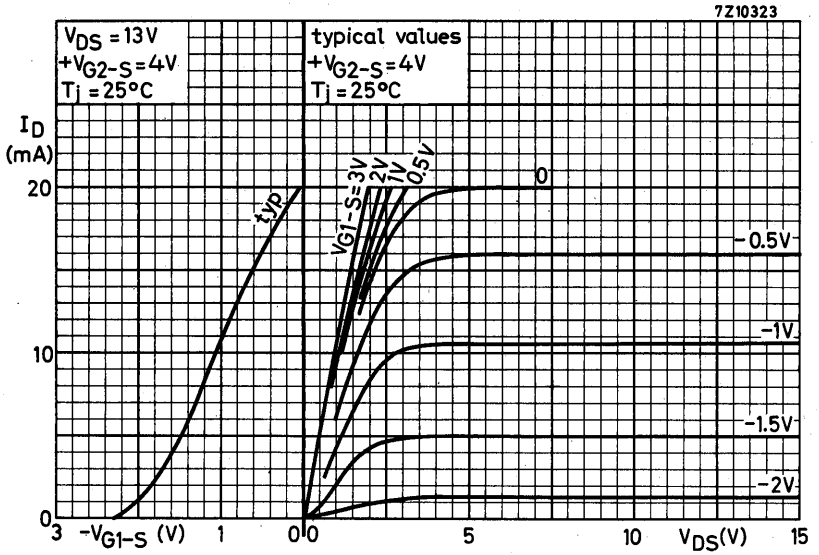
$$G_{UM} \text{ in dB} = 10 \log \frac{\lvert y_{fs} \rvert^2}{4 g_{is} g_{os}}$$

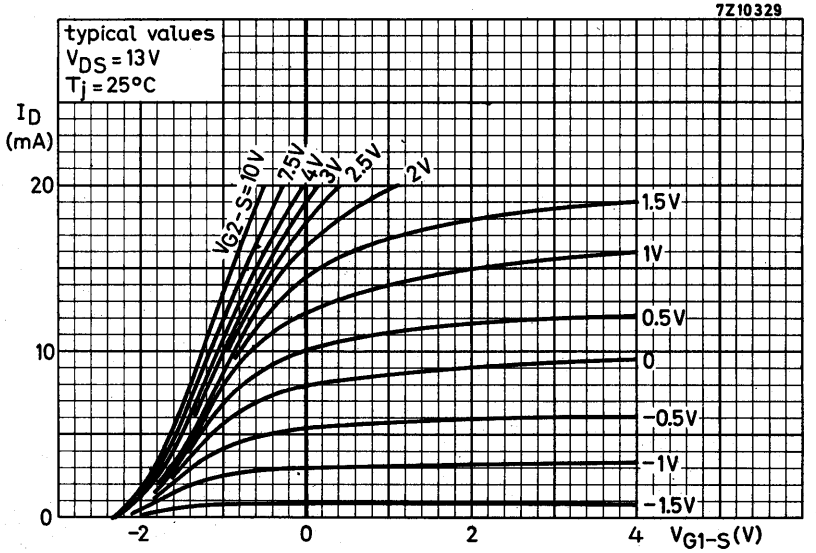
I_D = 10 mA; V_{DS} = 13 V; + V_{G2-S} = 4 V; f = 200 MHz	G_{UM}	typ.	21.3	dB
f = 500 MHz	G_{UM}	typ.	7.3	dB

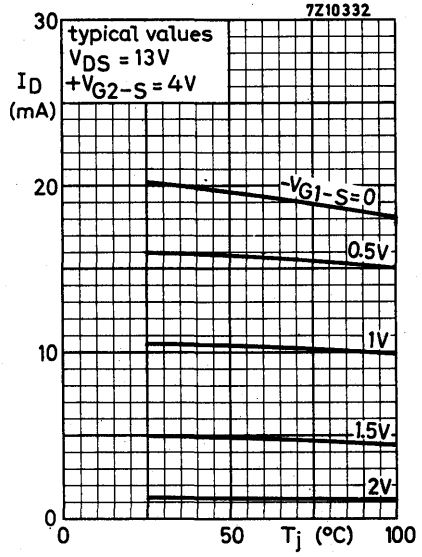
Noise figure at optimum source admittance at f = 200 MHz

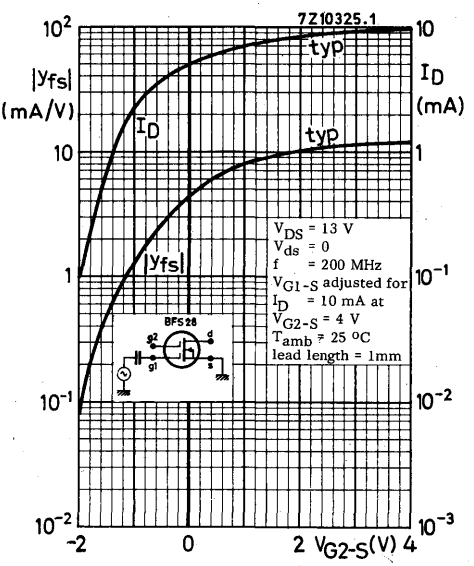
I_D = 10 mA; V_{DS} = 13 V; + V_{G2-S} = 4 V

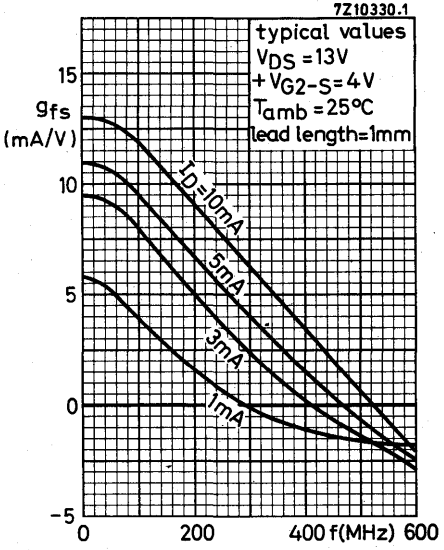
G_{Sopt} = 1.4 mA/V; B_{Sopt} = 5.5 mA/V; T_{amb} = 25 °C	F_{min}	typ.	3	dB
		<	4	dB

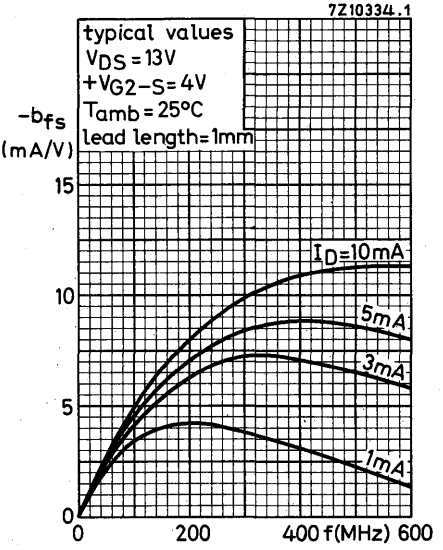

7Z10323
V_{DS} = 13 V
+V_{G2-S} = 4 V
T_j = 25 °C
typical values
+V_{G2-S} = 4 V
T_j = 25 °C
I_D (mA)
20
10
0
typ
V_{G1-S} = 3 V
2 V
1 V
0.5 V
0
−0.5 V
−1 V
−1.5 V
−2 V
3
−V_{G1-S} (V)
1
0
0
5
10
V_{DS} (V)
15

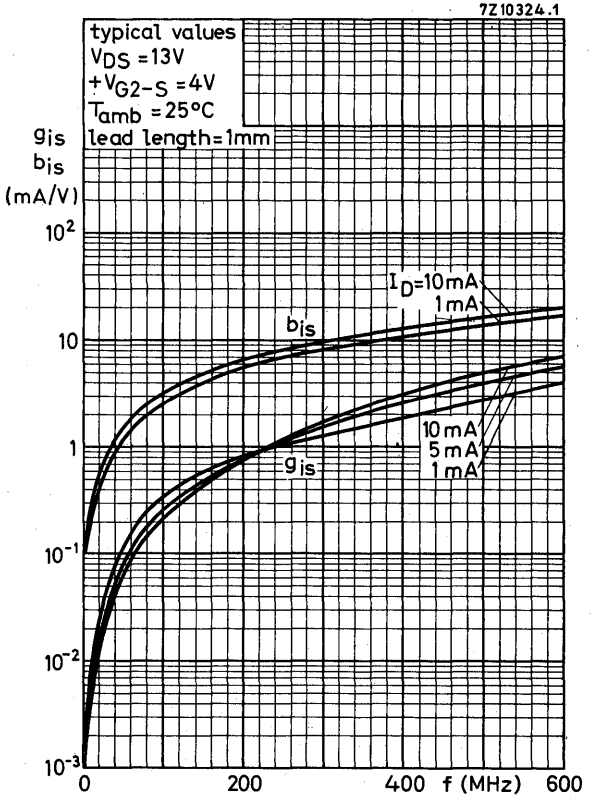

7Z10329
typical values
V_{DS} = 13 V
T_j = 25 °C
I_D (mA)
20
10
0
V_{G2-S} = 10 V
7.5 V
4 V
3 V
2.5 V
2 V
1.5 V
1 V
0.5 V
0
−0.5 V
−1 V
−1.5 V
−2
0
2
4
V_{G1-S} (V)

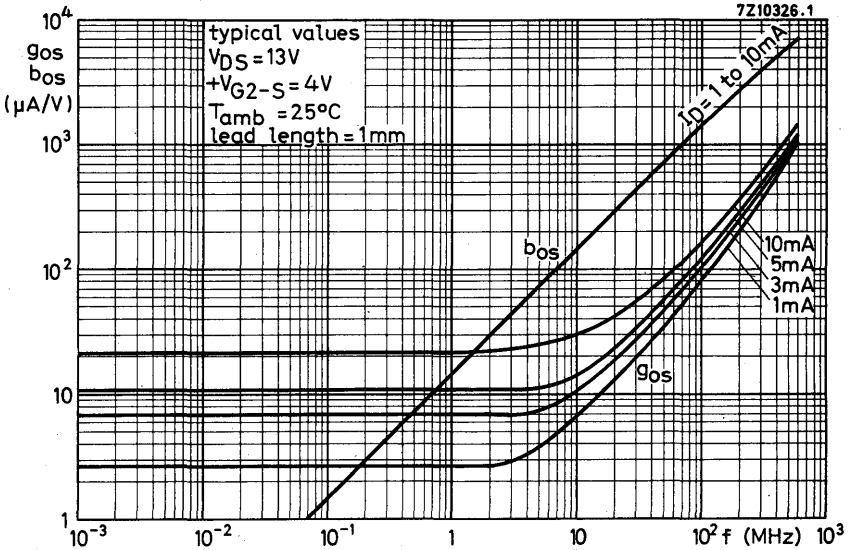

7Z10332
typical values
V_{DS} = 13V
$+V_{G2-S}$ = 4V
I_D (mA)
$-V_{G1-S}$=0
0.5V
1V
1.5V
2V
T_j (°C)

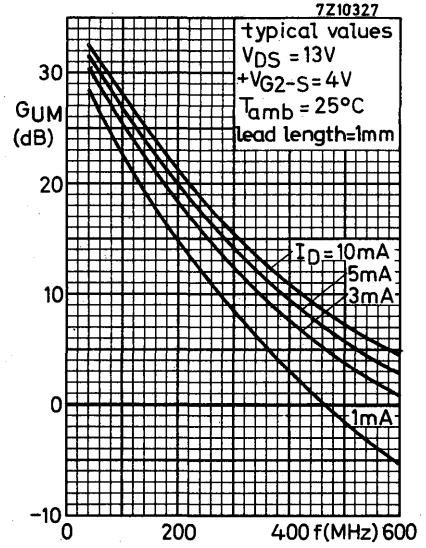

7Z10325.1
$|y_{fs}|$ (mA/V)
I_D (mA)
typ
I_D
typ
$|y_{fs}|$
V_{DS} = 13 V
V_{ds} = 0
f = 200 MHz
V_{G1-S} adjusted for
I_D = 10 mA at
V_{G2-S} = 4 V
T_{amb} = 25 °C
lead length = 1mm
BFS28
V_{G2-S}(V)

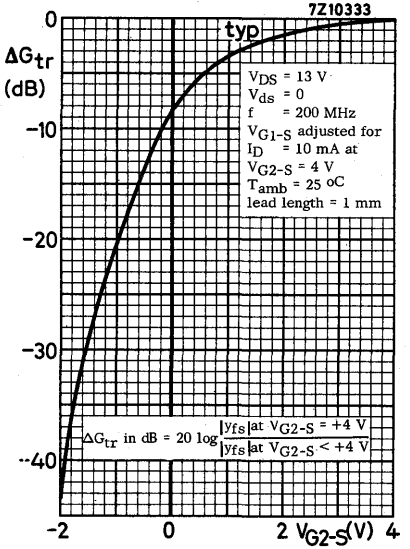

7Z10330.1
typical values
V_{DS} = 13V
$+V_{G2-S}$ = 4V
T_{amb} = 25°C
lead length = 1mm
g_{fs} (mA/V)
I_D=10mA
5mA
3mA
1mA
f(MHz)

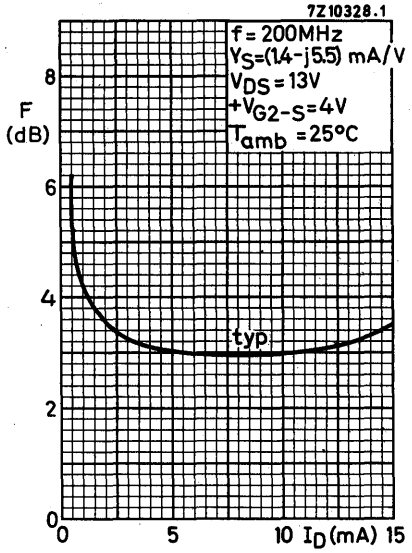

7Z10334.1
typical values
V_{DS} = 13V
$+V_{G2-S}$ = 4V
T_{amb} = 25°C
lead length = 1mm
$-b_{fs}$ (mA/V)
I_D=10mA
5mA
3mA
1mA
f(MHz)

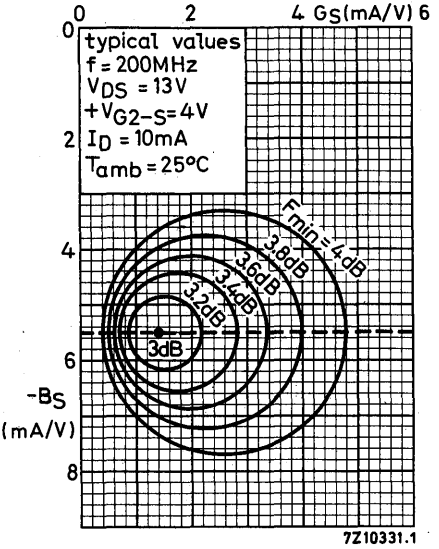

7Z10324.1
typical values
V_{DS} = 13V
$+V_{G2-S}$ = 4V
T_{amb} = 25°C
lead length = 1mm
gis
bis
(mA/V)
10^2
10
1
10^{-1}
10^{-2}
10^{-3}
I_D=10mA
1mA
bis
10mA
5mA
1mA
gis
0
200
400
f (MHz)
600


7Z10326.1
typical values
V_{DS} = 13V
+V_{G2-S} = 4V
T_{amb} = 25°C
lead length = 1mm
I_D = 1 to 10mA
b_{os}
g_{os}
10mA
5mA
3mA
1mA
gos
bos
(μA/V)
f (MHz)


7Z10327
typical values
V_{DS} = 13V
+V_{G2-S} = 4V
T_{amb} = 25°C
lead length = 1mm
I_D = 10mA
5mA
3mA
1mA
GUM
(dB)
f(MHz)


7Z10333
typ
V_{DS} = 13 V
V_{ds} = 0
f = 200 MHz
V_{G1-S} adjusted for
I_D = 10 mA at
V_{G2-S} = 4 V
T_{amb} = 25 °C
lead length = 1 mm
ΔG_{tr} in dB = 20 log $\frac{|y_{fs}| \text{ at } V_{G2-S} = +4 \text{ V}}{|y_{fs}| \text{ at } V_{G2-S} < +4 \text{ V}}$
ΔG_{tr}
(dB)
V_{G2-S}(V)


7Z10328.1
f = 200MHz
YS=(1.4-j5.5) mA/V
VDS = 13V
+VG2-S=4V
Tamb = 25°C
F
(dB)
typ.
0
5
10 ID(mA) 15
0
2
4
6
8


typical values
f = 200MHz
VDS = 13V
+VG2-S=4V
ID = 10mA
Tamb = 25°C
0
2
4 GS(mA/V) 6
F min = 4dB
3.8dB
3.6dB
3.4dB
3.2dB
3dB
-BS
(mA/V)
7Z10331.1

N-CHANNEL IG-MOS-FET

Symmetrical depletion type field-effect transistor in a TO-72 metal envelope with the substrate connected to the case. It is intended for chopper and other special switching applications, e.g. timing circuits, multiplex circuits, etc. The features are a very low drain-source 'on' resistance, a very high drain-source 'off' resistance and low feedback capacitances.

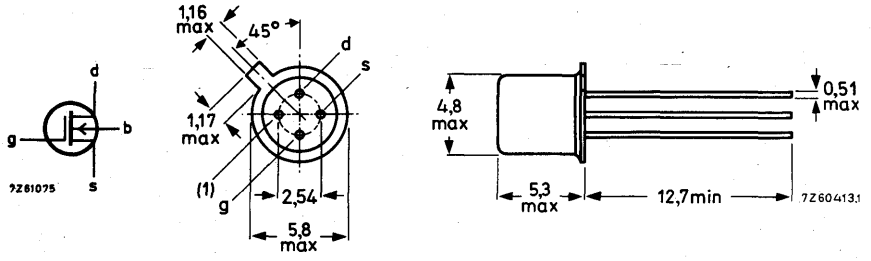
QUICK REFERENCE DATA

Drain-source resistance (on) at f = 1 kHz			
V_{DS} = 0; V_{GS} = 5 V; V_{BS} = 0	$r_{ds\ on}$	<	50 Ω
Drain-source resistance (off)			
V_{DS} = 10 V; $-V_{GS}$ = 5 V; V_{BS} = 0	r_{DSoff}	>	10 GΩ
Feedback capacitance at f = 1 MHz			
$-V_{GS}$ = 5 V; V_{DS} = 0; I_B = 0	C_{rs}	<	0,5 pF
$-V_{GD}$ = 5 V; V_{SD} = 0; I_B = 0	C_{rd}	<	0,5 pF

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-72.



(1) = substrate connected to case.

Accessories: 56246 (distance disc).

Note

To safeguard the gates against damage due to accumulation of static charge during transport or handling, the leads are encircled by a ring of conductive rubber which should be removed just after the transistor is soldered into the circuit.

Products approved to CECC 50 012-010, available on request.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

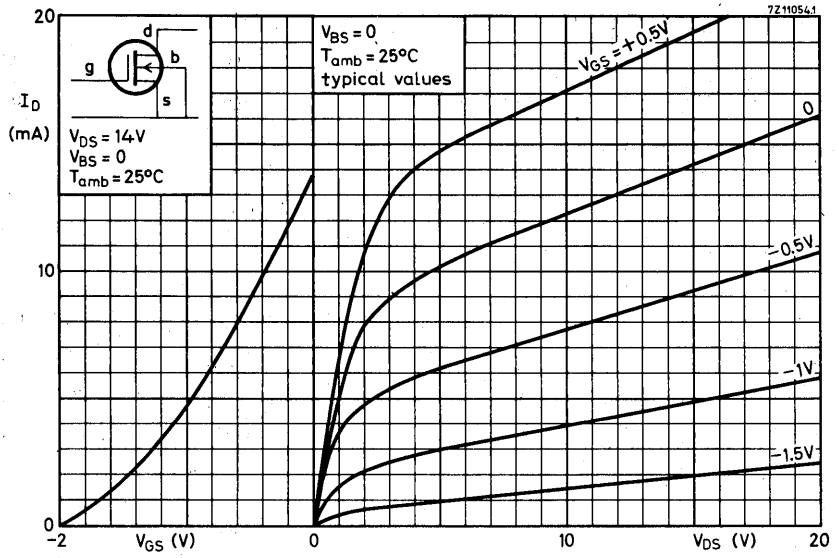
Voltages				
Drain-substrate voltage	V_{DB}	max.	30	V
Source-substrate voltage	V_{SB}	max.	30	V
Gate-substrate voltage (continuous)	V_{GB}	max.	10	V
		min.	−10	V
Repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $f > 100$ Hz	V_{G-N}	max.	15	V
		min.	−15	V
Non-repetitive peak gate to all other terminals voltage $V_{SB} = V_{DB} = 0$; $t < 10$ ms	V_{G-N}	max.	50	V
		min.	−50	V
Currents				
Drain current (peak value) $t_r = 20$ ms; $\delta = 0,1$	I_{DM}	max.	50	mA
Source current (peak value) $t_r = 20$ ms; $\delta = 0,1$	I_{SM}	max.	50	mA
Power dissipation				
Total power dissipation up to $T_{amb} = 25\ ^{o}C$	P_{tot}	max.	200	mW
Temperatures				
Storage temperature	T_{stg}	−65 to +125		^{o}C
Junction temperature	T_j	max.	125	^{o}C

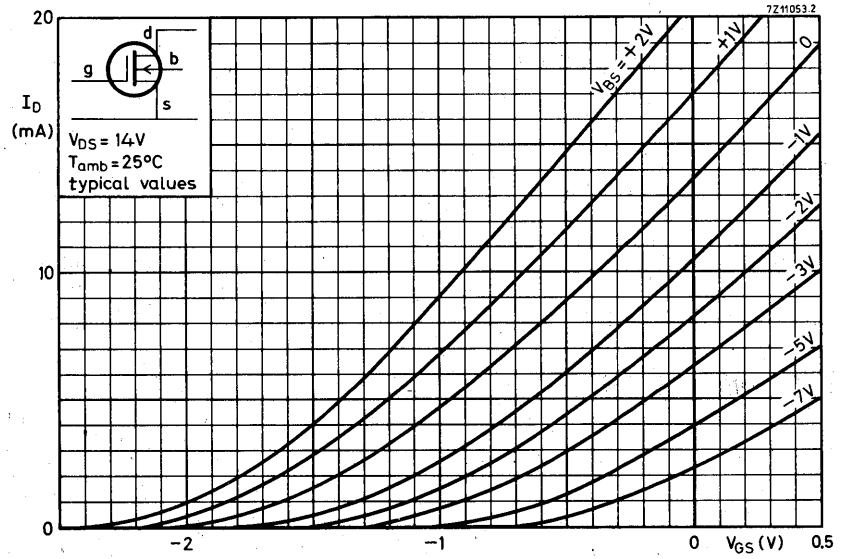
THERMAL RESISTANCE

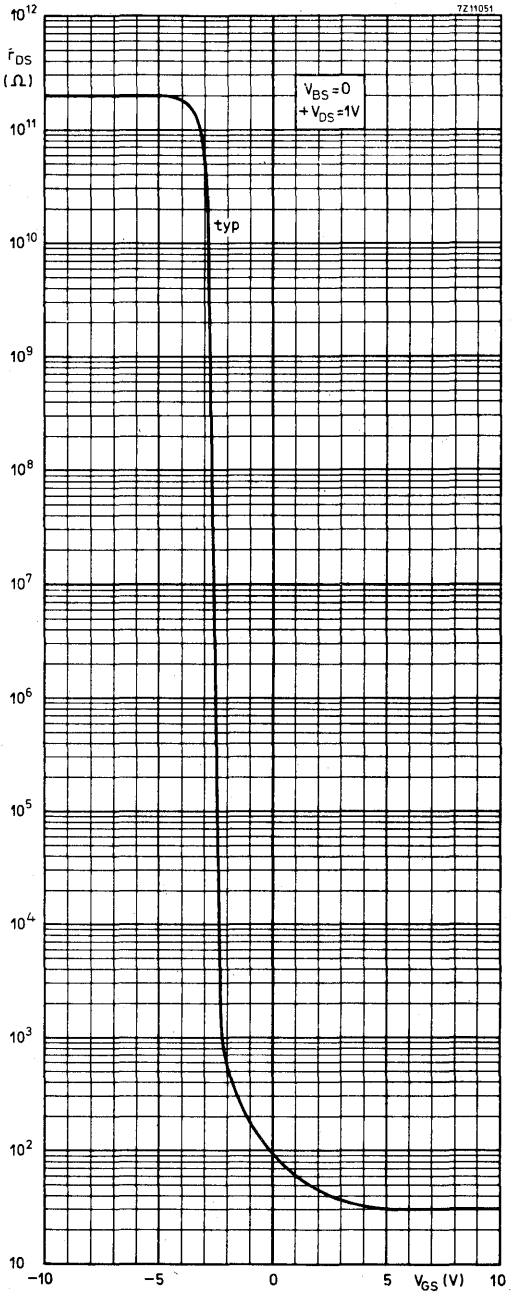
From junction to ambient in free air	$R_{th\ j-a}$	=	0,5	$^{o}C/mW$

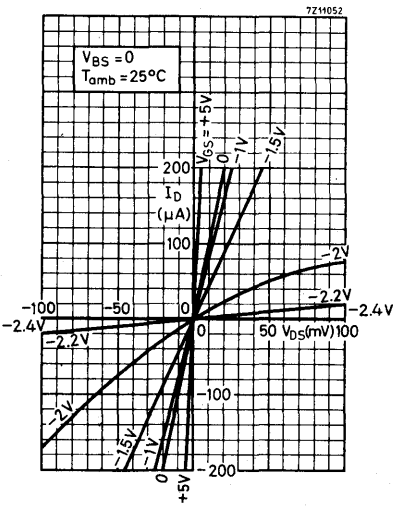
CHARACTERISTICS T_j = 25 °C unless otherwise specified

Drain cut-off currents; V_{BS} = 0				
V_{DS} = 10 V; $-V_{GS}$ = 5 V	I_{DSX}	<	1	nA
V_{DS} = 10 V; $-V_{GS}$ = 5 V; T_j = 125 °C	I_{DSX}	<	1	µA
Source cut-off currents; V_{BD} = 0				
V_{SD} = 10 V; $-V_{GD}$ = 5 V	I_{SDX}	<	1	nA
V_{SD} = 10 V; $-V_{GD}$ = 5 V; T_j = 125 °C	I_{SDX}	<	1	µA
Gate currents; V_{BS} = 0				
$-V_{GS}$ = 10 V; V_{DS} = 0	$-I_{GSS}$	<	10	pA
V_{GS} = 10 V; V_{DS} = 0	I_{GSS}	<	10	pA
$-V_{GS}$ = 10 V; V_{DS} = 0; T_j = 125 °C	$-I_{GSS}$	<	200	pA
V_{GS} = 10 V; V_{DS} = 0; T_j = 125 °C	I_{GSS}	<	200	pA
Bulk currents; V_{GB} = 0				
$-V_{BD}$ = 30 V; I_S = 0	$-I_{BDO}$	<	10	µA
$-V_{BS}$ = 30 V; I_D = 0	$-I_{BSO}$	<	10	µA
Drain-source resistance (on) at f = 1 kHz; V_{BS} = 0				
V_{GS} = 0 ; V_{DS} = 0	r_{dson}	<	100	Ω
V_{GS} = 0 ; V_{DS} = 0; T_j = 125 °C	r_{dson}	<	150	Ω
$+V_{GS}$ = 5 V; V_{DS} = 0	r_{dson}	<	50	Ω
Drain-source resistance (off)				
$-V_{GS}$ = 5 V; V_{DS} = 10 V; V_{BS} = 0	r_{DSoff}	>	10	GΩ
Feedback capacitances at f = 1 MHz				
$-V_{GS}$ = 5 V; V_{DS} = 0; I_B = 0	C_{rs}	<	0,5	pF
$-V_{GD}$ = 5 V; V_{SD} = 0; I_B = 0	C_{rd}	<	0,5	pF
Gate to all other terminals capacitance at f = 1 MHz				
$-V_{GB}$ = 5 V; V_{SB} = V_{DB} = 0	C_{g-n}	<	6	pF


7Z11054.1
20
10
0
I_D
(mA)
d
g
b
s
V_{DS} = 14V
V_{BS} = 0
T_{amb} = 25°C
V_{BS} = 0
T_{amb} = 25°C
typical values
V_{GS} = +0.5V
0
−0.5V
−1V
−1.5V
−2
V_{GS} (V)
0
10
V_{DS} (V)
20


7Z11053.2
20
10
0
I_D
(mA)
d
g
b
s
V_{DS} = 14V
T_{amb} = 25°C
typical values
V_{BS} = +2V
+1V
0
−1V
−2V
−3V
−5V
−7V
−2
−1
0
V_{GS} (V)
0.5


7Z11051
r_{DS} (Ω)
10^{12}
10^{11}
10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
10^{2}
10
V_{BS} = 0
$+V_{DS}$ = 1V
typ
−10
−5
0
5
V_{GS} (V)
10


7Z11052
V_{BS} = 0
T_{amb} = 25°C
V_{GS} = +5V
0
−1V
−1.5V
200
I_D (μA)
100
−2V
−2.2V
−2.4V
−100
−50
0
50
V_{DS}(mV)
100
−2.4V
−2.2V
−2V
−100
−1.5V
−1V
0
+5V
−200

SIGNETICS D-MOS FETS

SD205DB

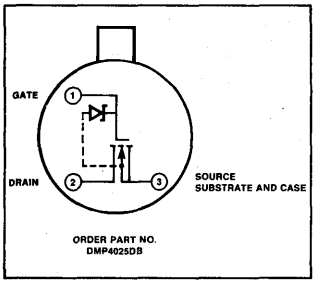
D-MOS POWER FET SINGLE GATE N-CHANNEL ENHANCEMENT

DESCRIPTION

The Signetics DMP4025 is a power MOSFET of the n-channel enhancement mode type designed for switching and amplifier applications requiring high current, high speed, and excellent linear transfer characteristics. Superior performance is achieved by utilizing the Signetics double-diffused MOS process which provides high gain, low drain to source "ON" resistance, low inter-electrode capacitance, and enhanced high frequency operation.

The device is hermetically sealed in a TO-39 package. The source, substrate, and case are connected to pin 3, which results in the package being at ground potential in the common source configuration.

PIN CONFIGURATION (Top View)



ORDER PART NO.
DMP4025DB

FEATURES

- **10dB gain @ 300MHz**
- **High I_{DS}: 800mA @ V_{GS} = +10V**
- **Withstands high VSWR**
- **No thermal runaway**
- **Low input capacitance**
- **Low feedback capacitance**
- **Switches 500mA in less than 2ns**
- **CMOS logic compatible input**
- **Extremely low drive current**

APPLICATIONS

- **Broadband power amplifier**
- **Power driver**
- **High speed switching**

ABSOLUTE MAXIMUM RATINGS[1] T_A = +25°C unless otherwise specified

	PARAMETER	RATING	UNIT
V_{DS}	Drain-to-source	+25	V
V_{GS}	Gate-to-source	+20	V
V_{DG}	Drain-to-gate	+20	V
$I_{D(ON)}$	Continuous drain current	0.8	A
I_Z	Gate (Zener) current	10	mA
P_D	Power dissipation		
	T_A = 25°C[2]	1	W
	T_C = 25°C[3]	4	W
	Power derating factors		
	Free air	10	mW/°C
	Infinite heat sink	40	mW/°C
θ_{JA}	Thermal resistance	100	°C/W
θ_{JC}	Thermal resistance	25	°C/W
T_{OP}	Operating Temperature	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to +150	°C

NOTES

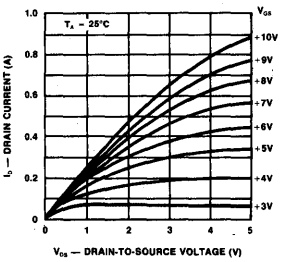
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Free air.
3. Infinite heat sink.
4. Pulsed @ 80μs, 1% duty cycle.
5. Measured in amplifier test fixture.

ELECTRICAL CHARACTERISTICS T_A = +25°C unless otherwise specified

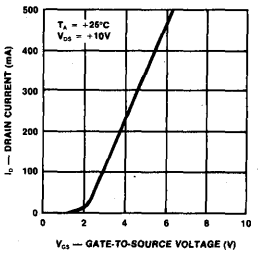
	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
BV_{DSS}	Drain-source breakdown	I_D = 10μA, V_{GS} = 0	25	30		V
$V_{GS(th)}$	Gate threshold voltage	I_D = 10μA, V_{GS} = V_{DS} = $V_{GS(th)}$	0.5		2	V
$I_{D(ON)}$	Drain "ON" current[4]	V_{GS} = V_{DS} = +10V	1			A
$I_{D(OFF)}$	Drain "OFF" current	V_{DS} = +25V, V_{GS} = 0			1	μA
$r_{DS(ON)}$	Drain-source "ON" resistance[4]	V_{GS} = +5V, I_D = 50mA		6	8	Ω
		V_{GS} = +10V, I_D = 50mA		4	6	Ω
		V_{GS} = +10V, I_D = 500mA		4	6	Ω
g_{fs}	Forward Transconductance[4]	V_{DS} = +15V, I_D = 200mA	100	120		mmhos
	Capacitance	V_{DS} = +10V, I_D = 0, f = 1MHz				pF
C_{iss}	Input			11	13	
C_{rss}	Reverse transfer			2	3	
C_{oss}	Common source output			6	8	
N_F	Noise figure[5]	f = 300MHz, V_{DS} = +10V, I_D = 100mA		3.5	4.5	dB
G_{ps}	Common source power gain[5]	f = 300MHz, V_{DS} = +10V, I_D = 100mA	9	12		dB
t_{ON}		See test figure		1		nS
t_{OFF}		See test figure		3		nS
P_I	Intercept point	f = 300MHz, V_{DS} = +12V, I_D = 400mA		29		dBM

TYPICAL PERFORMANCE CHARACTERISTICS

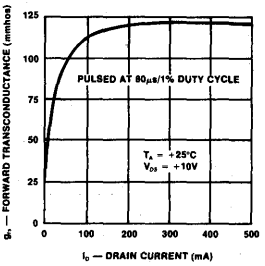
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



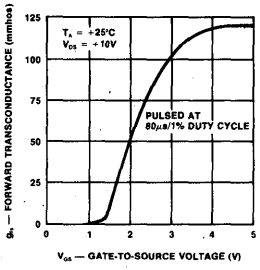
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



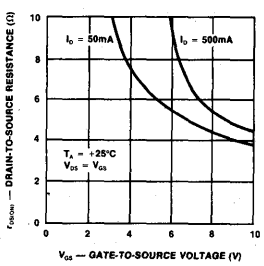
FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



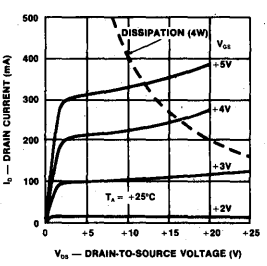
FORWARD TRANSCONDUCTANCE vs GATE-TO-SOURCE VOLTAGE



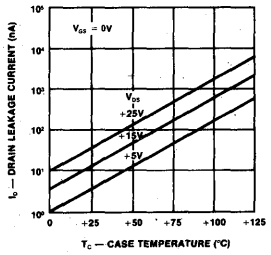
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



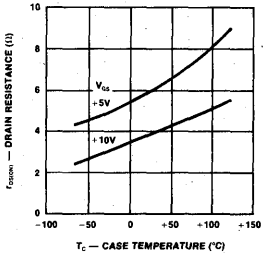
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



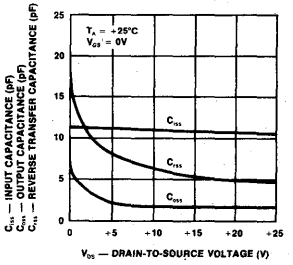
DRAIN LEAKAGE CURRENT vs CASE TEMPERATURE



DRAIN-TO-SOURCE RESISTANCE vs CASE TEMPERATURE

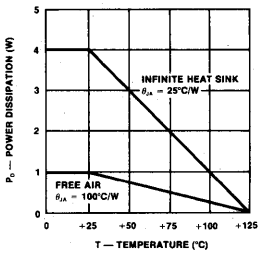


CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

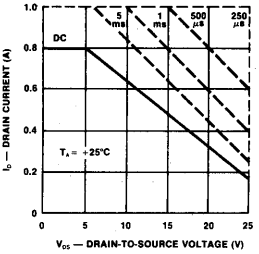


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

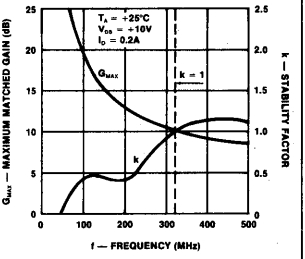
POWER DISSIPATION vs TEMPERATURE



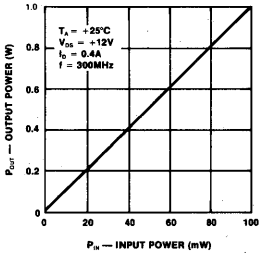
MAXIMUM SAFE OPERATING REGION



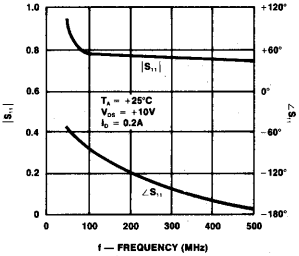
MAXIMUM MATCHED GAIN AND STABILITY FACTOR vs FREQUENCY



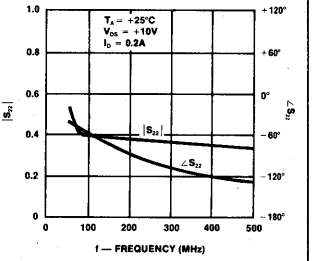
OUTPUT POWER vs INPUT POWER



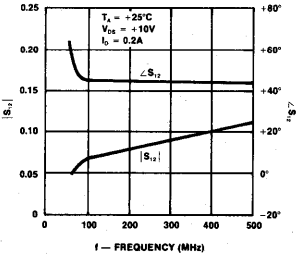
S_{11} vs FREQUENCY



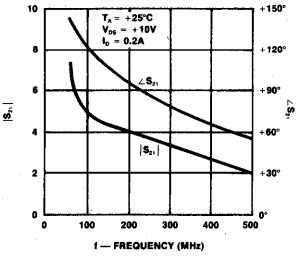
S_{22} vs FREQUENCY



S_{12} vs FREQUENCY



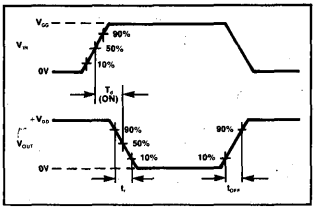
S_{21} vs FREQUENCY

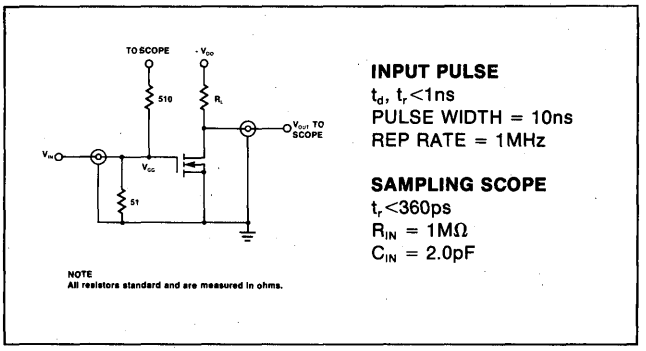


SWITCHING CHARACTERISTICS

V_{GG}(V)	V_{DD}(V)	$R_L(\Omega)$	$t_{d(ON)}$(ns) Typ	t_r(ns) Typ	t_{OFF}(ns) Typ
5	5	100	<1	1	3
	10	200	<1	1	3
	20	390	<1	1	3
10	5	67	<1	1	3
	10	133	<1	1	3
	20	270	<1	1	3

SWITCHING WAVEFORMS

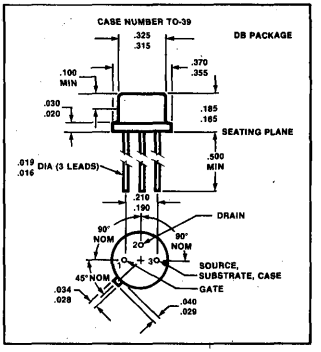




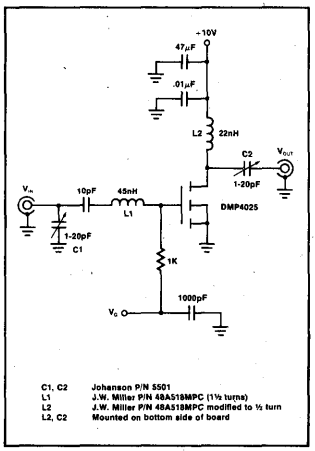
INPUT PULSE
t_d, t_r<1ns
PULSE WIDTH = 10ns
REP RATE = 1MHz

SAMPLING SCOPE
t_r<360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

PACKAGE OUTLINE



300MHz AMPLIFIER TEST CIRCUIT



SD210/211/212/213/214/215-DE

D-MOS FET SWITCH N-CHANNEL ENHANCEMENT

DESCRIPTION

The Signetics D-MOS SD210, 211, 212, 213, 214 and 215 are silicon, insulated gate, field effect transistors of the N-channel enhancement mode type. They are fabricated by the Signetics double-diffused process which gives high switching speed and low capacitance. A zener diode is connected between the gate and substrate of the SD211, 213 and 215. The diode bypasses any voltage transients which lie outside the range of -0.3V to +30V. Thus, the gate is protected against damage in all normal handling and operating situations. A drain-to-source breakdown of typically 35V makes the SD210 and 211 ideally suited for ±10V switch driver applications. Other characteristics allow them to be used as ±5V switches. The SD214 and 215 are designed to switch signals up to ±10V and the SD212 and 213 are designed to switch signals up to ±5V.

All the devices feature low gate node capacitance, extremely low drain node capacitance and very low feedback capacitance. Low "ON" resistance and hermetically sealed 4-lead TO-72 packages are also featured.

FEATURES

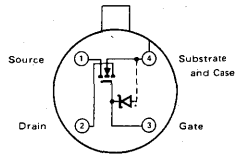
- **Low feedback capacitance: 0.30pF**
- **Low drain node capacitance: 1.3pF**
- **Low gate node capacitance: 2.4pF**
- **Low feedthrough and feedback transients**
- **Ion-implanted for greater reliability**
- **Excellent isolation from input to output: -120dB**
- **35V drain-to-source voltage for SD210/211**
- **Military qualifications pending**

APPLICATIONS

- **Switch driver**
- **Analog switch**
- **Multiplexers**
- **Digital switch**
- **Sample and hold**
- **Choppers**
- **A-TO-D converters**
- **D-TO-A converters**

PIN CONFIGURATION (Top View)

DE PACKAGE



*Diode protection on SD 211/213/215 only.

ORDER PART NO.
SD210DE, SD211DE, SD212DE,
SD213DE, SD214DE, SD215DE

ABSOLUTE MAXIMUM RATINGS (all devices)

PARAMETER	RATING	UNIT
Drain current (I_D)	50	mA
Ambient temperature range		
Storage	-65 to +175	°C
Operating	-55 to +125	°C
Transistor dissipation (P_T)		
At 25°C case temperature (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	1.2	W
At 25°C free-air temperature (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	300	mW

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified.*

PARAMETER		SD210	SD211	SD212	SD213	SD214	SD215	UNIT
V_{DS}	Drain-to-source	+30	+30	+10	+10	+20	+20	Vdc
V_{SD}	Source-to-drain*	+10	+10	+10	+10	+20	+20	Vdc
V_{DB}	Drain-to-substrate	+30	+30	+15	+15	+25	+25	Vdc
V_{SB}	Source-to-substrate	+15	+15	+15	+15	+25	+25	Vdc
V_{GS}	Gate-to-source	±40	-15 +25	±40	-15 +25	±40	-25 +30	Vdc
V_{GB}	Gate-to-substrate	±40	-0.3 +25	±40	-0.3 +25	±40	-0.3 +30	Vdc
V_{GD}	Gate-to-drain	±40	-30 +25	±40	-15 +25	±40	-25 +30	Vdc

*NOTE

Refer to test conditions specified in Electrical Characteristics Table.

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD210			SD211			SD212			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Breakdown voltage												
BV_{DS}	Drain-to-source	$V_{GS} = V_{BS} = 0V$, $I_D = 10\mu A$	30	35		30	35					V
		$V_{GS} = V_{BS} = -5V$, $I_S = 10nA$	10	25		10	25		10	25		V
BV_{SD}	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $I_D = 10nA$	10			10			10			V
BV_{DB}	Drain-to-substrate	$V_{GB} = 0V$, source OPEN $I_D = 10nA$	15			15			15			V
BV_{SB}	Source-to-substrate	$V_{GB} = 0V$, drain OPEN $I_S = 10\mu A$	15			15			15			V
Leakage current												
$I_{DS(OFF)}$	Drain-to-source	$V_{GS} = V_{BS} = -5V$ $V_{DS} = +10V$		1	10		1	10		1	10	nA
$I_{SD(OFF)}$	Source-to-drain	$V_{GD} = V_{BD} = -5V$ $V_{SD} = +10V$		1	10		1	10		1	10	nA
I_{GBS}	Gate	$V_{DB} = V_{SB} = 0V$ $V_{GB} = \pm 40V$			0.1						0.1	nA
		$V_{GB} = +25V$						10				μA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_S = 1\mu A$ $V_{SB} = 0V$	0.5	1.0	2.0	0.5	1.0	2.0	0.1	1.0	2.0	V
$r_{DS(ON)}$	Drain-to-source resistance	$I_D = 1.0mA$, $V_{SB} = 0$ $V_{GS} = +5V$		50	70		50	70		50	70	Ω
		$V_{GS} = +10V$		30	45		30	45		30	45	Ω
		$V_{GS} = +15V$		23			23			23		Ω
		$V_{GS} = +20V$		19			19			19		Ω
		$V_{GS} = +25V$		17						17		Ω

DC ELECTRICAL CHARACTERISTICS (Cont'd) T_A = 25 °C unless otherwise specified.

PARAMETER		TEST CONDITIONS	SD213			SD214			SD215			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Breakdown voltage												
BV_{DS}	Drain-to-source	V_{GS} = V_{BS} = -5V, I_S = 10nA	10	25		20	25		20	25		V
BV_{SD}	Source-to-drain	V_{GD} = V_{BD} = -5V I_D = 10nA	10			20			20			V
BV_{DB}	Drain-to-substrate	V_{GB} = 0V, source OPEN I_D = 10nA	15			25			25			V
BV_{SB}	Source-to-substrate	V_{GB} = 0V, drain OPEN I_S = 10μA	15			25			25			V
Leakage current												
$I_{DS}(OFF)$	Drain-to-source	V_{GS} = V_{BS} = -5V										
		V_{DS} = +10V		1	10							nA
		V_{DS} = +20V					1	10		1	10	nA
$I_{SD}(OFF)$	Source-to-drain	V_{GD} = V_{BD} = -5V										
		V_{SD} = +10V		1	10							nA
		V_{SD} = +20V					1	10		1	10	nA
I_{GBS}	Gate	V_{DB} = V_{SB} = 0V										
		V_{GB} = ±40V						0.1				nA
		V_{GB} = +25V			10							μA
		V_{GB} = +30V									10	μA
V_T	Threshold voltage	V_{DS} = V_{GS} = V_T, I_S = 1μA V_{SB} = 0V	0.1	1.0	2.0	0.1	1.0	2.0	0.1	1.0	2.0	V
$r_{DS}(ON)$	Drain-to-source resistance	I_D = 1.0mA, V_{SB} = 0										
		V_{GS} = +5V		50	70		50	70		50	70	Ω
		V_{GS} = +10V		30	45		30	45		30	45	Ω
		V_{GS} = +15V		23			23			23		Ω
		V_{GS} = +20V		19			19			19		Ω
		V_{GS} = +25V					17			17		Ω

AC ELECTRICAL CHARACTERISTICS T_A = 25 °C unless otherwise specified.

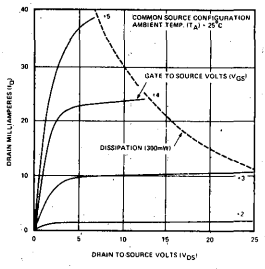
PARAMETER		TEST CONDITIONS	SD210			SD211			SD212			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
gfs	Forward transconductance	V_{DS} = 10V, V_{SB} = 0V I_D = 20mA, f = 1kHz	10	15		10	15		10	15		mmhos
Small Signal Capacitances (See capacitance model)		V_{DS} = 10V, f = 1MHz V_{GS} = V_{BS} = -15V										
$C_{(GS+GD+GB)}$	Gate node			2.4	3.5		2.4	3.5		2.4	3.5	pF
$C_{(GD+DB)}$	Drain node			1.3	1.5		1.3	1.5		1.3	1.5	pF
$C_{(GS+SB)}$	Source node			3.5	4.0		3.5	4.0		3.5	4.0	pF
C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	pF

AC ELECTRICAL CHARACTERISTICS (Cont'd) T_A = 25 °C unless otherwise specified.

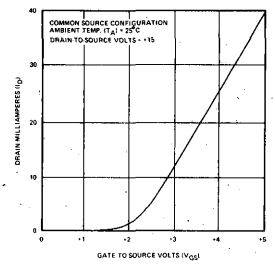
PARAMETER		TEST CONDITIONS	SD213			SD214			SD215			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
gfs	Forward transconductance	V_{DS} = 10V, V_{SB} = 0V I_D = 20mA, f = 1kHz	10	15		10	15		10	15		mmhos
Small Signal Capacitances (See capacitance model)		V_{DS} = 10V, f = 1MHz V_{GS} = V_{BS} = -15V										
$C_{(GS+GD+GB)}$	Gate node			2.4	3.5		2.4	3.5		2.4	3.5	pF
$C_{(GD+DB)}$	Drain node			1.3	1.5		1.3	1.5		1.3	1.5	pF
$C_{(GS+SB)}$	Source node			3.5	4.0		3.5	4.0		3.5	4.0	pF
C_{DG}	Reverse transfer			0.3	0.5		0.3	0.5		0.3	0.5	pF

TYPICAL PERFORMANCE CHARACTERISTICS

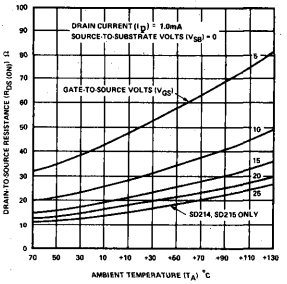
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



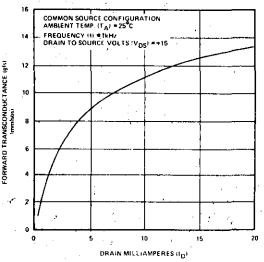
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



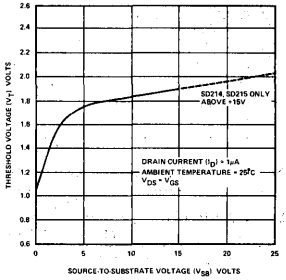
DRAIN-TO-SOURCE RESISTANCE vs TEMPERATURE



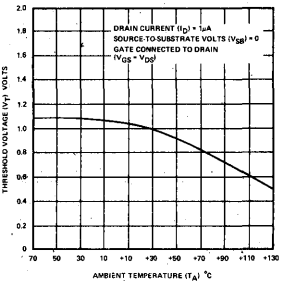
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



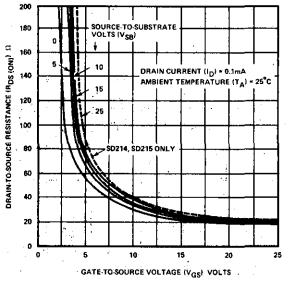
THRESHOLD VOLTAGE vs SOURCE-TO-SUBSTRATE VOLTAGE



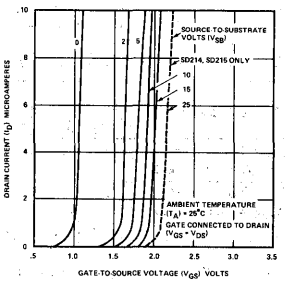
THRESHOLD VOLTAGE vs TEMPERATURE



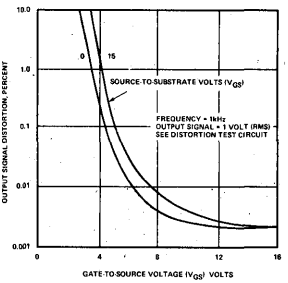
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

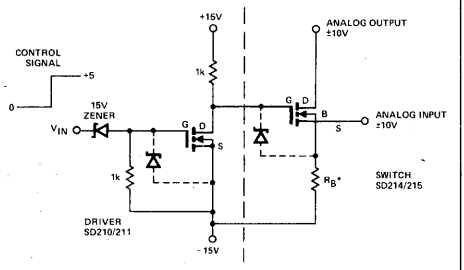


DISTORTION vs GATE-TO-SOURCE VOLTAGE



TYPICAL APPLICATION

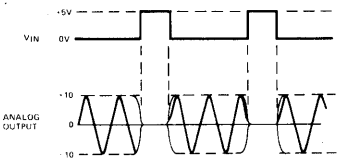
D-MOS DRIVER/SWITCH



RB*Optional current limiting resistor

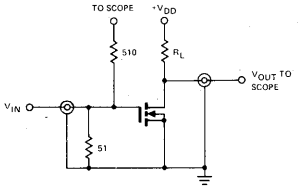
NOTE
*All resistors standard and are measured in ohms.

TYPICAL SWITCHING WAVEFORM



TEST CIRCUITS

SWITCHING

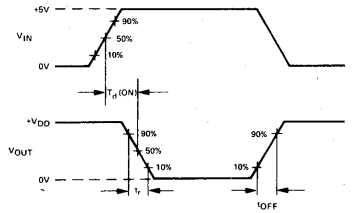


Input pulse: t_d, t_r < 1ns,
Pulse width = 100ns,
Rep rate = 1MHz

SAMPLING SCOPE

t_r < 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

TYPICAL SWITCHING WAVEFORM

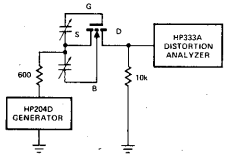


SWITCHING CHARACTERISTICS

		t_d(ON) (ns)		t_r(ns)		t_{OFF}(ns)	
V_{DD}	R_L	Typ	Max	Typ	Max	Typ	Max
5	680	0.6	1.0	0.7	1.0	9.0	*
10	680	0.7		0.8		9.0	*
15	1k	0.9		1.0		14.0	*

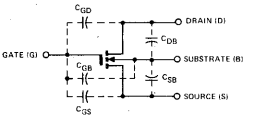
*t_{OFF} is dependent on R_L and C_L and does not depend on the device characteristics.

DISTORTION



NOTE: All resistors standard and are measured in ohms.

CAPACITANCE MODEL



D-MOS FET SWITCH N-CHANNEL ENHANCEMENT

DESCRIPTION

The Signetics DMS4025DE is a power MOSFET of the n-channel enhancement mode type designed for switching applications requiring high current, high speed, low "ON" resistance and excellent node-to-node isolation. Superior performance is achieved by utilizing the Signetics double-diffused MOS process which provides high gain, low drain to source "ON" resistance, low inter-electrode capacitance, and enhanced high frequency operation. The DMS4025DE is designed to switch analog signals up to ±7.5 volts. The device is hermetically sealed in a 4-lead TO-72 package.

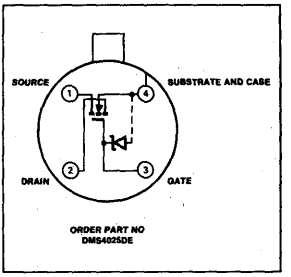
FEATURES

- **Low node capacitances**
- **Low feedthrough and feedback transients**
- **Excellent isolation from input to output**
- **CMOS logic compatible input**
- **Extremely low drive current**
- **Switches 500mA in less than 2ns**

APPLICATIONS

- **Switch driver**
- **Analog switch**
- **Multiplexers**
- **Digital switch**
- **Sample and hold**
- **A-to-D converters**
- **D-to-A converters**

PIN CONFIGURATION (Top View)



ABSOLUTE MAXIMUM RATINGS[1] T_A = +25°C unless otherwise specified

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source	+25	V
V_{SD}	Source-to-drain[2]	+15	V
V_{DB}	Drain-to-body	+22.5	V
V_{SB}	Source-to-body	+22.5	V
V_{GB}	Gate-to-body	+30	V
V_{GS}	Gate-to-source	±22.5	V
V_{GD}	Gate-to-drain	±22.5	V
$I_{D(ON)}$	Continuous drain current	800	mA
P_D	Power dissipation		
	T_A = +25°C[3]	300	mW
	T_C = +25°C[4]	1.2	W
	Power derating factors		
	Free air	3	mW/°C
	Infinite heat sink	12	mW/°C
θ_{JA}	Thermal resistance	330	°C/W
θ_{JC}	Thermal resistance	83.5	°C/W
T_{OP}	Operating temperature	−55 to +125	°C
T_{STG}	Storage temperature	−55 to +150	°C

NOTES

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. See test conditions in dc electrical characteristics section.
3. Free air.
4. Infinite heat sink.

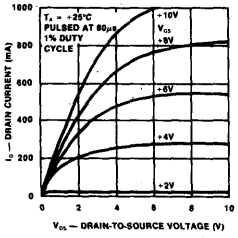
ELECTRICAL CHARACTERISTICS T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
BV_{DS}	Breakdown voltage drain-source	V_{GS} = V_{BS} = 0V, I_D = 10μA	25	30		V
		V_{GS} = V_{BS} = −5V, I_D = 100nA	15			V
BV_{SD}	Breakdown voltage source-drain	V_{GD} = V_{BD} = −5V, I_S = 100nA	15			V
BV_{DB}	Breakdown voltage drain-body	V_{GB} = 0V, I_D = 100nA, source open	22.5			V
BV_{SB}	Breakdown voltage source-body	V_{GB} = 0V, I_S = 100nA, drain open	22.5			V
$I_{D(OFF)}$	Leakage current drain node	V_{GS} = V_{BS} = −5V, V_{DS} = +15V		10	100	nA
$I_{S(OFF)}$	Leakage current source node	V_{GD} = V_{BD} = −5V, V_{SD} = +15V		10	100	nA
$I_{G(OFF)}$	Leakage current gate node (OFF)	V_{GB} = 0V, V_{GS} = V_{GD} = −22.5V		1	100	nA
$I_{G(ON)}$	Leakage current gate node (ON)	V_{GB} = +30V, V_{GS} = V_{GD} = +22.5V		.05	10	μA
$I_{D(ON)}$	Drain "ON" current [5]	V_{GS} = V_{DS} = +10V, V_{SB} = 0V,	1			A
V_T	Threshold voltage	V_{DS} = V_{GS} = V_T, V_{SB} = 0V, I_D = 10μA	0.1	1	2	V
$r_{DS(ON)}$	Drain-source "ON" resistance[5]	V_{GS} = +5V, I_D = 50mA		6	8	Ω
		V_{GS} = +10V, I_D = 50mA		4	6	Ω
		V_{GS} = +10V, I_D = 500mA		4	6	Ω
g_{fs}	Forward Transconductance[5]	V_{DS} = +15V, I_D = 200mA	100	120		mmhos
	Capacitances	(See capacitance model) V_{DS} = +10V, V_{GS} = V_{BS} = −15V, I_D = 0A, f = 1 MHz				
$C_{(GS+GD+GB)}$	Gate node			25	30	pF
$C_{(GD+DB)}$	Drain node			13	15	pF
$C_{(GS+SB)}$	Source node			35	40	pF
C_{DG}	Reverse transfer			3	5	pF
t_{ON}	Turn ON time	See switching		2	4	ns
t_{OFF}	Turn OFF time	time test circuit		3	5	ns

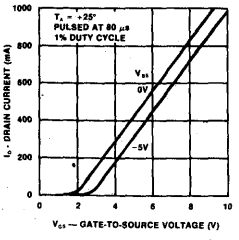
NOTES
5. Pulsed @ 80μs, 1% duty cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

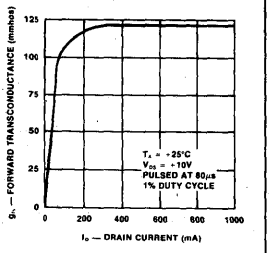
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

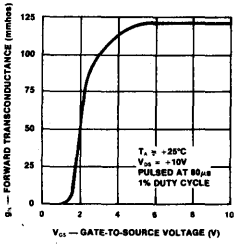


FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT

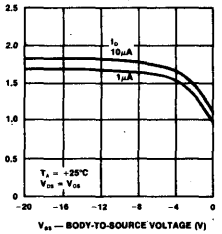


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

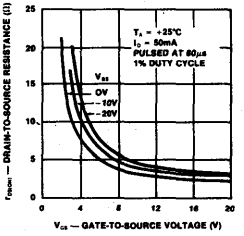
FORWARD TRANSCONDUCTANCE vs GATE-TO-SOURCE VOLTAGE



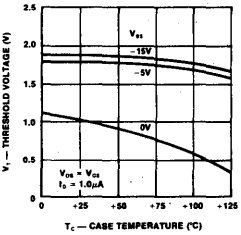
THRESHOLD VOLTAGE vs BODY-TO-SOURCE VOLTAGE



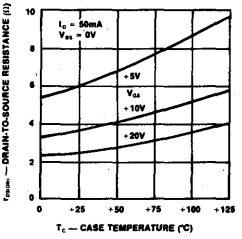
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



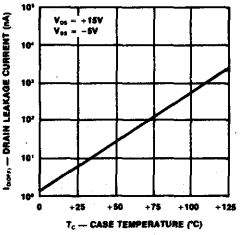
THRESHOLD VOLTAGE vs CASE TEMPERATURE



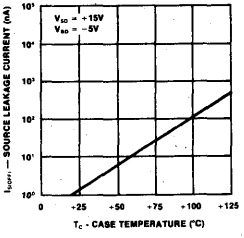
DRAIN-TO-SOURCE RESISTANCE vs CASE TEMPERATURE



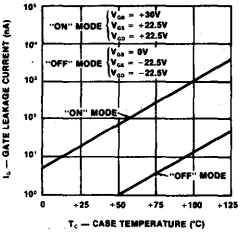
DRAIN LEAKAGE CURRENT vs CASE TEMPERATURE



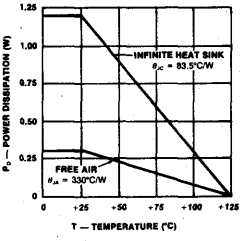
SOURCE LEAKAGE CURRENT vs CASE TEMPERATURE



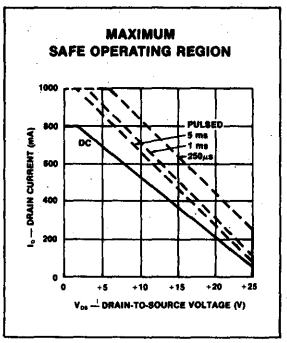
GATE LEAKAGE CURRENT vs CASE TEMPERATURE



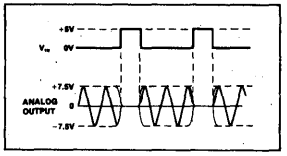
POWER DISSIPATION vs TEMPERATURE



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



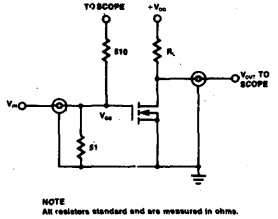
TYPICAL WAVEFORMS



SWITCHING CHARACTERISTICS

V_{GG}(V)	V_{DD}(V)	R_L(Ω)	$t_{d(ON)}$(ns) Typ	t_r(ns) Typ	t_{OFF}(ns) Typ
5	5	100	<1	1	3
	10	200	<1	1	3
	20	390	<1	1	3
10	5	67	<1	1	3
	10	133	<1	1	3
	20	270	<1	1	3

TEST CIRCUIT

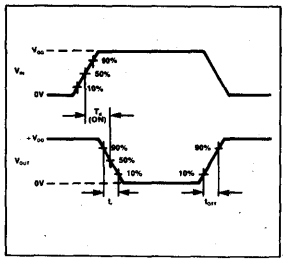


NOTE
All resistors standard and are measured in ohms.

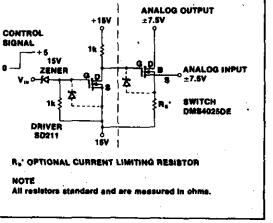
INPUT PULSE
t_d, t_r <1ns
PULSE WIDTH = 10ns
REP RATE = 1MHz

SAMPLING SCOPE
t_r <360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

SWITCHING WAVEFORMS

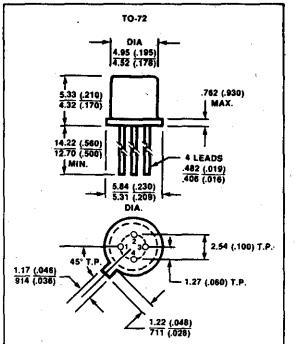


D-MOS DRIVER/SWITCH APPLICATION



NOTE
All resistors standard and are measured in ohms.

PACKAGE INFORMATION



NOTES
1. Lead Material: Kover or equivalent—gold plated.
2. Body Material: Eyelet, Kover or equivalent—gold plated, glass body.
3. Lid Material: Nickel, weld seal
4. All dimensions shown in parenthesis are English (inches)

D-MOS POWER FET SINGLE GATE N-CHANNEL ENHANCEMENT

DESCRIPTION

The Signetics SD220 is a POWER MOSFET of the N-channel enhancement mode type designed for switching and amplifier applications requiring high voltage, high current, high speed, and exceptional linear transfer characteristics. Superior performance is achieved by utilizing the Signetics D-MOS process which provides high gain, low inter-electrode capacitances, low drain-to-source "ON" resistance, and enhanced high frequency operation.

The device is hermetically sealed in a TO-39 package. The source, substrate, and case are internally connected.

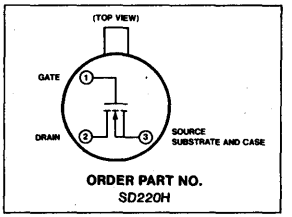
FEATURES

- **Low "ON" resistance: $<10\Omega$ @ 500mA**
- **High current: 500mA dc**
- **High voltage: $V_{DS} > +60V$**
- **Low input drive power**
- **Low inter-electrode capacitances**
- **Linear transfer characteristics**
- **No secondary breakdown**
- **Withstands high VSWR**

APPLICATIONS

- **Power amplification**
- **Power driver**
- **High speed switching**
- **Switching power supplies**

PIN CONFIGURATION



ORDER PART NO.
SD220H

ABSOLUTE MAXIMUM RATINGS[1] T_A = +25°C unless otherwise specified.

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source	+60	V
V_{GS}	Gate-to-source	±20	V
V_{DG}	Drain-to-gate	+60 −20	V
$I_{D(ON)}$	"ON" drain current		
	Continuous	500	mA
	Pulsed (80μs, 1% duty cycle)	800	mA
P_D	Power dissipation		
	T_A = +25°C[2]	1	W
	T_C = +25°C[3]	6.25	W
	Power derating factors		
	Free air	8	mW/°C
	Infinite heat sink	50	mW/°C
Θ_{JA}	Thermal resistance	125	°C/W
Θ_{JC}	Thermal resistance	20	°C/W
T_{op}	Operating temperature	−55 to +125	°C
T_{STG}	Storage temperature	−55 to +150	°C

NOTES
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Free air.
3. Infinite heat sink.

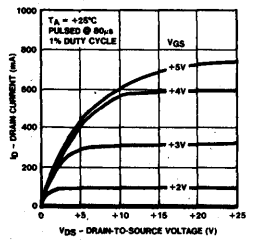
ELECTRICAL CHARACTERISTICS $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
BV_{DS}	Drain-source Breakdown voltage	$V_{GS} = V_{SB} = 0$, $I_D = 1\mu A$	60	100		V
I_{GSS}	Gate leakage current	$V_{GSS} = \pm 20V$			1.0	nA
$I_{D(OFF)}$	Drain leakage current	$V_{DS} = +60V$, $V_{GS} = 0$		0.1	1.0	μA
$I_{D(ON)}$	Drain "ON" current	$V_{DS} = +6V$, $V_{GS} = +10V$	500			mA
$I_{D(ON)}$	Drain "ON" current[4]	$V_{DS} = +10V$, $V_{GS} = +10V$	600	700		mA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $I_D = 10\mu A$ $V_{DS} = V_{GS} = V_T$, $I_D = 1mA$	0.1 0.5	0.8 1.5	2.3 3.0	V V
$r_{DS(ON)}$	Drain-source "ON" resistance[4]	$V_{GS} = +5V$, $I_D = 50mA$ $V_{GS} = +10V$, $I_D = 50mA$ $V_{GS} = +10V$, $I_D = 500mA$		7.5 6.5 9	10 9 12	Ω Ω Ω
g_{fs}	Forward transconductance[4]	$V_{DS} = +30V$, $I_D = 300mA$	220	250		mmhos
	Capacitances	$V_{DS} = +30V$, $I_D = 0$, f = 1MHz				
C_{iss}	Input			12	15	pF
C_{oss}	Output			2.8	3.5	pF
C_{rss}	Reverse transfer			0.6	1.0	pF
$t_{d(ON)}$	Turn-ON Delay Time	See switching		1	2	ns
t_r	Rise Time	Time test		1	3	ns
t_f	Fall Time	Circuit		3	5	ns

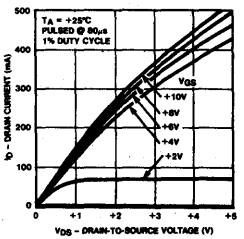
NOTE
4. Pulsed @ 80μs, 1% duty cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

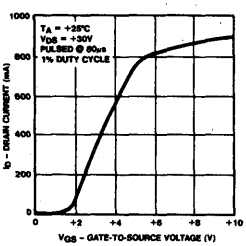
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

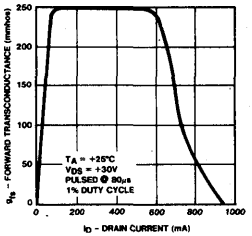


DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

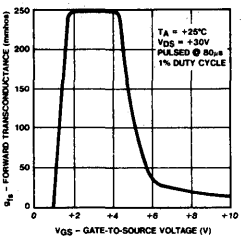


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

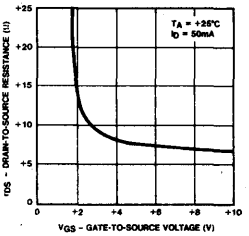
FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



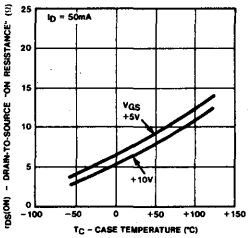
FORWARD TRANSCONDUCTANCE vs GATE-TO-SOURCE VOLTAGE



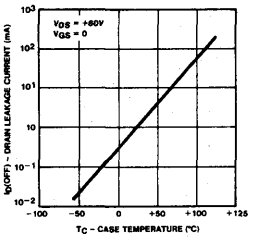
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



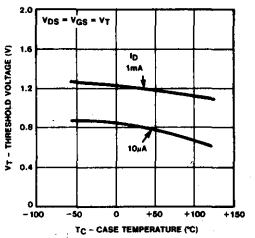
DRAIN-TO-SOURCE "ON RESISTANCE" vs CASE TEMPERATURE



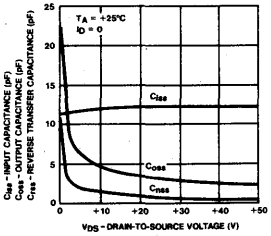
DRAIN LEAKAGE CURRENT vs CASE TEMPERATURE



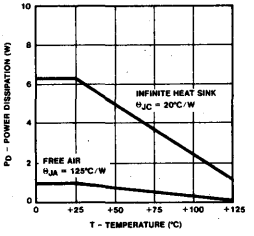
THRESHOLD VOLTAGE vs CASE TEMPERATURE



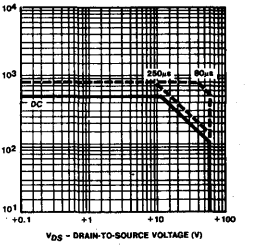
CAPACITANCES vs DRAIN-TO-SOURCE VOLTAGE



POWER DISSIPATION vs TEMPERATURE

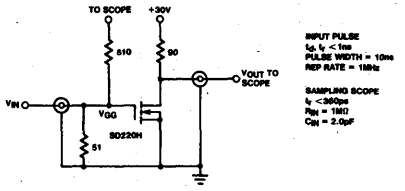


MAXIMUM SAFE OPERATING REGION



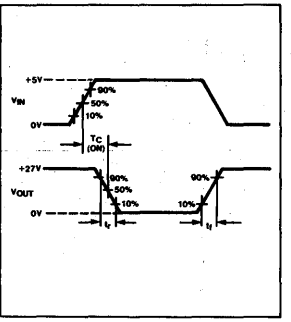
SWITCHING SPEED

TEST CIRCUIT

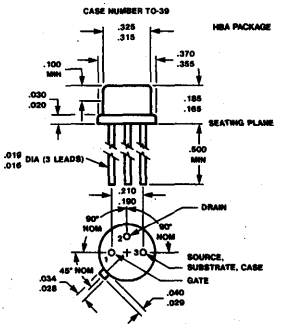


NOTE
All resistors standard and are measured in ohms.

WAVEFORM



PACKAGE OUTLINE



PRELIMINARY SPECIFICATION

D-MOS POWER FET SINGLE GATE N-CHANNEL ENHANCEMENT

DESCRIPTION

The Signetics SD222 is a POWER MOSFET of the N-channel enhancement mode type designed for switching applications requiring high voltage, high current, low "ON" resistance and high node-to-node isolation. Superior performance is achieved by utilizing the Signetics D-MOS process which provides high gain, low inter-electrode capacitances, low drain-to-source "ON" resistance and enhanced high frequency operation.

The device is hermetically sealed in a 4-lead TO-72 package.

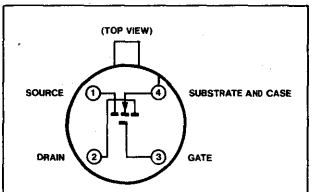
FEATURES

- **Low node capacitances**
- **Low feedthrough and feedback transients**
- **Excellent input and output isolations**
- **Extremely low input drive power**
- **High voltage: $V_{DS} > +60V$**

APPLICATIONS

- **Power driver**
- **High speed switching**
- **Analog switching**
- **Multiplexers**
- **Sample and hold**

PIN CONFIGURATION



ORDER PART NO.
SD222DC

ABSOLUTE MAXIMUM RATINGS[1] $T_A = +25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source	+60	V
V_{DB}	Drain-to-body	+60	V
V_{DG}	Drain-to-gate	+60 −20	V
V_{GS}	Gate-to-source	±20	V
V_{GB}	Gate-to-body	±20	V
V_{SB}	Source-to-body	+10	V
$I_D(ON)$	"ON" Drain current		
	Continuous	350	mA
	Pulsed (80μs, 1% duty cycle)	800	mA
P_D	Power dissipation		
	$T_A = +25°C$[2]	300	mW
	$T_C = 25°C$[3]	1.2	W
	Power derating factors		
	Free air	2.4	mW/°C
	Infinite heat sink	9.6	mW/°C
Θ_{JA}	Thermal resistance	417	°C/W
Θ_{JC}	Thermal resistance	104	°C/W
T_{op}	Operating temperature	−55 to +125	°C
T_{STG}	Storage temperature	−55 to +150	°C

NOTES
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Free air.
3. Infinite heat sink.

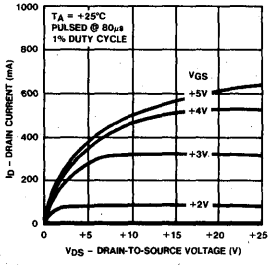
ELECTRICAL CHARACTERISTICS $T_A = +25°C$

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
BV_{DS}	Drain-source breakdown voltage	$V_{GS} = V_{SB} = 0$, $I_D = 1\mu A$	+60	+100		V
BV_{SB}	Source-Body breakdown voltage	$V_{GB} = 0$, Drain Open, $I_S = 1\mu A$	10			V
I_{GSS}	Gate leakage current	$V_{GSS} = \pm 20V$			1.0	nA
I_D (OFF)	Drain leakage current	$V_{DS} = +60V$, $V_{GS} = V_{SB} = 0$		0.1	1	μA
I_D (ON)	Drain "ON" current	$V_{DS} = +3.5V$, $V_{SB} = 0$, $V_{GS} = +10V$	275			mA
I_D (ON)	Drain "ON" current[4]	$V_{DS} = +6.5V$, $V_{SB} = 0$, $V_{GS} = +10V$	500	720		mA
V_T	Threshold voltage	$V_{DS} = V_{GS} = V_T$, $V_{SB} = 0$, $I_D = 10\mu A$ $V_{DS} = V_{GS} = V_T$, $V_{SB} = 0$, $I_D = 1mA$	0.1 0.5	0.8 1.5	2.3 3.0	V V
r_{DS} (ON)	Drain-source "ON" resistance[4]	$V_{GS} = +5V$, $V_{SB} = 0$, $I_D = 50mA$ $V_{GS} = +10V$, $V_{SB} = 0$, $I_D = 50mA$ $V_{GS} = +10V$, $V_{SB} = 0$, $I_D = 500mA$		7.5 6.5 9	10 9 13	Ω Ω Ω
g_{fs}	Forward transconductance[4]	$V_{DS} = +30V$, $V_{SB} = 0$, $I_D = 300mA$	220	250		mmhos
	Capacitances	$V_{DSS} = +30V$, $I_D = 0$, f = 1MHz				
C_{iss}	Input			12	15	pF
C_{oss}	Output			2.8	3.5	pF
C_{rss}	Reverse transfer			0.6	1.0	pF
t_d (ON)	Turn-ON delay time	See switching		1	2	ns
t_r	Rise time	Time test		1	3	ns
t_f	Fall time	Circuit		3	5	ns

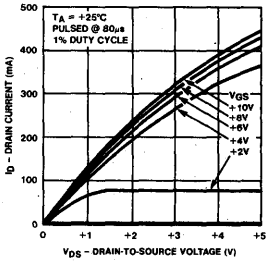
NOTE
4. Pulsed @ 80μs, 1% duty cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

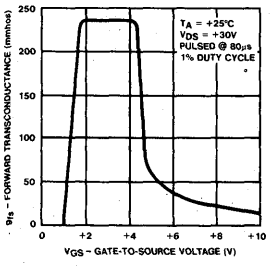
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

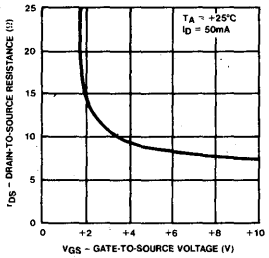


FORWARD TRANSCONDUCTANCE vs GATE-TO-SOURCE VOLTAGE

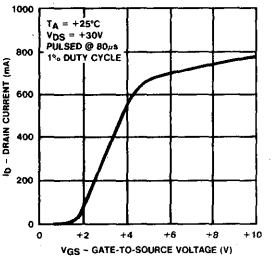


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

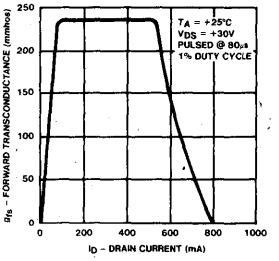
DRAIN TO SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



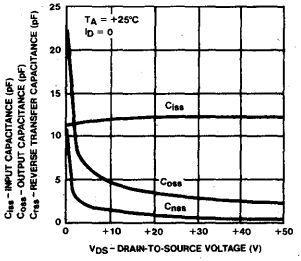
DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE



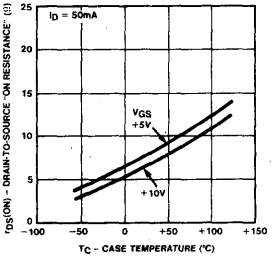
FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



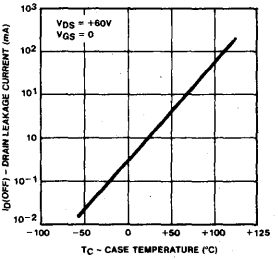
CAPACITANCES vs DRAIN-TO-SOURCE VOLTAGE



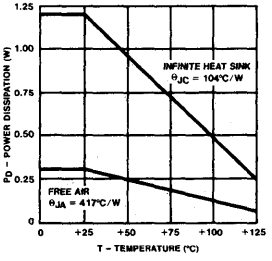
DRAIN-TO-SOURCE "ON" RESISTANCE vs CASE TEMPERATURE



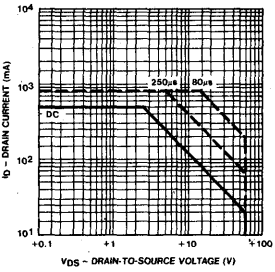
DRAIN LEAKAGE CURRENT vs CASE TEMPERATURE



POWER DISSIPATION vs TEMPERATURE

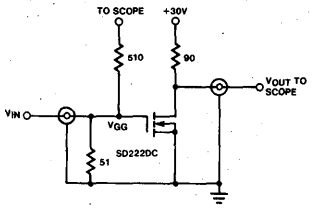


MAXIMUM SAFE OPERATING REGION



SWITCHING SPEED

TEST CIRCUIT

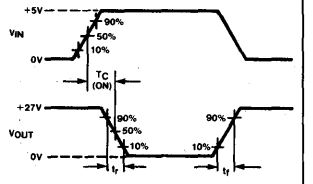


INPUT PULSE
t_d, t_f < 1ns
PULSE WIDTH = 10ns
REP RATE = 1MHz

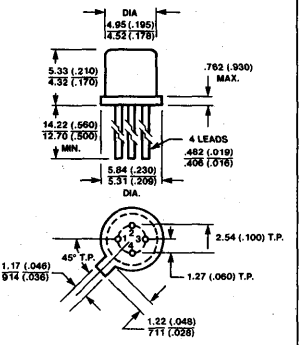
SAMPLING SCOPE
t_r ~ 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

NOTE
All resistors standard and are measured in ohms

WAVEFORM



PACKAGE INFORMATION



NOTES
1. Lead Material: Kover or equivalent—gold plated.
2. Body Material: Eyelet, Kover or equivalent—gold plated.
3. Lid Material: Nickel, weld seal.
4. All dimensions shown in parenthesis are English (inches).

D-MOS POWER FET SINGLE GATE N-CHANNEL ENHANCEMENT

DESCRIPTION

The Signetics SD226 is a POWER MOSFET of the N-channel enhancement mode type designed for switching and amplifier applications requiring high current, high speed, and exceptionally linear transfer characteristics. Superior performance is achieved by utilizing the Signetics D-MOS process which provides high gain, low drain-to-source "ON" resistance, low inter-electrode capacitances, and enhanced high frequency operation.

The device is hermetically sealed in a TO-39 package. The source, substrate, and case are internally connected.

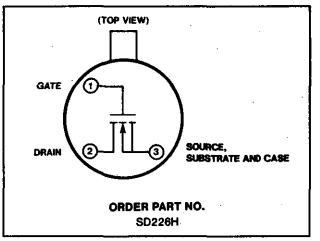
FEATURES

- **Low "ON" resistance: 1Ω @ 1A**
- **High current: 2A dc, 3A pulsed**
- **Withstands high VSWR**
- **No secondary breakdown**
- **Low drive power**
- **Low inter-electrode capacitances**
- **Linear transfer characteristics**

APPLICATIONS

- **Power amplification**
- **Power driver**
- **High speed switching**
- **Motor controls**
- **Switching power supplies**
- **Analog switching**

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS[1] T_A = +25°C unless otherwise specified

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source	+30	V
V_{GS}	Gate-to-source	±20	V
V_{GD}	Gate-to-drain	+20 −30	V
$I_{D(ON)}$	Continuous drain current	2	A
$I_{D(ON)}$	Pulsed drain current	3	A
P_D	Power dissipation		
	T_A = 25°C[2]	1	W
	T_C = 25°C[3]	6.25	W
	Power derating factors		
	Free Air	8	mW/°C
	Infinite Heat Sink	50	mW/°C
Θ_{JA}	Thermal Resistance[2]	125	°C/W
Θ_{JC}	Thermal Resistance[3]	20	°C/W
T_{op}	Operating Temperature	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to +150	°C

NOTES

1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Free air.
3. Infinite heat sink.

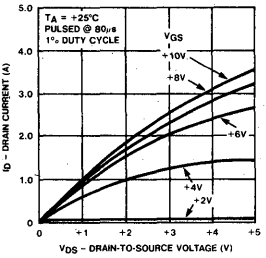
ELECTRICAL CHARACTERISTICS T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
BV_{DS}	Drain-source breakdown voltage	V_{GS} = V_{SB} = 0, I_D = 1μA	+30	+35		V
I_{GSS}	Gate leakage current	V_{GSS} = ±20V			1.0	nA
$I_{D(OFF)}$	Drain leakage current	V_{DS} = +30V, V_{GS} = 0		0.1	1	μA
$I_{D(ON)}$	Drain "ON" current	V_{DS} = +2.2V, V_{GS} = +10V	1.4	2.0		A
$I_{D(ON)}$	Drain "ON" current[4]	V_{DS} = +3.3V, V_{GS} = +10V	2.2	3.0		A
V_T	Threshold voltage	V_{DS} = V_{GS} = V_T, I_D = 10μA	0.1	1.0	2.3	V
		V_{DS} = V_{GS} = V_T, I_D = 1mA	0.5	1.5	3.0	V
$r_{DS(ON)}$	Drain-source "ON" resistance[4]	V_{GS} = +5V, I_D = 50mA		1.4	2.0	Ω
		V_{GS} = +10V, I_D = 50mA		1.1	1.5	Ω
		V_{GS} = +10V, I_D = 3A		1.1	1.5	Ω
g_{fs}	Forward transconductance[4]	V_{DS} = +15V, I_D = 2A	700	750		mmhos
	Capacitances	V_{DS} = +15V, I_D = 0, f = 1MHz				
C_{iss}	Input			35	45	pF
C_{oss}	Output			20	25	pF
C_{rss}	Reverse transfer			5	6	pF
$t_{d(ON)}$	Turn-ON delay time	See Switching		1	2	ns
t_r	Rise time	Time Test		1	3	ns
t_f	Fall time	Circuit		3	5	ns

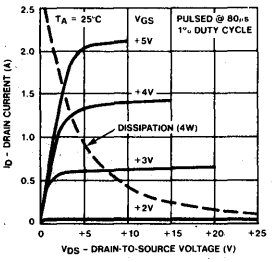
NOTE
4. Pulsed @ 80μs, 1% duty cycle.

TYPICAL PERFORMANCE CHARACTERISTICS

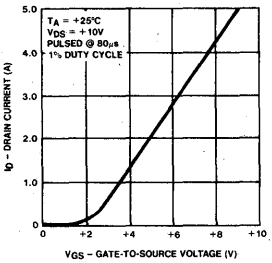
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE

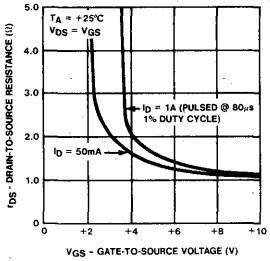


DRAIN CURRENT vs GATE-TO-SOURCE VOLTAGE

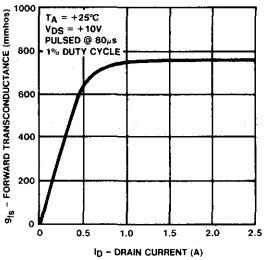


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

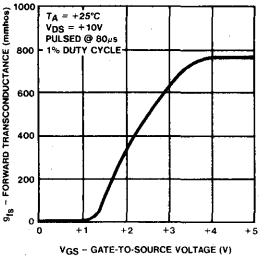
DRAIN-TO-SOURCE RESISTANCE vs GATE-TO-SOURCE VOLTAGE



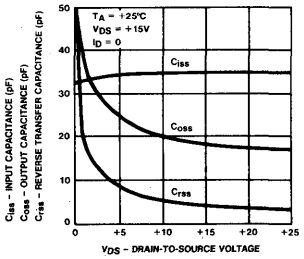
FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



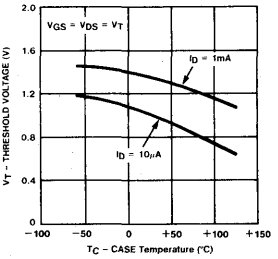
FORWARD TRANSCONDUCTANCE vs GATE-TO-SOURCE VOLTAGE



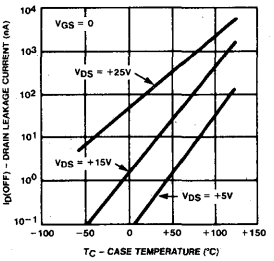
CAPACITANCES vs DRAIN-TO-SOURCE VOLTAGE



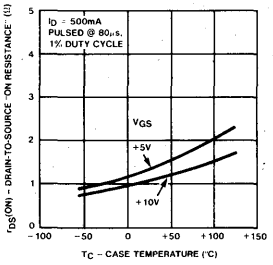
THRESHOLD VOLTAGE vs CASE TEMPERATURE



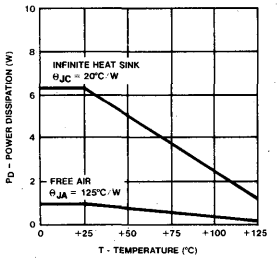
DRAIN LEAKAGE CURRENT vs CASE TEMPERATURE



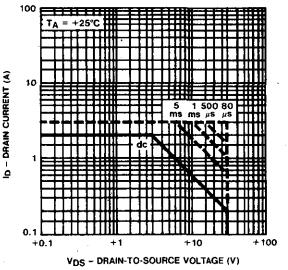
DRAIN-TO-SOURCE "ON RESISTANCE" vs CASE TEMPERATURE



POWER DISSIPATION vs TEMPERATURE



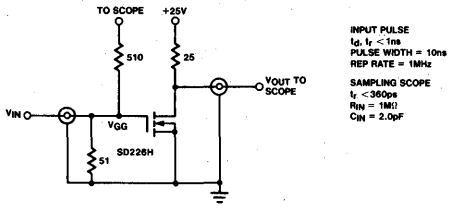
MAXIMUM SAFE OPERATING REGION



PRELIMINARY SPECIFICATION

SWITCHING SPEED

TEST CIRCUIT

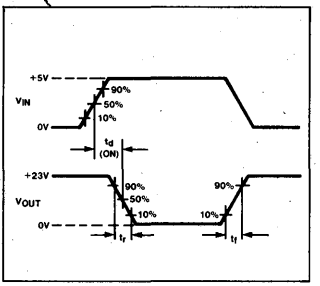


INPUT PULSE
t_d, t_r < 1ns
PULSE WIDTH = 10ns
REP RATE = 1MHz

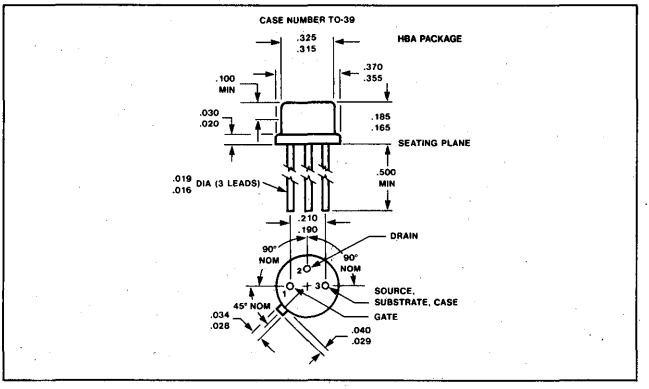
SAMPLING SCOPE
t_r < 360ps
R_{IN} = 1MΩ
C_{IN} = 2.0pF

NOTE
All resistors standard and are measured in ohms.

WAVEFORM



PACKAGE OUTLINE



SD304DE

D-MOS FET DUAL GATE N-CHANNEL ENHANCEMENT

DESCRIPTION

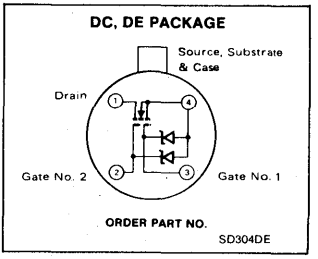
The Signetics D-MOS SD304 is a silicon, dual-insulated-gate, field effect transistor of the N-channel enhancement mode type. It is fabricated by the Signetics double-diffused process which gives superior high frequency performance. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of −0.3 V to +25.0 V. Thus the gates are protected against damage in all normal handling and operating situations.

The device characteristics make them ideally suited for a variety of high frequency amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure, has made the feedback capacity (Crss) less than 0.02 pF. A wide AGC capability plus a significant reduction in cross-modulation distortion is now available because of the inherent linearity of this device. The SD304 is hermetically sealed in a modified 4-lead TO-72 package.

GENERAL FEATURES

- **Lower cross-modulation and wider dynamic range than bipolar or single gate FETs**
- **Reverse AGC capability**
- **Linear mixing capability**
- ***Diode protected gates***
- **High forward transconductance: 10mmhos**
- **ION-implanted**
- **Positive bias only**

PIN CONFIGURATIONS (Top View)



FEATURES

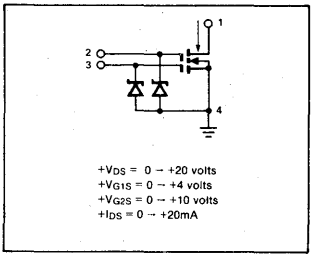
PARAMETER	SD304	UNIT
High gain through VHF range	16	dB at 500MHz
Low noise through VHF range	5	dB at 500MHz
Low input capacitance	2.5	pF
Low feedback capacitance	0.03	pF
Low outut capacitance	1.0	pF

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C *unless otherwise specified.*

	PARAMETER	RATING	UNIT
V_{DS}	Drain-to-source	+25	V
V_{G1B}	DC gate no. 1-to-substrate voltage	-0.3, +10	V
V_{G2B}	DC gate no. 2-to-substrate voltage	-0.3, +15	V
I_D	Drain current	50	mA
T_A	Ambient temperature range		
	Storage	-65 to +175	°C
	Operating	-55 to +125	°C
P_T	Transistor dissipation		
	At +25°C case temperature (Derate linearly to +125°C case temperature at the rate of 8.0mW/°C.)	1.2	W
	At +25°C free-air temperature (Derate linearly to +125°C free-air temperature at the rate of 2.0mW/°C.)	300	mW

DUAL GATE CASCODE BIAS SCHEME



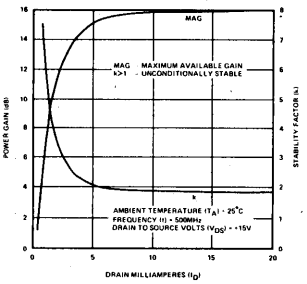
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	Min	Typ	Max	UNIT
BV_{DS}	Drain-to-source Breakdown voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	25	30		V
I_{G1SS}	Gate 1 Leakage current	$V_{G1S} = +5V$, $V_{G2S} = V_{DS} = 0V$		0.001	0.1	μA
I_{G2SS}	Gate 2 Leakage current	$V_{G2S} = +10V$ $V_{G1S} = V_{DS} = 0V$		0.001	0.1	μA
$I_{D(OFF)}$	Drain-to-source Leakage current	$V_{DS} = +15V$, $V_{G1S} = V_{G2S} = 0V$		0.001	0.1	μA
I_{DSS}	Zero bias Drain current	$V_{DS} = +15V$ $V_{G1S} = V_{G2S} = 0V$		0.001	0.1	μA
V_{T1}	Gate 1 Threshold voltage	$V_{DS} = V_{G1S} = V_{T1}$ $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	1.0	2.0	V
V_{T2}	Gate 2 Threshold voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +4V$, $I_D = 1\mu A$	0.1	1.0	2.0	V
$r_{DS(ON)}$	Drain-to-source On resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 1.0mA$		90	130	Ω

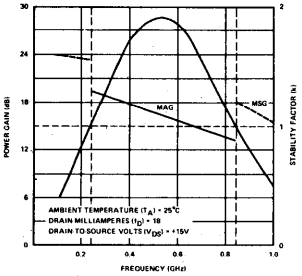
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	Min	Typ	Max	UNIT
	Small signal short circuit Capacitances	f = 1MHz, Gate 2 AC grounded				
C_{iss}	Input	$V_{DS} = +15V$, $V_{G1S} \cong 3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$		2.5	3.0	pF
C_{oss}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$ $V_{G2S} = +10V$		1.0	1.2	pF
C_{rss}	Reverse transfer	$V_{DS} = +15V$ $V_{G1S} = 0V$, $V_{G2S} = +10V$		0.03		pF
gfs	Forward transconductance	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$ $V_{G2S} = +10V$, $I_D = 18mA$, f = 1kHz	8.0	10.0		mmhos
Gps	Power gain	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$ f = 500MHz	13.0	16.0		dB
NF	Noise figure	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, $V_{G2S} = +10V$, $I_D = 18mA$ f = 500MHz		5.0	6.0	dB
E_{int}	Interfering signal level at gate for 1% cross-modulation distortion. Peak voltage referenced to 300Ω system.	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, Desired signal f = 500MHz, Undersired signal f = 501MHz		200		mV
AGC (V_{G2S})	Range of automatic Gain control	$V_{DS} = +15V$, $V_{G1S} \cong +3.5V$, f = 500MHz		40		dB

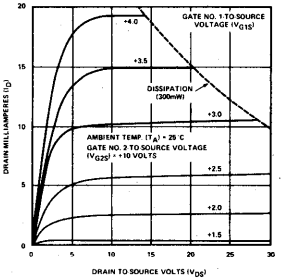
POWER GAIN vs DRAIN CURRENT



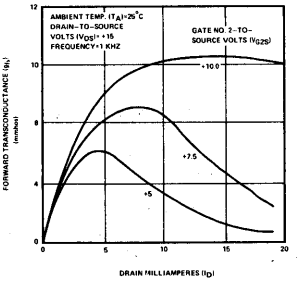
POWER GAIN vs FREQUENCY



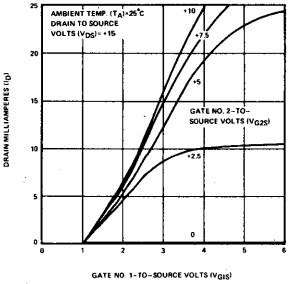
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



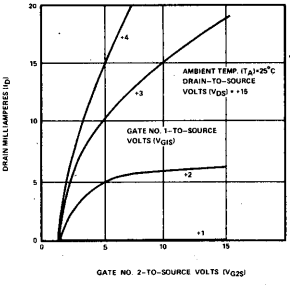
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



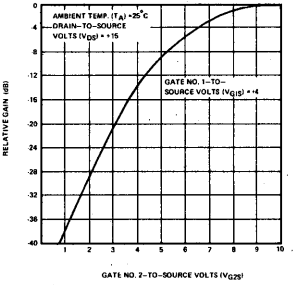
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE



AUTOMATIC GAIN CONTROL RANGE AT 500MHz

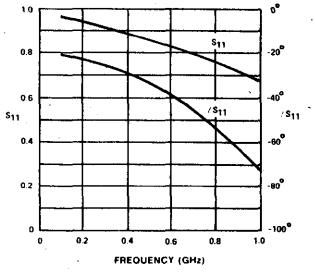


"S" PARAMETERS

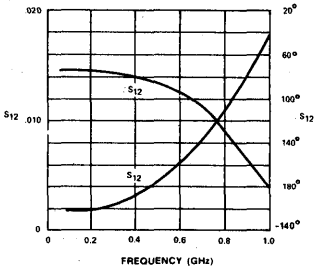
AMBIENT TEMP. (T_A) = +25° C
DRAIN MILLIAMPERES (I_D) = 18

DRAIN-TO-SOURCE VOLTS (V_{DS}) = +15
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) ≃ +3.5
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S}) = +10

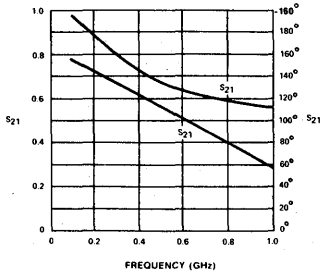
S_{11}



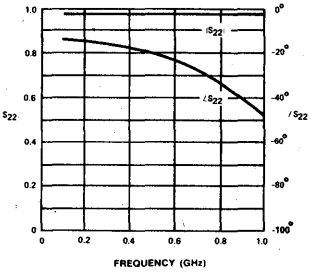
S_{12}



S_{21}



S_{22}



SD306DE

D-MOS FET DUAL GATE N-CHANNEL ENHANCEMENT

DESCRIPTION

The Signetics D-MOS SD306 is a silicon, dual-insulated gate, field-effect transistor of the N-channel enhancement mode type. Zener diodes are connected between the two gates and the substrate. These diodes bypass any voltage transients which lie outside the range of −0.3 V to +20.0 V. Thus, the gates are protected against damage in all normal handling and operating situations. The characteristics of the device makes them ideally suited for a variety of VHF amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure has made the feedback capacity (C_{G1D}) typically less than 0.03 pF. A wide AGC capability plus significant reduction in cross modulation distortion is now available because of the inherent linearity of the device. The SD306 is hermetically sealed in a 4-lead TO-72 package.

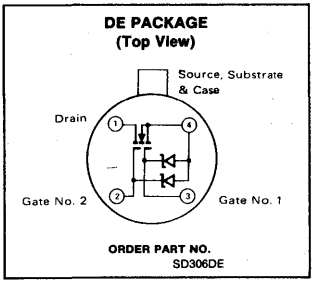
GENERAL FEATURES

- **Positive bias only**
- **Low gate voltages**
- **Enhancement mode operation**
- **Wide AGC range: -50dB at 200MHz**
- **Zener diode gate protection**
- **ION implanted for greater reliability**

FEATURES (VHF TV and FM RF Amplifier)

- **High power gain without neutralization: 20dB at 200MHz**
- **Low noise figure: 1.5dB at 200MHz**
- **Low input and output capacitance: 3.3pF and 1.0pF constant with AGC**
- **Low feedback capacitance: 0.03pF**
- **Superior cross modulation performance**
- **High transconductance: 15mmhos**

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

PARAMETER		RATING	UNIT
V_{DS}	Drain-to-source voltage	+20	V
V_{G1B}	Gate no. 1—to-substrate voltage	-0.3 to +20	Vdc
V_{G2B}	Gate no. 1—to-substrate voltage	-0.3 to +20	Vdc
I_D	Drain current	50	mA
T_A	Ambient temperature range		
	Storage	-65 to +175	°C
	Operating	-55 to +125	°C
P_T	Transistor dissipation		
	At 25°C case temperature (Derate linearly to 125°C case temperature at the rate of 8.0mW/°C)	1.2	W
	At 25°C free-air temperature (Derate linearly to 125°C free-air temperature at the rate of 2.0mW/°C)	300	mW

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	Min	Typ	Max	UNIT
OFF Characteristics						
BV_{DS}	Drain-to-source Breakdown voltage	$V_{G1S} = V_{G2S} = 0V$, $I_D = 5\mu A$	20	25		V
I_D (OFF)	Drain-to-source Leakage current	$V_{DS} = +15V$ $V_{G1S} = V_{G2S} = 0V$		0.001	1.0	μA
I_{DSS}	Zero bias drain current	$V_{DS} = +15V$ $V_{G1S} = V_{G2S} = 0V$		0.001	1.0	μA
I_{G1SS}	Gate no. 1 leakage current	$V_{G1S} = +5V$ $V_{G2S} = V_{DS} = 0V$		0.001	0.1	μA
I_{G2SS}	Gate no. 2 leakage current	$V_{G2S} = +10V$ $V_{G1S} = V_{DS} = 0V$		0.001	0.1	μA
ON Characteristics						
V_{T1}	Gate 1 threshold voltage	$V_{DS} = V_{G1S} = V_{T1}$, $V_{G2S} = +10V$, $I_D = 1\mu A$	0.1	0.5	1.5	V
V_{T2}	Gate 2 threshold voltage	$V_{DS} = V_{G2S} = V_{T2}$, $V_{G1S} = +5V$, $I_D = 1\mu A$	0.1	0.5	1.5	V
$r_{DS(ON)}$	Drain-to-source on resistance	$V_{G1S} = +5V$, $V_{G2S} = +10V$, $I_D = 1.0mA$		65	100	Ω

AC ELECTRICAL CHARACTERISTICS

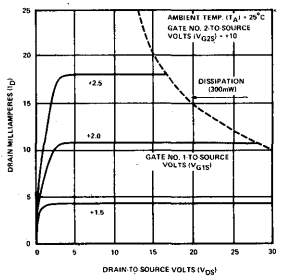
T_A = 25°C unless otherwise specified.

PARAMETER		TEST CONDITIONS	Min	Typ	Max	UNIT
Small signal characteristics						
g_{fs}	Forward transconductance	$V_{DS} = +15V$, $V_{G2S} = +10V$, f = 1kHz $I_D = 18mA$	13	15		mmhos
Capacitances		f = 1MHz, gate 2 AC grounded				
C_{G1S}	Input	$V_{DS} = +15V$, $V_{G2S} = +10V$ $I_D = 18mA$		3.3	3.6	pF
C_{DS}	Output	$V_{DS} = +15V$, $V_{G1S} = 0V$, $V_{G2S} = +10V$		1.0	1.3	pF
C_{G1D}	Reverse transfer	$V_{DS} = +15V$ $V_{G1S} = 0V$, $V_{G2S} = +10V$		0.03		pF
	Input admittance	f = 200MHz, $V_{DS} = +15V$	$V_{G2S} = +10V$, $I_D = 18mA$			
	$Re(Y_{11})$			1.11		mmhos
	$Im(Y_{11})$			4.76		mmhos
	Output admittance	f = 200MHz, $V_{DS} = +15V$				
	$Re(Y_{22})$			1.05		mmhos
	$Im(Y_{22})$			1.54		mmhos
	Forward transmittance	f = 200MHz, $V_{DS} = +15V$				
	$Re(Y_{21})$			13.23		mmhos
	$Im(Y_{21})$			-5.62		mmhos
	Reverse transmittance	f = 200MHz, $V_{DS} = +15V$				
	$Re(Y_{12})$			0.01		mmhos
	$Im(Y_{12})$			-0.04		mmhos
G_{ps}	Power gain[1]	$V_{DS} = +15V$, $V_{G2S} = +10V$ $I_D = 18mA$, f = 200MHz	17	20		dB
NF	Noise figure	$V_{DS} = +15V$, $V_{G2S} = +10V$, $I_D = 18mA$, f = 200MHz		1.5	2.5	dB
AGC_{VG2S}	Range of automatic gain control	$V_{DS} = +15V$, $V_{G1S} \cong +2.5V$, $V_{G2S} = +10V \rightarrow 0V$, f = 200MHz		50		dB
E_{INT}	Interfering signal level at gate 1 for 1% cross modulation distortion, peak voltage referenced to 50Ω system[2]	$V_{DS} = 15V$, $V_{G2S} = +8V$, $I_D = 15mA$ Wanted signal f = 200MHz interfering signal f = 196MHz		480		mV

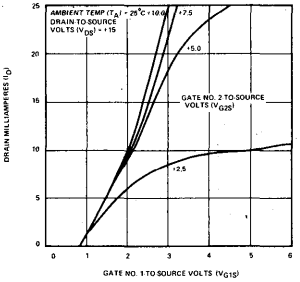
1. Measured in amplifier test fixture.
2. Measured as shown in block diagram.

TYPICAL PERFORMANCE CHARACTERISTICS

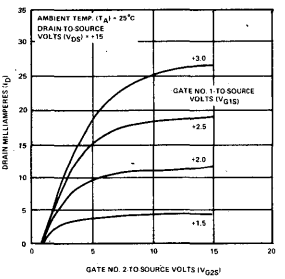
DRAIN CURRENT vs DRAIN-TO-SOURCE VOLTAGE



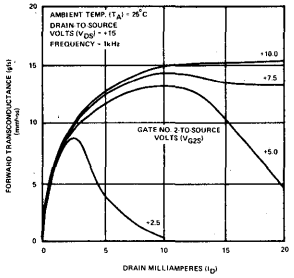
DRAIN CURRENT vs GATE NO. 1-TO-SOURCE VOLTAGE



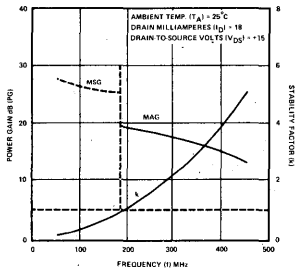
DRAIN CURRENT vs GATE NO. 2-TO-SOURCE VOLTAGE



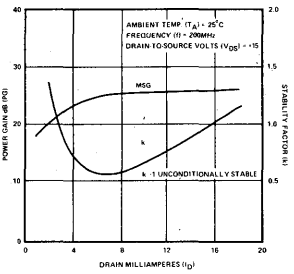
1kHz FORWARD TRANSCONDUCTANCE vs DRAIN CURRENT



POWER GAIN vs FREQUENCY

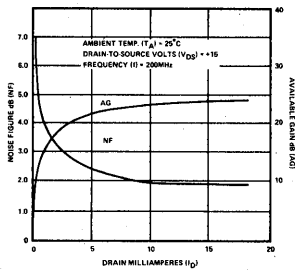


POWER GAIN vs DRAIN CURRENT

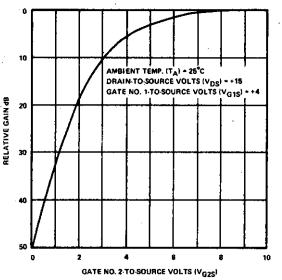


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

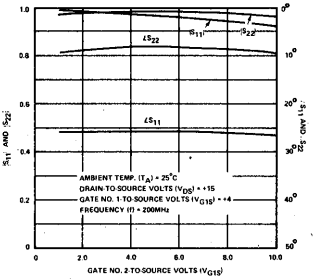
NOISE FIGURE AND AVAILABLE GAIN vs DRAIN CURRENT



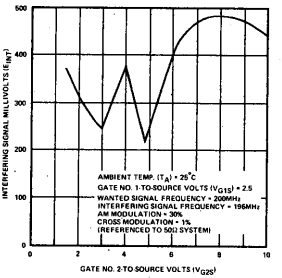
AUTOMATIC GAIN CONTROL RANGE AT 200MHz



S_{11} AND S_{22} vs AUTOMATIC GAIN CONTROL



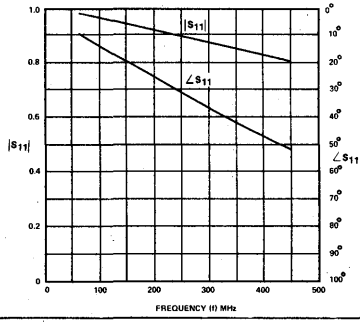
INTERFERING SIGNAL LEVEL vs GATE NO. 2-TO-SOURCE VOLTS



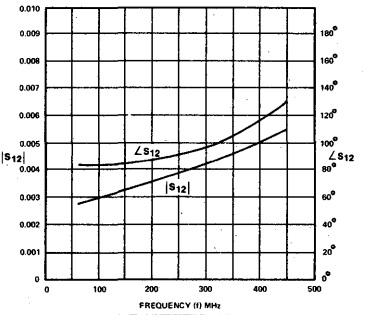
"S" PARAMETERS

AMBIENT TEMP. (T_A) = +25°C
DRAIN-TO-SOURCE VOLTS (V_{DS}) = 15
DRAIN MILLIAMPERES (I_D) = 8
GATE NO. 1-TO-SOURCE VOLTS (V_{G1S}) ≃ +2.5
GATE NO. 2-TO-SOURCE VOLTS (V_{G2S}) = +10

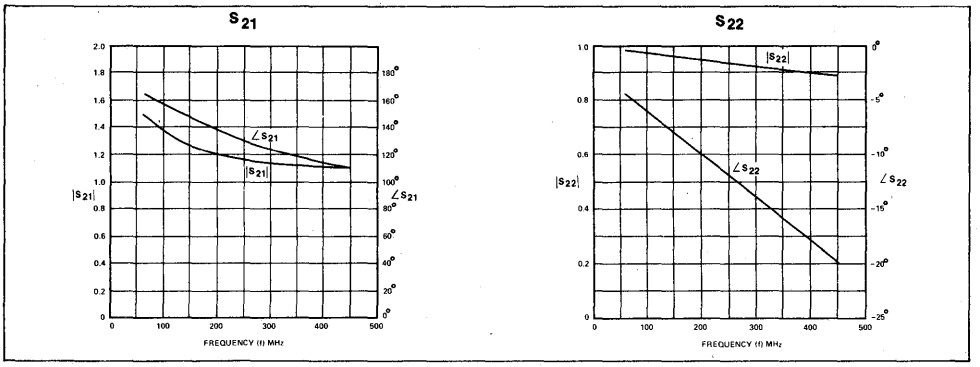
S_{11}



S_{12}

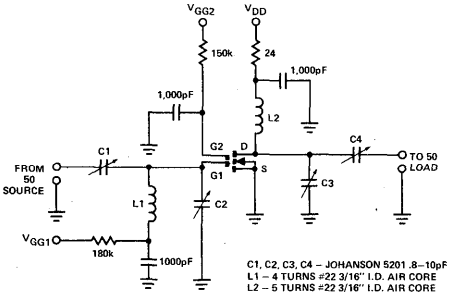


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

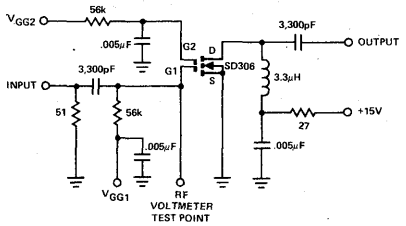


TEST CIRCUITS

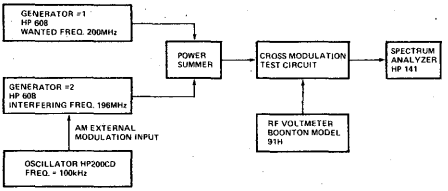
POWER GAIN, NOISE FIGURE 200MHz TEST AMPLIFIER;



CROSS MODULATION



BLOCK DIAGRAM OF CROSS MODULATION TEST



TEST PROCEDURE FOR CROSS MODULATION DISTORTION MEASUREMENTS

1. Modulation on Generator #2 is set at 100kHz, 30% AM modulation (sidebands down 15.6dB) with an output signal frequency equal to 196MHz.
2. Generator #2 is set at approximately -15dbm, 200MHz.
3. While observing the test circuit output spectrum, adjust the signal level of the interfering frequency so that the sidebands on the desired frequency are 46dB down from the carrier. This corresponds to 1% cross modulation.
4. Turn off Generator #1 and turnoff the modulation on Generator #2.
5. Using the RF voltmeter, measure the amplitude of the interfering signal at the test point.

SOLDERING RECOMMENDATIONS SOT-37
SOLDERING RECOMMENDATIONS SOT-103
ACCESSORIES

SOLDERING RECOMMENDATIONS SOT-37

Transistors in SOT-37 envelopes may be mounted with leads flat (Fig. 1) or bent (Figs 2 and 3). Different soldering procedures apply for the different styles of mounting.

FLAT-LEAD MOUNTING

Soldering by hand

Avoid putting any force on the leads during or just after soldering.

Solder the three leads one at a time, *not* simultaneously.

Proceed from one lead to the adjacent lead, *not* to the opposite one.

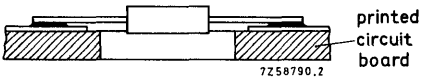


Fig. 1

Solder temperature	max.	300 °C
Soldering time	max.	5 s
Solder-to-case distance	min.	2 mm

BENT-LEAD MOUNTING

If leads are bent, all three may be soldered simultaneously if desired.

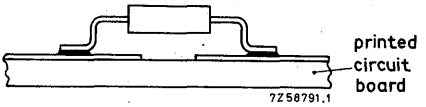


Fig. 2

Solder temperature	max.	300 °C
Soldering time	max.	10 s

DIP OR WAVE SOLDERING

When dip or wave soldering, the maximum allowable temperature of the solder is 260 °C. This temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the lead projections, but the temperature of the body must not exceed the specified storage maximum.

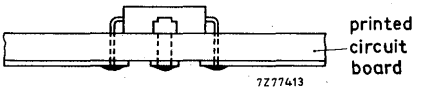


Fig. 3

Solder temperature	max.	260 °C
Soldering time	max.	5 s

SOLDERING RECOMMENDATIONS SOT-103

Transistors in SOT-103 envelopes may be mounted with leads flat (Fig. 1) or bent (Figs 2 and 3). Different soldering procedures apply for the different styles of mounting.

FLAT-LEAD MOUNTING

Soldering by hand

Avoid putting any force on the leads during or just after soldering.

Solder the four leads one at a time, *not* simultaneously.

Proceed from one lead to the adjacent lead, *not* to the opposite one.

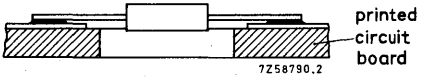


Fig. 1

Solder temperature	max.	300	°C
Soldering time	max.	5	s
Solder-to-case distance	min.	2	mm

BENT-LEAD MOUNTING

If leads are bent, all four may be soldered simultaneously if desired.

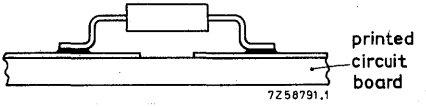


Fig. 2

Solder temperature	max.	300	°C
Soldering time	max.	10	s

DIP OR WAVE SOLDERING

When dip or wave soldering, the maximum allowable temperature of the solder is 260 °C. This temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the lead projections, but the temperature of the body must not exceed the specified storage maximum.

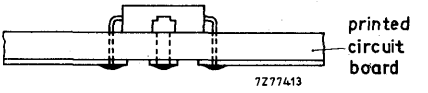


Fig. 3

Solder temperature	max.	260	°C
Soldering time	max.	5	s

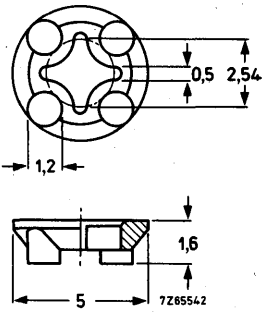
DISTANCE DISC

MECHANICAL DATA

Dimensions in mm

Fig. 2 **56246** for **TO-18** or **TO-72**

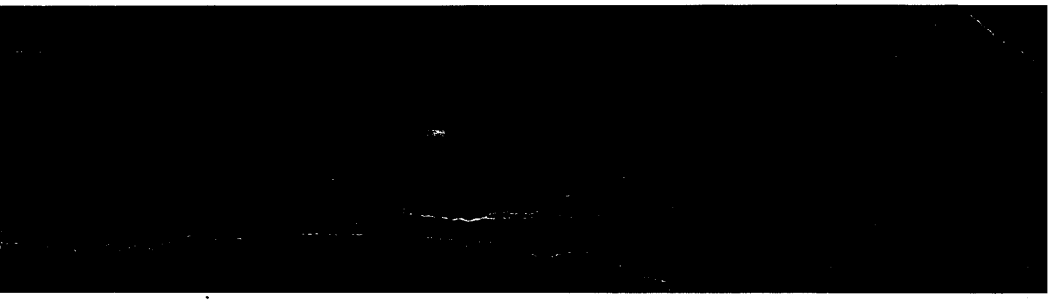
Insulating material.



TEMPERATURE

Maximum permissible temperature T max. 100 °C

FIELD-EFFECT TRANSISTORS



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Printed in The Netherlands

9398.106.60011