

**PHILIPS**

Data handbook



Electronic  
components  
and materials

Semiconductors

Part 9

January 1984

Power MOS transistors

# SEMICONDUCTORS

PART 9 - JANUARY 1984

## POWER MOS TRANSISTORS

DATA HANDBOOK SYSTEM  
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SELECTION GUIDE

GENERAL

TRANSISTOR DATA

MOUNTING INSTRUCTIONS

ACCESSORIES





## DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, sub-assemblies and materials; it is made up of four series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

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## ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks is comprised of the following parts:

- T1** Tubes for r.f. heating
- T2a** Transmitting tubes for communications, glass types
- T2b** Transmitting tubes for communications, ceramic types
- T3** Klystrons, travelling-wave tubes, microwave diodes
- ET3** Special Quality tubes, miscellaneous devices (will not be reprinted)
- T4** Magnetrons
- T5** Cathode-ray tubes  
Instrument tubes, monitor and display tubes, C.R. tubes for special applications
- T6** Geiger-Müller tubes
- T7** Gas-filled tubes  
Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories
- T8** Picture tubes and components  
Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display
- T9** Photo and electron multipliers  
Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates
- T10** Camera tubes and accessories, image intensifiers
- T11** Microwave semiconductors and components

## SEMICONDUCTORS (RED SERIES)

The red series of data handbooks is comprised of the following parts:

- S1 Diodes**  
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
- S2 Power diodes, thyristors, triacs**  
Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs
- S3 Small-signal transistors**
- S4a Low-frequency power transistors and hybrid modules**
- S4b High-voltage and switching power transistors**
- S5 Field-effect transistors**
- S6 R.F. power transistors and modules**
- S7 Microminiature semiconductors for hybrid circuits**
- S8 Devices for optoelectronics**  
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.
- S9 Power MOS transistors**
- S10 Wideband transistors and wideband hybrid IC modules**

## INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks is comprised of the following parts:

- IC1** Bipolar ICs for radio and audio equipment
- IC2** Bipolar ICs for video equipment
- IC3** ICs for digital systems in radio, audio and video equipment
- IC4** Digital integrated circuits  
CMOS HE4000B family
- IC5** Digital integrated circuits – ECL  
ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs
- IC6** Professional analogue integrated circuits
- IC7** Signetics bipolar memories
- IC8** Signetics analogue circuits
- IC9** Signetics TTL logic
- IC10** Signetics Integrated Fuse Logic (IFL)
- IC11** Microprocessors, microcomputers and peripheral circuitry

## COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks is comprised of the following parts:

- C1 Assemblies for industrial use**  
PLC modules, PC20 modules, HN1L FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs
- C2 Television tuners, video modulators, surface acoustic wave filters**
- C3 Loudspeakers**
- C4 Ferroxcube potcores, square cores and cross cores**
- C5 Ferroxcube for power, audio/video and accelerators**
- C6 Electric motors and accessories**  
Permanent magnet synchronous motors, stepping motors, direct current motors
- C7 Variable capacitors**
- C8 Variable mains transformers**
- C9 Piezoelectric quartz devices**  
Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements
- C10 Connectors**
- C11 Non-linear resistors**  
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
- C12 Variable resistors and test switches**
- C13 Fixed resistors**
- C14 Electrolytic and solid capacitors**
- C15 Film capacitors, ceramic capacitors**
- C16 Piezoelectric ceramics, permanent magnet materials**





## INDEX OF TYPE NUMBERS

Data Handbooks S1 to S10

The inclusion of a type number in this publication does not necessarily imply its availability.

type no.	book	section	type no.	book	section	type no.	book	section
AA119	S1	GD	BAS19	S7/S1	Mm/SD	BB109G	S1	T
AAZ15	S1	GD	BAS20	S7/S1	Mm/SD	BB112	S1	T
AAZ17	S1	GD	BAS21	S7/S1	Mm/SD	BB119	S1	T
AAZ18	S1	GD	BAT17	S7/S1	Mm/T	BB130	S1	T
BA220	S1	SD	BAT18	S7/S1	Mm/T	BB204B	S1	T
BA221	S1	SD	BAT81	S1	T	BB204G	S1	T
BA223	S1	T	BAT82	S1	T	BB212	S1	T
BA243	S1	T	BAT83	S1	T	BB405B	S1	T
BA244	S1	T	BAT85	S1	T	BB405G	S1	T
BA280	S1	T	BAV10	S1	SD	BB417	S1	T
BA314	S1	Vrg	BAV18	S1	SD	BB809	S1	T
BA315	S1	Vrg	BAV19	S1	SD	BB909A	S1	T
BA316	S1	SD	BAV20	S1	SD	BB909B	S1	T
BA317	S1	SD	BAV21	S1	SD	BBY31	S7/S1	Mm/T
BA318	S1	SD	BAV45	S1	Sp	BBY40	S7/S1	Mm/T
BA379	S1	T	BAV70	S7/S1	Mm/SD	BC107	S3	Sm
BA423	S1	T	BAV99	S7/S1	Mm/SD	BC108	S3	Sm
BA481	S1	T	BAW56	S7/S1	Mm/SD	BC109	S3	Sm
BA482	S1	T	BAW62	S1	SD	BC146	S3	Sm
BA483	S1	T	BAX12	S1	SD	BC177	S3	Sm
BA484	S1	T	BAX12A	S1	SD	BC178	S3	Sm
BAS11	S1	SD	BAX14	S1	SD	BC179	S3	Sm
BAS16	S7/S1	Mm/SD	BAX18	S1	SD	BC200	S3	Sm
BAS17	S7/S1	Mm/Vrg	BB105B	S1	T	BC264A	S5	FET
BAS18	S1	SD	BB105G	S1	T	BC264B	S5	FET

FET = Field-effect transistors

GD = Germanium diodes

Mm = Microminiature semiconductors  
for hybrid circuits

SD = Small-signal diodes

Sm = Small-signal transistors

Sp = Special diodes

T = Tuner diodes

Vrg = Voltage regulator diodes

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type no.	book	section	type no.	book	section	type no.	book	section
BC264C	S5	FET	BC868	S7	Mm	BCY71	S3	Sm
BC264D	S5	FET	BC869	S7	Mm	BCY72	S3	Sm
BC327;A	S3	Sm	BCF29;R	S7	Mm	BCY78	S3	Sm
BC328	S3	Sm	BCF30;R	S7	Mm	BCY79	S3	Sm
BC337;A	S3	Sm	BCF32;R	S7	Mm	BCY87	S3	Sm
BC338	S3	Sm	BCF33;R	S7	Mm	BCY88	S3	Sm
BC368	S3	Sm	BCF70;R	S7	Mm	BCY89	S3	Sm
BC369	S3	Sm	BCF81;R	S7	Mm	BD131	S4a	P
BC375	S3	Sm	BCV71;R	S7	Mm	BD132	S4a	P
BC376	S3	Sm	BCV72;R	S7	Mm	BD135	S4a	P
BC546	S3	Sm	BCW29;R	S7	Mm	BD136	S4a	P
BC547	S3	Sm	BCW30;R	S7	Mm	BD137	S4a	P
BC548	S3	Sm	BCW31;R	S7	Mm	BD138	S4a	P
BC549	S3	Sm	BCW32;R	S7	Mm	BD139	S4a	P
BC550	S3	Sm	BCW33;R	S7	Mm	BD140	S4a	P
BC556	S3	Sm	BCW60*	S7	Mm	BD201	S4a	P
BC557	S3	Sm	BCW61*	S7	Mm	BD202	S4a	P
BC558	S3	Sm	BCW69;R	S7	Mm	BD203	S4a	P
BC559	S3	Sm	BCW70;R	S7	Mm	BD204	S4a	P
BC560	S3	Sm	BCW71;R	S7	Mm	BD226	S4a	P
BC635	S3	Sm	BCW72;R	S7	Mm	BD227	S4a	P
BC636	S3	Sm	BCW81;R	S7	Mm	BD228	S4a	P
BC637	S3	Sm	BCW89;R	S7	Mm	BD229	S4a	P
BC638	S3	Sm	BCX17;R	S7	Mm	BD230	S4a	P
BC639	S3	Sm	BCX18;R	S7	Mm	BD231	S4a	P
BC640	S3	Sm	BCX19;R	S7	Mm	BD233	S4a	P
BC807	S7	Mm	BCX20;R	S7	Mm	BD234	S4a	P
BC808	S7	Mm	BCX51	S7	Mm	BD235	S4a	P
BC817	S7	Mm	BCX52	S7	Mm	BD236	S4a	P
BC818	S7	Mm	BCX53	S7	Mm	BD237	S4a	P
BC846	S7	Mm	BCX54	S7	Mm	BD238	S4a	P
BC847	S7	Mm	BCX55	S7	Mm	BD239	S4a	P
BC848	S7	Mm	BCX56	S7	Mm	BD239A	S4a	P
BC849	S7	Mm	BCX70*	S7	Mm	BD239B	S4a	P
BC850	S7	Mm	BCX71*	S7	Mm	BD239C	S4a	P
BC856	S7	Mm	BCY56	S3	Sm	BD240	S4a	P
BC857	S7	Mm	BCY57	S3	Sm	BD240A	S4a	P
BC858	S7	Mm	BCY58	S3	Sm	BD240B	S4a	P
BC859	S7	Mm	BCY59	S3	Sm	BD240C	S4a	P
BC860	S7	Mm	BCY70	S3	Sm	BD241	S4a	P

\* = series

FET = Field-effect transistors  
Mm = Microminiature semiconductors  
for hybrid circuits

P = Low-frequency power transistors  
Sm = Small-signal transistors

type no.	book	section	type no.	book	section	type no.	book	section
BD241A	S4a	P	BD676	S4a	P	BD940	S4a	P
BD241B	S4a	P	BD677	S4a	P	BD941	S4a	P
BD241C	S4a	P	BD678	S4a	P	BD942	S4a	P
BD242	S4a	P	BD679	S4a	P	BD943	S4a	P
BD242A	S4a	P	BD680	S4a	P	BD944	S4a	P
BD242B	S4a	P	BD681	S4a	P	BD945	S4a	P
BD242C	S4a	P	BD682	S4a	P	BD946	S4a	P
BD243	S4a	P	BD683	S4a	P	BD947	S4a	P
BD243A	S4a	P	BD684	S4a	P	BD948	S4a	P
BD243B	S4a	P	BD813	S4a	P	BD949	S4a	P
BD243C	S4a	P	BD814	S4a	P	BD950	S4a	P
BD244	S4a	P	BD815	S4a	P	BD951	S4a	P
BD244A	S4a	P	BD816	S4a	P	BD952	S4a	P
BD244B	S4a	P	BD817	S4a	P	BD953	S4a	P
BD244C	S4a	P	BD818	S4a	P	BD954	S4a	P
BD329	S4a	P	BD825	S4a	P	BD955	S4a	P
BD330	S4a	P	BD826	S4a	P	BD956	S4a	P
BD331	S4a	P	BD827	S4a	P	BDT20	S4a	P
BD332	S4a	P	BD828	S4a	P	BDT21	S4a	P
BD333	S4a	P	BD829	S4a	P	BDT29	S4a	P
BD334	S4a	P	BD830	S4a	P	BDT29A	S4a	P
BD335	S4a	P	BD839	S4a	P	BDT29B	S4a	P
BD336	S4a	P	BD840	S4a	P	BDT29C	S4a	P
BD337	S4a	P	BD841	S4a	P	BDT30	S4a	P
BD338	S4a	P	BD842	S4a	P	BDT30A	S4a	P
BD433	S4a	P	BD843	S4a	P	BDT30B	S4a	P
BD434	S4a	P	BD844	S4a	P	BDT30C	S4a	P
BD435	S4a	P	BD845	S4a	P	BDT31	S4a	P
BD436	S4a	P	BD846	S4a	P	BDT31A	S4a	P
BD437	S4a	P	BD847	S4a	P	BDT31B	S4a	P
BD438	S4a	P	BD848	S4a	P	BDT31C	S4a	P
BD645	S4a	P	BD849	S4a	P	BDT32	S4a	P
BD646	S4a	P	BD850	S4a	P	BDT32A	S4a	P
BD647	S4a	P	BD933	S4a	P	BDT32B	S4a	P
BD648	S4a	P	BD934	S4a	P	BDT32C	S4a	P
BD649	S4a	P	BD935	S4a	P	BDT41	S4a	P
BD650	S4a	P	BD936	S4a	P	BDT41A	S4a	P
BD651	S4a	P	BD937	S4a	P	BDT41B	S4a	P
BD652	S4a	P	BD938	S4a	P	BDT41C	S4a	P
BD675	S4a	P	BD939	S4a	P	BDT42	S4a	P

P = Low-frequency power transistors

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type no.	book	section	type no.	book	section	type no.	book	section
BDT42A	S4a	P	BDV65C	S4a	P	BDX64B	S4a	P
BDT42B	S4a	P	BDV66A	S4a	P	BDX64C	S4a	P
BDT42C	S4a	P	BDV66B	S4a	P	BDX65	S4a	P
BDT60	S4a	P	BDV66C	S4a	P	BDX65A	S4a	P
BDT60A	S4a	P	BDV66D	S4a	P	BDX65B	S4a	P
BDT60B	S4a	P	BDV67A	S4a	P	BDX65C	S4a	P
BDT60C	S4a	P	BDV67B	S4a	P	BDX66	S4a	P
BDT61	S4a	P	BDV67C	S4a	P	BDX66A	S4a	P
BDT61A	S4a	P	BDV67D	S4a	P	BDX66B	S4a	P
BDT61B	S4a	P	BDV91	S4a	P	BDX66C	S4a	P
BDT61C	S4a	P	BDV92	S4a	P	BDX67	S4a	P
BDT62	S4a	P	BDV93	S4a	P	BDX67A	S4a	P
BDT62A	S4a	P	BDV94	S4a	P	BDX67B	S4a	P
BDT62B	S4a	P	BDV95	S4a	P	BDX67C	S4a	P
BDT62C	S4a	P	BDV96	S4a	P	BDX68	S4a	P
BDT63	S4a	P	BDW55	S4a	P	BDX68A	S4a	P
BDT63A	S4a	P	BDW56	S4a	P	BDX68B	S4a	P
BDT63B	S4a	P	BDW57	S4a	P	BDX68C	S4a	P
BDT63C	S4a	P	BDW58	S4a	P	BDX69	S4a	P
BDT64	S4a	P	BDW59	S4a	P	BDX69A	S4a	P
BDT64A	S4a	P	BDW60	S4a	P	BDX69B	S4a	P
BDT64B	S4a	P	BDX35	S4a	P	BDX69C	S4a	P
BDT64C	S4a	P	BDX36	S4a	P	BDX77	S4a	P
BDT65	S4a	P	BDX37	S4a	P	BDX78	S4a	P
BDT65A	S4a	P	BDX42	S4a	P	BDX91	S4a	P
BDT65B	S4a	P	BDX43	S4a	P	BDX92	S4a	P
BDT65C	S4a	P	BDX44	S4a	P	BDX93	S4a	P
BDT91	S4a	P	BDX45	S4a	P	BDX94	S4a	P
BDT92	S4a	P	BDX46	S4a	P	BDX95	S4a	P
BDT93	S4a	P	BDX47	S4a	P	BDX96	S4a	P
BDT94	S4a	P	BDX62	S4a	P	BDY90	S4a	P
BDT95	S4a	P	BDX62A	S4a	P	BDY90A	S4a	P
BDT96	S4a	P	BDX62B	S4a	P	BDY91	S4a	P
BDV64	S4a	P	BDX62C	S4a	P	BDY92	S4a	P
BDV64A	S4a	P	BDX63	S4a	P	BF180	S3	Sm
BDV64B	S4a	P	BDX63A	S4a	P	BF181	S3	Sm
BDV64C	S4a	P	BDX63B	S4a	P	BF182	S3	Sm
BDV65	S4a	P	BDX63C	S4a	P	BF183	S3	Sm
BDV65A	S4a	P	BDX64	S4a	P	BF198	S3	Sm
BDV65B	S4a	P	BDX64A	S4a	P	BF199	S3	Sm

P = Low-frequency power transistors

Sm = Small-signal transistors

type no.	book	section	type no.	book	section	type no.	book	section
BF200	S3	Sm	BF569	S7	Mm	BFG91A	S10	WBT
BF240	S3	Sm	BF579	S7	Mm	BFG96	S10	WBT
BF241	S3	Sm	BF620	S7	Mm	BFP90A	S10	WBT
BF245A	S5	FET	BF621	S7	Mm	BFP91A	S10	WBT
BF245B	S5	FET	BF622	S7	Mm	BFP96	S10	WBT
BF245C	S5	FET	BF623	S7	Mm	BFQ10	S5	FET
BF246A	S5	FET	BF660;R	S7	Mm	BFQ11	S5	FET
BF246B	S5	FET	BF689K	S10	WBT	BFQ12	S5	FET
BF246C	S5	FET	BF767	S7	Mm	BFQ13	S5	FET
BF256A	S5	FET	BF819	S4b	HVP	BFQ14	S5	FET
BF256B	S5	FET	BF820	S7	Mm	BFQ15	S5	FET
BF256C	S5	FET	BF821	S7	Mm	BFQ16	S5	FET
BF324	S3	Sm	BF822	S7	Mm	BFQ17	S7	Mm
BF370	S3	Sm	BF823	S7	Mm	BFQ18A	S7	Mm
BF410A	S5	FET	BF857	S4b	HVP	BFQ19	S7	Mm
BF410B	S5	FET	BF858	S4b	HVP	BFQ22	S10	WBT
BF410C	S5	FET	BF859	S4b	HVP	BFQ22S	S10	WBT
BF410D	S5	FET	BF869	S4b	HVP	BFQ23	S10	WBT
BF419	S4b	HVP	BF870	S4b	HVP	BFQ24	S10	WBT
BF422	S3	Sm	BF871	S4b	HVP	BFQ32	S10	WBT
BF423	S3	Sm	BF872	S4b	HVP	BFQ33	S10	WBT
BF450	S3	Sm	BF926	S3	Sm	BFQ34	S10	WBT
BF451	S3	Sm	BF936	S3	Sm	BFQ34T	S10	WBT
BF457	S4b	HVP	BF939	S3	Sm	BFQ42	S6	RFP
BF458	S4b	HVP	BF960	S5	FET	BFQ43	S6	RFP
BF459	S4b	HVP	BF964	S5	FET	BFQ51	S10	WBT
BF469	S4b	HVP	BF966	S5	FET	BFQ52	S10	WBT
BF470	S4b	HVP	BF967	S3	Sm	BFQ53	S10	WBT
BF471	S4b	HVP	BF970	S3	Sm	BFQ63	S10	WBT
BF472	S4b	HVP	BF979	S3	Sm	BFQ65	S10	WBT
BF480	S3	Sm	BF980	S5	FET	BFQ66	S10	WBT
BF494	S3	Sm	BF981	S5	FET	BFQ68	S10	WBT
BF495	S3	Sm	BF982	S5	FET	BFR29	S5	FET
BF496	S3	Sm	BF989	S7	Mm	BFR30	S7	Mm
BF510	S7	Mm	BF990	S7	Mm	BFR31	S7	Mm
BF511	S7	Mm	BF991	S7	Mm	BFR49	S10	WBT
BF512	S7	Mm	BF992	S7	Mm	BFR53;R	S7	Mm
BF513	S7	Mm	BF994	S7	Mm	BFR54	S3	Sm
BF536	S7	Mm	BF996	S7	Mm	BFR64	S10	WBT
BF550;R	S7	Mm	BFG90A	S10	WBT	BFR65	S10	WBT

FET = Field-effect transistors

HVP = High-voltage power transistors

Mm = Microminiature semiconductors

for hybrid circuits

RFP = R.F. power transistors and modules

Sm = Small-signal transistors

WBT = Wideband hybrid IC transistors

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type no.	book	section	type no.	book	section	type no.	book	section
BFR84	S5	FET	BFX29	S3	Sm	BGY55	S10	WBM
BFR90	S10	WBT	BFX30	S3	Sm	BGY56	S10	WBM
BFR90A	S10	WBT	BFX34	S3	Sm	BGY57	S10	WBM
BFR91	S10	WBT	BFX84	S3	Sm	BGY58	S10	WBM
BFR91A	S10	WBT	BFX85	S3	Sm	BGY58A	S10	WBT
BFR92;R	S7	Mm	BFX86	S3	Sm	BGY59	S10	WBM
BFR92A;R	S7	Mm	BFX87	S3	Sm	BGY60	S10	WBM
BFR93;R	S7	Mm	BFX88	S3	Sm	BGY61	S10	WBT
BFR93A;R	S7	Mm	BFX89	S10	WBT	BGY65	S10	WBT
BFR94	S10	WBT	BFY50	S3	Sm	BGY67	S10	WBT
BFR95	S10	WBT	BFY51	S3	Sm	BGY70	S10	WBT
BFR96	S10	WBT	BFY52	S3	Sm	BGY71	S10	WBT
BFR96S	S10	WBT	BFY55	S3	Sm	BGY74	S10	WBM
BFR101A;B	S7	Mm	BFY90	S10	WBT	BGY75	S10	WBM
BFS17;R	S7	Mm	BG2000	S1	RT	BLV10	S6	RFP
BFS18;R	S7	Mm	BG2097	S1	RT	BLV11	S6	RFP
BFS19;R	S7	Mm	BGX11*	S2	ThM	BLV20	S6	RFP
BFS20;R	S7	Mm	BGX12*	S2	ThM	BLV21	S6	RFP
BFS21	S5	FET	BGX13*	S2	ThM	BLV25	S6	RFP
BFS21A	S5	FET	BGX14*	S2	ThM	BLV30	S6	RFP
BFS22A	S6	RFP	BGX15*	S2	ThM	BLV31	S6	RFP
BFS23A	S6	RFP	BGX17*	S2	ThM	BLV32F	S6	RFP
BFT24	S10	WBT	BGY22	S6	RFP	BLV33	S6	RFP
BFT25;R	S7	Mm	BGY22A	S6	RFP	BLV33F	S6	RFP
BFT44	S3	Sm	BGY23	S6	RFP	BLV36	S6	RFP
BFT45	S3	Sm	BGY23A	S6	RFP	BLV57	S6	RFP
BFT46	S7	Mm	BGY32	S6	RFP	BLW29	S6	RFP
BFT92;R	S7	Mm	BGY33	S6	RFP	BLW31	S6	RFP
BFT93;R	S7	Mm	BGY35	S6	RFP	BLW32	S6	RFP
BFW10	S5	FET	BGY36	S6	RFP	BLW33	S6	RFP
BFW11	S5	FET	BGY40A	S6	RFP	BLW34	S6	RFP
BFW12	S5	FET	BGY40B	S6	RFP	BLW50F	S6	RFP
BFW13	S5	FET	BGY41A	S6	RFP	BLW60	S6	RFP
BFW16A	S10	WBT	BGY41B	S6	RFP	BLW60C	S6	RFP
BFW17A	S10	WBT	BGY43	S6	RFP	BLW64	S6	RFP
BFW30	S10	WBT	BGY50	S10	WBM	BLW75	S6	RFP
BFW61	S5	FET	BGY51	S10	WBM	BLW76	S6	RFP
BFW92	S10	WBT	BGY52	S10	WBM	BLW77	S6	RFP
BFW92A	S10	WBT	BGY53	S10	WBM	BLW78	S6	RFP
BFW93	S10	WBT	BGY54	S10	WBM	BLW79	S6	RFP

\* = series

FET = Field-effect transistors

Mm = Microminiature semiconductors  
for hybrid circuits

RFP = R.F. power transistors and modules

RT = Tripler

Sm = Small-signal transistors

ThM = Thyristor Modules

WBM = Wideband hybrid IC modules

WBT = Wideband hybrid IC transistors

type no.	book	section	type no.	book	section	type no.	book	section
BLW80	S6	RFP	BLY87A	S6	RFP	BSR18;R	S7	Mm
BLW81	S6	RFP	BLY87C	S6	RFP	BSR18A;R	S7	Mm
BLW82	S6	RFP	BLY88A	S6	RFP	BSR30	S7	Mm
BLW83	S6	RFP	BLY88C	S6	RFP	BSR31	S7	Mm
BLW84	S6	RFP	BLY89A	S6	RFP	BSR32	S7	Mm
BLW85	S6	RFP	BLY89C	S6	RFP	BSR33	S7	Mm
BLW86	S6	RFP	BLY90	S6	RFP	BSR40	S7	Mm
BLW87	S6	RFP	BLY91A	S6	RFP	BSR41	S7	Mm
BLW89	S6	RFP	BLY91C	S6	RFP	BSR42	S7	Mm
BLW90	S6	RFP	BLY92A	S6	RFP	BSR43	S7	Mm
BLW91	S6	RFP	BLY92C	S6	RFP	BSR50	S3	Sm
BLW95	S6	RFP	BLY93A	S6	RFP	BSR51	S3	Sm
BLW96	S6	RFP	BLY93C	S6	RFP	BSR52	S3	Sm
BLW98	S6	RFP	BLY94	S6	RFP	BSR56	S7	Mm
BLX13	S6	RFP	BLY97	S6	RFP	BSR57	S7	Mm
BLX13C	S6	RFP	BPF10	S8	PDT	BSR58	S7	Mm
BLX14	S6	RFP	BPF24	S8	PDT	BSR60	S3	Sm
BLX15	S6	RFP	BPW22A	S8	PDT	BSR61	S3	Sm
BLX39	S6	RFP	BPW50	S8	PDT	BSR62	S3	Sm
BLX65	S6	RFP	BPX25	S8	PDT	BSS38	S3	Sm
BLX66	S6	RFP	BPX29	S8	PDT	BSS50	S3	Sm
BLX67	S6	RFP	BPX40	S8	PDT	BSS51	S3	Sm
BLX68	S6	RFP	BPX41	S8	PDT	BSS52	S3	Sm
BLX69A	S6	RFP	BPX42	S8	PDT	BSS60	S3	Sm
BLX91A	S6	RFP	BPX71	S8	PDT	BSS61	S3	Sm
BLX92A	S6	RFP	BPX72	S8	PDT	BSS62	S3	Sm
BLX93A	S6	RFP	BPX95C	S8	PDT	BSS63;R	S7	Mm
BLX94A	S6	RFP	BR100/03	S2	Th	BSS64;R	S7	Mm
BLX94C	S6	RFP	BRI01	S3	Sm	BSS68	S3	Sm
BLX95	S6	RFP	BRY39	S3	Sm	BST15	S7	Mm
BLX96	S6	RFP	BRY56	S3	Sm	BST16	S7	Mm
BLX97	S6	RFP	BRY61	S7	Mm	BST50	S7	Mm
BLX98	S6	RFP	BRY62	S7	Mm	BST51	S7	Mm
BLY33	S6	RFP	BSR12;R	S7	Mm	BST52	S7	Mm
BLY34	S6	RFP	BSR13;R	S7	Mm	BST60	S7	Mm
BLY35	S6	RFP	BSR14;R	S7	Mm	BST61	S7	Mm
BLY36	S6	RFP	BSR15;R	S7	Mm	BST62	S7	Mm
BLY83	S6	RFP	BSR16;R	S7	Mm	BSV15	S3	Sm
BLY84	S6	RFP	BSR17;R	S7	Mm	BSV16	S3	Sm
BLY85	S6	RFP	BSR17A;R	S7	Mm	BSV17	S3	Sm

Mm = Microminiature semiconductors  
for hybrid circuits  
PDT = Photodiodes or transistors

RFP = R.F. power transistors and modules  
Sm = Small-signal transistors  
Th = Thyristors



# INDEX

type no.	book	section	type no.	book	section	type no.	book	section
BSV52;R	S7	Mm	BTW58*	S2	Th	BUX82	S4b	SP
BSV64	S3	Sm	BTW63*	S2	Th	BUX83	S4b	SP
BSV78	S5	FET	BTW92*	S2	Th	BUX84	S4b	SP
BSV79	S5	FET	BTX18*	S2	Th	BUX85	S4b	SP
BSV80	S5	FET	BTX94*	S2	Tri	BUX86	S4b	SP
BSV81	S5	FET	BTY79*	S2	Th	BUX87	S4b	SP
BSW66A	S3	Sm	BTY87*	S2	Th	BUX88	S4b	SP
BSW67A	S3	Sm	BTY91*	S2	Th	BUX90	S4b	SP
BSW68A	S3	Sm	BU208A	S4b	SP	BUX98	S4b	SP
BSX19	S3	Sm	BU208B	S4b	SP	BUX98A	S4b	SP
BSX20	S3	Sm	BU326	S4b	SP	BUY89	S4b	SP
BSX45	S3	Sm	BU326A	S4b	SP	BUZ10	S9	PM
BSX46	S3	Sm	BU426	S4b	SP	BUZ10A	S9	PM
BSX47	S3	Sm	BU426A	S4b	SP	BUZ11	S9	PM
BSX59	S3	Sm	BU433	S4b	SP	BUZ11A	S9	PM
BSX60	S3	Sm	BU505	S4b	SP	BUZ14	S9	PM
BSX61	S3	Sm	BU508A	S4b	SP	BUZ15	S9	PM
BSY95A	S3	Sm	BU705	S4b	SP	BUZ20	S9	PM
BT136*	S2	Tri	BU806	S4b	SP	BUZ21	S9	PM
BT137*	S2	Tri	BU807	S4b	SP	BUZ23	S9	PM
BT138*	S2	Tri	BU824	S4b	SP	BUZ24	S9	PM
BT139*	S2	Tri	BU826	S4b	SP	BUZ25	S9	PM
BT149*	S2	Th	BUS11;A	S4b	SP	BUZ30	S9	PM
BT151*	S2	Th	BUS12;A	S4b	SP	BUZ31	S9	PM
BT152*	S2	Th	BUS13;A	S4b	SP	BUZ32	S9	PM
BT153	S2	Th	BUS14;A	S4b	SP	BUZ33	S9	PM
BT154	S2	Th	BUT11;A	S4b	SP	BUZ34	S9	PM
BT155*	S2	Th	BUV82	S4b	SP	BUZ35	S9	PM
BTV24*	S2	Th	BUV83	S4b	SP	BUZ36	S9	PM
BTV34*	S2	Tri	BUV89	S4b	SP	BUZ40	S9	PM
BTW58*	S2	Th	BUW11;A	S4b	SP	BUZ41A	S9	PM
BTW23*	S2	Th	BUW12;A	S4b	SP	BUZ42	S9	PM
BTW30S*	S2	Th	BUW13;A	S4b	SP	BUZ43	S9	PM
BTW31W*	S2	Th	BUW84	S4b	SP	BUZ44A	S9	PM
BTW38*	S2	Th	BUW85	S4b	SP	BUZ45	S9	PM
BTW40*	S2	Th	BUX46;A	S4b	SP	BUZ45A	S9	PM
BTW42*	S2	Th	BUX47;A	S4b	SP	BUZ45B	S9	PM
BTW43*	S2	Tri	BUX48;A	S4b	SP	BUZ45C	S9	PM
BTW45*	S2	Th	BUX80	S4b	SP	BUZ46	S9	PM
BTW47*	S2	Th	BUX81	S4b	SP	BUZ50A	S9	PM

\* = series

FET = Field-effect transistors  
Mm = Microminiature semiconductors  
for hybrid circuits

PM = Power MOS transistors

Sm = Small-signal transistors

SP = Low-frequency switching power transistors

Th = Thyristors

Tri = Triacs

type no.	book	section	type no.	book	section	type no.	book	section
BUZ50B	S9	PM	BY478	S1	R	BYX25*	S2	R
BUZ53A	S9	PM	BY505	S1	R	BYX30*	S2	R
BUZ54	S9	PM	BY509	S1	R	BYX32*	S2	R
BUZ54A	S9	PM	BY527	S1	R	BYX38*	S2	R
BUZ60	S9	PM	BY584	S1	R	BYX39*	S2	R
BUZ60B	S9	PM	BY609	S1	R	BYX42*	S2	R
BUZ63	S9	PM	BY610	S1	R	BYX45*	S2	R
BUZ63B	S9	PM	BYV20	S2	R	BYX46*	S2	R
BUZ64	S9	PM	BYV21*	S2	R	BYX49*	S2	R
BUZ71	S9	PM	BYV22	S2	R	BYX50*	S2	R
BUZ71A	S9	PM	BYV23	S2	R	BYX52*	S2	R
BUZ72	S9	PM	BYV24	S2	R	BYX56*	S2	R
BUZ72A	S9	PM	BYV27	S1	R	BYX71*	S2	R
BUZ73A	S9	PM	BYV28	S1	R	BYX90	S1	R
BUZ74	S9	PM	BYV30*	S2	R	BYX91*	S1	R
BUZ74A	S9	PM	BYV32*	S2	R	BYX94	S1	R
BUZ76	S9	PM	BYV92*	S2	R	BYX96*	S2	R
BUZ76A	S9	PM	BYV95A	S1	R	BYX97*	S2	R
BUZ80	S9	PM	BYV95B	S1	R	BYX98*	S2	R
BUZ80A	S9	PM	BYV95C	S1	R	BYX99*	S2	R
BUZ83	S9	PM	BYV96D	S1	R	BZT03	S1	Vrg
BUZ83A	S9	PM	BYV96E	S1	R	BZV10	S1	Vrf
BUZ84	S9	PM	BYW19*	S2	R	BZV11	S1	Vrf
BUZ84A	S9	PM	BYW25	S2	R	BZV12	S1	Vrf
BY184	S1	R	BYW29*	S2	R	BZV13	S1	Vrf
BY188G	S1	R	BYW30*	S2	R	BZV14	S1	Vrf
BY223	S2	R	BYW31*	S2	R	BZV15*	S2	Vrf
BY224*	S2	R	BYW54	S1	R	BZV37	S1	Vrf
BY225*	S2	R	BYW55	S1	R	BZV46	S1	Vrg
BY228	S1	R	BYW56	S1	R	BZV49*	S1/S7	Vrg
BY229*	S2	R	BYW92*	S2	R	BZV85	S1	Vrg
BY249	S2	R	BYW93*	S2	R	BZW70*	S2	TS
BY260*	S2	R	BYW94*	S2	R	BZW86*	S2	TS
BY261*	S2	R	BYW95A	S1	R	BZW91*	S2	TS
BY277*	S2	R	BYW95B	S1	R	BZX55	S1	Vrg
BY438	S1	R	BYW95C	S1	R	BZX70*	S2	Vrg
BY448	S1	R	BYW96D	S1	R	BZX75	S1	Vrg
BY458	S1	R	BYW96E	S1	R	BZX79*	S1	Vrg
BY476	S1	R	BYX10	S1	R	BZX84*	S7/S1	Mm/Vrg
BY477	S1	R	BYX22*	S2	R	BZX87*	S1	Vrg

\* = series

Mm = Microminiature semiconductors  
for hybrid circuits

PM = Power MOS transistors

R = Rectifier diodes

TS = Transient suppressor diodes

Vrf = Voltage reference diodes

Vrg = Voltage regulator diodes

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type no.	book	section	type no.	book	section	type no.	book	section
BZX90	S1	Vrf	CQL14B	S8	Ph	CQY11C	S8	LED
BZX91	S1	Vrf	CQN10	S8	LED	CQY24B(L)	S8	LED
BZX92	S1	Vrf	CQN11	S8	LED	CQY49B	S8	LED
BZX93	S1	Vrf	CQT10	S8	LED	CQY49C	S8	LED
BZX94	S1	Vrf	CQT11	S8	LED	CQY50	S8	LED
BZY91*	S2	Vrg	CQT12	S8	LED	CQY52	S8	LED
BZY93*	S2	Vrg	CQV60(L)	S8	LED	CQY54A	S8	LED
BZY95*	S2	Vrg	CQV60A(L)	S8	LED	CQY58A	S8	LED
BZY96*	S2	Vrg	CQV61A(L)	S8	LED	CQY89A	S8	LED
CNX21	S8	PhC	CQV62(L)	S8	LED	CQY94	S8	LED
CNX35	S8	PhC	CQV70(L)	S8	LED	CQY94B(L)	S8	LED
CNX36	S8	PhC	CQV70A(L)	S8	LED	CQY95B	S8	LED
CNX37	S8	PhC	CQV71A(L)	S8	LED	CQY96(L)	S8	LED
CNX38	S8	PhC	CQV72(L)	S8	LED	CQY97A	S8	LED
CNX44	S8	PhC	CQV80L	S8	LED	OA90	S1	GD
CNX48	S8	PhC	CQV80AL	S8	LED	OA91	S1	GD
CNX62	S8	PhC	CQV81L	S8	LED	OA95	S1	GD
CNY50	S8	PhC	CQV82L	S8	LED	OM320	S10	WBM
CNY52	S8	PhC	CQW10(L)	S8	LED	OM321	S10	WBM
CNY53	S8	PhC	CQW10A(L)	S8	LED	OM322	S10	WBM
CNY57	S8	PhC	CQW10B(L)	S8	LED	OM323	S10	WBM
CNY57A	S8	PhC	CQW11A(L)	S8	LED	OM323A	S10	WBM
CNY62	S8	PhC	CQW11B(L)	S8	LED	OM335	S10	WBM
CNY63	S8	PhC	CQW12(L)	S8	LED	OM336	S10	WBM
CQ209S	S8	D	CQW12B(L)	S8	LED	OM337	S10	WBM
CQ216X	S8	D	CQW20A	S8	LED	OM337A	S10	WBM
CQ216Y	S8	D	CQW21	S8	LED	OM339	S10	WBM
CQ327;R	S8	D	CQW22	S8	LED	OM345	S10	WBM
CQ330;R	S8	D	CQW24(L)	S8	LED	OM350	S10	WBM
CQ331;R	S8	D	CQW54	S8	LED	OM360	S10	WBM
CQ332;R	S8	D	CQX10	S8	LED	OM361	S10	WBM
CQ427;R	S8	D	CQX11	S8	LED	OM370	S10	WBM
CQ430;R	S8	D	CQX12	S8	LED	OM931	S4a	P
CQ431;R	S8	D	CQX24(L)	S8	LED	OM961	S4a	P
CQ432;R	S8	D	CQX51	S8	LED	OSB9110	S2	St
CQF24	S8	Ph	CQX54(L)	S8	LED	OSB9210	S2	St
CQL10A	S8	Ph	CQX64(L)	S8	LED	OSB9410	S2	St
CQL13	S8	Ph	CQX74(L)	S8	LED	OSM9110	S2	St
CQL13A	S8	Ph	CQX74Y	S8	LED	OSM9210	S2	St
CQL14A	S8	Ph	CQY11B	S8	LED	OSM9410	S2	St

\* = series

D = Displays

GD = Germanium diodes

LED = Light emitting diodes

P = Low-frequency power transistors

Ph = Photoconductive devices

PhC = Photocouplers

St = Rectifier stacks

Vrf = Voltage reference diodes

Vrg = Voltage regulator diodes

WBM = Wideband hybrid IC modules

type no.	book	section	type no.	book	section	type no.	book	section
OSM9510	S2	St	1N3880	S2	R	2N1711	S3	Sm
OSM9511	S2	St	1N3881	S2	R	2N1893	S3	Sm
OSM9512	S2	St	1N3882	S2	R	2N2218	S3	Sm
OSS9110	S2	St	1N3889	S2	R	2N2218A	S3	Sm
OSS9210	S2	St	1N3890	S2	R	2N2219	S3	Sm
OSS9410	S2	St	1N3891	S2	R	2N2219A	S3	Sm
PH2222;R	S3	Sm	1N3892	S2	R	2N2221	S3	Sm
PH2222A;RS3		Sm	1N3899	S2	R	2N2221A	S3	Sm
PH2369	S3	Sm	1N3900	S2	R	2N2222	S3	Sm
PH2907;R	S3	Sm	1N3901	S2	R	2N2222A	S3	Sm
PH2907A;RS3		Sm	1N3902	S2	R	2N2297	S3	Sm
PH2955T	S4a	P	1N3903	S2	R	2N2368	S3	Sm
PH3055T	S4a	P	1N3909	S2	R	2N2369	S3	Sm
PH40*	S2	R	1N3910	S2	R	2N2369A	S3	Sm
PH70*	S2	R	1N3911	S2	R	2N2483	S3	Sm
RPY58A	S8	Ph	1N3912	S2	R	2N2484	S3	Sm
RPY76B	S8	Ph	1N3913	S2	R	2N2904	S3	Sm
RPY86	S8	I	1N4001G	S1	R	2N2904A	S3	Sm
RPY87	S8	I	1N4002G	S1	R	2N2905	S3	Sm
RPY88	S8	I	1N4003G	S1	R	2N2905A	S3	Sm
RPY89	S8	I	1N4004G	S1	R	2N2906	S3	Sm
RPY90*	S8	I	1N4005G	S1	R	2N2906A	S3	Sm
RPY91*	S8	I	1N4006G	S1	R	2N2907	S3	Sm
RPY93	S8	I	1N4007G	S1	R	2N2907A	S3	Sm
RPY94	S8	I	1N4148	S1	SD	2N3019	S3	Sm
RPY95	S8	I	1N4150	S1	SD	2N3020	S3	Sm
RPY96	S8	I	1N4151	S1	SD	2N3053	S3	Sm
RPY97	S8	I	1N4154	S1	SD	2N3375	S6	RFP
RTC901	S8	LED	1N4446	S1	SD	2N3553	S6	RFP
RTC902	S8	LED	1N4448	S1	SD	2N3632	S6	RFP
RTC903	S8	LED	1N4531	S1	SD	2N3822	S5	FET
RTC904	S8	LED	1N4532	S1	SD	2N3823	S5	FET
1N821;A	S1	Vrf	1N5059	S1	R	2N3866	S6	RFP
1N823;A	S1	Vrf	1N5060	S1	R	2N3903	S3	Sm
1N825;A	S1	Vrf	1N5061	S1	R	2N3904	S3	Sm
1N827;A	S1	Vrf	1N5062	S1	R	2N3905	S3	Sm
1N829;A	S1	Vrf	2N918	S10	WBT	2N3906	S3	Sm
1N914	S1	SD	2N929	S3	Sm	2N3924	S6	RFP
1N916	S1	SD	2N930	S3	Sm	2N3926	S6	RFP
1N3879	S2	R	2N1613	S3	Sm	2N3927	S6	RFP

FET = Field-effect transistors

I = Infrared devices

LED = Light emitting diodes

P = Low-frequency power transistors

Ph = Photoconductive devices

R = Rectifier diodes

RFP = R.F. power transistors and modules

SD = Small-signal diodes

Sm = Small-signal transistors

St = Rectifier stacks

Vrf = Voltage reference diodes

WBT = Wideband hybrid IC transistors

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type no.	book	section	type no.	book	section	type no.	book	section
2N3966	S5	FET	375CQY/B	S8	Ph	56352	S4b	A
2N4030	S3	Sm	497CQF/A	S8	Ph	56353	S4b	A
2N4031	S3	Sm	498CQL	S8	Ph	56354	S4b	A
2N4032	S3	Sm	56201d	S4b	A	56359b	S4b	A
2N4033	S3	Sm	56201j	S4b	A	56359c	S4b	A
2N4091	S5	FET	56230	S2	HE	56359d	S4b	A
2N4092	S5	FET	56231	S2	HE	56360a	S4b	A
2N4093	S5	FET	56245	S3,6,10A		56363	S2,S4b	A
2N4123	S3	Sm	56246	S3,5,10A		56364	S2,S4b	A
2N4124	S3	Sm	56253	S2	DH	56366	S2	A
2N4125	S3	Sm	56256	S2	DH	56367	S2	A
2N4126	S3	Sm	56261a	S4b	A	56368a	S4b	A
2N4391	S5	FET	56262A	S2	A	56368b	S4b	A
2N4392	S5	FET	56264A	S2	A	56369	S2,S4b	A
2N4393	S5	FET	56268	S2	DH	56378	S4b	A
2N4427	S6	RFP	56290	S2	HE	56379	S4b	A
2N4856	S5	FET	56295	S2	A	56387a,b	S4b	A
2N4857	S5	FET	56312	S2	DH			
2N4858	S5	FET	56313	S2	DH			
2N4859	S5	FET	56316	S2	A			
2N4860	S5	FET	56317	S2	A			
2N4861	S5	FET	56326	S4b	A			
2N5415	S3	Sm	56339	S4b	A			
2N5416	S3	Sm	56348	S2	DH			
61SV	S8	I	56350	S2	DH			

A = Accessories  
 DH = Diecast heatsinks  
 FET = Field-effect transistors  
 HE = Heatsink extrusions

I = Infrared devices  
 Ph = Photoconductive devices  
 RFP = R.F. power transistors and modules  
 Sm = Small-signal transistors

SELECTION GUIDE



## SELECTION GUIDE

$V_{DS}$ max. V	case	$I_D$ max. A	$P_{tot}$ max. W	$R_{DS\ ON}$ < $\Omega$	$V_F$ typ. V	$g_{fs}$ typ. A/V	$t_f$ typ. ns	$C_{rs}$ typ. pF	type number
50	TO-220	12	75	0,1	1,4	4,8	60	120	BUZ10
		12	75	0,12	1,4	4,8	60	120	BUZ10A
		30	75	0,04	1,7	8,0	450	360	BUZ11
		25	75	0,06	1,6	8,0	450	360	BUZ11A
		12	40	0,1	1,6	4,8	150	160	BUZ71
		12	40	0,12	1,6	4,8	—	160	BUZ71A
50	TO-3	39	125	0,04	1,7	12,0	200	500	BUZ14
		45	125	0,03	1,8	12,0	200	500	BUZ15
100	TO-220	12	75	0,2	1,4	4,0	60	80	BUZ20
		18	75	0,1	1,6	3,5	60	200	BUZ21
		10	40	0,2	1,55	3,8	150	80	BUZ72
		9	40	0,25	1,55	3,8	150	80	BUZ72A
100	TO-3	10	78	0,2	1,3	4,0	60	80	BUZ23
		32	125	0,06	1,5	10,0	200	500	BUZ24
		19	78	0,1	1,5	8,0	450	360	BUZ25
200	TO-220	7	75	0,75	1,15	3,5	60	100	BUZ30
		12,5	75	0,2	1,4	5,0	60	140	BUZ31
		9,5	75	0,4	1,3	3,5	60	100	BUZ32
		5,8	40	0,6	1,4	3,5	130	60	BUZ73A
200	TO-3	7,2	78	0,75	1,15	3,5	60	100	BUZ33
		17	125	0,2	1,15	7,5	200	500	BUZ34
		9,9	78	0,4	1,3	3,5	60	100	BUZ35
		22	125	0,12	1,2	7,5	200	500	BUZ36
400	TO-220	5,5	75	1,0	1,15	2,5	100	30	BUZ60
		4,5	75	1,5	1,15	2,5	100	30	BUZ60B
		3,0	40	1,8	1,1	2,5	100	25	BUZ76
		2,6	40	2,5	1,1	2,5	100	25	BUZ76A
400	TO-3	5,9	78	1,0	1,2	2,5	100	30	BUZ63
		4,5	78	1,5	1,15	2,5	100	30	BUZ63B
		10,5	125	0,4	1,3	4,5	100	100	BUZ64
450	TO-3	10	125	0,5	1,3	4,0	100	100	BUZ45C

# SELECTION GUIDE

$V_{DS}$ max. V	case	$I_D$ max. A	$P_{tot}$ max. W	$R_{DS\ ON}$ < $\Omega$	$V_F$ typ. V	$g_{fs}$ typ. A/V	$t_f$ typ. ns	$C_{rs}$ typ. pF	type number
500	TO-220	2,5	75	4,5	1,0	2,5	100	30	BUZ40
		4,5	75	1,5	1,1	2,5	100	30	BUZ41A
		4,0	75	2,0	1,1	2,5	100	30	BUZ42
		2,4	40	3,0	1,0	2,5	100	20	BUZ74
		2,0	40	3,0	1,0	2,5	100	20	BUZ74A
500	TO-3	2,8	78	4,5	1,05	2,5	100	30	BUZ43
		4,8	78	1,5	1,15	2,5	100	30	BUZ44A
		9,6	125	0,6	1,3	4,0	100	100	BUZ45
		8,3	125	0,8	1,3	4,0	100	100	BUZ45A
		10	125	0,5	1,3	4,0	100	100	BUZ45B
4,2	78	2,0	1,1	2,5	100	30	BUZ46		
800	TO-220	2,6	75	4,0	1,05	1,8	100	30	BUZ80
		3,0	75	3,0	1,05	1,8	100	30	BUZ80A
800	TO-3	2,9	78	4,0	1,05	1,8	100	30	BUZ83
		3,4	78	3,0	1,1	1,8	100	30	BUZ83A
		5,3	125	2,0	1,0	3,0	100	100	BUZ84
		6,0	125	1,5	1,1	3,0	100	100	BUZ84A
1000	TO-220	2,5	75	5,0	1,05	1,5	100	30	BUZ50A
		2,0	75	8,0	1,05	1,5	100	30	BUZ50B
1000	TO-3	2,6	78	5,0	1,05	1,5	100	30	BUZ53A
		5,3	125	2,0	1,15	2,0	100	100	BUZ54
		4,6	125	2,6	1,15	2,0	100	100	BUZ54A



SELECTION GUIDE

CLIP MOUNTING

envelope	direct mounting		insulated mounting		
	clip		mica	alumina	clip
TO-220 (SOT-78)	56363		56369 or	56367	56364

SCREW MOUNTING

envelope	direct mounting		insulated mounting			
	metal washer	mounting material	mica washer	insul. bush	metal washer	mounting material
TO-220 (SOT-78) up to 800 V up to 1000 V	56360a	M3	56359b 56359b	56359c 56359d	56360a 56360a	M3 M3
TO-3 (SOT-3) up to 500 V  up to 2000 V	—	M4	56201d 56339	56201j or 56261a 56352		M3 M3

The accessories mentioned can be supplied on request.  
See also chapter Mounting Instructions.

GENERAL

Type designation  
Rating systems  
Transistor ratings  
Letter symbols  
s-parameters  
Explanatory notes





PRO ELECTRON TYPE DESIGNATION CODE  
FOR SEMICONDUCTOR DEVICES

This type designation code applies to discrete semiconductor devices – as opposed to integrated circuits –, multiples of such devices and semiconductor chips.

A basic type number consists of:

*TWO LETTERS FOLLOWED BY A SERIAL NUMBER*

**FIRST LETTER**

The first letter gives information about the material used for the active part of the devices.

- A. GERMANIUM or other material with band gap of 0,6 to 1,0 eV.
- B. SILICON or other material with band gap of 1,0 to 1,3 eV.
- C. GALLIUM-ARSENIDE or other material with band gap of 1,3 eV or more.
- R. COMPOUND MATERIALS (e.g. Cadmium-Sulphide).

**SECOND LETTER**

The second letter indicates the function for which the device is primarily designed.

- A. DIODE; signal, low power
- B. DIODE; variable capacitance
- C. TRANSISTOR; low power, audio frequency ( $R_{th\ j-mb} > 15\ ^\circ C/W$ )
- D. TRANSISTOR; power, audio frequency ( $R_{th\ j-mb} \leq 15\ ^\circ C/W$ )
- E. DIODE; tunnel
- F. TRANSISTOR; low power, high frequency ( $R_{th\ j-mb} > 15\ ^\circ C/W$ )
- G. MULTIPLE OF DISSIMILAR DEVICES – MISCELLANEOUS; e.g. oscillator
- H. DIODE; magnetic sensitive
- L. TRANSISTOR; power, high frequency ( $R_{th\ j-mb} \leq 15\ ^\circ C/W$ )
- N. PHOTO-COUPLER
- P. RADIATION DETECTOR; e.g. high sensitivity phototransistor
- Q. RADIATION GENERATOR; e.g. light-emitting diode (LED)
- R. CONTROL AND SWITCHING DEVICE; e.g. thyristor, low power ( $R_{th\ j-mb} > 15\ ^\circ C/W$ )
- S. TRANSISTOR; low power, switching ( $R_{th\ j-mb} > 15\ ^\circ C/W$ )
- T. CONTROL AND SWITCHING DEVICE; e.g. thyristor, power ( $R_{th\ j-mb} \leq 15\ ^\circ C/W$ )
- U. TRANSISTOR; power, switching ( $R_{th\ j-mb} \leq 15\ ^\circ C/W$ )
- X. DIODE: multiplier, e.g. varactor, step recovery
- Y. DIODE; rectifying, booster
- Z. DIODE; voltage reference or regulator (transient suppressor diode, with third letter W)

# TYPE DESIGNATION

## SERIAL NUMBER

Three figures, running from 100 to 999, for devices primarily intended for consumer equipment.\* One letter (Z, Y, X, etc.) and two figures, running from 10 to 99, for devices primarily intended for industrial/professional equipment.\*

This letter has no fixed meaning except W, which is used for transient suppressor diodes.

## VERSION LETTER

It indicates a minor variant of the basic type either electrically or mechanically. The letter never has a fixed meaning, except letter R, indicating reverse voltage, e.g. collector to case or anode to stud.

## SUFFIX

Sub-classification can be used for devices supplied in a wide range of variants called associated types. Following sub-coding suffixes are in use:

### 1. VOLTAGE REFERENCE and VOLTAGE REGULATOR DIODES: *ONE LETTER and ONE NUMBER*

The LETTER indicates the nominal tolerance of the Zener (regulation, working or reference) voltage

- A. 1% (according to IEC 63: series E96)
- B. 2% (according to IEC 63: series E48)
- C. 5% (according to IEC 63: series E24)
- D. 10% (according to IEC 63: series E12)
- E. 20% (according to IEC 63: series E6)

The number denotes the typical operating (Zener) voltage related to the nominal current rating for the whole range.

The letter 'V' is used instead of the decimal point.

### 2. TRANSIENT SUPPRESSOR DIODES: *ONE NUMBER*

The NUMBER indicates the maximum recommended continuous reversed (stand-off) voltage  $V_R$ . The letter 'V' is used as above.

### 3. CONVENTIONAL and CONTROLLED AVALANCHE RECTIFIER DIODES and THYRISTORS: *ONE NUMBER*

The NUMBER indicates the rated maximum repetitive peak reverse voltage ( $V_{RRM}$ ) or the rated repetitive peak off-state voltage ( $V_{DRM}$ ), whichever is the lower. Reversed polarity is indicated by letter R, immediately after the number.

### 4. RADIATION DETECTORS: *ONE NUMBER*, preceded by a hyphen (-)

The NUMBER indicates the depletion layer in  $\mu\text{m}$ . The resolution is indicated by a version LETTER.

### 5. ARRAY OF RADIATION DETECTORS and GENERATORS: *ONE NUMBER*, preceded by a stroke (/).

The NUMBER indicates how many basic devices are assembled into the array.

\* When these serial numbers are exhausted the serial number for consumer types may be extended to four figures, and that for industrial types to three figures.

## RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

### DEFINITIONS OF TERMS USED

*Electronic device.* An electronic tube or valve, transistor or other semiconductor device.

Note

This definition excludes inductors, capacitors, resistors and similar components.

*Characteristic.* A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

*Bogey electronic device.* An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

*Rating.* A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note

Limiting conditions may be either maxima or minima.

*Rating system.* The set of principles upon which ratings are established and which determine their interpretation.

Note

The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

### ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

### DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

### DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

## TRANSISTOR RATINGS

The ratings are presented as voltage, current, power and temperature ratings. The list of these ratings and their definitions is given as follows:

### Transistor voltage ratings

#### Collector to base voltage ratings

$V_{CBmax}$  The maximum permissible instantaneous voltage between collector and base terminals. The collector voltage is negative with respect to base in PNP transistors and positive with respect to base in NPN types.

$V_{CBmax} (I_E = 0)$  The maximum permissible instantaneous voltage between collector and base terminals, when the emitter terminal is open circuited.

#### Emitter to base voltage ratings

$V_{EBmax}$  The maximum permissible instantaneous reverse voltage between emitter and base terminal. The emitter voltage is negative with respect to base for PNP transistor and positive with respect to base for NPN types.

$V_{EBmax} (I_C = 0)$  The maximum permissible instantaneous reverse voltage between emitter and base terminals when the collector terminal is open circuited.

#### Collector to emitter voltage ratings

$V_{CEmax}$  The maximum permissible instantaneous voltage between collector and emitter terminals. The collector voltage is negative with respect to emitter in PNP transistors and positive with respect to emitter in NPN types. This rating is very dependent on circuit conditions and collector current and it is necessary to refer to the curve of  $V_{CE}$  versus  $I_C$  for the appropriate circuit condition in order to obtain the correct rating.

$V_{CEmax} (Cut-off)$  The maximum permissible instantaneous voltage between collector and emitter terminals when the emitter current is reduced to zero by means of a reverse emitter base voltage, i.e. the base voltage is normally positive with respect to emitter for PNP transistor and negative with respect to emitter for NPN types.

NOTE: The term "cut-off" is sometimes replaced by  $V_{BE} > x$  volts, or  $\frac{R_B}{R_E} \leq y$  which are equivalent conditions under which the device may be cut-off.

$V_{CEmax} (I_C = x \text{ mA})$  The maximum permissible instantaneous voltage between collector and emitter terminals when the collector current is at a high value, often the max. rated value.

$V_{CEmax} (I_B = 0)$  The maximum permissible instantaneous voltage between collector and emitter terminals when the base terminal is open circuited or when a very high resistance is in series with the base terminal. Special care must be taken to ensure that thermal runaway due to excessive collector leakage current does not occur in this condition.

Due to the current dependency of  $V_{CE}$  it is usual to present this information as a voltage rating chart which is a curve of collector current versus collector to emitter voltage (see Fig. 1).



# TRANSISTOR RATINGS

This curve is divided into two areas:

A permissible area of operation under all conditions of base drive provided the dissipation rating is not exceeded (area 1) and an area where operation is allowable under certain specified conditions (area 2). To assist in determining the rating in this second area, further curves are provided relating the voltage rating to external circuit conditions, for example:

$$\frac{R_B}{R_E}, R_B, Z_{Bg}, V_{BE}, I_B \text{ or } \frac{V_{BB}}{R_B}.$$

An example of this type of curve is given in Fig. 2 as  $V_{CE}$  versus  $\frac{R_B}{R_E}$  for two different values of collector current.

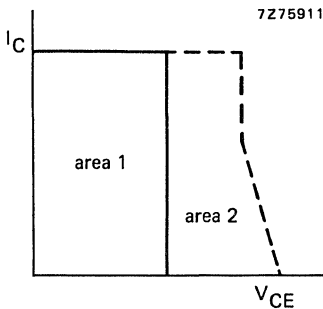


Fig. 1.

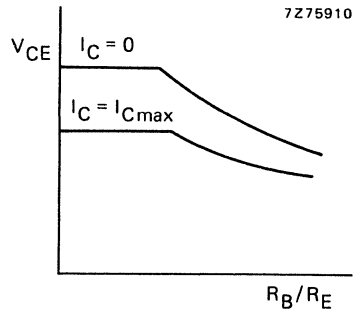


Fig. 2.

It should be noted that when  $R_E$  is shunted by a capacitor, the collector voltage  $V_{CE}$  during switching must be restricted to a value which does not rely on the effect of  $R_E$ .

In the case of an inductive load and when an energy rating is given, it may be permissible to operate outside the rated area provided the specified energy rating is not exceeded.

## Transistor current ratings

### Collector current ratings

$I_{Cmax}$  The maximum permissible collector current. Without further qualification, the d.c. value is implied.

$I_{C(AV)max}$  The maximum permissible average value of the total collector current

$I_{CM}$  The maximum permissible instantaneous value of the total collector current.

### Emitter current ratings

$I_{Emax}$  The maximum permissible emitter current. Without further qualification, the d.c. value is implied.

$I_{E(AV)max}$  The maximum permissible average value of the total emitter current.

$I_{ER(AV)max}$  The maximum permissible average value of the total emitter current when operating in the reverse emitter-base breakdown region.

$I_{EM}$  The maximum permissible instantaneous value of the total emitter current.

$I_{ERM}$  The maximum permissible instantaneous value of the total reverse emitter current allowable in the reverse breakdown region.

## Base current ratings

$I_{Bmax}$	The maximum permissible base current. Without further qualification, the d.c. value is implied.
$I_{B(AV)max}$	The maximum permissible average value of the total base current.
$I_{BR(AV)max}$	The maximum permissible average value of the total reverse base current allowable in the reverse breakdown region.
$I_{BM}$	The maximum permissible instantaneous value of the total base current. The rating also includes the switch off current.
$I_{BRM}$	The maximum permissible instantaneous value of the total reverse current allowable in the reverse breakdown region.

## Transistor power ratings

$P_{tot\ max}$ : The total maximum permissible continuous power dissipation in the transistor and includes both the collector-base dissipation and the emitter-base dissipation. Under steady state conditions the total power is given by the expression:

$$P_{tot} = V_{CE} \times I_C + V_{BE} \times I_B.$$

In order to distinguish between "steady state" and "pulse" conditions the terms "steady state power ( $P_S$ )" and "pulse power ( $P_P$ )" are often used. The permissible total power dissipation is dependent upon temperature and its relationship is shown by means of a chart as shown in Fig. 3.

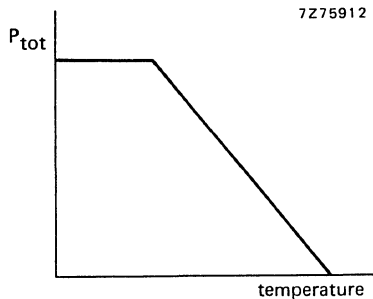


Fig. 3.

The temperature may be ambient, case or mounting base temperatures. Where a cooling clip or a heatsink is attached to the device, the allowable power dissipation is also dependent on the efficiency of the heatsink.

The efficiency of this clip or heatsink is measured in terms of its thermal resistance ( $R_{th\ h}$ ) normally expressed in degrees kelvin per watt (K/W). For a mounting base rated device, the added effect of the contact resistance ( $R_{th\ i}$ ) must be taken into account.

The effect of heatsinks of various thermal resistance and contact resistance is often included in the above chart.

# TRANSISTOR RATINGS

Thus for any heatsink of known thermal resistance and any given ambient temperature, the maximum permissible power dissipation can be established. Alternatively, knowing the power dissipation which will occur and the ambient temperature, the necessary heatsink thermal resistance can be calculated.

A general expression from which the total permissible steady state power dissipation can be calculated is:

$$P_{\text{tot}} = \frac{T_j - T_{\text{amb}}}{R_{\text{th } j-a}}$$

where  $R_{\text{th } j-a}$  is the thermal resistance from the transistor junction to the ambient. For case rated or mounting base rated devices, the thermal resistance  $R_{\text{th } j-a}$  is made up of the thermal resistance junction to case or mounting base ( $R_{\text{th } j-mb}$ ), the contact thermal resistance ( $R_{\text{th } i}$ ) and the heatsink thermal resistance  $R_{\text{th } h}$ .

For the calculation of pulse power operation  $P_p$ , the maximum pulse power is obtained by the aid of a chart as shown in Fig. 4.

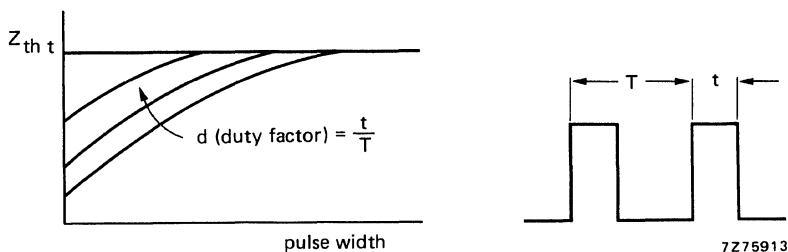


Fig. 4.

The general expression from which the maximum pulse power dissipation can be calculated is:

$$P_p = \frac{T_j - T_{\text{amb}} - P_s \times R_{\text{th } j-a}}{Z_{\text{th } t} + d (R_{\text{th } c-a})}$$

where  $Z_{\text{th } t}$  and  $d$  are given in the above chart and  $R_{\text{th } c-a}$  is the thermal resistance between case and ambient for case rated device. For mounting base rated device, it is equal to  $R_{\text{th } h} + R_{\text{th } i}$  and is zero for free air rated device because the effect of the temperature rise of the case over the ambient for a pulse train is already included in  $Z_{\text{th } t}$ .

## Temperature ratings

$T_{j\text{max}}$	The maximum permissible junction temperature which is used as the basis for the calculation of power ratings. Unless otherwise stated, the continuous value is implied.
$T_{j\text{max}}$ (continuous operation)	The maximum permissible continuous value.
$T_{j\text{max}}$ (intermittent operation)	The maximum permissible instantaneous junction temperature usually allowed for a total duration of 200 hours.
$T_{\text{mb}}$	The temperature of the surface making contact with a heatsink. This is confined to devices where a flange or stud for fixing onto a heatsink forms an integral part of the envelope.
$T_{\text{case}}$	The temperature of the envelope. This is confined to devices to which may be attached a clip-on cooling fin.

# LETTER SYMBOLS FOR TRANSISTORS AND SIGNAL DIODES

based on IEC Publication 148

## LETTER SYMBOLS FOR CURRENTS, VOLTAGES AND POWERS

### Basic letters

The basic letters to be used are:

I, i = current  
V, v = voltage  
P, p = power.

Lower-case basic letters shall be used for the representation of instantaneous values which vary with time.

In all other instances upper-case basic letters shall be used.

### Subscripts

A, a	Anode terminal
(AV), (av)	Average value
B, b	Base terminal, for MOS devices: Substrate
(BR)	Breakdown
C, c	Collector terminal
D, d	Drain terminal
E, e	Emitter terminal
F, f	Forward
G, g	Gate terminal
K, k	Cathode terminal
M, m	Peak value
O, o	As third subscript: The terminal not mentioned is open circuited
R, r	As first subscript: Reverse. As second subscript: Repetitive. As third subscript: With a specified resistance between the terminal not mentioned and the reference terminal.
(RMS), (rms)	R. M. S. value
S, s	{ As first or second subscript: Source terminal (for FETS only) As second subscript: Non-repetitive (not for FETS) As third subscript: Short circuit between the terminal not mentioned and the reference terminal
X, x	Specified circuit
Z, z	Replaces R to indicate the actual working voltage, current or power of voltage reference and voltage regulator diodes.

Note: No additional subscript is used for d. c. values.

Upper-case subscripts shall be used for the indication of:

- a) continuous (d. c.) values (without signal)  
Example  $I_B$
- b) instantaneous total values  
Example  $i_B$
- c) average total values  
Example  $I_{B(AV)}$
- d) peak total values  
Example  $I_{BM}$
- e) root-mean-square total values  
Example  $I_{B(RMS)}$

Lower-case subscripts shall be used for the indication of values applying to the varying component alone :

- a) instantaneous values  
Example  $i_b$
- b) root-mean-square values  
Example  $I_{b(rms)}$
- c) peak values  
Example  $I_{bm}$
- d) average values  
Example  $I_{b(av)}$

Note: If more than one subscript is used, subscript for which both styles exist shall either be all upper-case or all lower-case.

#### **Additional rules for subscripts**

##### Subscripts for currents

Transistors: If it is necessary to indicate the terminal carrying the current, this should be done by the first subscript (conventional current flow from the external circuit into the terminal is positive).

Examples:  $I_B$ ,  $i_B$ ,  $i_b$ ,  $I_{BM}$

Diodes: To indicate a forward current (conventional current flow into the anode terminal) the subscript F or f should be used; for a reverse current (conventional current flow out of the anode terminal) the subscript R or r should be used.

Examples:  $I_F$ ,  $I_R$ ,  $i_F$ ,  $I_{f(rms)}$

Subscripts for voltages

**Transistors:** If it is necessary to indicate the points between which a voltage is measured, this should be done by the first two subscripts. The first subscript indicates the terminal at which the voltage is measured and the second the reference terminal or the circuit node. Where there is no possibility of confusion, the second subscript may be omitted.

Examples:  $V_{BE}$ ,  $v_{BE}$ ,  $v_{be}$ ,  $V_{bem}$

**Diodes:** To indicate a forward voltage (anode positive with respect to cathode), the subscript F or f should be used; for a reverse voltage (anode negative with respect to cathode) the subscript R or r should be used.

Examples:  $V_F$ ,  $V_R$ ,  $v_F$ ,  $V_{rm}$

Subscripts for supply voltages or supply currents

Supply voltages or supply currents shall be indicated by repeating the appropriate terminal subscript.

Examples:  $V_{CC}$ ,  $I_{EE}$

**Note:** If it is necessary to indicate a reference terminal, this should be done by a third subscript

Example:  $V_{CCE}$

Subscripts for devices having more than one terminal of the same kind

If a device has more than one terminal of the same kind, the subscript is formed by the appropriate letter for the terminal followed by a number; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples:  $I_{B2}$  = continuous (d.c.) current flowing into the second base terminal

$V_{B2-E}$  = continuous (d.c.) voltage between the terminals of second base and emitter

Subscripts for multiple devices

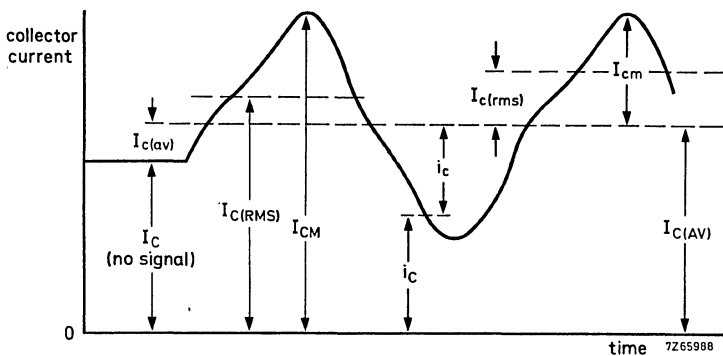
For multiple unit devices, the subscripts are modified by a number preceding the letter subscript; in the case of multiple subscripts, hyphens may be necessary to avoid misunderstanding.

Examples:  $I_{2C}$  = continuous (d.c.) current flowing into the collector terminal of the second unit

$V_{IC-2C}$  = continuous (d.c.) voltage between the collector terminals of the first and the second unit.

## Application of the rules

The figure below represents a transistor collector current as a function of time. It consists of a continuous (d.c.) current and a varying component.



## LETTER SYMBOLS FOR ELECTRICAL PARAMETERS

## Definition

For the purpose of this Publication, the term "electrical parameter" applies to four-pole matrix parameters, elements of electrical equivalent circuits, electrical impedances and admittances, inductances and capacitances.

## Basic letters

The following is a list of the most important basic letters used for electrical parameters of semiconductor devices.

B, b = susceptance; imaginary part of an admittance

C = capacitance

G, g = conductance; real part of an admittance

H, h = hybrid parameter

L = inductance

R, r = resistance; real part of an impedance

X, x = reactance; imaginary part of an impedance

Y, y = admittance;

Z, z = impedance;

Upper-case letters shall be used for the representation of:

- a) electrical parameters of external circuits and of circuits in which the device forms only a part;
- b) all inductances and capacitances.

Lower-case letters shall be used for the representation of electrical parameters inherent in the device (with the exception of inductances and capacitances).

## Subscripts

### General subscripts

The following is a list of the most important general subscripts used for electrical parameters of semiconductor devices:

F, f	= forward; forward transfer
I, i (or 1)	= input
L, l	= load
O, o (or 2)	= output
R, r	= reverse; reverse transfer
S, s	= source

Examples:  $Z_S$ ,  $h_I$ ,  $h_F$

The upper-case variant of a subscript shall be used for the designation of static (d.c.) values.

Examples :  $h_{FE}$  = static value of forward current transfer ratio in common-emitter configuration (d.c. current gain)

$R_E$  = d.c. value of the external emitter resistance.

Note: The static value is the slope of the line from the origin to the operating point on the appropriate characteristic curve, i.e. the quotient of the appropriate electrical quantities at the operating point.

The lower-case variant of a subscript shall be used for the designation of small-signal values.

Examples:  $h_{fe}$  = small-signal value of the short-circuit forward current transfer ratio in common-emitter configuration

$Z_e = R_e + jX_e$  = small-signal value of the external impedance

Note: If more than one subscript is used, subscripts for which both styles exist shall either be all upper-case or all lower-case

Examples:  $h_{FE}$ ,  $y_{RE}$ ,  $h_{fe}$



Subscripts for four-pole matrix parameters

The first letter subscript (or double numeric subscript) indicates input, output, forward transfer or reverse transfer

Examples:  $h_i$  (or  $h_{11}$ )  
 $h_o$  (or  $h_{22}$ )  
 $h_f$  (or  $h_{21}$ )  
 $h_r$  (or  $h_{12}$ )

A further subscript is used for the identification of the circuit configuration. When no confusion is possible, this further subscript may be omitted.

Examples:  $h_{fe}$  (or  $h_{21e}$ ),  $h_{FE}$  (or  $h_{21E}$ )

**Distinction between real and imaginary parts**

If it is necessary to distinguish between real and imaginary parts of electrical parameters, no additional subscripts should be used. If basic symbols for the real and imaginary parts exist, these may be used.

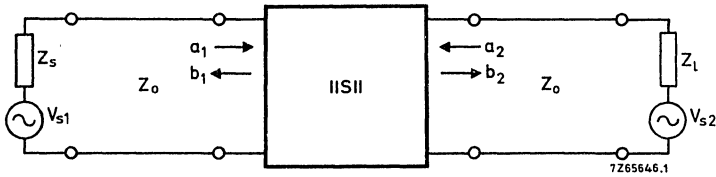
Examples:  $Z_i = R_i + jX_i$   
 $y_{fe} = g_{fe} + jb_{fe}$

If such symbols do not exist or if they are not suitable, the following notation shall be used:

Examples:  $\text{Re}(h_{ib})$  etc. for the real part of  $h_{ib}$   
 $\text{Im}(h_{ib})$  etc. for the imaginary part of  $h_{ib}$

## SCATTERING PARAMETERS

In distinction to the conventional h, y and z-parameters, s-parameters relate to traveling wave conditions. The figure below shows a two-port network with the incident and reflected waves  $a_1$ ,  $b_1$ ,  $a_2$  and  $b_2$ .



$$a_1 = \frac{V_{i1}}{\sqrt{Z_0}}$$

$$a_2 = \frac{V_{i2}}{\sqrt{Z_0}}$$

$$b_1 = \frac{V_{r1}}{\sqrt{Z_0}}$$

$$b_2 = \frac{V_{r2}}{\sqrt{Z_0}}$$

1)

$Z_0$  = characteristic impedance of the transmission line in which the two-port is connected.

$V_i$  = incident voltage

$V_r$  = reflected (generated) voltage

The four-pole equations for s-parameters are:

$$b_1 = s_{11}a_1 + s_{12}a_2$$

$$b_2 = s_{21}a_1 + s_{22}a_2$$

Using the subscripts i for 11, r for 12, f for 21 and o for 22, it follows that:

$$s_i = s_{11} = \left. \frac{b_1}{a_1} \right|_{a_2 = 0}$$

$$s_r = s_{12} = \left. \frac{b_1}{a_2} \right|_{a_1 = 0}$$

$$s_f = s_{21} = \left. \frac{b_2}{a_1} \right|_{a_2 = 0}$$

$$s_o = s_{22} = \left. \frac{b_2}{a_2} \right|_{a_1 = 0}$$

1) The squares of these quantities have the dimension of power.

## S-PARAMETERS

The s-parameters can be named and expressed as follows:

$s_i = s_{11}$  = Input reflection coefficient.

The complex ratio of the reflected wave and the incident wave at the input, under the conditions  $Z_1 = Z_0$  and  $V_{s2} = 0$ .

$s_r = s_{12}$  = Reverse transmission coefficient.

The complex ratio of the generated wave at the input and the incident wave at the output, under the conditions  $Z_s = Z_0$  and  $V_{s1} = 0$ .

$s_f = s_{21}$  = Forward transmission coefficient.

The complex ratio of the generated wave at the output and the incident wave at the input, under the conditions  $Z_1 = Z_0$  and  $V_{s2} = 0$ .

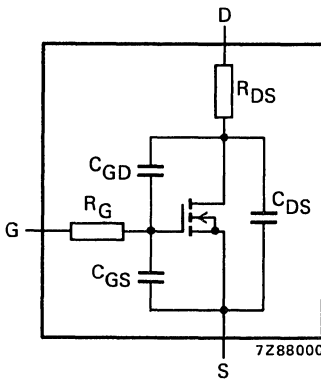
$s_o = s_{22}$  = Output reflection coefficient.

The complex ratio of the reflected wave and the incident wave at the output, under the conditions  $Z_s = Z_0$  and  $V_{s1} = 0$ .

## N-CHANNEL ENHANCEMENT POWER MOS TRANSISTORS

This new range of power MOS transistors offers:

- very low on-state resistance ( $< 0,1 \Omega$ , 50 V type)
- drain-source voltages up to 1000 V
- drain currents up to 14 A (continuous)
- microcomputer and TTL compatibility.



$C_{DS}$  is the drain-source capacitance  
 $C_{GS}$  is the gate-source capacitance  
 $C_{GD}$  is the gate-drain capacitance  
 $R_{DS}$  is the drain-source resistance  
 $R_G$  is the gate resistance.

Fig. 1 Equivalent circuit of a power MOS transistor.

$C_{GD}$  and  $C_{DS}$  depend on the drain-source voltage,  $C_{GS}$  does not.

If  $R_G$  and  $R_{DS}$  are neglected, the values stated in the data sheets for  $C_{is}$  (input capacitance)  $C_{os}$  (output capacitance) and  $C_{rs}$  (feedback capacitance) are related to the equivalent circuit capacitances by:

$$C_{is} = C_{GS} + C_{GD}$$

$$C_{os} = C_{DS} + C_{GD}$$

$$C_{rs} = C_{GD}$$

### PRECAUTIONS

The gate input of a power MOS transistor can easily be electrostatically charged to a high voltage. Ensure that the gate-source voltage never exceeds the maximum value stated in the data sheet, otherwise the transistor will be destroyed. When soldering by hand, use earthed soldering irons.

### MAXIMUM RATINGS

The ratings in the data sheets are absolute maximum ratings according to IEC 134. If any one of these ratings is exceeded the component may be destroyed.

# EXPLANATORY NOTES

## LETTER SYMBOLS

### Basic letters

$I, i$  = current

$V, v$  = voltage

$P, p$  = power

Lower-case letters indicate instantaneous values that vary with time. Otherwise, upper case letters are used.

### Subscripts for voltages

In general, two subscripts are used indicating the points between which a voltage is measured. The first subscript indicates the terminal at which the voltage is measured and the second the reference terminal or the circuit node.

### Subscripts for supply voltages

Supply voltages are indicated by repeating the appropriate terminal subscript, e.g.  $V_{DD}$ .

### Subscripts for currents

At least one subscript is used indicating the terminal carrying the current. Positive current is defined as conventional current flow into a terminal. Negative current is defined as conventional current flow out of a terminal.

## CHARACTERISTICS

The data given under Characteristics are mean values. In many cases, data are supplemented by a range statement.

### Drain-source voltage $V_{DS}$

Maximum permissible value of the voltage between drain and source.

### Drain-gate voltage $V_{DGR}$

Maximum permissible value of the voltage between drain and gate, when bridging gate-source with a predefined resistance.

### Continuous drain current $I_D$

Maximum permissible value of the direct current at the drain connection.

### Pulsed drain current $I_{D\text{ puls}}$

Maximum permissible peak value of the drain current during pulse operation as specified in the diagram "safe operating area" for a respective pulse width and duty cycle.

### Gate-source voltage $V_{GS}$

Maximum permissible value of the voltage between gate and source.

### Maximum power dissipation $P_D$

Maximum permissible power dissipation of the transistor.

### Operating temperature range $T_j$

The range of the permissible chip temperature, with which the transistor may be operated continuously.

### Storage temperature range $T_{stg}$

The temperature range within which the transistor may be stored or transported without electrical load.

**Soldering temperature**  $T_{\text{slid}}$ 

The maximum permissible temperature during soldering at the terminals of the component, at a specified distance to the case and for a specified time.

**Thermal resistance**  $R_{\text{th } j-c}$ 

Thermal resistance between chip and case at thermal equilibrium.

**Thermal resistance**  $R_{\text{th } j-a}$ 

Thermal resistance between chip and ambient air at thermal equilibrium.

**Thermal resistance**  $R_{\text{th } j-sr}$ 

Thermal resistance between chip and substrate metallization rear side at thermal equilibrium.

**Drain-source breakdown voltage**  $V_{(\text{BR})\text{DSS}}$ 

The voltage between the drain and source measured at a specified drain current and with the gate and source short-circuited.

**Gate threshold voltage**  $V_{\text{GST}}$ 

The gate source voltage measured at a specified drain current and drain-source voltage.

**Zero gate voltage drain current**  $I_{\text{DSS}}$ 

The drain current at a specified drain-source voltage and with the gate and source short-circuited.

**Gate-source leakage current**  $I_{\text{GSS}}$ 

The gate leakage current at a specified gate-source voltage and with the drain and source short-circuited.

**Drain-source on-state resistance**  $R_{\text{DS ON}}$ 

The resistance between the drain and source at specified values of gate-source voltage and drain current.

**Forward transfer conductance**  $g_{\text{fs}}$ 

Ratio of the change of the drain current to the change in gate-source voltage producing it for a specified drain-source voltage.

**Input capacitance**  $C_{\text{is}}$ 

The capacitance between gate and source with the drain and source short-circuited for alternating voltages.

**Output capacitance**  $C_{\text{Os}}$ 

The capacitance between drain and source with the gate and source short-circuited for alternating voltages.

**Feedback capacitance**  $C_{\text{rS}}$ 

The capacitance between drain and gate with the source connected to the protective screen of the measuring bridge. Stated at particular gate-source and drain-source voltages and measuring frequency.

**Turn-on time**  $t_{\text{on}}$ 

$$t_{\text{on}} = t_{\text{d on}} + t_{\text{r}}$$

where:

$t_{\text{d on}}$  is the turn-on delay time measured between the 10% value of the gate-source voltage and the 90% value of the drain-source voltage, and  $t_{\text{r}}$  is the rise time measured between the 90% and 10% value of the drain-source voltage.

**Turn-off time**  $t_{\text{off}}$ 

$$t_{\text{off}} = t_{\text{d off}} + t_{\text{f}}$$

where:

$t_{\text{d off}}$  is the turn-off delay time measured between the 90% value of the gate-source voltage and the 10% value of the drain-source voltage, and  $t_{\text{f}}$  is the fall time measured between 10% and 90% values of the drain-source voltage.

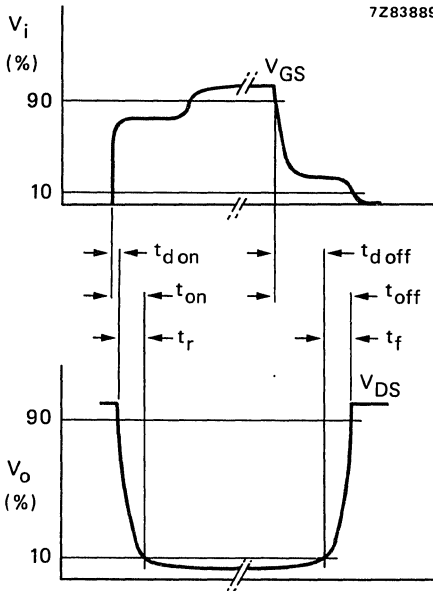


Fig. 2 Definition of switching times.

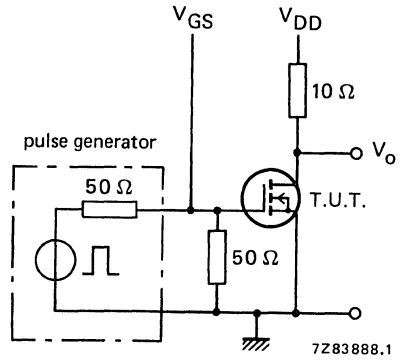


Fig. 3 Measuring circuit.

### MEASURING CIRCUITS

Parameters should be measured at the temperatures stated in the data sheets.

Drain current  $I_D$

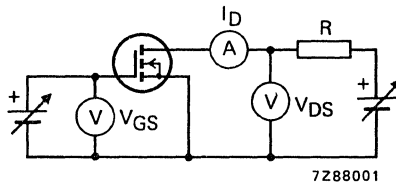
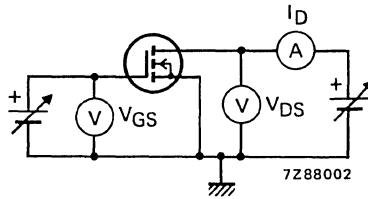


Fig. 4 Circuit for measuring the drain current  $I_D$ .

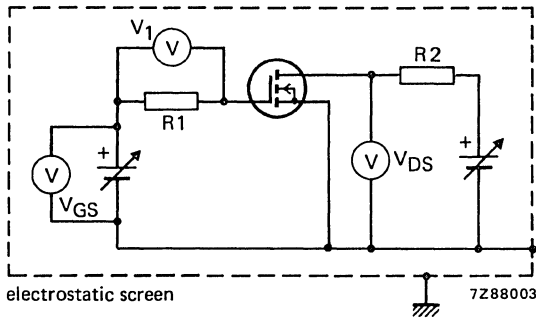
R limits the drain current. The specified gate-source voltage  $V_{GS}$  is set. If  $V_{GS} = 0$  has been specified, the gate and source must be short-circuited.

Drain-source on-resistance  $R_{DS\ ON}$ Fig. 5 Circuit for measuring the on-resistance  $R_{DS\ ON}$ .

In general,  $R_{DS\ ON}$  is measured in the saturation region. The internal resistance of the voltmeter  $V_{DS}$  must be much larger than the turn-on resistance to be measured.

Gate threshold voltage  $V_{GST}$ 

(Use the circuit for measuring  $I_D$ ). The gate-source voltage is slowly increased from zero until the specified drain current is reached.

Gate-source leakage current  $I_{GSS}$ Fig. 6 Circuit for measuring the gate-source leakage current  $I_{GSS}$ .

$R1$  and  $R2$  are protection resistors.  $R1$  should be smaller than  $V_{GS}/100I_{GSS}$ .  $V1$  should have an internal resistance  $> 100 R1$ . The leakage current is given by  $I_{GSS} = V1/R1$ .

The circuit must be electrostatically screened. Take care in the circuit arrangement to prevent leakage currents that would give false results.



Input capacitance  $C_{is}$

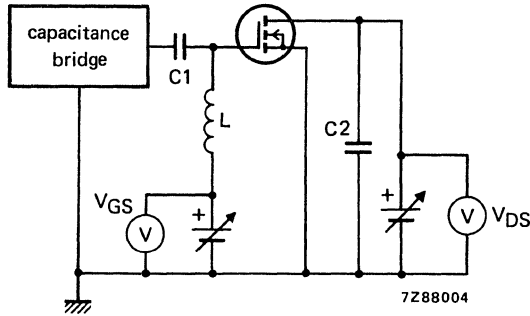


Fig. 7 Circuit for measuring the input capacitance  $C_{is}$ .

The impedances of C1 and C2 should be negligible at the measuring frequency. Inductance L should decouple the d.c. supply.

Output capacitance  $C_{os}$

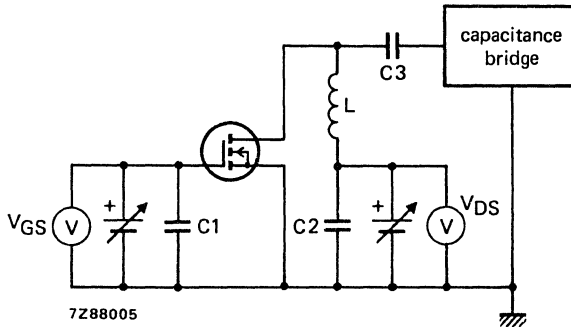


Fig. 8 Circuit for measuring the output capacitance  $C_{os}$ .

The impedances of C1, C2 and C3 should be negligible at the measuring frequency. Inductance L should decouple the d.c. supply.

Feedback capacitance  $C_{rs}$

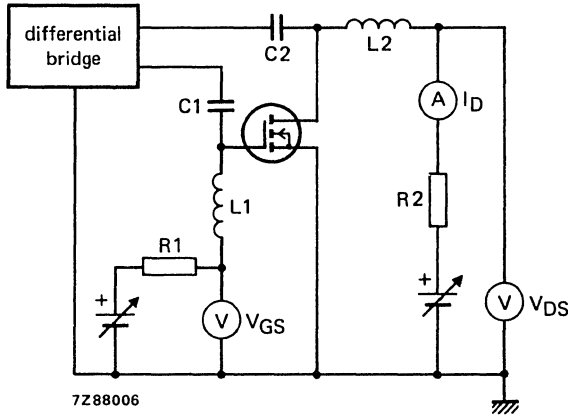


Fig. 9 Circuit for measuring the feedback capacitance  $C_{rs}$ .

The impedances of C1 and C2 should be negligible at the measuring frequency. Inductances L1 and L2 should decouple the d.c. supply.

**THERMAL RESISTANCE**

The thermal resistance between the junction and ambient of a transistor on a heatsink is:

$$R_{th\ j-a} = R_{th\ j-mb} + R_{th\ mb-a}$$

where  $R_{th\ j-mb}$  is the thermal resistance between junction and mounting base and  $R_{th\ mb-a}$  is the thermal resistance between mounting base and ambient.

**SOLDERING INSTRUCTIONS**

Take care that the transistors are not overheated during soldering. Do not move connections whilst soldering.

Recommended soldering times (seconds):

		Distance from soldering point to envelope (mm)	
		1,6	5
Soldering time	( $T_{sld} = 260\text{ }^{\circ}\text{C}$ )	15	15
Soldering time	( $T_{sld} = 300\text{ }^{\circ}\text{C}$ )	10	15

These times apply to hand soldering only. Where automatic soldering techniques are used, ensure that the maximum junction temperature is not exceeded.

# EXPLANATORY NOTES

## DEFINITION OF SYMBOLS USED IN THE DATA SHEETS

### Voltages

$V_{(BR)DSS}$	Drain-source breakdown voltage
$V_{DD}$	Supply voltage
$V_{DGR}$	Drain-gate voltage with a specified gate-source resistance
$V_{DS}$	Drain-source voltage
$V_F$	Forward diode voltage
$V_{GS}$	Gate-source voltage
$V_{GST}$	Gate threshold voltage

### Currents

$I_D$	Drain current (d.c. or average)
$I_{DM}$	Drain current (pulse peak value)
$I_{DSS}$	Zero gate voltage drain current
$I_F$	Forward diode current
$I_{FRM}$	Forward diode current (peak)
$I_{GSS}$	Gate-source leakage current

### Switching times

$t_{d\ off}$	Turn-off delay
$t_{d\ on}$	Turn-on delay
$t_f$	Turn-off fall time
$t_r$	Turn-on rise time

### Capacitances

$C_{is}$	Input capacitance
$C_{os}$	Output capacitance
$C_{rs}$	Feedback capacitance

### Miscellaneous

$g_{fs}$	Forward transfer conductance
$P_{tot}$	Total power dissipation
$R_{DS\ ON}$	Drain-source on-state resistance
$R_{th\ j-mb}$	Thermal resistance from junction to mounting base
$T_j$	Junction temperature
$T_{stg}$	Storage temperature

TRANSISTOR DATA





## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ10

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

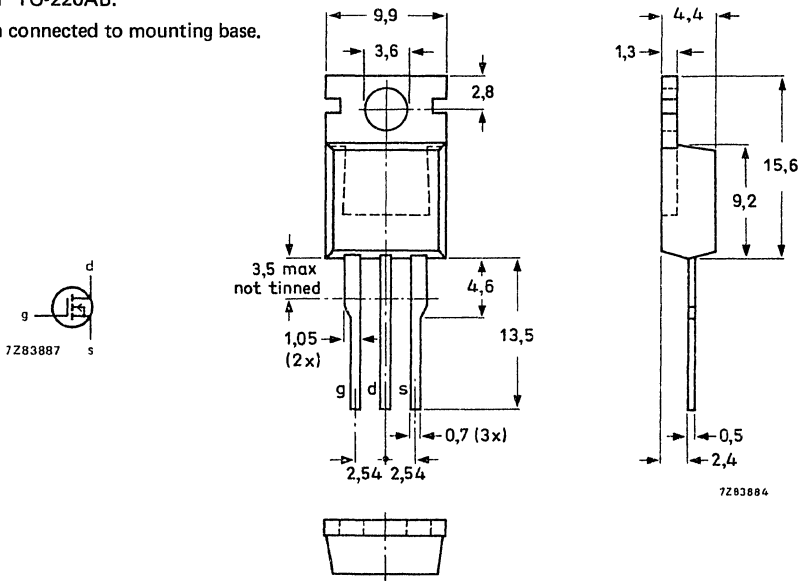
Drain-source voltage	$V_{DS}$	max.	50 V
Drain current (d.c.); $T_{mb} = 100\text{ }^{\circ}\text{C}$	$I_D$	max.	12 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,1 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}$ ; $I_D = 3\text{ A}$ ; $V_{GS} = 10\text{ V}$	$t_f$	typ.	60 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC134)

Drain-source voltage	$V_{DS}$	max.	50 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	50 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 100 \text{ }^\circ\text{C}$	$I_D$	max.	12 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	36 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	50 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 6 \text{ A}$	$R_{DS \text{ ON}}$	typ. <	0,085 $\Omega$ 0,1 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	12 A
Forward current (peak value)	$I_{FRM}$	<	36 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ.	1,4 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$	$t_{rr}$	typ.	150 ns
recovery time	$Q_s$	typ.	1 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 6 \text{ A}$

$g_{fs} > \text{typ. } 3 \text{ A/V}$   
 $4.8 \text{ A/V}$

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is} \text{ typ. } 1500 \text{ pF}$

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os} \text{ typ. } 400 \text{ pF}$

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs} \text{ typ. } 120 \text{ pF}$

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}} \text{ typ. } 20 \text{ ns}$   
 $t_r \text{ typ. } 60 \text{ ns}$

turn-off times: delay time  
 fall time

$t_{d \text{ off}} \text{ typ. } 120 \text{ ns}$   
 $t_f \text{ typ. } 60 \text{ ns}$

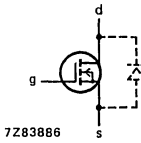


Fig. 2 Diode characteristics.

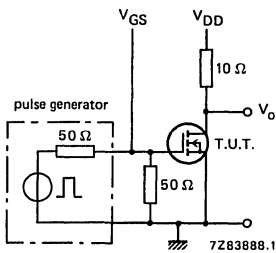


Fig. 3 Switching time test circuit.

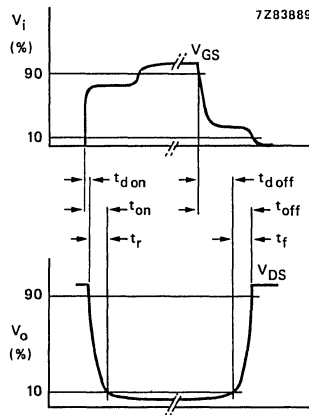


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA



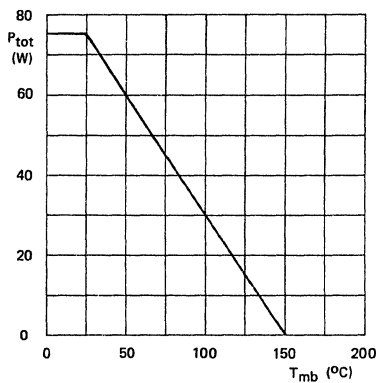


Fig. 5 Power derating curve.

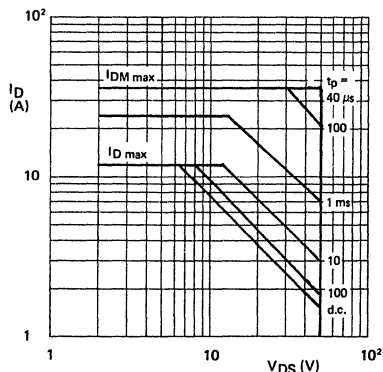


Fig. 6 Safe Operating Area  
 $T_{mb} = 25\text{ }^{\circ}\text{C}; \delta = 0,01.$

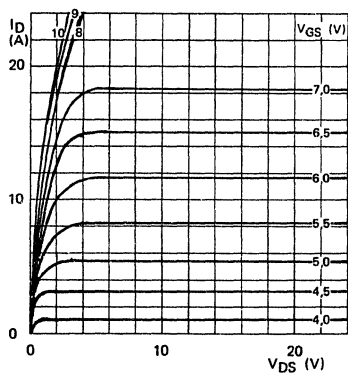


Fig. 7 Output characteristic.  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^{\circ}\text{C}.$

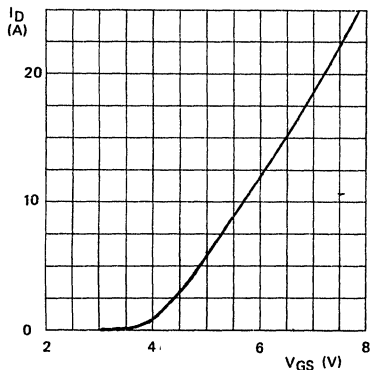


Fig. 8 Typical transfer characteristic  
 at  $V_{DS} = 25\text{ V}.$

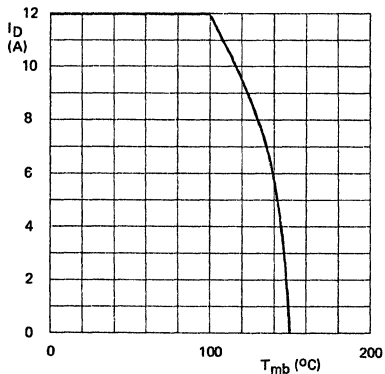


Fig. 9 Drain current as a function  
 of mounting base temperature.

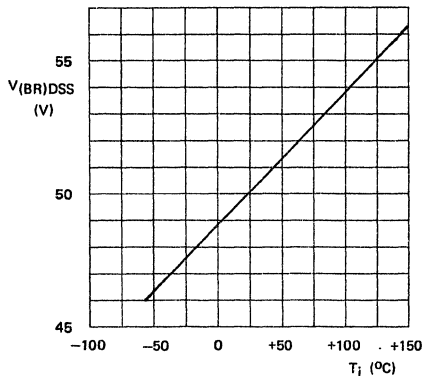


Fig. 10 Drain-source breakdown voltage  
 as a function of junction temperature.

# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ10A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

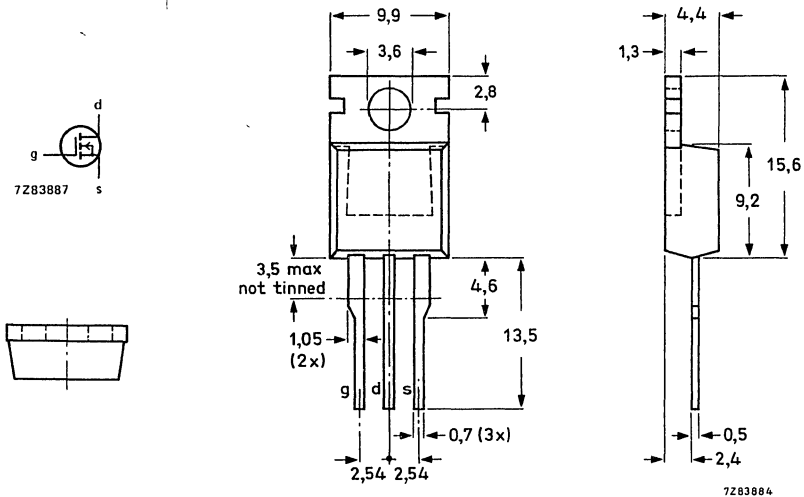
Drain-source voltage	$V_{DS}$	max.	50 V
Drain current (d.c.); $T_{mb} = 90\text{ }^{\circ}\text{C}$	$I_D$	max.	12 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,12 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	60 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	50 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	50 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 90 \text{ }^\circ\text{C}$	$I_D$	max.	12 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	36 A
Total power dissipation	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS****Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS** $T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$

$V_{(BR)DSS} > 50 \text{ V}$

Gate threshold voltage

$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$

$V_{GST} \text{ typ. } 2,1 \text{ to } 4 \text{ V}$   
 $3 \text{ V}$

Zero gate voltage drain current

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$

$I_{DSS} < 1 \text{ mA}$   
 $I_{DSS} < 4 \text{ mA}$

Gate-source leakage current

$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$

$I_{GSS} < 100 \text{ nA}$

Drain-source on-state resistance

$V_{GS} = 10 \text{ V}; I_D = 6 \text{ A}$

$R_{DS \text{ ON}} \text{ typ. } 0,11 \text{ } \Omega$   
 $< 0,12 \text{ } \Omega$

**Diode characteristics** $T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$I_F < 12 \text{ A}$

Forward current (peak value)

$I_{FRM} < 36 \text{ A}$

On-state voltage

$I_F = 2 I_D; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$

$V_F \text{ typ. } 1,4 \text{ V}$   
 $< 1,8 \text{ V}$

Reverse recovery

$I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$

recovery time

$t_{rr} \text{ typ. } 150 \text{ ns}$

recovery charge

$Q_s \text{ typ. } 1 \text{ } \mu\text{C}$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 6 \text{ A}$

$g_{fs}$	>	3,0 A/V
	typ.	4,8 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	1500 pF
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Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	400 pF
----------	------	--------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	120 pF
----------	------	--------

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	20 ns
--------------------	------	-------

rise time

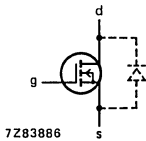
$t_r$	typ.	60 ns
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turn-off times: delay time

$t_{d \text{ off}}$	typ.	120 ns
---------------------	------	--------

fall time

$t_f$	typ.	60 ns
-------	------	-------



7Z83886

Fig. 2 Diode characteristics.

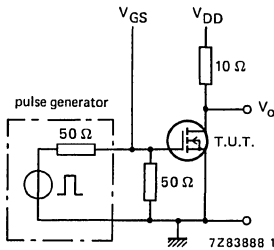


Fig. 3 Switching time test circuit.

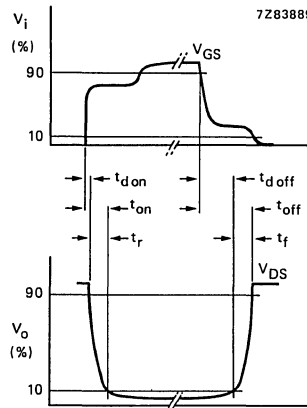


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

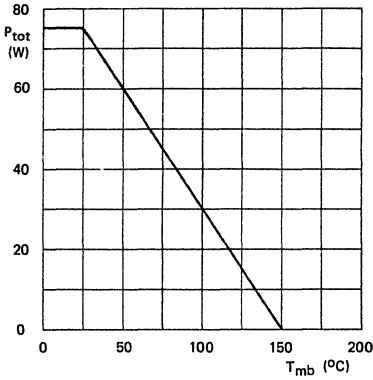


Fig. 5 Power derating curve.

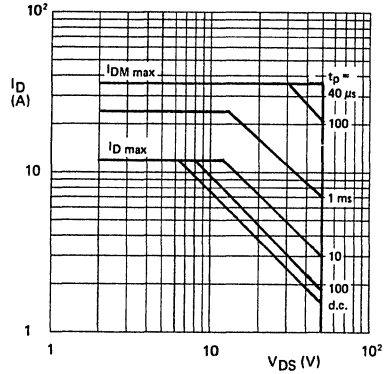


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

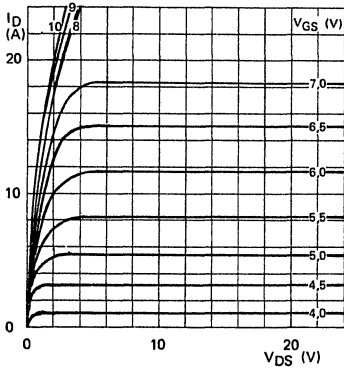


Fig. 7 Output characteristic.  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^{\circ}\text{C}$ .

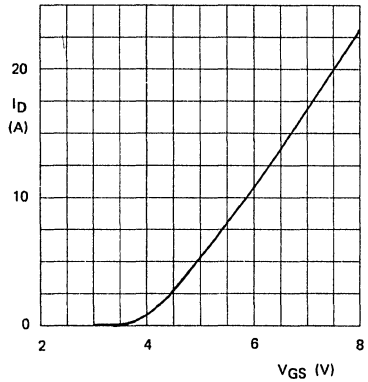


Fig. 8 Typical transfer characteristic  
 at  $V_{DS} = 25\text{ V}$ .

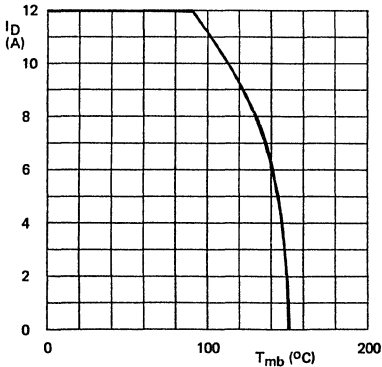


Fig. 9 Drain current as a function  
 of mounting base temperature.

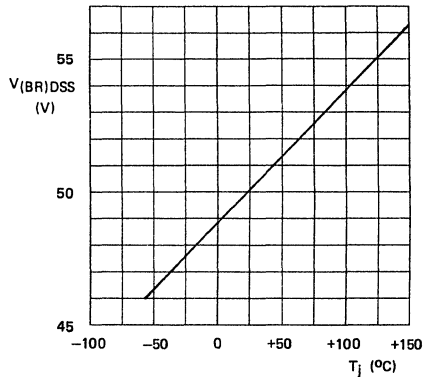


Fig. 10 Drain-source breakdown voltage  
 as a function of junction temperature.

# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ11

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

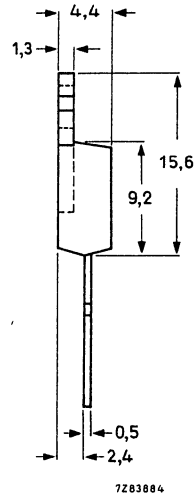
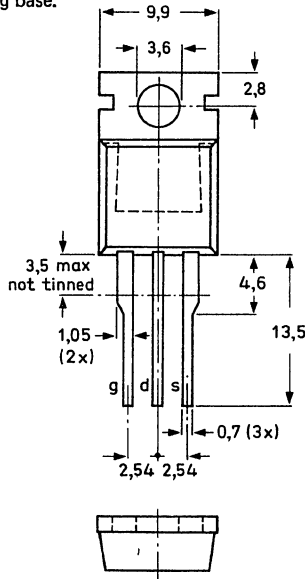
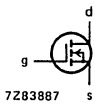
Drain-source voltage	$V_{DS}$	max.	50 V
Drain current (d.c.); $T_{mb} = 25\text{ }^{\circ}\text{C}$	$I_D$	max.	30 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,04 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	450 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	50 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	50 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	30 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	90 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$

$V_{(BR)DSS} > 50 \text{ V}$

Gate threshold voltage

$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$

$V_{GST} \text{ typ. } 2,1 \text{ to } 4 \text{ V}$   
 $3 \text{ V}$

Zero gate voltage drain current

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$

$I_{DSS} < 1 \text{ mA}$

$I_{DSS} < 4 \text{ mA}$

Gate-source leakage current

$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$

$I_{GSS} < 100 \text{ nA}$

Drain-source on-state resistance

$V_{GS} = 10 \text{ V}; I_D = 14 \text{ A}$

$R_{DS \text{ ON}} < 0,04 \text{ } \Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$I_F < 30 \text{ A}$

Forward current (peak value)

$I_{FRM} < 90 \text{ A}$

On-state voltage

$T_j = 25 \text{ }^\circ\text{C}; V_{GS} = 0 \text{ V}; I_D = 2 \times I_F$

$V_F \text{ typ. } 1,7 \text{ V}$

Reverse recovery

$I_D = 2 I_F; dI_F/dt = 100 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$

recovery time

$t_{rr} \text{ typ. } 200 \text{ ns}$

recovery charge

$Q_s \text{ typ. } 0,25 \text{ } \mu\text{C}$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 14 \text{ A}$

$g_{fs} > 4 \text{ A/V}$   
 typ. 8 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 900 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 800 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 360 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 30 ns  
 $t_r$  typ. 220 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 600 ns  
 $t_f$  typ. 450 ns

DEVELOPMENT SAMPLE DATA

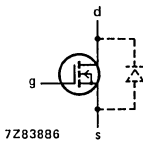


Fig. 2 Diode characteristics.

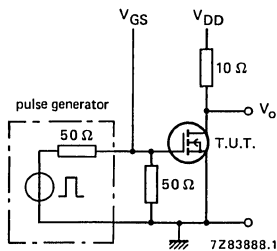


Fig. 3 Switching time test circuit.

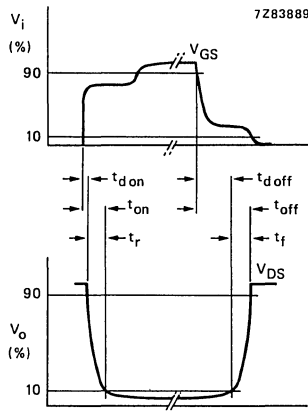


Fig. 4 Switching time waveforms.



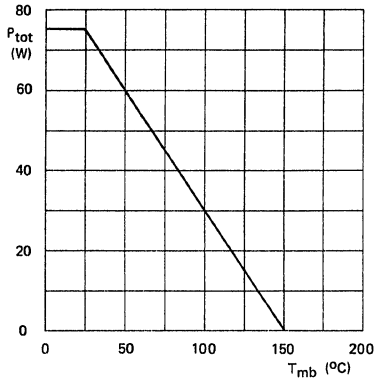


Fig. 5 Power derating curve.

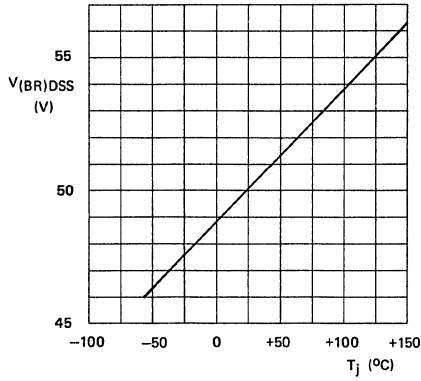


Fig. 6 Drain-source breakdown voltage as a function of junction temperature.

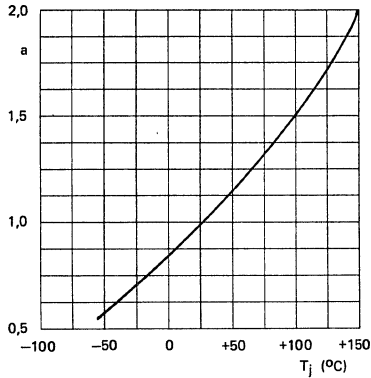


Fig. 7  $R_{DS ON}(T_j) = a \times R_{DS ON}(25\text{ }^\circ\text{C})$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ11A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

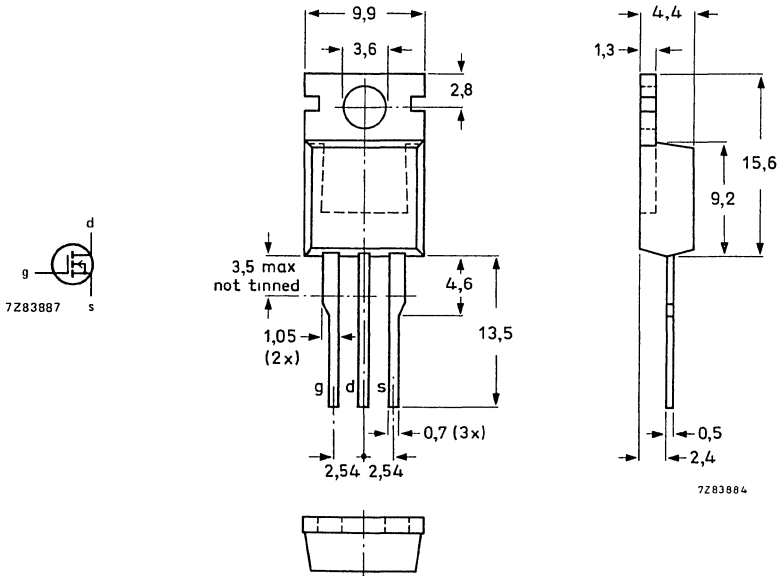
Drain-source voltage	$V_{DS}$	max.	50 V
Drain current (d.c.); $T_{mb} = 25\text{ }^{\circ}\text{C}$	$I_D$	max.	25 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,06 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	450 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	50 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	50 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	25 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	75 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	50 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 14 \text{ A}$	$R_{DS \text{ ON}}$	<	0,06 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	25 A
Forward current (peak value)	$I_{FRM}$	<	75 A
On-state voltage $T_j = 25 \text{ }^\circ\text{C}; V_{GS} = 0 \text{ V}; I_D = 2 \times I_F$	$V_F$	typ. <	1,6 V 2,4 V
Reverse recovery $I_D = 2 \text{ I}_F; dI_F/dt = 100 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$	$t_{rr}$	typ.	200 ns
recovery time	$Q_s$	typ.	0,25 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 14 \text{ A}$

$g_{fs}$	>	4 A/V
	typ.	8 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	900 pF
----------	------	--------

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	800 pF
----------	------	--------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	360 pF
----------	------	--------

Switching times (see Figs 3 and 4)  
(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

rise time

$t_{d \text{ on}}$	typ.	30 ns
--------------------	------	-------

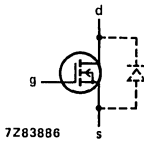
$t_r$	typ.	220 ns
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turn-off times: delay time

fall time

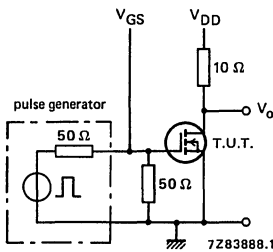
$t_{d \text{ off}}$	typ.	600 ns
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$t_f$	typ.	450 ns
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7Z83886

Fig. 2 Diode characteristics.



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Fig. 3 Switching time test circuit.

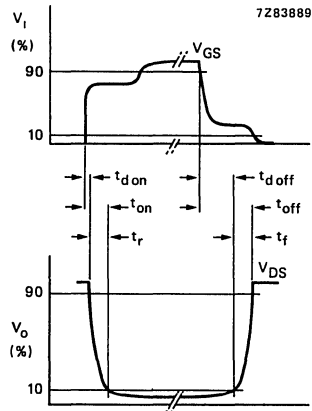


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA



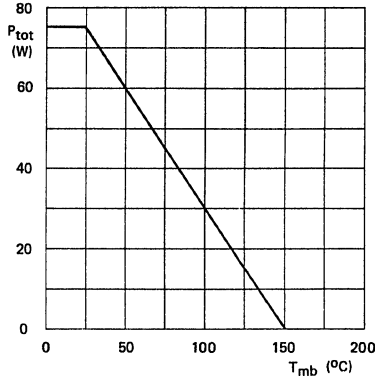


Fig. 5 Power derating curve.

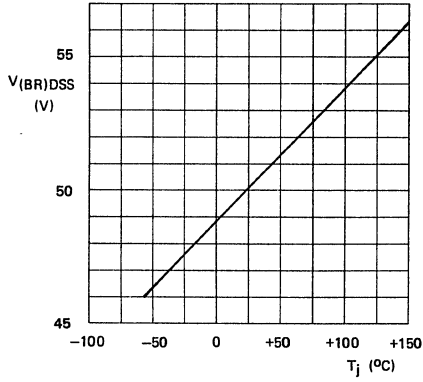


Fig. 6 Drain-source breakdown voltage as a function of junction temperature.

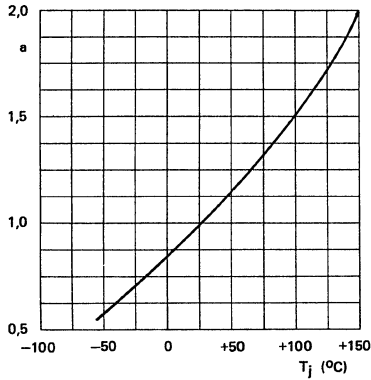


Fig. 7  $R_{DS ON}(T_j) = a \times R_{DS ON}(25\text{ }^\circ\text{C})$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ14

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

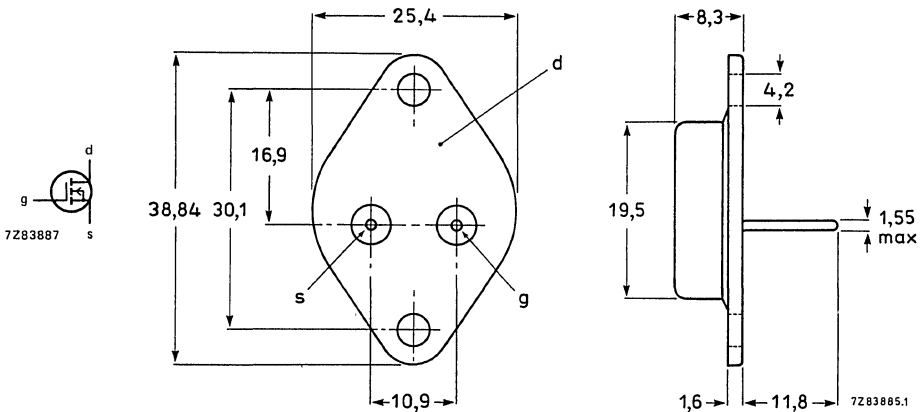
Drain-source voltage	$V_{DS}$	max.	50 V
Drain current (d.c.)	$I_D$	max.	39 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,04 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	200 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	50 V
Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	$V_{DGR}$	max.	50 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25\text{ }^\circ\text{C}$	$I_D$	max.	39 A
Drain current (pulse peak value); $T_{mb} = 25\text{ }^\circ\text{C}$	$I_{DM}$	max.	115 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th\ j-mb}$	=	1,0 K/W
From junction to ambient	$R_{th\ j-a}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0\text{ V}; I_D = 1\text{ mA}$	$V_{(BR)DSS}$	>	50 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10\text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3,0 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25\text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125\text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20\text{ V}; V_{DS} = 0\text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10\text{ V}; I_D = 22\text{ A}$	$R_{DS\ ON}$	typ. <	0,035 $\Omega$ 0,04 $\Omega$

**Diode characteristics**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	39 A
Forward current (peak value)	$I_{FRM}$	<	115 A
On-state voltage $I_F = 2\text{ I}_D; V_{GS} = 0\text{ V}$	$V_F$	<	2,2 V
Reverse recovery $I_F = 2\text{ I}_D; dI_F/dt = 100\text{ A}/\mu\text{s}$	$t_{rr}$	typ.	150 ns
recovery time	$Q_s$	typ.	1 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 6 \text{ A}$

$g_{fs}$	>	7 A/V
	typ.	12 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	1500 pF
----------	------	---------

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	1200 pF
----------	------	---------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	500 pF
----------	------	--------

Switching times (see Figs 3 and 4)  
(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

rise time

$t_{d \text{ on}}$	typ.	50 ns
$t_r$	typ.	200 ns

turn-off times: delay time

fall time

$t_{d \text{ off}}$	typ.	300 ns
$t_f$	typ.	200 ns

DEVELOPMENT SAMPLE DATA

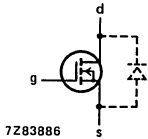


Fig. 2 Diode characteristics.

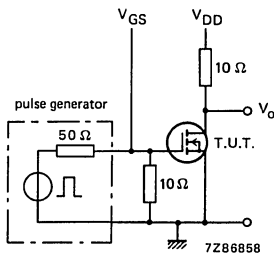


Fig. 3 Switching time test circuit.

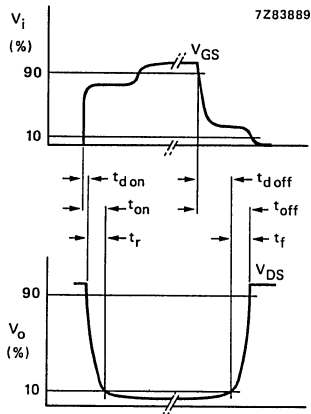


Fig. 4 Switching time waveforms.



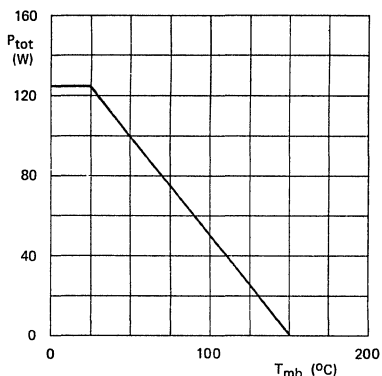


Fig. 5 Power derating curve.

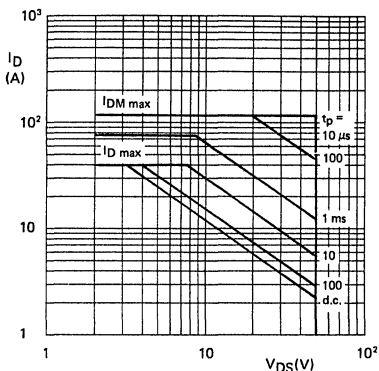


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

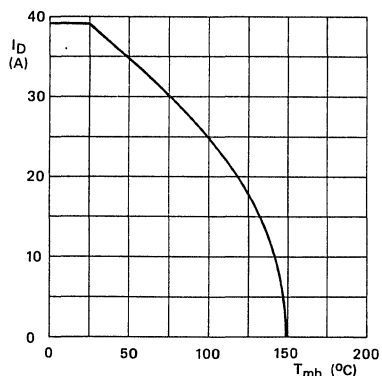


Fig. 7 Drain current as a function of mounting base temperature.

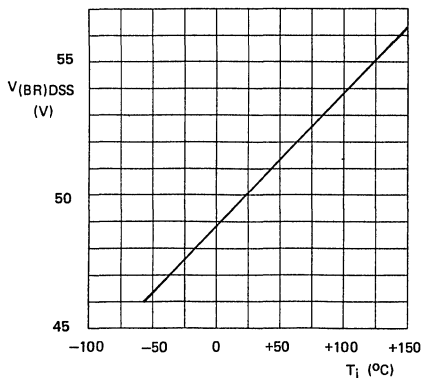


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

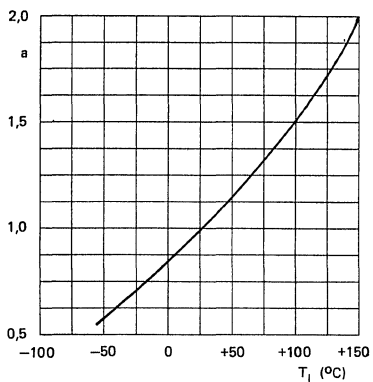


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^{\circ}\text{C})$ .

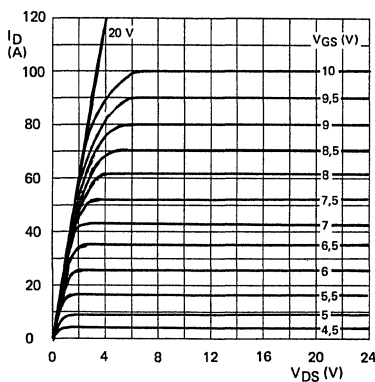


Fig. 10 Typical output characteristic.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $t_p = 80\text{ }\mu\text{s}$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ15

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

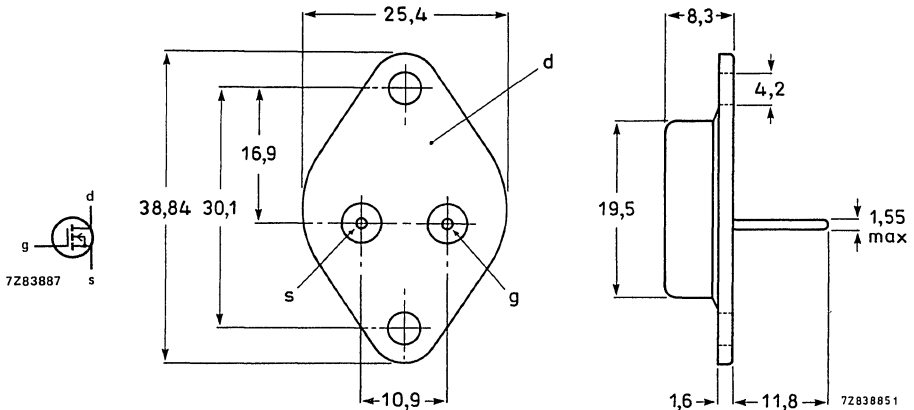
Drain-source voltage	$V_{DS}$	max.	50 V
Drain current (d.c.)	$I_D$	max.	45 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,03 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	200 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	50 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	50 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	45 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	135 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,0 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$   $V_{(BR)DSS} > 50 \text{ V}$

Gate threshold voltage

$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$   $V_{GST} \begin{matrix} 2,1 \text{ to } 4,0 \text{ V} \\ \text{typ. } 3,0 \text{ V} \end{matrix}$

Zero gate voltage drain current

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$   $I_{DSS} < 1 \text{ mA}$   
 $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$   $I_{DSS} < 4 \text{ mA}$

Gate-source leakage current

$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$   $I_{GSS} < 100 \text{ nA}$

Drain-source on-state resistance

$V_{GS} = 10 \text{ V}; I_D = 22 \text{ A}$   $R_{DS \text{ ON}} \begin{matrix} \text{typ. } 0,025 \text{ } \Omega \\ < 0,03 \text{ } \Omega \end{matrix}$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$I_F < 45 \text{ A}$

Forward current (peak value)

$I_{FRM} < 135 \text{ A}$

On-state voltage

$I_F = 2 I_D; V_{GS} = 0 \text{ V}$   $V_F < 2,4 \text{ V}$

Reverse recovery

$I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$   
 recovery time  $t_{rr} \text{ typ. } 150 \text{ ns}$   
 recovery charge  $Q_s \text{ typ. } 1 \text{ } \mu\text{C}$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance $V_{DS} = 25\text{ V}; I_D = 22\text{ A}$	$g_{fs}$	> typ.	7 A/V 12 A/V
Input capacitance at $f = 1\text{ MHz}$ $V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}$	$C_{is}$	typ.	1500 pF
Output capacitance at $f = 1\text{ MHz}$ $V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}$	$C_{os}$	typ.	1200 pF
Feedback capacitance at $f = 1\text{ MHz}$ $V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}$	$C_{rs}$	typ.	500 pF
Switching times (see Figs 3 and 4) (between 10% and 90% levels) $V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 10\text{ V}$			
turn-on times: delay time	$t_{d\text{ on}}$	typ.	50 ns
rise time	$t_r$	typ.	200 ns
turn-off times: delay time	$t_{d\text{ off}}$	typ.	300 ns
fall time	$t_f$	typ.	200 ns

DEVELOPMENT SAMPLE DATA

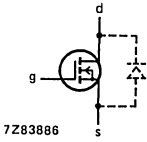


Fig. 2 Diode characteristics.

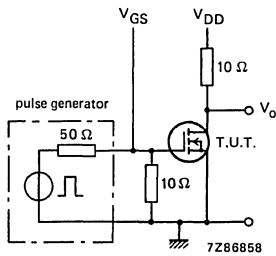


Fig. 3 Switching time test circuit.

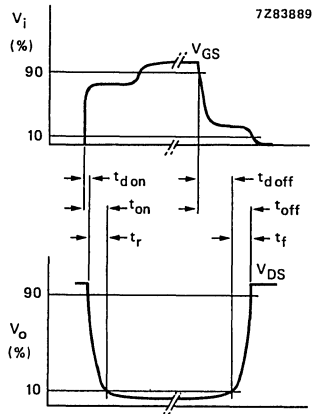


Fig. 4 Switching time waveforms.

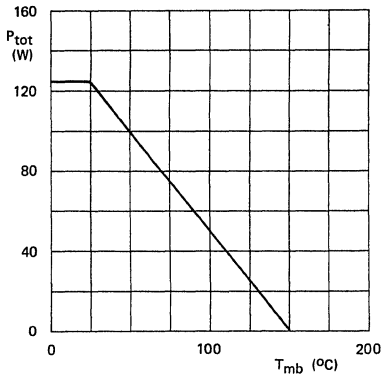


Fig. 5 Power derating curve.

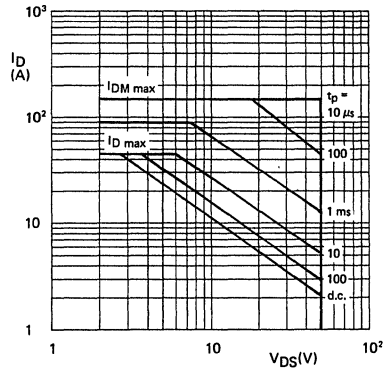


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

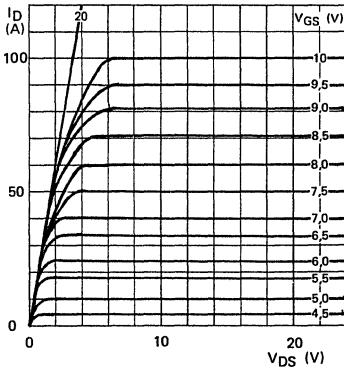


Fig. 7 Output characteristic.  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^\circ\text{C}$ .

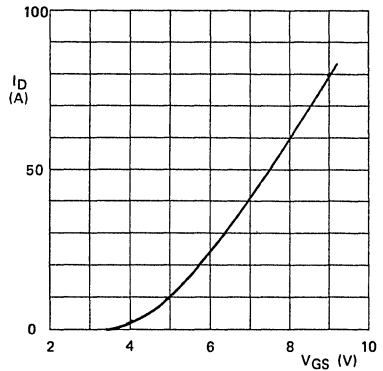


Fig. 8 Typical transfer characteristic  
 at  $V_{DS} = 25\text{ V}$ .

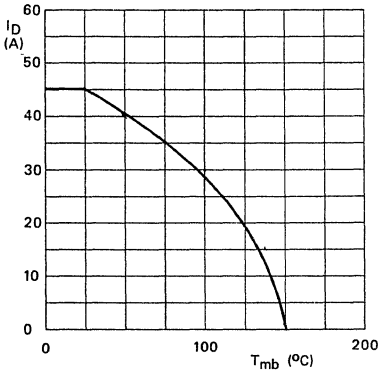


Fig. 9 Drain current as a function  
 of mounting base temperature.

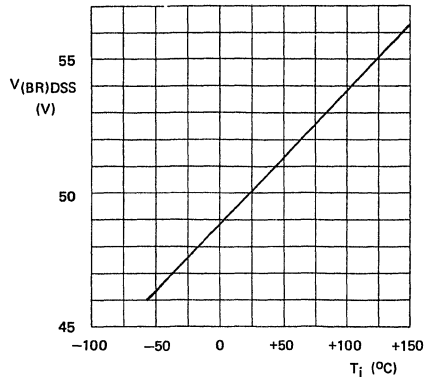


Fig. 10 Drain-source breakdown voltage  
 as a function of junction temperature.

# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ20

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.  
Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

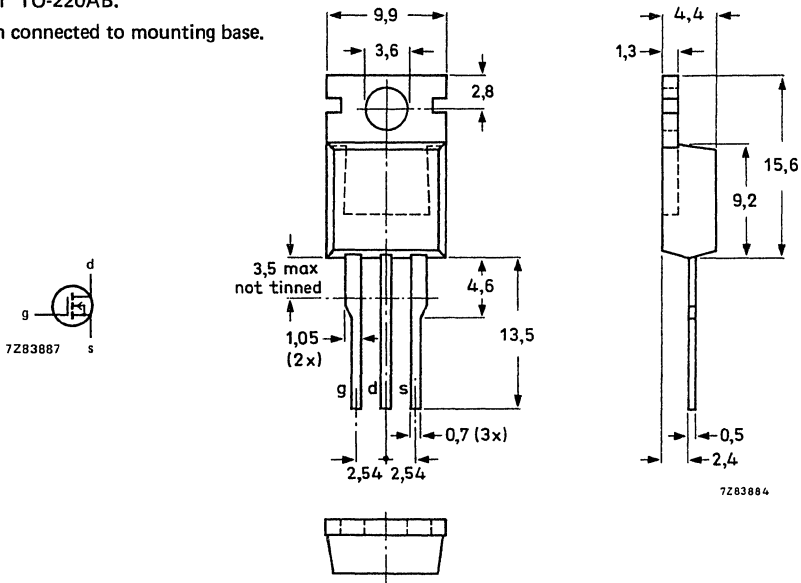
Drain-source voltage	$V_{DS}$	max.	100 V
Drain current (d.c.)	$I_D$	max.	12 A
Total power dissipation; $T_{mb} = 50\text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,2 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,9\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	60 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	100 V
Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	$V_{DGR}$	max.	100 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 50\text{ }^\circ\text{C}$	$I_D$	max.	12 A
Drain current (pulse peak value); $T_{mb} = 25\text{ }^\circ\text{C}$	$I_{DM}$	max.	36 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th\ j-mb}$	=	1,67 K/W
From junction to ambient	$R_{th\ j-a}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0\text{ V}; I_D = 1\text{ mA}$	$V_{(BR)DSS}$	>	100 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10\text{ mA}$	$V_{GST}$	typ.	2,1 to 4,0 V 3,0 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25\text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125\text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20\text{ V}; V_{DS} = 0\text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10\text{ V}; I_D = 6\text{ A}$	$R_{DS\ ON}$	typ.	0,15 $\Omega$ < 0,2 $\Omega$

**Diode characteristics**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	12 A
Forward current (peak value)	$I_{FRM}$	<	36 A
On-state voltage $I_F = 2\text{ }I_D; V_{GS} = 0\text{ V}$	$V_F$	typ.	1,4 V < 1,8 V
Reverse recovery $I_F = 2\text{ }I_D; dI_F/dt = 100\text{ A}/\mu\text{s}$	$t_{rr}$	typ.	200 ns
recovery time	$Q_s$	typ.	1,6 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 6 \text{ A}$

$g_{fs} >$  typ. 2,7 A/V  
4,0 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1500 pF

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 300 pF

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 80 pF

Switching times (see Figs 3 and 4)  
(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,9 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

rise time

$t_{d \text{ on}}$  typ. 20 ns

$t_r$  typ. 60 ns

turn-off times: delay time

fall time

$t_{d \text{ off}}$  typ. 120 ns

$t_f$  typ. 60 ns

DEVELOPMENT SAMPLE DATA

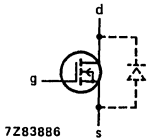


Fig. 2 Diode characteristics.

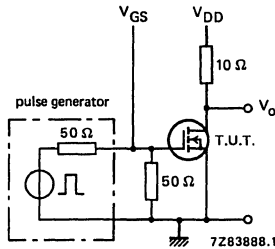


Fig. 3 Switching time test circuit.

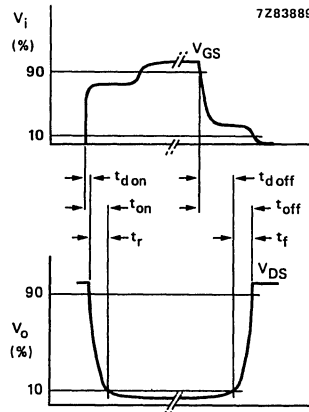


Fig. 4 Switching time waveforms.



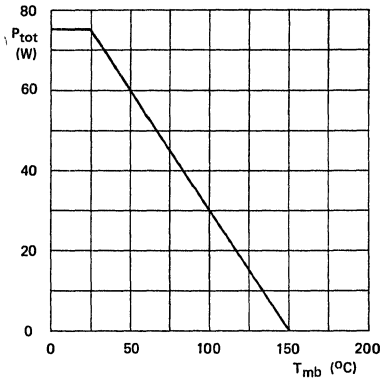


Fig. 5 Power derating curve.

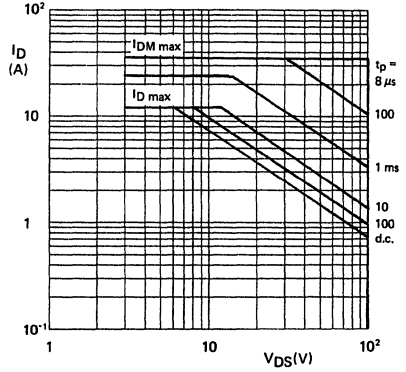


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

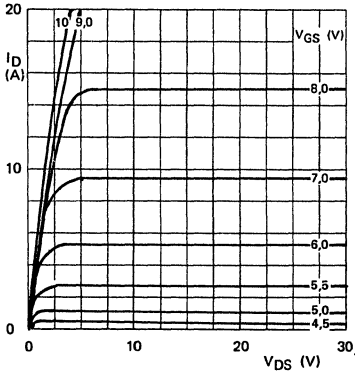


Fig. 7 Output characteristic.  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^\circ\text{C}$ .

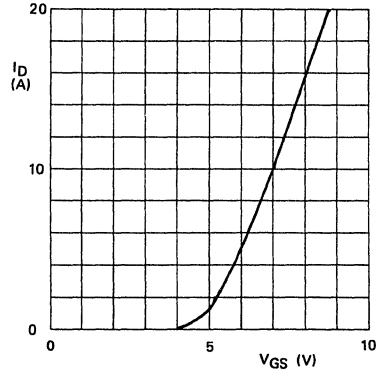


Fig. 8 Typical transfer characteristic  
 at  $V_{DS} = 25\text{ V}$ .

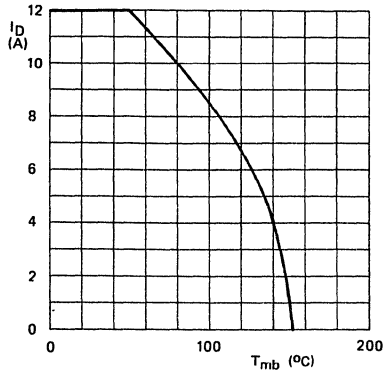


Fig. 9 Drain current as a function  
 of mounting base temperature.

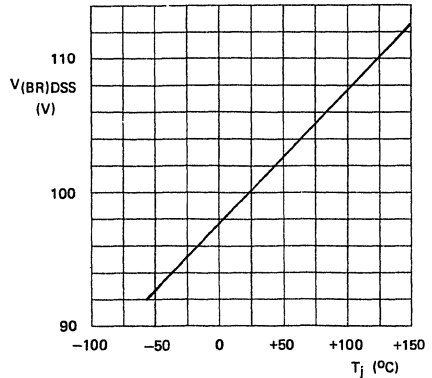


Fig. 10 Drain-source breakdown voltage  
 as a function of junction temperature.

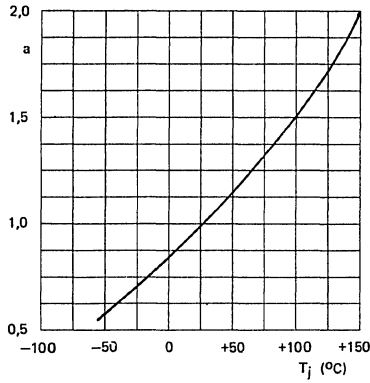


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ\text{C})$ .

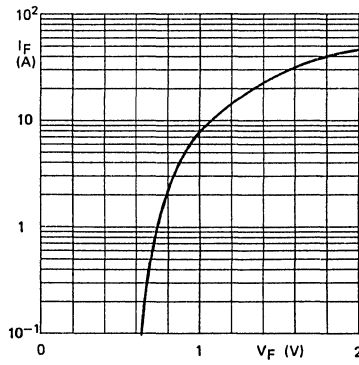


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu\text{s}$ ;  $T_j = 25\ ^\circ\text{C}$ .

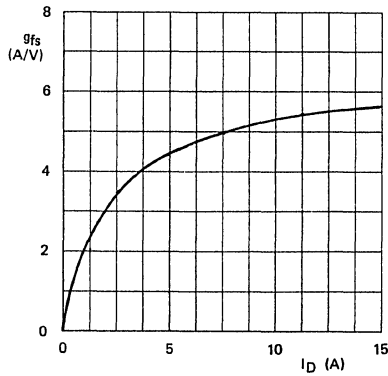


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ \text{V}$ ;  $T_j = 25\ ^\circ\text{C}$ .



# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ21

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

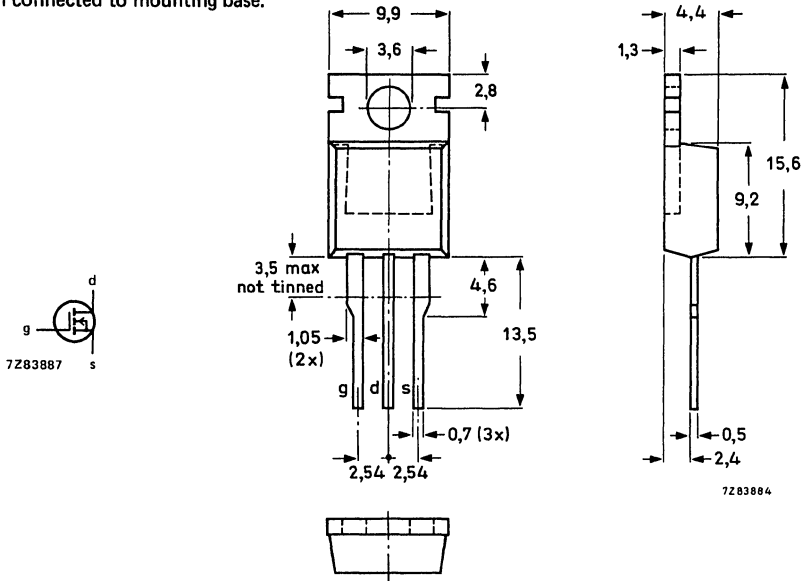
Drain-source voltage	$V_{DS}$	max.	100 V
Drain current (d.c.)	$I_D$	max.	18 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,1 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	60 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	100 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	100 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 40 \text{ }^\circ\text{C}$	$I_D$	max.	18 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	54 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	100 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4,0 V 3,0 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 9 \text{ A}$	$R_{DS \text{ ON}}$	typ. <	0,09 $\Omega$ 0,1 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	18 A
Forward current (peak value)	$I_{FRM}$	<	54 A
On-state voltage $I_F = 2 \times I_D; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	$V_F$	typ. <	1,6 V 2,2 V
Reverse recovery $I_F = 2 \times I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$	$t_{rr}$	typ.	200 ns
recovery time	$Q_s$	typ.	1,6 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 9 \text{ A}$

$g_{fs} > 3,5 \text{ A/V}$   
 typ. 6 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1000 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 450 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 200 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 20 ns  
 $t_r$  typ. 60 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 120 ns  
 $t_f$  typ. 60 ns

DEVELOPMENT SAMPLE DATA

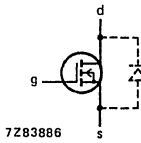


Fig. 2 Diode characteristics.

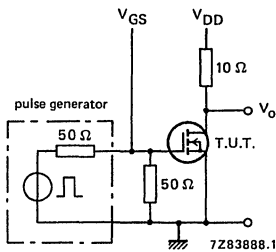


Fig. 3 Switching time test circuit.

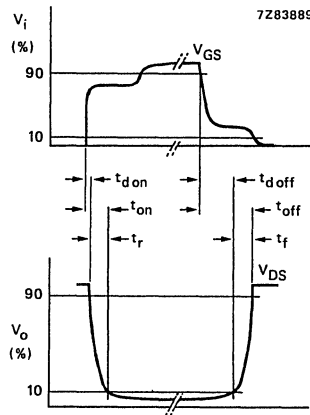


Fig. 4 Switching time waveforms.

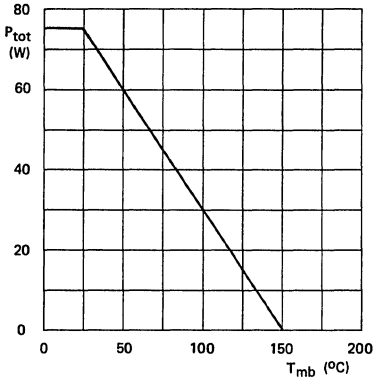


Fig. 5 Power derating curve.

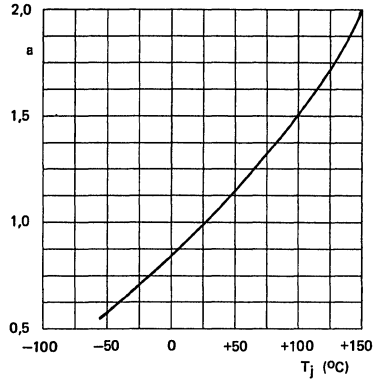


Fig. 6  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ C)$ .

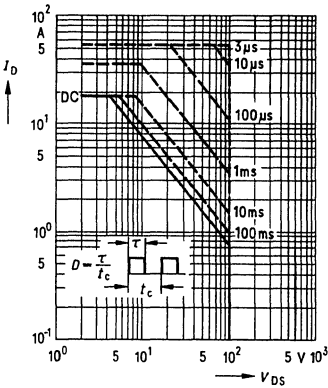


Fig. 7 Safe Operating Area.  
 $T_{mb} = 25\ ^\circ C$ ;  $\delta = 0,01$ .

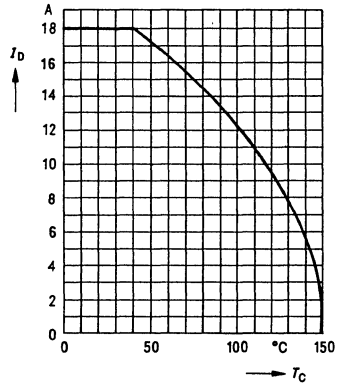


Fig. 8 Drain current as a function of mounting base temperature.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ23

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

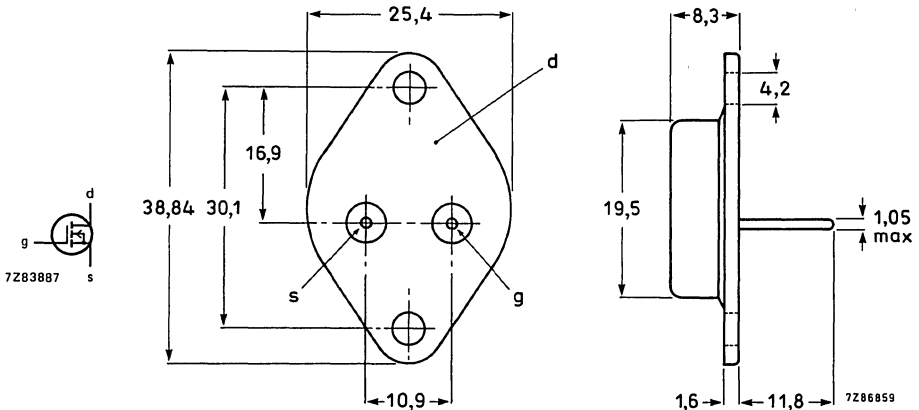
Drain-source voltage	$V_{DS}$	max.	100 V
Drain current (d.c.)	$I_D$	max.	10 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	78 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,2 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	60 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	100 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	100 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 85 \text{ }^\circ\text{C}$	$I_D$	max.	10 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	30 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

## THERMAL CHARACTERISTICS

### Thermal resistance

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

## STATIC CHARACTERISTICS

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$$

$$V_{(BR)DSS} > 100 \text{ V}$$

Gate threshold voltage

$$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$$

$$V_{GST} \text{ typ. } 2,1 \text{ to } 4 \text{ V} \\ 3 \text{ V}$$

Zero gate voltage drain current

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$$

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$$

$$I_{DSS} < 1 \text{ mA}$$

$$I_{DSS} < 4 \text{ mA}$$

Gate-source leakage current

$$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$$

$$I_{GSS} < 100 \text{ nA}$$

Drain-source on-state resistance

$$V_{GS} = 10 \text{ V}; I_D = 6 \text{ A}$$

$$R_{DS \text{ ON}} \text{ typ. } 0,15 \text{ } \Omega \\ < 0,2 \text{ } \Omega$$

### Diode characteristics

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$$I_F < 10 \text{ A}$$

Forward current (peak value)

$$I_{FRM} < 30 \text{ A}$$

On-state voltage

$$I_F = 2 \times I_D; V_{GS} = 0 \text{ V}$$

$$V_F \text{ typ. } 1,3 \text{ V} \\ < 1,6 \text{ V}$$

Reverse recovery

$$I_F = 2 \times I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$$

recovery time

$$t_{rr} \text{ typ. } 200 \text{ ns}$$

recovery charge

$$Q_s \text{ typ. } 1,6 \text{ } \mu\text{C}$$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 6 \text{ A}$

$g_{fs} >$  typ. 2,7 A/V  
 4 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1400 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 300 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 80 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,9 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$  typ. 20 ns

rise time

$t_r$  typ. 60 ns

turn-off times: delay time

$t_{d \text{ off}}$  typ. 120 ns

fall time

$t_f$  typ. 60 ns

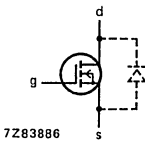


Fig. 2 Diode characteristics.

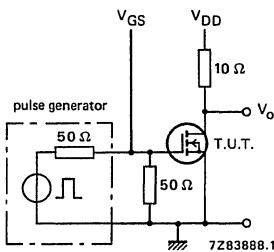


Fig. 3 Switching time test circuit.

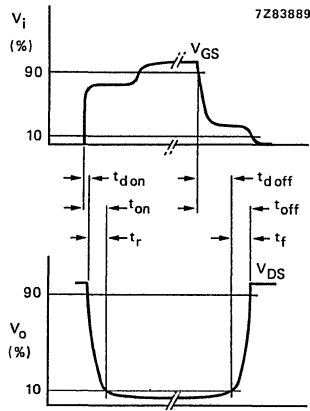


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

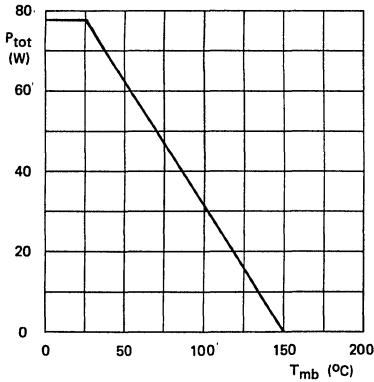


Fig. 5 Power derating curve.

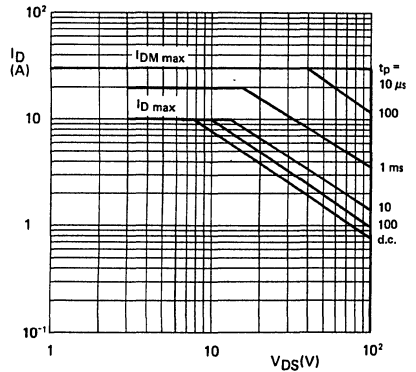


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

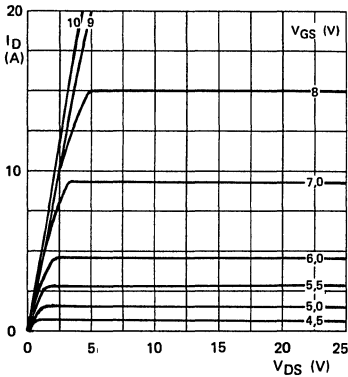


Fig. 7 Output characteristics.  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^\circ\text{C}$ .

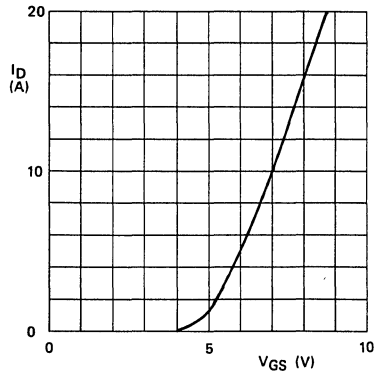


Fig. 8 Typical transfer characteristic  
 at  $V_{DS} = 25\text{ V}$ .

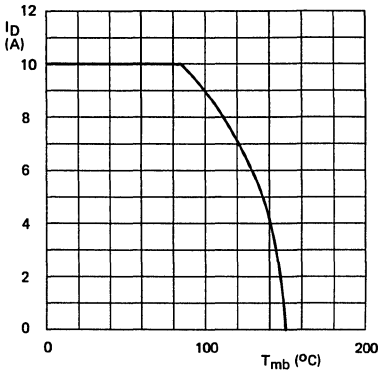


Fig. 9 Drain current as a function  
 of mounting base temperature.

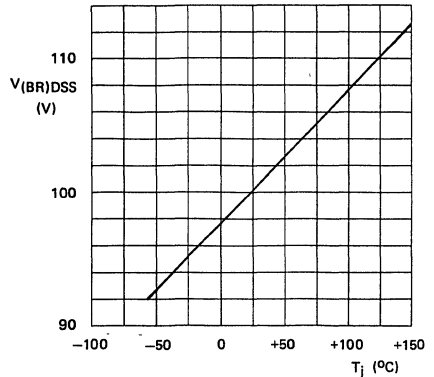


Fig. 10 Drain-source breakdown voltage  
 as a function of junction temperature.

DEVELOPMENT SAMPLE DATA

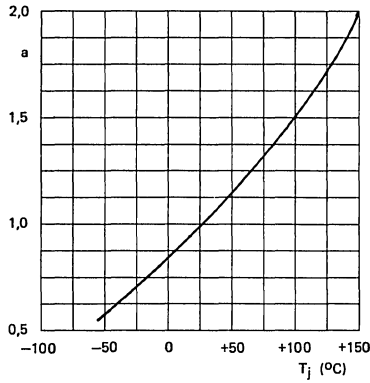


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ C)$ .

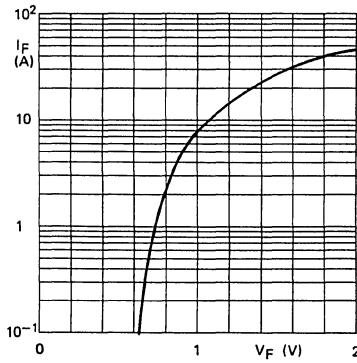


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu s$ ;  $T_j = 25\ ^\circ C$ .

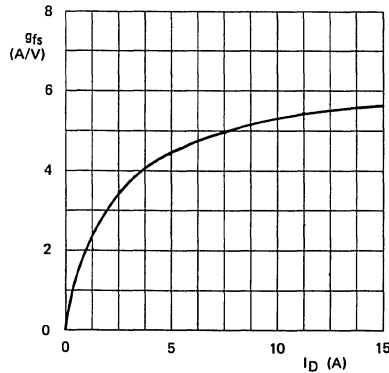


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ V$ ;  $T_j = 25\ ^\circ C$ .



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ24

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

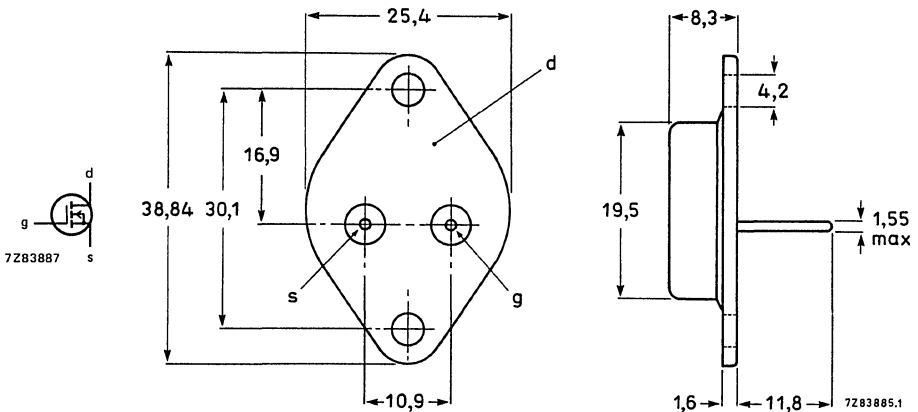
Drain-source voltage	$V_{DS}$	max.	100 V
Drain current (d.c.)	$I_D$	max.	32 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,06 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	200 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	100 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	100 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	32 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	95 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,0 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	100 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 16 \text{ A}$	$R_{DS \text{ ON}}$	typ. <	0,055 $\Omega$ 0,06 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	32 A
Forward current (peak value)	$I_{FRM}$	<	95 A
On-state voltage $I_F = 2 \times I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,5 V 2,0 V
Reverse recovery $I_F = 2 \times I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	200 ns
recovery time	$Q_s$	typ.	1,6 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 16 \text{ A}$

$g_{fs} > \begin{matrix} 6 \text{ A/V} \\ \text{typ. } 10 \text{ A/V} \end{matrix}$

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is} \text{ typ. } 1500 \text{ pF}$

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os} \text{ typ. } 900 \text{ pF}$

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs} \text{ typ. } 500 \text{ pF}$

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time  
 turn-off times: delay time  
 fall time

$t_{d \text{ on}} \text{ typ. } 50 \text{ ns}$   
 $t_r \text{ typ. } 200 \text{ ns}$   
 $t_{d \text{ off}} \text{ typ. } 300 \text{ ns}$   
 $t_f \text{ typ. } 200 \text{ ns}$

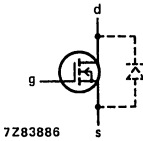


Fig. 2 Diode characteristics.

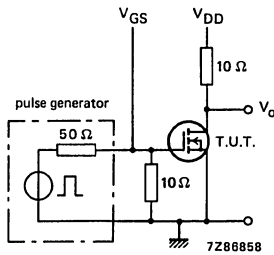


Fig. 3 Switching time test circuit.

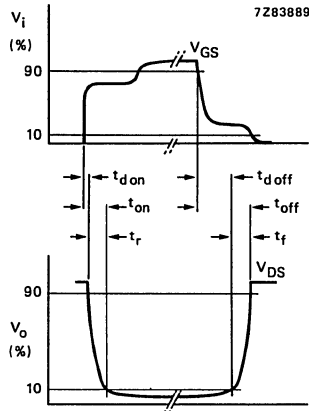


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA



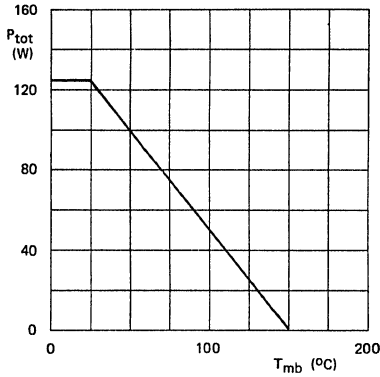


Fig. 5 Power derating curve.

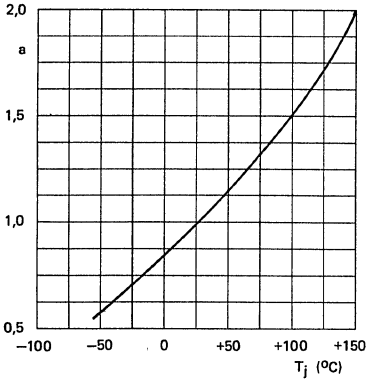


Fig. 7  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ C)$ .

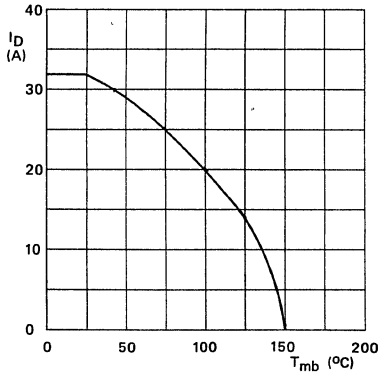


Fig. 9 Drain current as a function of mounting base temperature.

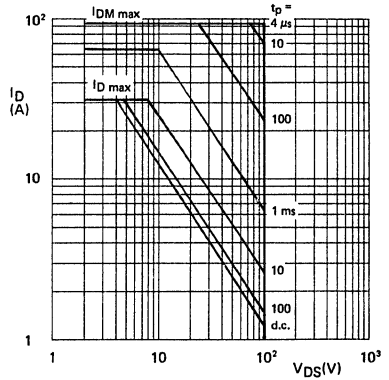


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\ ^\circ C$ ;  $\delta = 0,01$ .

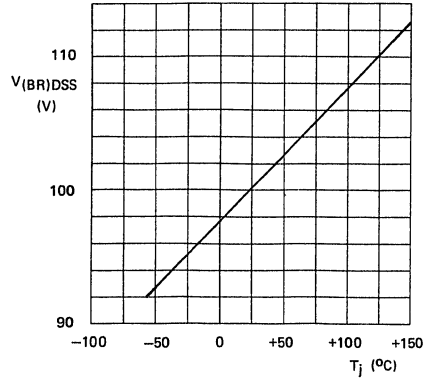


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ25

# POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

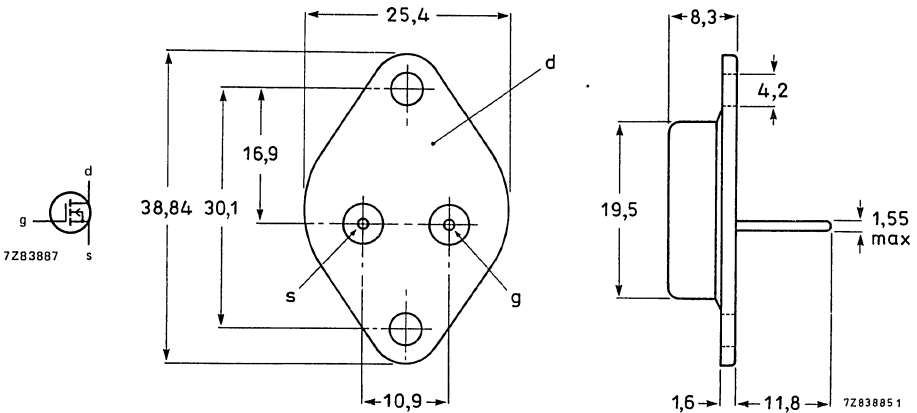
Drain-source voltage	$V_{DS}$	max.	100 V
Drain current (d.c.)	$I_D$	max.	19 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	78 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,1 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	320 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	100 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	100 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 30 \text{ }^\circ\text{C}$	$I_D$	max.	19 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	57 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$

$V_{(BR)DSS} > 100 \text{ V}$

Gate threshold voltage

$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$

$V_{GST} \text{ typ. } 2,1 \text{ to } 4 \text{ V}$   
 $3 \text{ V}$

Zero gate voltage drain current

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$   
 $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$

$I_{DSS} < 1 \text{ mA}$   
 $I_{DSS} < 4 \text{ mA}$

Gate-source leakage current

$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$

$I_{GSS} < 100 \text{ nA}$

Drain-source on-state resistance

$V_{GS} = 10 \text{ V}; I_D = 9 \text{ A}$

$R_{DS \text{ ON}} \text{ typ. } 0,09 \text{ } \Omega$   
 $< 0,1 \text{ } \Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$I_F < 19 \text{ A}$

Forward current (peak value)

$I_{FRM} < 57 \text{ A}$

On-state voltage

$I_F = 2 \times I_D; V_{GS} = 0 \text{ V}$

$V_F \text{ typ. } 1,5 \text{ V}$   
 $< 2,1 \text{ V}$

Reverse recovery

$I_F = 2 \times I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$   
 recovery time  
 recovery charge

$t_{rr} \text{ typ. } 200 \text{ ns}$   
 $Q_s \text{ typ. } 0,25 \text{ } \mu\text{C}$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 9 \text{ A}$

$g_{fs}$	>	4 A/V
	typ.	8 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	900 pF
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Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	450 pF
----------	------	--------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	200 pF
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Switching times (see Figs 3 and 4)  
(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

rise time

$t_{d \text{ on}}$	typ.	35 ns
--------------------	------	-------

$t_r$	typ.	120 ns
-------	------	--------

turn-off times: delay time

fall time

$t_{d \text{ off}}$	typ.	600 ns
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$t_f$	typ.	320 ns
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DEVELOPMENT SAMPLE DATA

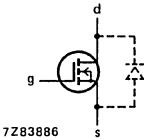


Fig. 2 Diode characteristics.

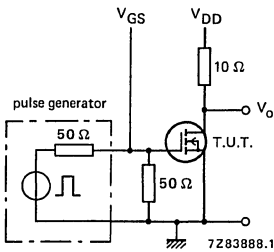


Fig. 3 Switching time test circuit.

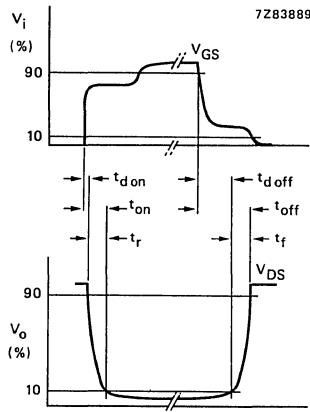


Fig. 4 Switching time waveforms.

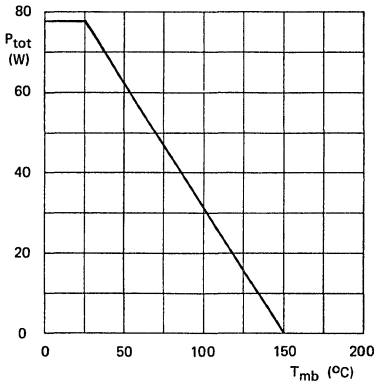


Fig. 5 Power derating curve.

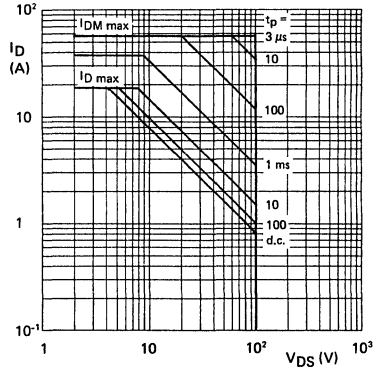


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ °C}; \delta = 0,01.$

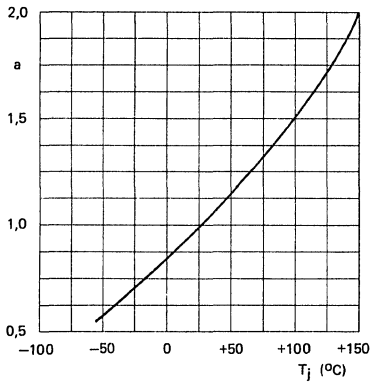


Fig. 7  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ °C}).$

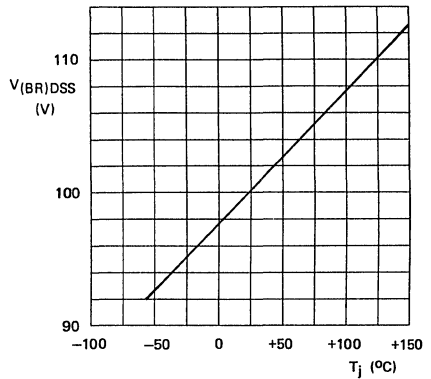


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

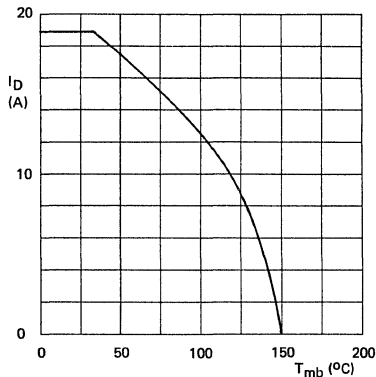


Fig. 9 Drain current as a function of mounting base temperature.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ30

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

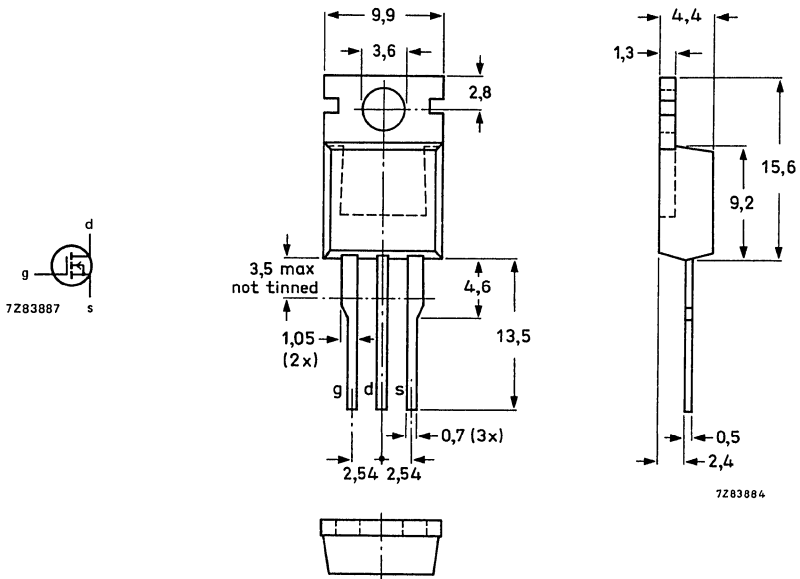
Drain-source voltage	$V_{DS}$	max.	200 V
Drain current (d.c.)	$I_D$	max.	7 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,75 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,8\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	60 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	200 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	7 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	21 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

## THERMAL CHARACTERISTICS

### Thermal resistance

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

## STATIC CHARACTERISTICS

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$$

$$V_{(BR)DSS} > 200 \text{ V}$$

Gate threshold voltage

$$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$$

$$V_{GST} \text{ typ. } 2,1 \text{ to } 4 \text{ V}$$

$$3 \text{ V}$$

Zero gate voltage drain current

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$$

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$$

$$I_{DSS} < 1 \text{ mA}$$

$$I_{DSS} < 4 \text{ mA}$$

Gate-source leakage current

$$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$$

$$I_{GSS} < 100 \text{ nA}$$

Drain-source on-state resistance

$$V_{GS} = 10 \text{ V}; I_D = 4,5 \text{ A}$$

$$R_{DS \text{ ON}} \text{ typ. } 0,45 \text{ } \Omega$$

$$< 0,75 \text{ } \Omega$$

### Diode characteristics

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$$I_F < 7 \text{ A}$$

Forward current (peak value)

$$I_{FRM} < 21 \text{ A}$$

On-state voltage

$$I_F = 2 I_D; V_{GS} = 0 \text{ V}$$

$$V_F \text{ typ. } 1,15 \text{ V}$$

$$< 1,50 \text{ V}$$

Reverse recovery

$$I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$$

recovery time

$$t_{rr} \text{ typ. } 400 \text{ ns}$$

recovery charge

$$Q_s \text{ typ. } 6 \text{ } \mu\text{C}$$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 4,5 \text{ A}$

$g_{fs} > 2,2 \text{ A/V}$   
 typ. 5 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1500 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 300 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 100 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,8 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 20 ns  
 $t_r$  typ. 60 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 120 ns  
 $t_f$  typ. 60 ns

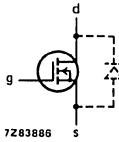


Fig. 2 Diode characteristics.

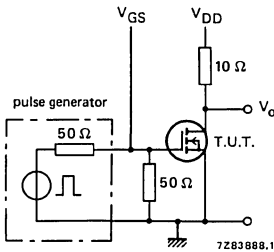


Fig. 3 Switching time test circuit.

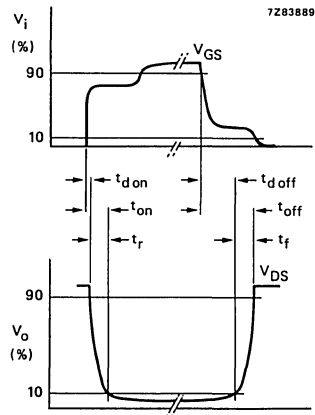


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA



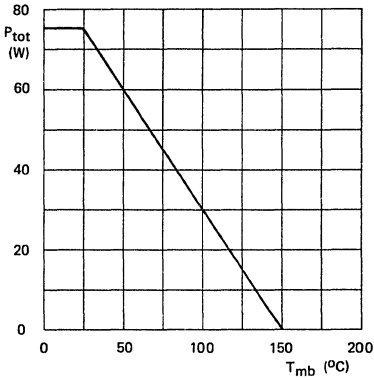


Fig. 5 Power derating curve.

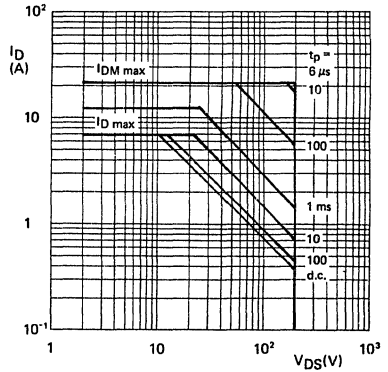


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

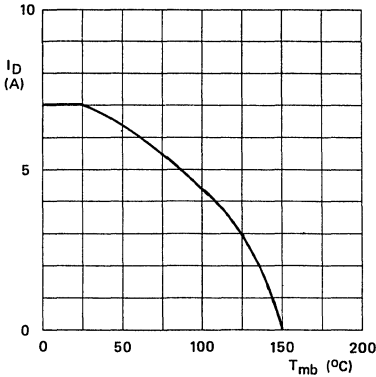


Fig. 7 Drain current as a function of mounting base temperature.

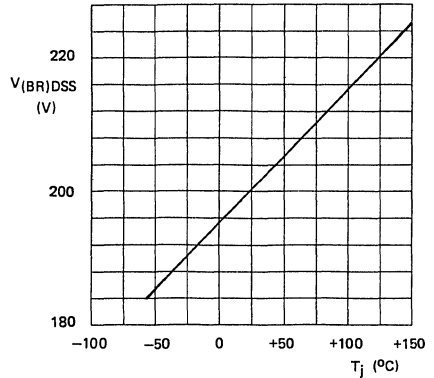


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

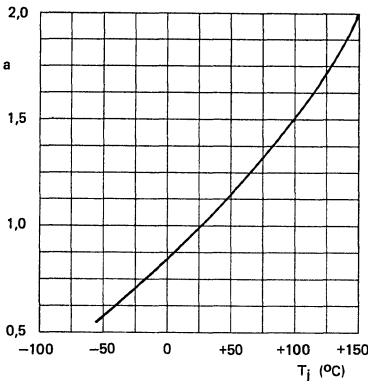


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^\circ\text{C})$ .

# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ31

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

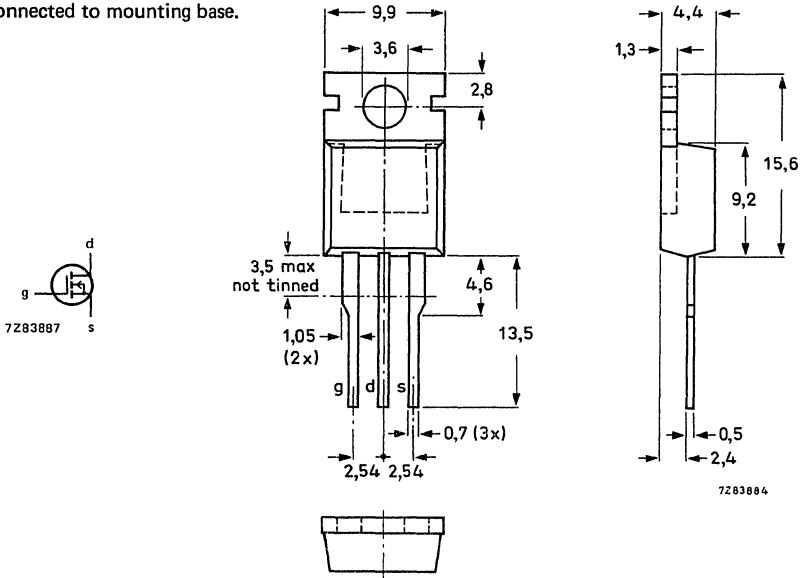
Drain-source voltage	$V_{DS}$	max.	200 V
Drain current (d.c.)	$I_D$	max.	12,5 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,2 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,9\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	60 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	200 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	12,5 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	37 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$   $V_{(BR)DSS} > 200 \text{ V}$

Gate threshold voltage

$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$   $V_{GST} \text{ typ. } 2,1 \text{ to } 4 \text{ V}$

Zero gate voltage drain current

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$   $I_{DSS} < 1 \text{ mA}$

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$   $I_{DSS} < 4 \text{ mA}$

Gate-source leakage current

$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$   $I_{GSS} < 100 \text{ nA}$

Drain-source on-state resistance

$V_{GS} = 10 \text{ V}; I_D = 6 \text{ A}$   $R_{DS \text{ ON}} \text{ typ. } 0,17 \text{ } \Omega$

$< 0,2 \text{ } \Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$I_F < 12,5 \text{ A}$

Forward current (peak value)

$I_{FRM} < 37 \text{ A}$

On-state voltage

$I_F = 2 I_D; V_{GS} = 0 \text{ V}$   $V_F \text{ typ. } 1,4 \text{ V}$

$< 1,8 \text{ V}$

Reverse recovery

$I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$

recovery time

$t_{rr} \text{ typ. } 400 \text{ ns}$

recovery charge

$Q_s \text{ typ. } 6 \text{ } \mu\text{C}$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 6 \text{ A}$

$g_{fs} > \text{typ. } 3 \text{ A/V}$   
 $5 \text{ A/V}$

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is} \text{ typ. } 1000 \text{ pF}$

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os} \text{ typ. } 300 \text{ pF}$

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs} \text{ typ. } 140 \text{ pF}$

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2.9 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}} \text{ typ. } 20 \text{ ns}$   
 $t_r \text{ typ. } 60 \text{ ns}$

turn-off times: delay time  
 fall time

$t_{d \text{ off}} \text{ typ. } 120 \text{ ns}$   
 $t_f \text{ typ. } 60 \text{ ns}$

DEVELOPMENT SAMPLE DATA

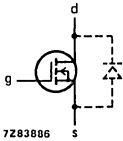


Fig. 2 Diode characteristics.

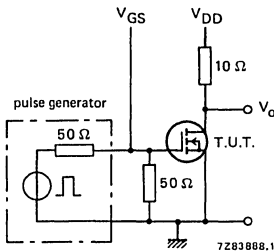


Fig. 3 Switching time test circuit.

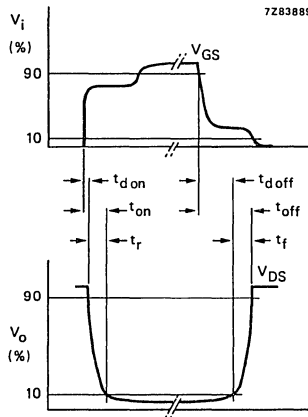


Fig. 4 Switching time waveforms.

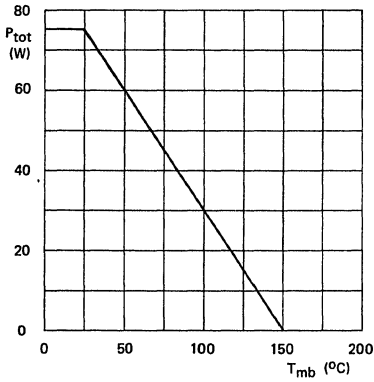


Fig. 5 Power derating curve.

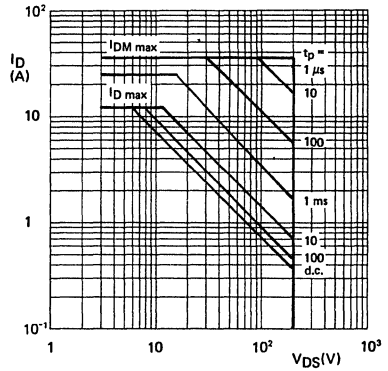


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ °C}; \delta = 0,01.$

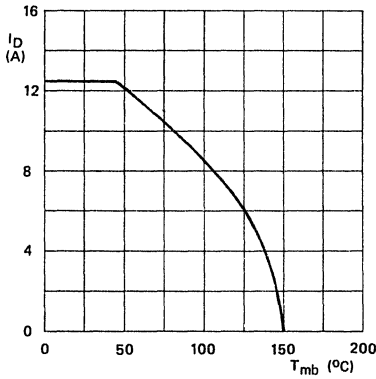


Fig. 7 Drain current as a function of mounting base temperature.

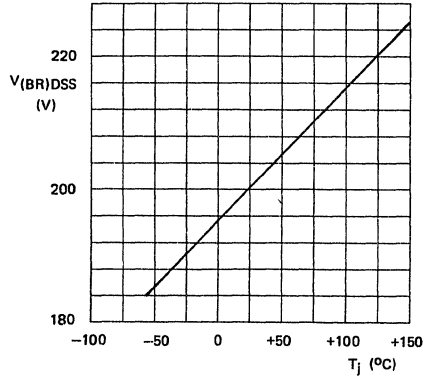


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

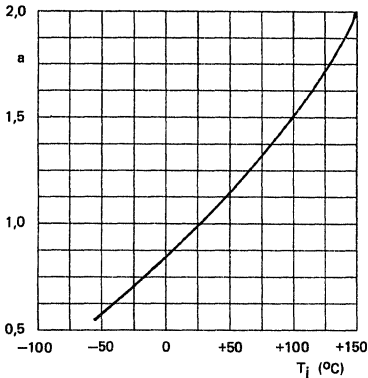


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ °C}).$

# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ32

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

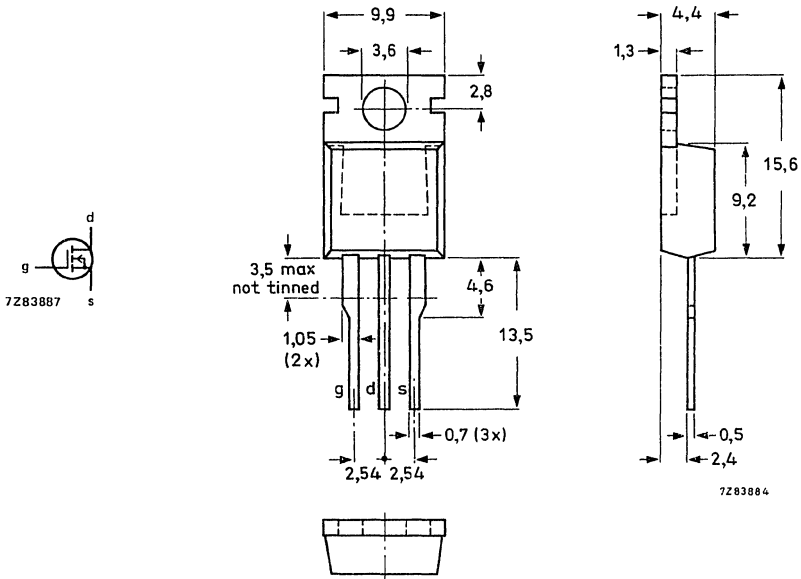
Drain-source voltage	$V_{DS}$	max.	200 V
Drain current (d.c.)	$I_D$	max.	9,5 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,4 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,9\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	60 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	200 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	9,5 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	28 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	200 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$ $I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 4,5 \text{ A}$	$R_{DS \text{ ON}}$	typ. <	0,35 $\Omega$ 0,4 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	9,5 A
Forward current (peak value)	$I_{FRM}$	<	28 A
On-state voltage $I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,3 V 1,7 V
Reverse recovery $I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$ $Q_s$	typ.	400 ns 6 $\mu\text{C}$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance $V_{DS} = 25 \text{ V}; I_D = 4,5 \text{ A}$	$g_{fs}$	>	2,2 A/V
		typ.	5 A/V
Input capacitance at $f = 1 \text{ MHz}$ $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$	$C_{is}$	typ.	1500 pF
Output capacitance at $f = 1 \text{ MHz}$ $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$	$C_{os}$	typ.	300 pF
Feedback capacitance at $f = 1 \text{ MHz}$ $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$	$C_{rs}$	typ.	100 pF
Switching times (see Figs 3 and 4) (between 10% and 90% levels) $V_{DD} = 30 \text{ V}; I_D = 2,9 \text{ A}; V_{GS} = 10 \text{ V}$			
turn-on times: delay time	$t_{d \text{ on}}$	typ.	20 ns
rise time	$t_r$	typ.	60 ns
turn-off times: delay time	$t_{d \text{ off}}$	typ.	120 ns
fall time	$t_f$	typ.	60 ns

DEVELOPMENT SAMPLE DATA

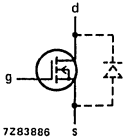


Fig. 2 Diode characteristics.

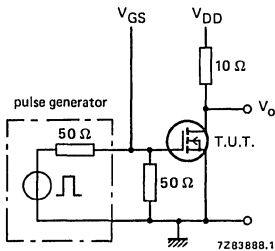


Fig. 3 Switching time test circuit.

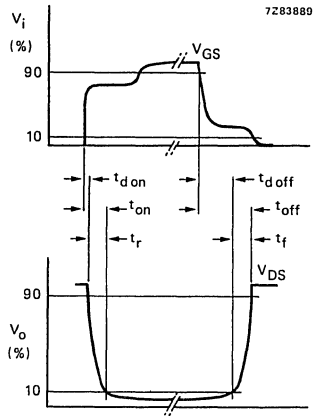


Fig. 4 Switching time waveforms.



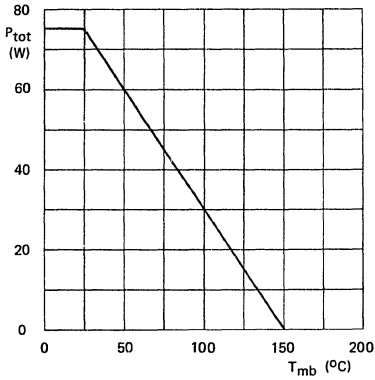


Fig. 5 Power derating curve.

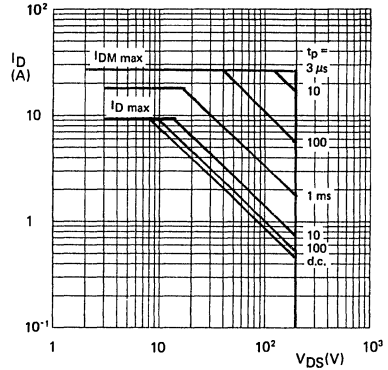


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

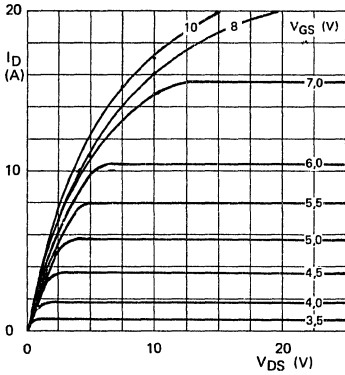


Fig. 7 Output characteristic,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^\circ\text{C}$ .

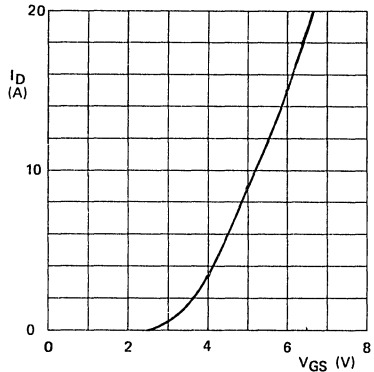


Fig. 8 Typical transfer characteristic  
at  $V_{DS} = 25\text{ V}$ .

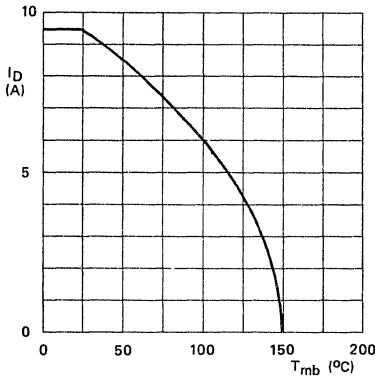


Fig. 9 Drain current as a function  
of mounting base temperature.

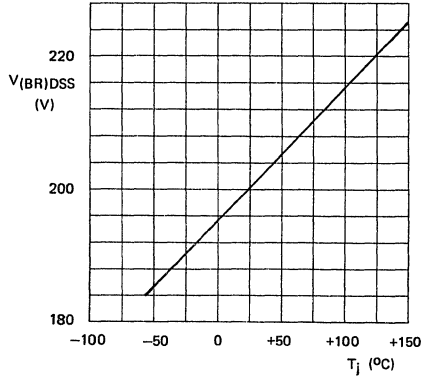


Fig. 10 Drain-source breakdown voltage  
as a function of junction temperature.

DEVELOPMENT SAMPLE DATA

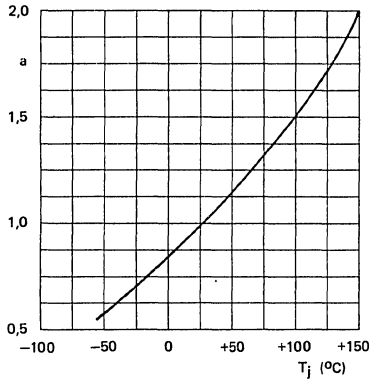


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25^\circ\text{C})$ .

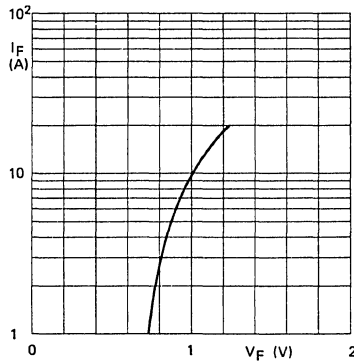


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu\text{s}$ ;  $T_j = 25^\circ\text{C}$ .

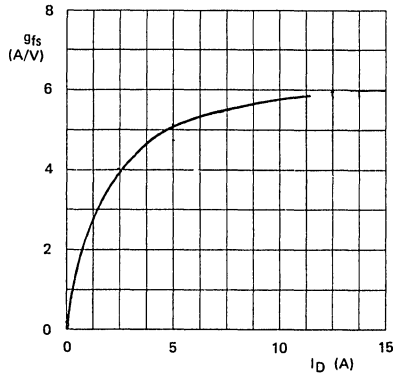
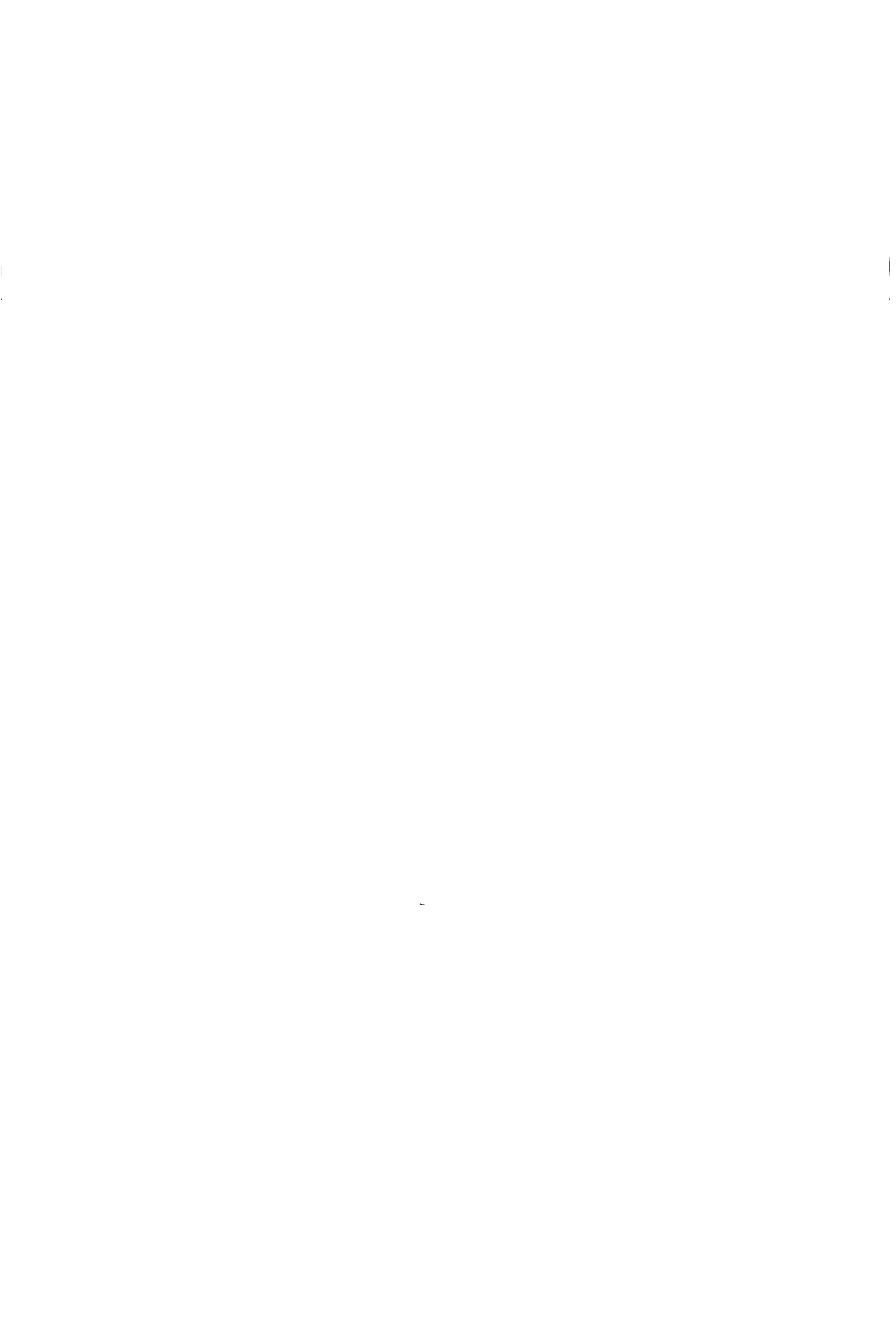


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ \text{V}$ ;  $T_j = 25^\circ\text{C}$ .



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ33

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

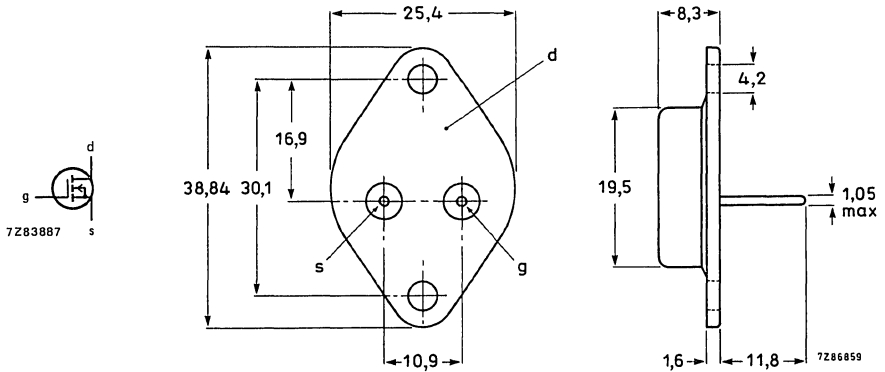
Drain-source voltage	$V_{DS}$	max.	200 V
Drain current (d.c.)	$I_D$	max.	7,2 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	78 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,75 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,8\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	60 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	200 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	7,2 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	21 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$   $V_{(BR)DSS} > 200 \text{ V}$

Gate threshold voltage

$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$   $V_{GST} \begin{matrix} 2,1 \text{ to } 4 \text{ V} \\ \text{typ. } 3 \text{ V} \end{matrix}$

Zero gate voltage drain current

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$   $I_{DSS} < 1 \text{ mA}$   
 $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$   $I_{DSS} < 4 \text{ mA}$

Gate-source leakage current

$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$   $I_{GSS} < 100 \text{ nA}$

Drain-source on-state resistance

$V_{GS} = 10 \text{ V}; I_D = 4,5 \text{ A}$   $R_{DS \text{ ON}} \begin{matrix} \text{typ. } 0,5 \text{ } \Omega \\ < 0,75 \text{ } \Omega \end{matrix}$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$I_F < 7,2 \text{ A}$

Forward current (peak value)

$I_{FRM} < 21 \text{ A}$

On-state voltage

$I_F = 2 I_D; V_{GS} = 0 \text{ V}$   $V_F \begin{matrix} \text{typ. } 1,15 \text{ V} \\ < 1,5 \text{ V} \end{matrix}$

Reverse recovery

$I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$

recovery time	$t_{rr}$	typ.	400 ns
recovery charge	$Q_s$	typ.	6 $\mu\text{C}$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 4,5 \text{ A}$

$g_{fs} > \text{typ. } \begin{matrix} 2,2 \text{ A/V} \\ 5 \text{ A/V} \end{matrix}$

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is} \text{ typ. } 1500 \text{ pF}$

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os} \text{ typ. } 300 \text{ pF}$

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs} \text{ typ. } 100 \text{ pF}$

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,8 \text{ A}; V_{GS} = 10 \text{ V}$

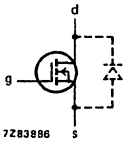
turn-on times: delay time  
 rise time

$t_{d \text{ on}} \text{ typ. } 20 \text{ ns}$   
 $t_r \text{ typ. } 60 \text{ ns}$

turn-off times: delay time  
 fall time

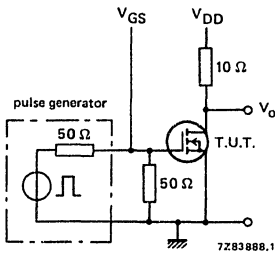
$t_{d \text{ off}} \text{ typ. } 120 \text{ ns}$   
 $t_f \text{ typ. } 60 \text{ ns}$

DEVELOPMENT SAMPLE DATA



7Z83886

Fig. 2 Diode characteristics.



7Z83888.1

Fig. 3 Switching time test circuit.

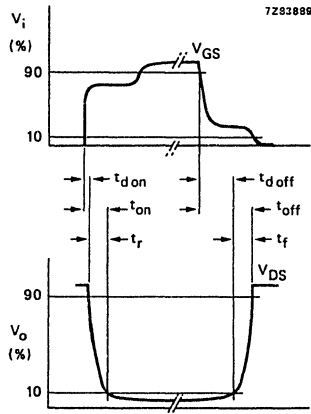


Fig. 4 Switching time waveforms.

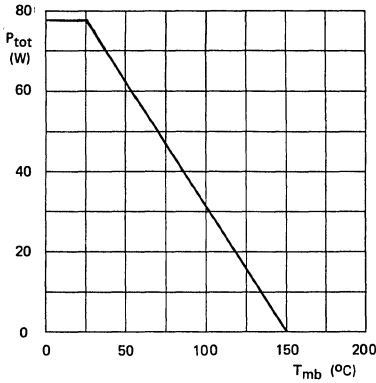


Fig. 5 Power derating curve.

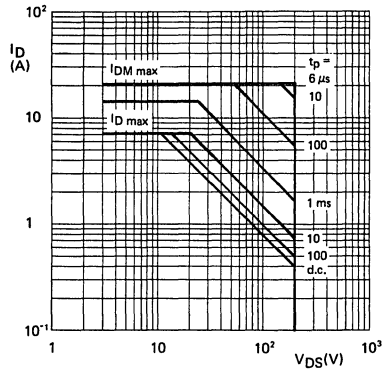


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

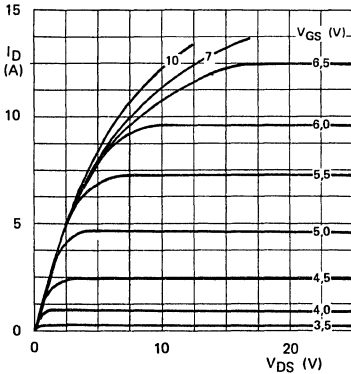


Fig. 7 Output characteristic,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^{\circ}\text{C}$ .

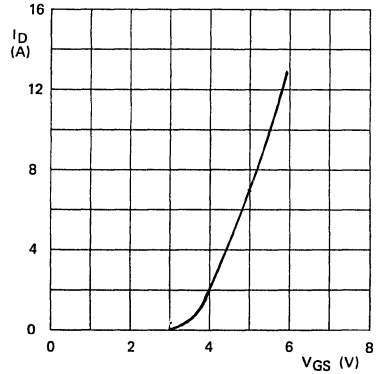


Fig. 8 Typical transfer characteristic  
 at  $V_{DS} = 25\text{ V}$ .

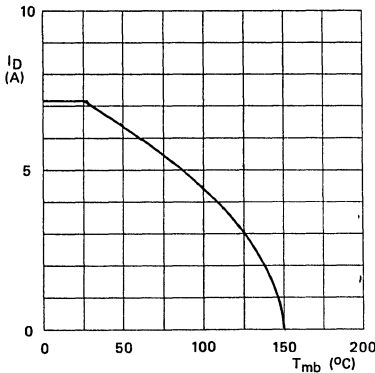


Fig. 9 Drain current as a function  
 of mounting base temperature.

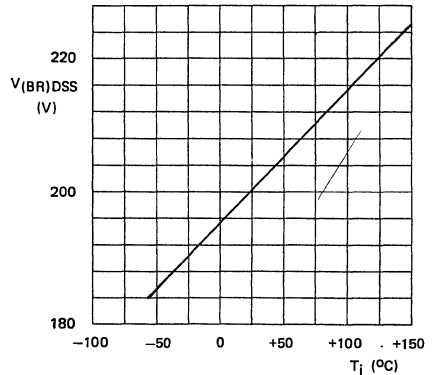


Fig. 10 Drain-source breakdown voltage  
 as a function of junction temperature.

DEVELOPMENT SAMPLE DATA

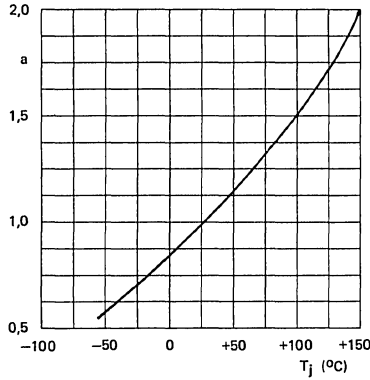


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ\text{C})$ .

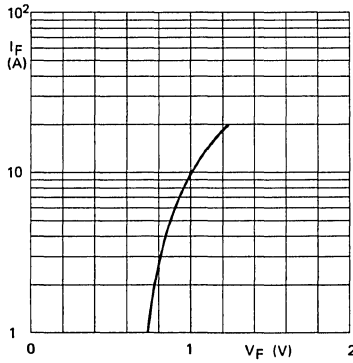


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu\text{s}$ ;  $T_j = 25\ ^\circ\text{C}$ .

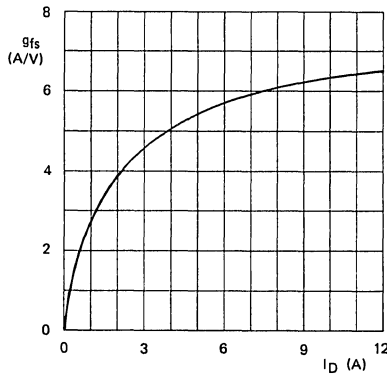


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ \text{V}$ ;  $T_j = 25\ ^\circ\text{C}$ .





## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ34

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

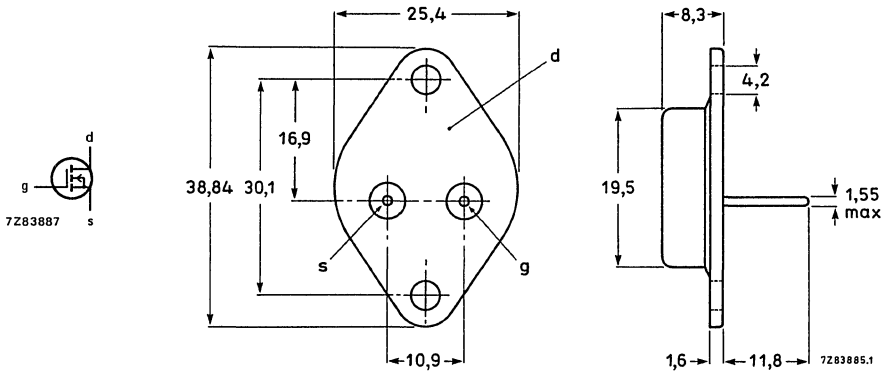
Drain-source voltage	$V_{DS}$	max.	200 V
Drain current (d.c.)	$I_D$	max.	17 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,2 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,9\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	200 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	$V_{DGR}$	max.	200 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 30\text{ }^\circ\text{C}$	$I_D$	max.	17 A
Drain current (pulse peak value); $T_{mb} = 30\text{ }^\circ\text{C}$	$I_{DM}$	max.	50 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th\ j-mb}$	=	1,0 K/W
From junction to ambient	$R_{th\ j-a}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0\text{ V}; I_D = 1\text{ mA}$	$V_{(BR)DSS}$	>	200 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10\text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3,0 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25\text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125\text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20\text{ V}; V_{DS} = 0\text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10\text{ V}; I_D = 44\text{ A}$	$R_{DS\ ON}$	typ. <	0,17 $\Omega$ 0,2 $\Omega$

**Diode characteristics**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	17 A
Forward current (peak value)	$I_{FRM}$	<	50 A
On-state voltage $I_F = 2\text{ }I_D; V_{GS} = 0\text{ V}$	$V_F$	typ. <	1,15 V 1,55 V
Reverse recovery $I_F = 2\text{ }I_D; dI_F/dt = 100\text{ A}/\mu\text{s}$	$t_{rr}$	typ.	400 ns
recovery time	$Q_s$	typ.	6 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 44 \text{ A}$

$g_{fs}$  > 3 A/V  
 typ. 5 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1500 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 900 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 500 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,9 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 50 ns  
 $t_r$  typ. 200 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 300 ns  
 $t_f$  typ. 200 ns

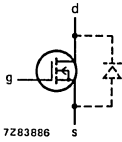


Fig. 2 Diode characteristics.

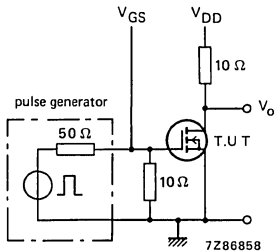


Fig. 3 Switching time test circuit.

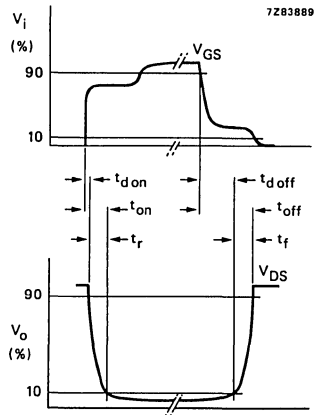


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA



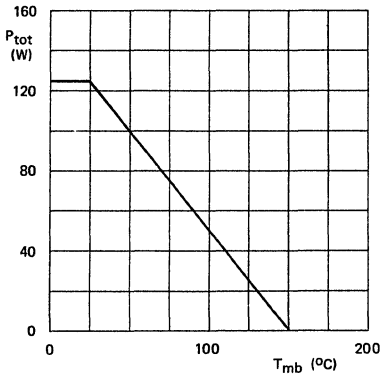


Fig. 5 Power derating curve.

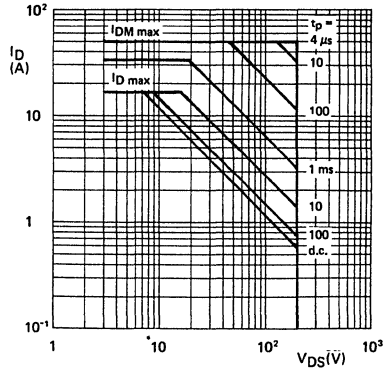


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

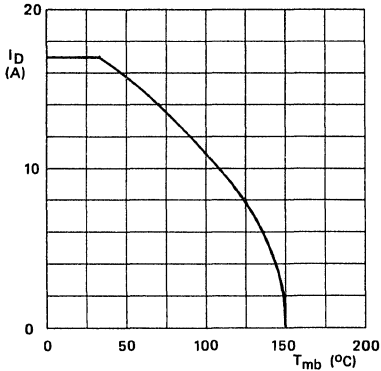


Fig. 7 Drain current as a function of mounting base temperature.

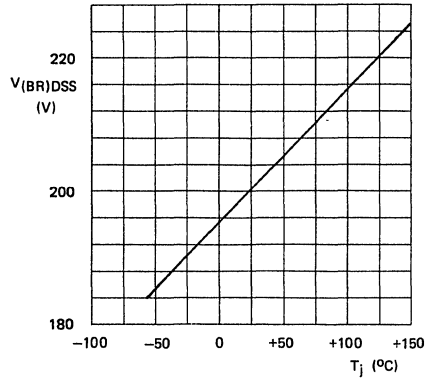


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

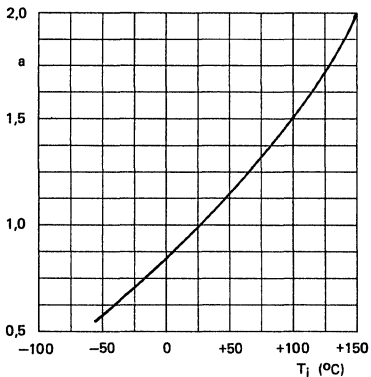


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^\circ\text{C})$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ35

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

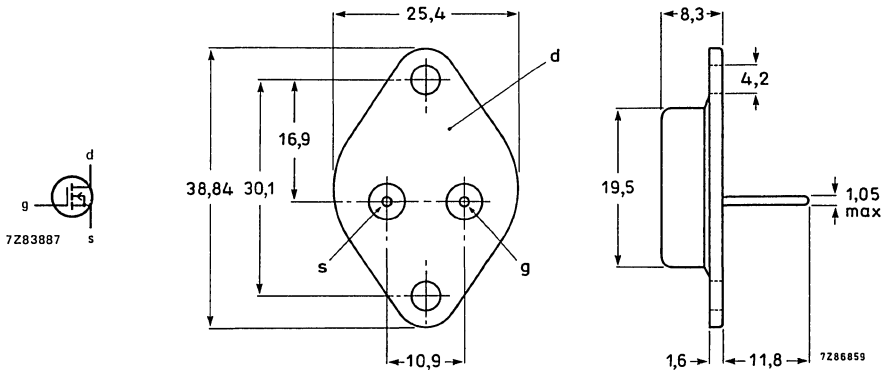
Drain-source voltage	$V_{DS}$	max.	200 V
Drain current (d.c.)	$I_D$	max.	9,9 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	78 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,4 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,9\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	60 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	200 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	9,9 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	29 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	200 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 4,5 \text{ A}$	$R_{DS \text{ ON}}$	typ. <	0,35 $\Omega$ 0,4 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	9,9 A
Forward current (peak value)	$I_{FRM}$	<	29 A
On-state voltage $I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,3 V 1,7 V
Reverse recovery $I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	400 ns
recovery time	$Q_s$	typ.	6 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 4,5 \text{ A}$

$g_{fs}$	>	2,2 A/V
	typ.	5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	1500 pF
----------	------	---------

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	300 pF
----------	------	--------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	100 pF
----------	------	--------

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,9 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	20 ns
--------------------	------	-------

rise time

$t_r$	typ.	60 ns
-------	------	-------

turn-off times: delay time

$t_{d \text{ off}}$	typ.	120 ns
---------------------	------	--------

fall time

$t_f$	typ.	60 ns
-------	------	-------

DEVELOPMENT SAMPLE DATA

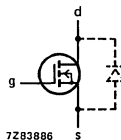


Fig. 2 Diode characteristics.

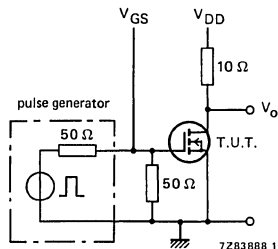


Fig. 3 Switching time test circuit.

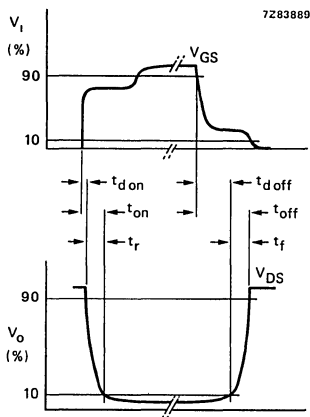


Fig. 4 Switching time waveforms.



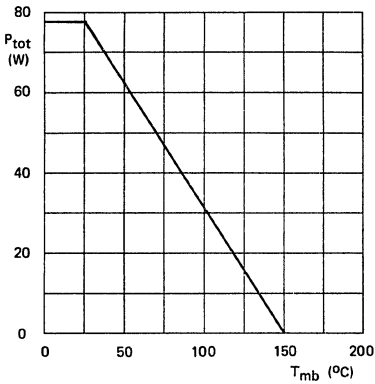


Fig. 5 Power derating curve.

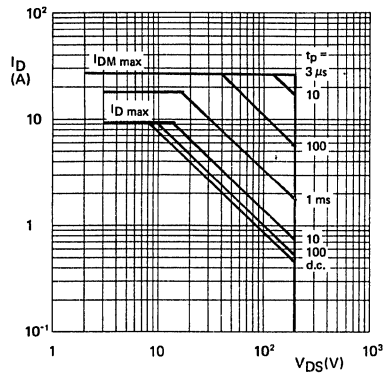


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

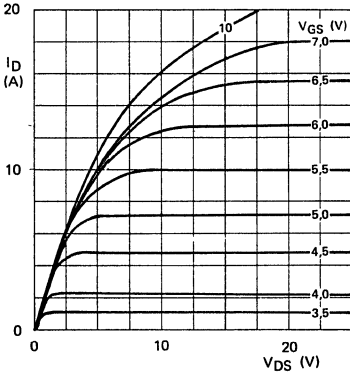


Fig. 7 Output characteristic,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^{\circ}\text{C}$ .

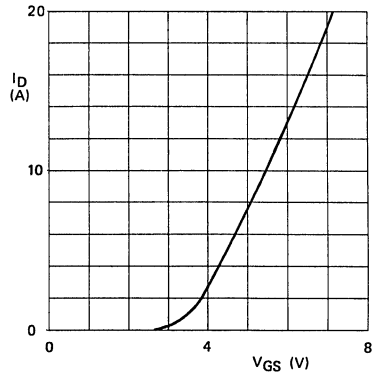


Fig. 8 Typical transfer characteristic  
 at  $V_{DS} = 25\text{ V}$ .

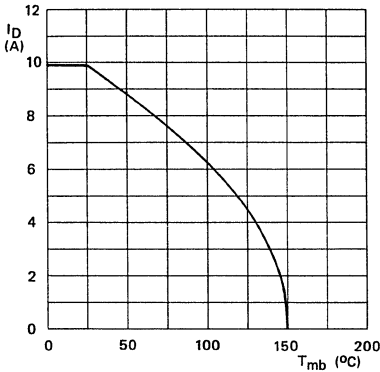


Fig. 9 Drain current as a function  
 of mounting base temperature.

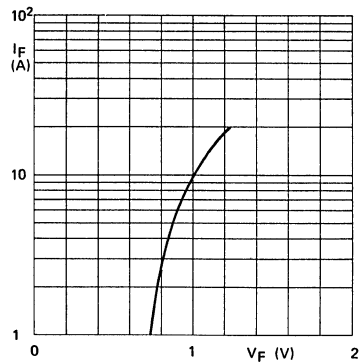


Fig. 10 Diode forward current as a function  
 of forward voltage.  $t_p = 80\text{ }\mu\text{s}$ ;  $T_j = 25\text{ }^{\circ}\text{C}$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ36

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

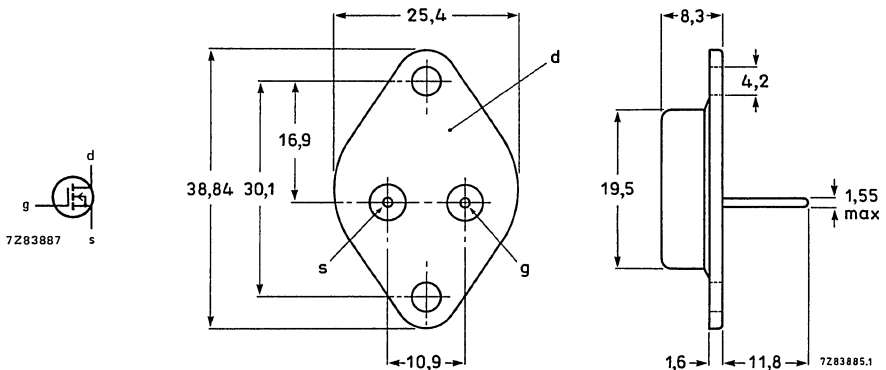
Drain-source voltage	$V_{DS}$	max.	200 V
Drain current (d.c.)	$I_D$	max.	22 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,12 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = \text{A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	200 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	200 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 30 \text{ }^\circ\text{C}$	$I_D$	max.	22 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	65 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,0 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	200 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 11 \text{ A}$	$R_{DS \text{ ON}}$	<	0,12 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	22 A
Forward current (peak value)	$I_{FRM}$	<	65 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,2 V 1,7 V
Reverse recovery $I_F = 2 I_D; DI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	400 ns
recovery time	$Q_s$	typ.	6 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 11 \text{ A}$

$g_{fs}$	>	9 A/V
	typ.	13 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	1500 pF
----------	------	---------

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	900 pF
----------	------	--------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	500 pF
----------	------	--------

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	50 ns
--------------------	------	-------

rise time

$t_r$	typ.	200 ns
-------	------	--------

turn-off times: delay time

$t_{d \text{ off}}$	typ.	300 ns
---------------------	------	--------

fall time

$t_f$	typ.	200 ns
-------	------	--------

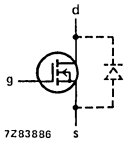


Fig. 2 Diode characteristics.

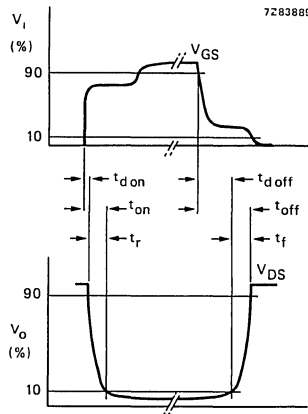


Fig. 4 Switching time waveforms.

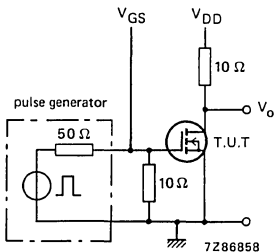


Fig. 3 Switching time test circuit.

DEVELOPMENT SAMPLE DATA

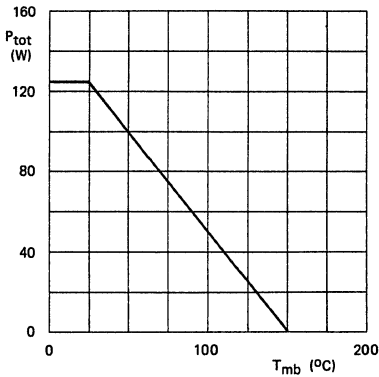


Fig. 5 Power derating curve.

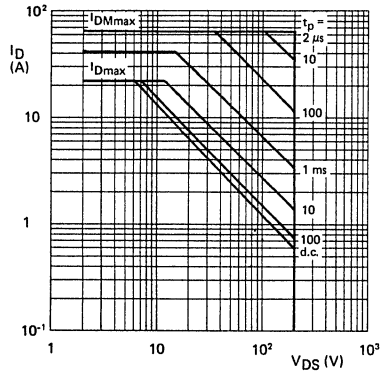


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

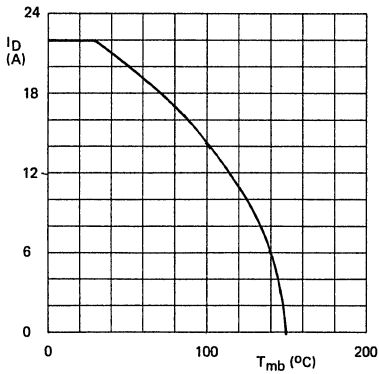


Fig. 7 Drain current as a function of mounting base temperature.

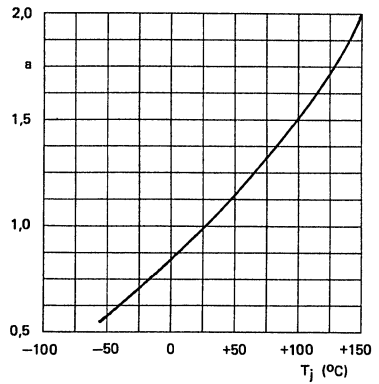


Fig. 8  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^\circ\text{C})$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ40

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

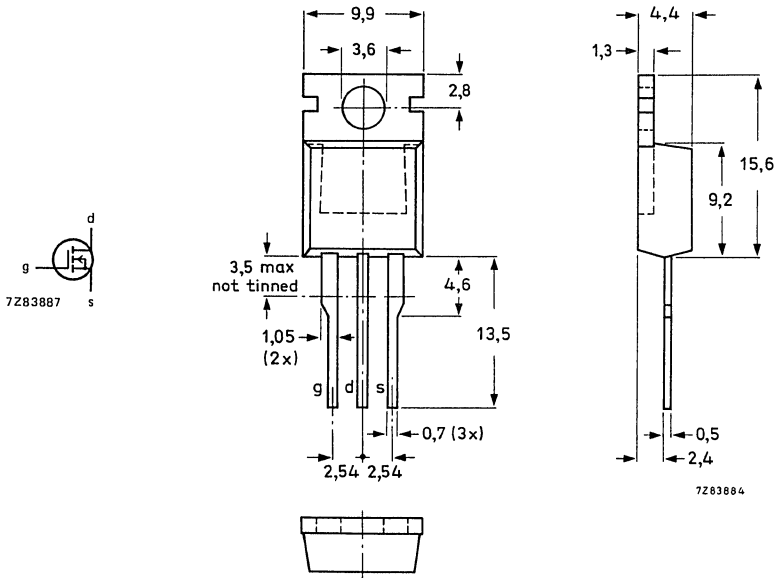
Drain-source voltage	$V_{DS}$	max.	500 V
Drain current (d.c.)	$I_D$	max.	2,5 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	4,5 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,1\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	500 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	500 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 45 \text{ }^\circ\text{C}$	$I_D$	max.	2,5 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	7,5 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

## THERMAL CHARACTERISTICS

### Thermal resistance

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

## STATIC CHARACTERISTICS

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$$

$$V_{(BR)DSS} > 500 \text{ V}$$

Gate threshold voltage

$$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$$

$$V_{GST} \text{ typ. } 2,1 \text{ to } 4 \text{ V}$$

Zero gate voltage drain current

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$$

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$$

$$I_{DSS} < 1 \text{ mA}$$

$$I_{DSS} < 4 \text{ mA}$$

Gate-source leakage current

$$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$$

$$I_{GSS} < 100 \text{ nA}$$

Drain-source on-state resistance

$$V_{GS} = 10 \text{ V}; I_D = 2,5 \text{ A}$$

$$R_{DS \text{ ON}} \text{ typ. } 3,0 \text{ } \Omega$$

$$R_{DS \text{ ON}} < 4,5 \text{ } \Omega$$

## Diode characteristics

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$$I_F < 2,5 \text{ A}$$

Forward current (peak value)

$$I_{FRM} < 7,5 \text{ A}$$

On-state voltage

$$I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$$

$$V_F \text{ typ. } 1,0 \text{ V}$$

$$V_F < 1,3 \text{ V}$$

Reverse recovery

$$I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$$

recovery time

$$t_{rr} \text{ typ. } 1200 \text{ ns}$$

recovery charge

$$Q_s \text{ typ. } 6 \text{ } \mu\text{C}$$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs}$  > 1,5 A/V  
 typ. 2,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1600 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 90 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 30 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,1 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 30 ns  
 $t_r$  typ. 70 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 160 ns  
 $t_f$  typ. 100 ns

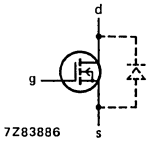


Fig. 2 Diode characteristics.

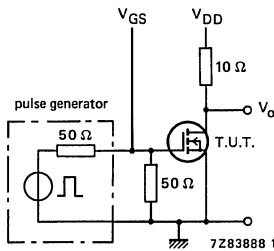


Fig. 3 Switching time test circuit.

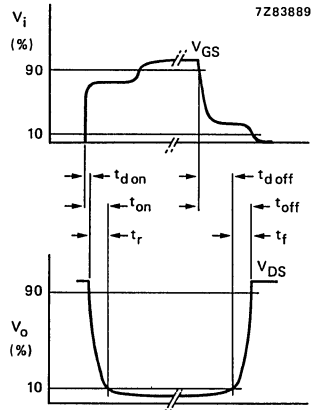


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA





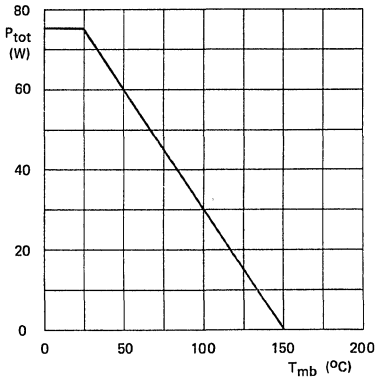


Fig. 5 Power derating curve.

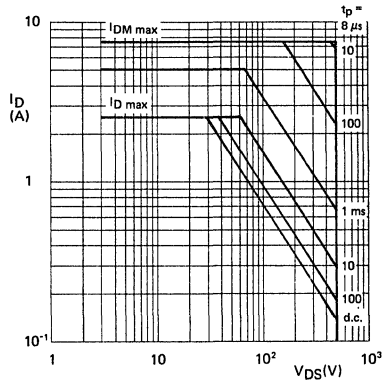


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

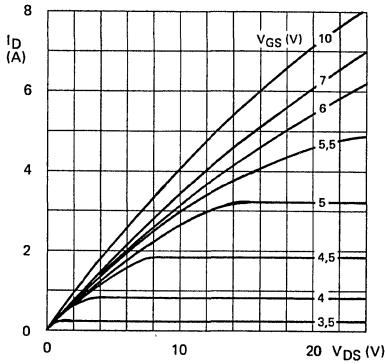


Fig. 7 Output characteristics,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^\circ\text{C}$ .

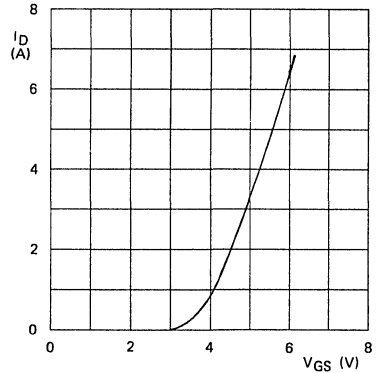


Fig. 8 Typical transfer characteristic  
at  $V_{DS} = 25\text{ V}$ .

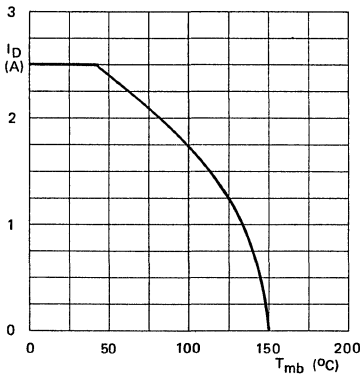


Fig. 9 Drain current as a function  
of mounting base temperature.

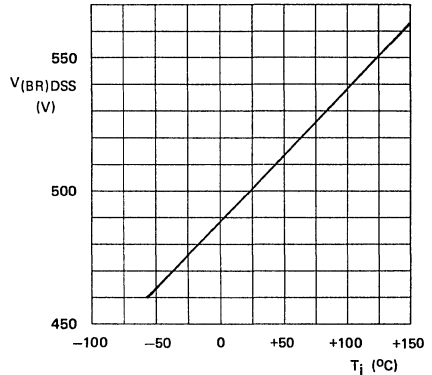


Fig. 10 Drain-source breakdown voltage  
as a function of junction temperature.

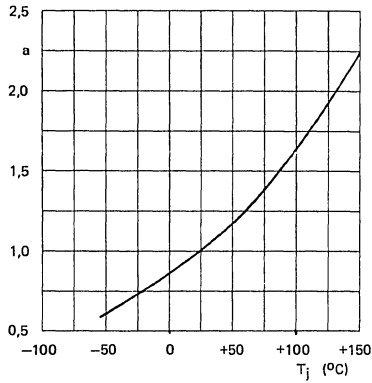


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ C)$ .

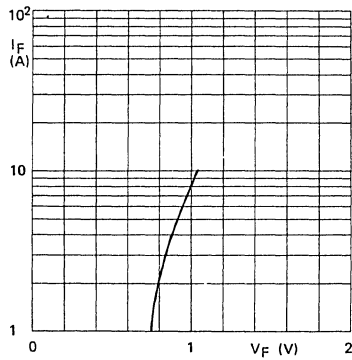


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu s$ ;  $T_j = 25\ ^\circ C$ .

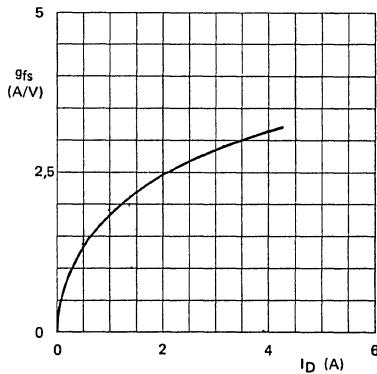


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ V$ ;  $T_j = 25\ ^\circ C$ .



# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ41A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

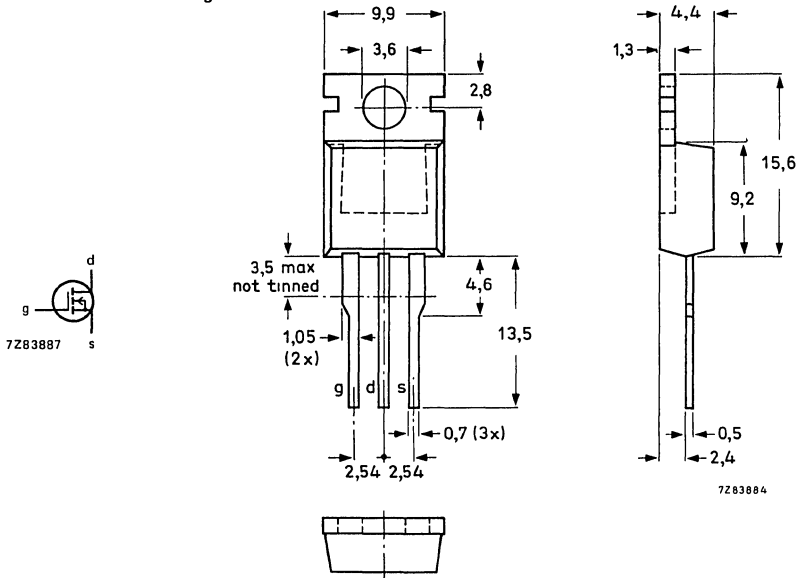
Drain-source voltage	$V_{DS}$	max.	500 V
Drain current (d.c.)	$I_D$	max.	4,5 A
Total power dissipation	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	1,5 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,6\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	500 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	500 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 35 \text{ }^\circ\text{C}$	$I_D$	max.	4,5 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	13 A
Total power dissipation	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

## THERMAL CHARACTERISTICS

### Thermal resistance

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

## STATIC CHARACTERISTICS

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	500 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 2,5 \text{ A}$	$R_{DS \text{ ON}}$	typ. <	1,4 $\Omega$ 1,5 $\Omega$

## Diode characteristics

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	4,5 A
Forward current (peak value)	$I_{FRM}$	<	13 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,1 V 1,5 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$	$t_{rr}$	typ.	1200 ns
recovery time	$Q_s$	typ.	6 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs} > 1,5 \text{ A/V}$   
 typ. 2,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1600 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 90 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 30 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,6 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time  
 turn-off times: delay time  
 fall time

$t_{d \text{ on}}$  typ. 30 ns  
 $t_r$  typ. 70 ns  
 $t_{d \text{ off}}$  typ. 160 ns  
 $t_f$  typ. 100 ns

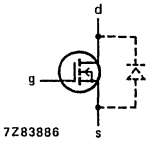


Fig. 2 Diode characteristics.

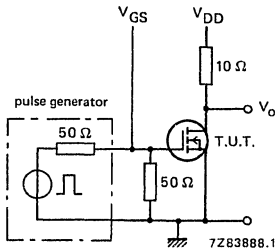


Fig. 3 Switching time test circuit.

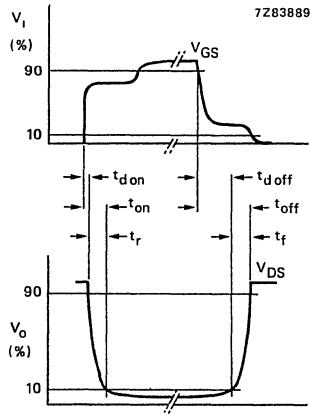


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

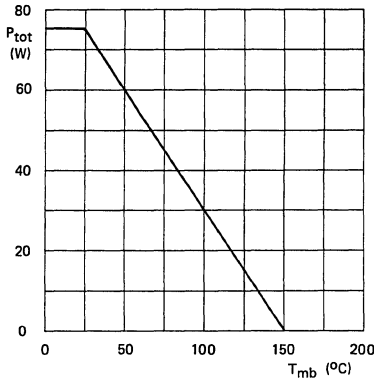


Fig. 5 Power derating curve.

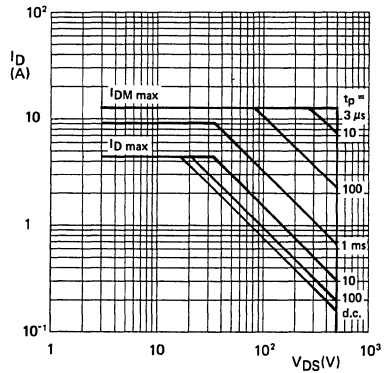


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

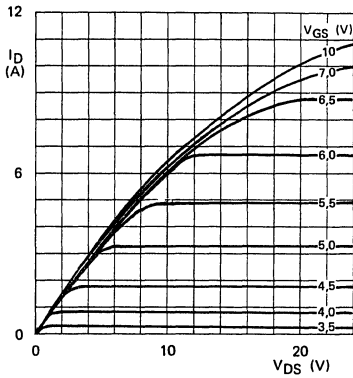


Fig. 7 Output characteristic,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^\circ\text{C}$ .

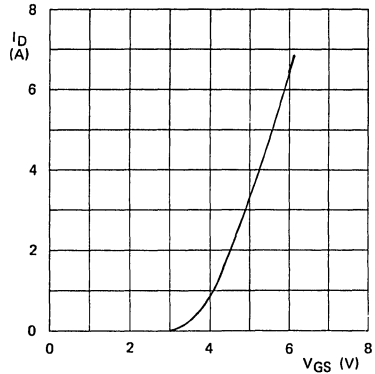


Fig. 8 Typical transfer characteristic  
 at  $V_{DS} = 25\text{ V}$ .

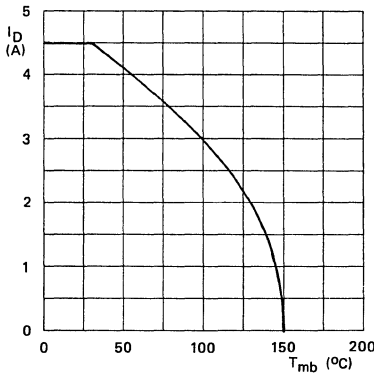


Fig. 9 Drain current as a function  
 of mounting base temperature.

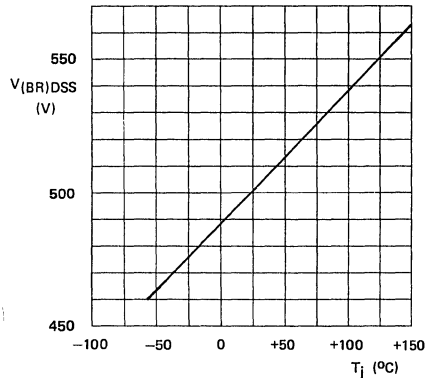


Fig. 10 Drain-source breakdown voltage  
 as a function of junction temperature.

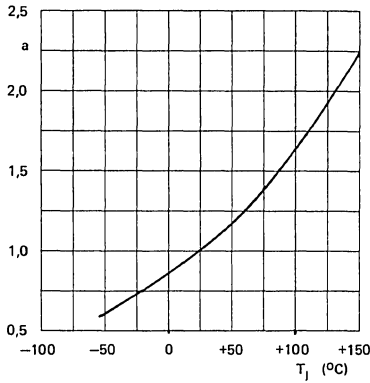


Fig. 11  $R_{DS\ ON}(T_J) = a \times R_{DS\ ON}(25\ ^\circ\text{C})$ .

DEVELOPMENT SAMPLE DATA

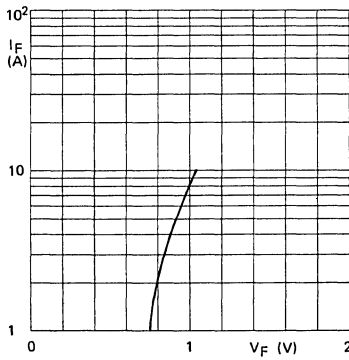


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu\text{s}$ ;  $T_j = 25\ ^\circ\text{C}$ .

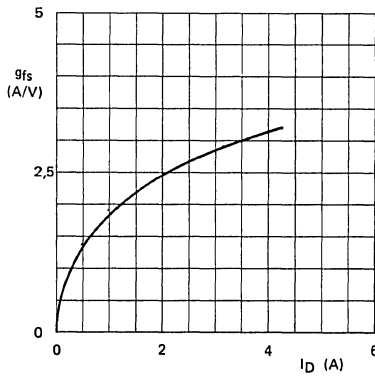


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ \text{V}$ ;  $T_j = 25\ ^\circ\text{C}$ .





# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ42

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

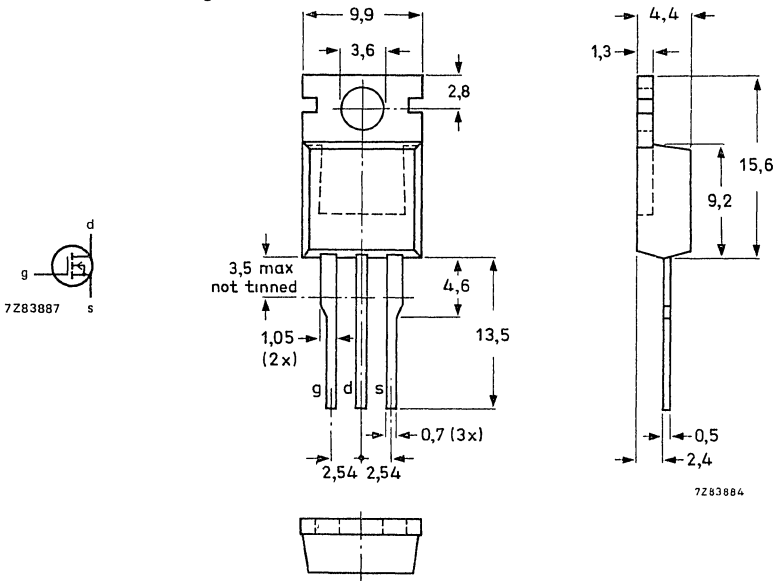
Drain-source voltage	$V_{DS}$	max.	500 V
Drain current (d.c.)	$I_D$	max.	4 A
Total power dissipation	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS ON}$	<	2,0 $\Omega$
Turn-off fall-time $V_{DD} = 30 V; I_D = 2,5 A; V_{GS} = 10 V$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	500 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	500 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 30 \text{ }^\circ\text{C}$	$I_D$	max.	4 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	12 A
Total power dissipation	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

## THERMAL CHARACTERISTICS

### Thermal resistance

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

## STATIC CHARACTERISTICS

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$$

$$V_{(BR)DSS} > 500 \text{ V}$$

Gate threshold voltage

$$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$$

$$V_{GST} \text{ typ. } 2,1 \text{ to } 4 \text{ V}$$

$$3,0 \text{ V}$$

Zero gate voltage drain current

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$$

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$$

$$I_{DSS} < 1 \text{ mA}$$

$$I_{DSS} < 4 \text{ mA}$$

Gate-source leakage current

$$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$$

$$I_{GSS} < 100 \text{ nA}$$

Drain-source on-state resistance

$$V_{GS} = 10 \text{ V}; I_D = 2,5 \text{ A}$$

$$R_{DS \text{ ON}} \text{ typ. } 1,8 \text{ } \Omega$$

$$< 2,0 \text{ } \Omega$$

## Diode characteristics

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$$I_F < 4 \text{ A}$$

Forward current (peak value)

$$I_{FRM} < 12 \text{ A}$$

On-state voltage

$$I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$$

$$V_F \text{ typ. } 1,1 \text{ V}$$

$$< 1,5 \text{ V}$$

Reverse recovery

$$I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$$

recovery time

$$t_{rr} \text{ typ. } 1200 \text{ ns}$$

recovery charge

$$Q_s \text{ typ. } 6 \text{ } \mu\text{C}$$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs}$	>	1,5 A/V
	typ.	2,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	1600 pF
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Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	90 pF
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Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	30 pF
----------	------	-------

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,5 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	30 ns
--------------------	------	-------

rise time

$t_r$	typ.	70 ns
-------	------	-------

turn-off times: delay time

$t_{d \text{ off}}$	typ.	160 ns
---------------------	------	--------

fall time

$t_f$	typ.	100 ns
-------	------	--------

DEVELOPMENT SAMPLE DATA

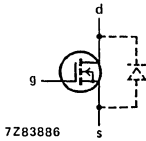


Fig. 2 Diode characteristics.

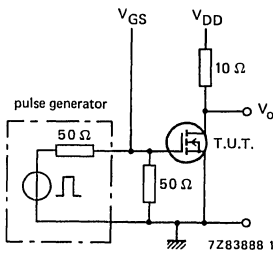


Fig. 3 Switching time test circuit.

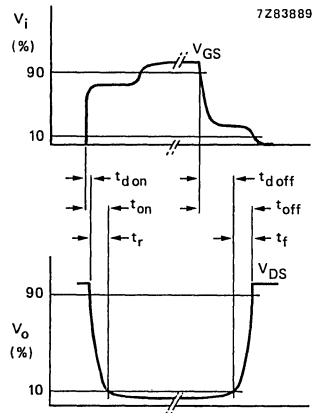


Fig. 4 Switching time waveforms.

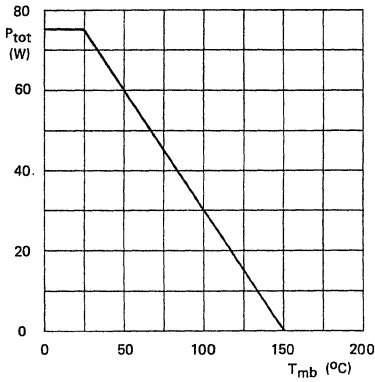


Fig. 5 Power derating curve.

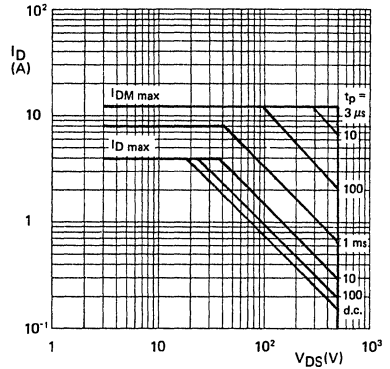


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

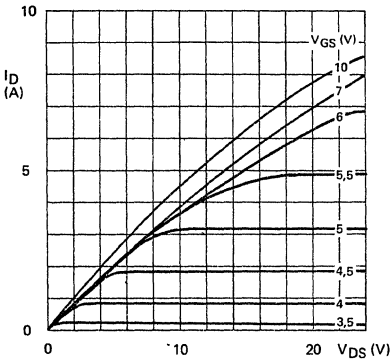


Fig. 7 Output characteristic,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^{\circ}\text{C}$ .

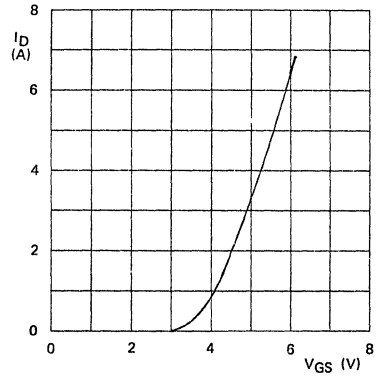


Fig. 8 Typical transfer characteristic  
at  $V_{DS} = 25\text{ V}$ .

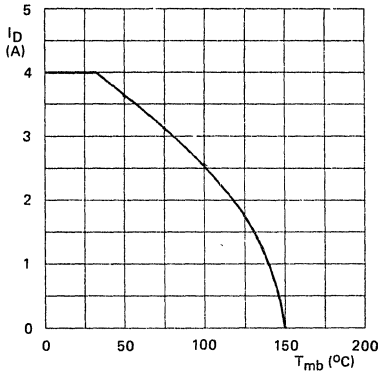


Fig. 9 Drain current as a function  
of mounting base temperature.

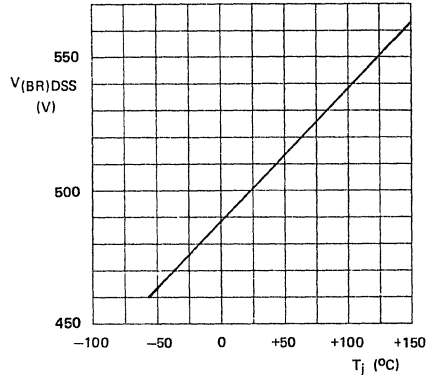


Fig. 10 Drain-source breakdown voltage  
as a function of junction temperature.

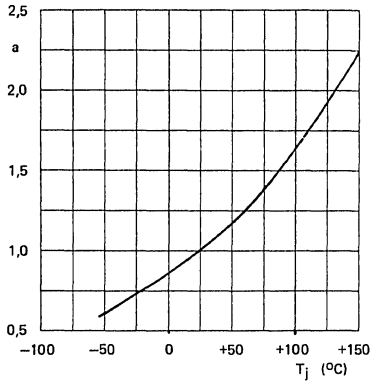


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ C)$ .

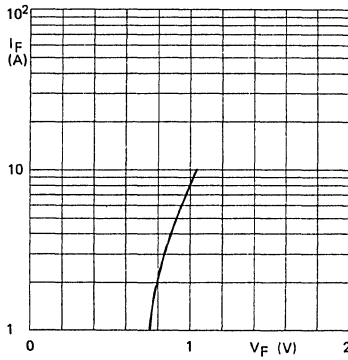


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu s$ ;  $T_j = 25\ ^\circ C$ .

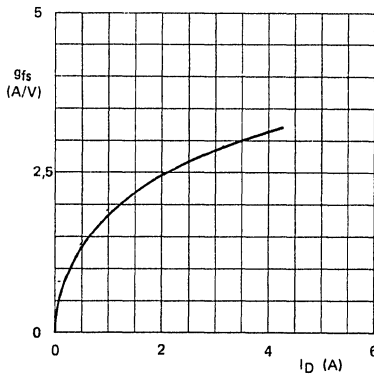
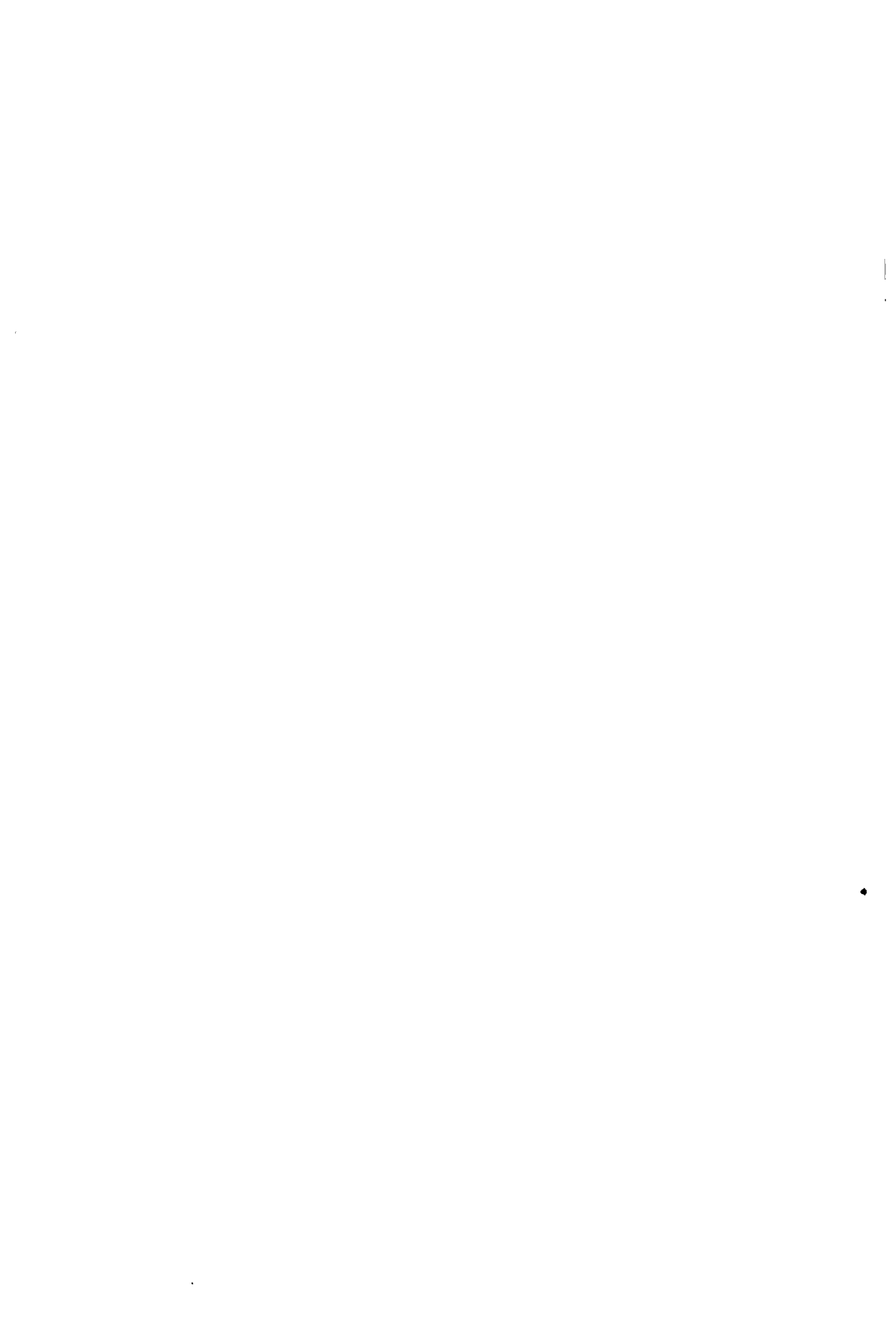


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ V$ ;  $T_j = 25\ ^\circ C$ .



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ43

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

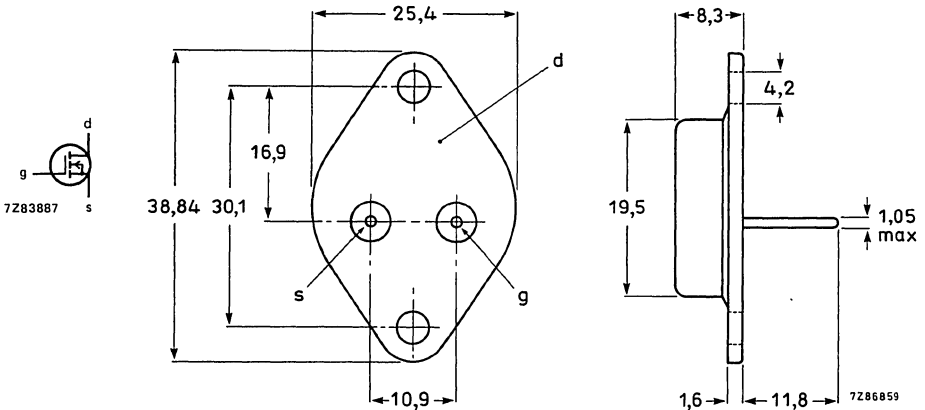
Drain-source voltage	$V_{DS}$	max.	500 V
Drain current (d.c.)	$I_D$	max.	2,8 A
Total power dissipation	$P_{tot}$	max.	78 W
Drain-source resistance (on)	$R_{DS ON}$	<	4,5 $\Omega$
Turn-off fall-time $V_{DD} = 30 V; I_D = 2,1 A; V_{GS} = 10 V$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	500 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	500 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	2,8 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	8,0 A
Total power dissipation	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	500 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 2,5 \text{ A}$	$R_{DS \text{ ON}}$	typ. <	3 $\Omega$ 4,5 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	2,8 A
Forward current (peak value)	$I_{FRM}$	<	8,0 A
On-state voltage $I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,05 V 1,3 V
Reverse recovery $I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1200 ns
recovery time	$Q_s$	typ.	6,0 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs} > 1,5 \text{ A/V}$   
 typ.  $2,5 \text{ A/V}$

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ.  $1600 \text{ pF}$

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{Os}$  typ.  $90 \text{ pF}$

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ.  $30 \text{ pF}$

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,1 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time  
 turn-off times: delay time  
 fall time

$t_{d \text{ on}}$  typ.  $30 \text{ ns}$   
 $t_r$  typ.  $70 \text{ ns}$   
 $t_{d \text{ off}}$  typ.  $160 \text{ ns}$   
 $t_f$  typ.  $100 \text{ ns}$

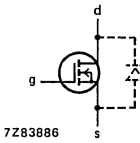


Fig. 2 Diode characteristics.

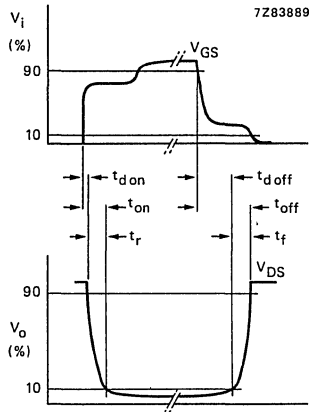


Fig. 4 Switching time waveforms.

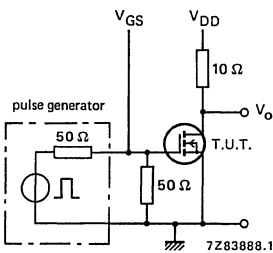


Fig. 3 Switching time test circuit.

DEVELOPMENT SAMPLE DATA



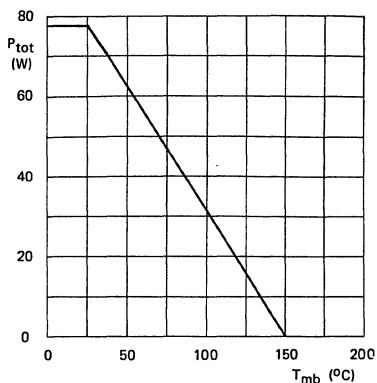


Fig. 5 Power derating curve.

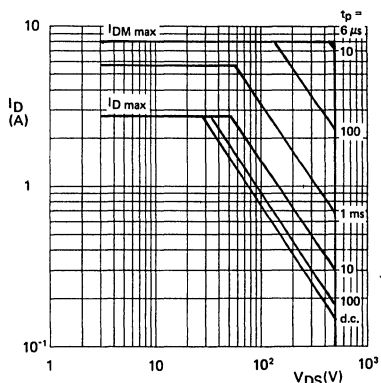


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

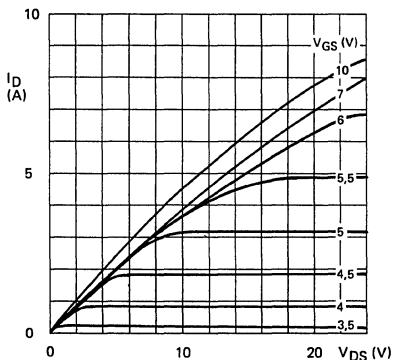


Fig. 7 Output characteristic,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^{\circ}\text{C}$ .

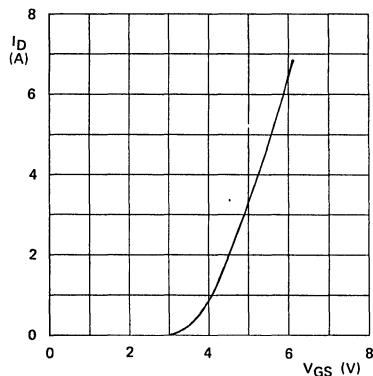


Fig. 8 Typical transfer characteristic  
 at  $V_{DS} = 25\text{ V}$ .

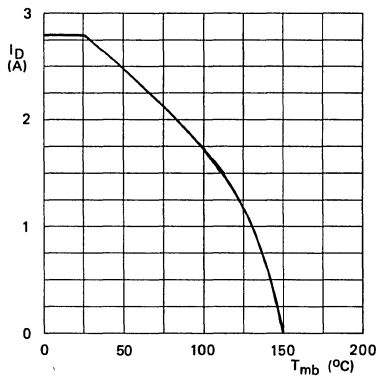


Fig. 9 Drain current as a function  
 of mounting base temperature.

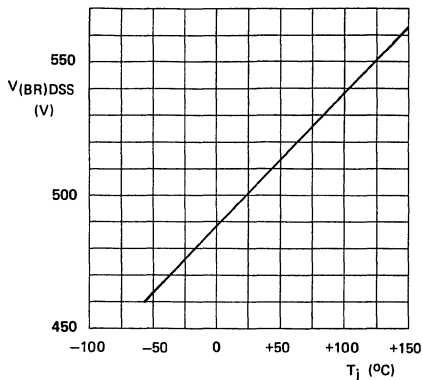


Fig. 10 Drain-source breakdown voltage  
 as a function of junction temperature.

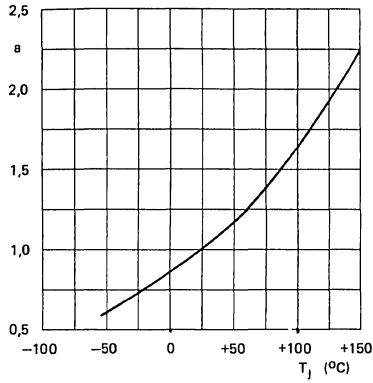


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ C)$ .

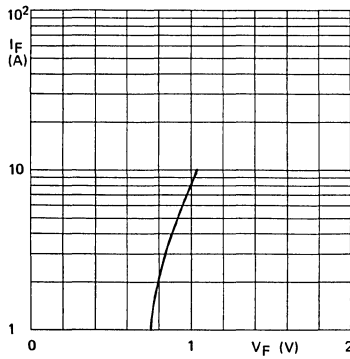


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu s$ ;  $T_j = 25\ ^\circ C$ .

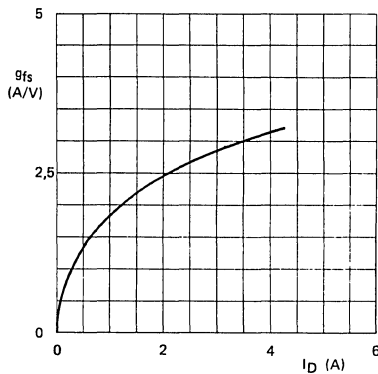


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ V$ ;  $T_j = 25\ ^\circ C$ .



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ44A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

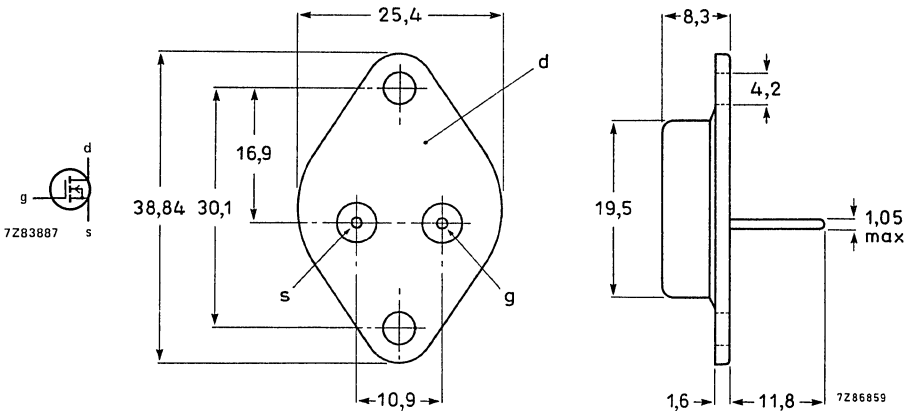
Drain-source voltage	$V_{DS}$	max.	500 V
Drain current (d.c.)	$I_D$	max.	4,8 A
Total power dissipation	$P_{tot}$	max.	78 W
Drain-source resistance (on)	$R_{DS ON}$	<	1,5 $\Omega$
Turn-off fall-time $V_{DD} = 30 V; I_D = 2,6 A; V_{GS} = 10 V$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	500 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	500 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	4,8 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	14 A
Total power dissipation	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	500 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 2,5 \text{ A}$	$R_{DS \text{ ON}}$	<	1,5 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	4,8 A
Forward current (peak value)	$I_{FRM}$	<	14 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ.	1,15 V < 1,5 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1200 ns
recovery time	$Q_s$	typ.	6 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs}$	>	1,5 A/V
	typ.	2,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	1600 pF
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Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	90 pF
----------	------	-------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	30 pF
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Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,6 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	30 ns
--------------------	------	-------

rise time

$t_r$	typ.	70 ns
-------	------	-------

turn-off times: delay time

$t_{d \text{ off}}$	typ.	160 ns
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fall time

$t_f$	typ.	100 ns
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DEVELOPMENT SAMPLE DATA

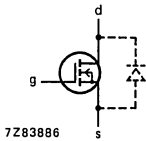


Fig. 2 Diode characteristics.

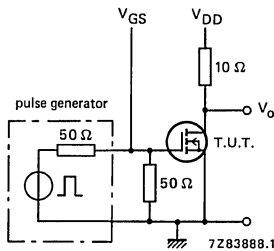


Fig. 3 Switching time test circuit.

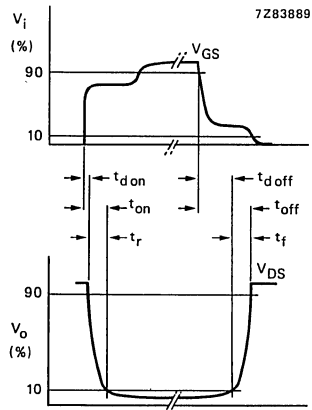


Fig. 4 Switching time waveforms.



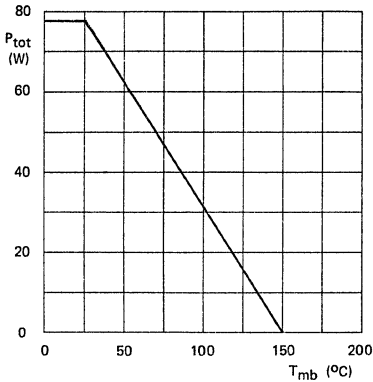


Fig. 5 Power derating curve.

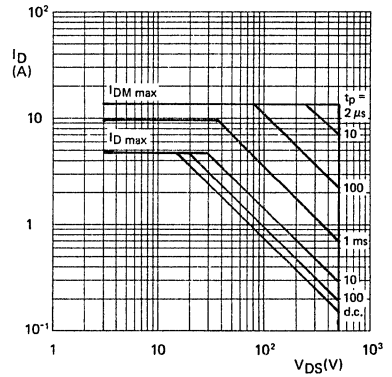


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

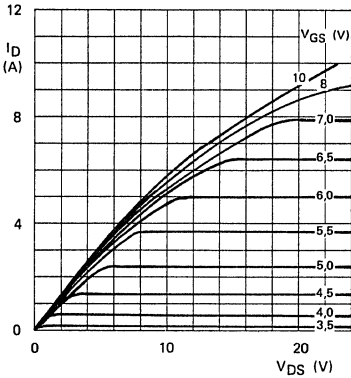


Fig. 7 Output characteristic,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^{\circ}\text{C}$ .

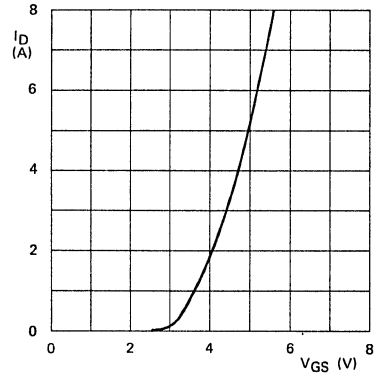


Fig. 8 Typical transfer characteristic  
 $V_{DS} = 25\text{ V}$ ;  $80\text{ }\mu\text{s}$  pulse test;  $T_j = 25\text{ }^{\circ}\text{C}$ .

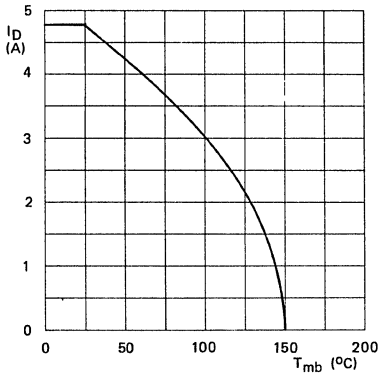


Fig. 9 Drain current as a function  
of mounting base temperature.

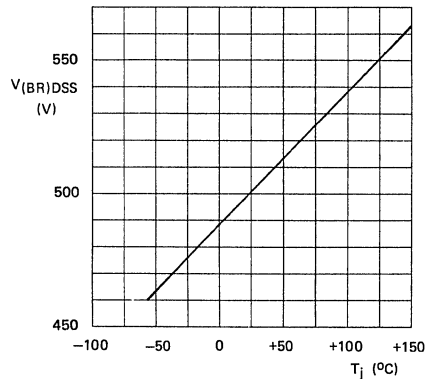


Fig. 10 Drain-source breakdown voltage  
as a function of junction temperature.

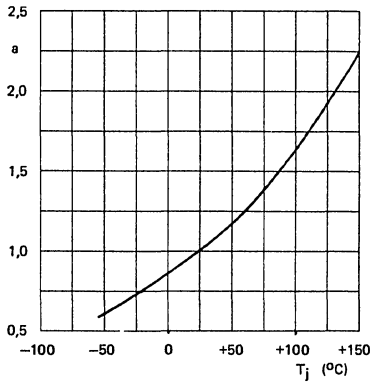


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ\text{C})$ .

DEVELOPMENT SAMPLE DATA

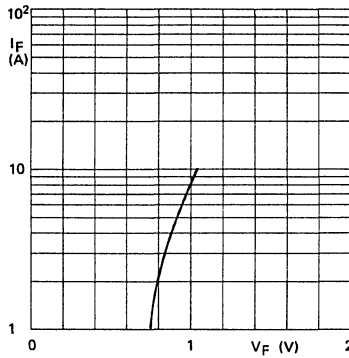


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu\text{s}$ ;  $T_j = 25\ ^\circ\text{C}$ .

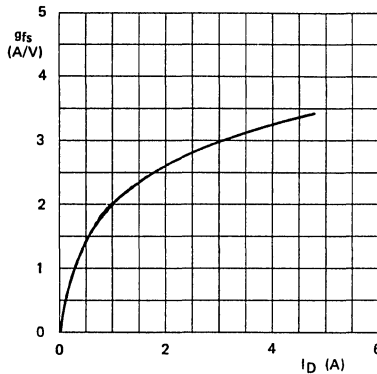


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ \text{V}$ ;  $T_j = 25\ ^\circ\text{C}$ .



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ45

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

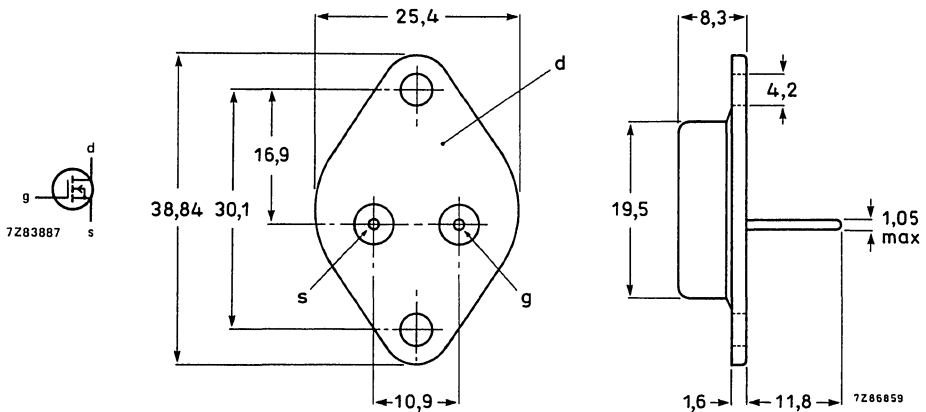
Drain-source voltage	$V_{DS}$	max.	500 V
Drain current (d.c.)	$I_D$	max.	9,6 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,6 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,8\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	500 V
Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	$V_{DGR}$	max.	500 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25\text{ }^\circ\text{C}$	$I_D$	max.	9,6 A
Drain current (pulse peak value); $T_{mb} = 25\text{ }^\circ\text{C}$	$I_{DM}$	max.	28 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th\ j-mb}$	=	1,0 K/W
From junction to ambient	$R_{th\ j-a}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0\text{ V}; I_D = 1\text{ mA}$	$V_{(BR)DSS}$	>	500 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10\text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25\text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125\text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20\text{ V}; V_{DS} = 0\text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10\text{ V}; I_D = 5\text{ A}$	$R_{DS\ ON}$	typ. <	0,55 $\Omega$ 0,6 $\Omega$

**Diode characteristics**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	9,6 A
Forward current (peak value)	$I_{FRM}$	<	28 A
On-state voltage $I_F = 2\text{ I}_D; V_{GS} = 0\text{ V}$	$V_F$	typ. <	1,3 V 1,7 V
Reverse recovery $I_F = 2\text{ I}_D; dI_F/dt = 100\text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1200 ns
recovery time	$Q_s$	typ.	12 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 5 \text{ A}$

$g_{fs}$	>	2,7 A/V
	typ.	5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	3500 pF
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Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	200 pF
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Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	100 pF
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Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,8 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

rise time

$t_{d \text{ on}}$	typ.	50 ns
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$t_r$	typ.	100 ns
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turn-off times: delay time

fall time

$t_{d \text{ off}}$	typ.	450 ns
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$t_f$	typ.	100 ns
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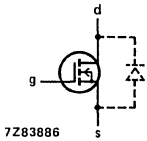


Fig. 2 Diode characteristics.

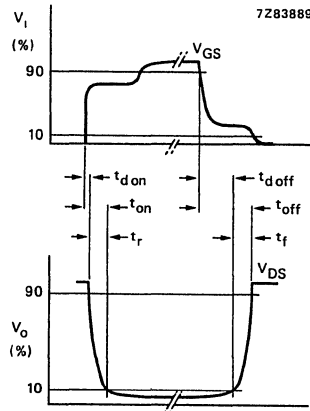


Fig. 4 Switching time waveforms.

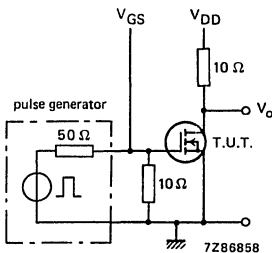


Fig. 3 Switching time test circuit.

DEVELOPMENT SAMPLE DATA

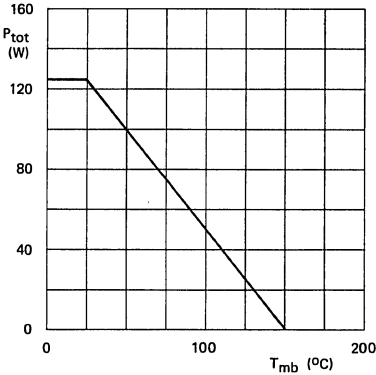


Fig. 5 Power derating curve.

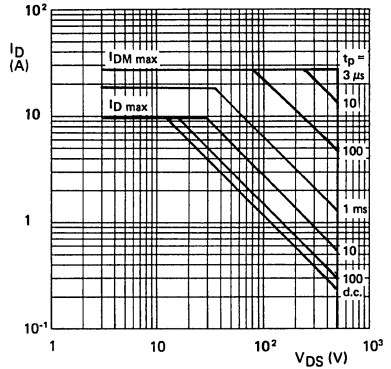


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

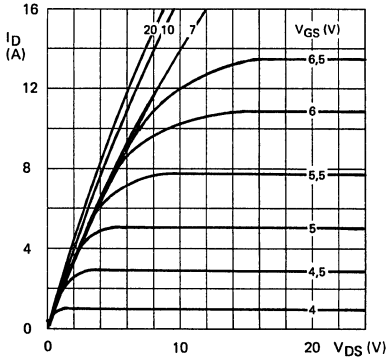


Fig. 7 Output characteristic,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^{\circ}\text{C}$ .

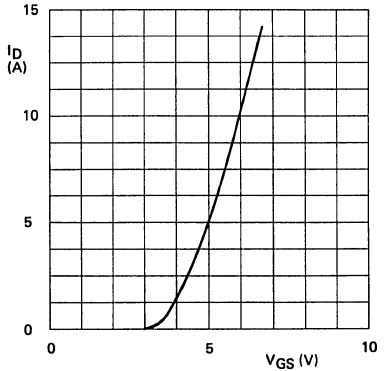


Fig. 8 Typical transfer characteristic  
 $V_{DS} = 25\text{ V}$ ;  $80\text{ }\mu\text{s}$  pulse test;  $T_j = 25\text{ }^{\circ}\text{C}$ .

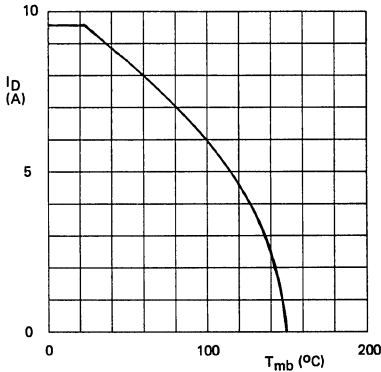


Fig. 9 Drain current as a function  
of mounting base temperature.

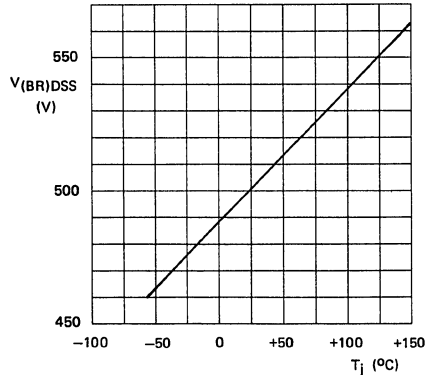


Fig. 10 Drain-source breakdown voltage  
as a function of junction temperature.

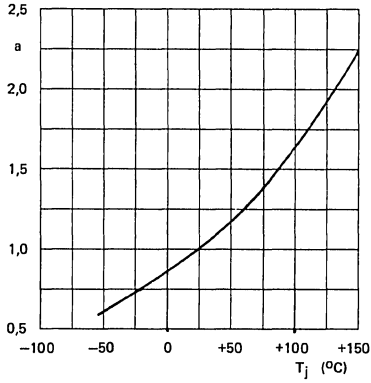


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ\text{C})$ .

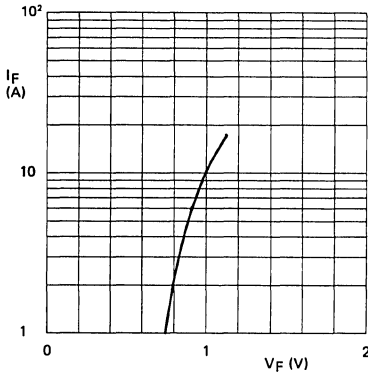


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu\text{s}$ ;  $T_j = 25\ ^\circ\text{C}$ .

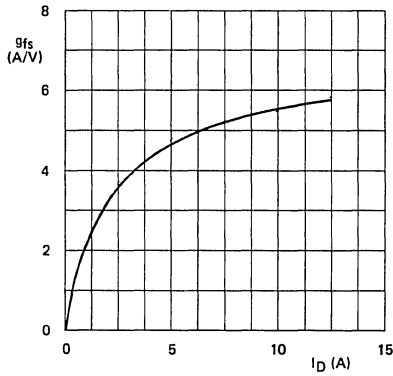


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ \text{V}$ ;  $T_j = 25\ ^\circ\text{C}$ .





# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ45A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

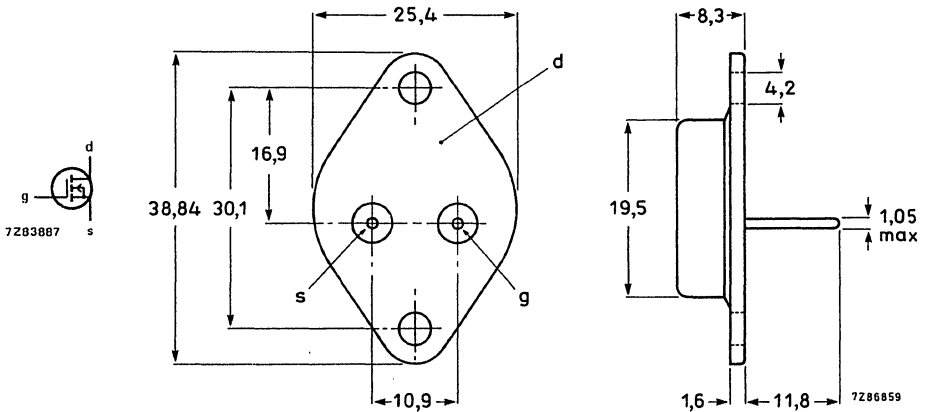
Drain-source voltage	$V_{DS}$	max.	500 V
Drain current (d.c.)	$I_D$	max.	8,3 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,8 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,8\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	500 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	500 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	8,3 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	24 A
Total power dissipation	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,0 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	500 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}$	$R_{DS \text{ ON}}$	typ. <	0,7 $\Omega$ 0,8 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	8,3 A
Forward current (peak value)	$I_{FRM}$	<	24 A
On-state voltage $I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,3 V 1,6 V
Reverse recovery $I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1200 ns
recovery time	$Q_s$	typ.	12 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 5 \text{ A}$

$g_{fs}$  > 2,7 A/V  
 typ. 5 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 3500 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 200 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 100 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,8 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 50 ns  
 $t_r$  typ. 100 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 450 ns  
 $t_f$  typ. 100 ns

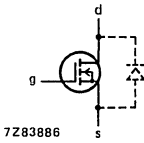


Fig. 2 Diode characteristics.

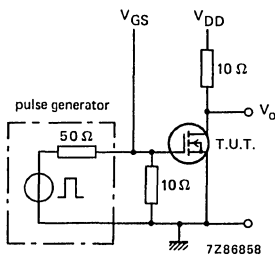


Fig. 3 Switching time test circuit.

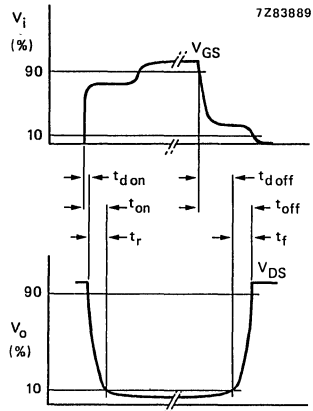


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

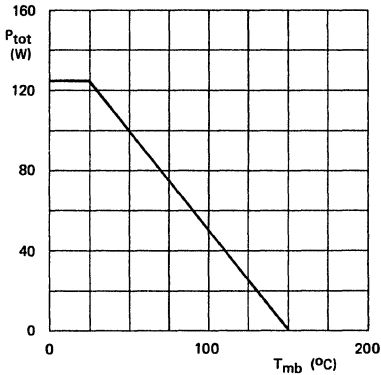


Fig. 5 Power derating curve.

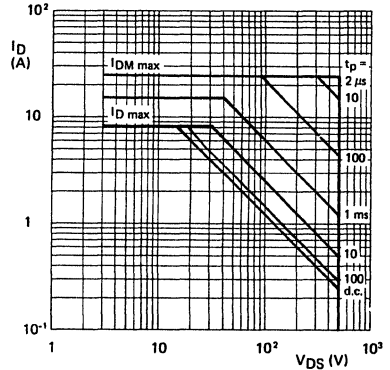


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

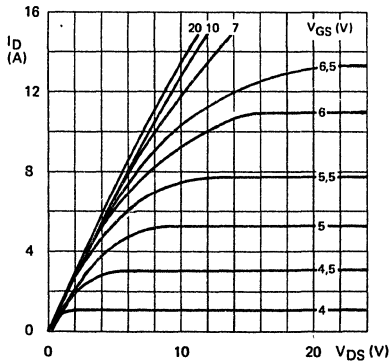


Fig. 7 Output characteristic,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^\circ\text{C}$ .

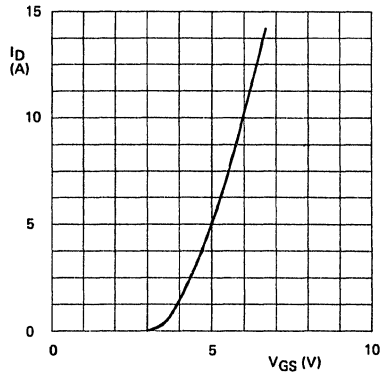


Fig. 8 Typical transfer characteristic  
 $V_{DS} = 25\text{ V}$ ;  $80\text{ }\mu\text{s}$  pulse test;  $T_j = 25\text{ }^\circ\text{C}$ .

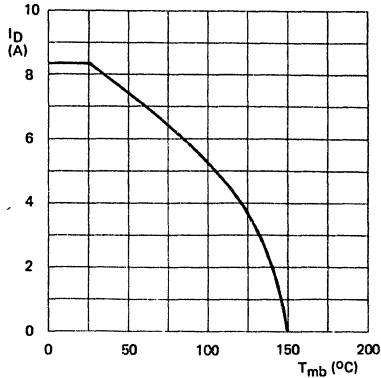


Fig. 9 Drain current as a function  
of mounting base temperature.

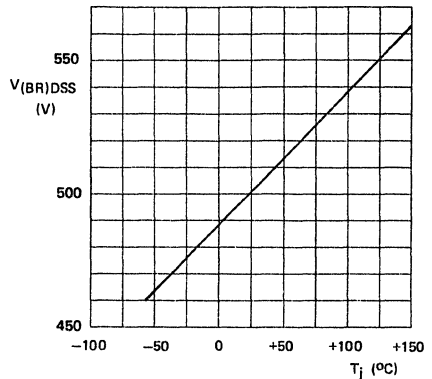


Fig. 10 Drain-source breakdown voltage  
as a function of junction temperature.

DEVELOPMENT SAMPLE DATA

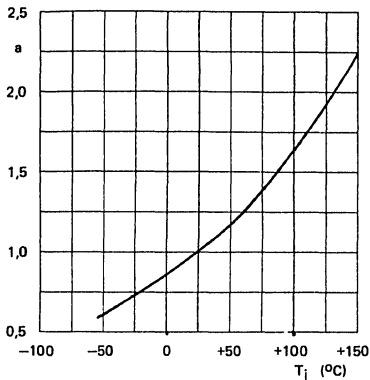


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ\text{C})$ .

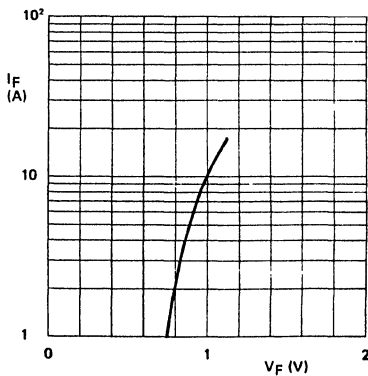


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu\text{s}$ ;  $T_j = 25\ ^\circ\text{C}$ .

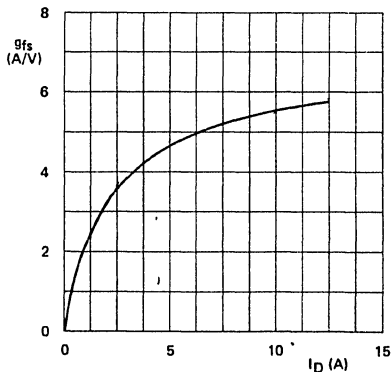


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ \text{V}$ ;  $T_j = 25\ ^\circ\text{C}$ .



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ45B

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

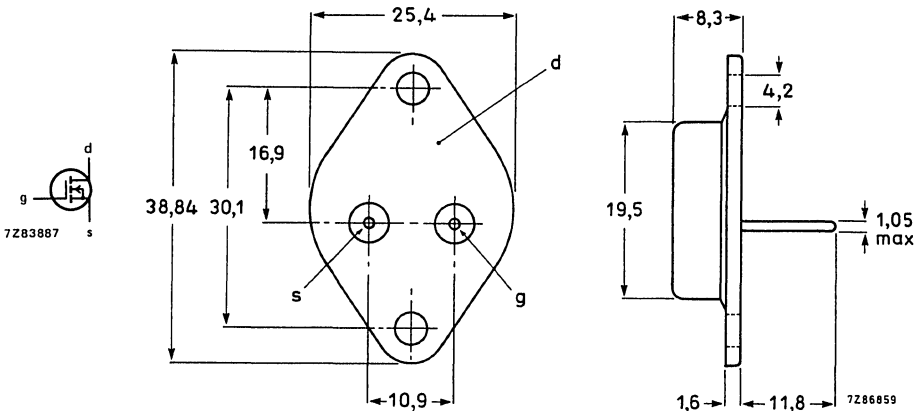
Drain-source voltage	$V_{DS}$	max.	500 V
Drain current (d.c.)	$I_D$	max.	10 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,5 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,9\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	500 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	500 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 35 \text{ }^\circ\text{C}$	$I_D$	max.	10 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	30 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,0 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	500 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}$	$R_{DS \text{ ON}}$	<	0,5 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	10 A
Forward current (peak value)	$I_{FRM}$	<	30 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,3 V 1,7 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1200 ns
recovery time	$Q_s$	typ.	12 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 5 \text{ A}$

$g_{fs} > 2,7 \text{ A/V}$   
 typ. 5 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 3500 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 200 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 100 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,9 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 50 ns

$t_r$  typ. 100 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 450 ns

$t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

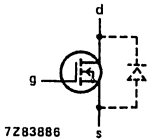


Fig. 2 Diode characteristics.

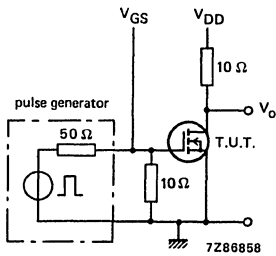


Fig. 3 Switching time test circuit.

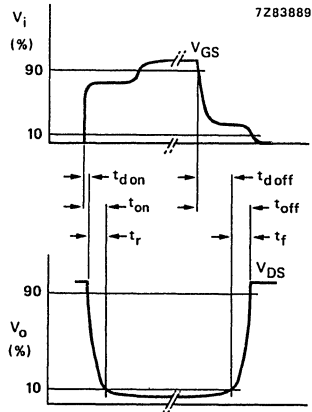


Fig. 4 Switching time waveforms.

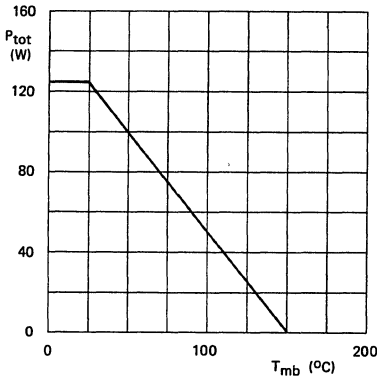


Fig. 5 Power derating curve.

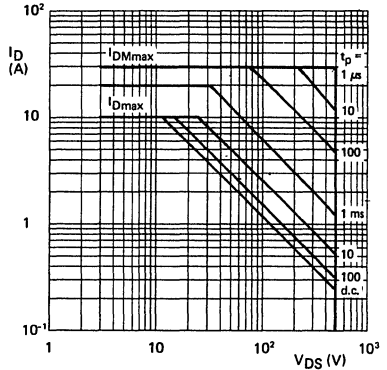


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

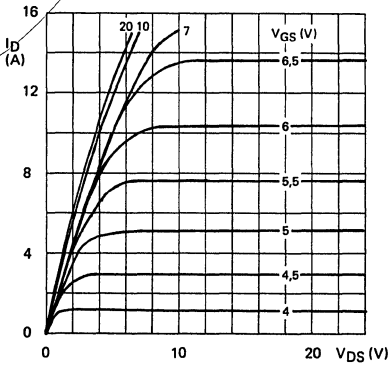


Fig. 7 Output characteristic,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^{\circ}\text{C}$ .

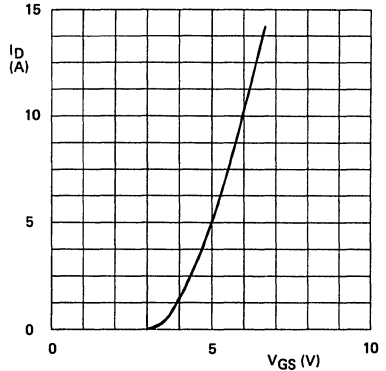


Fig. 8 Typical transfer characteristic  
 $V_{DS} = 25\text{ V}$ ;  $80\text{ }\mu\text{s}$  pulse test;  $T_j = 25\text{ }^{\circ}\text{C}$ .

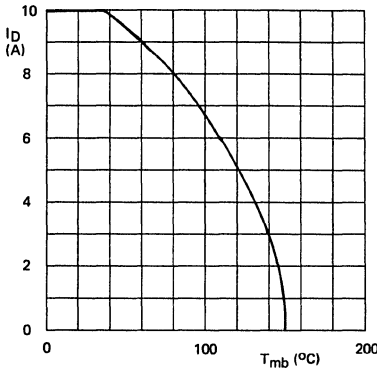


Fig. 9 Drain current as a function  
of mounting base temperature.

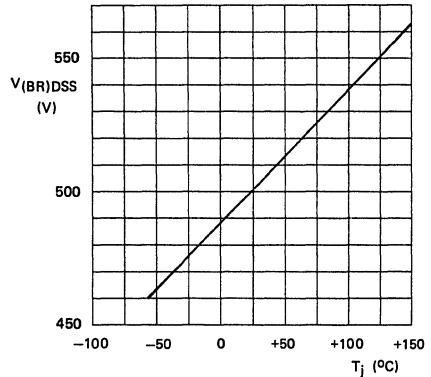


Fig. 10 Drain-source breakdown voltage  
as a function of junction temperature.

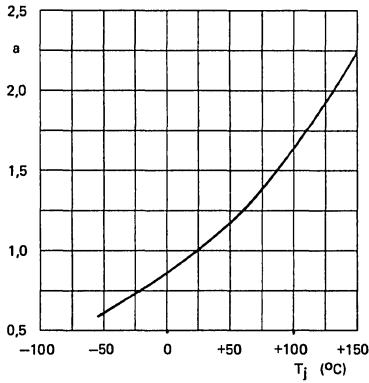


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ\text{C})$ .

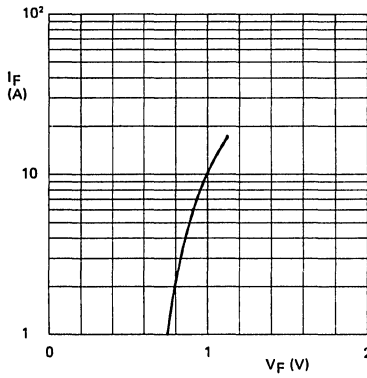


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu\text{s}$ ;  $T_j = 25\ ^\circ\text{C}$ .

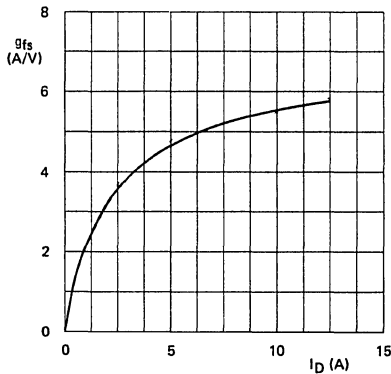


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ \text{V}$ ;  $T_j = 25\ ^\circ\text{C}$ .

DEVELOPMENT SAMPLE DATA



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ45C

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

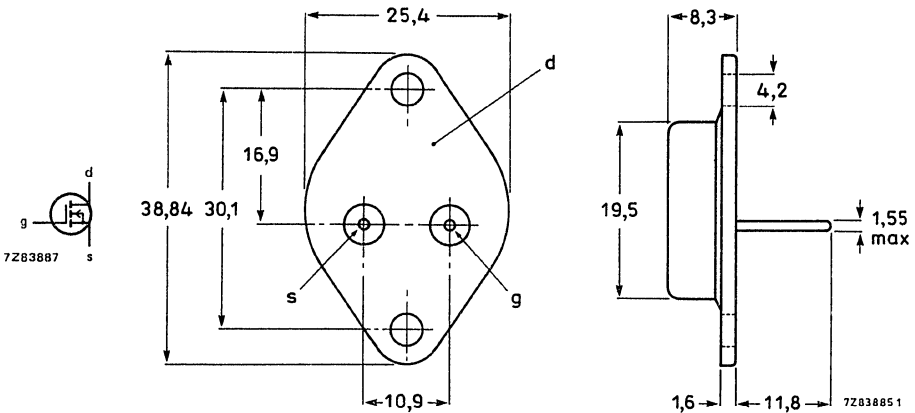
Drain-source voltage	$V_{DS}$	max.	450 V
Drain current (d.c.)	$I_D$	max.	10 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,5 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,9\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	450 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	450 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 35 \text{ }^\circ\text{C}$	$I_D$	max.	10 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	30 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,0 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	450 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}$	$R_{DS \text{ ON}}$	<	0,5 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	10 A
Forward current (peak value)	$I_{FRM}$	<	30 A
On-state voltage $I_F = 2 \times I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ.	1,3 V
		<	1,7 V
Reverse recovery $I_F = 2 \times I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1200 ns
recovery time	$Q_s$	typ.	12 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 16 \text{ A}$

$g_{fs} > 2,7 \text{ A/V}$   
 typ. 4,0 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 3500 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 200 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 100 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 50 ns  
 $t_r$  typ. 100 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 450 ns  
 $t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

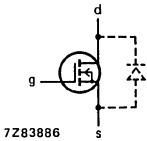


Fig. 2 Diode characteristics.

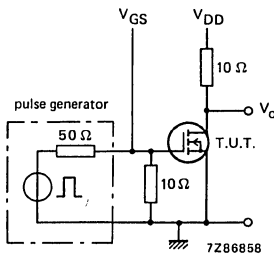


Fig. 3 Switching time test circuit.

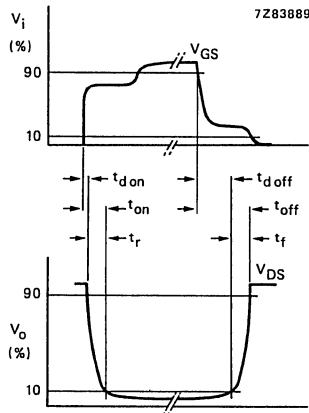


Fig. 4 Switching time waveforms.



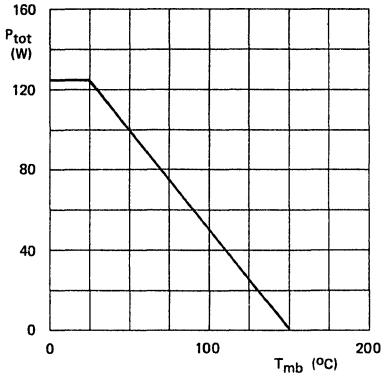


Fig. 5 Power derating curve.

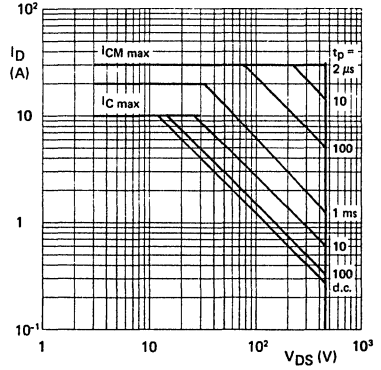


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

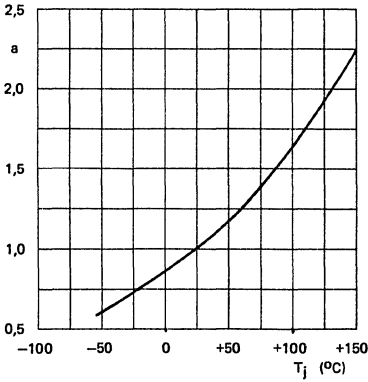


Fig. 7  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^\circ\text{C})$ .

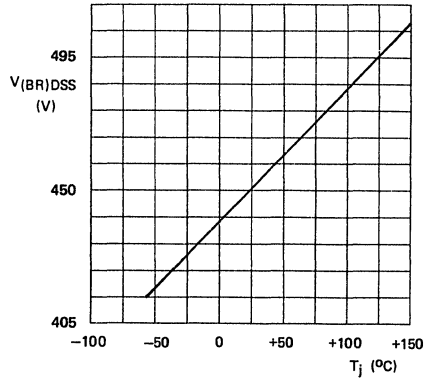


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

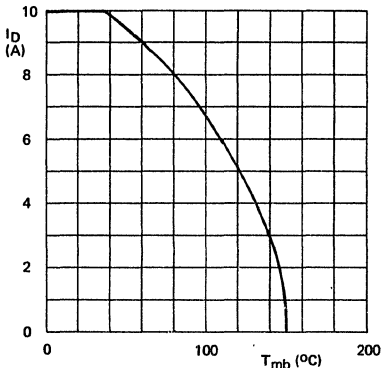


Fig. 9 Drain current as a function of mounting base temperature.

# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ46

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

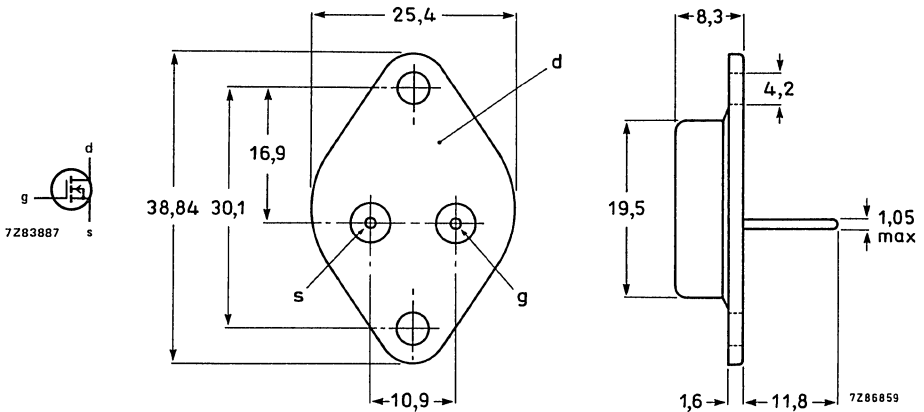
Drain-source voltage	$V_{DS}$	max.	500 V
Drain current (d.c.)	$I_D$	max.	4,2 A
Total power dissipation	$P_{tot}$	max.	78 W
Drain-source resistance (on)	$R_{DS ON}$	<	2,0 $\Omega$
Turn-off fall-time $V_{DD} = 30 V; I_D = 2,5 A; V_{GS} = 10 V$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	500 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	500 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	4,2 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	12 A
Total power dissipation	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$   $V_{(BR)DSS} > 500 \text{ V}$

Gate threshold voltage

$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$   $V_{GST} \begin{matrix} 2,1 \text{ to } 4 \text{ V} \\ \text{typ. } 3 \text{ V} \end{matrix}$

Zero gate voltage drain current

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$   $I_{DSS} < 1 \text{ mA}$

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$   $I_{DSS} < 4 \text{ mA}$

Gate-source leakage current

$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$   $I_{GSS} < 100 \text{ nA}$

Drain-source on-state resistance

$V_{GS} = 10 \text{ V}; I_D = 2,5 \text{ A}$   $R_{DS \text{ ON}} \begin{matrix} \text{typ. } 1,8 \text{ } \Omega \\ < 2,0 \text{ } \Omega \end{matrix}$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$I_F < 4,2 \text{ A}$

Forward current (peak value)

$I_{FRM} < 12 \text{ A}$

On-state voltage

$I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$   $V_F \begin{matrix} \text{typ. } 1,1 \text{ V} \\ < 1,4 \text{ V} \end{matrix}$

Reverse recovery

$I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$

recovery time  $t_{rr} \text{ typ. } 1200 \text{ ns}$

recovery charge  $Q_s \text{ typ. } 6,0 \text{ } \mu\text{C}$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs}$	>	1,5 A/V
	typ.	2,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	1600 pF
----------	------	---------

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	90 pF
----------	------	-------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	30 pF
----------	------	-------

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,5 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	30 ns
--------------------	------	-------

rise time

$t_r$	typ.	70 ns
-------	------	-------

turn-off times: delay time

$t_{d \text{ off}}$	typ.	160 ns
---------------------	------	--------

fall time

$t_f$	typ.	100 ns
-------	------	--------

DEVELOPMENT SAMPLE DATA

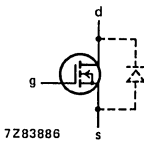


Fig. 2 Diode characteristics.

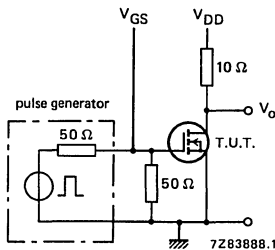


Fig. 3 Switching time test circuit.

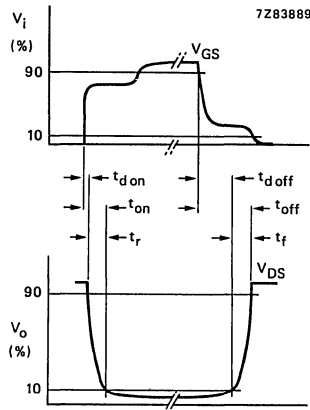


Fig. 4 Switching time waveforms.

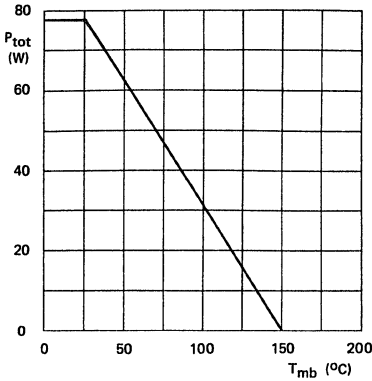


Fig. 5 Power derating curve.

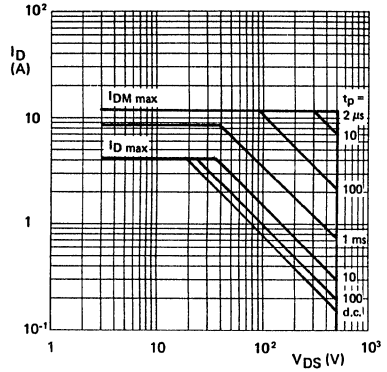


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

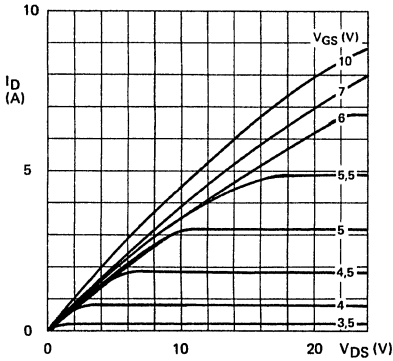


Fig. 7 Output characteristic,  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^\circ\text{C}$ .

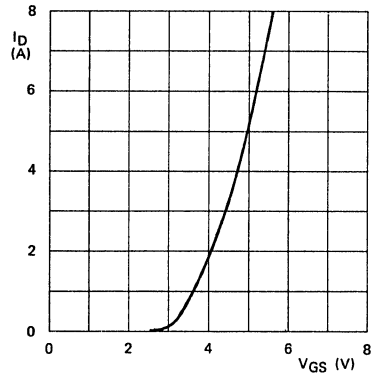


Fig. 8 Typical transfer characteristic  
at  $V_{DS} = 25\text{ V}$ .

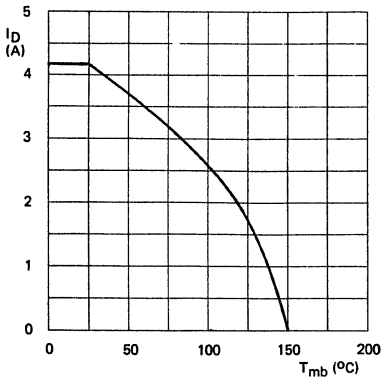


Fig. 9 Drain current as a function  
of mounting base temperature.

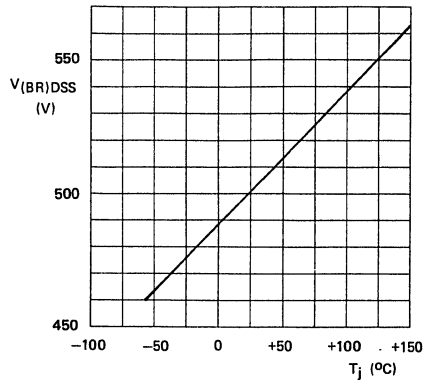


Fig. 10 Drain-source breakdown voltage  
as a function of junction temperature.

DEVELOPMENT SAMPLE DATA

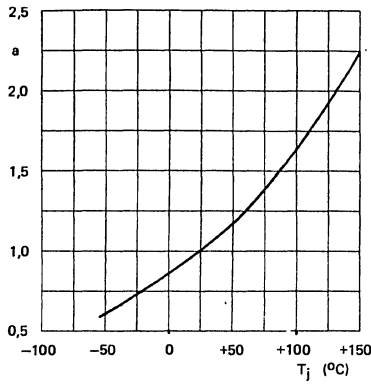


Fig. 11  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ\text{C})$ .

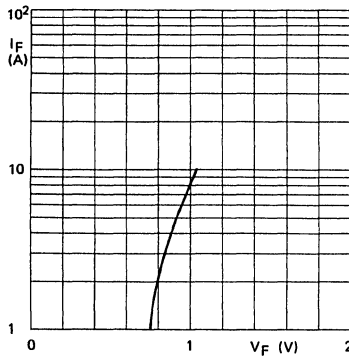


Fig. 12 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu\text{s}$ ;  $T_j = 25\ ^\circ\text{C}$ .

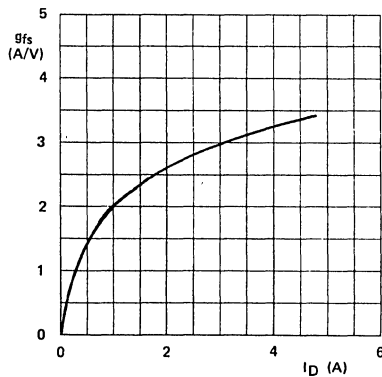


Fig. 13 Forward transfer conductance as a function of drain current.  $V_{DS} = 25\ \text{V}$ ;  $T_j = 25\ ^\circ\text{C}$ .



## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ50A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

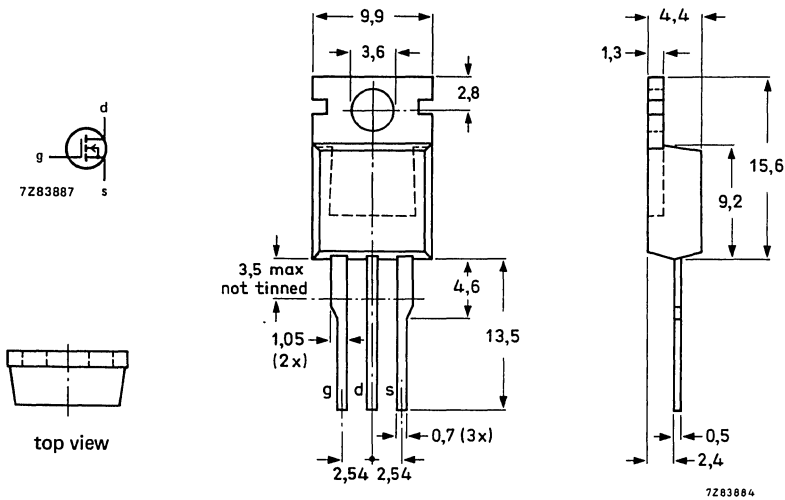
Drain-source voltage	$V_{DS}$	max.	1000 V
Drain current (d.c.)	$I_D$	max.	2,5 A
Total power dissipation	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS ON}$	<	5,0 $\Omega$
Turn-off fall-time $V_{DD} = 30 V$ ; $I_D = 2,0 A$ ; $V_{GS} = 10 V$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	1000 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	1000 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 30 \text{ }^\circ\text{C}$	$I_D$	max.	2,5 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	7,5 A
Total power dissipation	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	1000 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 1,5 \text{ A}$	$R_{DS \text{ ON}}$	<	5 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	2,5 A
Forward current (peak value)	$I_{FRM}$	<	7,5 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,05 V 1,3 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	2500 ns
recovery time	$Q_s$	typ.	250 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 1,5 \text{ A}$

$g_{fs}$	>	0,7 A/V
	typ.	1,5 A/V

input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	1600 pF
----------	------	---------

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	90 pF
----------	------	-------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	30 pF
----------	------	-------

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,0 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	40 ns
--------------------	------	-------

rise time

$t_r$	typ.	70 ns
-------	------	-------

turn-off times: delay time

$t_{d \text{ off}}$	typ.	200 ns
---------------------	------	--------

fall time

$t_f$	typ.	100 ns
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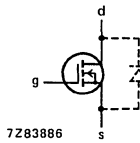


Fig. 2 Diode characteristics.

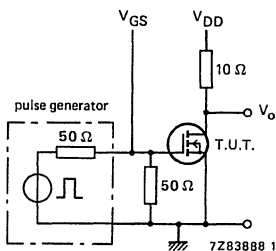


Fig. 3 Switching time test circuit.

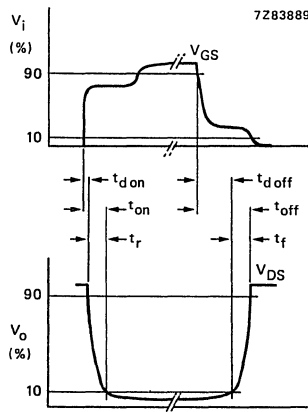


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA



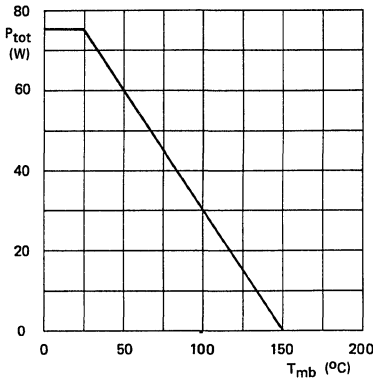


Fig. 5 Power derating curve.

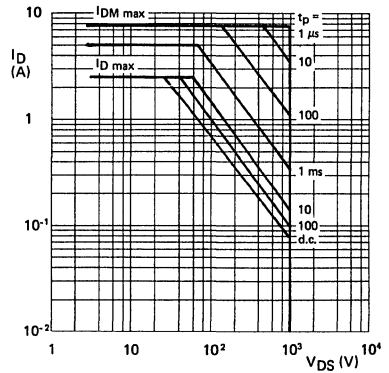


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

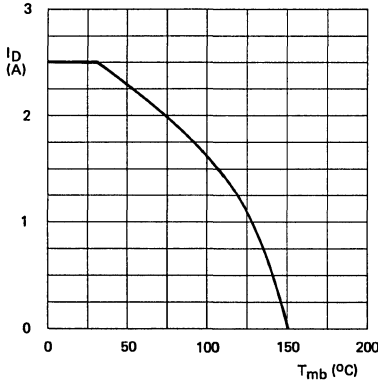


Fig. 7 Drain current as a function of mounting base temperature.

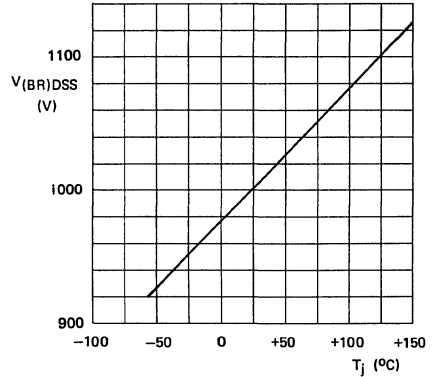


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

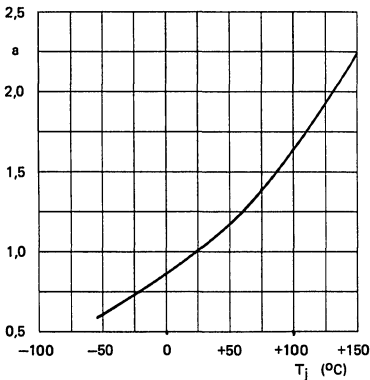


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^\circ\text{C})$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ50B

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

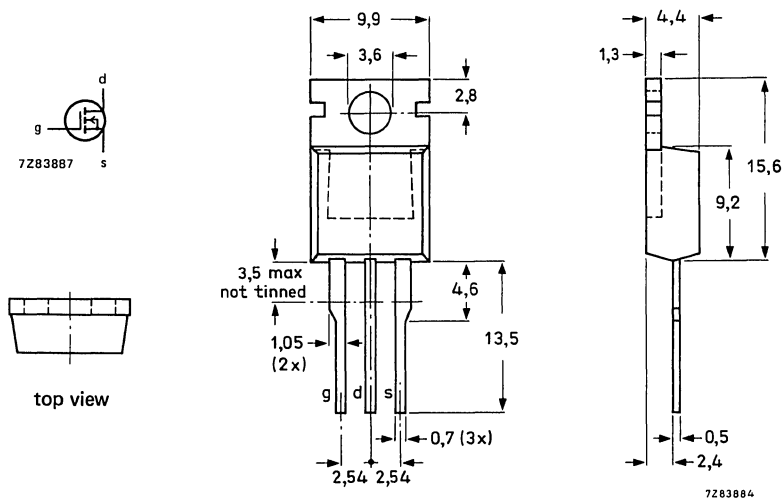
Drain-source voltage	$V_{DS}$	max.	1000 V
Drain current (d.c.)	$I_D$	max.	2,0 A
Total power dissipation	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	8 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 1,7\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	1000 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	1000 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 30 \text{ }^\circ\text{C}$	$I_D$	max.	2,0 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	6,0 A
Total power dissipation	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$

$V_{(BR)DSS} > 1000 \text{ V}$

Gate threshold voltage

$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$

$V_{GST} \text{ typ. } 2,1 \text{ to } 4 \text{ V}$   
 $3 \text{ V}$

Zero gate voltage drain current

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$

$I_{DSS} < 1 \text{ mA}$

$I_{DSS} < 4 \text{ mA}$

Gate-source leakage current

$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$

$I_{GSS} < 100 \text{ nA}$

Drain-source on-state resistance

$V_{GS} = 10 \text{ V}; I_D = 1,5 \text{ A}$

$R_{DS \text{ ON}} < 8 \text{ } \Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$I_F < 2 \text{ A}$

Forward current (peak value)

$I_{FRM} < 6 \text{ A}$

On-state voltage

$I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$

$V_F \text{ typ. } 1,05 \text{ V}$

$< 1,3 \text{ V}$

Reverse recovery

$I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$

recovery time

$t_{rr} \text{ typ. } 2000 \text{ ns}$

recovery charge

$Q_s \text{ typ. } 15 \text{ } \mu\text{C}$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 1,5 \text{ A}$

9fs	>	0,7 A/V
	typ.	1,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	1600 pF
----------	------	---------

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{Os}$	typ.	90 pF
----------	------	-------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	30 pF
----------	------	-------

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 1,7 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	40 ns
--------------------	------	-------

rise time

$t_r$	typ.	70 ns
-------	------	-------

turn-off times: delay time

$t_{d \text{ off}}$	typ.	200 ns
---------------------	------	--------

fall time

$t_f$	typ.	100 ns
-------	------	--------

DEVELOPMENT SAMPLE DATA

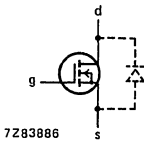


Fig. 2 Diode characteristics.

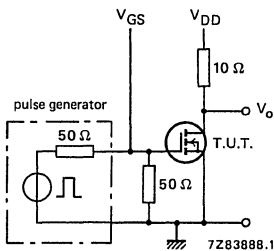


Fig. 3 Switching time test circuit.

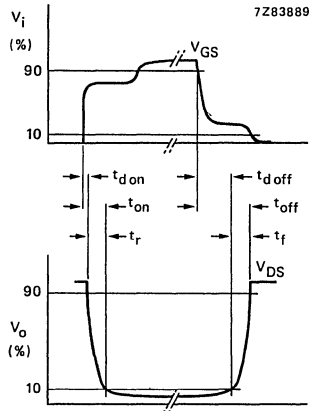


Fig. 4 Switching time waveforms.

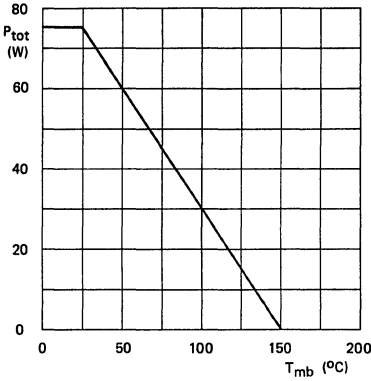


Fig. 5 Power derating curve.

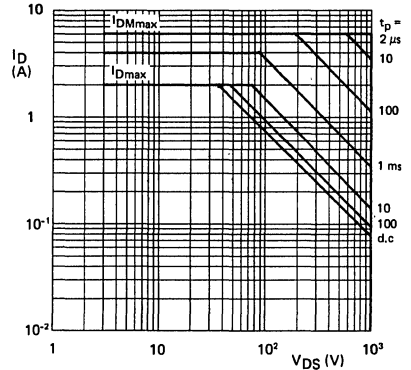


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

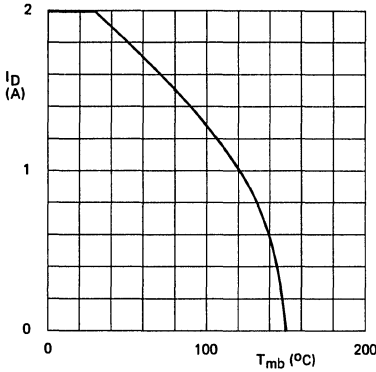


Fig. 7 Drain current as a function of mounting base temperature.

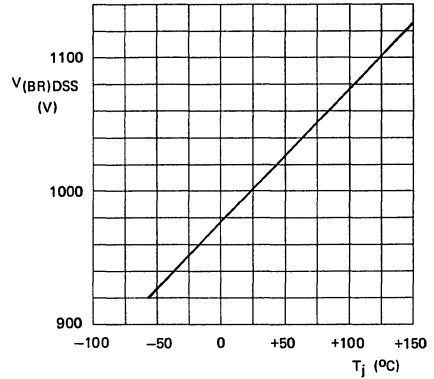


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

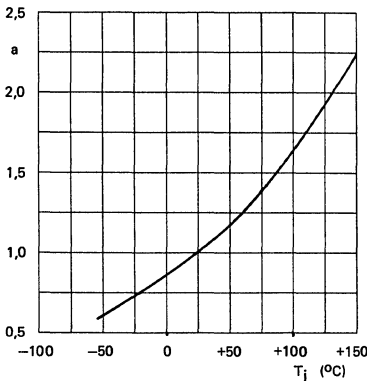


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^{\circ}\text{C})$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ53A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

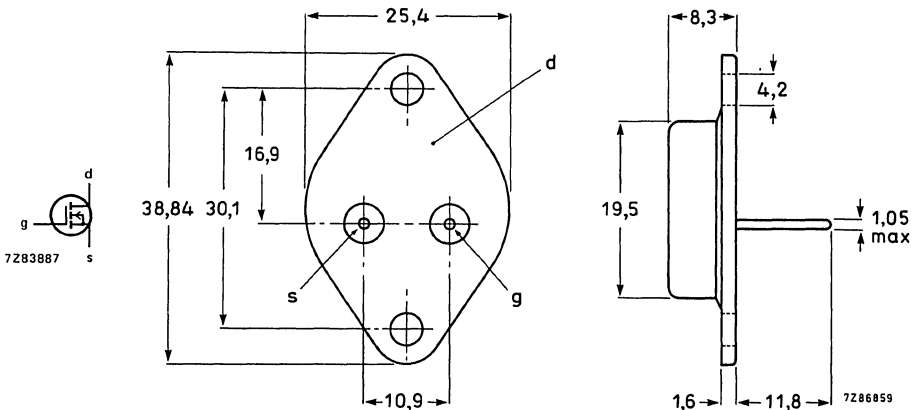
Drain-source voltage	$V_{DS}$	max.	1000 V
Drain current (d.c.)	$I_D$	max.	2,6 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	78 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	5,0 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,0\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	1000 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	1000 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	2,6 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	7,5 A
Total power dissipation	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	1000 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 1,5 \text{ A}$	$R_{DS \text{ ON}}$	<	5 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	2,6 A
Forward current (peak value)	$I_{FRM}$	<	7,5 A
On-state voltage $I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$	$V_F$	typ.	1,05 V
		<	1,3 V
Reverse recovery $I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	2000 ns
recovery time	$Q_s$	typ.	15 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 1,5 \text{ A}$

$g_{fs}$  > 0,7 A/V  
 typ. 1,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1600 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 90 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 30 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,0 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 40 ns  
 $t_r$  typ. 70 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 200 ns  
 $t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

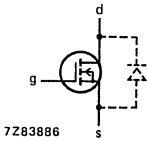


Fig. 2 Diode characteristics.

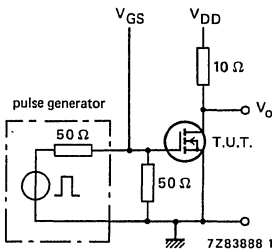


Fig. 3 Switching time test circuit.

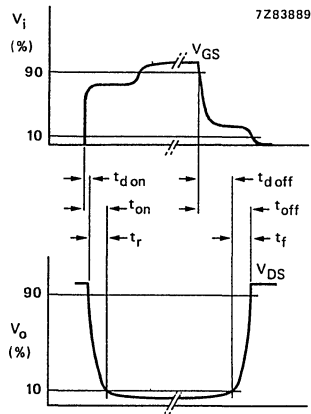


Fig. 4 Switching time waveforms.

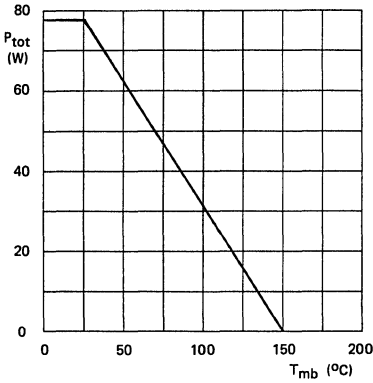


Fig. 5 Power derating curve.

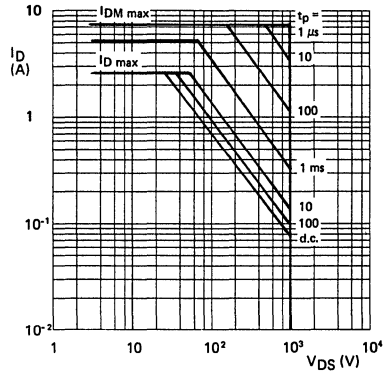


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

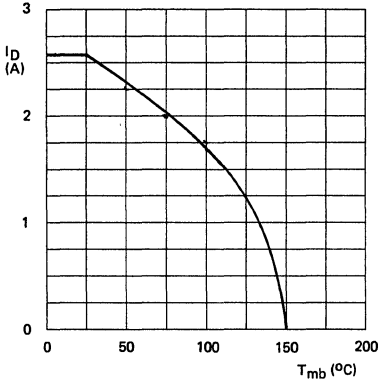


Fig. 7 Drain current as a function of mounting base temperature.

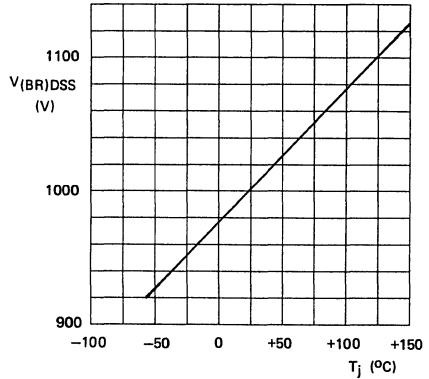


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

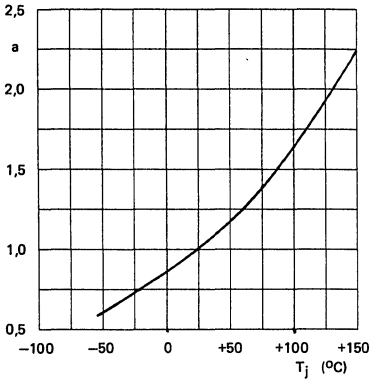


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^\circ\text{C})$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ54

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

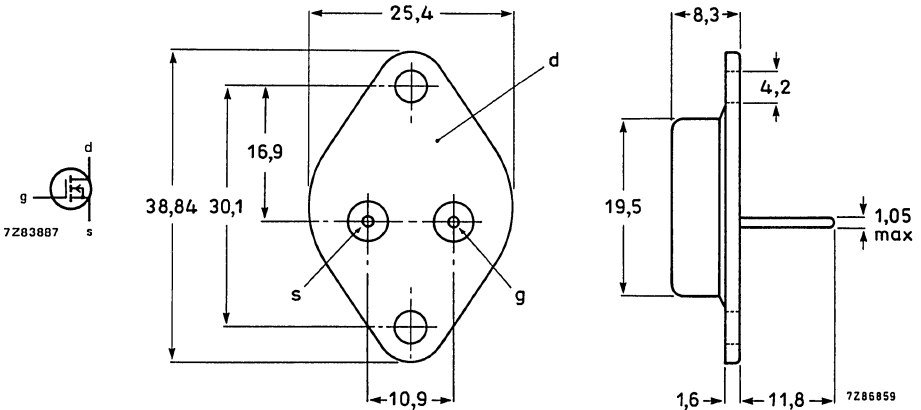
Drain-source voltage	$V_{DS}$	max.	1000 V
Drain current (d.c.)	$I_D$	max.	5,3 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	2,0 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,5\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	1000 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	1000 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	5,3 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	15 A
Total power dissipation	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,0 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	1000 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 2,5 \text{ A}$	$R_{DS \text{ ON}}$	<	2 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	5,3 A
Forward current (peak value)	$I_{FRM}$	<	15 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,15 V 1,4 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	2000 ns
recovery time	$Q_s$	typ.	30 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs}$  > 1,4 A/V  
 typ. 2,0 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 3500 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 200 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 100 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,5 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 60 ns  
 $t_r$  typ. 140 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 500 ns  
 $t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

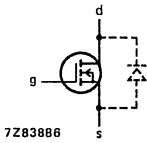


Fig. 2 Diode characteristics.

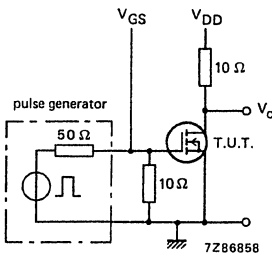


Fig. 3 Switching time test circuit.

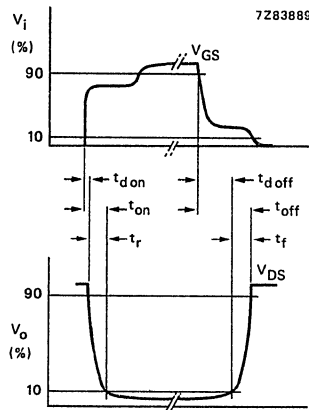


Fig. 4 Switching time waveforms.

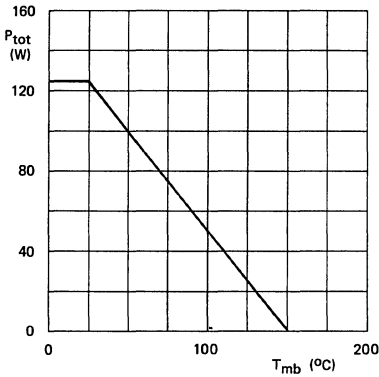


Fig. 5 Power derating curve.

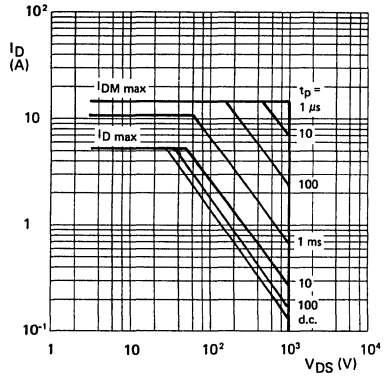


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ °C}$ ;  $\delta = 0,01$ .

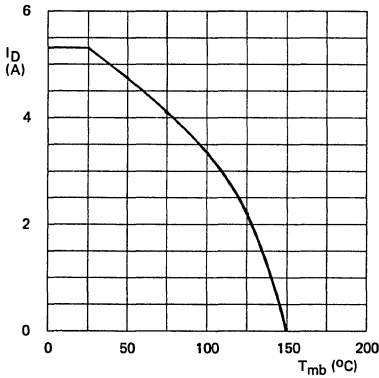


Fig. 7 Drain current as a function of mounting base temperature.

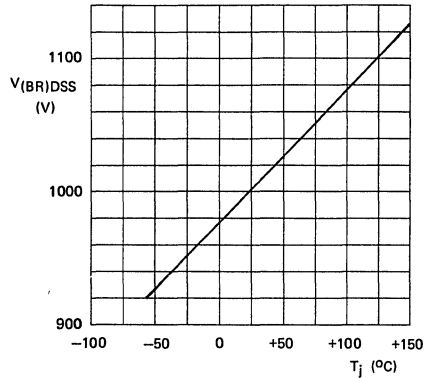


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

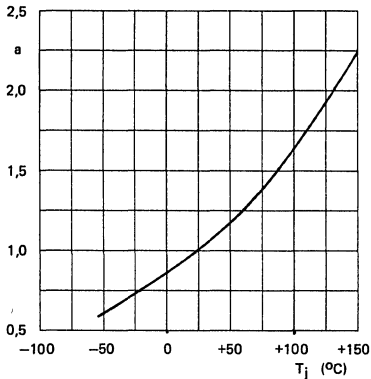


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ °C})$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ54A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

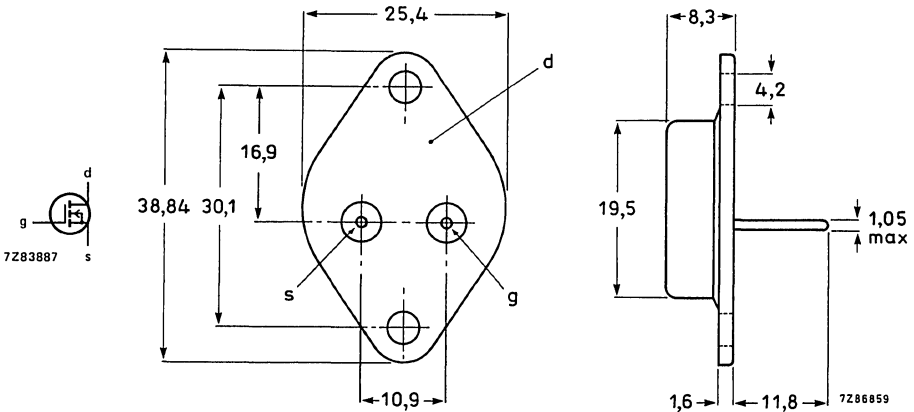
Drain-source voltage	$V_{DS}$	max.	1000 V
Drain current (d.c.)	$I_D$	max.	4,6 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	2,6 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,4\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	1000 V
Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	$V_{DGR}$	max.	1000 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25\text{ }^\circ\text{C}$	$I_D$	max.	4,6 A
Drain current (pulse peak value); $T_{mb} = 25\text{ }^\circ\text{C}$	$I_{DM}$	max.	13 A
Total power dissipation	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th\ j-mb}$	=	1,0 K/W
From junction to ambient	$R_{th\ j-a}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0\text{ V}; I_D = 1\text{ mA}$	$V_{(BR)DSS}$	>	1000 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10\text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25\text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125\text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20\text{ V}; V_{DS} = 0\text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10\text{ V}; I_D = 2,5\text{ A}$	$R_{DS\ ON}$	<	2,6 $\Omega$

**Diode characteristics**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	4,6 A
Forward current (peak value)	$I_{FRM}$	<	13 A
On-state voltage $I_F = 2\text{ I}_D; V_{GS} = 0\text{ V}$	$V_F$	typ.	1,15 V
		<	1,4 V
Reverse recoverh $I_F = 2\text{ I}_D; dI_F/dt = 100\text{ A}/\mu\text{s}$	$t_{rr}$	typ.	2000 ns
recovery time	$Q_s$	typ.	30 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs} > 1,4 \text{ A/V}$   
 typ. 2,0 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 3500 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 200 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 100 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,4 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 60 ns

$t_r$  typ. 140 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 500 ns

$t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

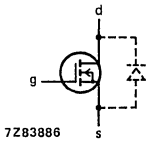


Fig. 2 Diode characteristics.

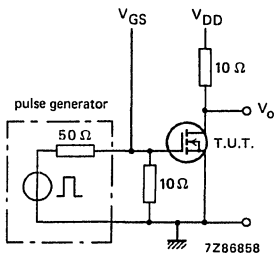


Fig. 3 Switching time test circuit.

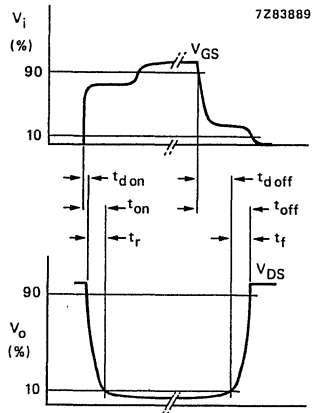


Fig. 4 Switching time waveforms.

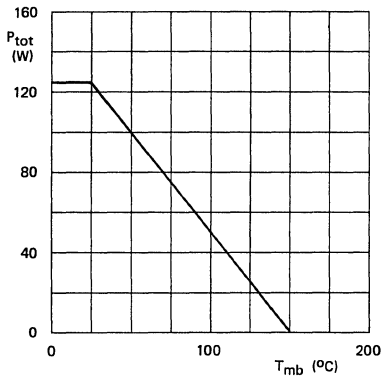


Fig. 5 Power derating curve.

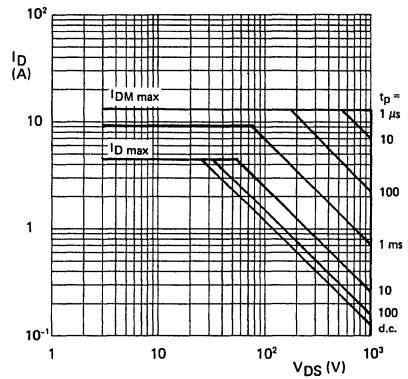


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ °C}; \delta = 0,01.$

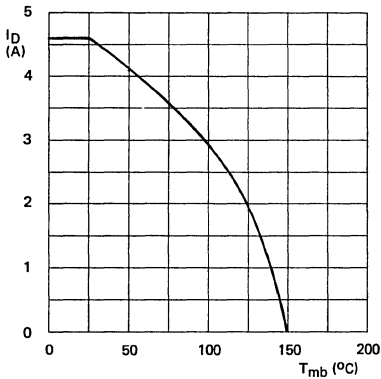


Fig. 7 Drain current as a function of mounting base temperature.

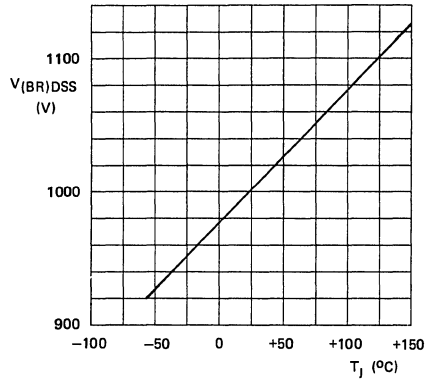


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

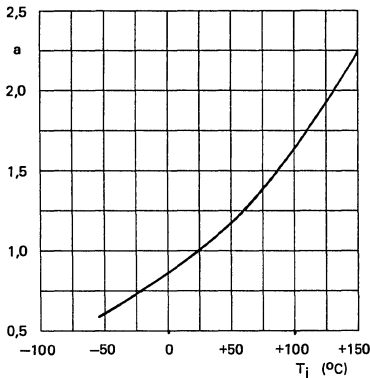


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ °C}).$

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ60

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

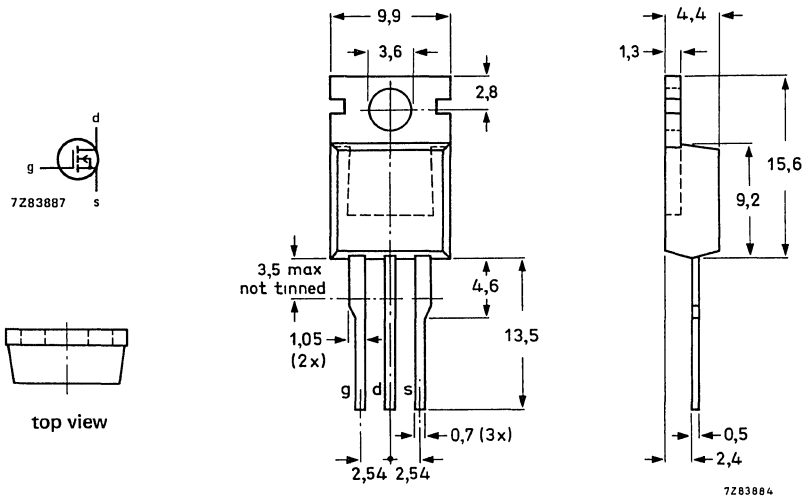
Drain-source voltage	$V_{DS}$	max.	400 V
Drain current (d.c.); $T_{mb} = 35\text{ }^{\circ}\text{C}$	$I_D$	max.	5,5 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	1 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,7\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	400 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	400 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 35 \text{ }^\circ\text{C}$	$I_D$	max.	5,5 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	16 A
Total power dissipation	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

## THERMAL CHARACTERISTICS

### Thermal resistance

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

## STATIC CHARACTERISTICS

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	400 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 2,5 \text{ A}$	$R_{DS \text{ ON}}$	<	1,0 $\Omega$

## Diode characteristics

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	5,5 A
Forward current (peak value)	$I_{FRM}$	<	16 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,15 V 1,6 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1000 ns
recovery time	$Q_s$	typ.	5 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs}$	>	1,7 A/V
	typ.	2,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	1600 pF
----------	------	---------

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	90 pF
----------	------	-------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	30 pF
----------	------	-------

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,7 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	30 ns
--------------------	------	-------

rise time

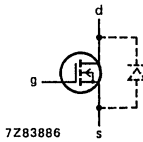
$t_r$	typ.	70 ns
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turn-off times: delay time

$t_{d \text{ off}}$	typ.	160 ns
---------------------	------	--------

fall time

$t_f$	typ.	100 ns
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7Z83886

Fig. 2 Diode characteristics.

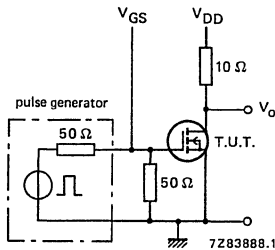


Fig. 3 Switching time test circuit.

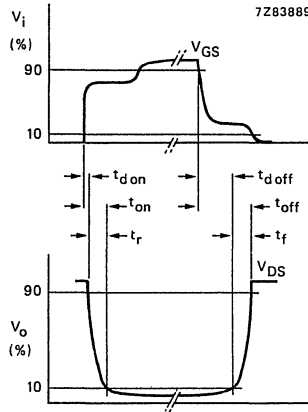


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

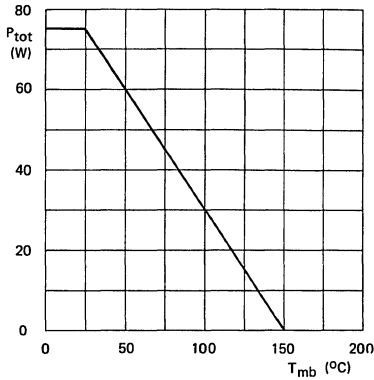


Fig. 5 Power derating curve.

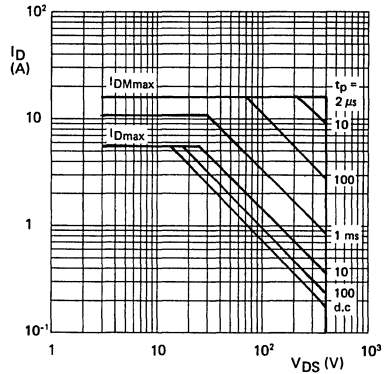


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

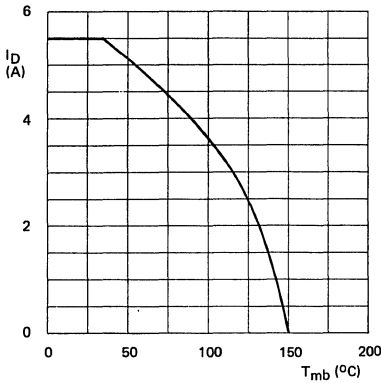


Fig. 7 Drain current as a function of mounting base temperature.

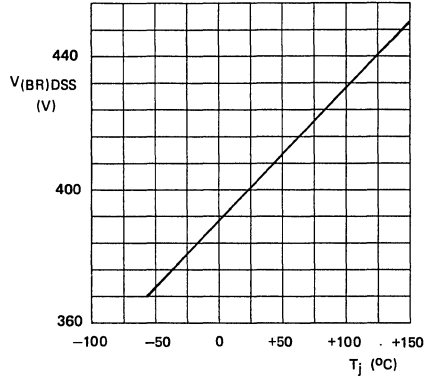


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

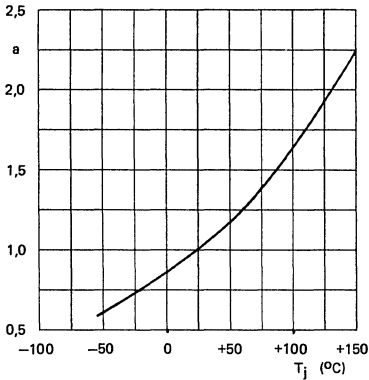


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^\circ\text{C})$ .

# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ60B

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.  
 Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

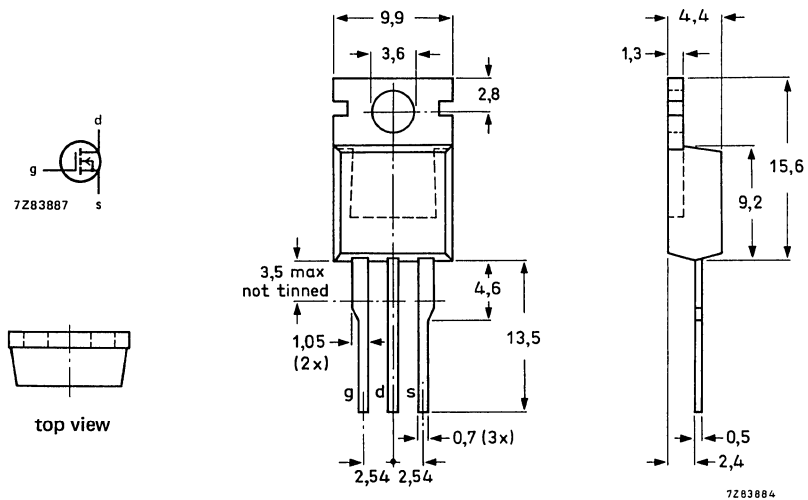
Drain-source voltage	$V_{DS}$	max.	400 V
Drain current (d.c.); $T_{mb} = 35\text{ }^{\circ}\text{C}$	$I_D$	max.	4,5 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	1,5 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,6\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	400 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	400 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 35 \text{ }^\circ\text{C}$	$I_D$	max.	4,5 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	13 A
Total power dissipation	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$   $V_{(BR)DSS} > 400 \text{ V}$

Gate threshold voltage

$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$   $V_{GST} \begin{matrix} 2,1 \text{ to } 4 \text{ V} \\ \text{typ. } 3 \text{ V} \end{matrix}$

Zero gate voltage drain current

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$   $I_{DSS} < 1 \text{ mA}$

$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$   $I_{DSS} < 4 \text{ mA}$

Gate-source leakage current

$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$   $I_{GSS} < 100 \text{ nA}$

Drain-source on-state resistance

$V_{GS} = 10 \text{ V}; I_D = 2,5 \text{ A}$   $R_{DS \text{ ON}} < 1,5 \text{ }\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$I_F < 4,5 \text{ A}$

Forward current (peak value)

$I_{FRM} < 13 \text{ A}$

On-state voltage

$I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$   $V_F \begin{matrix} \text{typ. } 1,15 \text{ V} \\ < 1,5 \text{ V} \end{matrix}$

Reverse recovery

$I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$

recovery time  $t_{rr} \text{ typ. } 1000 \text{ ns}$

recovery charge  $Q_s \text{ typ. } 5 \text{ }\mu\text{C}$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs} > 1,7 \text{ A/V}$   
 typ.  $2,5 \text{ A/V}$

input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ.  $1600 \text{ pF}$

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{Os}$  typ.  $90 \text{ pF}$

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ.  $30 \text{ pF}$

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,6 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ.  $30 \text{ ns}$   
 $t_r$  typ.  $70 \text{ ns}$

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ.  $160 \text{ ns}$   
 $t_f$  typ.  $100 \text{ ns}$

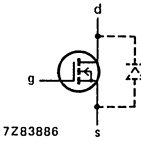


Fig. 2 Diode characteristics.

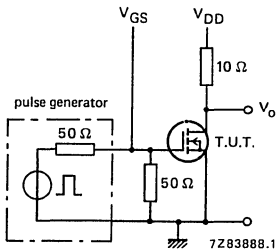


Fig. 3 Switching time test circuit.

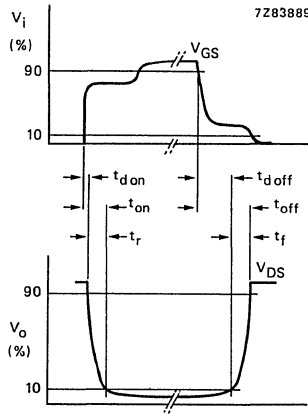


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

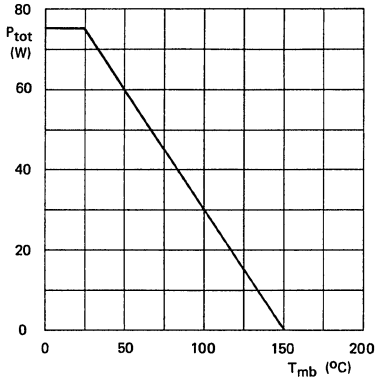


Fig. 5 Power derating curve.

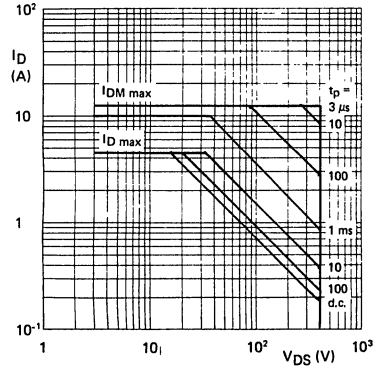


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}; \delta = 0,01.$

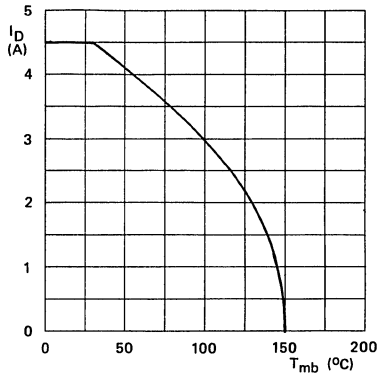


Fig. 7 Drain current as a function of mounting base temperature.

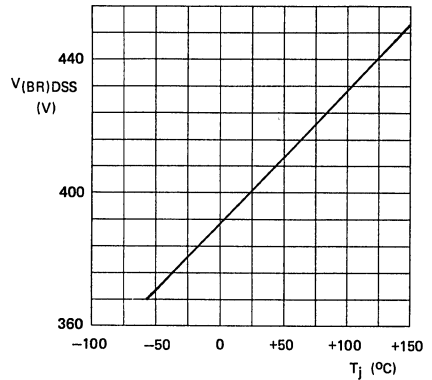


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

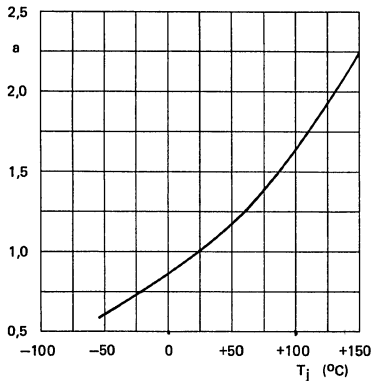


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^\circ\text{C}).$

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ63

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

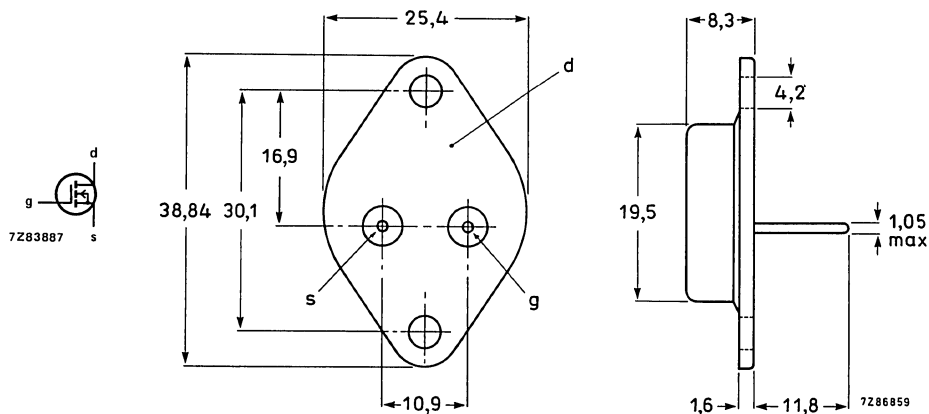
Drain-source voltage	$V_{DS}$	max.	400 V
Drain current (d.c.)	$I_D$	max.	5,9 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	78 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	1 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,7\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	400 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	400 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	5,9 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	17 A
Total power dissipation	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	400 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 2,5 \text{ A}$	$R_{DS \text{ ON}}$	<	1 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	5,9 A
Forward current (peak value)	$I_{FRM}$	<	17 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,2 V 1,65 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1000 ns
recovery time	$Q_s$	typ.	5 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs} > \begin{matrix} 1,7 \text{ A/V} \\ \text{typ. } 2,5 \text{ A/V} \end{matrix}$

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is} \text{ typ. } 1600 \text{ pF}$

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os} \text{ typ. } 90 \text{ pF}$

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs} \text{ typ. } 30 \text{ pF}$

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,7 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}} \text{ typ. } 30 \text{ ns}$

rise time

$t_r \text{ typ. } 70 \text{ ns}$

turn-off times: delay time

$t_{d \text{ off}} \text{ typ. } 160 \text{ ns}$

fall time

$t_f \text{ typ. } 100 \text{ ns}$

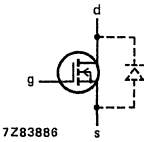


Fig. 2 Diode characteristics.

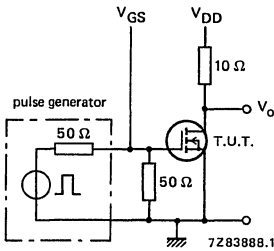


Fig. 3 Switching time test circuit.

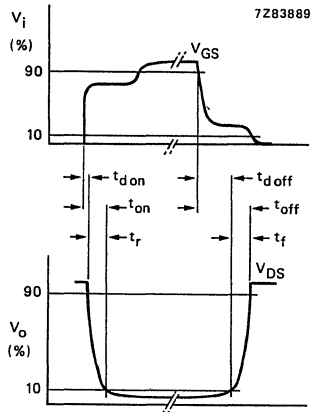


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

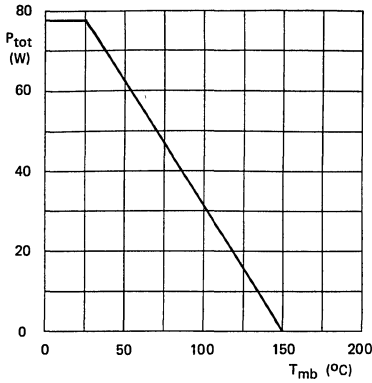


Fig. 5 Power derating curve.

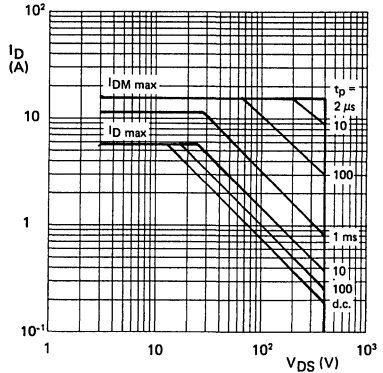


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

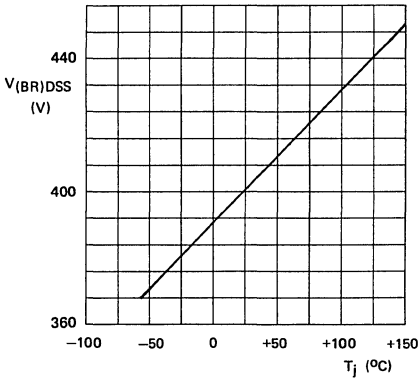


Fig. 7 Drain-source breakdown voltage as a function of junction temperature.

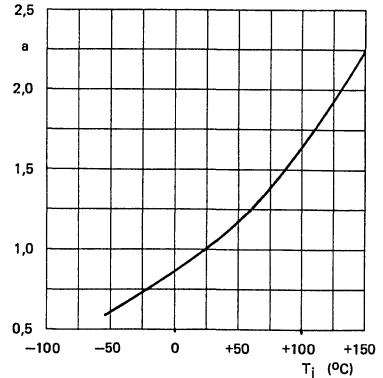


Fig. 8  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^\circ\text{C})$ .

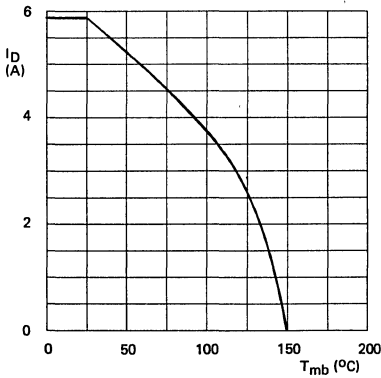


Fig. 9 Drain current as a function of mounting base temperature.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ63B

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

Drain-source voltage

$V_{DS}$  max. 400 V

Drain current (d.c.);  $T_{mb} = 40\text{ }^{\circ}\text{C}$

$I_D$  max. 4,5 A

Total power dissipation;  $T_{mb} = 25\text{ }^{\circ}\text{C}$

$P_{tot}$  max. 78 W

Drain-source resistance (on)

$R_{DS\ ON}$  < 1,5  $\Omega$

Turn-off fall-time

$V_{DD} = 30\text{ V}$ ;  $I_D = 2,6\text{ A}$ ;  $V_{GS} = 10\text{ V}$

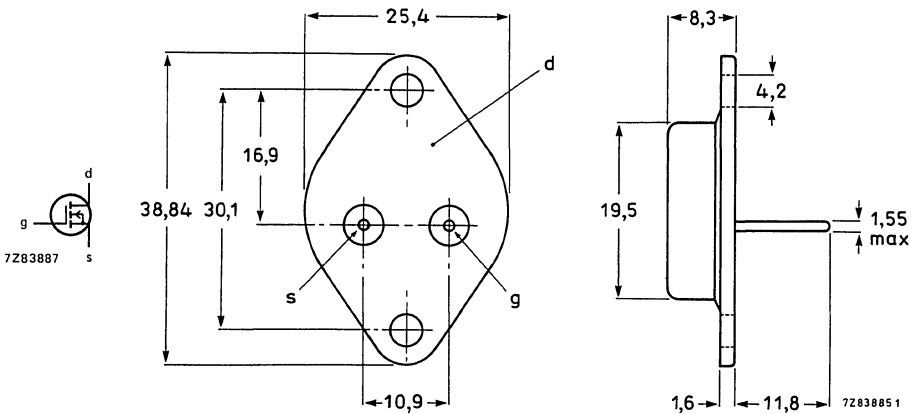
$t_f$  typ. 100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	400 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	400 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 40 \text{ }^\circ\text{C}$	$I_D$	max.	4,5 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	13 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	400 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 2,5 \text{ A}$	$R_{DS \text{ ON}}$	<	1,5 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	4,5 A
Forward current (peak value)	$I_{FRM}$	<	13 A
On-state voltage $I_F = 2 \times I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,15 V 1,5 V
Reverse recovery $I_F = 2 \times I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1000 ns
recovery time	$Q_s$	typ.	5 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 2,5 \text{ A}$

$g_{fs} >$  typ. 1,7 A/V  
2,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1600 pF

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 90 pF

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 30 pF

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,6 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

rise time

$t_{d \text{ on}}$  typ. 30 ns

$t_r$  typ. 70 ns

turn-off times: delay time

fall time

$t_{d \text{ off}}$  typ. 160 ns

$t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

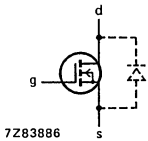


Fig. 2 Diode characteristics.

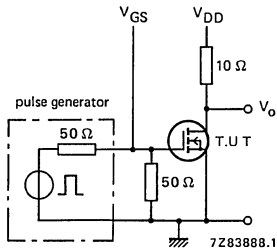


Fig. 3 Switching time test circuit.

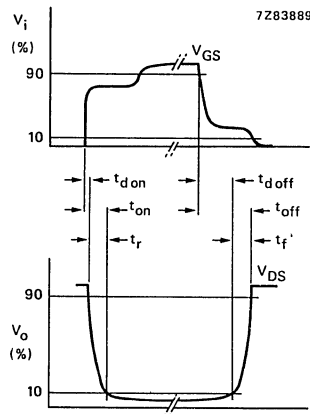


Fig. 4 Switching time waveforms.

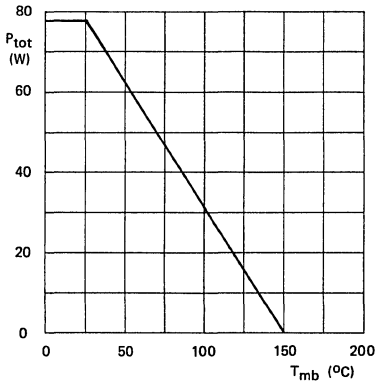


Fig. 5 Power derating curve.

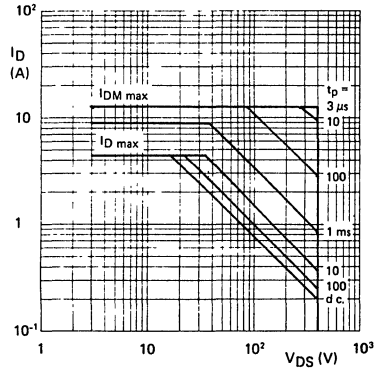


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

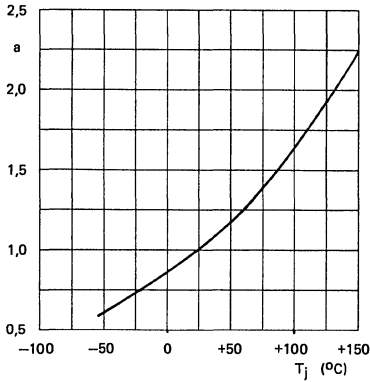


Fig. 7  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^{\circ}\text{C})$ .

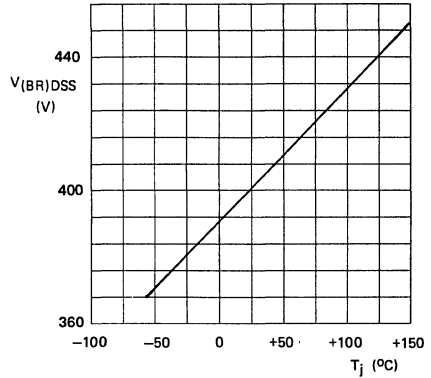


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

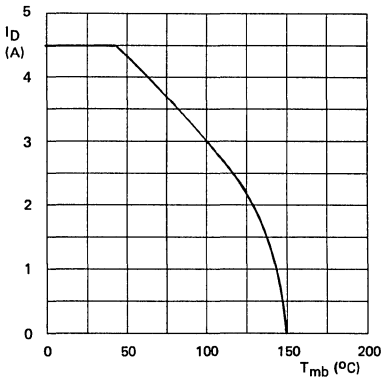


Fig. 9 Drain current as a function of mounting base temperature.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ64

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

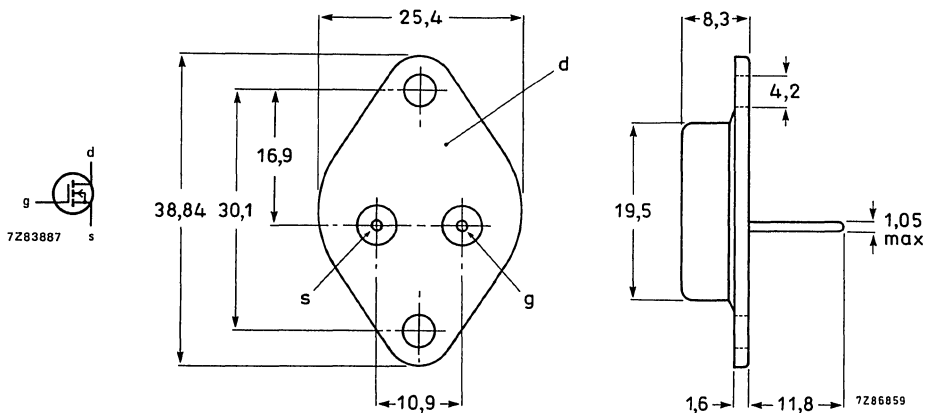
Drain-source voltage	$V_{DS}$	max.	400 V
Drain current (d.c.)	$I_D$	max.	10,5 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,4 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,9\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	400 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	400 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 50 \text{ }^\circ\text{C}$	$I_D$	max.	10,5 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	31 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,0 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	400 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}$	$R_{DS \text{ ON}}$	<	0,4 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	10,5 A
Forward current (peak value)	$I_{FRM}$	<	31 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,3 V 1,7 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1000 ns
recovery time	$Q_s$	typ.	10 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 5 \text{ A}$

$g_{fs}$	>	3,3 A/V
	typ.	4,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	3500 pF
----------	------	---------

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	200 pF
----------	------	--------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	100 pF
----------	------	--------

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,9 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

rise time

$t_{d \text{ on}}$	typ.	50 ns
--------------------	------	-------

$t_r$	typ.	100 ns
-------	------	--------

turn-off times: delay time

fall time

$t_{d \text{ off}}$	typ.	450 ns
---------------------	------	--------

$t_f$	typ.	100 ns
-------	------	--------

DEVELOPMENT SAMPLE DATA

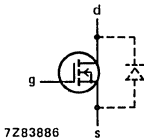


Fig. 2 Diode characteristics.

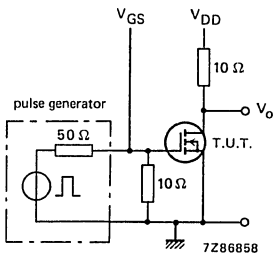


Fig. 3 Switching time test circuit.

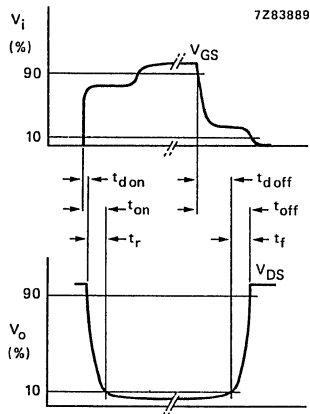


Fig. 4 Switching time waveforms.

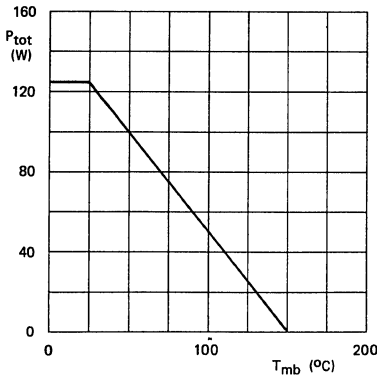


Fig. 5 Power derating curve.

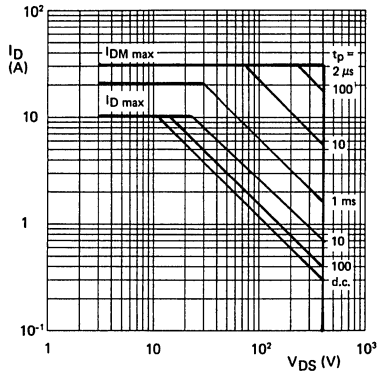


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ °C}$ ;  $\delta = 0,01$ .

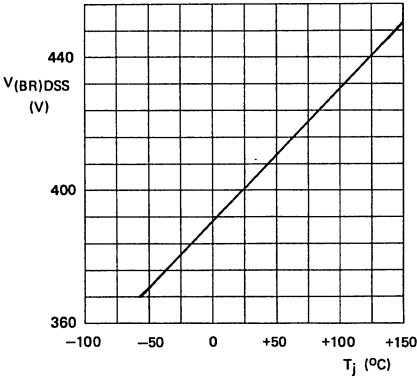


Fig. 7 Drain-source breakdown voltage as a function of junction temperature.

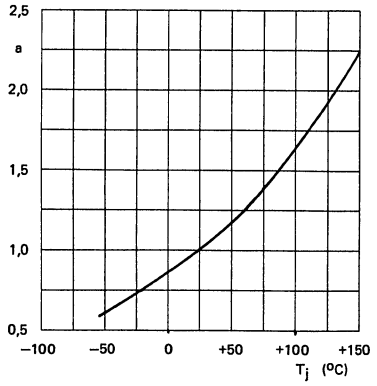


Fig. 8  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ °C})$ .

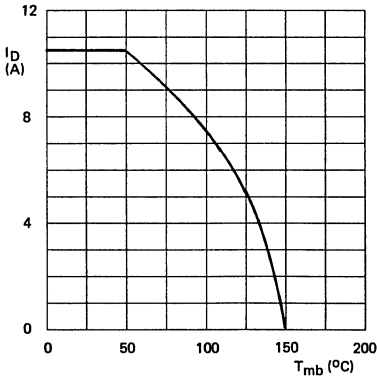


Fig. 9 Drain current as a function of mounting base temperature.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ71

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

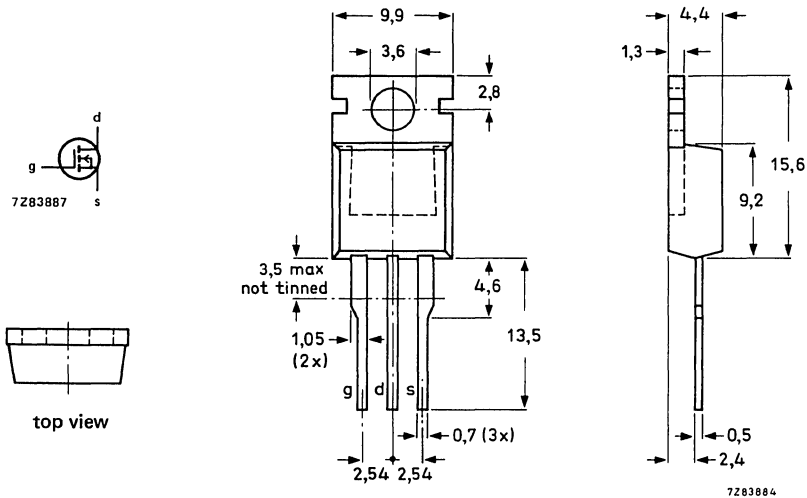
Drain-source voltage	$V_{DS}$	max.	50 V
Drain current (d.c.); $T_{mb} = 35\text{ }^{\circ}\text{C}$	$I_D$	max.	12 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	40 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,1 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,7\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	150 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



# BUZ71

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	50 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	50 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 60 \text{ }^\circ\text{C}$	$I_D$	max.	12 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	36 A
Total power dissipation	$P_{tot}$	max.	40 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+150 $^\circ\text{C}$

## THERMAL CHARACTERISTICS

### Thermal resistance

From junction to mounting base	$R_{th \text{ j-mb}}$	=	3,1 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

## STATIC CHARACTERISTICS

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$$

$$V_{(BR)DSS} > 50 \text{ V}$$

Gate threshold voltage

$$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$$

$$V_{GST} \text{ typ. } \begin{matrix} 2,1 \text{ to } 4 \text{ V} \\ 3 \text{ V} \end{matrix}$$

Zero gate voltage drain current

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$$

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$$

$$I_{DSS} < 0,25 \text{ mA}$$

$$I_{DSS} < 1,0 \text{ mA}$$

Gate-source leakage current

$$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$$

$$I_{GSS} < 100 \text{ nA}$$

Drain-source on-state resistance

$$V_{GS} = 10 \text{ V}; I_D = 6 \text{ A}$$

$$R_{DS \text{ ON}} < 0,1 \text{ } \Omega$$

### Diode characteristics

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$$I_F < 12 \text{ A}$$

Forward current (peak value)

$$I_{FRM} < 36 \text{ A}$$

On-state voltage

$$I_F = 2 I_D; V_{GS} = 0 \text{ V}$$

$$V_F \text{ typ. } \begin{matrix} 1,6 \text{ V} \\ < 2,2 \text{ V} \end{matrix}$$

Reverse recovery

$$I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$$

recovery time

$$t_{rr} \text{ typ. } 120 \text{ ns}$$

recovery charge

$$Q_s \text{ typ. } 0,15 \text{ } \mu\text{C}$$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 6 \text{ A}$

$g_{fs}$	>	3 A/V
	typ.	4,8 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	480 pF
----------	------	--------

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	280 pF
----------	------	--------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	160 pF
----------	------	--------

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	30 ns
--------------------	------	-------

rise time

$t_r$	typ.	100 ns
-------	------	--------

turn-off times: delay time

$t_{d \text{ off}}$	typ.	200 ns
---------------------	------	--------

fall time

$t_f$	typ.	150 ns
-------	------	--------

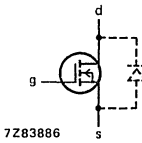


Fig. 2 Diode characteristics.

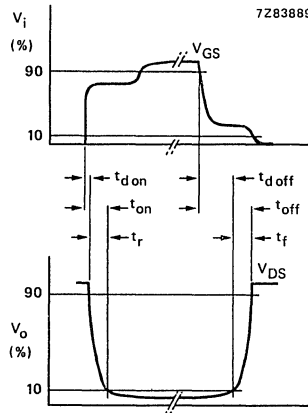


Fig. 4 Switching time waveforms.

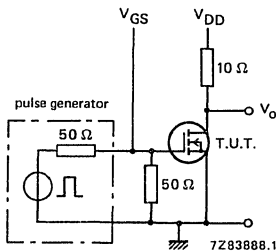


Fig. 3 Switching time test circuit.

DEVELOPMENT SAMPLE DATA

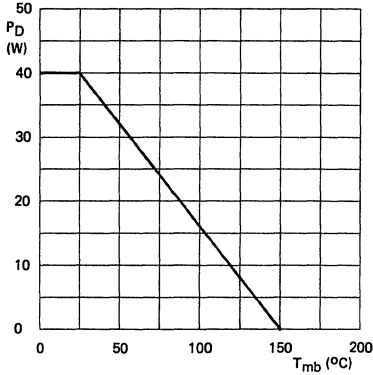


Fig. 5 Power derating curve.

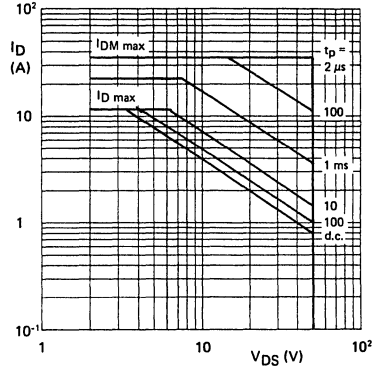


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25^\circ C; \delta = 0,01.$

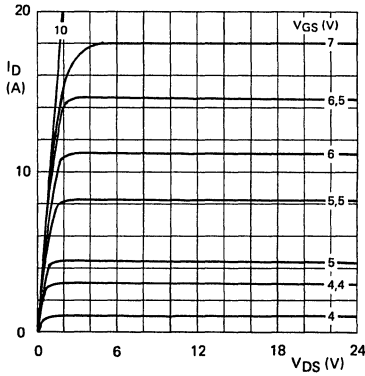


Fig. 7 Output characteristic,  
80  $\mu s$  pulse test;  $T_{mb} = 25^\circ C.$

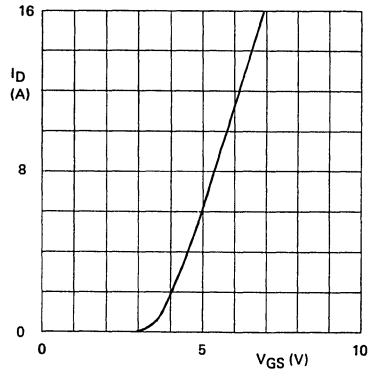


Fig. 8 Typical transfer characteristic  
at  $V_{DS} = 25 V.$

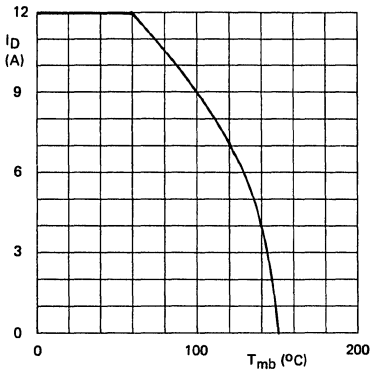


Fig. 9 Drain current as a function  
of mounting base temperature.

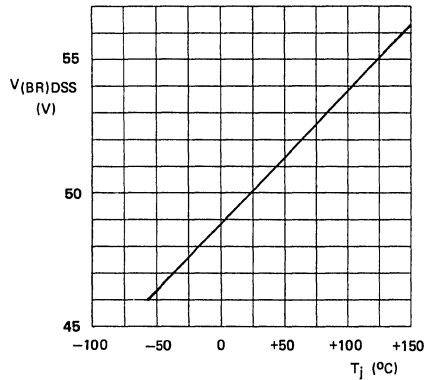


Fig. 10 Drain-source breakdown voltage  
as a function of junction temperature.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ71A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

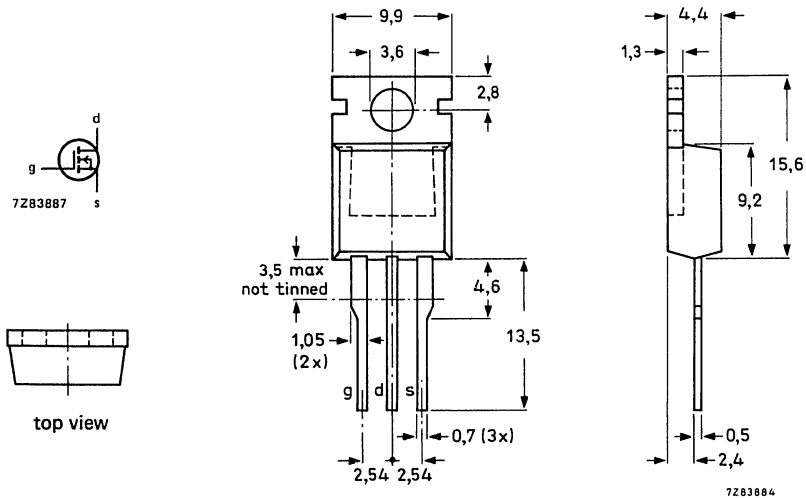
Drain-source voltage	$V_{DS}$	max.	50 V
Drain current (d.c.); $T_{mb} = 35\text{ }^{\circ}\text{C}$	$I_D$	max.	12 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	40 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,12 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	150 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

# BUZ71A

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	50 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	50 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 40 \text{ }^\circ\text{C}$	$I_D$	max.	12 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	36 A
Total power dissipation	$P_{tot}$	max.	40 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

## THERMAL CHARACTERISTICS

### Thermal resistance

From junction to mounting base	$R_{th \text{ j-mb}}$	=	3,1 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

## STATIC CHARACTERISTICS

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$$

$$V_{(BR)DSS} > 50 \text{ V}$$

Gate threshold voltage

$$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$$

$$V_{GST} \text{ typ. } 2,1 \text{ to } 4 \text{ V}$$

$$3 \text{ V}$$

Zero gate voltage drain current

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$$

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$$

$$I_{DSS} < 0,25 \text{ mA}$$

$$I_{DSS} < 1 \text{ mA}$$

Gate-source leakage current

$$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$$

$$I_{GSS} < 100 \text{ nA}$$

Drain-source on-state resistance

$$V_{GS} = 10 \text{ V}; I_D = 6 \text{ A}$$

$$R_{DS \text{ ON}} < 0,12 \text{ } \Omega$$

## Diode characteristics

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$$I_F < 12 \text{ A}$$

Forward current (peak value)

$$I_{FRM} < 36 \text{ A}$$

On-state voltage

$$I_F = 2 I_D; V_{GS} = 0 \text{ V}$$

$$V_F \text{ typ. } 1,6 \text{ V}$$

$$< 2,2 \text{ V}$$

Reverse recovery

$$I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$$

recovery time

$$t_{rr} \text{ typ. } 120 \text{ ns}$$

recovery charge

$$Q_s \text{ typ. } 0,15 \text{ } \mu\text{C}$$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 6 \text{ A}$

$g_{fs}$	>	3,0 A/V
	typ.	4,8 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	480 pF
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Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	280 pF
----------	------	--------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	160 pF
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Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

rise time

$t_{d \text{ on}}$	typ.	30 ns
--------------------	------	-------

$t_r$	typ.	100 ns
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turn-off times: delay time

fall time

$t_{d \text{ off}}$	typ.	200 ns
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$t_f$	typ.	150 ns
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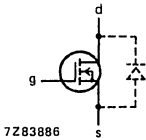


Fig. 2 Diode characteristics.

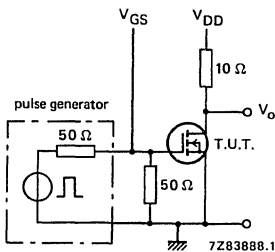


Fig. 3 Switching time test circuit.

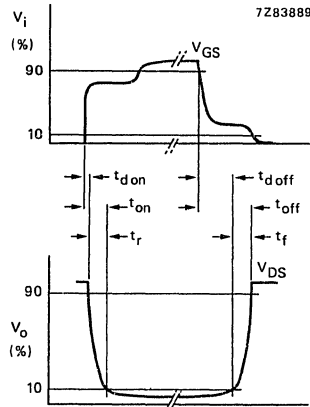


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

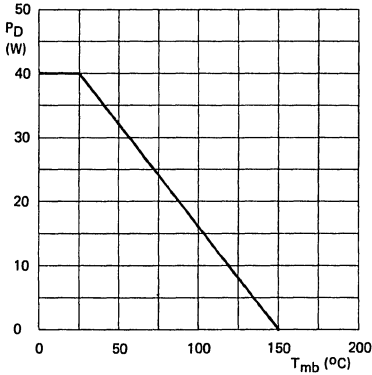


Fig. 5 Power derating curve.

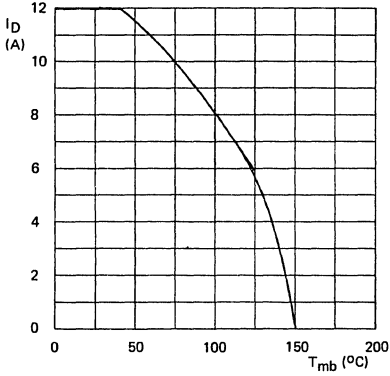


Fig. 7 Drain current as a function of mounting base temperature.

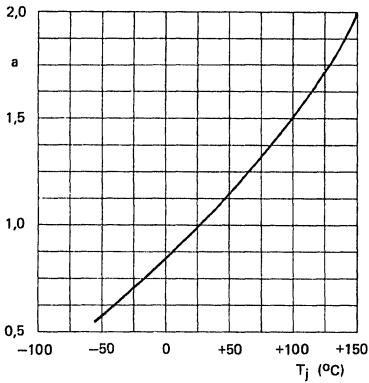


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25^\circ C)$ .

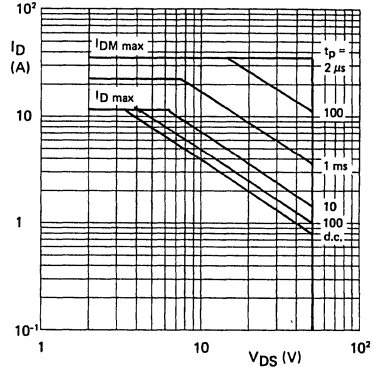


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25^\circ C; \delta = 0,01$ .

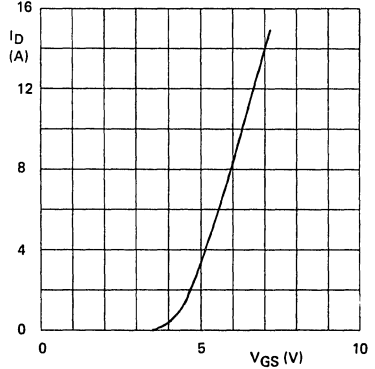


Fig. 8 Typical transfer characteristic at  $V_{DS} = 25\text{ V}$ .

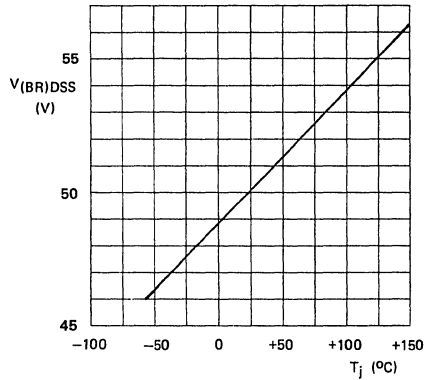


Fig. 10 Drain-source breakdown voltage as a function of junction temperature.

# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ72

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

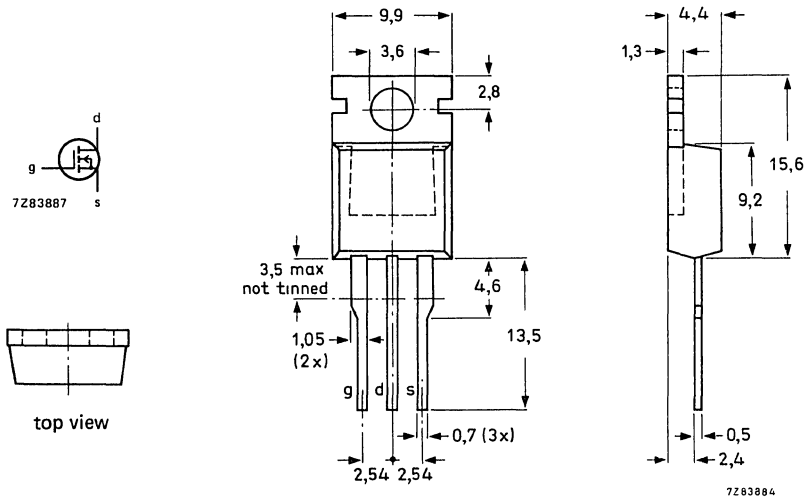
Drain-source voltage	$V_{DS}$	max.	100 V
Drain current (d.c.); $T_{mb} = 35\text{ }^{\circ}\text{C}$	$I_D$	max.	10 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	40 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,2 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,7\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	150 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	100 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	100 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	10 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	30 A
Total power dissipation	$P_{tot}$	max.	40 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	3,1 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	100 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$	$I_{DSS}$	<	0,25 mA
$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}$	$R_{DS \text{ ON}}$	<	0,2 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	10 A
Forward current (peak value)	$I_{FRM}$	<	30 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,55 V 2,1 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	170 ns
recovery time	$Q_s$	typ.	0,30 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 5 \text{ A}$

$g_{fs}$  > 2,7 A/V  
 typ. 3,8 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 440 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 150 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 80 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,9 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time  
 turn-off times: delay time  
 fall time

$t_{d \text{ on}}$  typ. 30 ns  
 $t_r$  typ. 100 ns  
 $t_{d \text{ off}}$  typ. 200 ns  
 $t_f$  typ. 150 ns

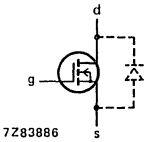


Fig. 2 Diode characteristics.

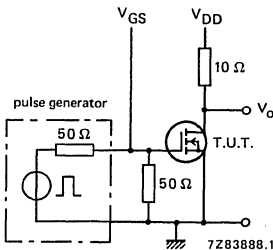


Fig. 3 Switching time test circuit.

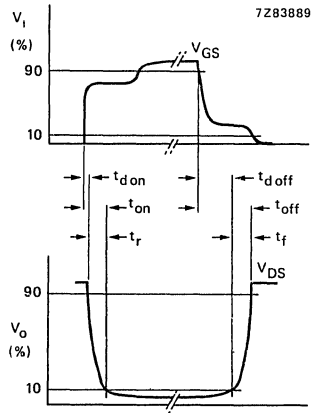


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

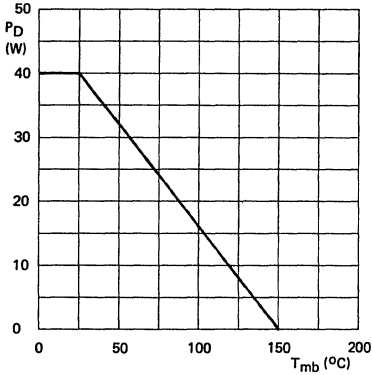


Fig. 5 Power derating curve.

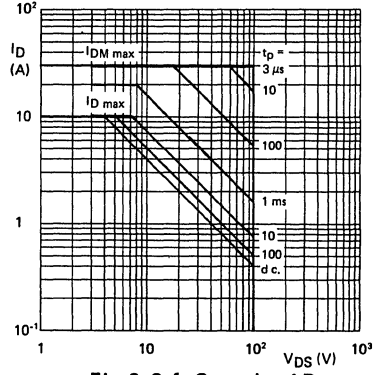


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25^\circ\text{C}; \delta = 0,01.$

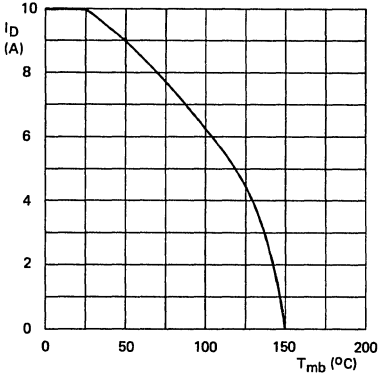


Fig. 7 Drain current as a function of mounting base temperature.

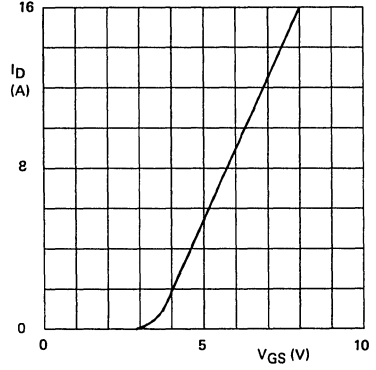


Fig. 8 Typical transfer characteristic at  $V_{DS} = 25\text{V}.$

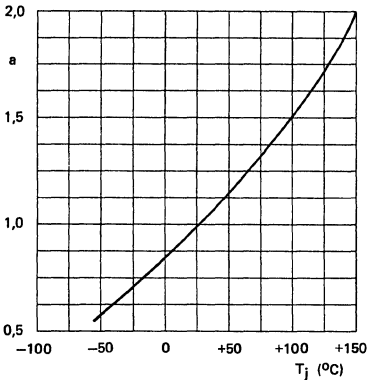


Fig. 9  $R_{DS\text{ ON}}(T_j) = a \times R_{DS\text{ ON}}(25^\circ\text{C}).$

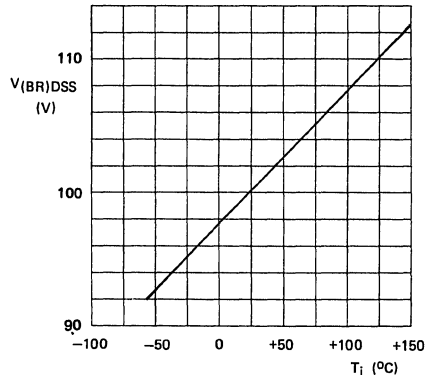


Fig. 10 Drain-source breakdown voltage as a function of junction temperature.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ72A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

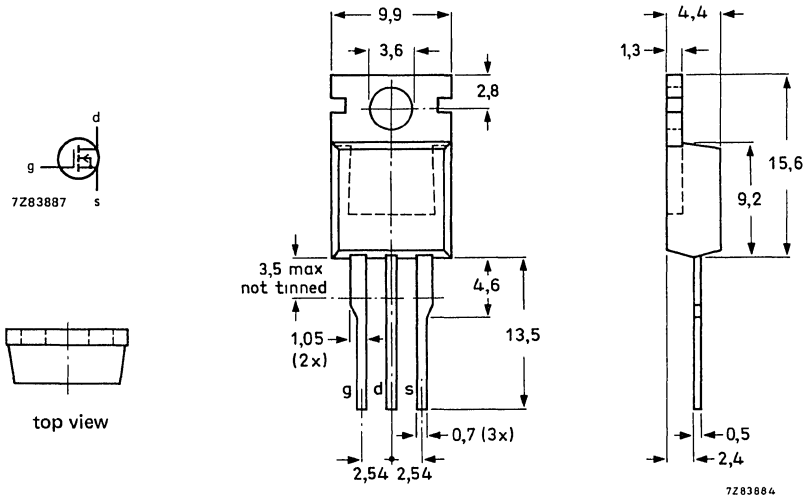
Drain-source voltage	$V_{DS}$	max.	100 V
Drain current (d.c.); $T_{mb} = 35\text{ }^{\circ}\text{C}$	$I_D$	max.	9 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	40 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,25 $\Omega$
Turn-off fall-time	$t_f$	typ.	150 ns
$V_{DD} = 30\text{ V}; I_D = 2,9\text{ A}; V_{GS} = 10\text{ V}$			

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	100 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	100 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	9 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	27 A
Total power dissipation	$P_{tot}$	max.	40 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	3,1 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	100 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	0,25 mA 1 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}$	$R_{DS \text{ ON}}$	<	0,25 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	9 A
Forward current (peak value)	$I_{FRM}$	<	27 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,5 V 2 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	170 ns
recovery time	$Q_s$	typ.	0,30 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 5 \text{ A}$

$g_{fs} >$  2,7 A/V  
 typ. 3,8 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 440 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 150 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 80 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,9 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 30 ns  
 $t_r$  typ. 100 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 200 ns  
 $t_f$  typ. 150 ns

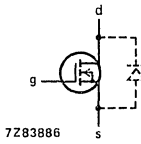


Fig. 2 Diode characteristics.

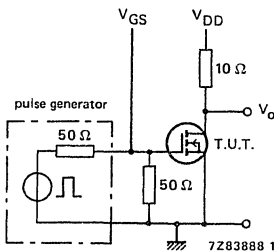


Fig. 3 Switching time test circuit.

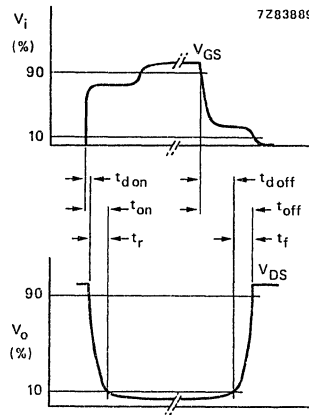


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

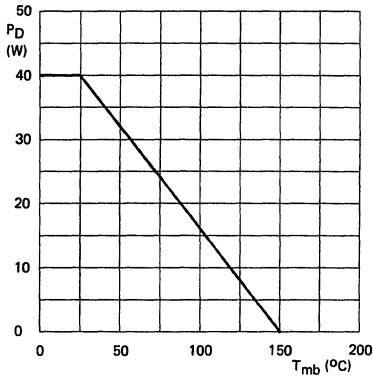


Fig. 5 Power derating curve.

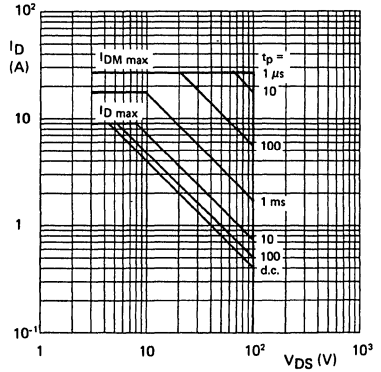


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

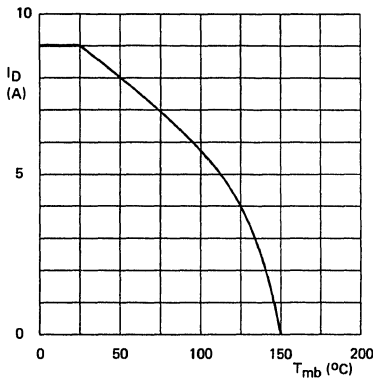


Fig. 7 Drain current as a function of mounting base temperature.

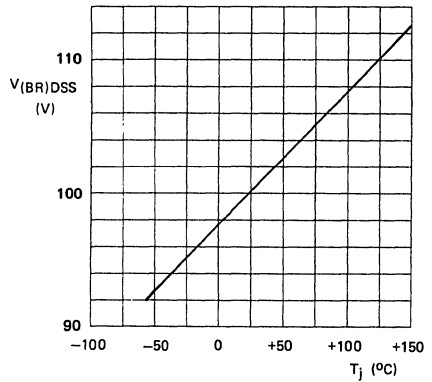


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

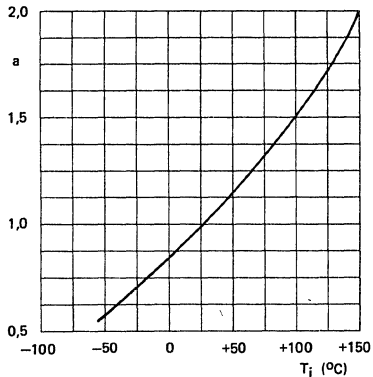


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^{\circ}\text{C})$ .

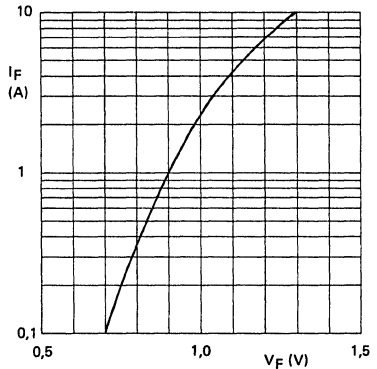


Fig. 10 Typical diode forward current as a function of forward voltage.  $t_p = 80\text{ }\mu\text{s}$ ;  $T_j = 25\text{ }^{\circ}\text{C}$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ73A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

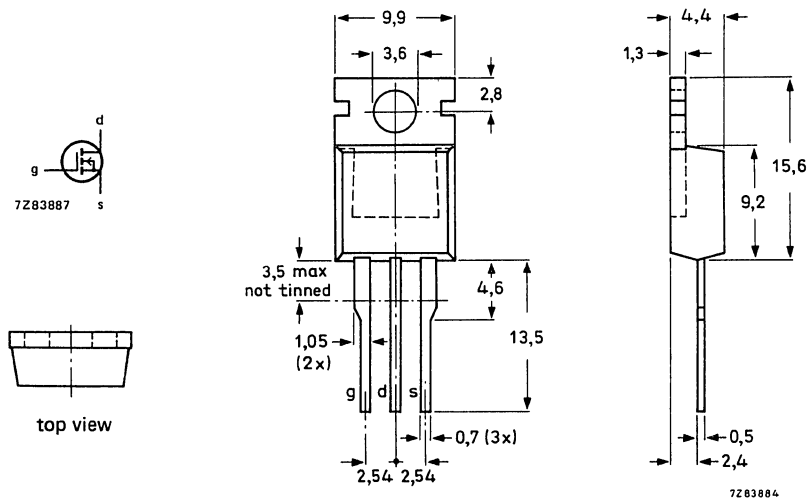
Drain-source voltage	$V_{DS}$	max.	200 V
Drain current (d.c.); $T_{mb} = 35\text{ }^{\circ}\text{C}$	$I_D$	max.	5,8 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	40 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	0,6 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,8\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	130 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	200 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	200 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	5,8 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	17 A
Total power dissipation	$P_{tot}$	max.	40 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature-	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	3,1 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	200 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	0,25 mA 1 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 3,5 \text{ A}$	$R_{DS \text{ ON}}$	<	0,6 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	5,8 A
Forward current (peak value)	$I_{FRM}$	<	17 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,4 V 1,7 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	200 ns
recovery time	$Q_s$	typ.	0,6 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 3,5 \text{ A}$

9fs > 2,2 A/V  
typ. 3,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 450 pF

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 120 pF

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 60 pF

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,8 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

rise time

$t_{d \text{ on}}$  typ. 30 ns

$t_r$  typ. 100 ns

turn-off times: delay time

fall time

$t_{d \text{ off}}$  typ. 190 ns

$t_f$  typ. 130 ns

DEVELOPMENT SAMPLE DATA

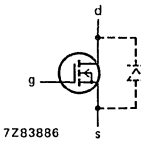


Fig. 2 Diode characteristics.

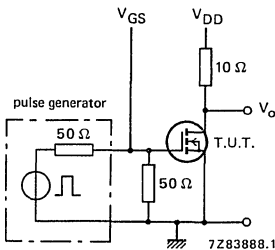


Fig. 3 Switching time test circuit.

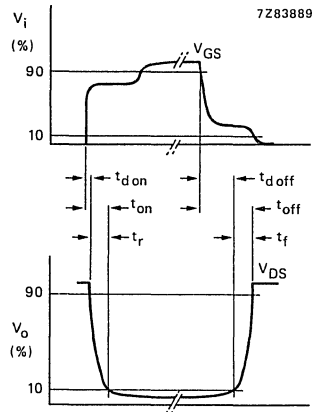


Fig. 4 Switching time waveforms.

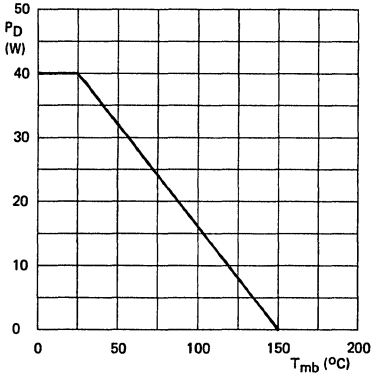


Fig. 5 Power derating curve.

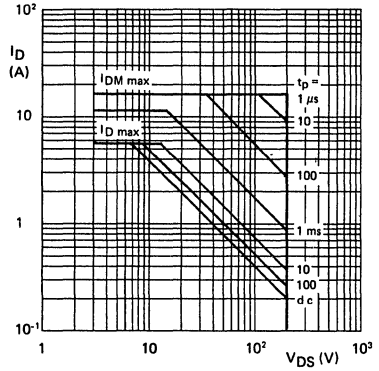


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25^\circ\text{C}$ ;  $\delta = 0,01$ .

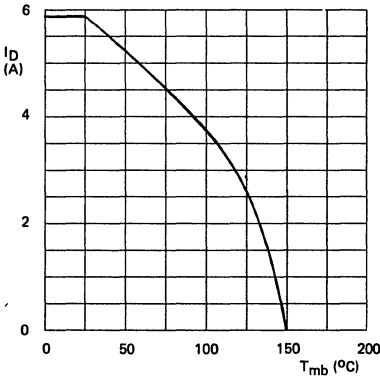


Fig. 7 Drain current as a function of mounting base temperature.

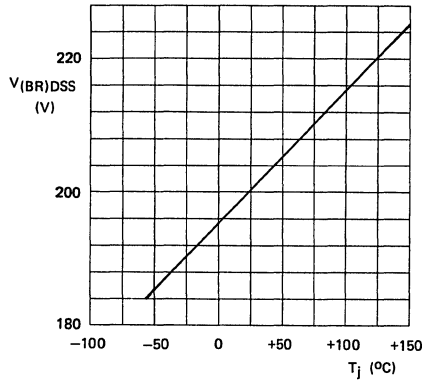


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

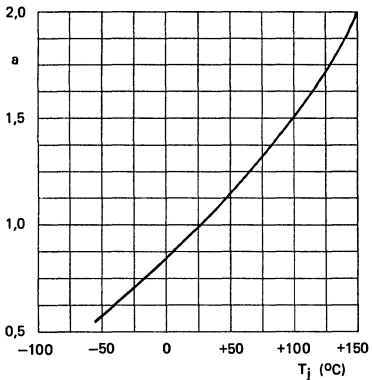


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25^\circ\text{C})$ .

# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ74

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

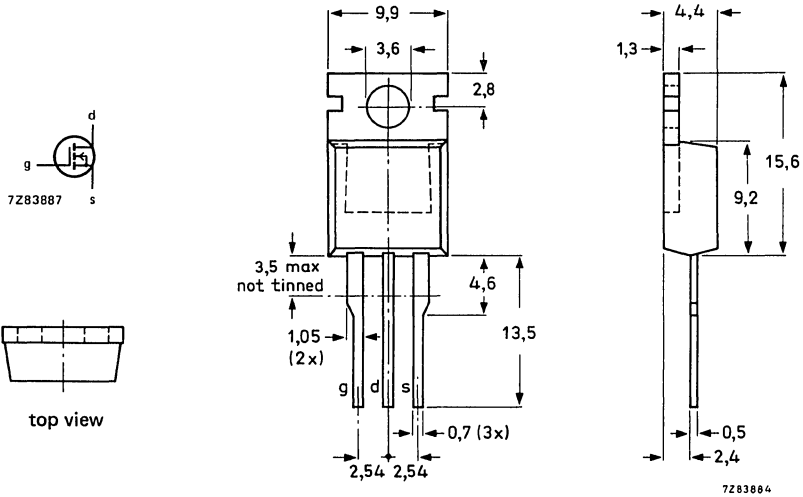
Drain-source voltage	$V_{DS}$	max.	500 V
Drain current (d.c.); $T_{mb} = 35\text{ }^{\circ}\text{C}$	$I_D$	max.	2,4 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	40 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	3 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	500 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	500 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 35 \text{ }^\circ\text{C}$	$I_D$	max.	2,4 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	7 A
Total power dissipation	$P_{tot}$	max.	40 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	3,1 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	500 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	0,25 mA 1 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 1,2 \text{ A}$	$R_{DS \text{ ON}}$	typ. <	2,6 $\Omega$ 3,0 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	2,4 A
Forward current (peak value)	$I_{FRM}$	<	7 A
On-state voltage $I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1 V 1,3 V
Reverse recovery $I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	350 ns
recovery time	$Q_s$	typ.	3,5 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 1,2 \text{ A}$

$g_{fs}$  typ. 2,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 350 pF

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 50 pF

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 20 pF

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

rise time

$t_{d\ on}$  typ. 30 ns

$t_r$  typ. 100 ns

turn-off times: delay time

fall time

$t_{d\ off}$  typ. 150 ns

$t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

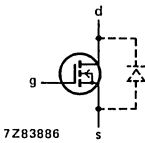


Fig. 2 Diode characteristics.

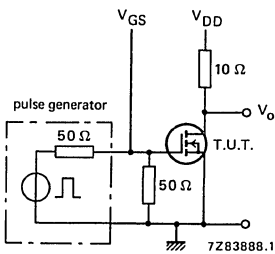


Fig. 3 Switching time test circuit.

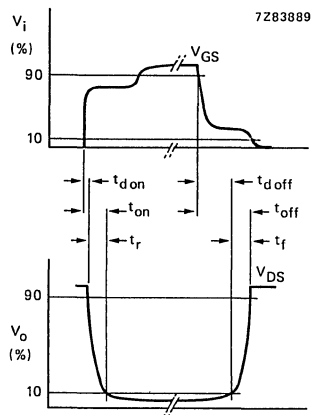


Fig. 4 Switching time waveforms.

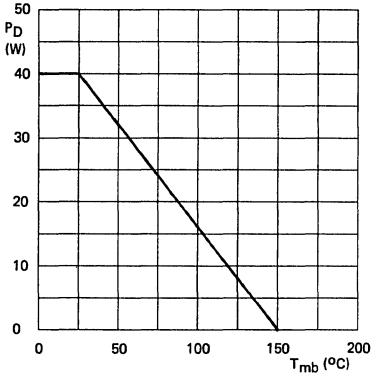


Fig. 5 Power derating curve.

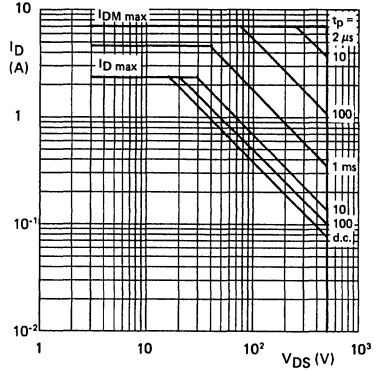


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

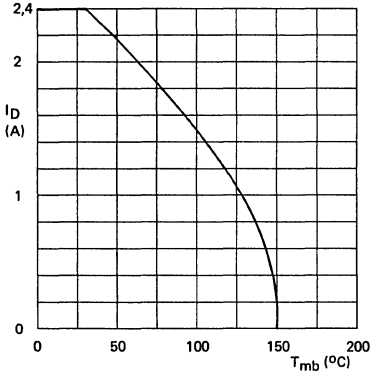


Fig. 7 Drain current as a function of mounting base temperature.

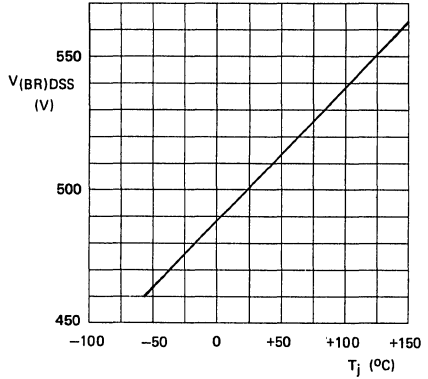


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

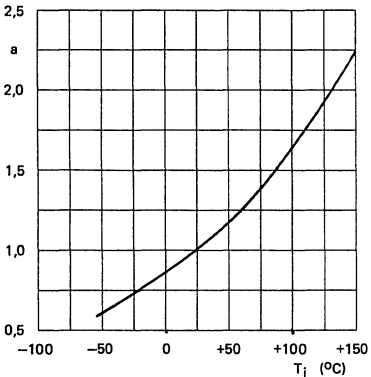


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^\circ\text{C})$ .

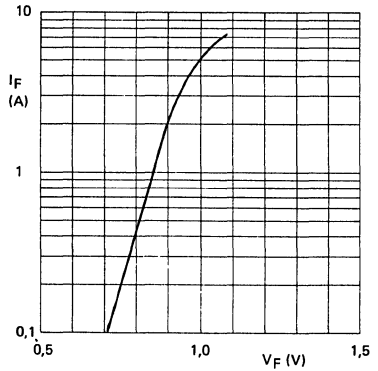


Fig. 10 Diode forward current as a function of forward voltage.  $t_p = 80\text{ }\mu\text{s}$ ;  $T_j = 25\text{ }^\circ\text{C}$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ74A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

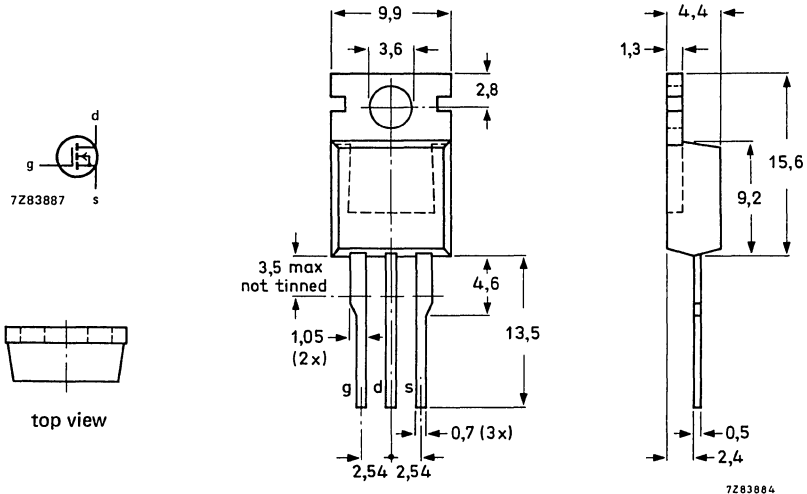
Drain-source voltage	$V_{DS}$	max.	500 V
Drain current (d.c.); $T_{mb} = 35\text{ }^{\circ}\text{C}$	$I_D$	max.	2 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	40 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	4 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}$ ; $I_D = 2,1\text{ A}$ ; $V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Fig. 1 TO-220AB.

Drain connected to mounting base.

Dimensions in mm



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	500 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	500 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 35 \text{ }^\circ\text{C}$	$I_D$	max.	2 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	6 A
Total power dissipation	$P_{tot}$	max.	40 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+150 $^\circ\text{C}$

## THERMAL CHARACTERISTICS

### Thermal resistance

From junction to mounting base	$R_{th \text{ j-mb}}$	=	3,1 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

## STATIC CHARACTERISTICS

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$$V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$$

$$V_{(BR)DSS} > 500 \text{ V}$$

Gate threshold voltage

$$V_{DS} = V_{GS}; I_D = 10 \text{ mA}$$

$$V_{GST} \text{ typ. } 2,1 \text{ to } 4 \text{ V}$$

$$3 \text{ V}$$

Zero gate voltage drain current

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$$

$$V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$$

$$I_{DSS} < 0,25 \text{ mA}$$

$$I_{DSS} < 1 \text{ mA}$$

Gate-source leakage current

$$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$$

$$I_{GSS} < 100 \text{ nA}$$

Drain-source on-state resistance

$$V_{GS} = 10 \text{ V}; I_D = 1,2 \text{ A}$$

$$R_{DS \text{ ON}} \text{ typ. } 3,6 \text{ } \Omega$$

$$< 4,0 \text{ } \Omega$$

## Diode characteristics

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current

$$I_F < 2 \text{ A}$$

Forward current (peak value)

$$I_{FRM} < 6 \text{ A}$$

On-state voltage

$$I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$$

$$V_F \text{ typ. } 1 \text{ V}$$

$$< 1,3 \text{ V}$$

Reverse recovery

$$I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$$

recovery time

$$t_{rr} \text{ typ. } 350 \text{ ns}$$

recovery charge

$$Q_s \text{ typ. } 3,5 \text{ } \mu\text{C}$$

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 1,2 \text{ A}$

$g_{fs}$  typ. 2,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 350 pF

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 50 pF

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 20 pF

Switching times (see Figs 3 and 4)  
(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,1 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
rise time

$t_{d \text{ on}}$  typ. 30 ns  
 $t_r$  typ. 100 ns

turn-off times: delay time  
fall time

$t_{d \text{ off}}$  typ. 150 ns  
 $t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

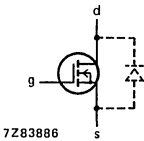


Fig. 2 Diode characteristics.

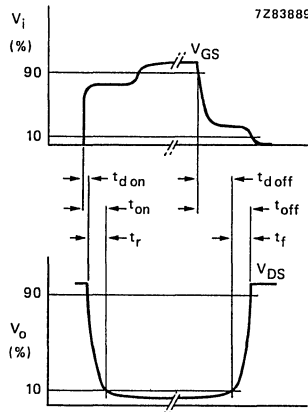


Fig. 4 Switching time waveforms.

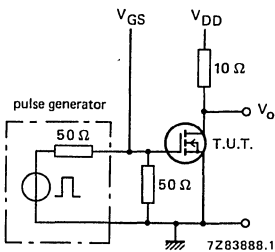


Fig. 3 Switching time test circuit.

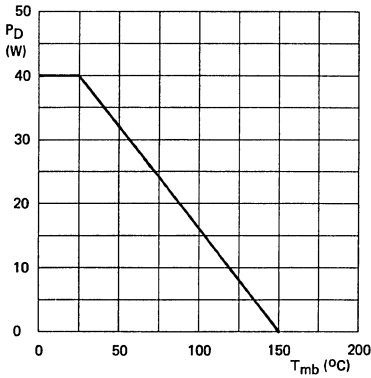


Fig. 5 Power derating curve.

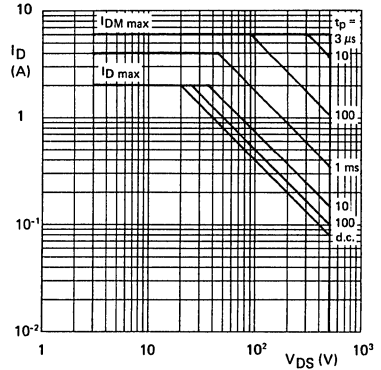


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

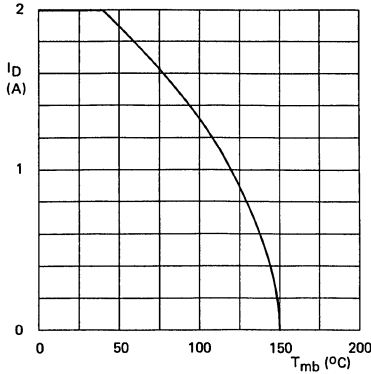


Fig. 7 Drain current as a function of mounting base temperature.

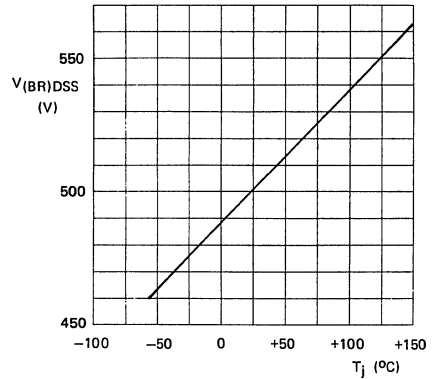


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

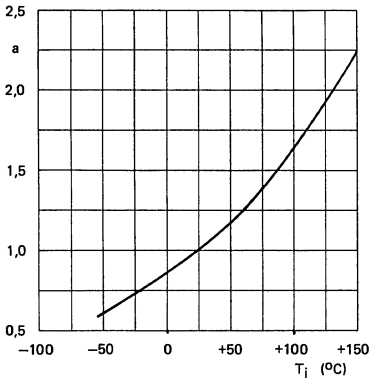


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^{\circ}\text{C})$ .

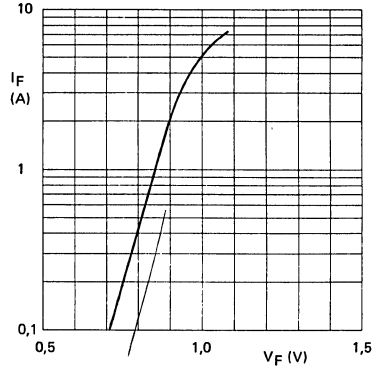


Fig. 10 Diode forward current as a function of forward voltage.  $t_p = 80\text{ }\mu\text{s}$ ;  $T_j = 25\text{ }^{\circ}\text{C}$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ76

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

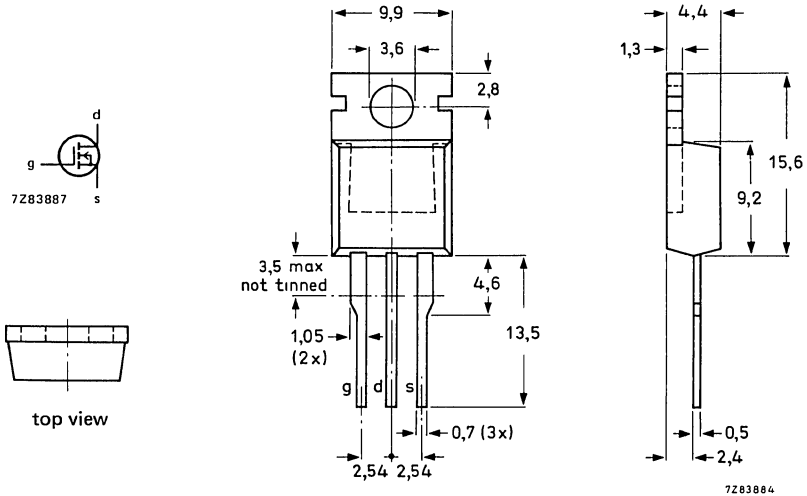
Drain-source voltage	$V_{DS}$	max.	400 V
Drain current (d.c.); $T_{mb} = 35\text{ }^{\circ}\text{C}$	$I_D$	max.	3 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	40 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	1,8 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}$ ; $I_D = 2,5\text{ A}$ ; $V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	400 V
Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	$V_{DGR}$	max.	400 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 35\text{ }^\circ\text{C}$	$I_D$	max.	3 A
Drain current (pulse peak value); $T_{mb} = 25\text{ }^\circ\text{C}$	$I_{DM}$	max.	9 A
Total power dissipation	$P_{tot}$	max.	40 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th\ j-mb}$	=	3,1 K/W
From junction to ambient	$R_{th\ j-a}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0\text{ V}; I_D = 1\text{ mA}$	$V_{(BR)DSS}$	>	400 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10\text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25\text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125\text{ }^\circ\text{C}$	$I_{DSS}$	<	0,25 mA 1 mA
Gate-source leakage current $V_{GS} = 20\text{ V}; V_{DS} = 0\text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10\text{ V}; I_D = 1,5\text{ A}$	$R_{DS\ ON}$	<	1,8 $\Omega$

**Diode characteristics**

$T_{mb} = 25\text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	3 A
Forward current (peak value)	$I_{FRM}$	<	9 A
On-state voltage $I_F = 2\text{ I}_D; V_{GS} = 0\text{ V}$	$V_F$	typ. <	1,1 V 1,4 V
Reverse recovery $I_F = 2\text{ I}_D; dI_F/dt = 100\text{ A}/\mu\text{s}$	$t_{rr}$	typ.	300 ns
recovery time	$Q_s$	typ.	2,5 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 1,5 \text{ A}$

$g_{fs}$  typ. 2,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 420 pF

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 60 pF

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 25 pF

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,5 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$  typ. 30 ns

rise time

$t_r$  typ. 100 ns

turn-off times: delay time

$t_{d \text{ off}}$  typ. 150 ns

fall time

$t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

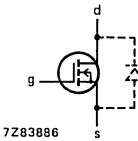


Fig. 2 Diode characteristics.

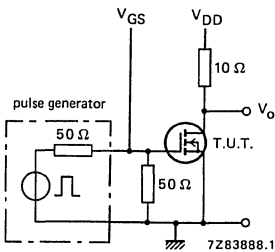


Fig. 3 Switching time test circuit.

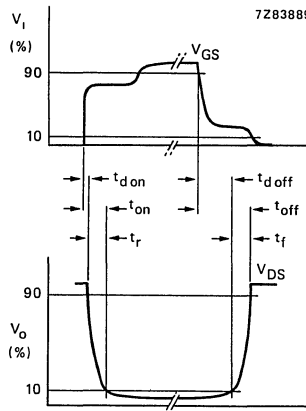


Fig. 4 Switching time waveforms.

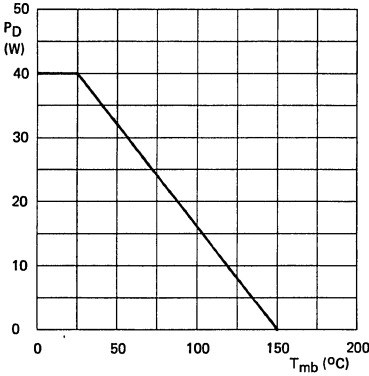


Fig. 5 Power derating curve.

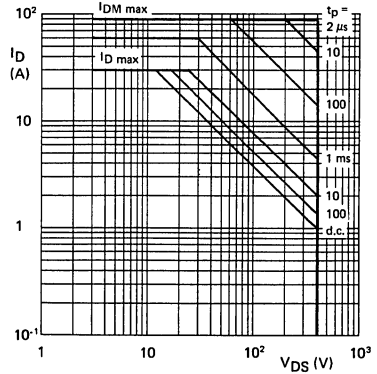


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25^\circ\text{C}$ ;  $\delta = 0,01$ .

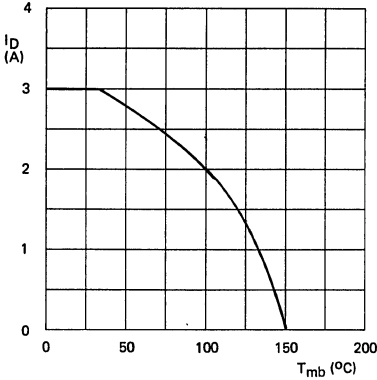


Fig. 7 Drain current as a function of mounting base temperature.

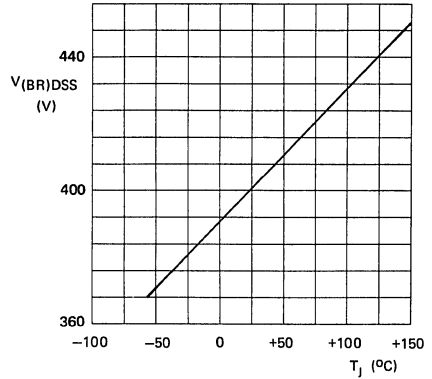


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

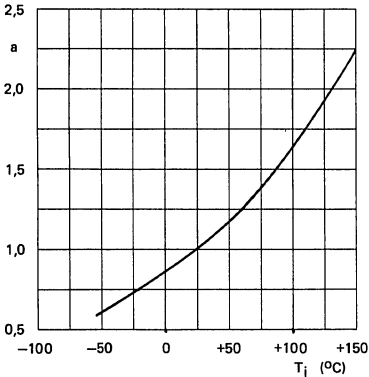


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25^\circ\text{C})$ .

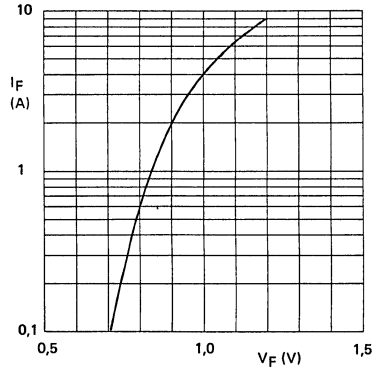


Fig. 10 Diode forward current as a function of forward voltage.  $t_p = 80\ \mu\text{s}$ ;  $T_j = 25^\circ\text{C}$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ76A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

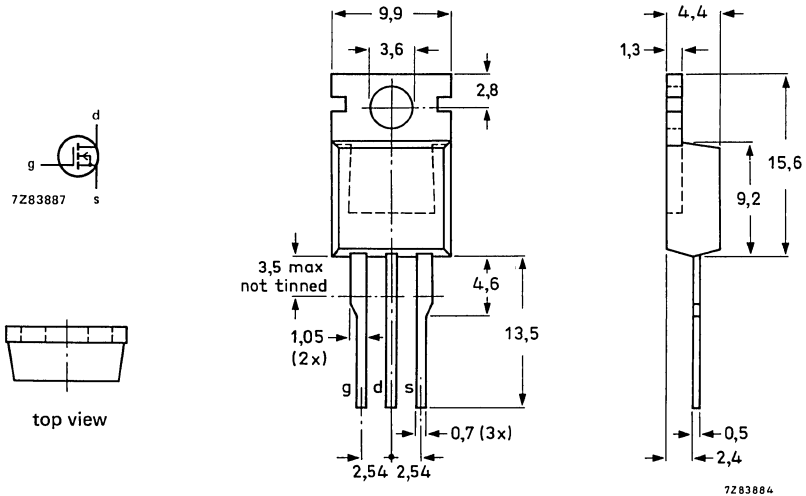
Drain-source voltage	$V_{DS}$	max.	400 V
Drain current (d.c.); $T_{mb} = 35\text{ }^{\circ}\text{C}$	$I_D$	max.	2,6 A
Total power dissipation; $T_{mb} = 25\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	40 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	2,5 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,4\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	400 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	400 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 35 \text{ }^\circ\text{C}$	$I_D$	max.	2,6 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	7,5 A
Total power dissipation	$P_{tot}$	max.	40 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	3,1 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	400 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	0,25 mA 1 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 1,5 \text{ A}$	$R_{DS \text{ ON}}$	typ. <	2,2 $\Omega$ 2,5 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	2,6 A
Forward current (peak value)	$I_{FRM}$	<	7,5 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,1 V 1,4 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	300 ns
recovery time	$Q_s$	typ.	2,5 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 1,5 \text{ A}$

$g_{fs}$  typ. 2,5 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 420 pF

Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 60 pF

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 25 pF

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,4 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

rise time

$t_{d \text{ on}}$  typ. 30 ns

$t_r$  typ. 100 ns

turn-off times: delay time

fall time

$t_{d \text{ off}}$  typ. 150 ns

$t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

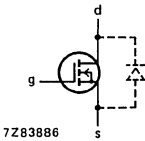


Fig. 2 Diode characteristics.

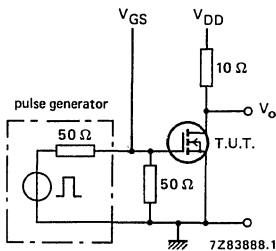


Fig. 3 Switching time test circuit.

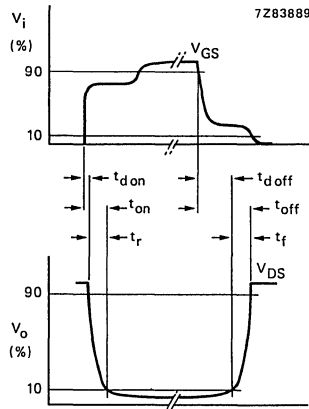


Fig. 4 Switching time waveforms.

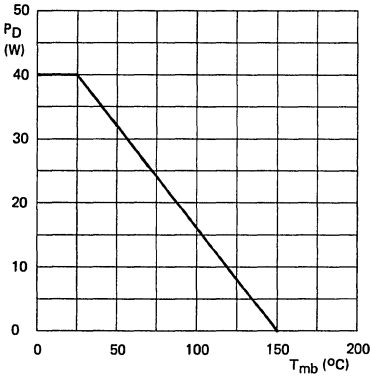


Fig. 5 Power derating curve.

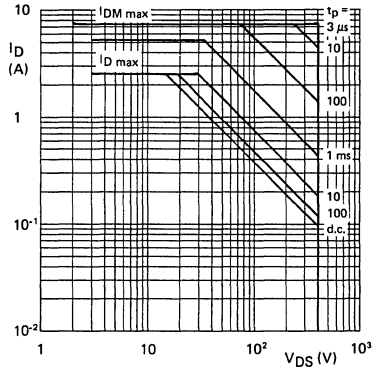


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25^\circ\text{C}$ ;  $\delta = 0,01$ .

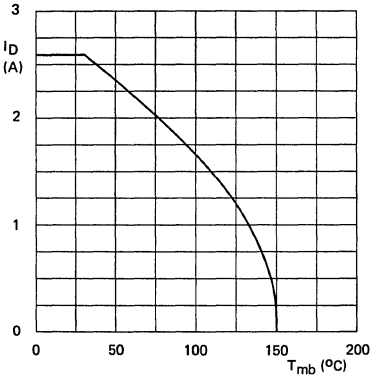


Fig. 7 Drain current as a function of mounting base temperature.

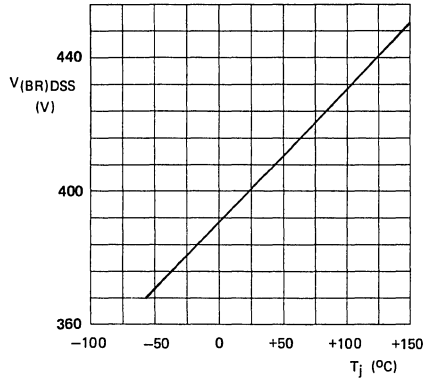


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

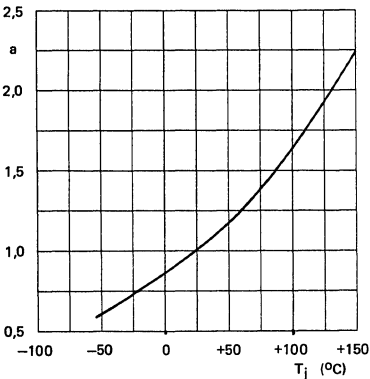


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25^\circ\text{C})$ .

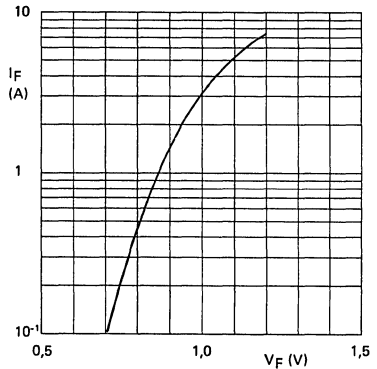


Fig. 10 Diode forward current as a function of forward voltage.  $t_p = 80 \mu\text{s}$ ;  $T_j = 25^\circ\text{C}$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ80

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

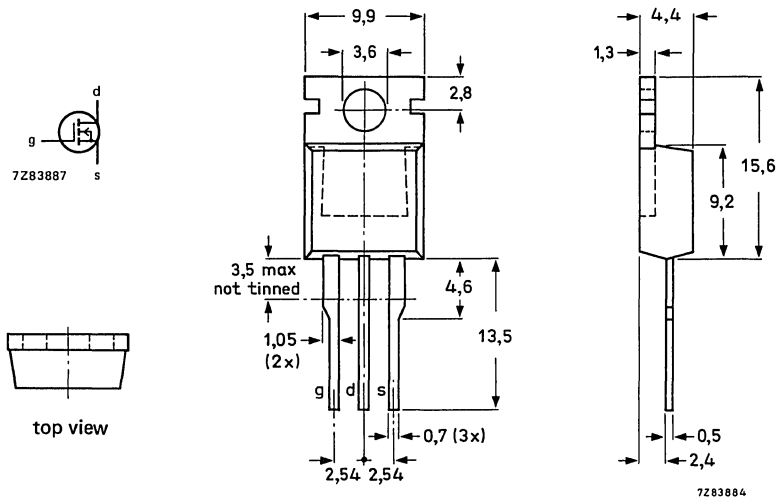
Drain-source voltage	$V_{DS}$	max.	800 V
Drain current (d.c.)	$I_D$	max.	2,6 A
Total power dissipation	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	4 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,1\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	800 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	800 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 45 \text{ }^\circ\text{C}$	$I_D$	max.	2,6 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	7,5 A
Total power dissipation	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	800 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 1,5 \text{ A}$	$R_{DS \text{ ON}}$	<	4 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	2,6 A
Forward current (peak value)	$I_{FRM}$	<	7,5 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,05 V 1,3 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1800 ns
recovery time	$Q_s$	typ.	12 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 1,5 \text{ A}$

$g_{fs} > 1,0 \text{ A/V}$   
 typ. 1,8 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1600 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{OS}$  typ. 90 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 30 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,1 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time  
 turn-off times: delay time  
 fall time

$t_{d \text{ on}}$  typ. 40 ns  
 $t_r$  typ. 70 ns  
 $t_{d \text{ off}}$  typ. 200 ns  
 $t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

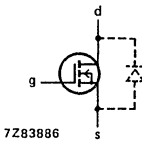


Fig. 2 Diode characteristics.

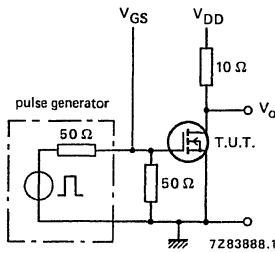


Fig. 3 Switching time test circuit.

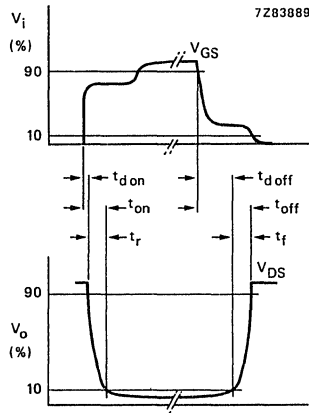


Fig. 4 Switching time waveforms.

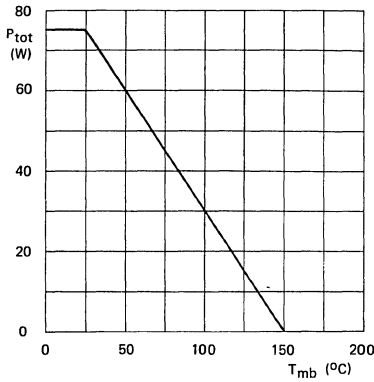


Fig. 5 Power derating curve.

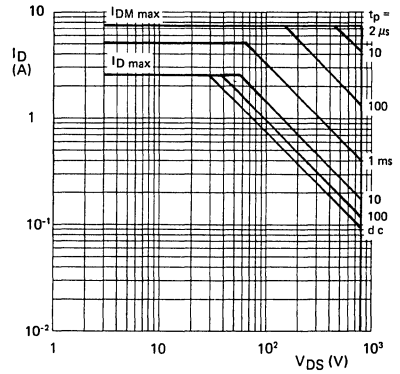


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

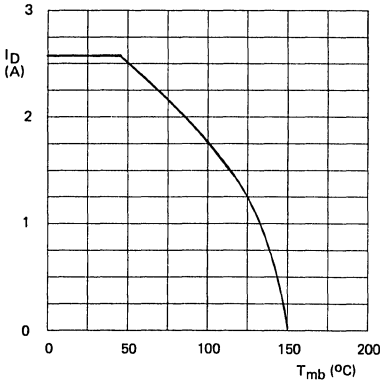


Fig. 7 Drain current as a function of mounting base temperature.

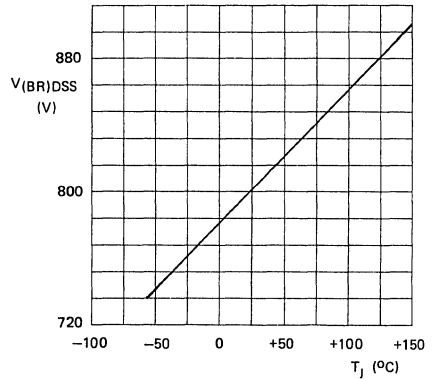


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

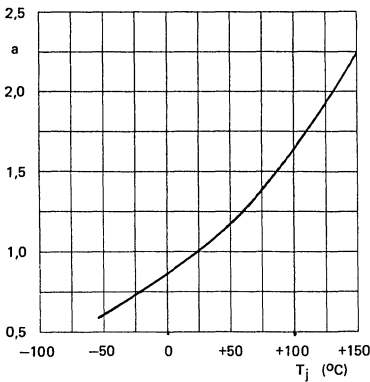


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^\circ\text{C})$ .

# DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ80A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a plastic envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

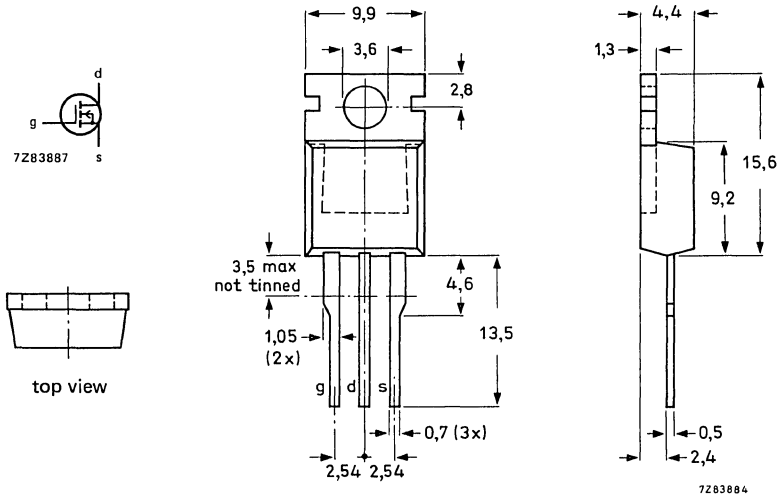
Drain-source voltage	$V_{DS}$	max.	800 V
Drain current (d.c.)	$I_D$	max.	3 A
Total power dissipation; $T_{mb} = 25\text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	3 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,3\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-220AB.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	800 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	800 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 45 \text{ }^\circ\text{C}$	$I_D$	max.	3 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	9 A
Total power dissipation; $T_{mb} = 25 \text{ }^\circ\text{C}$	$P_{tot}$	max.	75 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,67 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	75 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	800 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 1,5 \text{ A}$	$R_{DS \text{ ON}}$	<	3 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	3 A
Forward current (peak value)	$I_{FRM}$	<	9 A
On-state voltage $I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}$	$V_F$	typ.	1,05 V
		<	1,3 V
Reverse recovery $I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1800 ns
recovery time	$Q_s$	typ.	12 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 1,5 \text{ A}$

$g_{fs} > 1,0 \text{ A/V}$   
 typ. 1,8 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1600 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 90 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 30 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 40 ns

$t_r$  typ. 70 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 200 ns

$t_f$  typ. 100 ns

DEVELOPMENT SAMPLE DATA

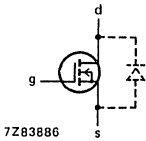


Fig. 2 Diode characteristics.

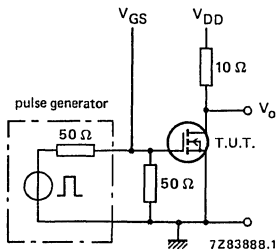


Fig. 3 Switching time test circuit.

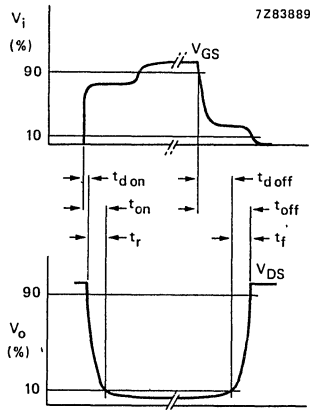


Fig. 4 Switching time waveforms.

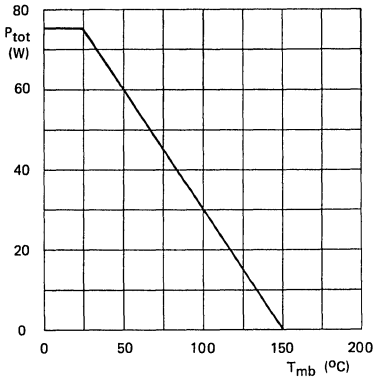


Fig. 5 Power derating curve.

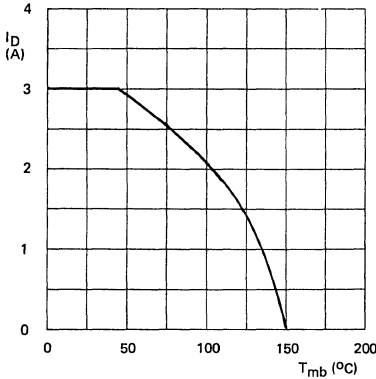


Fig. 7 Drain current as a function of mounting base temperature.

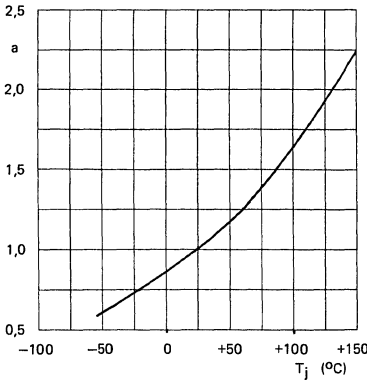


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\ ^\circ C)$ .

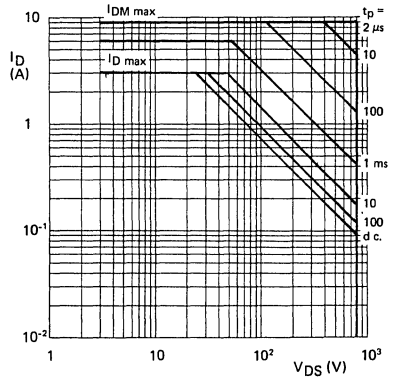


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\ ^\circ C; \delta = 0,01$ .

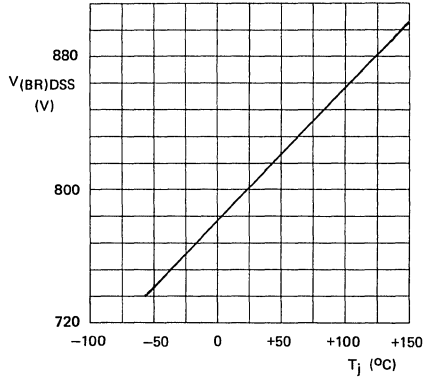


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ83

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

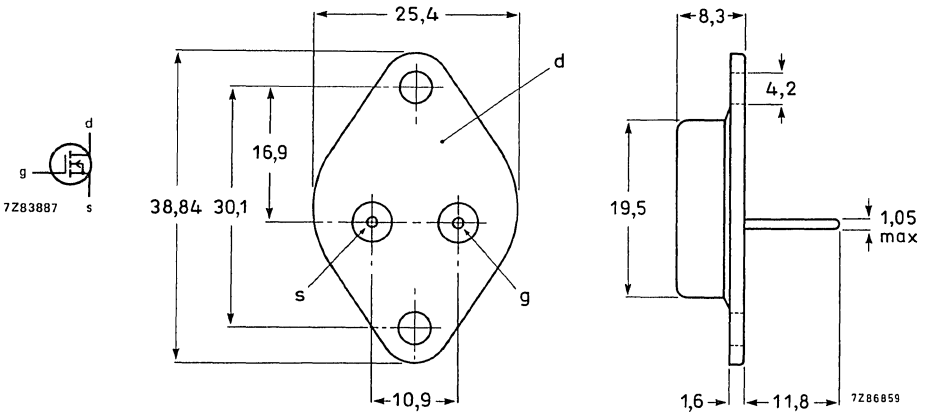
Drain-source voltage	$V_{DS}$	max.	800 V
Drain current (d.c.)	$I_D$	max.	2,9 A
Total power dissipation	$P_{tot}$	max.	78 W
Drain-source resistance (on)	$R_{DS ON}$	<	4 $\Omega$
Turn-off fall-time $V_{DD} = 30 V; I_D = 2,1 A; V_{GS} = 10 V$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

## RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	800 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	800 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 30 \text{ }^\circ\text{C}$	$I_D$	max.	2,9 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	8,5 A
Total power dissipation	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

## THERMAL CHARACTERISTICS

### Thermal resistance

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

## STATIC CHARACTERISTICS

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	800 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA
	$I_{DSS}$	<	4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 1,5 \text{ A}$	$R_{DS \text{ ON}}$	<	4 $\Omega$

## Diode characteristics

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	2,9 A
Forward current (peak value)	$I_{FRM}$	<	8,5 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ.	1,05 V
		<	1,3 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1800 ns
recovery time	$Q_s$	typ.	12 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance  
 $V_{DS} = 25 \text{ V}; I_D = 1,5 \text{ A}$

$g_{fs} > 1,0 \text{ A/V}$   
 typ. 1,8 A/V

Input capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$  typ. 1600 pF

Output capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$  typ. 90 pF

Feedback capacitance at  $f = 1 \text{ MHz}$   
 $V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$  typ. 30 pF

Switching times (see Figs 3 and 4)  
 (between 10% and 90% levels)  
 $V_{DD} = 30 \text{ V}; I_D = 2,1 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time  
 rise time

$t_{d \text{ on}}$  typ. 40 ns  
 $t_r$  typ. 70 ns

turn-off times: delay time  
 fall time

$t_{d \text{ off}}$  typ. 200 ns  
 $t_f$  typ. 100 ns

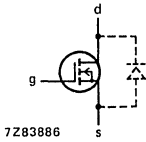


Fig. 2 Diode characteristics.

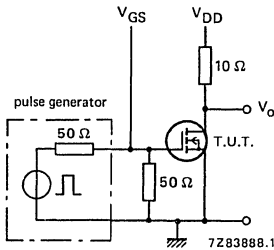


Fig. 3 Switching time test circuit.

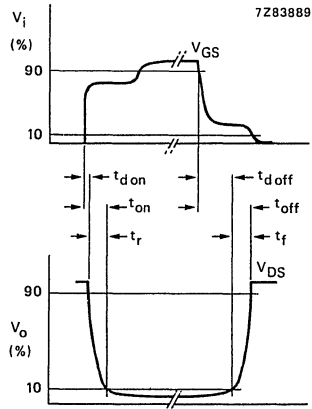


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

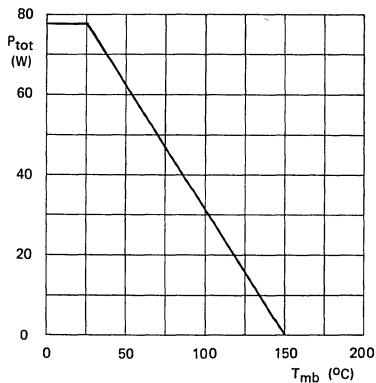


Fig. 5 Power derating curve.

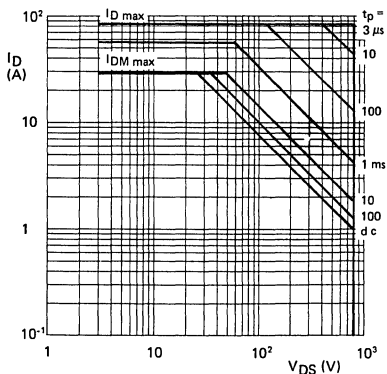


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

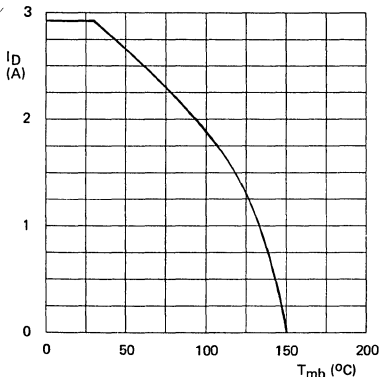


Fig. 7 Drain current as a function of mounting base temperature.

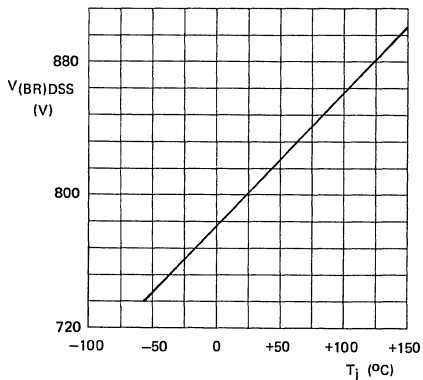


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

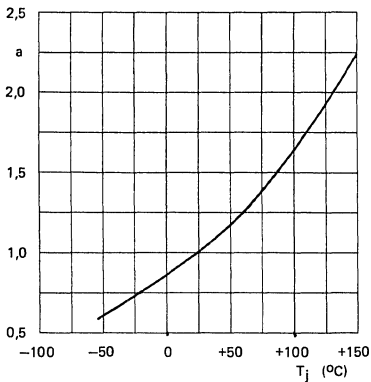


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^{\circ}\text{C})$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ83A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

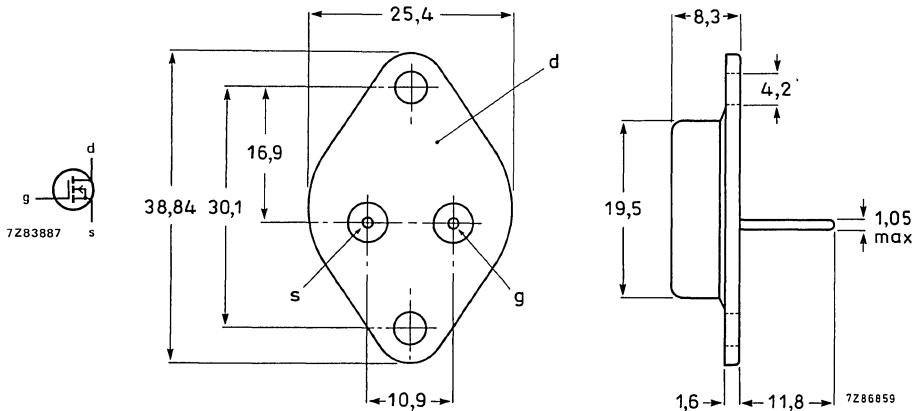
Drain-source voltage	$V_{DS}$	max.	800 V
Drain current (d.c.)	$I_D$	max.	3,4 A
Total power dissipation	$P_{tot}$	max.	78 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	3 $\Omega$
Turn-off fall-time	$t_f$	typ.	100 ns
$V_{DD} = 30\text{ V}; I_D = 2,3\text{ A}; V_{GS} = 10\text{ V}$			

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	800 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	800 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	3,4 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	10 A
Total power dissipation	$P_{tot}$	max.	78 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1,6 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	800 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 1,5 \text{ A}$	$R_{DS \text{ ON}}$	<	3 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	3,4 A
Forward current (peak value)	$I_{FRM}$	<	10 A
On-state voltage $I_F = 2 I_D; V_{GS} = 0 \text{ V}$	$V_F$	typ. <	1,1 V 1,35 V
Reverse recovery $I_F = 2 I_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1800 ns
recovery time	$Q_s$	typ.	12 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 1,5 \text{ A}$

$g_{fs}$	>	1,0 A/V
	typ.	1,8 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	1600 pF
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Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	90 pF
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Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	30 pF
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Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,3 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	40 ns
--------------------	------	-------

rise time

$t_r$	typ.	70 ns
-------	------	-------

turn-off times: delay time

$t_{d \text{ off}}$	typ.	200 ns
---------------------	------	--------

fall time

$t_f$	typ.	100 ns
-------	------	--------

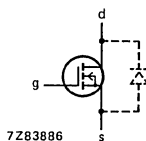


Fig. 2 Diode characteristics.

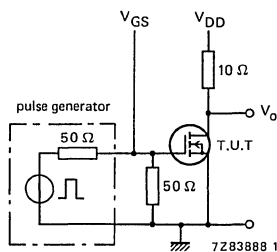


Fig. 3 Switching time test circuit.

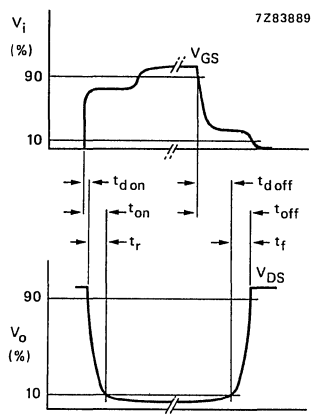


Fig. 4 Switching time waveforms.



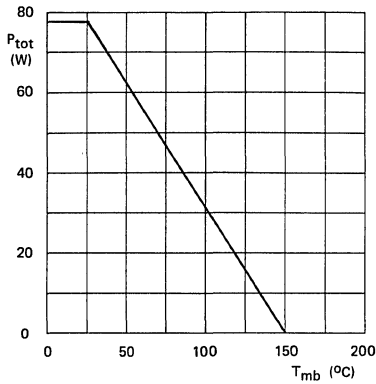


Fig. 5 Power derating curve.

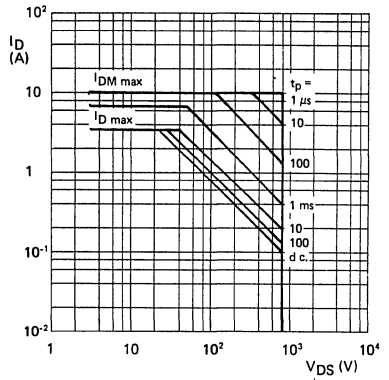


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^{\circ}\text{C}$ ;  $\delta = 0,01$ .

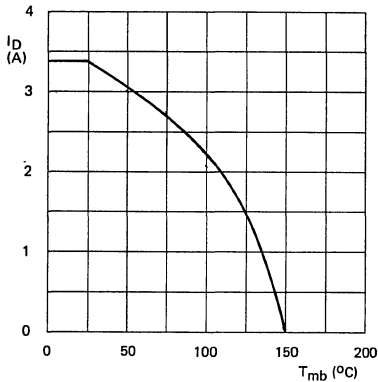


Fig. 7 Drain current as a function of mounting base temperature.

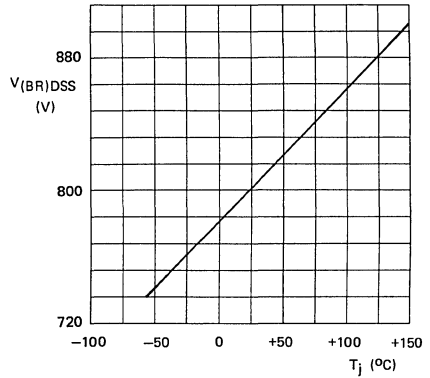


Fig. 8 Drain-source breakdown voltage as a function of junction temperature.

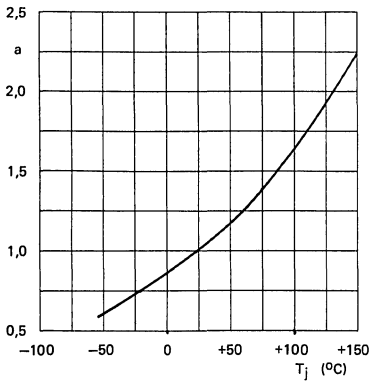


Fig. 9  $R_{DS\ ON}(T_j) = a \times R_{DS\ ON}(25\text{ }^{\circ}\text{C})$ .

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ84

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

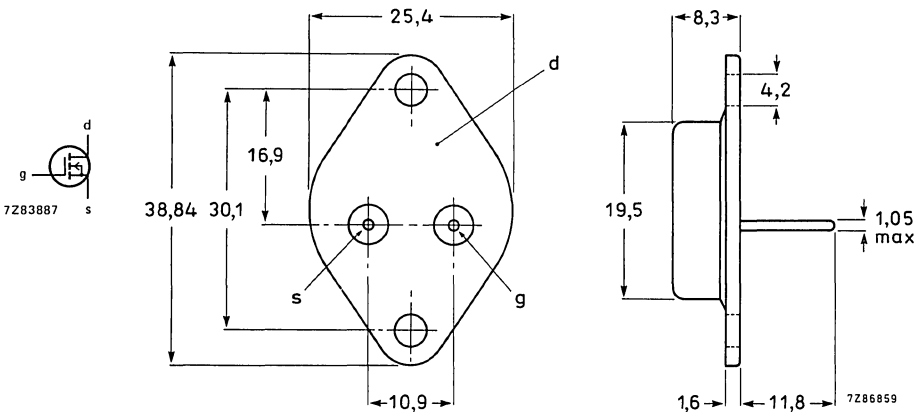
Drain-source voltage	$V_{DS}$	max.	800 V
Drain current (d.c.)	$I_D$	max.	5,3 A
Total power dissipation	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS\ ON}$	<	2 $\Omega$
Turn-off fall-time $V_{DD} = 30\text{ V}; I_D = 2,5\text{ A}; V_{GS} = 10\text{ V}$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	800 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	800 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	5,3 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	15 A
Total power dissipation	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to + 150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+ 150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	800 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 3 \text{ A}$	$R_{DS \text{ ON}}$	<	2 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	5,3 A
Forward current (peak value)	$I_{FRM}$	<	15 A
On-state voltage $I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	$V_F$	typ. <	1 V 1,45 V
Reverse recovery $I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}$	$t_{rr}$	typ.	1800 ns
recovery time	$Q_s$	typ.	25 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$V_{DS} = 25 \text{ V}; I_D = 3 \text{ A}$

$g_{fs}$	>	1,8 A/V
	typ.	3 A/V

Input capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{is}$	typ.	3500 pF
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Output capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{os}$	typ.	200 pF
----------	------	--------

Feedback capacitance at  $f = 1 \text{ MHz}$

$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$

$C_{rs}$	typ.	100 pF
----------	------	--------

Switching times (see Figs 3 and 4)

(between 10% and 90% levels)

$V_{DD} = 30 \text{ V}; I_D = 2,5 \text{ A}; V_{GS} = 10 \text{ V}$

turn-on times: delay time

$t_{d \text{ on}}$	typ.	60 ns
--------------------	------	-------

rise time

$t_r$	typ.	100 ns
-------	------	--------

turn-off times: delay time

$t_{d \text{ off}}$	typ.	500 ns
---------------------	------	--------

fall time

$t_f$	typ.	100 ns
-------	------	--------

DEVELOPMENT SAMPLE DATA

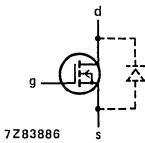


Fig. 2 Diode characteristics.

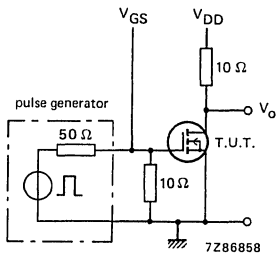


Fig. 3 Switching time test circuit.

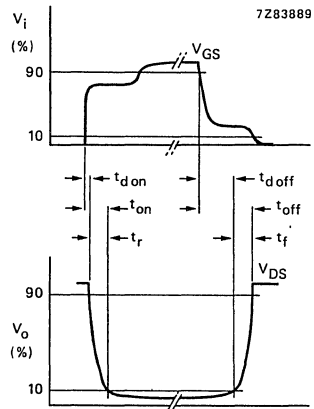


Fig. 4 Switching time waveforms.

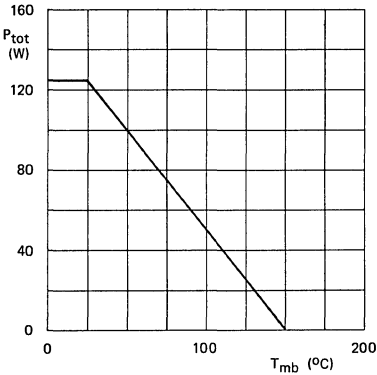


Fig. 5 Power derating curve.

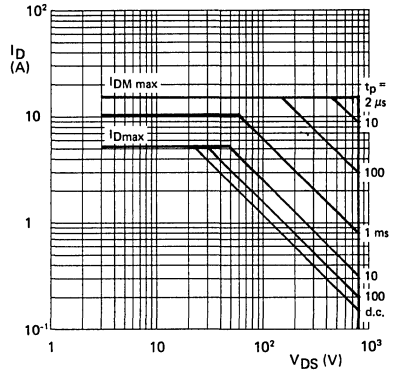


Fig. 6 Safe Operating ARea.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

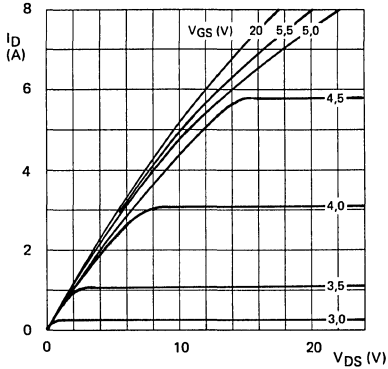


Fig. 7 Output characteristic.  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^\circ\text{C}$ .

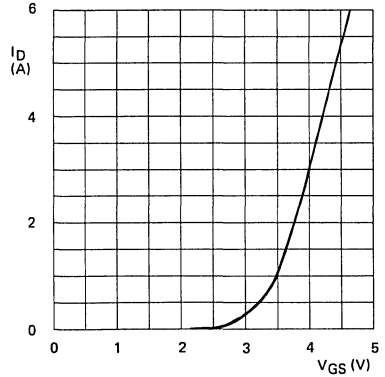


Fig. 8 Typical transfer characteristic  
 at  $V_{DS} = 25\text{ V}$ .

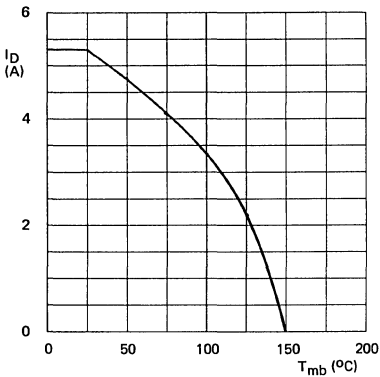


Fig. 9 Drain current as a function  
 of mounting base temperature.

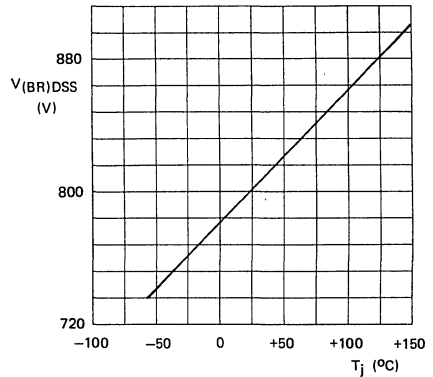


Fig. 10 Drain-source breakdown voltage  
 as a function of junction temperature.

## DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

BUZ84A

## POWER MOS TRANSISTOR

N-channel enhancement mode field-effect power transistor in a TO-3 envelope; with the drain connected to the mounting base.

Intended for use in motor control; SMPS; welding, DC/DC and DC/AC converters.

### QUICK REFERENCE DATA

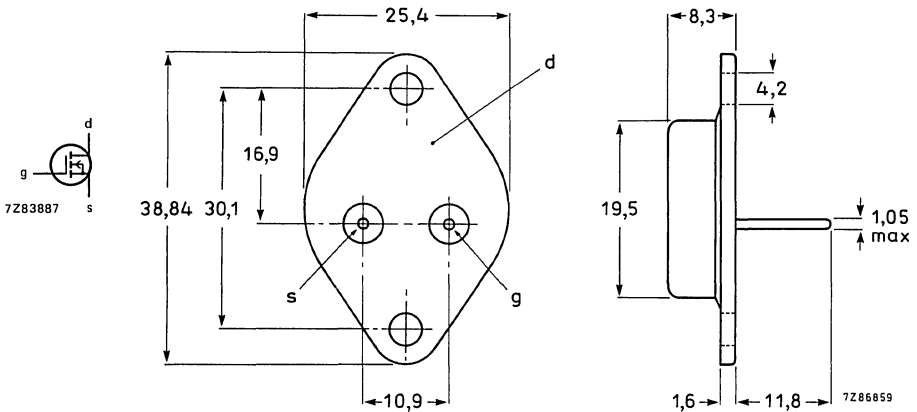
Drain-source voltage	$V_{DS}$	max.	800 V
Drain current (d.c.)	$I_D$	max.	6 A
Total power dissipation	$P_{tot}$	max.	125 W
Drain-source resistance (on)	$R_{DS ON}$	<	1,5 $\Omega$
Turn-off fall-time $V_{DD} = 30 V$ ; $I_D = 2,6 A$ ; $V_{GS} = 10 V$	$t_f$	typ.	100 ns

### MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-3.

Drain connected to mounting base.



Protect the gate-source input during transport or handling against static charge.

See relevant chapter for mounting instructions.



**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	800 V
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	$V_{DGR}$	max.	800 V
Gate-source voltage	$\pm V_{GS}$	max.	20 V
Drain current (d.c.); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_D$	max.	6 A
Drain current (pulse peak value); $T_{mb} = 25 \text{ }^\circ\text{C}$	$I_{DM}$	max.	18 A
Total power dissipation	$P_{tot}$	max.	125 W
Storage temperature	$T_{stg}$		-55 to +150 $^\circ\text{C}$
Junction temperature	$T_j$	max.	+150 $^\circ\text{C}$

**THERMAL CHARACTERISTICS**

**Thermal resistance**

From junction to mounting base	$R_{th \text{ j-mb}}$	=	1 K/W
From junction to ambient	$R_{th \text{ j-a}}$	=	35 K/W

**STATIC CHARACTERISTICS**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Drain-source breakdown voltage $V_{GS} = 0 \text{ V}; I_D = 1 \text{ mA}$	$V_{(BR)DSS}$	>	800 V
Gate threshold voltage $V_{DS} = V_{GS}; I_D = 10 \text{ mA}$	$V_{GST}$	typ.	2,1 to 4 V 3 V
Zero gate voltage drain current $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = V_{DSmax}; V_{GS} = 0; T_j = 125 \text{ }^\circ\text{C}$	$I_{DSS}$	<	1 mA 4 mA
Gate-source leakage current $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}$	$I_{GSS}$	<	100 nA
Drain-source on-state resistance $V_{GS} = 10 \text{ V}; I_D = 3 \text{ A}$	$R_{DS \text{ ON}}$	<	1,5 $\Omega$

**Diode characteristics**

$T_{mb} = 25 \text{ }^\circ\text{C}$  unless otherwise specified

Forward current	$I_F$	<	6 A
Forward current (peak value)	$I_{FRM}$	<	18 A
On-state voltage $I_F = 2 \text{ I}_D; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	$V_F$	typ. <	1,1 V 1,5 V
Reverse recovery $I_F = 2 \text{ I}_D; dI_F/dt = 100 \text{ A}/\mu\text{s}; T_j = 25 \text{ }^\circ\text{C}$	$t_{rr}$	typ.	1800 ns
recovery time	$Q_s$	typ.	25 $\mu\text{C}$
recovery charge			

**DYNAMIC CHARACTERISTICS**

Forward transfer conductance

$$V_{DS} = 25 \text{ V}; I_D = 3 \text{ A}$$

$g_{fs} > \begin{matrix} 1,8 \text{ A/V} \\ \text{typ. } 3 \text{ A/V} \end{matrix}$

Input capacitance at  $f = 1 \text{ MHz}$

$$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$$

$C_{is} \text{ typ. } 3500 \text{ pF}$

Output capacitance at  $f = 1 \text{ MHz}$

$$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$$

$C_{os} \text{ typ. } 200 \text{ pF}$

Feedback capacitance at  $f = 1 \text{ MHz}$

$$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}$$

$C_{rs} \text{ typ. } 100 \text{ pF}$

Switching times (see Figs 3 and 4)  
(between 10% and 90% levels)

$$V_{DD} = 30 \text{ V}; I_D = 2,6 \text{ A}; V_{GS} = 10 \text{ V}$$

turn-on times: delay time  
rise time

$t_{d \text{ on}} \text{ typ. } 60 \text{ ns}$   
 $t_r \text{ typ. } 100 \text{ ns}$

turn-off times: delay time  
fall time

$t_{d \text{ off}} \text{ typ. } 500 \text{ ns}$   
 $t_f \text{ typ. } 100 \text{ ns}$

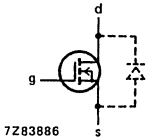


Fig. 2 Diode characteristics.

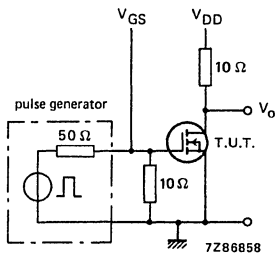


Fig. 3 Switching time test circuit.

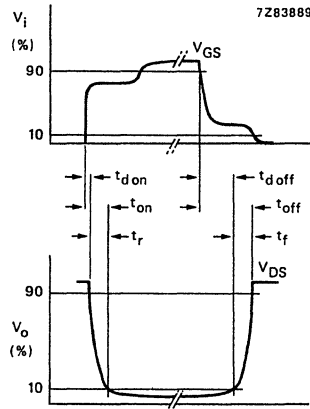


Fig. 4 Switching time waveforms.

DEVELOPMENT SAMPLE DATA

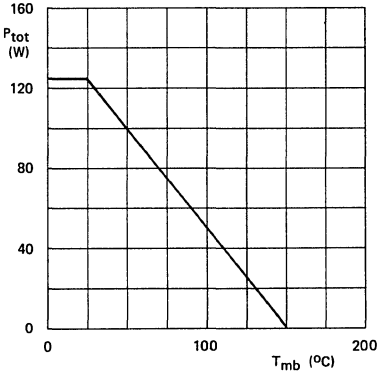


Fig. 5 Power derating curve.

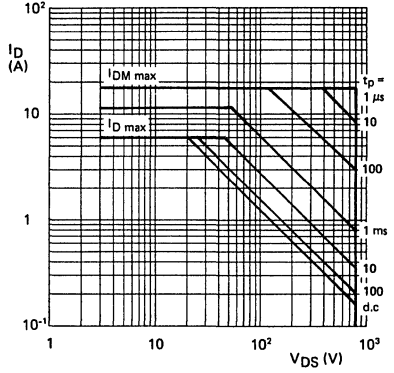


Fig. 6 Safe Operating Area.  
 $T_{mb} = 25\text{ }^\circ\text{C}$ ;  $\delta = 0,01$ .

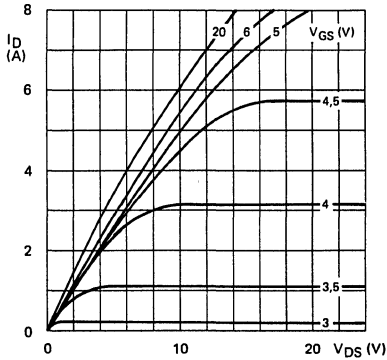


Fig. 7 Output characteristic.  
 $80\text{ }\mu\text{s}$  pulse test;  $T_{mb} = 25\text{ }^\circ\text{C}$ .

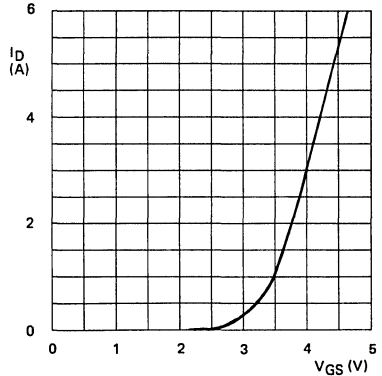


Fig. 8 Typical transfer characteristic  
 at  $V_{DS} = 25\text{ V}$ .

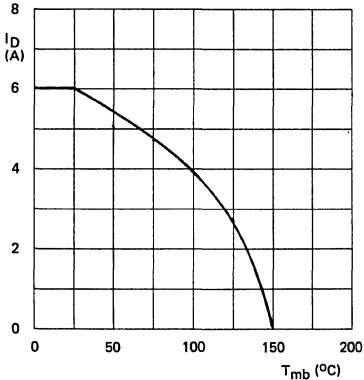


Fig. 9 Drain current as a function  
 of mounting base temperature.

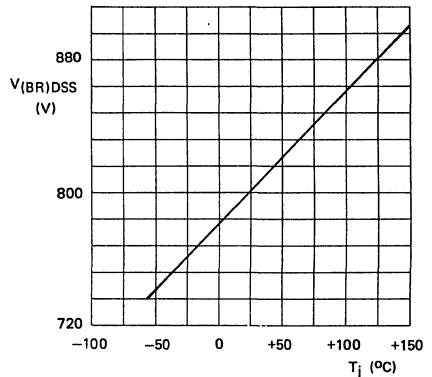


Fig. 10 Drain-source breakdown voltage  
 as a function of junction temperature.

MOUNTING INSTRUCTIONS





## MOUNTING INSTRUCTIONS FOR TO-220 ENVELOPES

### GENERAL DATA AND INSTRUCTIONS

#### General rules

1. First fasten the device to the heatsink before soldering the leads.
2. Avoid axial stress to the leads.
3. Keep mounting tool (e.g. screwdriver) clear of the plastic body.
4. The rectangular washer may only touch the plastic part of the body; it should not exert any force on that part (screw mounting).

#### Heatsink requirements

Flatness in the mounting area: 0,02 mm maximum per 10 mm.

Mounting holes must be deburred, see further mounting instructions.

#### Heatsink compound

Values of the thermal resistance from mounting base to heatsink ( $R_{th\ mb-h}$ ) given for mounting with heatsink compound refer to the use of a metallic oxide-loaded compound. Ordinary silicone grease is not recommended.

For insulated mounting, the compound should be applied to the bottom of both device and insulator.

#### Mounting methods for power transistors

##### 1. Clip mounting

Mounting with a spring clip gives:

- a. A good thermal contact under the crystal area, and slightly lower  $R_{th\ mb-h}$  values than screw mounting.
- b. Safe insulation for mains operation.

##### 2. M3 screw mounting

It is recommended that the rectangular spacing washer is inserted between screw head and mounting tab.

Mounting torque for screw mounting:

(For thread-forming screws these are final values. Do not use self-tapping screws.)

Minimum torque (for good heat transfer)	0,55 Nm (5,5 kgcm)
Maximum torque (to avoid damaging the device)	0,80 Nm (8,0 kgcm)

N.B.: When a nut or screw is not driven direct against a curved spring washer or lock washer (not for thread-forming screw), the torques are as follows:

Minimum torque (for good heat transfer)	0,4 Nm (4 kgcm)
Maximum torque (to avoid damaging the device)	0,6 Nm (6 kgcm)

N.B.: Data on accessories are given in separate data sheets.

**3. Rivet mounting non-insulated**

The device should not be pop-riveted to the heatsink. However, it is permissible to press-rivet providing that eyelet rivets of soft material are used, and the press forces are slowly and carefully controlled so as to avoid shock and deformation of either heatsink or mounting tab.

**Thermal data**

		clip mounting	screw mounting	
From mounting base to heatsink				
with heatsink compound, direct mounting	$R_{th\ mb-h}$	= 0,3	0,5	K/W
without heatsink compound, direct mounting	$R_{th\ mb-h}$	= 1,4	1,4	K/W
with heatsink compound and 0,1 mm maximum mica washer	$R_{th\ mb-h}$	= 2,2	—	K/W
with heatsink compound and 0,25 mm maximum alumina insulator	$R_{th\ mb-h}$	= 0,8	—	K/W
with heatsink compound and 0,05 mm mica washer insulated up to 500 V	$R_{th\ mb-h}$	= —	1,4	K/W
insulated up to 800 V/1000 V	$R_{th\ mb-h}$	= —	1,6	K/W
without heatsink compound and 0,05 mm mica washer insulated up to 500 V	$R_{th\ mb-h}$	= —	3,0	K/W
insulated up to 800 V/1000 V	$R_{th\ mb-h}$	= —	4,5	K/W

**Lead bending**

Maximum permissible tensile force on the body, for 5 seconds is 20 N (2 kgf).

The leads can be bent through 90° maximum, twisted or straightened. To keep forces within the above-mentioned limits, the leads are generally clamped near the body, using pliers. The leads should neither be bent nor twisted less than 2,4 mm from the body.

**Soldering**

**Lead soldering temperature at > 3 mm from the body;  $t_{sld} < 5$  s:**

Devices with  $T_{j\ max} \leq 175$  °C, soldering temperature  $T_{sld\ max} = 275$  °C.

Devices with  $T_{j\ max} \leq 110$  °C, soldering temperature  $T_{sld\ max} = 240$  °C.

Avoid any force on body and leads during or after soldering: do not correct the position of the device or of its leads after soldering.

It is not permitted to solder the metal tab of the device to a heatsink, otherwise its junction temperature rating will be exceeded.

**Mounting base soldering**

Recommended metal-alloy of solder paste (85% metal weight)

62 Sm/36 Pb/2 Ag or 60 Sn/40 Pb.

Maximum soldering temperature  $\leq 200$  °C (tab-temperature).

Soldering cycle duration including pre-heating  $\leq 30$  sec.

For good soldering and avoiding damage to the encapsulation pre-heating is recommended to a temperature  $\leq 165$  °C at a duration  $\leq 10$  s.

**INSTRUCTIONS FOR CLIP MOUNTING**

**Direct mounting with clip 56363**

1. Apply heatsink compound to the mounting base, then place the transistor on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of  $10^\circ$  to  $30^\circ$  to the vertical (see Figs 1 and 2).
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab (see Fig. 2a).

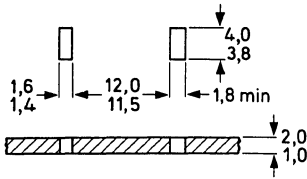


Fig. 1 Heatsink requirements.

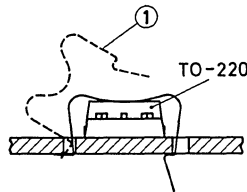


Fig. 2 Mounting.  
(1) spring clip 56363.

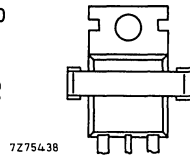


Fig. 2a Position of  
transistor (top view).

**Insulated mounting with clip 56364**

With the insulators 56367 or 56369 insulation up to 2 kV is obtained.

1. Apply heatsink compound to the bottom of both transistor and insulator, then place the transistor with the insulator on the heatsink.
2. Push the short end of the clip into the narrow slot in the heatsink with the clip at an angle of  $10^\circ$  to  $30^\circ$  to the vertical (see Figs 3 and 4).
3. Push down the clip over the device until the long end of the clip snaps into the wide slot in the heatsink. The clip should bear on the plastic body, not on the tab. Ensure that the device is centred on the mica insulator to prevent creepage.

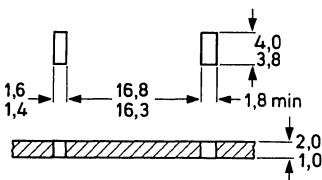


Fig. 3 Heatsink requirements.

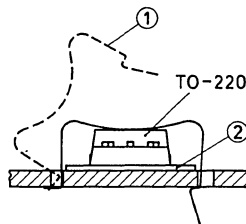


Fig. 4 Mounting.  
(1) spring clip 56364.  
(2) insulator 56369 or 56367.

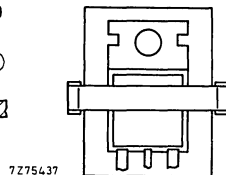


Fig. 4a Position of  
transistor (top view).



INSTRUCTIONS FOR SCREW MOUNTING  
Direct mounting with screw and spacing washer

Dimensions in mm

- *through heatsink with nut*

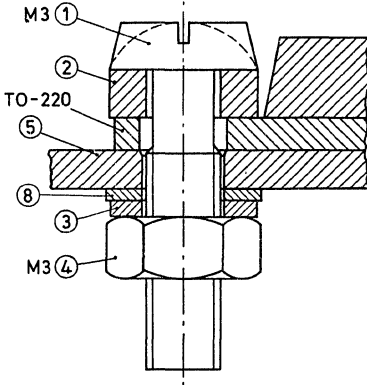


Fig. 5 Assembly.

- (1) M3 screw.
- (2) rectangular washer (56360a).
- (3) lock washer.
- (4) M3 nut.
- (5) heatsink.
- (8) plain washer.

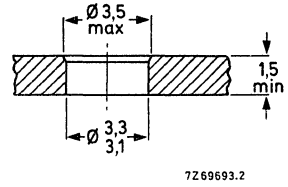


Fig. 6 Heatsink requirements.

- *into tapped heatsink*

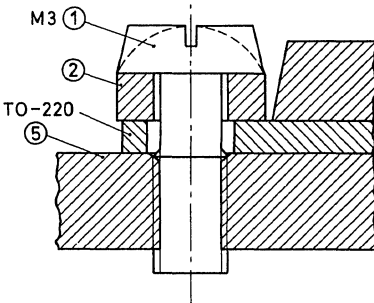


Fig. 7 Assembly.

- (1) M3 screw.
- (2) rectangular washer 56360a.
- (5) heatsink.

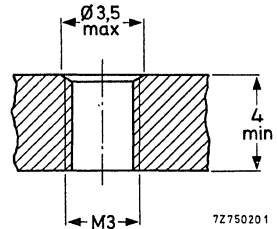


Fig. 8 Heatsink requirements.

Insulated mounting with screw and spacing washer  
(not recommended where mounting tab is on mains voltage)

Dimensions in mm

● *through heatsink with nut*

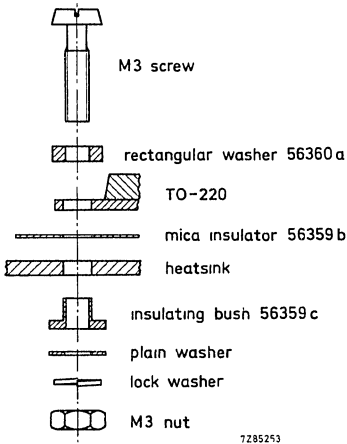


Fig. 9 Insulated screw mounting with rectangular washer. Known as a "bottom mounting".

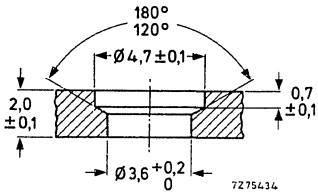


Fig. 10 Heatsink requirements for 500 V insulation.

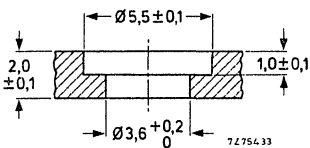


Fig. 11 Heatsink requirements for 800 V insulation.

● *into tapped heatsink*

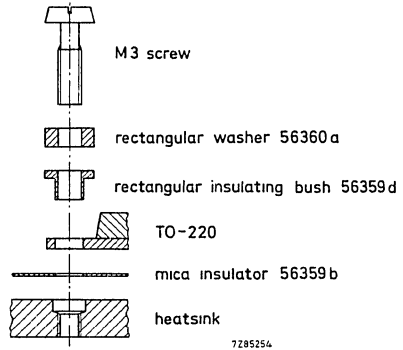


Fig. 12 Insulated screw mounting with rectangular washer into tapped heatsink. Known as a "top mounting".

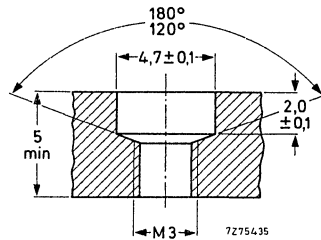


Fig. 13 Heatsink requirements for 500 V insulation.

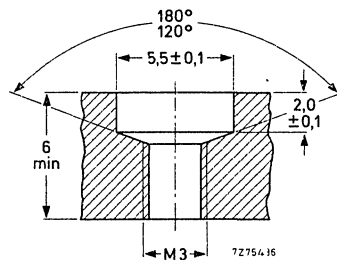


Fig. 14 Heatsink requirements for 1000 V insulation.



## MOUNTING INSTRUCTIONS FOR TO-3 ENVELOPES

### GENERAL DATA AND INSTRUCTIONS

Instructions for direct mounting.

Mounting instructions for up to 500 V insulation.

Using insulating bushes 56201j or 56261a and mica washer 56201d.

Mounting instructions for 500 to 2000 V insulation.

Using mounting support 56352 and mica washer 56339.

### Heatsink requirements

Flatness in the mounting area: 0,05 mm per 40 mm

Mounting holes must be deburred.

### Mounting torques

Minimum torque (for good heat transfer) 0,4 Nm (4 kgcm)

Maximum torque (to avoid damaging the transistor) 0,6 Nm (6 kgcm)

N.B.: When the driven nut or screw is in direct contact with a toothed lock washer (e.g. Fig. 10), the torques are as follows:

Minimum torque 0,55 Nm (5,5 kgcm)

Maximum torque 0,8 Nm (8 kgcm)

### Thermal data

The thermal resistance from mounting base to heatsink ( $R_{th\ mb-h}$ ) can be reduced by applying a heat conducting compound between transistor and heatsink. For insulated mounting the compound should be applied to the bottom of both device and insulator.

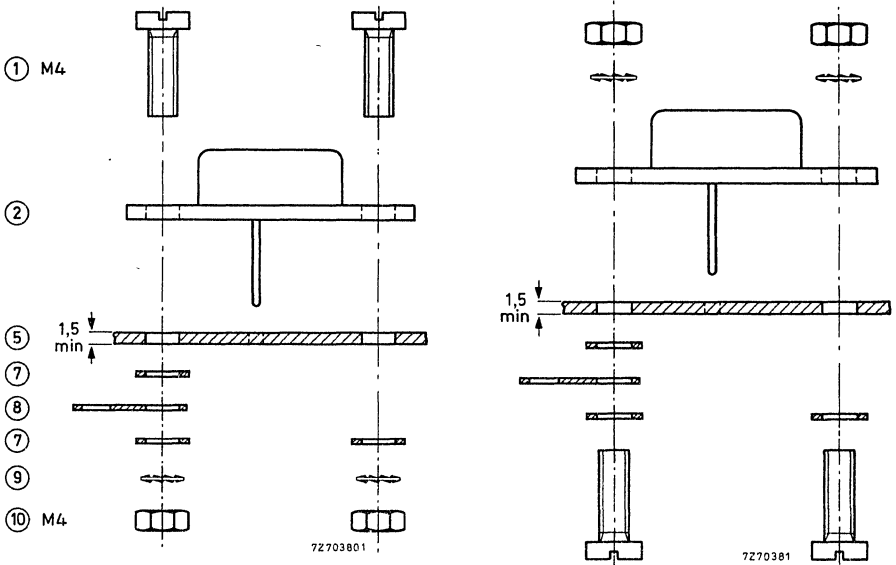
	Direct mounting	Insulated mounting		
		500 V mica	2000 V mica	
From mounting base to heatsink without heatsink compound	$R_{th\ mb-h}$ 0,6	1,0	1,25	K/W
with heatsink compound	$R_{th\ mb-h}$ 0,1	0,3	0,5	K/W

# MOUNTING INSTRUCTIONS TO-3

## INSTRUCTIONS FOR DIRECT MOUNTING

The transistors should be mounted with M4 screws, see Figs 1 and 2. Minimum heatsink thickness (for good heat transfer) 1,5 mm. Hole pattern: Fig. 3.

A heatsink with tapped holes or insert nuts can also be used, but a torque washer is necessary between metal washer and transistor. See Fig. 4.



Figs 1 and 2. Direct mounting with nuts.

### Legend

- (1) = screw
  - (2) = TO-3
  - (4) = mica
  - (5) = heatsink
  - (6) = insulating bush
  - (7) = metal washer
  - (8) = soldering tag
  - (9) = lock washer
  - (10) = nut
  - (11) = tapped hole
  - (12) = insert nut
- Dimensions in mm

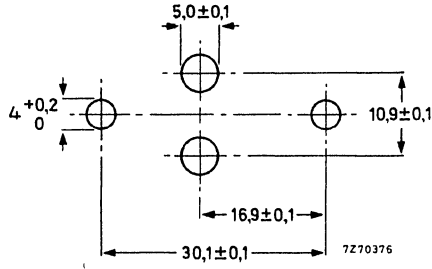


Fig. 3 Hole pattern for direct mounting with nuts.

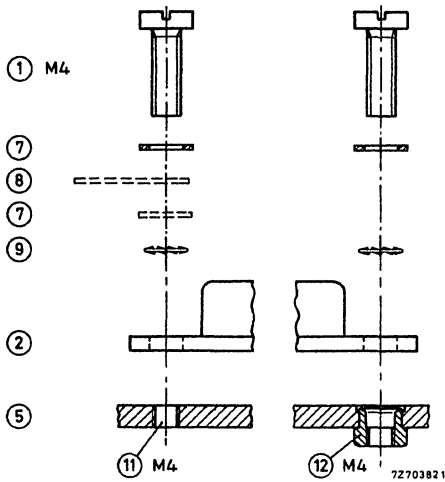


Fig. 4 Direct mounting with tapped holes or insert nuts.

# MOUNTING INSTRUCTIONS TO-3

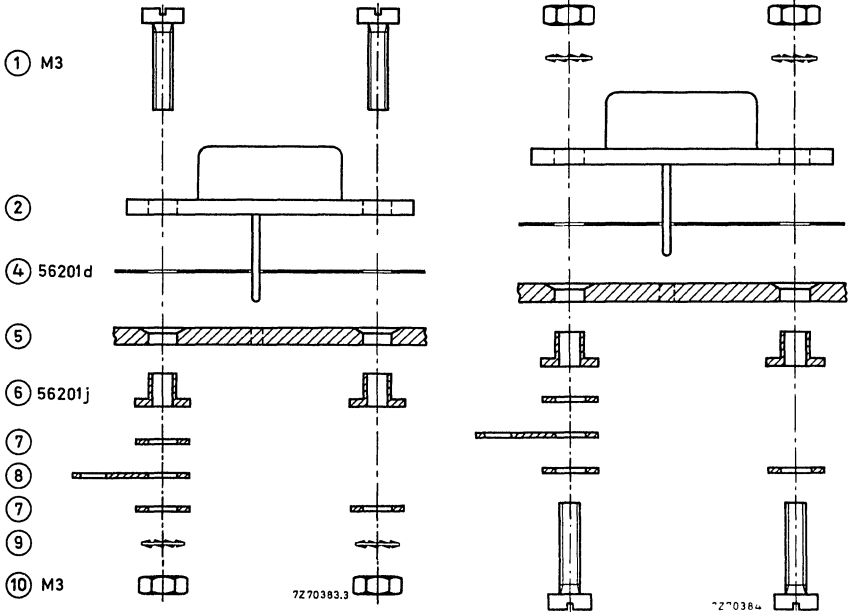
## MOUNTING INSTRUCTIONS FOR UP TO 500 V INSULATION

### Using insulating bushes 56201j and mica washer 56201d

For the component arrangement with minimum heatsink thickness see Figs 5 and 6. For hole pattern and shape of holes see Figs 7 and 8.

### Using insulating bush 56261a and mica washer 56201d

For an arrangement with M3 screws and nuts see Fig. 9, mounting holes are given in Figs 7 and 8. The accessories can also be used in combination with M3 screws and heatsinks provided with tapped holes or insert nuts. Lock washers are necessary between screw-head and metal washer, see Fig. 10. For an assembly drawing with tapped holes see Fig. 11, with insert nuts see Fig. 12.



Figs 5 and 6. Insulated mounting (500 V) with 56201j and 56201d. Heatsink thickness: 1,5 to 2,5 mm.

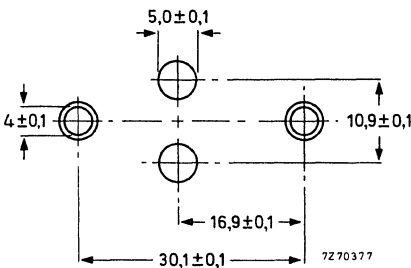


Fig. 7 Hole pattern for 500 V insulation, nut fastening.

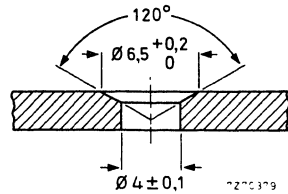


Fig. 8 Shape of hole for 500 V insulation, nut fastening.

For legend see page 276.

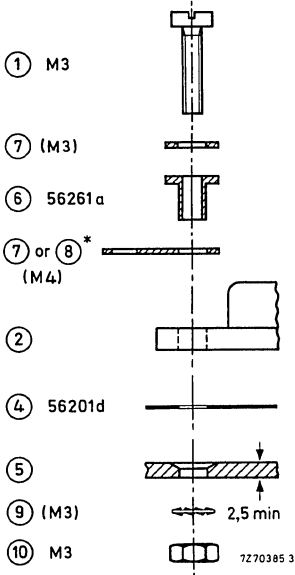


Fig. 9 Insulated mounting (500 V) with nuts.

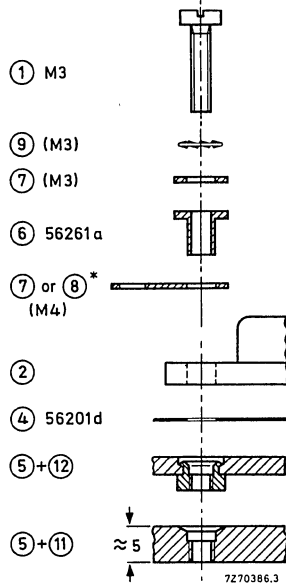


Fig. 10 Insulated mounting (500 V) with tapped holes or insert nuts.

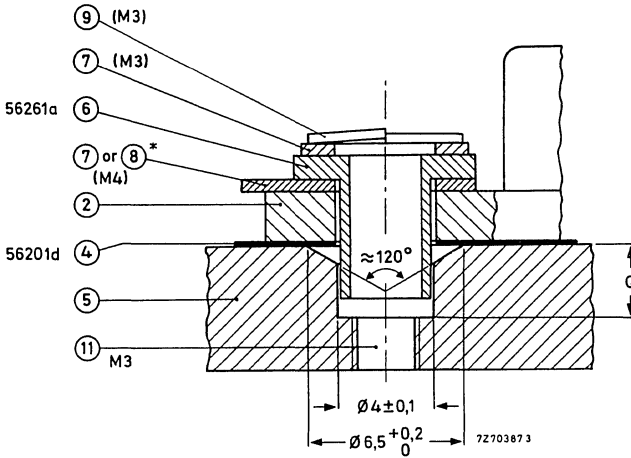


Fig. 11 Assembly (partial) for Fig. 10 - tapped holes. Q minimum 2,5 mm.

For legend see page 276.

\* Thickness approximately 0,6 mm, outer diameter 7,5 mm.



**MOUNTING  
INSTRUCTIONS  
TO-3**

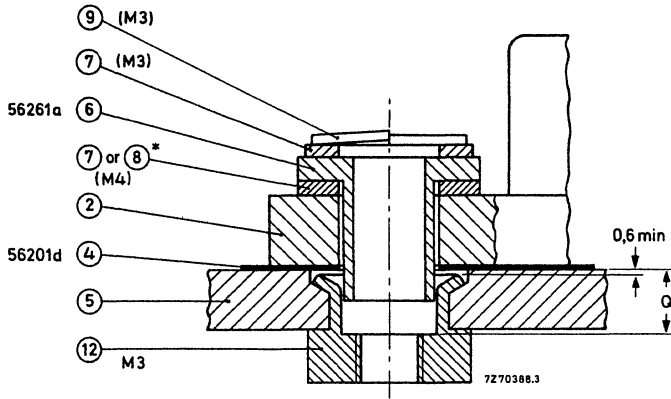


Fig. 12 Assembly (partial) for Fig. 10 - insert nuts Q minimum 2,5 mm.

For legend see page 276.

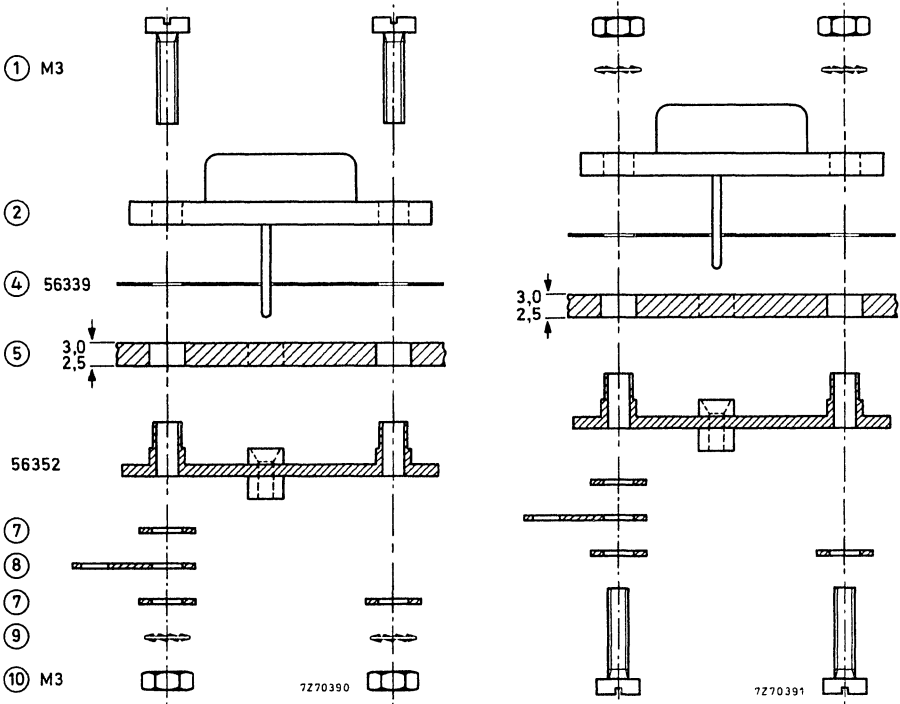
Dimensions in mm

\* Thickness approximately 0,6 mm, outer diameter 7,5 mm.

MOUNTING INSTRUCTIONS FOR 500 V TO 2000 V INSULATION

Using mounting support 56352 and mica washer 56339

The transistor should be mounted with M3 screws. For component arrangement see Figs 13 and 14. For hole pattern see Fig. 15. Thickness of heatsink 2,5 mm to 3 mm.



Figs 13 and 14. Insulated mounting (500 V–2000 V).

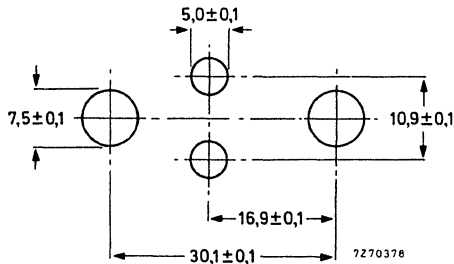


Fig. 15 Hole pattern for Figs 13 and 14.

For legend see preceding page.



ACCESSORIES



## TYPE NUMBER SURVEY ACCESSORIES

type number	description	envelope
56201d	mica washer (up to 500 V)	TO-3
56201j	insulating bushes (up to 500 V)	TO-3
56261a	insulating bushes (up to 500 V)	TO-3
56339	mica washer (500 to 2000 V)	TO-3
56352	insulating mounting support	TO-3
56359b	mica washer (up to 1000 V)	TO-220
56359c	insulating bush (up to 800 V)	TO-220
56359d	rectangular insulating bush (up to 1000 V)	TO-220
56360a	rectangular washer (brass)	TO-220
56363	spring clip (direct mounting)	TO-220
56364	spring clip (insulated mounting)	TO-220
56367	alumina insulator (up to 2000 V)	TO-220

Clip mounting TO-220 envelopes

56363

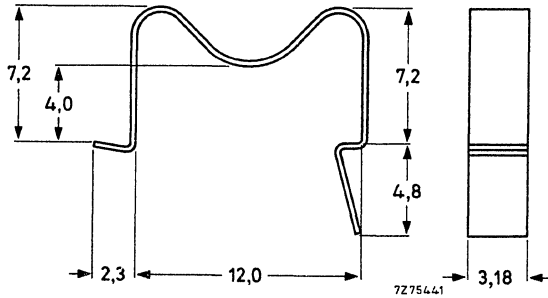
## SPRING CLIP

for direct mounting of TO-220 envelopes

## MECHANICAL DATA

Material: steel, zinc-chromate passivated.

Dimensions in mm



56364

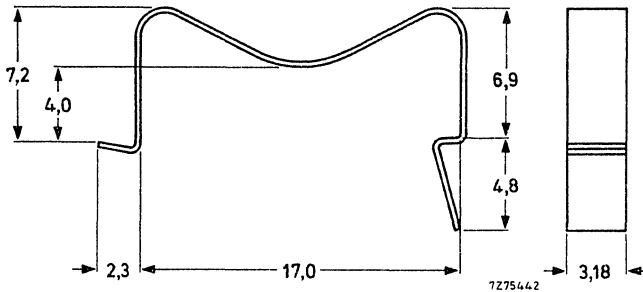
## SPRING CLIP

for insulated mounting of TO-220 envelopes

## MECHANICAL DATA

Material: steel, zinc-chromate passivated.

Dimensions in mm



to be used in  
conjunction with  
56367 or 56369.

Clip mounting TO-220 envelopes

56367

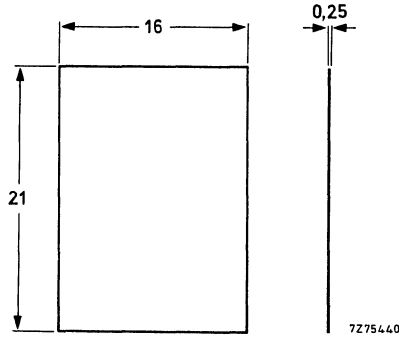
ALUMINA INSULATOR

for insulated clip mounting of TO-220 envelopes (up to 2 kV)

MECHANICAL DATA

Material: 96-alumina.

Dimensions in mm



\* Because alumina is brittle, extreme care must be taken when mounting devices not to crack the alumina, particularly when used without heatsink compound.

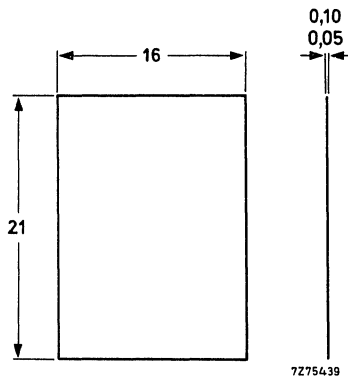
56369

MICA INSULATOR

for insulated clip mounting of TO-220 envelopes (up to 2 kV)

MECHANICAL DATA

Dimensions in mm



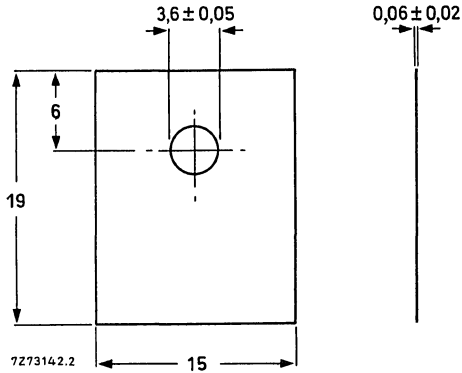
Mounting TO-220 envelopes

56359b

**MICA WASHER**  
for TO-220 envelopes (up to 1000 V)

**MECHANICAL DATA**

Dimensions in mm



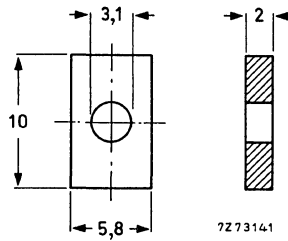
56360a

**RECTANGULAR WASHER**  
for direct and insulated mounting of TO-220 envelopes

**MECHANICAL DATA**

Material: brass; nickel plated

Dimensions in mm





Mounting TO-220 envelopes

56359c

INSULATING BUSH

for TO-220 envelopes (up to 800 V)

MECHANICAL DATA

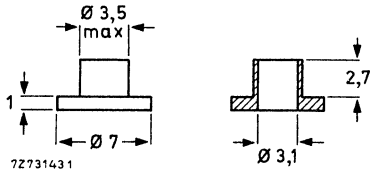
Material: polyester

TEMPERATURE

Maximum permissible temperature

$T_{max} = 150\text{ }^{\circ}\text{C}$

Dimensions in mm



56359d

RECTANGULAR INSULATING BUSH

for TO-220 envelopes (up to 1000 V)

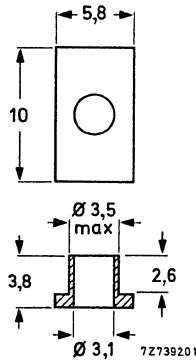
MECHANICAL DATA

TEMPERATURE

Maximum permissible temperature

$T_{max} = 150\text{ }^{\circ}\text{C}$

Dimensions in mm



Mounting TO-3 envelopes

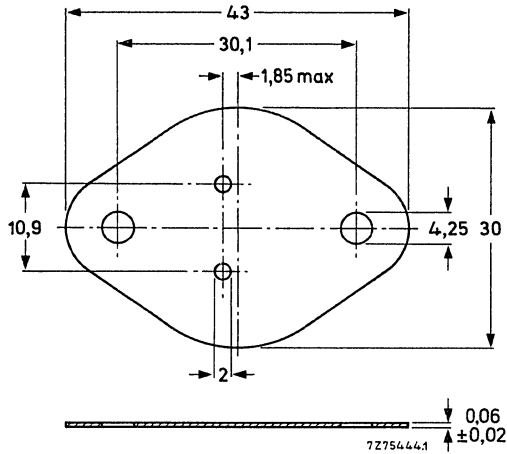
56201d

## MICA WASHER

Mica washer for up to 500 V insulation of TO-3 envelopes.

## MECHANICAL DATA

Dimensions in mm



56201j

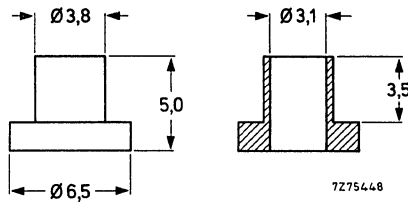
## 2 INSULATING BUSHES

Two insulating bushes for up to 500 V insulation of TO-3 envelopes.

## MECHANICAL DATA

Material: polyester

Dimensions in mm



## TEMPERATURE

Maximum permissible temperature

 $T_{\max}$  150 °C

Mounting TO-3 envelopes

56261a

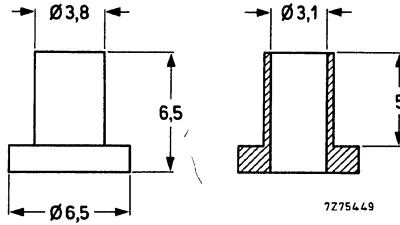
2 INSULATING BUSHES

Two insulating bushes for up to 500 V insulation of TO-3 envelopes.

MECHANICAL DATA

Material: polyester

Dimensions in mm



TEMPERATURE

Maximum permissible temperature

T<sub>max</sub> 150 °C

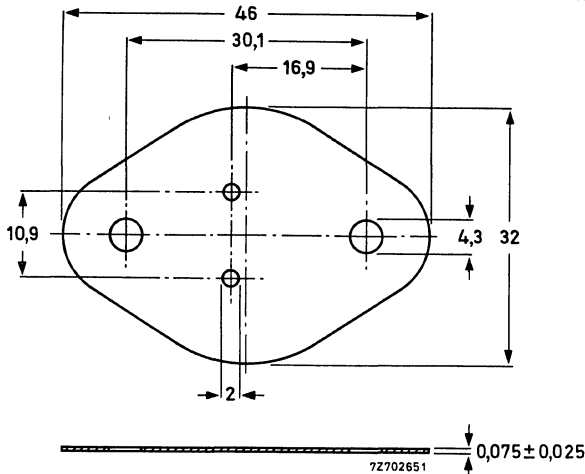
56339

MICA WASHER

Mica washer for 500 to 2000 V insulation of TO-3 envelopes, for which it should be combined with mounting support 56352.

MECHANICAL DATA

Dimensions in mm



Mounting TO-3 envelopes

56352

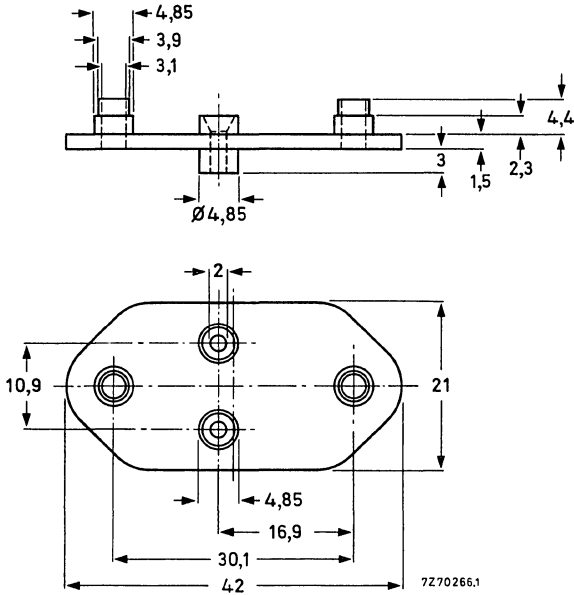
## MOUNTING SUPPORT

Mounting support for 500 to 2000 V insulation of TO-3 envelopes, for which it should be combined with mica washer 56339.

## MECHANICAL DATA

Dimensions in mm

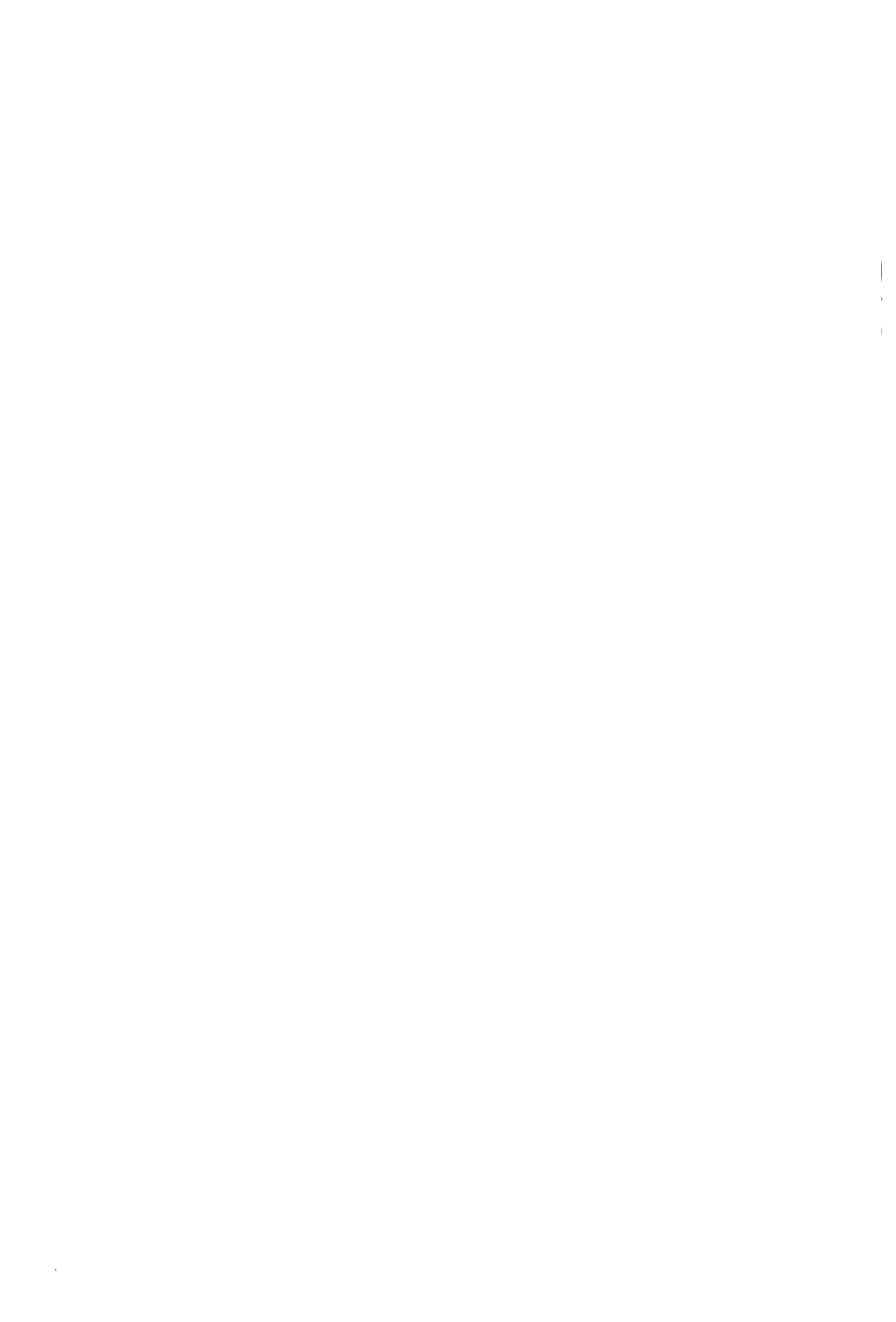
Material: polyester



## TEMPERATURE

Maximum permissible temperature

 $T_{\max}$  125 °C





# POWER MOS TRANSISTORS



SELECTION GUIDE

GENERAL

TRANSISTOR DATA

MOUNTING INSTRUCTIONS

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