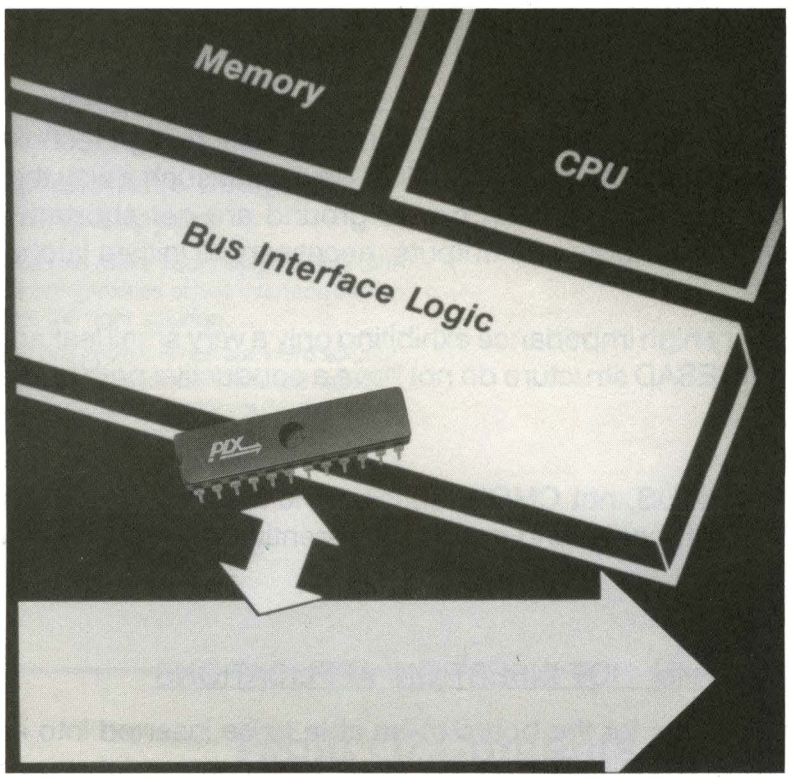
Product Description Guide: ICs for Bus Interface



PLX TECHNOLOGY

A NOTE ON 'LATCHUP' AND 'HOT INSERTION'

PLX DEVICES ARE LATCHUP-FREE

CMOS devices have gained a reputation for having a tendency to latchup, especially when used in the electrically hostile environment of the backplane. Through special design techniques on the input and output buffers, PLX has been able to develop our CMOS devices in such a way that they are latchup-free under normal operating conditions i.e., when power ground are not shorted. The devices lack the parasitic current path, in both the inputs and outputs, necessary to initiate latchup.

- PLX inputs have very high impedance exhibiting only a very small leakage currents. The input transistor and ESAD structure do not have a conductive path between power and ground.

- PLX outputs have NMOS, not CMOS, buffers. The NMOS buffer does not contain a latchup path between power and ground. Inherently, NMOS gates have no parasitic latchup path.

PLX DEVICES CAN FUNCTION IN 'HOT INSERTION' APPLICATIONS

Often, a design requirement exists for the board to be able to be inserted into and removed from the system while the system is powered up. This capability allows for easier debug and maintenance and is critical in "non-stop" applications. PLX devices are non-intrusive to their host board and to other boards in such a hot insertion application for three reasons:

- The devices have glitch free power up and power down characteristics. Spurious pulses from outputs are suppressed during ramp up or down.

- The devices' inputs and outputs, when powered down, appear as high impedance opens to the rest of the system. Other CMOS devices can have their inputs shorted to ground, a low impedance path which is hazardous since power and ground are shorted.

- The devices have no inherent latchup path under normal hot insertion procedures. A normal hot insertion procedure does not short power and ground under any conditions.

For more information on "latchup" and "hot insertion" please contact PLX and request a copy of our pamphlet entitled 'Interfacing To Backplane Buses Using CMOS Devices'.

High Drive Current, Standard and Programmable ICs for Bus Interface

PLX Technology, Inc. designs and manufactures programmable logic devices (PLDs) and integrated circuits optimized for use in bus interface and other high drive current applications. Whether you use standard buses like VME, VME Subsystem Bus (VSB), Multibus™, Micro Channel™ or a proprietary bus, PLX has the solution for you.

Choose from off-the-shelf ICs programmed for specific buses or programmable devices for custom requirements. Either way, you get a multitude of benefits:

- **Space-saving, 300-mil, 24-pin DIP or 28-pin LCC packages**
- **Integrated drivers up to 64mA, totem pole or open collector**
- **Integrated input buffers**
- **Maximum integration of bus control logic**
- **Reduced chip count**
- **Hot insertion capable and latchup-free design**
- **Metastable hardened circuitry**

PLX Gives You Comprehensive Design Assistance And Programming Support

Unique logic requirements can make your design task a difficult one. PLX understands the complexities of bus interface design and will help you find or create the right solution.

For example, first try one of our pre-programmed standard solution devices in your application. See how it performs. Then add capabilities by custom programming. This can be done for you by the willing experts at PLX or by you at your own premises. If you send or FAX a copy of the schematic or a block diagram of your application, PLX promises to save you time and design effort.

If programming is required, chances are you have the programming tools you need. PLX programmable devices are supported by industry standards like ABEL™ and CUPL™ and the most popular models of programmers.

Bus Interface Kits Aid In The Design Task

Design kits are available for your convenience. The enclosed Business Reply Cards describe the various Bus Interface Kits available from PLX Technology. Each kit is designed to give you the information and devices you need to find and implement the right bus interface solution for your application.

How To Use This Guide

Look under the section appropriate to the bus your design uses to see features, a description and pinouts for PLX devices. If a programmable device is better suited to your design, there's a section describing PLX PLDs.

For information in greater detail call 1-800-759-3753, FAX PLX at (415) 960-0479 or complete one of the enclosed Business Reply Cards.

Table Of Contents

VMEbus

For VMEbus, PLX offers several devices which implement master control, slave control, interrupt handling and interrupt generation. These devices can be used together or as separate solutions according to your needs.

PLX's VME devices include:

- **VME 1210/1220** **Master Controllers: Slot 1 and Non-slot 1**
- **VME 2000** **Slave Module Interface Device**
- **VME 3000/3010** **Interrupt Generators (ROAK or RORA)**
- **VME 4000** **Interrupt Handler**

VME 1210/1220 VME Master Controller with System Arbiter

Distinctive Features

- VME 1210 provides two device chip set for slot 1 master bus controller and single level arbiter
- VME 1220 provides two device chip set for non-slot 1 master bus controller
- Integrates 48 mA and 64 mA VMEbus signals: AS*, DS0*, DS1*, WRITE*, BR*, BBSY*
- Integrates input hysteresis buffers
- Supports Release When Done (RWD) and Release On Request (ROR) protocols
- Supports address pipelining, block transfers, and early BBSY* release
- Available in Commercial, Industrial, and Military temperature ranges

Applications

- VMEbus masters residing in slot 1 boards (VME 1210)
- VMEbus masters residing in non-slot 1 boards (VME 1220)

Packages

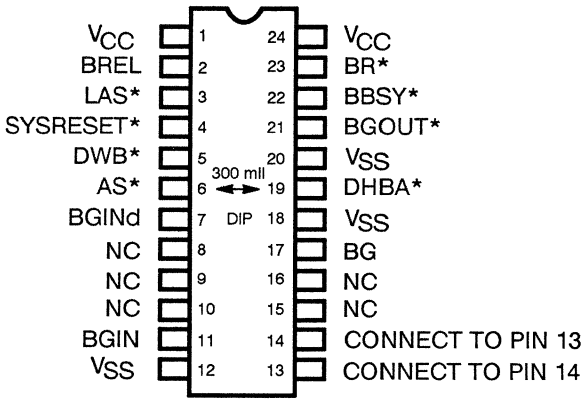
General Description

The VME 1210: The VME1210 is comprised of the VME 1210A and the VME 1210B for slot 1 applications. The devices are CMOS and packaged in 24 pin 300 mil wide DIPs or 28 pin J-type LCCs. The VME 1210A provides bus requesting, local arbitration, and single level system arbitration. The VME 1210B functions as the VMEbus controller. The requester initiates a VMEbus request from the local master's bus request for a data or interrupt cycle. The bus controller controls the bus after initiation of a bus cycle and relinquishes the bus at the end of the bus cycle. The bus controller supervises the handshaking between the local master CPU and the slave modules.

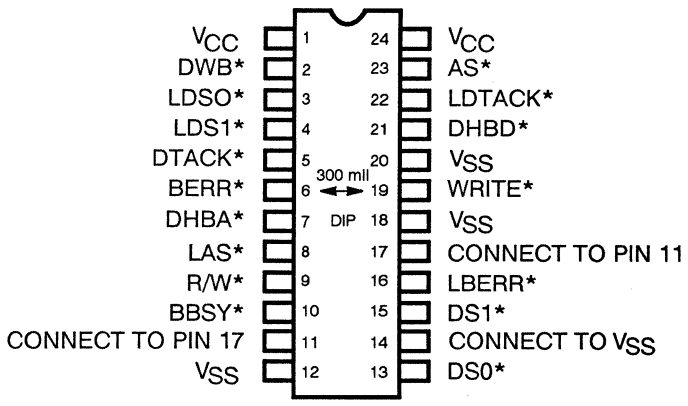
The VME 1220: The VME 1220 is comprised of the VME 1220A and the VME 1220B for non-slot 1 applications. The devices are CMOS and packaged in 24 pin 300 mil wide DIPs or 28 pin J-type LCCs. The VME 1220A provides bus requesting and local arbitration. The VME 1220B functions as the VMEbus controller. The requester initiates a VMEbus request from the local master's bus request for a data or interrupt cycle. The bus controller controls the bus after initiation of a bus cycle and relinquishes the bus at the end of the bus cycle. The bus controller supervises the handshaking between the local master CPU and the slave modules.

VME 1210 Slot 1 Master Set

VME 1210A

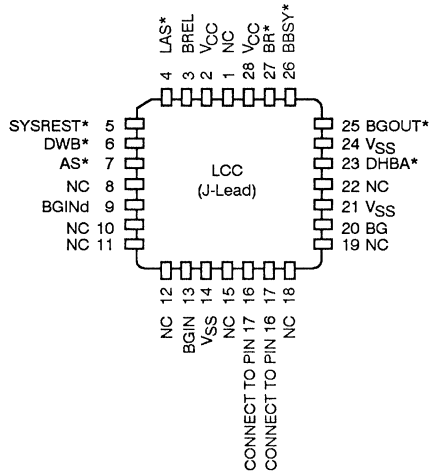


VME 1210B

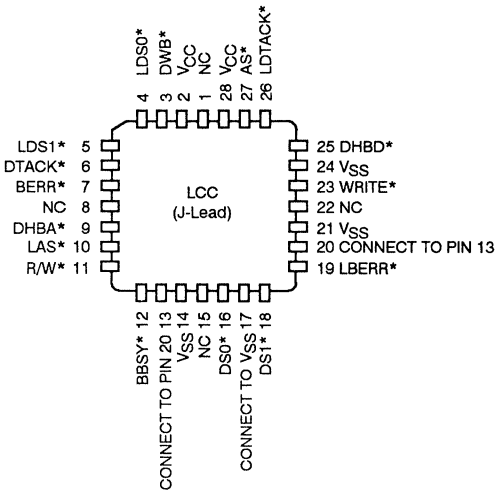


VME 1210 Slot 1 Master Set

VME 1210A

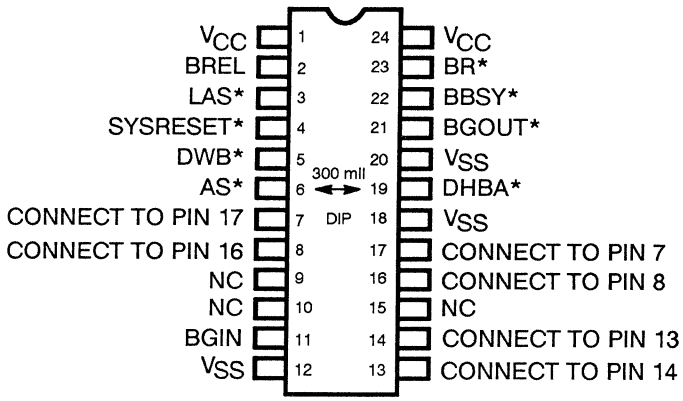


VME 1210B

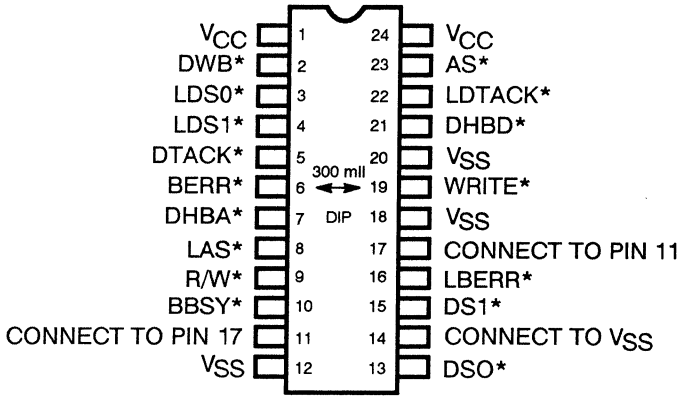


VME 1220 Non-Slot 1 Master Set

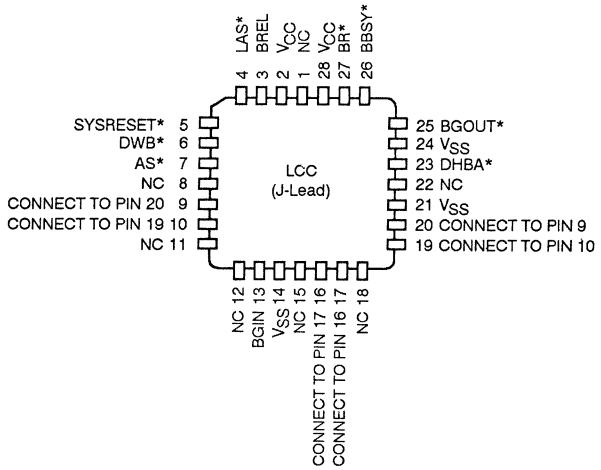
VME 1220A



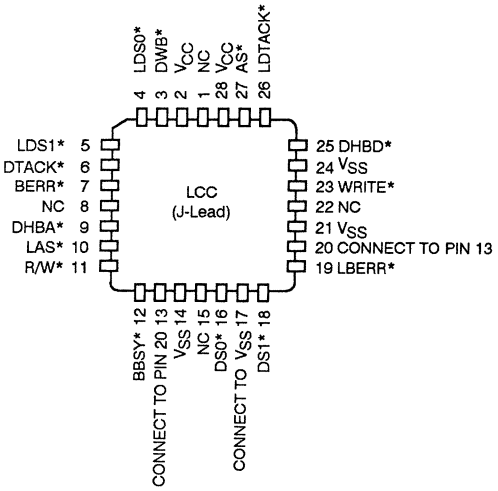
VME 1220B



VME 1220A



VME 1220B



Pin Descriptions

VME 1210A

Pin # LCC	Pin # DIP	Signal	Type	Function
3	2	BREL	I	Active high; Bus release signal indicating BBSY* can be released.
4	3	LAS*	I	Active low; Address strobe from local master.
5	4	SYSRESET*	I	Active low; VMEbus System Reset.
6	5	DWB*	I	Active low; Device wants bus, local master requests control of bus.
7	6	AS*	I	Active low; VMEbus Address Strobe.
9	7	BGINd	I	Active high; Delayed BG output via delay line.
10	8	NC	I	No Connect.
11	9	NC	I	No Connect.
12	10	NC	I	No Connect.
13	11	BGIN	I	Active high; Inverted VMEbus Bus Grant In signal, BGIN*.
14. 21, 24	12, 18, 20	V_{SS}		Chip Ground.
16	13	–	O	Connect to pin 14 (DIP) or pin 17 (LCC).
17	14	–	I	Connect to pin 13 (DIP) or pin 16 (LCC).
18	15	NC	O	No Connect.
19	16	NC	O	No Connect.
20	17	BG	O	Active high; Bus grant output from arbiter.
23	19	DHBA*	O	Active low; Device has bus address, address buffer enable.
25	21	BGOUT*	O	Active low; VMEbus Grant Out signal.
26	22	BBSY*	I/O	Active low; 48 mA open collector; VMEbus Bus Busy signal.
27	23	BR*	I/O	Active low; 48 mA open collector, VMEbus Bus Request signal.
2, 28	1, 24	V_{CC}		+5 V Chip Power.
1, 8, 15, 22	–	NC	–	No Connect.

VME 1220A

Pin # LCC	Pin # DIP	Signal	Type	Function
3	2	BREL	I	Active high; Bus release signal indicating BBSY* can be released.
4	3	LAS*	I	Active low; Address strobe from local master.
5	4	SYSRESET*	I	Active low; VMEbus System Reset.
6	5	DWB*	I	Active low; Device wants bus, local master requests control of bus.
7	6	AS*	I	Active low; VMEbus Address Strobe.
9	7	–	I	Connect to pin 17 (DIP) or pin 20 (LCC).
10	8	–	I	Connect to pin 16 (DIP) or pin 19 (LCC).
11	9	NC	I	No Connect.
12	10	NC	I	No Connect.
13	11	BGIN	I	Active high; Inverted VMEbus Bus Grant In signal, BGIN*.
14. 21, 24	12, 18, 20	V_{SS}		Chip Ground.
16	13	–	O	Connect to pin 14 (DIP) or pin 17 (LCC).
17	14	–	I	Connect to pin 13 (DIP) or pin 16 (LCC).
18	15	NC	O	No Connect.
19	16	–	O	Connect to pin 8 (DIP) or pin 10 (LCC).
20	17	–	O	Connect to pin 7 (DIP) or pin 9 (LCC).
23	19	DHBA*	O	Active low; Device has bus address, address buffer enable.
25	21	BGOUT*	O	Active low; VMEbus Grant Out signal.
26	22	BBSY*	I/O	Active low; 48 mA open collector; VMEbus Bus Busy signal.
27	23	BR*	O	Active low; 48 mA open collector, VMEbus Bus Request signal.
2, 28	1, 24	V_{CC}		+5 V Chip Power.
1, 8, 15, 22	–	NC	–	No Connect.

VME 1210B and VME 1220B

Pin # LCC	Pin # DIP	Signal	Type	Function
3	2	DWB*	I	Active low; Device wants bus; local master wants control of VMEbus.
4	3	LDS0*	I	Active low; Lower data strobe from local master.
5	4	LDS1*	I	Active low; Upper data strobe from local master.
6	5	DTACK*	I	Active low; VMEbus Data Transfer Acknowledge, data is valid during a read cycle or data has been accepted from the bus during a write cycle.
7	6	BERR*	I	Active low; VMEbus Error signal.
9	7	DHBA*	I	Active low; Device has bus address, address buffer enable.
10	8	LAS*	I	Active low; Address strobe from local master.
11	9	R/W*	I	Active high/low; Read or write cycle from local master.
12	10	BBSY*	I	Active low; VMEbus Busy, local master controls bus.
13	11	–	I	Connect to pin 17 (DIP) or pin 20 (LCC).
14. 21, 24	12, 18, 20	V_{SS}		Chip Ground.
16	13	DS0*	O	Active low; 64 mA VMEbus lower Data Strobe signal, indicates valid data on bus.
17	14	–	I	Connect to V_{SS}.
18	15	DS1*	O	Active low; 64 mA VMEbus upper Data Strobe signal, indicates valid data on bus.
19	16	LBERR*	O	Active low; Open collector signal, bus error to local master.
20	17	–	O	Connect to pin 11 (DIP) or pin 13 (LCC).
23	19	WRITE*	O	Active low; 48 mA VMEbus Write signal, indicates bus read or write cycle.
25	21	DHBD*	O	Active low; Device has bus data, data buffer enable.
26	22	LDTACK*	O	Active low; Open collector signal, data acknowledge to local master.
27	23	AS*	O	Active low; 64 mA VMEbus Address Strobe signal, indicates valid address on bus.
2, 28	1, 24	V_{CC}		+5 V Chip Power.
1, 8, 15, 22	–	NC	–	No Connect.

VME 1210/1220 General Information

	Commercial 0°C to +70°C	Industrial -40°C to +85°C	Military -55°C to +125°C
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic	Ceramic	Ceramic
High Drive Current Outputs (I_{OL})	To VMEbus spec (Up to 64 mA, Open Collector or Three-state)	To VMEbus spec (Up to 64 mA, Open Collector or Three-state)	To VMEbus spec (Up to 64 mA, Open Collector or Three-state)

VME 2000 VMEbus Slave Module Interface Device

Distinctive Features

- Provides logic, high current drive and buffers for slave module to VMEbus interface in 300 mil 24 pin DIP or 28 pin LCC package
- Supports Address Pipelining and Block Move Transfers
- Slave module selection in any VMEbus address space
- Drives 48 mA VMEbus DTACK* and BERR* signals
- Input Hysteresis filters bus noise
- Available in Commercial, Industrial, and Military temperature ranges

Applications

- Bus interface circuitry for VMEbus slave modules such as memories or I/O devices

General Description

The VME 2000 is a CMOS device which incorporates most of the logic required to interface a slave module, such as a memory or an I/O device, to the VMEbus. It is packaged in a compact 24 pin 300 mil wide DIP or 28 pin LCC. In a VMEbus system, the slave responds to a master and transfers data to and from a master. The protocols of the VME 2000 meet the VMEbus IEEE 1014 timing requirements. The devices buffers and drives the VMEbus signals to the IEEE 1014 electrical specifications.

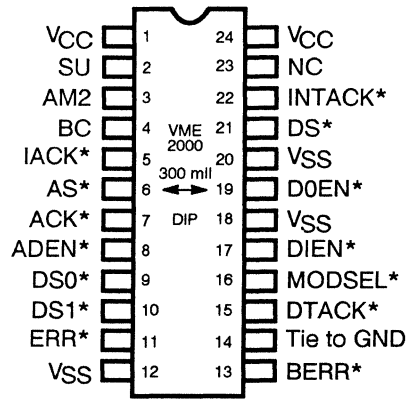
The VME 2000 supports address pipelining and block move data transfers. This part will function with any type of master module that meets the VMEbus specifications.

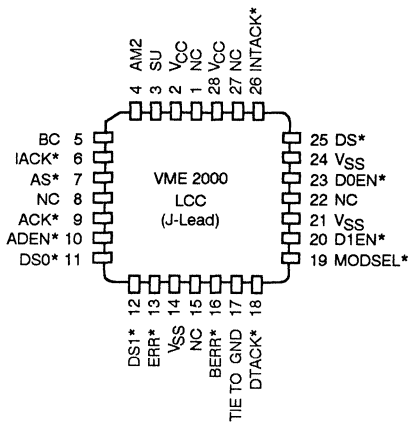
Pin Descriptions

VME 2000

28 Pin LCC	24 Pin DIP	Signal	Type	Function
2	1	V_{CC}	–	5 V Power Supply
3	2	SU	I	Active high; supervisor/user; when high, supervisor only transfers, when low, supervisor or non-supervisor modes (user)
4	3	AM2	I	Address modifier bit 2, for address size, cycle type.
5	4	BC	I	BERR* control, when high VME 2000 asserts BERR* if non-supervisor accesses are attempted when device is supervisor mode only, when low, BERR* control is disabled.
6	5	IACK*	I	Interrupt Acknowledge, denotes interrupt command.
7	6	AS*	I	Active low; Address Strobe, indicates valid address on bus.
9	7	ACK*	I	Active low, Data Acknowledge, local slave strobes ACK* to indicate data is available or accepted during read or write.
10	8	ADEN*	I	Active low, Address Enable, enable output from Address decoder.
11	9	DS0*	I	Active low, Data Strobe 0.
12	10	DS1*	I	Active low, Data Strobe 1, Data strobes indicate how many bytes are being transferred and indicate valid data on bus.
13	11	ERR*	I	Local Error.
14	12	V_{SS}	–	Chip Ground.
16	13	BERR*	I/O	Active low, Bus Error, indicates data transfer was not complete. 48 mA open collector.
17	14		I	Tie to GND.
18	15	DTACK*	I/O	Active low, Data Transfer Acknowledge, handshake to master indicating data is available or accepted during read or write, 48 mA open collector
19	16	MODSEL*	O	Active low, Module Select, the local slave module is selected if ADEN* in enabled and AM codes match.
20	17	DIEN*	O	Active low, Data One enable, upper case data byte enable.
21	18	V_{SS}	–	Chip Ground.
23	19	D0EN*	O	Active low, Data Zero Enable, lower case data byte enable.
24	20	V_{SS}	–	Chip Ground.
25	21	DS*	O	Active low, D0EN* or D1EN* active enables DS*.
26	22	INTACK*	I	Active low, Interrupt Acknowledge, from local slave's interrupt generator. When low, indicates interrupt cycle for this slave and enables MODSEL*.
27	23	NC	I	No Connect.
28	24	V_{CC}	–	5 V Power Supply
1, 8, 15, 22	–	NC	–	No Connect.

Packages





VME 2000 General Information

	Commercial 0°C to +70°C	Industrial -40°C to +85°C	Military -55°C to +125°C
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic	Ceramic	Ceramic
High Drive Current Outputs (I_{OL})	To VMEbus spec (Up to 48 mA, Open Collector or Three-state)	To VMEbus spec (Up to 48 mA, Open Collector or Three-state)	To VMEbus spec (Up to 48 mA, Open Collector or Three-state)

VME 3000/3010 VMEbus Interrupt Generator

Distinctive Features

- Provides random logic and high current drive for VMEbus interrupt generator in 300 mil 24 pin DIP or 28 pin LCC package
- IRQ* can be connected to any single interrupt request level
- Includes interrupter arbitration logic
- Drives 48 mA IRQ* signal
- Input hysteresis filters bus noise
- VME 3000 provides Release on Acknowledge operation
- VME 3010 provides Release on Register Access or Release on Acknowledge operation
- Available in Commercial, Industrial, and Military temperature ranges

Applications

- Single level interrupt generator logic for VMEbus slave modules generating an 8 bit interrupt vector

General Description

The VME 3000/3010 is a CMOS single level interrupt generator for the VMEbus which is packaged in a compact 24 pin 300 mil wide DIP or 28 pin LCC. The protocols of the VME 3000/3010 meet the VMEbus IEEE 1014 timing requirements. The device buffers and drives the VMEbus signals to the IEEE1014 electrical specifications.

The VME 3000/3010 will respond to an interrupt cycle when it receives IACKIN* fom the daisy chain. It arbitrates between IACKIN* and the interrupt request signal, compares priority levels and generates an interrupt acknowledge or IACKOUT* depending on which is appropriate.

The VME 3000 provides the Release on Acknowledge interrupter operation, while the VME 3010 provides both Release on Acknowledge and Release on Register Access.

This part will function with any interrupt handler and master module which meets the Rev. C.1 VMEbus specification.

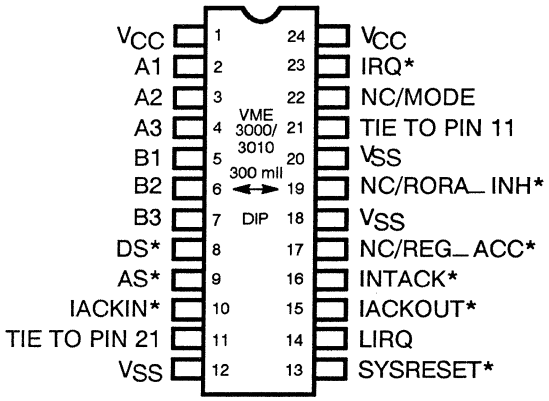
Pin Descriptions

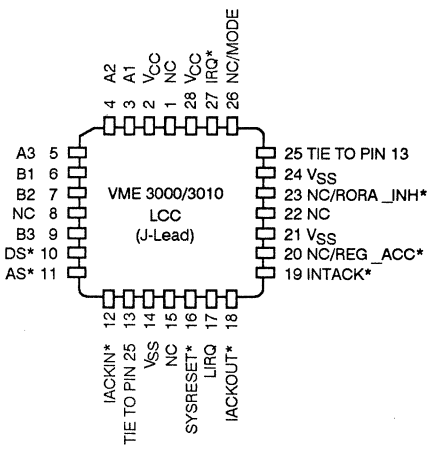
VME 3000/3010

28 Pin LCC	24 Pin DIP	Signal	Type	Function
2	1	V_{CC}	–	5 V Power Supply
3	2	A_1	I	Active high, Address bit 1; VME address bit.
4	3	A_2	I	Active high, Address bit 2; VME address bit.
5	4	A_3	I	Active high, Address bit 3; VME address bit.
6	5	B_1	I	Active high, Encode level bit 1; Encode bit for IRQ* priority level.
7	6	B_2	I	Active high, Encode level bit 2; Encode bit for IRQ* priority level.
9	7	B_3	I	Active high, Encode level bit 3; Encode bit for IRQ* priority level.
10	8	DS*	I	Active low, Data Strobe; DS0* for interrupt vector size.
11	9	AS*	I	Active low, VMEbus Address Strobe; Indicates valid address.
12	10	IACKIN*	I	Active low, Interrupt Acknowledge In; VMEbus IACK* daisy chain input.
13	11		I	Tie to pin 21 (DIP) or 25 (LCC).
14	12	V_{SS}	–	Chip Ground.
16	13	SYSRESET*	I	Active low, System Reset; VMEbus System Reset.
17	14	LIRQ	I	Active high, Local Interrupt Request; Interrupt Request from local slave.
18	15	IACKOUT*	O	Active low, Interrupt Acknowledge Out; IACK* daisy chain output if interrupt cycle does not belong to local slave.
19	16	INTACK*	O	Active low, Interrupt Acknowledge; VME 3000 generates INTACK* if interrupt cycle belongs to local slave.
20	17	NC/REG_ACC*	I	No connect on VME 3000. Register accessed input on VME 3010. Input used only in RORA mode. Indicates when the STATUS/ID register on the slave has been read to complete the RORA interrupt handling process. Assertion of this input causes IRQ* to be negated. Tie to GND if using VME 3010 ion ROAK mode.
21	18	V_{SS}	–	Chip Ground.
23	19	NC/RORA_INH*	I	No connect on VME 3000. LIRQ inhibit input to VME 3010. Input used only in RORA mode. Indicates when the 2 µsec window after the STATUS/ID register has been read is up. This window causes LIRQ from the slave to be ignored. When this input is negated, LIRQ will be sampled again by the VME 3010. Tie to GND if using the VME 3010 in ROAK mode.
24	20	V_{SS}	–	Chip Ground.
25	21		O	Tie to pin 11 (DIP) or pin 13 (LCC).
26	22	NC/MODE	I	No connect on VME 3000. Mode input to VME 3010. Indicates VME 3010 mode of operation: tie to GND to operated VME 3010 in ROAK mode: tie to V_{CC} to operate VME 3010 in RORA mode.
27	23	IRQ*	O	Active low, Interrupt Request; Interrupt request can be connected to any priority level, 48 mA OC.
28	24	V_{CC}	–	5 V Power Supply
1, 8, 15, 22	–	NC	–	No Connect.

Note: OC is Open Collector

Packages





VME 3000/3010 General Information

	Commercial 0°C to +70°C	Industrial -40°C to +85°C	Military -55°C to +125°C
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic	Ceramic	Ceramic
High Drive Current Outputs (I_{OL})	To VMEbus spec (Up to 48 mA, Open Collector or Three-state)	To VMEbus spec (Up to 48 mA, Open Collector or Three-state)	To VMEbus spec (Up to 48 mA, Open Collector or Three-state)

VME 4000 VMEbus Interrupt Handler

Distinctive Features

- Provides random logic and open collector drive for VMEbus interrupt handling in 300 mil 24 pin DIP or 28 pin LCC
- Monitors all seven interrupt levels
- Includes IACK-daisy chain driver for slot 1 configurations
- Directly drives open collector IACK* signal
- Works with PLX VME 1200 Master Controller or any other master controller that meets IEEE 1014
- Input hysteresis filters bus noise eliminating need for external buffers
- Available in Commercial, Industrial and Military temperature ranges

Applications

- Interrupt handler logic for VMEbus interrupts on master modules

Pin Descriptions

VME 4000

28-Pin LCC	24-Pin DIP	Signal	Type	Function
3	2	IRQ7*	I	Active low; VMEbus Interrupt Request level 7.
4	3	IRQ6*	I	Active low; VMEbus Interrupt Request level 6.
5	4	IRQ5*	I	Active low; VMEbus Interrupt Request level 5.
6	5	IRQ4*	I	Active low; VMEbus Interrupt Request level 4.
7	6	IRQ3*	I	Active low; VMEbus Interrupt Request level 3.
9	7	IRQ2*	I	Active low; VMEbus Interrupt Request level 2.
10	8	IRQ1*	I	Active low; VMEbus Interrupt Request level 1.
11	9	AS*	I	Active low; Data Address Strobe. Used in slot 1 IACK-daisy chain configurations only, otherwise should be tied high.
12	10	DS*	I	Active low; Logical AND of VMEbus Data Strobe DS0* and DS1*. Used in slot 1 IACK-daisy chain configurations only, otherwise should be tied high.
13	11	SYSRESET*	I	Active low; VMEbus system reset.
14, 21, 24	12, 18, 20	V_{SS}		Chip Ground.
16	13	INTREQ*	O	Active low, open collector, VMEbus interrupt request to local master (local interrupt)
17	14	VMEINTACK	I	Active high; VMEbus interrupt acknowledge from local master (IPL decode logic) to VME 4000.
18	15	IACK*	O	Active Low, open collector; Interrupt Acknowledge. Indicates interrupt acknowledge cycle occurring on VMEbus.
19	16	DHBA*	I	Active Low; Device has bus address. Indicates local master has control of the VME address bus.
20	17	IACKOUT*	O	Active low; Interrupt Acknowledge Out. IACK-daisy chain driver output. Used in slot 1 configurations only, otherwise should be left unconnected.
23	19	IACKIN*	O	Active low; Interrupt Acknowledge In. Input to IACK-daisy chain driver. Used in slot 1 configurations only, otherwise should be tied high.
25	21	A01*	O	Active high; Local master's address bus bit 1.
26	22	A02*	O	Active high; Local master's address bus bit 2.
27	23	A03*	–	Active high; Local master's address bus bit 3.
2, 28	1, 24	V_{CC}	–	+5 V Chip Power.
1, 8, 15, 22		NC	–	No Connect.

VME 4000 General Information

	Commercial 0°C to +70°C	Industrial -40°C to +85°C	Military -55°C to +125°C
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic	Ceramic	Ceramic
High Drive Current Outputs (I_{OL})	To VMEbus spec	To VMEbus spec	To VMEbus spec

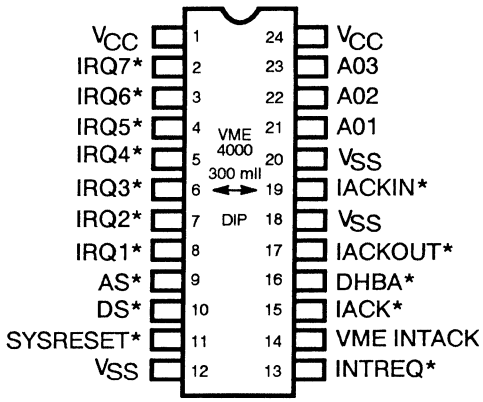
General Description

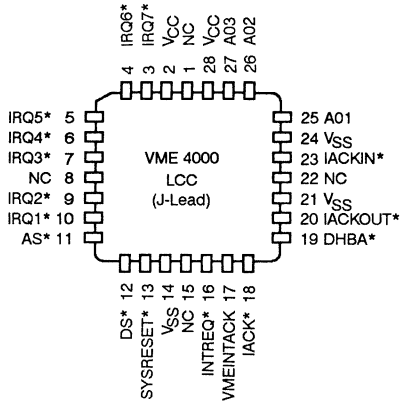
The VME 4000 is a CMOS seven level interrupt handler for VMEbus interrupts which is packaged in a compact 24 pin 300 mil wide DIP or 28 pin LCC. The VME 4000 meets the VMEbus IEEE 1014 timing and electrical requirements.

The VME 4000 will generate an interrupt request to the local master (via a local interrupt handler) when any of its seven VMEbus interrupt requests inputs is asserted. Once the master generates an interrupt acknowledge back to the VME 4000, it participates in a VMEbus interrupt acknowledge cycle by driving the appropriate interrupt level code onto the address bus as well as asserting IACK* on the bus.

If the VME 4000 is configured to be a slot 1 interrupt handler, it can provide the IACK-daisy chain driver function. The assertion of IACK* on the bus will cause the VME 4000 to drive IACKOUT* during the interrupt acknowledge cycle.

Packages





VSB Bus

VME Subsystem Bus (VSB) can be used in conjunction with the VMEbus to provide dedicated local memory or other subsystem functions. PLX offers single and multiple-master module interface devices plus a controller for slave applications:

- **VSB 1400** **Master Controller for Multimaster Systems**
- **VSB 1200** **Master Controller for Single Master Systems**
- **VSB 2000** **Controller for Slave Applications**

VSB 1400 VSB Master Module Interface Device

Distinctive Features

- Bus interface circuitry for multi-master VSB systems
- VSB master chip contains
  - Single level arbiter
  - Bus requester
  - Bus controller
  - Supports vectored interrupt acknowledge cycle
- Supports the following performance enhancing options
  - Block moves
  - Early Bus Busy release
- Drives 48mA VSB bus signals: BREQ*, DS*, BUSY*, PAS*
- Input hysteresis allows device to monitor VSB signals without additional input buffers
- Available in Commercial, Industrial and Military temperature ranges

Applications

- Bus interface circuitry for slot1 or non slot1 VSB master module in multi-master VSB systems

General Description

The VSB 1400 is a CMOS device which incorporates the protocol logic, drivers and buffers required to interface a master, typically a CPU, to the VSB (VME Subsystem Bus). It is packaged in compact 24 pin, 300 mil wide DIP or 28 pin LCC.

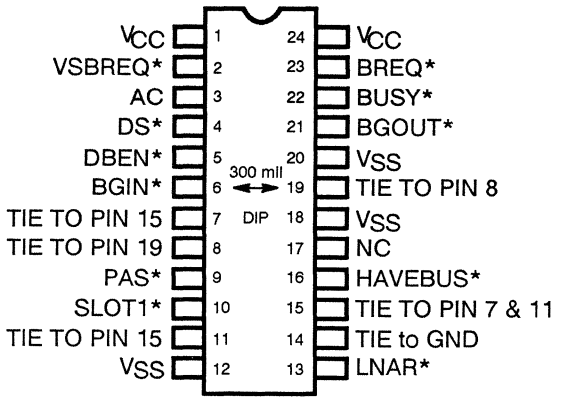
The VSB 1400 contains a VSB bus requester, controller and arbiter. The requester portion of the device asserts a VSB bus request in response to a request from the local master. The controller portion of the VSB 1400 supervises all the handshaking between the local master and the slaves. The VSB 1400 is designed to function in a multi-master VSB system, and can reside in any slot.

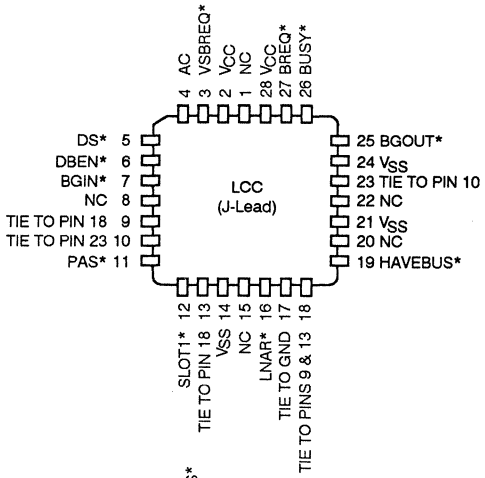
The protocols in the VSB 1400 are fully asynchronous.

This device is designed to function with any type of slave device or circuitry which meets the VSB specifications.

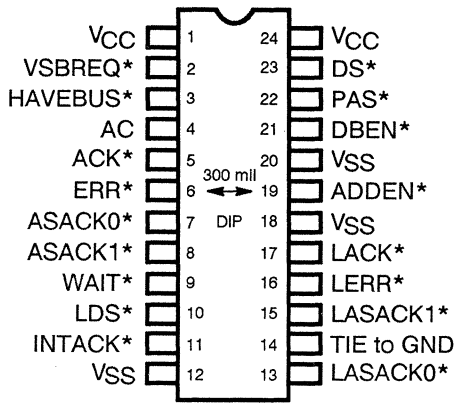
Packages

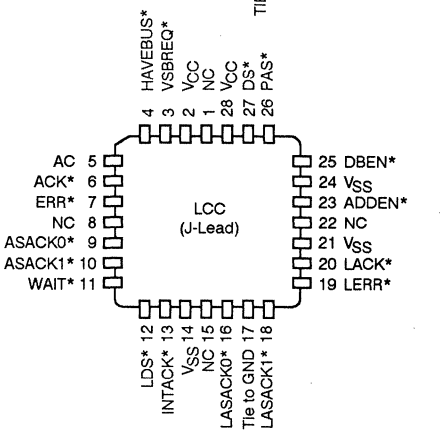
VSB 1400A





VSB 1400B





Pin Descriptions

VSB 1400A

Pin LCC	Pin DIP	Signal	I/O	Function
2	1	V_{CC}	—	5V supply.
3	2	VSBREQ*	I	Active low; Local master wants the bus.
4	3	AC	I	Active high; Indicates to master when address portion of VSB cycle is complete.
5	4	DS*	I	Active low; Indicates valid data on bus.
6	5	DBEN*	I	Active low; Data buffer enable
7	6	BGIN*	I	Active low; Bus Grant In from daisy chain or bus request input for slot1 applications.
9	7		I	Tie to pin 15 (DIP) or pin 18 (LCC).
10	8		I	Tie to pin 19 (DIP) or pin 23 (LCC).
11	9	PAS*	I	Active low; Indicates valid address on bus.
12	10	SLOT1*	I	Active high; Enables system arbiter for slot 1 masters.
13	11		I	Tie to pin 15 (DIP) or pin 18 (LCC).
14	12	V_{SS}	—	Chip Ground
16	13	LNAR*	O	Active low; Indicates to local master that single or block transfer cycle is complete.
17	14		I	Tie to Ground
18	15		O	Tie to pins 7 and 11 (DIP) or pins 9 and 13 (LCC).
19	16	HAVEBUS*	O	Active low; Indicates to local master that it owns the bus and enables the strobes.
20	17	NC	—	No Connect
21	18	V_{SS}		Chip Ground
23	19		O	Tie to pin 8 (DIP) or pin 10 (LCC).
24	20	V_{SS}	—	Chip Ground
25	21	BGOUT*	O	Active low; Bus Grant output to the daisy chain.
26	22	BUSY*	O	Active low; Indicates local master controls the bus, 48mA OC.
27	23	BREQ*	O	Active low; Bus request, 48mA OC.
28	24	V_{CC}	—	5V supply.
1, 8 15, 22		NC	—	No Connect

VSB 1400B

28-Pin LCC	24-Pin DIP	Signal	I/O	Function
2	1	V_{CC}	—	5V supply.
3	2	VSBREQ*	I	Active low; Local master wants the bus.
4	3	HAVEBUS*	I	Active low; Indicates to local master that it owns the bus and enables the strobes.
5	4	AC	I	Active high; Indicates to master when address portion of VSB cycle is complete.
6	5	ACK*	I	Active low; Data valid or has been accepted.
7	6	ERR*	I	Active low; Bus error or timeout has occurred.
9	7	ASACK0*	I	Active low; Byte size information and address transfer acknowledge.
10	8	ASACK1*	I	Active low; Byte size information and address transfer acknowledge.
11	9	WAIT*	I	Active low; VSB cycle extension or hold.
12	10	LDS*	I	Active low; local master data strobe.
13	11	INTACK*		Active low; Interrupt Acknowledge input, indicates that a vectored interrupt acknowledge cycle is being initiated by the local master. If not used, must tie high.
14	12	V_{SS}	—	Chip Ground
16	13	LASACK0*	O	Active low; Byte size information and address transfer acknowledge to local master.
17	14		I	Tie to Ground
18	15	LASACK1*	O	Active low; Byte size information and address transfer acknowledge to local master.
19	16	LERR*	O	Active low; Bus error or timeout to local master.
20	17	LACK*	O	Active low; Data validation or acceptance to local master.
21	18	V_{SS}	—	Chip Ground
23	19	ADDEN*	O	Active low; Address buffer enable.
24	20	V_{SS}	—	Chip Ground
25	21	DBEN*	O	Active low; Data buffer enable.
26	22	PAS*	I/O	Active low; Indicates valid address on bus, 48mA OC.
27	23	DS*	I/O	Active low; Indicates valid data on bus 48mA OC.
28	24	V_{CC}	—	5V supply.
1, 8 15, 22		NC	—	No Connect

VSB 1400 General Information (Two Chip Set)

	Commercial 0°C to +70°C	Industrial -40°C to +85°C	Military -55°C to +125°C
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic	Ceramic	Ceramic
High Drive Current Outputs (I_{OL})	To VSB bus spec (Up to 48mA Open Collector or Three-state)	To VSB bus spec (Up to 48mA Open Collector or Three-state)	To VSB bus spec (Up to 48mA Open Collector or Three-state)

VSB 1200 Master Module Interface Device

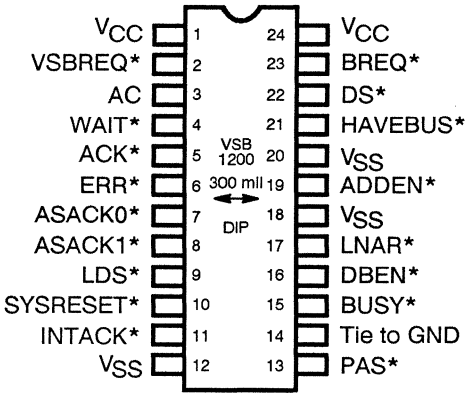
Distinctive Features

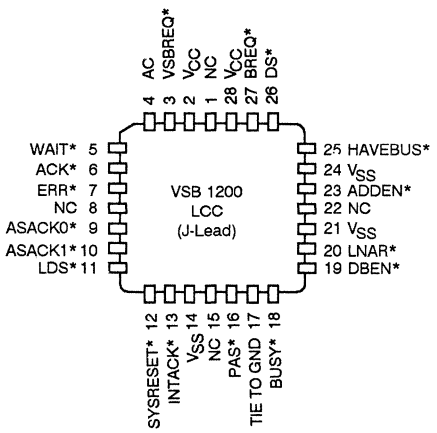
- Bus interface circuitry for single master VSB systems
- VSB master chip contains
  - Single level arbiter
  - Bus requester
  - Bus controller
  - Vectored interrupt acknowledge cycle logic
- Supports the following performance enhancing options
  - Block moves
  - Early Bus Busy release
- Drives 48mA VSB bus signals: DS*, BUSY*, PAS*
- Input hysteresis allows device to monitor VSB signals without additional input buffers
- Available in Commercial, Industrial and Military temperature ranges

Applications

- Bus interface circuitry for VSB master in single master VSB systems

Packages





VSB 1200 General Information

	Commercial 0°C to +70°C	Industrial -40°C to +85°C	Military -55°C to +125°C
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic	Ceramic	Ceramic
High Drive Current Outputs (I_{OL})	To VSB bus spec (up to 48mA, Open Collector or Three-state)	To VSB bus spec (up to 48mA, Open Collector or Three-state)	To VSB bus spec (up to 48mA, Open Collector or Three-state)

General Description

The VSB 1200 is a CMOS device which incorporates the protocol logic, drivers and buffers required to interface a master, typically a CPU, to the VSB (VME Subsystem Bus). It is packaged in a compact 24 pin, 300 mil wide DIP or 28 pin LCC.

The VSB 1200 contains a VSB bus requester, controller and arbiter. The requester portion of the device asserts a VSB bus request in response to a request from the local master. The controller portion of the VSB 1200 supervises all the handshaking between the local master and the slaves. Because the VSB 1200 is designed to work in a single master VSB system, the arbiter portion of the device always grants the bus to the local master.

The protocols in the VSB 1200 are fully asynchronous.

This device is designed to function with any type of slave device or circuitry which meets the VSB specifications.

Pin Descriptions

VSB 1200

28-Pin LCC	24-Pin DIP	Signal	I/O	Function
3	2	VSBREQ*	I	Active low; Local master wants the bus.
4	3	AC	I	Active high; Indicates to master when address portion of VSB cycle is complete.
5	4	WAIT*	I	Active low; VSB cycle should not be terminated until WAIT* is deasserted.
6	5	ACK*	I	Active Low*; Informs local master that data is valid or has been accepted.
7	6	ERR*	I	Active Low; Informs local master that there is a bus error or a time-out has occurred.
9	7	ASACK0*	I	Active low; Informs master of byte size and that slaves acknowledge are ready for the data cycle.
10	8	ASACK1*	I	Active low; Informs master of byte size and that slaves acknowledge are ready for the data cycle.
11	9	LDS*	I	Active Low; Data strobe from local master.
12	10	SYSRESET*	I	Active low; System reset input, initializes the VSB 2000 and should be tied to the VME SYSRESET* line or the local master's reset line.
13	11	INTACK*	I	Active low; Interrupt Acknowledge Input, Indicates that a vectored interrupt acknowledge cycle is being initiated by the local master. If not used, must tie high.
14, 21, 24	12, 18, 20			Chip Ground
16	13	PAS*	O	Active Low; Indicates valid address on bus; 48mA TS.
17	14		I	Tie to Ground
18	15	BUSY*	O	Active low; Indicates to local master that single or block transfer cycle is complete.
19	16	DBEN*	I	Active Low; Data buffer enable.
20	17	LNAR*	O	Active Low; Informs local master that single or block required transfer cycle is complete.
23	19	ADDEN*	O	Active Low; Address buffer enable.
25	21	HAVEBUS*	O	Active Low; Informs local master that it owns bus and enables address and data strobes.
26	22	DS*	–	Active Low; Indicates valid data on bus; 48mA TS.
27	23	BREQ*		Active low; VSB bus request; 48 mA OC.
2, 28	1, 24	V_{CC}	–	5V supply.
1, 8 15, 22		NC	–	No Connect

Note: TS is Tri-state
OC is Open Collector

VSB 2000 Slave Module Interface Device

Distinctive Features

- Provides logic, high current drive and buffers for slave module to VSB bus interface in slim 24 pin DIP or 28 pin LCC package
- Supports Block Transfers
- Drives 48 mA open collector VSB signals: AC, WAIT*, ACK* and ERR*
- Input hysteresis allows device to monitor VSB signals without additional input buffers
- Available in Commercial, Industrial and Military temperature ranges

Applications

- Bus interface circuitry for VSB slave modules such as memories or I/Os functioning as responding or participating slaves

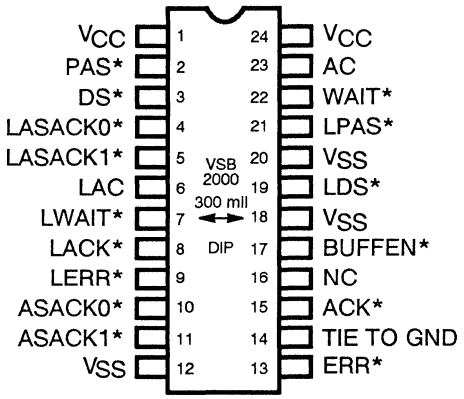
General Description

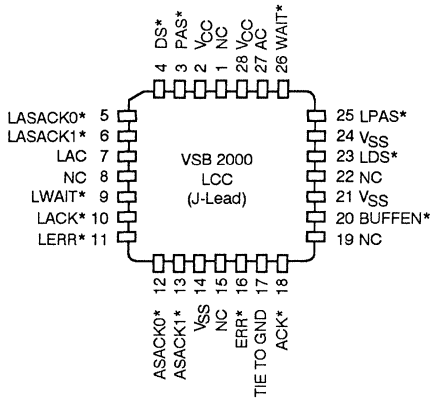
The VSB 2000 is a CMOS device which incorporates the protocol logic, drivers and buffers required to interface a slave module, such as memory or I/O device, to the VSB (VME Subsystem Bus). It is packaged in a compact 300 mil wide 24 pin DIP or 28 pin LCC.

The protocols in the VSB 2000 are fully asynchronous.

This device is designed to function with any type of master device or circuitry which meets the VSB specifications.

Packages





Pin Descriptions

VSB 2000

28 Pin LCC	24 Pin DIP	Signal	Type	Function
3	2	PAS*	I	Active low; indicates valid address on VSB bus strobe.
4	3	DS*	I	Active low; indicates valid data on VSB bus.
5	4	LASACK0*	I	Active low; acknowledges address cycle and contains byte size information from local slave.
6	5	LASACK1*	I	Active low; acknowledges address cycle and contains byte size information from local slave.
7	6	LAC	I	Active high; output of counter indicating slave has finished addressing range in block transfer "ANDed" with output of address decoder indicating address decode complete.
9	7	LWAIT*	I	Active low; output from local slave indicating when participating slave's cache operation is done.
10	8	LACK*	I	Active low; local slave indicating available for accepted data on bus.
11	9	LERR*	I	Active low; local slave indicating an error.
12	10	ASACK0*	I	Active low; Bus ASACK0* signal from responding slave.
13	11	ASACK1*	I	Active low; Bus ASACK1* signal from responding slave.
14, 21, 24	12, 18, 20	V_{SS}	—	Chip Ground.
16	13	ERR*	O	Active low; Bus error, 48 mA OC.
17	14		I	Tie to GND.
18	15	ACK*	O	Active low; indicates available or accepted data on bus 48 mA OC.
19	16	NC		No Connect.
20	17	BUFFEN*	O	Active low; data buffer enable.
23	19	LDS*	O	Active low; indicates valid data cycle to local slave.
25	21	LPAS*	O	Active low; indicates valid address on bus to local slave.
26	22	WAIT*	O	Active low; informs master not to terminate cycle until WAIT* is negated; 48 mA OC.
27	23	AC	I/O	Active high; informs master address cycle is complete; 48 mA OC complete.
2, 28	1, 24	V_{CC}	—	5 Volt power supply.
1, 8, 15, 22	—	NC	—	No Connect.

Note: OC is Open Collector

VSB 2000 General Information

	Commercial 0°C to +70°C	Industrial -40°C to +85°C	Military -55°C to +125°C
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic	Ceramic	Ceramic
High Drive Current Outputs (I_{OL})	To VSB bus spec (up to 48mA, Open Collector or Three-state)	To VSB bus spec (up to 48mA, Open Collector or Three-state)	To VSB bus spec (up to 48mA, Open Collector or Three-state)

Multibus I & II

Both Multibus I and Multibus II are supported by PLX ICs. PLX offers a solution which emulates the Intel 8289 but with lower power consumption (250mW) and a maximum processor clock rate of 16MHz. Multibus II interface chips include slave interface devices for the 32-bit Parallel System Bus (PSB™) and its local extension bus (iLBX™). The part numbers are as follows:

- **MBI 8289A/B** **Multibus I iAPX 86/88/186 Bus Arbiter**
- **PSB 2000** **PSB II Reply Only Agent Controller**
- **PSB 2100** **PSB II Reply Only Agent Error Generator**
- **LBX 2000** **LBX II Reply Only Agent Controller**
- **LBX 2100** **LBX II Reply Only Agent Address Error Generator**

MBI 8289A/8289B Multibus I iAPX 86/88/186 Bus Arbiter

Distinctive Features

- Emulates Intel 8289 Bus Arbiter, however, not pin for pin compatible. Please refer to pinout diagram.
- Provides arbitration of multiple masters on MULTIBUS I. Provides convenient arbitration for iAPX 86, 88, and 186 microprocessors in one package.
- Supports all four modes of the Intel 8289/8289-1 Bus Arbiter (8289A = single bus only, system/resident bus; 8289B = system/IO bus, and system/resident/IO bus).
- Can operate with microprocessors up to 20 mHz.
- Capable of directly driving both open collector and totem pole signals for arbitration.
- Handles other strappable options such as ANYRQST and CRQLCK*.

Applications

- Arbitration for iAPX 86,88,186 microprocessors on the MULTIBUS I system bus.

General Description

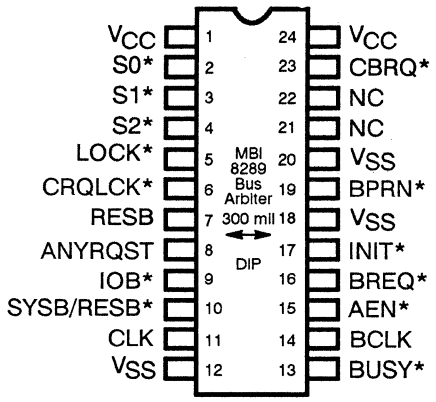
The MBI 8289 is a CMOS bus arbiter for iAPX 86/88/186 microprocessors interfacing to the MULTIBUS I multi-master system bus. It is packaged in a compact 300 mil slimline 24 pin DIP or 28 pin J-lead PLCC/LCC. The MBI 8289 works in conjunction with the bus controller to provide a complete interface to the multi-master MULTIBUS I system bus. The microprocessor is unaware of the MBI 8289's existence. When requesting a transfer on the MULTIBUS I system bus, the MBI 8289 prevents the bus controller, data transceivers and address latches from accessing the bus. Once the MULTIBUS I bus is obtained, the MBI 8289 signals the bus controller to continue with the access.

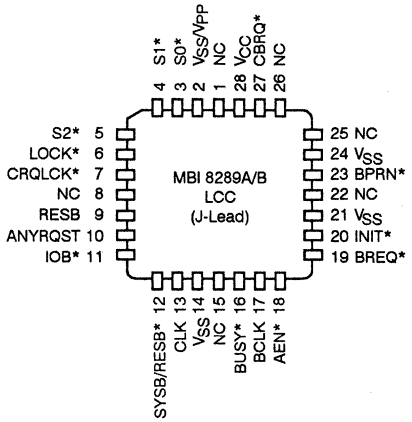
The MBI 8289 supports parallel arbitration resolution via the BREQ* output and BPRN* input pins. Please contact the factory if serial arbitration resolution is desired.

The MBI 8289 can support all four operating modes. These modes are selected via the RESB and IOB* input pins. The MBI 8289A supports the system bus only mode and the system/resident bus mode, while the MBI 8289B supports the IO bus/system bus and system/resident/IO bus modes. In addition, the MBI can support other strappable options, such as common bus request locking (CBRLCK*) and bus surrendering upon any request (ANYRQST).

The MBI 8289 is capable of supporting microprocessor speeds of up to 20 MHz and bus speeds up to10 MHz.

Packages





Pin Descriptions

MBI 8289A/8289B

Pin # LCC	Pin # DIP	Signal	I/O	Function
3	2	S0*	I	Active low; Status pin S0* from processor.
4	3	S1*	I	Active low; Status pin S1* from processor.
5	4	S2*	I	Active low; Status pin S2* from processor.
6	5	LOCK*	I	Active low; LOCK input from processor. Indicates LOCKed transaction on MULTIBUS I.
7	6	CRQLCK*	I	Active low; Input that prevents MBI 8289 from surrendering the bus to any other arbiter requesting the bus through the CBRQ* input.
9	7	RESB	I	Active high; A strappable option indicating that the MBI 8289 is operating in a system having both a multi-master system bus and a resident bus.
10	8	ANYRQST	I	Active high; A strappable option that permits the master to surrender the bus to a lower priority requesting master.
11	9	IOB*	I	Active low; A strappable option that allows the MBI 8289 to operate in a system having an I/O and multi-master system bus.
12	10	SYSB/RESB*	I	Active high; Indicates processor wishes to perform MULTIBUS I transaction when in resident bus mode (RESB strapped high). This pin is ignored if RESB is strapped low.
13	11	CLK	I	Processor CLK.
14, 21, 24	12, 18, 20	V_{SS}	–	Chip Ground
16	13	BUSY*	I/O	Active low, open collector; Output indicating this master has control of the bus and is driving address and command signals. Input indicating when the multi-master bus is available.
17	14	BCLK	I	Inverted BCLK*;
18	15	AEN*	O	Active low; Output indicating this processor has control of the MULTIBUS I system bus. Used to enable address and command onto the bus.
19	16	BREQ*	O	Active low, open collector; Output used to request use of the MULTIBUS I system bus. Generally routed to system arbiter.
20	17	INIT*	I	Active low; Input causing the device to initialize to the idle state.
23	19	BPRN*	I	Active low; Input indicating this device has priority on the bus starting on the next falling BCLK* edge.
25	21	NC	O	No Connect
26	22	NC	O	No Connect
27	23	CBRQ*	I/O	Active low, open collector; Input indicating that there is a lower priority arbiter requesting use of the multi-master bus. Output from a lower priority arbiter requesting use of the multi-master bus.
2, 28	1, 24	V_{CC}	–	+5V Chip Power
1, 8 15, 22	–	NC	–	No Connect

MBI 8289A/8289B General Information

	Commercial 0°C to +70°C	Industrial -40°C to +85°C	Military -55°C to +125°C
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic	Ceramic	Ceramic
Speed	Processor frequency 16.7, 22* MHz	Processor frequency 14, 18* MHz	Processor frequency 12.5, 15* MHz
High Drive Current Outputs (I_{OL})	To MBI spec (up to 20mA, Open Collector or Three-state)	To MBI spec (up to 20mA, Open Collector or Three-state)	To MBI spec (up to 20mA, Open Collector or Three-state)

*Contact PLX for availability

PSB 2000 PSB II Reply Only Agent Controller

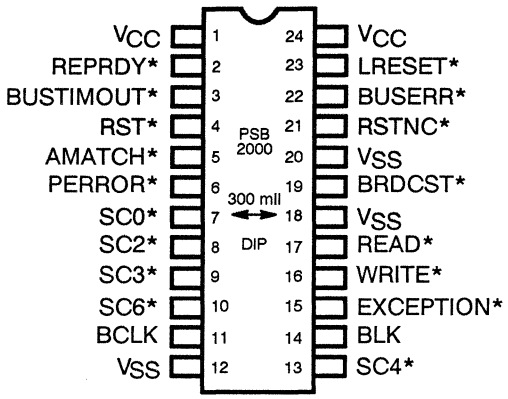
Distinctive Features

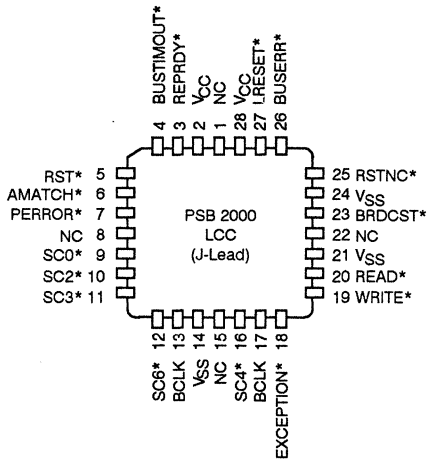
- Provides a Reply Only Agent Control Interface to iPSB II bus.
- Does not require external microcontroller or microprocessor to configure.
- Packaged in compact 300 mil 24 pin DIP or 28 pin J-lead LCC.
- Integrates 60 mA open collector driver required on BUSERR* and 64 mA three-state driver required on SC4* bus signals.
- Provides data transceiver direction signals READ* and WRITE*.
- Provides high current (64mA), open collector local reset (LRESET*) and exception signals (EXCEPTION*).
- Supports sequential transfer operations including broadcast.
- Can be used separately or together with PSB 2100 to provide complete reply agent control interface to iPSB II bus.

Applications

- Bus Interface Circuitry for iPSB II reply only agent modules such as I/O or memory devices.

Packages





PSB 2000 General Information

	Commercial (0°C to +70°C)
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic
High Drive Current Outputs (I_{OL})	To MBII spec (up to 64 mA, Open Collector or Three-state)

General Description

The PSB 2000 is a CMOS iPSB II Reply Only Agent controller packaged in a 300 mil 24 pin DIP or 28 pin J-lead LCC. The iPSB II bus is the Parallel System Bus of MULTIBUS II. The PSB 2000 contains the reply agent state machine and can drive the 64 mA three-state SC4* (replier ready) signal directly. To aid the system board designer, the device also provides separate READ* and WRITE* outputs indicating the direction of the transfer. The PSB 2000 is also capable of driving the BUSERR* signal (60 mA open collector) if a parity error occurs during the data transfer cycle. Finally, the PSB 2000 provides local buffered reset and exception signals (LRESET* and EXCEPTION*).

The PSB 2000 conforms to the Rev. C MULTIBUS II Bus Architecture Specification Handbook.

The PSB 2000 can be used separately to provide the reply only agent control interface to the iPSB II bus. In this manner, the SC5* - SC8* signals must be generated independently.

The PSB 2000 can be used in conjunction with the PSB 2100 where the 2100 is used to generate the SC5* - SC8* signals and the PSB 2000 is used to generate the SC4* signal and BUSERR* signals. In this manner, the two chip set provides a compact interface to the iPSB II bus.

Pin Descriptions

PSB 2000

28 Pin LCC	24 Pin DIP	Signal	Type	Function
3	2	REPRDY*	I	Active low; Reply agent ready to conduct data transfer in next cycle.
4	3	BUSTIMOUT*	I	Active low; Bus timeout. Causes device to re-initialize.
5	4	RST*	I	Active low; Reset. Causes device to re-initialize.
6	5	AMATCH*	I	Active low; Reply Agent match. Indicates this module is being accessed.
7	6	PERROR*	I	Active low; Parity error on PSB bus. Indicates parity error on SCn* or AD0-31* lines.
9	7	SC0*	I	Active low; Status/Control bit 0. Indicates request or not request cycle.
10	8	SC2*	I	Active low; Status/Control bit 2. Indicates end of cycle during reply cycles.
11	9	SC3*	I	Active low; Status/Control bit 3. Indicates requester ready during reply cycles.
12	10	SC6*	I	Active low; Status/Control bit 6. Indicates read/write* during request cycle.
13	11	BCLK	I	Inverted BCLK*. Connected to pin 14 (DIP) or pin 17 (LCC).
14, 21, 24	12, 18, 20	V_{SS}		Chip Ground.
16	13	SC4*	I/O	Active low, 64 mA three-state; Status/Control bit 4. Indicates replier ready during reply cycles.
17	14	BCLK	I	Inverted BCLK*. Connected to pin 11 (DIP) or pin 13 (LCC).
18	15	EXCEPTION*	O	Active low, 64 mA open collector; Indicates either BUSTIMOUT* or BUSERR* has been asserted.
19	16	WRITE*	O	Active low; Indicates write to this agent.
20	17	READ*	O	Active low; Indicates read from this agent.
23	19	BRDCST*	I	Active low: Broadcast. Input indicating when a broadcast operation is occurring.
25	21	RSTNC*	I	Active low; Reset Not Clear. Indicates a reset is not complete by the system.
26	22	BUSERR*	I/O	Active low, 60 mA open collector; Bus error. Indicates a bus error has occurred.
27	23	LRESET*	O	Active low, 64 mA open collector; Local reset. Reset from bus.
2, 28	1, 24	V_{CC}		+5 V Chip Power.
1, 8, 15, 22	–	NC	–	No Connect.

PSB 2100 PSB II Reply Only Agent Error Generator

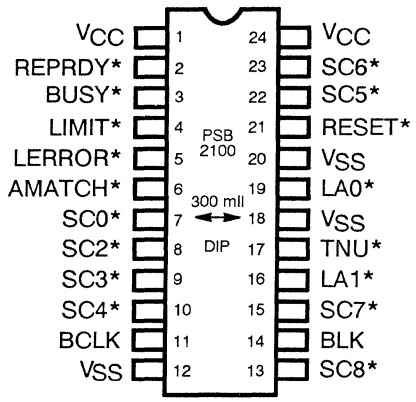
Distinctive Features

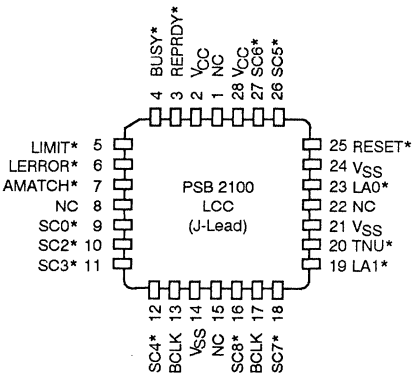
- Provides complete memory/IO error code generation including: width errors, transfer-not-understood errors, NACK errors, local data errors, and continuation errors for 8 bit reply only agents.
- Provides a parity signal (SC8*) over reply agent SC4* - SC7* signals.
- Integrates 64 mA three-state drivers required on SC5* - SC8* bus signals.
- Packaged in compact 300 mil 24 pin DIP or 28 pin J-lead LCC.
- Supports sequential operations including broadcast.
- Can be used separately or together with PSB 2000 to provide complete reply only agent control interfact to iPSB II bus.

Applications

- Bus Interface Circuitry for iPSB II reply only agent modules such as I/O or memory devices.

Packages





PSB 2100 General Information

	Commercial (0°C to +70°C)
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic
High Drive Current Outputs (I_{OL})	To MBII spec (up to 64 mA, Open Collector or Three-state)

General Description

The PSB 2100 is a CMOS iPSB II 8 bit Reply Only Agent error generator packaged in a 300 mil 24 pin DIP or 28 pin J-lead LCC. The PSB 2100 provides complete reply only agent memory/IO space error code generation and can drive the 64 mA three-state SC5* - SC8* signals directly. The PSB 2100 supports 8 bit memory or I/O accesses as well as 8 bit interconnect accesses and 32 bit messages. During the reply phase of the transfer the PSB 2100 will assert the appropriate error code and parity bit indicating either a valid transfer or and error condition due to width errors, transfer-not-understood errors, NACK errors, local data errors, or continuation errors. Other local errors can also be asserted to the PSB 2100 which will cause the transfer-not-understood error code to be generated. All errors are detected on memory and IO accesses only. Interconnect and message transfers are not checked for errors.

The PSB 2100 conforms to the Rev. C MULTIBUS II Bus Architecture Specification Handbook.

The PSB 2100 can be used separately to generate the SC5* - SC8* signals for the reply agent module that does not use the PSB 2000 as the reply only agent controller.

The PSB 2000 can be used in conjunction with the PSB2100 where the 2100 is used to generate the SC5* - SC8* signals and the PSB 2000 is used to generate the SC4* signal and BUSERR* signals. In this manner, the two chip set provides a compact interface to the iPSB II bus.

Pin Descriptions

PSB 2100

Pin # LCC	Pin # DIP	Signal	Type	Function
3	2	REPRDY*	I	Active low; Replier ready to conduct data transfer in next cycle.
4	3	BUSY*	I	Active low; Replier busy. Indicates replier can not reply now.
5	4	LIMIT*	I	Active low; Address limit. Indicates replier has reached address range limit.
6	5	LERROR*	I	Active low; Local error. Indicates local parity error.
7	6	AMATCH*	I	Active low; Address match. Indicates transfer is for this reply agent.
9	7	SC0*	I	Active low; Status/Control bit 0. Indicates request and non-request cycles.
10	8	SC2*	I	Active low; Status/Control bit 2. Indicates end of cycle during reply cycles.
11	9	SC3*	I	Active low; Status/Control bit 3. Indicates requester ready during reply cycles.
12	10	SC4*	I	Active low; Status/Control bit 4. Indicates replier ready during reply cycles.
13	11	BCLK	I	Inverted BCLK*. Connected to pin 14 (DIP) or pin 17 (LCC).
14, 21, 24	12, 18, 20	V_{SS}		Chip Ground.
16	13	SC7*	O	Active low, 64 mA three-state; Status/Control bit 7. Error code output bit.
17	14	BCLK	I	Inverted BCLK*. Connected to pin 11 (DIP) or pin 13 (LCC).
18	15	SC8*	O	Active low; 64 mA three-state; Parity bit for SC4* - SC7* during reply cycles.
19	16	LA1*	I	Active low Latched address bit A1*.
20	17	TNU*	I	Active low; Transfer-not-understood error (externally generated).
23	19	LA0*	I	Active low; Latched address bit A0*.
25	21	RESET*	I	Active low; Logical 'OR' of local reset and local exception.
26	22	SC6*	O	Active low; 64 mA three-state; Status/Control bit 6. Error code output bit.
27	23	SC5*	O	Active low; 64 mA three-state; Status/Control bit 5. Error code output bit.
2, 28	1, 24	V_{CC}		+5 V Chip Power.
1, 8, 15, 22	–	NC	–	No Connect.

LBX 2000 LBX II Reply Agent Controller

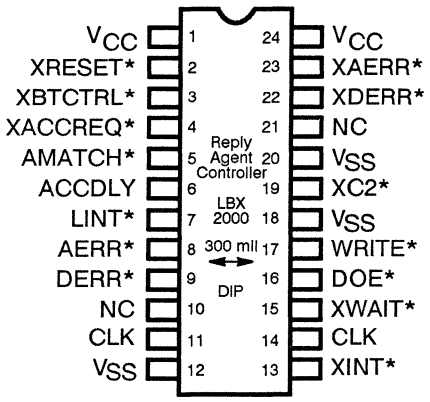
Distinctive Features

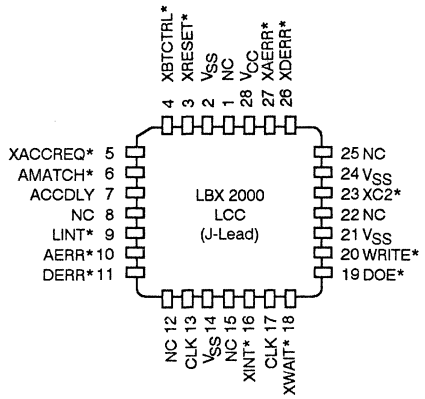
- Provides a Reply Agent Control Interface to iLBX II bus.
- Packaged in compact 300 mil 24 pin DIP or 28 pin J-lead LCC.
- Integrates 60 mA open collector drivers required on XWAIT*, XINT*, XDERR*, and XAERR* iLBX II signals.
- Provides data transceiver direction (WRITE*) and output enable (DOE*) control signals.
- Supports pipelined and block transfer operations.
- Can be used separately or together with LBX 2100 to provide complete reply agent control interface to iLBX II bus.

Applications

- Bus Interface Circuitry for iLBX II reply agent modules such as I/O or memory devices.

Packages





LBX 2000 General Information

	Commercial (0 °C to +70 °C)
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic
High Drive Current Outputs (I_{OL})	To MBII spec (up to 64 mA, Open Collector or Three-state)

General Description

The LBX 2000 is a CMOS iLBX II reply agent controller packaged in a 300 mil 24 pin DIP or 28 pin J-lead LCC. The iLBX II bus is the Local Bus Extension to the MULTIBUS II bus. The LBX 2000 contains the reply agent state machine and can drive the 60mA open collector XWAIT* signal directly. To aid the system board designer, the device also provides a WRITE* signal indicating the direction of the transfer and a data output enable signals (DOE*) to control the data buffers on the reply agent board. The LBX 2000 is also capable of driving the XDERR* (60 mA open collector) at the appropriate times on the bus if an error occurs during the data transfer cycle. Finally, the LBX 2000 provides clocked buffering of XINT* and XAERR* which are also 60mA open collector signals.

The LBX 2000 conforms to the Rev. C MULTIBUS II Bus Architecture Specification Handbook.

The LBX 2000 can be used separately to provide the reply agent control interface to the iLBX II bus. In this manner, the AERR* input to the LBX 2000 provides a flexible means for the designer to generate XAERR* signal. The LBX 2000 simply provides a synchronized buffering function for the XAERR* signal. The LBX 2100 can also be used separately to generate the XAERR* signal for the reply agent module that does not use the LBX 2000 as the reply agent controller.

The LBX 2000 can be used in conjunction with the LBX 2100 where the 2100 is used to generate the XAERR* signal instead of the LBX 2000. In this manner, the two chip set provides a compact interface to the iLBX II bus.

Pin Descriptions

LBX 2000

28-Pin LCC	24-Pin DIP	Signal	I/O	Function
3	2	XRESET*	I	Active low; System bus reset.
4	3	XBTCTRL*	I	Active low; Block transfer control. Indicates a block transfer cycle on bus.
5	4	XACCREQ*	I	Active low; Access request. Indicates valid address cycle on bus.
6	5	AMATCH*	I	Active low; Reply Agent match. Indicates this module is being accessed.
7	6	ACCDLY	I	Active high; Access delay. Induces wait states into access.
9	7	LINT*	I	Active low; Local Interrupt. Causes XINT* to be synchronously asserted on bus.
10	8	AERR*	I	Active low; Agent error. Causes XAERR* to be sychronously asserted on bus.
11	9	DERR*	I	Active Low; Data error. Indicates data bus error during transfer.
12	10	NC	I	No Connect.
13	11	CLK	I	Inverted XBCLK*. Connect to pin 14 (DIP) or pin 17 (LCC).
14, 21, 24	12, 18, 20	VSS		Chip Ground
16	13	XINT*	O	Active Low, 64 mA open collector; Interrupt output.
17	14	CLK	I	Inverted XBCLK*. Connect to pin 11 (DIP) or pin 13 (LCC).
18	15	XWAIT*	O	Active low, 64 mA open collector; Wait State Indicator
19	16	DOE*	O	Active low; Data output enable for data buffers.
20	17	WRITE*	O	Active low; Read/Write* Indicator.
23	19	XC2*	I	Active low; Command bit from bus.
25	21	NC	O	No Connect.
26	22	XDERR*	O	Active low, 64 mA open collector; Data portion bus error output.
27	23	XAERR*	O	Active low, 64 mA open collector; Address portion bus error output.
2, 28	1, 24	VCC		+5V Chip Power
1, 8 15, 22		NC	—	No Connect.

LBX 2100 LBX II Reply Agent Address Error Generator

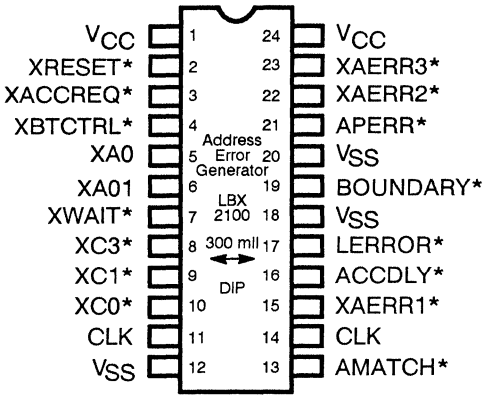
Distinctive Features

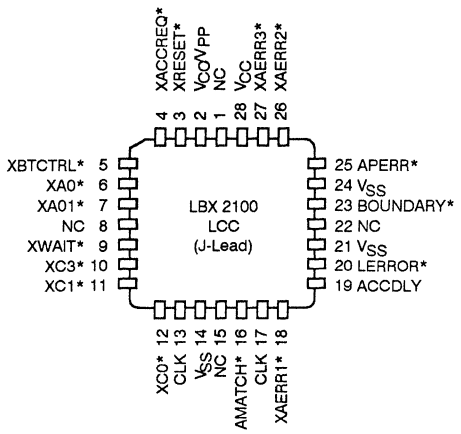
- Provides complete XAERR* (Address Error) signal generation including: alignment errors, width errors, transfer-not-understood errors, address portion bus errors, and continuation errors.
- Packaged in compact 300 mil 24 pin DIP or 28 pin J-lead LCC.
- Supports pipelined operations.
- Can be used separately or together with LBX 2000 to provide complete reply agent control interface to iLBX II bus.

Applications

- Bus Interface Circuitry for iLBX II reply agent modules such as I/O or memory devices.

Packages





LBX 2100 General Information

	Commercial (0°C to +70°C)
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic
High Drive Current Outputs (I_{OL})	To MBII spec (up to 64 mA, Open Collector or Three-state)

General Description

The LBX 2100 is a CMOS iLBX II reply agent address error generator packaged in a 300 mil 24 pin DIP or 28 pin J-lead LCC. The LBX 2100 provides complete reply agent address error generation and can drive the XAERR* signal directly (60 mA open collector). During specific cycles in a transaction the LBX 2100 will assert the XAERR* signal due to width errors, alignment errors, transfer-not-understood errors, address portion bus errors, and continuation errors. Other local errors can also be asserted to the LBX 2100 which will cause the XAERR* signal to be asserted.

The LBX 2100 conforms to the Rev C MULTIBUS II Bus Architecture Specification Handbook.

The LBX 2100 can also be used separately to generate the XAERR* signal for the reply agent module that does not use the LBX 2000 as the reply agent controller.

The LBX 2000 can be used in conjunction with the LBX 2100 where the 2100 is used to generate the XAERR* signal instead of the LBX 2000. In this manner, the two chip set provides a compact interface to the iLBX II bus.

Pin Descriptions

LBX 2100

Pin # LCC	Pin # DIP	Signal	I/O	Function
3	2	XRESET*	I	Active low; System bus reset.
4	3	XACCREQ*	I	Active low; Access request. Indicates valid address cycle on bus.
5	4	XBTCTRL*	I	Active low; Block transfer control. Indicates a block transfer cycle on bus.
6	5	XA0	I	Active high; Address bus bit 0.
7	6	XA01	I	Active high; Address bus bit 1.
9	7	XWAIT*	I	Active low; Wait state indicator.
10	8	XC3*	I	Active low; Command bit 3.
11	9	XC1*	I	Active low; Command bit 1.
12	10	XC0*	I	Active low; Command bit 0.
13	11	CLK	I	Inverted XBCLK*. Connect to pin 14 (DIP) or pin 17 (LCC).
14, 21, 24	12, 18, 20	VSS		Chip Ground
16	13	AMATCH*	O	Active low; Reply Agent match input. Indicates this module is being accessed.
17	14	CLK	I	Inverted XBCLK*. Connect to pin 11 (DIP) or pin 13 (LCC).
18	15	XAERR1*	O	Active low, 64 mA open collector; 0 WS address error output. Asserted if there is an address error during 0 WS accesses.
19	16	ACCDLY	O	Active high; Access delay. Indicates wait states during access.
20	17	LERROR*	O	Active low; Local errors. Used to indicates local address error (attempting to write to ROM).
23	19	BOUNDARY*	I	Active low; Address boundary exceeded. Indicates current transfer is over reply agent addressing limit for block transfers.
25	21	APERR*	O	Active low; Address parity error. Indicates parity error on address or command signals.
26	22	XAERR2*	O	Active low, 64 mA open collector; Non-0 WS address error output. Asserted if there is an address error during non-0 WS accesses.
27	23	XAERR3*	O	Active low, 64 mA open collector; Continuation error output. Asserted if there is a combination error during a block transfer.
2, 28	1, 24	VCC		+5V Chip Power
1, 8 15, 22	—	NC	—	No Connect

MCA 1200/1210 Micro Channel Controller and Local Arbiter

Distinctive Features

- Single chip device performs Micro Channel control and local arbitration
- Microprocessor independent
- Supports burst or single cycle data transfers
- Includes fairness arbitration option
- Handles PREEMPT* assertion error during arbitration cycles
- Drives Micro Channel signals to specifications: CMD*, ARB0-2, PREENPT* and BURST*
- Input hysteresis filters bus noise

Applications

- Bus masters for Micro Channel Architecture

General Description

The MCA 1200/1210 is a master bus controller, bus requester and local arbiter. The device functions as a Micro Channel adapter bus master.

The MCA 1200/1210 is a CMOS device housed in a 300 mil wide 24 pin DIP, or 28 pin LCC, and incorporates most of the logic, drivers and buffers required to control the bus. The bus controller, requester, and local arbiter protocols are asynchronous and meet the IBM Micro Channel Architecture timing and electrical specifications.

The MCA 1200/1210 performs bus request and local arbitration protocols. The device allows either single cycle or burst data transfer requests. The arbitration protocol features an optional fairness algorithm which prevents two consecutive bus accesses by the master. The bus control protocol controls the bus and aids the successful transfer of data.

MCA 1200: The MCA 1200 supports arbitration levels 12-15 (1100-1111 on ARB0-3).

MCA 1210: The MCA 1210 supports arbitration levels 8-11 (1000-1011 on ARB0-3).

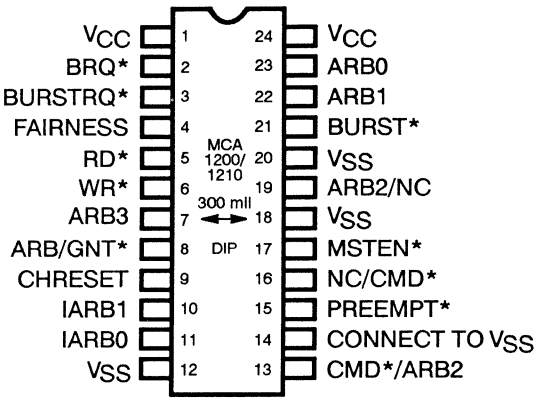
Note that the pinouts of the MCA 1200 and MCA 1210 are not identical.

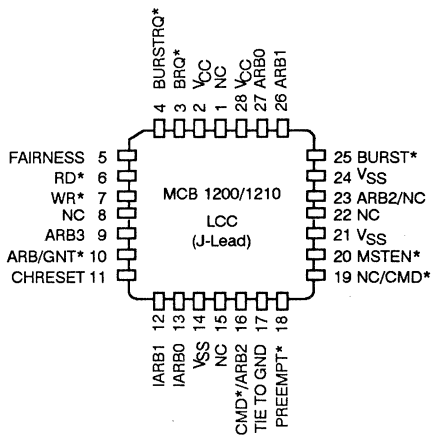
Pin Descriptions

MCA 1200/1210

28 Pin LCC	24 Pin DIP	Signal	Type	Function
2	1	V_{CC}	–	5 V supply.
3	2	BRQ*	I	Active low; Local bus request input to PREEMPT*.
4	3	BURSTRQ*	I	Active low; Local burst mode request input to BURST*.
5	4	FAIRNESS	I	Active high; Fairness alforithm enable input to arbiter.
6	5	RD*	I	Active low; Read command from 80X86 (UDS* from 680XX).
7	6	WR*	I	Active low; Write command from 80X86 (LDS* from 680XX).
9	7	ARB3	I	Micro Channel input; Active high; Arbitration priority level input.
10	8	ARB/GNT*	I	Micro Channel input; Indicates arbitration in process or bus is granted.
11	9	CHRESET	I	Micro Channel input; Active high; System reset.
12	10	IARB1	I	Active high; Selects arbitration level.
13	11	IARB0	I	Active high; Selects arbitration level.
14	12	V_{SS}	–	Chip Ground.
16	13	CMD*/ARB2	O/I/O	For MCA 1200, pin is "CMD*", Micro Channel Output, Active low indicates valid data cycle. For MCA 1210, pin is "ARB2", Micro Channel Input/Output, Active high, Arbitration priority level Input/Output.
17	14	V_{SS}	I	Tie Input to Ground.
18	15	PREEMPT*	I/O	Micro Channel Input/Output; Active low; Request control of bus to arbiter.
19	16	NC/CMD*	–/O	For MCA 1200 pin is "No Connect". For MCA 1210 pin is "CMD*", Micro Channel Output, Active low, indicates valid data cycle.
20	17	MSTEN*	O	Active low; Master enable output, master controls bus and enables buffers.
21	18	V_{SS}	–	Chip Ground.
23	19	ARB2/NC	I/–	For MCA 1200 pin is "ARB2", Micro Channel Input, Active high, Arbitration priority level input. For MCA 1210 pin is "No Connect".
24	20	V_{SS}	–	Chip Ground.
25	21	BURST*	O	Micro Channel Output; Active low; Indicates burst or block data transfer.
26	22	ARB1	I/O	Micro Channel Input/Output; Active high; Arbitration priority level.
27	23	ARB0	I/O	Micro Channel Input/Output; Active high; Arbitration priority level.
28	24	V_{CC}	–	5 V supply.
1, 8, 15, 22	–	NC	–	No Connect.

Packages





MCA 1200/1210 General Information

	Commercial (0°C to +70°C)
Package Type	24 pin 300 mil DIP 28 pin J-Lead LCC
Package Material	Plastic Ceramic
High Drive Current Outputs (I_{OL})	To Micro Channel spec (24 mA, Open Collector or Three-state)

Programmable Devices

Because each bus interface application has unique requirements, interface designs vary from board to board. With PLX programmable ICs, the design task is fast and simple. Create your own compact custom bus interface or modify the standard solutions PLX provides to meet your system's special needs.

PLX devices replace several components due to their high level of integration. Integrated high current drivers, Schmitt triggers, metastable hardened registers, multiple ground pins, two separate clock inputs and the dense programmable logic array ensure high performance and reliability.

Choose from two programmable devices:

- **PLX 464 with 64 mA and 48 mA drivers**
- **PLX 448 with 48 mA and 24 mA drivers**

Distinctive Features

- Integrated 48 mA and 64 mA or 24 mA and 48 mA drivers, meet drive requirements for VME, VSB, MBI, MBII, Micro Channel, NuBus and other leading bus specification signals
- 64 mA or 48 mA Quad-state drivers are individually programmable to open collector or three-state configurations
- Dynamic bi-directional I/O capability. Additional input path monitors bus level when output is high impedance
- Metastable hardened registers allow implementation of asynchronous arbiters and synchronizers
- Buried register and buried combinatorial feedback capability
- Low power UV erasable/reprogrammable CMOS, 80 mA max I_{CC}
- Two independent clock inputs
- Input hysteresis allows device to monitor input signals directly from the bus
- 3 ground pins for noise immunity and minimal ground bounce
- Hot insertion capable, latchup-free design

Applications

- Bus control logic including:
  - Intelligent Transceivers
  - Bus Controllers
  - Interrupt Handlers
  - Interrupt Requesters
  - Bus Arbiters
  - Slave Module Selectors
- Other logic applications where high drive currents and high logic integration are required

General Description

The PLX 464 and the PLX 448 are CMOS programmable logic devices designed to implement a broad range of bus protocol functions. The devices include a programmable logic array plus many common elements of bus interface circuitry, including four 64 mA or 48 mA Quad-state drivers, four 48 mA or 24 mA three state drivers, metastable hardened registers and inputs with hysteresis. In addition, to implement common bus logic structures, the device includes dynamic bi-directional I/Os, extra input paths to monitor bus levels, buried register capability to build state machines without wasting I/O pins, and two clock inputs for arbitration of asynchronous inputs.

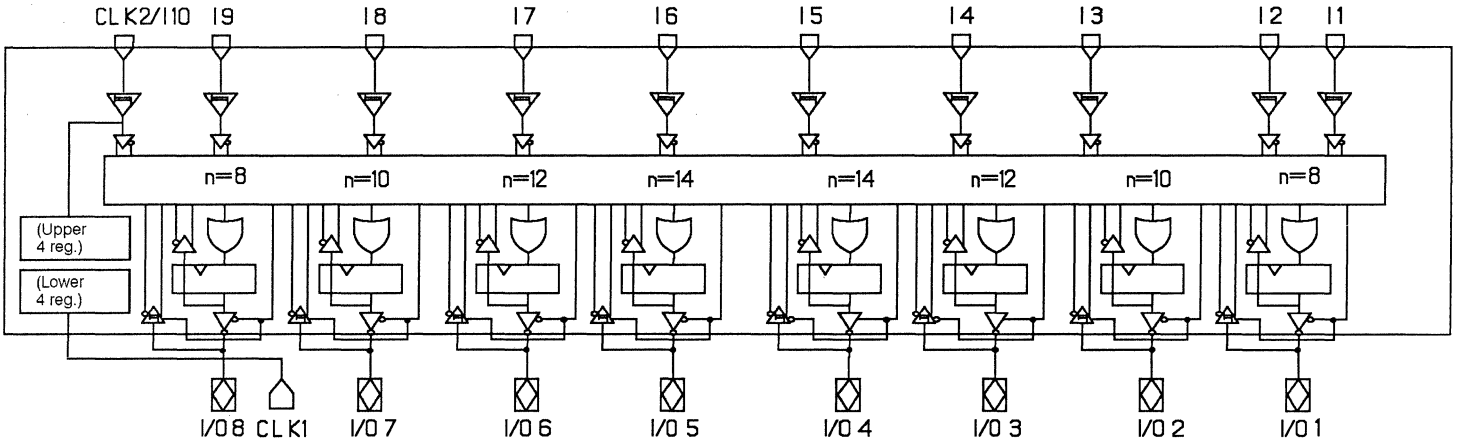
Programming Support

PLX programmable ICs are supported by industry standard development tools including ABEL and CUPL. A wide range of programmers will program PLX devices. See the list below for current suppliers

Manufacturer (Software)	Product
Data I/O, Redmond, WA	ABEL (version 3.0 or later)
Logical Devices, Fort Lauderdale, FL	CUPL (version 2.0 or later)
PistoHI Tools, Cupertino, CA	PET100
—Others are in development; contact PLX for an update.	

Manufacturer (Programmers)	Model No.
Advin Systems, Sunnyvale, CA	Sailor-PAL
Data I/O, Redmond, WA	29B
Data I/O	Unisite 40
InLab, Broomfield, CO	28 A/U
Logical Devices, Fort Lauderdale, FL	Allpro
PistoHI Tools, Cupertino, CA	PET100
Stag Microsystems, Santa Clara, CA	All Models
—Others in Development; contact PLX for an update.	

PLX448/464 Logic Diagram



(PLX464)	**64mA**	**64mA**	48mA	48mA	48mA	48mA	**64mA**	**64mA**
(PLX448)	**48mA**	**48mA**	24mA	24mA	24mA	24mA	**48mA**	**48mA**

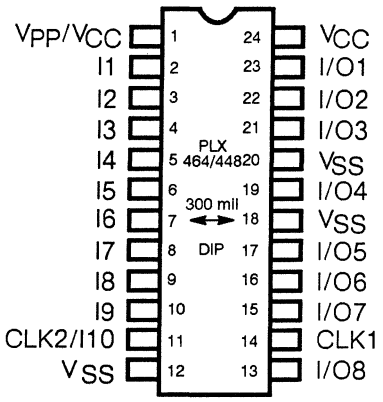
n = number of product terms.

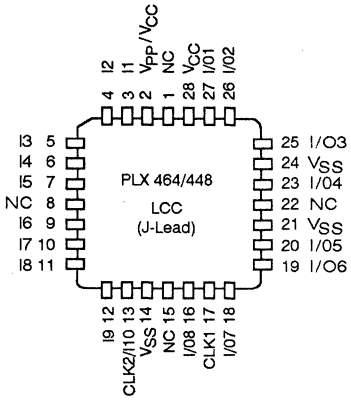
Pin Descriptions

PLX 464 and PLX 448

Pin No.		Description
LCC	**DIP**	
28	24	V_{CC}
3-7, 9-12	2-10	Dedicated Inputs
13	11	Dedicated Input and/or Clock Input registers 4-8 (CLK2)
17	14	Clock Input to registers 1-4 (CLK1)
2	1	V_{PP}/V_{CC}
14, 21, 24	12, 18, 20	V_{SS} (Ground)
16, 18, 19 20, 23, 25 26, 27	13, 15, 16 17, 19, 21 22, 23	Bidirectional Input/Output pins
1, 8, 15		No Connect

Packages





PLX 464 and PLX 448 General Information

		Commercial 0°C to +70°C	Industrial -40°C to +85°C	Military -55°C to +125°C
Package Type		24 pin 300 mil DIP	24 pin 300 mil DIP	24 pin 300 mil DIP
		28 pin J-Lead LCC	28 pin J-Lead LCC	28 pin J-Lead LCC
Package Material		Plastic Ceramic	Ceramic	Ceramic
Speed		tPD max = 45ns, 35ns* tCO max = 30 ns, 20ns*	tPD max = 55ns, 45ns* tCO max = 35ns, 25ns*	tPD max = 65ns, 55ns* tCO max = 40ns, 30ns*
High Drive Current Outputs (I_{OL})	PLX 464	4 at 64 mA, 4 at 48 mA	4 at 64 mA, 4 at 48 mA	4 at 64 mA, 4 at 48 mA
	PLX 448	4 at 48 mA, 4 at 24 mA	4 at 48 mA, 4 at 24 mA	4 at 48 mA, 4 at 24 mA

*Contact PLX for availability

For experienced help with your interface designs, call or FAX PLX. With a copy of your schematic or a block diagram, PLX can save you time and effort, no matter what the application.

TELEPHONE: 1-800-759-3753
FAX: 1-415-960-0479

WE WANT TO DESERVE YOUR BUSINESS

PLX Technology, Inc., 625 Clyde Avenue, Mountain View, CA 94043
FAX (415) 960-0479 PHONE (415) 960-0448, (800) 759-3753