BU29504KV
Serial ATA Bridge Chip
Description of Functions
Ver. 0.97

2007/Sep

Table of Contents

Page No.

Instructions for Use

- Although we believe that the examples of application circuit shown in this instruction should be recommended, please further make sure of characteristics of the product in prior to use.
- When using the product with changed external circuit constant, please allow for sufficient margin, considering its static/transient characteristics, external parts and variability of our IC's.
- Please understand that we have not confirmed the patent right enough.

- This product is designated for use in general electronic devices.
  Therefore, please contact our sales liaison in advance of using it in such devices or equipments as to require extremely high reliability and also to threaten human life directly by their failure or malfunction.
- Although we believe that the application circuits, etc. shown in this specification are accurate and reliable as for eliciting the characteristics of the product, we are not responsible for any problem concerning circuits or industrial right caused by using the product.
- This product is not designated for radiation resistance.

1 General

BU29504 (hereinafter called 'this LSI') is the Serial ATA to Parallel ATA Bridge LSI, in which the Physical layer, Link layer, Transport layer, Application layer of Serial ATA, and the Parallel ATA interface are all integrated in one chip. By adapting a complete hard wired structure without a operational processor mounted, we have actualized high processing capacity and low power consumption.

As the Serial ATA interface used in this LSI complies with the Serial ATA Standard, and the Application layer corresponds to the ATA/PACKET commands, it is possible to establish a storage system consisting of HDD, CD or DVD, etc.

Since this LSI has a bridge function for both modes of the Host/Device (ref. Figure 1-1), it is possible to connect the old Parallel ATA device to the latest Serial ATA Host Bus adaptor, or connect the latest Serial ATA device to the old Parallel ATA Host Bus adapter.

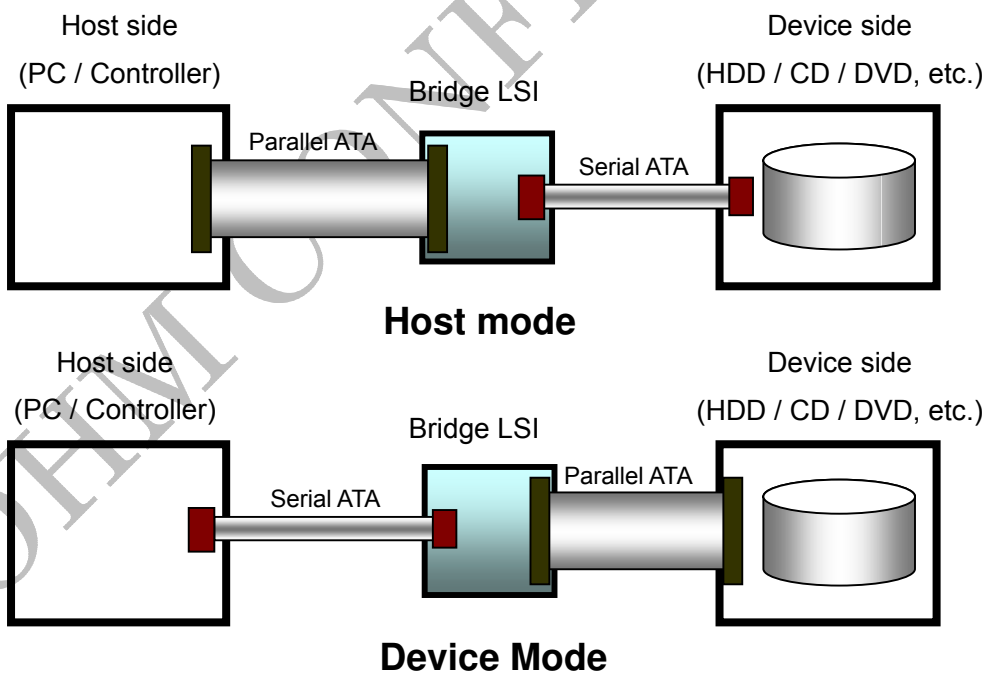


Figure 1-1 Connection Mode Chart

2 Features

2.1 List of Functions

Table 2-1 List of Functions

	BU29504KV
Serial ATA Revision (Usage Model)	Revision 1.0a (Gen1:1.5Gbps)
ATA/ATAPI PIO MODE	0/1/2/3/4
ATA/ATAPI MDMA MODE	0/1/2
ATA/ATAPI UDMA MODE	0/1/2/3/4/5/6
CMOS process	0.18μm
Input Voltage	1.8/3.3V
Outside XTAL	25MHz
Package	VQFP64
HBM/MM	±4000V/±400V
Port Multiplier	○
SSC(spread spectrum clock)	○ (※1)
PACKET Command feature set	○
48-bit Address feature set	○
Serial ATA power saving modes	○
Serial ATA BIST operation	○
Serial ATA hot-plug	○

(※1)Refer to the description related to SSC in clause 2.2.

2.2 Functional Precautions

- There will be a connection problem with Marvell 88i8030-B2P when SSC is switched ON (no problem will occur with any models after B4P).
- When resetting from the Partial/Slumber modes, Scramble will be stopped until receiving a command.
- Different sequence of power-on procedures for each supply voltage (VCCO, VCCK, AVDDH, and AVDDL) will not cause any breakdown or malfunction of LSI. This applies also to the power-off procedures.
- When using the product in the Host mode and also in Slave type, as DASP will be released when receiving the first FIS, there would be a connection problem with the Master which samples DASP after the first FIS is received (ref. Figure 2-1).
- When operating the product in the Device mode, receiving the DMAT Primitive (DMA Terminate) from the Host is not supported. Do not output a DMAT Primitive signal from the Host side to be connected when operating in the Device mode.
- In the Transfer mode higher than UDMA4, the actual throughput will not reach the standard of transfer rate (approximately 45MB/s in the Transfer mode of UDMA4).
- Receiving a command = A0h (PACKET Command) with HDD connected to the product in the Device mode will cause a freeze. It can be reset by Software Reset.
- When SSC is turned on, it is confirmed that there is a connectivity problem between devices made of old Marvell(88i8030-B2P).
- When SSC is turned on, a primitive error might occur according to the device because a permissible margin in connected, compatibility is not enough.

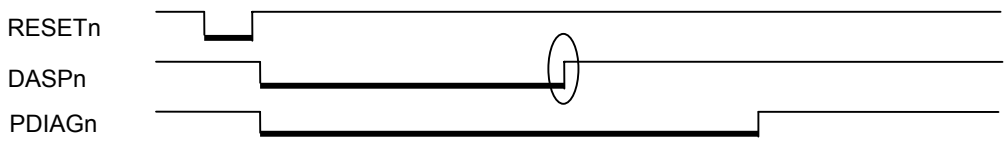


Figure 2-1

3 Block Diagram

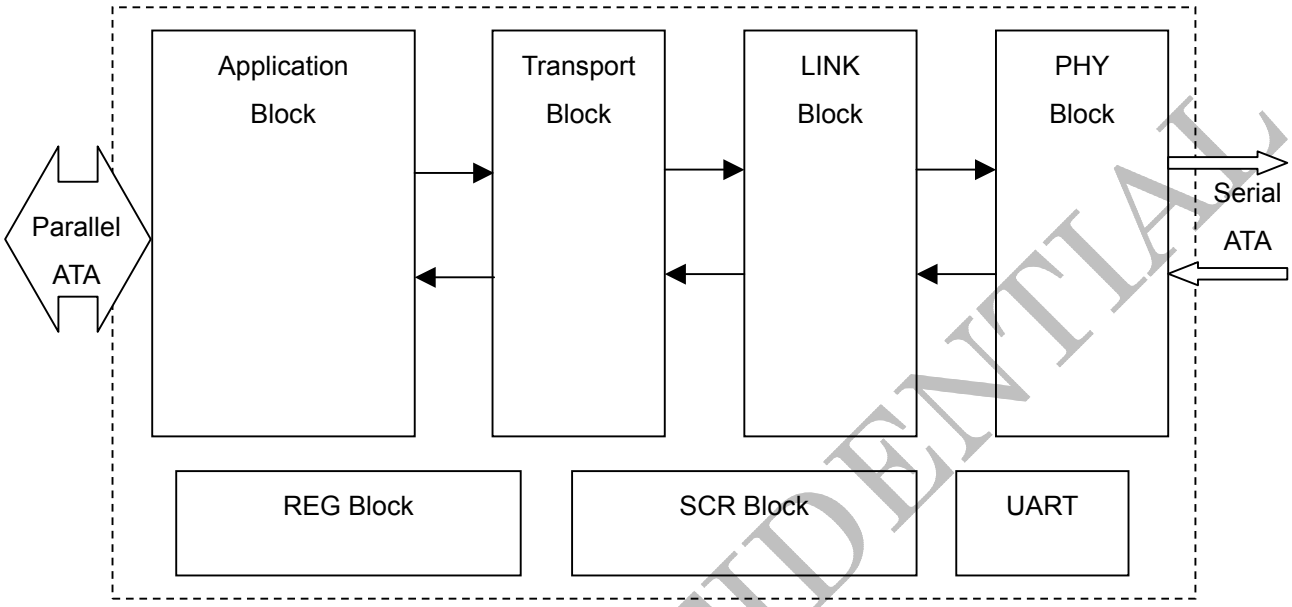


Figure 3-1 BU29504 Block Diagram

3.1 PHY Block

PHY block initializes the Serial ATA Bus with an Out Of Band (OOB) signal such as COMRESET or COMINIT/COMWAKE, etc.

When a data transfer request is received from the LINK block, arbitration is executed, the data is serialized and transferred via cable.

If data is received via cable, it is parallelized and transferred to the LINK block.

3.2 LINK Block

If the LINK block receives a data transfer request from the Transport block, it encodes the data, appends CRC data, randomizes it and issues a transfer request to PHY.

When data is received from the PHY block, randomized data is released, decoded and transferred to the Transport block if there is no error in CRC.

3.3 Transport Block

If the Transport block receives a data transferring request from the Application block, it packetizes the data and issues a data transferring request to the LINK block.

As for Serial ATA, this packet is called 'Frame Information Structure (FIS).'

When receiving data (FIS) from the LINK block, it is transferred to the Application block if there is no error in the data.

3.4 Application Block

When the Application block receives data or command transferring request from the Parallel ATA interface, it issues a data transferring request to the Transport block.

When receiving data from the Transport block, it determines a data command and transfers the data to the Parallel ATA interface in an appropriate format for the content of the data.

3.5 SCR Block

SCR (Status and Control Registers) block is defined in the Serial ATA specification in order to obtain detailed data about the Serial ATA.

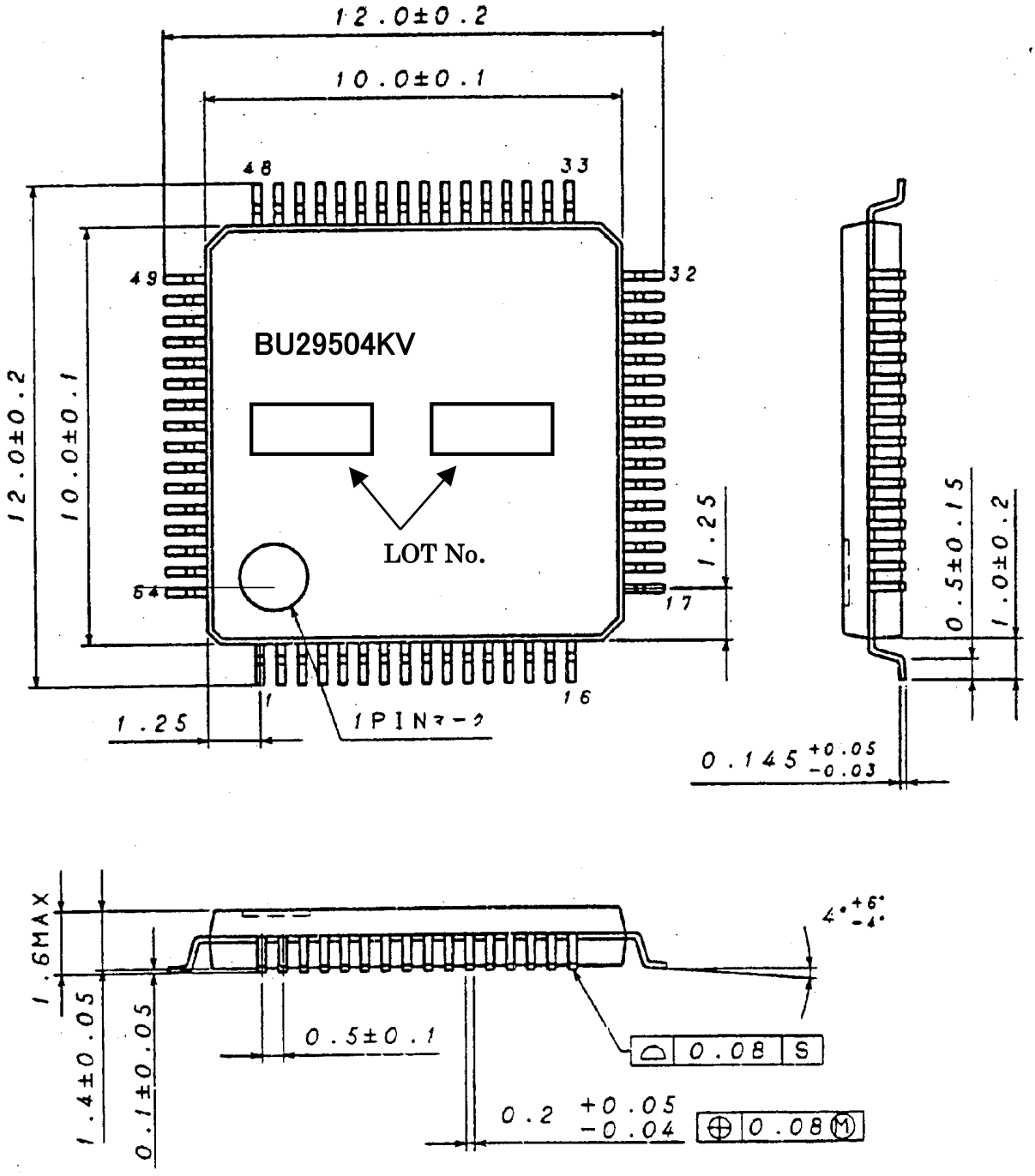
This LSI supports vendor commands to access to the group of registers from the Parallel ATA Bus and UART when operating in the Host mode (20 pin: MODE2 = 1).

3.6 REG Block

This LSI supports not only SCR but also the collection of registers to obtain or control the data inside the LSI.

REG block is writable and readable by vendor commands, just like SCR.

4 Outside Dimensions



(UNIT:mm)

5 Description of Pin

5.1 Pin Assign

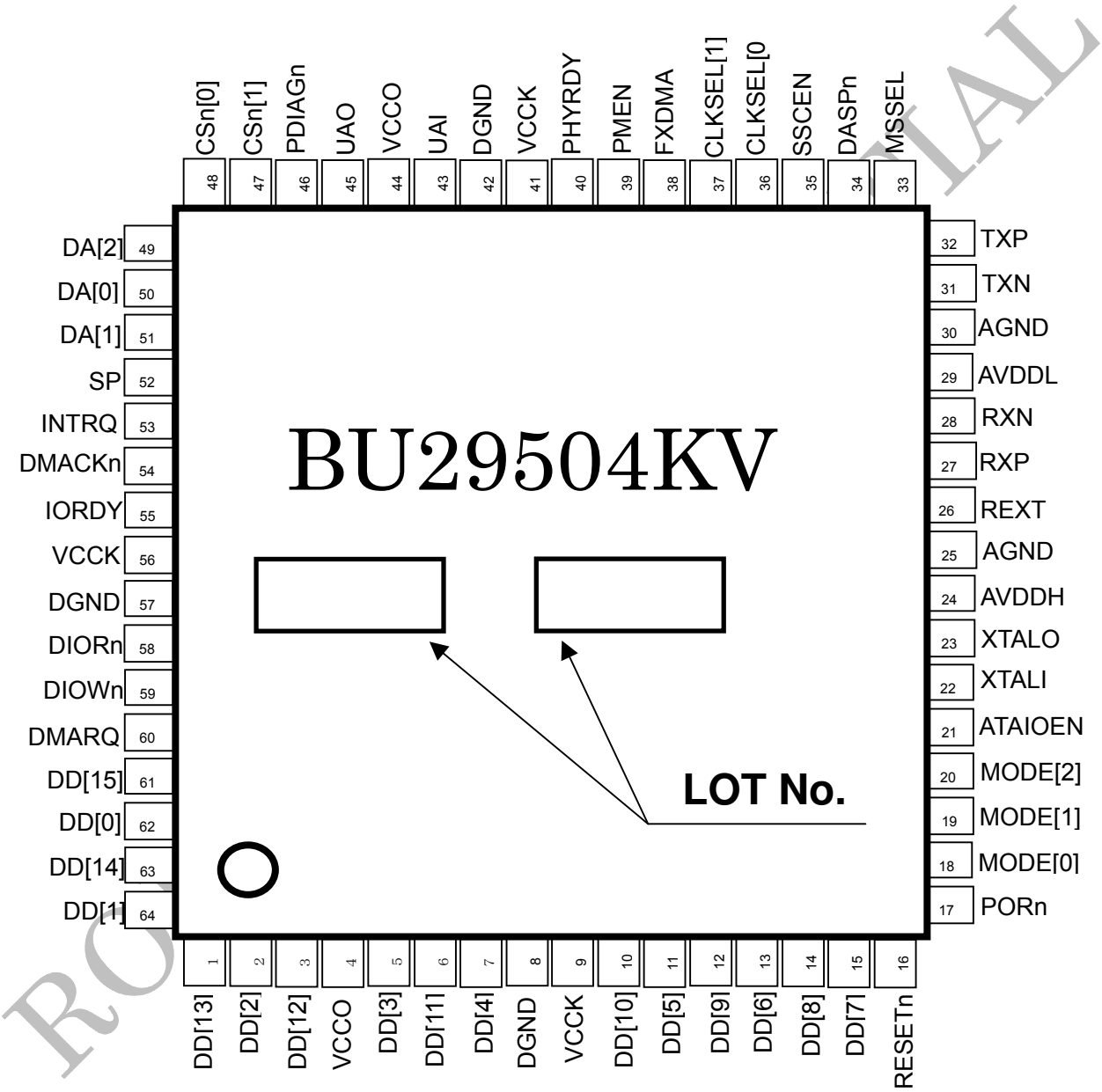


Figure 5-1 Pin Positions

5.2 Table of Pin Assign (Normal / Reverse)

It is possible to switch the input/output pins for BU29504 (ref. Table 5-1), which is valid only for the Device mode setting and controlled by PDIAGn pin.

PDIAGn = 0 : Normal Order

PDIAGn = 1 : Reverse Order

Table 5-1 Table of Pin Positions

Pin	Normal Order	Reverse Order	Pin	Normal Order	Reverse Order
1	DD[13]	DD[0]	48	CSn[0]	DD[7]
2	DD[2]	DD[15]	49	DA[2]	DD[8]
3	DD[12]	DMARQ	50	DA[0]	DD[6]
5	DD[3]	DIOWn	51	DA[1]	DD[9]
6	DD[11]	DIORn	52	SP	DD[5]
7	DD[4]	DMACKn	53	INTRQ	DD[10]
10	DD[10]	INTRQ	54	DMACKn	DD[4]
11	DD[5]	SP	55	IORDY	IORDY
12	DD[9]	DA[1]	58	DIORn	DD[11]
13	DD[6]	DA[0]	59	DIOWn	DD[3]
14	DD[8]	DA[2]	60	DMARQ	DD[12]
15	DD[7]	CSn[0]	61	DD[15]	DD[2]
16	RESETn	CSn[1]	62	DD[0]	DD[13]
34	DASPn	DASPn	63	DD[14]	DD[1]
46	PDIAGn	PDIAGn	64	DD[1]	DD[14]
47	CSn[1]	RESETn			

5.3 Description of Pin Functions

Table 5-2 Definition of Pin Types

Pin Type	Remarks
I	Input pin
O	Output pin
I/O	Bi-directional I/O pin
H	With pull-up resistor (typical 40 KΩ)
L	With pull-down resistor (typical 61 KΩ)
D	Digital pin
A	Analog pin

Table 5-3 Serial ATA Interface

Name of Signal	Pin No.	Type	Function
XTALI	22	AI	Crystal Oscillation Circuit Input: 25MHz crystal oscillator shall be connected externally.
XTALO	23	AO	Crystal Oscillation Circuit Output
REXT	26	AI	External Reference Resistor Connection Input: As the reference, a resistor with 11.3/10KΩ should be connected to ground. The accuracy of resistor must be within ±1% (ref. Figure 8-1).
RXP	27	AI	Serial Data Receiver: Differential input signal: 1.5Gbps Only AC connection shall be supported.
RXN	28	AI	Serial Data Receiver: Differential input signal: 1.5Gbps Only AC connection shall be supported.
TXP	32	AO	Serial Data Transmitter: Differential output signal: 1.5Gbps Only AC connection shall be supported.
TXN	31	AO	Serial Data Transmitter: Differential output signal: 1.5Gbps Only AC connection shall be supported.

Table 5-4 Parallel ATA Interface

Name of Signal	Pin No.	Type	Function
DD[15:0]	1, 2, 3, 5, 6, 7, 10, 11, 12, 13, 14, 15, 61, 62, 63, 64	DI/O DI/O DI/OL DI/O DI/O DI/O DI/O DI/OL DI/O DI/O DI/O DI/O DI/O DI/O DI/O DI/O 8mA	ATA/ATAPI Data Bus: ATA/ATAPI Bi-directional Data Bus.
CSn[1:0]	47 48	DI/O DI/O 8mA	ATA/ATAPI Chip Select: [Host mode: In, Device mode: Out] Chip select signal for the device register access.
DA[2:0]	49 50 51	DI/O DI/O DI/O 8mA	ATA/ATAPI Data Address: [Host mode: In, Device mode: Out] Address signal for data access.
DIORn/ HDMARDYn/ HSTROBE	58	DI/O 8mA	IO Read / UDMA Ready / UDMA Data Strobe: [Host mode: In, Device mode: Out] - At UDMA transfer: Functions as HDMARDYn (at reading) / HSTROBE (at writing) signal. Notification signal for 'Ready to Receive Data' when reading. Strobe signal for data latch timing when writing. - Other than UDMA transfer: Functions as DIORn. (Register data reading signal)
DIOWn/ STOP	59	DI/O 8mA	IO Write / UDMA Stop: [Host mode: In, Device mode: Out] - At UDMA transfer: Functions as a STOP signal. (Data transfer stop requesting signal) - Other than UDMA transfer: Functions as DIOWn. (Register data writing signal)
DMACKn	54	DI/O 8mA	DMA Acknowledge: [Host mode: In, Device mode: Out] Used at DMA transfer. Answering signal for data transfer start which the Host responds to the DMARQ signal (60 pin) from the device side.
DMARQ	60	DI/OL 8mA	DMA Request: [Host mode: Out, Device mode: In] Used at DMA transfer. Data transfer start requesting signal from the Device side to Host side.
INTRQ	53	DI/O 8mA	Device Interrupt: [Host mode: Out, Device mode: In] Interruption requesting signal from the device side.

Name of Signal	Pin No.	Type	Function
IORDY/ DDMARDYn/ DSTROBE	55	DI/O 8mA	IORDY / DDMARDY / DSTROBE: [Host mode: Out, Device mode: In] - At UDMA transfer: Functions as DDMARDYn (at writing)/DSTROBE (at reading) signal. Notification signal for 'Ready to Receive Data' when writing. Strobe signal for data latch timing when reading. - Other then UDMA transfer: Functions as IORDY signal. Wait requesting signal from the Device side.
PDIAGn	46	DI/OH 8mA	Pass Diagnostics / Parallel ATA Bus Order Reverse: - In the Host mode: Functions as PDIAGn signal. Notification signal for the results of the self-diagnostic from Slave to Master. - In the Device mode [Only valid for BU29504]: Bus switching signal for the Parallel ATA (ref. Table 5-1). 0: ATA interface (in the Normal Order mode) 1: ATA interface (in the Reverse Order mode) **CBLID** - No functionality
RESETn	16	DI/O 8mA	Hardware Reset: [Host mode: In, Device mode: Out] Resetting signal from the Host to Device side (Active Low).
DASPn	34	DI/OH 8mA	Slave Present / Device Active [In the Host mode only] - At operating a reset protocol: Functions as DASPn signal. (Present signal from the Slave to Master) [Active Low / Master: In, Slave: Out] (Also refer to the MSSEL Signal Pin.) - After operating the reset protocol: Signal for Device Active indicator.
SP	52	DI/OL 4mA	Slave Present [In the Host mode only] Present signal from the Slave to Master. Same functions as DASPn (34 pin). However, it operates as a present signal, except for the Reset protocol.. Mainly used when hot swapping is functioning. [Active Hi (PHYRDY output) / Master: In, Slave: Out] (Also refer to the MSSEL Signal Pin.)

Table 5-5 Operation Control Interface

Name of Signal	Pin No.	Type	Function
PORn	17	DIH	Power On Reset: Chip resetting signal (Active Low).
SSCEN	35	DIL 4mA	Spread Spectrum Clock Enable: Control signal for spread spectrum clock function. 0: Invalidate the spread spectrum clock function (default). 1: validate the spread spectrum clock function.
CLKSEL[1:0]	36, 37	DIH DIL 4mA	Reference Clock Selection: Frequency setting for crystal oscillator. 01: 25MHz external crystal oscillator (default). Others: Reserved.
PHYRDY	40	DOL 4mA	Physical Layer Ready: Communication establishment signal after completion of an initialization for the Serial ATA PHY layer. 0: Right after POR or when initialization failed for the Physical layer. 1: Initialization for the PHY layer has completed.
FXDMA	38	DIL 4mA	Fixed UDMA Data Rate: (for TEST) Forced setting of the transfer rate. 0: Settable by Set Feature command (default). 1: Fixed setting of the data transfer rate by MODE [1:0] (18,19 pin).
MODE[2]	20	DIL 4mA	Mode Selection: Selection of the Host mode / Device mode. 0: Device mode (default) 1: Host mode
MODE[1:0]	18, 19	DIL DIH 4mA	Mode Selection: (for TEST) For fixing a data transfer rate, also need to set FXDMA (38 pin). 00: 100MB/s 01: 133MB/s 10: 150MB/s (default) 11: Reserved (LSI test mode)
MSSEL	33	DI/OL 4mA	Master Slave Selection: [Host mode: In, Device mode: Out] - In the Host mode: 0: Master (default) 1: Slave (reserved) - In the Device mode: Data bit 4 of the Parallel ATA control register is output.
ATAIOEN	21	DIH 4mA	ATA IO Interface Enable: Forced setting of the Hi impedance output for ATA IO Pin. 0: Valid (Hi impedance mode) 1: Invalid (default)
PMEN	39	DIH 4mA	Power Management Command Enable: Power saving mode setting for the Serial ATA by ATA Power Management Feature Setting command. 0: Invalid 1: Valid (default)
UAI	43	DIH 4mA	On-Chip UART Input:

Name of Signal	Pin No.	Type	Function
UAO	45	DOH 4mA	On-Chip UART Output:

Table 5-6 Power Supply / Ground

Name of Signal	Pin No.	Type	Function
AVDDH	24	AI	3.3V Analog Power Supply:
AVDDL	29	AI	1.8V / 1.2V (ref. Table 2-1) Analog power supply:
AGND	25, 30	AI	Analog GND:
VCCO	4, 44	DI	3.3V I/O Power Supply:
VCCK	9, 41, 56	DI	1.8V / 1.2V (ref. Table 2-1) Core power supply:
DGND	8, 42, 57	DI	Digital GND:

6 ATA / ATAPI Commands

6.1 Command List

Table 6-1 PIO Data-In Commands

Command	Code
CFA TRANSLATE SECTOR	87h
DEVICE CONFIGURATION IDENTIFY	B1h (C2h)
IDENTIFY DEVICE	ECh
IDENTIFY COMPONENT	D0h
IDENTIFY PACKET DEVICE	A1h
READ BUFFER	E4h
READ LOG EXT	2Fh
READ MULTIPLE	C4h
READ MULTIPLE EXT	29h
READ SECTOR(S)	20h/21h
READ SECTOR(S) EXT	24h
READ LONG	22h/23h
SMART READ DATA	B0h (D0h)
SMART READ ATTRIBUTE THRESHOLDS	B0h (D1h)
SMART READ LOG	B0h (D5h)

Table 6-2 PIO Data-Out Commands

Command	Code
CFA WRITE MULTIPLE WITHOUT ERASE	CDh
CFA WRITE SECTORS WITHOUT ERASE	38h
DEVICE CONFIGURATION SET	B1h (C3h)
DOWNLOAD MICROCODE	92h
SECURITY DISABLE PASSWORD	F6h
SECURITY ERASE UNIT	F4h
SECURITY SET PASSWORD	F1h
SECURITY UNLOCK	F2h
SET MAX PASSWORD	F9h (01h)
SET MAX UNLOCK	F9h (03h)
SMART WRITE LOG	B0h (D6h)
SMART WRITE ATTRIBUTE THRESHOLDS	B0h (D7h)
WRITE BUFFER	E8h
WRITE LOG EXT	3Fh
WRITE MULTIPLE	C5h
WRITE MULTIPLE EXT	39h
WRITE SECTOR(S)	30h/31h
WRITE SECTOR(S) EXT	34h
WRITE LONG	32h/33h
WRITE VERIFY SECTOR(S)	3Ch

Table 6-3 DMA Data-In Commands

Command	Code
READ DMA	C8h/C9h
IDENTIFY DEVICE DMA	EEh
READ DMA EXT	25h

Table 6-4 DMA Data-Out Commands

Command	Code
WRITE DMA	CAh/CBh
WRITE DMA EXT	35h

Table 6-5 Commands for Host Mode Only

Command	Code
READ DMA QUEUED	C7h
READ DMA QUEUED EXT	26h
WRITE DMA QUEUED	CCh
WRITE DMA QUEUED EXT	36h
SERVICE	A2h

Table 6-6 PACKET/DIAG Commands

Command	Code
PACKET	A0h
DEVICE RESET	08h
EXECUTE DEVICE DIAGNOSTIC	90h

Table 6-7 Non-Data Commands

Command	Code
CHECK MEDIA CARD TYPE	D1h
CHECK POWER MODE	E5h/98h
DEVICE CONFIGURATION FREEZE LOCK	B1h (C1h)
DEVICE CONFIGURATION RESTORE	B1h (C0h)
FLUSH CACHE	E7h
FLUSH CACHE EXT	EAh
FORMAT TRACK	50h
GET MEDIA MODE	DAh
IDLE	E3h/97h
IDLE IMMEDIATE	E1h/95h
INITIALIZE DEVICE PARAMETERS	91h
MEDIA EJECT	EDh
MEDIA LOCK	DEh
MEDIA UNLOCK	DFh
NOP	00h
RECALIBRATE	1xh
READ NATIVE MAX ADDRESS	F8h
READ NATIVE MAX ADDRESS EXT	27h
READ VERIFY SECTOR(S)	40h/41h
READ VERIFY SECTOR(S) EXT	42h
SECURITY ERASE PREPARE	F3h
SECURITY FREEZE LOCK	F5h
SEEK	70h
SET FEATURES	EFh
SET MAX ADDRESS	F9h
SET MAX LOCK	F9h (02h)
SET MAX FREEZELOCK	F9h (04h)
SET MAX ADDRESS EXT	37h
SET MULTIPLE MODE	C6h
SLEEP	E6h/99h
SMART DISABLE OPERATIONS	B0h (D9h)

Command	Code
SMART ENABLE OPERATIONS	B0h (D8h)
SMART ENABLE/DISABLE AUTOSAVE	B0h (D2h)
SMART SAVE ATTRIBUTE VALUES	B0h (D3h)
SMART EXECUTE OFF_LINE IMMEDIATE	B0h (D4h)
SMART RETURN MODE	B0h (DAh)
SMART ENABLE/DISABLE AUTO OFFLINE	B0h (DBh)
STANDBY	E2h/96h
STANDBY IMMEDIATE	E0h/94h

Table 6-8 PACKET Commands

Command	Code
FORMAT UNIT	04h
MODE SELECT(6)	15h
MODE SELECT(10)	55h
MEDIUM SCAN	38h
SEND CUE SHEET	5Dh
SEND DVD STRUCTURE	BFh
SEND DIAGNOSTIC	1Dh
SEND EVENT	A2h
SEND KEY	A3h
SEND OPC INFORMATION	54h
WRITE	0Ah
WRITE(10)	2Ah
WRITE(12)	AAh
WRITE AND VERIFY(10)	2Eh
WRITE AND VERIFY(12)	AEh
WRITE BUFFER COMMAND	3Bh
BLANK	A1h
CLOSE TRACK/RZONE/SESSION/BORDER	5Bh
ERASE	19h
GET CONFIGURATION	46h
GET EVENT/MODE NOTIFICATION	4Ah
GET PERFORMANCE	ACh
INQUIRY	12h
LOAD/UNLOAD MEDIUM	A6h
MECHANISM MODE	BDh
MODE SENSE(6)	1Ah
MODE SENSE(10)	5Ah
PAUSE/RESUME	4Bh
PLAY AUDIO(10)	45h
PLAY AUDIO(12)	A5h
PLAY AUDIO MSF	47h
PLAY CD	BCh

Command	Code
PREVENT/ALLOW MEDIUM REMOVAL	1Eh
READ(6)	08h
READ(10)	28h
READ(12)	A8h
READ BLOCK LIMITS	05h
READ CAPACITY COMMAND	25h
READ CD	BEh
READ CD MSF	B9h
READ DISC INFORMATION	51h
READ DVD STRUCTURE	ADh
READ FORMAT CAPACITIES	23h
READ HEADER	44h
READ MASTER CUE	59h
READ POSITION	34h
READ REVERSE	0Fh
READ SUBCHANNEL	42h
READ TOC/PMA/ATIP	43h
READ TRACK/RZONE INFORMATION	52h
RECEIVE DIAGNOSTICS	1Ch
RECOVER BUFFERED DATA	14h
RELEASE	17h
REPAIR RZONE	58h
REPORT DENSITY SUPPORT	44h
REPORT KEY	A4h
RESERVE	16h
REQUEST SENSE	03h
RESERVE TRACK/RZONE	53h
REWIND	01h
SCAN	BAh
SEEK	2Bh
SET CD SPEED	BBh
SET READ AHEAD	A7h
SPACE	11h
START/STOP UNIT	1Bh

Command	Code
STOP PLAY/SCAN	4Eh
SYNCHRONIZE CACHE	35h
TEST UNIT READY	00h
VERIFY	13h
VERIFY(10)	2Fh
VERIFY(12)	AFh
READ BUFFER COMMAND	3Ch
READ BUFFER CAPACITY COMMAND	5Ch
WRITE FILEMARKS	10h

6.2 Vendor Commands

In the specification of Serial ATA, SCR (Status and Control registers) is defined to be mounted inside the host adaptor. Application can obtain detailed internal data of this LSI by accessing to this register.

However, as an accessing method to the SCR via Parallel ATA Bus is not defined in the specification, the following vendor commands have been added. Using these vendor commands, it is also possible to perform a test control such as for BIST.

Access to the SCR is supported only when operating the product in the Host mode.

Table 6-9 ROHM Special Function Register Configurations

Register	7	6	5	4	3	2	1	0
Features	FCh							
Sector count	N.A		PKT	SCR	SCR address			
LBA Low	4Ah							
LBA Mid	4Dh							
LBA High	43h							
Device	N.A			DEV	N.A			
Command	FCh							

SCR address: SCR address field

SCR: SCR access mode (when being set in 1)

PKT: Data receivable in the DMA mode (when being set in 1)

In the specification ‘AT Attachment with PACKET Interface,’ it is defined that ‘FA’h~’FF’h can be used as vendor commands. According to this specification, the LSI uses ’FC’h as a vendor command. This address is a fixed value.

During execution of this vendor command, ‘Register – Host to Device’ FIS is not transferred to the device.

6.2.1 SCR Access

When the SCR bit is set in 1, it is possible to access to the SCR.
Please perform an execution according to the procedures below:

1. Device numbers to be accessed should be set in the device register.
2. ‘FC’h shall be set in the features register.
3. SRC=1 and an address to be accessed should be set in the sector count register.
4. ‘4A’h shall be set in LBA Low.
5. ‘4D’h shall be set in LBA Mid.
6. ‘43’h shall be set in LBA High.
7. ‘FC’h should be set in the command register.
8. This LSI shall be switched to the SCR access mode.
9. Low 16 bit data should be transferred by the first data port access.
10. Low 16 bit data should be transferred by the next data port access.
11. SCR access mode will be unlocked by changing any value of the feature register or LBA Low/Mid/High register.
12. Transfer of the data port (in the order of lower to upper) is repeated until the SCR access mode is unlocked.

6.2.2 Register map

Table 6-10 Register Map Address for Special Function

Address	Name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00h	**SStatus**	Reserved (0)																				IPM				SPD				DET			
01h	**SError**	DIAG																								ERR							
02h	**SControl**	Reserved (0)																				IPM				SPD				DET			
03h	**BIST_CTL**	Reserved (0)															T	0	S	L	Reserved (0)												
04h	**BIST_DW0**	BIST Pattern DWord 0																															
05h	**BIST_DW1**	BIST Pattern DWord 1																															
06h	**SYSCTRL**	Reserved (0)																								BIST_scram	BIST_en	ff_threshold	Plug_irq	Tx_only_en	CONT_Disable	RxSCRMDIS	SEND_BIST
07h	**Debug 0**	Debug_0[31:0]																															
08h	**Debug 1**	Debug_1[31:0]																															
09h	**PHYCTRL**	ACTL [39:32]								0				GCO [3:0] / (reserved)			0				MS_SSC	MS_OOB	SSCSEL	Bridge_LSI	0	TX_RX_TST / (0)	TXAMP [2:0]			Force3G	Force PHYRDY	TXEN	
0Ah	**ACTL**	ACTL[31:0]																															
0Bh	**BIST_DW2**	BIST Pattern DWord 2																															
0Ch	**BIST_DW3**	BIST Pattern DWord 3																															
0Dh	**BIST_DW4**	BIST Pattern DWord 4																															
0Eh	**BIST_DW5**	BIST Pattern DWord 5 / Received data in TX_RX_TST mode																															
0Fh	**NOTIFY**	Reserved (0)																			pm_port [3:0]					Notify [15:0]							

Table 6-11 Description of Register Map

Register Name	ATA Address	UART Address	Description
SStatus	00h	00-03h	**Various Status for Serial ATA**

bit	*R/W*	*Reset*	*Description*
3:0	R	0000	**DET**. (Detection State) 0000 SATA device was not detected. 0001 SATA device was detected, but transfer rate failed to be set. 0011 Initialization completed and interface has become available. 0100 Interface is off-line. Others (Reserved)
7:4	R	0001	**SPD**. (Speed State) 0000 Transfer rate failed to be set. (Including the case when the device was not detected.) 0001 Transfer rate was set in 1.5 Gbps. Others (Reserved)
11:8	R	0000	**IPM**. (Interface Power Management state) 0000 Transfer rate failed to be set. (Including the case when the device was not detected.) 0001 Active mode 0010 PARTIAL mode 0110 SLUMBER mode Others (Reserved)
Others	R	0	(Reserved)

SError	01h	04-07h	**Indication of Serial ATA Error/Diagnostic Results**

bit	*R/W*	*Reset*	*Description*
0	R/WC	0	**I.** Although the data had an error, correct data has been sent by another attempt to transfer.
1	R/WC	0	**M.** Temporarily subjected to 'PHY not READY', but recovered.
8	R/WC	0	**T.** Non-recovered transient data integrity error.
9	R/WC	0	**C.** Non-recovered persistent communication or data integrity error.
10	R/WC	0	**P.** Protocol error was detected.
11	R/WC	0	**E.** Internal error was detected.
16	R/WC	0	**N.** PhyRdy signal value changed.
17	R/W	0	**I.** PHY internal error was detected.
18	R/WC	0	**W.** CommWake was detected.
19	R/WC	0	**B.** 10B/8B decode error was detected.
20	R/WC	0	**D.** Disparity error was detected.
21	R/WC	0	**C.** CRC error was detected.
22	R/WC	0	**H.** Handshake error (R_ERR) was detected.
23	R/WC	0	**S.** Link layer detected an error.

Register Name	ATA Address	UART Address	Description			
			24	R/WC	0	**T.** Transport layer detected an error.
			25	R/WC	0	**F.** Undefined FIS was detected.
			Others	R	0	Reserved.
SControl	02h	08-0Bh	**Serial ATA Control Register**			
			bit	***R/W***	***Reset***	***Description***
			3:0	R/W	0000	**DET.** (Initialize Sequence Request) 0000 No execution to be performed. 0001 Start an initialization of the interface, just like for the hard resetting. 0100 Set in the off-line mode. All other values reserved.
			7:4	R/W	0001	**SPD.** (Speed Restrictions) 0000 No restrictive condition for deciding a transfer rate. 0001 Only 1.5Gbps transfer rate is available. All other values reserved.
			11:8	R/W	0000	**IPM.** (Power Mode Restrictions) 0000 No restrictive condition for power control. 0001 Not available in the PARTIAL mode only. 0010 Not available in the SLUMBER mode only. 0011 Not available in the PARTIAL and SLUMBER modes. All other values reserved.
			Others	R/W	0	Reserved.
BIST_CTL	03h	0C-0Fh	**Control Register for BIST mode**			
			bit	***R/W***	***Reset***	***Description***
			20	RW	0	**L.** Execution of the far-end retimed loop-back mode. 0: Invalid 1: Valid
			21	RW	0	**S.** Scrambled data will be transferred. 0: Valid. 1: Invalid
			22	R	0	When transferring data in the transmitting-only mode, ALIGN primitive will be inserted.
			23	RW	0	**T.** Execution of the far-end transmitting-only mode. 0: Invalid 1: Valid
			others	R	0	Reserved.

Register Name	ATA Address	UART Address	Description
BIST_DW0	04h	10-13h	**Transfer data pattern 0 for BIST mode**
			bit / ***R/W*** / ***Reset*** / ***Description***
			31:0 / RW / 0 / BIST pattern (data prior to 10b/8b encoding)
BIST_DW1	05h	14-17h	**Transfer data pattern 1 for BIST mode**
			bit / ***R/W*** / ***Reset*** / ***Description***
			31:0 / RW / 0 / BIST pattern (data prior to 10b/8b encoding).
SYSCTRL	06h	18-1Bh	**System control register**
			bit / ***R/W*** / ***Reset*** / ***Description***
			0 / RW / 0 / **SEND_BIST.** Send BIST FIS. 0: Normal operation. 1: BIST FIS transferring request. If this data bit is set in, BIST_DW0, BIST_DW1 and BIST_DW2 will be transferred.
			1 / RW / 0 / **RxSCRMDis.** Receiver scrambler disable. 0: Enable receiver scrambler. 1: Disable receiver scrambler.
			2 / RW / 0 / **CONT_Disable.** CONT primitive enable. 0: Enable CONT primitive. 1: Disable CONT primitive.
			3 / RW / 0 / **Tx_only_en.** Transfer of BIST pattern shall be started forcibly. Before setting this data bit, Force PHYRDY bit should be set in.
			4 / RW / 0 / **Plug_irq.** Reserved.
			5 / RW / 0 / **ff_threshold.** Reserved.
			6 / RW / 0 / **BIST_en**. Reserved.
			7 / RW / 0 / **BIST_scram.** Reserved.
			others / R / 0 / Reserved.
DEBUG_0	07h	1C-1FH	**System Debug Port 0**
DEBUG_1	08h	20-23H	**System Debug Port 1**
PHYCTRL	09h	24-27h	**PHY Control Register**
			bit / ***R/W*** / ***Reset*** / ***Description***
			0 / RW / 1 / **TXEN.** Transmitter enable. 0: Disable. 1: Enable.
			1 / RW / 0 / **FORCEPHYRDY.** Forced PHY ready. 0: (Normal operation) 1: PHYRDY will be set in forcibly.

Register Name	ATA Address	UART Address	Description				
			2	RW	0	**FRCE3G.** Reserved.	
			5:3	RW	011	**TXAMP.** Transmitter amplitude control.	
			6	R	0	BU29504/	Reserved.
				RW		other model	**TX_RX_TST.** RX+ RX- read : BIST_DW5: TX+ TX- controlled : BIST_DW0, BIST_DW1:
			9:7	R	0	Reserved.	
			10	RW	1	**Bridge_LSI**. should not be changed.	
			11	RW	1	**SSCSEL.** should not be changed.	
			12	RW	0	**MS_OOB.** Reserved.	
			13	RW	0	**MS_SSC.** Reserved.	
			15:14	R	0	Reserved.	
			19:16	R	0	BU29504/	Reserved.
					TBD	other model	**GCO.** Calibration result.
			23:20	R	0	Reserved.	
			31:24	RW	0	ACTL [39:32]	

Register Name	ATA Address	UART Address	Description				
ACTL	0Ah	28-2Bh	**PHY Control Register ACTL [31:0]**				
			bit	***R/W***	***Reset***	***Description***	
			31:0	RW	0x2A1E99	BU29504	ACTL [39:0] Based on the default setting.
					-	BU19520	
					-	Other	
BIST_DW2	0Bh	2C-2Fh	**Transfer data pattern 2 for BIST mode**				
			bit	***R/W***	***Reset***	***Description***	
			31:0	RW	0	BIST pattern	
BIST_DW3	0Ch	30-33h	**Transfer data pattern 3 for BIST mode**				
			bit	***R/W***	***Reset***	***Description***	
			31:0	RW	0	BIST pattern	
BIST_DW4	0Dh	34-37h	**Transfer data pattern 4 for BIST mode**				
			bit	***R/W***	***Reset***	***Description***	
			31:0	RW	0	BIST pattern	
BIST_DW5	0Eh	38-3Bh	**Transfer data pattern 5 for BIST mode / Received data in TX_RX_TST mode**				
			bit	***R/W***	***Reset***	***Description***	
			31:0	RW	0	BU29504	BIST pattern
				RW /R		other	BIST pattern / Received data in the TX_RX_TST mode
NOTIFY	0Fh	3C-3Fh	**Notify.**				
			bit	***R/W***	***Reset***	***Description***	
			15:0	RW	0	**Notify register.** Reserved.	
			19:16	RW	0	**pm_port[3:0].** Reserved.	
			31:20	RW	0	Reserved.	

7 Electrical Specifications

7.1 Absolute Maximum Rating

Table 7-1 Absolute Maximum Rating

(Unless otherwise indicated, Ta = 25[℃])

Item	Symbol	Rating		Unit	Remarks
		BU29504	Other Model		
Supply Voltage 1 (for I/O)	VCCO	+4.5	-	V	Applicable for 4-pin and 44-pin.
Supply Voltage 2 (for core)	VCCK	+2.5	-	V	Applicable for 9-pin, 41-pin and 56-pin.
Supply Voltage 3 (for PLL)	AVDDH	+4.5	-	V	Applicable for 24-pin.
Supply Voltage 4 (for TX, RX)	AVDDL	+2.5	-	V	Applicable for 29-pin.
Storage Temperature Range	Tastg	-55 to +125	-	℃	
Input voltage	Vin	-0.3 to VCCO+0.3	-	V	
Power dissipation	Pd	1000	-	mW	Ta = 25 [degrees C] (For temperature 25 [degrees C] and above, it should be -10 [mW/degrees C].)

7.2 Operating Conditions

Table 7-2 Operating Conditions

(Unless otherwise indicated, Ta=25℃)

Item	Symbol	Spec.			Unit	Condition	Circuit Form
		BU29504					
		Min.	Typ.	Max.			
Operating Temperature Range	TOPR	0	25	70	Degrees C	-	-
Operational Supply Voltage (for I/O)	VCCO	3.0	3.3	3.6	V	-	-
Operating Supply Voltage (for core)	VCCK	1.62	1.80	1.98	V	-	-
Operating Supply Voltage (for analog)	AVDDH	3.0	3.3	3.6	V	-	-
Operating Supply Voltage (for analog)	AVDDL	1.62	1.80	1.98	V	-	-
Input voltage	Vin	-0.3		VCCO +0.3	V	All digital inputs	1,2,3,4

7.3 Electrical Characteristics

Unless otherwise indicated, VCCO = AVDDH = 3.3[V], VCCK = AVDDL = 1.8[V], and Ta = 25[degrees C]

Table 7-3 Circuit Current

Item	Symbol	Rating			Unit	Remarks
		BU29504				
		Min.	Typ.	Max.		
Consumption Current at Normal Operation (Without Data Transfer)	Ivcco	-	1	-	mA	VCCO (3.3V)
	Ivcck	-	58	-	mA	VCCK (1.8V)
	Iavddh	-	20	-	mA	AVCCH (3.3V)
	Iavddl	-	46	-	mA	AVCCL (1.8V)
Consumption Current at Partial	Ivcco	-	1	-	mA	VCCO (3.3V)
	Ivcck	-	30	-	mA	VCCK (1.8V)
	Iavddh	-	20	-	mA	AVCCH (3.3V)
	Iavddl	-	40	-	mA	AVCCL (1.8V)
Consumption Current at Slumber	Ivcco	-	1	-	mA	VCCO (3.3V)
	Ivcck	-	1	-	mA	VCCK (1.8V)
	Iavddh	-	20	-	mA	AVCCH (3.3V)
	Iavddl	-	26	-	mA	AVCCL (1.8V)

During normal operation, the consumption current is measured with PHYRDY being set after the Power On Reset Sequence completes and also in the mode prior to receiving a command (when no data transfer has been performed).

Table 7-4 Characteristics of Digital Circuit Input/Output Voltage

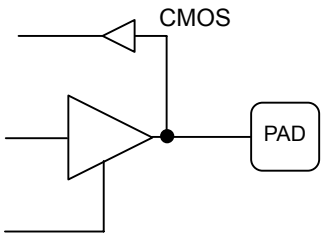
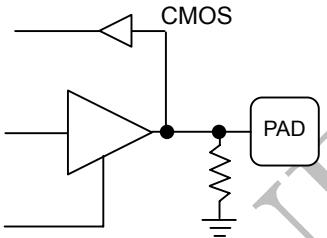
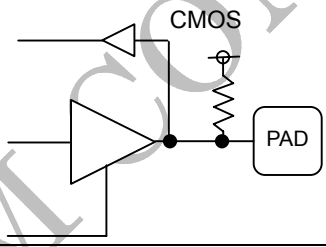
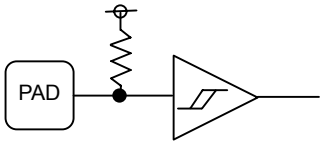
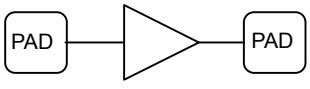
Item	Symbol	Rating			Unit	Remarks
		BU29504				
		Min.	Typ.	Max.		
'L' Input Voltage	Vil	- 0.3	-	0.3 x VCCO	V	3.0V ～ 3.6V
'H' Input Voltage	Vih	0.7 x VCCO	-	VCC +0.3	V	3.0V ～ 3.6V
'L' Output Voltage	Vol	-	-	DGND +0.4	V	3.0V
'H' Output Voltage	Voh	VCCO – 0.4	-	-	V	3.0V
Pull-Up Resistor	Rup	12.0	-	73.0	kΩ	At Pad = 0V, VCCO = 3.0V ～ 3.6V
Pull-Down Resistor	Rdn	22.0	-	100.0	kΩ	At Pad = 3.0V ～ 3.6V, VCCO = 3.0V ～ 3.6V
Input Leak Current	Iil	-1	-	1	μA	
Threshold Voltage	Vth+	1.69	-	2.37	V	At input voltage increasing (17-pin only)
	Vth-	1.01	-	1.58	V	At input voltage decreasing (17 pin only)
Hysteresis Voltage	Vh	0.30	-	0.85	V	(17 pin only)

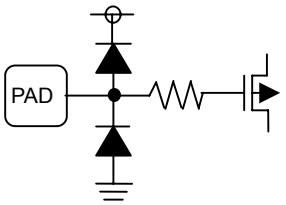
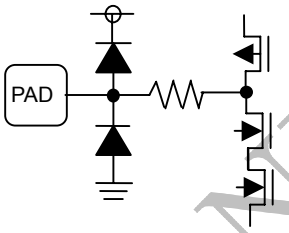
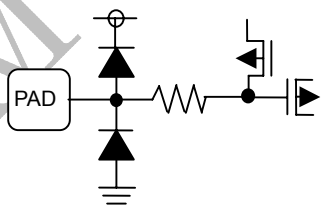
Table 7-5 AC Characteristics of OSC Circuit

Item	Symbol	Rating			Unit	Remarks
		BU29504				
		Min.	Typ.	Max.		
XTALIN Input Frequency	Fin	-	25	-	MHz	Accuracy of frequency should be within 100ppm.

7.4 Circuit Forms

Table 7-6 Circuit Forms

Name	Circuit Diagram	Pin No.
1. Bi-directional CMOS Input/Output		(1) DD[13], (2) DD[2], (5) DD[3], (6) DD[11], (7) DD[4], (10) DD[10], (12) DD[9], (13) DD[6], (14) DD[8], (15) DD[7], (61) DD[15], (62) DD[0], (63) DD[14], (64) DD[1], (16) RESETn, (47) CSn[1], (48) CSn[0], (49) DA[2], (50) DA[0], (51) DA[1], (53) INTRQ, (54) DMACKn, (55) IORDY, (58) DIORn, (59) DIOWn
2. Bi-directional CMOS Input/Output (With Pull-Down Resistor)		(3) DD[12], (11) DD[5], (18) MODE[0], (20) MODE[2], (33) MSSEL, (35) SSCEN, (37) CLKSEL[1] , (38) FXDMA, (40) PHYRDY, (52) SP, (60) DMARQ
3. Bi-directional CMOS Input/Output (With Pull-Up Resistor)		(19) MODE[1], (21) ATAIOEN, (34) DASPn, (36) CLKSEL[0], (39) PMEN, (43) UAI, (45) UAO, (46) PDIAGn
4. Schmitt Input (With Pull-Up Resistor)		(17) PORn
5. Oscillator Circuit		(22) XTALIN, (23) XTALO

Name	Circuit Diagram	Pin No.
6. Differential Input		(27) RXP, (28) RXN
7. LVDS Output		(31) TXN, (32) TXP
8. Current Source Input		(26) REXT

8 Evaluation Results

8.1 Results from Connectivity Verification (BU29504)

3. Results from Connectivity Verification

ATAPI Mode

Motherboard w/ SATA	Device Name			
	Pioneer DVD-RW		Plextor DVD-RW	
	Test Item	OK/NG	Test Item	OK/NG
GIGABYTE GA-8I915G ICH6 (IDE Mode)	Boot BIOS	OK	Boot BIOS	OK
	Boot WinXP	OK	Boot WinXP	OK
	Nero burn data	OK	Nero burn data	OK
	DVD Speed	OK	DVD Speed	OK
	Standby&Hibernate	OK	Standby&Hibernate	OK
GIGABYTE GA-8I915G ICH6R SATA (AHCI Mode)	Boot BIOS	OK	Boot BIOS	OK
	Boot WinXP	OK	Boot WinXP	OK
	Nero burn data	OK	Nero burn data	OK
	DVD Speed	OK	DVD Speed	OK
	Standby&Hibernate	OK	Standby&Hibernate	OK
ASUS P4V800-X VIA8237	Boot BIOS	OK	Boot BIOS	OK
	Boot WinXP	OK	Boot WinXP	OK
	Nero burn data	OK	Nero burn data	OK
	DVD Speed	OK	DVD Speed	OK
	Standby&Hibernate	OK	Standby&Hibernate	OK
ASUS P4S800D SiS964	Boot BIOS	OK	Boot BIOS	OK
	Boot WinXP	OK	Boot WinXP	OK
	Nero burn data	OK	Nero burn data	OK
	DVD Speed	OK	DVD Speed	OK
	Standby&Hibernate	OK	Standby&Hibernate	OK
ASUS P4C800 ICH5 (IDE Mode)	Boot BIOS	OK	Boot BIOS	OK
	Boot WinXP	OK	Boot WinXP	OK
	Nero burn data	OK	Nero burn data	OK
	DVD Speed	OK	DVD Speed	OK
	Standby&Hibernate	OK	Standby&Hibernate	OK

ATA Mode

Motherboard w/ SATA	Device Name			
	HITACHI 160GB		WD 40GB	
	Test Item	OK/NG	Test Item	OK/NG
GIGABYTE GA-8I915G ICH6 (IDE Mode) SSC enabled	Boot BIOS	OK	Boot BIOS	OK
	Boot WinXP	OK	Boot WinXP	OK
	Write/Read	OK	Write/Read	OK
	Standby&Hibernate	OK	Standby&Hibernate	OK
GIGABYTE GA-8I915G ICH6R (AHCI Mode) SSC enabled	Boot BIOS	OK	Boot BIOS	OK
	Boot WinXP	OK	Boot WinXP	OK
	Write/Read	OK	Write/Read	OK
	Standby&Hibernate	OK	Standby&Hibernate	OK
	Aggressive Power Mode	OK	Aggressive Power Mode	OK
ASUS P4V800-X VIA8237 SSC enabled	Boot BIOS	OK	Boot BIOS	OK
	Boot WinXP	OK	Boot WinXP	OK
	Write/Read	OK	Write/Read	OK
	Standby&Hibernate	OK	Standby&Hibernate	OK
ASUS P4V800D SiS964 SSC enabled	Boot BIOS	OK	Boot BIOS	OK
	Boot WinXP	OK	Boot WinXP	OK
	Write/Read	OK	Write/Read	OK
	Standby&Hibernate	OK	Standby&Hibernate	OK
ASUS P4C800 ICH5 (IDE Mode) SSC enabled	Boot BIOS	OK	Boot BIOS	OK
	Boot WinXP	OK	Boot WinXP	OK
	Write/Read	OK	Write/Read	OK
	Standby&Hibernate	OK	Standby&Hibernate	OK

HOST Mode:Interoperability Test Results (SSC ON/OFF)

SATA Device	Maker	Model	SSC-OFF	SSC-ON
Marvell (8030-B6P)	MAXTOR	6Y160M004721A	OK	OK
Marvell (8030-B6P)	WD	360	OK	OK
Marvell (8030-B5P)	SAMSUNG	SP2004C	OK	OK
Marvell (8030-B2P)	SAMSUNG	SP2004C	OK	NG
BU9580KVT	HITACHI	DK23AA-12	OK	OK
BU9580KVT	HITACHI	HTS541040G9AT00	OK	OK
AGERE	SEAGATE	ST380819As	OK	OK
Infinion	HITACHI	HDS728080pla380	OK	OK

DEVICE Mode:Interoperability Test Results (SSC ON/OFF)

SATA Device	Maker	Model	SSC-OFF	SSC-ON
Intel (ICH5)	ASUS	P4P800	OK	OK
Intel (ICH6)	GIGABYTE	GA-8I915	OK	OK
Intel (ICH6R)	GIGABYTE	GA-8I915G	OK	OK
Intel (ICH7)	GIGABYTE	GA-8I955	OK	OK
SiS (964)	ASUS	P4S800-D	OK	OK
VIA (VT8237)	ASUS	P4V800-X	OK	OK
Silicon Image (3112A)	FCCE	5-SATA-01A	OK	OK
Uli (M1573)	MSI	RD480	OK	OK
nVidia (nForce410 MCP)	Asrock	939NF4G-SATA2	OK	OK
nVidia (nForce4-Ultra)	ASUS	A8N-E	NG (Note 2)	NG (Note 2)

Note 1) Devices which was used in the Device mode are as follows:

BenQ:DW1620-ON2 DVD-R/W Drive
Pioneer: DVD-R/W Drive
MAXTOR:D540X-4K HDD
HITACHI:HTS5410 HDD

Note 2) The combination of BenQ:DW1620-ON2(DVD-R/W) and Nero 6616 is not available, while BenQ:DW1620-ON2(DVD-R/W) and Nero 6302 can be used in combination. This is because vendor definition commands in the ATA COMMAN have been issued, which is not a bug but a limitation of permeability of the bridge c

SATA Compliance Test Results (BU29504)

Conditions:

Temp. = 25 degrees C

Power = 3.3V/1.8V

Oscilloscope: LeCroy SDA6000A

Waveform generator: Tektronix DTG5334

TDR: Agilent 86100C

	UI [ps]	Tj(n=5) [ps]	Tj(n=250) [ps]	Tr[ps] (min)	Tr[ps] (max)	Tf[ps] (min)	Tf[ps] (max)	
DS-2-1	666.520	54.550	80.010	109.730	137.640	113.040	141.400	
DS-2-2	666.510	47.270	94.540	109.920	135.750	112.300	139.210	
DS-2-3	666.530	47.270	80.010	114.450	143.700	114.160	140.870	
Target	666.630	50.000	92.000	109.000	136.000	112.000	137.000	
Ave.	666.520	49.773	86.640	110.775	138.273	112.875	139.620	
Sigma.	0.056	3.435	7.726	2.482	3.714	0.962	1.980	
Spec. Max	670.12	200.00	300.00		273.00		273.00	
Spec. Min	666.43			100.00		100.00		
Cpk	3	11.92	8.55	1.42	10.75	4.69	38.66	

	Vdiff(Tx) [mV] (min)	Vdiff(Tx) [mV] (max)	Vdiff(Rx) [mV] (min)	Vdiff(Rx) [mV] (max)	Vcm(Tx) [mV]	Vcm(Rx) [mV]	Tx imp. [Ω}	Rx imp. [Ω}
DS-2-1	437.10	547.60	377.10	518.40	52.00	85.90	99.80	105.60
DS-2-2	440.00	554.90	380.00	500.10	54.80	89.30	95.30	107.00
DS-2-3	437.10	565.80	397.10	524.70	46.30	89.00	97.70	102.00
Target	430.00	550.00	390.00	525.00	55.00	90.00	100.00	103.00
Ave.	436.05	554.58	386.05	514.40	51.03	88.07	97.60	104.87
Sigma.	4.26	8.08	9.21	11.70	4.05	1.82	2.20	2.58
Spec. Max		600.00		600.00	100.00	100.00	115.00	115.00
Spec. Min	400.00		325.00				85.00	85.00
Cpk	7.58	1.60	1.84	2.23	3.77	2.11	1.87	1.31

	Squel. [mV]	Uoob [ps]	Xmit-Bst len [ns]	RST/INIT B-gap[ns]	WAKE B-gap[ns]	Align Send[us]		
DS-2-1	161.800	654.738	104.760	320.690	108.000	32.020		
DS-2-2	170.400	655.360	104.860	321.690	108.460	31.160		
DS-2-3	167.700	659.331	105.400	321.120	108.510	31.400		
Target	165.000	666.700	106.700	320.000	106.700	32.000		
Ave.	166.633	656.476	105.007	321.167	108.323	31.527		
Sigma.	4.398	2.492	0.344	0.502	0.281	0.444		
Spec. Max	200.00	686.67	109.90	329.60	109.90			
Spec. Min	50.00	646.67	103.50	310.40	103.50	54.61		
Cpk	2.53	1.31	1.46	5.6	1.87	17.34		

	RST/INIT In-Spec	RST/INIT Out-Spec	WAKE In-Spec	WAKE Out-Spec	Eye (Tx)	Eye (Rx)	Wd/Rd Stress	
DS-2-1	OK	OK	OK	OK	OK	OK	OK	
DS-2-2	OK	OK	OK	OK	OK	OK	OK	
DS-2-3	OK	OK	OK	OK	OK	OK	OK	
Target	OK	OK	OK	OK	OK	OK	OK	
Ave.	-	-	-	-	-	-	-	
Sigma.	-	-	-	-	-	-	-	
Spec. Max	329	>525	112	>515	-	-	-	
Spec. Min	310	<175	101.3	<175	-	-	-	
Cpk	-	-	-	-	-	-	-	

Revision Record

Ver.	Revised Items	Details	Date
0.80	First edition	-	-
0.92	-	Corrected.	Feb. 23, 2007
0.97	-	Corrected.	Aug. 24, 2007