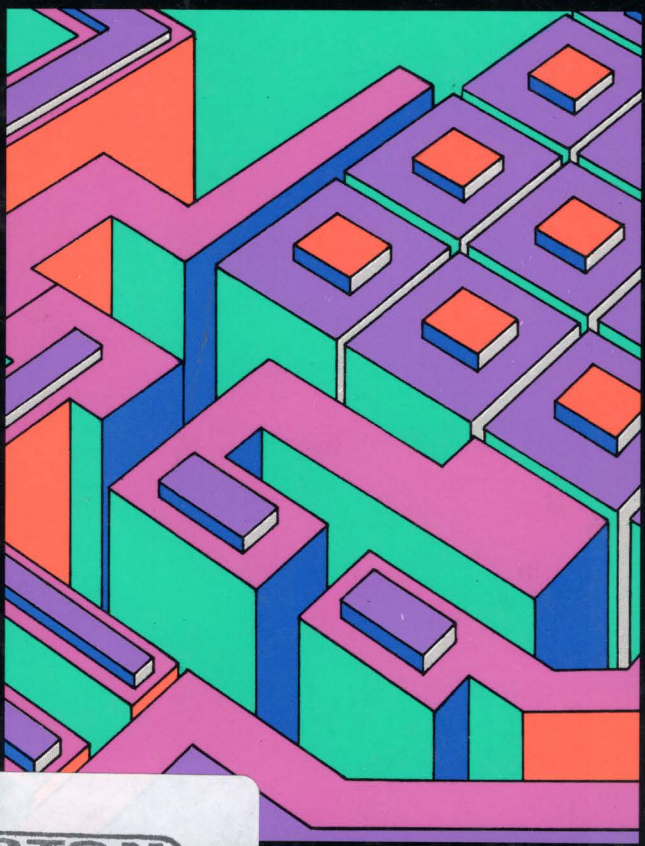
THE L4970 SWITCHING REGULATOR IC FAMILY

DESIGNER's DATABOOKLET



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L4970 SMPS IC FAMILY

DESIGNER'S DATA BOOKLET

1st EDITION

MAY 1989

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SELECTION GUIDE

SGS-THOMSON HIGH CURRENT SWITCHING REGULATOR ICs

	L497X FAMILY						BIPOLAR SOLUTIONS		
	L4970	**L4977**	**L4975**	**L4974**	**L4972**	**L4972D** Surface Mounting	**L296P**	**L4960**	**L4962**
Max Input Operating Voltage	50V	50V	50V	50V	50V	50V	46V	46V	46V
Output Voltage Range	5 1V to 40V ±2% (Internal Ref)								
Max Output Current	10A	7A	5A	3 5A	2A	2A	4A	2 5A	1 5
Max Output Power	400W	280W	200W	140W	80W	80W	160W	100W	60W
Power Switch	DMOS R_{DSON} 0 18ohm						V_{CESAT} 4A 3.2V	V_{CESAT} 2A 3V	V_{CESAT} 1 5A 2V
Switching Mode Control System	Continuous Mode, Direct Duty Cycle Control with Feed Forward (Improved Transient Response)						Continuous MODE, Direct Duty, Cycle Control		
Chopping Frequency	500kHz	500kHz	500kHz	200kHz	200kHz	200kHz	100kHz	100kHz	100kHz
Efficiency V_{INPUT} = 35V V_{OUT} = 5 1V 100kHz	10A 83%	7A 84%	5A 84%	3 5A 84%	2A 83%	2A 83%	3 5A 76%	2A 74%	1A 76%
Current Limiting	True Current Generator						Soft Start Triggers		
Soft Start	Yes						Yes		
Reset and Power Fail	Yes						Yes	No	No
Crowbar	No						Yes	No	No
Package Max $R_{thj\text{-}case(PIN)}$	Multiwatt15 1°C/W	Multiwatt15 1°C/W	Multiwatt15 1°C/W	Powerdip16+2+2 12°C/W	Powerdip16+2+2 12°C/W	SO20L 15°C/W	Multiwatt15 3°C/W	Heptawatt 4°C/W	Powerdip12+2+2 14°C/W

This table presents the characteristics off all SGS-THOMSON power switching regulator ICs. The L497X types are described in this booklets; datasheets for the bipolar ICs are included in the SGS-THOMSON Industrial and Computer Peripheral ICs databook.

HOW TO CHOOSE THE RIGHT STEPDOWN SMPS IC

CURRENT RANGE	MAIN DESIGN TARGETS							
	Component Cost	PCB Space	Power Dissipation	Reset Block	50V Input	Current Control and Best Line Regulation	DIP and SO Automatic Assembly	Crow bar
7 to 10A	L4970	L4970				L4970		
5 to 7A	L4977	L4977				L4977		
4 to 5A	L4975	L4975				L4975		
3 5 to 4A	L296P	L296P L4975	L4975	L296P	L4975	L4975		L296P
2 to 3 5A	L296P	L4974	L4974	L296P	L4974	L4974	L4974 (DIP)	
1 to 2A	L4960	L4972 L4972D		L4972 L4972D L296	L4972 L4972D	L4972 L4972D	L4972 (DIP) L4972D (SO)	
UP to 1A	L4962	L4962 L4972D	L4972 L4972D	L4972 L4972D	L4972 L4972D	L4972 L4972D	L4972 (DIP) L4962 (DIP) L4972D (SO)	

Use this table to identify the most suitable type for your application. The vertical columns represent possible main design considerations. For example, if 4A output current is needed and low dissipation is the most important design target the L4975 is the best solution.

DATASHEETS

10A SWITCHING REGULATOR

ADVANCE DATA

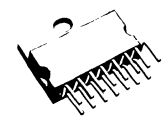
- 10A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND P. FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4970 include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components

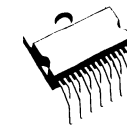
MULTIPOWER BCD TECHNOLOGY

Multiwatt 15
(15-lead)

Vertical



Horizontal

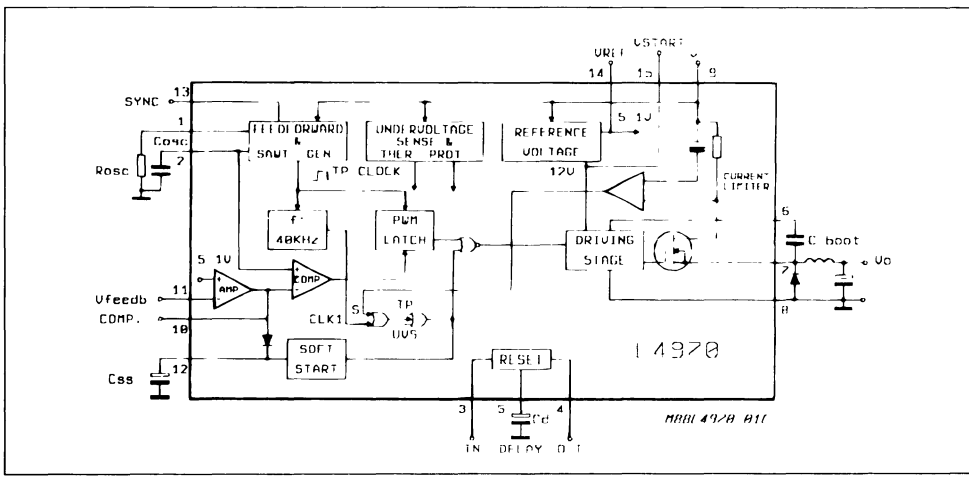


ORDER CODE : L4970 (Vertical)
L4970HT (Horizontal)

DESCRIPTION

The L4970 is a stepdown monolithic power switching regulator delivering 10A at a voltage variable from 5.1 to 40V.

BLOCK DIAGRAM

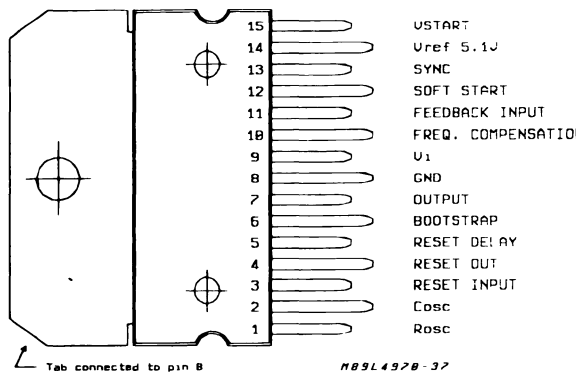


This advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	– 1 – 7	V V
I_7	Max Output Current	Internally limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	mA
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
7	OUTPUT	Regulator Output
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
12	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant.
13	SYNC INPUT	Multiple L4970's are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
14	V_{ref}	5.1V_{ref} Device Reference Voltage
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage

CIRCUIT OPERATION (refer to the block diagram).

The L4970 is a 10A monolithic stepdown switching regulator realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 10A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50nS. Due to the fast commutation switching frequencies upto 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing

Figure 1 : Feedforward Waveform.

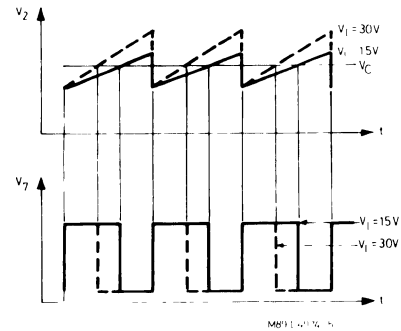


Figure 2 · Soft Start Function

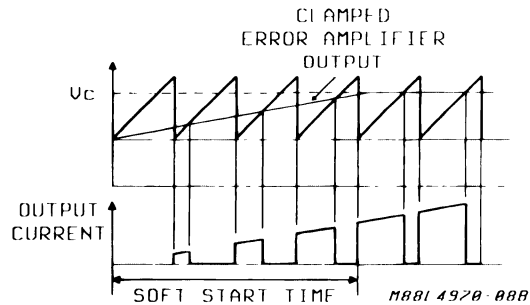
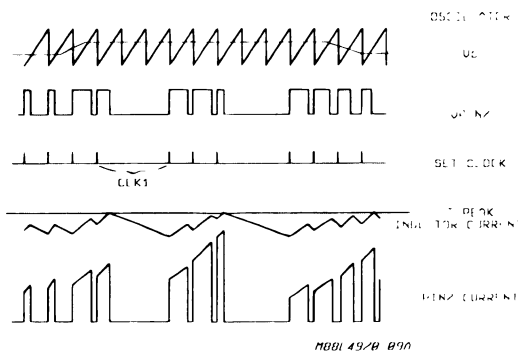


Figure 3 : Limiting Current Function.



the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy enviroments. The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency in this condition to 40kHz.

The Reset and Power fail circuit (fig. 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector drain.

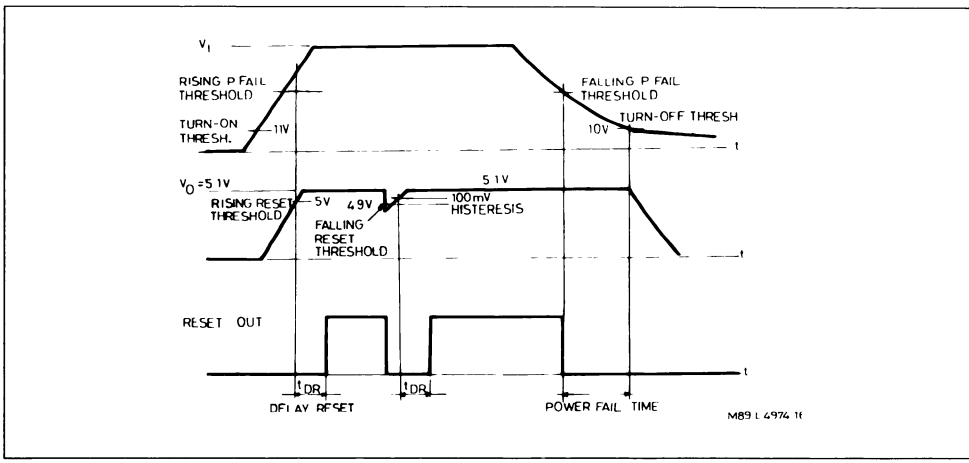
Fig. 4A shows the case when the supply voltage is higher than the threshold but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

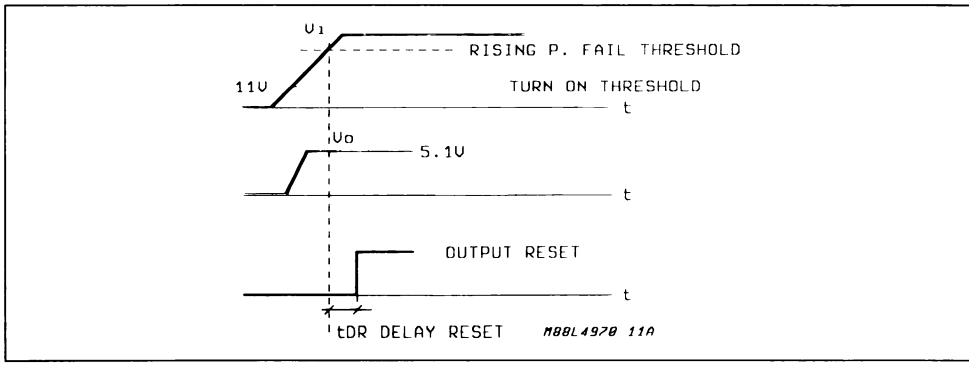
The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has an hysterysis to prevent unstable conditions.

Figure 4 : Reset and Power Fail Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 15KΩ , C_9 = 2.2nF, f_{sw} = 200KHz typ., unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 9)	V_o = V_{ref} to 40V I_o = 10A	15		50	V	5
V_o	Output Voltage	V_i = 15V to 50V I_o = 5A ; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 2A ; V_o = V_{ref}		12	30	mV	5
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 3A to 6A I_o = 2A to 10A		 10 20	 30 50	 mV mV	5
V_d	Dropout Voltage between Pin 9 and 7	I_o = 5A I_o = 10A		0.55 1.1	0.8 1.6	V V	5
I_{7L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	11	12.5	14	A	5
Efficiency		I_o = 5A V_o = V_{ref} V_o = 12V	80	85 92		 % %	5
		I_o = 10A V_o = V_{ref} V_o = 12V	75	80 87		 %	5
SVR	Supply Voltage Ripple Reject.	V_i = 2VRMS ; I_o = 5A f = 100Hz ; V_o = Vref	56	60		dB	5
f	Switching Freq.		180	200	220	KHz	5
$\Delta f/\Delta V_i$	Volt. Stability of Switching Freq.	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temp. Stability of Switch. Freq.	T_j = 0 to 125°C		1		%	5
f_{max}	Max. Operating Switch. Freq.	V_o = V_{ref} ; R_4 = 9.1KΩ I_o = 10A ; C_9 = 1.2nF	500			KHz	5

ELECTRICAL CHARACTERISTICS (continued)

V_{REF} SECTION (pin 14)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{REF}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{REF}	Line Regulation	V_I = 15V to 50V V_{12} = 0		10	25	mV	7
ΔV_{REF}	Load Regulation	I_{REF} = 0 to 3mA		20	40	mV	7
$\Delta V_{REF}/\Delta T$	Average Temp. Coeff. Ref. Voltage	T_j = 0°C to 125°C		0.4		mV/C	7
I_{REF}	Short Circuit Curr. Limit	V_{REF} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{ref}	Reference Voltage	P_{12} = 0V	11.4	12	12.6	V	7
ΔV_{ref}	Line Regulation	P_{12} = 0V ; V_I = 15 to 50V		0.4	1	V	7
ΔV_{ref}	Load Regulation	I_{ref} = 0 to 1mA P_{12} = 0V		50	200	mV	7
I_{ref}	Short Circuit Current Limit	P_{12} = 0V ; P_{15} = 0V		80		mA	7

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn–on Thresh.		10	11	12	V	7A
V_{9Hyst}	Turn–off Hyster.			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0 ; S1 = D ; S2 = C ; S4 = A		10	16	mA	7A
I_{9OQ}	Operating Quiescent Curr.	V_{12} = 0		16	20	mA	7A
I_{7L}	Out Leak Current	V_I = 55V ; S3 = A ; V_{12} = 0V			2	mA	7A

SOFT START (pin 12)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V ; V_{11} = 0V	70	100	130	µA	7B
V_{12s}	Output Saturation Voltage	I_{12s} = 20mA ; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level out Voltage	I_{10} = – 50µA ; S2 = A P_{11} = 0V ; S1 = C	6			V	7C
V_{10L}	Low Level out Voltage	I_{10} = 50µA ; S2 = A P_{11} = 6V ; S1 = C			0.7	V	7C
I_{11}	Input Bias Current	V_{11} = 5 ; S1 = B ; R_S = 10K		2	10	uA	7C
VOS	Input off Voltage	P_{11} = Vos ; R_s = 50Ω ; S1 = A		2	10	mV	7C
G_V	DC Open Loop Gain	P_{VCM} = 4V ; R_S = 50Ω ; S1 = A	60			dB	7C
SVR	Supply Volt. Rej.	15 < V_I < 50V	60	80		dB	7C

ELECTRICAL CHARACTERISTICS (continued)

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
	Ramp Valley			1.5		V	7A
	Ramp Peak	V_i = 15V V_i = 45V		2 5 5 5		V V	7A
	Min Ramp Current	S1 = A , I1 = 100µA		270	300	µA	7A
	Max Ramp Current	S1 = A , I1 = 1mA	2.4	2 7		mA	7A

SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYNC	Low Input Voltage	V_i = 15V to 50V	– 0 3		0.9	V	
SYNC	High Input Voltage	V_{12} = 0	3 5		5 5	V	
$-I_{13L}$	Sync Input Current with Low Input Voltage	V_{13} = 0 9V			0 4	mA	
$-I_{13H}$	Input Current with High Input Voltage	V_{13} = 3 5V			1.5	mA	
SYNC	Delay			50		ns	
	Output Amplitude		4	5		V	
	Output Pulse Width	V_{thr} = 2 5V	0 3	0 5	0.8	µsec	

RESET AND P. FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V S1 = B	Vref – 120	Vref – 100	Vref – 80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	V_i = 15 to 50V S1 = B	4 77	Vref – 200	Vref – 160	V mV	7D
V_{5H}	Delay High Threshold Voltage	S1 = B	5	5.1	5 2	V	7D
V_{5L}	Delay Low Threshold Voltage	S1 = B	1	1 1	1 2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5 3V , V_5 = 3V S1 = A	40	55	70	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V ; V_5 = 3V S1 = A	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA ; S2 = B			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V ; S2 = A			100	µA	7D
V_{3R}	Rising Threshold Voltage		5	5 1	5 2	V	7D
	Hysteresis		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Application Circuit

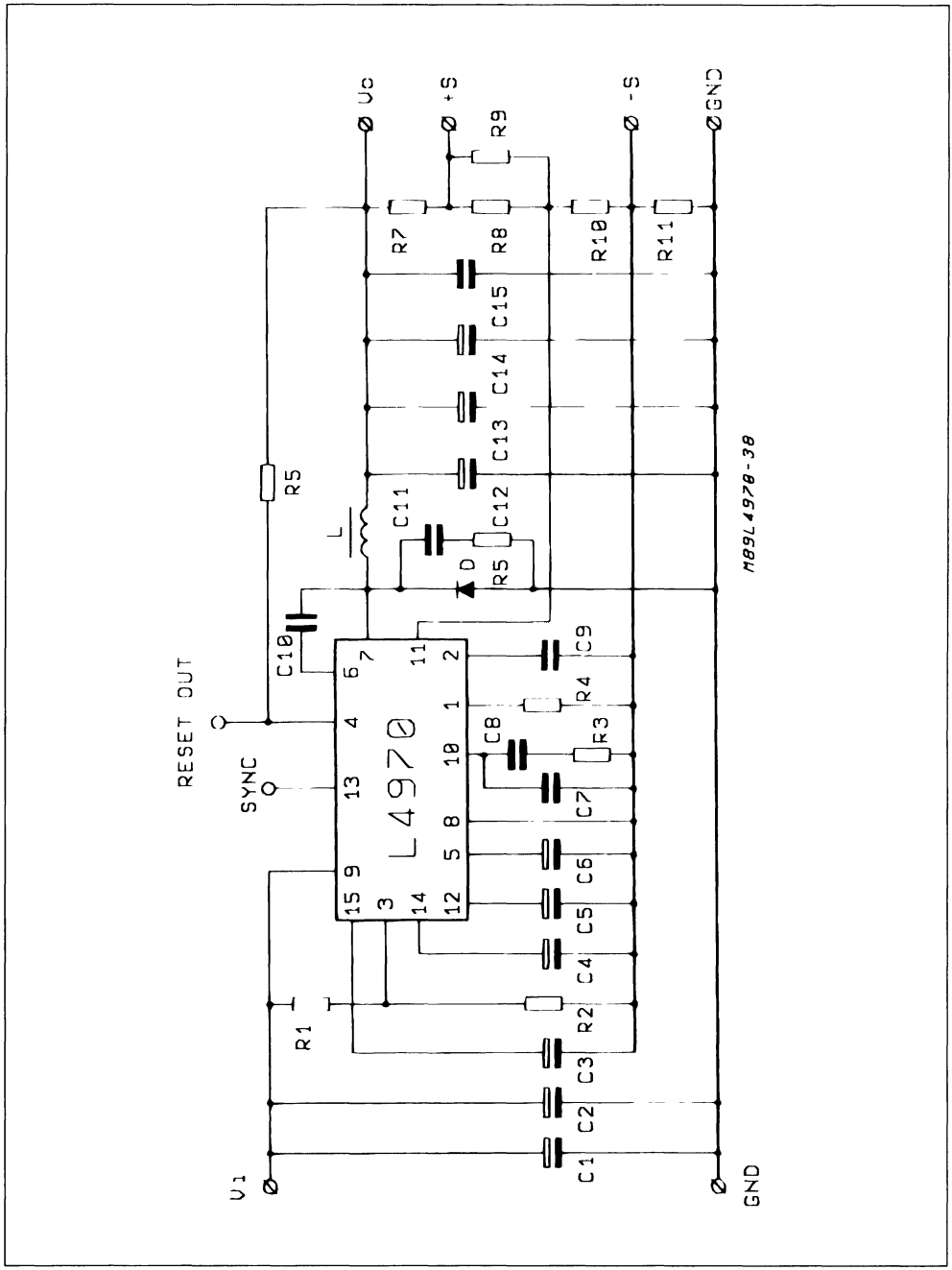
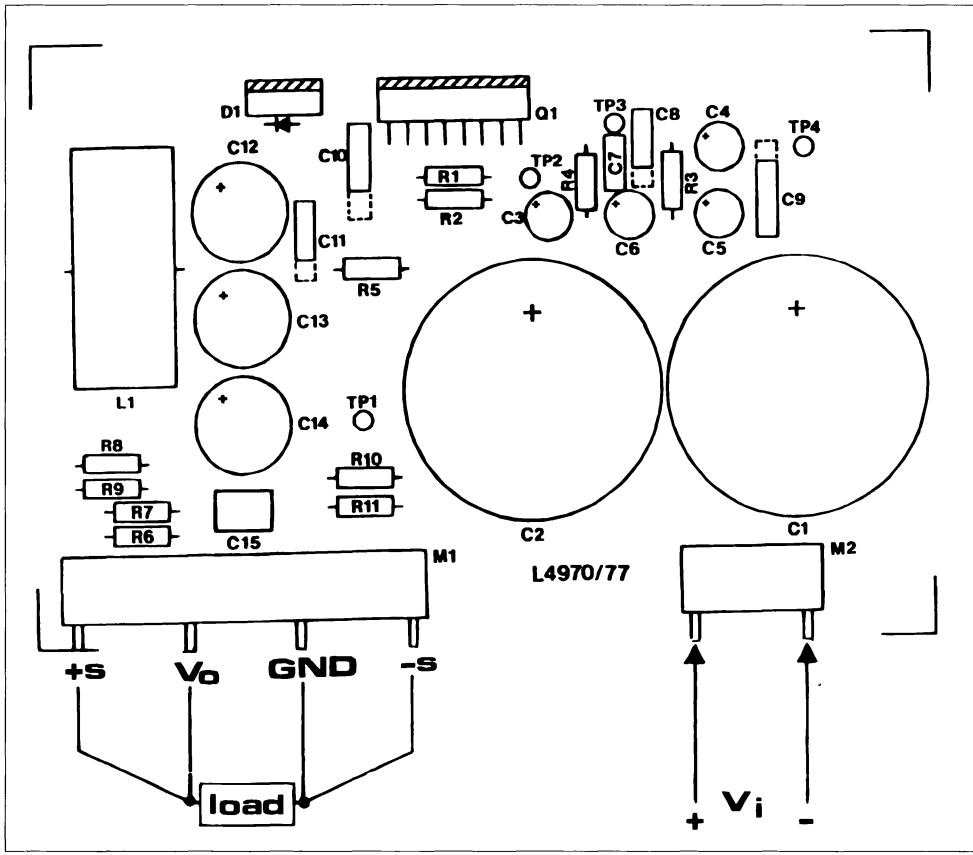


Figure 6 : Component Layout of Figure 5 (1:1 scale).



PART LISTS

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 22KΩ
R_4 = 15KΩ
R_5 = 22KΩ 0.5W
R_6 = 4K7
R_7 = 10KΩ
R_8 = see table A
R_9 = OPTION
R_{10} = 4K7
R_{11} = 10Ω
D = SBP 1660T
L = 40µH

*C_1, C_2 = 3300µF 63 V_L EYF (ROE)
C_3, C_4, C_5, C_6 = 2.2µF
C_7 = 390pF
C_8 = 22nF MKT 1817 (ERO)
C_9 = 2.2nF KP1830
C_{10} = 0.1µF MKT
C_{11} = 2.2nF MP 1830
**C_{12}, C_{13}, C_{14} = 220µF 40 V_L EKR (ROE)
C_{15} = 1µF Film

(or 16A/60V equivalent)
core 58071 MAGNETICS
27 TURNS Ø 1,3mm (AWG 16)
COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR.

Table A.

V_o	R_{10}	R_8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	4.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Figure 7 : DC Test Circuits.

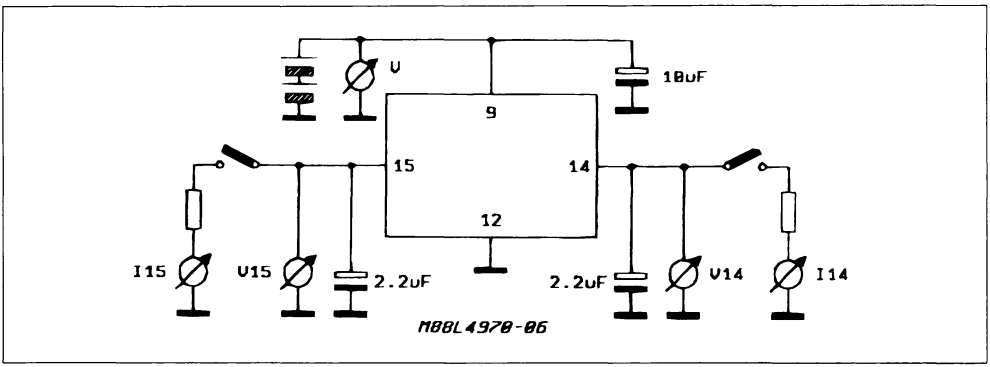


Figure 7A.

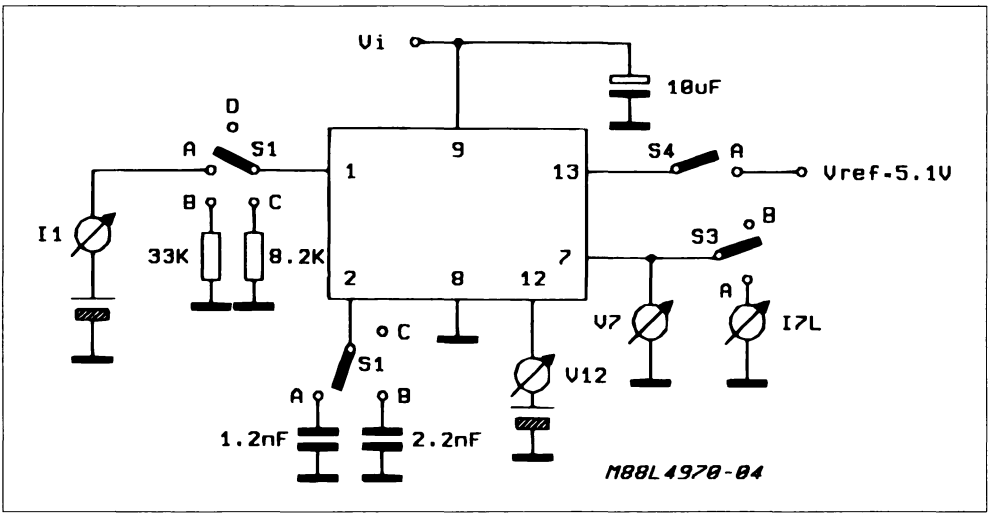


Figure 7B.

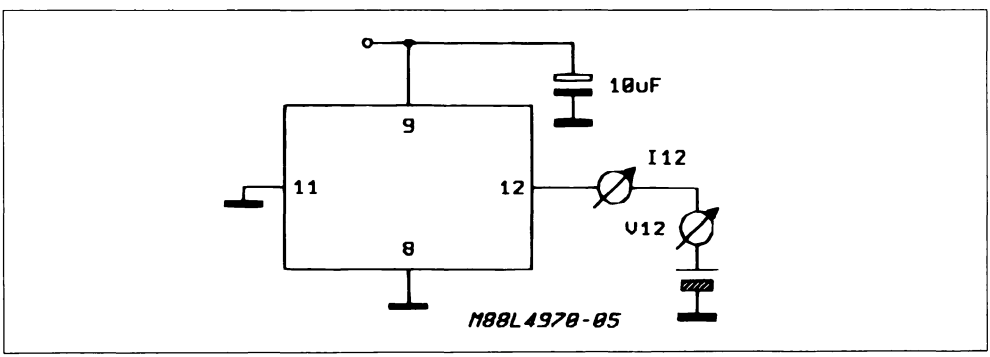


Figure 7C.

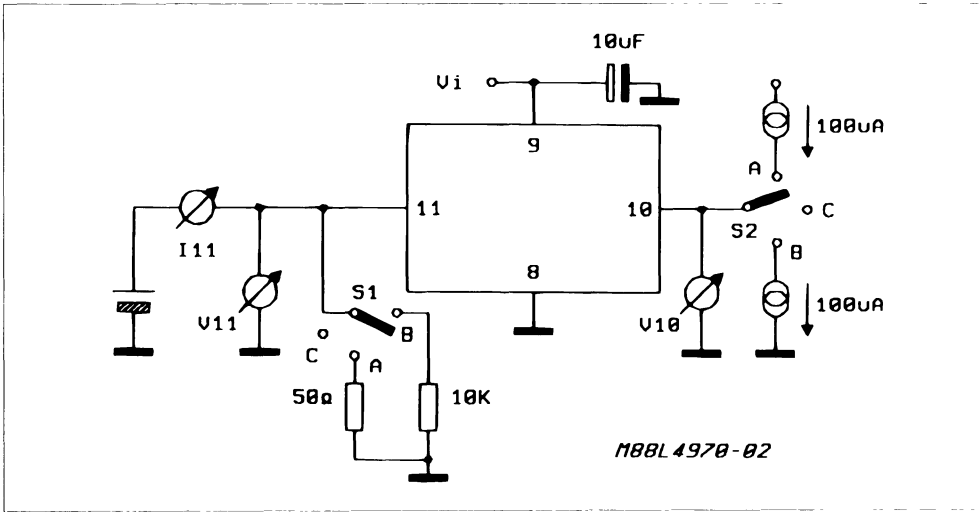


Figure 7D.

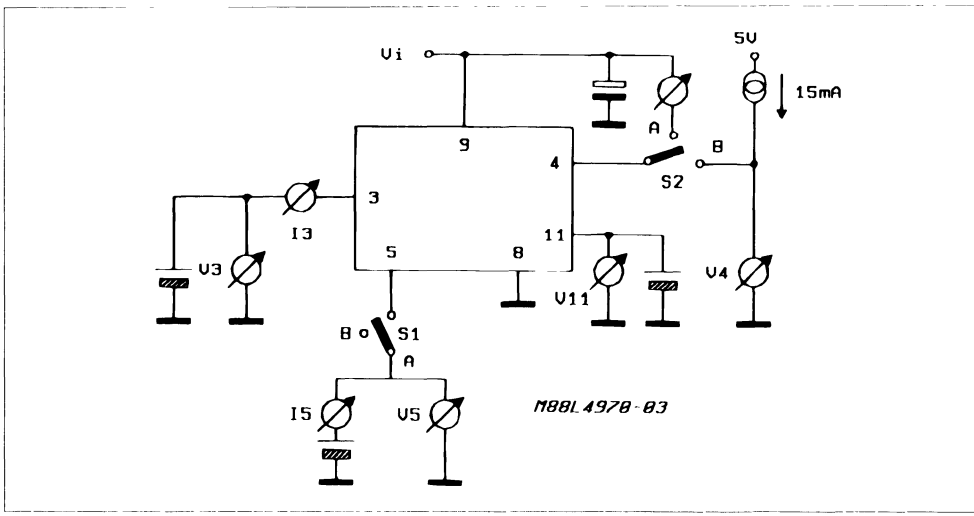


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0 % duty cycle - see fig. 7A).

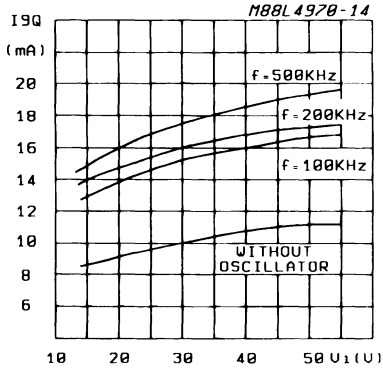


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0 % duty cycle).

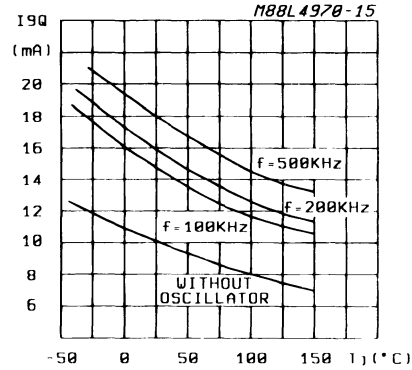


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

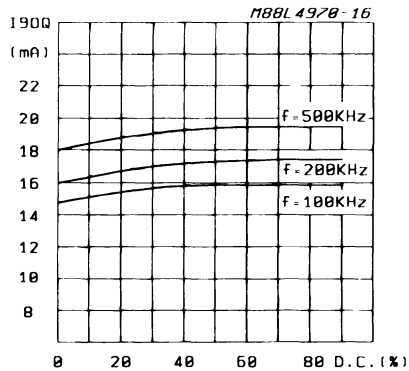


Figure 11 : Reference Voltage (pin 14) vs. V_i (see fig. 7).

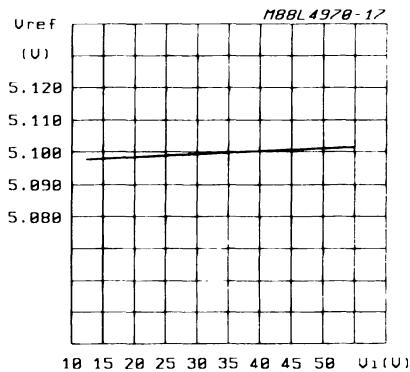


Figure 12 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

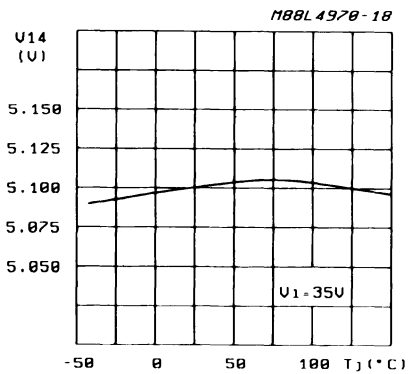


Figure 13 : Reference Voltage (pin 15) vs. V_i (see fig. 7).

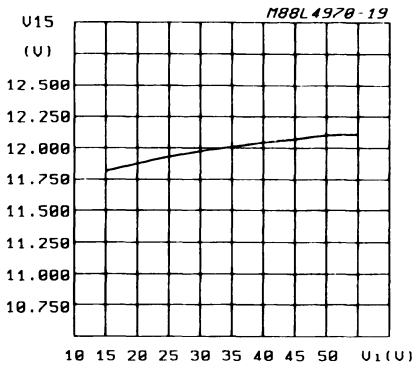


Figure 14 : Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7).

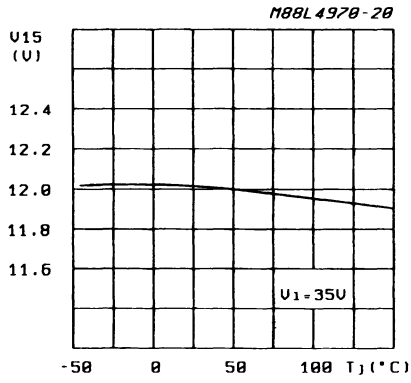


Figure 15 : Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency.

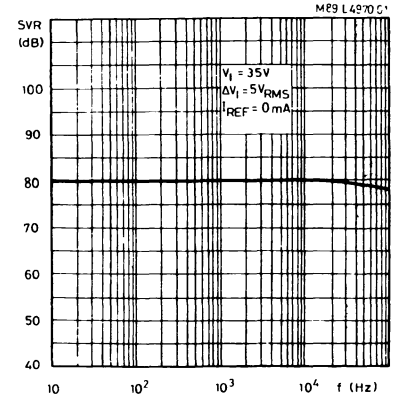


Figure 16 : Switching Frequency vs. Input Voltage (see fig.5).

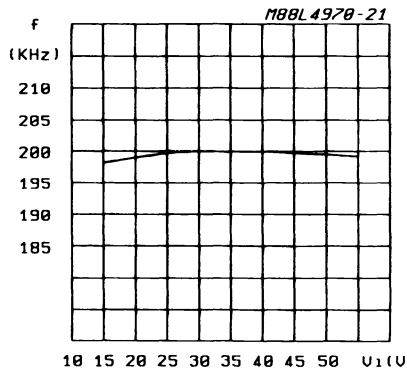


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

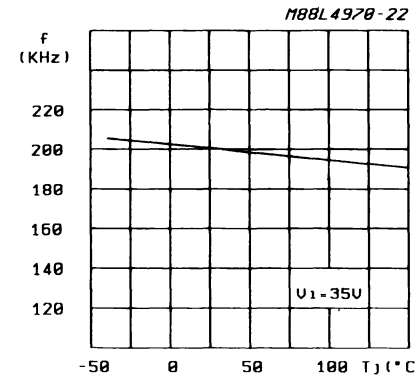


Figure 18 : Switching Frequency vs. R4 (see fig 5).

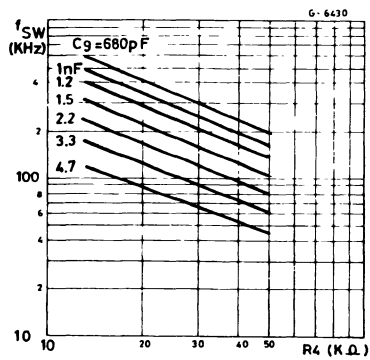


Figure 19 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 7C).

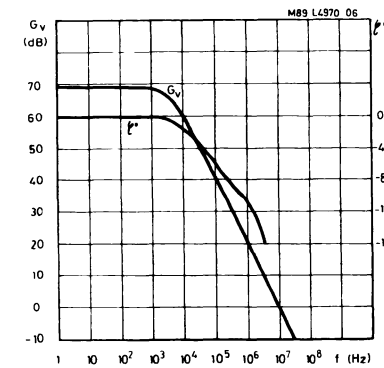


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

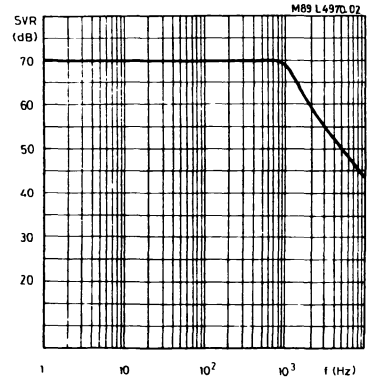


Figure 21 : Line Transient Response (see fig. 5).

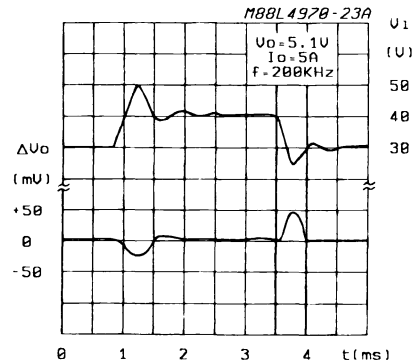


Figure 22 : Load Transient Response (see fig. 5).

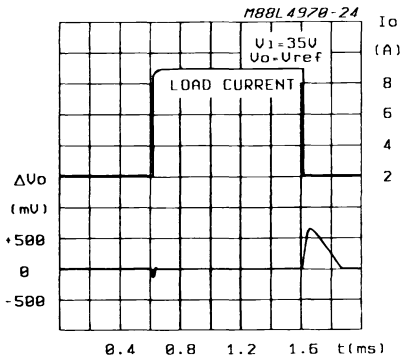


Figure 23 : Dropout Voltage between Pin 9 and Pin 7 vs. Current at Pin 7.

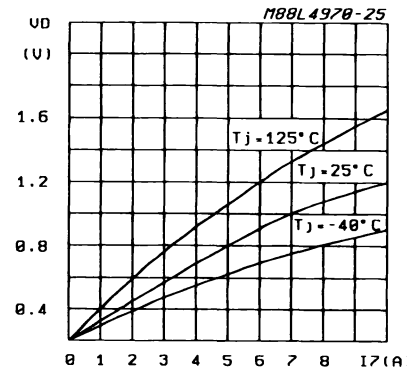


Figure 24 : Dropout Voltage between Pin 9 and Pin 7 vs. Junction Temperature.

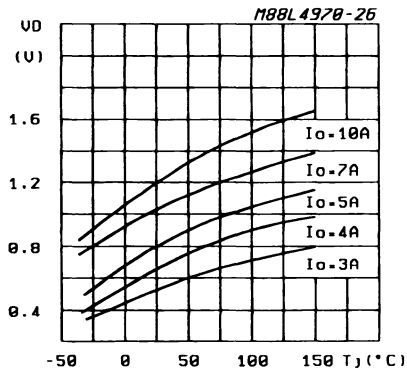


Figure 25 : Power Dissipation (device only) vs. Output Voltage.

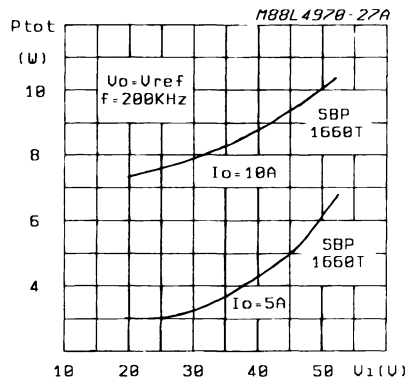


Figure 26 : Power Dissipation (device only) vs. Output Voltage.

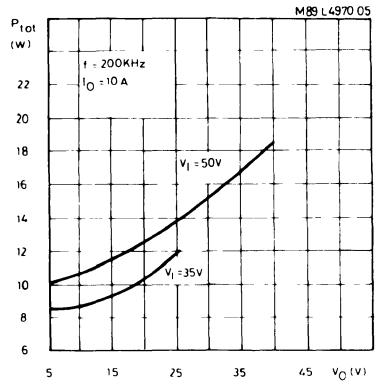


Figure 27 : Heatsink Used to Derive theDevice's Power Dissipation.

$$(R_{th-heatsink} = \frac{T_{case} - T_{amb}}{P_d})$$

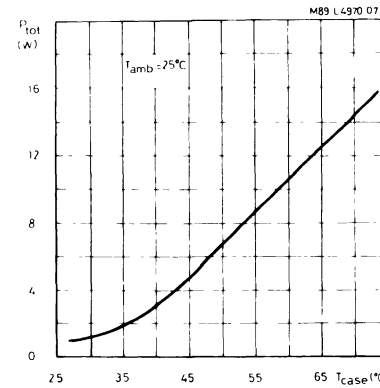


Figure 28 : Efficiency vs Output Current.

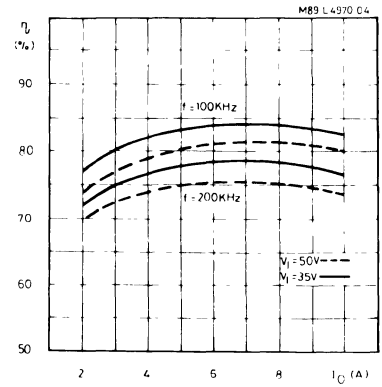


Figure 29 : Efficiency vs. Output Voltage

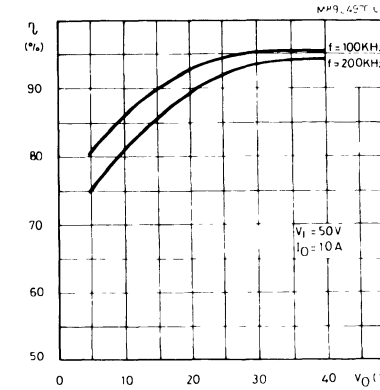


Figure 30 : Efficiency vs. Output Voltage.

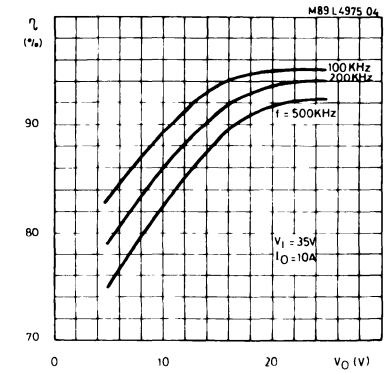


Figure 31 : Power Dissipation Derating Curve.

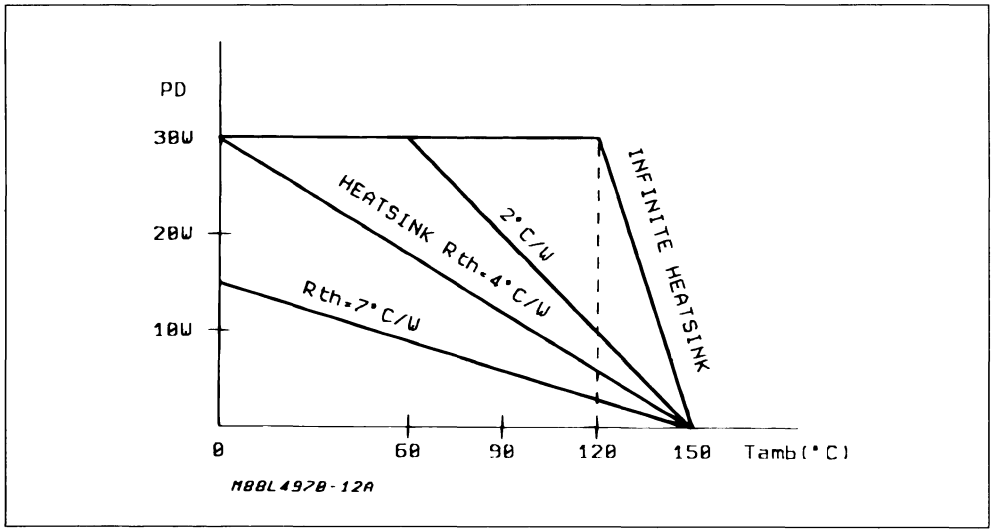
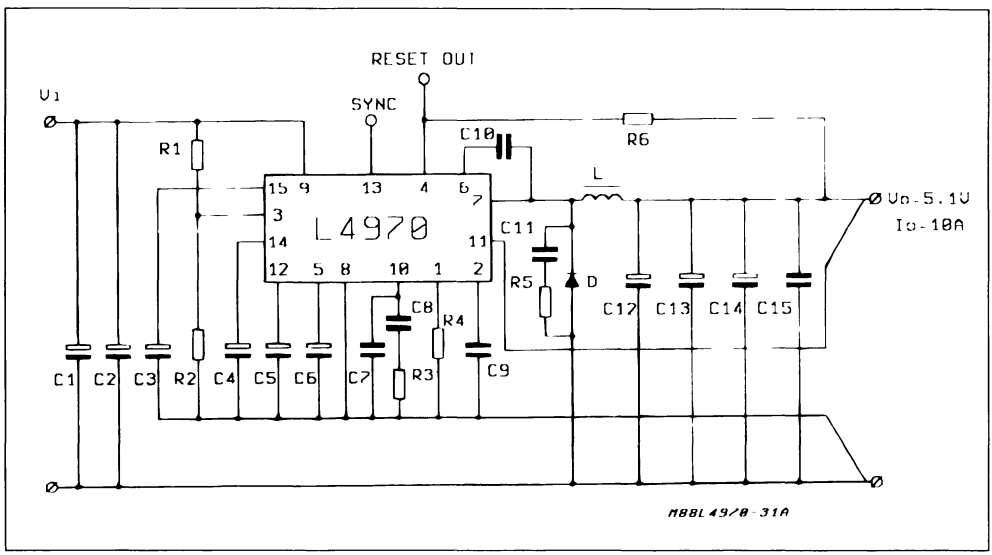


Figure 32 : 10A - 5.1V Application Circuit.



TYPICAL PERFORMANCES :

n = 83% (V_I = 35V ; V_o = V_{REF} ; I_o = 10A ; f_{SW} = 200KHz)

$V_{o\ RIPPLE}$ = 30mV (at 10A)

Line regulation = 5mV (V_I = 15 to 50V)

Load regulation = 15mV (I_o = 2 to 10A)

For component values, refer to test circuit part list.

Figure 33 : 5.1V / 10A Low Cost Application (for component values refer to the test circuit part list).

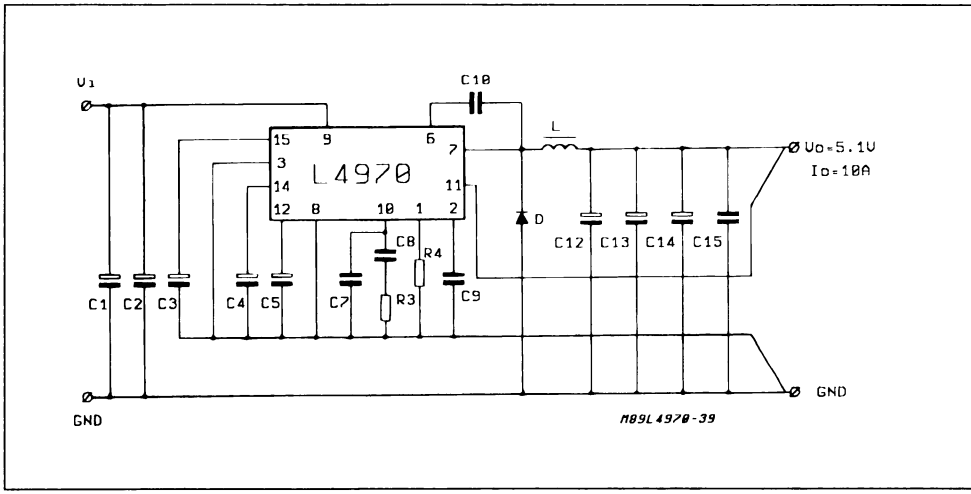


Figure 34 : 5.1V / 12V Multiple Supply. Note the Synchronization between the L4970 and the L4974.

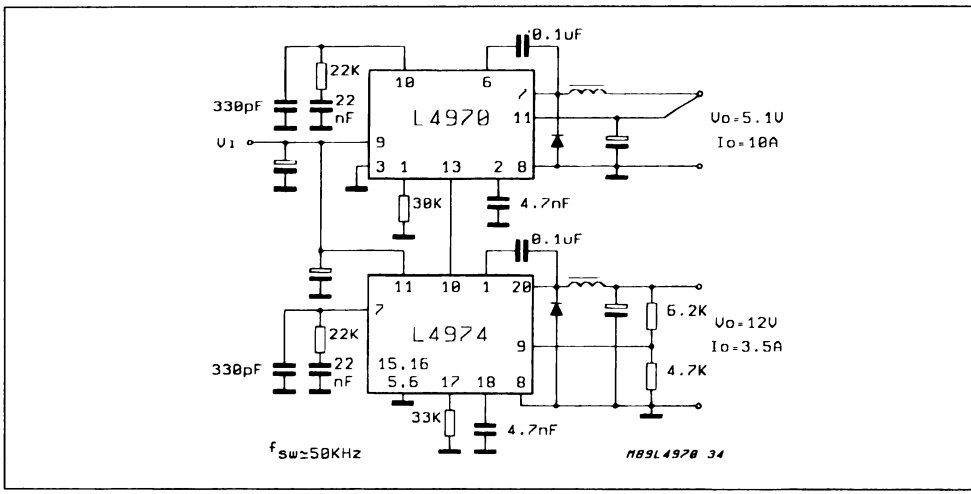


Figure 35 : L4970's Sync. Example.

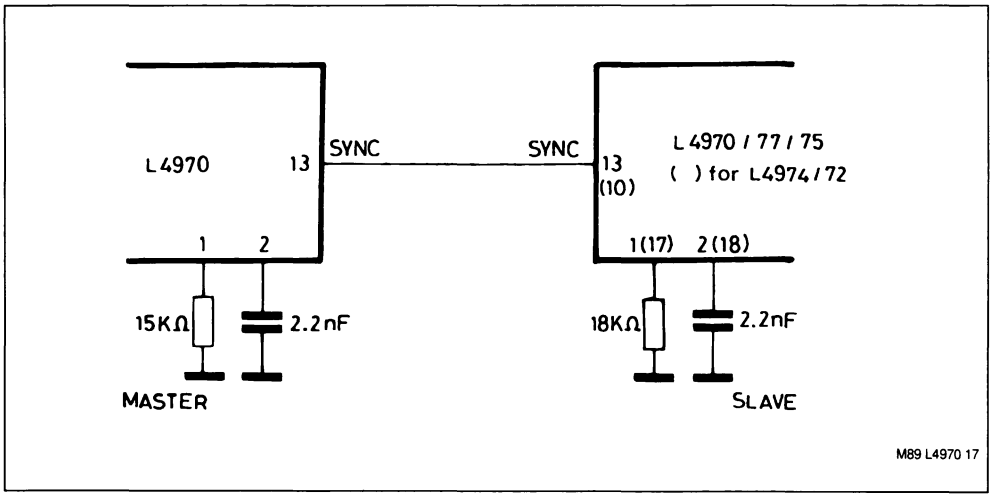
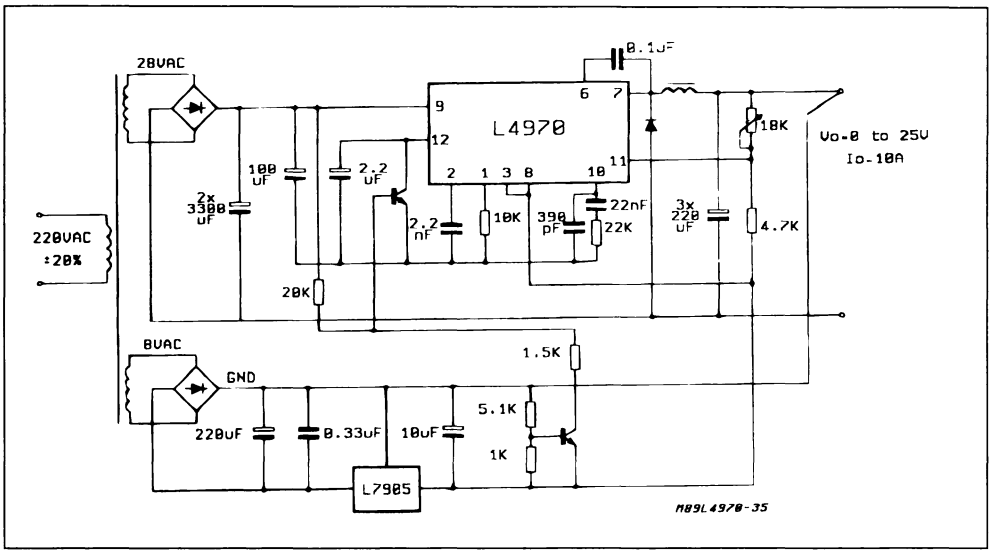


Figure 36 : 10A Switching Regulator, Adjustable from 0V to 25V.

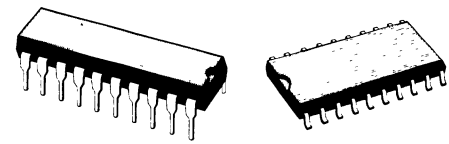


3.5A SWITCHING REGULATOR

ADVANCE DATA

- 2A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHz
- THERMAL SHUTDOWN

MULTIPOWER BCD TECHNOLOGY



POWERDIP (16 + 2 + 2)

SO20L

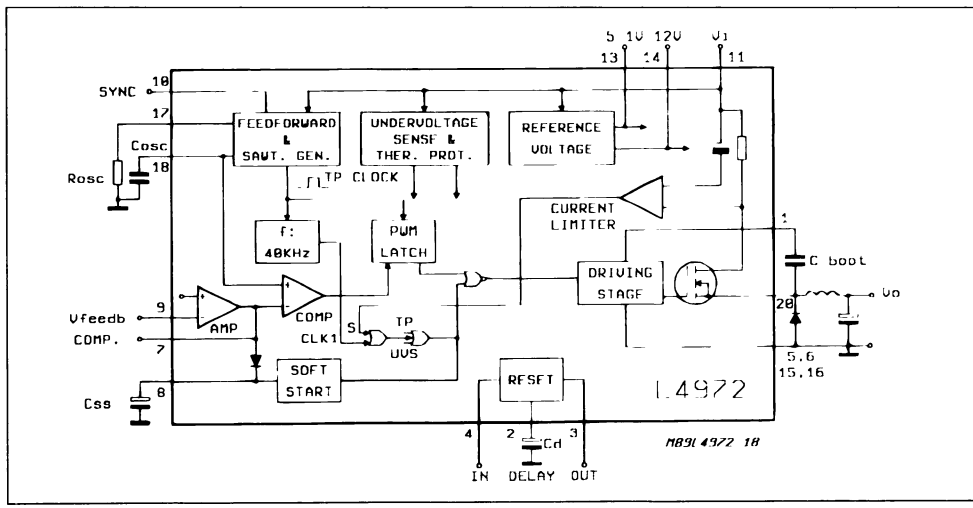
ORDER CODE : L4972 (Powerdip)
L4972D (SO20L)

DESCRIPTION

The L4972 is a stepdown monolithic power switching regulator delivering 2A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4972 include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 and SO20 large plastic packages and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

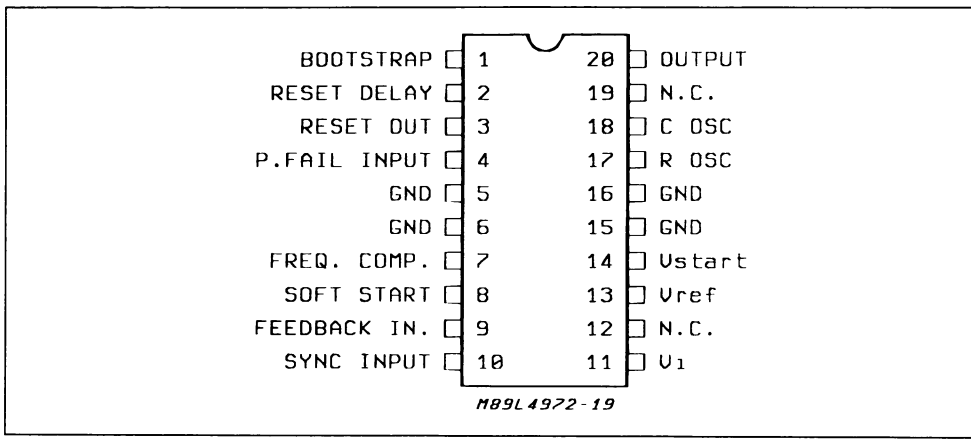
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{11}	Input Voltage	55	V
V_{11}	Input Operating Voltage	50	V
V_{20}	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	– 1 – 5	V V
I_{20}	Maximum Output Current	Internally Limited	
V_1	Bootstrap Voltage Bootstrap Operating Voltage	65 V_{11} + 15	V V
V_4, V_8	Input Voltage at Pins 4, 12	12	V
V_3	Reset Output Voltage	50	V
I_3	Reset Output Sink Current	50	mA
V_2, V_7, V_9, V_{10}	Input Voltage at Pin 2, 7, 9, 10	7	V
I_2	Reset Delay Sink Current	30	mA
I_7	Error Amplifier Output Sink Current	1	mA
I_8	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{PINS} < 80°C	5	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

			Powerdip	SO20L
Rth j–pins	Thermal Resistance Junction–pins	Max	12°C/W	15°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	80°C/W	–

PIN FUNCTIONS

N°	Name	Function
1	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
2	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
3	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
4	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 with an external 30KΩ resistor when power fail signal not required.
5, 6 15, 16	GROUND	Common Ground Terminal
7	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
8	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant.
9	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
10	SYNC INPUT	Multiple L4972's are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
11	SUPPLY VOLTAGE	Unregulated Input Voltage
12, 19	N. C.	
13	V_{ref}	5.1 V_{ref} Device Reference Voltage
14	V_{start}	Internal Start-up Circuit to Drive the Power Stage
17	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
18	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
20	OUTPUT	Regulator Output

CIRCUIT OPERATION

The L4972 is a 2A monolithic stepdown switching regulator realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 2A at an output voltage adjustable from 5.1V to 40V and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistors and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold porvides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charge to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 200kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate frixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments.

The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on, output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor, Css, and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold, the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator, will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz. The Reset and Power fail circuit (fig. 4), generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V, the reset output goes low immediately. The reset output is an open drain.

Fig. 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V, but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has a hysterysis to prevent unstable conditions.

Figure 1 : Feedforward Waveform.

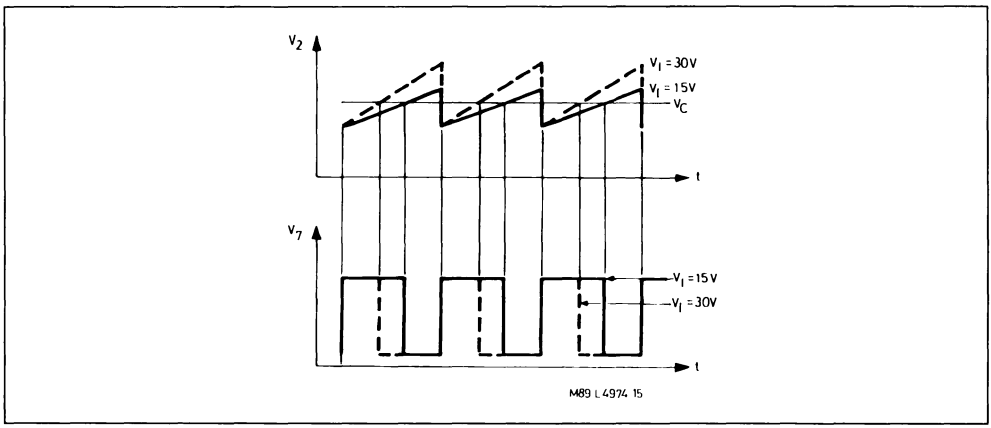


Figure 2 : Soft Start Function.

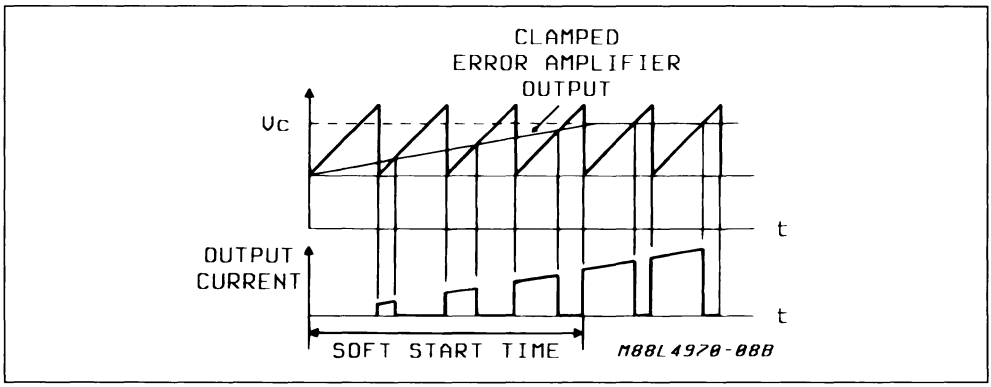


Figure 3 : Limiting Current Function.

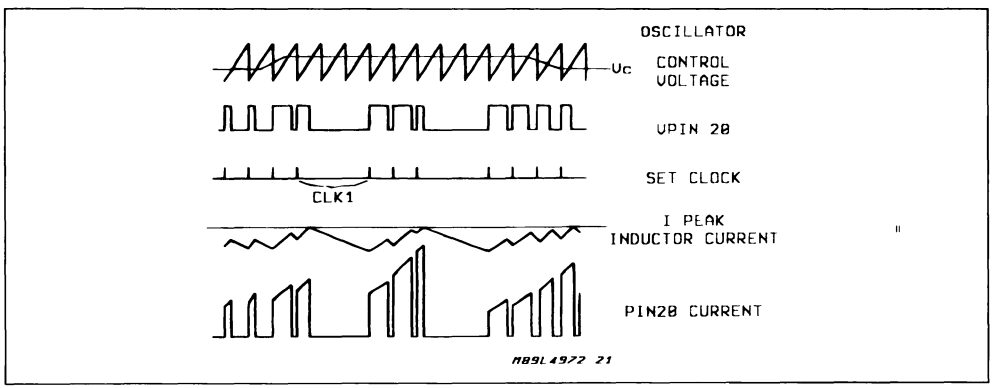
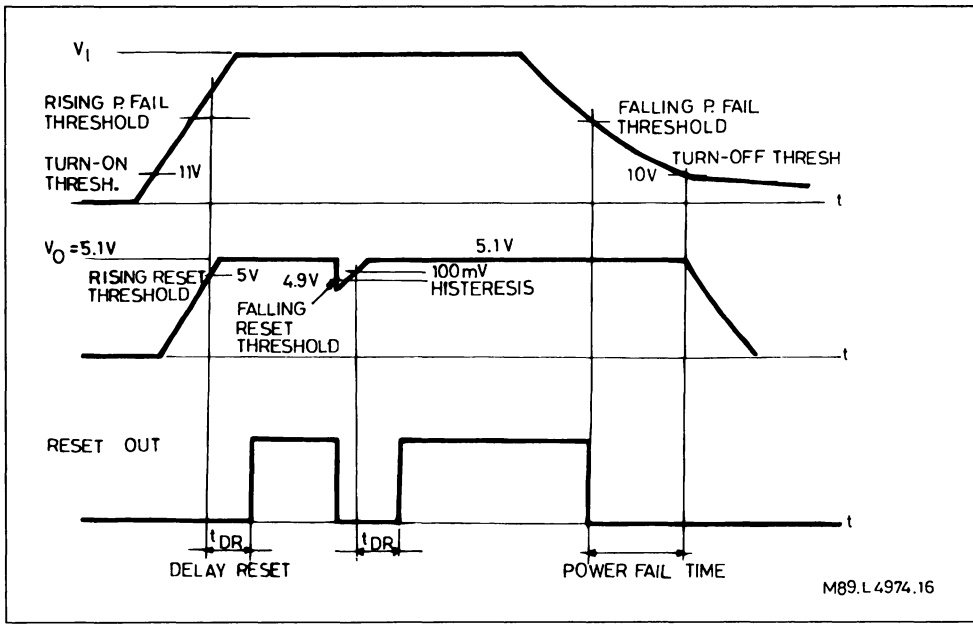
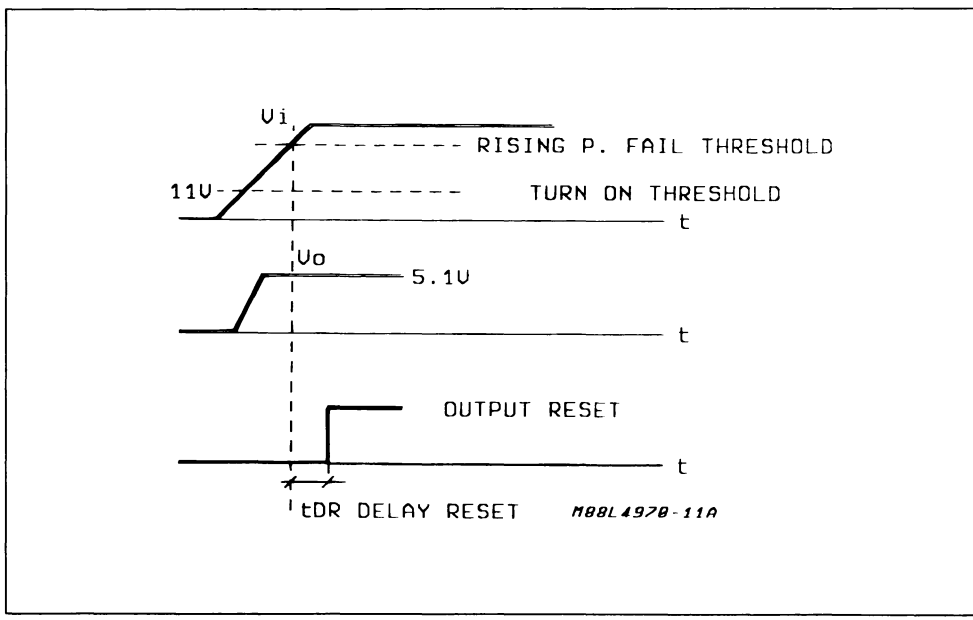


Figure 4 : Reset and Power Fail Functions.

A



B



ELECTRICAL CHARACTERISTICS(refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 33KΩ, C_9 = 2.2nF, f_w = 100KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 11)	V_o = V_{ref} to 40V I_o = 2A	15		50	V	5
V_o	Output Voltage	V_i = 15V to 50V I_o = 1A ; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 0.5A ; V_o = V_{ref}		12	30	mV	
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 0.5A to 2A		7	20	mV	
V_d	Dropout Voltage between Pin 11 and 20	I_o = 2A		0.25	0.4	V	
I_{20L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	2.5	2.8	3.1	A	
η	Efficiency	I_o = 2A, f = 100kHz V_o = V_{ref} V_o = 12V	80	85 90		%	
SVR	Supply Voltage Ripple Rejection	V_i = 2VRMS ; I_o = 1A f = 100Hz ; V_o = V_{ref}	56	60		dB	5
f	Switching Freq.		90	100	110	kHz	5
$\Delta f/\Delta V_i$	Volt. Stability of Switching Freq.	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temp. Stability of Switch. Freq.	T_j = 0 to 125°C		1		%	5
f_{max}	Max. Operating Switch. Freq.	V_o = V_{ref} R_4 = 15kΩ I_o = 2A C_9 = 2.2nF	200			kHz	5

V_{REF} SECTION (pin 13)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{REF}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{REF}	Line Regulation	V_i = 15V to 50V V_8 = 0		10	25	mV	7
ΔV_{REF}	Load Regulation	I_{REF} = 0 to 3mA		20	40	mV	7
$\Delta V_{REF}/\Delta T$	Average Temp. Coeff. Ref. Voltage	T_j = 0°C to 125°C		0.4		mV/C	7
I_{REF}	Short Circuit Curr. Limit	V_{REF} = 0		70		mA	7

V_{START} SECTION (pin 14)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{ref}	Reference Voltage	P_8 = 0V	11.4	12	12.6	V	7
ΔV_{ref}	Line Regulation	P_8 = 0V ; V_i = 15 to 50V		0.4	1	V	7
ΔV_{ref}	Load Regulation	I_{ref} = 0 to 1mA P_8 = 0V		50	200	mV	7
I_{ref}	Short Circuit Curr. Limit	P_8 = 0V ; P_{14} = 0V		80		mA	

ELECTRICAL CHARACTERISTICS (continued)

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{11on}	Turn–on Thresh		10	11	12	V	7A
V_{11Hyst}	Turn–off Hyster.			1		V	7A
I_{11Q}	Quiescent Current	$V_8 = 0$, S1 = D S2 = C , S4 = A		10	16	mA	7A
I_{11OQ}	Operating Quiescent Curr.	$V_8 = 0$		16	20	mA	7A
I_{20L}	Out Leak Current	$V_I = 55V$, S3 = A , $V_8 = 0V$,			2	mA	7A

SOFT START (pin 8)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_8	Soft Start Source Current	$V_8 = 3V$, $V_9 = 0V$	70	100	130	µA	7B
V_{8s}	Output Saturation Voltage	$I_{8s} = 20mA$, $V_{11} = 10V$			0 7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{7H}	High Level out Voltage	$I_7 = -50\mu A$; S2 = A $P_9 = 0V$, S1 = C	6			V	7C
V_{7L}	Low Level out Voltage	$I_7 = 50\mu A$, S2 = A $P_9 = 6V$, S1 = C			0 7	V	7C
I_9	Input Bias Current	$V_9 = 5V$, S1 = B , $R_S = 10K\Omega$		2	10	µA	7C
VOS	Input off Voltage	$P_9 = Vos$, $R_S = 50\Omega$, S1 = A		2	10	mV	7C
G_V	DC Open Loop Gain	$P_{VCM} = 4V$; $R_S = 50\Omega$, S1 = A	60			dB	7C
SVR	Supply Volt. Rejec	$15 < V_I < 50V$	60	80		dB	7C

ELECTRICAL CHARACTERISTICS (continued)

RAMP GENERATOR (pin 18)

Symbol	Parameter	Test Conditions	Min.	Typ.	max.	Unit	Fig.
	Ramp Valley			1 5		V	7A
	Ramp Peak	V_I = 15V V_I = 45V		2.5 5 5		V V	7A
	Min Ramp Current	S1 = A ; I_{17} = 100µA		270	300	µA	7A
	Max Ramp Current	S1 = A ; I_{17} = 1mA	2 4	2.7		mA	7A

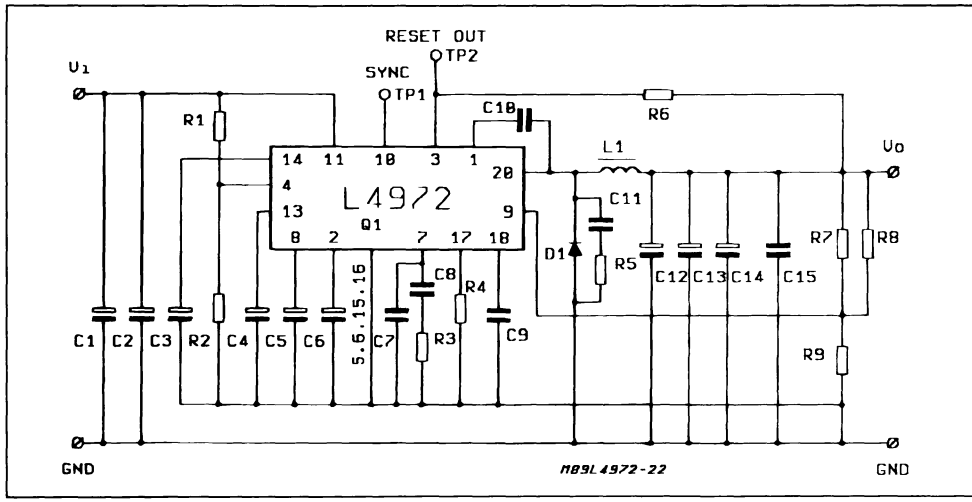
SYNC FUNCTION (pin 10)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYNC	Low Input Voltage	V_I = 15 to 50V	– 0 3		0 9	V	
SYNC	High Input Voltage	V_8 = 0	2 5		5 5	V	
$-I_{10L}$	Sync Input Current with Low Input Voltage	V_{10} = 0 9V			0 4	mA	
$-I_{10H}$	Input Current with High	V_{10} = 2 5V			1.5	mA	
SYNC	Delay			50		ns	
	Output Amplitude		4	5		V	
	Output Pulse Width	V_{thr} = 2 5V	0.3	0 5	0.8	µs	

RESET AND POWER FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9R}	Rising Threshold Voltage (pin 9)	V_I = 15 to 50V S1 = B	Vref – 120	Vref – 100	Vref – 80	V mV	7D
V_{9F}	Falling Threshold Voltage (pin 9)		4 77	Vref –200	Vref –160	V mV	7D
V_{2H}	Delay High Threshold Voltage	S1 = B	5	5.1	5 2	V	7D
V_{2L}	Delay Low Threshold Voltage	S1 = B	1	1.1	1.2	V	7D
I_{2SO}	Delay Source Current	V_4 = 5 3V , V_2 = 3V S1 = A	40	56	70	µA	7D
I_{2SI}	Delay SINK Current	V_4 = 4.7V ; V_2 = 3V S1 = A	10			mA	7D
V_{3S}	Out Saturation Voltage	I_3 = 15mA , S2 = B			0.4	V	7D
I_3	Output Leak Current	V_3 = 50V , S2 = A			100	µA	7D
V_{4S}	Rising Threshold Voltage		5	5.1	5.2	V	7D
	Hysteresis		0 4	0.5	0.6	V	7D
I_4	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Application Circuit.



PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 22K
R_4 = 36K
R_5 = 22Ω
R_6 = 4.7K
R_7 = see table A
R_8 = OPTION
R_9 = 4.7K

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 330pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.2nF KP 1830 (ERO)
C_{10} = 0.1µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film

D = SBS 560 (OR EQUIVALENT)

L = 150µH
core 58310 MAGNETICS
45 TURNS 0.8mm (AWG 19)
COGEMA 949181

* 2 capacitors in parallel to increase input RMS current capability.
** 3 capacitors in parallel to reduce total output ESR.

Table A.

V_0	R_9	R_7
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Figure 6 : Component Layout of fig.5 (1 : 1 scale). Evaluation Board Available.

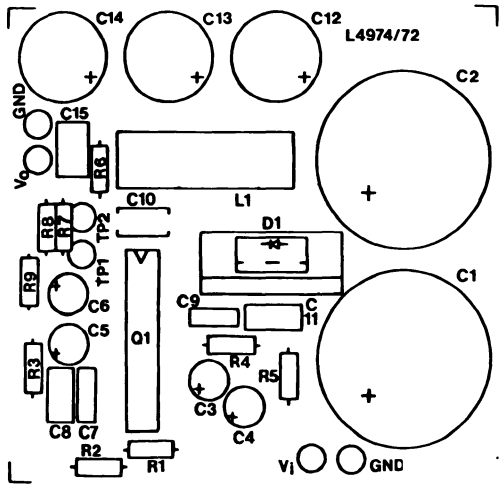


Figure 7 : DC Test Circuits.

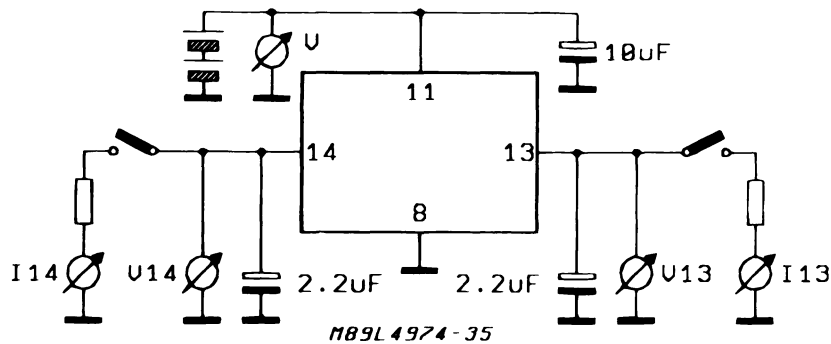


Figure 7A.

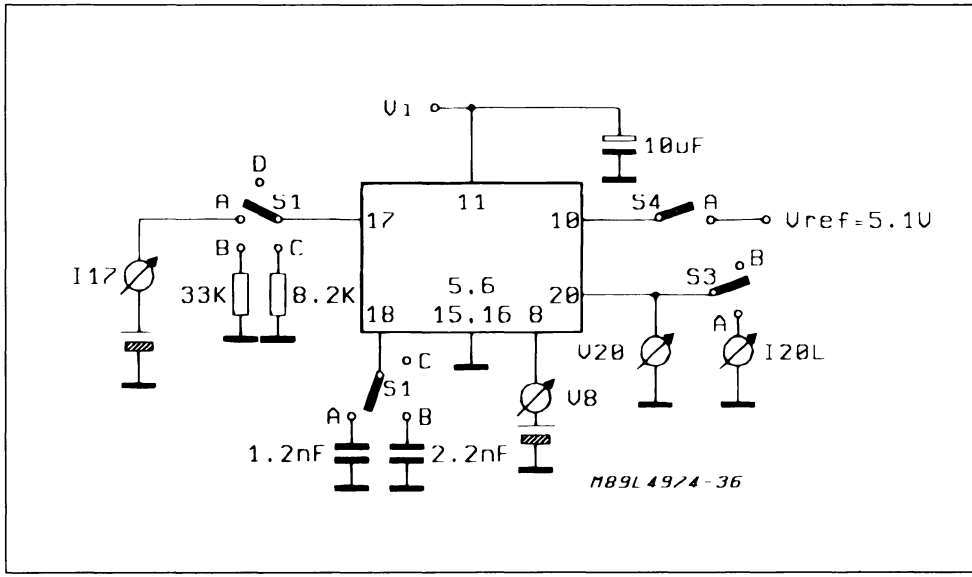


Figure 7B.

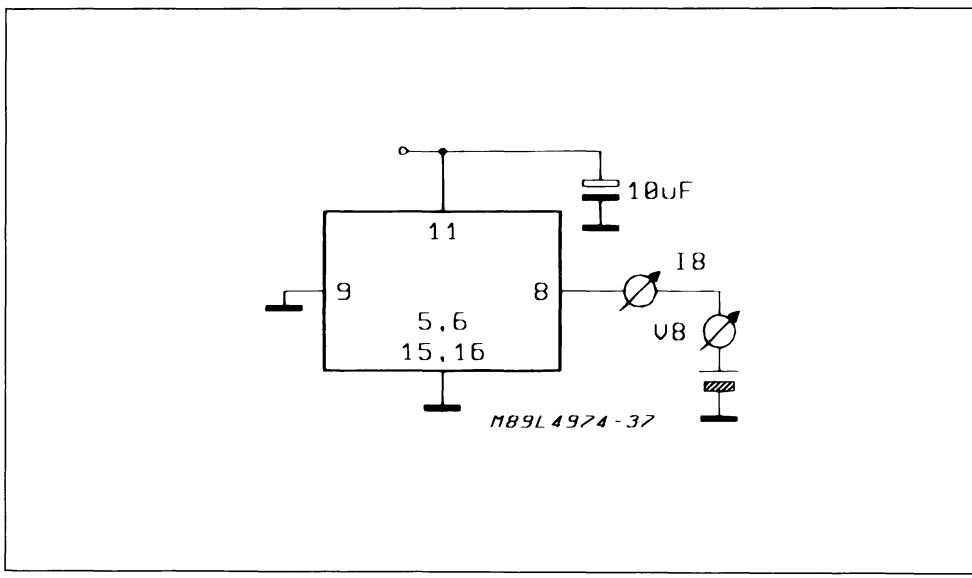


Figure 7C.

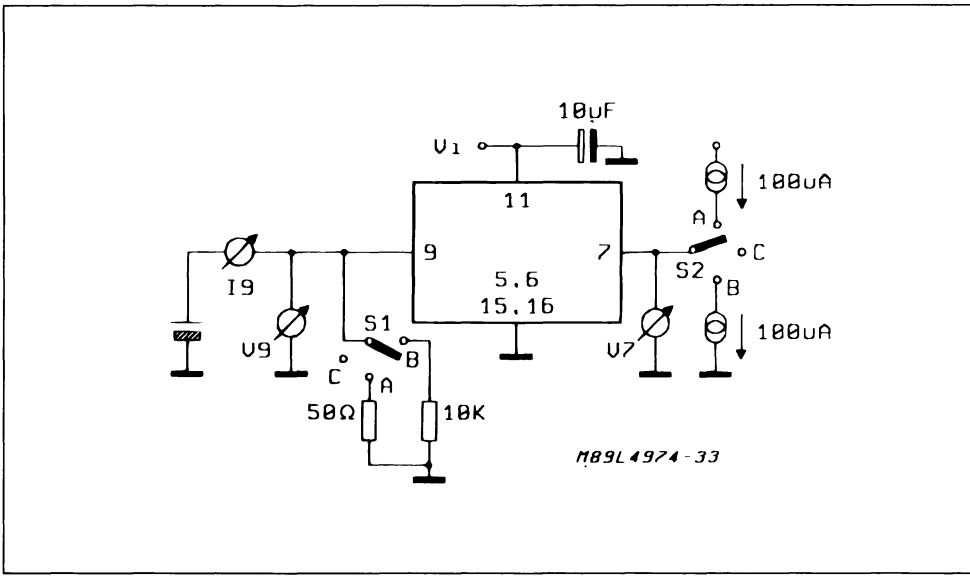


Figure 7D.

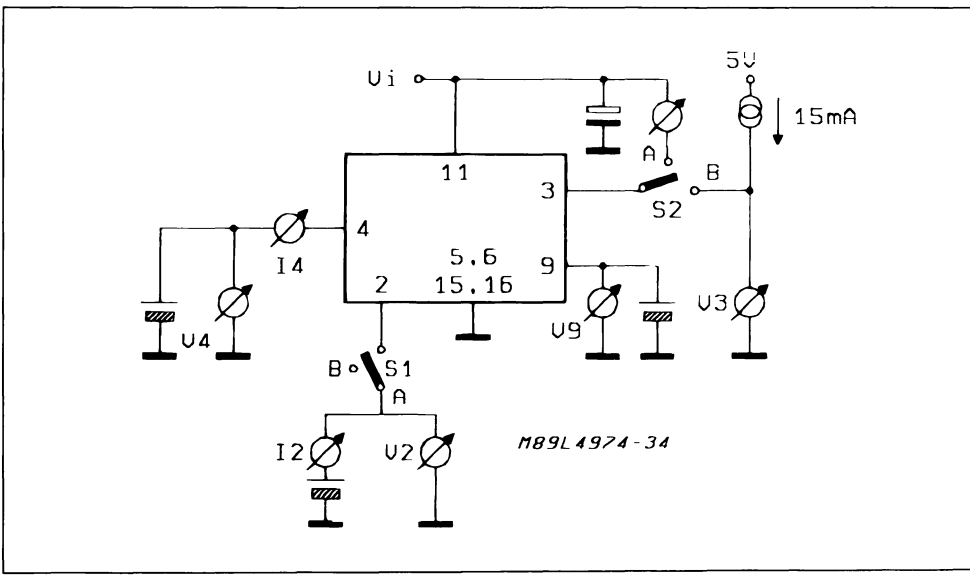


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

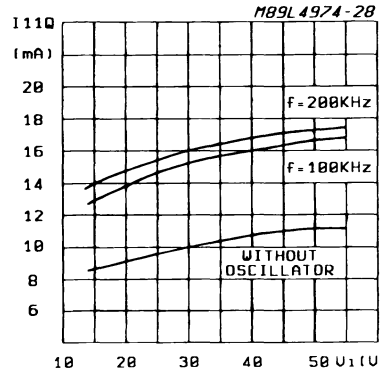


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

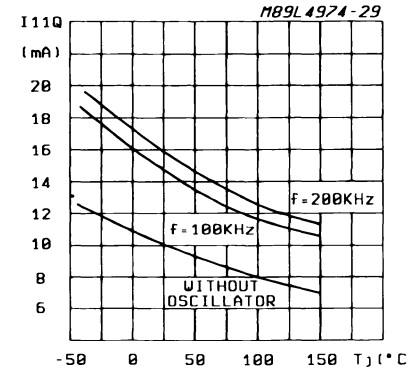


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

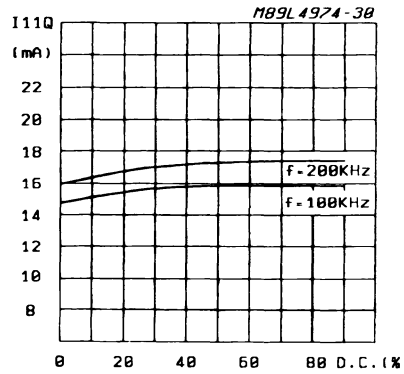


Figure 11 : Reference Voltage (pin 13) vs. Vi (see fig. 7).

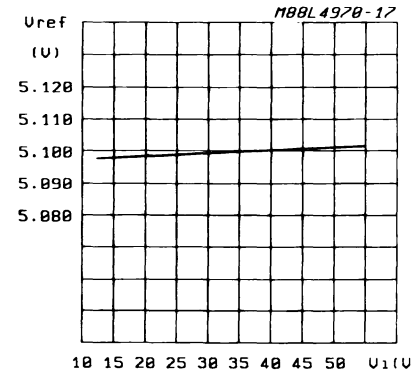


Figure 12 : Reference Voltage (pin 13) vs. Junction Temperature (see fig. 7).

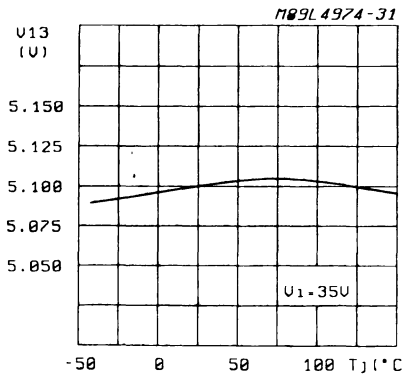


Figure 13 : Reference Voltage (pin 14) vs. Vi (see fig. 7).

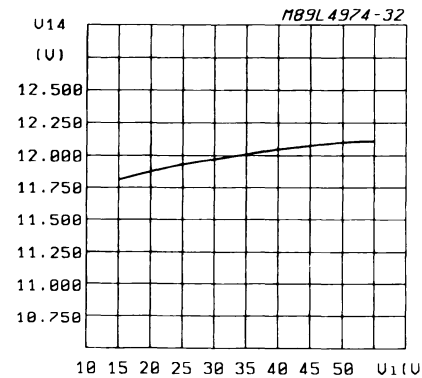


Figure 14 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

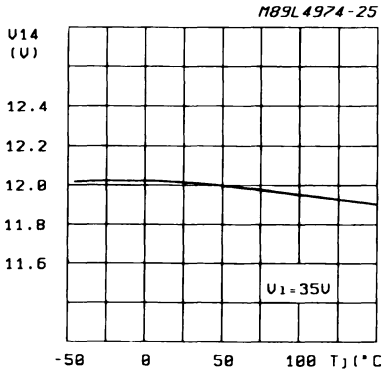


Figure 15 : Reference Voltage 5.1V (pin 13) Supply Voltage Ripple Rejection vs. Frequency.

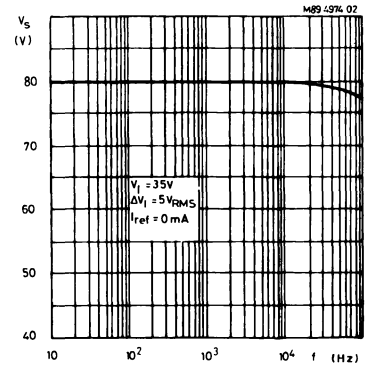


Figure 16 : Switching Frequency vs. Input Voltage (see fig. 5).

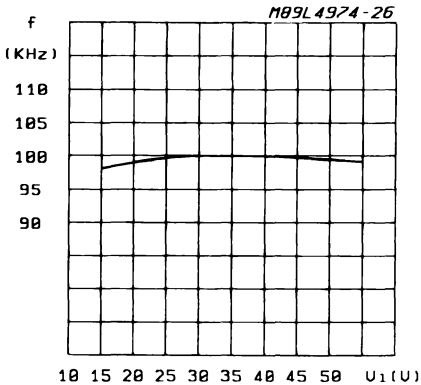


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

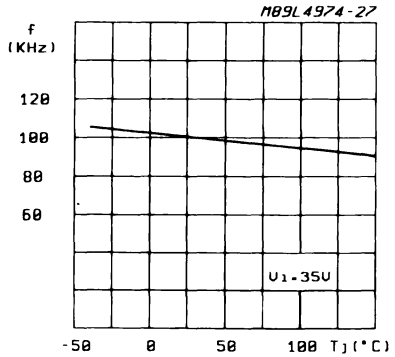


Figure 18 : Switching Frequency vs. R4 (see fig.5).

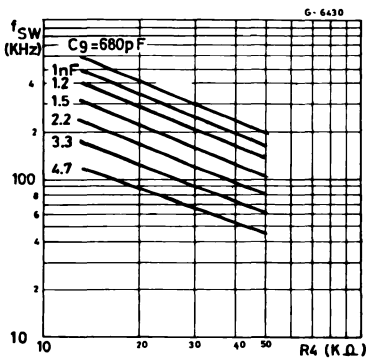


Figure 19 : Open Loop Frequency and Phase of Error Amplifier (see fig. 7C).

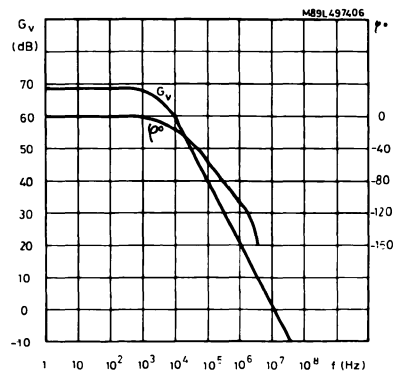


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

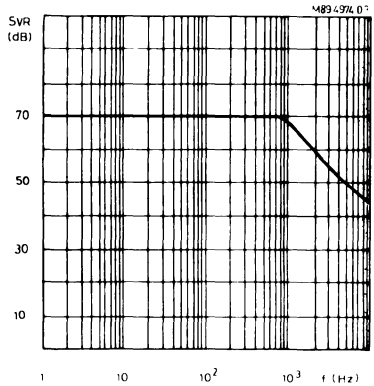


Figure 21 : Efficiency vs. Output Voltage.

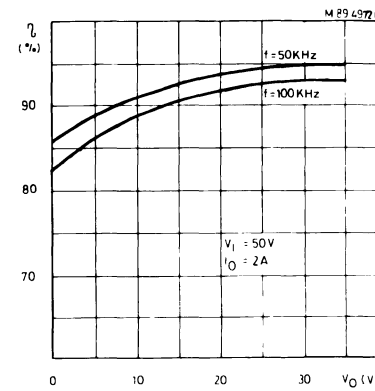


Figure 22 : Line Transient Response (see fig. 5).

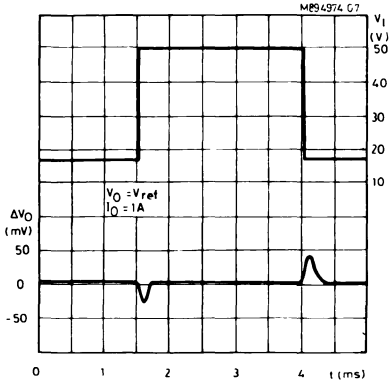


Figure 23 : Load Transient Response (see fig. 5).

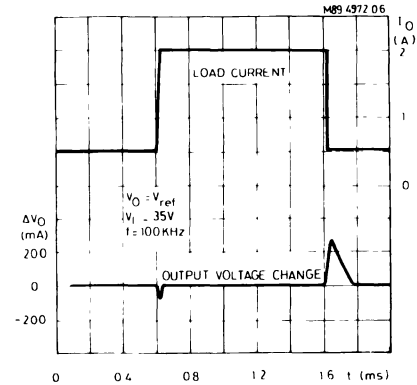


Figure 24 : Dropout Voltage between Pin 11 and Pin 20 vs. Current at Pin 20.

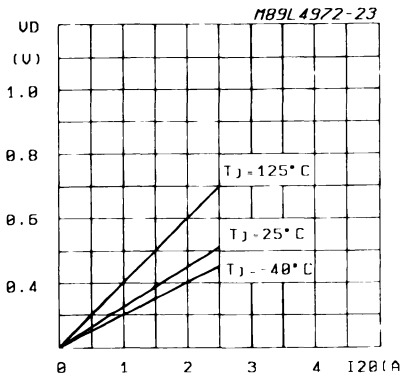


Figure 25 : .Dropout Voltage between Pin 11 and Pin 20 vs. Junction Temperature.

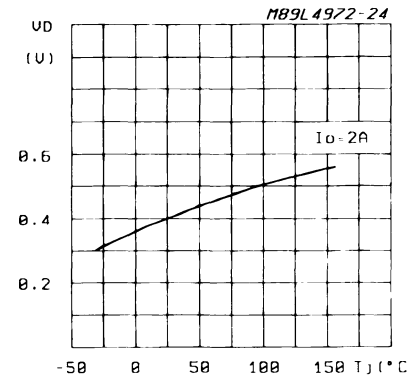


Figure 26 : Power Dissipation (device only) vs. Input Voltage.

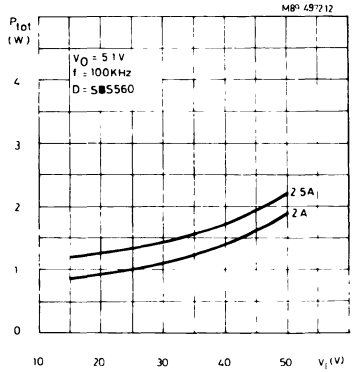


Figure 27 : Power Dissipation (device only) vs. Input Voltage.

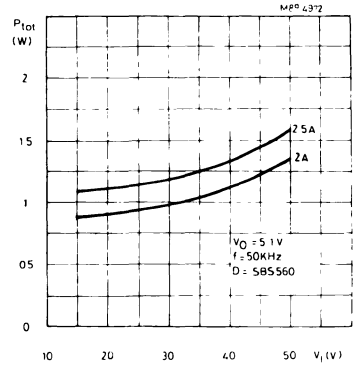


Figure 28 : Power Dissipation (device only) vs. Output Voltage.

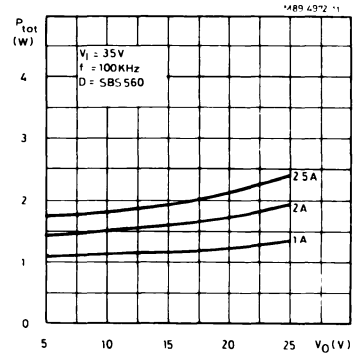


Figure 29 : Power Dissipation (device only) vs. Output Voltage.

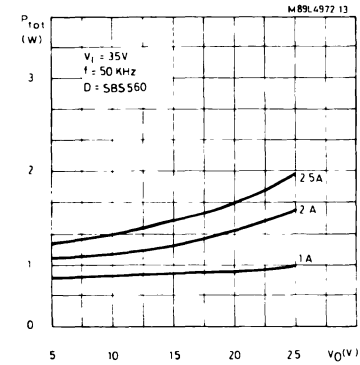


Figure 30 : Power Dissipation (device only) vs. Output Current.

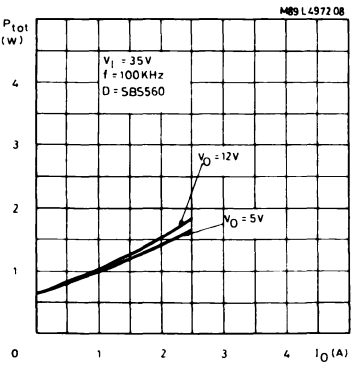


Figure 31 : Power Dissipation (device only) vs. Output Current.

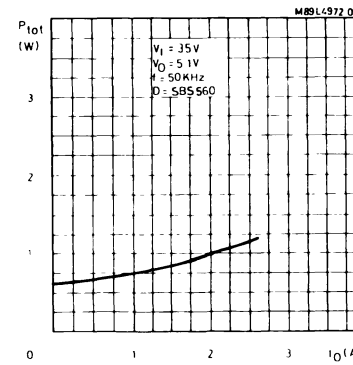


Figure 32 : Efficiency vs. Output Current.

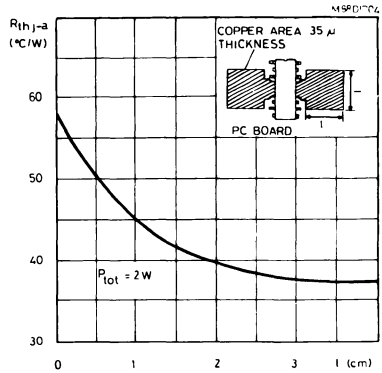


Figure 33 : Test PCB Thermal Characteristic.

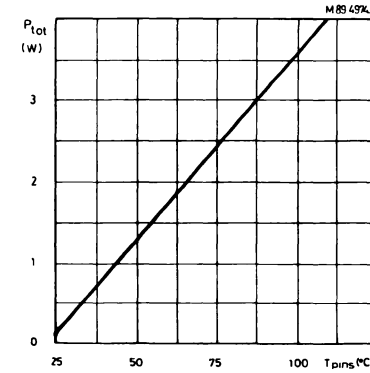


Figure 34 : R_{th} with two "on board" Square Heat Sinks vs. Side l.

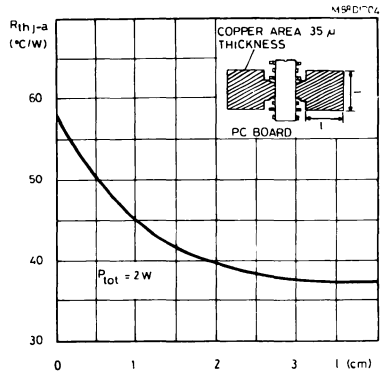
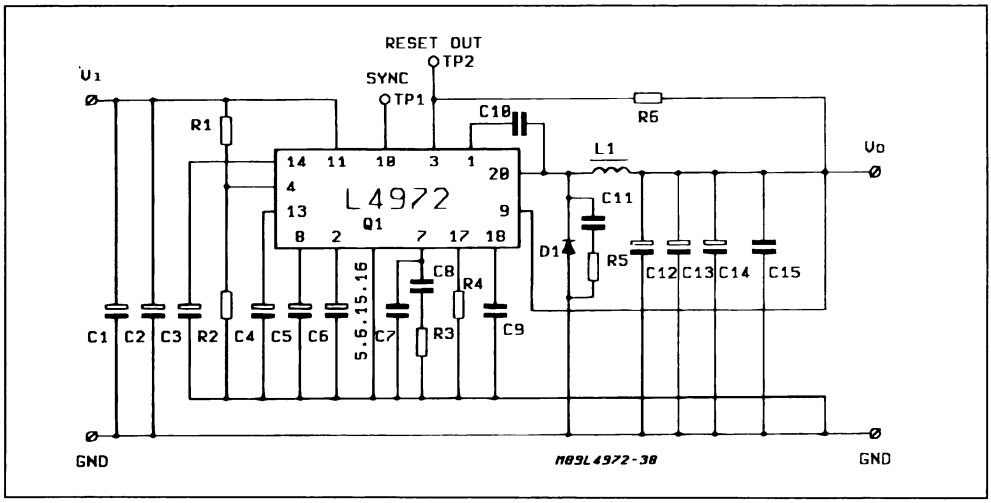


Figure 35 : 2A – 5.1V Application Circuit.



TYPICAL PERFORMANCE (using evaluation board) :

n = 83% (V_i = 35V ; V_o = VREF ; I_o = 2A ; f_{sw} = 100KHz)

$V_{o\ RIPPLE}$ = 30mV (at 1A)

Line regulation = 12mV (V_I = 15 to 50V)

Load regulation = 7mV (I_o = 0.5A, I_o = 0.5 – 2A)

for component values Refer to the fig. 5 (Part list).

Figure 36 : A 5.1V/12V Multiple Supply. Note the Synchronization between the L4972 and L4970.

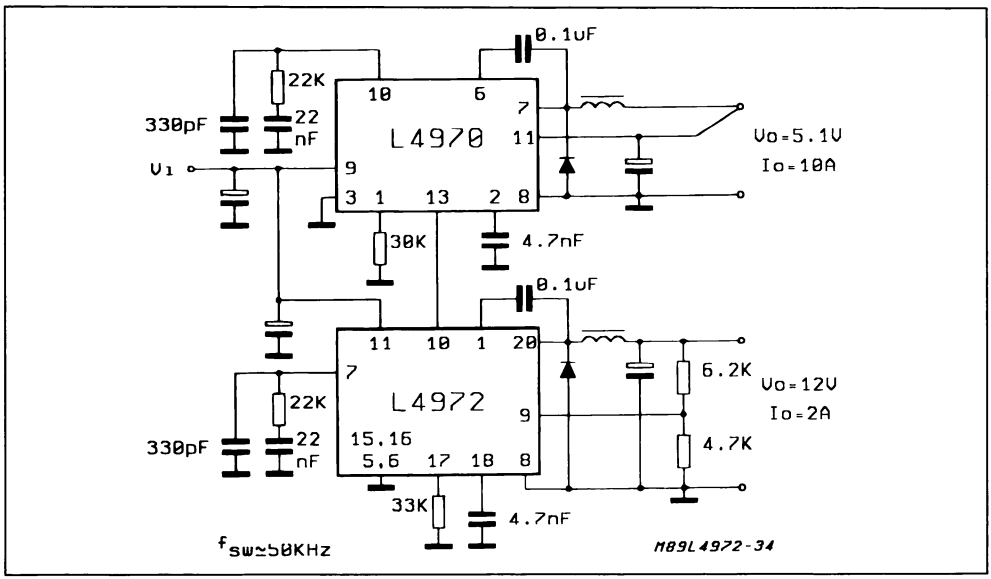
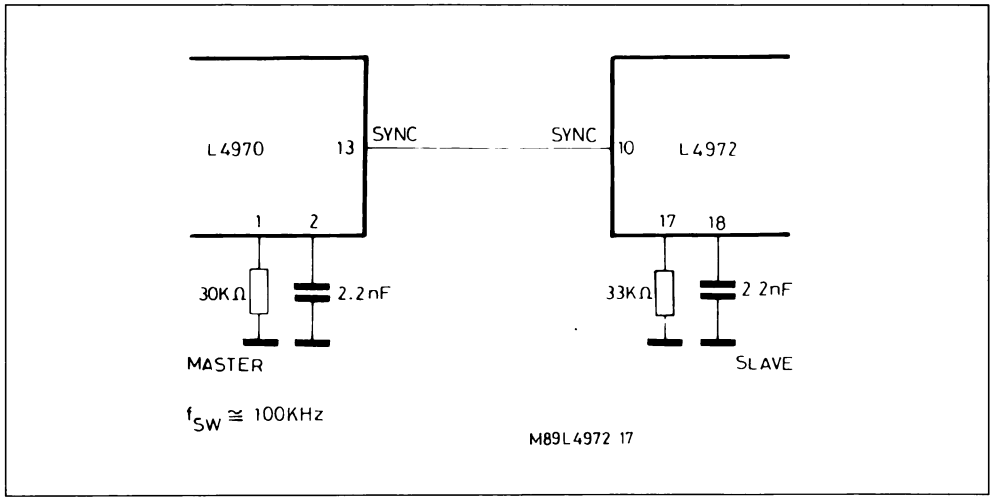


Figure 37 : L4972's Sync. Example.

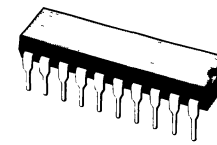


3.5A SWITCHING REGULATOR

ADVANCE DATA

- 3.5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REG.
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND POWER FAIL FUNCTIONS
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 200KHz
- THERMAL SHUTDOWN

MULTIPOWER BCD TECHNOLOGY



POWERDIP
(16 + 2 + 2)

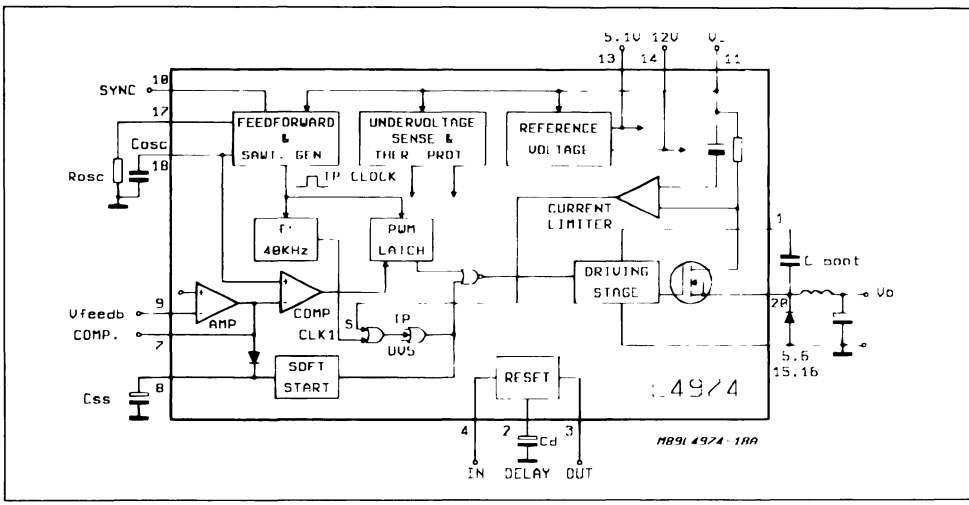
ORDER CODE : L4974

DESCRIPTION

The L4974 is a stepdown monolithic power switching regulator delivering 3.5A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching tmes. Features of the L4974 include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a Powerdip 16 + 2 + 2 plastic package and requires few external components. Efficient operation at switching frequencies up to 200KHz allows reduction in the size and cost of external filter component.

BLOCK DIAGRAM

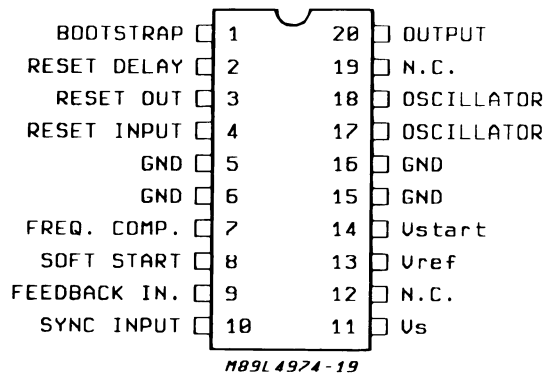


This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{11}	Input Voltage	55	V
V_{11}	Input Operating Voltage	50	V
V_{20}	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	– 1 – 7	V V
I_{20}	Maximum Output Current	Internally Limited	
V_1	Bootstrap Voltage Bootstrap Operating Voltage	65 V_{11} + 15	V V
V_4, V_8	Input Voltage at Pins 4, 12	12	V
V_3	Reset Output Voltage	50	V
I_3	Reset Output Sink Current	50	mA
V_2, V_7, V_9, V_{10}	Input Voltage at Pin 2, 7, 9, 10	7	V
I_2	Reset Delay Sink Current	30	mA
I_7	Error Amplifier Output Sink Current	1	mA
I_8	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{PINS} < 80°C	5	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

Rth j–pins	Thermal Resistance Junction–pins	Max	12	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	80	

PIN FUNCTIONS

N°	Name	Function
1	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
2	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
3	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe.
4	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 14 with an external 30KΩ resistor when power fail signal not required.
5, 6 15, 16	GROUND	Common Ground Terminal
7	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
8	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant.
9	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
10	SYNC INPUT	Multiple L4974's are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse.
11	SUPPLY VOLTAGE	Unregulated Input Voltage
12, 19	N. C.	
13	V_{ref}	5.1 V_{ref} Device Reference Voltage
14	V_{start}	Internal Start-up Circuit to Drive the Power Stage
17	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
18	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
20	OUTPUT	Regulator Output

CIRCUIT OPERATION

The L4974 is a 3.5A monolithic stepdown switching regulator realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 3.5A at an output voltage adjustable from 5.1V to 40V and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistors and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charge to 12V by an internal voltage reference is needed to provide correct gate frive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 200kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing

the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate frixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments.

The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on, output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor, Css, and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by a internal metal resistor connected to a comparator. When the load current exceeds a preset threshold, the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator, will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz. The Reset and Power fail circuit (fig. 4), generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V, the reset output goes low immediately. The reset output is an open drain.

Fig. 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V, but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150°C and has a hysterysis to prevent unstable conditions.

Figure 1 : Feedforward Waveform.

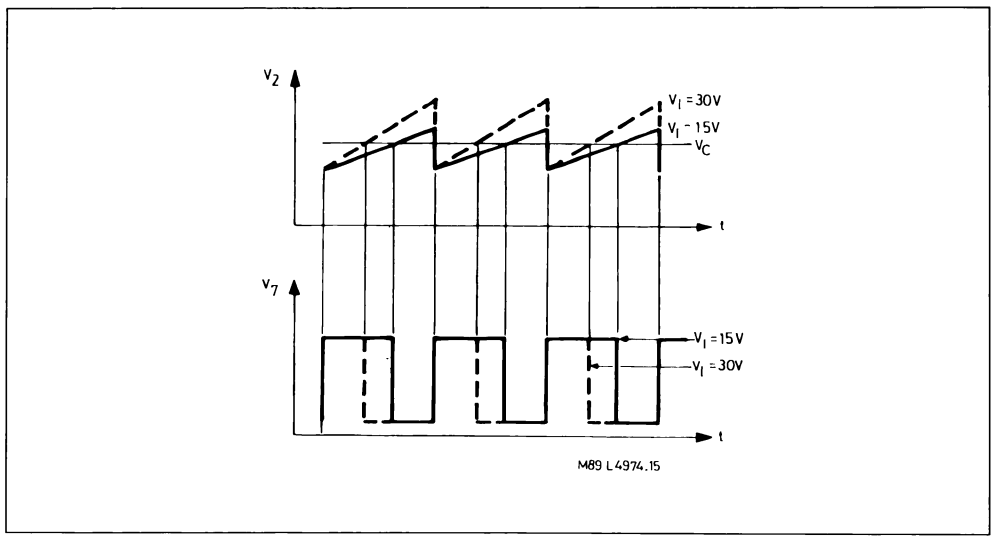


Figure 2 : Soft Start Function.

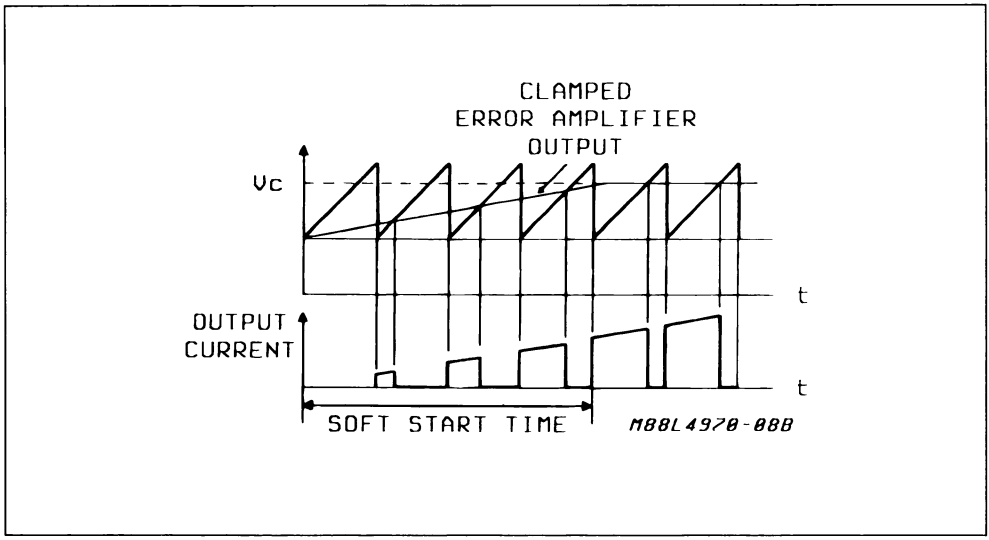


Figure 3 : Limiting Current Function.

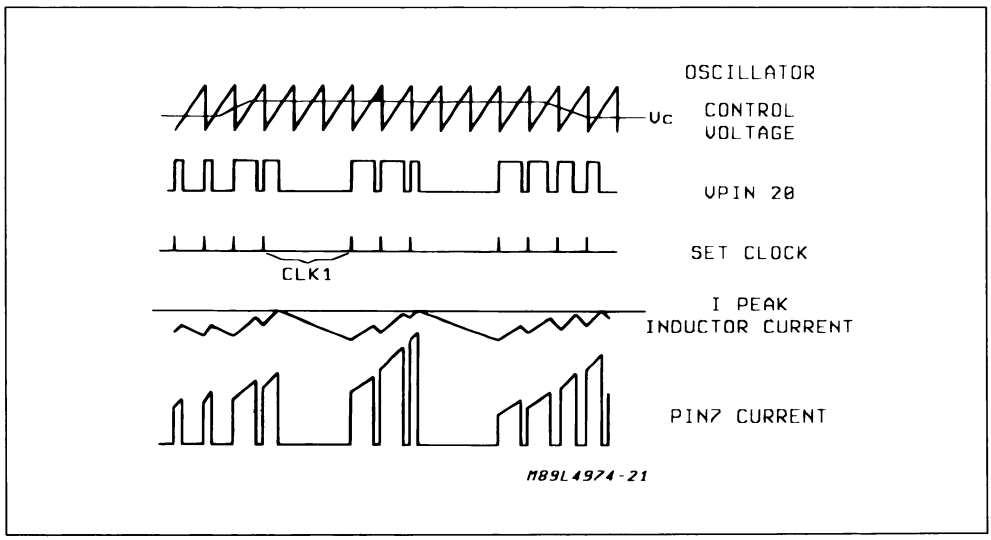
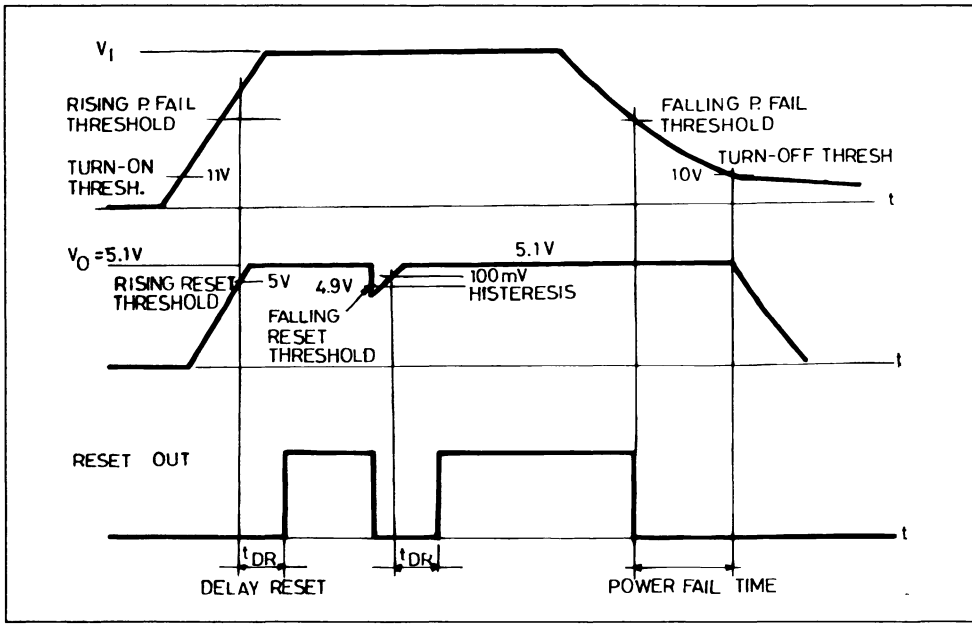
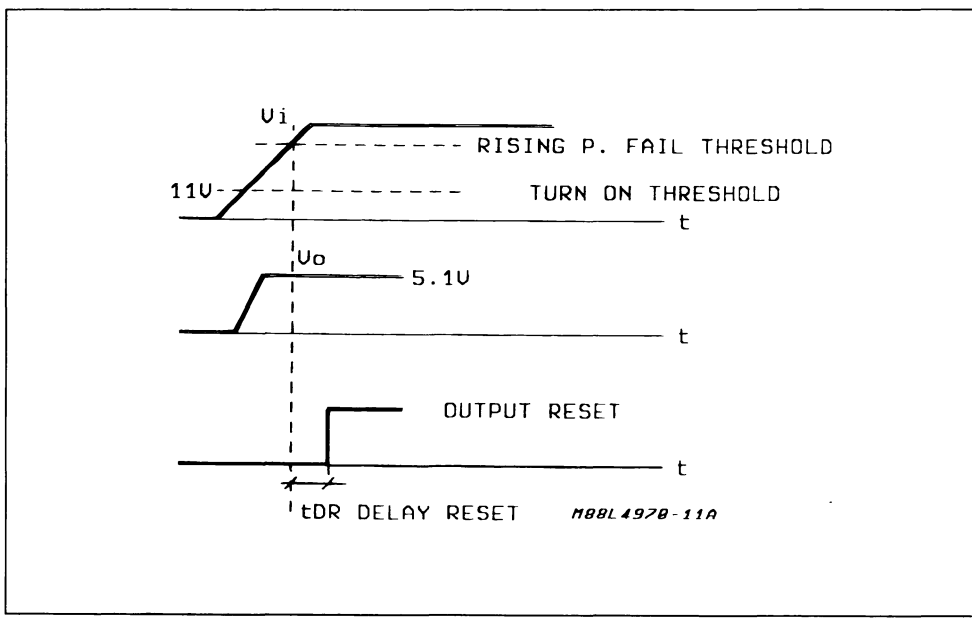


Figure 4 : Reset and Power Fail Functions.

A



B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 36KΩ, C_g = 2.2nF, f_w = 100KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 11)	V_o = V_{ref} to 40V I_o = 3.5A	15		50	V	5
V_o	Output Voltage	V_i = 15V to 50V I_o = 2A ; V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 1A ; V_o = V_{ref}		12	30	mV	
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 1A to 3.5A I_o = 2A to 3A		 8 4	 25 10	 mV mV	
V_d	Dropout Voltage between Pin 11 and 20	I_o = 2A I_o = 3.5A		0.25 0.45	0.4 0.7	V V	
I_{20L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	4	4.5	5	A	
η	Efficiency	I_o = 2A, f = 100kHz V_o = V_{ref} V_o = 12V	80	 85 90		 % %	
		I_o = 3.5A, f = 100kHz V_o = V_{ref} V_o = 12V	80	 85 90		 % %	
SVR	Supply Voltage Ripple Rejection	V_i = 2VRMS ; I_o = 5A f = 100Hz ; V_o = V_{ref}	56	60		dB	5
f	Switching Freq.		90	100	110	kHz	5
$\Delta f/\Delta V_i$	Volt. Stability of Switching Freq.	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temp. Stability of Switch. Freq.	T_j = 0 to 125°C		1		%	5
f_{max}	Max. Operating Switch. Freq.	V_o = V_{ref} R4 = 15KΩ I_o = 3.5A C_9 = 2.2nF	200			kHz	5

V_{REF} SECTION (pin 13)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{REF}	Reference Voltage		5	5.1	5.2	V	7
ΔV_{REF}	Line Regulation	V_i = 15V to 50V V_8 = 0		10	25	mV	7
ΔV_{REF}	Load Regulation	I_{REF} = 0 to 3mA		20	40	mV	7
$\Delta V_{REF}/\Delta T$	Average Temp. Coeff. Ref. Voltage	T_j = 0°C to 125°C		0.4		mV/C	7
I_{REF}	Short Circuit Curr. Limit	V_{REF} = 0		70		mA	7

ELECTRICAL CHARACTERISTICS (continued)

V_{START} SECTION (pin 14)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{ref}	Reference Voltage	P_8 = 0V	11 4	12	12 6	V	7
ΔV_{ref}	Line Regulation	P_8 = 0V , V_i = 15 to 50V		0.4	1	V	7
ΔV_{ref}	Load Regulation	I_{ref} = 0 to 1mA P_8 = 0V		50	200	mV	7
I_{ref}	Short Circuit Curr Limit	P_8 = 0V , P_{14} = 0V		80		mA	

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{11on}	Turn–on Thresh.		10	11	12	V	7A
V_{11Hyst}	Turn–off Hyster.			1		V	7A
I_{11Q}	Quiescent Current	V_8 = 0 , S1 = D S2 = C ; S4 = A		10	16	mA	7A
I_{11OQ}	Operating Quiescent Curr	V_8 = 0		16	20	mA	7A
I_{20L}	Out Leak Current	V_i = 55V ; S3 = A ; V_8 = 0V ;			2	mA	7A

SOFT START (pin 8)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_8	Soft Start Source Current	V_8 = 3V ; V_9 = 0V	70	100	130	µA	7B
V_{8s}	Output Saturation Voltage	I_{8s} = 20mA ; V_{11} = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{7H}	High Level out Voltage	I_7 = – 50µA , S2 = A P_9 = 0V ; S1 = C	6			V	7C
V_{7L}	Low Level out Voltage	I_7 = 50µA , S2 = A P_9 = 6V ; S1 = C			0.7	V	7C
I_9	Input Bias Current	V_9 = 5V ; S1 = B ; R_S = 10KΩ		2	10	µA	7C
VOS	Input off Voltage	P_9 = Vos ; R_S = 50Ω , S1 = A		2	10	mV	7C
G_V	DC Open Loop Gain	P_{VCM} = 4V ; R_S = 50Ω ; S1 = A	60			dB	7C
SVR	Supply Volt. Rejc.	15 < V_I < 50V	60	80		dB	7C

ELECTRICAL CHARACTERISTICS (continued)

RAMP GENERATOR (pin 18)

Symbol	Parameter	Test Conditions	Min.	Typ.	max.	Unit	Fig.
	Ramp Valley			1.5		V	7A
	Ramp Peak	V_i = 15V V_i = 45V		2.5 5.5		V V	7A
	Min Ramp Current	S1 = A ; I_{17} = 100µA		270	300	µA	7A
	Max Ramp Current	S1 = A ; I_{17} = 1mA	2.4	2.7		mA	7A

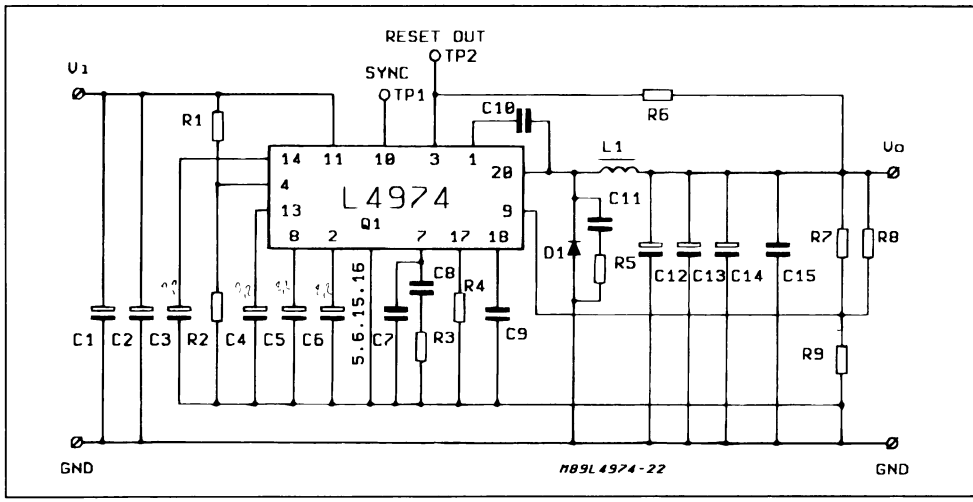
SYNC FUNCTION (pin 10)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYNC	Low Input Voltage	V_i = 15 to 50V	– 0.3		0 9	V	
SYNC	High Input Voltage	V_8 = 0	2 5		5 5	V	
$-I_{10L}$	Sync Input Current with Low Input Voltage	V_{10} = 0.9V			0.4	mA	
$-I_{10H}$	Input Current with High	V_{10} = 2.5V			1.5	mA	
SYNC	Delay			50		ns	
	Output Amplitude		4	5		V	
	Output Pulse Width	V_{thr} = 2.5V	0.3	0.5	0 8	µs	

RESET AND POWER FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9R}	Rising Threshold Voltage (pin 9)	V_i = 15 to 50V S1 = B	Vref – 120	Vref – 100	Vref – 80	V mV	7D
V_{9F}	Falling Threshold Voltage (pin 9)		4.77	Vref –200	Vref –160	V mV	7D
V_{2H}	Delay High Threshold Voltage	S1 = B	5	5.1	5.2	V	7D
V_{2L}	Delay Low Threshold Voltage	S1 = B	1	1.1	1.2	V	7D
I_{2SO}	Delay Source Current	V_4 = 5.3V ; V_2 = 3V S1 = A	40	56	70	µA	7D
I_{2SI}	Delay SINK Current	V_4 = 4.7V ; V_2 = 3V S1 = A	10			mA	7D
V_{3S}	Out Saturation Voltage	I_3 = 15mA ; S2 = B			0.4	V	7D
I_3	Output Leak Current	V_3 = 50V ; S2 = A			100	µA	7D
V_{4S}	Rising Threshold Voltage		5	5.1	5.2	V	7D
	Hysteresis		0.4	0.5	0.6	V	7D
I_4	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Application Circuit.



PART LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 22K
R_4 = 36K
R_5 = 22Ω
R_6 = 4.7K
R_7 = see table A
R_8 = OPTION
R_9 = 4.7K

* C_1 = C_2 = 1000µF 63V EYF (ROE)
C_3 = C_4 = C_5 = C_6 = 2,2µF 50V
C_7 = 330pF Film
C_8 = 22nF MKT 1837 (ERO)
C_9 = 2.2nF KP 1830 (ERO)
C_{10} = 0.1µF Film
C_{11} = 1nF
** C_{12} = C_{13} = C_{14} = 100µF 40V EKR (ROE)
C_{15} = 1µF Film

D = SBS 560 (OR EQUIVALENT)

L = 150µH
core 58310 MAGNETICS
45 TURNS 10mm (AWG 19)
COGEMA 949181

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V_o	R_9	R_7
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9.1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Figure 6 : Component Layout of fig.5 (1 : 1 scale). Evaluation Board Available.

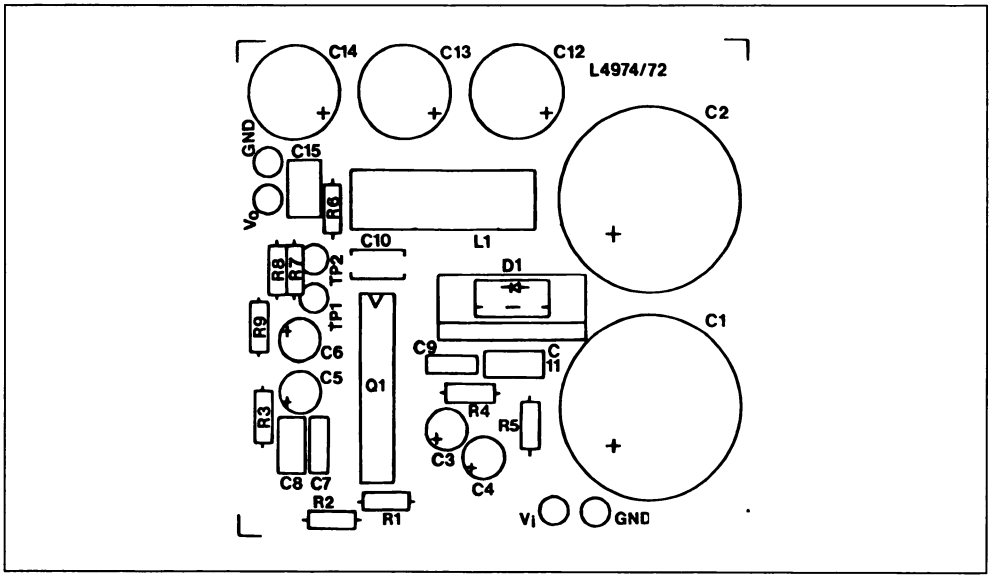


Figure 7 : DC Test Circuits.

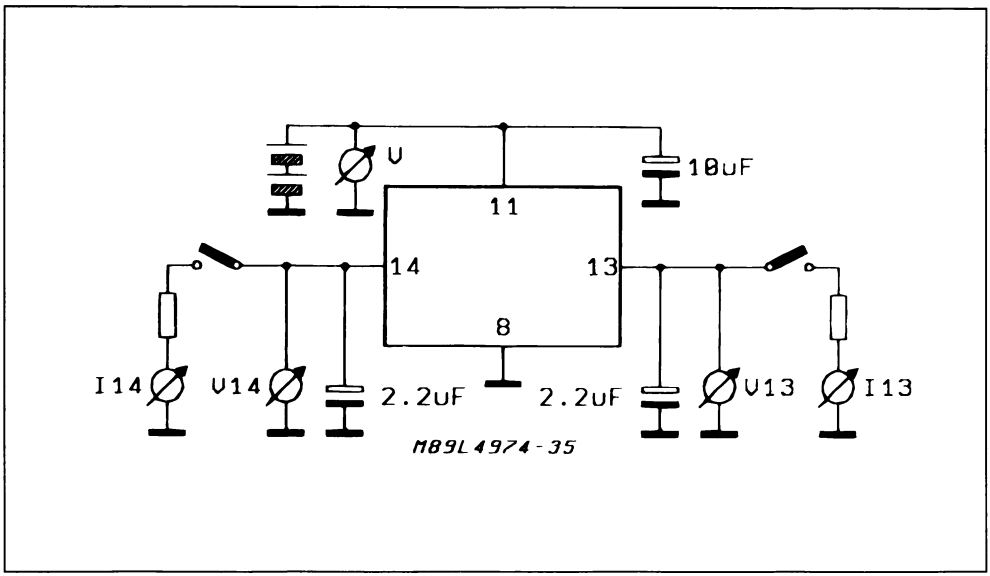


Figure 7A.

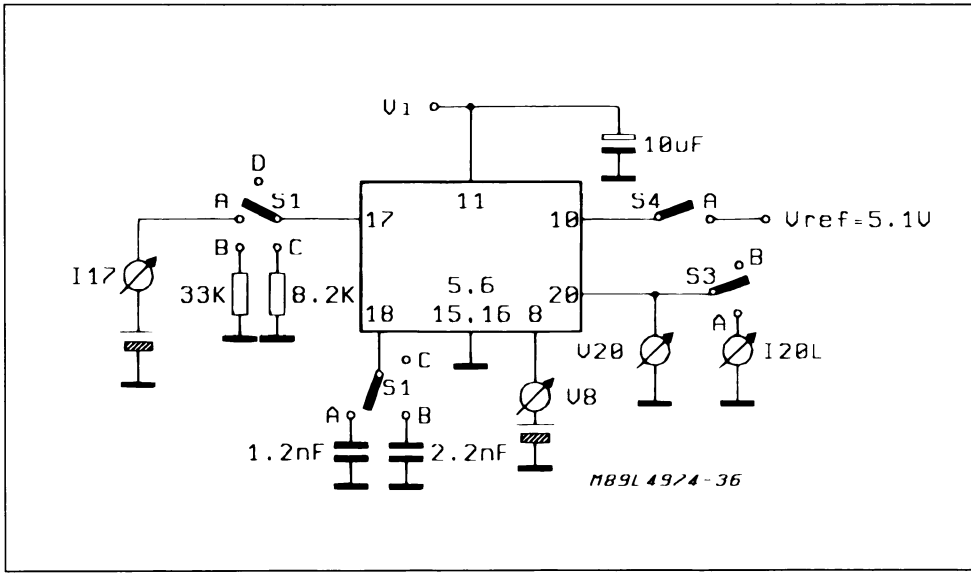


Figure 7B.

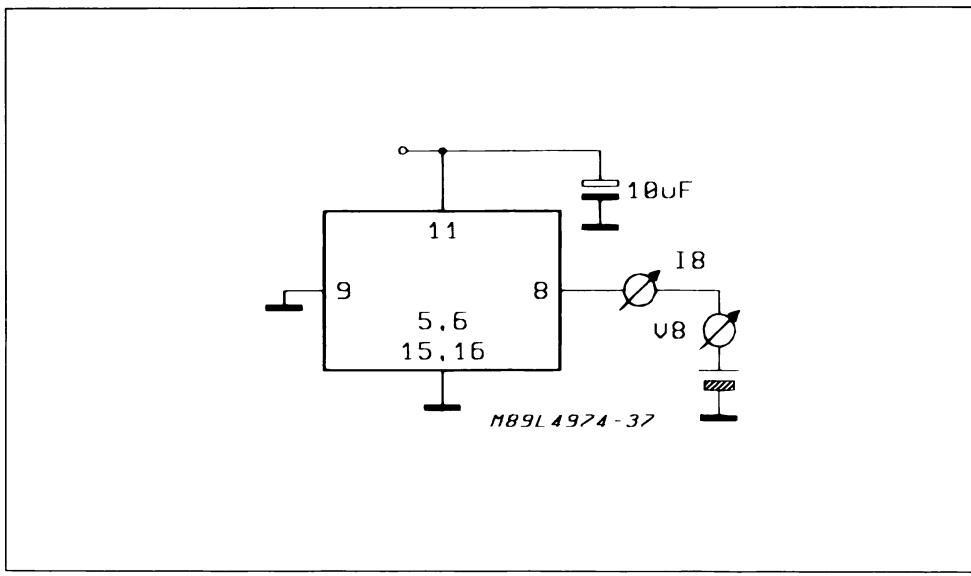


Figure 7C.

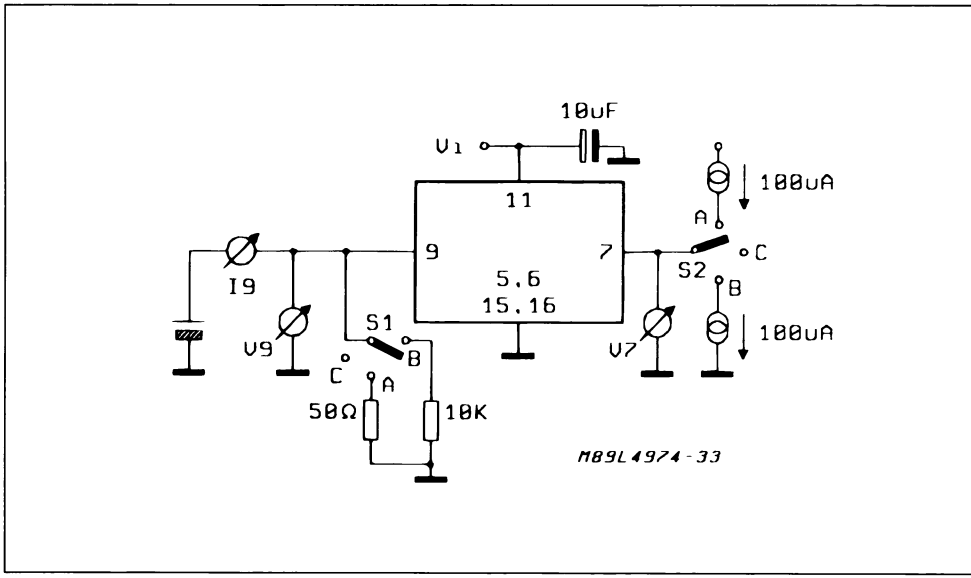


Figure 7D.

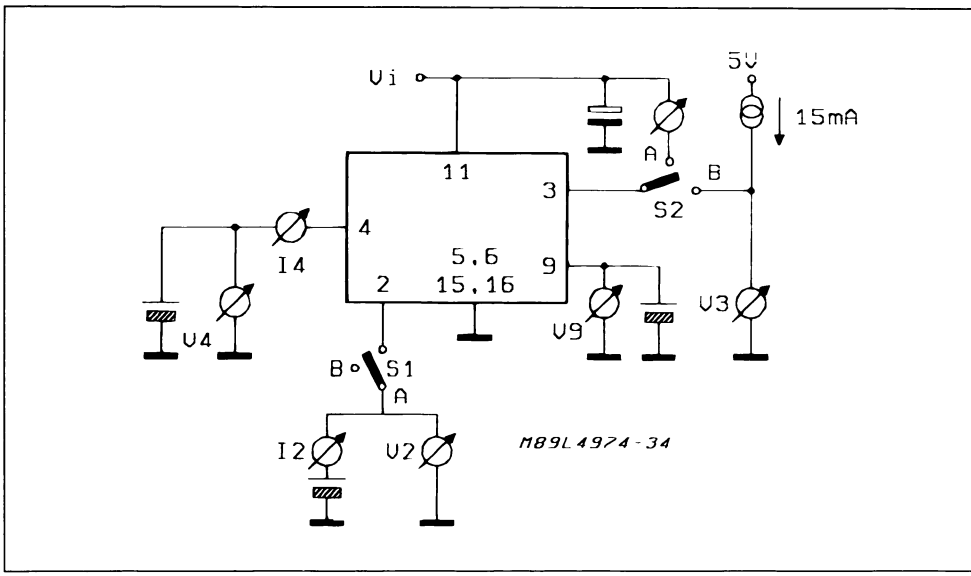


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

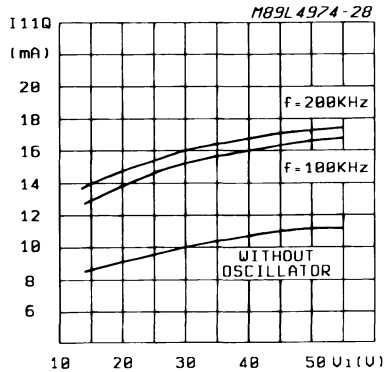


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

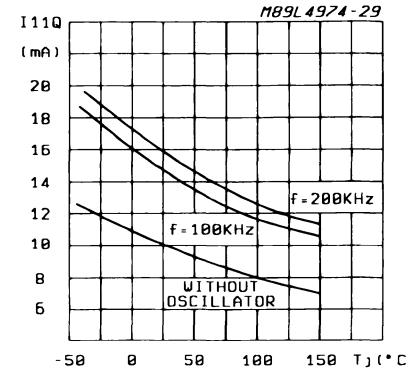


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

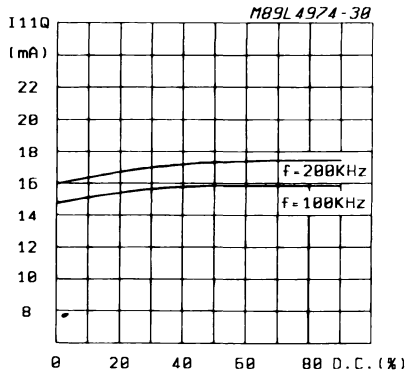


Figure 11 : Reference Voltage (pin 13) vs. Vi (see fig. 7).

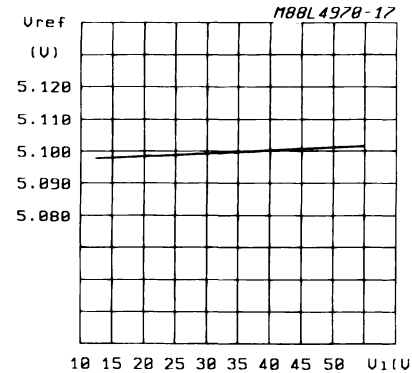


Figure 12 : Reference Voltage (pin 13) vs. Junction Temperature (see fig. 7).

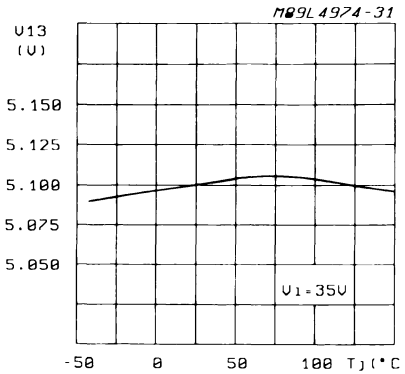


Figure 13 : Reference Voltage (pin 14) vs. Vi (see fig. 7).

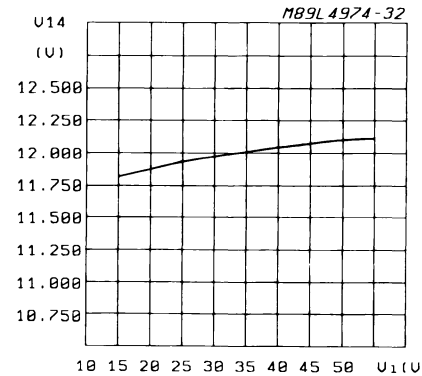


Figure 14 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

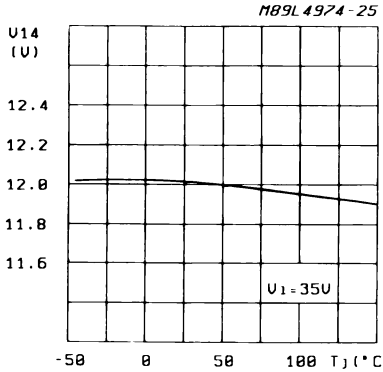


Figure 15 : Reference Voltage 5.1V (pin 13) Supply Voltage Ripple Rejection vs. Frequency.

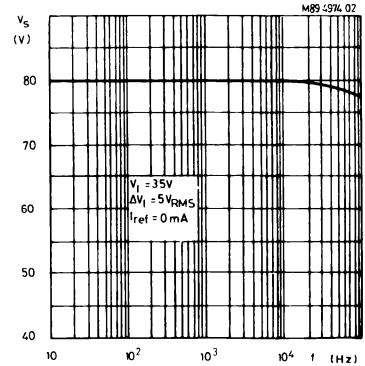


Figure 16 : Switching Frequency vs. Input Voltage (see fig. 5).

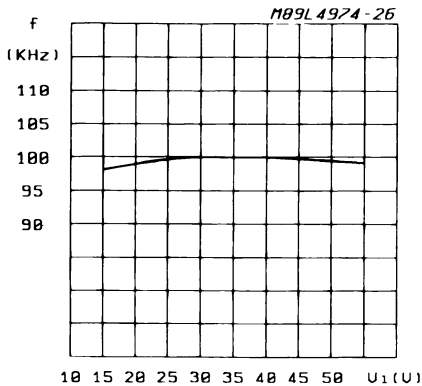


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

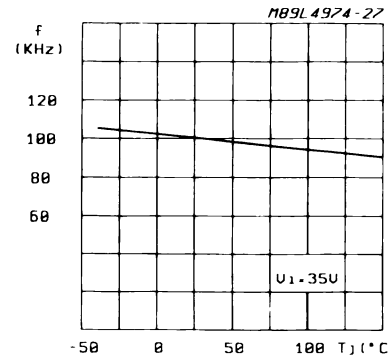


Figure 18 : Switching Frequency vs. R4 (see fig.5).

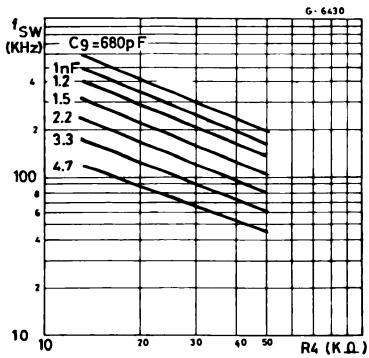


Figure 19 : Open Loop Frequency and Phase of Error Amplifier (see fig. 7C).

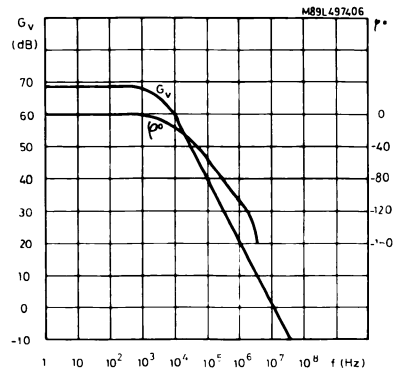


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

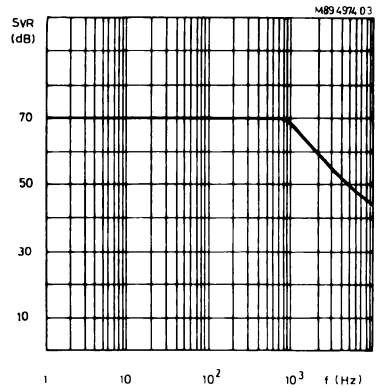


Figure 21 : Efficiency vs. Output Voltage.

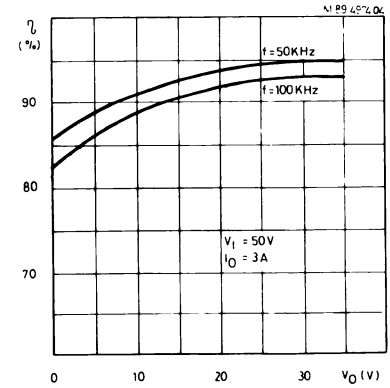


Figure 22 : Line Transient Response (see fig. 5).

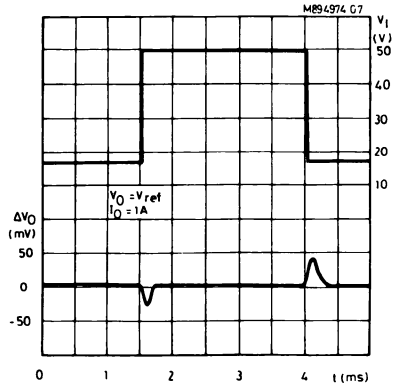


Figure 23 : Load Transient Response (see fig. 5).

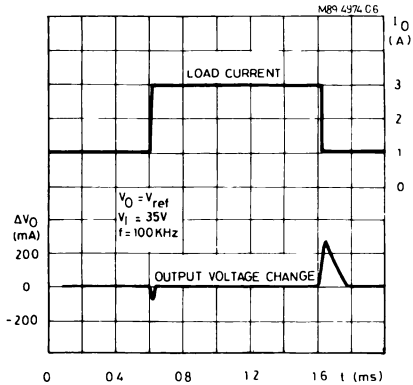


Figure 24 : Dropout Voltage between Pin 11 and Pin 20 vs. Current at Pin 20.

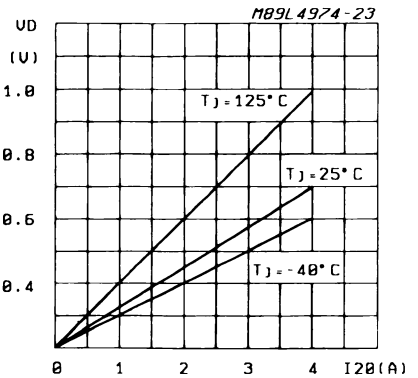


Figure 25 : Dropout Voltage between Pin 11 and Pin 20 vs. Junction Temperature.

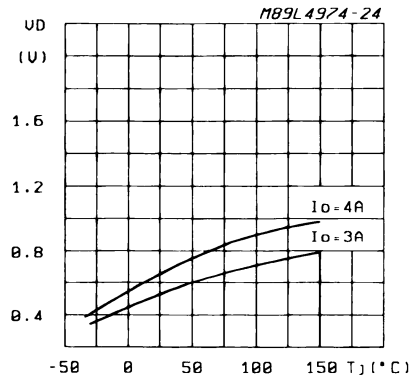


Figure 26 : Power Dissipation (device only) vs. Input Voltage.

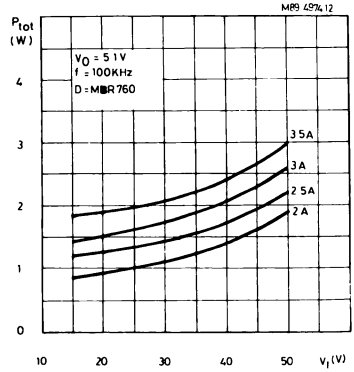


Figure 27 : Power Dissipation (device only) vs. Input Voltage.

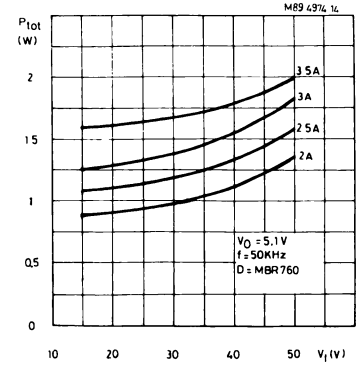


Figure 28 : Power Dissipation (device only) vs. Output Voltage.

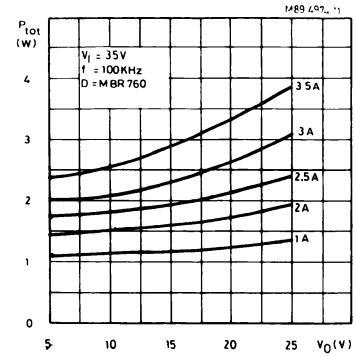


Figure 29 : Power Dissipation (device only) vs. Output Voltage.

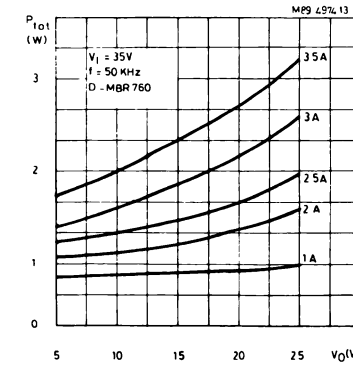


Figure 30 : Power Dissipation (device only) vs. Output Current.

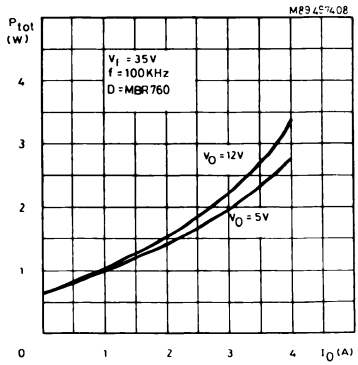


Figure 31 : Power Dissipation (device only) vs. Output Current.

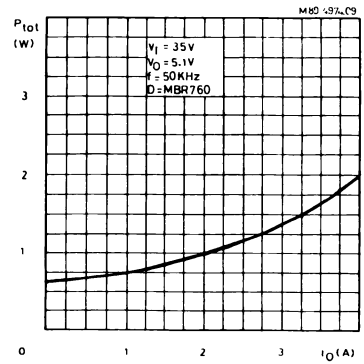


Figure 32 : Efficiency vs. Output Current.

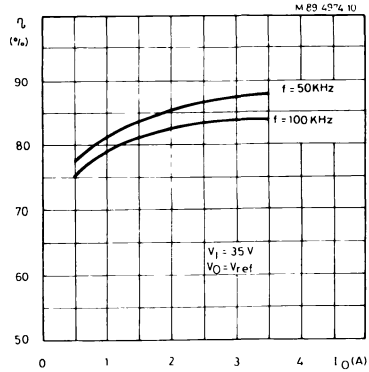


Figure 33 : Test PCB Thermal Characteristic.

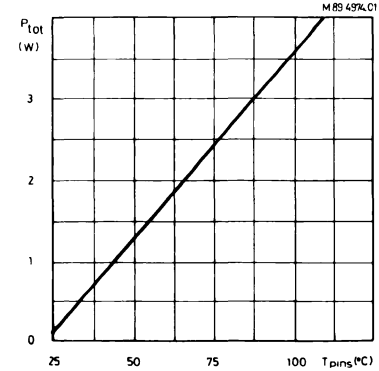


Figure 34 : R_{th} with two "on board" Square Heat Sinks vs. Side l.

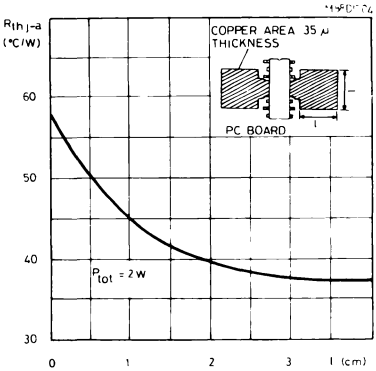
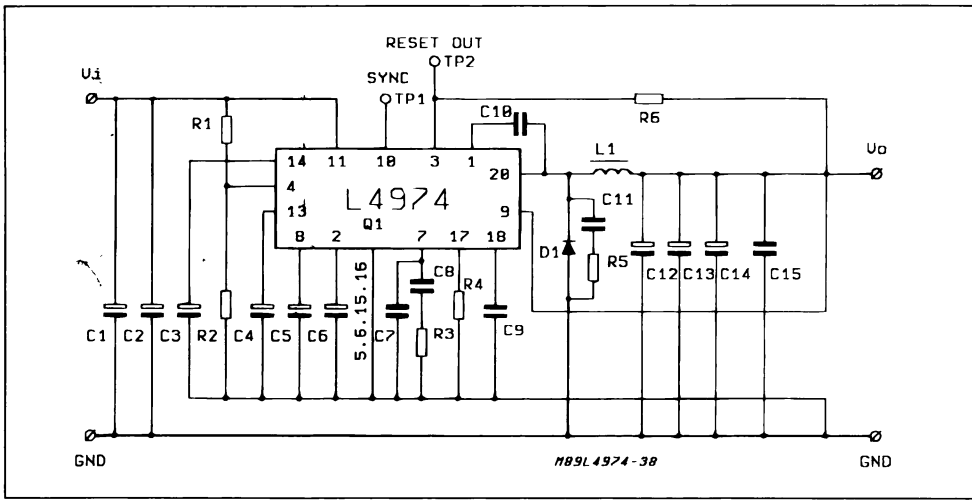


Figure 35 : 3.5A – 5.1V Application Circuit.



TYPICAL PERFORMANCES (using evaluation board) :

n = 83% (V_I = 35V ; V_o = VREF ; I_o = 2.5A ; f_{sw} = 100KHz)

$V_{o\ RIPPLE}$ = 30mV (at 1A)

Line regulator = 5mV (V_I = 15 to 50V)

Load regulator = 15mV (I_o = 2 top 10A)

for component values Refer to the fig. 5 (Part list).

Figure 36 : A 5.1V/12V Multiple Supply. Note the Synchronization between the L4974 and L4970.

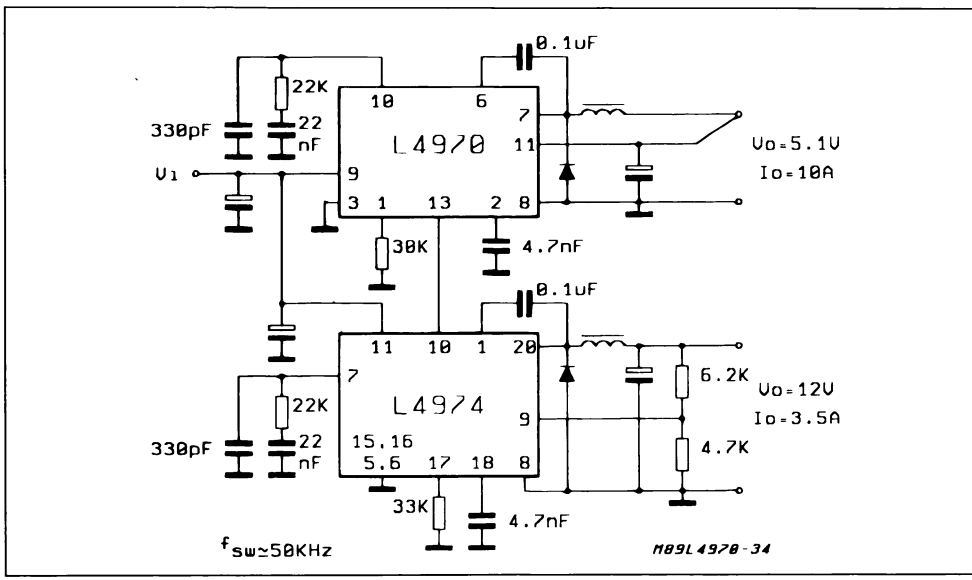
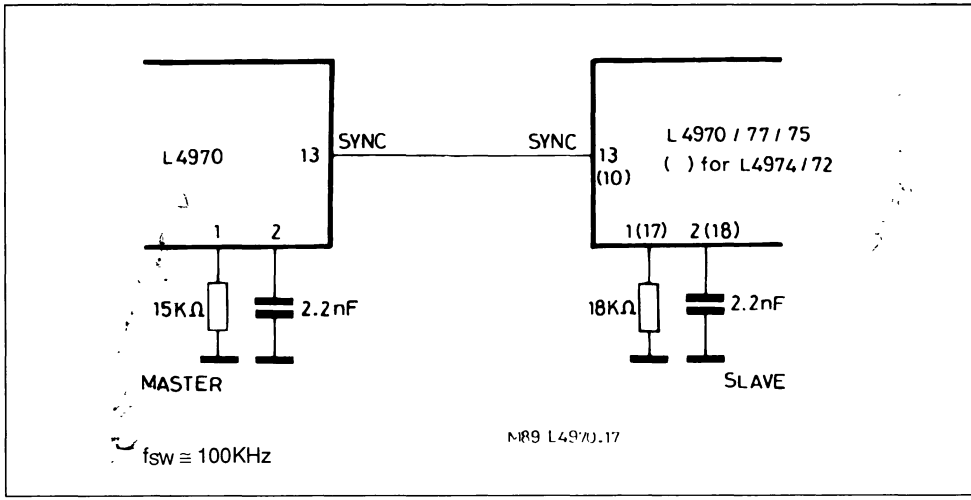


Figure 37 : L4974's Sync. Example.



5A SWITCHING REGULATOR

ADVANCE DATA

- 5A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND P. FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN

DESCRIPTION

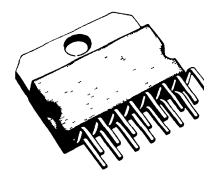
The L4975 is a stepdown monolithic power switching regulator delivering 5A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4975 include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

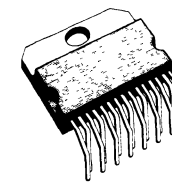
MULTIPOWER BCD TECHNOLOGY

Multiwatt ®
(15-lead)

Vertical

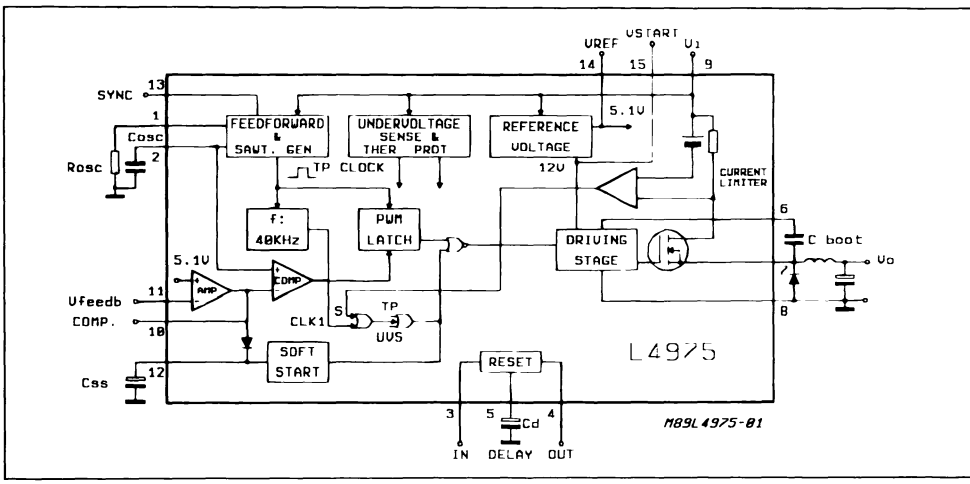


Horizontal



ORDER CODES : L4975 (Vertical)
L4975HT (Horizontal)

BLOCK DIAGRAM

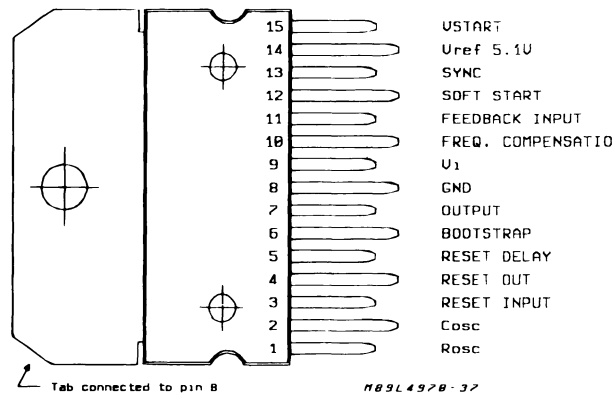


This is advanced information on a new product now in development or undergoing evaluation Details are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	– 1 – 7	V V
I_7	Max Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	mA
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external 30KΩ resistor when power fail signal not required
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor
7	OUTPUT	Regulator Output
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages
12	SOFT START	A capacitor is connected between this terminal and ground to define the soft start time.
13	SYNC INPUT	Multiple L4975's are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse
14	V_{ref}	5.1 V_{ref} Device Reference Voltage
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage

CIRCUIT OPERATION (refer to the block diagram)

The L4975 is a 5A monolithic stepdown switching regulator realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 5A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysterysis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysterysis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50nS. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing

Figure 1 : Feedforward Waveform.

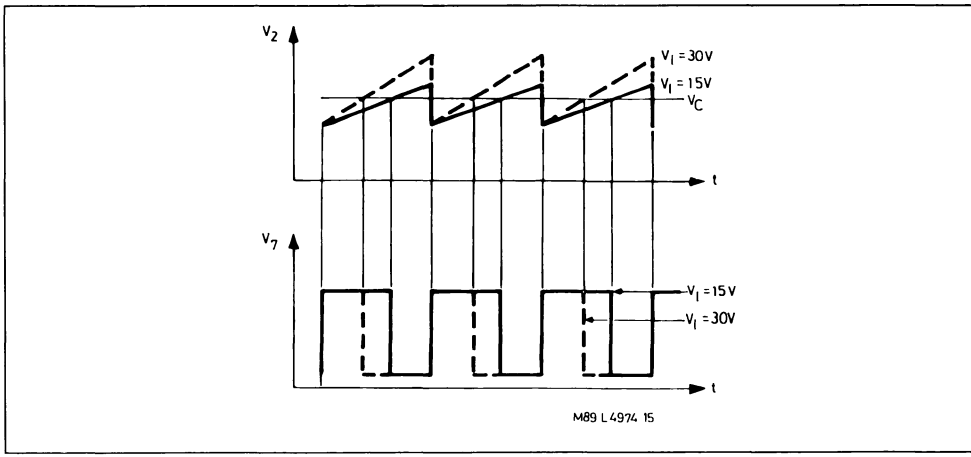


Figure 2 : Soft Start Function.

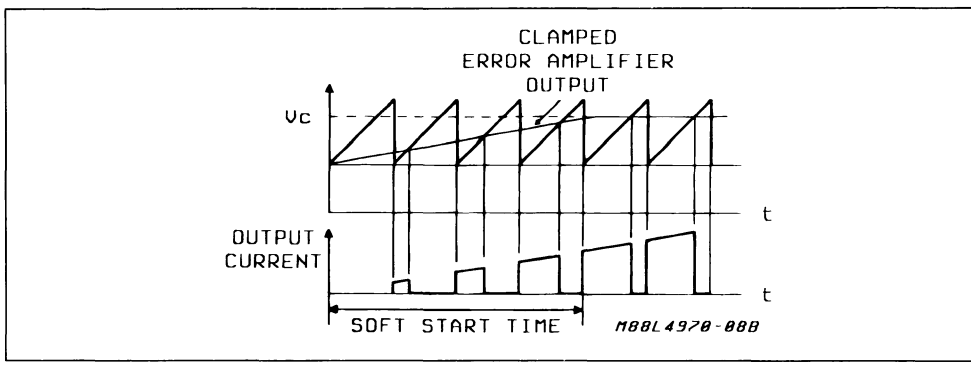
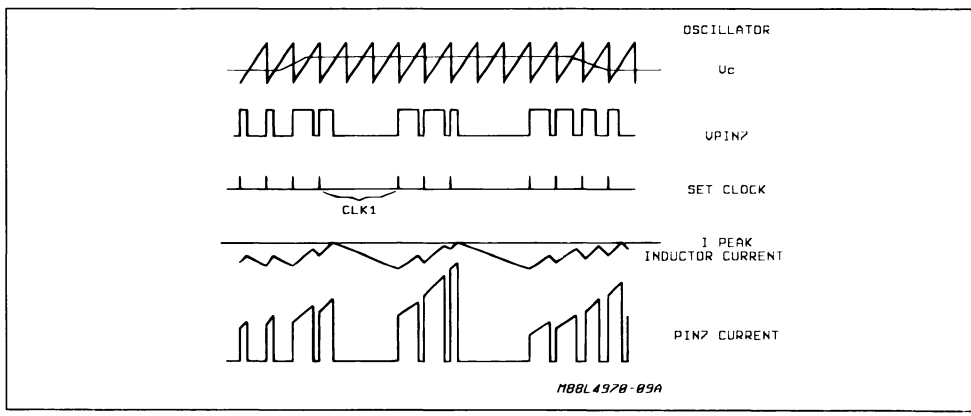


Figure 3 : Limiting Current Function.



the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy enviroments. The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

The Reset and Power fail circuit (fig. 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by a external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open drain.

Fig. 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig. 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150C and has an hysterysis to prevent unstable conditions.

Figure 4 : Reset and Power Fail Functions.

A

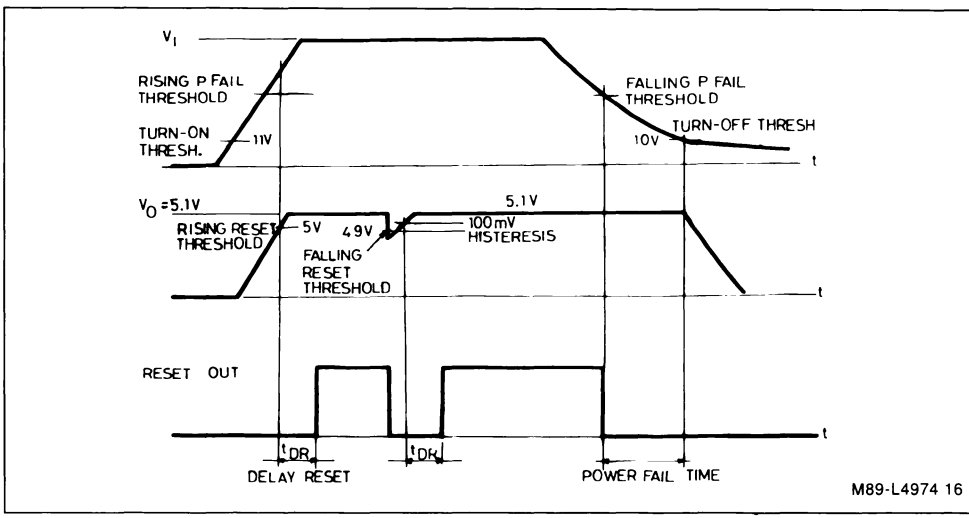
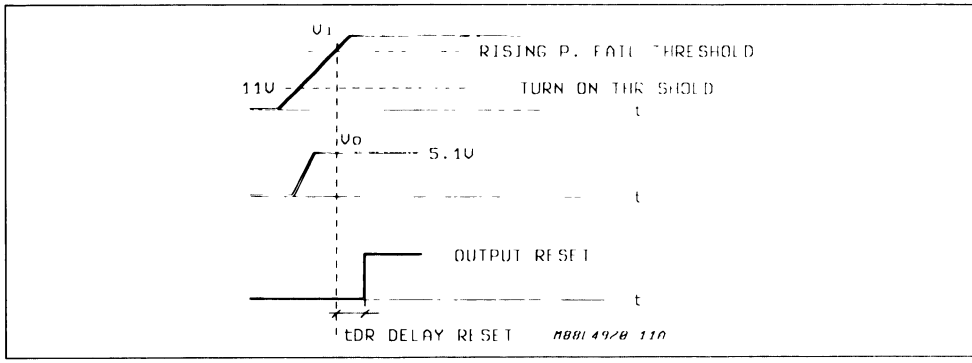


Figure 4 : Reset and Power Fall Functions (continued).

B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 15KΩ, C_9 = 2.2nF, f_{sw} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt Range (pin 9)	V_o = V_{ref} to 40V I_o = 5A	15		50	V	5
V_o	Output Voltage	V_i = 15V to 50V I_o = 3A , V_o = V_{ref}	5	5.1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 2A ; V_o = V_{ref}		12	30	mV	5
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 2A to 4A I_o = 1A to 5A		 10 20	 20 40	 mV mV	5
V_d	Dropout Voltage between Pin 9 and 7	I_o = 3A I_o = 5A		0.4 0.55	0.6 0.8	V V	5
I_{7L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	5.5	6.25	7	A	5
Efficiency		I_o = 3A V_o = V_{ref} V_o = 12V	 80	 85 92		 % %	5
		I_o = 5A V_o = V_{ref} V_o = 12V	 80	 85 92		 %	5
SVR	Supply Voltage Ripple Reject	V_i = 2VRMS , I_o = 3A f = 100Hz ; V_o = Vref	56	60		dB	5
f	Switching Freq		180	200	220	KHz	5
$\Delta f/_{\Delta V_i}$	Volt Stability of Switching Freq	V_i = 15V to 45V		2	6	%	5
$\Delta f/_{T_j}$	Temp Stability of Switch. Freq	T_j = 0 to 125 C		1		%	5
f_{max}	Max Operating Switch Freq	V_o = V_{ref} , R_4 = 9.1KΩ I_o = 5A ; C_9 = 1.2nF	500			KHz	5

ELECTRICAL CHARACTERISTICS (continued)

V_{REF} SECTION (pin 14)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{REF}	Reference Voltage		5	5 1	5.2	V	7
ΔV_{REF}	Line Regulation	V_i = 15V to 50V V_{12} = 0		10	25	mV	7
ΔV_{REF}	Load Regulation	I_{REF} = 0 to 3mA		20	40	mV	7
$\Delta V_{REF}/\Delta T$	Average Temp Coeff. Ref. Voltage	T_j = 0°C to 125°C		0 4		mV/C	7
I_{REF}	Short Circuit Curr Limit	V_{REF} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{ref}	Reference Voltage	P_{12} = 0V	11 4	12	12 6	V	7
ΔV_{ref}	Line Regulation	P_{12} = 0V ; V_i = 15 to 50V		0.4	1	V	7
ΔV_{ref}	Load Regulation	I_{ref} = 0 to 1mA P_{12} = 0V		50	200	mV	7
I_{ref}	Short Circuit Current Limit	P_{12} = 0V , P_{15} = 0V		80		mA	7

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn-on Thresh.		10	11	12	V	7A
V_{9Hyst}	Turn-off Hyster			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0 ; S1 = D ; S2 = C ; S4 = A		10	16	mA	7A
I_{9OQ}	Operating Quiescent Curr.	V_{12} = 0		16	20	mA	7A
I_{7L}	Out Leak Current	V_i = 55V ; S3 = A ; V_{12} = 0V ;			2	mA	7A

SOFT START (pin 12)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V , V_{11} = 0V	70	100	130	µA	7B
V_{12s}	Output Saturation Voltage	I_{12s} = 20mA ; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level out Voltage	I_{10} = – 50µA ; S2 = A P_{11} = 0V ; S1 = C	6			V	7C
V_{10L}	Low Level out Voltage	I_{10} = 50µA ; S2 = A P_{11} = 6V , S1 = C			0.7	V	7C
I_{11}	Input Bias Current	V_{11} = 5 ; S1 = B , R_S = 10K		2	10	uA	7C
VOS	Input off Voltage	P_{11} = Vos ; R_s = 50Ω ; S1 = A		2	10	mV	7C
G_V	DC Open Loop Gain	P_{VCM} = 4V ; R_S = 50Ω ; S1 = A	60			dB	7C
SVR	Supply Volt. Rej.	15 < Vi < 50V	60	80		dB	7C

ELECTRICAL CHARACTERISTICS (continued)

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	max.	Unit	Fig.
	Ramp Valley			1.5		V	7A
	Ramp Peak	V_I = 15V V_I = 45V		2.5 5.5		V V	7A
	Min Ramp Current	S1 = A ; I1 = 100µA		270	300	µA	7A
	Max Ramp Current	S1 = A ; I1 = 1mA	2.4	2 7		mA	7A

SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYNC	Low Input Voltage	V_I = 15V to 50V	– 0.3		0 9	V	
SYNC	High Input Voltage	V_{12} = 0	3.5		5.5	V	
$-I_{13L}$	Sync Input Current with Low Input Voltage	V_{13} = 0.9V			0 4	mA	
$-I_{13H}$	Input Current with High Input Voltage	V_{13} = 3.5V			1 5	mA	
SYNC	Delay			50		ns	
	Output Amplitude		4	5		V	
	Output Pulse Width	V_{thr} = 2.5V	0 3	0.5	0 8	µsec	

RESET AND P. FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_I = 15 to 50V S1 = B	Vref – 120	Vref – 100	Vref – 80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	V_I = 15 to 50V S1 = B	4 77	Vref –200	Vref –160	V mV	7D
V_{5H}	Delay High Threshold Voltage	S1 = B	5	5.1	5 2	V	7D
V_{5L}	Delay Low Threshold Voltage	S1 = B	1	1 1	1 2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5.3V , V_5 = 3V S1 = A	40	55	70	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V , V_5 = 3V S1 = A	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA ; S2 = B			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V ; S2 = A			100	µA	7D
V_{3R}	Rising Threshold Voltage		5	5.1	5.2	V	7D
	Hysteresis		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Application Circuit.

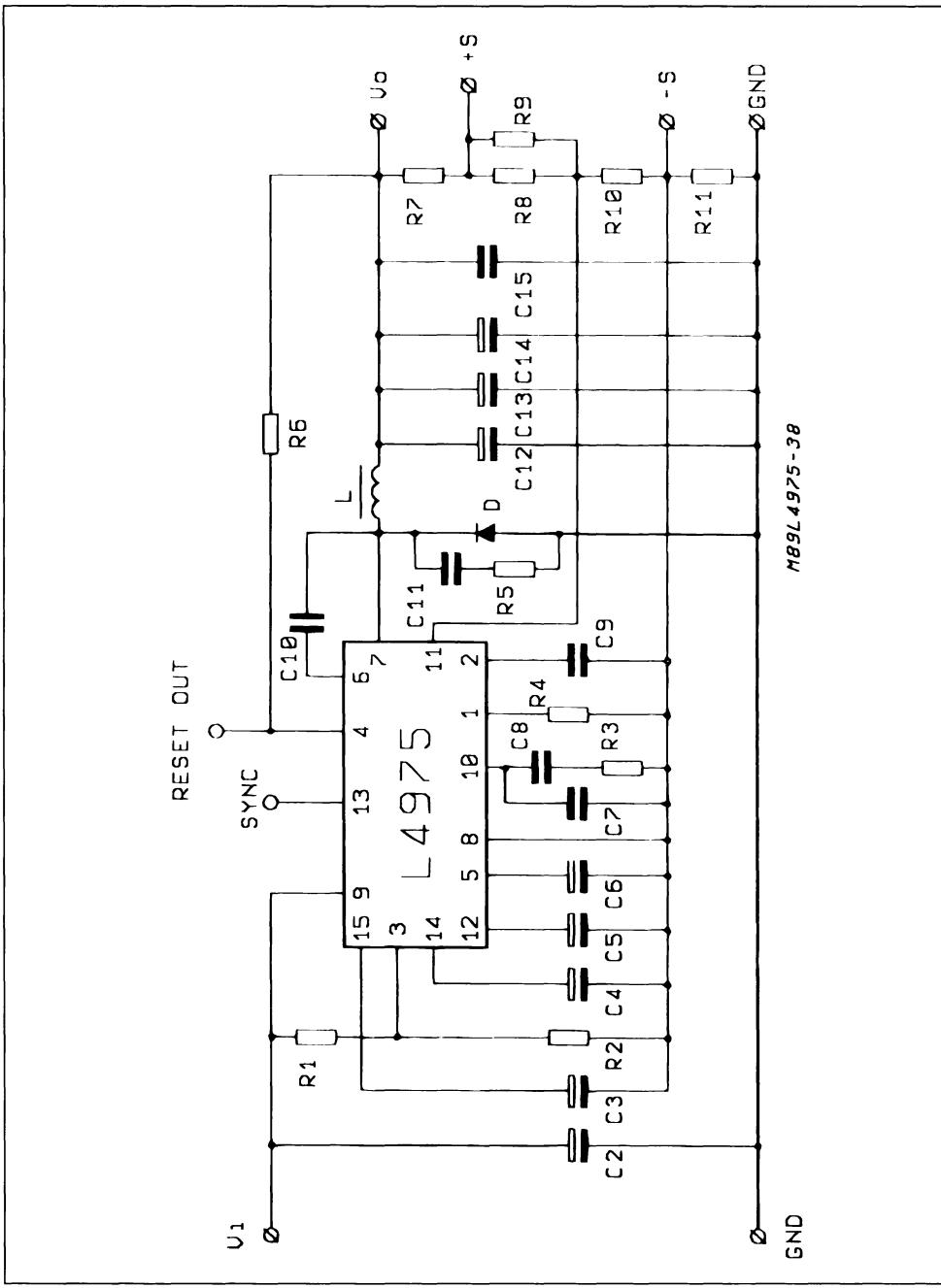
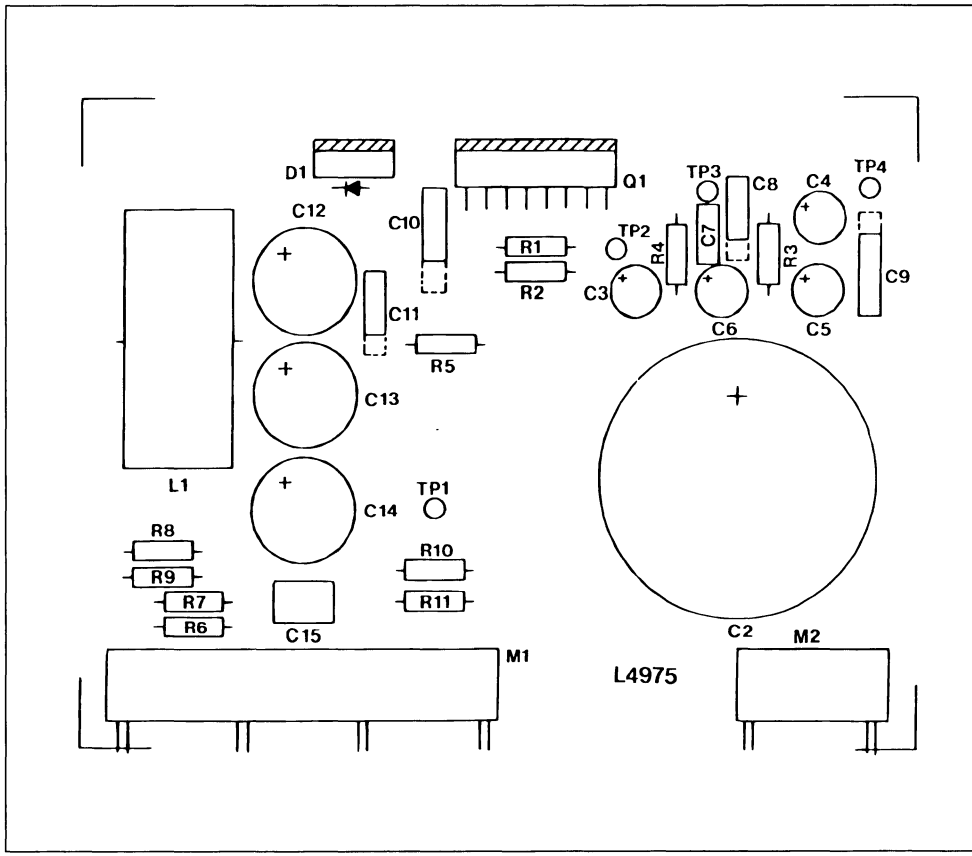


Figure 6 : Component Layout of Figure 5 (1 : 1 scale).



PARTS LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 22KΩ
R_4 = 15KΩ
R_5 = 22Ω 0,5W
R_6 = 4K7
R_7 = 10Ω
R_8 = see table A
R_9 = OPTION
R_{10} = 4K7
R_{11} = 10Ω
C_2 = 3300µF 63V_L EYF (ROE)
C_3, C_4, C_5, C_6 = 2 2µF
C_7 = 330pF Film
C_8 = 22nF MKT 1817 (ERO)
C_9 = 2.2nF KP1830
C_{10} = 0.1µF MKT
C_{11} = 2 2nF MP1830
**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR (ROE)
C_{15} = 1µF Film
D = SBS 860T (or 8A/60V equivalent)
L = 1000µH cote 58071 MAGNETICS
27 TURNS Ø 1,3mm (AWG 16)
COGEMA 949180

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V_0	R_{10}	R_8
12V	4.7KΩ	6.2KΩ
15V	4 7KΩ	9 1KΩ
18V	4.7KΩ	12KΩ
24V	4 7KΩ	18KΩ

Figure 7 : DC Test Circuits.

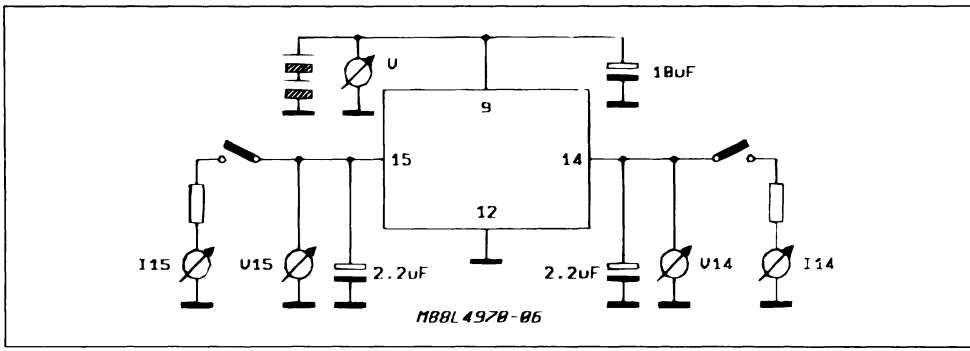


Figure 7A.

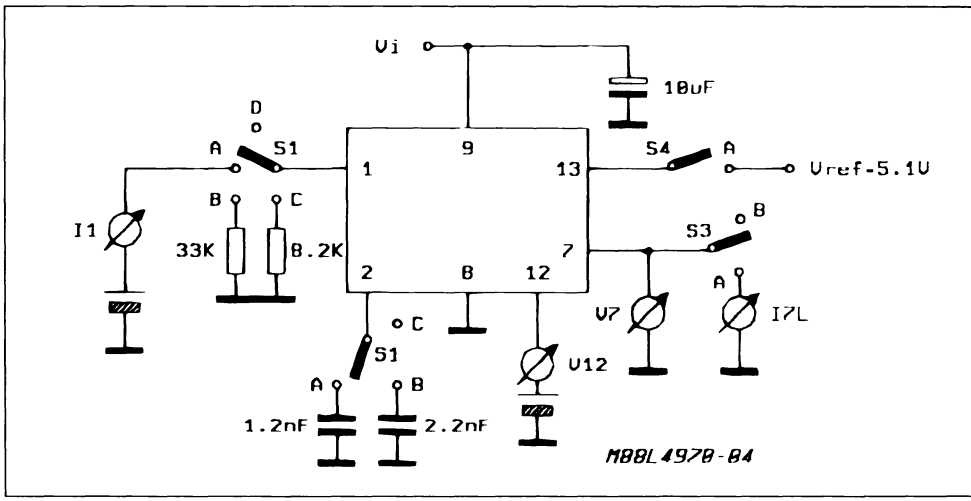


Figure 7B.

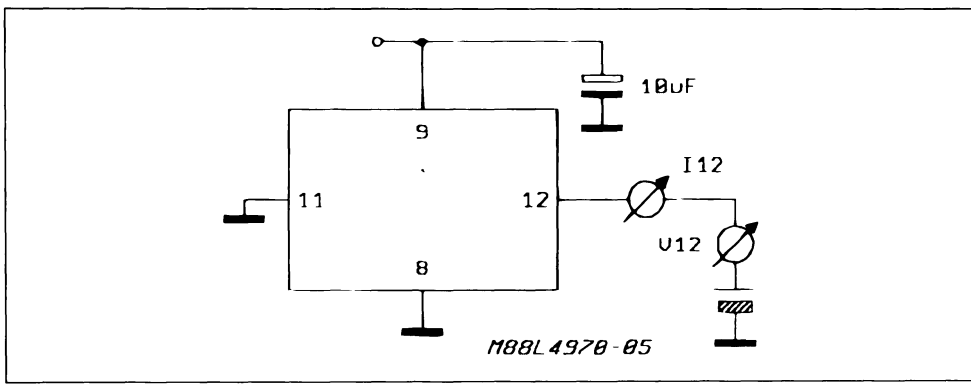


Figure 7C.

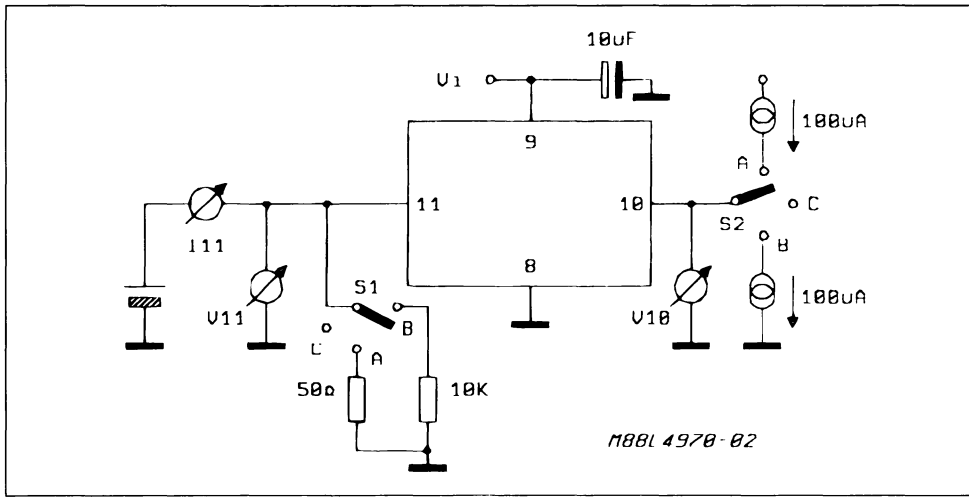


Figure 7D.

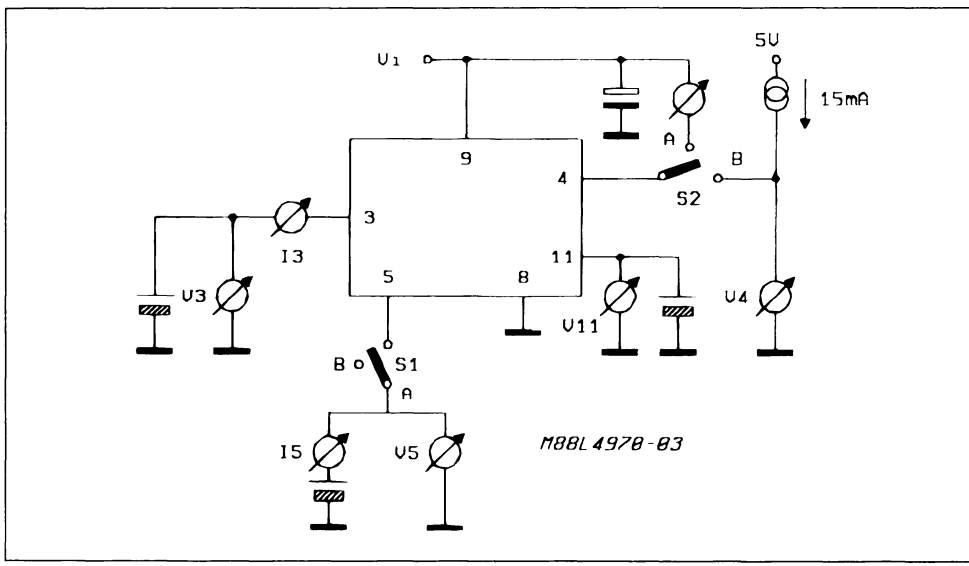


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

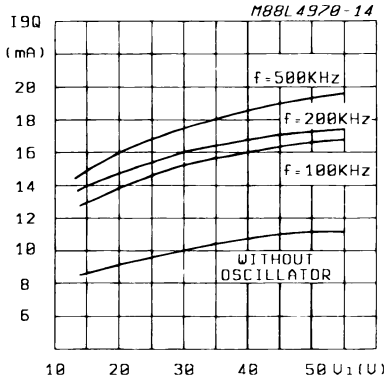


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

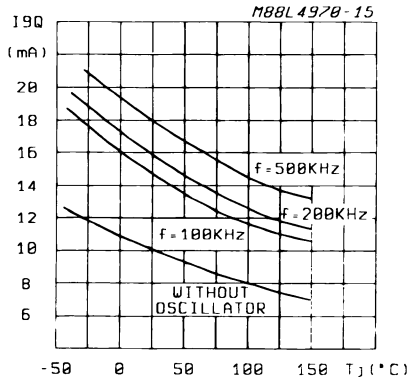


Figure 10 : Quiescent Drain Current vs. Duty Cycle.

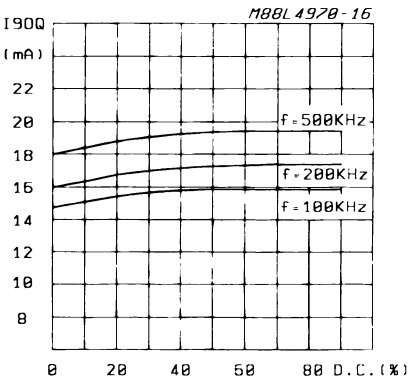


Figure 11 : Reference Voltage (pin 14) vs. V_I (see fig. 7).

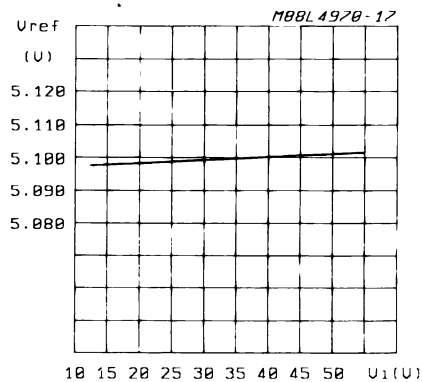


Figure 12 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

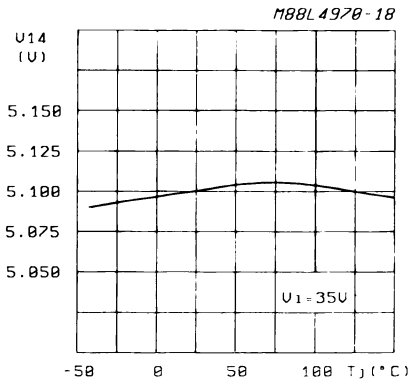


Figure 13 : Reference Voltage (pin 15) vs. V_I (see fig. 7).

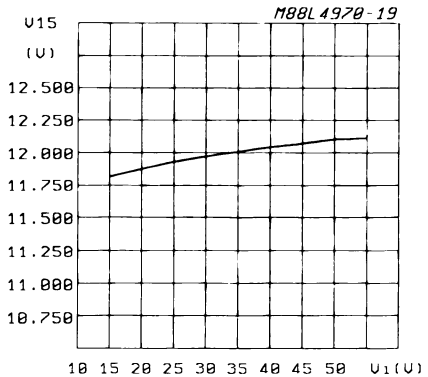


Figure 14 : Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7).

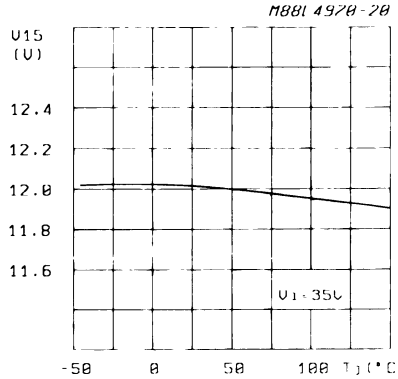


Figure 15 : Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency.

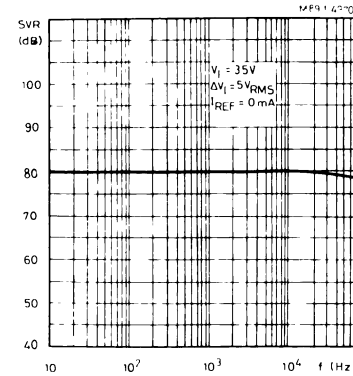


Figure 16 : Switching Frequency vs. Input Voltage (see fig. 5).

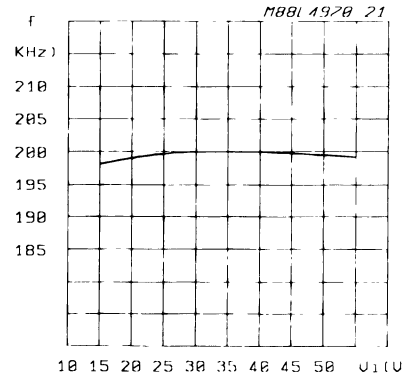


Figure 17 : Switching Frequency vs Junction Temperature (see fig. 5).

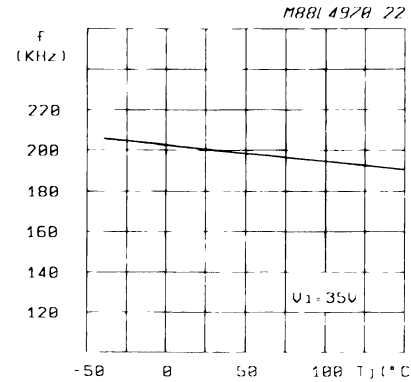


Figure 18 : Switching Frequency vs. R4 (see fig. 5).

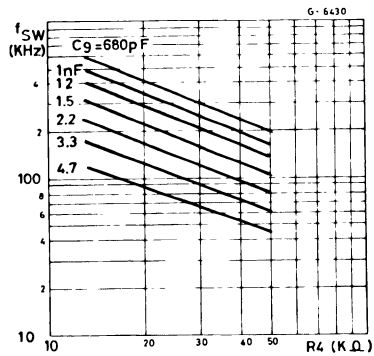


Figure 19 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 7C).

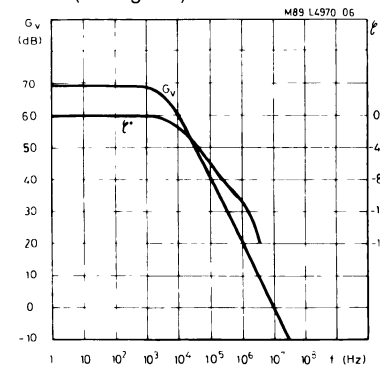


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

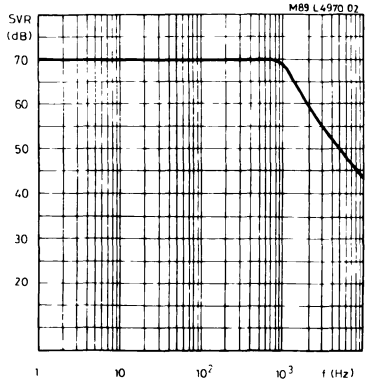


Figure 21 : Line Transient Response (see fig. 5).

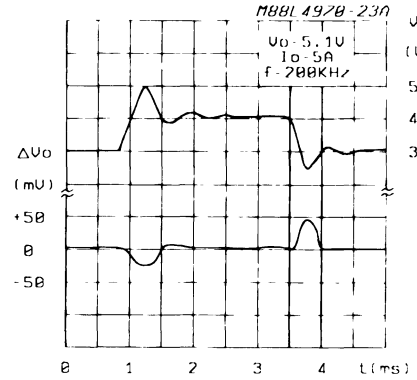


Figure 22 : Load Transient Response (see fig. 5).

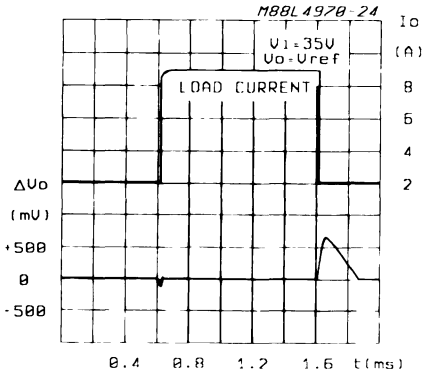


Figure 23 : Dropout Voltage between Pin 9 and Pin 7 vs. Current at Pin 7.

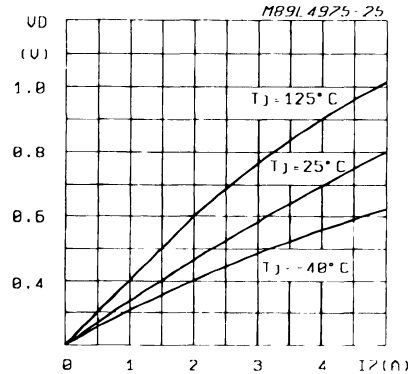


Figure 24 : Dropout Voltage between Pin 9 and Pin 7 vs. Junction Temperature.

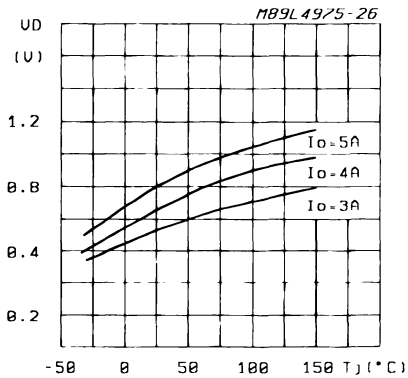


Figure 25 : Power Dissipation (device only) vs. Input Voltage.

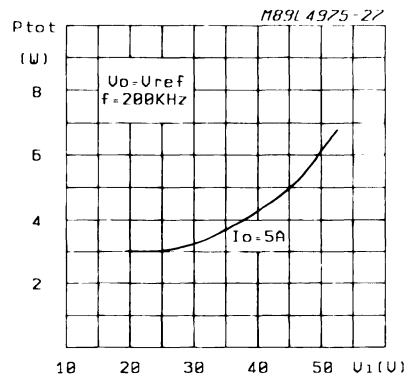


Figure 26 : Power Dissipation (device only) vs. Output Voltage.

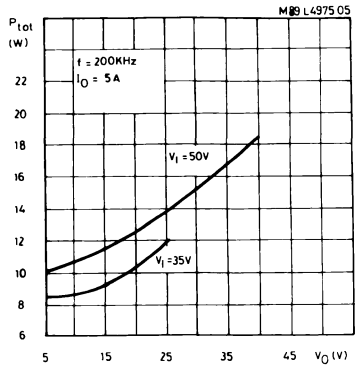


Figure 27 : Heatsink Used to Derive the Device's Power Dissipation (R_{th} – Heatsink = T_{case} – T_{amb}).

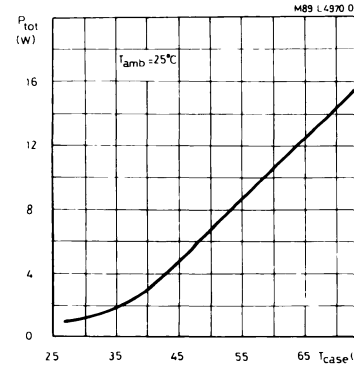


Figure 28 : Efficiency vs. Output Current.

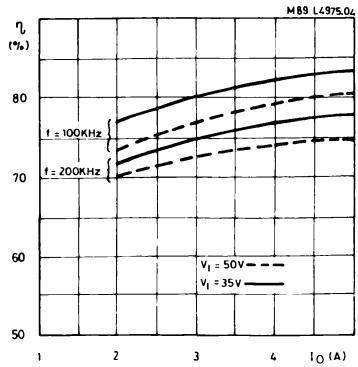


Figure 29 : Efficiency vs. Output Voltage.

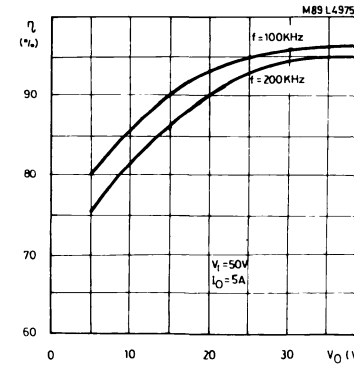


Figure 30 : Efficiency vs. Output Voltage.

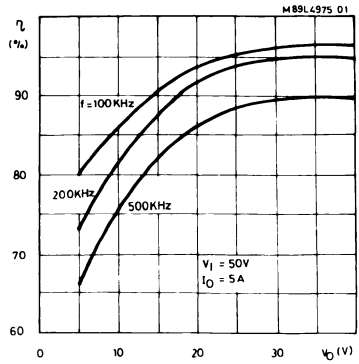


Figure 31 : Efficiency vs. Output Voltage.

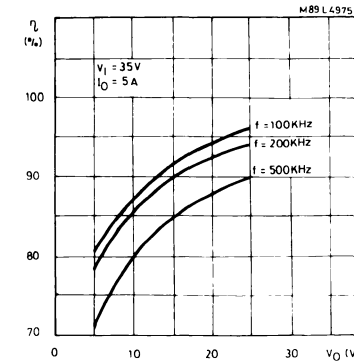


Figure 32 : Power Dissipation Derating Curve.

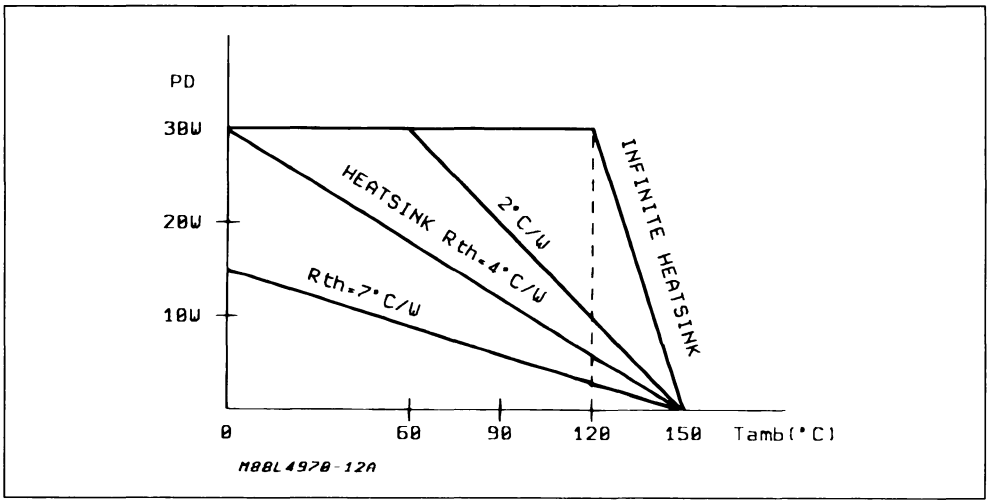
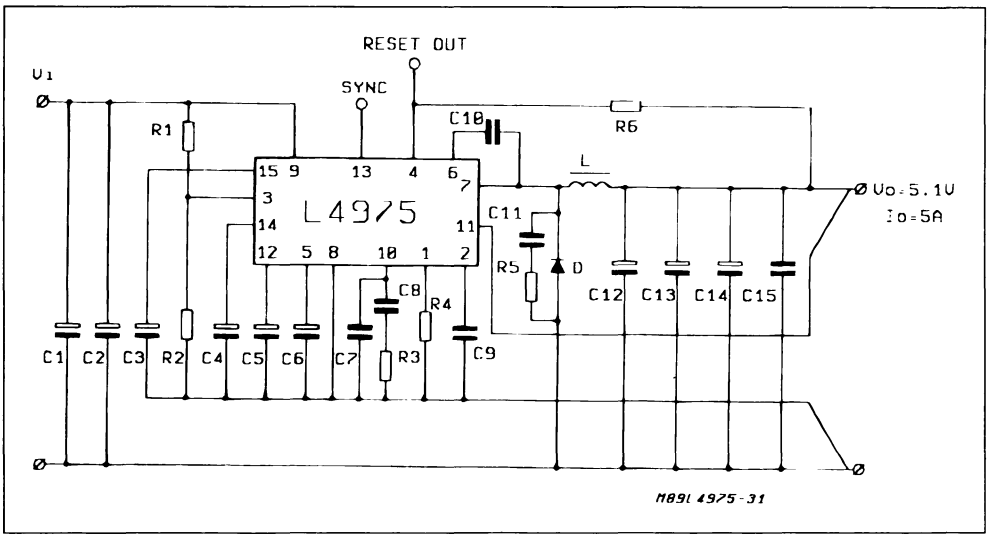


Figure 33 : 5A - 5.1V Application Circuit.



TYPICAL PERFORMANCES (using evaluation board) :

n = 83% (V_I = 35V ; V_o = V_{REF} ; I_o = 5A ; f_{SW} = 200KHz)

$V_{o\ RIPPLE}$ = 30mV (at 5A)

Line regulation = 5mV (V_I = 15 to 50V)

Load regulation = 15mV (I_o = 2 to 5A)

For component values, refer to test circuit part list.

Figure 34 : A 5.1V / 12V Multiple Supply. Note the Synchronization between the L4975 and the L4974.

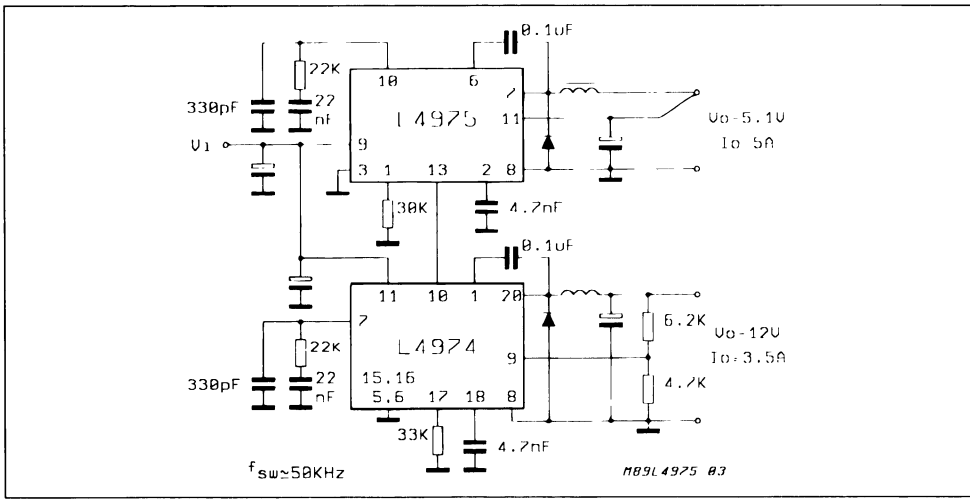


Figure 35 : L4970's Sync. Example.

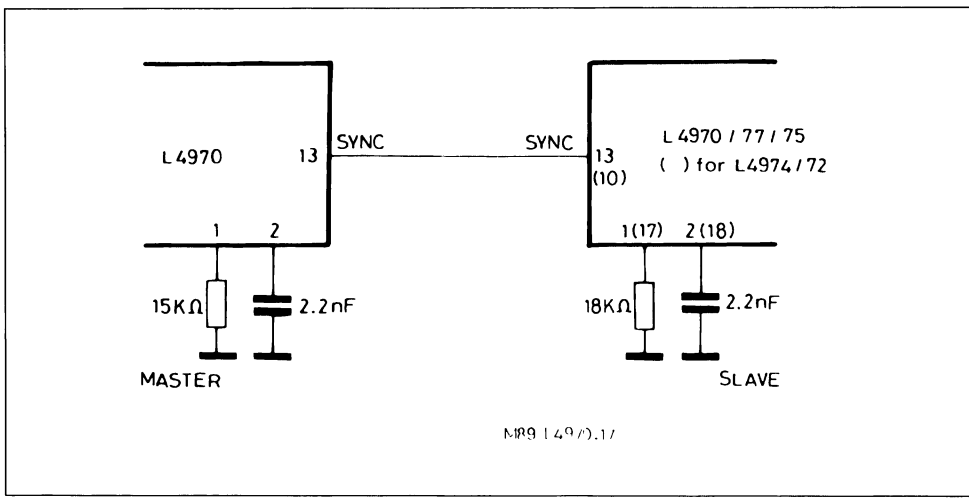
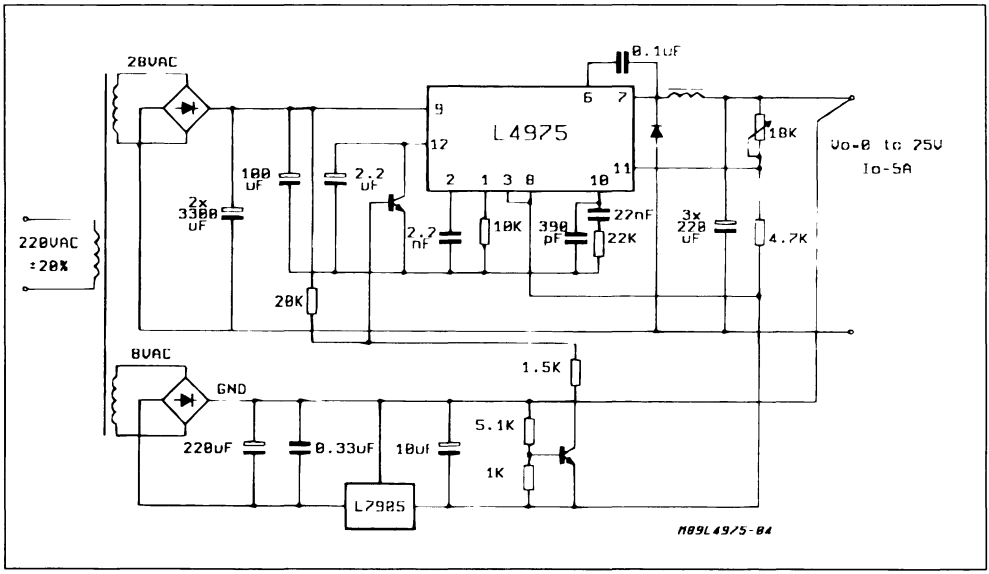


Figure 36 : 5A Switching Regulator, Adjustable from 0V to 25V.



7A SWITCHING REGULATOR

ADVANCE DATA

- 7A OUTPUT CURRENT
- 5.1V TO 40V OUTPUT VOLTAGE RANGE
- 0 TO 90% DUTY CYCLE RANGE
- INTERNAL FEED-FORWARD LINE REGULATION
- INTERNAL CURRENT LIMITING
- PRECISE 5.1V ± 2% ON CHIP REFERENCE
- RESET AND P FAIL FUNCTIONS
- SOFT START
- INPUT/OUTPUT SYNC PIN
- UNDER VOLTAGE LOCK OUT WITH HYSTERETIC TURN-ON
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- VERY HIGH EFFICIENCY
- SWITCHING FREQUENCY UP TO 500KHz
- THERMAL SHUTDOWN

DESCRIPTION

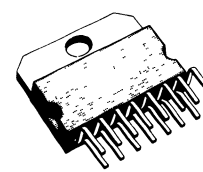
The L4977 is a stepdown monolithic power switching regulator delivering 7A at a voltage variable from 5.1 to 40V.

Realized with BCD mixed technology, the device uses a DMOS output transistor to obtain very high efficiency and very fast switching times. Features of the L4977 include reset and power fail for microprocessors, feed forward line regulation, soft start, limiting current and thermal protection. The device is mounted in a 15-lead multiwatt plastic power package and requires few external components. Efficient operation at switching frequencies up to 500KHz allows reduction in the size and cost of external filter components.

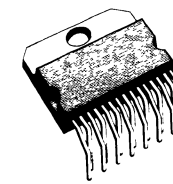
MULTIPOWER BCD TECHNOLOGY

Multiwatt ®
(15-lead)

Vertical

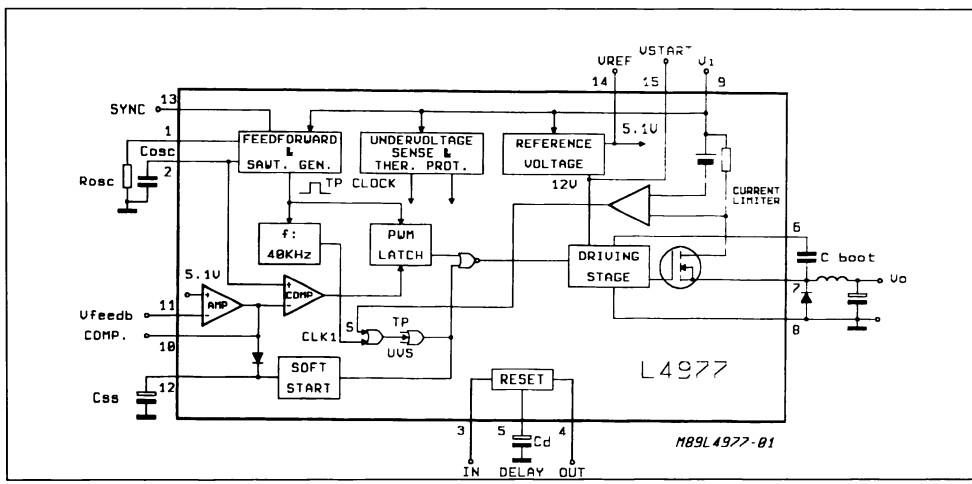


Horizontal



ORDER CODES : L4977 (Vertical)
L4977HT (Horizontal)

BLOCK DIAGRAM

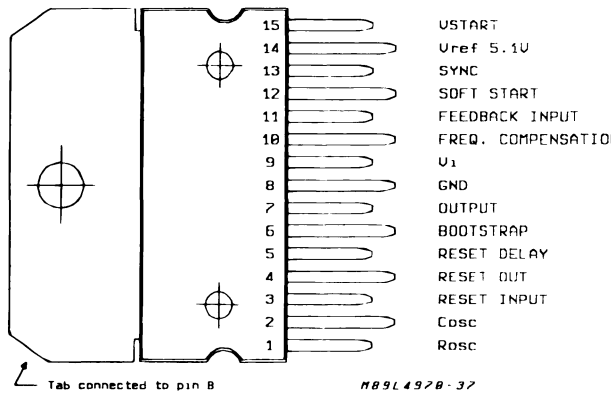


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_9	Input Voltage	55	V
V_9	Input Operating Voltage	50	V
V_7	Output DC Voltage Output Peak Voltage at t = 0.1µs f = 200KHz	– 1 – 7	V V
I_7	Max Output Current	Internally Limited	
V_6	Bootstrap Voltage Bootstrap Operating Voltage	65 V_9 + 15	V V
V_3, V_{12}	Input Voltage at Pins 3, 12	12	V
V_4	Reset Output Voltage	50	V
I_4	Reset Output Sink Current	50	mA
V_5, V_{10}, V_{11}, V_{13}	Input Voltage at Pin 5, 10, 11, 13	7	V
I_5	Reset Delay Sink Current	30	mA
I_{10}	Error Amplifier Output Sink Current	1	mA
I_{12}	Soft Start Sink Current	30	mA
P_{tot}	Total Power Dissipation at T_{case} < 120°C	30	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

PIN CONNECTION (top view)



THERMAL DATA

Rth j–case	Thermal Resistance Junction–case	Max	1	°C/W
Rth j–amb	Thermal Resistance Junction–ambient	Max	35	

PIN FUNCTIONS

N°	Name	Function
1	OSCILLATOR	R_{osc}. External resistor connected to ground determines the constant charging current of C_{osc}.
2	OSCILLATOR	C_{osc}. External capacitor connected to ground determines (with R_{osc}) the switching frequency.
3	RESET INPUT	Input of Power Fail Circuit. The threshold is 5.1V. It may be connected via a divider to the input for power fail function. It must be connected to the pin 15 with an external 30KΩ resistor when power fail signal not required.
4	RESET OUT	Open Collector Reset/power Fail Signal Output. This output is high when the supply and the output voltages are safe
5	RESET DELAY	A C_d capacitor connected between this terminal and ground determines the reset signal delay time.
6	BOOTSTRAP	A C_{boot} capacitor connected between this terminal and the output allows to drive properly the internal D–MOS transistor.
7	OUTPUT	Regulator Output
8	GROUND	Common Ground Terminal
9	SUPPLY VOLTAGE	Unregulated Input Voltage
10	FREQUENCY COMPENSATION	A serie RC network connected between this terminal and ground determines the regulation loop gain characteristics.
11	FEEDBACK INPUT	The Feedback Terminal of the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
12	SOFT START	A capacitor is connected between this terminal and ground to define the soft start time.
13	SYNC INPUT	Multiple L4977's are synchronized by connecting pin 13 inputs togheter or via an external syncr. pulse
14	V_{ref}	5.1 V_{ref} Device Reference Voltage
15	V_{start}	Internal Start-up Circuit to Drive the Power Stage

CIRCUIT OPERATION (refer to the block diagram)

The L4977 is a 7A monolithic stepdown switching regulator realized in the new BCD Technology. This technology allows the integration of isolated vertical DMOS power transistors plus mixed CMOS/Bipolar transistors.

The device can deliver 7A at an output voltage adjustable from 5.1V to 40V, and contains diagnostic and control functions that make it particularly suitable for microprocessor based systems.

BLOCK DIAGRAM

The block diagram shows the DMOS power transistor and the PWM control loop. Integrated functions include a reference voltage trimmed to 5.1V ± 2%, soft start, undervoltage lockout, oscillator with feedforward control, pulse by pulse current limit, thermal shutdown and finally the reset and power fail circuit. The reset and power fail circuit provides an output signal for a microprocessor indicating the status of the system.

Device turn on is around 11V with a typical 1V hysteresis, this threshold provides a correct voltage for the driving stage of the DMOS gate and the hysteresis prevents instabilities.

An external bootstrap capacitor charged to 12V by an internal voltage reference is needed to provide correct gate drive to the power DMOS. The driving circuit is able to source and sink peak currents of around 0.5A to the gate of the DMOS transistor. A typical switching time of the current in the DMOS transistor is 50ns. Due to the fast commutation switching frequencies up to 500kHz are possible.

The PWM control loop consists of a sawtooth oscillator, error amplifier, comparator, latch and the output stage. An error signal is produced by comparing

Figure 1 : Feedforward Waveform.

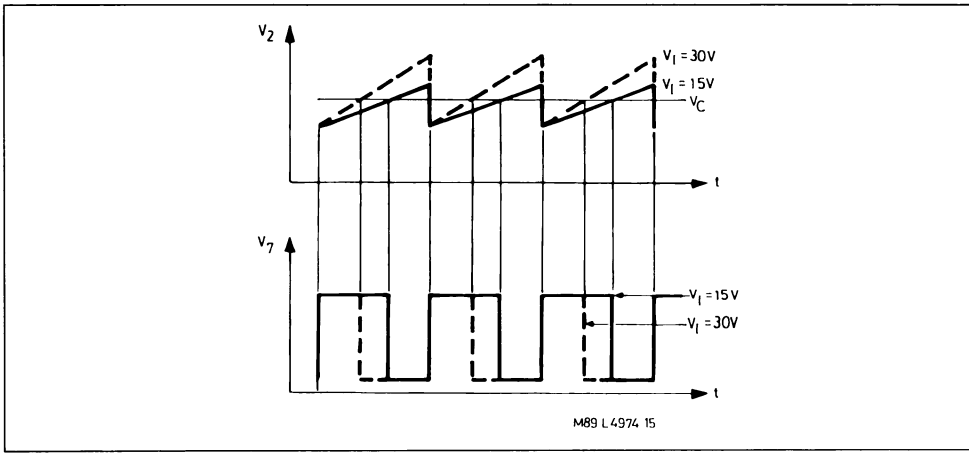


Figure 2 : Soft Start Function.

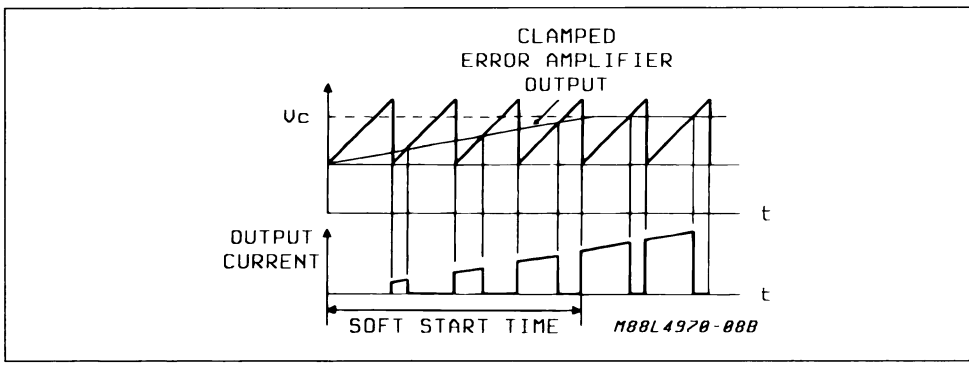
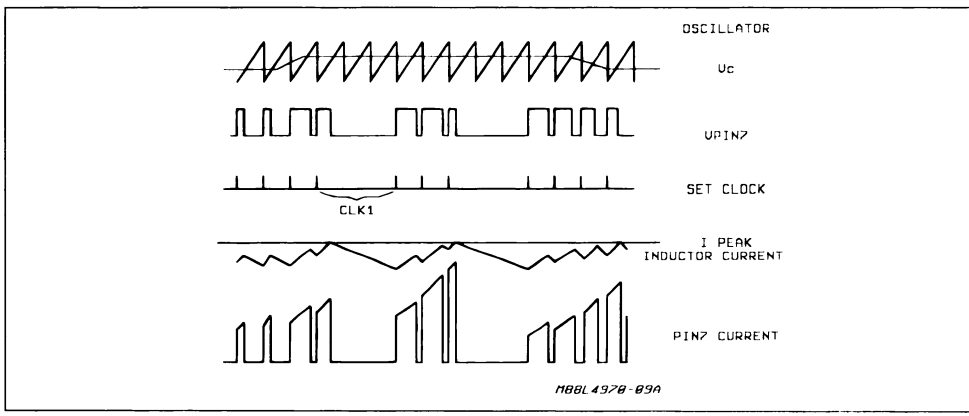


Figure 3 : Limiting Current Function.



the output voltage with the precise 5.1V ± 2% on chip reference. This error signal is then compared with the sawtooth oscillator in order to generate fixed frequency pulse width modulated drive for the output stage. A PWM latch is included to eliminate multiple pulsing within a period even in noisy environments. The gain and stability of the loop can be adjusted by an external RC network connected to the output of the error amplifier. A voltage feedforward control has been added to the oscillator, this maintains superior line regulation over a wide input voltage range. Closing the loop directly gives an output voltage of 5.1V, higher voltages are obtained by inserting a voltage divider.

At turn on output overcurrents are prevented by the soft start function (fig. 2). The error amplifier is initially clamped by an external capacitor Css and allowed to rise linearly under the charge of an internal constant current source.

Output overload protection is provided by a current limit circuit. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold the output of the comparator sets a flip flop which turns off the power DMOS. The next clock pulse, from an internal 40kHz oscillator will reset the flip flop and the power DMOS will again conduct. This current protection method, ensures a constant current output when the system is overloaded or short circuited and limits the switching frequency, in this condition, to 40kHz.

The Reset and Power fail circuitry (fig 4) generates an output signal when the supply voltage exceeds a threshold programmed by an external voltage divider. The reset signal, is generated with a delay time programmed by an external capacitor on the delay pin. When the supply voltage falls below the threshold or the output voltage goes below 5V the reset output goes low immediately. The reset output is an open collector-drain.

Fig 4A shows the case when the supply voltage is higher than the threshold, but the output voltage is not yet 5V.

Fig 4B shows the case when the output is 5.1V but the supply voltage is not yet higher than the fixed threshold.

The thermal protection disables circuit operation when the junction temperature reaches about 150C and has an hysterysis to prevent unstable conditions.

Figure 4 : Reset and Power Fail Functions.

A

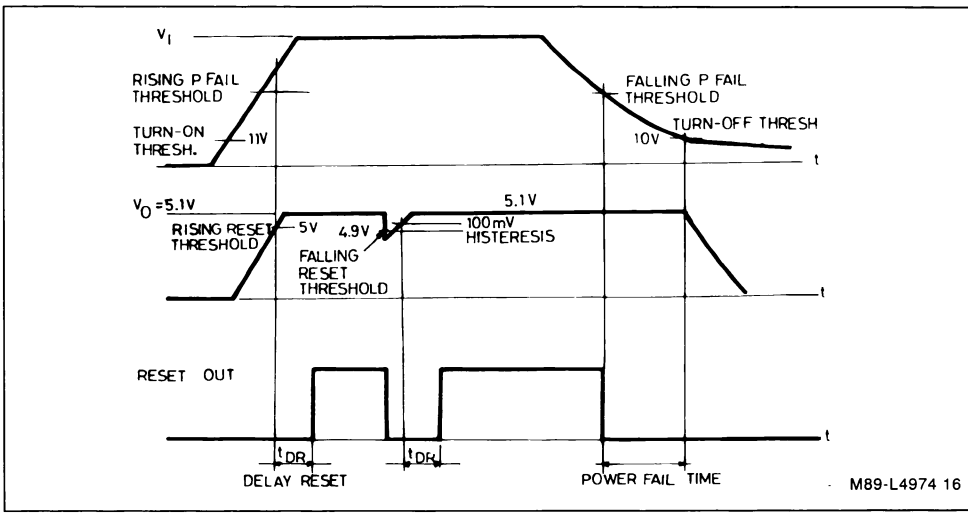
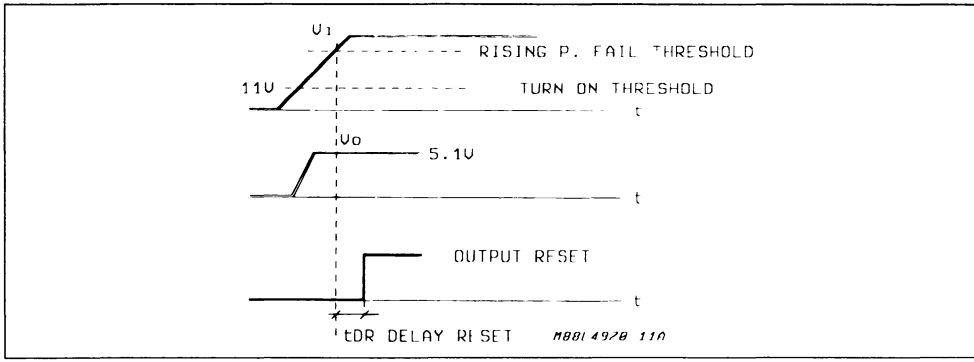


Figure 4 : Reset and Power Fall Functions (continued).

B



ELECTRICAL CHARACTERISTICS (refer to the test circuit, T_j = 25°C, V_i = 35V, R_4 = 15KΩ, C_9 = 2.2nF, f_{sw} = 200KHz typ, unless otherwise specified)

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_i	Input Volt. Range (pin 9)	V_o = V_{ref} to 40V I_o = 7A	15		50	V	5
V_o	Output Voltage	V_i = 15V to 50V I_o = 3A ; V_o = V_{ref}	5	5 1	5.2	V	5
ΔV_o	Line Regulation	V_i = 15V to 50V I_o = 2A , V_o = V_{ref}		12	30	mV	5
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 3A to 5A I_o = 2A to 7A		 10 20	 25 40	 mV mV	5
V_d	Dropout Voltage between Pin 9 and 7	I_o = 3A I_o = 7A		0 4 0 8	0.6 1 8	V V	5
I_{7L}	Max Limiting Current	V_i = 15V to 50V V_o = V_{ref} to 40V	8	9	10	A	5
Efficiency		I_o = 3A V_o = V_{ref} V_o = 12V	80	85 92		 % %	5
		I_o = 7A V_o = V_{ref} V_o = 12V	75	80 87		 % %	5
SVR	Supply Voltage Ripple Reject	V_i = 2VRMS , I_o = 3A f = 100Hz ; V_o = Vref	56	60		dB	5
f	Switching Freq		180	200	220	KHz	5
$\Delta f/\Delta V_i$	Volt Stability of Switching Freq	V_i = 15V to 45V		2	6	%	5
$\Delta f/T_j$	Temp. Stability of Switch Freq.	T_j = 0 to 125°C		1		%	5
f_{max}	Max Operating Switch. Freq	V_o = V_{ref} ; R_4 = 9.1KΩ I_o = 7A ; C_9 = 1 2nF	500			KHz	5

ELECTRICAL CHARACTERISTICS (continued)

V_{REF} SECTION (pin 14)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{REF}	Reference Voltage		5	5 1	5 2	V	7
ΔV_{REF}	Line Regulation	V_i = 15V to 50V V_{12} = 0		10	25	mV	7
ΔV_{REF}	Load Regulation	I_{REF} = 0 to 3mA		20	40	mV	7
$\Delta V_{REF}/\Delta T$	Average Temp. Coeff Ref Voltage	T_j = 0°C to 125°C		0 4		mV/C	7
I_{REF}	Short Circuit Curr Limit	V_{REF} = 0		70		mA	7

V_{START} SECTION (pin 15)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{ref}	Reference Voltage	P_{12} = 0V	11.4	12	12 6	V	7
ΔV_{ref}	Line Regulation	P_{12} = 0V ; V_i = 15 to 50V		0.4	1	V	7
ΔV_{ref}	Load Regulation	I_{ref} = 0 to 1mA P_{12} = 0V		50	200	mV	7
I_{ref}	Short Circuit Current Limit	P_{12} = 0V ; P_{15} = 0V		80		mA	7

DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{9on}	Turn–on Thresh.		10	11	12	V	7A
V_{9Hyst}	Turn–off Hyster.			1		V	7A
I_{9Q}	Quiescent Current	V_{12} = 0 ; S1 = D ; S2 = C ; S4 = A		10	16	mA	7A
I_{9OQ}	Operating Quiescent Curr.	V_{12} = 0		16	20	mA	7A
I_{7L}	Out Leak Current	V_i = 55V , S3 = A , V_{12} = 0V ,			2	mA	7A

SOFT START (pin 12)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
I_{12}	Soft Start Source Current	V_{12} = 3V ; V_{11} = 0V	70	100	130	µA	7B
V_{12s}	Output Saturation Voltage	I_{12s} = 20mA ; V_9 = 10V			0.7	V	7B

ERROR AMPLIFIER

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{10H}	High Level out Voltage	I_{10} = – 50µA , S2 = A P_{11} = 0V ; S1 = C	6			V	7C
V_{10L}	Low Level out Voltage	I_{10} = 50µA ; S2 = A P_{11} = 6V ; S1 = C			0 7	V	7C
I_{11}	Input Bias Current	V_{11} = 5 ; S1 = B , R_S = 10K		2	10	µA	7C
VOS	Input off Voltage	P_{11} = Vos ; R_s = 50Ω ; S1 = A		2	10	mV	7C
G_V	DC Open Loop Gain	P_{VCM} = 4V ; R_S = 50Ω , S1 = A	60			dB	7C
SVR	Supply Volt. Rej.	15 < V_I < 50V	60	80		dB	7C

ELECTRICAL CHARACTERISTICS (continued)

RAMP GENERATOR (pin 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	max.	Unit	Fig.
	Ramp Valley			1.5		V	7A
	Ramp Peak	V_i = 15V V_i = 45V		2 5 5 5		V V	7A
	Min Ramp Current	S1 = A , I1 = 100µA		270	300	µA	7A
	Max Ramp Current	S1 = A , I1 = 1mA	2.4	2 7		mA	7A

SYNC FUNCTION (pin 13)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SYNC	Low Input Voltage	V_i = 15V to 50V	– 0.3		0 9	V	
SYNC	High Input Voltage	V_{12} = 0	3 5		5 5	V	
$-I_{13L}$	Sync Input Current with Low Input Voltage	V_{13} = 0 9V			0.4	mA	
$-I_{13H}$	Input Current with High Input Voltage	V_{13} = 3.5V			1 5	mA	
SYNC	Delay			50		ns	
	Output Amplitude		4	5		V	
	Output Pulse Width	V_{thr} = 2 5V	0 3	0.5	0 8	µsec	

RESET AND P. FAIL FUNCTIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{11R}	Rising Threshold Voltage (pin 11)	V_i = 15 to 50V S1 = B	Vref – 120	Vref – 100	Vref – 80	V mV	7D
V_{11F}	Falling Threshold Voltage (pin 11)	V_I = 15 to 50V S1 = B	4.77	Vref –200	Vref –160	V mV	7D
V_{5H}	Delay High Threshold Voltage	S1 = B	5	5.1	5.2	V	7D
V_{5L}	Delay Low Threshold Voltage	S1 = B	1	1.1	1 2	V	7D
$-I_{5SO}$	Delay Source Current	V_3 = 5 3V ; V_5 = 3V S1 = A	40	55	70	µA	7D
I_{5SI}	Delay Sink Current	V_3 = 4.7V , V_5 = 3V S1 = A	10			mA	7D
V_{4S}	Out Saturation Voltage	I_4 = 15mA , S2 = B			0.4	V	7D
I_4	Output Leak Current	V_4 = 50V ; S2 = A			100	µA	7D
V_{3R}	Rising Threshold Voltage		5	5.1	5.2	V	7D
	Hysteresis		0.4	0.5	0.6	V	7D
I_3	Input Bias Current			1	3	µA	7D

Figure 5 : Test and Application Circuit.

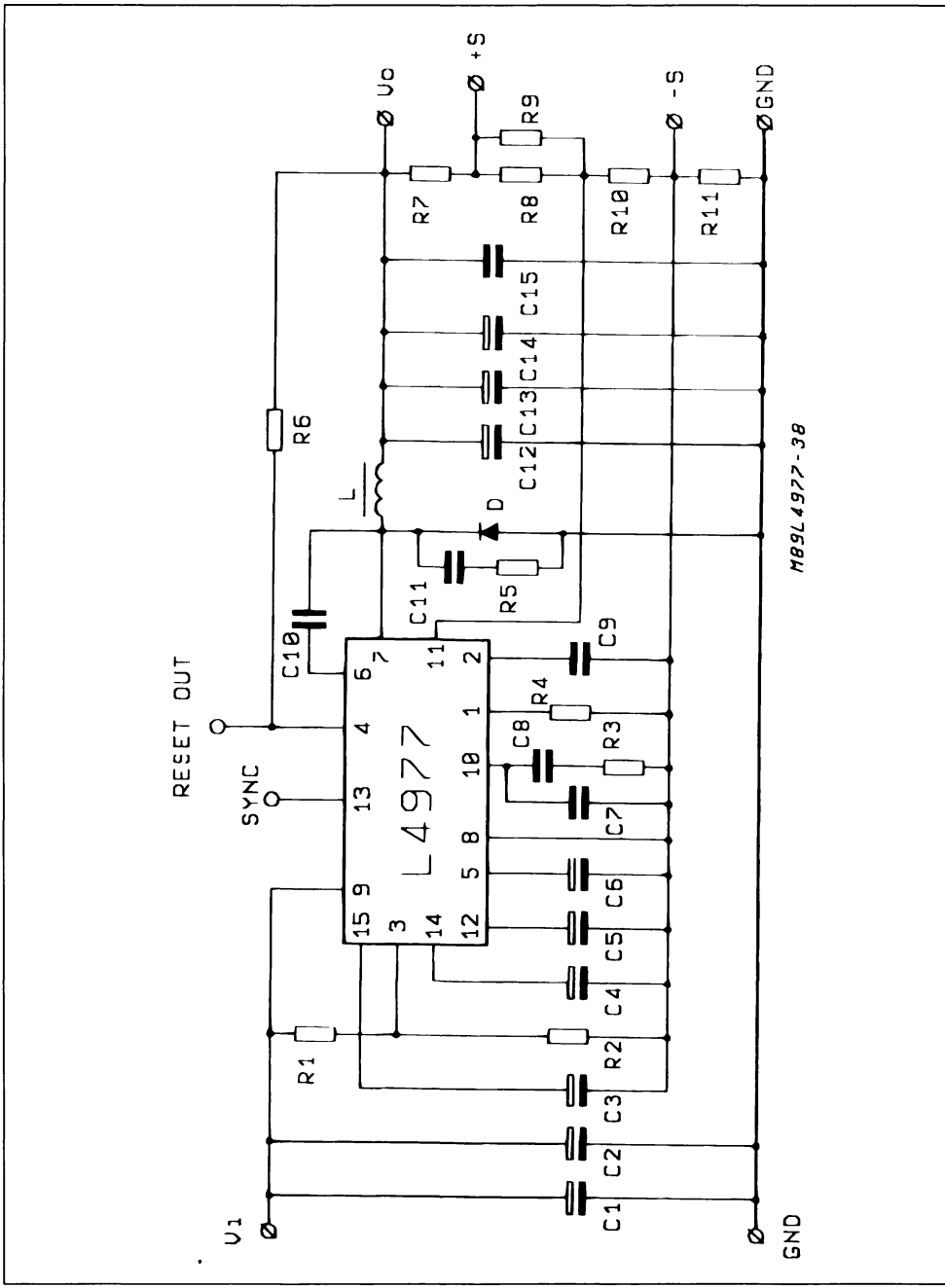
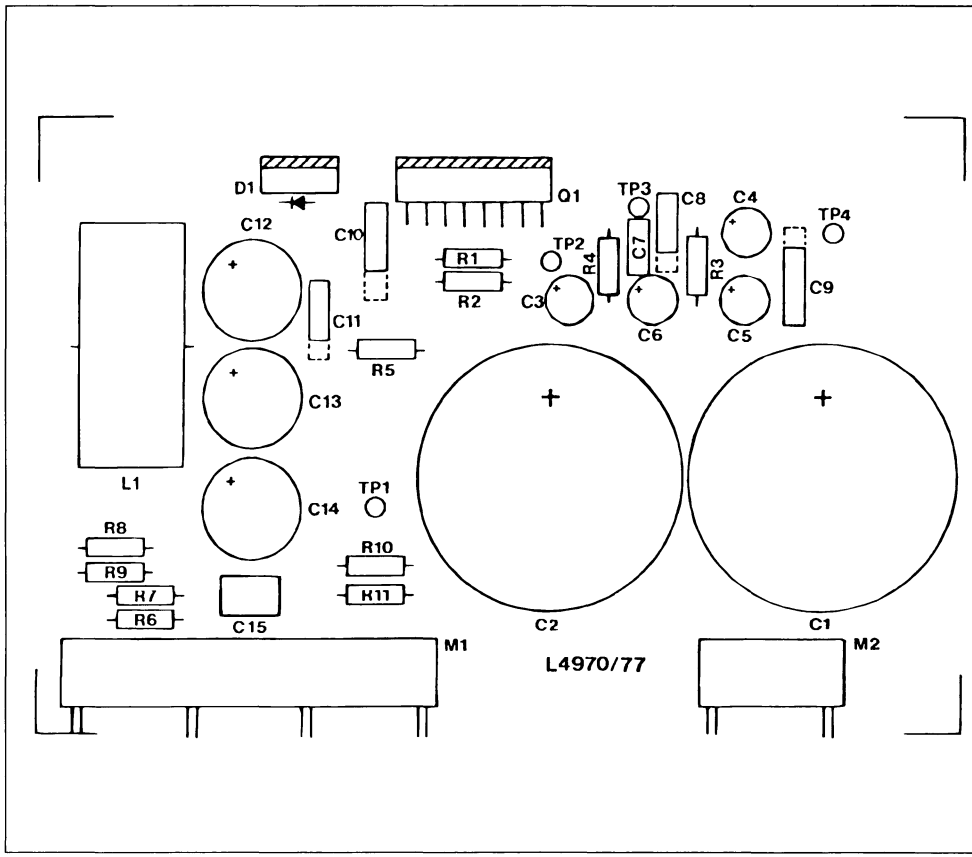


Figure 6 : Component Layout of Figure 5 (1 : 1 scale).



PARTS LIST

R_1 = 30KΩ
R_2 = 10KΩ
R_3 = 22KΩ
R_4 = 15KΩ
R_5 = 22Ω 0,5W
R_6 = 4K7
R_7 = 10Ω
R_8 = see table A
R_9 = OPTION
R_{10} = 4K7
R_{11} = 10Ω
C_1, C_2 = 3300µF 63V_L EYF (ROE)
C_3, C_4, C_5, C_6 = 2 2µF
C_7 = 330pF Film
C_8 = 22nF MKT 1817 (ERO)
C_9 = 2.2nF KP1830
C_{10} = 0 1µF MKT
C_{11} = 2 2nF MP1830
**C_{12}, C_{13}, C_{14} = 220µF 40V_L EKR (ROE)
C_{15} = 1µF Film
D = SBP 1660T (or 16A/60V equivalent)
L = 40µH cote 58894 MAGNETICS
27 TURNS Ø 1,3mm (AWG 16)
COGEMA 949178

* 2 capacitors in parallel to increase input RMS current capability
** 3 capacitors in parallel to reduce total output ESR

Table A.

V0	R10	R8
12V	4.7KΩ	6.2KΩ
15V	4.7KΩ	9 1KΩ
18V	4.7KΩ	12KΩ
24V	4.7KΩ	18KΩ

Figure 7 : DC Test Circuits.

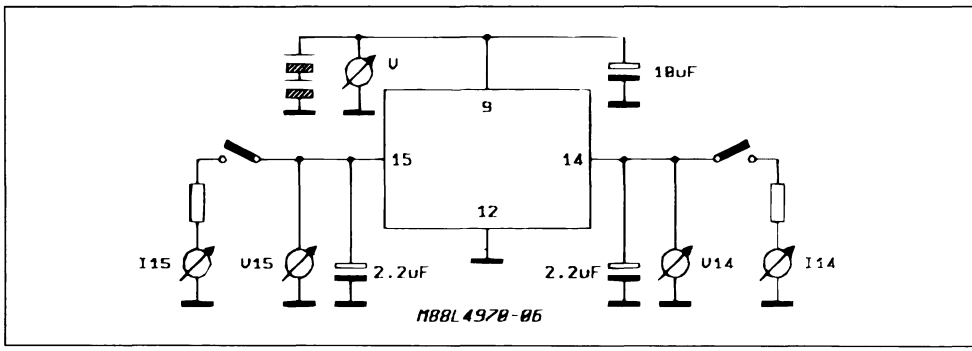


Figure 7A.

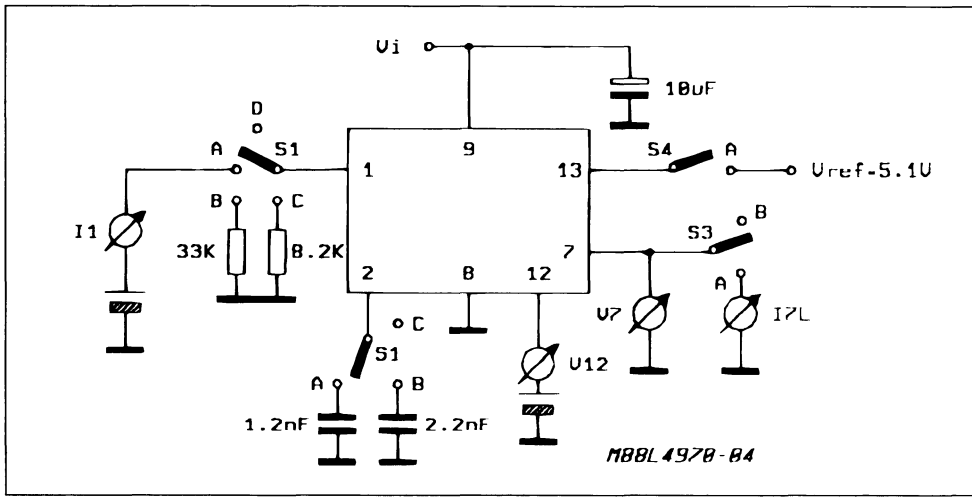


Figure 7B.

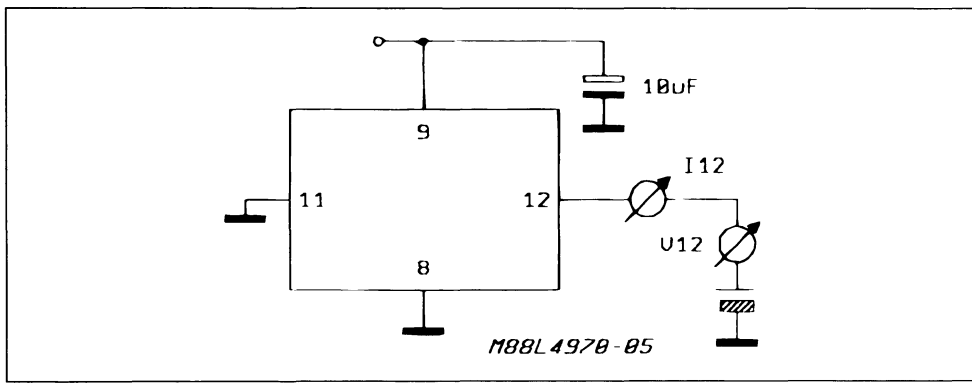


Figure 7C.

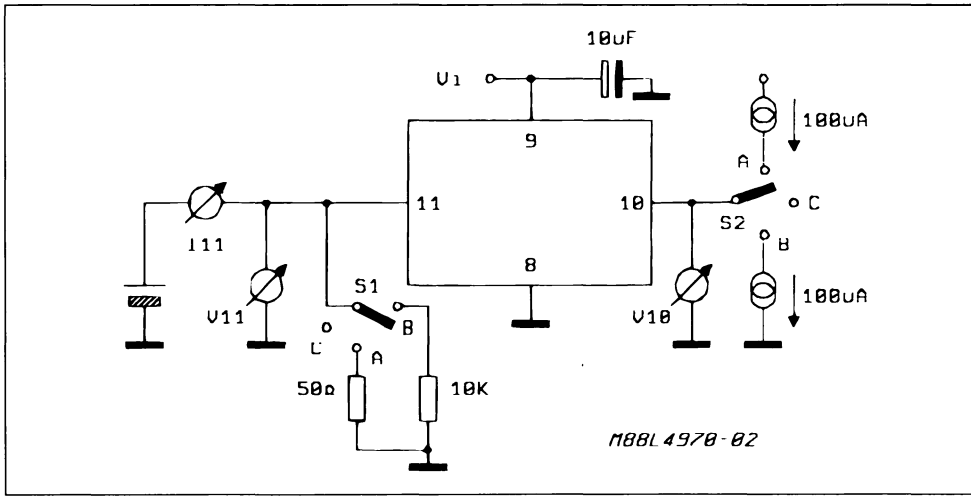


Figure 7D.

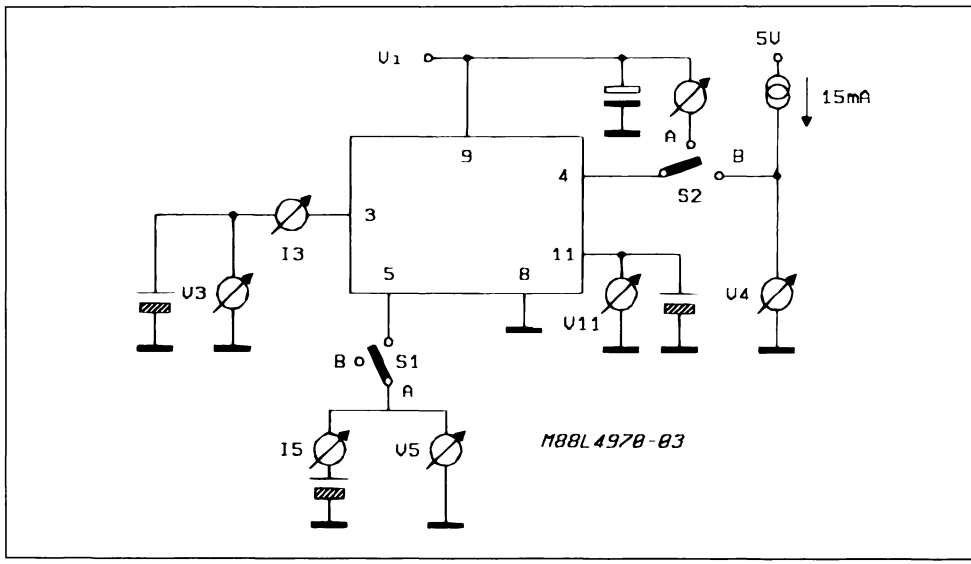


Figure 8 : Quiescent Drain Current vs. Supply Voltage (0% duty cycle - see fig. 7A).

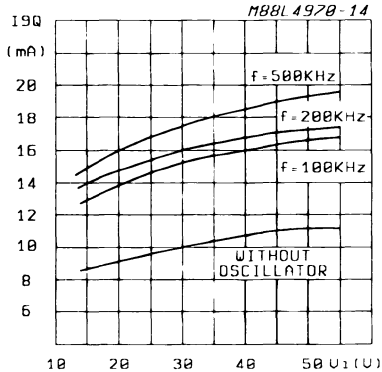


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0% duty cycle).

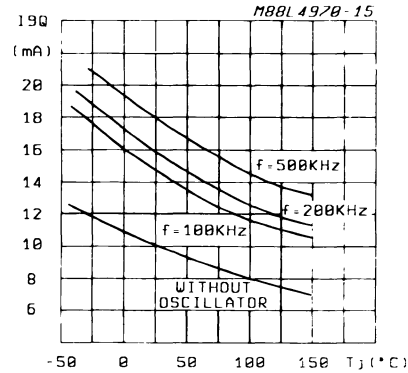


Figure 10 : Quiescent Drain Current vs. Duty Cycle

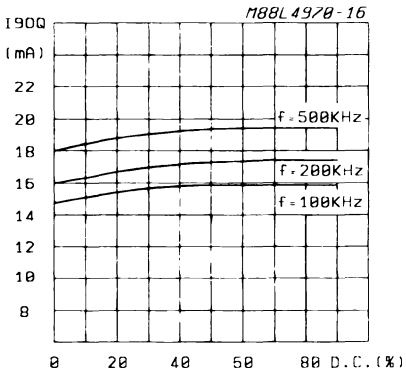


Figure 11 : Reference Voltage (pin 14) vs. V_i (see fig. 7).

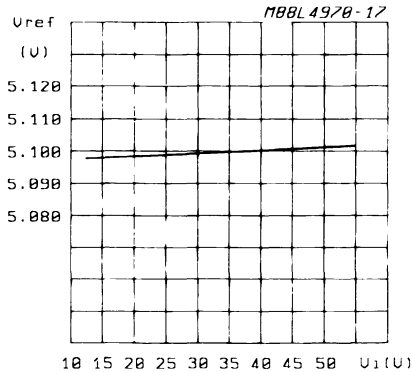


Figure 12 : Reference Voltage (pin 14) vs. Junction Temperature (see fig. 7).

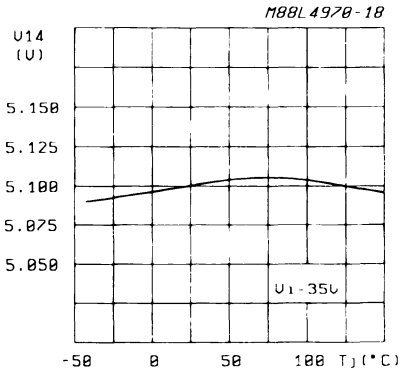


Figure 13 : Reference Voltage (pin 15) vs. V_i (see fig. 7).

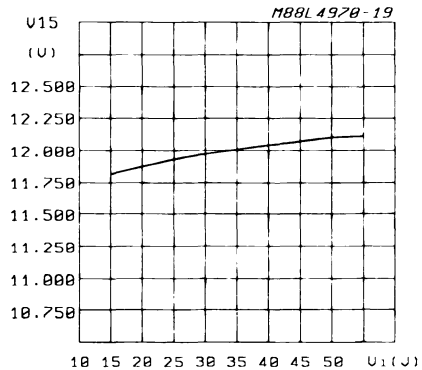


Figure 14 : Reference Voltage (pin 15) vs. Junction Temperature (see fig. 7)

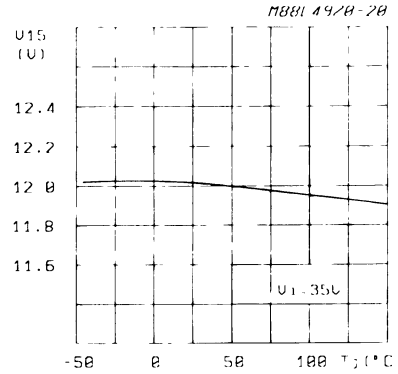


Figure 15 : Reference Voltage 5.1V (pin 14) Supply Voltage Ripple Rejection vs. Frequency.

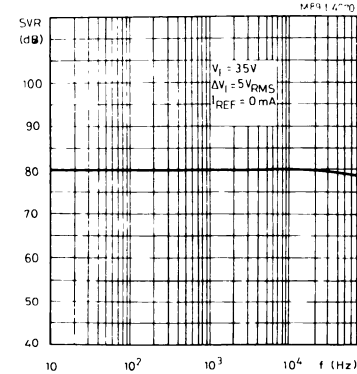


Figure 16 : Switching Frequency vs. Input Voltage (see fig. 5).

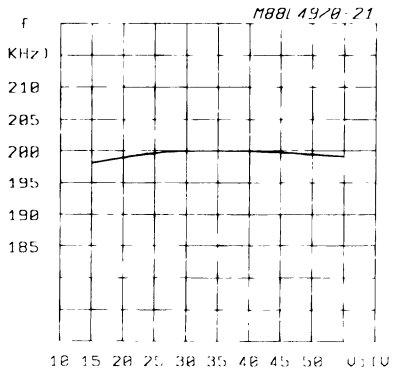


Figure 17 : Switching Frequency vs. Junction Temperature (see fig. 5).

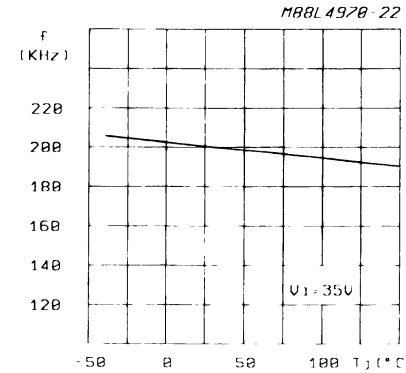


Figure 18 : Switching Frequency vs R4 (see fig. 5).

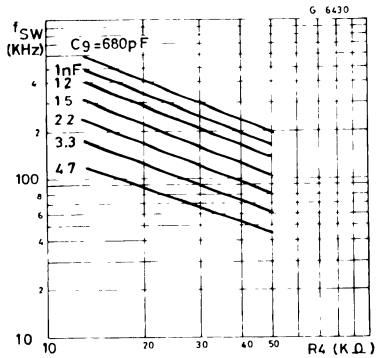


Figure 19 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 7C).

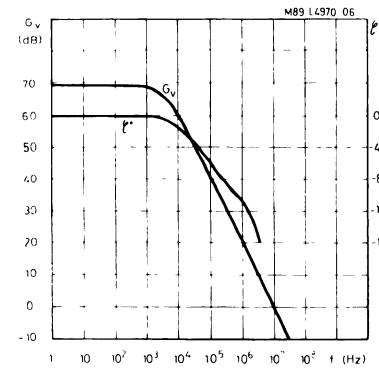


Figure 20 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 5).

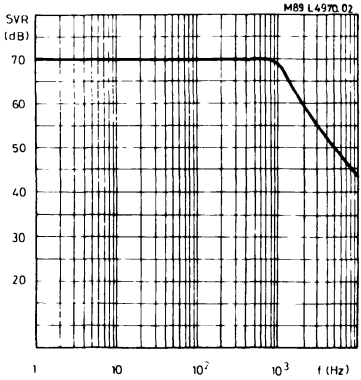


Figure 21 : Line Transient Response (see fig. 5).

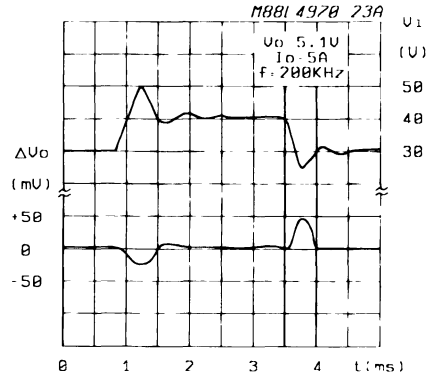


Figure 22 : Load Transient Response (see fig. 5).

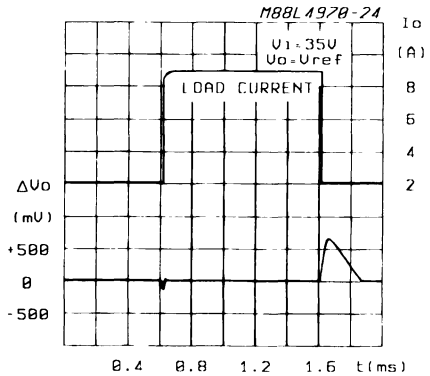


Figure 23 : Dropout Voltage Between Pin 9 and Pin 7 vs. Current at Pin 7.

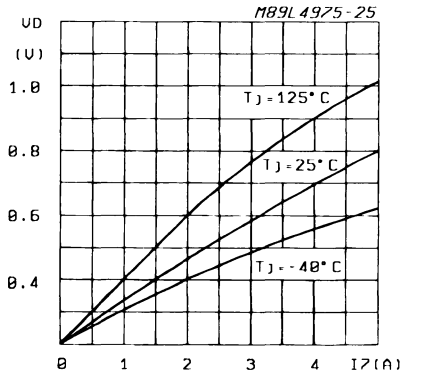


Figure 24 : Dropout Voltage Between Pin 9 and Pin 7 vs. Junction Temperature.

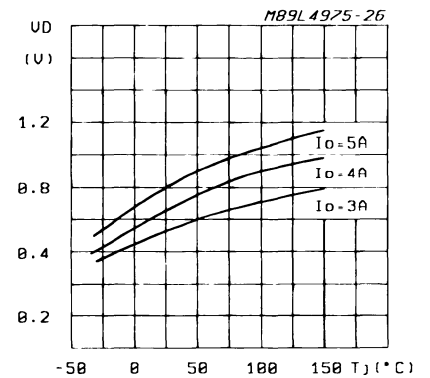


Figure 25 : Power Dissipation (device only) vs. Input Voltage.

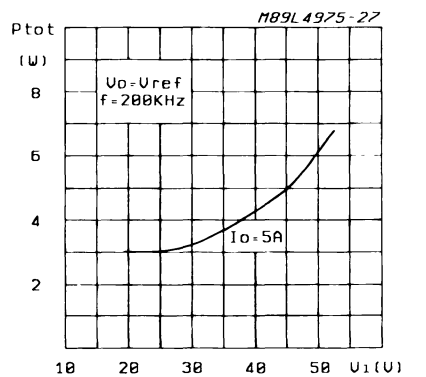


Figure 26 : Power Dissipation (device only) vs. Output Voltage.

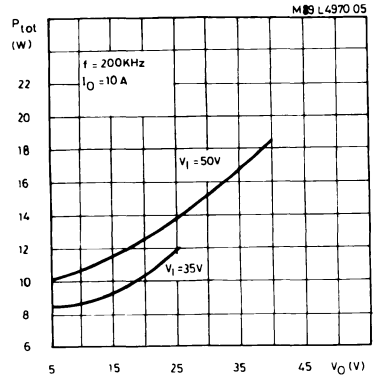


Figure 27 : Heatsink Used to Derive the Device's Power Dissipation (R_{th} – Heatsink = $T_{case} - T_{amb}$).

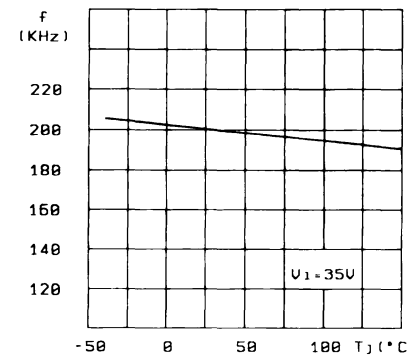


Figure 28 : Efficiency vs. Output Current.

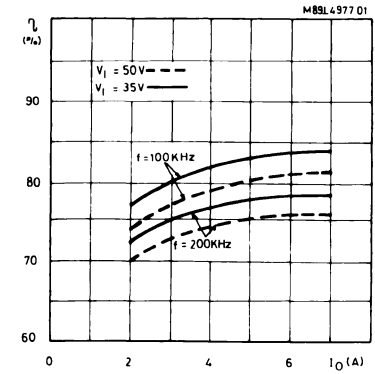


Figure 29 : Efficiency vs. Output Voltage.

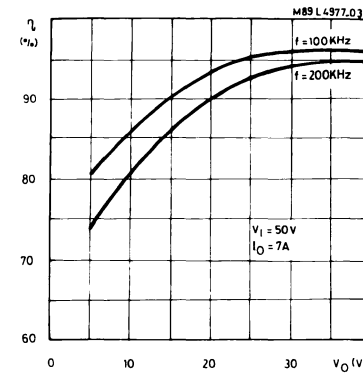


Figure 30 : Efficiency vs. Output Voltage.

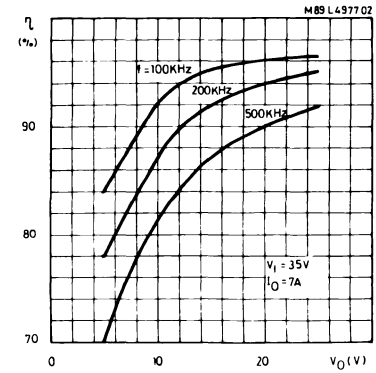


Figure 31 : Power Dissipation Derating Curve.

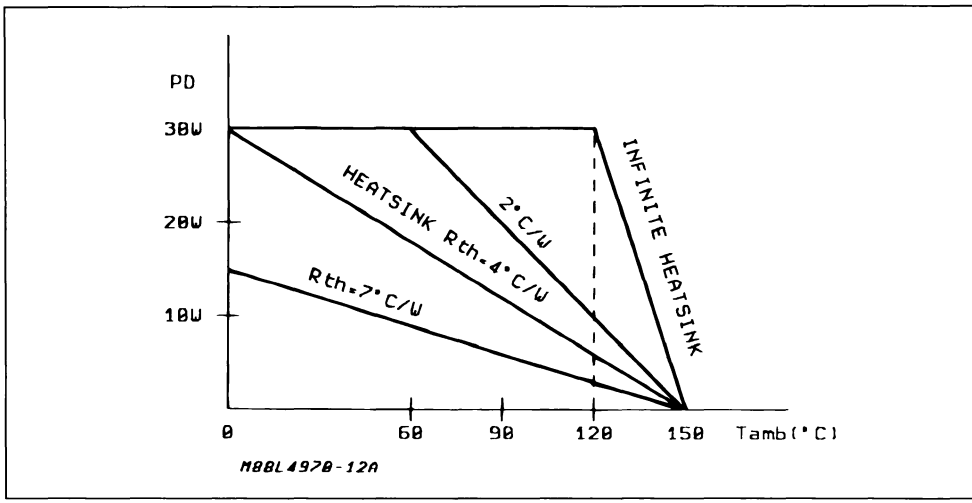
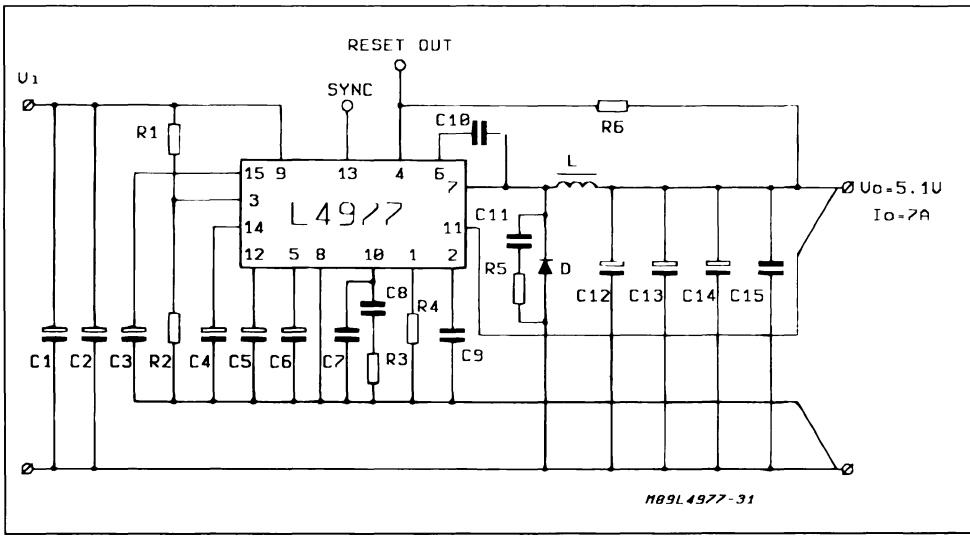


Figure 32 : 7A - 5.1V Application Circuit.



TYPICAL PERFORMANCES (using evaluation board) :

n = 83% (V_I = 35V ; V_O = V_{REF} ; I_O = 7A ; f_{SW} = 200KHz)

$V_{O\ RIPPLE}$ = 30mV (at 7A)

Line regulation = 5mV (V_i = 15 to 50V)

Load regulation = 15mV (I_o = 2 to 7A)

For component values, refer to test circuit part list.

Figure 33 : A 5.1V/12V Multiple Supply. Note the Synchronization between the L4970 and the L4974.

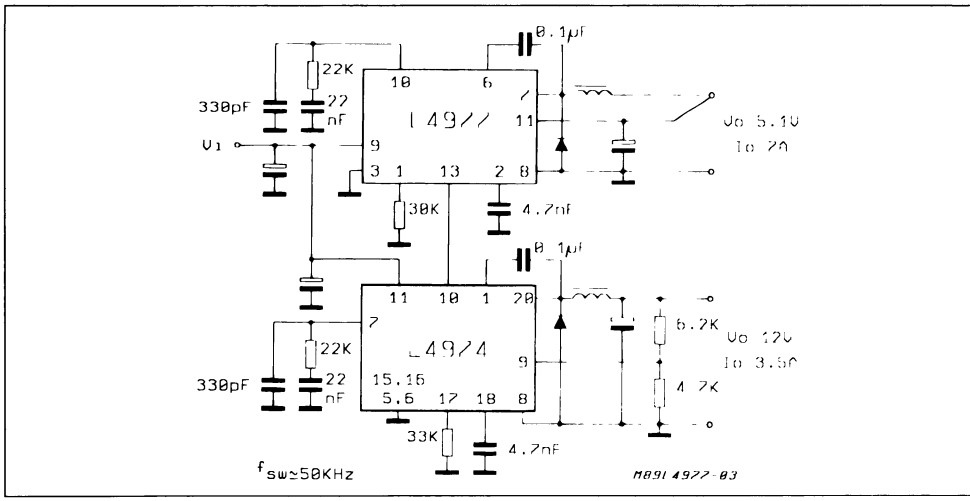


Figure 34 : L4970's Sync. Example.

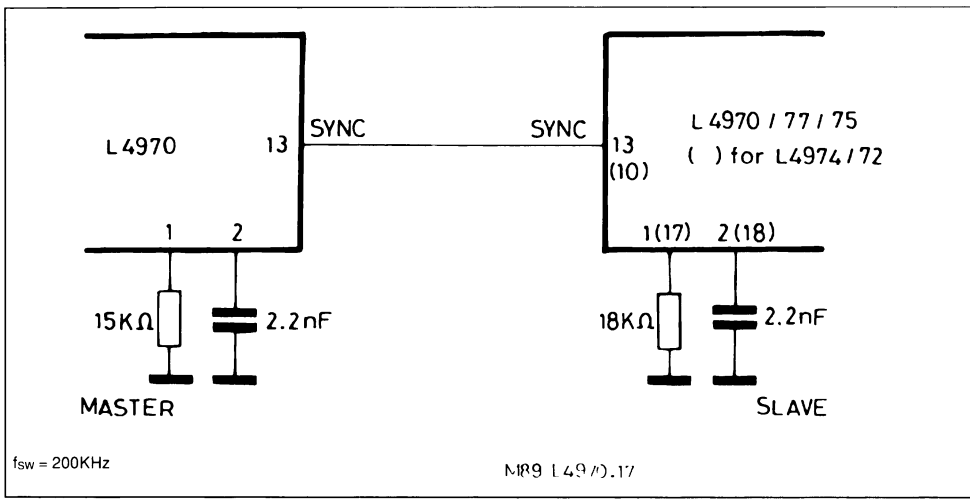
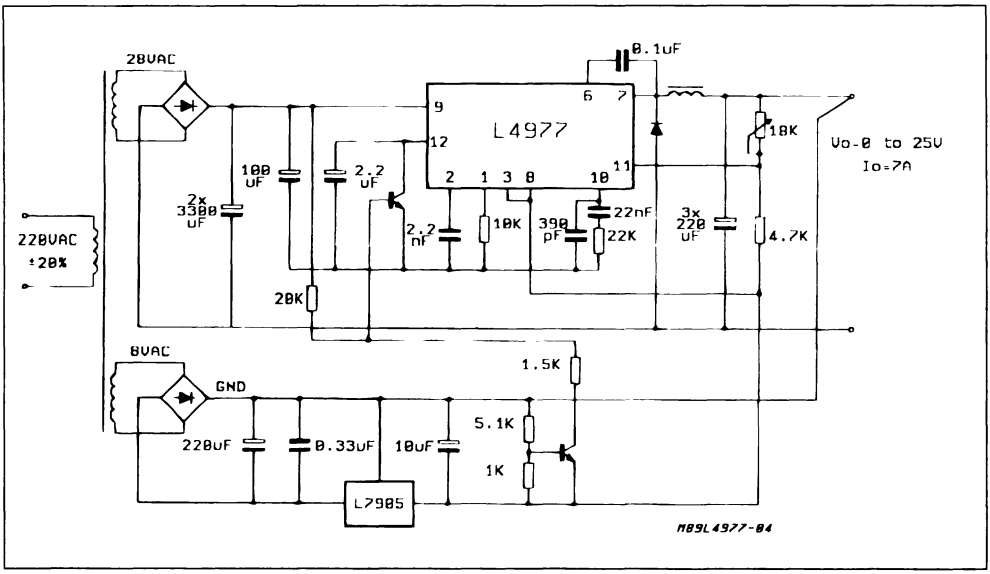


Figure 35 : 7A Switching Regulator, Adjustable from 0V to 25V.



APPLICATION NOTES

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

80W TO 400W MONOLITHIC BUCK REGULATORS INTEGRATED IN MULTIPOWER BCD TECHNOLOGY

By C. DIAZZI, G. GATTAVARI

Presented at the High Frequency Power Conversion Conference, San Diego, May 2-5th 1988

The paper describes recent developments in "intelligent" power integrated circuits realized in Bipolar, CMOS, DMOS (MULTIPOWER-BCD) mixed technology integrating both the control and power sections.

The new technology led to a new generation of monolithic switched mode power supplies in Buck configuration working at high switching frequency (up to 500KHz) and with output current in the range from 2A to 10A, at a supply voltage up to 55V.

Switched mode techniques led to the development of high efficiency circuits offering room saving and reduction in costs, mainly of heatsink and output LC filter.

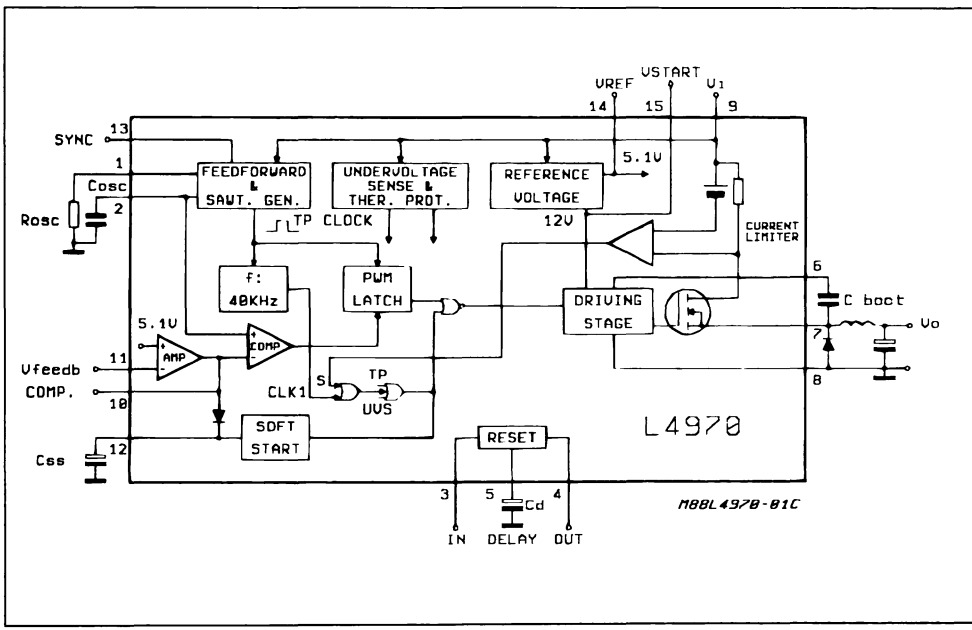
For these applications a new technology, called MULTIPOWER-BCD, has been developed which allows the integration on the same chip of isolated power DMOS elements, Bipolar transistors and CMOS logic.

The technology is particularly suitable for the problems arising in switching mode techniques field, due to the characteristics of high efficiency, fast switching speed, no secondary breakdown of the power DMOS element.

The great flexibility that we have at our disposal for the choice of the signal and driving sections components allows optimization and compactness of the system.

By MULTIPOWER-BCD it has been possible to implement the family L497X, a new series of fully integrated switching regulators suitable for DC-DC converters working in Buck configuration.

BLOCK DIAGRAM.



The complete family consists of five devices which differ each other only by the output current value (2A, 3.5A, 5A, 7A, 10A) they can deliver to the load.

The devices rated at 2A and 3.5A are assembled in Dual in Line package, Power Dip 16 + 2 + 2, while the others are assembled in Multiwatt 15 package. Each device integrates a DMOS output power stage, a control section, limiting current and supervisor functions like Reset and Power Fail signal for microprocessors applications.

Output voltage can be adjusted starting from the internal reference voltage (5.1V) up to 40V, allowing a maximum output power of 80W for the 2A version and of 400W for the 10A version.

Maximum operating supply voltage is 55V.

THE TECHNOLOGY

The technology architecture is based on the vertical DMOS silicon gate process that allows a channel length of 1.5μm ; using a junction isolation technique it has been possible to mix on the same chip Bipolar and CMOS transistors along with the DMOS power components.

Fig. 1 shows a cross section of the technology and table 1 lists the main electrical characteristics of the components.

TAB. 2 shows transistors density comparison between BCD and a standard Bipolar process capable to sustain the same voltage. The table shows that power bipolar component is cheaper in terms of silicon area than DMOS power component, but the disadvantage is largely compensated by the extremely simple circuitry required to drive the DMOS.

On the other side the table shows the compactness of signal components for BCD process that allows the implementation of complex control circuits.

Figure 1 : Technology Cross Section.

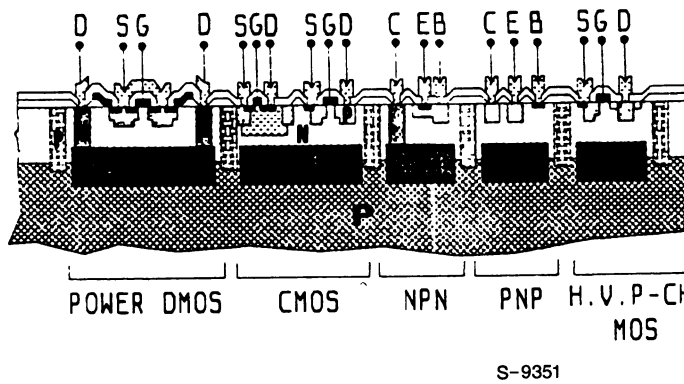


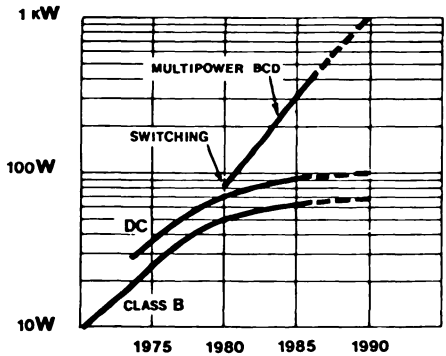
Table 1 : Electrical Characteristics.

Vertical DMOS	BV_{DSS} > 60V	V_{TH} = 3V	f_t = 1GHz
P-Channel Drain Ext.	BV_{DSS} > 75V	V_{TH} = 1.9V	f_t = 200MHz
CMOS N-Channel	BV_{DSS} > 15V	V_{TH} = 1V	
CMOS P-Channel	BV_{DSS} > 15V	V_{TH} = 1.9V	
Bipolar PNP	BV_{CEO} > 30V	β = 35	f_t = 10MHz
Bipolar NPN1	BV_{CEO} > 30V	β = 35	f_t = 300MHz
Bipolar NPN2	BV_{CEO} > 30V	β = 200	f_t = 150MHz

Table 2 : Transistors Density.

	MultipowerBCD Process(60V)	**Bipolar Process**(50V)
Power DMOS (1A/1V)	1mm²	
Power Bipolar (1A/1V)		0.7mm²
Signal Bipolar	200Tr./mm²	100Tr./mm²
CMOS	700Tr./mm²	

Figure 2 : Power Capability Progress of Power ICs.



The curves of fig. 2 show the progress in terms of power capability of power ICs as a function of years. In the 70's class B circuits and DC circuits allowed output power in the range of 70W.

In 1980 with the introduction of switching techniques in power IC's output power up to 200W were reached ; with the introduction of BCD technology output power increased up to 400W.

THE DEVICES : FUNCTIONS AND BLOCK DIAGRAM

The family of L497X products finds its typical application in those systems which require stabilized supply voltage starting from a non stabilized supply of 60V.

Such applications are typically found in personal computer systems, printers, typewriters and so on where for safety of working people a maximum supply voltage of 48V is allowed on the secondary side of the transformer which supplies the system.

The devices are used in step down configuration (buck converter) and can regulate output voltage from 5.1V up to 40V.

The circuits contain the power stage, control sections and diagnostic and protection circuits that make the devices particularly indicated to supply microprocessor based systems.

By integrating the power and control functions on a single monolithic chip a very compact and low cost system has been realized.

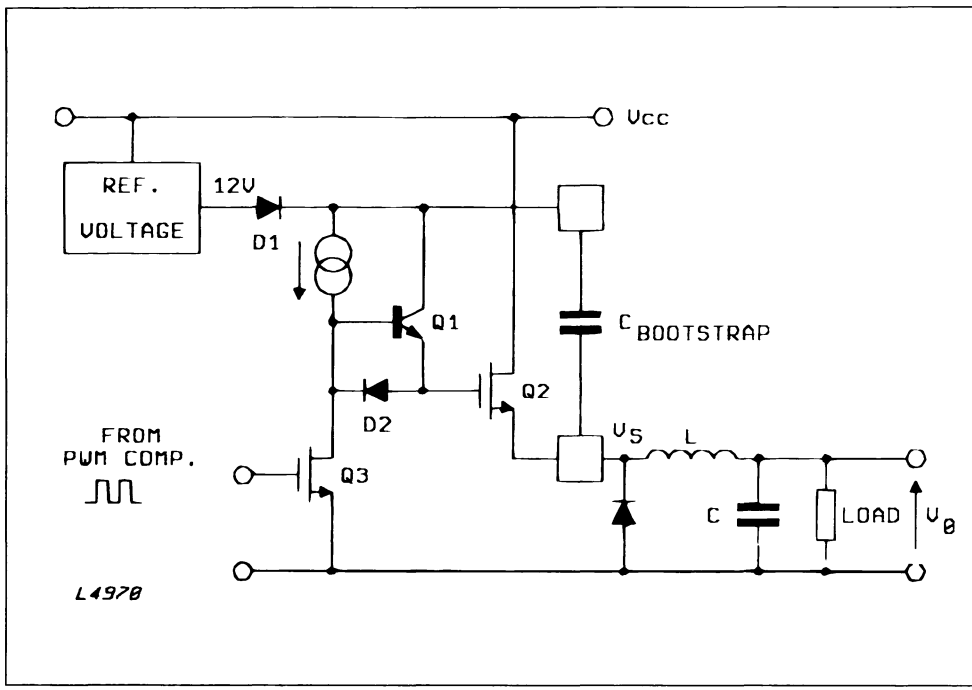
Additional cost and volume savings can be obtained since the high switching frequency (200-500KHz) offers significant savings in LC filter.
See the block diagram of the device at the first page of this note.

It includes a DMOS power stage with PWM control loop, soft start circuits, trimmed 5.1V voltage reference, under voltage lock out circuit, feedforward function, pulse by pulse current protection, thermal protection for the power stage and a Power Fail-Reset circuit which generates a Reset signal for a microprocessor.

The family of devices is rated at five different maximum output current levels to the load : 2A, 3.5A, 5A, 7A, 10A.

The first two devices are assembled in Dual in Line power package which needs no heatsink and which shows a thermal resistance junction to pin of 11°C/W.

Figure 3.



The last three devives are assembled in Multiwatt package which shows a thermal resistance of 1°C/W (j-case).

THE POWER STAGE

A semplified schematic of the output stage along with the external filter components is shown in fig. 3.

Power stage and its associated driving circuits are among the most critical components to achieve good performances at high switching frequency.

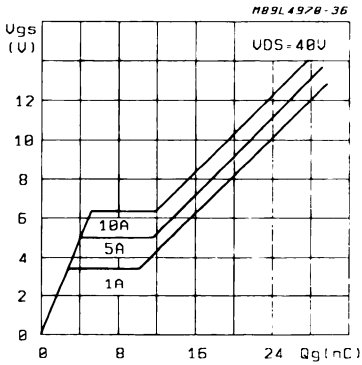
An external bootstrap capacitance, charged via diode D1 at 12V, is needed to provide the correct gate drive to the power DMOS N-channel transistor.

The driving circuit is able to deliver a current peak of 0.5A, during turn on and turn off phases, to the gate of power DMOS transistor.

Table 3 : Power DMOS Electrical Characteristics.

BV_{DSS} > 60V	at I_D = 1mA		V_{GS} = 0V
$R_{DS(ON)}$ = 100mΩ	at I_D = 10A	T_j = 25°C	V_{GS} = 10V
$R_{DS(ON)}$ = 150mΩ	at I_D = 10A	T_j = 150°C	V_{GS} = 10V
V_{TH} = 3V	at I_D = 1mA		

Figure 4 : GATE-CHARGE Curves for the Power DMOS.



The described circuit shows commutation times of 50ns.

The five devices of L497X family differentiate each other only for the level of current protection, while the control part is the same and power device area is the same to guarantee low power dissipation also for low current versions in Dual in Line package.

Table 3 shows electrical characteristics of the power DMOS implemented in the chip.

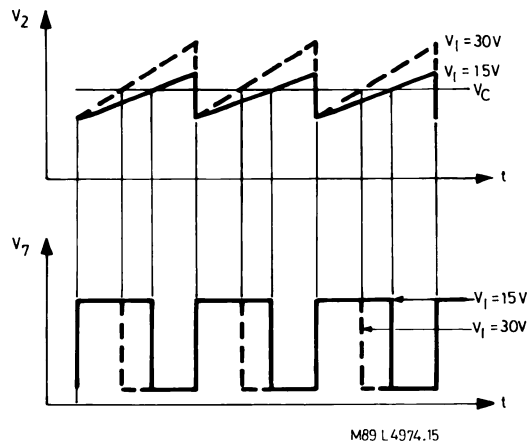
REGULATION LOOP

The regulation loop (block diagram) consists of a classical Pulse Width Modulation circuit and includes a sawtooth oscillator, error amplifier, voltage comparator and PWM latch.

A precision 5.1V voltage reference, trimmed on the chip to guarantee a tight 1% initial tolerance and 1% temperature range, is generated and constitutes the voltage reference for the loop. The error amplifier is a transconductance type with high impedance current output and the loop can be easily compensated by placing a resistor capacitor series network between amplifier output and ground (pole-zero compensation).

The soft start circuit incorporated in the device

Figure 5 : Voltage-feed-forward Technique.



allows the device to soft start the power stage after power up and after an inhibit state. The L497X devices feature a voltage feedforward technique, which is completely integrated and does not require any external component, that increases the slope of the sawtooth oscillator proportionally to the value of supply voltage Vcc.

As Vcc increases the output pulse width (transistor on time) decreases in such a manner as to provide a constant "volt-second" product to the inductance (fig. 5).

Freedom of Vo from Vcc minimizes error amplifier gain requirements while maintaining good output regulation.

The amplifier not compensated has a DC voltage gain $Av = g_m \cdot Ro = 70Db$ with $g_m = 1.3mA/V$ and $Ro = 3.3M\Omega$, $Co = 5pF$.

POWER FAIL-RESET CIRCUIT

L497X include a voltage sensing circuit that may be used to generate a power on power off reset signal for a microprocessor system.

The circuit senses the input supply voltage and the output generated voltage and will generate the required reset signal only when both the sensed voltages have reached the required value for correct system operation. The Reset signal is generated after a delay time programmable by an external capacitor on the delay pin.

Fig. 6 shows the circuit implementation of Reset circuit.

The supply voltage is sensed on an external pin, for programmability of the threshold, by a first comparator.

The second comparator has the reference threshold set at slightly less the ref. voltage for the regulation circuit and the other input connected internally at the feedback point on the error amplifier.

This allows to sense the output regulated voltage.

When both the supply voltage and the regulated voltage are in the correct range, transistor Q1 turns off and allows the current generator to charge the delay capacitor.

When the capacitor voltage reaches 5V the output Reset signal is generated. A latch assures that if a spike is present on the sensed voltage the delay capacitor discharges completely before initialization of a new Reset cycle.

Figure 6 : Power Fail / Reset Circuit.

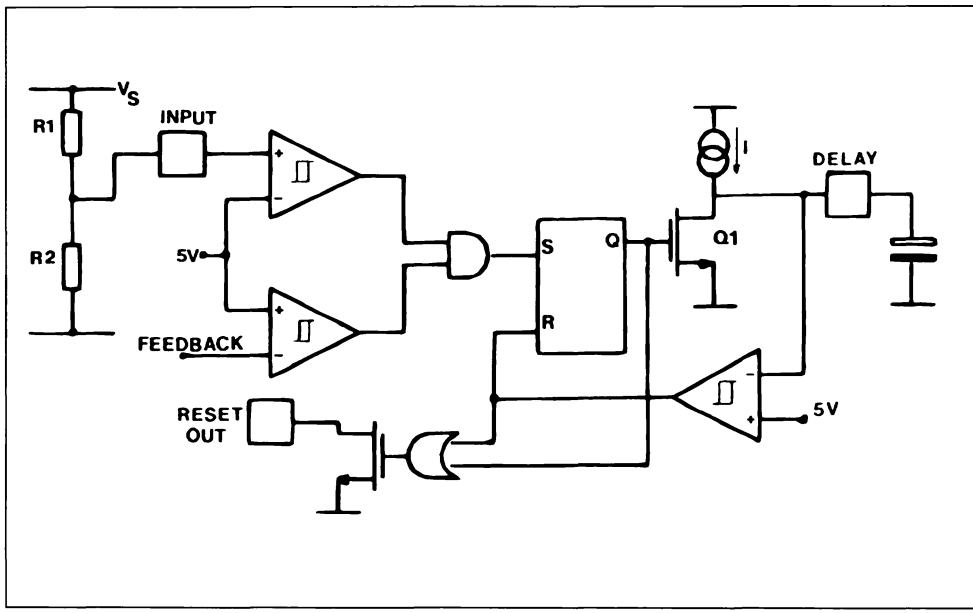
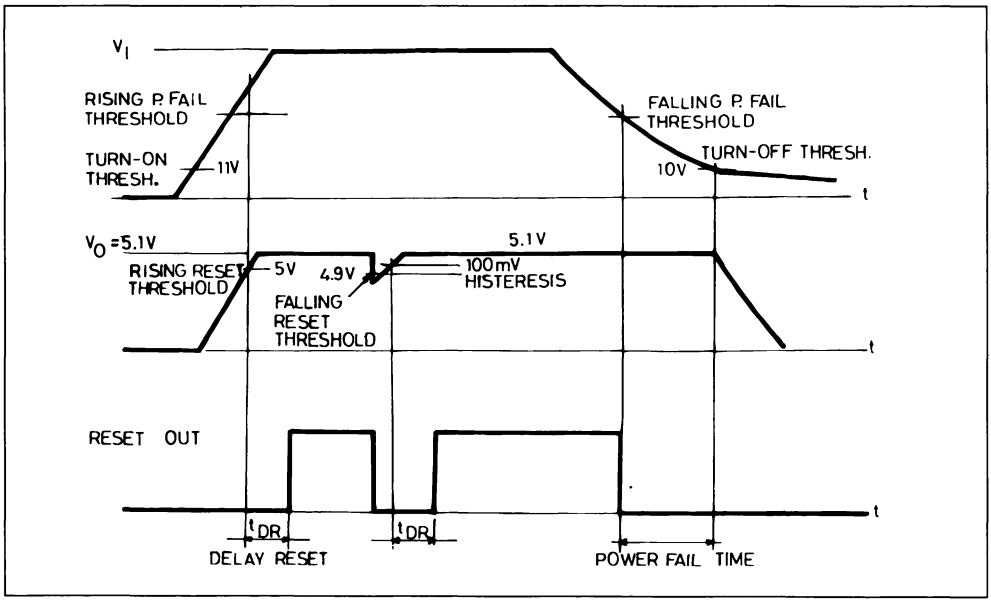


Figure 7 : Reset Waveforms.



The output gate assures immediate take of reset signal without waiting for complete discharge of delay capacitor.

Reset output is an open collector transistor capable of sinking 20mA at 200mV voltage.
Fig. 7 shows reset waveforms.

THERMAL CONSIDERATIONS

Power losses in the switched mode devices are given by three major contributions : DC losses of the power stage, switching losses of the power stage and quiescent losses of control circuit.

DC losses of the power stage are given by the following relationship :

$P_{DC} = R_{DS(ON)} \cdot I^2 \cdot \delta$ $\quad \delta$ = Duty cycle (1)

Switching losses of the power stage are given by the following relationship assuming square waveform for DRAIN-SOURCE voltage and triangular waveform for DRAIN current (inductive load) :

$P_{DS} = (1/2\ Vcc \cdot I_D \cdot t_{rise} + 1/2\ Vcc\ I_D \cdot t_f) \cdot f_{switch}$ (2)

Quiescent current drawn from Vcc to supply driving and control circuits is Iq = 12mA. Power dissipation due to quiescent current is given by :

$P_{DQ} = Vcc \cdot I_q$ (3)

L497X family consists of 5 devices differentiating for the level of output current and for the package in which they are included.

TABLE 4 shows the current capability and type of package for the 5 devices :

Table 4.

Type	Current Limit (internally set)	Package	$R_{thj\text{-}c}$
L4972	2.7A ± 10%	D.I.P. 16 + 2 + 2	11°C/W
L4974	4.5A ± 10%	D.I.P. 16 + 2 + 2	11°C/W
L4975	6.3A ± 10%	Multiwatt 15	1°C/W
L4977	8.8A ± 10%	Multiwatt 15	1°C/W
L4970	12A ± 10%	Multiwatt 15	1°C/W

L4972 and L4974 are assembled in a Dual in Line package (power dip) with 4 pins mechanically connected to the copper frame of the package.

This allows to dissipate heat from the frame to external world by some dissipating copper area on the PC board, without heatsink on the package.

Fig. 8 shows Thermal Resistance junction to ambient as a function of copper dissipating area on the PC board.

As we can see from fig. 8 and 9 we have $R_{thj\text{-}pin}$ = 11°C/W, $R_{thj\text{-}a}$ = 35°C/W.

Thermal Resistance junction-case of Multiwatt package is 1°C/W for a dissipating silicon area of 30000mils^2.

Figure 8 : Thermal Resistance j-pin (DIP).

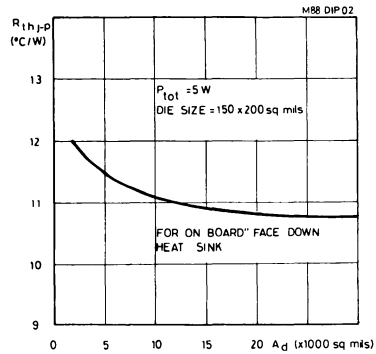
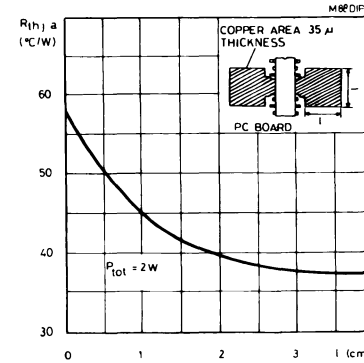


Figure 9 : Thermal Resistance j-ambient (DIP).



According to formula (1) (2) (3) and to Thermal Resistance Data we can calculate power dissipation and junction temperature for the 5 applications.

Assuming $R_{DS(ON)}$ = 0.15Ω T_j = 150°C ; t_{rise} = t_{fall} = 50ns ;

f_{switch} = 100KHz ; V_{CC} = 50V

we can consider the power dissipated in the following working conditions :

Table 5.

Type	P_O	P_{Dtot}	T_j (T_{amb} = 70°C)	
L4972	80W (2A, 40V)	1.58W	125°C	
L4974	70W (3.5A, 20V)	2.2W	147°C	
L4975	200W (5A, 40V)	4.85W	140°C	($R_{thj\text{-}a}$ = 14°C/W)
L4977	280W (7A, 40V)	8.23W	140°C	($R_{thj\text{-}a}$ = 8.5°C/W)
L4970	400W (10A, 40V)	15W	140°C	($R_{thj\text{-}a}$ = 5°C/W)

For chips in Multiwatt package it has been calculated the heatsink required to guarantee 140°C junction temperature.

For Power Dip package it has been calculated junction temperature knowing j-amb thermal resistance according to fig. 8 and 9.

The data show that MULTIPOWER BCD technology has allowed, with its outstanding features, the implementation of a complete switched mode power supply able to deliver about 80W in Dual in Line package without heatsink and 400W in Multiwatt package.

APPLICATION CIRCUIT

Fig. 10 shows typical application circuit for 10A device and in the table are listed the typical electrical characteristics and performances achieved.

Figure 10 : Application Circuit.

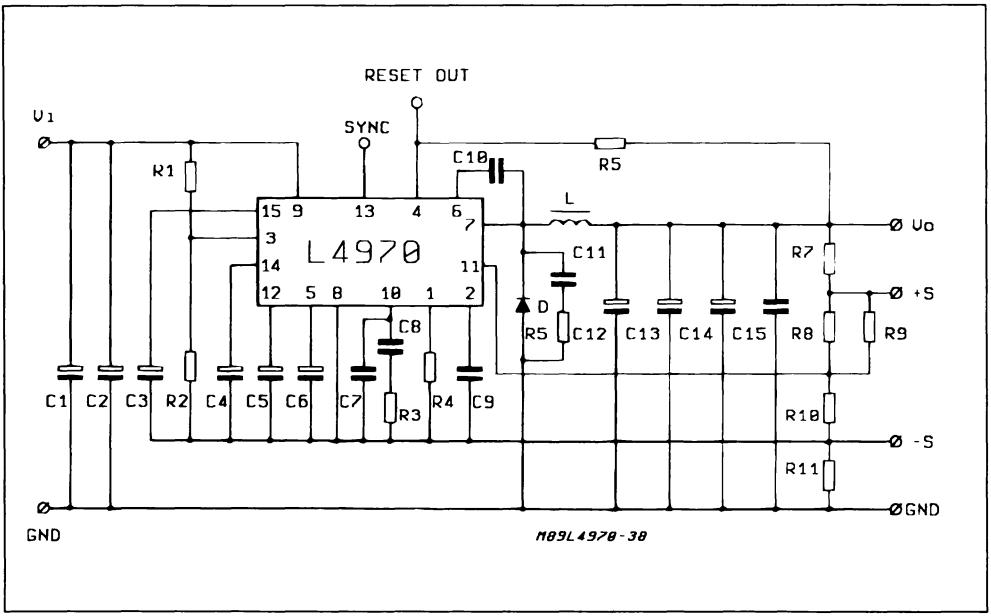


Table 6 : Electrical and System Characteristics.

Input Voltage		55V MAX
Output Current		10A (internally limited)
Reference Voltage		5.1V ± 10%
Temp. Stability of Ref. Volt.		0.2mV/°C
Line Regulation	V_i = 12V-50V	70dB
Ripple Rejection	f = 120Hz	60dB
Soft Start Time		20ms
Reset Delay Time		100ms
Switching Frequency		200kHz

Fig. 11 shows efficiency curves for 10A output current and fig.12 for 5A output current, as a function of output voltage and switching frequency.

Figure 11.

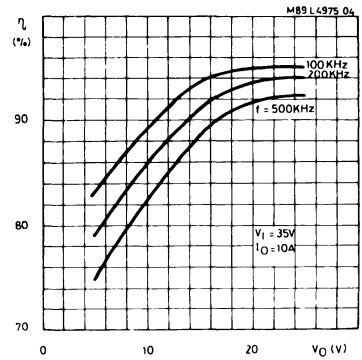


Figure 12.

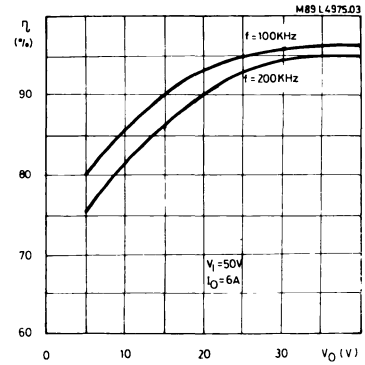
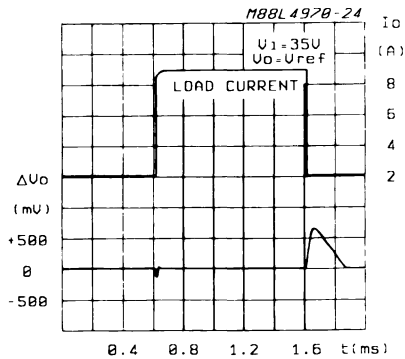


Fig. 13 shows a transient load condition from 2A to 8A and viceversa and the output voltage transient.

Figure 13 : Load Transient.



Lo = 50µH
Co = 300µF
Vo = 5.1V
Vi = 35V
f = 200KHz

CONCLUSIONS

A family of integrated Buck regulators realized in MULTIPOWER BCD technology has been presented.

The high efficiency characteristics of the devices implemented allows to deliver to the load 80W in a DIP package and 400W in a Multiwatt package working at high switching frequency (> 100KHz).

Future trends for MULTIPOWER BCD technology is the increase of breakdown voltage (250V, 500V) for the implementation of off-line systems.

ACKNOWLEDGMENTS

The authors whish to thank F. CONSIGLIERI, G. IZZO and L. PAGOTTO for the contribution given to prepare the material for the paper.

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THERMAL CHARACTERISTICS OF THE MULTIWATT PACKAGE

By R. TIZIANI

INTRODUCTION

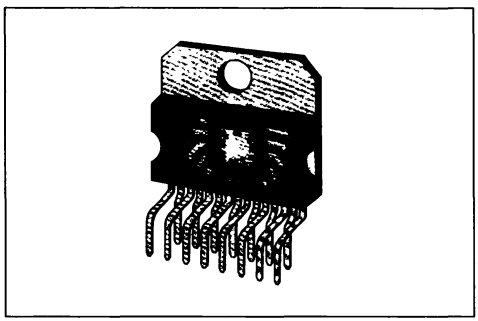
This Application Note provides a complete thermal characterization of the Multiwatt ® package (multilead double TO-220 - fig. 1).

Characterization is performed according with recomandations included in the G32-86 SEMI guideline, by means of a dedicated test pattern. It refers to :

1. Junction to case thermal resistance $R_{th(j-c)}$
2. Junction to ambient thermal resistance $R_{th(j-a)}$
3. Junction to ambient thermal impedance for single pulses and repated pulses, with different pulse width and duty cycle ;
4. Thermal resistance in DC and pulsed conditions, with a typical external heat sink.

Most of the experimental work is related to the thermal impedance, as required by the increasing use of switching techniques.

Figure 1 : Multiwatt Assembly.



EXPERIMENTAL CONDITIONS

The thermal evaluation was performed by means of the test pattern P432, which is a 20K mils^2 die with a dissipating element formed by two transistors working in parallel and one sensing diode. In order to characterize the worst case of a high power density IC, the total size of the element is 2K mils^2 with a power capability of 20W. Measurement method is described in Appendix A.

Samples with the indicated characteristics were prepared :

Package Multiwatt 15 leads

Frame Material	Copper
Slug Thickness	1.5mm
Slug Thermal Conductivity	3.9W/cm°C
Die Attach	Soft (PbSn)

Measurement of junction to case thermal resistance $R_{th(j-c)}$ is performed by holding the package against a water cooled heat sink, according with fig. 2. A thermocouple placed in contact with the slug measures the reference temperature of the case.

For junction to ambient thermal resistance $R_{th(j-a)}$ the samples are suspended horizontally in a one cubic foot box, to prevent drafts.

Both DC and pulsed conditions are used ; in the second case the contribution of package thermal capacitance is effective and transient thermal resistances much lower than the steady stata $R_{th(j-a)}$ can be found, according to pulse length and duty cycle.

The effect of the external heat sink is quantified, using as test vehicle the commercially available heat sink THM7023 especially developed by Thermalloy for the Multiwatt package, whose thermal resistance in still air is about 9°C/W.

The measurement circuit shown in fig. A3 was used for all the thermal evaluations.

JUNCTION TO CASE THERMAL RESISTANCE

The dependance of $R_{th(j-c)}$ on the dissipated power is reported in fig. 3.

It is well known that the main contribution to $R_{th(j-c)}$ of power packages in given by the silicon die.

Figure 2 : Measurement of $R_{th\ (j-c)}$.

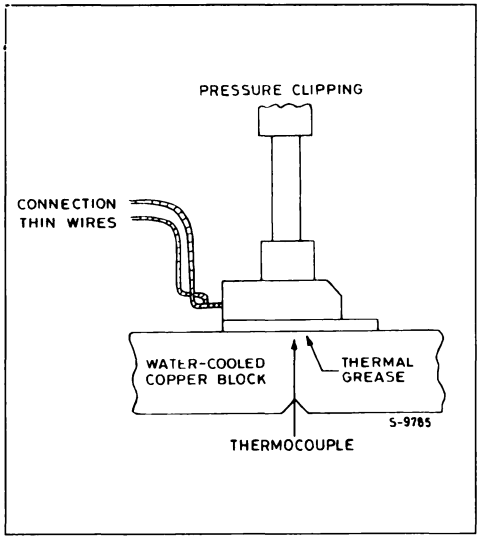
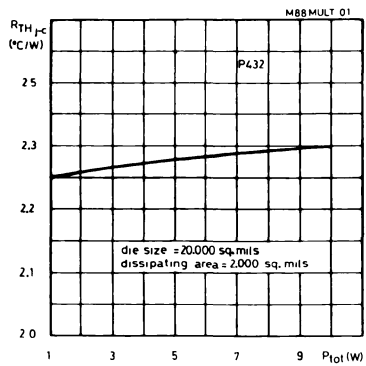


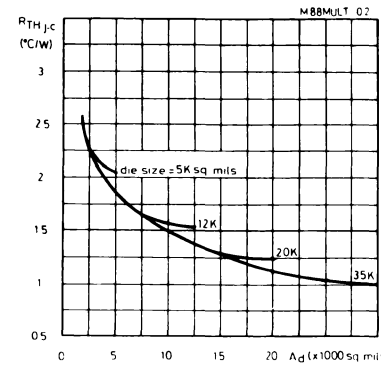
Figure 3 : $R_{th\ (j-c)}$ of Multiwatt Package vs. Power Level.



FOR DEVICES OTHER THAN THE TEST PATTERN P432 THE CALIBRATION CURVE OF FIG. 4 IS NEEDED.

It shows the relationship between $R_{th(j-c)}$ and the dissipating area existing on the silicon die (power diodes, power transistors, high current resistors), for different die sizes.

Figure 4 : $R_{th(j-c)}$ Thermal Resistance vs. Die Size and on Die dissipating Area.



JUNCTION TO AMBIENT THERMAL RESISTANCE

In medium power applications (1.5-2W), the Multiwatt package can be used without external heat sink, thanks to the significant size (about 3.5cm^2) of its integrated thermal mass.

Its $R_{th(j-a)}$ has two contributions : the $R_{th(j-c)}$, mainly due to the silicon die (as shown in fig. 4) and the thermal resistance of the copper slug $R_{th\ slug}$.

Figure 5 : $R_{th(j-a)}$ of Multiwatt Package vs. dissipated Power.

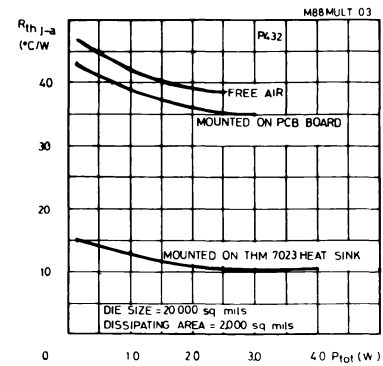


Fig. 5 gives the relationship between $R_{th(j-a)}$ and the power dissipation level for the P432 test pattern is still air, on PC board and on a commercial heat sink.

IN ORDER TO HAVE AN ACCURATE VALUE FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 5 SHOULD BE CORRECTED THROUGH THE CALIBRATION CURVE OF FIG. 4 CORRECTION TERM IS ALWAYS IN THE RANGE OF 0-2°C/W ; THEREFORE, IT AFFECTS THE $R_{th(j-a)}$ OF NO MORE THAN 5% IN STILL AIR OR WITH THE PACKAGE MOUNTED ON PC BOARD.

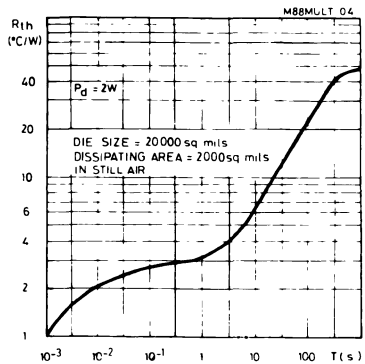
TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (without external heat sink)

The effect of single pulses of different length and height for the Multiwatt package without any external heat sink is shown in fig. 6.

This behaviour is discussed in Appendix B. Due to a significant thermal capacitance (C = 2J/°C) and correspondingly long risetime (τ = 80s), single pulses up to 30W can be delivered to the Multiwatt package for 1s with acceptable junction temperature increase.

IN ORDER TO HAVE ACCURATE R_{th} (t_o FOR OTHER DEVICES, WITH DIFFERENT DIE SIZE AND DISSIPATING AREA, VALUES OF FIG. 7 MUST BE CORRECTED AS DESCRIBED IN EXAMPLE 2 OF THE LAST SECTION.

Figure 6 : Transient Thermal Resistance for Single Pulse.



Repetition of pulses with defined P_d, period and duty cycle DC (ratio betwen pulse length and signal period), gives rise to oscillations in junction temperature as described in Appendix B.

The transient thermal resistance corresponding to the upper limit of the curve of fig. B4 (peak transient thermal resistance) is reported in fig. 7 and depends on pulse length and duty cycle. It can be noticed that DC becomes less effective for longer pulses.

TRANSIENT THERMAL RESISTANCE IN PULSED CONDITION (with external heat sink)

Characterization has been repeated with a commercial heat sink (Thermalloy THM7023) in order to have an example of the effect of an external thermal mass on the impedance of the thermal module.

Relationship between transient R_{th} and pulse length is reported in fig. 8.

The effect of the increased thermal capacitance is evident in fig. 9, where thermal data of fig. 6 and 8 are compared : it can be noticed that the curves are definitely different for pulses longer than 1s, corresponding about to the rise time of the slug. The effect of the thermal mass is to keep low the heating rate of the silicon die thus allowing a better power management of long power pulses. This conclusion has general validity and can be applied to other heat sinks than the one considered in this note.

Figure 7 : Peak Transient R_{th} vs. Pulse width and Duty Cycle.

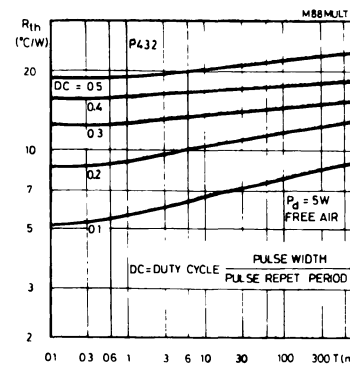


Figure 8 : Transient R_{th} for single pulses, with Heatsink.

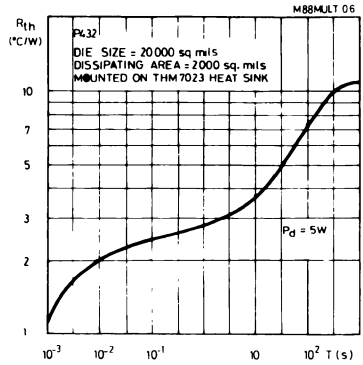
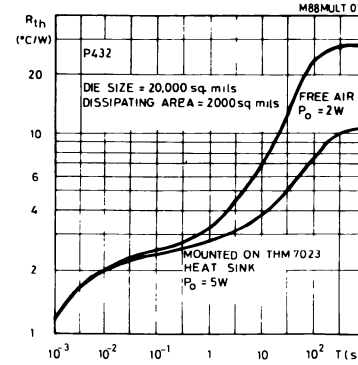


Figure 9 : Comparison of Transient R_{th} for single pulses, with and without Heat Sink.



APPENDIX A

The thermal resistance evaluation is performed with the especially designed test chip P432 which has two bipolar power transistor and one sensing diode (fig. A1). The active area is about 2000 $mils^2$ on a 35000$mils^2$ chip. Its lay-out was optimized in order to have a uniform temperature area, once the two transistor are powered ; the sensing diode is placed at the center of this area.

The relationship between the forward voltage V_f of the diode at the constant current of 100µA and the temperature is shown in fig. A2. The curve calibrates the junction temperature through the voltage drop of the diode.

The measurement circuit is shown in fig. A3. A storage oscilloscope or a fast digital voltmeter can be used for recording the V_f value.

Figure A1 : Test Pattern P432 Lay-out.

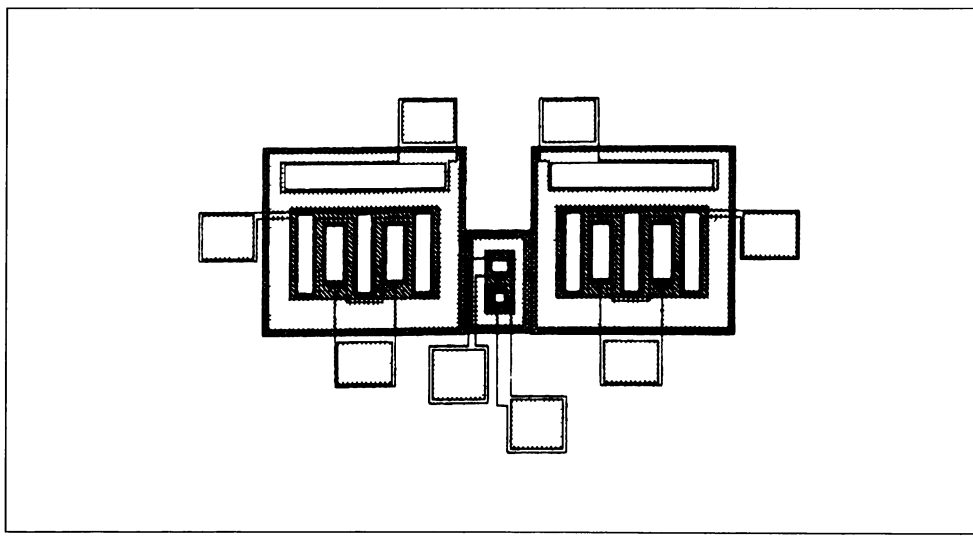


Figure A2 : Calibration Curse (sensing diode).

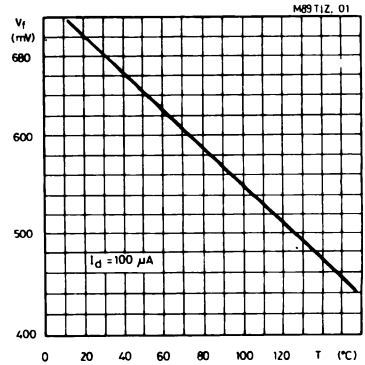
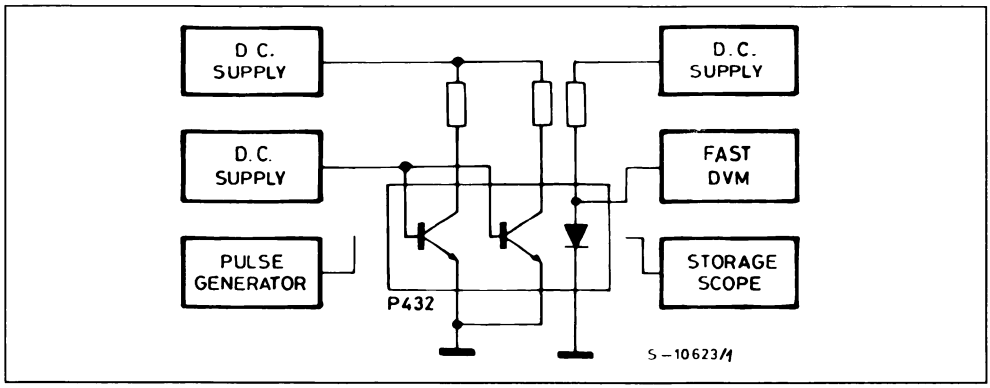


Figure A3 : Measurement Circuits.



APPENDIX B - THERMAL MANAGEMENT IN PULSED CONDITION

THERMAL RESISTANCE AND CAPACITANCE

The electrical equivalent of heat dissipation, for a thermal module formed by the active device with its package and the external heat sink is shown in fig. B1.

To each cell of the thermal chain are associated a value of thermal resistance R_{th} (°C/W) and a value of thermal capacitance C_{th} (J/°C). The former informs about temperature increase due to the element represented by the cell ; as, in the example under consideration, heat transfer is mainly based on conduction for the silicon, the copper integrated heat sink and to metallic body of the external heat sink R_{th} can be calculated from the relationship :

$$R_{th} = \frac{\gamma}{K \times S}$$

where K is the thermal conductivity of the material, the length of the conductive path and S its section.

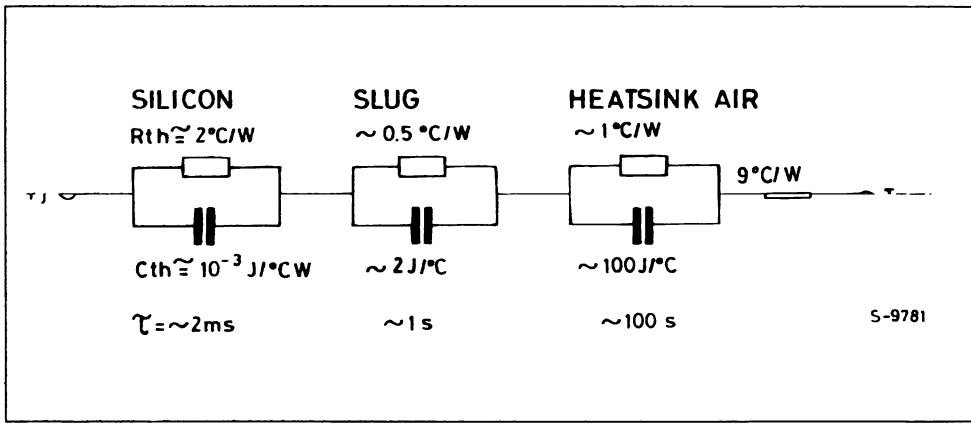
Thermal capacitance C_{th} is the capability of heat accumulation ; it depends on the specific heat of the material and on the volume effectively interested by heat exchange (this means that the parts which are not heated during heat dissipation DO NOT contribute to thermal capacitance). Thermal capacitance is given by :

$$C_{th} = d \times c_t \times V$$

where d is the density of the material, c_t its specific heat and V the volume interested to heat accumulation.

The last element of the network, assumed as purely resistive, is due to convection and radiation from the external heat sink towards the ambient.

Figure B1 : Electrical Equivalent of Multiwatt Package Mounted on the External Heatsink.



Each cell has its own risetime τ , given by the product of the thermal resistance and capacitance :

$$\tau = R_{th} \times C_{th}$$

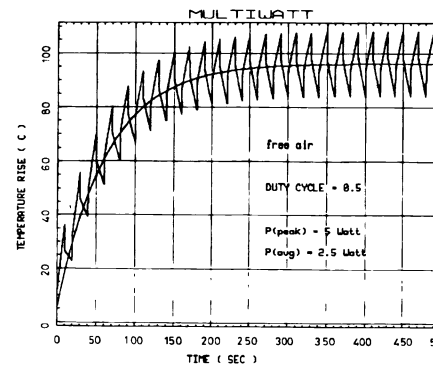
The value of the time constant determines whether a cell approaches equilibrium rapidly of slowly : if R_{th} or C_{th} increases, equilibrium is reached at a slower rate. The following relationship is valid for each cell :

$$\Delta T = R_{th} \times P_d [1 - e^{-t/r}] \quad (1)$$

Typical values of R_{th}, C_{th} and τ for Multiwatt application are shown in fig. B1.

When power is switched on, temperature increase is ruled by subsequent charging of thermal capacitances while the value reached in the steady state depends on thermal resistances only. Qualitative behaviour of the network of fig. B1 is shown in fig. B2.

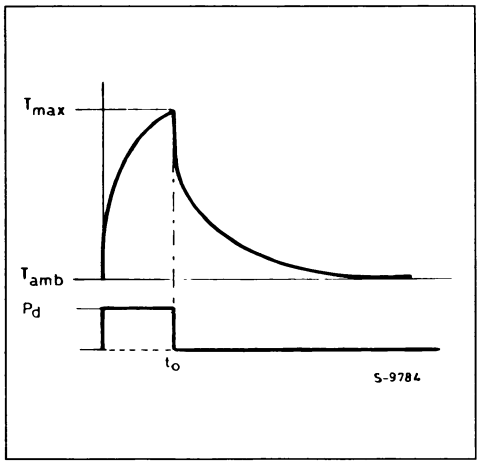
Figure B2 : Qualitative T_j increase (network of fig. B1) for repeated Power Pulse.



SINGLE POWER PULSE

When the pulse length has an assigned value, effective T_j can be significantly lower than the steady state T_j (fig. B3.).

Figure B3 : Effect of a Single Power Pulse.



For any pulse length t_o, a transient thermal resistance R_{th} (t_o) is defined, from the ratio between the junction temperature at the end of the pulse and the dissipated power. Obviously, for shorted pulses, R_{th} (t_o) is lower and a higher power can be dissipated, without exceeding the maximum junction temperature $T_{j\text{-}max}$ allowed to the IC from reliability considerations. Fig. 7 and 9 of this Application Note give experimental values of R_{th} (t_o) for the two cases of the Multiwatt package without and with external heat sink.

REPEATED PULSES

When pulses of the same height P_d are repeated with a defined duty cycle DC and pulse length is short in comparison with the total risetime of the system (many tens of seconds) the train of pulses is seen by the system as a continuous source, at a mean power level of

$$P_{davg} = P_d \times DC$$

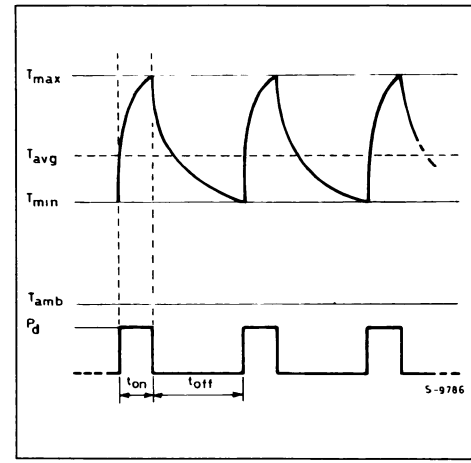
The average temperature increase is :

$$\Delta T_{avg} = R_{th} \times P_{davg} = R_{th} \times P_d \times DC$$

On the other hand, the silicon die (τ_S = 1– 3ms) is able to follow frequencies of some KHz and junction temperature oscillates about the average as qualitatively shown in fig. B4.

The thermal resistance corresponding to the peak of the oscillation at equilibrium (peak thermal resistance $R_{th\,peak}$) is now given by fig. 5, and can be obtained if pulse length and duty cycle are known ; P_{dmax} is derived from the same figure.

Figure B4 : Junction Temperature increase for repeated Pulses.



APPLICATION EXAMPLES

EXAMPLE 1 - MAXIMUM P_d FOR SINGLE PULSE OF ASSIGNED LENGTH

PROBLEM : define the maximum P_d for a single pulse with a length of 20ms in the case of Multiwatt package used without heat sink. Ambient temperature is 50°C ; maximum temperature is 130°C. Die size is 20K mils^2, with dissipating area of 2K mils^2 (as in P432 test pattern).

SOLUTION : allowed temperature increase ΔT is 80°C. Having a $R_{th(j\text{-}a)}$ of 39°C/W, Multiwatt package can dissipate about 2W in steady state. From fig. 7 the transient thermal resistance corresponding to one single pulse of 20ms is R_{th} (20ms)$_{P432}$ = 2.2°C/W. A peak of 80/2.2 = 36.3W can be applied to the circuit.

EXAMPLE 2 - CORRECTION FOR DIE SIZE AND DISSIPATING AREA

PROBLEM : correct the results obtained in example 1, for assigned die size and dissipating area. Practical case : IC having a die size of 35K mils^2 with a dissipating area of 20k mils^2.

SOLUTION : from fig. 5, thermal resistances of P432 and of the IC under consideration are $R_{th\,P432}$ = 2.3°C/W and $R_{th(j\text{-}c)IC}$ = 1.2°C/W.

As the length of the pulse is 10-15 times longer than the rise time of the silicon, the die (first cell of fig. B1) can be assumed to have reached its equilibrium condition.

R_{th} (20ms) found in previous example has to be corrected in order to take into account the new value of $R_{th(j-c)}$:

$$R_{th}\ (20ms)_{IC} = R_{th}\ (20ms)_{P432} - R_{th(j-c)P432} + R_{th(j-c)IC} =$$
$$= 2.2 - 2.3 + 1.2^{\circ}C/W = 1.1^{\circ}C/W$$

A single pulse of 80/1.1 ≅ 72W can be delivered to such device.

When the pulse has the same order of silicon rise time τ P432 is about 1ms) another type of correction is needed. In first approximation, τ increase with dissipating area with the relationship :

$$t_{IC} = \sqrt{20K_{IC}/2K_{P432} \times \tau_{P432}} \equiv 3.1ms$$

Expansion of the exponential term of relationship (1) limited to the first term term, is :

$$R_{th\ IC}\ (t_o) \cong R_{th\ P432}\ (t_o)\ /3.1$$

for t_o = 1ms :

$$R_{th\ IC}\ (1ms) = 1.05/3.1^{\circ}C/W \cong 0.34^{\circ}C/W$$

A single pulse of 80/0.34 ≅ 235W can be delivered to such device.

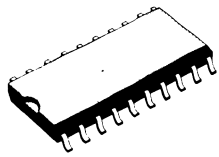
EXAMPLE 3 – R_{th} WITH REPEATED PULSES

PROBLEM : find the peak power which can be dissipated by Multiwatt package without heatsink, when power is continuously switched on 10ms and switched off 90ms. Ambient temperature is 50°C, maximum temperature is allowed to be 125°C.

SOLUTION : a maximum $\Delta T = 75^{\circ}C$ has to be considered. Fig. 5 indicated that for a pulse width of 10ms and a duty cycle of 0.1, $R_{th\ peak}$ is 6.7°C/W. Maximum P_d is 75/6.7 = 11.2W, with an average temperature increase ΔT_{peak} of 39 x 0.1 x 11.2 ≅ 43°C.

PACKAGES

SO-20L



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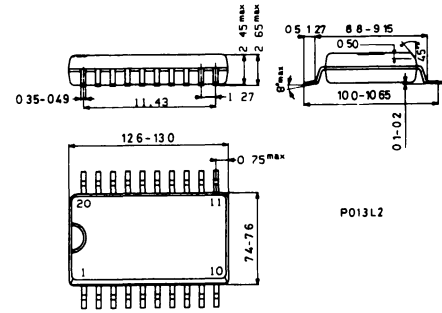
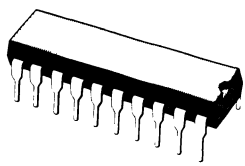


POWERDIP (16 + 2 + 2)



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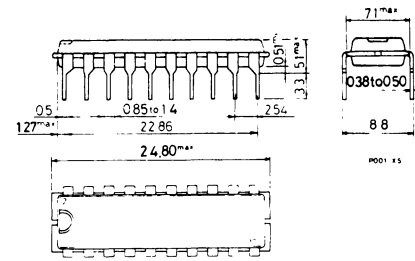
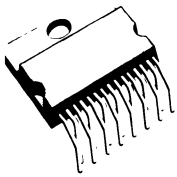


MULTIWATT 15 (Horizontal)



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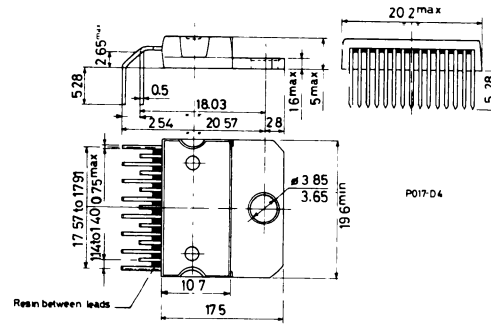
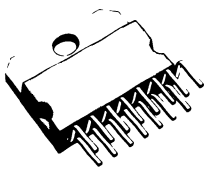


MULTIWATT 15 (Vertical)



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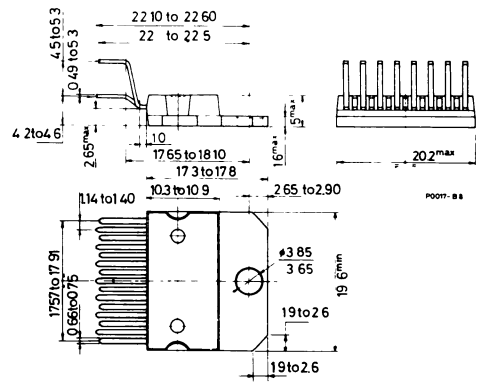

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