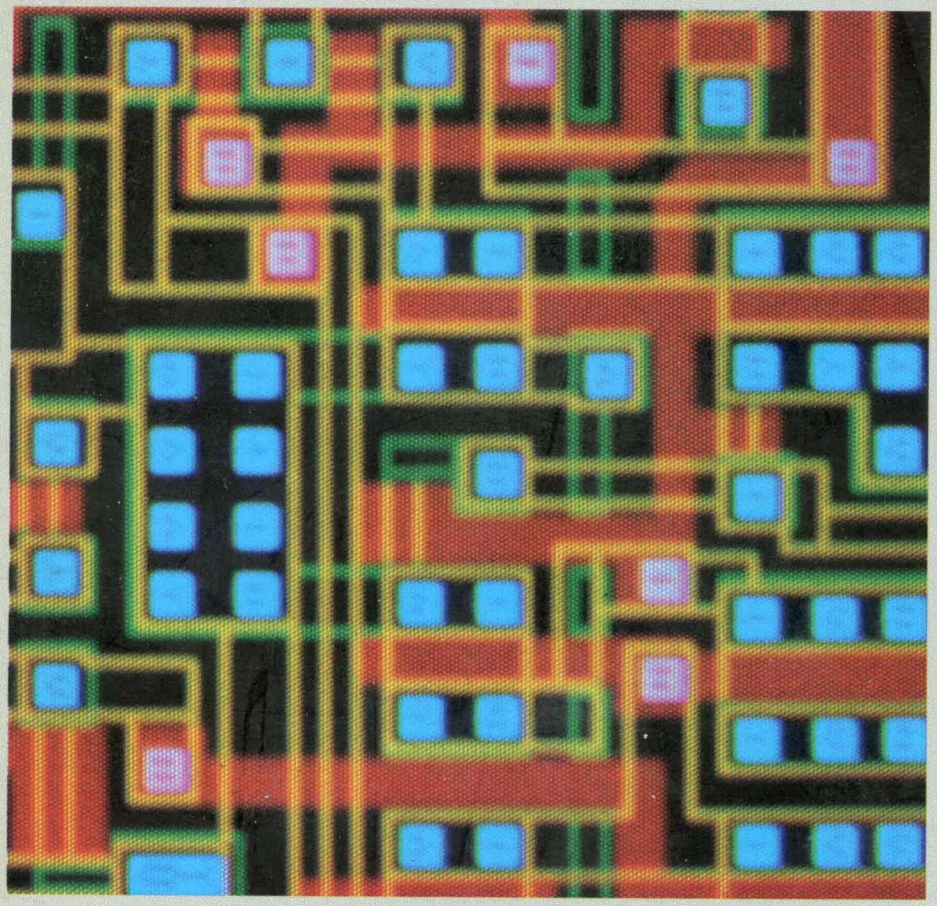
SIEMENS

Industrial IC Data Book 1985



Microprocessors ■ Microcontrollers ■ Peripherals ■ Support
Memory ■ Telecom ■ Data Converters ■ SMPS Controllers

SIEMENS Industrial IC Data Book ■ 1985 Microprocessors ■ Microcontrollers ■ Peripherals ■ Support Memory ■ Telecom ■ Data Converters ■ SMPS Controllers

SIEMENS

Industrial IC Data Book 1985

Table of Contents

Table of Contents

4. Peripheral and Support Components

5. Memory Components

6. Telecom Components

Table of Contents

*See Consumer Data Book or contact your local Siemens Representative.

Table of Contents

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Table of Contents

*See Consumer Data Book or contact your local Siemens Representative.

General Information

1.1 Type Designation Code For ICs

The IC type designations are based on the European code system of Pro Electron.* The code system is explained in the Pro Electron brochure D 15, 1982 edition, which can be obtained from:

Pro Electron
Boulevard de Waterloo 103
1000 Brussels, Belgium

*Some exceptions exist.

1.2 Mounting Instructions

Plastic Package With 8, 14, 16, 18, 20, 22, 24, 28, or 40 Pins

The pins are bent downwards in a 90° angle and fit into holes with a diameter of between 0.7 and 0.9 mm spaced 2.54 mm apart. The dimension x(see figure below) is given in the mechanical dimension drawings for the various packages.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package (see figure below).

After the package is inserted into the PC board, it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. Plastic packages are soldered on that side of the PCB facing away from the package.

The maximum permissable soldering temperature is 265°C (max. 10 s) for manual soldering and 240°C (max 4 s) for dip soldering.

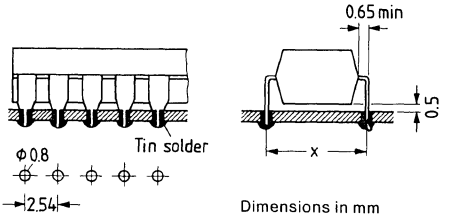


Figure 1

Power Package With 9 Pins

Power packages generally have wider pins than standard plastic packages; meaning the hole diameter on the PCB must be between 1.1 and 1.8 mm. If the pins are bent, there should be no stress between the pins and the package. The minimum distance between the package and the bending point is 2 mm.

The soldering temperatures for power packages are the same as for plastic packages.

Micropack Packages

Mounting instructions for components available in a micropack are found within the Data Sheet.

Precautions

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.

When they are being prepared and inserted in a PCB, integrated circuits should be protected against static charging. Under no circumstances may the components be removed or inserted while the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductive loads.

1.3 Processing Guidelines For ICs

Integrated circuits (ICs) are electrostatic-sensitive (ESS) devices. The requirement for greater packing density has led to increasingly small structures on semiconductor chips, with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is hardly possible any more for them to be destroyed by purely static electricity. On the other hand, there is acute danger from electrostatic discharges (ESD).

Of the multitude of possible sources of discharge, charged devices should be mentioned in addition to charged persons. With low-resistance discharges, it is possible for peak power amounting to kilowatts to be produced.

For the protection of devices, the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible. Means which are effective here are an increase in relative humidty to $\geq$ 60% and the replacement of highly charging plastics by antistatic materials.

b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally R = 10^6 to 10^8 ohms).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences, can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer.

Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, as well as equipment and soldered circuit boards that contain such components.

Handling of Devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to 10^9 ohms to ground.
3. With humidity of > 50% pure cotton clothing is sufficient. In the case of chargeable synthetic fibers, the clothing should be worn close-fitting. A wrist strap grounded across a resistor of 5 x 10^4 to 10^5 ohms must be worn snugly on the skin.
4. If conductive floors, R = 5 x 10^4 to 10^7 ohms are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole (R = 10^5 to 10^7 ohms).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be accross a resistor of 10^6 to 10^8 ohms.
6. When loading machines and production devices, it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

   Example 1) conductive (black) tubes.
   The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person. Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounded).

   Example 2) anti-static (transparent) tubes.
   The devices cannot be destroyed by charged persons in the tube (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be endangered as in 1) when the tube is emptied if the tube, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

   In both cases, damage can be avoided by discharging the devices across a grounded adapter of high-resistance material (= 10^6 to 10^8 ohms) between the tube and the machine.

   The use of metal tubes — especially of anodized aluminum — is not advisable because of the danger of low-resistance device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage, the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 60°C.

Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of high-charging plastic or very low-resistance materials are in like manner unsuitable.

Transfer cars and their rollers should exhibit adequate electrical resistance ($R < 10^6$ ohms). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming Inspection

At incoming inspection, the above guidelines should be observed. Otherwise any right to refund or replacement if devices fail inspection may be lost.

Material and Mounting

1. The drive belts of machines used for the processing of the devices (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontaktchemie).
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control should not be used. Siemens EMI-suppression capacitors of the type B 81711-B31...-B36 are recommended to protect against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered electrostatically sensitive.

Electrical Tests

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.
2. Test receptacles must not have voltage applied when individual devices or assembled circuit boards are inserted or withdrawn, unless specifications state otherwise. Ensure that the testers do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. Signal voltages may only be applied to the inputs of ICs when or after the supply voltage is turned on. They must be disconnected before or when the supply voltage is turned off.
4. Observe any notes and instructions in the respective data books.

Packing Of Assembled PC Boards or Flatpack Units

The packing material should exhibit low volume conductivity: 10^5 ohm-cm $< \rho < 10^{10}$ ohm-cm.

In most cases — especially with humidity of > 40% — this requirement is fulfilled by simple corrugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, CA).

One should always ensure that boards cannot touch.

In special cases, it may be necessary to provide protection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose, a sheath of aluminum foil is recommended, although direct contact between the foil and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping Siemens devices, are available from Laber of Munich.

Ultrasonic Cleaning Of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic), separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	$f > 40$ KHz
exposure	$t < 2$ min.
alternating sound pressure	$p < 0.29$ bar
sound power	$N <$ W/cm²/liter

1.4 Electrical And Environmental Ratings

Maximum Ratings

The maximum ratings are absolute limits. The IC may be destroyed if only a single one of these values is exceeded.

Electrical Characteristics

The electrical characteristics include the guaranteed tolerances of the values maintained by an IC for the specified operating range.

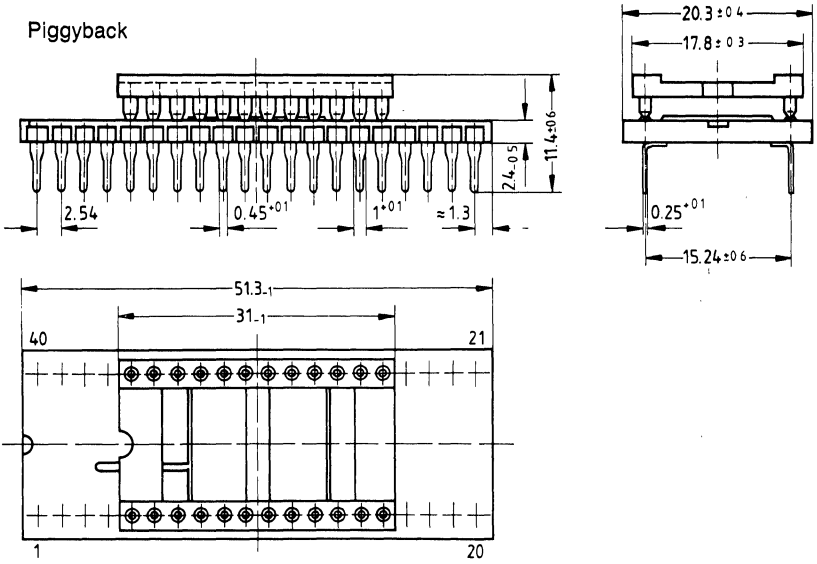
The typical characteristics are mean values that can be expected on the basis of the production. Unless otherwise specified, the typical characteristics apply to $T_{amb} = 25°C$ and the given supply voltage.

Operating Data

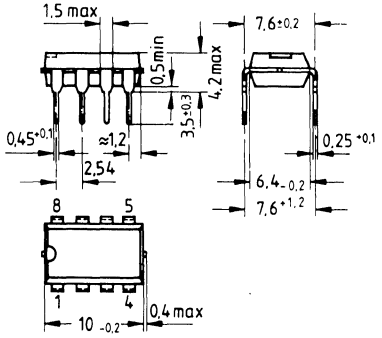
The functions stated in the circuit description are fulfilled within the range of the operating data.

1.5 Mechanical Dimensions
Package Dimensions

Piggyback

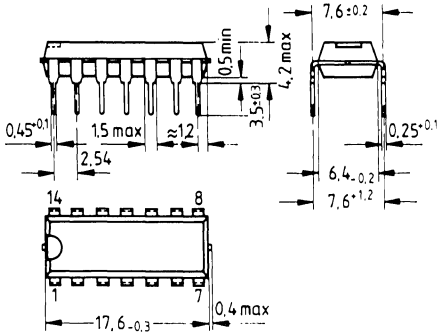


Plastic plug-in package 20 A 8 DIN 41866
8 pins, DIP



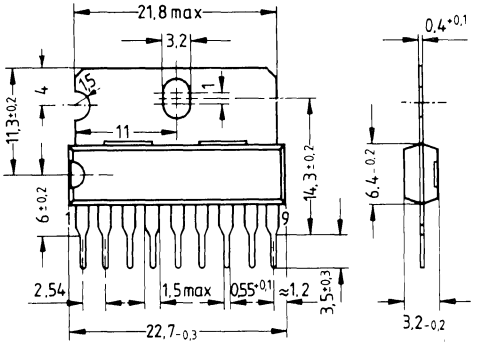
Approx. weight 0.7 g

Plastic plug-in package 20 A 14 DIN 41866
14 pins, DIP



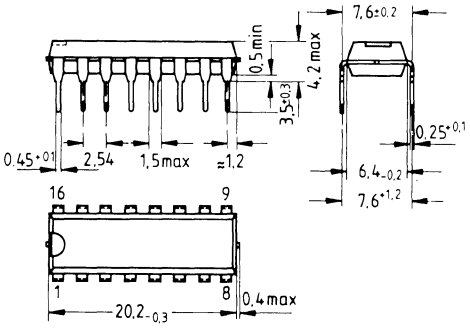
Approx. weight 1.1 g

Plastic power package,
with cooling fin and 9 pins, SIP (TDA 4601)



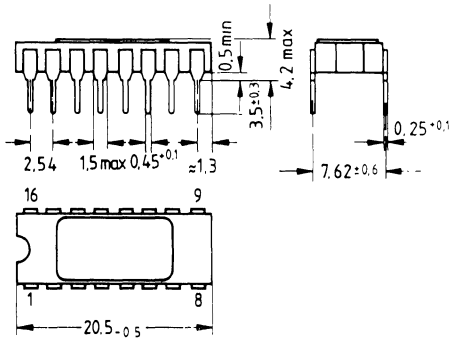
Approx. weight 1.9 g

Plastic plug-in package 20 A 16 DIN 41866,
16 pins, DIP



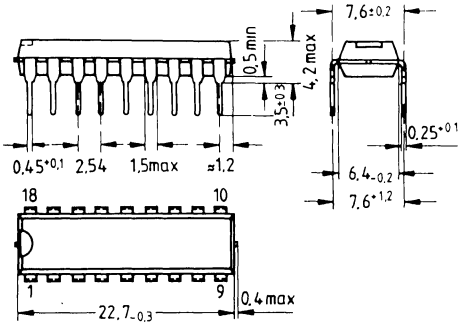
Approx. weight 1.2 g

Ceramic package, 16 pins, DIC



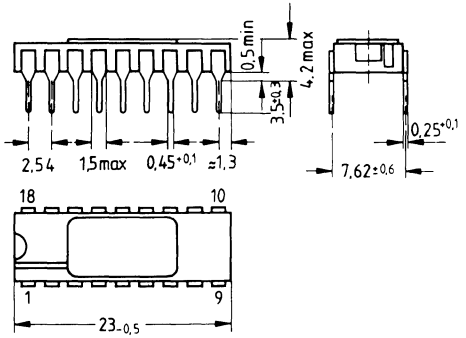
Approx. weight 1.4 g

Plastic plug-in package 20 A 18 DIN 41866,
18 pins, DIP



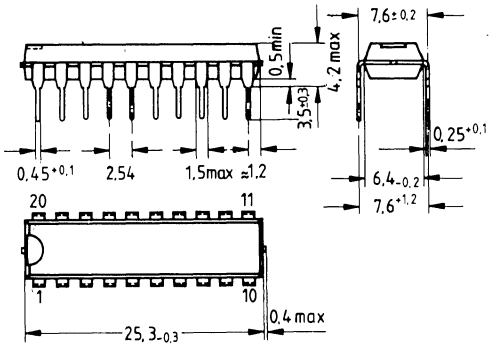
Approx. weight 1.3 g

Ceramic package, 18 pins, DIC



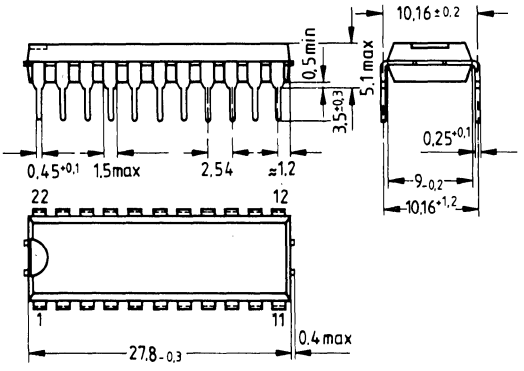
Approx. weight 2.7 g

Plastic plug-in package 20 A 20 DIN 41866,
20 pins, DIP



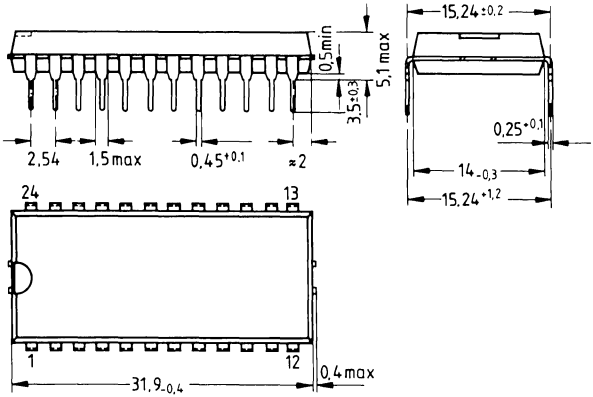
Approx. weight 1.5 g

Plastic plug-in package 20 D 22 DIN 41866,
22 pins, DIP



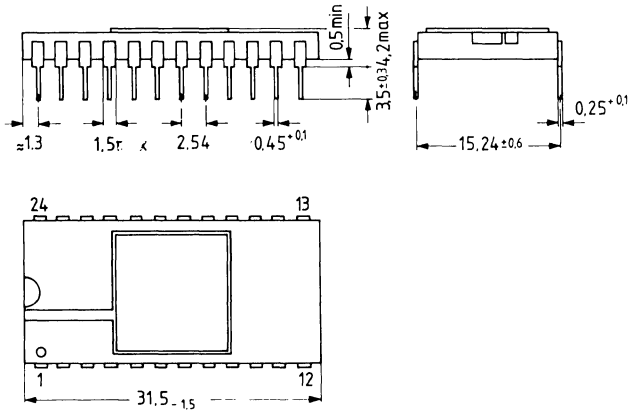
Approx. weight 2.1 g

Plastic plug-in package 20 B 24 DIN 41866,
24 pins, DIP



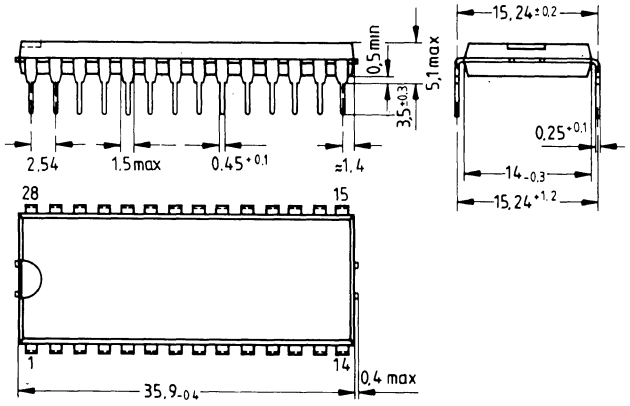
Approx. weight 2.5 g

Ceramic package, 24 pins, DIC



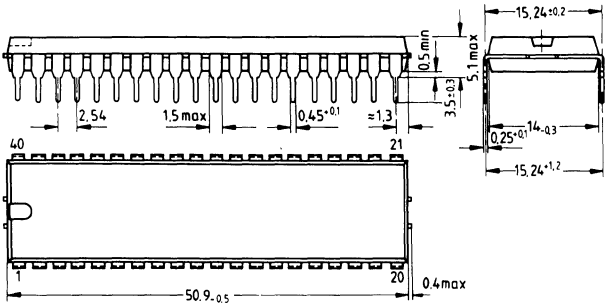
Approx. weight 3 g

Plastic plug-in package 20 B 28 DIN 41866,
28 pins, DIP



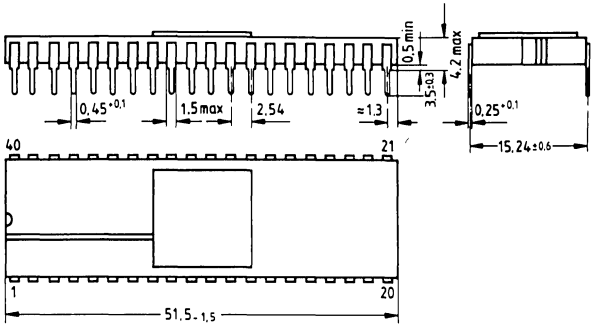
Approx. weight 3 g

Plastic plug-in package 20B 40 DIN 41866,
40 pins, DIP



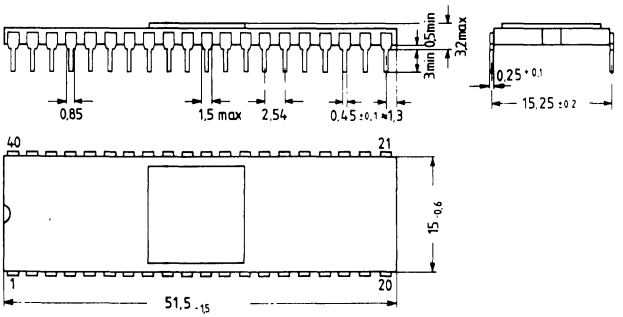
Approx. weight 5.9 g

Ceramic package, 40 pins, DIC (SAB 8086)



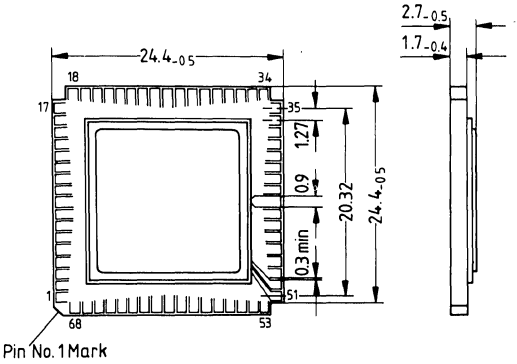
Approx. weight 6.8 g

Ceramic package, 40 pins, DIC

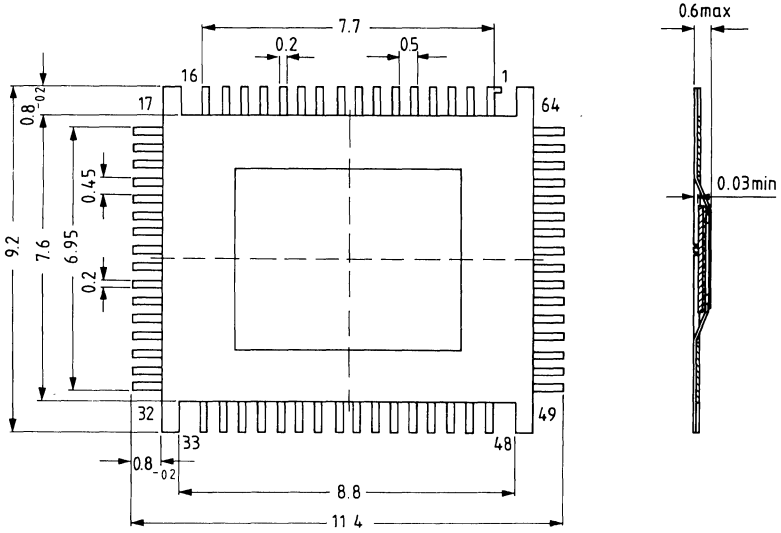


Approx. weight 5.9 g

Ceramic package, 68 pins, LCC

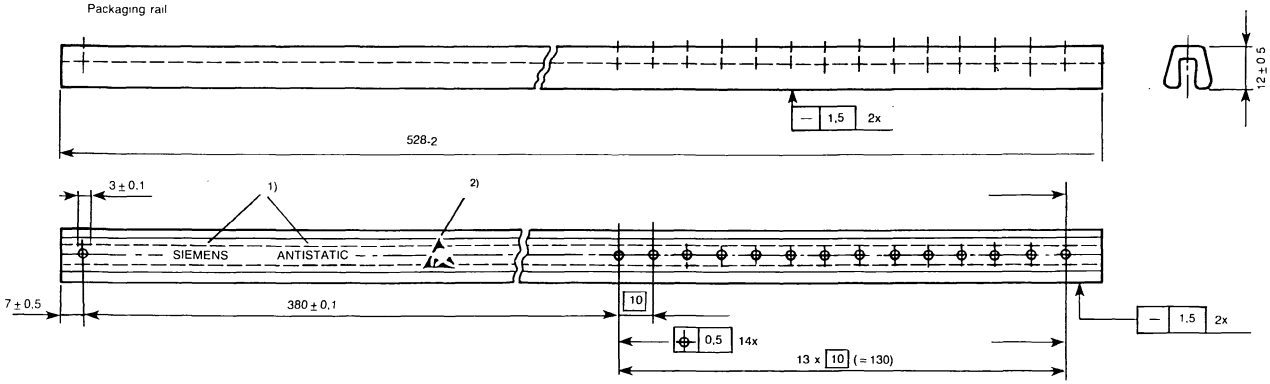


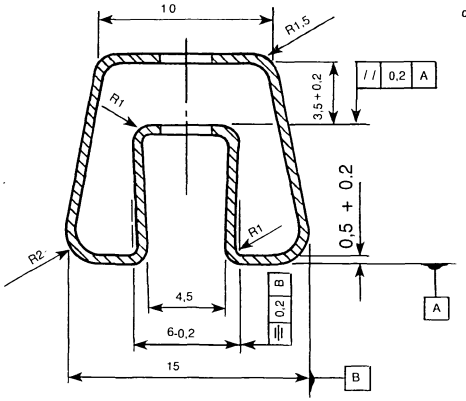
MICROPACK, 64 connections



Shipping Tube Dimensions — MIL 300 (DIC 14; 16; 18)

Packaging rail





cross-section, rotated by 90°

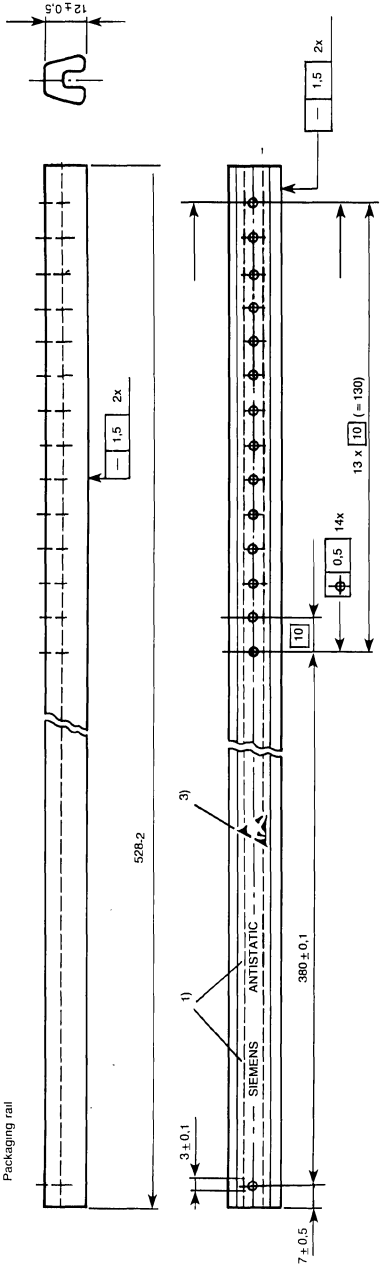
1) Labeling: Height: 4mm, color: blue

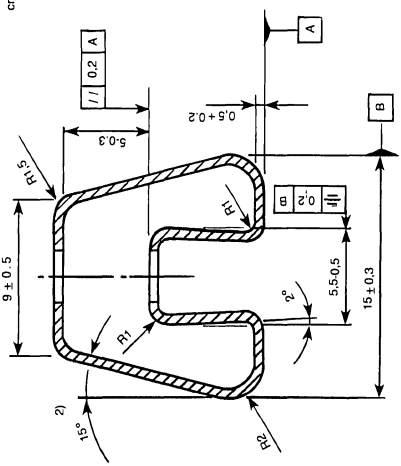
2) ESD — symbol according to SN68410

seam 0,03 max.

Hard PVC, transparent,
impact resistant

Shipping Tube Dimensions — MIL 300 (DIP 4, 6, 8, 14, 16, 19, 20)





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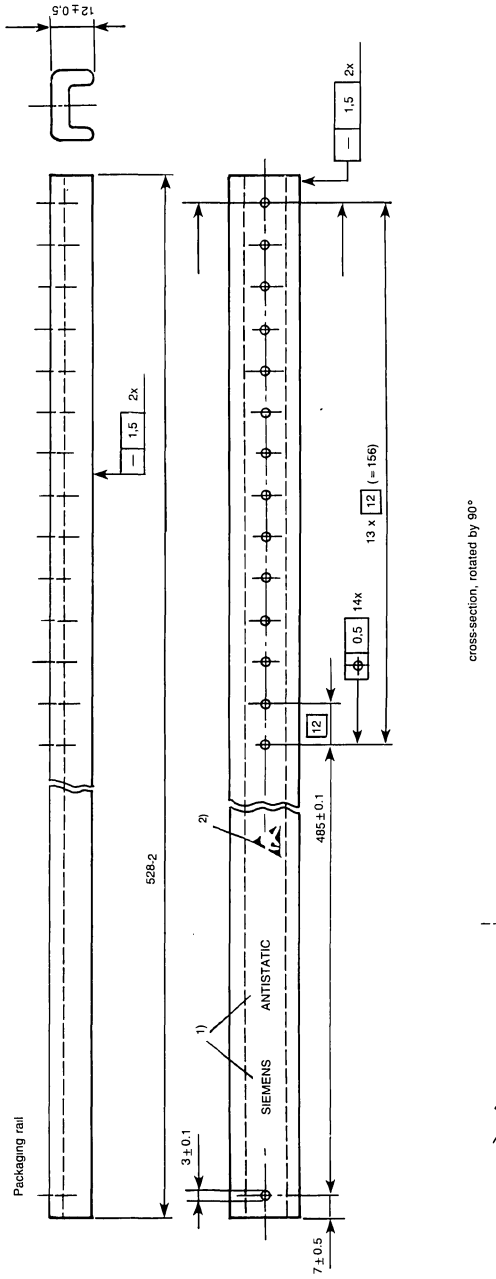
2) measurement

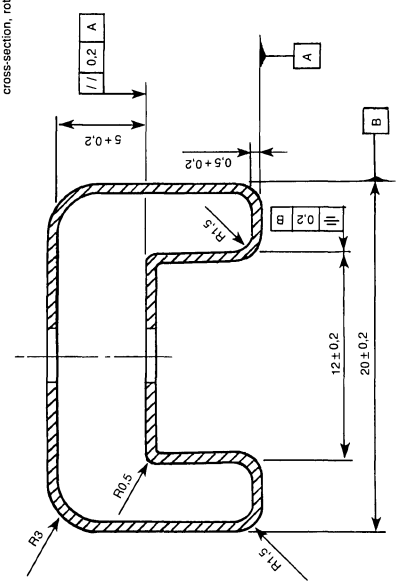
3) ESD — symbol according to SN68410

seam 0,03 max.

Hard PVC, transparent, impact resistant

Shipping Tube Dimensions — MIL 600 (DIC 24; 28; 40)





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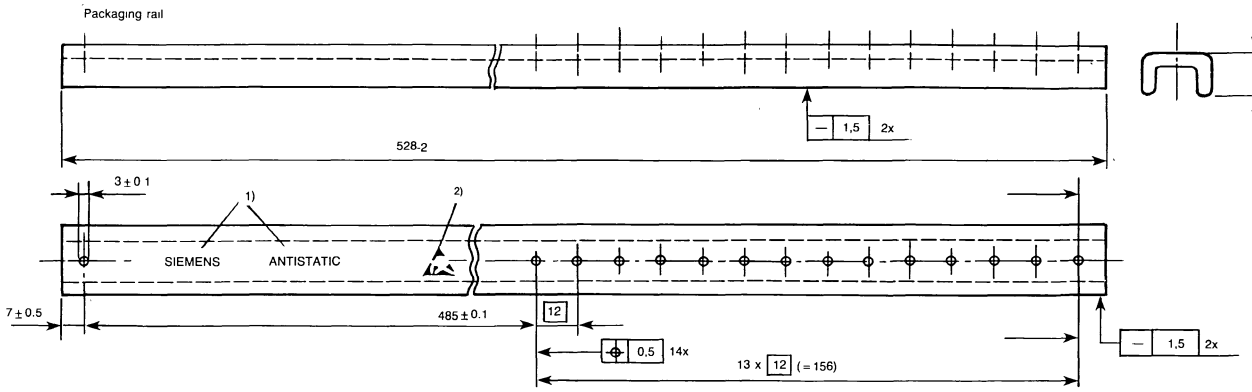
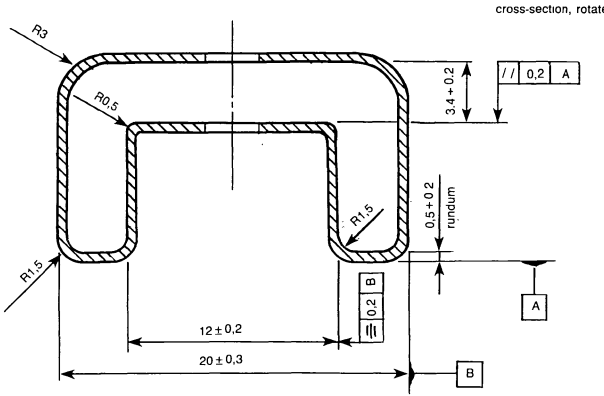
2) ESD — symbol according to SN68410

seam 0,03 max.

Hard PVC, transparent, impact resistant





1) Labeling: Height: 4mm, color: red

2) ESD — symbol according to SN68410

seam 0,03 max.

Hard PVC, transparent,
impact resistant

1.6 Quality And Reliability

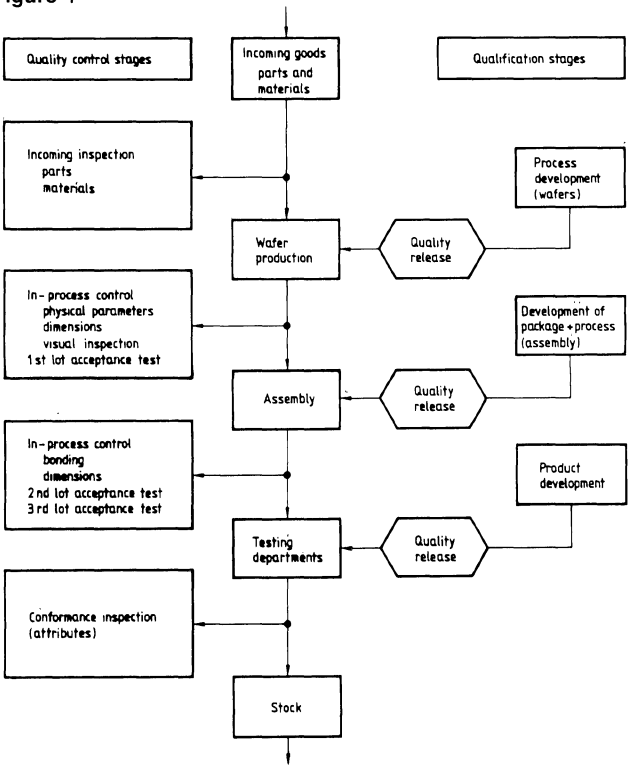
Quality Assurance System

The high quality and reliability of integrated circuits from Siemens is the result of a carefully arranged production which is systematically checked and controlled at each production stage.

The procedures are subject to a quality assurance system; full details are given in the brochure "Siemens Quality Assurance System-Integrated Circuits" (SQS-IC).

Figure 1 shows the most important stages of the "SQS-IC". A quality assurance (QA) department which is independent of production and development, is responsible for the selected control measures, acceptance procedures, and information feedback loops. This department has state-of-the-art test and measuring equipment at its disposal, works according to approved methods of statistical quality control, and is provided with facilities for accelerated life and environmental tests used for both qualification and routine monitoring tests.

Figure 1



The latest methods and equipment for preparation and analysis are employed to achieve a continuous development of quality and reliability.

Quality Specifications

The delivery quality of integrated circuits is specified as follows:

1. **Maximum ratings and tolerance limits of the characteristics.**
2. **Sampling inspection, AQL values (acceptable quality level)**
   Inspection by attributes[1] is based on the identical sampling inspection plans DIN 40080, (or) MIL-STD-105, inspection level II, normal inspection, or IEC 410.

   A delivery lot for which the defect percentage for a certain characteristic is equal or less than the specified AQL value, will most probably (more than 95%) be accepted in the appropriate sampling inspection.

   The average defect percentage of delivered products lies, in general, clearly below the AQL value and is known as the average outgoing quality (AOQ). Only the number of defective units is evaluated in the sampling inspection.

3. **Defects**

   A defect exists if a component characteristic does not correspond to the specifications in the data sheet.

   The defects are classified as total defects, defects in the electrical features, and defects in the mechanical features. Unless otherwise agreed upon, the AQL values in section 5 apply to the various defect types.

4. **Classification of defects**

Total defect:	- open contact or short circuit within a specified temperature range - no marking, or wrong type and/or direction of marking - wrong marking of pin 1 - mixed with wrong versions/types - components not aligned within one rail/tube - broken package and/or pins
Defects in the electrical features:	- exceeding electrical specification limits
Defects in the mechanical features:	- defects on the package surface - type marking hard to identify - bent pins - wrong dimensions

1) Inspection for a characteristic for which only two mutually exclusive properties are specified (good/bad).

5. AQL table

Defect type	AQL values Bipolar IC	MOS IC
Total defect (mechanical and electrical)	0.1	0.25
Defect in the electrical features	0.4	0.4
Defect in the mechanical features	0.4	0.4

AQL value 1.5 applies to switching times

6. Incoming inspection

The tests carries out by the manufacturer are intended to render expensive incoming inspection by the user unnecessary. If the user, however, wants to carry out such inspections, we recommend the use of a sampling inspection plan as described in section 7. The test method used must be agreed upon between customer and supplier.

The following information is required to adjust a possible claim:
test circuit, sample size, number of defective items found, sample of evidence, packing list.

7. Sampling inspection plan for normal inspection

in accordance with DIN 40080 or MIL-Std-105 D, inspection level II, or IEC410

Lot size	Sample size	AQL value										
		0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5
		A R	A R	A R	A R	A R	A R	A R	A R	A R	A R	A R
2 to 8	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1 ↕
9 to 15	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1 ↕	↕
16 to 25	5	↓	↓	↓	↓	↓	↓	↓	↓	0 1 ↕	↕	↕
26 to 50	8	↓	↓	↓	↓	↓	↓	↓	0 1 ↕	↕	↓	1 2
51 to 90	13	↓	↓	↓	↓	↓	↓	0 1 ↕	↕	↕	1 2 ↕	2 3
91 to 150	20	↓	↓	↓	↓	↓	0 1 ↕	↕	↕	1 2 ↕	2 3	3 4
151 to 280	32	↓	↓	↓	↓	0 1 ↕	↕	↓	1 2	2 3	3 4	5 6
281 to 500	50	↓	↓	↓	0 1 ↕	↕	↕	1 2 ↕	2 3	3 4	5 6	7 8
501 to 1200	80	↓	↓	0 1 ↕	↕	↕	1 2 ↕	2 3	3 4	5 6	7 8	10 11
1201 to 3200	125	↓	0 1 ↕	↕	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15
3201 to 10000	200	0 1 ↕	↕	↕	1 2 ↕	2 3	3 4	5 6	7 8	10 11	14 15	21 22
10001 to 35000	315	↕	↕	1 2 ↕	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↕
35001–150000	500	↓	1 2 ↕	2 3	3 4	5 6	7 8	10 11	14 15	21 22 ↕	↕	↕
150001–500000	800	1 2 ↕	2 3	3 4	5 6	7 8	10 11	14 15	21 22 ↕	↕	↕	↕
500001 and more	1250	2 3 ↕	3 4 ↕	5 6 ↕	7 8 ↕	10 11 ↕	14 15 ↕	21 22 ↕	↕	↕	↕	↕

A = Acceptance number, i.e. the maximum number of defective sample units up to which the lot is accepted.

B = Rejection number, i.e. the number of defective sample units which must at least be found for the lot to be rejected.

Additional requirement

As the combination Acceptance 0 and Rejection 1 has a low degree of significance, the next larger size should be sampled.

Quality Conformance

Each integrated circuit is subject to a final test at the end of the production process. Those tests are carried out by computer-controlled, automatic test systems because hundred of thousands of operating conditions as well as many static and dynamic parameters are to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum failure rate as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

The table below shows the results of such sampling inspections performed with hundred of thousands of ICs in 1984. Those results correspond to the average outgoing quality (AOQ), and are specified as defectives per million.

	Total defects AOQ (dpm)	Sum of electrical defects AOQ (dpm)	Sum of mechanical defects AOQ (dpm)
SSI/MSI $\leq$ 1000 gate functions	60	300	500
LSI/VLSI $\geq$ 1000 gate functions	400	800	600

Due to the low failure rate, the user generally need not perform an incoming inspection.

Reliability

Measures taken during development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, specifying e.g. minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional offenses against those design standards.

In-process control during production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

The decreasing failure rates reflect the never ending effort in this direction; in the course of years they have been reduced considerably despite an immense rise in the IC's complexity.

Figure 2

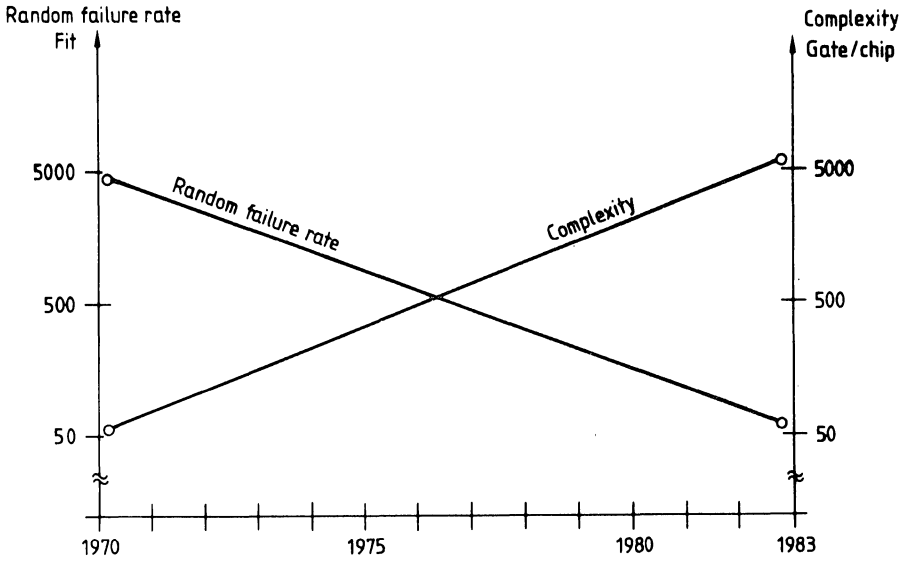
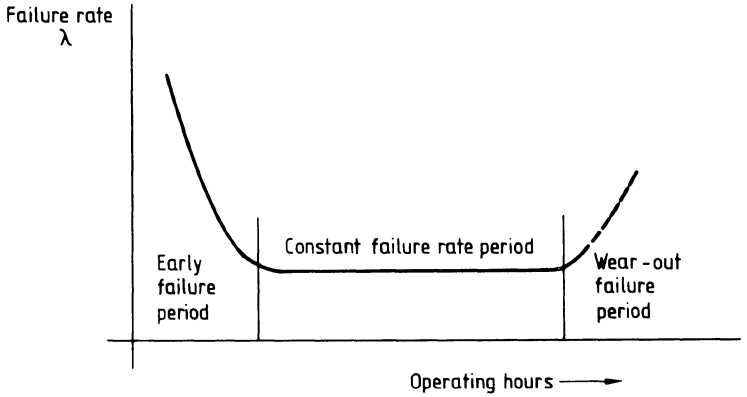


Figure 2 shows the general course of the failure rate for digital MOS ICs in fit for the years 1970 to 1983. The increasing complexity as regards gate functions/chip is also specified.

Reliability monitoring

The general course of the IC's failure rate versus time is shown by a so-called "bathtub" curve (figure 3). The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For IC's, however, the latter period lies usually far beyond the service life specified for the individual equipment.

Figure 3



Reliability tests for ICs are usually destructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simulate a future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius Equation

$$B = \exp\left[\left(\frac{EA}{k}\right)\left(\frac{T_2-T_1}{T_1 T_2}\right)\right]$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of T_{amb} = 40°C, assuming an average activation energy of 0.4 eV. The acceleration factor for life tests is thus 24, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line-this is described in the brochure "SQS-IC". Such tests are e.g. humidity test at 85°C and 85% relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

1.7 Thermal Coefficients

Plastic Packages

Type/ Pins	Mounting Area mm x mm	Chip Size mm²	R_{thSA} °K/W
DIL 8	2.0 x 3.0	4	108
14	2.0 x 3.6 N	4/5	79/77
	3.5 x 4.2 N	4/7/12	72/67/62
16	2.0 x 3.6	4/5	77/75
	3.5 x 5.0	4/7/15	71/65/59
	3.5 x 6.5	8	63
	3.7 x 10.2	25	60
18	2.8 x 3.6	4/7	70/65
	3.5 x 5.5	4/7/15	66/60/55
20	3.8 x 5.5 N	7/17	65/60
	4.0 x 7.8	18	56
22	4.5 x 5.5	7/21	56/47
24	4.2 x 5.2	7/18	55/52
	6.2 x 7.2	7/30/40	49/45/44
28	4.2 x 5.2	7/18	51/48
	6.0 x 7.5	7/30/40	45/41/40
40	6.0 x 7.5	7/30/40	43/39/38

N = new package, S = special package according to package catalogue

Ceramic multi-layer packages

Type/ Pins	Mounting Area mm x mm	Chip Size mm²	R_{thSA} °K/W
DIC 16	3.9 x 6.1 S	4/7/15	78/71/65
	5.6 x 10 N	30	55
18	3.9 x 5.6 S	4/7/13	75/68/63
24	6.5 x 6.5 S	7/30	54/46
40	7.8 x 7.8 S	7/30/46	49/42/37
	9.0 x 9.0 N	7/30/46	45/38/36

N = new package, S = special package according to package catalogue.

Plastic power package

Type/ Pins	Mounting Area mm x mm	Chip Size mm²	R_{thSA} °K/W	R_{thSC} °K/W
SIL 9	2.5 x 3.4	4.7	60	2.2
	3.4 x 4.3	7	60	2.2

N = new package, S = special package according to package catalogue.

Summary of Types

2.1 Component Selection Guide

Microcontroller and Microprocessor Components

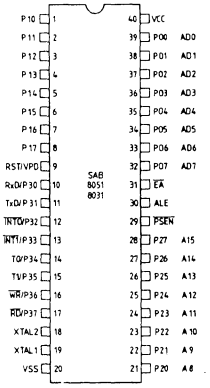
Microcontroller and Microprocessor Components

SAB 8031/8051
8-Bit Single Chip Microcomputer

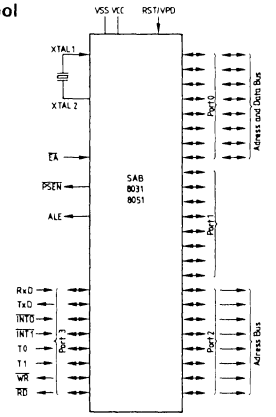
SAB 8031/8031-10 Control Oriented CPU With RAM and I/O
SAB 8051/8051-10 An SAB 8031 With Factory Mask-Programmable ROM

- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-Bit Ports, 32 I/O Lines
- Two 16-Bit Timer/Event Counters
- High-Performance Full-Duplex Serial Channel
- External Memory Expandable to 128K
- Compatible with SAB 8080/8085 Peripherals
- SAB 8031/8051 12 MHz Operation
- SAB 8031-10/8051-10 10 MHz Operation
- Boolean Processor
- SAB 8048 Architecture Enhanced with:
  Non-Paged Jumps
  Direct Addressing
  Four 8-Register Banks
  Stack Depth Up to 128-Bytes
  Multiply, Divide, Subtract, Compare
- Most Instructions Execute in 1 µs
- 4 µs Multiply and Divide

Pin Configuration



Logic Symbol



The SAB 8031/8051 is a stand-alone, high-performance single-chip computer fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 40-pin DIP. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64K bytes of program memory and/or up to 64K bytes of data storage.

The SAB 8051 contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The SAB 8031 is identical, except that it lacks the program memory. For systems that require extra capability, the SAB 8051 can be expanded using standard TTL compatible memories and the byte oriented SAB 8080 and SAB 8085 peripherals.

The SAB 8051 microcomputer, like the SAB 8048, is efficient both as a controller and as an arithmetic processor. The SAB 8051 has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte. 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1.0 µs, 40% in 2.0 µs and multiply and divide require only 4.0 µs. Among the many instructions added to the standard SAB 8048 instruction set are multiply, divide, subtract and compare.

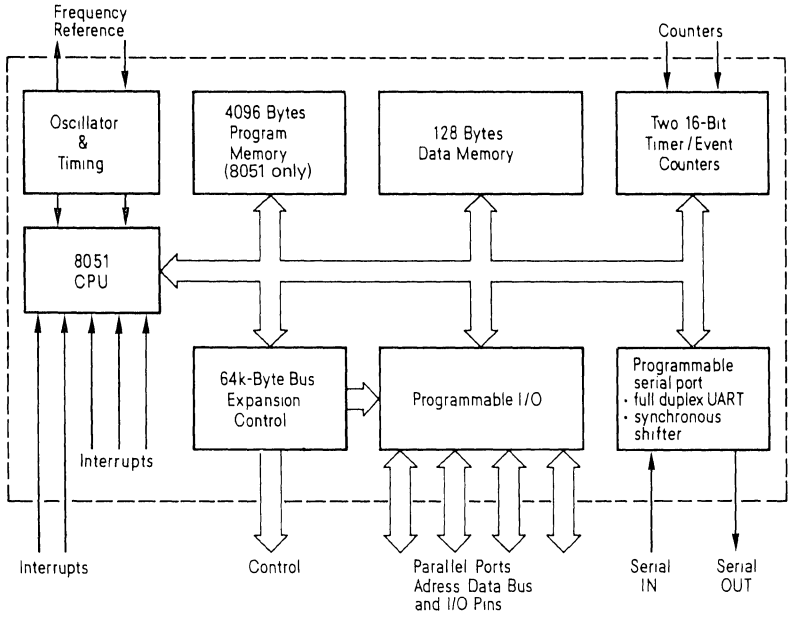
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Functions
P1.Ø–P1.7	1–8	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source three LS TTL loads.
RST/VPD	9	I	A high level on this pin resets the SAB 8051. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.Ø–P3.7	10–17	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source three LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: – RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INTO}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory. – $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.
XTAL1 XTAL2	19 18	I	XTAL 1 Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL2. XTAL2 Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.Ø–P2.7	21–28	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source three LS TTL loads.
$\overline{PSEN}$	29	O	The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	O	Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Functions
$\overline{EA}$	31	I	When held at a TTL high level, the SAB 8051 executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 8051 fetches all instructions from external Program Memory.
P0.0–P0.7	39–32	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
VCC	40		+5V power supply during operation and program verification.
VSS	20		Circuit ground potential.

Block Diagram



Instruction Set Description

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to Accumulator	1	1
ADD	A, direct	Add direct byte to Accumulator	2	1
ADD	A, @Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry flag	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A w/Borrow	1	1
SUBB	A,#data	Subtract immediate data from A w/Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A & B	1	4
DA	A	Decimal Adjust Accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load Data Pointer with a 16-bit constant	3	2
Data transfer (cont.)				
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order Digit ind. RAM w/A	1	1
Boolean variable manipulation				
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute Subroutine Call	2	2
LCALL	addr 16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute Jump	2	2
LJMP	addr 16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if Carry flag is not set	2	2
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit Not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp. immed. to A & Jump if Not Equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. & Jump if Not Equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. & Jump if Not Equal	3	2
DJNZ	Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ	direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7

direct – 128 internal RAM locations, any I/O port, control or status register

@Ri – Indirect internal RAM location addressed by register R0 or R1

#data – 8-bit constant included in instruction

#data 16 – 16-bit constant included as bytes 2 & 3 of instruction

bit – 128 software flags, any I/O pin, control or status bit

Notes on program addressing modes:

addr 16 – Destination address for LCALL & LJMP may be anywhere within the 64-Kilobyte program memory address space.

addr 11 – Destination address for ACALL & AJMP will be within the same 2-Kilobyte page of program memory as the first byte of the following instruction.

rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Opcodes in Hexadecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A

Hex Code	Number of Bytes	Mnemonic	Operands
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr*
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

Absolute Maximum Ratings[1)]

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground (VSS)	−0.5 to + 7 V
Power Dissipation	2 W

D.C. Characteristics

TA = 0 to 70°C; VCC = 5 V ± 5%; VSS = 0 V

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
VIL	Input Low Voltage	−0.5		0.8	V	–
VIH	Input High Voltage (Except RST/VPD and XTAL2)	2.0		VCC+0.5		
VIH1	Input High Voltage to RST/VPD for Reset, XTAL2	2.5		–		XTAL1 to VSS
VPD	Power Down Voltage To RST/VPD	4.5		5.5		VCC = 0V
VOL	Output Low Voltage Ports 1, 2, 3	–		0.45		IOL = 1.6 mA
VOL1	Output Low Voltage Port 0, ALE, /PSEN		–			IOL = 3.2 mA
VOH	Output High Voltage Ports 1, 2, 3	2.4		–		IOH = −60 µA
VOH1	Output High Voltage Port 0, ALE, /PSEN					IOH = −400 µA
IIL	Logical 0 Input Current Ports 1, 2, 3	–		−800	µA	VIL = 0.45 V
IIL2	Logical 0 Input Current XTAL 2			−2.0	mA	XTAL1 = VSS VIL = 0.45 V
IIH1	Input High Current to RST/VPD for Reset			500	µA	VIN = VCC−1.5 V
ILI	Input Leakage Current To Port 0,/EA			±10		0 < VIN < VCC
ICC	Power Supply Current		125	160	mA	–
IPD	Power Down Current		10	20		
CIO	Capacitance of I/O Buffer		–	10	pF	f_c = 1 MHz

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics for SAB 8031/8051

TA 0°C to 70°C; VCC = 5V ±5%; VSS = 0V
(CL for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	127		2TCLCL-40		
TAVLL	Address Setup to ALE	53	–	TCLCL-30	–	
TLLAX1	Address Hold After ALE	48		TCLCL-35		
TLLIV	ALE to Valid Instr In	–	233	–	4TCLCL-100	
TLLPL	ALE to $\overline{PSEN}$	58	–	TCLCL-25	–	ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		3TCLCL-35		
TPLIV	$\overline{PSEN}$ to Valid Instr In	–	150	–	3TCLCL-100	
TPXIX	Input Instr Hold After $\overline{PSEN}$	0	–	0	–	
TPXIZ*)	Input Instr Float After $\overline{PSEN}$	–	63	–	TCLCL-20	
TPXAV*)	Address Valid After $\overline{PSEN}$	75	–	TCLCL-8	–	
TAVIV	Address to Valid Instr In	–	302	–	5TCLCL-115	
TAZPL	Address Float to $\overline{PSEN}$	0	–	0	–	

External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL-100		
TWLWH	$\overline{WR}$ Pulse Width		–	6TCLCL-100	–	
TLLAX2	Address Hold After ALE	132		2TCLCL-35		
TRLDV	$\overline{RD}$ to Valid Data In	–	250	–	5TCLCL-165	
TRHDX	Data Hold After $\overline{RD}$	0	–	0	–	
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL-70	
TLLDV	ALE to Valid Data In	–	517	–	8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		9TCLCL-165	
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	3TCLCL-50	3TCLCL+50	
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	203	–	4TCLCL-130	–	
TWHLH	$\overline{WR}$ or $\overline{RD}$ High to ALE High	43	123	TCLCL-40	TCLCL+40	
TDVWX	Data Valid to $\overline{WR}$ Transition	33		TCLCL-50		
TQVWH	Data Setup Before $\overline{WR}$	433	–	7TCLCL-150	–	
TWHQX	Data Hold After $\overline{WR}$	33		TCLCL-50		
TRLAZ	Address Float After $\overline{RD}$	–	0	–	0	

*) Interfacing the SAB 8051 to devices with float times up to 75ns is permissible. This limited bus contention will not caused any damage to Port 0 drivers.

A.C. Characteristics for SAB 8031-10/8051-10

TA 0°C to 70°C; VCC = 5 V ±5%; VSS = 0 V
(CL for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		10 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 10 MHz		
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	160		2TCLCL-40		
TAVLL	Address Setup to ALE	70	–	TCLCL-30	–	
TLLAX1	Address Hold After ALE	65		TCLCL-35		
TLLIV	ALE to Valid Instr In	–	300	–	4TCLCL-100	
TLLPL	ALE to $\overline{PSEN}$	75	–	TCLCL-25	–	ns
TPLPH	$\overline{PSEN}$ Pulse Width	265		3TCLCL-35		
TPLIV	$\overline{PSEN}$ to Valid Instr In	–	200	–	3TCLCL-100	
TPXIX	Input Instr Hold After $\overline{PSEN}$	0	–	0	–	
TPXIZ*)	Input Instr Float After $\overline{PSEN}$	–	80	–	TCLCL-20	
TPXAV*)	Address Valid After $\overline{PSEN}$	92	–	TCLCL-8	–	
TAVIV	Address to Valid Instr In	–	385	–	5TCLCL-115	
TAZPL	Address Float to $\overline{PSEN}$	0	–	0	–	

External Data Memory Characteristics

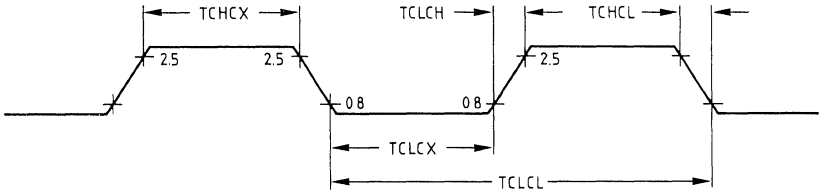
Symbol	Parameter	Limit Values				Unit
		10 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 10 MHz		
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	500		6TCLCL-100		
TWLWH	$\overline{WR}$ Pulse Width		–	6TCLCL-100	–	
TLLAX2	Address Hold After ALE	165		2TCLCL-35		
TRLDV	$\overline{RD}$ to Valid Data In	–	335	–	5TCLCL-165	
TRHDX	Data Hold After $\overline{RD}$	0	–	0	–	
TRHDZ	Data Float After $\overline{RD}$		130		2TCLCL-70	
TLLDV	ALE to Valid Data In	–	650	–	8TCLCL-150	ns
TAVDV	Address to Valid Data In		735		9TCLCL-165	
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	250	350	3TCLCL-50	3TCLCL+50	
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	270	–	4TCLCL-130	–	
TWHLH	$\overline{WR}$ or $\overline{RD}$ High to ALE High	60	140	TCLCL-40	TCLCL+40	
TDVWX	Data Valid to $\overline{WR}$ Transition	50		TCLCL-50		
TQVWH	Data Setup Before $\overline{WR}$	550	–	7TCLCL-150	–	
TWHQX	Data Hold After $\overline{WR}$	50		TCLCL-50		
TRLAZ	Address Float After $\overline{RD}$	–	0	–	0	

*) Interfacing the SAB 8051 to devices with float times up to 92ns is permissible. This limited bus contention will not caused any damage to Port 0 drivers.

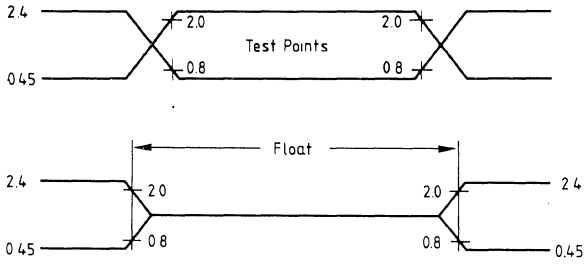
External Clock Drive XTAL2

Symbol	Parameter	Limit Values		Unit
		Variable Clock Freq = 1.2 MHz to 12 MHz (8031/8051) Freq = 1.2 MHz to 10 MHz (8031-10/8051-10)		
		Min	Max	
TCLCL	Oscillator Period 8031/8051 Oscillator Period 8031-10/8051-10	83.3 100	833.3	ns
TCHCX	High Time	20	TCLCL-TCLCX	
TCLCX	Low Time		TCLCL-TCHCX	
TCLCH	Rise Time	–	20	
TCHCL	Fall Time			

External Clock Cycle



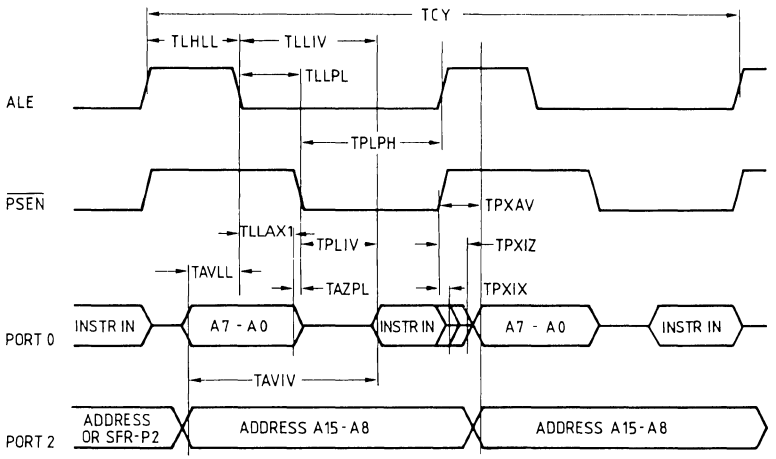
A.C. Testing Input, Output, Float Waveforms



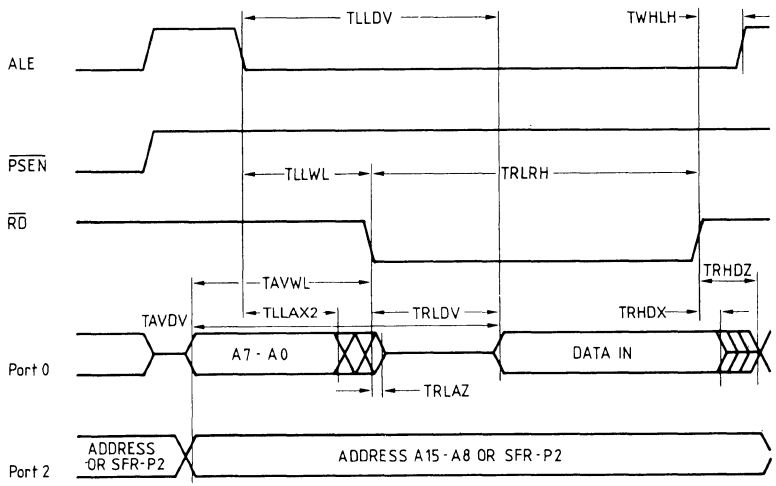
A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400 µA at the voltage test levels.

Waveforms

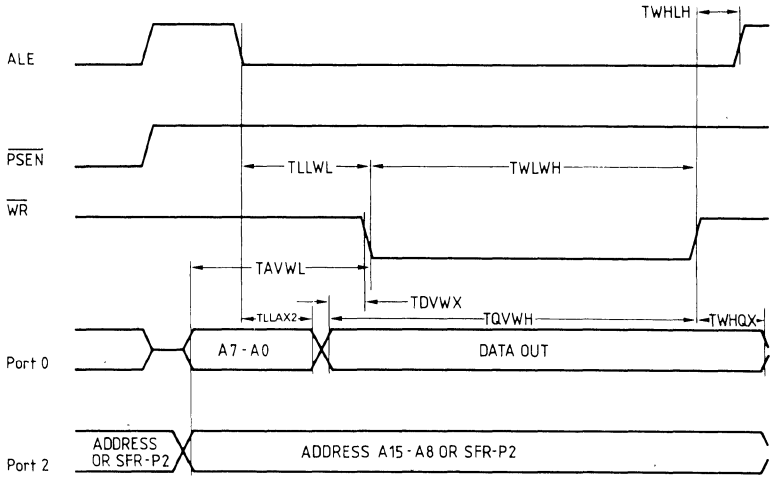
Program Memory Read Cycle



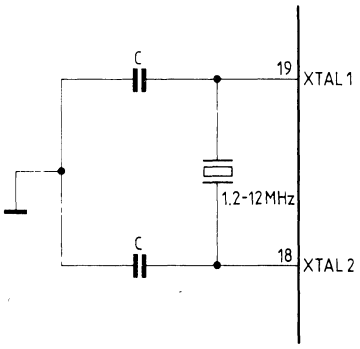
Data Memory Read Cycle



Data Memory Write Cycle

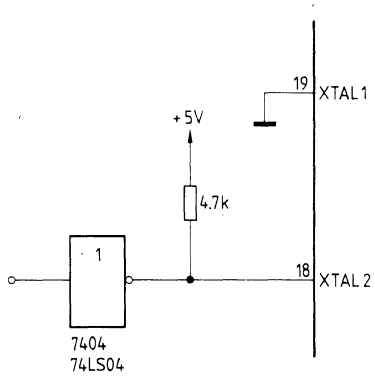


Recommended Oscillator Circuits



C = 30 pF ± 10 pF

Crystal Oscillator Mode



Driving from External Source

SAB 8031/8051
8-Bit Single Chip Microcomputer

Extended Temperature Range: −40 to + 85°C
−40 to +110°C

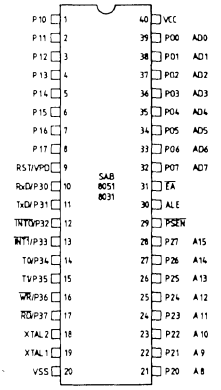
SAB 8051-P-T40/85
SAB 8051-P-T40/110 **Mask Programmable ROM**

- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-Bit Ports, 32 I/O Lines
- Two 16-Bit Timer/Event Counters
- High-Performance Full-Duplex Serial Channel
- External Memory Expandable to 128K
- Compatible with SAB 8080/8085 Peripherals

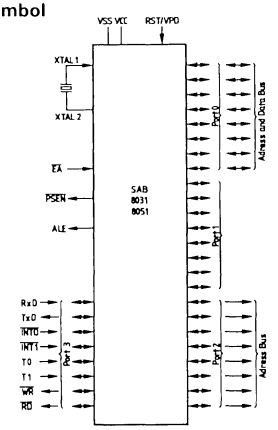
SAB 8031-P-T40/85
SAB 8031-P-T40/110 **External ROM**

- Boolean Processor
- SAB 8048 Architecture Enhanced with:
  - Non-Paged Jumps
  - Direct Addressing
  - Four 8-Register Banks
  - Stack Depth Up to 128-Bytes
  - Multiply, Divide, Subtract, Compare
- Single +5V Power Supply with ±10% Voltage Margins

Pin Configuration



Logic Symbol



The SAB 8031/8051 for the two extended temperature ranges (Industrial temperature range: −40 to +85 C, Automative temperature range: −40 to +110 C) is fully compatible with the standard SAB 8031/8051 with respect to architecture, instruction set, and software portability.

The SAB 8031/8051 is a stand-alone, high-performance single-chip computer fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 40-pin DIP.

The SAB 8031 is identical to the SAB 8051, except that it lacks the program memory.

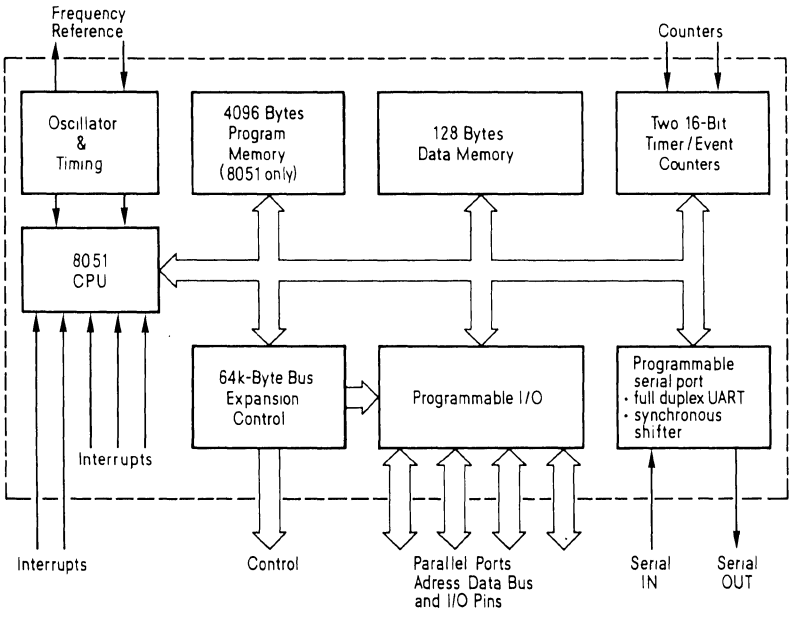
The SAB 8051 microcomputer, like the SAB 8048, is efficient both as a controller and as an arithmetic processor. The SAB 8051 has extensive facilities for binary and BCD arithmetic and excels in bit-handling capabilities. Among the many instructions added to the standard SAB 8048 instruction set are multiply, divide, subtract and compare.

Pin Description

Symbol	Number	Input (I) Output (O)	Function
P1.0–P1.7	1–8	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification.
RST/VPD	9	I	A high level on this pin resets the SAB 8051. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.0–P3.7	10–17	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of Port 3, as follows: – RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory. – $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.
XTAL1 XTAL2	19 18	I	XTAL 1 Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL2. XTAL2 Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0–P2.7	21–28	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification.
$\overline{PSEN}$	29	O	The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	O	Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.

Symbol	Number	Input (I) Output (O)	Function
$\overline{EA}$	31	I	When held at a high level, the SAB 8051 executes instructions from the internal ROM when the PC is less than 4096. When held at a low level, the SAB 8051 fetches all instructions from external Program Memory.
P0.0–P0.7	39–32	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification.
VCC	40		+5 V power supply during operation and program verification.
VSS	20		Circuit ground potential.

Block Diagram



Instruction Set Description

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to Accumulator	1	1
ADD	A, direct	Add direct byte to Accumulator	2	1
ADD	A, @Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry flag	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A w/Borrow	1	1
SUBB	A,#data	Subtract immediate data from A w/Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A & B	1	4
DA	A	Decimal Adjust Accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1

Data transfer

MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load Data Pointer with a 16-bit constant	3	2
Data transfer (cont.)				
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order Digit ind. RAM w/A	1	1
Boolean variable manipulation				
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute Subroutine Call	2	2
LCALL	addr 16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute Jump	2	2
LJMP	addr 16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if Carry flag not set	2	2
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp. immed. to A & Jump if Not Equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. & Jump if Not Equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. & Jump if Not Equal	3	2
DJNZ	Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ	direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7

direct – 128 internal RAM locations, any I/O port, control or status register

@Ri – Indirect internal RAM location addressed by register R0 or R1

#data – 8-bit constant included in instruction

#data 16 – 16-bit constant included as bytes 2 & 3 of instruction

bit – 128 software flags, any I/O pin, control or status bit

Notes on program addressing modes:

addr 16 – Destination address for LCALL & LJMP may be anywhere within the 64-Kilobyte program memory address space.

addr 11 – Destination address for ACALL & AJMP will be within the same 2-Kilobyte page of program memory as the first byte of the following instruction.

rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Opcodes in Hexadecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Opcodes in Hexadecimal Order (Continued)

Hex Code	Number of Bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Opcodes in Hexadecimal Order (Continued)

Hex Code	Number of Bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr*
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

Absolute Maximum Ratings[1)]

Ambient Temperature Under Bias	−40 to + 85°C for T40/85 −40 to +110°C for T40/110
Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground (VSS)	−0.5 to + 7 V
Power Dissipation	2 W

D.C. Characteristics

VCC = 5 V ±10%; VSS = 0 V; TA = −40 to + 85°C for T40/85;
TA = −40 to +110°C for T40/110

Symbol	Parameter		Limit Values			Units	Test Conditions
			Min.	Typ.	Max.		
VIL	Input Low Voltage	T40/85 T40/110	−0.5		0.8 0.7		−
VIH	Input High Voltage except RST/VPD and XTAL2	T40/85 T40/110	2.0 2.1		VCC+0.5		
VIH1	Input High Voltage to RST/VPD for Reset, XTAL2	T40/85 T40/110	2.5 2.8		−		XTAL1 to VSS
VPD	Power Down Voltage To RST/VPD		4.5		5.5		VCC = 0 V
VOL	Output Low Voltage Ports 1, 2, 3		−		0.45	V	IOL = 1.2 mA
VOL1	Output Low Voltage Port 0, ALE, /PSEN			−			IOL = 2.4 mA
VOH	Output High Voltage Ports 1, 2, 3	T40/85 T40/110	2.4		−		IOH = −60 µA IOH = −50 µA
VOH1	Output High Voltage Port 0, ALE, /PSEN	T40/85 T40/110					IOH = −400 µA IOH = −360 µA
IIL	Logical 0 Input Current Ports 1, 2, 3		−		−800	µA	VIL = 0.45 V
IIL2	Logical 0 Input Current XTAL2				−2.0	mA	XTAL1 = VSS VIL = 0.45 V
IIH1	Input High Current to RST/VPD for Reset				500	µA	VIN = VCC−1.5 V
ILI	Input Leakage Current to Port 0,/EA				±10		0 < VIN < VCC
ICC	Power Supply Current			−	175	mA	−
IPD	Power Down Current				20		
CIO	Capacitance of I/O Buffer				10	pF	f_c = 1 MHz

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics for T40/85

VCC = 5 V ±10%; VSS = 0 V; TA = −40 to +85°C
(CL for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		10 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 10 MHz		
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	160		2TCLCL-40		
TAVLL	Address Setup to ALE	70	–	TCLCL-30	–	
TLLAX	Address Hold After ALE	65		TCLCL-35		
TLLIV	ALE To Valid Instr In	–	300	–	4TCLCL-100	
TLLPL	ALE To $\overline{PSEN}$	75	–	TCLCL-25	–	ns
TPLPH	$\overline{PSEN}$ Pulse Width	265		3TCLCL-35		
TPLIV	$\overline{PSEN}$ To Valid Instr In	–	200	–	3TCLCL-100	
TPXIX	Input Instr Hold After $\overline{PSEN}$	0	–	0	–	
TPXIZ*)	Input Instr Float After $\overline{PSEN}$	–	80	–	TCLCL-20	
TPXAV*)	Address Valid After $\overline{PSEN}$	92	–	TCLCL-8	–	
TAVIV	Address To Valid Instr In	–	385	–	5TCLCL-115	
TAZPL	Address Float To $\overline{PSEN}$	0	–	0	–	

External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		10 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 10 MHz		
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	500		6TCLCL-100		
TWLWH	$\overline{WR}$ Pulse Width		–	6TCLCL-100	–	
TLLAX	Address Hold After ALE	65		TCLCL-35		
TRLDV	$\overline{RD}$ To Valid Data In	–	335	–	5TCLCL-165	
TRHDX	Data Hold After $\overline{RD}$	0	–	0	–	
TRHDZ	Data Float After $\overline{RD}$		130		2TCLCL-70	
TLLDV	ALE To Valid Data In	–	650	–	8TCLCL-150	ns
TAVDV	Address To Valid Data In		735		9TCLCL-165	
TLLWL	ALE To $\overline{WR}$ or $\overline{RD}$	250	350	3TCLCL-50	3TCLCL+50	
TAVWL	Address To $\overline{WR}$ or $\overline{RD}$	270	–	4TCLCL-130	–	
TWHLH	$\overline{WR}$ or $\overline{RD}$ High To ALE High	60	140	TCLCL-40	TCLCL+40	
TDVWX	Data Valid To $\overline{WR}$ Transition	50		TCLCL-50		
TQVWH	Data Setup Before $\overline{WR}$	550	–	7TCLCL-150	–	
TWHQX	Data Hold After $\overline{WR}$	50		TCLCL-50		
TRLAZ	Address Float After $\overline{RD}$	–	0	–	0	

*) Interfacing the SAB 8051 to devices with float times up to 92ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

A.C. Characteristics for T40/110

VCC = 5 V ±10%; VSS = 0 V; TA = −40 to +110°C
(CL for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		8 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 8 MHz		
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	210	–	2TCLCL-40	–	ns
TAVLL	Address Setup to ALE	90		TCLCL-35		
TLLAX	Address Hold After ALE	85		TCLCL-40		
TLLIV	ALE To Valid Instr In	–	375	–	4TCLCL-125	
TLLPL	ALE To $\overline{PSEN}$	100	–	TCLCL-25	–	
TPLPH	$\overline{PSEN}$ Pulse Width	340		3TCLCL-35		
TPLIV	$\overline{PSEN}$ To Valid Instr In	–	250	–	3TCLCL-125	
TPXIX	Input Instr Hold After $\overline{PSEN}$	0	–	0	–	
TPXIZ*)	Input Instr Float After $\overline{PSEN}$	–	105	–	TCLCL-20	
TPXAV*)	Address Valid After $\overline{PSEN}$	112	–	TCLCL-13	–	
TAVIV	Address To Valid Instr In	–	485	–	5TCLCL-140	
TAZPL	Address Float To $\overline{PSEN}$	0	–	0	–	

External Data Memory Characteristics

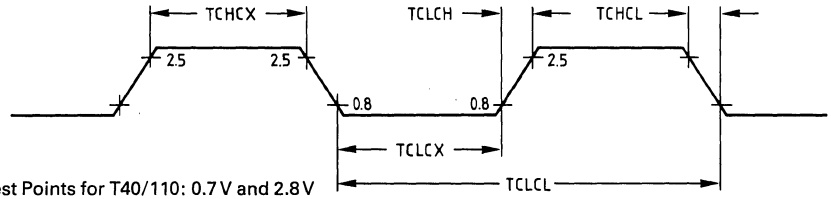
Symbol	Parameter	Limit Values				Unit
		8 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 8 MHz		
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	650	–	6TCLCL-100	–	ns
TWLWH	$\overline{WR}$ Pulse Width			6TCLCL-100		
TLLAX	Address Hold After ALE	85		TCLCL-40		
TRLDV	$\overline{RD}$ To Valid Data In	–	460	–	5TCLCL-165	
TRHDX	Data Hold After $\overline{RD}$	0	–	0	–	
TRHDZ	Data Float After $\overline{RD}$	–	180	–	2TCLCL-70	
TLLDV	ALE To Valid Data In		850		8TCLCL-150	
TAVDV	Address To Valid Data In		960		9TCLCL-165	
TLLWL	ALE To $\overline{WR}$ or $\overline{RD}$	325	425	3TCLCL-50	3TCLCL+50	
TAVWL	Address To $\overline{WR}$ or $\overline{RD}$	370	–	4TCLCL-130	–	
TWHLH	$\overline{WR}$ or $\overline{RD}$ High To ALE High	85	165	TCLCL-40	TCLCL+40	
TDVWX	Data Valid To $\overline{WR}$ Transition	75	–	TCLCL-50	–	
TQVWH	Data Setup Before $\overline{WR}$	725		7TCLCL-150		
TWHQX	Data Hold After $\overline{WR}$	75		TCLCL-50		
TRLAZ	Address Float After $\overline{RD}$	–	0	–	0	

*) Interfacing the SAB 8051 to devices with float times up to 112ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

External Clock Drive XTAL2

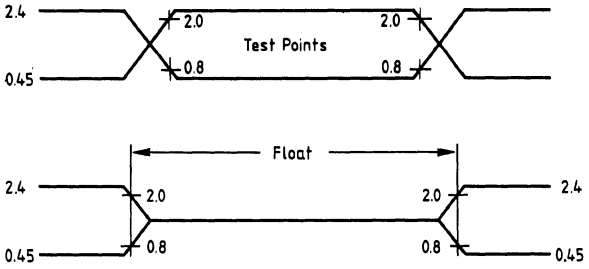
Symbol	Parameter	Limit Values		Unit
		Variable Clock Freq = 1.2 MHz to 10 MHz (T40/85) Freq = 1.2 MHz to 8 MHz (T40/110)		
		Min	Max	
TCLCL	Oscillator Period T40/85 T40/110	100 125	833.3	ns
TCHCX	High Time	20	TCLCL-TCLCX	
TCLCX	Low Time		TCLCL-TCHCX	
TCLCH	Rise Time	–	20	
TCHCL	Fall Time			

External Clock Cycle



Test Points for T40/110: 0.7 V and 2.8 V

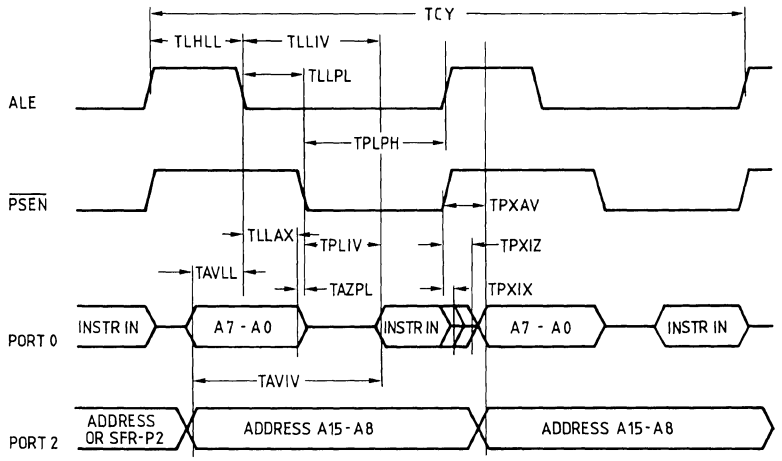
A.C. Testing Input, Output, Float Waveforms



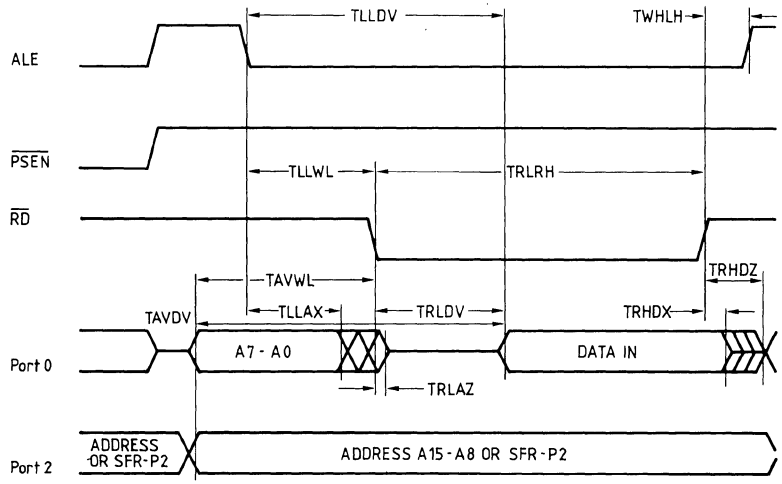
AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

Waveforms

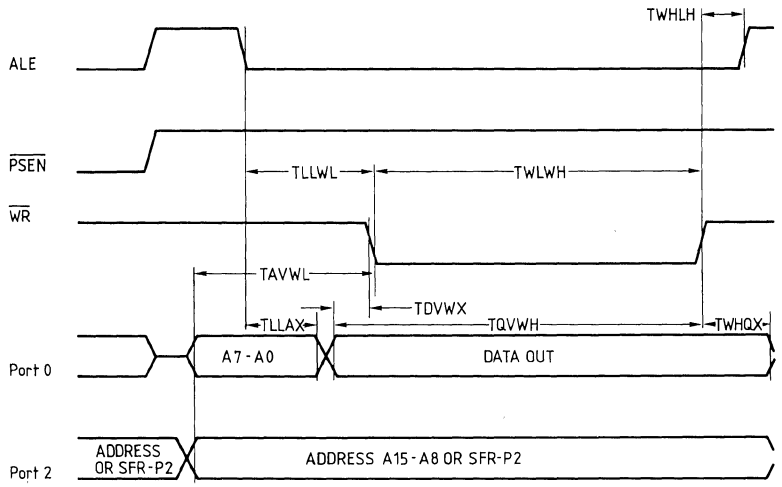
Program Memory Read Cycle



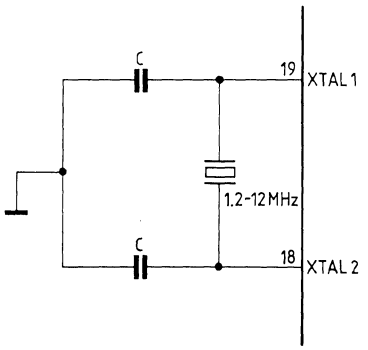
Data Memory Read Cycle



Data Memory Write Cycle

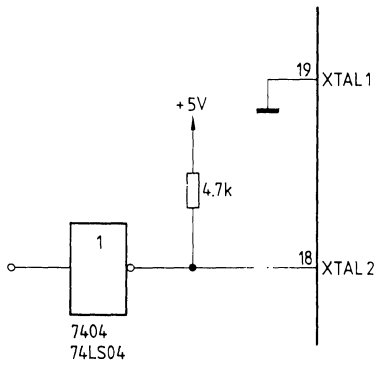


Recommended Oscillator Circuits



C = 30 pF ± 10 pF

Crystal Oscillator Mode



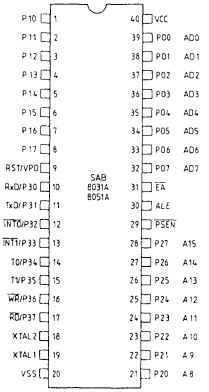
Driving from External Source

SAB 8031A/8051A
SAB 8031A-15/8051A-15
8-Bit Single Chip Microcomputer

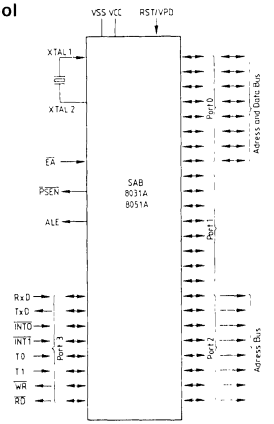
SAB 8031A/8031A-15 Control Oriented CPU with RAM and I/O
SAB 8051A/8051A-15 A SAB 8031A with Factory Mask-Programmable ROM

- SAB 8031A/8051A, 12 MHz Operation
  SAB 8031A-15/8051A-15, 15 MHz Operation
- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-Bit Ports, 32 I/O Lines
- Two 16-Bit Timer/Event Counters
- High-Performance Full-Duplex Serial Channel
- External Memory Expandable to 128K
- Compatible with SAB 8080/8085 Peripherals
- Boolean Processor
- 218 User Bit-Addressable Locations
- Most Instruction Execute in:
  1 µs (SAB 8031A/8051A)
  800 ns (SAB 8031A-15/8051A-15)
- 4 µs (3.2 µs) Multiply and Divide

Pin Configuration



Logic Symbol



The SAB 8031A/8051A is a stand-alone, high-performance single-chip computer fabricated in +5V advanced Siemens MYMOS technology and packaged in a 40-pin DIP. It provides the hardware features, architectural enhancements and new instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data storage.

The SAB 8051A contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The SAB 8031A is identical, except that it lacks the program memory.

For systems that require extra capability, the SAB 8051A can be expanded using standard TTL compatible memories and the byte oriented SAB 8080 and SAB 8085 peripherals.

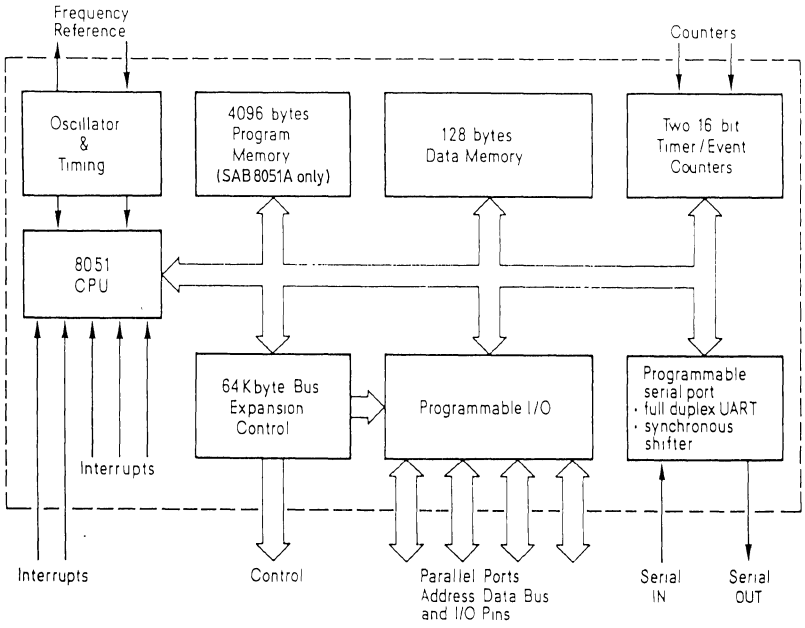
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Functions
P1.0–P1.7	1–8	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.
RST/VPD	9	I	A high level on this pin resets the SAB 8051A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.0–P3.7	10–17	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: – RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	I	XTAL 1 input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0–P2.7	21–28	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
$\overline{PSEN}$	29	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Functions
$\overline{EA}$	31	I	When held at a TTL high level, the SAB 8051A executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 8051A fetches all instructions from external program memory. For the SAB 8031A this pin must be tied low.
P0.0–P0.7	39–32	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
VCC	40		+5V power supply during operation and program verification.
VSS	20		Circuit ground potential.

Block Diagram



Instruction Set Description

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to Accumulator	1	1
ADD	A, direct	Add direct byte to Accumulator	2	1
ADD	A, @Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry flag	1	1
ADDC	A,direct	Add direct byte to Accu with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to Accu with Carry flag	1	1
ADDC	A,#data	Add immediate data to Accu with Carry flag	2	1
SUBB	A,Rn	Subtract register from Accu with borrow	1	1
SUBB	A,direct	Subtract direct byte from Accu with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A & B	1	4
DA	A	Decimal adjust Accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator left	1	1
RLC	A	Rotate A left through the Carry flag	1	1
RR	A	Rotate Accumulator right	1	1
RRC	A	Rotate A right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1

Data transfer

MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
Data transfer (cont.)				
MOVC	A,@A+DPTR	Move code byte relative to DPTR to Accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to Accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr) to Accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr) to Accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit ind. RAM with Accu	1	1
Boolean variable manipulation				
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is zero	2	2
JNZ	rel	Jump if Accumulator is not zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if Carry flag is not set	2	2
JB	bit,rel	Jump if direct bit set	3	2
JNB	bit,rel	Jump if direct bit not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct to accu and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to accu and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 & 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL & LJMP may be anywhere within the 64-Kbyte program memory address space.
addr 11 – Destination address for ACALL & AJMP will be within the same 2-Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Opcodes in Hexadecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A

Hex Code	Number of Bytes	Mnemonic	Operands
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr*
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

Absolute Maximum Ratings[1)]

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground (VSS)	−0.5 to + 7 V
Power Dissipation	2 W

D.C. Characteristics

TA = 0 to 70°C; VCC = 5 V ± 10%; VSS = 0 V

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
VIL	Input Low Voltage	−0.5	0.8	V	–
VIH	Input High Voltage (Except RST/VPD and XTAL2)	2.0	VCC+0.5		
VIH1	Input High Voltage to RST/VPD for Reset, XTAL2	2.5			XTAL1 to VSS
VPD	Power Down Voltage to RST/VPD	4.5	5.5		VCC = 0V
VOL	Output Low Voltage Ports 1, 2, 3	–	0.45		IOL = 1.6 mA
VOL1	Output Low Voltage Port 0, ALE, /PSEN				IOL = 3.2 mA
VOH	Output High Voltage Ports 1, 2, 3	2.4	–		IOH = −80 µA
VOH1	Output High Voltage Port 0, ALE, /PSEN				IOH = −400 µA
IIL	Logical 0 Input Current Ports 1, 2, 3	–	−800	µA	VIL = 0.45 V
IIL2	Logical 0 Input Current XTAL 2		−2.0	mA	XTAL1 = VSS VIL = 0.45 V
IIH1	Input High Current to RST/VPD for Reset		500	µA	VIN = VCC−1.5 V
ILI	Input Leakage Current to Port 0,/EA		±10		0V < VIN < VCC
ICC	Power Supply Current SAB 8031A/8051A SAB 8031A-15/8051A-15		 125 140	mA	All outputs disconnected
IPD	Power Down Current		10		VCC = 0V
CIO	Capacitance of I/O Buffer		10	pF	f_c = 1 MHz

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics for SAB 8031A/8051A

TA 0 to 70°C; VCC = 5 V ±10%; VSS = 0 V
(CL for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	127		2TCLCL-40		
TAVLL	Address Setup to ALE	53	–	TCLCL-30	–	
TLLAX1	Address Hold After ALE	48		TCLCL-35		
TLLIV	ALE to Valid Instr In	–	233	–	4TCLCL-100	
TLLPL	ALE to $\overline{PSEN}$	58		TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215	–	3TCLCL-35	–	
TPLIV	$\overline{PSEN}$ to Valid Instr In	–	150	–	3TCLCL-100	
TPXIX	Input Instr Hold After $\overline{PSEN}$	0	–	0	–	
TPXIZ*)	Input Instr Float After $\overline{PSEN}$	–	63	–	TCLCL-20	
TPXAV*)	Address Valid After $\overline{PSEN}$	75	–	TCLCL-8	–	
TAVIV	Address to Valid Instr In	–	302	–	5TCLCL-115	
TAZPL	Address Float to $\overline{PSEN}$	0	–	0	–	

External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL-100		
TWLWH	$\overline{WR}$ Pulse Width		–		–	
TLLAX2	Address Hold After ALE	132		2TCLCL-35		
TRLDV	$\overline{RD}$ to Valid Data In	–	250	–	5TCLCL-165	
TRHDX	Data Hold After $\overline{RD}$	0	–	0	–	
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL-70	
TLLDV	ALE to Valid Data In	–	517	–	8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		9TCLCL-165	
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	3TCLCL-50	3TCLCL+50	
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	203	–	4TCLCL-130	–	
TWHLH	$\overline{WR}$ or $\overline{RD}$ High to ALE High	43	123	TCLCL-40	TCLCL+40	
TDVWX	Data Valid to $\overline{WR}$ Transition	33		TCLCL-50		
TQVWH	Data Setup Before $\overline{WR}$	433	–	7TCLCL-150	–	
TWHQX	Data Hold After $\overline{WR}$	33		TCLCL-50		
TRLAZ	Address Float After $\overline{RD}$	–	0	–	0	

*) Interfacing the SAB 8051A to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

External Clock Drive XTAL2

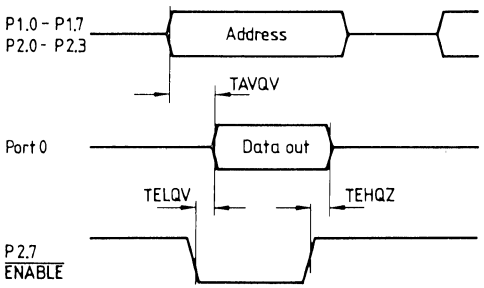
Symbol	Parameter	Limit Values		Unit
		Variable Clock Freq = 1.2 MHz to 12 MHz		
		Min	Max	
TCLCL	Oscillator Period	83.3	833.3	ns
TCHCX	High Time	20	TCLCL-TCLCX	
TCLCK	Low Time		TCLCL-TCHCX	
TCLCH	Rise Time	–	20	
TCHCL	Fall Time			

ROM Verification Characteristics for SAB 8051A

TA = 25°C ±5°C; VCC = 5V ±10%; VSS = 0V

Symbol	Parameter	Limit Values		Unit
		Min	Max	
TAVQV	Address to Valid Data	–	48 TCLCL	ns
TELQV	$\overline{\text{Enable}}$ to Valid Data			
TEHQZ	Data Float after $\overline{\text{Enable}}$	0		
1/TCLCL	Oscillator Frequency	4	6	MHz

ROM Verification



Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11
Data: Port 0 = D0–D7

Inputs: P2.4–P2.6, $\overline{\text{PSEN}}$ = VSS
ALE, $\overline{\text{EA}}$ = TTL high level
RST/VPD = VIH1

A.C. Characteristics for SAB 8031A-15/8051A-15

TA 0 to 70°C; VCC = 5V ±10%; VSS = 0V
(CL for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		15 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 15 MHz		
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	93		2TCLCL-40		
TAVLL	Address Setup to ALE	37	–	TCLCL-30	–	
TLLAX1	Address Hold After ALE	32		TCLCL-35		
TLLIV	ALE to Valid Instr In	–	167	–	4TCLCL-100	
TLLPL	ALE to $\overline{PSEN}$	42	–	TCLCL-25	–	ns
TPLPH	$\overline{PSEN}$ Pulse Width	165		3TCLCL-35		
TPLIV	$\overline{PSEN}$ to Valid Instr In	–	100	–	3TCLCL-100	
TPXIX	Input Instr Hold After $\overline{PSEN}$	0	–	0	–	
TPXIZ*)	Input Instr Float After $\overline{PSEN}$	–	52	–	TCLCL-15	
TPXAV*)	Address Valid After $\overline{PSEN}$	64	–	TCLCL-3	–	
TAVIV	Address to Valid Instr In	–	243	–	5TCLCL-90	
TAZPL	Address Float to $\overline{PSEN}$	0	–	0	–	

External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		15 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 15 MHz		
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	300	–	6TCLCL-100	–	
TWLWH	$\overline{WR}$ Pulse Width					
TLLAX2	Address Hold After ALE	98		2TCLCL-35		
TRLDV	$\overline{RD}$ to Valid Data In	–	168	–	5TCLCL-165	
TRHDX	Data Hold After $\overline{RD}$	0	–	0	–	
TRHDZ	Data Float After $\overline{RD}$	–	63	–	2TCLCL-70	
TLLDV	ALE to Valid Data In		383		8TCLCL-150	ns
TAVDV	Address to Valid Data In		435		9TCLCL-165	
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	150	250	3TCLCL-50	3TCLCL+50	
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	137	–	4TCLCL-130	–	
TWHLH	$\overline{WR}$ or $\overline{RD}$ High to ALE High	27	107	TCLCL-40	TCLCL+40	
TDVWX	Data Valid to $\overline{WR}$ Transition	17	–	TCLCL-50	–	
TQVWH	Data Setup Before $\overline{WR}$	317		7TCLCL-150		
TWHQX	Data Hold After $\overline{WR}$	17		TCLCL-50		
TRLAZ	Address Float After $\overline{RD}$	–	0	–	0	

*) Interfacing the SAB 8051A-15 to devices with float times up to 60ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

External Clock Drive XTAL2

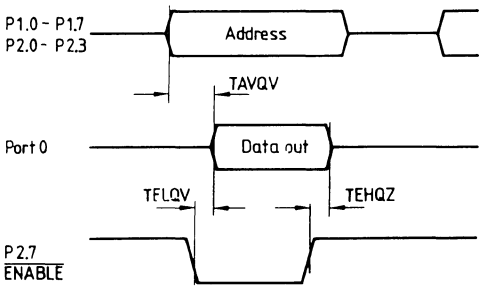
Symbol	Parameter	Limit Values		Unit
		Variable Clock Freq = 1.2 MHz to 15 MHz		
		Min	Max	
TCLCL	Oscillator Period	66.6	833.3	ns
TCHCX	High Time	15	TCLCL-TCLCX	ns
TCLCK	Low Time		TCLCL-TCHCX	ns
TCLCH	Rise Time	–	15	ns
TCHCL	Fall Time			ns

ROM Verification Characteristics for SAB 8051A-15

TA = 25°C ±5°C; VCC = 5 V ±10%; VSS = 0 V

Symbol	Parameter	Limit Values		Unit
		Min	Max	
TAVQV	Address to Valid Data	–	48 TCLCL	ns
TELQV	$\overline{\text{Enable}}$ to Valid Data			ns
TEHQZ	Data Float after $\overline{\text{Enable}}$	0		ns
1/TCLCL	Oscillator Frequency	4	6	MHz

ROM Verification

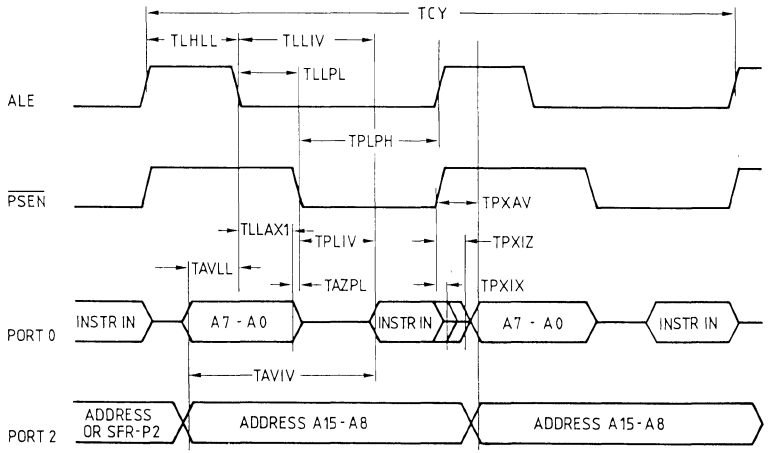


Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11
Data: Port 0 = D0–D7

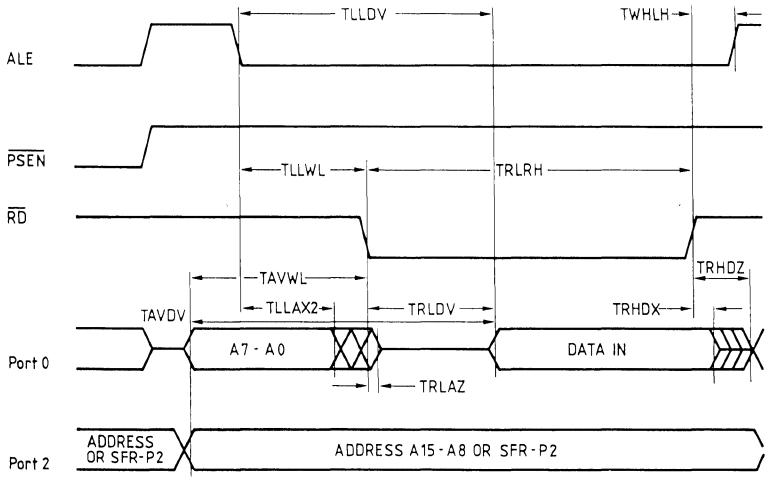
Inputs: P2.4–P2.6, $\overline{\text{PSEN}}$ = VSS
ALE, $\overline{\text{EA}}$ = TTL high level
RST/VPD = VIH1

Waveforms

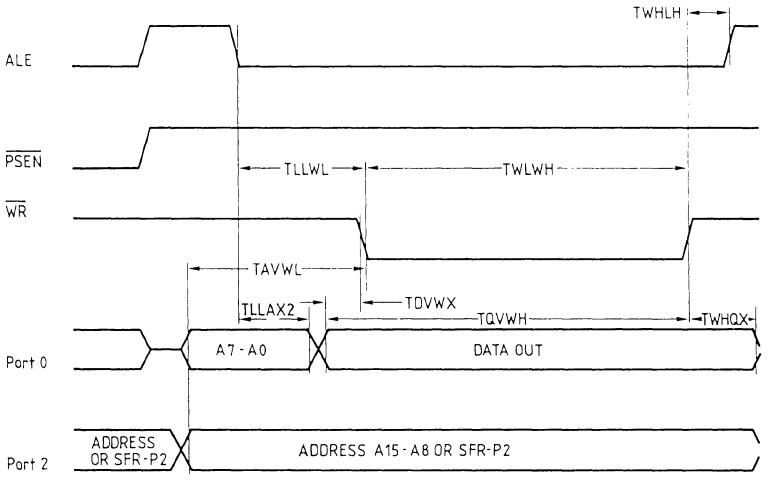
Program Memory Read Cycle



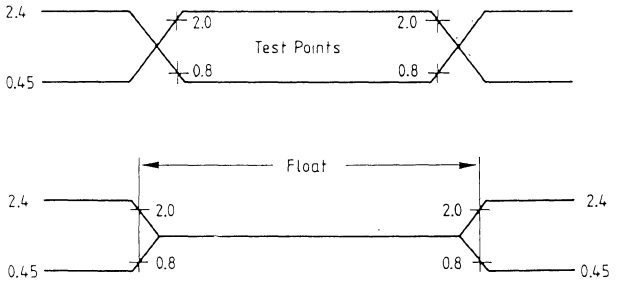
Data Memory Read Cycle



Data Memory Write Cycle

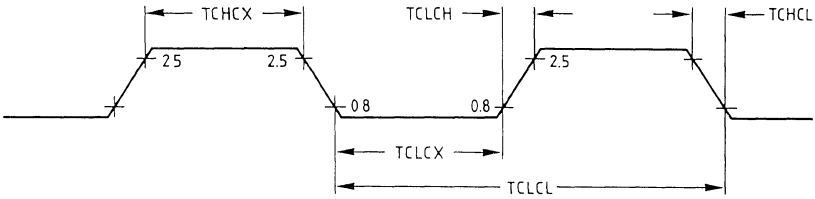


A.C. Testing Input, Output, Float Waveforms

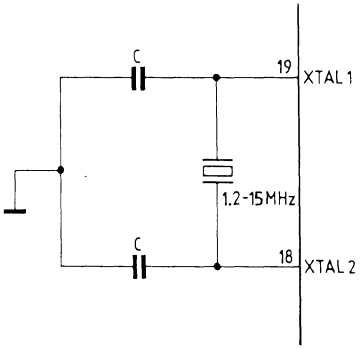


A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" ans 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400 µA at the voltage test levels.

External Clock Cycle

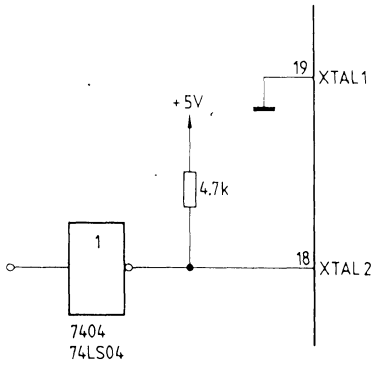


Recommended Oscillator Circuits



C = 30 pF ± 10 pF

Crystal Oscillator Mode



Driving from External Source

SAB 8031A/8051A Ext. Temp. 8-Bit Single Chip Microcomputer

Extended Temperature Range: −40 to + 85°C
−40 to +110°C

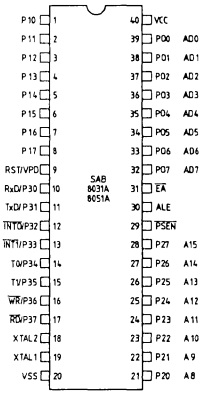
SAB 8051A-12-P-T40/85 **Mask Programmable ROM**
SAB 8051A-10-P-T40/110

- Advanced Version of the SAB 8031/8051 for Extended Temperature Range
- SAB 8031A/8051A-12-T40/85: 12 MHz Operation
- SAB 8031A/8051A-10-T40/110: 10 MHz Operation
- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-bit Ports, 32 I/O Lines

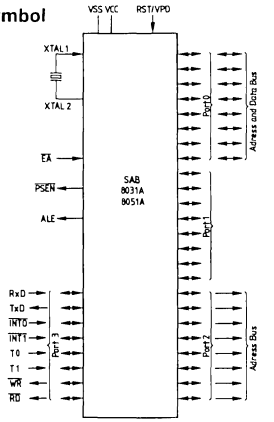
SAB 8031A-12-P-T40/85 **External ROM**
SAB 8031A-10-P-T40/110

- Two 16-bit Timer/Event Counters
- High-Performance Full-Duplex Serial Channel
- External Memory Expandable up to 128K
- Compatible with SAB 8080/8085 Peripherals
- Boolean Processor
- 218 User bit-Addressable Locations
- Most Instructions Execute in 1 µs
- 4 µs Multiply and Divide

Pin Configuration



Logic Symbol



The SAB 8031A/8051A for the two extended temperature ranges (Industrial temperature range: −40 to +85°C, Automotive temperature range: −40 to +110°C) is fully compatible with the standard SAB 8031A/8051A with respect to architecture, instruction set, and software portability.

The SAB 8031A/8051A is a stand-alone, high-performance single-chip computer fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 40-pin DIP.

The SAB 8051A contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full duplex UART; and on-chip oscillator and clock circuits. The SAB 8031A is identical, except that it lacks the program memory.

For systems that require extra capability, the SAB 8051A can be expanded using standard TTL compatible memories and the byte oriented SAB 8080 and SAB 8085 peripherals.

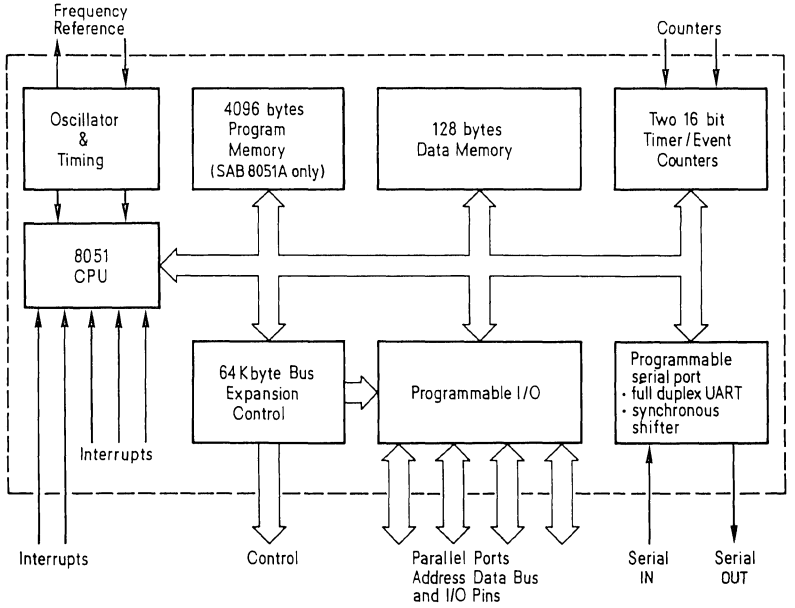
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Functions
P1.0–P1.7	1–8	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification.
RST/VPD	9	I	A high level on this pin resets the SAB 8051A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.0–P3.7	10–17	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of Port 3, as follows: – RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from Port 0 into the External Data Memory. – $\overline{RD}$ (P3.7). The read control signal enables External Data Memory to Port 0.
XTAL1 XTAL2	19 18	I	XTAL 1 Input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL2. XTAL2 Output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0–P2.7	21–28	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification.
$\overline{PSEN}$	29	O	The Program Store Enable output is a control signal that enables the external Program Memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.
ALE	30	O	Provides Address Latch Enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
$\overline{EA}$	31	I	When held at a high level, the SAB 8051A executes instructions from the internal ROM when the PC is less than 4096. When held at a low level, the SAB 8051A fetches all instructions from external Program Memory. For the SAB 8031A this pin must be tied low.
P0.0–P0.7	39–32	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification.
VCC	40		+5V power supply during operation and program verification.
VSS	20		Circuit ground potential.

Block Diagram



Instruction Set Description

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to Accumulator	1	1
ADD	A, direct	Add direct byte to Accumulator	2	1
ADD	A, @Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry flag	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A w/Borrow	1	1
SUBB	A,#data	Subtract immediate data from A w/Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment Data Pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A & B	1	4
DA	A	Decimal Adjust Accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1
Data transfer				
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct *)	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2

*) MOV A,ACC is not a valid instruction

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load Data Pointer with a 16-bit constant	3	2
Data transfer (cont.)				
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order Digit ind. RAM w/A	1	1
Boolean variable manipulation				
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute Subroutine Call	2	2
LCALL	addr 16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute Jump	2	2
LJMP	addr 16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if Carry flag not set	2	2
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp. immed. to A & Jump if Not Equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. & Jump if Not Equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. & Jump if Not Equal	3	2
DJNZ	Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ	direct,rel	Decrement direct & Jump if Not Zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 & 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit

Notes on program addressing modes:

addr 16 – Destination address for LCALL & LJMP may be anywhere within the 64-Kilobyte program memory address space.
addr 11 – Destination address for ACALL & AJMP will be within the same 2-Kilobyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Opcodes in Hexadecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A

Hex Code	Number of Bytes	Mnemonic	Operands
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr,data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data,code addr*
B5	3	CJNE	A,*data addr,code addr*
B6	3	CJNE	@R0,#*data,code addr*
B7	3	CJNE	@R1,#*data,code addr*
B8	3	CJNE	R0,#*data,code addr*
B9	3	CJNE	R1,#*data,code addr*
BA	3	CJNE	R2,#*data,code addr*
BB	3	CJNE	R3,#*data,code addr*
BC	3	CJNE	R4,#*data,code addr*
BD	3	CJNE	R5,#*data,code addr*
BE	3	CJNE	R6,#*data,code addr*
BF	3	CJNE	R7,#*data,code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *)
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*) MOV A,ACC is not a valid instruction

Absolute Maximum Ratings[1)]

Ambient Temperature Under Bias	−40 to + 85°C for T40/85 −40 to +110°C for T40/110
Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground (VSS)	−0.5 to + 7 V
Power Dissipation	2 W

D.C. Characteristics

VCC = 5 V ± 10%; VSS = 0 V TA = −40 to + 85°C for T40/85;
TA = −40 to +110°C for T40/110

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
VIL	Input Low Voltage	−0.5	0.8	V	–
VIH	Input High Voltage except RST/VPD and XTAL2	2.0	VCC+0.5		–
VIH1	Input High Voltage to RST/VPD for Reset, XTAL2	2.5			XTAL 1 to VSS
VPD	Power Down Voltage To RST/VPD	4.5	5.5		VCC = 0 V
VOL	Output Low Voltage Ports 1, 2, 3	–	0.45		IOL = 1.6 mA
VOL1	Output Low Voltage Port 0, ALE, /PSEN				IOL = 3.2 mA
VOH	Output High Voltage Ports 1, 2, 3	2.4	–		IOH = −80 µA
VOH1	Output High Voltage Port 0, ALE, /PSEN				IOH = −400 µA
IIL	Logical 0 Input Current Ports 1, 2, 3	–	−800	µA	VIL = 0.45 V
IIL2	Logical 0 Input Current XTAL2		−2.5	mA	XTAL1 = VSS VIL = 0.45 V
IIH1	Input High Current to RST/VPD for Reset		500	µA	VIN = VCC−1.5 V
ILI	Input Leakage Current to Port 0,/EA		±10		0 < VIN < VCC
ICC	Power Supply Current		150	mA	–
IPD	Power Down Current		15		
CIO	Capacitance of I/O Buffer		10	pF	fc = 1 MHz

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics for T40/85

VCC = 5V ±10%; VSS = 0V; TA = −40 to +85°C
(CL for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	127		2TCLCL-40		
TAVLL	Address Setup to ALE	53	–	TCLCL-30	–	
TLLAX1	Address Hold After ALE	48		TCLCL-35		
TLLIV	ALE To Valid Instr In	–	233	–	4TCLCL-100	
TLLPL	ALE To $\overline{PSEN}$	58	–	TCLCL-25	–	ns
TPLPH	$\overline{PSEN}$ Pulse Width	215		3TCLCL-35		
TPLIV	$\overline{PSEN}$ To Valid Instr In	–	150	–	3TCLCL-100	
TPXIX	Input Instr Hold After $\overline{PSEN}$	0	–	0	–	
TPXIZ*)	Input Instr Float After $\overline{PSEN}$	–	63	–	TCLCL-20	
TPXAV*)	Address Valid After $\overline{PSEN}$	75	–	TCLCL-8	–	
TAVIV	Address To Valid Instr In	–	302	–	5TCLCL-115	
TAZPL	Address Float To $\overline{PSEN}$	0	–	0	–	

External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL-100		
TWLWH	$\overline{WR}$ Pulse Width		–	6TCLCL-100	–	
TLLAX2	Address Hold After ALE	132		2TCLCL-35		
TRLDV	$\overline{RD}$ To Valid Data In	–	250	–	5TCLCL-165	
TRHDX	Data Hold After $\overline{RD}$	0	–	0	–	
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL-70	
TLLDV	ALE To Valid Data In	–	517	–	8TCLCL-150	ns
TAVDV	Address To Valid Data In		585		9TCLCL-165	
TLLWL	ALE To $\overline{WR}$ or $\overline{RD}$	200	300	3TCLCL-50	3TCLCL+50	
TAVWL	Address To $\overline{WR}$ or $\overline{RD}$	203	–	4TCLCL-130	–	
TWHLH	$\overline{WR}$ or $\overline{RD}$ High To ALE High	43	123	TCLCL-40	TCLCL+40	
TDVWX	Data Valid To $\overline{WR}$ Transition	33		TCLCL-50		
TQVWH	Data Setup Before $\overline{WR}$	433	–	7TCLCL-150	–	
TWHQX	Data Hold After $\overline{WR}$	33		TCLCL-50		
TRLAZ	Address Float After $\overline{RD}$	–	0	–	0	

*) Interfacing the SAB 8051A to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

A.C. Characteristics for T40/110

VCC = 5V ±10%; VSS = 0V; TA = −40 to +110°C
(CL for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		10 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 10 MHz		
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	160	–	2TCLCL-40	–	ns
TAVLL	Address Setup to ALE	70		TCLCL-30		
TLLAX1	Address Hold After ALE	65		TCLCL-35		
TLLIV	ALE To Valid Instr In	–	300	–	4TCLCL-100	
TLLPL	ALE To $\overline{PSEN}$	75	–	TCLCL-25	–	
TPLPH	$\overline{PSEN}$ Pulse Width	265		3TCLCL-35		
TPLIV	$\overline{PSEN}$ To Valid Instr In	–	200	–	3TCLCL-100	
TPXIX	Input Instr Hold After $\overline{PSEN}$	0	–	0	–	
TPXIZ*)	Input Instr Float After $\overline{PSEN}$	–	80	–	TCLCL-20	
TPXAV*)	Address Valid After $\overline{PSEN}$	92	–	TCLCL-8	–	
TAVIV	Address To Valid Instr In	–	385	–	5TCLCL-115	
TAZPL	Address Float To $\overline{PSEN}$	0	–	0	–	

External Data Memory Characteristics

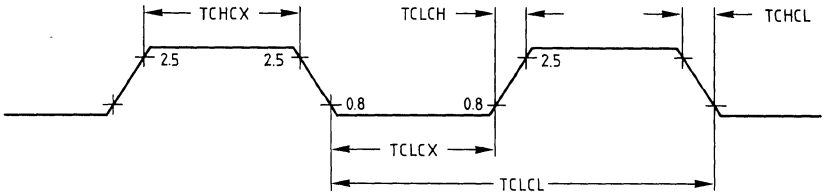
Symbol	Parameter	Limit Values				Unit
		10 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 10 MHz		
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	500	–	6TCLCL-100	–	ns
TWLWH	$\overline{WR}$ Pulse Width			6TCLCL-100		
TLLAX2	Address Hold After ALE	165		2TCLCL-35		
TRLDV	$\overline{RD}$ To Valid Data In	–	335	–	5TCLCL-165	
TRHDX	Data Hold After $\overline{RD}$	0	–	0	–	
TRHDZ	Data Float After $\overline{RD}$	–	130	–	2TCLCL-70	
TLLDV	ALE To Valid Data In		650		8TCLCL-150	
TAVDV	Address To Valid Data In		735		9TCLCL-165	
TLLWL	ALE To $\overline{WR}$ or $\overline{RD}$	250	350	3TCLCL-50	3TCLCL+50	
TAVWL	Address To $\overline{WR}$ or $\overline{RD}$	270	–	4TCLCL-130	–	
TWHLH	$\overline{WR}$ or $\overline{RD}$ High To ALE High	60	140	TCLCL-40	TCLCL+40	
TDVWX	Data Valid To $\overline{WR}$ Transition	50	–	TCLCL-50	–	
TQVWH	Data Setup Before $\overline{WR}$	550		7TCLCL-150		
TWHQX	Data Hold After $\overline{WR}$	50		TCLCL-50		
TRLAZ	Address Float After $\overline{RD}$	–	0	–	0	

*) Interfacing the SAB 8051A to devices with float times up to 92ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

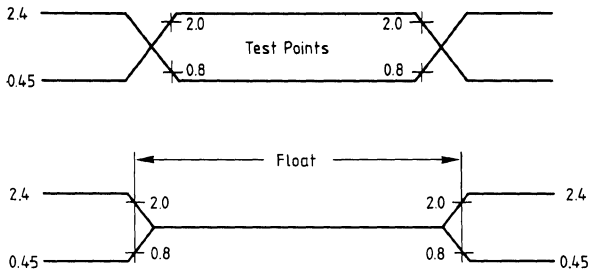
External Clock Drive XTAL2

Symbol	Parameter	Limit Values		Unit
		Variable Clock Freq = 1.2 MHz to 12 MHz (T40/85) Freq = 1.2 MHz to 10 MHz (T40/110)		
		Min	Max	
TCLCL	Oscillator Period T40/85 T40/110	83.3 100	833.3	ns
TCHCX	High Time	20	TCLCL-TCLCX	
TCLCX	Low Time		TCLCL-TCHCX	
TCLCH	Rise Time	–	20	
TCHCL	Fall Time			

External Clock Cycle



A.C. Testing Input, Output, Float Waveforms



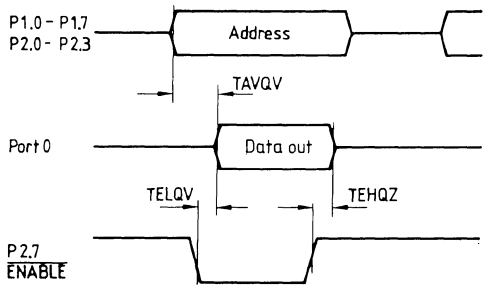
AC testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

ROM Verification Characteristics —

TA = 25°C ±5°C; VCC = 5 V ±10%; VSS = 0 V

Symbol	Parameter	Limit Values		Unit
		Min	Max	
TAVQV	Address to Valid Data	–	48 TCLCL	ns
TELQV	$\overline{\text{Enable}}$ to Valid Data			
TEHQZ	Data Float after $\overline{\text{Enable}}$	0		
1/TCLCL	Oscillator Frequency	4	6	MHz

ROM Verification

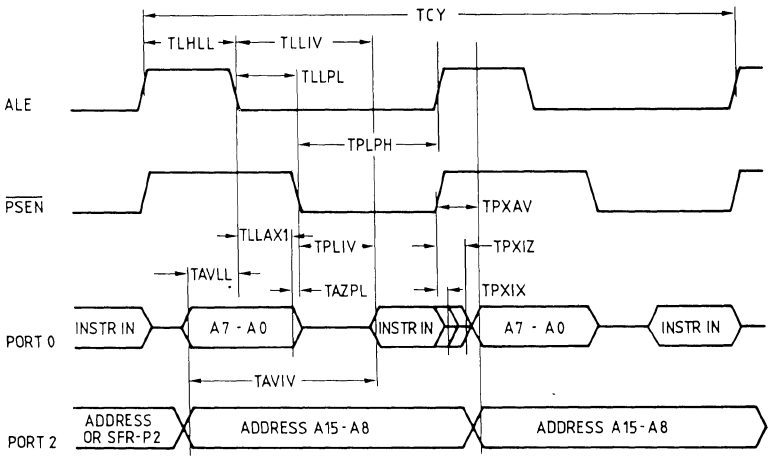


Address: P1.0–P1.7 = A0–A7
P2.0–P2.3 = A8–A11
Data: Port 0 = D0–D7

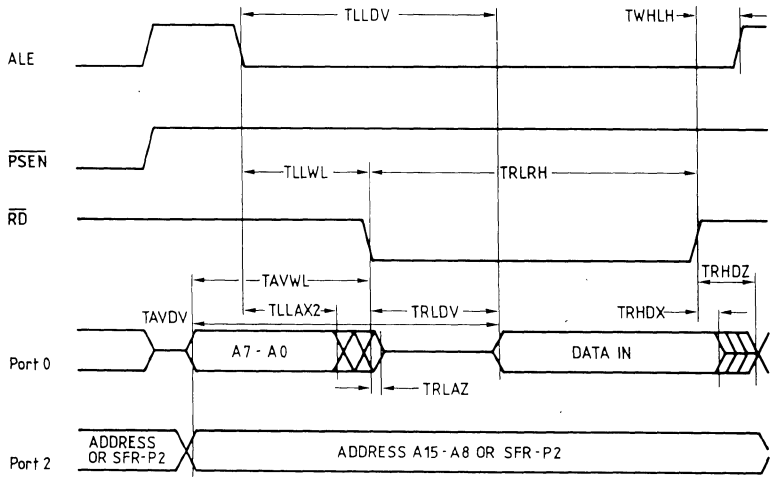
Inputs: P2.4–P2.6, $\overline{\text{PSEN}}$ = VSS
ALE, $\overline{\text{EA}}$ = TTL high level
RST/VPD = VIH1

Waveforms

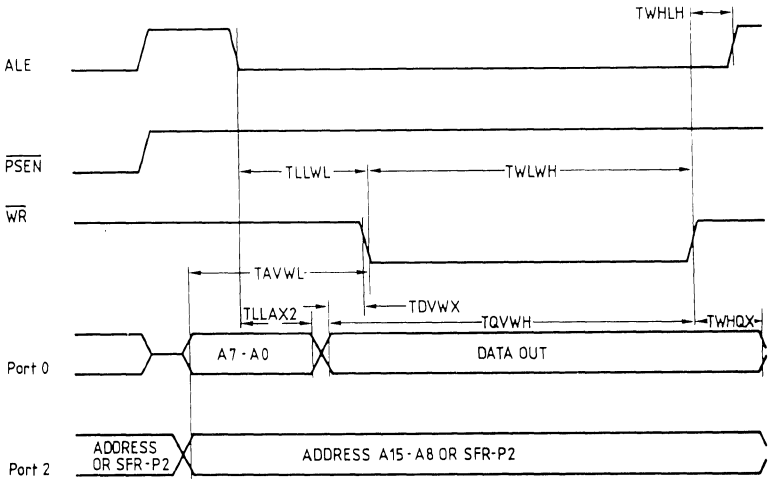
Program Memory Read Cycle



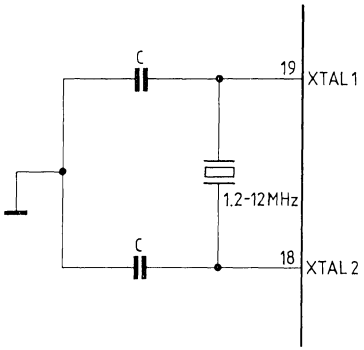
Data Memory Read Cycle



Data Memory Write Cycle

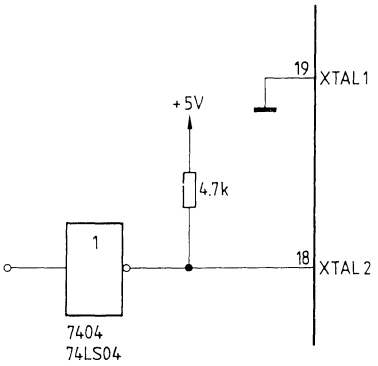


Recommended Oscillator Circuits



C = 30 pF ± 10 pF

Crystal Oscillator Mode



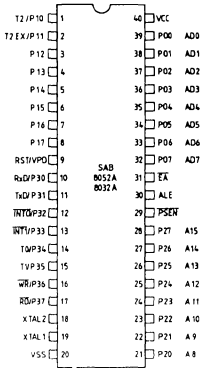
Driving from External Source

SAB 8032A/8052A
8-Bit Single Chip Microcomputer

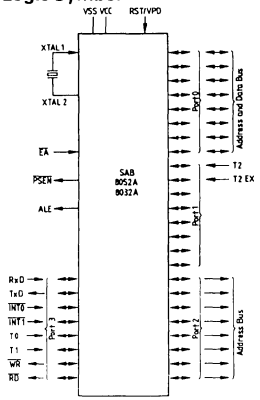
SAB 8032A Control-oriented CPU with RAM and I/O
SAB 8052A A SAB 8032A with factory mask-programmable ROM

- 8K × 8 ROM (SAB 8052A only)
- 256 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Three 16-bit timer/event counters
- High-performance full-duplex serial channel
- External memory expandable to 128 Kbytes
- Compatible with SAB 8080/8085 peripherals
- Timer 2 capture capability
- Variable transmit/receive baud rate capability
- Boolean processor
- Most instructions execute in 1 µs
- 4 µs multiply and divide
- Upward compatible with SAB 8031A/8051A

Pin Configuration



Logic Symbol



The SAB 8032A/8052A is a stand-alone, high-performance single-chip microcomputer fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology, packaged in a 40-pin DIP. It is upward compatible with the SAB 8031A/8051A. It provides the hardware features, architectural enhancements, and instructions that are necessary to make it a powerful and cost effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data memory.

The SAB 8052A contains a non-volatile 8 K × 8 read-only program memory; a volatile 256 × 8 read/write data memory; 32 I/O lines; three 16-bit timer/counters; a six-source, two-priority-level, nested interrupt structure; a serial I/O port for either multiprocessor communications, I/O expansion, or full duplex UART; as well as on-chip oscillator and clock circuits. The SAB 8032A is identical, except that it lacks the program memory.

For systems that require extra capability, the SAB 8052A can be expanded using standard TTL compatible memories and the byte oriented SAB 8080 and SAB 8085 peripherals.

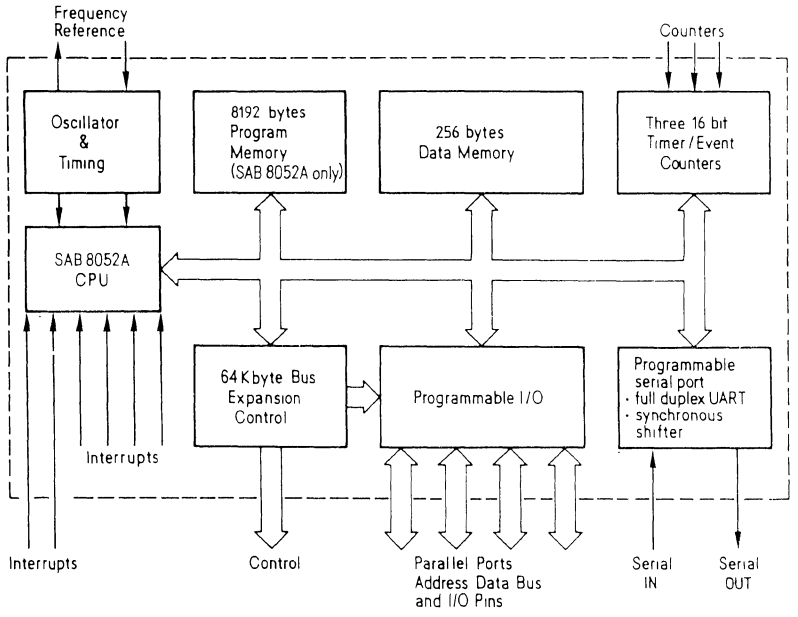
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
P1.0–P1.7	1–8	I/O	Port 1 is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads. Pins P1.0 and P1.1 also correspond to the special functions T2, external input to Timer 2, and T2EX, Timer 2 trigger input. The output latch on these two special function pins must be programmed to a one (1) for that function to operate.
RST/VPD	9	I	A high level on this pin resets the SAB 8052A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to VCC. If VPD is held within its spec while VCC drops below spec, VPD will provide standby power to the RAM. When VPD is low, the RAM's current is drawn from VCC.
P3.0–P3.7	10–17	I/O	Port 3 is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of Port 3, as follows: – RXD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). – TXD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). – $\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. – $\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. – T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. – $\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. – $\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL1 XTAL2	19 18	I	XTAL 1 input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to VSS when external source is used on XTAL 2. XTAL 2 output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0–P2.7	21–28	I/O	Port 2 is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
$\overline{PSEN}$	29	O	The program store enable output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
ALE	30	O	Provides address latch enable output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	31	I	When held at a TTL high level, the SAB 8052A executes instructions from the internal ROM when the PC is less than 8192. When held at a TTL low level, the SAB 8052A fetches all instructions from external program memory. For the SAB 8032A this pin must be tied low.
P0.0–P0.7	39–32	I/O	Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
VCC	40		+5V power supply during operation and program verification.
VSS	20		Circuit ground potential.

Block Diagram



Instruction Set Description

Mnemonic		Description	Byte	Cycle
Arithmetic operations				
ADD	A, Rn	Add register to Accumulator	1	1
ADD	A, direct	Add direct byte to Accumulator	2	1
ADD	A, @Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry flag	1	1
ADDC	A,direct	Add direct byte to Accu with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to Accu with Carry flag	1	1
ADDC	A,#data	Add immediate data to Accu with Carry flag	2	1
SUBB	A,Rn	Subtract register from Accu with borrow	1	1
SUBB	A,direct	Subtract direct byte from Accu with borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with borrow	1	1
SUBB	A,#data	Subtract immediate data from A with borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Increment indirect RAM	1	1
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
INC	DPTR	Increment data pointer	1	2
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A & B	1	4
DA	A	Decimal adjust Accumulator	1	1
Logical operations				
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL	A,#data	Exclusive-OR immediate data to Accumulator	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator left	1	1
RLC	A	Rotate A left through the Carry flag	1	1
RR	A	Rotate Accumulator right	1	1
RRC	A	Rotate A right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1

Data transfer

MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct *	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2

*Note: MOV A, ACC is not a valid instruction

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load data pointer with a 16-bit constant	3	2
Data transfer (cont.)				
MOVC	A,@A+DPTR	Move code byte relative to DPTR to Accumulator	1	2
MOVC	A,@A+PC	Move code byte relative to PC to Accumulator	1	2
MOVX	A,@Ri	Move external RAM (8-bit addr) to Accumulator	1	2
MOVX	A,@DPTR	Move external RAM (16-bit addr) to Accumulator	1	2
MOVX	@Ri,A	Move A to external RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to external RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte from stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with Accumulator	1	1
XCHD	A,@Ri	Exchange low-order digit ind. RAM with Accu	1	1
Boolean variable manipulation				
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

Instruction Set Description (continued)

Mnemonic		Description	Byte	Cycle
Program and machine control				
ACALL	addr 11	Absolute subroutine call	2	2
LCALL	addr 16	Long subroutine call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute jump	2	2
LJMP	addr 16	Long jump	3	2
SJMP	rel	Short jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is zero	2	2
JNZ	rel	Jump if Accumulator is not zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if Carry flag is not set	2	2
JB	bit,rel	Jump if direct bit set	3	2
JNB	bit,rel	Jump if direct bit not set	3	2
JBC	bit,rel	Jump if direct bit is set and clear bit	3	2
CJNE	A,direct,rel	Compare direct to Accu and jump if not equal	3	2
CJNE	A,#data,rel	Comp. immed. to Accu and jump if not equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg. and jump if not equal	3	2
CJNE	@Ri,#data,rel	Comp.immed. to ind. and jump if not equal	3	2
DJNZ	Rn,rel	Decrement register and jump if not zero	2	2
DJNZ	direct,rel	Decrement direct and jump if not zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn – Working register R0–R7
direct – 128 internal RAM locations, any I/O port, control or status register
@Ri – Indirect internal RAM location addressed by register R0 or R1
#data – 8-bit constant included in instruction
#data 16 – 16-bit constant included as bytes 2 & 3 of instruction
bit – 128 software flags, any I/O pin, control or status bit
A – Accumulator

Notes on program addressing modes:

addr 16 – Destination address for LCALL & LJMP may be anywhere within the 64-Kbyte program memory address space.
addr 11 – Destination address for ACALL & AJMP will be within the same 2-Kbyte page of program memory as the first byte of the following instruction.
rel – SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/–128 bytes relative to first byte of the following instruction.

Instruction Opcodes in Hexadecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	*code addr*
02	3	LJMP	*code addr*
03	1	RR	A
04	1	INC	A
05	2	INC	*data addr*
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	*bit addr code addr*
11	2	ACALL	*code addr*
12	3	LCALL	*code addr*
13	1	RRC	A
14	1	DEC	A
15	2	DEC	*data addr*
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	*bit addr code addr*
21	2	AJMP	*code addr*
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,*data addr*
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	*bit addr, code addr*
31	2	ACALL	*code addr*
32	1	RETI	
33	1	RLC	A

Hex Code	Number of Bytes	Mnemonic	Operands
34	2	ADDC	A,#*data*
35	2	ADDC	A,*data addr*
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R7
3F	1	ADDC	A,R7
40	2	JC	*code addr*
41	2	AJMP	*code addr*
42	2	ORL	*data addr*,A
43	3	ORL	*data addr*,#*data*
44	2	ORL	A,#*data*
45	2	ORL	A,*data addr*
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	*code addr*
51	2	ACALL	*code addr*
52	2	ANL	*data addr*,A
53	3	ANL	*data addr*,#*data*
54	2	ANL	A,#*data*
55	2	ANL	A,*data addr*
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	*code addr*
61	2	AJMP	*code addr*
62	2	XRL	*data addr*,A
63	3	XRL	*data addr*,#*data*
64	2	XRL	A,#*data*
65	2	XRL	A,*data addr*
66	1	XRL	A,@R0
67	1	XRL	A,@R1

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonic	Operands
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	*code addr*
71	2	ACALL	*code addr*
72	2	ORL	C,*bit addr*
73	1	JMP	@A+DPTR
74	2	MOV	A,#*data*
75	3	MOV	*data addr*,#*data*
76	2	MOV	@R0,#*data*
77	2	MOV	@R1,#*data*
78	2	MOV	R0,#*data*
79	2	MOV	R1,#*data*
7A	2	MOV	R2,#*data*
7B	2	MOV	R3,#*data*
7C	2	MOV	R4,#*data*
7D	2	MOV	R5,#*data*
7E	2	MOV	R6,#*data*
7F	2	MOV	R7,#*data*
80	2	SJMP	*code addr*
81	2	AJMP	*code addr*
82	2	ANL	C,*bit addr*
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	*data addr*,*data addr*
86	2	MOV	*data addr*,@R0
87	2	MOV	*data addr*,@R1
88	2	MOV	*data addr*,R0
89	2	MOV	*data addr*,R1
8A	2	MOV	*data addr*, R2
8B	2	MOV	*data addr*, R3
8C	2	MOV	*data addr*,R4
8D	2	MOV	*data addr*,R5
8E	2	MOV	*data addr*,R6
8F	2	MOV	*data addr*,R7
90	3	MOV	DPTR,#*data*
91	2	ACALL	*code addr*
92	2	MOV	*bit addr*,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#*data*
95	2	SUBB	A,*data addr*
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/*bit addr*
A1	2	AJMP	*code addr*
A2	2	MOV	C,*bit addr*
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,*data addr*
A7	2	MOV	@R1,*data addr*
A8	2	MOV	R0,*data addr*
A9	2	MOV	R1,*data addr*
AA	2	MOV	R2,*data addr*
AB	2	MOV	R3,*data addr*
AC	2	MOV	R4,*data addr*
AD	2	MOV	R5,*data addr*
AE	2	MOV	R6,*data addr*
AF	2	MOV	R7,*data addr*
B0	2	ANL	C,/*bit addr*
B1	2	ACALL	*code addr*
B2	2	CPL	*bit addr*
B3	1	CPL	C
B4	3	CJNE	A,#*data*,*code addr*
B5	3	CJNE	A,*data addr*,*code addr*
B6	3	CJNE	@R0,#*data*,*code addr*
B7	3	CJNE	@R1,#*data*,*code addr*
B8	3	CJNE	R0,#*data*,*code addr*
B9	3	CJNE	R1,#*data*,*code addr*
BA	3	CJNE	R2,#*data*,*code addr*
BB	3	CJNE	R3,#*data*,*code addr*
BC	3	CJNE	R4,#*data*,*code addr*
BD	3	CJNE	R5,#*data*,*code addr*
BE	3	CJNE	R6,#*data*,*code addr*
BF	3	CJNE	R7,#*data*,*code addr*
C0	2	PUSH	*data addr*
C1	2	AJMP	*code addr*
C2	2	CLR	*bit addr*
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,*data addr*
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7

Instruction Opcodes in Hexadecimal Order (continued)

Hex Code	Number of Bytes	Mnemonic	Operands
D0	2	POP	*data addr*
D1	2	ACALL	*code addr*
D2	2	SETB	*bit addr*
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	*data addr,code addr*
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,*code addr*
D9	2	DJNZ	R1,*code addr*
DA	2	DJNZ	R2,*code addr*
DB	2	DJNZ	R3,*code addr*
DC	2	DJNZ	R4,*code addr*
DD	2	DJNZ	R5,*code addr*
DE	2	DJNZ	R6,*code addr*
DF	2	DJNZ	R7,*code addr*
E0	1	MOVX	A,@DPTR
E1	2	AJMP	*code addr*
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,*data addr* *
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	*code addr*
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	*data addr,A*
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

*Note: MOV A, ACC is not a valid instruction

Absolute Maximum Ratings[1)]

Ambient Temperature under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground (VSS)	−0.5 to + 7 V
Power Dissipation	2 W

D.C. Characteristics

TA = 0 to 70°C; VCC = 5 V ± 10%; VSS = 0 V

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
VIL	Input Low Voltage	−0.5	0.8	V	–
VIH	Input High Voltage (Except RST/VPD and XTAL2)	2.0	VCC+0.5		
VIH1	Input High Voltage to RST/VPD for Reset, XTAL2	2.5			XTAL1 to VSS
VPD	Power Down Voltage to RST/VPD	4.5	5.5		VCC = 0V
VOL	Output Low Voltage Ports 1, 2, 3	–	0.45		IOL = 1.6 mA
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$				IOL = 3.2 mA
VOH	Output High Voltage Ports 1, 2, 3	2.4	–		IOH = −80 µA
VOH1	Output High Voltage Port 0, ALE, $\overline{PSEN}$				IOH = −400 µA
IIL	Logical 0 Input Current Ports 1, 2, 3	–	−800	µA	VIL = 0.45 V
IIL2	Logical 0 Input Current XTAL 2		−2.0	mA	XTAL1 = VSS VIL = 0.45 V
IIH1	Input High Current to RST/VPD for Reset		500	µA	VIN = VCC−1.5 V
ILI	Input Leakage Current to Port 0, $\overline{EA}$		±10		0V < VIN < VCC
ICC	Power Supply Current		175	mA	All outputs disconnected
IPD	Power Down Current		15		VCC = 0V
CIO	Capacitance of I/O Buffer		10	pF	f_c = 1 MHz

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

TA = 0°C to 70°C; VCC = 5 V ±10%; VSS = 0 V
(CL for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; CL for All Other Outputs = 80 pF)

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Min	Max	
TLHLL	ALE Pulse Width	127		2TCLCL-40		
TAVLL	Address Setup to ALE	53	–	TCLCL-30	–	
TLLAX1	Address Hold after ALE	48		TCLCL-35		
TLLIV	ALE to Valid Instr In	–	233	–	4TCLCL-100	
TLLPL	ALE to $\overline{PSEN}$	58		TCLCL-25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	215	–	3TCLCL-35	–	
TPLIV	$\overline{PSEN}$ to Valid Instr In	–	150	–	3TCLCL-100	
TPXIX	Input Instr Hold after $\overline{PSEN}$	0	–	0	–	
TPXIZ*)	Input Instr Float after $\overline{PSEN}$	–	63	–	TCLCL-20	
TPXAV*)	Address Valid after $\overline{PSEN}$	75	–	TCLCL-8	–	
TAVIV	Address to Valid Instr In	–	302	–	5TCLCL-115	
TAZPL	Address Float to $\overline{PSEN}$	0	–	0	–	

External Data Memory Characteristics

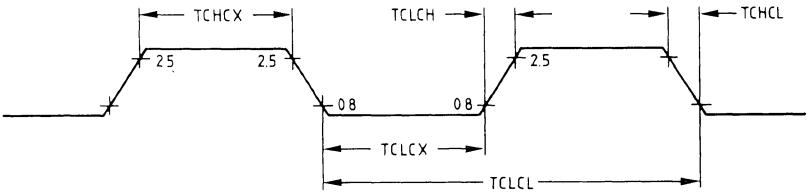
Symbol	Parameter	Limit Values				Unit
		12 MHz Clock		Variable Clock 1/TCLCL = 1.2 MHz to 12 MHz		
		Min	Max	Min	Max	
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL-100		
TWLWH	$\overline{WR}$ Pulse Width		–		–	
TLLAX2	Address Hold after ALE	132		2TCLCL-35		
TRLDV	$\overline{RD}$ to Valid Data In	–	250	–	5TCLCL-165	
TRHDX	Data Hold after $\overline{RD}$	0	–	0	–	
TRHDZ	Data Float after $\overline{RD}$		97		2TCLCL-70	
TLLDV	ALE to Valid Data In	–	517	–	8TCLCL-150	ns
TAVDV	Address to Valid Data In		585		9TCLCL-165	
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	3TCLCL-50	3TCLCL+50	
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	203	–	4TCLCL-130	–	
TWHLH	$\overline{WR}$ or $\overline{RD}$ High to ALE High	43	123	TCLCL-40	TCLCL+40	
TDVWX	Data Valid to $\overline{WR}$ Transition	33		TCLCL-50		
TQVWH	Data Setup before $\overline{WR}$	433	–	7TCLCL-150	–	
TWHQX	Data Hold after $\overline{WR}$	33		TCLCL-50		
TRLAZ	Address Float after $\overline{RD}$	–	0	–	0	

*) Interfacing the SAB 8052A to devices with float times up to 75ns is permissible. This limited bus contention will not cause any damage to Port 0 drivers.

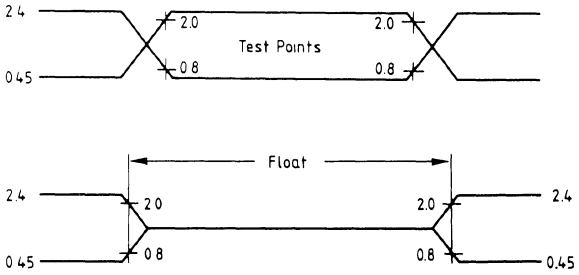
External Clock Drive XTAL2

Symbol	Parameter	Limit Values		Unit
		Variable Clock Freq = 1.2 MHz to 12 MHz		
		Min	Max	
TCLCL	Oscillator Period	83.3	833.3	ns
TCHCX	High Time	20	TCLCL-TCLCX	ns
TCLCX	Low Time	20	TCLCL-TCHCX	ns
TCLCH	Rise Time	–	20	ns
TCHCL	Fall Time	–	20	ns

External Clock Cycle



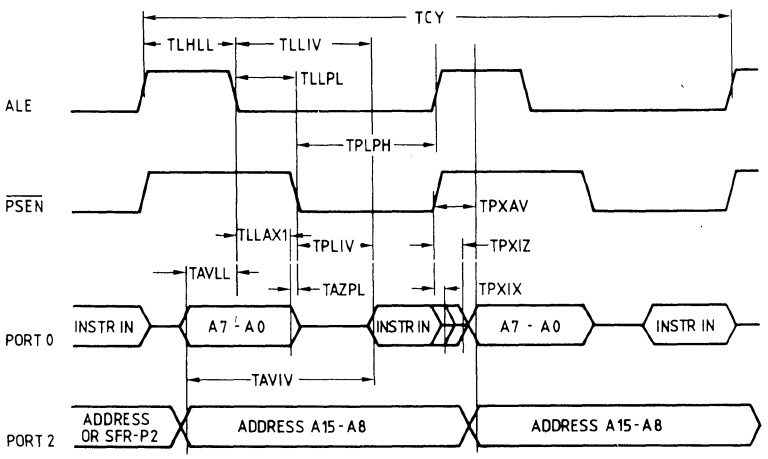
A.C. Testing Input, Output, Float Waveforms



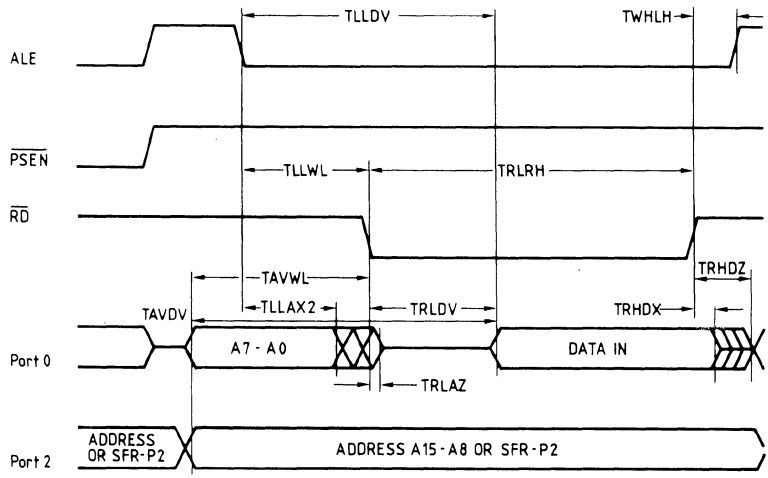
A.C. testing inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2mA or sources 400 µA at the voltage test levels.

Waveforms

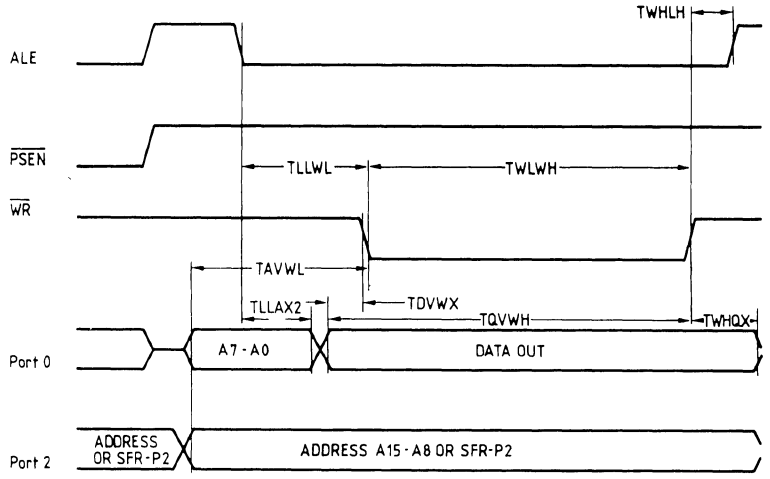
Program Memory Read Cycle



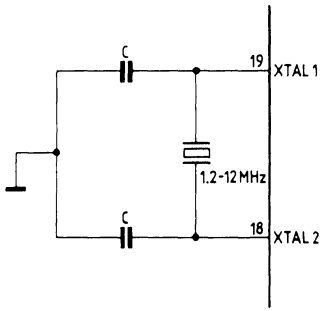
Data Memory Read Cycle



Data Memory Write Cycle

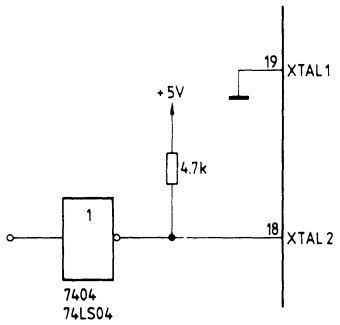


Recommended Oscillator Circuits



C = 30 pF ± 10 pF

Crystal Oscillator Mode



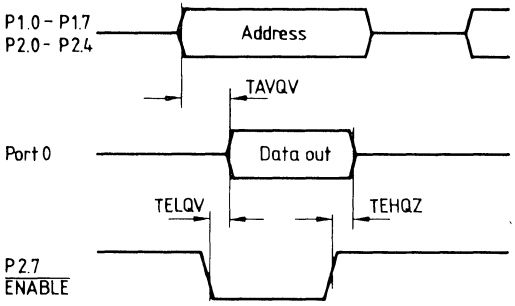
Driving from External Source

ROM Verification Characteristics

TA = 25°C ± 5°C; VCC = 5 V ± 10%; VSS = 0 V

Symbol	Parameter	Limit Values		Unit
		Min	Max	
TAVQV	Address to Valid Data	–	48 TCLCL	ns
TELQV	$\overline{\text{Enable}}$ to Valid Data			
TEHQZ	Data Float after $\overline{\text{Enable}}$	0		
1/TCLCL	Oscillator Frequency	4	6	MHz

ROM Verification



Address: P1.0–P1.7 = A0–A7
P2.0–P2.4 = A8–A12

Data: Port 0 = D0–D7

Inputs: P2.5–P2.6, $\overline{\text{PSEN}}$ = VSS
ALE, $\overline{\text{EA}}$ = TTL high level
RST/VPD = VIH1

SAB 80C482 (SM 850)
8-Bit Single Chip Microcomputer

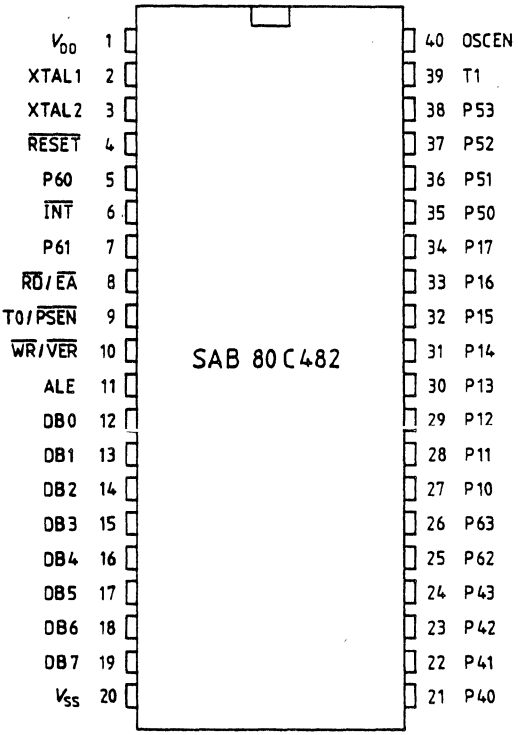
Preliminary data **CMOS circuit**

The SAB 80C482 is a low-power, advanced CMOS member of the popular SAB 8048 family. The SAB 80C482 contains double-sized program memory and 4 additional I/O lines. For systems that require extra capability, the SAB 80C482 can easily be expanded using CMOS external memories. The on-chip mask-programmable keyboard wake-up offers a convenient solution for a power-saving keyboard scanner. The SAB 80C482 has the same cycle time at about half the SAB 8048 clock frequency. The 100% static operation provides the possibility to optimize between power consumption and program speed.

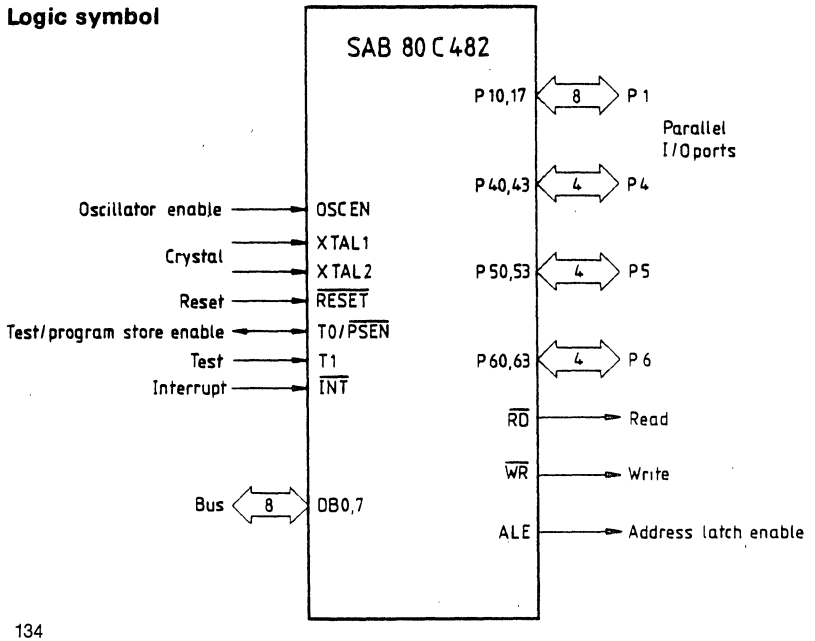
The CMOS design of the SAB 80C482 opens new application areas that require battery operation, low power standby, wide voltage range, and the ability to maintain operation during AC power line interruptions. These applications include telecommunications, automotive, consumer, portable, and hand-held instruments.

- 2K × 8 ROM
- 64 × 8 RAM
- 31 I/O lines
- 2.66 µs cycle time (with 3 MHz crystal)
- Automatic power-on reset
- Keyboard wake-up
- Very low power consumption
- Normal: 1.2 mA@5 V@8 µs cycle
- Halt 0.4 mA@5 V@8 µs cycle
- Standby: 2 µA@5 V
- 100% static operation
- Supply voltage: 2.5 to 6 V

Pin configuration
(top view)



Logic symbol

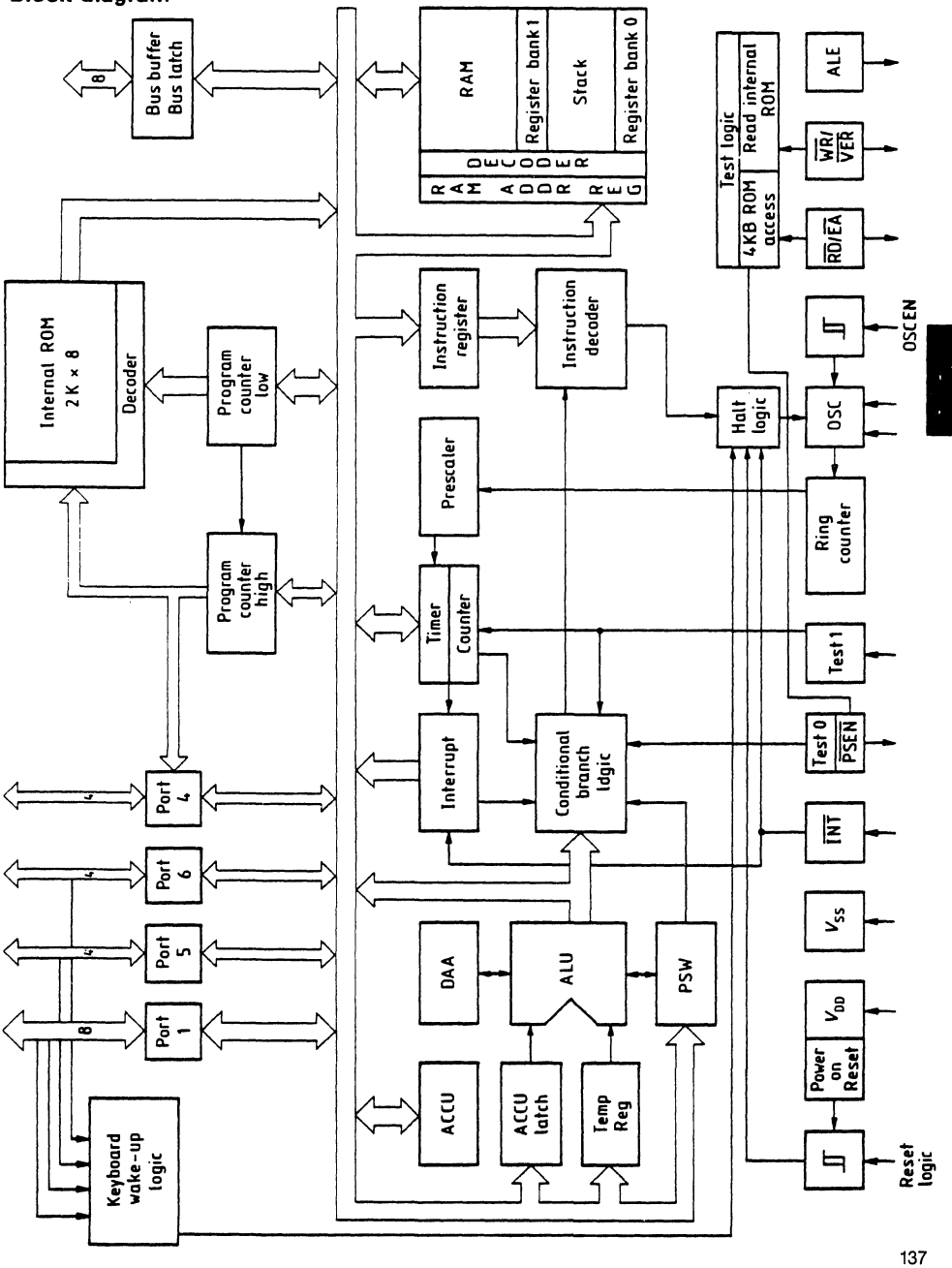


Pin description

Pin No.	Symbol	Description
2	XTAL1	Oscillator input; one side of crystal input
3	XTAL2	Oscillator output; other side of crystal input
40	OSCEN	Oscillator enable input (Schmitt-Trigger input) A high signal enables oscillator to run A low signal stops oscillator and initializes standby mode
4	$\overline{\text{RESET}}$	Input used to initialize processor (active low).
6	$\overline{\text{INT}}$	Interrupt input with internal pull-up resistor. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after reset. HALT mode is terminated by interrupt (active low).
8	$\overline{\text{RD}}/\overline{\text{EA}}$	Output strobe activated during a bus read. Can be used to enable transfer of data on the bus from an external device. Used as a read strobe to external data memory (active low). External access input which forces all program memory fetches to reference external memory. Active only during the initialization time (RESET at low)! (active low).
9	T0/$\overline{\text{PSEN}}$	Input pin testable using the instructions JT0 and JNT0 until disabled through an execution of instructions SEL MB0 or SEL MB1. Program store enable. This output is enabled through the first execution of instructions SEL MB0 or SEL MB1. It can be disabled only through a new RESET initialization. It occurs only during a fetch to external program memory (active low).
10	$\overline{\text{WR}}/\overline{\text{VER}}$	Output strobe during a bus write. Used as write strobe to external data memory (active low). ROM verification input is low during the initialization time (RESET at low). The contents of the internal ROM can be read without program execution.

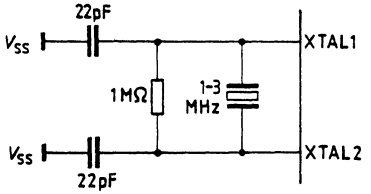
Pin No.	Symbol	Description
11	ALE	Address latch enable. This signal occurs once during each cycle and is useful as clock output. Negative edge of ALE strobes address into external data and program memory.
12...19	DB0...DB7	True bidirectional port which can be written or read synchronously using WR, RD strobes. Contains the 8 low-order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR.
21...24	P40...P43	4-bit quasi-bidirectional port. Internal pull-up resistors. This port contains the four high order program-counter bits during an external program memory fetch.
5, 7,	P60..P63	4-bit quasi-bidirectional port. Internal pull-up resistors.
25, 26		Keyboard wake-up capability mask-programmable.
27...34	P10...P17	8-bit quasi-bidirectional port. Internal pull-up resistors. Keyboard wake-up capability mask-programmable.
35...38	P50...P53	4-bit quasi-bidirectional port. Internal pull-up resistors. Keyboard wake-up capability mask-programmable.
39	T1	Input pin testable using JT1, and JNT1 instructions. Can be designated as timer/counter input using the STRT CNT instruction.
1	VDD	Power supply
20	VSS	Circuit GND potential (0 V)

Block diagram

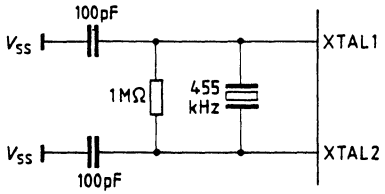


Oscillator

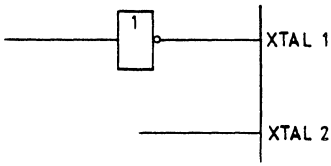
The on-board oscillator is a high-gain resonant circuit with a frequency range between 0 and 3 MHz. The clock frequency is determined by the resonator (e.g. crystal) connected between the pins XTAL1 and XTAL2.



a)



b)



c)

8-bit timer/counter

The SAB 80C842 contains a timer/counter to aid the user in counting and generating accurate time delays without placing a burden on the processor for these functions.

Timer

Execution of a START T instruction connects an internal clock to the counter input. The XTAL frequency divided by 256 is the timer input frequency.

Counter

Execution of a START CNT instruction connects the T1 pin to the counter input and enables the counter. Subsequent high-to-low transition on T1 pin must be held low for at least one machine cycle to ensure it is not missed. The counter may be incremented only once throughout three instruction cycles. There is no minimum frequency limit.

Program memory

The resident program memory consists of 2048 bytes. There are three particulary important locations in program memory:

1. **Location 0:**
   Executing the initialization reset causes the first instruction to be fetched from location 0.
2. **Location 3:**
   Execution starts at location 3 after the interrupt input (pin 6) of the processor has gone low (if interrupt is enabled).
3. **Location 7:**
   A timer/counter interrupt resulting from timer/counter overflow (if enabled).

Program memory configurations

1. **Internal 2 Kbyte ROM**
   - pin 9 is available as T0 input
   - port 4 serves only as I/O port
2. **Internal 2 Kbyte ROM and additional, external 2 Kbyte ROM**
   - with external access, instruction words are read in via bus (data bus, DB).
   - an SEL MB0 or an SEL MB1 instruction must be executed before using the data bus for external program store access.
   - execution of SEL MB1 instruction followed by CALL or JMP enables exceeding internal 2 Kbyte limits and accessing of external ROM.
   - external program memory access causes loading of program counter bits PC8 through PC11 at port lines 40 to 43. PC0 through PC7 appear on bus during the falling edge of ALE.
   - execution of MOVP3 A,@A instruction causes internal ROM (bank 0) to be selected.
   - internal ROM is automatically selected during every execution of an interrupt service routine.
   - in second cycle of MOVX instruction no $\overline{\text{PSEN}}$ signal appears and $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal is active. Port 4 is not affected.
3. **External 4 Kbyte ROM, internal ROM disabled**
   - sole access to external 4 Kbyte ROM is initiated by logic 0 at pin 8 ($\overline{\text{RD}}/\overline{\text{EA}}$) during initialization time (RESET at low). At the machine cycle T8 test logic calls up status from pin 8.
   - pin 9 serves as $\overline{\text{PSEN}}$ output.
   - program counter bits PC0 through PC7 appear at DB0 through DB7 and PC8 through PC11 appear at port lines P40 through P43.
   - execution of MOVP3 A,@A instruction or interrupt routine selects automatically lower 2 Kbytes of external ROM.

4. Internal ROM verification without program execution

- pin 10 ($\overline{WR}/\overline{VER}$) is tested at the machine cycle T8 during the initialization time (RESET at low). The low level at this pin forces the SAB 80C482 to the verification mode.
- contents of internal ROM appear on lines DB0 through DB7
- program-counter bits PC0 through PC7 appear at DB0 through DB7 and PC8 through PC11 at port lines P40 through P43.
- ALE and $\overline{PSEN}$ are enabled.

Reset

The reset signal sets the microcomputer to a defined initial state. There are two possibilities to reach this state.

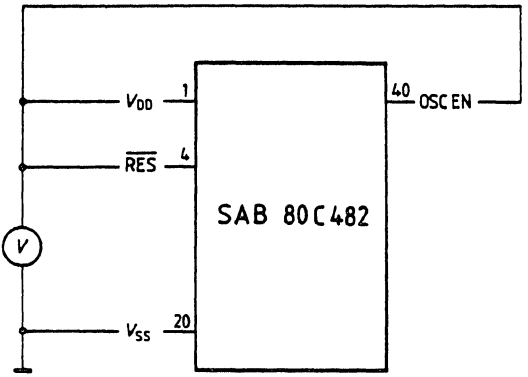
1. by an external signal at pin 4 (RESET)
2. by an internal signal generated through the built-in power-on-reset circuit.

If the oscillator is enabled (OSCEN at high), reset performs the following functions:

1. sets program counter to zero (PC = 000H)
2. sets stack pointer to zero (SP = 00H)
3. selects register bank 0
4. selects memory bank 0 (internal ROM)
5. sets bus to high impedance state
   (except when $\overline{RD}/\overline{EA}$ or $\overline{WR}/\overline{VER}$ is at low)
6. sets ports 1, 4, 5, 6 to input mode
7. stops counter/timer
8. enables pin 9 as test input T0
9. disables interrupts
10. clears timer flag
11. releases HALT mode
12. does not affect internal RAM contents

Timing diagrams for power-on and external reset are shown in fig. a) and b).

Figure a) Internal power-on reset



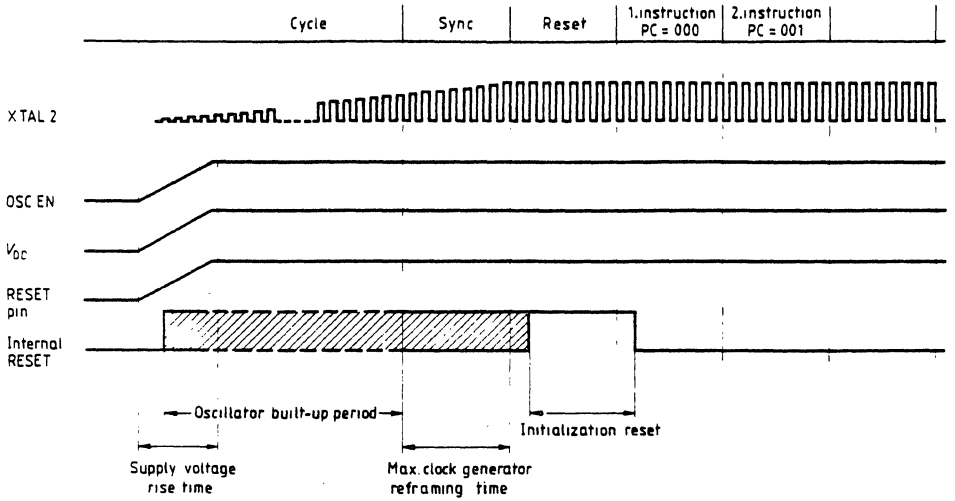
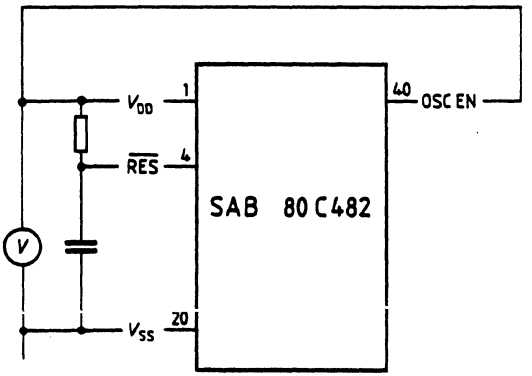
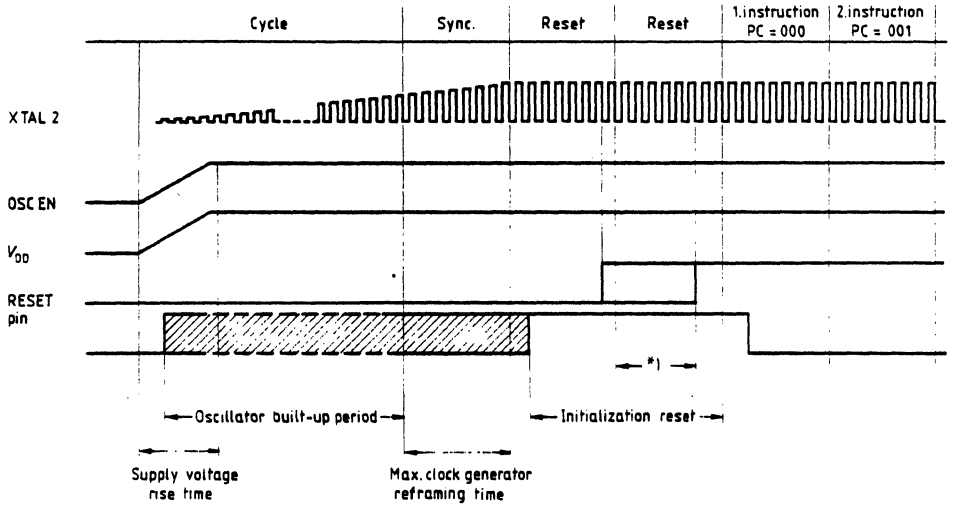


Figure b) External reset





*) During this time-slot the signal at Reset-pin can change to V_{DD} without lengthening the Reset execution

Interrupt

The SAB 80C482 has the same interrupt logic as the SAB 8048. The interrupt can be initialized through two possible sources:

1. external low active signal at pin $\overline{INT}$
2. overflow of the internal counter/timer.

Keyboard wake-up

The SAB 80C482 has a special on-chip circuitry for a convenient keyboard-scanning named "Keyboard wake-up". Four NAND gates can be connected to the ports P10–13, P14–17, P50–53 and P60–63 by mask programming. The outputs of these gates are interconnected in the NOR manner. The resulting output controls the release from the HALT mode.

This means, the SAB 80C482 can be "waked up" on any keystroke without the necessity of using a double contact keyboard.

HALT mode

After execution of the HALT instruction the processor enters the HALT mode where the internal clocks and internal logic are disabled. The oscillator is running. In the HALT mode, power consumption is about 1/3 of normal SAB 80C482 operation.

HALT mode can be released in three different ways:

1. by low pulse on the $\overline{RESET}$ pin
   (program starts at address location 0)
2. via keyboard wake-up
   (program continues at address location PC+1)
3. by low pulse on the $\overline{INT}$ pin
   (if interrupt is enabled the interrupt subroutine starting at the address location 3 is executed. After its execution, or if interrupt is disabled, program continues at address location PC+1.)

Standby

Standby provides additional, drastic power consumption savings over the HALT mode.

Standby is initiated by forcing the OSCEN pin to low state. Oscillator operation is discontinued. While in standby, the following data is maintained:

1. internal RAM
2. stack pointer
3. program counter
4. memory bank status
5. TO/$\overline{\text{PSEN}}$ status
6. I/O status on all ports
7. all internal logic states

It is possible, but not recommended, to put the SAB 80C482 on standby without regard to the running program. Stopping at any time in the instruction cycle can result in an undefined status. Consequently, it is advisable to enter standby only from the HALT state or if an external reset signal is applied. The $\overline{\text{RES}}$ pin must be forced at least 2.5 cycles earlier to the low level than the OSCEN pin.

If the SAB 80C482 has entered the standby from the HALT mode, it is still in the HALT mode after the OSCEN pin has been forced high. In the second case, the $\overline{\text{RES}}$ pin has to be held at least for the oscillator built-up period plus one cycle at low level after the OSCEN pin has been forced high.

Instruction set

There are five new instructions in addition to the SAB 8048 instruction set:

DEC	@ R0	instruction code	C0
DEC	@ R1	instruction code	C1
DJNZ	@ R0, addr	instruction code	E0
DJNZ	@ R1, addr	instruction code	E1
HALT		instruction code	F3

The following SAB 8048 instructions are not available:

IN	A, P2	instruction code	0A
MOVD	A, P7	instruction code	0F
OUTL	P2, A	instruction code	3A
MOVD	P7, A	instruction code	3F
ENTO	CLK	instruction code	75
JF1	addr	instruction code	76
CLR	F0	instruction code	85
ORL	P2, # data	instruction code	8A
ORLD	P7, A	instruction code	8F
CPL	F0	instruction code	95
ANL	P2, # data	instruction code	9A
ANLD	P7, A	instruction code	9F
CLR	F1	instruction code	A5
CPL	F1	instruction code	B5
JF0	addr	instruction code	B6
MOV	A, PSW	instruction code	C7
MOV	PSW, A	instruction code	D7

The opcode of the following instruction has been changed:

JNI	addr	instruction code	66 (8048 = 86)

Symbols and abbreviations

A	Accumulator
AC	Auxiliary carry
addr	Program memory address
An	Accumulator bit n
Bb	Bit designator b = 0 to 7
BS	Bank switch
BUS	Bus port
CY	Carry
CLK	Clock
CNT	Event counter
data	8-Bit number or expression
DBF	Memory bank flipflop
I	Interrupt
PC	Program counter
Pp	Port designator p = 4 to 6
P1	Port 1
PSW	Program status word
Ri	Register designator i = 0, 1
Rr	Register designator r = 0 to 7
SP	Stack pointer
T	Timer
TF	Timer/counter flag
T0/T1	Test 0, test 1
X	Mnemonic for external RAM
#	Immediate data prefix
@	Indirect address prefix
(X)	Contents of X
((X))	Contents of location addressed by (X)
←	Is replaced by
↔	Is exchanged with
AND	Logical AND operation
OR	Logical OR operation
XOR	Logical EXOR operation

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Accumulator and register move instructions						
MOV A, Rr	(A) ← (Rr)	Move register to accumulator	F8–FF		1	1
MOV A, @ Ri	(A) ← ((Ri))	Move data memory to accumulator	F0–F1		1	1
MOV A, # data	(A) ← data	Move data to accumulator	23		2	2
MOV Rr, A	(Rr) ← (A)	Move accumulator to register	A8–AF		1	1
MOV @ Ri, A	((Ri)) ← (A)	Move accumulator to data memory	A0–A1		1	1
MOV Rr, # data	(Rr) ← data	Move data to register	B8–BF		2	2
MOV @ Ri, # data	((Ri)) ← data	Move data to data memory	B0–B1		2	2
MOVX A, @ Ri	(A) ← ((Ri))	Move external data to accumulator	80–81		1	2
MOVX @ Ri, A	((Ri)) ← (A)	Move accumulator to external data memory	90–91		1	2
XCH A, Rr	(A) ↔ (R)	Exchange register and accumulator	28–2F		1	1
XCH A, @ Ri	(A) ↔ ((Ri))	Exchange data memory and accumulator	20–21		1	1
XCHD A, @ RI	(A0–3) ↔ ((Ri0–3))	Exchange nibble of data memory and accumulator	30–31		1	1
MOVP3 A, @ A	save (PC) (PC0–7) ← (A) (PC8–11) ← 011 B (A) ←((PC)) restore PC	Move data from page 3 of program memory to accumulator	E3		1	2
MOVP A, @ A	save (PC) (PC0–7) ← (A) (A) ← ((PC)) restore PC	Move data from current page of program to accumulator	A3		1	2
SWAP A	(A4–7) ↔ (A0–3)	Exchange accumulator nibbles	47		1	1

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Timer/counter move instructions						
MOV A, T	(A) ← (T)	Read counter/timer into accumulator	42		1	1
MOV T, A	(T) ← (A)	Load counter/timer from accumulator	62		1	1
Port move instructions						
IN A, P1	(A) ← (P1)	Move data at port 1 to accumulator	09		1	2
OUTL P1, A	(P1) ← (A)	Output accumulator on port 1	39		1	2
ANL P1, # data	(P1) ← (P1) AND data	Logical AND port 1 with data	99		2	2
ORL P1, # data	(P1) ← (P1) OR data	Logical OR port 1 with data	89		2	2
IN A, BUS	(A) ← (BUS)	Move data on bus to accumulator	08		1	2
OUTL BUS, A	(BUS) ← A	Output accumulator on bus	02		1	2
ANL BUS, # data	(BUS) ← (BUS) AND data	Logical AND bus with data	98		2	2
ORL BUS, # data	(BUS) ← (BUS) OR data	Logical OR bus with data	88		2	2
MOVD A, Pp	(A0–3) ← (Pp) (A4–7) ← 0	Move data at port 4 – 6 to accumulator	0C–0E		1	2
MOVD Pp, A	(Pp) ← (A0–3)	Output accumulator on port 4 – 6	3C–3E		1	2
ANLD Pp, A	(Pp) ← (A0–3) AND (Pp)	Logical AND accumulator with port 4 – 6	9C–9E		1	2
ORLD Pp, A	(Pp) ← (A0–3) OR (Pp)	Logical OR accumulator with port 4 – 6	8C–8E		1	2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Arithmetic accumulator instructions						
ADD A, Rr	(A) ← (A) + (Rr)	Add register to accumulator	68–6F	AC CY	1	1
ADD A, @ Ri	(A) ← (A) + ((Ri)	Add data memory to accumulator	60–61	AC CY	1	1
ADD A, # data	(A) ← (A) + data	Add data to accumulator	03	AC CY	2	2
ADDC A, Rr	(A) ← (A) + (Rr) + (CY)	Add register and carry to accumulator	78–7F	AC CY	1	1
ADDC A, @ Ri	(A) ← (A) + ((Ri)) + (CY)	Add data memory and carry to accumulator	70–71	AD CY	1	1
ADDC A, # data	(A) ← (A) + data + (CY)	Add data and carry to accumulator	13	AC CY	2	2
INC A	(A) ← (A) + 1	Increment accumulator by 1	17		1	1
DEC A	(A) ← (A) – 1	Decrement accumulator by 1	07		1	1
DA A		Decimal adjust accumulator	57	AC CY	1	1
Arithmetic register instructions						
INC Rr	(Rr) ← (Rr) + 1	Increment register by 1	18–1F		1	1
DEC Rr	(Rr) ← (Rr) – 1	Decrement register by 1	C8–CF		1	1
DEC @ Ri	((Ri)) ← ((Ri)) + 1	Decrement data memory by 1	C0–C1		1	1
INC @ Ri	((Ri)) ← ((Ri)) + 1	Increment data memory by 1	10–11		1	1
DJNZ Rr, addr	(Rr) ← (Rr) – 1 if (Rr) ≠ 0 (PC0–7)←addr	Decrement register by 1 and jump if register not zero	E8–EF		2	2
DJNZ @ Ri, addr	((Ri)) ← ((Ri)) – 1 if ((Ri)) ≠ 0 (PC0–7)←addr	Decrement data memory by 1 and jump if data memory is not zero	E0–E1		2	2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Logical accumulator and register instructions						
ANL A, Rr	(A) ← (A) AND (Rr)	Logical AND accumulator with register	58–5F		1	1
ANL A, @ Ri	(A) ← (A) AND ((Ri))	Logical AND accumulator with data memory	50–51		1	1
ANL A, # data	(A) ← (A) AND data	Logical AND accumulator with data	53		2	2
ORL A, Rr	(A) ← (A) OR (Rr)	Logical OR accumulator with register	48–4F		1	1
ORL A, @ Ri	(A) ← (A) OR ((Ri))	Logical OR accumulator with data memory	40–41		1	1
ORL A, # data	(A) ← (A) OR data	Logical OR accumulator with data	43		2	2
XRL A, Rr	(A) ← (A) XOR (Rr)	Logical XOR accumulator with register	D8–DF		1	1
XRL A, @ Ri	(A) ← (A) XOR ((Ri))	Logical XOR accumulator with data memory	D0–D1		1	1
XRL A, # data	(A) ← (A) XOR data	Logical XOR accumulator with data	D3		2	2
CLR A	(A) ← 0	Clear accumulator	27		1	1
CPL A	(A) ← ($\overline{A}$)	Complement accumulator	37		1	1

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Rotate instructions						
RL A	(An+1) ← (An)	Shift accumulator 1 bit to left	E7		1	1
RLC A	(An+1) ← (An) (CY) ← (A7) (A0) ← (CY)	Shift accumulator 1 bit to left through carry	F7	CY	1	1
RR A	(An) ← (An+1)	Shift accumulator 1 bit to right	77		1	1
RRC A	(An) ← (An+1) (CY) ← (A0) (A7) ← (CY)	Shift accumulator 1 bit to right through carry	67	CY	1	1
Flag instructions						
CLR C	(CY) ← 0	Clear carry bit	97	CY	1	1
CPL C	(CY) ← $(\overline{CY})$	Complement carry bit	A7	CY	1	1

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Branch instructions						
JMP addr	(PC0–7) ← addr 0–7 (PC8–10) ← addr 8–10 (PC11) ← DBF	Jump to address, page 0 1 2 3 4 5 6 7	 04 24 44 64 84 A4 C4 E4		2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2
JMPP @ A	(PC0–7) ← ((A))	Jump to address defined in program memory	B3		1	2
JC addr	if (CY) = 1 (PC0–7) ← addr	Jump to address if carry = 1	F6		2	2
JNC addr	if (CY) = 0 (PC0–7) ← addr	Jump to address if carry = 0	E6		2	2
JZ addr	if (A) = 0 (PC0–7) ← addr	Jump to address if accumulator = 0	C6		2	2
JNZ addr	if (A) > 0 (PC0–7) ← addr	Jump to address if accumulator > 0	96		2	2
JT0 addr	if T0 = 1 (PC0–7) ← addr	Jump to address if T0 is High	36		2	2
JNT0 addr	if T0 = 0 (PC0–7) ← addr	Jump to address if T0 is Low	26		2	2
JT1 addr	if T1 = 1 (PC0–7) ← addr	Jump to address if T1 is High	56		2	2
JNT1 addr	if T1 = 0 (PC0–7) ← addr	Jump to address if T1 is Low	46		2	2
JTF addr	if TF = 1 (PC0–7) ← addr (TF) ← 0	Jump to address if counter/timer flag = 1	16	TF	2	2
JNI addr	if $\overline{INT}$ = 0 (PC0–7) ← addr	Jump to address if interrupt input Low	66		2	2
JBb addr	if (An) = 1 (PC0–7) ← addr	Jump to address, n=0 if bit n of 1 accumulator = 1 2 3 4 5 6 7	12 32 52 72 92 B2 D2 F2		2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Subroutine instructions						
CALL addr	((SP)) ← (PC0–11, PSW4–7) (SP) ← (SP)+1 (PC0–10) ← addr 0–10 (PC11) ← DBF	Jump to page 0 subroutine 1 2 3 4 5 6 7	14 34 54 74 94 B4 D4 F4		2 2 2 2 2 2 2 2	2 2 2 2 2 2 2 2
RET	(SP) ← (SP)–1 (PC) ← ((SP))	Return without PSW Restore	83		1	2
RETR	(SP) ← (SP)–1 (PC) ← ((SP)) (PSW4–7) ← ((SP))	Return with PSW Restore	93	CY AC DBF	1	2

Mnemonic	Function	Description	Hex code	Flag	Bytes	Cycles
Control instructions						
STRT T		Start timer	55		1	1
STRT CNT		Start counter	45		1	1
STOP TCNT		Stop timer/counter	65		1	1
EN TCNTI		Enable timer/ counter interrupt	25		1	1
DIS TCNTI		Disable timer/ counter interrupt	35		1	1
EN I		Enable external interrupt	05		1	1
DIS I		Disable external interrupt	15		1	1
SEL RB0		Select register bank 0	C5	BS	1	1
SEL RB1		Select register bank 1	D5	BS	1	1
SEL MB0		Select program-memory bank 0	E5	DBF	1	1
SEL MB1		Select program-memory bank 1	F5	DBF	1	1
NOP		No operation	00		1	1
HALT		HALT instruction	F3		1	1

Maximum ratings

Ambient temperature under bias	T_{amb}	0 to 70	°C
Storage temperature	T_{stg}	−55 to 125	°C
Supply voltage ref. to GND (V_{SS})	V_{DD}	0 to 7	V
Total power dissipation	P_{tot}	1	W
All input and output voltages		−0.3 to V_{DD}	V

DC characteristics

T_{amb} = 0 to 70°C; V_{DD} = 2.5 to 6 V; V_{SS} = 0 V

		Test conditions	Min.	Typ.	Max.	
L input voltage (all except XTAL1, XTAL2, $\overline{\text{RESET}}$)	V_{IL}		−0.1		0.75	V
L input voltage (XTAL1, XTAL2, $\overline{\text{RESET}}$)	V_{IL1} V_{IL1}	 V_{DD} < 4.5 V	−0.1		0.75 0.25	V V
H input voltage (all except XTAL1, XTAL2, $\overline{\text{RESET}}$	V_{IH}		0.7x V_{DD}		V_{DD}	V
H input voltage (XTAL1, XTAL2, $\overline{\text{RESET}}$	V_{IH1}		0.7x V_{DD}		V_{DD}	V
L output voltage (BUS, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, $\overline{\text{ALE}}$)	V_{OL}	I_{OL} = 1.0 mA			0.45	V
L output voltage (all other outputs)	V_{OL1}	I_{OL} = 1.0 mA			0.45	V
H output voltage (BUS, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PSEN}}$, $\overline{\text{ALE}}$)	V_{OH}	I_{OH} = 1.0 mA	0.75x V_{DD}			V
H output voltage; low impedance (all other outputs), high impedance	V_{OH1} V_{OH1}	I_{OH} = 1 mA I_{OH} = 1 µA	0.75x V_{DD} 0.75x V_{DD}			V V
Input leakage current (Port1, 4, 5, 6)	I_{ILP}	$V_{IN} \leq V_{IL}$			−5	µA
Input leakage current ($\overline{\text{RESET}}$, T1)	I_{ILC}	$V_{SS} \leq V_{IN} \leq V_{DD}$			±1	µA
Input leakage current ($\overline{\text{INT}}$; pullup)	I_{IL}	$V_{IN} = V_{DD}$ $V_{IN} \leq V_{IL}$			+1 −5	µA µA
Input current XTAL	I_{XT}	$V_{SS} \leq V_{IN} \leq V_{DD}$			±10	µA
Output leakage current (For bus and T0 in high-impedance states)	I_{OL}	$V_{IN} \leq V_{IL}$			±1	µA
Total supply current	I_{DD}	1 MHz; 5 V 3 MHz; 5 V 500 kHz; 5 V		1.2 4.2 0.9	1.4	mA mA mA
HALT supply current	I_{DD}	1 MHz; 5 V 3 MHz; 5 V 500 kHz; 5 V		 550 250	400	µA µA µA
Power-down mode	I_{DD}	5 V		1	2	µA
Operation supply voltage	V_{DD}		2.5		6	V

AC characteristics

T_{amb} = 0 to 70°C; V_{DD} = 5 V; V_{SS} = 0 V; f_{OSC} = 3 MHz
C_L = 40 pF

		Test conditions	Min.	Typ.	Max.	
ALE pulse width	t_{LL}		800	833		ns
Address set-up before ALE	t_{AL}		120	166		ns
Address hold from ALE	t_{LA}		0		160	ns
Control pulse width						
$\overline{PSEN}$	t_{CC}		300	333		ns
$\overline{RD}$, $\overline{WR}$	t_{CC}		1300	1333		ns
Data set-up before $\overline{WR}$	t_{DW}		1300	1333		ns
Data hold after $\overline{WR}$	t_{WD}	t_{CY} = 2.66 µs C_L = 40 pF	300	333		ns
Cycle time	t_{CY}		2.66			µs
Data hold after $\overline{RD}$	t_{DR}		0		300	ns
Instr. hold after $\overline{PSEN}$	t_{DR}		0		300	ns
$\overline{RD}$ to data in	t_{RD}				1200	ns
$\overline{PSEN}$ to data in	t_{RD}				300	ns
Address set-up before $\overline{WR}$	t_{AW}		2000			ns
Address set-up to data						
at $\overline{RD}$	t_{AD}		3500			ns
at $\overline{PSEN}$	t_{AD}		500			ns
Address float to						
$\overline{RD}$	t_{AFC}		166	333		ns
$\overline{PSEN}$	t_{AFC}		140	166		ns
$\overline{WR}$ to ALE	t_{CA}			333		ns
$\overline{PSEN}$ to ALE	t_{CA}			1333		ns
ALE to $\overline{RD}$	t_{CA}		0		50	ns
ADDRESS Time Port 4	t_{ADD}			666		ns

Time parameters versus f_{OSC}

Symbol	Parameter	
t	$1/f_{OSC}$	µs
t_{CY}	8 t	µs

Read from external data memory

t_{LL}	2.5 t	µs
t_{CA}	–	µs
t_{AFC}	1.0 t	µs
t_{CC}	4.0 t	µs
t_{DR}	–	µs
t_{RD}	3.5 t	µs
t_{AD}	10.5 t	µs

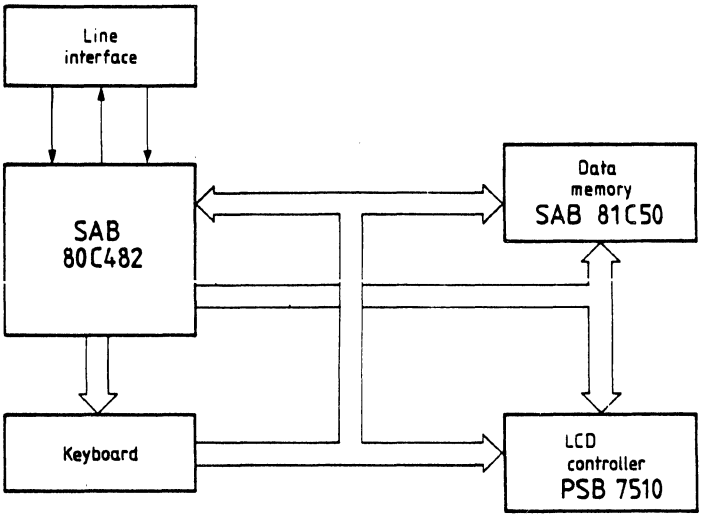
Write into external data memory

t_{CA}	1.0 t	µs
t_{CC}	4.0 t	µs
t_{WD}	1.0 t	µs
t_{DW}	4.0 t	µs
t_{AW}	6.0 t	µs

Instruction fetch from external program memory

t_{AL}	0.5 t	µs
t_{CA}	4.0 t	µs
t_{LA}	–	µs
t_{CC}	1.0 t	µs
t_{DR}	–	µs
t_{RD}	0.5 t	µs
t_{AD}	1.5 t	µs
t_{ADD}	2.0 t	µs
t_{AFC}	0.5 t	µs

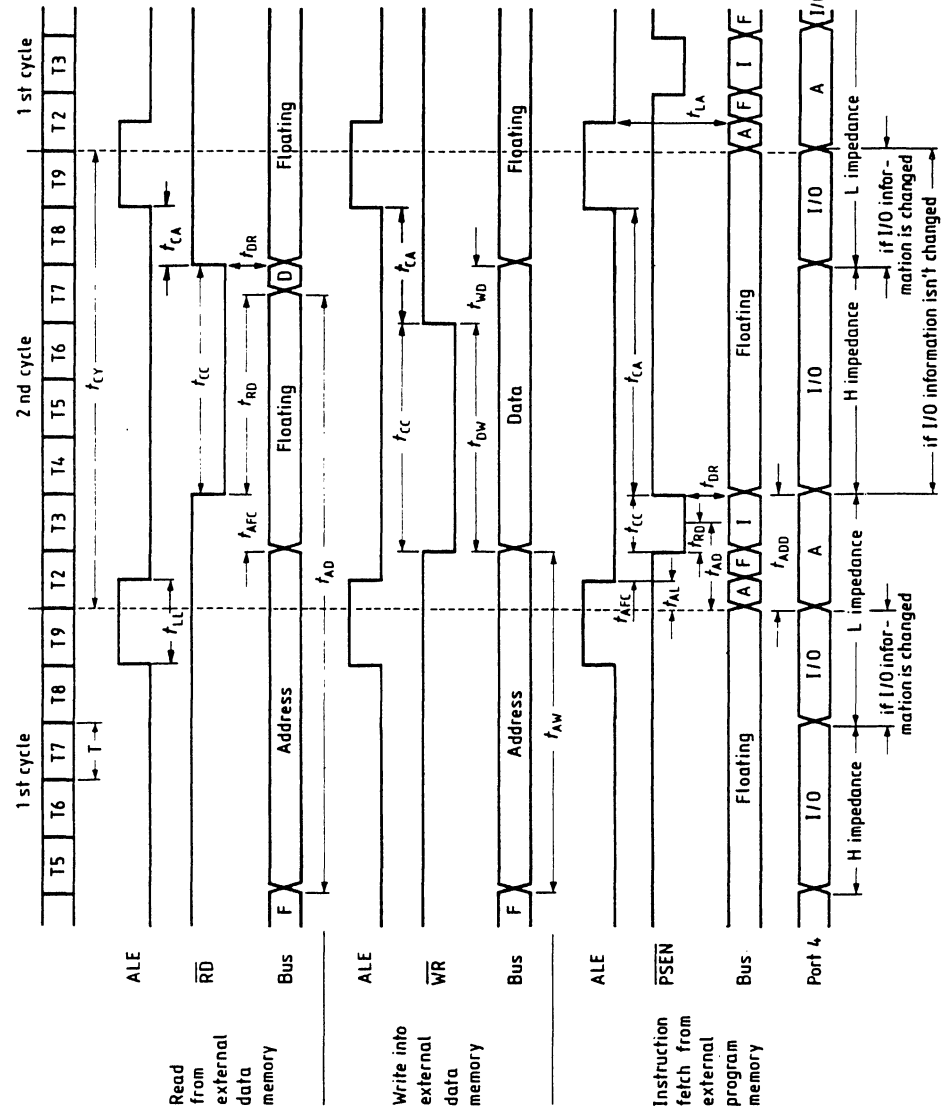
Application example "Intelligent Telephone Set"



Features of this telephone set

- direct and indirect redialing
- short dialing (10 memories)
- auto dialing by special keys
- babysitter function
- LC-display control
- electronic keylock
- clock function
- rate signaling

Pulse diagram SAB 80C482



SAB 8086
16-Bit Microprocessor

SAB 8086-2 8 MHz
SAB 8086-1 10 MHz

SAB 8086 5 MHz

- Direct Addressing Capability to 1 MByte of Memory
- Assembly Language Compatible with SAB 8080 / SAB 8085
- 14 Word, By 16-Bit Register Set with Symmetrical Operations
- 8- and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide
- Bit, Byte, Word, and Block Operations
- 24 Operand Addressing Modes
- Clock Rate upto 10 MHz (SAB 8086-1)
- Compatible with Industry Standard 8086
- In plastic and ceramic package

Figure 1. Pin Diagram

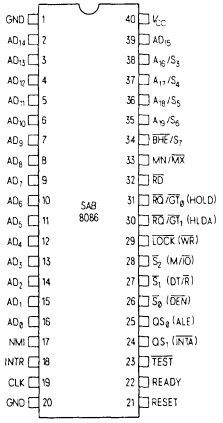


Figure 2. Pin Names

AD_{0-15}	Address/Data	A_{16-19}	Address
$\overline{S}_{0-2}$	Status	S_{3-7}	Status
INTR	Interrupt Request	$\overline{BHE}$	Bus High Enable
CLK	Clock	HOLD	Hold
QS_{0-1}	Queue Status	HLDA	Hold Acknowledge
$\overline{TEST}$	Test for Busy	$\overline{WR}$	Write
READY	Ready	DT/$\overline{R}$	Bus Driver Transmit/ Receive
RESET	Chip Reset		
MN/$\overline{MX}$	Minimum/Maximum Mode	$\overline{DEN}$	Bus Driver Enable
		ALE	Address Latch Enable
$\overline{RD}$	Read	$\overline{INTA}$	Interrupt Acknowledge
$\overline{RQ}/\overline{GT}_{0-1}$	Request/Grant	NMI	Non-maskable Interrupt
$\overline{LOCK}$	Bus Lock		
M/$\overline{IO}$	Memory/IO	GND	Ground
		V_{CC}	+5 Volts

SAB 8086 is a new generation, high performance 16-bit Microprocessor implemented in +5 Volts, depletion load, N channel, silicon gate Siemens MYMOS technology packaged in a 40 pin package. It is 100 percent compatible with the industry standard 8086. With features like string handling, 16-bit arithmetic with multiply and divide it significantly increases system performance. It is highly suited for multiprocessor applications in various configurations.

Functional Pin Definition

The following pin function descriptions are for SAB 8086 systems in either minimum or maximum mode. The "Local Bus" in these descriptions is the direct multiplexed bus interface connection to the SAB 8086 (without regard to additional bus buffers).

<table>
<tr><th>Number</th><th>Symbol</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>2–16
39</td><td>AD_0–AD_{15}</td><td>I/O</td><td>These lines constitute the time multiplexed memory I/O address (T_1) and data (T_2, T_3, T_4) bus. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7–D_0. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>35–38</td><td>A_{16}/S_3
A_{17}/S_4
A_{18}/S_5
A_{19}/S_6</td><td>O</td><td>During T_1 these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_w and T_4. The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle.
A_{17}/S_4 and A_{16}/S_3 are encoded as follows:
<table>
<tr><th>A_{17}/S_4</th><th>A_{16}/S_3</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>Alternate Data</td></tr>
<tr><td>0</td><td>1</td><td>Stack</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>Code or None</td></tr>
<tr><td>1</td><td>1</td><td>Data</td></tr>
<tr><td>S_6 is 0 (LOW)</td><td></td><td></td></tr>
</table>
This information indicates which relocation register is presently being used for data accessing.
These lines float to 3-state OFF during local bus "hold acknowledge".</td></tr>
<tr><td>34</td><td>$\overline{BHE}/S_7$</td><td>O</td><td>During T_1 the bus high enable signal ($\overline{BHE}$) should be used to enable data onto the most significant half of the data bus, pins D_{15}–D_8. Eight-bit oriented devices tied to the upper half of the bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus.
The S_7 status information is available during T_2, T_3, and T_4. The signal is active LOW, and floats to 3-state OFF in "hold". It is LOW during T_1 for the first interrupt acknowledge cycle.</td></tr>
<tr><td>32</td><td>$\overline{RD}$</td><td>O</td><td>Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the S_2 pin. This signal is used to read devices which reside on the SAB 8086 local bus. $\overline{RD}$ is active LOW during T_2, T_3 and T_w of any read cycle, and is guaranteed to remain HIGH in T_2 until the SAB 8086 local bus has floated.
This signal floats to 3-state OFF in "hold acknowledge".</td></tr>
</table>

Number	Symbol	Input (I) Output (O)	Function
22	READY	I	READY is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory I/O is synchronized by the SAB 8284A Clock Generator to form READY. This signal is active HIGH. The SAB 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.
18	INTR	I	Interrupt request is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software reseting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.
23	$\overline{\text{TEST}}$	I	The $\overline{\text{TEST}}$ input is examined by the "Wait" instruction. If the $\overline{\text{TEST}}$ input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
17	NMI	I	Non-maskable interrupt is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
21	RESET	I	RESET causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. RESET is internally synchronized.
19	CLK	I	The clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
33	MN/$\overline{\text{MX}}$	I	Minimum/Maximum: indicates what mode the processor is to operate in. The two modes are discussed in the following sections.
40	V_{CC}		+5 V (power supply)
1, 20	GND		GND (ground)

The following pin function descriptions are for the SAB 8086/8288 system in **maximum mode** (i.e. MN/$\overline{MX}$ = GND). Only the pin functions which are unique to maximum mode are described; all other pin functions are as already described.

<table>
<tr><th>Number</th><th>Symbol</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>26–28</td><td>$\overline{S_2}$, $\overline{S_1}$, $\overline{S_0}$</td><td>O</td><td>These status lines are encoded as follows:
<table>
<tr><th>S_2</th><th>S_1</th><th>S_0</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write I/O Port</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Halt</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>0</td><td>Code Access</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Passive</td></tr>
</table>
Status is active during T_4, T_1, and T_2 and is returned to the passive state (1,1,1) during T_3 or during T_w when READY is HIGH. This status is used by the SAB 8288 Bus Controller to generate all memory and I/O access control signals. Any change by S_2, S_1, or S_0 during T_4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T_3 or T_w is used to indicate the end of a bus cycle.
These signals float to 3-state OFF in "hold acknowledge".</td></tr>
<tr><td>30–31</td><td>$\overline{RQ}/\overline{GT_0}$, $\overline{RQ}/\overline{GT_1}$</td><td>I/O</td><td>The request/grant pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT_0}$ having higher priority than $\overline{RQ}/\overline{GT_1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor so may be left unconnected. The request/grant sequence is as follows (see Figure 14):
1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the SAB 8086 (pulse1).
2. During the CPU's next T_4 or T_1 a pulse 1 CLK wide from the SAB 8086 to the requesting master (pulse 2) indicates that the SAB 8086 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge".
3. A pulse 1 CLK wide from the requesting master indicates to the SAB 8086 (pulse 3) that the "hold" request is about to end and that the SAB 8086 can reclaim the local bus at the next CLK.
Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.
If the request is made while the CPU is performing a memory cycle, it will release the local bus during T_4 of the cycle when all the following conditions are met:
1. Request occurs on or before T_2.
2. Current cycle is not the low byte of a word (on an odd address).
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.</td></tr>
</table>

<table>
<tr><th>Number</th><th>Symbol</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>29</td><td>$\overline{LOCK}$</td><td>O</td><td>The $\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in "hold acknowledge".</td></tr>
<tr><td>24–25</td><td>QS_1, QS_0</td><td>O</td><td>QS_1 and QS_0 provide status to allow external tracking of the internal SAB 8086 instruction queue.
<table>
<tr><th>QS_1</th><th>QS_0</th><th>Characteristics</th></tr>
<tr><td>0 (LOW)</td><td>0</td><td>No Operation</td></tr>
<tr><td>0</td><td>1</td><td>First Byte of Op Code from Queue</td></tr>
<tr><td>1 (HIGH)</td><td>0</td><td>Empty the Queue</td></tr>
<tr><td>1</td><td>1</td><td>Subsequent Byte from Queue</td></tr>
</table>
The queue status is valid during the CLK cycle after which the queue operation is performed.</td></tr>
</table>

The following pin function descriptions are for the SAB 8086 **minimum mode** (i. e. MN/$\overline{MX}$ = V_{CC}). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described before.

Number	Symbol	Input (I) Output (O)	Function
28	M/$\overline{IO}$	O	This status line is logically equivalent to S_2 in the maximum mode. It is used to distinguish a memory access from an I/O access. M/$\overline{IO}$ becomes valid in the T_4 preceding a bus cycle and remains valid until the final T_4 of the cycle (M = HIGH, IO = LOW). M/$\overline{IO}$ floats to 3-state OFF in local bus "hold acknowledge".
29	$\overline{WR}$	O	Write strobe indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/$\overline{IO}$ signal. $\overline{WR}$ is active for T_2, T_3 and T_w of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge"
24	$\overline{INTA}$	O	$\overline{INTA}$ is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T_2, T_3 and T_w of each interrupt acknowledge cycle.
25	ALE	O	Address latch enable is provided by the processor to latch the address into the SAB 8282/SAB 8283 address latch. It is a HIGH pulse active during T_1 of any bus cycle. Note that ALE is never floated.
27	DT/$\overline{R}$	O	Data transmit/receive is needed in minimum system that desires to use a SAB 8286/SAB 8287 data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/$\overline{R}$ is equivalent to S_1 in the maximum mode, and its timing is the same as for M/$\overline{IO}$. (T=HIGH, R=LOW). This signal floats to 3-state OFF in local bus "hold acknowledge".
26	$\overline{DEN}$	O	Data enable is provided as an output enable for the SAB 8286/SAB 8287 in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access and for INTA cycles. For a read or INTA cycle it is active from the middle of T_2 until the middle of T_4, while for a write cycle it is active from the beginning of T_2 until the middle of T_4. $\overline{DEN}$ floats to 3-state OFF in local bus "hold acknowledge".
30–31	HOLD HLDA	I O	HOLD indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of T_4 or T_1. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will lower HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time. The same rules as for $\overline{RQ}$/$\overline{GT}$ apply regarding when the local bus will be released.

Figure 3. Functional Block Diagram

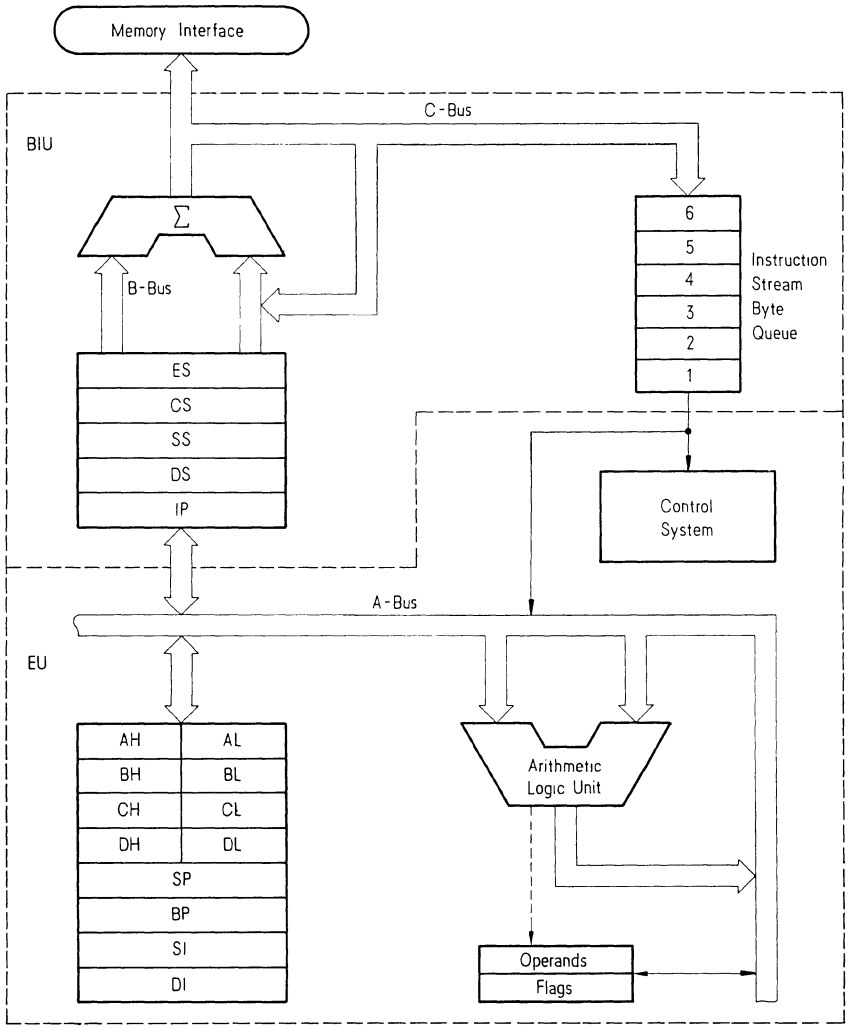
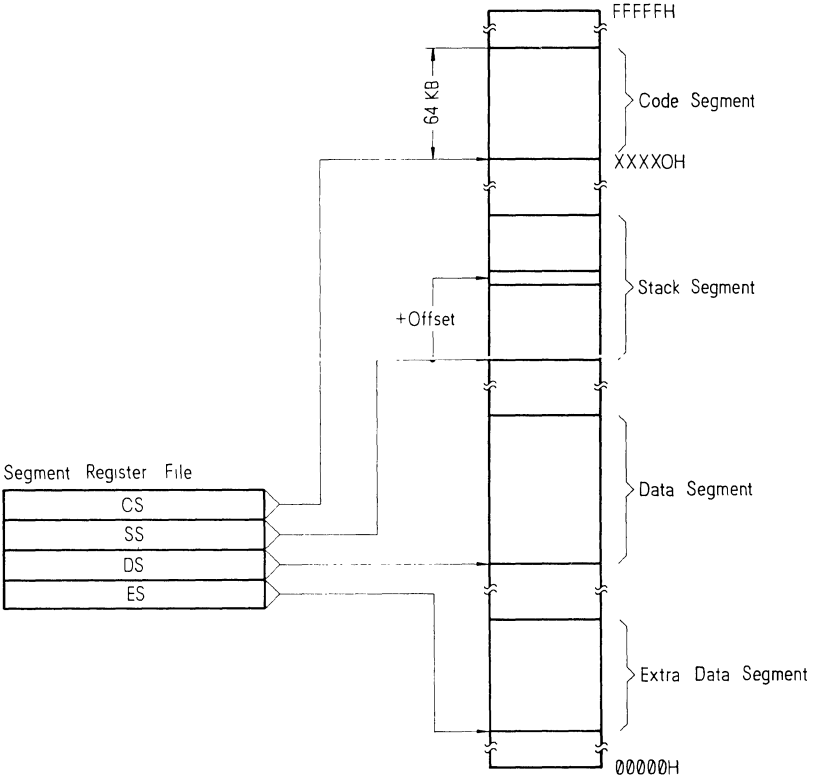


Figure 4. Memory Organization



Functional Description

The internal functions of the SAB 8086 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU) as shown in the block diagram of Figure 3.

The bus interface unit provides the functions related to instruction fetching and queuing, operand fetch and store, and address relocation. The overlap of instruction pre-fetching provided by this unit serves to increase processor performance through improved bus bandwidth utilization. Up to 6 bytes of the instruction stream can be queued while waiting for decoding and execution.

The instruction stream queuing mechanism allows the BIU to keep the memory utilized very efficiently. Whenever there is space for at least 2 bytes in the queue, the BIU will attempt a word fetch memory cycle. This greatly reduces „dead time" on the memory bus.

The execution unit receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is logically organized as a linear array of 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory can be further logically divided into code, data, alternate data, and stack segments of up to 64 Kbytes each, with each segment falling on 16-byte boundaries. (See Figure 4)

Minimum and Maximum Modes

The requirements for supporting minimum and maximum SAB 8086 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the SAB 8086 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration.

The definition of a certain subset of the pins changes dependent on the condition of the strap pin.

When MN/$\overline{MX}$ pin is strapped to GND, the SAB 8086 treats pins 24 through 31 in maximum mode. An SAB 8288 bus controller interprets status information coded into $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ to generate bus timing and control signals.

When the MN/$\overline{MX}$ pin is strapped to V_{CC}, the SAB 8086 generates bus control signals itself on pins 24 through 31, as shown in parentheses in Figure 1.

Bus Operation

The SAB 8086 has a combined address and data bus commonly referred to as a time multiplexed bus.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T_1, T_2, T_3 and T_4 (see Figure 5). The address is emitted from the processor during T_1 and data transfer occurs on the bus during T_3 and T_4. T_2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "Wait" states (T_w) are inserted between T_3 and T_4. Each inserted "Wait" state is of the same duration as a CLK cycle. Periods can occur between SAB 8086 bus cycles. These are referred to as "Idle" states (T_i) or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T_1 of any bus cycle the ALE (Address Latch Enable) signal is emitted (by either the processor or the SAB 8288 bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Status bits $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ are used, in maximum mode, by the bus controller to identify the type of bus transaction according to the following table:

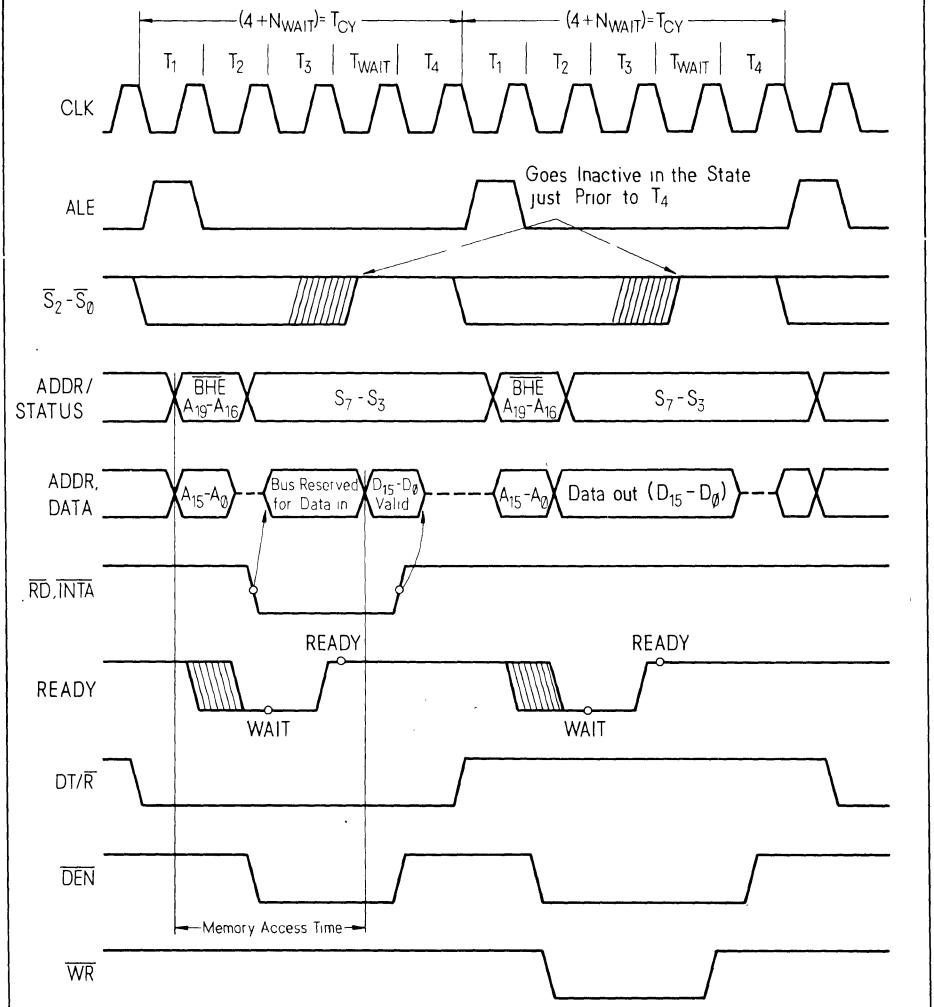
$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Characteristics
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S_3 through S_7 are multiplexed with high-order address bits and the $\overline{BHE}$ signal, and are therefore valid during T_2 through T_4. S_3 and S_4 indicate which segment register (see Instruction Set description) was used for this bus cycle in forming the address, according to the following table:

S_4	S_3	Characteristics
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S_5 is a reflection of the PSW interrupt enable bit. $S_6 = 0$ and S_7 is a spare status bit.

Figure 5. Basic System Timing



I/O Addressing

In the SAB 8086, I/O operations can address up to a maximum of 64 K I/O byte registers or 32 K I/O word registers.
The I/O address appears in the same format as the memory address on bus lines A_{15}–A_0. The address lines A_{19}–A_{16} are zero in I/O operations.
The variable I/O instructions which use register DX as a pointer have full address capability while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space.

System Components

Processors

SAB 8088	– 100% Compatible CPU with SAB 8086 with 8-bit bus
SAB 8087	– Numeric Data Processor. Coprocessor to SAB 8086 and SAB 8088.
SAB 8089	– Input / Output Processor.

Support Circuits

SAB 8282	Octal Latch
SAB 8283	Octal Latch (Inverting)
SAB 8284A	Clock Generator and Driver
SAB 8286	Octal Bus Transceiver
SAB 8287	Octal Bus Transceiver (Inverting)
SAB 8288	Bus Controller
SAB 8289	Bus Arbiter
SAB 8259A	Programmable Interrupt Controller

Typical Applications

SAB 8086 is a general purpose 16-bit microprocessor which can be used for applications ranging from process control to data processing. Figures 6 and 7 show typical system configurations for SAB 8086 familiy components.

Figure 6. Minimum Mode SAB 8086 Typical System Configuration

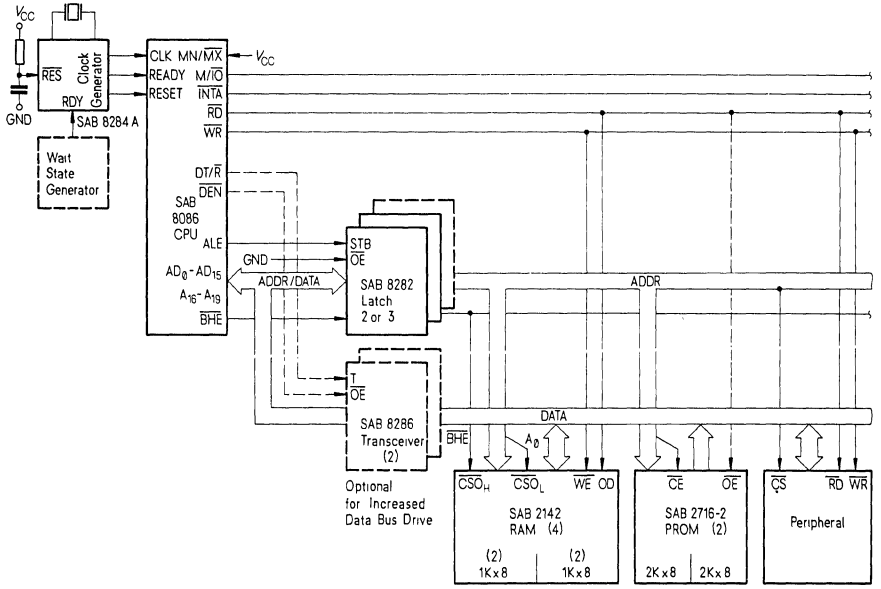
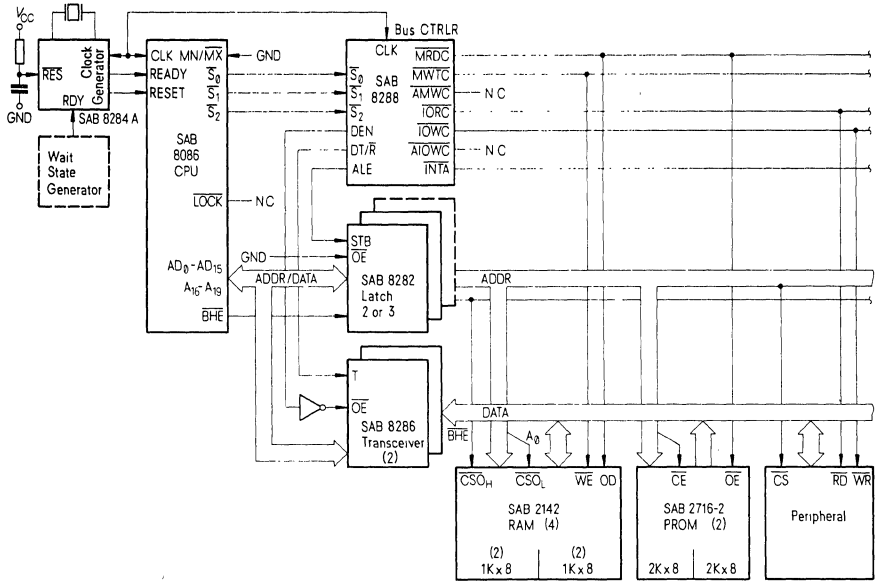


Figure 7. Maximum Mode SAB 8086 Typical System Configuration



Instruction Set Summary

DATA TRANSFER

MOV = Move	76543210	76543210	76543210	76543210
Register / memory to / from register	100010dw	mod reg r/m		
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1
Immediate to register	1011w reg	data	data if w=1	
Memory to accumulator	1010000w	addr-low	addr-high	
Accumulator to memory	1010001w	addr-low	addr-high	
Register/memory to segment register	10001110	mod 0 reg r/m		
Segment register to register/memory	10001100	mod 0 reg r/m		
PUSH = Push:				
Register/memory	11111111	mod 110 r/m		
Register	01010 reg			
Segment register	000 reg 110			
POP = Pop:				
Register/memory	10001111	mod 000 r/m		
Register	01011 reg			
Segment register	000 reg 111			
XCHG = Exchange:				
Register/memory with register	1000011w	mod reg r/m		
Register with accumulator	10010 reg			
IN = Input from:				
Fixed port	1110010w	port		
Variable port	1110110w			

OUT = Output to:	**76543210**	**76543210**	**76543210**	**76543210**
Fixed port	1110011w	port		
Variable port	1110111w			
XLAT = Translate byte to AL	11010111			
LEA = Load EA to register	10001101	mod reg r/m		
LDS = Load pointer to DS	11000101	mod reg r/m		
LES = Load pointer to ES	11000100	mod reg r/m		
LAHF = Load AH with flags	10011111			
SAHF = Store AH into flags	10011110			
PUSHF = Push flags	10011100			
POPF =Pop flags	10011101			

ARITHMETIC
ADD = Add:

Reg./memory with register to either	000000dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s: w=01
Immediate to accumulator	0000010w	data	data if w=1	

ADC = Add with carry:

Reg./memory with register to either	000100dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s:w=01
Immediate to accumulator	0001010w	data	data if w=1	

INC = Increment:

Register/memory	1111111w	mod 000 r/m
Register	01000reg	
AAA = ASCII adjust for add	00110111	
DAA = Decimal adjust for add	00100111	

SUB = Subtract:	76543210	76543210	76543210	76543210
Reg./memory and register to either	001010dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s:w=01
Immediate from accumulator	0010110w	data	data if w=1	

SBB = Subtract with borrow				
Reg./memory and register to either	000110dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s:w=01
Immediate from accumulator	0001110w	data	data if w=1	

DEC = Decrement:	76543210	76543210	76543210	76543210
Register/memory	1111111w	mod 001 r/m		
Register	01001reg			
NEG = Change sign	1111011w	mod 011 r/m		

CMP = Compare:				
Register/memory and register	001110dw	mod reg r/m		
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s:w=01
Immediate with accumulator	0011110w	data	data if w=1	
AAS = ASCII adjust for subtract	00111111			
DAS = Decimal adjust for subtract	00101111			
MUL = Multiply (unsigned)	1111011w	mod 100 r/m		
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m		
AAM = ASCII adjust for multiply	11010100	00001010		
DIV = Divide (unsigned)	1111011w	mod 110 r/m		
IDIV = Integer divide (signed)	1111011w	mod 111 r/m		
AAD = ASCII adjust for divide	11010101	00001010		
CBW = Convert byte to word	10011000			
CWD = Convert word to double word	10011001			

LOGIC	76543210	76543210	76543210	76543210
NOT = Invert	1111011w	mod010r/m		
SHL/SAL = Shift logical/arithmetic left	110100vw	mod100r/m		
SHR = Shift logical right	110100vw	mod101r/m		
SAR = Shift arithmetic right	110100vw	mod111r/m		
ROL = Rotate left	110100vw	mod000r/m		
ROR = Rotate right	110100vw	mod001r/m		
RCL = Rotate through carry flag left	110100vw	mod010r/m		
RCR = Rotate through carry right	110100vw	mod011r/m		
AND = And:				
Reg/memory and register to either	001000dw	mod reg r/m		
Immediate to register/memory	1000000w	mod100r/m	data	data if w=1
Immediate to accumulator	0010010w	data	data if w=1	
TEST = And function to flags, no result:				
Register/memory and register	1000010w	mod reg r/m		
Immediate data and register/memory	1111011w	mod000r/m	data	data if w=1
Immediate data and accumulator	1010100w	data	data if w=1	
OR = Or:				
Reg/memory and register to either	000010dw	mod reg r/m		
Immediate to register/memory	1000000w	mod001r/m	data	data if w=1
Immediate to accumulator	0000110w	data	data if w=1	
XOR = Exclusive or:				
Reg./memory and register to either	001100dw	mod reg r/m		
Immediate to register/memory	1000000w	mod110r/m	data	data if w=1
Immediate to accumulator	0011010w	data	data if w=1	

STRING MANIPULATION	76543210	76543210	76543210
REP = Repeat	1111001z		
MOVS = Move byte/word	1010010w		
CMPS = Compare byte/word	1010011w		
SCAS = Scan byte/word	1010111w		
LODS = Load byte/word to AL/AX	1010110w		
STDS = Store byte/word from AL/A	1010101w		

CONTROL TRANSFER

CALL = **Call**:			
Direct within segment	11101000	disp-low	disp-high
Indirect within segment	11111111	mod 010 r/m	
Direct intersegment	10011010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 011 r/m	

JMP = **Unconditional Jump**:			
Direct within segment	11101001	disp-low	disp-high
Direct within segment short	11101011	disp	
Indirect within segment	11111111	mod 100 r/m	
Direct intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 101 r/m	

RET = Return from CALL:	**76543210**	**76543210**	**76543210**
Within segment	11000011		
Within seg. adding immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment adding immediable to SP	11001010	data-low	data-high
JE/JZ = Jump on equal/zero	01110100	disp	
JL/JNGE = Jump on less/not greater or equal	01111100	disp	
JLE/JNG = Jump on less or equal/not greater	01111110	disp	
JB/JNAE = Jump on below/not above or equal	01110010	disp	
JBE/JNA = Jump on below or equal/ not above	01110110	disp	
JP/JPE = Jump on parity/parity even	01111010	disp	
JO = Jump on overflow	01110000	disp	
JS = Jump on sign	01111000	disp	
JNE/JNZ = Jump on not equal/not zero	01110101	disp	
JNL/JGE = Jump on not less/greater or equal	01111101	disp	
JNLE/JG = Jump on not less or equal/ greater	01111111	disp	
JNB/JAE = Jump on not below/above or equal	01110011	disp	
JNBE/JA = Jump on not below or equal/above	01110111	disp	
JNP/JPO = Jump on not par/par odd	01111011	disp	
JNO = Jump on not overflow	01110001	disp	
JNS = Jump on not sign	01111001	disp	
LOOP = Loop CX times	11100010	disp	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp	
JCXZ = Jump on CX zero	11100011	disp	

INT = Interrupt	**76543210**	**76543210**
Type specified	11001101	type
Type 3	11001100	
INTO = Interrupt on overflow	11001110	
IRET = Interrupt return	11001111	

PROCESSOR CONTROL

CLC = Clear carry	11111000	
CMC = Complement carry	11110101	
STC = Set Carry	11111001	
CLD = Clear direction	11111100	
STD = Set direction	11111101	
CLI = Clear interrupt	11111010	
STI = Set interrupt	11111011	
HLT = Halt	11110100	
WAIT = Wait	10011011	
ESC = Escape (to external device)	11011xxx	mod x x x r/m
LOCK = Bus lock prefix	11110000	

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp high is absent
if mod = 10 then DISP = disp-high: disp low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) +DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high:disp-low.

if s:w = 01 then 16-bits of immediate data from the operand
it s:w = 11 then an immediate data byte is sign extended to form the 16-bit operand
if v = 0 then "count" = 1; if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparsion with ZF FLAG

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table

16-Bit (w=1)	8-Bit (w=0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instruction which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Absolute maximum ratings *)

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on any Pin with Respect to Ground	−1.0 to +7V
Power Dissipation	2.5 Watt

D.C. Characteristics

SAB 8086: T_A = 0 to 70°C, V_{CC} = 5 V ±10%
SAB 8086-1/8086-2: T_A = 0 to 70°C, V_{CC} = 5 V ± 5%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	+0.8	V	–
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5		
V_{OL}	Output Low Voltage	–	0.45		I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4	–		I_{OH} = −400 µA
I_{CC}	Power Supply Current SAB 8086 SAB 8086-2 SAB 8086-1	–	 340 350 360	mA	T_A = 25°C
I_{LI}	Input Leakage Current		±10	µA	0V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current				0.45 V ≤ V_{OUT} ≤ V_{CC}
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	–
V_{CH}	Clock Input High Voltage	3.9	V_{CC}+1.0		
C_{IN}	Capacitance of Input Buffer (All input except AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)	–	15	pF	f_C = 1 MHz
C_{IO}	Capacitance of I/O Buffer (AD_0–AD_{15}, $\overline{RQ}/\overline{GT}$)				

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics for SAB 8086/8086-2

SAB 8086: T_A = 0 to 70°C, V_{CC} = 5 V ± 10%
SAB 8086-2: T_A = 0 to 70°C, V_{CC} = 5 V ± 5%

Minimum Complexity System (Figures 8, 9, 12, 15)
Timing Requirements

Symbol	Parameter	Limit Values				Units	Test Conditions
		SAB 8086		SAB 8086-2			
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period SAB 8086	200	500	125	500	ns	–
TCLCH	CLK Low Time	118	–	68			
TCHCL	CLK High Time	69		44			
TCH1CH2	CLK Rise Time	–	10	–	10		From 1.0 to 3.5V
TCL2CL1	CLK Fall Time						From 3.5 to 1.0V
TDVCL	Data in Setup Time	30	–	20	–		–
TCLDX	Data in Hold Time	10		10			
TR1VCL	RDY Setup Time into SAB 8284A [1) 2)]	35		35			
TCLR1X	RDY Hold Time into SAB 8284A [1) 2)]	0		0			
TRYHCH	READY Setup Time into SAB 8086	118		68			
TCHRYX	READY Hold Time into SAB 8086	30		20			
TRYLCL	READY Inactive to CLK [3)]	−8		−8			
THVCH	HOLD Setup Time	35		20			
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time [2)]	30		15			
TILIH	Input Rise Time (Except CLK)	–	20	–	20		From 0.8 to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12		From 2.0 to 0.8V

[1)] Signal at SAB 8284A shown for reference only.
[2)] Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3)] Applies only to T_2 state. (8 ns into T_3)

Timing Responses

Symbol	Parameter	Limit Values				Units	Test Conditions
		SAB 8086		SAB 8086-2			
		Min.	Max.	Min.	Max.		
TCLAV	Address Valid Delay	10	110	10	60	ns	C_L = 20–100 pF for all SAB 8086 Outputs (In addition to SAB 8086 self-load)
TCLAX	Address Hold Time		–		–		
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50		
TLHLL	ALE Width	TCLCH–20	–	TCLCH–10	–		
TCLLH	ALE Active Delay	–	80	–	50		
TCHLL	ALE Inactive Delay		85		55		
TLLAX	Address Hold Time to ALE Inactive	TCHCL–10	–	TCHCL–10	–		
TCLDV	Data Valid Delay	10	110	10	60		
TCHDX	Data Hold Time		–		–		
TWHDX	Data Hold Time After WR	TCLCH–30		TCLCH–30			
TCVCTV	Control Active Delay 1	10	110	10	70		
TCHCTV	Control Active Delay 2				60		
TCVCTX	Control Inactive Delay				70		
TAZRL	Address Float to READ Active	0	–	0	–		
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100		
TCLRH	$\overline{RD}$ Inactive Delay		150		80		
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL–45	–	TCLCL–40	–		
TCLHAV	HLDA Valid Delay	10	160	10	100		
TRLRH	$\overline{RD}$ Width	2TCLCL–75	–	2TCLCL–50	–		
TWLWH	$\overline{WR}$ Width	2TCLCL–60		2TCLCL–40			
TAVAL	Address Valid to ALE Low	TCLCH–60		TCLCH–40			
TOLOH	Output Rise Time	–	20	–	20		From 0.8 to 2.0V
TOHOL	Output Fall Time		12		12		From 2.0 to 0.8V

Max Mode System (Using SAB 8288 Bus Controller) (Figures 10–14)
Timing Requirements

Symbol	Parameter	Limit Values				Units	Test Conditions
		SAB 8086		SAB 8086-2			
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period SAB 8086	200	500	125	500	ns	–
TCLCH	CLK Low Time	118	–	68	–		
TCHCL	CLK High Time	69		44			
TCH1CH2	CLK Rise Time	–	10	–	10		From 1.0 to 3.5V
TCL2CL1	CLK Fall Time						From 3.5 to 1.0V
TDVCL	Data In Setup Time	30	–	20	–		–
TCLDX	Data In Hold Time	10		10			
TR1VCL	RDY Setup Time into SAB 8284A [1] [2]	35		35			
TCLR1X	RDY Hold Time into SAB 8284A [1] [2]	0		0			
TRYHCH	READY Setup Time into SAB 8086	118		68			
TCHRYX	READY Hold Time into SAB 8086	30		20			
TRYLCL	READY Inactive to CLK [4]	–8		–8			
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) [2]	30		15			
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time						
TCHGX	$\overline{RQ}$ Hold Time into SAB 8086	40		30			
TILIH	Input Rise Time (Except CLK)	–	20	–	20		From 0.8 to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12		From 2.0 to 0.8V

[1]) Signal at SAB 8284A or SAB 8288 shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T_3 and wait states.
[4]) Applies only to T_2 state (8 ns into T_3).

Timing Responses

Symbol	Parameter	Limit Values				Units	Test Conditions
		SAB 8086		SAB 8086-2			
		Min.	Max.	Min.	Max.		
TCLML	Command Active Delay [1]	10	35	10	35	ns	C_L = 20–100 pF for all SAB 8086 Outputs (In addition to SAB 8086 self-load)
TCLMH	Command Inactive Delay [1]						
TRYHSH	READY Active to Status Passive [3]	–	110	–	65		
TCHSV	Status Active Delay	10		10	60		
TCLSH	Status Inactive Delay		130		70		
TCLAV	Address Valid Delay		110		60		
TCLAX	Address Hold Time		–		–		
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50		
TSVLH	Status Valid to ALE High [1]	–	20	–	20		
TSVMCH	Status Valid to MCE High [1]						
TCLLH	CLK Low to ALE Valid [1]						
TCLMCH	CLK Low to MCE High [1]						
TCHLL	ALE Inactive Delay [1]	4	15	4	15		
TCLDV	Data Valid Delay	10	110	10	60		
TCHDX	Data Hold Time		–		–		
TCVNV	Control Active Delay [1]	5	45	5	45		
TCVNX	Control Inactive Delay [1]	10		10			

[1]) Signal at SAB 8284A or SAB 8288 shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T_3 and wait states.
[4]) Applies only to T_2 state (8 ns into T_3).

Symbol	Parameter	Limit Values				Units	Test Conditions
		SAB 8086		SAB 8086-2			
		Min.	Max.	Min.	Max.		
TAZRL	Address Float to READ Active	0	–	0	–	ns	C_L = 20–100 pF for all SAB 8086 Outputs (In addition to SAB 8086 self-load)
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100		
TCLRH	$\overline{RD}$ Inactive Delay		150		80		
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL–45	–	TCLCL–40	–		
TCHDTL	Direction Control Active Delay [1]	–	50	–	50		
TCHDTH	Direction Control Inactive Delay [1]		30		30		
TCLGL	$\overline{GT}$ Active Delay	0	85	0	50		
TCLGH	$\overline{GT}$ Inactive Delay						
TRLRH	$\overline{RD}$ Width	2TCLCL–75	–	2TCLCL–50	–		
TOLOH	Output Rise Time	–	20	–	20		From 0.8 to 2.0V
TOHOL	Output Fall Time		12		12		From 2.0 to 0.8V

[1]) Signal at SAB 8284A or SAB 8288 shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T_3 and wait states.
[4]) Applies only to T_2 state (8 ns into T_3).

A.C. Characteristics for SAB 8086-1

T_A = 0 to 70°C, V_{CC} = 5V ± 5%

Minimum Complexity System (Figures 8, 9, 12, 15)
Timing Requirements (Preliminary)

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
TCLCL	CLK Cycle Period	100	500	ns	
TCLCH	CLK Low Time	53	–		–
TCHCL	CLK High Time	39			
TCH1CH2	CLK Rise Time	–	10		From 1.0 to 3.5V
TCL1CL2	CLK Fall Time				From 3.5 to 1.0V
TDVCL	Data in Setup Time	5			
TCLDX	Data in Hold Time	10			
TR1VCL	RDY Setup Time into SAB 8284A[1])[2])	35			
TCLR1X	RDY Hold Time into SAB 8284A[1])[2])	0			
TRYHCH	READY Setup Time into SAB 8086	53	–		–
TCHRYX	READY Hold Time into SAB 8086	20			
TRYLCL	READY Inactive to CLK[3])	–10			
THVCH	HOLD Setup Time	20			
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time [2])	15			
TILIH	Input Rise Time (Except CLK)	–	20		From 0.8 to 2.0V
TILHIL	Input Fall Time (Except CLK)		12		From 2.0 to 0.8V

[1]) Signal at SAB 8284A shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T_2 state. (8 ns into T_3)

Timing Responses SAB 8086-1 (Preliminary)

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
TCLAV	Address Valid Delay	10	50	ns	C_L = 20–100 pF for all SAB 8086 Outputs (In addition to SAB 8086 self-load)
TCLAX	Address Hold Time		–		
TCLAZ	Address Float Delay		40		
TLHLL	ALE Width	TCLCH-10	–		
TCLLH	ALE Active Delay	–	40		
TCHLL	ALE Inactive Delay		45		
TLLAX	Address Hold Time to ALE Inactive	TCHCL-10	–		
TCLDV	Data Valid Delay	10	50		
TCHDX	Data Hold Time		–		
TWHDX	Data Hold Time After WR	TCLCH-25			
TCVCTX	Control Active Delay 1	10	50		
TCHCTV	Control Active Delay 2		45		
TCVCTX	Control Inactive Delay		50		
TAZRL	Address Float to READ Active	0	–		
TCLRL	$\overline{RD}$ Active Delay	10	70		
TCLRH	$\overline{RD}$ Inactive Delay		60		
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL-35	–		
TCLHAV	HLDA Valid Delay	10	60		
TRLRH	$\overline{RD}$ Width	2TCLCL-40	–		
TWLWH	$\overline{WR}$ Width	2TCLCL-35			
TAVAL	Address Valid to ALE Low	TCLCH-35			
TOLOH	Output Rise Time	–	20		From 0.8 to 2.0V
TOHOL	Output Fall Time		12		From 2.0 to 0.8V

Max Mode System (Using SAB 8288 Bus Controller) (Figures 10-14)
Timing Requirements SAB 8086-1 (Preliminary)

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
TCLCL	CLK Cycle Period	100	500	ns	–
TCLCH	CLK Low Time	53	–		
TCHCL	CLK High Time	39			
TCH1CH2	CLK Rise Time	–	10		From 1.0 to 3.5V
TCL2CL1	CLK Fall Time				From 3.5 to 1.0V
TDVCL	Data In Setup Time	5	–		
TCLDX	Data In Hold Time	10			
TR1VCL	RDY Setup Time into SAB 8284A[1])[2])	35			
TCLR1X	RDY Hold Time into SAB 8284A[1])[2])	0			
TRYHCH	READY Setup Time into SAB 8086	53			
TCHRYX	READY Hold Time into SAB 8086	20			
TRYLCL	READY Inactive to CLK[3])	–10			
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{\text{TEST}}$)[2])	15			
TGVCH	$\overline{\text{RQ}}/\overline{\text{GT}}$ Setup Time	12			
TCHGX	$\overline{\text{RQ}}$ Hold Time into SAB 8086	20			
TILIH	Input Rise Time (Except CLK)	–	20		From 0.8 to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		From 2.0 to 0.8V

[1]) Signal at SAB 8284A or SAB 8288 shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T_2 state (8 ns into T_3).

Timing Responses SAB 8086-1 (Preliminary)

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
TCLML	Command Active Delay[1])	10	35	ns	C_L = 20–100 pF for all SAB 8086 Outputs (In addition to SAB 8086 self-load)
TCLMH	Command Inactive Delay[1])				
TRYHSH	READY Active to Status Passive[2])	–	45		
TCHSV	Status Active Delay	10			
TCLSH	Status Inactive Delay		55		
TCLAV	Address Valid Delay		50		
TCLAX	Address Hold Time		–		
TCLAZ	Address Float Delay		40		
TSVLH	Status Valid to ALE High[1])	–	20		
TSVMCH	Status Valid to MCE High[1])				
TCLLH	CLK Low to ALE Valid[1])				
TCLMCH	CLK Low to MCE High[1])				
TCHLL	ALE Inactive Delay[1])	4	15		
TCLDV	Data Valid Delay	10	50		
TCHDX	Data Hold Time		–		
TCVNV	Control Active Delay[1])	5	45		
TCVNX	Control Inactive Delay[1])	10			

[1]) Signal at SAB 8284A or SAB8288 shown for reference only.
[2]) Applies only to T_2 and wait states.

Timing Responses SAB 8086-1 (continued)
(Preliminary)

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
TAZRL	Address Float to READ Active	0	–	ns	C_L = 20–100 pF for all SAB 8086 Outputs (In addition to SAB 8086 self-load)
TCLRL	$\overline{RD}$ Active Delay	10	70		
TCLRH	$\overline{RD}$ Inactive Delay		60		
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL-35	–		
TCHDTL	Direction Control Active Delay[1])	–	50		
TCHDTH	Direction Control Inactive Delay[1])		30		
TCLGL	$\overline{GT}$ Active Delay	0	45		
TCLGH	$\overline{GT}$ Inactive Delay				
TRLRH	$\overline{RD}$ Width	2TCLCL-40	–		
TOLOH	Output Rise Time	–	20		From 0.8 to 2.0V
TOHOL	Output Fall Time		12		From 2.0 to o.8V

[1]) Signal at SAB 8284A or SAB 8288 shown for reference only.
[2]) Applies only to T_3 and wait states.

Figure 8. Bus Timing – Minimum Mode System

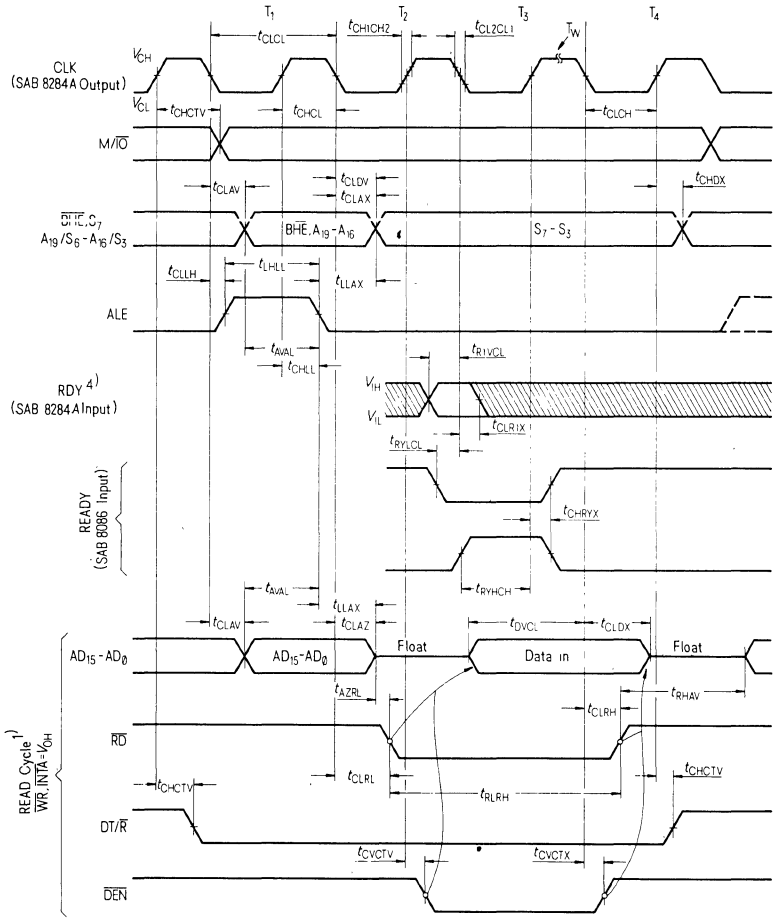
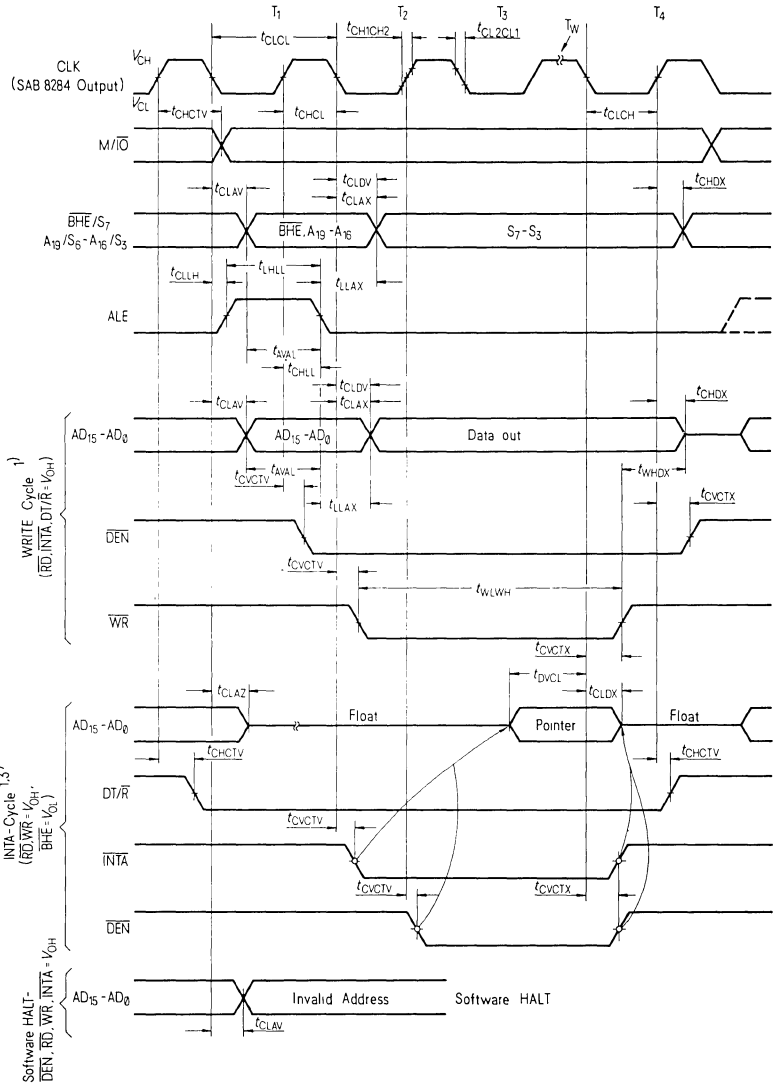


Figure 9. SAB 8086 Bus Timing – Minimum Mode System (cont'd)



[1]) All signals switch between V_{OH} and V_{OL} unless otherwise specified.
[2]) RDY is sampled near the end of T_2, T_3, T_w to determine if T_w machines states are to be inserted.
[3]) Two INTA cycles run back to back. The SAB 8086 local ADDR/DATA Bus is floating during both INTA cycles. Control signals shown for second INTA cycle.
[4]) Signals at SAB 8284A are shown for reference only.
[5]) All timing measurements are made at 1.5 V unless otherwise noted.

Figure 10. SAB 8086 Bus Timing – Maximum Mode System (Using SAB 8288)

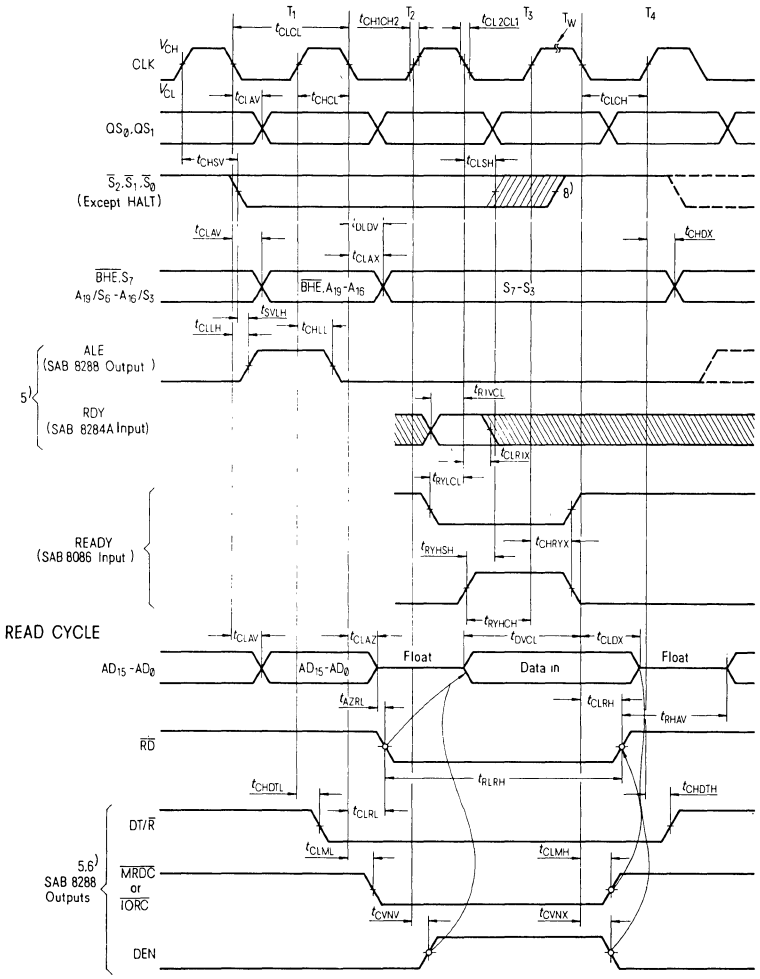
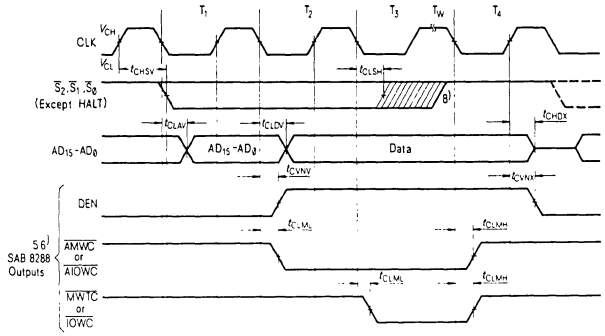
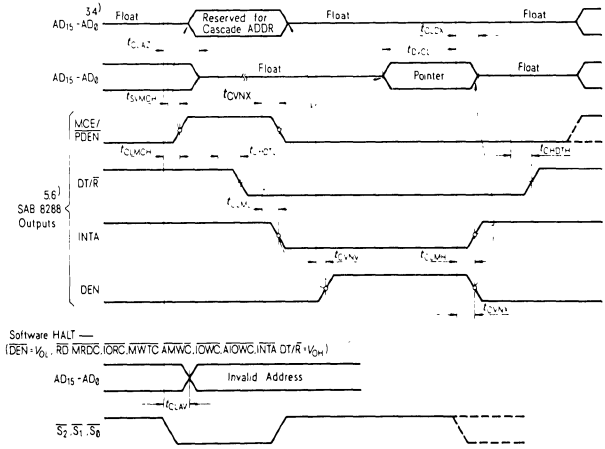


Figure 11. SAB 8086 Bus Timing – Maximum Mode System (Using SAB 8288) (cont.)

WRITE CYCLE

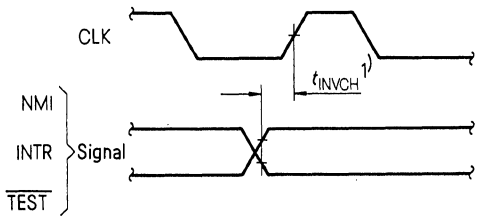


INTA CYCLE



1) All Signals switch between V_{OH} and V_{OL} unless otherwise specified.
2) RDY is sampled near the end of T_2, T_3, T_w to determine if T_w machines states are to be inserted.
3) Cascade address is valid between first and second INTA cycle.
4) Two INTA cycles run back-to-back. The SAB 8086 local ADDR/DATA Bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5) Signals at SAB 8284A or SAB 8288 are shown for reference only.
6) The issuance of the SAB 8288 command and control signals ($\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$ and DEN) lags the active HIGH SAB 8288 DEN.
7) All timing measurements are made at 1.5 V unless otherwise noted.
8) Status inactive in state just prior to T_4.

Figure 12. Asynchronous Signal Recognition



1) Setup requirements for asynchronous signals only to guarantee recognition at next CLK

Figure 13. Bus Lock Signal Timing (Maximum Mode Only)

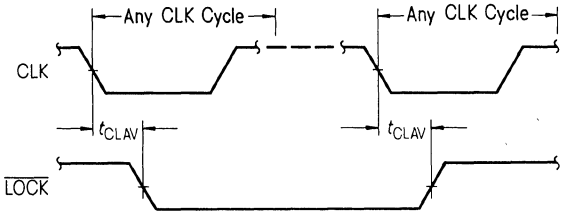
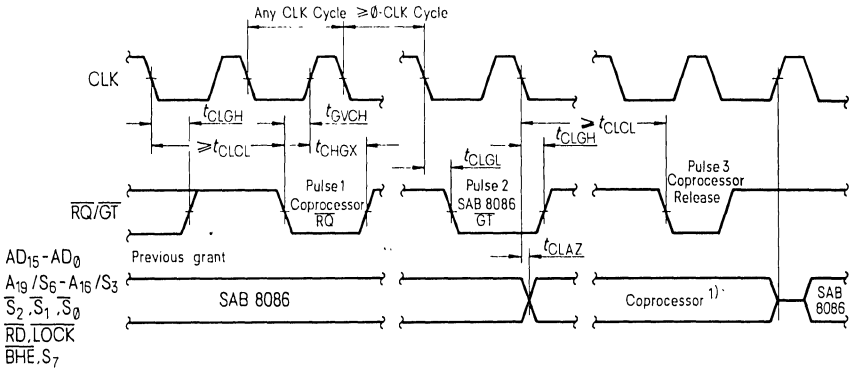
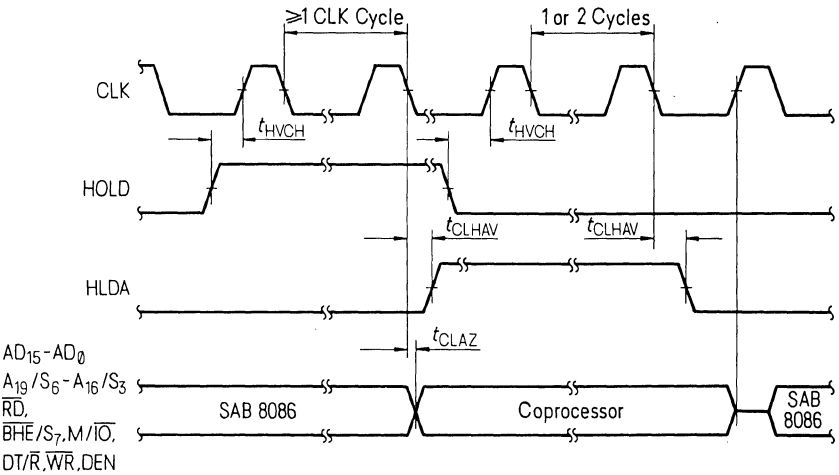


Figure 14. Request/Grant Sequence Timing (Maximum Mode Only)



[1]) The coprocessor may not drive the buses outside the region shown without risking contention

Figure 15. Hold/Hold Acknowledge Timing (Minimum Mode Only)



SAB 8088
8-Bit Microprocessor

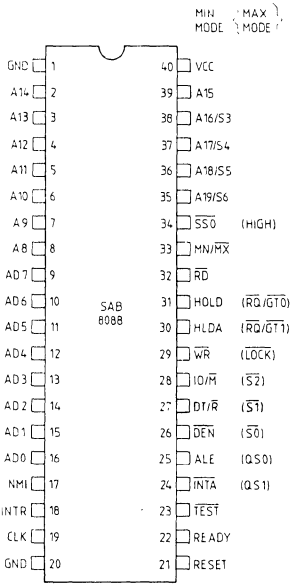
SAB 8088 5 MHz

- 8 Bit Data Bus Interface
- 16 Bit Internal Architecture
- Direct Addressing Capability to 1 MByte of Memory
- Software Compatible with SAB 8086
- 14-Word by 16-Bit Register Set with Symetrical Operations
- Byte, Word, and Block Operations

SAB 8088-2 8 MHz

- 24 Operand Addressing Modes
- 8-Bit and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal, Including Multiply and Divide
- Two Clock Rates:
  5 MHz for SAB 8088
  8 MHz for SAB 8088-2
- Compatible with Industry Standard 8088

Pin Configuration



Pin Names

AD0-7	Address/Data
$\overline{S}$0-2	Status
INTR	Interrupt Request
CLK	Clock
QS0-1	Queue Status
$\overline{TEST}$	Test for Busy
READY	Ready
RESET	Chip Reset
MN/$\overline{MX}$	Minimum/Maximum Mode
$\overline{RD}$	Read
$\overline{RQ}$/GT0-1	Request/Grant
$\overline{LOCK}$	Bus Lock
IO/$\overline{M}$	IO/Memory
A8-19	Address
S3-6	Status
$\overline{SS0}$	Status (= $\overline{S0}$)
HOLD	Hold
HLDA	Hold Acknowledge
$\overline{WR}$	Write
DT/$\overline{R}$	Bus Driver Transmit/Receive
$\overline{DEN}$	Bus Driver Enable
ALE	Address Latch Enable
$\overline{INTA}$	Interrupt Acknowledge
NMI	Non-maskable Interrupt
VCC	+ 5 Volt
GND	Ground

SAB 8088 is a high-performance 8-bit microprocessor implemented in + 5 volts, advanced Siemens MYMOS technology, packaged in a 40-pin package. It is 100 percent compatible with the industry standard 8088. With features like string handling, 16-bit arithmetic with multiply and divide it significantly increases system performance. It is highly suited for multiprocessor applications in various configurations.

Pin Definitions and Functions

The following pin function descriptions are for SAB 8088 systems in either minimum or maximum mode. The "local bus" in these descriptions is the direct multiplexed bus interface connection to the SAB 8088 (without regard to additional bus buffers).

<table>
<tr><th>Symbol</th><th>Number</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>AD7–AD0</td><td>9–16</td><td>I/O</td><td>ADDRESS DATA BUS: These lines constitute the time multiplexed memory I/O address (T1) and data (T2, T3, Tw, and T4) bus. These lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A15–A8</td><td>39, 2–8</td><td>O</td><td>ADDRESS BUS: These lines provide address bits 8 through 15 for the entire bus cycle (T1–T4). These lines do not have to be latched by ALE to remain valid. A15–A8 are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge".</td></tr>
<tr><td>A19/S6, A18/S5,
A17/S4, A16/S3</td><td>34–38</td><td>O</td><td>ADRESS/STATUS: During T1, these are the four most significant address lines for memory operations. During I/O operations, these lines are LOW. During memory and I/O operations, status information is available on these lines during T2, T3, Tw and T4. S6 is always low. The status of the interrupt enable flag bit (S5) is updated at the beginning of each clock cycle. S4 and S3 are encoded as shown.
<table>
<tr><th>S4</th><th>S3</th><th>Characteristics</th></tr>
<tr><td>0</td><td>0</td><td>Alternate Data</td></tr>
<tr><td>0</td><td>1</td><td>Stack</td></tr>
<tr><td>1</td><td>0</td><td>Code or None</td></tr>
<tr><td>1</td><td>1</td><td>Data</td></tr>
</table>
This information indicates which segment register is presently being used for data accessing.
These lines float to 3-state OFF during local bus "hold acknowledge".</td></tr>
<tr><td>$\overline{RD}$</td><td>32</td><td>O</td><td>READ: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the IO/$\overline{M}$ pin or S2. This signal is used to read devices which reside on the SAB 8088 local bus. $\overline{RD}$ is active LOW during T2, T3 and Tw of any read cycle, and is guaranteed to remain HIGH in T2 until the SAB 8088 local bus has floated.
This signal floats to 3-state OFF in "hold acknowledge".</td></tr>
<tr><td>READY</td><td>22</td><td>I</td><td>READY: is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The RDY signal from memory or I/O is synchronized by the SAB 8284A/8284B clock generator to form READY. This signal is active HIGH. The SAB 8088 READY input is not synchronized. Correct operation is not guaranteed if the set up and hold times are not met.</td></tr>
<tr><td>INTR</td><td>18</td><td>I</td><td>INTERRUPT REQUEST: is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. A subroutine is vectored to via an interrupt vector lookup table located in system memory. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH.</td></tr>
</table>

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
$\overline{TEST}$	23	I	$\overline{TEST}$: input is examined by the "wait for test" instruction. If the $\overline{TEST}$ input is LOW, execution continues, otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.
NMI	17	I	NON-MASKABLE INTERRUPT: is an edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized.
RESET	21	I	RESET: causes the processor to immediately terminate its present activity. The signal must be active HIGH for at least four clock cycles. It restarts execution, as described in the instruction set description, when RESET returns LOW. RESET is internally synchronized.
CLK	19	I	CLOCK: provides the basic timing for the processor and bus controller. It is asymmetric with a 33% duty cycle to provide optimized internal timing.
VCC	40	–	POWER SUPPLY (+5V)
GND	1, 20	–	GROUND (0V)
MN/$\overline{MX}$	*33*	I	MINIMUM/MAXIMUM: indicates what mode the processor is to operate in. The two modes are discussed in the following sections.

The following pin function descriptions are for the SAB 8088 minimum mode (i.e. MN/$\overline{MX}$ = VCC). Only the pin functions which are unique to minimum mode are described; all other pin functions are as described above.

IO/$\overline{M}$	28	O	STATUS LINE: is an inverted maximum mode $\overline{S2}$. It is used to distinguish a memory access from an I/O access. IO/$\overline{M}$ becomes valid in the T4 preceding a bus cycle and remains valid until the final T4 of the cycle (I/O = HIGH, M = LOW). IO/$\overline{M}$ floats to 3-state OFF in local bus "hold acknowledge".
$\overline{WR}$	29	O	WRITE: strobe indicates that the processor is performing a write memory or write I/O cycle depending on the state of the IO/$\overline{M}$ signal. $\overline{WR}$ is active for T2, T3, and Tw of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge".
$\overline{INTA}$	24	O	INTA: is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and Tw of each interrupt acknowledge cycle.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
ALE	25	O	ADDRESS LATCH ENABLE: is provided by the processor to latch the address into the SAB 8282 /8282A/8283/8283A address latch. It is a HIGH pulse active during clock low of T1 of any bus cycle. Note that ALE is never floated.
DT/$\overline{R}$	27	O	DATA TRANSMIT/RECEIVE: is needed in a minimum system that desires to use an SAB 8286/8286A/8287/8287A data bus transceiver. It is used to control the direction of data flow through the transceiver. Logically, DT/$\overline{R}$ is equivalent to $\overline{S1}$ in the maximum mode, and its timing is the same as for IO/$\overline{M}$ (T = HIGH, R = LOW). This signal floats to 3-state OFF in local "hold acknowledge".
$\overline{DEN}$	26	O	DATA ENABLE: is provided as an output enable for the SAB 8286/8286A/ 8287/8287A in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and I/O access, and for $\overline{INTA}$ cycles. For a read or $\overline{INTA}$ cycle, it is active from the middle of T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. $\overline{DEN}$ floats to 3-state OFF during local bus "hold acknowledge".
HOLD, HLDA	31, 30	I/O	HOLD: indicates that another master is requesting a local bus "hold". To be acknowledged, HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement, in the middle of a T4 or T1 clock cycle. Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor lowers HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines. Hold is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the set up time.
$\overline{SSO}$	34	O	STATUS LINE: is logically equivalent to $\overline{SO}$ in the maximum mode. The combination of $\overline{SSO}$, IO/$\overline{M}$ and DT/$\overline{R}$ allows the system to completely decode the current bus cycle status.

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SSO}$	Characteristics
1	0	0	Interrupt Acknowledge
1	0	1	Read I/O Port
1	1	0	Write I/O Port
1	1	1	Halt
0	0	0	Code access
0	0	1	Read memory
0	1	0	Write memory
0	1	1	Passive

Pin Definitions and Functions (continued)

The following pin function descriptions are for the SAB 8088/8288 system in maximum mode (i.e. MN/MX GND). Only the pin functions which are unique to maximum mode are described. All other pin functions are as described above.

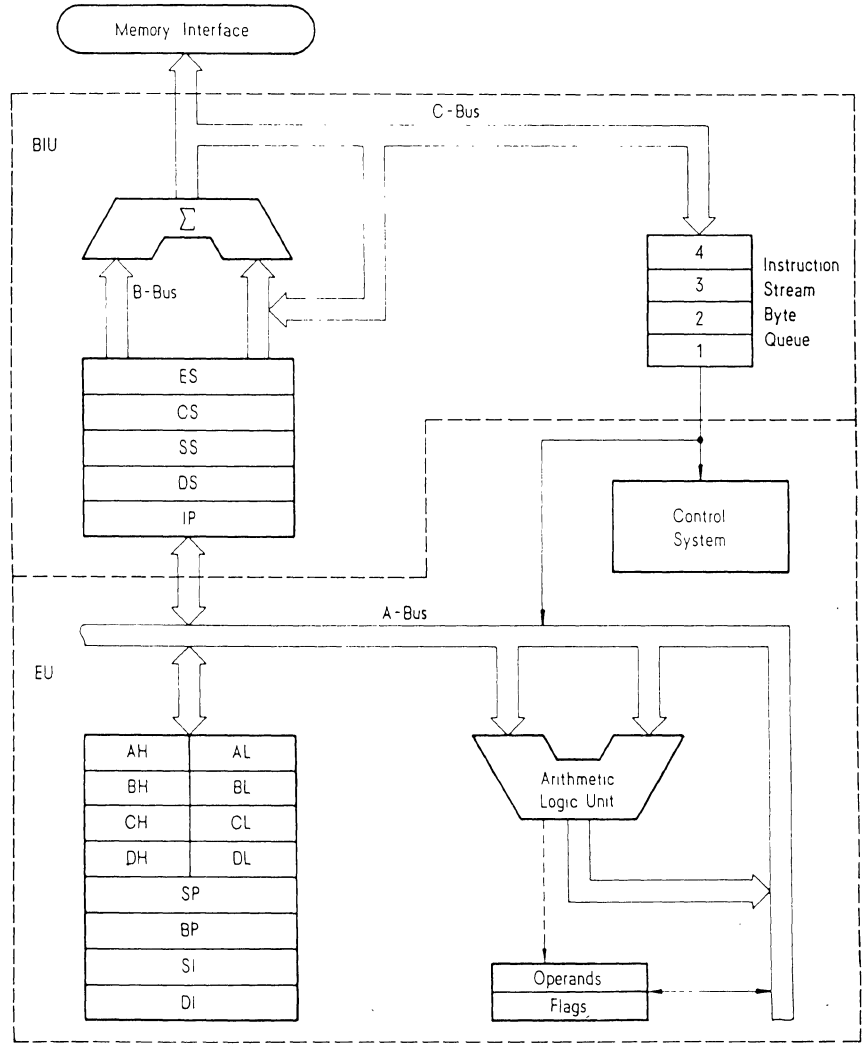
Symbol	Number	Input (I) Output (O)	Function
S2, S1, S0	28 26	O	STATUS: is active during clock high of T4, T1, and T2, and is returned to the passive state (1,1,1) during T3 or during Tw when READY is HIGH. This status is used by the SAB 8288/8288A bus controller to generate all memory and I/O access control signals. Any change by $\overline{S2}$, $\overline{S1}$, or $\overline{S0}$ during T4 is used to indicate the beginning of a bus cycle, and the return to the passive state in T3 or Tw is used to indicate the end of a bus cycle. These signals float to 3-state OFF during "hold acknowledge". During the first clock cycle after RESET becomes active, these signals are active HIGH. After this first clock, they float to 3-state OFF.
$\overline{RQ}/\overline{GT0}$ $\overline{RQ}/\overline{GT1}$	31 30	I/O I/O	REQUEST/GRANT: pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with $\overline{RQ}/\overline{GT0}$ having higher priority than $\overline{RQ}/\overline{GT1}$. $\overline{RQ}/\overline{GT}$ has an internal pull-up resistor so may be left unconnected. The request/grant sequence is as follows (See page 28): 1. A pulse of one CLK wide from another local bus master indicates a local bus request ("hold") to the SAB 8088 (pulse 1). 2. During a T4 or T1 clock cycle, a pulse one clock wide from the SAB 8088 to the requesting master (pulse 2), indicates that the SAB 8088 has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". The same rules as for HOLD/HOLDA apply as for when the bus is released. 3. A pulse one CLK wide from the requesting master indicates to the SAB 8088 (pulse 3) that the "hold" request is about to end and that the SAB 8088 can reclaim the local bus at the next CLK. The CPU then enters T4. Each master-master exchange of the local bus is a sequence of three pulses. There must be one idle CLK cycle after each bus exchange. Pulses are active LOW.

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

Pin Definitions and Functions (continued)

<table>
<tr><th>Symbol</th><th>Number</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td></td><td></td><td></td><td>If the request is made while the CPU is performing a memory cycle, it will release the local bus during T4 of the cycle when all the following conditions are met:
1. Request occurs on or before T2.
2. Current cycle is not the low byte of a word.
3. Current cycle is not the first acknowledge of an interrupt acknowledge sequence.
4. A locked instruction is not currently executing.
If the local bus is idle when the request is made the two possible events will follow:
1. Local bus will be released during the next clock.
2. A memory cycle will start within 3 clocks. Now the four rules for a currently active memory cycle apply with condition number 1 already satisfied.</td></tr>
<tr><td>$\overline{\text{LOCK}}$</td><td>29</td><td>O</td><td>$\overline{\text{LOCK}}$: indicates that other system bus masters are not to gain control of the system bus while $\overline{\text{LOCK}}$ is active (LOW). The $\overline{\text{LOCK}}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state off in "hold acknowledge".</td></tr>
<tr><td>QS1, QS0</td><td>24, 25</td><td>O</td><td>QUEUE STATUS: provide status to allow external tracking of the internal SAB 8088 instruction queue.
The queue status is valid during the CLK cycle after which the queue operation is performed.
<table><tr><th>QS1</th><th>QS0</th><th>Characteristics</th></tr><tr><td>0</td><td>0</td><td>No operation</td></tr><tr><td>0</td><td>1</td><td>First Byte of opcode from queue</td></tr><tr><td>1</td><td>0</td><td>Empty the queue</td></tr><tr><td>1</td><td>1</td><td>Subsequent byte from queue</td></tr></table></td></tr>
<tr><td>–</td><td>34</td><td>O</td><td>Pin 34 is always high in the maximum mode.</td></tr>
</table>

Block Diagram



Functional Description

Memory Organization

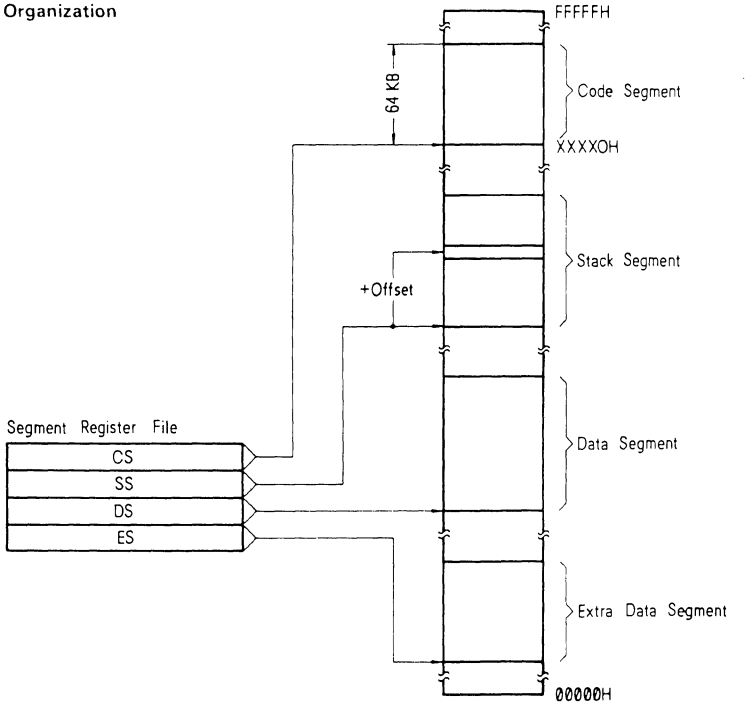
The processor provides a 20-bit address to memory which locates the byte being referenced. The memory is organized as a linear array of up to 1 million bytes, addressed as 00000(H) to FFFFF(H). The memory is logically divided into code, data, extra data, and stack segments of up to 64 Kbytes each, with each segment falling on 16-byte boundaries.

All memory references are made relative to base addresses contained in high speed segment registers. The segment types were chosen based on the addressing needs of programs. The segment register to be selected is automatically chosen according to the rules of the following table. All information in one segment type share the same logical attributes (e.g. code or data). By structuring memory into relocatable areas of similar characteristics and by automatically selecting segment registers, programs are shorter, faster, and more structured.

Word (16-bit) operands can be located on even or odd address boundaries. For address and data operands, the least significant byte of the word is stored in the lower valued address location and the most significant byte in the next higher address location. The BIU will automatically execute two fetch or write cycles for 16-bit operands.

Certain locations in memory are reserved for specific CPU operations. Locations from addresses FFFF0H trough FFFFFH are reserved for operations including a jump to the initial system initialization routine. Following RESET, the CPU will always begin execution at location FFFF0H where the jump must be located. Locations 00000H through 003FFH are reserved for interrupt operations. Four-byte pointers consisting of a 16-bit segment address and a 16-bit offset address direct program flow to one of the 256 possible interrupt service routines. The pointer elements are assumed to have been stored at their respective places in reserved memory prior to the occurrence of interrupts.

Memory Organization



Minimum and Maximum Modes

The requirements for supporting minimum and maximum SAB 8088 systems are sufficiently different that they cannot be done efficiently with 40 uniquely defined pins. Consequently, the SAB 8088 is equipped with a strap pin (MN/$\overline{MX}$) which defines the system configuration. The definition of a certain subset of the pins changes, dependent on the condition of the strap pin. When the MN/$\overline{MX}$ pin is strapped to GND, the SAB 8088 defines pins 24 through 31 and 34 in maximum mode. When the MN/$\overline{MX}$ pin is strapped to VCC, the SAB 8088 generates bus control signals itself on pins 24 through 31 and 34.

The minimum mode SAB 8088 can be used with either a multiplexed or demultiplexed bus. The multiplexed bus configuration is compatible with the SAB 8085A multiplexed bus peripherals (e.g. SAB 8155) and provides the user with a minimum chip count system. This architecture provides the 8088 processing power in a highly integrated form.

The demultiplexed mode requires one latch (for 64K addressability) or two latches (for a full megabyte of addressing). A third latch can be used for buffering if the address bus loading requires it An SAB 8286/8286A or SAB 8287/8287A transceiver can also be used if data bus buffering is required. The SAB 8088 provides $\overline{DEN}$ and DT/$\overline{R}$ to control the transceiver, and ALE to latch the addresses. This configuration of the minimum mode provides the standard demultiplexed bus structure with heavy bus buffering and relaxed bus timing requirements.

The maximum mode employs the SAB 8288/8288A bus controller. The SAB 8288/8288A decodes status lines $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$, and provides the system with all bus control signals. Moving the bus control to the SAB 8288/8288A provides better source and sink current capability to the control lines, and frees the SAB 8088 pins for extended large system features. Hardware lock, queue status, and two request/grant interfaces are provided by the SAB 8088 in maximum mode. These features allow co-processors in local bus and remote bus configurations.

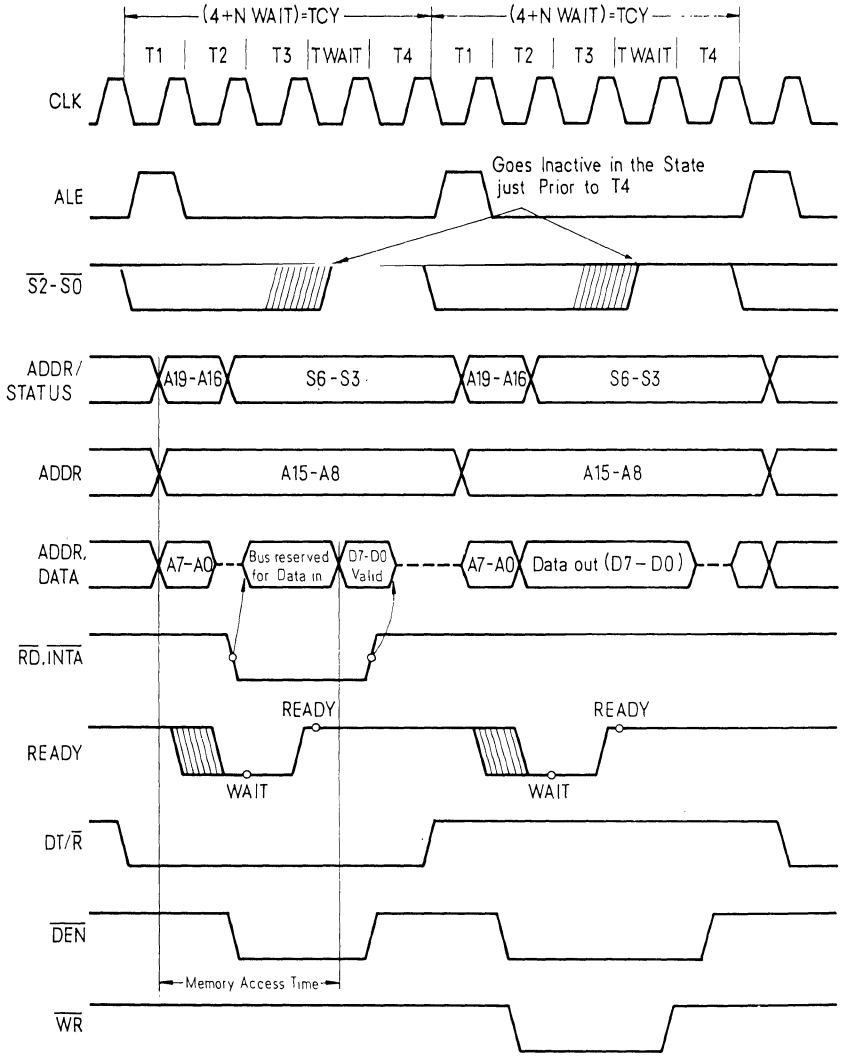
Bus Operation

The SAB 8088 address/data bus is broken into three parts – the lower eight address/data bits (AD0–AD7), the midle eight address bits (A8–A15), and the upper four address bits (A16–A19). The address/data bits and the highest four address bits are time multiplexed. This technique provides the most efficient use of pins on the processor, permitting the use of a standard 40 lead package. The middle eight address bits are not multiplexed, i.e. they remain valid through hout each bus cycle. In addition, the bus can be demultiplexed at the processor with a single address latch if a standard, non-multiplexed bus is desired for the system.

Each processor bus cycle consists of at least four CLK cycles. These are referred to as T1, T2, T3 and T4. The address is emitted from the processor during T1 and data transfer occurs on the bus during T3 and T4. T2 is used primarily for changing the direction of the bus during read operations. In the event that a "NOT READY" indication is given by the addressed device, "wait" states (Tw) are inserted between T3 and T4. Each inserted "wait" state is of the same duration as a CLK cycle. Periods can occur between SAB 8088 driven bus cycles. These are referred to as "idle" states (Ti), or inactive CLK cycles. The processor uses these cycles for internal housekeeping.

During T1 of any bus cycle, the ALE (address latch enable) signal is emitted (by either the processor or the SAB 8288/8288A bus controller, depending on the MN/$\overline{MX}$ strap). At the trailing edge of this pulse, a valid address and certain status information for the cycle may be latched.

Basic System Timing



Status bits $\overline{S0}$, $\overline{S1}$, and $\overline{S2}$ are used by the bus controller, in maximum mode, to identify the type of bus transaction according to the following table:

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Characteristics
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1 (HIGH)	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

Status bits S3 through S6 are multiplexed with high-order address bits and are therefore valid during T2 through T4. S3 and S4 indicate which segment register was used for this bus cycle in forming the address according to the following table:

S4	S3	Characteristics
0 (LOW)	0	Alternate Data (extra segment)
0	1	Stack
1 (HIGH)	0	Code or None
1	1	Data

S5 is a reflection of the PSW interrupt enable bit. S6 is always equal to 0.

I/O Addressing

In the SAB 8088, I/O operations can address up to a maximum of 64 K I/O registers. The I/O address appears in the same format as the memory address on bus lines A15–A0. The address lines A19–A16 are zero in I/O operations. The variable I/O instructions, which use register DX as a pointer have full address capability, while the direct I/O instructions directly address one or two of the 256 I/O byte locations in page 0 of the I/O address space. I/O ports are addressed in the same manner as memory locations.

Designers familiar with the SAB 8085 or upgrading an SAB 8085 design should note that the SAB 8085 addresses I/O with an 8-bit address on both halves of the 16-bit address bus. The SAB 8088 uses a full 16-bit address on its lower 16 address lines.

System Components

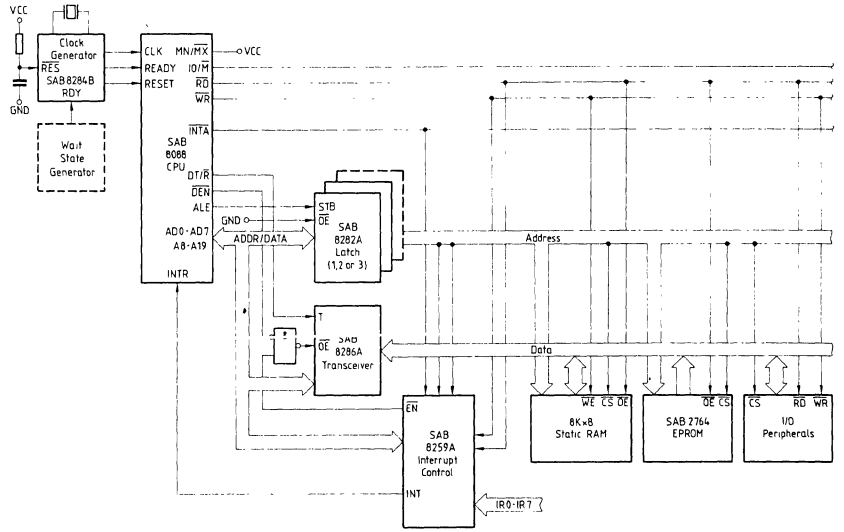
Support Circuits

SAB 8282/8282A Octal Latch
SAB 8283/8283A Octal Latch (Inverting)
SAB 8284A/8284B Clock Generator and Driver
SAB 8286/8286A Octal Bus Transceiver
SAB 8287/8287A Octal Bus Transceiver (Inverting)
SAB 8288/8288A Bus Controller
SAB 8289 Bus Arbiter
SAB 8259A Programmable Interrupt Controller

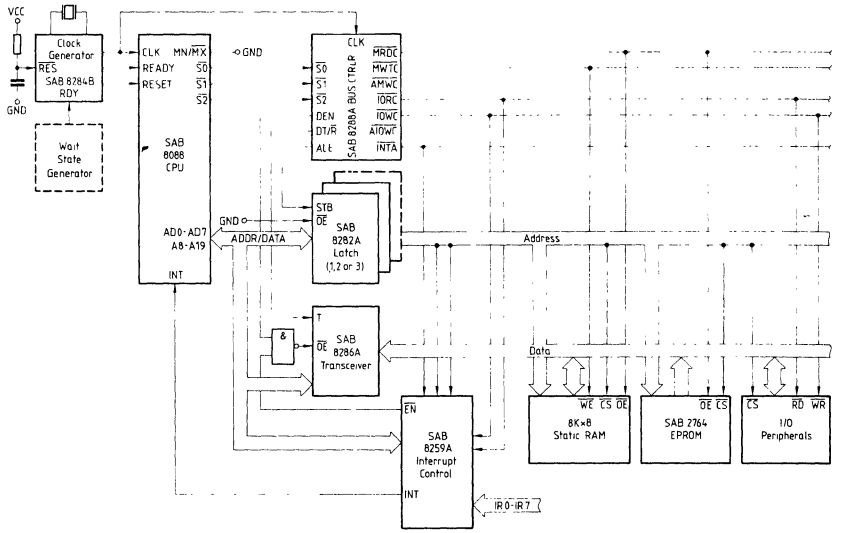
Typical Applications

The SAB 8088 is a general purpose 8-bit microprocessor which can be used for applications ranging from process control to data processing. On page 12 are shown typical system configurations for SAB 8088 familiy components.

Minimum Mode SAB 8088 Typical System Configuration



Maximum Mode SAB 8088 Typical System Configuration



DATA TRANSFER

MOV = Move

	76543210	76543210	76543210	76543210
Register / memory to / from register	100010dw	mod reg r/m		
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w=1
Immediate to register	1011w reg	data	data if w=1	
Memory to accumulator	1010000w	addr-low	addr-high	
Accumulator to memory	1010001w	addr-low	addr-high	
Register/memory to segment register	10001110	mod 0 reg r/m		
Segment register to register/memory	10001100	mod 0 reg r/m		

PUSH = Push:

Register/memory	11111111	mod 110 r/m		
Register	01010 reg			
Segment register	000 reg 110			

POP = Pop:

Register/memory	10001111	mod 000 r/m		
Register	01011 reg			
Segment register	000 reg 111			

XCHG = Exchange:

Register/memory with register	1000011w	mod reg r/m		
Register with accumulator	10010 reg			

IN = Input from:

Fixed port	1110010w	port		
Variable port	1110110w			

OUT = Output to:

	76543210	76543210	76543210	76543210
Fixed port	1110011w	port		
Variable port	1110111w			
XLAT = Translate byte to AL	11010111			
LEA = Load EA to register	10001101	mod reg r/m		
LDS = Load pointer to DS	11000101	mod reg r/m		
LES = Load pointer to ES	11000100	mod reg r/m		
LAHF = Load AH with flags	10011111			
SAHF = Store AH into flags	10011110			
PUSHF = Push flags	10011100			
POPF = Pop flags	10011101			

ARITHMETIC

ADD = Add.

Reg /memory with register to either	000000dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w = 01
Immediate to accumulator	0000010w	data	data if w = 1	

ADC = Add with carry

Reg /memory with register to either	000100dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w = 01
Immediate to accumulator	0001010w	data	data if w = 1	

INC = Increment.

Register/memory	1111111w	mod 000 r/m		
Register	01000 reg			
AAA = ASCII adjust for add	00110111			
DAA = Decimal adjust for add	00100111			

SUB = Subtract:

	76543210	76543210	76543210	76543210
Reg /memory and register to either	001010dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s:w=01
Immediate from accumulator	0010110w	data	data if w=1	

SBB = Subtract with borrow

Reg /memory and register to either	000110dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s:w=01
Immediate from accumulator	0001110w	data	data if w=1	

DEC = Decrement:

	76543210	76543210	76543210	76543210
Register/memory	1111111w	mod 001 r/m		
Register	01001reg			
NEG = Change sign	1111011w	mod 011 r/m		

CMP = Compare:

Register/memory and register	001110dw	mod reg r/m		
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s:w=01
Immediate with accumulator	0011110w	data	data if w=1	
AAS = ASCII adjust for subtract	00111111			
DAS = Decimal adjust for subtract	00101111			
MUL = Multiply (unsigned)	1111011w	mod 100 r/m		
IMUL = Integer multiply (signed)	1111011w	mod 101 r/m		
AAM = ASCII adjust for multiply	11010100	00001010		
DIV = Divide (unsigned)	1111011w	mod 110 r/m		
IDIV = Integer divide (signed)	1111011w	mod 111 r/m		
AAD = ASCII adjust for divide	11010101	00001010		
CBW = Convert byte to word	10011000			
CWD = Convert word to double word	10011001			

LOGIC

	76543210	76543210	76543210	76543210
NOT = Invert	1111011w	mod 010 r/m		
SHL/SAL = Shift logical/arithmetic left	110100vw	mod 100 r/m		
SHR = Shift logical right	110100vw	mod 101 r/m		
SAR = Shift arithmetic right	110100vw	mod 111 r/m		
ROL = Rotate left	110100vw	mod 000 r/m		
ROR = Rotate right	110100vw	mod 001 r/m		
RCL = Rotate through carry flag left	110100vw	mod 010 r/m		
RCR = Rotate through carry right	110100vw	mod 011 r/m		

AND = And:

Reg/memory and register to either	001000dw	mod reg r/m		
Immediate to register/memory	1000000w	mod 100 r/m	data	data if w 1
Immediate to accumulator	0010010w	data	data if w 1	

TEST = And function to flags, no result

Register/memory and register	1000010w	mod reg r/m		
Immediate data and register/memory	1111011w	mod 000 r/m	data	data if w 1
Immediate data and accumulator	1010100w	data	data if w 1	

OR = Or:

Reg/memory and register to either	000010dw	mod reg r/m		
Immediate to register/memory	1000000w	mod 001 r/m	data	data if w=1
Immediate to accumulator	0000110w	data	data if w=1	

XOR = Exclusive or:

Reg /memory and register to either	001100dw	mod reg r/m		
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w=1
Immediate to accumulator	0011010w	data	data if w=1	

STRING MANIPULATION	76543210	76543210	76543210
REP Repeat	1111001z		
MOVS Move byte/word	1010010w		
CMPS Compare byte/word	1010011w		
SCAS Scan byte/word	1010111w		
LODS Load byte/word to AL/AX	1010110w		
STOS Store byte/word from AL/A	1010101w		

CONTROL TRANSFER

CALL Call

Direct within segment	11101000	disp-low	disp-high
Indirect within segment	11111111	mod 010 r/m	
Direct intersegment	10011010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 011 r/m	

JMP Unconditional Jump.

Direct within segment	11101001	disp-low	disp-high
Direct within segment short	11101011	disp	
Indirect within segment	11111111	mod 100 r/m	
Direct intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	11111111	mod 101 r/m	

RET Return from CALL.	76543210	76543210	76543210
Within segment	11000011		
Within seg adding immed to SP	11000010	data-low	data high
Intersegment	11001011		
Intersegment adding immediable to SP	11001010	data-low	data high
JE/JZ - Jump on equal/zero	01110100	disp	
JL/JNGE - Jump on less/not greater or equal	01111100	disp	
JLE/JNG - Jump on less or equal/not greater	01111110	disp	
JB/JNAE - Jump on below/not above or equal	01110010	disp	
JBE/JNA - Jump on below or equal/ not above	01110110	disp	
JP/JPE - Jump on parity/parity even	01111010	disp	
JO - Jump on overflow	01110000	disp	
JS - Jump on sign	01111000	disp	
JNE/JNZ - Jump on not equal/not zero	01110101	disp	
JNL/JGE = Jump on not less/greater or equal	01111101	disp	
JNLE/JG = Jump on not less or equal/ greater	01111111	disp	
JNB/JAE = Jump on not below/above or equal	01110011	disp	
JNBE/JA = Jump on not below or equal/above	01110111	disp	
JNP/JPO = Jump on not par/par odd	01111011	disp	
JNO = Jump on not overflow	01110001	disp	
JNS = Jump on not sign	01111001	disp	
LOOP = Loop CX times	11100010	disp	
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp	
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp	
JCXZ = Jump on CX zero	11100011	disp	

INT Interrupt	76543210	76543210
Type specified	11001101	type
Type 3	11001100	
INTO Interrupt on overflow	11001110	
IRET Interrupt return	11001111	

PROCESSOR CONTROL

CLC Clear carry	11111000	
CMC Complement carry	11110101	
STC Set Carry	11111001	
CLD Clear direction	11111100	
STD Set direction	11111101	
CLI Clear interrupt	11111010	
STI Set interrupt	11111011	
HLT Halt	11110100	
WAIT Wait	10011011	
ESC Escape (to external device)	11011xxx	mod x x x r/m
LOCK Bus lock prefix	11110000	

Footnotes:

AL 8-bit accumulator
AX 16-bit accumulator
CX Count register
DS Data segment
ES Extra segment
Above/below refers to unsigned value
Greater more positive,
Less less positive (more negative) signed values
if d 1 then "to" reg, if d 0 then "from" reg
if w 1 then word instruction, if w 0 then byte instruction

if mod 11 then r/m is treated as a REG field
if mod 00 then DISP 0*, disp-low and disp-high are absent
if mod 01 then DISP disp-low sign-extended to 16-bits, disp high is absent
if mod 10 then DISP disp-high disp low
if r/m 000 then EA (BX) + (SI) + DISP
if r/m 001 then EA (BX) + (DI) + DISP
if r/m 010 then EA (BP) + (SI) + DISP
if r/m 011 then EA (BP) + (DI) + DISP
if r/m 100 then EA (SI) + DISP
if r/m 101 then EA (DI) + DISP
if r/m 110 then EA (BP) + DISP*
if r/m 111 then EA (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod 00 and r/m 110 then EA disp-high disp-low

if s w 01 then 16-bits of immediate data from the operand
if s:w 11 then an immediate data byte is sign extended to form the 16-bit operand
if v 0 then "count" 1, if v 1 then "count" in (CL)
x don't care
z is used for string primitives for comparsion with ZF FLAG

SEGMENT OVERRIDE PREFIX

001 reg 110

REG is assigned according to the following table

16-Bit (w 1)	8-Bit (w 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instruction which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file

FLAGS X X X X (OF) (DF) (IF) (TF) (SF) (ZF) X (AF) X (PF) X (CF)

Absolute Maximum Ratings *)

Ambient Temperature Under Bias	0 to 70 °C
Storage Temperature	−65 to +150 °C
Voltage on any Pin with Respect to Ground	−1.0 to +7 V
Power Dissipation	2.5 Watt

D.C. Characteristics

SAB 8088: T_A = 0 to 70 °C, V_{CC} = 5 V ± 10%
SAB 8088-2: T_A = 0 to 70 °C, V_{CC} = 5 V ± 5%

Symbol	Parameter	Limit Values		Unit	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	+0.8	V	–
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5		
V_{OL}	Output Low Voltage	–	0.45		I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4	–		I_{OH} = −400 µA
I_{CC}	Power Supply Current SAB 8088 SAB 8088-2	–	 340 350	 mA	 All outputs open T_A = 25 °C
I_{LI}	Input Leakage Current	–	±10	µA	0 V ≤ V_{IN} ≤ V_{CC}
I_{LO}	Output Leakage Current				0.45 V ≤ V_{OUT} ≤ V_{CC}
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	–
V_{CH}	Clock Input High Voltage	3.9	V_{CC}+1.0		
C_{IN}	Capacitance of Input Buffer (All input except AD0–AD7, $\overline{RQ}/\overline{GT}$)	–	15	pF	f_c = 1 MHz
C_{IO}	Capacitance of I/O Buffer (AD0–AD7, $\overline{RQ}/\overline{GT}$)				

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

SAB 8088: T_A = 0 to 70 C, V_{CC} = 5 V ± 10%
SAB 8088-2: T_A = 0 to 70 C, V_{CC} = 5 V ± 5%

Minimum Complexity System Timing Requirements

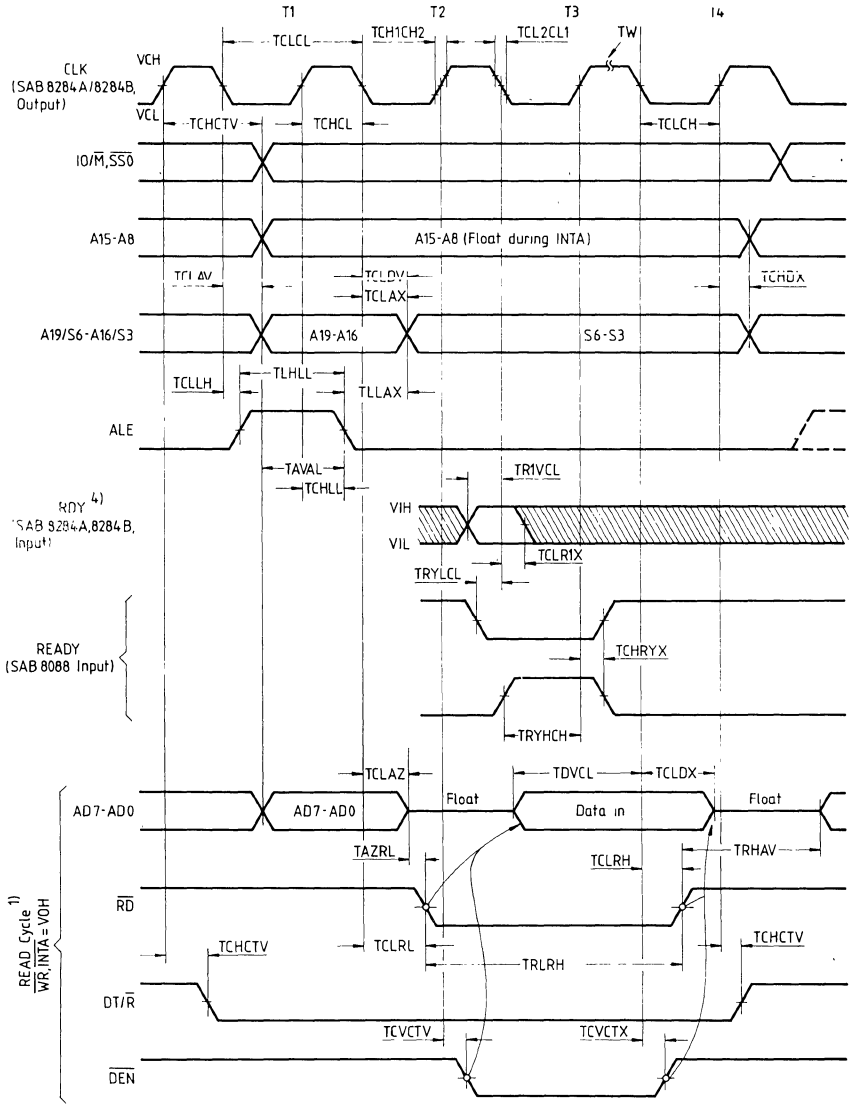
Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8088		SAB 8088-2			
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	125	500	ns	–
TCLCH	CLK Low Time	118	–	68	–		
TCHCL	CLK High Time	69		44			
TCH1CH2	CLK Rise Time	–	10	–	10		From 1.0 to 3.5V
TCL2CL1	CLK Fall Time						From 3.5 to 1.0V
TDVCL	Data in Setup Time	30	–	20	–		–
TCLDX	Data in Hold Time	10		10			
TR1VCL	RDY Setup Time into SAB 8284A/8284B [1] [2]	35		35			
TCLR1X	RDY Hold Time into SAB 8284A/8284B [1] [2]	0		0			
TRYHCH	READY Setup Time into SAB 8088	118		68			
TCHRYX	READY Hold Time into SAB 8088	30		20			
TRYLCL	READY Inactive to CLK [3]	−8		−8			
THVCH	HOLD Setup Time	35		20			
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time [2]	30		15			
TILIH	Input Rise Time (Except CLK)	–	20	–	20		From 0.8 to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12		From 2.0 to 0.8V

[1] Signal at SAB 8284A/8284B shown for reference only.
[2] Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3] Applies only to T2 state (8 ns into T3).

Timing Responses

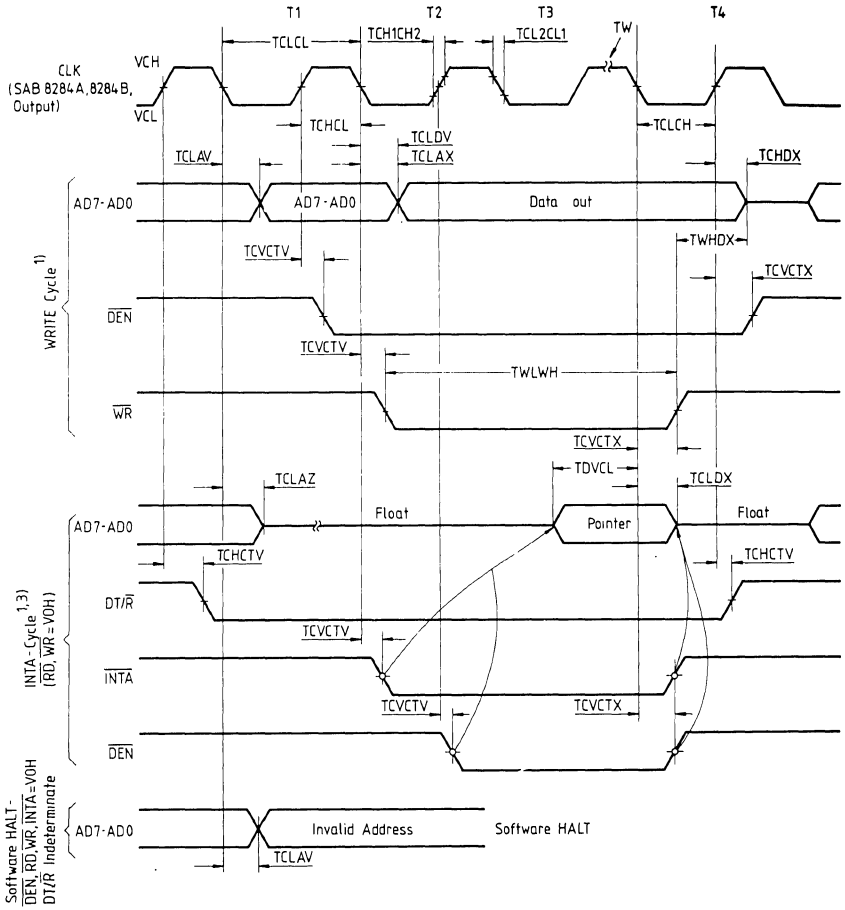
Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8088		SAB 8088-2			
		Min.	Max.	Min.	Max.		
TCLAV	Address Valid Delay	10	110	10	60	ns	C_L = 20 – 100 pF for all SAB 8088 Outputs in addition to the internal loads
TCLAX	Address Hold Time		–		–		
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50		
TLHLL	ALE Width	TCLCH – 20	–	TCLCH – 10	–		
TCLLH	ALE Active Delay	–	80	–	50		
TCHLL	ALE Inactive Delay		85		55		
TLLAX	Address Hold Time to ALE Inactive	TCHCL – 10	–	TCHCL – 10	–		
TCLDV	Data Valid Delay	10	110	10	60		
TCHDX	Data Hold Time		–		–		
TWHDX	Data Hold Time After $\overline{WR}$	TCLCH – 30		TCLCH – 30			
TCVCTV	Control Active Delay 1	10	110	10	70		
TCHCTV	Control Active Delay 2				60		
TCVCTX	Control Inactive Delay				70		
TAZRL	Address Float to READ Active	0	–	0	–		
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100		
TCLRH	$\overline{RD}$ Inactive Delay		150		80		
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL – 45	–	TCLCL – 40	–		
TCLHAV	HLDA Valid Delay	10	160	10	100		
TRLRH	$\overline{RD}$ Width	2TCLCL–75	–	2TCLCL – 50	–		
TWLWH	$\overline{WR}$ Width	2TCLCL – 60		2TCLCL – 40			
TAVAL	Address Valid to ALE Low	TCLCH – 60		TCLCH – 40			
TOLOH	Output Rise Time	–	20	–	20		From 0.8 to 2.0V
TOHOL	Output Fall Time		12		12		From 2.0 to 0.8V

Bus Timing – Minimum Mode System



Notes see next page

Bus Timing – Minimum Mode System (cont'd)



[1]) All signals switch between VOH and VOL unless otherwise specified.
[2]) RDY is sampled near the end of T2, T3, Tw to determine if Tw machines states are to be inserted.
[3]) Two INTA cycles run back to back. The SAB 8088 local ADDR/DATA Bus is floating during both INTA cycles. Control signals shown for second INTA cycle.
[4]) Signals at SAB 8284A/8284B are shown for reference only.
[5]) All timing measurements are made at 1.5V unless otherwise noted.

Max Mode System (Using SAB 8288/8288A Bus Controller)
Timing Requirements

Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8088		SAB 8088-2			
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	200	500	125	500	ns	–
TCLCH	CLK Low Time	118	–	68	–		
TCHCL	CLK High Time	69		44			
TCH1CH2	CLK Rise Time	–	10	–	10		From 1.0 to 3.5V
TCL2CL1	CLK Fall Time						From 3.5 to 1.0V
TDVCL	Data In Setup Time	30	–	20	–		–
TCLDX	Data In Hold Time	10		10			
TR1VCL	RDY Setup Time into SAB 8284A/8284B [1] [2]	35		35			
TCLR1X	RDY Hold Time into SAB 8284A/8284B [1] [2]	0		0			
TRYHCH	READY Setup Time into SAB 8088	118		68			
TCHRYX	READY Hold Time into SAB 8088	30		20			
TRYLCL	READY Inactive to CLK [3]	−8		−8			
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) [2]	30		15			
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time						
TCHGX	$\overline{RQ}$ Hold Time into SAB 8088	40		30			
TILIH	Input Rise Time (Except CLK)	–	20	–	20		From 0.8 to 2.0V
TIHIL	Input Fall Time (Except CLK)		12		12		From 2.0 to 0.8V

[1]) Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only.
[2]) Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
[3]) Applies only to T2 state (8 ns into T3).

Timing Responses

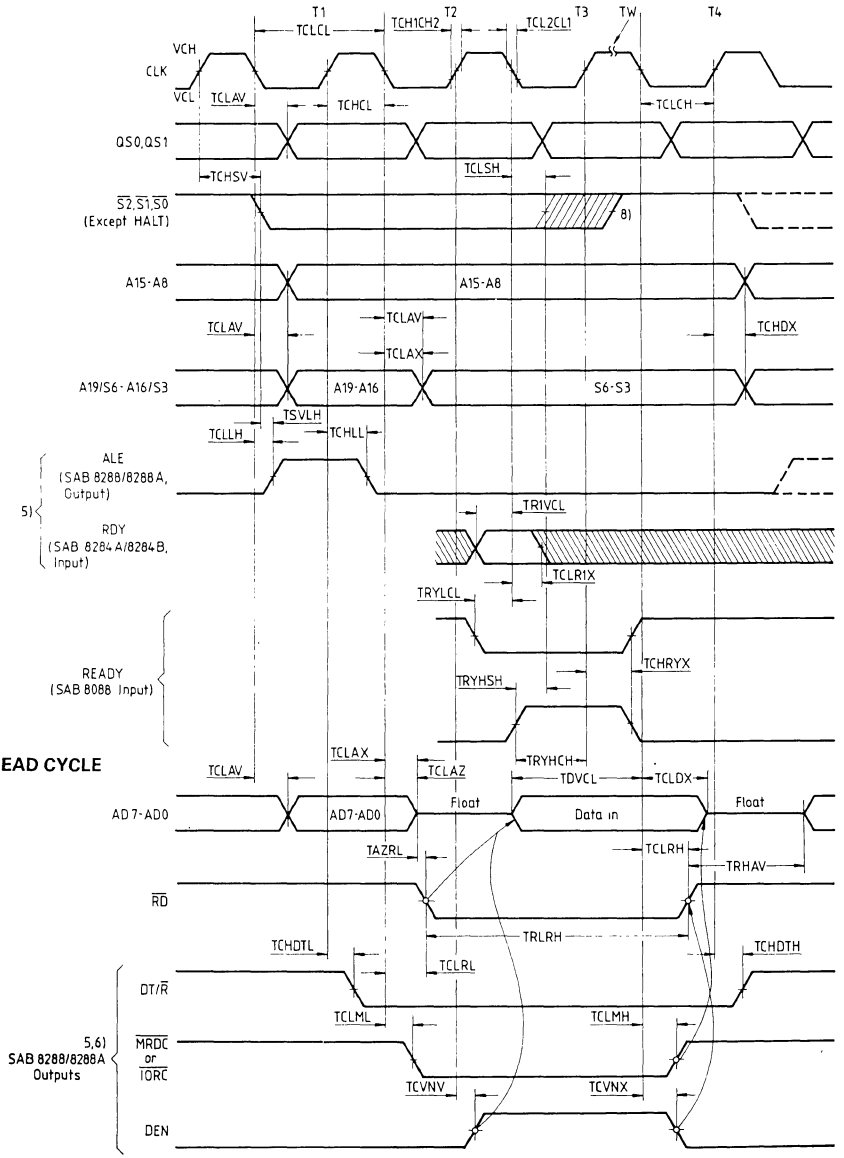
Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8088		SAB 8088-2			
		Min.	Max.	Min.	Max.		
TCLML	Command Active Delay [1]	10	35	10	35	ns	CL 20 100 pF for all SAB 8088 Outputs in addition to the internal loads
TCLMH	Command Inactive Delay [1]						
TRYHSH	READY Active to Status Passive [2]	–	110	–	65		
TCHSV	Status Active Delay	10		10	60		
TCLSH	Status Inactive Delay		130		70		
TCLAV	Address Valid Delay		110		60		
TCLAX	Address Hold Time		–		–		
TCLAZ	Address Float Delay	TCLAX	80	TCLAX	50		
TSVLH	Status Valid to ALE High [1]	–	20	–	20		
TSVMCH	Status Valid to MCE High [1]						
TCLLH	CLK Low to ALE Valid [1]						
TCLMCH	CLK Low to MCE High [1]						
TCHLL	ALE Inactive Delay [1]	4	15	4	15		
TCLDV	Data Valid Delay	10	110	10	60		
TCHDX	Data Hold Time		–		–		
TCVNV	Control Active Delay [1]	5	45	5	45		
TCVNX	Control Inactive Delay [1]	10		10			

[1] Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only.
[2] Applies only to T2 state (8 ns into T3).

Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8088		SAB 8088-2			
		Min.	Max.	Min.	Max.		
TAZRL	Address Float to READ Active	0	–	0	–		
TCLRL	$\overline{RD}$ Active Delay	10	165	10	100		CL = 20 - 100 pF for all SAB 8088 Outputs in addition to the internal loads
TCLRH	$\overline{RD}$ Inactive Delay		150		80		
TRHAV	$\overline{RD}$ Inactive to Next Address Active	TCLCL - 45	–	TCLCL - 40	–		
TCHDTL	Direction Control Active Delay [1])	–	50	–	50		
TCHDTH	Direction Control Inactive Delay [1])		30		30		
TCLGL	$\overline{GT}$ Active Delay		85		50		
TCLGH	$\overline{GT}$ Inactive Delay						
TRLRH	$\overline{RD}$ Width	2TCLCL - 75	–	2TCLCL - 50	–		
TOLOH	Output Rise Time	–	20	–	20		From 0.8 to 2.0V
TOHOL	Output Fall Time		12		12		From 2.0 to 0.8V

[1]) Signal at SAB 8284A/8284B or SAB 8288/8288A shown for reference only.

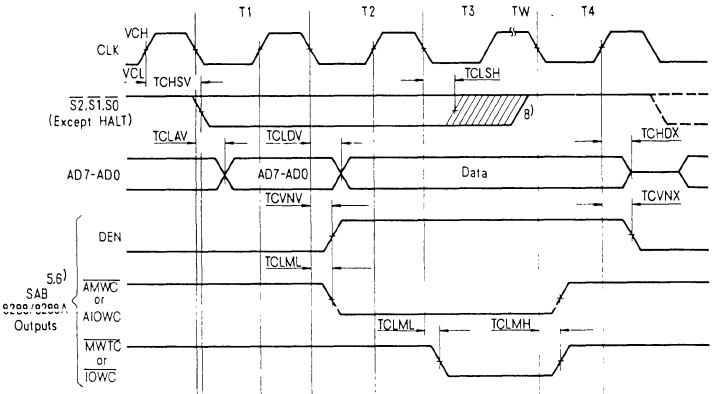
Bus Timing – Maximum Mode System (Using SAB 8288/8288A)



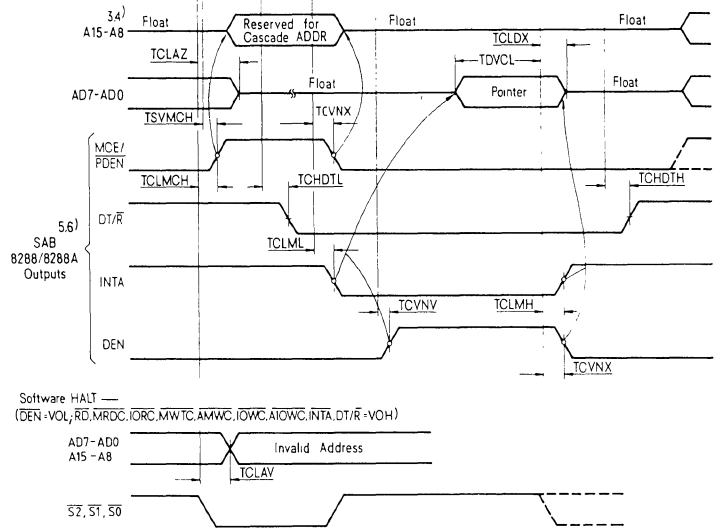
Notes see next page.

Bus Timing – Maximum Mode System (Using SAB 8288/8288A)

WRITE CYCLE

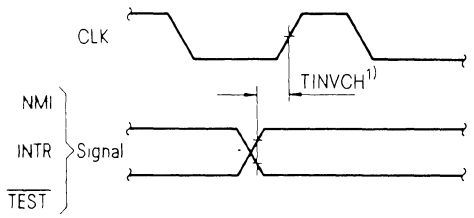


INTA CYCLE



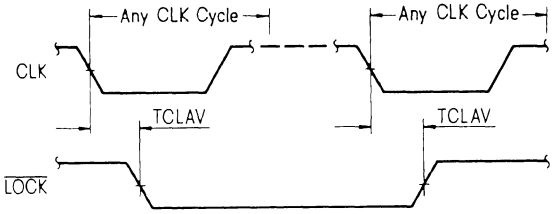
1) All Signals switch between VOH and VOL unless otherwise specified.
2) RDY is sampled near the end of T2, T3, Tw to determine if Tw machines states are to be inserted.
3) Cascade address is valid between first and second INTA cycle.
4) Two INTA cycles run back-to-back. The SAB 8088 local ADDR/DATA Bus is floating during both INTA cycles. Control for pointer address is shown for second INTA cycle.
5) Signals at SAB 8284A/8284B or SAB 8288/8288A are shown for reference only.
6) The issuance of the SAB 8288/8288A command and control signals (MRDC, MWTC, AMWC, IORC, IOWC, AIOWC, INTA and DEN) lags the active HIGH SAB 8288/8288A DEN.
7) All timing measurements are made at 1.5 V unless otherwise noted.
8) Status inactive in state just prior to T4.

Asynchronous Signal Recognition

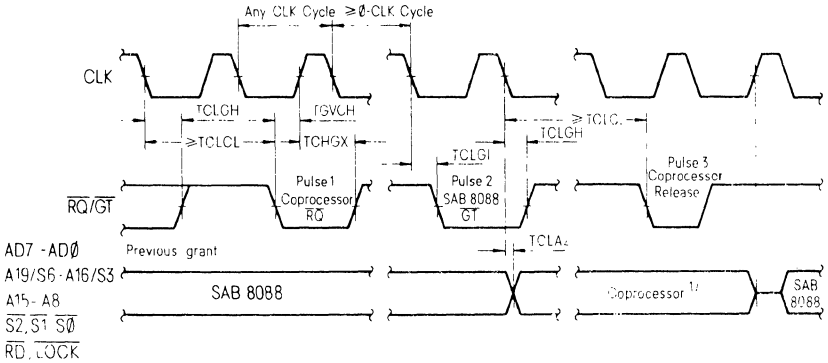


[1]) Setup requirements for asynchronous signals only to guarantee recognition at next CLK

Bus Lock Signal Timing (Maximum Mode Only)

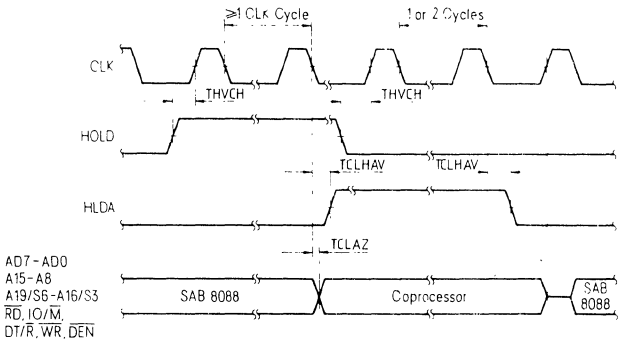


Request/Grant Sequence Timing (Maximum Mode Only)

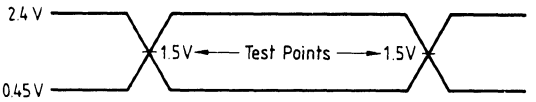


[1]) The coprocessor may not drive the buses outside the region shown without risking contention

Hold/Hold Acknowledge Timing (Minimum Mode Only)

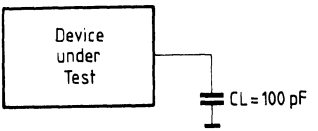


Input/Output Waveforms for A.C.-Tests



A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0" The clock is driven at 4.3V and 0.25V. Timing measurements are made at 1.5V for both a logic "1" and "0".

Load Circuit for A.C.-Tests

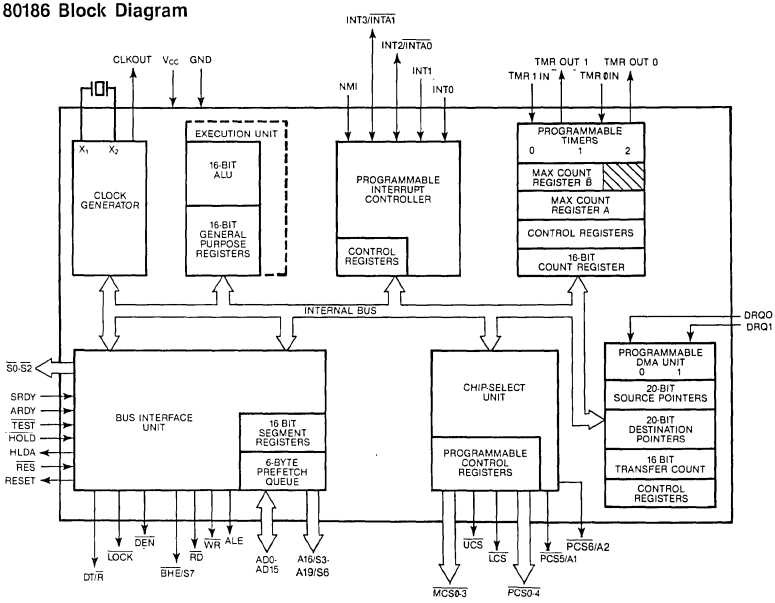


CL includes Jig Capacitance

SAB 80186
High Integration
16-Bit Microprocessor

- Integrated Feature Set
  - —Enhanced SAB 8086-2 CPU
  - —Clock Generator
  - —2 Independent, High-Speed DMA Channels
  - —Programmable Interrupt Controller
  - —3 Programmable 16-bit Timers
  - —Programmable Memory and Peripheral Chip-Select Logic
  - —Programmable Wait State Generator
  - —Local Bus Controller
- High Performance Processor
  - —2 Times the Performance of the Standard SAB 8086
  - —4 MByte/Sec Bus Bandwidth Interface
- Direct Addressing Capability to 1 MByte of Memory
- Completely Object Code Compatible with All Existing SAB 8086/8088 Software
  - —10 New Instruction Types
- Complete System Development Support
- Fully Compatible with Industry Standard 80186

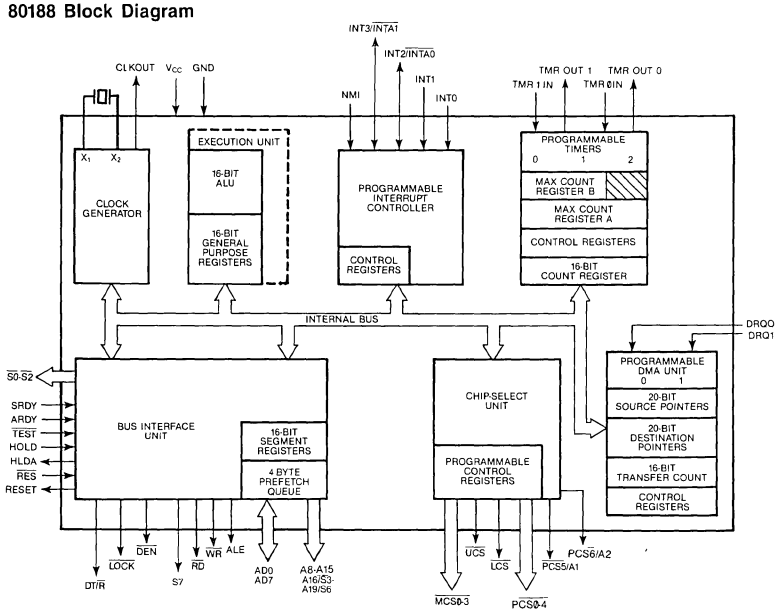
SAB 80186 Block Diagram



SAB 80188
High Integration
8-Bit Microprocessor

- Integrated Feature Set
  - —Enhanced SAB 8088-2 CPU
  - —Clock Generator
  - —2 Independent, High-Speed DMA Channels
  - —Programmable Interrupt Controller
  - —3 Programmable 16-bit Timers
  - —Programmable Memory and Peripheral Chip-Select Logic
  - —Programmable Wait State Generator
  - —Local Bus Controller
- 8-Bit Data Bus Interface; 16-Bit Internal architecture
- High Performance 8 MHz Processor
  - —2 Times the Performance of the Standard SAB 8088
  - —2 MByte/Sec Bus Bandwidth Interface
- Completely Object Code Compatible with All Existing SAB 8086/8088 Software
  - —10 New Instruction Types
- Direct Addressing Capability to 1 MByte of Memory
- Complete System Development Support
- Fully Compatible with Industry Standard 80188

SAB 80188 Block Diagram

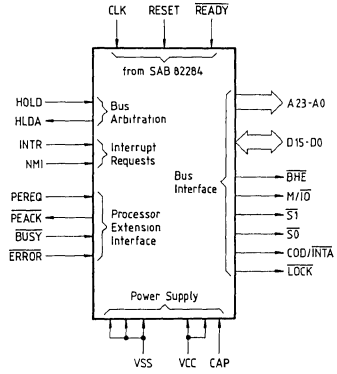


Advance Information

SAB 80286
High Performance Microprocessor with Memory Management and Protection

- High-Performance Processor (up to Six Times the SAB 8086)
- Large Address Space:
  - 16 Megabytes Physical
  - 1 Gigabyte Virtual per Task
- Integrated Memory Management, Four-Level Memory Protection and Support for Virtual Memory and Operating Systems
- Two SAB 8086 Upward-Compatible Operating Modes:
  - SAB 8086 Real Address Mode
  - Protected Virtual Address Mode
- High Bandwidth Bus Interface (8 Megabyte/s)
- Full Hardware and Software Support

Logic Symbol



Pin Names

A23-A0	Address Bus	HOLD	Bus Hold Request
D15-D0	Data Bus	HLDA	Bus Hold Acknowledge
$\overline{S1}$, $\overline{S0}$	Bus Cycle Status	INTR	Interrupt Request
$\overline{BHE}$	Bus High Enable	NMI	Non-Maskable Interrupt Request
M/$\overline{IO}$	Memory/IO Select	PEREQ	Processor Extension Operand Request
COD/$\overline{INTA}$	Code/Interrupt Acknowledge		
$\overline{LOCK}$	Bus Lock	$\overline{PEACK}$	Processor Extension Operand Acknowledge
CLK	System Clock		
RESET	System Reset	$\overline{BUSY}$	Processor Extension Busy
READY	Bus Ready	$\overline{ERROR}$	Processor Extension Error
CAP	Substrate Filter Capacitor	VCC	Power supply (+5V)
		VSS	Ground (0 V)

The SAB 80286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multitasking systems. The SAB 80286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. An 8 MHz SAB 80286 provides up to six times greater throughput than the standard 5 MHz SAB 8086. The SAB 80286 includes memory management capabilities that map up to 2^{30} (one gigabyte) of virtual address space per task into 2^{24} bytes (16 megabytes) of physical memory.

The SAB 80286 is upward-compatible with SAB 8086/8088 software. Using SAB 8086 real address mode, the SAB 80286 is object codecompatible with existing SAB 8086/8088 software. In protected virtual address mode, the SAB 80286 is source code-compatible with SAB 8086/8088 software and may require upgrading to use virtual addresses supported by SAB 80286's integrated memory management and protection mechanism. Both modes operate at full SAB 80286 performance and execute a superset of the SAB 8086/8088 instructions.

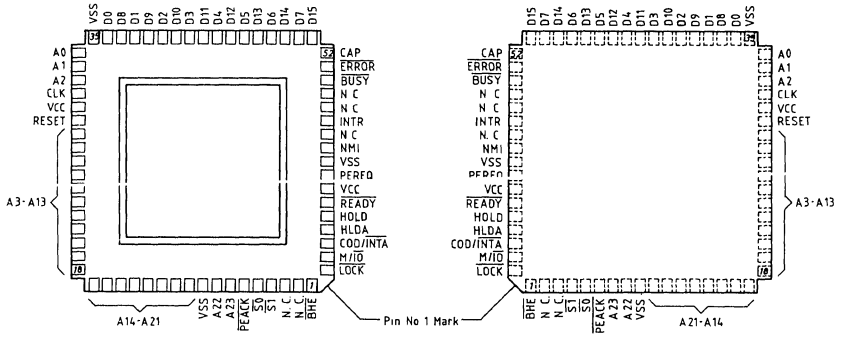
The SAB 80286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The SAB 80286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

Pin Configuration

LCC package

Component pad view – as viewed from underside of component when mounted on the board.

PC board view – as viewed from the component side of the pc board.

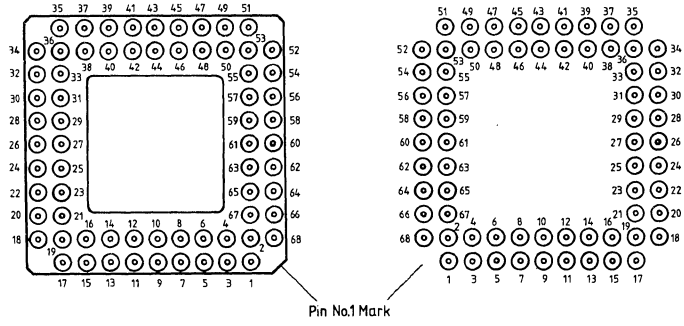


Note: N.C. Pads must not be connected.

Pin grid array package

Bottom view

Top view



Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
$\overline{BHE}$	1	O	BUS HIGH ENABLE indicates transfer of data on the upper byte of the data bus D15-8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active LOW and floats to Tri-state OFF during bus hold acknowledge.

$\overline{BHE}$ and A0 encodings

$\overline{BHE}$ value	A0 value	Function
0	0	Word transfer
0	1	Byte transfer on upper half of data bus (D15-8)
1	0	Byte transfer on lower half of data bus (D7-0)
1	1	Reserved

$\overline{S1}$, $\overline{S0}$	4, 5	O	BUS CYCLE STATUS indicates initiation of a bus cycle and, along with M/$\overline{IO}$ and COD/$\overline{INTA}$, defines the type of bus cycle. The bus is in a Ts state whenever one or both are LOW, $\overline{S1}$ and $\overline{S0}$ are active LOW and float to Tri-state OFF during bus hold acknowledge.

Bus cycle status definition

COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S1}$	$\overline{S0}$	Bus cycle initiated
0 (LOW)	0	0	0	Interrupt acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	None; not a status cycle
0	1	0	0	IF A1 = 1 then halt; else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None; not a status cycle
1 (HIGH)	0	0	0	Reserved
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	None; not a status cycle
1	1	0	0	Reserved
1	1	0	1	Memory instruction read
1	1	1	0	Reserved
1	1	1	1	None; not a status cycle

PEREQ $\overline{PEACK}$	6	I O	PROCESSOR EXTENSION OPERAND REQUEST AND ACKNOWLEDGE extend the memory management and protection capabilities of the SAB 80286 to processor extensions. The PEREQ input requests the SAB 80286 to perform a data operand transfer for a processor extension. The $\overline{PEACK}$ output signals the processor extension when the requested operand is being transferred. PEREQ is active HIGH and floats to Tri-state OFF during bus hold acknowledge. $\overline{PEACK}$ may be asynchronous to the system clock. $\overline{PEACK}$ is active LOW.

Pin Definitions and Functions (continued)

<table>
<tr><th>Symbol</th><th>Number</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>A23–A0</td><td>7 – 34</td><td>O</td><td>ADDRESS BUS outputs physical memory and I/O port addresses. A0 is LOW when data is to be transferred on pins D7–0. A23–A10 are LOW during I/O transfers. The address bus is active HIGH and floats to Tri-state OFF during bus hold acknowledge.</td></tr>
<tr><td>RESET</td><td>29</td><td>I</td><td>SYSTEM RESET clears the internal logic of the SAB 80286 and is active HIGH. The SAB 80286 may be reinitialized at any time a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the SAB 80286 enter the state shown below:
<table><tr><th colspan="2">Pin state during reset</th></tr><tr><th>Pin value</th><th>Pin names</th></tr><tr><td>1 (HIGH)</td><td>$\overline{S0}$, $\overline{S1}$, $\overline{PEACK}$, A23–A0, $\overline{BHE}$, $\overline{LOCK}$</td></tr><tr><td>0 (LOW)</td><td>M/$\overline{IO}$, COD/$\overline{INTA}$, $\overline{HLDA}$</td></tr><tr><td>Tri-state OFF</td><td>D15 – D0</td></tr></table>Operation of the SAB 80286 begins after a HIGH to LOW transition on RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the SAB 80286 for internal initializations before performing the first bus cycle to fetch code from the power-on execution address.
A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the system clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase-synchronous to another clock.</td></tr>
<tr><td>CLK</td><td>31</td><td>I</td><td>SYSTEM CLOCK provides the fundamental timing for SAB 80286 systems. It is divided by two (inside the SAB 80286) to generate the processor clock. The internal divide-by-two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.</td></tr>
<tr><td>D15 – D0</td><td>36 – 51</td><td>I
O</td><td>DATA BUS inputs data during memory, I/O, and interrupt acknowledge read cycles: outputs data during memory and I/O write cycles. The data bus is active HIGH and floats to Tri-state OFF during bus hold acknowledge.</td></tr>
<tr><td>$\overline{BUSY}$
$\overline{ERROR}$</td><td>53, 54</td><td>I
I</td><td>PROCESSOR EXTENSION BUSY AND ERROR indicate the operating condition of a processor extension to the SAB 80286. An active $\overline{BUSY}$ input stops the SAB 80286 program execution on WAIT and some ESC instructions until $\overline{BUSY}$ becomes inactive (HIGH). The SAB 80286 may be interrupt while waiting for $\overline{BUSY}$ to become inactive. An active $\overline{ERROR}$ input causes the SAB 80286 to perform a processor extension interrupted when executing WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock.</td></tr>
</table>

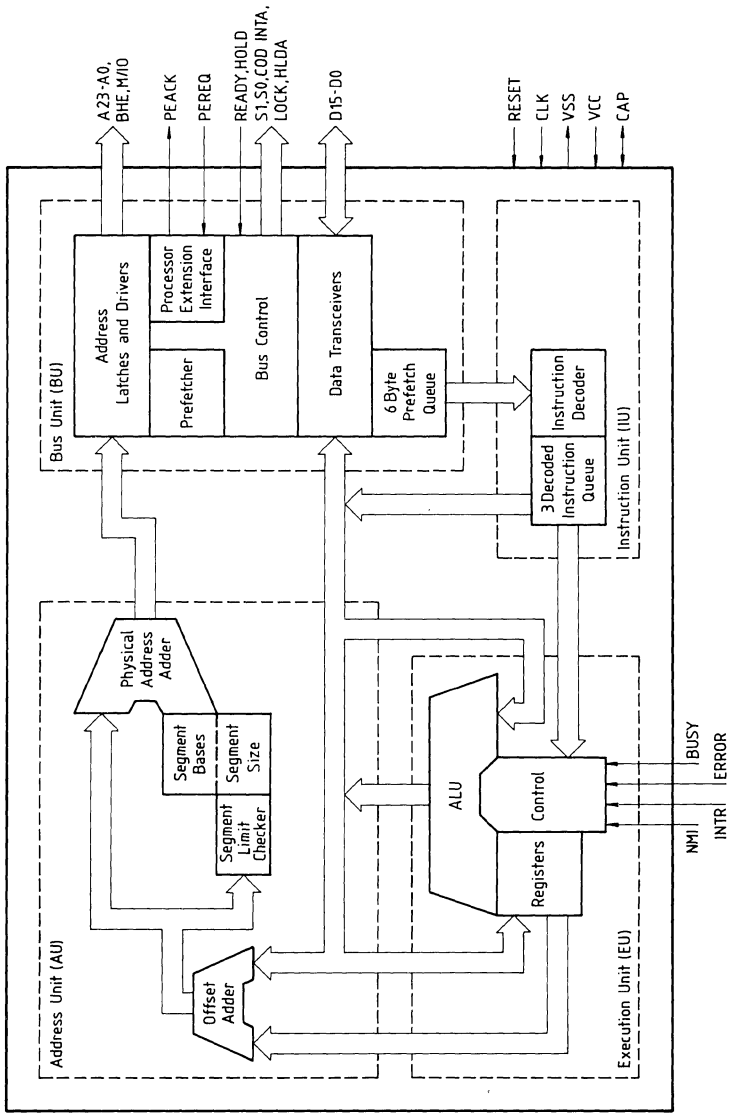
Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
INTR	57	I	INTERRUPT REQUEST requests the SAB 80286 to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the SAB 80286 responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active HIGH, and may be asynchronous to the system clock.
NMI	59	I	NON-MASKABLE INTERRUPT REQUEST interrupts the SAB 80286 with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the SAB 80286 flag word does not affect this input. The NMI input is active HIGH, may be asynchronous to the system clock, and is edge-triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles and remain HIGH for at least four system clock cycles.
$\overline{\text{READY}}$	63	I	BUS READY terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{\text{READY}}$ LOW. $\overline{\text{READY}}$ is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{\text{READY}}$ is ignored during bus hold acknowledge.
HOLD HLDA	64 65	I O	BUS HOLD REQUEST AND HOLD ACKNOWLEDGE control ownership of the SAB 80286 local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the SAB 80286 will float its bus drivers to Tri-state OFF and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the SAB 80286 deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition, HOLD may be asynchronous to the system clock. These signals are active HIGH.
COD/$\overline{\text{INTA}}$	66	O	CODE/INTERRUPT ACKNOWLEDGE distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{\text{INTA}}$ floats to Tri-state OFF during bus hold acknowledge.
M/$\overline{\text{IO}}$	67	O	MEMORY I/O SELECT distinguishes memory access from I/O access. If HIGH during Ts, a memory cycle or a halt/shutdown cycle is in progress. If LOW, an I/O cycle or an interrupt acknowledge cycle is in progress M/$\overline{\text{IO}}$ floats to Tri-state OFF during bus hold acknowledge.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
$\overline{\text{LOCK}}$	68	O	BUS LOCK indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The $\overline{\text{LOCK}}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by SAB 80286 hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{\text{LOCK}}$ is active LOW and floats to Tri-state OFF during bus hold acknowledge.
VCC	30, 62	–	POWER SUPPLY (+5V)
VSS	9, 35, 60	–	GROUND (0V)
CAP	52	I	SUBSTRATE FILTER CAPACITOR: a 0,047 µf ±20% 12V capacitor must be connected between this pin and ground. This capacitor filters the output of the internal substrate bias generator. A maximum dc leakage current of 1 µa is allowed through the capacitor. For correct operation of the SAB 80286 the substrate bias generator must charge this capacitor to its operating voltage. The capacitor's charging time is 5 milliseconds (max.) after VCC and CLK reach their specified ac and dc parameters. RESET may be applied to prevent spurious activity by the CPU during this time. After this time, the SAB 80286 processor clock can be phase-synchronized to another clock by pulsing RESET LOW synchronous to the system clock.

Internal Block Diagram



Functional Description

Introduction

The SAB 80286 is an advanced, high-performance microprocessor with specially optimized capabilities for multiple user and multitasking systems. Depending on the application, the SAB 80286's performance is up to six times faster than that of the standard 5 MHz SAB 8086, while providing complete upward software compatibility with the Siemens 16-bit CPU family (SAB 8086/88, SAB 80186/88).

The SAB 80286 operates in two modes: real address mode (8086 mode) and protected virtual address mode. Both modes execute a superset of the SAB 8086/88 instruction set. In real address mode programs use real addresses with up to one megabyte of address space. Programs use virtual addresses in protected virtual address mode, also called protected mode. In protected mode, the SAB 80286 CPU automatically maps 1 gigabyte of virtual addresses per task into a 16 megabyte real address space. This mode also provides memory protection to isolate the operating system and ensure privacy of each task's programs and data. Both modes provide the same basic instruction set, registers, and addressing modes.
The following functional description describes first the basic SAB 80286 architecture common to both modes, second the real address mode, and thirdly the protected mode.

Basic Architecture

The processors of the Intel/Siemens 16-bit CPU family all contain the same basic set of registers, instructions, and addressing modes. Therefore, the SAB 80286 processor is upward-compatible with the SAB 8086, 8088 and 80186 CPUs.

Register Set

The SAB 80286 basic architecture has fifteen registers as shown below. These registers are grouped into the following four categories:

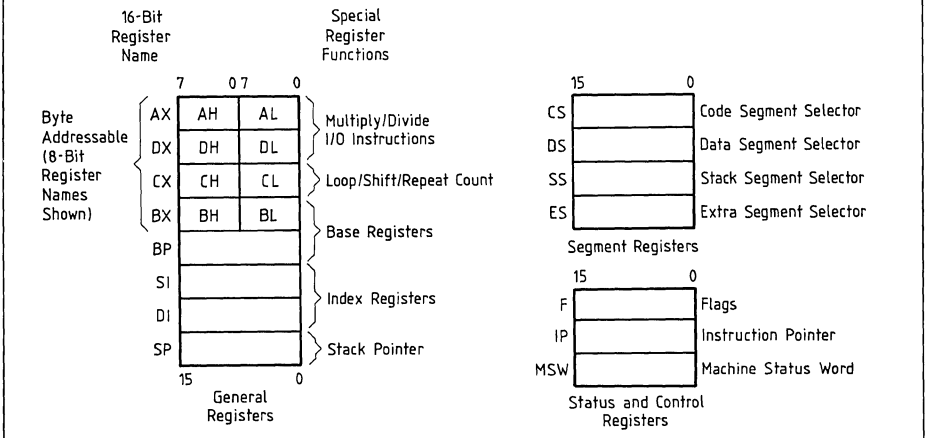
General registers: Eight 16-bit general purpose registers used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used either in their entirety as 16-bit words or split into pairs of separate 8-bit registers.

Segment registers: Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data (For usage, refer to Memory Organization).

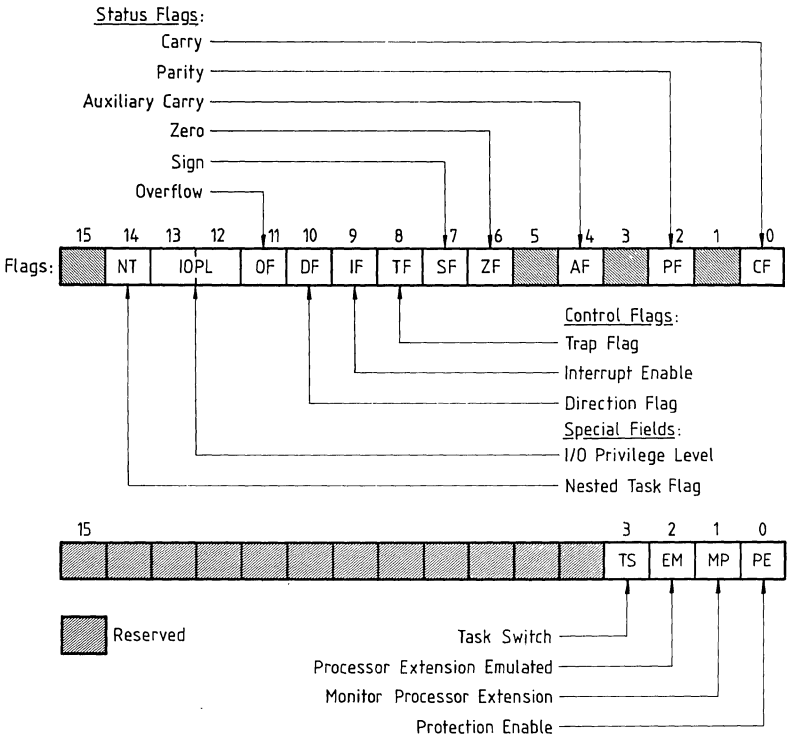
Base and index registers: Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode determines the specific registers used for operand address calculations.

Status and control registers: The three 16-bit special purpose registers in the figure below record or control certain aspects of the SAB 80286 processor state including the instruction pointer which contains the offset address of the next sequential instruction to be executed.

Register Set



Status and Control Register Bit Functions



Flags Word Description

The flags word (flags) records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 7, and 11) and controls the operation of the SAB 80286 within a given operating mode (bits 8 and 9). Flags is a 16-bit register. The function of the flag bits is given in table 1.

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high level instructions, and processor control.

An SAB 80286 instruction can reference zero, one, or two operands; where an operand resides in a register, in the instruction itself, or in memory. Zero-operand instructions (e.g. NOP and HLT) are usually one byte long. One-operand instructions (e.g. INC and DEC) are usually two bytes long but some are encoded in only one byte. One-operand instructions may reference a register or memory location. Tow-operand instructions permit the following six types of instruction operations:

- register to register
- memory to register
- immediate data to register
- memory to memory
- register to memory
- immediate data to memory

Two-operand instructions (e.g. MOV and ADD) are usually three to six bytes long. Memory to memory operations are provided by a special class of string instructions requiring one to three bytes. For detailed instruction formats and encodings refer to the instruction set summary.

Table 1
Flags Word Bit Functions

Bit position	Name	Functions
0	CF	Carry Flag – Set on high-order bit carry or borrow; cleared otherwise
2	PF	Parity Flag – Set if low-order 8 bits of result contain an even number of 1-bits; cleared otherwise
4	AF	Set on carry from or borrow to the low-order 4 bits of AL; cleared otherwise
6	ZF	Zero Flag – Set if result is zero; cleared otherwise
7	SF	Sign Flag – Set equal to high-order bit of result (0 if positive, 1 if negative)
11	OF	Overflow Flag – Set if result is a positive number too large or a negative number too small (excluding sign bit) to fit in destination operand; cleared otherwise
8	TF	Single Step Flag – Once set, a single step interrupt occurs after the next instruction has been executed. TF is cleared by the single step interrupt
9	IF	Interrupt Enable Flag – When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location
10	DF	Direction Flag – Causes string instructions to autodecrement the appropriate index registers when set. Clearing DF causes autoincrement

Memory Organization

Memory is organized as sets of variable length segments. Each segment is a linear contiguous sequence of up to 64 K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit segment selector, and a 16-bit offset. The segment selector indicates the desired segment in memory. The offset component indicates the desired byte address within the segment.

Two Component Address

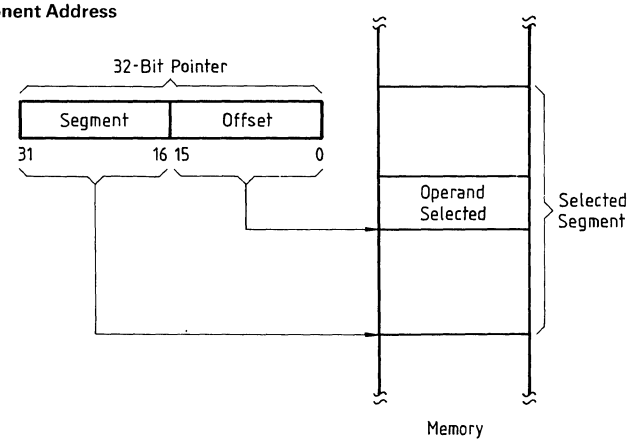


Table 2
Segment Register Selection Rules

Memory reference needed	Segment register used	Implicit segment selection rule
Instructions	Code (CS)	Automatic with instruction prefetch
Stack	Stack (SS)	All stack pushes and pops. Any memory reference which uses BP as a base register
Local data	Data (DS)	All data references except when relative to stack or string destination
Externed (global) data	Extra (ES)	Alternate data segment and destination of string operation

All instructions that address operands in memory must specify the segment and the offset. For speed and compact instruction encoding, segment selectors are usually stored in the high-speed segment registers. An instruction need specify only the desired segment register and an offset in order to address a memory operand.

Most instructions need not explicitly specify which segment register is used. The correct segment register is automatically chosen according to the rules of table 2.

These rules follow the way programs are written as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs. To access operands not residing in one of the four immediately available segments, a full 32-bit pointer or a new segment selector must be loaded.

Addressing Modes

The SAB 80286 provides a total of eight adressing modes for instructions to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

Register operand mode: The operand is located in one of the 8 or 16-bit general registers.

Immediate operand mode: The operand is included in the instruction.

Direct mode: The operand's offset is contained in the instruction as an 8 or 16-bit displacement element.

Register indirect mode: The operand's offset is in one of the registers SI, DI, BX, or BP.

Based mode: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of a base register (BX or BP).

Indexed mode: The operand's offset is the sum of an 8 or 16-bit displacement and the contents of an index register (SI or DI).

Based indexed mode: The operand's offset is the sum of the contents of a base register and an index register.

Based indexed mode with displacement: The operand's offset is the sum of a base register's contents, an index register's contents, and an 8 or 16-bit displacement.

Data Types

The SAB 80286 directly supports the following data types:

Integer:
A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32 and 64-bit integers are supported using the numeric data processor extension.

Ordinal:
An unsigned binary numeric value contained in an 8-bit byte or 16-bit word.

Pointer:
A 32-bit quantity, composed of a segment selector component and an offset component. Each component is a 16-bit word.

String:
A contiguous sequence of bytes or words. A string may contain between 1 byte and 64 Kbytes.

ASCII:
A byte representation of alphanumeric and control characters using the ASCII standard of character representation.

BCD:
A byte (unpacked) representation of the decimal digits 0 to 9.

Packed BCD:
A byte (packed) representation of two decimal digits 0 to 9 storing one digit in each nibble of the byte.

Floating Point:
A signed 32, 64, or 80-bit real number representation (Floating point operands are supported using the extended processor configuration with SAB 80287).

I/O Space
The I/O space consists of 64 K 8-bit or 32 K 16-bit ports. I/O instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register, 8-bit port addresses are zero extended such that A15-A8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Table 3
Interrupt Vector Assignments

Function	Interrupt Number	Related instructions	Return address before instruction causing exception?
Divide error exception	0	DIV, IDIV	Yes
Single step interrupt	1	All	–
NMI interrupt	2	All	–
Breakpoint interrupt	3	INT	–
INT0 detected overflow exception	4	INT0	No
BOUND range exceeded exception	5	BOUND	Yes
Invalid opcode exception	6	any undefined opcode	Yes
Processor extension not available exception	7	ESC or WAIT	Yes
Reserved	8–15		–
Processor extension error interrupt	16	ESC or WAIT	–
Reserved	17–31		–
User defined	32–255		–

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (flags) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware-initiated interrupts occur in response to an external input and are classified as non-maskable or maskable. Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. The return address from an exception will always point at the instruction causing the exception and include any leading instruction prefixes.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0 to 31, some of which are used for instruction exceptions, are reserved. For each interrupt, an 8-bit vector must be supplied to the SAB 80286 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Single step interrupt

The SAB 80286 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single step interrupt and is controlled by the single step flag bit (TF) in the flag word. Once this bit is set, an internal single step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single-stepped.

Interrupt Priorities

When simultaneous interrupt requests occur, they are processed in a fixed order as shown in table 4. Interrupt processing involves saving the flags, return address, and setting CS:IP to point at the first instruction of the interrupt handler. If other interrupts remain enabled they are processed before the first instruction of the current interrupt handler is executed. The last interrupt processed is therefore the first one serviced.

Table 4
Interrupt Processing Order

Order	Interrupt
1	Instruction exception
2	Single step
3	NMI
4	Processor extension segment overrun
5	INTR
6	INT instruction

Initialization and processor reset

Processor initialization or start up is accomplished by driving the RESET input pin HIGH. RESET forces the SAB 80286 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as RESET is active. After RESET became inactive and an internal processing interval has elapsed, the SAB 80286 begins execution in real address mode with the instruction at physical location FFFFF0(H). RESET also sets some registers to predefined values as shown in table 5.
A23 to A20 will be HIGH when the SAB 80286 performs memory references relative to the CS register until CS is changed. A23 to A20 will be zero for references to the DS, ES, or SS segments. Changing CS in real address mode will force A23 to A20 LOW whenever CS is used again. The initial CS:IP value of F000:FFF0 provides 64 Kbytes of code space for initialization code without changing CS.

Table 5
SAB 80286 Initial Register State after RESET

Flag word	0002(H)
Machine status word	FFF0(H)
Instruction pointer	FFF0(H)
Code segment	F000(H)
Data segment	0000(H)
Extra segment	0000(H)
Stack segment	0000(H)

Machine Status Word Description

The machine status word (MSW) records when a task switch takes place and controls the operating mode of the SAB 80286. It is a 16-bit register of which the lower four bits are used. One bit places the CPU into protected mode, while the other three bits, as shown in table 6, control the processor extension interface. After RESET, this register contains FFF0(H) which places the SAB 80286 in real address mode.

Table 6
MSW Bit Functions

Bit position	Name	Function
0	PE	**P**rotected mode **e**nable places the SAB 80286 into protected mode and cannot be cleared except by RESET
1	MP	**M**onitor **p**rocessor extension allows WAIT instructions to cause a processor extension not present exception (number 7)
2	EM	**Em**ulate processor extension causes a processor extension not present exception (number 7) on ESC instructions to allow emulating a processor extension
3	TS	**T**ask **s**witched indicates that the next instruction using a processor extension will cause exception 7, allowing software to test whether the current processor extension context belongs to the current task

The LMSW and SMSW instructions can load and store the MSW in real address mode. The recommended use of TS, EM, and MP is shown in table 7.

Table 7
Recommended MSW Encodings For Processor Extension Control

TS	MP	EM	Recommended use	Instructions causing exception 7
0	0	0	Initial encoding after RESET. SAB 20286 operation is identical with SAB 8086/88 operation	none
0	0	1	No processor extension is available. Software will emulate its function	ESC
1	0	1	No processor extension is available. Software will emulate its function. The current processor extension context may belong to another task	ESC
0	1	0	A processor extension exists	none
1	1	0	A processor extension exists. The current processor extension context may belong to another task. The exception on WAIT allows software to test for an error pending from a previous processor extension operation	ESC or WAIT

Halt

The HLT instruction stops program execution and prevents the CPU from using the local bus until restarted. Either NMI, INTR with IF = 1, or RESET will force the SAB 80286 out of halt. If interrupted the saved CS:IP will point to the next instruction after the HLT.

Real Address Mode

The SAB 80286 executes a fully upward-compatible superset of the SAB 8086's instruction set in real address mode. In real address mode, the SAB 80286 is object code compatible with SAB 8086 and SAB 8088 software. The real address mode architecture (registers and addressing modes) is exactly as described in the SAB 80286 basic architecture section of this functional description.

Memory Size

Physical memory is a contiguous array of up to 1,048,576 bytes (one megabyte) addressed by pins A0 through A19 and $\overline{BHE}$. A20 through A23 may be ignored.

Memory Addressing

In real address mode the processor generates 20-bit physical addresses directly from a 20-bit-segment base address and a 16-bit offset.

The selector portion of a pointer is interpreted as the upper 16 bits of a 20-bit segment address. The lower four bits of the 20-bit segment addresses are always zero. Segment addresses, therefore, begin on multiples of 16 bytes. See figure on address calculation for a graphic representation of address formation.

All segments in real address mode are 64 Kbytes in size and may be read, written, or executed. An exception or interrupt can occur if data operands or instructions attempt to wrap around the end of a segment (e.g. a word with its low-order byte at offset FFFF(H) and its high-order byte at offset 0000(H). If, in real address mode, the information contained in a segment does not use the full 64 Kbytes, the unused end of the segment may be overlayed by another segment to reduce physical memory requirements.

Real Address Mode, Address Calculation

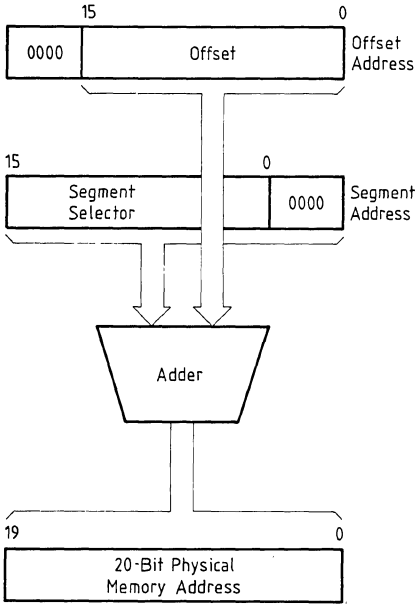


Table 8
Real Address Mode, Addressing Interrupts

Function	Interrupt number	Related instructions	Return address before instruction?
Interrupt table limit too small exception	8	INT vector is not within table limit	Yes
Processor extension segment overrun interrupt	9	ESC with memory operand extending beyond offset FFFF(H)	No
Segment overrun exception	13	Word memory reference with offset = FFFF(H) or an attempt to execute past the end of a segment	Yes

Interrupts

Table 8 shows the interrupt vectors reserved for exceptions and interrupts which indicate an addressing error. The exceptions leave the CPU in the state existing before attempting to execute the failing instruction (except for PUSH, POP, PUSHA, or POPA).

Shutdown

Shutdown occurs when a severe error is detected that prevents further instruction processing by the CPU. Shutdown and halt are externally signalled via a halt bus operation. They can be distinguished by A1 HIGH for halt and A1 LOW for shutdown. In real address mode, shutdown can occur under two conditions:

- Exceptions 8 or 13 happen and the IDT limit does not include the interrupt vector.
- A CALL, INT or POP instruction attempts to wrap around the stack segment when SP is not even.

An NMI input can bring the CPU out of shutdown if the IDT limit is at least 000F(H) and SP is greater than 0005(H), otherwise shutdown can only be exited via the RESET input.

Protected Virtual Address Mode

The SAB 80286 executes a fully upward-compatible superset of the SAB 8086 instruction set in protected virtual address mode (protected mode). Protected mode also provides memory management and protection mechanisms and associated instructions.

The SAB 80286 enters protected virtual address mode from real address mode by setting the PE (Protection Enable) bit of the machine status word with the Load Machine Status Word (LMSW) instruction. Protected mode offers extended physical and virtual memory address space, memory protection mechanisms, and new operations to support operating system and virtual memory.

All registers, instructions and addressing modes described in the SAB 80286 basic architecture section of the functional description remain the same. Programs for the SAB 8086, SAB 8088, SAB 80186 and real address mode SAB 80286 can be run in protected mode: however, embedded constants for segment selectors are different.

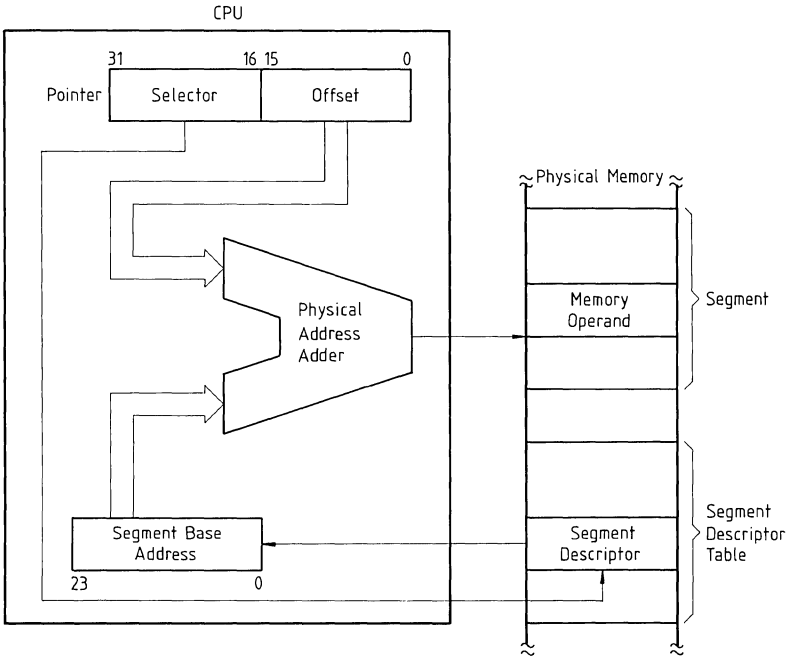
Memory Size

The protected mode SAB 80286 provides a 1 gigabyte virtual address space per task mapped into a 16 megabyte physical address space defined by the address pins A23–A0 and $\overline{BHE}$. The virtual address space may be larger than the physical address space since any use of an address that does not map to a physical memory location will cause a restartable exception.

Memory Addressing

As in real address mode, protected mode uses 32-bit pointers, consisting of 16-bit selector and offset components. The selector, however, specifies an index into a memory resident table rather than the upper 16-bits of a real memory address. The 24-bit base address of the desired segment is obtained from the tables in memory. The 16-bit offset is added to the segment base address to form the physical address as shown in the figure below. The tables are automatically referenced by the CPU whenever a segment register is loaded with a selector. All SAB 80286 instructions which load a segment register will reference the memory-based tables without additional software. The memory-based tables contain 8 byte values called descriptors.

Protected Mode, Memory Addressing



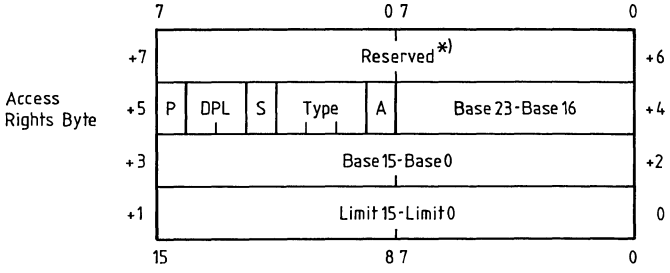
Descriptors

Descriptors define the use of memory. Special types of descriptors also define new functions for transfer of control and task switching. The SAB 80286 has segment descriptors for code, stack and data segments, as well as system control descriptors for special system data segments and control transfer operations. Descriptor accesses are performed as locked bus operations to assure descriptor integrity in multiprocessor systems.

Code and data segment descriptors (S = 1)

Besides segment base addresses, code and data descriptors contain other segment attributes including segment size (1 to 64 Kbytes), access rights (read only, read/write, execute only, and execute/read), and presence in memory (for virtual memory systems; figure and table next page). Any segment usage violating a segment attribute indicated by the segment descriptor will prevent the memory cycle and cause an exception or interrupt.

Code or Data Segment Descriptor



*) Must be set to 0 for compatibility with SAB 80386

Access Rights Byte Definition

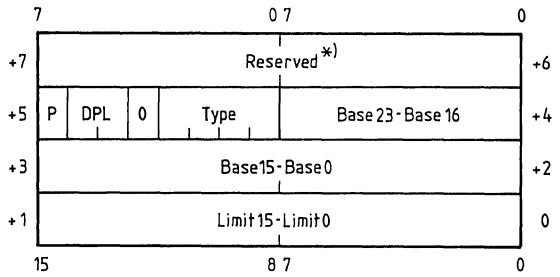
	Bit Position	Name		Function	
	7	Present (P)	P = 1	Segment is mapped into physical memory	
			P = 0	No mapping to physical memory exists, base and limit are not used	
	6-5	Descriptor privilege level (DPL)		Segment privilege attribute used in privilege tests	
	4	Segment descriptor (S)	S = 1	Code or data (includes stacks) segment descriptor	
			S = 0	System segment descriptor or gate descriptor	
Type field definition	3	Executable (E)	E = 0	Data segment descriptor type is:	If
	2	Expansion direction (ED)	ED = 0	Expand up segment, offsets must be ≤ limit	data
			ED = 1	Expand down segment, offsets must be > limit	segment
	1	Writeable (W)	W = 0	Data segment may not be written into	(S = 1,
			W = 1	Data segment may be written into	E = 0)
	3	Executable (E)	E = 1	Code segment descriptor type is:	If
	2	Conforming (C)	C = 1	Code segment may only be executed when CPL ≥ DPL and CPL remains unchanged	code segment
	1	Readable (R)	R = 0	Code segment may not be read	(S = 1,
			R = 1	Code segment may be read	E = 1)
	0	Accessed (A)	A = 0	Segment has not be accessed	
			A = 1	Segment selector has been loaded into segment register or used by selector test instructions	

Code and data (including stack data) are stored in two types of segments: code segments and data segments. Both types are identified and defined by segment descriptors (S = 1). Code segments are identified by the executable (E) bit set to 1 in the descriptor access rights byte, whereas the data segments have the E bit set to 0.

System segment descriptors (S = 0, type = 1-3)

In addition to code and data segment descriptors, the protected mode SAB 80286 defines system segment descriptors. These descriptors define special system data segments which contain a table of descriptors (local descriptor table descriptor) or segments which contain the execution state of a task (task state segment descriptor).
The figure and table on next page show the formats for the special system data segment descriptors.

System Segment Descriptor



*) Must be set to 0 for compatibility with SAB 80386

System Segment Descriptor Fields

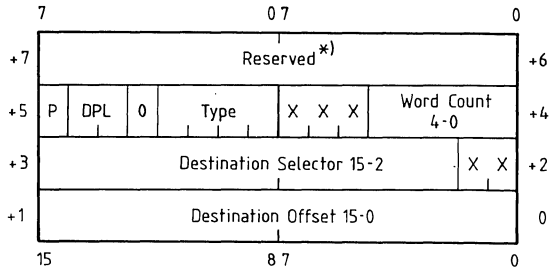
Name	Value	Description
TYPE	1 2 3	Available task state segment Local descriptor table descriptor Busy task state segment
P	0 1	Descriptor contents are not valid Descriptor contents are valid
DPL	0–3	Descriptor privilege level
BASE	24-bit number	Base address of special system data segment in real memory
LIMIT	16-bit number	Offset of last byte in segment

Gate Descriptors (S = 0, Type = 4-7)

Gates are used to control access to entry points within the target code segment. The gate descriptors are **call** gates, **task** gates, **interrupt** gates and **trap** gates. Gates provide a level of indirection between the source and destination of the control transfer. This indirection allows the CPU to automatically perform protection checks and control entry point of the destination. Call gates are used to change privilege levels (see privilege), task gates are used to perform a task switch, and interrupt and trap gates are used to specify interrupt service routines. The interrupt gate disables interrupts (resets IF) while the trap gate does not.

The figure and table below show the format of the gate descriptors. The descriptor contains a destination pointer that points to the descriptor of the target segment and the entry point offset. The destination selector in an interrupt gate, trap gate, and call gate must refer to a code segment descriptor. Exception 13 is generated when the gate is used if a destination selector does not refer to the correct descriptor type.

Gate Descriptor



*) Must be set to 0 for compatibility with SAB 80386 (X is don't care)

Gate Descriptor Fields

Name	Value	Description
TYPE	4 5 6 7	– Call gate – Task gate – Interrupt gate – Trap gate
P	0 1	– Descriptor contents are not valid – Descriptor contents are valid
DPL	0–3	Descriptor Privilege level
WORD COUNT	0–31	Number of words to copy from callers stack to called procedures stack. Only used with call gate
DESTINATION SELECTOR	16-bit selector	Selector to the target code segment (call, interrupt or trap gate)
DESTINATION OFFSET	16-bit offset	Entry point within the target code segment

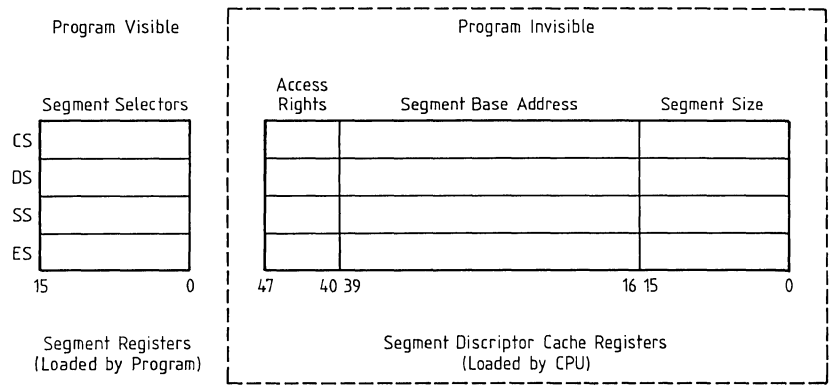
Segment Descriptor Cache Registers

A segment descriptor cache register is assigned to each of the four segment registers (CS, SS, DS, ES). Segment descriptors are automatically loaded (cached) into a segment descriptor cache register (see figure) whenever the associated segment register is loaded with a selector. Only segment descriptors may be loaded into segment descriptor cache registers. Once loaded, all references to that segment of memory use the cached descriptor information instead of reaccessing memory. The descriptor cache registers are not visible to programs. No instructions exist to store their contents. They only change when a segment register is loaded.

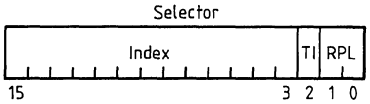
Selector Fields

A protected mode selector has three fields: descriptor entry index, local or global descriptor table indicator (TI), and selector privilege (RPL) as shown in the figure on selector fields. These fields select one of two memory-based tables of descriptors, select the appropriate table entry and allow highspeed testing of the selector's privilege attribute (refer to privilege discussion below).

Descriptor Cache Registers



Selector Fields

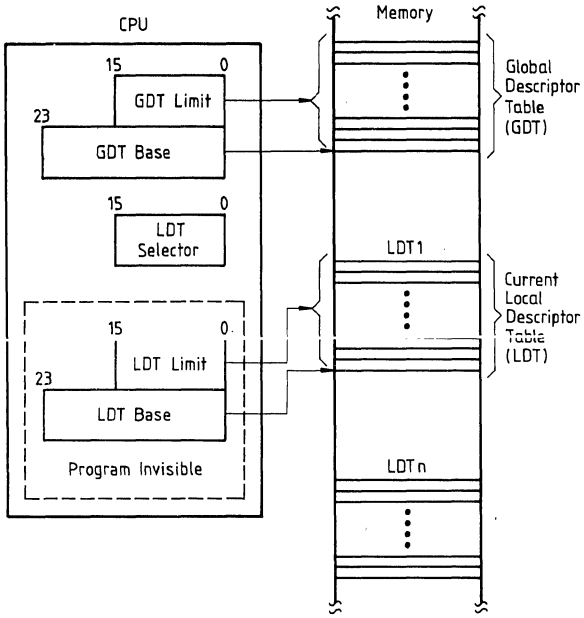


Bits	Name	Function
1-0	Requested Privilege Level (RPL)	Indicates Selector Privilege Level Desired
2	Table Indicator (TI)	TI = 0 Use Global Descriptor Table (GDT) TI = 1 Use Local Descriptor Table (LDT)
15-3	Index	Select Descriptor Entry in Table

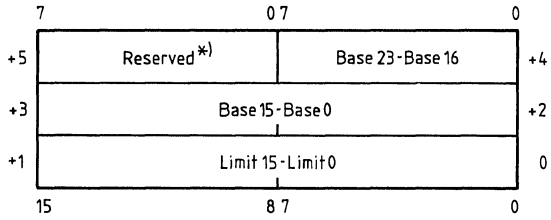
Local and Global Descriptor Tables (LDT, GDT)

Two tables of descriptors, called descriptor tables, contain all descriptors accessible by a task at any given time. A descriptor table is a linear array of up to 8192 descriptors. The upper 13 bits of the selector value are an index into a descriptor table. Each table has a 24-bit base register to locate the descriptor table in physical memory and a 16-bit limit register that confine descriptor access to the defined limits of the table as shown in the figure below. A restartable exception (13) will occur if an attempt is made to reference a descriptor outside the table limits.

Local and Global Descriptor Table Definition



Global Descriptor Table and Interrupt Descriptor Table Data Type

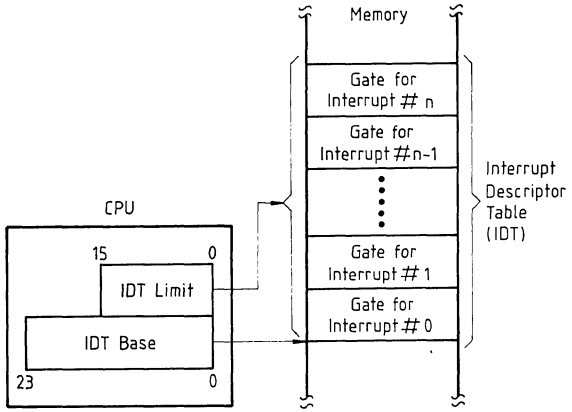


*) Must be set to 0 for compatibility with SAB 80386

Interrupt Descriptor Table

The protected mode SAB 80286 has a third descriptor table, called the interrupt descriptor table (DT) (see figure below), used to define up to 256 interrupts. It may contain only task gates, interrupt gates and trap gates. The IDT (interrupt descriptor table) has a 24-bit base and 16-bit limit register in the CPU. References to IDT entries are made via INT instructions, external interrupt vectors, or exceptions. The IDT must be at least 256 bytes in size to allocate space for all reserved interrupts.

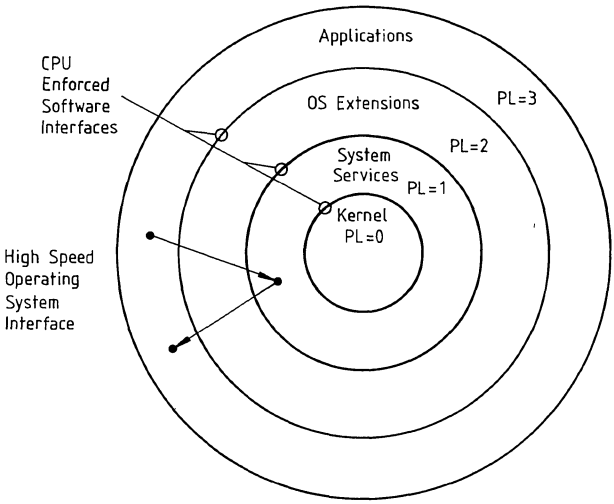
Interrupt Descriptor Table Definition



Privilege

The SAB 80286 has a four-level hierarchical privilege system which controls the use of privileged instructions and access to descriptors (and their associated segments) within a task (figure below). The privilege levels are numbered 0 through 3. Level 0 is the most privileged level.

Hierarchical Privilege Levels



Protection

The SAB 80286 includes mechanisms to protect critical instructions that affect the CPU execution state (e.g. HLT) and code or data segments from improper usage. These mechanisms are grouped under the term "protection" and have three forms:

Restricted usage of segments (e.g. no write allowed to read-only data segments). The only segments available for use are defined by descriptors in the local descriptor table (LDT) and global descriptor table (GDT).

Restricted access to segments via the rules of privilege and descriptor usage.

Privileged instructions or operations that may only be executed at certain privilege levels as determined by the CPL and I/O privilege level (IOPL). The IOPL is defined by bits 14 and 13 of the flag word.

These checks are performed for all instructions and can be split into three categories: segment load checks (table 9), operand reference checks (table 10), and privileged instruction checks (table 11). Any violation of the rules shown will result in an exception. A not-present exception related to the stack segment causes exception 12.

The IRET and POPF instructions do not perform some of their defined functions if CPL is not of sufficient privilege (numerically small enough). No exceptions or other indication are given when these conditions occur.

The IF bit is not changed if CPL > IOPL.
The IOPL field of the flag word is not changed if CPL > 0.

Table 9
Segment Register Load Checks

Error description	Exception number
Descriptor table limit exceeded	13
Segment descriptor not present	11 or 12
Privilege rules violated	13
Invalid descriptor/segment type segment register load: – read only data segment load to SS – special control descriptor load to DS, ES, SS – execute only segment load to DS, ES, SS – data segment load to CS – read/execute code segment load to SS	13

Table 10
Operand Reference Checks

Error description	Exception number
Write into code segment	13
Read from execute-only code segment	13
Write to read-only data segment	13
Segment limit exceeded [1]	12 or 13

[1] Carry out in offset calculations is ignored.

Table 11
Privileged Instruction Checks

Error description	Exception number
CPL > 0 when executing the following instructions LIDT, LLDT, LGDT, LTR, LMSW, CTS, HLT	13
CPL > IOPL when executing the following instructions INS, IN, OUTS, OUT, STI, CLI, LOCK	13

Exceptions

The SAB 80286 detects several types of exceptions and interrupts in protected mode (see table 12). Most of then are restartable after the exceptional condition is removed. Interrupt handlers for most exceptions receive an error code, pushed on the stack after the return address, that identifies the selector involved (0 if none). The return address normally points to the failing instruction, including all leading prefixes. For a processor extension segment overrun exception, the return address will not point at the ESC instruction that caused the exception; however, the processor extension registers may contain the address of the failing instruction.

Table 12
Protected Mode Exceptions

Interrupt vector	Function	Return address at failing instruction?	Always restart-able?	Error code on stack?
8	Double exception detected	yes	no	yes
9	Processor extension segment overrun	no	no	no
10	Invalid task state segment	yes	yes	yes
11	Segment not present	yes	yes	yes
12	Stack segment overrun or segment not present	yes	yes[1)]	yes
13	General protection	yes	no	yes

[1)] When a PUSHA instruction attempts to wrap around the stack segment, the machine state after the exception will not be restartable. This condition is identified by the value of the saved SP being either 0000(H), 0001(H), FFFE(H), or FFFF(H).

Special Operations

Task Switch Operation

The SAB 80286 provides a built-in task switch operation which saves the entire SAB 80286 execution state (registers, address space, and a link to the previous task), loads a new execution state, and commences execution in the new task. Like gates, the task switch operation is invoked by executing an inter-segment JMP or CALL instruction which refers to a task state segment (TSS) or task gate descriptor in the GDT or LDT. An INT instruction, exception, or external interrupt may also invoke the task switch operation by selecting a task gate descriptor in the associated IDT descriptor entry.

The TSS descriptor points at a segment (see figure on next page) containing the entire SAB 80286 execution state while a task gate descriptor contains a TSS selector. The limit field must be > 002B(H).

The task state segment is marked busy by changing the descriptor type field from type 1 to type 3. Use of a selector that references a busy task state segment causes exception 13.

Processor Extension Context Switching

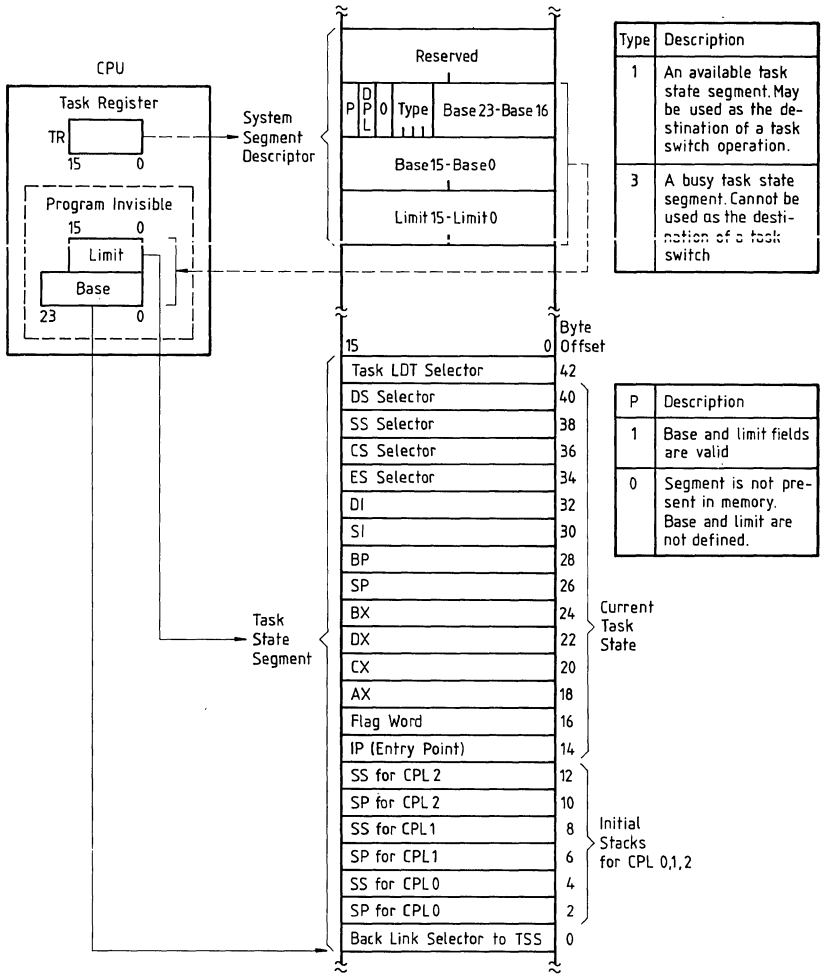
The context of a processor extension (such as the SAB 80287 numerics processor) is not changed by the task switch operation. A processor extension context need only be changed when a different task attempts to use the processor extension (which still contains the context of a previous task).

Whenever the SAB 80286 switches tasks, it sets the task switched (TS) bit of the MSW. TS indicates that a processor extension context may belong to a different task than the current one. The processor extension not present exception (7) will occur when attempting to execute an ESC or WAIT instruction if TS = 1 and a processor extension is present (MP = 1 in MSW).

Double Fault and Shutdown

If two seperate exceptions are detected during a single instruction execution, the SAB 80286 performs the double fault exception (8). If an exception occurs during processing of the double fault exception, the SAB 80286 will enter shutdown. During shutdown no further instructions or exceptions are processed. Either NMI (CPU remains in protected mode) or RESET (CPU exits protected mode) can force the SAB 80286 out of shutdown. Shutdown is externally signalled via a HALT bus operation with A1 HIGH.

Task State Segment and TSS Registers



Type	Description
1	An available task state segment. May be used as the destination of a task switch operation.
3	A busy task state segment. Cannot be used as the destination of a task switch

P	Description
1	Base and limit fields are valid
0	Segment is not present in memory. Base and limit are not defined.

System Interface

The SAB 80286 system interface appears in two forms: a local bus and a system bus. The local bus consists of address, data, status, and control signals at the pins of the CPU. A system bus is any buffered version of the local bus. A system bus may also differ from the local bus in terms of coding of status and control lines and/or timing and loading of signals. The SAB 80286 family includes several devices to generate standard system buses such as the IEEE 796 standard Multibus©

Bus Interface Signals and Timing

The SAB 80286 local bus interfaces the SAB 80286 to local memory and I/O components. The interface has 24 address lines, 16 data lines, and 8 status and control signals.

The SAB 80286 CPU, SAB 82284 clock generator, SAB 82288 bus controller, SAB 82289 bus arbiter, SAB 8286A/8287A transceivers, and SAB 8282A/8283A latches provide a buffered and decoded system bus interface. The SAB 82284 generates the system clock and synchronizes $\overline{\text{READY}}$ and RESET. The SAB 82288 converts bus operation status encoded by the SAB 80286 into command and bus control signals.

The SAB 82289 bus arbiter generates Multibus bus arbitration signals. These components can provide the timing and electrical power drive levels required for most system bus interfaces including the Multibus.

Physical Memory and I/O Interface

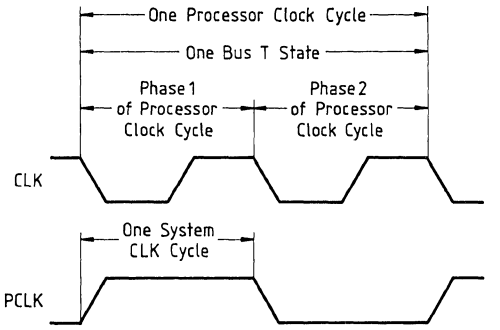
A maximum of 16 megabytes of physical memory can be addressed in protected mode. One megabyte can be addressed in real address mode. Memory is accessible as bytes or words. Words consist of any two consecutive bytes addressed with the least significant byte stored in the lowest address.

The I/O address space contains 64 K addresses in both modes. The I/O space is accessible as either bytes or words, as is memory. Byte-wide peripheral devices may be attached to either the upper or lower byte of the data bus. An interrupt controller such as the SAB 8259A must be connected to the lower byte of the data bus (D7-D0) for proper return of the interrupt vector.

Bus Operation

The SAB 80286 uses a double frequency system clock (CLK input) to control bus timing. All signals on the local bus are measured relative to the system CLK input. The CPU divides the system clock by 2 to produce the internal processor clock, which determines bus state. Each processor clock is composed of two system clock cycles named phase 1 and phase 2. The SAB 82284 clock generator output (PCLK) identifies the next phase of the processor clock (see figure on system and processor clock relationship).

System and Processor Clock Relationship



Six types of bus operations are supported: memory read, memory write, I/O read, I/O write, interrupt acknowledge, and halt/shutdown. Data can be transferred at a maximum rate of one word per two processor clock cycles.

The SAB 80286 bus has three basic states: idle (TI), send status (TS), and perform command (TC). The SAB 80286 CPU also has a fourth local bus state called hold (TH). TH indicates that the SAB 80286 has surrendered control of the local bus to another bus master in response to a HOLD request.

Each bus state is one processor clock long. The figure below shows the four SAB 80286 local bus states and allowed transitions.

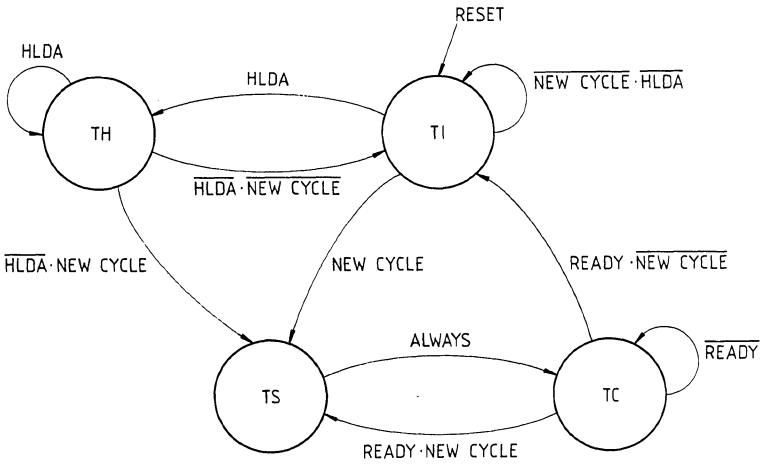
Pipelined Addressing

The SAB 80286 uses a local bus interface with pipelined timing to allow as much time as possible for data access. Pipelined timing allows bus operations to be performed in two processor cycles, while allowing each individual bus operation to last for three processor cycles.

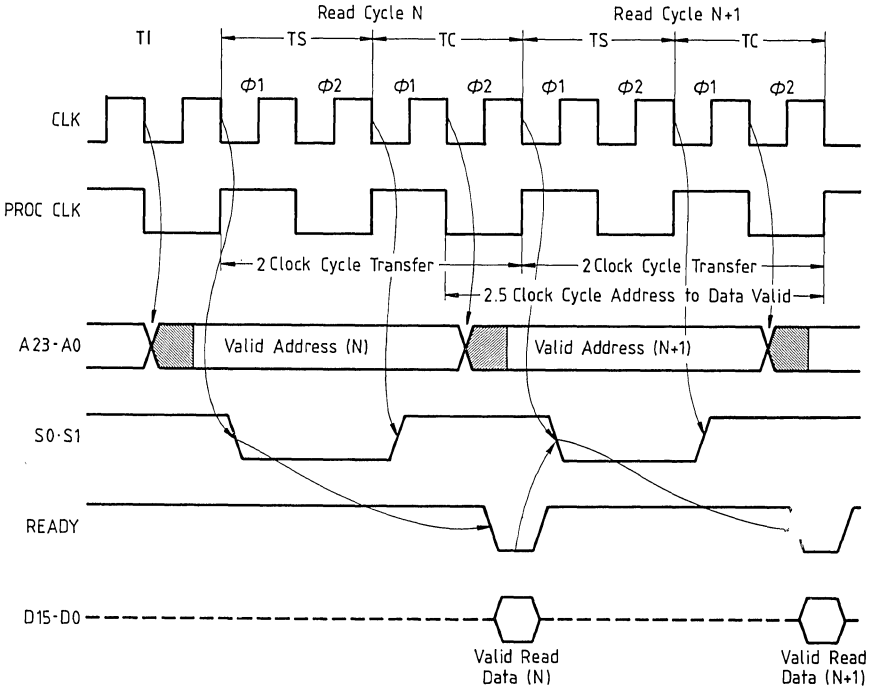
The timing of the address outputs is pipelined such that the address of the next bus operation becomes available during the current bus operation. Or in other words, the first clock of the next bus operation is overlapped with the last clock of the current bus operation. Therefore, address decoder and routing logic can operate in advance of the next bus operation. External address latches may hold the address stable for the entire bus operation, and provide additional ac and dc buffering.

The SAB 80286 does not maintain the address of the current bus operation during all TC states. Instead, the address for the next bus operation may be emitted during phase 2 of any TC. The address remains valid during phase 1 of the first TC to guarantee hold time, relative to ALE, for the address latch inputs.

SAB 80286 Bus States



Basic Bus Cycle



Bus Cycle Termination

At maximum transfer rates, the SAB 80286 bus alternates between the status and command states. The bus status signals become inactive after TS so that they may correctly signal the start of the next bus operation after the completion of the current cycle. No external indication of TC exists on the SAB 80286 local bus. The bus master and bus controller enter TC directly after TS, and continue executing TC cycles until terminated by $\overline{\text{READY}}$.

$\overline{\text{READY}}$ Operation

The current bus master and SAB 82288 bus controller terminate each bus operation simultaneously to achieve maximum bus bandwidth. Both are informed in advance by $\overline{\text{READY}}$ active which identifies the last TC cycle of the current bus operation. The bus master and bus controller must see the same sense of the $\overline{\text{READY}}$ signal, there by requiring $\overline{\text{READY}}$ be synchronous to the system clock.

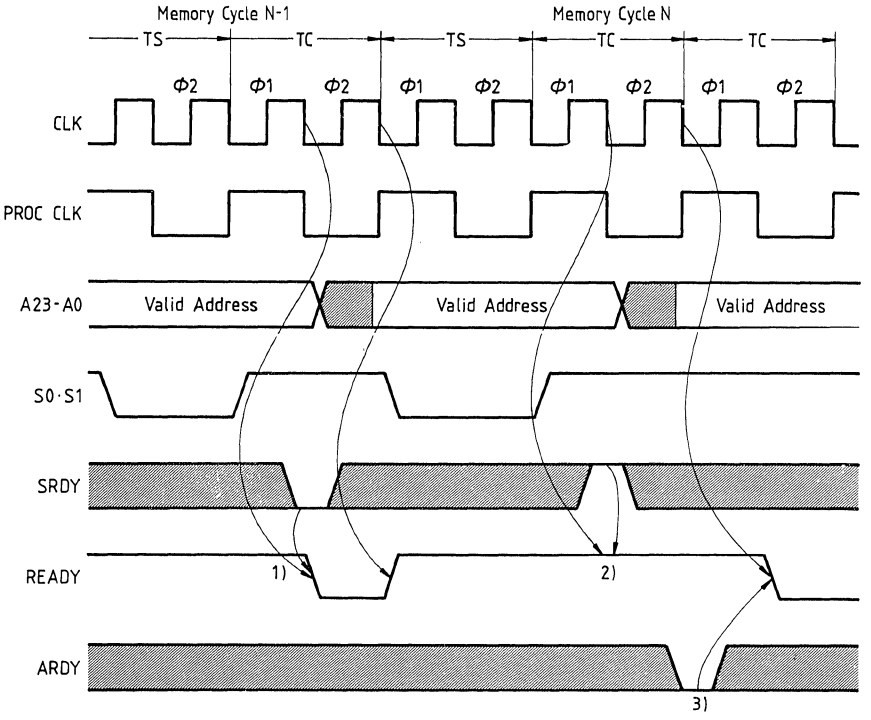
Synchronous Ready

The SAB 82284 clock generator provides $\overline{\text{READY}}$ synchronization from both synchronous and asynchronous sources (see figure on next page). The synchronous ready input ($\overline{\text{SRDY}}$) of the clock generator is sampled with the falling edge of CLK at the end of phase 1 of each TC. The state of $\overline{\text{SRDY}}$ is then transferred to the bus master and bus controller via the $\overline{\text{READY}}$ output line.

Asynchronous Ready

Many systems have devices of subsystems that are asynchronous to the system clock. As a result, their ready outputs cannot be guaranteed to meet the SAB 82284 $\overline{\text{SRDY}}$ setup and hold time requirements. But the SAB 82284 asynchronous ready input ($\overline{\text{ARDY}}$) is designed to accept such signals. The $\overline{\text{ARDY}}$ input is sampled at the beginning of each TC cycle by SAB 82284 synchronization logic. This provides one system CLK cycle time to resolve its value before transferring it to the bus master and bus controller.

Synchronous and Asynchronous Ready



1) $\overline{\text{SRDYEN}}$ is active low
2) If $\overline{\text{SRDYEN}}$ is high, the state of $\overline{\text{SRDY}}$ will not effect $\overline{\text{READY}}$
3) $\overline{\text{ARDYEN}}$ is active low

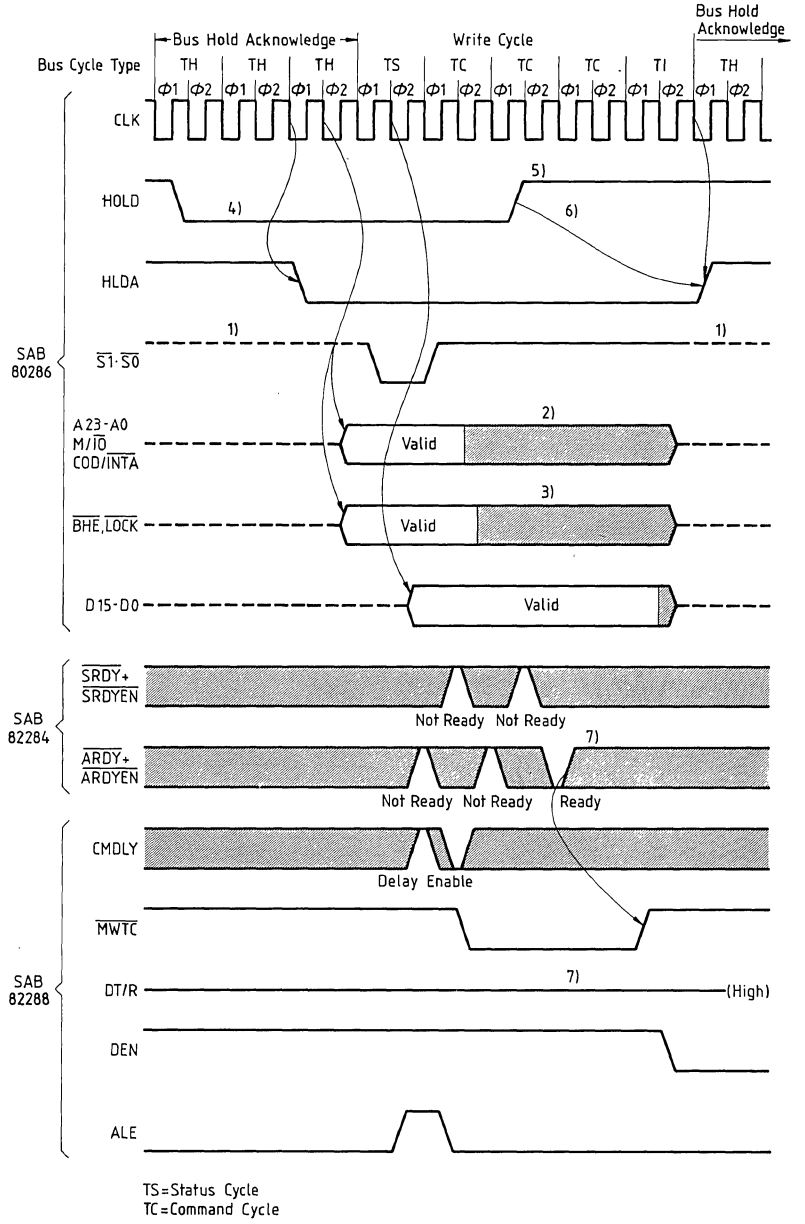
$\overline{\text{ARDY}}$ or $\overline{\text{ARDYEN}}$ must be HIGH at the end of TS. $\overline{\text{ARDY}}$ cannot be used to terminate a bus cycle with no wait states.

Each ready input of the SAB 82284 has an enable pin ($\overline{\text{SRDYEN}}$ and $\overline{\text{ARDYEN}}$) to select whether the current bus operation will be terminated by the synchronous or asynchronous ready. Either of the ready inputs may terminate a bus operation. These enable inputs are active low and have the same timing as their respective ready inputs. An address decode logic usually selects whether the current bus operation should be terminated by $\overline{\text{ARDY}}$ or $\overline{\text{SRDY}}$.

Hold and HLDA

HOLD and HLDA allow another bus master to gain control of the local bus by placing the SAB 80286 bus into the Th state. The sequence of events required to pass control between the SAB 80286 and another local bus master is shown in the next figure.

Multibus Write Terminated by Asynchronous Ready with Bus Hold



1) Status lines are not driven by SAB 80286 yet remain high due to pullup resistors in SAB 80288 and SAB 82289 during HOLD state.
2) Address, M/$\overline{IO}$ and COD/$\overline{INTA}$ may start floating during any TC depending on when internal SAB 80286 bus arbiter decides to release bus to external HOLD. The float starts in ∅2 of TC.
3) $\overline{BHE}$ and $\overline{LOCK}$ may start floating after the end of any TC depending on when internal SAB 80286 bus arbiter decides to release bus to external HOLD. The float starts in ∅1 of TC.
4) The minimum HOLD to HLDA time in shown. Maximum is one TH longer.
5) The earliest HOLD time is shown. It will always allow a subsequent memory cycle if pending as shown.
6) The minimum HOLD in HLDA time is shown. Maximum is a function of the instruction, type of bus cycle and other machine status (i.e., interrupts, waits, lock, etc.)
7) Asynchronous ready allows termination of the cycle. Synchronous ready does not signal ready in this example. Synchronous ready state in ignored after ready is signalled via the asynchronous input.

Processor Extension Transfers

The processor extension interface uses I/O port addresses 00F8(H), 00FA(H), and 00FC(H) which are part of the I/O port address range reserved. An ESC instruction with EM = 0 and TS = 0 will perform I/O bus operations to one or more of these I/O port addresses independent of the value of IOPL and CPL.

ESC instructions with memory references enable the CPU to accept PEREQ inputs for processor extension operand transfers. The CPU will determine the operand starting address and read/write status of the instruction. For each operand transfer, two or three bus operations are performed, one word transfer with I/O port address 00FA(H) and one or two bus operations with memory. Three bus operations are required for each word operand aligned on an odd byte address.

Interrupt Acknowledge Sequence

The figure Interrupt Acknowledge Sequence illustrates a sequence performed by the SAB 80286 in response to an INTR input. An interrupt acknowledge sequence consists of two INTA bus operations. The first allows a master SAB 8259A programmable interrupt controller (PIC) to determine which if any of its slaves should return the interrupt vector. An eight-bit vector is read by the SAB 80286 during the second INTA bus operation to select an interrupt handler routine from the interrupt table.

The master cascade enable (MCE) signal of the SAB 82288 is used to enable the cascade address drivers, during INTA bus operations (see interrupt acknowledge sequence figure), onto the local address bus for distribution to slave interrupt controllers via the system address bus. The SAB 80286 emits the $\overline{LOCK}$ signal (active LOW) during TS of both INTA bus operations. A local bus "hold" request will not be honored until the end of the second INTA bus operation.

Three idle processor clocks are provided by the SAB 80286 between INTA bus operations to allow for the minimum INTA to INTA time and CAS (cascade address) out delay of the SAB 8259A. The second INTA bus operation must always have at least one extra TC state added via logic controlling $\overline{READY}$. A23–A0 are in Tri-state OFF until the first TC state of the second INTA bus operation. This prevents bus contention between the cascade address drivers and CPU address drivers. The extra TC state provides time for the SAB 80286 to resume driving the address lines for subsequent bus operations.

Local Bus Usage Priorities

The SAB 80286 local bus is shared among several internal units and external HOLD requests. In case of simultaneous requests, their relative priorities are:

(Highest)
Any transfers which assert $\overline{LOCK}$ either explicitly (via the LOCK instruction prefix) or implicitly (i.e. segment descriptor access, interrupt acknowledge sequence, or an XCHG with memory).

The second of the two byte bus operations required for an odd-aligned word operand.

The second or third cycle of a processor extension data transfer.

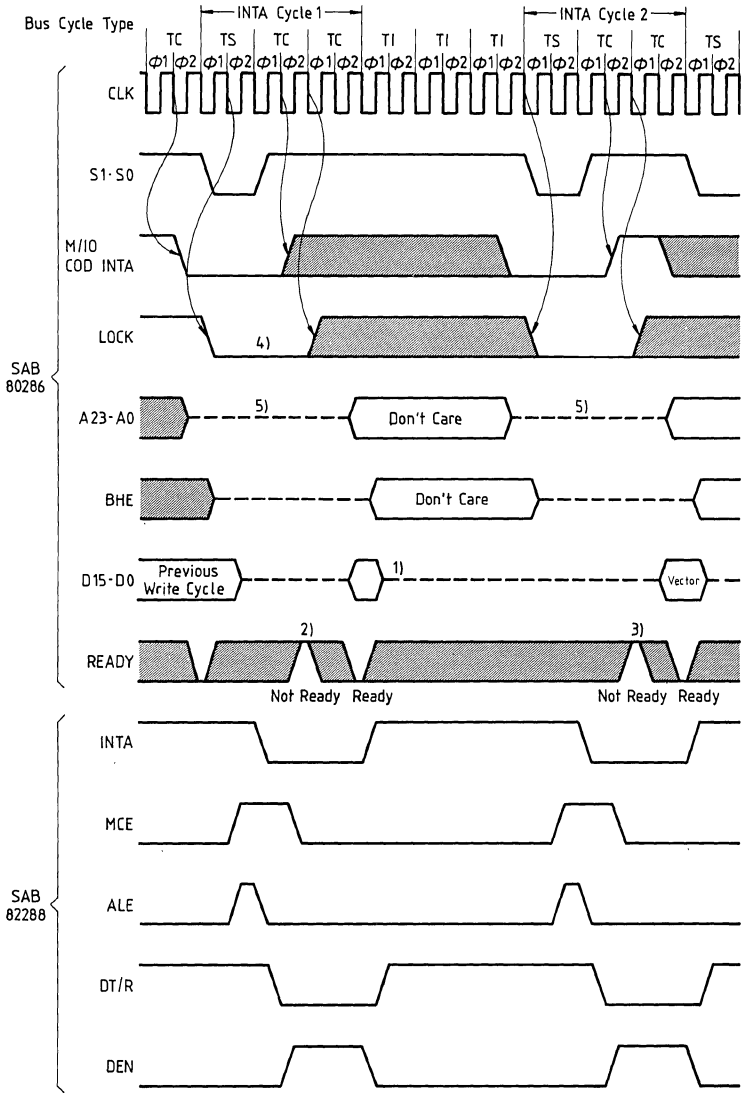
Local bus request via HOLD input.

Processor extension data operand transfer via PEREQ input.

Data transfer performed by EU as part of an instruction.

(Lowest)
An instruction prefetch request from BU. The EU wil inhibit prefetching two processor clocks in advance of any data transfer to minimize waiting by EU for a prefetch to finish.

Interrupt Acknowledge Sequence



Halt or Shutdown Cycles

The SAB 80286 externally indicates halt or shutdown conditions as a bus operation. These conditions occur due to an HLT instruction or multiple protection exceptions while attempting to execute one instruction. A halt or shutdown bus operation is signalled when $\overline{S1}$, $\overline{S0}$ and COD/$\overline{INTA}$ are LOW and M/$\overline{IO}$ is HIGH. A1 HIGH indicates halt, and A1 LOW indicates shutdown. The SAB 82288 bus controller does not issue ALE, nor is $\overline{READY}$ required to terminate a halt or shutdown bus operation.

During halt or shutdown, the SAB 80286 may service $\overline{PEREQ}$ or HOLD requests. A processor extension segment overrun exception during shutdown will inhibit further service of $\overline{PEREQ}$. Either NMI or RESET will force the SAB 80286 out of halt or shutdown. An INTR, if interrupts are enabled, or a processor extension segment overrun exception will also force the SAB 80286 out of halt.

1) Data is ignored.
2) First INTA cycle should have at least one wait state inserted to meet SAB 8259A minimum INTA pulse width.
3) Second INTA cycle must have at least one wait state inserted since the CPU will not drive A23–A0. $\overline{BHE}$, and $\overline{LOCK}$ until after the first TC state.

   The CPU-imposed one clock delay prevents bus contention between cascade address buffer being disabled by MCE ↓ and address outputs.

   Without the wait state, the SAB 80286 address will not be valid for a memory cycle started immediately after the second INTA cycle.
   The SAB 8259A also requires one wait state for minimum INTA pulse width.
4) $\overline{LOCK}$ is activated during the INTA cycles to prevent the SAB 82289 from releasing the bus between INTA cycles in a multimaster system.
5) A23–A0 exit Tri-state OFF during ∅2 of the second TC in the INTA cycle.

System Configuration

The versatile bus structure of the SAB 80286 microsystem, with a full complement of support chips, allows flexible configuration of a wide range of system. The basic configuration shown above is similar to an SAB 80286 maximum mode system. It includes the CPU plus an SAB 8259A interrupt controller, SAB 82284 clock generator and the SAB 82288 bus controller. The latches (SAB 8282A and SAB 8283A) and transceivers (SAB 8286A and SAB 8287A) used in an SAB 8086 system may be used in a SAB 80286 microsystem.

As indicated by the dashed lines in the figure above, the ability to add processor extensions is an integral feature of SAB 80286 microsystems. The processor extension interface allows external hardware to perform special functions and transfer data concurrently with CPU execution of other instructions. Full system integrity is maintained because the SAB 80826 supervises all data transfers and instruction execution for the processor extension. The SAB 80287 numeric processor extension (NPX), for example, uses this interface. The SAB 80287 has all the instructions and data types of an SAB 8087. The SAB 80287 NPX can perform numeric calculations and data transfers concurrently with CPU program execution. Numerics code and data have the same integrity as all other information protected by the SAB 80286 protection mechanism.

The SAB 80286 can overlap chip select decoding and address propagation during the data transfer for the previous bus operation. This information is latched into the SAB 8282A/8283A's by ALE in the middle of a TS cycle. The latched chip select and address information remains stable during the bus operation while the next cycles address is being decoded and propagated into the system. Decode logic can be implemented with a high-speed bipolar PROM.

The optional decode logic shown in the figure on basic system configuration takes advantage of the overlap between address and data of the SAB 80286 bus cycle to generate advance memory and IO-select signals. This minimizes system performance degradation caused by address propagation and decode delays. In addition to selection of memory and I/O, the advance selects may be used with configurations supporting local and system buses to enable the appropriate bus interface for each bus cycle. The COD/INTA and M/IO signals are applied to the decode logic to distinguish between interrupt, I/O, code, and data bus cycles. By adding the SAB 82289 bus arbiter chip, the SAB 80286 provides a Multibus system bus interface. A second SAB 82288 bus controller and additional latches and transceivers could be added to the local bus. This configuration allows the SAB 80286 to support an on-board bus for local memory and peripherals, and the Multibus for system bus interfacing.

Basic SAB 80286 System Configuration

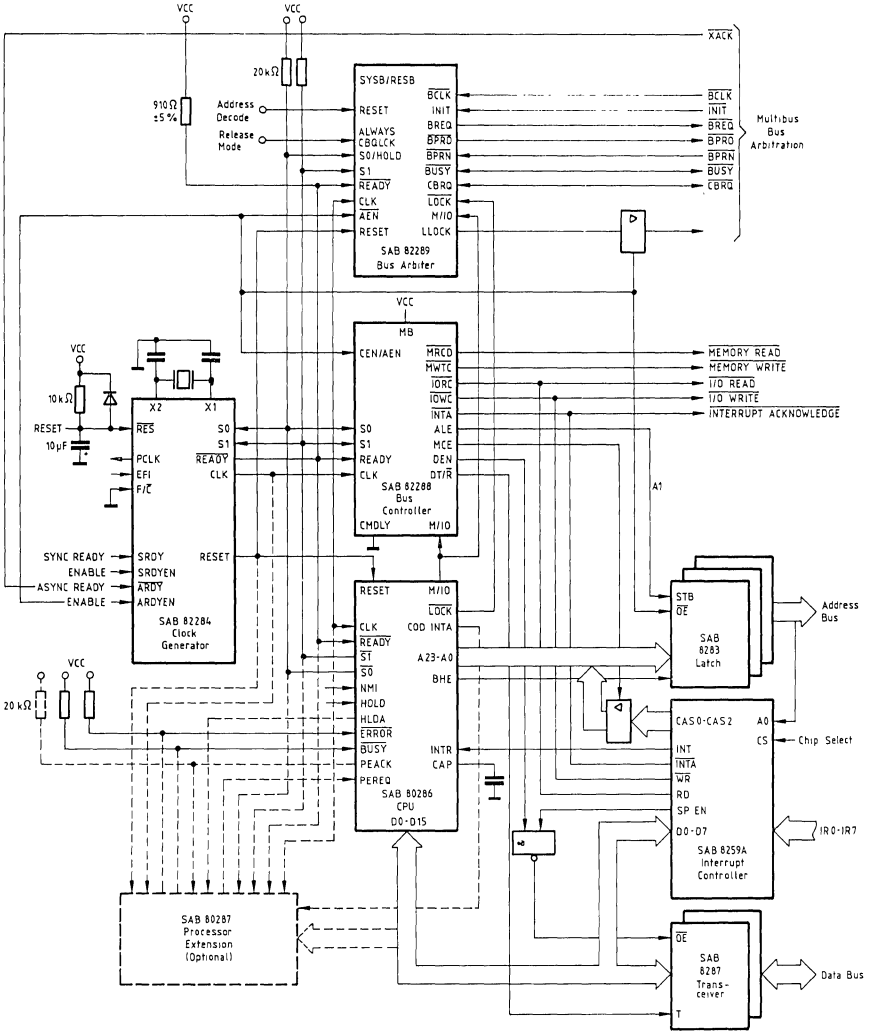


Table 13
SAB 80286 Systems, Recommended Pullup Resistor Values

SAB 80286 Pin and name	Pullup value	Purpose
4-$\overline{S1}$	20 KΩ ± 10%	Pull $\overline{S0}$, $\overline{S1}$, and $\overline{PEACK}$ inactive during SAB 80286 hold periods
5-$\overline{S0}$		
6-$\overline{PEACK}$		
53-$\overline{ERROR}$	20 kΩ ± 10%	Pull $\overline{ERROR}$ and $\overline{BUSY}$ inactive when SAB 80287 not present (or temporarily removed from socket)
54-$\overline{BUSY}$		
63-$\overline{READY}$	910 Ω ± 5%	Pull $\overline{READY}$ inactive within required minimum time CL = 150 pF, IR ≤ 7 mA)

Absolute Maximum Ratings *)

Temperature under bias	0 to +70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to ground	−1.0 to +7 V
Power dissipation	3.6 W

D.C. Characteristics

(TA = 0 to 70°C; VCC = +5 V ± 5%)

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
VIL	Input LOW voltage	−0.5	+0.8	V	–
VIH	Input HIGH voltage	2.0	VCC+0.5		
VOL	Output LOW voltage	–	0.45		IOL = 3.0 mA
VOH	Output HIGH voltage	2.4	–		IOH = 400 µA
ICC	Power supply current	–	600	mA	TA = 0°C
			390		TA = 70°C
ILI	Input leakage current		±10	µA	0 V ≤ VIN ≤ VCC
IIL	Input sustaining current on $\overline{\text{BUSY}}$ and $\overline{\text{ERROR}}$	30	500		VIN = 0 V
ILO	Output leakage current	–	±10		0.45 V ≤ VOUT ≤ VCC
ILO	Output leakage current		±1	mA	0 V ≤ VOUT ≤ 0.45 V
VCL	Clock input LOW voltage	−0.5	+0.6	V	–
VCH	Clock input HIGH voltage	3.8	VCC+1.0		
CIN	Capacitance of inputs (all input exept CLK)	–	10	pF	fc = 1 MHz
CO	Capacitance of I/O or outputs		20		
CCLK	Capacitance of CLK, $\overline{\text{READY}}$, $\overline{\text{BUSY}}$, $\overline{\text{ERROR}}$, and RESET inputs		12		

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics SAB 80286

(TA = 0 to 70°C, VCC = 5 V, ± 5%)

AC timings are referenced to 0.8 V and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
1	System clock (CLK) period	62	250	ns	–
2	System clock (CLK) LOW time	15	225		at 0.6 V
3	System clock (CLK) HIGH time	25	235		at 3.2 V
17	System clock (CLK) rise time	–	10		1.0 V to 3.5 V
18	System clock (CLK) fall time				3.5 V to 1.0 V
4	Async inputs, setup time	20	–		1)
5	Async inputs, hold time				
6	RESET setup time				–
7	RESET hold time	0			
8	Read data setup time	10			
9	Read data hold time	5			
10	$\overline{\text{READY}}$ setup time	38.5			
11	$\overline{\text{READY}}$ hold time	25			
12	Status PEACK valid delay	0	37.5		2) 3)
13	Address valid delay		60		
14	Write data valid delay		50		
15	Address/status/data float delay		60		2) 4)
16	HLDA valid delay				2) 3)

1) Asynchronous inputs are INTR, NMI, HOLD, PEREQ, $\overline{\text{ERROR}}$, and $\overline{\text{BUSY}}$. The specification is given only for testing purposes, to assure recognition at a specific CLK edge.

2) Delay from 0.8 V on the CLK to 0.8 V or 2.0 V or float on the output as apropriate for valid or floating condition.

3) Output load CL = 100 pF

4) Float condition occurs when output current is less than ILO in magnitude.

SAB 82284 Timing Requirements

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
11	$\overline{SRDY}/\overline{SRDYEN}$ setup time	15	–	ns	–
12	$\overline{SRDY}/\overline{SRDYEN}$ hold time	0			
13	$\overline{ARDY}/\overline{ARDYEN}$ setup time				1)
14	$\overline{ARDY}/\overline{ARDYEN}$ hold time	16			
19	PCLK delay	0	45		CL = 75 pF IOL = 5 mA IOH = −1 mA

1) These times are given for testing purposes to assure a predetermined action

SAB 82288 Timing Requirements

Symbol	Parameter		Limit values		Unit	Test condition
			Min.	Max.		
12	CMDLY setup time		20	–	ns	–
13	CMDLT hold time		0			
30	Command delay from CLK	Command inactive	3	20		CL = 300 pF max IOL = 32 mA max IOH = 5 mA max
29		Command active				
16	ALE active delay			15		
17	ALE inactive delay		–	20		
19	DT/$\overline{R}$ read active delay		0			
22	DT/$\overline{R}$ read inactive delay		10	40		CL = 150 pF IOL = 16 mA max IOH = −1 mA max
20	DEN read active delay					
21	DEN read inactive delay		3	15		
23	DEN write active delay		–	30		
24	DEN write inactive delay		3			

A.C. Characteristics SAB 80286-6

(TA = 0 to 70°C, VCC = 5 V, ± 5%)

AC timings are referenced to 0.8 V and 2.0 V points of signals as illustrated in data sheet waveforms, unless otherwise noted.

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
1	System clock (CLK) period	83	250	ns	–
2	System clock (CLK) LOW time	20	250		at 0.6 V
3	System clock (CLK) HIGH time	25	0		at 3.2 V
17	System clock (CLK) rise time	–	10		1.0 V to 3.5 V
18	System clock (CLK) fall time				3.5 V to 1.0 V
4	Async inputs, setup time	30	–		1)
5	Async inputs, hold time				
6	RESET setup time	25			–
7	RESET hold time	0			
8	Read data setup time	20			
9	Read data hold time	8			
10	$\overline{\text{READY}}$ setup time	50			
11	$\overline{\text{READY}}$ hold time	35			
12	Status PEACK valid delay	0	55		2) 3)
13	Address valid delay		80		
14	Write data valid delay		65		
15	Address/status/data float delay		80		2) 4)
16	HLDA valid delay				2) 3)

1) Asynchronous inputs are INTR, NMI, HOLD, PEREQ, $\overline{\text{ERROR}}$, and $\overline{\text{BUSY}}$. The specification is given only for testing purposes, to assure recognition at a specific CLK edge.

2) Delay from 0.8 V on the CLK to 0.8 V or 2.0 V or float on the output as apropriate for valid or floating condition.

3) Output load CL = 100 pF

4) Float condition occurs when output current is less than ILO in magnitude.

SAB 82284-6 Timing Requirements

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
11	$\overline{\text{SRDY}}/\overline{\text{SRDYEN}}$ setup time	25	–	ns	–
12	$\overline{\text{SRDY}}/\overline{\text{SRDYEN}}$ hold time	0			
13	$\overline{\text{ARDY}}/\overline{\text{ARDYEN}}$ setup time	5			1)
14	$\overline{\text{ARDY}}/\overline{\text{ARDYEN}}$ hold time	30			
19	PCLK delay	0	45		CL = 75 pF IOL = 5 mA IOH = −1 mA

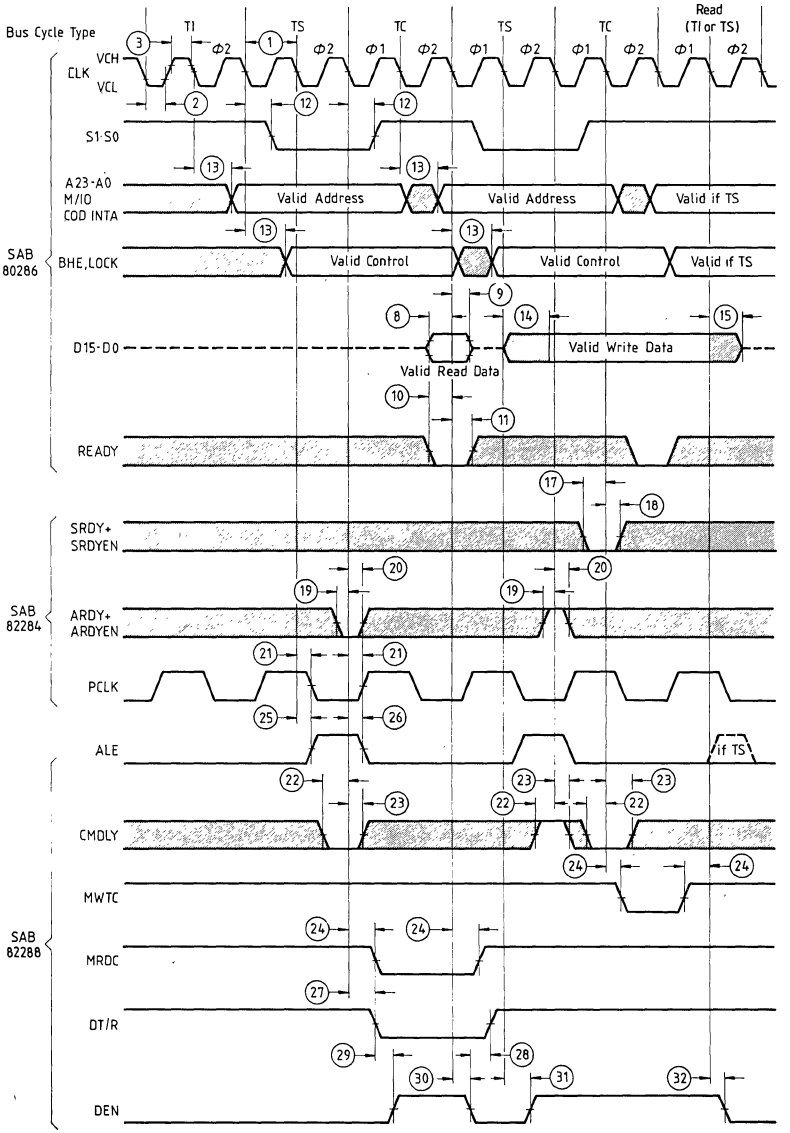
1) These times are given for testing purposes to assure a predetermined action

SAB 82288-6 Timing Requirements

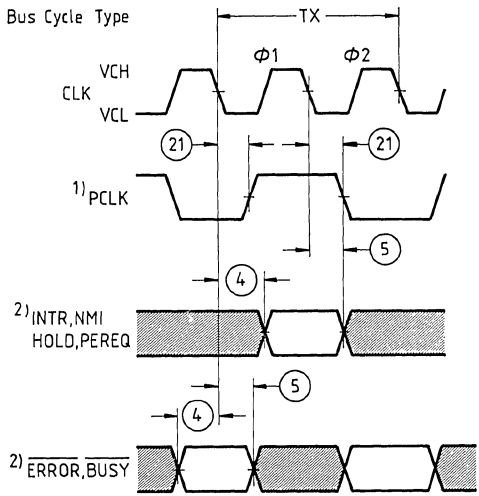
Symbol	Parameter		Limit values		Unit	Test condition
			Min.	Max.		
12	CMDLY setup time		25	–	ns	–
13	CMDLT hold time		0			
30	Command delay from CLK	Command inactive	3	30		CL = 300 pF max IOL = 32 mA max IOH = 5 mA max
29		Command active		40		
16	ALE active delay			25		
17	ALE inactive delay		–	35		
19	DT/$\overline{\text{R}}$ read active delay			40		
22	DT/$\overline{\text{R}}$ read inactive delay		5	45		CL = 150 pF IOL = 16 mA max IOH = −1 mA max
20	DEN read active delay		0	50		
21	DEN read inactive delay		3	40		
23	DEN write active delay		–	35		
24	DEN write inactive delay		3			

Waveforms

Major cycle timing



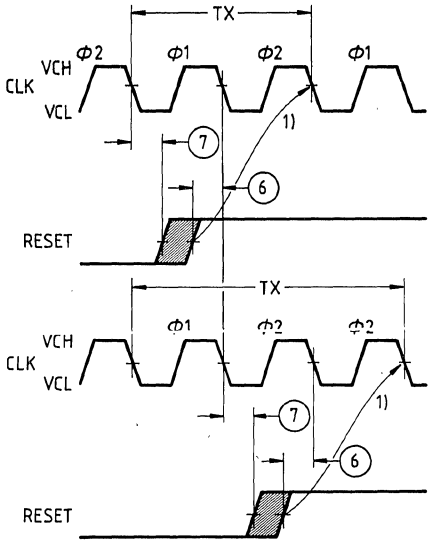
Asynchronous Input Signal Timing



1) PCLK indicates which processor cycle phase will occur on the next CLK, PCLK may not indicate the correct phase until the first bus cycle is performed.

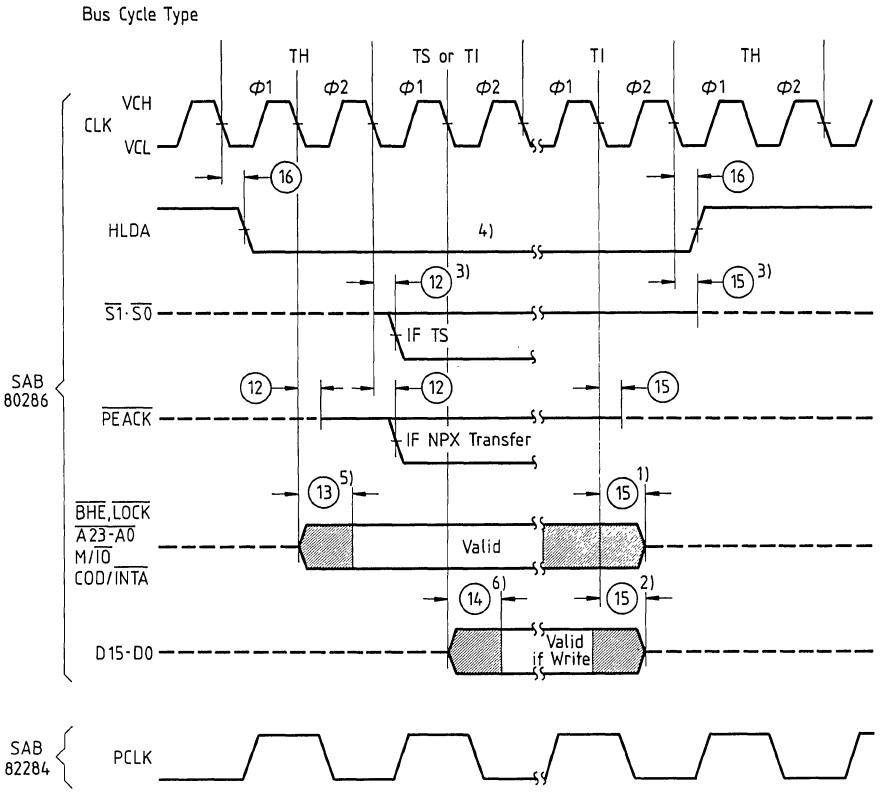
2) These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

Reset Input Timing and Subsequent Processor Cycle Phase



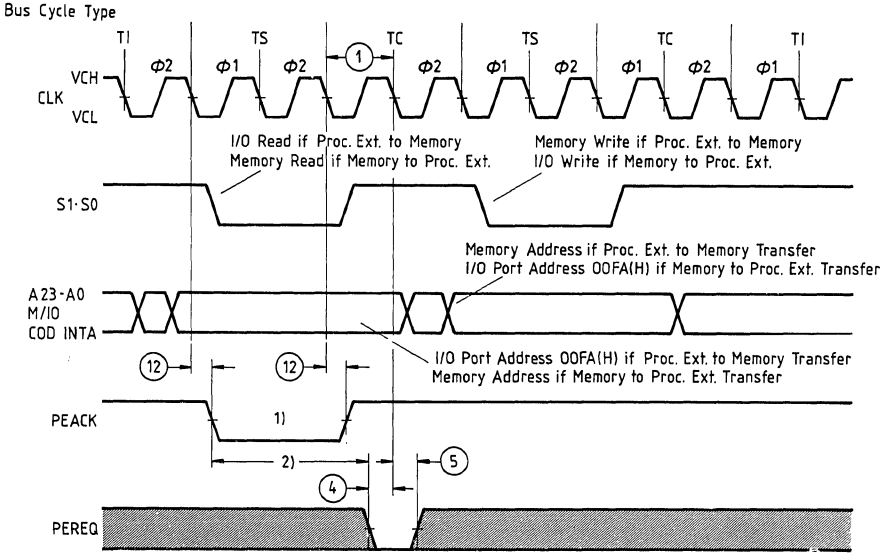
1) When RESET meets the setup time shown, the next CLK will start or repeat ∅2 of a processor cycle.

Exiting and Entering Hold



1) These signals may not be driven by the SAB 80286 during the time shown. The worst case in terms of latest float time is shown.
2) The data bus will be driven as shown if the last cycle before TI in the diagram was a write TC.
3) The SAB 80286 floats its status pins during TH. Pullup resistors in SAB 80288 keep these signals high.
4) For HOLD request set up to HLDA (refer to figure on Multibus write terminated by async ready).
5) $\overline{BHE}$ and $\overline{LOCK}$ are driven at this time but will not become valid until TS.
6) The data bus will remain in Tri-state OFF if a read cycle is performed.

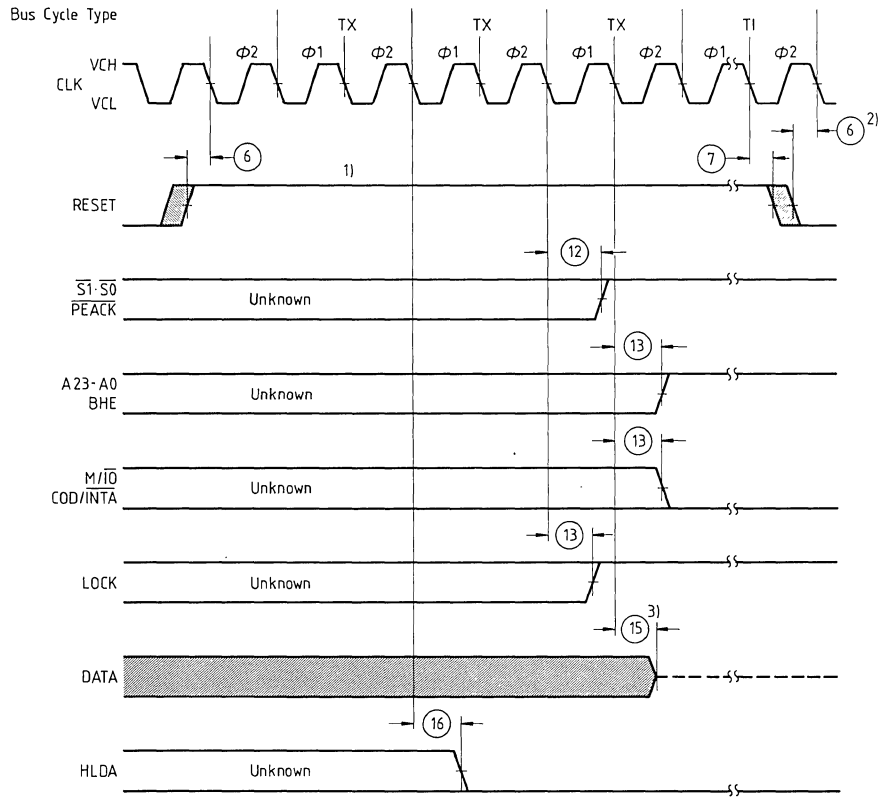
PEREQ/PEACK timing for One Transfer Only



1) $\overline{\text{PEACK}}$ always goes active during the first bus operation of a processor extension data operand transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).

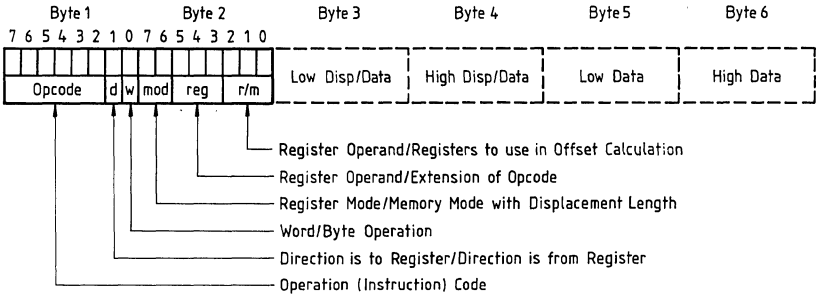
2) To prevent a second processor extension data operand transfer, the worst case maximum time (shown above) is: 3X① – ⑪ max – ④ min. The actual, configuration-dependent, maximum time is: 3X① – ⑪ max. – ④ min + AX2X①.
A is the number of extra TC states added to either the first or second bus operation of the processor extension data operand transfer sequence.

Initial SAB 80286 pin state during RESET

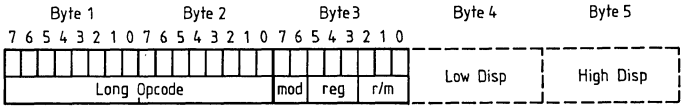


1) Setup time for RESET ↑ may be violated with the consideration that ∅1 of the processor clock may begin one system CLK period later.
2) Setup and hold times for RESET ↓ must be met for proper operation.
3) The data bus is only guaranteed to be in Tri-state OFF at the time shown.

Instruction Format Examples



A. Short Opcode Format Example



B. Long Opcode Format Example

SAB 80286 Instruction set summary

Instruction Timing Notes

The instruction clock counts listed below establish the maximum execution rate of the SAB 80286. With no delays in bus cycles, the actual clock count of an SAB 80286 program will average 5% more than the calculated clock count, due to instruction sequences which execute faster than they can be fetched from memory.

To calculate elapsed times for instruction sequences multiply the sum of all instruction clock counts, as listed in the table below, by the processor clock period. An 8 MHz processor clock has a clock period of 125 nanoseconds and requires an SAB 80286 system clock (CLK input) of 16 MHz.

Instruction Clock Count Assumptions

1. The instruction has been prefetched, decoded, and is ready for execution. Control transfer instruction clock counts include all time required to fetch, decode, and prepare the next instruction for execution.
2. Bus cycles do not require wait states.
3. There are no processor extension data transfer or local bus HOLD requests.
4. No exceptions occur during instruction execution.

Instruction Set Summary Notes

Addressing displacements selected by the MOD field are not shown. If necessary they appear after the instruction fields shown.

Above/below refers to unsigned value

Greater refers to positive signed value

Less refers to less positive (more negative) signed values

if d = 1 then to register; if d = 0 then from register

if w = 1 then word instruction; if w = 0 then byte instruction

if s = 0 then 16-bit immediate data form the operand

if s = 1 then an immediate data byte is sign-extended to form the 16-bit operand

x don't care

Z used for string primitives for comparison with ZF FLAG

If two clock counts are given, the smaller refers to a register operand and the larger refers to a memory operand

* = add one clock if offset calculation requires summing 3 elements

n = number of times repeated

m = number of bytes of code in next instruction

Level(L) – Lexical nesting level of the procedure

The following comments describe possible exceptions, side effects, and allowed usage for instructions in both operating modes of the SAB 80286.

Real address mode only

1. This is a protected mode instruction. Attempted execution in real address mode will result in an undefined opcode exception (6).
2. A segment overrun exception (13) will occur if a word operand reference at offset FFFF(H) is attempted.
3. This instruction may be executed in real address mode to initialize the CPU for protected mode.
4. The IOPL and NT fields will remain 0.
5. Processor extension segment overrun interrupt (9) will occur if the operand exceeds the segment limit.

Either mode

6. An exception may occur, depending on the value of the operand.
7. $\overline{\text{LOCK}}$ is automatically asserted regardless of the presence or absence of the LOCK instruction prefix.
8. $\overline{\text{LOCK}}$ does not remain active between all operand transfers.

Protected virtual address mode only

9. A general protection exception (13) will occur if the memory operand can not be used due to either a segment limit or access rights violation. If a stacksegment limit is violated, a stack segment overrun exception (12) occurs.
10. For segment load operations, the CPL, RPL and DPL must agree with privilege rules to avoid an exception. The segment must be present to avoid a not-present exception (11). If the SS register is the destination and a segment not-present violation occurs, a stack exception (12) occurs.
11. All segment descriptor accesses in the GDT or LDT made by this instruction will automatically assert $\overline{\text{LOCK}}$ to maintain descriptor integrity in multiprocessor systems.
12. JMP, CALL, INT, RET, IRET instructions referring to another code segment will cause a general protection exception (13) if any privilege rule is violated.
13. A general protection exception (13) occurs if CPL $\neq 0$.
14. A general protection exception (13) occurs if CPL>IOPL.
15. The IF field of the flag word is not updated if CPL>IOPL. The IOPL field is updated only if CPL = 0.
16. Any violation of privilege rules as applied to the selector operand does not cause a protection exception; rather, the instruction does not return a result and the zero flag is cleared.
17. If the starting address of the memory operand violates a segment limit, or an invalid access is attempted, a general protection exception (13) will occur before the ESC instruction is executed. A stack segment overrun exception (12) will occur if the stack limit is violated by the operand's starting address. If a segment limit is violated during an attempted data transfer then a processor extension segment overrun exception (9) occurs.
18. The destination of an INT, JMP, CALL, RET or IRET instruction must be in the defined limit of a code segment or a general protection exception (13) will occur.

Instruction Set Summary

Function	Format	Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Data Transfer					
MOV = Move:					
Register to register/memory	1000100w | mod reg r/m	2, 3 *	2, 3 *	2	9
Register/memory to register	1000101w | mod reg r/m	2, 5 *	2, 5 *	2	9
Immediate to register/memory	1100011w | mod 000 r/m | data | data if w = 1	2, 3 *	2, 3 *	2	9
Immediate to register	1011w reg | data | data if w = 1	2	2		
Memory to accumulator	1010000w | addr-low | addr-high	5	5	2	9
Accumulator to memory	1010001w | addr-low | addr-high	3	3	2	9
Register/memory to segment register	10001110 | mod 0 reg r/m	2, 5 *	17, 19 *	2	9, 10, 11
Segment register to register/memory	10001100 | mod 0 reg r/m	2, 3 *	2, 3 *	2	9
PUSH = Push:					
Memory	11111111 | mod 110 r/m	5 *	5 *	2	9
Register	01010 reg	3	3	2	9
Segment register	000 reg 110	3	3	2	9
Immediate	011010s0 | data | data if s = 0	3	3	2	9
PUSHA = Push All	01100000	17	17	2	9
POP = Pop:					
Memory	10001111 | mod 000 r/m	5 *	5 *	2	9
Register	01011 reg	5	5	2	9
Segment register	000 reg 111 (reg ≠ 01)	5	20	2	9, 10, 11

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format			Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Data Transfer (Continued)							
POPA = Pop All	01100001			19	19	2	9
XCHG = **Exchange:**							
Register/memory with register	1000011w	mod reg r/m		3, 5 *	3, 5 *	2, 7	7, 9
Register with accumulator	10010 reg			3	3		
IN = **Input from:**							
Fixed port	1110010w	port		5	5		14
Variable port	1110110w			5	5		14
OUT = **Output to:**							
Fixed port	1110011w	port		3	3		14
Variable port	1110111w			3	3		14
XLAT = Translate byte to AL	11010111			5	5		9
LEA =Load EA to register	10001101	mod reg r/m		3 *	3 *		
LDS = Load pointer to DS	11000101	mod reg r/m	(mod ≠ 11)	7 *	21 *	2	9, 10, 11
LES = Load pointer to ES	11000100	mod reg r/m	(mod ≠ 11)	7 *	21 *	2	9, 10, 11
LAHF = Load AH with flags	10011111			2	2		
SAHF = Store AH into flags	10011110			2	2		
PUSHF = Push flags	10011100			3	3	2	9
POPF = Pop flags	10011101			5	5	2, 4	2, 4

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Arithmetic					
ADD = Add:					
Reg/memory with register to either	000000dw | mod reg. r/m	2, 7 *	2, 7*	2	9
Immediate to register memory	100000sw | mod 000 r/m | data | data if s w = 01	3, 7 *	3, 7 *	2	9
Immediate to accumulator	0000010w | data | data if w = 1	3	3		
ADC = Add with carry:					
Reg memory with register to either	000100dw | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate to register/memory	100000sw | mod 010 r/m | data | data if s w = 01	3, 7 *	3, 7 *	2	9
Immediate to accumulator	0001010w | data | data if w = 1	3	3		
INC = Increment					
Register memory	1111111w | mod 000 r/m	2, 7 *	2, 7 *	2	9
Register	01000 reg	2	2		
SUB = Subtract					
Reg memory and register to either	001010dw | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate from register memory	100000sw | mod 101 r/m | data | data if s w = 01	3, 7 *	3, 7 *	2	9
Immediate from accumulator	0010110w | data | data if w = 1	3	3		
SSB = Subtract with borrow:					
Reg/memory and register to either	000110dw | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate from register/memory	100000sw | mod 011 r/m | data | data if s w = 01	3, 7 *	3, 7 *	2	9
Immediate from accumulator	0001110w | data | data if w = 1	3	3		

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Arithmetic (Continued):					
DEC = **Decrement:**					
Register memory	1 1 1 1 1 1 1 w | mod 0 0 1 r/m	2, 7 *	2, 7 *	2	9
Register	0 1 0 0 1 reg	2	2		
CMP = **Compare:**					
Register memory with register	0 0 1 1 1 0 1 w | mod reg r/m	2, 6 *	2, 6 *	2	9
Register with register/memory	0 0 1 1 1 0 0 w | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate with register memory	1 0 0 0 0 0 s w | mod 1 1 1 r/m | data | data if s w=01	3, 6 *	3, 6 *	2	9
Immediate with accumulator	0 0 1 1 1 1 w | data | data if w = 1	3	3		
NEG = Change sign	1 1 1 1 0 1 1 w | mod 0 1 1 r/m	2	7 *	2	7
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1	3	3		
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1	3	3		
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1	3	3		
DAS = Decimal adjust for substract	0 0 1 0 1 1 1 1	3	3		
MUL = Multiply (unsigned):	1 1 1 1 0 1 1 w | mod 1 0 0 r/m				
register-byte		13	13		
register-word		21	21		
memory-byte		16 *	16 *	2	9
menory-word		24 *	24 *	2	9
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w | mod 1 0 1 r/m				
register-byte		13	13		
register-word		21	21		
memory-byte		16 *	16 *	2	9
memory-word		24 *	24 *	2	9

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Arithmetic (Continued):					
IMUL = Integer immediate multiply (signed)	0 1 1 0 1 0 s 1 | mod reg r/m | data | data if s = 0	21, 24 *	21, 24 *	2	9
DIV = Divide unsigned):	1 1 1 1 0 1 1 w | mod 1 1 0 r/m				
register-byte		14	14	6	6
register-word		22	22	6	6
memory-byte		17 *	17 *	2, 6	6, 9
memory-word		25 *	25 *	2, 6	6, 9
IDIV = Integer divide (signed):	1 1 1 1 0 1 1 w | mod 1 1 1 r/m				
register-byte		17	17	6	6
register-word		25	25	6	6
memory-byte		20 *	20 *	2, 6	6, 9
memory-word		28 *	28 *	2, 6	6, 9
AMM = ASCII adjust for multiply	1 1 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0	16	16		
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1 | 0 0 0 0 1 0 1 0	14	14		
CBW = Convert byte to word	1 0 0 1 1 0 0 0	2	2		
CWD = Convert word to double word	1 0 0 1 1 0 0 1	2	2		
Logic					
Shift/Rotate Instructions:					
Register/memory by 1	1 1 0 1 0 0 0 w | mod TTT r/m	2, 7 *	2, 7 *	2	9
Register/memory by CL	1 1 0 1 0 0 1 w | mod TTT r/m	5+n, 8+n*	5+n, 8+n*	2	9
Register/memory by count	1 1 0 0 0 0 0 w | mod TTT r/m | count	5+n, 8+n*	5+n, 8+n*	2	9

TTT	Instruction
0 0 0	ROL
0 0 1	ROR
0 1 0	RCL
0 1 1	RCR
1 0 0	SHL/SAL
1 0 1	SHR
1 1 1	SAR

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Arithmetic (Continued):					
AND = And:					
Reg/memory and register to either	0 0 1 0 0 0 d w | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 0 0 r/m | data | data if w = 1	3, 7 *	3, 7 *	2	9
Immediate to accumulator	0 0 1 0 0 1 0 w | data | data f w = 1	3	3		
TEST = And function to flags, no result:					
Register/memory and register	1 0 0 0 0 1 0 w | mod reg r/m	2, 6 *	2, 6 *	2	9
Immediate data and register/memory	1 1 1 1 0 1 1 w | mod 0 0 0 r/m | data | data if w = 1	3, 6 *	3, 6 *	2	9
Immediate data and accumulator	1 0 1 0 1 0 0 w | data | data if w = 1	3	3		
OR = Or:					
Reg/memory and register to either	0 0 0 0 1 0 d w | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 0 0 1 r/m | data | data if w = 1	3, 7 *	3, 7 *	2	9
Immediate to accumulator	0 0 0 0 1 1 0 w | data | data if w = 1	3	3		
XOR = Exclusive or:					
Reg/memory and register to either	0 0 1 1 0 0 d w | mod reg r/m	2, 7 *	2, 7 *	2	9
Immediate to register/memory	1 0 0 0 0 0 0 w | mod 1 1 0 r/m | data | data if w = 1	3, 7 *	3, 7 *	2	9
Immediate to accumulator	0 0 1 1 0 1 0 w | data | data if w = 1	3	3		
NOT = Invert register/memory	1 1 1 1 0 1 1 w | mod 0 1 0 r/m	2, 7 *	2, 7 *	2	9

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
String Manipulation:					
MOVS = Move byte word	1010010w	5	5	2	9
CMPS = Compare byte/word	1010011w	8	8	2	9
SCAS = Scan byte/word	1010111w	7	7	2	9
LODS = Load byte/wd to AL/AX	1010110w	5	5	2	9
STOS = Store byte/wd from AL/A	1010101w	3	3	2	9
INS = Input byte/wd from DX port	0110110w	5	5	2	9, 14
OUTS = Output byte/wd to DX port	0110111w	5	5	2	9, 14
Repeated by count in CX					
MOVS = Move string	11110010 1010010w	5 + 4n	5 + 4n	2	9
CMPS = Compare string	1111001z 1010011w	5 + 9n	5 + 9n	2, 8	8, 9
SCAS = Scan string	1111001z 1010111w	5 + 8n	5 + 8n	2, 8	8, 9
LODS = Load string	11110010 1010110w	5 + 4n	5 + 4n	2, 8	8, 9
STOS = Store string	11110010 1010101w	4 + 3n	4 + 3n	2, 8	8, 9
INS = Input string	11110010 0110110w	5 + 4n	5 + 4n	2	9, 14
OUTS = Output string	11110010 0110111w	5 + 4n	5 + 4n	2	9, 14

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Control transfer					
CALL = Call:					
Direct within segment	11101000 | disp-low | disp-high	7 + m	7 + m	2	18
Register/memory indirect within segment	11111111 | mod 010 r/m	7+m,11+m*	7+m,11+m*	2, 8	8, 9, 18
Direct intersegment	10011010 | segment offset | segment selector	13 + m	26 + m	2	11,12,18
Protected mode only (direct intersegment):					
Via call gate to same privilege level			41 + m		8,11,12,18
Via call gate to different privilege level, no parameters			82+m		8,11,12,18
Via call gate to different privilege level, x parameters			86+4x+m		8,11,12,18
Via TSS			177+m		8,11,12,18
Via task gate			182+m		8,11,12,18
Indirect intersegment	11111111 | mod 011 r/m (mod ≠ 11)	16+n	29+n*	2	8,9,11,12,18
Protected mode only (indirect intersegment):					
Via call gate to same privileg level			44+m*		8,9,11,12,18
Via call gate different privilege level, no parameters			83+m*		8,9,11,12,13
Via call gate to different privilege level, x parameters			90+4x+m*		8,9,11,12,18
Via TSS			180+m*		8,9,11,12,18
Via task gate			185+m*		8,9,11,12,18

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Control transfer (Continued):					
JMP = Unconditional jump:					
Short/long	11101011 | disp-low	7+m	7+m		18
Direct within segment	11101001 | disp-low | disp-high	7+m	7+m		18
Register/memory indirect within segment	11101010 | mod 010 r/m	7+m,11+m*	7+m,11+m*	2	9, 18
Direct intersegment	11101010 | segment offset segment selector	11+m	23+m		11,12,18
Protected mode only (direct intersegment):					
Via call gate to same privilege level			38+m		8,11,12,18
Via TSS			175+m		8,11,12,18
Via task gate			180+m		8,11,12,18
Indirect intersegment	11111111 | mod 101 r/m (mod ≠ 11)	15+m*	26+m*	2	8,9,11,12,18
Protected mode only (indirect intersegment):					
Via call gate to same privilege level			41+m*		8,9,11,12,18
Via TSS			178+m*		8,9,11,12,18
Via task gate			183+m*		8,9,11,12,18
RET = Return from CALL:					
Within segment	11000011	11+m	11+m	2	8,9,18
Within seg adding immediate to SP	11000010 | data-low | data-high	11+m	11+m	2	8,9,18
Intersegment	11001011	15+m	25+m	2	8,9,11,12,18
Intersegment adding immediate to SP	11001010 | data-low | data-high	15+m		2	8,9,11,12,18
Protected mode only (RET):					
To different privilege level			55+m		9,11,12,18

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format		Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Control transfer (Continued):						
JE/JZ = Jump on equal/zero	01110100	disp	7+m or 3	7+m or 3		18
JL/JNGE = Jump on less/not greater equal	01111100	disp	7+m or 3	7+m or 3		18
JLE/JNG = Jump on less or equal/not greater	01111110	disp	7+m or 3	7+m or 3		18
JB/JNAE = Jump on below/not above or equal	01110010	disp	7+m or 3	7+m or 3		18
JBE/JNA = Jump on below or equal/not above	01110110	disp	7+m or 3	7+m or 3		18
JP/JPE = Jump on parity/parity even	01111010	disp	7+m or 3	7+m or 3		18
JO = Jump on overflow	01110000	disp	7+m or 3	7+m or 3		18
JS = Jump on sign	01111000	disp	7+m or 3	7+m or 3		18
JNE/JNZ = Jump on not equal/not zero	01110101	disp	7+m or 3	7+m or 3		18
JNL/JGE = Jump on not less/greater or equal	01111101	disp	7+m or 3	7+m or 3		18
JNLE/JG = Jump on not less or equal/greater	01111111	disp	7+m or 3	7+m or 3		18
JNB/JAE = Jump on not below/above or equal	01110011	disp	7+m or 3	7+m or 3		18
JNBE/JA = Jump on not below or equal/above	01110111	disp	7+m or 3	7+m or 3		18
JNP/JPO = Jump on not par/par odd	01111011	disp	7+m or 3	7+m or 3		18
JNO = Jump on not overflow	01110001	disp	7+m or 3	7+m or 3		18
JNS = Jump on not sign	01111001	disp	7+m or 3	7+m or 3		18
LOOP = Loop CX times	11100010	disp	8+m or 4	8+m or 4		18
LOOPZ/LOOPE = Loop while zero/equal	11100001	disp	8+m or 4	8+m or 4		18
LOOPNZ/LOOPNE = Loop while not zero/equal	11100000	disp	8+m or 4	8+m or 4		18
JCXZ = Jump on CX zero	11100011	disp	8+m or 4	8+m or 4		18

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Control transfer (Continued):					
ENTER = Enter procedure	11001000 | data-low | data-high | L			2, 8	8, 9
L = 0		11	11	2, 8	8, 9
L = 1		15	15	2, 8	8, 9
L > 1		16+4(L-1)	16+4(L-1)	2, 8	8, 9
LEAVE = Leave procedure	11001001	5	5	2, 8	8, 9
INT = **Interrupt:**					
Type specified	11001101 | type	23+m		2, 7, 8	
Type 3	11001100	23+m		2, 7, 8	
INTO = Interrupt on overflow	11001110	24+m or 3 (3 if no interrupt)	(3 if no interrupt)	2, 6, 8	
Protected mode only:					
Via interrupt or trap gate to same privilege level			40+m		7,8,11,12,18
Via interrupt or trap gate to fit different privilege level			78+m		7,8,11,12,18
Via Task Gate			167+m		7,8,11,12,18
IRET = Interrupt return	11001111	17+m	31+m	2, 4	8,9,11,12,15,18
Protected mode only:					
To different privilege level			55+m		8,9,11,12,15,18
To different task (NT = 1)			169+m		8,9,11,12,18
BOUND = Detect value out of range	01100010 | mod reg r/m	13 *	13 * (Use INT clock count if exception 5)	2, 6	6,8,9,11,12,18

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Processor Control					
CLC = Clear carry	11111000	2	2		
CMC = Complement carry	11110101	2	2		
STC = Set carry	11111001	2	2		
CLD = Clear direction	11111100	2	2		
STD = Set direction	11111101	2	2		
CLI = Clear interrupt	11111010	3	3		14
STI = Set interrupt	11111011	2	2		14
HLT = Halt	11110100	2	2		13
WAIT = Wait	10011011	3	3		
LOCK = Bus lock prefix	11110000	0	0		14
CTS = Clear task switched flag	00001111 00000110	2	2	3	13
ESC = Processor extension escape	11011TTT mod LLL r/m (TTT LLL are opcode to processor extension)	9-20 *	9-20 *	5, 8	8, 17
SEG = Segment override prefix	001 reg 110	0	0		

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Function	Format	Clock Count: Real address mode	Clock Count: Protected virtual address mode	Comments: Real address mode	Comments: Protected virtual address mode
Protection Control					
LGDT = Load global descriptor table register	00001111 | 00000001 | mod 010 r/m	11 *	11 *	2, 3	9, 13
SGDT = Store global descriptor table register	00001111 | 00000001 | mod 000 r/m	11 *	11 *	2, 3	9
LIDT = Load interrupt descriptor table register	00001111 | 00000001 | mod 011 r/m	12 *	12 *	2, 3	9, 13
SIDT = Store interrupt descriptor table register	00001111 | 00000001 | mod 001 r/m	12 *	12*	2, 3	9
LLDT = Load local descriptor table register from register memory	00001111 | 00000000 | mod 010 r/m		17, 19 *	1	9, 11, 13
SLDT = Store local descriptor table register to register/memory	00001111 | 00000000 | mod 000 r/m		2, 3 *	1	9
LTR = Load task register from register/memory	00001111 | 00000000 | mod 011 r/m		17, 19 *	1	9, 11, 13
STR=Store task register to register memory	00001111 | 00000000 | mod 001 r/m		2, 3*	1	9
LMSW = Load machine status word from register/memory	00001111 | 00000001 | mod 110 r/m	3, 6 *	3, 6 *	2,3	9, 13
SMSW = Store machine status word	00001111 | 00000001 | mod 100 r/m	2, 3 *	2, 3 *	2, 3	9
LAR = Load access rights from register/memory	00001111 | 00000010 | mod reg r/m		14, 16 *	1	9, 11, 16
LSL = Load segment limit from register/memory	00001111 | 00000011 | mod reg r/m		14, 16 *	1	9, 11, 16
ARPL = Adjust requested privilege level: from register/memory	01100011 | mod reg r/m		10*, 11*	2	8, 9
VERR = Verify read access: register/memory	00001111 | 00000000 | mod 100 r/m		14, 16 *	1	9, 11, 16
VERW = Verify write access:	00001111 | 00000000 | mod 101 r/m		14, 16*	1	9, 11, 16

Shaded areas indicate instructions not available in SAB 8086, 8088 microsystems.

Notes:

The effective address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (Before data if required)

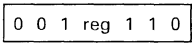
* except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

REG is assigned according to the following table:

16-bit (w = 1)	8-bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 DI

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

segment override prefix



reg is assigned according to the following:

reg	Segment register
00	ES
01	CS
10	SS
11	DS

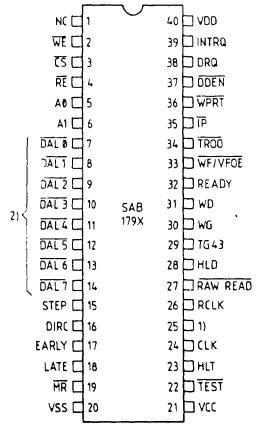
Peripheral and Support Components

SAB 179X
Floppy Disk Formatter/ Controller Family

FEATURES	SAB 1791	SAB 1793	SAB 1795	SAB 1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

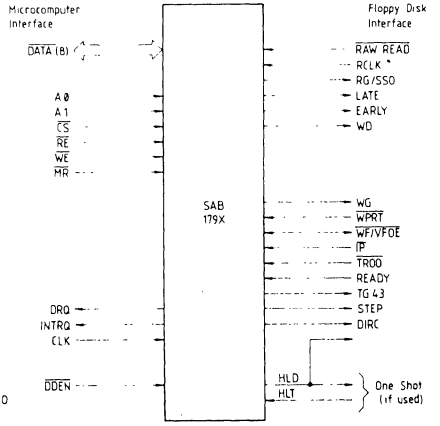
- Two VFO Control Signals-RG & VFOE
- Soft Sector Format Compatibility
- Automatic Track Seek with Verification
- Accomodates Single and Double Density Formats
  IBM 3740 Single Density (FM)
  IBM System 34 Double Density (MFM)
- Read Mode
  Single/Multiple Sector Read with Automatic Search or Entire Track Read
  Selectable 128 Byte or Variable length Sector
- Write Mode
  Single/Multiple Sector Write with Automatic Sector Search
  Entire Track Write for Diskette Formatting
- System Compatibility
  Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  DMA or Programmed Data Transfers
  All Inputs and Outputs are TTL Compatible
  On-Chip Track and Sector Registers/Comprehensive Status Information
- Programmable Controls
  Selectable Track to Track Stepping Time
  Side Select Compare
- Write Precompensation
- Window Extension
- Incorprorates Encoding/Decoding and Address Mark Circuitry
- For 8" and 5¼" Floppy Disks
- Compatible with Industry Standard 179X

Pin Connections



1) SAB 1791/1793 = RG, SAB 1795/7 = SSO
2) SAB 1793/SAB 1797 = True Bus

Logic Diagram



SAB 179X is a floppy disk controller family of N-channel MOS LSI components designed to interface with SAB 8080/8085/8086/8051 family processors. Its flexibility and ease of use makes it an ideal floppy disk interface between conventional floppy disks and all computer systems.

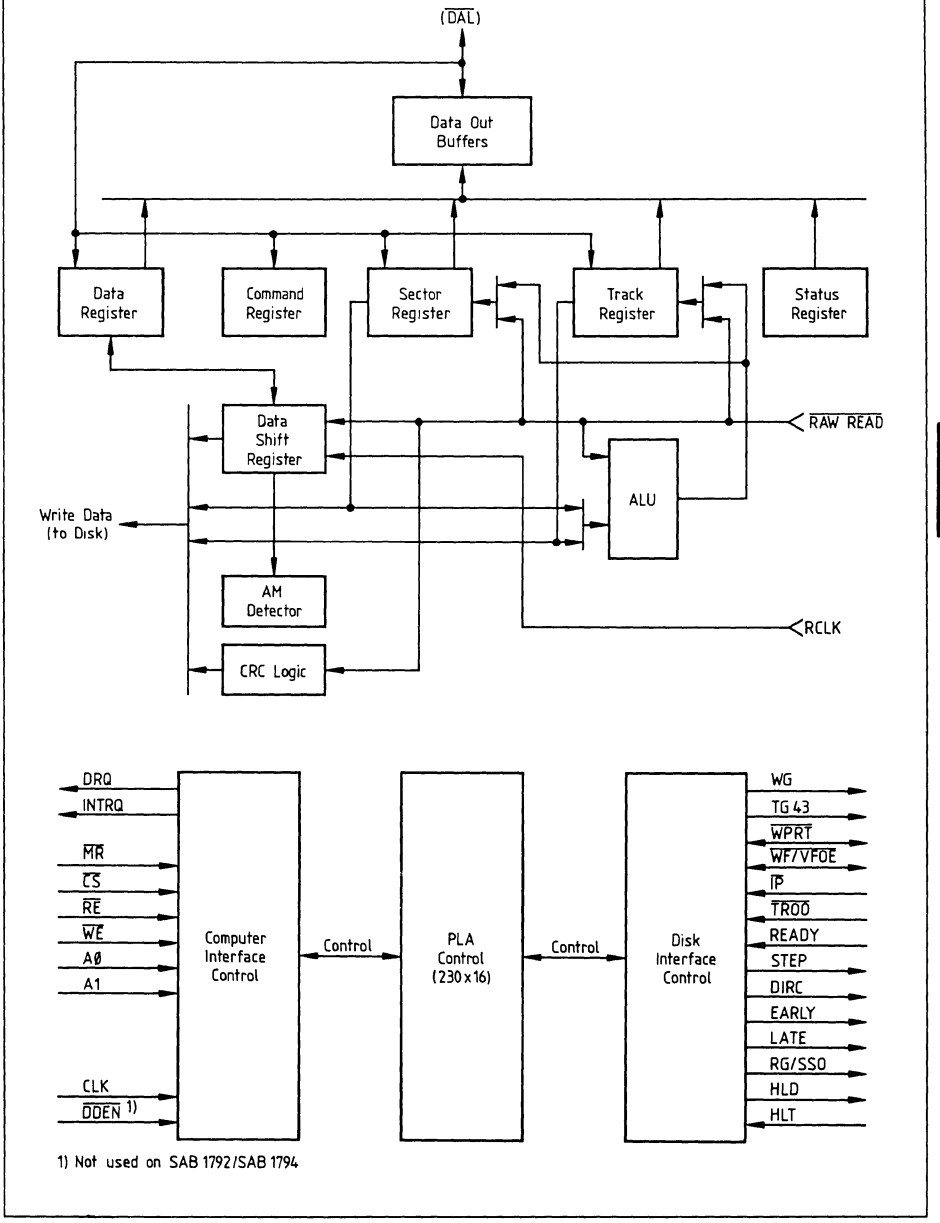
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
NC	1	–	NO CONNECTION – Pin 1 is internally connected to a back bias generator and must be left open by the user.
$\overline{MR}$	19	I	$\overline{MASTER\ RESET}$ - A logic low (50μs min.) on this input resets the device and loads HEX Ø3 into the command register. The Not Ready (Status Bit 7) is reset during MR ACTIVE. When MR is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX Ø1 is loaded into sector register.
$\overline{WE}$	2	I	$\overline{WRITE\ ENABLE}$ – A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
$\overline{CS}$	3	I	$\overline{CHIP\ SELECT}$ - A logic low on this input selects the chip and enables computer communication with the device.
$\overline{RE}$	4	I	$\overline{READ\ ENABLE}$ – A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
AØ, A1	5,6	I	REGISTER SELECT LINES – These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: $\overline{CS}$ A1 AØ $\overline{RE}$ $\overline{WE}$ Ø Ø Ø Status Reg Command Reg Ø Ø 1 Track Reg Track Reg Ø 1 Ø Sector Reg Sector Reg Ø 1 1 Data Reg Data Reg
$\overline{DALØ}$ to $\overline{DAL7}$	7 to 14	I/O	$\overline{DATA\ ACCESS\ LINES}$ - Eight bit inverted (SAB 1791/5) or true (SAB 1793/7) bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by WE or transmitter enabled by $\overline{RE}$. Drive capability is 1 TTL Load
CLK	24	I	CLOCK – This input requires a free-running square wave clock for internal timing reference. 2 MHz ± 1% with 50% duty cycle. 1 MHz ± 1% for mini-floppies.
DRQ	38	O	DATA REQUEST – This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5V.
INTRQ	39	O	INTERRUPT REQUEST – This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5V.
STEP	15	O	STEP – The step output contains a pulse for each step.
DIRC	16	O	DIRECTION – Direction Output is active high when stepping in, active low when stepping out.
EARLY	17	O	EARLY – Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
LATE	18	O	LATE – Indicates that the write data pulse occuring while Late is active (high) should be shifted late for write precompensation.

Symbol	Number	Input (I) Output (O)	Function
$\overline{\text{TEST}}$	22	I	$\overline{\text{TEST}}$ – This input is used for testing purposes only and should be tied to + 5V or left open by the user unless interfacing to voice coil actuated motors.
HLT	23	I	HEAD LOAD TIMING – When a logic high is found on the HLT input the head is assumed to be engaged.
RG	25	O	READ GATE (SAB 1791/3) – A high level on this output indicates to the data separator circuitry that 2 bytes of zeros in single density, or 4 bytes of either zeros or ones in double density have been encountered, and is used for synchronization.
SSO	25	O	SIDE SELECT OUTPUT (SAB 1795/1797) – The logic level of the Side Select Output is directly controlled by the ‚S' flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = Ø, SSO is set to a logic Ø. The SSO is compared with side information in the sector ID field. If they do not compare, status bit 4 (RNF) is set. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic Ø upon a MASTER RESET condition.
RCLK	26	I	READ CLOCK – A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i. e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
$\overline{\text{RAW READ}}$	27	I	$\overline{\text{RAW READ}}$ – The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
HLD	28	O	HEAD LOAD – The HLD output controls the loading of the Read-Write head against the media.
TG43	29	O	TRACK GREATER THAN 43 – This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
WG	30	O	WRITE GATE – This output is made valid before writing is to be performed on the diskette.
WD	31	O	WRITE DATA – A 200 ns (MFM) or 500 ns (FM) output pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
READY	32	I	READY – This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
$\overline{WF/VFOE}$	33	I/O	$\overline{WRITE\ FAULT\ VFO\ ENABLE}$ – This is a bidirectional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = Ø, any write command will immediately be terminated. When WG = Ø, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the SAB 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the SAB 1791/3, VFOE will remain low until the end of the Data Field. This pin has an internal 100 kOhm pull-up resistor.
TRØØ	34	I	$\overline{TRACK\ ØØ}$ – This input informs the SAB 179X that the Read/Write head is positioned over Track ØØ.
IP	35	I	$\overline{INDEX\ PULSE}$ – This input informs the SAB 179X when the index hole is encountered on the diskette
WPRT	36	I	$\overline{WRITE\ PROTECT}$ – This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
$\overline{DDEN}$	37	I	$\overline{DOUBLE\ DENSITY}$ – This pin selects either single or double density operation. When $\overline{DDEN}$ = Ø, double density is selected. When $\overline{DDEN}$ = 1, single density is selected.
VCC	21	–	POWER SUPPLY (+5 V).
VDD	40	–	POWER SUPPLY (+12 V).
VSS	20	–	GROUND (0 V)



1) Not used on SAB 1792/SAB 1794

General Description

The SAB 179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The SAB 179X is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation.
The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The SAB 179X is set up to operate on a multiplexed bus with other bus-oriented devices. The SAB 179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The SAB 1793 is identical to the SAB 1791 except the DAL lines are TRUE for systems that utilize true data busses.
The SAB 1795/7 has a side select output for controlling double sided drives.

Organization

The Floppy Disk Formatter block diagram is illustrated on previous page. The primary sections include the parallel processor interface and the Floppy Disk interface.
Data Shift Register – This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.
Data Register – This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operation information is transferred in parallel from the Data Register to the Data Shift Register.
When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.
Track Register – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track ØØ). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.
Sector Register (SR) – This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.
Command Register (CR) – This 8-bit register holds the command presently being executed.This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.
Status Register (STR) – This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.
CRC Logic – This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.
The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.
Arithmetic/Logic Unit (ALU) – The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.
Timing and Control – All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.
The SAB 179X has two different modes of operation according to the state of $\overline{\text{DDEN}}$. When $\overline{\text{DDEN}} = Ø$ double density (MFM) is assumed. When $\overline{\text{DDEN}} = 1$, single density (FM) is assumed.
AM Detector – The address mark detector detects ID, data and index address marks during read and write operations.

Processor Interface

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the SAB 179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.
When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and AØ, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-AØ	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
ØØ	Status Register	Command Register
Ø1	Track Register	Track Register
1Ø	Sector Register	Sector Register
11	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the SAB 179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.
On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.
On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.
At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the Status Register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.
Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are:

Operation	Next Operation	Delay Req'd.[1] FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit Ø)	12 µs	6 µs
Write to Command Reg.	Read Status Bits 1-7	28 µs	14 µs
Write Any Register	Read From Diff. Register	Ø	Ø

[1] Times double for CLK=1MHz (Minifloppies)

Floppy Disk Interface

The SAB 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

Head Positioning

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and Ø of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock.If $\overline{TEST}$ = Ø, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.
The rates can be applied to a Step-Direction Motor through the device interface.

Step – A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.
Direction (DIRC) – The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12μs before the first stepping pulse is generated.
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The SAB 179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

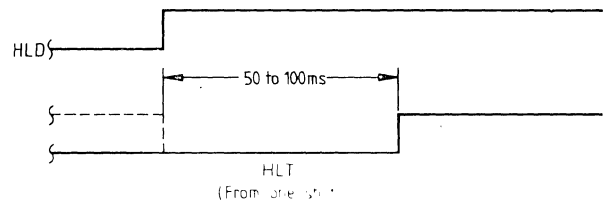
Stepping Rates

CLK $\overline{DDEN}$ R1 R0	2 MHz Ø $\overline{TEST}$=1	2 MHz 1 $\overline{TEST}$=1	1 MHz Ø $\overline{TEST}$=1	1 MHz 1 $\overline{TEST}$=1	2 MHz x $\overline{TEST}$=Ø	1 MHz x $\overline{TEST}$=Ø
R1						
Ø Ø	3 ms	3 ms	6 ms	6 ms	184 μs	368 μs
Ø 1	6 ms	6 ms	12 ms	12 ms	190 μs	380 μs
1 Ø	10 ms	10 ms	20 ms	20 ms	198 μs	396 μs
1 1	15 ms	15 ms	30 ms	30 ms	208 μs	416 μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = Ø and V = Ø); or if the SAB 179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the SAB 179X which is used for the head engage time. When HLT = 1, the SAB 179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the SAB 179X.

Head Load Timing



When both HLD and HLT are true, the SAB 179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.
In summary for the Type I commands: if h = Ø and V = Ø, HLD is reset. If h = 1 and V = Ø, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = Ø and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the SAB 179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the SAB 179X then waits for HLT to occur.
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

General Disk Read Operations

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "Ø." Sector lengths are determined at format time by the fourth byte in the "ID" field.

Sector Length Table*)	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
ØØ	128
Ø1	256
Ø2	512
Ø3	1024

*) SAB 1795/97 may vary – see command summary.

The number of sectors per track as far as the SAB 179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the SAB 179X is concerned is from Ø to 255 tracks.
For read operations in 8" double density the SAB 179X requires $\overline{RAW\ READ}$ Data (Pin 27) signal which is a 200 ns pulse per flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase locked loop, one shots, or counter techniques. In addition a Read Gate Signal is provided as an output (Pin 25) on SAB 1791 93 which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM, RG is made true when 2 bytes of zeroes are detected. The SAB 179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the SAB 179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "ØØ" or "FF" are detected. The SAB 179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.
During read operations (WG = Ø), the $\overline{VFOE}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{VFOE}$ will got active low when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The SAB 179X is inspecting data off the disk

If $\overline{WF}/\overline{VFOE}$ is not used, this pin may be left open, as it has an internal pull-up resistor.

General Disk Write Operations

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the SAB 179X before the Write Gate signal can be activated.
Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The $\overline{Write\ Fault}$ input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the SAB 179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The $\overline{Write\ Fault}$ input should be made inactive when the Write Gate output becomes inactive.

For write operations, the SAB 179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{DDEN}$ = 1) and 200 ns pulses in MFM ($\overline{DDEN}$ = Ø). Write Data provides the unique address marks in both formats.
Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written EARLY. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the SAB 179X The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

Ready

Whenever a Read or Write command (Type II or III) is received the SAB 179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

Command Description

The SAB 179X accepts eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit Ø). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types.
Commands and types are summarized on next page.

Status Register

Upon receipt of any command, except, the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The user has the option of reading the status register through program control or using the DRQ line with DMA or interrupt methods. When the Data register is read the DRQ bit in the status register and the DRQ line are automatically reset. A write to the Data register also causes both DRQ's to reset.

The busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the status register to determine the condition of busy will reset the INTRQ line.

(Bits)							
7	6	5	4	3	2	1	Ø
S7	S6	S5	S4	S3	S2	S1	SØ

Status varies according to the type of command executed.

Command Summary

Commands for SAB 1791, SAB 1793										Commands for SAB 1795, SAB 1797								
		Bits								Bits								
Type	Command	7	6	5	4	3	2	1	Ø	7	6	5	4	3	2	1	Ø
I	Restore	Ø	Ø	Ø	Ø	h	V	r_1	$r_Ø$	Ø	Ø	Ø	Ø	h	V	r_1	$r_Ø$
I	Seek	Ø	Ø	Ø	1	h	V	r_1	$r_Ø$	Ø	Ø	Ø	1	h	V	r_1	$r_Ø$
I	Step	Ø	Ø	1	T	h	V	r_1	$r_Ø$	Ø	Ø	1	T	h	V	r_1	$r_Ø$
I	Step-in	Ø	1	Ø	T	h	V	r_1	$r_Ø$	Ø	1	Ø	T	h	V	r_1	$r_Ø$
I	Step-out	Ø	1	1	T	h	V	r_1	$r_Ø$	Ø	1	1	T	h	V	r_1	$r_Ø$
II	Read Sector	1	Ø	Ø	m	S	E	C	Ø	1	Ø	Ø	m	L	E	U	Ø
II	Write Sector	1	Ø	1	m	S	E	C	$a_Ø$	1	Ø	1	m	L	E	U	$a_Ø$
III	Read Address	1	1	Ø	Ø	Ø	E	Ø	Ø	1	1	Ø	Ø	Ø	E	U	Ø
III	Read Track	1	1	1	Ø	Ø	E	Ø	Ø	1	1	1	Ø	Ø	E	U	Ø
III	Write Track	1	1	1	1	Ø	E	Ø	Ø	1	1	1	1	Ø	E	U	Ø
IV	Force Interrupt	1	1	Ø	1	I_3	I_2	I_1	$I_Ø$	1	1	Ø	1	I_3	I_2	I_1	$I_Ø$

Flag Summary

Command Type	Bit No(s)		Description
I	Ø, 1	r_1 $r_Ø$ = Stepping Motor Rate	
I	2	V = Track Number Verify Flag	V = Ø, No verify V = 1, Verify on destination track
I	3	h = Head Load Flag	h = Ø, Unload head at beginning h = 1, Load head at beginning
I	4	T = Track Update Flag	T = Ø, No update T = 1, Update track register
II & III	Ø	$a_Ø$ = Data Address Mark	$a_Ø$ = Ø, FB (DAM) $a_Ø$ = 1, F8 (deleted DAM)
II	1	C = Side Compare Flag	C = Ø, Disable side compare C = 1, Enable side compare
II & III	1	U = Update SSO	U = Ø, Update SSO to Ø U = 1, Update SSO to 1
II & III	2	E = 15 ms Delay	E = Ø, No 15 ms delay E = 1, 15 ms delay
II	3	S = Side Compare Flag	S = Ø, Compare for side Ø S = 1, Compare for side 1
II	3	L = Sector Length Flag L = 1 (implicit) for SAB 1791/3	
II	4	m = Multiple Record Flag	m = Ø, Single record m = 1, Multiple records
IV	Ø-3	I_x = Interrupt Condition Flags $I_Ø$ = 1 Not Ready To Ready Transition I_1 = 1 Ready To Not Ready Transition I_2 = 1 Index Pulse I_3 = 1 Immediate Interrupt, Requires A Reset I_3-I_1 = Ø Terminate With No Interrupt (INTRQ)	

	LSB's Sector Length in ID Field			
	ØØ	Ø1	10	11
L = Ø	256	512	1024	128
L = 1	128	256	512	1024

Status Register Summary

Bit	All Type I Commands	Read Address	Read Sector	Read Track	Write Sector	Write Track
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	Ø	Ø	Ø	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	Ø	RECORD TYPE	Ø	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	Ø	RNF	Ø
S3	CRC ERROR	CRC ERROR	CRC ERROR	Ø	CRC ERROR	Ø
S2	TRACK Ø	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
SØ	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

Status for Type I Commands

Bit	Name	Meaning
S7	NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically "ored" with MR.
S6	PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5	HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to Ø when updated.
S3	CRC ERROR	CRC encountered in ID field.
S2	TRACK ØØ	When set, indicates Read/Write head is positioned to Track Ø. This bit is an inverted copy of the $\overline{TRØØ}$ input.
S1	INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
SØ	BUSY	When set command is in progress. When reset no command is in progress.

Status for Type II and III Commands

Bit	Name	Meaning
S7	NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and "ored" with MR. The Type II and III Commands will not execute unless the drive is ready.
S6	WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5	RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. Ø = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4	RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
SØ	BUSY	When set, command is under execution. When reset, no command is under execution.

Formatting the Disk

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command.

Upon receipt of the Write Track command, the head is loaded and the Busy Status bis is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the SAB 179X detects a data pattern of F5 through FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation.

The CRC generator is initialized when any data byte from F8 to FE is about to be tranferred from the DR to the DSR in FM or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 through FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F 7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

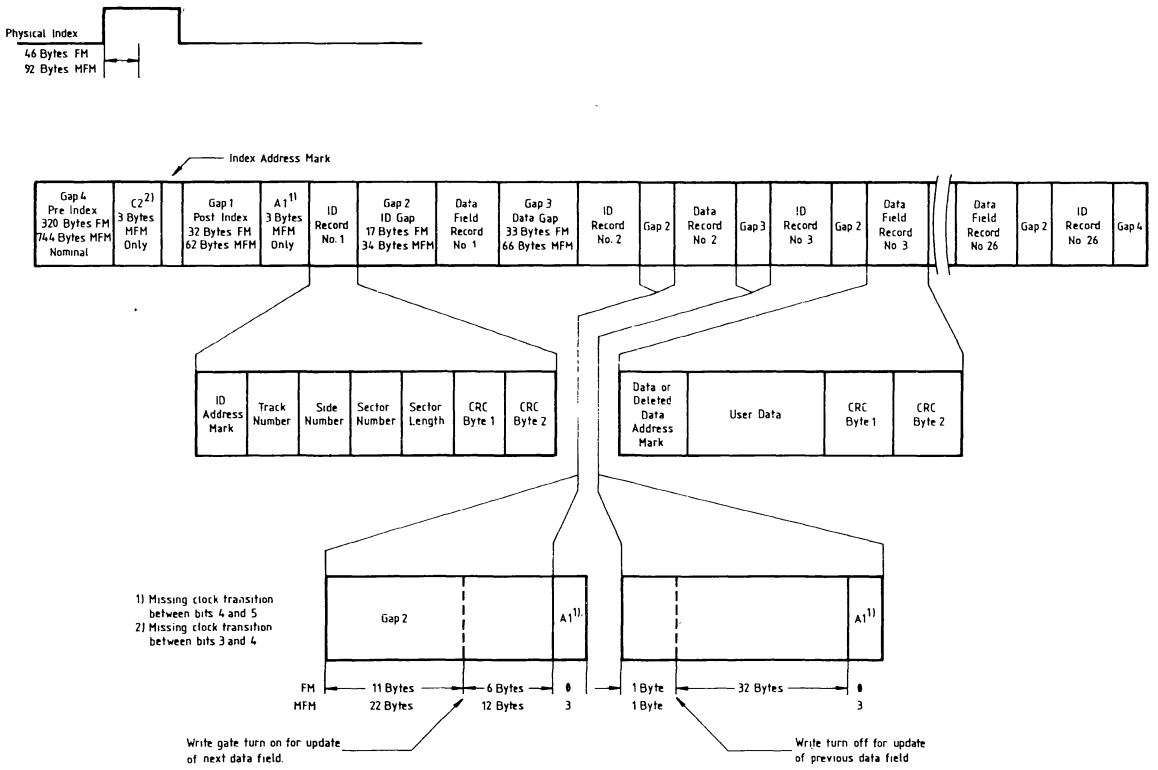
IBM 3740 Format – 128 Bytes/Sector (8")

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	FF (or ØØ)[3]
6	ØØ
1	FC (Index Mark)
26	FF (or ØØ)
[1] 6	ØØ
1	FE (ID Address Mark)
1	Track Number
1	Side Number (ØØ or Ø1)
1	Sector Number (1 thru 1A)
1	ØØ
1	F7 (2 CRC's written)
11	FF (or ØØ)
6	ØØ
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or ØØ)
247[2]	FF (or ØØ)

[1] Write bracketed field 26 times
[2] Continue writing until SAB 179X interrupts out. Approx. 247 bytes.
[3] Optional 'ØØ' on SAB 1795/7 only.

IBM Track Format



IBM System 34 Format 256 Bytes/Sector (8")

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex value of Byte written
80	4E
12	Ø0
3	F6 (writes C2)
1	FC (Index Mark)
50 [1]	4E
12	Ø0
3	F5
1	FE (ID Address Mark)
1	Track Number (Ø through 4C)
1	Side Number (Ø or 1)
1	Sector Number (1 through 1A)
1	Ø1 (Sector length)
1	F7 (2 CRCs written)
22	4E
12	Ø0
3	F5 (writes A1)
1	FB (Data Adress Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598 [2]	4E

[1] Write bracketed field 26 times
[2] Continue writing until SAB179X interrupts out. Approx. 598 bytes.

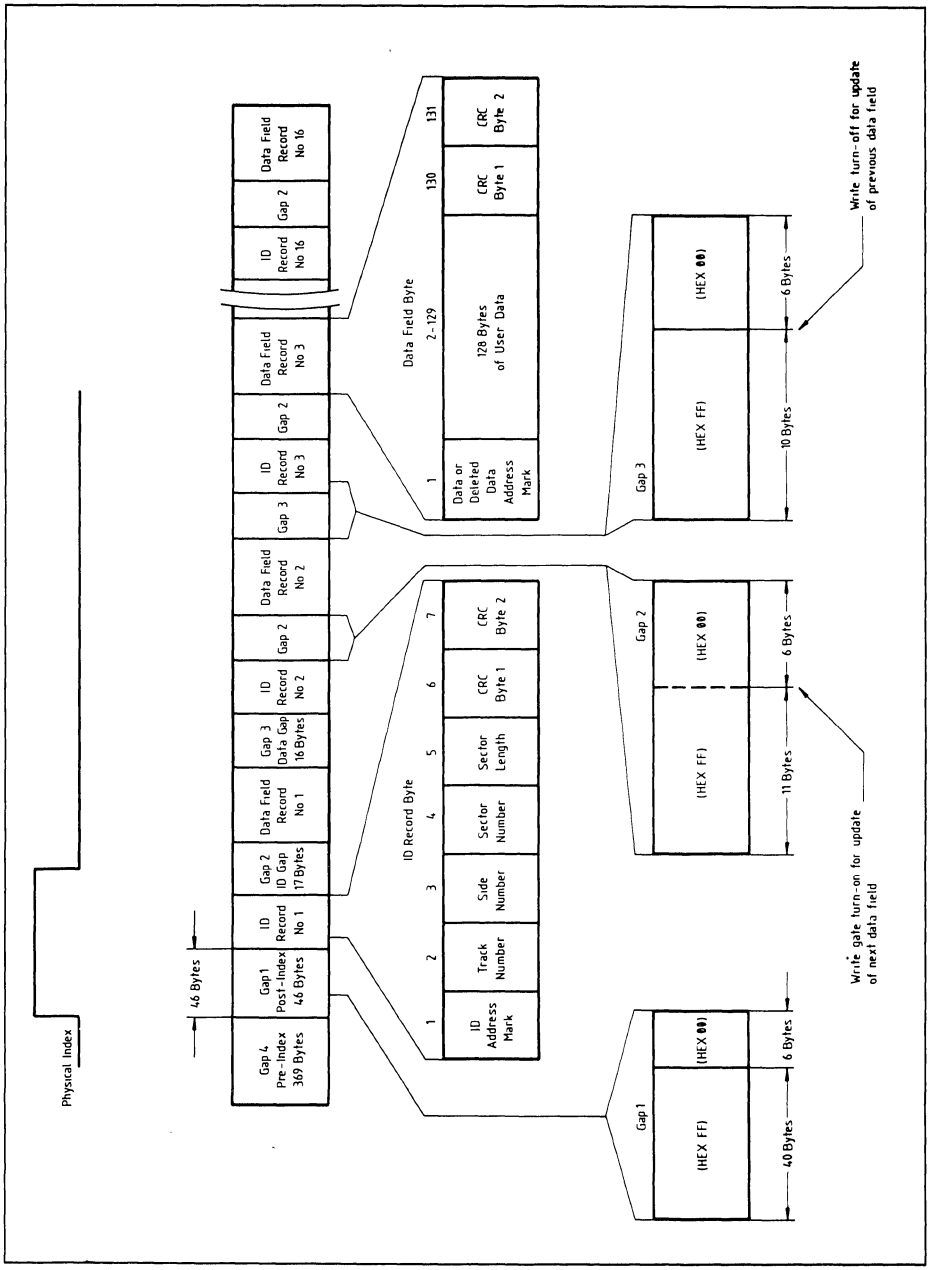
Recommended — 128 Bytes/Sector (Mini-Diskette)

Shown below is the Recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40 [1]	FF (or Ø0) [3]
6	Ø0
1	FE (ID Address Mark)
1	Track Numer
1	Side Number (Ø0 or Ø1)
1	Sector Number (1 through 1A)
1	Ø0 (Sector length)
1	F7 (2 CRC's written)
11	FF (or Ø0) [3]
6	Ø0
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
10	FF (or Ø0) [3]
369 [2]	FF (or Ø0) [3]

[1] Write bracketed field 16 times
[2] Continue writing until SAB 179X interrupts out. Approx 369 bytes.
[3] Optional 'Ø0' on SAB 1795/7 only.

Recommended Single Density Format (Mini-Diskette)



256 Bytes/Sector (Mini-Diskette)

Shown below is the recommended dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex value of Byte written
60	4E
12	ØØ
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (Ø through 4C)
1	Side Number (Ø or 1)
1	Sector Number (1 through 1A)
1	Ø1 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	ØØ
3	F5 (Writes A1)
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
24	4E
718[2]	4E

[1] Write bracketed field 26 times
[2] Continue writing until SAB 179X interrupts out. Approx. 718 bytes.

Non-standards Formats

Variations in the recommended formats are possible to a limited extent if the following requirements are met:

1) Sector size must be 128, 256, 512 of 1024 bytes.
2) Gap 2 cannot be varied from the recommended format.
3) 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the SAB 179X. Gap 1, 3, and 4 lengths can be as short as 2 bytes for SAB 179X operation, however PPL lock up time, motor speed variation, write-splice area, etc. will add more bytes to each gap to achieve proper operation. It is recommended that the recommended format be used for highest system reliability.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
[3]	6 bytes ØØ	12 bytes ØØ
		3 bytes A1
Gap III	10 bytes FF	24 bytes 4E
[4]	4 bytes ØØ	8 bytes ØØ
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

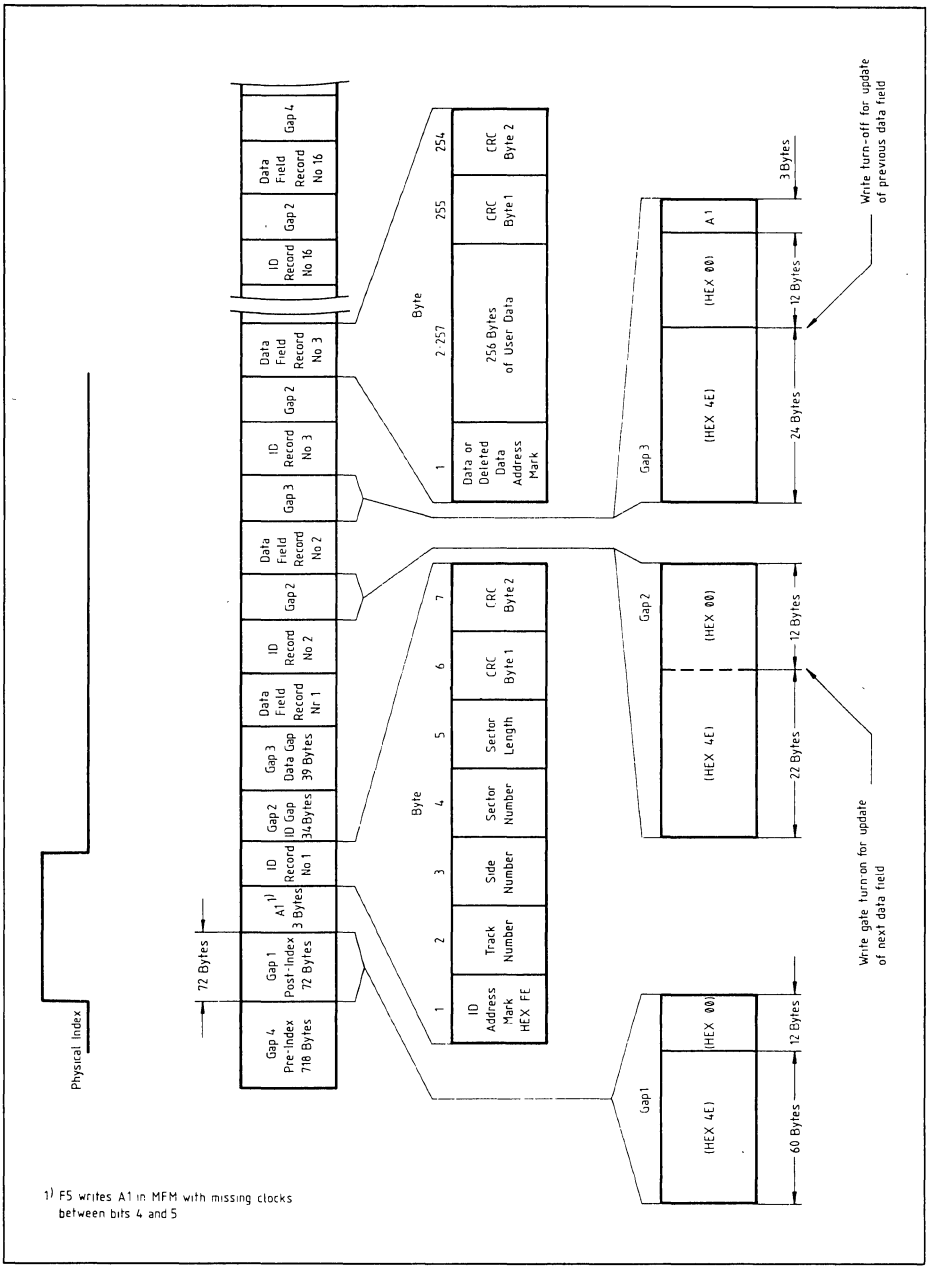
[3] Byte counts must be exact.
[4] Byte counts are minimum, except exactly 3 bytes of A1 must be written in MFM.

Control Bytes for Initialization

Data Pattern in DR (Hex.)	SAB 179X Interpretation in FM (DDEN = 1)	SAB 179X Interpretation in MFM (DDEN = Ø)
ØØ through F4	Write ØØ through F4 with CLK = FF	Write ØØ through F4, in MFM
F5	Not Allowed	Write A1[1] in MFM, Preset CRC
F6	Not Allowed	Write C2[2] in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 through FB	Write F8 through FB, Clk = C7, Preset CRC	Write F8 through FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Present CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

[1] Missing clock transition between bits 4 and 5
[2] Missing clock transition between bits 3 and 4

Recommended Double Density Format (Mini-Diskette)



Absolute maximum ratings[1)]

Operating Temperature	0 to 70°C
Storage Temperature	−65 to +150°C
VDD with Respect to Vss (Ground)	+15 to −0.3 V
Max. Voltage to any Input with Respect to VSS	+15 to −0.3 V

D. C. Characteristics

TA = 0 to 70° C; VDD = +12 V ± 5%; VCC = +5V ± 5%; VSS = OV

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
IIL	Input Leakage	–		10	µA	VIN = VDD[2)]
IOL	Output Leakage					VOUT = VDD
VIH	Input High Voltage	2.6	–	–	V	–
VIL	Input Low Voltage	–		0.8		
VOH	Output High Voltage	2.8		–		IO = −100 µA
VOL	Output Low Voltage			0 45		IO = 1.6mA
ICC	Power Supply Current	–	35	60	mA	–
IDD	Power Supply Current		10	15		
PD	Power Dissipation		–	0 6	W	

Capacitance[3)]

Symbol	Parameter	Limit Value (max.)	Unit	Test Condition
CIN	Input Capacitance	15	pF	Unmeasured pins returned to GND
COUT	Output Capacitance			

[1)] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2)] Leakage conditions are for input pins without internal pull-up resistors.

[3)] This parameter is periodically sampled and not 100% tested.

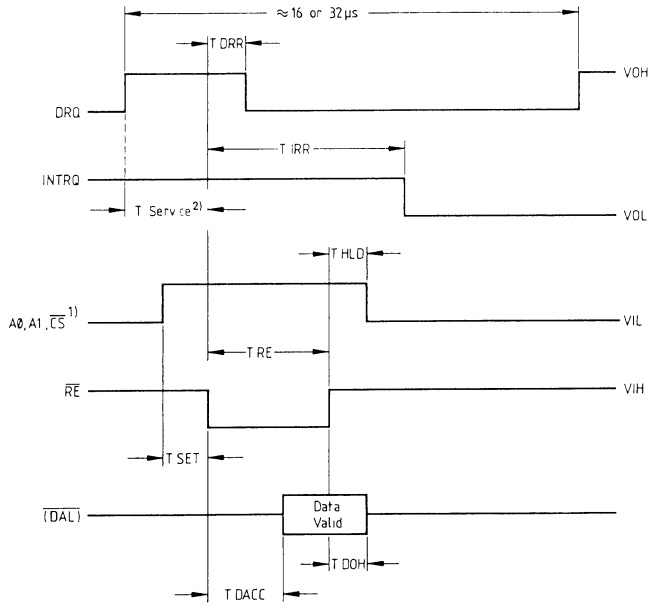
A.C. Characteristics

TA = 0 to 70° C, VDD = +12 V ± 5%; VSS = 0V, VCC = +5V ± 5%

All timing readings at VOL 0.8 V and VOH 2.0 V

Read Enable Timing

Symbol	Parameter	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
TSET	Setup ADDR & CS to $\overline{RE}$	50	–	–	ns	–
THLD	Hold ADDR & CS from $\overline{RE}$	10				
TRE	$\overline{RE}$ Pulse Width	400				CL = 50pf
TDRR	DRQ Reset from $\overline{RE}$	–	400	500		–
TIRR	INTRQ Reset from $\overline{RE}$		500	3000		
TDACC	Data Access from $\overline{RE}$		–	350		CL = 50pf
TDOH	Data Hold from $\overline{RE}$	50		150		



DRQ rising edge: Indicates that the data register has assembled data.
DRQ falling edge: Indicates that the data register was read.
INTRQ rising edge: Occurs at end of command.
INTRQ falling edge: Indicates that the status register was read.

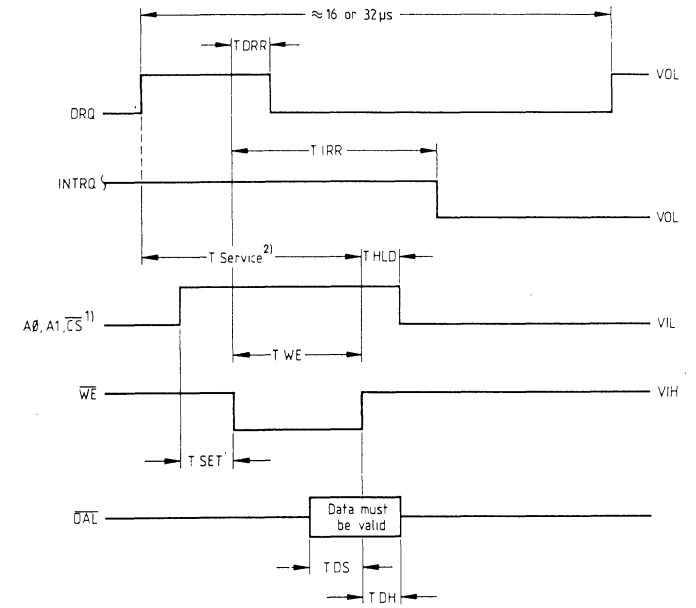
1) $\overline{CS}$ may be permanently tied LOW if desired.

2) T Service (worst case)
– FM = 27.5 µs
– MFM = 13.5 µs

3) Times double when CLK = 1MHz

Write Enable Timing

Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
TSET	Setup ADDR & CS to $\overline{WE}$	50				
THLD	Hold ADDR & CS from $\overline{WE}$	10	–	–		
TWE	$\overline{WE}$ Pulse Width	350			ns	–
TDRR	DRQ Reset from $\overline{WE}$	–	400	500		
TIRR	INTRQ Reset from $\overline{WE}$		500	3000		
TDS	Data Setup to $\overline{WE}$	250	–	–		
TDH	Data Hold from $\overline{WE}$	70				



DRQ rising edge: Indicates that the data register is empty.
DRQ falling edge: Indicates that the data register is loaded.
INTRQ rising edge: Indicate the end of a command.
INTRQ falling edge: Indicates that the command register is written to.

[1] CS may be permanently tied LOW if desired. When writing Data into Sector Track or Data Register User cannot read this Register until at least 4µs in MFM after the rising edge of WE when writing into the command Register Status is not valid until some 28µs in FM, 14 µs in MFM later.

[2] T Service (worst case); FM = 23.5 µs; MFM = 11.5 µs

[3] Times double when CLK=1MHz

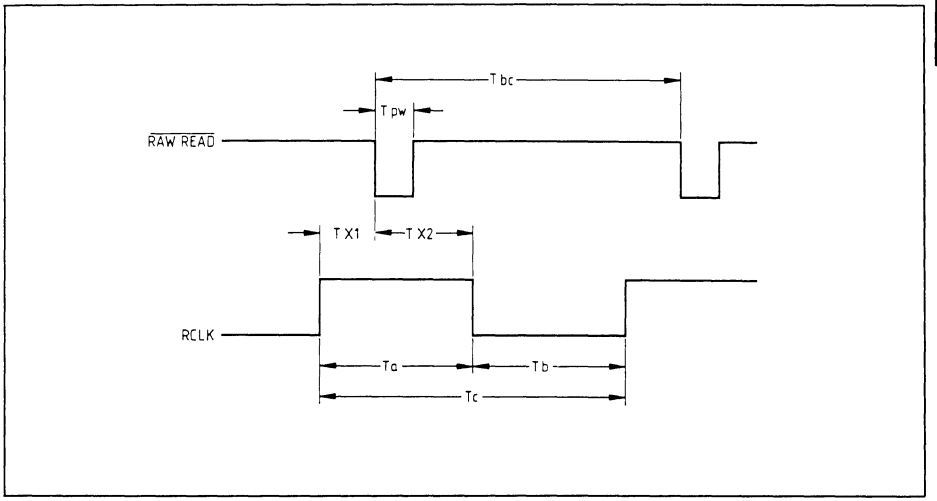
Input Data Timing

Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
Tpw	$\overline{\text{RAW READ}}$ Pulse Width	100	200	–	ns	1)
Tbc	$\overline{\text{RAW READ}}$ Cycle Time[2]	1500	2000	–	ns	1800 ns @ 70°C
Tc	RCLK Cycle Time[3]					
Tx1	RCLK hold to $\overline{\text{RAW READ}}$	40	–	–	ns	1)
Tx2	$\overline{\text{RAW READ}}$ hold to RCLK					1)

[1] Pulse width on RAW READ (Pin 27) is normally 100 – 300ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300ns for MFM at CLK = 2MHz and 600ns for FM at 2MHz. Times double for 1MHz.

[2] tbc should be 2 μs, nominal in MFM and 4 μs nominal in FM. Times double when CLK = 1 MHz.

[3] RCLK may be high or low during $\overline{\text{RAW READ}}$ (Polarity is unimportant).

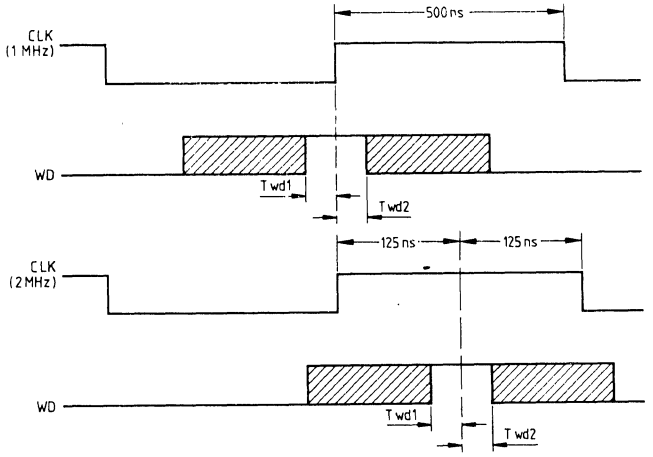


				Nominal		
Diskette	Mode	$\overline{\text{DDEN}}$	CLK	Ta	Tb	Tc
8"	MFM	Ø	2 MHz	1 μs	1 μs	2 μs
8"	FM	1	2 MHz	2 μs	2 μs	4 μs
5"	MFM	Ø	1 MHz	2 μs	2 μs	4 μs
5"	FM	1	1 MHz	4 μs	4 μs	8 μs

A PPL Data Separator is recommended for 8" MFM

Write Data Timing (All Times Double when CLK = 1 MHz)

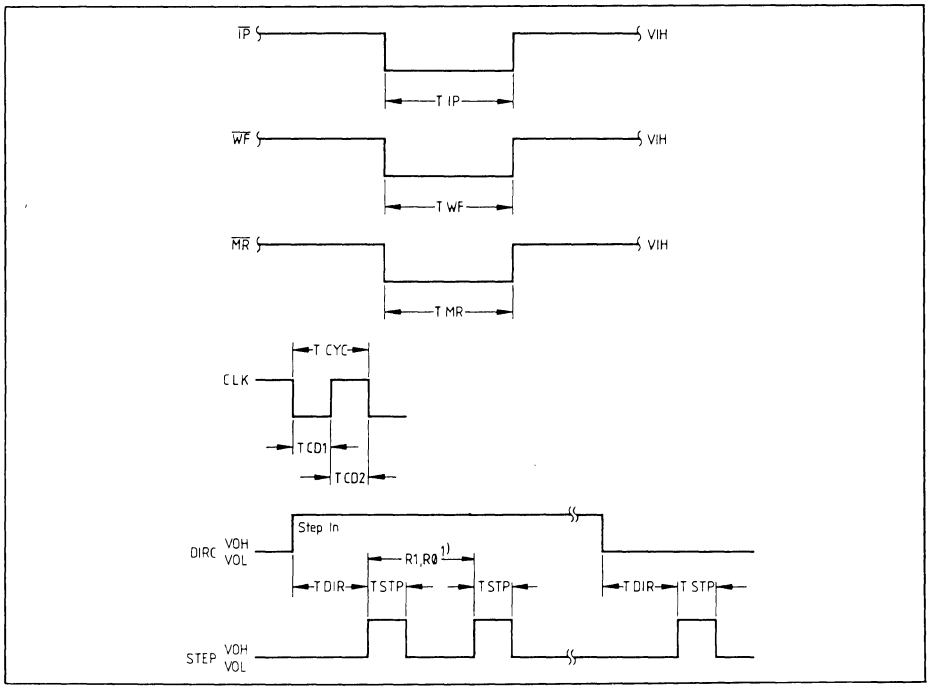
Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
Twp	Write Data Pulse Width	450 150	500 200	550 250	ns	FM MFM
Twg	Write Gate to Write Data	–	2 1	–	µs	FM MFM
Tbc	Write data cycle Time		2,3 or 4			± CLK Error
Ts	Early (Late) to Write Data	125			ns	MFM
Th	Early (Late) from Write Data					
Twf	Write Gate off from WD	–	2 1	–	µs	FM MFM
Twd1	WD Valid to CLK	100 50	–		ns	CLK = 1MHz CLK = 2MHz
Twd2	WD Valid after CLK	100 30				CLK = 1MHz CLK = 2MHz



Write Data/Clock Relationship ($\overline{DDEN}$ = Ø)
WD must have rising edge in first shaded area and trailing edge in second shaded area

Miscellaneous Timing

Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
TCD1	Clock Duty (LOW)	230		20000	ns	2)
TCD2	Clock Duty (HIGH)	200				
TSTP	Step Pulse Output	2 or 4	–	–	μs	± CLK Error
TDIR	Dir Setup to Step	–	12			
TMR	Master Reset Pulse Width	50				2)
TIP	Index Pulse Width	10	–			
TWF	Write Fault Pulse Width	20				



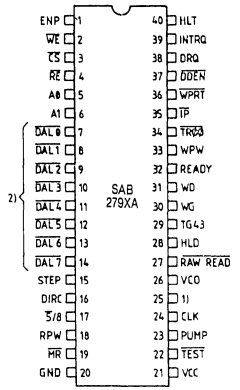
1) From step rate table.
2) Times double when CLK=1MHz

SAB 279XA Floppy Disk Formatter/ Controller Family

Features	SAB 2791A	SAB 2793A	SAB 2795A	SAB 2797A
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Side Select Output			X	X
Internal CLK Divide	X	X		

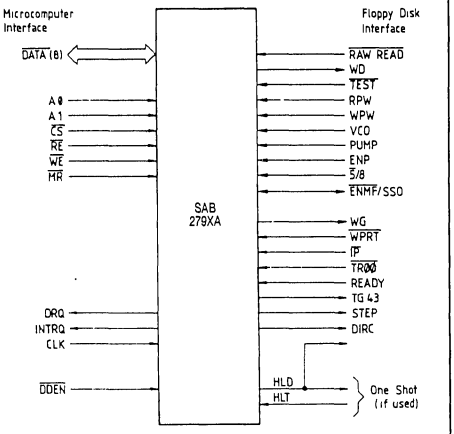
- On-Chip PLL Data Separator
- On-Chip Write Precompensation Logic
- Single +5V Supply
- Accommodates Single and Double Density Formats
  IBM 3740 Single Density (FM)
  IBM System 34 Double Density (MFM)
- Automatic Seek with Verify
- Multiple Sector Read/Write
- TTL Compatible
- Programable Control
  Selectable Track-to-Track Access
  Head Load Timing
- Software Compatible with the SAB 179X Floppy Disk Formatter/Controller Family
- Soft Sector Format Compatibility

Pin Connections



1) SAB 2791A/2793A = $\overline{\text{ENMF}}$ 2) SAB 2793A/2797A = True Bus
SAB 2795A/2797A = SSO

Logic Diagram



SAB 279XA is a floppy disk controller family of N-channel MOS LSI components designed to interface with SAB 8080/8051 family processors. Its flexibility and ease of use makes it an ideal floppy disk interface between conventional floppy disks and all computer systems. Software compatible with its predecessor, the SAB 179X, the device also contains a high performance Phase-Lock-Loop Data Separator as well as Write Precompensation Logic.
When operating in Double Density mode, Write Precompensation is automatically engaged to a value programmed via an external potentiometer. An on-chip VCO and phase comparator allows adjustable frequency range for 5¼"-8" Floppy Disk and Micro Floppy Disk Interface.

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Functions
ENP	1	I	ENABLE PRECOMP – A logic high on this input enables write precompensation to be performed on the Write Data output
$\overline{WE}$	2	I	$\overline{WRITE\ ENABLE}$ – A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low
$\overline{CS}$	3	I	$\overline{CHIP\ SELECT}$ – A logic low on this input selects the chip and enables computer communication with the device
$\overline{RE}$	4	I	$\overline{READ\ ENABLE}$ – A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low
A0, A1	5,6	I	REGISTER SELECT LINES – These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control:
$\overline{DAL0}$ to $\overline{DAL7}$	7–14	I/O	$\overline{DATA\ ACCESS\ LINES}$ – Eight bit directional bus used for transfer of commands, status and data. These lines are inverted on SAB 2791A and SAB 2795A.
STEP	15	O	STEP – The step output contains a pulse for each step
DIRC	16	O	DIRECTION – Direction output is active high when stepping in, active low when stepping out
$\overline{5}/8$	17	I	$5\,^1/_4$", 8" SELECT – This input selects the internal VCO frequency for use with $5\,^1/_4$" drives or 8" drives
RPW	18	I	READ PULSE WIDTH – An external potentiometer tied to this input controls the phase comparator within the data separator
$\overline{MR}$	19	I	$\overline{MASTER\ RESET}$ – A logic low (50 μsec min.) on this input resets the device and loads hex 03 into the command register. The Not Ready bit (Status bit 7) is reset during $\overline{MR}$ active. When $\overline{MR}$ is brought to a logic high a Restore command is executed, regardless of the state of the Ready signal from the drive. Also hex 01 is loaded into Sector Register.
$\overline{TEST}$	22	I	$\overline{TEST}$ – A logic low on this input allows adjustment of external resistors by enabling internal signals to appear on selected pins

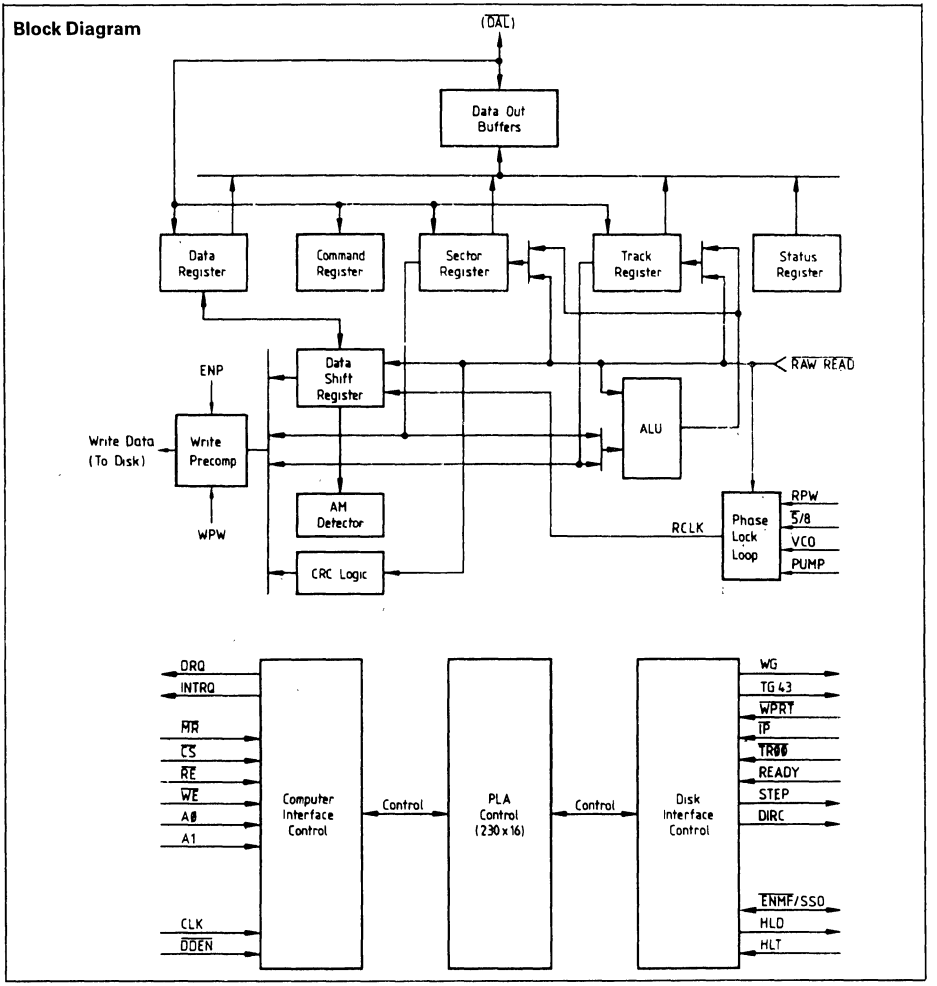
$\overline{CS}$	A1	A0	$\overline{RE}$	$\overline{WE}$
0	0	0	Status Register	Command Register
0	0	1	Track Register	Track Register
0	1	0	Sector Register	Sector Register
0	1	1	Data Register	Data Register

Symbol	Number	Input (I) Output (O)	Functions
PUMP	23	0	PUMP – High-impedance output signal which is forced high or low to increase/decrease the VCO frequency
CLK	24	I	CLOCK – This input requires a free-running 50% duty cycle square wave clock for internal timing reference, 2 MHz ±1% for 8" drives, 1 MHz ±1% for mini-floppies
$\overline{\text{ENMF}}$	25	I	$\overline{\text{ENABLE MINI-FLOPPY}}$ (SAB 2791A/2793A)— A logic low on this input enables an internal divide by 2 of the master clock. This allows both $5^1/_4$" and 8" drive operation with a single 2 MHz clock. For a 1 MHz clock on Pin 24, this line must be left open or tied to a logic 1
SSO	25	O	SIDE SELECT OUTPUT (SAB 2795A/2797A)— The logic level of the Side Select output is directly controlled by the U flag in Type II or III commands. When U = 1, SSO is set to a logic 1. When U = Ø, SSO is set to a logic Ø. The SSO is compared with the side information in the sector ID field. If they do not compare, Status Bit 4 (RNF) is set. The Side Select output is only updated at the beginning of a Type II or III command. It is forced to a logic Ø upon a master reset condition
VCO	26	–	VOLTAGE CONTROLLED OSCILLATOR – An external capacitor tied to this pin adjusts the VCO center frequency
$\overline{\text{RAW READ}}$	27	I	$\overline{\text{RAW READ}}$ – The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition
HLD	28	O	HEAD LOAD – The HLD output controls the loading of the Read/Write head against the media
TG43	29	O	TRACK GREATER THAN 43 – This output informs the drive that the Read/Write head is positioned between tracks 44 and 76. This output is valid only during read and write commands
WG	30	O	WRITE GATE – This output is made valid before writing is to be performed on the diskette
WD	31	O	WRITE DATA – MFM or FM output pulse per flux transition. WD contains the unique address marks as well as data and clock in both FM and MFM formats
READY	32	I	READY – This input indicates disk readiness and is sampled for a logic high before read or write commands are performed. If Ready is low the read or write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Functions
WPW	33	I	WRITE PRECOMP WIDTH – An external potentiometer tied to this input controls the amount of delay in write precompensation mode
$\overline{TR00}$	34	I	$\overline{TRACK\ 00}$ – This input informs the SAB 279XA that the Read/Write head is positioned over Track 00
$\overline{IP}$	35	I	$\overline{INDEX\ PULSE}$ – This input informs the SAB 279XA when the index hole is encountered on the diskette
$\overline{WPRT}$	36	I	$\overline{WRITE\ PROTECT}$ – This input is sampled whenever a write command is received. A logic low terminates the command and sets the Write Protect status bit
$\overline{DDEN}$	37	I	$\overline{DOUBLE\ DENSITY}$ – This input pin selects either single or double density operation. When $\overline{DDEN}$ = 0, double density is selected. When $\overline{DDEN}$ = 1, single density is selected
DRQ	38	O	DATA REQUEST – This output indicates that the Data Register contains assembled data in read operations, or the DR is empty in write operations. This signal is reset when serviced by the computer through reading or loading the Data Register
INTRQ	39	O	INTERRUPT REQUEST – This output is set at the completion of any command and is reset when the Status Register is read or the Command Register is written to
HLT	40	I	HEAD LOAD TIMING – When a logic high is found on the HLT input the head is assumed to be engaged. It is typically derived from a single shot triggered by HLD
VCC	21	–	POWER SUPPLY (+5V)
VSS	20	–	GROUND (0V)

Block Diagram



General Description

The SAB 279XA are N-channel MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The SAB 279XA is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The SAB 297XA contains all the features of its predecessor, the SAB 179X, plus a high performance phase-lock-lopp data separator as well as write precompensation logic. In double density mode, write precompensation is automatically engaged to a value programmed via an external potentiometer. In order to maintain compatibility, the SAB 179X and SAB 279XA designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical in each case, the actual pin assignments vary only by a few pins from any one to another.
The processor interface consists of an 8-bit bi-directional bus for data, status, and control word transfers. The SAB 279XA is set up to operate on a multiplexed bus with other bus-oriented devices. The SAB 279XA is TTL compatible on all inputs and outputs. The outputs will drive one TTL load or three LS loads. The SAB 2793A is identical with the SAB 2791A, except that the DAL lines are true for systems that utilize true data busses.
The SAB 2795A/97A has a side select output for controlling double sided drives.

Organization

The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register (DSR) – This 8-bit register assembles serial data from the Read Data input (RAW READ) during read operations and transfers serial data to the Write Data output during write operations.

Data Register (DR)– This 8-bit register is used as a holding register during disk read and write operations. In disk read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In disk write operations information is transferred in parallel from the Data Register to the Data Shift Register. When executing the Seek command the Data Register holds the address of the desired track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register (TR) – This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk read, write and verify operations. The Track Register can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Sector Register (SR) – This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk read or write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) – This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a Force Interrupt command. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) – This 8-bit register holds device status information. The meaning of the status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic – This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$
The CRC includes all information starting with the address mark und up to the CRC character. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) – The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control – All computer and Floppy Disk interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

AM Detector – The address mark detector detects ID, data and index address marks during read and write operations.

Write Precompensation – enables write precompensation to be performed on the Write Data output.

Data Separator – a high performance phase-lock-loop data separator with on-chip VCO and phase comparator allows adjustable frequency range for $5^1/_4$" or 8" Floppy Disk interfacing.

Processor Interface

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer data, status, and control words out of, or into the SAB 279XA. The DAL are three state buffers that are enabled as output drivers when Chip Select ($\overline{CS}$) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.
When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a read operation or $\overline{WE}$ during a write operation are interpreted as selector for the following registers:

A1	A0	READ	WRITE
0	0	Status Register	Command Register
0	1	Track Register	Track Register
1	0	Sector Register	Sector Register
1	1	Data Register	Data Register

During direct memory access (DMA) types of data are transferred between the Data Register of the SAB 279XA and the processor, the Data Request (DRQ) output is used in data transfer control This signal also appears as status bit 1 during read and write operations.
In disk read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters have been lost by having transferred new data into the register prior to processor readout, the Lost Data bit is set in the Status Register. The read operation continues until the end of sector is reached.

In disk write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.
Upon completion of every command an INTRQ is generated. INTRQ is reset either by reading the Status Register or by loading the Command Register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.
The SAB 279XA has two modes of operating depending on the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, Single Density (FM) is selected. When $\overline{DDEN}$ = 0, Double Density (MFM) is selected. In either case, the CLK input (Pin 24) is set at 2 MHz for 8" drives or 1 MHz for $5^1/_4$" drives.
On the SAB 2791A/2793A, the $\overline{ENMF}$ input (Pin 25) can be used for controlling both, 5¼" and 8" drives with a single 2 MHz clock. When $\overline{ENMF}$ = 0, an internal divide by 2 of the CLK is performed. When $\overline{ENMF}$ = 1, no divide takes place. This allows the use of a 2 MHz clock for both, $5^1/_4$" and 8" configurations.
The internal VCO frequency must also be set to the proper value. The $\overline{5}/8$ input (Pin 17) is used to select data separator operation by internally dividing the read clock. When $\overline{5}/8$ = 0, $5^1/_4$" data separation is selected; when $\overline{5}/8$ = 1, 8" drive data separation is selected.

CLOCK (24)	$\overline{ENMF}$ (25)	$\overline{5}/8$ (17)	DRIVE
2 MHz	1	1	8"
2 MHz	0	0	$5^1/_4$"
1 MHz	1	0	$5^1/_4$"

All other conditions are invalid.

Functional Description

The SAB 279XA is software compatible with the SAB 179X series of Floppy Disk Controllers. Commands, status, and data transfers are performed in the same way. Software generated for the SAB 179X can be transferred to a SAB 279XA system without modification.
In addition to the SAB 179X, the SAB 279XA contains an internal data separator and write precompensation circuit. The $\overline{TEST}$ (Pin 22) line is used to adjust both, data separator and precompensation. When $\overline{TEST}$ = 0, the WD (Pin 31) line is internally connected to the output of the write precomp single shot. Adjustment of the WPW (Pin 33) line can then be accomplished. A second single shot tracks the precomp setting at approximately 3:1 to ensure adequate Write Data pulse widths to meet drive specifications.
Similarly, data separation is also adjusted with $\overline{TEST}$ = 0. The TG43 (Pin 29) line is internally connected to the output of the read data single shot, which is adjusted via the RPW (Pin 18) line. The DIRC (Pin 16) line contains the read clock output (500 kHz for 8" drives). The VCO trimming capacitor (Pin 26) is adjusted to center frequency.
Internal timing signals are used to generate pulses during the adjustment mode so that these adjustments can be made while the device is in operation. The $\overline{TEST}$ line also contains a pull-up resistor, so adjustments can be performed simply by grounding the $\overline{TEST}$ pin, overriding the pull-up. The $\overline{TEST}$ pin cannot be used to disable stepping rates during operation as its function is quite different from the SAB 179X.
Other pins on the device also include pull-up resistors and may be left open to satisfy a logic 1 condition. These are: ENP, $\overline{5/8}$, $\overline{ENMF}$, $\overline{WPRT}$, $\overline{DDEN}$, HLT, $\overline{TEST}$, and $\overline{MR}$.

General Disk Read Operation

Sector lengths of 128, 256, 512 or 1024 are obtainable either in FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logic 1. For MFM formats, $\overline{DDEN}$ should be placed to a logic 0. Sector lengths are determined at format time by the fourth byte in the ID field.

Sector Length Table*

Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

* SAB 2795A/97A may vary - see command summary.

The number of sectors per track as far as the SAB 279XA is concerned can be from 1 to 255 sectors. The number of tracks as far as the SAB 279XA is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track.

General Disk Write Operation

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the SAB 279XA before the Write Gate Signal can be activated.
Writing is inhibited when the Write Protect input is logic low, in which case any write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.
For write operations, the SAB 279XA provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write Data consists of a series of pulses set to a width approximately three times greater than the precomp adjustment. Write Data provides the unique address marks in both formats.

Ready

Whenever a read or write command (Type II or III) is received the SAB 279XA samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.
TG 43 may be tied to ENP to enable write precompensation on tracks 44–76.

Write Precompensation

When operating in double density mode ($\overline{DDEN}$ = 0), the SAB 279XA has the capability of providing a user-defined precompensation value for Write Data. An external potentiometer (10K) tied to the WPW signal (Pin 33) allows a setting of 100 to 300 ns from nominal.
Setting the write precomp value is accomplished by forcing the $\overline{TEST}$ line (Pin 22) to a logic 0. A stream of pulses can then be seen on the Write Data (Pin 31) line. Adjust the WPW Potentiometer for the desired pulse width. This adjustment may be performed in-circuit since Write Gate (Pin 30) is inactive while $\overline{TEST}$ = 0.

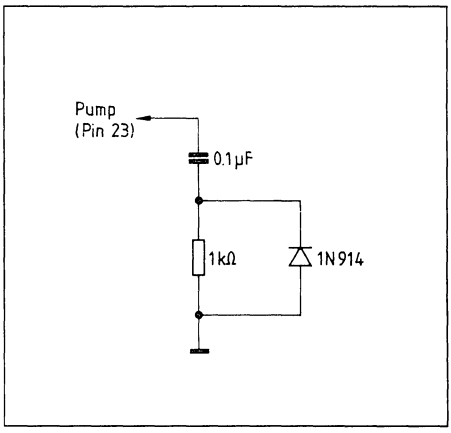
Data Separation

The SAB 279XA can operate with either an external data separator or its own internal recovery circuit. The condition of the $\overline{TEST}$ line (Pin 22) in conjunction with $\overline{MR}$ (Pin 19) will select internal or external mode.
To program the SAB 279XA for external VCO, a $\overline{MR}$ pulse must be applied while $\overline{TEST}$ = 0. A clock equivalent to eight times the data rate (e. g., 4.0 MHz for 8" double density) is applied to the VCO input (Pin 26). The feedback reference voltage is available on the Pump output (Pin 23) for external integration to control the VCO. $\overline{TEST}$ is returned to a logic 1 for normal operation. Note: To maintain this mode, $\overline{TEST}$ must be held low whenever $\overline{MR}$ is applied. For internal VCO operation, the $\overline{TEST}$ line must be high during the $\overline{MR}$ pulse, then set to a logic 0 for the adjustment procedure.
A 50 k Potentiometer tied to the RPW input (Pin 18) is used to set the internal Read Data pulse for proper phasing. With a scope on Pin 29 (TG43), adjust the RPW pulse for 1/8 of the data rate (250 ns for 8" Double Density). An external variable capacitor of typically 5–60 pF is tied to the VCO input (Pin 26) for adjusting center frequency. With a frequency counter on Pin 16 (DIRC) adjust the trimmer cap to yield the appropriate data rate (500 kHz for 8" Double Density). The $\overline{DDEN}$ line must be low while the $\overline{5/8}$ line is held high or the adjustment times above will be doubled.

VCO Operation

After adjustments have been made, the $\overline{TEST}$ pin is returned to a logic 1 and the device is ready for operation. Adjustments may be made in-circuit since the DIRC and TG43 lines may toggle without affecting the drive.
The PUMP output (Pin 23) consists of positive and negative pulses. Their duration is equivalent to the pnase difference of incoming Data vs. VCO frequency. This signal is internally connected to the VCO input, but a filter is needed to connect these pulses to a slow moving DC voltage.
The internal phase-detector is unsymmetrical for a random distribution of data pulses by a factor of two, in favor of a PUMP UP condition. Therefore it is desirable to have a PUMP DOWN twice as responsive to prevent run-away during a lock attempt.
A first order lag-lead filter can be used at the PUMP output (PIN 23). This filter controls the instantaneous response of the VCO to bit-shifted data (jitter) as well as the response to normal frequency shift i.e. the lock-up time. A balance must be accomplished between the two conditions to inhibit overresponsiveness to jitter and to prevent an extremely wide lock-up response leading to PUMP run-away. The filter affects these two reactions in mutually opposite directions.

The following Filter Circuit is recommended for 8" FM/MFM:



Since $5^1/_4$" Drives operate at exactly one-half the data rate (250 Kbytes/sec) the above capacitor should be doubled to 0.2 or 0.22 µF.

Command Summary

Commands for SAB 2791A, SAB 2793A										Commands for SAB 2795A, SAB 2797A								
		Bits								Bits								
Type	Command	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	T	h	V	r_1	r_0	0	0	1	T	h	V	r_1	r_0
I	Step-in	0	1	0	T	h	V	r_1	r_0	0	1	0	T	h	V	r_1	r_0
I	Step-out	0	1	1	T	h	V	r_1	r_0	0	1	1	T	h	V	r_1	r_0
II	Read-Sector	1	0	0	m	S	E	C	0	1	0	0	m	L	E	U	0
II	Write Sector	1	0	1	m	S	E	C	a_0	1	0	1	m	L	E	U	a_0
III	Read Address	1	1	0	0	0	E	0	0	1	1	0	0	0	E	U	0
III	Read Track	1	1	1	0	0	E	0	0	1	1	1	0	0	E	U	0
III	Write Track	1	1	1	1	0	E	0	0	1	1	1	1	0	E	U	0
IV	Force Interrupt	1	1	0	1	I_3	I_2	I_1	I_0	1	1	0	1	I_3	I_2	I_1	I_0

Flag Summary

Command Type	Bit	Description
I	r_1, r_0 = Stepping Motor Rate	see page 13 for details
I	V = Track Number Verify Flag	V = 0, No verify V = 1, Verify on destination track
I	h = Head Load Flag	h = 0, Unload head at beginning h = 1, Load head at beginning
I	T = Track Update Flag	T = 0, No update T = 1, Update track register
II & III	a_0 = Data Address Mark	a_0 = 0, FB (DAM) a_0 = 1, F8 (deleted DAM)
II	C = Side Compare Flag	C = 0, Disable side compare C = 1, Enable side compare
II & III	U = Update SSO	U = 0, Update SSO to 0 U = 1, Update SSO to 1
II & III	E = 15 ms Delay	E = 0, No 15 ms delay E = 1, 15 ms delay (30 ms for 1 MHz clock)
II	S = Side Compare Flag	S = 0, Compare for side 0 S = 1, Compare for side 1
II	L = Sector Length Flag L = 1 (implicit) for SAB 2791A/93A	
II	m = Multiple Record Flag	m = 0, Single record m = 1, Multiple records
IV	Ix = Interrupt Condition Flags I0 = 1: Interrupt on Not Ready to Ready Transition I1 = 1: Interrupt on Ready to Not Ready Transition I2 = 1: Interrupt on next Index Pulse I3 = 1: Immediate Interrupt, requires a Reset* I3–I0 = 0: Terminate with no interrupt (INTRQ)	

	LSB's Sector Length in ID Field			
	00	01	10	11
L = 0	256	512	1024	128
L = 1	128	256	512	1024

* See Type IV command description for further information.

Status Register Summary

Bit	All Type I Commands	Read Address	Read Sector	Read Track	Write Sector	Write Track
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	0	0
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 00	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

Status for Type I Commands

Bit	Name	Meaning
S7	NOT READY	This bit, when set, indicates that the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically "ored" with MR.
S6	WRITE PROTECT	When set, indicates that Write Protect is activated. This bit is an inverted copy of $\overline{\text{WPRT}}$ input.
S5	HEAD LOADED	When set, it indicates that the head is loaded and engaged. This bit is a logical "And" of HLD and HLT signals.
S4	SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3	CRC ERROR	CRC encountered in ID field.
S2	TRACK 00	When set, indicates that Read/Write head is positioned to Track 00. This bit is an inverted copy of the $\overline{\text{TR00}}$ input.
S1	INDEX	When set, indicates that index mark is detected from drive. This bit is an inverted copy of the $\overline{\text{IP}}$ input.
S0	BUSY	When set, command is in progress. When reset, no command is in progress.

Status for Type II and III Commands

Bit	Name	Meaning
S7	NOT READY	This bit, when set, indicates that the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and "ored" with MR. The Type II and III Commands will not execute unless the drive is ready.
S6	WRITE PROTECT	For Read Record: not used. For Read Track: not used. On any Write: It indicates a Write Protect. This bit is reset, when updated.
S5	RECORD TYPE	For Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. For any Write: forced to a zero.
S4	RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3	CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2	LOST DATA	When set, it indicates that the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1	DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates that the DR is full on a read Operation or the DR is empty on a write operation. This bit is reset to zero when updated.
S0	BUSY	When set, command is under execution. When reset, no command is under execution.

Summary of Adjustment Procedures

Write Precompensation

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19).
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe pulse width on WD (Pin 31).
5) Adjust WPW (Pin 33) for desired pulse width (Precomp Value).
6) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

Data Separator

1) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.
2) Strobe $\overline{\text{MR}}$ (Pin 19). Ensure that 5/8, and $\overline{\text{DDEN}}$ are set properly.
3) Set $\overline{\text{TEST}}$ (Pin 22) to a logic low.
4) Observe pulse width on TG43 (Pin 29).
5) Adjust RPW (Pin 18) for 1/8 of the read clock (250ns for 8" DD, 500ns for $5^1/_4$" DD, etc.).
6) Observe frequency on DIRC (Pin 16).
7) Adjust variable capacitor on VCO pin for data rate (500 kHz for 8" DD, 250 kHz for $5^1/_4$" DD, etc.).
8) Set $\overline{\text{TEST}}$ (Pin 22) to a logic high.

NOTE: To maintain internal VCO operation, insure that $\overline{\text{TEST}}$ = 1 whenever a master reset pulse is applied.

Status Register

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared as after a Type I command.

The user has the option of reading the Status Register through program control or using the DRQ line with DMA or interrupt methods. When the Data Register is read the DRQ bit in the Status Register and the DRQ line are automatically reset. A write to the Data Register also causes both DRQs to reset.

The Busy bit in the status may be monitored with a user program to determine when a command is complete, in lieu of using the INTRQ line. When using the INTRQ, a busy status check is not recommended because a read of the Status Register to determine the condition of Busy will reset the INTRQ line.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown on page 11.

Because of internal sync cycles, certain time delays must be observed when operating under programmed I/O. They are:

Operation	Next Operation	Delay Req'd.	
		FM	MFM
Write to Command Reg.	Read Busy Bit (Status Bit 0)	12 μs	6 μs
Write to Command Reg.	Read Status Bits 1--7	28 μs	14 μs
Write to Any Register	Read From Diff. Register	0	0

Times double when clock =1 MHz

Command Description

The SAB 279XA will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The only exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault-free. For ease of discussion, commands are divided into four types. Commands and types are summarized on page 10.

Type I Commands

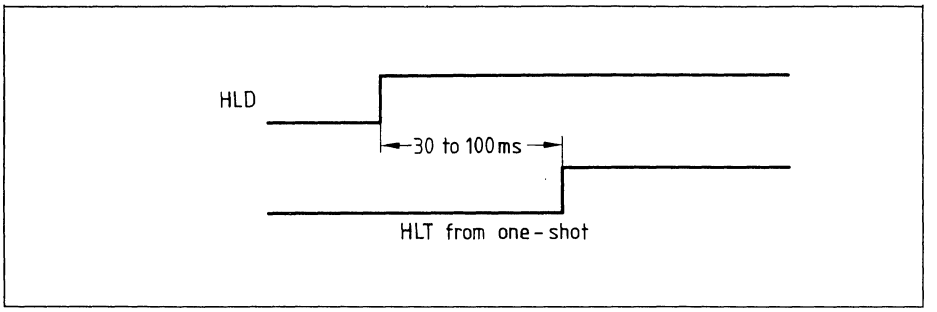
The Type I commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I commands contains a rate field (r_0, r_1) which determines the stepping motor rate.
A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the Direction output. The chip steps the drive in the same direction it has been stepped previously, unless the command changes the direction. The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated. The rates can be applied to a Step-Direction motor through the device interface.

Stepping Rates

CLK		2 MHz	1 MHz
r1	r0	$\overline{TEST}$ = 1	$\overline{TEST}$ - 1
0	0	3 ms	6 ms
0	1	6 ms	12 ms
1	0	10 ms	20 ms
1	1	15 ms	30 ms

After the last directional step, additional 15 milliseconds of head settling time are generated if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.
When a Seek, Step or Restore command is executed an optional verification of Read/Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID field is compared against the contents of the Track Register. If the track numbers compare and the ID field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. If there is a match but not a valid CRC, the CRC Error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. The SAB 279XA must find an ID field with correct track number and correct CRC within 5 revoltuions of the media; otherwise the Seek Error is set and an INTRQ is generated. If V = 0, no verification is performed.
The Head Load (HLD) output controls the movement of the Read/Write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the Verify flag is set (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with h = 0 and V = 0; or if the SAB 279XA is in an idel state (non-busy) and 15 index pulses have occured.
Head Load Timing (HLT) is an input to the SAB 279XA which is used for the head engage time.
When HLT = 1, the SAB 279XA assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a single shot. The output of the single shot is then used for HLT and supplied as an input to the SAB 279XA.

Head Load Timing



When both HLD and HLT are true, the SAB 279XA will then read from or write to the media. The "And" of HLD and HLT appears as status bit 5 in Type I status.

Summary of the Type I commands:
If h = 0 and V = 0, HLD is reset.
If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay.
If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the SAB 279X waits for HLT to be true.
If h = 1 and V = 1, HLD is set at the beginning of the command.
Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the SAB 279X then waits for HLT to occur.
For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

Restore (Seek Track 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read/Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses at a rate specified by the r_1 r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the SAB 279XA terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is always executed when $\overline{MR}$ goes from an active to an inactive state.

Seek

This command assumes that the Track Register contains the track number of the current position of the Read/Write head and the Data Register contains the desired track number. The SAB 279XA will update the Track Register and issue stepping pulses in the appropriate direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command. Note: When using multiple drives, the Track Register must be updated for the drive selected before seek commands are issued.

Step

Upon receipt of this command, the SAB 279XA issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous Step command. After a delay determined by the r_1 r_0 field, a verification takes place if the V flag is on. If the T flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

Step-In

Upon receipt of this command,t he SAB 279XA issues one stepping pulse in the direction towards track 76. If the T flag is on, the Track Register is incremented by one. After a delay determined by the r_1 r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

Step-Out

Upon receipt of this command, the SAB 279XA issues one stepping pulse in the direction twoards track 0. If the T flag is on, the Track Register is decremented by one. After a delay determined by the r_1 r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the termination of the command.

Exceptions

On the SAB 2795A/97A devices, the SSO output is not affected during Type I commands, and an internal side compare does not take place when the (V) Verify flag V is on.

Type II Commands

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading a Type II command into the Command Register the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the Busy status bit is set. If the E flag is 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 ms delay. If the E flag is 0, the head is loaded and HLT is sampled without a 15 ms delay.

When an ID field is located on the disk, the SAB 279XA compares the track number on the ID field with the Track Register. If they do not match, the next encountered ID field is read and a comparison is again made. If there has been a match, the Sector Number of the ID field is compared with the Sector Register. If there is no sector match, the next encountered ID field is read off the disk and again compared. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The SAB 279XA must find an ID field with a track number, sector number, side number, and CRC within 5 revolutions of the disk; otherwise, the Record-Not-Found status bit is set (Status bit 4) and the command is terminated with an interrupt.

Each of the Type II commands contains an m flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the termination of the command. If m = 1, multiple records are read or written with the Sector Register internally updated so that an address verification can occur on the next record. The SAB 279XA will continue to read or write multiple records and update the Sector Register in numerical ascending sequence until the Sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

For example: If the SAB 279XA is instructed to read sector 27 and there are only 26 on the track, the Sector Register exceeds the number available. The SAB 279XA will search for 5 disk revolutions, interrupt out, reset Busy, and set the Record-Not-Found status bit.

The Type II commands for SAB 2795A/97A also contain Side Select Compare flags. When C = 0 (bit 1) no side comparison is made. When C = 1, the LSB of the side number is read off the ID field of the disk and compared with the contents of the (S) flag (bit 3). If the S flag corresponds to the side number recorded in the ID field, the SAB 279XA continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The Type II and III commands for the SAB 2795A/97A contain a Side Select flag (bit 1). When U = 0, SSO is updated to 0. Similarly, U = 1 updates SSO to 1. The chip compares the SSO to the ID field. If they do not correspond within 5 revolutions the interrupt line is made active and the RNF status bit is set.

The SAB 2795A/97A Read Sector and Write Sector commands include an L flag. The L flag, in conjunction with the sector length byte of the ID Field, allows different byte lenghts to be implemented in each sector. For IBM compatibility, the L flag should be set to a one.

Read Sector

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the ID field search is repeated. When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the computer has not read the previous contents of the DR before a new character is transferred that character is lost and the Lost Data status bit is set. This sequence continues until the complete data field has been input to the computer. If there is a CRC error at the end of the data field, the CRC Error status bit is set, and the command is terminated (even if it is a multiple sector command).

At the end of the read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (bit 5) as shown:

Status Bit 5	
1	Deleted Data Mark
0	Data Mark

Write Sector

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The SAB 279XA counts off 11 bytes in single density and 22 bytes in double density from the CRC field, and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeroes in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The SAB 279XA then writes the data field and generates DRQs to the computer. If the DRQ is not serviced in time for continous writing, the Lost Data status bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of hex FE in FM or in MFM. The WG output is then deactivated. For a 2 MHz clock the INTRQ is set between 8 and 12 μsec after the last CRC byte has been written. For partial sector writing, the proper method is to write the data and fill the balance with zeroes. By letting the chip fill the zeroes, errors may be masked by the Lost Data status and improper CRC bytes.

Types III Commands

Read Address

Upon receipt of the Read Address command, the head is loaded and the Busy status bit is set. The next encountered ID field is then read from the disk, and the six data bytes of the ID field are assembled and transferred to the DR. And DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the SAB 279XA checks for validity and the CRC Error status bit is set if there is a CRC error. The track address of the ID field is written into the Sector Register so that a comparison can be made by the host. At the end of the operation an interrupt is generated and the Busy status bit is reset.

Read Track

Upon receipt of the Read Track command, the head is loaded, and the Busy status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. All gap, header, and data bytes are assembled and transferred to the Data Register. DRQs are generated for each byte. The accumulation of bytes is synchronized to each address mark encountered. An interrupt is generated at the termination of the command.
This command has several characteristics which make it suitable for diagnostic purposes. They are: no CRC checking is performed; gap information is included in the data stream; the internal side compare is not performed; and the address mark detector is on for the duration of the command. Because the A.M. detector is always on, write splices or noise may cause the chip to look for an A.M. If an address mark does not appear on schedule with the Lost Data status flag being set.
The ID A.M., ID field, ID CRC bytes, DAM, data and data CRC bytes for each sector will be correct. The gap bytes may be read incorrectly during write-splice time because of synchronization.

Write Track Formatting the Disk

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA with a large amount of memory. Data and gap information must be provided at the computer interface. Formatting the disk is accomplished

by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the head is loaded and the Busy status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The data request is activated immediately upon receiving the command, but writing will not start before the first byte is loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated by making the device not busy. The Lost Data status bit is set, and the interrupt is activated. If a byte is not present in the DR when needed, a byte of zeroes is substituted.

This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the Data Register, it is written on the disk with a normal clock pattern. However, if the SAB 279XA detects a data pattern of F5 thru FE in the Data Register. This is interpreted as Data Address Marks with missing clocks or CRC generation. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR or by receipt of F5 in MFM. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRCs must be generated by an F7 pattern. Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

Control Bytes for Initialization

Data Pattern in DR (HEX)	SAB 279XA Interpretation in FM ($\overline{DDEN}$ = 1)	SAB 279XA Interpretation in MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1[1] in MFM, Preset CRC
F6	Not Allowed	Write C2[2] in MFM
F7	Generate 2 CRC Bytes	Generate 2 CRC Bytes
F8 thru FB	Write F8 thru FB, CLK = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with CLK = D7	Write FC in MFM
FD	Write FD with CLK = FF	Write FD in MFM
FE	Write FE, CLk = C7, Preset CRC	Write FE in MFM
FF	Write FF with CLK = FF	Write FF in MFM

[1] Missing clock transition between bits 4 and 5
[2] Missing clock transition between bits 3 and 4

Type IV Commands

The Force Interrupt command is generally used to terminate a multiple sector Read or Write command or to ensure Type I status in the Status Register. This command can be loaded into the Command Register at any time. If there is a current command under execution (Busy status bit set) the command will be terminated and the Busy status bit reset. The lower four bits of the command determine the conditional interrupt as follows:
I0: Not-Ready to Ready Transition
I1: Ready to Not-Ready Transition
I2: Every Index Pulse
I3: Immediate Interrupt
The conditional interrupt is enabled when the corresponding bit positions of the command (I3-I0) are set to a1. Then, when the condition for interrupt is met, the INTRQ line will go high signifying that the condition specified has occurred. If I3-I0 are all set to zero (hex D0), no interrupt will occur but any command presently under execution will be immediately terminated. When using the immediate interrupt condition (I3 = 1), an interrupt will be immediately generated and the current command terminated. Reading the status or writing to the Command Register will not automatically clear the interrupt. The hex D0 is the only command that will enable the immediate interrupt (hex D8) to clear on a subsequent load Command Register or read Status Register operation. Follow a hex D8 with D0 command. Wait 8 μs (double density) or 16 μs (single density) before issuing a new command after issuing a Force Interrupt command (times double when clock = 1 MHz). Loading a new command sooner than this will nullify the forced interrupt. Forced interrupt stops any command at the end of an internal micro-instruction and generates INTRQ when the specified condition is met. Forced interrupt will wait until ALU operations in progress are completed (CRC calculations, comparisons, etc.). More than one condition may be set at a time. If for example, the Ready to Not-Ready condition (I1 = 1) and the Every Index Pulse (I2 = 1) are both set, the resultant command would be hex DA. The OR function is performed so that either a Ready to Not-Ready or the next Index Pulse will cause an interrupt condition.

Formats

IBM 3740 Format – 128 Bytes/Sector (8")

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the Data Register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	FF (or 00)[3]
6	00
1	FC (Index Mark)
26	FF (or 00)
[1] 6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRCs written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (E5)
1	F7 (2 CRCs written)
27	FF (or 00)
247[2]	FF (or 00)

IBM System 34 Format – 256 Bytes/Sector (8")

Shown in the following table is the IBM double-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
80	4E
12	00
3	F6 (writes C2)
1	FC (Index Mark)
50	4E
[1] 12	00
3	F5 (writes A1)
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	Side Number (0 or 1)
1	Sector Number (1 through 1A)
1	01 (Sector length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (writes A1)
1	FB (Data Address Mark)
256	Data (E5)
1	F7 (2 CRCs written)
54	4E
598[2]	4E

[1]) Write bracketed field 26 times.
[2]) Continue writing until SAB 279XA interrupts out. Approx. 247 (598) bytes.
[3]) Optional '00' on SAB 2795A/97A only is allowed.

Recommended – 128 Bytes/Sector (Mini-Diskette)

Shown below is the recommended single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the Data Register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
40	FF (or 00)
[1] 6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 through 10)
1	00 (Sector length)
1	F7 (2 CRCs written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (E5)
1	F7 (2 CRCs written)
10	FF (or 00)
349[2]	FF (or 00)

Recommended – 256 Bytes/Sector (Mini-Diskette)

Shown below is the recommended double-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the Data Register with the following values. For every byte to be written, there is one data request.

Number of Bytes	Hex Value of Byte Written
60	4E
[1] 12	00
3	F5 (Writes A1)
1	FE (ID Address Mark)
1	Track Number (0 through 4C)
1	Side Number (0 or 1)
1	Sector Number (1 through 10)
1	01 (Sector Length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (Write A1)
1	FB (Data Address Mark)
256	Data (E5)
1	F7 (2 CRCs written)
24	4E
718[2]	4E

Non-Standard Formats

Variations in the IBM formats are possible to a limited extent if the following requirements are met:

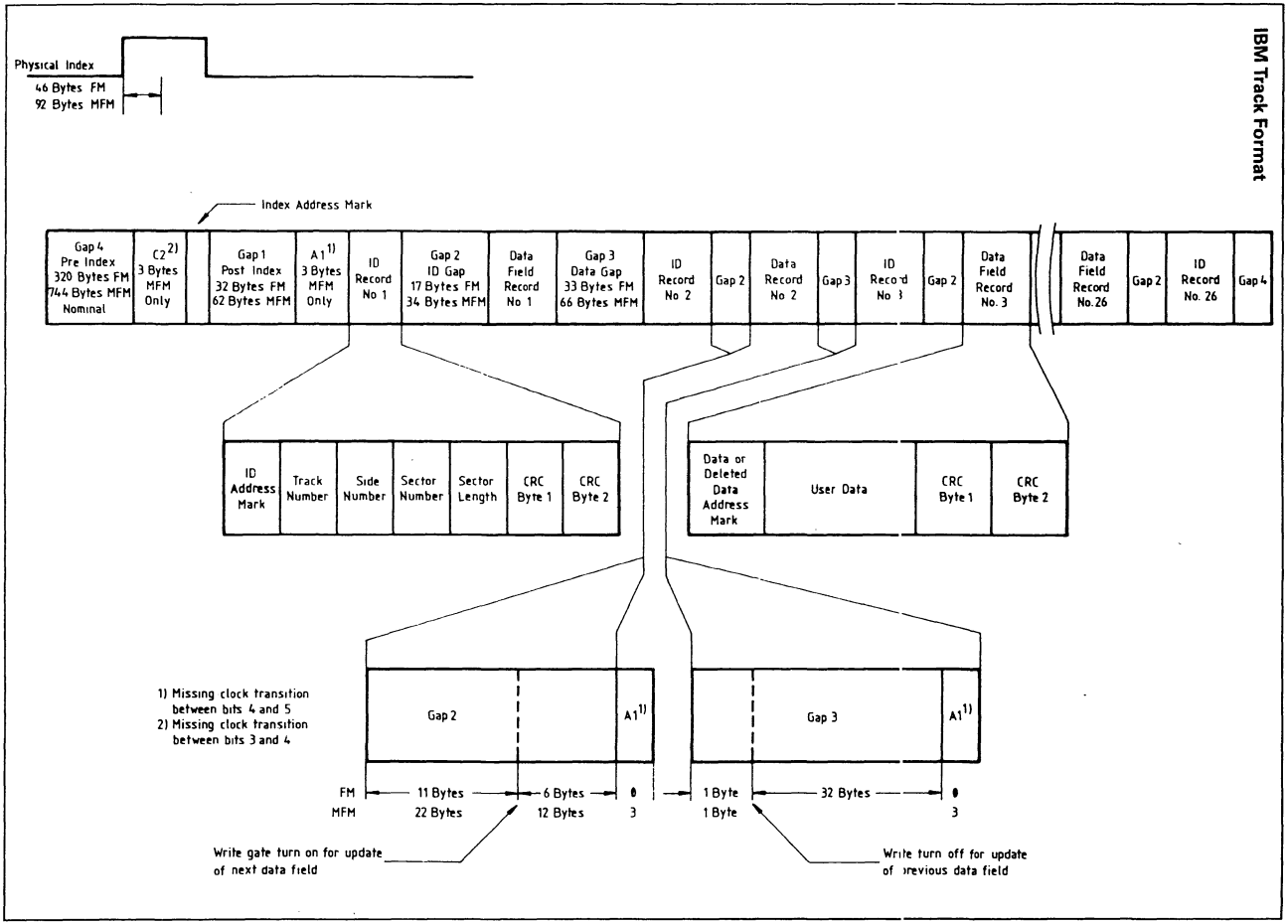
1. Sector size must be 128, 256, 512 or 1024 bytes.
2. Gap 2 cannot be varied from the recommended format.
3. 3 bytes of A1 must be used in MFM.

In addition, the Index Address Mark is not required for operation by the SAB 279XA. Gap 1, 3, and 4 lengths can be as short as 2 bytes for SAB 279XA operation, however, PLL lock up time, motor speed variation, write-splice area, etc., will add more bytes to each gap to achieve proper operation. It is recommended that the IBM format should be used for highest system reliability.

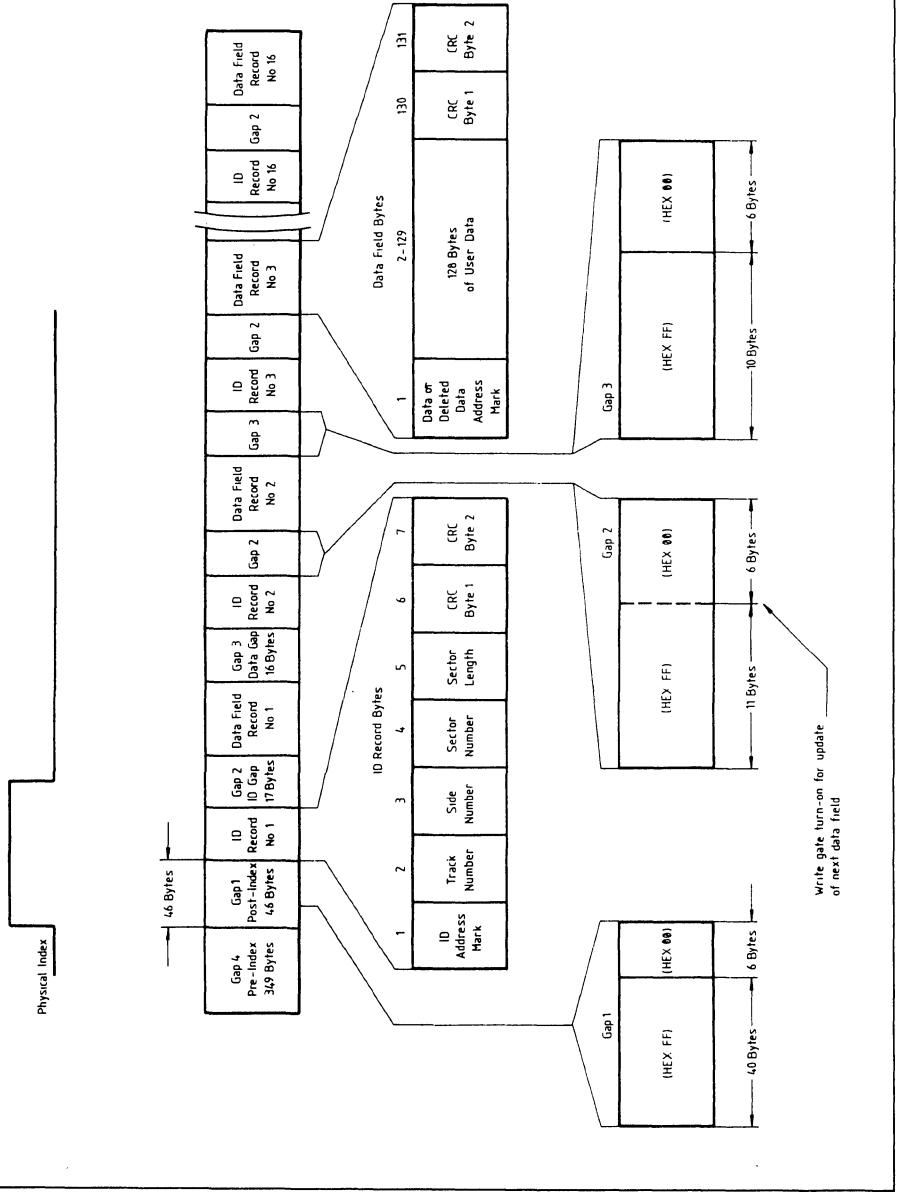
	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
[3]	6 bytes 00	12 bytes 00
A1		
Gap III	10 bytes FF	24 bytes 4E
[4]	4 bytes 00	8 bytes 00
		3 bytes A1
Gap IV	16 bytes FF	16 bytes 4E

[1] Write bracketed field 16 times.
[2] Continue writing until SAB 279XA interrupts out. Approx. 349 (718) bytes.
[3] Byte counts must be exact.
[4] Byte counts are minimum, except exactly 3 bytes of A1 must be written in MFM.

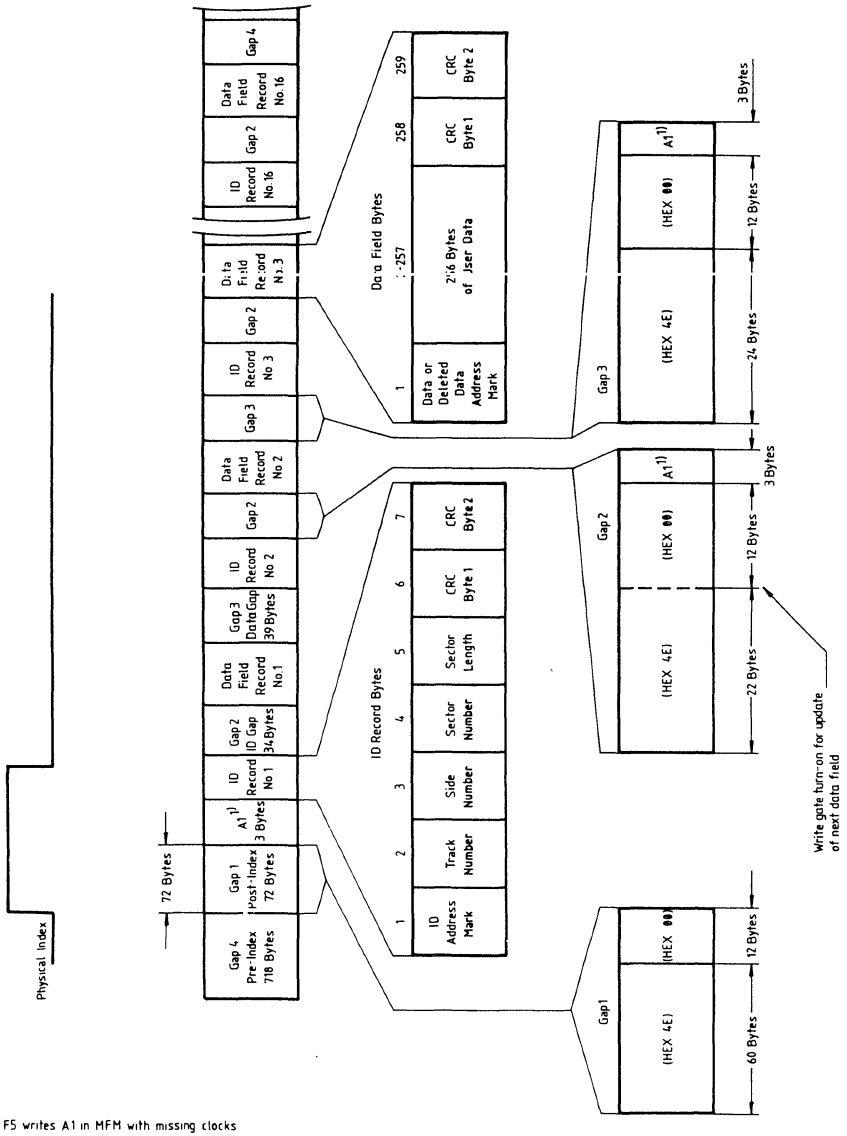
IBM Track Format



Recommended Single Density Format (Mini-Diskette)



Recommended Double Density Format (Mini-Diskette)



[1] FD writes A1 in MFM with missing clocks between bits 4 and 5

Absolut Maximum Ratings[1)]

Ambient Temperature Under Bias	0 to + 70 °C
Storage Temperature	−65 to + 150 °C
Voltage on Any Pin with Respect to Ground (VSS)	−0.5 to + 7 V
Power Dissipation	2 W

D.C. Characteristics

TA = 0 to 70°C; VCC = +5V ±5%, VSS = 0V

Symbol	Parameter	Limit Values			Unit	Test Conditions
		Min.	Typ.	Max.		
IIL 1	Input Leakage Current[2)]	–		10	µA	VIN = VCC
IIL 2	Internal Leakage Current[2)]	100		1700		VIN = OV
IOL	Output Leakage Current	–		10		VOUT = VCC
VIH	Input High Voltage	2.0		–	V	–
VIL	Input Low Voltage	–		0.8		
VOH	Output High Voltage	2.4	–	–		IOH = −100 µA
VOL	Output Low Voltage	–		0.45		IOL = 1.6 mA
VOHP	Output High PUMP	2.2		–		IOHP = −1.0 mA
VOLP	Output Low PUMP	–		0.2		IOLP = +1.0 mA
ICC	Supply Current	–	70	150	mA	All outputs open

Capacitance[3)]

Symbol	Parameter	Limit Value (max.)	Unit	Test Condition
CIN	Input Capacitance	15	pF	Unmeasured pins returned to GND
COUT	Output Capacitance			

[1)] Stresses above those listed under „Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2)] ILL 1 applies to normal inputs, IIL 2 to inputs with internal pull-up resistors on pins 1, 17, 19, 22, 36, 37, and 40. Also pin 25 on SAB 2791A/93A.

[3)] This parameter is periodically sampled and not 100% tested.

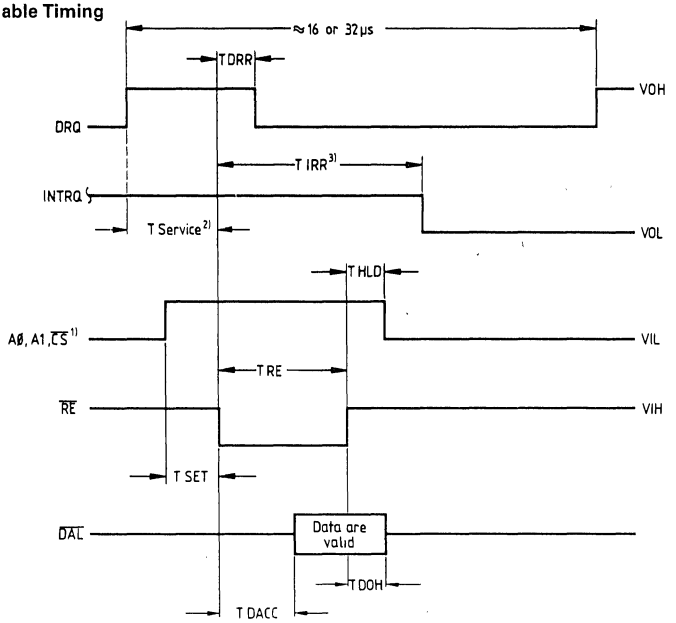
A.C. Characteristics

TA = 0 to 70°C; VCC = +5V ± 5%; VSS = 0V.
All timing readings at VOL = 0.8 V and VOH = 2.0 V.

Read Enable Timing

Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
TSET	Setup ADDR & CS to $\overline{RE}$	50	–	–	ns	–
THLD	Hold ADDR & CS from $\overline{RE}$	10				
TRE	$\overline{RE}$ Pulse Width	200				CL = 50 pF
TDRR	DRQ Reset from $\overline{RE}$	–	100	200		–
TIRR	INTRQ Reset from $\overline{RE}$		500	3000		
TDACC	Data Valid from $\overline{RE}$		100	200		CL = 50 pF
TDOH	Data Hold from $\overline{RE}$	20	–	150		

Read Enable Timing



DRQ rising edge: Indicates that the data register has assembled data.
DRQ falling edge: Indicates that the data register was read.
INTRQ rising edge: Occurs at end of command.
INTRQ falling edge: Indicates that the status register was read.

1) $\overline{CS}$ may be permanently tied LOW if desired.

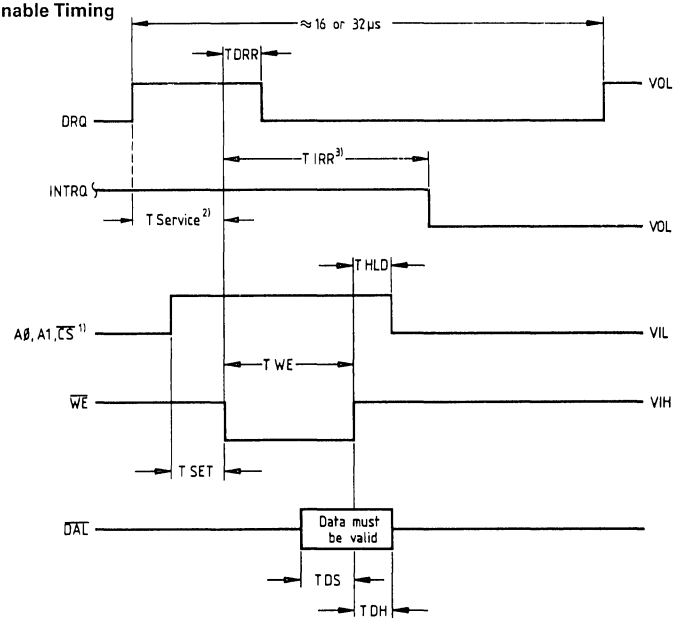
2) T Service (worst case)
– FM = 27.5 µs
– MFM = 13.5 µs

3) Time doubles when CLK = 1 MHz.

Write Enable Timing

Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
TSET	Setup ADDR & CS to $\overline{WE}$	50				
THLD	Hold ADDR & CS from $\overline{WE}$	10	–	–		
TWE	$\overline{WE}$ Pulse Width	200			ns	
TDRR	DRQ Reset from $\overline{WE}$	–	100	200		
TIRR	INTRQ Reset from $\overline{WE}$		500	3000		
TDS	Data Setup to $\overline{WE}$	150	–	–		
TDH	Data Hold from $\overline{WE}$	50				

Write Enable Timing



DRQ rising edge: Indicates that the data register is empty.
DRQ falling edge: Indicates that the data register is loaded.
INTRQ rising edge: Indicate the end of a command.
INTRQ falling edge: Indicates that the command register is written to.

1) CS may permanently tied LOW if desired. When writing Data into Sector, Track or Data Register, the User cannot read this register until at least 4µs in MFM after the rising edge of WE. When writing into the Command Register status is not valid until some 28µs in FM/14µs in MFM later. These times double when CLK = 1 MHz.

2) T Service (worst case); FM = 23.5µs; MFM = 11.5µs.

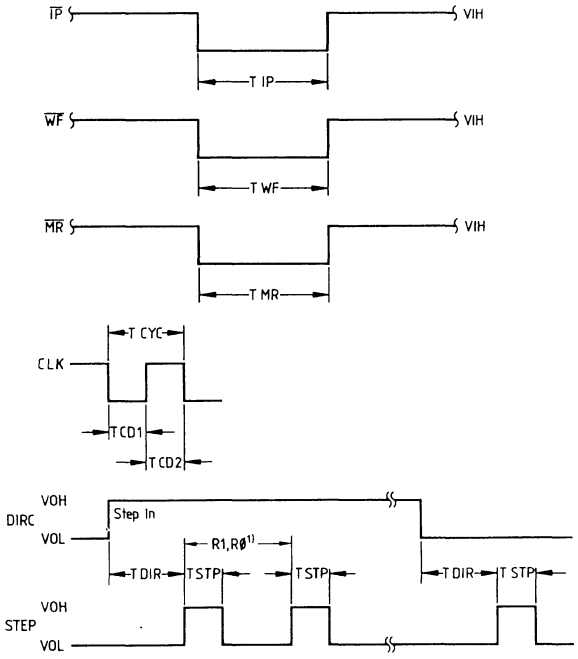
3) Time doubles when CLK = 1 MHz.

Miscellaneous Timing

Symbol	Parameter	Limit Values			Unit	Test Conditions	
		Min.	Typ.	Max.			
TCD 1	Clock Duty (low)	230	250	20000	ns	–	
TCD 2	Clock Duty (high)						
TSTP[1]	Step Pulse Output	2 or 4	–	--	µs		
TDIR	DIRC Setup to Step	–	12			± CLK Error	
TMR	Master Reset Pulse Width	50	–			–	
TIP	Index Pulse Width	10					
RPW	Read Window Pulse Width	120	–	700	ns	MFM	Input 0-5V
		240		1400		FM±15%	
	Precomp Adjust	100		300		MFM	
WPW	Write Data Pulse Width	200	300	400		Precomp = 100ns MFM	
		600	900	1200		Precomp = 300ns MFM	
VCO	Free Run Voltage Controlled Oscillator, Adjustable by Ext. Capacitor on Pin 26 Oscillator, Adjustable	6.0	–	–	MHz	Cext = Ø	
		–	4.0			Cext = 35pF	
	Pump Up +25%	5.0	–			PU = 2.2V, Cext = 35pF	
	Pump Down −25%	–		3.0		$\overline{PD}$ = 0.2V, Cext = 35pF	
	5% Change VCC	3.8		4.2		Cext = 35pF	
		3.5		–		TA = 75°C, Cext = 35pF	
	Adjustable External Capacitor	20	35	100	pF	VCO = 4.0 MHz nom.	
RCLK	Derived Read Clock = VCO: 8, 16, 32	–	500	–	kHz	$\overline{DDEN}$ = Ø 5/8 = 1	VCO = 4.0 MHz
			250			$\overline{DDEN}$ = Ø 5/8 = Ø	
			250			$\overline{DDEN}$ = 1 5/8 = 1	
			125			$\overline{DDEN}$ = 1 5/8 = Ø	
PU/ DON	PU/$\overline{PD}$ Time On (Pulse Width)		–	250	ns	MFM	
				500		FM	

[1] See stepping rates on page 13

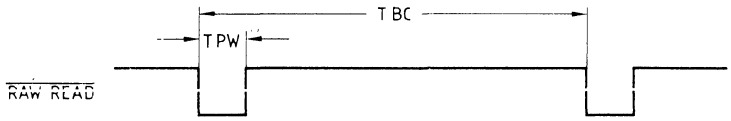
Miscellaneous Timing



Read Data Timing

Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
TPW	$\overline{\text{RAW READ}}$ Pulse Width	100	200	–	ns	–
TBC	$\overline{\text{RAW READ}}$ Cycle Time	1500	2000			

Read Data Timing

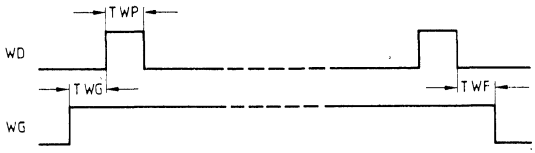


Write Data Timing

Symbol	Parameter	Limit Values			Units	Test Conditions
		Min.	Typ.	Max.		
TWP	Write Data Pulse Width	400	500	600	ns	FM
		200	250	300		MFM
TWG	Write Gate to Write Data		2		µs	FM
			1			MFM
TWF	Write Gate off from WD		2			FM
			1			MFM

All Times double when CLK = 1 MHz; no Write precompensation.

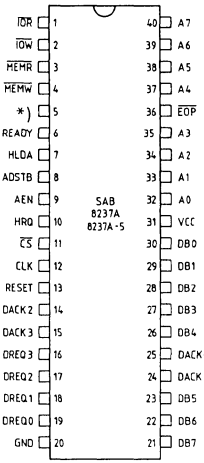
Write Data Timing



SAB 8237A, SAB 8237A-5 High Performance Programmable DMA Controller

- Four Independent DMA Channels
- Enable/Disable Control of Individual DMA Requests
- Memory-to-Memory Transfers
- Memory Block Initialization
- Address Increment or Decrement
- Independent Autoinitialization of all Channels
- High performance: Transfers up to 1.6 MBytes/Second with 5 MHz SAB 8237A-5
- Directly Expandable to any Number of Channels
- End of Process Input for Terminating Transfers
- Software DMA Requests
- Independent Polarity Control for DREQ and DACK Signals
- Single +5V Power Supply
- 40 Pin Dual-In-Line Package
- Fully compatible with the Industry Standard 9517A/8237A

Pin Configuration



*) Pin always tied high

Pin Names

DB7-DB0	Data Bus (bidirectional)
IOR, IOW	I/O Read and Write Input/Output
MEMR, MEMW	Memory Read and Write Output
A0-A3	Address Input/Output
A4-A7	Adress Output
CS	Chip Select Input
CLK	Clock Input
READY	Ready Input
HRQ	Hold Request Output
HLDA	Hold Acknowledge Input
RESET	Reset Input
DREQ0-DREQ3	DMA Request Input
DACK0-DACK3	DMA Acknowledge Output
AEN	Address Enable Output
ADSTB	Address Strobe Output
EOP	End of Process Input/Output

The SAB 8237A Multimode Direct Memory Access (DMA) Controller is designed to improve system performance by allowing external devices to directly transfer information to or from system memory. Memory-to-memory transfer capability is also provided.

The SAB 8237A contains four independent channels, each with a separate register set, and may be expanded to any number of channels by cascading additional controller chips. The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original state following an End of Process (EOP). Each channel has a full 64K address and word count capability.

The SAB 8237A is fabricated in +5V advanced N-channel, silicon gate Siemens MYMOS technology and packaged in a 40-pin DIP. The SAB 8237A-5 is the 5 MHz version of the standard 3 MHz SAB 8237A respectively.

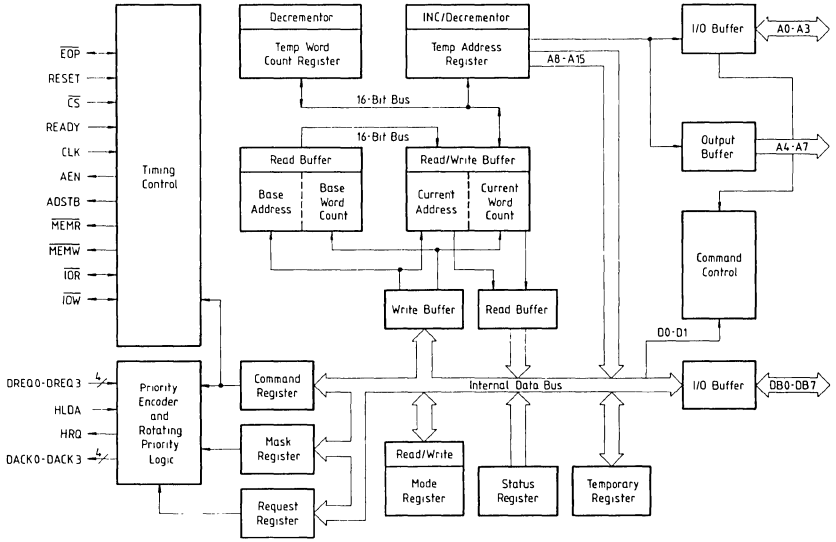
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
$\overline{IOR}$	1	I/O	I/O READ I/O Read is a bidirectional active low three-state line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the SAB 8237A to access data from a peripheral device during a DMA Write transfer.
$\overline{IOW}$	2	I/O	I/O WRITE I/O Write is a bidirectional active low three-state line. In the idle cycle it is an input control signal used by the CPU to load information into the SAB 8237A. In the Active cycle it is an output control signal used by the SAB 8237A to load data to a peripheral device during a DMA Read transfer. Write operations by the CPU to the SAB 8237A require a rising $\overline{IOW}$ edge following each data byte transfer. It is not sufficient to hold the $\overline{IOW}$ pin low and toggle $\overline{CS}$.
$\overline{MEMR}$	3	O	MEMORY READ The Memory Read signal is an active low three-state output used to access data from the selected memory location during a memory-to-peripheral or a memory-to-memory transfer.
$\overline{MEMW}$	4	O	MEMORY WRITE The Memory Write signal is an active low three-state output used to write data to the selected memory location during a peripheral-to-memory or a memory-to-memory transfer.
–	5	I	Pin 5 must be tied high.
READY	6	I	READY Ready is an input used to extend the memory read and write pulses from the SAB 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.
HLDA	7	I	HOLD ACKNOWLEDGE The active high Hold Acknowledge from the CPU indicates that control of the system busses has been relinquished.
ADSTB	8	O	ADDRESS STROBE The active high Address Strobe is used to strobe the upper address byte from DBØ-DB7 into an external latch.
AEN	9	O	ADDRESS ENABLE Address Enable is an active high signal used to disable the system bus during DMA cycles and to enable the output of the external latch which holds the upper byte of the address. Note that during DMA transfers HLDA and AEN should be used to deselect all other I/O peripherals which may erroneously be accessed as programmed I/O during the DMA operation. The SAB 8237A automatically deselects itself by disabling the $\overline{CS}$ input during DMA transfers.

Symbol	Number	Input (I) Output (O)	Function
HRQ	10	O	HOLD REQUEST The Hold Request to the CPU is used by the DMA to request control of the system bus. Software requests or unmasked DREQs cause the SAB 8237A to issue HRQ.
$\overline{CS}$	11	I	CHIP SELECT Chip Select is an active low input used to select the SAB 8237A as an I/O device during an I/O Read or I/O Write by the host CPU. This allows CPU communication on the data bus. During multiple transfers to or from the SAB 8237A by the host CPU $\overline{CS}$ may be held low providing $\overline{IOR}$ or $\overline{IOW}$ is toggled following each transfer.
CLK	12	I	CLOCK This input controls the internal operations of the SAB 8237A and its rate of data transfers. The input may be driven at up to 3 MHZ for the standard SAB8237A and up to 5 MHz for the SAB 8237A-5.
RESET	13	I	RESET Reset is an asynchronous active high input which clears the Command, Status, Request and Temporary register. It also clears the First/Last Flip/Flop and sets the Mask register. Following a Reset the device is in the idle cycle.
DACK0 DACK1 DACK2 DACK3	25 24 14 15	O O O O	DMA ACKNOWLEDGE The DMA Acknowledge lines indicate that a channel is active. In many systems they will be used to select a peripheral. Only one DACK will be active at a time and none will be active unless the DMA is in control of the bus. The polarity of these lines is programmable. Reset initializes them to active-low.
DREQ0 DREQ1 DREQ2 DREQ3	19 18 17 16	I I I I	DMA REQUEST The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service in Fixed Priority, DREQ0 has the highest priority and and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. The Polarity of DREQ is programmable. Reset initializes these lines to active high.
DB0-DB7	30-26, 23-21	I/O	DATA BUS The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled during the I/O Read by the host CPU, permitting the CPU to examine the contents of an Address register, the Status register, the Temporary register or a Word Count register. The Data Bus is enabled to input data during a host CPU I/O write, allowing the CPU to program the SAB 8237A control registers. During DMA cycles the most significant eight bits of the address are output onto the data bus to be strobed into an external latch by ADSTB. In memory-to-memory operations data from the source memory location comes into the SAB 8237A's Temporary register on the read-from-memory half of the operation. On the write-to-memory half of the operation, the data bus outputs the Temporary register data into the destination memory location.

Symbol	Number	Input (I) Output (O)	Function
A0–A3	32–35	I/O	ADDRESS 0–3 The four least significant address lines are bidirectional 3-state signals. During DMA idle cycles they are inputs and allow the host CPU to load or read control registers. When the DMA is active, they are outputs and provide the lower 4-bits of the output address.
A4–A7	37–40	O	ADDRESS 4–7 The four most significant address lines are three-state outputs and provide four bits of address. These lines are enabled only during DMA service.
$\overline{EOP}$	36	I/O	END OF PROCESS $\overline{EOP}$ is an active low bidirectional open-drain signal providing information concerning the completion of DMA service. When a channel's Word Count goes to zero, the SAB 8237A pulses $\overline{EOP}$ low to provide the peripheral with a completion signal. $\overline{EOP}$ may also be pulled low by the peripheral to cause premature completion. The reception of $\overline{EOP}$, either internal or external, causes the currently active channel to terminate the service, to set its TC bit in the Status register and to reset its request bit. If Autoinitialization is selected for the channel, the current registers will be updated from the base registers. Otherwise the channel's mask bit will be set and the register contents will remain unaltered. During memory-to-memory transfers, $\overline{EOP}$ will be output when the TC for channel 1 occurs. $\overline{EOP}$ always applies to the channel with an active DACK; external $\overline{EOP}$s are disregarded when DACK0-DACK3 are all inactive if the DMA is in state SI. In situations where two or more SAB 8237A DMAs are cascaded, the $\overline{EOP}$ pins should be logically OR'ed (not wire-OR'ed). Because $\overline{EOP}$ is an open-drain signal, an external pullup resistor is required. Values of 3.3 kΩ or 4.7 kΩ are recommanded; the $\overline{EOP}$ pin cannot sink the current passed by a 1 kΩ pullup.
VCC	31	–	POWER SUPPLY (+5 V)
GND	20	–	GROUND (0 V)

Block Diagram



Register Description

Current Address Register
Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address register during the transfer.

Current Word Count Register
Each channel has a 16-bit Current Word Count register. This register should be programmed with, and will return on a CPU read, a value one less than the number of words to be transferred. The word count is decremented after each transfer. The intermediate value of the word count is stored in the register during the transfer. When the value in the register goes to zero, a TC will be generated.

Base Address and Base Word Count Registers
Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original values of their associated current registers. During Autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with their corresponding current register in 8-bit bytes during DMA programming by the microprocessor.

Command Register
This 8-bit register controls the operation of the SAB 8237A. It is programmed by the microprocessor in the Program Condition and is cleared by Reset.

Mode Registers
Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits Ø and 1 determine which channel Mode register it to be written.

Request Register
The SAB 8237A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with it in the 4-bit Request register. These are nonmaskable and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control or is cleared upon generation of a TC or external EOP. The entire register is cleared by a Reset.

Mask Register
Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset.

Status Register
The Status registers may be read out of the SAB 8237A by the microprocessor. It indicates which channels have reached a terminal count and which channels have pending DMA requests.

Temporary Register
The Temporary register is used to hold data during memory-to-memory transfers. Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition.

Functional Description

DMA Operation
The SAB 8237A is designed to operate in two major cycles. These are called Idle and Activa cycles. Each device cycle is made up of a number of states. State I (SI)is the inactive state. It is entered when the SAB 8237A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the Program Condition, being programmed by the processor. State Ø (SØ) is the first state of a DMA service. The SAB 8237A has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the CPU will signal that transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (SW) can be inserted before S4 by the use of the Ready line on the SAB 8237A.
Memory-to-memory transfers require a read-from and a write-to-memory to complete each transfer. The states, which resemble the normal working states, use two digit numbers for identification. Eight states are required for each complete transfer. The first four states (S11, S12, S13, S14) are used for the read-from-memory half and the last four states (S21, S22, S23 and S24) for the write-to-memory half of the transfer.

Idle Cycle
When no channel is requesting service, the SAB 8237A will enter the Idle cycle and perform "SI" states. In this cycle the SAB 8237A will sample the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device will also sample $\overline{CS}$, looking for an attempt by the microprocessor to write or read the internal registers of the SAB 8237A.

Active Cycle
When the SAB 8237A is in the Idle cycle and a channel requests a DMA service, the device will output a HRQ to the microprocessor and enter the Active cycle. It is in this cycle that the DMA service will take place, in one of four modes:

Single Transfer Mode
In Single Transfer mode, the SAB 8237A will make a one-byte transfer during each HRQ/HLDA handshake. When DREQ goes active, HRQ will go active. After the CPU responds by driving HRQ active, a one-byte transfer will take place. Following the transfer, HRQ will go inactive, the word count will be decremented and the address will be either incremented or decremented.

Block Transfer Mode
In Block Transfer mode, the SAB 8237A will continue making transfers until a TC (caused by the word count going to zero) or an external End of Process ($\overline{EOP}$) is encountered.

Demand Transfer Mode
In Demand Transfer mode the device will continue making transfers until a TC or external $\overline{EOP}$ is encountered or until DREQ goes inactive. Thus, the device requesting service may discontinue transfers by bringing DREQ inactive. Service may be resumed by asserting an active DREQ once again.

Cascade Mode
This mode is used to cascade more than one SAB 8237A together for simple system expansion. The HRQ and HLDA signals from the additional SAB 8237A are connected to the DREQ and DACK signals of a channel of the initial SAB 8237A.

TRANSFER TYPES

Each of the three active transfer modes can perform three different types of transfers. These are Read, Write and Verify. Write transfers move data from an I/O device to the memory by activating $\overline{IOR}$ and $\overline{MEMW}$. Read transfers move data from memory to an I/O device by activating $\overline{MEMR}$ and $\overline{IOW}$. Verify transfers are pseudo transfers; the SAB8237A operates as in Read or Write transfers generating addresses, responding to $\overline{EOP}$, etc., however, the memory and I/O control lines remain inactive.

Memory-to-Memory

The SAB8237A includes a block move capability that allows blocks of data to be moved from one memory adress space to another. Channel Ø forms the source address and channel 1 forms the destination address. The channel 1 word count is used. A memory-to-memory transfer is initiated by setting a software DMA request for channel Ø.

Autoinitialize

By programming a bit in the Mode register a channel may be set up for an Autoinitialize operation. During Autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of that channel following $\overline{EOP}$.

Extended Write

For Flyby Transactions late write is normally used, as this allows sufficient time for the $\overline{IOR}$ signal to get data from the peripheral onto the bus before $\overline{MEMW}$ is activated. In some systems, performance can be improved by starting the write cycle earlier.

Address Generation

In order to reduce pin count, the SAB 8237A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch from which they may be placed on the address bus. The falling edge of Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a 3-state enable. The lower order address bits are output by the SAB 8237A directly. To save time and speed transfers, the SAB 8237A executes S1 states only when updating of A8–A15 in the latch is necessary.

Compressed Timing

In order to achieve even greater throughput where system characteristics permit, the SAB 8237A can compress the transfer time to two clock cycles. By removing state S3 the read pulse width is made equal to the write pulse width and a transfer consists only of state S2 to change the address and state S4 to perform the read/write.

Priority

The SAB 8237A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel Ø. The second schema is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly.

Software Commands

There are two special software commands which can be executed in the Program Condition.
Clear First/Last Flip/Flop: This command may be issued prior to writing or reading SAB 8237A address or word count information. This initializes the Flip/Flop to a known state so that subsequent accesses to register contents by the microprocessor will address lower and upper bytes in the correct sequence.
Master Clear: This software instruction has the same effect as the hardware Reset. The Command, Status, Request, Temporary and Internal First/Last Flip/Flop registers are cleared and the Mask register is set.

Absolute Maximum Ratings [1]

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to + 150°C
Voltage on Any Pin with Respect to Ground (VSS)	−0.5 to + 7 V
Power Dissipation	2 W

D.C. Characteristics

TA = 0 to 70°C; VCC = 5 V ± 5%; VSS = 0 V

Symbol	Parameter	Limit Values			Unit	Test Condition	
		Min.	Typ. [2]	Max.			
VOH	Output High Voltage	2.4	–	–	V	IOH = −200 µA	
		3.3				IOH = −100 µA (HRQ only)	
VOL	Output Low Voltage	–		0.40		IOL = 3.2 mA	
VIH	Input High Voltage	2.0		VCC+0.5		–	
VIL	Input Low Voltage	-0.5		0.8			
ILI	Input Load Current	–		±10	µA	0 V ≤ VIN ≤ VCC	
ILO	Output Leakage Current					0.4 V ≤ VOUT < VCC	
ICC	VCC Supply Current	–	110	130	mA	TA = +25°C	All outputs disconnected
			130	150		TA = 0°C	
CO	Output Capacitance		4	8	pF	fc = 1.0 MHz, Inputs = 0 V	
CI	Input Capacitance		8	15			
CIO	I/O Capacitance		10	18			

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) Typical values are for TA = 25°C, nominal supply voltage and nominal processing parameters.

A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = 5V ±5%; V_{SS} = 0V

DMA (Master) Mode

Symbol	Parameter	Limit Values				Unit
		8237A		8237A-5		
		Min.	Max.	Min.	Max.	
TAEL	AEN High from CLK Low (S1) Delay Time		300		200	
TAET	AEN Low from CLK High (S1) Delay Time		200		130	
TAFAB	ADR Active to Float Delay from CLK High	–	150	–	90	
TAFC	$\overline{READ}$ or $\overline{WRITE}$ Float from CLK High		150		120	
TAFDB	DB Active to Float Delay from CLK High		250		170	
TAHR	ADR from $\overline{READ}$ High Hold Time	TCY–100		TCY–100		
TAHS	DB from ADSTB Low Hold Time	50	–	40	–	
TAHW	ADR from $\overline{WRITE}$ High Hold Time	TCY –50		TCY –50		
TAK	DACK Valid from CLK Low Delay Time [1]		250		170	
	$\overline{EOP}$ High from CLK High Delay Time [2]	–	250	–	170	
	$\overline{EOP}$ Low to CLK High Delay Time		250		170	
TASM	ADR Stable from CLK High		250		170	
TASS	DB to ADSTB Low Setup Time	100		100	ns	ns
TCH	CLK High Time (transitions ≤ 10 ns)	120	–	80	–	
TCL	CLK Low Time (transitions ≤ 10 ns)	150		68		
TCY	CLK Cycle Time	320		200		
TDCL	CLK High to $\overline{READ}$ or $\overline{WRITE}$ Low Delay [3]		270		190	
TDCTR	$\overline{READ}$ High from CLK High (S4) Delay Time [3]		270		190	
TDCTW	$\overline{WRITE}$ High from CLK High (S4) Delay Time [3]	–	200	–	130	
TDQ1	HRQ Valid from CLK High Delay Time [4]		160		120	
TDQ2			250		120	
TEPS	$\overline{EOP}$ Low from CLK Low Setup Time	60	–	40	–	
TEPW	$\overline{EOP}$ Pulse Width	300		220		
TFAAB	ADR Float to Active Delay from CLK High		250		170	
TFAC	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK High		200		150	
TFADB	DB Float to Active Delay from CLK High		300		200	

Notes see next page.

Symbol	Parameter	Limit Values				Unit
		8237A		8237A-5		
		Min.	Max.	Min.	Max.	
THS	HLDA Valid to CLK High Setup Time	100		75		
TIDH	Input Data from $\overline{MEMR}$ High Hold Time	0		0		
TIDS	Input Data to $\overline{MEMR}$ High Setup Time	250		170		
TODH	Output Data from $\overline{MEMW}$ High Hold Time	20	–	10	–	ns
TODV	Output Data Valid to $\overline{MEMW}$ High [5]	200		125		
TQS	DREQ to CLK Low (S1, S4) Setup Time [1]	0		0		
TRH	CLK to READY Low Hold Time	20		20		
TRS	READY to CLK Low Setup Time	100		60		
TSTL	ADSTB High from CLK High Delay Time	–	200	–	130	
TSTT	ADSTB Low from CLK High Delay Time		140		90	
TQH	DREQ from DACK Valid Hold Time	0	–	0	–	
TRQHA	HRQ to HLDA Delay Time	1		1		clk

1) DREQ and DACK signals may be active high or low. Timing diagrams assume the active high mode.

2) $\overline{EOP}$ is an open collector output. This parameter assumes the presence of a 2.2 kΩ pullup to *VCC*.

3) The net $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be TCY -100 ns and for extended write will be 2TCY -100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY -50 ns and for compressed read will be TCY -50 ns.

4) TDQ is specified for two different output high levels. TDQ1 is measured at 2.0 V. TDQ2 is measured a 3.3 V. The value for TDQ2 assumes an external 3.3 kΩ pull-up resistor connected from HRQ to *VCC*.

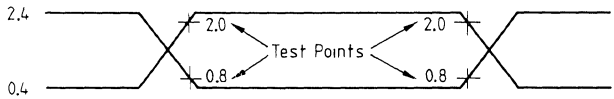
5) If N wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by N (TCY).

Peripheral (Slave) Mode

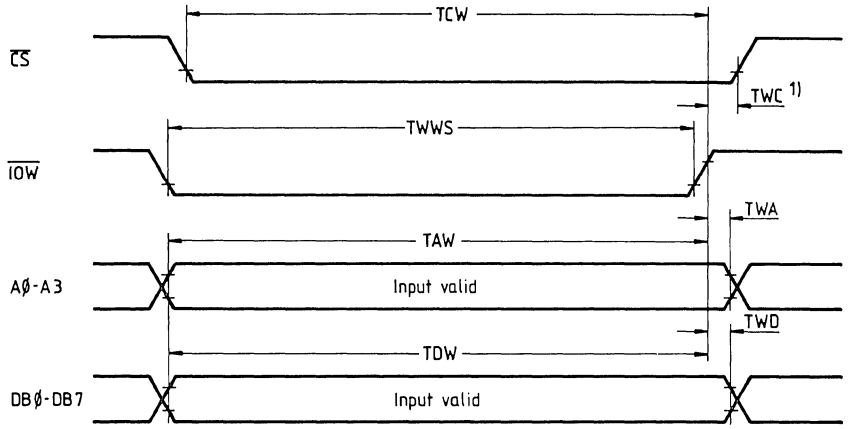
Symbol	Parameter	Limit Values				Unit
		8237A		8237A-5		
		Min.	Max.	Min.	Max.	
TAR	ADR Valid or $\overline{CS}$ Low to $\overline{READ}$ Low	50		50		
TAW	ADR Valid to $\overline{WRITE}$ High Setup Time	200		130		
TCW	$\overline{CS}$ Low to $\overline{WRITE}$ High Setup Time	200	–	130	–	
TDW	Data Valid to $\overline{WRITE}$ High Setup Time	200		130		
TRA	ADR or $\overline{CS}$ Hold from $\overline{READ}$ High	0		0		
TRDE	Data Access from $\overline{READ}$ Low [1]	–	200	–	140	
TRDF	DB Float Delay from $\overline{READ}$ High	20	100	0	70	ns
TRSTD	Power Supply High to RESET Low Setup Time	500		500		
TRSTS	RESET to First $\overline{IOWR}$	2 TCY		2 TCY		
TRSTW	RESET Pulse Width	300		300		
TRW	$\overline{READ}$ Width	300	–	200	–	
TWA	ADR from $\overline{WRITE}$ High Hold Time	20		20		
TWC	$\overline{CS}$ High from $\overline{WRITE}$ High Hold Time	20		20		
TWD	Data from $\overline{WRITE}$ High Hold Time	30		30		
TWWS	$\overline{WRITE}$ Width	200		160		

1) Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.

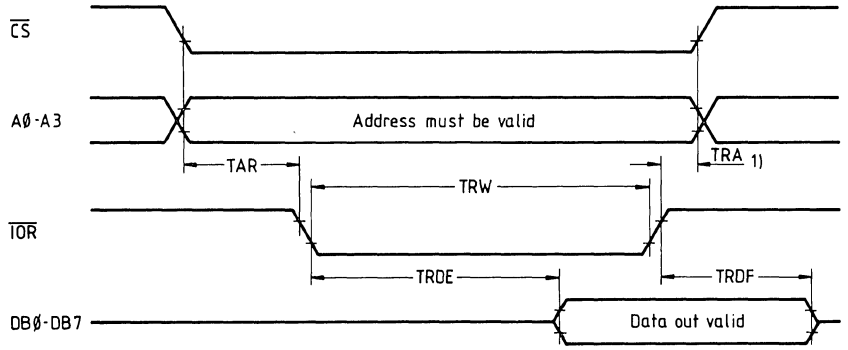
Input Waveforms for AC-Tests



Slave Mode Write Timing

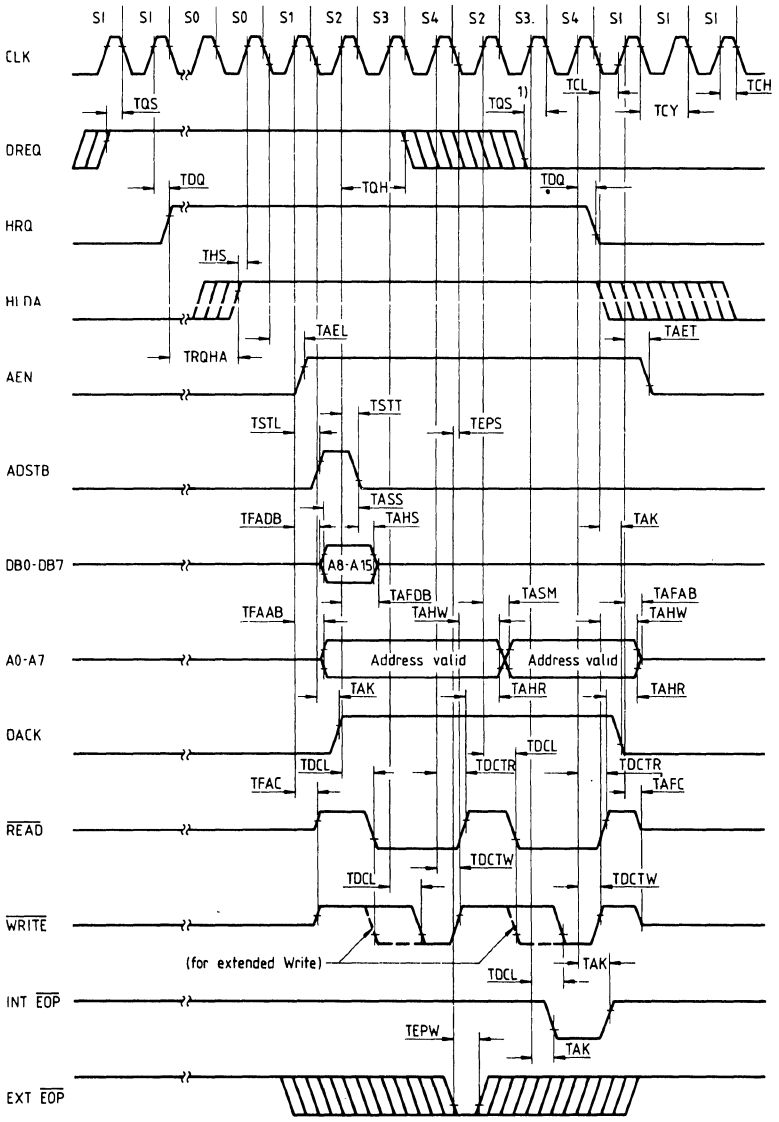


Slave Mode Read Timing



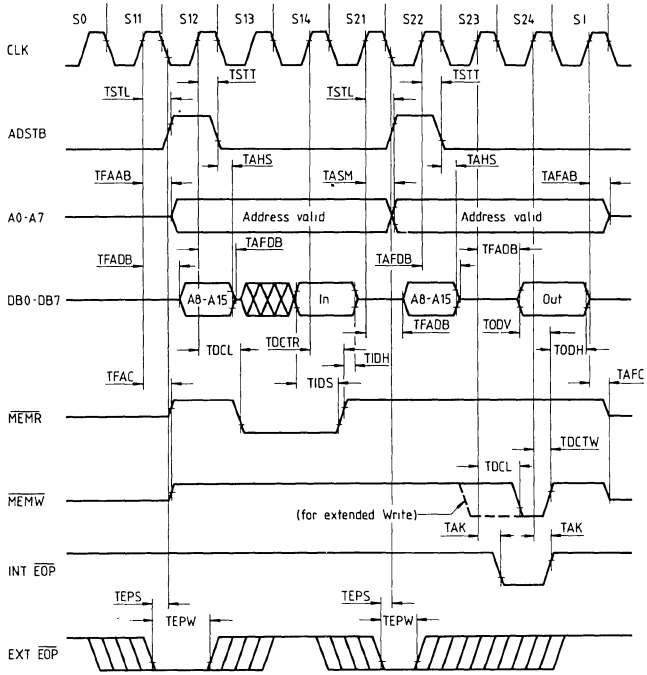
1) Successive read and/or write operation by the CPU to program or examine the controller must be timed to allow at least 600 µs for the SAB 8237A and at least 400 ns for the SAB 8237A-5, as recovery time between active read or write pulses.

DMA Transfer Timing

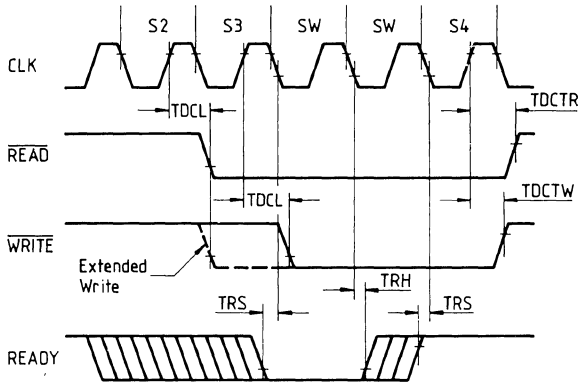


1) DREQ should be held active until DACK is returned.

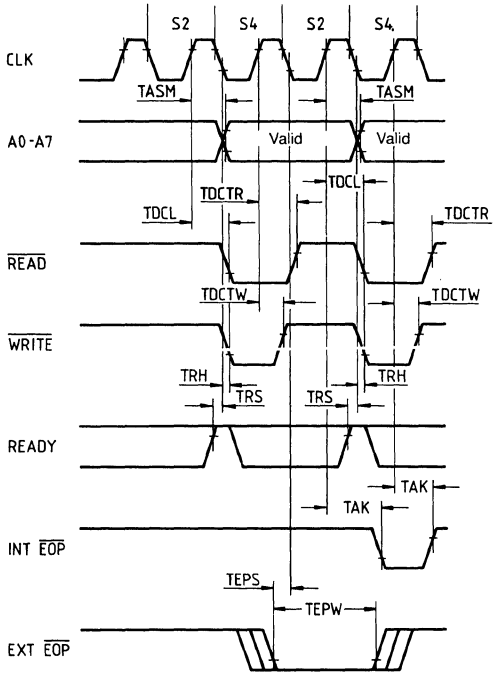
Memory-to-Memory Transfer Timing



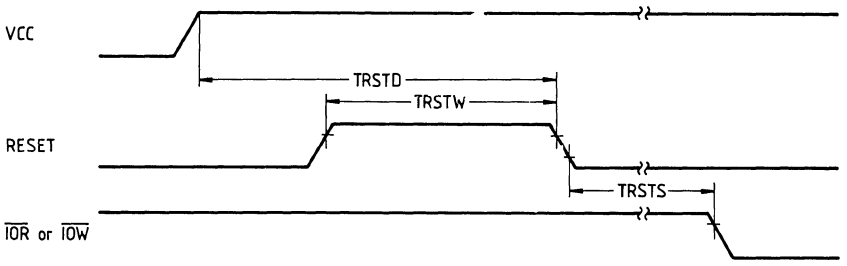
Ready Timing



Compressed Transfer Timing



Reset Timing

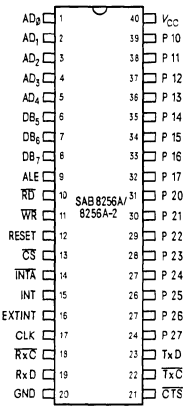


Preliminary

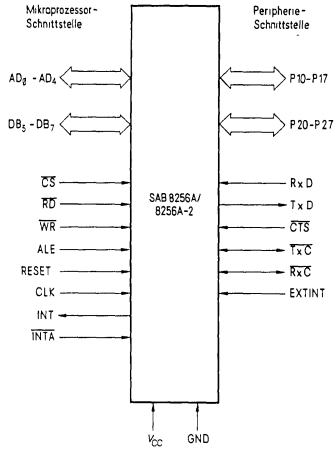
SAB 8256A, SAB 8256A-2 Programmable Multifunction UART (MUART)

- SAB 8256A compatible with processors up to 3 MHz system clock (e. g. SAB 8085A, SAB 8048, SAB 8051).
  SAB 8256A-2 compatible with processors up to 8 MHz system clock (e.g. SAB 8085A-2, SAB 8086 - minimum mode, SAB 80186).
- Full-Duplex asynchronous serial interface with programmable 5–8 data bits, 0.75–2 stop bits, parity generation and checking.
- Internal baud rate generator programmable for 50–19200 Baud; 0–1 Megabaud possible with external baud rate clock.
- Interrupt Controller with 8 priority levels; each level independently maskable, programmable for normal and fully nested operation with SAB 8085 and SAB 8086 processor families.
- Five programmable 8-bit counter/timers, internal or external clock, four are cascadable to two 16-bit counter/timers.
- Two 8-bit I/O ports, bit programmable for input/output, hand-shake mode supported.

Pin Configuration



Logic Symbol



SAB 8256A integrates four of the most used peripheral functions in a microcomputer system into a 40 pin package: serial interface, parallel interface, timer/counter and interrupt controller. It is primarily suited for system like SAB 8048, SAB 8085, SAB 8086, SAB 8088, SAB 80186 and SAB 80188 which have a multiplexed bus. With some additional circuitry, it can also be used with other processors. All the functions of SAB 8256A are programmable by software, leading to a great flexibility in system design.

AG 2/85

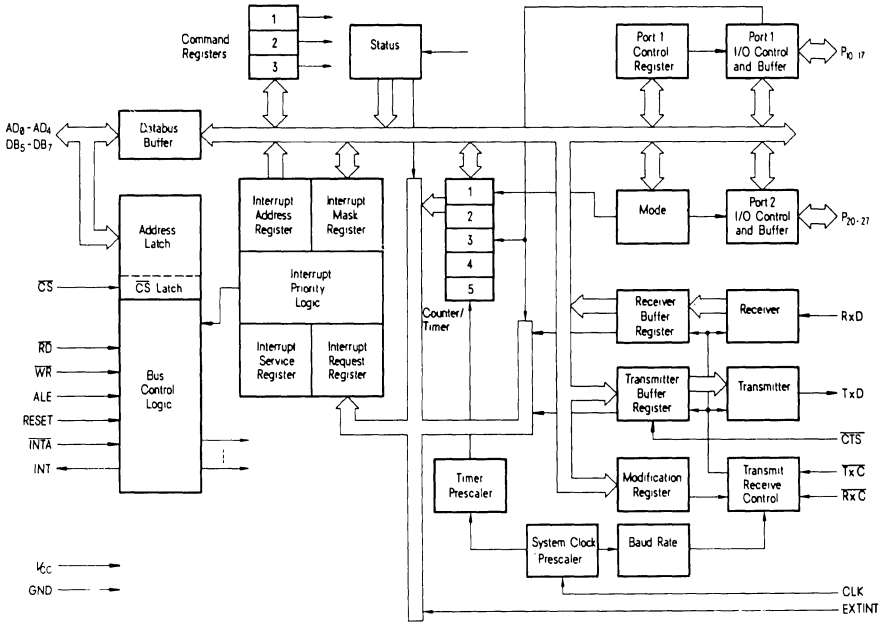
Pin Description and Functions

Symbol	Pin No.	Input (I) Output (O)	Function
AD0 – AD4, DB5 – DB7	1 – 8	I/O	**Interface to Multiplexed Bus** Bidirectional lines to 8 data bits and 5 least significant address bits which are latched internally on the falling edge of ALE.
ALE	9	I	**Adress Latch Enable** The five least significant address bits and $\overline{CS}$ are latched on the falling edge of ALE into an internal register.
$\overline{RD}$	10	I	**Read Control** The microprocessor reads data from the chip when this signal is low.
$\overline{WR}$	11	I	**Write Control** The microprocessor writes data into the chip with a low on this pin.
RESET	12	I	**Reset** A high on this pin forces the chip to its initial state. The chip remains in this state till control information is written into the chip.
$\overline{CS}$	13	I	**Chip Select** A low on this pin during ALE enables the bus interface of the chip. Neither read nor write operations are possible without this enable. The signal has no effect on the internal operation of the chip.
$\overline{INTA}$	14	I	**Interrupt Acknowledge** The microprocessor informs the chip a low on this pin that an interrupt request is being serviced, if this functions has been enabled.
INT	15	O	**Interrupt Request** The chip demands interrupt service from the microprocessor with a high on this output.
EXTINT	16	I	**External Interrupt** An external source can request interrupt service through this input. The source can be either a peripheral or another SAB 8256A with its INT pin as the signal source. The input is level sensitive (high). The request must be held high until the processor acknowledges it.
CLK	17	I	**System Clock** Clock on this input is the reference clock for various function like timers, baud rate generator etc.

Symbol	Pin No.	Input (I) Output (O)	Function
$\overline{R \times C}$	18	I/O	**Receiver Clock** If this pin is programmed as an output, it provides a low-to-high transition at the sampling point of each received data bit (excluding the framing bits). When programmed as an input, an externally generated receiver clock must be connected to this pin. At DC, its frequency can range up to 1.024 MHz matching the receiver baud rate. The internal baud rate generator is disabled if this pin is used as input.
R×D	19	I	**Receiver Data** Input for serial data, which is converted to parallel format while discarding the framing bits and then is made available for the processor.
$\overline{CTS}$	21	I	**Clear to Send** This input enables the serial transmitter. If 1, 1.5 or 2 stop bits are selected, $\overline{CTS}$ is level sensitive. As long as $\overline{CTS}$ is low, any character loaded into the transmitter buffer register will be transmitted serially. For continuous transmission, this input must be tied to low. A single negative going pulse causes the transmission of a single character previously loaded into the transmitter buffer register. If the transmitter buffer is empty, this pulse will be ignored. If this pulse occurs during the transmission of a character upto the time where 0.5 of the first (or the only) stop bit is sent out, it will be ignored. If it occurs afterwards, but before the end of the stop bits the next character will be transmitted immediatly following the current one. If $\overline{CTS}$ is still high when the transmitter register is sending the last stop bit, the transmitter will enter its idle state until the next high-to-low transition on $\overline{CTS}$ occurs. If 0.75 stop bits is chosen, $\overline{CTS}$ input is edge sensitive. A negative edge on $\overline{CTS}$ results in the immediate transmission of the next character. The length of the stop bits is determined by the time interval between the beginning of the first stop bit and the next negative edge on $\overline{CTS}$. A high-to-low transition has no effect if the transmitter buffer is empty or if the time interval between the beginning of the stop bit and next negative edge is less than 0.75 bit. A high or a low level or a low-to-high transition has no effect on the transmitter for the 0.75 stop bit mode.
$\overline{T \times C}$	22	I/O	**Transmitter Clock** The function of this pin can be programmed in 3 configurations. As an output it delivers the transmitter clock corresponding to the baud rate. If programmed as an input, an external clock of 32 or 64 times the baud rate that is common to transmitter and receiver, or a 1× clock matching the baud rate which is used for the transmitter only, can be tied to this pin. The maximum frequency is 1.024 MHz. Thus, baud rates ranging from 0 to 16 Kbaud (64×) or from 0 to 32 Kbaud (32×) or from 0 to 1.024 Mbaud (1×) are possible. The internal baud rate generator is disabled if $\overline{T \times C}$ is selected as input.

Symbol	Pin No.	Input (I) Output (O)	Function
TxD	23	O	**Transmitter Data** Serial data output. The parallel data received from the processor and the framing bits added by the SAB 8256A are sent out serially over this output when the transmitter is enabled by the $\overline{CTS}$ signal.
P27–P20	24–31	I/O	**Parallel I/O Port 2** The eight general purpose I/O pins of parallel port 2 can be configured in sets of four pins (nibbles) as inputs or outputs or 8 bit I/O with handshake (control-signals at port 1). In the nibble mode the output signals are latched whereas the input signals are not. In the handshake mode both inputs and outputs are latched.
P17–P10	32–39	I/O	**Parallel I/O Port 1** Each one of these 8 pins can be programmed as input or output. Alternatively these pins can serve as control pins which extends considerably the functional spectrum of the chip. The pins are assigned special functions implicitly by programming. All outputs are latched whereas inputs are not.
V_{CC}	40	–	**Power Supply** (+5 V)
GND	20	–	**Ground** (0 V)

Block Diagram



Functional Description

Bus Interface

The bus interface unit, consisting of bus drivers, address latches and bus control logic, interfaces the SAB 8256A to the data, address and control busses of a microcomputer system. The chip is selected by the $\overline{CS}$ signal, which is latched into the chip along with address lines AD0–AD4 by the ALE signal. $\overline{WR}$ and $\overline{RD}$ signals are used to write data into and read data from SAB 8256A.
Signals INT und $\overline{INTA}$ are used to handle interrupt protocol with the processor.
RESET signal resets the chip to its initial state.

Counter/Timer

Five programmable counter/timers can be used in several modes. Each can be used as an 8-bit timer while two can alternatively serve as counters. Counter/timer 2 and timer 4 as well as 3 counter/timer and timer 5 can be cascaded to 16-bit counter/timers. All counter/timers function as binary down-counters with a programmable initial value and generate an interrupt request on their 1 to 0 transition. An internal register is provided for the initial count of timer 5 and with an external trigger pulse it is possible to reload the initial value into timer 5 (also for cascaded counter/timer 3 and timer 5).
A common clock source with a frequency of either 1 KHz or 16 KHz is available for the timers. In addition, for counters 2, 3 and the cascaded counters, an external clock source can be provided through two pins of part 1.

Asynchronous Serial Interface

For double buffered full-duplex operations both transmitter and receiver have two registers. The received data (5 to 8 data bits, programmable) is assembled to parallel format in the receiver register, the framing bits (Start, Stop, and Parity) are stripped off and stored into the receiver buffer register. The data to be transmitted is first loaded into the transmitter buffer register and then sent out through the transmitter register.
Controlling the $\overline{CTS}$ signal, single characters on character strings can be transmitted. Baud rate clock (50 to 19,200 Baud) is generated on the chip which is common to both the receiver and the transmitter. It is also possible to provide an external baud rate clock (common or separate for receiver and transmitter) to provide baud rates from 0 to 1.024 Mbaud.

Parallel Interface

The parallel interface consists of two 8-bit ports programmable as inputs or outputs. Each pin of port 1 can be programmed separately as an input or an output. They can also be used as control pins. Ports 2 can be programmed as input our output in two 4-bit groups. Port 2 can also be used as an 8-bit input or output port with handshake signals.

Assignment of Control Signals to Port 1

Pins Port 1	P17	P16	P15	P14	P13	P12	P11	P10
Control Function	External interrupt input	Break-In detect input	Trigger input for timer 5 (cascaded counter/timer 3+5)	Output of the clock of the internal baudrate-generator	Clock input for counter 3	Clock input for counter 2	Handshake Control Signals for Port 2	

Interrupt Controller

The interrupt controller manages 12 interrupt sources (10 internal and 2 external) on 8 priority levels. Normal (every interrupt request immediately recognized) and "fully nested" (recognition based on priority) modes are supported.
The interrupt controller supports various methods of connecting SAB 8256A to the processor. Firstly, the true interrupt mode (using INT and $\overline{\text{INTA}}$ signals for interrupt protocol), secondly, a combination of polling and interrupt (using INT and interrupt address registers). The interrupt protocols of SAB 8048, SAB 8085A, SAB 8086, SAB 8088, SAB 80186 and SAB 80188 are directly supported.

Programming the SAB 8256A

The functional characteristics of SAB 8256A can be programmed by writing appropriate control information into it. It is specially designed for ease of programming. It is hence possible to alter individual bits in certain registers like e.g. the Interrupt Mask Register and Command Register 3. All functions of SAB 8256A can be easily used because each unit (e.g. counter/timer, serial interface) has specially assigned registers which can be directly read or written.

Register Select

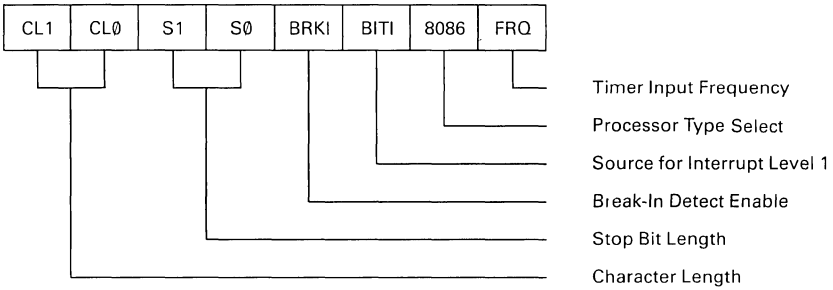
Write Registers								Address				Read Registers							
								SAB 8085 Mode: AD3	AD2	AD1	ADØ								
								SAB 8086 Mode: AD4	AD3	AD2	AD1								
CL1	CLØ	S1	SØ	BRKI	BITI	8086	FRQ	Ø	Ø	Ø	Ø	CL1	CLØ	S1	SØ	BRKI	BITI	8086	FRQ
Command Word 1												Command Register 1							
PEN	EP	C1	CØ	B3	B2	B1	BØ	Ø	Ø	Ø	1	PEN	EP	C1	CØ	B3	B2	B1	BØ
Command Word 2												Command Register 2							
SET	R×E	IAE	NIE	END	SBRK	TBRK	SRES	Ø	Ø	1	Ø	Ø	R×E	IAE	NIE	Ø	SBRK	TBRK	Ø
Command Word 3												Command Register 3							
T35	T24	T5C	CT3	CT2	P2C2	P2C1	P2C0	Ø	Ø	1	1	T35	T24	T5C	CT3	CT2	P2C2	P2C1	P2C0
Mode Word												Mode Register							
P17	P16	P15	P14	P13	P12	P11	P10	Ø	1	Ø	Ø	P17	P16	P15	P14	P13	P12	P11	P10
Port 1 Control Word												Port 1 Control Register							
L7	L6	L5	L4	L3	L2	L1	L0	Ø	1	Ø	1	L7	L6	L5	L4	L3	L2	L1	L0
Interrupt-Level Enable Word												Interrupt Mask Register							

Write Registers								Address				Read Registers							
								SAB 8085 Mode: AD3	AD2	AD1	AD0								
								SAB 8086 Mode: AD4	AD3	AD2	AD1								
L7	L6	L5	L4	L3	L2	L1	L0	0	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Interrupt-Level Disable Word												Interrupt Address Register							
D7	D6	D5	D4	D3	D2	D1	D0	0	1	1	1	D7	D6	D5	D4	D3	D2	D1	D0
Transmitter Buffer												Receiver Buffer							
D7	D6	D5	D4	D3	D2	D1	D0	1	0	0	0	D7	D6	D5	D4	D3	D2	D1	D0
Write Port 1												Read Port 1							
D7	D6	D5	D4	D3	D2	D1	D0	1	0	0	1	D7	D6	D5	D4	D3	D2	D1	D0
Write Port 2												Read Port 2							
D7	D6	D5	D4	D3	D2	D1	D0	1	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Write Timer 1												Read Timer 1							
D7	D6	D5	D4	D3	D2	D1	D0	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0
Write Timer/Counter 2												Read Timer/Counter 2							

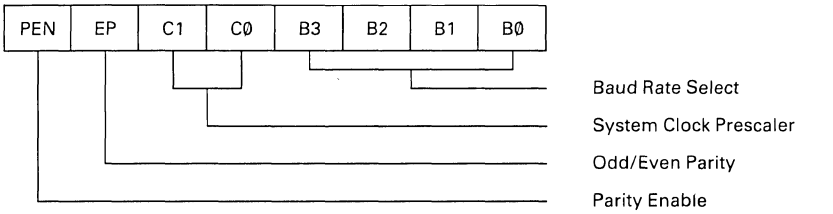
Write Registers								Address				Read Registers							
								SAB 8085 Mode: AD3	AD2	AD1	AD0								
								SAB 8086 Mode: AD4	AD3	AD2	AD1								
D7	D6	D5	D4	D3	D2	D1	D0	1	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0
Write Timer/Counter 3												Read Timer/Counter 3							
D7	D6	D5	D4	D3	D2	D1	D0	1	1	0	1	D7	D6	D5	D4	D3	D2	D1	D0
Write Timer 4												Read Timer 4							
D7	D6	D5	D4	D3	D2	D1	D0	1	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Write Timer 5												Read Timer 5							
0	RS4	RS3	RS2	RS1	RS0	TME	DSC	1	1	1	1	INT	RBF	TBE	TRE	BD	PE	OE	FE
Modification Word												Status Register							

Programming

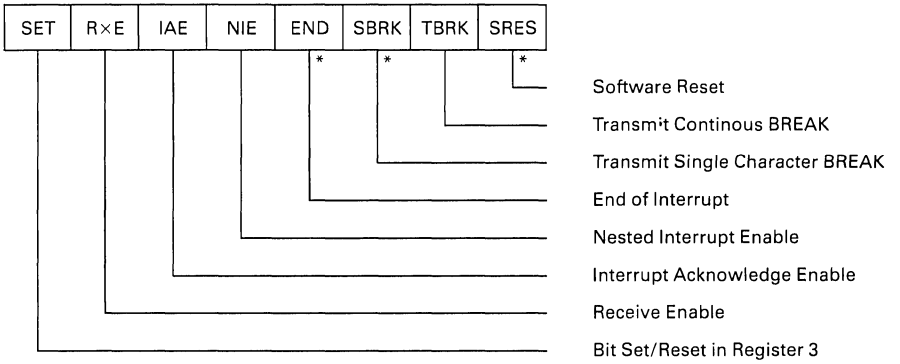
Command Word 1



Command Word 2

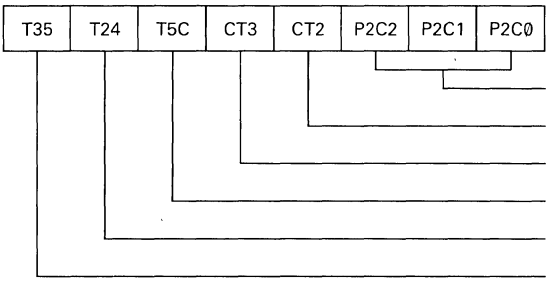


Command Word 3

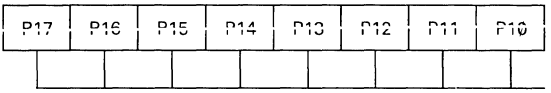


*) These bits can only be set, they are reset at the end of the operation.

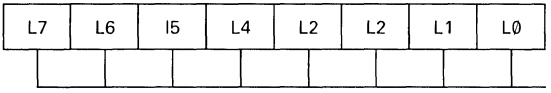
Mode Word



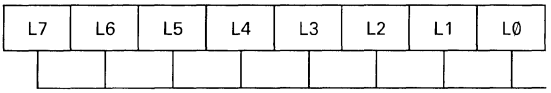
Port 1 Control World



Interrupt-Level Enable Word

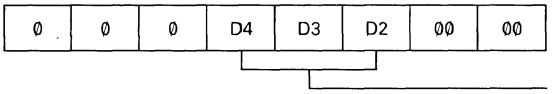


Interrupt-Level Disable Word



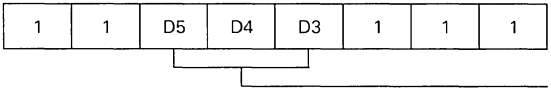
Determination of Interrupt Level

Reading the Interrupt Address Register



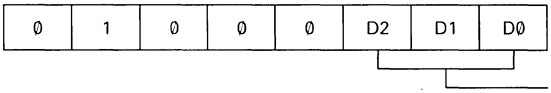
Response to $\overline{INTA}$

SAB 8085-Mode (RST-instruction in response to $\overline{INTA}$)



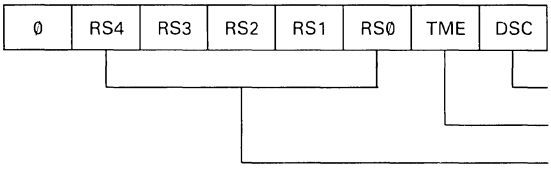
Interrupt Level

SAB 8086-Mode (Interrupt Vector in response to second $\overline{INTA}$)



Interrupt Level

Modification Word

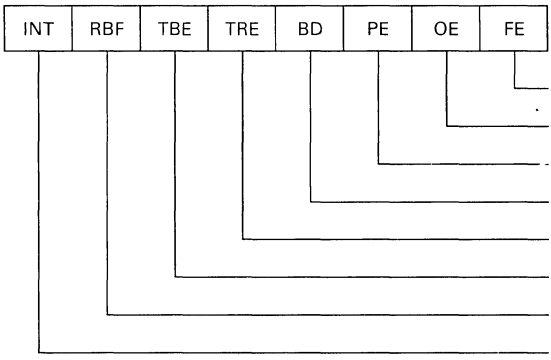


Disable Start Bit Check

Transmission Mode Enable

Receiver Sampling Point

Status Register



Framing Error/Transmission Mode Indication

Overrun Error

Parity Error

Break Detect or Break-in Detect

Transmitter Register Empty

Transmitter Buffer Empty

Receiver Buffer Full

Interrupt Pending

Absolute Maximum Ratings [1]

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin With Respect to Ground	−0.5 to +7 V
Power Dissipation	1 W

D.C. Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V
(when not otherwise specified)

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	–
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5		
V_{OL}	Output Low Voltage	–	0.45		I_{OL} = 2.5 mA
V_{OH}	Output High Voltage	2.4	–		I_{OH} = −400 µA
I_{IL}	Input Leakage	–	±10	µA	V_{IN} = 0 V to V_{CC}
I_{LO}	Output Leakage Current				V_{OUT} = 0 V to V_{CC}
I_{CC}	V_{CC} Supply Current		190	mA	–

Capacitance [2]

Symbol	Parameter	Limit Value (Max.)	Unit	Test Condition
C_{IN}	Input Capacitance	10	pF	f_C = 1 MHz Unmeasured pins returned to GND
$C_{I/O}$	I/O Capacitance	20		

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2) This parameter is periodically sampled and not 100% tested.

A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5V ± 5%; V_{SS} = 0V

Test Conditions

Capacitive load C_L = 150 pF

The timings are with respect to the following levels:

H-level: 2.0V
L-level: 0.8V
Rise and fall times: 20 ns

The timings are valid for an internal clock of 1.024 MHz.

Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8256A		SAB 8256A-2			
		Min.	Max.	Min.	Max.		
t AC	$\overline{STB}$ ↓ to $\overline{IBF}$ ↓	–	300	–	300	ns	–
t ACK	$\overline{ACK}$ Pulse Width	t ADP	–	t ADP	–	–	
t AD	Address Stable to Data Valid	–	400	–	230	ns	
t ADP	$\overline{ACK}$ ↓ to $\overline{OBF}$ ↑		300		300		
t AED	$\overline{OBF}$ ↓ to $\overline{ACK}$ ↓	0	–	0	–		
t AI	$\overline{ACK}$ ↑ to INT ↑	–	1.5 t CY	–	1.5 t CY	–	
t AL	Address Stable to ALE ↓	50	–	30	–	ns	
t CC	$\overline{RD}$ and $\overline{WR}$ Pulse widths	300		200			
t CL	$\overline{RD}$ ↑ or $\overline{WR}$ ↑ to Next ALE ↑	50		25			
t CPI	Counter input Cycle Time (P12, P13,)	2.2		2.2		µs	
t CSL	$\overline{CS}$ Stable to ALE ↓	60		10		ns	
t CTS	$\overline{CTS}$ Pulse Width for Single Character Transmission	[1])		[1])		–	
t CY	System Clock Period	300		195		ns	–
t DEI	$\overline{STB}$ ↑ to INT ↑	–	1.5 t CY	–	1.5 t CY	–	
t DEX	EXTINT ↑ to INT ↑		200		200	ns	
t DH	$\overline{STB}$ ↑ to P2 Data Stable	10	–	10	–		
t DPI	Interrupt Request on P17 to INT ↑	–	1.5 t CY	–	1.5 t CY	–	
t DSI	P2 Data Stable before $\overline{STB}$ ↓	10	–	10	–	ns	
t DTX	$\overline{T \times C}$ ↓ to T×D Data Valid	–	300	–	300		
t DW	Data Valid before $\overline{WR}$ ↑	250	–	150	–		
t HEA	EXTINT ↓ after $\overline{INTA}$ ↑ or $\overline{RD}$ ↑	30		30			
t HIA	INT ↓ after $\overline{INTA}$ ↑ or $\overline{RD}$ ↑	–	300	–	300		
t LA	$\overline{CS}$ and Address valid after ALE ↓	50	–	20	–		
t LC	ALE ↓ to $\overline{RD}$ ↓ or $\overline{WR}$ ↓	60		20			
t LL	ALE Pulse width	100		50			

Notes see next page.

Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8256A		SAB 8256A-2			
		Min.	Max.	Min.	Max.		
t_{PI}	Pulse Width of Interrupt Request on P17	1.1	–	1.1	–	µs	–
t_{PP}	Counter 5 Load (P15↓) before Next Clock Pulse on P13 ↑			1.1			
t_{PR}	P1, P2 Data Stable before $\overline{RD}$ ↓	300		300		ns	
t_{RD}	Data Valid after $\overline{RD}$ ↓	–	200	–	150		
t_{RDE}	$\overline{RD}$ ↓ to Data Drivers Active	10	100	10	50		
t_{RDF}	Data Bus Float After $\overline{RD}$ ↑						
t_{RES}	RESET Pulse Width	300	–	300	–		
t_{RI}	$\overline{RD}$ ↑ to $\overline{IBF}$ ↑	–	300	–	300		
t_{RP}	P1, P2 Data Hold after $\overline{RD}$ ↑	50	–	50	–		
t_{RRD}	Data Bit Start to R×C ↓	300	[2]	150	[2]		[3]
t_{RV}	$\overline{RD}$ ↑ or $\overline{WR}$ ↑ to Next $\overline{RD}$ ↓ or $\overline{WR}$ ↓						$\overline{CS}$=Low
t_{SCY}	Serial Clock Period (32×, 64×)	975		975			–
t_{SPD}	Serial Clock High (32×, 64×)	350		350			
t_{SPW}	Serial Clock Low (32×, 64×)						
t_{STB}	Strobe Pulse Width	t_{AC}	–	t_{AC}	–	–	
t_{TCY}	Serial Clock Period (1×)	975		975		ns	
t_{TPD}	Serial Clock High (1×)	350		350			
t_{TIH}	Load Pulse for Counter 5 (P15)-High	1.1		1.1		µs	
t_{TIL}	Load Pulse for Counter 5 (P15)-Low						
t_{TPI}	Counter Input ↑ (P12, P13) to INT ↑ at Terminal Count	–	2.5	–	2.5		–
t_{TPW}	Serial Clock Low (1)	350	–	350	–	ns	
t_{TRV}	Time between 2 readcycles onto the same counter/timer	1.1		1.1		µs	
t_{WD}	Data Hold after $\overline{WR}$ ↑	40		30		ns	
t_{WP}	P1, P2 Data Valid after $\overline{WR}$ ↑	–	300	–	300		
t_{WPH}	Count Clock (P12, P13) High	1.1	–	1.1	–	µs	
t_{WPL}	Count Clock (P12, P13) Low						
t_{WPO}	$\overline{OBF}$ ↑ after $\overline{WR}$ ↓	–	300	–	300	ns	
t_f	Clock Fall Time		30		30		
$t_{\Phi H}$	Clock High	105	–	65	–		
$t_{\Phi L}$	Clock Low						
t_r	Clock Rise Time	–	30	–	30		

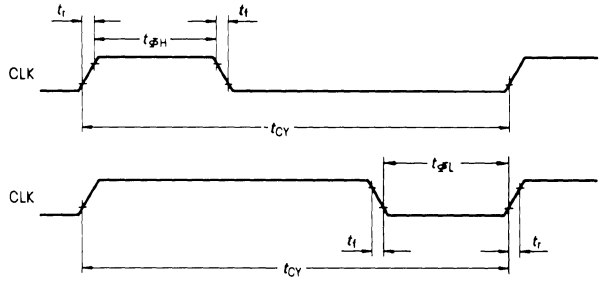
[1]) 1/32 bit length with transmitter clock with a baud rate factor of 32 or 64
100 ns when baud rate factor = 1

[2]) 300 ns + (1/32 bit length)

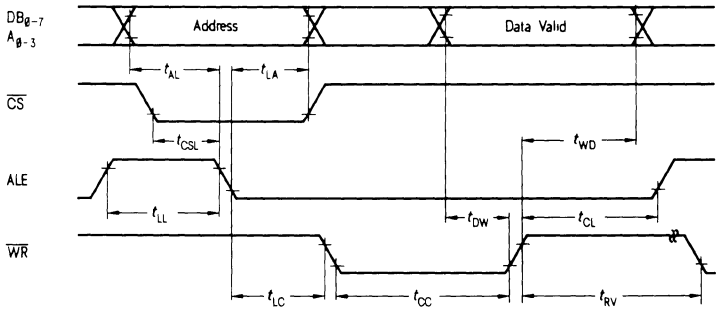
[3]) Sampling time at bit center

Waveforms

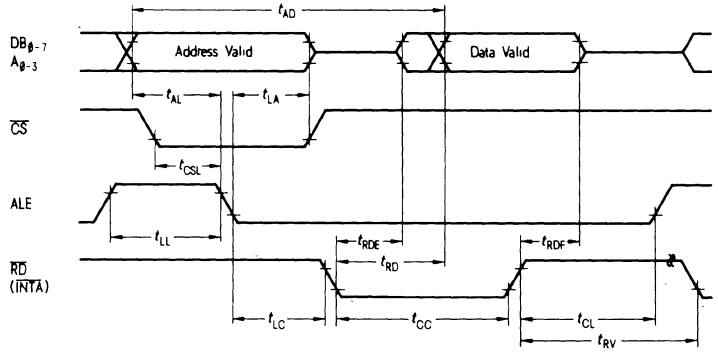
System Clock



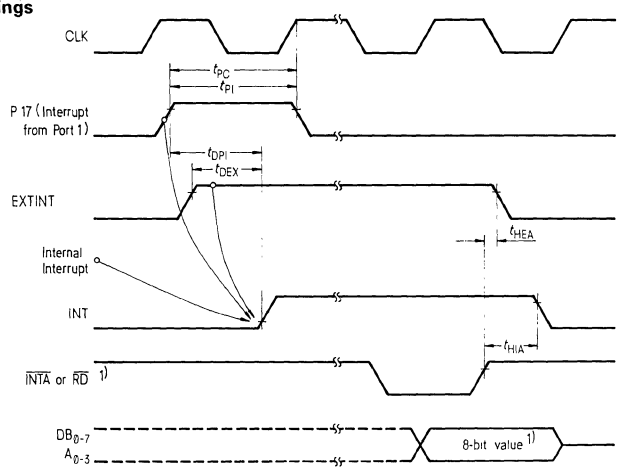
Write Cycle (Processor → SAB 8256A)



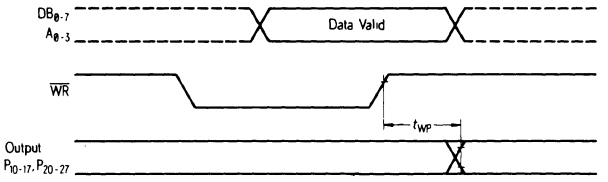
Read Cycle (SAB 8256A → Processor)



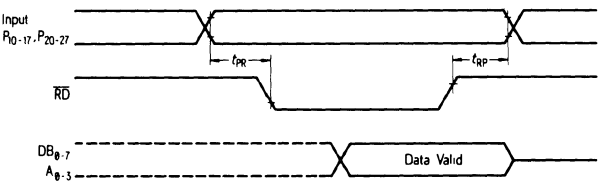
Interrupt Timings



Basic Output from Port 1 and Port 2

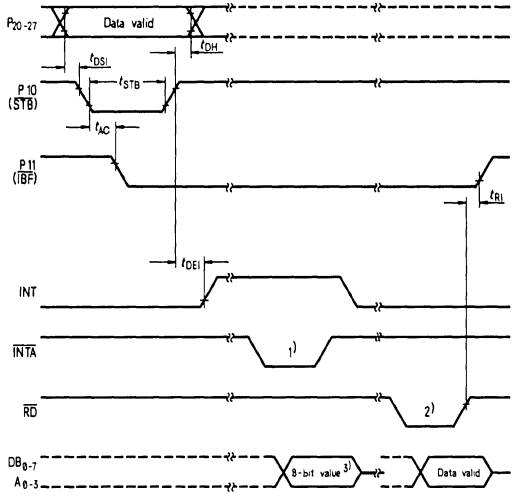


Basic Input from Port 1 and Port 2

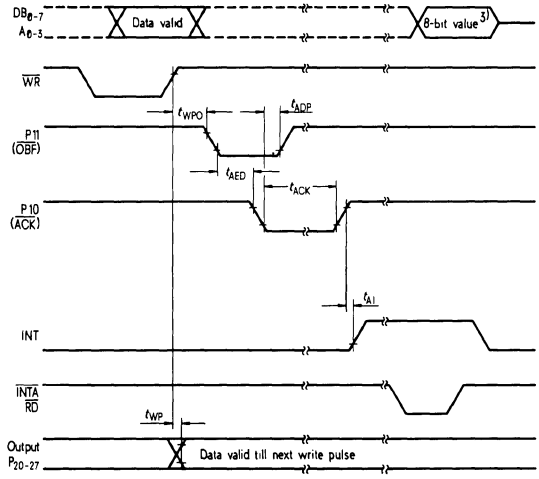


1) If $\overline{\text{INTA}}$ is enabled, RSTn instruction is output on $\overline{\text{INTA}}$ (SAB 8085 mode) or interrupt vector is output on second $\overline{\text{INTA}}$ (SAB 8086 mode) otherwise, interrupt address is output on a read address register operation.

Input from Port 2 in Hand-shake mode
(Control signals from Port 1)

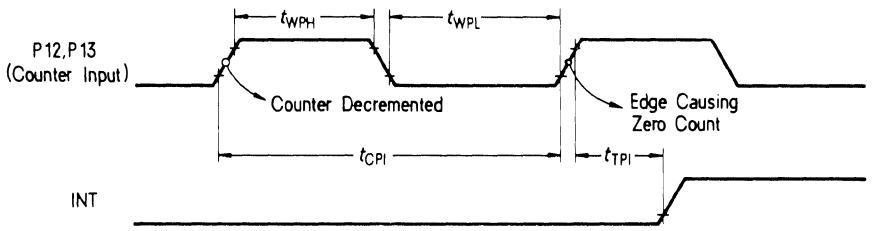


Output from Port 2 in Hand-shake mode
(Control signals from Port 1)

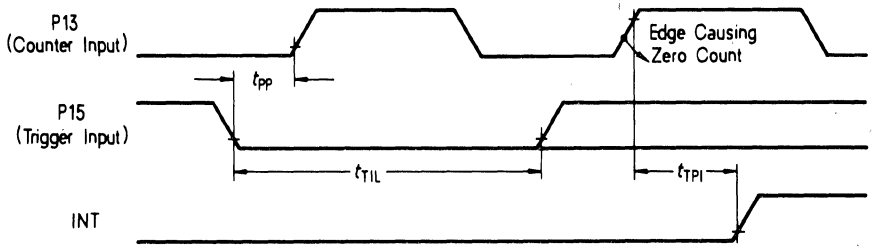


1) Instead of $\overline{INTA}$, $\overline{RD}$ can serve as interrupt acknowledge (reading the interrupt address register).
2) Read from channel 2.
3) If $\overline{INTA}$ is enabled, RSTn instruction is output on $\overline{INTA}$ (SAB 8085 mode) or interrupt vector is output on second $\overline{INTA}$ (8086 mode) otherwise, interrupt address is output on a read address register operation.

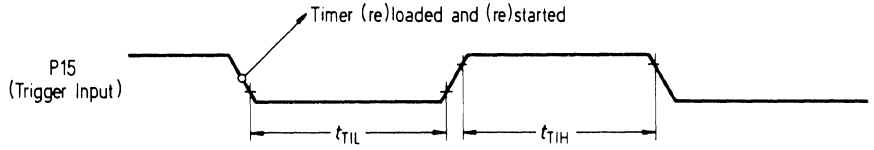
Count Pulse Timings and Zero-Crossing of Counter



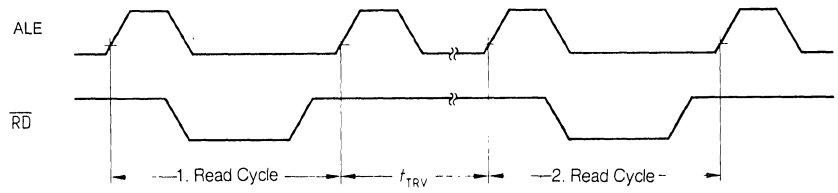
Loading Timer 5 (or Cascaded Counter/Timer 3 and 5) and Zero-Crossing of Counters (Cascaded Counter/Timer 3 and 5)



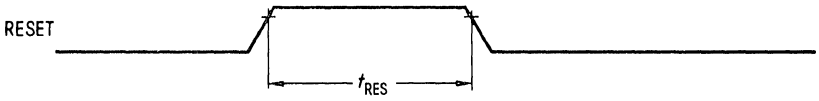
Trigger Pulse for Timer 5 (Cascaded Event Counter/Timer 3 and 5)



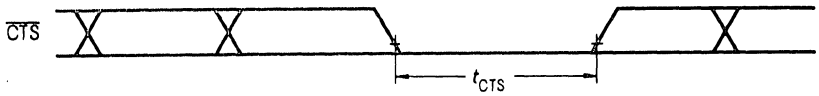
Reading event counters/timers



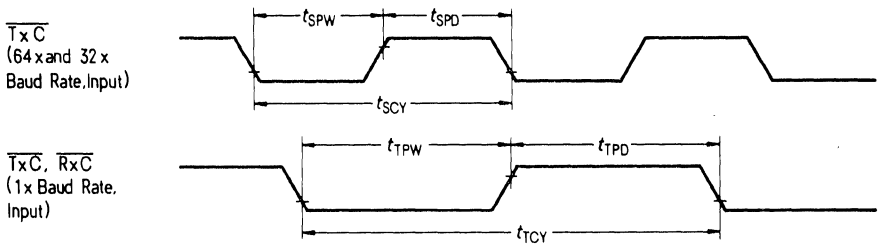
Reset Timing



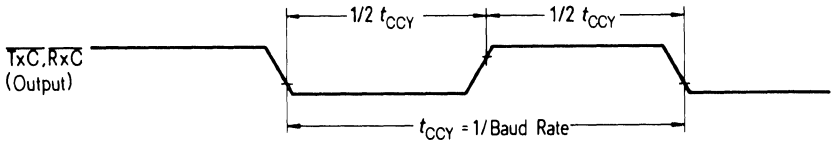
CTS for Single Character Transmission



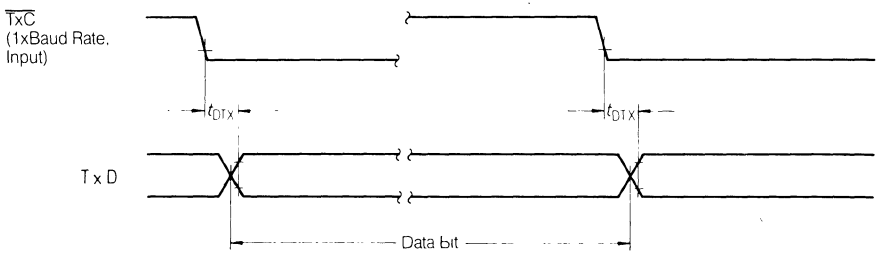
External Baud Rate Clock for Serial Interface



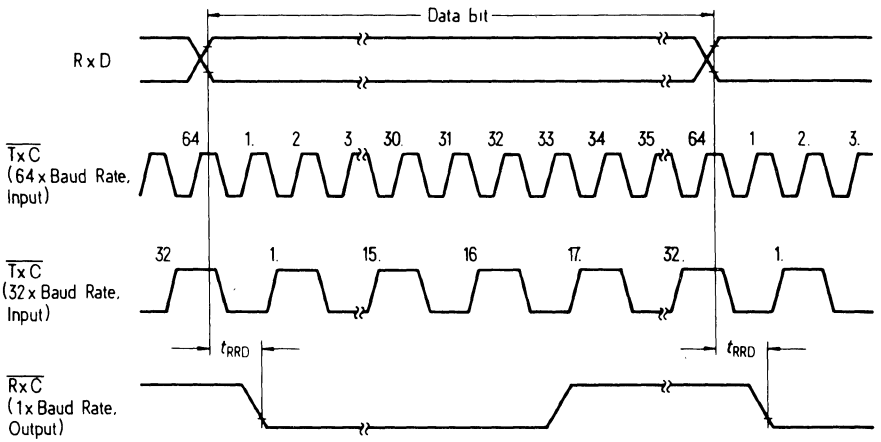
Transmitter and Receiver Clock from Internal Clock Source



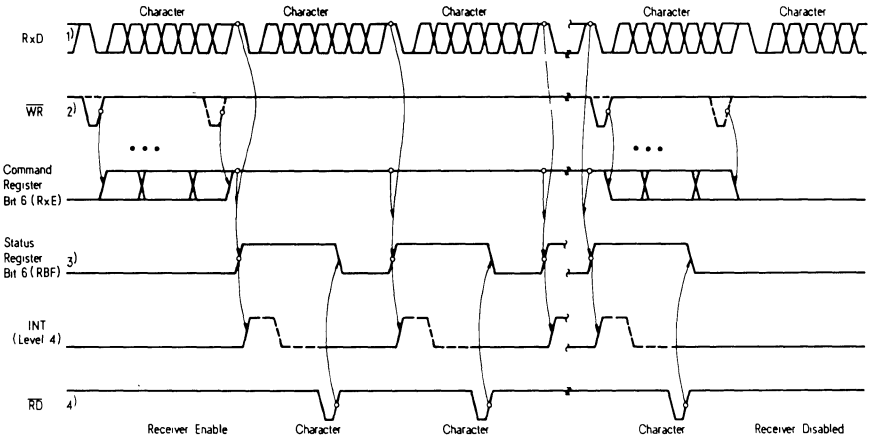
Data Bit Output on Serial Interface



Data Bit Input on Serial Interface



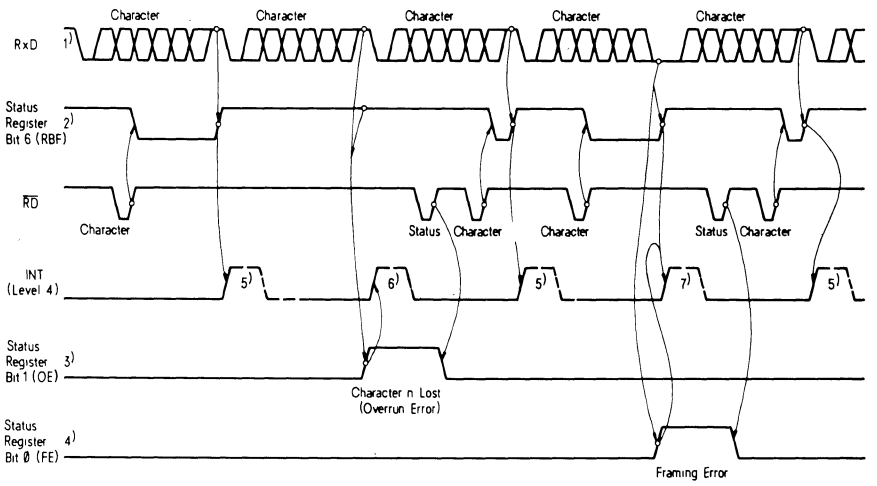
Continuous Reception of Characters on Serial Interface without error conditions



1) Character format for this example: 6 Data bits with Parity bit and one Stop bit.
2) Set or Reset bit 6 of Command Register 3 (Enable Receiver)
3) Receiver Buffer Loaded
4) Read Receiver Buffer Register
5) Receiver is active even though no data is sent or Status bit set.

No Status bits are altered when $\overline{RD}$ is active.

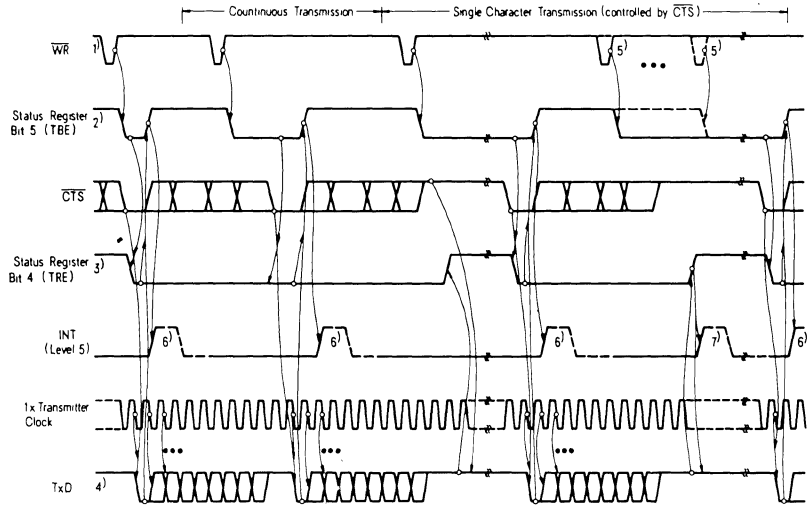
Error Conditions during Reception of Characters on the Serial Interface



1) Character format for this example: 6 Data bits without Parity and one Stop bit
2) Receiver Buffer Register Loaded
3) Overrun error
4) Framing error
5) Interrupt from receiver buffer register loading
6) Interrupt from Overrun error
7) Interrupt from framing error and loading receiver buffer register

No Status bits are altered when $\overline{RD}$ is active.

Transmission of Characters on Serial Interface



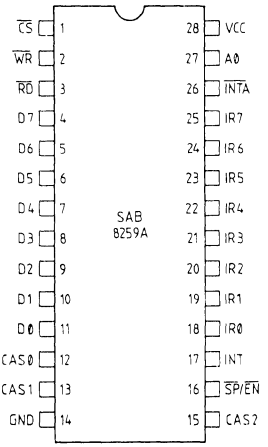
1) Load Transmitter buffer register
2) Transmitter buffer register is empty
3) Transmitter register is empty
4) Character format for this example: 7 Data bits with Parity bit and 2 Stop bits
5) Loading of transmitter buffer register must be completed before $\overline{CTS}$ goes low
6) Interrupt due to transmitter buffer register empty
7) Interrupt due to transmitter register empty

No Status bits are altered when $\overline{RD}$ is active.

SAB 8259A, SAB 8259A-2, SAB 8259A-8 Programmable Interrupt Controller

- SAB 8086 and SAB 8080/85 Family Compatible
- Eight-Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Single +5 V Supply (No Clocks)
- 28-Pin Dual-In-Line Package

Pin Configuration



Pin Names

D7-D0	Data Bus (Bi-Directional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS2-CAS0	Cascade Lines
$\overline{SP}/\overline{EN}$	Slave Program/Enable Buffer
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0-IR7	Interrupt Request Inputs

SAB 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5 V supply. Circuitry is static, requiring no clock input.

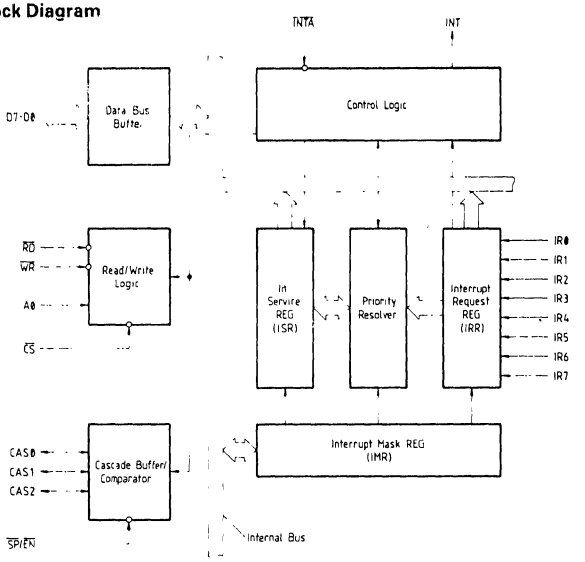
The SAB 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

SAB 8259A is fully upward compatible with SAB 8259. Software originally written for SAB 8259 will operate the SAB 8259A in all SAB 8259 equivalent modes (SAB 8080,85, Non-Buffered, Edge Triggered).

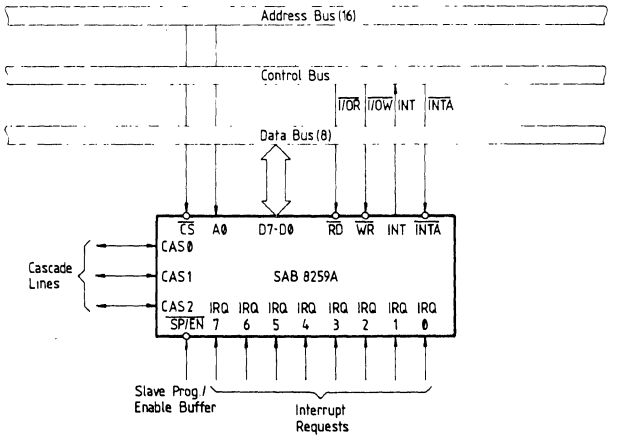
Functional Pin Definition

Symbol	Pin No.	Input (I) Output (O)	Function
$\overline{CS}$	1	I	**Chip Select** A low an this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the SAB 8259A. INTA functions are independent of $\overline{CS}$.
$\overline{WR}$	2	I	**Write** A low on this pin when $\overline{CS}$ is low, enables the SAB 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	**Read** A low on this pin when $\overline{CS}$ is low, enables the SAB 8259A to release status onto the data bus for the CPU.
D7-DØ	4-11	I/O	**Bidirectional Data Bus** Control, status and interrupt vector information is transferred via this bus.
CASØ-CAS1	12, 13, 15	I/O	**Cascade Lines** The CAS lines form a private SAB 8259A bus to control a multiple SAB 8259A structure. These pins are outputs for a master SAB 8259A and inputs for a slave SAB 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	**Slave Program/Enable Buffer** This is dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP=1) or slave (SP=Ø).
INT	17	O	**Interrupt** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IRØ-IR7	18-25	I	**Interrupt Requests** Asynchronous inputs. An interrupt request can be generated by raising an IR input (low to high) and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	**Interrupt Acknowledge** This pin is used to enable SAB 8259A interrupt-vector data onto the data bus. This is done by a sequence of interrupt acknowledge pulses issued by the CPU.
AØ	27	I	**AØ Address Line** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$ and $\overline{RD}$ pins. It is used by the SAB 8259A to decipher between various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU AØ address line (A1 for SAB 8086/SAB 8088)
VCC	28	I	**Power Supply** (+5V)
GND	14	I	**Ground** (0V)

Functional Block Diagram



Interface to Standard System Bus



Functional Description

General

The SAB 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other SAB 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral.
A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the SAB 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

Interrupt Request Register (IRR) and In-Service Register (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service, and the ISR is used to store all the interrupt levels which are being serviced.

Priority Resolver

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

Interrupt Mask Register (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (Interrupt)

This output goes directly to the CPU interrupt input. The VOH level on this line is designed to be fully compatible with the SAB 8080A, SAB 8085A, SAB 8086 and SAB 8088.

$\overline{INTA}$ (Interrupt Acknowledge)

$\overline{INTA}$ pulses will cause the SAB 8259 A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the SAB 8259A.

Data Bus Buffer

This 3-state, bidirectional 8-bit buffer is used to interface the SAB 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

Read/Write Control Logic

The function of this block is to accept Output commands from CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the SAB 8259A to be transferred onto the Data Bus.

$\overline{CS}$ (Chip Select)

A LOW on this input enables the SAB 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (Write)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the SAB 8259A.

$\overline{RD}$ (Read)

A LOW on this input enables the SAB 8259A to send the status of the Interrupt Request Register (IRR), In-Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

A0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

The Cascade Buffer/Comparator

This function block stores and compares the IDs of all SAB 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the SAB 8259A is used as a master and are inputs when the SAB 8259A is used as a slave. As a master, the SAB 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses.

Interrupt Sequence

The powerful features of the SAB 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an SAB 8080/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7-Ø) are raised high, setting the corresponding IRR bit(s).
2. The SAB 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{\text{INTA}}$ pulse.
4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The SAB 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-Ø pins.
5. This CALL instruction will initiate two more $\overline{\text{INTA}}$ pulses to be sent to the SAB 8259A from the CPU group.
6. These two $\overline{\text{INTA}}$ pulses allow the SAB 8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{\text{INTA}}$ pulse and the higher 8-bit address is released at the second $\overline{\text{INTA}}$ pulse.
7. These completes the 3-byte CALL instruction released by the SAB 8259A. In the AEOI mode the ISR bit is reset at the end of the third $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occuring in an SAB 8086/SAB 8088 system are the same until step 4.

4. Upon receiving an $\overline{\text{INTA}}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The SAB 8259A does not drive the Data Bus during this cycle.
5. The SAB 8086/SAB 8088 CPU will initiate a second $\overline{\text{INTA}}$ pulse. During this pulse, the SAB 8259A releases an 8-bit pointer onto the Data Bus where it is ready by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{\text{INTA}}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e. the request was too short in duration) the SAB 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

Absolute Maximum Ratings*)

Ambient Temperature Under Bias	−40 to 85°C
Storage Temperature	−65 to 125°C
Voltage on Any Pin with Respect to Ground	−0.5 to 7 V
Power Dissipation	1 Watt

D.C. Characteristics

T_A=0 to 70°C, V_{CC}=5 V±10%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	–
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5 V		
V_{OL}	Output Low Voltage	–	0.45		I_{OL}=2.2 mA
V_{OH}	Output High Voltage	2.4	–		I_{OH}=−400μA
V_{OH} (INT)	Interrupt Output High Voltage	3.5			I_{OH}=−100μA
		2.4			I_{OH}=−400μA
I_{LI}	Input Load Current	–	10	μA	0V≤V_{IN}≤V_{CC}
I_{LOL}	Output Leakage Current		−10		0.45V≤V_{OUT}≤V_{CC}
I_{CC}	V_{CC} Supply Current		85	mA	–
I_{LIR}	IR Input Load Current		−300	μA	V_{IN}=0V
			10		V_{IN}=V_{CC}

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device

Capacitance

T_A =25°C, V_{CC}=GND=0V

Symbol	Parameter	Limit Values		Unit	Test Conditions
		Min.	Max.		
C_{IN}	Input Capacitance	–	10	μF	f_C=1 MHz
$C_{I/O}$	I/O Capacitance		20		Unmeasured pins returned to V_{SS}

A.C. Characteristics

T_A=0 to 70°C, V_{CC}=5 V±10%

Timing Requirements

Symbol	Parameter	Limit Values						Units	Test Conditions
		SAB8259A-8		SAB8259A		SAB8259A-2			
		Min.	Max.	Min.	Max.	Min.	Max.		
TAHRL	A0/$\overline{CS}$ Setup to $\overline{RD}$/$\overline{INTA}\downarrow$	50		0		0			
TRHAX	A0/$\overline{CS}$ Hold after $\overline{RD}$/$\overline{INTA}\uparrow$	5							
TRLRH	$\overline{RD}$ Pulse Width	420		235		160			
TAHWL	A0/$\overline{CS}$ Setup to $\overline{WR}\downarrow$	50		0		0			–
TWHAX	A0/$\overline{CS}$ Hold after $\overline{WR}\uparrow$	20							
TWLWH	$\overline{WR}$ Pulse Width	400	–	290	–	190	–	ns	
TDVWH	Data Setup to $\overline{WR}\downarrow$	300		240		160			
TWHDX	Data Hold after $\overline{WR}\uparrow$	40		0		0			
TJLJH	Interrupt Request Width (Low)	100		100		100			[1]
TCVIAL	Cascade Setup to Second or Third $\overline{INTA}\downarrow$ (Slave Only)	55		55		40			
TRHRL	End of $\overline{RD}$ to Next Command	160		160		160			–
TWHRL	End of $\overline{WR}$ to Next Command	190		190		190			

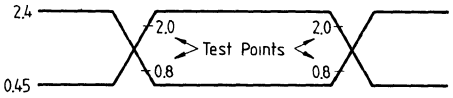
[1] This is the low time required to clear the input latch in the edge triggered mode.

Timing Responses

Symbol	Parameter	Limit Values						Units	Test Conditions
		SAB8259A-8		SAB8259A		SAB8259A-2			
		Min.	Max.	Min.	Max.	Min.	Max.		
TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}\downarrow$	–	300		200		120		C of Data Bus = 100 pF
TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}\uparrow$	10	200		100		85		
TJHIH	Interrupt Output Delay		400		350		300		C of Data Bus Max. test C=100pF Min. test C=15 pF
TIALCV	Cascade Valid from First $\overline{INTA}\downarrow$ (Master Only)		565		565		360		
TRLEL	Enable Active from $\overline{RD}\downarrow$ or $\overline{INTA}\downarrow$		160	–	125	–	100	ns	CINT=100 pF
TRHEH	Enable Inactive from $\overline{RD}\uparrow$ or $\overline{INTA}\uparrow$	–	325		150		150		
TAHDV	Data Valid from Stable Address		350		200		200		CCascade=100 pF
TCVDV	Cascade Valid to Valid Data		300		300				

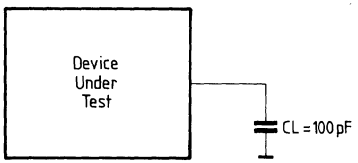
A.C. Testing Input, Output Waveform

Input/Output



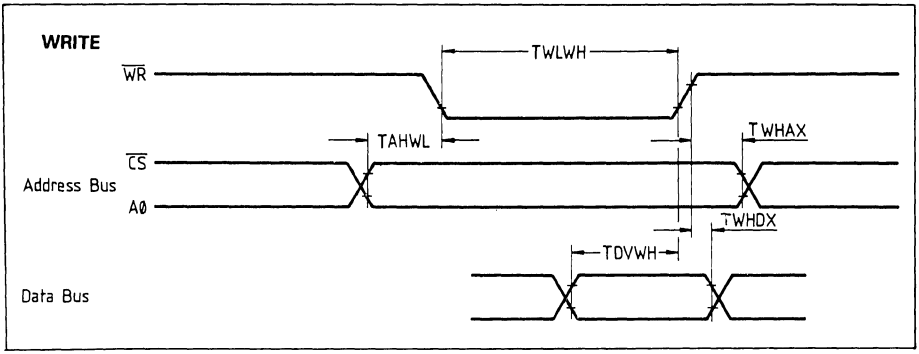
AC testing: inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

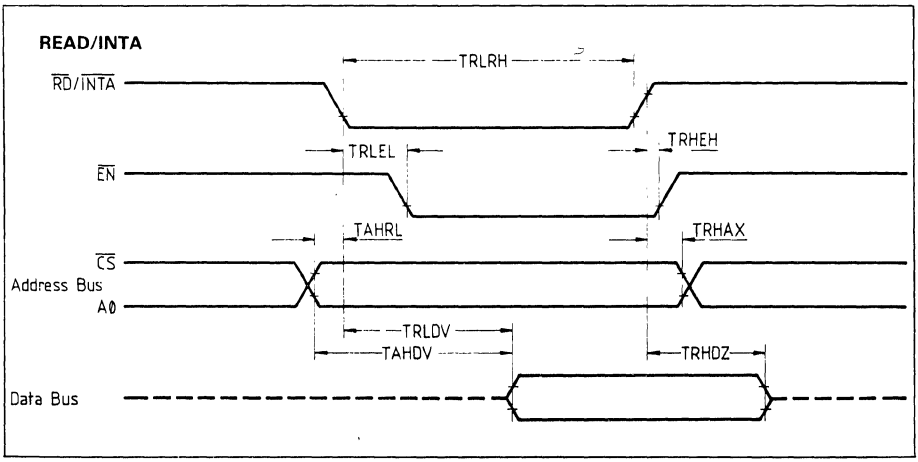
A.C. Testing Load Circuit

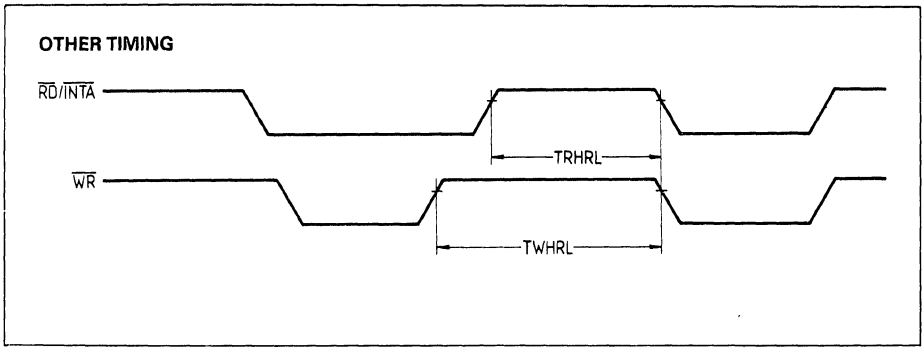


CL = 100 pF
CL includes jig capacitance

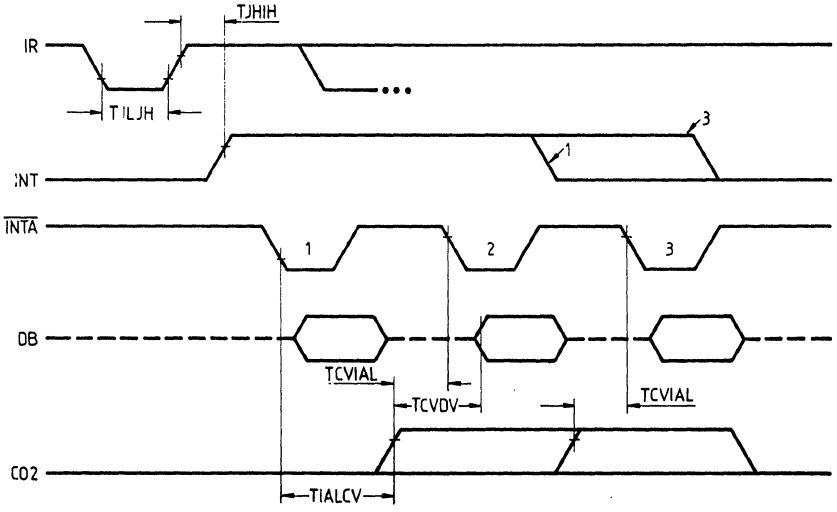
Waveforms


WRITE
WR
TWLWH
TAHWL
TWHAX
CS
Address Bus
A0
TWHDX
TDVWH
Data Bus


READ/INTA
RD/INTA
TRLRH
TRLEL
TRHEH
EN
TAHRL
TRHAX
CS
Address Bus
A0
TRLDV
TAHDV
TRHDZ
Data Bus


OTHER TIMING
RD/INTA
TRHRL
WR
TWHRL

INTA SEQUENCE

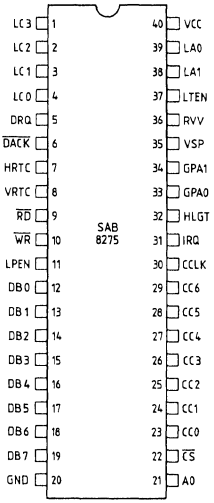


Notes: Interrupt output must remain HIGH at least until leading edge of first INTA.
1. Cycle 1 in SAB 8086/88 systems, the Data Bus is not active.

SAB 8275
Programmable CRT Controller

- Programmable screen and character format
- 6 independent visual field attributes
- 11 visual character attributes (graphics capability)
- Cursor control (4 types)
- Light pen detection and registers
- SAB 8051, SAB 8085, SAB 8086 and SAB 8088 compatible
- Dual row buffers
- Programmable DMA burst mode
- Single +5V supply
- High performance MYMOS technology
- Fully compatible with industry standard 8275

Pin configuration



Pin Names

LC0–LC3	Line Count
DRQ	DMA Request
$\overline{\text{DACK}}$	DMA Acknowledge
HRTC	Horizontal Retrace
VRTC	Vertical Retrace
$\overline{\text{RD}}$	Read Input
$\overline{\text{WR}}$	Write Input
LPEN	Light Pen
DB0–DB7	Bidirectional Three-State Data Bus Lines
LA0, LA1	Line Attribute Codes
LTEN	Light Enable
RVV	Reverse Video
VSP	Video Suppression
GPA0, GPA1	General Purpose Attribute Codes
HLGT	Highlight
IRQ	Interrupt Request
CCLK	Character Clock
CC0–CC6	Character Codes
$\overline{\text{CS}}$	Chip Select
A0	Port Address

The SAB 8275 programmable CRT controller is a single chip device to interface CRT raster scan displays. It is manufactured in Siemens advanced MYMOS technology. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the SAB 8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

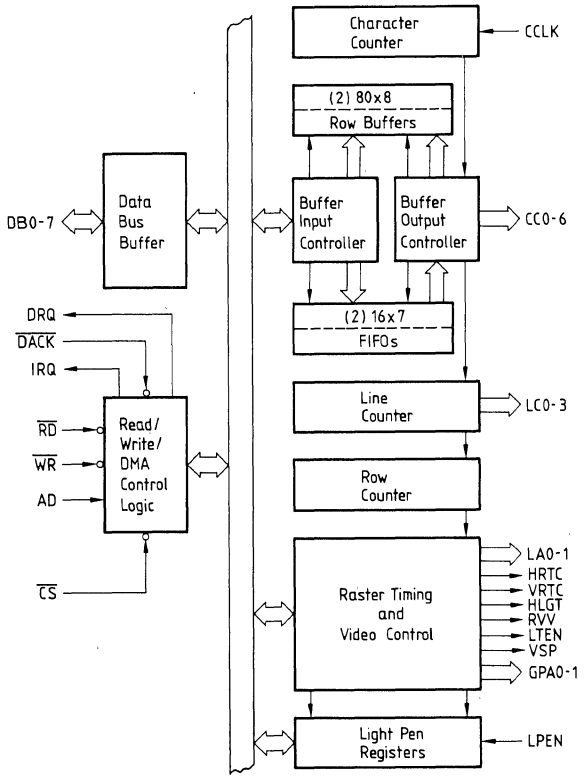
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
LC3 LC2 LC1 LC0	1 2 3 4	O	LINE COUNT: Output from the line counter which is used to address the character generator for the line positions on the screen.
DRQ	5	O	DMA REQUEST: Output signal to the SAB 8237A DMA controller requesting a DMA cycle.
$\overline{\text{DACK}}$	6	I	DMA ACKNOWLEDGE: Input signal from the SAB 8237A DMA controller acknowledging that the requested DMA cycle has been granted.
HRTC	7	O	HORIZONTAL RETRACE: Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
VRTC	8	O	VERTICAL RETRACE: Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
$\overline{\text{RD}}$	9	I	READ INPUT: A control signal to read registers.
$\overline{\text{WR}}$	10	I	WRITE INPUT: A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
LPEN	11	I	LIGHT PEN: Input signal from the CRT system signifying that a light pen signal has been detected.
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	12 13 14 15 16 17 18 19	I/O	BIDIRECTIONAL THREE-STATE DATA BUS LINES: The outputs are enable during a read of the C or P ports.
LA0 LA1	39 38	O	LINE ATTRIBUTE CODES: These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes.
LTEN	37	O	LIGHT ENABLE: Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
RVV	36	O	REVERSE VIDEO: Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
VSP	35	O	VIDEO SUPPRESSION: Output signal used to blank the video signal to the CRT. This output is active: – During the horizontal and vertical retrace intervals. – at the top and bottom lines of rows if underline is programmed to be number 8 or greater. – when an end of row or end of screen code is detected. – when a DMA underrun occurs. – at regular intervals (1/16 frames frequency for cursor, 1/32 frame frequency for character and field attributes) – to create blinking displays as specified by cursor, character attribute, or field attribute programming.
GPA1, GPA0	34 33	O	GENERAL-PURPOSE ATTRIBUTE CODES: Outputs which are enable by the general purpose field attribute codes.
HLGT	32	O	HIGHLIGHT: Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.
$\overline{IRQ}$	31	O	INTERRUPT REQUEST.
CCLK	30	I	CHARACTER CLOCK (from dot/timing logic).
CC6 CC5 CC4 CC3 CC2 CC1 CC0	29 28 27 26 25 24 23	O	CHARACTER CODES: Output from the row buffers used for character selection in the character generator.
$\overline{CS}$	22	I	CHIP SELECT: The read and write are enabled by $\overline{CS}$.
A0	21	I	PORT ADDRESS: A high input on A0 selects the "C" port or command registers and a low input selects the "P" port or parameter registers.
VCC	40	–	+5V Power supply.
GND	20	–	Ground (0V)

SAB 8275 Block diagram showing counter and register functions



Functional Description

Data bus buffer

This three-state, bidirectional, 8-bit buffer is used to interface the SAB 8275 to the system data bus.

This functional block accepts inputs from the system control bus and generates control signals for overall device operation. It contains the command, parameter, and status registers that store various control formats for the device functional definition.

A0	Operation	Register
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	1	0	0	Write SAB 8275 parameter
0	0	1	0	Read SAB 8275 parameter
1	1	0	0	Write SAB 8275 command
1	0	1	0	Read SAB 8275 status
X	1	1	0	Three-state
X	X	X	1	Three-state

$\overline{RD}$ (Read)

A "low" on this input informs the SAB 8275 that the CPU is reading data or status information from the SAB 8275.

$\overline{WR}$ (Write)

A "low" on this input informs the SAB 8275 that the CPU is writing data or control words to the SAB 8275.

$\overline{CS}$ (Chip select)

A "low" on this input selects the SAB 8275. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the data bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.

DRQ (DMA request)

A "high" on this output informs the DMA controller that the SAB 8275 desires a DMA transfer.

$\overline{DACK}$ (DMA acknowledge)

A "low" on this input informs the SAB 8275 that a DMA cycle is in progress.

IRQ (Interrupt request)

A "high" on this output informs the CPU that the SAB 8275 desires interrupt service.

Character counter

The character counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (character clock) input, which should be a derivative of the external dot clock.

Line counter

The line counter is a programmable counter that is used to determine the number of horizontal lines (sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row counter

The row counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Light pen registers

The light pen registers are two registers that store the contents of the character counter and the row counter whenever there is a rising edge on the LPEN (Light Pen) input.

Note: Software correction is required.

Raster timing and video controls

The raster timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The video control circuitry controls the generation of LA0–1 (line attribute), HGLT (highlight), RVV (reverse video), LTEN (Light enable), VSP (video suppress), and GPA0–1 (general purpose attribute) outputs.

Row buffers

The row buffers are two 80 character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

FIFOs

There are two 16 character FIFOs in the 8275. They are used to provide extra row buffer length in the transparent attribute mode.

Buffer input/output controllers

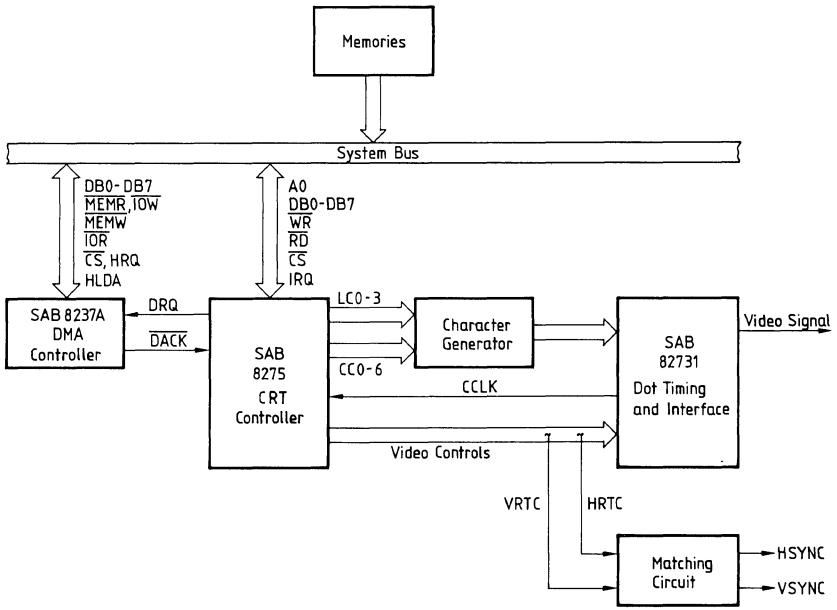
The buffer input/output controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action (Examples: An "end of screen-stop DMA" special code will cause the buffer input controller to stop further DMA requests. A "highlight" field attribute will cause the buffer output controller to activate the HGLT output).

System Operation

The SAB 8275 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with the SAB 8237A DMA controller and standard character generator ROMs for dot matrix decoding. Dot level timing must be provided by external circuitry.

SAB 8275 Block diagram showing systems operation



Raster timing

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace (programmable from 2 to 32). This is constantly repeated.

The line counter is driven by the character counter. It is used to generate the line address outputs (LC0–3) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

The video suppression output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT display.

DMA timing

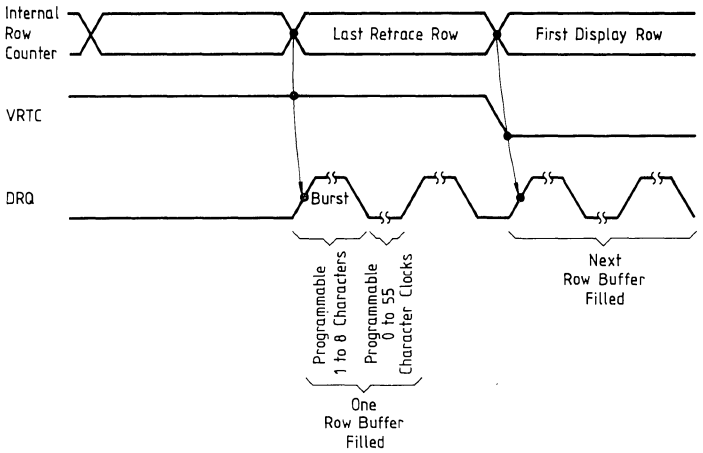
The SAB 8275 can be programmed to request burst DMA transfers of 1 to 8 characters. The interval between bursts is also programmable (from 0 to 55 character clock periods ±1). This allows the user to tailor his DMA overhead to fit his system needs.

The first DMA request of the frame occurs one *row time* before the end of vertical retrace. DMA requests continue as programmed, until the row buffer is filled. If the row buffer is filled in the middle of a burst, the SAB 8275 terminates the burst and resets the burst counter. No more DMA requests will occur until the *beginning* of the *next* row. At that time, DMA requests are activated as programmed until the other buffer is filled.

The DMA request for a row will start at the first character clock of the preceding row. If the burst mode is used, the first DMA request may occur a number of character clocks later. This number is equal to the programmed burst space.

If, for any reason, there is a DMA underrun, a flag in the status word will be set.

DMA timing

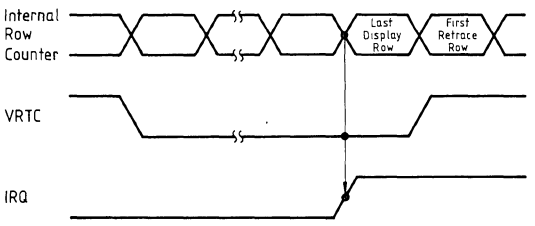


The DMA controller is typically initialized for the next frame at the end of the current frame.

Interrupt timing

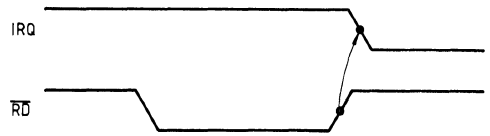
The SAB 8275 can be programmed to generate an interrupt request at the end of each frame. This can be used to reinitialize the DMA controller. If the SAB 8275 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row*.

Beginning of interrupt request



IRQ will go inactive after the status register is read.

End of interrupt request



A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Another method of reinitializing the DMA controller is to have the DMA controller itself interrupt on terminal count. With this method, the SAB 8275 interrupt enable flag should not be set.

Note: Upon power-up, the SAB 8275 interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the SAB 8275 before system interrupts are enabled.

General systems operational description

The SAB 8275 provides a "window" into the microcomputer system memory.

Display characters are retrieved from memory and displayed on a row by row basis. The SAB 8275 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (see programming section.)

The SAB 8275 requests DMA to fill the row buffer that is not being used for display. DMA burst length and spacing is programmable. (See programming section.)

The SAB 8275 displays character rows one line at a time.

The number of lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See programming section.)

The SAB 8275 provides special control codes which can be used to minimize DMA or software overhead. It also provides visual attribute codes to cause special action or symbols on the screen without the use of the character generator (see visual attribute section).

The SAB 8275 also controls raster timing. This is done by generating horizontal retrace (HRTC) and vertical retrace (VRTC) signals. The timing of these signals is programmable.

The SAB 8275 can generate a cursor. Cursor location and format are programmable. (See programming section.)

The SAB 8275 has a light pen input and registers. The light pen input is used to load the registers. Light pen registers can be read on command. (See programming section.)

Display row buffering

Before the start of a frame, the SAB 8275 requests DMA and one row buffer is filled with characters.

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, DMA begins filling the other row buffer with the next row of characters.

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

This is repeated until all of the character rows are displayed.

Screen format

The SAB 8275 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

The SAB 8275 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. DMA is not requested for the blanked rows.

Row format

The SAB 8275 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the whole character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*.

Note: In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by line counter.

Mode 0 is use ful for character generators that leave address zero blank and start at address 1, Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

If the line *number* underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (light enable) signal.

Dot format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

Note: Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

Visual Attributes and Special Codes

The characters processed by the SAB 8275 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The most significant bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

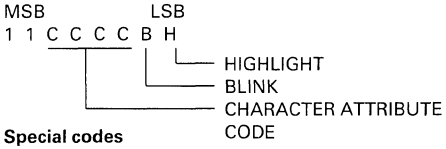
There are two types of visual attribute codes. They are character attributes and field attributes.

Character attribute codes

Character attribute codes are codes that can be used to generate graphics symbols without the use of a character generator. This is accomplished by selectively activating the line attribute outputs (LA0–1), the video suppression output (VSP), and the light enable output. The dot level timing circuitry can use these signals to generate the proper symbols.

Character attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the video suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the highlight output (HGLT).

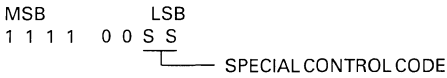
Character attributes



Special codes

Four special codes are available to help reduce memory, software or DMA overhead.

Special control character



S S	Function
0 0	End of Row
0 1	End of Row-stop DMA
1 0	End of Screen
1 1	End of Screen-stop DMA

The End-of-Row code (00) activates VSP and holds it to the end of the line.

The End-of-Row-Stop DMA code (01) causes the DMA control logic to stop DMA for the rest of the row when it is written into the row buffer. It affects the display in the same way as the end-of-row code (00).

The end-of-screen code (10) activates VSP and holds it to the end of the frame.

The end-of-screen-stop DMA code (11) causes the DMA control logic to stop DMA for the rest of the frame when it is written into the row buffer. It affects the display in the same way as the end-of-screen code (10).

If the stop DMA feature is not used, all characters after an end-of-row character are ignored, except for the end-of-screen character, which operates normally. All characters after an end-of-screen character are ignored.

Note: If a stop DMA character is not the last character in a burst or row, DMA is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the stop DMA character.

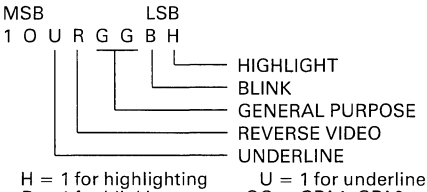
Field attributes

The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

There are six field attributes:

1. *Blink* – Characters following the code are caused to blink by activating the Video Suppression Output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* – Characters following the code are caused to be highlighted by activating the Highlight Output (HGLT).
3. *Reverse Video* – Characters following the code are caused to appear with reverse video by activating the Reverse Video Output (RVV).
4. *Underline* – Characters following the code are caused to be underlined by activating the Light Enable Output (LTEN).
5, 6. *General Purpose* – There are two additional SAB 8275 outputs which act as general purpose, independently programmable field attributes. GPA0–1 are active high outputs.

Field attribute code



* More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

The SAB 8275 can be programmed to provide visible or invisible field attribute characters.

If the SAB 8275 is programmed in the visible field attribute mode, all field attributes will occupy a position on the screen. They will appear as blanks caused by activation of the video suppression output (VSP). The chosen visual attributes are activated after this blanked character.

If the SAB 8275 is programmed in the invisible field attribute mode, the SAB 8275 FIFO is activated.

Each row buffer has a corresponding FIFO. These FIFOs are 16 characters by 7 bits in size.

When a field attribute is placed in the row buffer during DMA, the buffer input controller recognizes it and places the next character in the proper FIFO.

When a field attribute is placed in the buffer output controller during display, it causes the controller to immediately put a character from the FIFO on the character code outputs (CC0–8). The chosen visual attributes are also activated.

Since the FIFO in 16 characters long, no more then 16 field attribute characters may be used per line in this mode. If more are used, a bit in the status word is set and the first characters in the FIFO are written over and lost.

Note: Since the FIFO is 7 bits wide, the MSB of any characters put in it are stripped off. Therefore, a visual attribute or special code must *not* immediately follow a field attribute code. If this situation does occur, the visual attribute or special code will be treated as normal display character.

Field and character attribute interaction

Character attribute symbols are affected by the reverse video (RVV) and general purpose (GPA0–1) field attributes. They are not affected by underline, blink or highlight field attribute; however, these characteristics can be programmed *individually* for character attribute symbols.

Cursor timing

The cursor location is determined by a cursor row register and a character position register which are located by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Light pen detection

A light pen consists of a micro switch and a tiny light sensor. When the light pen is pressed against the CRT screen, the micro switch enable the light sensor. When the raster sweep reaches the light sensor, it triggers the light pen output.

If the output of the light pen is presented to the SAB 8275 LPEN input, the row and character position coordinates are stored in a pair of registers. These registers can be read on command. A bit in the status word is set, indicating that the light pen signal was detected. The LPEN input must be a 0 to 1 transition for proper operation.

Note: Due to internal and external delays, the character position coordinate will be off by at least three character positions. This has to be corrected in software.

Device programming

The SAB 8275 has two programming registers, the command register (CREG) and the parameter register (PREG). It also has a status register (SREG). The command register can only be written into and the Status registers can only be read from. They are addressed as follows:

A_0	operation	register
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

The SAB 8275 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

Instruction Set

The SAB 8275 instruction set consists of 8 commands

Command	No. of parameter bytes
Reset	4
Start Display	0
Stop Display	0
Read Light Pen	2
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

In addition, the status of the SAB 8275 (SREG) can be read by the CPU at any time.

1 Reset command

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Reset command	0 0 0 0 0 0 0 0
Parameters	Write	0	Screen Comp Byte 1	S H H H H H H H
	Write	0	Screen comp Byte 2	V V R R R R R R
	Write	0	Screen comp Byte 3	U U U U L L L L
	Write	0	Screen comp Byte 4	M F C C Z Z Z Z

Action – After the reset command is written, DMA requests stop, SAB 8275 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter – S Spaced rows

S	Functions
0	Normal rows
1	Spaced Rows

Parameter – HHHHHHH Horizontal characters/row

H H H H H H H	No. of characters per row
0 0 0 0 0 0 0	1
0 0 0 0 0 0 1	2
0 0 0 0 0 1 0	3
. . .	.
. . .	.
1 0 0 1 1 1 1	80
1 0 1 0 0 0 0	Undefined
. . .	.
. . .	.
1 1 1 1 1 1 1	Undefined

Parameter – VV Vertical retrace row count

V V	No. of row counts per VRTC
0 0	1
0 1	2
1 0	3
1 1	4

Parameter – RRRRRR Vertical rows/frame

R R R R R R	No. of rows/frame
0 0 0 0 0 0	1
0 0 0 0 0 1	2
0 0 0 0 1 0	3
. . .	.
. . .	.
1 1 1 1 1 1	64

Parameter – UUUU Underline placement

U U U U	Line number of underline
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
. . .	.
. . .	.
1 1 1 1	16

Note: uuuu MSB determines blanking of top and botton lines (1 = blanked, 0 = not blanked).

Parameter – LLLL Number of lines per character row

L	L	L	L	No. of lines/row
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter – ZZZZ Horizontal retrace count

Z	Z	Z	Z	No. of character counts per HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

Parameter – M Line Counter Mode

M	Line counter mode
0	Mode 0 (non-offset)
1	Mode 1 (offset by 1 count)

Parameter – F Field attribute mode

F	Field attribute mode
0	Transparent
1	Non-transparent

Parameter – CC Cursor format

C	C	Cursor format
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Nonblinking reverse video block
1	1	Nonblinking underling

2 Start display command

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Start display	0 0 1 S S S B B
No parameters				

SSS Burst space code

S S S	No. of character clocks between DMA requests
0 0 0	0
0 0 1	7
0 1 0	15
0 1 1	23
1 0 0	31
1 0 1	39
1 1 0	47
1 1 1	55

BB Burst count code

B B	No. of DMA cycles per burst
0 0	1
0 1	2
1 0	4
1 1	8

Action – SAB 8275 interrupts are enabled, DMA requests begin, video is enabled, interrupt enable and video enable status flags are set.

3 Stop display command

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Stop display	0 1 0 0 0 0 0 0
No parameters				

Action – Disables video, interrupts remain enabled. HRTC and VRTC continue to run, video enable status flag is reset, and the "Start display" command must be given to re-enable the display.

4 Read light pen command

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	read light pen	0 1 1 0 0 0 0 0
Parameters	Read	0	Char. number	(Char. position in row)
	Read	0	Row number	(Row number)

Action – The SAB 8275 is conditioned to supply the contents of the light pen position registers in the next two read cycles of the parameter register. Status flags are not affected.

Note: Software correction of light pen position is required.

5 Load cursor position

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Load cursor	1 0 0 0 0 0 0 0
Parameters	Write	0	Char. number	(Char. position in row)
	Write	0	Row number	(Row number)

Action – The SAB 8275 is conditioned to place, the next two parameter bytes into the cursor position registers. Status flags not affected.

6 Enable interrupt command

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Enable interrupt	1 0 1 0 0 0 0 0
No parameters				

Action – The interrupt enable status flag is set and interrupts are enabled.

7 Disable interrupt command

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Disable interrupt	1 1 0 0 0 0 0 0
No parameters				

Action – Interrupts are disabled and the interrupt enable status flag is reset.

8 Preset counters command

	Operation	A0	Description	Data bus MSB LSB
Command	Write	1	Preset counters	1 1 1 0 0 0 0 0
No parameters				

Action – The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU. After this command, two additional clock cycles are required before the first character of the first row is put out.

Status flags

	Operation	A0	Description	Data bus MSB LSB
Command	Read	1	Status word	0 IE IR LP IC VE DU F0

IE – (Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command reset with the "Reset" command.

IR – (Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

LP – This flag is set when the light pen input (LPEN) is activated and the light pen registers have been loaded. This flag is automatically reset after a status read.

IC – (Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE – (Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

DU – (DMA Underrun) This flag is set whenever a data underrun occurs during DMA transfers. Upon detection of DU, the DMA operation is stopped and the screen is blanked until after the vertical retrace interval. This flag is reset after a status read.

FO – (FIFO Overrun) This flag is set whenever the FIFO is overrun. It is reset on a status read.

Absolute Maximum Ratings [1]

Temperature under bias	0 to +70 °C
Storage temperature	−65 to +150 °C
All output ans supply and supply voltages	−0,5 to +7 V
All input voltages	−0,5 to +5,5 V
Power dissipation	1,0 W

DC Characteristics

(TA = 0°C to 70°C, VCC = 5 V ±5%)

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
VIL	Input low voltage	−0.5	0.8	V	–
VIH	Input high voltage	2.0	VCC+0.5V		
VOL	Output low voltage	–	0.45		IOL = 2.2 mA
VOH	Output high voltage	2.4	–		IOH = −400 µA
IIL	Input load current	–	±10	µA	VIN = VCC to 0 V
IOFL	Output float leakage				VOUT = VCC to 0.45 V
ICC	VCC supply current		160	mA	–

Capacitance

(TA = 25°C, VCC = GND = 0 V)

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
CIN	Input capacitance	–	10	pF	fc = 1 MHz
CI/O	I/O capacitance		20		Unmeasured pins returned to GND

1) Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics (SAB 8275)

(TA = 0C to 70°C, VCC = 5.0V ± 5%, GND = 0V)

Clock timing

Symbol	Parameter	Limit values		Units	Test condition
		Min.	Max.		
TCLK	Clock period	480			
TKH	Clock high	240	–		
TKL	Clock low	160		ns	–
TKR	Clock rise	5	30		
TKF	Clock fall				

Bus parameters
Read cycle

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TAR	Address stable before READ	0			
TRA	Address hold time for READ		–		–
TRR	READ pulse width	250		ns	
TRD	Data delay from READ	–	200		CL = 150 pF
TDF	READ to data floating		100		

Write cycle

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TAW	Address stable before WRITE	0			
TWA	Address hold time for WRITE				
TWW	WRITE pulse width	250	–	ns	–
TDW	Data seting time for WRITE	150			
TWD	Data hold time for WRITE	0			

Other timings

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TCC	Character code output delay	–	150	ns	CL = 50 pF
THR	Horizontal retrace output delay		200		
TLC	Line count output delay		400		
TAT	Control-attribute output delay		275		
TVR	Vertical retrace output delay				
TRI	IRQ↓ from RD↑		250		
TWQ	DRQ↑ from WR↑				
TRQ	DRQ↓ from WR↓		200		
TLR	DACK↓ to WR↓	0	–		–
TRL	WR↑ to DACK↑				
TPR	LPEN rise	–	50		
TPH	LPEN hold	100	–		

AC Characteristics (SAB 8275-2)

(TA = 0 C to 70°C, VCC = 5.0 V ± 5%, GND = 0 V)

Clock timing

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TCLK	Clock period	320	–	ns	–
TKH	Clock high	120			
TKL	Clock low				
TKR	Clock rise	5	30		
TKF	Clock fall				

Bus parameters
Read cycle

Symbol	Parameter	Limit value		Unit	Test condition
		Min.	Max.		
TAR	Address stable before READ	0	–	ns	–
TRA	Address hold time for READ				
TRR	READ pulse width	250			
TRD	Data delay from READ	–	200		CL = 150 pF
TDF	READ to data floating		100		CL = 150 pF

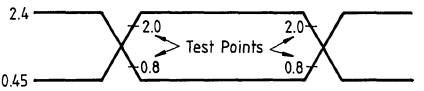
Write cycle

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TAW	Address stable before WRITE	0	–	ns	–
TWA	Address hold time for WRITE				
TWW	WRITE pulse width	250			
TDW	Data seting time for WRITE	150			
TWD	Data hold time for WRITE	0			

Other timings

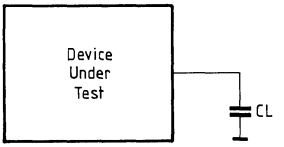
Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TCC	Character code output delay	–	150	ns	CL = 50 pF
THR	Horizontal retrace output delay				
TLC	Line count output delay		250		
TAT	Control-attribute output delay				
TVR	Vertical retrace output delay				
TRI	IRQ↓ from RD↑				
TWQ	DRQ↑ from WR↑				
TRQ	DRQ↓ from WR↓		200		
TLR	DACK↓ to WR↓	0	–		–
TRL	WR↑ to DACK↑				
TPR	LPEN rise	–	50		
TPH	LPEN hold	100	–		

A.C. Testing input/output



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

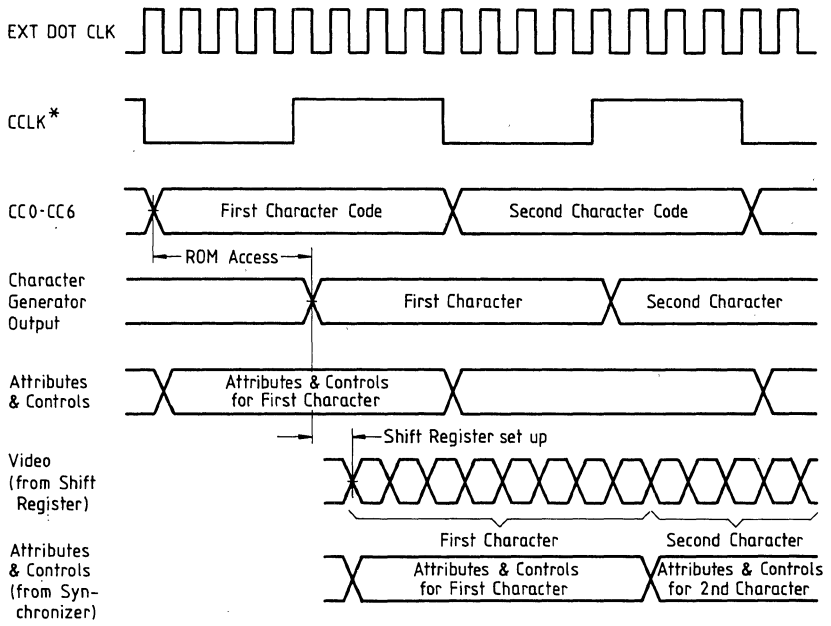
A.C. Testing load circuit



CL Includes Jig Capacitance

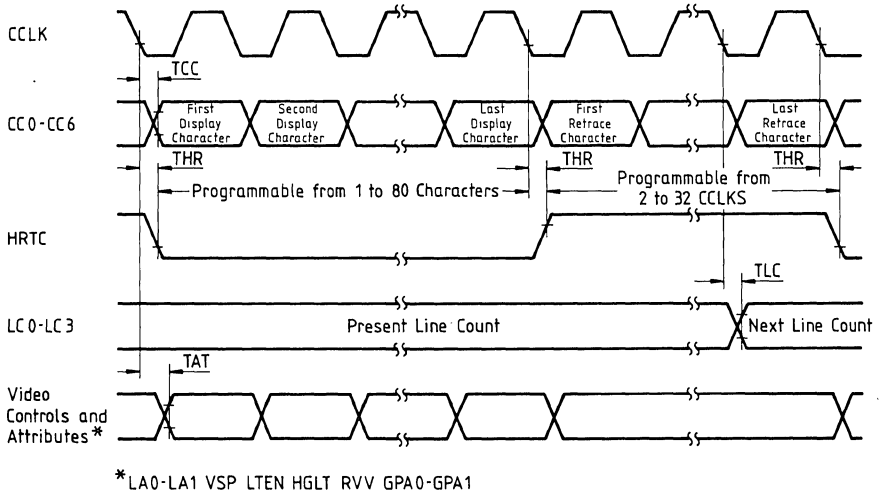
Waveforms

Typical dot level timing



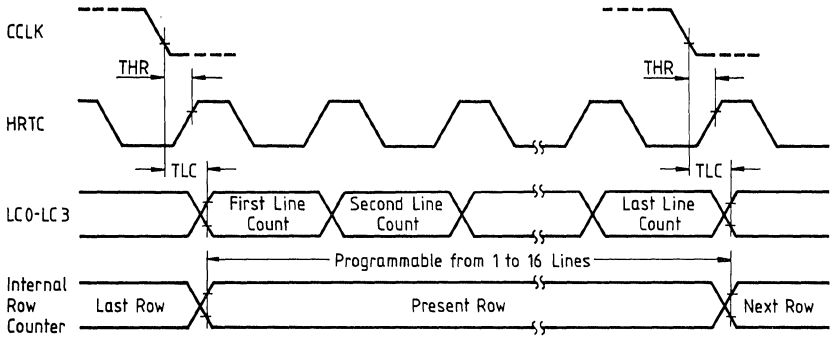
*CCLK is a Multiple of the Dot Clock and an Input to the SAB 8275

Line timing

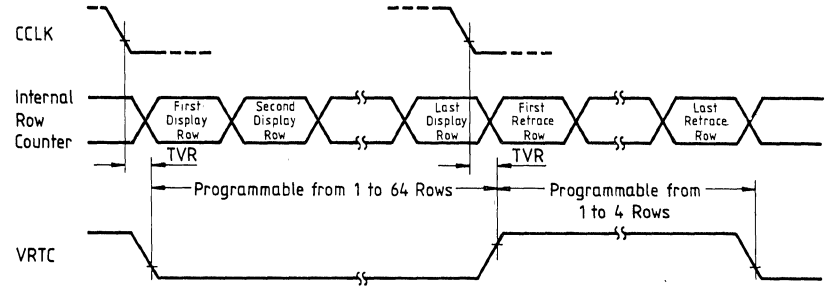


*LA0-LA1 VSP LTEN HGLT RVV GPA0-GPA1

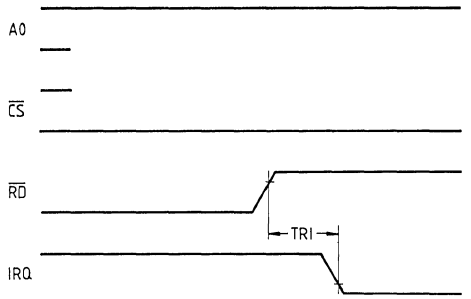
Row timing



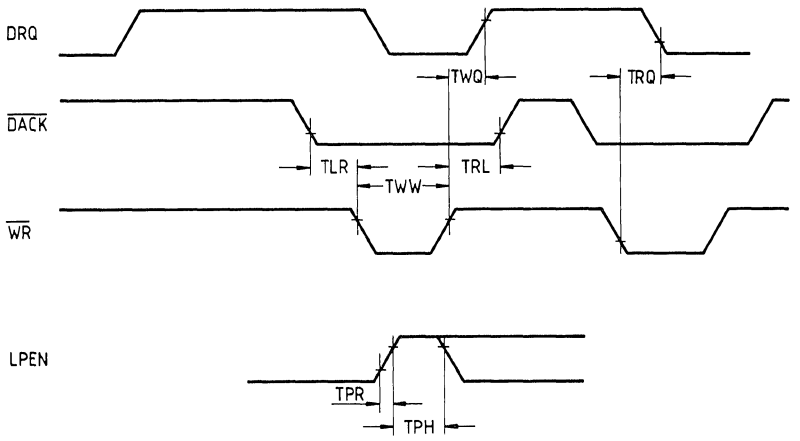
Frame timing



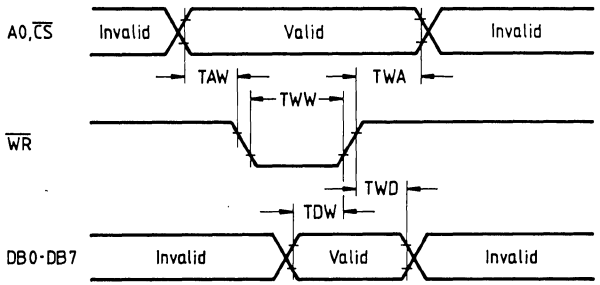
Interrupt timing



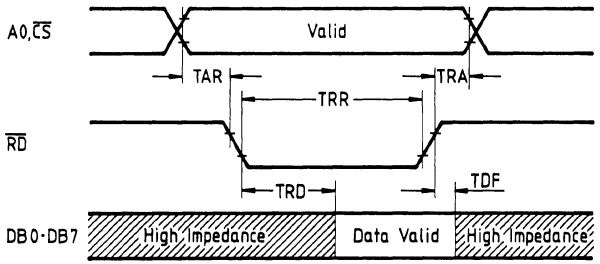
DMA timing



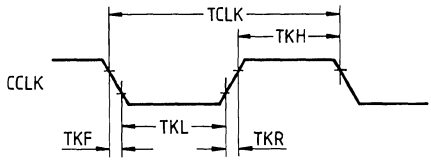
Write timing



Read timing



Clock timing

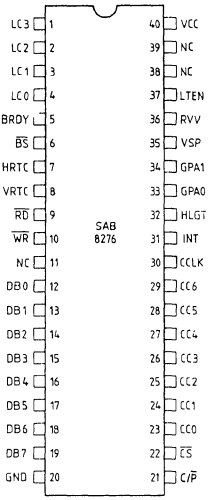


Preliminary

SAB 8276
Small System CRT Controller

- Programmable screen and character format
- 6 independent visual attributes
- Cursor control (4 types)
- SAB 8051, SAB 8085, SAB 8086 and SAB 8088 compatible
- Dual row buffers
- Programmable DMA burst mode
- Single +5V supply
- High performance MYMOS technology
- Fully compatible with industry standard 8276

Pin configuration



Pin Names

LC0–LC3	Line Count
BRDY	Buffer Ready
$\overline{BS}$	Buffer Select
HRTC	Horizontal Retrace
VRTC	Vertical Retrace
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
DB0–DB7	Bidirectional Three-State Data Bus Lines
LTEN	Light Enable
RVV	Reverse Video
VSP	Video Suppression
GPA0, GPA1	General Purpose Attribute Codes
HLGT	Highlight
INT	Interrupt Output
CCLK	Character Clock
CC0–CC6	Character Codes
$\overline{CS}$	Chip Select
C/$\overline{P}$	Port Address

The SAB 8276 Small System CRT Controller is a single chip device to interface CRT raster scan displays. It is manufactured in Siemens advanced MYMOS technology. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the SAB 8276 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

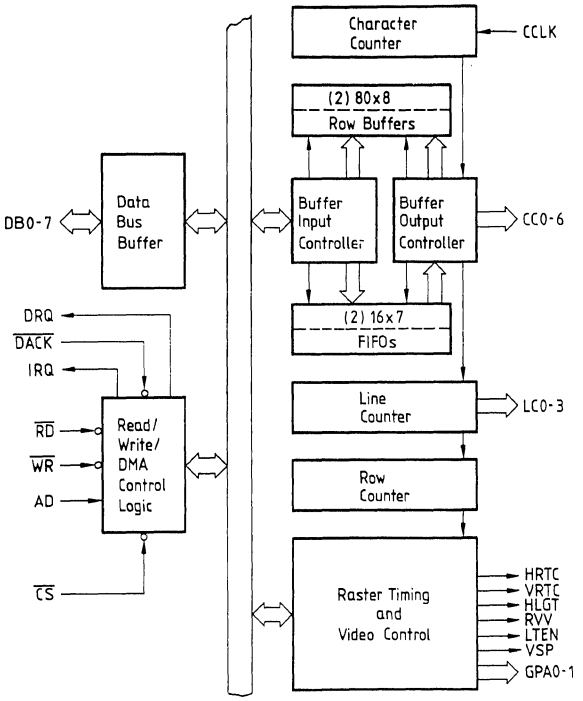
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
LC3 LC2 LC1 LC0	1 2 3 4	O	LINE COUNT: Output from the line counter which is used to address the character generator for the line positions on the screen.
BRDY	5	I	BUFFER READY: Output signal indicating that a row buffer is ready for loading of character data.
$\overline{BS}$	6	O	BUFFER SELECT: Input signal enabling $\overline{WR}$ for character data into the row buffers.
HRTC	7	O	HORIZONTAL RETRACE: Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
VRTC	8	O	VERTICAL RETRACE: Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
$\overline{RD}$	9	I	READ INPUT: A control signal to read registers.
$\overline{WR}$	10	I	WRITE INPUT: A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
NC	11		No Connection
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	12 13 14 15 16 17 18 19	I/O	BIDIRECTIONAL THREE-STATE DATA BUS LINES: The outputs are enable during a read of the C or P ports.
NC	38/39		No Connection
LTEN	37	O	LIGHT ENABLE: Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
RVV	36	O	REVERSE VIDEO: Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
VSP	35	O	VIDEO SUPPRESSION: Output signal used to blank the video signal to the CRT. This output is active: – During the horizontal and vertical retrace intervals. – at the top and bottom lines of rows if underline is programmed to be number 8 or greater. – when an end of row or end of screen code is detected. – when a DMA underrun occurs. – at regular intervals (1/16 frames frequency for cursor, 1/32 frame frequency for character and field attributes) – to create blinking displays as specified by cursor or field attribute programming.
GPA1 GPA0	34 33	O	GENERAL-PURPOSE ATTRIBUTE CODES: Outputs which are enable by the general purpose field attribute codes.
HLGT	32	O	HIGHLIGHT: Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.
INT	31	O	INTERRUPT OUTPUT
CCLK	30	I	CHARACTER CLOCK (from dot/timing logic).
CC6 CC5 CC4 CC3 CC2 CC1 CC0	29 28 27 26 25 24 23	O	CHARACTER CODES: Output from the row buffers used for character selection in the character generator.
$\overline{CS}$	22	I	CHIP SELECT: The read and write are enabled by $\overline{CS}$.
C/$\overline{P}$	21	I	PORT ADDRESS: A high input on C/$\overline{P}$ selects "C" port or command registers and a low input selects the "P" port or parameter registers.
VCC	40	–	+5V Power supply.
GND	20	–	Ground (0V)

SAB 8276 Block diagram showing counter and register functions



Functional Description

Data bus buffer

This three-state, bidirectional, 8-bit buffer is used to interface the SAB 8276 to the system data bus.

This functional block accepts inputs from the system control bus and generates control signals for overall device operation. It contains the command, parameter, and status registers that store various control formats for the device functional definition.

C/$\overline{P}$	Operation	Register
0	Read	Reserved
0	Write	Parameter
1	Read	STATUS
1	Write	COMMAND

C/$\overline{P}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	$\overline{BS}$	
0	0	1	0	1	Reserved
0	1	0	0	1	Write 8276 Parameter
1	0	1	0	1	Read 8276 Status
1	1	0	0	1	Write 8276 Command
X	1	0	1	0	Write 8276 Row Buffer
X	1	1	X	X	High Impedance
X	X	X	1	1	High Impedance

$\overline{RD}$ (Read)

A "low" on this input informs the SAB 8276 that the CPU is reading data or status information from the SAB 8276.

$\overline{WR}$ (Write)

A "low" on this input informs the SAB 8276 that the CPU is writing data or control words to the SAB 8276.

$\overline{CS}$ (Chip select)

A "low" on this input selects the SAB 8276. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the data bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.

BRDY (BUFFER READY)

A "high" on this output indicates that the SAB 8276 is ready to receive character data.

$\overline{BS}$ (BUFFER SELECT)

A "low" on this input enables $\overline{WR}$ of character data to the SAB 8276 row buffers.

INT (Interrupt Output)

A "high" on this output informs the CPU that the SAB 8276 desires interrupt service.

Character counter

The character counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (character clock) input, which should be a derivative of the external dot clock.

Line counter

The line counter is a programmable counter that is used to determine the number of horizontal lines (sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row counter

The row counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Raster timing and video controls

The raster timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The video control circuitry controls the generation of HGLT (highlight), RVV (reverse video), LTEN (Light enable), VSP (video suppress), and GPA0–1 (general purpose attribute) outputs.

Row buffers

The row buffers are two 80 character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

Buffer input/output controllers

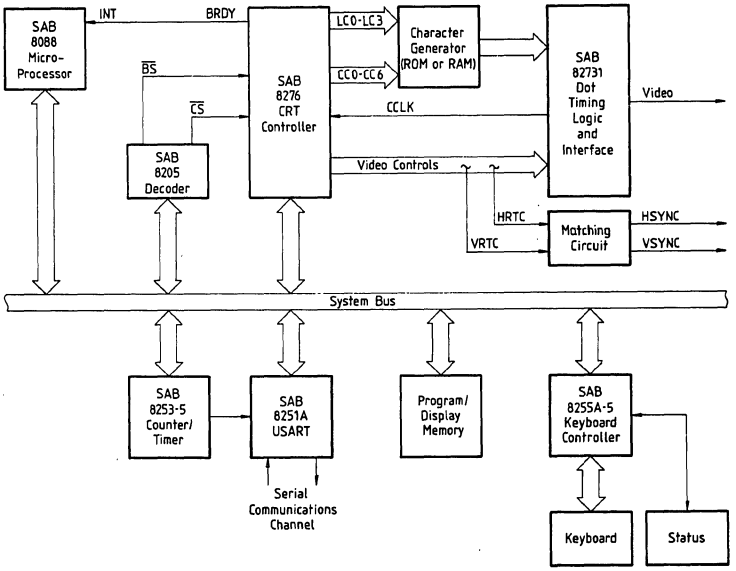
The buffer input/output controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action (Examples: A "HIGHLIGHT" attribute will cause the Buffer Output Controller to activate the HGLT output).

System Operation

The SAB 8276 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with standard character generator for dot matrix decoding.
Dot level must be provided by external circuitry.

SAB 8276 Block diagram showing systems operation



Raster timing

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then cause the line counter to increment, and it starts counting out the horizontal retrace (programmable from 2 to 32). This is constantly repeated.

The line counter is driven by the character counter. It is used to generate the line address outputs (LC0–3) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

The video suppression output (VSP) is active during horizontal and vertical retrace intervals.

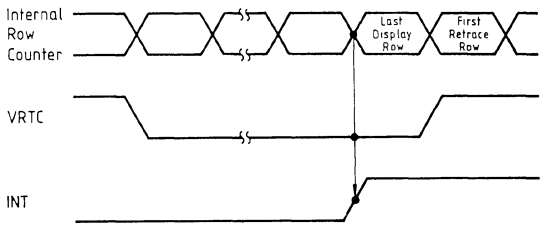
Dot level timing circuitry must synchronize these outputs with the video signal to the CRT display.

Interrupt timing

The SAB 8276 can be programmed to generate an interrupt request at the end of each frame.

If the SAB 8276 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row*.

Beginning of interrupt request



IRQ will go inactive after the status register is read.

End of interrupt

A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Note: Upon power-up, the SAB 8276 interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the SAB 8276 before system interrupts are enabled.

Generalsystems operational description

Display characters are retrieved from memory and displayed on a row by row basis. The SAB 8276 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays (see programming section).

The SAB 8276 uses BRDY to request data to fill the row buffer that is not being used for display. The SAB 8276 displays character rows one line at a time. The number of lines per character row, the underline position, and blanking of top and bottom lines are programmable (see programming section).

The SAB 8276 provides special control codes which can be used to minimize overhead. It also provides visual attribute codes to cause special action on the screen without the use of the character generator (see visual attribute section).

The SAB 8276 also controls raster timing. This is done by generating horizontal retrace (HRTC) and vertical retrace (VRTC) signals. The timing of these signals is programmable.

The SAB 8276 can generate a cursor. Cursor location and format are programmable (see programming section).

Display row buffering

Before the start of a frame, the SAB 8276 uses BRDY and $\overline{BS}$ to fill one row buffer with characters.

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, the other row buffer is filled with the next row of characters.

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

This is repeated until all of the character rows are displayed.

Screen format

The SAB 8276 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

The SAB 8276 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. Display data is not requested for the blanked rows.

Row format

The SAB 8276 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the whole character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*.

Note: In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by line counter.

Mode 0 is useful for character generators that leave address zero blank and start at address 1, Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

If the line *number* underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (light enable) signal.

Dot format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

Note: Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

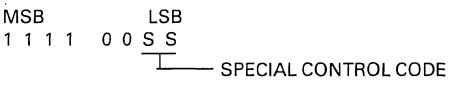
Visual Attributes and Special Codes

The characters processed by the SAB 8276 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The most significant bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

Special codes

Four special codes are available to help reduce memory, software or DMA overhead.

Special control character



S S	Function
0 0	End of Row
0 1	End of Row-stop Buffer Loading
1 0	End of Screen
1 1	End of Screen-stop Buffer Loading

The end-of-row code (00) activates VSP and holds it to the end of the line.

The end-of-row Buffer Loading code (BRDY) causes the Buffer Loading control logic to stop Buffer Loading for the rest of the row when it is written into the row buffer. It affects the display in the same way as the end-of-row code (00).

The end-of-screen code (10) activates VSP and holds it to the end of the frame.

The end-of-screen-stop Buffer Loading code (BRDY) causes the Buffer Loading control logic to stop Buffer Loading for the rest of the frame when it is written into the row buffer. It affects the display in the same way as the end-of-screen code (10).

If the stop Buffer Loading feature is not used, all characters after an end-of-row character are ignored, except for the end-of-screen character, which operates normally. All characters after an end-of-screen character are ignored.

Note: If a stop Buffer Loading character is not the last character in a burst or row, Buffer Loading is not stopped until after the next character is read. In the situation, a dummy character must be placed in memory after the stop Buffer Loading character.

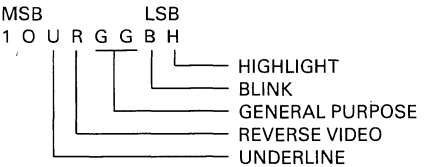
Field attributes

The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

There are six field attributes:

1. *Blink* – Characters following the code are caused to blink by activating the Video Suppression Output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* – Characters following the code are caused to be highlighted by activating the Highlight Output (HGLT).
3. *Reverse Video* – Characters following the code are caused to appear with reverse video by activating the Reverse Video Output (RVV).
4. *Underline* – Characters following the code are caused to be underlined by activating the Light Enable Output (LTEN).
5. 6. *General Purpose* – There are two additional SAB 8276 outputs which act as general purpose, independently programmable field attributes. GPA0–1 are active high outputs.

Field attribute code



H = 1 for highlighting
B = 1 for blinking
R = 1 for reverse video
U = 1 for underline
GG = GPA1, GPA0

* More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

Cursor timing

The cursor location is determined by a cursor row register and a character position register which are located by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.
If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Device programming

The SAB 8276 has two programming registers, the command register and the parameter register. It also has a status register. The command register can only be written into and the Status registers can only be read from. They are addressed as follows:

A_0	operation	register
0	Read	Reserved
0	Write	Parameter
1	Read	Status
1	Write	Command

The SAB 8276 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

Instruction Set

The SAB 8276 instruction set consists of 7 commands.

Command	No. of parameter bytes
Reset	4
Start Display	0
Stop Display	0
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

In addition, the status of the SAB 8276 can be read by the CPU at any time.

1 Reset command

	Operation	C/$\overline{P}$	Description	Data bus MSB							LSB
Command	Write	1	Reset command	0	0	0	0	0	0	0	0
Parameters	Write	0	Screen comp Byte 1	S	H	H	H	H	H	H	H
	Write	0	Screen comp Byte 2	V	V	R	R	R	R	R	R
	Write	0	Screen comp Byte 3	U	U	U	U	L	L	L	L
	Write	0	Screen comp Byte 4	M	1	C	C	Z	Z	Z	Z

Action – After the reset command is written, BRDY goes inactive, SAB 8276 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up. As parameters are written, the screen composition is defined.

Parameter – S Spaced rows

S	Functions
0	Normal rows
1	Spaced rows

Parameter – HHHHHHH Horizontal characters/row

H	H	H	H	H	H	H	No. of characters per row
0	0	0	0	0	0	0	1
0	0	0	0	0	0	1	2
0	0	0	0	0	1	0	3
			.				.
			.				.
			.				.
1	0	0	1	1	1	1	80
1	0	1	0	0	0	0	Undefined
			.				.
			.				.
			.				.
1	1	1	1	1	1	1	Undefined

Parameter – VV Vertical retrace row count

V	V	No. of row counts per VRTC
0	0	1
0	1	2
1	0	3
1	1	4

Parameter – LLLL Number of lines per character row

L	L	L	L	No. of lines/row
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter – M Line counter mode

M	Line counter mode
0	Mode 0 (non-offset)
1	Mode 1 (offset by 1 count)

Parameter – RRRRRR Vertical rows/frame

R	R	R	R	R	R	No. of rows/frame
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
			.			.
			.			.
			.			.
1	1	1	1	1	1	64

Parameter – UUUU Underline placement

U	U	U	U	Line number of underline
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Note: uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

Parameter – ZZZZ Horizontal retrace count

Z	Z	Z	Z	No. of character counts per HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

Parameter – CC Cursor format

C	C	Cursor format
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Nonblinking reverse video block
1	1	Nonblinking underline

2 Start display command

	Operation	C/$\overline{P}$	Description	Data bus MSB LSB
Command	Write	1	Start display	0 0 1 0 0 0 0 0
No parameters				

Action – SAB 8276 interrupts are enabled, DMA requests begin, video is enabled, interrupt enable and video enable status flags are set.

3 Stop display command

	Operation	C/$\overline{P}$	Description	Data bus MSB LSB
Command	Write	1	Stop display	0 1 0 0 0 0 0 0
No parameters				

Action – Disables video, interrupts remain enabled. HRTC and VRTC continue to run, video enable status flag is reset, and the "Start display" command must be given to re-enable the display.

4 Load cursor position

	Operation	C$\overline{P}$	Description	Data bus MSB LSB
Command	Write	1	Load cursor	1 0 0 0 0 0 0 0
Parameters	Write	0	Char. number	(Char. position in row)
	Write	0	Row number	(Row number)

Action – The SAB 8276 is conditioned to place, the next two parameter bytes into the cursor position registers. Status flags not affected.

5 Enable interrupt command

	Operation	C/$\overline{P}$	Description	Data bus MSB LSB
Command	Write	1	Enable interrupt	1 0 1 0 0 0 0 0
No parameters				

Action – The interrupt enable status flag is set and interrupts are enabled.

6 Disable interrupt command

	Operation	C/$\overline{P}$	Description	Data bus MSB							LSB
Command	Write	1	Disable interrupt	1	1	0	0	0	0	0	0
No parameters											

Action – Interrupts are disabled and the interrupt enable status flag is reset.

7 Preset counters command

	Operation	C/$\overline{P}$	Description	Data bus MSB							LSB
Command	Write	1	Preset counters	1	1	1	0	0	0	0	0
No parameters											

Action – The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU. After this command, two additional clock cycles are required before the first character of the first row is put out.

Status flags

	Operation	C/$\overline{P}$	Description	Data bus MSB							LSB
Command	Read	1	Status word	0	IE	IR	X	IC	VE	BU	X

IE – (Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command reset with the "Reset" command.

IR – (Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

IC – (Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE – (Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

BU – (Buffer Underrun) This flag is set whenever a Row Buffer is not filled with character data in time for buffer swap required by the display. Upon activation of this bit, buffer loading ceases, and the screen is blanked until after the vertical retrace interval.

Absolute Maximum Ratings [1)]

Temperature under bias	0 to +70 °C
Storage temperature	−65 to +150 °C
All output ans supply and supply voltages	−0.5 to +7 V
All input voltages	−0.5 to +5.5 V
Power dissipation	1.0 W

D.C. Characteristics

(TA = 0 to 70°C, VCC = 5 V ±5%)

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
VIL	Input low voltage	−0.5	0.8	V	–
VIH	Input high voltage	2.0	VCC+0.5V		
VOL	Output low voltage	–	0.45		IOL = 2.2 mA
VOH	Output high voltage	2.4	–		IOH = −400 µA
IIL	Input load current	–	±10	µA	VIN = VCC to 0 V
IOFL	Output float leakage				VOUT = VCC to 0.45 V
ICC	VCC supply current		160	mA	–

Capacitance

(TA = 25°C, VCC = GND = 0 V)

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
CIN	Input capacitance	–	10	pF	fc = 1 MHz
CI/O	I/O capacitance		20		Unmeasured pins returned to GND

1) Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics (SAB 8276)

(TA = 0 to 70°C, VCC = 5.0 V ± 5%, GND = 0 V)

Clock timing

Symbol	Parameter	Limit values		Units	Test condition
		Min.	Max.		
TCLK	Clock period	480			
TKH	Clock high	240	–		
TKL	Clock low	160		ns	–
TKR	Clock rise	5	30		
TKF	Clock fall				

Bus parameters
Read cycle

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TAR	Address stable before READ	0			
TRA	Address hold time for READ		–		–
TRR	READ pulse width	250		ns	
TRD	Data delay from READ	–	200		CL = 150 pF
TDF	READ to data floating		100		

Write cycle

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TAW	Address stable before WRITE	0			
TWA	Address hold time for WRITE				
TWW	WRITE pulse width	250	–	ns	–
TDW	Data setting time for WRITE	150			
TWD	Data hold time for WRITE	0			

Other timings

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TCC	Character code output delay	–	150	ns	CL = 50 pF
THR	Horizontal retrace output delay		200		
TLC	Line count output delay		400		
TAT	Control-attribute output delay		275		
TVR	Vertical retrace output delay				
TRI	INT↓ from RD↑		250		
TWQ	BRDY↑ from WR↑				
TRQ	BRDY↓ from WR↓		200		
TLR	$\overline{BS}$↓ to WR↓	0	–		–
TRL	WR↑ to $\overline{BS}$↑				

A.C. Characteristics (SAB 8276-2)

(TA = 0 C to 70°C, VCC = 5.0 V ± 5%, GND = 0 V)

Clock timing

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TCLK	Clock period	320			
TKH	Clock high	120	–		
TKL	Clock low			ns	–
TKR	Clock rise	5	30		
TKF	Clock fall				

Bus parameters
Read cycle

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TAR	Address stable before READ	0			
TRA	Address hold time for READ		–		–
TRR	READ pulse width	250		ns	
TRD	Data delay from READ	–	200		CL = 150 pF
TDF	READ to data floating		100		

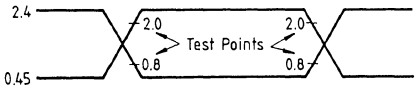
Write cycle

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TAW	Address stable before WRITE	0			
TWA	Address hold time for WRITE				
TWW	WRITE pulse width	250	–	ns	–
TDW	Data setting time for WRITE	150			
TWD	Data hold time for WRITE	0			

Other timings

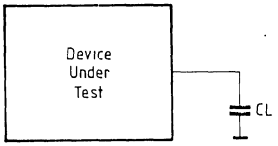
Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
TCC	Character code output delay	–	150	ns	CL = 50 pF
THR	Horizontal retrace output delay				
TLC	Line count output delay		250		
TAT	Control-attribute output delay				
TVR	Vertical retrace output delay				
TRI	INT↓ from RD↑				
TWQ	BRDY↑ from WR↑				
TRQ	BRDY↓ from WR↓		200		
TLR	$\overline{BS}$↑ to WR↓	0	–		–
TRL	WR↑ to $\overline{BS}$↑				

A.C. Testing input/output



AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

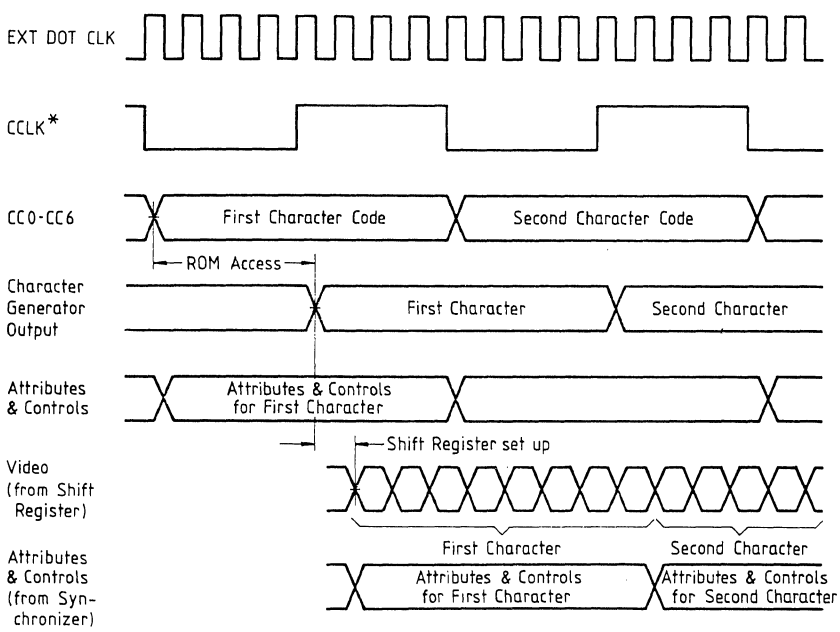
A.C. Testing load circuit



CL Includes Jig Capacitance

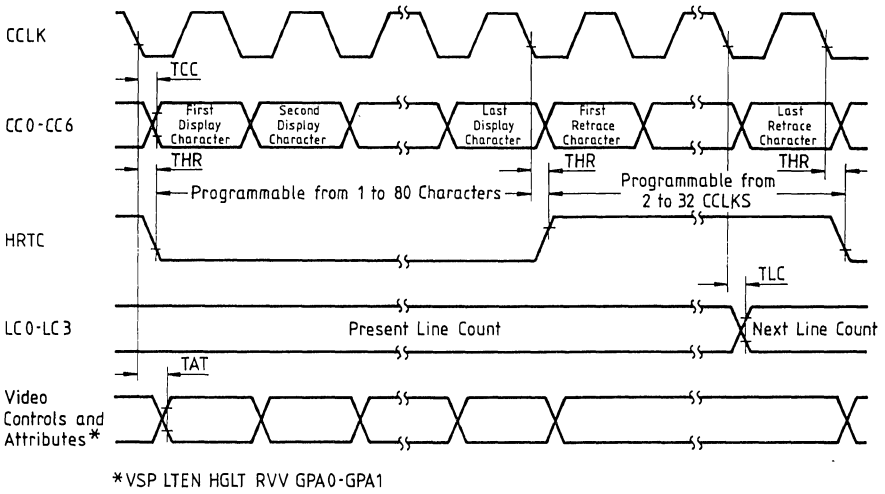
Waveforms

Typical dot level timing

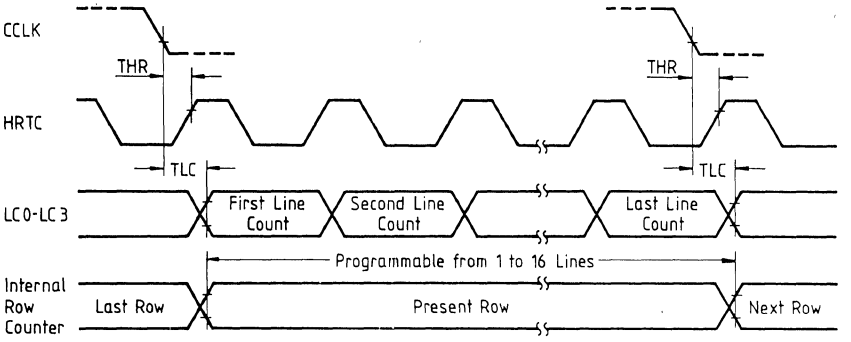


*CCLK is a Multiple of the Dot Clock and an Input to the SAB 8276

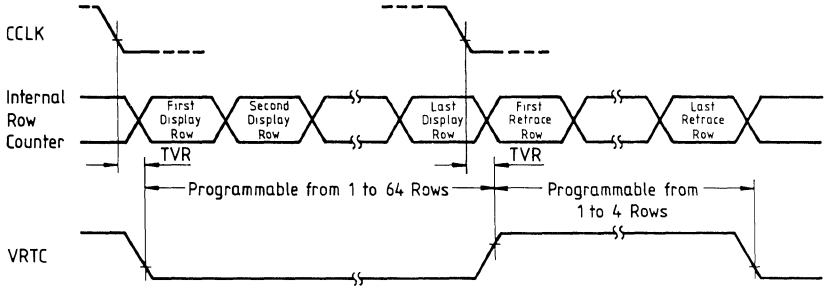
Line timing


CCLK
TCC
CC0-CC6
First Display Character
Second Display Character
Last Display Character
First Retrace Character
Last Retrace Character
THR
THR
THR
Programmable from 1 to 80 Characters
Programmable from 2 to 32 CCLKS
HRTC
TLC
LC0-LC3
Present Line Count
Next Line Count
TAT
Video Controls and Attributes*
*VSP LTEN HGLT RVV GPA0-GPA1

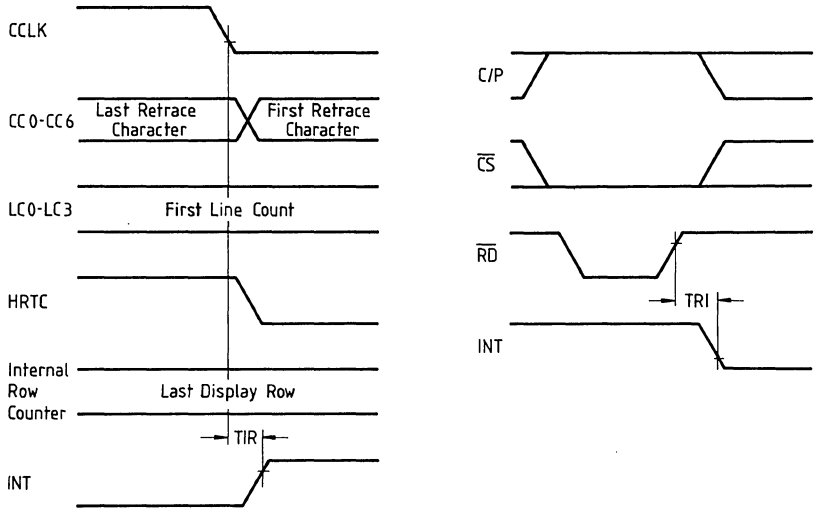
Row timing



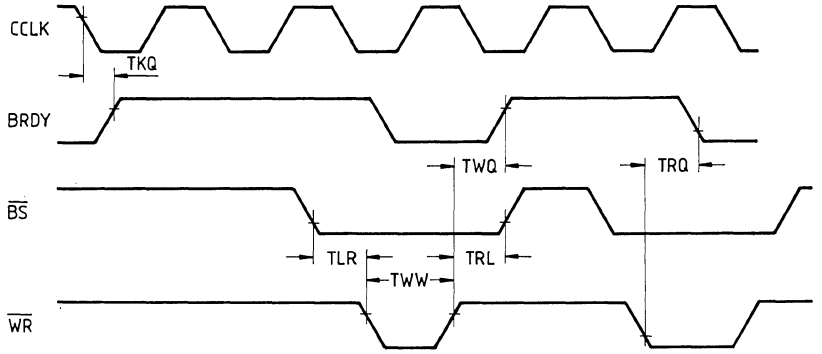
Frame timing



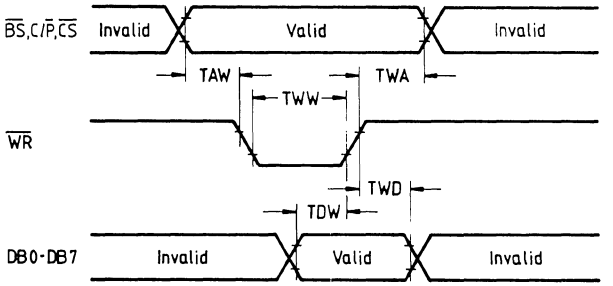
Interrupt timing



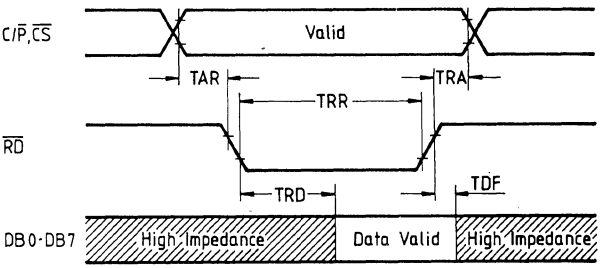
Timing for Buffer Loading



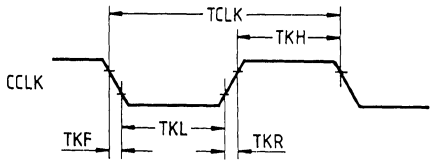
Write timing



Read timing



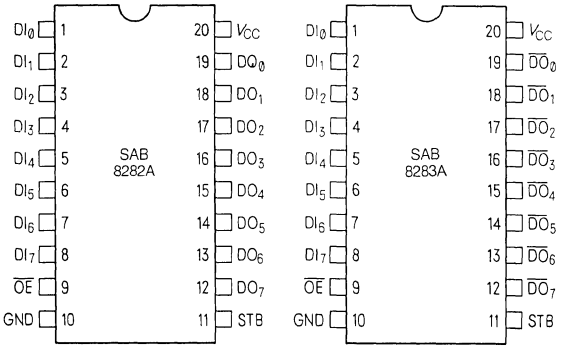
Clock timing



SAB 8282A/SAB 8283A
Octal Latch

- Fully compatible with SAB 8282/SAB 8283
- 40% Less Power Supply Current than Standard SAB 8282/SAB 8283
- Address Latch for SAB 80286, SAB 80186, SAB 8086, SAB 8085, SAB 8048 and SAB 8051 Families
- High Output Drive Capability for Driving System Data Bus
- Fully Parallel 8-Bit Data Register and Buffer
- No Output Low Noise when Entering or Leaving High Impedance State
- 3-State Outputs
- Transparent during Active Strobe
- 20-Pin Package

Pin Configuration



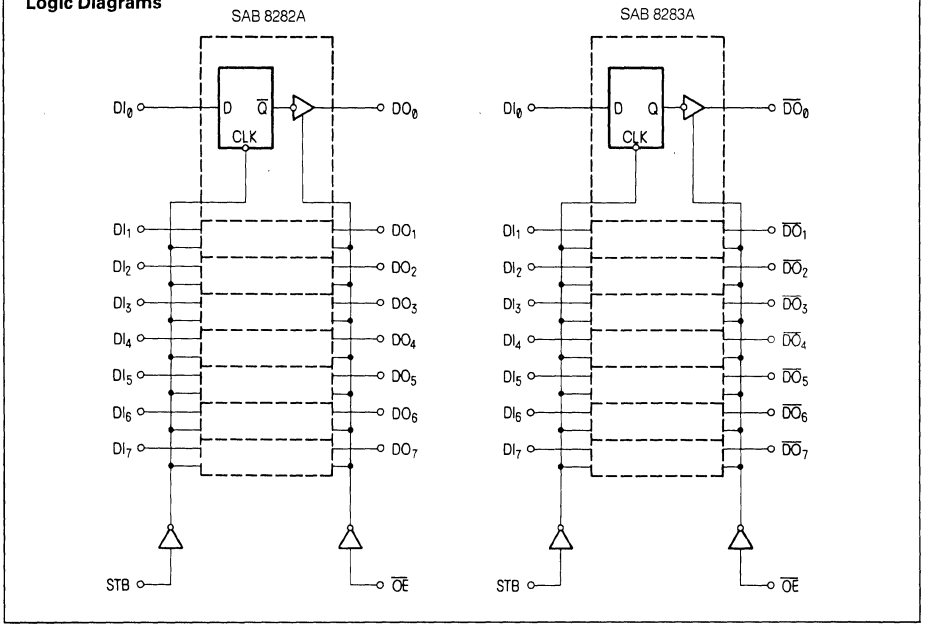
Pin Names

DI_0–DI_7	Data In
DO_0–DO_7	Data Out
$\overline{OE}$	Output Enable
STB	Strobe
V_{CC}	Power Supply (+5V)
GND	Ground (0V)

The SAB 8282A and SAB 8283A are 8-bit bipolar latches with 3-state output buffers. They can be used to implement latches, buffers, or multiplexers. The SAB 8283A inverts the input data at its outputs while the SAB 8282A does not.

Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with these devices. This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

Logic Diagrams



Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
STB	11	I	STROBE – STB is an input control pulse used to strobe data at the data input pins (A_0–A_7) into the data latches. This signal is active HIGH to admit input data. The data is latched at the HIGH to LOW transition of STB.
$\overline{OE}$	9	I	OUTPUT ENABLE – $\overline{OE}$ is an input control signal which when active LOW enables the contents of the data latches onto the data output pin (DO_0–DO_7 or $\overline{DO_0}$–$\overline{DO_7}$). $\overline{OE}$ being inactive HIGH forces the output buffers to their high impedance state.
DI_0–DI_7	1–8	I	DATA INPUT PINS – Data presented at these pins satisfying setup time requirements when STB is strobed and latched into the data input latches.
DO_0–DO_7 (SAB 8282A) $\overline{DO_0}$–$\overline{DO_7}$ (SAB 8283A)	12–19	O	DATA OUTPUT PINS – When $\overline{OE}$ is true, the data in the data latches is presented as inverted (SAB 8283A) or non-inverted (SAB 8282A) data onto the data output pins.
V_{CC}	20	–	Power Supply (+5V)
GND	10	–	Ground (0V)

Functional Description

The SAB 8282A and SAB 8283A octal latches are 8-bit latches with 3-state output buffers.
Data having satisfied the setup time requirements is latched into the data latches by strobing the STB line HIGH to LOW. Holding the STB line in its active HIGH state makes the latches appear transparent.

Data is presented to the data output pins by activating the $\overline{OE}$ input line. When $\overline{OE}$ is inactive HIGH the output buffers are in their high impedance state. Enabling or disabling the output buffers will not cause negative-going transients to appear on the data output bus.

Absolute Maximum Ratings[1)]

Temperature Under Bias	0 to +70°C
Storage Temperature	−65 to +150°C
All Output and Supply Voltages	−0.5 to +7V
All Input Voltages	−1.0 to +5.5V
Power Dissipation	1W

D. C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5V ±10%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_C	Input Clamp Voltage		−1	V	I_C = −5 mA
I_{CC}	Power Supply Current SAB 8282A SAB 8283A	–	 100 90	mA	all outputs open
I_F	Forward Input Current	–	−0.2		V_F = 0.45V
I_R	Reverse Input Current		50	µA	V_R = 5.25V
V_{OL}	Output LOW Voltage		0.45	V	I_{OL} = 32 mA
V_{OH}	Output HIGH Voltage	2.4	–		I_{OH} = −5 mA
I_{OFF}	Output Off Current	–	±50	µA	V_{OFF} = 0.45 to 5.25V
V_{IL}	Input LOW Voltage		0.8	V	V_{CC} = 5.0V [2)]
V_{IH}	Input HIGH Voltage	2.0	–		
C_{IN}	Input Capacitance	–	12	pF	F = 1 MHz V_{BIAS} = 2.5V, V_{CC} = 5V T_A = 25°C

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) Output Loading: I_{OL} = 32 mA; I_{OH} = −5 mA; C_L = 300 pF

A.C. Characteristics

T_A = 0 to +70°C; V_{CC} = +5 V ± 10%

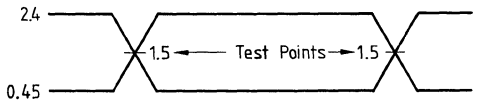
Loading

Outputs: I_{OL} = 32 mA; I_{OH} = −5 mA; C_L = 300 pF

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
t_{IVOV}	Input to Output Delay –Inverting –Non-Inverting	 5 5	 22 30	ns	2)
t_{SHOV}	STB to Output Delay –Inverting –Non-Inverting	 10 10	 40 45		
t_{EHOZ}	Output Disable Time	5	18		
t_{ELOV}	Output Enable Time	10	30		
t_{IVSL}	Input to STB Setup Time	0	–		
t_{SLIX}	Input to STB Hold Time	25			
t_{SHSL}	STB HIGH Time	15			
t_{ILIH}, t_{OLOH}	Input, Output Rise Time	–	20		From 0.8 to 2.0 V
t_{IHIL}, t_{OHOL}	Input, Output Fall Time		12		From 2.0 to 0.8 V

A.C. Testing Input, Output Waveform

Input/Output

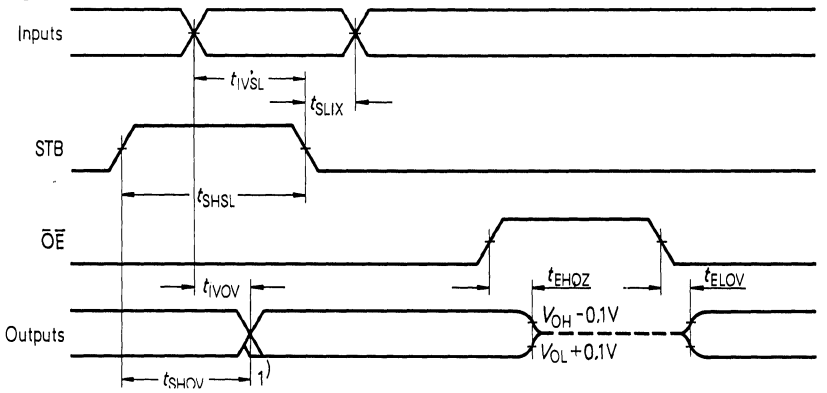


A.C. Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 1.5 V for both a logic "1" and "0".

Waveforms

All timing measurements are made at 1.5 V unless otherwise noted.

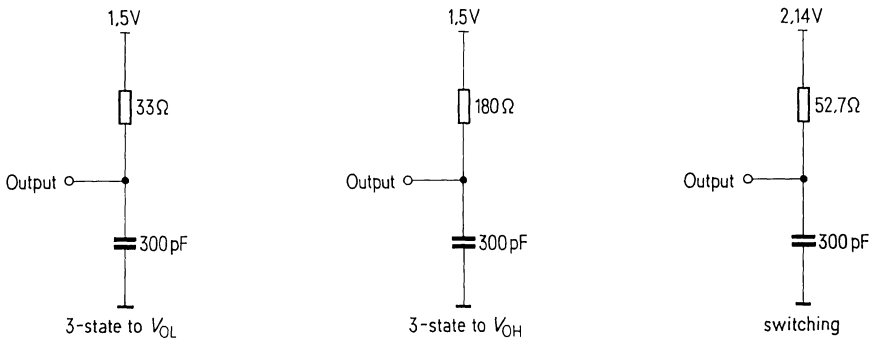
Timing



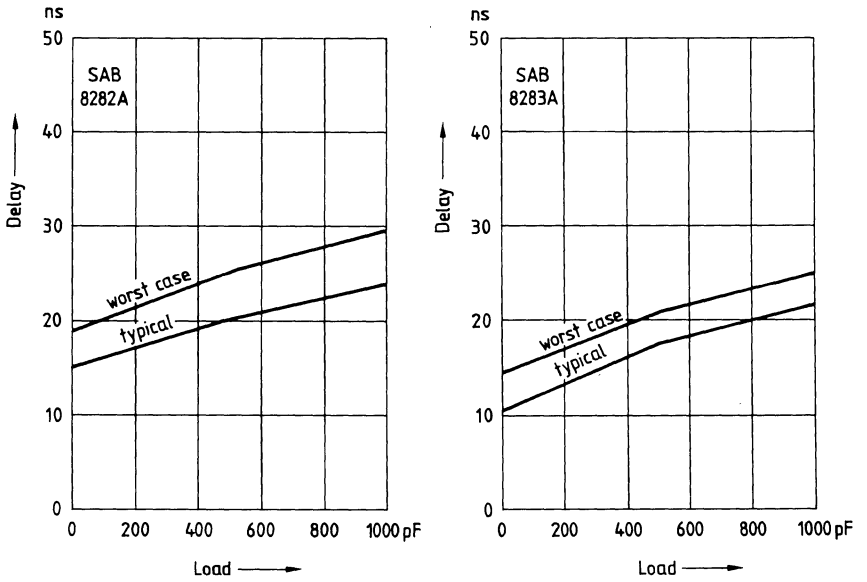
1) SAB 8283A Only – Output may be momentarily invalid following the high going STB transition.

2) See waveforms and test load circuit.

Output Test Load Circuits



Output Delay vs. Capacitance

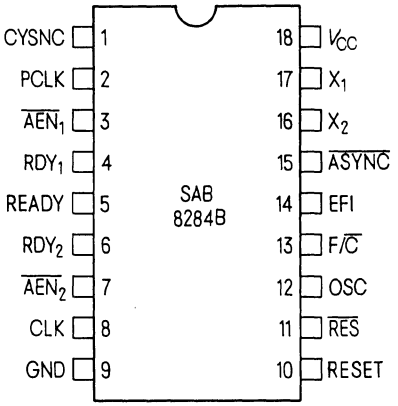


Preliminary

SAB 8284B, SAB 8284B-1 Clock Generator and Driver for SAB 8086 Family Processors

- Fully compatible with SAB 8284A, SAB 8284A-1
- 30% Less Power Supply Current than Standard SAB 8284A, SAB 8284A-1
- Generates the System clock for SAB 8086 and SAB 8088. Processors:
  up to 8 MHz with SAB 8284B
  up to 10 MHz with SAB 8284B-1
- Uses a Crystal or a TTL Signal for Frequency Source up to 30 MHz
- Provides Synchronization for Synchronous and Asynchronous READY Signals
- 18-Pin Package
- Single +5V Power Supply
- Generates System Reset Output from Schmitt Trigger Input
- Capable of Clock Synchronization with Other SAB 8284Bs

Figure 1
Pin Configuration



Pin Names

X_1 X_2	Connections for crystal
F/$\overline{C}$	Clock source select
EFI	External clock input
CSYNC	Clock synchronization input
$\overline{ASYNC}$	Ready synchronization select
$\overline{RDY_1}$ $\overline{RDY_2}$	Ready signal
$\overline{AEN_1}$ $\overline{AEN_2}$	Address enabled qualifiers for $RDY_{1,2}$
$\overline{RES}$	Reset input
RESET	Synchronized reset output
OSC	Oscillator output
CLK	MOS Clock for the processor
PCLK	TTL Clock for peripherals
READY	Synchronized ready output
V_{CC}	Power Supply (+5V)
GND	Ground (OV)

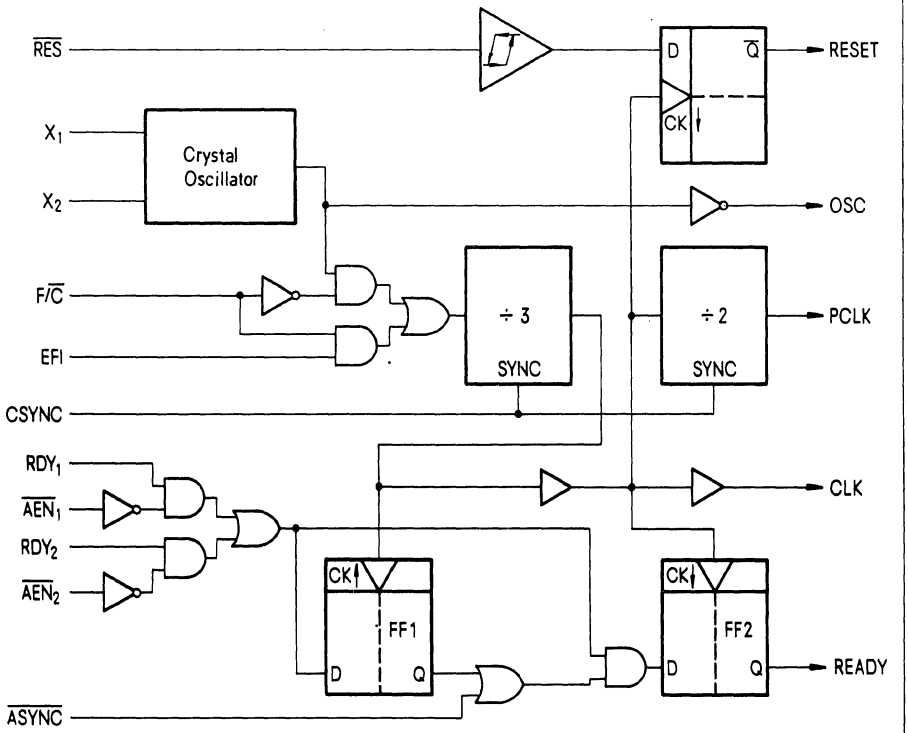
SAB 8284B is a bipolar clock generator/driver designed to provide clock signals for SAB 8086 and SAB 8088 processors and peripherals. It also contains READY logic for operation with two bus systems and provides the processors required READY synchronization and timing. Reset logic with hysteresis and synchronization is also provided. This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
$\overline{AEN_1}$ $\overline{AEN_2}$	3, 7	I	ADDRESS ENABLE. $\overline{AEN}$ is an active LOW signal. $\overline{AEN}$ serves to qualify its respective Bus Ready Signal (RDY_1 or RDY_2). $\overline{AEN_1}$ validates RDY_1 while $\overline{AEN_2}$ validates RDY_2. Two $\overline{AEN}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Busses. In non Multi-Master configurations the $\overline{AEN}$ signal inputs are tied true (LOW).
RDY_1, RDY_2	4, 6	I	BUS READY (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{AEN_1}$ while RDY2 is qualified by $\overline{AEN_2}$.
$\overline{ASYNC}$	15	I	READY SYNCHRONIZATION SELECT. $\overline{ASYNC}$ is an input which defines the synchronization mode of the READY logic. When $\overline{ASYNC}$ is low, two stages of READY synchronization are provided. When $\overline{ASYNC}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	5	O	READY. READY is an active HIGH signal which is the synchronized RDY signal input. READY is cleared after the guaranteed hold time to the processor has been met.
X_1, X_2	16, 17	I	CRYSTAL IN. X_1 and X_2 are the pins to which a crystal is attached. The crystal frequency is 3 times the desired processor clock frequency.
F/$\overline{C}$	13	I	FREQUENCY/CRYSTAL SELECT. F/$\overline{C}$ is a strapping option. When strapped LOW, F/$\overline{C}$ permits the processors clock to be generated by the crystal. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the EFI input.
EFI	14	I	EXTERNAL FREQUENCY IN. When F/$\overline{C}$ is strapped HIGH, CLK is generated from the input frequency appearing on this pin. The input signal is a square wave 3 times the frequency of the desired CLK output.
CLK	8	O	PROCESSOR CLOCK. CLK is the clock output used by the processor and all devices which directly connect to the processor's local bus (i.e., the bipolar support chips and other MOS devices). CLK has an output frequency which is 1/3 of the crystal or EFI input frequency and a 1/3 duty cycle. An output HIGH of 4.5 volts (V_{CC} = 5V) is provided on this pin to drive MOS devices.
PCLK	2	O	PERIPHERAL CLOCK. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK and has 50% duty cycle.
OSC	12	O	OSCILLATOR OUTPUT. OSC is the TTL level output of the internal oscillator circuitry. Its frequency is equal to that of the crystal.
$\overline{RES}$	11	I	RESET IN. $\overline{RES}$ is an active LOW signal which is used to generate RESET. The SAB 8284B provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration.

Symbol	Number	Input (I) Output (O)	Function
RESET	10	O	RESET. RESET is an active HIGH signal which is used to reset the SAB 8086 family processors. Its timing characteristics are determined by $\overline{RES}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION. CSYNC is an active HIGH signal which allows multiple SAB 8284B to be synchronized to provide clocks that are in phase. When CSYNC is HIGH the internal counters are reset. When CSYNC goes LOW the internal counters are allowed to resume counting. CSYNC needs to be externally synchronized to EFI. When using the internal oscillator CSYNC should be hard-wired to ground.
V_{CC}	18	–	Power Supply (+5V)
GND	9	–	Ground (OV)

Figure 2
Block Diagram



Functional Description

General

The SAB 8248B is a single chip block generator/ driver for SAB 8086 and SAB 8088 processors. The chip contains a crystal-controlled oscillator, a divide-by-three counter, "Ready" synchronization and reset logic. Refer to Figure 2 for "Block Diagram" and Figure 1 for "Pin Configuration".

Oscillator

The oscillator circuit of the SAB 8284B is designed primarily for use with an external series resonant fundamental mode crystal from which the basic operating frequency is derived.

The crystal frequency should be selected at three times the required CPU clock. X1 and X2 are the two crystal input crystal connections. For the most stable operation of the oscillator (OSC) output circuit, two series resistors ($R_1 = R_2 = 510\ \Omega$) as shown in figure 7 are recommended. The output of the oscillator is buffered and brought out on OSC so that other system timing signals can be derived from this stable, crystal-controlled source.

It is advisable to limit stray capacitances to less than 10pF on X1 and X2 to minimize deviation from operating at the fundamental frequency.

Clock Generator

The clock generator consists of a synchronous divide-by-three counter with a special clear input that inhibits the counting. This clear input (CSYNC) allows the output clock to be synchronized with an external event (such as another SAB 8284B clock). It is necessary to synchronize the CSYNC input to the EFI clock external to the SAB 8284B. This is accomplished with two Schottky flip-flops (see figure 3). The counter output is a 33% duty cycle clock at one-third the input frequency.

The F/$\overline{C}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the clock for the ÷3 counter. If the EFI input is selected as the clock source, the oscillator section can be used independently for another clock source. Output is taken from OSC.

Clock Outputs

The CLK output is a 33% duty cycle MOS clock driver designed to drive the SAB 8086 and SAB 8088 processors directly. PCLK is a TTL level peripheral clock signal whose output frequency is 1/2 that of CLK. PCLK has 50% duty cycle.

Reset Logic

The reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate the reset timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the SAB 8284B. Waveforms for clocks and reset signals are illustrated in Figure 4.

READY Synchronization

Two READY inputs (RDY_1, RDY_2) are provided to accomodate two Multi-Master system busses. Each input has a qualifier ($\overline{AEN_1}$ and $\overline{AEN_2}$, respectively).

The $\overline{AEN}$ signals validate their respective RDY signals. If a Multi-Master system is not being used the $\overline{AEN}$ pin should be tied LOW.

Synchronization is required for all asynchronous active going edges of either RDY input to guarantee that the RDY setup and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

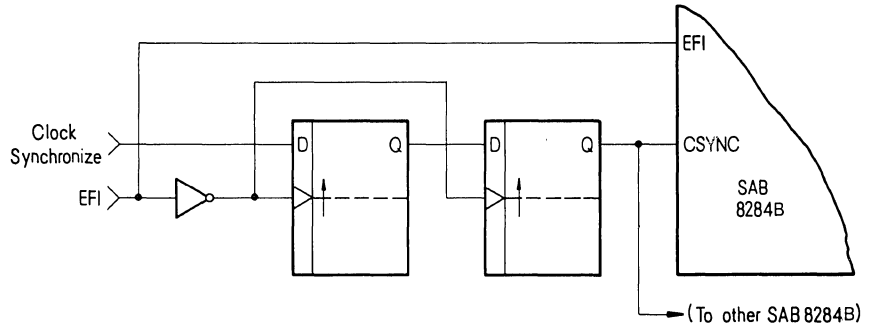
The $\overline{ASYNC}$ input defines two modes of READY synchronization operation.

When $\overline{ASYNC}$ is LOW, two stages of synchronization are provided for active READY input signals. Positive-going asynchronous READY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time t_{R1VCH}) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go active (HIGH). Negative-going asynchronous READY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the READY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing, t_{R1VCL}, on each bus cycle (Refer to Figure 5).

When $\overline{ASYNC}$ is high or left open, the first READY flip-flop is bypassed in the READY synchronization logic. READY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices **that can be guaranteed to meet the required RDY time** (Refer to Figure 6).

$\overline{ASYNC}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

Figure 3
CSYNC Synchronization



Absolute maximum ratings [1]

Temperature Under Bias	0 to 70°C
Storage Temperature	− 65 to 150°C
All Output and Supply Voltages	−0.5 to 7 V
All Input Voltages	−1.0 to 5.5 V
Power Dissipation	1W

D.C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5 V ±10%

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
I_F	Forward Input Current ($\overline{ASYNC}$) Other Inputs		−1.3 −0.5	mA	V_F = 0.45 V V_F = 0.45 V
I_R	Reverse Input Current ($\overline{ASYNC}$) Other Inputs	–	50 50	µA	$V_R = V_{CC}$ V_R = 5.25 V
V_C	Input Forward Clamp Voltage		−1.0	V	I_C = −5 mA
I_{CC}	Power Supply Current		110	mA	All outputs open
V_{IL}	Input LOW Voltage		0.8	V	–
V_{IH}	Input HIGH Voltage	2.0	–		
V_{IHR}	Reset Input HIGH Voltage	2.6			
V_{OL}	Output LOW Voltage	–	0.45		5 mA
V_{OH}	Output HIGH Voltage CLK Other Outputs	4 2.4	–		−1 mA −1 mA
$V_{IHR}-V_{ILR}$	$\overline{RES}$ Input Hysteresis	0.25			–

[1]) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics

T_A = 0 to +70°C; V_{CC} = +5 V ±10%

Timing Requirements

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
t_{EHEL}	External Frequency HIGH Time	13		ns	90%–90% V_{IN}
t_{ELEH}	External Frequency LOW Time		–		10%–10% V_{IN}
t_{ELEL}	EFI Period	$t_{EHEL}+t_{ELEH}+\delta$			[3]
	XTAL Frequency	12	25 [7]	MHz	–
t_{R1VCL}	RDY_1, RDY_2 Active Setup to CLK	35		ns	$\overline{ASYNC}$ = HIGH
t_{R1VCH}	RDY_1, RDY_2 Active Setup to CLK				$\overline{ASYNC}$ = LOW
t_{R1VCL}	RDY_1, RDY_2 Inactive Setup to CLK				–
t_{CLR1X}	RDY_1, RDY_2 Hold to CLK	0			
t_{AYVCL}	$\overline{ASYNC}$ Setup to CLK	50			
t_{CLAYX}	$\overline{ASYNC}$ Hold to CLK	0			
t_{A1VR1V}	$\overline{AEN_1}$, $\overline{AEN_2}$ Setup to RDY_1, RDY_2	15	–		
t_{CLA1X}	$\overline{AEN_1}$, $\overline{AEN_2}$ Hold to CLK	0			
t_{YHEH}	CSYNC Setup to EFI	20			
t_{EHYL}	CSYNC Hold to EFI	10			
t_{YHYL}	CSYNC Width	$2 \cdot t_{ELEL}$			
t_{I1HCL}	$\overline{RES}$ Setup to CLK	65			[4]
t_{CLI1H}	$\overline{RES}$ Hold to CLK	20			
t_{ILIH}	Input Rise Time	–	20		From 0.8 V to 2.0 V
t_{IHIL}	Input Fall Time		12		From 2.0 V to 0.8 V

Notes see next page.

Timing Responses

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
t_{CLCL}	CLK Cycle Period	100			–
t_{CHCL}	CLK HIGH Time	[1]	–		Fig. 7 & Fig. 8
t_{CLCH}	CLK LOW Time	[2]			Fig. 7 & Fig. 8
t_{CH1CH2} t_{CL2CL1}	CLK Rise or Fall Time	–	10		1.0 V to 3.5 V
t_{PHPL}	PCLK HIGH Time	t_{CLCL}–20			–
t_{PLPH}	PCLK LOW Time	t_{CLCL}–20	–		
t_{RYLCL}	Ready Inactive to CLK [6]	–8		ns	Fig. 9 & Fig. 10
t_{RYHCH}	Ready Active to CLK [5]	[2]			Fig. 9 & Fig. 10
t_{CLIL}	CLK to Reset Delay		40		–
t_{CLPH}	CLK to PCLK HIGH Delay	–			
t_{CLPL}	CLK to PCLK LOW Delay		22		
t_{OLCH}	OSC to CLK HIGH Delay	–5			
t_{OLCL}	OSC to CLK LOW Delay	2	35		
t_{OLOH}	Output Rise Time (except CLK)	–	20		From 0.8 V to 2.0 V
t_{OHOL}	Output Fall Time (except CLK)		12		From 2.0 V to 0.8 V

[1]) ($^1/_3$ t_{CLCL}) +2 for CLK Freq. ≤ 8 MHz
($^1/_3$ t_{CLCL}) +6 for CLK Freq. = 10 MHz

[2]) ($^2/_3$ t_{CLCL}) –15 for CLK Freq. ≤ 8 MHz
($^2/_3$ t_{CLCL}) –14 for CLK Freq. = 10 MHZ

[3]) δ = EFI rise (5 ns max) + EFI fall (5 ns max).

[4]) Setup and hold necessary only to guarantee recognition at next clock.

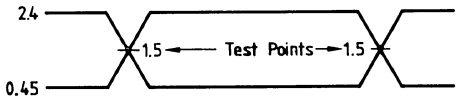
[5]) Applies only to T_3 and T_W states.

[6]) Applies only to T_2 states.

[7]) 30 MHz for SAB 8284B–1

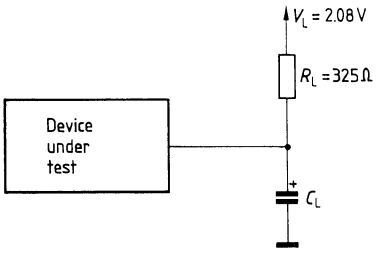
A.C. Testing

Input/Output Waveform



A.C. Testing: Input are driven at 2.4 V for a Logic "1" and 0.45 V for a Logic "0".
Timing Measurements are made at 1.5 V for Both a Logic "1" and "0".

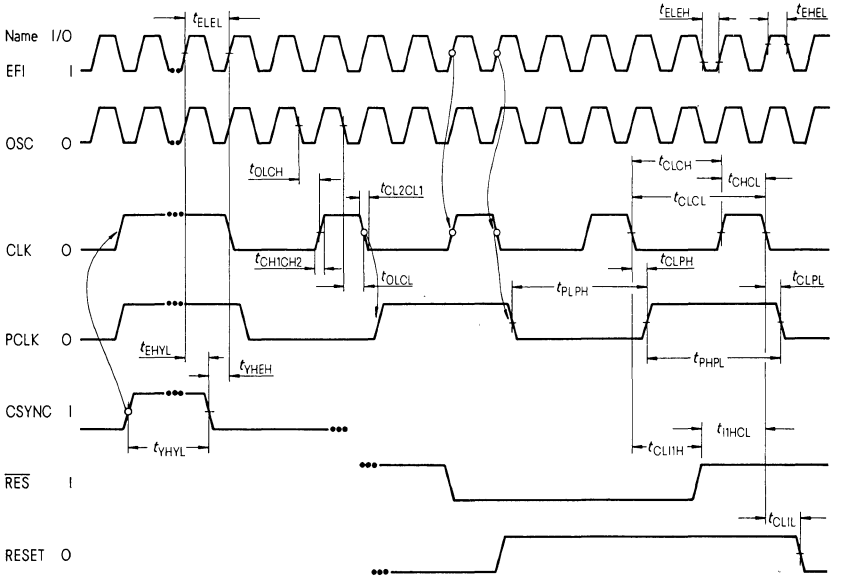
Load Circuit



C_L = 100 pF for CLK
C_L = 30 pF for READY

Waveforms

Figure 4
Clocks and Reset Signals



Note All timing measurements are made at 1.5 V, unless otherwise noted

Figure 5
Ready Signals – Asynchronous Devices

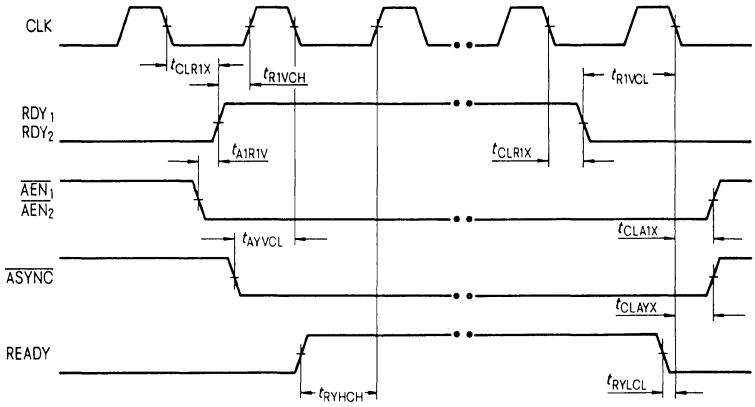
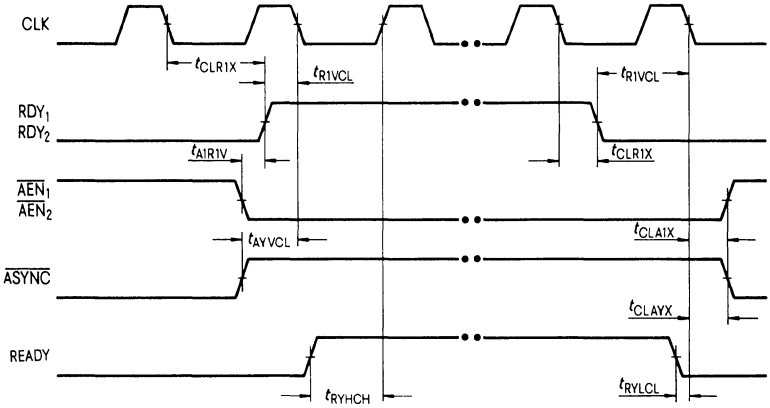


Figure 6
Ready Signals – Synchronous Devices



Testconditions

Figure 7
Clock High- and Low Time; Using X1, X2

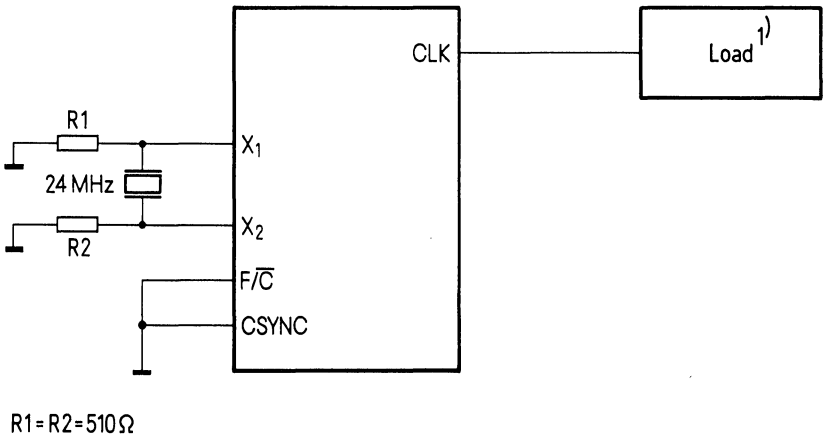
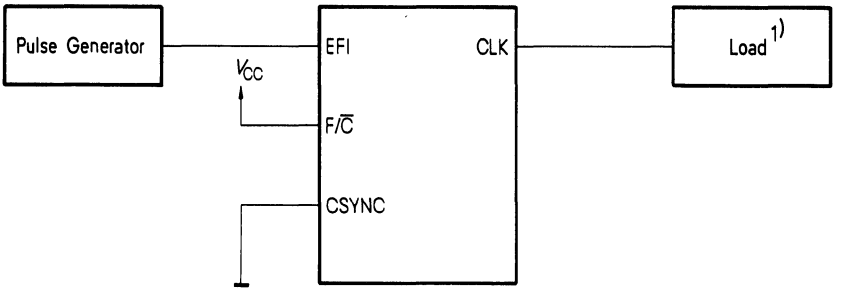
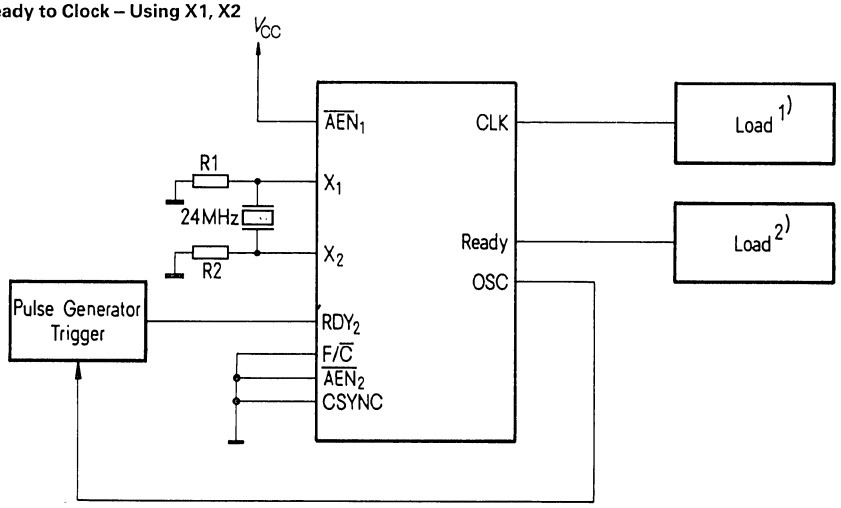


Figure 8
Clock High- and Low Time; Using EFI



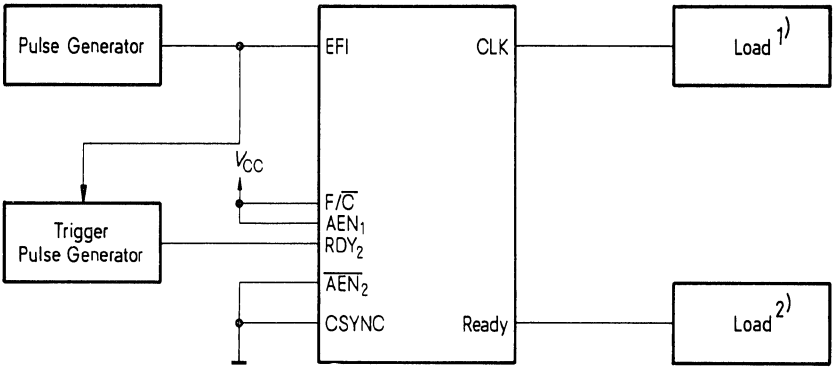
1) C_L = 100 pF

Figure 9
Ready to Clock – Using X1, X2



R1 = R2 = 510 Ω

Figure 10
Ready to Clock – Using EFI

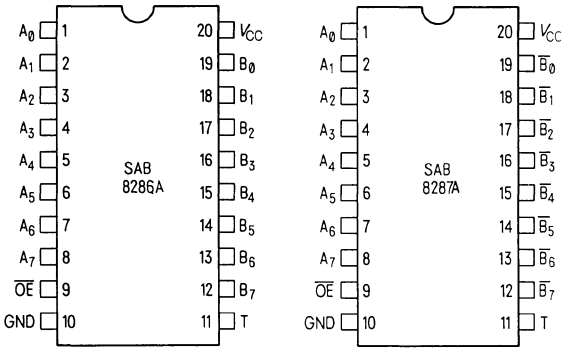


1) C_L = 100 pF
2) C_L = 30 pF

SAB 8286A/SAB 8287A
Octal Bus Transceiver

- Fully compatible with SAB 8286/SAB 8287
- 40% Less Power Supply Current than Standard SAB 8286/SAB 8287
- Data Bus Buffer Driver for SAB 80286, SAB 80186, SAB 8086, SAB 8085, SAB 8048 and SAB 8051 Families
- High Output Drive Capability for Driving System Data Bus
- Fully Parallel 8-Bit Transceivers
- 3-State Outputs
- 20-Pin Package
- No Output Low Noise when Entering or Leaving High Impedance State

Pin Configuration

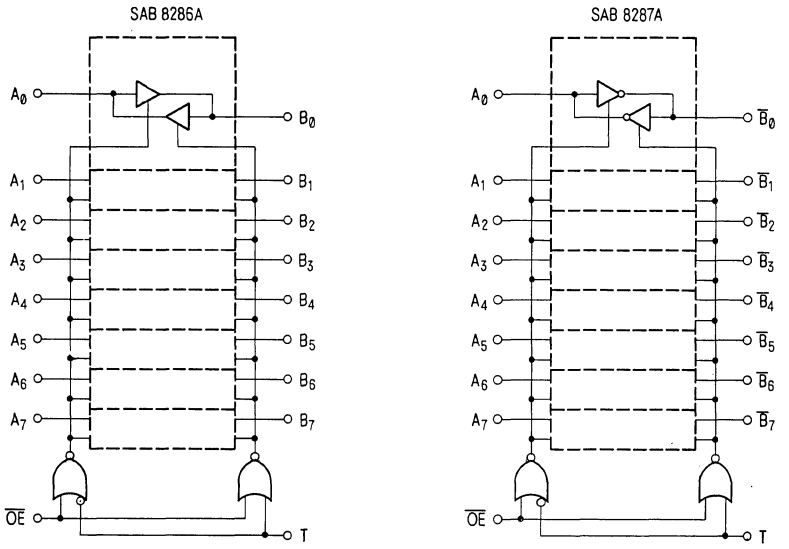


Pin Names

A_0–A_7	Local Bus Data
B_0–B_7	System Bus Data
$\overline{OE}$	Output Enable
T	Transmit
V_{CC}	Power Supply (+5V)
GND	Ground (0V)

The SAB 8286A and SAB 8287A are 8-bit bipolar transceivers with 3-state outputs. The SAB 8287A inverts the input data at its outputs while the SAB 8286A does not. Thus, a wide variety of applications for buffering in microcomputer systems can be met. This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

Logic Diagrams



Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
T	11	I	TRANSMIT – T is an input control signal used to control the direction of the transceivers. When HIGH, it configures the transceiver's B_0–B_7 as outputs with A_0–A_7 as inputs. T LOW configures A_{0-7} as the outputs with B_0–B_7 serving as the inputs.
$\overline{OE}$	9	I	OUTPUT ENABLE – $\overline{OE}$ is an input control signal used to enable the appropriate output driver (as selected by T) onto its respective bus. This signal is active LOW.
A_0–A_7	1–8	I/O	LOCAL BUS DATA PINS – These pins serve to either present data to or accept data from the processor's local bus depending upon the state of the T pin.
B_0–B_7 (SAB 8286A) $\overline{B_0}$–$\overline{B_7}$ (SAB 8287A)	12–19	I/O	SYSTEM BUS DATA PINS – These pins serve to either present data to or accept data from the system bus depending upon the state of the T pin.
V_{CC}	20	–	Power Supply (+5V)
GND	10	–	Ground (0V)

Functional Description

The SAB 8286A and SAB 8287A transceivers are 8-bit transceivers with high impedance outputs. With T active HIGH and $\overline{OE}$ active LOW, data at the A_0–A_7 pins is driven onto the B_0–B_7 pins. With T inactive LOW and $\overline{OE}$ active LOW, data at the B_0–B_7 pins is driven onto the A_0–A_7 pins. No output low glitching will occur whenever the transceivers are entering or leaving the high impedance state.

Absolute Maximum Ratings[1)]

Temperature Under Bias	0 to +70°C
Storage Temperature	−65 to +150°C
All Output and Supply Voltages	−0.5 to +7V
All Input Voltages	−1.0 to +5.5V
Power Dissipation	1W

D. C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5V ±10%

Symbol	Parameter	Limit Values Min.	Limit Values Max.	Unit	Test Condition
V_C	Input Clamp Voltage		−1	V	I_C = −5 mA
I_{CC}	Power Supply Current		90	mA	All outputs open
I_F	Forward Input Current	–	−0.2		V_F = 0.45V
I_R	Reverse Input Current		50	µA	V_R = 5.25V
V_{OL}	Output LOW Voltage – B Outputs – A Outputs		0.45 0.45	V	I_{OL} = 32 mA I_{OL} = 16 mA
V_{OH}	Output HIGH Voltage – B Outputs – A Outputs	2.4 2.4	–		I_{OH} = −5 mA I_{OH} = −1 mA
I_{OFF} I_{OFF}	Output Off Current Output Off Current	–	I_F I_R	–	V_{OFF} = 0.45V V_{OFF} = 5.25V
V_{IL}	Input LOW Voltage – A Side – B Side		0.8 0.9	V	V_{CC} = 5.0V, See Note 2 V_{CC} = 5.0V, See Note 2
V_{IH}	Input HIGH Voltage	2.0			V_{CC} = 5.0V, See Note 2
C_{IN}	Input Capacitance	–	12	pF	F = 1 MHz V_{BIAS} = 2.5V, V_{CC} = 5V T_A = 25°C

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2) B Outputs: I_{OL} = 32 mA; I_{OH} = −5 mA; C_L = 300 pF
A Outputs: I_{OL} = 16 mA; I_{OH} = −1 mA; C_L = 100 pF

A.C. Characteristics

T_A = 0 to +70°C; V_{CC} = +5 V ± 10%

Loading
B Outputs: I_{OL} = 32 mA; I_{OH} = −5 mA; C_L = 300 pF A Outputs: I_{OL} = 16 mA; I_{OH} = −1 mA; C_L = 100 pF

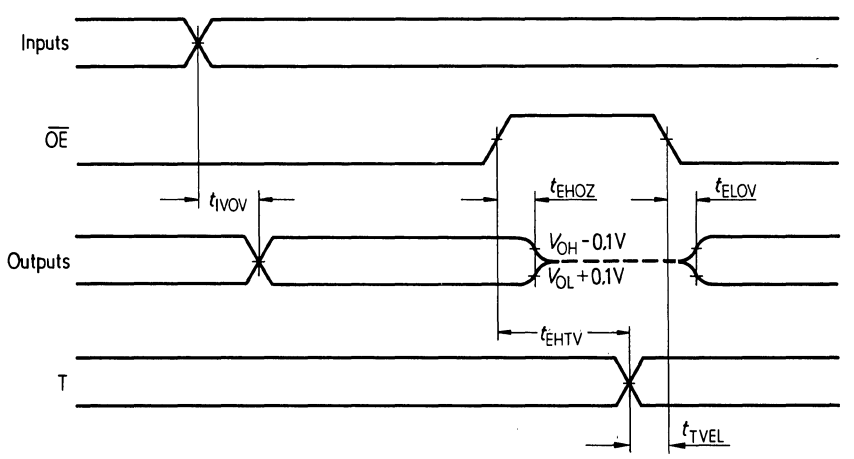
Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
t_{IVOV}	Input to Output Delay Inverting Non-Inverting	 5 5	 22 30	ns	1)
t_{EHTV}	Transmit/Receive Hold Time	5	–		
t_{TVEL}	Transmit/Receive Setup	10			
t_{EHOZ}	Output Disable Time	5	18		
t_{ELOV}	Output Enable Time	10	30		
t_{ILIH}, t_{OLOH}	Input, Output Rise Time	–	20		From 0.8 to 2.0 V
t_{IHIL}, t_{OHOL}	Input, Output Fall Time		12		From 2.0 to 0.8 V

1) See waveforms and test load circuit.

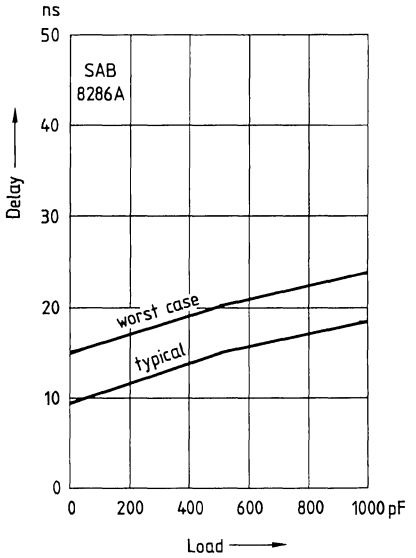
Waveforms

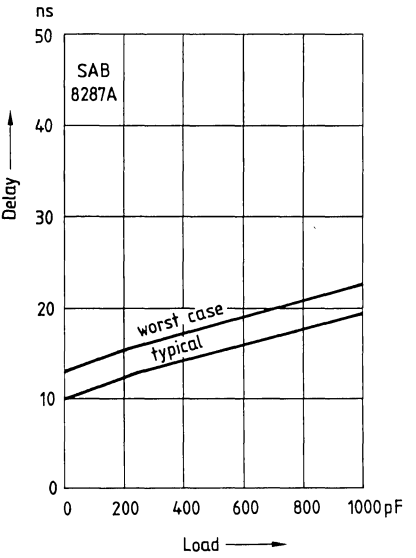
All timing measurements are made at 1.5 V unless otherwise noted.

Timing

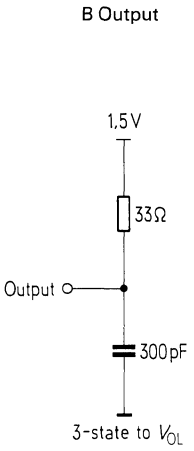


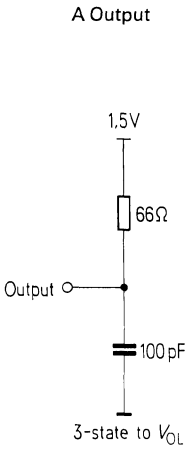
Output Delay vs. Capacitance

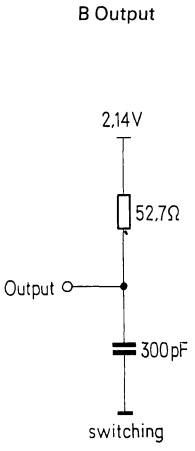




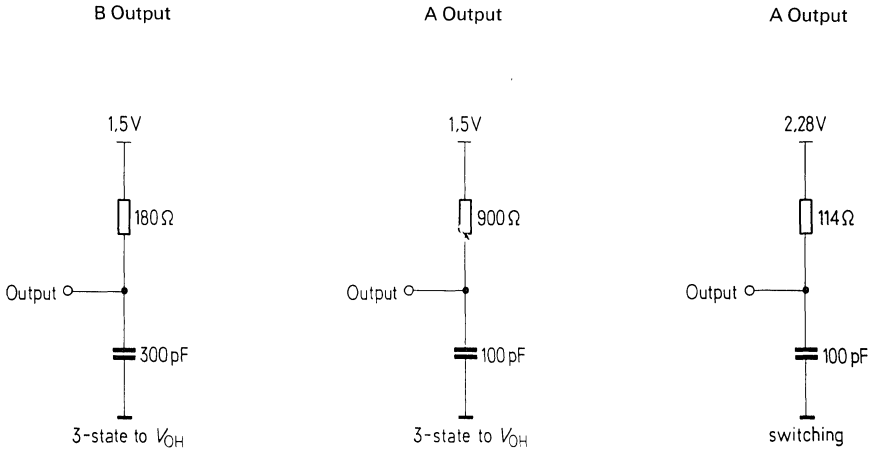
Output Test Load Circuit







Output Test Load Circuit

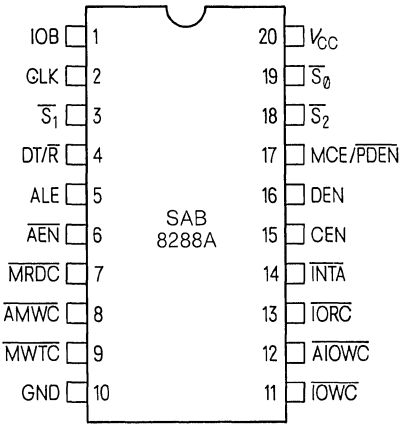


Preliminary

SAB 8288A Bus Controller for SAB 8086 Family Processors

- Fully compatible with SAB 8288
- 40% Less Power Supply Current than Standard SAB 8288
- Bipolar Drive Capability
- Provides Advanced Commands
- Provides Wide Flexibility in System Configurations
- 3-State Command Output Drivers
- Configurable for Use with an I/O Bus
- Facilitates Interface to One or Two Multi-Master Busses

Pin Configuration



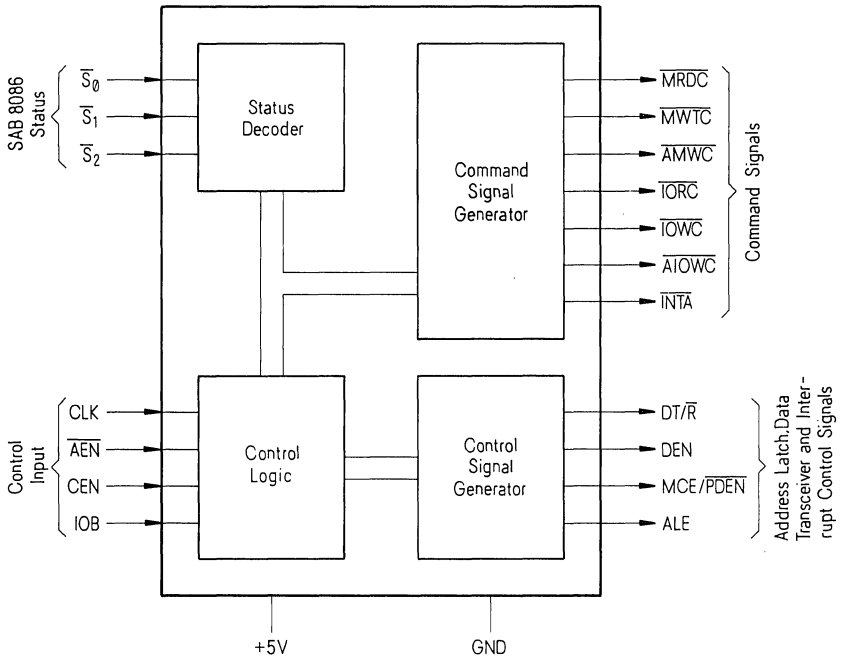
Pin Names

$\overline{S_0} - \overline{S_2}$	Status
CLK	Clock
ALE	Adress Latch Enable
DEN	Data Enable
DT/$\overline{R}$	Data Transmit/Receive
$\overline{AEN}$	Address Enable
CEN	Command Enable
IOB	Input/Output Bus Mode
$\overline{AIOWC}$	Advanced I/O Write
$\overline{IOWC}$	I/O Write
$\overline{IORC}$	I/O Read
$\overline{AMWC}$	Advanced Memory Write
$\overline{MWTC}$	Memory Write
$\overline{MRDC}$	Memory Read
$\overline{INTA}$	Interrupt Acknowledge
MCE/$\overline{PDEN}$	Master Cascade/Peripheral Data
V_{CC}	Power Supply (+5V)
GND	Ground (0V)

SAB 8288A Bus Controller is a 20-pin bipolar component for use with medium-to-large SAB 80186, SAB 80188, SAB 8086 and SAB 8088 processing systems. The bus controller provides command and control timing generation as well as bipolar bus drive capability while optimizing system performance.

A strapping option on the bus controller configures it for use with a multi-master system bus and separate I/O bus.
This device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

Block Diagram



Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
IOB	1	I	INPUT/OUTPUT BUS MODE – When the IOB is strapped HIGH the SAB 8288A functions in the I/O Bus mode. When it is strapped LOW, the SAB 8288A functions in the System Bus mode. (See sections on I/O Bus and Systems Bus modes).
CLK	2	I	CLOCK – This is a clock signal from the SAB 8284A or SAB 8284B clock generator and serves to establish when command and control signals are generated.
$\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$	3, 18, 19	I	STATUS INPUT PINS – These pins are the status input pins from the SAB 80186, SAB 80188, SAB 8086 or SAB 8088 processors. The SAB 8288A decodes these inputs to generate command and control signals at the appropriate time. When these pins are not in use (passive) they are all HIGH. (See chart under Functional Description).

Symbol	Number	Input (I) Output (O)	Function
DT/$\overline{R}$	4	O	DATA TRANSMIT/RECEIVE – This signal establishes the direction of data flow through the transceivers. A HIGH on this line indicates Transmit (write to I/O or memory) and a LOW indicates Receive (Read).
ALE	5	O	ADDRESS LATCH ENABLE – This signal serves to strobe an address into the address latches. This signal is active HIGH and latching occurs on the falling (HIGH to LOW) transition. ALE is intended for use with transparent D type latches.
$\overline{AEN}$	6	I	ADDRESS ENABLE – $\overline{AEN}$ enables command outputs of the SAB 8288A Bus Controller at least 105 ns after it becomes active (LOW). $\overline{AEN}$ going inactive immediately 3-states the command output drivers. $\overline{AEN}$ does not affect the I/O command lines if the SAB 8288A is in the I/O Bus mode (IOB tied HIGH).
$\overline{MRDC}$	7	O	MEMORY READ COMMAND – This command line instructs the memory to drive its data onto the data bus. This signal is active LOW.
$\overline{AMWC}$	8	O	ADVANCED MEMORY WRITE COMMAND – The $\overline{AMWC}$ issues a memory write command earlier in the machine cycle to give memory devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AMWC}$ is active LOW.
$\overline{MWTC}$	9	O	MEMORY WRITE COMMAND – This command line instructs the memory to record the data present on the data bus. This signal is active LOW.
$\overline{IOWC}$	11	O	I/O WRITE COMMAND – This command line instructs an I/O device to read the data on the data bus. This signal is active LOW.
$\overline{AIOWC}$	12	O	ADVANCED I/O WRITE COMMAND – The $\overline{AIOWC}$ issues an I/O Write Command earlier in the machine cycle to give I/O devices an early indication of a write instruction. Its timing is the same as a read command signal. $\overline{AIOWC}$ is active LOW.
$\overline{IORC}$	13	O	I/O READ COMMAND – This command line instructs an I/O device to drive its data onto the data bus. This signal is active LOW.
$\overline{INTA}$	14	O	INTERRUPT ACKNOWLEDGE – This command line tells an interrupting device that its interrupt has been acknowledged and that it should drive vectoring information onto the data bus. This signal is active LOW.
CEN	15	I	COMMAND ENABLE – When this signal is LOW all SAB 8288A command outputs and the DEN and $\overline{PDEN}$ control outputs are forced to their inactive state. When this signal is HIGH, these same outputs are enabled.
DEN	16	O	DATA ENABLE – This signal serves to enable data transceivers onto either the local or system data bus. This signal is active HIGH.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
MCE/$\overline{PDEN}$	17	O	This is a dual function pin: MCE (IOB is tied LOW) – **Master Cascade Enable** occurs during an interrupt sequence and serves to read a Cascade. Address from a master PIC (Priority Interrupt Controller) onto the data bus. The MCE signal is active HIGH. $\overline{PDEN}$ (IOB is tied HIGH) – **Peripheral Data Enable** enables the data bus transceiver for the I/O bus during I/O instructions. It performs the same function for the I/O bus that DEN performs for the system bus. $\overline{PDEN}$ is active LOW.
V_{CC}	20	–	Power Supply (+5V)
GND	10	–	Ground (0V)

Functional Description

The command logic decodes the three SAB 80186, SAB 80188, SAB 8086 or SAB 8088 CPU status lines ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) to determine what command is to be issued. This chart shows the meaning of each status "word".

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Processor State	SAB 8288A Command
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Code Access	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

The command is issued in one of two ways dependent on the mode of the SAB 8288A Bus Controller.

I/O Bus Mode – The SAB 8288A is in the I/O Bus mode if the IOB pin is strapped HIGH. In the I/O Bus mode all I/O command lines ($\overline{IORC}$, $\overline{IOWC}$, $\overline{AIOWC}$, $\overline{INTA}$) are always enabled (i.e., not dependent on $\overline{AEN}$). When an I/O command is initiated by the processor, the SAB 8288A immediately activates the command lines using $\overline{PDEN}$ and DT/$\overline{R}$ to control the I/O bus transceiver. The I/O command lines should not be used to control the system bus in this configuration because no arbitration is present. This mode allows one SAB 8288A Bus Controller to handle two external busses. No waiting is involved when the CPU wants to gain access to the I/O bus. Normal memory access requires a "Bus Ready" signal ($\overline{AEN}$ LOW) before it will proceed. It is advantageous to use the IOB mode if I/O or peripherals dedicated to one processor exist in a multi-processor system.

System Bus Mode – The SAB 8288A is in the System Bus mode if the IOB pin is strapped LOW. In this mode no command is issued until 115 ns after the $\overline{AEN}$ Line is activated (LOW). This mode assumes bus arbitration logic will inform the bus controller (on the $\overline{AEN}$ line) when the bus is free for use. Both memory and I/O commands wait for bus arbitration. This mode is used when only one bus exists. Here, both I/O and memory are shared by more than one processor.

Command Outputs

The advanced write commands are made available to initiate write procedures early in the machine cycle. This signal can be used to prevent the processor from entering an unnecessary wait state.

The command output are:
$\overline{MRDC}$ – Memory Read Command
$\overline{MWTC}$ – Memory Write Command
$\overline{IORC}$ – I/O Read Command
$\overline{IOWC}$ – I/O Write Command
$\overline{AMWC}$ – Advanced Memory Write Command
$\overline{AIOWC}$ – Advanced I/O Write Command
$\overline{INTA}$ – Interrupt Acknowledge

$\overline{INTA}$ (Interrupt Acknowledge) acts as an I/O read during an interrupt cycle. Its purpose is to inform an interrupting device that its interrupt is being acknowledged and that it should place vectoring information onto the data bus.

Control Outputs

The control outputs of the SAB 8288A are Data Enable (DEN), Data Transmit/Receive (DT/$\overline{R}$) and Master Cascade Enable/Peripheral Data Enable (MCE/$\overline{PDEN}$). The DEN signal determines when the external bus should be enable onto the local bus and the DT/$\overline{R}$ determines the direction of data transfer. These two signals usually go to the chip select and direction pins of a transceiver.

The MCE/$\overline{PDEN}$ pin changes function with the two modes of the SAB 8288A. When the SAB 8288A is in the IOB mode (IOB HIGH) the PDEN signal serves as a dedicated data enable signal for the I/O or Peripheral System bus.

Interrupt Acknowledge and MCE

The MCE signal is used during an interrupt acknowledge cycle if the SAB 8288A is in the System Bus mode (IOB LOW). During any interrupt sequence there are two interrupt acknowledge cycle no data or address transfers take place. Logic should be provided to mask off MCE during this cycle. Just before the second cycle begins the MCE signal gates a master Priority Interrupt Controller's (PIC) cascade address onto the processor's local bus where ALE (Address Latch Enable) strobes it into the address latches. On the leading edge of the second interrupt cycle the addressed slave PIC gates an interrupt vector onto the system data bus where it is read by the processor.

If the system contains only one PIC, the MCE signal is not used. In this case the second Interrupt Acknowledge signal gates the interrupt vector onto the processor bus.

Address Latch Enable and Halt

Address Latch Enable (ALE) occurs during each machine cycle and serves to strobe the current address into the address latches. ALE also serves to strobe the status ($\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$) into a latch for halt state decoding.

Command Enable

The Command Enable (CEN) input acts as a command qualifier for the SAB 8288A. If the CEN pin is high the SAB 8288A functions normally. If the CEN pin is pulled LOW, all command lines are held in their inactive state (not 3-state). This feature can be used to implement memory partitioning and to eliminate address conflicts between system bus devices and resident bus devices.

Absolute Maximum Ratings [1]

Temperature Under Bias	0 to +70°C
Storage Temperature	−65 to +150°C
All Output and Supply Voltages	−0.5 to +7 V
All Input Voltages	−1.0 to +5.5 V
Power Dissipation	1 W

D.C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5 V ±10%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
V_C	Input Clamp Voltage		−1	V	I_C = −5 mA
I_{CC}	Power Supply Current		140	mA	All outputs open
I_F	Forward Input Current	–	−0.7		V_F = 0.45 V
I_R	Reserve Input Current		50	µA	V_R = V_{CC}
V_{OL}	Output Low Voltage Command Outputs Control Outputs		 0.5 0.5	V	 I_{OL} = 32 mA I_{OL} = 16 mA
V_{OH}	Output High Voltage Command Outputs Control Outputs	 2.4 2.4	–		 I_{OH} = −5 mA I_{OH} = −1 mA
V_{IL}	Input Low Voltage	–	0.8		–
V_{IH}	Input High Voltage	2.0	–		
I_{OFF}	Output Off Current	–	100	µA	V_{OFF} = 0.4 to 5.25 V

A.C. Characteristics

T_A = 0 to 70°C; V_{CC} = +5 V ±10%

Timing Requirements

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
t_{CLCL}	CLK Cycle Period	100			
t_{CLCH}	CLK Low Time	50			
t_{CHCL}	CLK High Time	30			
t_{SVCH}	Status Active Setup Time	35	–	ns	–
t_{CHSV}	Status Active Hold Time	10			
t_{SHCL}	Status Inactive Setup Time	35			
t_{CLSH}	Status Inactive Hold Time	10			
t_{ILIH}	Input, Rise Time	–	20		From 0.8V to 2.0V
t_{IHIL}	Input, Fall Time		12		From 2.0V to 0.8V

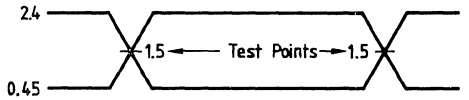
1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Timing Responses

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
t_{CVNV}	Control Active Delay	5	45	ns	
t_{CVNX}	Control Inactive Delay	10			
t_{CLLH}, t_{CLMCH}	ALE MCE Active Delay (from CLK)	–	20		
t_{SVLH}, t_{SVMCH}	ALE MCE Active Delay (from Status)				
t_{CHLL}	AIE Inactive Delay	4	15		$\overline{MRDC}$, $\overline{IORC}$, $\overline{MWTC}$, $\overline{IOWC}$, $\overline{INTA}$, $\overline{AMWC}$, $\overline{AIOWC}$: I_{OL} = 32 mA, I_{OH} = −5 mA, C_L = 300 pF
t_{CLML}	Command Active Delay	10	35		
t_{CLMH}	Command Inactive Delay				
t_{CHDTL}	Direction Control Active Delay	–	50		
t_{CHDTH}	Direction Control Inactive Delay		30		
t_{AELCH}	Command Enable Time		40		Other: I_{OL} = 16 mA, I_{OH} = −1 mA, C_L = 80 pF
t_{AEHCZ}	Command Disable Time				
t_{AELCV}	Enable Delay Time	115	200		
t_{AEVNV}	$\overline{AEN}$ to DEN	–	20		
t_{CEVNV}	CEN to DEN, PDEN		25		
t_{CELRH}	CEN to Command		t_{CLML}		
t_{OLOH}	Output, Rise Time		20		From 0.8V to 2.0V
t_{OHOL}	Output, Fall Time		12		From 2.0V to 0.8V

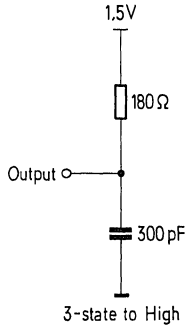
A.C. Testing Input, Output Waveform

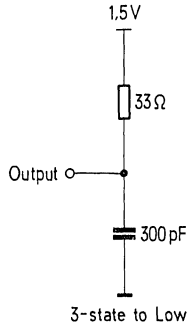
Input/Output



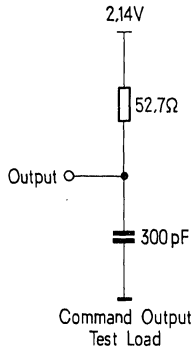
A.C. Testing Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0". The clock is driven at 4.3V and 0.25V timing measurements are made at 1.5V for both a logic "1" and "0"

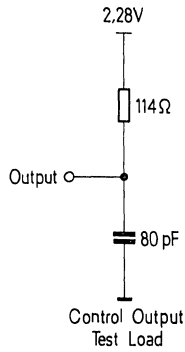
Test Load Circuits – 3-State Command Output Test Load





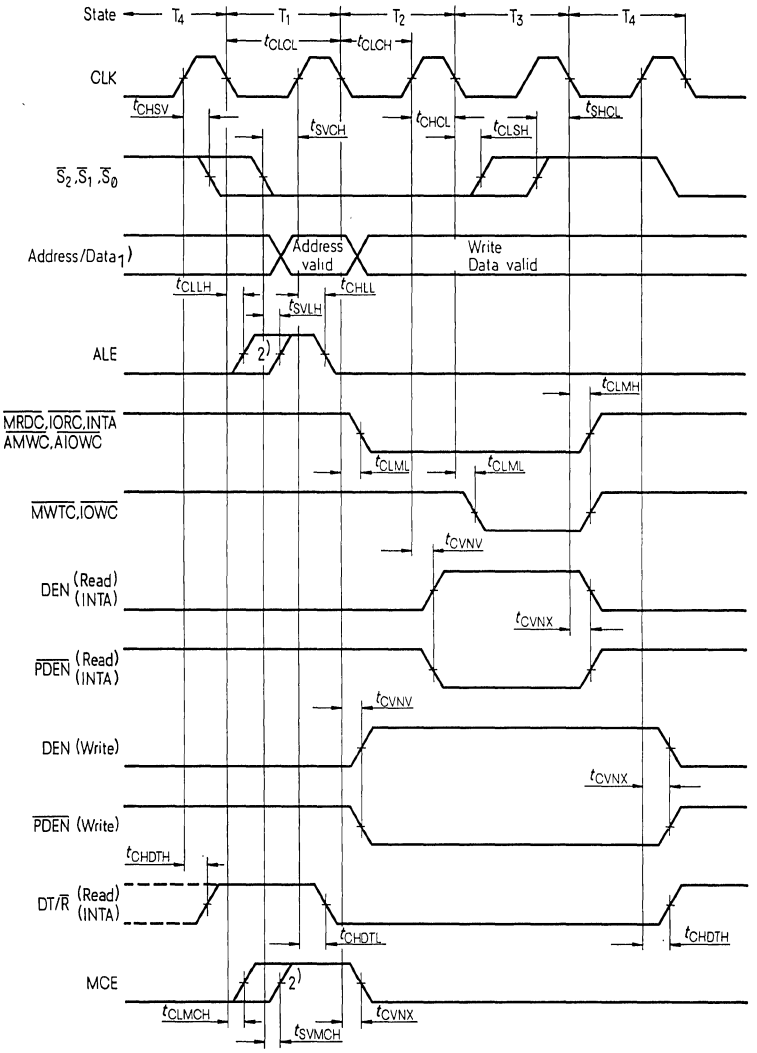
Test Load Circuits – 3-State Command Output Test Load





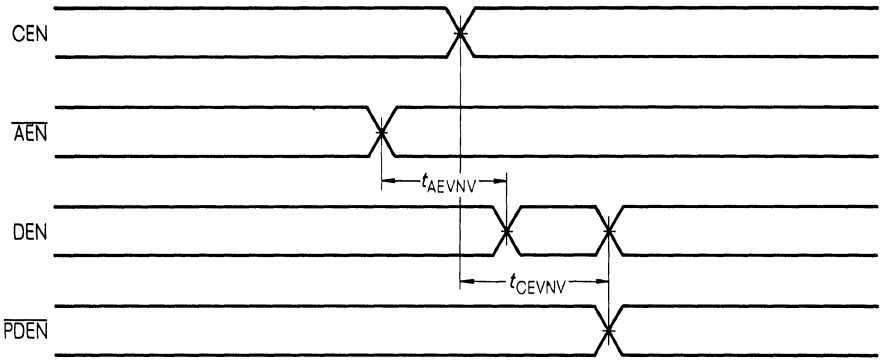
Waveforms

Timing Diagram

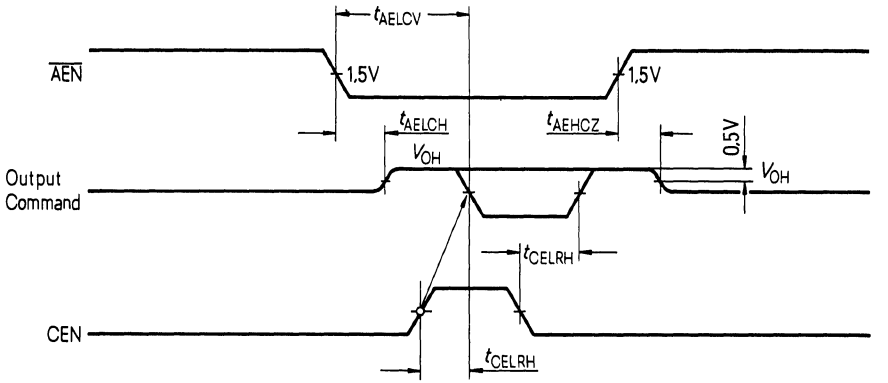


1) Address/Data Bus is shown only for reference purposes
2) Leading edge of ALE and MCE is determined by the falling edge of CLK or status going active, whichever occurs last.
3) All timing measurements are made at 1.5V unless specified otherwise.

DEN, PDEN Qualification Timing



Address Enable (AEN) Timing (3-State Enable/Disable)



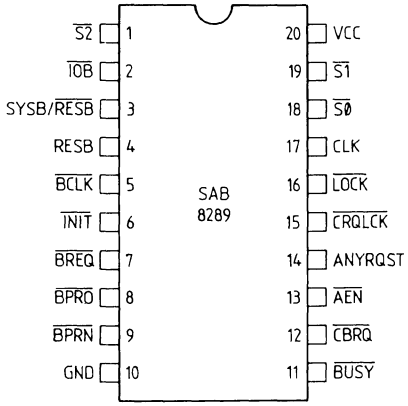
CEN must be low or valid prior to T2 to prevent the command from being generated.

SAB 8289
Bus Arbiter

SAB 8289 8 MHz
SAB 8289-1 10 MHz

- Provides Multi-Master System Bus Protocol
- Synchronizes SAB 8086/SAB 8088 Processors with Multi-Master Bus
- Provides Simple Interface with SAB 8288 Bus Controller
- Four Operating Modes for Flexible System Configuration
- Compatible with Intel Bus Standard MULTIBUS™ (MULTIBUS is a trademark of INTEL Corporation USA)
- Provides System Bus Arbitration for SAB 8089 IOP in Remote Mode

Pin Configuration



Pin Names

S0-2	Status
IOB	I/O Bus Present
SYSB/RESB	System/Resident Bus
RESB	Resident Bus Present
BCLK	Bus Clock
INIT	Initialisation
BREQ	Bus Request
BPRO	Bus Priority Out
BPRN	Bus Priority In
CLK	System Clock
AEN	Address Enable
ANYRQST	Any Request
CRQLCK	Common Request Lock
CBRQ	Common Bus Request
LOCK	Bus Lock
VCC	+5 V
GND	Ground (0V)

The SAB 8289 Bus Arbiter is a 20-pin, 5-volt-only bipolar component for use with medium to large SAB 8086/SAB 8088 multi-master/multiprocessing systems. The SAB 8289 provides system bus arbitration for systems with multiple bus masters, such as an SAB 8086 CPU with SAB 8089 IOP in its REMOTE mode, while providing bipolar buffering and drive capability.

Pin Definitions and Functions

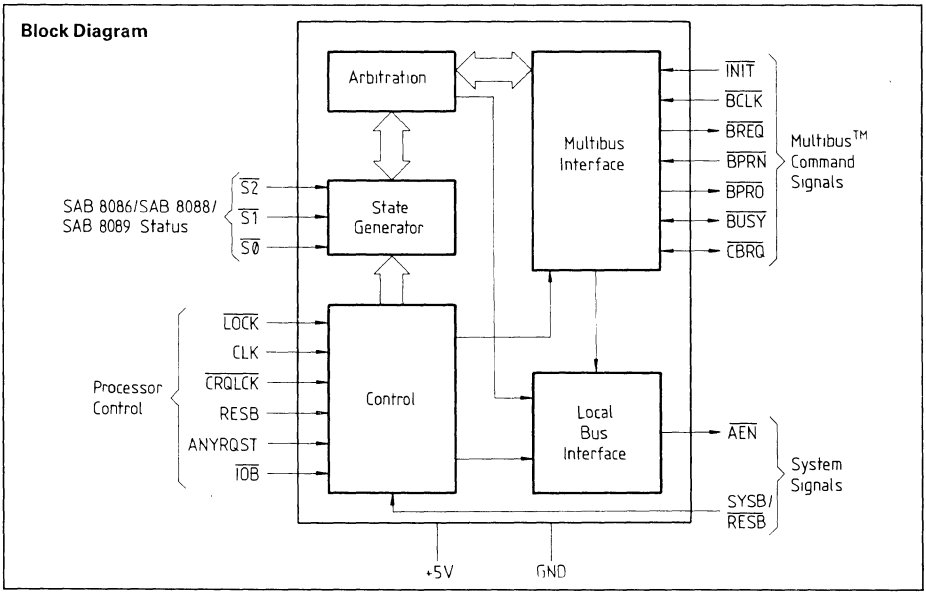
Symbol	Number	Input (I) Output (O)	Function
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	1, 18, 19	I	**Status Input Pins** These pins are the status input pins from a SAB 8086, SAB 8088 or SAB 8089 processor. The SAB 8289 decodes these pins to initiate bus request and surrender actions.
CLK	17	I	**Clock** This is the clock from the SAB 8284A clock chip and serves to establish when bus arbiter actions are initiated.
$\overline{LOCK}$	16	I	**Lock** $\overline{LOCK}$ is a processor generated signal which when activated (low) serves to prevent the arbiter from surrendering the multi-master system bus to any other bus arbiter, regardless of its priority.
$\overline{CRQLCK}$	15	I	**Common Request Lock** $\overline{CRQLCK}$ is an active low signal which serves to prevent the arbiter from surrendering the multi-master system bus to any other bus arbiter requesting the bus through the $\overline{CBRQ}$ input pin.
RESB	4	I	**Resident Bus** RESB is a strapping option to configure the arbiter to operate in systems having both a multi-master system bus and a Resident Bus. When it is strapped high the multi-master system bus is requested or surrendered as a function of the SYSB/$\overline{RESB}$ input pin. When it is strapped low the SYSB/$\overline{RESB}$ input is ignored.
ANYRQST	14	I	**Any Request** ANYRQST is a strapping option which permits the multimaster system bus to be surrendered to a lower priority arbiter as though it were an arbiter of higher priority (i.e., when a lower priority arbiter requests the use of the multi-master system bus, the bus is surrendered as soon as it is possible). Strapping $\overline{CBRQ}$ low and ANYRQST high forces the SAB 8289 arbiter to surrender the multi-master system bus after each transfer cycle. Note that when surrender occurs $\overline{BREQ}$ is driven false (high).
$\overline{IOB}$	2	I	**IO Bus** $\overline{IOB}$ is a strapping option which configures the SAB 8289 Arbiter to operate in systems having both an IO Bus (Peripheral Bus) and a multimaster system bus. The arbiter requests and surrenders the use of the multimaster system bus as a function of the status line, $\overline{S2}$. The multi-master system bus is permitted to be surrendered while the processor is performing IO commands and is requested whenever the processor performs a memory command. Interrupt cycles are assumed as coming from the peripheral bus and are treated as would be an IO command.
$\overline{AEN}$	13	O	**Address Enable** $\overline{AEN}$ is the output of the SAB 8289 Arbiter to the processor's address latches, to the SAB 8288 Bus Controller and SAB 8284A Clock Generator. $\overline{AEN}$ serves to instruct the Bus Controller and address latches when to tri-state their output drivers.

Symbol	Number	Input (I) Output (O)	Function
SYSB/$\overline{\text{RESB}}$	3	I	**System Bus/Resident Bus** SYSB/$\overline{\text{RESB}}$ is an input signal when the arbiter is configured in the S.R. Mode (RESB is strapped high) which serves to determine when the multimaster system bus is requested and when the multi-master system bus surrendering is permitted. The signal is intended to originate from some form of address mapping circuitry such as a decoder or PROM attached to the resident address bus. Signal transitions and glitches are permitted on this pin from Ø1 of T4 to Ø1 to T2 of the processor cycle. During the period from Ø1 of T2 to Ø1 of T4 only clean transitions are permitted on this pin (no glitches). If a glitch does occur the arbiter may capture or miss it, and the multi-master system bus may be requested or surrendered, depending upon the state of the glitch. The arbiter requests the multi-master system bus in the S.R. Mode when the state of the SYSB/$\overline{\text{RESB}}$ pin is high and permits the bus to be surrendered when this pin is low.
$\overline{\text{CBRQ}}$	12	I/O	**Common Bus Request** $\overline{\text{CBRQ}}$ is an input signal which serves to instruct the arbiter if there are any other arbiters of lower priority requesting the use of the multi-master system bus. The $\overline{\text{CBRQ}}$ pins (open-collector output) of all the SAB 8289 Bus Arbiters which are to surrender the multi-master-system bus upon request are connected together. The Bus Arbiter running the current transfer cycle will not itself pull the $\overline{\text{CBRQ}}$ line low. Any other arbiter connected to the $\overline{\text{CBRQ}}$ line can request the multi-master system bus. The arbiter presently running the current transfer cycle drops its $\overline{\text{BREQ}}$ signal and surrenders the bus whenever the proper surrender conditions exist. Strapping $\overline{\text{CBREQ}}$ low and ANYRQST – high allows the multi-master system bus to be surrendered after each transfer cycle. See the pin definition of ANYRQST.
$\overline{\text{INIT}}$	6	I	**Initialize** $\overline{\text{INIT}}$ is an active low multimaster system bus input signal which is used to reset all the bus arbiters on the multi-master system bus. After initialization, no arbiters have the use of the multi-master system bus.
$\overline{\text{BCLK}}$	5	I	**Bus Clock** $\overline{\text{BCLK}}$ is the multi-master system bus clock to which all multimaster system bus interface signals are synchronized.
$\overline{\text{BREQ}}$	7	0	**Bus Request** $\overline{\text{BREQ}}$ is an active low output signal in the parallel Priority Resolving Scheme which the arbiter activates to request the use of the multi-master system bus.
$\overline{\text{BPRN}}$	9	I	**Bus Priority In** $\overline{\text{BPRN}}$ is the active low signal returned to the arbiter to instruct it that it may acquire the multimaster system bus on the next falling edge of BCLK. $\overline{\text{BPRN}}$ indicates to the arbiter that it is the highest priority requesting arbiter presently on the bus. The loss of $\overline{\text{BPRN}}$ instructs the arbiter that it has loss priority to a higher priority arbiter.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
$\overline{\text{BPRO}}$	8	O	**Bus Priority Out** $\overline{\text{BPRO}}$ is an active low output signal which is used in the serial priority resolving scheme where $\overline{\text{BPRO}}$ is daisy chained to $\overline{\text{BPRN}}$ of the next lower priority arbiter.
$\overline{\text{BUSY}}$	11	I/O	**Busy** $\overline{\text{BUSY}}$ is an active low open collector multi-master system bus interface signal which is used to instruct all the arbiters on the bus when the multi-master system bus is available. When the multi-master system bus is available the highest requesting arbiter (determined by $\overline{\text{BPRN}}$) seizes the bus and pulls $\overline{\text{BUSY}}$ low to keep other arbiters off of the bus. When the arbiter is done with the bus it releases the $\overline{\text{BUSY}}$ signal permitting it to go high and thereby allowing another arbiter to acquire the multi-master system bus.
VCC	20	I	**Power Supply** (+5 V ± 10%)
GND	10	I	**Ground** (0V)

Block Diagram



Functional Description

The SAB 8289 Bus Arbiter operates in conjunction with the SAB 8288 Bus Controller to interface SAB 8086/SAB 8088/ SAB 8089 processors to a multi-master system bus (both the SAB 8086 and the SAB 8088 are configured in their max mode). The processor is unaware of the arbiter's existence and issues commands as though it has exclusive use of the system bus. If the processor does not have the use of the multi-master system bus, the arbiter prevents the Bus Controller (SAB 8288), the data transceivers and the address latches from accessing the system bus (e.g. all bus driver outputs are forced into the high impedance state). Since the command sequence was not issued by the SAB 8288, the system bus will appear as "Not Ready" and the processor will enter wait states. The processor will remain in Wait until the Bus Arbiter acquires the use of the multi-master system bus whereupon the arbiter will allow the bus controller, the data transceivers, and the address latches to access the system. Typically, once the command has been issued and a data transfer has taken place, a transfer acknowledge (XACK) is returned to the processor to indicate "READY" from the accessed slave device. The processor then completes its transfer cycle. Thus the arbiter serves to multiplex a processor (or bus master) onto a multi-master system bus and avoid contention problems between bus masters.

Arbitration between Bus Masters

In general, higher priority masters obtain the bus when a lower priority master completes its present transfer cycle. Lower priority bus masters obtain the bus when a higher priority master is not accessing the system bus. A strapping option (ANYRQST) is provided to allow the arbiter to surrender the bus to a lower priority master as though it were a master of higher priority. If there are no other bus masters requesting the bus, the arbiter maintains the bus so long as its processor has not entered the HALT State. The arbiter will not voluntarily surrender the system bus and has to be forced off by another master's bus request, the HALT State being the only exception. Additional strapping options permit other modes of operation wherein the multimaster system bus is surrendered or requested under different sets of conditions.

Modes of Operation

There are two types of processors in the SAB 8086 family. An Input/Output processor (the SAB 8089 IOP) and the SAB 8086/SAB 8088 CPUs. Consequently, there are two basic operating modes in the SAB 8289 bus arbiter. One, the $\overline{IOB}$ (I/O Peripheral Bus) mode, permits the processor access to both an I/O Peripheral Bus and a multi-master system bus. The second, the RESB (Resident Bus mode), permits the processor to communicate over both a Resident Bus and a multi-master system bus. An I/O Peripheral Bus is a bus where all devices on that bus, including memory, are treated as I/O devices and are addressed by I/O commands. All memory commands are directed to another bus, the multi-master system bus. A Resident Bus can issue both memory and I/O commands, but it is a distinct and separate bus from the multi-master system bus. The distinction is that the Resident Bus has only one master, providing full availability and being dedicated to that one master.

The $\overline{IOB}$ strapping option configures the SAB 8289 Bus Arbiter into the $\overline{IOB}$ mode and the strapping option RESB configures it into the RESB mode. It might be noted at this point that if both strapping options are strapped false, the arbiter interfaces the processor to a multi-master system bus only. With both options strapped true, the arbiter interfaces the processor to a multi-master system bus, a Resident Bus, and an I/O Bus.

In the $\overline{IOB}$ mode, the processor communicates and controls a host of peripherals over the Peripheral Bus. When the I/O Processor needs to communicate with system memory, it does so over the system memory bus.

The SAB 8086 and SAB 8088 processor can communicate with a Resident Bus and a multi-master system bus. Two bus controllers and only one Bus Arbiter would be needed in such a configuration. In such a system configuration the processor would have access to memory and peripheral of both busses. Memory mapping techniques are applied to select which bus is to be accessed. The SYSB/$\overline{RESB}$ input on the arbiter serves to instruct the arbiter as to whether or not the system bus is to be accessed. The signal connected to SYSB/$\overline{RESB}$ also enables or disables commands from one of the bus controllers.

Summary of SAB 8289 Modes, Requesting and Relinquisting the Multi-master system bus

	Status Lines From SAB 8086 / 88 / 89			IOB Mode Only	RESB (Mode) Only IOB=High RESB=High		IOB Mode RESB Mode IOB=Low RESB=High		Single Bus Mode IOB=High RESB=Low
	$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	IOB=Low	SYSB/$\overline{RESB}$ =High	SYSB/$\overline{RESB}$ =Low	SYSB/$\overline{RESB}$ =High	SYSB/$\overline{RESB}$ =Low	
I/O	0	0	0	x		x	x	x	
COMMANDS	0	0	1	x		x	x	x	
	0	1	0	x		x	x	x	
HALT	0	1	1	x	x	x	x	x	x
MEM	1	0	0			x		x	
COMMANDS	1	0	1			x		x	
	1	1	0			x		x	
IDLE	1	1	1	x	x	x	x	x	x

NOTE:
x = Multi-Master System Bus is allowed to be Surrendered.

Mode	Pin Strapping	Multi-Master System Bus	
		Requested**	Surrendered*
Single Bus Multi-Master Mode	$\overline{IOB}$=High RESB=Low	Whenever the processor's status lines go active	HLT+TI•CBRQ+HPBRQ***
RESB Mode Only	$\overline{IOB}$=High RESB=High	SYSB/$\overline{RESB}$=High• ACTIVE STATUS	(SYSB/$\overline{RESB}$=Low+TI)• CRBQ+HLT+HPBRQ
IOB Mode Only	IOB=Low RESB=Low	Memory Commands	(I/O Status+TI)•CBRQ+ HLT+HPBRQ
IOB Mode•RESB Mode	$\overline{IOB}$=Low RESB=High	(Memory Command)• (SYSB/$\overline{RESB}$=High)	((I/O Status Commands)+ SYSB/RESB=LOW))•CBRQ +HPBRQ***+HLT

NOTES:
*$\overline{LOCK}$ prevents surrender of Bus to any other arbiter, $\overline{CRQLCK}$ prevents surrender of Bus to any lower priority arbiter.
**Except for HALT and Passive or IDLE Status.
***HPBRQ, Higher priority Bus request or $\overline{BPRN}$=1.
1. $\overline{IOB}$ Active Low.
2. RESB Active High.
3. +is read as "OR" and•as "AND".
4. TI=Processor Idle Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$=111
5. HLT=Processor Halt Status $\overline{S2}$, $\overline{S1}$, $\overline{S0}$=011

Absolute Maximum Ratings*

Ambient Temperature Under Bias	0 to 70°C
Storage Temperature	–65 to 150°C
All Output and Supply Voltages	–0.5 to 7 V
All Input Voltages	–1.0 to 5.5 V
Power Dissipation	1.5 Watt

D.C. Characteristics

T_A = 0 to 70°C, V_{CC} = 5 V ± 10%

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
V_C	Input Clamp Voltage	–	–1.0	V	V_{CC}=4.5 V, I_C=–5 mA
I_F	Input Forward Current		–0.5	mA	V_{CC}=5.5 V, V_F=0.45 V
I_R	Reverse Input Leakage Current		60	µA	V_{CC}=5.5 V, V_R=5.5 V
V_{OL}	Output Low Voltage $\overline{BUSY}$, $\overline{CBRQ}$ $\overline{AEN}$ $\overline{BPRO}$, $\overline{BREQ}$		0.45	V	 I_{OL}=20 mA I_{OL}=16 mA I_{OL}=10 mA
V_{OH}	Output High Voltage $\overline{BUSY}$, $\overline{CBRQ}$	Open Collector			–
	All Other Outputs	2.4	–	V	I_{OH}=400 µA
I_{CC}	Power Supply Current	–	165	mA	–
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0	–		
C_{in} Status	Input Capacitance	–	25	pF	
C_{in} (Others)	Input Capacitance		12		

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended perods may affect device reliability.

A.C. Characteristics

T_A=0 to 70°C, V_{CC}=5 V ± 10%

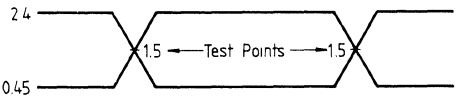
Timing Requirements

Symbol	Parameter	Limit Values				Unit	Test Condition
		SAB 8289		SAB 8289-1			
		Min.	Max.	Min.	Max.		
TCLCL	CLK Cycle Period	125		100			
TCLCH	CLK Low Time	65	–	53	–		
TCHCL	CLK High Time	35		35			
TSVCH	Status Active-Setup	65		55			
TSHCL	Status Inactive-Setup	50	TCLCL-10	45	TCLCL-10		
THVCH	Status Active Hold	10		10			
THVCL	Status Inactive Hold						
TBYSBL	Busy↑↓Setup to BCLK↓	20	–	20	–		–
TCBSBL	CBRQ↑↓Setup to BCLK↓					ns	
TBLBL	BCLK Cycle Time	100		100			
TBHCL	BCLK High Time	30	0.65 [TBLBL]	30	0.65 [TBLBL]		
TCLLL1	LOCK Inactive Hold	10		10			
TCLLL2	LOCK Active Setup	40		40			
TPNBL	BPRN↓↑ to BCLK Setup Time	15	–	15	–		
TCLSR1	SYSB/RESB Setup	0		0			
TCLSR2	SYSB/RESB Hold	20		20			
TNIH	Initialization Pulse Width	3TBLBL+ 3TCLCL		3TBLBL+ 3TCLCL			
TILIH	Input Rise Time	–	20	–	20		From 0.8 to 2.0 V
TIHIL	Input Fall Time		12		12		From 2.0 to 0.8 V

↑↓ Denotes the spec applies to both transitions of the signal.

A.C. Testing Input/Output Waveform

Input/Output



A.C. Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". The clock is driven at 4.3 V and 0.25 V. Timing measurements are made at 1.5 V for both a logic "1" and "0".

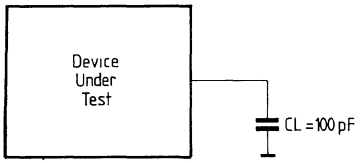
Timing Responses

Symbol	Parameter	Limit Values		Unit	Test Condition
		Min.	Max.		
TBLBRL	BCLK to BREQ Delay↓↑	–	35	–	–
TBLPOH	BCLK to BPRO↓↑[1]		40		
TPNPO	BPRN↓↑ to BPRO↓↑ Delay[1]		25		
TBLBYL	BCLK to BUSY Low		60		
TBLBYH	BCLK to BUSY Float[2]		35		
TCLAEH	CLK to AEN High		65	ns	
TBLAEL	BCLK to AEN Low		40		
TBLCBL	BCLK to CBRQ Low		60		
TBLCRH	BCLK to CBRQ Float[2]		35		
TOLOH	Output Rise Time		20		From 0.8 to 2.0 V
TOHOL	Output Fall Time		12		From 2.0 to 0.8 V

↓↑ Denotes the spec applies to both transitions of the signal.

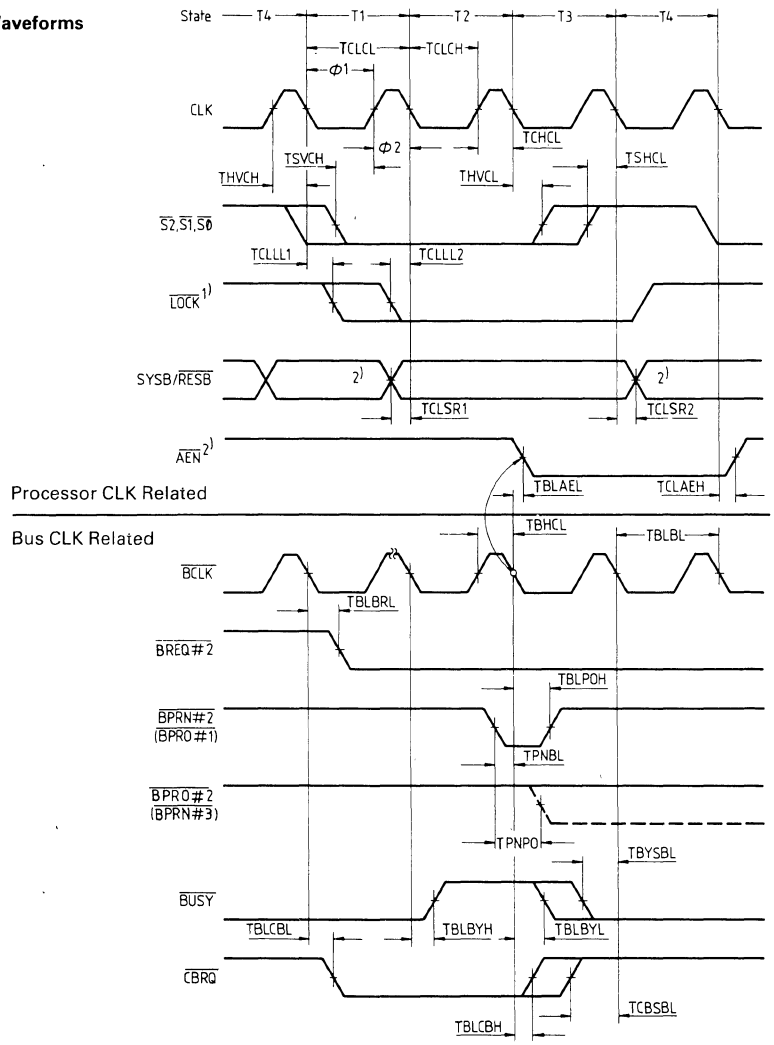
NOTES:
[1] BCLK generates the first BPRO wherein subsequent BPRO changes lower in the chain are generated through BPRON.
[2] Measured at 0.5 V above GND.

A.C. Testing Load Circuit



*C*L = 100 pF
*C*L Includes jig capacitance

Waveforms



NOTES:

1. LOCK active can occur during any state, as long as the relationships shown above with respect to the CLK are maintained.
   LOCK inactive has not critical time and can be asynchronous.
   CRQLCK has no critical timing and is considered an asynchronous input signal.
2. Glitching of SYSB/RESB pin is permitted during this time. After I 2 of T1, and before I 1 of T4, SYSB/RESB should be stable.
3. AEN leading edge is related to BCLK, trailing edge to CLK. The trailing edge of AEN occurs after bus priority is lost.

Additional Notes:
The signals related to CLK are typical processor signals, and do not relate to the depicted sequence of events of the signals referenced to $\overline{BCLK}$. The signals shown related to the $\overline{BCLK}$ represent a hypothetical sequence of events for illustration. Assume 3 bus arbiters of priorities 1, 2 and 3 configured in serial priority resolving scheme as shown in Figure 6. Assume arbiter has the bus and is holding busy low. Arbiter #2 detects its processor wants the bus and pulls low $\overline{BREQ\#2}$. If $\overline{BPRN\#2}$ is high (as shown), arbiter #2 will pull low $\overline{CBRQ}$ line. $\overline{CBRQ}$ signals to the higher priority arbiter #1 that a lower priority arbiter wants the bus. [A higher priority arbiter would be granted BPRN when it makes the bus request rather than having to wait for another arbiter to release the bus through $\overline{CBRQ}$].** Arbiter #1 will relinquish the multi-master system bus when it enters a state not requiring it (see Table 1), by lowering its $\overline{BPRO\#1}$ (tied to $\overline{BPRN\#2}$) and releasing BUSY. Arbiter #2 now sees that it has priority from $\overline{BPRN\#2}$ being low and releases CBRQ. As soon as BUSY signifies the bus is available (high), arbiter #2 pulls BUSY low on next falling edge of BCLK. Note that if arbiter #2 didn't want the bus at the time it received priority, it would pass priority to the next lower priority arbiter by lowering its $\overline{BPRO\#2}$ [TPNPO].

**Note that even a higher priority arbiter which is acquiring the bus through $\overline{BPRN}$ will momentarily drop $\overline{CBRQ}$ until it has acquired the bus.

Advance Information

SAB 82258
ADMA-Advanced DMA Controller for 16 bit Microcomputer Systems

- 16 bit DMA Controller for 16 bit Family Processors
  SAB 80286
  SAB 8086/88
  SAB 80186/188
- 4 Independent Channels
- 16 Mbyte Addressing Range
- 16 Mbyte Byte Count
- Memory Based Communication with CPU
- "On-the-Fly" Compare, Translate and Verify Operations
- Transfer Rates up to 8 Mbyte/sec
- Single and Double Cycle Transfer
- Automatic Chaining of Command Blocks
- Automatic Chaining of Data Blocks
- Multiplexor Mode Operation with 32 Subchannels
- Local and Remote (Stand Alone) Mode of Operation

Figure 1
Pin Configuration (Pad View, 286 mode)

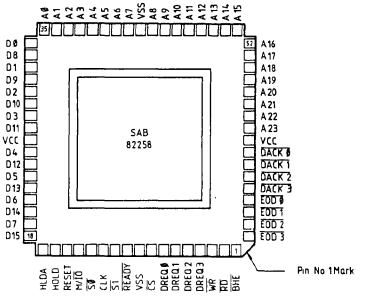
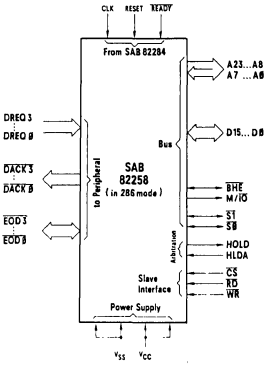


Figure 2
Function Symbol



SAB 82258 is an advanced DMA (Direct Memory Access) Controller designed especially for the 16 bit microprocessors SAB 80286 and SAB 8086/186/88/188. In addition, the operation with other processors is supported by the remote mode. It has 4 independent DMA channels which can transfer data at rates up to 8 Mbytes/second at 8 MHz clock in a SAB 80286 system or up to 4 Mbytes/second at 8 MHz in a 8086/80186 system. This great bandwidth allows the user to handle very fast data transfer or a large number of concurrent peripherals. The device is fabricated in advanced +5 Volt N-channel Siemens MYMOS technology and packaged in a 68 pin package.

Modes of Operation, Adaptive Bus Interface

SAB 82258 has been defined to work with all 16 bit processors, i.e. SAB 80286, SAB 80186/188 and SAB 8086/88 without additional support and interface logic. Hence the local busses of above processors are different in signals, functions and timings, SAB 82258 has an adaptive bus interface to meet the different requirements of these local busses.

Figure 3
Function Symbol in 186 Mode

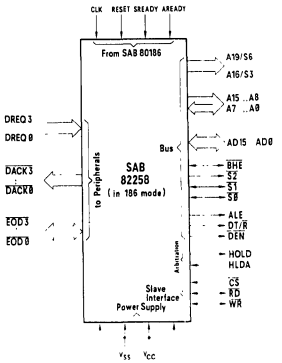
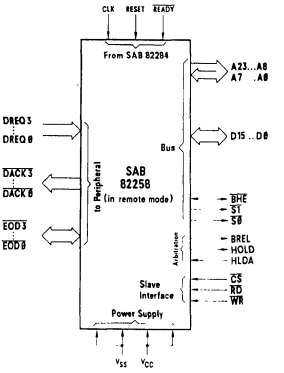
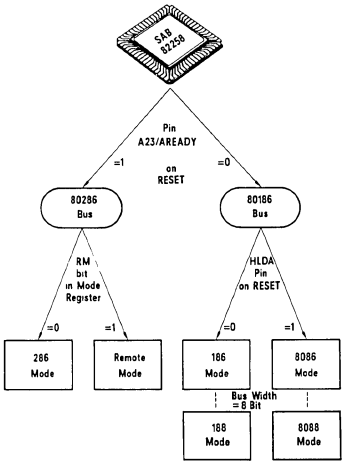


Figure 4
Function Symbol in Remote Mode



As a result of this, a bus compatibility with identical timing is attained with processors SAB 80286, SAB 80186 and SAB 8086. A compatibility with the 8 bit bus versions of these processors SAB 8088 and SAB 80188 is also guaranteed by defining the physical bus width of SAB 82258 (per software) as 8 bits. The only difference in operation with SAB 8086 or SAB 80186 is that for SAB 8086 the HOLD pin functions as $\overline{RQ}/\overline{GT}$ line (if HLDA is held high on RESET).

Figure 5
Mode Selection



SAB 82258 can also operate in a remote or stand alone mode where it is not coupled directly to a processor. Figure 5 shows the way how SAB 82258 detects with which processor or in which mode it is operating. Figure 2 shows the logic pinning in the 286 mode – for operation with SAB 80286. Figure 3 shows the logic pinning in the 186 mode – for operation with SAB 80186/188 and SAB 8086/88, and Figure 4 shows the pinning when SAB 82258 is in the remote mode and not directly coupled to a processor.

Pin Definitions and Functions

The pins of SAB 82258 have different meaning for each of the 4 modes of bus operation. The pinning in 286 mode and remote mode as well as 186 and 8086 mode are very similar. Table 1 summarizes the pinning of SAB 82258 in the various modes, the following sections give a detailed description of the pin function in each of the modes.

Table 1 Pin Name and Function

Pin No.	286 mode		Remote mode		186/8086 mode	
	Designation	Input/ Output	Designation	Input/ Output	Designation	Input/ Output
16	HOLD	O	HOLD	O	HOLD or $\overline{RQ}/\overline{GT}$	O (186) I/O (8086)
17	HLDA	I	HLDA	I	HLDA	I
1	$\overline{BHE}$	I/O	$\overline{BHE}$	I/O	$\overline{BHE}$	I/O
14	M/$\overline{IO}$	O	BREL	O	$\overline{S2}$	O
11	$\overline{S1}$	I/O	$\overline{S1}$	O	$\overline{S1}$	I/O
13	$\overline{S0}$	I/O	$\overline{S0}$	O	$\overline{S0}$	I/O
8	$\overline{CS}$	I	$\overline{CS}$	I	$\overline{CS}$	I
2	$\overline{RD}$	I	$\overline{RD}$	I	$\overline{RD}$	I/O
3	$\overline{WR}$	I	$\overline{WR}$	I	$\overline{WR}$	I/O
10	$\overline{READY}$	I	$\overline{READY}$	I	SREADY	I
59	A23	O	A23	O	AREADY	I
58	A22	O	A22	O	ALE	O
57	A21	O	A21	O	DT/$\overline{R}$	O
56	A20	O	A20	O	$\overline{DEN}$	O
55	A19	O	A19	O	A19/S6	O
54	A18	O	A18	O	A18/S5	O
53	A17	O	A17	O	A17/S4	O
52	A16	O	A16	O	A16/S3	O
51	A15	O	A15	O	A15	O
50	A14	O	A14	O	A14	O
49	A13	O	A13	O	A13	O
48	A12	O	A12	O	A12	O
47	A11	O	A11	O	A11	O
46	A10	O	A10	O	A10	O
45	A9	O	A9	O	A9	O
44	A8	O	A8	O	A8	O
42	A7	I/O	A7	I/O	A7	I/O
41	A6	I/O	A6	I/O	A6	I/O
40	A5	I/O	A5	I/O	A5	I/O
39	A4	I/O	A4	I/O	A4	I/O
38	A3	I/O	A3	I/O	A3	I/O
37	A2	I/O	A2	I/O	A2	I/O
36	A1	I/O	A1	I/O	A1	I/O
35	A0	I/O	A0	I/O	A0	I/O

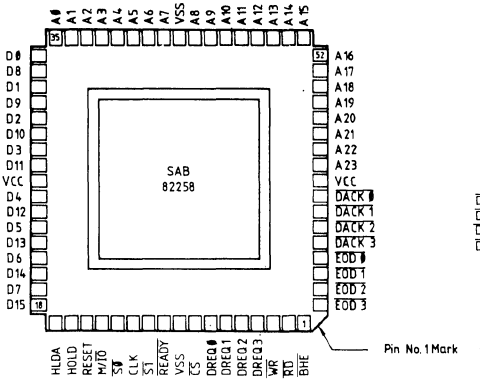
Pin No.	286 mode		Remote mode		186/8086 mode	
	Designation	Input/ Output	Designation	Input/ Output	Designation	Input/ Output
18	D15	I/O	D15	I/O	AD15	I/O
20	D14	I/O	D14	I/O	AD14	I/O
22	D13	I/O	D13	I/O	AD13	I/O
24	D12	I/O	D12	I/O	AD12	I/O
27	D11	I/O	D11	I/O	AD11	I/O
29	D10	I/O	D10	I/O	AD10	I/O
31	D9	I/O	D9	I/O	AD9	I/O
33	D8	I/O	D8	I/O	AD8	I/O
19	D7	I/O	D7	I/O	AD7	I/O
21	D6	I/O	D6	I/O	AD6	I/O
23	D5	I/O	D5	I/O	AD5	I/O
25	D4	I/O	D4	I/O	AD4	I/O
28	D3	I/O	D3	I/O	AD3	I/O
30	D2	I/O	D2	I/O	AD2	I/O
32	D1	I/O	D1	I/O	AD1	I/O
34	D0	I/O	D0	I/O	AD0	I/O
7	DREQ0	I	DREQ0	I	DREQ0	I
6	DREQ1	I	DREQ1	I	DREQ1	I
5	DREQ2	I	DREQ2	I	DREQ2	I
4	DREQ3	I	DREQ3	I	DREQ3	I
61	$\overline{\text{DACK0}}$	O	$\overline{\text{DACK0}}$	O	$\overline{\text{DACK0}}$	O
62	$\overline{\text{DACK1}}$	O	$\overline{\text{DACK1}}$	O	$\overline{\text{DACK1}}$	O
63	$\overline{\text{DACK2}}$	O	$\overline{\text{DACK2}}$	O	$\overline{\text{DACK2}}$	O
64	$\overline{\text{DACK3}}$	O	$\overline{\text{DACK3}}$	O	$\overline{\text{DACK3}}$	O
65	$\overline{\text{EOD0}}$	I/O	$\overline{\text{EOD0}}$	I/O	$\overline{\text{EOD0}}$	I/O
66	$\overline{\text{EOD1}}$	I/O	$\overline{\text{EOD1}}$	I/O	$\overline{\text{EOD1}}$	I/O
67	$\overline{\text{EOD2}}$	I/O	$\overline{\text{EOD2}}$	I/O	$\overline{\text{EOD2}}$	I/O
68	$\overline{\text{EOD3}}$	I/O	$\overline{\text{EOD3}}$	I/O	$\overline{\text{EOD3}}$	I/O
15	RESET	I	RESET	I	RESET	I
12	CLK	I	CLK	I	CLK	I
9,43	VSS	(Ground)	VSS	(Ground)	VSS	(Ground)
26,60	VCC	(Power Supply)	VCC	(Power Supply)	VCC	(Power Supply)

Pinning in 286 Mode

In the 286 mode the SAB 82258 bus signals and bus timings are the same as of the SAB 80286 processor. Additional features of SAB 82258 require a slight change in pin definitions. The processor can access internal registers of the SAB 82258. Therefore the bus signals must support these accesses. This means that some of the bus control signals must be bidirectional and some additional bus control signals are necessary. All pins and their functions are listed below.

Figure 6
Pin Configuration in 286 Mode

Component Pad View – As viewed from underside of component when mounted on the board



PC Board View – As viewed from the component side of the pc board

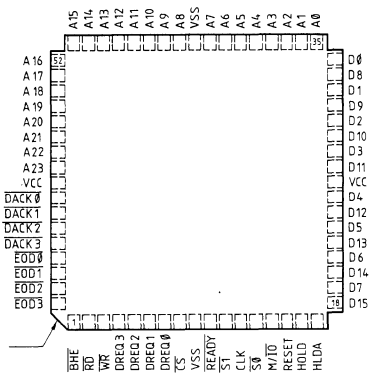


Table 2
Pin Description for 286 Mode
(Contains also the description for pins identical in all modes)

Symbol	Number	Input (I) Output (O)	Functions
$\overline{BHE}$	1	I/O	Bus High Enable indicates transfer of data on the upper byte of the data bus, D15–8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active LOW and floats to 3-state OFF when the SAB 82258 does not own the bus.
			$\overline{BHE}$ and A0 encodings
			$\overline{BHE}$ A0 Function
			0 0 Word transfer (D15–0)
			0 1 Byte transfer on upper half of data bus (D15–8)
			1 0 Byte transfer on lower half of data bus (D7–0)
			1 1 Odd addressed byte on 8 bit bus (D7–0)
$\overline{RD}$	2	I	Read command in conjunction with chip select enables reading out of SAB 82258 register which is addressed by the address lines A7–A0. This signal can be asynchronous to SAB 82258 clock.
$\overline{WR}$	3	I	Write command is used for writing into SAB 82258 registers. This signal can be asynchronous to SAB 82258 clock.
DREQ0-DREQ3	4-7	I	DMA request input signals are used for synchronized DMA transfers. DREQ3 has the meaning of I/O request (IOREQ) if channel 3 is a multiplexer channel. These signals can be asynchronous to SAB 82258 clock.
$\overline{CS}$	8	I	Chip select is used to enable the access of a processor to SAB 82258 registers. This access is additionally controlled either by bus status signals or by the Read or Write command signals. Chip select can be asynchronous to SAB 82258 clock.
$\overline{READY}$	10	I	Bus Ready terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{READY}$ LOW. $\overline{READY}$ is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation.

<table>
<tr><th>Symbol</th><th>Number</th><th>Input (I)
Output (O)</th><th>Functions</th></tr>
<tr><td>$\overline{S0}$, $\overline{S1}$</td><td>11, 13</td><td>I/O</td><td>The bus status signals control the support circuits. The beginning of a bus cycle is indicated by $\overline{S1}$ or $\overline{S0}$ or both going active. The termination of a bus cycle is indicated by all status signals going inactive in 186 mode or bus ready signal ($\overline{READY}$) going active in 286 mode. The type of bus cycle is indicated by $\overline{S0}$, $\overline{S1}$ and $\overline{S2}$ (in 186 mode) or M/$\overline{IO}$ (in 286 mode). $\overline{S2}$ and M/$\overline{IO}$ have the same meaning but in 186 mode the $\overline{S2}$ signal can be active only when at least one of $\overline{S1}$ or $\overline{S0}$ is active, whereas in 286 mode the M/$\overline{IO}$ signal is valid with the address on the address lines. SAB 82258 can generate the following bus cycles by activating the status signals (and M/$\overline{IO}$ in 286 mode):
<table>
<tr><th>M/$\overline{IO}$ or $\overline{S2}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Cycle Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Read I/O-Vector (for Multiplexor channel)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from I/O Space</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into I/O Space</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle, does not occur in 186 mode</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Does not occur</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Read from Memory Space</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Write into Memory Space</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>No bus cycle</td></tr>
</table>
When SAB 82258 is not the master of the local bus the status signals are used as inputs for detection of synchronous accesses to SAB 82258. The following table shows the bus status and $\overline{CS}$, signals and their interpretation by SAB 82258.
<table>
<tr><th>$\overline{CS}$</th><th>$\overline{S1}$</th><th>$\overline{S0}$</th><th>Description</th></tr>
<tr><td>1</td><td>X</td><td>X</td><td>SAB 82258 is not selected (no action)</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>no SAB 82258 access (no action)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Read from an SAB 82258 register</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Write into an SAB 82258 register</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>No bus cycle (Note 1)</td></tr>
</table>
Note 1: SAB 82258 is selected but no synchronous access is activated. In this case SAB 82258 monitors $\overline{RD}$ and $\overline{WR}$ signals for detection of an asynchronous access.</td></tr>
<tr><td>CLK</td><td>12</td><td>I</td><td>This clock provides the fundamental timing. It must be two times the system clock. It can be directly connected to the SAB 82284 CLK output. It is divided by two to generate the SAB 82258 internal clock. The on chip divide-by-two circuitry can be synchronized to the external clock generator by a LOW to HIGH transition on the RESET input, or by first HIGH to LOW transition on the Status Inputs $\overline{S0}$ or $\overline{S1}$ after RESET.</td></tr>
</table>

Symbol	Number	Input (I) Output (O)	Functions
M/$\overline{IO}$	14	O	Distinction between memory and I/O space addresses.
RESET	15	I	An activation of the reset signal forces SAB 82258 to the initial state. The reset signal must be synchronous to CLK.
HOLD	16	O	HOLD output, when true, indicates a request for control of the local bus. When the SAB 82258 relinquishes the bus it drops the HOLD output.
HLDA	17	I	HLDA, when true, indicates that the SAB 82258 can acquire the control of the bus. When it goes low SAB 82258 must relinguish the bus at the end of its current cycle. It can be asynchronous to the SAB 82258 clock.
D0-D15	18-25, 27-34	I/O	Data Bus – This is the bidirectional 16 bit data bus. For use with an 8 bit bus, only the lower 8 data lines D7-D0 are relevant.
A0–A7	35–42	I/O	The lower 8 address lines for DMA transfers. They are also used to input the register address when the processor accesses a SAB 82258 register.
A8–A23	44–59	O	Higher address outputs.
$\overline{DACK0}$-$\overline{DACK3}$	61–64	O	The $\overline{DACK}$i signal acknowledges the requests on the related DREQi signal. It is activated when the requested transfer(s) is (are) performed. If the channel 3 is a multiplexor channel the signal $\overline{DACK3}$ has the meaning of I/O acknowledge ($\overline{IOACK}$).
$\overline{EOD0}$-$\overline{EOD3}$	65–68	I/O	The End of DMA signals are implemented as open drain output drivers with a high impedance pull up resistor and thus can be used as bidirectional lines. As **outputs** the signals are activated for two system clock cycles at the end of the DMA transfer of the corresponding channel (if enabled) or they are activated under program control (EOD output or interrupt output). If the signals are held internally high but forced to low by external circuitry, they act as "End-of-DMA" **inputs**. The current transfer is aborted and SAB 82258 continues with the next command. Additionally, a special function is possible with the $\overline{EOD2}$ pin: this pin can also be used as common interrupt signal for all 4 channels. In this mode this signal is not a open drain output but a pushpull output (output only). The other EOD pins may be used as EOD outputs/inputs described above.
VCC	26,60		Power supply (5 V)
VSS	9,43		Ground (0 V)

Pinning in 186 Mode

In 186 mode many pins have a different meaning than in the 286 mode. They are listed below (for corresponding 286 names see table 1).

Figure 7
Pin Configuration in 186 Mode

Component Pad View – As viewed from underside of component when mounted on the board

PC Board View – As viewed from the component side of the pc board

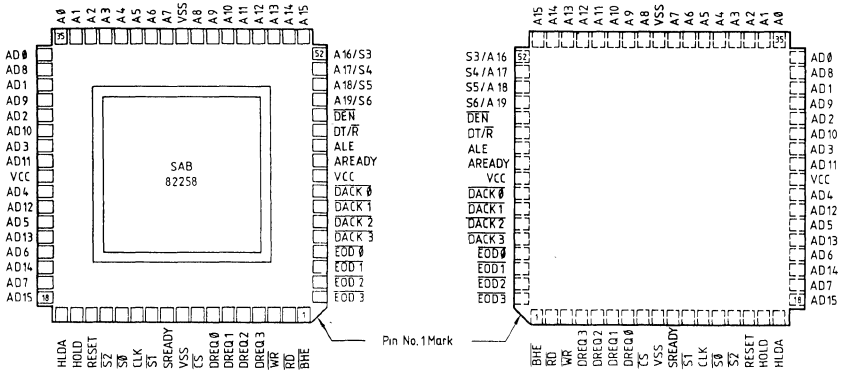


Table 3
Changes of Pin Description in 186 mode

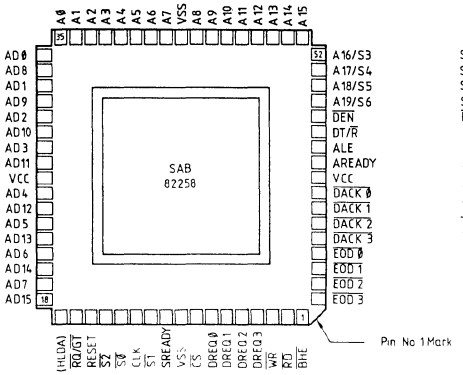
Symbol	Number	Input (I) Output (O)	Functions
$\overline{RD}$ $\overline{WR}$	2, 3	I/O	In 186 mode, the $\overline{RD}$ and $\overline{WR}$ pins are additionally used as output pins to support 80186 or 8086 minimum mode systems.
ALE	58	O	Address latch enable signal provides a strobe to separate the address information on the multiplexed AD lines.
$\overline{DEN}$	56	O	Data enable signal is used for enabling the data transceiver.
DT/$\overline{R}$	57	O	Data transmit/receive signal controls the direction of the data transceivers. When LOW, data is transferred to the SAB 82258, when HIGH the ADMA places data on to the data bus.
$\overline{S2}$	14	O	Status signal as for SAB 186/8086/88 processors (see also $\overline{S1}$, $\overline{S0}$ description in 286 mode).
AREADY	59	I	This is an asynchronous bus ready signal, the rising edge is internally synchronized, the falling edge must be synchronous to CLK. During reset this signal must be low for entering the 186 mode.
SREADY	10	I	Synchronous ready input. This signal must be synchronized externally. The use of this pin permits a relaxed system-timing specification by eliminating the clock phase which is required for resolving the signal level when using the AREADY input.
CLK	12	I	This is the input for the one time system clock. No internal prescaling is done.
AD0– AD15	18–25 27–34	I/O	Lower address and data information is multiplexed on pin AD0–AD15. Additionally the demultiplexed address information is available on address pin A0–A15.
A0–A7 A8–A15	35–42 44–51	I/O O	
A16/S3– A19/S6	52, 55	O	The higher address bits are multiplexed with additional status information.

Pinning in 8086 Mode

In 8086 mode the bus arbitration is done via $\overline{RQ}/\overline{GT}$ protocol instead of the HOLD/HLDA protocol in 186 mode. The function of the other pins is identical to 186 mode.

Figure 8
Pin Configuration in 8086 Mode

Component Pad View – As viewed from underside of component when mounted on the board



PC Board View – As viewed from the component side of the pc board

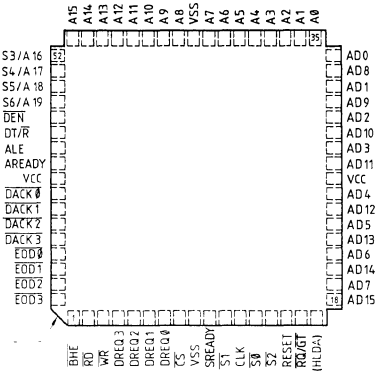


Table 4
Changes of Pin Description in 8086 Mode

Symbol	Number	Input (I) Output (O)	Functions
$\overline{RG}/\overline{GT}$	16	I/O	In the 8086 mode the HOLD input acts as REQUEST/ GRANT line. The REQUEST/GRANT protocol implements a one-line communication dialog required to arbitrate the use of the system bus normally done via HOLD/HLDA. The $\overline{RG}/\overline{GT}$ signal is active low and has an internal pullup.
HLDA	17	I	After entering 8086-mode this pin no longer acts as hold-acknowledge input for the bus arbitration with the processor. But it can still be used to force the SAB 82258 off the bus by a low input level (e.g. it a third priority bus master needs the bus).

Pinning in Remote Mode

In remote mode most of the bus signals have the same functions as in the 286 mode. The other pins are listed below.

Figure 9
Pin Configuration in Remote Mode

Component Pad View – As viewed from underside of component when mounted on the board

PC Board View – As viewed from the component side of the pc board

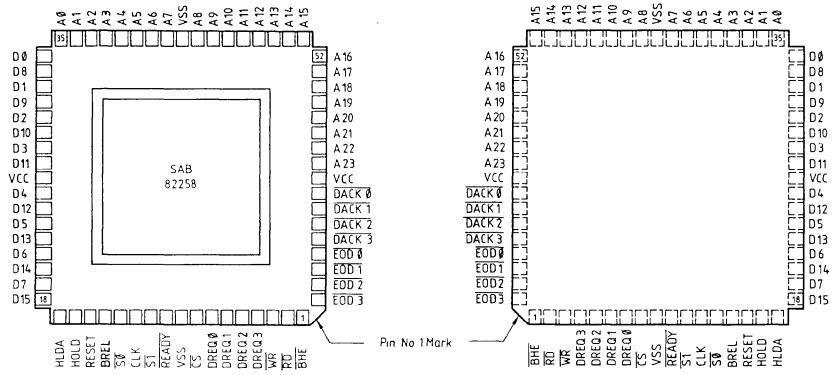


Table 5
Changes of Pin Description in Remote Mode

Symbol	Number	Input (I) Output (O)	Functions
BREL	14	O	In this mode pin 14 is used to indicate when SAB 82258 has released the control of the local bus.
$\overline{CS}$	8	I	In Remote Mode the $\overline{CS}$ input has two functions: besides enabling the access to SAB 82258 internal registers it works as an Access Request input. When forced to low it signals the SAB 82258 that another bus master needs access to the local bus of the SAB 82258 (e.g. to read/write SAB 82258 registers). SAB 82258 releases the bus as soon as possible and indicates this by activating the BREL output.
HOLD HLDA	16 17	O I	Signals on these pins are only used for access to the system bus. They are connected to the bus arbiter. Resident bus accesses are directly executed (without HOLD/HLDA sequence).

Functional Description

General

SAB 82258 is an advanced general purpose DMA controller especially tailored for efficient high speed data transfers on a SAB 80286 as well as an SAB 80186/188 or SAB 8086/88 bus.
It supports two basic operating modes:

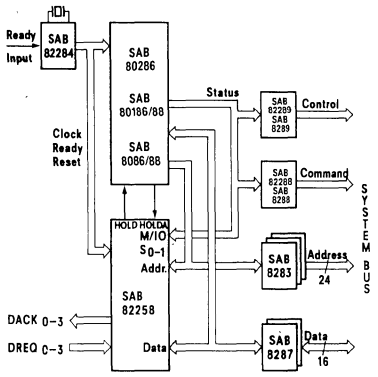
– local mode (tightly coupled to a processor) and
– remote mode (loosely coupled to a processor).

In the first case SAB 82258 is directly coupled to the CPU and uses the same system support/control devices as the CPU (see figure 10a). This mode is possible with the above mentioned processors.

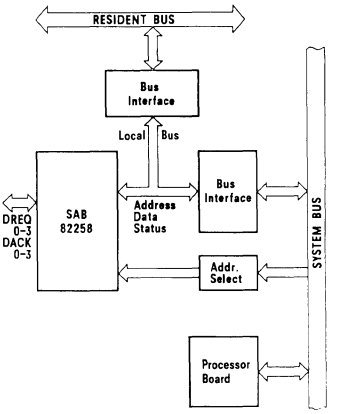
As a second basic operating mode a remote (stand alone) mode is supported (see fig. 10b). Here the SAB 82258 has his own sets of bus interface circuits and thus can dispose of its own local bus. This allows the DMA-controller to work in parallel to the main CPU and therefore overall system performance could be increased. Besides that, this mode is very useful for the design of modular systems and allows connecting the ADMA to any other processor via the system bus independent of the processor's unique local bus.

Figure 10
Basic ADMA Operating Modes

a) Local Mode

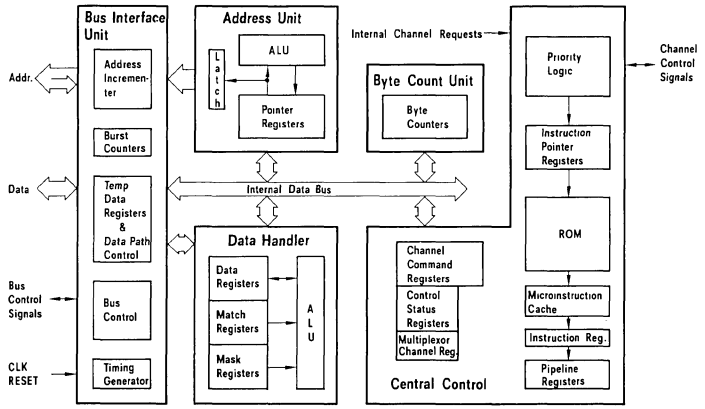


b) Remote Mode



SAB 82258 has four independent DMA channels that can transfer up to 8 Mbytes/sec in the single cycle mode (2 clocks/transfer). In the 2 cycle transfer mode the maximum rate is 4 Mbytes/sec. Switching between channels induces no time penalty. Thus the overall maximum transfer rate of 8 Mbytes/sec is also valid for multiple channel operation.
This fast operation is possible because of the pipelined architecture of the SAB 82258 that allows the different function units to work in parallel.

Figure 11
Block diagram of SAB 82258



The ADMA supports two address spaces, memory space and I/O space, each with a maximum address range of 16 Mbytes. In addition, the maximum block length (byte count) is also 16 Mbytes to support applications where large blocks of data have to be transferred (e.g. graphics).

As source or as destination, four parameters can be independently selected:

- Address Space (memory or I/O)
- Physical Bus Width (8 bit or 16 bit),
- Logical Bus Width (same as physical bus width or 8 bit on a 16 bit physical bus)
  and
- Transfer Direction (increasing, decreasing, fixed pointer or constant value).

If the physical bus width of source or destination does not meet the logical bus width an automatic byte/word assembly (word/byte disassembly) takes place if this minimizes the necessary transfers. The same is true if the logical bus widths of source and destination are different.
Transfers between different address spaces can be performed within one cycle or in two cycles, transfers within one address space can be performed only in two cycles.

The transfers can be executed free running or externally synchronized via DRQ where source or destination synchronization is possible.

In summary, this very symmetrical operation of SAB 82258 gives the user a great amount of design flexibility.

Adaptive Bus Interface

As shown in figure 5 the SAB 82258 bus interface has two basic timing modes: the 286 mode and the 186 mode. In 286 mode SAB 82258 is directly coupled to an SAB 80286, in 186 mode to an SAB 80186 or SAB 80188. For each of these two modes a slightly different variation exists:

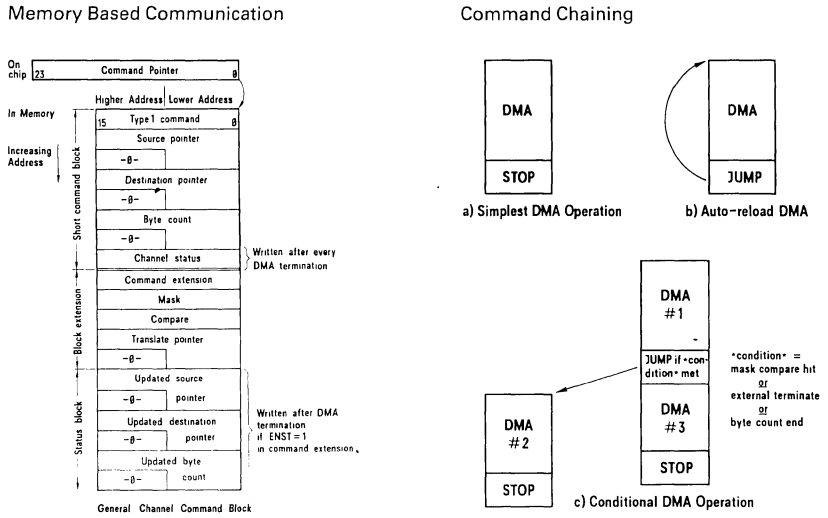
- For the 286 mode, the Remote Mode, where the ADMA operates as a bus master on the system bus without being directly coupled to a processor. In this mode SAB 82258 can dispose of its own local bus and the communication with the main processor is done via the system bus. To enable access to ADMA registers by the main processor, SAB 82258 must release its local bus. This "local bus arbitration" in remote mode is done via the $\overline{CS}$ and BREL lines.
- For the 186 mode the variation is the 8086 mode where the SAB 82258 supports the $\overline{RQ}/\overline{GT}$ protocol and thus can be directly coupled to an SAB 8086 or SAB 8088.

Memory Based Communication

The normal communication between the ADMA and the processor is memory based. This means that all necessary data for a transfer is contained in a command block in memory accessible for CPU and SAB 82258 (see figure 12). To start the transfer the CPU loads one of the command pointer registers of SAB 82258 with the address of the command block and then gives a "start channel command". Getting the command SAB 82258 loads the entire command block from memory into its on-chip channel registers and executes it. On completing the operation, channel status information is written back by SAB 82258 into the channel status word contained in the command block in memory. If desired the actual contents of the channel registers, i.e. source pointer, destination pointer and byte count is transferred into the Channel Status Block. The Channel Status Block immediately follows the Command Block in memory (see figure 12).

Figure 12

Memory Based Communication and Command Chaining



Command Chaining

Command blocks for any channel can be chained for sequential execution (see figure 12). When SAB 82258 comes to an end with one command, it automatically starts to fetch and execute the next command block until a stop command is found. As a result a chain of command blocks can be executed by the ADMA without any CPU intervention. Due to conditional and unconditional STOP and JUMP commands, quite complex sequences of DMA can be executed by SAB 82258.

Data Chaining

Data chaining permits an automatic, dynamic linking of data blocks scattered in memory. There are two types: list and linked-list data chaining.

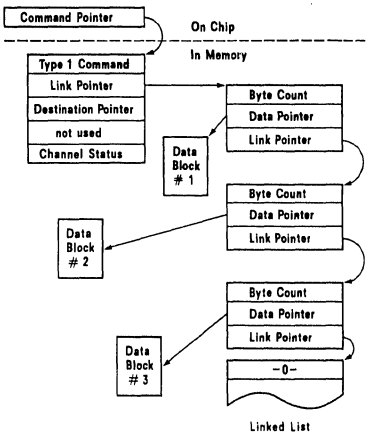
If for a DMA the source blocks are to be dynamically linked during DMA it is called source chaining and the effect is that of gathering data blocks and sending them out effectively as one block.

If one source block is dynamically broken-up into multiple destination blocks, it is called destination chaining. This results in scattering of a block.

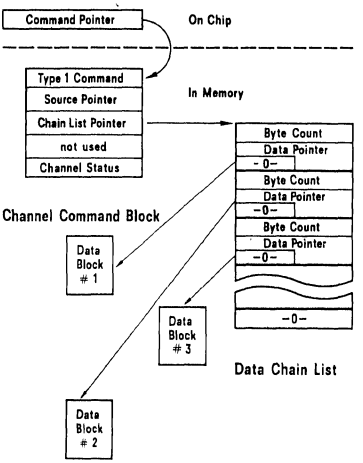
This dynamic linking and un-linking of data blocks makes the logical sequencing of data independent of its physical sequencing in memory.

Figure 13
Data Chaining

a) Linked List Chaining



b) List Chaining



In the case of linked list chaining (see figure 13 a) each data block has a descriptor containing information on position of data block in memory, length of data block, and a pointer to the next description.

During data transfer the data block 1 is sent out first, then 2 and so on till a 0 is encountered in the byte count field.

The second type of data chaining is List Chaining (figure 13 b).

Unlike linked list chaining, here the data block descriptors are continuous in a block and thus determine the sequence of data blocks. The flexibility lost in terms of predefined sequence is gained in terms of linking time.

"On-The-Fly" Operations

A normal DMA controller blindly transfers data from source to destination without looking at the data. In case of the ADMA on-the-fly operations are executed during the DMA transfer and allow inspection and/or operation on the transferred data. There are three on-the-fly operations possible:

- Mask/Compare,
- Translate and
- Verify

During a mask/compare operation each byte/word transferred is compared to a given pattern. One or more bits can be masked and thus do not contribute to the result of the compare operation. The result can be used by subsequent conditional stop or jump operations.

For translate operation the byte (no word possible) that is fetched from source is added to a translate pointer to build the effective source pointer. The byte pointed to by this pointer is then fetched and sent out to the destination. Of course a mask/compare operation is possible on the byte sent out.

The verify operation is a type of block compare operation to compare each byte/word of data read from a peripheral with that in a data block in memory. There are three options:

1. Verify with no termination on mismatch (2-cycle transfer only)
2. Verify with termination on mismatch (2-cycle transfer only).
3. Verify and save (single cycle transfer only). Here an actual transfer with compare takes place. The transfer is not stopped on mismatch.

Multiplexer Channel

When programmed to multiplexer mode channel 3 (supported by a multiplexer logic) can be used to service up to 32 subchannel request lines (see figure 14). Thus it is ideally suited to service a large number of relatively slow equipment like CRT terminals, line printers etc. Since multiple subchannels are processed with the resource of one DMA channel, the overhead of subchannel switching, of course, decreases the total effective throughput on the multiplexer channel.

Figure 14a
Multiplexer Channel

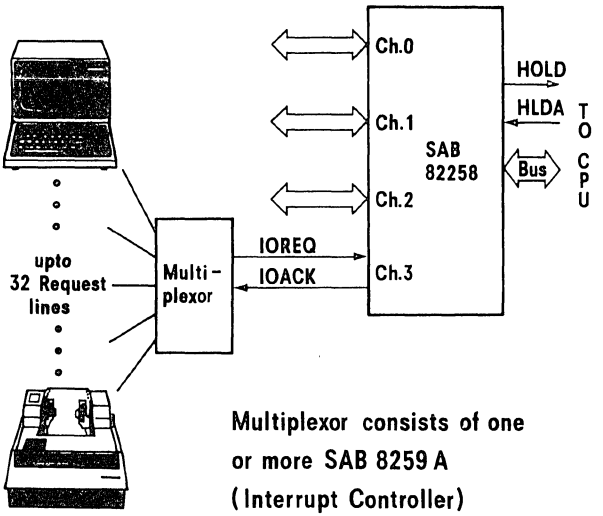
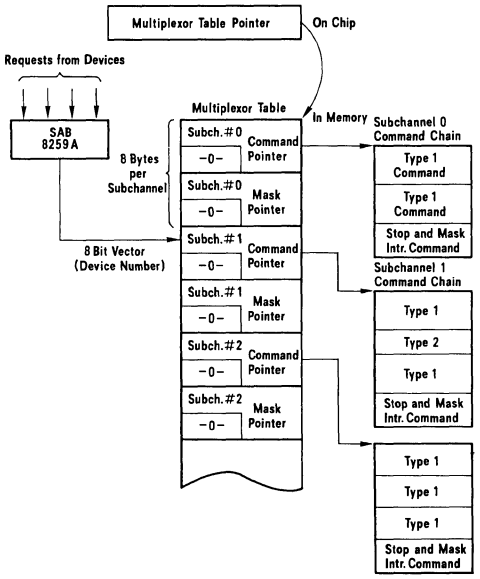


Figure 14b)
Structure of Multiplexer Table



The mask pointer is the address of the appropriate SAB 8259A mask register.

Operating the SAB 82258

Reset

When activating the reset input, SAB 82258 is forced into its initial state. All channels and bus activities are stopped, tristate lines are tristated and the others enter the inactive state.
While the reset input is active line A23/AREADY and HLDA must be forced to the appropriate levels to select the desired bus interface mode (see figures 5 and 36).
After deactivating reset the inactive state is maintained, in addition the state of SAB 82258 registers is as follows:

- General Mode Register, General Burst Register, General Delay Register, General Status Register and the four Channel Status Registers are set to zero,
- the Vector Not Valid bit of the Multiplexer Interrupt Vector Register is set to 1,
- all other registers and bits are undefined.

Note that the General Mode Register (GMR) should be loaded first to select the mode of operation before any other activity is started on the ADMA.

DMA Interface

The DMA interface consists of three lines:

- DRQ – DMA request,
- DACK – DMA acknowledge and
- EOD – end of DMA

The first two lines work as request and acknowledge lines to control synchronized DMA transfers as known from conventional DMA controllers.

A special feature of SAB 82258 are the bidirectional EOD lines. First they can be used as inputs to receive an asynchronous external terminate signal to terminate a running DMA. Second, as an output, they can be used to send out a pulse which interrupts the CPU and/or signals to the peripheral a specific status (e.g. transfer aborted or end of a block or send/receive next block ...).

The EOD output signal can be generated synchronously to a transfer (during the last transfer) or asynchronously to the transfers by a specific command.

In addition the EOD output of channel 2 can be used as a collective interrupt output for all DMA channels while the other three retain their normal function.

Slave Interface

The slave interface is used to access SAB 82258 internal registers. Although nearly all of the communication between CPU and ADMA is done via memory based data blocks, some direct accesses to ADMA registers are necessary. For example during the initialization phase the general mode registers must be written, or to start a channel the command pointer register and the general command register must be loaded. Also during the debugging phase it is of great benefit to have access to all of the SAB 82258 internal registers.

The slave interface is enabled by the $\overline{CS}$ input and consists of the following lines:

- $\overline{S0}$, $\overline{S1}$ – Status Lines (inputs)
- $\overline{RD}$, $\overline{WR}$ – Control Lines (inputs)
- A0–A7 – Register Address (inputs)
- D0–D15 – Data Lines (inputs/outputs) and
- AD0–AD15 – Address/Data Lines (inputs/outputs) for synchronous access in 186 mode

Note, that all of these lines are outputs if SAB 82258 is an active bus master.

In 186 mode and 286 mode two types of accesses are possible:

- Synchronous access by means of the status lines. Processor and SAB 82258 are directly coupled and must use the same clock,
- Asynchronous access by using the control lines $\overline{RD}$ and $\overline{WR}$ (processor and ADMA may have different clocks).

  In all modes except the synchronous access in 186 mode the register address must be supplied on address pins A0–A7. Using synchronous access in 186 mode the address information is expected at address/data lines AD0–AD7.

  In remote mode only the asynchronous access is possible because SAB 82258 first has to release its local bus to enable the register access. On receiving an access request (activation of $\overline{CS}$ input) SAB 82258 releases its local bus as soon as possible and signals this by activating the BREL line. Now the CPU can accomplish its access.

Register Set

Figure 15 shows the user visible registers of SAB 82258. A set of 5 registers, called the general registers, is used for all the 4 channels. The mode register is written first after reset and it describes the SAB 82258 environment – bus widths, priorities etc. The General Command Register (GCR) is used to start and stop the DMA transfer on different channels. General Status Register (GSR) shows the status of all the 4 channels; if the channel is running, if interrupt is pending etc. General Burst Register (GBR) and General Delay Register (GDR) are used to specify the bus load which is permissible for SAB 82258.

There is a set of channel registers for each of the 4 channels. Most channel registers serve as cache registers and need to be accessed only for debugging. During normal operation they are automatically loaded by SAB 82258 (see next paragraph).

The layout of register addresses is shown in figure 16. All register lie at even addresses. Locations not designated in figure 16 are reserved.

Figure 15
SAB 82258 Register Set

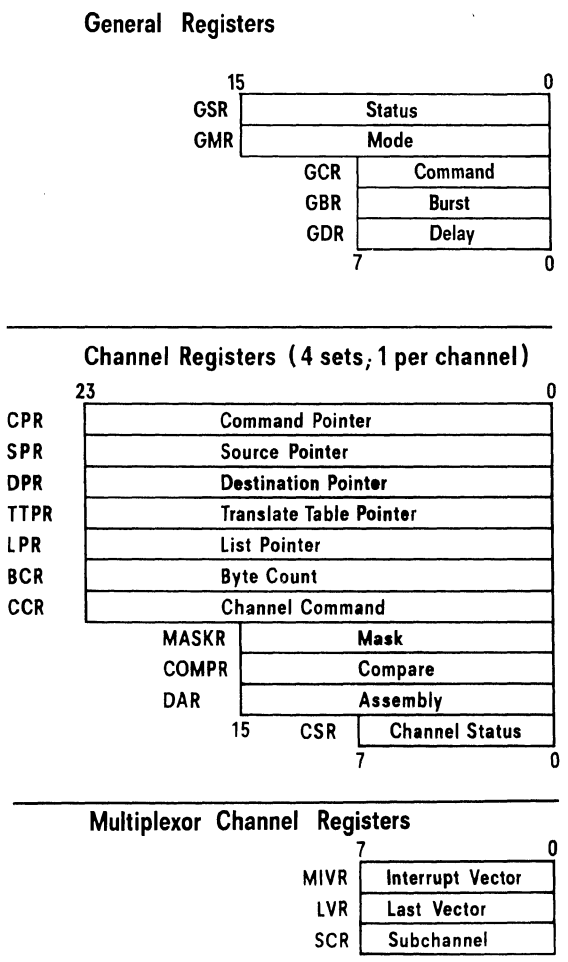


Figure 16
Layout of Register Addresses

Address Bits 0-5	Address Bits 7,6			
	00	01	10	11
0	GCR			
2	SCR			
4	GSR			
6				
8	GMR			
A	GBR			
C	GDR			
E				
10	$CSR_{Ø}$	CSR_1	CSR_2	CSR_3
12	$DAR_{Ø}$	DAR_1	DAR_2	DAR_3
14	$MASKR_{Ø}$	$MASKR_1$	$MASKR_2$	$MASKR_3$
16	$COMPR_{Ø}$	$COMPR_1$	$COMPR_2$	$COMPR_3$
18				MIVR
1A				LVR
1C				
1E				
20	$CPR_{LØ}$	CPR_{L1}	CPR_{L2}	CPR_{L3}
22	$CPR_{HØ}$	CPR_{H1}	CPR_{H2}	CPR_{H3}
24	$SPR_{LØ}$	SPR_{L1}	SPR_{L2}	SPR_{L3}
26	$SPR_{HØ}$	SPR_{H1}	SPR_{H2}	SPR_{H3}
28	$DPR_{LØ}$	DPR_{L1}	DPR_{L2}	DPR_{L3}
2A	$DPR_{HØ}$	DPR_{H1}	DPR_{H2}	DPR_{H3}
2C	$TTPR_{LØ}$	$TTPR_{L1}$	$TTPR_{L2}$	$TTPR_{L3}$
2E	$TTPR_{HØ}$	$TTPR_{H1}$	$TTPR_{H2}$	$TTPR_{H3}$
30	$LPR_{LØ}$	LPR_{L1}	LPR_{L2}	$LPR_{L3}/MTPR_{L}$
32	$LPR_{HØ}$	LPR_{H1}	LPR_{H2}	$LPR_{H3}/MTPR_{H}$
34				
36				
38	$BCR_{LØ}$	BCR_{L1}	BCR_{L2}	BCR_{L3}
3A	$BCR_{HØ}$	BCR_{H1}	BCR_{H2}	BCR_{H3}
3C	$CCR_{LØ}$	CCR_{L1}	CCR_{L2}	CCR_{L3}
3E	$CCR_{HØ}$	CCR_{H1}	CCR_{H2}	CCR_{H3}

GCR = General Command Register
SCR = Subchannel Register
GSR = General Status Register
GMR = General Mode Register
GBR = General Burst Register
GDR = General Delay Register
CSR = Channel Status Register
DAR = Data Assembly Register
MASKR = Mask Register
COMPR = Compare Register
MIVR = Multiplexor Interrupt Vector Register
LVR = Last Vector Register
CPR = Command Pointer Register
SPR = Source Pointer Register
DPR = Destination Pointer Register
TTPR = Translate Table Pointer Register
LPR = List Pointer Register
MTPR = Multiplexer Table Pointer Register
BCR = Byte Count Register
CCR = Channel Command Register

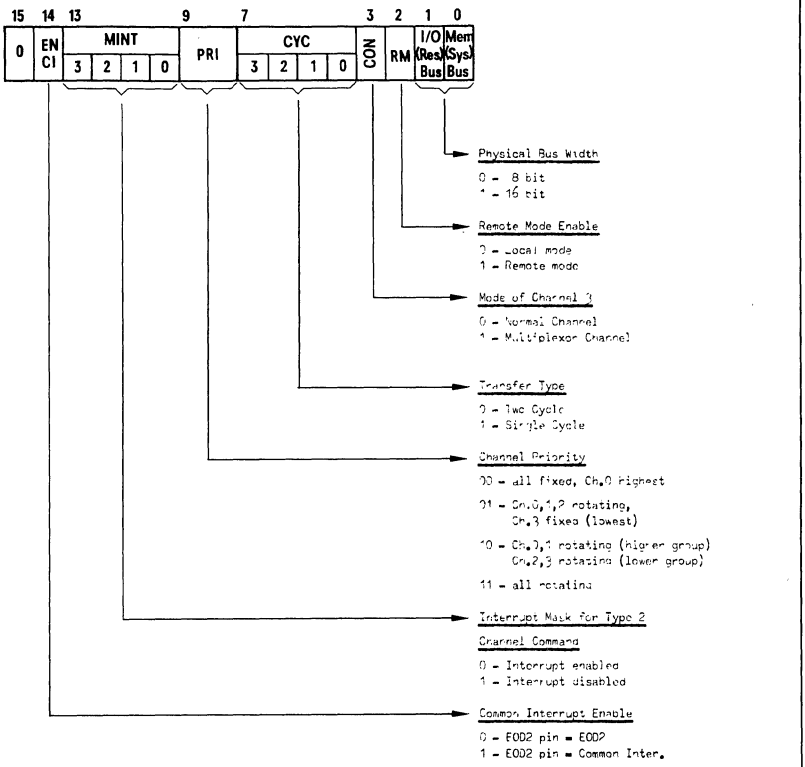
Register Description

General Mode Register

In the General Mode Register GMR (figure 17) the system wide parameters are specified.

This register should be programmed first after reset.

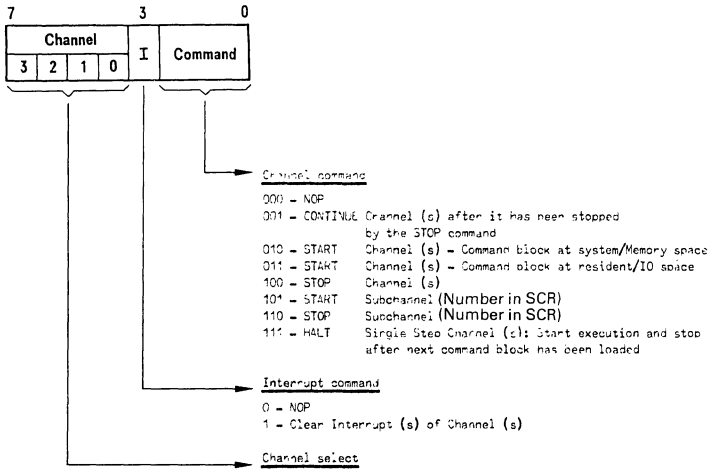
Figure 17
General Mode Register (GMR)



General Command Register

Individual channels are started and stopped by a command written to the General Command Register GCR (figure 18). The GCR is directly loaded by the CPU.

Figure 18
General Command Register (GCR)

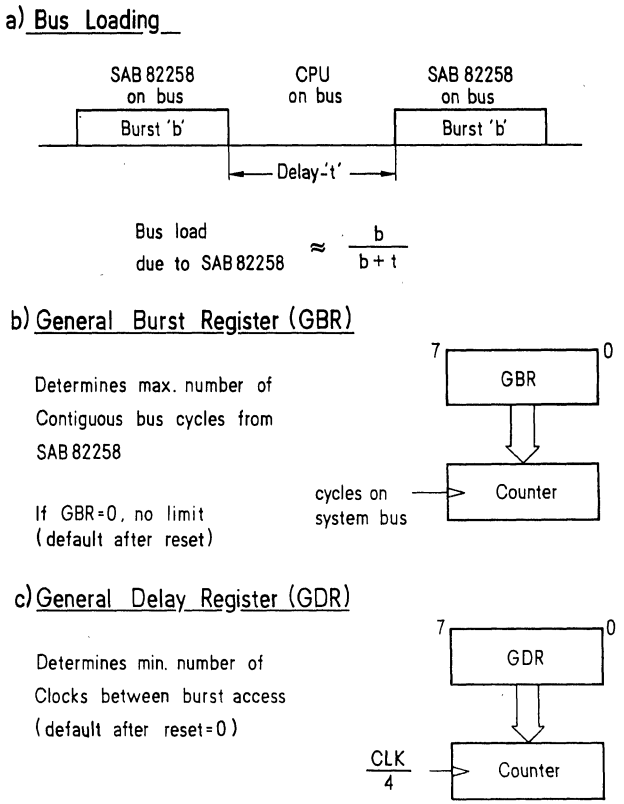


General Burst and Delay Register

It is possible to restrict the bus load generated by SAB 82258 on the CPU bus by programming the burst and the delay register. The bus load is defined by the formula given in figure 19a. The factor b (burst) is programmed in the General Burst Register GBR, t (delay time) in the General Delay Register GDR (see figure 19b and c).

Since SAB 82258 can also execute locked bus cycles, the maximum burst length consists of b+3 (8 bit bus) or b+2 (16 bit bus) bus cycles. GBR and GDR must be directly loaded by the CPU. Loading GBR with 0 leads to no bus load limitations for SAB 82258 (default after reset).

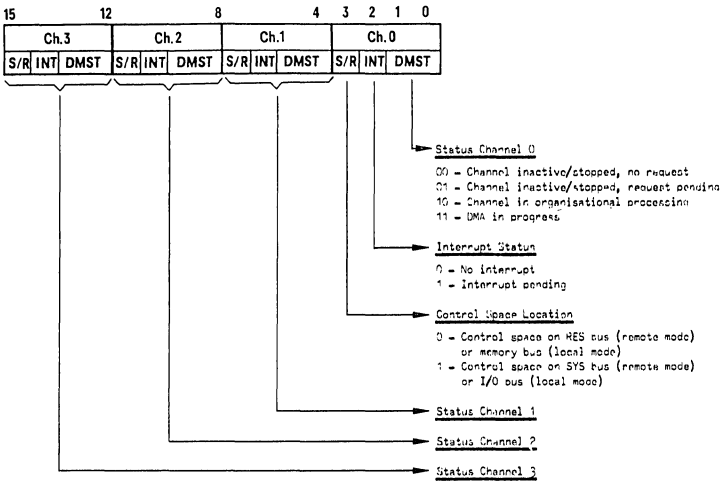
Figure 19
General Burst and Delay Register



General Status Register

The General Status Register GSR (figure 20) shows the current states of all the channels.

Figure 20
General Status Register (GSR)



Channel Commands

The channel commands are contained in the channel command block (figure 12). Up to 22 bits are used to specify the command. There are two types of channel commands:

- Type 1: for data movement
- Type 2: for command chaining control

The command block for a Type 1 command is in general 26 bytes long (see figure 12).

For certain type 1 transfers which, for example, do not use "on-the-fly" match, translate or verify feature, the command is only 16 bits long and only a short command block is necessary (see figure 12).

The Type 1 command fields (see figures 21 and 22) contain information on:

a. Bus width of source and destination
b. If source and/or destination address should be incremented or decremented or kept constant during the transfer
c. If source/destination is in memory or I/O space (local mode) or in system or I/O space (remote mode)
d. If data chaining (list or linked-list) is to be performed
e. If the data transfer is synchronized (source or destination)
f. If an "on-the-fly" match operation and/or translate operation has to be performed
g. If a verify operation has to be performed.

Type 2 command blocks are 6 bytes long (see figure 23) of which the first 2 bytes form the command and the rest is either a relative displacement or an absolute address for the JUMP operation. There are 2 basic type 2 commands (figure 23):

a. JUMP – conditional and non-conditional
b. STOP – conditional and non-conditional

The conditional case tests for either of the 4 condition bits which are altered at the termination of any DMA operation:

- Termination due to byte count end
- Termination due to mask-compare
- Termination due to external terminate
- Verify operation resulting in mismatch.

It is thus possible to JUMP or STOP further execution of commands based on any of these conditions and optionally generate EOD or interrupt signal.

The combination of type 1 and 2 commands gives SAB 82258 a high degree of "programmability". It can thus execute quite complex algorithms with a fairly low demand for CPU service.

Figure 21
Type 1 (DMA) Channel Command

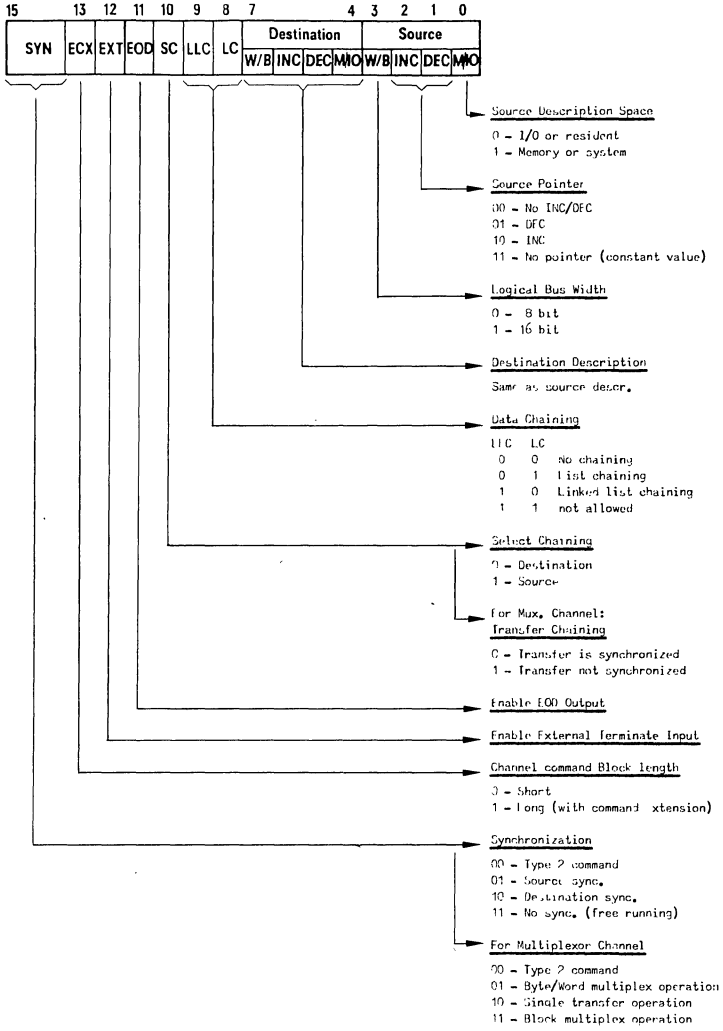


Figure 22
Type 1 Channel Command Extension

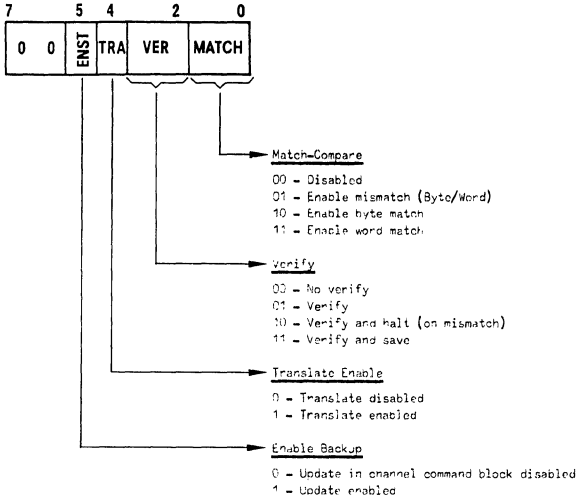


Figure 23

Type 2 Command Blocks (for command chaining control)

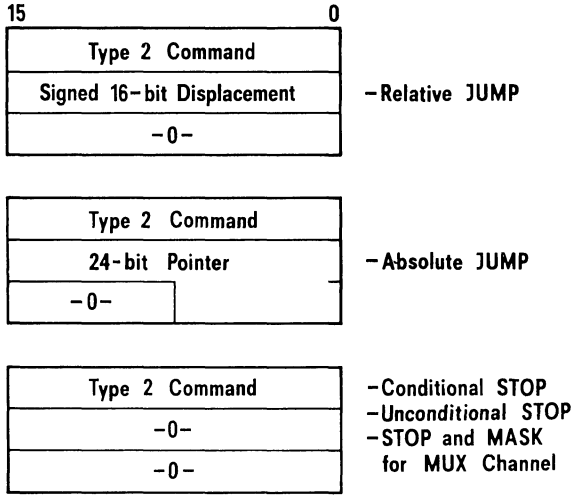
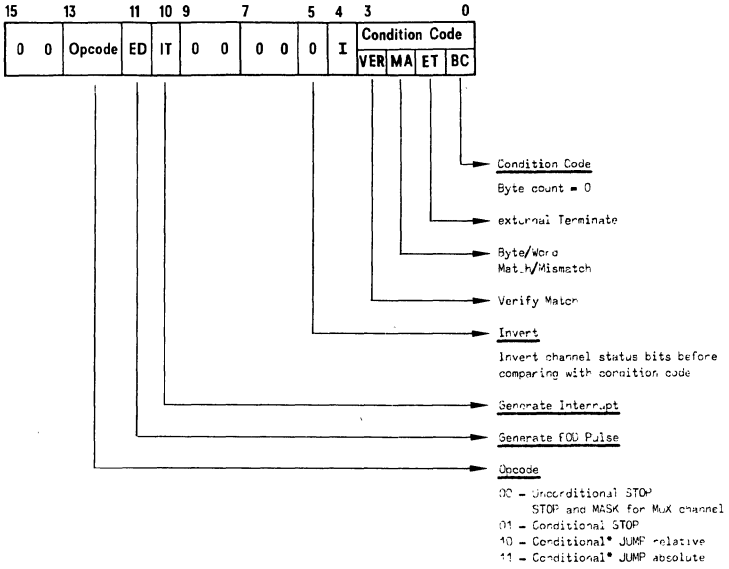


Figure 24
Type 2 Command Format

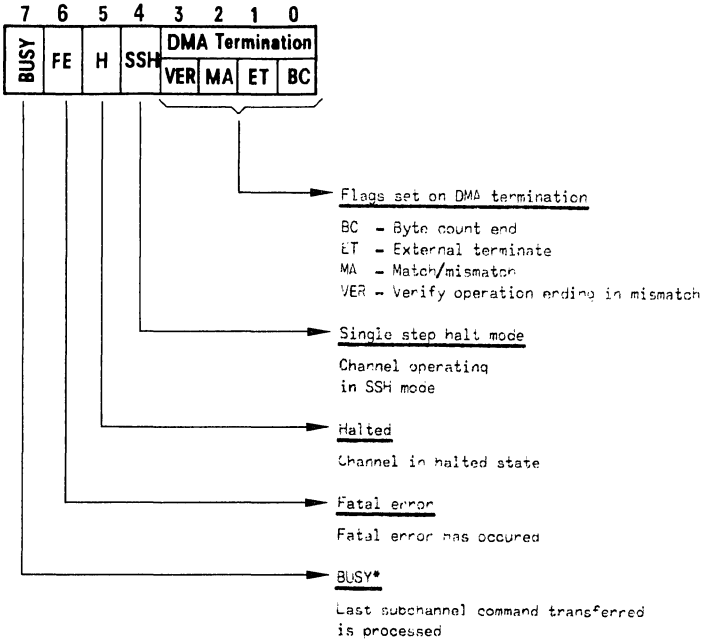


*) Unconditional JUMP when all condition code bits are set 1.

Channel Status Register

For each channel exists a Channel Status Register (see figure 25). This register shows the current state of the appropriate channel.

Figure 25
Channel Status Register



*) Valid only for channel 3 in multiplexer mode. In all other cases 0 is returned.

Multiplexer Channel Registers

These registers are valid only for channel 3 if programmed as multiplexer channel.

Multiplexer Table Pointer Register (MTPR)

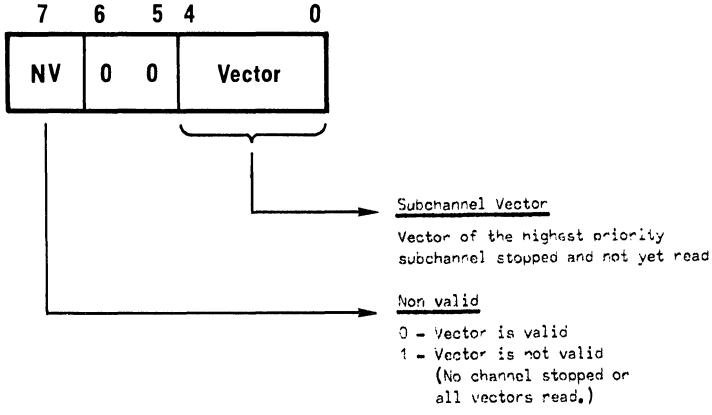
This 24 bit register is used to reference the multiplexer table in memory (see figure 14b). It must be loaded by the CPU. Physically the List Pointer Register is used, since data chaining is not allowed for multiplexer channel.

Multiplexer Interrupt Vector Register

This 8 bit register is read by the CPU to determine which channels are stopped. The vectors of the stopped subchannels are output on subsequent read operations in order of their priority (0 has highest priority).

Figure 26

Multiplexer Interrupt Vector Register (MIVR)



Last Vector Register (LVR)

This 8 bit register holds the last vector read by SAB 82258 (from SAB 8259A). In case of a stop caused by a fatal error on channel 3, LVR determines the failing subchannel.

Subchannel Register

This 8 bit register must be loaded by the CPU with the desired subchannel number before a subchannel command is written into GCR.

Timings

The bus timings in 286 and Remote mode are identical to that for SAB 80286, in the 186 and 8086 mode the timings are identical to that for SAB 80186. For exact timings see timing diagrams of A.C. Characteristics.

Asynchronous control inputs are specified with setup and hold times which are only meaningful to determine whether the SAB 82258 responds to the signal in the current cycle or the next cycle.

Absolute Maximum Ratings[1)]

Temperature Under Bias	0 to 70°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground	− 1 to +7V
Power Dissipation	3.6W

D.C. Characteristics[2)]

TA = 0 to 70°C; VCC = +5 ±10%

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
VIL	Input Low Voltage (except CLK)	−0.5	+0.8	V	–
VIH	Input High Voltage (except CLK)	2.0	VCC+0.5		
VOL	Output Low Voltage	–	0.45		IOL = 3.0 mA
VOH	Output High Voltage	2.4	–		IOH = −400 µA
ICC	Power Supply Current	–	450	mA	TA = 25°C, all outputs open
ILI	Input Leakage Current				0V ≤ VIN ≤ VCC
	$\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{BHE}$, $\overline{RD}$, $\overline{WR}$, M/$\overline{IO}$		−200	µA	
	HOLD ($\overline{RQ}$/$\overline{GT}$ mode), $\overline{EOD}$		−1.5	mA	
	other pins		±10	µA	
ILO	Output Leakage Current				0.45V ≤ VOUT ≤ VCC
VCL	Clock Input Low Voltage	−0.5	+0.6	V	–
VCH	Clock Input High Voltage	3.8	VCC+1.0		
CIN	Capacitance of Inputs (except CLK)	–	10	pF	fc = 1 MHz
CO	Capacitance of I/O or Outputs		20		
CCLK	Capacitance of CLK Input		12		

[1)] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2)] Clock must be applied.

A.C. Characteristics

TA = 0 to +70°C; VCC = +5V ±10%
Any output timing is measured at 1.5V.

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
1	CLK Cycle Period	62.5	250	ns	–
2	CLK Low Time	15	230		at 0.6V
3	CLK High Time	20	235		at 3.2V
4	Output Delay	0	60		CL = 125 pF
5	Output Delay		40		
6	DATA Setup Time	10	–		–
7	DATA Hold Time	5			
8	READY Setup Time	38.5			
9	READY Hold Time	25			
10	Input Setup Time	20			
11	Input Hold Time				
12	Address Set Up	2.5			
13	Output Delay	0	50		
14	Delay to Float	–	60		
15	Chip Select Set Up	60	–		
16	Command Length	290			at 8 MHz Operation
17	Data Set Up	165			
18	Address Set Up	80			–
19	Command Inactive	290			at 8 MHz Operation
19a	Access Time	–	320		

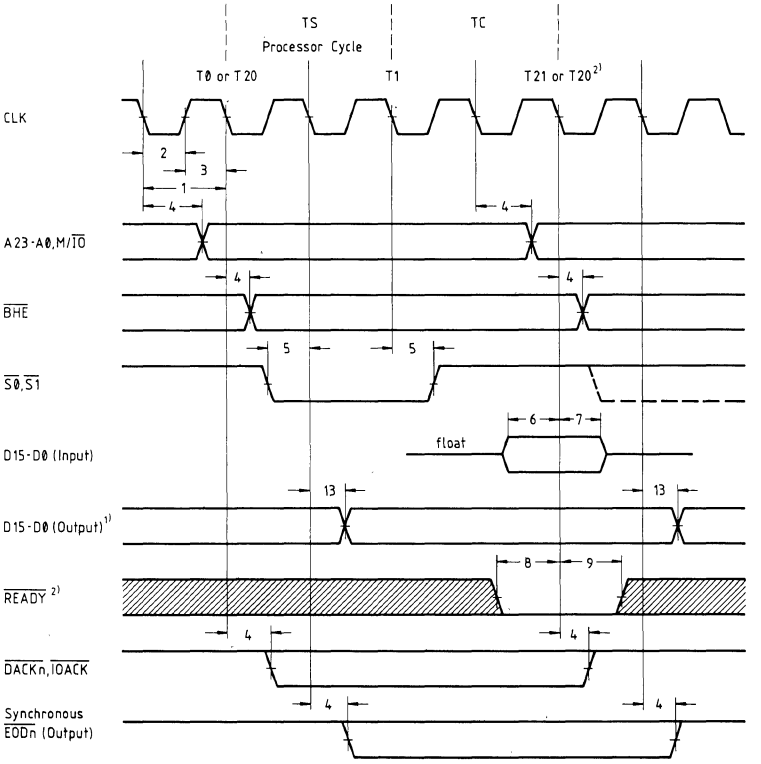
A.C. Characteristics (continued)

Symbol	Parameter	Limit Values		Units	Test Conditions
		Min.	Max.		
CLK Timing for 186 Mode					
20	CLK Period	125	500	ns	–
21	CLK Low Time	55	–		
22	CLK High Time				
23	CLK Rise Time	–	15		1.0 to 3.5V
24	CLK Fall Time				3.5 to 1.0V
Ready Timing for 186 Mode					
25	Ready Active Set Up Time	20	–	ns	–
26	Ready Hold Time	10			
27	Ready Inactive Set Up Time	35			
28	Set Up Time	20			
29	Hold Time	0			
30	Data Delay	10	50		
31	Status Delay		55		
32	Delay to Float		50		

Asynchronous inputs are specified with setup and hold times which are only intended for determination of whether the SAB 82258 responds to the signal in the current cycle or the next cycle.

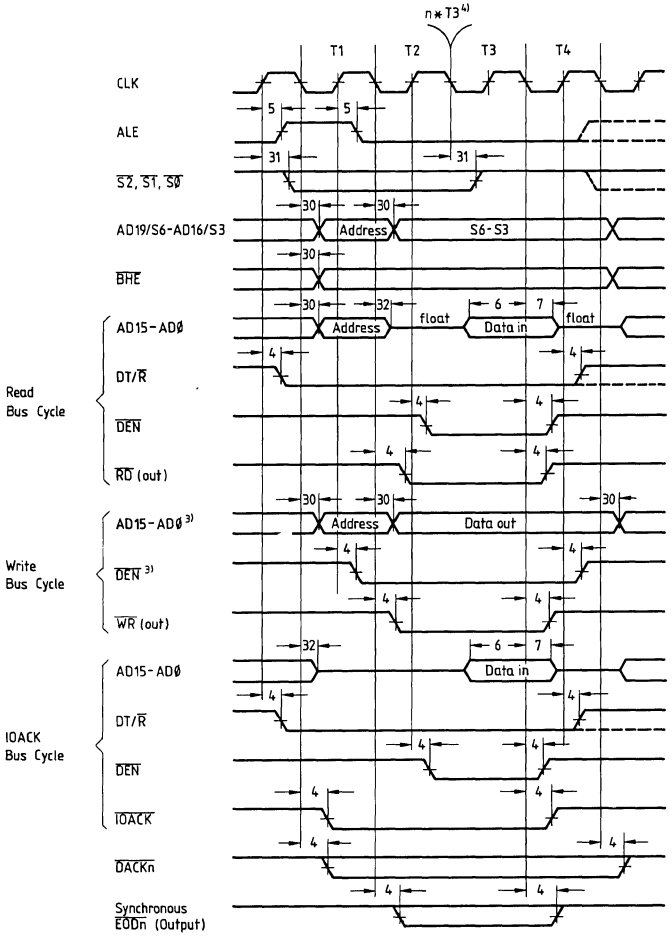
Waveforms

Figure 27
Timing of an Active Bus Cycle (286 mode)



Note 1: D15-D0 floats during Single Cycle Transfer like a Read Cycle.
Note 2: T2 will be repeated, if READY is inactive.

Figure 28
Timing of an Active Bus Cycle (186 mode)



Note 3: For a Single Cycle Transfer the timing of AD15-AD0, $\overline{DEN}$ and DT/$\overline{R}$ is the same as in a Read Bus Cycle.

Note 4: Additional T3 cycles will be inserted if bus is not ready (see fig. 32).

Figure 29

Timing of a Synchronous Access to the SAB 82258 (286 mode)

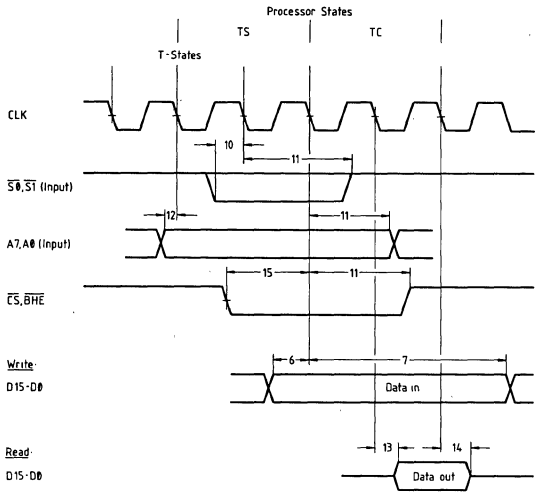


Figure 30
Timing of a Synchronous Access to the SAB 82258 (186 mode)

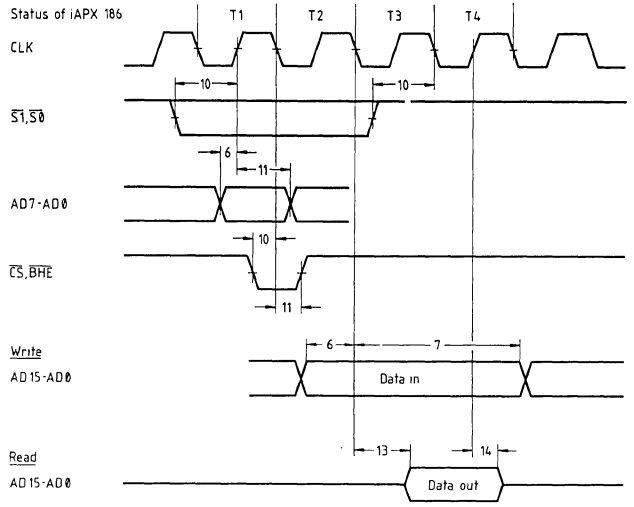


Figure 31
Timing of an Asynchronous Access to the SAB 82258

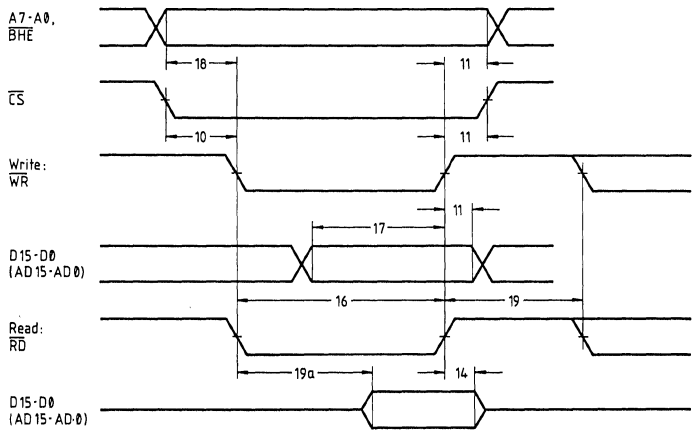


Figure 32
READY Timing (186 mode)

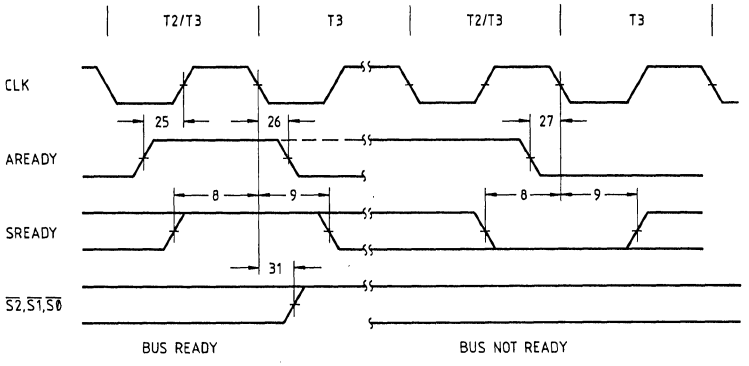
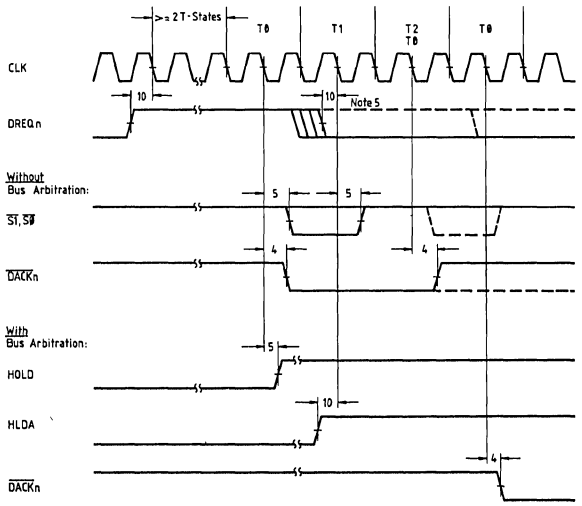


Figure 33
DREQ, DACK Timing (286 mode)



Note 5: The trailing edge of DREQn, as specified in this diagram, is necessary if only one bus cycle should be executed.
A later trailing edge may cause an additional bus cycle (continuous DREQ), if no READY-wait-states are inserted.

Figure 34
DREQ, DACK Timing (186 mode)

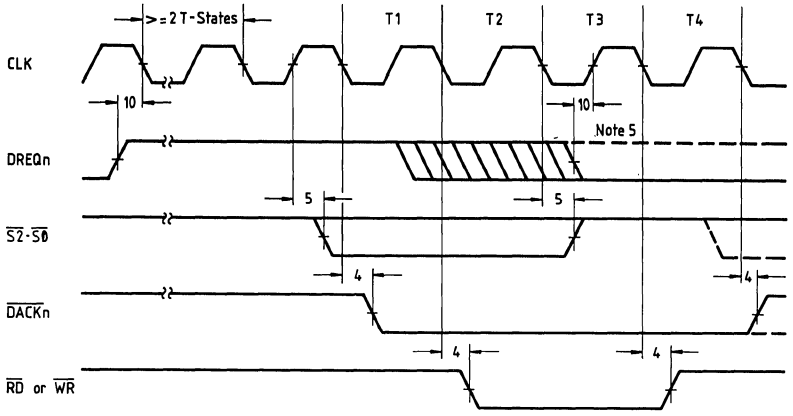


Figure 35
BREL, Bus Tristate Timing (Remote mode)

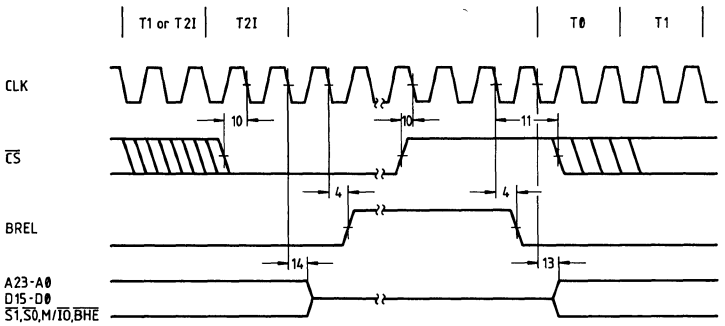


Figure 36
RESET Timing

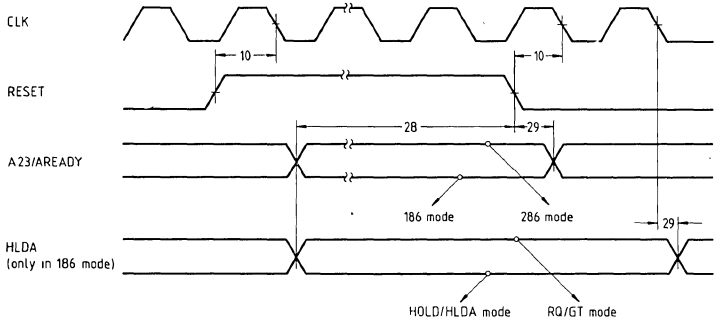


Figure 37
HOLD, HLDA Timing (286 mode)

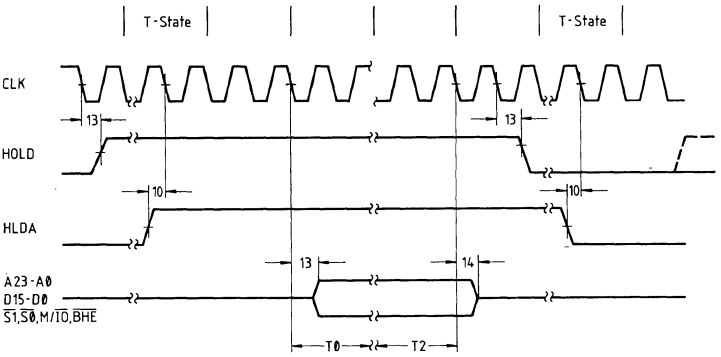


Figure 38
HOLD, HLDA Timing (186 mode)

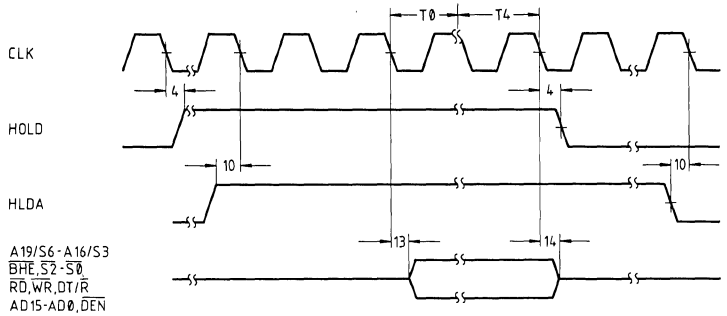


Figure 39
$\overline{RQ}/\overline{GT}$ Timing (8086 mode)

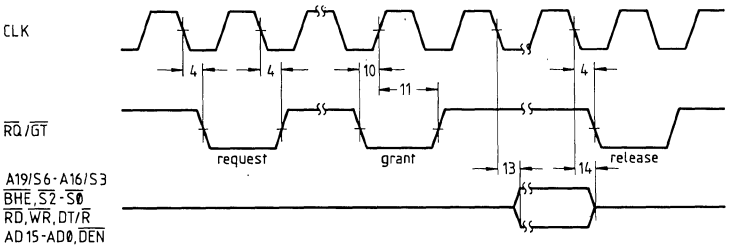


Figure 40
INTOUT, EOD Timing (286 mode)

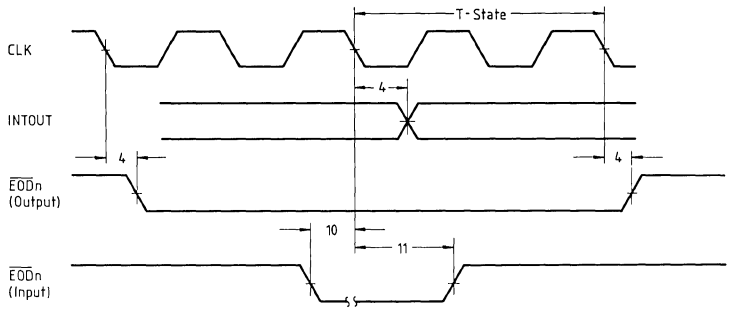
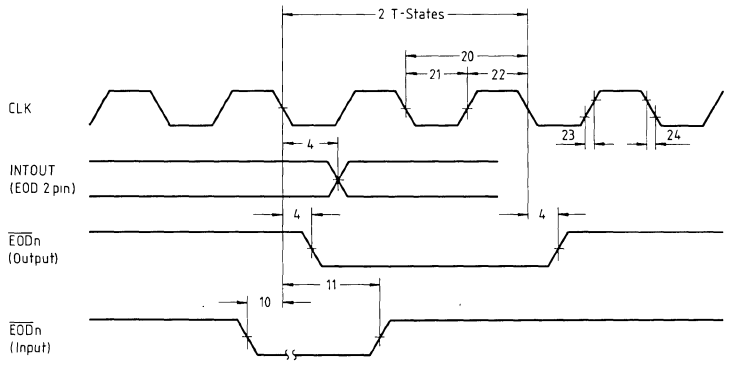


Figure 41
INTOUT, EOD, CLK Timing (186 mode)



SAB 82284
Clock Generator and Ready Interface for SAB 80286 Processors

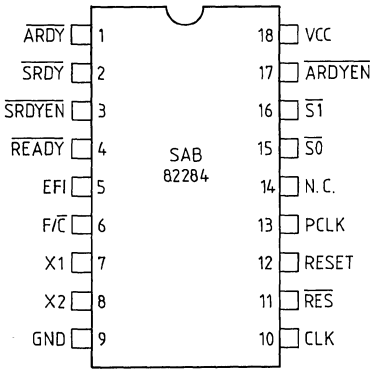
SAB 82284 upto 16 MHz

- Generates System Clock for SAB 80286 Processors
- Uses Crystal or TTL Signal for Frequency Source
- Provides Local READY and Multimaster System Bus READY Synchronization

SAB 82284-6 upto 12 MHz

- 18-Pin Package
- Single +5V Power Supply
- Generates System Reset Output from Schmitt Trigger Input

Pin Configuration



Pin Names

CLK	System Clock
F/C	Frequency/Crystal Select
X1, X2	Crystal In
EFI	External Frequency In
PCLK	Peripheral Clock
ARDYEN	Asynchronous Ready Enable
ARDY	Asynchronous Ready
SRDYEN	Synchronous Ready Enable
SRDY	Synchronous Ready
READY	Ready
S0, S1	Status
RESET	Reset
RES	Reset In
VCC	Power supply (+5V)
GND	Ground (0V)

The SAB 82284 is a bipolar clock generator/driver which provides clock signals for SAB 80286 processors and support components. It also contains logic to supply READY to the CPU from either asynchronous or synchronous sources and synchronous RESET from an asynchronous input with hysteresis.

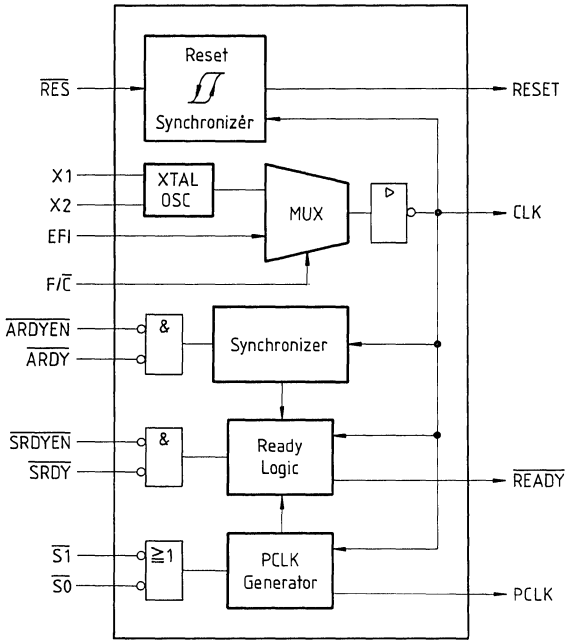
Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
$\overline{ARDY}$	1	I	ASYNCHRONOUS READY is an active LOW input used to terminate the current bus cycle. The $\overline{ARDY}$ input is qualified by $\overline{ARDYEN}$. Inputs to ARDY may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
$\overline{SRDY}$	2	I	SYNCHRONOUS READY is an active LOW input used to terminate the current bus cycle. The $\overline{SRDY}$ input is qualified by the $\overline{SRDYEN}$ input. Setup and hold times must be satisfied for proper operation.
$\overline{SRDYEN}$	3	I	SYNCHRONOUS READY ENABLE is an active LOW input which qualifies $\overline{SRDY}$. $\overline{SRDYEN}$ selects $\overline{SRDY}$ as the source for $\overline{READY}$ to the CPU for the current bus cycle. Setup and hold times must be satisfied for proper operation.
$\overline{READY}$	4	O	READY is an active LOW output which signals the current bus cycle is to be completed. The $\overline{SRDY}$, $\overline{SRDYEN}$, $\overline{ARDY}$, $\overline{ARDYEN}$, $\overline{S1}$, $\overline{S0}$ and $\overline{RES}$ inputs control $\overline{READY}$ as explained later in the $\overline{READY}$ generator section. $\overline{READY}$ is an open collector output requiring an external 300 ohm pullup resistor.
EFI	5	I	EXTERNAL FREQUENCY IN drives CLK when the F/$\overline{C}$ input is strapped HIGH. The EFI input frequency must be twice the desired internal processor clock frequency.
F/$\overline{C}$	6	I	FREQUENCY/CRYSTAL SELECT is a strapping option to select the source for the CLK output. When F/$\overline{C}$ is strapped LOW, the internal crystal oscillator drives CLK. When F/$\overline{C}$ is strapped HIGH, the EFI input drives the CLK output.
X1, X2	7, 8	I	CRYSTAL IN are the pins to which a parallel resonant fundamental mode crystal is attached for the internal oscillator. When F/$\overline{C}$ is LOW, the internal oscillator will drive the CLK output at the crystal frequency. The crystal frequency must be twice the desired internal processor clock frequency.
CLK	10	O	SYSTEM CLOCK is the signal used by the processor and support devices which must be synchronous with the processor. The frequency of the CLK output has twice the desired internal processor clock frequency. CLK can drive both TTL and MOS level inputs.
$\overline{RES}$	11	I	RESET IN is an active LOW input which generates the system reset signal RESET. Signals to $\overline{RES}$ may be applied asynchronously to CLK. A Schmitt trigger input is provided on $\overline{RES}$, so that an RC circuit can be used to provide a time delay. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
RESET	12	O	RESET is an active HIGH output which is derived from the $\overline{RES}$ input. RESET is used to force the system into an initial state. When RESET is active, $\overline{READY}$ will be active (LOW).

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
PCLK	13	O	PERIPHERAL CLOCK is an output which provides a 50% duty cycle clock with 1/2 the frequency of CLK. PLCK will be in phase with the internal processor clock following the first bus cycle after the processor has been reset.
$\overline{S0}$, $\overline{S1}$	15,16	I	STATUS inputs prepare the SAB 82284 for a subsequent bus cycle. $\overline{S0}$ and $\overline{S1}$ synchronize PCLK to the internal processor clock and control $\overline{READY}$. These inputs have pullup resistors to keep them HIGH if nothing is driving them. Setup and hold times must be satisfied for proper operation.
$\overline{ARDYEN}$	17	I	ASYNCHRONOUS READY ENABLE is an active LOW input which qualifies the $\overline{ARDY}$ input. $\overline{ARDYEN}$ selects $\overline{ARDY}$ as the source of ready for the current bus cycle. Inputs to $\overline{ARDYEN}$ may be applied asynchronously to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs.
VCC	18	–	POWER SUPPLY (+5V)
GND	9	–	GROUND (OV)

Block Diagram



Functional Description

Introduction

The SAB 82284 generates the clock, ready, and reset signals required for SAB 80286 processors and support components. The SAB 82284 is packaged in an 18-pin DIP package and contains a crystal-controlled oscillator, MOS clock generator, peripheral clock generator, Multibus ready synchronization logic, and system reset generation logic.

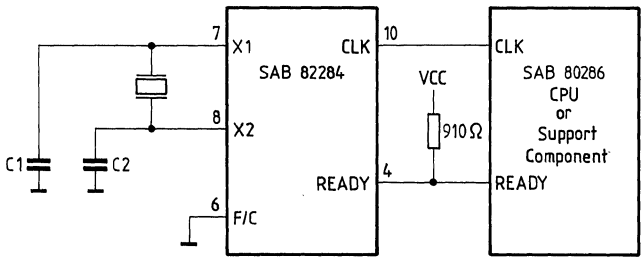
Clock generator

The CLK output provides the basic timing control for an SAB 80286 system. CLK has output characteristics sufficient to drive MOS devices. CLK is generated by either an internal crystal oscillator or an external source as selected by the F/$\overline{C}$ strapping option. When F/$\overline{C}$ is LOW, the crystal oscillator drives the CLK output. When F/$\overline{C}$ is HIGH, the EFI input drives the CLK output. The SAB 82284 provides a second clock output (PCLK) for peripheral devices. PCLK is CLK divided by two. PCLK has a duty cycle of 50% and TTL output drive characteristics. PCLK is normally synchronized to the internal processor clock. After reset, the PCLK signal may be out of phase with the internal processor clock. The $\overline{S1}$ and $\overline{S0}$ signals of the first bus cycle are used to synchronize PCLK to the internal processor clock. The phase of the PCLK output changes by extending its High time beyond one system clock (see waveforms). PCLK is forced HIGH whenever either $\overline{S0}$ or $\overline{S1}$ were active (LOW) for the two previous CLK cycles. PCLK continues to oscillate when both $\overline{S0}$ and $\overline{S1}$ are HIGH.
Since the phase of the internal processor clock will not change except during reset, the phase of PCLK will not change except during the first bus cycle after reset.

Oscillator

The oscillator circuit of the SAB 82284 is a linear Pierce oscillator which requires an external, parallel, resonant, fundamental-mode crystal. The output of the oscillator is internally buffered. The crystal frequency chosen should be twice the required internal processor clock frequency. The crystal should have a typical load capacitance of 32 pF.
X1 and X2 are the oscillator crystal connections. For stable operation of the oscillator, two loading capacitors are recommended, as shown in the figure below. The sum of the board capacitance and loading capacitance should equal the values shown. It is advisable to limit stray board capacitances (not including the effect of the loading capacitors or crystal capacitance) to less than 10pF between the X1 and X2 pins.
Decouple VCC and GND as close to the SAB 82284 as possible.

Recommended Crystal and Ready Connections



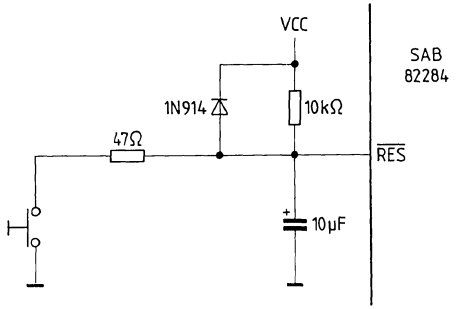
Crystal Frequency	C1 Capacitance	C2 Capacitance
1 to 8MHz	60pF	40pF
8 to 16MHz	25pF	15pF

Reset Operation

The reset logic provides the RESET output to force the system into a known, initial state. When the $\overline{RES}$ input is active (LOW), the RESET output becomes active (HIGH). $\overline{RES}$ is synchronized internally at the falling edge of CLK before generating the RESET output (see waveforms). Synchronization of the $\overline{RES}$ input introduces a one or two CLK delay before affecting the RESET output.

At power up, a system does not have a stable VCC and CLK. To prevent spurious activity, $\overline{RES}$ should be asserted until VCC and CLK stabilize at their operating values. SAB 80286 processors and support components also require their RESET inputs be HIGH a minimum number of CLK cycles. An RC network, as shown below, will keep $\overline{RES}$ LOW long enough to satisfy both needs.

Typical RC RESET Timing Circuit



A Schmitt trigger input with hysteresis on $\overline{RES}$ assures a single transition of RESET with an RC circuit on $\overline{RES}$. The hysteresis separates the input voltage level at which the circuit output switches from HIGH to LOW from the input voltage level at which the circuit output switches from LOW to HIGH. The $\overline{RES}$ HIGH to LOW input transition voltage is lower than the $\overline{RES}$ LOW to HIGH input transition voltage. As long as the slope of the $\overline{RES}$ input voltage remains in the same direction (increasing or decreasing) around the $\overline{RES}$ input transition voltage, the RESET output will make a single transition.

Ready Operation

The SAB 82284 accepts two ready sources for the system ready signal which terminates the current bus cycle. Either a synchronous ($\overline{SRDY}$) or asynchronous ready ($\overline{ARDY}$) source may be used. Each ready input has an enable ($\overline{SRDYEN}$ and $\overline{ARDYEN}$) for selecting the type of ready source required to terminate the current bus cycle. An address decoder would normally select one of the enable inputs.

The figure on synchronous ready mode illustrates the operation of $\overline{SRDY}$ and $\overline{SRDYEN}$. These inputs are sampled on the falling edge of CLK when $\overline{S1}$ and $\overline{S0}$ are inactive and PCLK is HIGH. $\overline{READY}$ is forced active when both $\overline{SRDY}$ and $\overline{SRDYEN}$ are sampled as LOW.

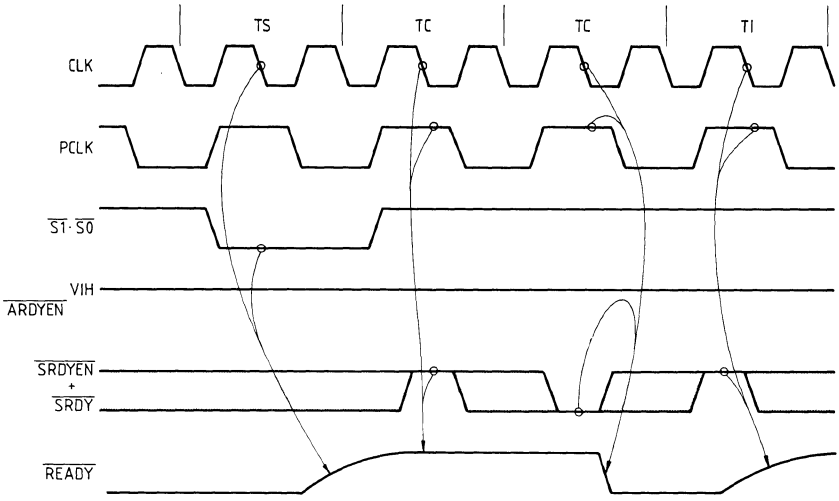
The figure on asynchronous ready mode shows the operation of $\overline{ARDY}$ and $\overline{ARDYEN}$. These inputs are sampled by an internal synchronizer at each falling edge of CLK. The output of the synchronizer is then sampled when PCLK is HIGH. If the synchronizer resolved both the $\overline{ARDY}$ and $\overline{ARDYEN}$ inputs to have been active (LOW), $\overline{READY}$ becomes active (LOW) and the $\overline{SRDY}$ and $\overline{SRDYEN}$ inputs are ignored.

$\overline{READY}$ remains active until either $\overline{S1}$ or $\overline{S0}$ is sampled LOW, or the ready inputs are sampled as inactive.

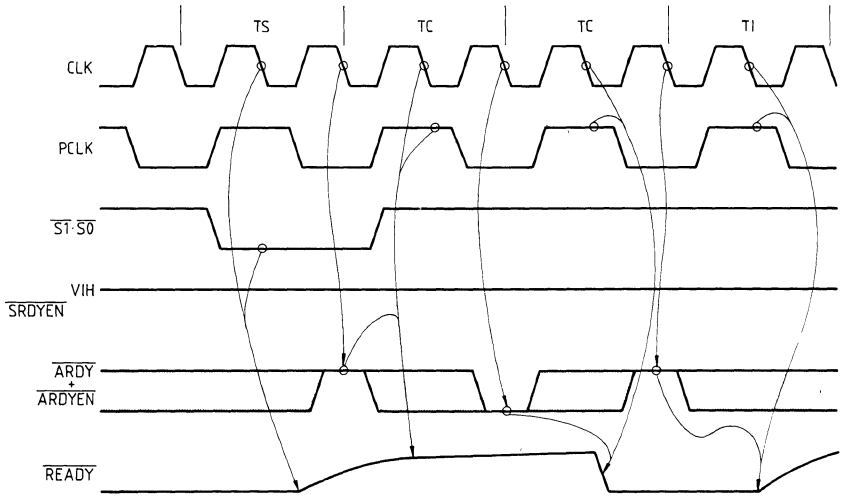
$\overline{READY}$ is enabled (LOW), if either $\overline{SRDY}$ + $\overline{SRDYEN}$ = 0 or $\overline{ARDY}$ + $\overline{ARDYEN}$ = 0 when sampled by the SAB 82284 $\overline{READY}$ generation logic. $\overline{READY}$ will remain active for at least two CLK cycles.

The $\overline{READY}$ output has an open-collector driver allowing other ready circuits to be wire ored with it. The $\overline{READY}$ signal of an SAB 80286 system requires an external 300 ohm pullup resistor. To force the $\overline{READY}$ signal inactive (HIGH) at the start of a bus cycle, the $\overline{READY}$ output floats when either $\overline{S1}$ or $\overline{S0}$ are sampled LOW at the falling edge of CLK. Two system clock periods are allowed for the pullup resistor to pull the $\overline{READY}$ signal to VIH. When RESET is active, $\overline{READY}$ is forced active one CLK later (see waveforms).

Synchronous Ready Operation



Asynchronous Ready Operation



Absolute Maximum Ratings [1)]

Temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
All output and supply voltages	−0.5 to +7V
All input voltages	−1.0 to +5.5V
Power dissipation	1 Watt

D.C. Characteristics

TA = 0 to 70°C, VCC = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
IF	Forward input current	–	−0.5	mA	VF = 0.45V
IR	Reverse input current		50	µA	VR = 5.25V
VC	Input forward clamp voltage		−1.0	V	IC = −5mA
ICC	Power supply current		145	mA	–
VIL	Input LOW voltage		0.8	V	
VIH	Input HIGH voltage	2.0	–		
VOL, VCL	Output LOW voltage	–	0.45		IOL = 5mA
VCH	CLK output HIGH voltage	4.0	–		IOH = −1mA
VOH	Output HIGH voltage	2.4			
VIHR	$\overline{RES}$ input HIGH voltage	2.6			–
VIHR − VILR	$\overline{RES}$ input hysteresis	0.25			
CI	Input capacitance	–	10	pF	

[1)] Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

A.C. Characteristics SAB 82284

TA = 0 to 70°C, VCC = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
T1	EFI to CLK delay	–	30	ns	
T2	EFI LOW time	32	–		at 1.5V CL = 150pF IOL = 5mA
T3	EFI HIGH time	28			
T4	CLK period	62	500		
T5	CLK LOW time	15	–		at 0.6V see [1]
T6	CLK HIGH time	20			at 3.8V
T7	CLK rise time	–	10		from 1.0V to 3.5V see [2]
T8	CLK fall time				from 3.5V to 1.0V
T9	Status setup time	22.5	–		at 0.8V and 2.0V on input and 0.8V on CLK
T10	Status hold time	0			
T11	$\overline{SRDY}$ + $\overline{SRDYEN}$ setup time	15			
T12	$\overline{SRDY}$ + $\overline{SRDYEN}$ hold time	0			
T13	$\overline{ARDY}$ + $\overline{ARDYEN}$ setup time [4]				
T14	$\overline{ARDY}$ + $\overline{ARDYEN}$ hold time [4]	16			
T15	$\overline{RES}$ setup time [4]				
T16	$\overline{RES}$ hold time [4]	0			
T17	$\overline{READY}$ inactive delay	5			at 0.8V CL = 150pF IOL = 20mA
T18	$\overline{READY}$ active delay	0	24		
T19	PCLK delay		40		at 0.8V on CLK to see [3]
T20	RESET delay				0.8V or 2.0V on output
T21	PCLK low time	T4–13	–		at 0.6V see [3]
T22	PCLK high time				at 3.8V

[1] CL = 150pF, IOL = 5mA. With either the internal oscillator with the recommended crystal and load or with the EFI input meeting specification T2 and T3.
[2] CL = 150pF, IOL = 5mA
[3] CL = 75pF, IOL = 5mA
[4] This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific clock edge.

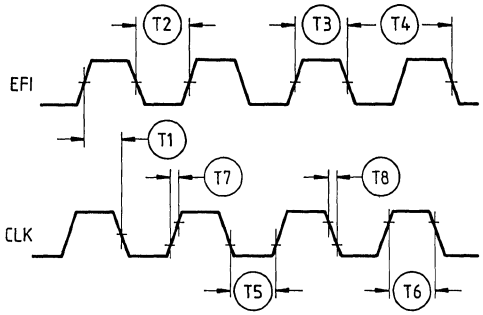
A.C. Characteristics SAB 82284-6

TA = 0 to 70°C, VCC = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
T1	EFI to CLK delay	–	35	ns	
T2	EFI LOW time	35	–		at 1.5V CL = 150pF IOL = 5mA
T3	EFI HIGH time	35			
T4	CLK period	83	500		
T5	CLK LOW time	20	–		at 0.6V see [1]
T6	CLK HIGH time	25			at 3.8V
T7	CLK rise time	–	10		from 1.0V to 3.5V see [2]
T8	CLK fall time				from 3.5V to 1.0V
T9	Status setup time	28	–		at 0.8V and 2.0V on input and 0.8V on CLK
T10	Status hold time	0			
T11	$\overline{SRDY}$ + $\overline{SRDYEN}$ setup time	25			
T12	$\overline{SRDY}$ + $\overline{SRDYEN}$ hold time	0			
T13	$\overline{ARDY}$ + $\overline{ARDYEN}$ setup time [4]	5			
T14	$\overline{ARDY}$ + $\overline{ARDYEN}$ hold time [4]	30			
T15	$\overline{RES}$ setup time [4]	25			
T16	$\overline{RES}$ hold time [4]	10			
T17	$\overline{READY}$ inactive delay	5			at 0.8V CL = 150pF IOL = 20mA
T18	$\overline{READY}$ active delay	0	45		at 0.8V on CLK to see [3]
T19	PCLK delay				
T20	RESET delay		50		0.8V or 2.0V on output
T21	PCLK low time	T4–20	–		at 0.6V see [3]
T22	PCLK high time				at 3.8V

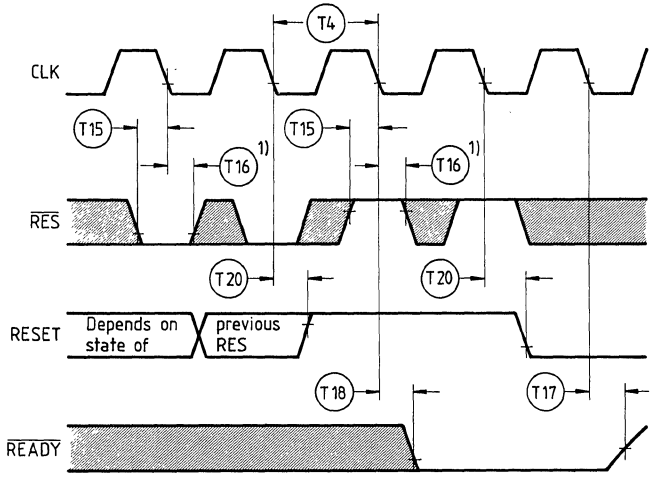
[1] CL = 150pF, IOL = 5mA. With either the internal oscillator with the recommended crystal and load or with the EFI input meeting specification T2 and T3.
[2] CL = 150pF, IOL = 5mA
[3] CL = 75pF, IOL = 5mA
[4] This is an asynchronous input. This specification is given for testing purposes only, to assure recognition at a specific clock edge.

CLK versus EFI



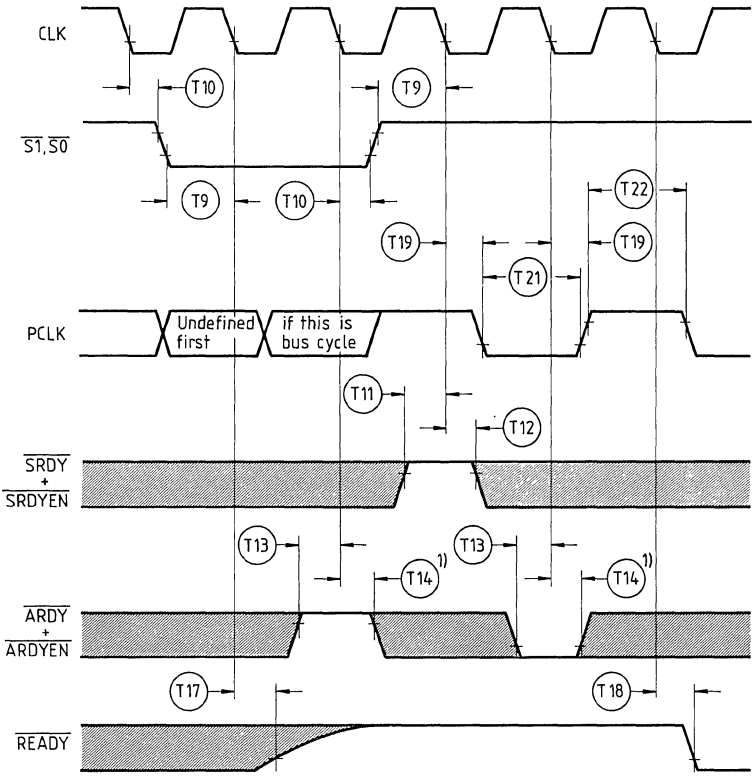
The EFI input LOW and HIGH times as shown are required to guarentee the CLK LOW and HIGH times shown.

RESET and $\overline{\text{READY}}$ Timing versus $\overline{\text{RES}}$ with $\overline{\text{S1}}$ and $\overline{\text{S0}}$ HIGH



[1] This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

$\overline{\text{READY}}$ and PCLK Timing with $\overline{\text{RES}}$ HIGH



1) This is an asynchronous input. The setup and hold times shown are required to guarantee the response shown.

SAB 82288 Bus Controller for SAB 80286 Processors

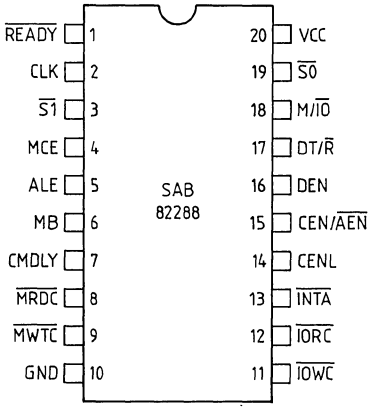
SAB 82288 upto 16 MHz

- Provides Commands and Control for Local and System Bus
- Offers Wide Flexibility in System Configurations
- Flexible Command Timing

SAB 82288-6 upto 12 MHz

- Optimal Multibus™-Compatible Timing
- Control Drivers with 16 mA IOL and Tri-State Command Drivers with 32 mA IOL
- Single +5V Supply

Pin Configuration



Pin Names

CLK	System Clock
$\overline{S0}$, $\overline{S1}$	Bus Cycle Status
M/$\overline{IO}$	Memory or I/O Select
MB	Multibus Mode Select
CENL	Command Enable Latched
CMDLY	Command Delay
$\overline{READY}$	Ready
CEN/$\overline{AEN}$	Command Enable/Address Enable
ALE	Address Latch Enable
MCE	Master Cascade Enable
DEN	Data Enable
DT/$\overline{R}$	Data Transmit/Receive
$\overline{IOWC}$	I/O Write Command
$\overline{IORC}$	I/O Read Command
$\overline{MWTC}$	Memory Write Command
$\overline{MRDC}$	Memory Read Command
$\overline{INTA}$	Interrupt Acknowledge
VCC	Power supply (+5V)
GND	Ground (0V)

The SAB 82288 bus controller is a 20-pin MYMOS component for use in SAB 80286 microsystems. The bus controller provides command and control outputs with flexible timing options. Separate command outputs are used for memory and I/O devices. The data bus is controlled with separate data enable and direction control signals. Two modes of operation are possible via a strapping option: Multibus-compatible bus cycles, and high-speed bus cycles.

Multibus™ is a trademark of Intel Corporation.

Pin Definitions and Functions

<table>
<tr><th>Symbol</th><th>Number</th><th>Input (I)
Output (O)</th><th>Function</th></tr>
<tr><td>$\overline{\text{READY}}$</td><td>1</td><td>I</td><td>READY indicates the end of the current bus cycle. $\overline{\text{READY}}$ is an active LOW input. Multibus mode requires at least one wait state to allow the command outputs to become active. $\overline{\text{READY}}$ must be LOW during reset, to force the SAB 82288 into the idle state. Setup and hold times must be met for proper operation.</td></tr>
<tr><td>CLK</td><td>2</td><td>I</td><td>SYSTEM CLOCK provides the basic timing control for the SAB 82288 in an SAB 80286 microsystem. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and control outputs change.</td></tr>
<tr><td>$\overline{\text{S0}}$, $\overline{\text{S1}}$</td><td>3, 19</td><td>I</td><td>BUS CYCLE STATUS starts a bus cycle and, along with M/$\overline{\text{IO}}$, defines the type of bus cycle. These inputs are active LOW. A bus cycle is started when either $\overline{\text{S1}}$ or $\overline{\text{S0}}$ is sampled LOW at the falling edge of CLK. These inputs have pullups sufficient to hold them HIGH when nothing drives them. Setup and hold times must be met for proper operation.
<table>
<tr><th colspan="4">SAB 80286 bus cycle status definition</th></tr>
<tr><th>M/$\overline{\text{IO}}$</th><th>$\overline{\text{S1}}$</th><th>$\overline{\text{S0}}$</th><th>Type of bus cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupr acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>I/O read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>None; idle</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Halt or shutdown</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Memory read</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory write</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>None; idle</td></tr>
</table></td></tr>
<tr><td>MCE</td><td>4</td><td>O</td><td>MASTER CASCADE ENABLE signals that a cascade address from a master SAB 8259A interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active HIGH. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.</td></tr>
<tr><td>ALE</td><td>5</td><td>O</td><td>ADDRESS LATCH ENABLE controls the address latches used to hold an address stable during a bus cycle. This control output is active HIGH. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.</td></tr>
<tr><td>MB</td><td>6</td><td>I</td><td>MULTIBUS MODE SELECT determines timing of the command and control outputs. When HIGH, the bus controller operates in Multibus mode. When LOW, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/$\overline{\text{AEN}}$ input pin is selected by this signal. This input is intended to be a strapping option and not dynamically changed. This input may be connected to VCC or GND.</td></tr>
</table>

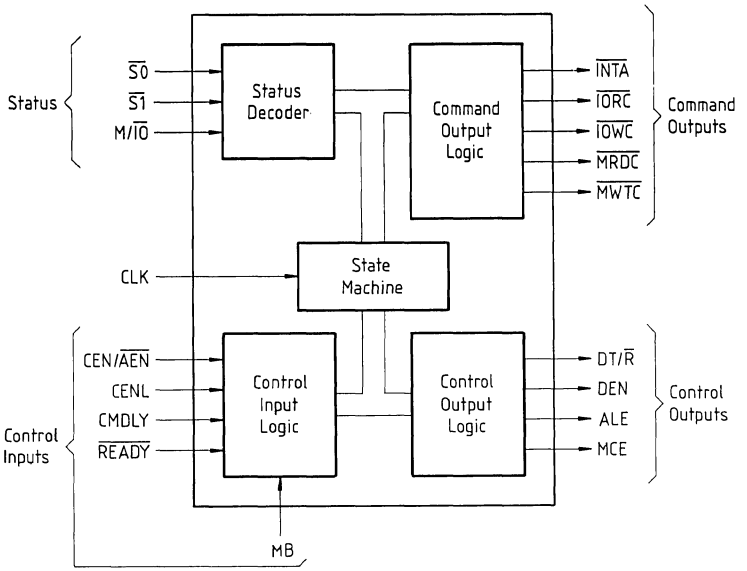
Pin Definitions and Function (continued)

Symbol	Number	Input (I) Output (O)	Function
CMDLY	7	I	COMMAND DELAY allows delaying the start of a command. CMDLY is an active HIGH input. If sampled HIGH, the command output is not activated and CMDLY is again sampled at the next CLK cycle. When sampled LOW the selected command is enabled. If $\overline{\text{READY}}$ is detected LOW before the command output is activated, the SAB 82288 will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be connected to GND if no delays are required before starting a command.
$\overline{\text{MRDC}}$	8	O	MEMORY READ COMMAND instructs the memory device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{MWTC}}$	9	O	MEMORY WRITE COMMAND instructs a memory device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{IOWC}}$	11	O	I/O WRITE COMMAND instructs an I/O device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{IORC}}$	12	O	I/O READ COMMAND instructs an I/O device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
$\overline{\text{INTA}}$	13	O	INTERRUPT ACKNOWLEDGE tells an interrupting device that its interrupt request is being acknowledged. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{\text{READY}}$ controls when it becomes inactive.
CENL	14	I	COMMAND ENABLE LATCHED is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENL is an active HIGH input latched internally at the start of each bus cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be connected to VCC to select this SAB 82288 for all transfers. No control inputs affect CENL. Setup and hold times must be met for proper operation.

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
CEN/$\overline{AEN}$	15	I	COMMAND ENABLE/ADDRESS ENABLE controls the command and DEN outputs of the bus controller. CEN/$\overline{AEN}$ inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. This input may be connected to VCC or GND. When MB is HIGH this pin has the $\overline{AEN}$ function. $\overline{AEN}$ is an active LOW input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit Tri-state OFF and become inactive (HIGH). $\overline{AEN}$ HIGH indicates that the CPU does not have control of the shared bus and forces the command outputs into Tri-state OFF and DEN inactive (LOW). $\overline{AEN}$ would normally be controlled by an SAB 82289 bus arbiter which activates $\overline{AEN}$ when that arbiter owns the bus to which the bus controller is attached. When MB is LOW this pin has the CEN function. CEN is an unlatched active HIGH input which allows the bus controller activate its command and DEN outputs. With MB LOW, CEN LOW forces the command and DEN outputs inactive but does not Tri-state them.
DEN	16	O	DATA ENABLE controls when data transceivers connected to the local data bus should be enabled. DEN is an active HIGH control output. DEN is delayed for write cycles in the Multibus mode.
DT/$\overline{R}$	17	O	DATA TRANSMIT/RECEIVE establishes the direction of data flow to or from the local data bus. When HIGH, this control output indicates that a write bus cycle is being performed. A LOW indicates a read bus cycle. DEN is always inactive when DT/$\overline{R}$ changes states. This output is HIGH when no bus cycle is active. DT/$\overline{R}$ is not affected by any of the control inputs.
M/$\overline{IO}$	18	I	MEMORY OR I/O SELECT determines whether the current bus cycle is in the memory space or I/O space. When LOW, the current bus cycle is in the I/O space. Setup and hold times must be met for proper operation.
VCC	20	–	POWER SUPPLY (+5V)
GND	10	–	GROUND (0V)

Block Diagram



Functional Description

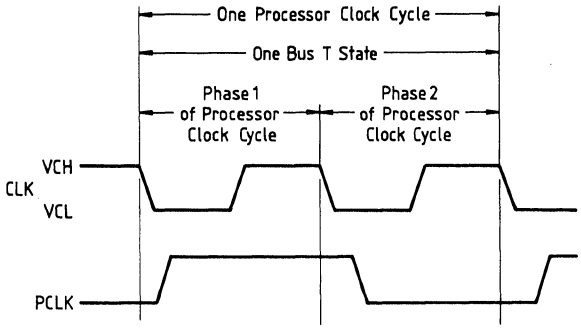
Introduction

The SAB 82288 bus controller is used in SAB 80286 systems to provide address latch control, data transceiver control, and standard level-type command outputs. The command outputs are timed and have sufficient drive capabilities for large TTL buses and meet all IEEE-796 requirements for Multibus. A special Multibus mode is provided to statisfy all address/data setup and hold time requirements. Command timing may be tailored to special needs via a CMDLY input to determine the start of a command and $\overline{\text{READY}}$ to determine the end of a command.
Connection to multiple buses is supported with a latched enable input (CENL). An address decoder can determine which, if any, bus controller should be enabled for the bus cycle. This input is latched to allow an address decoder to take full advantage of the pipelined timing on the SAB 80286 local bus.
Buses shared by several bus controllers are supported. An $\overline{\text{AEN}}$ input prevents the bus controller from driving the shared bus command and data signals except when enabled by an external bus arbiter such as the SAB 82289.
Separate DEN and DT/$\overline{\text{R}}$ outputs control the data transceivers for all buses. Bus contention is eliminated by disabling DEN before changing DT/$\overline{\text{R}}$. The DEN timing allows sufficient time for Tri-state bus drivers to enter Tri-state OFF before enabling other drivers onto the same bus.
The term CPU refers to any SAB 80286 processor or SAB 80286 support component which may become an SAB 80286 local bus master and thereby drive the SAB 82288 status inputs.

Processor Cycle Definition

Any CPU which drives the local bus uses an internal clock which is one half the frequency of the system clock (CLK) (see figure below). Knowledge of the phase of the local bus master's internal clock is required for proper operation of the SAB 80286 local bus. The local bus master informs the bus controller of its internal clock phase when it asserts the status signals. Status signals are always asserted in phase 1 of the local bus master's internal clock.

CLK Relationship to the Processor Clock and Bus T-States

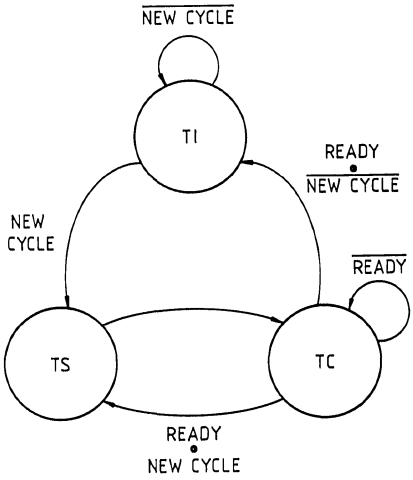


Bus State Definition

The SAB 82288 bus controller has three bus states (see figure below): Idle (TI), Status (TS), and Command (TC). Each bus state is two CLK cycles long. Bus state phases correspond to the internal CPU processor clock phases.

The TI bus state occurs when no bus cycle is currently active on the SAB 80286 local bus. This state may be repeated indefinitely. When control of the local bus is being passed between masters, the bus remains in the TI state.

Bus States



Bus Cycle Definition

The $\overline{S1}$ and $\overline{S0}$ inputs signal the start of a bus cycle. When either input becomes LOW, a bus cycle is started. The TS bus state is defined to be the two CLK cycles during which either $\overline{S1}$ or $\overline{S0}$ is active (see figure on bus cycle definition). These inputs are sampled by the SAB 82288 at every falling edge of CLK. When either $\overline{S1}$ or $\overline{S0}$ is sampled LOW, the next CLK cycle is considered the second phase of the internal CPU clock cycle.
The local bus enters the TC bus state after the TS state. The shortest bus cycle may have one TS state and one TC state. Longer bus cycles are formed by repeating TC states. A repeated TC bus state IS called a wait state.

The $\overline{READY}$ input determines whether the current TC bus state is to be repeated. The $\overline{READY}$ input has the same timing and effect for all bus cycles. $\overline{READY}$ is sampled at the end of each TC bus state to see if it is active. If sampled HIGH, the TC bus state is repeated. This is called inserting a wait state. The control and command outputs do not change during wait states.
When $\overline{READY}$ is sampled LOW, the current bus cycle is terminated. Note that the bus controller may enter the TS bus state directly from TC if the status lines are sampled active at the next falling edge of CLK.

Bus Cycle Definition

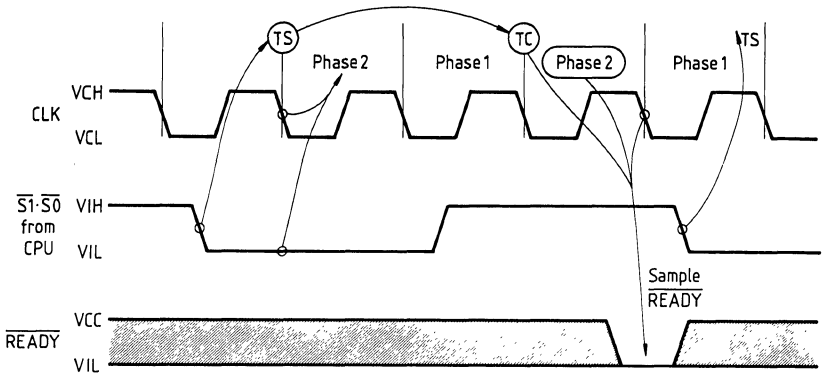


Table 2 Command and Control Output for each Type Bus Cycle

Type of bus cycle	M/IO	S1	S0	Command activated	DT/R state	ALE, DEN issued?	MCE issued?
Interrupt acknowledge	0	0	0	INTA	LOW	yes	yes
VO read	0	0	1	IORC	LOW	yes	no
VO write	0	1	0	IOWC	HIGH	yes	no
None; idle	0	1	1	none	HIGH	no	no
Halt/shutdown	1	0	0	none	HIGH	no	no
Memory read	1	0	1	MRDC	LOW	yes	no
Memory Write	1	1	0	MWTC	HIGH	yes	no
None; idle	1	1	1	none	HIGH	no	no

Operating Modes

Two types of buses are supported by the SAB 82288: Multibus and non-Multibus. When the MB input is strapped HIGH, Multibus timing is used. In Multibus mode, the SAB 82288 delays command and data activation to meet IEEE-796 requirements on address to command active and write data to command active setup timing. Multibus mode requires at least one wait state in the bus cycle since the command outputs are delayed. The non-Multibus mode does not delay any outputs and does not require wait states. The MB input affects the timing of the command and DEN outputs.

Command and Control Outputs

The type of bus cycle performed by the local bus master is encoded in the M/$\overline{IO}$, $\overline{S1}$, and $\overline{S0}$ inputs. Different command and control outputs are activated depending on the type of bus cycle. Table 2 indicates the cycle decoding done by the SAB 82288 and the effect on command, DT/$\overline{R}$, ALE, DEN, and MCE outputs.

Bus cycles come in three forms: read, write, and halt. Read bus cycle include memory read, I/O read, and interrupt acknowledge. The timing of the associated read command outputs ($\overline{MRDC}$, $\overline{IORC}$, and $\overline{INTA}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical for all read bus cycles. Read cycles differ only in which command output is activated. The MCE control output is only asserted during interrupt acknowledge cycles.

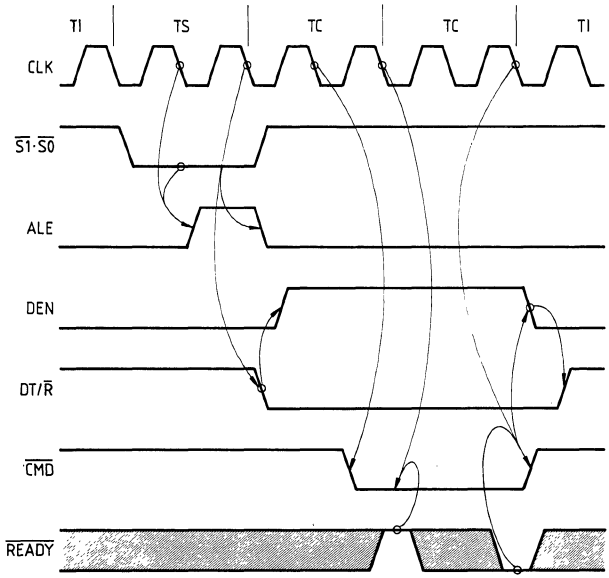
Write bus cycles activate different control and command outputs with different timing than read bus cycles. Memory write and I/O write are write bus cycles whose timing for command outputs ($\overline{MWTC}$ and $\overline{IOWC}$), control outputs (ALE, DEN, DT/$\overline{R}$) and control inputs (CEN/$\overline{AEN}$, CENL, CMDLY, MB, and $\overline{READY}$) are identical. They differ only in which command output is activated.

Halt bus cycles are different because no command or control output is activated. All control inputs are ignored until the next bus cycle is started via $\overline{S1}$ and $\overline{S0}$.

The basic command and control output timing for read and write bus cycles is shown in the next five figures. Halt bus cycles are not shown since they activate no outputs. The basic idle-read-idle and idle-write-idle bus cycles are shown. The signal label $\overline{CMD}$ represents the appropriate command output for the bus cycle. For those five figures, the CMDLY input is connected to GND and CENL to VCC. The effects of CENL and CMDLY are described later in the section on control inputs.

The next two figures show non-Multibus cycles. MB is connected to GND while CEN is connected to VCC. The figure below shows a read cycle with no wait states while the figure on the next page shows a write cycle with one wait state. The $\overline{READY}$ input is shown to illustrate how wait states are added.

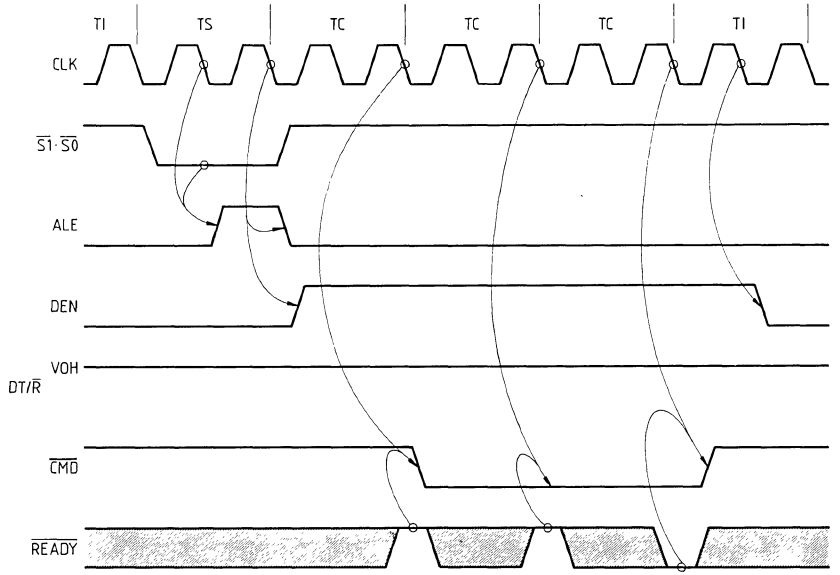
Idle-Read-Idle Bus Cycles with MB = 0



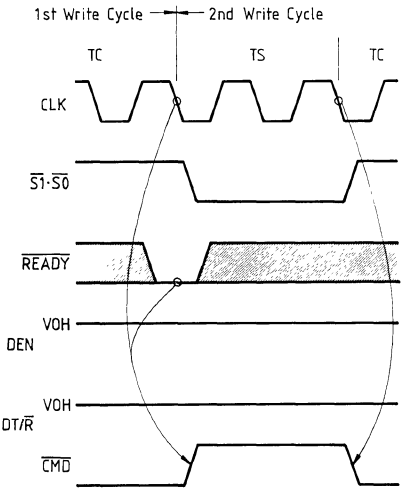
Bus cycles can occur back-to-back with no TI bus states between TC and TS. Back-to-back cycles do not affect the timing of the command and control outputs. Command and control outputs always reach the states shown for the same clock edge (within TS, TC, or following bus state) of a bus cycle. A special case in control timing occurs for back-to-back write cycles with MB = 0. In this case, DT/$\overline{R}$ and DEN remain HIGH between the bus cycles (see respective idle-read-idle cycle diagram). The command and ALE output timing does not change.

The figures on page 10 show a Multibus cycle with MB = 1. $\overline{AEN}$ and CMDLY are connected to GND. The effects of CMDLY and $\overline{AEN}$ are described later in the section on control inputs. The top figure shows a read cycle with one wait state and the figure below shows a write cycle with two wait states. The second wait state of the write cycle is shown only for example purposes and is not required. The $\overline{READY}$ input is shown to illustrate how wait states are added.

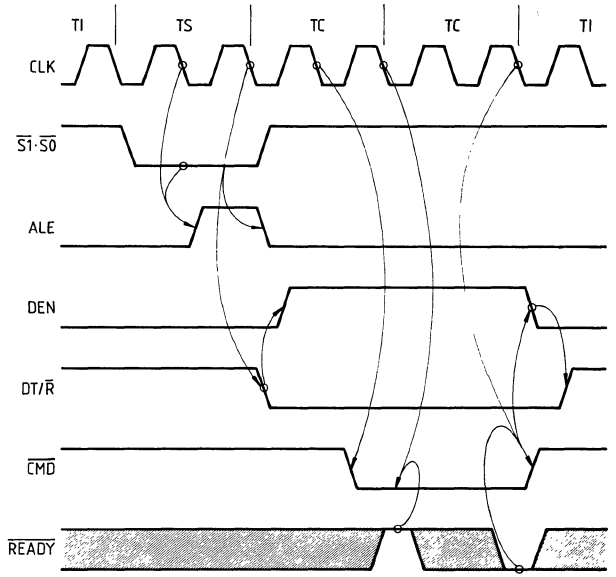
Idle-Write-Idle Bus Cycles with MB = 0



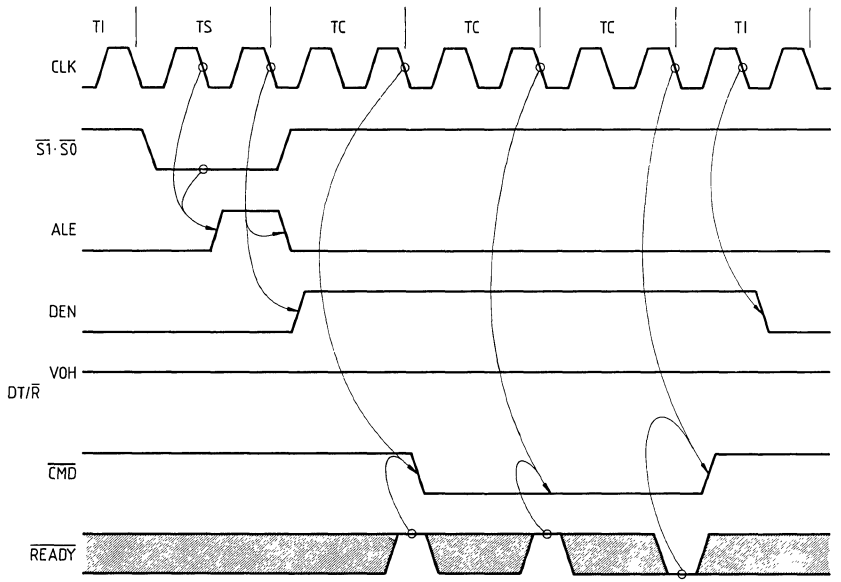
Write-Write Bus Cycles with MB = 0



Idle-Read-Idle Bus Cycles with MB = 1



Idle-Write-Idle Bus Cycles with MB = 1



The MB control input affects the timing of the command and DEN outputs. These outputs are automatically delayed in Multibus mode to satisfy three requirements:

1) 50 ns minimum setup time for valid address before any command output becomes active.
2) 50 ns minimum setup time for valid write data before any write command output becomes active.
3) 65 ns maximum time from when any read command becomes inactive until the slave's read data drivers reach Tri-state OFF.

Three signal transitions are delayed by MB = 1 as compared to MB = 0:

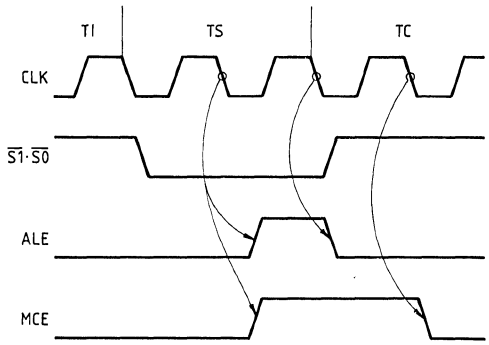
1) The HIGH to LOW transition of the read command outputs ($\overline{IORC}$, $\overline{MRDC}$, and $\overline{INTA}$) is delayed one CLK cycle.
2) The HIGH to LOW transition of the write command outputs ($\overline{IOWC}$ and $\overline{MWTC}$) is delayed two CLK cycles.
3) The LOW to HIGH transition of DEN for write cycles is delayed one CLK cycle.

Back to back bus cycles with MB = 1 do not change the timing of any of the command or control outputs. DEN always becomes inactive between bus cycles with MB = 1.

Except for a halt or shutdown bus cycle, ALE will be issued during the second half of TS for any bus cycle. ALE becomes inactive at the end of the TS to allow latching the address to keep it stable during the entire bus cycle. The address outputs may change during phase 2 of any TC bus state. ALE is not affected by any control input.

The figure below shows how MCE is timed during interrupt acknowledge (INTA) bus cycles. MCE is one CLK cycle longer than ALE to hold the cascade address from a master SAB 8259A valid after the falling edge of ALE. With the exception of the MCE control output, an INTA bus cycle is identical in timing with a read bus cycle. MCE is not affected by any control input.

MCE Operation for an INTA Bus Cycle



Control Inputs

The control inputs can alter the basic timing of command outputs, allow interfacing to multiple buses, and share a bus between different masters. For many SAB 80286 systems, each CPU will have more than one bus which may be used to perform a bus cycle. Normally, a CPU will only have one bus controller active for each bus cycle. Some buses may be shared by more than one CPU (i.e. Multibus) requiring only one of them use the bus at a time.

Systems with multiple and shared buses use two control input signals of the SAB 82288 bus controller, CENL and $\overline{AEN}$ (see figure on system use of those signals). CENL enables the bus controller to control the current bus cycle. The $\overline{AEN}$ input prevents a bus controller from driving its command outputs. $\overline{AEN}$ HIGH means that another bus controller may be driving the shared bus.

In the figure on the $\overline{AEN}$ and CENL signal, two buses are shown: a local bus and a Multibus. Only one bus is used for each CPU bus cycle. The CENL inputs of the bus controllers select which bus controller is to perform the bus cycle. An address decoder determines which bus to use for each bus cycle. The SAB 82288 connected to the shared Multibus must be selected by CENL and be given access to the Multibus by $\overline{AEN}$ before it will begin a Multibus operation.

CENL must be sampled HIGH at the end of the TS bus state (see waveforms) to enable the bus controller to activate its command and control outputs. If sampled LOW the commands and DEN will not go active and DT/$\overline{R}$ will remain HIGH. The bus controller will ignore the CMDLY, CEN, and $\overline{READY}$ inputs until another bus cycle is started via $\overline{S1}$ and $\overline{S0}$. Since an address decoder is commonly used to identify which bus is required for each bus cycle, CENL is latched to avoid the need for latching its input.

The CENL input can affect the DEN control output. When MB = 0, DEN normally becomes active during phase 2 of TS in write bus cycles. This transition occurs before CENL is sampled. If CENL is sampled LOW, the DEN output will be forced LOW during TC as shown in the timing waveforms.

When MB = 1, CEN/$\overline{AEN}$ becomes $\overline{AEN}$, $\overline{AEN}$ controls when the bus controller command outputs enter and exit Tri-state OFF. $\overline{AEN}$ is intended to be driven by a bus arbiter, like the SAB 82289, which assures only one bus controller is driving the shared bus at any time. When $\overline{AEN}$ makes a LOW to HIGH transition, the command outputs immediately enter Tri-state OFF and DEN is forced inactive. An inactive DEN should force the local data transceivers connected to the shared data bus into Tri-state OFF (see next figure). The LOW to HIGH transition of $\overline{AEN}$ should only occur during TI or TS bus states.

The HIGH to LOW transition of $\overline{AEN}$ signals that the bus controller may now drive the shared bus command signals. Since a bus cycle may be active or be in the process of starting, $\overline{AEN}$ can become active during any T-state. $\overline{AEN}$ LOW immediately allows DEN to go to the appropriate state. Three CLK

edges later, the command outputs will go active (see timing waveforms). The Multibus requires this delay for the address and data to be valid on the bus before the commands become active.

When MB = 0, CEN/$\overline{\text{AEN}}$ becomes CEN. CEN is an asynchronous input which immediately affects the command and DEN outputs. When CEN makes a HIGH to LOW transition, the commands and DEN are immediately forced inactive. When CEN makes a LOW to HIGH transition, the commands and DEN outputs immediately go to the appropriate state (see timing waveforms). $\overline{\text{READY}}$ must still become avtive to terminate a bus cycle if CEN remains LOW for a selected bus controller (CENL was latched HIGH).

Some memory or I/O systems may require more address or write data setup time to command active than provided by the basic command output timing. To provide flexible command timing, the CMDLY input can delay the activation of command outputs. The CMDLY input must be sampled LOW to activate the command outputs. CMDLY does not affect the control outputs ALE, MCE, DEN, and DT/$\overline{\text{R}}$.

CMDLY is first sampled on the falling edge of the CLK ending TS. If sampled HIGH, the command output is not activated, and CMDLY is again sampled on the next falling edge of CLK. Once sampled LOW, the proper command output becomes active immediately if MB = 0. If MB = 1, the proper command goes active no earlier than shown in the figures on page 10.

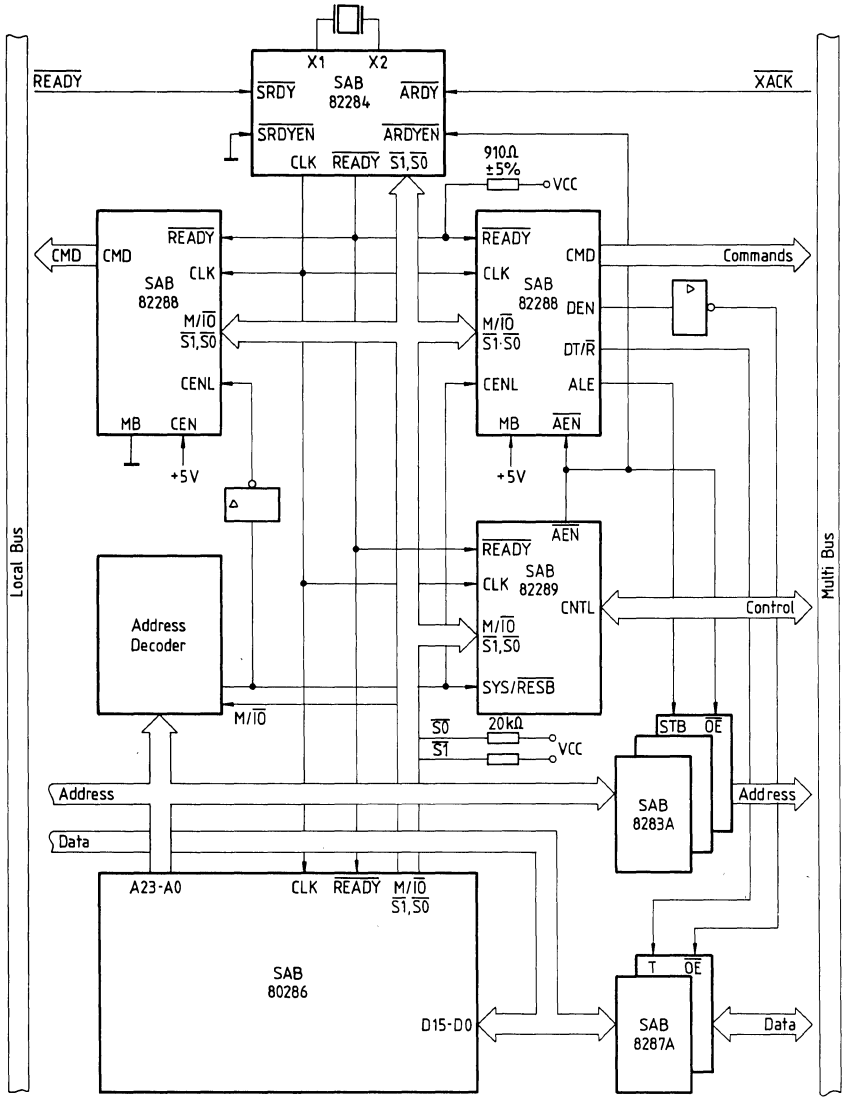
$\overline{\text{READY}}$ can terminate a bus cycle before CMDLY allows a command to be issued. In this case no commands are issued and the bus controller will deactivate DEN and DT/$\overline{\text{R}}$ in the same manner as if a command had been issued.

Waveforms

The waveforms show the timing relationships of inputs and outputs and do not show all possible transitions of all signals in all modes. Instead, all signal timing relationships are shown via the general cases. Special cases are shown when needed. The waveforms provide some functional descriptions of the SAB 82288; however, most functional descriptions are provided in the figures of section Functional Description.

To find the timing specification for a signal transition in a particular mode, first look for a special case in the waveforms. If no special case applies, then use a timing specification for the same or related function in another mode.

System Use of $\overline{AEN}$ and CENL



Absolute Maximum Ratings [1]

Ambient temperature under bias	0 to 70°C
Storage temperature	−65 to +150°C
Voltage on any pin with respect to GND	−0.5 to +7V
Power dissipation	1 W

DC Characteristics

TA = 0 to 70°C, VCC = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
ICC	Power supply current	–	100	mA	
IF	Forward input current CLK input Other inputs		−1 −5		VF = 0.45V
IR	Reverse input current		50	µA	VR = VCC
VOL	LOW output voltage Command outputs Control outputs		0.45	V	IOL = 32mA IOL = 16mA
VOH	HIGH output voltage Command outputs Control outputs	2.4	–		IOH = −5mA IOH = −1mA
VIL	LOW input voltage	−0.5	0.8		–
VCL	CLK LOW input voltage		0.6		
VIH	HIGH input voltage	2.0	VCC +0.5		
VCH	CLK HIGH input voltage	3.9			
IOFF	Output off current	–	100	µA	
CCLK	CLK input capacitance		10	pF	
CI	Input capacitance				

1) Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC Characteristics SAB 82288

TA = 0 to 70°C, VCC = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
T1	CLK period	62.5	250	ns	at 1.5V
T2	CLK HIGH time	20	235		at 3.9V
T3	CLK LOW time	15	230		at 0.6V
T4	CLK fall time	–	10		3.5 to 1.0V
T5	CLK rise time				1.0 to 3.5V
T6	M/$\overline{IO}$ and status setup time	22.5	–		from 0.8 or 2.0V on input to 0.8V on CLK
T7	M/$\overline{IO}$ and status hold time	0			
T8	CENL setup time	20			
T9	CENL hold time	0			
T10	$\overline{READY}$ setup time	38.5			
T11	$\overline{READY}$ hold time	25			
T12	CMDLY setup time	20			
T13	CMDLY hold time	0			
T14	$\overline{AEN}$ setup time 1)	25			
T15	$\overline{AEN}$ hold time 1)	0			
T16	ALE, MCE active delay	3	15		
T17	ALE, MCE inactive delay	–	20		
T18	DEN (WRITE) inactive from CENL		35		
T19	DT/$\overline{R}$ LOW from CLK		20		
T20	DEN (READ) active from DT/$\overline{R}$	10	50		from 0.8V on CLK to 0.8 or 2.0V on output IOL = 16mA IOH = −1mA CL = 150pF
T21	DEN (READ) inactive delay	3	35		
T22	DT/$\overline{R}$ HIGH from DEN inactive	10	40		
T23	DEN (WRITE) active delay	–	30		
T24	DEN (WRITE) inactive delay	3			
T25	DEN inactive from CEN	–	25		
T26	DEN active from CEN				
T27	DT/$\overline{R}$ HIGH from CLK and CEN 2)		50		
T28	DEN Active from $\overline{AEN}$		30		

Notes see next page

AC Characteristics SAB 82288 (cont.)

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
T29	Command active delay	3	20	ns	IOL = 32 mA IOH = −5mA CL = 300 pF from 0.8V on CLK to 0.8 or 2.0V on output
T30	Command inactive delay				
T31	Command inactive from CEN	–	25		
T32	Command active from CEN				
T33	Command inactive enable from $\overline{AEN}$		40		
T34	Command float time				

1) $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold times are specified to guarantee the response shown in the waveforms.

2) T27 only applies to bus cycles where MB = 0, the SAB 82288 was selected, and DEN = 0 when the cycle terminated (because CEN = 0).

AC Characteristics SAB 82288-6

TA = 0 to 70°C, VCC = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
T1	CLK period	83	250	ns	at 1.5V
T2	CLK HIGH time	25	235		at 3.9V
T3	CLK LOW time	20	225		at 0.6V
T4	CLK fall time	–	10		3.5 to 1.0V
T5	CLK rise time				1.0 to 3.5V
T6	M/$\overline{IO}$ and status setup time	28	–		from 0.8 or 2.0V on input to 0.8V on CLK
T7	M/$\overline{IO}$ and status hold time	0			
T8	CENL setup time	30			
T9	CENL hold time	0			
T10	$\overline{READY}$ setup time	50			
T11	$\overline{READY}$ hold time	35			
T12	CMDLY setup time	25			
T13	CMDLY hold time	0			
T14	$\overline{AEN}$ setup time 1)	30			
T15	$\overline{AEN}$ hold time 1)	0			
T16	ALE, MCE active delay	3	25		from 0.8V on CLK to 0.8 or 2.0V on output IOL = 16mA IOH = −1mA CL = 150pF
T17	ALE, MCE inactive delay	–	35		
T18	DEN (WRITE) inactive from CENL		35		
T19	DT/$\overline{R}$ LOW from CLK		40		
T20	DEN (READ) active from DT/$\overline{R}$	10	50		
T21	DEN (READ) inactive delay	3	40		
T22	DT/$\overline{R}$ HIGH from DEN inactive	5	45		
T23	DEN (WRITE) active delay	–	35		
T24	DEN (WRITE) inactive delay	3			
T25	DEN inactive from CEN	–	40		
T26	DEN active from CEN		35		
T27	DT/$\overline{R}$ HIGH from CLK and CEN 2)		50		
T28	DEN Active from $\overline{AEN}$		35		

Notes see next page

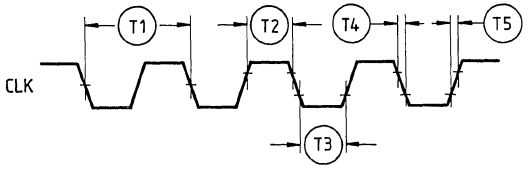
AC Characteristics SAB 82288-6 (cont.)

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
T29	Command active delay	3	40	ns	IOL = 32 mA IOH = −5mA CL = 300 pF from 0.8V on CLK to 0.8 or 2.0V on output
T30	Command inactive delay		30		
T31	Command inactive from CEN	–	35		
T32	Command active from CEN		45		
T33	Command inactive enable from $\overline{AEN}$		40		
T34	Command float time				

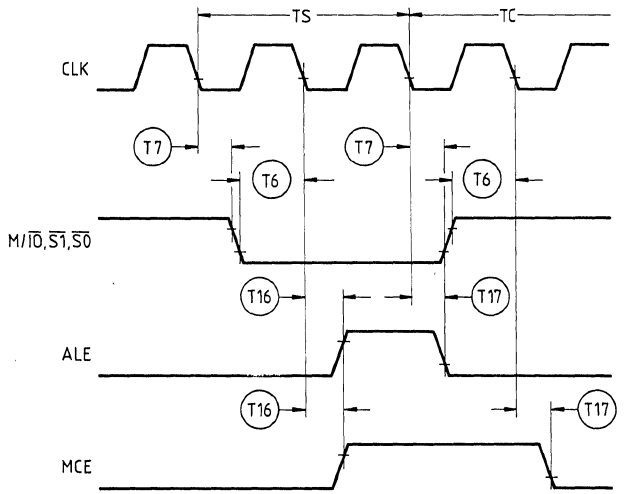
1) $\overline{AEN}$ is an asynchronous input. $\overline{AEN}$ setup and hold times are specified to guarantee the response shown in the waveforms.

2) T27 only applies to bus cycles where MB = 0, the SAB 82288 was selected, and DEN = 0 when the cycle terminated (because CEN = 0).

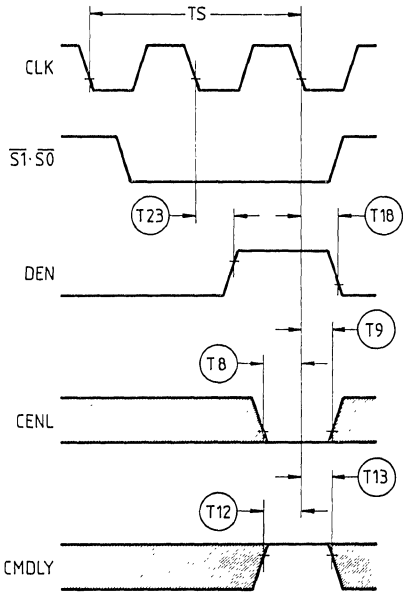
CLK Characteristics



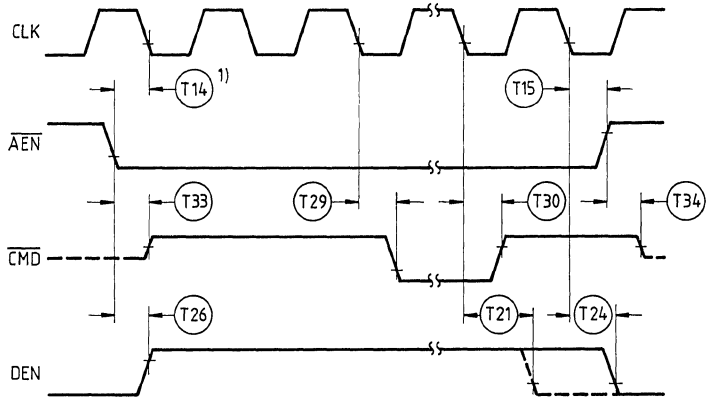
Status, ALE, MCE, Characteristics



CENL, CMDLY, DEN Characteristics with MB = 0 and CEN = 1 during Write Cycle

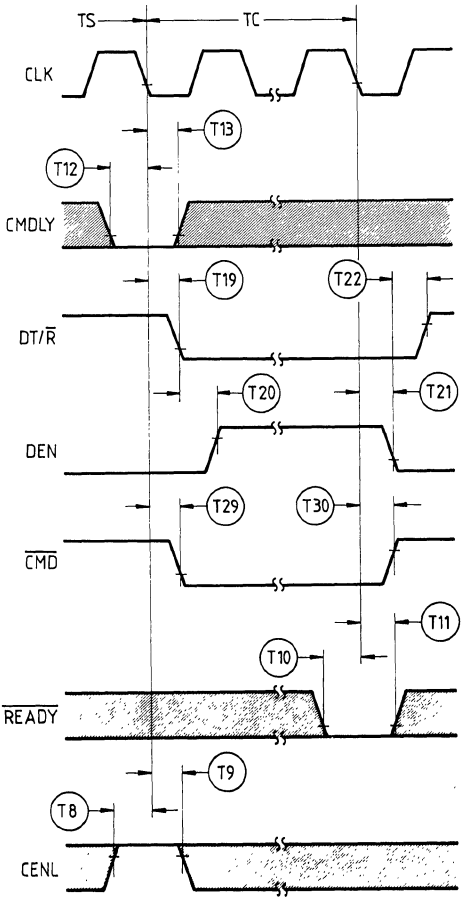


AEN Characteristics with MB = 1

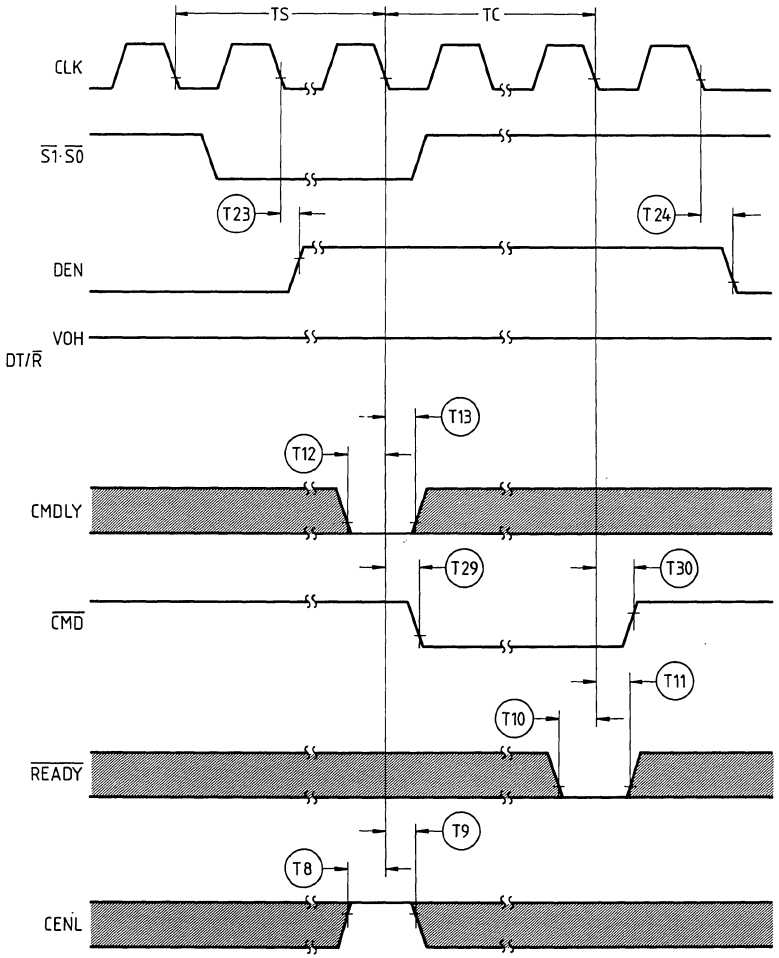


1) AEN is an asynchronous input. AEN setup and hold time is specified to guarantee the response shown in the waveforms.

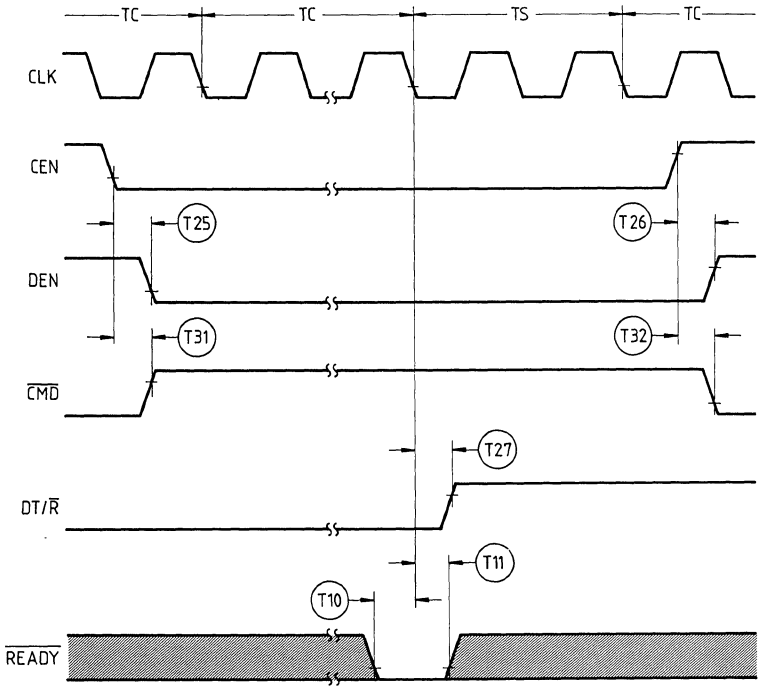
Read Cycle Characteristics with MB = 0 and CEN = 1



Write Cycle Characteristics with MB = 0 and CEN = 1



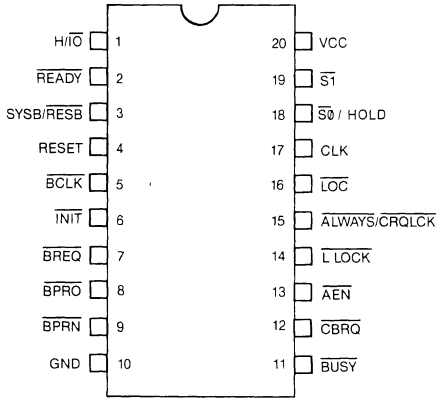
CEN Characteristics with MB = 0



SAB 82289
Bus Arbiter for
SAB 80286 Processor Family

- Supports Multi-master System Bus Arbitration Protocol
- Synchronizes SAB 80286 Process with Multi-master Bus
- Compatible with IEEE 796 Standard Bus (Multibus*)
- Three Modes of Bus Release Operation for Flexible System Configuration
- Supports Parallel, Serial, and Rotating Priority Resolving Schemes

Pin Configuration



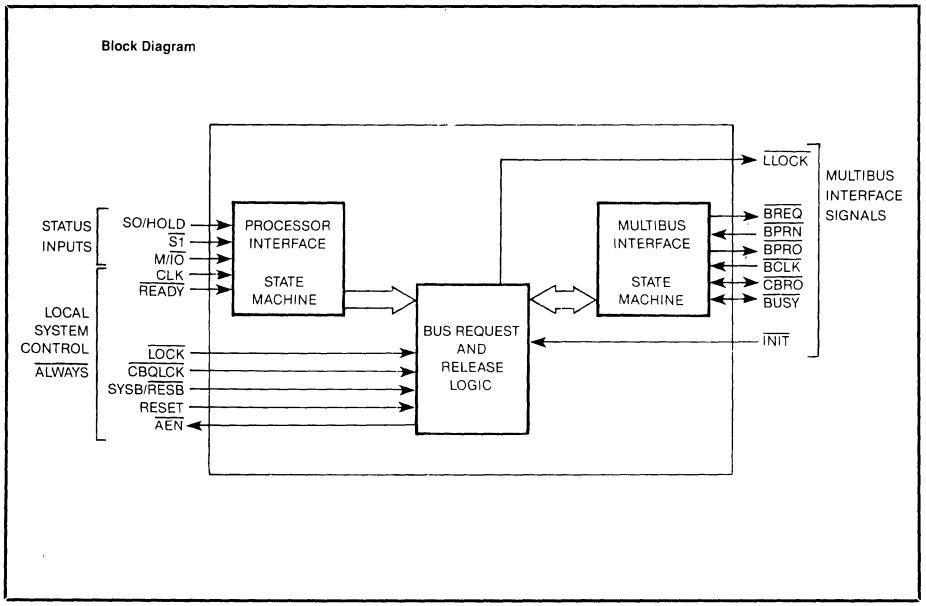
Pin Names

S0 / HOLD	Status S0 / Hold Input
S1, H/IO	Status Inputs
BUSY	Busy Input/Output
READY	Ready Input
SYSB/RESB	System/Resident Bus
RESET	Processor Reset
BCLK	Bus Clock
INIT	Initialize
BREQ	Bus Request
BPRO	Bus Priority Out
BPRN	Bus Priority In
CLK	System Clock
AEN	Address Enable
ALWAYS/CBQLCK	Always Release/ Common Bus Request Lock
L LOCK	Level Lock
CBRQ	Common Bus Request
LOCK	Bus Lock
VCC	+ 5 V
GND	Ground (0V)

The SAB 82289 Bus Arbiter is a 5-Volt, 20-pin MYMOS component for use in multiple bus master SAB 80286 systems. The SAB 82289 provides a compact solution to system bus arbitration for the SAB 80286 CPU.

The complete IEEE 796 Standard bus arbitration protocol is supported. Three modes of bus release operation support a number of bus usage models.

* Multibus is a trademark of Intel Corporation.



Functional Description

The SAB 82289 Bus Arbiter in conjunction with the SAB 82288 Bus Controller and the SAB 82284 Clock Generator interfaces the SAB 80286 processor or some other bus master to a multi-master system bus. The arbiter multiplexes a processor onto a multi-master system bus. It avoids contention with other bus masters.

The SAB 82289 has two separate state machines which communicate through bus request and release logic. The processor interface state machine is synchronous with the local system clock (CLK) and the multi-master system bus interface state machine is synchronous with the bus clock (BCLK).

The SAB 82289 performs all signalling to request, obtain, and release the system bus. External logic is used to determine which bus cycles require the system bus and to resolve the priorities of simultaneous requests for control of the system bus.

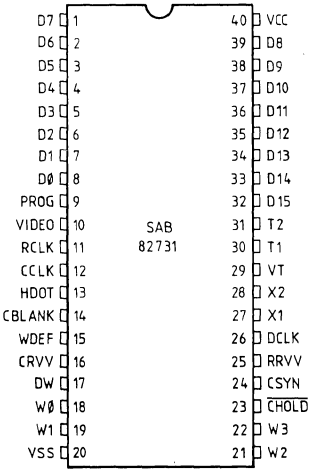
SAB 82731
Dot Rate Generator

A complete video interface between CRT Controller and CRT Display

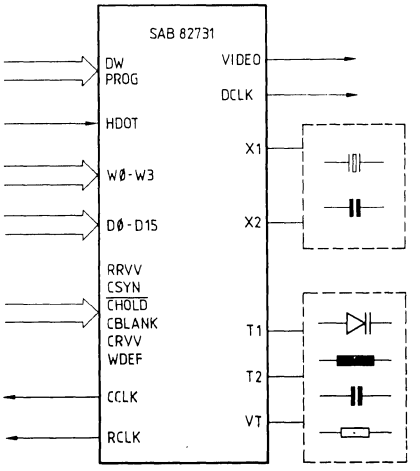
SAB 82731 – 50 MHz
SAB 82731-2 – 80 MHz

- Dot shift rates up to 80 MHz (SAB 82731-2)
- Character length up to 16 dots
- Proportional character spacing supported
- Half dot shifts for character rounding
- Character attribute processing
- Single 5V power supply
- 40 pin DIP package
- Interface optimized for next generation CRT controllers

Pin Configuration



Functional Symbol



The SAB 82731 is a general purpose video interface, which generates a video signal output for the CRT monitor from parallel character and attribute information coming from the character generator and the CRT controller. The SAB 82731 together with minimal hardware, comprises a complete video interface system for the CRT controller and the CRT monitor. The device is fabricated in a fast bipolar ASBC (Advanced Standard Buried Collector) process of Siemens.

Pin Definitions and Functions

Symbol	Number	Input (I) Output (O)	Function
DØ-D15	1-8, 32-39	I	Character data parallel inputs
PROG	9	I	Program control input; used to program default width value of CCLK and width of RCLK; the default width value of CCLK and the width of RCLK are latched into the SAB 82731 via DØ-D7 at the rising edge of CCLK (active high)
VIDEO	10	O	Video output; provides the dot information clocked by the internal dot clock
RCLK	11	O	Reference clock output; used to generate the timing for the screen columns for data formatting. The period of RCLK is programmable from 6 to 21 times the period of the internal dot clock
CCLK	12	O	Character clock output; used to clock character and attribute information out of the CRT controller. The period of CCLK is programmable from 3 to 18 times the period of the internal dot clock
HDOT	13	I	Half dot shift input; the video signal at the video output will be delayed by half dot clock for character rounding (active high)
CBLANK	14	I	Character blank attribute input; the video output is blanked (active high)
WDEF	15	I	Width defeat attribute input; the CCLK period is set to a preprogrammed default value (active high)
CRVV	16	I	Character reverse video attribute input; inverts the character data from DØ-D15 (active high)

Pin Definitions and Functions (continued)

Symbol	Number	Input (I) Output (O)	Function
DW	17	I	Double width attribute input; the internal dot clock frequency and the CCLK frequency are divided by two (active high). The RCLK frequency remains unchanged
WØ-W3	18, 19 21, 22	I	Clock width inputs; they are used for programming the CCLK clock width on a character by character base
$\overline{\text{CHOLD}}$	23	I	CCLK inhibit input; this signal suppresses the CCLK generation and is used for TAB function (active low)
CSYN	24	I	CCLK synchronization input; CCLK will be synchronized to RCLK and the video output signal is defined by RRVV (active high)
RRVV	25	I	Field reverse video input; the video signal at the video output will be inverted (active high)
DCLK	26	O	Dot clock output; ECL-level signal intended for test purposes only. Must be grounded via a 3.3k resistor if used
X1-X2	27, 28	I	Inputs for fundamental mode crystal; its frequency must be 1/8 of the required dot clock frequency
VT	29	O	Tuning voltage for PLL-VCO; this output is used to tune the LC-circuit and thus controls the oscillator frequency of the internal dot clock
T1-T2	30, 31	I	LC-circuit inputs for PLL-VCO. T1 can be used to provide the SAB 82731 with an external clock
VCC	40	–	+5V power supply
VSS	20	–	Ground (0V)

Figure 1: CRT System Block Diagramm

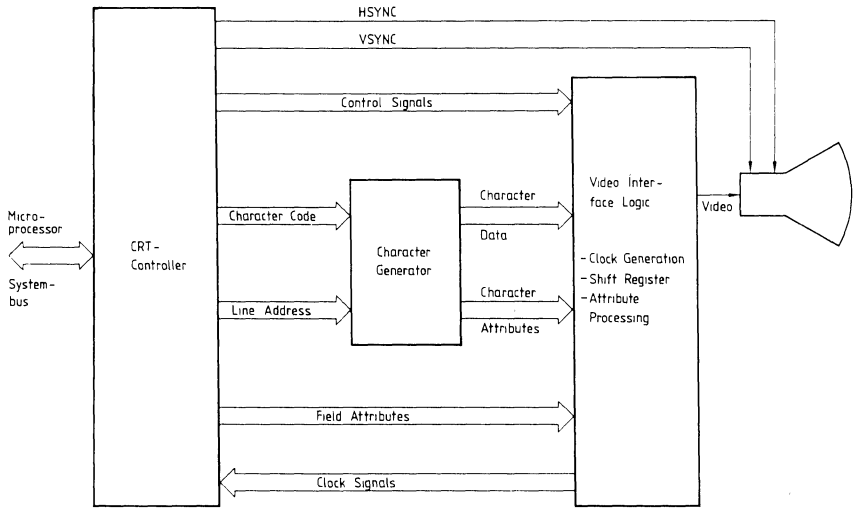
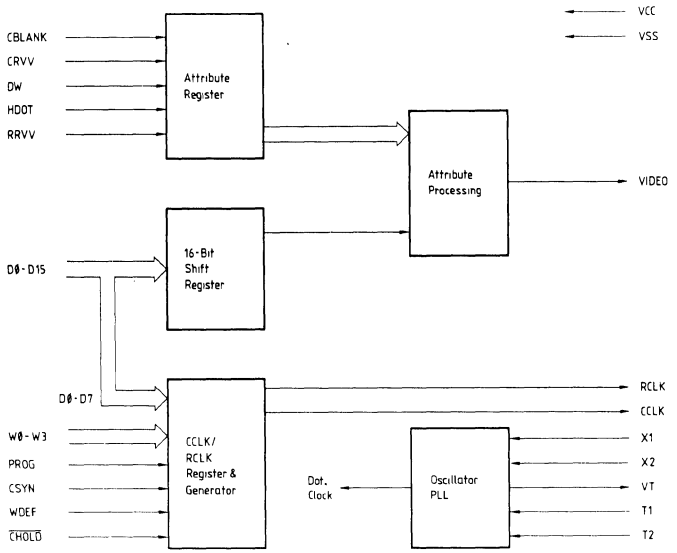


Figure 2: SAB 82731 Block Diagramm



General Description

The dot rate generator, SAB 82731, in a typical CRT system shown in figure 1, interfaces the CRT controller to the CRT video terminal (Video Interface Logic). It receives the parallel data along with the attribute and control information from the CRT controller, processes it into a serial video signal which can be fed to a video CRT terminal. It also generates the basic dot clock (DCLK), character clock (CCLK) and reference clock (RCLK) signals. CCLK and RCLK are required by the CRT controller.

CRT terminals requiring very high resolution, extremely stable and absolutely flicker-free pictures, place special demands on the dot rate generator. In such applications very high dot rates up to 80 MHz are necessary. This leaves very little time per dot (pixel) to convert the data, attribute, and control information into serial form for the video terminal.

The functions of SAB 82731 are largely determined by the complexity and the demands of the CRT controller it supports. Figure 2 shows the block diagram of the dot rate generator. The dot clock is generated by a voltage controlled LC circuit connected at T1 and T2. Another clock is generated which is crystal controlled and has a frequency 1/8 of the dot clock. This is used to stabilize the dot clock using an on-chip phase locked loop (PLL). This two-oscillator concept enables the use of low cost, fundamental mode crystals.

The 16 bit shift register receives parallel inputs from pins DØ-D15. This allows a maximum character width of 16 dots. The minimum width can be 3 dots. The character width is programmable on a character to character base through pins WØ-W3 for proportional character spacing. This also determines the character clock (CCLK) frequency. Programming of the default character width and the reference clock (RCLK) is done through inputs DØ-D7 and PROG. Signal WDEF can be used to switch between the default character width and the one specified dynamically through the lines WØ-W3. A special problem is encountered when using variable character width. For example, when tables are formatted on the screen it is essential that every entry in a column starts at the same dot distance (and not the character distance) from the start of line. This is directly supported by SAB 82731 providing a tabulator function using $\overline{\text{CHOLD}}$ signal.

It is possible to shift every line of character by half a dot using the HDOT signal. This feature, known as character rounding, further enhances the quality of high resolution character display. Other features, like blinking of characters, reverse video which improves the readability of text on screen, are directly supported by SAB 82731 using signals CRVV and RRVV from the CRT controller, processing them and effecting the final video signal to show the characters with the desired attributes.

Functional Description

Clock Generation

The most fundamental clock required to run the CRT display is the dot clock which provides the reference for the dot data to be shifted serially to the CRT. In addition, it is basis for the character clock CCLK and the reference clock RCLK required by the CRT controllers.

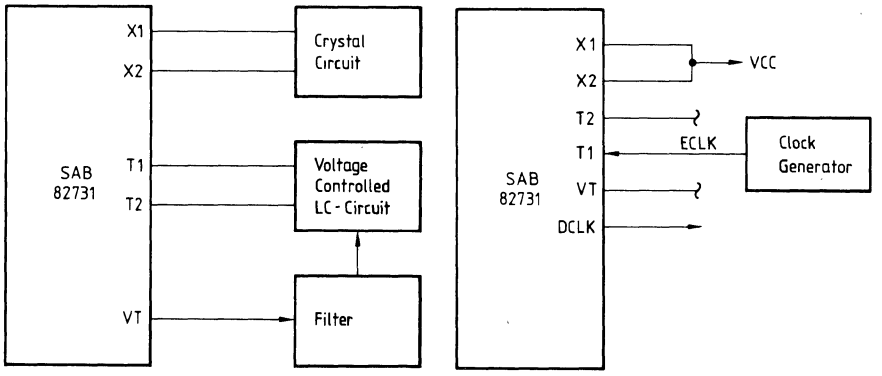
Dot Clock

The dot clock is derived from on-chip oscillator (T1, T2). Its frequency is determined by an external voltage controlled LC-circuit that has a center frequency of about two times the desired dot clock frequency. The on-chip PLL-circuit causes via VT this oscillator to be locked to the 16th harmonic of the on-chip crystal oscillator (X1, X2) which is running at 1/8 of the dot clock frequency (see figure 3a).

Alternatively, the SAB 82731 can be supplied with an external TTL-level clock via T1 that must be two times the dot clock rate (see figure 3b).

The SAB 82731 provides the dot clock at the DCLK output. It is an ECL-level output and is intended for testing and adjustment purposes only.

Figure 3: Clock Generation



a) Internal Clock Generation

b) External Clock Generation

Designing the Oscillator Circuit

The whole external oscillator circuit consists of three parts

- the crystal circuit,
- the voltage controlled LC-circuit and
- the loop filter for the PLL.

Figure 4a shows the general crystal circuit. The crystal must be a fundamental mode series resonant type with a resonant frequency of 1/8 of the desired dot clock frequency. The capacitor Cx is necessary if a fine adjustment of the dot clock rate must be done. Figure 4b shows as example how the dot clock frequency can vary with different values of Cx. The capacitors C1 and C2 may be necessary to suppress overtone oscillations if the crystal frequency is below of 6 MHz. The exact values depend on the used crystal and must be determined in an empiric way. The recommended ranges are 1 to 10 nF for C1 and 0 to 100 pF for C2.

The voltage controlled LC-circuit is shown in figure 4c. The effective oscillating LC-circuit consists of the inductance L, the capacitance CD of the varactor diode, and the parasitic capacitance CP. Its resonant frequency is

$$fR = \frac{1}{2\pi \sqrt{L \cdot (CD + CP)}}$$

where fR must be 2 × fDCLK. The value of CP depends on many factors (e.g. layout, single/multi-layer board ...), thus it changes from application to application. However a value of about 5 to 15 pF seems to be a good approximation.

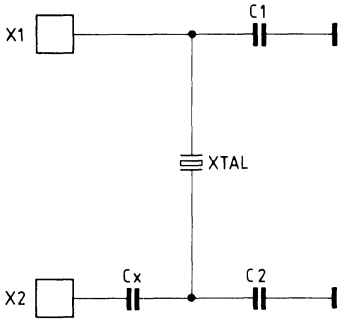
The value of CD (capacitive diode) should be determined at a control voltage of 2.5V to get the lock-in-range as wide as possible. The variation of VT ranges from 1V to VCC-1 which results in a minimum frequency shift of about 6-8% with respect to the center frequency at 2.5V.

The value of the inductance L must be determined in such a way that the resulting center frequency lies as near as possible to the needed frequency fR = 2 × fDCLK to guarantee a stable dot clock under all operation conditions. Figure 4f shows a diagram that will help you find the required inductance L. It is based on the use of the capacitive diode BB 505G that has a capacitance of 12 pF at a control voltage of 2.5V. The use of other diodes will, of course, lead to other diagrams.

At dot clock frequencies higher than 50 MHz the needed inductance becomes lower than 100 nH. In these cases, it is favorable to integrate the inductance into the board layout. Figure 4e shows a possible layout for the external oscillator circuit and approximate (measured) values of the inductance of the printed coil (track width and track distance 0.5 mm).

The loop filter converts the current pulses delivered by the PLL into the control voltage VT for the VCO. It is an essential part of the PLL and determines, for example, the lock-in-range and the control action of the PLL. A second-order filter that was found to work well under all operation conditions and over the full frequency range is shown in figure 4d.

Figure 4: Designing the Oscillator Circuit

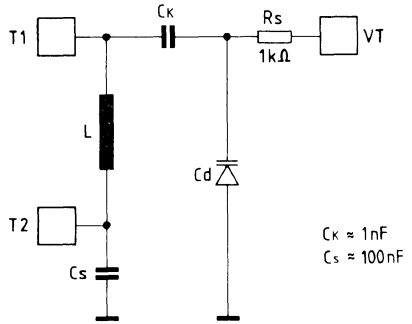


a) crystal circuit

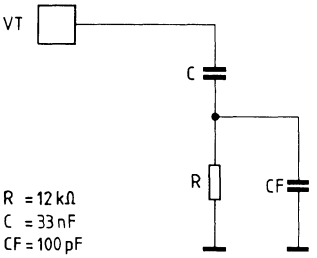
CX (pF)	fDCLK (MHz)
2.2	64.053
6.8	64.016
15	63.987
33	63.966

(nominal crystal frequency 8 MHz)

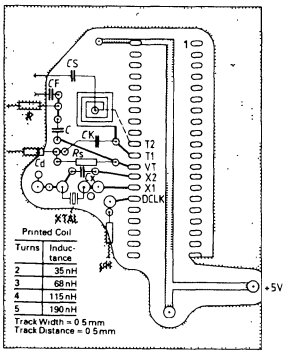
b) example for the influence of Cx on the dot clock frequency



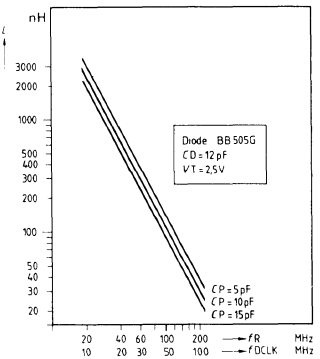
c) VCO-circuit



d) PLL-loop filter



e) example layout for printed circuit



f) L/f-diagramm

Reference Clock (RCLK)

RCLK is the reference clock output used to generate the timing for the screen layout and to define screen columns for data formatting and tabulator locations. In addition, it is used to clock the field attribute signals into the SAB 82731. The period of RCLK is programmable from 6 to 21 times the period of the dot clock, i.e. the RCLK high time is 3 dot clock periods and the RCLK low time is programmable from 3 to 18 dot clock periods. It is programmed via D4-D7 at the rising edge of CCLK, when PROG is active (see table and figure 5).

It is recommended to program the RCLK clock width only once after a system reset.

Programming table for the clock width of RCLK

D7	D6	D5	D4	PROG	RCLK period x dot clock period
0	0	0	0	1	16
0	0	0	1	1	17
0	0	1	0	1	18
0	0	1	1	1	19
0	1	0	0	1	20
0	1	0	1	1	21
0	1	1	0	1	6
0	1	1	1	1	7
1	0	0	0	1	8
1	0	0	1	1	9
1	0	1	0	1	10
1	0	1	1	1	11
1	1	0	0	1	12
1	1	0	1	1	13
1	1	1	0	1	14
1	1	1	1	1	15

Character Clock (CCLK)

CCLK is the fundamental character clock output used to clock character and attribute information out of the CRT controller and into the SAB 82731.

It is a rising edge triggered clock and inside the active character field its period is programmable from 3 to 18 times the period of the dot clock, i.e. the CCLK high time is 2 dot clock periods and the CCLK low time is programmable from 1 to 16 dot clock periods.

When CSYN is active (normally outside the active character field) CCLK is forced to match RCLK. In this case the CCLK high time is 3 dot clock periods instead of 2.

In order to support proportional spacing, the period of CCLK can be reprogrammed at the beginning of each CCLK cycle via the W0-W3 inputs (i.e. at the beginning of each character) if PROG is inactive.

Programming of the character width is done via the clock width inputs WØ-W3 according to the programming table. The WØ-W3 input data is clocked into the SAB 82731 at the rising edge of CCLK and defines the width of the currently displayed character (see figure 6).

If the width defeat attribute (WDEF) is active, the period of CCLK will be set to the programmed default value ignoring the clock width inputs WØ-W3. This value is programmable from 3 to 18 times the period of the dot clock via the DØ-D3 data inputs, when the PROG input is active (see figure 5).

It is recommended to programm the default CCLK clock width only once after a system reset.

The CCLK clock period will be doubled if the double width attribute (DW) is asserted.

Note:
If the width of CCLK is programmed to 17 or 18, zeros are shifted out from the internal shift register after the 16 data bits and displayed according to the attribute signal.

Programming table for the clock width of CCLK

PROG = 1	D3	D2	D1	DØ	CCLK clock period x dot clock period
PROG = Ø	W3	W2	W1	WØ	
	0	0	0	0	16
	0	0	0	1	17
	0	0	1	0	18
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

Note:
PROG = 1: Programming the CCLK default clock width during the initialization phase via DØ-D3 at the rising edge of CCLK.
PROG = Ø: Programming the clock width of the current CCLK cycle via WØ-W3 at the rising edge of CCLK.

Clock Initialization Sequence (PROG)

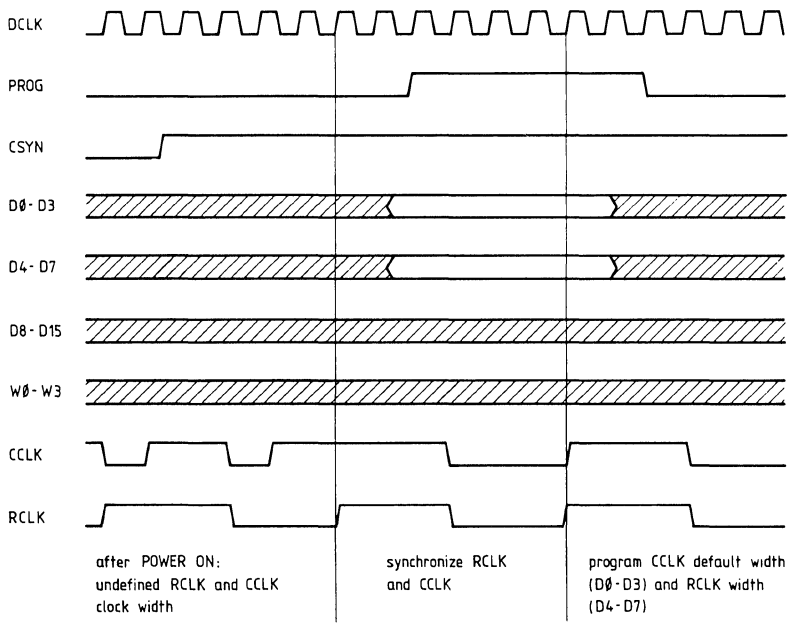
After power on the width of RCLK is a random value between 6 and 21 and the width of CCLK is a random value between 3 and 18.

It is recommended to initialize the SAB 82731 in the following way:

- Activate the CSYN signal.
  CCLK is forced to match RCLK, which has a minimum clock width of 6 dot clock periods.
- Apply the clock width information to DØ-D3 and D4-D7 according to tables.
- Activate the PROG signal.
  The default width of CCLK and the width of RCLK are programmed at the next rising edge of CCLK (see figure 5).
- Remove the PROG signal

CSYN can be removed at the beginning of the next active data field.

Figure 5: Clock Initialization



Character Data Signals

The character data signals are normally provided by the character ROM and clocked into the SAB 82731 at the rising edge of CCLK.

The character data signals consist of

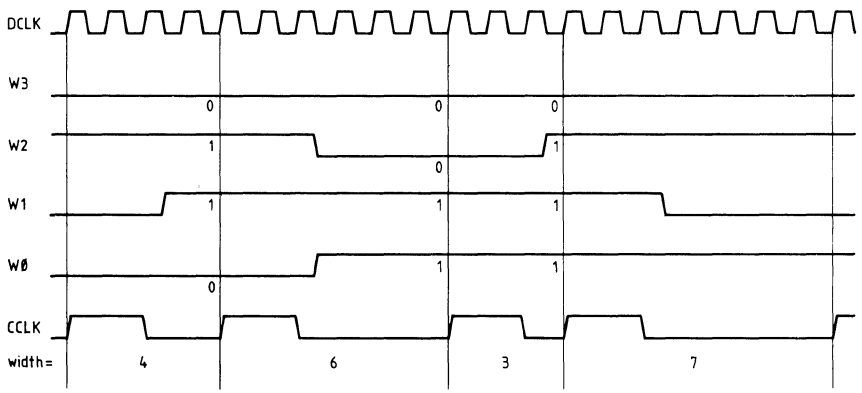
- the character data lines (DØ-D15),
- the character width information (WØ-W3) and
- the half dot shift signal (HDOT).

Dot Data (DØ-D15)
The dot data signals will be clocked into the SAB 82731 via the DØ-D15 inputs at the rising edge of CCLK. The actually used inputs are defined by the WØ–W3 inputs or the internally latched default width information previously programmed. The dot data will be displayed dependent on the control signals and on the corresponding attribute information. The data are serially shifted out at the video output starting with DØ.

If CCLK width is greater than 16, zeros are shifted out for the rest of the dot clocks and displayed according to the attribute signals.

Character Width (WØ-W3)
The WØ-W3 inputs are clocked into the SAB 82731 at the rising edge of CCLK and determine the width of the currently displayed character (see CCLK).

Figure 6: Action of Clock Width Inputs WØ-W3 on CCLK



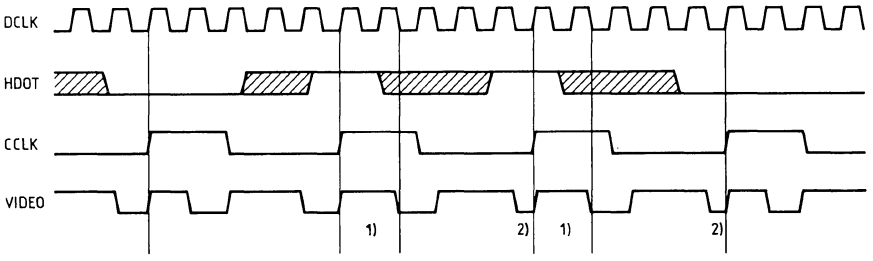
Half Dot Shift (HDOT)

The half dot shift character data signal is clocked into the SAB 82731 at the rising edge of CCLK. When the half dot shift signal is active (high), the output of the displayed data will be delayed by half a dot line. The first dot of the character dot line is transmitted during one and a half dot clock period while the last dot of this character dot line is displayed for half a dot clock period only. The remaining character dots are transmitted within one dot clock period and thus the whole character dots are shifted by half a dot.

The HDOT signal is no character attribute signal, because it can change from dot line to dot line of a character. Thus it is reasonable to generate it from the character ROM together with the dot data and the width information.

Note that only the character dot line to which the HDOT signal is attached is effected.

Figure 7: Function of HDOT on VIDEO



Width is assumed to 5 D3-DØ=Ø5H

1) 1 1/2 DCLK

2) 1/2 DCLK

Character Attribute Signals

These signals are clocked into the SAB 82731 at the rising edge of CCLK. Thus they are valid for the next character only.

The character attribute signals consist of:

- character blanking CBLANK,
- character reverse video CRVV,
- double width DW,
- width defeat WDEF.

Outside the active character field (which is defined by the CSYN signal) all character attribute signals are ignored.

Character Blanking (CBLANK)

The CBLANK input is clocked into the SAB 82731 at the rising edge of CCLK. If aktive (high), the blank attribute will produce the effect of blanking the display of the character. When the CBLANK attribute is active the corresponding dot data information DØ-D15 will be as if all zeros where forced at the inputs. The video output can be inverted to all ones by simultaneously activating the CRVV attribute. Independent of these character oriented operations the video output signal is also effected by the RRVV field attribute signal.

Although the CBLANK signal is normally a character attribute, it may change from dot line to dot line of a character. Thus together with the CRVV signal one or more underlines or cursors can be generated controlled by the CRT controller.

Character Reverse Video (CRVV)

The CRVV input is clocked into the SAB 82731 at the rising edge of CCLK. It is an active high signal. In the character field, the CRVV attribute will produce the effect of reversing the polarity of the display during the transmission of the current character. CRVV is also effective together with the CBLANK attribute (see CBLANK description) and the RRVV signal.

Outside the character field, the CRVV attribute is ingnored. Although the CRVV signal normally is a character attribute signal it may change from dot line to dot line of a character in order to support underlines or cursors.

Double Width (DW)

The DW input is clocked into the SAB 82731 at the rising edge of CCLK. The dot clock frequency and the CCLK frequency will be halved when the double width attribute is active (high), producing characters that are twice as wide. The period of RCLK is not changed (see figure 8).

Width Defeat (WDEF)

The WDEF attribute signal is clocked into the SAB 82731 at the rising edge of CCLK. When the width defeat attribute is active (high), the width of CCLK will be set to a default width value previously programmed (see figure 9).

Figure 8: Function of DW on DCLK and CCLK

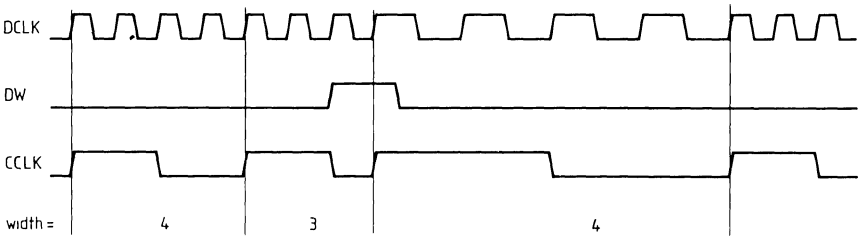
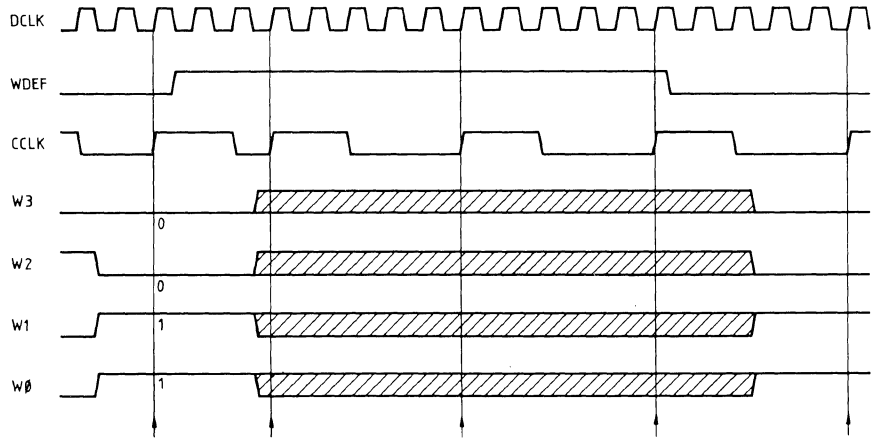


Figure 9: Function of WDEF



The default width of CCLK was previously defined as 5

Field Attribute Signals

The field attribute signals are clocked into the SAB 82731 with the rising edge of RCLK. Thus the attributes are valid for a specifical part of the screen independent of how many characters are displayed within this part.

The SAB 82731 supports two field attributes:

- field reverse video RRVV and
- clock synchronization CSYN.

Field Reverse Video (RRVV)

The RRVV control signal is clocked into the SAB 82731 at the rising edge of RCLK. It immediately effects the display by the polarity of the video output in both the character field and the border of the display. It is an active high signal.

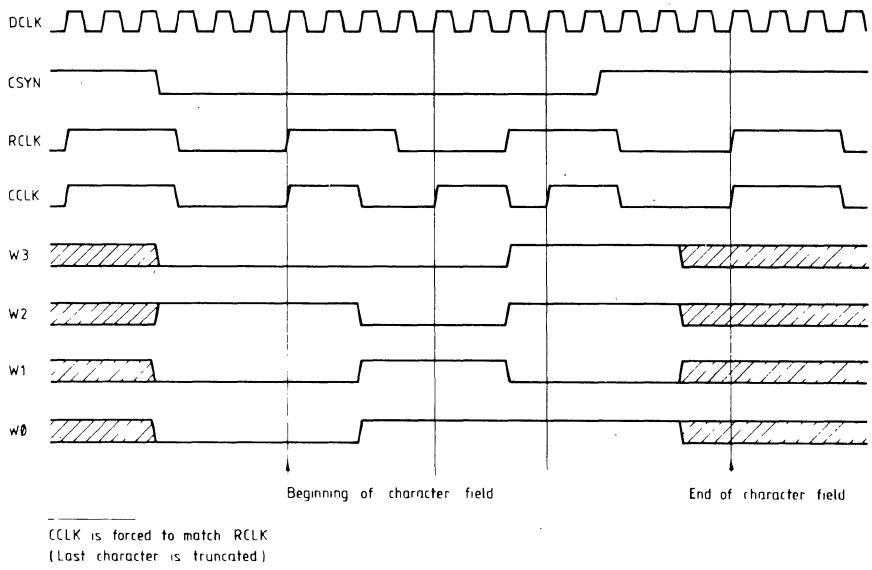
Clock Synchronization (CSYN)

CSYN is a field attribute signal, because it defines the active character field in addition to its function of synchronizing CCLK and RCLK.

With a low level of CSYN (deactivated) clocked into the SAB 82731 with the rising edge of RCLK, the beginning of the character field area is defined (see figure 10) and the first character will be displayed. At the next rising edge of RCLK after CSYN is activated (i.e. at the end of the character field), the video output is forced to zero or, if the RRVV control signal is active, to a high level. The currently transmitted character will be truncated at this location. At the same time, CCLK will be forced to match RCLK starting with the next rising edge of RCLK (see figure 10). While CSYN is active all character attribute and data signals are ignored and only the field reverse video signal is effecting the video output.

Before the deactivation of CSYN, the data and attribute pipeline has to be filled by the CRT controller with the information of the first character.

Figure 10: Function of CSYN



Tabulator Function

The SAB 82731 supports tabulator functions by providing the $\overline{\text{CHOLD}}$ (character clock inhibit) input.

CCLK Inhibit ($\overline{\text{CHOLD}}$)

When the $\overline{\text{CHOLD}}$ signal is activated (low) it inhibits the CCLK clock and thus freezes the information pipeline between CRT-controller and SAB 82731 until the next tabulator location is reached. $\overline{\text{CHOLD}}$ has to be activated simultaneously with the display of the TAB-character. If the TAB-character doesn't consist of all zeros, it must be blanked by activating CBLANK.

The width of the TAB-character can be determined by WØ-W3 or by activating WDEF.

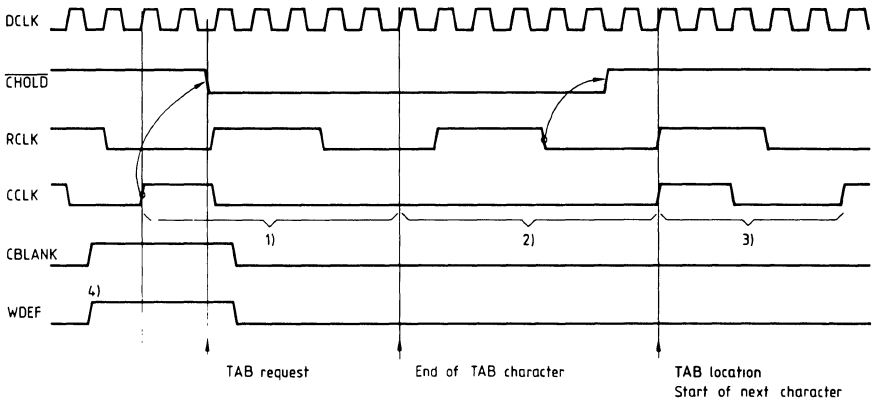
The $\overline{\text{CHOLD}}$-signal is provided by the CRT-controller and it is assumed to be triggered with the leading edge of CCLK (figure 11). With the same edge of CCLK, the TAB-character will be latched into the SAB 82731. Thereby the attributes CBLANK and WDEF must be active if used. Thus the TAB-character will be displayed completely and the CCLK will be inhibited until reaching the specified tabulator location, which is defined by $\overline{\text{CHOLD}}$ inactive (high) at the rising edge of RCLK.
In the timing diagrams it is assumed that $\overline{\text{CHOLD}}$ is deactivated by the trailing edge of RCLK. Figure 11 shows the normal case where the display of the TAB-character is finished before the deactivation of $\overline{\text{CHOLD}}$. The gap between the TAB-location and the following character is normally blanked. In this scheme the TAB-character will be handled by the SAB 82731 like any other character (attribute processing is done quite normally).

In case of $\overline{\text{CHOLD}}$ active width being less than the TAB-character width the TAB-character will also be displayed completely. However, we have to distinguish three different cases:

1) TAB-character is terminated before reaching TAB-location. The next character will be displayed as described before. In the gap the video output is normally blanked.
2) TAB-character is finished exactly at the TAB-location. The next character will be displayed immediately without delay.
3) TAB-character is not terminated when reaching the TAB-location (see figure 12). The following character will be displayed subsequently after the display of the TAB-character (i.e. the start of the following character is not at the TAB-location).

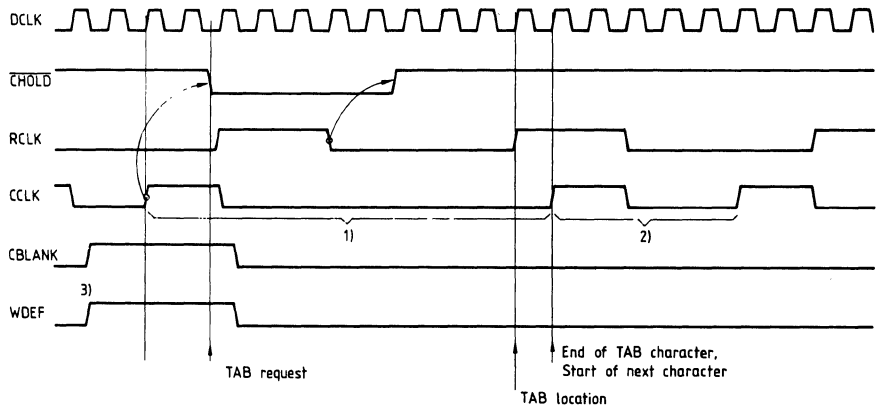
If the $\overline{\text{CHOLD}}$ signal is not deactivated the video output will be continuously blanked. In the gap between the end of the TAB-character and the TAB-location all character attribute signals will have no effect on the video output signal. If the RRVV control signal is active the video output signal is inverted.

Figure 11: Function of $\overline{\text{CHOLD}}$ (normal case)



1) TAB character is displayed completely video output is blanked
2) Video output is blanked
3) Next character
4) Default width 7, TAB character width defined by WDEF

Figure 12: Function of $\overline{\text{CHOLD}}$ with $\overline{\text{CHOLD}}$ Width Less than Character Width (case 3)



1) TAB character is displayed completely video output is blanked
2) Next character displayed subsequently (not on TAB location)
3) Default width: 11, TAB character width defined by WDEF

Video Output

The video output provides an ECL oriented signal (see figure 13) and is matched to drive a 50 Ohm coax cable (see figure 14). In case of external attribute processing the external logic can be ECL- or STTL-compatible.

Figure 13: Video Output Stage

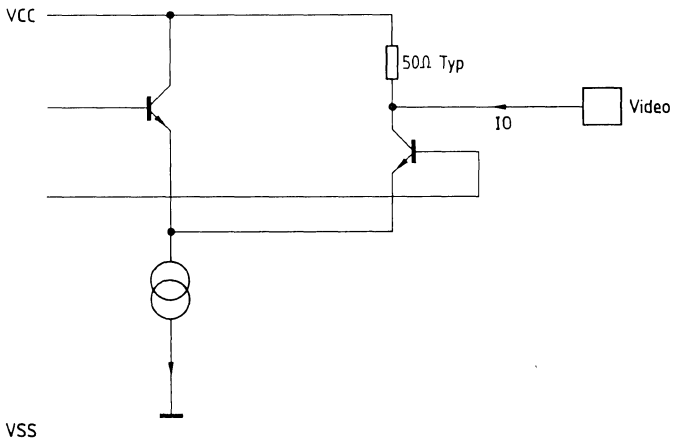


Figure 14: Video Output Load

Coax Cable

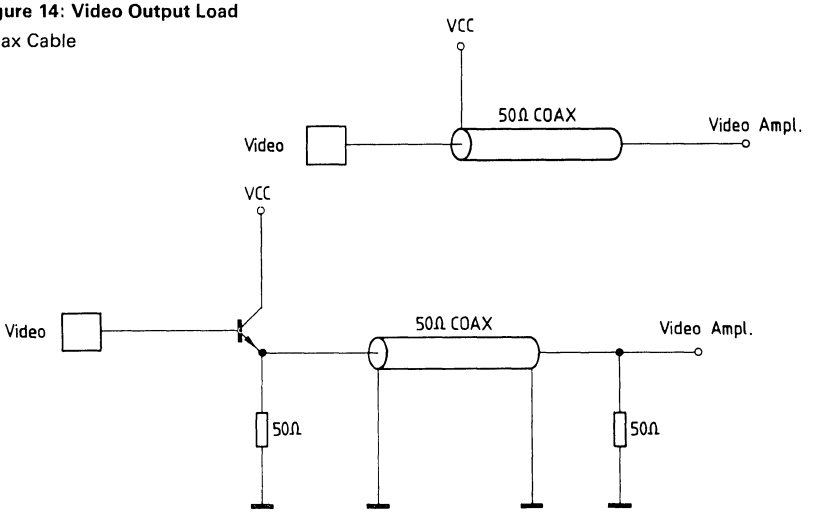


Figure 14: Video Output Load (continued)

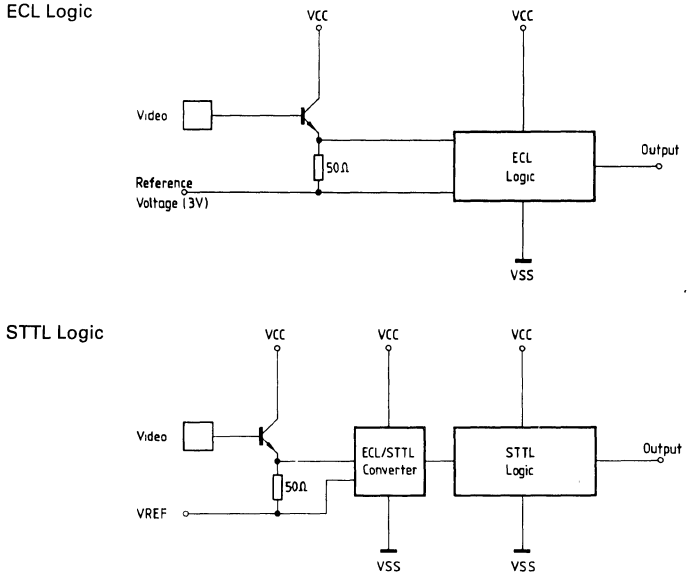
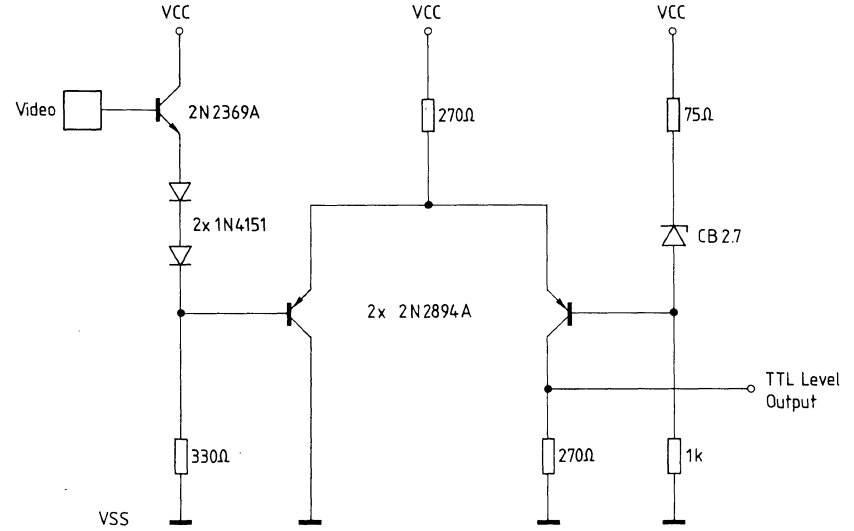


Figure 15: Proposed Converter for Video Output to TTL Level Output



Absolute Maximum Ratings[1])

Temperature under bias	0 to + 70°C
Storage Temperature	−65 to +150°C
All output and supply voltages	−0.5V to +6V
All input voltages	−0.5V to +5.5V
Power dissipation	1.5 Watts

D.C. Characteristics

TA = 0 to 70°C; VCC = 5V ±10%

Symbol	Parameter	Limit values		Unit	Test conditions
		Min.	Max.		
VC	Input clamp voltage		−1	V	IC = −5 mA
IIL	Forward input current	–	−0.7	mA	VIL = 0.5 V
IIH	Reverse input current	–	50	µA	VIH = VCC
VOL	Output low voltage				
	CCLK		0.5	V	IOL = 8 mA
	RCLK		0.5		IOL = 4 mA
	VIDEO	VCC-1.2V	VCC-0.6V	–	IOL = 0
VOH	Output high voltage				
	CCLK, RCLK	2.4	–	V	IOH = −400 µA
	VIDEO	VCC-0.2V	VCC	–	IOL = 0
VIL	Input low voltage	–	0.8	V	–
VIH	Input high voltage	2.0	–		
ICC	Power supply current	–	250	mA	[2])
ZO	Output impedance VIDEO	40	70	Ohms	–
CIN	Input capacitance	–	15	pF	fc = 1 MHz

[1]) Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]) All outputs open; VCC = 5V; TA = 25°C.

A.C. Characteristics

TA = 0 to 70°C; VCC = 5V ±10%

Symbol	Parameter	Limit values				Unit	Test conditions
		SAB 82731		SAB 82731-2			
		Min.	Max.	Min.	Max.		
tDHDH	DCLK cycle period	20	125			ns	–
tCHCH	CCLK cycle period	3	18			tDHDH	
tCLCH	CCLK low time	tDHDH −10	16 tDHDH +20			ns	
tCHCL	CCLK high time	2 tDHDH −20	–				
tRHRH	RCLK cycle period	6	21			tDHDH	
tRLRH	RCLK low time	3 tDHDH −10	18 tDHDH +20				
tRHRL	RCLK high time	3 tDHDH −20					
tDVCH	Data and attribute input set up time	30		1)			Fig. 16
tCHDX	Data and attribute input hold time	0					
tHLTE	$\overline{\text{CHOLD}}$ active before end of TAB.-char.	30	–			ns	
tHLHH	$\overline{\text{CHOLD}}$ pulse width	20					
tHHRH	$\overline{\text{CHOLD}}$ inactive set up before rising edge of RCLK	30					
tHLRH	$\overline{\text{CHOLD}}$ inactive hold time after rising edge of RCLK	0					

[1]) A.C. data for the SAB 82731-2 was not available at the time this data book was compiled. Contact your Siemens representative for complete information.

A.C. Characteristics (continued)

Symbol	Parameter	Limit values				Unit	Test conditions
		SAB 82731		SAB 82731-2			
		Min.	Max.	Min.	Max.		
tCHVV	Video output valid after rising edge of CCLK	–	6	1)		ns	–
tOLOH	TTL-output rise time		10				Fig. 16
tOHOL	TTL-output fall time						
tVLVH	Video output rise time		3				Fig. 17
tVHVL	Video output fall time						

1) A.C. data for the SAB 82731-2 was not available at the time this data book was compiled. Contact your Siemens representative for complete information.

A.C. Testing Waveforms

Figure 16: TTL-Level Input/Output Testing

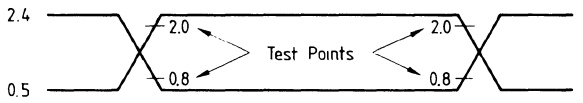
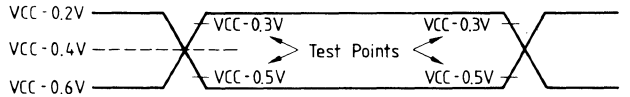
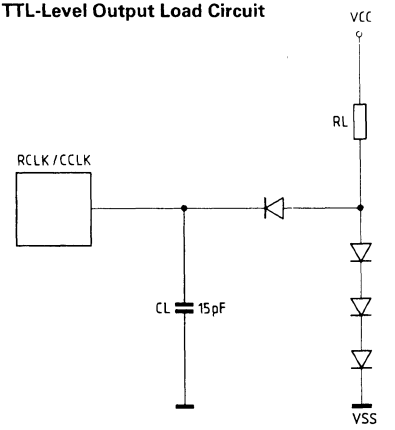


Figure 17: ECL-Level Output Testing



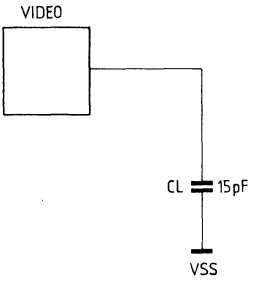
A.C. Testing Load Circuits

Figure 18: TTL-Level Output Load Circuit



RCLK: RL = 700Ω
CCLK: RL = 350Ω

Figure 19: ECL-Level Load Circuit



A.C. Waveforms

Figure 20: Basic Timing

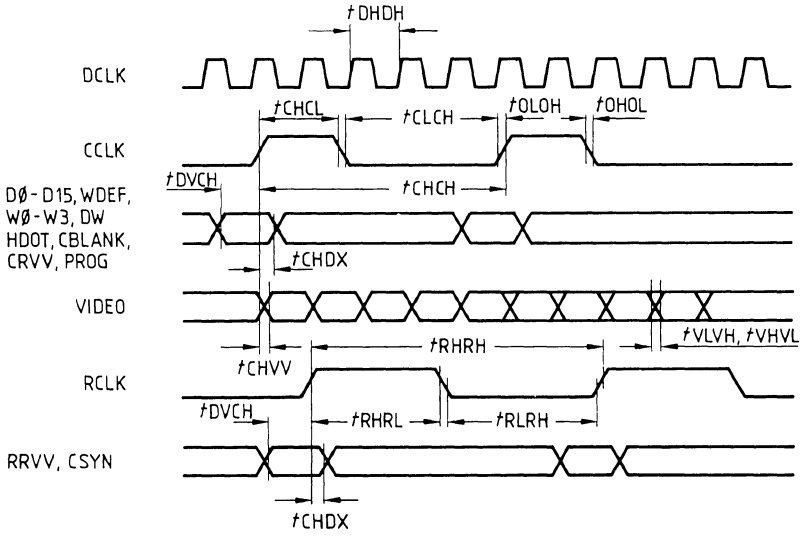
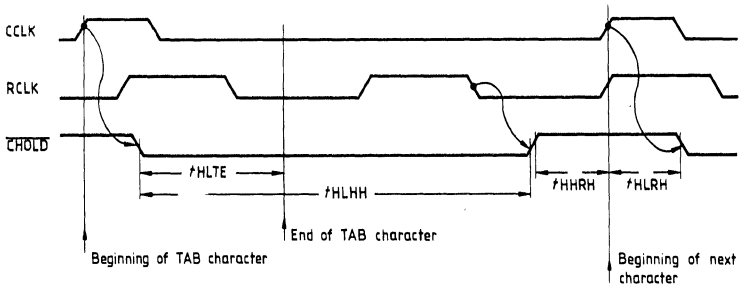
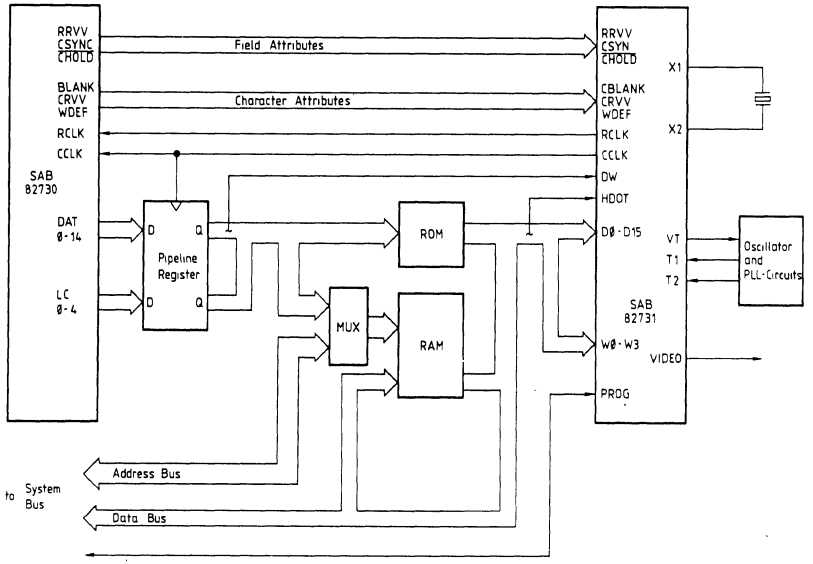


Figure 21: Timing on $\overline{\text{CHOLD}}$



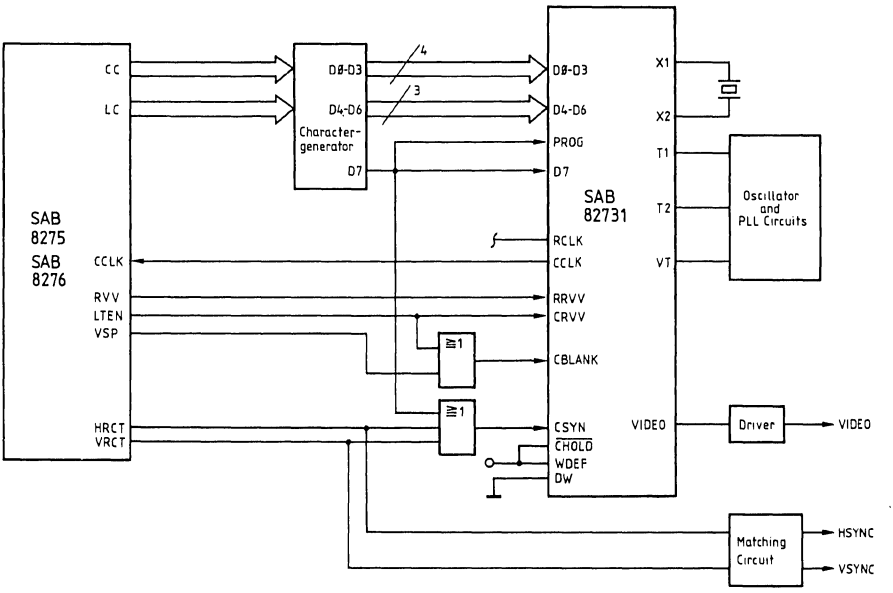
Application Examples

Figure 22: Example of Interface to SAB 82730



RAM or ROM may be selected either by addresses or by control signals. For pipeline register use positive edge triggered D-Flipflops (non-transparent latch) like SN 74374.

Figure 23: Example of Interface to SAB 8275



Memory Components

SAB 81C5x
256 x 8-Bit Static CMOS RAM

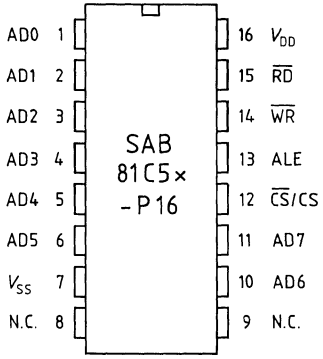
Preliminary data **MOS circuit**

The SAB 81C5x is a 2048 bit static random access memory (RAM), organized as 256 words by 8 bits, manufactured using CMOS silicon gate technology. The multiplexed address and data bus allows to interface directly with the CMOS 8-bit organized processors and microcomputers, for example with SAB 8085, SAB 8086, SAB 8088, SAB 8048, SAB 80C48, SAB 8051 and SAB 80C482. Low standby power dissipation (<1 µA) minimizes system power requirements.

Features

- 256 x 8-bit organization
- Multiplexed address and data bus
- Tristate address / data lines
- Very low power consumption
  Standby 1 µA at 6 V
  Operation 500 µA at 6 V, 1 MHz
- Wide supply voltage range: 2.5 to 6 V
- Data retention: 1.5 V

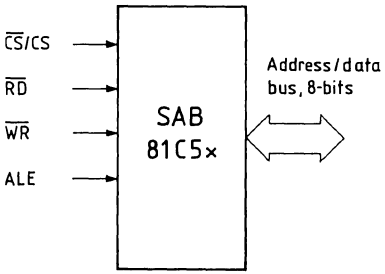
Pin configuration
top view



Pin designation

Pin No.	Symbol	Description
1–6 10, 11	AD0-7	Address/data lines
12	$\overline{CS}$, CS	Chip select $\overline{CS}$ = active low; internal pullup; CS = active high internal pulldown
13	ALE	Address latch enable
14	$\overline{WR}$	Write enable
15	$\overline{RD}$	Read enable
16	V_{DD}	Power supply (2.5 – 6 V)
7	V_{SS}	Ground (0 V)
8, 9	NC	Not connected

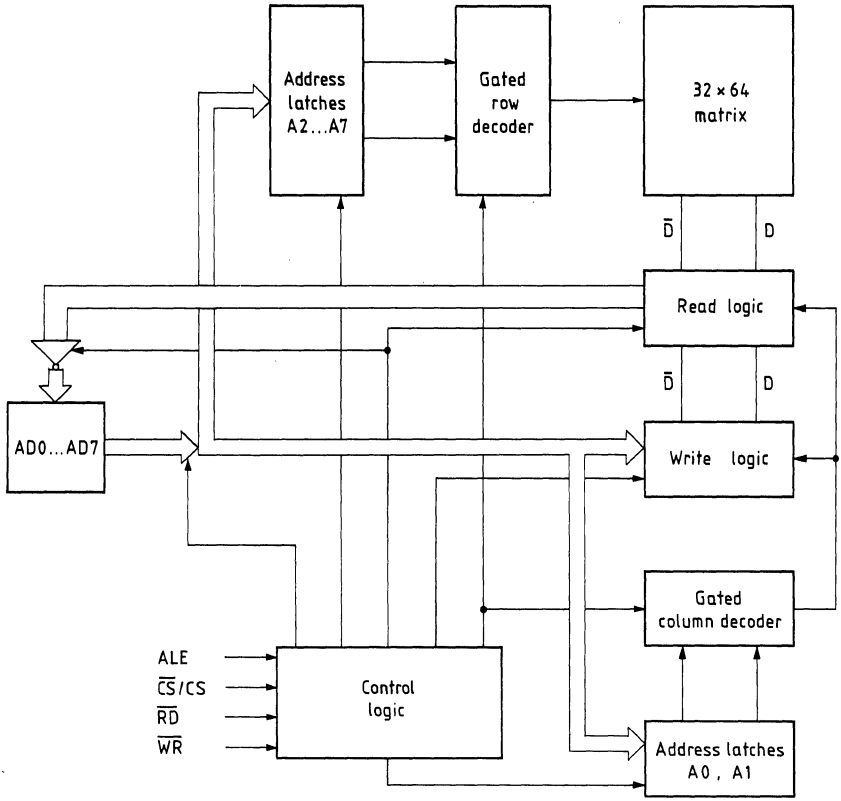
Logic symbol



Truth table for control and data bus pin status

$\overline{CS}$	CS	$\overline{RD}$	$\overline{WR}$	AD0...AD7 during data portion of cycle	Function
H	L	X	X	floating	none
L	H	L	H	data from memory	read
L	H	H	L	data to memory	write
L	H	H	H	floating	none

Block diagram



Maximum ratings *)

Ambient temperature under bias	T_{amb}	−25 to 70	°C
Storage temperature	T_{stg}	−55 to 125	°C
Supply voltage referred to GND (V_{SS})	V	0 to 7	V
Total power dissipation	P_{tot}	250	mW
All input and output voltages		−0.3 to V_{DD}	V

*) Stresses above absolute maximum ratings may cause permanent damage to the device.

DC characteristics

$T_{amb} = 25\,°C$; $V_{DD} = 2.5$ to 6 V; $V_{SS} = 0$ V

		Test conditions	Min.	Typ	Max.	Unit
Standby supply current	I_{DD}				1	µA
Operating supply current	I_{DD}	$f = 1$ MHz			500	µA
Operating supply voltage	V_{DD}		2.5		6	V
Standby voltage	V_{DD}	for data retention	1.5		6	V
Input current	I_{IL}	$V_I = 0$ to 6 V			1	µA
Output leakage current	I_{OL}	$V_O = 0$ to 6 V high impedance			1	µA
L input voltage	V_{IL}		−0.3		0.45	V
H input voltage	V_{IH}		0.7xV_{DD}		V_{DD}	V
L output voltage	V_{OL}	$I_{OL} = 1$ mA			0.45	V
H output voltage	V_{OH}	$I_{OH} = 1$ mA	0.75xV_{DD}			V

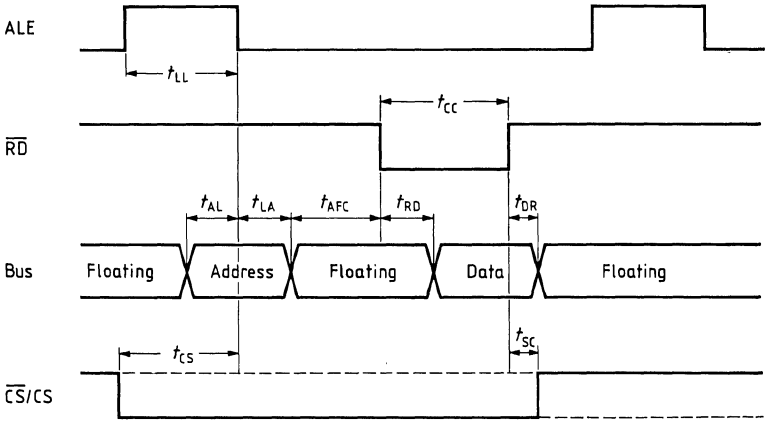
AC characteristics:

T_{amb} = 25°C to 70°C; V_{DD} = 5 V; V_{SS} = 0 V

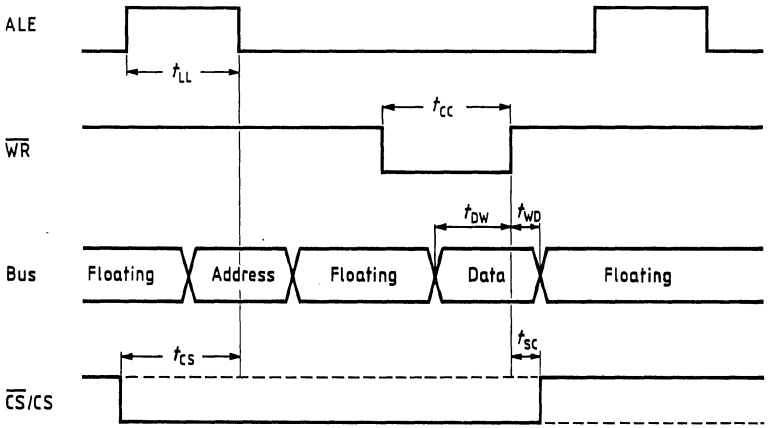
		Min.	Typ.	Max.	Unit
ALE pulse width	t_{LL}	120			ns
Address set-up before ALE	t_{AL}	60			ns
Address hold from ALE	t_{LA}	45			ns
$\overline{RD}$, $\overline{WR}$ pulse width	t_{CC}	400			ns
Data set-up before $\overline{WR}$↑	t_{DW}	433			ns
Data hold after $\overline{WR}$↑	t_{WD}	33			ns
Data hold after $\overline{RD}$↑	t_{DR}	0		95	ns
$\overline{RD}$↓ to data out	t_{RD}			250	ns
Address float to $\overline{RD}$↓	t_{AFC}	150			ns
CS or $\overline{CS}$ before ALE	t_{CS}	100			ns
CS or $\overline{CS}$ after $\overline{WR}$ or $\overline{RD}$	t_{SC}	100			ns

Timing waveforms

Read



Write



SAB 81C52P
256 x 8-Bit Static CMOS RAM NMOS-Compatible

Preliminary data **CMOS circuit**

The SAB 81C52P is a CMOS silicon gate, static random access memory (RAM), organized as 256 words by 8 bits. The multiplexed address and data bus allows to interface directly to 8-bit NMOS microprocessors/microcomputers without any timing or level problems, e.g. the families SAB 8085, SAB 8088, SAB 8048, SAB 8051, and SAB 80515.

All inputs and outputs are fully compatible with NMOS circuits, except CS 1. Data retention is given up to $V_{DD} \geqq 1.2$ V.*) The SAB 81C52P has three different inputs for two chip select modes which allow to inhibit either the address/data lines (AD 0 ... AD 7) and the control lines ($\overline{WR}$, $\overline{RD}$, ALE, CS 2, $\overline{CS\ 3}$), or only the control lines $\overline{RD}$, $\overline{WR}$.

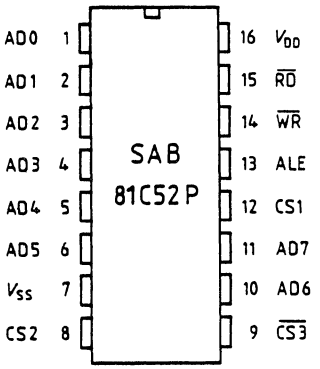
The power consumption is max. 5.5 µW in standby mode and max. 2.75 mW in operation. In standby mode, the power consumption will not increase if the control inputs are on undefined potential.

Features

- 256 x 8-bit organization
- standby mode
- compatible with the µC/µP families SAB 8085, SAB 8088, SAB 8048, SAB 8051, the new SAB 80515, etc.
- very low power dissipation
- data retention up to $V_{DD} \geqq 1.2$ V*)
- three different chip select inputs for two chip select modes
- no increasing power consumption in standby mode if the control inputs are on undefined potential

*Values for applications up to + 110 °C upon request.

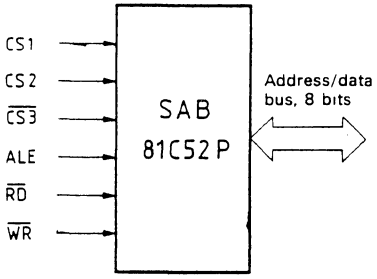
Pin configuration
(top view)



Pin designation

Pin No.	Symbol	Function
1–6 10, 11	AD Ø–7	Address/data lines
12	CS 1	Chip select 1 (standby) active low; inhibits all lines including control lines
13	ALE	Address latch enable
14	$\overline{WR}$	Write enable
15	$\overline{RD}$	Read enable
16	V_{DD}	Power supply
7	V_{SS}	GND
8	CS 2	Chip select 2; inhibits control inputs $\overline{RD}$, $\overline{WR}$
9	$\overline{CS 3}$	Counterpart to CS 2

Logic symbol

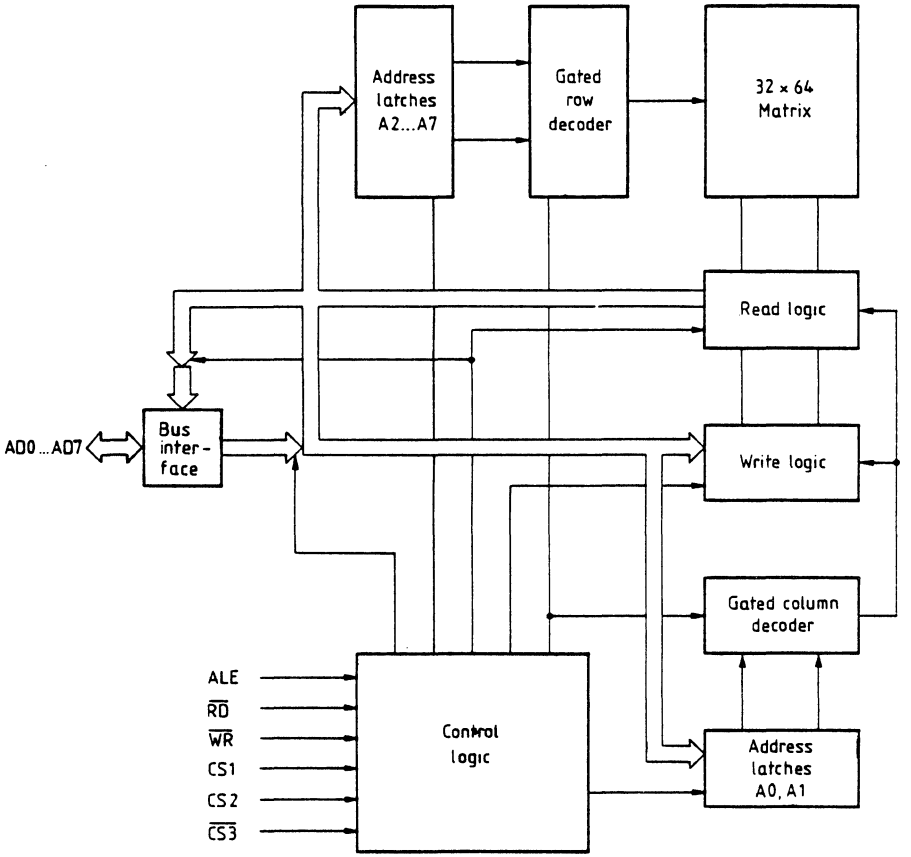


Truth table

CS 1	CS 2	$\overline{CS 3}$	ALE	$\overline{RD}$	$\overline{WR}$	AD Ø ... AD 7	Function
L	*	*	*	*	*	floating (tristate)	standby
H	X	X	H	H	H	addresses to memory	store addresses
H	H	L	L	L	H	data from memory	read
H	H	L	L	H	L	data to memory	write
H	L	X	L	X	X	floating (tristate)	none
H	X	H	L	X	X	floating (tristate)	none

*: Level = V_{SS} ... V_{DD}
X: Level = LOW or HIGH

Block diagram



Maximum ratings

Maximum ratings are absolute limits. The integrated circuit may be destroyed if only a single value is exceeded.

Supply voltage referred to GND (V_{SS})	V_{DD}	−0.3 to 6	V
All input and output voltages	V_{IM}	V_{SS} −0.3	V
		V_{DD} +0.3	V
Total power dissipation	P_{tot}	250	mW
Power dissipation for each output	P_Q	50	mW
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	−55 to 125	°C
Thermal resistance	$R_{th\,SA}$	70	K/W

Operating range

In the operating range, the functions shown in the circuit description will be fulfilled. Deviations from the electrical characteristics may be possible.

Supply voltage	V_S	4.5 to 5.5	V
Ambient temperature	T_{amb}	−40 to 85*)	°C

*) Values for applications up to 110°C upon request

Electrical Characteristics

The electrical characteristics include the guaranteed tolerance of the values which the IC stays within for the specified operating range.

The typical characteristics are average values which can be expected from production. Unless otherwise specified, the typical characteristics apply to T_{amb} and the specified supply voltage.

DC characteristics

T_{amb} = −40 to +85°C*); V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V

		Test conditions	min.	max.	
Standby supply current	I_{DD}			1	µA
Supply current	I_{DD}	f = 1 MHz		500	µA
Standby voltage for data retention	V_{DD}		1.2		V
L input current (for each input)	I_{IL}	V_I = 0 to 6 V		1	µA
Output leakage current	I_{QIK}	V_Q = 0 to 6 V tristate		1	µA
L input voltage	V_{IL}	except CS 1	2.2	0.8	V
H input voltage	V_{IH}	except CS 1			
L output voltage	V_{QL}	I_{QL} = 1 mA		0.4	V
H output voltage	V_{QH}	I_{QH} = 1 mA	2.6		V
L input voltage CS1	V_{IL}			1	V
H input voltage CS1	V_{IH}		4		V

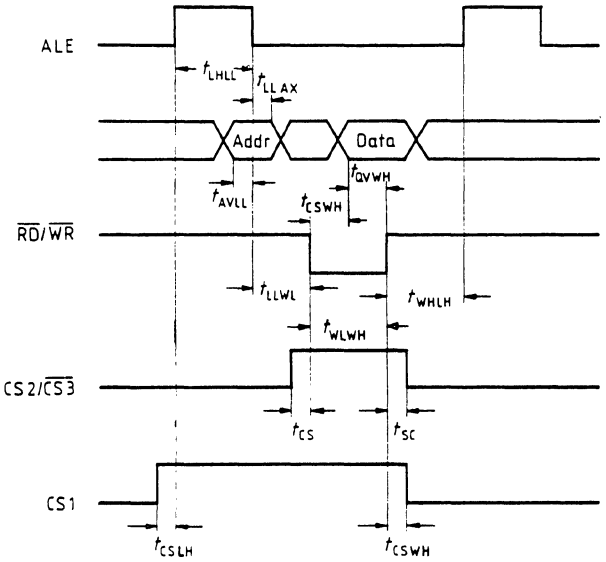
AC characteristics

T_{amb} = −40 to 85°C*), V_{DD} = 4.5 to 5.5 V; V_{SS} = 0 V

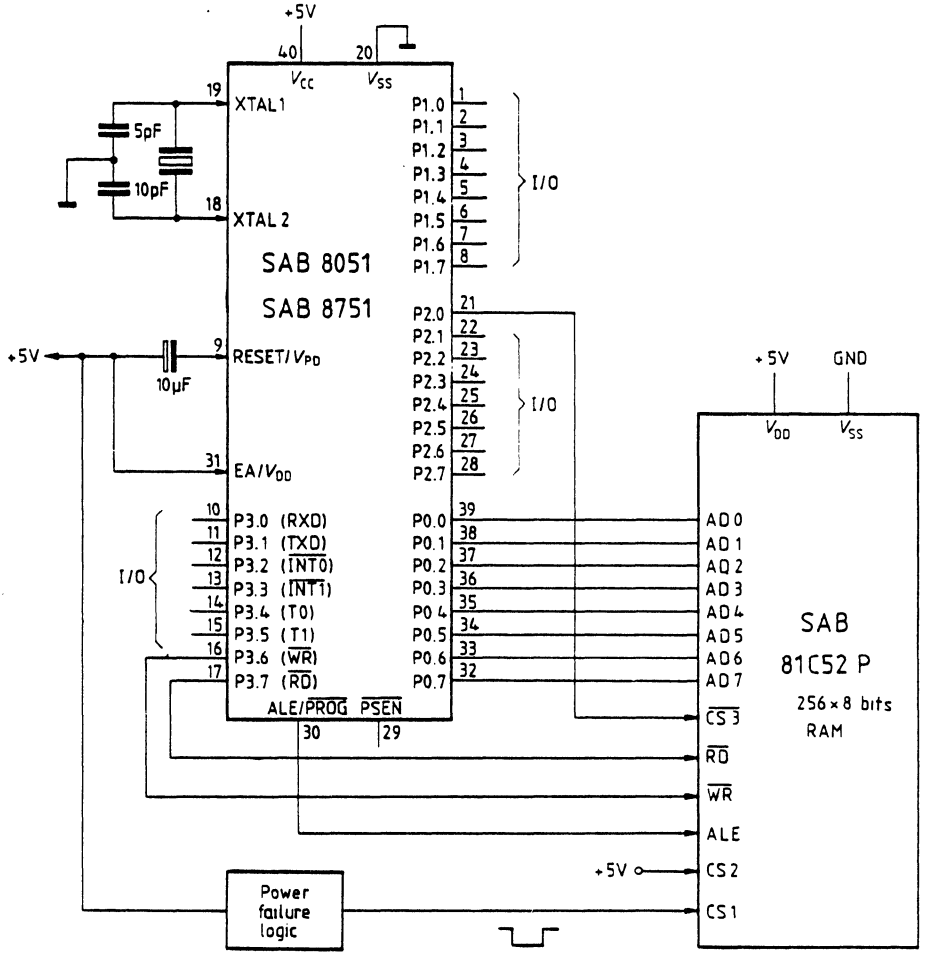
		min.	max.	
ALE pulse width	t_{LHLL}	100		ns
ALE LOW to $\overline{RD}$ LOW	t_{LLRL}	50		ns
$\overline{RD}$ HIGH to ALE HIGH	t_{RHLH}	30		ns
ALE LOW to $\overline{WR}$ LOW	t_{LLWL}	50		ns
$\overline{WR}$ HIGH to ALE HIGH	t_{WHLH}	30		ns
Address setup before ALE	t_{AVLL}	25		ns
Address hold after ALE	t_{LLAX}	20		ns
$\overline{WR}$ or $\overline{RD}$ pulse width	t_{WLWH}	250		ns
Data setup before $\overline{WR}$	t_{QVWH}	100		ns
Data hold after $\overline{RD}$	t_{RHDX}		50	ns
Chip select (2, 3) before $\overline{RD}$, $\overline{WR}$	t_{CS}	50		ns
Chip select (2, 3) after $\overline{RD}$, $\overline{WR}$	t_{SC}	50		ns
Chip select 1 before ALE	t_{CSLH}	20		ns
Chip select 1 after $\overline{RD}$, $\overline{WR}$	t_{CSWH}	50		ns
Output delay time	t_{RLDV}		200	ns
Input capacitance against V_{SS} (for each input)	C_I		10	pF

*) Values for applications up to 110°C upon request

Timing diagram



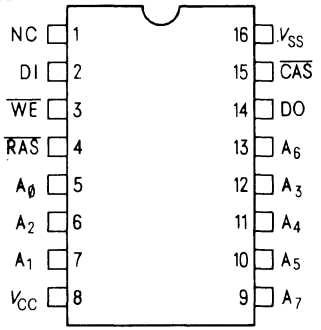
Application circuit
SAB 81C52 P with the µC SAB 8051



HYB 4164-P1, HYB 4164-P2, HYB 4164-P3
65,536-Bit Dynamic Random Access Memory (RAM)

- 65,536 X1 bit organization
- Industry standard 16-pin JEDEC configuration
- Single +5 V ±10% power supply
- Low power dissipation
  - 150 mW active (max.)
  - 20 mW standby (max.)
- 120 ns access time,
  220 ns cycle (HYB 4164-P1)
  150 ns access time,
  280 ns cycle (HYB 4164-P2)
  200 ns access time,
  330 ns cycle (HYB 4164-P3)
- All inputs and outputs TTL compatible
- High over- and undershooting capability on all inputs
- Low supply current transients
- $\overline{CAS}$ controlled output providing latched or unlatched data
- Common I/O capability using "early write" operation
- Read-Modify-Write, $\overline{RAS}$-only refresh, hidden refresh
- 256 refresh cycles with 4 ms long refresh period
- Page Mode Read and Write

Pin Configuration

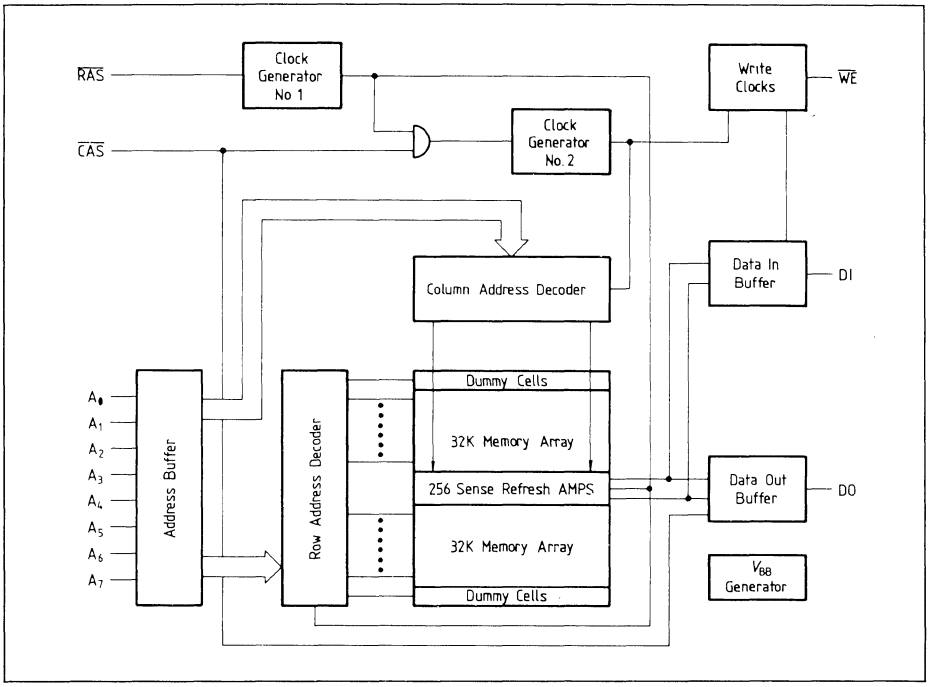


Pin Names	
$A_0 - A_7$	Address Inputs
$\overline{CAS}$	Column Address Strobe
DI	Data In
NC	No Connection
DO	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5 V)
V_{SS}	Ground (0 V)

The HYB 4164 is a 65536-word by 1-bit, MOS random access memory circuit fabricated with Siemens new 5-Volt only n-channel silicon gate technology, using double layer polysilicon. To protect the chip against α-radiation a Siemens proprietary chip cover is used. The HYB 4164 uses single transistor dynamic storage cells and dynamic control circuitry to achieve high speed at very low power dissipation.
Multiplexed address inputs permit the HYB 4164 to be packaged in an industry standard 16-pin dual-in-line package.

System oriented features include single power supply with ±10% tolerance, on-chip address and data latches which eliminate the need for interface registers and fully TTL compatible inputs and outputs, including clocks.
In addition to the usual read, write and read-modify-write cycles, the HYB 4164 is capable of early and delayed write cycles, $\overline{RAS}$-only refresh and hidden refresh. Common I/O capability is given by using "early write" operation.

Block Diagram



Functional Description

Addressing (A_0-A_7)

For selecting one of the 65536 memory cells, a total of 16 address bits are required. First 8 row-address bits are set-up on pins A_0 through A_7 and latched onto the row address latches by the Row Address Strobe ($\overline{RAS}$). Then the 8 column-address bits are set-up on pins A_0 through A_7 and latched onto the column address latches by the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or shortly after the falling edge of $\overline{RAS}$ and $\overline{CAS}$ respectively. $\overline{CAS}$ is internally gated by $\overline{RAS}$ to permit triggering of column address latches as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-address to column-address.
It should be noted that $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip-select activating the column decoder and the input and output buffers.

Write Enable ($\overline{WE}$)

The read or write mode is selected with the $\overline{WE}$ input. A logic high (V_{IH}) on $\overline{WE}$ dictates read mode; logic low (V_{IL}) dictates write mode. The data input is disabled when the read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data output (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data Input (DI)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latch. In an early write cycle $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with set-up and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with set-up and hold times referenced to this signal.

Power On

An initial pause of 200 μs is required after power-up followed by a minimum of eight (8) initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh) prior to normal operation. The current requirement of the HYB 4164 during power on is, however, dependent upon the inut levels $\overline{RAS}$, $\overline{CAS}$ and the rise time of V_{CC}, as shown in the following diagram.

Data Output (DO)

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high-impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from the transition of $\overline{RAS}$ when t_{RCD} (min) is satisfied, or after t_{CAC} from the transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). $\overline{CAS}$ going high returns the ouput to a high-impedance state. In an early write cycle the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle.

Hidden Refresh

$\overline{RAS}$ only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.
Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} from a previous memory read cycle.

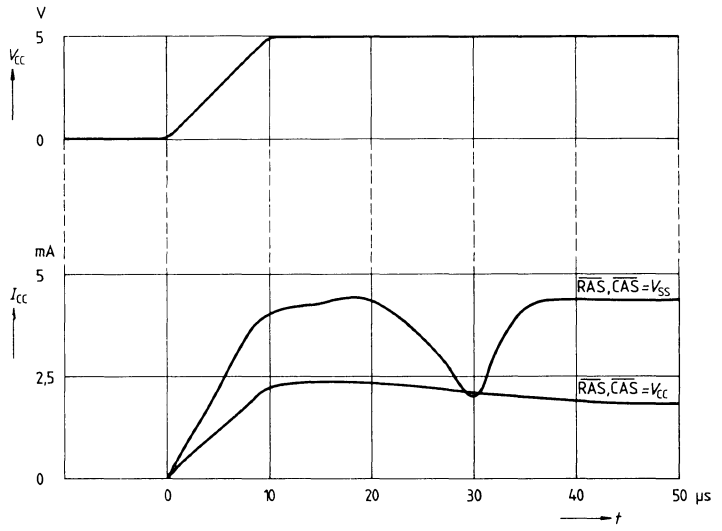
Refresh Cycle

A refresh operation must be performed at least every four milli-seconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output signal during refresh. Strobing each of the 256 row addresses (A_0 through A_7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

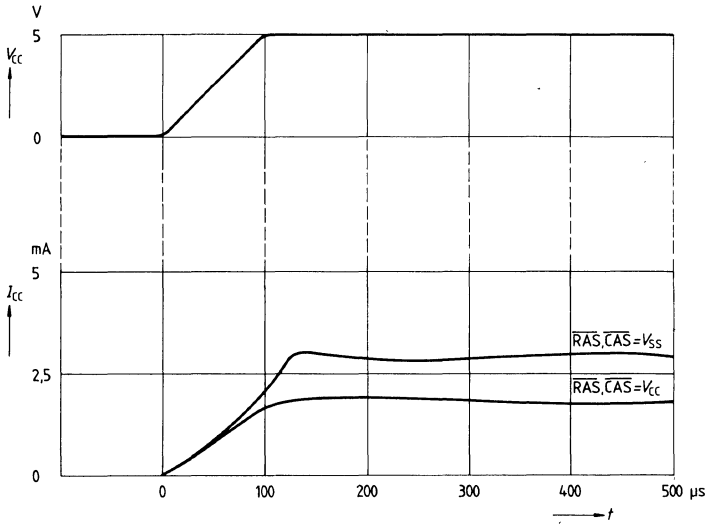
Page Mode

Page Mode operations allows a faster data transfer rate. This is achieved by maintaining the row address while strobing successive column addresses onto the chip. The time required to set-up and strobe sequential row addresses for the same page is eliminated.

Current Consumption During Power up
(V_{CC} rise time 10 μs)



Current Consumption During Power up
(V_{CC} rise time 100 µs)



Absolute Maximum Ratings [1]

Operating Temperature Range	0 to + 70 °C
Storage Temperatures Range	−65 to +150 °C
Voltages on any Pin relative to V_{SS}	−1 to +7.0 V
Power Dissipation	1.0 W
Short Circuit Output Current	50 mA

A.C. Test Conditions

Input Pulse Levels		0.8 to 2.4 V
Input Rise and Fall Times	5 ns between	0.8 and 2.4 V
Input Timing Reference Levels		0.8 and 2.4 V
Output Timing Reference Levels		0.4 and 2.4 V
Output Load		Equivalent to 2 standard TTL Loads and 100 pF

1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

T_A = 0 to 70 °C; V_{CC} = +5 V ±10%

Symbol	Parameter	Limit Values		Units	Test Conditions [1]
		Min.	Max.		
V_{IH}	High level input voltage (all inputs) [2]	2.4	6.0	V	–
V_{IL}	Low level input voltage [2]	−1.0	0.8		
V_{OH}	Output high voltage	2.4	V_{CC}		I_O = −5 mA
V_{OL}	Output low voltage	–	0.4		I_O = 4.2 mA
I_{CC1}	Average V_{CC} power supply current [3]	–	27	mA	–
I_{CC2}	Standby V_{CC} power supply current	–	3.5		$\overline{RAS}$ at V_{IH} $\overline{CAS}$ at V_{IH}
I_{CC3}	Average V_{CC} current during refresh [3]	–	24		$\overline{RAS}$ cycling $\overline{CAS}$ at V_{IH}
I_{CC4}	Page mode current [3]	–	20	mA	$\overline{RAS}$ at V_{IL} $\overline{CAS}$ cycling
$I_{I(L)}$	Input leakage current (any input) [4]	−10	10	µA	–
$I_{O(L)}$	Output leakage current	−10	10		$\overline{CAS}$ at V_{IH} V_O = V_{SS} to V_{CC}

Capacitances [5]

Symbol	Parameter [6]	Limit Values		Units	Test Conditions
		Min.	Max.		
C_{I1}	Input capacitance (A_0–A_7), DI	–	5	pF	–
C_{I2}	Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	–	10		–
C_O	Output capacitance	–	7		DO disabled

Notes:

1) An initial pause of 200 µs is required after power-up followed by a minimum of eight initialization cycles prior to normal operation.

2) Over- and undershooting on input levels of 6.5 V or − 2 V for a period of 30 ns will not influence function or reliability of the device.

3) I_{CC} depends on frequency of operation, Maximum current is measured at 260 ns cycle rate.

4) All device pins at 0 V and pin under test at + 5.5V.

5) Capacitance measured with a Boonton Meter 72 BD or effective capacitance calculated from the equation

$$C = \frac{I \cdot \triangle t}{\triangle V} \text{ with } \triangle V = 3 \text{ V}.$$

6) This parameter is periodically sampled and not 100% tested.

A.C. Characteristics [1]

T_A = 0 to +70 °C; V_{CC} = +5 V ±10%

Symbol	Parameter	Limit Values						Units
		HYB 4164-P1		HYB 4164-P2		HYB 4164-P3		
		Min.	Max.	Min.	Max.	Min.	max.	
t_{RC}	Random read or write cycle time [2]	220	–	280	–	330	–	ns
t_{RWC}	Read/write cycle time [2]	220	–	280	–	330	–	
t_{PC}	Page mode cycle time	125	–	170	–	225	–	
t_{RMWC}	Read/modify/write cycle time [2]	255	–	280	–	330	–	
t_{RAC}	Access time from $\overline{RAS}$ [3] [4]	–	120	–	150	–	200	
t_{CAC}	Access time from $\overline{CAS}$ [3] [5] [7]	–	80	–	100	–	135	
t_{OFF}	Output buffer turn-off delay [6]	–	35	–	40	–	50	
t_{RP}	$\overline{RAS}$ precharge time	90	–	100	–	120	–	
t_{RAS}	$\overline{RAS}$ pulse width	120	10^4	150	10^4	200	10^4	
t_{RSH}	$\overline{RAS}$ hold time	80	–	100	–	135	–	
t_{CSH}	$\overline{CAS}$ hold time	120	–	150	–	200	–	
t_{CAS}	$\overline{CAS}$ pulse width	80	–	100	–	135	–	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time [7]	25	40	30	50	35	65	
t_{ASR}	Row address set-up time	0	–	0	–	0	–	
t_{RAH}	Row address hold time	15	–	20	–	25	–	
t_{ASC}	Column address set-up time	0	–	0	–	0	–	
t_{CAH}	Column address hold time	40	–	45	–	55	–	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	80	–	95	–	120	–	
t_{RCS}	Read command set-up time (RMW)	0	–	0	–	0	–	
t_{RCH}	Read command hold time	0	–	0	–	0	–	
t_{WCH}	Write command hold time	40	–	45	–	55	–	

Symbol	Parameter	Limit Values						Units
		HYB 4164-P1		HYB 4164-P2		HYB 4164-P3		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95	–	110	–	120	–	ns
t_{WCS}	Write command set-up time [3]	−10	–	−10	–	−10	–	
t_{WP}	Write command pulse width	40	–	45	–	55	–	
t_{RWL}	Write command to $\overline{RAS}$ lead time	40	–	50	–	60	–	
t_{CWL}	Write command to $\overline{CAS}$ lead time	40	–	50	–	60	–	
t_{DS}	Data in set-up time	0	–	0	–	0	–	
t_{DH}	Data in hold time [9]	40	–	45	–	55	–	
t_{DHR}	Data in hold time [9] referenced to $\overline{RAS}$	95	–	110	–	120	–	
t_{CP}	$\overline{CAS}$ precharge time (Page mode)	35	–	60	–	80	–	
t_{CPN}	$\overline{CAS}$ precharge time [10]	40	–	50	–	60	–	
t_{RF}	Refresh period	–	4.0	–	4.0	–	4.0	ms
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ delay [8]	60	–	60	–	80	–	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ delay [8]	110	–	120	–	145	–	
t_T	Transition time (Rise and Fall)	3	35	3	35	3	50	

Notes:

1) V_{IH} and V_{IL} are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

2) The specifications for $t_{RC(min)}$ and $t_{RWC(min)}$ are used only to indicate cycle time at which proper operation over full temperature range ($0\ °C \leq T_A \leq 70\ °C$) is assured.

3) Measured with a load equivalent to two standard TTL loads and 100 pF.

4) Assumes that $t_{RCD} \leq t_{RCD(max)}$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

5) Assumes that $t_{RCD} \geq t_{RCD(max)}$.

6) $t_{OFF(max)}$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

7) Operation within the $t_{RCD(max)}$ limit ensures that $t_{RAC(max)}$ can be met. $t_{RCD(max)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD(max)}$ limit, then access time is controlled exclusively by t_{CAC}.

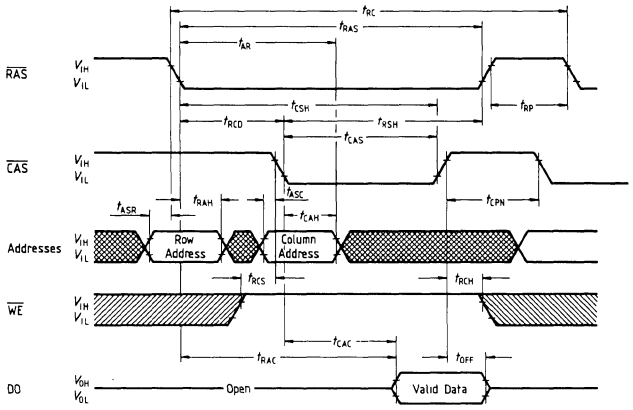
8) t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS(min)}$, the cycle is an early write cycle and the data-out will remain open circuit (high impedance) throughout the entire cycle: If $t_{CWD} \geq t_{CWD(min)}$ and $t_{RWD} \geq t_{RWD(min)}$ the cycle is a read-write cycle and the data will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

9) t_{DS} and t_{DH} are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.

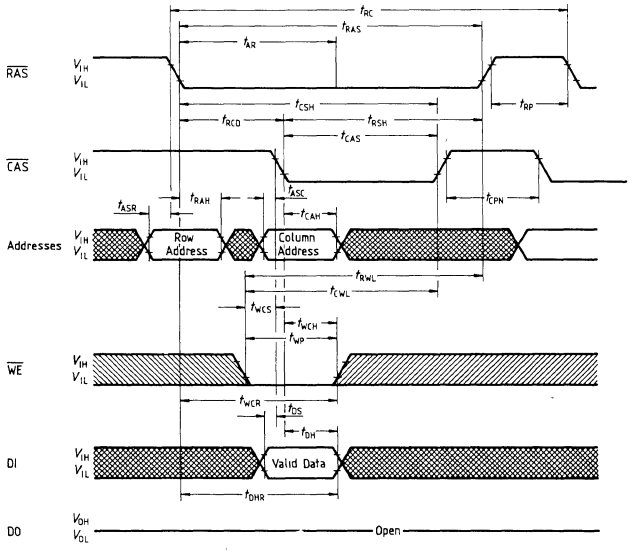
10) Not for page mode.

Waveforms

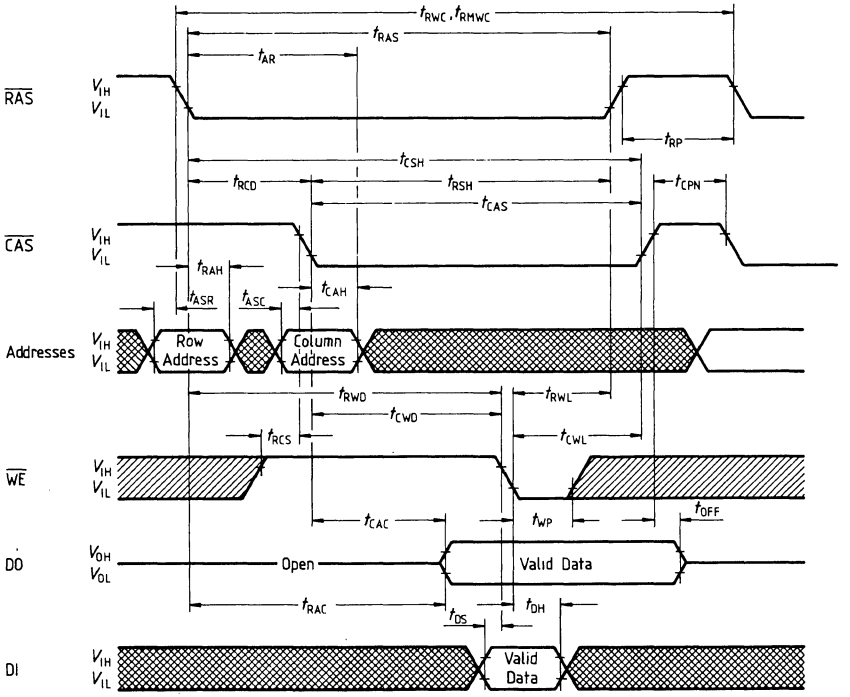
Read cycle



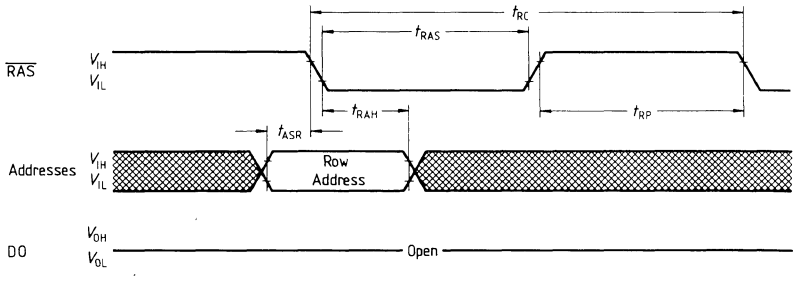
Write cycle (Early write)



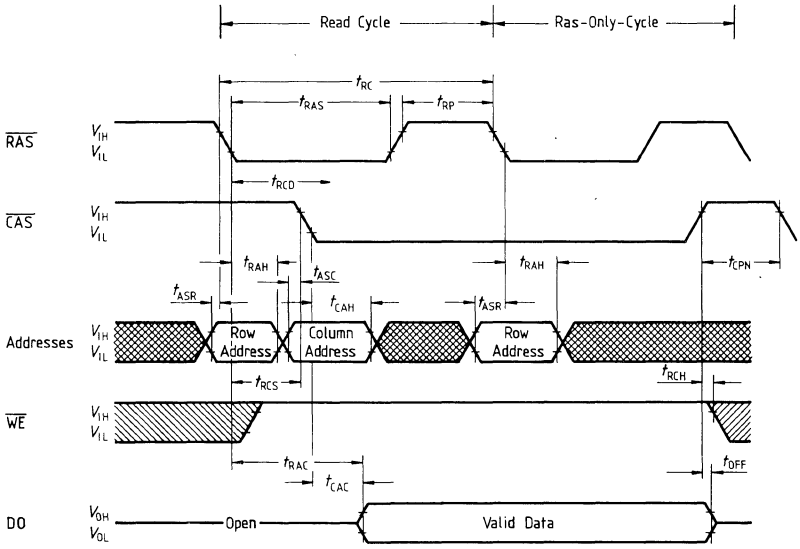
Read-write/Read-modify-write cycle



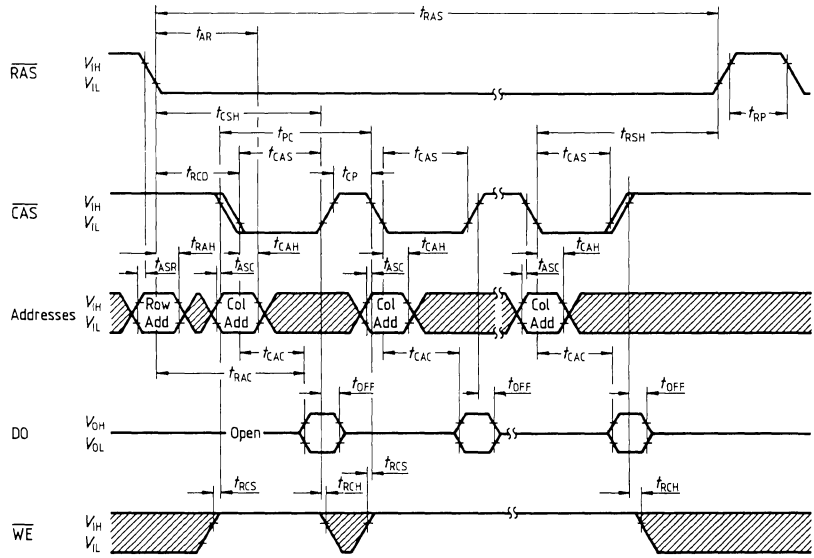
"$\overline{\text{RAS}}$-ONLY" REFRESH CYCLE
Note $\overline{\text{CAS}} = V_{IH}$; $\overline{\text{WE}}$ = Don't care



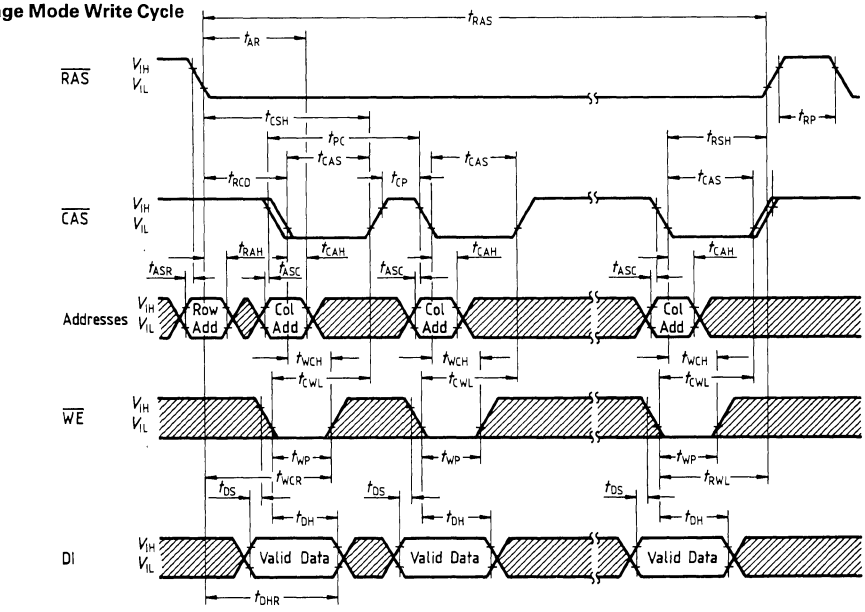
Hidden Refresh



Page Mode Read Cycle

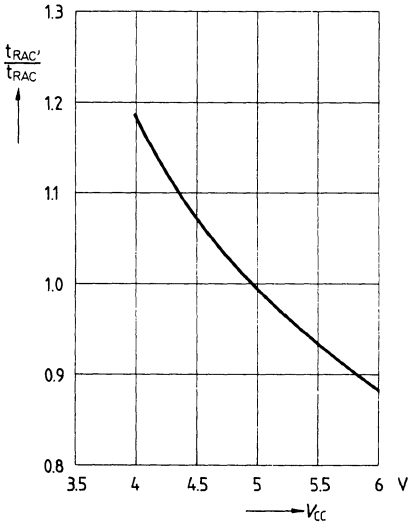


Page Mode Write Cycle

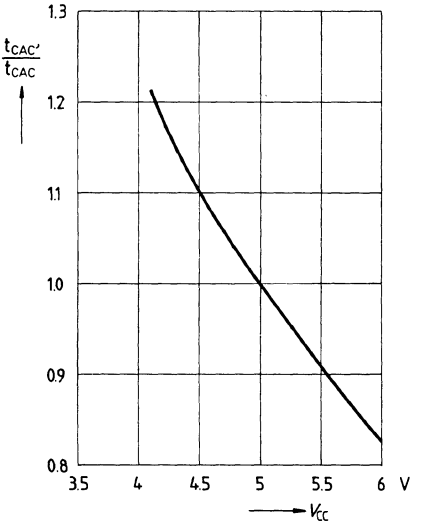


Typical Access Time Curves

$\overline{\text{RAS}}$ Access Time
vs. Supply Voltage
$T_A = 25\,°C$

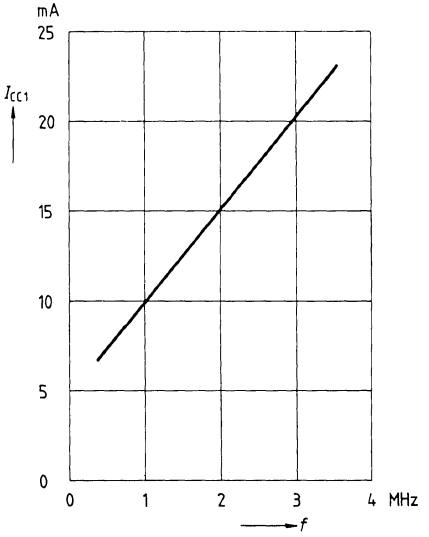


$\overline{\text{CAS}}$ Access Time
vs. Supply Voltage
$T_A = 25\,°C$

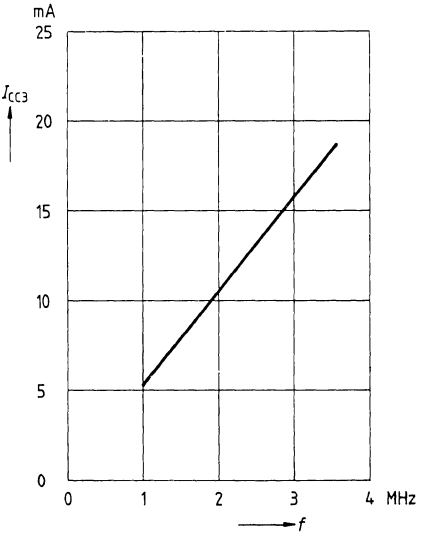


Typical Current Consumption Curves

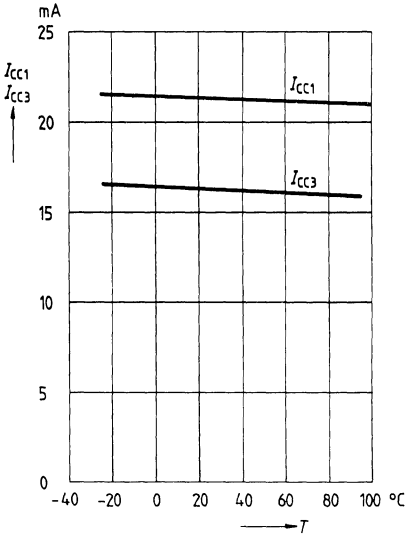
I_{CC1} (Average) vs. Cycle Rate
V_{CC} = 5.5 V
Write Cycle
T_A = 25 °C



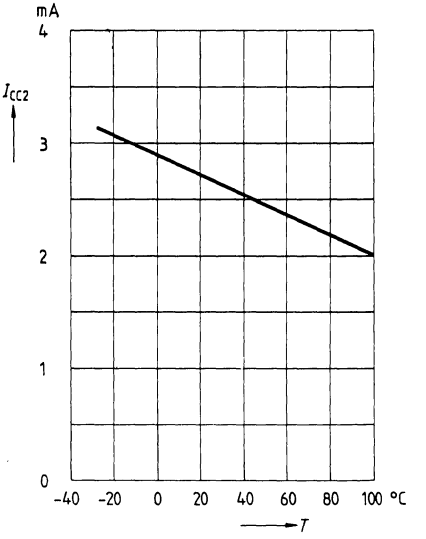
I_{CC3} (Average) vs. Cycle Rate
V_{CC} = 5.5 V
$\overline{RAS}$ Only Refresh Cycle
T_A = 25 °C



I_{CC} (Average) vs. Temperature (typ.)
V_{CC} = 5.5 V, t_{RC} = 280 nsec
I_{CC1} Write cycle
I_{CC3} $\overline{RAS}$ Only Refresh Cycle



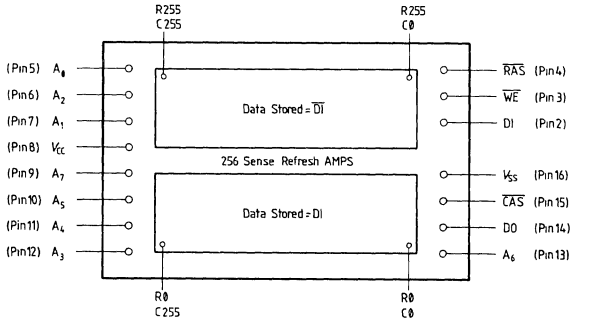
I_{CC2} Standby current vs. temperature (typ.)
V_{CC} = 5.5 V



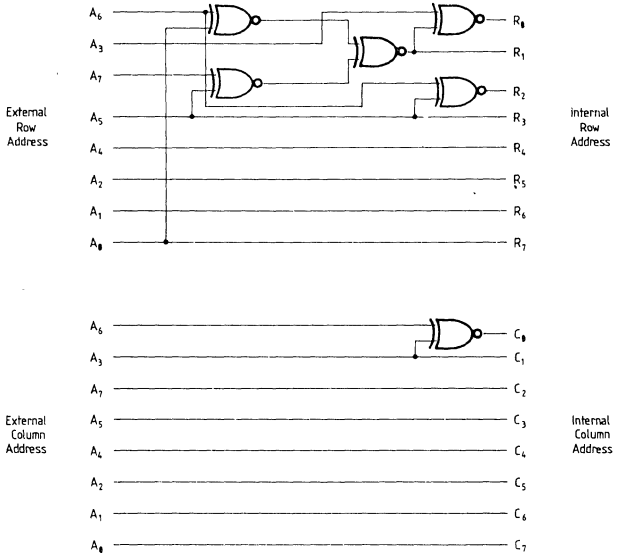
Topology Description

The evaluation and incoming testing of RAMs normally requires a description of the internal topology of the device in order to check for "worst case" pattern.

Internal Topology



Address Decoder scrambling



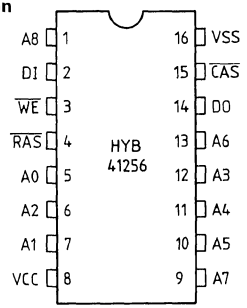
Internal Data Polarity
Data Stored = DI $\oplus$ $A_{0\,(ROW)}$

Note:
The logic symbol "exclusive nor" is used solely to indicate the logic function.

HYB 41256-12/-15/-20 262,144-Bit Dynamic Random Access Memory (RAM)

- 262,144 × 1-bit organization
- Industry standard 16 pins
- Single +5V supply, ±10% tolerance
- Low power dissipation:
  –385 mW active (max.)
  – 28 mW standby (max.)
- 120 ns access time
  220 ns cycle time (HYB 41256-12)
  150 ns access time
  260 ns cycle time (HYB 41256-15)
  200 ns access time
  330 ns cycle time (HYB 41256-20)
- All inputs and outputs TTL compatible
- On-chip substrate bias generator
- Three-state data output
- Read, write, read-modify-write, $\overline{RAS}$-only-refresh, hidden refresh
- Common I/O capability using "early write" operation
- Page mode read and write, read-write
- 256 refresh cycles with 4ms refresh period
- Redundancy incorporated for increasing yield
  – activation via laser links
  – roll-call mode as pretest with DI at 10V provides:
    redundancy signature
    individual address decoder
    scrambling

Pin configuration



Pin names

A0-A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
DI	Data In
DO	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
VCC	Power Supply (+5V)
VSS	Ground (0V)

The HYB 41256 is a 262,144 word by 1-bit dynamic Random Access Memory. This 5V-only component is fabricated with Siemens new high performance N-channel silicon gate technology. The use of tantalum polycide provides high speed. A Siemens proprietary chip cover protects the chip against α radiation.

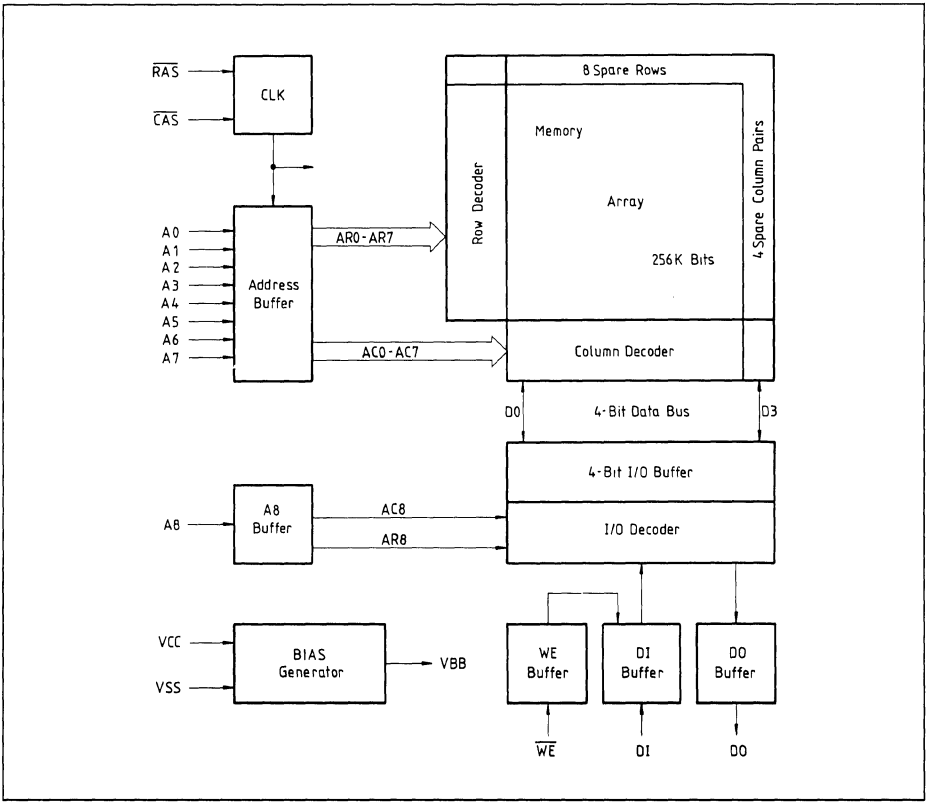
Nine multiplexed address inputs permit the HYB 41256 to be packaged in an industry standard 16-pin dual-in-line package. System-oriented features include single power supply with ±10% tolerance, on-chip address and data registers which eliminate the need for interface registers, and fully TTL compatible inputs and output, including clocks.

In addition to the usual read, write and read-modify-write cycles, the HYB 41256 is capable of early and late write cycles, $\overline{RAS}$-only refresh, and hidden refresh. Common I/O capability is given by using early write operation.

The HYB 41256 also features page mode which allows high-speed random access of bits in the same row.

The HYB 41256 has the capability of using laser links to perform redundancy. With the roll-call mode, which is a new test feature, the user can separate repaired devices easily, and additionally gets information on the individual row and column addresses which have been repaired and how they are substituted by redundant lines.

Block Diagram



Functional Description

Device Initialization

Since the HYB 41256 is a dynamic RAM with a single 5V supply, no power sequencing is required. For power-up, an initial pause of 200 microseconds is necessary for the internal bias generator to establish the proper substrate bias voltage. To initialize the nodes of the dynamic circuitry, a minimum of 8 active cycles of the Row Address Strobe ($\overline{RAS}$) has to be performed. This is also necessary after an extended inactive state of greater than 4 milliseconds.

Addressing (A0-A8)

For selecting one of the 262,144 memory cells, a total of 18 address bits are required. First 9 Row Address bits are set up on pins A0 through A8 and latched into the row address latches by the Row Address Strobe ($\overline{RAS}$). Then the 9 column address bits are set up on pins A0 through A8 and latched into the column address latches by the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. It should be noted that $\overline{RAS}$ is similar to a Chip Enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

Write enable ($\overline{WE}$)

The read or write mode is selected with the $\overline{WE}$ input. A logic high (VIH) on $\overline{WE}$ dictates read mode; logic low (VIL) dictates write mode. The data input is disabled when read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data ouput (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data input (DI)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latch. In an early write cycle $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

Data output (DO)

The output is three-state TTL compatible with a fan-out of two standard TTL loads. Data Out has the same polarity as Data In. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle or read-write cycle, the output is valid after tRAC from transition of $\overline{RAS}$ when tRCD (min) is satisfied, or after tCAC from transition of $\overline{CAS}$ when the transition occurs after tRCD (max). In an early write cycle, the output is always in the high impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle. With $\overline{CAS}$ going high the output returns to the high impedance state within tOFF.

Hidden refresh

$\overline{RAS}$-only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at VIL of a previous memory read cycle.

Refresh cycle

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any signal during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$, causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

Page mode

Page-mode operation allows effectively faster memory access by maintaining the row address and strobing random column addresses onto the chip. Thus, the time necessary to setup and strobe sequential row addresses for the same page is no longer required. The maximum number of columns that can be addressed in sequence is determined by tRAS, the maximum $\overline{RAS}$ low pulse width.

Absolute Maximum Ratings*)

Operating Temperature Range	0 to 70 °C
Storage Temperature Range	–65 to 150 °C
Voltage on Any Pin Relative to VSS	–1 to 7V
Voltage on DI Relative to VSS	–1 to 11V
Power Dissipation	1W
Data Out Current (Short Circuit)	50mA

DC Characteristics

TA = 0 to 70 °C, VSS = OV, VCC = +5 V ± 10%

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
VIH	Input high voltage (all inputs)	2.4	VCC+1	V	1) 2)
VIL	Input low voltage (all inputs)	–1.0	0.8		
VOH	Output high voltage	2.4	—		–
VOL	Output low voltage	–	0.4		
ICC1	Average VCC supply current –12 tRC=220ns –15 tRC=260ns –20 tRC=330ns	–	 85 70 60	mA	3)
ICC2	Standby VCC supply current		5		4)
ICC3	Average VCC supply current during $\overline{RAS}$-only refresh cycles –12 tRC=220ns –15 tRC=260ns –20 tRC=330ns		 65 55 45		3)
ICC4	Average VCC supply current during page mode –12 tPC=120ns –15 tPC=150ns –20 tPC=200ns		 65 55 45		
II(L)	Input leakage current (any input)	–	10	μA	–
IO(L)	Output leakage current ($\overline{CAS}$ at logic 1, 0 ≤ V out ≤ 5.5)				
VCC	VCC supply voltage	4.5	5.5	V	1)
VSS	VSS supply voltage	0	0		

Notes see page 5

Capacitance

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
CI1	Input capacitance (A0–A8)	–	6	pF	5
CI2	Input capacitance ($\overline{RAS}$, DI)		7		
CI3	Input capacitance ($\overline{CAS}$, $\overline{WE}$)		8		
CO	Output capacitance (DO, $\overline{CAS}$=VIH to disable output)				

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1) All voltages referenced to VSS.

2) Overshooting and undershooting on input levels of 6.5V or –2V for a period of 30ns max. will not influence function and reliability of the device.

3) ICC depends on frequency of operation. Maximum current is measured at the fastest cycle rate.

4) $\overline{RAS}$ and $\overline{CAS}$ are both at VIH.

5) Effective capacitance calculated from the equation

$C = \frac{I \cdot \Delta t}{\Delta V}$ with $\Delta V = 3V$ or measured with Boonton meter.

AC Test Conditions

Input pulse levels	0 to 3.0V
Input rise an fall times	5ns between 0.8 and 2.4V
Input timing reference levels	0.8 to 2.4V
Output timing reference levels	0.4 to 2.4V
Output load	equivalent to 2 standard TTL loads and 100pF

AC Characteristics

TA=0 to 70 °C, VCC=5 V ±10% (unless otherwise specified; see notes 6, 7, 8)

Symbol	Parameter	Limit values						Unit
		HYB 41256						
		–12		–15		–20		
		Min.	Max.	Min.	Max.	Min.	Max.	
tRC	Random read or write cycle time [9]	220	–	260	–	330	–	ns
tRWC	Read-modify-write cycle time [9]	265		310		390		
tRAC	Access time from $\overline{RAS}$ [10] [11]	–	120	–	150	–	200	
tCAC	Access time from $\overline{CAS}$ [10] [11] [12]		60		75		100	
tRAS	$\overline{RAS}$ pulse width	120	10^4	150	10^4	200	10^4	
tCAS	$\overline{CAS}$ pulse width	60	—	75	—	100	—	
tREF	Refresh period	—	4	—	4	—	4	ms
tRP	$\overline{RAS}$ precharge time	90	–	100	–	120	–	ns
tCRP	$\overline{CAS}$ to $\overline{RAS}$ precharge time	10		10		10		
tRCD	$\overline{RAS}$ to $\overline{CAS}$ delay time [13]	30	60	30	75	35	100	
tRSH	$\overline{RAS}$ hold time	60		75		100		
tCSH	$\overline{CAS}$ hold time	120		150		200		
tASH	Row address setup time	0		0		0		
tRAH	Row address hold time	20	—	20	—	25		
tASC	Column address setup time	0		0		0		
tCAH	Column address hold time	30		30		35	—	
tAR	Column address hold time referenced to $\overline{RAS}$ [14]	90		105		135		
tT	Transition time (rise and fall) [6]	3	50	3	50	3	50	ns
tRCS	Read command setup time	0	–	0	–	0		
tRCH	Read command hold time referenced to $\overline{CAS}$ [15]							
tRRH	Read command hold time referenced to $\overline{RAS}$ [15]	25		25		30		
tOFF	Output buffer turn-off delay [16]	0	30	0	40	0	50	
tWCS	Write command setup time [17]		–		–		–	
tWCH	Write command hold time	40		45		55		

Notes see page 7

Symbol	Parameter	Limit values						Unit
		HYB 41256						
		–12		–15		–20		
		Min.	Max.	Min.	Max.	Min.	Max.	
tWCR	Write command hold time referenced to $\overline{RAS}$ [14]	100		120		155		
tWP	Write command pulse width							
tRWL	Write command to $\overline{RAS}$ lead time	40		45		55		
tCWL	Write command to $\overline{CAS}$ lead time							
tDS	Data in setup time [18]	0		0		0		
tDH	Data in hold time [18]	40	–	45	–	55	–	ns
tDHR	Data in hold time referenced to $\overline{RAS}$ [14]	100		120		155		
tCWD	$\overline{CAS}$ to $\overline{WE}$ delay [17]	60		75		100		
tRWD	$\overline{RAS}$ to $\overline{WE}$ delay [17]	120		150		200		
tRRW	RMW cycle $\overline{RAS}$ pulse width	165		200		260		
tCRW	RMW cycle $\overline{CAS}$ pulse width	105		125		160		
tPC	Page mode cycle time [9]	120		150		200		
tPRWC	Page mode read-write cycle time	160		195		255		
tCP	Page mode $\overline{CAS}$ precharge time	50		65		90		

Notes:

6) VIH and VIL are reference levels to measure timing of input signals. Also, transition times are measured between VIH and VIL.

7) An initial pause of 200μs is required after power-up followed by a minimum of eight initialization cycles prior to normal operation.

8) The time parameters specified here are valid for a transition time of tT = 5ns for the input signals.

9) The specification for tRC (min), tRWC (min), and page-mode cycle time (tPC) are only used to indicate cycle time at which proper operation over full temperature range (0 °C ≤ TA ≤ 70 °C) is assured.

10) Measured with a load equivalent to two TTL loads and 100pF.

11) Assumes that tRCD ≤ tRCD (max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.

12) Assumes that tRCD ≥ tRCD (max).

13) Operation within the tRCD (max) limit ensures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.

14) tRCD + tCAH ≥ tAR min, tRCD + tDH ≥ tDHR min, tRCD + tWCH ≥ tWCR min.

15) Either tRRH or tRCH must be satisfied for a read cycle.

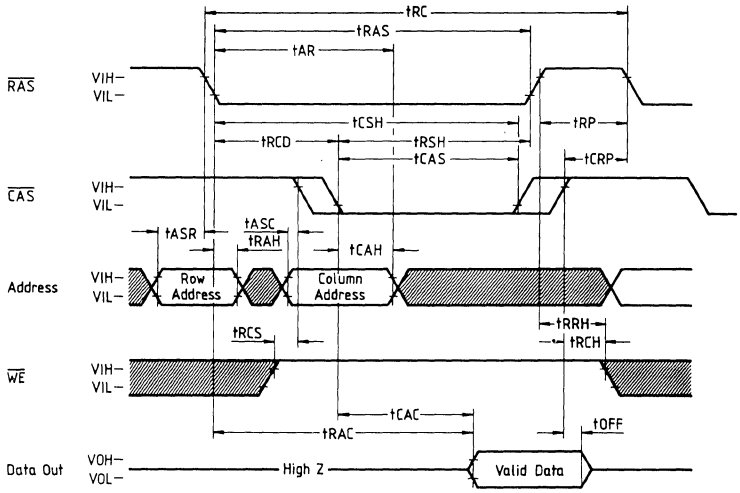
16) tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

17) tWCS, tCWD and tRWC are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If tWCS ≥ tWCS (min), the cycle is an early write cycle and the Data Out will remain open circuit (high impedance) throughout the entire cycle; if tCWD ≥ tCWD (min) and tRWD ≥ tRWD (min) the cycle is a read-write cycle and the Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the Data Out (at access time) is indeterminate.

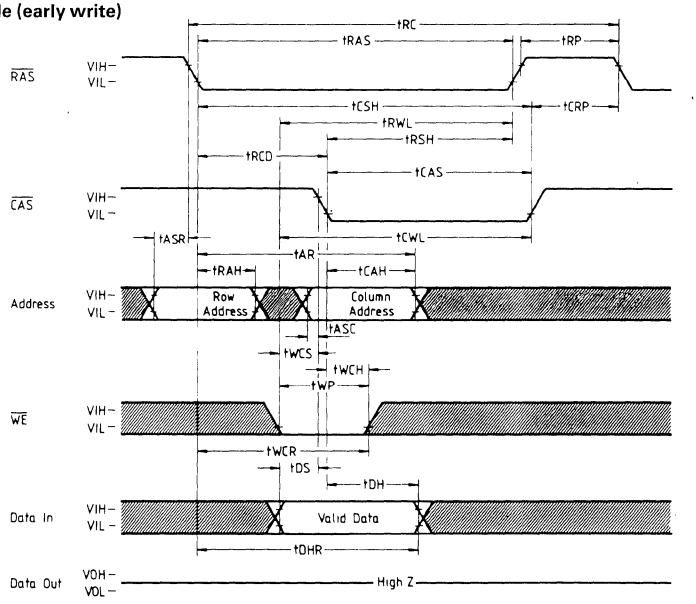
18) tDS and tDH are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write of read-modify-write cycles.

Waveforms

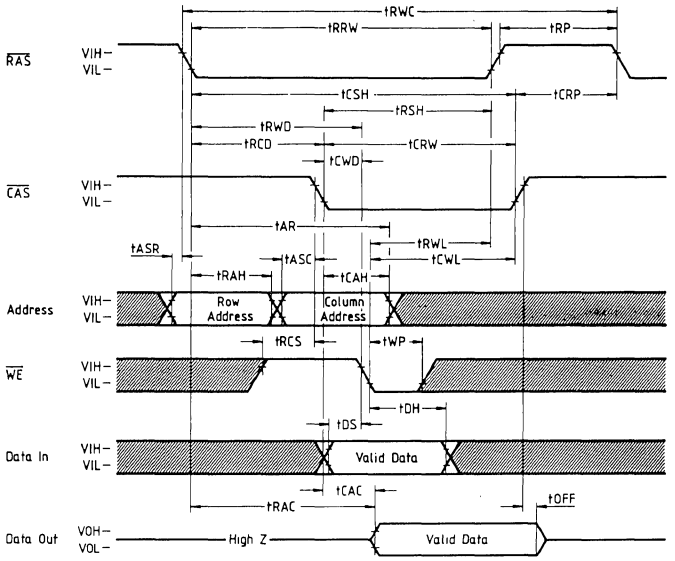
Read cycle



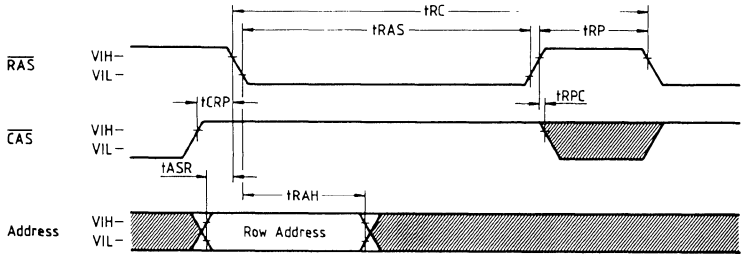
Write cycle (early write)



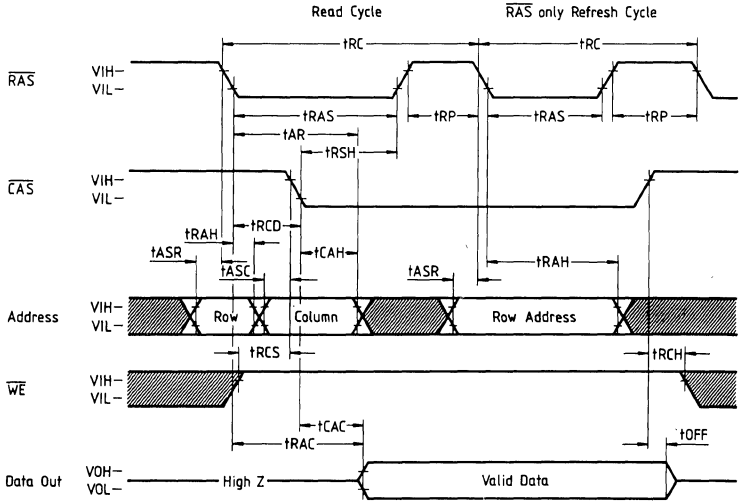
Read-modify-write or late write cycle



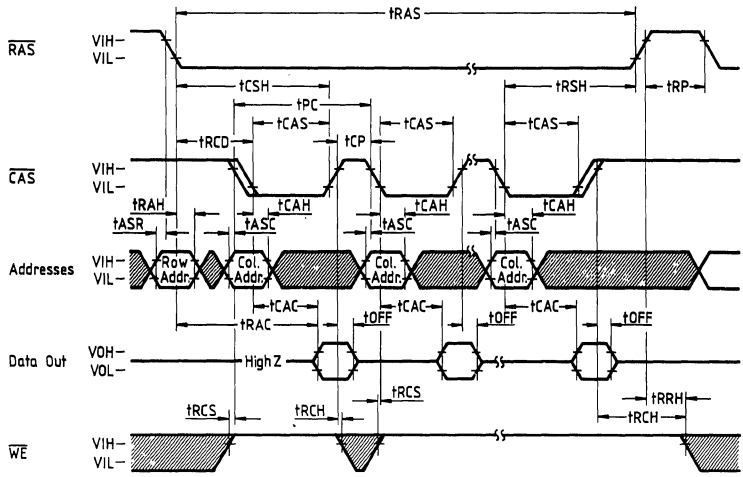
RAS-only refresh cycle
(DI and WE = don't care)



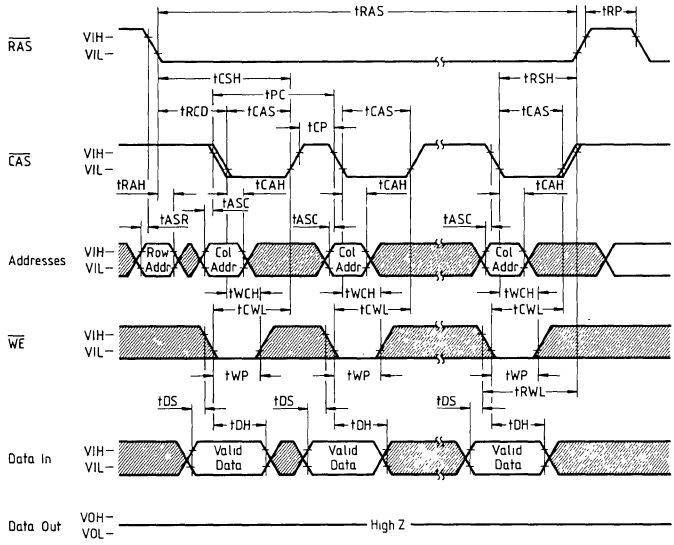
Hidden refresh cycle



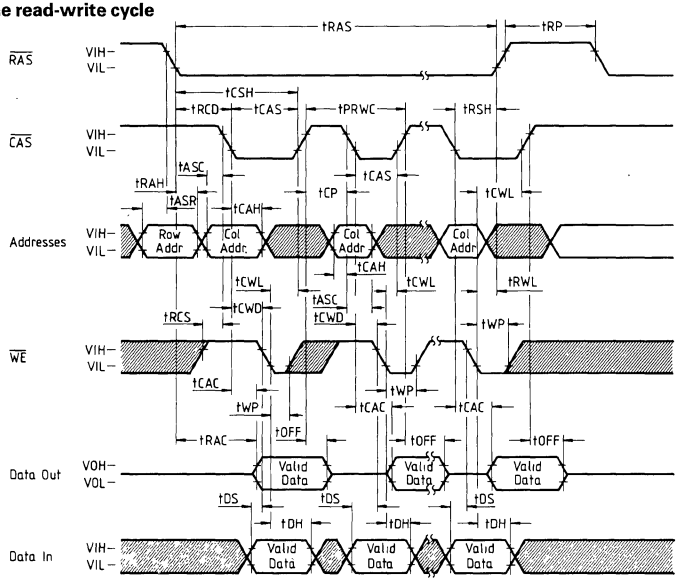
Page-mode read cycle



Page-mode write cycle



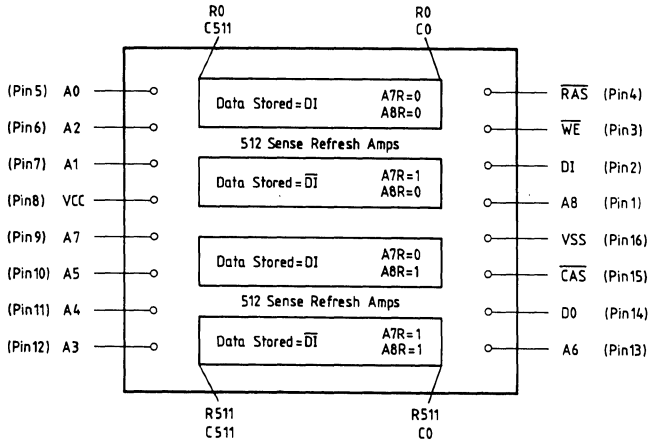
Page-mode read-write cycle



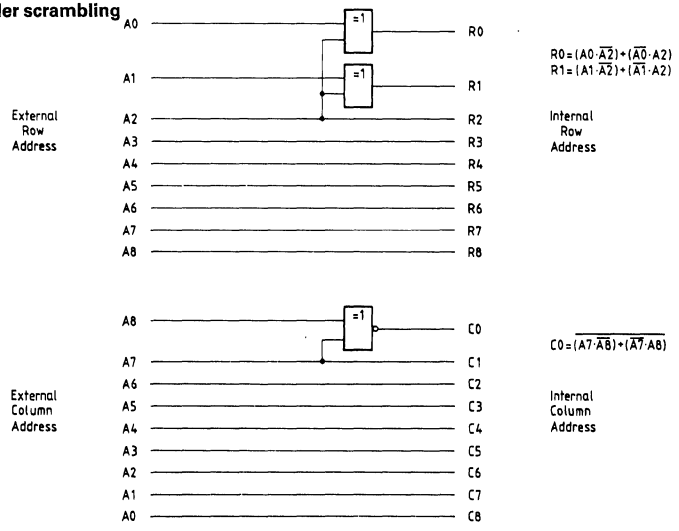
Address Decoder Scrambling (without redundancy)

The evaluation and incoming testing of RAMs normally requires a description of the internal address scrambling of the device in order to check for 'worst case' pattern.

Internal address scrambling



Address decoder scrambling



Note: The logic symbols are used solely to indicate the logic function.

Redundancy

Redundancy concept

The HYB 41526 takes advantage of the redundancy concept for increasing yield. This is done by providing the chip with a total of 8 spare rows and 4 spare column pairs. Two spare rows can be selected independently in each of four 64K cell arrays, and two spare column pairs can be selected independently in each of two 128K cell blocks. The spare lines can be selected by spare decoders which have to be programmed by laser technique during wafer probe.

Laser technology

For activation of redundant circuitry a laser pulse is used to open polycide links within the spare row and spare column decoders. The laser technique is used because it is mature and has proven reliable in a number of semiconductor applications including the implementation of redundant memory circuitry. Due to the fact, that the laser beam is very fine and can easily and accurately be positioned, and that it incorporates the energy for a controlled blow up of the polycide links, the laser technique is well suited for highly complex memory circuitry. All that results in a more efficient use of chip real estate.

Redundancy testability (roll-call mode)

With the redundancy concept two categories of devices, repaired and non-repaired ones, will be available. These two categories have to be separated easily and reliably by both, the manufacturer and the user (signature). When testing repaired devices, the reconfigurated address scrambling which results from activating spare rows and columns has to be taken into account for efficient device testing (individual bit map recognition).

The HYB 41256 has the capability of performing these two novel functions. It is done with a simple electrical test at the beginning of the final test or incoming inspection of each device (roll-call mode). The roll-call mode for performing both signature and individual bit map recognition can be activiated with DI at VIHR (10 V ± 10%).

Signature

With DI at VIHR and performing at least one $\overline{RAS}$-only cycle with a cycle time of tRCR on any address combination, in the case of non-repaired devices the Data Output is in the high-performance state as in normal $\overline{RAS}$-only cycles. For repaired devices the Data Output will go to VOLR or VOHR after the access time tRACR.

Individual bit map recognition

If the test for signature has shown a repaired device, additional tests can be performed to reognize which addresses have been repaired and how they are replaced by spare lines.
Row and column redundancy can be recognized independently.

Row redundancy

Row redundancy can be recognized with DI at VIHR and $\overline{CAS}$ at high, and $\overline{RAS}$-only cycles on all 512 row address combinations. The data output is low (VOLR) for non-repaired addresses, and is high (VOHR) for repaired addresses only. Within each 64K cell array, spare row 1 is always used if only one row is to be replaced. If two rows are to be replaced in an 64K cell array, spare row 2 is used to replace the defective row with the higher address.

Column redundancy

Column redundancy can be recognized with DI at VIHR, and early write cycles with tRCDR ≤ tRCD (min) on all 512 column address combinations. A8 row must be used to distinguish between the two 128K cell blocks. The data output is low (VOLR) for non-repaired addresses, and high (VOHR) for repaired addresses. Within each 128K cell block, spare column pair 1 is always used if only one column is to be replaced. Otherwise, spare column pair 2 is used to replace the defective column with the higher address.

Recommended operating conditions

Roll-call mode

DC operating conditions and characteristics (Full operating voltage and temperature range unless otherwise specified.)

Symbol	Parameter	Limit values			Unit
		Min.	Typ.	Max.	
VCC	Supply voltage HYB 41256–12, –15, –20 [1]	4.75	5.0	5.25	V
VSS	[1]	0	0	0	
VIH	Logic 1 voltage: All inputs (except DI)	2.4	—	VCC+1	
VIHR	Logic 1 voltage: DI [1] [2]	9.0	10	11	
VIL	Logic 0 voltage: All inputs [1]	–1.0	—	0.8	
VOHR	Output logic 1 voltage Iout = –5 mA [1]	2.0		—	
VOLR	Output logic 0 voltage Iout = –4.2 mA [1]	—		0.4	

1) All voltages referenced to VSS.

2) VIHR at DI must only be used for the roll-call-mode test and not for normal memory tests or applications. To avoid device damage, VIHR is to be applied after the initialization conditions (initial pause of 200 µs and 8 cycles) have been satisfied, and must never exceed 11V.

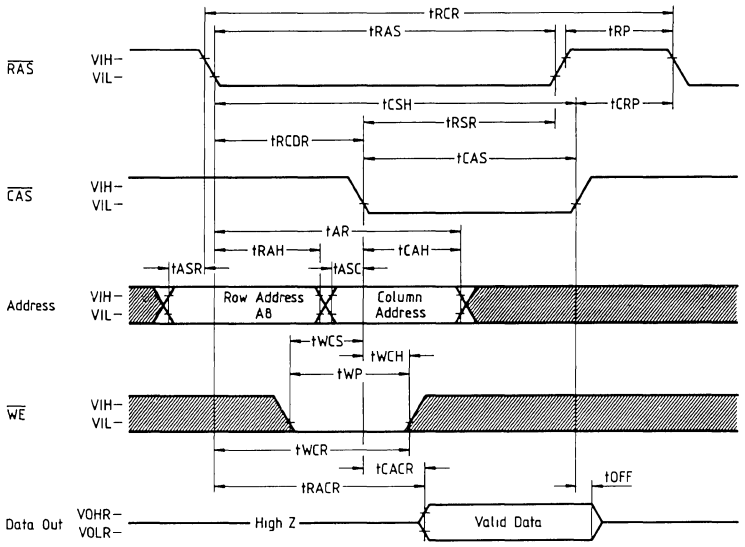
AC operating conditions and characteristics

(Full operating voltage and temperature range unless otherwise specified.)

Symbol	Parameter	Limit values						Unit
		HYB 41256						
		–12		–15		–20		
		Min.	Max.	Min.	Max.	Min.	Max.	
tRCR	Roll-call cycle time	330	—	390	—	490	—	ns
tRCDR	Roll-call $\overline{RAS}$ to $\overline{CAS}$ delay	—	30	—	30	35	35	
tRACR	Roll-call $\overline{RAS}$ access time	180	–	225	–	300	–	
tCACR	Roll-call $\overline{CAS}$ access time	90		115		150		

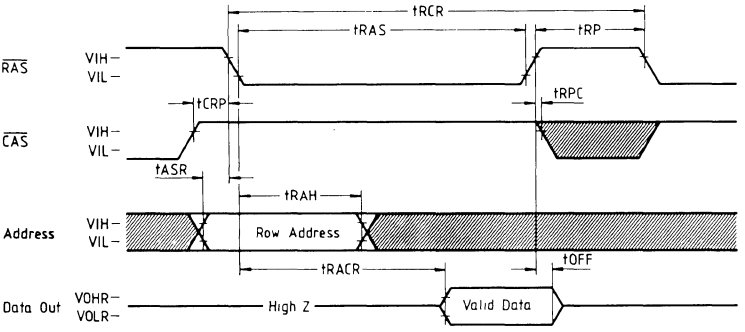
Column Redundancy

Early $\overline{CAS}$ – early write cycle
(DI at VIHR, tRCD = tRCD (min), row addresses A0 to A7 = don't care)

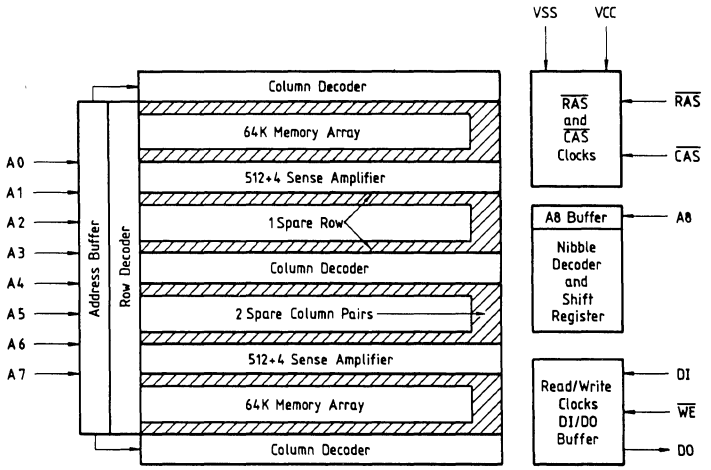


Row Redundancy and Signature

$\overline{RAS}$-only cycle
(DI at VIHR, $\overline{WE}$ = don't care)



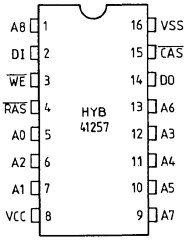
Siemens 256K DRAM Chip Topology



HYB 41257-12/-15/-20 262,144-Bit Dynamic Random Access Memory (RAM)

- 262,144 × 1-bit organization
- Industry standard 16 pins
- Single +5 V supply, ±10% tolerance
- Low power dissipation:
  – 385 mW active (max.)
  – 28 mW standby (max.)
- 120 ns access time
  220 ns cycle time (HYB 41257-12)
  150 ns access time
  260 ns cycle time (HYB 41257-15)
  200 ns access time
  330 ns cycle time (HYB 41257-20)
- All inputs and outputs TTL compatible
- Common I/O capability using "early write" operation
- Valid data during $\overline{CAS}$ precharge until start of next nibble cycle provides higher system data rate
- Fast nibble mode on read and write cycles via addresses A8 row and A8 column
  30 ns access time
  65 ns cycle time (HYB 41257-12)
  40 ns access time
  80 ns cycle time (HYB 41257-15)
  50 ns access time
  110 ns cycle time (HYB 41257-20)
- Read, write, read-modify-write, RAS-only-refresh, hidden refresh
- On-chip substrate bias generator
- Three-state data output
- 256 refresh cycles with 4 ms refresh period
- Redundancy incorporated for increasing yield
  – activation via laser links
  – roll-call-mode as pretest with DI at 10V provides: redundancy signature individual address decoder scrambling

Pin configuration

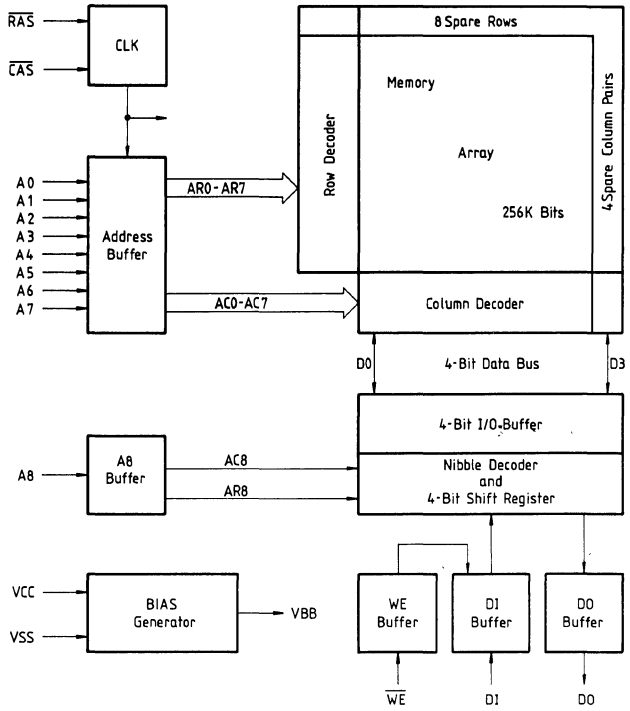


Pin names

A0 – A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
DI	Data In
DO	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
VCC	Power Supply (+5 V)
VSS	Ground (0 V)

The HYB 41257 is a 262,144 word by 1-bit dynamic Random Access Memory. This 5V-only component is fabricated with Siemens new high performance N-channel silicon gate technology. The use of tantalum polycide provides high speed. A Siemens proprietary chip cover protects the chip against α radiation.
Nine multiplexed address inputs permit the HYB 41257 to be packaged in an industry standard 16-pin dual-in-line package. System-oriented features include single power supply with ±10% tolerance, on-chip address and data registers which eliminate the need for interface registers, and fully TTL compatible inputs and output, including clocks. In addition to the usual read, write and read-modify-write cycles, the HYB 41257 is capable of early and late write cycles, $\overline{RAS}$-only refresh, and hidden refresh. Common I/O capability is given by using "early write" operation.
Nibble Mode is a new feature of the HYB 41257 allowing the user to perform a serial access of 4 bits at a high data rate by using an on-chip nibble shift register which is controlled by one set of addresses on pin 1 (A8 Row and A8 Column) and the $\overline{CAS}$ clock only.
The HYB 41257 has the capability of using laser links to perform redundancy. With the roll-call mode, which is a new test feature, the user can separate repaired devices easily, and additionally gets information on the individual row and column addresses which have been repaired and how they are substituted by redundant lines.

Block Diagram



Functional Description

Device Initialization

Since the HYB 41257 is a dynamic RAM with a single 5V supply, no power sequencing is required. For power-up, an initial pause of 200 microseconds is necessary for the internal bias generator to establish the proper substrate bias voltage. To initialize the nodes of the dynamic circuitry, a minimum of 8 active cycles of the Row Address Strobe ($\overline{RAS}$) has to be performed. This is also necessary after an extended inactive state of greater than 4 milliseconds.

Adressing (A0 – A8)

For selecting one of the 262,144 memory cells, a total of 18 address bits are required. First 9 Row Address bits are set up on pins A0 through A8 and latched into the row address latches by the Row Address Strobe ($\overline{RAS}$). Then the 9 column address bits are set up on pins A0 through A8 and latched into the column address latches by the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. It should be noted that $\overline{RAS}$ is similar to a Chip Enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

Write enable ($\overline{WE}$)

The read or write mode is selected with the $\overline{WE}$ input. A logic high (VIH) on $\overline{WE}$ dictates read mode; logic low (VIL) dictates write mode. The data input is disabled when read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data output (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data Input (DI)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latch. In an early write cycle $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

Data output (DO)

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data Out has the same polarity as Data In. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle or read-write cycle, the output is valid after tRAC from transition of $\overline{RAS}$ when tRCD (min) is satisfied, or after tCAC from transition of $\overline{CAS}$ when the transition occurs after tRCD (max.).
In an early write cycle, the output is always in the impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle. With $\overline{CAS}$ going high and $\overline{RAS}$ being high, the output returns to the high impedance state within tOFF.
For nibble-mode read cycles, the data output shows a novel function that gives advantages for system application. With $\overline{RAS}$ low the data output remains valid after and during $\overline{CAS}$ high. That gives time for a proper strobing of the data despite of system time tolerances, and increases the system data rate because the minimum $\overline{CAS}$ low time, tCAS and tNAS, can be realized more easily. With $\overline{CAS}$ going low for the next nibble cycle the data output returns to the high-impedance state within tNOFF. In a read, late write, or read-modify-write mode for a normal cycle or the last nibble cycle, the data output condition depends on whether $\overline{CAS}$ or $\overline{RAS}$ is brought high first. With $\overline{CAS}$ going high and $\overline{RAS}$ at low, the data output is valid until $\overline{RAS}$ goes high and returns to the high-impedance state within tOFF referenced to $\overline{RAS}$. With $\overline{CAS}$ being low at $\overline{RAS}$ high, the data output is valid until $\overline{CAS}$ goes high and returns to the high-impedance state within tOFF referenced to $\overline{CAS}$.

Hidden refresh

$\overline{RAS}$-only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at VIL of a previous memory read cycle.

Refresh cycle

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output signal during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

Nibble-mode cycle

Nibble-mode operation allows a very fast serial data streaming up to 4 bits by applying only one set of addresses for the first bit to be accessed as normal (tCAC). By holding $\overline{RAS}$ low, only $\overline{CAS}$ has to be cycled up and then down for reading or writing the next 3 bits at a high data rate with tNAC tCAC. After 4 bits have been accessed, the following bit will be the same as the first bit accessed. Address on pin 1 (row address A8 and column address A8) is used to select 1 of the 4 nibble bits for initial access. Toggling $\overline{CAS}$ causes row A8 and column A8 to be incremented by the internal shift register with A8 row being the least significant address, and allows access to the next nibble bit. In nibble mode, any combination of read, write, and read-modify-write operation is possible (e.g. first bit: read; second bit: write; third bit: read-modify-write, etc.).

Absolute Maximum Ratings *)

Operating Temperature Range	0 to + 70 °C
Storage Temperature Range	−65 to +150 °C
Voltages on Any Pin Relative to VSS	−1 to +7 V
Voltage on DI Relative to VSS	−1 to +11 V
Power Dissipation	1 W
Data Out Current (Short Circuit)	50 mA

D.C. Characteristics

TA = 0 to 70 °C, VSS = 0V, VCC = +5 V ±10%

Symbol	Parameter	Limit Values		Unit	Test condition
		Min.	Max.		
VIH	Input high voltage (all inputs)	2.4	VCC+1	V	1) 2)
VIL	Input low voltage (all inputs)	−1.0	0.8		
VOH	Output high voltage	2.4	–		–
VOL	Output low voltage		0.4		
ICC1	Average VCC supply current −12 tRC = 220 ns −15 tRC = 260 ns −20 tRC = 330 ns	–	 85 70 60	mA	 3)
ICC2	Standy VCC supply current		5		4)
ICC3	Average VCC supply current during $\overline{RAS}$-only refresh cycles −12 tRC = 220 ns −15 tRC = 260 ns −20 tRC = 330 ns		 65 55 45		 3)
ICC6	Average VCC supply current during nibble mode −12 tNC = 65 ns −15 tNC = 80 ns −20 tNC = 110 ns		 10 8 7		
II(L)	Input leakage current (any input)	–	10	µA	–
IO(L)	Output leakage current ($\overline{CAS}$ at logic 1, 0 ≤ Vout ≤ 5.5)				
VCC	VCC supply voltage	4.5	5.5	V	1)
VSS	VSS supply voltage	0	0		

Notes see page 5

Capacitance

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
CI1	Input capacitance (A0–A8)		6	pF	5)
CI2	Input capacitance ($\overline{RAS}$, DI)		7		
CI3	Input capacitance ($\overline{CAS}$, $\overline{WE}$)		8		
CO	Output capacitance (D_{OUT}, $\overline{CAS}$ = VIH to disable output)				

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1) All voltages referenced to VSS.

2) Overshooting and undershooting on input levels of 6.5 V or −2 V for a period of 30 ns max. will not influence function and reliability of the device.

3) ICC depends on frequency of operation. Maximum current is measured at the fastest cycle rate.

4) $\overline{RAS}$ and $\overline{CAS}$ are both at VIH.

5) Effective capacitance calculated from the equation $C = \frac{I \cdot \Delta t}{\Delta V}$ with $\Delta V = 3$ V or measured with Boonton meter.

A.C. Test Conditions

Input pulse levels		0 to 3.0 V
Input rise an fall times	5 ns between	0.8 and 2.4 V
Input timing reference levels		0.8 to 2.4 V
Output timing reference levels		0.4 to 2.4 V
Output load		equivalent to 2 standard TTL loads and 100 pF

A.C. Characteristics

TA = 0 to +70 °C; VCC = +5 V ±10% (unless otherwise specified; see notes 6, 7, 8)

Symbol	Parameter	Limit values						Unit
		HYB 41257-						
		-12		-15		-20		
		Min.	Max.	Min.	Max.	Min.	Max.	
tRC	Random read or write cycle time 9)	220	–	260	–	330	–	ns
tRWC	Read-modify-write cycle time 9)	265		310		390		
tRAC	Access time from $\overline{RAS}$ 10) 11)	–	120	–	150	–	200	
tCAC	Access time from $\overline{CAS}$ 10) 11) 12)		60		75		100	
tRAS	$\overline{RAS}$ pulse width	120	10^4	150	10^4	200	10^4	
tCAS	$\overline{CAS}$ pulse width	60	–	75	–	100	–	
tREF	Refresh period	–	4	–	4	–	4	ms
tRP	$\overline{RAS}$ precharge time	90	–	100	–	120	–	ns
tCRP	CAS to RAS precharge time	10		10		10		
tRCD	$\overline{RAS}$ to $\overline{CAS}$ delay time 13)	30	60	30	75	35	100	
tRSH	$\overline{RAS}$ hold time	60	–	75	–	100	–	ns
tCSH	$\overline{CAS}$ hold time	120		150		200		
tASR	Row address setup time	0		0		0		
tRAH	Row address hold time	20		20		25		
tASC	Column address setup time	0		0		0		
tCAH	Column address hold time	30		30		35		
tAR	Column address hold time referenced to $\overline{RAS}$ 14)	90		105		135		
tT	Transition time (rise and fall) 6)	3	50	3	50	3	50	
tRCS	Read command setup time	0	–	0	–	0		
tRCH	Read command hold time referenced to $\overline{CAS}$ 15)							
tRRH	Read command hold time referenced to $\overline{RAS}$ 15)	25		25		30		

Notes see page 8

Symbol	Parameter	Limit values						Unit
		HYB 41257-						
		-12		-15		-20		
		Min.	Max.	Min.	Max.	Min.	Max.	
tOFF	Output buffer turn-off delay 16)	0	30	0	40	0	50	ns
tWCS	Write command setup time 17)		–		–		–	
tWCH	Write command hold time	40		45		55		
tWCR	Write command hold time referenced to $\overline{RAS}$ 14)	100		120		155		
tWP	Write command pulse width	40		45		55		
tRWL	Write command to $\overline{RAS}$ lead time							
tCWL	Write command to $\overline{CAS}$ lead time							
tDS	Data in setup time 18)	0		0		0		
tDH	Data in hold time 18)	40	–	45	–	55	–	
tDHR	Data in hold time referenced to $\overline{RAS}$ 14)	100		120		155		
tCWD	$\overline{CAS}$ to $\overline{WE}$ delay 17)	60		75		100		
tRWD	$\overline{RAS}$ to $\overline{WE}$ delay 17)	120		150		200		
tRRW	RMW cycle $\overline{RAS}$ pulse width	165		200		260		
tCRW	RMW cycle $\overline{CAS}$ pulse width	105		125		160		
tNC	Nibble-mode cycle time 9)	65		80		110	–	
tNAC	Nibble-mode access time from $\overline{CAS}$ 10)	–	30	–	40	–	50	
tNAS	Nibble-mode setup time	30		40		50		
tNP	Nibble-mode precharge time	25		30				
tNRSH	Nibble-mode $\overline{RAS}$ hold time	30		40				
tNCWD	Nibble-mode $\overline{CAS}$ to $\overline{WE}$ delay		–		–		–	
tNCRW	Nibble-mode RMW $\overline{CAS}$ pulse width	65		85		105		
tNCWL	Nibble-mode $\overline{WE}$ to $\overline{CAS}$ lead time	30		40		50		
tNWRH	Nibble-mode write $\overline{RAS}$ hold time	45		55		75		
tNOFF	Nibble-mode output buffer turn-off delay 19)	0		0		0		
tNWP	Nibble-mode $\overline{WE}$ pulse width	30		40		50		
tNWCH	Nibble-mode $\overline{WE}$ command hold time							

Notes see page 8

Notes:

6) VIH and VIL are reference levels to measure timing of input signals. Also, transition times are measured between VIH and VIL.

7) An initial pause of 200 µs is required after powerup following by a minimum of eight initialization cycles prior to normal operation.

8) The time parameters specified here are valid for a transition time of tT = 5 ns for the input signals.

9) The specifications for tRC (min), tRWC (min), and nibble cycle time (tNC) are only used to indicate cycle time at which proper operation over full temperature range (0 °C ≤ TA ≤ 70 °C) is assured.

10) Measured with a load equivalent to two TTL loads and 100 pF.

11) Assumes that tRCD ≤ tRCD(max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.

12) Assumes that tRCD ≥ tRCD (max).

13) Operation within the tRCD (max) limit ensures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.

14) tRCD + tCAH ≥ tAR min, tRCD + tDH ≥ tDHR min, tRCD + tWCH ≥ tWCR min.

15) Either tRRH or tRCH must be satisfied for a read cycle.

16) tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. tOFF is referenced either to the $\overline{CAS}$ leading edge with $\overline{RAS}$ being high or to the $\overline{RAS}$ leading edge with $\overline{CAS}$ being high.

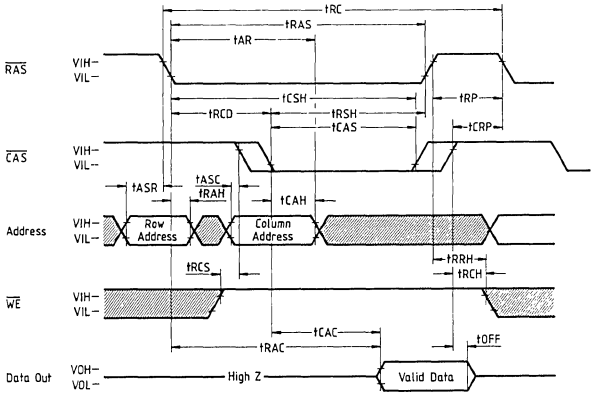
17) tWCS, tCWD and tRWC are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If tWCS ≥ tWCS(min), the cycle is an early write cycle and the Data Out will remain open circuit (high impedance) throughout the entire cycle; if tCWD ≥ tCWD (min) and tRWD ≥ tRWD (min) the cycle is a read-write cycle and the Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the Data Out (at access time) is indeterminate.

18) tDS and tDH are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.

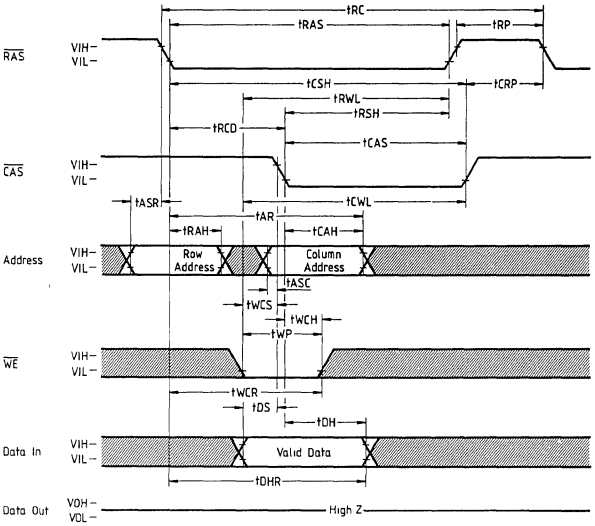
19) tNOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. tNOFF is referenced to the $\overline{CAS}$ falling edge of the next nibble cycle with $\overline{RAS}$ being low.

Waveforms

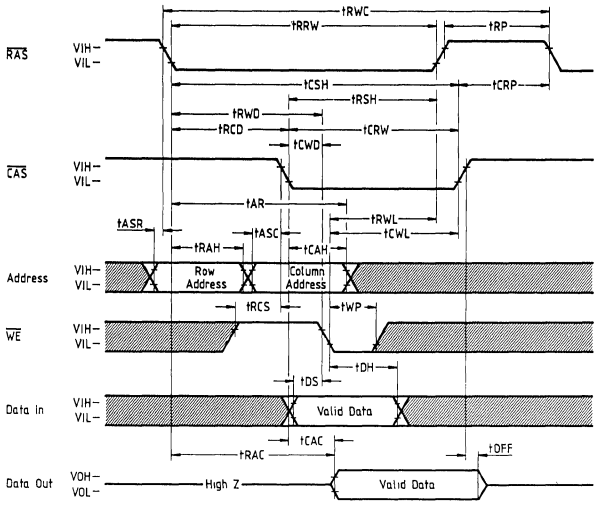
Read cycle



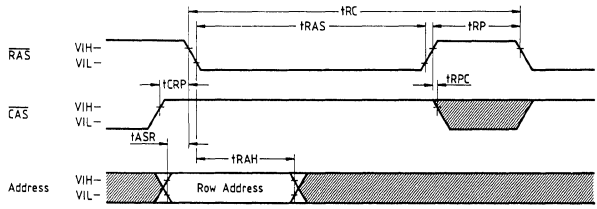
Write cycle (early write)



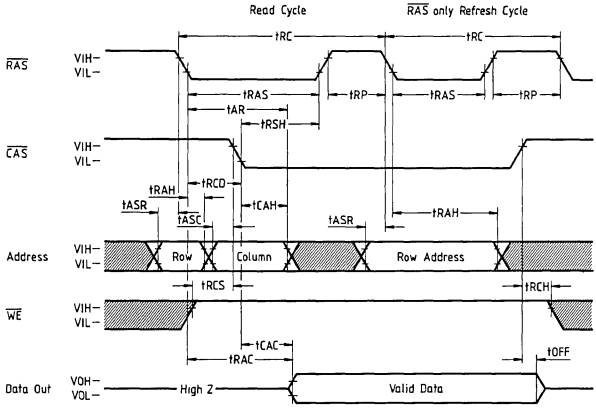
Read-modify-write or write cycle



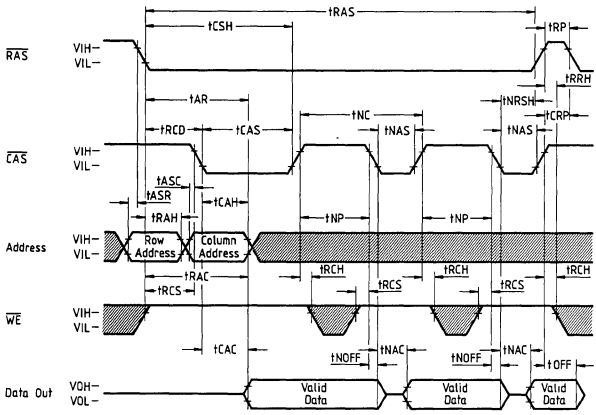
RAS-only refresh cycle
(DI and WE = don't care)



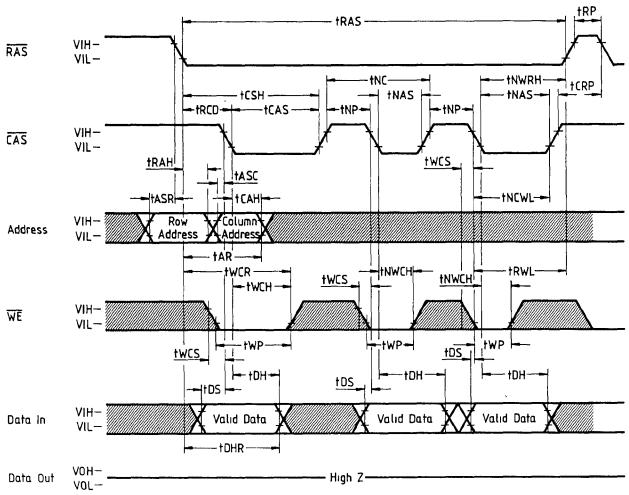
Hidden refresh cycle



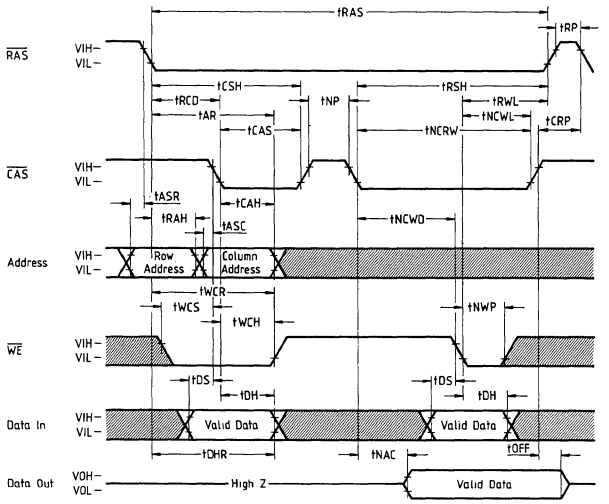
Nibble-mode read cycle



Nibble-mode write cycle (early write)



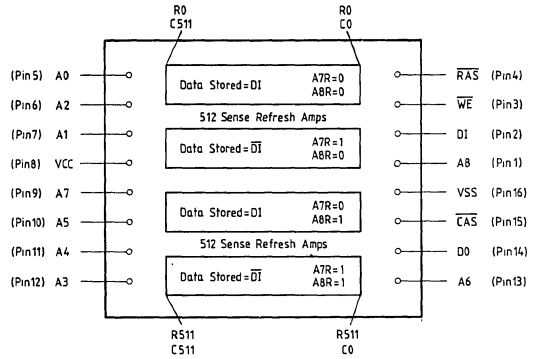
Nibble-mode read-modify-write



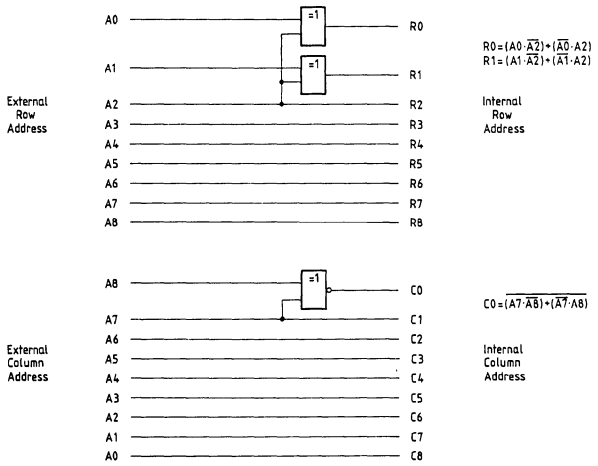
Address Decoder Scrambling (without redundancy)

The evaluation and incoming testing of RAMs normally requires a description of the internal address scrambling of the device in order to check for 'worst case' pattern.

Internal address scrambling



Address decoder scrambling



Note: The logic symbols are used solely to indicate the logic function.

Redundancy

Redundancy concept

The HYB 41257 takes advantage of the redundancy concept for increasing yield. This is done by providing the chip with a total of 8 spare rows and 4 spare column pairs. Two spare rows can be selected independently in each of four 64K cell arrays, and two spare column pairs can be selected independently in each of two 128K cell blocks. The spare lines can be selected by spare decoders which have to be programmed by laser technique during wafer probe.

Laser technology

For activation of redundant circuitry a laser pulse is used to open polycide links within the spare row and spare column decoders. The laser technique is used because it is mature and has proven reliable in a number of semiconductor applications including the implementation of redundant memory circuitry. Due to the fact, that the laser beam is very fine and can easily and accurately be positioned, and that it incorporates the energy for a controlled blow up of the polycide links, the laser technique is well suited for highly complex memory circuitry. All that results in a more efficient use of chip real estate.

Redundancy testability (roll-call mode)

With the redundancy concept two categories of devices, repaired and non-repaired ones, will be available. These two categories have to be separated easily and reliably by both, the manufacturer and the user (signature). When testing repaired device, the reconfigurated address scrambling which results from activating spare rows and columns has to be taken into account for efficient device testing (individual bit map recognition).
The HYB 41257 has the capability of performing these two novel functions. It is done with a simple electrical test at the beginning of the final test or incoming inspection of each device (roll-call mode). The roll-call mode for performing both signature and individual bit map recognition can be activated with DI at VIHR (10V ±10%).

Signature

With DI at VIHR and performing at least one $\overline{RAS}$-only cycle with a cycle time of tRCR on any address combination, in the case of non-repaired devices the Data Output is in the high-impedance state as in normal early write cycles. For repaired devices the Data Output will go to VOLR or VOHR after the access time tRACR.

Individual bit map recognition

If the test for signature has shown a repaired device, additional tests can be performed to recognize which addresses have been repaired and how they are replaced by spare lines. Row and column redundancy can be recognized independently.

Row redundancy

Row redundancy can be recognized with DI at VIHR and $\overline{CAS}$ at high, and $\overline{RAS}$-only cycles on all 512 row address combinations. The data output is low (VOLR) for non-repaired addresses, and is high (VOHR) for repaired addresses only. Within each 64K cell array, spare row 1 is always used if only one row is to be replaced. If two rows are to be replaced in an 64K cell array, spare row 2 is used to replace the defective row with the higher address.

Column redundancy

Column redundancy can be recognized with DI at VIHR, and early write cycles with tRCDR ≤ tRCD (min) on all 512 column address combinations.

A8 row must be used to distinguish between the two 128K cell blocks. The data output is low (VOLR) for non-repaired addresses, and high (VOHR) for repaired addresses. Within each 128K cell block, spare column pair 1 is always used if only one column is to be replaced. Otherwise, spare column pair 2 is used to replace the defective column with the higher address.

Recommended operating conditions

Roll-call mode

DC operating conditions and characteristics (Full operating voltage and temperature range unless otherwise specified).

Symbol	Parameter	Limit values			Unit
		Min.	Typ.	Max.	
VCC	Supply voltage HYB 41257-12, -15, -20 1)	4.75	5.0	5.25	V
VSS	1)	0	0	0	
VIH	Logic 1 voltage: All inputs (except DI)	2.4	–	VCC+1	
VIHR	Logic 1 voltage: DI 1) 2)	9.0	10	11	
VIL	Logic 0 voltage: All inputs 1)	−1.0	–	0.8	
VOHR	Output logic 1 voltage Iout = −5mA 1)	2.0		–	
VOLR	Output logic 0 voltage Iout = −4.2 mA 1)	–		0.4	

A.C. operating conditions and characteristics

(Full operating voltage and temperature range unless otherwise specified.)

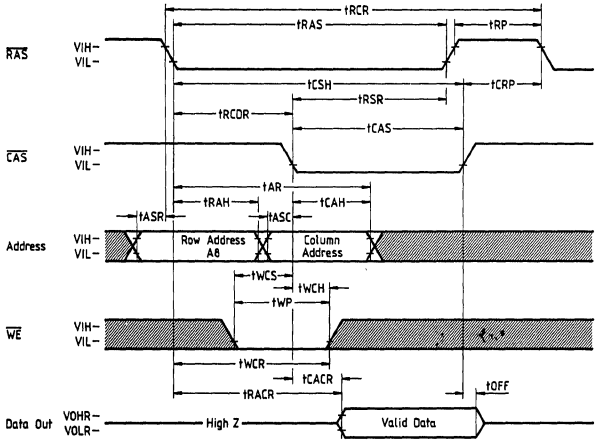
Symbol	Parameter	Limit values						Unit
		HYB 41257-						
		−12		−15		−20		
		Min.	Max.	Min.	Max	Min.	Max.	
tRCR	Roll-call cycle time	330	–	390	–	490	–	ns
tRCDR	Roll-call $\overline{RAS}$ to $\overline{CAS}$ delay	–	30	–	30	–	35	
tRACR	Roll-call $\overline{RAS}$ access time	180	–	225	–	300	–	
tCARC	Roll-call $\overline{CAS}$ access time	90		115		150		

1) All voltages referenced to VSS.

2) VIHR at DI must only be used for the roll-call mode test and not for normal memory tests or applications. To avoid device damage, VIHR is to be applied after the initialization conditions (initial pause of 200 µs and 8 cycles) have been satisfied, and must never exceed 11V.

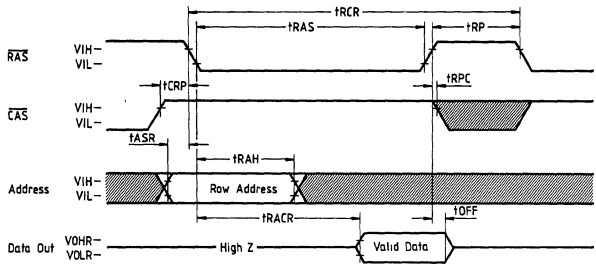
Column Redundancy

Early CAS – early write cycle
(DI at VIHR, *t*RCD = tRCD (min), row addresses A0 to A7 = don't care)

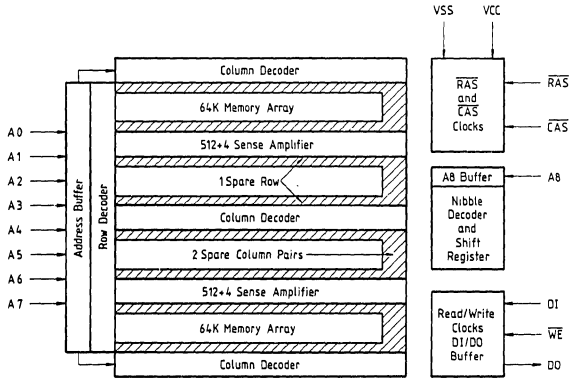


Row Redundancy and Signature

RAS-only cycle
(DI at VIHR, WE = don't care)



Siemens 256K DRAM Chip Topology



Telecom Components

PEB 2030
Frame Aligner Module

Preliminary data

Features

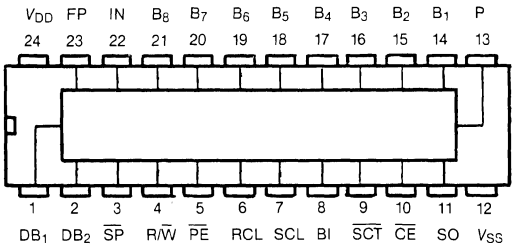
- Detection of frame alignment signals for PCM 30 highways in accordance with CCITT recommendation G 732
- Delay compensation and clock alignment between transmission line and exchange
- Compensation of phase jitter up to 60μs
- Detection and initiation of route alarms (AIS, service word)
- Indication of loss of frame alignment
- Slip detection
- Error simulation for test purposes
- Digital interface TTL-compatible

Applications

The PEB 2030 frame aligner module is used for interfacing PCM 30 routes with PCM switching networks. Its main applications are as follows:

- in multiplex units for PCM transmission routes
- in concentrators and subscriber multiplexers at one end of PCM routes
- as an interface between PCM routes and public and private PCM switches (DIU)
- for delay compensation between switching stages (e.g., Swiss Post Office IFS design concept)

Pin configuration, top view



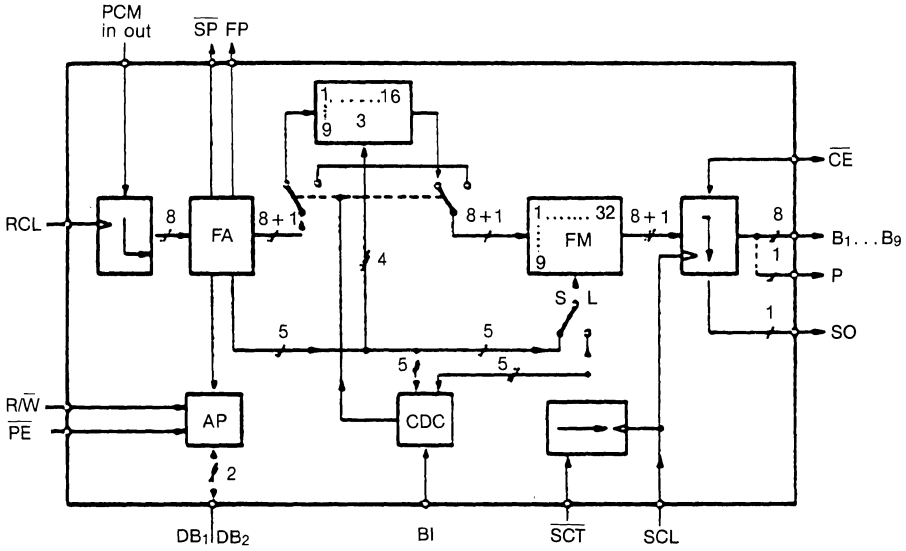
DB_1, DB_2	Data interfaces
$\overline{SP}$	Synchronous pulse
R / $\overline{W}$	Direction of data transfer
$\overline{PE}$	Alarm port enable
RCL	Route clock
SCL	Station clock
BI	Buffer inactive
$\overline{SCT}$	Station counter trigger pulse
$\overline{CE}$	Chip enable
SO	Serial output
FP	Fault pulse
IN	PCM input
B_1 ... B_8	Parallel outputs
P	Parity bit
V_{SS}	Ground (0 V)
V_{DD}	Supply voltage (+5 V)

General description

The Siemens frame aligner module PEB 2030 is a monolithic NMOS circuit. Its main application is the detection of frame alignment signals of PCM 30 routes according to CCITT recommendation G 732 and the clock adjustment with delay compensation between PCM routes and PCM switches.

An incorporated buffer enables the PEB 2030 to compensate phase jitter up to 60μs.
Route alarms can be challenged by a bidirectional data interface.

Block diagram



FA Frame alignment
AP Alarm port
B Buffer
COC Coincidence circuit
FM Frame memory

Description of function

The PEB 2030 module is fabricated using the n-channel depletion technique.
The module, connected to a PCM 30 line, and the associated input clock (route clock RCl), are synchronized with the PCM frame in accordance with CCITT recommendation G 732. In the stable condition the module supplies 488 ns synchronous pulses ($\overline{SP}$) at a bit rate of 4 kbit/s which identify the beginning of the PCM frames containing the bunched frame alignment signal (FAS). During the synchronizing phase and in the event of frame alignment being lost, the synchronizing pulses are suppressed and a 2μs fault pulse FP is delivered every 250μs. When a synchronized stage exists, such a fault pulse appears only if an FAS is not recognized.

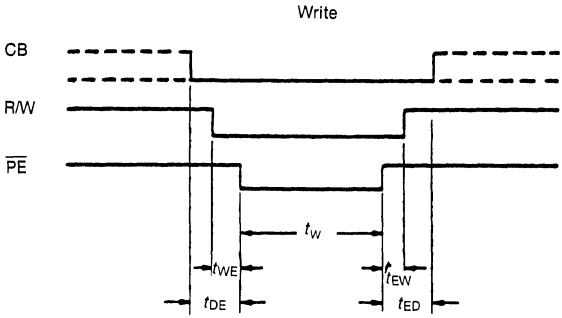
On the output side the PCM information can be read out in serial and in parallel form. For this purpose, a reading clock (SCl) and a 488 ns reading synchronizing pulse ($\overline{SCT}$) must be applied at 250μs intervals to fix the beginning of the frame. The module supplies a parity check bit (even parity) to each PCM word via a tri-state output which is activated by a chip enable ($\overline{CE}$) in the same way as the tri-state outputs for the parallel information.

An alarm flip-flop (FA Alarm) in the module is set in the event of frame alignment loss, route timing loss or loss of the $\overline{CE}$ or $\overline{SCT}$ signals. The alarm bit is recorded in another flip-flop in the service word (bit 3), whereas a third flip-flop stage is set when logic "1" signals are received by the PCM route for the duration of two frames (Alarm Indication Signal AIS). A further flip-flop is set when a slip of the frame occurs. The alarms are polled via a bidirectional data interface. The alarm circuits can be triggered and reset for test purposes via the data interface.

Pin description

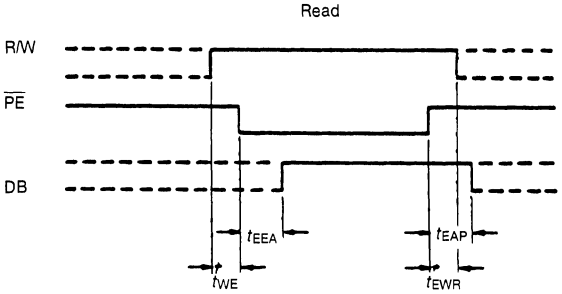
Symbol	Function	Description
1. Supply		
V_{DD}	+5V ± 5%	Power consumption 300 mW
V_{SS}	0V	
2. PCM interfaces		
IN	PCM input	Information bit from one negative RC edge to the next.
RCL	2.048 MHz ± 50 ppm	Route clock
$B_1 \ldots B_8$	256 kbit/s	Parallel PCM output information. B_1 = most significant inf. bit
P	256 kbit/s	Parity bit (even parity)
SO	2.048 Mbit	Serial PCM output. Bit sequence with decreasing significance.
SCL	2.048 MHz	Station clock. Information bits from one neg. SCI edge to the next.
3. Control signals		
$\overline{SCT}$	4 kbit/s width 488 ns	From one neg. SCI edge to the next. Frame begins from pos. $\overline{SCT}$ edge.
$\overline{SP}$	4 kbit/s, width 488 ns	From one neg. RCI edge to the next. Frame begins with FAS from pos. $\overline{SP}$ edge.
BI	Continuous signal	B1 = 1 or not connected: Buffer inactive.
FP	Width: 4 x 488 ns = 1.95μs	Fault pulse delivered for every undetected FAS or every 250μs in the event of frame alignment loss.
$\overline{CE}$	256 kbit, width 488 ns or continuous level	Chip enable controls outputs B_1 to B_8, P low-impedance. The $\overline{CE}$ must be active during the $\overline{SCT}$, so that the $\overline{SCT}$ supervision by station counter is not impaired.

4. Data interface



DB input timing (Write)

$t_W > 1\ \mu s$
$t_{WE} > 100$ ns
$t_{DE} > 100$ ns
$t_{EW} > 50$ ns
$t_{ED} > 150$ ns



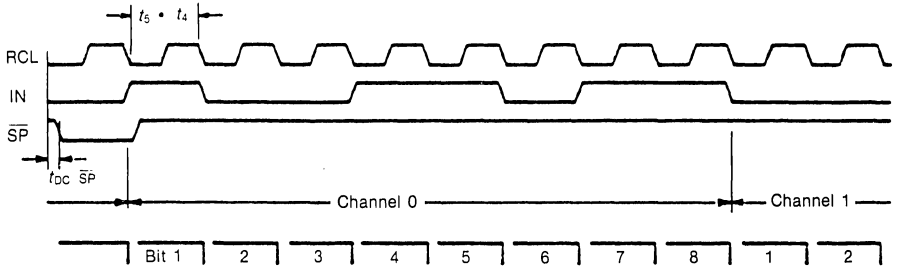
DB output timing (Read)

$t_{EWR} > 100$ ns
$0.8 < t_{EAA} < 1.2\ \mu s$ $C_L = 300pF$
$t_{EAP} > 160$ ns
$t_{WE} > 100$ ns

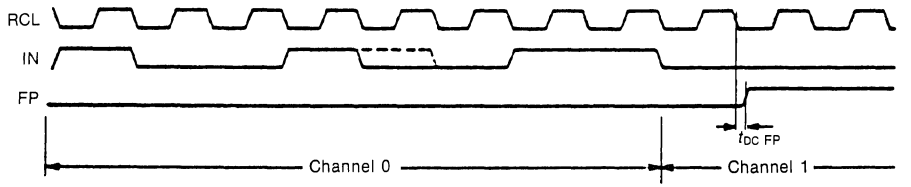
Data transfer direction
R / $\overline{W}$ = 1 read alarm port
R / $\overline{W}$ = 0 write alarm port
Alarm port enable
bidirectional data interface for command acceptance or alarm signalling:

DB_2	DB_1
0	0 Command : poll FA alarm, AIS alarm
0	1 Command : poll B_3 of the service word, Slip alarm
1	0 Command : reset alarm flip-flop
1	1 Command : failure simulation
AIS alarm Slip alarm	FA alarm B_3 alarm Alarms are signaled as log. '1'

Pulse diagram

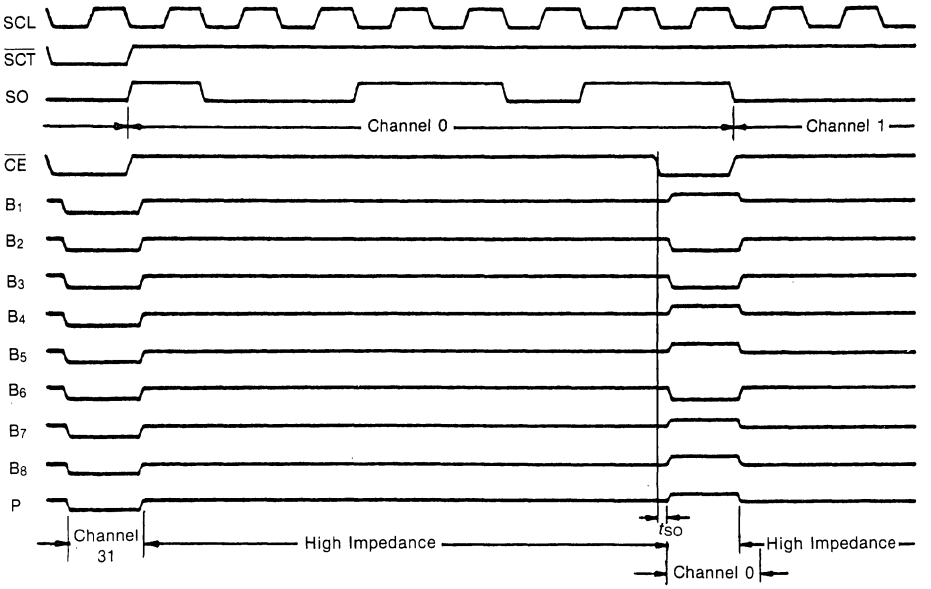


Delivery of synchronous pulse $\overline{SP}$ in synchronized state

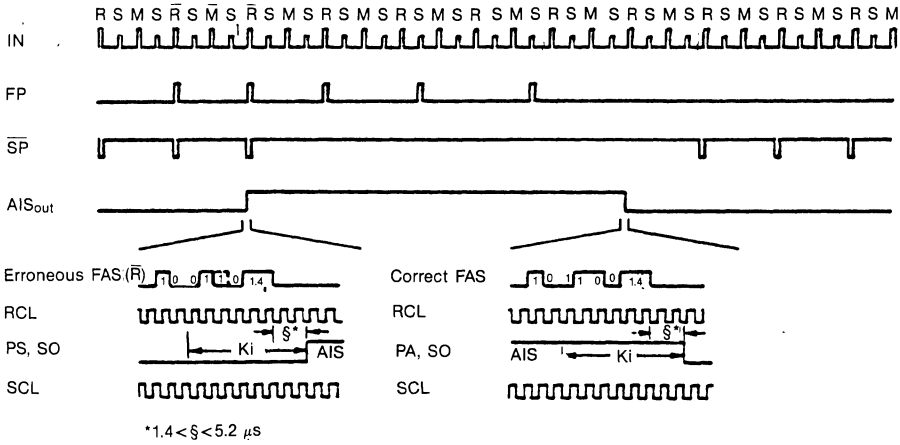


Delivery of fault pulse FP in the event of erroneous frame alignment signal

Pulse diagram



Output signals (B_1 to B_8,P) as functions of the station trigger pulse $\overline{SCT}$ and chip enable $\overline{CE}$



Loss of frame alignment due to bit falsification on the PCM route

R Frame alignment signal (FAS)
M Service word
S Simulated FAS (Random FAS)
$\overline{R}$ Erroneous FAS
$\overline{M}$ Erroneous service word

Absolute maximum ratings[1]		Min	Max	Unit
Operating temperature	T_{amb}	0	70	°C
Storage temperature	T_{stg}	-55	125	°C
Total power consumption	P_{tot}		400	mW
Input voltage	V_I	-0.3	7	V
Supply voltage	V_{DD}	-0.3	7	V

Electrical characteristics (T_{amb} = 25°C)		Min	Typ.	Max	Unit
Supply voltage	V_{DD}	4.75	5	5.25	V
Supply current	I_S		50	70	mA
Input current	I_{IL}	50		150	µA
H input voltage	V_{IH}	2.4			V
L input voltage	V_{IL}			0.7	V
L output voltage	V_{QL}			0.4	V
H output voltage	V_{QH}	2.7			V
H output current (FP,SQ,SP,B_i,P)	I_{QH}			-0.02	mA
L output current (FP,SQ,SP,B_i,P)	I_{QL}			0.46	mA
H output current (DB_i)	I_{QH}			-0.04	mA
L output current (DB_i)	I_{QL}			0.9	mA
Timing specification					
Input H-L transfer time	t_{HL}			20	ns
Input L-H transfer time	t_{LH}			20	ns
Clock frequency (pulse-pause ratio 1:1)	f_{CL}	0.2	2.048	2.1	MHz
$t_{WH}:t_{WL}$		1			
Set up time	t_S	150			ns
Hold time	t_H	40			ns

Switching times (V_{DD} = 5V, T_{amb} = 25°C)

from (input)	to (output)		Test conditions	Min	Typ.	Max	Unit
$\overline{CE}$	$B_1 \ldots B_8$,P	t_{DQ}	50 pF, 10 kΩ			200	ns
SCL	DB_1,DB_2	t_{DQ}	50 pF, 5 kΩ			350	ns
RCL	FP,SP	t_{DQ}	15 pF, 10 kΩ			200	ns
SCL	SQ	t_{DQ}	15 pF, 10 kΩ			200	ns

[1] Stresses above those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicatd in the operational section of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The information describes the type of component
and shall not be considered as assured characteristics.

PEB 2040
Memory Time Switch

Preliminary data **MOS circuit**

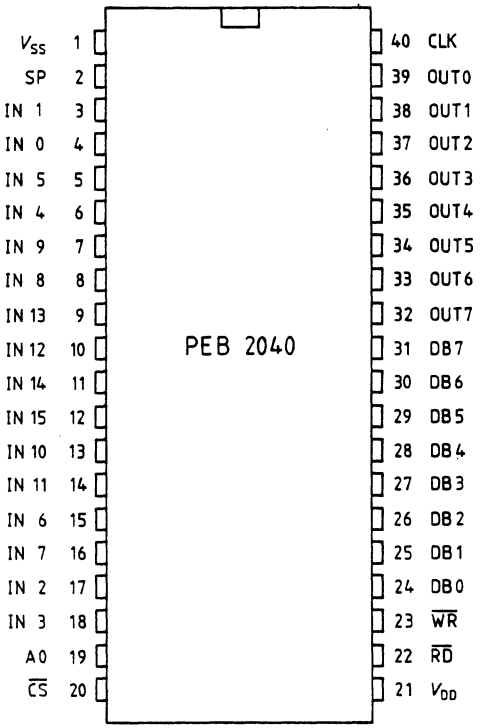
Features

- Time/space switch for 2.048 MHz and 8.192 MHz PCM systems
- Different kinds of operation modes (2 Mbit/s, 8 Mbit/s or mixed mode)
- 16 input PCM lines and speech memory for all 512 subscriber on chip
- Connection memory for 256 channels of 8 output lines on chip
- Non blocking time switch with 16/16 PCM lines can be built with two devices
- µP-interface for writing and reading the connection memory
- Delay between input and output lines selectable
- Tristate for further expansion or hot standby
- Advanced NMOS technology
- Single +5 V power supply

Applications

- All types of switching systems
- Complete switch in PCM PABX for up to 512 subscriber with only two devices
- Concentrator function
- Frequency-transforming interface between 2 MHz and 8 MHz PCM systems
- 16/16 space switch for 8 MHz PCM systems

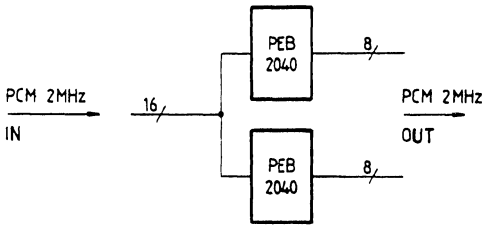
Pin configuration



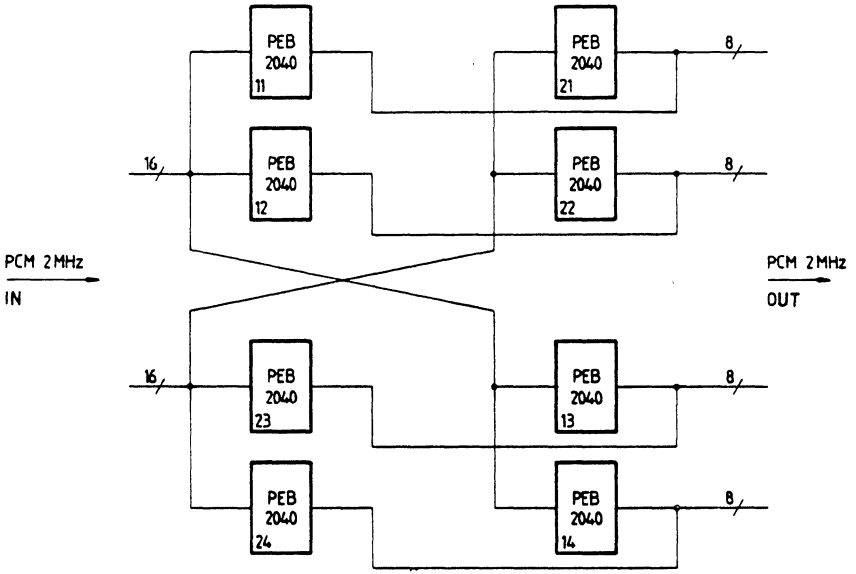
General description

The SIEMENS memory time switch PEB 2040 is a monolithic NMOS circuit with speech and connection memory on chip. It connects any of 512 incoming PCM channels to any of 256 outgoing PCM channels. Two chips give a non blocking 512 channel switch. Block diagrams of 2 PCM systems using the PEB 2040 are shown in **figure 1**. In- and outputs are TTL compatible.

Figure 1
Block diagram of two PCM switch configurations with PEB 2040



Memory time switch 16/16 for a non blocking 512 channel switch.



Memory time switch 32/32 for a non blocking 1022 channel switch using the tristate function.

Functional description of MTS 16/8

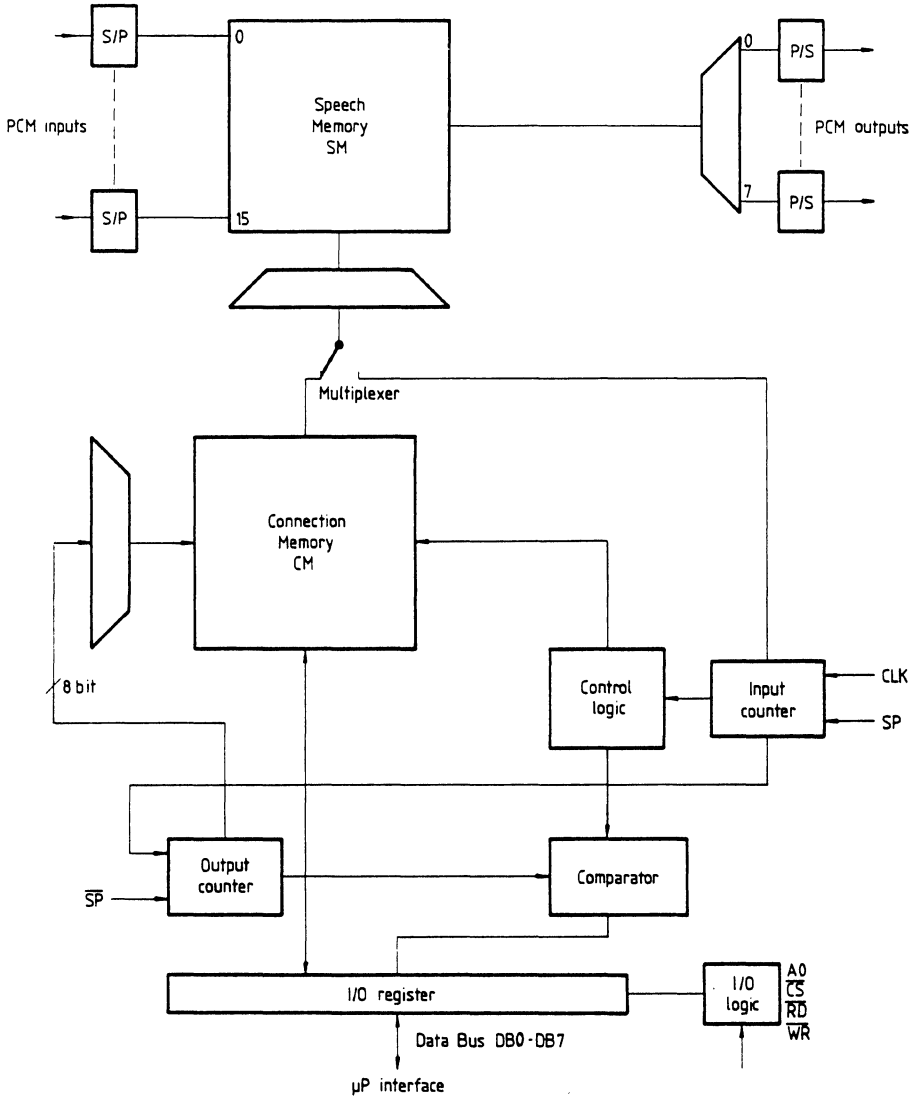
The PEB 2040 is a memory time switch module which has the ability to connect any of the 512 PCM channels of 16 incoming PCM lines to any of the 256 PCM channels of 8 output lines.

A block diagram of the main components is shown in **figure 2.**

The PCM information of a complete frame is stored in the 4K speech memory SM. That means all of the 512 words with 8 bits are written into a fixed position of the SM. This is controlled by the input counter every 125 µs. The words are read with a random access with an address that is stored in a connection memory CM for each of the 256 output channels. The access to the CM is controlled by the output counter.

To realize a connection the SM address and the CM address must be written into the PEB 2040 via a µP interface. The SM address contains the channel and line number of the incoming PCM words. The CM address consists of the channel and line number of the output words.

Figure 2
Block diagram



Operation modes

The PEB 2040 can be connected to 2.048 Mbit/s and 8.192 Mbit/s PCM lines. The operation mode is selected by the mode bits, where MIØ and MI1 defines the bit rate of the input lines and independently MOØ and MO1 that of the output lines.

The corresponding input and output addresses are given in **table 1.** The mode MIØ = MI1 = 1 is only for space switch application.

Table 1
Input configuration

PIN Nr.	MIØ=Ø, MI1=Ø	MIØ=1, MI1=Ø	MIØ=Ø, MI1=1	MIØ=1, MI1=1
	16x2 Mbit/s	4x8 Mbit/s	8x2+2x8 Mbit/s	16x8 Mbit/s
3	IN 1			1
4	IN Ø		IN Ø	Ø
5	IN 5			5
6	IN 4		IN 4	4
7	IN 9			9
8	IN 8		IN 8	8
9	IN 13	IN 1	IN 1	13
1Ø	IN 12	IN Ø	IN 12	12
11	IN 14	IN 2	IN 14	14
12	IN 15	IN 3	IN 3	15
13	IN 1Ø		IN 1Ø	1Ø
14	IN 11			11
15	IN 6		IN 6	6
16	IN 7			7
17	IN 2		IN 2	2
18	IN 3			3

Output configuration

PIN Nr.	MOØ =Ø, MO1=Ø	MOØ=1, MO1=Ø	MOØ=Ø, MO1=1
	8x2 Mbit/s	2x8 Mbit/s	4x2/1x8 Mbit/s
32	OUT 7		OUT 7
33	OUT 6		
34	OUT 5		OUT 5
35	OUT 4		
36	OUT 3		OUT 3
37	OUT 2		
38	OUT 1	OUT 1	OUT 1
39	OUT Ø	OUT Ø	OUT Ø

Pin description

Pin-No.	Name	Function
1	V_{SS}	Ground (OV)
2	SP	Synchronous pulse (8 kHz); rising edge for input counter falling edge for output counter; difference between rising and falling edge should be $\Delta = (2 + N \times 4)\ t_{CLK}$ ($N = \emptyset - 255$) rising edge synchronous with the incoming frames; output frame starts 2 clock pulses before the falling edge.
3	IN 1	PCM input port 1
4	IN $\emptyset$	PCM input port $\emptyset$
5	IN 5	PCM input port 5
6	IN 4	PCM input port 4
7	IN 9	PCM input port 9
8	IN 8	PCM input port 8
9	IN 13	PCM input port 13
1$\emptyset$	IN 12	PCM input port 12
11	IN 14	PCM input port 14
12	IN 15	PCM input port 15
13	IN 1$\emptyset$	PCM input port 1$\emptyset$
14	In 11	PCM input port 11
15	IN 6	PCM input port 6
16	IN 7	PCM input port 7
17	IN 2	PCM input port 2
18	IN 3	PCM input port 3
19	A $\emptyset$ *	Address $\emptyset$, for separating different modes of the control words
2$\emptyset$	$\overline{CS}$*	Chip select
21	V_{DD}	Supply voltage + 5 V ± 5%
22	$\overline{RD}$*	Read pulse
23	$\overline{WR}$*	Write pulse
24	DB $\emptyset$*	DATA Bus $\emptyset$
25	DB 1*	DATA Bus 1
26	DB 2*	DATA Bus 2
27	DB 3*	DATA Bus 3
28	DB 4*	DATA Bus 4
29	DB 5*	DATA Bus 5
3$\emptyset$	DB 6*	DATA Bus 6
31	DB 7*	DATA Bus 7
32	OUT 7	PCM output port 7
33	OUT 6	PCM output port 6
34	OUT 5	PCM output port 5
35	OUT 4	PCM output port 4
36	OUT 3	PCM output port 3
37	OUT 2	PCM output port 2
38	OUT 1	PCM output port 1
39	OUT $\emptyset$	PCM output port $\emptyset$
4$\emptyset$	CLK	Clock pulse 8.192 MHz, duty cycle 50%

bidirectional

* µP-controlled interface

PCM-interface

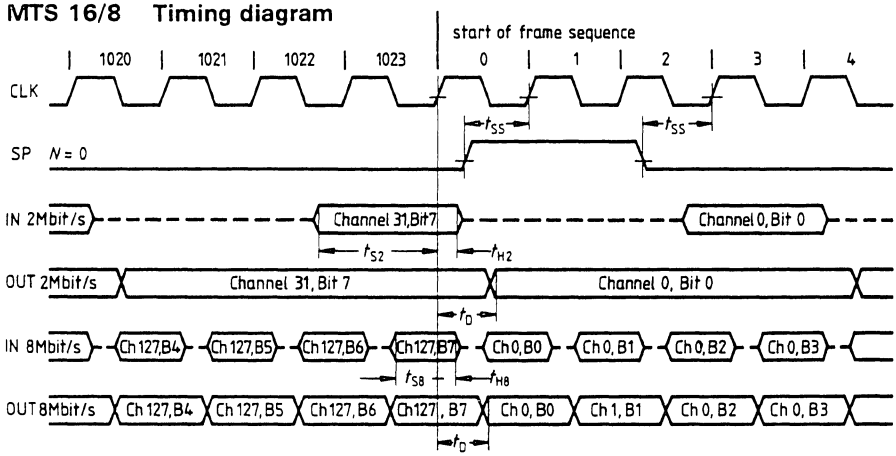
Control signals:
Clock: CLK f_{CLK} = 8.192 MHz 50% duty cycle, t_r, $t_f \leqq 10$ ns
synchronous pulse: SP f_{CLK} = 8.000 kHz defines the PCM frame with 1024 clock pulses
t_r, $t_f \leqq 10$ ns

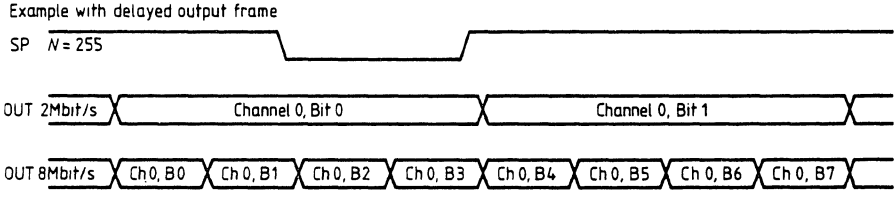
PCM input: IN Ø – IN 15
for 2 or 8 Mbit/s organized as 32 words of 8 bits or 128 words of 8 bit within a frame. The frame for all input lines starts with the rising edge of the SP signal.

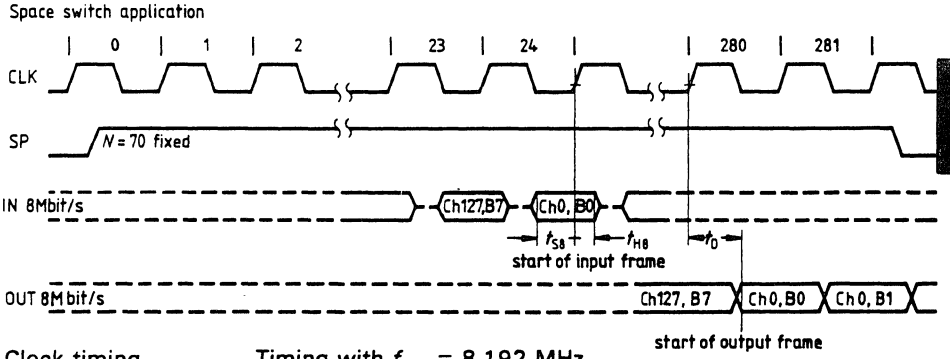
PCM output: OUT Ø – OUT 7
for 2 or 8 Mbit/s. The frame for all output lines is controlled by the falling edge of the SP signal. The difference between the rising and the falling edge of the SP signal should be $\lrcorner = (2 + N \times 4)\ t_{CLK}$, $Ø \leq N \leq 255$ (fixed at space switch application: $\lrcorner = (2 + 70 \times 4)\ t_{CLK} = 282\ t_{CLK}$, $N = 70$). N defines the delay of the output frame counted in 2 MHz bit steps relative to the input frame, as shown in the timing diagram.

The outputs have tristate capability.

MTS 16/8 Timing diagram







Clock timing
f_{CLK} = 8.192 MHz
t_{CLK} = 122 ns
50% duty cycle

Timing with f_{CLK} = 8.192 MHz

	min	max	
t_{SS}	70	170	ns
t_{S2}	180		ns
t_{H2}	0		ns
t_{S8}	60		ns
t_{H8}	0		ns
t_D		50	ns

C_L = 200 pF

µP Interface DBØ – DB7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, AØ

Commands for access to the connection memory, selected by AØ = 1.

All commands have a three byte strukture and must be executed completly.

DB7							DBØ	
X	X	K1	KØ	X	X	X	S8	Key word
S7	S6	S5	S4	S3	S2	S1	SØ	Speech Memory Address
C7	C6	C5	C4	C3	C2	C1	CØ	Connection Memory Address

Keyword K1	Keyword KØ	
1	Ø	Write Connection Memory
Ø	1	Write Connection Memory, with checkbytes
Ø	Ø	Read Connection Memory

S8	S7	S6	S5	S4	S3	S2	S1	SØ

Speech memory address, stored in the connection memory

C7	C6	C5	C4	C3	C2	C1	CØ

Connection memory address

The speech memory address contains the channel and line number of the incoming PCM words. The connection memory address consists of the channel and line number of the output words with the following coordination.

2 Mbit/s input lines	bit Ø–3 line number bit 4–8 channel number
8 Mbit/s input lines	bit Ø–1 line number bit 2–8 channel number
2 Mbit/s output lines	bit Ø–2 line number bit 3–7 channel number
8 Mbit/s output lines	bit Ø line number bit 1–7 channel number

Example

Channel 7 of the coming 2 Mbit/s line No. 9 shall be switched to channel 126 of the output line No. 1 of an 8 Mbit/s system without checkbyte:

Byte			
	Ø	20 H	(ØØ1ØØØØØ)
	1	79 H	(Ø1111ØØ1)
	2	FD H	(111111Ø1)

(Ø Ø 1 Ø Ø Ø Ø Ø) (Ø 1 1 1 1 Ø Ø 1) (1 1 1 1 1 1 Ø 1)

Key Word write — Channel 7 — Line 9 — Channel 126 — Line 1

For space switch application with MI Ø = 1, MI 1 = 1; MO Ø = 1, MO 1 = Ø

8 Mbit/s input lines	bit Ø – 3 line number bit 4 – 8 the lower 5 bits of the channel number
8 Mbit/s output lines	bit Ø line number bit 1 – 7 channel number

The difference between the rising and the falling edge of the SP is fixed:
$N = 7Ø$, $J = (2 + 70 \times 4)\ t_{CLK} = 282\ t_{CLK}$

The selection of 128 input channels is possible by writing the connection memory (CM) as shown below.

In CM-address ØØ – 3F → S8 – S4 (SM-adr.) means ch. Ø – ch. 31
In CM-address 4Ø – 7F → S8 – S4 (SM-adr.) means ch. 32 – ch. 63
In CM-address 8Ø – BF → S8 – S4 (SM-adr.) means ch. 64 – ch. 95
In CM-address CØ – FF → S8 – S4 (SM-adr.) means ch. 96 – ch. 127

3 examples:

	C7 CØ	
CM-address = 3F	ØØ111111	output line 1, ch. 31
SM-address = 1FA	111111Ø1Ø	input line 1Ø, ch. 31
	S8 SØ	
	C7 CØ	
CM-address = 7F	Ø1111111	output line 1, ch. 63
SM-address = 1FA	111111Ø1Ø.	input line 1Ø, ch. 63
	S8 SØ	
	C7 CØ	
CM-address = CØ	11ØØØØØØ	output line Ø, ch. 96
SM-address = ØØ8	ØØØØØ1ØØØ	input line 8, ch. 96
	S8 SØ	

Write connection Memory

X	X	1	Ø	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	SØ
C7	C6	C5	C4	C3	C2	C1	CØ

AØ=1, $\overline{WR}$=Ø, $\overline{CS}$=Ø

Stores S8 – SØ into the Connection Memory addressed with C7 – CØ.

Write Connection Memory with check bytes desired

X	X	Ø	1	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	SØ
C7	C6	C5	C4	C3	C2	C1	CØ

AØ=1, $\overline{WR}$=Ø, $\overline{CS}$=Ø

Stores S8 – SØ into the Connection Memory addressed with C7 – CØ.

X	X	Ø	1	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	SØ
C7	C6	C5	C4	C3	C2	C1	CØ

AØ=1, $\overline{RD}$=Ø, $\overline{CS}$=Ø

S8 – SØ have been overwritten by the Connection Memory in the next frame after writing the Connection Memory.

Read Connection Memory

X	X	Ø	Ø	X	X	X	X
X	X	X	X	X	X	X	X
C7	C6	C5	C4	C3	C2	C1	CØ

AØ=1, $\overline{WR}$=Ø, $\overline{CS}$=Ø

overwrites S8 – SØ with the Connection Memory address C7 – CØ, and can be read with the following sequence.

X	X	Ø	Ø	X	X	X	S8
S7	S6	S5	S4	S3	S2	S1	SØ
C7	C6	C5	C4	C3	C2	C1	CØ

AØ=1, $\overline{RD}$=Ø, $\overline{CS}$=Ø

Mode/Status selected AØ=Ø
Status AØ=Ø, $\overline{RD}$=Ø, ($\overline{WR}$=1), $\overline{CS}$=Ø

DB7							DBØ
B	Z	X	RY	Ø	Ø	Ø	Ø

B = 1 Chip busy during command execution
Z = 1 Incomplete command instruction
RY = 1 Mode register blocked (after "Power-on")

Power on tristate

SB is set by "Power-on" or by "Write Moderegister".
SB is reset by "Write Moderegister".
"Write Moderegister" is blocked at most seven frames after "Power-on".
During that time RY in the status register is set to "1"
SP and CLK should be applied immediately after "Power-on"

Mode AØ = Ø, $\overline{WR}$ = Ø, ($\overline{RD}$ = 1), $\overline{CS}$ = Ø

DB7							DBØ
R	TE	Ø	SB	MI1	MIØ	MO1	MOØ

R = Reset — R = Ø Reset
TE = Tristate enable — TE = Ø Mode without tristate function; TE = 1 Tristate dependent from code
SB = Standby — SB = 1 Tristade independent from code

MI1	MIØ	Input operation mode
Ø	Ø	16x2 Mbit/s
Ø	1	4x8 Mbit/s
1	Ø	2x8+8x2 Mbit/s

MO1	MOØ	Output operation mode
Ø	Ø	8x2 Mbit/s
Ø	1	2x8 Mbit/s
1	Ø	1x8/4x2 Mbit/s

1	1	16x8 Mbit/s

for space switch application only

Reset

DB7 = R

The PEB 2040 can be initialized by a mode byte with R=Ø. This causes the complete connection memory to be overwritten with zeros. During this time the busy bit is set.

Tristate

DB6 = TE, DB4 = SB

The PCM outputs of the PEB 2040 have tristate capability.

1. SB = 1 is a standby mode. All outputs are tristate. The connection memory works in the normal mode.

   The chip can be activated immediately by setting SB = Ø.
2. TE = 1, (SB = Ø): The output channels are tristate, if the speech memory address stored in the connection memory is S8 – SØ = Ø. This means that channel Ø of line Ø is not available for any output.
3. TE = Ø, (SB = Ø): Channel Ø of line Ø is available, but tristate is not possible.

Operation Mode (Input/Output bit rate)

DBØ=MOØ, DB1=MO1, DB2=MIØ, DB3=MI1

The operation mode is selected by the mode bits, where MIØ and MI1 defines the bit rate of the input lines and independently MOØ and MO1 that of the output lines.

The corresponding input and output addresses are given in **table 1**.

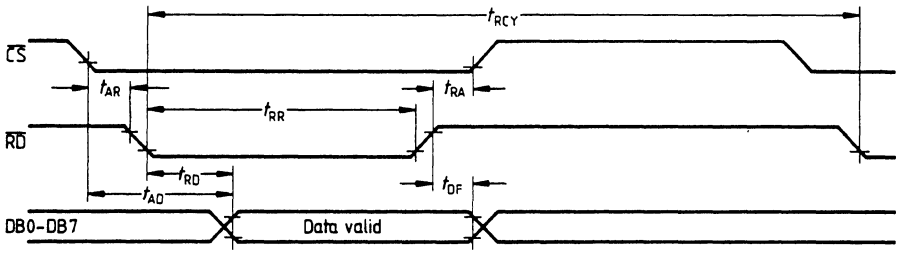
Example

DB7							DBØ
1	1	Ø	Ø	Ø	Ø	Ø	Ø

PCM mode: 16x2 Mbit/s input
PCM mode: 8x2 Mbit/s output
with tristate

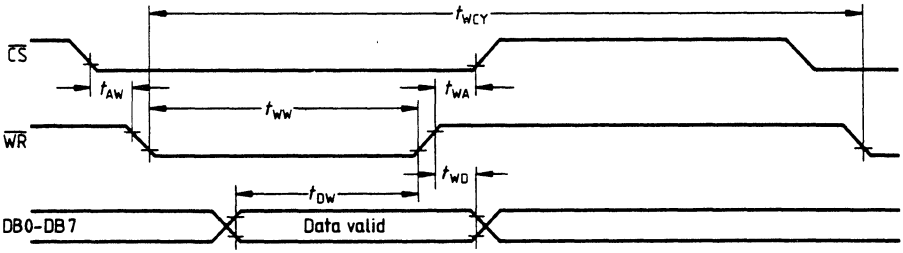
Timing of µP interface

Read operation



		Min.	Max.	Unit
Adr. stable before $\overline{RD}$	t_{AR}	0		ns
Adr. hold after $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ width	t_{RR}	180		ns
$\overline{RD}$ to data valid	t_{RD}		90	ns
Adr. stable to data valid	t_{AD}		100	ns
Data float after $\overline{RD}$	t_{DF}	10	100	ns
$\overline{RD}$-cycle time	t_{RCY}	500		ns

Write operation



		Min.	Max.	Unit
Adr. stable before $\overline{WR}$	t_{AW}	0		ns
Adr. hold time	t_{WA}	0		ns
$\overline{WR}$ width	t_{WW}	190		ns
Data set up time	t_{DW}	130		ns
Data hold time	t_{WD}	0		ns
$\overline{WR}$ cycle time	t_{WCY}	500		ns

The "busy time" during which a command or reset instruction is executed has to be programmed with its maximum length or must be controlled via the busy bit of the status register.

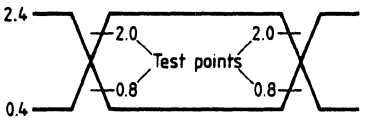
Busy time	Average	Max.	Unit
Reset	188	250	µs
Read connection memory	63	125	µs
Write connection memory	63	125	µs
Write connection memory with check bytes desired	188	250	µs

Maximum ratings		Min.	Typ	Max.	Unit
Supply voltage	V_{DD}	-0,3		7	V
Input voltage	V_I	-0,3		7	V
Total power dissipation	P_{tot}			1	W
Output power dissipation	P_O			10	mW
Operating temperature	T_{amb}	-0		70	°C
Storage temperature	T_{stg}	-55		125	°C

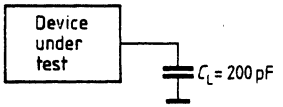
DC and operating characteristics
T_{amb} = -0 to 70°C, V_{CC} = 5 V ± 5%

Supply current	I_{DD}		60	150	mA
Input leakage current V_I = 0 to V_{DD}	I_{IL}	-10		10	µA
H input voltage	V_{IH}	2.0		V_{DD}	V
L input voltage	V_{IL}	0		0.8	V
H output voltage (I_O = -0.2 mA)	V_{OH}	2.4			V
L output voltage (I_O = 2.0 mA)	V_{OL}			0.4	V
Tristate output leakage V_O = 0 to V_{DD}	I_{OL}	-10		10	µA

AC testing input, output waveform



AC testing load circuit



AC testing:

Inputs are driven at 2.4 V for a logic "1" and 0.4 V for a logic "Ø".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "Ø".

PEB 2050
Peripheral Board Controller (PBC)

Preliminary data **MOS circuit**

Features

- Board controller for up to 16 subsribers of a digital switching system
- Designed for different PCM systems
- Time slot assignment freely programmable for all connected subscribers
- Control of voice, data, signaling and line board parameters to minimize hardware requirements and to simplify software
- Provides two full duplex PCM highways for the system interface
- System control uses the HDLC protocol with X.25 level 2 functions performed by the PBC
- Standard µP interface
- Two DMA channels for expansion of internal buffer capability of 16 bytes per direction
- µP access to all internal data streams including time slot-oriented data streams
- Support of subscriber circuits by generating timing signals
- Single 5 V power supply
- Low power consumption

General description

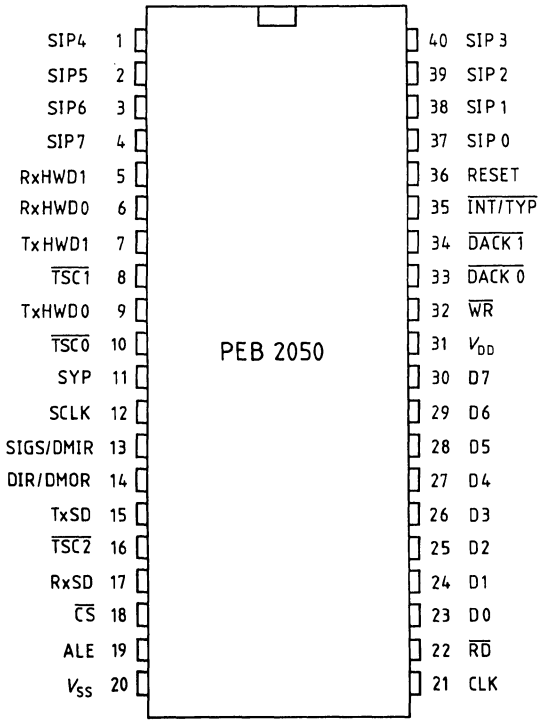
The Peripheral Board Controller PEB 2050 is a device for the control of voice, data, and signaling paths of up to 16 subscribers on peripheral component boards in digital telephone systems. In combination with the highly flexible Siemens Codec Filter (SICOFI PEB 2060) it forms an optimized analog subscriber line board architecture. Its flexibility allows the operation as a general purpose controller for data switching and MUX/De MUX applications.

The PBC controls space and time switching functions between subscriber line devices and time division multiplex highways. Further, it controls the flow of information between the subscriber interface ports and a processor, which can be an optional line card local processor or the central processor directly. Last, it performs all protocol control functions, using the HDLC protocol format for all information passing between the line card and the central processor via a dedicated HDLC line or via interleaved time slots on the PCM lines.

To meet the different requirements the PBC PEB 2050 provides the following interfaces:

- 8 serial, bidirectional I/O ports for the transfer of voice, data, control, and signaling information between the PBC and Codec Filters (e.g. SICOFI PEB 2060), digital interface circuits or signal processors.
- Double constructed PCM interface.
- Fast serial communication link to the central processor.
- Bit-parallel interface for the connection of 8 bit standard microcomputers such as the SAB 8048. The interface is characterized by an interrupt control and two independent DMA channels, one for the transmit and one for the receive direction.

Pin configuration
top view



Pin designation

Pin No.	Symbol	Name/function	Functional description
1 · · · · 4	SIP 4 · · · · SIP 7	Subscriber interface port (input/output)	These interface ports are used for bidirectional, bit-serial transfer of speech, data and control words to and from the Siemens Codec Filter (SICOFI) or standard Codec. Corresponding with the direction signal the PBC PEB 2050 is transmitting during the high level of DIR within the first half of a 125 µs frame.
5	R x HWD 1	Receive highway data (input)	Receive PCM highway 1 interface
6	R x HWD 0	Receive highway data (input)	Receive PCM highway 0 interface. The PBC serially receives a PCM word (8 bits) through one of these leads at the programmed time slot.
7	T x HWD 1	Transmit highway data (output)	Output of the transmit side onto the send PCM highway 1 (serial bus). The 8-bit PCM word is serially sent out on this pin at the programmed time slot. Tristate output.
8	$\overline{\text{TSC 1}}$	Tristate control (output, active low)	Normally high, this signal goes low while the PBC is transmitting an 8-bit PCM word on the PCM highway 1.
9	T x HWD 0	Transmit highway data (output)	Output of the transmit side onto the send PCM highway 0.
10	$\overline{\text{TSC 0}}$	Tristate control (output, active low)	Tristate control of highway 0.
11	SYP	Synchronization	SYP is a frame synchronization pulse which resets the on-chip time-slot counters.
12	SCLK	Slave clock (output)	Clock output for the peripheral devices. The signals between the codec filter and the PBC are latched and transmitted with the rising edge of SCLK.
13	SIGS/DMIR	Signal strobe (output, active high)/direct memory input request (output, active high)	The SIGS output supplies a programmable strobe signal. In the DMA mode, this pin is used as DMA input request.

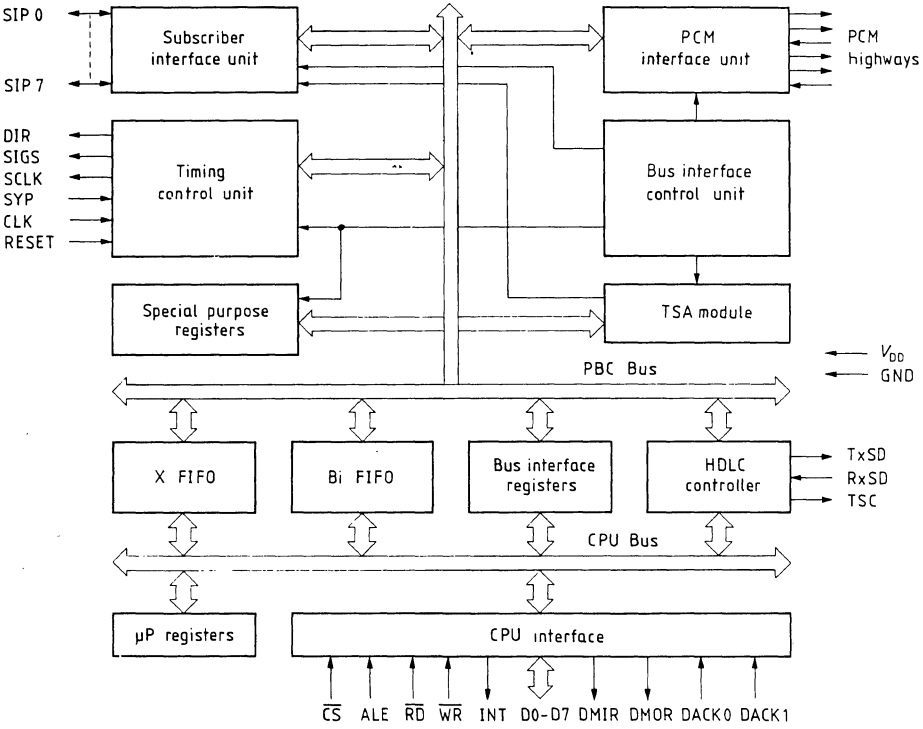
Pin designation

Pin No.	Symbol	Name/function	Functional description
14	DIR/DMOR	Direction (output, active high) direct memory output request (output, active high)	DIR is an 8 kHz symmetric frame signal which controls the direction of the data transfer from and to the peripheral devices. The PBC is able to receive data during the low state of DIR. In the DMA mode this pin is used as DMA output request. DMIR and DMOR are generated by the PBC-internal HDLC receiver or transmitter and are used for handshaking during the DMA transfer.
15	T x SD	Transmit signaling Data (output)	This line transmits the serial data to the dedicated HDLC channel.
16	$\overline{\text{TSC 2}}$	Tristate control to 2 (output, active low)	Normally high, this signal goes low while the PBC is transmitting an HDLC message.
17	R x SD	Receive signaling Data (input)	This line receives the serial data from the HDLC channel.
18	$\overline{\text{CS}}$	Chip select (input, active low)	$\overline{\text{CS}}$ is used to address the PBC. A low level at this input enables the PBC to accept commands or data from a µP within a write cycle, or to transmit data during a read cycle.
19	ALE	Address latch enable (input, active high)	A high level at this input indicates that the data on the external bus is an address selecting one of the PBC-internal sources or destinations. Latching into the address latch occurs during the high low transition.
20	V_{SS}		Ground: 0 V
21	CLK	Clock (input)	A standard TTL clock provides the basic timing of the controller. The clock is synchronous to the PCM clock.

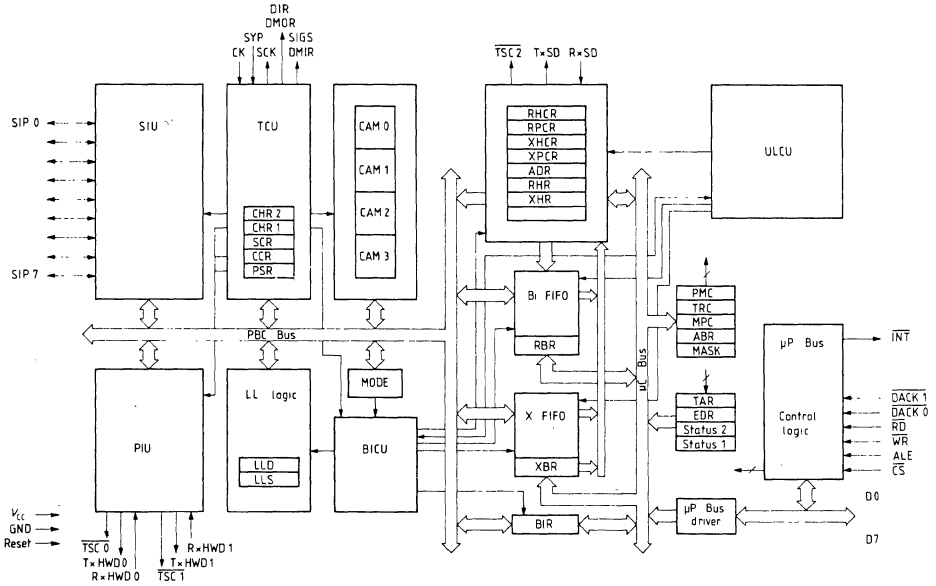
Pin designation

Pin No.	Symbol	Name/function	Functional description
22	$\overline{RD}$	Read strobe (input, active low)	$\overline{RD}$ is used together with CS to transfer data from the PBC to a µP or memory.
23 30	D0 . . . . . D7	System data bus	The data bus transfers data and commands between the µP or memory and the PBC.
31	V_{DD}		Power supply: V_{DD} = 5.0 ± 0.25 V
32	$\overline{WR}$	Write strobe (input, active low)	During the low state of $\overline{WR}$ data can be transferred from the µP or memory to the PBC.
33	$\overline{DACK\ 0}$	DMA acknowledge (inputs, active low)	$\overline{DACK\ 0}$ and $\overline{DACK\ 1}$ are used to acknowledge the DMA output and DMA input request, respectively.
34	$\overline{DACK\ 1}$		
35	$\overline{INT/TYP}$	Interrupt request (output, active low)	This signal is pulled down, when the PBC is requesting an interrupt. In that case the µP should enter into an interrupt routine for reading the status register 1.
36	RESET	Reset (input, active high)	A "high" on this input forces the PBC into reset state. The minimum reset pulse is 16 complete clock cycles.
37 40	SIP 0 . . . . . SIP 3	Subscriber interface port (input/output)	These interface ports are used for bidirectional, bit-serial transfer of speech, data and control words to and from the Siemens Codec Filter (SICOFI) or standard Codec. Corresponding with the direction signal the PBC PEB 2050 is transmitting during the high level of DIR within the first half of a 125 µs frame.

Block diagram



Block diagram



Description of the functional blocks

The PBC has been designed especially for use in peripheral subscriber boards, but its functional flexibility also permits its application in various parts of a digital exchange telecommunication system.

Used in peripheral subscriber boards it performs two essential functions:

1) Exchange of control data between a central processing unit, an "on board" processing unit and individual subscriber connections. The PBC supports the ISO/CCITT's HDLC communication line protocol. An application specific PBC internal controller controls the distribution of data on the board.
2) The time slot controlled transfer of PCM data (64 Kbaud channels) between the PCM highways and the subscriber connections.

Data transfers between both parts, such as signaling through PCM highways (common channel) or the access of the "on board" µP to 64 Kbaud channels, are considerably simplified by the IC.

The two central functional blocks are reflected in the circuit structure: The PCM synchronous portion constitutes the interfaces to the subscribers and the PCM highways. It comprises the following functional blocks:

- SIU (Serial Interface Unit) with Last Look logic.
- PIU (PCM Interface Unit)
- CAM (Content Addressable Memory)
- TCU (Timing Control Unit)
- MODE register
- PBC Bus

The asynchronous portion constitutes the interface to the local microprocessor (8-bit parallel) and to the central control (serial HDLC interface) and comprises the following functional blocks:

- HDLC controller
- µP interface
- µP control and status register
- ULCU (User Level Control Unit)

The two portions are interconnected by the following functional blocks:

- X FIFO (Transmit FIFO)
- Bidirectional FIFO
- BICU (Bus Interface Control Unit)
- BIR (Bus Interface Register)

Maximum ratings		Min	Max	Unit
Storage temperature	T_{stg}	−65	125	°C
Range of operation				
Ambient temperature	T_{amb}	0	70	°C
Voltage at any pin vs. ground	V	−0.3	7	V
Total power consumption	P_{tot}		600	mW

DC characteristics
T_{amb} = 0 to 70°C; V_{CC} = 5 V ± 0.25 V; GND = 0 V

		Conditions	Min	Typ.	Max	Unit
L input voltage	V_{IL}		−0.5		0.8	Volts
H input voltage	V_{IH}		2.0		5.5	Volts
L output voltage	V_{OL}	I_{OL} = +1.6 mA			0.45	Volts
H output voltage	V_{OH}	I_{OH} = −400 µA	2.4			Volts
Input leakage current	I_{IL}	V_{IN} = V_{CC} to 0 V	−10		10	µA
Output leakage current	I_{OL}	V_{OUT} = V_{CC} to 0 V	−10		10	µA
V_{CC} – supply current	I_{CC}	V_{CC} = 5 V		85	120	mA

Capacitance

T_{amb} = 25°C; V_{CC} = GND = 0 V

		Conditions	Min	Typ.	Max	Unit
Input capacitance	C_{IN}	f_C = 1 MHz		5	10	pF
Input/output capacitance	$C_{I/O}$			10	20	pF
Output capacitance	C_{OUT}	unmeasured pins returned to GND		8	15	pF

AC characteristics

T_{amb} = 0 to 70°C; V_{CC} = 5 V ± 0.25 V; GND = 0 V

Microprocessor interface

Read cycle

		Min	Max	Unit
Address hold after ALE	t_{LA}	20		ns
Address to ALE setup	t_{AL}	30		ns
Data delay from $\overline{RD}$	t_{RD}		150	ns
$\overline{RD}$ pulse width	t_{RR}	150	10^7	ns
Output float delay	t_{DF}		25	ns
$\overline{RD}$ control interval case 1*	t_{RI}	2 x CP		ns
$\overline{RD}$ control interval case 2**	t_{RI}	100		ns
ALE pulse width	t_{AA}	60		ns

Write cycle

		Min	Max	Unit
$\overline{WR}$ pulse width	t_{WW}	100		ns
Data setup to $\overline{WR}$	t_{DW}	50		ns
Data hold after $\overline{WR}$	t_{WD}	25		ns
$\overline{WR}$ control interval case 1*	t_{WI}	2 x CP		ns
$\overline{WR}$ control interval case 2**	t_{WI}	50		ns

* Case 1: Read, write of BI FIFO and X FIFO
** Case 2: All other registers

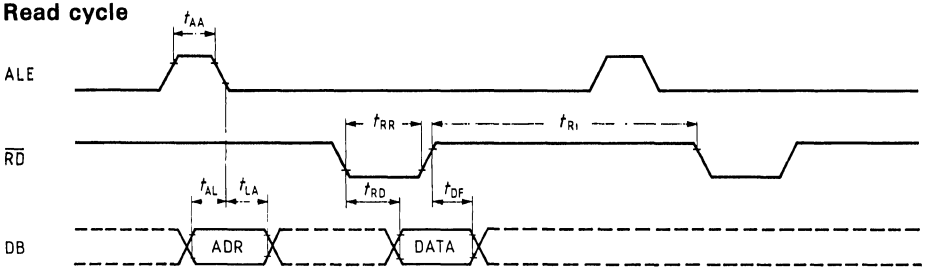
DMA Read		Min	Max	Unit
DMA read time*	t_{DMA}		7 x CP	ns
DMOR hold time	t_{DH}		75	ns
Address stable before $\overline{RD}$	t_{AR}	0		ns
Data delay from $\overline{RD}$	t_{RD}		150	ns
Output floating delay	t_{DF}	20		ns
Address hold after $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ pulse width	t_{RR}	150	10^4	ns

DMA Write		Min	Max	Unit
DMA Write time*	t_{DMA}		7 x CP	ns
DMIR hold time	t_{IH}		80	ns
Address stable before $\overline{WR}$	t_{AW}	0		ns
Address hold after $\overline{WR}$	t_{WA}	0		ns
Data setup to $\overline{WR}$	t_{DW}	30		ns
Data hold after $\overline{WR}$	t_{WD}	25		ns
$\overline{WR}$ pulse width	t_{WW}	100		ns

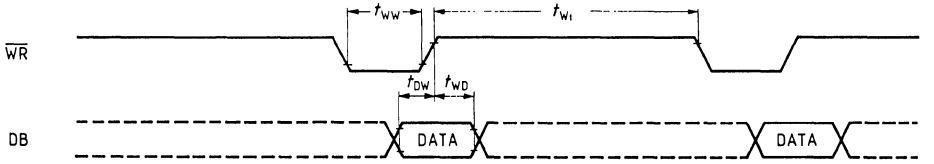
*)

PBC clock/MHz	2.048	4.096	1.536	3.072
2 x CP/ns	980	490	1300	650
7 x CP/µs	3.4	1.7	4.56	2.3

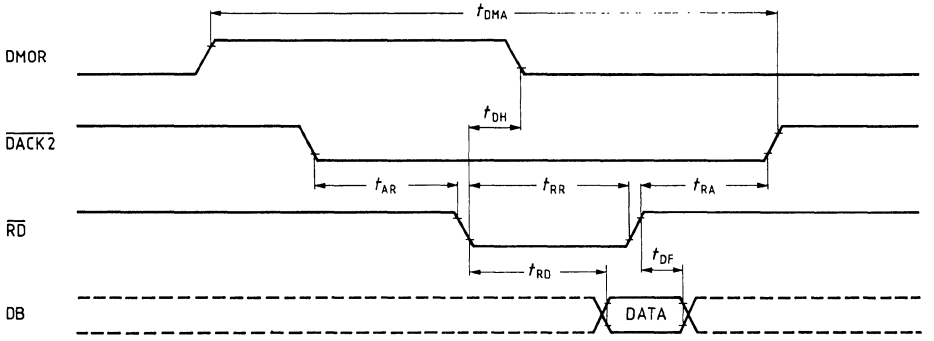
Read cycle



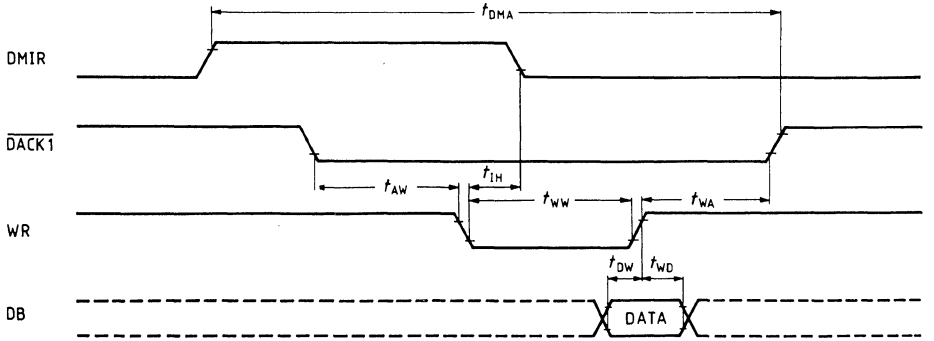
Write cycle



DMA read



DMA write



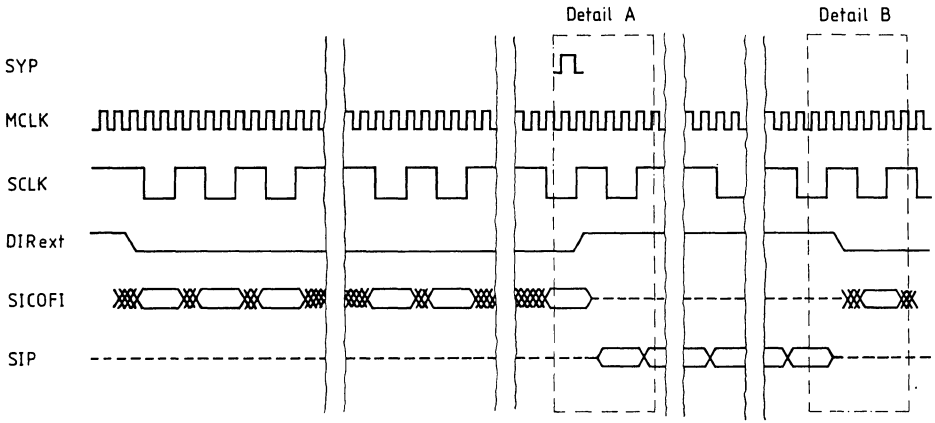
Clock timing

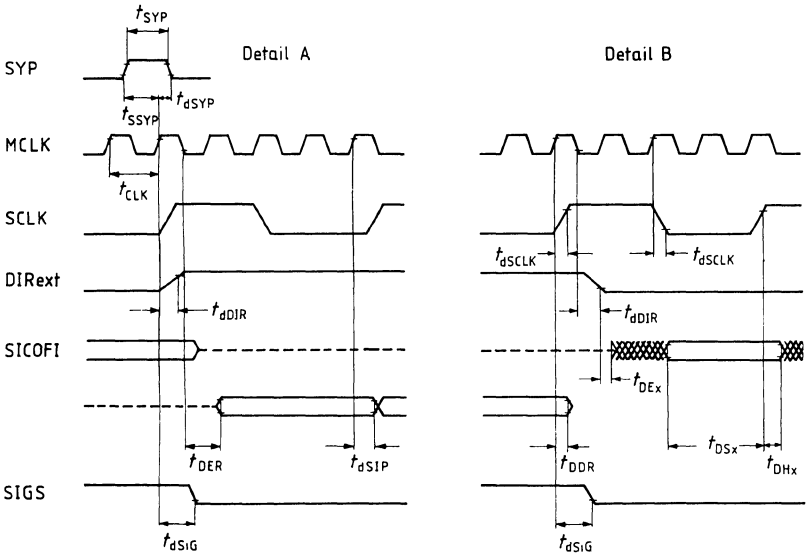
		Min	Max	Unit
System clock				
System clock frequency	CLK	1	4.2	MHz
Duty cycle		45	55	%
Synchron pulse period	t_{SPP}	125	M x 125	µs
Synchron pulse width	t_{SYP}	60	t_{CKL}	ns
Pulse delay to CLK	t_{dSYP}	10		ns
Setup time to CLK	t_{sSYP}	50		ns
Clock rise/fall time	CLK_{rf}		10	ns
Slave clock				
Clock frequency	SCLK	512	512	kHz
Clock delay time	t_{dSCLK}	100	165	ns
DIR Clock				
Delay time to CLK	t_{dDIR}	120	190	ns

SIU interface

		Min	Max	Unit
SIP data delay	t_{dSIP}	160	300	ns
Data enable receive	t_{DER}	100	180	ns
Data disable receive	t_{DDR}	100	180	ns
Data enable transmit	t_{DEX}	0		ns
Data hold transmit	t_{DAX}	0		ns
Data setup transmit	t_{DSX}	CP/2+200		ns
Signaling strobe delay	t_{DSIG}	110	160	ns

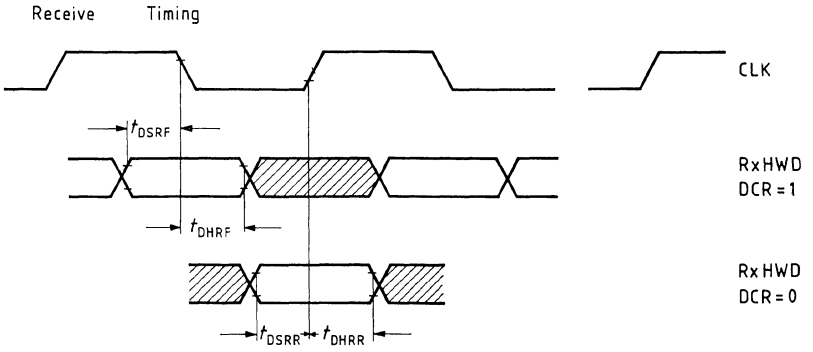
SIP interface timing





Serial port timing

PCM interface		Conditions	Min	Max	Unit
Receive timing					
Receive data setup DCR = 1	t_{DSRF}		20		ns
Receive data setup DCR = 0*	$t_{DS\,RR}$		40		ns
Receive data hold DCR = 1	$t_{DU\,RF}$		40		ns
Receive data hold DCR = 0	$t_{DH\,RR}$		10		ns

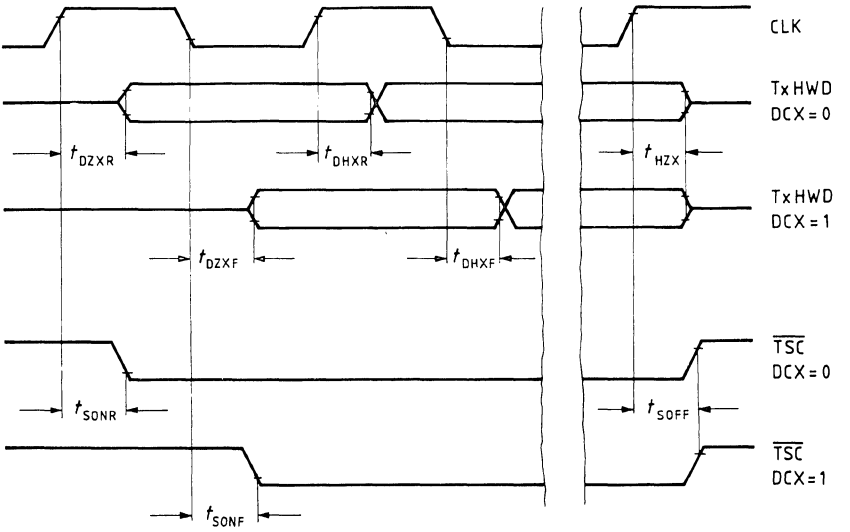


*) Common channel mode t_{DSRR} 60 ns

PCM interface (cont'd)

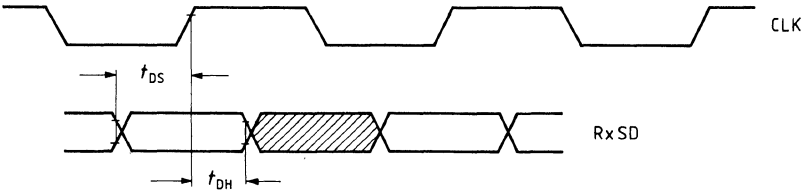
		Conditions	Min	Max	Unit
Transmit timing					
Data enable DCX = 0	t_{DZXR}	C_L = 200 pF	80	160	ns
Data enable DCX = 1	t_{DZXF}	C_L = 200 pF	40	100	ns
Data hold time DCX = 0	$t_{DH\,XR}$	C_L = 200 pF	45	160	ns
Data hold time DCX = 1	t_{DHXF}	C_L = 200 pF	40	100	ns
Data float on TS EXIT	t_{HZX}	C_L = 150 pF	35	80	ns
Time slot x to enable DCX = 0	t_{SONR}	C_L = 150 pF	70	130	ns
Time slot x to enable DCX = 1	t_{SONF}	C_L = 150 pF	40	100	ns
Time slot x to disable	t_{SOFF}	C_L = 150 pF	40	100	ns

Transmit Timing

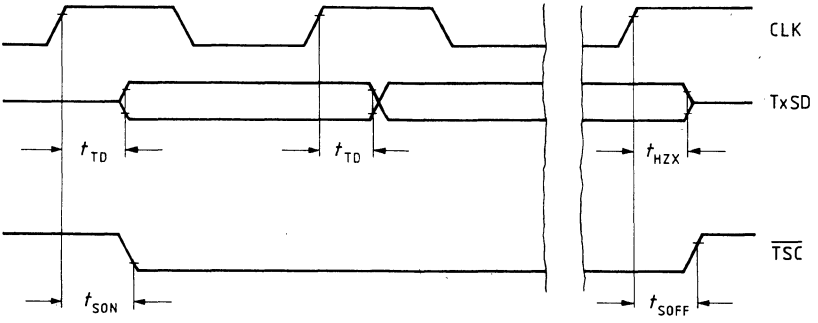


HDLC interface		Condition	Min	Max	Unit
Receive timing					
Receive data setup	t_{DS}		40		ns
Receive data hold	t_{DH}		10		ns
Transmit timing					
Transmit data delay	t_{TD}	C_L = 200 pF	40	100	ns
Data float on TS EXIT	t_{HZX}	C_L = 200 pF	35	80	ns
Time slot x to enable	t_{SON}	C_L = 150 pF	40	95	ns
Time slot x to disable	t_{soff}	C_L = 150 pF	35	90	ns

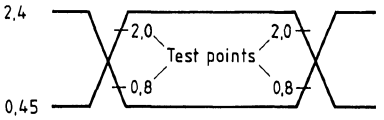
Receive Timing



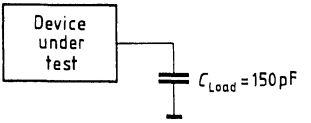
Transmit Timing



AC testing input, output waveform



AC testing load circuit



AC testing: inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

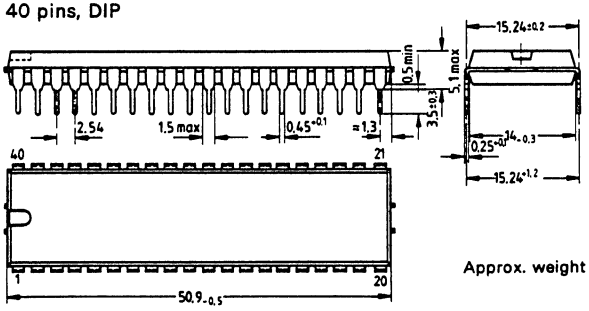
PEB 2051
Peripheral Board Controller (PBC)

Preliminary data **MOS circuit**

Features

- Board controller for up to 16 subscribers of a digital switching system
- Designed for different PCM systems
- Time slot assignment freely programmable for all connected subscribers
- Control of voice, data, signaling and line board parameters to minimize hardware requirements and to simplify software
- Provides four full duplex PCM highways for the system interface
- System control uses the HDLC protocol with X.25 level 2 functions performed by the PBC
- Standard µP interface
- Two DMA channels for expansion of internal buffer capability of 16 bytes per direction
- µP access to all internal data streams including time slot-oriented data streams
- Support of subscriber circuits by generating timing signals
- Single 5 V power supply
- Low power consumption

Plastic plug-in package 20 B 40 DIN 41866
40 pins, DIP



Approx. weight 5.9 g

Dimensions in mm

General description

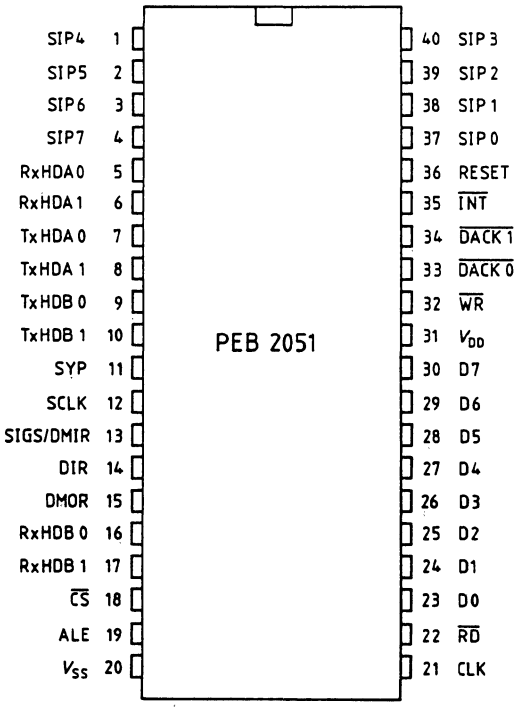
The Peripheral Board Controller PEB 2051 is a device for the control of voice, data, and signaling paths of up to 16 subscribers on peripheral component boards in digital telephone systems. In combination with the highly flexible Siemens Codec Filter (SICOFI PEB 2060) it forms an optimized analog subscriber line board architecture. Its flexibility allows the operation as a general purpose controller for data switching and MUX/De MUX applications.

The PBC controls space and time switching functions between subscriber line devices and time division multiplex highways. Further, it controls the flow of information between the subscriber interface ports and a line card local processor. Last, it performs all protocol control functions, using the HDLC protocol format for all information passing between the line card and the central processor via interleaved time slots on the PCM lines.

To meet the different requirements the PBC PEB 2051 provides the following interfaces:

- 8 serial, bidirectional I/O ports for the transfer of voice, data, control, and signaling information between the PBC and Codec Filters (e.g. SICOFI PEB 2060), digital interface circuits or signal processors.
- Four independent PCM interfaces.
- Bit-parallel interface for the connection of 8 bit standard microcomputers such as the SAB 8048. The interface is characterized by an interrupt control and two independent DMA channels, one for the transmit and one for the receive direction.

Pin configuration
top view

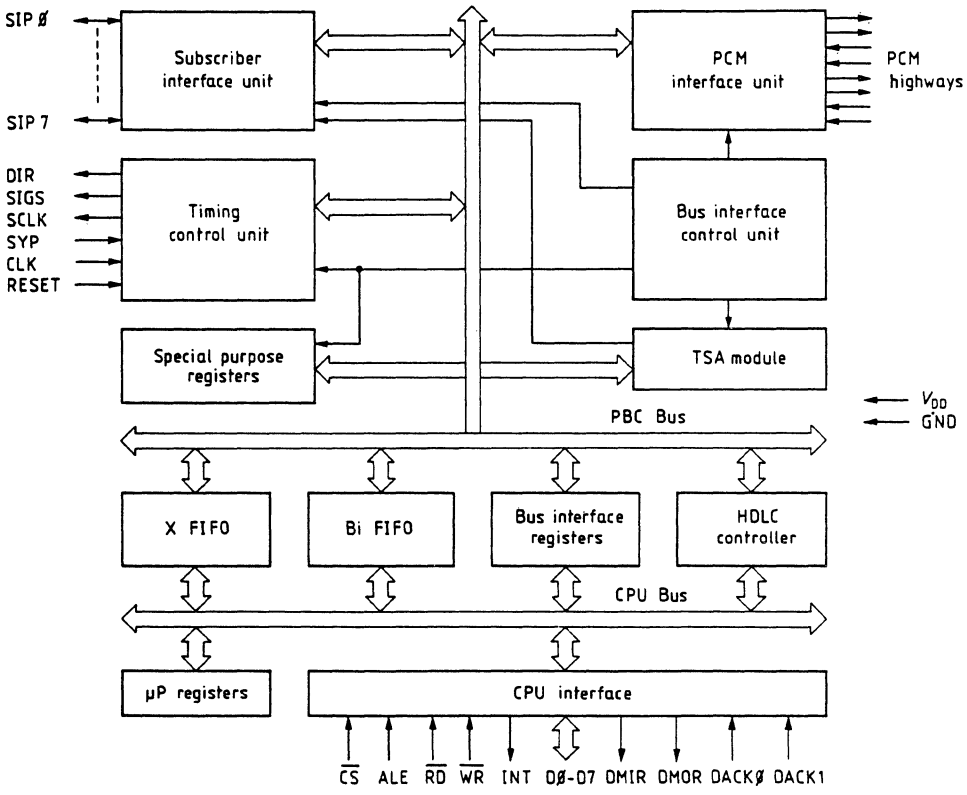


Pin designation

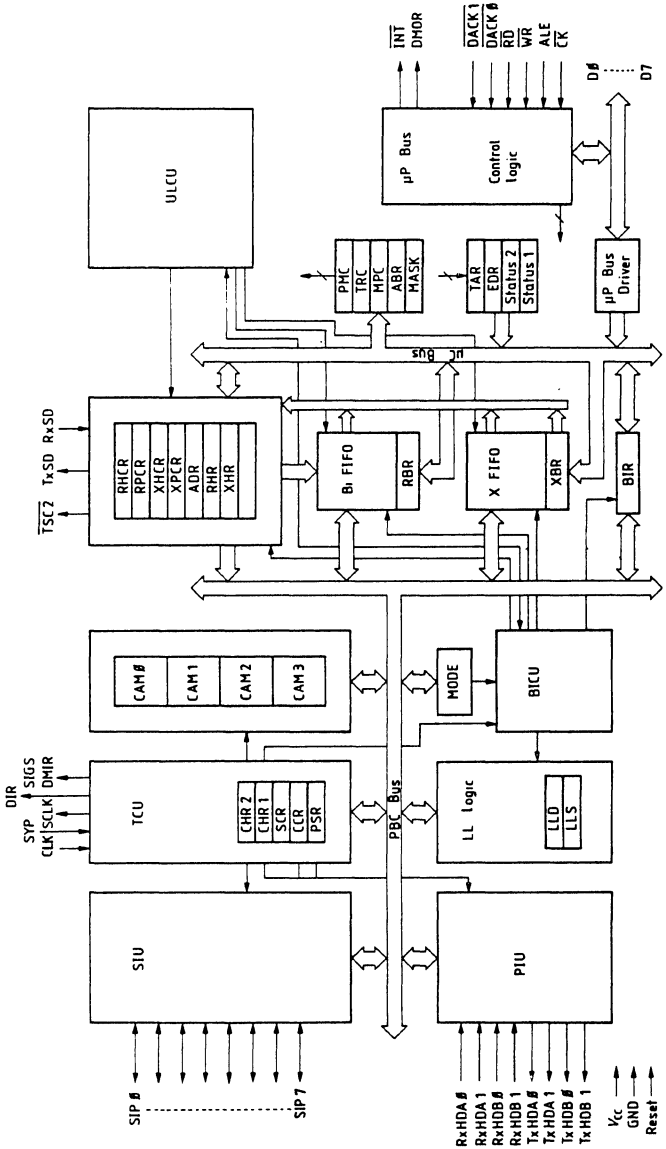
Pin No.	Symbol	Name/function	Functional description
1 . . 4	SIP 4 . . SIP 7	Subscriber Interface Port (input/output)	These interface ports are used for bidirectional, bitserial transfer of speech-, data- and controlwords to and from the Siemens-Codec-Filter (SICOFI) or standard Codec. Corresponding with the direction signal the PBC PEB 2051 is transmitting the high level of DIR within the first half of a 125 µs frame.
5, 6 16, 17	RxHDAØ,1 RxHDBØ,1	Receive Highways Data (input)	Interface ports to the PCM highways.
7, 8 9, 10	TxHDAØ,1 TxHDBØ,1	Transmit Highways Data (output)	The displacement between receive and transmit direction is programmable up to 8 bits.
11	SYP	Synchronization	SYP is a frame synchronization pulse which resets the on chip time slot counters.
12	SCLK	Slave Clock (output)	Clock output for the peripheral devices. The signals between the Codec-filter and the PBC are latched and transmitted with the rising edge of SCLK.
13	SIGS/DMIR	Signal Strobe (output, active High)/ Direct Memory Input Request (output, active High)	The SIGS-output supplies a programmable strobe signal. In the DMA-mode this pin is used as DMA-input-request.
14	DIR	Direction (output)	DIR is a 8 kHz symmetric frame signal which controls the direction of the data transfer from and to the peripheral devices. The PBC is able to receive datas during the low state of DIR.
15	DMOR	Memory Output Request (output) active High	DMIR and DMOR are generated by the PBC internal HDLC-receiver or transmitter and are used for handshaking during the data transfer.
18	$\overline{CS}$	Chip select (input, active Low)	$\overline{CS}$ is used to address the PBC. A low level at this input enables the PBC to accept commands or datas from a µP within a write cycle, or to transmit datas during a read cycle.

Pin No.	Symbol	Name/function	Functional description
19	ALE	Address Latch Enable (input, active High)	A high level at this input indicates that the data on the external bus is an address selecting one of the PBC-internal sources or destinations. Latching into the address latch occurs during the high low transition.
20	V_{SS}		Ground
21	CLK	Clock (input)	A standart TTL-Clock provides the basic timing of the controller. The clock is synchronous to the PCM-clock.
22	$\overline{RD}$	Read Strobe (input, active Low)	$\overline{RD}$ is used together with CS to transfer data from the PBC to a µP or memory
23 . . . 30	DØ . . . D7	System Data Bus	The data bus transfers data and commands between the µP or memory and the PBC.
31	V_{DD}	Supply Voltage	V_{DD} = 5.Ø ± Ø.25 V
32	$\overline{WR}$	Write Strobe (input, active Low)	During the low state of $\overline{WR}$ data can be transfered from the µP or memory to the PBC.
33 34	$\overline{DACKØ}$ $\overline{DACK1}$	DMA-Acknowledge (inputs, active Low)	$\overline{DACKØ}$ and $\overline{DACK1}$ are used to acknowledge the DMA-output and DMA-input request, respectively.
35	$\overline{INT}$	Interrupt Request (output, active Low)	These signal is pulled down, when the PBC is requesting an interrupt. In that case the µP should enter into an interrupt routine for reading the status register 1.
36	RESET	Reset (input, active High)	A "high" on this input forces the PBC into reset state. The minimum reset puls is 16 complete clock cycles.

Block diagram



Block diagram



Description of the functional blocks

The PBC has been designed especially for use in peripheral subscriber boards, but its functional flexibility also permits its application in various parts of a digital exchange telecommunication system.

Used in peripheral subscriber boards it performs two essential functions:

1) Exchange of control data between a central processing unit, an "on board" processing unit and individual subscriber connections. The PBC supports the ISO/CCITT's HDLC communication line protocol. An application specific PBC internal controller controls the distribution of data on the board.
2) The time slot controlled transfer of PCM data (64 Kbaud channels) between the PCM highways and the subscriber connections.

Data transfers between both parts, such as signaling through PCM highways (common channel) or the access of the "on board" µP to 64 Kbaud channels, are considerably simplified by the IC.

The two central functional blocks are reflected in the circuit structure: The PCM synchronous portion constitutes the interfaces to the subscribers and the PCM highways. It comprises the following functional blocks:

- SIU (Serial Interface Unit) with Last Look logic
- PIU (PCM Interface Unit)
- CAM (Content Addressable Memory)
- TCU (Timing Control Unit)
- MODE register
- PBC Bus

The asynchronous portion constitutes the interface to the local microprocessor (8-bit parallel) and to the central control (serial HDLC interface) and comprises the following functional blocks:

- HDLC controller
- µP interface
- µP control and status register
- ULCU (User Level Control Unit)

The two portions are interconnected by the following functional blocks:

- X FIFO (Transmit FIFO)
- Bidirectional FIFO
- BICU (Bus Interface Control Unit)
- BIR (Bus Interface Register)

Maximum ratings		min.	max.	
Storage temperature	T_{stg}	−65	125	°C
Range of operation				
Ambient temperature	T_{amb}	0	70	°C
Voltage at any pin vs. ground	V	−0.3	7	V
Total power consumption	P_{tot}		600	mW

DC characteristics

T_{amb} = 0°C to 70°C; V_{CC} = 5 V ± 0.25 V; GND = 0 V

		Conditions	min.	typ.	max.	
L input voltage	V_{IL}		−0.5		0.8	V
H input voltage	V_{IH}		2.0		5.5	V
L output voltage	V_{OL}	I_{OL} = +1.6 mA			0.45	V
H output voltage	V_{OH}	I_{OH} = −400 µA	2.4			V
Input leakage current	I_{IL}	V_{IN} = V_{CC} to 0 V	−10		10	µA
Output leakage current	I_{OL}	V_{OUT} = V_{CC} to 0 V	−10		10	µA
V_{CC} – supply current	I_{CC}	V_{CC} = 5 V		85	120	mA

Capacitance

T_{amb} = 25°C; V_{CC} = GND = 0 V

		Conditions	min.	typ.	max.	
Input capacitance	C_{IN}	f_c = 1 MHz		5	10	pF
Input/output capacitance	$C_{I/O}$			10	20	pF
Output capacitance	C_{OUT}	unmeasured pins returned to GND		8	15	pF

AC characteristics

T_{amb} = 0°C to 70°C; V_{CC} = 5 V ± 0.25 V; GND = 0 V

Microprocessor interface

Read cycle

		min.	max.	
Address hold after ALE	t_{LA}	20		ns
Address to ALE setup	t_{AL}	30		ns
Data delay from $\overline{RD}$	t_{RD}		150	ns
$\overline{RD}$ pulse width	t_{RR}	150	10^7	ns
Output float delay	t_{DF}		25	ns
$\overline{RD}$ control interval case 1*	t_{RI}	2 x CP		ns
$\overline{RD}$ control interval case 2**	t_{RI}	100		ns
ALE pulse width	t_{AA}	60		ns

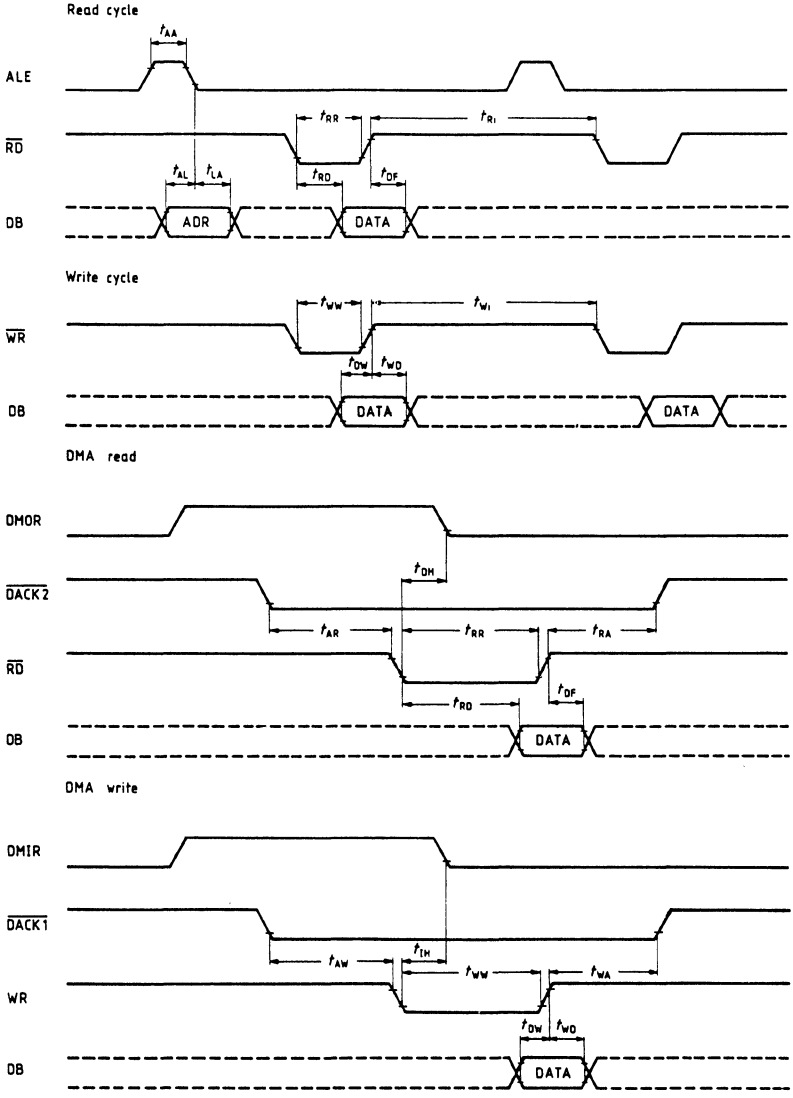
Write cycle

$\overline{WR}$ pulse width	t_{WW}	100		ns
Data setup to $\overline{WR}$	t_{DW}	50		ns
Data hold after $\overline{WR}$	t_{WD}	25		ns
$\overline{WR}$ control interval case 1*	t_{WI}	2 x CP		ns
$\overline{WR}$ control interval case 2**	t_{WI}	50		ns

*Case 1: Read, write of BI FIFO and X FIFO
**Case 2: All other registers

DMA Read		min.	max.	
DMOR hold time	t_{DH}		75	ns
Address stable before $\overline{RD}$	t_{AR}	0		ns
Data delay from $\overline{RD}$	t_{RD}		150	ns
Output floating delay	t_{DF}	20		ns
Address hold after $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ pulse width	t_{RR}	150	10^4	ns
DMA Write				
DMIR hold time	t_{IH}		80	ns
Address stable before $\overline{WR}$	t_{AW}	0		ns
Address hold after $\overline{WR}$	t_{WA}	0		ns
Data setup to $\overline{WR}$	t_{DW}	30		ns
Data hold after $\overline{WR}$	t_{WD}	25		ns
$\overline{WR}$ pulse width	t_{WW}	100		ns

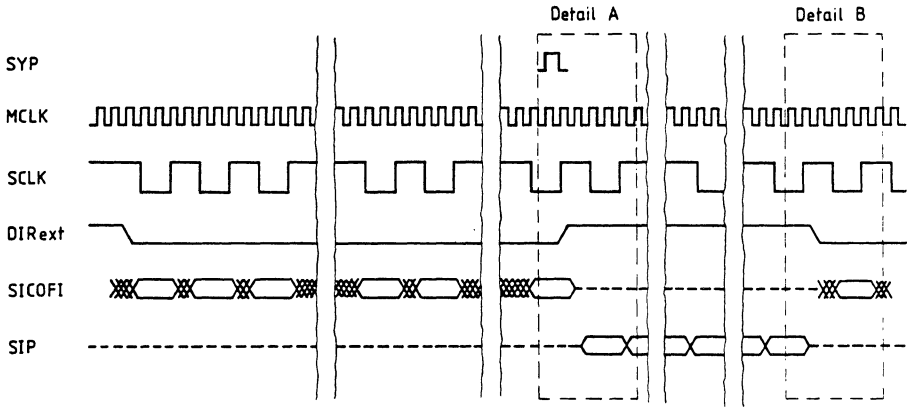
Read cycle

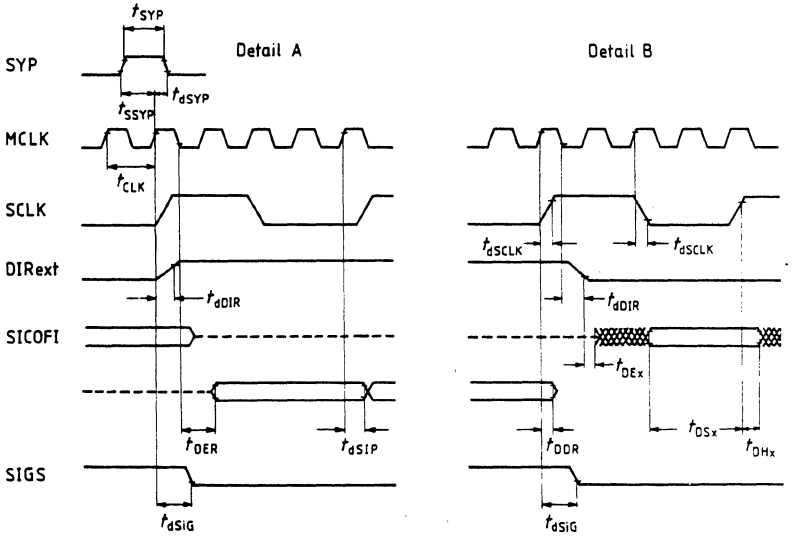

Read cycle
t_{AA}
ALE
t_{RR}
t_{RI}
$\overline{RD}$
t_{AL}
t_{LA}
t_{RD}
t_{DF}
DB
ADR
DATA
Write cycle
t_{WW}
t_{WI}
$\overline{WR}$
t_{DW}
t_{WD}
DB
DATA
DATA
DMA read
DMOR
t_{DH}
$\overline{DACK2}$
t_{AR}
t_{RR}
t_{RA}
$\overline{RD}$
t_{DF}
t_{RD}
DB
DATA
DMA write
DMIR
$\overline{DACK1}$
t_{IH}
t_{AW}
t_{WW}
t_{WA}
WR
t_{DW}
t_{WD}
DB
DATA

Clock timing

		min.	max.	
System clock				
System clock frequency	CLK	1	4.2	MHz
Duty cycle		45	55	%
Synchron pulse period	t_{SPP}	125	M x 125	µs
Synchron pulse width	t_{SYP}	60	t_{CKL}	ns
Pulse delay to CLK	$t_{d\ SYP}$	10		ns
Setup time to CLK	$t_{s\ SYP}$	50		ns
Clock rise/fall time	CLK_{rf}		10	ns
Slave clock				
Clock frequency	SCLK	512	512	kHz
Clock delay time	$t_{d\ SCLK}$	100	165	ns
DIR Clock				
Delay time to CLK	$t_{d\ DIR}$	120	190	ns
SIU interface				
SIP data delay	$t_{d\ SIP}$	160	300	ns
Data enable receive	$t_{D\ ER}$	100	180	ns
Data disable receive	$t_{D\ DR}$	100	180	ns
Data enable transmit	$t_{D\ EX}$	0		ns
Data hold transmit	$t_{D\ AX}$	0		ns
Data setup transmit	$t_{D\ SX}$	CP/2+200		ns
Signaling strobe delay	$t_{D\ SIG}$	110	160	ns

SIP interface timing

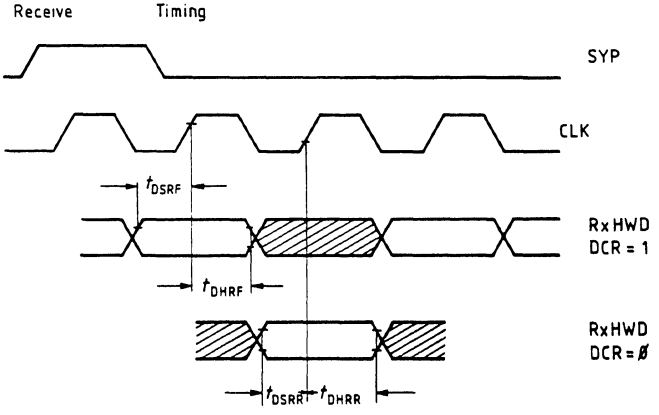




Serial port timing

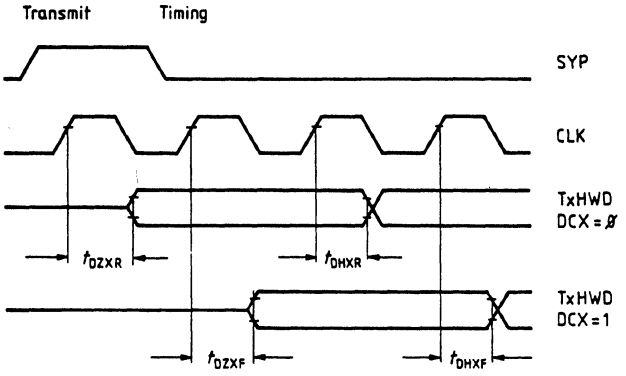
PCM interface

		Conditions	min.	max.	
Receive timing					
Receive data setup DCR = 1	$t_{DS\ RF}$		25		ns
Receive data setup DCR = Ø	$t_{DS\ RR}$		25		ns
Receive data hold DCR = 1	$t_{DU\ RF}$		20		ns
Receive data hold DCR = Ø	$t_{DH\ RR}$		20		ns

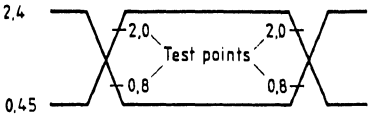


PCM interface (cont'd)

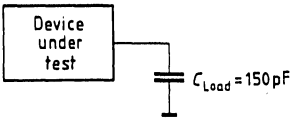
		Conditions	min.	max.	
Transmit timing					
Data enable DCX = Ø	$t_{DZ\,XR}$	C_L = 200 pF	60	140	ns
Data enable DCX = 1	$t_{DZ\,XF}$	C_L = 200 pF	60	140	ns
Data hold time DCX = Ø	$t_{DH\,XR}$	C_L = 200 pF	60	140	ns
Data hold time DCX = 1	$t_{DH\,XF}$	C_L = 200 pF	60	140	ns



AC testing input, output waveform



AC testing load circuit



AC testing: inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

SICOFI PEB 2060
Signal Processing Codec Filter

Target Specification

1. General Description

1.1 Features

The SICOFI PEB 2060 is a fully integrated PCM Codec (coder-decoder) and transmit/receive filter, fabricated in an advanced CMOS technology for applications in digital exchange telecommunication systems. Based on a digital filter concept, the PEB 2060 provides improved transmission performance and high flexibility. The device is optimized for working in conjunction with the Peripheral Board Controller PEB 2050.

- Single chip Codec and Filter
- A/D-, D/A-conversion and PCM-coding/-decoding in A-law and μ-law
- Band limitation in receive and transmit-direction according to CCITT and AT&T recommendations
- Programmable
  - Impedance matching
  - Trans-hybrid balancing
  - Level control
  - Frequency response correction
- Advanced test capabilities
  - Analog loop back (1)
  - Digital loop back (2)
- Serial interface to PEB 2050
- No external components
- No trimming or adjustments
- Digital signal processing techniques
- Programmable interface to periphery (e.g. SLIC)
- Signaling Expansion possible
- Prepared for three-party conferencing
- 0.512 MHz clock
- Low Power CMOS design
- +5V, —5V power supply
- Package: 22-pin DIP

1.2 Subscriber line board architecture

The technical goals for the next stage of innovation for subscriber line boards analog are to efficiently realize in a high degree of integration intricate switching functions, decentralized intelligence, software control of analog functions and expanded testing capability. Fig. 1 shows the Siemens line board concept containing the PEB 2050 Peripheral Board Controller and, working as it's slave device, the PEB 2060.

The PEB 2050 constitutes the interface between up to 16 SICOFIs, the PCM lines, a remote central control unit and, optionally, an on-board microprocessor. The device permits efficient switching of data streams between all these interfaces and supplies

fully programmable time slot assignment for 16 subscribers as well as processing of voice, data, signaling and control information (see PBC-specification). The PEB 2050 thus opens up attractive technical possibilities such as common channel signaling via PCM-time slots and microprocessor access to PCM data. Hardwired implementation of basic control and interface functions allows real time processing of different complex procedures and simplifies software structure without loss of flexibility.

Datahandling between the PEB 2060 SICOFI and the PEB 2050 PBC in a simple serial Ping Pong interface for the SICOFI results in significant pin-reduction and comprises modular pc-board design.

Besides PCM filtering and PCM coding, the PEB 2060 supports software controlled adjustment of the analog behavior and handles the signals for monitoring and control of a SLIC.

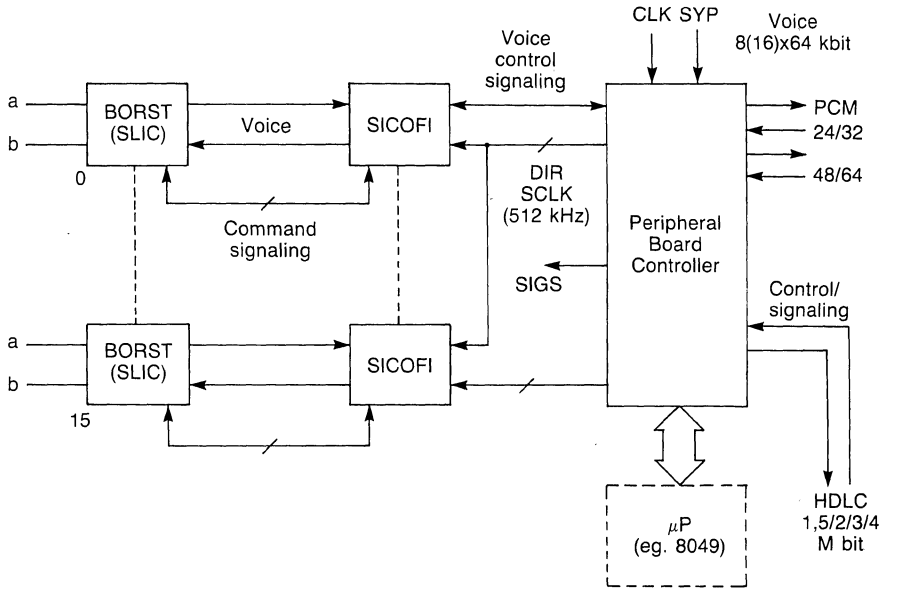


Fig. 1: Line Board Architecture

2. SICOFI-Principles

The SICOFI-approach is highly digital comprising the typical advantages of digital signal processing such as highly predictable performance, flexibility, tolerance to technology fluctuations and temperature variation, low crosstalk sensitivity, high power supply rejection and excellent testability. Moreover, the approach potentially enables the control of the device's analog behavior by digital signal processing, including attractive features such as programmable level control, impedance matching and programmable trans-hybrid balancing.

2.1 Signal Processing Flow

Fig. 2 shows the SICOFI's complete signal processing flow.

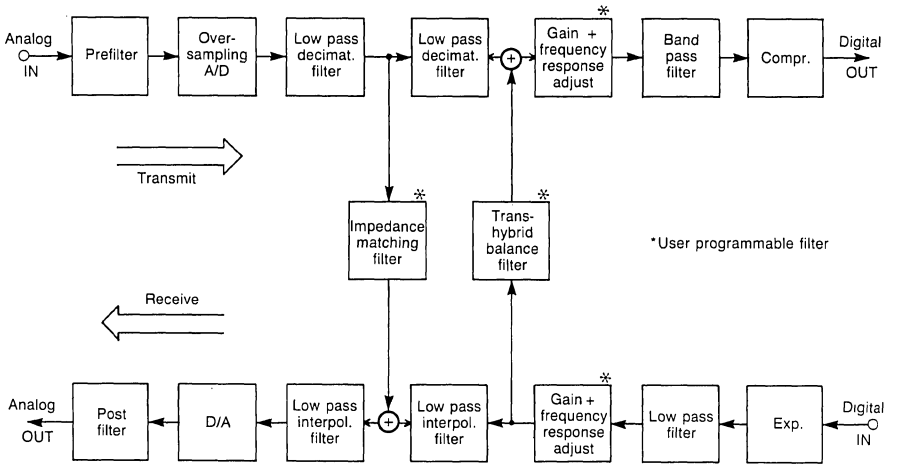


Fig. 2: Signal Flow

In the transmit path, the analog input signal is converted, filtered and companded. The pre-filter is a 2nd order anti-aliasing Filter (Sallen-Key). The A/D-Converter uses a modified slope-adaptive interpolative delta-sigma modulator and samples the input signal at a rate of 128 kHz. Together with the PCM-lowpass of the bandpass-filter, subsequent decimation filters perform down-sampling to 8 kHz. Bandlimitation is performed by the combination of a high order lowpass and highpass-filter. The use of Wave-Digital-Filters for bandlimitation provides excellent pass- and stopband properties and traceable stability (important in cases of critical system loops).

In receive direction, built with similar filters as in the transmit direction, the PCM-Signal is expanded, band-limited, interpolated to a frequency of 256 kHz and fed to the D/A-Converter. The post-filter is a simple 1st order Low-Pass.

The X- and GX-Filters in transmit- and the R- and GR-Filters in receive-direction are user-programmable filters for gain and frequency response adjust, respectively. The programmable B- and Z-Filters provide trans-hybrid-balancing and complex line termination.

Actually, all the digital filtering is performed by a signal processor with highly optimized architecture. While the band pass in transmit- and the low pass in receive-direction are realized by Wave-Digital-Filters, all other programmable and non-programmable filters are FIR-Filters.

The SCIOFI is capable of both A-law and μ-law companding.

2.2 SICOFI Block Diagram

In a simplified block diagram, the SICOFI sections are shown in Fig. 3.

The Slic-interface provides for voice and signaling I/O and the PBC-interface provides clock, frame synchronisation and bi-directional serial data transfer. All digital in-puts and outputs are TTL-compatible.

The voltage reference is generated on-chip and is calibrated during the manufacturing process. The PLL-circuit supplies the SICOFI's internal master clock of 4.096 MHz, derived from the 512 kHz slave clock.

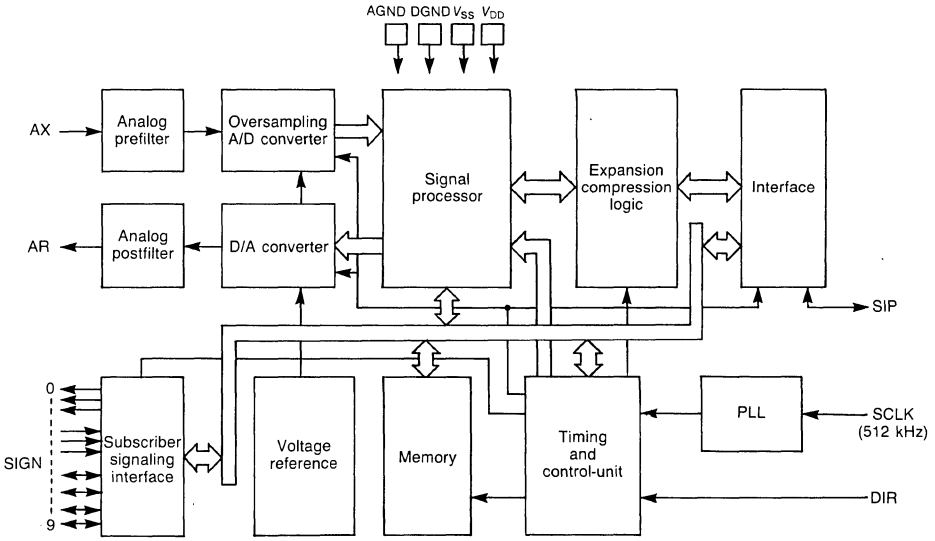


Fig. 3: Block Diagram

3. Serial Interface

The exchange of data between the Peripheral Board Controller and the SICOFI is based on a bidirectional bitserial interface consisting of 3 PINs: SIP, DIR and SCLK. Data are loaded or read out on the Serial Interface Port SIP under control of a symmetric direction signal DIR with a period of 125 μsec.

The interface clock frequency supplied via the slave clock pin SCLK is 512 kHz (Fig. 4).

During the high level state of DIR, 4 bytes of information are transfered from the PBC to the SICOFI and similarly from the SICOFI to the PBC during the low level state. Bit 7 is the first bit transfered and Bit ϕ is the last one in each byte. The four bytes are:

Channel A
Channel B
Control
Signaling

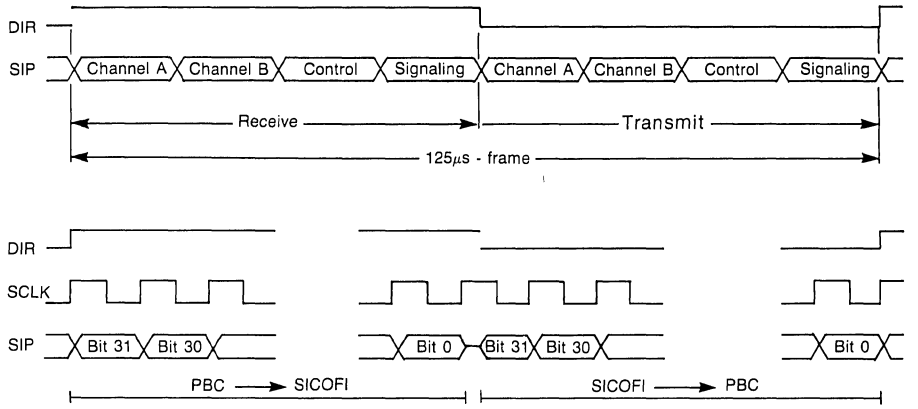


Fig. 4: Byte sequence and timing at Serial Interface Port SIP

If one SICOFI is connected to a PBC-Port, voice is received on channel A and transmitted on Channel A and B.

For a three-way conference, channel B is the third party voice channel.

If two SICOFI's are connected to one PBC-Port, channel A is assigned to one and channel B to the other SICOFI. (see 4.5, case 6). Conferencing is not possible in this configuration.

Bytes 3 and 4 contain feature-control for the SICOFI and signaling information for periphery (e.g. SLIC).

The SICOFI is transparent to byte 4.

4. Programming

Due to the fact, that the SICOFI needs extended control information, a message oriented byte transfer is used. One control byte per frame and direction is transferred. If no status modification or data exchange is required, this is a NOP-Byte. With the appropriate commands, data can be written into or read back from the SICOFI.

A message to the SICOFI is opened by a SICOFI-write-command, which is followed by up to 8 bytes of data. To a PBC-read-command, the SICOFI responds with the requested information, immediately starting with the next transmission period. The message end is characterized by a NOP-Byte.

4.1 Classes of Control-Bytes

The 8 bit wide control words consist of either commands, status information or data.

There are 3 classes of commands:

NOP NORMAL OPERATION
no status modification or data exchange

SOP STATUS OPERATION
contains information about the SICOFI status and use of signaling expansion logic

COP COEFFICIENT OPERATION
contains information about data exchange

SOP and COP contain additional address information which is valid if 2 SICOFIS are connected to one PBC-port.
The class of a command is defined by bits 2 and 3 in each control-byte in the following way.

CONTROL-BYTE

BIT	7	6	5	4	3	2	1	ϕ

BIT 3	2	
x	ϕ	COP
ϕ	1	SOP
1	1	NOP

4.2 NOP-Command

If no status modification of the SICOFI or control-data exchange with the PBC is required, a Normal Operation byte NOP is transferred.

NOP-Format

BIT	7							0
	1	1	1	1	1	1	1	1

4.3 SOP-Command

If the SICOFI-Status has to be changed, a Status Operation byte SOP is transferred, which contains the following information:

BIT	7	6	5	4	3	2	1	0
	AD	R/W	PU	TR	ϕ	1	LSEL	

AD ..... Address information which is relevant if 2 SICOFIs are connected to one PBC-Port. A SICOFI is identified, if AD is consistent with the level at SA (see 4.5/6)

R/W .... Read/Write-information
Enables reading out from the SICOFI or writing information to the SICOFI (READ = 1, Write = ϕ)

PU ..... Power up/Power down
PU = 1 sets the SICOFI to power-up mode (operating),
PU = ϕ resets the SICOFI to power-down (standby).

TR ..... Trunk offering (Three party conferencing)
If TR = 1, the received voice bytes of channel A and B are added.

LSEL ... Length select
Defines the number of the subsequent data-bytes

4.3.1 SOP-WRITE

If the SICOFI-status has to be defined initially or changed, the SOP-Command looks like

7						ϕ
AD	ϕ	PU	TR	0	1	LSEL

and the subsequent configuration-bytes are written into one or both of the two Configuration Registers CR1, CR2 available.

In this case, the meaning of LSEL is

ϕ	ϕ	status setting is completed (no byte following)
1	1	one byte will follow and is stored in CR1
1	ϕ	two bytes will follow and are stored in CR2 and CR1 (see 4.6)
ϕ	1	not used

Corresponding to the configuration-bytes transmitted, the information contained in the configuration-registers is for

CR1:

DB	RZ	RX	RR	RG	TM	TM	TM

where

DB ..... Disable B-Filter (DB = 1), restore B-Filter (DB = 0)
RZ ..... Disable Z-Filter (RZ = ϕ), restore Z-Filter (RZ = 1)
RX ..... Disable X-Filter (RX = ϕ), restore X-Filter (RX = 1)
RR ..... Disable R-Filter (RR = ϕ), restore R-Filter (RR = 1)
RG ..... Disable GX, GR (RG = ϕ), restore GX, GR (RG = 1)

TM ..... Test-Modes

ϕ	ϕ	ϕ	No Test-Mode
ϕ	ϕ	1	Analog loop-back via Z-Filter (Z = 1, I1 = ϕ)
ϕ	1	ϕ	Disable High-Pass
ϕ	1	1	Cut off receive-path (HP active)
1	ϕ	ϕ	not used
1	ϕ	1	not used
1	1	ϕ	Digital loop back via B-Filter (B = 1, D3 = ϕ, HP Active)
1	1	1	Digital loop back via PCM-Register (PCM-in = PCM-out)

and CR2:

7							ϕ
D	C	B	A	EL	AM	μ/A	PCS

where

D signaling PIN SD is input (D = 1) or output (D = ϕ)
C SC is input (C = 1) or output (C = ϕ)
B SB is input (B = 1) or output (B = ϕ)

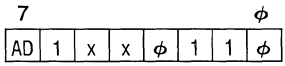
A	SA is input (A = 1) or output (A = ϕ)
EL	signaling expansion logic connected (EL = 1) or not connected (EL = ϕ)
AM	Address-Mode one SICOFI (AM = 1) or two SICOFIs (AM = ϕ) connected to one PBC-port (If AM = ϕ, SA is input automatically)
μ/A	μ-law (μ/A = 1), A-law (μ/A = ϕ)
PCS	Programmed B-Filter-coefficients (PCS = ϕ) or fixed coefficients for B-Filter (PCS = 1)

Note:

1) The power-on-reset or a hardware-reset via RS-PIN reset all CR1-bits to ϕ (all of the programmable Filters are disabled except the B-Filter, where fixed coefficients are used) and set all CR2-bits to 1 (SA, SB, SC, SD are inputs; singaling expansion recognition; μ-law chosen; one SICOFI per PBC-Port). The Serial Interface Port SIP remains tri-state until the content of CR2 has been defined (transmitted and loaded).
2) If two SICOFIs are connected to one PBC-Port, while initializing, both SICOFIs get the same SOP and CR2- information. The subsequent CR1-byte is assigned to the addressed SICOFI only. If the two SICOFIs need different CR2-information, the SOP-CR2-sequence has to be provided once again (each SICOFI knows it's address now).

4.3.2 SOP-Read

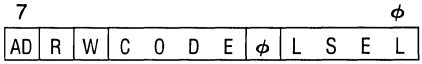
If the SICOFI-Status has to be evaluated, with the SOP-Command



the content of CR1 and CR2 is read back on SIP. The meaning of the SOP-Bits is as described in the SOP-write section.

4.4 COP-Command

With a COP-Command



coefficients for the programmable filters can be written into or read out from the coefficient-RAM.

Where

AD ..... Address (relevant if 2 SICOFIs are connected to one PBC-Port)
R/W .... Read (R/W = 1), Write (R/W = ϕ)

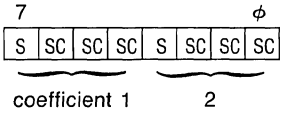
Code

000	B-Filter coefficients part 1	(followed by 8 bytes of data)
001	B-Filter coefficients part 2	(followed by 8 bytes of data)
010	Z-Filter coefficients	(followed by 8 bytes of data)
011	B-Filter delay coefficients	(followed by 4 bytes of data)
100	X-Filter coefficients	(followed by 8 bytes of data)
101	R-Filter coefficients	(followed by 8 bytes of data)
110	GX, GR-coefficients	(followed by 4 bytes of data)
111	not used	

LSEL

ϕ	ϕ	4 Byte
ϕ	1	12 Byte (presently not used)
1	ϕ	ϕ Byte
1	1	8 Byte

Data-Byte Format



S: Sign
SC: Shift-Code

Note: Subsequent to reading of the Filter coefficients, CR2 and CR1 are transmitted additionally.

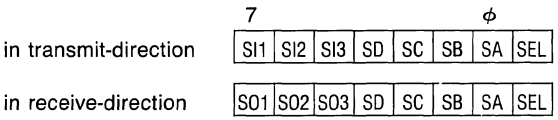
4.5 Signaling-Byte

The signaling interface of the SICOFI consists of 10 pins 3 transmit signaling inputs SI_n, 3 receive signaling outputs SO_m and 4 signaling pins SA, SB, SC, SD, which are programmable individually as either transmit input or receive output.

Data present at SI_n and possibly at some or all of SA, SB, SC, SD (if programmed as inputs) are sampled and transferred serially on SIP to the PBC.

Data received serially on SIP are latched and fed to SO_m and possibly to some or all of SA, SB, SC, SD (if programmed as outputs).

The signaling field format generally is



where SEL is the signaling expansion bit if EL = 1 in CR2.

For the different cases possible, the signaling byte format at SIP is for

		Receive Signaling byte								Transmit Signaling byte							
CASE	**BIT**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**φ**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**φ**
1		SO1	SO2	SO3	Y	Y	Y	Y	Y	SI1	SI2	SI3	SD	SC	SB	SA	X
2		SO1	SO2	SO3	Y	Y	Y	Y	Y	SI1	SI2	SI3	SD	SC	SB	SA	Z
3		SO1	SO2	SO3	SD	SC	SB	SA	Y	SI1	SI2	SI3	φ	φ	φ	φ	X
4		SO1	SO2	SO3	SD	SC	SB	SA	Y	SI1	SI2	SI3	Z	Z	Z	Z	Z
5	A-SICOFI	SO1	SO2	SO3	Y	Y	Y	Y	Y	SI1	SI2	SI3	SD	Z	Z	Z	Z
	B-SICOFI	Y	Y	Y	Y	SO1	SO2	SO3	Y	Z	Z	Z	Z	SI1	SI2	SI3	SD
6	A-SICOFI	SO1	SO2	SO3	SD	Y	Y	Y	Y	SI1	SI2	SI3	φ	Z	Z	Z	Z
	B-SICOFI	Y	Y	Y	Y	SO1	SO2	SO3	SD	Z	Z	Z	Z	SI1	SI2	SI3	φ

Z...High impedance state
Y...Don't care state
X...Either high or low level state, that is not evaluated by the PBC

cases:

1 one SICOFI connected to one PBC-Port; EL = ϕ (no expansion logic); SA, SB, SC, SD programmed as transmit signaling inputs

2 one SICOFI; EL = 1 (expansion logic provided); SA, SB, SC, SD programmed as in case 1

3 one SICOFI; EL = ϕ; SA, SB, SC, SD programmed as receive signaling outputs

4 one SICOFI; EL = 1; SA, SB, SC, SD programmed as in case 3
If an expansion logic is provided (cases 2, 4), the signaling bits SA, SB, SC, SD which are programmed as signaling inputs or outputs can be used as additional expansion bits in receive or transmit direction, respectively (As far as the SICOFI is concerned, SIP is in a high impedance or don't care state while these bits are transfered).

5 Two SICOFIs connected to one PBC-Port; SD programmed as transmit signaling input

6 Two SICOFIs, SD programmed as receive signaling output. If two SICOFIs are connected to one PBC-Port, no expansion logic is provided. SA is programmed as input automatically and defines the addressed SICOFI: SA = ϕ : A-SICOFI
SA = 1 : B-SICOFI

SB and SC are not usable in this configuration

4.6 Programming Procedure

The following table shows some control byte sequences. If the SICOFI has to be configured completely while initializing, up to 58 bytes are transfered.

DIR	Receive	Transmit										
Normal Status	NOP	NOP	NOP	NOP								
SOP-Write	SOP	NOP	CR2	NOP	CR1	NOP	{NOP COP SOP}					
SOP-Read	SOP	CR2	Y	CR1	{NOP SOP COP}							
COP-Write	COP	NOP	DB1	NOP	.....		DBN	NOP				
COP-Read	COP	DB1	Y	DB2	..	DBN	Y	CR2	Y	CR1	{NOP COP SOP}	

where

y . . . ignored

DBn . . . Data Bye #n

5. Operating modes

5.1 Basic setting

Upon intial application of V_{DD} or RS = 1 while operating, the SICOFI enters a basic setting mode.

Additionally, once the V_{DD} supply is up, if it falls below a voltage, which could lead to the loss of programmed coefficients (spikes on V_{DD}-rail are ignored), the SICOFI is forced to this mode again. Basic setting means, that the configuration registers 1 and 2 are initialized (see 4.3.1), receive signaling registers are cleared, SIP is in a high impedance state, the analog output and the receive signaling outputs are forced to ground.

The serial interface is active to receive commands.

5.2 Standby mode

By reception of an SOP-command to load CR2, from the basic setting the SICOFI enters the standby mode (basic setting replaced by individual (CR2). Being in the operating mode, the SICOFI is reset to standby mode with a power-down command.

The interface is active to receive and transmit new commands and data.

5.3 Operating mode

From the standby mode, the operating mode is entered upon recognition of a power-up command. A received power-up command is recognized only, if V_{SS} ‡GND at this instant, otherwise the SCIOFI stays in the standby mode.

6. Transmission Characteristics

The target figures in this specification are based on the subscriber line board requirements. The proper adjustment of the programmable filters (trans-hybrid balancing: B; line termination: Z; frequency-response-correction: X, R) needs a complete knowledge of the SICOFIs analog environment. In the figures listed below it is assumed therefore, unless otherwise stated, that the programmable filters have the following transfer functions:

$$Z = B = O;\ X = R = 1$$

A ϕ dBmϕ signal is equivalent to 1,6 VRMS. A 3 dBmϕ signal is equivalent to 2.26 VRMS which corresponds to the overload point of 3.196 V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITION
G	Gain (either value)					
	Deviation from ideal value		±0.1	±0.2	dB	800Hz at ϕ dBmϕ
	Deviation from initial value		±0.1	±0.2	dB	800Hz at ϕ dBmϕ
G_1	Loop gain (digital to dig)			±0.1	dB	
D_{XA}	Transmit delay, absolute		350		μsec	f = 1.4 kHz, Note 1
D_{RA}	Receive delay, absolute		352		μsec	f = 300 Hz, Note 1
HD	Harmonic distortion			-46	dB	Note 2
IMD	Intermodulation			-42	dB	Note 3, $2f_1$-f_2
				-56	dBMϕ	Note 4, $2f_1$-f_2
CT	Crosstalk					
CT_{XR}	Transmit to Receive			-70	dBmϕ	ϕ dBmϕ, f = 300Hz to 3400Hz
CT_{RX}	Receive to Transmit			-70	dBmϕ	ϕ dBmϕ, f = 300Hz to 3400Hz
N	Idle channel noise					
N_{RP}	weighted			-75	dBmϕp	
N_{RS}	single frequency			-55	dBmϕ	f = 0 to 100kHz, loop around

Note 1: typical delays for B = 0, Z = 0, R = X = 1, including delay through A/D, D/A Specific filter-programming (Z, R, X) may cause additional group delays.

Note 2: single frequency components between 300 Hz and 3400Hz, produced by a ϕdBM ϕ sine wave in the range 300Hz to 3400Hz

Note 3: equal input levels in the range of -4dBMϕ to -21dBmϕ, different frequencies in the range of 300 Hz to 3400 Hz

Note 4: input level -9dBmϕ, frequency range 300Hz-3400Hz and -23dBmϕ, 50Hz

6.1 A-law/μ-law Conversion codes

The encoding laws according to CCITT or AT&T recommendations are digitally selectable.

6.2 Gain Adjustments

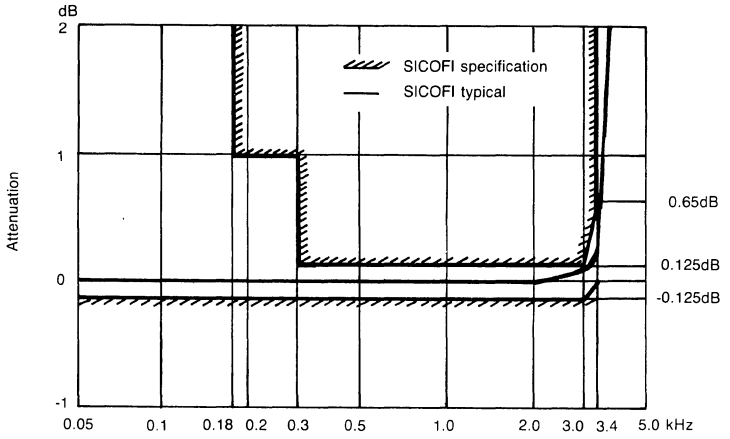
The transmit and receive path gain values are digitally programmable.

Convered range	Resolution
-40 . . . +10,2dB	≤0,5 dB
-40 . . . +12 dB	≤1,2 dB

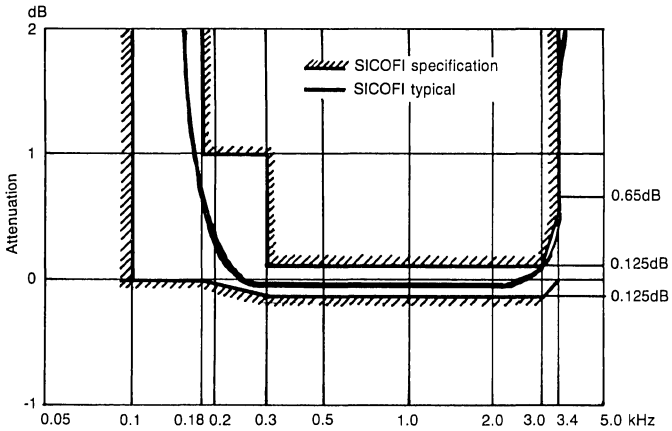
All level-dependent characteristics hold true for any gain setting within the above defined range.

6.3 Attenuation distortion

The attenuation-characteristics for transmit and receive-path are shown in the following diagrams.



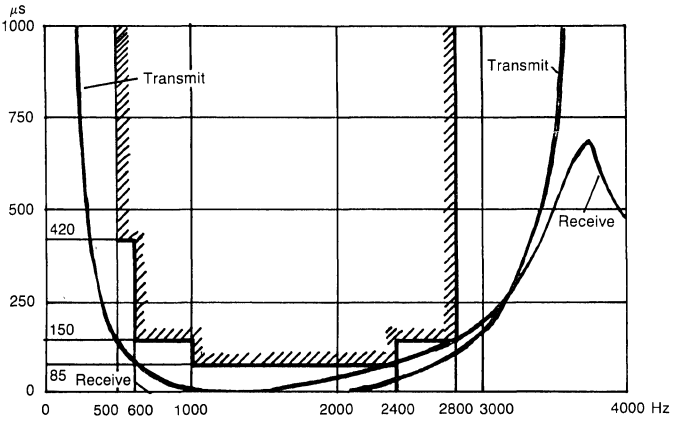
ATTENUATION DISTORTION in RECEIVE DIRECTION
Reference frequency is 1kHz
Input signal level is ϕdBmϕ



ATTENUATION DISTORTION in TRANSMIT DIRECTION
Reference frequency is 1kHz
Input signal level is ϕdBmϕ

6.4 Group delay distortion

For either transmission path, the group delay distortion is within the limits of the following figure. The minimum value of the group delay is taken as reference (see table).



GROUP DELAY DISTORTION
Input signal is ϕdBmϕ

6.5 Out-of-Band Signals at Analog Input

When an out-of-band sine-wave signal with frequency f and level A is applied to the analog input, the level of any frequency component below 4 kHz at the digital output causes by the out-of-band signal is at least X dB below the level of a signal at the same output originating from an 800 Hz AϕdBmϕ sine-wave signal applied to the analog input.

The minimum requirements fullfilled are listed below.

out-of-band input frequency f	out-of-band input level A	attenuation at digital output
0Hz≤f≤ 60Hz	-45dBm0≤A≤0dBm0	25dB
60Hz≤f≤ 100Hz	-45dBM0≤A≤0dBm0	10dB
3400Hz≤f≤4000Hz	-45dBm0≤A≤0dBm0	0dB
4000Hz≤f≤4600Hz	-45dBm0≤A≤0dBm0	14dB
4600Hz≤f≤ 12kHz	-45dBm0≤A≤-15.8dBm0	35dB
12kHz≤f≤ 20kHz	-45dBm0≤A≤-23.2dBm0	35dB
20kHz≤f	-45dBm0≤A≤-25 dBm0	35dB

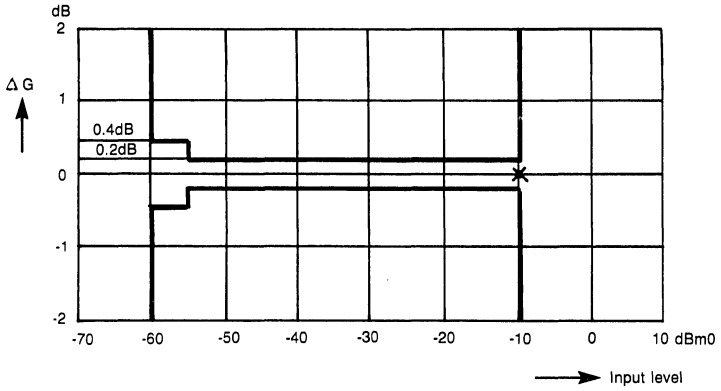
6.6 Out-of-Band Signals at Analog Output

With code words representing any sine-wave signal with the frequency f at a level of ϕdBmϕ applied to the digital input, the maximum level of the spurious out-of-band signals is listed in the table below.

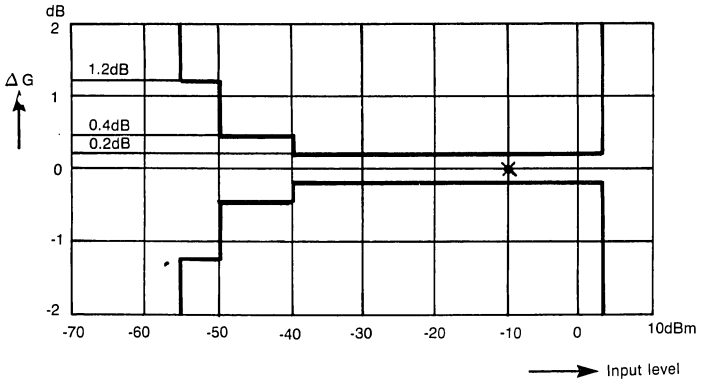
digital input frequency range	level	spurious out-of-band signal frequency range f	max. level at analog output
300Hz 3400Hz	0dBm0	f<90kHz	-40dBm0
300Hz 3400Hz	0dBm0	90kHz≤f≤1MHz	-44dBm0
3400Hz 4000Hz	0dBm0	3400Hz≤f≤4000Hz	0dBm0
3400Hz 4000Hz	0dBm0	4000Hz≤f≤4600Hz	-14dBm0

6.7 Gain Tracking

The gain deviations stay within the limits in the figures below for either transmission path.



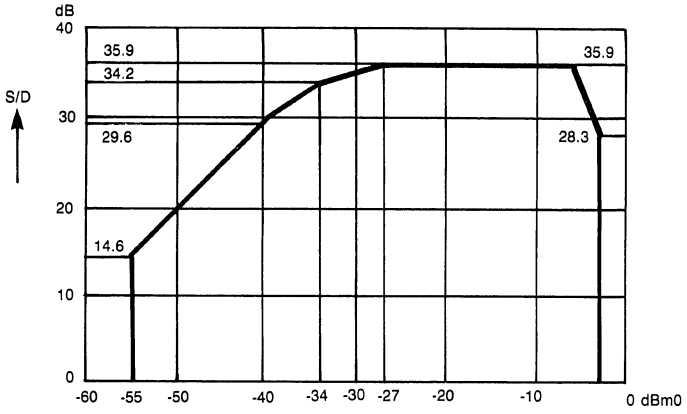
GAIN TRACKING
Measured with noise signal according to CCITT-Recommendation
*Reference level is -1ϕdBmϕ



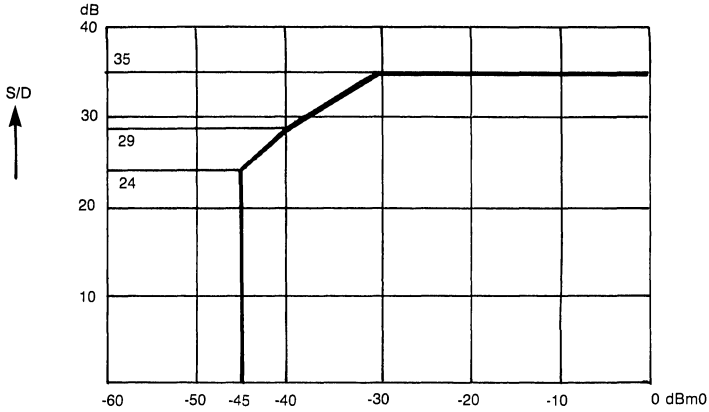
GAIN TRACKING
Measured with sine wave in the range 700-1100Hz
*Reference level is -1ϕdBmϕ

6.8 Total Distortion

The signal-to-total distortion ratio independent of the actual gain adjustment exceeds the limits in the following figures.



SIGNAL-TO-TOTAL DISTORTION
Measured with noise signal



SIGNAL-TO-TOTAL DISTORTION
Measured with sine-wave in the range 700-1100Hz, excluding submultiples of 8kHz

7. Electrical characteristics

7.1 Absolute maximum ratings

Storage temperature	-60 to 125°C
Ambient temperature under Bias	-10 to 80°C
V_{DD} with respect to AGND	-0.3 to 5.5V
V_{SS} with respect to AGND	-5.5 to 0.3V
AGND to DGND	±0.3V
Analog input and output voltage	
with respect to V_{DD}	-11 to +0.3V
with respect to V_{SS}	-0.3 to +11V
All digital input and output voltages	
with respect to DGND	-0.3 to 5.5V
with respect to V_{DD}	-5.5 to 0.3V
Power dissipation	1W

7.2 Operating range

Ambient temperature	0 to 70°C

V_{DD} = 5V ± 5% V_{SS} = 5V ± 5%
DGND = OV AGND = OV

Symbol	Parameter	Min	Typ	Max	Units	Condition
I_{DD}	V_{DD} supply current					
	standby			6	mA	±5% supply
	operating			40	mA	±5% supply
I_{SS}	V_{SS} supply current					
	standby			6	mA	±5% supply
	operating			8	mA	±5% supply
PSRR	Power supply rejection	40			dB	0<f<2MHz 100mVRMS ripple
Pdϕ	standby power dissipation			60	mW	±5% supply
Pd1	operating power dissipation			240	mW	±5% supply

7.3 Digital Interface

Symbol	Parameter	Min	Typ	Max	Units	Condition
I_{IL}	Input leakage current			±10	μA	$-0.3 \leq V_{IN} \leq V_{DD}$
V_{IL}	Input low voltage	-0.3		0.8	V	
V_{IH}	Input high voltage	2		V_{DD} +0.3	V	
V_{OL}	Output low voltage			0.45	V	$I_Q = -2mA$
V_{OH}	Output high voltage	2.4			V	$I_Q = 400\mu A$
C_I	Input capacitance					
C_L	Load capacitance					
R_L	Load resistance					

7.4 Analog Interface

Symbol	Parameter	Min	Typ	Max	Units	Condition
Z_I	Analog input impedance	1			MΩ	
Z_O	Analog output impedance			10	Ω	$-3.2 \leq V_{out} \leq 3.2V$
V_{IOS}	Offset voltage allowed on V_{IN}		±10	±20	mV	
V_{OOS}	Output offset voltage		±50	±100	mV	
V_{IR}	Input voltage range			±3.2	V	
V_{OR}	Output voltage range			±3.2	V	$R_L \geq 10K$
I_O	Output current					$R_L \geq 10K$
C_I	Input capacitance					
C_L	Load capacitance					
R_L	Load resistance					

8. Interface Signals

Name	Pin No.	Description
V_{DD}	1	+ 5V Power Supply
V_{SS}	4	— 5V Power Supply
AGND	3	Analog Ground. Not internally connected to DGND. All analog signals are referenced to this pin.
DGND	5	Digital Ground. Not internally connected to AGND. All digital signals are referenced to this pin.
VIN	22	Analog Voice Input to transmit path.
VOUT	2	Analog Voice Output corresponding to received PCM-data.
SCLK	12	512 kHz Slave Clock. Supplied by PEB 2050 Peripheral Board Controller.
DIR	10	8 kHz Direction Signal. When high, SIP becomes input and SICOFI receives data from PBC. When low, SIP becomes output and data are transferred from SICOFI to PBC.
SIP	17	Serial Interface Port. 512 kHz bi-directional serial data port, clocked by SCLK.
TEST	18	Digital Test-Input. When low, SICOFI is in normal operating condition. When high, SICOFI runs in different testmodes, accepting test-signals at SCLK-, RS-, PLL-, SI-Pins and making available test-results at SO-PINS.
PLL	11	4 MHz Phase-Locked-Loop output *). The PLL-circuit supplies the SICOFIs internal 4 MHz-Master-Clock, derived from the 512 kHz SCLK-input.

*) (Available in testmode only; during normal operating condition, the PLL-output is in a high impedance state).

SI1	19	Transmit Signaling Inputs. Data present at SI_n
SI2	20	are sampled and serially transfered to PBC on SIP
SI3	21	during DIR = Low
SO1	8	Receive Signaling Outputs. Data received serially
SO2	7	on SIP during DIR = High are latched and fed to
SO3	6	to these outputs.
SA	16	Programmable I/O signaling pins. With the appro-
SB	15	priate bits in the control-byte, each of these pins is
SC	14	declared to be input or output individually. If 2
SD	13	SICOFIs are connected to 1 PBC-Port, the input level on SA (High or Low) decides, to which of the SICOFIs voice-, control- and signaling-data are assigned.
RS	9	Reset Input. The external RS-signal forces the SICOFI to power-down mode and additionally resets the configuration registers. SIP remains in a high impendance state until the SICOFI is reconfigured.

PSB 6520
Tone Ringer

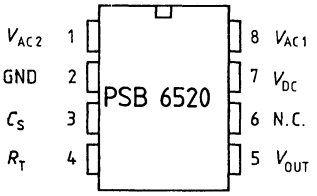
Preliminary data

The PSB 6520 bipolar integrated circuit, in conjunction with an electro-acoustic converter, replaces the mechanical bell in the telephone set **(fig. 1)**. The component generates two periodic switchable tone frequencies that can either drive a piezo-ceramic converter directly, or a loudspeaker.

Special features

- Integrated bridge rectifier allows direct input via call signal (AC voltage)
- Low current consumption (several tone ringers can be connected in parallel)
- High noise immunity due to built-in voltage-current hysteresis
- Direct replacement of the mechanical bell requiring 4 additional external components and an acoustic converter
- Two tone frequencies, switched internally
- Tone and switching frequencies adjustable by means of a resistor and a capacitor
- Overvoltage protection in accordance with VDE 0433 (2 kV–10/700 µs)

Pin configuration top view

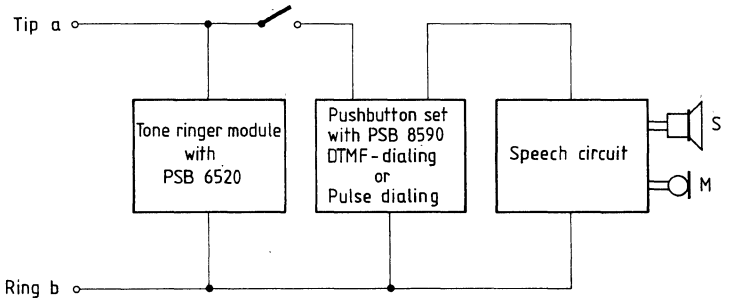


Pin designation

Pin No.	Symbol	Description
1	V_{AC2}	AC voltage input (fig. 3)
2	GND	Ground
3	C_S	Connection for capacitor C_S
4	R_T	Connection for resistor R_T
5	V_{OUT}	Output voltage
6	N.C.	Not connected
7	V_{DC}	Connection for smoothing capacitor 10 µF (internal supply voltage)
8	V_{AC1}	AC voltage input

Fig. 1

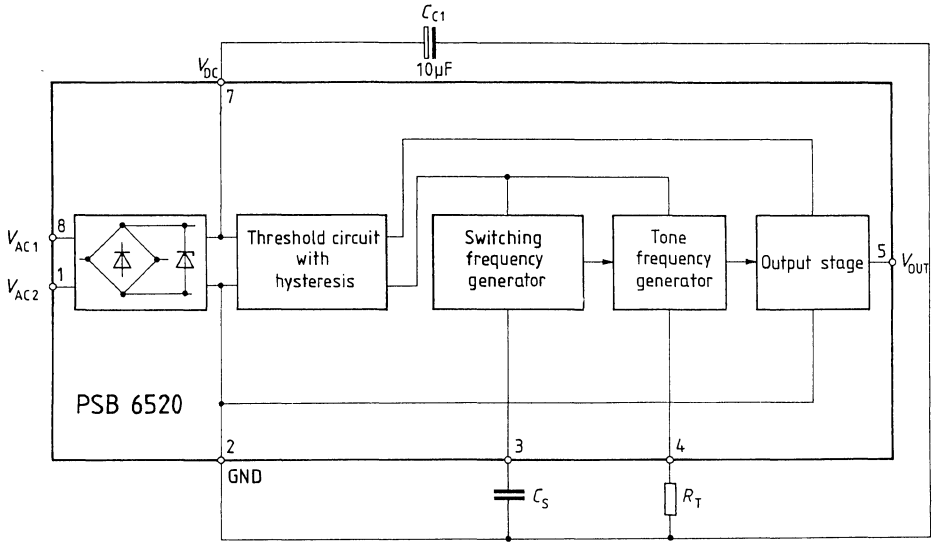
Block diagram of a standard electronic telephone set.
(Push button set and speech circuit connected in series).



Functional description

The tone ringer PSB 6520 is designed for use as an electronic bell in a telephone set. **Fig. 2** shows the block diagram and **fig. 3** the application circuit of the PSB 6520 in the telephone set.

Fig. 2
Block diagram of the PSB 6520 tone ringer.



The IC contains an oscillator which generates a square wave voltage. The frequency of this voltage is periodically switched by a second oscillator back and forth between two basic values having a ratio of 1 : 1.38. The basic frequency f_{1T} is adjusted by the resistor R_T and the switching frequency f_S by the capacitor C_S **(fig. 12 and 13).**

Tone frequencies f_{1T} [Hz] $= \dfrac{2.72 \cdot 10^4}{R\ [k\Omega]} \pm 10\%$

f_{2T} [Hz] $= 0.725 \cdot f_{1T} \pm 2\%$

Switching frequency f_S [Hz] $= \dfrac{750}{C\ (nF)} \pm 15\%$

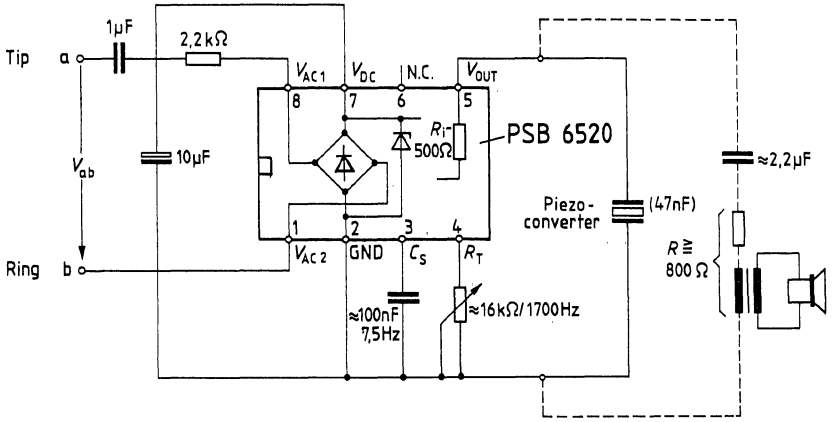
Good frequency stability is achieved by means of internal temperature compensation.

An output stage increases the generated tone voltage and transfers it to a piezo-resonator via an internal resistor. An electro-dynamic converter can be similarly driven, but must be matched to the internal resistance of the output stage **(fig. 6, 7, 8 and 12)** with a transmitter.

An integrated bridge rectifier enables, direct input via the call AC voltage signal (tip (a), ring (b) wires or) via DC voltage (independent of polarity). A DC voltage supply without use of the integrated bridge is possible via the connections 2 and 7. In conjunction with a Z-diode, the bridge rectifier serves simultaneously as an overvoltage protection.

The application circuit shown in **fig. 3** can handle overvoltages occurring due to lightning strikes between terminals a and b according to the VDE 0433 standard, or the occurrence of an AC voltage of 110 V/50 Hz over a period of 30s, thus avoiding the possibility of any damage to the IC. The threshold circuit with high threshold voltage and hysteresis is designed to prevent activation **(fig. 4)** of the IC due to noise pulses.

Fig. 3
PSB 6520 application circuit for telephone sets.



The characteristic curves from **fig. 4** to **fig. 6** show the relation-ship between current consumption, supply voltage, output current, output power, output restistance and AC calling voltage.

Maximum ratings[1]		Test conditions	Min.	Max.	Unit
Supply voltage	V_{DC}	10 ms		28	V
Voltage pin 3 to pin 2	$V_{3,2}$			5.5	V
Voltage pin 4 to pin 2	$V_{4,2}$			7	V
Noise current into the output	$I_{N\ OUT}$	30 µs/mark to space ratio 1 : 100		20	mA
Storage temperature	T_{stg}		−40	125	°C
Operating range					
Calling voltage	V_{ab}	f = 50 Hz Test circuit **fig. 3** Continous operation		90	V_{rms}
		5 s operation/ 10 s pause		110	V_{rms}
Supply voltage	I_{-}	DC supply current		22	mA
Tone frequency	f_{1T}	Validity of the formula f_{1T}	0.1	15	kHz
Ambient temperature	T_{amb}		−20	70	°C

DC characteristics		Test conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DC}	−20°C to 70°C			26	V
Current consumption without load	I_{DC}	V_S = 8.8 V to 26 V, 25°C		1.5	1.8	mA
Hysteresis circuit						
Threshold voltage	V_{th}	−20°C to 70°C	12.2	12.6	13.0	V
Switch-OFF voltage	V_{OFF}	−20°C to 70°C	8.0	8.4	8.8	V
Initial resistance	R_{INI}	25°C	6.4	7.4	8.5	KΩ
Voltage[2] deviation at output pin 5 referenced to pin 2	V_{OUT}	25°C		V_S−3		V
Short circuit current	I_{OUT}	U_5 = 20 V, 25°C		35		mA
Tone frequency temperature coefficient	TC	−20°C to 70°C		$8 \cdot 10^{-4}$		K^{-1}

[1]) Maximum ratings are absolute limits and the IC can be destroyed by exceeding them. Functioning of the integrated circuit is not assured under conditions other than those stated in the electrical characteristics. Operation for long periods of time under maximum rating conditions can adversely affect the reliability of the integrated circuit.

[2]) An internal resistor of 500 Ω is connected before the output.

Characteristic curves

Fig. 4
Dependence of current consumtion on the supply voltage V_{DC} without output load

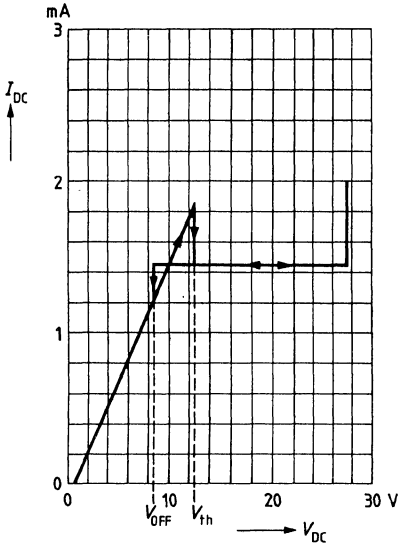


Fig. 5
Dependence of amplitude of output current on the supply voltage V_{DC} in the case of short-circuit

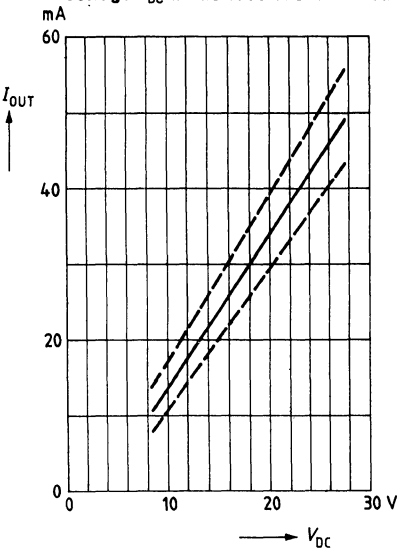


Fig. 6
Dependence of output power on the load resistance R_{OUT} (ohmic)

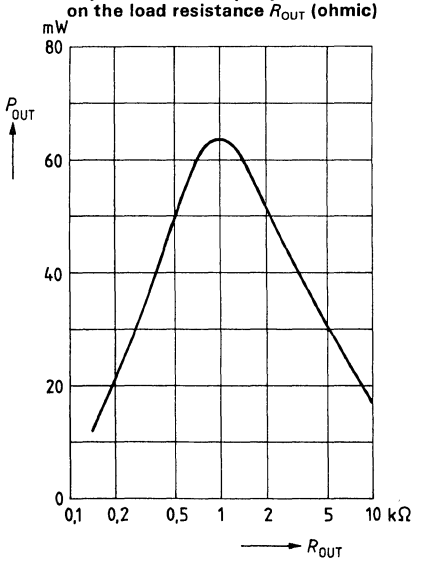


Fig. 6.1
Test circuit to determine output power at different load resistances

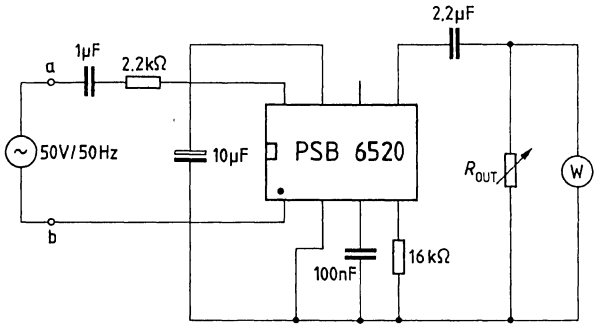


Fig. 7
Test circuit to determine output power for variable call voltage V_{ab}

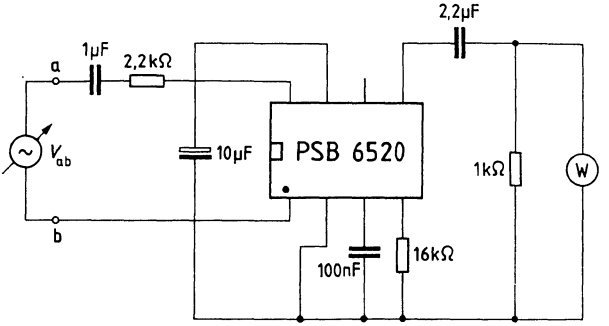


Fig. 7.1
Dependence of output power on the call voltage for power matching

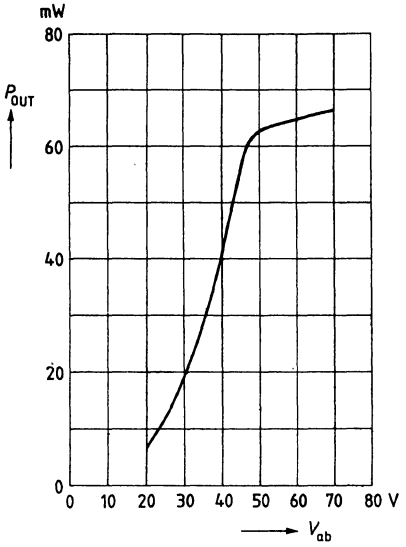
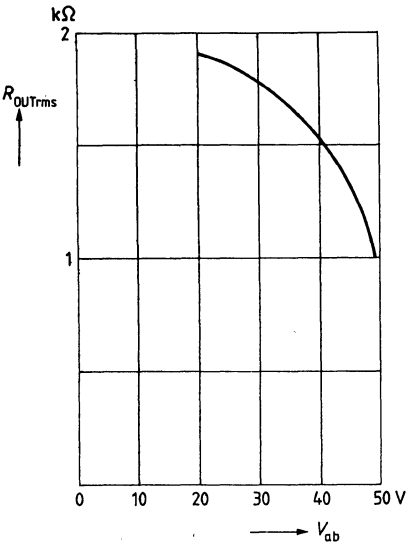
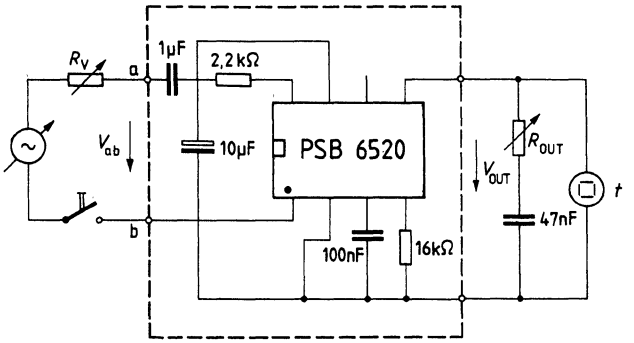


Fig. 8
Dependence of effective output resistance on the call voltage V_{ab}



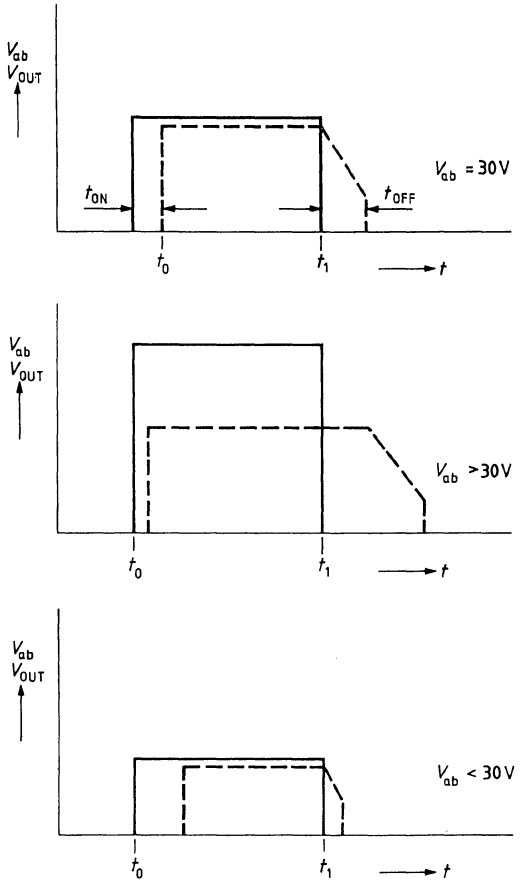
Delay times

Fig. 9
Test circuit to determine delay times



Delay times

Fig. 9.1
Dependence of delay times t_{ON}, t_{OFF} on V_{ab}



——— Effective value of input signal (call voltage V_{ab})
- - - - - - - - - - Effektive value of output signal (output voltage V_{OUT})
$t_1 - t_0$ Time duration of applied call voltage V_{ab}

Fig. 10
Dependence of switch-on delay time t_{ON} on V_{ab} (independent of R_{OUT})

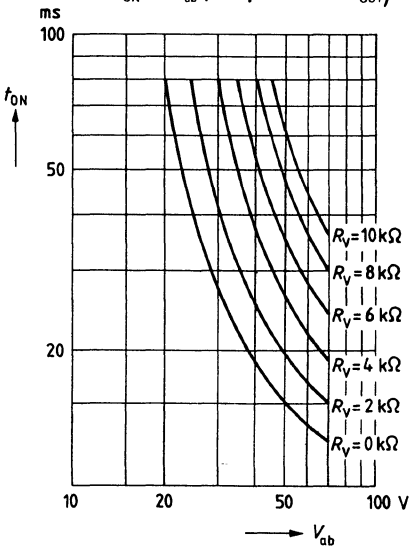


Fig. 11
Dependence of switch-off delay time t_{OFF} on V_{ab} (independent of R_V)

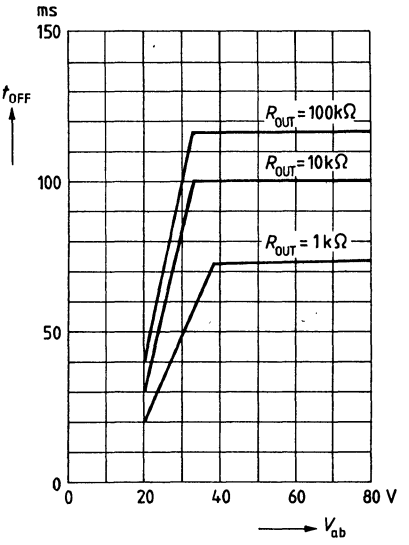


Fig. 12
Dependence of the frequencies f_{1T} and f_{2T} on the resistor R_T.

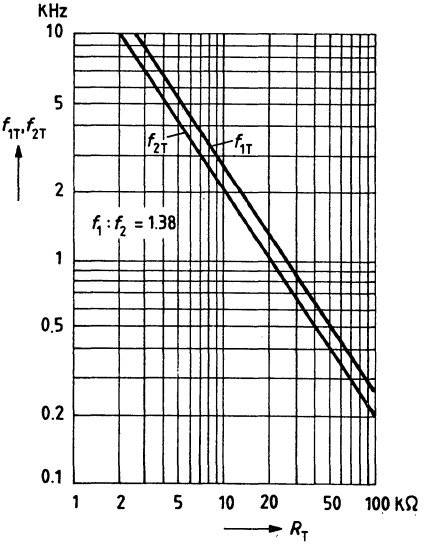
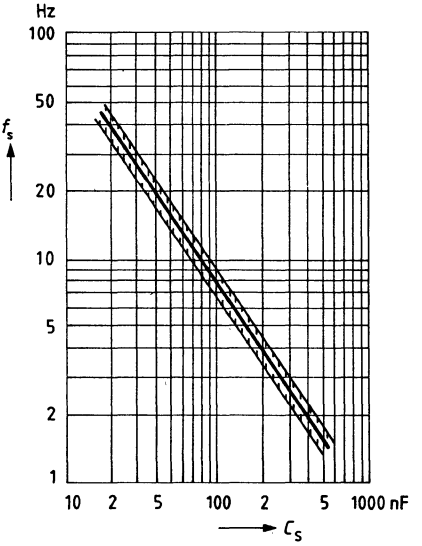
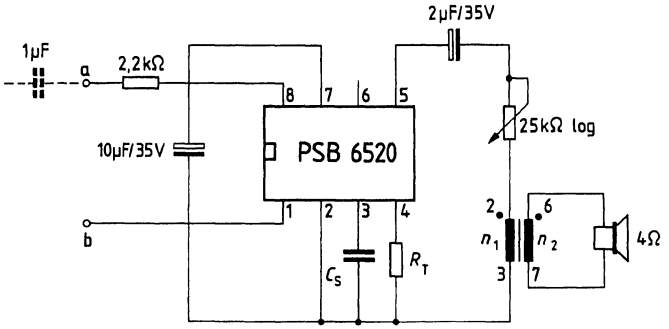


Fig. 13
Dependence of switching frequency on the capacitor C_S



Recommended circuitry of PSB 6520 with a small loudspeaker

Fig. 14
Matching a 4 Ω loudspeaker to the PSB 6520



Transformer

Pot core: (18 x 11)	Ordering code B65651–K0000–R030
Material:	N30, A_L = 5600 nH/W^2
Bobbin:	Ordering code B65652–B0000–T001
Windings:	n_1 = 800, d_1 = 0.08 mm CuL n_2 = 50, d_2 = 0.4 mm CuL

PSB 6521
Tone Ringer

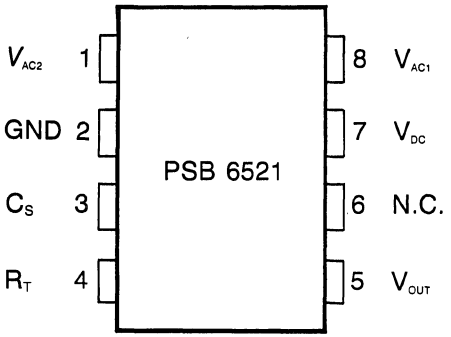
Preliminary Data

The PSB 6521 bipolar integrated circuit, in conjunction with an electro-acoustic converter, replaces the mechanical bell in the telephone set (Fig. 1). The component generates two periodic switchable tone frequencies that can either drive a piezo-ceramic converter directly, or a loudspeaker.

Special features

- Integrated bridge rectifier allows direct input via call signal (ac voltage)
- Low current consumption (several tone ringers can be connected in parallel)
- High noise immunity due to built-in voltage-current hysteresis
- Direct replacement of the mechanical bell requiring 4 additional external components and an acoustic converter
- Two tone frequencies, switched internally
- Tone and switching frequencies adjustable by means of a resistor and a capacitor
- Overvoltage protection in accordance with VDE 0433 (2kV - 1o/700μs)

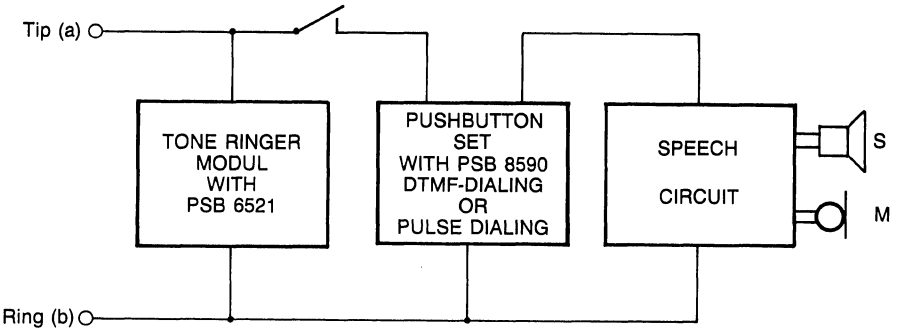
Pin configuration



Pin designation

Pin No.	Name	Function
1	V_{AC2}	AC voltage input (Fig. 3)
2	GND	Ground
3	C_S	Connection for capacitor C_S
4	R_T	Connection for resistor R_T
5	V_{OUT}	Output voltage
6	N.C.	Not connected
7	V_{DC}	Connection for smoothing capacitor 1oμF (internal supply voltage)
8	V_{AC1}	AC voltage input

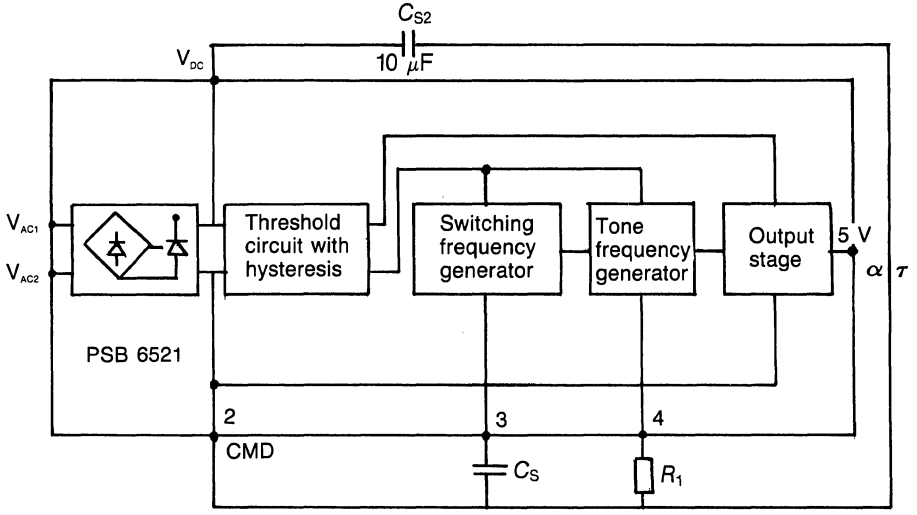
Fig. 1
Block diagram of a standard electronic telephone set (Push button set and speech circuit connected in series)



Functional description

The tone ringer PSB 6521 is designed for use as an electronic bell in a telephone set. Fig. 2 shows the block diagram and Fig. 3 the application circuit of the PSB 6521 in the telephone set.

Fig. 2.
Block diagram of the PSB 6521 tone ringer.



The IC contains an oscillator which generates a square wave voltage. The frequency of this voltage is periodically switched by a second oscillator back and forth between two basic values having a ratio of 1 : 1.25. The basci frequency f_{1T} is adjusted by the resistor R_T and the switching frequency f_S by the capacitor C_S (Figs. 12 and 13).

Tone frequencies	f_{1T} [Hz] =	$\frac{1{,}93 \cdot 10^4}{R\ [k\Omega]}$	± 15%
	f_{2T} [Hz] =	$0{,}8 \cdot f_{1T}$	± 2%
Switching frequency	f_S [Hz] =	$\frac{750}{C(nF)}$	± 15%

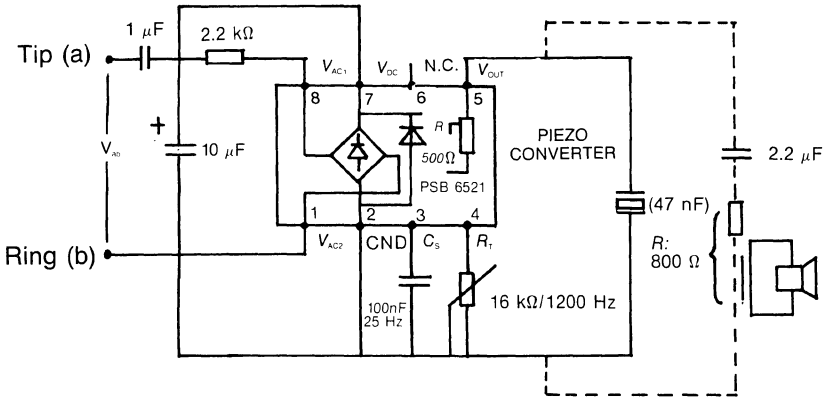
Good frequency stability is achieved by means of internal temperature compensation.

An output stage increases the generated tone voltage and transfers it to a piezo-resonator via an internal resistor. An electro-dynamic converter can be similarly driven, but must be matched to the internal resistance of the output stage (Figs. 6,7,8 and 12) with a transmitter.

An integrated bridge rectifier enables direct input via the call a.c. voltage signal (tip (a), ring (b) wires or via d.c. voltage (independent of polarity)). A d.c. voltage supply without use of the integrated bridge is possible via the connections 2 and 7. In conjunction with a Zener diode, the bridge rectifier serves simultaneously as an overvoltage protection.

The application circuit shown in figure 3 can handle overvoltages occurring due to lightning strikes between terminals a and b according to the VDE 0433 norm, or the ocurrence of an a.c. voltage of 110V/50Hz over a period of 30s, thus avoiding the possibility of any damage to the IC. The threshold circuit with high threshold voltage and hysteresis is designed to prevent activation (Fig. 4) of the IC due to noise pulses.

Fig. 3 PSB 6521 application circuit for telephone sets.



The characteristic curves from fig. 4 to fig. 6 show the relationship between current consumption, supply voltage, output current, output power, output resistance and a.c. calling voltage.

Maximum ratings [1]

		Test condition	Min.	Max.	Unit
Supply voltage	V_{DC}	10ms		28	V
Voltage pin 3 to pin 2	V_{32}			5.5	V
Voltage in 4 to pin 2	V_{42}			7	V
Noise current into the output	I_{NOUT}	30Ωs/mark to space ration 1 : 100		20	mA
Storage temperature	T_{stg}		-40	125	°C

[1] Maximum ratings are absolute values and the IC can be damaged by exceeding them. Functioning of the integrated circuit is not assured under conditions other than those stated in the electrical characteristics. Operation for long periods of time under maximum rating conditions can adversely affect the reliability of the integrated circuit.

Operating range

		Test condition	Min.	Max.	Unit
Calling voltage	V_{ab}	f = 50 Hz Test circuit Figure 3			
		Continuous operation		90	V_{rms}
		5 sec operation/ 10 sec pause		110	V_{rms}
Supply voltage	$I_{=}$	DC supply current		22	mA
Tone frequency	f_{1T}	Validity of the formula f_{1T}	0.1	10	kHz
Ambient temperature	T_{amb}		-20	70	°C

D.C. characteristics

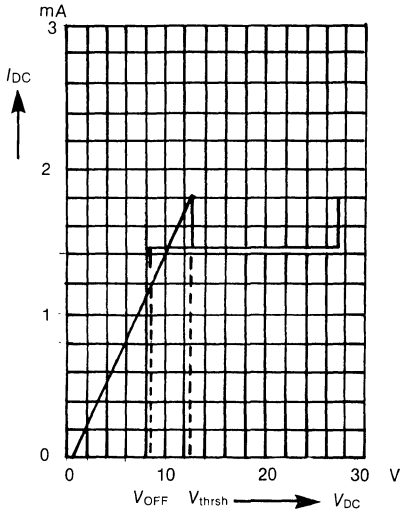
		Test condition	Min.	Typ.	Max.	Unit
Supply	V_{DC}	-20°C to 70°C			26	V
Current consumption tion without load	I_{DC}	V_S = 8.8V to 26V, 25°C		1.5	1.8	mA
Hysteresis circuit						
Threshold voltage	V_{thrsh}	-20° to 70°C	12.2	12.6	13.0	V
Switch-off voltage	V_{off}	-20°C to 70°C	8.0	8.4	8.8	V
Initial resistance	R_{INI}	25°C	6.4	7.4	8.5	KΩ
Voltage* deviation at output Pin 5 referenced to pin 2	V_{OUT}	25°C		V_S-3		V
Short circuit current	I_{OUT}	U_5 = 20V, 25°C		35		mA
Tone frequency temperature coefficient	TC	-20°C to 70°C		$8 \cdot 10^{-4}$		K^{-1}

*An internal resistor of 500Ω is connected before the output

Characteristic Curves

Fig. 4

Dependence of current consumption on the supply voltage V_{DC} without output load.



Fig,. 5

Dependence of amplitude of output current on the supply voltage V_{DC} in the case of short circuit.

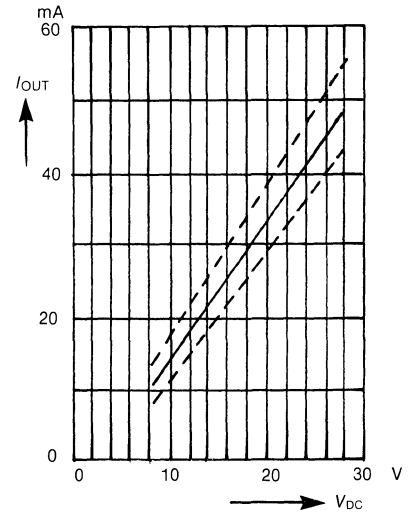


Fig. 6
Dependence of output power on the load resistance R_{out} (ohmic)

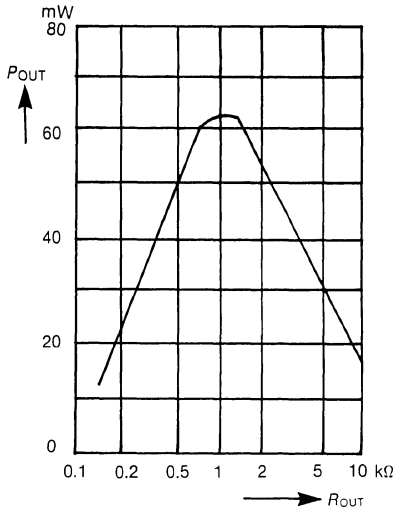


Fig. 6.1
Test circuit to determine output power at different load resistances

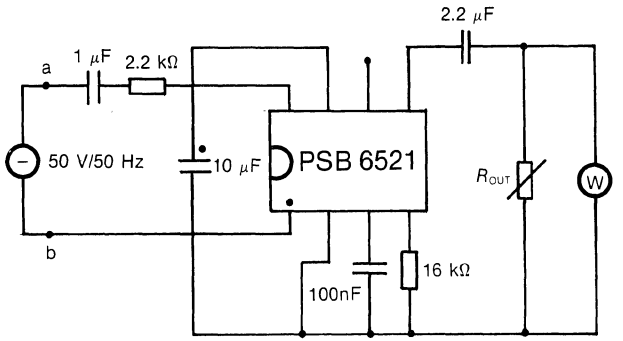


Fig. 7
Dependence of output power on the call voltage for power matching

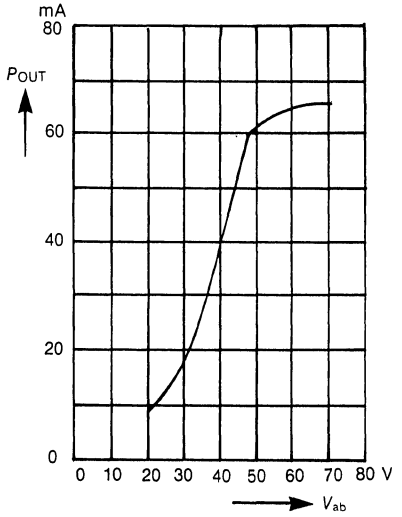


Fig. 7.1
Test circuit to determine output power for variable call voltage V_{ab}

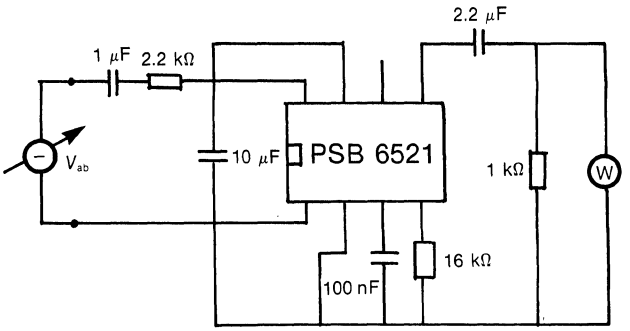
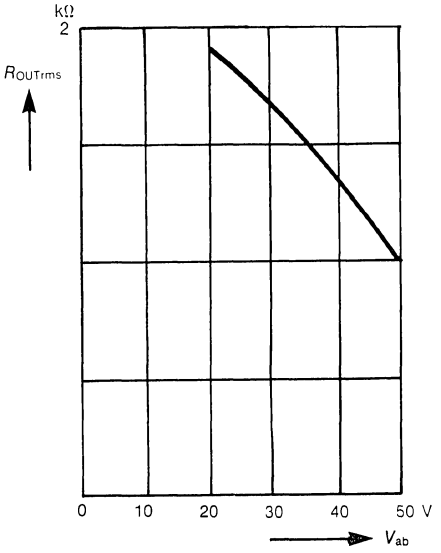


Fig. 8
Dependence of effective output resistance on the call voltage V_{ab}



Delay times

Fig. 9
Test circuit to determine delay times

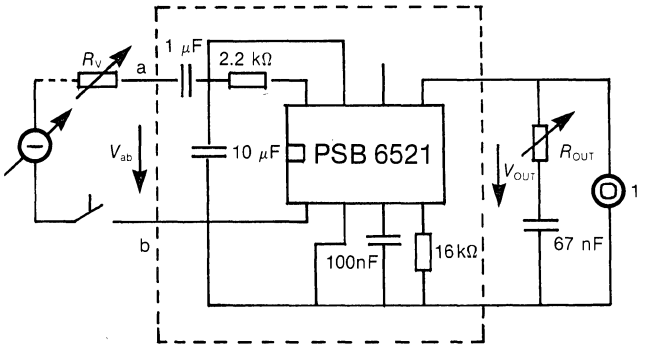
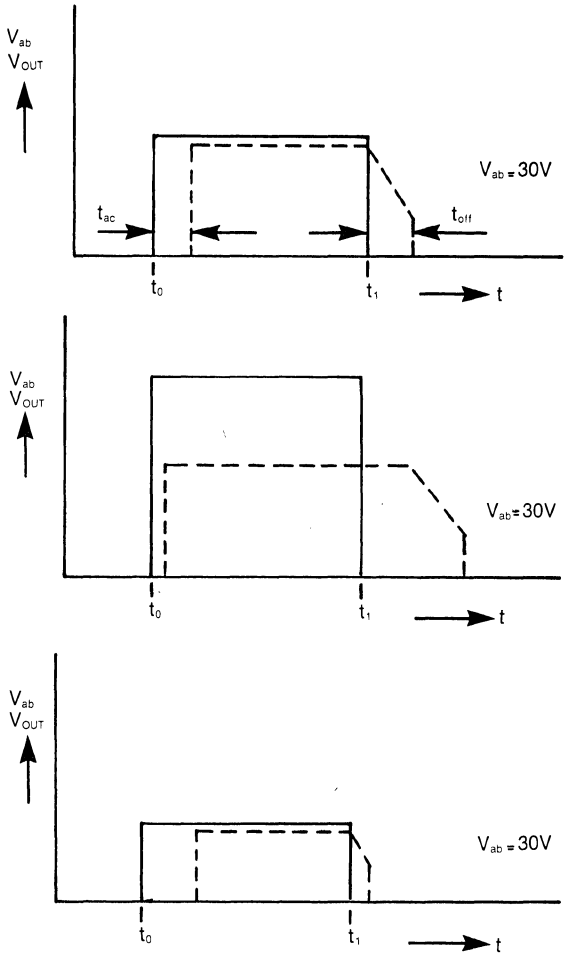


Fig. 9.1
Dependence of delay times t_{on}, t_{off} on V_{ab}



_____ Effective value of input signal (Call voltage V_{ab})

— — — Effective value of output signal (Output voltage V_{OUT})

$t_1 - t_0$ Time duration of applied call voltage V_{ab}

Fig. 10
Dependence of switch-on delay time t_{on} on V_{ab} (independent of R_{OUT})

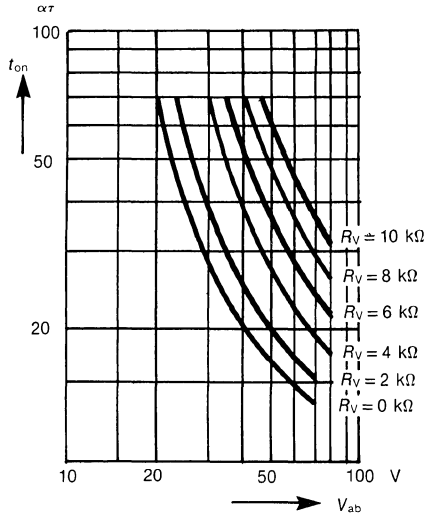


Fig. 11
Dependence of switch-off delay time t_{off} on V_{ab} (independent of R_V)

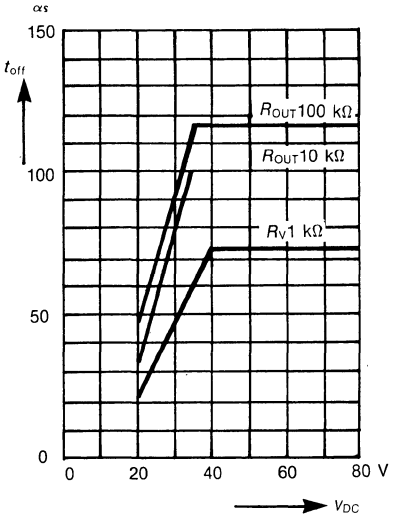


Fig. 12
Dependence of the frequencies f_{1T} and f_{2T} on the resistor R_T.

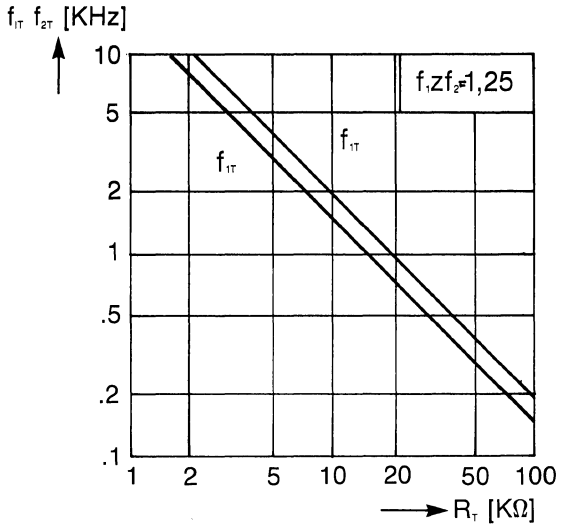
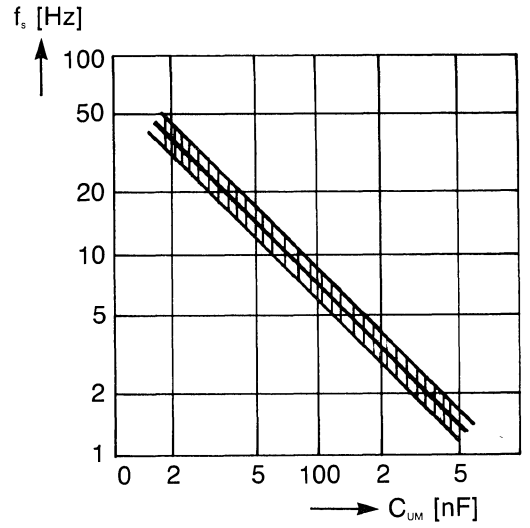
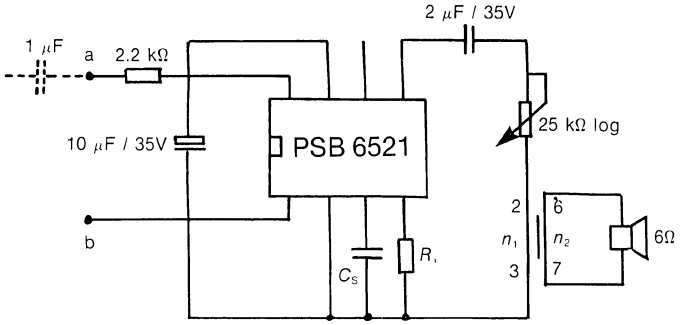


Fig. 13
Dependence of switching frequency on the capacitor C_{UM}



Recommended circuitry of PSB 6521 with a small loudspeaker

Fig. 14
Matching a 4Ω loudspeaker to the PSB 6521



Transformer

Pot core (18 x 11)	: Siemens Ordering code: B65651-KOOOO-Ro3O
Material	: N30, A_L = 5600 nH/W²
Bobbin	: Siemens Ordering code B65652-BOOOO-TOO1
Windings	: N_1 = 800, d_1 = 0.08mm C_{u1}
	N_2 = 50, d_2 = 0.4mm C_{u1}

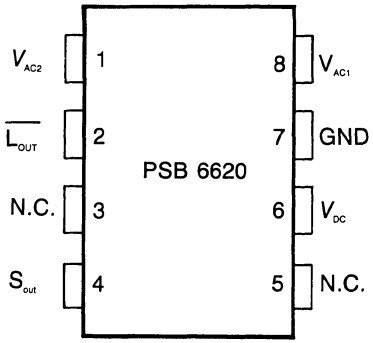
PSB 6620
Ringing Detector

Preliminary data

Features:

- Integrated bridge rectifier allows direct connection to an AC voltage (e.g. a telephone call signal)
- Low current consumption
- High "tapping" (noise) immunity
- Built-in hysteresis for stable operation
- Only three external components necessary
- Regulated 5V output voltage
- Logical TTL/CMOS output signal (open collector)
- Overvoltage protection in accordance with VDE 0433 (2kV-10/700μs)
- Pincompatible with TCM 1520 (Texas Instruments)

Pin configuration



Pin description

Pin No.	Symbol	Description
1	V_{AC2}	AC voltage input
2	$\overline{L_{out}}$	Logical TTL output (low active)
3	N.C.	not connected
4	S_{out}	5V supply-voltage output
5	N.C.	not connected
6	V_{DC}	DC supply voltage input
7	GND	ground
8	V_{AC1}	AC voltage input

AG 10/84

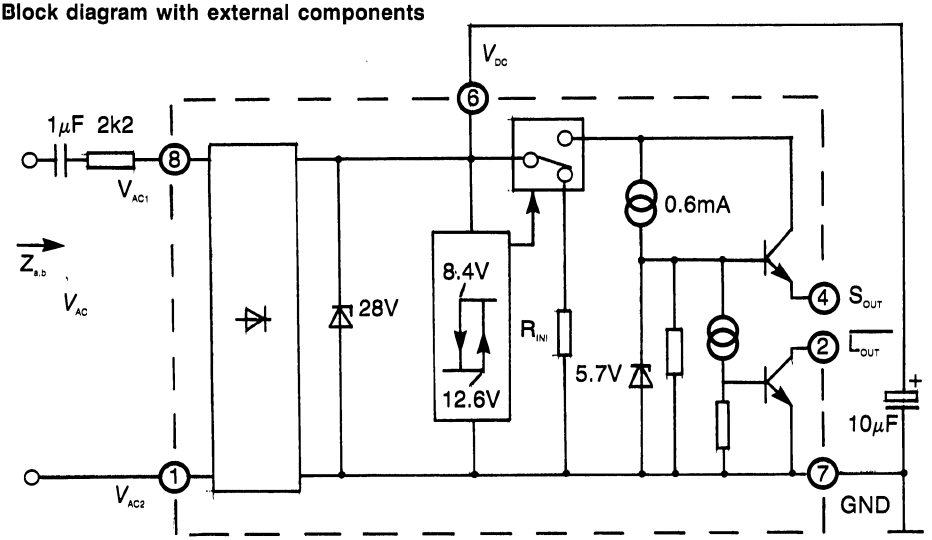
General description

The integrated circuit PSB 6620 is designed to detect a telephone call signal (AC voltage).

The supply voltage of the IC is divided from the AC-input-voltage (call signal). During the active state of the device a regulated 5V DC-voltage and a TTL/CMOS-logic level is available at the outputs. The high threshold activation voltage provides a good immunity against noise (e.g. dialing signals, charge indicator) and a built-in voltage hysteresis guarantees the stable operation.

The regulated 5V voltage (pin 4) of the PSB 6620 allows to supply other devices. The PSB 6620 is not limited to telephone applications. For example the device can be used to build up an inexpensive AC-voltage detector.

Block diagram with external components



Electrical characteristics

Maximum ratings [1]

		Test condition	Min.	Max.	Unit
Supply voltage (pin1 to pin8)	$V_{AC\ peak}$			28	V
Voltage pin 6 to pin 7	V_{DC}			26	V
Output current	$I_{N\ OUT}$			20	mA
Input current AC	I_I	Pin 1-8		30	mA
Pulse current AC	I_p	pulse = 100µs pause = 30s		1	A
Total power consumption	P_{tot}			1	W
Operating ambient temperature	T_{op}		-20	70	°C
Storage ambient temperature	T_{stg}		-75	150	°C

Operating characteristics (T_{amb} = 20°C to 70°C)

		Test conditions	Min.	Typ	Max.	Unit
Supply voltage	V_{DC}				26	V
Current consumption without load	I_{DC}	V_{DC} = 25V	0,4	0,6	0,85	mA
Supply output voltage	V_{Sout}	I_{Sout} = 4mA, T = 25°	4,5	5	5,5	V
Supply output current	I_{SOUT}	R_L = 500Ω	8	10		mA
Logical output voltage (pin 2 to pin 7)	V_{LOUT}	V_{LOUT} = L, I_{LOUT} = 5mA		0,25	0,7	V
Max. voltage on the logical output	$V_{Loutmax}$	V_{Lout} = H, $I_{Lout} \leq$ 1mA			35	V
Logic output current	I_{Lout}	V_{Lout} = 1V	10			mA
Temperature coefficient from						
Supply output voltage	TC_{VS}	I_{Sout} = -5mA		+9		mV/K
Logical output Voltage	TC_{VL}	I_{Lout} = 10mA		+0,3		mV/K

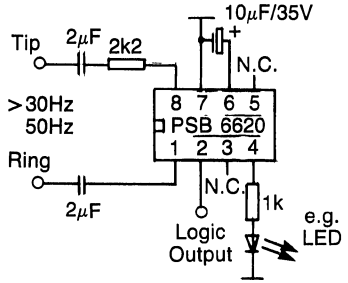
Hysteresis circuit (pin 6 to pin 7)

		Test conditions	Min	Typ	Max	Unit
Threshold voltage	V_{th}		12,2	12,6	13,2	V
Switch-OFF voltage	V_{off}		8	8,4	8,8	V
Initial resistance	R_{INI}			7,4		kΩ
Input impedance (cf. block diagram)	$Z_{a,b}$	f ≤ 20kHz, V_{AC} = 1,3, V_{rms}	100			kΩ

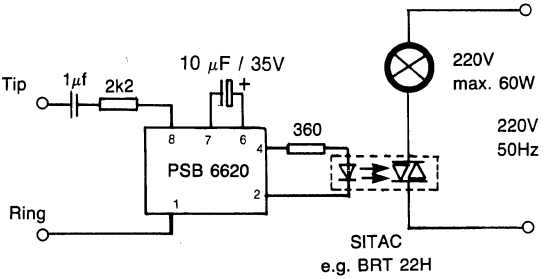
[1] Maximum ratings are absolute values and the IC can be damaged by exceeding them. Functioning of the integrated circuit is not assure under conditions other than those stated in the electrical characteristics. Operating for long periods of time under maximum rating conditions can adversely affect the reliability of the integrated circuits.

Application examples:

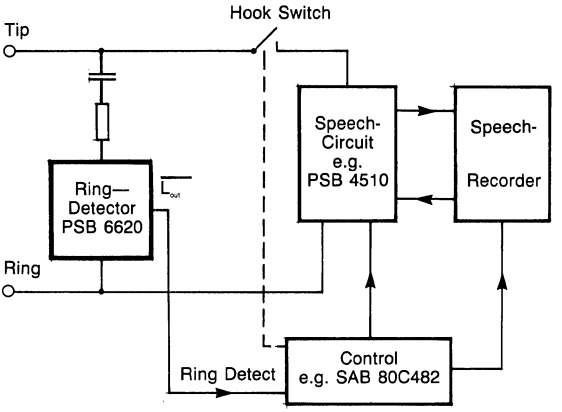
a) Call Signal Indicator



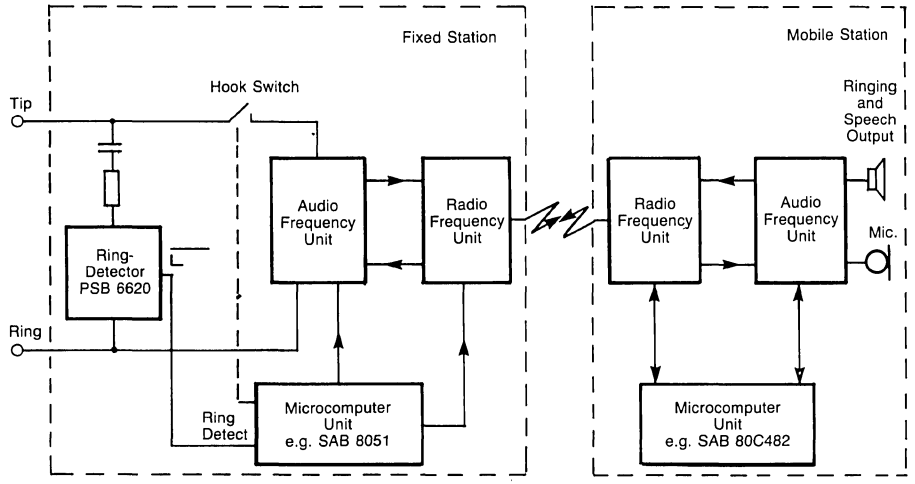
b) Optical Call Signal Indicator



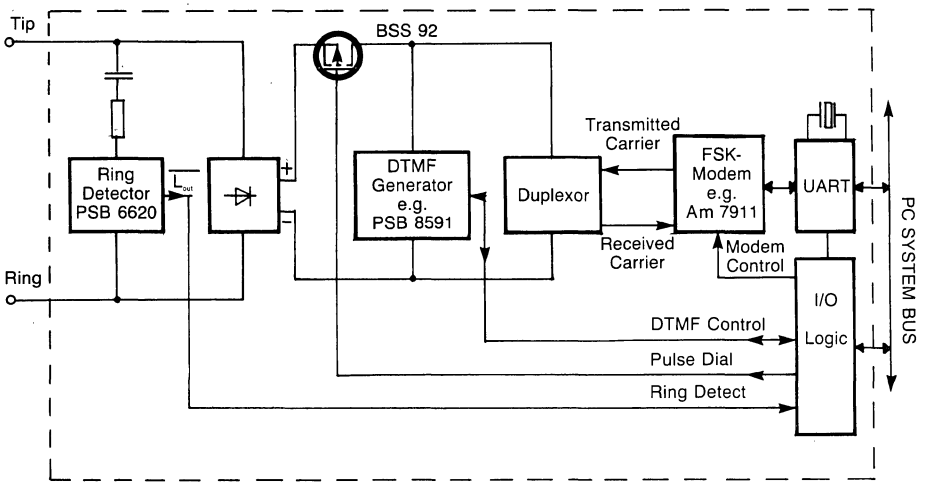
c) Automatic Telephone Answering System



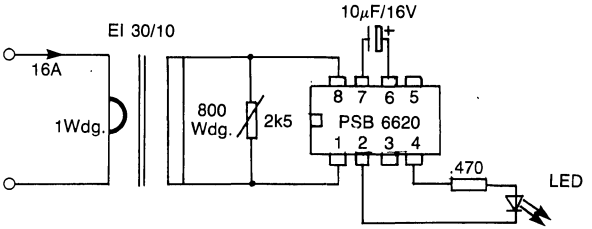
d) Cordless Telephone



e) Bilingual Telephone Interface for Personal Computer



f) AC - Current Indicator



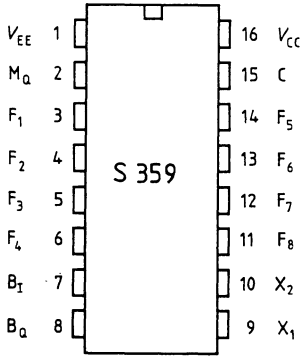
PSB 8590
Dual Tone Multifrequency Generator

Preliminary data

Features

- CEPT-compatible
- Direct line feeding
- High frequency accuracy (deviation less than 0.4%)
- Standard low cost clock crystal 4.19 MHz
- Operation with either single contact or 2 – of – 8 keypads
- Dual tone as well as single tone capability
- Multi-key lockout and debouncing
- Binary interface mode
- Power dissipation limited by internal thermal overload protection

Pin configuration

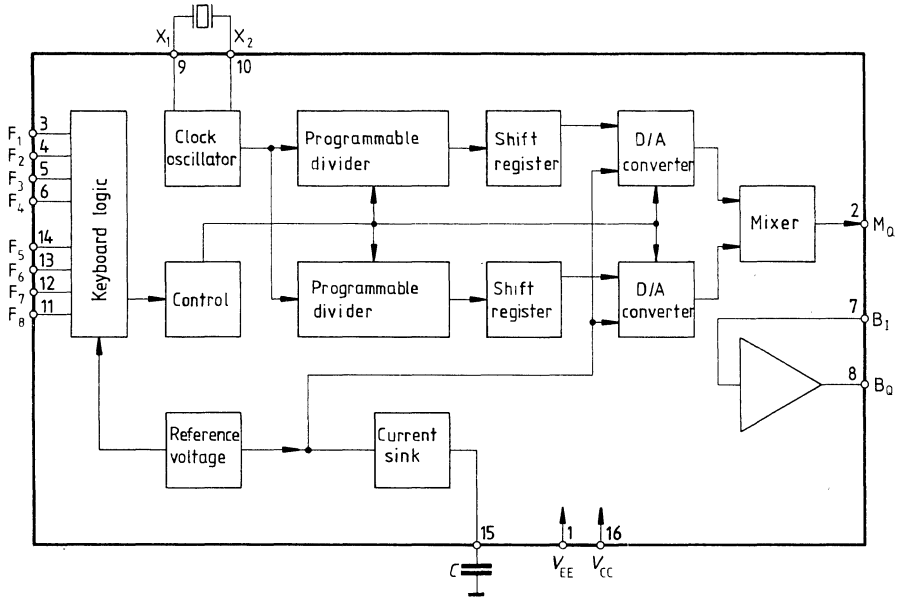


General description

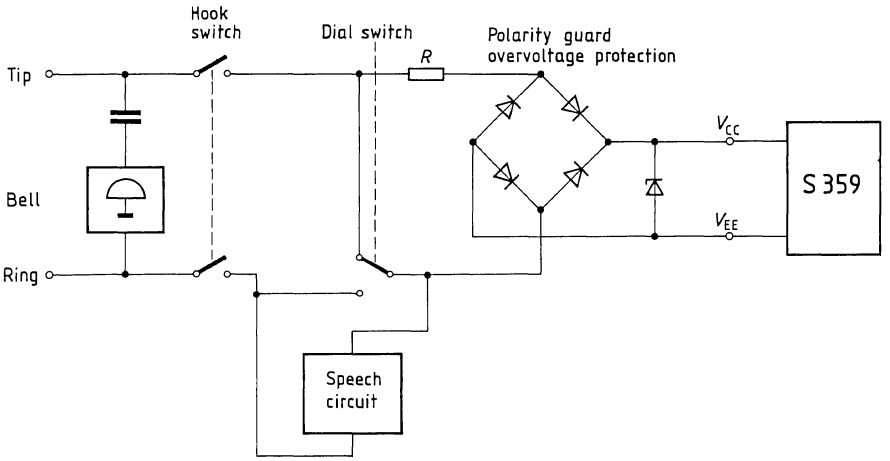
The DTMF generator S 359 is a monolithic IC using the I^2L technology. It provides all dual tone multi frequency (DTMF) pairs required in tone dialing systems. The eight different audio output frequencies are generated from an on-chip reference oscillator with an external low cost clock crystal 4.19 MHz. The internal temperature compensated voltage reference determines the audio output levels and it also controls the on-chip shunt regulator which provides the adaptation to different feeding conditions. In order to meet the CEPT recommendations an external 2-pole RC filter can easily be connected.

The S 359 can interface directly to a single contact keypad. Furthermore, open collector outputs can control the S 359 either in a BCD-mode or in a 2-of-8 keypad mode.

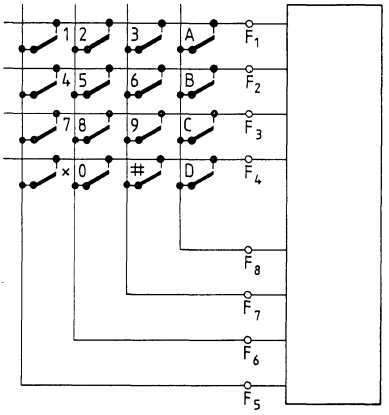
Block diagram



Connection to line



Connection to keyboard



The keys are debounced and electronically interlocked. If more than one key is pressed simultaneously, the key recognized as pressed first will be evaluated.

The requirements for the quality of contacts are:

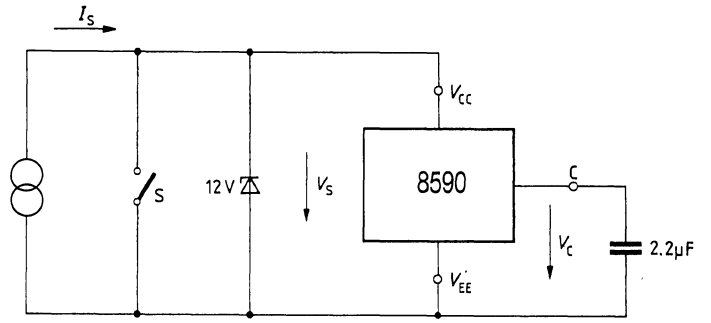
Open contact: Resistance $R_N > 50$ kΩ
Closed contact: Contact resistance $R_E \leqq 1$ kΩ for $I = 100$ µA

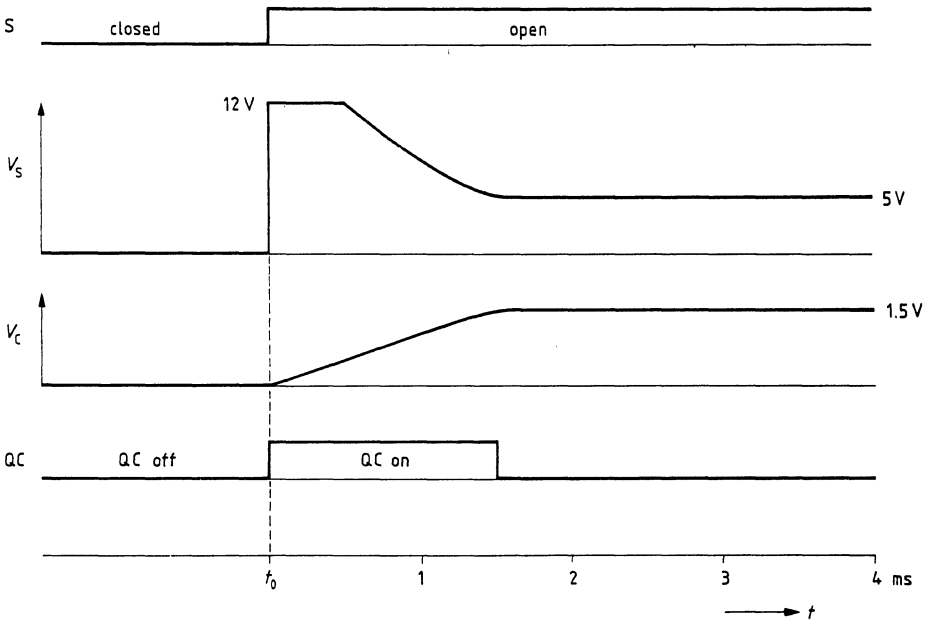
Functional description

1. Line adaption

The DTMF generator has an internal temperature-compensated voltage reference. This reference voltage controls a shunt regulator which sets the DC voltage $V_S = V_{CC} - V_{EE}$ to 5 V. The external filtering capacitor C gives the shunt regulator for frequencies above 300 Hz the behavior of a high impedance current sink. The shunt regulator includes a start-up circuit for the quick charging of the filtering capacitor (Fig. 1) The shunt regulator can sink feeding currents up to 120 mA while the power dissipation is limited by internal thermal overload protection. If the chip temperature exceeds a preset value ($\approx T_j = 150\,°C$, $P_V \approx 1\,W$), the filtering capacitor is discharged, the shunt regulator is switched of and the voltage V_S rises to the breakdown voltage of the external overvoltage protection network (Fig. 2).

Figure 1
Tuning diagram of the quick charging circuit (QC) for the filter capacitor

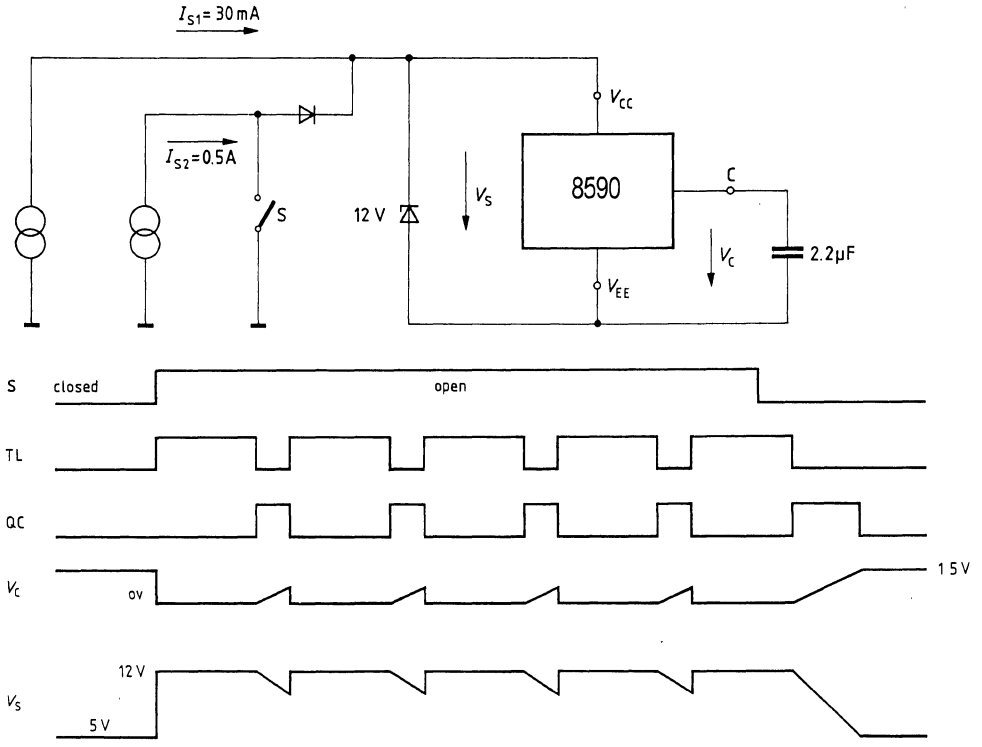




The control circuitry for the quick charging circuit has hysteresis with the following thresholds

QC	V_S	V_C
on	X	< 0.7 V
on	> 9 V	X
off	< 6.5 V	> 0.7 V

Figure 2
Output waveforms V_S during thermal limitation (TL) of the power dissipation



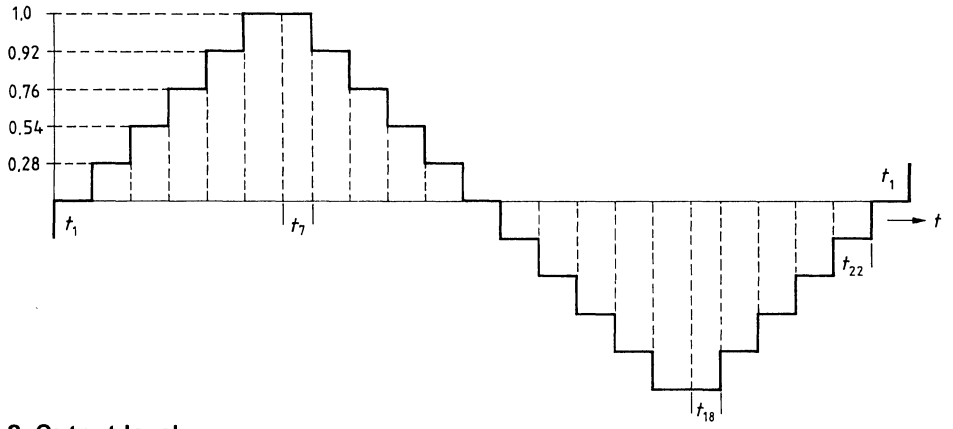
The thermal limitation (TL) overrides the quick charger (QC).

2. Tone generation

The on-chip oscillator generates together with the external clock crystal the master clock frequency f_{C1} = 4.194.304 MHz. This master clock f_{C1} is scaled by a factor of 16 to f_{C2} = 262.144 kHz. The programmable dividers for the higher ($f_5 - f_8$) and lower ($f_1 - f_4$) frequency tone groups are driven by the clock f_{C2}. The programmable dividers generate the clock for the 6 bit *L/R* shift register. Each shift register controls one D/A converter and the polarity of its output waveform. The output sinewave is synthesized as a stairstep-function with 11 voltage levels. The output waveform has 22 time segments (Fig. 3). The time segments t_1 to t_6, t_8 to t_{17} and t_{19} to t_{22} are equal. The time segments t_7 and t_{18} are equal but slightly different from the others in order to meet

the required output frequencies as closely as possible. The output waveforms are symmetrical; therefore, no even harmonics exist. The stairstep function with 11 voltage levels is calculated such that, theoretically, the lowest order harmonics are the 21st and the 23rd. Because of the different length of time segments t_7 and t_{18} and the tolerances of the D/A converter, lower odd harmonics exist.

Figure 3
Synthesized output waveforms



3. Output levels

Each D/A converter generates a five-level stairstep function. The mixer alternately reverses the polarity of the five-level stairstep function which leads to the symmetrical 11-level stairstep function (Fig. 3). Furthermore, the mixer adds the stairstep function of the lower and of the higher frequency groups.

The nominal amplitudes of the stairstep function at the mixer output are:

Lower frequency group $i_{ML} = 42.5\ \mu A$
Higher frequency group $i_{MH} = 53.5\ \mu A$

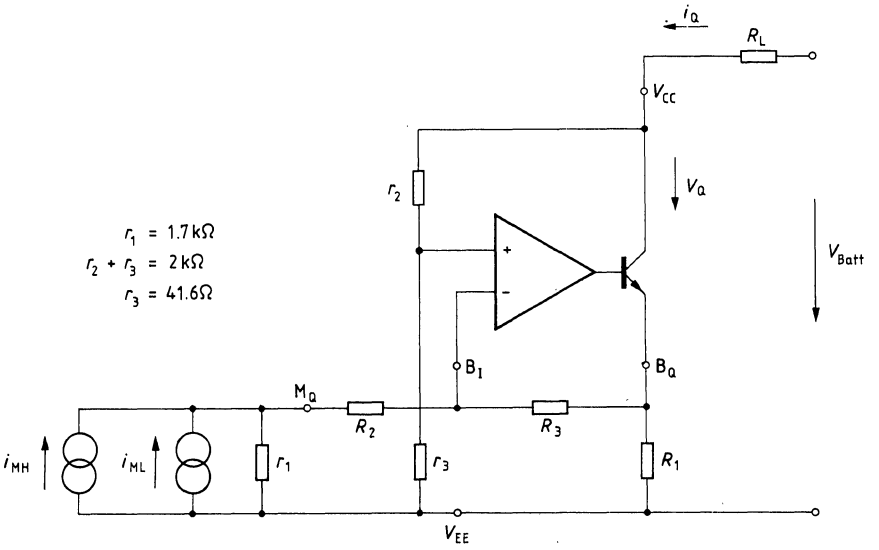
Figure 4 shows the AC-schematic of the output section of the S 359. The feedback loop of the output amplifier is externally arranged. The resistors R_1 to R_3 determine the output level (V_{QL} and V_{QH}) and the output impedance R_Q, as shown below.

$$R_Q = \frac{R_1(r_2+r_3)}{R_1+r_3\left(1+\frac{R_3+R_1}{R_2+r_1}\right)}$$

$$V_{QL,H} = i_{ML,H} \cdot \frac{(R_3+R_1)R_L \cdot r_1}{R_1(R_2+r_1)} \cdot \frac{R_Q}{R_Q+R_L}$$

The ratio of the resistors R_3/R_2 is restricted to the range $R_3/R_2 < 1.2$, otherwise the output amplitudes are clipped. Normally, the resistors R_2 and R_3 are equal. Fig. 8 shows the sum level P_S and the output impedance R_Q as a function of R_1 and R_2.

Figure 4
AC schematic of the output stage



An external *RC* filter network is necessary in order to meet the CEPT recommendation concerning distortion and harmonics. The *RC* filter is easy to implement, because the pins M_Q, B_I, B_Q of the output amplifier are accessible. The 8590 is shown in Fig. 5 with a one-pole *RC*filter for application corresponding to the recommendations of the DBP and in Fig. 6 witha two-pole *RC* filter for CEPT applications. Fig. 7 shows the output spectrum for the most critical case, the frequency f_S.

The nominal output levels $P_{L,H}$ are identical for the arrangement in Fig. 5 and Fig. 6, they are

$$P_L = 20 \log \frac{V_{QL}}{\sqrt{2}\ \sqrt{1\,mW \cdot 600\,\Omega}} = -8.12\ dBm$$

$$P_H = 20 \log \frac{V_{QH}}{\sqrt{2}\ \sqrt{1\,mW \cdot 600\,\Omega}} = -6.12\ dBm$$

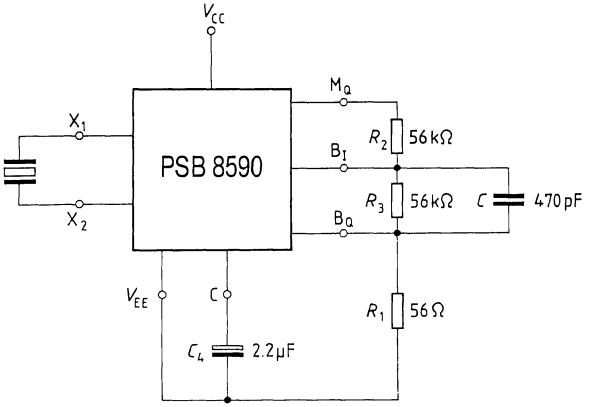
The sum output level P_S is

$P_S = 10 \log (10\ P_L/10 + 10\ P_M/10) = -4.0$ dBm

and the preemphasis P_D is

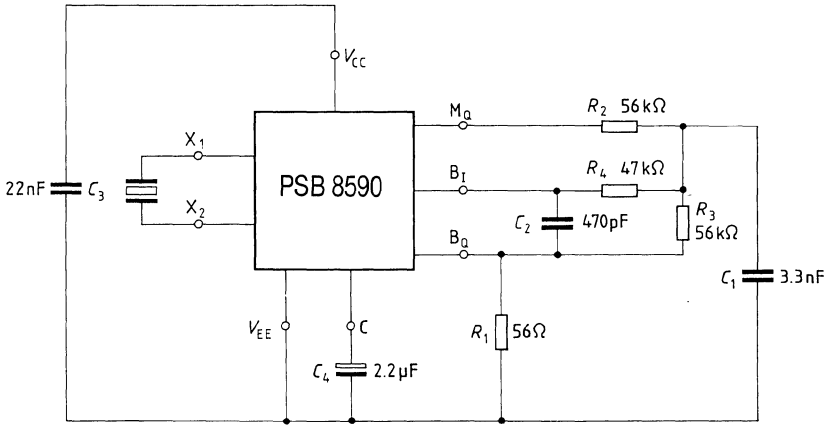
$P_D = P_H - P_L = 2$ dB

Figure 5
PSB 8590 with a 1-pole *RC* filter



In order to keep the insertion loss for all the DTMF frequencies less than 0.2 dB the 3 dB cutoff frequency of the filter should be at least 6 kHz.

Figure 6
S 359 with a 2-pole *RC* filter (Butterworth)



The pole is $f_P \approx 2.7$ kHz

Figure 7
Output spectrum for frequency f_8 with a 2-pole Butterworth filter

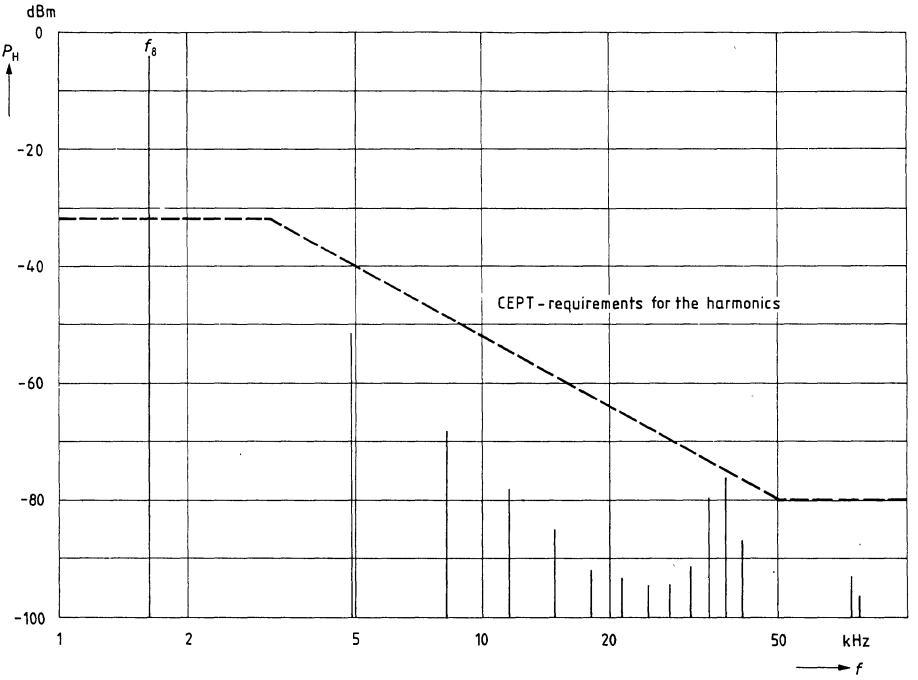
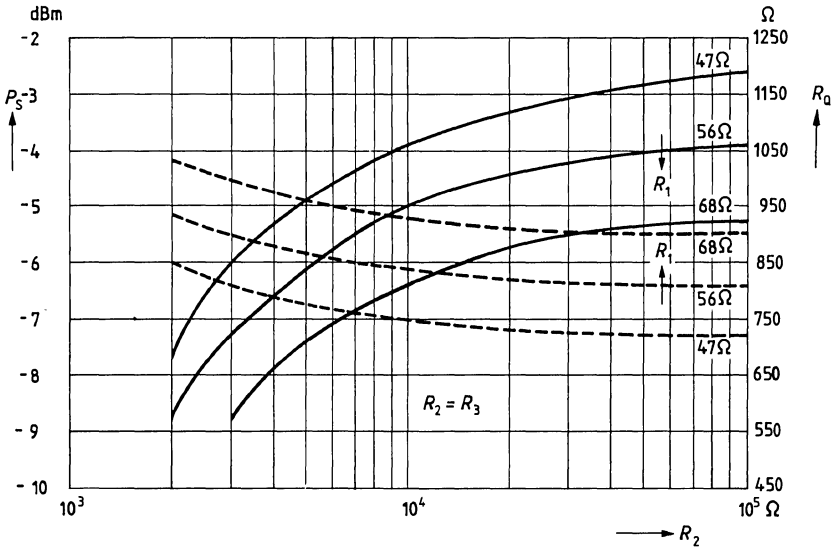


Figure 8
Sum output level P_S (–) and output impedance R_O (– – –) versus resistors R_1, R_2



4. Interface to keypad

There are three different operation modes of the interface:

a) Single contact or 2–of–8 keypad
b) Electronic interface with a 2–of–8 keypad code
c) Electronic interface with a BCD code

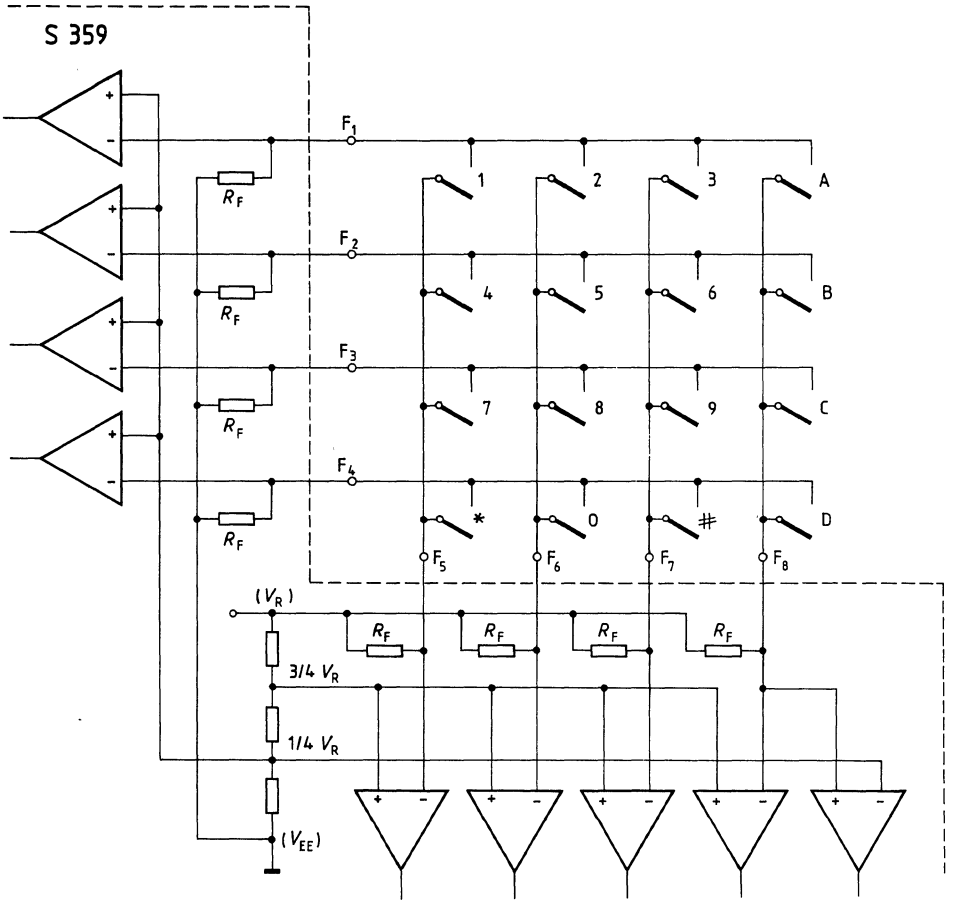
Figure 9 shows the schematic of the interface inputs F_1 – F_8. The inputs are divided into two groups F_1 – F_4 and F_5 – F_8. In addition, the pin F_8 controls the operation modes. The resistors R_F are optimized for the single-contact keypad mode.

a) Interface to single contact or 2–of–8 keypads (Fig. 9)

The buttons are debounced and electronically interlocked. If multiple buttons are pushed, the frequencies of the firstly activated button are generated. The requirements for the quality of the contacts are

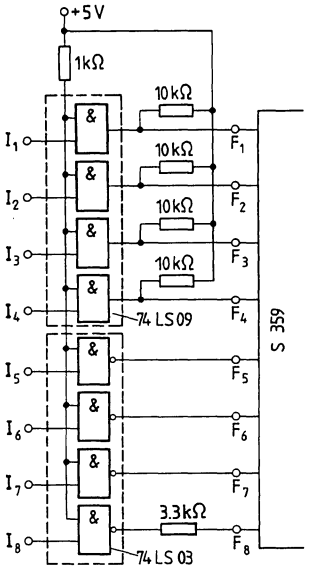
Contact open:	OFF resistance	$R_{OFF} > 50$ kΩ
Contact closed:	ON resistance	$R_{ON} \leqq 1$ kΩ
		$I = 100$ µA

Figure 9
Schematic of keypad interface



b) Electronic interface with a 2–of–8 keypad code

Figure 10
Electronic control using the key code



The inputs I_1 to I_4 control the frequencies of the lower frequency group $f_1 - f_4$ and the inputs I_5 to I_8 control the frequencies of the higher frequency group. For the generation of a dual tone, one input of I_1 to I_4 of the lower group and one input of I_5 to I_8 of the higher group must have an H-level.

If more than one input of the respective group has an H-level, that is recognized as a multiple button push the frequencies of the firstly sensed H-levels are generated.

Truth table

I_1	1	2	3	A	Digit
I_2	4	5	6	B	
I_3	7	8	9	C	
I_4	*	0	#	D	
Inputs	I_5	I_6	I_7	I_8	

c) Electronic interface with a binary code
Electronic control using the binary code

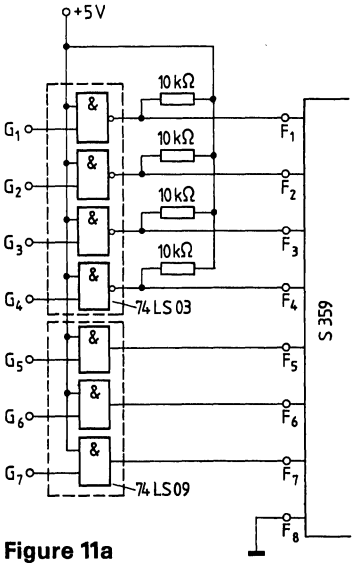


Figure 11a

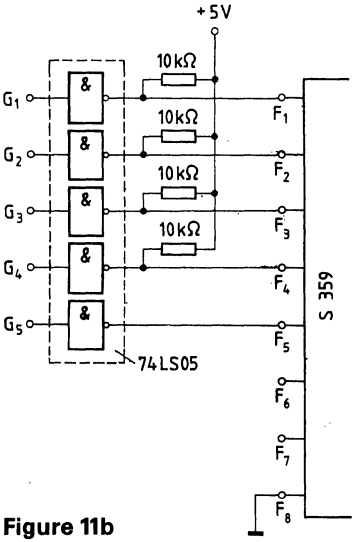


Figure 11b

Application 11a

This application enables both dual and single frequency output.

The mode control input F_8 is connected to ground. The dual tone pairs are generated corresponding to the binary code on the inputs G_1 to G_4. The enable inputs G_5 to G_7 have the following function:

G_5 enable lower and higher frequency group; G_6 enable higher frequency group F_5 to F_8; G_7 enable lower frequency group F_1 to F_4

Application 11b

This application is optimized for dual tone output without single tone capability.

G_1 to G_4 inputs for binary code; G_5 enable lower and higher frequency group.

L-level enables the frequencies, H-level disables the frequencies. If the frequencies are disabled, the internal clock is inhibited.

Table information is present at inputs G_1 to G_4 in binary code

Digit	0	1	2	3	4	5	6	7	8	9	X	#	A	B	C	D
G_4	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
G_3	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
G_2	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
G_1	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H

Pin description

Pin No.	Name	Function
1	V_{EE}	Negative line connection
2	M_O	Mixer output
3	F_1	Keyboard interface
4	F_2	Keyboard interface
5	F_3	Keyboard interface
6	F_4	Keyboard interface
7	B_I	Input of output amplifier
8	B_O	Output of output amplifier
9	X_1	Connections for crystal $f = 2^{22}$ Hz
10	X_2	Connections for crystal $f = 2^{22}$ Hz
11	F_8	Keyboard interface and mode select
12	F_7	Keyboard interface
13	F_6	Keyboard interface
14	F_5	Keyboard interface
15	C	Connection for filtering capacitor for the current sink
16	V_{CC}	Positive line connection

Electrical characteristics

Absolute maximum ratings[1)]

		Min	Max	Unit
Voltage at any pin		$V_{EE}-0.3$ V	$V_{CC}-V_{EE}$	
Supply voltage	$V_{CC}-V_{EE}$	−0.3	14	V
Storage temperature	T_{stg}	−55	125	°C

Operating characteristics (T_{amb} = −25°C to 70°C)

		Test condition	Min.	Typ.	Max.	Unit
Supply current	I_S		16		120	mA
DC output voltage	V_S	16 mA$<I_S<$120 mA	4.5	5	6	V
Internal reference voltage	V_R		1.15	1.25	1.35	V
Input resistors	R_F		2.5	3.5	4.5	kΩ
Input levels:						
Logical L	F_1–F_4				0.15	V
Logical H	F_1–F_4		0.5			V
Logical L	F_5–F_7				0.7	V
Logical H	F_5–F_8		1.1			V
Logical L	F_8		0.5		0.7	V
BCD mode enable	F_8				0.1	V

[1)] Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating characteristics (T_{amb} = –25°C to 70°C)

		Test conditions	Min.	Typ.	Max.	Unit
Output levels:						
Low group	P_L			–8.12		dBm
High group	P_H			–6.12		dBm
Sum level	P_S	I_S = 17 mA to 120 mA Fig. 12	–5.4	–4	–2.8	dBm
Preemphasis	P_D	I_S = 17 mA to 120 mA	1.8	2.4	2.8	dB
Sum level (Frequencies disabled)	P_{SQ}			–80		dBm
Output dynamic impedance	R_{DQ}	I_S = 120 mA I_S = 20 mA	600 660		1000 1000	Ω Ω
Timing specification:						
Tone frequency deviation	$\Delta f/f$		–2.9		+3.9	‰
Key debounce time	t_d		2		6	ms
Set-up time (Fig. 13)	t_s	I_S = 17 mA to 20 mA I_S = 20 mA to 120 mA			7 5	ms ms

Tone frequency deviation (without tolerances of crystal)

	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	Unit
Required frequency	697	770	852	941	1209	1336	1477	1633	Hz
Generated frequency*)	697.2	771.0	851.1	943	1212.6	1337.5	1472.7	1638.4	Hz
deviation	2.75	1.374	–1.037	2.087	3.829	1.1	–2.898	3.307	‰

*) The generated frequencies are derived from a clock crystal with 4.194304 MHz (2^{22} Hz).

Figure 12
Measuring circuit for output sum level P_{SQ}

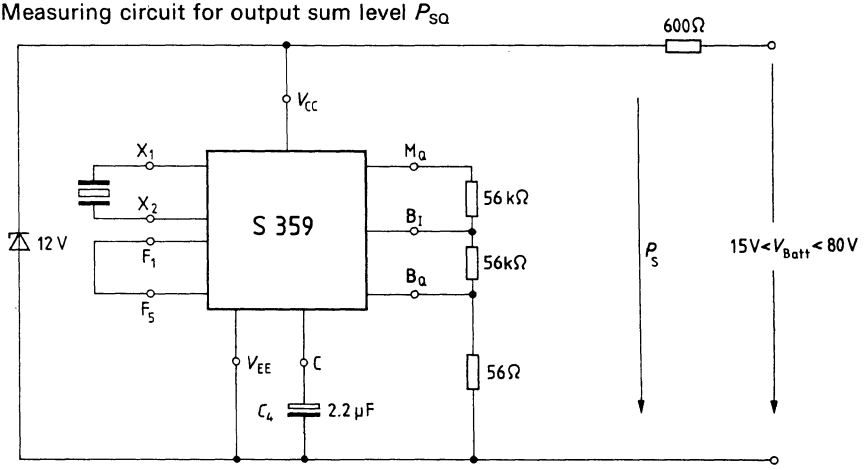
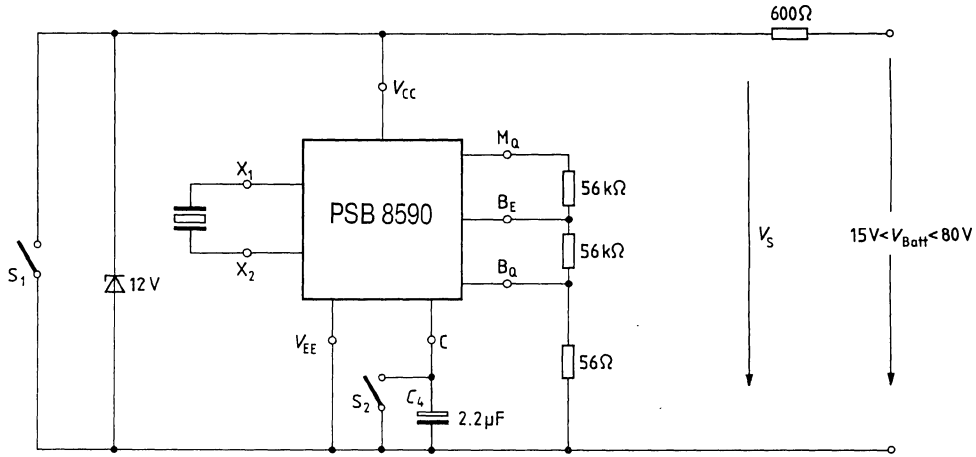
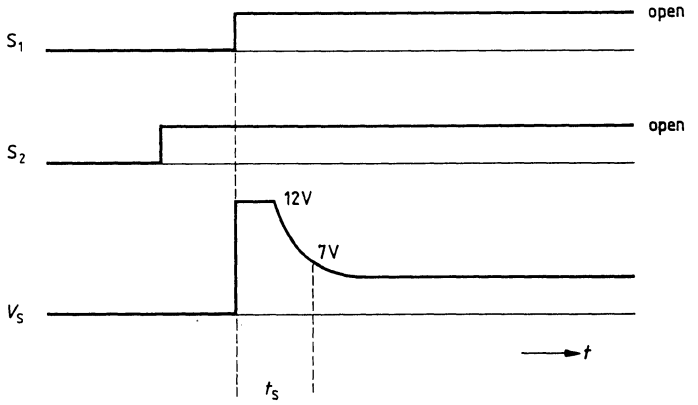


Figure 13
Circuit for measuring set-up time t_s





PSB 8591
Dual Tone Multifrequency Generator

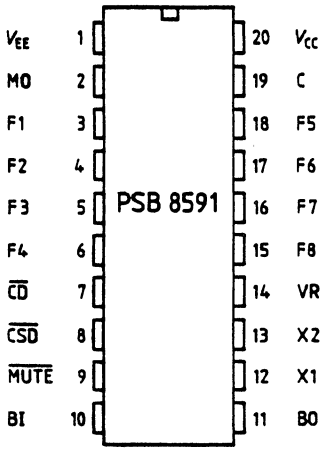
Preliminary data **Bipolar circuit**

The DTMF generator PSB 8591 is an advanced development of the PSB 8590. The PSB 8591 has an additional mute output, a chip disable function and a current sink disable function.

Features

- CEPT compatible output spectrum and output levels
- Direct line powered
- Mute output
- Chip disable ($\overline{CD}$)
- Current sink disable ($\overline{CSD}$)
- MPU interface with data latch on-chip
- Operation with either single contact or 2-of-8 keypads
- 2 key rollover with contact debounce
- Dual-tone and single-tone operation
- High frequency accuracy (typ. 0.4%)
- Standard low cost clock crystal 4.19 MHz
- Power dissipation limited by internal thermal overload protection
- I^2L technology

Pin configuration
(top view)



Pin designation

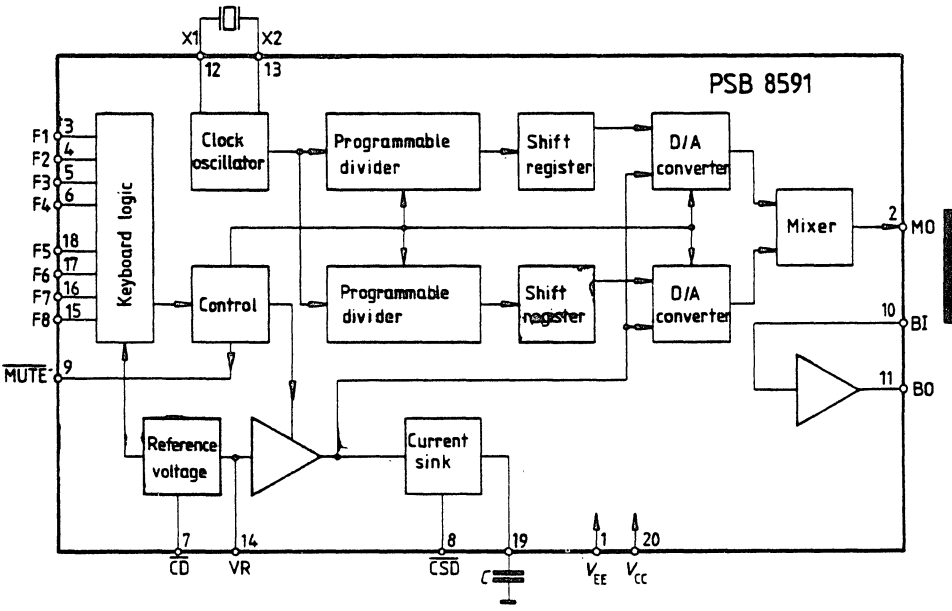
Pin No.	Symbol	Description
1	V_{EE}	Negative line connection
2	MO	Mixer output
3	F1	Keyboard interface
4	F2	
5	F3	
6	F4	
7	$\overline{CD}$	Chip disable
8	$\overline{CSD}$	Current sink disable
9	$\overline{MUTE}$	Mute output (open collector)
10	BI	Input of output amplifier
11	BO	Output of output amplifier
12	X1	Connections for crystal $f = 2^{22}$ Hz
13	X2	
14	V_R	Voltage reference
15	F8	Keyboard interface and mode select
16	F7	Keyboard interface and write enable
17	F6	
18	F5	Keyboard interface and supply current enable
19	C	Connection for filtering capacitor for the current sink
20	V_{CC}	Positive line connection

General description

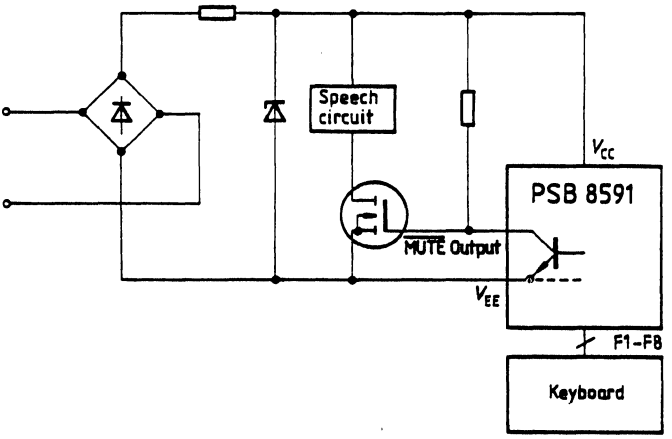
The DTMF generator PSB 8591 is a monolithic IC using the I^2L technology. It provides all dual-tone multi-frequency (DTMF) pairs required in tone dialing systems. The eight different audio output frequencies are generated from an on-chip reference oscillator with an external low cost clock crystal (2^{22} Hz). The internal temperature compensated voltage reference determines the audio output levels and controls the on-chip shunt regulator which provides the adaptation to different feeding conditions.

In order to meet the CEPT recommendations an external 2-pole RC-filter can easily be connected. Typical telephone application are shown in **figure 15.** The PSB 8591 can interface directly to a single contact keypad. Furthermore, the device can be controlled either from a MPU (binary mode) or via a 2-of-8 keypad. The PSB 8591 works in parallel to the speech circuit. If no button is pressed, the device consums only a low standby current. When data is input via keyboard or MPU interface, a low-active mute signal is generated.

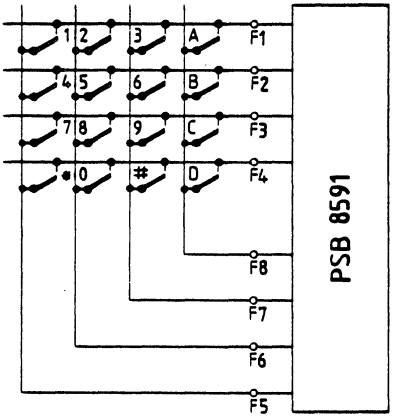
Block diagram



Connection to the telephone-line



Single contact keypad interface



Two key rollover with contact debounce is provided.

Required contact spezifications:

Open contact: Resistance $R_N > 400$ kΩ
Closed contact: Resistance $R_E \leq 1$ kΩ for I = 100 µA

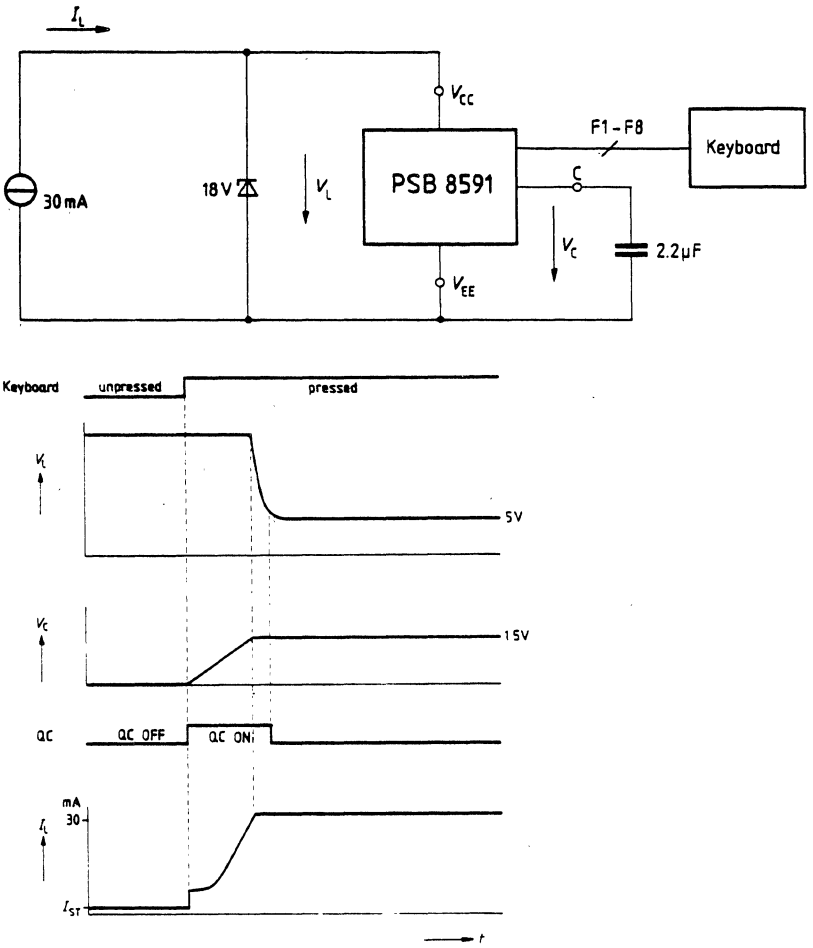
Functional description

1. Line adaptation

The DTMF generator PSB 8591 has an internal temperature-compensated voltage reference. This reference voltage controls a shunt regulator which sets the DC voltage $V_S = V_{CC} - V_{EE}$ to 5 V. The external filtering capacitor C gives the shunt regulator for frequencies above 300 Hz the behavior of a high impedance current sink. The shunt regulator includes a start-up circuit for the quick charging of the filtering capacitor (**fig. 1**). The shunt regulator can sink line currents up to 120 mA while the power dissipation is limited by internal thermal overload protection. If the chip temperature exceeds a preset value ($\approx T_j$ = 150°C, $P_V \approx 1$ W), the filtering capacitor is discharged, the shunt regulator is switched off and the voltage V_S rises to the breakdown voltage of the external overvoltage protection network (**fig. 2**). If the current sink is disabled (low level at $\overline{CSD}$, pin 8) an external shunt regulator or speech circuit should be used.

Figure 1

Tuning diagram of the quick charging circuit (QC) for the filter capacitor. Additional test conditions: Pin 7 ($\overline{CD}$) open and button pressed.

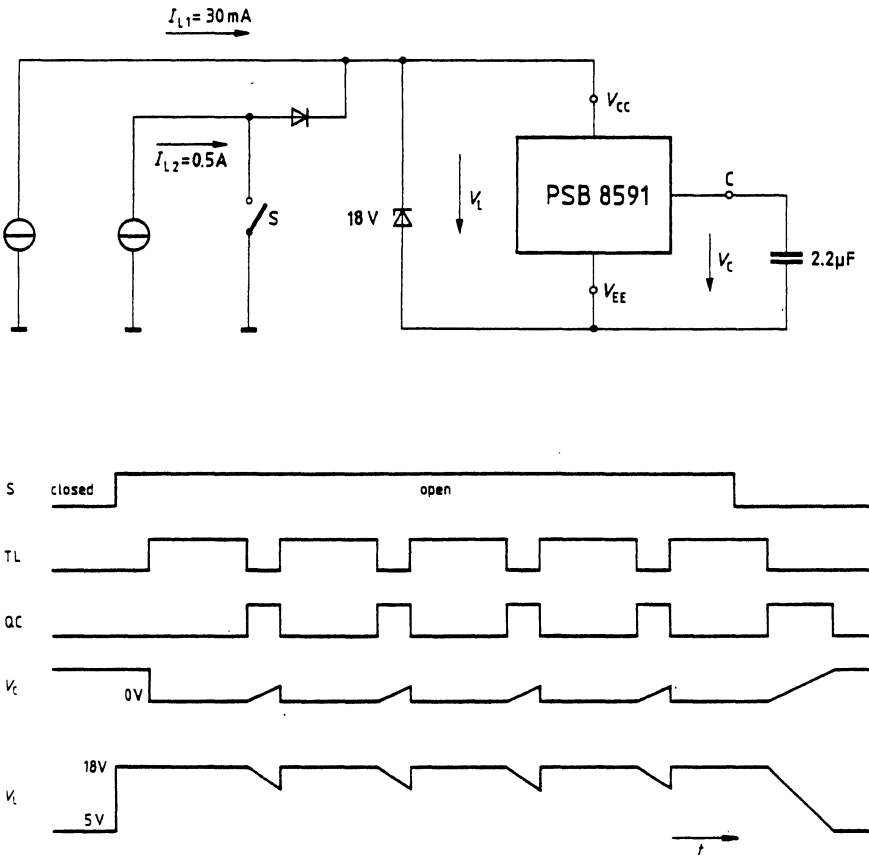


The control circuitry for the quick charging circuit has a hysteresis with the following thresholds:

QC	V_L	V_C
ON	X	0.7 V
ON	9 V	X
OFF	6.5 V	0.7 V

Figure 2

Output waveforms V_S during thermal limitation (TL) of the power dissipation.
Additional test conditions: Pin 7 ($\overline{CD}$) open and button pressed



The thermal limitation (TL) overrides the quick charger (QC).

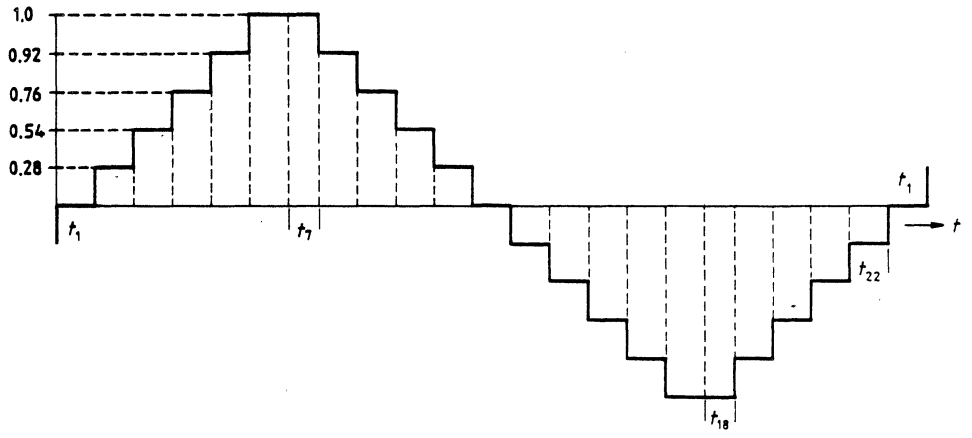
2. Tone generation

The on-chip oscillator generates together with the external clock crystal the master clock frequency f_{CLK} = 4.194304 MHz.

Clock f_{CLK} is scaled by a factor of 16 to f_{CLK} = 262.144 kHz. The programmable dividers for the higher (f_5–f_8) and lower (f_1–f_4) frequency tone groups are driven by the clock f_{CLK}. The programmable dividers generate the clock for the 6-bit L/R shift register. Each shift register controls one D/A converter and the polarity of its output waveform. The output sinewave is synthesized as a stairstep function with 11 voltage levels. The output waveform has 22 time segments **(fig. 3)**. The time segments t_1 to t_6, t_8 to t_{17} and t_{19} to t_{22} are equal. The time segments t_7 and t_{18} are equal but slightly different from the others in order to meet the required output frequencies as closely as possible. The output waveforms are symmetrical; therefore, no even harmonics exist. The stairstep function with 11 voltage levels is calculated such that, theoretically, the lowest order harmonics are the 21st and 23rd. Because of the different length of time segments t_7 and t_{18} and the tolerances of the D/A converter, lower odd harmonics exist.

Figure 3

Synthesized output waveforms



3. Output levels

Each D/A converter generates a five-level stairstep function. The mixer alternately reverses the polarity of the five-level stairstep function which leads to the symmetrical 11-level stairstep function **(fig. 3)**. Furthermore, the mixer adds the stairstep function of the lower and of the higher frequency groups.

The nominal amplitudes of the stairstep function at the mixer output are:

Lower frequency group $i_{ML} = 42.5\ \mu A$
Higher frequency group $i_{MH} = 53.5\ \mu A$

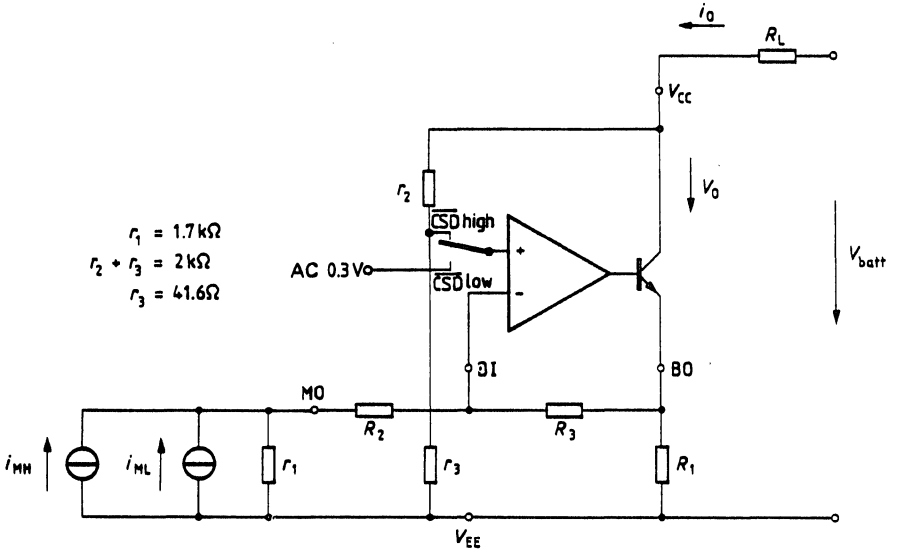
Figure 4 shows the AC-schematic of the output section of the PSB 8591. The feedback loop of the output amplifier is externally arranged. The resistors R_1 to R_3 determine the output level (V_{OL} and V_{OH}) and the output impedance R_O, as shown below.

$$R_O = \frac{R_1\,(r_2 + r_3)}{R_1 + r_3\left(1 + \frac{R_3 + R_1}{R_2 + r_1}\right)}$$

$$V_{OL,\,H} = i_{ML,\,H} \times \frac{(R_3 + R_1)\,R_L \times r_1}{R_1\,(R_2 + r_1)} \times \frac{R_O}{R_O + R_L}$$

The ratio of the resistors R_3/R_2 is restricted to the range $R_3/R_2 < 1.2$, otherwise the output amplitudes are clipped. Normally, the resistors R_2 and R_3 are equal. **Fig. 8** shows the sum level P_S and the output impedance R_O as a function of R_1 and R_2.

Figure 4
AC schematic of the output stage



The internal feedback loop is normally closed (r_2, r_3, positive input of output amplifier). If the current sink is disabled, the positiv input of the output amplifier is supported with a fixed voltage of about 0.3 V. This voltage is derived from the internal reference voltage.

An external RC filter network is necessary in order to meet CEPT recommendation concerning distortion and harmonics. The RC filter is easy to implement, because the pins MO, BI, BO of the output amplifier are accessible. The PSB 8591 is shown in **fig. 5** with an one-pole RC filter for application corresponding to the recommendations of the DBP and in **fig. 6** with a two-pole RC filter for CEPT applications. **Fig. 7** shows the output spectrum for the most critical case, the frequency f_8.

The nominal output levels $P_{L,H}$ are identical for the arrangement in **fig. 5** and **fig. 6,** they are

$$P_L = 20 \log \left(\frac{V_{OL}}{\sqrt{2}\ \sqrt{1\ \text{mW} \times 600\ \Omega}} \right) = -8.12\ \text{dBm}$$

$$P_H = 20 \log \left(\frac{V_{OH}}{\sqrt{2}\ \sqrt{1\ \text{mW} \times 600\ \Omega}} \right) = -6.12\ \text{dBm}$$

The sum output level P_S is

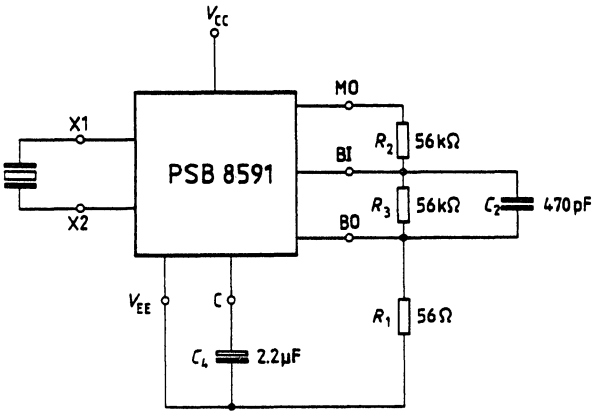
$P_S = 10 \log\ (10\ \text{EXP}(P_L/10) + 10\ \text{EXP}(P_H/10)) = -4$ dBm

and the preemphasis P_D is

$P_D = P_H - P_L = 2$ dB

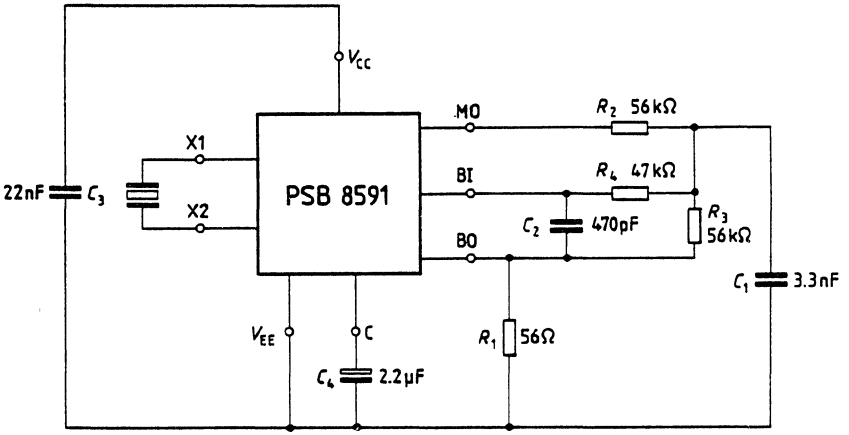
Figure 5

PSB 8591 with a 1-pole RC filter



In order to keep the insertion loss for all the DTMF frequencies less than 0.2 dB the 3 dB cutoff frequency of the filter should be at least 6 kHz.

Figure 6
PSB 8591 with a 2-pole RC filter (Butterworth)



The pole is $f_p \approx 2.7$ kHz

Figure 7
Output spectrum for frequency f_8 with a 2-pole Butterworth filter

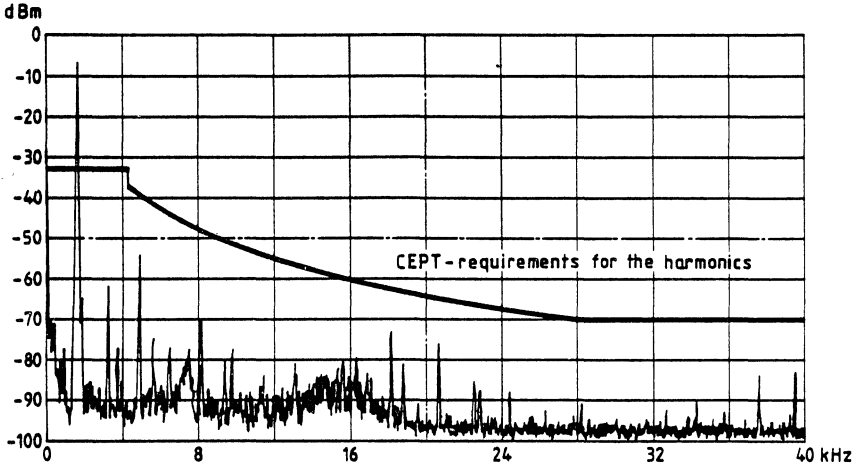
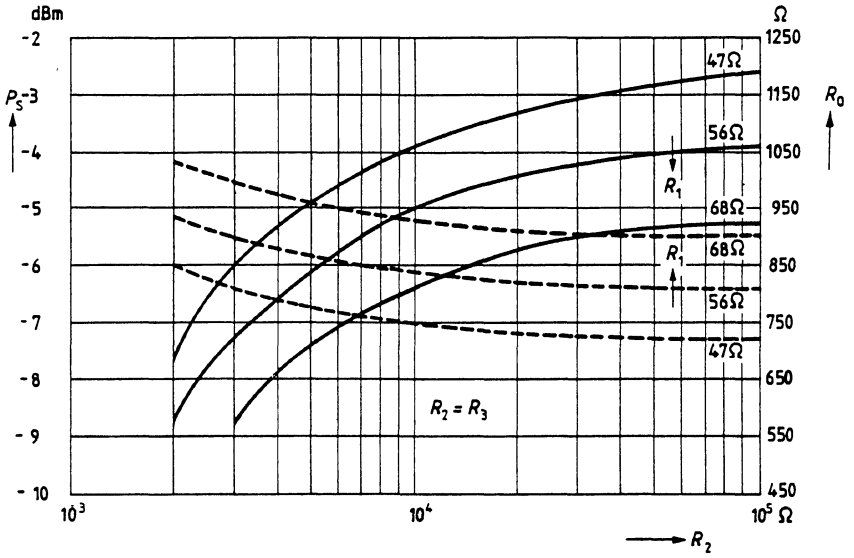


Figure 8

Sum output level P_S (–) and output impedance R_O (---) versus resistors R_1, R_2.



Operation modes:

a) Single contact or 2-of-8 keypad interface
b) MPU interface

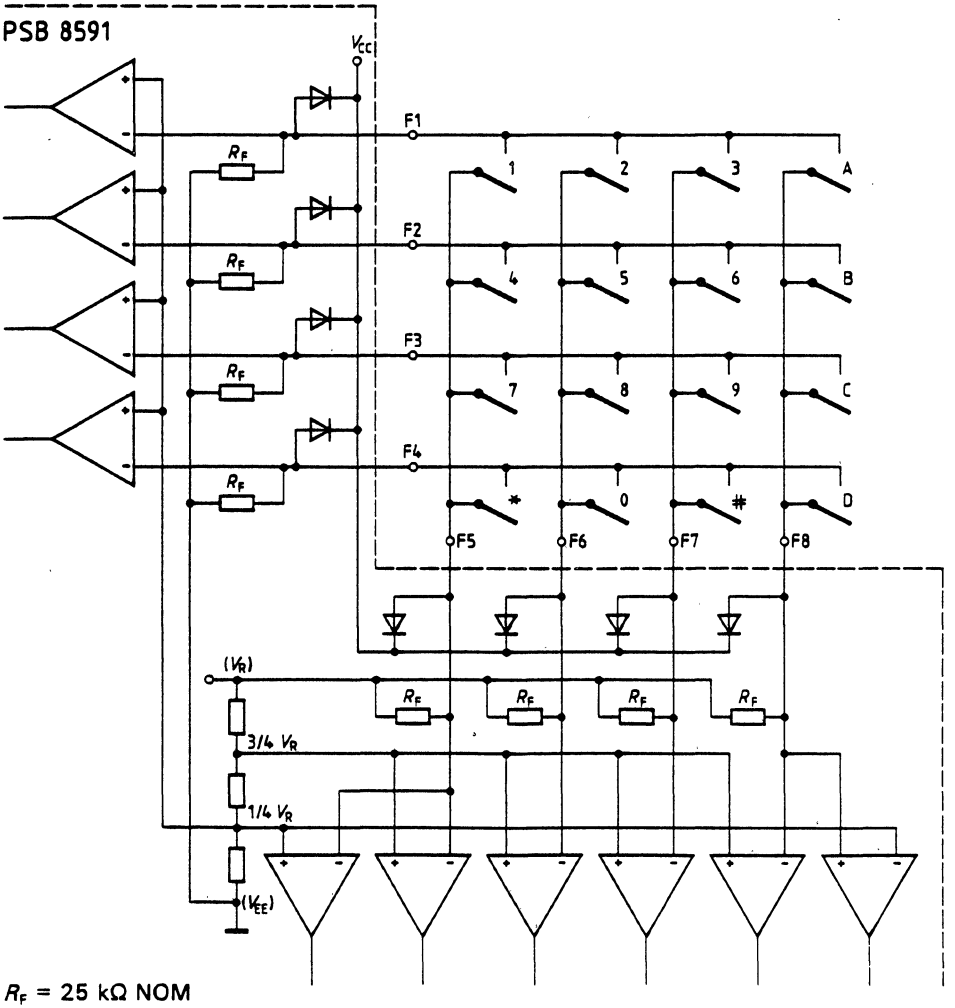
Figure 9 shows the schematic of the interface inputs F1 to F8. The inputs are divided into two groups F1 to F4 and F5 to F8. In addition, pin F8 controls the operation modes. The resistors R_F are optimized for the single-contact keypad mode.

a) Interface to single contact or 2-of-8 keypads **(fig. 9)**

The buttons are debounced and electronically interlocked. If multiple buttons are pushed, the frequencies of the first activated button are generated. The requirements for the quality of the contacts are

Contact open:	OFF resistance	$R_{OFF} > 400$ kΩ
Contact closed:	ON resistance	$R_{ON} \leq 1$ kΩ
		$I = 100$ µA

Figure 9
Schematic of keypad interface



R_F = 25 kΩ NOM
V_R = 1.25 V ±0.1 V

The mode control input F8 is connected to ground; pin 7 ($\overline{CD}$) ist open. Low level at pin 8 ($\overline{CSD}$) disables the current sink. The dual tone pairs are generated corresponding to the binary code at the inputs G1 to G4, as shown in the following table.

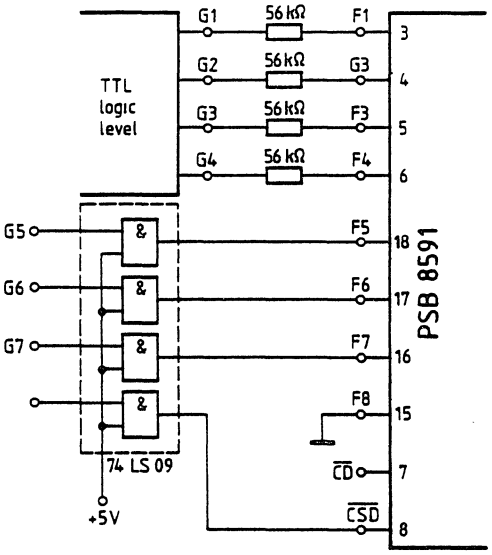
Table information is present at inputs G1 to G4 in binary code

Digit	0	1	2	3	4	5	6	7	8	9	*	#	A	B	C	D
G4	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L
G3	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L
G2	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L
G1	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L

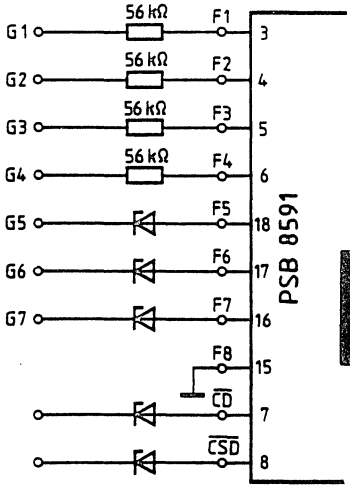
b) Figure 10

MPU interface

I. with open collector AND-Gate



II. with Schottky-diodes



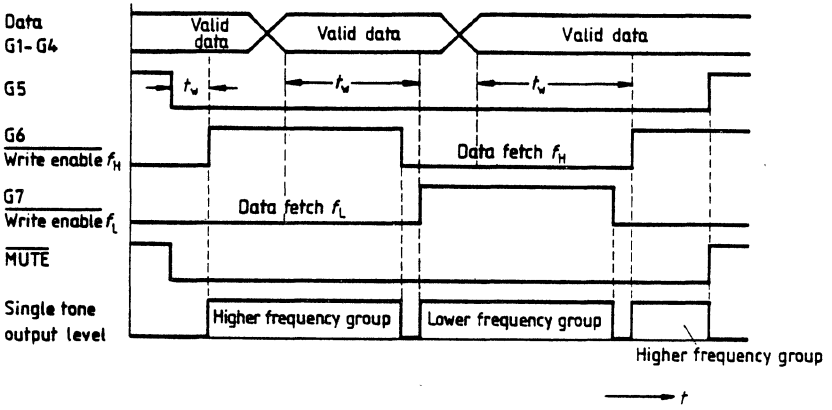
The enable inputs G5 to G7 have the following functions:

G5	G6	G7	
L	L	L	data fetch for f_L and f_H, output inhibited
L	H	L	single-tone, higher frequency group (f_H), data fetch for f_L
L	L	H	single-tone, lower frequency group (f_L), data fetch for f_H
L	H	H	sending, dual-tone

The application in **fig. 10** enables both, dual-and single-tone output.

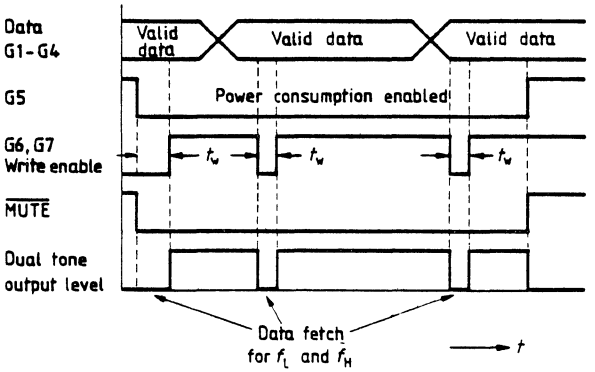
Timing diagram

Binary data input; single-tone output, F8 connected to ground.



Timing diagram

Binary data input; dual-tone output, F8 connected to ground



The valid input data is stored in clock-level-controlled flipflops

$t_w \geq 10\,\mu s$

Electrical characteristics

Absolute maximum ratings[1])

		min.	max.	
Voltage at any pin	V	V_{EE} −0.3	see operating characteristics	V
Supply Voltage	$V_{CC} - V_{EE}$	−0.3	22 (2ms)	V
Storage temperature	T_{stg}	−55	125	°C

Operating characteristics (T_{amb} = −25°C to 70°C)

		Test conditions	min.	typ.	max.	
Leakage current[2])	I_{LK}	V_L = 18 V			100	µA
		V_L = 5 V		20		µA
Standby current[3])	I_{St}	V_L = 18 V			0.6	mA
		V_L = 5 V		0.4		mA
Line current[4])	I_L		16		120	mA
Supply current[6])	I_S	V_L = 5 V		13	15	mA
Current sink voltage drop[4]) (average DC value)	V_L	16 mA ≦ I_L ≦ 120 mA	4.5	5	6	V
Minimal peak line voltage[6])	V_{Lmin}	(see fig. 11)		3		V
Maximal peak line voltage[6])	V_{Lmax}	(see fig. 11)		18		V
Internal reference voltage[5])	V_{REF}		1.15	1.25	1.35	V
Input resistors at pin 3–6, 13–16, F1–F8 and $\overline{CSD}$	R_F		15	25	35	kΩ

[1]) Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]) $\overline{CD}$ connected to ground, chip disabled

[3]) F1–F8 open, $\overline{CD}$ open, chip enabled

[4]) Current sink enabled ($\overline{CSD}$ = high level), button pressed or F5 and F8 connected to ground

[5]) $\overline{CD}$ open, chip enabled

[6]) Current sink disabled ($\overline{CSD}$ = low level), button pressed or F5 and F8 connected to ground

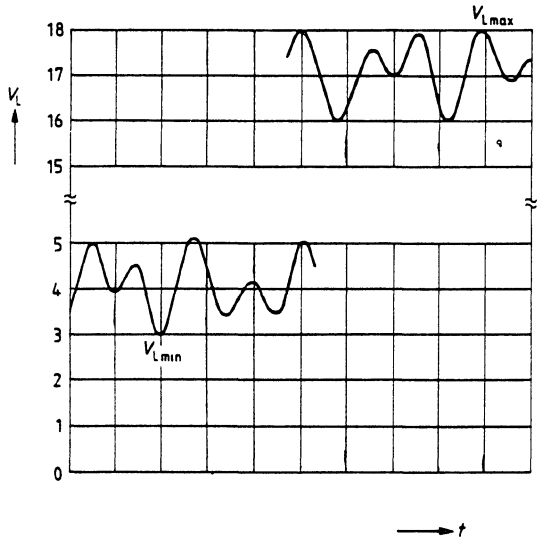
Operating characteristics (T_{amb} = −25°C to 70°C)

Input levels		Test conditions	min.	typ.	max.	
Logical L	$V_{IL\ F1-F4}$		−0.3		0.15	V
H	$V_{IH\ F1-F4}$		0.5		V_{CC}	V
Logical L	$V_{IL\ \overline{CSD},\ F8-F7}$		−0.3		0.7	V
H	$V_{IH\ \overline{CSD},\ F5-F8}$		1.1		V_R	V
Logical L, key code	$V_{IL\ F5,\ F8}$		0.5		0.7	V
Binary mode enable	$V_{IL\ F8}$		−0.3		0.1	V
Supply current enable	$V_{IL\ F5}$		−0.3		0.1	V
Logical L	$V_{IL\ \overline{CD}}$	$I_{IL\,max}$ −10 µA	−0.3		0.3	V
Logical H	$V_{IH\ \overline{CD}}$	Input current $I_{IH\,max}$ = 1 mA	0.7		5	V
Mute output levels						
Logical L	$V_{OL\overline{MUTE}}$	$I_{OL\,max}$ = 1 mA			0.5	V
Logical H	$V_{OH\overline{MUTE}}$	$I_{OH\,max}$ = 1 mA			V_{CC}	V
	$I_{IH\overline{MUTE}}$	$V_{OH\overline{MUTE}}$ = 18 V			100	nA
Output levels						
Low group	P_L			−8.12		dBm
High group	P_H			−6.12		dBm
Sum level	P_S	I_L = 16 mA to 120 mA fig. 13	−5.4	−4	−2.8	dBm
Preemphasis	P_D	I_L = 16 mA to 120 mA	1.8	2.4	2.8	dB
Sum level (Frequencies disabled)	P_{SO}			−80		dBm
Output dynamic impedance	R_{DO}	I_L = 120 mA	600		1000	Ω
		I_L = 20 mA	660		1000	Ω
	R_{Dd}	$\overline{CSD}$ low V_L = 5 V (current sink disabled)		9		kΩ
Output dynamic impedance in Standby mode	R_{St}	V_L = 5 V	10	20		kΩ
Timing specification						
Tone frequency deviation	$\Delta f/f$		−7	4	+7	‰
Key debounce time	t_d		2		6	ms
Set-up time (fig. 13)	t_s	I_L = 16 mA to 120 mA			7	ms
		I_L = 16 mA to 120 mA			5	ms
Width of write pulse (see page 15)	t_w			2	10	µs

Tone frequency deviation (without tolerances of crystal)*

	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	Unit
Required frequency	697	770	852	941	1209	1336	1477	1633	Hz
Generated frequency*)	697.2	771.0	851.1	943	1212.6	1337.5	1472.7	1638.4	Hz
deviation	2.75	1.374	-1.037	2.087	3.829	1.1	-2.898	3.307	‰

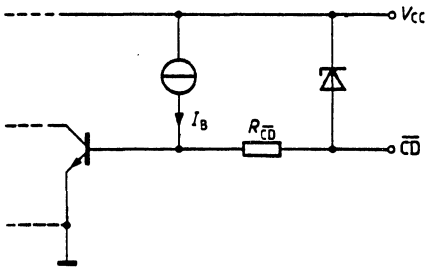
Figure 11
Minimal/maximal peak line voltage



*) The low cost crystal has the following deviations (including aging and temperature range): $\Delta f/f \leq 3.5 \times 10^{-3}$.

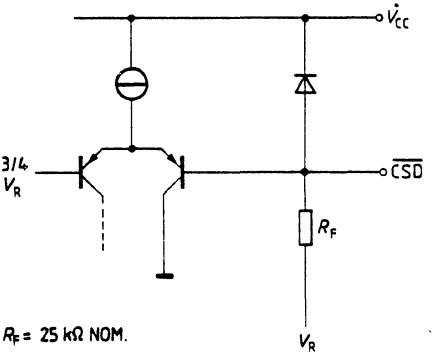
Figure 12
Schematic of inputs $\overline{CD}$ (pin 7) and $\overline{CSD}$ (pin 8):

Equivalent of input $\overline{CD}$



I_B = 5 µA typ
$R_{\overline{CD}}$ = 5 kΩ NOM.

Equivalent of input $\overline{CSD}$



R_F = 25 kΩ NOM.

Figure 13
Measuring circuit for output sum level P_{SO}, power enabled

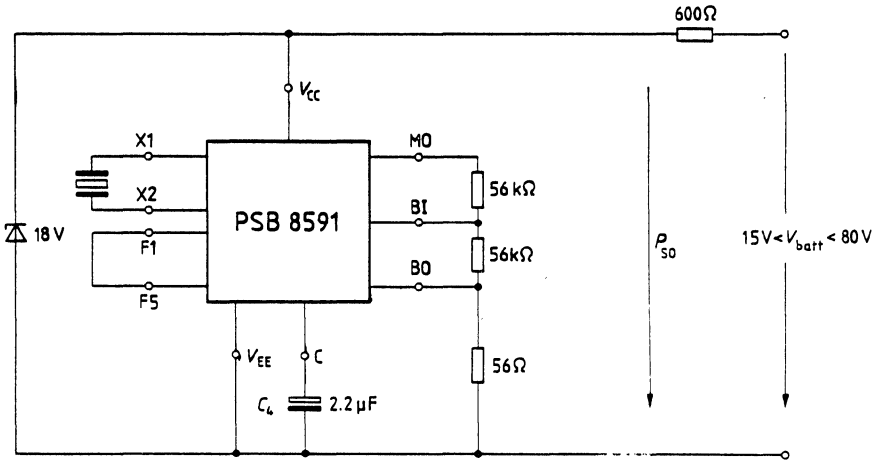
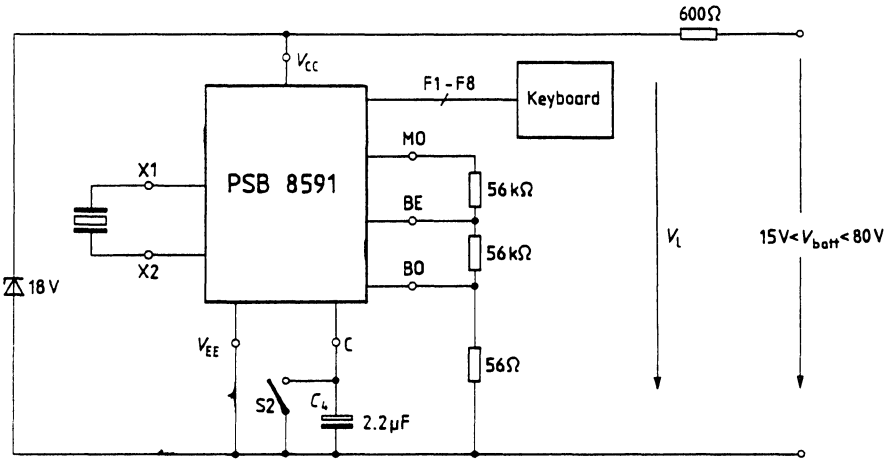


Figure 14
Circuitry for measuring set-up time t_s, buttons pressed or binary mode



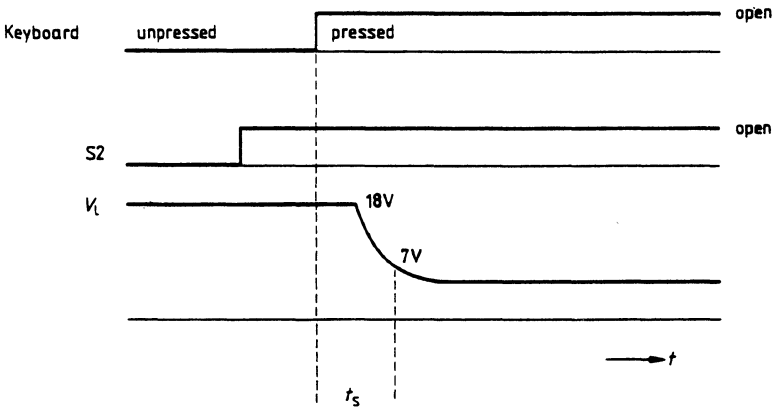


Fig. 15 a

Application example

PSB 8591 connected to a speech network with hybrid transformer

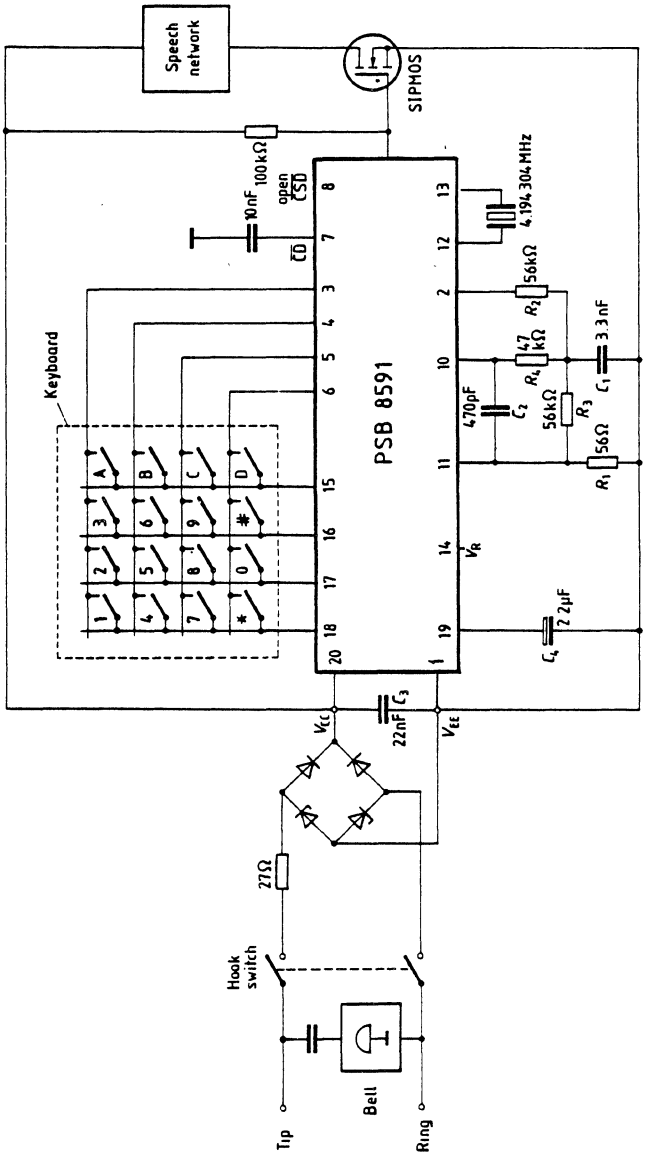


Fig. 15 b

Application example

PSB 8591 connected to a integrated speech circuit

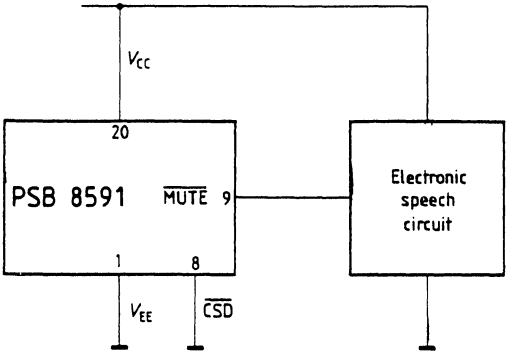
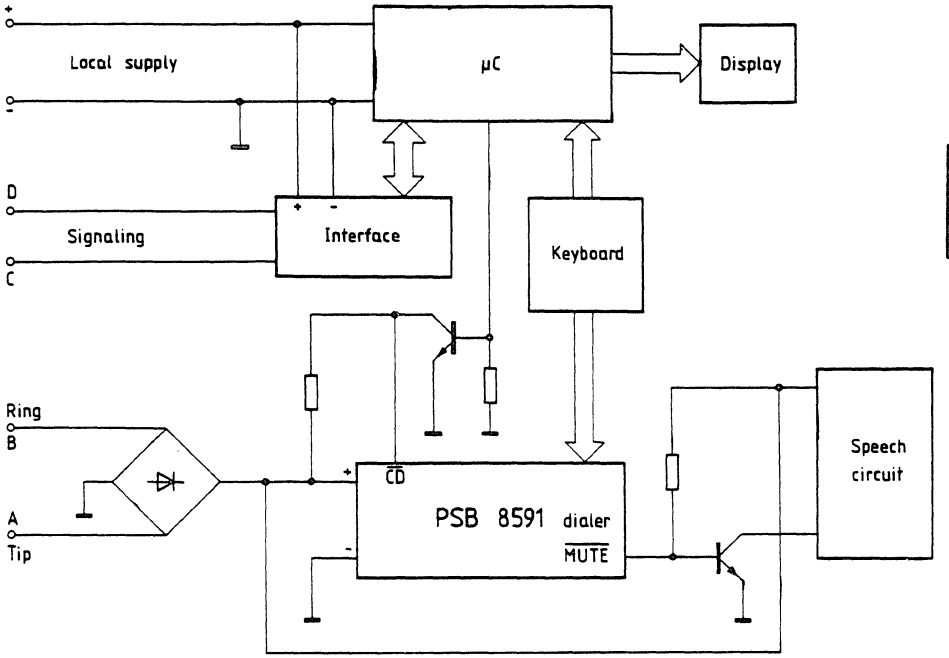


Fig. 15 c

Principle blockdiagram of a key telephone using the $\overline{CD}$-function.

In the case of local supply failure the PSB 8591 is activited so that dialing is still possible.



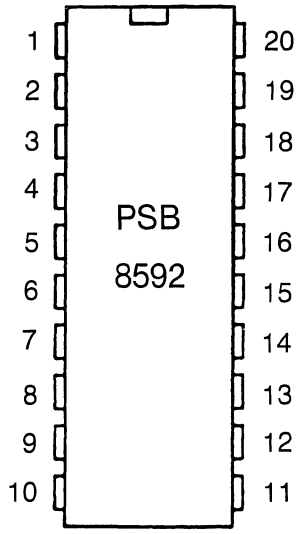
PSB 8592
Dual Tone Multi Frequency Generator

Preliminary data MOS-circuit

Features

- Advanced CMOS Technology
- Last number redial up to 22 digits
- Flash generation (register call)
- CEPT compatible without external filtering
- Standard low cost TV crystal 3,58 MHz
- High frequency accuracy (better than 0,4%)
- Operation with single contact matrix keyboard, 20 buttons
- Multikey lockout and debouncing
- Binary data input
- Dual tone and single tone output
- Defined audio output time and interdigital pause
- Programmable access pause
- Low operation and standby current
- Mute output
- Chip enable input
- Internal power-on reset
- 20 Pin DIL package

Pin configuration
top view

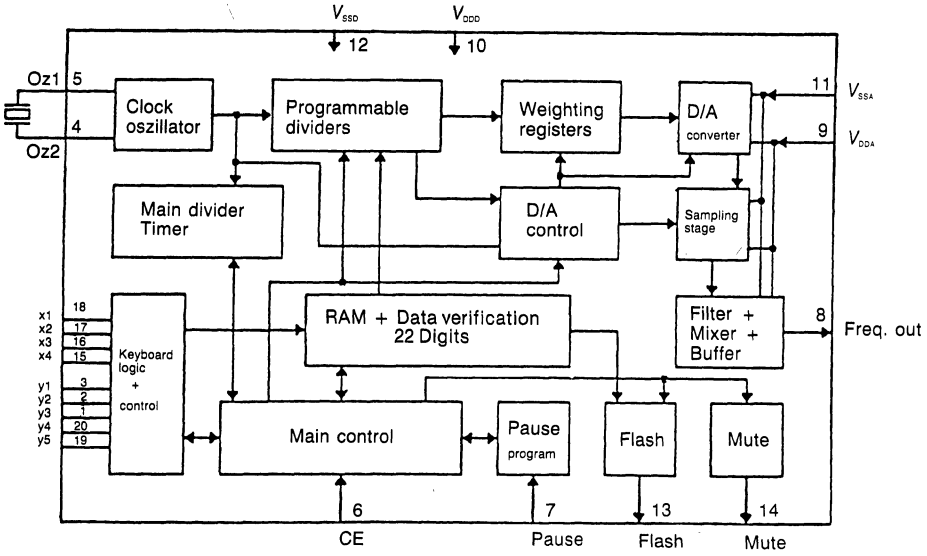


Pin	Funktion
18	x1
17	x2
16	x3
15	x4
19	y5
20	y4
1	y3
2	y2
3	y1
6	Hook-Switch-Chipenable
13	Flash out
10	V_{DD} dig
12	V_{SS} dig
7	Pause 3,5,00
9	V_{DD} ana
11	V_{SS} ana
8	Freq. out
5	oz 1
4	oz 2
14	Mute out

General description

The DTMF Generator PSB 8592 is specifically designed to implement a dual tone telephone dialing system. The device can interface direcly to a standard pushbutton telephone single-contact keyboard type x-y matrix code and operates together with an integrated speech circuit. All necessary dual-tone frequencies are derived from the widely used standard TV crystal (3.58 MHz) providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. The votage reference is on speech circuit and regulates the signal levels of the dual tones to meet the recommended telephone specifications. The Buffer-Amplifier is also situated in the speech circuit, which provides the Overvoltage-Protection. Other applications of the device include radio and mobile telephones, remote control and process control.

Block diagram



Functional description

Internal Logic Description

After detecting a key closure the oscillator will start. When the oscillation is high enough to operate the first flip-flop the oscillator current will be reduced and the whole logic will be reset. The chip command starts first the logic-comparator to suppress the switch bouncing. After the protection time the valid code will be stored in the RAM. First the RAM will be reset, when the valid Code is a new dialed number. Then the code will be read out of the RAM and will program the two dividers of the sinewave synthesizer. This will be done continuously until the key is released, or as long as the sending timer (80 ms) works. In the meantime further digits can be stored in the RAM. After the sending timer has finished or the key contact opens the command starts the

pausetimer (80 ms), the same counter is used in both cases. At this point the command reads the next digit from the RAM or finishes the function of the device. The command also sets the MUTE output to high, when it is programming the dividers and sets the MUTE output to low before finishing the function of the device and will remain low until new sinewaves are generated. If the detected key closure is the redial function the commmand starts to readout the stored number from the RAM. If the detected key closure is a single tone mode, the command only programs the appropriate divider during key depression. The MUTE output has the same function as in dual-tone-mode without timing.

Mute output:

	sending DTMF-signals
no key depressed	

Tone Generation

When a valid key closure is detected or a digit is still in the RAM marked for access the command programs the high and low group dividers with appropriate divider ratios, so that the output of these dividers cycle at 26 times the desired high group and low group frequencies for a minimum of 80 ms.

The outputs of the programmable dividers drive two 6 stage up and down counters with connected sign bit. The symmetry pulses of the clock inputs to the two counters divided by 2 with the sign bit allows 26 equal time segments to be generated within each output cycle.

The 26 segments are used to synthesize digitally a stair-step waveform to approximate the sinewave function (see Figure) in one D/A converter for the high and low group frequency. To synthesize the two sinewave functions in one D/A-converter it is necessary that the converter works in under 600 ns because he must be multiplexed between the two functions. This is done by connecting a weighted capacitor ladder network between the outputs of the counter via sign bit circuit connected to $V_{ref} = V_{DD}$ or V_{SS} and virtual ground. The peak-to-peak amplitude of the stairstep function is weighted by a connected sample and hold capacitor with a different value for the high and low frequency-group. After the sample and hold capacitor a low passfilter follows, one for the high and one for the low frequency group. The individual tones generated with different amplitudes and filtered separately are added linearly and drive an output buffer.

Single Tone Mode

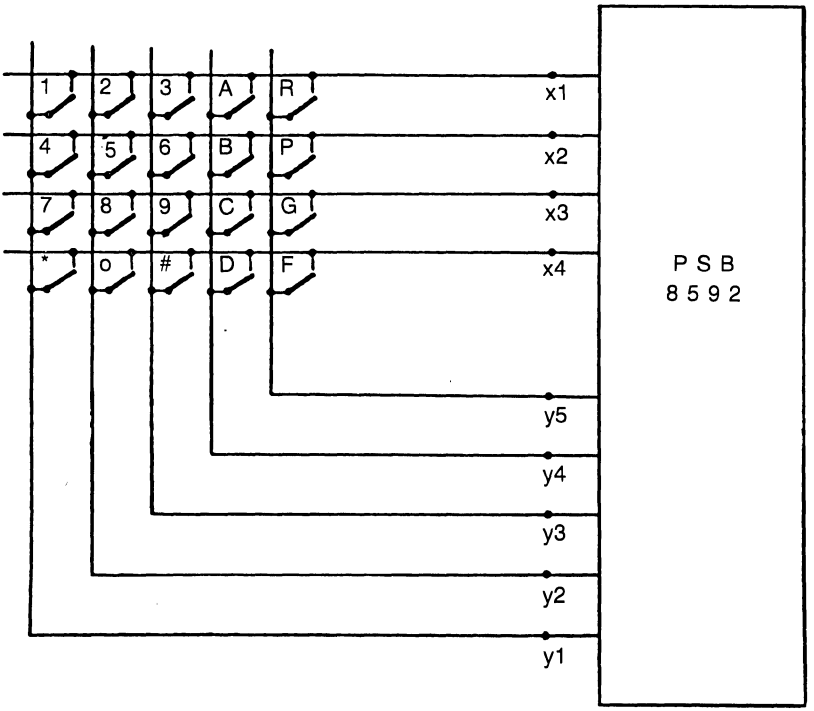
A low group tone can be generated by activating the appropriate row inputs with ground. A high group tone can be generated by activating the appropriate column inputs with V_{DD}. In this mode no digit frequency combination will be activated and no digit will be stored in the RAM.

The generation time depends on the duration of the input function. A stored dial-number remains in the RAM.

Clock Generation

The device contains an oscillator circuit with the necessary parasitic capacitances on chip so that it is only necessary to connect the standard 3.58 MHz TV crystal across the OSCI and OSCO terminals to implement the oscillator function. The oscillator functions whenever a row or column input is activated until all timing functions are terminated.

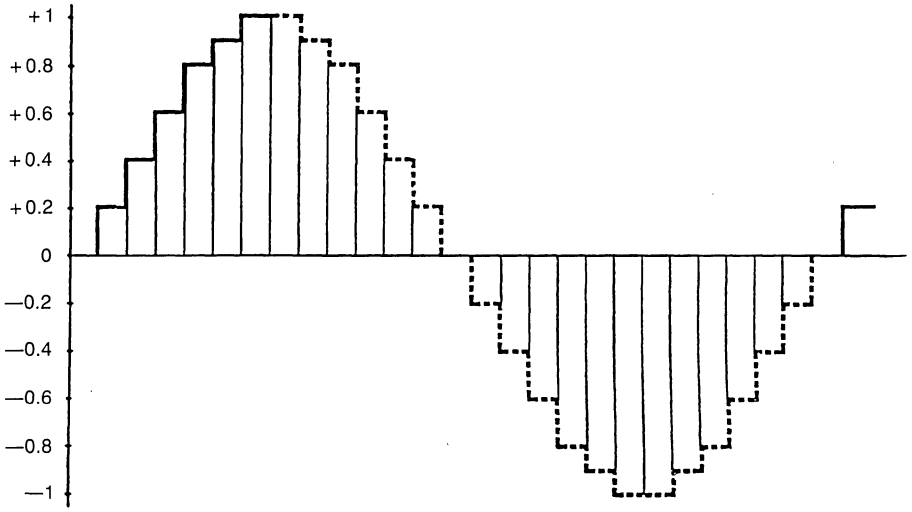
Connection to keyboard



Keyboard Interface

The device can be connected directly on a X-Y Matrix Key-Board without protection against multi key function. Internal logic prevents the transmission of illegal tones when more than one key is pressed. Individual tones can be obtained by connecting a column input to V_{DD} or grounding a row input. The inputs are static after key recognition, i.e. there is no noise generation as occurs with scanned or dynamic inputs. The interrupt of more than 4 ms on the key-inputs releases the Key-function in the recognition-circuit.
After this next digit will be detected.

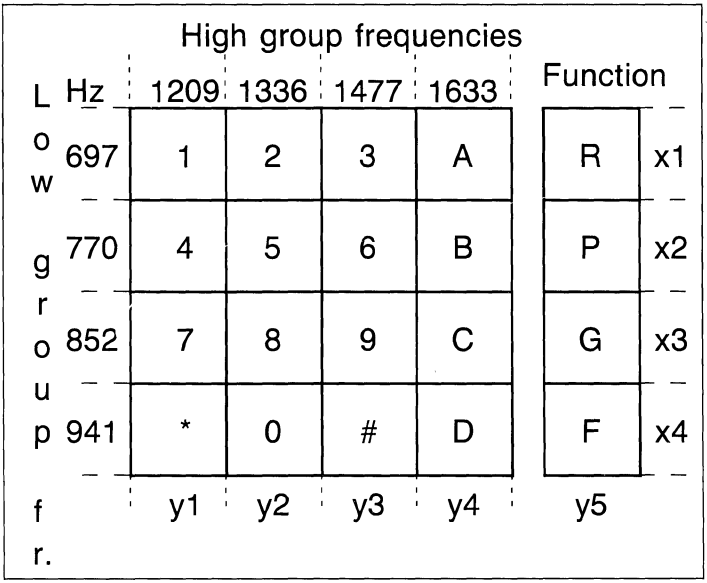
Synthesized output waveforms



Aktiv Input	Output Frequency (Hz) specified	actual	% without crystal drift
X1	697	695.32731	— 0.241
X2	770	773.4539	+ 0.448
X3	852	849.84449	— 0.254
X4	941	942.97813	+ 0.210
Y1	1209	1207.67375	— 0.110
Y2	1336	1336.64862	+ 0.049
Y3	1477	1480.37428	+ 0.228
Y4	1633	1638.98581	+ 0.365

Special Functions

Keyboard configuration (maximal)



R = Redial
P = Pause
G = Go for shortening Pausetime
F = Flash

The position of the 4 Special-Keys is in the device mask-programmable.

Redial-Function

If the redial-button is depressed after handset pickup, all stored numbers in the RAM including Pause- and Flash-function will be sent out. After termination and during Redial-Function it is possible to dial further digits, which will be sent after termination of the Redial-Function. Before starting the redial-function a superversion circuit checks the usefulness of the RAM contents.

Programming of Pause

If the telephonsystem needs pauses for example for trunksearching or dial-tone connection, the pauses must be stored in the RAM. To store such pauses only depress the Pause-Button, after this further digits can be dialled. The number of pauses is unlimited. The timing of the pause is programmable via the Pause-Programming-Pin.

There are 3 choice: Programming-Pin connected for 3 s,
connected to ground 5 s,
open unlimited Pause.

Go-Function

To Go-Button terminates the unlimited pause. Furthermore all timed pause-functions can be terminated earlier. With a transistor connected in parallel to the Go-Button-Switch the pause can be terminated by operating the transistor with a dial-tone recognition-circuit.

Flash-Function

The Flash-Function will be handled like the pause-function, it will be stored in the RAM. The number of Flashes is unlimited. The Flash-Output goes to V_{DD} for 90 ms and after one Flash-function is completed the DTMF-Signaling will continue after a pause of 900 ms.

Special-Pulse-Pause-Timing for German-Post-Application in the Redial-Mode

In the Redial-Mode in German-Post-Application the timing must be 80 ms for sending DTMF and 240 ms for pause.

This feature is realized with a lightly modified device. The reason for this is, to keep the sending levels on carrier-wave-systems in the specified ratio.

BCD-Coding

The device has the possibility to operate with a BCD-Interface. The BCD-Inputs are the column pins y1 to y5. To program the device for BCD-Code the row inputs x1 and x4 must be grounded in the same time, when the BCD-Code appears on the column inputs. All digits including pause and flash are stored in the RAM. The minimum timing will be 5 to 8 ms. A quick timing for BCD-Code-Input is possible with Test-Mode-Feature.

Hook-switch/Power-Down

The device is in Power-Down-Mode, when the Hook-Switch-Input is low. In this mode the pull-up resistances are disconnected on the 4 row-inputs and all inputs a passive. In this case the maximum ratings are valid on the inputs. When the Hook-Switch-Input is high $= V_{DD}$, the row and column-inputs are activated and the device can be started via the inputs.

Option: Different exchanges have interruptions in the power feed of the line during trunk-searching time. Therefore it is difficult to detect the right onhook-switch function; we propose to provide our line-power-fault detection with the following function. After every interruption of line power feed, the device starts a timing of 320 ms, during this time the needed power comes from the buffercapacitor (only DTMF and PAUSE-Function). If the power feed is restored in the meantime, the device will ignore the interruption, after 320 ms, the device will accept the interruption as a exchange release and the stored digits are prepared for Redial. During the interruption the device accept dialing but can no send DTMF.

Electrical Characteristics

Absolute Maximum ratings:

		min	max	unit
DC Supply voltage	V_{DD}-V_{SS}	-0.3	+7	V
Input voltage at any pin		-0.3	V_{DD} + 0.5	V
Power Dissipation at 25°C	P		10	mW
Operating Temperature	top	-25	+70	°C
Storage Temperature	t_{stg}	-55	+125	°C

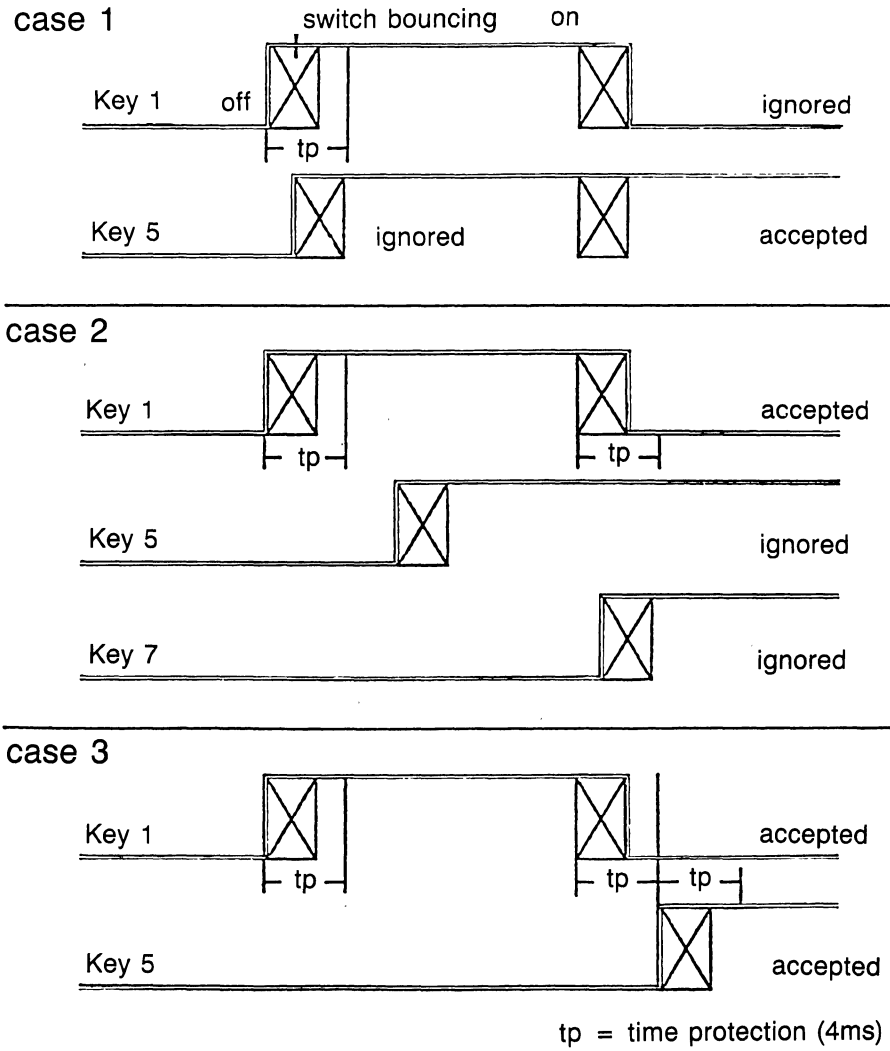
D.C. Characteristics

	Test conditions	min	typ	max	unit
Supply Voltage = Reference Voltage		—	3.5	—	V
Operating current	One Key selected Tone, Mute output unloaded	1	2	—	mA
standby current	no key selected output unloaded	—	1	—	µA
MUTE output resistance		4	5	7	KΩ

A.C. Characteristics

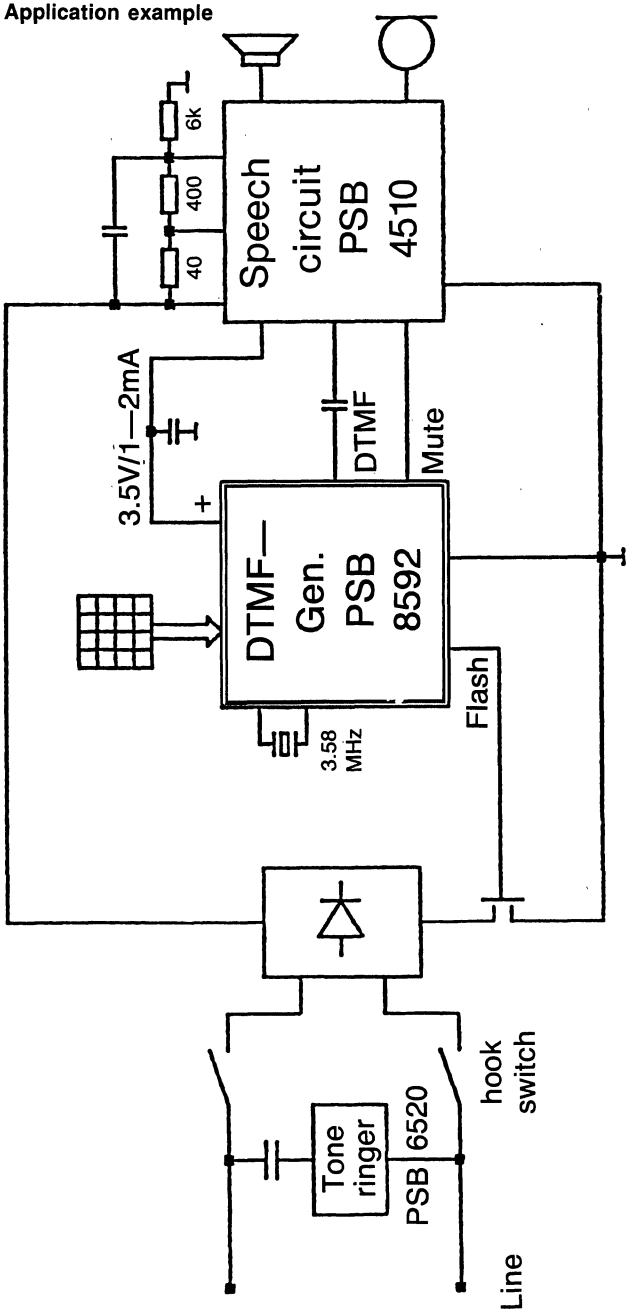
	Test conditions	min	typ	max	unit
Oscillator frequency		—	3.5795	—	MHz

Key closure recognition with x-y key-board



tp = time protection (4ms)

Application example



PSB 7510
LCD Controller

Advance information **MOS circuit**

The PSB 7510 monolithic integrated circuit controls numeric LC displays in quadruple multiplex operation.

Due to "MICROPACK" outline (film carrier), the LC display units are extremely thin and compact.

Features

- CMOS Si-gate technology
- Supply voltage 2.5 V to 6 V
- Display up to 20 digits, 7 segment
- MUX 4
- On-chip oscillator
- Cursor or blinking selectable
- Selection of one flag per digit available
- 2 different character sets
  (0 – 9, 3 bars, A, U blank or
  0 – 9, 2 bars, A, b, c, d, blank)
- 64 pin MICROPACK

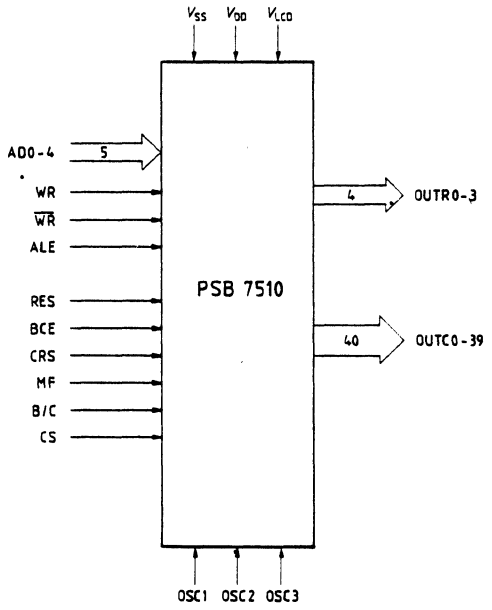
	Type	Ordering code	Quantity per order unit (items)	Minimum shipping quantity (items)	Maximum shipping quantity (items)
Series product film	PSB 7510	Q 67100-Z 155-A 101	1500-2500	100	—
Sample punched out	PSB 7510	Q 67100-Z 155-A 103	5	5	50
DIP 64 intermediate carrier	PSB 7510	Q 67100-Z 155-A 102	1	1	5

For **prototyping,** limited quantities of components can be delivered as punched out MICRO-PACK, or soldered on a DIP 64 intermediate carrier.

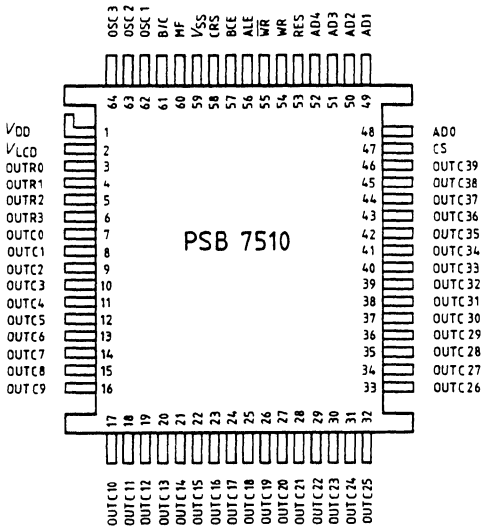
Shipment of the **series product** will be on metal film rolls (CMOS!). These film rolls are the property of Siemens and must be returned when empty.

As the individual rolls do not contain a constant number of components, smaller or lager quantities are possible for partial shipments of large quantities.

Logic symbols



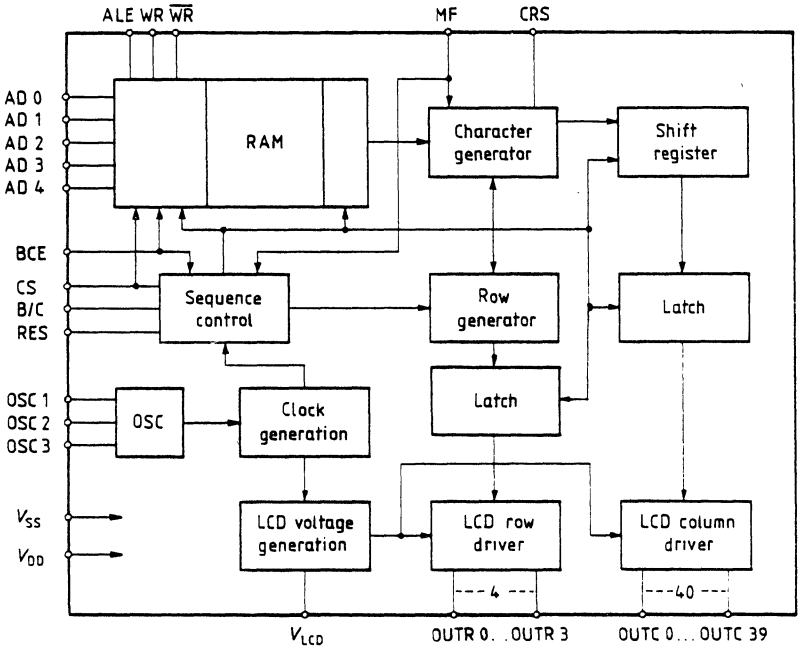
Pin configuration
top view



Pin designation

Pin No.	Symbol	Description
1	V_{DD}	Positive supply voltage
2	V_{LCD}	LCD input voltage
3 ⋮ 6	OUT R0 ⋮ OUT R3	Output row drivers
7 ⋮ 46	OUT C0 ⋮ OUT C39	Output column drivers
47	CS	Chip select
48 ⋮ 52	AD0 ⋮ AD4	Binary inputs for address and data
53	RES	Reset
54	WR	Write data latch enable (non inverting)
55	$\overline{WR}$	Write data latch enable (inverting)
56	ALE	Address latch enable
57	BCE	Blink and cursor enable
58	CRS	Character ROM select
59	V_{SS}	Ground
60	MF	Selection of multiple flag
61	B/C	Blink or cursor function select
62 ⋮ 64	OSC1 ⋮ OSC3	Oscillator inputs

Figure 1
Block diagram



Functional description
(fig. 1 and pin description)

The PSB 7510 controls LCDs in a quadruple MUX mode.

The inputs AD0-AD4 accept the display address and display data in binary code. The display address is latched with ALE and used to address an internal RAM. The data is then stored in the internal RAM using $\overline{WR}$ control signal **(fig. 2)**. The further translation of the display address and data in the RAM is asynchronous to the external control signals and is performed internally using an on-chip oscillator.

In each MUX step the character ROM translates the RAM contents and loads the result into a shift register. At the end of each MUX phase the shift register is latched and used to control the bidirectional switches for the LCD drive signals. The LCD voltages are generated from the input voltage V_{LCD} by an integrated resistor network. Polarity as well as magnitude of the actual LCD voltage for the output analog drivers is provided by a low-resistive switching network.

The IC additionally features underscoring of selected digits by blinking or cursor.

Input B/C selects blinking or cursor and is enabled with blink or cursor enable BCE.

Logic type

Positive logic is used
V_{DD} = "H" high level = logical 1 = positive voltage
V_{SS} = "L" low level = logical 0 = negative voltage

1. Chip select CS

The PSB 7510 responds to external signals only when CS is activated.

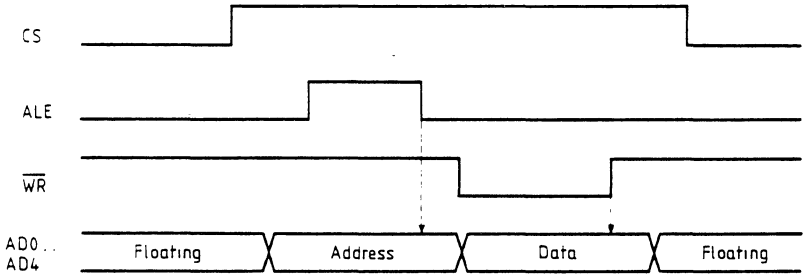
2. Reset RES

Reset clears the display and fills the internal RAM with blanks.

3. Address and data input AD0...AD4

The address pending at AD0....AD4 is latched with the falling edge of ALE. After this address assigment, the display data pending at AD0...AD4 is read into the RAM with the trailing edge of $\overline{WR}$ **(fig. 2).** The inputs use binary code.

Figure 2



4. Multiple flag MF (internal high-ohmic connection with V_{DD})

When MF = 1, normal data input can be used to set one flag per digit at any desired position of the display. The character set automatically specified by MF = 1 (set I) comprises the characters 0...9, 3 bars A, U and a blank. In this case, the character ROM select CRS input is "don't care".

The selected locations are specified by writing a "1" into the unused fifth data bit for this character set (set I).

When a character with a flag is changed, the flag must also be rewritten.

5. Select of character set CRS (internal high-ohmic pullup resistor)

Input CRS is used to select the character set I or II, when MF = 0

Set I: CRS = 0
Set II: CRS = 1

6. Blink or cursor function select B/C (internal high-ohmic pullup resistor with V_{DD})

The input selects whether a digit is to be highlighted in the display by blinking or by a cursor.

Blinking: B/C = 1
Cursor: B/C = 0

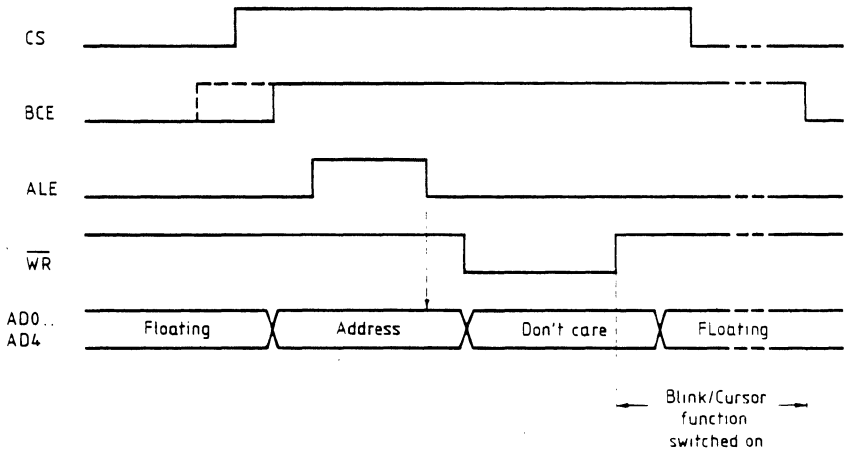
When using the blink option with characters with a flag, the flag blinks as well. The cursor option is not available for characters with a flag.

7. Blink or cursor function enable BCE

BCE = 1 enables the blinking or the cursor function **(fig. 3).** The address of the character in the display that is to be highlighted is latched with the falling edge of ALE. ALE must be followed by a WR signal.
Following data information is "don't care".
This function can only be stopped with BCE = 0.
Reset RES has no effect.
Characters can only be changed when this function is disabled. After a character change, the blinking or cursor address must be given again. The blink or cursor function is available only for one digit at a time.

Figure 3

Blink/cursor functions switched on

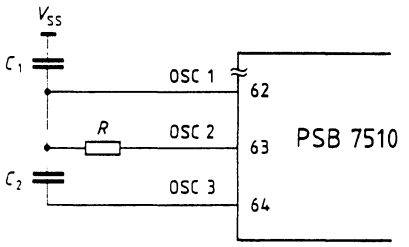


8. Oscillator inputs OSC 1, OSC 2 and OSC 3

The *RC* circuitry of these inputs determines the frequency of the oscillator. With an oscillator frequency of 25.6 kHz, the refresh rate is 40 Hz. **(refer** to **fig. 4).**

Figure 4

***RC* circuitry of oscillator inputs**



Suggested values: $R \approx 270\,k\Omega$
$C_1, C_2 \approx 47\,pF$

9. LCD voltage V_{LCD}

This voltage is applied from off-board and is divided by an integrated resistor network into the optimum interim values.

10. Output drivers

They provide the analog voltages for the LC display

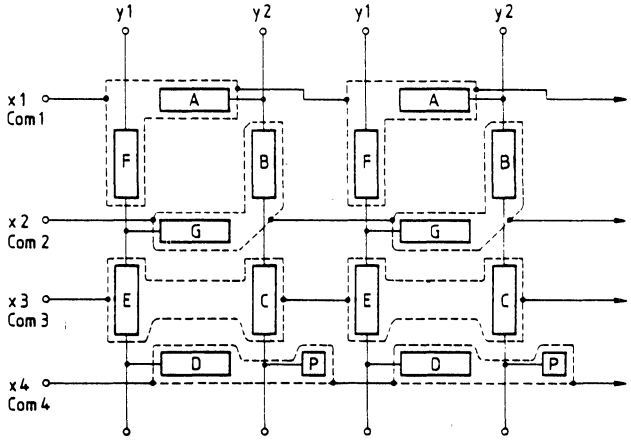
Display input data

Data	Display		Address	Address code
	Set I	Set II		
00000	0	0	0	00000
00001	1	1	1	00001
00010	2	2	2	00010
00011	3	3	3	00011
00100	4	4	4	00100
00101	5	5	5	00101
00110	6	6	6	00110
00111	7	7	7	00111
01000	8	8	8	01000
01001	9	9	9	01001
01010	bar above	bar above	10	01010
01011	bar center	bar center	11	01011
01100	bar below	A	12	01100
01101	A	B	13	01101
01110	U	C	14	01110
01111	blank	D	15	01111
10000		blank	16	10000
			17	10001
			18	10010
			19	10011

Input of an undefined data word causes a blank to be displayed at the respective display location.

Figures 5

Liquid crystal matrix organization



	y1	y2
x1	F	A
x2	G	B
x3	E	C
x4	D	P

Maximum ratings

Ambient temperature under bias	T_{amb}	−25 to 70	°C
Storage temperature	T_{stg}	−40 to 125	°C
Supply voltage referred to GND	V_{DD}	0 to 7	V
All input and output voltages	V	−0.3 to V_{DD}+0.3	V
Total power dissipation	P_{tot}	3	mW

DC characteristics

T_{amb} = 25 °C, V_{SS} = 0 V, V_{DD} = 2.5 V to 6 V

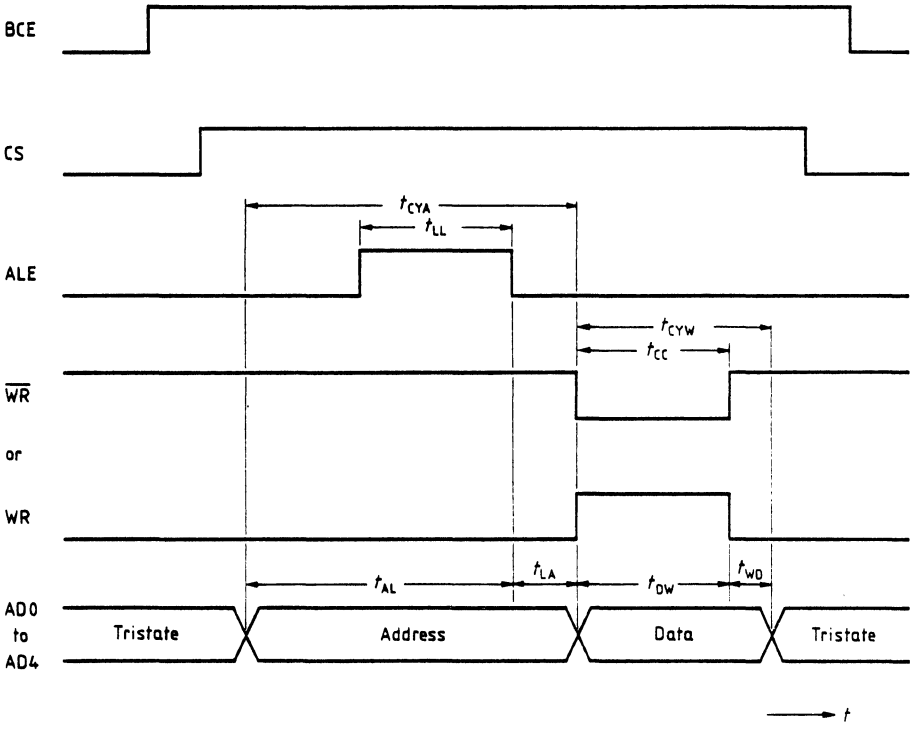
		Test conditions	Min.	Typ.	Max.	Unit
L input voltage (all inputs, OSC1)	V_{IL}		V_{SS}		0.25 x V_{DD}	V
H input voltage (all inputs, OSC1)	V_{IH}		0.7 x V_{DD}		V_{DD}	V
Input leakage current (all inputs, OSC1)	I_{IL}				1	µA
Operating supply voltage	V_{DD}		2.5		6	V
LCD voltage	V_{LCD}	$V_{SS} \leq V_{LCD} \leq V_{DD}$	V_{SS}		V_{DD}	V
Supply current	I_{DD}	V_{DD} = 3 V, ext. clock		30		µA
		V_{DD} = 4 V; ext. clock		50	100	µA
		V_{DD} = 6 V; ext. clock		100		µA
Resistor network for LCD voltage				62		kΩ

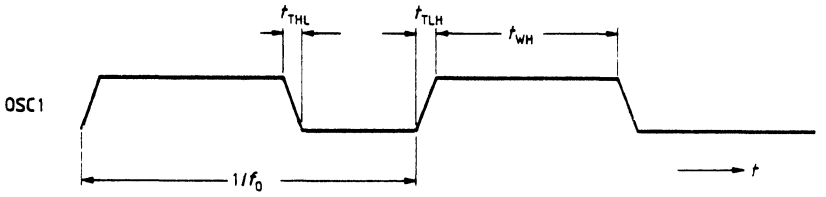
AC characteristics

T_{amb} = 25 °C to 70 °C, V_{SS} = 0 V, V_{DD} = 2.5 V to 6 V

ALE pulse width	t_{LL}		100			ns
Address set-up before ALE	t_{AL}		120			ns
Address hold from ALE	t_{LA}	V_{DD} = 6 V	50			ns
Address latch cycle time	t_{CYA}		1			µs
Control pulse width WR, $\overline{WR}$	t_{CC}		100			ns
Data set-up before WR, $\overline{WR}$	t_{DW}		150			ns
Data hold from WR, $\overline{WR}$	t_{WD}	V_{DD} = 6 V	50			ns
Write data cycle time	t_{CYW}		1			µs
Oscillator frequency	f_{osc}			25	100	kHz
Clock pulse width	t_{WH}	External clock	0.1	20		µs
Clock pulse rise time	t_{TLH}	f_{osc} 25 kHz			5	µs
Clock pulse fall time	t_{THL}	f_{osc} 25 kHz			5	µs

Waveforms


BCE
CS
t_{CYA}
t_{LL}
ALE
t_{CYW}
t_{CC}
$\overline{WR}$
or
WR
t_{AL}
t_{LA}
t_{DW}
t_{WD}
AD0
to
AD4
Tristate
Address
Data
Tristate
t


t_{THL}
t_{TLH}
t_{WH}
OSC1
$1/f_0$
t

Delivery package

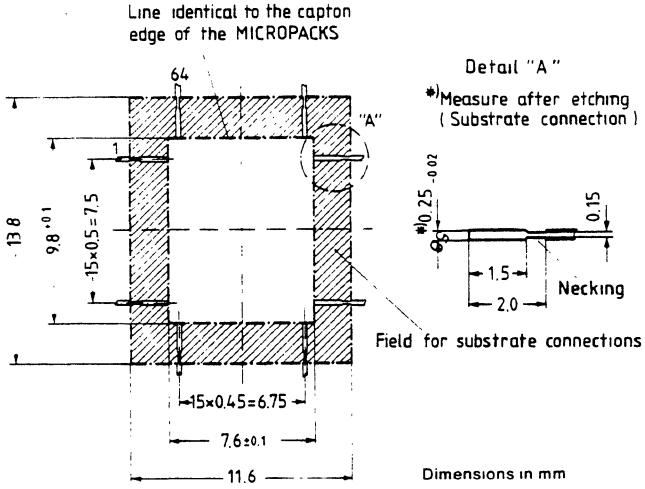
The MICROPACK PSB 7510 is generally delivered on metal film spools in metal cans. For prototypes, the IC can also be packed individually. MOS handling is necessary.

Substrate connections

For assembly of the MICROPACK, the connection points on the substrate must be coated with solder. This can be achieved by:

- galvanic deposition and melting
- screen printing and melting
- dip or wave tinning

Solder tin composition: Sn 60 / Pb 40
Thickness of the layer: approx. 15 µm (after melting)



Note: Necking of the connection leads is not required in the case of galvanically deposited Sn/Pb and subsequent melting.

Assembly recommendations

All assembly recommendations are valid for the following substrate materials:

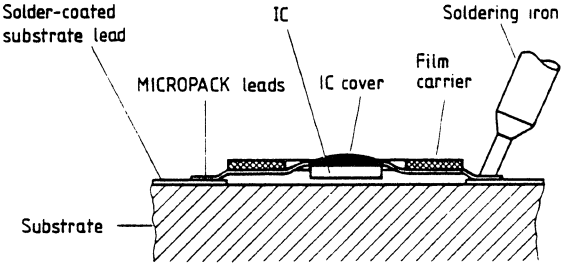
- epoxy resin
- hard-paper
- ceramic (thick-thin-film)
- flexible materials, as for example polyimide
- glass

I. Prototypes and small quantities
(e.g. up to approx. 1.0/year)

Recommended processing method:

Manual soldering with mini soldering iron

Principle



Required equipment and accessories

- devices for cutting and punching (only when processing from tape)
- forming tools
- temperature-regulated miniature soldering iron, certified for the soldering of MOS components
- stereo microscope (magnification 6...40 x)
- suction tube or tweezers
- hair brush
- sodium-free flux according to DIN 8511 (e.g. pure colophonium dissolved in alcohol)
- cleaning agents (if required): e.g. Freon T-P 35 and TF
- bench top suited for the processing of MOS components

Soldering data

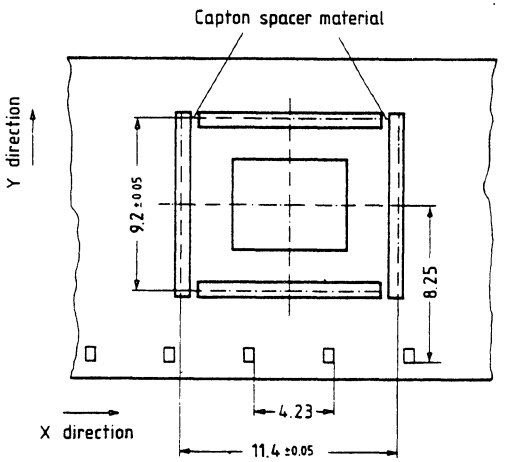
- soldering temperature at the soldering iron tip: 230°C max.
- soldering time: approx. 1 to 2 s

Procedure

Caution! The general rules for the processing of MOS components must be followed during all operations.

Cut MICROPACK leads free with hand tool (for components delivered on spools only).

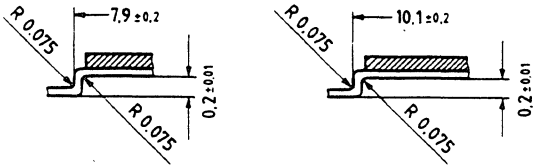
Cutting dimensions: 9.2 ± 0.05 mm x 11.4 ± 0.05 mm



Caution! Only cut free along the dashed lines!
Do not cut the 4 capton spacers.

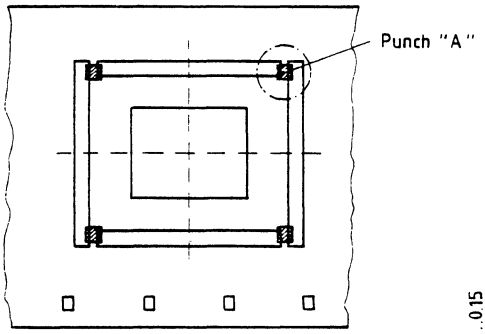
Form MICROPACK leads with hand tool.
(For the relief of mechanical stress when mounted)

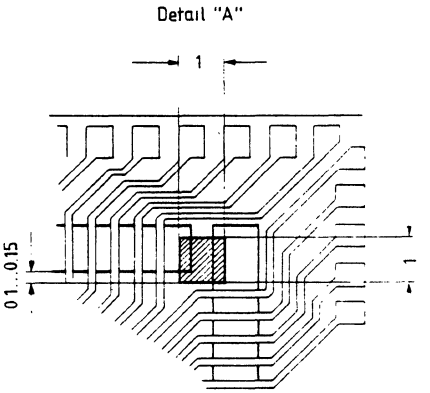
Forming dimensions



Dimensions in mm

Punch MICROPACK out of the film tape with hand tool (for components delivered on spools only)





Lay down the punched MICROPACK onto an electrically conductive surface vacuum pickup.

Coat the mounting points on the substrate with flux (with brush by hand).

Position the MICROPACK and adjust by hand under stereo microscope (approx. 5 to 10x magnification).

Solder the individual leads by hand with soldering iron under stereo microscope

Important! First solder two opposite leads. This prevents a shifting of the MICROPACK during the soldering process.

Cleaning (if required)

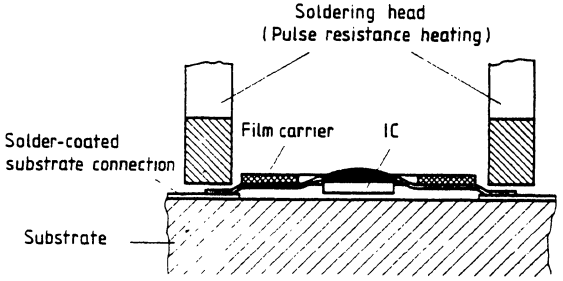
Move the substrates one after the other for approx. 1 minute in T-P 35 and TF for example (no ultrasonic cleaning).

Place the cleaning substrates on an electrically conductive surface or in appropriate trays.

II. Medium quantities
(e.g. up to approx. 30.0/year)

Recommended assembling method:
Pulse soldering with manual device

Principle

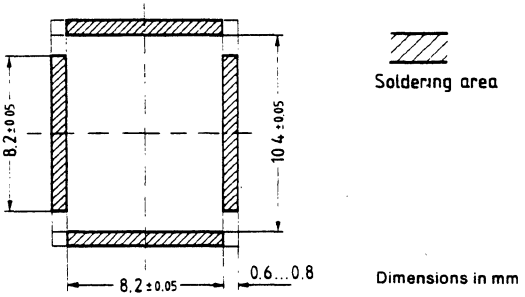


Required equipment and accessories

As in I., only instead of the soldering iron:

Pulse soldering device

Pulse soldering head (dimensions according to the drawing)



Head holder
Control device (temperature, time)
Substrate holder (with micro-manipulator, if necessary)
Stereo microscope

Soldering data

Soldering temperature at the pulse soldering head: 230°C max.
Soldering time: approx. 2 s plus an additional holding time of 1 s until the solder becomes solidified.

Procedure

As described in I. including the positioning of the MICROPACK onto the substrate and the adjustment.

Further steps

Position the substrate with the positioned MICROPACK onto the substrate holder of the pulse soldering device.

Lower, adjust and set down the soldering head onto the MICROPACK leads manually, then trigger the soldering pulse.

After the Pb/Sn solder becomes solidified (holding time, observation through stereo microscope) raise the soldering head and place the substrate onto an electrically conductive surface or in an appropriate tray.

Caution! Ceramic and glass substrates must be preheated and the stated temperatures must be maintained during the soldering process.

Ceramic: 150°C
Glass: 125°C

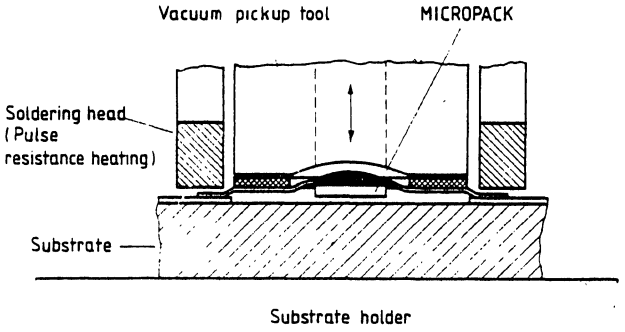
Neither preheating nor cooling may be sudden (danger of breakage).

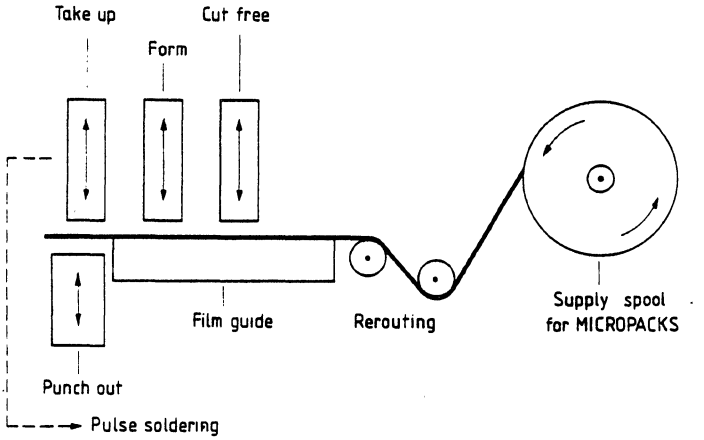
Cleaning (if required) as in I.

III. Large quantities
(e.g. approx. 30.0/year)

Recommended assembling method:
Semi-automatic pulse soldering

Principle





Required equipment and accessories

Semi-automatic pulse soldering device including tools for cutting, forming and punching.

Stereo microscope (magnification 6 to 40x).
Flux according to DIN 8511 (e.g. pure colophonium dissolved in alcohol).
Cleaning agents (if necessary): Freon T-P 35 and TF.

Soldering data

Soldering temperature at the pulse soldering head 230 °C max.
Soldering time: approx. 2 s plus an additional holding time of 1 s until the solder becomes solidified.

Procedure

Position the supply roll in the pulse soldering device.

Coat the mounting positions on the substrate with flux by hand or machine.

Position the substrate onto the substrate holder.

Caution! Ceramic and glass substrates must be preheated and the stated temperatures must be maintained during the soldering process.

Ceramic: 150 °C
Glass: 125 °C

Neither preheating nor cooling may be sudden (danger of breakage).

Machine-cut, form, punch and pre-adjust the MICROPACK.

Fine-adjust with micro-manipulator (under the stereo microscope or on a monitor).

Pulse-solder by machine.

Place the substrate onto an electrically conductive surface or in an appropriate tray.

Cleaning (if required): as in I.

IV. Very large quantities
(e.g. approx. 500.0/year)

Recommended assembling method:

Fully automatic pulse soldering

Processing method as in III. but fully automatic

Final inspection

It is recommended that a final visual inspection of the mounted MICROPACKs be included after soldering or cleaning, respectively (under the stereo microscope, magnification 6 to 40x).

Important criteria

The solder transition between the MICROPACK leads and the substrate traces should be concave tapered.

The connections to the semiconductor IC must not be damaged.

The solder on all substrate leads must be visibly melted.

MICROPACK and substrate surface must not show signs of soiling after soldering or cleaning, respectively.

Replacement

Experience shows that MICROPACKs can be replaced as many as five times depending on substrate material and layer construction.

Desolder the MICROPACK with miniature soldering iron or hot air gun and tweezers. The leads are heated to the melting point of the Pb/Sn solder and bent up with the tweezers.

Plane the mounting spots and recoat with flux.

Solder in a new MICROPACK using one of the methods described.

Manufacturers of assembly equipment for MICROPACKs

The following companies supply equipment for manual, semi-automatic and fully-automatic assembling:

1. Weld-Equip Sales b.v.
Engelseweg 217
5705 AE Helmond
Netherlands

Fa. Weld-Equip Deutschland
Josef-Retzer-Str. 47
8000 München 60
Phone (089) 883601/02

2. Fa. Farco Schweiz
Girardet 29
CH 2400 Le Locle
Phone (0041) 39318954

3. The Jade Cooperation
3063 Philmont Avenue
Huntingdon Vallery, Penna, 19006
USA

Jade Corp. USA, represented by Fa. BFI
Assar-Gabrielssonstraße 1 B
6057 Dietzenbach-Steinberg
Phone (06074) 27051

Data Conversion Components

SDA 5200 N
6-Bit Analog Digital Converter

Preliminary data

The SDA 5200 N is an ultrafast A/D converter with 6 bit resolution and overflow output. After cascading, it enables straightforward construction of 7 bit or 8 bit A/D converters, respectively (refer to application circuit).

Apart from a guaranteed strobe frequency of 100 MHz and excellent linearity, the SDA 5200 N has an outstanding analog bandwidth which — from the analog side — enables application up to the limit of the Nyquist theorem.

The SDA 5200 N is pin-compatible to the ICs SDA 5010, SDA 6020, and SDA 5200 S (differing output code in the overflow).

Main features

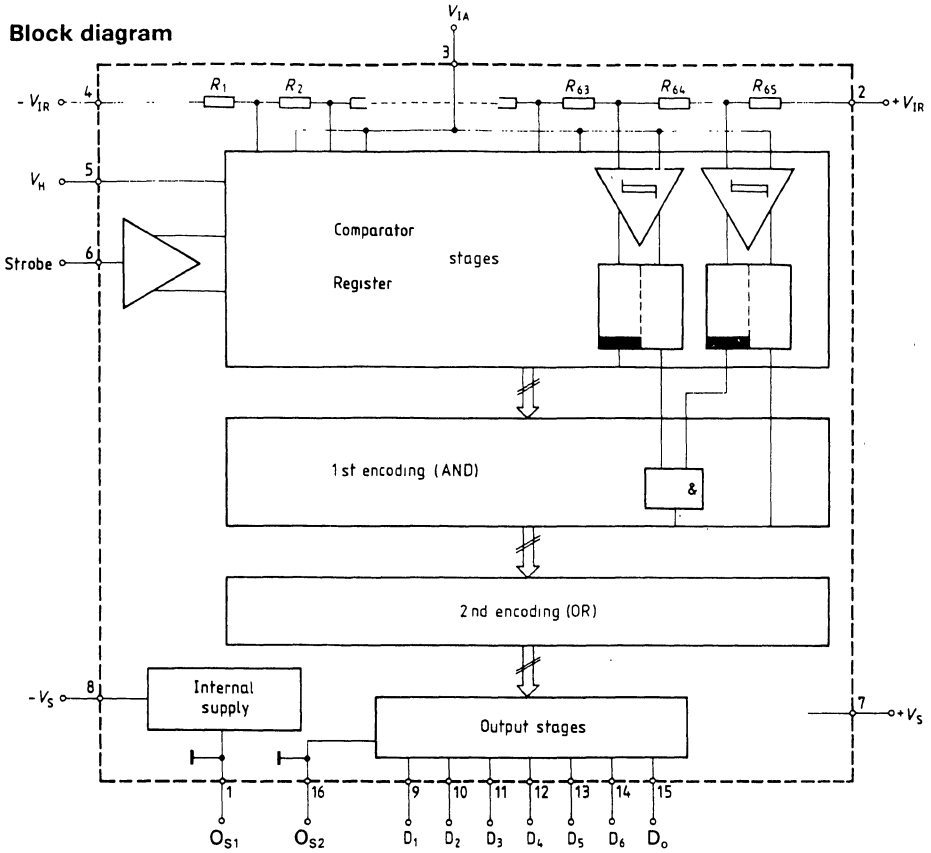
- Strobe frequency 100 MHz
- 6 bit resolution (1.6%)
- Overflow output (7th bit) at simultaneous blocking of the remaining outputs → simple cascading for 7 bit or 8 bit A/D converters
- Broad analog bandwidth (140 MHz)
- High slew rate of the input stages (typ. 0.5 V/ns)
- Processing of analog signals up to the Nyquist limit
- Linearity ± 1/4 LSB
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- Power dissipation 550 mW
- ECL compatible
- Logic compatible supply voltage +5 V; −5.2 V
- DIC 16 package

The following versions[1]) are available upon request:

- IC with a non-linear conversion characteristic of a given characteristic curve
- IC with any output code (e.g. gray code)

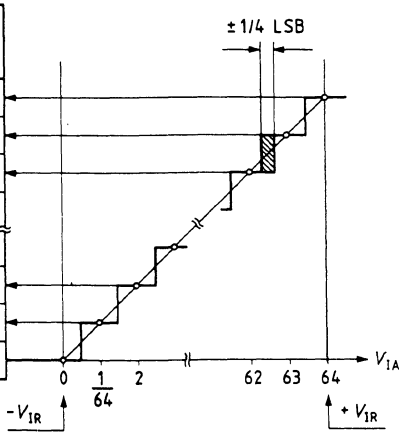
[1]) Conditions upon request

Block diagram

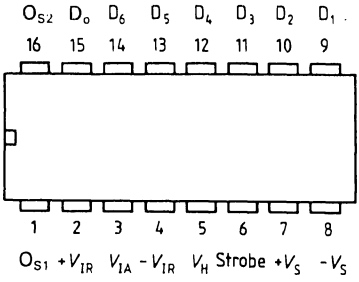


Signal chart

D_o	D_6	D_5	D_4	D_3	D_2	D_1
H	L	L	L	L	L	L
L	H	H	H	H	H	H
L	H	H	H	H	H	L
≈	≈	≈	≈	≈	≈	≈
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L



Pin configuration (Ceramic 16 pin DIL package)
(top view)



Pin	Symbol	Function
1	O_{S1}	Digital ground 1
2	$+V_{IR}$	Positive reference voltage (+2 V)
3	V_{IA}	Analog signal input (max. +2 V; −3 V)
4	$-V_{IR}$	Negative reference voltage (−3 V)
5	V_{IH}	Hysteresis control (0 V ... +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 ... 14	D_1 ... D_6	Data outputs, bits 1 ... 6 (ECL)
15	D_O	Overflow output
16	O_{S2}	Digital ground 2

Maximum ratings

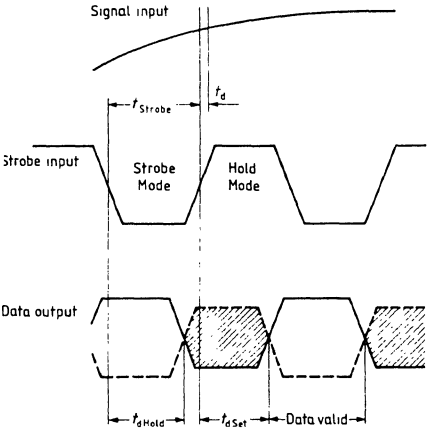
		Lower limit B	Upper limit A	Unit
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	V_{IA}, $+V_{IR}$, $-V_{IR}$	−3.5	2.5	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	V_{IH}	0	3.0	V
Voltage difference	$O_{S1}-O_{S2}$	−0.5	0.5	V
Operating temperature	T_{amb}	0	70	°C
Storage temperature	T_{stg}	−55	125	°C

Characteristics

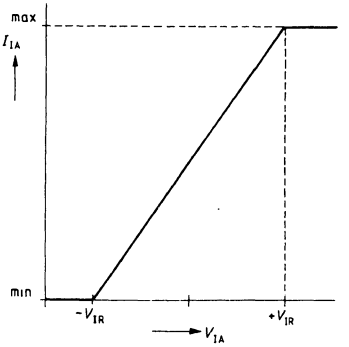
		Lower limit B	typ.	Upper limit A	Unit
Power supply					
Pos. supply voltage	$+V_S$	4.5	5.0	5.5	V
Neg. supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S$ = +5.0 V, $V_{IA} \leqq -V_{IR}$	I_{S+}		50	80	mA
at $-V_S$ = −5.2 V, $V_{IA} \leqq -V_{IR}$	I_{S-}		55	80	mA
Analog part					
Signal input					
Max. input voltage	V_{IAmax}	$-V_{IRmin}$		$+V_{IRmax}$	V
$V_{IAmax} = \lvert(+V_{IRmax}) - (-V_{IRmin})\rvert$				5	V
V_{IA} for 6 bit resolution			0.3		V
V_{IA} for ½ LSB linearity		1.2	0.6		V
V_{IA} for ¼ LSB linearity		2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$	I_{IA}		150	500	µA
at $V_{IA} < -V_{IR}$	I_{IA}	−500		500	nA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}		25		pF
Reference inputs					
Pos. reference voltage	$+V_{IR}$	−2.5		2	V
Neg. reference voltage	$-V_{IR}$	−3.0		1.5	V
Reference resistance	R_{Ref}	96	128	195	Ω
Digital part					
Strobe input					
H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.6	V
H input current	I_{IH}		6	50	µA
L input current	I_{IL}		6	50	µA
Data outputs (100 Ω to −2 V)					
H output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

Characteristics (cont'd)		Lower limit B	typ.	Upper limit A	Unit
Dynamic parameters					
Aperture time	t_d		2		ns
Aperture jitter			25		ps
t_{strobe}			5		ns
Signal transition time	$t_{d\ Hold}$		12	17	ns
Signal transition time	$t_{d\ Set}$		12	17	ns
Strobe frequency	f_{strobe}	100			MHz
Max. slew rate			0.5		V/ns
Bandwidth (−3 dB)	B		140		MHz

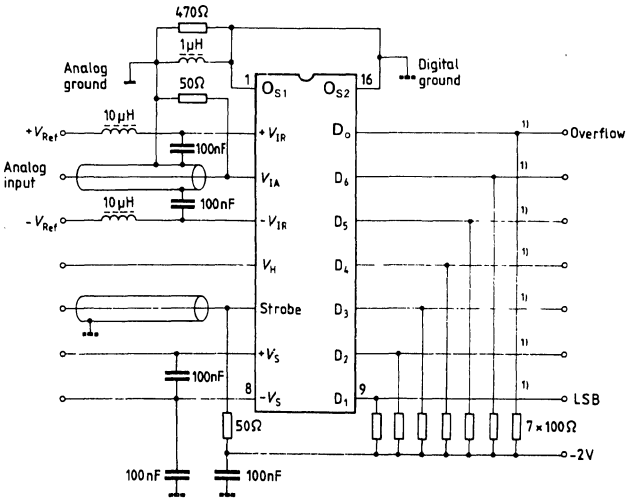
Pulse diagram of strobe input and data outputs



Input current versus input voltage



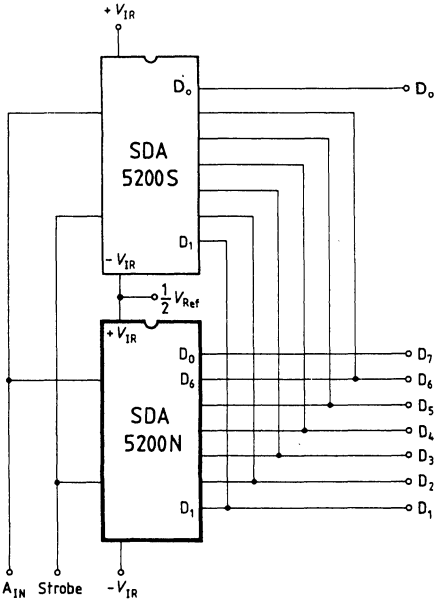
Test circuit



1) Lines carried out as microstrip

Application circuit

7 bit A/D converter with SDA 5200 S and SDA 5200 N



SDA 5200 S
6-Bit Analog Digital Converter

Preliminary data

The SDA 5200 S is an ultrafast 6 bit A/D converter with overflow output. It has been designed as terminating device for a 7 bit or 8 bit A/D converter comprising several cascaded ICs (refer to application circuit), or exclusively for 6 bit operation.

Apart from a guaranteed strobe frequency of 100 MHz and excellent linearity, the SDA 5200 S has an outstanding analog bandwidth which — from the analog side — enables application up to the limit of the Nyquist theorem.

The SDA 5200 S is pin-compatible to the ICs SDA 5010, SDA 6020, and SDA 5200 N (differing output code in the overflow).

Main features

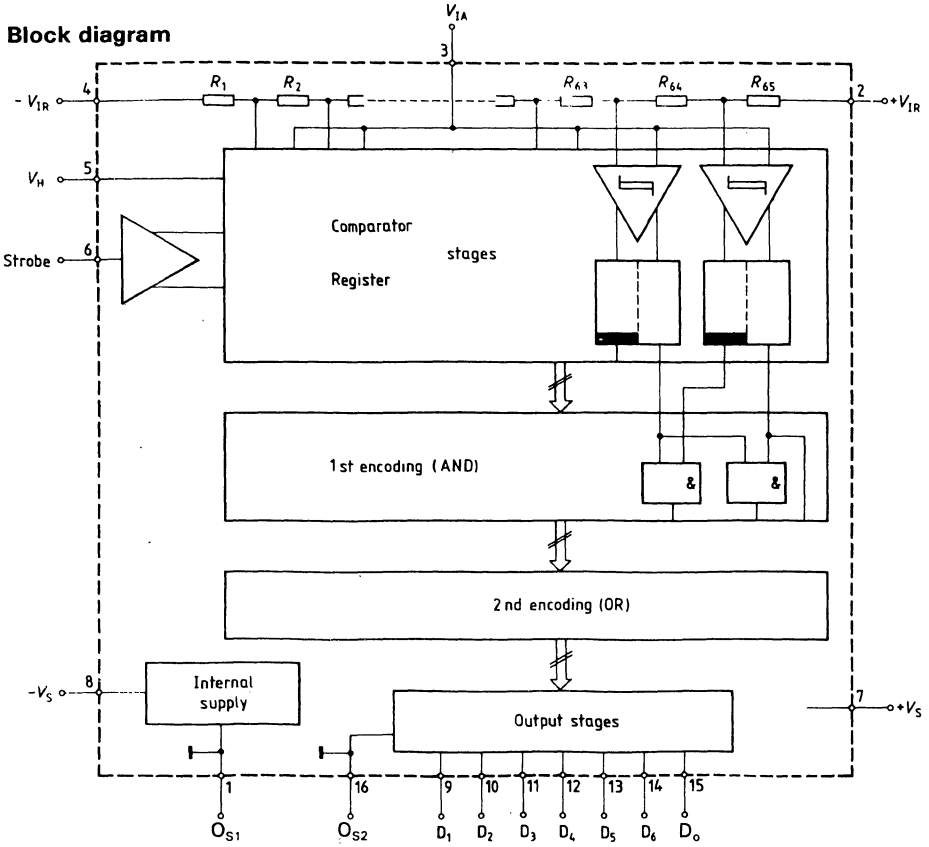
- Strobe frequency 100 MHz
- 6 bit resolution (1.6%)
- Overflow output (7th bit)
- Broad analog bandwidth (140 MHz)
- High slew rate of the input stages (typ. 0.5 V/ns)
- Processing of analog signals up to the Nyquist limit
- Linearity ± 1/4 LSB
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- Power dissipation 550 mW
- ECL compatible
- Logic compatible supply voltage +5 V; –5.2 V
- DIC 16 package

The following versions[1]) are available upon request:

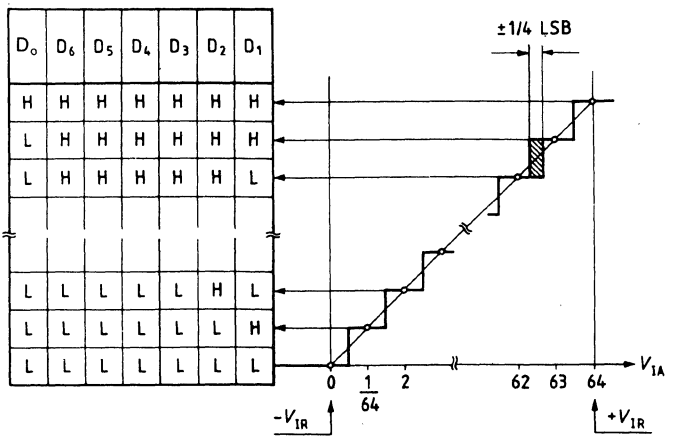
- IC with a non-linear conversion characteristic of a given characteristic curve
- IC with any output code (e.g. gray code)

[1]) Conditions upon request

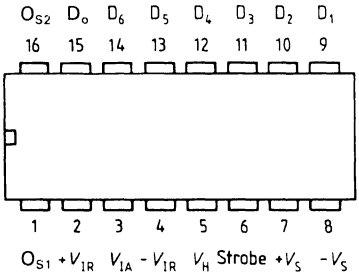
Block diagram



Signal chart



Pin configuration (Ceramic 16 pin DIL package)
(top view)



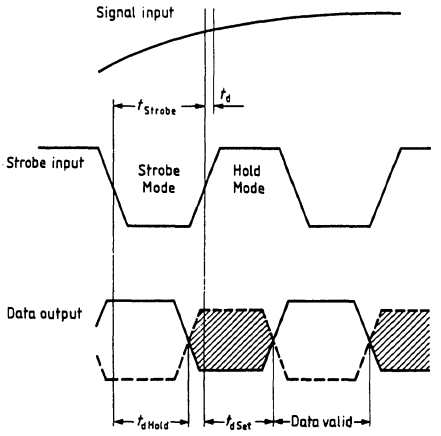
Pin	Symbol	Function
1	O_{S1}	Digital ground 1
2	$+V_R$	Positive reference voltage (+2 V)
3	V_{IA}	Analog signal input (max. +2 V; −3 V)
4	$-V_{IR}$	Negative reference voltage (−3 V)
5	V_{IH}	Hysteresis control (0 V ... +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 ... 14	D_1 ... D_6	Data outputs, bits 1 ... 6 (ECL)
15	D_O	Overflow output
16	O_{S2}	Digital ground 2

Maximum ratings		Lower limit B	Upper limit A	Unit
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	V_{IA}, $+V_{IR}$, $-V_{IR}$	−3.5	2.5	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	V_{IH}	0	3.0	V
Voltage difference	$O_{S1}-O_{S2}$	−0.5	0.5	V
Operating temperature	T_{amb}	0	70	°C
Storage temperature	T_{stg}	−55	125	°C

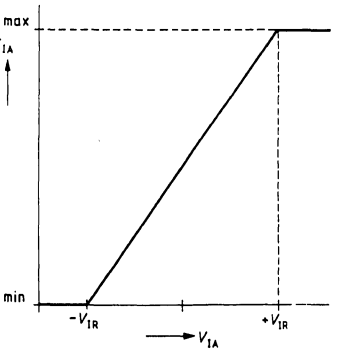
Characteristics		Lower limit B	typ.	Upper limit A	Unit
Power supply					
Pos. supply voltage	$+V_S$	4.5	5.0	5.5	V
Neg. supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S$ = +5.0 V, $V_{IA} \leqq -V_{IR}$	I_{S+}		50	80	mA
at $-V_S$ = −5.2 V, $V_{IA} \leqq -V_{IR}$	I_{S-}		55	80	mA
Analog part					
Signal input					
Max. input voltage	V_{IAmax}	$-V_{IRmin}$		$+V_{IRmax}$	V
$V_{IAmax} = \lvert(+V_{IRmax}) - (-V_{IRmin})\rvert$				5	V
V_{IA} for 6 bit resolution			0.3		V
V_{IA} for ½ LSB linearity		1.2	0.6		V
V_{IA} for ¼ LSB linearity		2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$	I_{IA}		150	500	µA
at $V_{IA} < -V_{IR}$	I_{IA}	−500		500	nA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}		25		pF
Reference inputs					
Pos. reference voltage	$+V_{IR}$	−2.5		2	V
Neg. reference voltage	$-V_{IR}$	−3.0		1.5	V
Reference resistance	R_{ref}	96	128	195	Ω
Digital part					
Strobe input					
H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.6	V
H input current	I_{IH}		6	50	µA
L input current	I_{IL}		6	50	µA
Data outputs (100 Ω to −2 V)					
H output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

Characteristics (cont'd) **Dynamic parameters**		Lower limit B	typ.	Upper limit A	Unit
Aperture time	t_d		2		ns
Aperture jitter			25		ps
t_{strobe}			5		ns
Signal transition time	$t_{d\ Hold}$		12	17	ns
Signal transition time	$t_{d\ Set}$		12	17	ns
Strobe frequency	f_{strobe}	100			MHz
Max. slew rate			0.5		V/ns
Bandwidth (–3 dB)	B		140		MHz

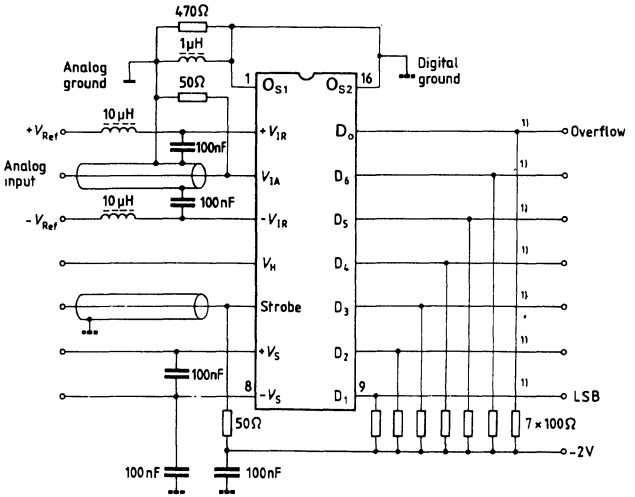
Pulse diagram of strobe input and data outputs



Input current versus input voltage



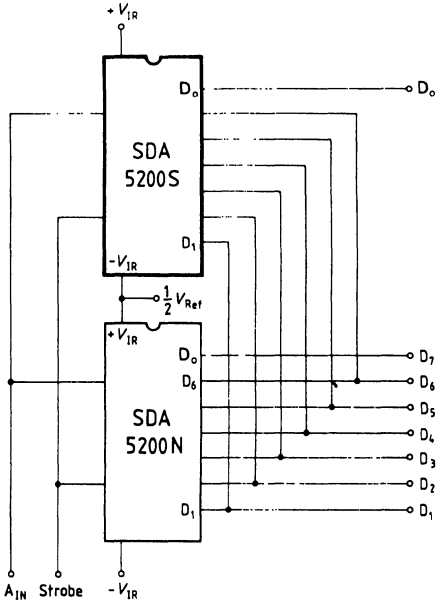
Test circuit



[1]) Lines carried out as microstrip.

Application circuit

7 bit A/D converter with SDA 5200 S and SDA 5200 N



SDA 6020
6-Bit Analog Digital Converter

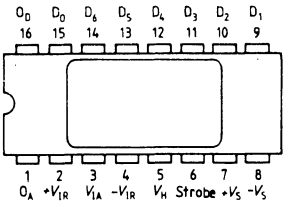
The SDA 6020 is an ultrafast A/D converter with 6 bit resolution. In addition to a strobe frequency of typically 50 MHz and excellent linearity, the SDA 6020 has the following outstanding features:

- 6-bit resolution (1.6%), simple expansion to 8 bits
- ±1/4 LSB linearity
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- ECL compatible (ECL – TTL matching possible, e.g. with SH 100.255)
- Low power dissipation 450 mW
- Logic compatible supply voltage +5 V; –5.2 V

Maximum ratings

		Lower limit B	Upper limit A	Unit
Supply voltage	$+V_S$	–0.3	6.0	V
Supply voltage	$-V_S$	–6.0	0.3	V
Input voltages	V_{IA}, $+V_{IR}$, $-V_{IR}$	–3.0	3.0	V
Strobe	V_{Strobe}	$-V_S$	0	V
Hysteresis control	V_{IH}	0	3.0	V
Voltage difference	$O_A - O_D$	–0.5	0.5	V
Operating temperature	T_{amb}	0	70	°C
Storage temperature	T_s	–55	125	°C

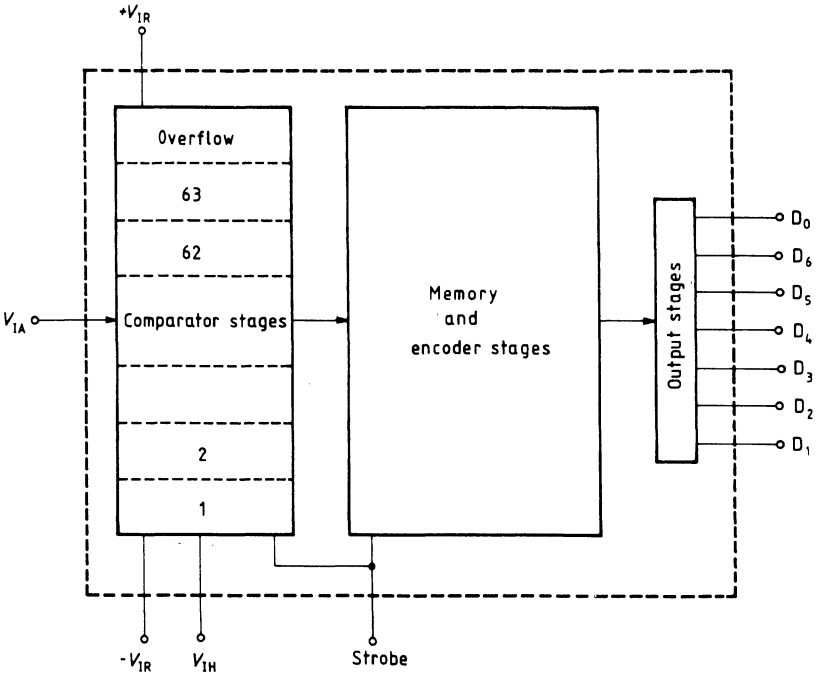
Pin configuration
(top view)



(Ceramic 16 pin DIL package)

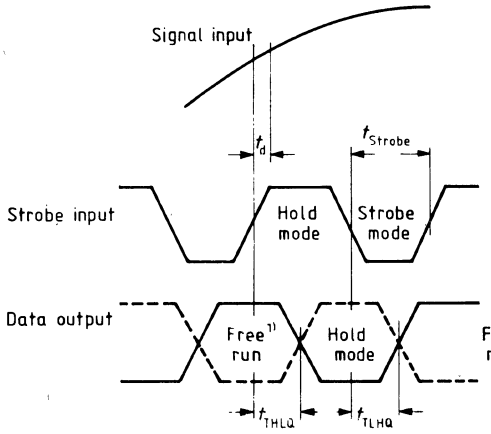
Pin	Symbol	Function
1	O_A	Anlog ground
2	$+V_{IR}$	Positive reference voltage (< +2.5 V)
3	V_{IA}	Analog signal input (max. ±2.5 V)
4	$-V_{IR}$	Negative reference voltage (> −2.5 V)
5	V_{IH}	Hysteresis control (0 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+6 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9–14	D_1–D_6	Data outputs bit 1 to 6 (ECL)
15	D_O	Overflow
16	O_D	Digital ground

Block diagram



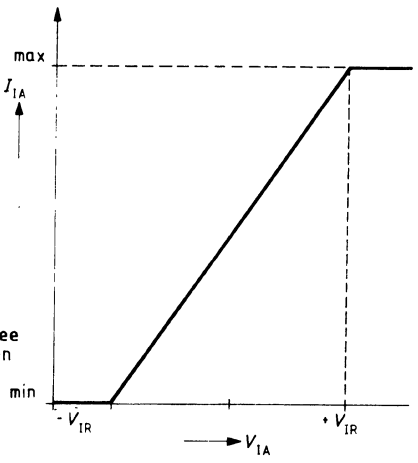
Characteristics		Lower limit B	typ.	Upper limit A	Unit
Power supply					
Pos. supply voltage	$+V_S$	4.5	5.0	5.5	V
Neg. supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S$ = +5.0 V; $V_{IA} \leqq -V_{IR}$	I_S		30	60	mA
at $-V_S$ = −5.2 V; $V_{IA} \leqq -V_{IR}$	I_S		55	80	mA
Analog part (T_{amb}=25 °C,$+V_S$=5V,$-V_S$=−5.2V)					
Signal input					
Max. input voltage	$V_{IA\,max}$	$-V_{IR\,min}$		$+V_{IR\,max}$	V
$V_{IA\,max} = \lvert + V_{IR\,max} - -V_{IR\,min}\rvert$				5	V
V_{IA} for 6 bit resolution			0.3		V
V_{IA} for 1/2 LSB linearity		1.2	0.6		V
V_{IA} for 1/4 LSB linearity		2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$ in sample mode	I_{IA}		200	800	µA
at $V_{IA} = <-V_{IR}$ in sample mode	I_{IA}	−10		10	µA
$-V_{IR} < V_{IA} < +V_{IR}$ in hold mode	I_{IA}	−10		10	µA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}		35		pF
Reference inputs					
Pos. reference voltage	$+V_{IR}$	−2		2.5	V
Neg. reference voltage	$-V_{IR}$	−2.5		2	V
Reference resistance	64 R	96	128	256	Ω
Digital part					
Strobe input					
H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.5	V
H input current	I_{IH}	5	30	100	µA
L input current	I_{IL}	5	30	100	µA
Data outputs (100 Ω to − 2 V)					
H output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V
Dynamic parameters					
Aperture time	t_d		2		ns
Aperture jitter			25		ps
Strobe	t_{Strobe}	15	8		ns
Signal transition time	t_{THLQ}		12	20	ns
Signal transition time	t_{TLHQ}		12	20	ns
Scanning frequency	f_{Strobe}	50			MHz

Pulse diagram of strobe inputs and data output

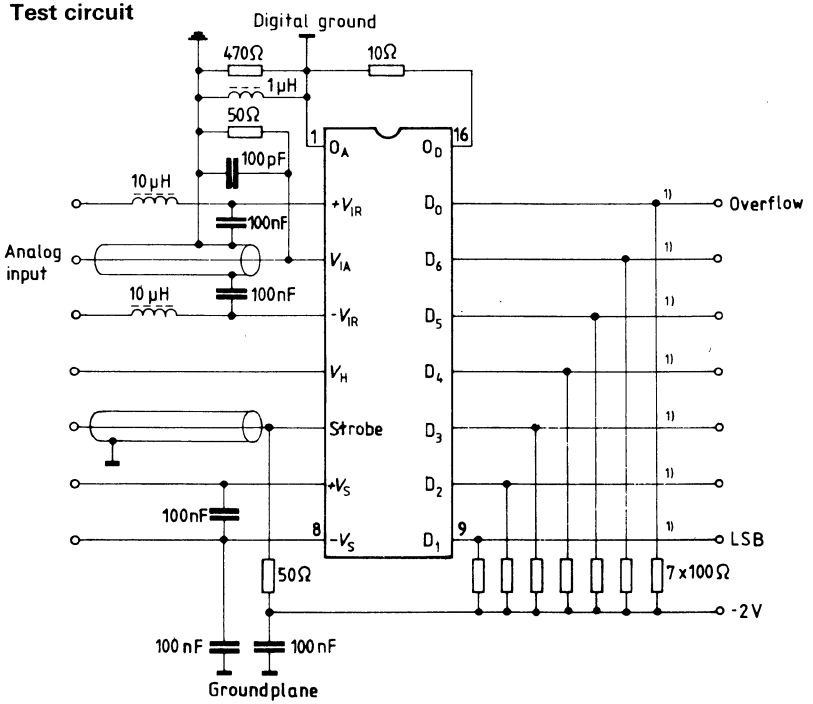


1) undefined output levels

Input current versus input voltage

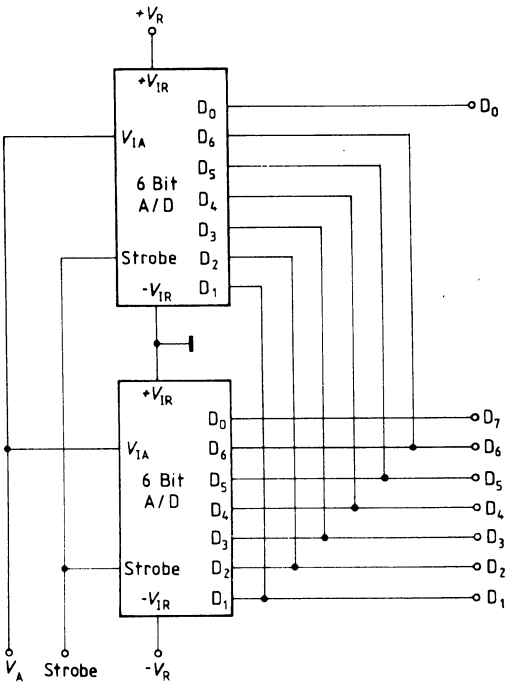


Test circuit

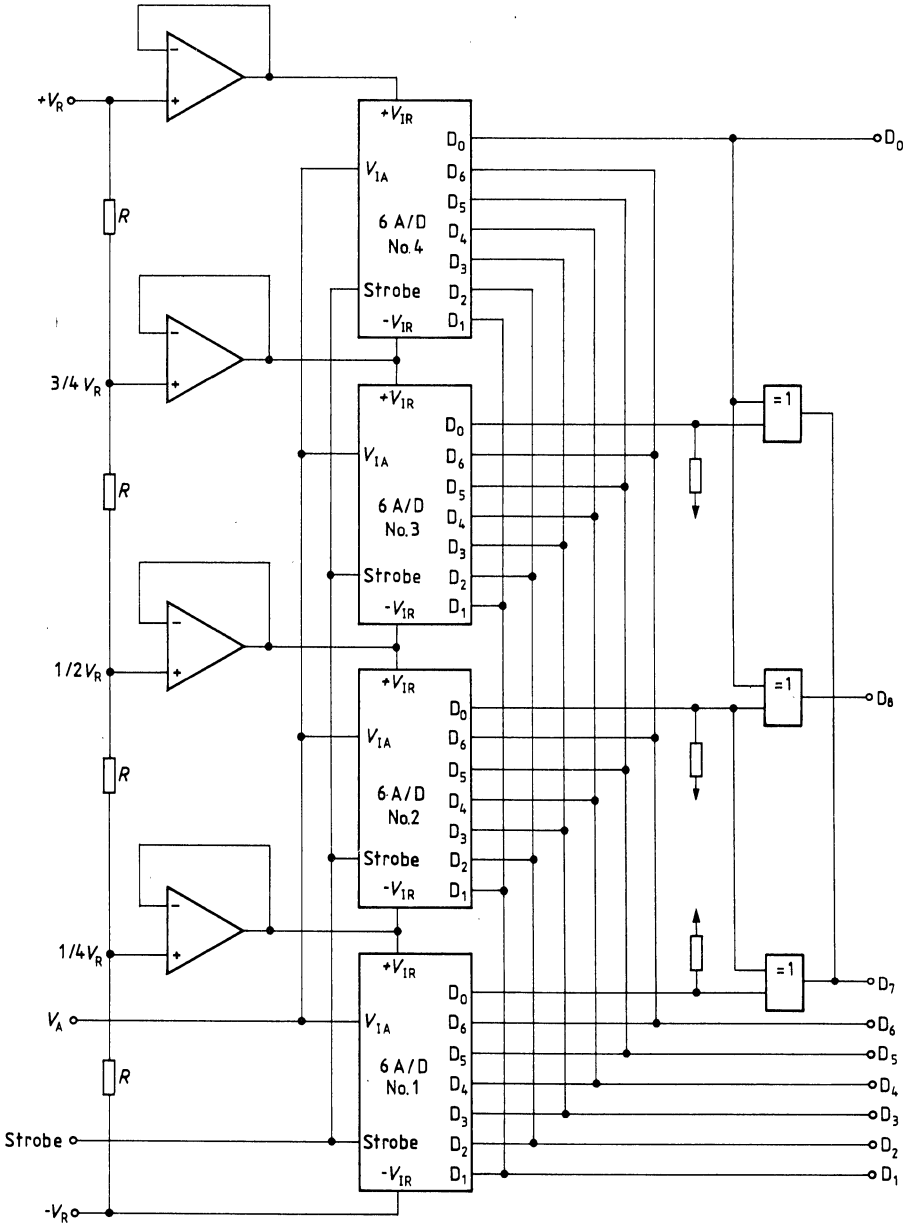


1) Lines effected as Microstrip

Circuit example for expansion to 7 bit



Circuit example for expansion to 8 bit



SDA 8005
8-Bit/7 ns Analog Digital Converter

Preliminary data **Bipolar circuit**

The SDA 8005 is a high speed D/A converter with excellent dynamic characteristics, it offers the following features:

- Settling time typ. 7 ns
- Extremely small glitch area
- Digital input register
- Data inputs 10 K and 100 K ECL compatible
- Single power supply: –5.2 V
- Deglitch control input

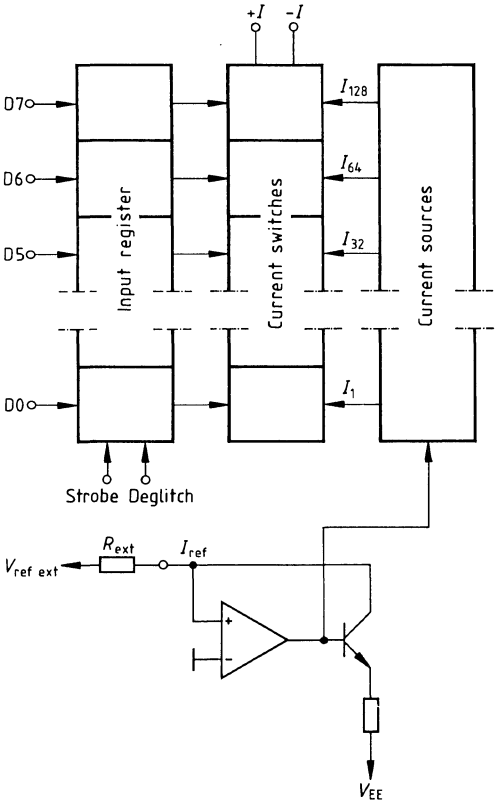
Functional description

The SDA 8005 is a high speed 8 bit D/A converter with ECL compatible data and strobe inputs.

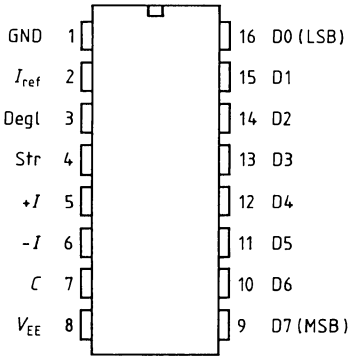
The data word is received in the input buffer by the low active strobe. An external reference voltage source with a reference resistor is needed. At a reference current of 2.5 mA the full scale output current amounts to 40 mA.

The output glitches can be minimized by adjusting the deglitch input voltage between −2.3 V and −2.9 V. The deglitch input can also be left open.

Block diagram



Pin configuration (Ceramic 16 pin DIL package)
top view



Pin designation

Pin No.	Symbol	Function
1	GND	Ground
2	I_{ref}	Reference current input
3	Degl	Deglitch input
4	Str	Strobe
5, 6	$+I$, $-I$	Complementary current outputs $+I$: zero current if D0 to D7 are high
7	C	Stabilization
8	V_{EE}	Supply voltage –5.2 V
16 ... 9	D0 ... D7	Data input 0 (LSB) to 7 (MSB)

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_{EE}	−6.0	0.3	V
Input voltages	$V_{D0...D7}$	−3.0	0	V
Strobe input voltage	V_{Str}	−4.0	0	V
Deglitch input voltage	V_{Degl}	−5.2	0	V
Output voltages, $+I$, $-I$	V_{QI+}, V_{QI-}	−1.9	5	V
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Ambient temperature	T_{amb}	−25	85	°C
Thermal resistance	R_{thJU}		85	K/W

Characteristics

Analog outputs

Static performance

		Lower limit B	typ.	Upper limit A	
Ratio full scale output current to reference current	I_{QFS}/I_{ref}		16		
Absolute unadjusted error	ERR	−1		+1[2])	%
Integrale nonlinearity	I NL		0.40[1])	0.55[2])	LSB
Differential nonlinearity	D NL		0.6[1])	1[2])	LSB
Full scale temperature coefficient					
−25°C to +25°C	TC	80		120	ppm/°C
+25°C to +85°C	TC	50		80	ppm/°C
Zero code output current	I_{QO}		6[1])	30[3])	µA
Full scale output current	$I_{Q\,FS}$			40[2])	mA
Output voltage range	V_Q	−1.4		+5	V
Supply voltage sensitivity	S_{VS}		0.03[1])	0.04[2])	%/%

Dynamic performance[1])

Output rise time	t_{rQ}		1.3		ns
Output settling time	t_{sQ}		7		ns
Adjusted worst case glitch area			80		pVs
Digital crosstalk					
Data	a_{Data}		15[4])		pVs
Strobe	a_{Strobe}		30[4])		pVs

Comments see page 896

Characteristics		Lower limit B	typ.	Upper limit A	
Digital inputs					
DC characteristics					
H input voltage	V_{IH}	−1.105		−0.810	V
L input voltage	V_{IL}	−1.850		−1.505	V
Input capacitance D7	$C_{I\,D7}$		1.2		pF
D6	$C_{I\,D6}$		0.8		pF
D0 to D5	$C_{I\,D0...D5}$		0.5		pF
Strobe	$C_{I\,Str}$		1.5		pF
H input voltage D7	$I_{IH\,D7}$		25		µA
D6	$I_{IH\,D6}$		12		µA
D0 to D5	$I_{IH\,D0...D5}$		6		µA
Strobe	$I_{IH\,Str}$		75		µA
Input coding			binary		
Switching characteristics					
Setup time	t_S	0.5			ns
Hold time	t_H	2.5			ns
Strobe time (see **Fig. 1**)	t_{Str}	2			ns
Deglitch input					
Deglitch input current at V_{Degl} = 2.3 V	$I_{I\,Degl}$			200	µA
at V_{Degl} = 2.9 V	$I_{I\,Degl}$	−150			µA
Deglitch voltage range	V_{Degl}	−2.9		−2.3	V
Deglitch voltage (not connected)	V_{Degl}		0.5xV_{EE}		V
Power supply[1])					
Supply voltage	V_{EE}	−5.46		−4.94	V
Supply current	I_{EE}		98		mA
Power consumtion	P_D		495		mW

Comments

[1]) Measured at
25°C
V_{EE} = −5.2 V
Full scale output current I_Q = 20 mA
Output loads = 50 Ω

[2]) Quaranteed at
−25°C bis +85°C
−5.46 V to −4.94 V
Full scale output current I_Q = 1 mA to 40 mA

[3]) Measured at
100°C
Full scale output current I_Q = 20 mA
V_{Degl} = −2.3 V
V_{EE} = −5.2 V

[4])
V_{IH} = −0.95 V
V_{IL} = −1.6 V
Input signal rise time t_r = 3 ns

Switching all inputs at the same time in the same direction (worst case)

The crosstalk can be reduced by using other input signals.

Pulse diagram of the inputs

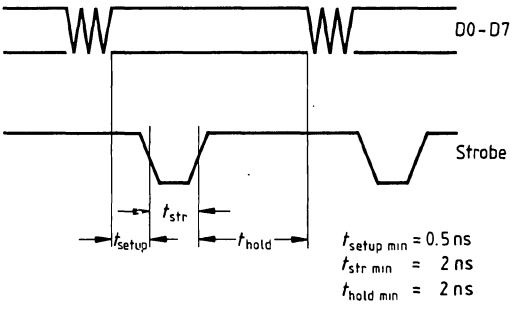


Figure 1

Terminology

Absolute unadjusted error

The full scale output current with the same reference voltage and reference resistance is different for different chips. The variation results from the deviation of technology parameters. The specification is the maximum deviation from an average value.

Integral nonlinearity

The integral nonlinearity is the maximum deviation of the output from a linear regression over the output values of all possible input codes.

Differential nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent input codes. A specified differential nonlinearity of ± 1 LSB max. over the operating temperature range ensures monotonicity.

Supply voltage sensitivity

The supply voltage sensitivity is the dependence of the analog output current on the supply voltage V_{EE} with all other parameters constant. It is specified in % per %.

Output rise time

The output rise time is the time between the 10% value and the 90% value of V_Q max. at the leading edge.

Output settling time

The output settling time is the time from the trailing strobe edge (50% point) to the time when the analog output signal is within ± 1/2 LSB of the final value.

The specified value is measured by using a comparator to detect the entry time point (see **fig. 2**).

Adjusted worst case glitch area

Glitches which arise from input code switching can be minimized by varying the deglitch input voltage.

The specified value can be measured under following conditions:

- input code change from 0111 1111 to 1000 0000 and viceversa
- input data are received with strobe
- deglitch input voltage is optimized for switching in both directions

Figure 2 shows the test circuit and the timing diagram for the determination of the output settling time.

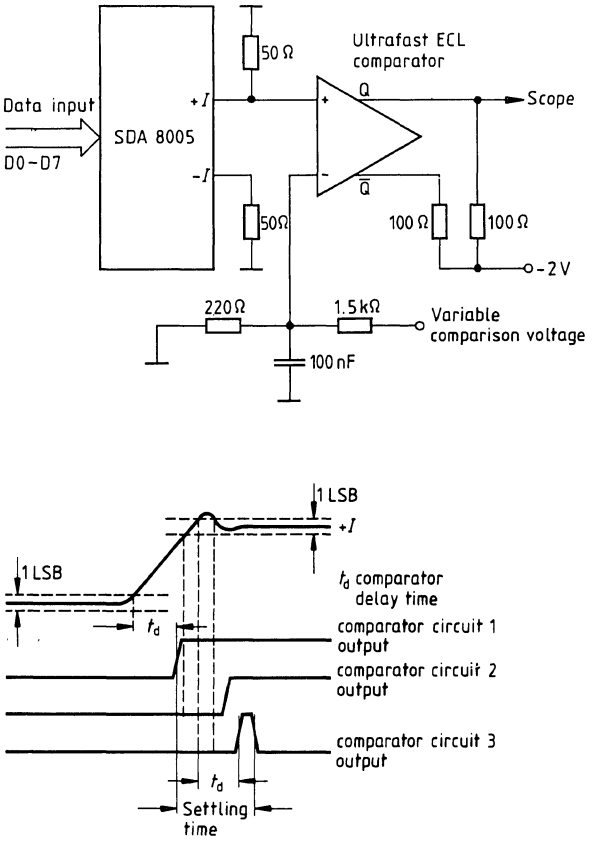


Figure 2

Application instructions

- Board with at least one ground area in its entirety
- Ground-pin should be connected nearby the large ground area by using contact studs or by direct soldering.
- Voltage supply must be blocked directly at the V_{EE}-pin by using a 100 nF ceramic capacitor (preferably use a chip capacitor).
- The analog outputs should be loaded with 50 Ω as near as possible at the package.
- The DC voltages (V_{EE}, *DEGL*, V_{ref}) have to be checked to ensure low ripple and noise.
- To minimize the crosstalk of Strobe to the output you can place a voltage divider at the Strobe input to build up an RC filter in combination with the input capacitance (see **figure 4**).
- To connect the D/A-converter output to the 50 Ω input of the scope, the line has to be terminated on the D/A-converter side to prevent reflections. The ground-connection between the board and the instrument should have a very low impedance.

  The ground-connection between the board and the instrument should have a very low impedance.

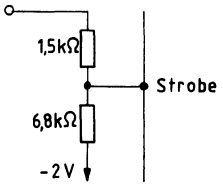


Figure 3 shows an application where the output signal is transmitted over a 50 Ω line to a receiver with a 50 Ω input, such as a high speed oscilloscope.

I_{ref} may be adjusted by varying V_{ref} between 0 V and 2.5 V, when the reference resistor (R_{ref}) is 1 kΩ.

Alternatively, the R_{ref} value can be changed with V_{ref} constant.

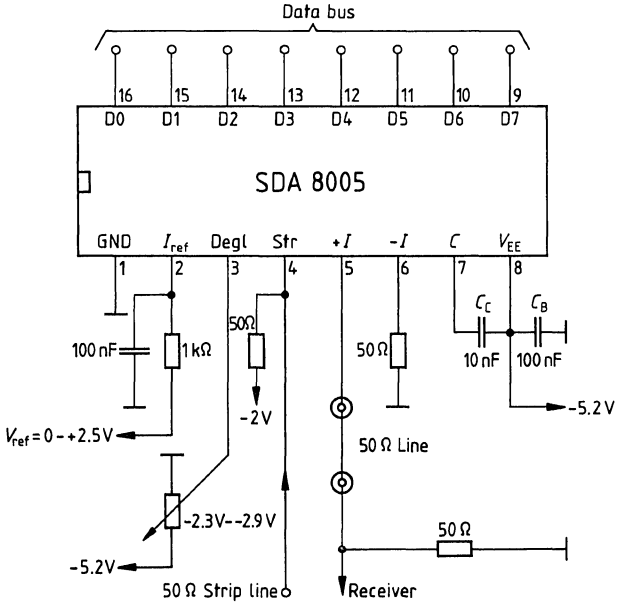


Figure 3

Here the strobe input is connected to a voltage divider, which forms an RC filter together with the input capacitance, and in this way reduces the digital crosstalk from strobe to output. The 100 Ω output line from $+I$ is terminated on both ends.

The full scale output current in this case also allows an acceptable voltage range.

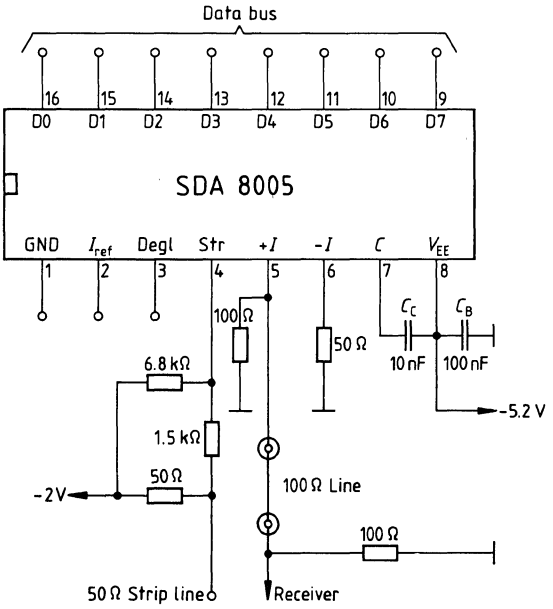


Figure 4

SDA 8010
8-Bit Analog Digital Converter

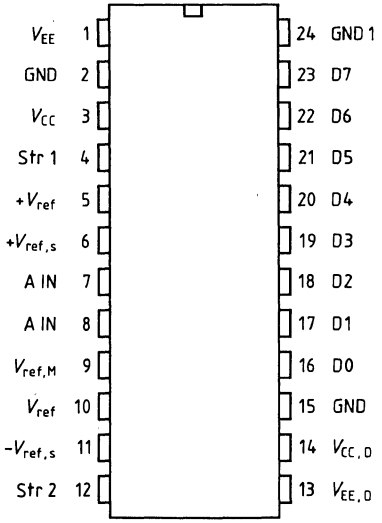
Preliminary information **Bipolar circuit**

The SDA 8010 is an ultra-fast A/D converter according to the parallel principle, with a resolution of 8 bits and a guaranteed strobe frequency of 100 MHz. The component is comprised of 11,000 elements and is produced in a highly modern bipolar technology. The SDA 8010 features a wide analog bandwidth, low input capacitance and an input voltage range symmetrical to ground.

Main features

- 100 MHz strobe frequency
- 8 bit resolution
- Excellent large signal bandwidth
- High input stage slew rate
- Symmetrical input voltage range
- Compatible with ECL 100 K
- Low power dissipation approx 1.3 W only
- Logic compatible supply voltage –4.5 V; + 5 V

Pin configuration (Ceramic 24 pin DIL package)
top view



Pin designation

Pin No.	Symbol	Function
1	V_{EE}	Neg. supply voltage, analog part
2	GND	Ground
3	V_{CC}	Pos. supply voltage, analog part
4	Str 1	Strobe signal 1
5	$+V_{ref}$	Pos. reference voltage
6	$+V_{ref,s}$	Pos. reference voltage sense
7	A IN	Analog input
8	A IN	Analog input
9	$V_{ref,M}$	Center tap of voltage divider
10	$-V_{ref}$	Neg. reference voltage
11	$-V_{ref,s}$	Neg. reference voltage sense
12	Str 2	Strobe signal 2
13	$V_{EE,D}$	Neg. supply voltage, digital part
14	$V_{CC,D}$	Pos. supply voltage, digital part
15	GND	Ground
16–23	D0 ... D7	Digital output signal
24	GND 1	Ground connection for output emitter fallower

Functional description

The SDA 8010 is an ultra-fast AD-Converter according to the parallel priciple and consists of a field of 255 comparators, three encoding stages and the output drivers (see block diagram).

The analog signal is routed via input A IN in parallel to all comparators and compared with 255 reference voltages spread linearly over the input voltage range. The result of this comparison, pending in the so-called thermometer code, is converted into the binary representation by way of three encoding stages, and is available as a digital signal with ECL level at outputs D0 ... D7.

The reference voltages are generated internally by means of a resistance divider. The potentials at its end points are set via the reference voltage inputs $+V_{ref}$ and $-V_{ref}$, and determine the input voltage range, which is resolved with a resolution of 8 bit. Additional potential terminals, $+V_{ref,\,sense}$ and $-V_{ref,\,sense}$, that enable a precise adjustment of the input voltage, independent of transition resistances, according to the principle of a Kelvin connection are provided at the reference voltage inputs according to this resolution. The assignment of the input signal, referenced to 1 LSB $= |+V_{ref}| + |-V_{ref}|/256$, to the digital output code is shown in the signal table. As no overflow function is provided, the output signal will remain at a value of 255 after the input voltage range is exceeded.

The individual comparators consist of a differential amplifier as input, and a register stage, operating in master-slave operation, which are activated alternately by strobe signals Str 1 and Str 2. The sequence of the conversion process is described according to the pulse diagram.

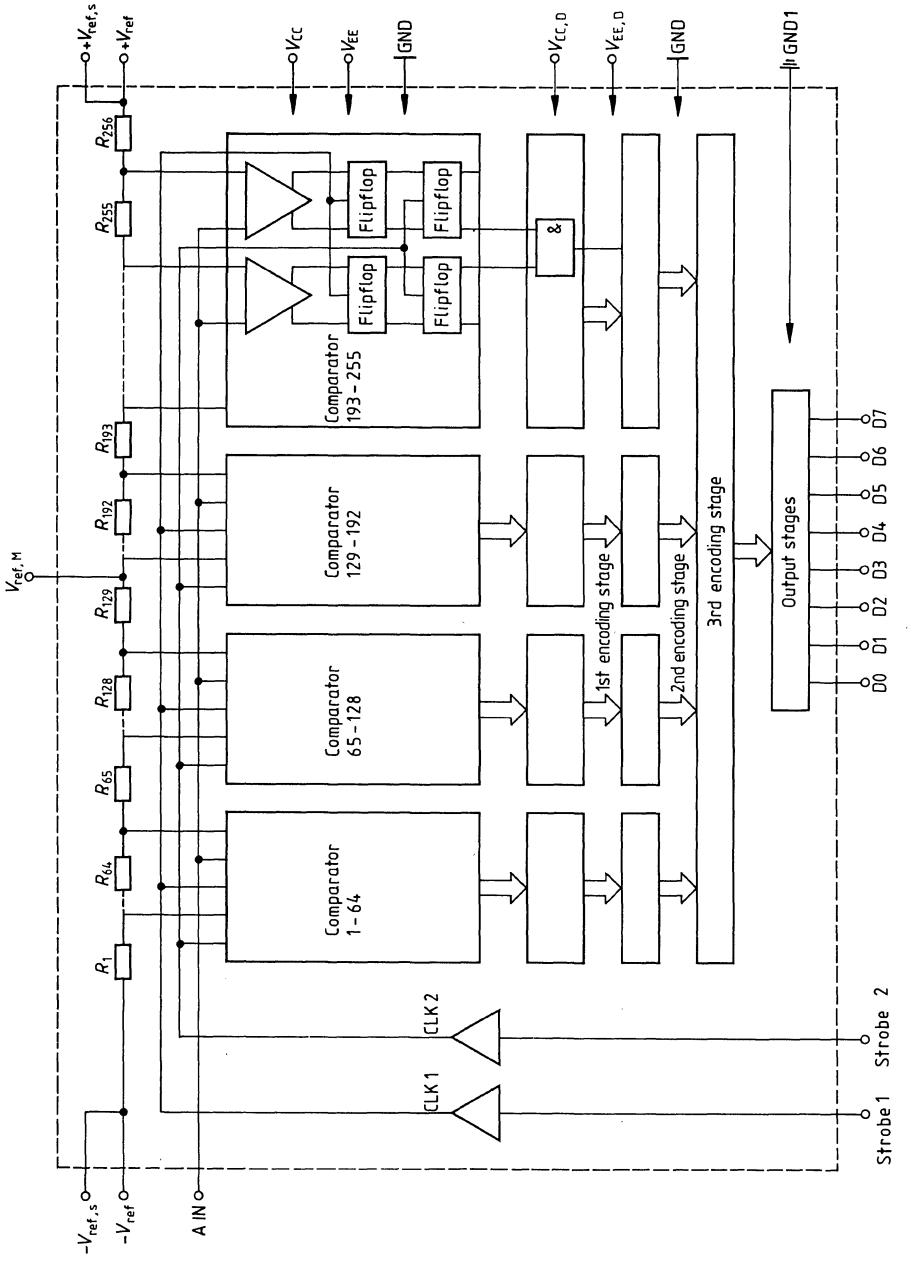
During the L-phase of signal Str 1, the analog signal is compared with the reference voltages. With the rising edge of Str 1, the result of the comparison is passed into the first register stage and held there until the falling edge of the strobe. Toward the end of this hold period t_{H1}, the signal is accepted into the second flipflop with the L phase of the second strobe Str 2, and stored with the rising edge. After a delay period t_d this data is pending at the output.

The validity range $t_{V,\,Q}$ of the output data depends on the duty cycle set at Str 2. In general, data will also be pending outside this interval $t_{V,\,Q}$. As, however, the second comparator latch is transparent in this phase, rise processes of the first stage could reach the output for especially critical settings.

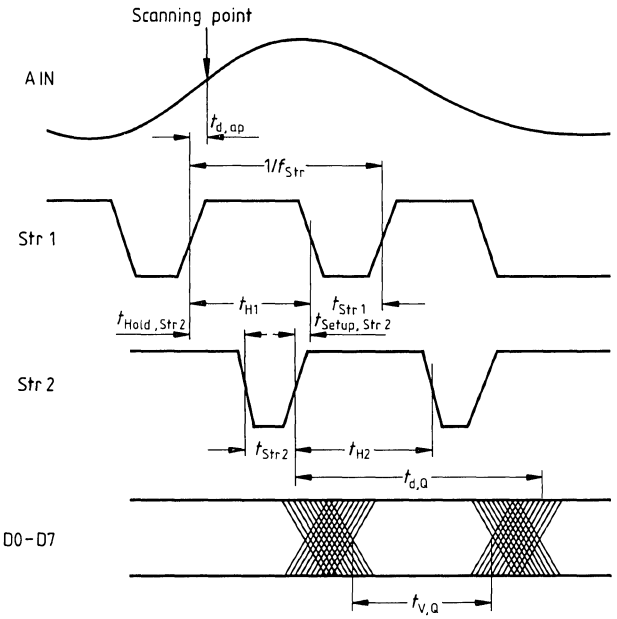
Essential for the analog features is that the input differential amplifier of the comparators is free of current at no time during the strobe process, so that on the one hand, an coupling of the strobe on to the input is prevented, and on the other hand, excellent large signal bandwidths are achieved. The low input capacitance of 30 pF and the input voltage range symmetrical about 0 V, in many cases permit the operation of the converter in 50 Ω systems. The dual design of the analog input A IN assures a low inductance lead and also plays a part in achieving a flat frequency response up to 50 MHz.

Connection $V_{ref,\,M}$ serves to HF decouple the reference voltage divider. The use of two supply systems V_{CC}, V_{EE} and $V_{CC,\,D}$, $V_{EE,\,D}$ and an additional ground lead GND 1 for the output stages reduces the cross influence of analog and digital signal to a minimum. Additionally, the separate return of the analog signal ground lead, the so-called analog ground is recommended (see test circuit).

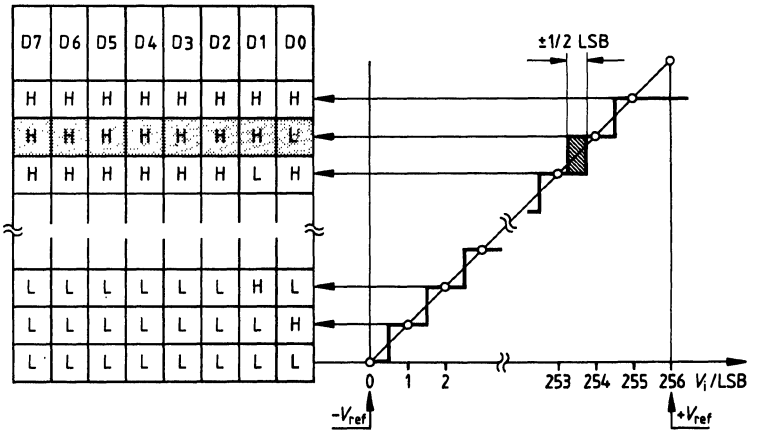
Block diagram



Pulse diagram



Transfer characteristic and truth table



Maximum ratings

		Lower limit B	Upper limit A	
Pos. supply voltages	V_{CC}, $V_{CC,\,D}$	−0.3	6.0	V
Neg. supply voltages	V_{EE}, $V_{EE,\,D}$	−6.0	0.3	V
Analog input voltages	$+V_{ref}$, $-V_{ref}$ $V_{A\,IN}$	−2.5	1.5	V
Digital input voltages	$V_{Str\,1}$, $V_{Str\,2}$	−3.5	0	V
Junction temperature	T_j		125	°C
Thermal resistance				
Junction-air (without dissipator)	R_{thJA}		50	K/W

Characteristics

		Lower limit B	typ.	Lower limit A	
Current supply					
Pos. supply voltage	V_{CC}, $V_{CC,\,D}$	4.75	5	5.25	V
Neg. supply voltage	V_{EE}, $V_{EE,\,D}$	−4.75	−4.5	−4.25	V
Current consumption at $V_{CC} = V_{CC,\,D} = 5$ V	$I_{CC} + I_{CC,\,D}$		180		mA
Current consumption at $V_{EE} = V_{EE,\,D} = 4.5$ V	$I_{EE} + I_{EE,\,D}$		90		mA
Analog part					
Reference inputs					
Pos. reference voltage	$+V_{ref}$	−1		1	V
Neg. reference voltage	$-V_{ref}$	−2		0	V
Reference resistance	256 R		130		Ω
Signal input					
Input voltage range (peak to peak)					
for 8 bit resolution	V_I		1		V
for 1/2 LSB linearity	V_I		1.5		V
Large-signal bandwidth[1])	B		50		MHz
Slew rate of input signal	SR		300		V/µs
Input capacity	C_I		30		pF
Input current[2])	I_I		400		µA

Comments see page 911

Characteristics

Digital part Strobe inputs		Lower limit B	typ.	Upper limit A	
H input voltage	V_{IH}	−1.165			V
L input voltage	V_{IL}			−1.475	V
Max. Strobe frequency[3]	$f_{Str,\ max}$	100			MHz
Strobe time 1	$t_{Str\ 1}$		4		ns
Aperture delay[4]	$t_{d,\ ap}$		3		ns
Strobe time 2	$t_{Str\ 2}$		2		ns
Setup time Strobe 2[5]	$t_{Setup,\ Str\ 2}$	0			ns
Hold time Strobe 2[5]	$t_{Hold,\ Str\ 2}$	3			ns

Characteristics		Lower limit	typ.	Upper limit	
Data outputs					
H output voltage	V_{QH}	−1.025			V
L output voltage	V_{QL}			−1.620	V
Signal transition time	$t_{d,\ Q}$		12		ns
Time of valid output data[6]	$t_{V,\ Q}$		5		ns

Comments

[1]) The large signal bandwidth is measured at a strobe frequency of 100 MHz with a sine-shaped input signal and with an amplitude of (peak to peak) 2 V in a 50 Ω system. The bandwidth is that input frequency at which either the amplitude value in the output signal has decreased by 1 dB over the low frequency value, or at which significant errors occur in the output code. If the voltage drop caused by the input capacitance being driven with 50 Ω is regulated out, or if a lower-ohmic input is used, the input bandwidth increases further.

[2]) The input current is linearly dependent on the input voltage. The stated value represents the input current at $V_{A\,IN} = +V_{ref}$.

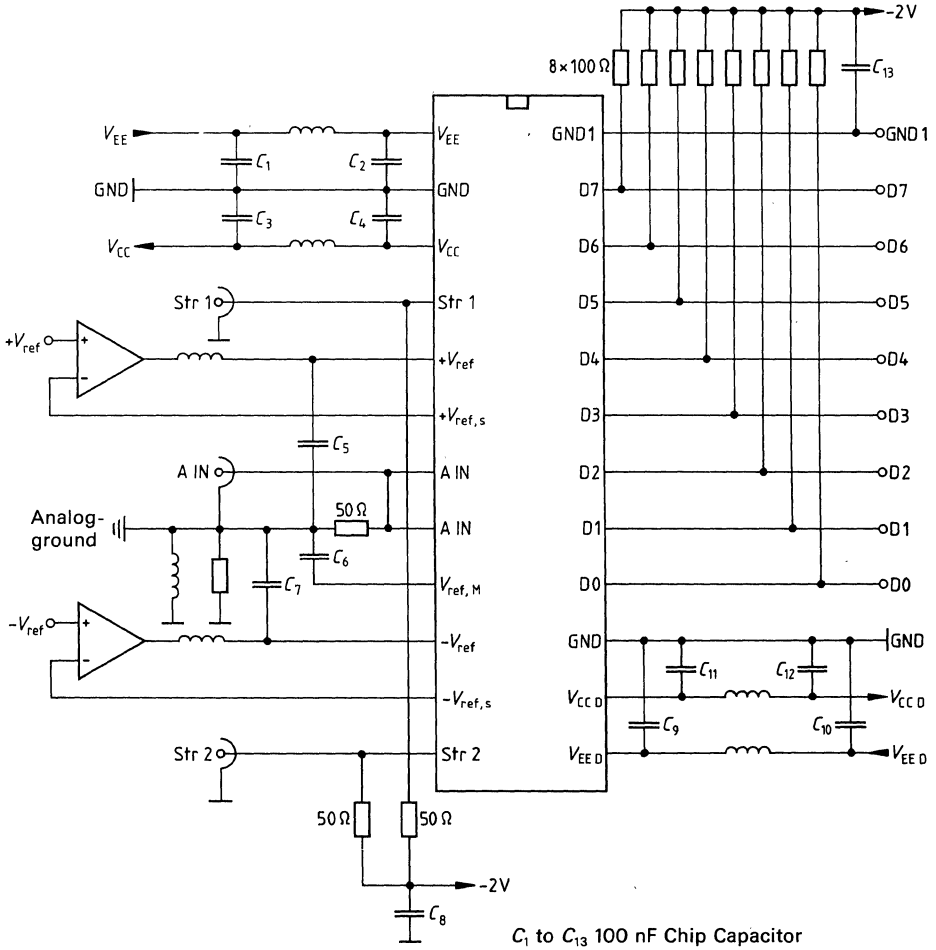
[3]) That strobe frequency up to which a sine-shaped input signal with an amplitude of (peak to peak) 2 V and a frequency of 50 MHz is reproduced without significant errors in the output code. The increase in signal-to-noise ratio with increasing analog frequency as a result of jitter of the sampling point and dynamic distortion is not considered.

[4]) As the sampling of the analog signal occurs with the edge of signal Str 1, no mention can be made here of an aperture period, but rather only of a delay ($t_{d,\,ap}$) of the sampling point.

[5]) This data describes a range for the adjustment of signal Str 2. The most favourable behavior of the output signals is achieved when the L-phase of signal Str 2 is selected as short as possible and placed at the end of the H-phase of signal Str 1.

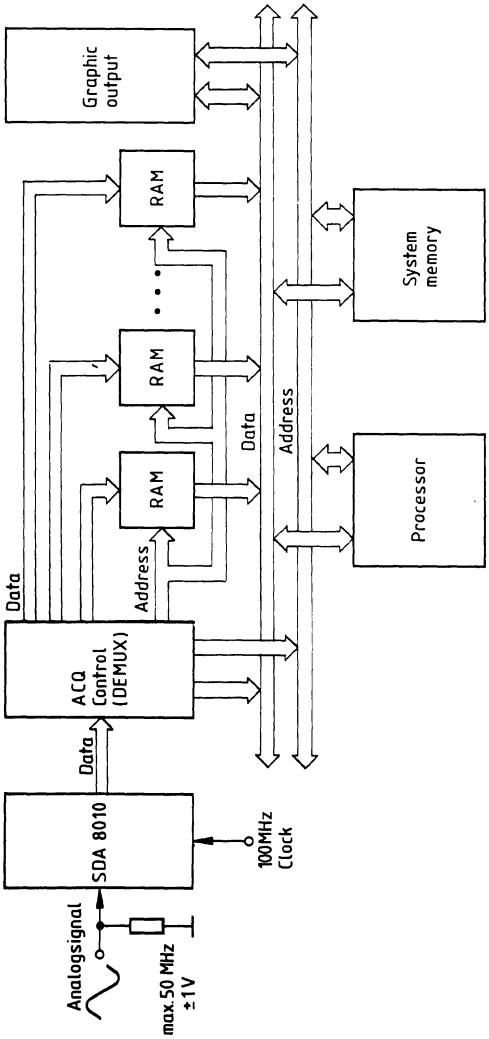
[6]) At f_{Str} = 100 MHz, $t_{Str\,2}$ = 2 ns and $t_{Setup,\,Str\,2}$ = 0.

Test circuit

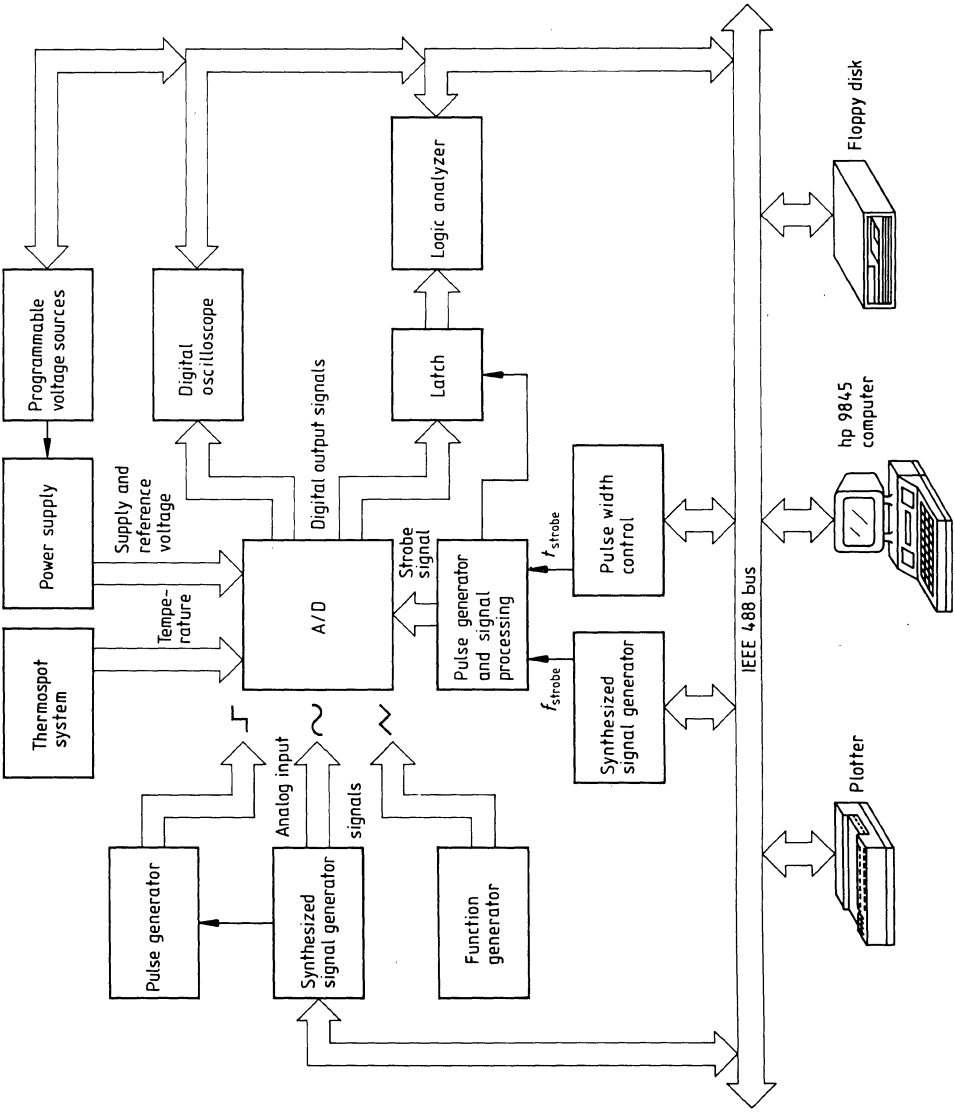


C_1 to C_{13} 100 nF Chip Capacitor

Application example



Computer supported test setup



Switched Mode Power Supply (SMPS) Components

TDA 4600-2/TDA 4600-2D Control IC for Switched-Mode Power Supplies

Bipolar IC

In addition to their use with TV receivers and video recorders, the ICs TDA 4600-2 and TDA 4600-2 D can be applied in power supplied of hi-fi sets and active speakers due to their wide operational ranges and superior voltage stability during high load changes.

Features

- Direct driving of switching transistor
- Low start-up current
- Reversing linear overload characteristic
- Collector current – proportional to base-current input

Maximum ratings

Supply voltage	V_9	20	V
Voltages			
reference output	V_1	6	V
identification input	V_2	± 0.6	V
controlled amplifier	V_3	3	V
collector current simulation	V_4	7	V
blocking input	V_5	7	V
base current cut-off point	V_7	V_9	V
base current amplifier output	V_8	V_9	V
Currents			
feedback, zero passage	$I_{i\,2}$	−3 to 3	mA
controlled amplifier	$I_{i\,3}$	−3 to 3	mA
collector current simulation	$I_{i\,4}$	5	mA
base current cut-off point	$I_{q\,7}$	1.5	mA
base current amplifier output	$I_{q\,8}$	−1.5	mA
Thermal resistances			
junction-air TDA 4600 – 2	$R_{th\,JA}$	70	K/W
junction-case TDA 4600 – 2	$R_{th\,JC}$	15	K/W
junction-air TDA 4600 – 2 D[1])	$R_{th\,JA}$	60	K/W
junction-air TDA 4600 – 2 D[2])	$R_{th\,JA\,1}$	44	K/W
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C

Operating range

Supply voltage range	V_9	7.8 to 18	V
Case temperature range TDA 4600 – 2	T_{case}	0 to 85	°C
Ambient temperature range TDA 4600 – 2 D[3])	T_{amb}	0 to 70	°C

1) Package soldered in PCB without cooling area

2) Package soldered in PCB with copper-clad 35 µ layer, cooling area 25 cm²

3) $R_{th\,JA\,1} = 44$ K/W and $P_V = 1$ W

Characteristics

T_{amb} = 25°C, according to test circuit 1 and diagram

		min	typ	max	
Start operation					
Current consumption (V_1 not yet switched on)					
V_9 = 2 V	I_9			0.5	mA
V_9 = 5 V	I_9		1.5	2.0	mA
V_9 = 10 V	I_9		2.4	3.2	mA
Switching point for V_1	V_9	11	11.8	12.3	V
Normal operation (V_9 = 10 V; $V_{control}$ = −10 V; V_{clock} = ±0.5 V; f = 20 kHz; duty cycle 1:2) after switch on					
Current consumption $V_{control}$ = −10 V	I_9	110	135	160	mA
$V_{control}$ = 0 V	I_9	55	85	110	mA
Reference voltage I_1 < 0.1 mA	V_1	4.0	4.2	4,5	V
I_1 = 5 mA	V_1	4.0	4.2	4.4	V
Temperature coefficient of reference voltage	TC_1		10^{-3}		1/K
Feedback voltage	V_2*)		0.2		V
Control voltage $V_{control}$ = 0 V	V_3	2.3	2.6	2.9	V
Collector current simulation voltage					
$V_{control}$ = 0 V	V_4*)	1.8	2.2	2.5	V
$V_{control}$ = 0 V/−10 V	ΔV_4*)	0.3	0.4	0.5	V
Blocking input voltage	V_5	5.5	6.3	7.0	V
Output voltage $V_{control}$ = 0 V	$V_{q\,7}$*)	2.7	3.3	4.0	V
$V_{control}$ = 0 V	$V_{q\,8}$*)	2.7	3.4	4.0	V
$V_{control}$ = 0 V/−10 V	$\Delta V_{q\,8}$*)	1.4	1.8	2.2	V
Safety operation (V_9 = 10 V; $V_{control}$ = −10 V; V_{clock} = ±0.5 V; f = 20 kHz; duty cycle 1:2)					
Current consumption (V_5 < 1.8 V)	I_9	14	22	28	mA
Switch-off voltage (V_5 < 1.8 V)	$V_{q\,7}$	1.3	1.5	1.8	V
	V_4	1.8	2.1	2.5	V
Ext. blocking input					
enable voltage $V_{control}$ = 0 V	V_5		2.4	2.7	V
disable voltage $V_{control}$ = 0 V	V_5	1.8	2.2		V
Supply voltage					
for V_8 blocked $V_{control}$ = 0 V	V_9	6.7	7.4	7.8	V
Supply voltage for V_1 off (while further decreasing V_9)	ΔV_9	0.3	0.6	1.0	V

Characteristics

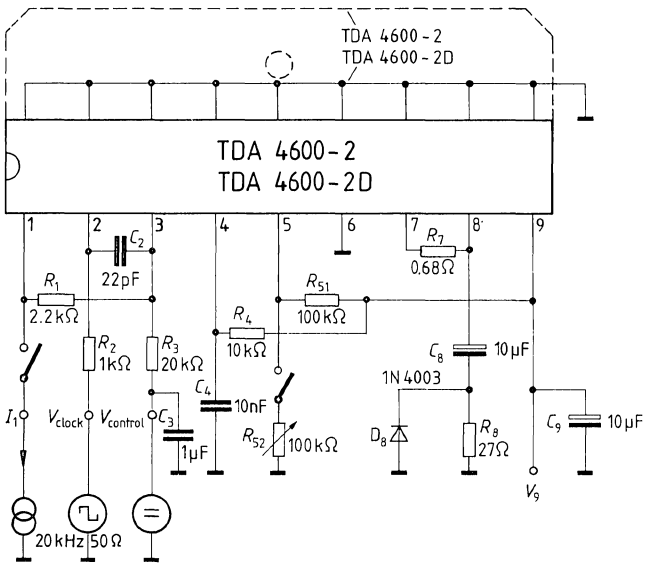
T_{amb} = 25 °C, according to test circuit 2

Switch-on time (secondary voltages)	t_{on}		350	450	ms
Voltage change					
S3 = closed (ΔN_3 = 20 W)	ΔV_2		100	500	mV
Sound output power					
S2 = closed (ΔN_2 = 15 W)	ΔV_2		500	1000	mV
Standby operation					
(secondary useful load = 3 W)					
S1 = open	ΔV_2		20	30	V
	f	70	75		kHz
	$N_{primary}$		10	12	VA

The cooling area should be optimized according to the limit values (T_{amb}, T_j, R_{thJC}, R_{thJA}, $R_{thJA\,1}$)

*) only dc part

Measurement circuit 1



Circuit description

During start-up, normal and overload operations the TDA 4600-2; or -2D regulates, controls and protects the switching transistor installed in the flyback converter power supplies.

I) Start-up operation

The start-up operation is divided into three consecutive phases:

1. An internal reference voltage is built up which supplies the voltage regulator and effects the charging of the coupling electrolytic capacitor and the switching transistor. During these procedures an I_9 current less than 3.2 mA will be maintained, if the supply voltage V_9 does not exceed ≈ 12 V.
2. At V_9 ≈ 12 V an internal reference voltage V_1 = 4 V is suddenly released to provide all IC components with the exception of the control logic with a thermally stable and overload-resistant current.
3. In concurrence with the release of the reference voltage the control logic is activated by an additional stabilization circuit, and the IC is now ready for operation.

Above sequential start-up phases ensure the charging of the switching transistor by the coupling electrolytic capacitor and subsequent precision switching.

II) Normal operation

Zero passages of the feedback coil are registered at pin 2 and forwarded to the control logic.

At pin 3 (input control, overload, and standby recognition) the rectified amplitude variations of the feedback coil are applied. The regulating (control) amplifier operates with an input voltage of about 2 V and a current of about 1.4 mA. According to the internal reference voltage, the operating region of the regulating amplifier will be defined by the collector current simulation pin 4 and the overload recognition. The simulation of the collector current is generated by an external *RC* network at pin 4 and an internally set voltage level. By increasing the capacitance (10 nF), the collector current of the switching transistor is increased as well and establishes the desired control range. The control range extends between a 2 V clamped dc voltage and an ac voltage rising as a sawtooth wave, which may vary up to a maximum amplitude of 4 V (reference voltage).

By reducing the secondary load to 20 W, the switching frequency increases to about 50 kHz at an almost constant pulse duty factor (on-time to period approx. 1/3). During additional secondary load reduction to about 1 W, the switching frequency will change to approx. 70 kHz, while the pulse duty factor falls to approx. 1/11. At the same time, the collector peak current falls below 1 A.

The output level of the regulating (control) amplifier, the overload recognition, and the collector current simulation are compared in the trigger and the control logic is instructed accordingly. Pin 5 will provide additional blocking alternatives, i.e. the output at pin 8 is blocked at a voltage of equal to or less than 2.2 V at pin 5.

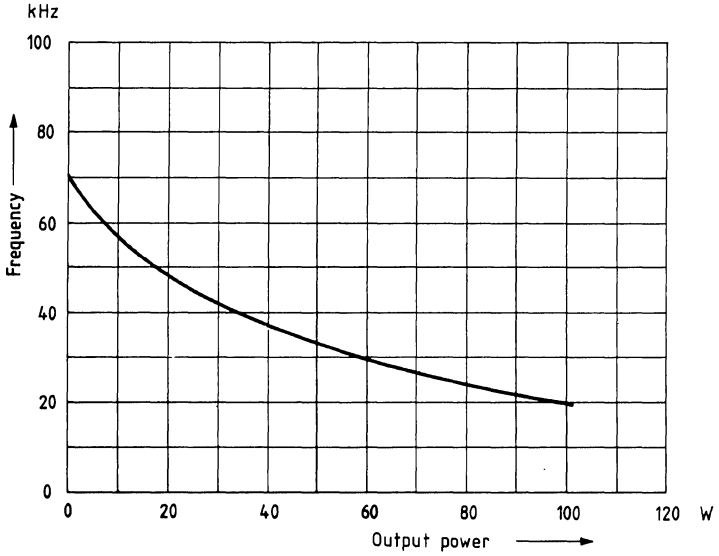
Based on the start-up circuit, the zero crossing identification, and the trigger-activated release, the control logic flipflops are set which control both the base current amplification and shut-down. The base current amplifier forwards the sawtooth voltage V_4 to pin 8. Also, a current feedback with an external resistance of $R \approx 0.68\ \Omega$ is inserted between pin 8 and pin 7. The resistance value determines the maximum amplitude of the base current for the switching transistor.

III) Safety features

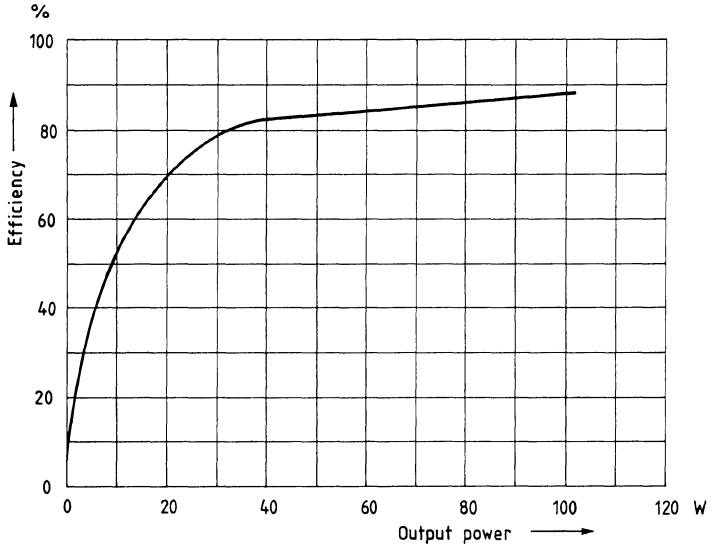
The base current shut-down, released by the control logic, clamps the output of pin 7 at 1.6 V and thus blocks the driving of the switching transistor. This preventive method will go into effect, if the voltage at pin 9 falls below typ. 7.4 V or if voltages of less than typ. 22 V are present at pin 5. In case of short-circuited secondary windings in the SMPS, the fault condition will be continuously monitored by the IC.

With the load completely removed from the secondary winding in the SMPS, the IC is set at a small pulse duty factor. The total power consumption of the SMPS is kept below $n = 6$ to 10 W during both operating conditions. After the output has been blocked at a supply voltage V_9 of less than or equal to typ. 7.4 V, an additional voltage reduction of $\Delta V_9 = 0.6$ V will switch off the reference voltage (4 V).

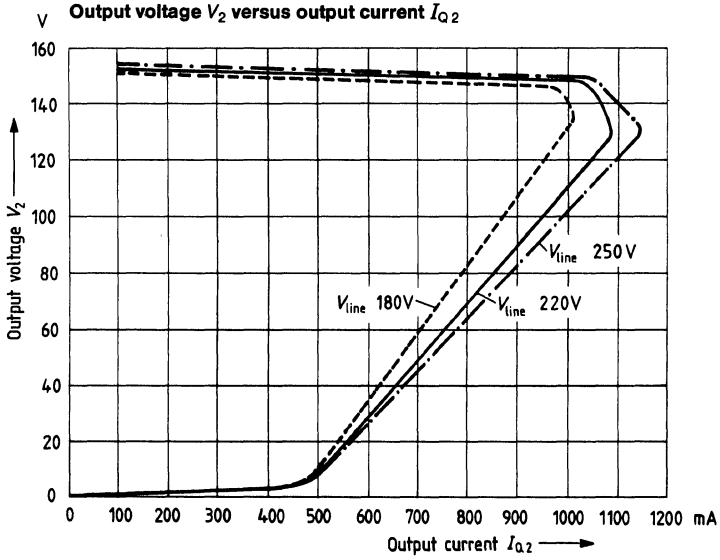
Frequency versus output power



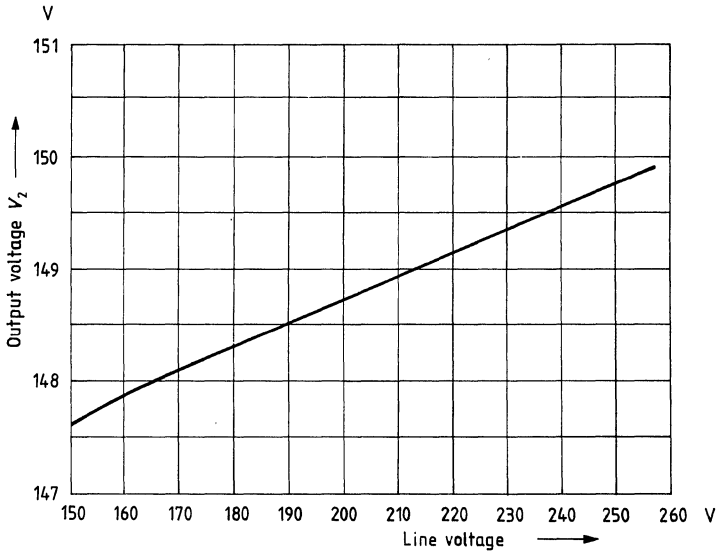
Efficiency versus output power



Load characteristic
Output voltage V_2 versus output current I_{Q2}



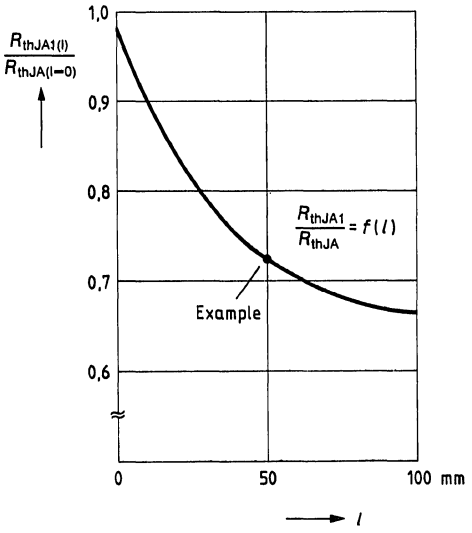
Output voltage V_2 versus line voltage alterations



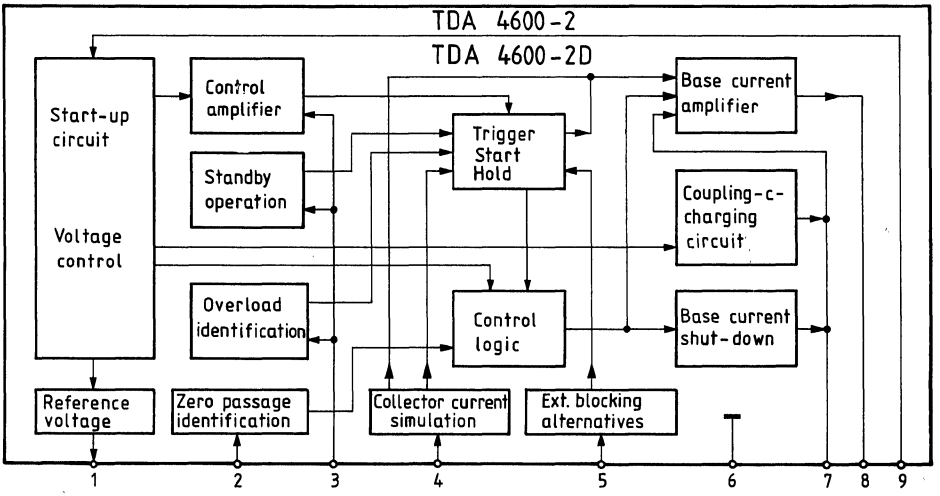
Thermal resistance (only applicable to TDA 4600-2 D)

Standardized, ambience-related thermal resistance $R_{th\ JA1}$ versus lateral length l of a square copper-clad cooling area (35 µm copper lamination).

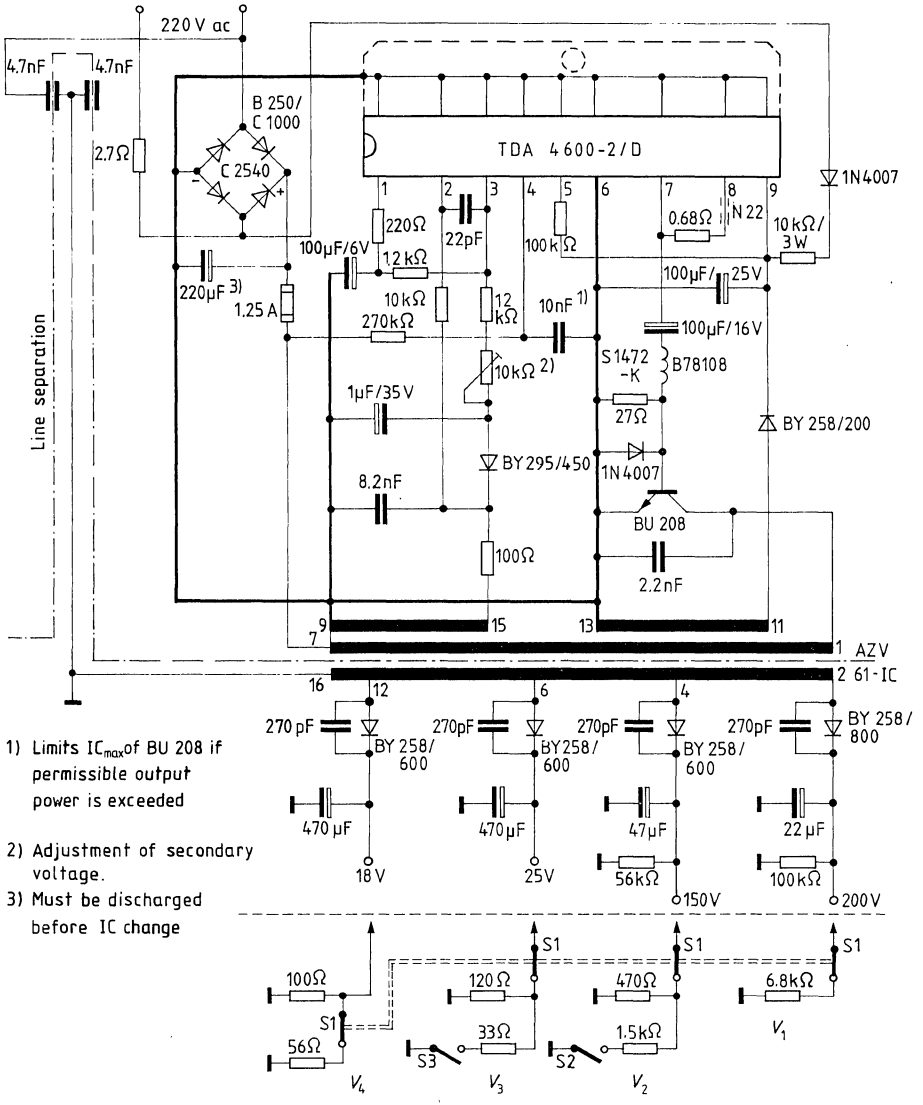
$R_{th\ JA}$ (l = 0) = 60 K/W
$T_{amb} \leq 70$ °C
P_V = 1 W
PCB in vertical position
circuit in vertical position
static air



Block diagram



Measurement circuit 2 and application circuit

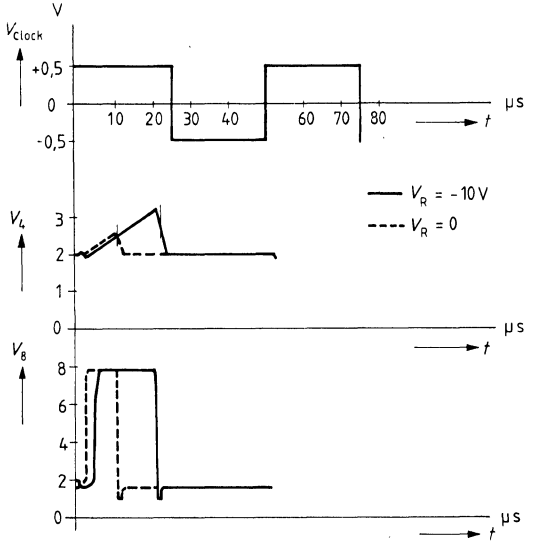


1) Limits IC_{max} of BU 208 if permissible output power is exceeded

2) Adjustment of secondary voltage.

3) Must be discharged before IC change

Measurement diagram for overload operations



(TDA 4600-2: Plastic Power Package - 9 pin SIP package)

Pin configuration (TDA 4600-2D: Plastic 18 pin DIP package)

Pin No.	Function
1	V_{ref} output
2	Zero passage identification
3	Input regulating amplifier, overload amplifier
4	Collector current simulation
5	Possible connection for additional protective circuit
6	Ground
7	DC voltage output for charging the coupling capacitor
8	Pulse output – driving the switching transistor
9	Current supply input

only applicable to TDA 4600-2D

10	interconnected (ground)
11	
12	
13	
14	
15	
16	
17	
18	

TDA 4601/TDA 4601D Control IC for Switched-Mode Power Supplies

Bipolar IC

During start-up, normal and overload operations the TDA 4601 or TDA 4601D regulates, controls and protects the switching transistor installed in the flyback converter power supplies. It also protects the complete SMPS by preventing an increase in the secondary voltage in case of errors. In addition to their use with TV receivers and video recorders, these ICs can be applied in power supplies of hi-fi sets and active speakers due to their wide operational ranges and superior voltage stability during high load changes.

Features

- Direct driving of switching transistor
- Low start-up current
- Reversing linear overload characteristic
- Collector current – proportional to base-current input
- Protective circuit for the event of errors

Maximum ratings

		Lower limit	Upper limit	
Supply voltage	V_9	0	20	V
Voltages				
reference output	V_1	0	6	V
zero-passage identification	V_2	−0.6	0.6	V
control amplifier	V_3	0	3	V
collector-current simulation	V_4	0	8	V
blocking input	V_5	0	8	V
base-current cut-off point	V_7	0	V_9	V
base-current amplifier output	V_8	0	V_9	V
Currents				
zero-passage identification	I_{I2}	−3	3	mA
control amplifier	I_{I3}	−3	3	mA
collector-current simulation	I_{I4}	0	5	mA
blocking input	I_{I5}	0	5	mA
base-current cut-off point	I_{Q7}	0	1.5	mA
base-current amplifier output	I_{Q8}	−1.5	0	mA
Thermal resistance				
junction-air TDA 4601	$R_{th\ JA}$		70	K/W
junction-case TDA 4601	$R_{th\ JC}$		15	K/W
junction-air TDA 4601 D[1]	$R_{th\ JA}$		60	K/W
junction-air TDA 4601 D[2]	$R_{th\ JA\ 1}$		44	K/W
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C

Operating range

Supply voltage range		V_9	7.8 to 18	V
Case temperature range	TDA 4601	T_{case}	0 to 85	°C
Ambient temperature range[3]	TDA 4601 D	T_{amb}	0 to 70	°C

1) Package soldered in PCB without cooling area.

2) Package soldered in PCB with copper-clad 35-µm layer, cooling area 25 cm²

3) $R_{th\ JA\ 1} = 44$ K/W and $P_V = 1$ W

Characteristics

$T_{amb} = 25\ °C$
according to test circuit 1 and diagram

		min	typ	max	
Start operation					
Current consumption (V_1 not yet applied)					
$V_9 = 2$ V	I_9			0.5	mA
$V_9 = 5$ V	I_9		1.5	2.0	mA
$V_9 = 10$ V	I_9		2.4	3.2	mA
Switching point for V_1	V_9	11.0	11.8	12.3	V
Normal operation					
($V_9 = 10$ V; $V_{control} = -10$ V; $V_{clock} = \pm 0.5$ V; $f = 20$ kHz; duty cycle 1 : 2) after switch-on					
Current consumption					
$V_{control} = -10$ V	I_9	110	135	160	mA
$V_{control} = 0$ V	I_9	50	75	100	mA
Reference voltage					
$I_1 < 0.1$ mA	V_1	4.0	4.2	4.5	V
$I_1 = 5$ mA	V_1	4.0	4.2	4.4	V
Temperature coefficient of reference voltage	TC_1		10^{-3}		1/K
Control voltage $V_{control} = 0$ V	V_3	2.3	2.6	2.9	V
Collector-current simulation voltage					
$V_{control} = 0$ V	V_4*)	1.8	2.2	2.5	V
$V_{control} = 0$ V/−10 V	ΔV_4*)	0.3	0.4	0.5	V
Blocking voltage	V_5	6.0	7.0	8.0	V
Output voltages					
$V_{control} = 0$ V	V_{q7}*)	2.7	3.3	4.0	V
$V_{control} = 0$ V	V_{q8}*)	2.7	3.4	4.0	V
$V_{control} = 0$ V/−10 V	ΔV_{q8}*)	1.6	2.0	2.4	V
Feedback voltage	V_2		0.2		V

*) only dc part

Characteristics

$T_{amb} = 25$ °C

Safety operation

($V_9 = 10$ V; $V_{control} = -10$ V; $V_{clock} = \pm 0.5$ V; $f = 20$ kHz; duty cycle 1 : 2)

		min	typ	max	
Current consumption ($V_5 < 1.9$ V)	I_9	14	22	28	mA
Switch-off voltage ($V_5 < 1.9$ V)	V_{q7}	1.3	1.5	1.8	V
Blocking input	V_4	1.8	2.1	2.5	V
Blocking voltage ($V_{control} = 0$ V)	V_5	$\frac{V_1}{2} - 0.1$	$\frac{V_1}{2}$		V
Supply voltage for V_8 blocked ($V_{control} = 0$ V)	V_9	6.7	7.4	7.8	V
(with further decrease of V_9)	ΔV_9	0.3	0.6	1	V

Characteristics

$T_{amb} = 25$ °C acc. to test circuit 2

Turn-on time (secondary voltage)	t_{on}		350	450	ms
Voltage change with S3 = closed ($\Delta N_3 = 20$ W)	ΔV_{2s}		100	500	mV
Voltage change with S2 = closed ($\Delta N_2 = 15$ W)	ΔV_{2s}		500	1000	mV
Standby operation with S1 = open (secondary useful load = 3 W)	ΔV_{2s}		20	30	V
	f	70	75		kHz
	$N_{primary}$		10	12	VA

The cooling area should be optimized in consideration of the limit values (T_{case}; T_j; $R_{th\,JC}$; $R_{th\,JA}$).

Circuit description

During start-up, normal, overload, and disturbed operations the TDA 4601/D regulates, controls and protects the switching transistor installed in the flyback converter power supplies. If an error occurs, the driving of the switching transistor is blocked and the voltage on the secondary side is prevented from increasing.

I) Start-up operation

The start-up operation is divided into three consecutive phases:

1. An internal reference voltage is built up which supplies the voltage regulator and effects the charging of the coupling electrolytic capacitor and the switching transistor. During these procedures an I_9 current less than 3.2 mA will be maintained, if the supply voltage V_9 does not exceed $\approx$ 12 V.
2. At $V_9 \approx 12$ V an internal reference voltage $V_1 = 4$ V is suddenly released to provide all IC components with the exception of the control logic with a thermally stable and overload-resistant current.
3. In concurrence with the release of the reference voltage the control logic is activated by an additional stabilization circuit, and the IC is now ready for operation.

Above sequential start-up phases ensure the charging of the switching transistor by the coupling electrolytic capacitor and subsequent precision switching.

II) Normal operation

Zero passages of the feedback coil are registered at pin 2 and forwarded to the control logic.

At pin 3 (input control, overload, and standby recognition) the rectified amplitude variations of the feedback coil are applied. The regulating (control) amplifier operates with an input voltage of about 2 V and a current of about 1.4 mA. According to the internal reference voltage, the operating region of the regulating amplifier will be defined by the collector current simulation pin 4 and the overload recognition. The simulation of the collector current is generated by an external *RC* network at pin 4 and an internally set voltage level. By increasing the capacitance (10 nF), the collector current of the switching transistor is increased as well and establishes the desired control range. The control range extends between a 2 V clamped dc voltage and an ac voltage rising as a sawtooth wave, which may vary up to a maximum amplitude of 4 V (reference voltage).

By reducing the secondary load to 20 W, the switching frequency increases to about 50 kHz at an almost constant pulse duty factor (on-time to period approx. 1/3). During additional secondary load reduction to about 1 W, the switching frequency will change to approx. 70 kHz, while the pulse duty factor falls to approx. 1/11. At the same time, the collector peak current falls below 1 A.

The output level of the regulating (control) amplifier, the overload recognition, and the collector current simulation are compared in the trigger and the control logic is instructed accordingly. Pin 5 will provide additional blocking alternatives, i.e. the output at pin 8 is blocked at a voltage of equal to or less than $V_{ref}/2 - 0.1$ V at pin 5.

Based on the start-up circuit, the zero crossing identification, and the trigger-activated release, the control logic flipflops are set which control both the base current amplification and shut-down. The base current amplifier forwards the sawtooth voltage V_4 to pin 8. Also, a current feedback with an external resistance of $R \approx 0.68\ \Omega$ is inserted between pin 8 and pin 7. The resistance value determines the maximum amplitude of the base current for the switching transistor.

III) Safety features

The base current shut-down, released by the control logic, clamps the output of pin 7 at 1.6 V and thus blocks the driving of the switching transistor. This preventive method will go into effect, if the voltage at pin 9 falls below typ. 6.7 V or if voltages of equal to or less than $V_{ref}/2$ – 0.1 V are present at pin 5. In case of short-circuited secondary windings in the SMPS, the fault condition will be continuously monitored by the IC.

With the load completely removed from the secondary winding in the SMPS, the IC is set at a small pulse duty factor. The total power consumption of the SMPS is kept below $n = 6$ to 10 W during both operating conditions. After the output has been blocked at a supply voltage V_9 of less than or equal to typ. 6.7 V, an additional voltage reduction of $\Delta V_9 = 0.6$ V will switch of the reference voltage (4 V).

Protective operation for faults with pin 5

For protection against disturbances such as primary undervoltages and/or secondary overvoltages (e.g. as a result of alterations in the parameters of components of the SMPS), it is possible to implement applications of the following kind:

● **Protective operation with periodic sampling**

In the event of the fault condition, falling below the protective threshold V_5 of typically $V_{1/2}$ causes the output pulses on pin 8 to be inhibited and pin 5 to be clamped internally to ground across typically 300 Ω. The current consumption of the IC reduces ($I_9 \geq 14$ mA for $V_9 = 10$ V).

With a suitably **high-impedance** starting resistor*) the supply voltage V_9 then falls below the minimal turn-off threshold (5.7 V) for the reference voltage V_1. As a result V_1 is turned off and the blocking of pin 5 is cancelled.

Because of the renewed reduction in the current consumption of the IC ($I_9 \leq 3.2$ mA for $V_9 \leq 10$ V) the supply voltage can again climb to the turn-on threshold $V_9 \geq 12.3$ V. The protective threshold on pin 5 is released and the switched-mode power supply attempts to turn on.

If the same fault is still present or another ($V_5 \leq V_{1/2} - 0.1$ V), the turn-on will be interrupted by the above, periodic protective operation, i.e. pin 8 is disabled, pin 5 is blocked, V_9 falls off, etc.

*) 10 kΩ/3 W in application circuit 1

● **Protective operation with capture circuit**

The starting resistor on pin 9 is chosen sufficiently low-impedance so that in the event of a fault V_9 does not fall below the maximum turn-off threshold (7.5 V) for V_1. The blocking of pin 5 is preserved because V_1 will not have been turned off. A one-time fault is thus captured and turning the SMPS on again is not possible, for example, until the supply voltage has been manually turned off (power switch).

In the designing of the starting resistor it should be considered that in protective operation the current consumption reduces to $I_9 \leq 28$ mA for $V_9 = 10$ V.

IV) Turn-on in wide-range power supply (90 to 270 Vac)
(application circuit 2)

Free-running flyback converters used as wide-range power supplies call for a power supply to the TDA 4601 that is independent of the rectified line voltage, thus the sense of the winding 11/13 corresponds to the secondary side of the flyback-converter transformer. Turning on is hampered by the fact that the TDA 4601 must be supplied by the start-up circuit until the entire load secondary side is charged. This leads to long turn-on times, especially with a low line voltage.

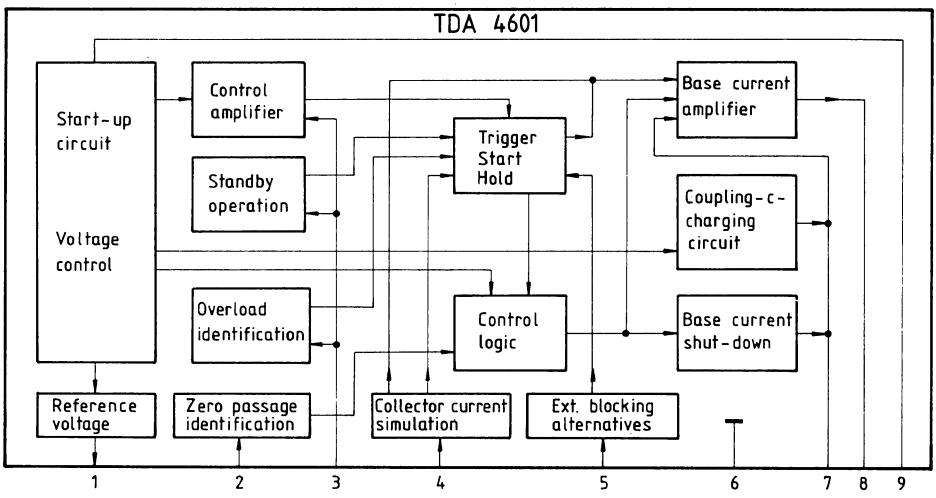
If the special start-up circuit is used (marked by dashed lines) this time can be shortened. The unregulated phase of the feedback control winding 15/9 is used as a turn-on aid. The transistor T1 blocks after turn-on, when the winding 11/13 has taken over the power supply to the TDA 4601, thus eliminating any effects on the control circuit during operation.

Pin configuration

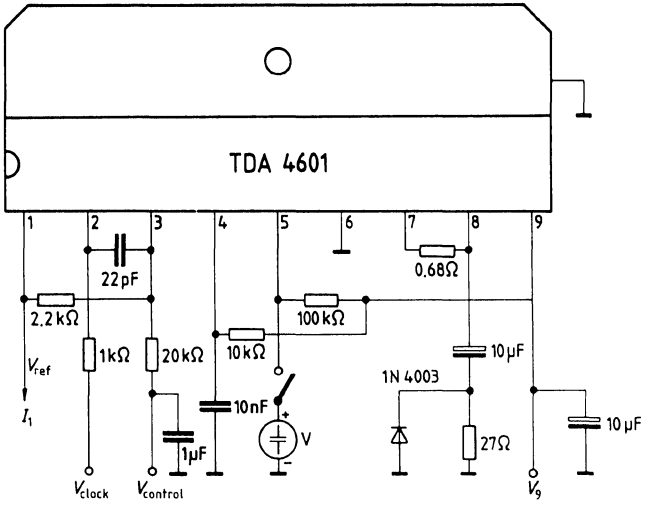
(TDA 4601: Plastic Power Package - 9 pin SIP package)
(TDA 4601D: Plastic 18 pin DIP package)

Pin No.	Function
1	V_{ref} output
2	Zero-passage identification
3	Input regulating amplifier, overload amplifier
4	Collector-current simulation
5	Possible connection for additional protective circuit
6	Ground (rigidly connected to substrate mounting plate)
7	DC voltage output for charging the coupling capacitor
8	Pulse output, driving the switching transistor
9	Power supply
10 - - - 18	connected to ground

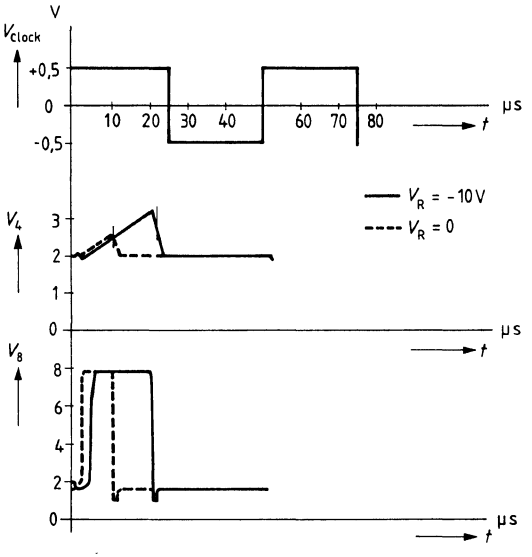
Block diagram



Test and measurement circuit 1

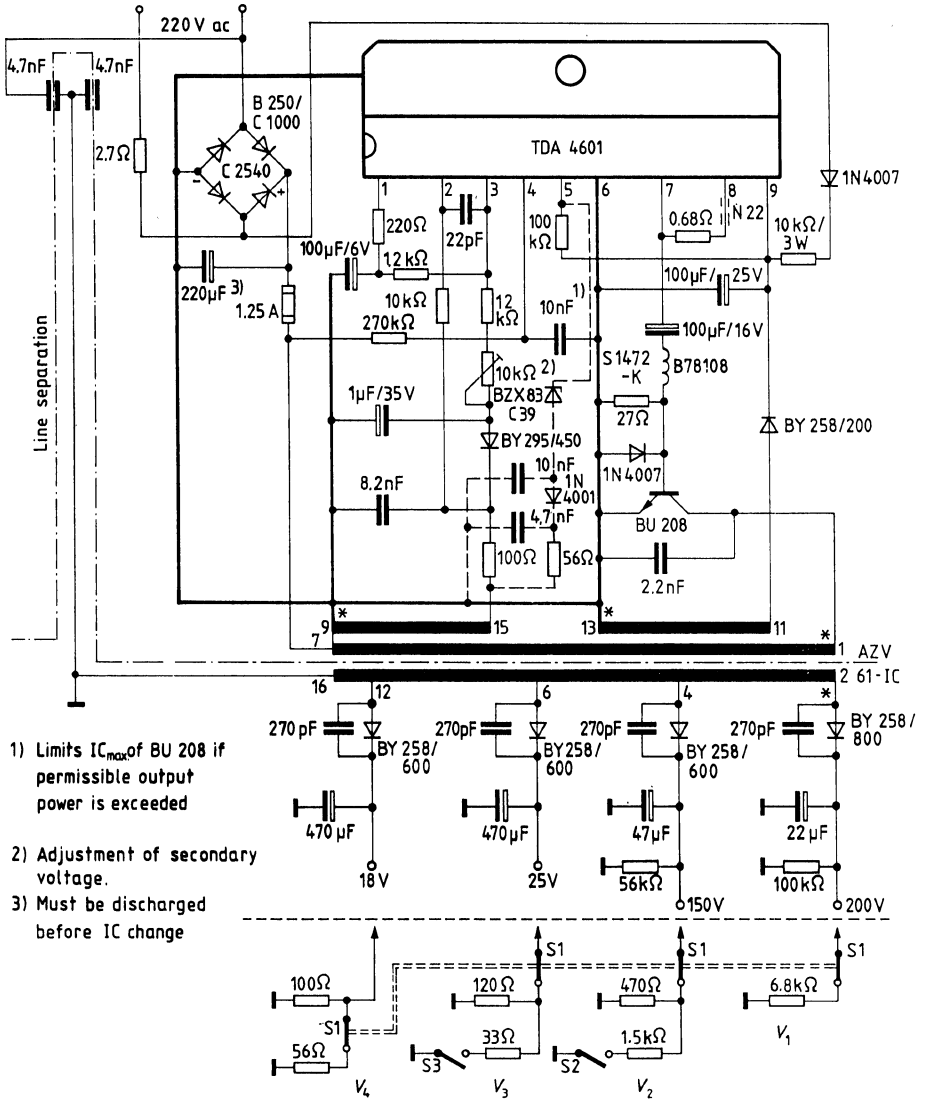


Test diagram: overload operation



Test and measurement circuit 2

Application circuit 1



1) Limits IC_{max} of BU 208 if permissible output power is exceeded

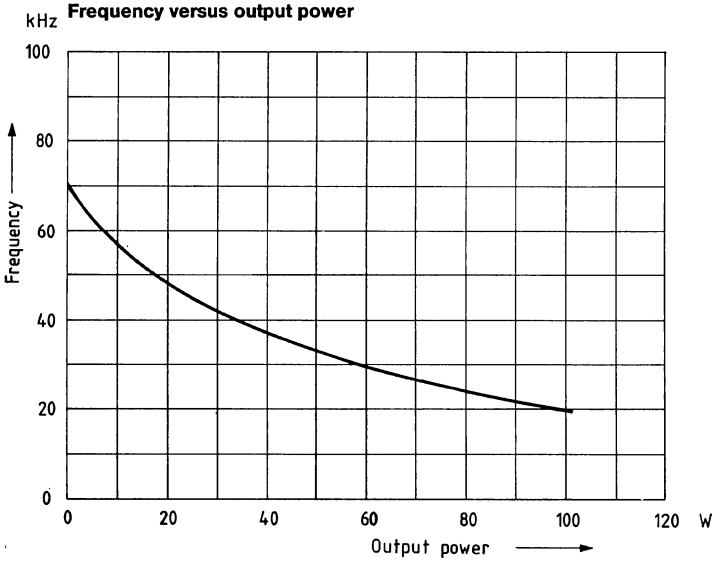
2) Adjustment of secondary voltage.

3) Must be discharged before IC change

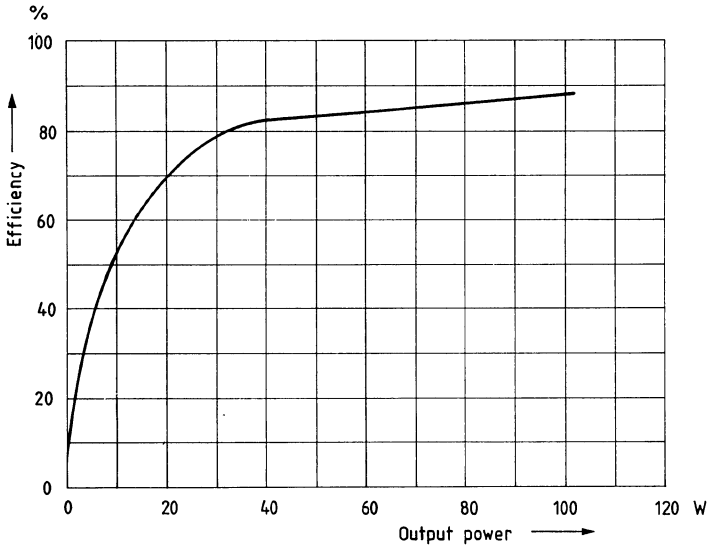
— — — Protective circuit to prevent increase of secondary voltage when fault occurs

Additions to test circuit 2

Frequency versus output power

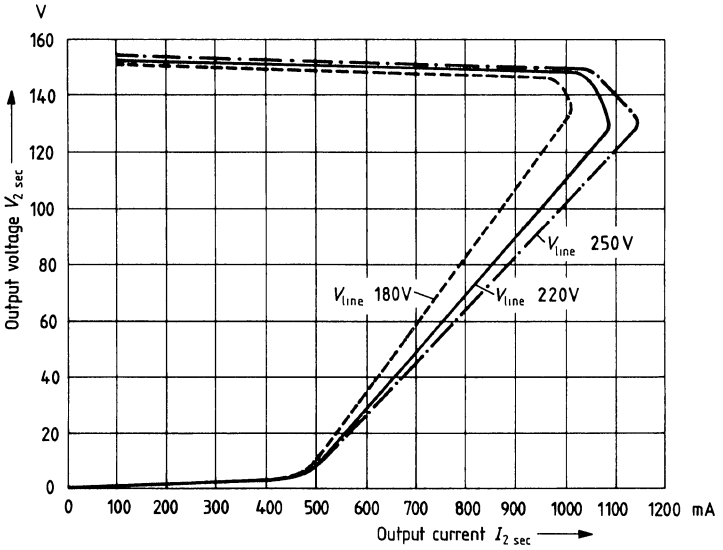


Efficiency versus output power

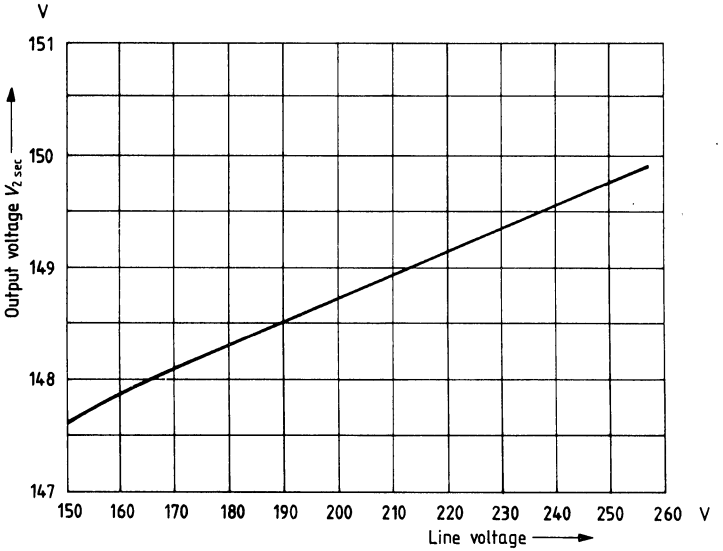


Additions to test circuit 2

Load characteristic $V_{2\,sec}$ versus output current $I_{2\,sec}$

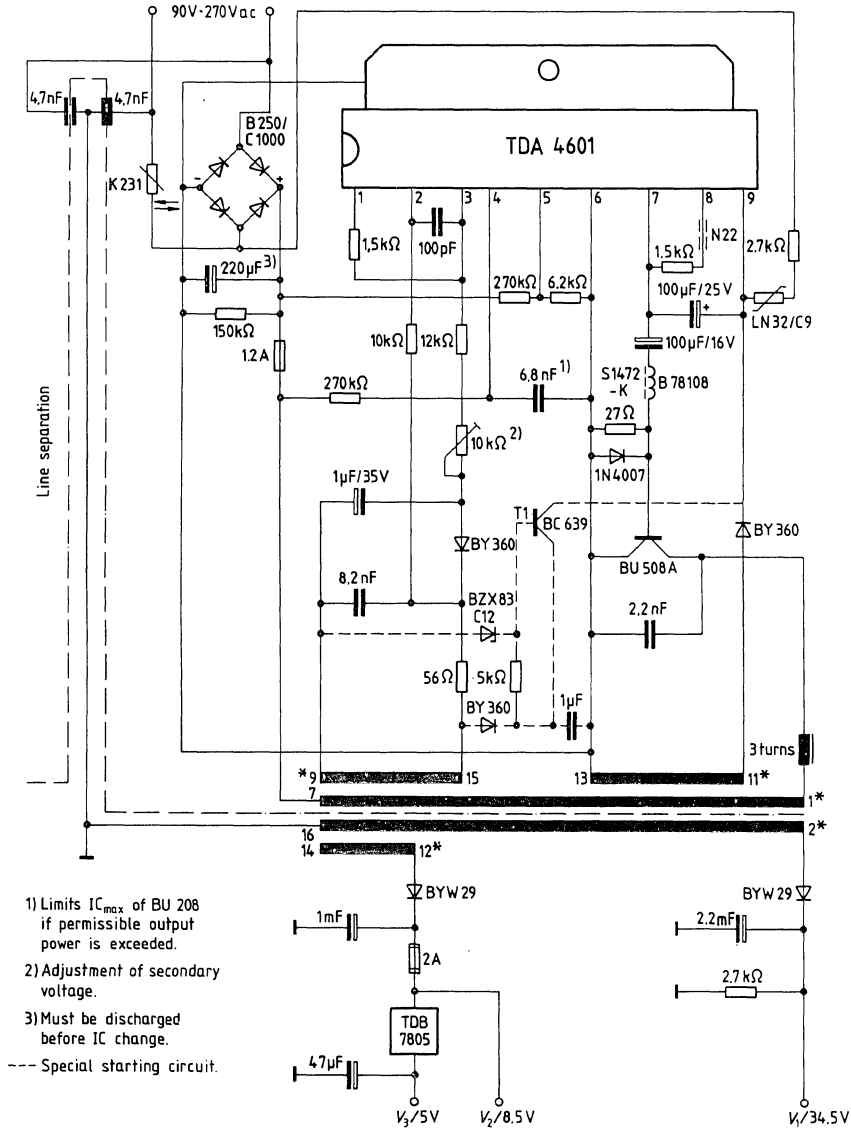


Output voltage $V_{2\,sec}$ versus line-voltage alterations



Application circuit 2

Wide range 90 Vac to 270 Vac



1) Limits IC_{max} of BU 208 if permissible output power is exceeded.

2) Adjustment of secondary voltage.

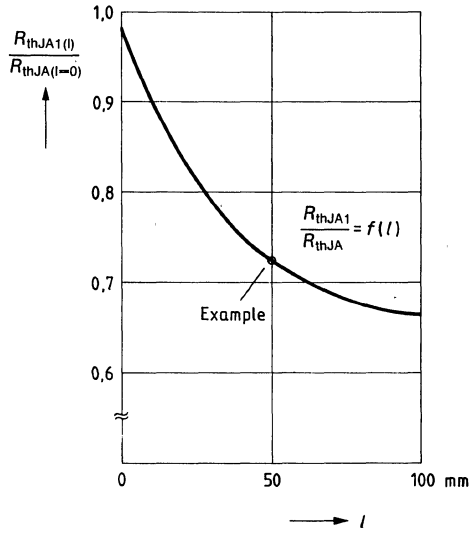
3) Must be discharged before IC change.

--- Special starting circuit.

Thermal resistance (only applies to TDA 4601 D)

Standardized, ambience-related thermal resistance $R_{th\,JA\,1}$ versus lateral length l of a square copper-clad cooling area (35 µm copper lamination).

$R_{th\,JA}$ ($l = 0$) = 60 K/W
$T_{amb} \leq 70$ °C
$P_V = 1$ W
PCB in vertical position
circuit in vertical position
static air



TDA 4700/TDA 4700A Control IC for Single-Ended and Push-Pull Switched-Mode Power Supplies

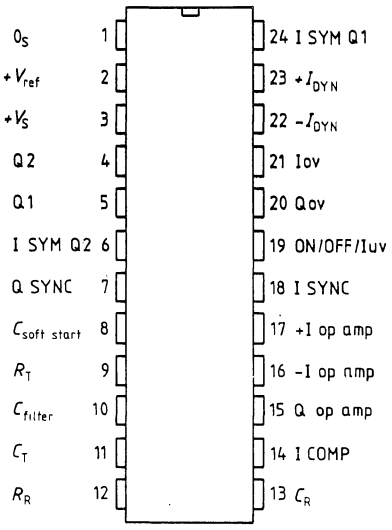
Bipolar IC

This versatile SMPS control IC comprises digital and analog functions which are required to design high-quality flyback, single-ended and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated operational amplifiers and activate protective functions.

In addition to the noticeable reduction in components, our SMPS ICs offer a number of advantages:

- Feed-forward control (line hum suppression)
- Symmetry inputs for push-pull converter
- Dynamic output current limitation
- Overvoltage protection
- Undervoltage protection
- Soft start
- Double pulse suppression

Pin configuration,
top view



Pin designation

Pin No.	Function
1	0_S
2	Reference voltage V_{ref}
3	Supply voltage V_S
4	Output Q 2
5	Output Q 1
6	Symmetry Q 2
7	Sync. output
8	Soft start $C_{soft\ start}$
9	VCO R_T
10	Capacitance C_{filter}
11	VCO C_T
12	Ramp generator R_R
13	Ramp generator C_R
14	Comparator input
15	Operational amplifier output
16	Operational amplifier input (−)
17	Operational amplifier input (+)
18	Sync. input
19	ON/OFF, undervoltage
20	Overvoltage output
21	Overvoltage input
22	Dynamic current limitation (−)
23	Dynamic current limitation (+)
24	Symmetry Q 1

(TDA 4700 - Ceramic 24 pin DIL package)
(TDA 4700A - Plastic 24 pin DIL package)

Circuit description

Voltage controlled oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. By varying the voltage at C_{filter}, the oscillator frequency can be changed by its rated value. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. **This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.**

Phase comparator

If the component is operated without external synchronization, the sync input must be connected to the sync output for the phase comparator to set the rated voltage at C_{filter}. The VCO then oscillates with rated frequency. In the case of external synchronization, other components can be synchronized with the sync output. **The component can be frequency-synchronized, but not phase-synchronized, with the sync input.** The duty cycle of the square-wave voltage at the sync input is arbitrary. The best stability as to small phase and frequency interference deviation is achieved with a duty cycle as offered by the sync output.

Push-pull flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational amplifier K1

The K1 op amp is a high-quality amplifier. Fluctuations in the output voltage of the power supply are amplified by K1 and applied to the free + input of comparator K2. Variations in output voltage are, in this way, converted to a corresponding change in output duty cycle. K1 has a common-mode input voltage range between 0 V and +5 V.

Pulse turn-off flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{\text{soft start}}$ (and also at K2) to a maximum of +5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{\text{soft start}}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 μA to the maximum value of 5 V. In case of an error, $C_{\text{soft start}}$ is discharged with a current of 2 μA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{\text{soft start}}$ exceeds 1.8 V.

Error flipflop

Error signals which are led to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again using the soft start.

Comparator K5, K6, K8, V_{ref} overcurrent load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start. The output of K5 can be fed back to the input. This causes the IC output stage to remain disabled even after elimination of the overvoltage. However, it requires high-ohmic overvoltage coupling.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start.

The K7 common-mode range covers 0 V to +4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Symmetry

In push-pull converters, a saturation of the transformer core must be prevented. The degree of saturation of the transformer can be determined with an external circuit, thus the active periods of the outputs can be decreased unsymmetrically at the symmetry inputs.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are active low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference voltage

The reference voltage source is a highly constant source with regard to its temperature behavoir. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum ratings

		Notes	Lower limit B	Upper limit A	
Supply voltage	V_S		−0.3	33	V
Voltage at Q1, Q2	V_Q	Q1, Q2 high	−0.3	33	V
Current at Q1, Q2	I_Q	Q1, Q2 low		70	mA
Symmetry 1, 2	V_{SYM}		−0.3	33	V
Sync output	$V_{SYNC\,Q}$	SYNC Q high	−0.3	7	V
	$I_{SYNC\,Q}$	SYNC Q low	0	10	mA
Sync input	$V_{SYNC\,I}$		−0.3	33	V
Input C_{filter}	$V_{I\,Cf}$		−0.3	7	V
Input R_T	$V_{I\,RT}$		−0.3	7	V
Input C_T	$V_{I\,CT}$		−0.3	7	V
Input R_R	$V_{I\,RR}$		−0.3	7	V
Input C_R	$I_{I\,CR}$		−10	10	mA
Input comparator K 2, K 5, K 6, K 7	$V_{I\,K}$		−0.3	33	V
Output K 5	$V_{Q\,K5}$		−0.3	33	V
Input op amp	$V_{I\,op\,amp}$		−0.3	33	V
Output op amp	$V_{Q\,op\,amp}$		−0.3	V_S-1	V
				max. 7	V
Reference voltage	V_{ref}		−0.3	V_{ref}	V
Input $C_{soft\,start}$	$V_{I\,soft\,start}$		−0.3	7	V
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−55	125	°C
Thermal resistance (system-air)					
TDA 4700	$R_{th\,SA}$			65	K/W
TDA 4700 A	$R_{th\,SA}$			65	K/W

Operating range

Supply voltage	V_S		10.5	30	V
Ambient temperature					
TDA 4700	T_{amb}		−25	85	°C
TDA 4700 A	T_{amb}		0	70	°C
VCO frequency	f		40	250000	Hz
Ramp generator frequency	f_{RG}		40	250000	Hz

Characteristics

$V_S = 11$ V to 30 V;
$T_{amb} = -25$ °C to +85 °C

		Test conditions	Lower limit B	typ	Upper limit A	
Supply current	I_S	$C_T = 1$ nF, $f_{VCO} = 100$ kHz	8		20	mA
Reference						
Reference voltage	V_{ref}	$0mA < I_{ref} < 5mA$	2.35	2.5	2.65	V
Reference voltage change	ΔV_{ref}	14 V ± 20%		8		mV
Reference voltage change	ΔV_{ref}	25 V ± 20%		15		mV
Reference voltage change	ΔV_{ref}	$0mA < I_{ref} < 5mA$			15[1]	mV
Temperature coefficient	TC			0.25	0.4	mV/K
Response threshold of I_{ref} overcurrent	I_{ref}			10		mA
Oscillator (VCO)						
Frequency range	f_{VCO}		40		100000	Hz
Frequency change	$\Delta f/f_{VCO}$	14 V ± 20%		0.5		%
Frequency change	$\Delta f/f_{VCO}$	25 V ± 20%	−1		1	%
Tolerance	$\Delta f/f_{VCO}$	$\Delta R_T = 0, \Delta C_T = 0$	−7		7	%
Fall time sawtooth	t	$C_T = 1$ nF		1		µs
	t	$C_T = 10$ nF		10		µs
RC combination	C_T		0.82		47	nF
VCO	R_T		5		700	kΩ
Ramp generator						
Frequency range	f		40		100000	Hz
Maximum voltage at C_R	V_H			5.5		V
Minimum voltage at C_R	V_L			1.8		V
Input current through R_R	I_{RR}		0		400	µA
Current transformation ratio	I_{RR}/I_{CR}			1/4		
Synchronization						
Sync output	V_{QH}	$I_{QH} = -200$ µA	4			V
	V_{QL}	$I_{QL} = 1.6$ mA			0.4	V
Sync input	V_{IH}		2			V
	V_{IL}				0.8	V
Input current	$-I_I$				5	µA
Comparator K2						
Input current	$-I_{IK2}$				2	µA
Turn-off delay[2]	$t_{d\,off}$				500	ns
Input voltage	V_{IK2}	for duty cycle				
		$\nu = 0$		1.8		V
		$\nu =$ max.		5		V
Common-mode input voltage range	V_{IC}		0		5.5	V

1) At $T_{amb} = 0$ °C to 70 °C, this value falls to max. 5 mV.
2) At the input: step function $\Delta V = -100$ mV ↛ $\Delta V = +100$ mV

Characteristics

$V_S = 11$ V to 30 V;
$T_{amb} = -25$ °C to +85 °C

		Test conditions	Lower limit B	typ	Upper limit A	
Soft start K3, K4						
Charging current for $C_{soft\ start}$	I_{ch}			6		µA
Discharging current for $C_{soft\ start}$	I_{dch}			2		µA
Upper limiting voltage	V_{lim}			5		V
Switching voltage K4	V_{K4}			1.5		V
Operational amplifier						
Open-loop voltage gain	G_{V0}		60	80		dB
Input offset voltage	V_{IO}		−10		10	mV
Temperature coefficient of V_{IO}	TC		−30		30	µV/K
Input current	$-I_I$				2	µA
Common-mode input voltage range	V_{IC}		0		5	V
Output current	I_Q		−3		1.5	mA
Rise time of output voltage	$\Delta V/\Delta t$			1		V/µs
Transition frequency	f_T			3		MHz
Phase at f_T	φ_T			120		degrees
Output voltage	$V_{Q\,H/L}$	$-3\,mA < I < 1.5\,mA$	1.5		5.5	V
Symmetry						
Input voltage	V_{IH}		2.0			V
	V_{IL}				0.8	V
Input current	$-I_I$				2	µA
Output stages Q1, Q2						
Output voltage	$V_{Q\,H}$				30	V
	$V_{Q\,L}$	$I_Q = 20$ mA			1.1	V
Output leakage current	I_Q	$V_{Q\,H} = 30$ V			2	µA
ON, OFF, undervoltage K6						
Switching voltage	V		V_{ref}-30mV		V_{ref}+30mV	V
Input current	$-I_I$				2	µA
Turn-off delay time[1]	$t_{d\,off}$			250		ns
Error detection time[1]	t			50		ns

1) At the input: step function $V_{ref} = -100$ mV ↛ $V_{ref} = +100$ mV

Characteristics

$V_S = 11$ V to 30 V; $T_{amb} = -25$ °C to +85 °C

		Test conditions	Lower limit B	typ	Upper limit A	
Dynamic current limitation K 7						
Common-mode input voltage range	V_{IC}		0		4	V
Input offset voltage	V_{IO}		−10		10	mV
Input current	$-I_I$				2	µA
Turn-off delay time[1]	$t_{d\,off}$			250		ns
Error detection time[1]	t			50		ns
Overvoltage K 5						
Switching voltage	V		V_{ref}−30 mV		V_{ref}+30 mV	V
Input current	$-I_I$				2	µA
Output current	$-I_Q$	$V_{QHmin} = 5$ V	0		200	µA
Turn-off delay time[2]	$t_{d\,off}$			250		ns
Error detection time[2]	t			50		ns
Supply undervoltage						
Turn-on threshold for V_S	V_S		8.8		11	V
rising		0°C<T_{amb}<70°C			10.5	V
Turn-off threshold for V_S	V_S		8.5		10.5	V
falling		0°C<T_{amb}<70°C			10	V
Input C_{filter}						
Rated voltage for rated frequency	V_R			4		V
Frequency approx. proportional to voltage within the range	V_R		3		5	V
Voltage at open sync input	$V_{C\,filter}$			1.6		V

1) At the input: step function $\Delta V = -100$ mV ⌐→ $\Delta V = +100$ mV

2) At the input: step function $V_{ref} = -100$ mV ⌐→ $V_{ref} = +100$ mV

Dimensioning notes for RC network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$

2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.

3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.

4. Duration of the soft start process
   → selection of $C_{soft\ start}$.

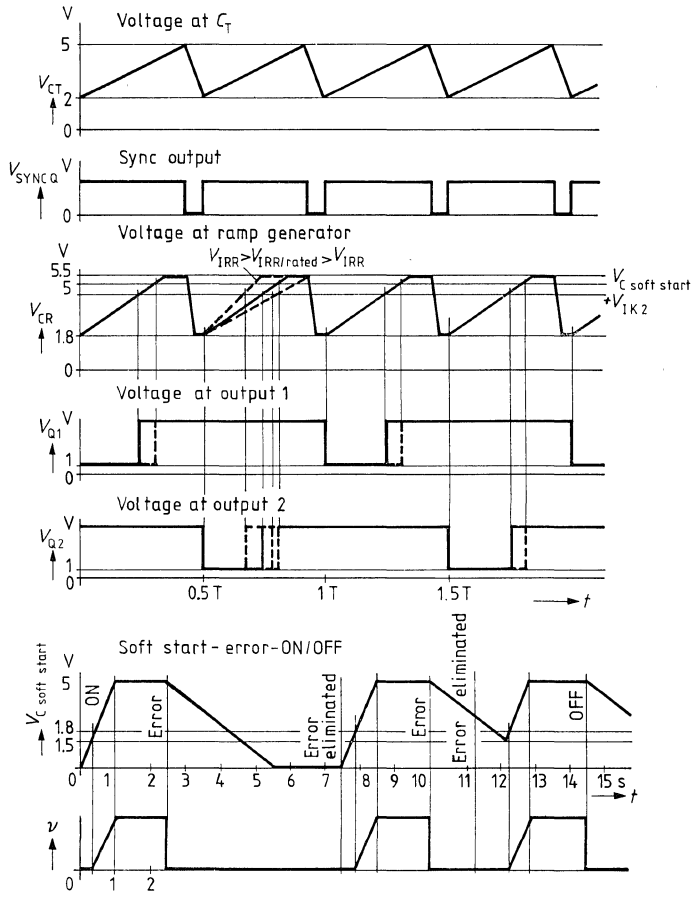
5. In the case of a free-running VCO: connect sync output with sync input.

6. Wiring of the op amp according to the dynamic requirements and connection of its output with the free input of K2.

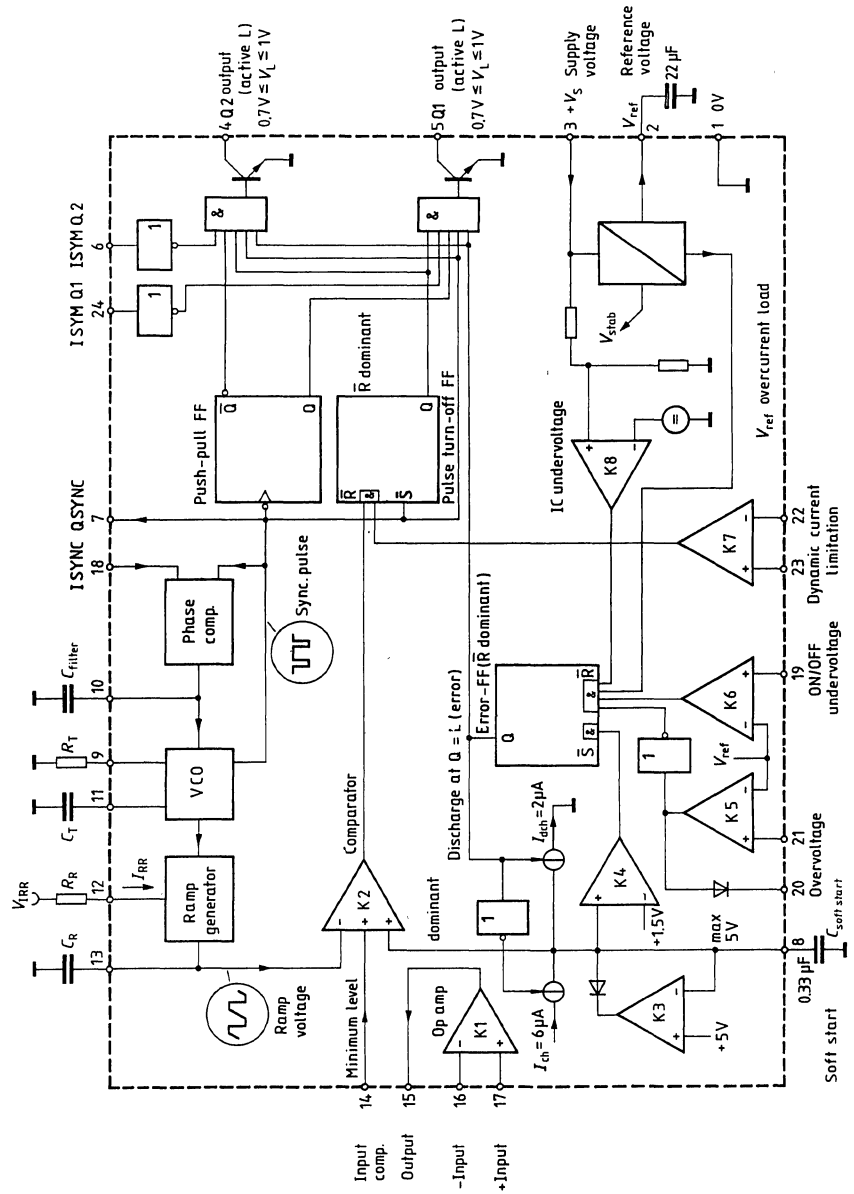
7. Capacitance C_{filter} is not required in the free-running operation (sync input connected with sync output).
   In the case of external synchronization, that value depends on the selected operating frequency and the required maximum phase interference deviation.

Rated VCO frequency:	100 kHz	50 Hz
C_{filter} favorable:	10 nF	1 µF

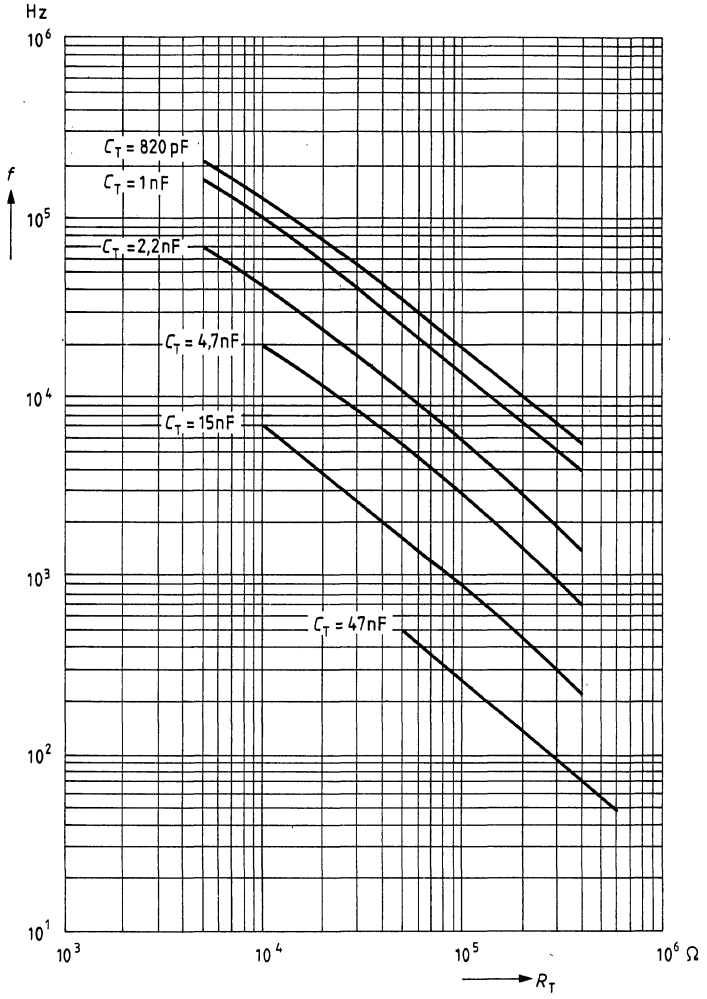
Pulse diagram



Block diagram

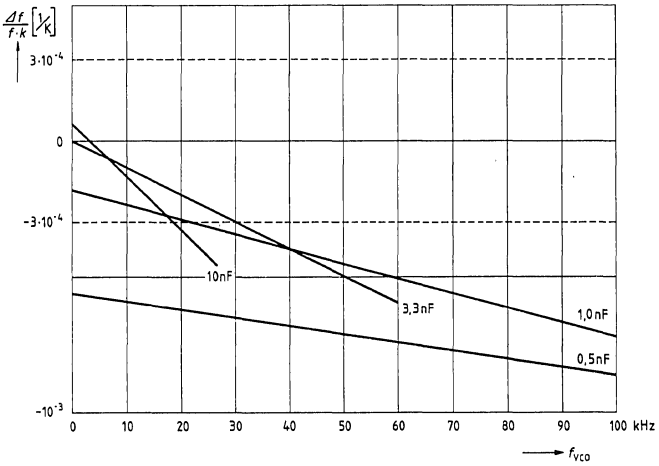


VCO frequency versus R_T and C_T.

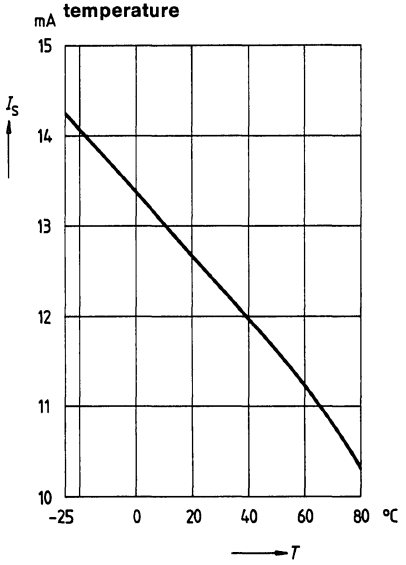


VCO temperature response
$V_S = 12$ V; ν = max.

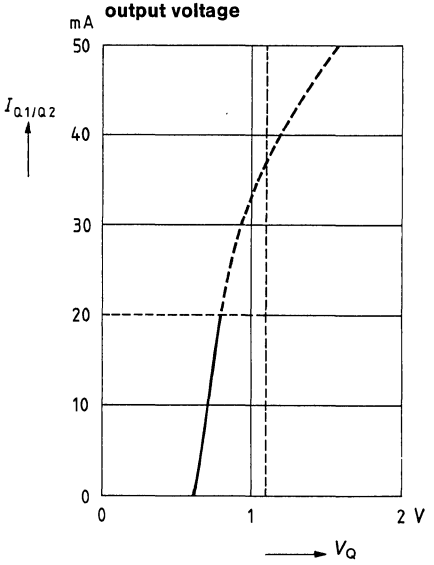
$\frac{\Delta f_{VCO}}{f_K \cdot K}\left[\frac{1}{K}\right]$ with C_T as parameter



Current consumption versus temperature



Output current versus output voltage



TDA 4714A/TDA 4714B
IC for
Switched-Mode Power Supplies

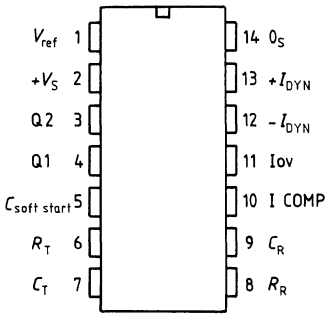
Bipolar IC

This versatile, 14-pin SMPS IC comprises digital and analog functions which are required to design high-quality flyback, single-ended, and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated op amps and activate protective functions.

Features

- Push-pull outputs (open collector)
- Double pulse suppression
- Dynamic current limitation
- Overvoltage protection
- IC undervoltage protection
- Reference voltage source (± 2% for TDA 4714 B)
- Reference overload protection
- Soft start
- Feed-forward control

Pin configuration
top view



Pin designation

Pin No.	Function
1	Reference voltage V_{ref}
2	Supply voltage V_S
3	Output Q 2
4	Output Q 1
5	Soft start $C_{soft\ start}$
6	VCO R_T
7	VCO C_T
8	Ramp generator R_R
9	Ramp generator C_R
10	Input comparator
11	Input overvoltage
12	Dynamic current limitation (−)
13	Dynamic current limitation (+)
14	0_S

(TDA 4714A/4714B - Plastic 14 pin DIL package)

Circuit description

The following is a description of the individual functional units and their interaction.

Voltage controlled oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. **This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.**

Push-pull flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Pulse turn-off flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{\text{soft start}}$ (and also at K2!) to a maximum of 5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{\text{soft start}}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way, the outputs cannot be turned on again as long as an error signal is present.

Soft start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{soft\ start}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{soft\ start}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{soft\ start}$ exceeds 1.8 V.

Error flipflop

Error signals, which are led to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again using the soft start.

Comparator K5, K8, V_{ref} overcurrent load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start. K7 has a common-mode input voltage range between 0 V and 4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are actively low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.3	33	V
Voltage at Q1, Q2 Q 1/2 high	V_Q	−0.3	33	V
Current at Q1, Q2 Q 1/2 low	I_Q		70	mA
Input R_T	$V_{I\,RT}$	−0.3	7	V
Input C_T	$V_{I\,CT}$	−0.3	7	V
Input R_R	$V_{I\,RR}$	−0.3	7	V
Input C_R	$I_{I\,CR}$	−10	10	mA
Input comparator K2, K5, K7	$V_{IK\,2,5,7}$	−0.3	33	V
Output K5	$V_{QK\,5}$	−0.3	33	V
Reference voltage	$V_{Q\,ref}$	−0.3	V_{ref}	V
Input $C_{soft\,start}$	$V_{I\,soft\,start}$	−0.3	7	V
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		60	K/W

Operating range

Supply voltage TDA 4714 A	V_S	10.5	30	V
TDA 4714 B	V_S	11	30	V
Ambient temperature TDA 4714 A	T_{amb}	0	70	°C
TDA 4714 B	T_{amb}	−25	85	°C
Frequency range	f	40	100000	Hz
VCO frequency	f_{VCO}	40	250000	Hz
Ramp generator frequency	f_{RG}	40	250000	Hz

Characteristics		TDA 4714 A			TDA 4714 B			
		Lower limit B	typ	Upper limit A	Lower limit B	typ	Upper limit A	
Supply voltage	V_S	10.5		30	11		30	V
Ambient temperature	T_{amb}	0		70	−25		85	°C
Supply current $C_T = 1$ nF $f_{VCO} = 100$ kHz	I_S	8		16	8		20	mA
Reference								
Reference voltage $0 \text{ mA} < I_{ref} < 5$ mA	V_{ref}	2.35	2.5	2.65	2.45	2.5	2.55	V
Voltage change $V_S = 14 \text{ V} \pm 20\%$	ΔV_{ref}		8			8		mV
Voltage change $V_S = 25 \text{ V} \pm 20\%$	ΔV_{ref}		15			15		mV
Voltage change $0 \text{ mA} < I_{ref} < 5$ mA	ΔV_{ref}			5			15	mV
Temperature coefficient	TC		0.25	0.4		0.25	0.4	mV/K
Response threshold of I_{ref} overcurrent	I_{ref}		10			10		mA
Oscillator (VCO)								
Frequency range	f	40		100000	40		100000	Hz
Frequency change $V_S = 14 \text{ V} \pm 20\%$	$\Delta f/f$		0.5			0.5		%
Frequency change $V_S = 25 \text{ V} \pm 20\%$	$\Delta f/f$	−1		1	−1		1	%
Tolerance $\Delta R_T = 0; \Delta C_T = 0$	$\Delta f/f$	−7		7	−7		7	%
Fall time sawtooth								
$C_T = 1$ nF			1			1		µs
$C_T = 10$ nF			10			10		µs
RC combination	C_T	0.82		47	0.82		47	nF
VCO	R_T	5		700	5		700	kΩ
Ramp generator								
Frequency range	f_{RG}	40		100 000	40		100 000	Hz
Maximum voltage at C_R	V_H		5.5			5.5		V
Minimum voltage at C_R	V_L		1.8			1.8		V
Input current through R_R	I_{RR}	0		400	0		400	µA
Current transformation ratio	I_{RR}/I_{CR}		1/4			1/4		

		TDA 4714 A			TDA 4714 B			
		Lower limit B	typ	Upper limit A	Lower limit B	typ	Upper limit A	
Comparator K2								
Input current	$-I_{K2}$			2			2	µA
Turn-off delay time[1]	$t_{d\,off}$			500			500	ns
Input voltage	$V_{I\,K2}$							
Duty cycle $\nu = 0$			1.8			1.8		V
Duty cycle ν = max.			5			5		V
Common-mode input voltage range	V_{IC}	0		5.5	0		5.5	V
Soft start K 3, K 4								
Charging current for $C_{soft\,start}$	I_{ch}		6			6		µA
Discharging current for $C_{soft\,start}$	I_{dch}		2			2		µA
Upper limiting voltage	V_{lim}		5			5		V
Switching voltage K4	V_{K4}		1.5			1.5		V
Output stages Q1, Q2								
Output voltage	V_{QH}			30			30	V
$I_Q = 20$ mA	V_{QL}			1.1			1.1	V
Output current $V_{QH} = 30$ V	I_Q			2			2	µA
Dynamic current limitation K 7								
Common-mode input voltage range	V_{IC}	0		4	0		4	V
Input offset voltage	V_{IO}	−10		10	−10		10	mV
Input current	$-I_I$			2			2	µA
Turn-off delay time[1]	$t_{d\,off}$		250			250		ns
Error detection time[1]	t		50			50		ns
Overvoltage K 5								
Switching voltage	V	$V_{ref}-$ 30		$V_{ref}+$ 30	$V_{ref}-$ 30		$V_{ref}+$ 30	V mV
Input current	$-I_I$			2			2	µA
Turn-off delay time[2]	$t_{d\,off}$		250			250		ns
Error detection time[2]	t		50			50		ns
Supply undervoltage								
Turn-on threshold for V_S, rising	V_S	8.8		10.5	8.8		11	V
Turn-on threshold for V_S, falling	V_S	8.5		10	8.5		10.5	V

1) At the input: step function $\Delta V = -100$ mV ⌐→ $\Delta V = +100$ mV
2) At the input: step function $V_{ref} = -100$ mV ⌐→ $V_{ref} = +100$ mV

Dimensioning notes for RC network

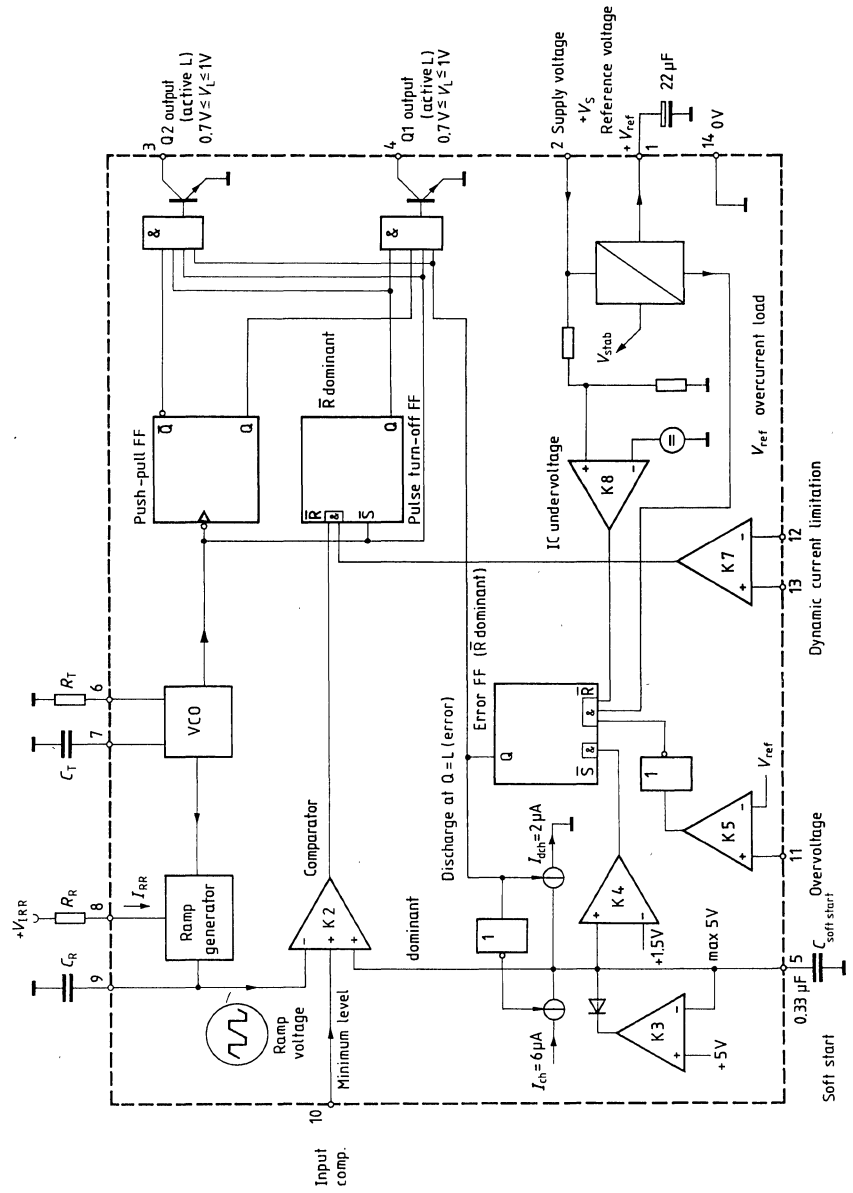
1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.

2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.

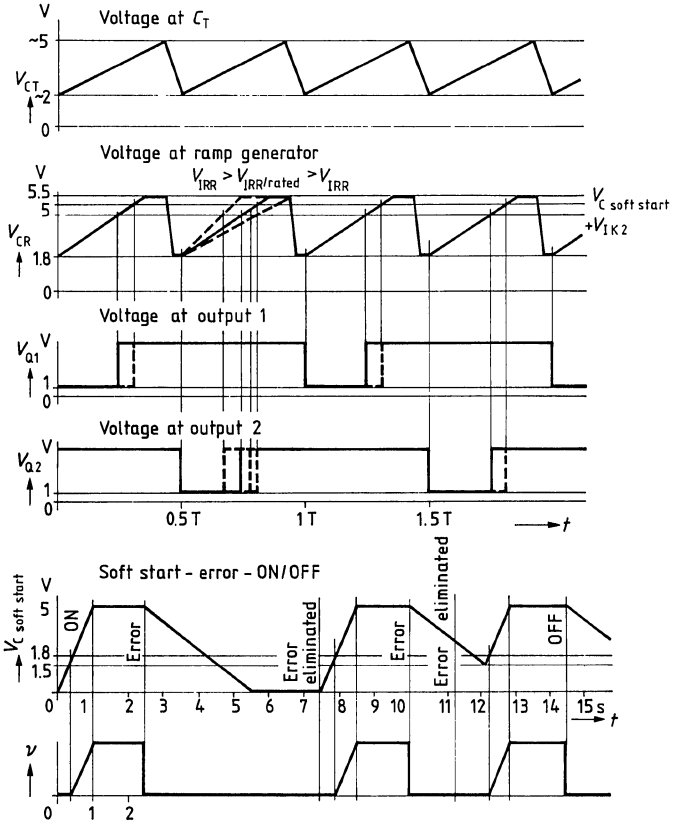
3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.

4. Duration of the soft start process
   → selection of $C_{soft\ start}$.

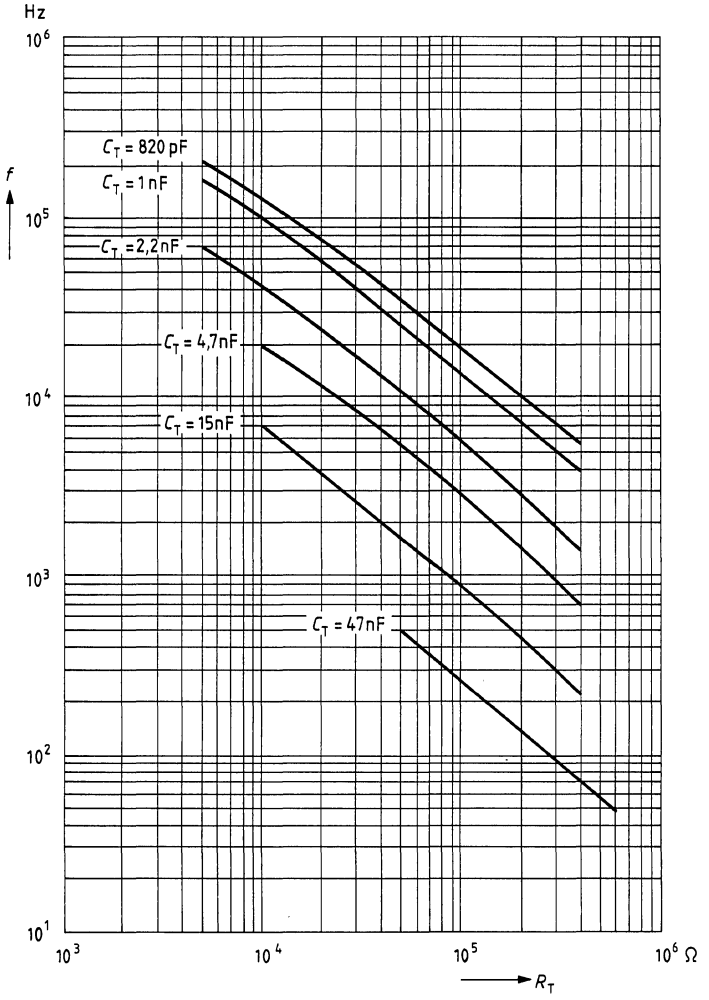
Block diagram



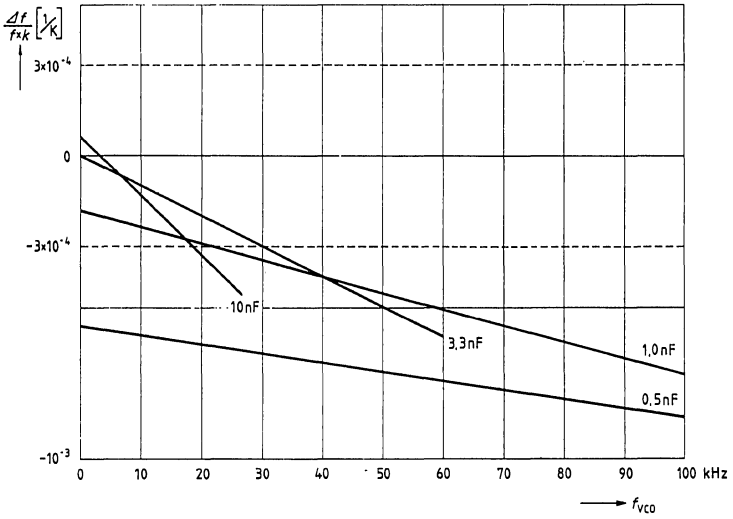
Pulse diagram



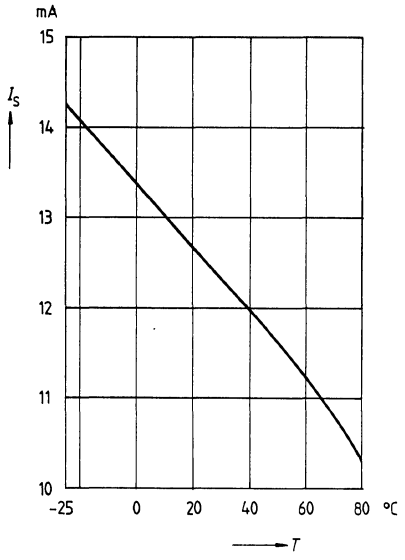
VCO frequency versus R_T and C_T



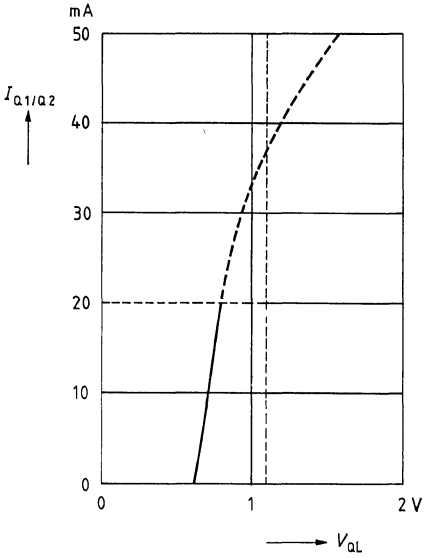
VCO temperature response
$V_S = 12$ V; $\nu = \max.$
$\frac{\Delta f_{VCO}}{f_K \times K} \left[\frac{1}{K}\right]$ with C_T as parameter



Supply current versus temperature



Output current versus L output voltage



TDA 4716A/TDA 4716B
IC for
Switched-Mode Power Supplies

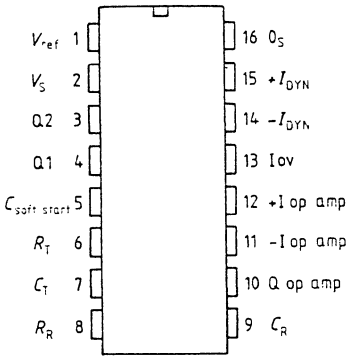
Bipolar IC

This versatile, 16-pin SMPS IC comprises digital and analog functions which are required to design high-quality flyback, single-ended, and push-pull converters in normal, half-bridge and full-bridge configurations. The component can also be used in single-ended voltage multipliers and speed-controlled motors. Malfunctions in electrical operation are recognized by the integrated op amps, and activate protective functions.

Features

- Push-pull outputs (open collector)
- Double pulse suppression
- Dynamic current limitation
- Overvoltage protection
- IC undervoltage protection
- Reference voltage source (± 2% for TDA 4716 B)
- Reference overload protection
- Feed-forward control
- Operational amplifier
- Soft start

Pin configuration
top view



Pin designation

Pin. No.	Function
1	Reference voltage V_{ref}
2	Supply voltage V_S
3	Output Q 2
4	Output Q 1
5	Soft start $C_{soft\ start}$
6	VCO R_T
7	VCO C_T
8	Ramp generator R_R
9	Ramp generator C_R
10	Operational amplifier output
11	Operational amplifier input (−)
12	Operational amplifier input (+)
13	Input overvoltage
14	Dynamic current limitation (−)
15	Dynamic current limitation (+)
16	0_S

(TDA 4716A/4716B - Plastic 16 pin DIL package)

Circuit description

The following is a description of the individual functional units and their interaction.

Voltage controlled oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximalety the frequency, is determined by the value of R_T. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage at comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.

Push-pull flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the two plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational amplifier K1

The op amp K1 is a high-quality amplifier. Fluctuations in the output voltage of the power supply are amplified by K1 and applied to the free + input of comparator K2. Variations in output voltage are, in this way, converted to a corresponding change in output duty cycle. K1 has a common-mode input voltage range between 0 V and +5 V.

Pulse turn-off flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage of capacitance $C_{\text{soft start}}$ (and also at K2!) to a maximum of 5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{soft\ start}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft start

The lower one of the two voltages at the plus inputs of K2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{soft\ start}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA at the maximum value of 5 V. In case of an error, $C_{soft\ start}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{soft\ start}$ exceeds 1.8 V.

Error flipflop

Error signals, which are led to input $\overline{R}$ of the error flipflop cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again using the soft start.

Comparator K5, K8, V_{ref} overcurrent load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start.

Comparator K7

K7 serves to recognize overcurrents. This is the reason why both inputs of the operational amplifier have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start. K7 has a common-mode input voltage range between 0 V and +4 V. The delay time between occurrence of an error and disabling of the outputs is only 250 ns.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are actively low. The time in which only one of the two outputs is conductive can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously. The minimum L voltage is 0.7 V.

Reference voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.3	33	V
Voltage at Q1, Q2 Q 1/2 high	V_Q	−0.3	33	V
Current at Q1, Q2 Q 1/2 low	I_Q		70	mA
Input R_T	$V_{I\,RT}$	−0.3	7	V
Input C_T	$V_{I\,CT}$	−0.3	7	V
Input R_R	$V_{I\,RR}$	−0.3	7	V
Input C_R	$I_{I\,CR}$	−10	10	mA
Input comparator K5, K7	$V_{IK\,5,7}$	−0.3	33	V
Output K5	$V_{QK\,5}$	−0.3	33	V
Input op amp	$V_{I\,op\,amp}$	−0.3	33	V
Output op amp	$V_{Q\,op\,amp}$	−0.3	V_S-1 but max. 7 V	V
Reference voltage	$V_{Q\,ref}$	−0.3	V_{ref}	V
Input $C_{soft\,start}$	$V_{I\,soft\,start}$	−0.3	7	V
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		60	K/W

Operating range

Supply voltage TDA 4716 A	V_S	10.5	30	V
TDA 4716 B	V_S	11	30	V
Ambient temperature TDA 4716 A	T_{amb}	0	70	°C
TDA 4716 B	T_{amb}	−25	85	°C
Frequency	f	40	100000	Hz
VCO frequency	f_{VCO}	40	250000	Hz
Ramp generator frequency	f_{RG}	40	250000	Hz

Characteristics

		TDA 4716 A			TDA 4716 B			
		Lower limit B	typ	Upper limit A	Lower limit B	typ	Upper limit A	
Supply voltage	V_S	10.5		30	11		30	V
Ambient temperature	T_{amb}	0		70	−25		85	°C
Supply current $C_T = 1$ nF $f_{VCO} = 100$ kHz	I_S	8		16	8		20	mA
Reference								
Reference voltage 0 mA $< I_{ref} <$ 5 mA	V_{ref}	2.35	2.5	2.65	2.45	2.5	2.55	V
Voltage change $V_S = 14$ V ± 20%	ΔV_{ref}		8			8		mV
Voltage change $V_S = 25$ V ± 20%	ΔV_{ref}		15			15		mV
Voltage change 0 mA $< I_{ref} <$ 5 mA	ΔV_{ref}			5			15	mV
Temperature coefficient	TC		0.25	0.4		0.25	0.4	mV/K
Response threshold of I_{ref} overcurrent	I_{ref}		10			10		mA
Oscillator (VCO)								
Frequency range	f	40		100000	40		100000	Hz
Frequency change $V_S = 14$ V ± 20%	$\Delta f/f$		0.5			0.5		%
Frequency change $V_S = 25$ V ± 20%	$\Delta f/f$	−1		1	−1		1	%
Tolerance $\Delta R_T = 0; \Delta C_T = 0$	$\Delta f/f$	−7		7	−7		7	%
Fall time sawtooth								
$C_T =$ 1 nF			1			1		µs
$C_T = 10$ nF			10			10		µs
RC combination	C_T	0.82		47	0.82		47	nF
VCO	R_T	5		700	5		700	kΩ
Ramp generator								
Frequency range	f_{RG}	40		100000	40		100000	Hz
Maximum voltage at C_R	V_H		5.5			5.5		V
Minimum voltage at C_R	V_L		1.8			1.8		V
Input current through R_R	I_{RR}	0		400	0		400	µA
Current transformation ratio	I_{RR}/I_{CR}		1/4			1/4		

		TDA 4716 A			TDA 4716 B			
		Lower limit B	typ	Upper limit A	Lower limit B	typ	Upper limit A	
Comparator K2								
Input current	$-I_{K2}$			2			2	µA
Turn-off delay time[1]	$t_{d\,off}$			500			500	ns
Input voltage	$V_{I\,K2}$							
Duty cycle $\nu = 0$			1.8			1.8		V
ν = max			5			5		V
Common-mode input voltage range	V_{IC}	0		5.5	0		5.5	V
Soft start K 3, K 4								
Charging current for $C_{soft\,start}$	I_{ch}		6			6		µA
Discharging current for $C_{soft\,start}$	I_{dch}		2			2		µA
Upper limiting voltage	V_{lim}		5			5		V
Switching voltage K4	V_{K4}		1.5			1.5		V
Operational amplifier								
Open-loop voltage gain	G_{V0}	60	80		60	80		dB
Input offset voltage	V_{IO}	−10		10	−10		10	mV
Temperature coefficient of V_{IO}	TC	−30		30	−30		30	µV/K
Incupt current	$-I_I$			2			2	µA
Common-mode input voltage range	V_{IC}	0		5	0		5	V
Output current	I_Q	−3		1.5	−3		1.5	mA
Rise time of output voltage	$\Delta V/\Delta t$		1			1		V/µs
Transition frequency	f_T		3			3		MHz
Phase at f_T	φ_T		120			120		degr
Output voltage $-3\ mA < I < 1.5\ mA$	$V_{Q\,H/L}$	1.5		5.5	1.5		5.5	V
Output stages Q1, Q2								
Output voltage	V_{QH}			30			30	V
$I_Q = 20$ mA	V_{QL}			1.1			1.1	V
Output current $V_{QH} = 30$ V	I_Q			2			2	µA
Dynamic current limitation K 7								
Common-mode input voltage range	V_{IC}	0		4	0		4	V
Input offset voltage	V_{IO}	−10		10	−10		10	mV
Input current	$-I_I$			2			2	µA
Turn-off delay time[1]	$t_{d\,off}$		250			250		ns
Error detection time[1]	t		50			50		ns

1) At the input: step function $\Delta V = -100$ mV ⌐→ $\Delta V = +100$ mV

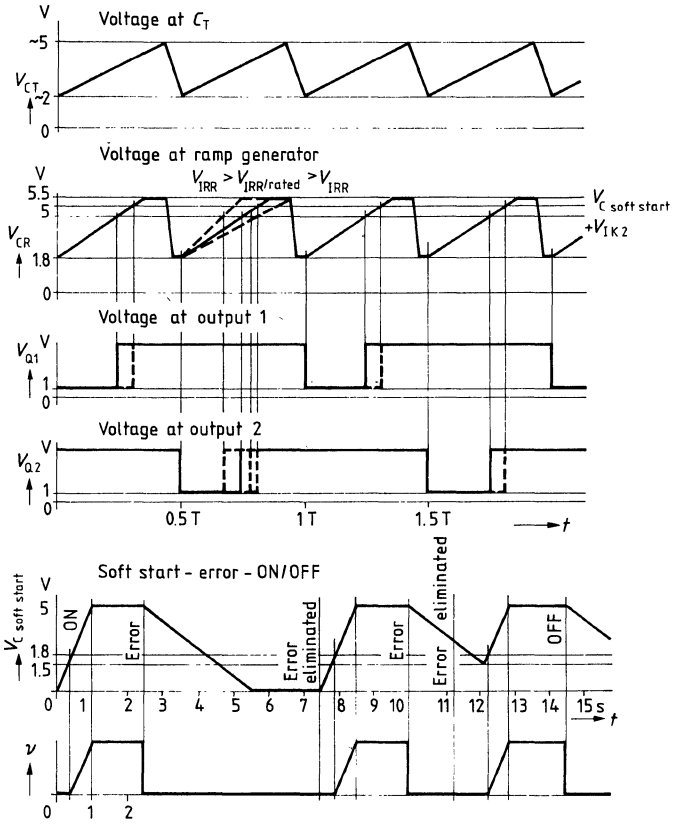
		TDA 4716 A			TDA 4716 B			
		Lower limit B	typ	Upper limit A	Lower limit B	typ	Upper limit A	
Overvoltage K 5								
Switching voltage	V	$V_{ref}-$ 30		$V_{ref}+$ 30	$V_{ref}-$ 30		$V_{ref}+$ 30	V mV
Input current	$-I_I$			2			2	µA
Turn-off delay time[1]	$t_{d\,off}$		250			250		ns
Error detection time[1]	t		50			50		ns
Supply undervoltage								
Turn-on threshold for V_S, rising	V_S	8.8		10.5	8.8		11	V
Turn-on threshold for V_S, falling	V_S	8.5		10	8.5		10.5	V

Dimensioning notes for RC network

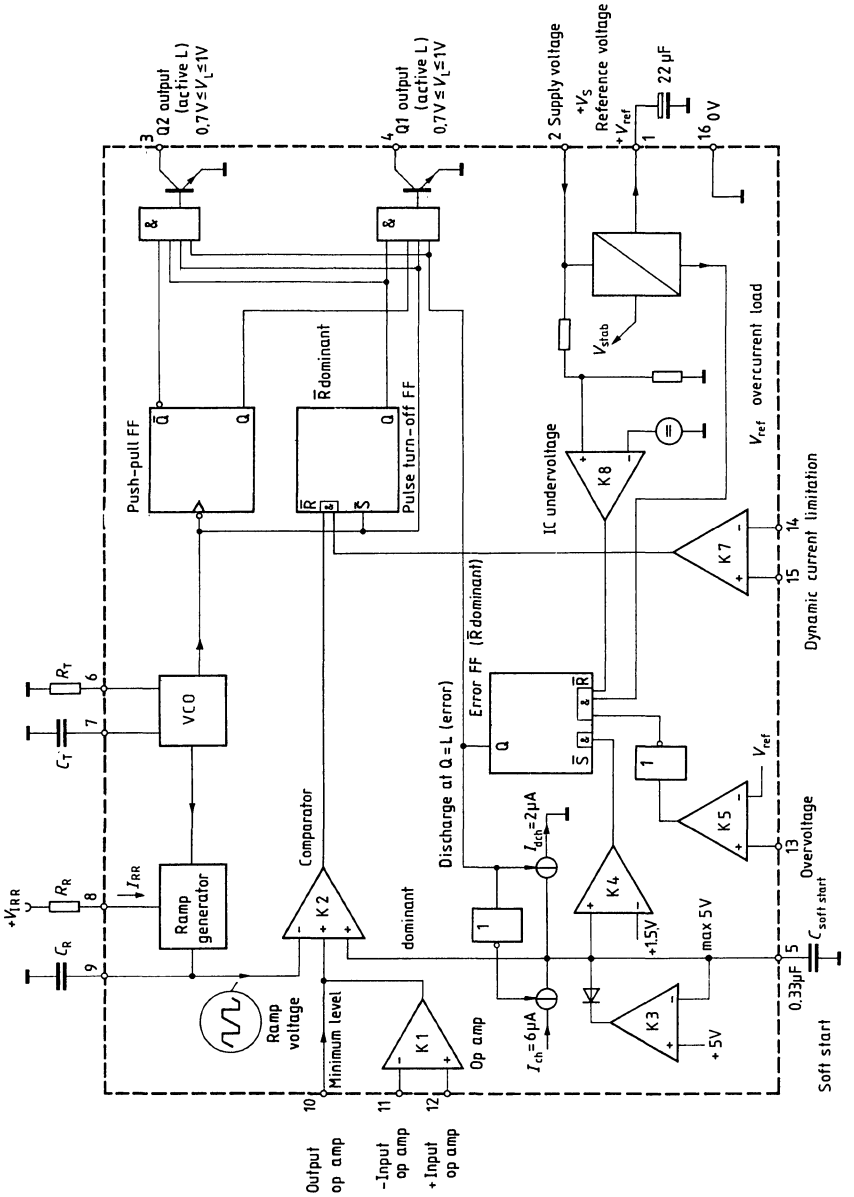
1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.
2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.
3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.
4. Duration of the soft start process
   → selection of $C_{soft\,start}$
5. Wiring of the operational amplifier according to the dynamic requirements

1) At the input: step function $V_{ref} = -100$ mV ⌟→ $V_{ref} = +100$ mV

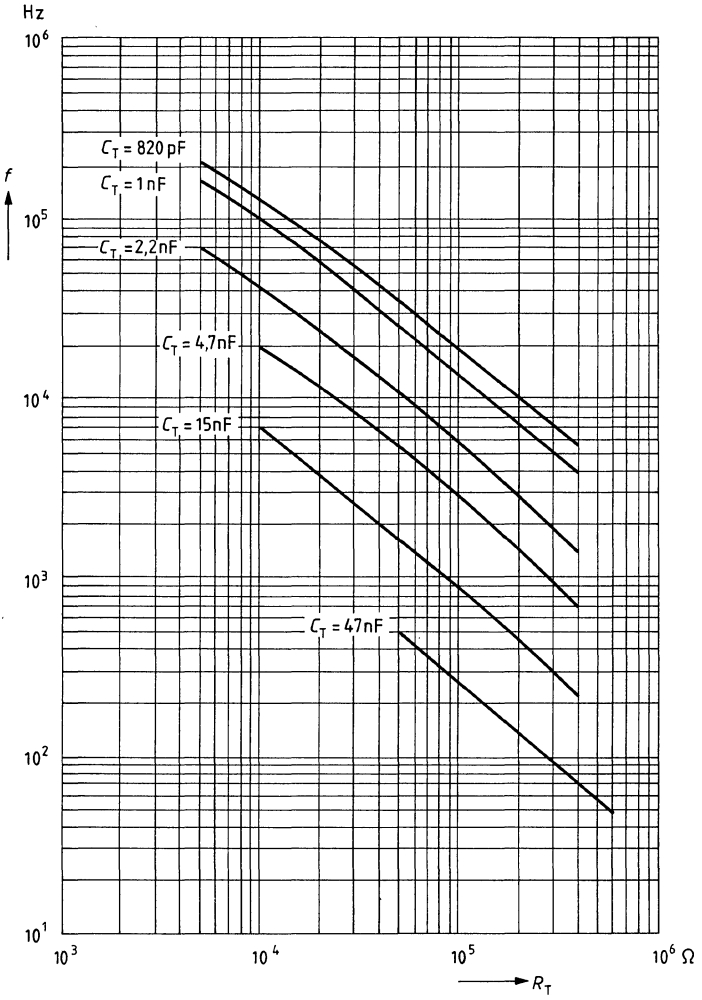
Pulse diagram



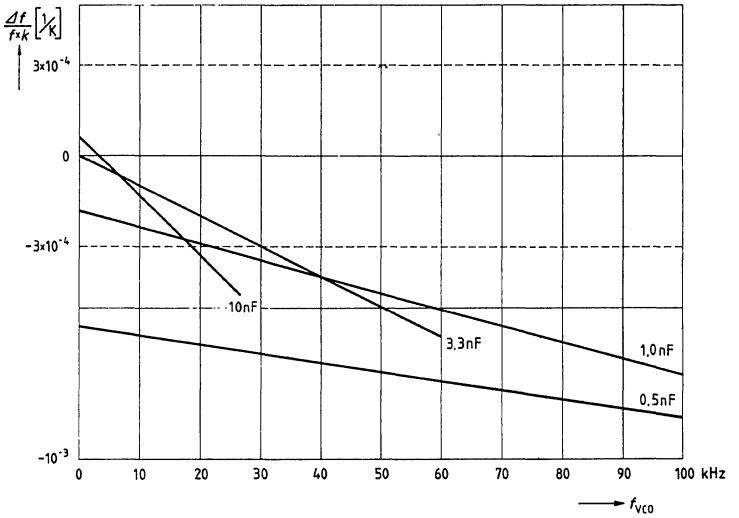
Block diagram



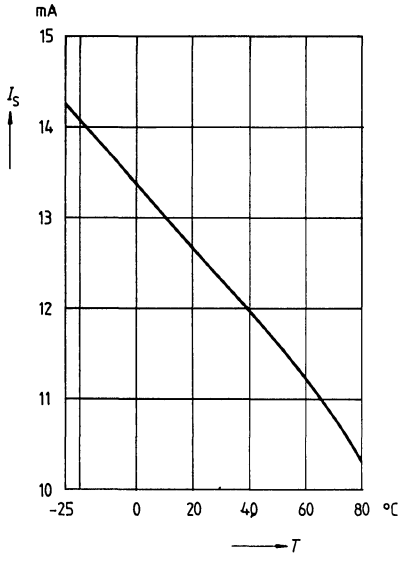
VCO frequency versus R_T and C_T



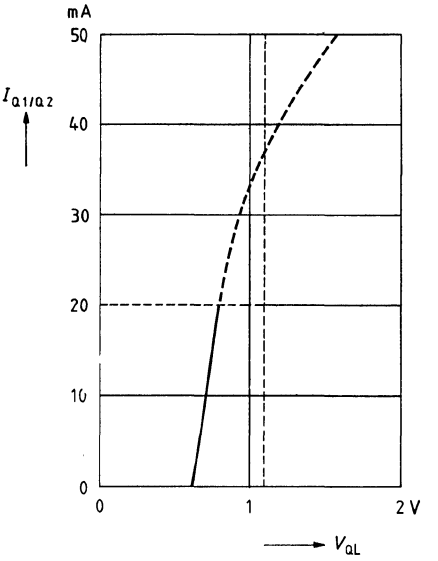
VCO temperature response
V_S = 12 V; ν = max.
$\frac{\Delta f_{VCO}}{f_K \times K}$ $\left[\frac{1}{K}\right]$ with C_T as parameter



Supply current versus temperature



Output current versus L output voltage



TDA 4718/TDA 4718A Control IC for Single-Ended and Push-Pull Switched-Mode Power Supplies

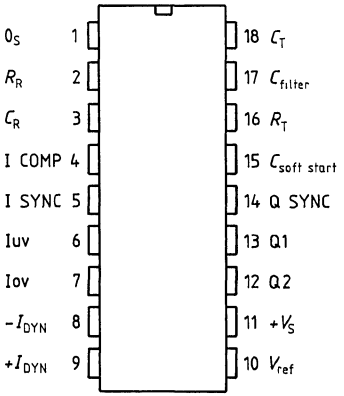
Bipolar IC

This 18-pin SMPS control IC comprises digital and analog functions which are required to design high-quality flyback, single-ended, and push-pull converters in normal and half-bridge configurations. In addition to the control functions, the circuit contains operational amplifiers which detect malfunctions during electrical operation and suitable protective measures. A PLL circuit for synchronization is one of the special advantages offered by this IC in addition to the following features:

- Feed-forward control (line hum suppression)
- Push-pull outputs
- Dynamic current limitation
- Overvoltage protection
- Undervoltage protection
- Soft start
- Double pulse suppression

(TDA 4718 - Ceramic 18 pin DIL package)
(TDA 4718A - Plastic 18 pin DIL package)

Pin configuration
top view



Pin designation

Pin No.	Function
1	0_S
2	Ramp generator R_R
3	Ramp generator C_R
4	+ input comparator K 2
5	Sync input
6	Input undervoltage, ON/OFF
7	Input overvoltage
8	Input dynamic current limitation (−)
9	Input dynamic current limitation (+)
10	Reference voltage V_{ref}
11	Supply voltage V_S
12	Output Q 2
13	Output Q 1
14	Sync output
15	Soft start
16	VCO R_T
17	Capacitance C_{filter}
18	VCO C_T

Circuit description

Voltage controlled oscillator (VCO)

The VCO generates a sawtooth voltage. The duration of the falling edge is determined by the value of C_T. The duration of the rising edge of the waveform and, therefore, approximately the frequency, is determined by the value of R_T. By varying the voltage at C_{filter}, the oscillator frequency can be changed by its rated value. During the fall time, the VCO provides a trigger signal for the ramp generator, as well as an L signal for a number of IC parts to be controlled.

Ramp generator

The ramp generator is triggered by the VCO and oscillates at the same frequency. The duration of the falling edge of the ramp generator waveform is to be shorter than the fall time of the VCO. To control the pulse width at the output, the voltage of the rising edge of the ramp generator signal is compared with a dc voltage comparator K2. The slope of the rising edge of the ramp generator signal is controlled by the current through R_R. This offers the possibility of an additional, superimposed control of the output duty cycle. **This additional control capability, called »feed-forward control«, is utilized to compensate for known interference such as ripple on the input voltage.**

Phase comparator

If the component is operated without external synchronization, the sync input must be connected to the sync output for the phase comparator to set the rated voltage at C_{filter}. The VCO then oscillates with rated frequency. In the case of external synchronization, other components can be synchronized with the sync output. **The component can be frequency-synchronized, but not phase-synchronized, with the sync input.** The duty cycle of the square-wave voltage at the sync input is arbitrary. The best stability as to small phase and frequency interference is achieved with a duty cycle as offered by the sync output.

Push-pull flipflop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K2

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge exceeds the lower of the plus levels, both outputs are disabled via the pulse turn-off flipflop. The period during which the respective, active output is low can be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Pulse turn-off flipflop

The pulse turn-off flipflop enables the outputs at the start of each half cycle. If an error signal from comparator K7 or a turn-off signal from K2 is present, the outputs will immediately be switched off.

Comparator K3

Comparator K3 limits the voltage at capacitance $C_{soft\ start}$ (and also at K2!) to a maximum of + 5 V. The voltage at the ramp generator output may, however, rise to 5.5 V. With a corresponding slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value.

Comparator K 4

The comparator has its switching threshold at 1.5 V and sets the error flipflop with its output if the voltage at capacitance $C_{soft\ start}$ is below 1.5 V. However, the error flipflop accepts the set signal only if no reset pulse (error) is applied. In this way the outputs cannot be turned on again as long as an error signal is present.

Soft start

The lower one of the two voltages at the plus inputs of K 2 is a measure for the duty cycle at the output. At the instant of turning on the component, the voltage at capacitor $C_{soft\ start}$ equals 0 V. As long as no error is present, this capacitor is charged with a current of 6 µA to the maximum value of 5 V. In case of an error, $C_{soft\ start}$ is discharged with a current of 2 µA. A set signal is pending at the error flipflop below a charge of 1.5 V and the outputs are enabled if no reset signal is pending simultaneously. As the minimum ramp generator voltage, however, is 1.8 V, the duty cycle at the outputs is actually increased slowly and continuously not before the voltage at $C_{soft\ start}$ exceeds 1.8 V.

Error flipflop

Error signals, which are led to input $\overline{R}$ of the error flipflop, cause an immediate disabling of the outputs, and after the error has been eliminated, the component to switch on again using the soft start.

Comparator K 5, K 6, K 8, V_{ref} overcurrent load

These are error detectors which cause immediate disabling of the outputs via the error flipflop when an error occurs. After elimination of the error, the component switches on again using the soft start.

Comparator K 7

K 7 serves to recognize overcurrents. This is the reason why both inputs of the op amp have been brought out. Turning on is resumed after error recovery at the beginning of the next half period but without using the soft start.

Outputs

Both outputs are transistors with open collectors and operate in a push-pull arrangement. They are actively low. The time in which only one of the two outputs is conductive, can be varied infinitely. The length of the falling edge at VCO is equal to the minimum time during which both outputs are disabled simultaneously.

Reference voltage

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be utilized in the external wiring of the op amp, the error comparators, the ramp generator, or other external components.

Maximum ratings

		Notes	Lower limit B	Upper limit A	
Supply voltage	V_S		−0.3	33	V
Voltage at Q1, Q2	V_Q	Q1, Q2 high	−0.3	33	V
Current at Q1, Q2	I_Q	Q1, Q2 low		70	mA
Sync output	$V_{SYNC\,Q}$	SYNC Q high	−0.3	7	V
	$I_{SYNC\,Q}$	SYNC Q low	0	10	mA
Sync input	$V_{SYNC\,I}$		−0.3	33	V
Input C_{filter}	$V_{I\,Cf}$		−0.3	7	V
Input R_T	$V_{I\,RT}$		−0.3	7	V
Input C_T	$V_{I\,CT}$		−0.3	7	V
Input R_R	$V_{I\,RR}$		−0.3	7	V
Input C_R	$I_{I\,CR}$		−10	10	mA
Input comparator					
K2, K5, K6, K7	$V_{I\,K}$		−0.3	33	V
Output K5	$V_{Q\,K5}$		−0.3	33	V
Reference voltage	V_{ref}		−0.3	V_{ref}	V
Input $C_{soft\,start}$	$V_{I\,soft\,start}$		−0.3	7	V
Junction temperature	T_j			125	°C
Storage temperature	T_{stg}		−55	125	°C
Thermal resistance (system-air)					
TDA 4718	$R_{th\,SA}$			70	K/W
TDA 4718 A	$R_{th\,SA}$			60	K/W

Operating range

Supply voltage	V_S		10.5	30	V
Ambient temperature					
TDA 4718	T_{amb}		−25	85	°C
TDA 4718 A	T_{amb}		0	70	°C
Max. VCO frequency	f		40	250000	Hz
Ramp generator frequency	f_{RG}		40	250000	Hz

Characteristics $V_S = 11$ V to 30 V; $T_{amb} = -25$ °C to +85 °C		Test conditions	Lower limit B	typ	Upper limit A	
Supply current	I_S	$C_T = 1$ nF $f_{VCO} = 100$ kHz	8		20	mA
Reference						
Reference voltage	V_{ref}	$0\,mA < I_{ref} < 5$ mA	2.35	2.5	2.65	V
Reference voltage change	ΔV_{ref}	14 V ± 20%		8		mV
Reference voltage change	ΔV_{ref}	25 V ± 20%		15		mV
Reference voltage change	ΔV_{ref}	$0\,mA < I_{ref} < 5$ mA			15[1]	mV
Temperature coefficient	TC			0.25	0.4	mV/K
Response threshold of I_{ref} overcurrent	I_{ref}			10		mA
Oscillator (VCO)						
Frequency range	f_{VCO}		40		100000	Hz
Frequency change	$\Delta f/f_{VCO}$	14 V ± 20%		0.5		%
Frequency change	$\Delta f/f_{VCO}$	25 V ± 20%	−1		1	%
Tolerance	$\Delta f/f_{VCO}$	$\Delta R_T = 0, \Delta C_T = 0$	−7		7	%
Fall time sawtooth	t	$C_T = 1$ nF		1		µs
	t	$C_T = 10$ nF		10		µs
RC combination	C_T		0.82		47	nF
VCO	R_T		5		700	kΩ
Ramp generator						
Frequency range	f		40		100000	Hz
Maximum voltage at C_R	V_H			5.5		V
Minimum voltage at C_R	V_L			1.8		V
Input current through R_R	I_{RR}		0		400	µA
Current transformation ratio	I_{RR}/I_{CR}			1/4		
Synchronization						
Sync output	V_{QH}	$I_{QH} = -200$ µA	4			V
	V_{QL}	$I_{QL} = 1.6$ mA			0.4	V
Sync input	V_{IH}		2			V
	V_{IL}				0.8	V
Input current	$-I_I$				5	µA
Comparator K2						
Input current	$-I_{IK2}$				2	µA
Turn-off delay[2]	$t_{d\,off}$				500	ns
Input voltage	V_{IK2}	for duty cycle				
		$\nu = 0$		1.8		V
		$\nu = \max$		5		V
Common-mode input voltage range	V_{IC}		0		5.5	V

1) At $T_{amb} = 0$ °C to 70 °C, this value falls to max. 5 mV
2) At the input: step function $\Delta V = -100$ mV ⌐→ $\Delta V = +100$ mV

Characteristics V_S = 11 V to 30 V; T_{amb} = −25 °C to +85 °C		Test conditions	Lower limit B	typ	Upper limit A	
Soft start K3, K4						
Charging current for $C_{soft\ start}$	I_{ch}			6		µA
Discharging current for $C_{soft\ start}$	I_{dch}			2		µA
Upper limiting voltage	V_{lim}			5		V
Switching voltage K4	V_{K4}			1.5		V
Output stages Q1, Q2						
Output voltage	V_{QH}				30	V
	V_{QL}	I_Q = 20 mA			1.1	V
Output current	I_Q	V_{QH} = 30 V			2	µA
ON, OFF, undervoltage K6						
Switching voltage	V		V_{ref}−30 mV		V_{ref}+30 mV	V
Input current	$-I_I$				2	µA
Turn-off delay time[1]	$t_{d\ off}$			250		ns
Error detection time[1]	t			50		ns
Dynamic current limitation K7						
Common-mode input voltage	V_{IC}		0		4	V
Input offset voltage	V_{IO}		−10		10	mV
Input current	$-I_I$				2	µA
Turn-off delay time[2]	$t_{d\ off}$			250		ns
Error detection time[2]	t			50		ns
Overvoltage K5						
Switching voltage	V		V_{ref}−30 mV		V_{ref}+30 mV	V
Input current	$-I_I$				2	µA
Turn-off delay time[1]	$t_{d\ off}$			250		ns
Error detection time[1]	t			50		ns
Supply undervoltage						
Turn-on threshold for V_S	V_S		8.8		11	V
rising		0 °C<T_{amb}<70 °C			10.5	V
Turn-off threshold for V_S	V_S		8.5		10.5	V
falling		0 °C<T_{amb}<70 °C			10	V
Input C_{filter}						
Rated voltage for rated frequency	V_R			4		V
Frequency approx. proportional to voltage within the range	V_R		3		5	V
Voltage at open sync input	$V_{C\ filter}$			1.6		V

1) At the input: step function V_{ref} = −100 mV ⌐→ V_{ref} = +100 mV
2) At the input: step function ΔV = −100 mV ⌐→ ΔV = +100 mV

Dimensioning notes for RC network

1. Determination of the minimum time during which both outputs must be disabled
   → selection of C_T; selection of $C_R \leq C_T$.

2. Determination of the VCO frequency = 2 x output frequency
   → selection of R_T.

3. Determination of the rated slope of the rising ramp generator voltage, which the maximum possible turn-on period per half wave depends on
   → selection of R_R.

4. Duration of the soft start process
   → selection of $C_{soft\ start}$.

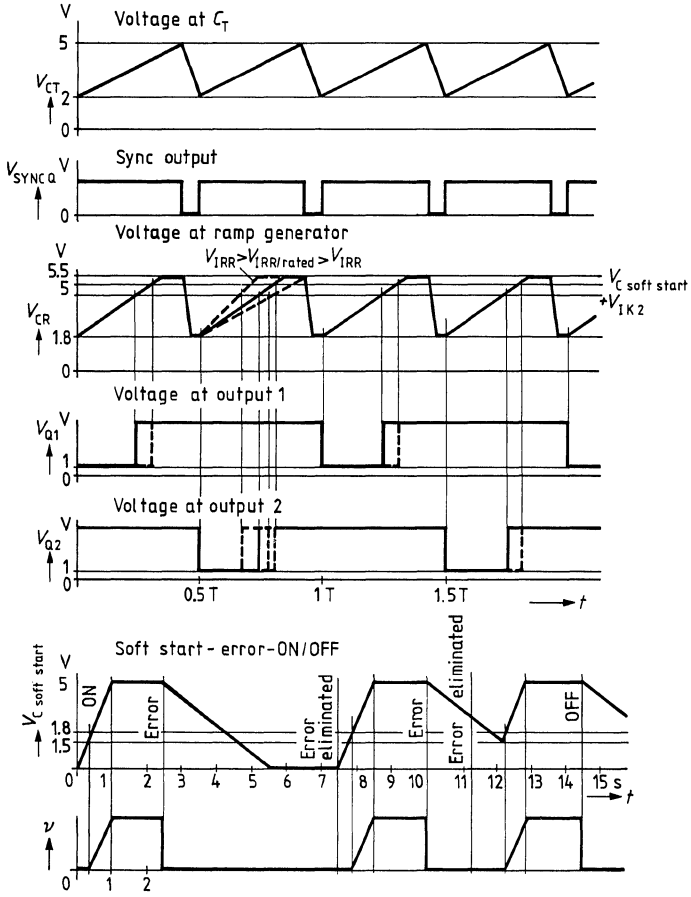
5. In the case of a free-running VCO: connect sync output with sync input.

6. Capacitance C_{filter} is not required in the free-running operation (sync input connected with sync output).

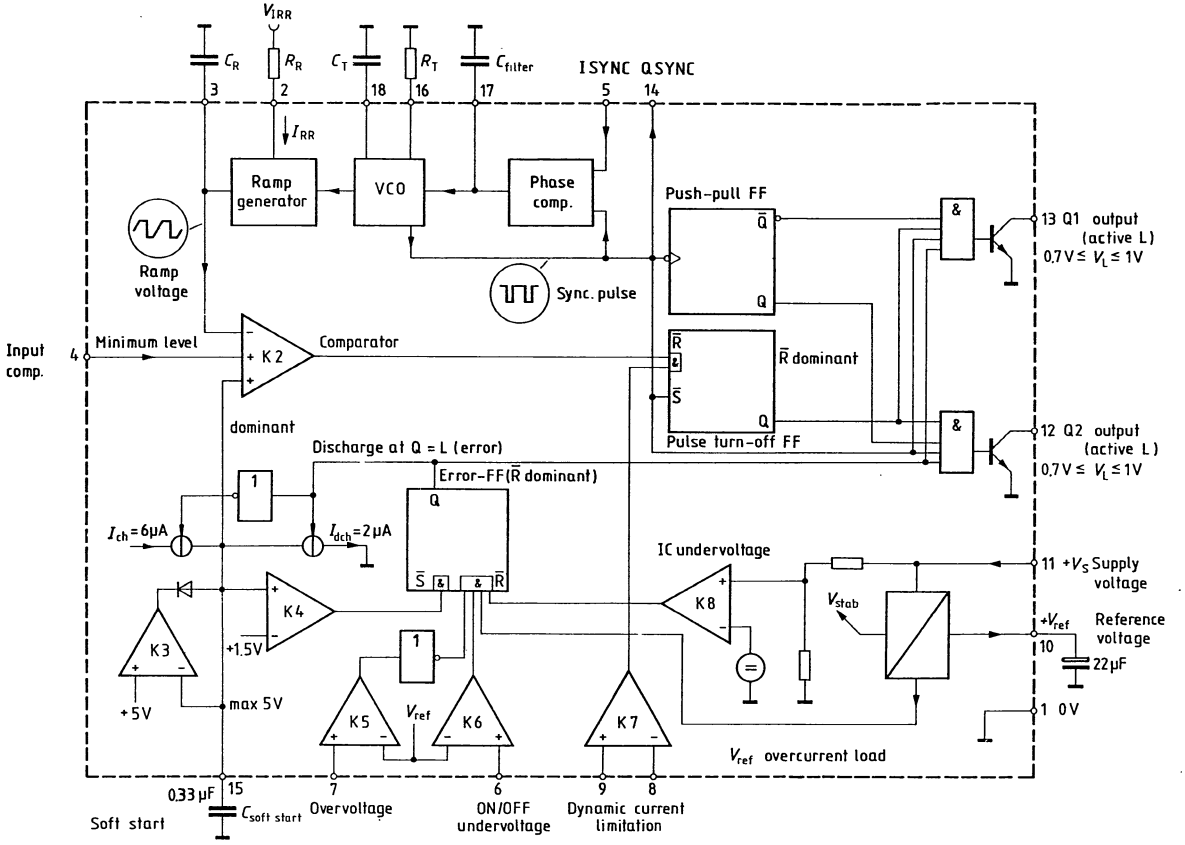
   In the case of external synchronization, that value depends on the selected operating frequency and the required maximum phase interference deviation.

Rated VCO frequency:	100 kHz	50 Hz
C_{filter} favorable:	10 nF	1 µF

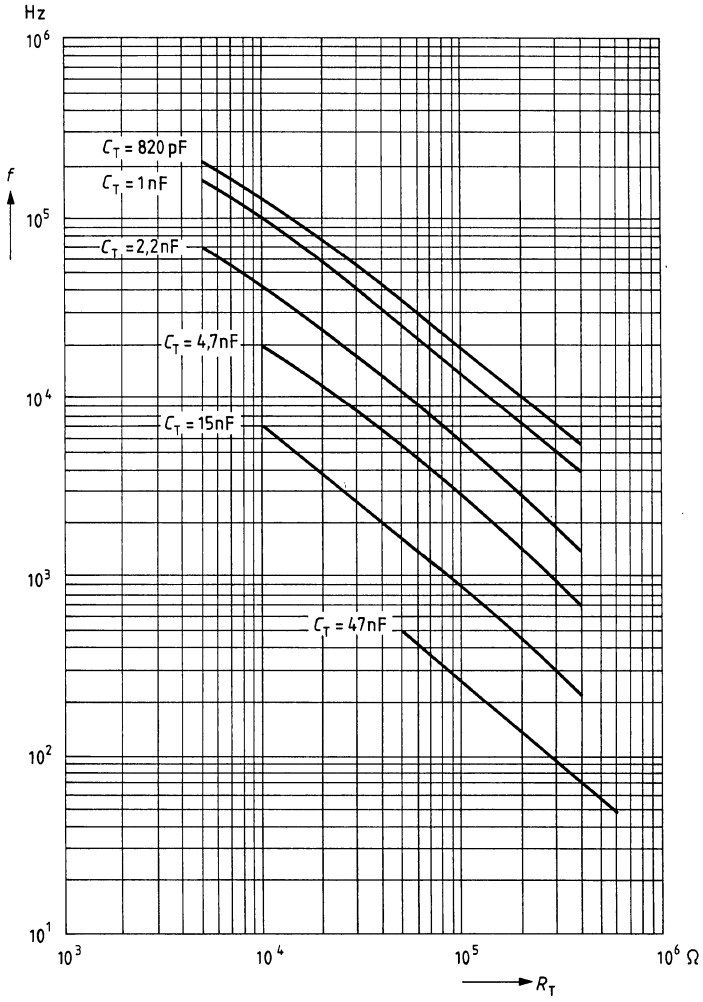
Pulse diagram



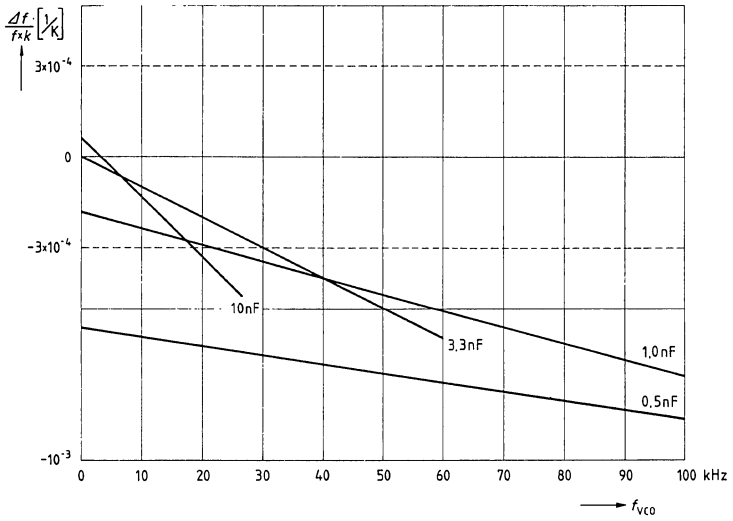
Block diagram



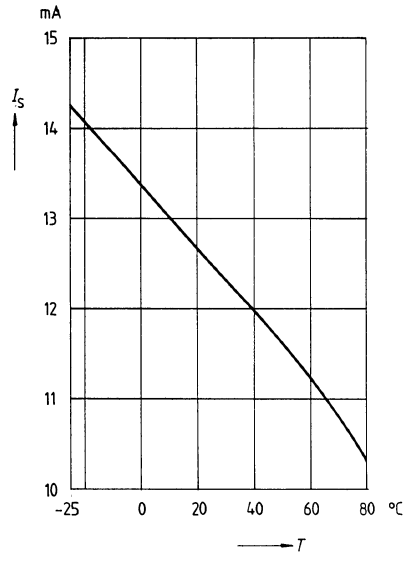
VCO frequency versus R_T and C_T



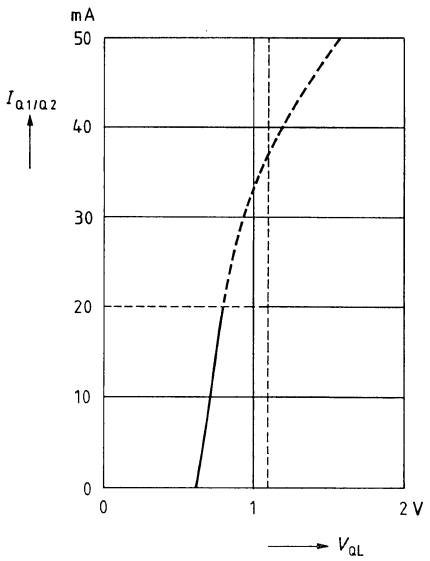
VCO temperature response
$V_S = 12$ V; ν = max.
$\frac{\Delta f_{VCO}}{f_K \times K}\left[\frac{1}{K}\right]$ with C_T as parameter



Current consumption versus temperature



Output current versus output voltage



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*See Consumer Data Book or contact your local Siemens Representative.

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