SIGNETICS
MICROCONTROLLER
8X300

signetics

I0 — 13
I1 — 14
I2 — 15
I3 — 16
I4 — 17
I5 — 18
I6 — 19
I7 — 20
I8 — 21
I9 — 22
I10 — 23
I11 — 24
I12 — 25
I13 — 26
I14 — 27
I15 — 28

A0 — 9
A1 — 8
A2 — 7
A3 — 6
A4 — 5
A5 — 4
A6 — 3
A7 — 2
A8 — 49
A9 — 48
A10 — 47
A11 — 46
A12 — 45

16-BIT INSTRUCTION BUS

SHIFT LOGIC

MERGE LOGIC

OVF

R1
R2
R3
R4
R5
R6
R11
AUX (R0)

INSTRUCTION REGISTER
0   15

IR8–IR15

IR3–IR7

ARITHMETIC LOGIC UNIT (ALU)
B
A
A ≠ 0

AR0–AR4
AR0–AR12
AR5–AR12

ADDRESS MULTIPLEXER

ADDRESS INCREMENT LOGIC

MASK LOGIC
(Note: Internal Working Registers Cannot be Masked)

RIGHT ROTATE LOGIC

INPUT/OUTPUT LATCHES

41 — IV0
40 — IV1
39 — IV2
38 — IV3
36 — IV4
35 — IV5
34 — IV6
33 — IV7

ADDRESS REGISTER (AR)
0   12

PROGRAM CTR (PC)
0   12

13-BIT ADDRESS BUS

R1 — General Working Register
R2 — General Working Register
R3 — General Working Register
R4 — General Working Register
R5 — General Working Register
R6 — General Working Register
R11 — General Working Register
AUX — General Working Register
Implied Operand for Arithmetic or Logical Operations.

OVF — The Least-Significant Bit of This Register is Used to Reflect Overflow Status Resulting From the Most Recent ADD Operation

INSTRUCTION REGISTER (R)
— Holds the 16-Bit Instruction Word Currently Being Executed.

PROGRAM COUNTER (PC)
— Normally Contains the Address of the Current Instruction and is Incremented to Obtain the Next Instruction Address.

ADDRESS REGISTER (AR)
— A 13-Bit Register Containing the Address of the Current Instruction

IR0–IR15
IR0–IR2

DECODE AND CONTROL LOGIC

INTERNAL CONTROL

RESET — 43
HALT — 44

29 — SC
30 — WC
31 — LB
32 — RB
42 — MCLK
37 — VCC

INTERNAL SUPPLY
1 — VCR

X1 — 10

OSC & TIMING GENERATOR
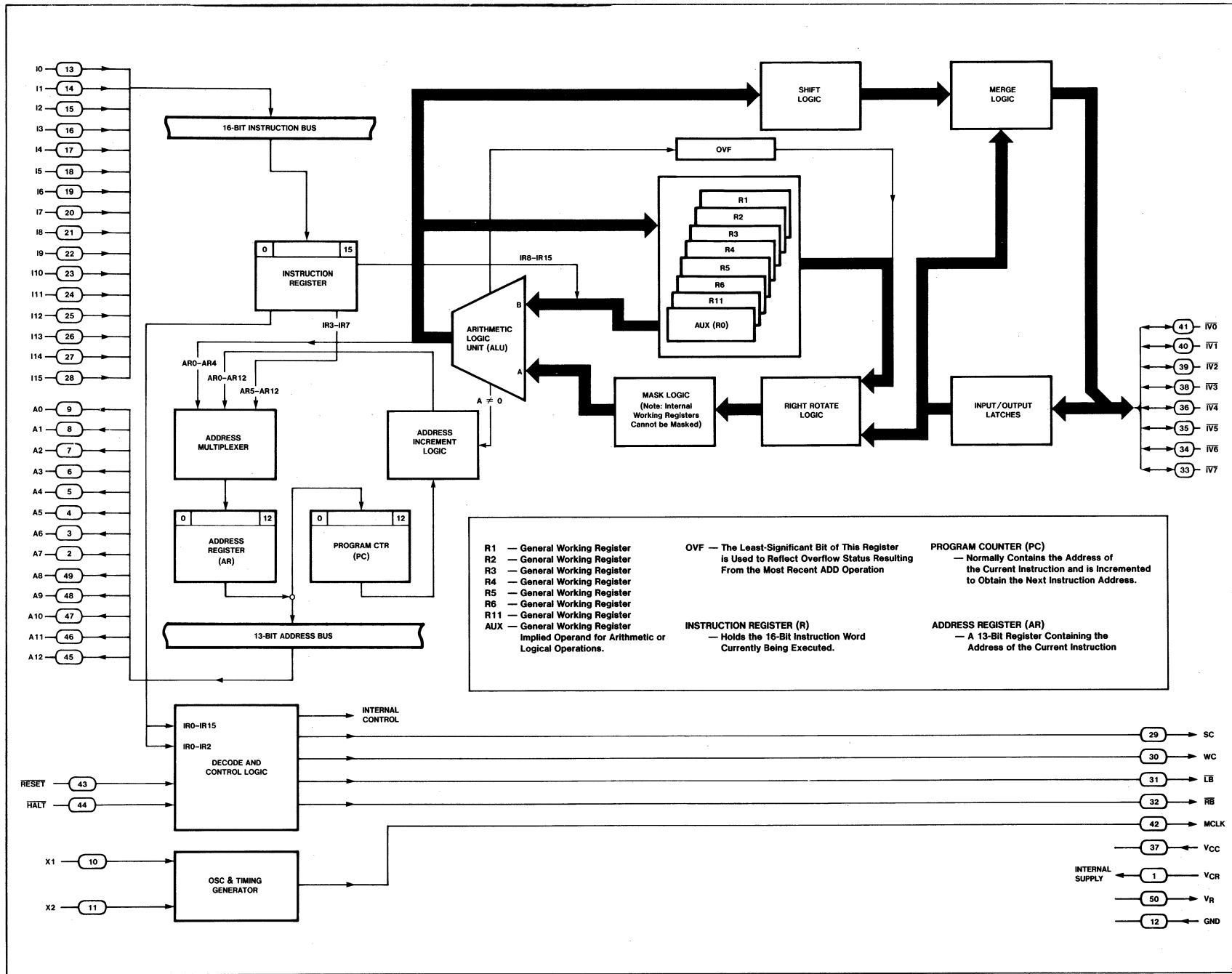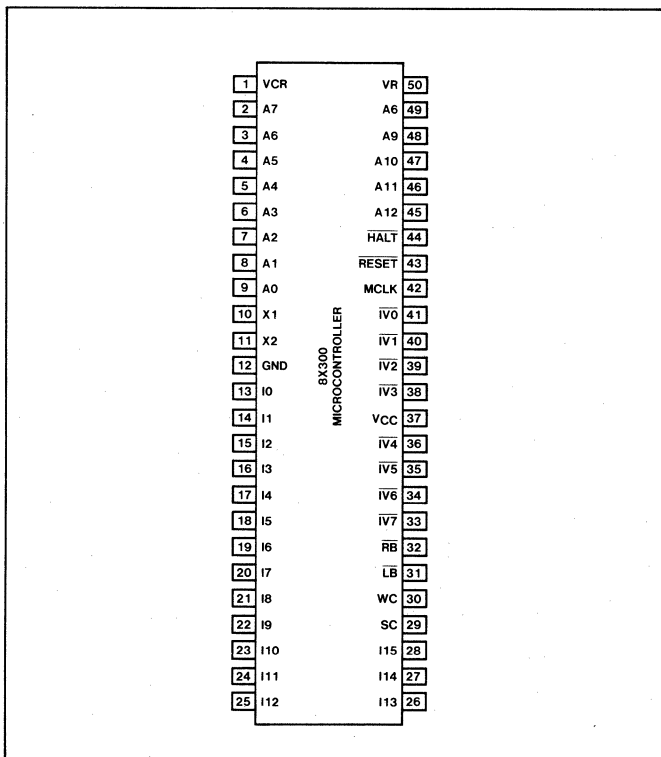
X2 — 11

50 — VR
12 — GND

Figure 1.   CPU Architecture and PIN Designations For 8X300 Microcontroller

ARCHITECTURAL OVERVIEW

The Signetics 8X300 Microcontroller (Figure 1) is a high-speed bipolar microprocessor implemented with low-power Schottky technology. The 8X300 brings together all the qualities needed—SPEED, FLEXIBILITY, and ECONOMY—for systems design in the many areas that require reliable bit stream management. Consider!—5V operation, TTL bus compatibility, and an on-chip clock—the result, a system with fewer parts. Consider!—the inherent power of LSI logic (programmable Rotate, Mask, Shift, and Merge functions in the data-processing path) and the ability to Fetch, Decode, and Execute a 16-bit instruction in a minimum of 250-nanoseconds—the result, a system with superior bit handling capabilities. Consider!—the 250ns cycle time in conjunction with extended microcode—the result, the flexibility of bit-slice devices with the programming ease of MOS microprocessors. Now, consider the results!—a device tailored to bit-stream management in the areas of Industrial Control, Input/Output Control, and Data Communications.

The 8X300 uses three separate buses—one for 13-bit instruction addresses, one for 16-bit instructions, and a bidirectional 8-bit input/output data bus; except for the I/O bus, there are no time multiplexing of functions.

PIN CONFIGURATION

1	VCR	VR	50
2	A7	A6	49
3	A6	A9	48
4	A5	A10	47
5	A4	A11	46
6	A3	A12	45
7	A2	HALT	44
8	A1	RESET	43
9	A0	MCLK	42
10	X1	IV0	41
11	X2	IV1	40
12	GND	IV2	39
13	I0	IV3	38
14	I1	VCC	37
15	I2	IV4	36
16	I3	IV5	35
17	I4	IV6	34
18	I5	IV7	33
19	I6	RB	32
20	I7	LB	31
21	I8	WC	30
22	I9	SC	29
23	I10	I15	28
24	I11	I14	27
25	I12	I13	26

8X300 MICROCONTROLLER

FEATURES

- **Fetch, Decode, and Execute a 16-bit instruction in a minimum of 250-nanoseconds (one machine cycle)**
- **Bit-oriented instruction set (addressable single-or-multiple bit subfields)**
- **Separate address, instruction, and I/O buses**
- **Source/destination architecture**
- **On-Chip oscillator and timing generation**
- **Eight 8-bit working registers**
- **TTL inputs and outputs**
- **BiPolar Low-Power Schottky technology**
- **3-State I/O bus**
- **Single +5V supply**

ORDERING INFORMATION

Commercial

Order number: N8X300I
Packaging information: Refer to Signetics price list
Supply voltage: 5V ($\pm$5%)
Operating temperature range: 0°C to +70°C

Military

Order number: S8X300-1
Packaging information: Refer to Signetics price list
Supply voltage: 5V ($\pm$5%)
Operating temperature range: −40°C to +100°C

Order number: S8X300-2
Packaging information: Refer to Signetics price list
Supply voltage: 5V ($\pm$10%)
Operating temperature range: −20°C to +100°C
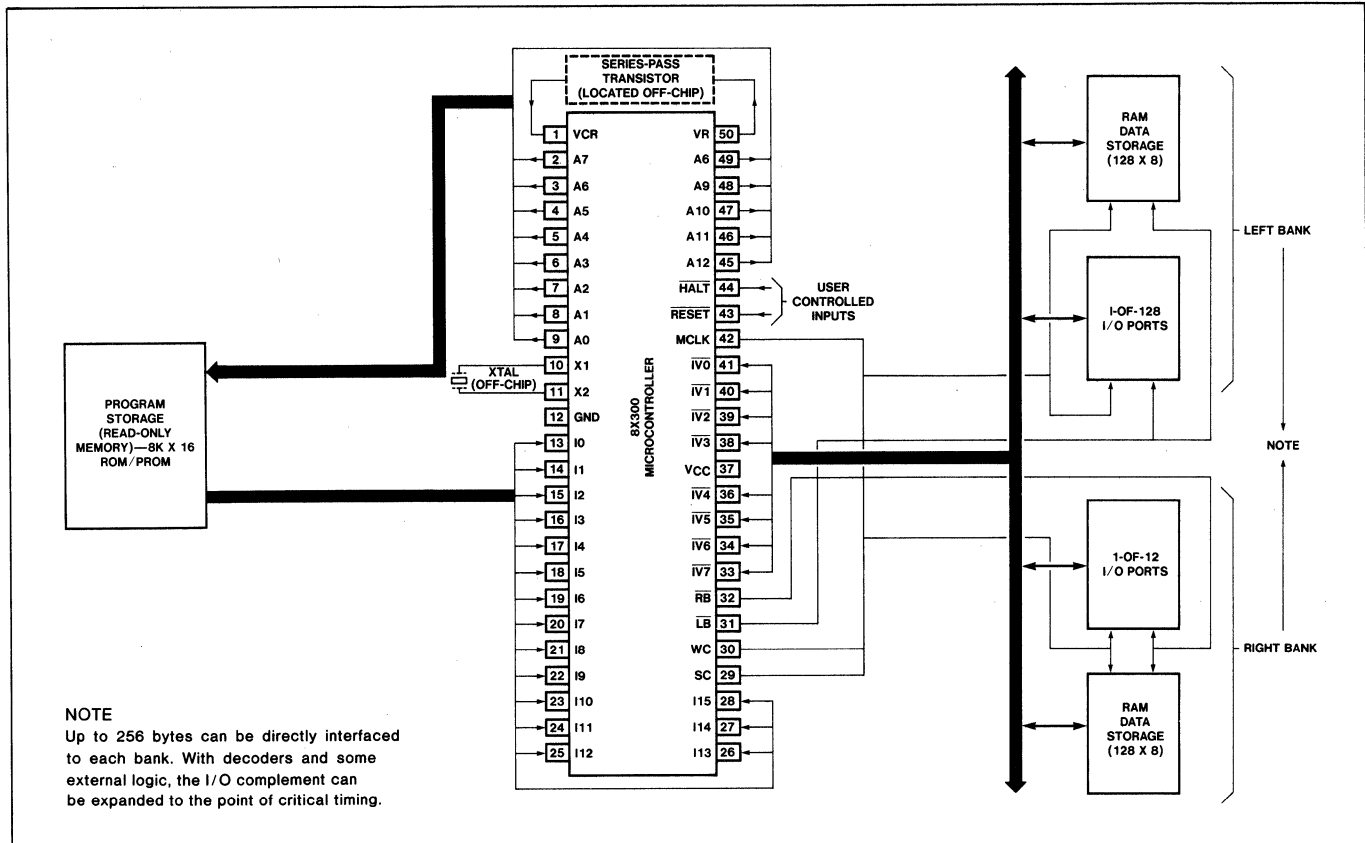
NOTE
Up to 256 bytes can be directly interfaced
to each bank. With decoders and some
external logic, the I/O complement can
be expanded to the point of critical timing.

PIN NO.	IDENTIFIER	NAME AND FUNCTION	ACTIVE STATE
2-9/45-49	A0-A12	**Program Address Lines:** These outputs permit direct addressing of up to 8192 words of program storage. A high voltage level equals a binary "1"; A12 is Least Significant Bit.	High
13-28	I0-I15	**Instruction Lines:** These input lines receive 16-bit instructions from program storage. A high voltage level equals a binary "1"; I15 is Least Significant Bit.	High
33-36 38-41	IV0-IV7	**Input/Output Bus:** These bidirectional three-state lines communicate with up to 512 I/O devices (256 per bank). A low voltage level equals a binary "1"; IV7 is Least Significant Bit.	Low
10 & 11	X1 & X2	**Connections** for a capacitor, a series-resonant crystal, or an external clock source with complementary outputs. For precise frequency control, a crystal or external source is required.	—
42	MCLK	**Master Clock:** This output is used for clocking I/O devices and/or synchronization of external logic.	High
30	WC	**Write Command:** When signal is high (binary 1), data is being output on pins IV0-IV7 of I/O bus.	High
29	SC	**Select Command:** When signal is high (binary 1), an address is being output on pins IV0-IV7 of I/O bus.	High
31	LB	When the LB signal is low (binary 0), any one of up-to-256 I/O devices (or memory locations) in the left bank can be accessed. When the address of a particular device (or memory location) matches the address on the IV bus, that particular device (or memory location) is enabled and selected for input/output operations. All addresses on the left bank that do not match are deselected.	Low
32	RB	When the RB signal is low (binary 0), any one of up-to-256 I/O devices (or memory locations) in the right bank can be accessed. When the address of a particular device (or memory location) matches the address on the I/O bus, that particular device (or memory location) is enabled and selected for input/output operations. All addresses on the right bank that do not match are deselected.	Low
43	RESET	When reset input is low (binary 0), the microcontroller is initialized—sets Program Counter/Address to zero and inhibits MCLK output.	Low
44	HALT	When halt input is low (binary 0), internal operation of microcontroller stops at the start of next instruction. The stop function does not inhibit MCLK or affect any internal registers.	Low
50	VR	Internally-generated reference output voltage for external series-pass transistor.	—
1	VCR	Regulated voltage input from series-pass transistor (2N5320 or equivalent).	—
12	GND	Circuit ground.	—
37	Vcc	Input connection for +5V power.	—

Figure 2.   Typical 8X300 System with Pin Definitions

TYPICAL 8X300 SYSTEM HOOKUP

Although the system hookup shown in Figure 2 is of the simplest form, it provides a fundamental look at the 8X300 microcontroller and peripheral relationships. As indicated, program storage can be either ROM or PROM and, by using various addressing-methods/decoding-schemes, memory paging techniques can be easily implemented. Also, by proper bit assignment, some external interface logic and, under software control, the program memory can be used as a storage device for interrupt-service subroutines. The user interface ($\overline{IV0}$ through $\overline{IV7}$) is capable of addressing 256 Input/Output ports and, with the additional bank-select bit ($\overline{LB}$ and $\overline{RB}$), the number of addressable I/O ports is 512— the left bank and right bank each consisting of 256 ports. The I/O ports of each bank can be used in a variety of ways; one of these ways is shown in Figure 2. When $\overline{LB}$ is active low, the left bank can be enabled and, providing there is an address match, anyone of 128 I/O ports or anyone of 128 locations within the RAM memory can be accessed for input/output operations. When $\overline{RB}$ is active low, the same set of conditions are applicable to the right bank. With some sacrifice in speed, any given I/O port can be interfaced to a memory peripheral or other I/O device of the user.

PROGRAM STORAGE INTERFACE

As shown in Figure 2, program storage is connected to output address lines A0 through A12 (A12 = LSB) and input instruction lines I0 through I15. An address output on A0/A12 identifies one 16-bit instruction word in program storage. The instruction word is subsequently input on I0/I15 and defines the microcontroller operations which are to follow.

The Signetics 82S115 PROM or any TTL-compatible memory can be used for program storage. (Note. The worst-case access time depends upon the instruction cycle time, and also, the overall system configuration.)

I/O INTERFACE AND CONTROL

An 8-bit I/O data bus is used by the microcontroller to communicate with two fields of I/O devices. The complementary $\overline{LB}$ and $\overline{RB}$ signals identify which field of the I/O devices is enabled.

Both data and address information are output on the I/O bus. The SC (Select Command) and WC (Write Command) signals distinguish between data and address information as follows:

SC	WC	FUNCTION
High	Low	I/O address is being output on the I/O (IV) bus
Low	High	I/O data is being output on the I/O (IV) bus
Low	Low	Input data expected from selected I/O device
High	High	Invalid (not generated by 8X300)

DATA PROCESSING

From a data processing point of view, the 8X300 microcontroller chip (Figure 1) contains eight 8-bit working registers (R1 through R6, R11, AUXiliary), an arithmetic logic unit (ALU), an overflow register (OVF), rotate/shift/mask/merge logic, and a bidirectional 8-bit I/O bus. Internal 8-bit data paths connect the registers and I/O bus to the ALU inputs, and the ALU output to the registers and I/O bus. Inputs to the ALU are preceded by the data-rotate and data-mask logic and the ALU output is followed by the shift and merge logic. Any one or all of the logic functions can operate on 8-bits of data in a single instruction cycle. Data from the source register can be right-rotated (end around) before processing by the ALU; external data (I/O bus) can also be masked to isolate a portion of the 8-bit field. Since the ALU always processes 8-bits of data, bit positions not specified by the mask operation are filled with zeroes.

When less than 8-bits of data are specified as output to the I/O bus from the ALU, the data field (shifted and masked, as required) is merged with prior contents of the I/O latches to form the output data. Bit positions of the I/O data not affected by the logic operations are not modified. Depending upon whether an I/O peripheral or an internal register is specified in the instruction as the source of data, the I/O latches contain, respectively, I/O-bus source data or destination data. For instance, when an internal register is specified as a source of data and an I/O peripheral as the destination, data from the peripheral is read into the I/O latches at the start of the instruction cycle; processed data is then merged with contents of the I/O latches to form the I/O output data at the end of the instruction cycle. When an I/O peripheral is specified as both data source and destination, data from the source is used both as the input to the I/O latches and as data to be processed; the processed data is then merged with data from the I/O latches to form the previously-described I/O bus output. If the data source and destination are on opposite banks of the 8X300 bus, the destination data is written with a full 8-bits, since the prior contents were not stored in the I/O latches.

INSTRUCTION CYCLE

Each microcontroller operation is executed in a single instruction cycle. The instruction cycle is divided into quarters with each quarter cycle being as short as 62.5-nanoseconds. Figure 3 shows the general functions that occur during each quarter cycle; specifics regarding minimum/maximum timing and other critical values are described under "Design Parameters" in this data sheet. During the first quarter cycle, a new instruction from program storage is input on signal lines I0 through I15; simultaneously, new data is fetched via the input/output bus ($\overline{IV0}$ through $\overline{IV7}$). At the end of the first quarter cycle, the new instruction is latched in the instruction register and the new I/O data is present at the input of the chip but is not, as yet, latched by the IV latches.

In the second quarter cycle, the I/O data stabilizes and preliminary processing is completed; at the end of this quarter, the IV latches are closed and final processing can be accomplished. During the third quarter cycle, the address for the next instruction is output to the I/O (IV) bus, control signals are generated, and I/O data is setup for the output

phase. During the fourth quarter cycle, a master clock signal (MCLK) generated by the 8X300 is used to latch valid address or data into peripheral devices connected to the IV bus; MCLK is also used to synchronize any external logic with timing circuits of the 8X300. To summarize the action, the first half of the instruction cycle deals primarily with input functions and the second half is mostly concerned with output functions.
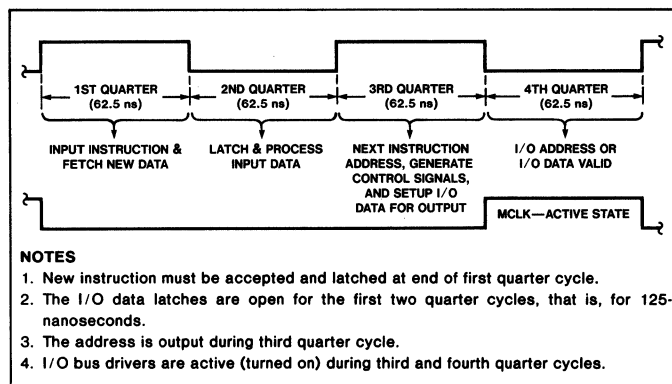

NOTES
1. New instruction must be accepted and latched at end of first quarter cycle.
2. The I/O data latches are open for the first two quarter cycles, that is, for 125-nanoseconds.
3. The address is output during third quarter cycle.
4. I/O bus drivers are active (turned on) during third and fourth quarter cycles.

Figure 3. Instruction Cycle and MCLK with: Crystal = 8MHz and Cycle Time = 250 ns

INSTRUCTION SET
General Format and Basic Operations
The 16-bit instruction word (I0 through I5) from program storage is input to the instruction register (Figure 1) and is subsequently decoded to implement the events to occur during the current instruction cycle. The instruction word is formatted as follows:
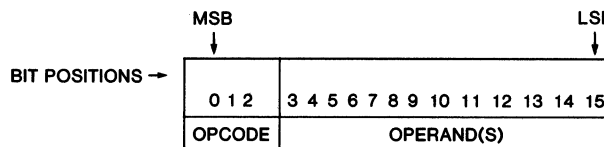
Rather than discrete instructions, the three operation code (OP CODE) bits specify eight instruction classes. Each instruction class is subject to a number of powerful variations; these variations are specified by the thirteen operand bits. General areas of control for the eight instruction classes are:

- Arithmetic and Logic Operations (ADD, AND, AND XOR)
- Movement of Data and Constants (MOVE and XMIT)
- Branch or Test (JMP, NZT, and XEC)

Basic operations for each of the eight instruction classes are as follows; a summary of the instruction set is provided in Table 1.

MOVE—data in source register or I/O-bus input is moved to destination register or I/O-bus output. Data can be shifted any number of places and/or masked to any length.

ADD—data in source register or I/O-but input is added to content of AUX (R0) register and the result is placed in the destination register or I/O-bus output. Data can be shifted and/or masked, as required.

Table 1.   Summary of 8X300 Instruction Set

INSTRUC CLASS	OPCODE	FORMATS	DESCRIPTION	I/O CONT SIG	STATE OF CONTROL SIGNAL DURING INSTRUCTION CYCLE	
					INPUT PHASE (INSTRUCTION INPUT & DATA PROCESSING)	OUTPUT PHASE (ADDRESS & I/O BUS)
MOVE	0	**F1: Register to Register** 0 1 2 / 3 4 5 6 7 / 8 9 10 / 11 12 13 14 15 OPCODE / S / R / D Invalid values of "S": 07₈, 17₈, 20₈-37₈ Invalid values of "D": 10₈, 20₈-37₈	(S) → D Move content of internal register specified by S-field to internal register specified by D-field. Prior to the "MOVE" operation, right-rotate contents of internal source register by octal value (0 through 7) defined by the R-field.	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L X X	H if "D" = 07₈, 17₈ L H if "D" = 17₈ L if "D" = 07₈
		F2: I/O Bus to Register 0 1 2 / 3 4 5 6 7 / 8 9 10 / 11 12 13 14 15 OPCODE / S / L / D Valid values of "S": 20₈-37₈ Invalid values of "D": 10₈, 20₈-37₈	Move right-rotated I/O bus (source) data specified by the S-field to internal register specified by the D-field. The L-field specifies the length of source data starting from the LSB-position and, if less than 8-bits, the remaining bits are filled with zeroes.	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if "S" = 20₈-27₈ H if "S" = 30₈-37₈	H if "D" = 07₈, 17₈ L H if "D" = 17₈ L if "D" = 07₈
		F2: Register to I/O Bus 0 1 2 3 / 4 5 6 7 / 8 9 10 / 11 12 13 14 15 OPCODE / S / L / D Invalid values of "S": 07₈, 17₈, 20₈, 37₈ Valid values of "D": 20₈-37₈	Move contents of internal register specified by the S-field to the I/O latches. Before outputting on I/O bus, data is shifted as specified by the least significant octal digit of the D-field and the bits specified by the L-field are merged with the latched I/O data.	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if "D" = 20₈-27₈ H if "D" = 30₈-37₈	L H L if "D" = 20₈-27₈ H if "D" = 30₈-37₈
		F2: I/O Bus to I/O Bus 0 1 2 / 3 4 5 6 7 / 8 9 10 / 11 12 13 14 15 OPCODE / S / L / D Valid values of "S": 20₈-37₈ Valid values of "D": 20₈-37₈	Move right rotated I/O-bus (source) data specified by the S-field to the I/O latches. Before outputting on I/O bus, shift data as specified by the D-field; then merge source and latched I/O data as specified by the L (length) field.	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if "D" = 20₈-27₈ H if "D" =30₈-37₈	L H L if "D" = 20₈-27₈ H if "D" = 30₈-37₈

Table 1. Summary of 8X300 Instruction Set (Continued)

INSTRUC CLASS	OPCODE	FORMATS	DESCRIPTION	I/O CONT SIG	STATE OF CONTROL SIGNAL DURING INSTRUCTION CYCLE	
					INPUT PHASE (INSTRUCTION INPUT & DATA PROCESSING)	OUTPUT PHASE (ADDRESS & I/O BUS)
ADD	1	Same as MOVE instruction class	(S) plus (AUX) → D. Same as MOVE instruction class except that contents of AUX (R0) register are ADDed to the source data. If there is a "carry" from MSB, then OVF (overflow) = 1, otherwise OVF = 0.	Same as MOVE instruction class		
AND	2	Same as MOVE instruction class	(S) ∧ (AUX) → D. Same as MOVE instruction class except that contents of AUX (R0) register are ANDed with source data.	Same as MOVE instruction class.		
XOR	3	Same as MOVE instruction class	(S) ⊕ (AUX) → D. Same as MOVE instruction class except that contents of AUX (R0) register are exclusively ORed with source data.	Same as MOVE instruction class.		
XEC	4	**F3: Register Immediate** 	0 1 2	3 4 5 6 7	8 9 10 11 12 13 14 15
OPCODE	S	J | Invalid values of "S": 07_8, 17_8, 20_8-37_8 Valid values of "J": 000_8-377_8	Execute instruction at current page address offset by J (literal) + (S). Return to normal instruction flow unless a branch is encountered. Execute instruction at an address determined by replacing the low-order 8-bits of the Program Counter with the following derived sum: • Value of literal (J-field) plus • Contents of internal register specified by S-field The PC is not incremented and the overflow status (OVF) is not changed.	SC = WC = $\overline{LB}$ =	L L X	L L X
		F4: I/O Bus Immediate 	0 1 2	3 4 5 6 7	8 9 10	11 12 13 14 15
OPCODE	S	L	J | Valid values of "S": 20_8-37_8 Valid values of "J": 00_8-37_8	Execute instruction at an address determined by replacing the low-order 5-bits of Program Counter with the following derived sum: • 5-bit value of literal (J-field) plus • Value of rotated source data specified by S-field (The L-field specifies the length of source data starting from the LSB-position and, if less than 8-bits, the remaining bits are filled with zeros; the Program Counter is not incremented and the overflow status (OVF) is not changed.)	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if "S" = 20_8-27_8 H if "S" = 30_8-37_8	L L X X
NZT	5	**F3: Register Immediate** 	0 1 2	3 4 5 6 7	8 9 10 11 12 13 14 15
OPCODE	S	J | Invalid values of "S": 07_8, 17_8, 20_8-37_8 Valid values of "J": 000_8-377_8	If data specified by the S-field is not equal to zero, jump to current page address offset by value of J-field; otherwise, increment the Program Counter. If contents of internal register specified by S-field is **non-zero**, transfer to address determined by replacing the low-order 8-bits of Program Counter with "J", otherwise, increment PC.	SC = WC = $\overline{LB}$ =	L L X	L L X
		F4: I/O Bus Immediate 	0 1 2	3 4 5 6 7	8 9 10	11 12 13 14 15
OPCODE	S	L	J | Valid values of "S": 20_8-37_8 Valid values of "J": 00_8-37_8	If right-rotated I/O bus data is **non-zero**, transfer to address determined by replacing low-order 5-bits of Program Counter with "J", otherwise, increment PC. (The L-field specifies the length of source I/O data starting from the LSB-position and, if less than 8-bits, the remaining bits are filled with zeroes.)	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if "S" = 20_8-27_8 H if "S" = 30_8-37_8	L L X X
XMIT	6	**F3: Register Immediate** 	0 1 2	3 4 5 6 7	8 9 10 11 12 13 14 15
OPCODE	D	J | Invalid values of "D": 10_8, 20_8-37_8 Valid values of "J": 000_8-377_8	Transmit J → D. Transmit and store 8-bit binary pattern in J-field to internal register specified by D-field.	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L X X	H if D = 07_8 or 17_8 L H if D = 17_8 L if D = 07_8
		F4: I/O Bus Immediate 	0 1 2	3 4 5 6 7	8 9 10	11 12 13 14 15
OPCODE	D	L	J | Valid values of "D": 20_8-37_8 Valid values of "J": 00_8-37_8	Transmit binary pattern in J-field to I/O bus. Before putting data on I/O bus, shift literal value "J" as specified by the D-field and merge bits specified by the L-field with existing I/O bus data. If the L-field specifies more than 5-bits starting from the LSB-position, all remaining bits are set to zero.	SC = WC = $\overline{LB}$ = $\overline{LB}$ =	L L L if D = 20_8-27_8 H if D = 30_8-37_8	L H L if D = 20_8-27_8 H is D = 30_8-37_8
JMP	7	**F5: Address Immediate** 	0 1 2	3 4 5 6 7 8 9 10 11 12 13 14 15
OPCODE	A	 Valid values of A: 00000_8-17777_8	Jump to address in program storage specified by A-field; this address is loaded into the Address Register and the Program Counter.	SC = WC = $\overline{LB}$ =	L L X	L L X

NOTES
* $\overline{RB}$ is complement of $\overline{LB}$, X = Undefined

AND—data in source register or I/O-bus input is ANDed with content of AUX (R0) register and the result is placed in the destination register or I/O-bus output. Data can be shifted and/or masked, as required.

XOR—data in source register or I/O-bus input is exclusively ORed with contents of AUX (R0) register and the result is placed in the destination register or I/O-bus output. Data can be shifted and/or masked, as required.

XMIT—immediate data field of instruction word replaces data in destination register or I/O-bus output.

XEC—executes instruction at the program address which is formed by replacing the least significant bits of the last address with the sum of:

- Literal (J) field value of instruction plus,
- Value of data in source register or I/O-bus input.

NZT—least significant bits of program address are replaced by literal (J) field of instruction if the source register or I/O-bus is not equal to zero.

JMP—program address is replaced by address field of the instruction word.

Instruction Fields

As shown in Table 1, each instruction contains an operations code (OPCODE) field and from one-to-three operand fields. The operand fields are: Source (S), Destination (D), Rotate/Length (R/L), Literal (J), and Address (A). The OPCODE and operand fields are briefly described in the following paragraphs.

Operations Code Field: The three-bit OPCODE field specifies one of eight classes of 8X300 instructions; octal designations for this field and operands for each instruction class are shown in Table 1.

Source (S) and Destination (D) Fields: The five-bit (S) and (D) fields specify the source and destination of data for the operation defined by the OPCODE field. The AUXiliary (R0) register is an implied second operand for the ADD, AND, and XOR instructions, each of which require two source fields. That is, instructions of the form:
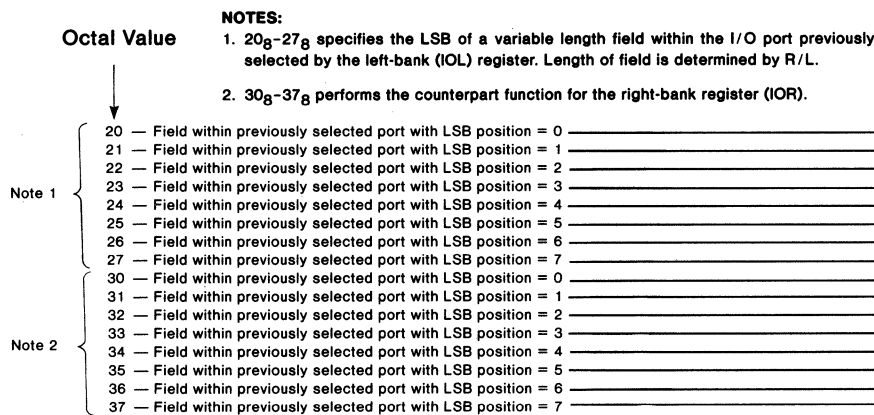
ADD X, Y

imply a third operand, say Z, located in the AUX (R0) register. Thus, the operation for the preceding expression is actually (X + Z), with the result stored in Y. The (S) and/or (D) fields can specify an internal 8X300 register or any one-to-eight bit I/O field; octal values for these registers and Source/Destination field assignments are provided in Table 2.

Table 2. Octal Addresses of 8X300 Registers and Address/Bit Assignments of Source/Destination Fields

| Octal Value	8X300 Register	Octal Value	8X300 Register
00	Auxiliary (R0)	10	OVF (Overflow Register)— used only as a source
01	R1	11	R11
02	R2	12	Unassigned
03	R3	13	Unassigned
04	R4	14	Unassigned
05	R5	15	Unassigned
06	R6	16	Unassigned
07	*IOL Register—Left Bank I/O Address Register; Used only as destination	17	*IOR Register—Right Bank I/O Address Register; Used only as destination

NOTE
*If IOL or IOR is specified as a source of data, the source data is all zeroes.

NOTES:
1. 20_8-27_8 specifies the LSB of a variable length field within the I/O port previously selected by the left-bank (IOL) register. Length of field is determined by R/L.

2. 30_8-37_8 performs the counterpart function for the right-bank register (IOR).

Octal Value

MSB ◄—BYTE—► LSB

| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |

Note 1
- 20 — Field within previously selected port with LSB position = 0
- 21 — Field within previously selected port with LSB position = 1
- 22 — Field within previously selected port with LSB position = 2
- 23 — Field within previously selected port with LSB position = 3
- 24 — Field within previously selected port with LSB position = 4
- 25 — Field within previously selected port with LSB position = 5
- 26 — Field within previously selected port with LSB position = 6
- 27 — Field within previously selected port with LSB position = 7

Note 2
- 30 — Field within previously selected port with LSB position = 0
- 31 — Field within previously selected port with LSB position = 1
- 32 — Field within previously selected port with LSB position = 2
- 33 — Field within previously selected port with LSB position = 3
- 34 — Field within previously selected port with LSB position = 4
- 35 — Field within previously selected port with LSB position = 5
- 36 — Field within previously selected port with LSB position = 6
- 37 — Field within previously selected port with LSB position = 7

BIPOLAR LSI DIVISION

Rotate (R) and Length (L) Field: The three-bit R/L field performs one of two functions, specifying either the field length (L) or a right-rotate (R). For a given instruction, the specified function depends upon the contents of the source (S) and destination (D) fields.

- When an internal register is specified by both the source and destination fields, the (R) field is invoked and it specifies a right-rotate of the data specified in the (S) field—see accompanying diagram. The source-register data (up to eight-bits) is right-rotated within one instruction cycle. (The right-rotate function is implemented on the bus and not in the source register.)

RIGHT-ROTATE FUNCTION
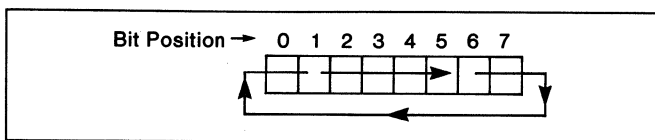
- When either or both of the source and destination fields specify a variable-length I/O data field, the (L) field specifies the length of the I/O data field—see accompanying diagram. If the source field specifies an I/O address (20_8-37_8) and the destination field specifies an internal register $(00_8-06_8, 07_8, 11_8,$ or $17_8)$, the L-field specifies the length of source data; the source data is formed by right-rotating the I/O bus data according to the source address (Table 2) and then masking result as specified by L-field. If length is less than eight-bits, all remaining bits are set to zero prior to processing data in the ALU. If the source field specifies an internal register $(00_8,-06_8, 10_8,$ or $11_8)$ and the destination field specifies I/O bus data (20_8-37_8), the L field specifies the length of the destination data. To form the destination data, the ALU output is left-shifted according to the destination address (Table 2) and then masked to the required length—see DATA LENGTH SPECIFICATION. The destination data is merged with data in the I/O latches to finalize the I/O bus data. Hence, a one-to-eight bit destination data field can be inserted into the existing eight-bit I/O port without modifying surrounding bits. If both the source and destination fields specify I/O bus data (20_8-37_8), the L-field specifies the length of both the source and destination data.

DATA LENGTH SPECIFICATION
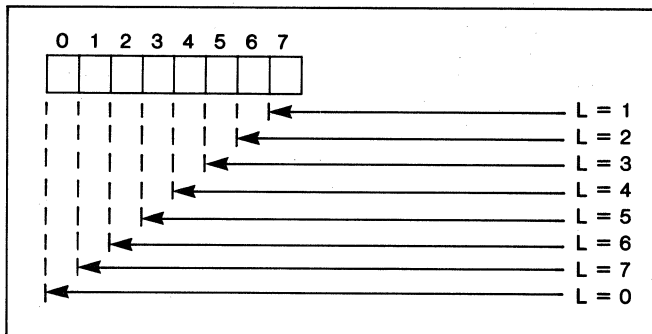
To form the source data, the I/O bus data is right-rotated according to the source address (Table 2) and then masked to the required length—see preceding DATA LENGTH SPECIFICATION. If length is less than eight-bits, all remaining bits are set to zero before processing in the ALU. To form the destination data, the ALU output is left-shifted according to the destination address (Table 2) and masked to the required length specification. The destination data is then merged into the I/O bus data that was used to obtain the source; thus, if the source and destination addresses are on the same bank, the I/O bus data written to the destination register appears unmodified, except for bits changed during the shift-and-mask operations. If the source and destination addresses refer to different banks, the destination register is changed to contain the contents of the source register in those bit positions not affected by the destination data.

J-Field: The 5-bit or 8-bit (J) field is used to load a literal value (contained in the instruction) into a register, into a variable I/O data field, or to modify the low-order bits of the Program Counter. The bit-length of the (J) field is implied by the (S) field in the XEC, NZT, and XMIT instructions, based on the following considerations.

- When the source (S) field specifies an internal register, the literal value of the J-field is an 8-bit binary number.
- When the source (S) field specifies a variable I/O data field, the literal value of the J-field is a 5-bit binary number.

A-Field: The 13-bit (A) field is an address field which allows the 8X300 to directly address up 8192 locations in Program Storage memory.

INSTRUCTION SEQUENCE CONTROL
Formation of Instruction Address
The Address Register and Program Counter are used to generate addresses for accessing an instruction from program storage. The instruction address is formed in any one of four ways:

- For all except the JMP, XEC, and a "satisfied" NZT instruction, the Program Counter is incremented by one and placed in the Address Register.
- For the JMP instruction, the 13-bit A-field contained in the JMP instruction word replaces the contents of both the Address Register and Program Counter.
- For the XEC instruction, the Address Register is loaded with the high-order bits of the Program Counter modified as follows:
  XEC using I/O Bus Data: low order 5-bits of ALU output replaces counterpart bits in Address Register.
  XEC using Data from Internal Register: low order 8-bits of ALU output replaces counterpart bits in Address Register.
  The Program Counter is not modified for either of the above conditions.
- For a "satisfied" NZT instruction, the low order 5-bits (NZT source is I/O Bus Data) or low order 8/bits (NZT source is an Internal Register) of both the Address Register and Program Counter are loaded with the literal value specified by J-field of the instruction word.

Data Addressing

The source and/or destination addresses of the data to be operated upon are specified as part of the instruction word. As shown in Table 3, source/destination addresses are specified using a five-bit address (00_8 through 37_8). When the most significant octal digit is a 0 or 1, the source and/or destination address is an internal register; if the most significant digit is a 2 or 3, an I/O bus address is indicated—2 specifying a left-bank (LB) address and 3 specifying a right-bank (RB) address. The least significant octal digit (0 through 7) indicates either a specific internal register address or positioning information for the least significant bit when specifying I/O bus data. Referring to Table 1, the AUXiliary register (00) is the implied source of the second argument for the ADD, AND, and XOR operations. IOL (destination address 07_8) and IVR (destination address 17_8) provide a means of routing address information to I/O registers. With IOL or IOR specified as the destination address, the data is placed on the I/O bus during the output phase of the instruction cycle. Simultaneously, a select command (SC) is generated to inform all I/O devices that information on the I/O bus is to be considered as an I/O address. Since IOL and IOR are not harware registers, they should never be specified as a source address.

Control outputs $\overline{LB}$ and $\overline{RB}$ are used to partition I/O bus devices into two fields of 256 addresses. With LB in the active-low state and a source address of 20_8–27_8, the left bank of I/O devices are enabled during the input phase of the instruction cycle. With $\overline{RB}$ in the active-low state and a source address of 30_8–37_8, the right bank of devices are enabled. During the output phase, $\overline{RB}$ is low if the destination address is IOR (17_8) or 30_8–37_8; $\overline{LB}$ is low if the destination address is IOL (07_8) or 20_8–27_8. Each address field

($\overline{LB}$ and $\overline{RB}$) can have a different I/O device selected; thus, two devices can be directly accessed within one instruction cycle.

Table 3. Source/Destination Addresses

Source and/or Destination Field (Octal)	Source/Destination
00	AUXiliary register (R0)
01–06	Working registers R1–R6, respectively
07	IOL Left-bank enable (Destination only)
10	Overflow status—OVF (Source only)
11	Working register R11
17	IOR Right-bank enable (Destination only)
2N (N = 0, 1, 2, 3 4, 5, 6, or 7)	If a source, I/O data is right-rotated (7 − N) bits and then masked as specified by the L-field. $\overline{LB}$ = low and $\overline{RB}$ = high generated during input phase. If a destination, I/O data is left-shift (7 − N) bits and merged (specified by L-field) with data contained in the I/O latches. $\overline{LB}$ = low and $\overline{RB}$ = high generated during output phase.
3N (N = 0, 1, 2, 3, 4, 5, 6, or 7)	If a source, I/O data is right-rotated (7 − N) bits and then masked as specified by the L-field. $\overline{LB}$ = high and $\overline{RB}$ = low generated during input phase. If a destination, I/O data is left-shifted (7 − N) bits and merged (specified by L-field) with data contained in the I/O latches. $\overline{LB}$ = high and $\overline{RB}$ = low generated during output phase.

DESIGN PARAMETERS

Hardware design of an 8X300-based system largely consists of the following operations:

- Selecting and interfacing a Program Storage device— ROM, PROM, etc. (Pins 2 through 9 and 45 through 49 for 13-bit address interface; Pins 13 through 28 for 16-bit instruction interface.)
- Selecting and interfacing Input/Output devices— RAM, Multiplexers, I/O Ports, and other eight-bit addressable I/O devices. (Pins 33 through 36 and pins 38 through 41 for eight-bit I/O interface.)
- Choosing and implementing System Clock—Capacitor-Controlled, Crystal-Controlled, or Externally-Driven. (Pins 10 and 11 for System Clock interface.)

- Selection of 5-volt power supply and off-chip series-pass transistor.
- External logic, as required, to meet the control requirements of a particular application.

All information required for easy implementation of these design requirements is provided under the following captions.

- DC Characteristics
- AC Characteristics
- Timing Considerations
- Clock Considerations
- HALT/RESET Logic
- Voltage Regulator

DC CHARACTERISTICS (Commercial Part) $4.75V \leq V_{CC} \leq 5.25V$, $0°C \leq T_A \leq 70°C$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT	COMMENTS
			Min	Typ	Max		
V_{CC}	Supply voltage		475	5.0	5.25	V	5V ± 5%; pin 37 only
V_{IH}	High level input voltage		0.6 2.0		2.0	V	X1 and X2 All other pins
V_{IL}	Low level input voltage				0.4 0.8	V	X1 and X2 All other pins
V_{OH}	High level output voltage	V_{CC} = min; I_{OH} = −3mA	2.4	3.0		V	
V_{OL}	Low level output voltage	V_{CC} = min; I_{OL} = 6mA V_{CC} = min; I_{OL} = 16mA		0.39 0.39	0.55 0.55	V	A0 through A12 All other outputs
V_{CR}	Regulator voltage	V_{CC} = 5V		3.1		V	From series-pass transistor
V_{IC}	Input clamp voltage	V_{CC} = min; I_{IN} = −10mA			−1.5	V	Crystal inputs X1 and X2 do not have internal clamp diodes.
I_{IH}	High-level input current	V_{CC} = max; V_{IH} = 0.6V V_{IH} = 4.5V	1.0	1.7 1	3.0 50	mA μA	X1 and X2 All other pins
I_{IL}	Low-level input current	V_{CC} = max; V_{IL} = 0.4V		−0.13 −0.67 −0.23	−3 −0.2 −1.6 −0.4	mA	X1 and X2 $\overline{IV0}$-$\overline{IV7}$ I0-I15 $\overline{HALT}$ and $\overline{RESET}$
I_{OS}	Short circuit output current	V_{CC} = max; V_{CR} = V_{CRH} (Note: At any time, no more than one output should be connected to ground.)	−30		−140	mA	All output pins
I_{CC}	Supply current	V_{CC} = max; V_{CR} = V_{CRH}			150	mA	
I_{REG}	Regulator control	V_{CC} = 5.0V	−14		−21	mA	
I_{CR}	Regulator current	V_{CC} = max			250	mA	

NOTES:
1. Operating temperature ranges are guaranteed after thermal equilibrium has been reached.

2. All voltages measured with respect to ground terminal.

AC CHARACTERISTICS (Commercial Part)   CONDITIONS: V_{CC} = 5V (± 5%), V_{IN} = 0V or 3V, $0°C \leq T_A \leq 70°C$
LOADING: (See test circuits)

PARAMETER (NOTE 1)		LIMITS (INSTRUCTION CYCLE TIME = 250 ns)			LIMITS (INSTRUCTION CYCLE TIME > 250 ns)			UNITS	COMMENTS
		Min	Typ	Max	Min	Typ	Max		
T_{PC}	Processor cycle time	250			250			ns	
T_{CP}	X1 clock period	125			125			ns	
T_{CH}	X1 clock high time	62			62			ns	
T_{CL}	X1 clock low time	62			62		•	ns	
T_{MCH}	MCLK high delay	31	42	52	31	42	52	ns	
T_{MCL}	MCLK low delay	31	42	52	31	42	52	ns	
T_W	MCLK pulse width	55	62	69	T_{4Q}−7	T_{4Q}		ns	Note 2
T_{AS}	X1 falling edge to address stable	50	63	80	50	63	80	ns	Note 7

AC CHARACTERISTICS (Commercial Part) (Continued)

CONDITIONS: $V_{CC} = 5V$ ($\pm 5\%$), $V_{IN} = 0V$ or $3V$, $0°C \leq T_A \leq 70°C$

LOADING: (See test circuits)

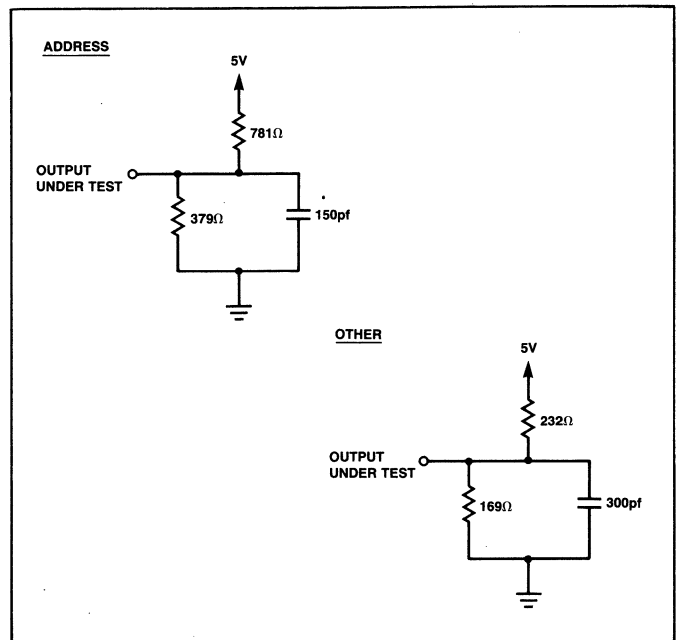| PARAMETER (NOTE 1)		LIMITS (INSTRUCTION CYCLE TIME = 250 ns)			LIMITS (INSTRUCTION CYCLE TIME > 250 ns)			UNITS	COMMENTS
		Min	Typ	Max	Min	Typ	Max		
T_{MAS}	MCLK falling edge to address stable	130	143	160	$T_{1Q}+T_{2Q}$ $+5$	$T_{1Q}+T_{2Q}$ $+18$	$T_{1Q}+T_{2Q}$ $+35$	ns	Notes 2, 3, & 7
T_{IA}	Instruction to address			170			$T_{2Q}+108$	ns	Notes 2, 3, & 8
T_{IVA}	Input data to address			105			105	ns	Notes 3 & 9
T_{IS}	Instruction set-up time (X1 rising edge)	-7			-7			ns	Note 10
T_{MIS}	MCLK falling edge to instruction stable			20			$T_{1Q}-42$	ns	Notes 2, 4, & 10
T_{IH}	Instruction hold time (X1 rising edge)	45			45			ns	Note 11
T_{MIH}	Instruction hold time) (MCLK falling edge)	60			$T_{1Q}-2$			ns	Notes 2 & 11
T_{WH}	X1 falling edge to SC/WC rising edge	40	49	58	40	49	58	ns	
T_{MWH}	MCLK falling edge to SC/WC rising edge	125	130	135	$T_{1Q}+T_{2Q}$	$T_{1Q}+T_{2Q}$ $+5$	$T_{1Q}+T_{2Q}$ $+10$	ns ns	Note 2
T_{WL}	X1 falling edge to SC/WC falling edge	40	49	58	40	49	58	ns	
T_{MWL}	MCLK falling edge to SC/WC falling edge	5	7	15	5	7	15	ns	
T_{IBS}	X1 falling edge to $\overline{LB}/\overline{RB}$ (Input phase)	48	60	70	48	60	70	ns	
T_{MIBS}	MCLK falling edge to $\overline{LB}/\overline{RB}$ (Input phase)	7	17	25	7	17	25	ns	
T_{IIBS}	Instruction to $\overline{LB}/\overline{RB}$ (Input phase)		27	35		27	35	ns	
T_{OBS}	X1 falling edge to $\overline{LB}/\overline{RB}$ (Output phase)	48	60	70	48	60	70	ns	
T_{MOBS}	MCLK falling edge to $\overline{LB}/\overline{RB}$ (Output phase)	132	137	147	$T_{1Q}+T_{2Q}$ $+7$	$T_{1Q}+T_{2Q}$ $+12$	$T_{1Q}+T_{2Q}$ $+22$	ns	Note 2
T_{IDS}	Input data set-up time (X1 falling edge)	25	16		25	16		ns	
T_{MIDS}	MCLK falling edge to input data stable		65	55		$T_{1Q}+T_{2Q}$ -60	$T_{1Q}+T_{2Q}$ -70	ns	Notes 2 & 5
T_{IDH}	Input data hold time (X1 falling edge)	40	30		40	30		ns	
T_{MDIH}	Input data hold time (MCLK falling edge)	125	112		$T_{1Q}+T_{2Q}$	$T_{1Q}+T_{2Q}$ -13		ns	Note 2
T_{ODH}	Output data hold time (X1 falling edge)	55	65	75	55	65	75	ns	
T_{MODH}	Output data hold time (MCLK falling edge)	11	20	25	11	20	25	ns	
T_{ODS}	Output data stable (X1 falling edge)	74	84	94	74	84	94	ns	Notes 12, 14, & 15
T_{MODS}	Output data stable (MCLK falling edge)	150	160	170	$T_{1Q}+T_{2Q}$ $+25$	$T_{1Q}+T_{2Q}$ $+35$	$T_{1Q}+T_{2Q}$ $+45$	ns	Notes 2, 12, 14, & 15

AC CHARACTERISTICS (Commercial Part) (Continued)

CONDITIONS: V_{CC} = 5V ($\pm$5%), V_{IN} = 0V or 3V, 0°C $\leq T_A \leq$ 70°C

LOADING: (See test circuits)

PARAMETER (NOTE 1)		LIMITS (INSTRUCTION CYCLE TIME = 250 ns)			LIMITS (INSTRUCTION CYCLE TIME > 250 ns)			UNITS	COMMENTS
		Min	Typ	Max	Min	Typ	Max		
T_{DD}	Input data to output data	104	120	136	104	120	136	ns	Notes 13 & 15
T_{HS}	$\overline{HALT}$ set-up time (X1 rising edge)	0			0			ns	
T_{MHS}	MCLK falling edge to $\overline{HALT}$ falling edge			18			$T_{1Q}-44$	ns	Notes 2 & 6
T_{HH}	$\overline{HALT}$ hold time (X1 rising edge)	32			32			ns	
T_{MHH}	$\overline{HALT}$ hold time (MCLK falling edge)	50			$T_{1Q}-12$			ns	Note 2
T_{ACC}	Program storage access time			80					
T_{IO}	I/O port output enable time ($\overline{LB}/\overline{RB}$ to valid IV data input)			30					

NOTES:

1. X1 and X2 inputs are driven by an external pulse generator with an amplitude of 1.5 volts; all timing parameters are measured at this voltage level.
2. Respectively, T_{1Q}, T_{2Q}, T_{3Q}, and T_{4Q} represent time intervals for the first, second, third, and fourth quarter cycles.
3. Capacitive loading for the address bus is 150 picofarads.
4. Same as TIS but referenced to falling edge of MCLK.
5. Same as TIDS but referenced to falling edge of MCLK.
6. Same as THS but referenced to falling edge of MCLK.
7. TAS is obtained by forcing a valid instruction and an I/O bus input to occur earlier than the specified minimum set-up time; the TAS parameter then represents the earliest time that the address bus is valid.
8. TIA is obtained by forcing a valid instruction input to occur earlier than the minimum set-up time.
9. TIVA is obtained by forcing a valid I/O bus input to just meet the minimum set-up time.
10. TMIS represents the set-up time required by internal latches of the 8X300. In system applications, the instruction input may have to be valid before the worst-case set-up time in order for the system to respond with a valid I/O bus input that meets the I/O bus input set-up time (TIDS and TMIDS).
11. TIH represents the hold time required by internal latches of the 8X300. To generate proper LB/RB signals, the instruction must be held valid until the address bus changes.
12. TODS is obtained by forcing a valid I/O bus input to occur earlier than the I/O bus input set-up time (TIDS); this timing parameter represents the earliest time that the I/O output data can be valid.
13. TDD is obtained by forcing a valid I/O bus input to just meet the minimum I/O bus input set-up time; thus timing parameter represents the latest time that the I/O output data can be valid.
14. The minimum figure for these parameters represents the earliest time that I/O bus output drivers of the 8X300 will turn on.
15. For TIDS $\geq$ 35 ns, TODS or TMODS should be used to determine when the output data is stable.

TEST CIRCUITS

ADDRESS

5V

781Ω

OUTPUT UNDER TEST

379Ω   150pf

OTHER

5V

232Ω

OUTPUT UNDER TEST

169Ω   300pf

DC CHARACTERISTICS (Military Part)   S8X300-1 −40°C ≤ TC ≤ 100°C V$_{CC}$ = 5V ± 5%
S8X300-2 −20°C ≤ TC ≤ 100°C V$_{CC}$ = 5V ± 10%

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V$_{IH}$	High level input voltage X1, X2 All others		0.6 2.0			V V
V$_{IL}$	Low level input voltage X1, X2 All others				0.4 0.8	V V
V$_{IC}$	Input clamp voltage (Notes 1 & 5)	V$_{CC}$ = min I$_I$ = −10mA			−1.5	V
I$_{IH}$	High level input current X1, X2 All others	V$_{CC}$ = max V$_{IH}$ = 0.6V V$_{CC}$ = max V$_{IH}$ = 4.5V			3.0 0.05	mA
I$_{IL}$	Low level input current X1, X2	V$_{CC}$ = max V$_{IL}$ = 0.4V			−3.0	mA
	$\overline{IV0}$–$\overline{IV7}$	V$_{CC}$ = max V$_{IL}$ = 0.4V			−0.3	mA
	I0–I15	V$_{CC}$ = max V$_{IL}$ = 0.4V			−1.6	mA
	$\overline{HALT}$, $\overline{RESET}$	V$_{CC}$ = max V$_{IL}$ = 0.4V			−0.4	mA
V$_{OL}$	Low level output voltage A0–A12 All others	V$_{CC}$ = min I$_L$ = 4.25mA V$_{CC}$ = min I$_{OL}$ = 16mA			0.55 0.55	V V
V$_{OH}$	High level output voltage	V$_{CC}$ = min I$_{OH}$ = −3mA	2.4			V
I$_{OS}$	Short circuit output current (Note 2)	V$_{CC}$ = max	−30		−140	mA
I$_{CC}$	Supply current (Note 4)	V$_{CC}$ = max			160	mA
I$_{REG}$	Regulator control	V$_{CC}$ = 5.0V	−14		−21	mA
I$_{CR}$	Regulator current	V$_{CC}$ = max			285	mA
I$_{CR}$	Regulator current	TC ≥ 25°C V$_{CC}$ = max			330	mA
V$_{CR}$	Regulator voltage	TC < 25°C (Note 3)		3.1		V

NOTES:
1. Crystal inputs X1 and X2 do not have clamp diodes.
2. Only one output may be grounded at a time.
3. From series-passed transistor under the following conditions:
   VCC = Max, HALT = RESET = ADDRESS = IVX = 0.0V, all other pins open.
4. Pin 37 only.

5. Test each input one at a time.
6. All voltages are with respect to ground terminal.
7. The operating temperature ranges are guaranteed after thermal equilibrium has been reached.
8. Storage temperature −65°C to +150°C.

AC CHARACTERISTICS (Military Part)   CONDITIONS: S8X300-1—V_{CC} = 5V ($\pm$5%) -40°C $\leq$ T_C $\leq$ 100°C
S8X300-2—V_{CC} = 5V ($\pm$10%) -20°C $\leq$ T_C $\leq$ 100°C

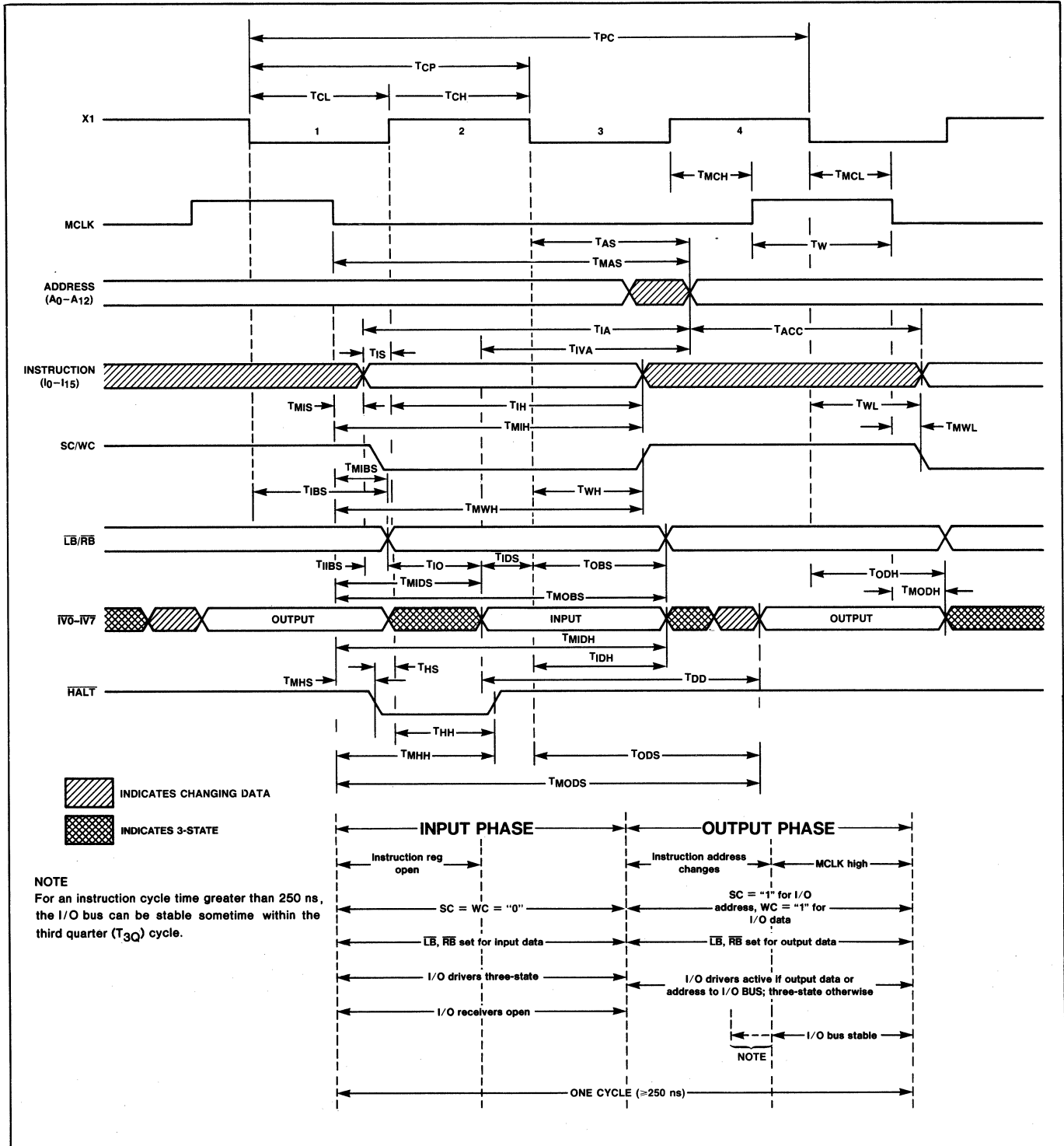| PARAMETER		TEST CONDITIONS (NOTES 1 & 2)	LIMITS			UNIT
			Min	Typ	Max	
Clock:						
T_{PC}	Processor cycle time		300			ns
T_{CP}	X1 clock period		150			ns
T_{CH}	X1 clock high time		62			ns
T_{CL}	X1 clock low time		62			ns
Controls:						
T_{HS}	$\overline{HALT}$ set-up time (X1 rising edge)		0			ns
T_{HH}	$\overline{HALT}$ hold time (X1 rising edge)		50			ns
Instructions:						
T_{AS}	X1 falling edge to address stable	CL = 100pF	35		92	ns
T_{IS}	Instruction set-up time (X1 rising edge)		0			ns
T_{IH}	Instruction hold time (X1 rising edge)		50			ns
T_{MCH}	MCLK high delay	X1 = 2.0V	20		55	ns
T_{MCL}	MCLK low delay	X1 = 2.0V	20		55	ns
T_{WH}	X1 falling edge to SC/WC rising edge				80	ns
T_{WL}	X1 falling edge to SC/WC falling edge				80	ns
T_{IIBS}	Instruction to $\overline{LB}$/$\overline{RB}$ (input phase)				52	ns
T_{IBS}	X1 falling edge to $\overline{LB}$/$\overline{RB}$ (input phase)		24			ns
T_{OBS}	X1 falling edge to $\overline{LB}$/$\overline{RB}$ (output phase)				90	ns
T_{IDS}	Input data set-up time (X1 falling edge)		36			ns
T_{IDH}	Input data hold time (X1 falling edge)		50			ns
T_{ODS}	Output data stable (X1 falling edge)				125	ns
T_{ODH}	Output data hold time (X1 falling edge)		35		85	ns
T_{ACC}	Instruction access time	Provided by worst case timing	80			ns
T_{IO}	Data I/O access time	Provided by worst case timing	40			ns

NOTES:
1. Operating temperature ranges are guaranteed after thermal equilibrium has been reached.
2. Unless otherwise noted CL = 300 pF, VIN = 3V.

TIMING CONSIDERATIONS (Commercial Part)

As shown in the "AC CHARACTERISTICS" table for this part, the minimum instruction cycle time is 25 ns, whereas, the maximum is determined by the on-chip oscillator frequency and can be any value the user chooses. With an instruction cycle time of 250 ns, the part can be characterized in terms of absolute values; these are shown in the first "LIMITS" column of the table. When the instruction cycle time is greater than 250 ns, certain parameters are cycle-time dependent; thus, these parameters are specified in terms of the four quarter cycles (T_{1Q}, T_{2Q}, T_{3Q}, and T_{4Q}) that make up one instruction cycle—see 8X300 TIMING DIAGRAM. As the time interval for each instruction cycle increases (becomes greater than 250 ns), the delay for all parameters that are cycle-time dependent is likewise increased. In some cases, these delays have a significant impact on timing relationships and other areas of systems design; subsequent paragraphs describe these timing parameters and reliable methods of calculation.

8X300 TIMING DIAGRAM

INDICATES CHANGING DATA

INDICATES 3-STATE

NOTE
For an instruction cycle time greater than 250 ns, the I/O bus can be stable sometime within the third quarter (T_{3Q}) cycle.

INPUT PHASE

Instruction reg open

SC = WC = "0"

$\overline{LB}$, $\overline{RB}$ set for input data

I/O drivers three-state

I/O receivers open

OUTPUT PHASE

Instruction address changes

MCLK high

SC = "1" for I/O address, WC = "1" for I/O data

$\overline{LB}$, $\overline{RB}$ set for output data

I/O drivers active if output data or address to I/O BUS; three-state otherwise

I/O bus stable

NOTE

ONE CYCLE (≥250 ns)

Timing parameters for the 8X300 are normally measured with reference to X1 or MCLK; those referenced to MCLK are prefaced with an "M" in the mnemonic—TMAS, TMIH, and so on. To determine the timing relationship between a particular signal, say "A" and MCLK, the user should, at all times, use the value specified in the table—DO NOT calculate the value by adding or subtracting two or more parameters that are referenced to X1. When deriving timing relationships between two signals (A to B, etc.) by adding or subtracting the parameter values, the user must consistently use the same parameter reference—MCLK or X1.

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System determinants for the instruction cycle time are:
- Propagation delays within the 8X300
- Access time of Program Storage
- Enable time of the I/O port

Normally, the instruction cycle time is constrained by one or more of the following conditions:

Condition 1—Instruction or MCLK to $\overline{LB}/\overline{RB}$ (input phase) plus I/O port access time (TIO) $\leq$ IV data set-up time (Figure 4a).

Condition 2—Program storage access time (TACC) plus instruction to $\overline{LB}/\overline{RB}$ (input phase) plus I/O port access time (TIO) plus IV data (input phase) to address $\leq$ instruction time (Figure 4b).

Condition 3—Program storage access time plus instruction to address $\leq$ instruction cycle time (Figure 4c).

a. Condition #1

① MCLK to $\overline{LB}/\overline{RB}$ (input phase) or instruction to $\overline{LB}/\overline{RB}$ (input phase).
② I/O port access (TIO).
③ IV data set-up time (referenced to MCLK).

b. Condition #2

① Program storage access time.
② MCLK to LB/RB (input phase) or instruction to LB/RB (input phase).
③ I/O port access (TIO).
④ IV data (input phase) to address.

c. Condition #3

Figure 4. Constraints of 8X300 Instruction Cycle Time

From condition #1 and with an instruction cycle time of 250 ns, the I/O port access time (TIO) can be calculated as follows:

$$TMIBS + TIO \leq TMIDS$$
transposing, $$TIO \leq TMIDS - TMIBS$$
substituting, $$TIO \leq 55ns - 25ns$$
result, $$TIO \leq 30 \text{ ns}$$

Using 30 ns for TIO, the constraint imposed by condition #1 can also be used to calculate the minimum cycle time:

$$TMIBS + TIO \leq TMIDS$$
thus, $$25ns + 30ns \leq T_{1Q} + T_{2Q} - 70$$
$$25ns + 30ns \leq \tfrac{1}{2} \text{ cycle} - 70$$ therefore, the worst-case instruction cycle time is 250 ns. With subject parameters referenced to X1, the same calculations are valid:

$$TIBS + TIO + TIDS \leq \tfrac{1}{2} \text{ cycle}$$
thus, $$70ns + 30ns + 25ns \leq \tfrac{1}{2} \text{ cycle}$$ therefore, the worst-case instruction cycle time is again 250 ns. From condition #2 and with an instruction cycle time of 250 ns, the program storage access time can be calculated:

$$TACC + TIIBS + TIO + TIVA \leq 250ns$$
transposing, $$TACC \leq 250ns - TIIBS - TIO - TIVA$$
substituting, $$TACC \leq 250ns - 35ns - 30ns - 105ns$$
thus, $$TACC \leq 80ns$$ hence, for an instruction cycle time of 250 ns, a program storage access time of 80 ns is implied. The constraint imposed by condition #3 can be used to verify the maximum program storage access time:

$$TIA + TACC \leq \text{Instruction Cycle}$$
thus, $$TACC \leq 250ns - 170ns$$
and, $$TACC \leq 80ns,$$ confirming that a program storage access time of 80 ns is satisfactory.

For an instruction cycle time of 250 ns and a program storage access time of 80 ns (Condition #2/Figure 4b), the instruction should be valid 10 ns before the falling edge of MCLK. This relationship can be derived by the following equation:

$$250ns - TMAS - TACC$$
$$= 250ns - 160ns - 80ns$$
$$= 10ns$$

It is important to note that, during the input phase, the beginning of a valid $\overline{LB}/\overline{RB}$ signal is determined by either the instruction to $\overline{LB}/\overline{RB}$ delay (TIIBS) or the delay from the falling edge of MCLK to $\overline{LB}/\overline{RB}$ (TMIBS). Assuming the instruction is valid 10 ns before the falling edge of MCLK and adding the instruction-to-LB/RB delay (TIIBS) = 30ns), the $\overline{LB}/\overline{RB}$ signal will be valid 25 ns after the falling edge of MCLK. With a fast program storage memory and with a valid instruction more than 10 ns before the falling edge of MCLK—the $\overline{LB}/\overline{RB}$ signal will, due to the TMIBS delay, still be valid 25 ns after the falling edge of MCLK. Using a worst-case instruction cycle time of 250 ns, the user cannot gain a speed advantage by selecting a memory with faster access time. Under the same conditions, a speed advantage cannot be obtained by using an I/O port with fast access time (TIO) because the address bus will be stable 80 ns (TAS) after the beginning of the third quarter cycle—no matter how early the IV data input is valid.
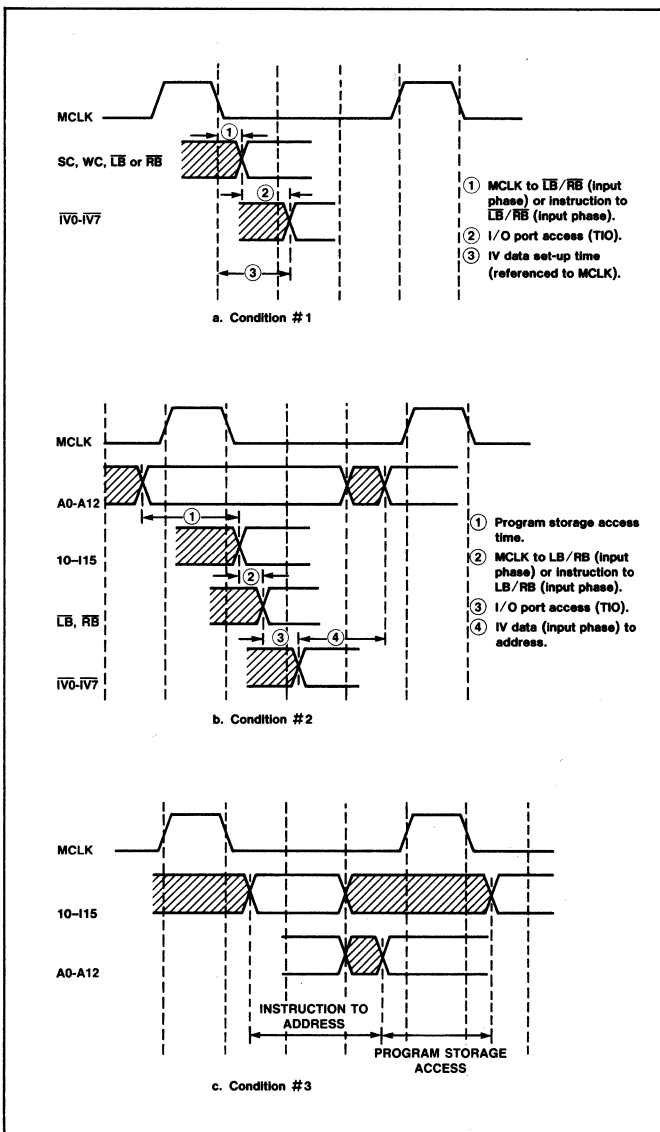
Internal Timing and Timing Relationships

All timing and timing-control signals of the 8X300 are gener-
ated by the oscillator and sequencer shown in Figure 5. The
sequencer outputs direct and control all of the timing param-
eters specified in the TIMING DIAGRAM. Observe that each
input quarter cycle bears a fixed relationship to X1 via the
propagation delay.

General and interactive timing relationships pertaining to
I/O signals of the 8X300 are shown in Figure 6. Example—in
the input phase, the switching point of the $\overline{LB}/\overline{RB}$ signal is
caused by the worst-case delay from the instruction to
$\overline{LB}/\overline{RB}$ or from the beginning of the first internal quarter
cycle to $\overline{LB}/\overline{RB}$; the two arrows pointing to the $\overline{LB}/\overline{RB}$ tran-
sition indicate this "either/or" dependency. This information
coupled with tabular values and the TIMING DIAGRAM pro-
vides the user with the wherewithal to calculate any and all
system timing parameters.

CLOCK CONSIDERATIONS

The on-chip oscillator and timing-generation circuits of the
8X300 can be controlled by any one of the following
methods:
Capacitor: if timing is not critical
Crystal: if precise timing is required
External Drive: if application requires that the 8X300 be
synchronized with system clock

Capacitor Timing: A non-polarized ceramic or mica capaci-
tor with a working voltage equal to or greater than 25-volts is
recommended. The lead lengths of capacitor should be ap-
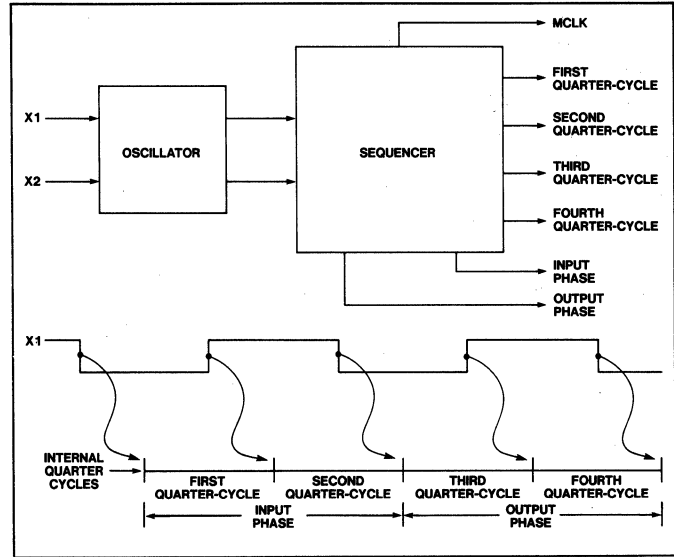proximately the same and as short as possible; also, the

Figure 5. Timing and Timing Control Signals of the 8X300

timing circuits should not be in close proximity to external
sources of noise. For various capacitor (C_X) values, the
cycle time can be approximated as:

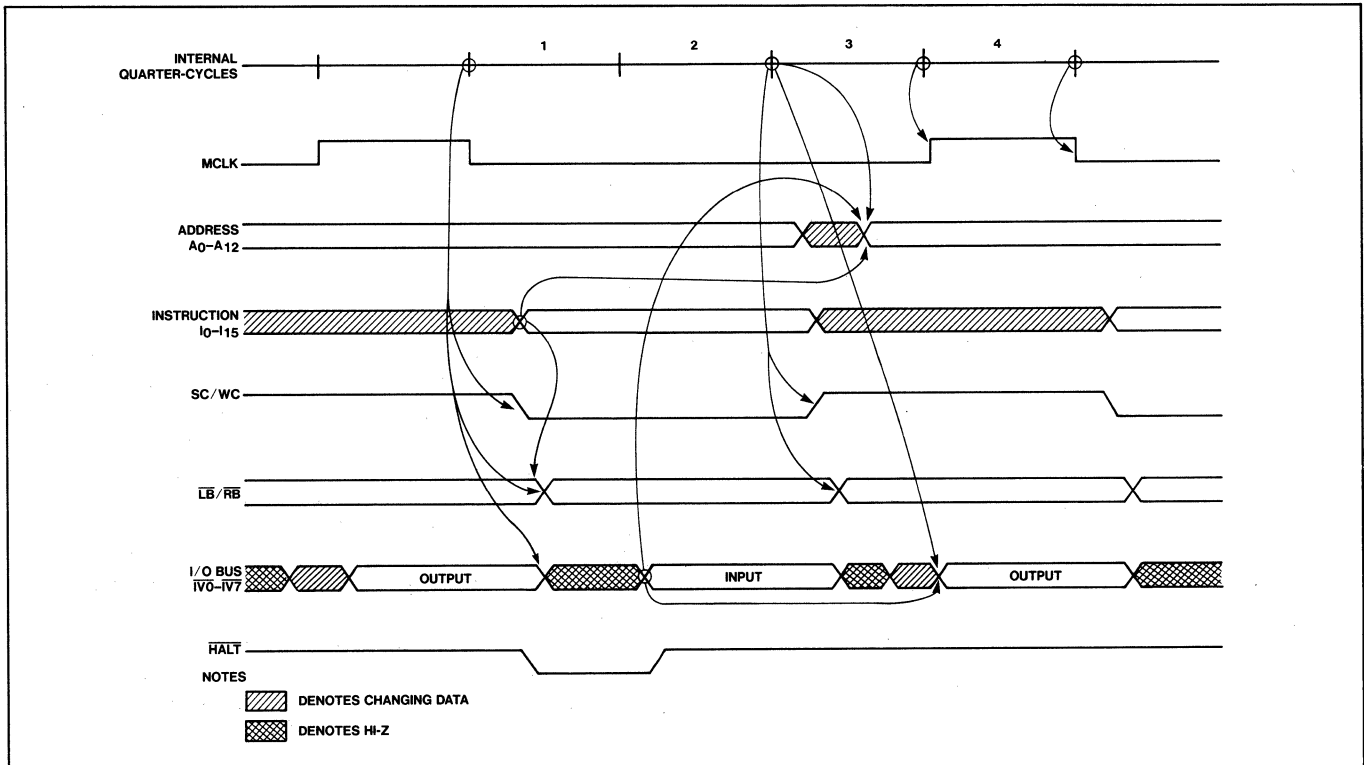| C_X (in pF)	APPROXIMATE CYCLE TIME
100	300 ns
200	500 ns
500	1.1 μs
1000	2.0 μs

Figure 6. Timing Relationships of 8X300 I/O Signals

Crystal Timing: When a crystal is used, the on-chip oscillator operates at the resonant frequency (f_O) of the crystal; the series-resonant quartz crystal connects to the 8X300 via pins 10 (X1) and 11 (X2). The lead lengths of the crystal should be approximately equal and as short as possible; also, the timing circuits should not be in close proximity to external sources of noise. The crystal should be hermetically sealed (HC type can) and have the following electrical characteristics:
Type: Fundamental mode, series resonant
Impedance at Fundamental: 35-ohms maximum
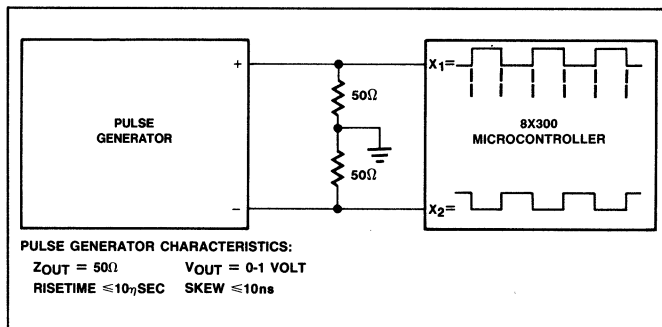**Impedance at Harmonics and Spurs:** 50-ohms minimum

The resonant frequency (f_O) of the crystal is related to the desired cycle time (T) by the equation $f_O = 2/T$; for a cycle time of 250 ns, $f_O = 8$MHz.

Using an External Clock: The 8X300 can be synchronized with an external clock by simply connecting appropriate drive circuits to the X1/X2 inputs. Figure 7 shows how the on-chip oscillator can be driven from the complementary outputs of a pulse generator. In applications where the microcontroller must be driven from a master clock, the X1/X2 lines can be interfaced to TTL logic as shown in Figure 8.
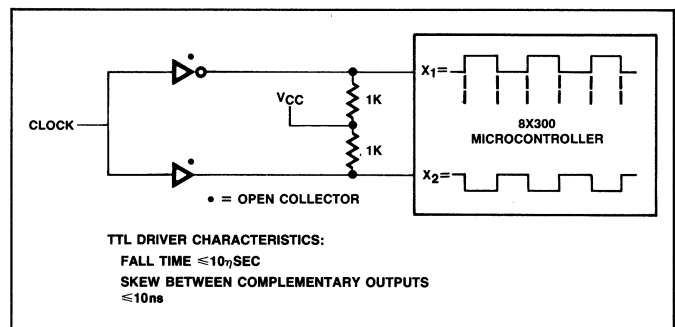

Figure 7. Clocking with a Pulse Generator

Figure 8. Clocking with TTL

RESET Logic
The $\overline{\text{RESET}}$ line (pin 43) can be driven from a high (inactive) state to a low (active) state at any time with respect to the system clock, that is, the reset function is asynchronous. To ensure proper operation, the $\overline{\text{RESET}}$ line should be held low (active) for one full instruction time. When the line is driven from a high state to an active-low state, several events occur—the precise instant of occurrence is basically a function of the propagation delay for that particular event. As shown in the acompanying $\overline{\text{RESET}}$ timing diagram, these events are:

- **The Program Counter and Address Register are set to an all-zero configuration and remain in that state as long as the $\overline{\text{RESET}}$ line is low. Other than PC and AR, reset does not affect other internal registers.**
- **The input/output (IV) bus goes three-state and remains in that mode as long as the $\overline{\text{RESET}}$ line is low.**
- **The Select Command and Write Command signals are driven low and remain inactive as long as the $\overline{\text{RESET}}$ line is low.**
- **The Left Bank/Right Bank signals are undefined for the period in which the $\overline{\text{RESET}}$ line is low.**
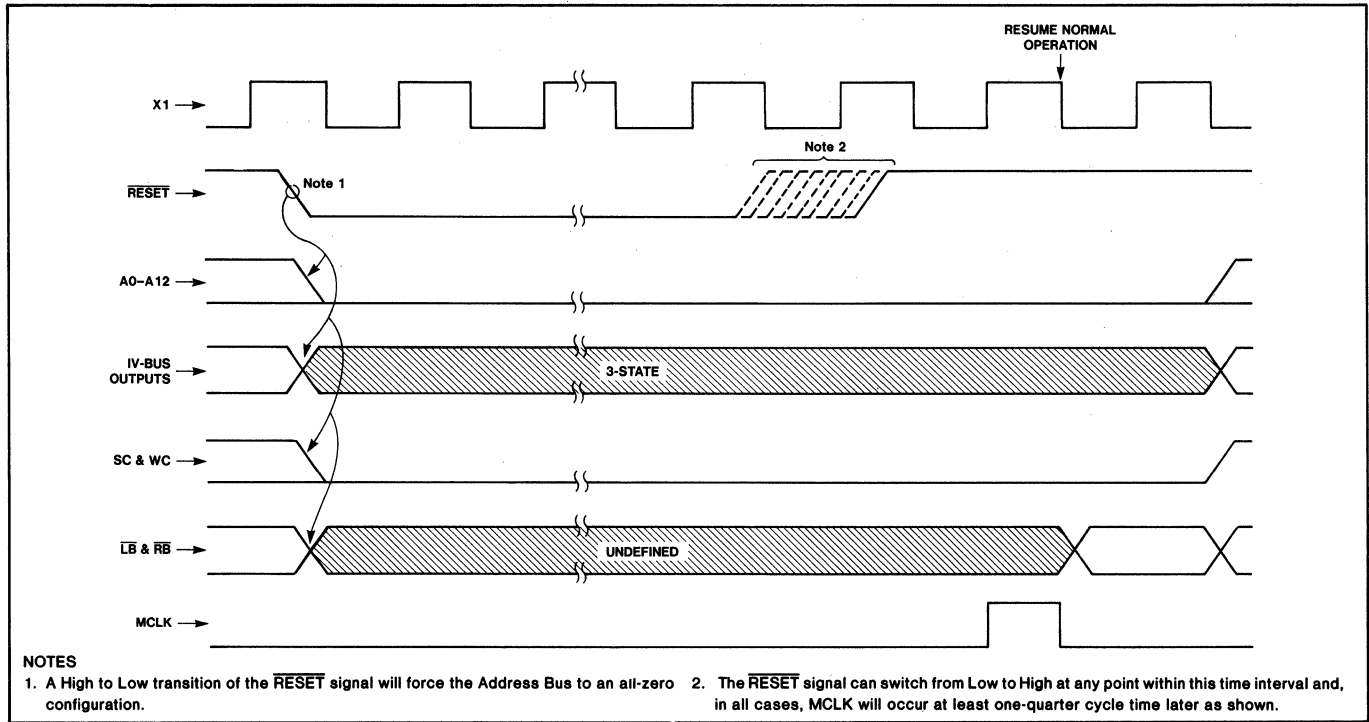
During the time $\overline{\text{RESET}}$ is active-low, MCLK is inhibited; moreover, if the $\overline{\text{RESET}}$ line is driven low during the last two

quarter cycles, MCLK can be shortened for that particular machine cycle. When $\overline{\text{RESET}}$ line is driven high (inactive)—one-quarter to one full instruction cycle later—MCLK appears just before normal operation is resumed. The $\overline{\text{RESET}}$/MCLK relationship is clearly shown by "B" in the timing diagram. As long as the $\overline{\text{RESET}}$ line is active-low, the $\overline{\text{HALT}}$ signal (described next) is not sampled by internal logic of the 8X300.

HALT Logic
The $\overline{\text{HALT}}$ signal is sampled via internal chip logic at the end of the first internal quarter of each instruction cycle. If, when sampled, the HALT signal is active-low, a halt is immediately executed and the current instruction cycle is terminated; however, the halt cycle does not inhibit MCLK nor does it affect any internal registers of the 8X300. As long as the $\overline{\text{HALT}}$ line is active-low, the SC and WC lines are low (inactive) and the input/output (IV) bus remains in the three-state mode of operation. The halt cycle continues until, when again sampled, the $\overline{\text{HALT}}$ line is found to be high; at this time, normal operation is resumed. Timing for the halt signal is shown in the accompanying diagram.

RESET TIMING DIAGRAM

NOTES
1. A High to Low transition of the $\overline{\text{RESET}}$ signal will force the Address Bus to an all-zero configuration.
2. The $\overline{\text{RESET}}$ signal can switch from Low to High at any point within this time interval and, in all cases, MCLK will occur at least one-quarter cycle time later as shown.

HALT TIMING DIAGRAM

NOTES
1. The $\overline{\text{HALT}}$ signal can switch from High to Low at any time during this interval.

2. The $\overline{\text{HALT}}$ signal can switch from Low to High at any time during this interval.

Timing Descriptions:
T_{HS}—set-up time from $\overline{\text{HALT}}$ to X1 (independent of instruction cycle time)

T_{HH}—hold time from X1 to $\overline{\text{HALT}}$ (independent of instruction cycle time)

T_{MHS}—set-up time from MCLK to $\overline{\text{HALT}}$ (dependent upon instruction cycle time)

T_{MHH}—hold time from MCLK to $\overline{\text{HALT}}$ (dependent upon instruction cycle time)

VOLTAGE REGULATOR

All internal logic of the 8X300 is powered by an on-chip voltage regulator that requires an external series-pass transistor. Electrical specifications for the off-chip power transistor and a typical hook-up are shown in the accompanying diagram. To minimize lead inductance, the transistor should be as close as possible to the 8X300 package and the emitter should be ac-grounded via a 0.1-microfarad ceramic capacitor.

PARAMETER	CONDITIONS	LIMITS
h_{fe}	V_{CE} = 2V; $100mA < I_C < 500mA$	>50
BE_{ON}	V_{CE} = 5V; I_C = 500mA	<1V
V_{CESAT}	I_C = 500mA; I_B = 50mA	<0.5V
BV_{CEO}		>15V
f_t		>30MHz

NOTE:
Typical approved parts—2N5320, 2N5337

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