SIGNETICS
LINEAR

PHASE
LOCKED
LOOPS
APPLICATIONS
BOOK

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SECTION 1

INTRODUCTION

PHASE LOCKED LOOP TERMINOLOGY

INTRODUCTION

Phase Locked Loops (PLLs) are a new class of monolithic circuits developed by Signetics, but they are based on frequency feedback technology which dates back 40 years.

A phase locked loop is basically an electronic servo loop consisting of a phase detector, a low pass filter and a voltage controlled oscillator. Its controlled oscillator phase makes it capable of locking or synchronizing with an incoming signal. If the phase changes, indicating the incoming frequency is changing, the phase detector output voltage increases or decreases just enough to keep the oscillator frequency the same as the incoming frequency, preserving the locked condition. Thus, the average voltage applied to the controlled oscillator is a function of the frequency of the incoming signal. In fact, the low pass filter voltage *is* the demodulated output when the incoming signal is frequency modulated (provided the controlled oscillator has a linear voltage-to-frequency transfer characteristic). The synchronous reception of radio signals using PLL techniques was described (Ref. 1) in the early thirties. You may have heard of the "homodyne" receiver.

The first widespread use of phase lock, however, was in TV receivers to synchronize the horizontal and vertical sweep oscillators to the transmitted sync pulses. Lately, narrow-band phase locked receivers have proved to be of considerable benefit in tracking weak satellite signals because of their superior noise immunity. Applications such as these were implemented primarily in discrete component form and involved considerable complexity even after the advent of transistors. This complexity made PLL techniques impractical or uneconomical in the majority of systems.

The development of complete, single-chip phase locked loops has changed this situation considerably. Now, a single packaged device with a few external components will offer the user all the benefits of phase locked loop operation, including independent center frequency and bandwidth adjustment, high noise immunity, high selectivity, high frequency operation and center frequency tuning by means of a single external component.

Signetics makes three basic classes of single-chip PLL circuits: the general purpose PLL, the PLL with an added multiplier and the PLL tone decoder.

The 560B, 562B and 565 are general purpose phase locked loops containing an oscillator, phase detector and amplifier. When locked to an incoming signal, they provide two outputs: a voltage proportional to the frequency of the incoming signal (FM output) and the square wave oscillator output which, during lock, is equal to the incoming frequency. All general purpose devices are optimized to provide a linear frequency-to-voltage transfer characteristic.

The 561B contains a complete PLL as those above, plus the additional multiplier or quadrature phase detector required for AM demodulation. In addition to the standard FM and oscillator outputs, it also provides an output voltage which is proportional to the amplitude of the incoming signal (AM output). The 561B is optimized for highly linear FM and AM demodulation.

The 567 is a special purpose phase locked loop intended solely for use as a tone decoder. It contains a complete PLL including oscillator, phase detector and amplifier as well as a quadrature phase detector or multiplier. If the signal amplitude at the locked frequency is above a minimal value, the driver amplifier turns on, driving a load as much as 200mA. It, thus, gives an output whenever an in-band tone is present. The 567 is optimized for both center frequency and bandwidth stability.

The 566 is not a phase locked loop, but a precision voltage-controllable waveform generator derived from the oscillator of the 565 general purpose loop. Because of its similarity to the 565 and because it lends itself well to use in, and in conjunction with, phase locked loops, it has been included in this section.

Table 8—1 summarizes the characteristics of Signetics phase locked loop products.

USER'S QUICK-LOOK GUIDE TO SIGNETICS PLLs

	Upper Frequency (MHz)	Maximum Lock Range (% f_o)	FM Distortion	Output Swing ±5% Deviation (volts p.p.)	Center Frequency Stability (ppm/°C)	Frequency Drift with Supply Voltage (%/volt)	Input Resistance	AM Output Available	Typical Supply Current (mA)	Supply Voltage Range (volts)
NE560	30	40%	.3%	1	±600	.3	2K**	No	9	+15 to +26
NE561	30	40%	.3%	1	±600	.3	2K**	Yes	10	+15 to +26
NE562	30	40%	.5%	1	±600	.3	2K**	No	12	+15 to +30
NE565	.5	120%	.2%	.15	±200	.16	5K	No	8	± 5 to ±12
SE565	.5	120%	.2%	.15	±100	.08	5K	No	8	± 5 to ±12
NE567	.5	14%	5%*	.20	35±60	.7	20K**	Yes*	7	+ 4.5 to +9
SE567	.5	14%	5%*	.20	35±60	.5	20K**	Yes*	6	+ 4.5 to +9
NE566	.5		.2%	30%/V***	±200	.16			7	+10 to +26
SE566	.5		.2%	30%/V***	±100	.08			7	+10 to +26

*   The 567 AM and FM outputs are available, but are not optimized for linear demodulation.

**   Input biased internally.

*** Figure shown is VCO gain in percent deviation per volt.

A considerable quantity of detailed specifications and publications information for these products is included in the Linear Spec. Handbook. Because many readers are likely to be unfamiliar with the terminology and operating characteristics of phase locked loops, a glossary of terms and a general explanation of PLL principles are included here with a detailed discussion of the action of the individual loop elements.

The tradeoff and setup section will assist the reader in some of the considerations involved in selecting and applying the loop products to meet system requirements. A brief summary of measurement techniques has been presented to aid the user in achieving his performance goals.

Detailed descriptions have been provided for each of the loop products. The user can supplement the suggested connection diagrams with his own schemes.

Perhaps the best way to become familiar with the many uses of phase locked loops is to actually study the various application circuits provided. These circuits have been drawn from many sources — textbooks, users, Signetics' applications engineers and the 1970 Signetics—EDN Phase Locked Loop contest. Every effort has been made to provide usable, workable circuits which may be copied directly or used as jumping-off points for other imaginative applications.

The section on interfacing will aid the user in driving different forms of logic from PLL outputs and the section on expanding loop capabilities will show how to achieve improved performance in certain difficult applications.

PHASE LOCKED LOOP TERMINOLOGY

The following is a brief glossary of terms encountered in PLL literature.

CAPTURE RANGE (2 ω_C) — Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes. The range over which the loop *can* acquire lock is termed capture range. The capture range is sometimes called the LOCK-IN RANGE. (The latter refers to how close a signal must be to the center frequency before acquisition can occur. It is thus one-half the capture range or ω_C.)

CURRENT CONTROLLED OSCILLATOR (CCO) — An oscillator similar to a VCO in which the frequency is determined by an applied current.

DAMPING FACTOR (ζ) — The standard damping constant of a second order feedback system. In the case of the PLL, it refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

FREE-RUNNING FREQUENCY (f_0, ω_0) — Also called the CENTER FREQUENCY, this is the frequency at which the loop VCO operates when not locked to an input signal. The same symbols (f_0, ω_0) used for the free-running frequency are commonly used for the general oscillator frequency. It is usually clear which is meant from the context.

LOCK RANGE (2 ω_L) — The range of input frequencies over which the loop will remain in lock. It is also called the TRACKING RANGE or HOLD-IN RANGE. (The latter refers to how far the loop frequency can be deviated from the center frequency and is one-half the lock range or ω_L.)

LOOP GAIN (K_v) — The product of the dc gains of all the loop elements, in units of $(\sec)^{-1}$.

LOOP NOISE BANDWIDTH (B_L) — A loop property related to damping and natural frequency which describes the effective bandwidth of the received signal. Noise and signal components outside this band are greatly attenuated.

LOW PASS FILTER (LPF) — A low pass filter in the loop which permits only dc and low frequency voltages to travel around the loop. It controls the capture range and the noise and out-band signal rejection characteristics.

NATURAL FREQUENCY (ω_n) — The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane. May be determined experimentally as the modulation frequency for which an underdamped loop gives the maximum output and at which phase error swing is the greatest.

PHASE DETECTOR GAIN FACTOR (K_d) — The conversion factor between the phase detector output voltage and the phase difference between input and VCO signals in volts/radian. At low input signal amplitudes, the gain is also a function of input level.

PHASE DETECTOR (PD) — A circuit which compares the input and VCO signals and produces an error voltage which is dependent upon their relative phase difference. This error signal corrects the VCO frequency during tracking. Also called PHASE COMPARATOR. A MULTIPLIER or MIXER is often used as a phase detector.

QUADRATURE PHASE DETECTOR (QPD) — A phase detector operated in quadrature (90^0 out of phase) with the loop phase detector. It is used primarily for AM demodulation and lock detection.

VCO CONVERSION GAIN (K_0) — The conversion factor between VCO frequency and control voltage in radians/ second/volt.

VOLTAGE CONTROLLED OSCILLATOR (VCO) — An oscillator whose frequency is determined by an applied control voltage.

SECTION 2

THE PHASE LOCKED LOOP PRINCIPLE

PHASE LOCKED LOOP BUILDING BLOCKS
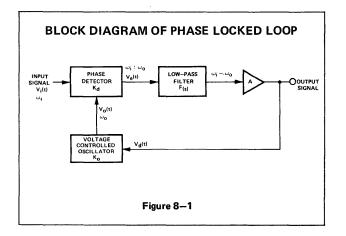
FUNCTIONAL APPLICATIONS

THE PHASE LOCKED LOOP PRINCIPLE

The phase locked loop is a feedback system comprised of a phase comparator, a low pass filter and an error amplifier in the forward signal path and a voltage-controlled oscillator (VCO) in the feedback path. The block diagram of a basic PLL system is shown in Figure 8—1. Detailed analysis of the PLL as a feedback control system has been discussed in the literature (Ref. 2). Perhaps the single most important point to realize when designing with the PLL is that it is a feedback system and, hence, is characterized mathematically by the same equations that apply to other, more conventional feedback systems. The parameters in the equations are somewhat different, however, since the feedback error signal in the phase locked system is a phase rather than a current or voltage signal, as is usually the case in conventional feedback systems.

BLOCK DIAGRAM OF PHASE LOCKED LOOP

Figure 8—1

LOOP OPERATION

A rigorous mathematical analysis of the system is quite cumbersome and will not be repeated here. However, from a qualitative point of view, the basic principle of PLL operation can be briefly explained as follows: With no signal input applied to the system, the error voltage V_d is equal to zero. The VCO operates at a set frequency ω_0, which is known as the free-running frequency. If an input signal is applied to the system, the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage $V_e(t)$ that is related to the phase and the frequency difference between the two signals. This error voltage is then filtered, amplified and applied to the control terminal of the VCO. In this manner, the control voltage $V_d(t)$ forces the VCO frequency to vary in a direction that reduces the frequency difference between f_0 and the input signal. If the input frequency ω_i is sufficiently close to ω_0, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once in lock, the VCO frequency is identical to the input signal except for a finite phase difference. This net phase difference θ_0 is necessary to generate the corrective error voltage V_d to shift the VCO frequency from its free-running value to the input signal

frequency ω_i and, thus, keep the PLL in lock. This self-correcting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can maintain lock with an input signal is defined as the "lock range" of the system. The band of frequencies over which the PLL can acquire lock with an incoming signal is known as the "capture range" of the system and is never greater than the lock range.

Another means of describing the operation of the PLL is to observe that the phase comparator is in actuality a multiplier circuit that mixes the input signal with the VCO signal. This mix produces the sum and difference frequencies $\omega_i \pm \omega_0$ shown in Figure 8—1. When the loop is in lock, the VCO duplicates the input frequency so that the difference frequency component $(\omega_i - \omega_0)$ is zero; hence, the output of the phase comparator contains a dc component. The low pass filter removes the sum frequency component $(\omega_i + \omega_0)$ but passes the dc component which is then amplified and fed back to the VCO. Notice that when the loop is in lock, the difference frequency component is always dc, so the lock range is independent of the band edge of the low pass filter.

LOCK AND CAPTURE

Consider now the case where the loop is not yet in lock. The phase comparator again mixes the input and VCO signals to produce sum and difference frequency components. Now, however, the difference component may fall outside the band edge of the low pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at its initial free-running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the low pass filter. Now some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to be transmitted through the low pass filter to the VCO. This is essentially a positive feedback mechanism which causes the VCO to snap into lock with the input signal. With this mechanism in mind, the term "capture range" can again be defined as *the frequency range centered about the VCO initial free-running frequency over which the loop can acquire lock with the input signal.* The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low pass filter together with the closed loop gain of the system. It is this signal capturing phenomenon which gives the loop its frequency selective properties.

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It is important to distinguish the "capture range" from the "lock range" which can, again, be defined as *the frequency range usually centered about the VCO initial free-running frequency over which the loop can track the input signal once lock has been achieved.*

When the loop is in lock, the difference frequency component on the output of the phase comparator (error voltage) is dc and will always be passed by the low pass filter. Thus, the lock range is limited by the range of error voltage that can be generated and the corresponding VCO frequency deviation produced. The lock range is essentially a dc parameter and is not affected by the band edge of the low pass filter.

THE CAPTURE TRANSIENT

The capture process is highly complex and does not lend itself to simple mathematical analysis. However, a qualitative description of the capture mechanism may be given as follows: Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as

$$\Delta\omega = \frac{d\theta_o}{d_t}$$

where $\Delta\omega$ is the instantaneous frequency separation between the signal and VCO frequencies and θ_o is the phase difference between the input signal and VCO signals.

If the feedback loop of the PLL was opened, say between the low pass filter and the VCO control input, then for a given condition of ω_o and ω_i the phase comparator output would be a sinusoidal beat note at a fixed frequency $\Delta\omega$. If ω_i and ω_o were sufficiently close in frequency, this beat note would appear at the filter output with negligible attenuation. Now suppose that the feedback loop is closed by connecting the low pass filter output to the VCO control terminal. The VCO frequency will be modulated by the beat note. When this happens, $\Delta\omega$ itself will become a function of time. If during this modulation process, the VCO frequency moves closer to ω_i (i.e., decreasing $\Delta\omega$), then $\frac{d\theta_o}{d_t}$ decreases and the output of the phase comparator becomes a slowly varying function of time. Similarly, if the VCO is modulated away from ω_i, $\frac{d\theta_o}{d_t}$ increases and the error voltage becomes a rapidly varying function of time. Under this condition the beat note waveform no longer looks sinusoidal; it looks like a series of aperiodic cusps, depicted schematically in Figure 8–2a. Because of its asymmetry, the beat note waveform contains a finite dc component that pushes the average value of the VCO toward ω_i, thus decreasing $\Delta\omega$. In this manner, the beat note frequency rapidly decreases toward zero, the VCO frequency drifts toward ω_i and the lock is established. When the system is in lock, $\Delta\omega$ is equal to zero and only a steady-state dc error voltage remains.

ASYNCHRONOUS ERROR BEAT FREQUENCY DURING THE CAPTURE PROCESS
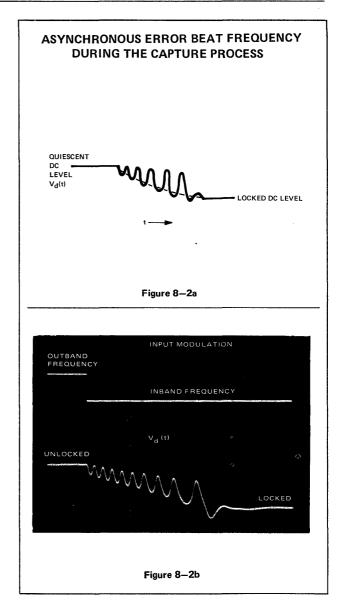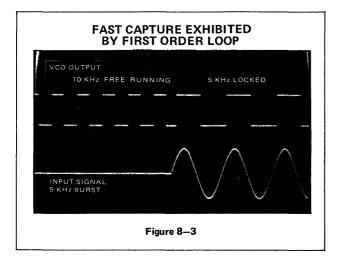

Figure 8–2a

Figure 8–2b

Figure 8–2b displays an oscillogram of the loop error voltage V_d in an actual PLL system during the capture process. Note that as lock is approached, $\Delta\omega$ is reduced, the low pass filter attenuation becomes less and the amplitude of the beat note increases.

The total time taken by the PLL to establish lock is called the pull-in time. Pull-in time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat note and the loop can lock without an oscillatory error transient.

A specific case to illustrate this is shown in Figure 8–3. The 565 PLL is shown acquiring lock within the first cycle of the input signal. The PLL was able to capture in this short time because it was operated as a first order loop (no low pass filter) and the input tone-burst frequency was within its lock and capture range.

**FAST CAPTURE EXHIBITED
BY FIRST ORDER LOOP**

VCO OUTPUT

10 KHz FREE RUNNING   5 KHz LOCKED

INPUT SIGNAL
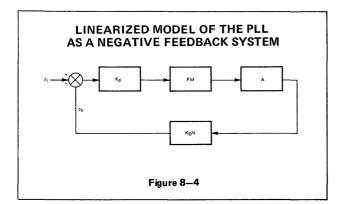5 KHz BURST

Figure 8—3

EFFECT OF THE LOW PASS FILTER

In the operation of the loop, the low pass filter serves a dual function: First, by attenuating the high frequency error components at the output of the phase comparator, it enhances the interference-rejection characteristics; second, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. The low pass filter bandwidth has the following effects on system performance:

a.) The capture process becomes slower, and the pull-in time increases.

b.) The capture range decreases.

c.) Interference-rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low pass filter.

d.) The transient response of the loop (the response of the PLL to sudden changes of the input frequency within the capture range) becomes underdamped.

The last effect also produces a practical limitation on the low pass loop filter bandwidth and roll-off characteristics from a stability standpoint. These points will be explained further in the following analysis.

**LINEARIZED MODEL OF THE PLL
AS A NEGATIVE FEEDBACK SYSTEM**

Figure 8—4

LINEAR ANALYSIS FOR LOCK CONDITION — FREQUENCY TRACKING

When the PLL is in lock, the non-linear capture transients are no longer present. Therefore, under lock condition, the PLL can often be approximated as a linear control system (see Figure 8—4) and can be analyzed using Laplace transform techniques. In this case, it is convenient to use the net phase error in the loop $(\theta_s - \theta_o)$ as the system variable. Each of the gain terms associated with the blocks can be defined as follows:

K_d = conversion gain of phase detector (volt/rad)
$F(s)$ = transfer characteristic of low pass filter
A = amplifier voltage gain
K_θ = VCO conversion gain (rad/volt-sec)

Note that, since the VCO converts a voltage to a frequency and since phase is the integral of frequency, the VCO functions as an integrator in the feedback loop.

The open loop transfer function for the PLL can be written as

$$T(s) = \frac{K_v F(s)}{s}$$

where K_v is the total loop gain, i.e., $K_v = K_o K_d A$. Using linear feedback analysis techniques, the closed loop transfer characteristics $H(s)$ can be related to the open loop performance as
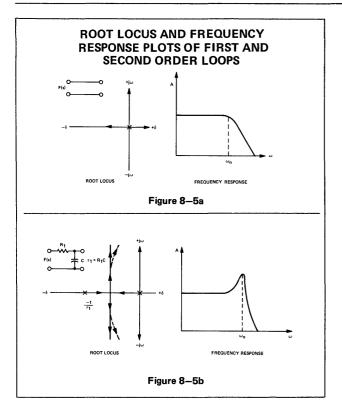
$$H(s) = \frac{T(s)}{1 + T(s)}$$

and the roots of the characteristic system polynominal can be readily determined by root-locus techniques.

From these equations, it is apparent that the transient performance and frequency response of the loop is heavily dependent upon the choice of filter and its corresponding transfer characteristic, $F(s)$.

The simplest case is that of the first order loop where $F(s) = 1$ (no filter). The closed loop transfer function then becomes

$$T(s) = \frac{K_v}{s + K_v}$$

This transfer function gives the root locus as a function of the total loop gain K_v and the corresponding frequency response shown in Figure 8—5a. The open loop pole at the origin is due to the integrating action of the VCO. Note that the frequency response is actually the amplitude of the difference frequency component versus modulating frequency when the PLL is used to track a frequency modulated input signal. Since there is no low pass filter in this case, sum frequency components are also present on the phase detector output and must be filtered outside of the loop if the difference frequency component (demodulated FM) is to be measured.

ROOT LOCUS AND FREQUENCY RESPONSE PLOTS OF FIRST AND SECOND ORDER LOOPS

ROOT LOCUS   FREQUENCY RESPONSE

Figure 8—5a

ROOT LOCUS   FREQUENCY RESPONSE

Figure 8—5b

With the addition of a single pole low pass filter $F(s)$ of the form

$$F(s) = \frac{1}{1 + \tau_1 s}$$

where $\tau_1 = R_1 C$, the PLL becomes a second order system with the root locus shown in Figure 8—5b. Here, we again have an open loop pole at the origin because of the integrating action of the VCO and another open loop pole at a position equal to $\dfrac{-1}{\tau_1}$ where τ_1 is the time constant of the low pass filter.
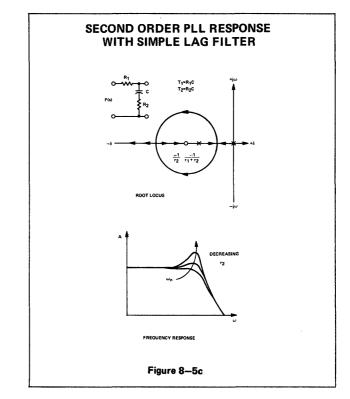
One can make the following observations from the root locus characteristics of Figure 8—5b.

   a.)   As the loop gain K_v increases for a given choice of τ_1, the imaginary part of the closed loop poles increase; thus, the natural frequency of the loop increases and the loop becomes more and more underdamped.

   b.)   If the filter time constant is increased, the real part of the closed loop poles becomes smaller and the loop damping is reduced.

As in any practical feedback system, excess shifts or non-dominant poles associated with the blocks within the PLL can cause the root loci to bend toward the right half plane as shown by the dashed line in Figure 8—5b. This is likely to happen if either the loop gain or the filter time constant is too large and may cause the loop to break into sustained oscillations.

The stability problem can be eliminated by using a lag-lead type of filter, as indicated in Figure 8—5c. This type of a filter has the transfer function

$$F(s) = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s}$$

where $\tau_2 = R_2 C$ and $\tau_1 = R_1 C$. By proper choice of R_2, this type of filter confines the root locus to the left half plane and ensures stability. The lag-lead filter gives a frequency response dependent on the damping, which can now be controlled by the proper adjustment of τ_1 and τ_2. In practice, this type of filter is important because it allows the loop to be used with a response between that of the first and second order loops and it provides an additional control over the loop transient response. If $R_2 = 0$, the loop behaves as a second order loop and if $R_2 = \infty$, the loop behaves as a first order loop due to a pole-zero cancellation. Note, however, that as first order operation is approached, the noise bandwidth increases and interference rejection decreases since the high frequency error components in the loop are now attenuated to a lesser degree.

SECOND ORDER PLL RESPONSE WITH SIMPLE LAG FILTER

ROOT LOCUS

FREQUENCY RESPONSE

Figure 8—5c

In terms of the basic gain expressions in the system, the lock range of the PLL ω_L can be shown to be numerically equal to the dc loop gain

$$2\omega_L = 4\pi f_L = 2K_v.$$

Since the capture range ω_L denotes a transient condition, it is not as readily derived as the lock range. However, an approximate expression for the capture range can be written as

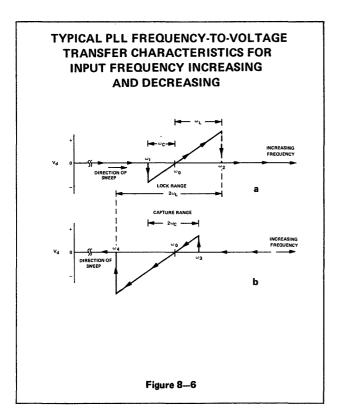$$2\omega_c = 4\pi f_c \simeq 2K_v \; F(j\omega_c)$$

where $F(j\omega_c)$ is the low pass filter amplitude response at $\omega = \omega_L$. Note that at all times the capture range is smaller than the lock range. If the simple lag filter of Figure 8—5b is used, the capture range equation can be approximated as

$$2\omega_c \simeq 2\sqrt{\frac{\omega_L}{\tau_1}} = 2\sqrt{\frac{K_v}{\tau_1}}$$

Thus, the capture range decreases as the low pass filter time constant is decreased, whereas the lock range is unaffected by the filter and is determined solely by the loop gain.

Figure 8—6 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range. The vertical scale is the corresponding loop error voltage. In Figure 8—6a, the input frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency ω_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input and causes a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of VCO gain $(1/K_o)$ and goes through zero as $\omega_i = \omega_0$. The loop tracks the input until the input frequency reaches ω_2, corresponding to the upper edge of the lock range. The PLL then loses lock and the error voltage drops to zero. If the input frequency is swept slowly back now, the cycle repeats itself, but it is inverted, as shown in Figure 8—6b. The loop recaptures the signal at ω_3 and tracks it down to ω_4. The total capture and lock ranges of the system are:

$$2\omega_c = \omega_3 - \omega_1 \text{ and } 2\omega_L = \omega_2 - \omega_4$$

**TYPICAL PLL FREQUENCY-TO-VOLTAGE
TRANSFER CHARACTERISTICS FOR
INPUT FREQUENCY INCREASING
AND DECREASING**

Figure 8—6

Note that, as indicated by the transfer characteristics of Figure 8—6, the PLL system has an inherent selectivity about the center frequency set by the VCO free-running frequency ω_0; it will respond only to the input signal frequencies that are separated from ω_0 by less than ω_c or ω_L, depending on whether the loop starts with or without an initial lock condition. The linearity of the frequency-to-voltage conversion characteristics for the PLL is determined solely by the VCO conversion gain. Therefore, in most PLL applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.

PHASE LOCKED LOOP BUILDING BLOCKS

VOLTAGE CONTROLLED OSCILLATOR

Since three different forms of VCO have been used in the Signetics PLL series, the VCO details will not be discussed until the individual loops are described. However, a few general comments about VCOs are in order.

When the PLL is locked to a signal, the VCO voltage is a function of the frequency of the input signal. Since the VCO control voltage is the demodulated output during FM demodulation, it is important that the VCO voltage-to-frequency characteristic be linear so that the output is not distorted. Over the linear range of the VCO, the conversion gain is given by K_o (in radian/volt-sec).

$$K_o = \frac{\Delta\omega_o}{\Delta V_o}$$

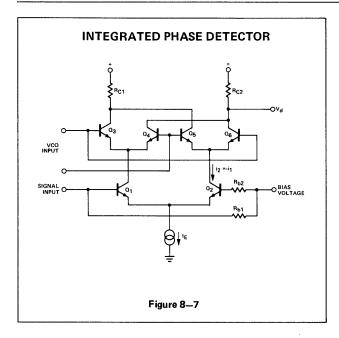Since the loop output voltage is the VCO voltage, we can get the loop output voltage as

$$\Delta V_o = \frac{\Delta\omega_o}{K_o}$$

The gain K_o can be found from the data sheet by taking the change in VCO control voltage for a given percentage frequency deviation and multiplying by the center frequency. When the VCO voltage is changed, the frequency change is virtually instantaneous.

PHASE DETECTOR

All Signetics phase locked loops use the same form of phase detector—often called the doubly-balanced multiplier or mixer. Such a circuit is shown in Figure 8—7.

INTEGRATED PHASE DETECTOR

Figure 8—7

The input stage formed by transistors Q_1 and Q_2 may be viewed as a differential amplifier which has a collector resistance R_C and whose differential gain at balance is the ratio of R_C to the emitter resistance r_e of Q_1 and Q_2.

$$A_d = \frac{R_C}{r_e} = \frac{R_C}{\frac{0.026}{I_e/2}} = \frac{R_C}{0.013\, I_e}$$

The switching stage formed by $Q_3 - Q_6$ is switched on and off by the VCO square wave. Since the collector current swing of Q_2 is the negative of the collector current swing of Q_1, the switching action has the effect of multiplying the differential stage output first by +1 and then by −1. That is, when the base of Q_4 is positive, R_{C2} receives I_1 and when the base of Q_6 is positive, R_{C2} receives $I_2 = -I_1$. Since we have called this a multiplier, let us perform the multiplication to gain further insight into the action of the phase detector.

Suppose we have an input signal which consists of two added components: a component at frequency ω_i which is close to the free-running frequency and a component at frequency ω_k which may be at any frequency. The input signal is

$$V_i + V_k = V_i \sin(\omega_i t + \theta_i) + V_k \sin(\omega_k t + \theta_k)$$

where θ_i and θ_k are the phase in relation to the VCO signal. The unity square wave developed in the multiplier by the VCO signal is

$$\frac{4}{\pi(2n+1)} \sin[(2n+1)\,\omega_0 t]$$

where ω_0 is the VCO frequency. Multiplying the two terms, using the appropriate trigonometric relationship and inserting the differential stage gain A_d, we get

$$V_d =$$

$$\frac{2A_d}{\pi}\left[\sum_{n=0}^{\infty} \frac{V_i}{(2n+1)} \cos\left[(2n+1)\,\omega_0 t - \omega_i t - \theta_i\right] \right.$$

$$- \sum_{n=0}^{\infty} \frac{V_i}{(2n+1)} \cos\left[(2n+1)\,\omega_0 t + \omega_i t + \theta_i\right]$$

$$+ \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos\left[(2n+1)\,\omega_0 t - \omega_k t - \theta_k\right]$$

$$\left. - \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos\left[(2n+1)\,\omega_0 t + \omega_k t + \theta_k\right] \right]$$

Assuming the V_k is zero, temporarily, if ω_i is close to ω_0, the first term (n = 0) has a low frequency difference frequency component. This is the beat frequency component that feeds around the loop and causes lock up by modulating the VCO. As ω_0 is driven closer to ω_i, this difference component becomes lower and lower in frequency until $\omega_0 = \omega_i$ and lock is achieved. The first term then becomes

$$\frac{2A_d V_i}{\pi} \cos\theta_i$$

which is the usual phase detector formula showing the dc component of the phase detector during lock. This component must equal the voltage necessary to keep the VCO at ω_0. It is possible for ω_0 to equal ω_i momentarily during the lock up process and, yet, for the phase to be incorrect so that ω_0 passes through ω_i without lock being achieved. This explains why lock is usually not achieved instantaneously, even when $\omega_i = \omega_0$ at t = 0.

If $n \neq 0$ in the first term, the loop can lock when $\omega_i = (2n + 1) \omega_o$, giving the dc phase detector component

$$\frac{2A_dV_i}{\pi(2n + 1)} \quad \cos \theta_i$$

showing that the loop can lock to odd harmonics of the center frequency. The $(2n + 1)$ term in the denominator shows that the phase detector output is lower for harmonic lock, which explains why the lock range decreases as higher and higher odd harmonics are used to achieve lock.

Note also that the phase detector output during lock is (assuming A_d is constant) also a function of the input amplitude V_i. Thus, for a given dc phase detector output V_d, an input amplitude decrease must be accompanied by a phase change. Since the loop can remain locked only for θ_i between 0 and 180°, the lower V_i becomes, the more reduced is the lock range.

Going to the second term, we note that during lock the lowest possible frequency is $\omega_o + \omega_i = 2\omega_i$. A sum frequency component is always present at the phase detector output. This component is usually greatly attenuated by the low pass filter capacitor connected to the phase detector output. However, when rapid tracking is required (as with high-speed FM detection or FSK-frequency shift keying), the requirement for a relatively high frequency cutoff in the low pass filter may leave this component unattenuated to the extent that it interferes with detection. At the very least, additional filtering may be required to remove this component. Components caused by $n \neq 0$ in the second term are both attenuated and of much higher frequency, so they may be neglected.

Suppose that we have other frequencies represented by V_k present. What is their effect for $V_k \neq 0$?

The third term shows that V_k introduces another difference frequency component. Obviously, if ω_k is close to ω_i, it can interfere with the locking process since it may form a beat frequency of the same magnitude as the desired locking beat frequency. Suppose lock has been achieved, however, so that $\omega_o = \omega_i$. In order for lock to be maintained, the average phase detector output must be constant. If $\omega_o = \omega_k$ is relatively low in frequency, the phase θ_i must change to compensate for this beat frequency. Broadly speaking, any signal in addition to the signal to which the loop is locked causes a phase variation. Usually this is negligible since ω_k is often far removed from ω_i. However, it has been stated that the phase θ_i can move only between 0 and 180°. Suppose the phase limit has been reached and V_k appears. Since it cannot be compensated for, it will drive the loop out of lock. This explains why extraneous signals can result in a decrease in the lock range. If V_k is assumed to be an instantaneous noise component, the same effect occurs. When the full

swing of the loop is being utilized, noise will decrease the lock or tracking range. We can reduce this effect by decreasing the cutoff frequency of the low pass filter so that the $\omega_o - \omega_k$ is attenuated to a greater extent, which illustrates that noise immunity and out-band frequency rejection is improved (at the expense of capture range since $\omega_o - \omega_i$ is likewise attenuated) when the low pass filter capacitor is large.

The third term can have a dc component when ω_k is an odd harmonic of the locked frequency so that $(2n + 1)(\omega_o - \omega_i)$ is zero and θ_k makes its appearance. This will have an effect on θ_i which will change the θ_i versus frequency ω_i. This is most noticeable when the waveform of the incoming signal is, for example, a square wave. The θ_k term will combine with the θ_i term so that the phase is a linear function of input frequency. Other waveforms will give different phase versus frequency functions. When the input amplitude V_i is large and the loop gain is large, the phase will be close to 90° throughout the range of VCO swing, so this effect is often unnoticed.

The fourth term is of little consequence except that if ω_k approaches zero, the phase detector output will have a component at the locked frequency ω_o at the output. For example, a dc offset at the input differential stage will appear as a square wave of fundamental ω_o at the phase detector output. This is usually small and well attenuated by the low pass filter. Since many out-band signals or noise components may be present, many V_k terms may be combining to influence locking and phase during lock. Fortunately, we need only worry about those close to the locked frequency.

The quadrature phase detector action is exactly the same except that its output is proportional to the sine of the phase angle. When the phase θ_i is 90°, the quadrature phase detector output is then at its maximum, which explains why it makes a useful lock or amplitude detector. The output of the quadrature phase detector is given by:

$$V_q = \frac{2A_qV_i}{\pi} \quad \sin \theta_i$$

where V_i is the constant or modulated AM signal and $\theta_i \approx 90°$ in most cases so that sine $\theta_i = 1$ and

$$V_q = \frac{2A_qV_i}{\pi}$$

This is the demodulation principle of the autodyne receiver and the basis for the 567 tone decoder operation.

FUNCTIONAL APPLICATIONS

LOW PASS FILTER

The simplest type of low pass filter for the second order loop is a single pole RC type shown in Figure 8—5b. In all Signetics' loops, the resistor is internal and the capacitor is external. The inside resistor greatly improves the center frequency stability of the loop with temperature variations. Fortunately, the capture range and loop damping are related to the square root of this internal resistor value, so variations in its absolute value have little effect on loop performance. The nominal value of the internal resistor for each loop is given in the circuit diagrams of the detailed circuit descriptions in this chapter. The typical tolerance on these integrated resistors is ±20%.

As a functional building block, the phase locked loop is suitable for a wide variety of frequency related applications. These applications generally fall into one or more of the following categories:

  a.) FM Demodulation
  b.) Frequency Synthesizing
  c.) Frequency Synchronization
  d.) Signal Conditioning
  e.) AM Demodulation

FM DEMODULATION

If the PLL is locked to a frequency modulated (FM) signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage, which forces the VCO to maintain lock with the input signal then becomes the demodulated FM output. The linearity of this demodulated signal depends solely on the linearity of the VCO control-voltage-to-frequency transfer characteristic.

It should be noted that since the PLL is in lock during the FM demodulation process, the response is linear and can be readily predicted from a root locus plot.
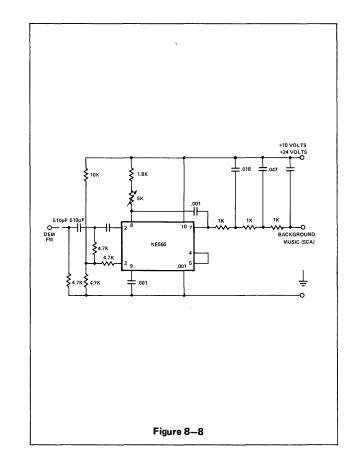
FM demodulation applications are numerous; however, some of the more popular are:

Broadcast FM Detection

Here, the PLL can be used as a complete IF strip, limiter and FM detector which may be used for detecting either wide or narrow band FM signals with greater linearity than can be obtained by other means. For frequencies within the range of the VCO, the PLL functions as a self contained receiver since it combines the functions of frequency selectivity and demodulation. One increasingly popular use of the PLL is in scanning-receivers where a number of broadcast channels may be sequentially monitored by simply varying the VCO free-running frequency.

FM Telemetry

This application involves demodulation of a frequency modulated subcarrier of the main channel. A popular example here is the use of the PLL to recover the SCA (storecast music) signal from the combined signal of many commercial FM broadcast stations. The SCA signal is a 67kHz frequency modulated subcarrier which puts it above the frequency spectrum of the normal stereo or monaural FM program material. By connecting the circuit of Figure 8—8 to a point between the FM discrimator and the de-emphasis filter of a commercial band (home) FM receiver and tuning the receiver to a station which broadcasts an SCA signal, one can obtain hours of commercial free background music.

Figure 8—8

Frequency Shift Keying (FSK)

This refers to what is essentially digital frequency modulation. FSK is a means for transmitting digital information by a carrier which is shifted between two discrete frequencies. In this case, the two discrete frequencies correspond to a digital "1" and a digital "0," respectively. When the PLL is locked to a FSK signal, the demodulated output (error voltage) shifts between two discrete voltage levels, corresponding to the demodulated binary output. FSK techniques are often used in modems (modulator-demodulators), intended for transmitting data over telephone lines.
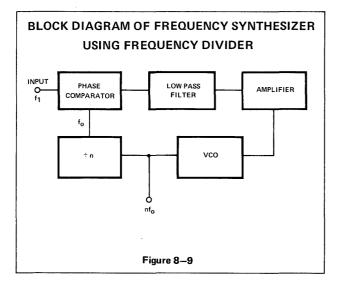
FREQUENCY SYNTHESIS

Frequency Multiplication can be achieved with the PLL in two ways:

- a.) Locking to a harmonic of the input signal
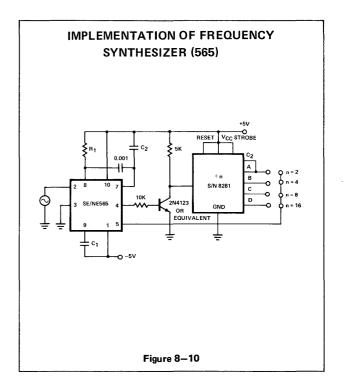- b.) Insertion of a counter (digital frequency divider) in the loop

Harmonic locking is the simplest and can usually be achieved by setting the VCO free-running frequency to a multiple of the input frequency and allowing the PLL to lock. A limitation on this scheme, however, is that the lock range decreases as successively higher and weaker harmonics are used for locking. This limits the practical harmonic locking range to multiples of approximately less than ten. For larger multiples, the second scheme is more desirable.

A block diagram of the second scheme is shown in Figure 8–9. Here, the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the *divided* VCO frequency is locked to the input frequency so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the counter. An obvious practical application of this multiplication property, is the use of the PLL in wide range frequency synthesizers.

BLOCK DIAGRAM OF FREQUENCY SYNTHESIZER USING FREQUENCY DIVIDER

Figure 8–9

In frequency multiplication applications it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency component is dc and is the error voltage which drives the VCO to keep the PLL in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal) if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication it

is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more underdamped loop transient response.
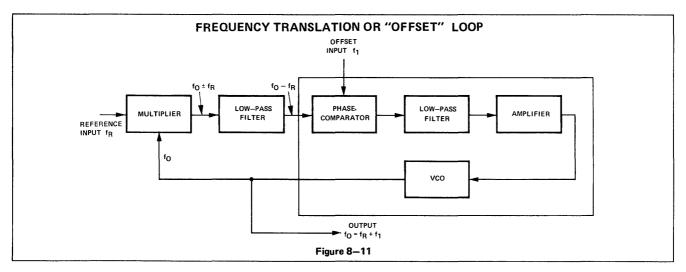
For the case of frequency fractionalization, both harmonic locking and frequency countdown could be used to generate, for instance, a frequency exactly 16/3 the input. In this case, the circuit of Figure 8–10 could be used with the initial VCO frequency set to approximately 16/3 the expected input frequency. The counter then divides the VCO frequency by 16, and the input is locked to the 3rd harmonic of the counter output. Now the output can be taken as the VCO output and it will be exactly 16/3 of the input frequency as long as the loop is in lock.

IMPLEMENTATION OF FREQUENCY SYNTHESIZER (565)

Figure 8–10

Frequency translation can be achieved by adding a mixer and a low pass filter stage to the basic PLL as shown in Figure 8–11. With this system the PLL can be used to translate the frequency of a highly stable but fixed-frequency reference oscillator by a small amount in frequency.

In this case, the reference input f_R and the VCO output f_o are applied to the inputs of the mixer stage. The mixer output is made up of the sum and the difference components of f_R and f_o. The sum component is filtered by the first low pass filter. The translation or offset frequency f_1 is applied to the phase comparator along with the $f_R - f_o$ component of the mixer output. When the system is in lock, the two inputs of the phase comparator are at identical frequency, that is,

$$f_o - f_R = f_1 \quad \text{or} \quad f_o = f_R + f_1$$

FREQUENCY TRANSLATION OR "OFFSET" LOOP

Figure 8—11

FREQUENCY SYNCHRONIZATION

Using the phase locked loop system, the frequency of the less precise VCO can be phase locked with a low level but highly stable reference signal. Thus, the VCO output reproduces the reference signal frequency at the same per-unit accuracy, but at a much higher power level. In some applications, the synchronizing signal can be in the form of a low duty cycle burst at a specific frequency. Then, the PLL can be used to regenerate a coherent CW reference frequency blocking onto this short synchronizing pulse. A typical example of such an application is seen in the phase locked chroma-reference generators of color television receivers.

In digital systems, the PLL can be used for a variety of synchronization functions. For example, two system clocks can be phase locked to each other such that one can function as a back up for the other; or PLLs can be used in synchronizing disk or tape drive mechanisms in information storage and retrieval systems. In pulse-code modulation (PCM) telemetry receivers or in repeater systems, the PLL is used for bit synchronization.

Other popular applications include locking to WWVB to generate a cheap laboratory frequency standard and synchronizing tape speed for playback of a tape recorded at an irregular speed.
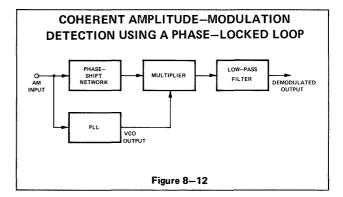
SIGNAL CONDITIONING

By proper choice of the VCO free-running frequency, the PLL can be made to lock to any one of a number of signals present at the input. Hence, the VCO output reproduces the frequency of the desired signal, while greatly attenuating the undesired frequencies of sidebands present at the input.

If the loop bandwidth is sufficiently narrow, the signal-to-noise ratio at the VCO output can be much better than that at the input. Thus, the PLL can be used as a noise filter for regenerating weak signals buried in noise.

AM DEMODULATION

AM demodulation may be achieved with PLL by the scheme shown in Figure 8—12. In this mode of operation, the PLL functions as a synchronous AM detector. The PLL locks on the carrier of the AM signal so that the VCO output has the same frequency as that of the carrier but no amplitude modulation. The demodulated AM is then obtained by multiplying the VCO signal with the modulated input signal and filtering the output to remove all but the difference frequency component. It may be recalled from the initial discussion that when the frequency of the input signal is identical to the free-running frequency of the VCO, the loop goes into lock with these signals 90° out of phase. If the input is now shifted 90° so that it is in phase with the VCO signal and the two signals are mixed in a second phase comparator, the average dc value (difference frequency component) of the phase comparator output will be directly proportional to the amplitude of the input signal.

The PLL still exhibits the same capture range phenomena discussed earlier so that the loop has an inherent high degree of selectivity centered about the free-running VCO frequency. Because this method is essentially a coherent detection technique which involves averaging of the two compared signals, it offers a higher degree of noise immunity than can be obtained with conventional peak-detector-type AM demodulators.

COHERENT AMPLITUDE—MODULATION DETECTION USING A PHASE—LOCKED LOOP

Figure 8—12

SECTION 3

GENERAL LOOP SETUP AND TRADEOFFS

PHASE LOCKED LOOP MEASUREMENT TECHNIQUES

MONOLITHIC PHASE LOCKED LOOP DESCRIPTIONS

EXPANDING LOOP CAPABILITIES

GENERAL LOOP SETUP AND TRADEOFFS

In a given application, maximum PLL effectiveness can be achieved if the user understands the tradeoffs which can be made. Generally speaking, the user is free to select the frequency, tracking or lock range, capture range and input amplitude.

CENTER FREQUENCY SELECTION

Setting the center frequency is accomplished by selecting one or two external components. The center frequency is usually set in the center of the expected input frequency range. Since the loop's ability to capture is a function of the *difference* between the incoming and free-running frequencies, the band edges of the capture range are *always* an equal distance (in Hz) from the center frequency. Typically, the lock range is also centered about the free-running frequency. Occasionally, the center frequency is chosen to be offset from the incoming so that detection or tracking range is limited on one side. This permits rejection of an adjacent higher or lower frequency signal without paying the penalty for narrow band operation (reduced tracking speed).

All of Signetics' loops use a multiplier in which the input signal is multiplied by a unity square wave at the VCO frequency. The odd harmonics present in the square wave permit the loop to lock to input signals at these odd harmonics. Thus, the center frequency may be set to, say, 1/3 or 1/5 of the input signal. The tracking range however, will be considerably reduced as the higher harmonics are utilized.

The foregoing phase detector discussion would suggest that the PLL cannot lock to subharmonics because the phase detector cannot produce a dc component if ω_i is less than ω_o.

The loop can lock to both odd harmonic and subharmonic signals in practice because such signals often contain harmonic components at f_o. For example, a square wave of fundamental $f_o/3$ will have a substantial component at f_o to which the loop can lock. Even a pure sine wave input signal can be used for harmonic locking if the PLL input stage is overdriven (the resultant internal limiting generates harmonic frequencies). Locking to even harmonics or subharmonics is the least satisfactory since the input or VCO signal must contain second harmonic distortion. If locking to even harmonics is desired, the duty cycle of the input and VCO signals must be shifted away from the symmetrical to generate substantial even harmonic content.

In evaluating the loop for a potential application, it is best to actually compute the magnitude of the expected signal component nearest f_o. This magnitude can be used to estimate the capture and lock range.

All of Signetics' loops are stabilized against center frequency drift due to power supply variations. Both the 565 and the 567 are temperature compensated over the entire military temperature range (−55 to +125°C). To benefit from this inherent stability, however, the user must provide equally stable (or better) external components. For maximum cost effectiveness in some noncritical applications, the user may wish to trade some stability for lower cost external components.

TRACKING OR LOCK RANGE CONTROL

Two things limit the lock or tracking range. First, any VCO can only swing so far; if the input signal frequency goes beyond this limit, lock will be lost. Second, the voltage developed by the phase detector is proportional to the product of *both* the phase and the amplitude of the in-band component to which the loop is locked. If the signal amplitude decreases, the phase difference between the signal and the VCO must increase in order to maintain the same output voltage and, hence, the same frequency deviation. It often happens with low input amplitudes that even the full ±90° phase range of the phase detector cannot generate enough voltage to allow tracking wide deviations. When this occurs, the effective lock range is reduced. We must, therefore, give up some tracking capability and accept greater phase errors if the input signal is weak. Conversely, a strong input signal will allow us to use the entire VCO swing capability and keep the VCO phase (referred to the input signal) very close to 90° throughout the range. Note that tracking range does not depend on the low pass filter. However, if a low pass filter *is* in the loop, it will have the effect of limiting the maximum *rate* at which tracking can occur. Obviously, the LPF capacitor voltage cannot change instantly, so lock may be lost when large enough step changes occur. Between the constant frequency input and the step-change frequency input is some limiting frequency slew rate at which lock is just barely maintained. When tracking at this rate, the phase difference is at its limit of 0 or 180°. It can be seen that if the LPF cutoff frequency is low, the loop will be unable to track as fast as if the LPF cutoff frequency is higher. Thus, when maximum tracking rate is needed, the LPF should have a high cutoff frequency. However, a high cutoff frequency LPF will attenuate the sum frequencies to a lesser extent so that our output contains a significant and often bothersome signal

at twice the input frequency. (Remember that the multiplier forms both the sum and difference frequencies. During lock, the difference frequency is zero, but the sum frequency of twice the locked frequency is still present.) This sum frequency component can then be filtered out with an external low pass filter.

CAPTURE RANGE CONTROL

There are two main reasons for making the low pass filter time constant large. First, a large time constant provides an increased memory effect in the loop so that it remains at or near the operating frequency during momentary fading or loss of signal. Second, the large time constant integrates the phase detector output so that increased immunity to noise and out-band signals is obtained.

Besides the lower tracking rates attendant to large loop filters, other penalties must be paid for the benefits gained. The capture range is reduced and the capture transient becomes longer. Reduction of capture range occurs because the loop must utilize the magnitude of the difference frequency component at the phase detector to drive the VCO towards the input frequency. If the LPF cutoff frequency is low, the difference component amplitude is reduced and the loop cannot swing as far. Thus, the capture range is reduced.

CHOICE OF INPUT LEVEL

Whenever amplitude limiting of the in-band signal occurs, whether in the loop input stages or prior to the input, the tracking (lock) and capture range becomes independent of signal amplitude.

Better noise and out-band signal immunity is achieved when the input levels are below the limiting threshold since the input stage is in its linear region and the creation of cross-modulation components is reduced. Higher input levels will allow somewhat faster operation due to greater phase detector gain and will result in a lock range which becomes constant with amplitude as the phase detector gain becomes constant. Also, high input levels will result in a linear phase versus frequency characteristic.

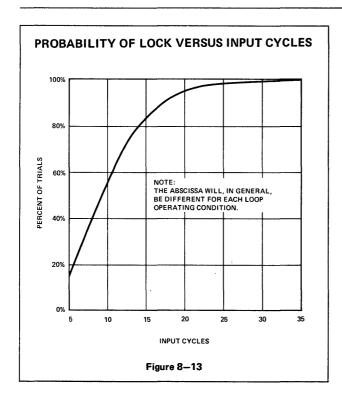## LOCK-UP TIME AND TRACKING SPEED CONTROL

In tracking applications, lock-up time is normally of little consequence, but occasions do arise when it is desirable to keep lock-up time short to minimize data loss when noise or extraneous signals drive the loop out of lock. Lock-up time is of great importance in tone decoder type applications. Tracking speed is important if the loop is used to

demodulate an FM signal. Although the following discussion dwells largely on lock-up time, the same comments apply to tracking speed.

No simple expression is available which adequately describes the acquisition or lock-up time. This may be appreciated when we review the following factors which influence lock-up time.

a.) Input phase
b.) Low pass filter characteristic
c.) Loop damping
d.) Deviation of input frequency from center frequency
e.) In-band input amplitude
f.) Out-band signals and noise
g.) Center frequency

Fortunately, it is usually sufficient to know how we can improve the lock-up time and what we must tradeoff to get faster lock-up. Suppose we have set up a loop or tone decoder and find that occasionally the lock-up transient is too long. What can be done to improve the situation—keeping in mind the factors that influence lock?

a.) Initial phase relationship between incoming signal and VCO — This is the greatest single factor influencing the lock time. If the initial phase is wrong, it first drives the VCO frequency *away* from the input frequency so that the VCO frequency must walk back on the beat notes. Figure 8–13 gives a typical distribution of lock-up times with the input pulse initiated at random phase. The only way to overcome this variation is to send phase information all the time so that a favorable phase relationship is guaranteed at t = 0. For example, a number of PLLs or tone decoders may be weakly locked to low amplitude harmonics of pulse train and the transmitted tone phase-related to the same pulse train. Usually, however, the incoming phase cannot be controlled.

b.) Low pass filter — The larger the low pass filter time constant, the longer will be the lock-up time. We can reduce lock-up time by decreasing the filter time constant, but in doing so, we sacrifice some of the noise immunity and out-band signal rejection which caused us to use a large filter in the first place. We must also accept a sum frequency (twice the VCO frequency) component at the low pass filter and greater phase jitter resulting from out-band signals and noise. In the case of the tone decoder (where control of the capture range is required since it specifies the device bandwidth) a lower value of low pass capacitor automatically increases the bandwidth. We gain speed only at the expense of added bandwidth.

PROBABILITY OF LOCK VERSUS INPUT CYCLES

NOTE:
THE ABSCISSA WILL, IN GENERAL,
BE DIFFERENT FOR EACH LOOP
OPERATING CONDITION.

PERCENT OF TRIALS

INPUT CYCLES

Figure 8–13

the lock-up time may be limited by the rate at which the low pass capacitor can charge with the reduced phase detector output (see d above).

f.) Out-band signals and noise — Low levels of extraneous signals and noise have little effect on the lock-up time, neither improving or degrading it. However, large levels may over-drive the loop input stage so that limiting occurs, at which point the in-band signal starts to be suppressed. The lower effective input level can cause the lock-up time to increase, as discussed in e above.

g.) Center frequency — Since lock-up time can be described in terms of the number of cycles to lock, fastest lock-up is achieved at higher frequencies. Thus, whenever a system can be operated at a higher frequency, lock will typically take place faster. Also, in systems where different frequencies are being detected, the higher frequencies *on the average* will be detected before the lower frequencies. How-ever, because of the wide variation due to initial phase, the reverse may be true for any single trial.

c.) Loop damping — Loop damping for a simple time constant low pass filter is:

$$\zeta = \frac{1}{2} \sqrt{\frac{1}{\tau K_v}}$$

Damping can be increased not only by reducing τ, as discussed above, but also by reducing the loop gain K_v. By using the loop gain reduction to control bandwidth or capture and lock range, we achieve better damping for narrow bandwidth operation. The penalty for this damping is that more phase detector output is required for a given deviation so that phase errors are greater and noise immunity is reduced. Also, more input drive may be required for a given deviation.

d.) Input frequency deviation from free-running frequency — Naturally, the further an applied input signal is from the free-running frequency of the loop, the longer it will take the loop to reach that frequency due to the charging time of the low pass filter capacitor. Usually, how-ever, the effect of this frequency deviation is small compared to the variation resulting from the initial phase uncertainty. Where loop damping is very low, however, it may be predominant.

e.) In-band input amplitude — Since input ampli-tude is one factor in the phase detector gain K_d and since K_d is a factor in the loop gain K_v, damping is also a function of input amplitude. When the input amplitude is low,

PLL MEASUREMENT TECHNIQUES

This section deals with user measurements of PLL operation. The techniques suggested are meant to help the user in evaluating the performance of his PLL during the initial setup period as well as to point out some pitfalls that may obscure loop evaluation. Recognizing that the user's test equipment may be limited, we have stressed the techniques which require a minimum of standard test items.

CENTER FREQUENCY

Center frequency measurements are easily made by connecting a frequency counter or oscilloscope to the VCO output of the loop. The loop should be connected in its final configuration with the chosen values of input, bypass and low pass filter capacitors. No input signal should be present. As the center frequency is read out, it can be adjusted to the desired value by the adjustment means selected for the particular loop. It is important not to make the frequency measurement directly at the timing capacitor unless the capacity added by the measurement probe is much less than the timing capacitor value since the probe capacity will then cause a frequency error.

When the frequency measurement is to be converted to a dc voltage for production readout or automated testing, a calibrated phase locked loop can be used as a frequency meter (see Applications Section).

CAPTURE AND LOCK RANGE

Figure 8—14a shows a typical measurement setup for capture and lock range measurements. The signal input from a variable frequency oscillator is swept linearly through the frequency range of interest and the loop FM output is displayed on a scope or (at low frequencies) X—Y recorder. The sweep voltage is applied to the X axis.

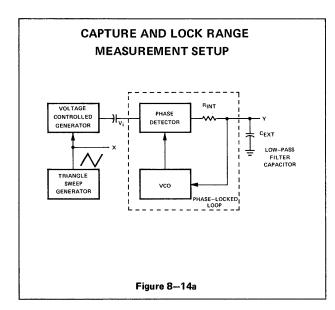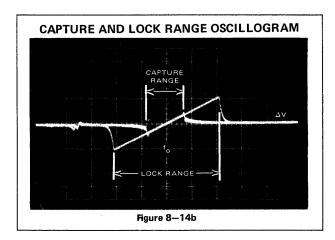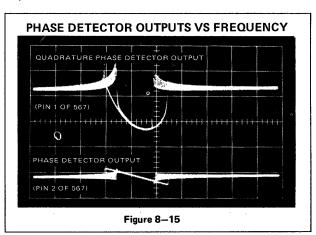### CAPTURE AND LOCK RANGE MEASUREMENT SETUP

Figure 8—14a

Figure 8—14b shows the type of trace which results. The lock range (also called hold-in or tracking range) is given by the outer lines on the trace, which are formed as the incoming frequency sweeps *away* from the center frequency. The inner trace, formed as the frequency sweeps *toward* the center frequency, designates the capture range. Linearity of the VCO is revealed by the straightness of the trace portion within the lock range. The slope ($\Delta f/\Delta V$) is the gain or conversion factor for the VCO.

CAPTURE AND LOCK RANGE OSCILLOGRAM

Figure 8—14b

By using the sweep technique, the effect on center frequency, capture range and lock range of the input amplitude, supply voltage, low pass filter and temperature can be examined.

Because of the lock-up time duration and variation, the sweep frequency must be very much lower than the center frequency, especially when the capture range is below 10% of center frequency. Otherwise, the *apparent* capture and lock range will be a function of sweep frequency. It is best to start sweeping as slow as possible and, if desired, increase the rate until capture range begins to show an apparent reduction—indicating that the sweep is too fast. Typical sweep frequencies are in the range of 1/1000 to 1/100,000 of the center frequency. In the case of the 561 and 567, the quadrature detector output may be similarly displayed on the Y axis, as shown in Figure 8—15, showing the output level versus frequency for one value of input amplitude.

PHASE DETECTOR OUTPUTS VS FREQUENCY

Figure 8—15

Capture and lock range measurements may also be made by sweeping the generator manually through the band of interest. Sweeping must be done very slowly as the edges of the capture range are approached (sweeping toward center frequency) or the lock-up transient delay will cause an error in reading the band edge. Frequency should be read from the generator rather than the loop VCO because the VCO frequency gyrates wildly around the center frequency just before and after lock. Lock and unlock can be readily detected by simultaneously monitoring the input and VCO signals, the dc voltage at the low pass filter or the ac beat frequency components at the low pass filter. The latter are greatly reduced during lock as opposed to frequencies just outside of lock.

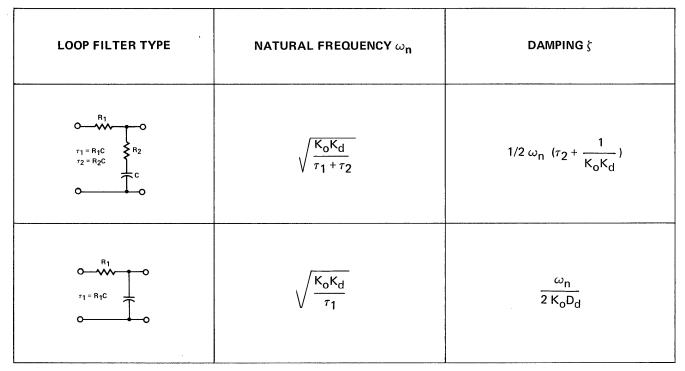## FM AND AM DEMODULATION DISTORTION

These measurements are quite straightforward. The loop is simply setup for FM or AM (561 or 567) detection and the test signal is applied to the input. A spectrum analyzer or distortion analyzer (HP 333 A) can be used to measure distortion at the FM or AM output.

For FM demodulation, the input signal amplitude must be large enough so that lock is not lost at the frequency extremes. The data sheets give the lock (or tracking) range as a function of input signal and the optional range control adjustments. Due to the inherent linearity of the VCOs, it makes little difference whether the FM carrier is at the free-running frequency or offset slightly as long as the tracking range limits are not exceeded.

The faster the FM modulation in relation to the center frequency, the lower the value of the capacitor in the low pass filter must be for satisfactory tracking. As this value decreases, however, it attenuates the sum frequency component of the phase detector output less. The demodulated signal will appear to have greater distortion unless this component is filtered out before the distortion is measured. The same comment applies to the measurement of AM distortion on the 561.

When AM distortion is being measured, the carrier frequency offset becomes more important. The lowest absolute value of carrier voltage at the modulation valleys must be high enough to maintain lock at the frequency deviation present. Otherwise, lock will periodically be lost and the distortion will be unreasonable. For example, the typical tracking range as a function of input signal graph in the 561 data sheet gives a total 3% tracking range at 0.3mV rms input. Thus, for a carrier deviation of 1.5%, the carrier must not drop below 0.3V rms in the modulation valleys. Naturally, the AM amplitude must not be too high or the AM information will be suppressed.

NATURAL FREQUENCY (ω_n)

Expressions for the natural frequency in terms of the loop gains and filter parameters are given in Table 8—2.

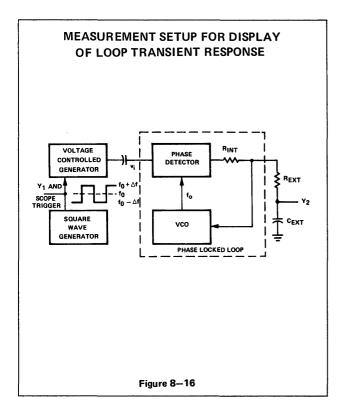## EXPRESSIONS FOR ω_n AND ζ IN SECOND ORDER LOOP

LOOP FILTER TYPE	NATURAL FREQUENCY ω_n	DAMPING ζ
$\tau_1 = R_1 C$ $\tau_2 = R_2 C$	$\sqrt{\dfrac{K_o K_d}{\tau_1 + \tau_2}}$	$1/2\, \omega_n \left(\tau_2 + \dfrac{1}{K_o K_d} \right)$
$\tau_1 = R_1 C$	$\sqrt{\dfrac{K_o K_d}{\tau_1}}$	$\dfrac{\omega_n}{2\, K_o D_d}$

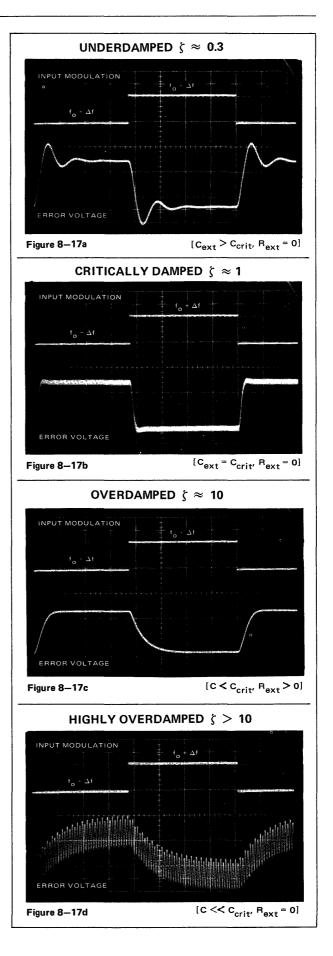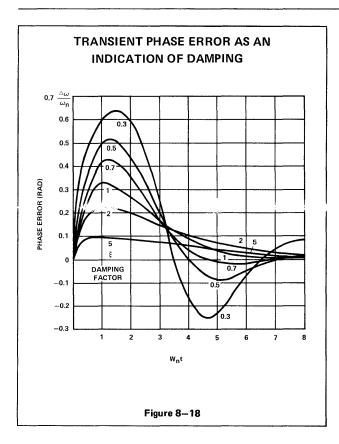**Table 8—2**

The natural frequency (ω_n) of a loop in its final circuit configuration can be measured by applying a frequency modulated signal of the desired amplitude to the loop (Table 8—2 shows that the natural frequency is a function of K_d, in turn a function of input amplitude). As the modulation frequency (ω_m) is increased, the phase relationship between the modulation and recovered sine wave will go through 90° at $S_m = \omega_n$ and the output amplitude will peak.

DAMPING (ζ)

As shown in Table 8—2 in the discussion on low pass filter, damping is a function of K_o, K_d and the low pass filter. Since K_o and K_d are functions of center frequency and input amplitude, respectively, damping is highly dependent on the particular operating condition of the loop. Damping estimates for the desired operating condition can be made by applying an input signal which is frequency modulated within the lock range by a square wave. The low pass filter voltage is then monitored on an oscilloscope which is synchronized to the modulating waveform, as shown in Figure 8—16. Figure 8—17 shows typical waveforms displayed. The loop damping can be estimated by comparing the number and magnitude of the overshoots with the graph of Figure 8—18, which gives the transient phase error due to a step in input frequency.

MEASUREMENT SETUP FOR DISPLAY OF LOOP TRANSIENT RESPONSE

Figure 8—16

UNDERDAMPED $\zeta \approx 0.3$

Figure 8—17a $[C_{ext} > C_{crit}, R_{ext} = 0]$

CRITICALLY DAMPED $\zeta \approx 1$

Figure 8—17b $[C_{ext} = C_{crit}, R_{ext} = 0]$

OVERDAMPED $\zeta \approx 10$

Figure 8—17c $[C < C_{crit}, R_{ext} > 0]$

HIGHLY OVERDAMPED $\zeta > 10$

Figure 8—17d $[C \ll C_{crit}, R_{ext} = 0]$

TRANSIENT PHASE ERROR AS AN INDICATION OF DAMPING

Figure 8—18

Another way of estimating damping is to make use of the frequency response plot measured for the natural frequency (ω_n) measurement. For low damping constants, the frequency response measurement peak will be a strong function of damping. For high damping constants, the 3dB-down point will give the damping. Table 8—3 gives the approximate relationship.

ESTIMATING DAMPING FROM MODULATING FREQUENCY (ω_m) RESPONSE

ζ	PEAK AMPLITUDE LOW FREQUENCY AMPLITUDE	$\dfrac{\omega_{-3dB}}{\omega_n}$
.3	6.0dB	1.8
.5	3.2dB	2.1
.7	2.2dB	2.5
1.0	1.3dB	4.3
5.0	.5dB	10

NOISE EFFECTS

The effect of input noise on loop operation is very difficult to predict. Briefly, the input noise components near the center frequency are converted to phase noise. When the phase noise becomes so great that the $\pm 90°$ permissible phase variation is exceeded, the loop drops out of lock or fails to acquire lock. The best technique is to actually apply the anticipated noise amplitude and bandwidth to the input and then perform the capture and lock range measurements as well as perform operating tests with the anticipated input level and modulation deviations. By including a small safety factor in the loop design to compensate for small processing variations, satisfactory operation can be assured.

SIMPLIFIED MEASUREMENT EQUIPMENT

The majority of the PLL tests described can be done with a signal generator, a scope and a frequency counter. Most laboratories have these. A low-cost digital voltmeter will facilitate accurate measurement of the VCO conversion gain. Where the need for a FM generator arises, it may be met in most cases by the VCO of a Signetics PLL. (See the applications in this section.) Any of the loops may be set up to operate as a VCO by simply applying the modulating voltage to the low pass filter terminal(s). The resulting generator may be checked for linearity by using the counter to check frequency as a function of modulating voltage. Since the VCOs may be modulated right down to dc, the calibration may be done in steps. Moreover, Gardner*shows how loop measurements may be made by applying a *constant* frequency to the loop input and the modulating signal to the low pass filter terminal to simulate the effect of a FM input so that a FM generator may be omitted for many measurements.
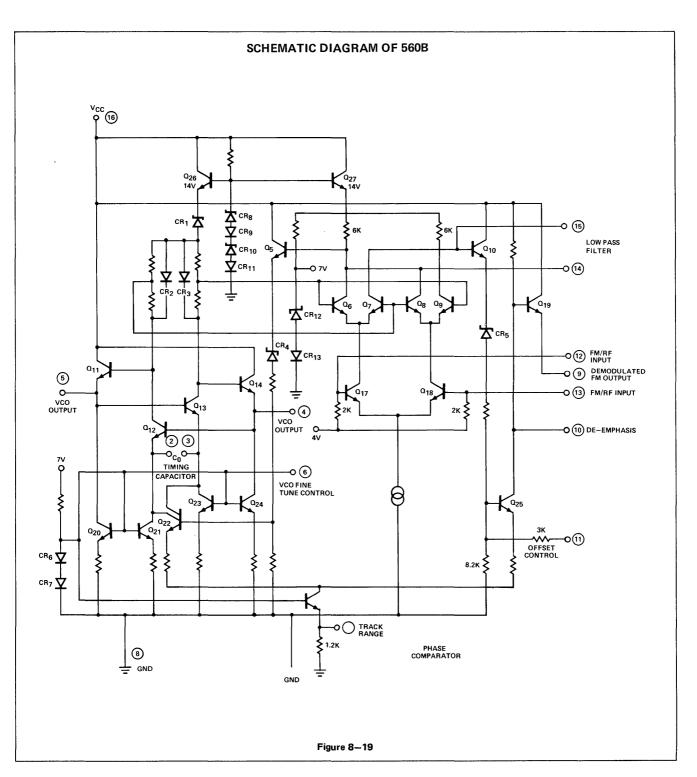
*see references

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SIGNETICS MONOLITHIC PHASE LOCKED LOOPS

DETAILED DESCRIPTION OF 560B, 561B AND 562B

The 560B, 561B and 562B phase locked loops are all derived from the same monolithic die with different metal interconnections. Each device contains the same VCO, phase detector and voltage regulator stage and, hence, the basic loop parameters are the same for all three circuits.

The 560B is the most fundamental of the three circuits, having a block diagram equivalent to that shown in Figure 8–1. The actual circuit diagram is shown in Figure 8–19.

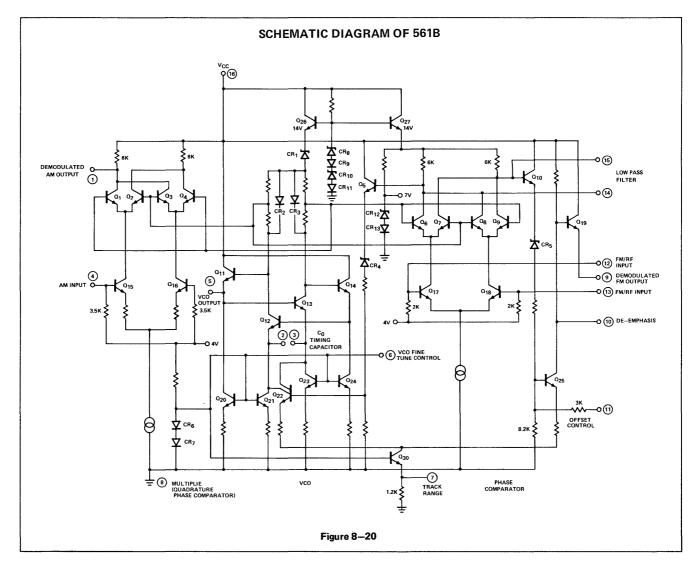**SCHEMATIC DIAGRAM OF 560B**

Figure 8–19

The VCO is a high frequency emitter-coupled multivibrator formed by transistors $Q_{11}-Q_{14}$. It operates from a regulated 7.7V supply formed by 6.3V supply formed by Zener diode CR_1 (a reverse-biased base-emitter junction) in series with the 14V regulated supply. The VCO frequency is thus immune from supply voltage variations. Four constant current sources formed by Q_{20}, Q_{21}, Q_{23}, Q_{24}, and biased by CR_6 and CR_7 supply operating current for the VCO. Voltage control of the frequency is achieved by a differential amplifier, Q_{22} and Q_{25}. As the base voltage of Q_{22} increases with respect to the base voltage of Q_{25}, additional current is supplied to the emitters of Q_{12} and Q_{13}, increasing the charge and discharge current of the timing capacitor C_0, increasing the VCO frequency. Reducing the base voltage of Q_{22} with respect to Q_{25} similarly reduces the VCO frequency. Two Zener diodes and two transistors, CR_4, CR_5, Q_5 and Q_{10}, respectively, provide level shifting which allows the VCO to be driven by the outputs of the phase detector.

The phase detector is a doubly-balanced multiplier formed by transistors Q_6-Q_9, Q_{17} and Q_{18}. Signal input is made to the lower stage, biased at about 4V by means of 2kΩ base resistors. The upper stage is biased and driven directly by the VCO output taken from the collector resistors of Q_{12} and Q_{13}. A differential output signal is available between the collectors of Q_6 (and Q_8) and Q_7 (and Q_9). An external network, together with the 6K collector resistors, comprises the low pass filter. The phase detector is operated from regulated 14V appearing at the emitter of Q_{27}. A resistor in the collector of Q_{25} can be shunted with an external capacitor to form a de-emphasis filter. The de-emphasized signal is buffered by emitter follower Q_{19} before being brought out.
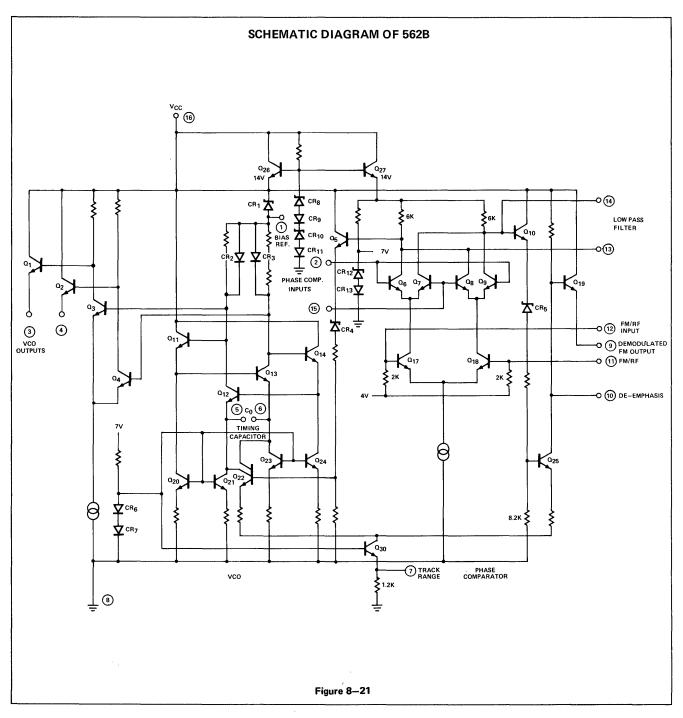
The TRACK RANGE input, pin 7 on all three loops, allows the user to control the total current flowing through the frequency controlling differential amplifier Q_{22}, Q_{25}. This is done by controlling the effective emitter resistance of Q_{29}, the current source for Q_{22}, Q_{25}. Current may be added or subtracted at pin 7 to, respectively, reduce or increase the tracking range.

SCHEMATIC DIAGRAM OF 561B

Figure 8—20

The 561, shown in Figure 8–20, contains all of the circuitry of the 560 and in addition, has a quadrature phase comparator. This enables it to be used as a synchronous AM detector. The quadrature phase detector consists of transistors Q_1-Q_4 and Q_{15}, Q_{16} which are biased and driven in the same manner as the loop phase detector. However, the quadrature detector input is single ended rather than differential (as the loop phase detector input) and an external 90° phase shift network is required to provide the proper phase relations. The demodulated AM output is brought out at pin 1.

The 562, shown in Figure 8–21, is basically the same as the 560 except that the loop is broken between the VCO and phase comparator. This allows a counter to be inserted in the loop for frequency multiplication applications. Transistors Q_1-Q_4 provide low impedance differential VCO outputs (pins 3 and 4), and the upper stage phase detector inputs are brought out of the package (pins 2 and 15). A bias voltage is brought out through pin 1 to provide a convenient bias level for the upper stage of the phase detector.

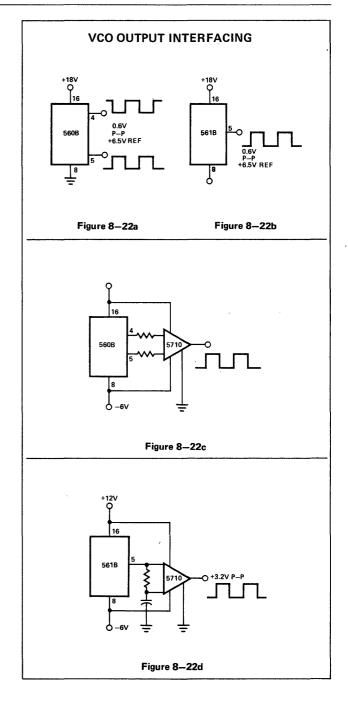**SCHEMATIC DIAGRAM OF 562B**

Figure 8–21

INTERFACING

Connection of the Signetics 560B and 561B phase locked loops to external input and output circuitry is readily accomplished; however, as with any electrical system, there are voltage, current and impedance limitations that must be considered.

The inputs of the phase comparators in the 560B, 561B and 562B and the AM detector in the 561B are biased internally from a +4 volt supply; therefore, the input signals must be capacitively coupled to the PLL to avoid interfering with this bias. These coupling capacitors should be selected to give negligible phase shift at the input frequency and impedance of the PLL. (The capacitive impedance at the operating frequency should be as small as possible, compared to the input resistance of the PLL.)
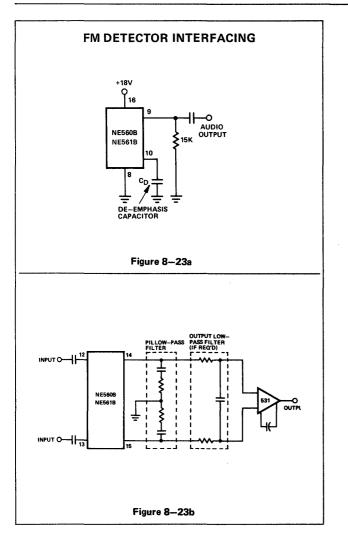
The input resistance of the phase comparator is 2000Ω single-ended, and 4000Ω when differentially connected. The input resistance of the AM detector is 3000Ω. The signal input to the phase comparator may be applied differentially if there is a common mode noise problem; however, in most applications, a single-ended input will be satisfactory. When inputs are not used differentially, the unused input may be ac-coupled to ground to double the phase detector gain at low input amplitudes.

The amplitude of the input signal should be adjusted to give optimum results with the PLL. Signals of less than 0.2mV rms may have an unsatisfactory signal-to-noise ratio; signals exceeding 25mV rms will have reduced AM rejection (less than 30dB). The AM detector will handle input signals up to 200mV peak-to-peak without excessive distortion, and will handle up to 2V peak-to-peak where distortion is not a factor.
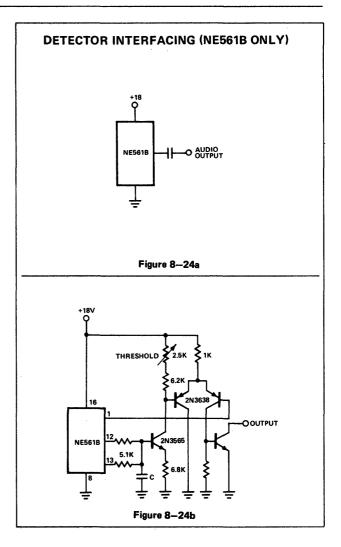
Interfacing of the available outputs is best described by referring to the following diagrams. Figure 8–22 shows the PLL VCO output as a clock circuit for logic pulse synchronization. Figures 8–22a and 8–22b show the 560B and 561B, respectively, connected directly to the clock circuit; however, this configuration may be limited by low voltage and the possibility of too large a capacitive load swamping the oscillator. Figures 8–22c and 8–22d show the PLL clock output for the 560B and 561B, respectively, using the 5710 Voltage Comparator as a buffer amplifier to provide an output voltage swing suitable for driving logic circuits. The power supply for circuits utilizing the 5710 is split (+12 and −6V dc).

VCO OUTPUT INTERFACING

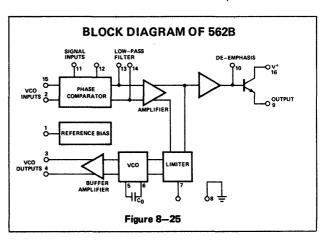Figure 8–22a   Figure 8–22b

Figure 8–22c

Figure 8–22d

In Figure 8–23a the 560B is a FM demodulator used for the detection of audio information on frequency modulated carriers. Since the lower frequency limit of this type of information is approximately 1Hz, capacitive coupling may be used. However, in some applications where carrier shifts occur at an extremely slow rate, direct coupling from the output to load is necessary. Figure 8–23b shows an alternate FM detector output configuration which should be used if a different output is desirable. In this case, the output is removed at pins 14 and 15. These pins are the terminals of the low pass filter and are in the line containing the demodulated signal. The signal level (single-ended) is about one-sixth of that at pin 9 so that additional amplification may be required.
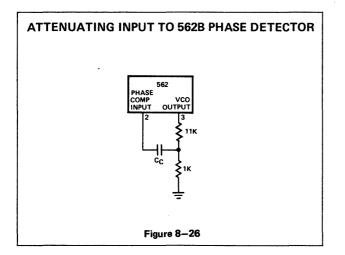
FM DETECTOR INTERFACING

Figure 8—23a

Figure 8—23b

DETECTOR INTERFACING (NE561B ONLY)

Figure 8—24a

Figure 8—24b

Additional receiving modes are illustrated in Figure 8—24 for the 561B only. Figure 8—24a shows the 561B output when used as an AM detector; note the straight capacitive coupling. Figure 8—24b shows the 561B used as a continuous wave detector. Since this version of the circuit is for the detection of CW or AM signals, external circuitry must be incorporated for use with CW inputs. With a CW input applied, there will be a dc shift at the output of the AM detector, pin 1. This shift is small compared to the no-signal dc level and may be difficult to detect in relation to power supply voltage changes. Therefore, a reference must be generated to track any power supply voltage variations and to compensate for internal PLL thermal drift. This is best accomplished by simulating a portion of the PLL internal structure. The 2N3565 npn transistor is used as a constant-current source. Its reference voltage is obtained from an internal PLL bias source at pins 12 and 13, with the current level established by the 6.8K resistor. The 6.2K resistor and the 2.5K potentiometer simulate the PLL output resistance. The differential amplifier, composed of two 2N3638 pnp transistors, amplifies the dc output and allows it to drive a npn transistor referenced to ground. This type of circuit may also be used as a tone detector or to sense that the PLL is locked to an incoming signal.

The 562 phase locked loop is especially designed for utilizing the output of the VCO. In this configuration, an amplifier-buffer has been added to the VCO to provide differential square wave outputs with a 4.5V amplitude (see block diagram Figure 8—25). This facilitates the utilization of the frequency stabilized VCO as a timing or clocking signal. The outputs (pins 3 and 4) are emitter-followers and have no internal load resistors; therefore, external 3K to 12K Ω load resistors are required.

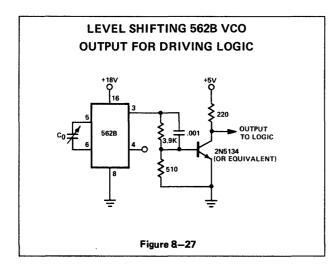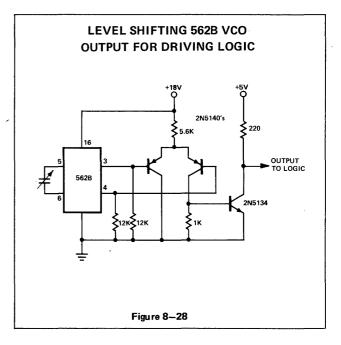### BLOCK DIAGRAM OF 562B

Figure 8—25

It is essential that the resistance from each pin to ground be equal in order to maintain output waveform symmetry and to minimize frequency drift. When locking the VCO output to the phase comparator (pins 3 to 2 for single-ended connection), capacitive coupling should be used. If a signal exceeding 2V is to be applied, a 1K Ω resistor should be placed in series with the coupling capacitor. This resistor may be part of the load resistance of 12K Ω, by using two resistors (1K and 11K) to form the VCO load, as shown in Figure 8—26.

ATTENUATING INPUT TO 562B PHASE DETECTOR

Figure 8—26

The output from the VCO is a minimum of 3V peak-to-peak, but has an average level of 12V dc; that is, it oscillates from 10.5 to 13.5V. To utilize this output with logic circuits, some means of voltage level shifting must be used. Figures 8—27 and 8—28 show two methods of accomplishing level shifting. These circuits will operate satisfactorily to 20MHz.

The phase comparator inputs of the 562B (pins 2 and 15) must be biased by connecting a 1K Ω resistor from each pin to the 8V bias supply available at pin 1. Pin 1 should be capacitively bypassed to ground. The inputs to the phase comparator should be capacitively coupled.

LEVEL SHIFTING 562B VCO
OUTPUT FOR DRIVING LOGIC

Figure 8—27

LEVEL SHIFTING 562B VCO
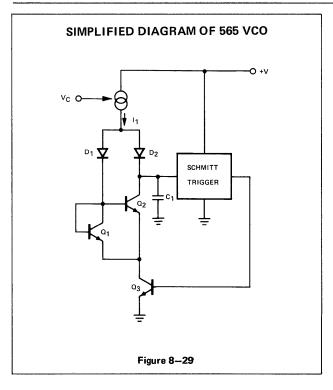OUTPUT FOR DRIVING LOGIC

Figure 8—28

DETAILED DESCRIPTION OF 565

The 565 is a general purpose PLL designed to operate at frequencies below 1MHz. Functionally, the circuit is similar to the 562 in that the loop is broken between the VCO and phase comparator to allow the insertion of a counter for frequency multiplication applications. With the 565, it is also possible to break the loop between the output of the phase comparator and the control terminal of the VCO to allow additional stages of gain or filtering. This is described later in this section.
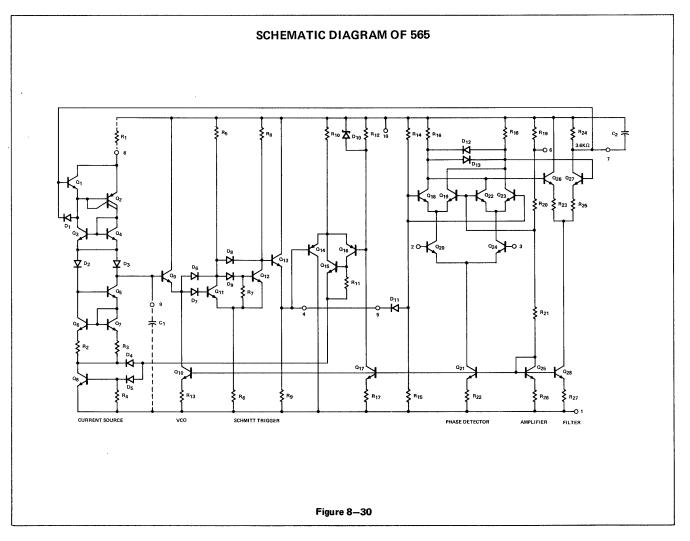
The VCO is made up of a precision current source and a non-saturating Schmitt trigger. In operation, the current source alternately charges and discharges an external timing capacitor between two switching levels of the Schmitt trigger, which in turn controls the direction of current generated by the current source.

A simplified diagram of the VCO is shown in Figure 8—29. I_1 is the charging current created by the application of the control voltage V_c. In the initial state, Q_3 is off and the current I_1 charges capacitor C_1 through the diode D_2. When the voltage on C_1 reaches the upper triggering threshold, the Schmitt trigger changes state and activates the transistor Q_3. This provides a current sink and essentially grounds the emitters of Q_1 and Q_2 to become reverse biased. The charging current I_1 now flows through D_1, Q_1 and Q_3 to ground. Since the base-emitter voltage of Q_2 is the same as that of Q_1, an equal current flows through Q_2. This discharges the capacitor C_1 until the lower triggering threshold is reached at which point the cycle repeats itself. Because the capacitor C_1 is charged and discharged with the constant current I_1, the VCO produces a triangle wave form as well as the square wave output of the Schmitt trigger.

SIMPLIFIED DIAGRAM OF 565 VCO

Figure 8–29

The actual circuit is shown in Figure 8–30. Transistors Q_1–Q_7 and diodes D_1–D_3 form the precision current source. The base of Q_1 is the control voltage input to the VCO. This voltage is transferred to pin 8 where it is applied across the external resistor R_1. This develops a current through R_1 which enters pin 8 and becomes the charging current for the VCO. With the exception of the negligible Q_1 base current, all the current that enters pin 8, appears at the anodes of diodes D_2 and D_3. When Q_8 (controlled by the Schmitt trigger) is on, D_3 is reverse biased and all the current flows through D_2 to the duplicating current source Q_5–Q_7, R_2–R_3 and appears as the capacitor discharge current at the collector of Q_5. When Q_8 is off, the duplicating current source Q_5–Q_7, R_2–R_3 floats and the charging current passes through D_3 to charge C_1.

The Schmitt trigger (Q_{11}, Q_{12}) is driven from the capacitor triangle wave form by the emitter follower Q_9. Diodes D_6–D_9 prevent saturation of Q_{11} and Q_{12}, enhancing the switching speed. The Schmitt trigger output is buffered by emitter follower Q_{13} and is brought out to pin 4, and is also connected back to the current source by the differential amplifier (Q_{14}–Q_{16}).

SCHEMATIC DIAGRAM OF 565

Figure 8–30

When operated from dual symmetrical supplies, the square wave on pin 4 will swing between a low level of slightly (0.2V) below ground to a high level of one diode voltage drop (0.7V) below positive supply. The triangle wave form on pin 9 is approximately centered between positive and negative supply and has an amplitude of 2V with supply voltages of ±5V. The amplitude of the triangle waveform is directly proportional to the supply voltages.

The phase detector is again of the doubly-balanced modulator type. Transistors Q_{20} and Q_{24} form the signal input stage, and must be biased externally. If dual symmetrical supplies are used, it is simplest to bias Q_{20} and Q_{24} through external resistors to ground. The switching stage Q_{18}, Q_{19}, Q_{22} and Q_{23} is driven from the Schmitt trigger via pin 5 and D_{11}. Diodes D_{12} and D_{13} limit the phase detector output, and differential amplifier Q_{26} and Q_{27} provides increased loop gain.

The loop low pass filter is formed with an external capacitor (connected to pin 7) and the collector resistance R_{24} (typically 3.6Ω). The voltage on pin 7 becomes the error voltage which is then connected back to the control voltage terminal of the VCO (base of Q_1). Pin 6 is connected to a tap on the bias resistor string and provides a reference voltage which is nominally equal to the output voltage on pin 7. This allows differential stages to be both biased and driven by connecting them to pins 6 and 7.

The free-running center frequency of the 565 is adjusted by means of R_1 and C_1 and is given approximately by

$$f_o \simeq \frac{1.2}{4R_1C_1}$$

When the phase comparator is in the limiting mode (Vin ≥ 200mV p-p), the lock range can be calculated from the expression:

$$2\omega_L = 2K_oK_dA\theta_d$$

where K_o is the VCO conversion gain, K_d is the phase detector gain factor, A is the amplifier gain and θ_d is the maximum phase error over which the loop can remain in lock.

For the 565: $K_o = \dfrac{50f_o}{V_{cc}}$ radians/sec/volt

(where f_o is the free-running frequency of the VCO and V_{cc} is the total supply voltage applied to the circuit.)

$$K_d = \frac{1.4}{\pi} \text{ volts/radian}$$

$$A = 1.4$$

$$\theta_d = \frac{\pi}{2} \text{ radians}$$

The lock range for the 565 then becomes:

$$f_L \cong \frac{\omega_L}{2\pi} \cong \frac{8f_o}{V_{cc}} \text{ Hz}.$$

to each side of the center frequency, or a total range of:

$$2f_L \cong \frac{16f_o}{V_{cc}} \text{ Hz}$$

The capture range, over which the loop can acquire lock with the input signal is given approximately by:

$$2\omega_c \cong 2\sqrt{\frac{\omega_L}{\tau}}$$

where ω_L is the one-sided lock range

$$\omega_L = 2\pi f_L$$

and τ is the time constant of the loop filter

$$\tau = RC_2$$

with R = 3.6kΩ.

This can be written as:

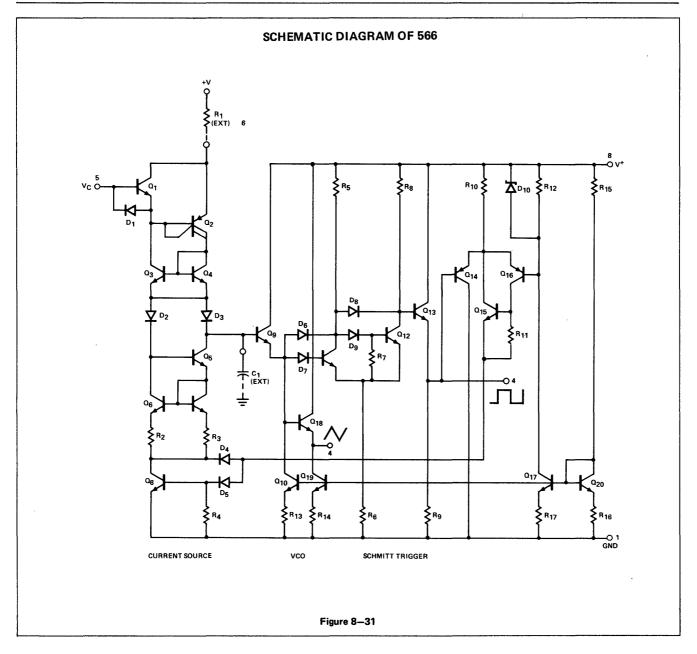$$f_c \cong \pm \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}} = \pm \frac{1}{2\pi}\sqrt{\frac{32\pi f_o}{V_{cc}}}$$

to each side of the center frequency or a total capture range of:

$$f_c \cong \frac{1}{\pi}\sqrt{\frac{32\pi f_o}{\tau V_{cc}}}$$

This approximation works well for narrow capture ranges ($f_c = 1/3f_L$) but becomes too large as the limiting case is approached ($f_c = f_L$).

DETAILED DESCRIPTION OF 566

The 566 is the voltage controlled oscillator portion of the 565. The basic die is the same as that of the 565; modified metalization is used to bring out only the VCO. The 566 circuit diagram is shown in Figure 8—31. Transistor Q_{18} has been a buffered triangle waveform output. (The triangle waveform is available at capacitor C_1 also, but any current drawn from pin 7 will alter the duty cycle and frequency.) The square wave output is available from Q_{19} by pin 4. The circuit will operate at frequencies up to 1MHz and may be programmed by the voltage applied on the control terminal (pin 5), current injected into pin 6 or the value of the external resistor and capacitor (R_1 and C_1).

SCHEMATIC DIAGRAM OF 566
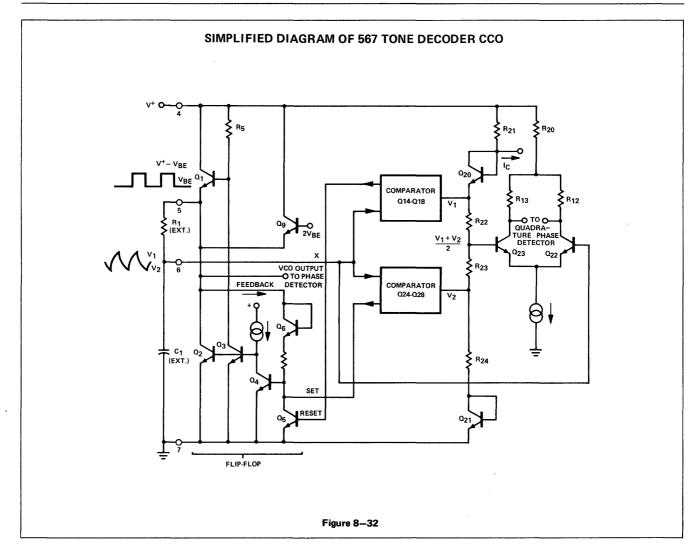

Figure 8—31

DETAILED DESCRIPTION OF 567

The 567 is a PLL designed specifically for frequency sensing or tone decoding. Like the 561, the 567 has a controlled oscillator, a phase detector and a second auxiliary or quadrature phase detector. In addition, however, it contains a power output stage which is driven directly by the quadrature phase detector output. During lock, the quadrature phase detector drives the output stage on, so the device functions as a tone decoder or frequency relay. The tone decoder center frequency and bandwidth are specified by the center frequency and capture range of the loop portion. Since a tone decoder, by definition, responds to a stable frequency, the lock or tracking range is relatively unimportant except as it limits the maximum attainable capture range.

The current controlled oscillator is shown in simplified form in Figure 8—32. It provides both a square wave output and a quadrature output. The control current I_c sweeps the oscillator ±7% of the center frequency, which is set by external components R_1 and C_1. It operates as follows:

Transistors Q_1 through Q_6 form a flip-flop which can switch pin 5 between V_{be} and $V^+ - V_{be}$. Thus, the $R_1 C_1$ network is driven from a square wave of $V^+ - 2V_{be}$ peak-to-peak volts. On the positive portion of the square wave, C_1 is charged through R_1 until V_1 is reached. A comparator circuit driven from C_1 at pin 6 then supplies a pulse which resets the flip-flop so that pin 5 switches to V_{be} and C_1 is discharged until V_2 is reached. A second comparator then supplies a pulse which sets the flip-flop and C_1 resumes charging.

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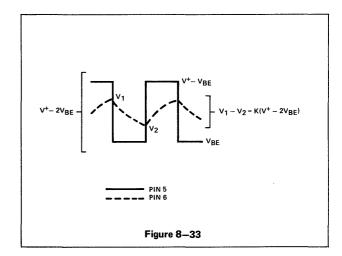## SIMPLIFIED DIAGRAM OF 567 TONE DECODER CCO

Figure 8—32

The total swing of the capacitor voltage, as determined by the comparator sensing voltages, is

$$V_1 - V_2 = (V^+ - 2V_{be}) \frac{R_{22} + R_{23}}{R_{21} + R_{22} + R_{23} + R_{24}}$$

$$= K (V^+ - 2V_{be})$$

Due to the excellent matching of integrated resistors, the resistor ratio K may be considered constant. Figure 8—33 shows the pin 5 and pin 6 voltages during operation. It is obvious from the proportion that $t_1 + t_2$ is independent of the magnitude of V^+ and dependent only on the time constant R_1C_1 of the external components. Moreover, if $(V_1 + V_2)/2 = V^+/2$, then $t_1 = t_2$ and the duty cycle is 50%. Note that the triangular waveform is phase shifted from the square wave. A differential stage (Q_{22} and Q_{23}) amplifies the triangular wave with respect to $(V_1 + V_2)/2$ to provide the quadrature output. (Due to the exponential distortion of the triangle wave, the quadrature output is actually phase shifted about $80°$, but no operating compromises result from this slight deviation from true quadrature.)
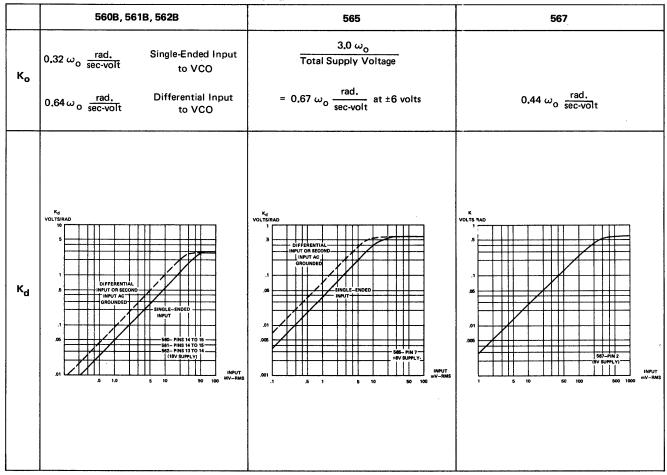

Figure 8—33

One source of error in this oscillator scheme is current drawn by the comparators from the R_1C_1 mode. An emitter follower, therefore, is inserted at X to minimize this drain and Q_{21} placed in series with Q_{20} to drop the comparator sensing voltage one V_{be} to compensate for the V_{be} drop in the emitter follower.

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LOOP GAIN CONSTANTS (K_o, K_d)

Table 8—4 gives the gain constants (K_o, K_d) for the Signetics' loops. The values given are for the standard connection with no gain reduction or tracking adjustment components connected. The dc amplifier gain A has been included in either the K_o or K_d value, depending on which side of the low pass filter terminals the gain is present. This causes no hardship in calculations since the loop gain K_v becomes simply $K_o K_d$.

PLL GAIN CONSTANTS* $K_o K_d$ ($K_v = K_o K_d$)

	560B, 561B, 562B	565	567
K_o	$0.32\,\omega_o\,\dfrac{rad.}{sec\text{-}volt}$ Single-Ended Input to VCO $0.64\,\omega_o\,\dfrac{rad.}{sec\text{-}volt}$ Differential Input to VCO	$\dfrac{3.0\,\omega_o}{Total\ Supply\ Voltage}$ $= 0.67\,\omega_o\,\dfrac{rad.}{sec\text{-}volt}$ at ±6 volts	$0.44\,\omega_o\,\dfrac{rad.}{sec\text{-}volt}$
K_d			

*The dc amplifier gain A has been included in K_o or K_d, depending on which side of the LPF terminals the amplifier is located.
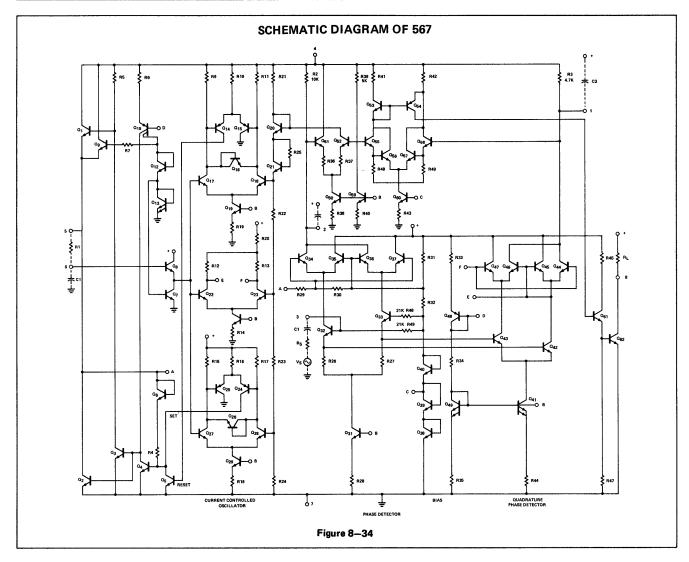
Table 8—4

In order to insure that the square wave drops quickly and accurately to V_{be}, an active clamp scheme is applied to the collector of Q_2. The base of Q_9 is held at $2\,V_{be}$ so that as Q_2 is turned on by its base current, its collector is held at V_{be}. Because Q_2 and Q_3 have the same geometry and their base-emitter voltages are the same, the maximum Q_2 current when clamped is essentially the same as the collector current of Q_3 (as limited by R_5). The flip-flop was optimized for maximum switching speed to reduce frequency drift due to switching speed variations.

Current control of the frequency is achieved by making

R_{21} somewhat less than R_{24} and restoring the proper voltage for 50% duty cycle by drawing I_c of 100μA for the R_{21}, Q_{20} junction. When I_c is then varied between 0 and 200μA, the frequency changes by ±7%. Because of the slight shift in the voltage levels V_1 and V_2 with I_c, the square wave duty cycle changes from about 47% to about 53% over the control range. To avoid drift of center frequency with temperature and supply voltage changes when $I_c \neq 0$, I_c is also made a function of $V^+ - 2V_{be}$.

The CCO circuit is shown in the tone decoder schematic diagram, Figure 8—34.

SCHEMATIC DIAGRAM OF 567

Figure 8—34

A doubly-balanced multiplier formed by Q_{32} through Q_{37} (Figure 8—34) functions as the phase detector. The input signal is applied to the base of Q_{32}. Transistors $Q_{34} - Q_{37}$ are driven by a square wave taken from the CCO at the collector of Q_2. Phase detector input bias is provided by three diodes, Q_{38} through Q_{40}, connected in series, assuring good bias voltage matching from run to run. Emitter resistors R_{26} and R_{27}, in addition to providing the necessary dynamic range at the input, help stabilize the gain over the wide temperature range.

The loop dc amplifier is formed by Q_{51} and Q_{52}. Having a current gain of 8, it permits even a small phase detector output to drive the CCO the full ±7%. Therefore, full detection bandwidth can be obtained for any in-band input signal greater than about 70mV rms. However, the main purpose of high loop gain in the tone decoder is to keep the locked phase as close to $\pi/2$ as possible for all but the smallest input levels since this greatly facilitates operation of the quadrature lock detector. Emitter resistors R_{36} and R_{37} help stabilize the gain over the required temperature range. Another function of the dc amplifier is to allow a higher impedance level at the low pass filter terminal

(pin 2) so that a smaller capacitor can be used for a given loop cutoff frequency. Once again, emitter resistors help stabilize the loop gain over the temperature range.

The quadrature phase detector (QPD), formed by a second doubly-balanced multiplier $Q_{42} - Q_{47}$, is driven from the quadrature output (E, F, in Figure 8—34) of the CCO. The signal input comes from the emitters of the input transistors Q_{32} and Q_{33}.

The output stage, Q_{53} through Q_{62}, compares the average QPD current in the low pass output filter R_3C_3 with a temperature compensated current in R_{39} (forming the threshold voltage V_t).

Since R_3 is slightly lower in value than R_{39}, the output stage is normally off. When the lock and the QPD current I_q occurs, pin 1 voltage drops below the threshold voltage V_t and the output stage is energized.

The uncommitted collector (pin 8) of the power npn output transistor can drive both 100 − 200mA loads and logic elements, including TTL.

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EXPANDING LOOP CAPABILITY

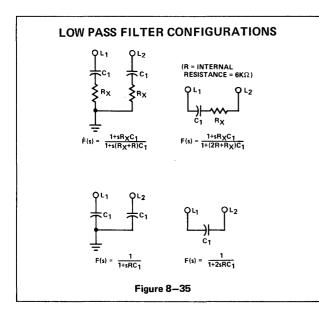### LOW PASS FILTER CIRCUITS (560B, 561B and 562B)

The low pass filters used with the 560B, 561B and 562B are externally adjusted to provide the desired operational characteristics. To select the most appropriate type of filter and component values, a basic understanding of filter operation is required.

A FM signal to be demodulated is matched in the phase comparator with the voltage controlled oscillator signal, which is tuned to the FM center frequency. Any resulting phase difference between these two signals is the demodulated FM signal. This demodulated signal is normally at frequencies between dc and upper audio frequencies.

The choice of low pass filter response gives a degree of design freedom in determining the capture range or selectivity of the loop. The attenuation of the high frequency error components at the output of the phase detector enhances the interference rejection characteristics of the loop. The filter also provides a short-term memory for the PLL that ensures rapid recapture of the signal if the system is thrown out of lock due to a noise transient.

To ensure absolute closed loop stability at all signal levels within the dynamic range of the loop, the open loop PLL is required to have no more than 12dB per octave high frequency roll-off.

The capacitor in each filter circuit shown in Figure 8–35 will provide 6dB per octave roll-off at the first break point—the desired bandwidth frequency. The resistance Rx shown in filters (c) and (d) is used to break the response up at high frequencies to ensure 6dB per octave roll-off at the loop unity gain frequency. Rx is typically between 50 and 200Ω.

LOW PASS FILTER CONFIGURATIONS

$$F(s) = \frac{1+sR_xC_1}{1+s(R_x+R)C_1}$$

$$F(s) = \frac{1+sR_xC_1}{1+(2R+R_x)C_1}$$

$$F(s) = \frac{1}{1+sRC_1}$$

$$F(s) = \frac{1}{1+2sRC_1}$$

(R = INTERNAL RESISTANCE = 6KΩ)

Figure 8–35

Calculation of values for low pass filters shown can be made using the complex second-degree transfer function equations given, or approximated using the equation:

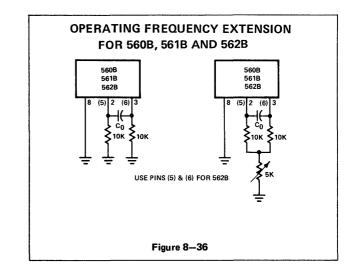$$C_1 = \frac{2660}{f} \text{ mfd for filters (a) and (c), and the equation:}$$

$$C_1 = \frac{1330}{f} \text{ mfd for filters (b) and (d) where f is the desired}$$

first break frequency in Hz.

At frequencies greater than 5MHz where the loop may be prone to instability, filters (a) and (c) should be used. For operation at low frequencies, a simple type (b) lag filter with no added resistance is usually sufficient.
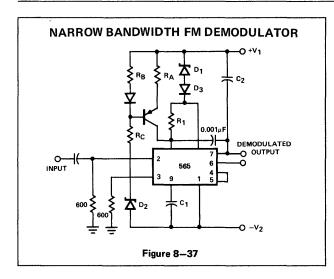
OPERATING FREQUENCY EXTENSION TO 60MHz (560B, 561B, 562B)

The frequency range of the 560B, 561B and 562B phase locked loops may be extended to 60MHz by the addition of two 10K Ω resistors from the timing capacitor terminals to the negative power supply as shown in Figure 8–36. The inclusion of a 5K Ω potentiometer between these 10K Ω resistors and the negative supply provides a simple method of fine tuning.

OPERATING FREQUENCY EXTENSION FOR 560B, 561B AND 562B

USE PINS (5) & (6) FOR 562B

Figure 8–36

INCREASED LOOP OUTPUT VOLTAGE FOR SMALL FREQUENCY DEVIATIONS (565)

For applications where both a narrow lock range and a large output voltage swing are required, it is necessary to inject a constant current into pin 8 and increase the value of R_1. One scheme for this is shown in Figure 8–37. The basis for this scheme is the fact that the output voltage controls only the current through R_1 while the current through Q_1 remains constant. Thus, if most of the charging current is due to Q_1, the total current can be varied only a small amount due to the small change in current through R_1. Consequently, the VCO can track the input signal over a small frequency range yet the output voltage of the loop (control voltage of the VCO) will swing its maximum value.

NARROW BANDWIDTH FM DEMODULATOR

Figure 8—37

Diode D_1 is a Zener diode, used to allow a larger voltage drop across R_A than would otherwise be available. D_4 is a diode which should be matched to the emitter-base junction of Q_1 for temperature stability. In addition, D_1 and D_2 should have the same breakdown voltages and D_3 and D_4 should be similar so that the voltage seen across R_B and R_C is the same as that seen across pins 10 and 1 of the phase locked loop. This causes the frequency of the loop to be insensitive to power supply variations. The center frequency can be found by:

$$f_o \simeq \frac{2R_B}{(R_B + R_C)\, R_A C_1} + \frac{1}{4R_1 C_1}\ \text{Hz}$$

and the total lock range is given by:

$$2\Delta f_L \simeq \frac{22.4 V_D (R_B + R_C) R_A f_o}{(|V_1| + |V_2| - V_z - V_D)(8R_B R_1 + R_A[R_B + R_C])}\ \text{Hz}$$

where: V_D = forward biased diode voltage $\simeq 0.7V$
V_z = Zener diode breakdown voltage
V_1 = positive supply voltage
V_2 = negative supply voltage
f_o = free-running VCO center frequency

When the output excursion at pin 7 need be only a volt or so, diodes D_1, D_2 and D_3 may be replaced by short circuits.

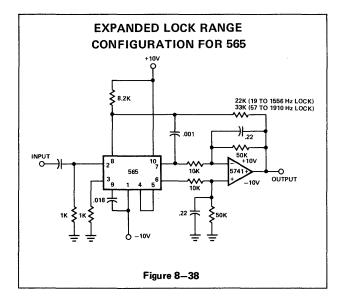The value of R_1 can be selected to give a prescribed output voltage for a given frequency deviation.

$$R_1 = \frac{R_A (R_B + R_C)\, f_o}{R_B (|V_1| + |V_2| - 0.7)\, \Delta f}$$

where f_o is the center frequency and Δf is the desired frequency deviation per volt of output.

In most instances, R_B and R_A are chosen to be equal so that the voltage drop across them is about 200mV. For best temperature stability, diode D_1 should be a base-collector shorted transistor of the same type as Q_1.
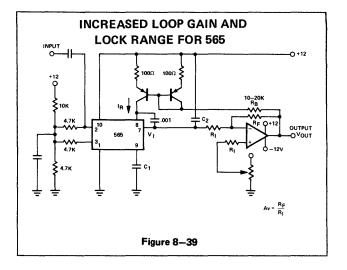
EXPANDED LOCK RANGE (565)

When the 565 is connected normally, feedback to the VCO from the phase detector is internal. That is, an amplifier makes the pin 8 voltage track the pin 7 (phase detector output) voltage. Since the capacitor C_1 charge current is determined by the current through resistance R_1, the frequency is a function of the voltage at pin 8. It is possible, however, to bypass and swamp the internal loop amplifier so that the current into pin 8 is no longer a function of the pin 8 voltage but only of the pin 7 voltage. This makes a greater charge-discharge current variation possible, allowing a greater lock range. Figure 8—38 shows such a circuit in which the 5741 operational amplifier is set for a differential gain of 5, feeding current to pin 8 through the 33K resistor (simulating a current source). Not only is the tracking range greatly expanded, but the output voltage as a function of frequency is five times greater than normal. In setting up such a circuit, the user should keep in mind that for best frequency stability, the charge-discharge current should be in the range of 50 to 1500μA which also specifies the pin 8 input current range, showing that a ratio of upper to lower lock extremes of about 30 can be achieved.

EXPANDED LOCK RANGE CONFIGURATION FOR 565

Figure 8—38

BREAKING THE INTERNAL FEEDBACK LOOP (565)

Many times it would be advantageous to be able to break the feedback connection between the output (pin 7) and the control voltage terminal (Q_1) of the VCO. This can be easily done once it is seen that it is the *current* into pin 8 which controls the VCO frequency. If the external resistor R_1 is replaced with a current source, such as in Figure 8—39, we have effectively broken the internal voltage feedback connection. The current flowing into pin 8 is now independent of the voltage on pin 8. The output voltage (on pin 7) can now be amplified or filtered and used to drive the current source by a scheme such as that shown in Figure 8—39. This scheme allows the addition of enough

gain for the loop to stay in lock over a 100:1 frequency range, or conversely, to stay in lock with a precise phase difference (between input and VCO signals) which is almost independent of frequency variation. Adjustment of the voltage to the non-inverting input of the op amp, together with a large enough loop gain allows the phase difference to be set at a constant value between 0° and 180°. In addition, it is now possible to do special filtering to improve the performance in certain applications. For instance, in frequency multiplication applications it may be desirable to include a notch filter tuned to the sum frequency component to minimize incidental FM without excessive reduction of capture range.

INCREASED LOOP GAIN AND LOCK RANGE FOR 565
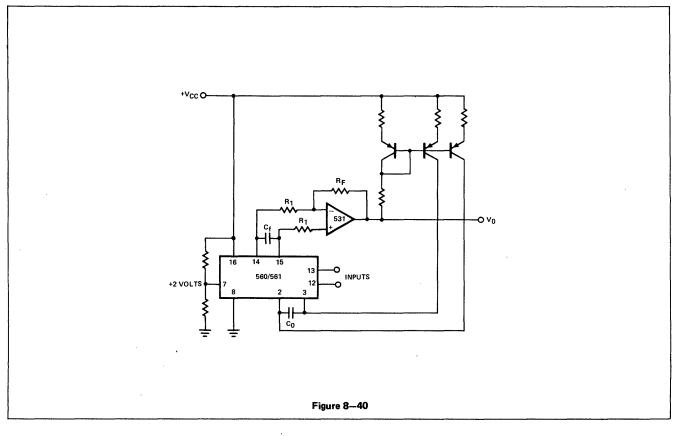
Figure 8—39

BREAKING THE INTERNAL FEEDBACK LOOP (560, 561, 562)

The internal control voltage feedback loop can also be easily broken on the 560, 561 and 562. The key in this case is to bias the range control terminal (pin 7) to +2V which turns off the controlled current source. Now the phase comparator output voltage will have no effect on the charging current which sets the VCO frequency. Now an external feedback loop can be built with the desired transfer function. Figure 8—40 shows a practical application of this principle. The control voltage is taken from across the low pass filter terminals, amplified, and used to add or subtract current into the timing capacitor nodes.
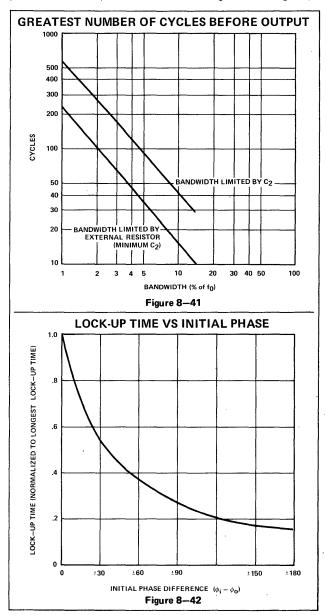
MINIMIZING TONE DECODER RESPONSE TIME (567)

The 567 Tone Decoder is a specialized loop which can be set up to respond to a given tone (constant frequency) within its bandwidth. The center frequency is set by a resistor R_1 and capacitor C_1 which determine the free-running frequency. The bandwidth is controlled by the low pass filter capacitor C_2. A third capacitor C_3 integrates the output of the quadrature phase detector (QPD) so that the dc lock-indicating component can switch the power output stage on when lock is present. The 567 is optimized for stability and predictability of center frequency and bandwidth.
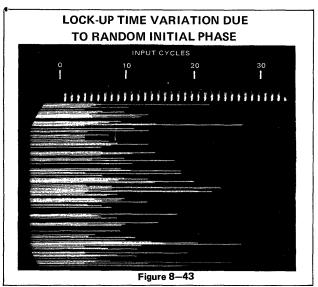

Figure 8—40

Two events must occur before an output is given. First, the loop portion of the 567 must achieve lock. Second, the output capacitor C_3 must charge sufficiently to activate the output stage. For minimum response time, these events must be as brief as possible.

As previously discussed, the lock time of a loop can be minimized by reducing the response time of the low pass filter. Thus, C_2 must be as small as possible. However, C_2 also controls the bandwidth. Therefore, the response time is an inverse function of bandwidth as shown by Figure 8—41, reprinted from the 567 data sheet. The upper curve denotes the expected worst-case response time when the bandwidth is controlled solely by C_2 and the input amplitude is 200mV rms or greater. The response time is given in cycles of center frequency. For example, a 2% bandwidth at a center frequency of 1000 cycles can require as long as 280 cycles (280ms) to lock when the initial phase relationship is at its worst. Figure 8—42 gives a

typical distribution of response time versus input phase. Note that, assuming random initial input phase, only 30/180 = 1/6 of the time will the lock-up time be longer than half the worst case lock-up time. Figure 8—43 shows some actual measurements of lock-up time for a set-up having a worst case lock-up time of 27 cycles and a best-case lock-up time of four input cycles.

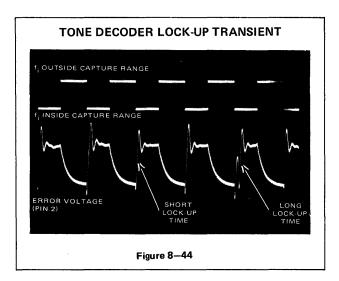**LOCK-UP TIME VARIATION DUE TO RANDOM INITIAL PHASE**

Figure 8—43

The lower curve on the graph shows the worst-case lock-up time when the loop gain is reduced as a means of reducing the bandwidth (see data sheet, Alternate Method of Bandwidth Reduction). The value of C_2 required for this minimum response time is
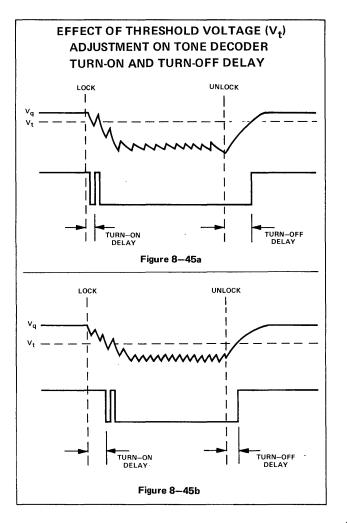
$$C_2' = \frac{130}{f_o}\left[\frac{10K + R_A}{R_A}\right]\ \mu F$$

It is important to note that noise immunity and rejection of out-band tones suffer somewhat when this minimum value (C_2') of C_2 is used so that response time is gained at their expense. Except at very low input levels, input amplitude has only a minor effect on the lock-up time—usually negligible in comparison to the variation caused by input phase.

Lock-up transients can be displayed on a two-channel scope with ease. Figure 8—44 shows the display which results. The top trace shows the square wave which either gates the input generator signal off and on (or shifts the frequency in and out of the band if you have a generator which has a frequency control input only). The lower trace shows the voltage at pin 2, the low pass filter voltage. The input frequency is offset slightly from the center frequency so that the locked and unlocked voltage are different. It is apparent that, while the C_2 decay during unlock is always the same, the lock transient is different each time. This is because the turn-on repetition rate is such that a different initial phase relationship occurs with each appearance of the in-band signal. It is tempting to adjust the repetition rate so that a fast, constant lock-up transient is displayed. However, in doing a favorable initial phase is created that is

GREATEST NUMBER OF CYCLES BEFORE OUTPUT

BANDWIDTH LIMITED BY C_2

BANDWIDTH LIMITED BY EXTERNAL RESISTOR (MINIMUM C_2)

CYCLES

BANDWIDTH (% of f_0)

Figure 8—41

LOCK-UP TIME VS INITIAL PHASE

LOCK-UP TIME (NORMALIZED TO LONGEST LOCK-UP TIME)

INITIAL PHASE DIFFERENCE $(\phi_i - \phi_o)$

Figure 8—42

not present in actual operation. On the contrary, it is most realistic to adjust the repetition rate so that the longest lock-up time is displayed, such as the fifth lock transient shows. Once this display is achieved, the effect of various adjustments in C_2 or input amplitude is seen. However, *the repetition rate must be readjusted for worst-case lock-up after each such change.*

TONE DECODER LOCK-UP TRANSIENT

f_i OUTSIDE CAPTURE RANGE

f_i INSIDE CAPTURE RANGE

ERROR VOLTAGE (PIN 2) SHORT LOCK-UP TIME LONG LOCK-UP TIME

Figure 8—44

EFFECT OF THRESHOLD VOLTAGE (V_t) ADJUSTMENT ON TONE DECODER TURN-ON AND TURN-OFF DELAY

LOCK   UNLOCK

V_q
V_t

TURN—ON DELAY   TURN—OFF DELAY

Figure 8—45a

LOCK   UNLOCK

V_q
V_t

TURN—ON DELAY   TURN—OFF DELAY

Figure 8—45b

Once lock is achieved, the quadrature phase detector output at pin 1 is integrated by C_3 to extract the dc component. As C_3 charges from its quiescent value V_q (see Figure 8—45) to its final value $(V_q - \Delta V)$, it passes through the output stage threshold, turning it on. The total voltage change is a function of input amplitude. Since the unadjusted V_q is very close (within 50mV) to V_t, the output stage turns on very soon after lock. Only a small fraction of the output stage time constant $(\tau = 4700C_3)$ expires before V_t is crossed so that C_3 does not greatly influence the response time. However, as shown in Figure 8—45a, the turn-off delay time can be quite long when C_3 is large. Figure 8—45b shows how desensitizing the output stage by connecting a high-value resistor between pin 1 and pin 4 (plus supply) can equalize the turn-on and turn-off time. If turn-off delay is important in the overall response time, then desensitizing can reduce the total delay.

But why not make C_3 very small so that these delays can be totally neglected? The problem here is that the QPD output has a large twice-center-frequency component that must be filtered out. Also, noise, outband signals and difference frequencies formed by close out-band frequencies beating with the VCO frequency appear at the QPD output. All these must be attenuated by C_3 or the output stage will chatter on and off as the threshold is approached. The more noisy the input signal and the larger the near-band signals, the greater C_3 must be to reject them. Thus, there is a complicated relationship between the input spectrum and the size of C_3. What must be done, then, is to make C_3 more than sufficient for proper operation (no false outputs or missed signals) under actual operating conditions and then reduce its value in small steps until either the required response time is obtained or operation becomes unsatisfactory.

In setting up the tone decoder for maximum speed, it is best to proceed as follows:

a.) After the center frequency has been set, adjust C_2 to give the desired bandwidth or, if the graph of response time in cycles (Figure 8—43) suggests that worst case lock-up time will be too long, incorporate the loop gain reduction scheme as an alternate means of bandwidth reduction. (Page 8 of 567 data sheet.)

b.) Check lock-up time by observing the waveform at pin 2 while pulsing the input signal on and off (or in and out of the band when a FM generator is used). Adjust repetition rate to reveal worst lock-up time.

c.) Starting with a large value of C_3 (say 10 C_2), reduce it as much as possible in steps while monitoring the output to be certain that no false outputs or missed signals occur. The full input spectrum should be used for this test. Ignore brief transients or chatter during turn-on and turn-off as they can be eliminated with the chatter prevention feedback technique described in the data sheet.

d.) Use the desensitizing technique, also described in the data sheet, to balance turn-on and turn-off delay.

e.) Apply the chatter prevention technique to clean up the output.

If this procedure results in a worst-case response time that is too slow, the following suggestions may be considered:

a.) Relax the bandwidth requirement.

b.) Operate the entire system at higher frequency when this option is available.

c.) Use two tone decoders operating at slightly different frequencies and OR the outputs. This will reduce the statistical occurance of the worst-case lock-up time so that excessive lock-up time occurs. For example, if the lock-up time is marginal 10% of the time with one unit, it will drop to 1% with two units.

d.) Control the in-band input amplitude to stabilize the bandwidth, set up two tone decoders for maximum bandwidth and overlap the detection bands to make the desired frequency range equal to the overlap. Since both tone decoders are on only when a tone appears within the overlap range, the outputs can be ANDed to provide the desired selectivity.

e.) If the system design permits, send the tone to be detected continuously at a low level (say 25mV rms) to keep the loop in lock at all times. The output stage, slightly desensitized, can then be gated on as required by increasing signal the amplitude during the on time. Naturally, the signal phase should be maintained as the amplitude is changed. This scheme is extremely fast, allowing repetition rates as fast as 1/3 to 1/2 the center frequency when C_3 is small. This is equivalent to ASK (amplitude shift keying).

SECTION 4

SPECIFIC APPLICATIONS
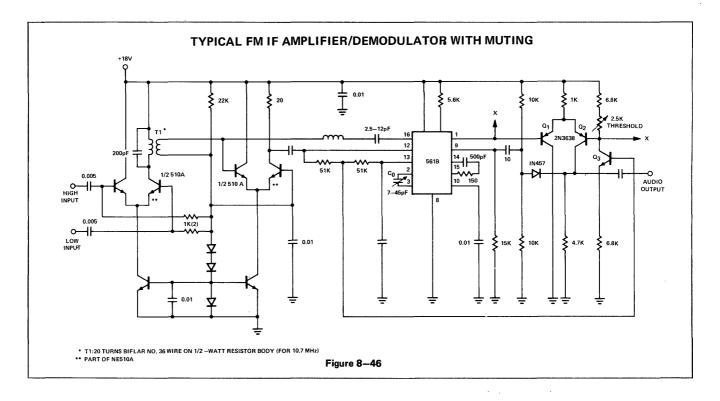
FM IF AMPLIFIER/DEMODULATOR WITH MUTING (561B)

In this application, the loop portion of the 561B operates in the usual manner for FM demodulation. To introduce muting (squelch) the synchronous AM detector portion of the PLL is used to detect the presence of an input signal and to open a muting gate. Figure 8—46 shows a typical circuit incorporating the muting feature.

The input section of the circuit is a broad-band, amplifier-limiter. The tuned LC network at the AM input, pin 4, is adjusted to provide a 90^0 phase shift at the IF frequency. This network is adjusted for maximum output at pin 1, demodulated AM output, with a carrier applied at the IF frequency.

Three transistors at the right of the diagram (Q_1, Q_2 and Q_3) and the 1N457 diode form the muting gate. Gating is accomplished by applying the demodulated FM output through the 1N457 diode and by biasing the diode on and off as follows: During periods with no input applied, Q_1 is shut off and Q_2 continues. Therefore, the diode is effectively back biased since its anode potential developed by the two 10K resistors across the power supply is approximately +13.5V. When an input is applied to the circuit, Q_1 is turned on and Q_2 shuts off, reducing its collector potential below 9V. Thus, the diode is forward biased and the demodulated IF output is gated through to the circuit output.

Muting threshold adjustment is accomplished using the 2.5K potentiometer. Transistor Q_3 is used as a bias generator for the differential pair, Q_1 and Q_2. In turn, the bias of Q_3 is obtained from internal PLL bias points at pins 12 and 13. Thus, the muting gate will track the PLL over wide temperature variations.

TYPICAL FM IF AMPLIFIER/DEMODULATOR WITH MUTING

* T1: 20 TURNS BIFLAR NO. 36 WIRE ON 1/2 —WATT RESISTOR BODY (FOR 10.7 MHz)
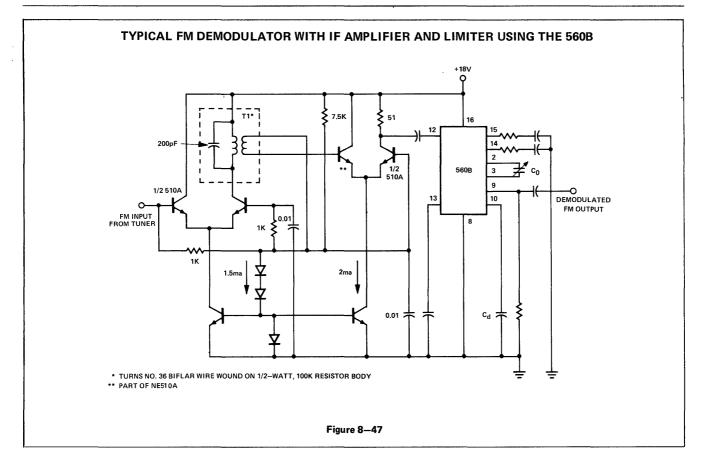** PART OF NE510A

Figure 8—46

FM DEMODULATOR (560B)

When used as a FM demodulator, the 560B phase locked loop requires selection of external components and/or circuits to create the desired response. The areas to be considered are:

    a.)   Input Signal Conditioning
    b.)   Tuning — VCO Frequency
    c.)   Low Pass Filter Selection/Gain Adjustment
    d.)   Output Swing
    e.)   Tracking Range Adjustment
    f.)   De-emphasis Network Selection

Figure 8—47 illustrates schematically a typical FM demodulator with IF amplifier and limiter using the 560B PLL. The amplitude of the input signal has a pronounced effect on the operation. For the tracking range to be constant, the input signal level should be greater than 2mV rms. In addition, AM rejection diminishes at higher signal levels and drops to less than 20dB for signals greater than 30mV. If either the tracking range or AM rejection is critical, the input signal should be conditioned to be in the 2 to 10mV range, using either a limiter or a combination limiter-amplifier. This circuit should limit at the smallest input voltage that is expected.

TYPICAL FM DEMODULATOR WITH IF AMPLIFIER AND LIMITER USING THE 560B

* TURNS NO. 36 BIFLAR WIRE WOUND ON 1/2—WATT, 100K RESISTOR BODY
** PART OF NE510A

Figure 8—47

The PLL is tuned by adjusting the VCO to the center frequency of the FM signal. This is accomplished by connecting a capacitor across pins 2 and 3. The capacitor value is determined using the equation $C_o \cong 300/f_o$, pF where f_o, the free-running VCO frequency, is in MHz. The exact value is not important as the internal resistors are only within ±10% of nominal value and fine tuning is normally required. Fine tuning may be accomplished by using a trimmer capacitor in parallel with C_o or by using a potentiometer connected across the power supply with the rotor connected to pin 6 through a 200Ω current limiting resistor.

The dc gain of the loop, which sets the lock range and threshold sensitivity, can be controlled by the placement of a resistance between pins 14 and 15, the low pass filter terminals. A low pass filter connected to these terminals controls the capture range or selectivity· of the loop. In basic terms, it may be said that the low pass filter sets the bandwidth of the demodulated information which will be obtained. For most applications, a single capacitor connected between pins 14 and 15 will provide the required filtering. The capacitance value required can be approximated as follows:

$$C \approx \frac{1330}{f} \text{ mfd}$$

where f is the desired bandwidth in Hz. For example, if the desired information bandwidth is 15kHz, the required low pass filter capacitance will be:

$$C \approx \frac{1330}{15000} = .09 \text{ mfd}$$

The output swing is a function of the frequency deviation of the incoming signal, and is approximately 0.3V p-p for ±1% deviation. For example, a standard 10.7MHz IF frequency has a deviation of ±75kHz; therefore, the percentage deviation equals $\frac{\pm0.75 \times 100}{10.7} = \pm0.7\%$ and the output voltage will be 0.3V p-p x $\frac{.7\%}{1\%}$ = .21V p-p, or 74mV rms for 100% modulation.
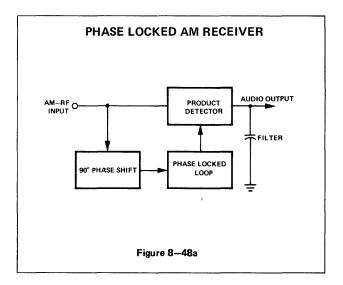
The de-emphasis network requires an external capacitor from pin 10 to ground. This capacitor C_d and the 8000Ω internal resistance should produce a time constant of approximately 75μsec for standard FM broadcast demodulation. The value of the de-emphasis capacitor for this application is determined by the following formula:

$$C_d = \frac{75 \times 10^{-6}}{8000} = 0.0094 \text{ mfd}$$

For most applications, a 0.01mfd value would be satisfactory since the manufacturing tolerance of the resistor is on the order of 20%.
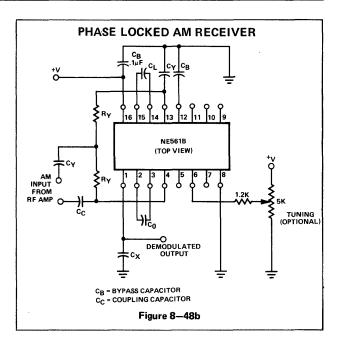
PHASE LOCKED AM RECEIVER (561B)

The Signetics 561B can be used as an AM detector/receiver. AM detection is accomplished as illustrated in the block diagram of Figure 8–48a. The phase locked loop is locked to the signal carrier frequency and its VCO output is used to provide the local oscillator signal for the product detector or synchronous demodulator. The PLL locks to its input signal with a constant 90° phase error. The amplitude of the signal at the output of the product detector is a function of the phase relationship of the carrier of the incoming signal and the local oscillator; it will be a maximum when the carrier and local oscillator are in phase or 180° out of phase and a minimum when they are in quadrature. It is, therefore, necessary to add a 90° phase shift network in the system to compensate for the normal PLL phase shift. The 561 is designed for this to be incorporated between the signal input and the input to the phase comparator input, pin 12 or pin 13.

PHASE LOCKED AM RECEIVER

Figure 8–48a

Connection as an AM detector/receiver is given in Figure 8–48b. The bypass and coupling capacitors should be selected for low impedance at the operating frequency. C_o is selected to make the VCO oscillate at the frequency to be received and C_x is selected, in conjunction with the output resistance (8000Ω) and the load resistance, to roll off the audio output for the desired bandwidth. The phase shift network may be determined from the following equations:

$$C_y = \frac{1.3 \times 10^{-4}}{f_c} \ pF$$

where f_c is the carrier frequency of the signal to be received and $R_y = 3000\Omega$. A receiver for standard AM reception is easily constructed using the circuit of Figure 8-48b. Its operating range will be from 550kHz to 1.6MHz. All by-pass and coupling capacitors are 0.1mfd. C_y is selected using a frequency which is the geometric mean of the limits of the frequencies which are to be received.

PHASE LOCKED AM RECEIVER

C_B = BYPASS CAPACITOR
C_C = COUPLING CAPACITOR

Figure 8–48b

$$f_c = \quad f_{hi}f_{lo} = \quad 1.6 \times 0.55 = .94MHz \ then:$$

$$C_y = \frac{1.3 \times 10^{-4}}{.94 \times 10^{-6}} = 135pF$$

The low pass filter for the loop, C_L, is not critical for no information is being derived directly from the loop error signal and one need only be assured of stable loop operation. A .01mfd capacitor was found to be adequate.

Tuning may be accomplished in several ways. The simplest method uses a variable capacitor as C_o. It should be trimmed so that when set for minimum capacitance, the VCO frequency is approximately 1.6MHz. The capacitance used may be obtained from the following formula: $C_o \approx \frac{300pF}{f_o}$ where f_o is in MHz.

Application of this formula shows that the minimum capacitance should be about 180pF and the maximum capacitance should be 550pF. A second tuning method utilizes the fine tuning input, pin 6. When current is inserted or removed from this pin, the VCO frequency will change, thereby tuning the receiver. Select C_o, when the current at pin 6 is zero, to make the VCO operate at the mean frequency used in the phase shift network calculation (940kHz). The complete standard AM broadcast band may now be tuned with one potentiometer. The resistor in series with the arm of the potentiometer is selected to give the desired tuning range and will be about 1200Ω when an 18V power supply is used.

For operation, this receiver requires an antenna and a good grounding system. Operation may be improved by including a broadband untuned RF amplifier, but care should be used to ensure that the phase locked loop is not overdriven, e.g. input signals should be kept less than 0.5V rms.

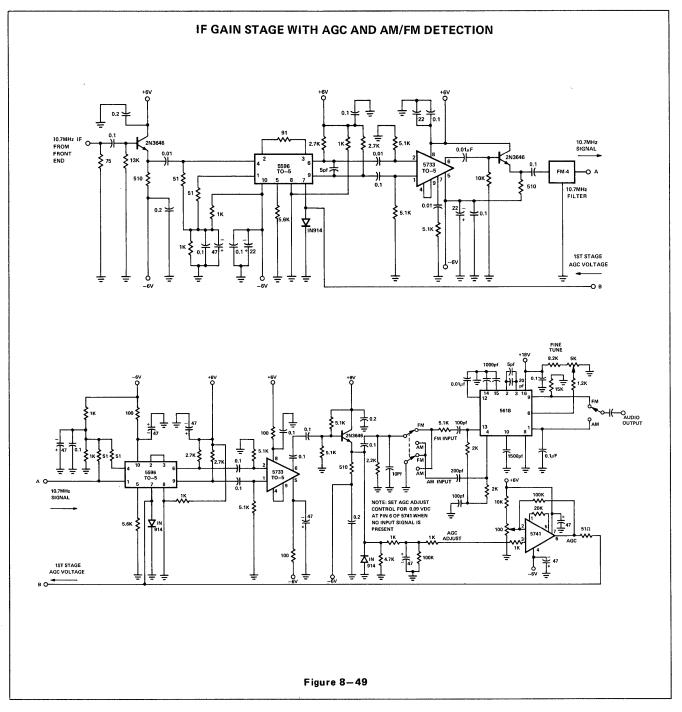## IF STAGE WITH AGC AND AM/FM DETECTION (561B)

The circuit shown in Figure 8—49 is basically an IF strip at 10.7MHz employing a buffer amplifier, two stages of gain, two ganged stages of AGC and an AGC summing amplifier. A single 561B PLL serves as both the AM and FM detector. Input sensitivity to insure lockup for either AM or FM demodulation is approximately $10\mu V$. The input level to the 561B is held level at 305mV p-p during input amplitude excursion from $10\mu V$ to 120mV p-p. Potentiometer R_{AGC} is adjusted at no input for a quiescent dc voltage (pin 6 of amplifier 5741) of —90mV. This presets the 5596

multipliers at a maximum gain condition. The gain is slowly reduced as the RF input level rises and full AGC action begins.

The bandwidth of linear demodulation of AM is 1Hz to 4.5kHz and of FM is 1Hz to 36kHz.

IF gain adjustment can be provided with the installation of a potentiometer between pins 4 and 9 of either (or both) of the 5733, a zero ohm setting insuring maximum gain.

The addition of a conventional converter front-end and audio driver stages completes the circuitry for a receiver.

IF GAIN STAGE WITH AGC AND AM/FM DETECTION

Figure 8—49

TRANSLATION LOOP FOR PRECISE FM (561B, 562B)

A translation loop mixes the output of two oscillators and produces a signal whose frequency is equal to the sum or difference of the two. In the most useful application of this circuit, one oscillator is a precise crystal-controlled oscillator and the second is a low frequency voltage-controlled oscillator so that the loop output is a FM signal whose center frequency is slightly offset from the crystal oscillator frequency. Since the offset oscillator supplies only a small percentage of the final output frequency, it need not be as precise as the crystal oscillator.

Such a loop is shown in Figure 8—50a. The VCO is driven until the filtered low frequency component of the PD2 output is equal to the offset frequency f_m. When this occurs, lockup is achieved and the VCO output is either $f_R + f_m$ or $f_R - f_m$. By adjusting the VCO free-running slightly above f_m, the latter case can be eliminated. If f_m is frequency modulated, then the output will also be frequency modulated since it has the same absolute deviation.
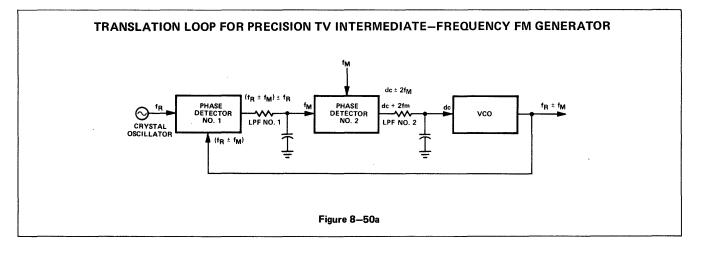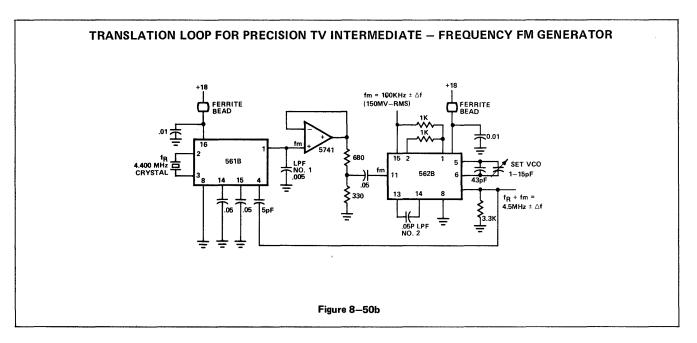

TRANSLATION LOOP FOR PRECISION TV INTERMEDIATE—FREQUENCY FM GENERATOR

Figure 8—50a

Figure 8—50b shows a translation loop made from a 561B and 562B. It is designed to produce a 4.5MHz signal with a deviation of ±25kHz. The 561B serves as the VCO and PD1; the 562B serves as the crystal oscillator and PD2. A 4.400MHz crystal controls the reference frequency f_R. The offset frequency f_m is 100kHz frequency modulated ±25kHz at a modulation frequency of 400Hz. The

accuracy of the output frequency is that of the reference oscillator plus that of the offset oscillator; since f_m is a small percentage (2%) of f_R, its stability can be considerably less than that of the crystal oscillator. In this case, f_m can be provided by a 566 VCO modulated, if desired, by a second 566. (The triangle wave 566 output results in a constant df/dt.)

TRANSLATION LOOP FOR PRECISION TV INTERMEDIATE — FREQUENCY FM GENERATOR
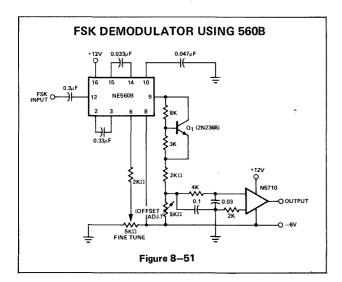
Figure 8—50b

Special layout precautions are required to be sure that no high frequency coupling occurs via grounds or power supply lines. The circuit is adjusted by trimming the 562 VCO trimmer capacitor until the beat note present at test point 1 has the same frequency as f_m throughout the deviation range (f_m can be deviated by hand or very slowly, say, at a 1Hz rate, to observe that the beat note does not break up during sweep. If the beat note is lost at either extreme, adjust the VCO trimmer. If the full deviation cannot be obtained, decrease the 562 low pass filter capacitor slightly. Connect a counter to the output to be sure the loop is locked to $f_R + f_m$ and not $f_R - f_m$ (unless the latter is desired).

Naturally, the component values given may be altered for other applications. Note that as f_m is made a smaller and smaller percentage of the total output frequency, it becomes difficult to prevent locking in the $f_R - f_m$ mode since the 562 lock range will likely include both $f_R - f_m$ and $f_R + f_m$. However, if f_m is made too large a portion of the output frequency, then overall stability suffers unless f_m is also quite precise.

PHASE LOCKED FSK DEMODULATORS (560B, 565)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

The 560B phase locked loop can be used as a receiving converter to demodulate FSK audio tones and to provide a shifting dc voltage to initiate mark or space code elements. The PLL can replace the bulky audio filters and undependable relay circuits previously used for this application. Connection of the 560B PLL as a FSK demodulator is illustrated in Figure 8–51.
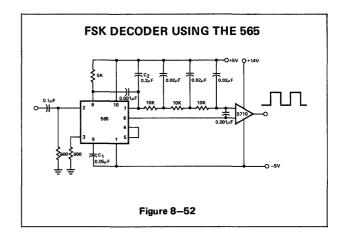
The system functions by locking-on and tracking the output frequency of the receiver. The demodulator frequency shift appears at pin 9 as a direct-current voltage of about 60mV amplitude and must be amplified and signal-conditioned to interface with the printer. The input voltage at pin 12 should be from 30mV to 2V peak-to-peak, square or sine wave. Pin 10, the de-emphasis terminal, is used for bandshaping. The capacitor connected between this terminal and ground bypasses unwanted high frequency noise to ground. Pin 9 is the output (approximately 60mV dc) which is amplified, conditioned and fed to a voltage comparator amplifier (N5710) to provide the proper voltages for interfacing with the printer. This specific circuit was designed to match the Bell 103C and 103D Data Phones. When modifying this circuit to accommodate other systems, maintain the resistance to ground from pin 9 at approximately 15Ω. Pins 3 and 2 are the connections for the external capacitor that determine the free-running frequency of the VCO. The 0.33μF value indicated provides a VCO frequency, f_o, of approximately 1060Hz. The value of the timing capacitor can be calculated by use of the following equation:
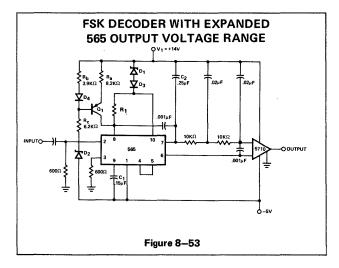
$$C_o = \frac{300pF}{f_o}$$

where f_o is in Hertz.

The output has a swing of 2V peak-to-peak, over a 0 to 600 baud input FSK rate, with less than 10% jitter at the comparator output. The circuit is operative over a temperature range of 0° to 75°C with a total drift of approximately 100mV over the temperature range.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 8–52. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.
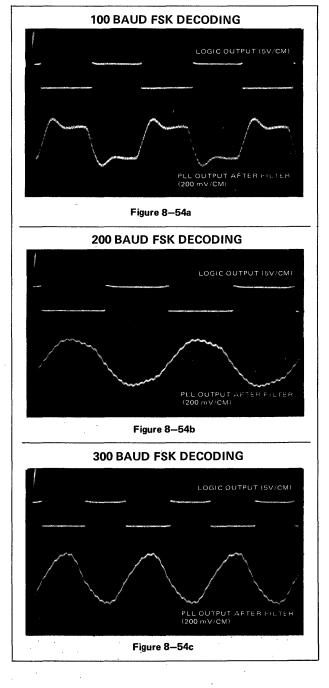

FSK DECODER USING THE 565

Figure 8–52

FSK DEMODULATOR USING 560B

Figure 8–51

The loop filter capacitor C_2 is chosen to set the proper overshoot on the output and a three-stage RC ladder filter is used to remove the sum frequency component. The band edge of the ladder filter is chosen to be approximately half-way between the maximum keying rate (300

baud or bits per second, or 150Hz) and twice the input frequency (about 2200Hz). The free-running frequency should be adjusted (with R_1) so that the dc voltage level at the output is the same as that at pin 6 of the loop. The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6.

The input connection is typical for cases where a dc voltage is present at the source and, therefore, a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to achieve a 600Ω input impedance.)

FSK DECODER WITH EXPANDED 565 OUTPUT VOLTAGE RANGE

Figure 8–53

A more sophisticated approach primarily useful for narrow frequency deviations is shown in Figure 8–53. Here, a constant current is injected into pin 8 by means of transistor Q_1. This has the effect of decreasing the lock range and increasing the output voltage sensitivity to the input frequency shift. The basis for this scheme is the fact that the output voltage (control voltage for VCO) controls only the current through R_1, while the current through Q_1 remains constant. Thus, if most of the capacitor charging current is due to Q_1, the current variation due to R_1 will be a small percentage of the total charging current and, consequently, the total frequency deviation of the VCO will be limited to a small percentage of the center frequency. A 0.25mfd loop filter capacitor gives approximately 30% overshoot on the output pulse, as seen in the accompanying photographs.

The output is then filtered with a two-stage RC ladder filter with a band edge chosen to be approximately 800Hz (approximately half-way between the maximum keying rate of 150Hz and twice the carrier frequency). The number of stages on the filter can be more or less depending on the degree of uncertainty allowable in the comparator output pulse. Two small capacitors (typically 0.001mfd) are connected between pins 8 and 7 of the 565 and across the input of the comparator to avoid possible oscillation problems.

For best operation, the free-running VCO frequency should be adjusted so that the output voltage (corresponding to the input frequencies of 1070Hz and 1270Hz swings equally to both sides of the reference voltage at pin 6. This can be easily done by adjusting the center frequency of the VCO so that the output signal of the 5710 comparator has a 50% duty cycle. It is usually necessary to decouple pin 6 with a large capacitor connected to the positive supply in order to obtain a stable reference voltage for the 5710 comparator.

Figure 8–54 shows the output of the 5710 comparator and the output of the 565 phase locked loop after the filter at rates of 100, 200 and 300 baud, respectively.

100 BAUD FSK DECODING

Figure 8–54a

200 BAUD FSK DECODING

Figure 8–54b

300 BAUD FSK DECODING

Figure 8–54c

ANALOG LIGHT-COUPLED ISOLATORS (565, 567)

The analog isolator shown in Figure 8—55a is basically a
FM transmission system with light as the transmission
medium. Because of the high degree of electrical isolation
achieved, low-level signals may be transmitted without
interference by great potential difference between the
sending and receiving circuits. The transmitter is a 565
used as a VCO with the input applied to the VCO terminal
7. Since the light emitting diode is driven from the 565
VCO output, the LED flashes at a rate proportional to the
input voltage. The receiver is a photo transistor which
drives an amplifier having sufficient gain to apply a 200mV
peak-to-peak signal to the input of the receiving 565,
which then acts as a FM detector with the output appearing
at pin 7. Since the output has a twice carrier frequency
ripple, it is best to keep the carrier frequency as high as
possible (say, 100 times the highest modulation frequency).
Because of the excellent temperature stability of the 565,
drift is minimal even when dc levels are being transmitted.
If operation to dc is not required, the output of the receiver
can be capacitively coupled to the next stage. Also, a 566
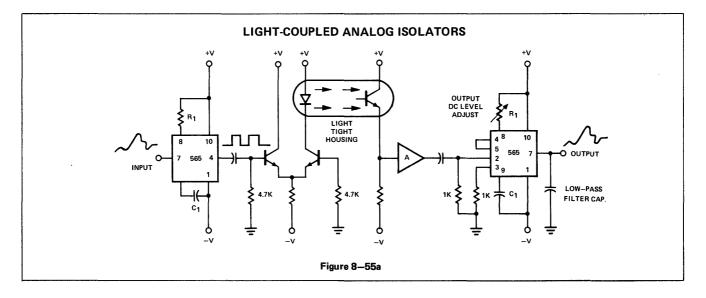can be used as the transmitter.

LIGHT-COUPLED ANALOG ISOLATORS

Figure 8—55a

Figure 8—55b shows that the 567 may be used in the same
manner when operation from 5V supplies is required. Here,
the output stage of the 567 is used to drive the LED
directly. When the free-running frequency of the receiving
567 is the same as that of the transmitting 567, the
non-linearity of the two controlled oscillator transfer
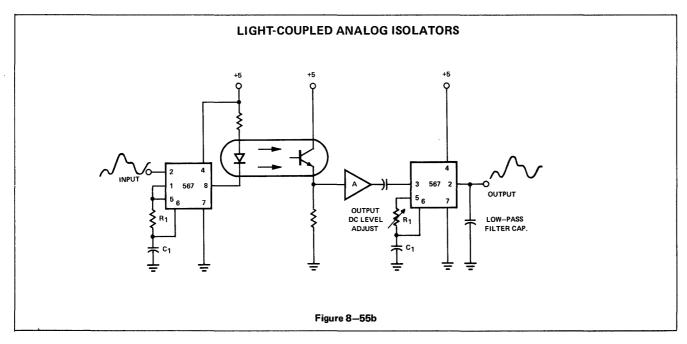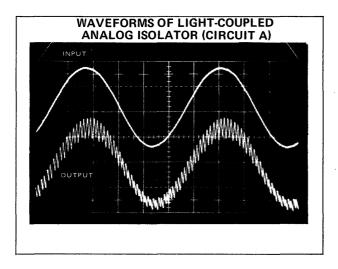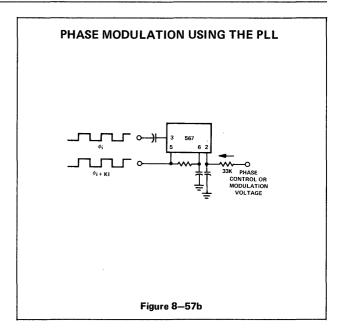functions cancel so that highly linear information transfer
results.

LIGHT-COUPLED ANALOG ISOLATORS

Figure 8—55b

Figure 8–56 is an oscillogram of the input and output of the Figure 8–55a circuit. The output can easily be filtered to remove the sum frequency component.

WAVEFORMS OF LIGHT-COUPLED ANALOG ISOLATOR (CIRCUIT A)
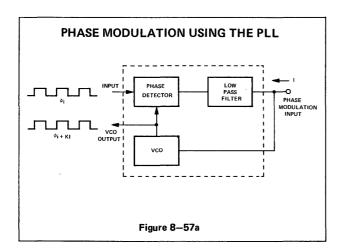
INPUT

OUTPUT

PHASE MODULATORS

If a phase locked loop is locked onto a signal at the center frequency, the phase of the VCO will be 90° with respect to the input signal. If a current is injected into the VCO terminal (the low pass filter output), the phase will shift sufficiently to develop an opposing average current out of the phase detector so that the VCO voltage is constant and lock is maintained. When the input signal amplitude is low enough so that the loop frequency swing is limited by the phase detector output rather than the VCO swing, the phase can be modulated over the full range of 0 to 180°. If the input signal is a square wave, the phase will be a linear function of the injected current.

A block diagram of the phase modulator is given in Figure 8–57a. The conversion factor K is a function of which loop is used, as well as the input square wave amplitude. Figure 8–57b shows an implementation of this circuit using the 567.
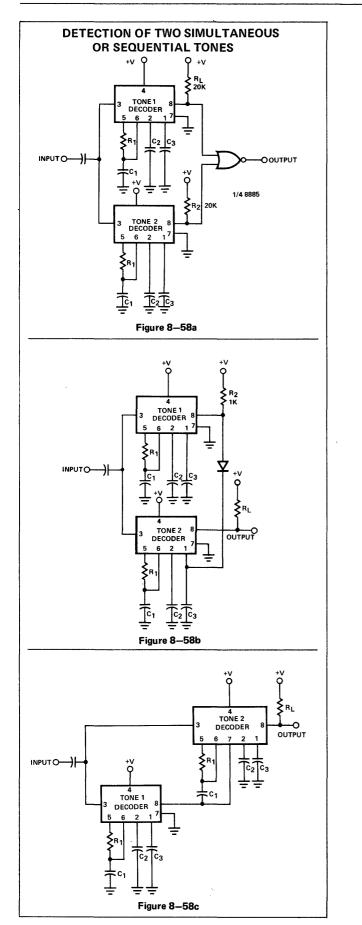

PHASE MODULATION USING THE PLL

INPUT

ϕ_i

$\phi_i + KI$

VCO OUTPUT

PHASE DETECTOR

LOW PASS FILTER

VCO

PHASE MODULATION INPUT

Figure 8–57a

PHASE MODULATION USING THE PLL

ϕ_i

$\phi_i + KI$

3 567

5   6 2

33K PHASE CONTROL OR MODULATION VOLTAGE

Figure 8–57b

DUAL TONE DECODERS (567)

Two integrated tone decoders can be connected (as shown in Figure 8–58a) to permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R_1C_1 and $R_1'C_1'$ are chosen, respectively, for tones 1 and 2. If sequential tones (1 followed by 2) are to be decoded, then C_3 is made very large to delay turn off of unit 1 until unit 2 has turned on and the NOR gate is activated. Note that the wrong sequence (2 followed by 1) will not provide an output since unit 2 will turn off before unit 1 comes on. Figure 8–58b shows a circuit variation which eliminates the NOR gate. The output is taken from unit 2, but the unit 2 output stage is biased off by R_2 and CR_1 until activated by tone 1. A further variation is given in Figure 8–58c. Here, unit 2 is turned on by the unit 1 output when tone 1 appears, reducing the standby power to half. Thus, when unit 2 is on, tone 1 is or was present. If tone 2 is now present, unit 2 comes on also and an output is given. Since a transient output pulse may appear during unit 1 turn-on, even if tone 2 is not present, the load must be slow in response to avoid a false output due to tone 1 alone.
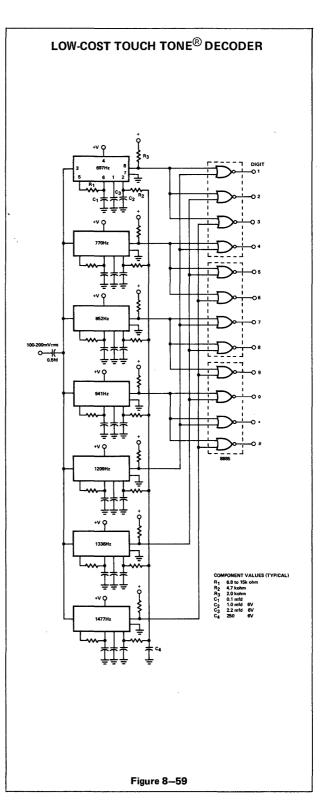
HIGH SPEED, NARROW BAND TONE DECODER (567)

The circuit of Figure 8–58a may be used to obtain a fast, narrow band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than 70mV rms at all times to prevent detection band shrinkage and C_2 should be between $130/f_o$ and $1300/f_o$ mfd where f_o is the nominal detection frequency. The small value of C_2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

DETECTION OF TWO SIMULTANEOUS OR SEQUENTIAL TONES

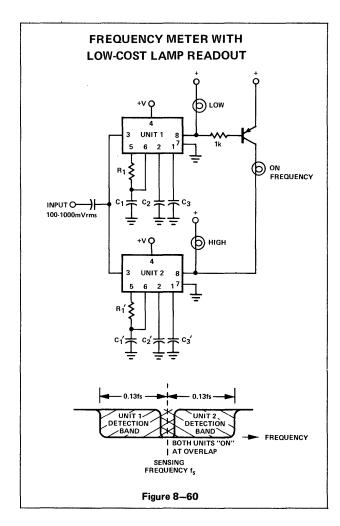
Figure 8—58a

Figure 8—58b

Figure 8—58c

TOUCH-TONE® DECODER (567)

Touch-Tone® decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the push-button dial) that will ultimately be part of every phone. A low cost decoder can be made as shown in Figure 8—59. Seven 567 tone decoders, their

LOW-COST TOUCH TONE® DECODER

COMPONENT VALUES (TYPICAL)
R_1 6.8 to 15k ohm
R_2 4.7 kohm
R_3 2.0 kohm
C_1 0.1 mfd
C_2 1.0 mfd 6V
C_3 2.2 mfd 6V
C_4 250 6V

Figure 8—59

inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R_1 and C_1, to one of the seven tones. The R_2 resistor reduces the bandwidth to about 8% at 100mV and 5% at 50mV rms. Capacitor C_4 decouples the seven units. If you are willing to settle for a somewhat slower response at low input voltages (50 to 100mV rms), the bandwidth can be controlled in the normal manner by selecting C_2, thereby eliminating the seven R_2 resistors and C_4. In this case, C_2 would be 4.7mfd for the three lower frequencies and 2.2mfd for the four higher frequencies.

The only unusual feature of this circuit is the means of bandwidth reduction using the R_2 resistors. As shown in the 567 data sheet under Alternate Method of Bandwidth Reduction, an external resistor R_A can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R_2 serves the same function as R_A except that instead of going to a voltage divider for dc bias it goes to a common point with the six other R_2 resistors. In effect, the five 567s which are not being activated during the decoding process serve as bias voltage sources for the R_2 resistors of the two 567s which are being activated. Capacitor C_4 (optional) decouples the ac currents at the common point.
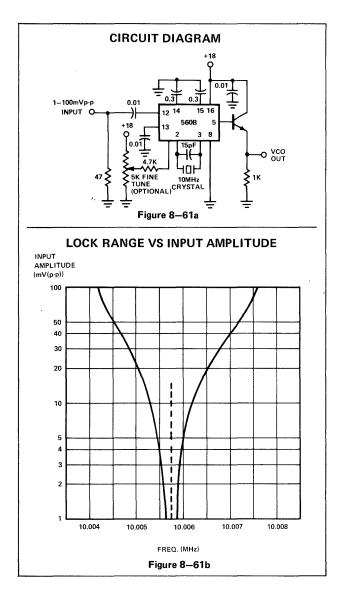
LOW COST FREQUENCY INDICATOR (567)

Figure 8–60 shows how two tone decoders set up with overlapping detection bands can be used for a go/no-go frequency meter. Unit 1 is set 6% above the desired sensing frequency and unit 2 is set 6% below the desired frequency. Now, if the incoming frequency is within 13% of the desired frequency, either unit 1 or unit 2 will give an output. If both units are on, it means that the incoming frequency is within 1% of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

CRYSTAL-STABILIZED PHASE LOCKED LOOP (560B)

Figure 8–61a shows the 560B connected as a tracking filter for signals near 10MHz. The crystal keeps the free-running frequency at the desired value. Figure 8–61b gives the lock and capture range as a function of input amplitude. An emitter follower has been added to the normal VCO output to prevent pulling the loop off frequency.

FREQUENCY METER WITH LOW-COST LAMP READOUT

Figure 8–60

CIRCUIT DIAGRAM

Figure 8–61a

LOCK RANGE VS INPUT AMPLITUDE
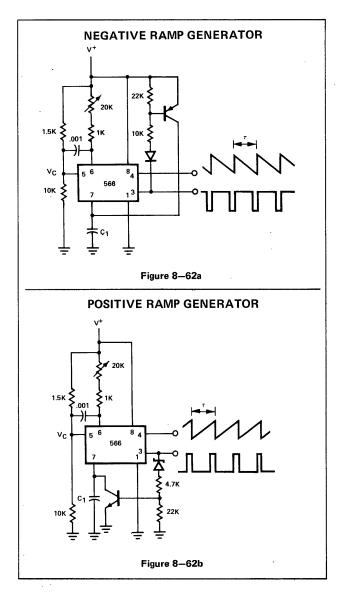
Figure 8–61b

RAMP GENERATORS (566)

Figure 8–62 shows how the 566 can be wired as a positive or negative ramp generator. In the positive ramp generator, the external transistor driven by the pin 3 output rapidly discharges C_1 at the end of the charging period so that charging can resume instantaneously. The pnp transistor likewise rapidly charges the timing capacitor C_1 at the end of the discharge period. Because the circuits are reset so quickly, the temperature stability of the ramp generator is excellent. The period τ is $1/2f_0$ where f_0 is the 566 free-running frequency in normal operation. Therefore,

$$\tau = \frac{1}{2f_0} = \frac{R_T C_1 V^+}{5(V^+ - V_c)}$$

where V_c is the bias voltage τ pin 5 and R_T is the total resistance between pin 6 and V^+. Note that a short pulse is available at pin 3. (Placing collector resistance in series with the external transistor collector will lengthen the pulse.)
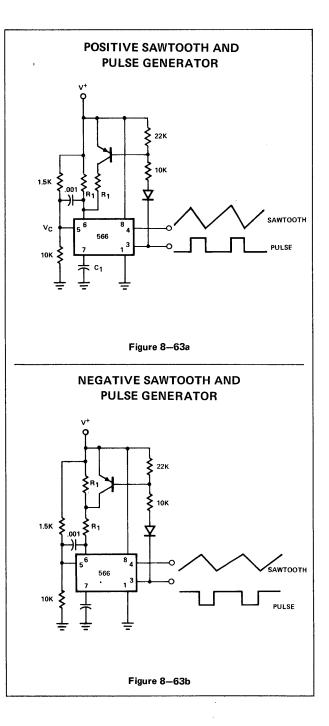

NEGATIVE RAMP GENERATOR

Figure 8–62a

POSITIVE RAMP GENERATOR

Figure 8–62b

SAWTOOTH AND PULSE GENERATOR (566)

Figure 8–63 shows how pin 3 output can be used to provide different charge and discharge currents for C_1 so that a sawtooth output is available at pin 4 and a pulse at pin 3. The pnp transistor should be well saturated to preserve good temperature stability. The charge and discharge times may be estimated by using the formula

$$\tau = \frac{R_T C_1 V^+}{5(V^+ - V_c)}$$

where R_T is the combined resistance between pin 6 and V^+ for the interval considered.

POSITIVE SAWTOOTH AND PULSE GENERATOR

Figure 8–63a

NEGATIVE SAWTOOTH AND PULSE GENERATOR
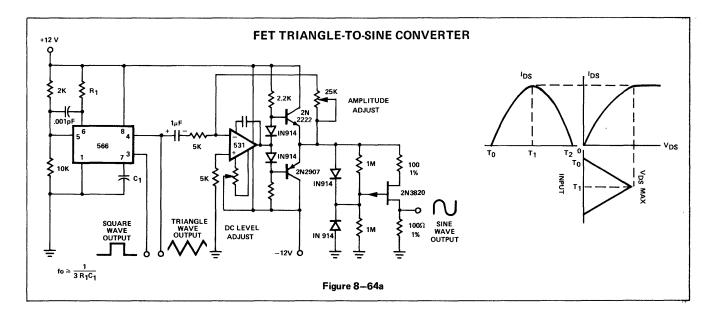
Figure 8–63b
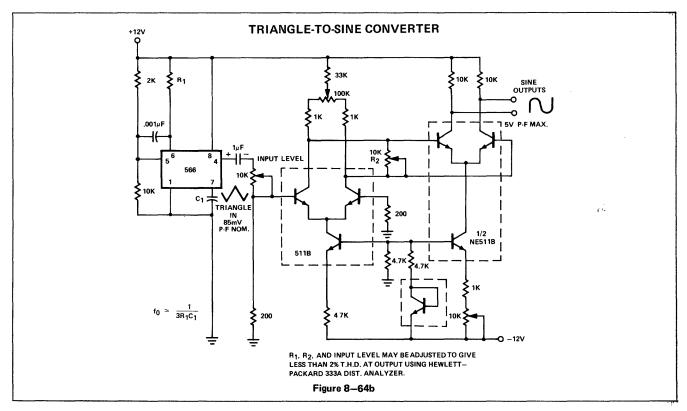
TRIANGLE-TO-SINE CONVERTERS (566)

Conversion of triangular wave shapes to sinusoids is usually accomplished by diode-resistor shaping networks, which accurately reconstruct the sine wave segment by segment. Two simpler and less costly methods may be used to shape the triangle waveform of the 566 into a sinusoid with less than 2% distortion.

The first scheme (Figure 8–64a) uses the non-linear $I_{DS} - V_{DS}$ transfer characteristic of a p-channel junction

FET to shape the triangle waveform. The second scheme (Figure 8–64b) uses the non-linear emitter base junction characteristic of the 511B for shaping.

In both cases, the amplitude of the triangle waveform is critical and must be carefully adjusted to achieve a low distortion sinusoidal output. Naturally, where additional waveform accuracy is needed, the diode-resistor shaping scheme can be applied to the 566 with excellent results since it has very good output amplitude stability when operated from a regulated supply.

FET TRIANGLE-TO-SINE CONVERTER

Figure 8–64a

TRIANGLE-TO-SINE CONVERTER

R_1, R_2, AND INPUT LEVEL MAY BE ADJUSTED TO GIVE LESS THAN 2% T.H.D. AT OUTPUT USING HEWLETT–PACKARD 333A DIST. ANALYZER.
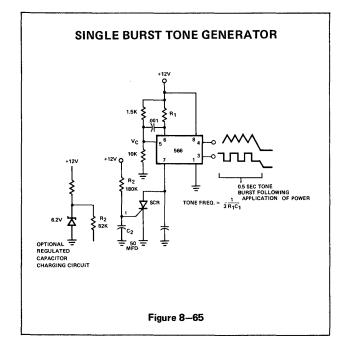
Figure 8–64b

SINGLE TONE BURST GENERATOR (566)

Figure 8–65 is a tone burst generator which supplies a tone for one-half second after the power supply is activated; its intended use is as a communications network alert signal. Cessation of the tone is accomplished by the SCR, which shunts the timing capacitor C_1 charge current when activated. The SCR is gated on when C_2 charges up to the gate voltage, which occurs in 0.5 seconds. Since only $70\mu A$ are available for triggering, the SCR must be sensitive enough to trigger at this level. The triggering current can be increased, of course, by reducing R_2 (and increasing C_2 to keep the same time constant). If the tone duration must be constant under widely varying supply voltage conditions, the optional Zener diode regulator circuit can be added, along with the new value for R_2, $R_2' = 82K$.

If the SCR is replaced by a npn transistor, the tone can be switched on and off at will at the transistor base terminal.

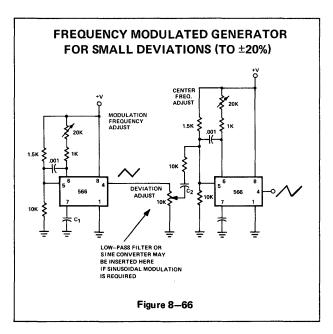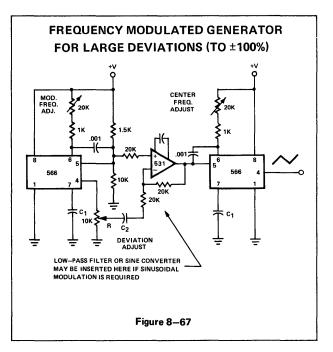

SINGLE BURST TONE GENERATOR

Figure 8–65

LOW FREQUENCY FM GENERATORS (566)

Figures 8–66 and 8–67 show FM generators for low frequency (less than 0.5MHz center frequency) applications. Each uses a 566 function generator as a modulation generator and a second 566 as the carrier generator.

Capacitor C_1 selects the modulation frequency adjustment range and C_1' selects the center frequency. Capacitor C_2 is a coupling capacitor which only needs to be large enough to avoid distorting the modulating waveform.

If a frequency sweep in only one direction is required, the 566 ramp generators given in this section may be used to drive the carrier generator.

FREQUENCY MODULATED GENERATOR FOR SMALL DEVIATIONS (TO ±20%)

Figure 8–66

FREQUENCY MODULATED GENERATOR FOR LARGE DEVIATIONS (TO ±100%)
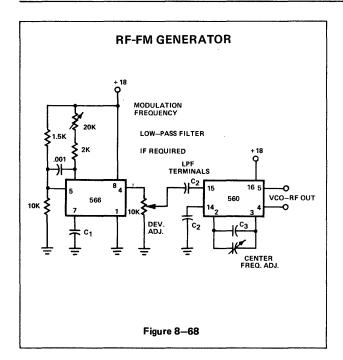
Figure 8–67

RADIO FREQUENCY FM GENERATORS (566, 560B)

Figure 8–68 shows how a 560B may be used as a FM generator with modulation supplied by a 566 function generator. Capacitor C_1 is chosen to give the desired modulation range, C_2 is large enough for undistorted coupling and C_3 with its trimmer specifies the center frequency. The VCO output may be taken differentially or single ended.

A 561B or 562B with appropriate pin numbering changes may also be used in this application. If a sweep generator is desired, the 566 may be connected as a ramp generator (described elsewhere in this chapter).

RF-FM GENERATOR

Figure 8—68

PRECISION POWER INVERTER (566, 540)

Figure 8—69 shows a precision 12 VDC to 115 VAC 100W inverter. Its triangular output is derived from the 566 function generator, providing a high degree of frequency stability (±.02%/°C). The 540 power driver is used to drive the power output stage. Because of third harmonic attenuation in the transformer, the output is very close to a pure 60Hz sine wave.

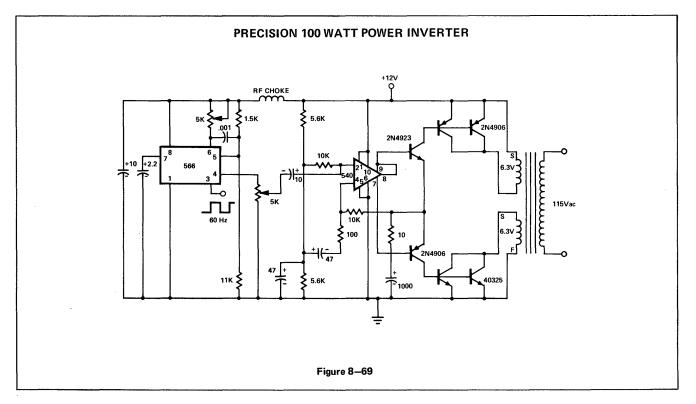## DESIGN IDEAS FOR USING PHASE LOCKED LOOPS

The following design ideas were drawn mainly from the Signetics-EDN Phase Locked Loop Contest. These circuits should be viewed as design suggestions only since Signetics has not verified their operating characteristics. In all cases, however, the principle of operation appears to be sound.

Quotation marks indicate quotes taken directly from the contest entry.

AIRCRAFT VHF OMNIDIRECTIONAL RANGE (VOR) RECEIVER

Herbert F. Kraemer of Minneapolis, Minnesota, submitted the winning contest entry which uses one phase locked loop (562) as an AM detector, a second loop (565) as an FM detector and a third loop (565) as a self-biased phase detector.

"The circuit is a new type of VOR (VHF omnidirectional range) receiver used in air navigation to determine an airplane's angular bearing with respect to a VOR transmitter located on the ground. The principles of the circuit allow any desired increase in accuracy, as compared to current units, with potential cost savings.

PRECISION 100 WATT POWER INVERTER

Figure 8—69

A VOR station transmits in the VHF band (108–117.9MHz). Two signals are transmitted on the same carrier, i.e.,

1) A 30Hz reference signal which frequency modulates an audio frequency subcarrier of 9960Hz. This subcarrier then amplitude modulates the VHF carrier.

2) A 30Hz directional signal which amplitude modulates the VHF carrier.

The latter signal varies in phase with respect to the reference, depending on the bearing of the VOR station and the receiver. Both signals are in phase when the receiver is north of the transmitter and 180 degrees out of phase when the receiver is south.

Current VOR receivers are specified to be accurate within a 1–2 degree bearing, but many pilots accept 4 degree errors. The major design problem is to produce a receiver which will measure phase differences to an accuracy of about 1 degree, throughout the entire 360 degree range."

Although analog quarter-square multipliers can be built to an accuracy of 0.01%, the simpler analog phase detectors are only accurate to 3–4°. This circuit uses the NE562 PLL to frequency multiply the two 30Hz signals, producing 60 and 120Hz signals. A digital method combines these signals, thereby dividing the entire range of bearings into eight 45° sectors. One of eight lights on the display will light, showing the pilot his approximate bearing. An analog method .is then used to further determine the phase difference and the bearing within the given 45° sector. Extending the principle further, sectors of 22½$^\circ$ could be used for improved accuracy.

This VOR receiver does not have the conventional to-from switch since it indicates directly throughout the entire 360° range. Confusion of 180° in bearing (going the wrong way) is impossible with this receiver.

System Description (References to Block Number — Figure 8–70)

Block 1. This is a standard VHF tuner.
Block 2. The NE561 is used for IF and AM detection.
Block 3. A low pass filter removes the 9960Hz subcarrier. It appears that a zero crossing detector is not needed to shape the input signal to the NE562.
Block 4. Frequency multiplier.
Block 5. High pass filter.
Block 6. FM detection of 30Hz signal.
Block 7. A calibration adjustment to compensate for any phase shifts throughout the circuit. A gain may be needed since the FM detector output is low.
Block 8. Another frequency multiplier.
Block 9. Standard ripple flip-flops for divide-by-two.

Block 10. A null principle is normally used in a VOR receiver so that the pilot can fly along a predetermined course, nulling the needle by turning his plane. To insure that the needle always reacts in the same direction for a given direction of error, even sectors are treated differently than odd sectors." The phase comparison is made with respect to C for *odd* sectors, and with respect to $\overline{C}$ for *even* sectors.
Block 11. "At the desired null, the two signals must be 90 degrees out of phase to obtain a zero output from the phase detector. Some gain may be needed to compensate for the losses in Block 10.
Block 12. The phase detector portion of the NE565 only is used. The VCO part is unused but may be valuable in certain types of special displays.

An alternate form of analog phase detector might be an AND gate followed by a standard duty cycle integrator, such as used on dwell meters.
Block 13. The digital signals from the flip-flops are decoded with AND gates to indicate the sector corresponding to the phase lag between the two 30Hz signals."
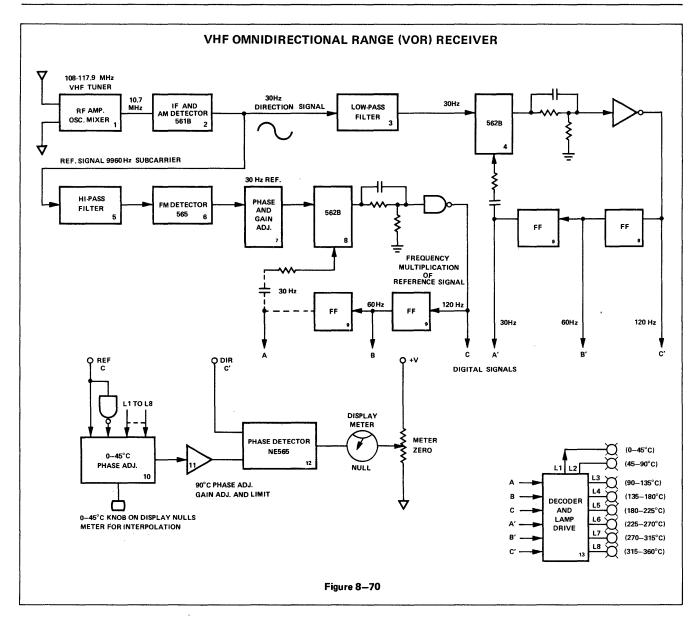
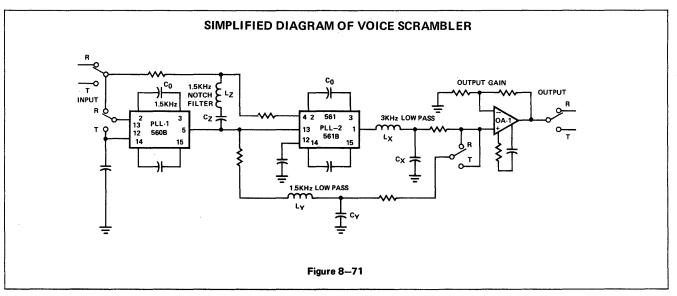## SPEECH PRIVACY CIRCUIT (SPEECH SCRAMBLER)

The second place entry was that of David M. Alexander of Austin, Texas. His application for the loop was a voice scrambler-unscrambler for private communications.

"This circuit utilizes the principles of frequency inversion and masking to render speech unintelligible to listeners not possessing a similar unit. A synchronization signal is generated as part of the scrambled signal which phase locks the decoding carrier oscillator to the coding oscillator and thus guarantees minimum distortion in the unscrambled speech. This synch signal also increases the security close to the inversion point where they are displaced only slightly from their original values."

In operation, a single circuit serves as both scrambler and unscrambler at one end of a two-way communications link. It is switched from the receive mode to the transmit mode by a multipole relay controlled by the push-to-talk switch on the system microphone or handset.

As can be seen by the diagram (Figure 8 –71), the major components of the system are the synch oscillator PLL-1 (NE560B), the carrier oscillator-modulator PLL-2 (NE561B) and the mixer-gain stage OA-1 (5709).

VHF OMNIDIRECTIONAL RANGE (VOR) RECEIVER

Figure 8—70

SIMPLIFIED DIAGRAM OF VOICE SCRAMBLER

Figure 8—71

In the transmit mode, PLL-1 is adjusted to free-run at the inversion frequency (1.5kHz), or ½ the desired carrier frequency. PLL-2 is phase locked to this oscillator and operates on its second harmonic frequency (3kHz). The audio to be scrambled is applied to the input of the multiplier of PLL-2. This produces the sum and difference products of the input audio and the encoding carrier. The sum product is filtered out by the low pass filter (Lx-Cx), leaving only the difference product. This product consists of the original audio signal with the frequency components inverted about ½ the carrier frequency, or 1.5kHz. The square wave output of the oscillator of PLL-1 is low pass filtered by network Ly-Cy to produce a sine wave sync signal which is mixed with the inverted speech by OA-1 to produce the final scrambled signal.

In the receive mode, PLL-1 is phase locked to the 1.5kHz synch and masking signal and acts as a signal conditioner for this signal. PLL-2 doubles this frequency to produce the decoding carrier. The scrambled signal is notch-filtered by network Lz-Cz to remove the 1.5kHz sync and masking signal and the resultant inverted audio applied to the multiplier of PLL-2. Here it is re-inverted in a manner similar to that of the transmit mode. The resultant unscrambled audio is amplified in OA-1 for output to further system audio stages."

[Note: It is suggested that the 1.5kHz "sync and masking" signal be changed to 1.0kHz, since PLL-2 (free-running at 3kHz) will lock to the third harmonic of the 1kHz square wave from PLL-1 more readily than to the small second harmonic of the 1.5kHz signal. It may then be desirable to disconnect the notch filter during transmission. Of course, the filters may be implemented using active filter techniques.]

PRECISION PROGRAMMABLE TIME DELAY GENERATOR

Sam Butt of Gaithersburg, Maryland, submitted the third place entry. This circuit provides both a pulse and a high frequency output at some time t_d after an input pulse is received. The interval t_d is programmable in 10 steps by means of a digital output switch.

Figure 8–72 shows the circuit in simplified form. It works as follows:

The 562 VCO is set so that its center frequency is at a point slightly above (say 10.5MHz) the window of the 10MHz band pass filter (BPF). Thus, no rf appears at the output. When a pulse is received at the input, the flip-flop is set so as to actuate one input A of the N8880A NAND gate.

The other side of the NAND gate B receives a signal which occurs at the rate of f_r/M where M is set by the binary-output switch. The output of the NAND gate begins to drive the N8291A binary ripple counter which is connected to the divide-by-N circuit in the loop feedback path. When 10 counts have been registered, the divide-by-N counter is putting out $f_o/10$ or (in the assumed case) 1.05MHz. Since the phase comparator now sees two frequencies very close together, the loop locks up and $f_o = 10 f_r$. Since f_r is 1MHz, the VCO operates at 10MHz rf which the band pass filter passes to the output. This rf is detected and used to reset the input flip-flop and the counter in preparation for the next input pulse. The duration of the rf output is determined mainly by the detector time constant. The duration of the output pulse, which begins when the rf detector actuates the one-shot, is determined by the one-shot time constant.

The delay time is

$$t_d = \frac{NM}{f_r}$$

where M is settable between 1 and 10 using the digital switch.

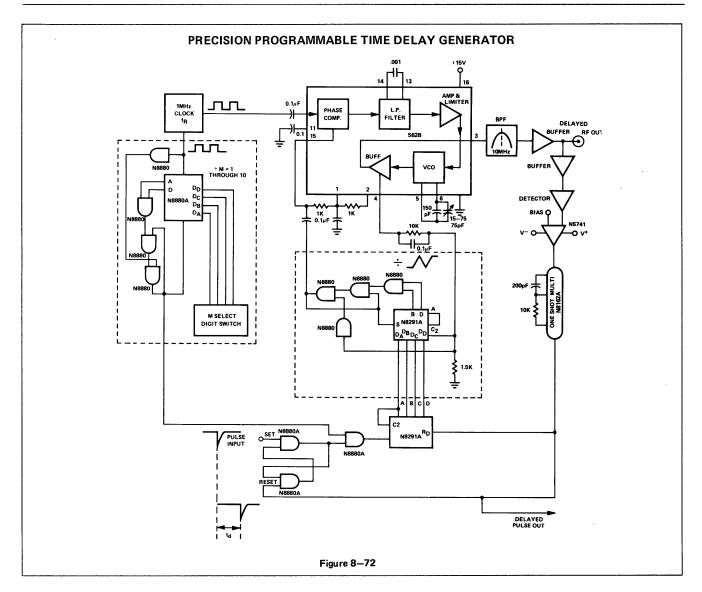## METAL DETECTOR USING PLL AS A FREQUENCY METER (565)

The metal detector shown in Figure 8–73 was submitted to the Signetics-EDN Phase Locked Loop Contest by Jim Blecksmith of Irvine, California. It incorporates a 565 as a frequency meter which indicates the frequency change in a Colpitts oscillator whose tank coil approaches a metal object. The loop output voltage at pin 7 is compared with the reference voltage at pin 6 and the difference amplified by meter amplifier Q_4, Q_5.
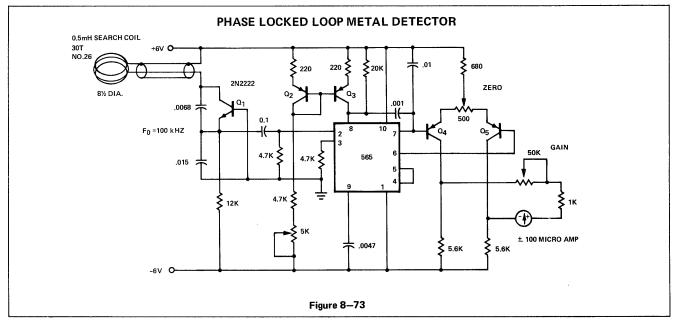
To increase the loop output (pin 7) to about 0.5V per percent of frequency deviation, a current source (Q_2, Q_3) is used to supply most of the capacitor (2.5mA) charge and discharge current at pin 8. The 20K resistor connected to pin 8 changes the charge and discharge current by $\frac{0.5V}{20K\Omega} =$ .025mA or about 1% per 0.5V. Since the voltage at pins 8 and 7 track, the loop output voltage is also 0.5V per percent deviation. (This technique of increasing loop output swing for small frequency deviations is discussed in the Expanding Loop Capability section of this chapter.)

Increasing oscillator frequency, as indicated by a rising meter indication, results when the search coil is brought near a non-ferrous metal object. Reduced oscillator frequency, as indicated by a dropping meter reading, results from the search coil being brought near a ferrous object.

PRECISION PROGRAMMABLE TIME DELAY GENERATOR

Figure 8—72

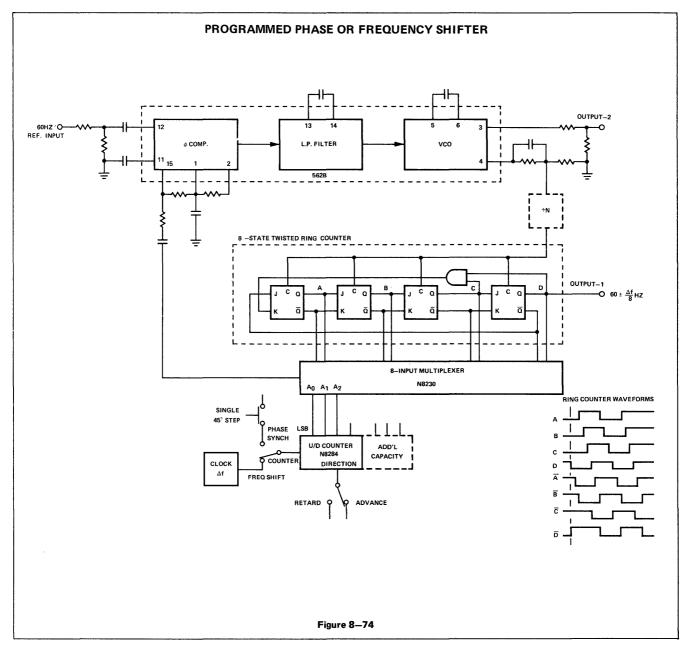## PHASE LOCKED LOOP METAL DETECTOR

Figure 8—73

PROGRAMMED PHASE OR FREQUENCY SHIFT

Howard E. Clupper of Chadds Ford, Pennsylvania, submitted the following circuit in which "a digital phase shifter is inserted in the loop between the VCO and the phase comparator. The phase shift is programmed by sequentially selecting the ring counter outputs by means of the multiplexer and up-down counter.

"As shown in Figure 8—74, the eight ring counter outputs are separated by 45°, which is within the lock-in range of the loop. Output 1 is constrained to follow the phase shift introduced and may be used, for example, to drive a synchronous motor above or below its normal speed, while still maintaining reference with the input. This is accomplished by monitoring the contents of the up-down

counter (which may be any length). As long as the counter does not overflow, the motor may be advanced or retarded in any manner and then returned to the original relationship with respect to the 60Hz reference input by running the U/D counter to the initial value.

For higher frequency outputs, a divide-by-N counter may be added in the normal manner and the output taken directly from the VCO at output 2. Operation in this mode would provide means to generate a precisely controlled FM signal of any arbitrary center frequency depending upon the frequency of the reference input and the value of N."

The 565 may be used in this circuit in place of the 562 for lower frequency applications (less than 500kHz).

PROGRAMMED PHASE OR FREQUENCY SHIFTER

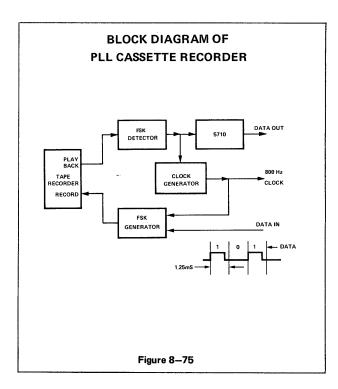Figure 8—74

FSK DATA CONVERTER FOR CASSETTE RECORDER

A circuit scheme which allows an ordinary reel or cassette tape recorder to be used as a digital data recorder was submitted by Daniel Chin of Burlington, Massachusetts.

"The circuit design allows any single-track audio tape recorder with frequency response to 7kHz to be used as a digital recorder for many non-critical applications. This application provides a complete data recording system using two recorded frequencies on a single track. The two frequencies are obtained from two synchronized NE565s. Detection of the recorded frequencies requires a third NE565. A fourth circuit is used to generate and synchronize the system clock. The advantages obtained by using these techniques are elimination of the need for:

1.   A timing channel to strobe off the data, or
2.   A third frequency for null, while using the other two frequencies for 1 and 0.

This implementation, therefore, is one of the simplest ways to get a digital recording system on an audio recorder. It is shown in block diagram form in Figure 8—75.

The parameters chosen for the circuit design allow a digital recording bit rate of 800Hz or 100 8-bit characters per second. Though 100 characters per second is less than the 300-character-per-second speed of a high-speed paper tape reader, the low cost of this circuitry combined with the audio tape recorder should make this system very attractive from a cost performance viewpoint. This is especially true when compared with the normal Teletype speed of 10 characters per second.
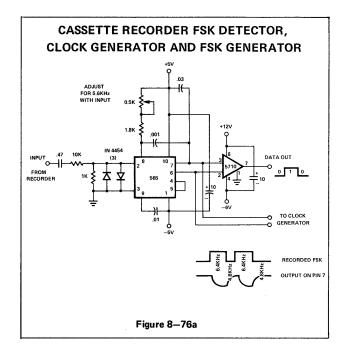
The circuits will also work with the readily available low cost cassette recorders now available, which make compact as well as low cost information storage. A FSK system of recording is used, which allows the voice recording and reproduction electronics of the recorder to be unmodified for use in recording digital information. The retained electronics may also be used to record voice message identification of the various sections of the tape.

The intended use of this circuit is to convert an audio recorder for minicomputer programs written for engineering design applications. Such an application requires good information storage and retrieval over a wide range of storage time. Redundancy may be incorporated by using a two-channel recorder (stereo) and a FSK detector per channel. The outputs of the two detectors could then be ORed digitally to recovered recorded 1s and, thus, give a safeguard against dropouts.

Circuit Description

Four NE565s are used in three circuits to achieve the design. These are:

The FSK detector (Figure 8—76a) is used to detect 6.4kHz for a 1 and 4.8kHz for a 0. The data output is taken from a 5711 connected to pins 7 and 6 of the NE565. The recording method used is RZ FSK, which means that a zero is recorded as 4.8kHz for the entire bit period and one is recorded as 6.4kHz for about 60 percent of the period and 4.8kHz for the remaining 40 percent of the period. This 60 percent bit duty cycle insures that the clock will synchronize with a negative transition during the time that a 1 should be detected.

BLOCK DIAGRAM OF PLL CASSETTE RECORDER

Figure 8—75

CASSETTE RECORDER FSK DETECTOR, CLOCK GENERATOR AND FSK GENERATOR

Figure 8—76a

The clock generator (Figure 8—76b) is used to derive the 800Hz with no input. When the data pulses are extracted from the recorded data, the clock is synchronized to the data. The design allows up to 7 zeros in succession without causing the clock to go out of synchronization. This condition is easily met if odd parity is used to record the 8-bit characters. (One of the 8 bits is a parity bit and, thus, one bit out of 8 is always a one.)

The FSK generator (Figure 8—76c) provides the FSK signal for recording on tape. It consists of 2 oscillators locked to the basic 800Hz system clock but oscillating at 6.4kHz and 4.8kHz. The incoming data to be recorded selects either oscillator as the frequency to be recorded. Harmonic suppression of the square wave output is taken care of automatically by the high frequency roll off characteristic of the tape recorder."

CLOCK GENERATOR

Figure 8—76b

FSK GENERATOR

Figure 8—76c

SELF-RESETTING DIGITAL CLOCK

The following application, submitted by Don Lancaster of Goodyear, Arizona, makes use of the 561B as a 60kHz AM detector.

"The 561B Phase Lock Loop may be combined with TTL integrated circuits to form an always-accurate digital clock based upon the monitoring and direct display of the time code provided by NBS radio station WWVB operating at a 60kHz carrier frequency. Unlike the other time services, WWVB presents a time code directly in BCD digital form, coded as a 10 decibel AM reduction of the carrier. A clock based on this time code information would always be accurate as no counters would be involved and the digital display would always correct itself after a power failure, unlike regular electric clocks which must be manually reset.

Until recently, this type of clock circuitry would have been prohibitively expensive, but now the PLL makes the receiver portion of the clock extremely simple, while recent drastic price reductions in TTL MSI make the display and readout also a simple and relatively economical proposition.

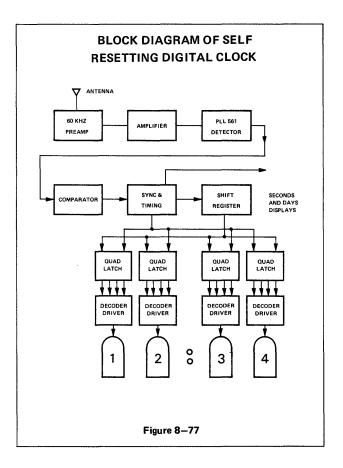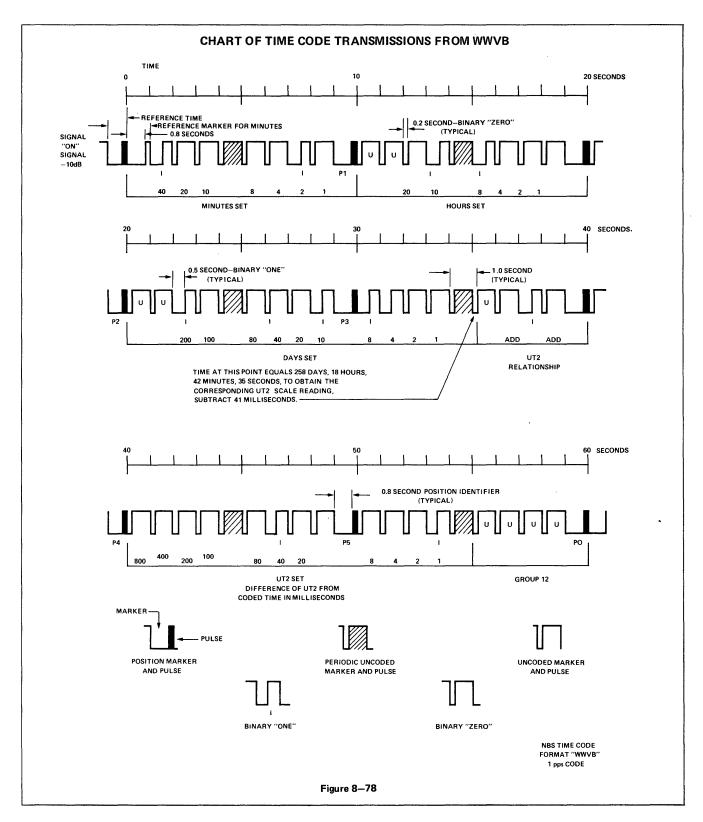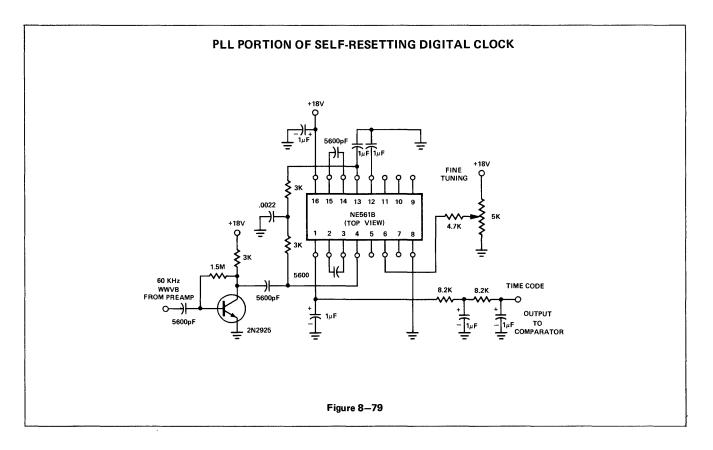**BLOCK DIAGRAM OF SELF RESETTING DIGITAL CLOCK**

Figure 8—77

Figure 8—71 shows a block diagram of the system. A high Q antenna and a suitable low noise preamplifier are used for a front end, followed by an additional gain stage and the 561 set up as a synchronous AM detector. The output of the 561 consists directly of the demodulated time code.

The code is then translated with a comparator and routed to a two-monostable synchronizer that seeks the double once-each-minute sync pulse that identifies that the tens of hours code will follow (Figure 8–78). After synchronization, the code is "1"–"0" detected and routed to a five stage shift register. On every fifth count (consisting of a BCD word and a marker) one of four quad latches are strobed. The latches then store the appropriate minutes, tens of minutes, hours and tens of hours. Each quad latch then drives a BCD/Decimal Decoder/Driver, which in turn drives a NIXIE® or other suitable display tube.

CHART OF TIME CODE TRANSMISSIONS FROM WWVB

TIME AT THIS POINT EQUALS 258 DAYS, 18 HOURS, 42 MINUTES, 35 SECONDS, TO OBTAIN THE CORRESPONDING UT2 SCALE READING, SUBTRACT 41 MILLISECONDS.

NBS TIME CODE
FORMAT "WWVB"
1 pps CODE

Figure 8–78

The display gives the time to the nearest minute and is updated every minute. Seconds are added simply by a blinker, or else a divide-by-60 counter and decoder driver may be used. This counter may be reset every minute by the sync pulse; thus, after a power failure, the clock would correct its seconds reading within a minute of the power being reapplied. If desired, the day of the year may be similarly displayed and if local time is preferred to GMT, a suitable BCD adder or subtractor may be placed between the shift register and the latches.

Figure 8—79 shows the PLL detector circuit. It was found that either a rooftop hula hoop or a ferrite rod and a local 10dB gain amplifier was sufficient to drive the PLL if a single transistor gain stage was added between the two. The amplified 60kHz signal is applied directly to the RF input and applied to the AM Multiplier input via a 90° phase shift network. The output of the multiplier is triply RC filtered to give a good rejection of 60Hz hum, while still allowing the 0.2 second minimum-width pulses to pass with good fidelity."

PLL PORTION OF SELF-RESETTING DIGITAL CLOCK

Figure 8—79

TAPE RECORDER FLUTTER METER

Using the 561 as a flutter meter for tape recorders was suggested by Ronald Blair of Houston, Texas. His circuit is given in Figure 8—80.

"The Signetics PLL 561B is used to detect the frequency variations of the playback 3kHz tone. The VCO frequency is set to a nominal 3kHz by C_O and fine tuning trimmer. The demodulated output is ac coupled to a high input impedance amplifier. An oscilloscope can be used to measure peak deviations and a true RMS voltmeter is used to make RMS flutter readings. Note: Waveform is complex and averaging or peak reading meters will not give true readings.
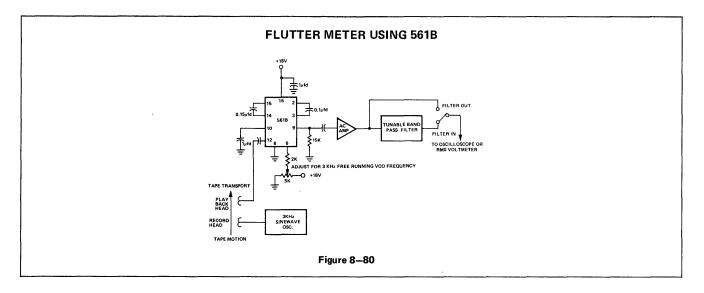
The output may be calibrated by feeding in a 3kHz tone from an oscillator and offsetting the frequency by 1% and measuring the output level shift. Good recorders have RMS flutter of less than 0.1%. The output can be filtered to study selected frequency bands.

Speed variations in the movement of tape across the heads in a 4 tape recorder cause the playback frequency to vary from the original signal being recorded. These speed variations are caused by mechanical problems associated with the tape drive and tape guidance mechanisms. The variation in frequency of the playback signal is called flutter and is generally measured over a frequency range of 0.5Hz + 0.200Hz.

Test tapes with low recorded flutter variations are available to test playback mechanisms. These tapes are standardized at 3kHz. With systems equipped with record heads, a 3kHz tone can be recorded for analysis."
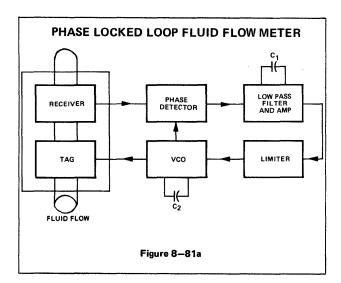
[Note: A 565 may be used in place of the 561B since the frequency is quite low.]

FLUTTER METER USING 561B

Figure 8—80

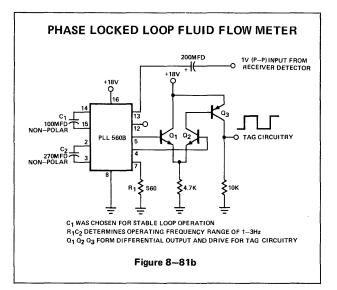## PHASE LOCKED LOOP FLUID FLOWMETER

Whenever a phase locked loop is locked, its VCO signal is 90° out of phase with the input signal (unless the input signal is off frequency and very weak). It has been found that the loop can lock to itself if its VCO signal is phase shifted 90° and then applied to the input. The loop will then run at whatever frequency develops a 90° phase shift in the phase shift network. An interesting application of this technique was submitted by Richard E. Halbach of Milwaukee, Wisconsin. Mr. Halbach used the time delay of a mass (bolus) of fluid moving through a length of tubing as a phase shift mechanism so that the PLL frequency became a function of the flow rate. Figure 8—81 shows this technique in block diagram form (a) and implemented using a 560B (b).

"Simply stated, Nuclear Magnetic Resonance (NMR) is that precession of nuclei, in this case hydrogen, in the presence of a magnetic field. Its precession can be detected by an appropriate receiver coil assembly. A coil up-stream from the receiver coil when activated changes the nuclear magnetization of a bolus (or mass) of fluid in such a way that this change can be detected in the receiver as the bolus subsequently passes through it...transport delay from the tag coil to the receiver, an inverse function of flow velocity, can be used to introduce a 90° phase lag into the external feed back loop of the PLL, which when matched with the 90° internal lag of the PLL, allows the loop to lock. The VCO frequency is then a direct function of velocity of flow."

[Note: A 565 can be used as well as the 560 at this low frequency. Frequency can be read out at the low pass filter (using a low frequency integrating voltmeter) or by measuring the period of the output waveform (flow is then inversely related to the period). If the VCO is run at a carefully chosen higher frequency and then divided down prior to the phase detector and tag coil, the frequency of the VCO as read by a counter can be adjusted to indicate in flow units directly.]

PHASE LOCKED LOOP FLUID FLOW METER

Figure 8—81a

PHASE LOCKED LOOP FLUID FLOW METER

C_1 WAS CHOSEN FOR STABLE LOOP OPERATION
R_1C_2 DETERMINES OPERATING FREQUENCY RANGE OF 1–3Hz
Q_1 Q_2 Q_3 FORM DIFFERENTIAL OUTPUT AND DRIVE FOR TAG CIRCUITRY

Figure 8—81b

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