Signetics

Logic Interface
October 1981

Logic Interface Circuits

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CONTENTS

Quad 3-State Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74125	10ns	32mA
74LS125	8ns	11mA
74126	10ns	36mA
74LS126	9ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74125N • N74LS125N N74126N • N74LS126N	
Ceramic DIP	N74125F • N74LS125F N74126F • N74LS126F	S54LS125F S54126F • S54LS126F
Flatpack		S54LS125W S54126W • S54LS126W

FUNCTION TABLE '125

INPUTS		OUTPUT
C	A	Y
L	L	L
L	H	H
H	X	(Z)

FUNCTION TABLE '126

INPUTS		OUTPUT
C	A	Y
H	L	L
H	H	H
L	X	(Z)

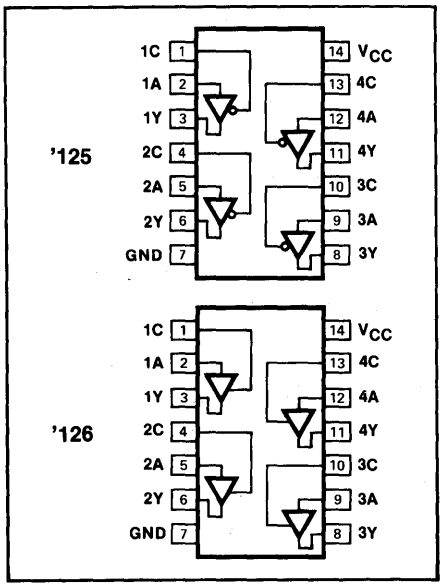
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off)

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

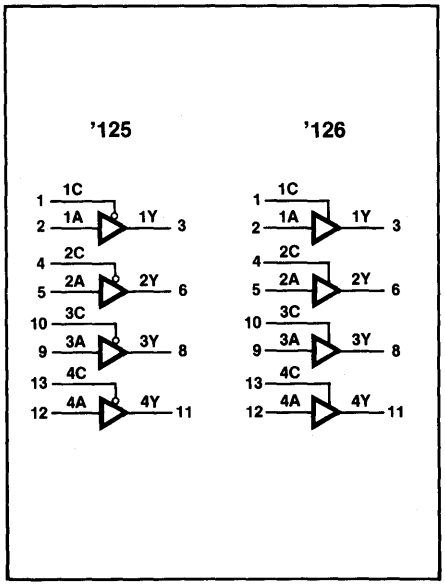
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	30LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL} and, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

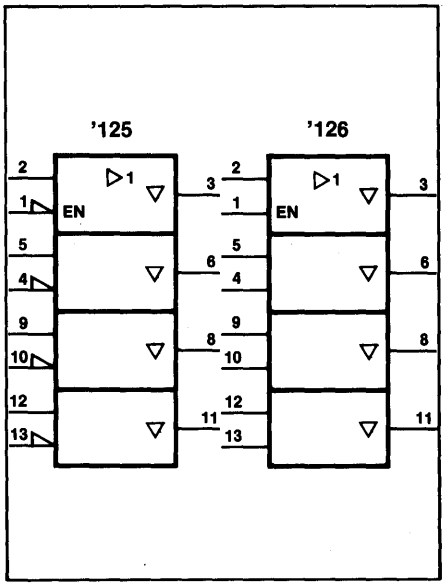
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

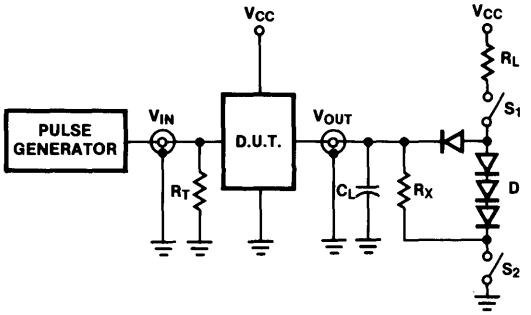
PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0			−1.0	mA
		Com'l			−5.2			−2.6	mA
I_{OL}	LOW-level output current	Mil			16			12	mA
		Com'l			16			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



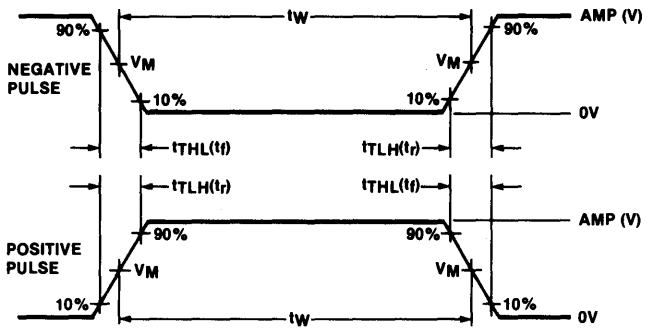
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

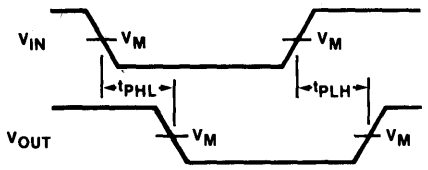
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74125 54/74126			54/74LS125 54/74LS126			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.3		2.4			V
				Com'l	2.4	3.1		2.4			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4		0.25	0.4	V
				Com'l			0.4		0.35	0.5	V
			I_{OL} = 12mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 2.4V					40			20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 0.4V					– 40			– 20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 30		– 70	– 40		– 130	mA
				Com'l	– 28		– 70	– 40		– 130	mA
I_{CC}	Supply current (total)	V_{CC} = MAX		'125		32	54		11	20	mA
				'126		36	62		12	22	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

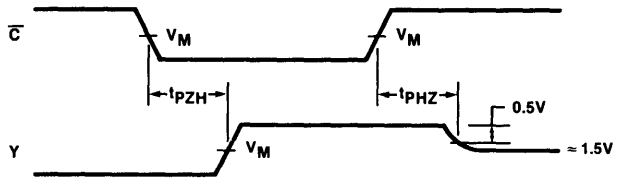
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

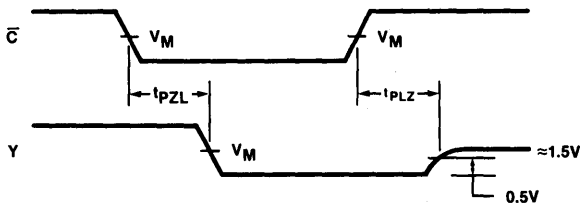
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74125 $C_L = 50pF$ $R_L = 400\Omega$		54/74LS125 $C_L = 45pF$ $R_L = 667\Omega$		54/74126 $C_L = 50pF$ $R_L = 400\Omega$		54/74LS126 $C_L = 45pF$ $R_L = 667\Omega$		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		13 18		15 18		13 18		15 18	ns
t_{PZH}	Enable to HIGH	Waveform 2		17		20		18		25	ns
t_{PZL}	Enable to LOW	Waveform 3		25		25		25		35	ns
t_{PHZ}	Disable from HIGH	Waveform 2, $C_L = 5pF$		8.0		20		16		25	ns
t_{PLZ}	Disable from LOW	Waveform 3, $C_L = 5pF$		12		20		18		25	ns

'240 Octal Inverter Buffer (3-State)
'241 Octal Buffer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS240	11ns	24mA
74S240	4.5ns	93mA
74LS241	12ns	25mA
74S241	6ns	112mA

FUNCTION TABLE, '240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

FUNCTION TABLE, '241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ORDERING CODE

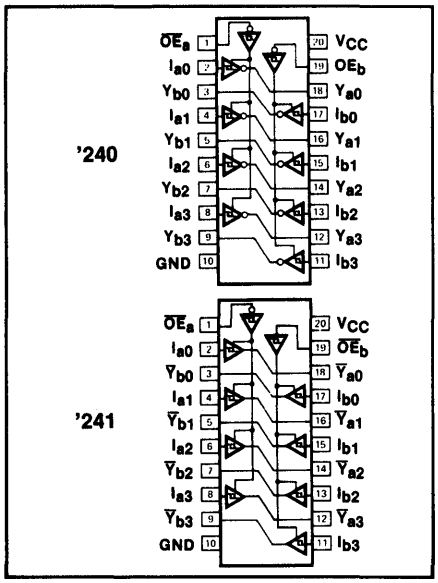
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS240N • N74S240N N74LS241N • N74S241N	
Ceramic DIP	N74LS240F • N74S240F N74LS241F • N74S241F	S54LS240F • S54S240F S54LS241F • S54S241F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

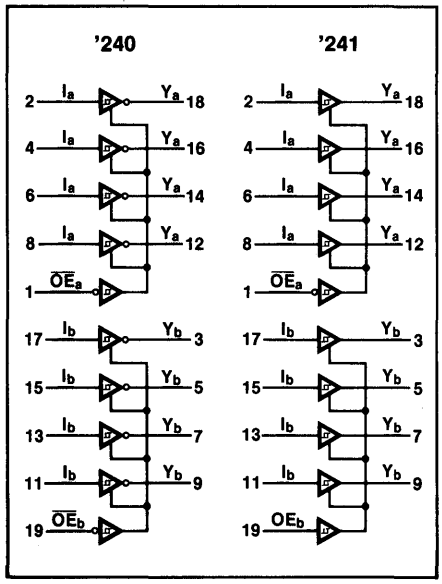
PINS	DESCRIPTION	54/74S	54/74LS
I_{a0}–I_{a3}, I_{b0}–I_{b3}	Inputs	1Sul	1LSul
$\overline{OE}_a$, $\overline{OE}_b$, OE_b	Inputs	1Sul	1LSul
All	Outputs	24Sul	32LSul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

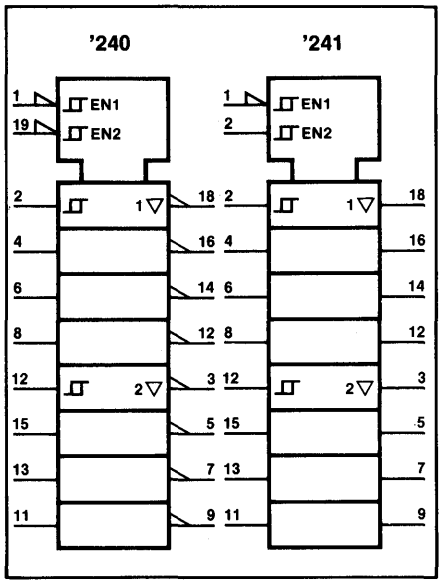
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

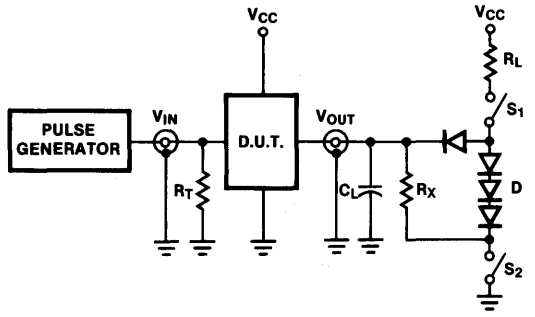
PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−12			−12	mA
		Com'l			−15			−15	mA
I_{OL}	LOW-level output current	Mil			12			48	mA
		Com'l			24			64	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C
External resistance between any input or V_{CC} and ground								40	kΩ

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



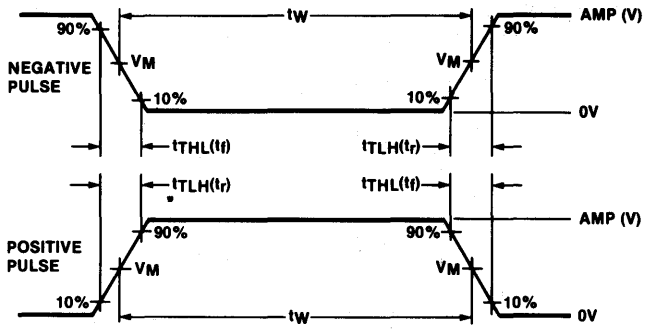
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]				54/74LS240, 241			54/74S240, 241			UNIT
						Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN				0.2	0.4		0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V, I_{OH} = MAX				2.0			2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = −3mA			2.4	3.4		2.4	3.4		V
			I_{OH} = −1mA	74S					2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil				0.4			0.55	V
				Com'l				0.5			0.55	V
			I_{OL} = 12mA	74LS				0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$						−1.5			−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX	V_O = 2.4V								50	μA
			V_O = 2.7V					20				μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX	V_O = 0.4V					−20				μA
			V_O = 0.5V								−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V								1.0	mA
			V_I = 7.0V					0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V						20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V					−0.2				mA
			V_I = 0.5V	I_{a0}–I_{a3}, I_{b0}–I_{b3} inputs							−400	μA
				$\overline{OE_a}$, $\overline{OE_b}$, OE_b inputs							−2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX				−40		−130	−50		−225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	'LS240	Mil & Com'l		17	27				mA
			I_{CCL}				26	44				mA
			I_{CCZ}				29	50				mA
			I_{CCH}	'LS241	Mil & Com'l		17	27				mA
			I_{CCL}				27	46				mA
			I_{CCZ}				32	54				mA
			I_{CCH}	'S240	Mil					80	123	mA
					Com'l					80	135	mA
			I_{CCL}		Mil					100	145	mA
					Com'l					100	150	mA
			I_{CCZ}		Mil					100	145	mA
					Com'l					100	150	mA
			I_{CCH}	'S241	Mil					95	147	mA
					Com'l					95	160	mA
			I_{CCL}		Mil					120	170	mA
					Com'l					120	180	mA
			I_{CCZ}		Mil					120	170	mA
					Com'l					120	180	mA

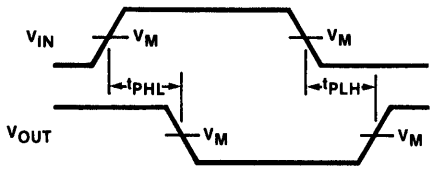
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and $V_{CC} = V_{CC}$ MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS		54LS/74LS $C_L = 45pF$, $R_L = 667\Omega$ Min	54LS/74LS $C_L = 45pF$, $R_L = 667\Omega$ Max	54S/74S $C_L = 50pF$, $R_L = 90\Omega$ Min	54S/74S $C_L = 50pF$, $R_L = 90\Omega$ Max	UNIT
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '240			14 18		7 7	ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '241			18 18		9 9	ns
t_{PZH}	Enable to HIGH	Waveform 3	LS		23			
			'S240				10	ns
			'S241				12	
t_{PZL}	Enable to LOW	Waveform 4			30		15	ns
t_{PHZ}	Disable from HIGH	Waveform 3, $C_L = 5pF$			18		9	ns
t_{PLZ}	Disable from LOW	Waveform 4, $C_L = 5pF$			25		15	ns

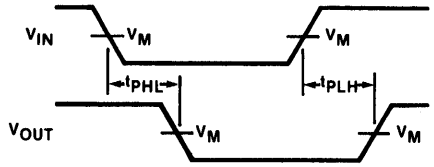
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



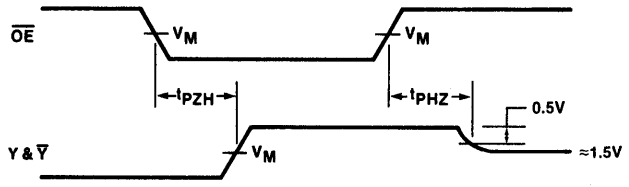
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



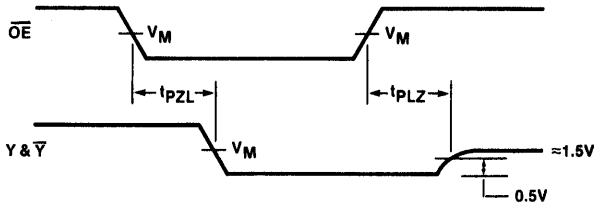
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

$V_M = 1.3V$ for 54LS/74LS, $V_M = 1.5V$ for all other TTL families.

'242 Quad Inverting Transceiver (3-State)
'243 Quad Transceiver (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURENT (Total)
74LS242	10ns	27mA
74LS243	12ns	28mA

FUNCTION TABLE, '242

INPUTS		INPUT/OUTPUT	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	$B = \overline{A}$
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	$A = \overline{B}$	INPUT

FUNCTION TABLE, '243

INPUTS		INPUT/OUTPUT	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	B = A
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	A = B	INPUT

H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance (off) state
(a) = This condition is not allowed due to excessive currents.

ORDERING CODE

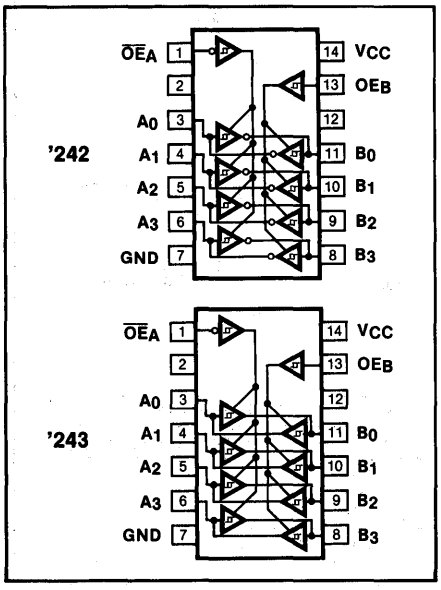
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS242N • N74LS243N	
Ceramic DIP	N74LS242F • N74LS243F	S54LS242F • S54LS243F
Flatpack		S54LS242W • S54LS243W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

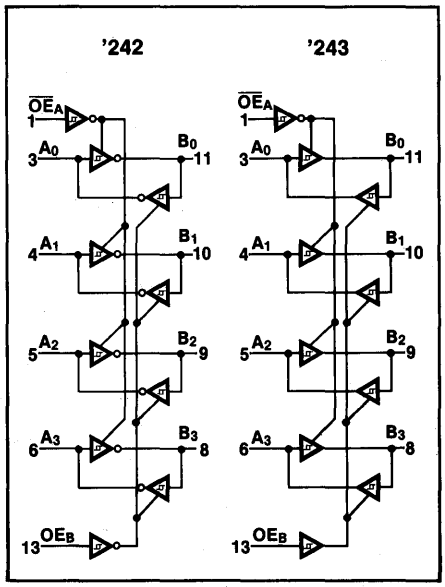
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
A, B	Outputs	30LSul

NOTE
Where a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

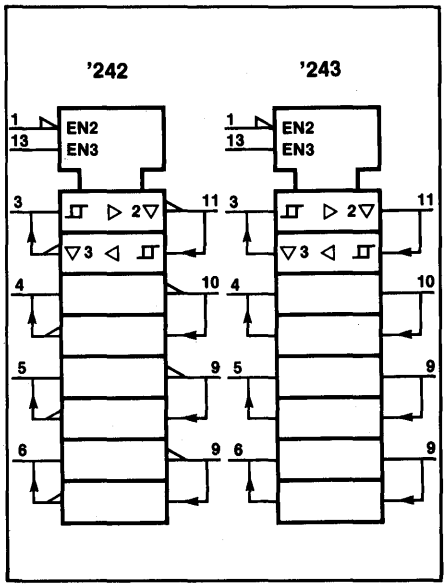
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

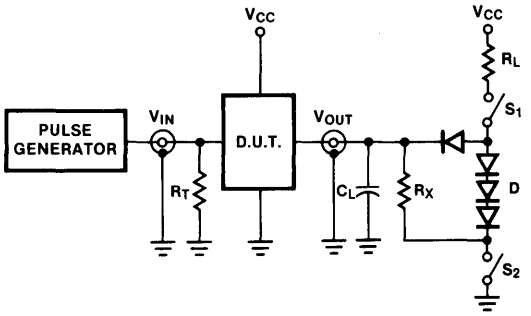
NOTE
V_{IN} limited to +5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

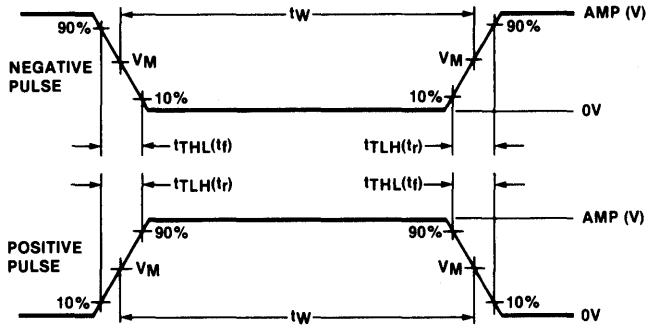


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS242 54/74LS243			UNIT
					Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN			0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V, I_{OH} = MAX			2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = −3mA			2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 2.7V					40	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 0.4V					−200	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A, B inputs			0.1	mA
			V_I = 7.0V	$\overline{OE}_A$, OE_B inputs			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	A inputs $\overline{OE}_A$, OE_B = V_{IL} = MAX				−0.2	mA
			B inputs $\overline{OE}_A$, OE_B = V_{IH} = MIN				−0.2	mA
			$\overline{OE}_A$, OE_B inputs				−0.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH	'242		22	38	mA
			I_{CCL}	Outputs LOW			29	50	mA
			I_{CCZ}	Outputs OFF			29	50	mA
			I_{CCH}	Outputs HIGH	'243		22	38	mA
			I_{CCL}	Outputs LOW			29	50	mA
			I_{CCZ}	Outputs OFF			32	54	mA

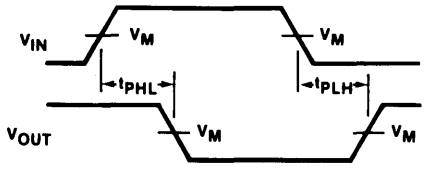
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open and transceivers enabled in one direction only, or with all transceivers disabled.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS242 C_L = 45pF, R_L = 667Ω		54/74LS243 C_L = 45pF, R_L = 667Ω		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		14 18			ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2				18 18	ns
t_{PZH}	Enable to HIGH	Waveform 3		23		23	ns
t_{PZL}	Enable to LOW	Waveform 4		30		30	ns
t_{PHZ}	Disable from HIGH	Waveform 3, C_L = 5pF		18		18	ns
t_{PLZ}	Disable from LOW	Waveform 4, C_L = 5pF		25		25	ns

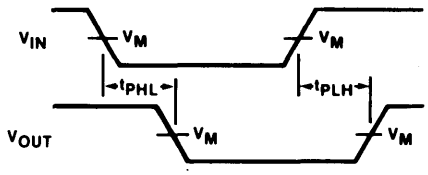
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

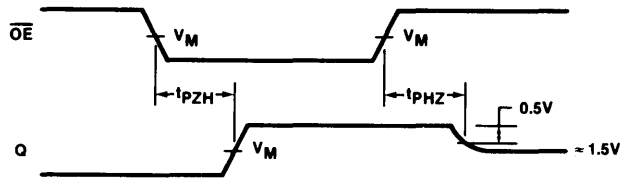
WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 2

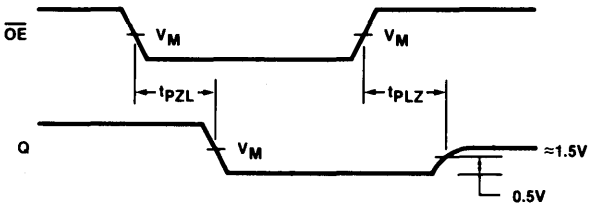
V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

Octal Buffers (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS244	12ns	25mA
74S244	6ns	112mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS244N • N74S244N	
Ceramic DIP	74LS244F • N74S244F	S54LS244F • S54S244F

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

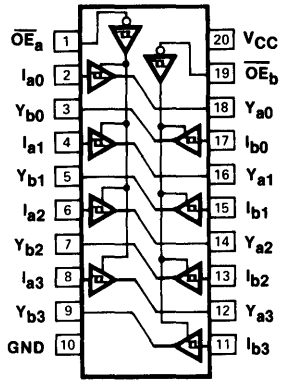
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

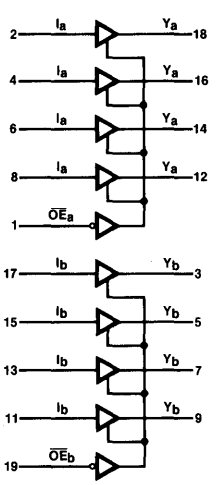
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1SuI	1LSuI
All	Outputs	24SuI	30LSuI

NOTE
A 54/74S unit load (SuI) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSuI) is 20μA I_{IH} and −0.4mA I_{IL}.

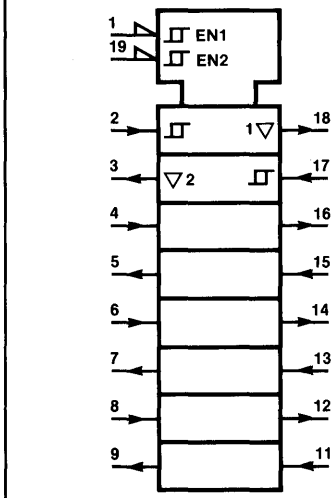
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

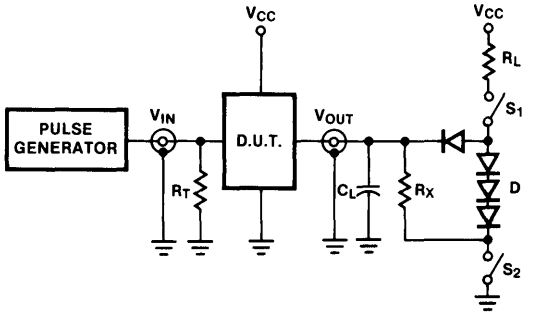
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−12			−12	mA
		Com'l			−15			−15	mA
I_{OL}	LOW-level output current	Mil			12			48	mA
		Com'l			24			64	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

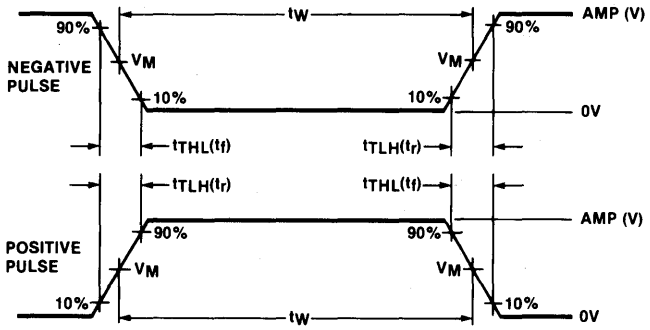


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS244			54/74S244			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V, I_{OH} = MAX			2.0			2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = −3mA			2.4	3.4		2.4			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4			0.55	V
				Com'l			0.5			0.55	V
			I_{OL} = 12mA	74LS			0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX	V_O = 2.7V				20				μA
			V_O = 2.4V							50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX	V_O = 0.4V				-20				μA
			V_O = 0.5V							-50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				-0.2				mA
			V_I = 0.5V	$\overline{OE}$ inputs						-2.0	mA
				Other inputs						-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-130	-50		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH	Mil		17	27		95	147	mA
				Com'l		17	27		95	160	mA
			I_{CCL} Outputs LOW	Mil		27	46		120	170	mA
				Com'l		27	46		120	180	mA
			I_{CCZ} Outputs OFF	Mil		32	54		120	170	mA
				Com'l		32	54		120	180	mA

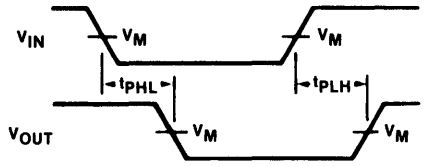
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
			C_L = 45pF, R_L = 667Ω		C_L = 50pF, R_L = 90Ω		
			Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1		18		9	ns
t_{PHL}	Propagation delay	Waveform 1		18		9	ns
t_{PZH}	Enable to HIGH	Waveform 2		23		12	ns
t_{PZL}	Enable to LOW	Waveform 3		30		15	ns
t_{PHZ}	Disable from HIGH	Waveform 2, C_L = 5pF		18		9	ns
t_{PLZ}	Disable from LOW	Waveform 3, C_L = 5pF		25		15	ns

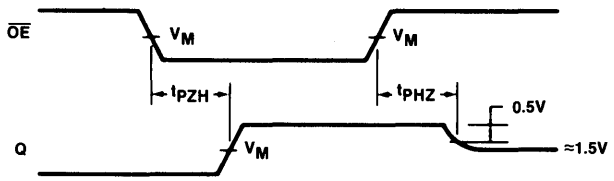
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



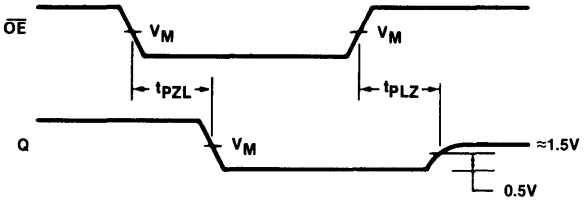
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

TRANSCEIVER 54/74LS245

Octal Transceiver (3-State)

- **Octal bidirectional bus interface**
- **3-State buffer outputs**
- **PNP inputs for reduced loading**
- **Hysteresis on all inputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS245	8ns	58mA

DESCRIPTION

The 'LS245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable (CE) input for easy cascading and a Send/Receive (S/R) input for direction control. All inputs have hysteresis built in to minimize ac noise effects.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS245N	
Ceramic DIP	N74LS245F	S54LS245F
Flatpack		

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUT	B = A
H	X	(Z)	(Z)

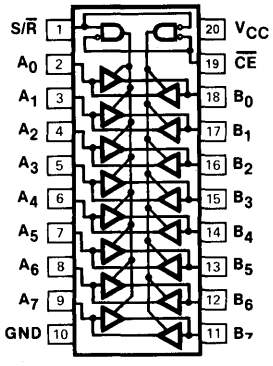
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

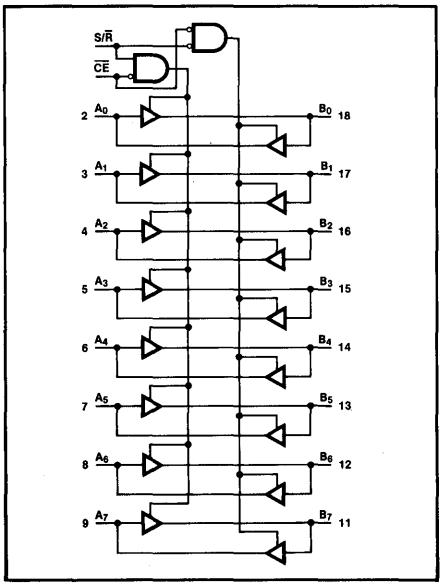
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

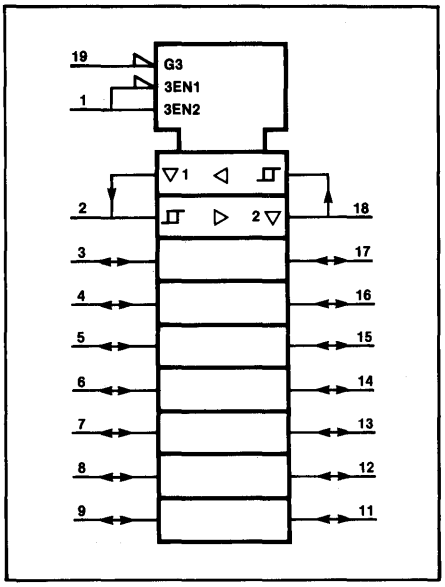
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

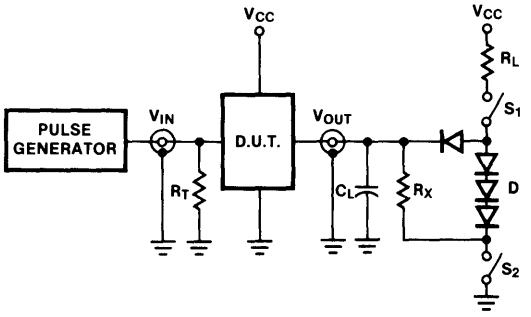
NOTE
V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

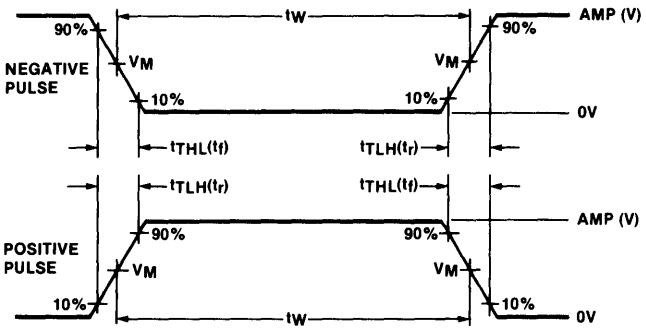


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

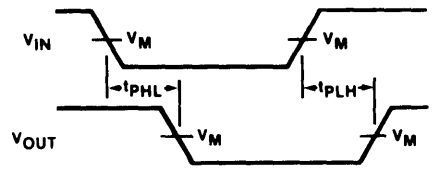
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS245 Min	54/74LS245 Typ[2]	54/74LS245 Max	UNIT
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN			0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX		2.0			V
			I_{OH} = −3mA		2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4	V
				Com'l			0.5	V
			I_{OL} = 12mA	74LS			0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.7V, $\overline{CE}$ = 2.0V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.4V, $\overline{CE}$ = 2.0V					−200	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A, B inputs			0.1	mA
			V_I = 7.0V	S/$\overline{R}$, $\overline{CE}$ inputs			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−0.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		48	70	mA
			I_{CCL}	Outputs LOW		62	90	mA
			I_{CCZ}	Outputs OFF		64	95	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open.

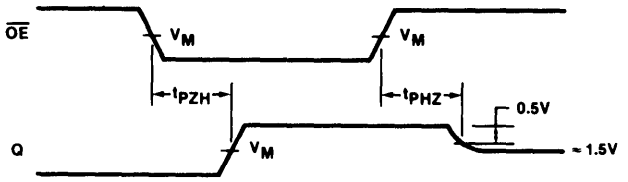
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

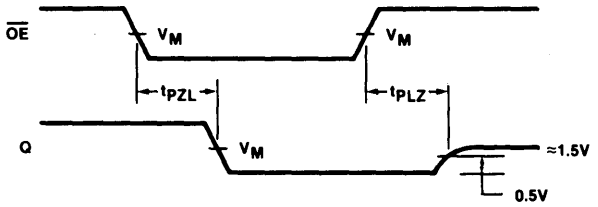
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			$C_L = 45pF$, $R_L = 667\Omega$		
			Min	Max	
t_{PLH}	Propagation delay	Waveform 1		12	ns
t_{PHL}	Propagation delay	Waveform 1		12	ns
t_{PZH}	Enable to HIGH	Waveform 2		40	ns
t_{PZL}	Enable to LOW	Waveform 3		40	ns
t_{PHZ}	Disable from HIGH	Waveform 2, $C_L = 5pF$		25	ns
t_{PLZ}	Disable from LOW	Waveform 3, $C_L = 5pF$		25	ns

Octal D Flip-Flops

- **Ideal buffer for MOS microprocessor or memory**
- **Eight edge-triggered D flip-flops**
- **High speed Schottky version available**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**
- **Slim 20-pin plastic and ceramic DIP packages**
- **See '377 for Clock Enable version**
- **See '373 for transparent latch version**
- **See '374 for 3-state version**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS273	40MHz	17mA
74S273	95MHz	109mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S273N • N74LS273N	
Ceramic DIP	N74S273F • N74LS273F	S54LS273F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

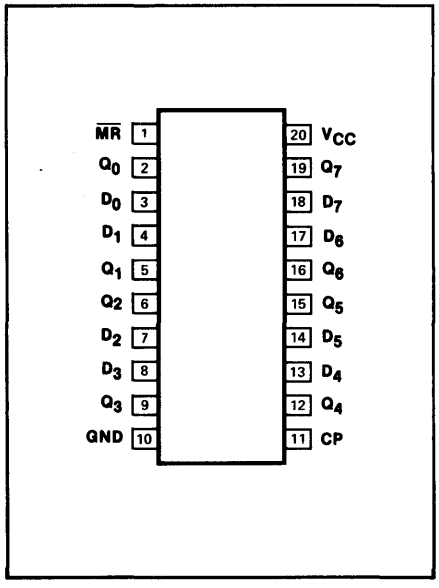
DESCRIPTION

The '273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

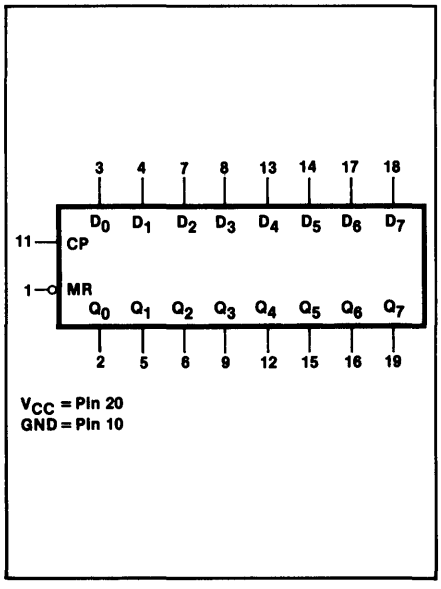
The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

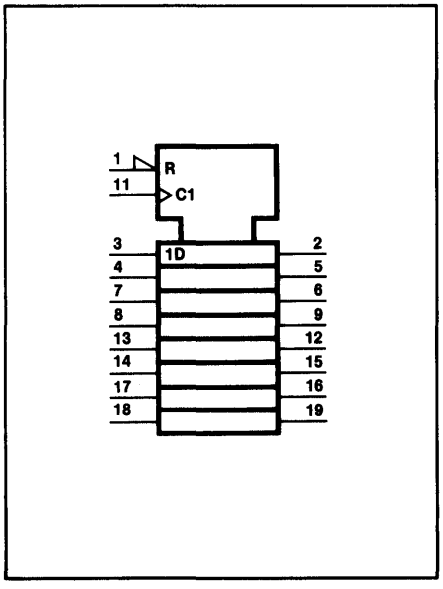
PIN CONFIGURATION



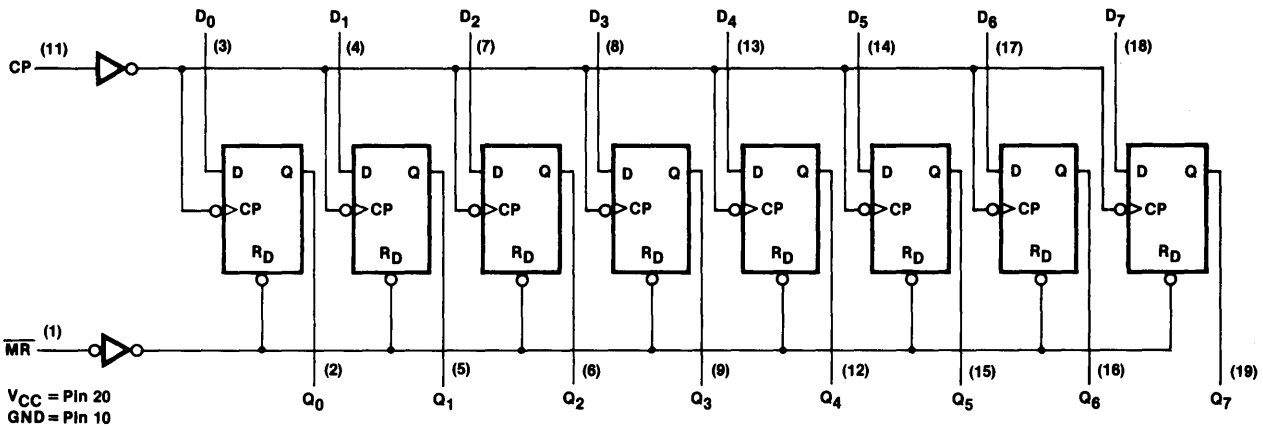
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT--FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current				−400			−1000	μA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS273			54/74S273			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		2.5			V
				Com'l	2.7	3.4		2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 0.4				mA
			V_I = 0.5V							– 2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				17	27		109	150	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} after a momentary ground, then 4.5V is applied to clock with all outputs open and 4.5V applied to all Data inputs and the Master Reset input.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
			C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 27		15 15	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		27		15	ns

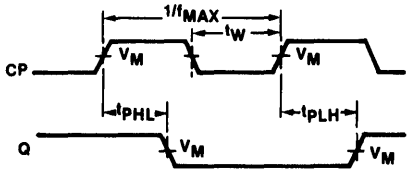
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_f, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
			Min	Max	Min	Max	
t_W(L)	Clock pulse width (LOW)	Waveform 1	20		7.0		ns
t_W	Master Reset pulse width	Waveform 2	20		10		ns
t_s(H)	Setup time, HIGH data to CP	Waveform 3	20		5.0		ns
t_h(H)	Hold time, HIGH data to CP	Waveform 3	5.0		3.0		ns
t_s(L)	Setup time, LOW data to CP	Waveform 3	20		5.0		ns
t_h(L)	Hold time, LOW data to CP	Waveform 3	5.0		3.0		ns
t_{rec}	Recovery time, MR to CP	Waveform 2	25		5.0		ns

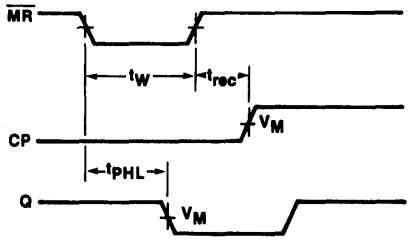
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



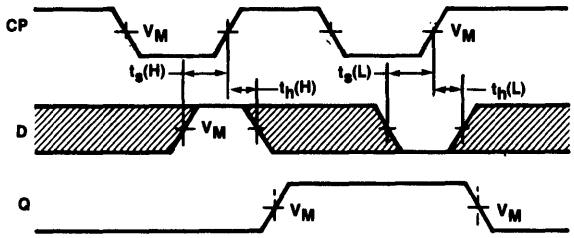
Waveform 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

DATA SET-UP AND HOLD TIMES

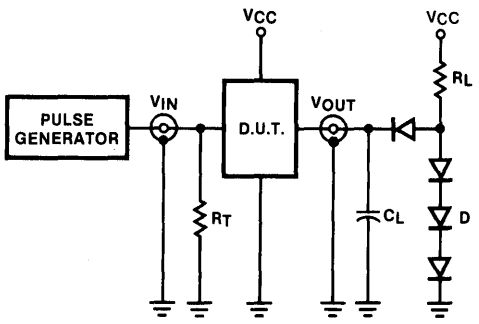


Waveform 3

V_M = 1.5V for 54/74 and 54/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

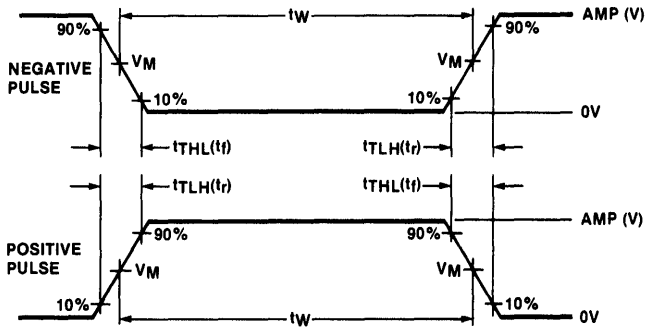
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LATCH 54/74LS363

Octal Transparent Latch With 3-State Outputs

- **8-bit transparent latch**
- **3-State MOS compatible output buffers**
- **Common Latch Enable input with hysteresis**
- **Common 3-state Output Enable control**
- **Independent latch and 3-state buffer operation**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS363	19ns	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS363N	
Ceramic DIP	N74LS363F	S54LS363F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

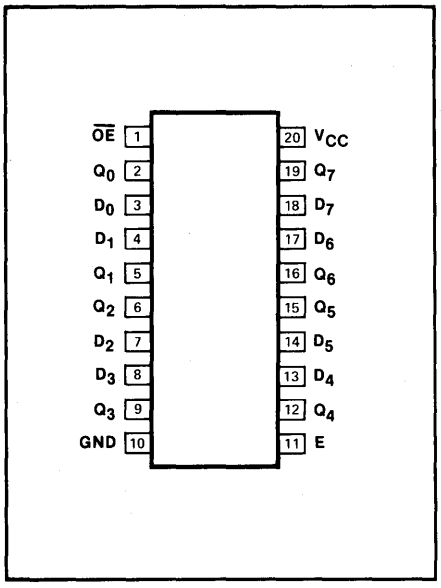
The '363 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the Latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the Data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

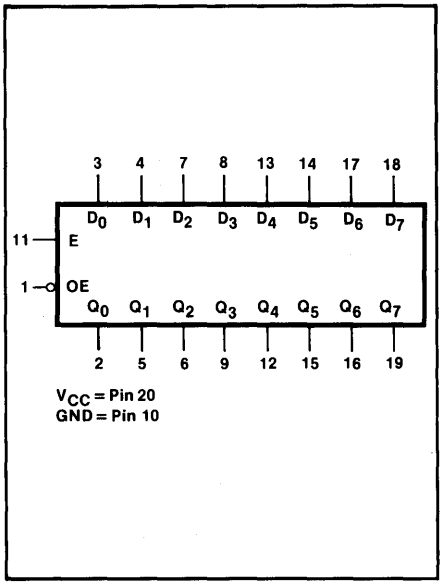
The 3-State output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about 1V closer to V_{CC}, or to over 3.5V at minimum V_{CC}. This feature makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V.

The active LOW Output Enable ($\overline{OE}$) controls all eight 3-state buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

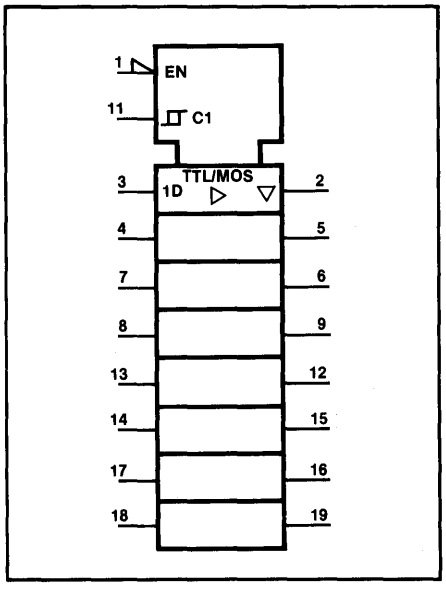
PIN CONFIGURATION



LOGIC SYMBOL

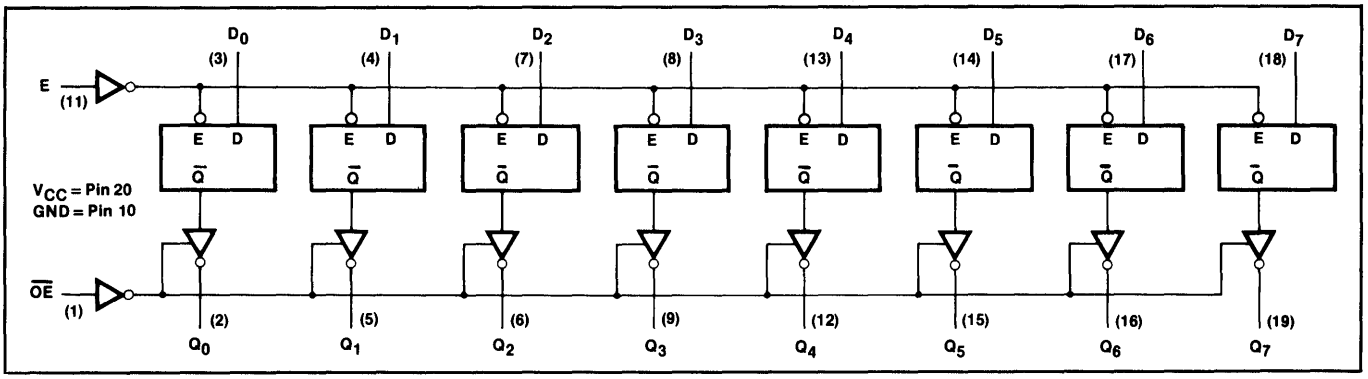


LOGIC SYMBOL (IEEE/IEC)



LATCH 54/74LS363

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0-Q_7
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW enable transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
(Z) = HIGH impedance "off" state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0	mA
		Com'l			−2.6	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS363 Min	54/74LS363 Typ[2]	54/74LS363 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	3.45			V
				Com'l	3.65			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IL} = MAX, V_O = 3.65V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.4V					– 20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 30		– 130	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, $\overline{OE}$ = 4.5V				42	70	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

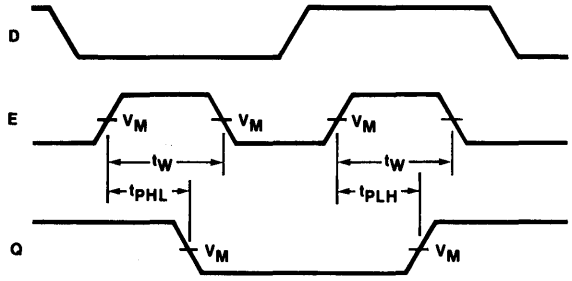
PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 45pF, R_L = 667Ω Min	54LS/74LS C_L = 45pF, R_L = 667Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1		30 36	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4		23 27	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		28	ns
t_{PZL}	Enable time to LOW level	Waveform 3		36	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		20	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		25	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS Min	54LS/74LS Max	UNIT
t_W	Latch Enable pulse width	Waveform 1	15		ns
t_s	Setup time, Data to Latch Enable	Waveform 5	0		ns
t_h	Hold time, Data to Latch Enable	Waveform 5	10		ns

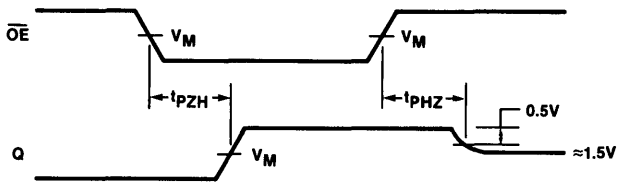
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



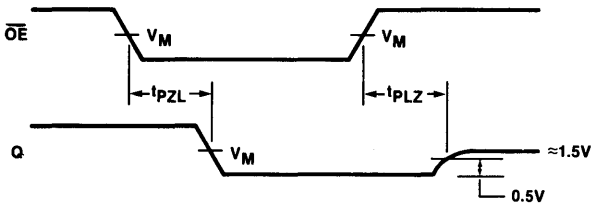
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



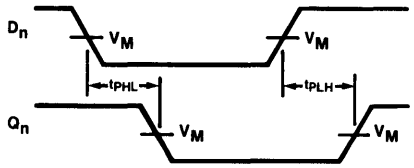
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



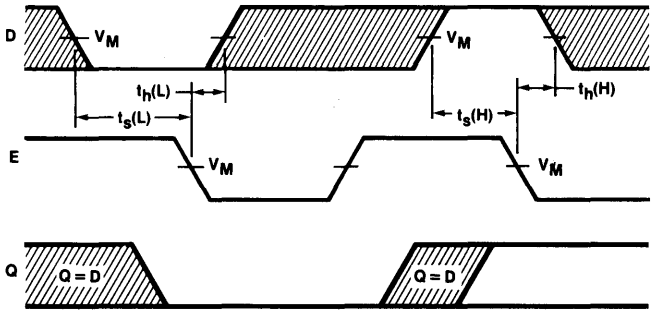
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



Waveform 4

DATA SETUP AND HOLD TIMES



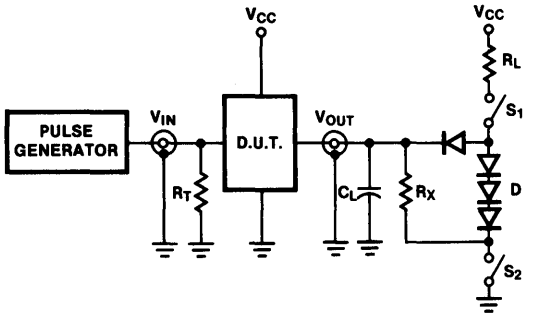
Waveform 5

V_M= 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



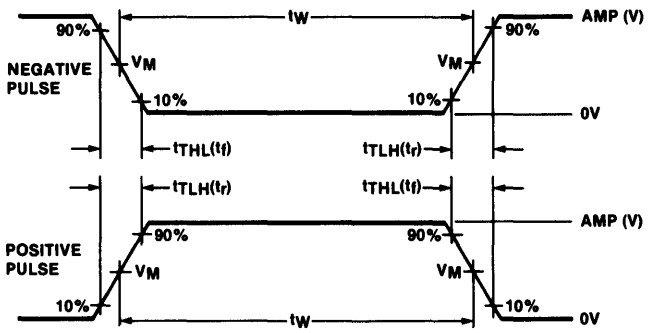
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal D Flip-Flop With 3-State Outputs

- 8-bit positive edge-triggered register
- 3-State MOS compatible output buffers
- Common Clock input with hysteresis
- Common 3-state Output Enable control
- Independent register and 3-state buffer operation

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS364	50MHz	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS364N	
Ceramic DIP	N74LS364F	S54LS364F

DESCRIPTION

The '364 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

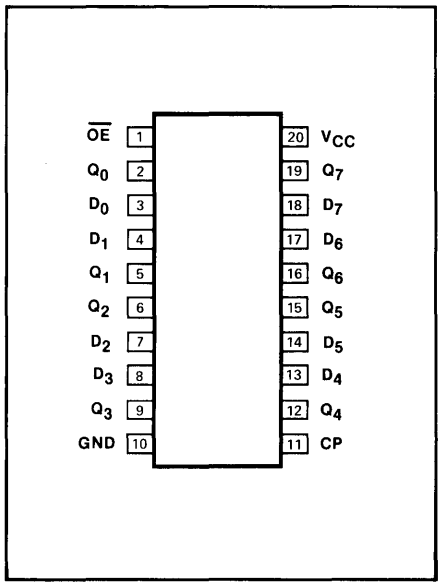
The 3-State output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about 1V closer to V_{CC}, or to over 3.5V at minimum V_{CC}. This feaure makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-state buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

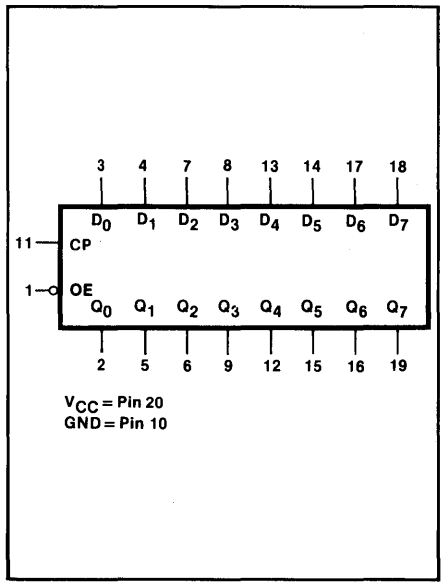
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

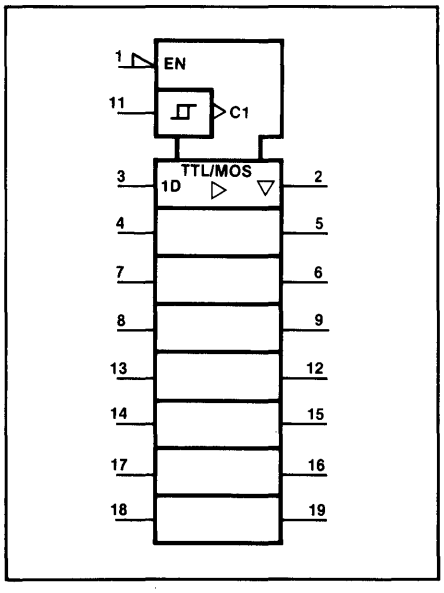
PIN CONFIGURATION



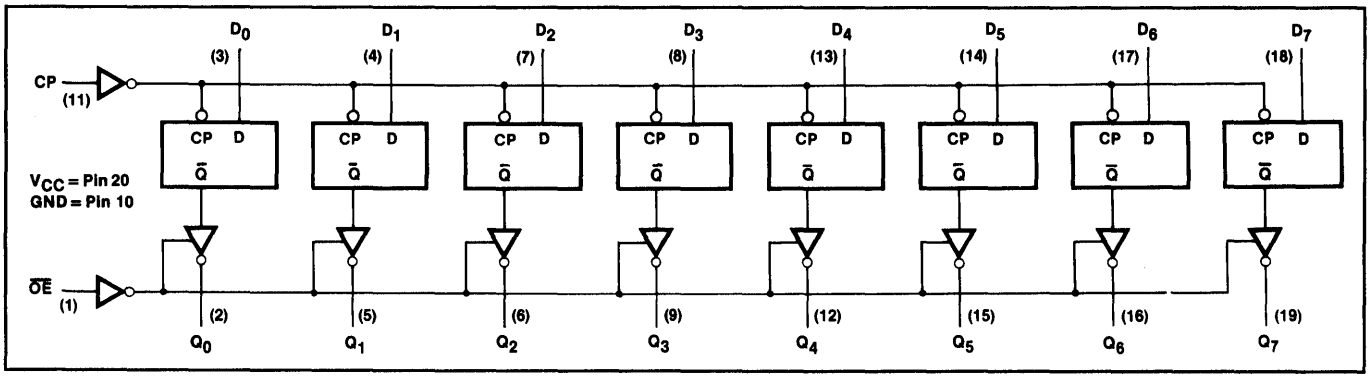
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Latch register and disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0	mA
		Com'l			−2.6	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS364 Min	54/74LS364 Typ[2]	54/74LS364 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	3.45			V
				Com'l	3.65			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IL} = MAX, V_O = 3.65V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.4V					– 20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 30		– 130	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, $\overline{OE}$ = 4.5V				42	70	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 45pF, R_L = 667Ω Min	54LS/74LS C_L = 45pF, R_L = 667Ω Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 1	35		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		33 34	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		28	ns
t_{PZL}	Enable time to LOW level	Waveform 3		36	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		18	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		24	ns

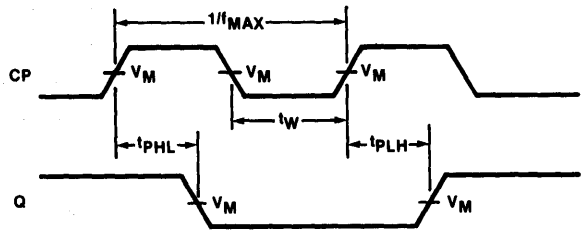
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS Min	54LS/74LS Max	UNIT
t_W	Clock pulse width	Waveform 1	15		ns
t_s	Setup time, Data to clock	Waveform 4	20		ns
t_h	Hold time, Data to clock	Waveform 4	0		ns

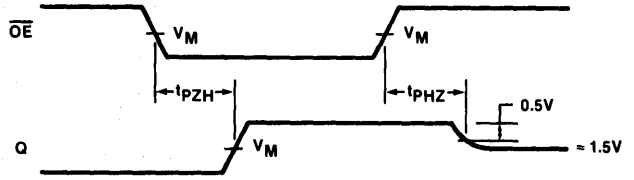
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



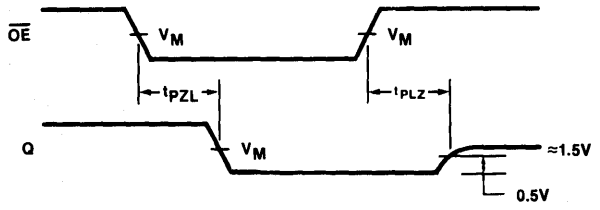
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



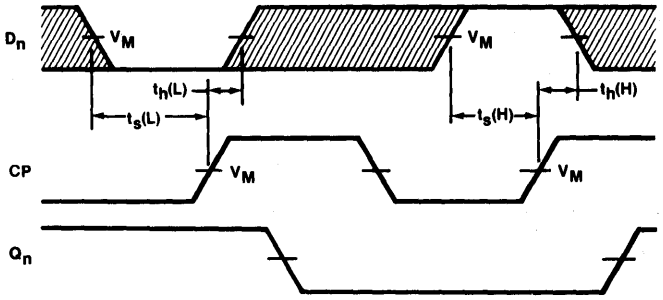
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

DATA SETUP AND HOLD TIMES



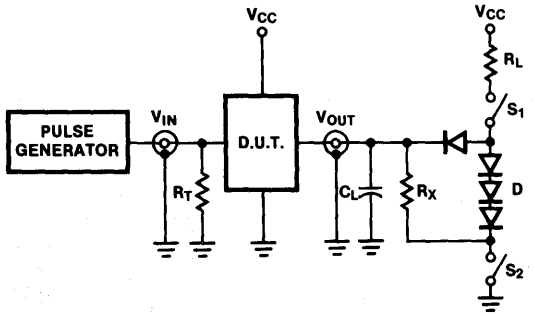
Waveform 4

V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



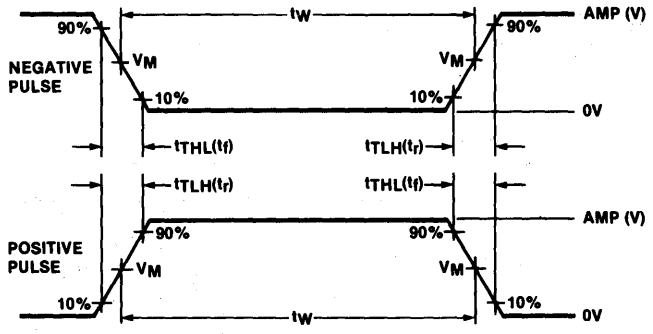
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

'365A, '367A Hex Buffer/Driver (3-State)
'366A, '368A Hex Inverter Buffer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74365A, 367A	10ns	65mA
74LS365A, 367A	10ns	14mA
74366A, 368A	9ns	59mA
74LS366A, 368A	10ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74365AN • N74LS365AN N74366AN • N74LS366AN N74367AN • N74LS367AN N74368AN • N74LS368AN	
Ceramic DIP	N74365AF • N74LS365AF N74366AF • N74LS366AF N74367AF • N74LS367AF N74368AF • N74LS368AF	S54365AF • S54LS365AF S54366AF • S54LS366AF S54367AF • S54LS367AF S54368AF • S54LS368AF
Flatpack		S54365AW • S54LS365AW S54366AW • S54LS366AW S54367AW • S54LS367AW S54368AW • S54LS368AW

FUNCTION TABLE, '365A, '366A

INPUTS			OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I	Y	$\overline{Y}$
L	L	L	L	H
L	L	H	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

FUNCTION TABLE, '367A, '368A

INPUTS		OUTPUTS	
$\overline{OE}$	I	Y	$\overline{Y}$
L	L	L	H
L	H	H	L
H	X	(Z)	(Z)

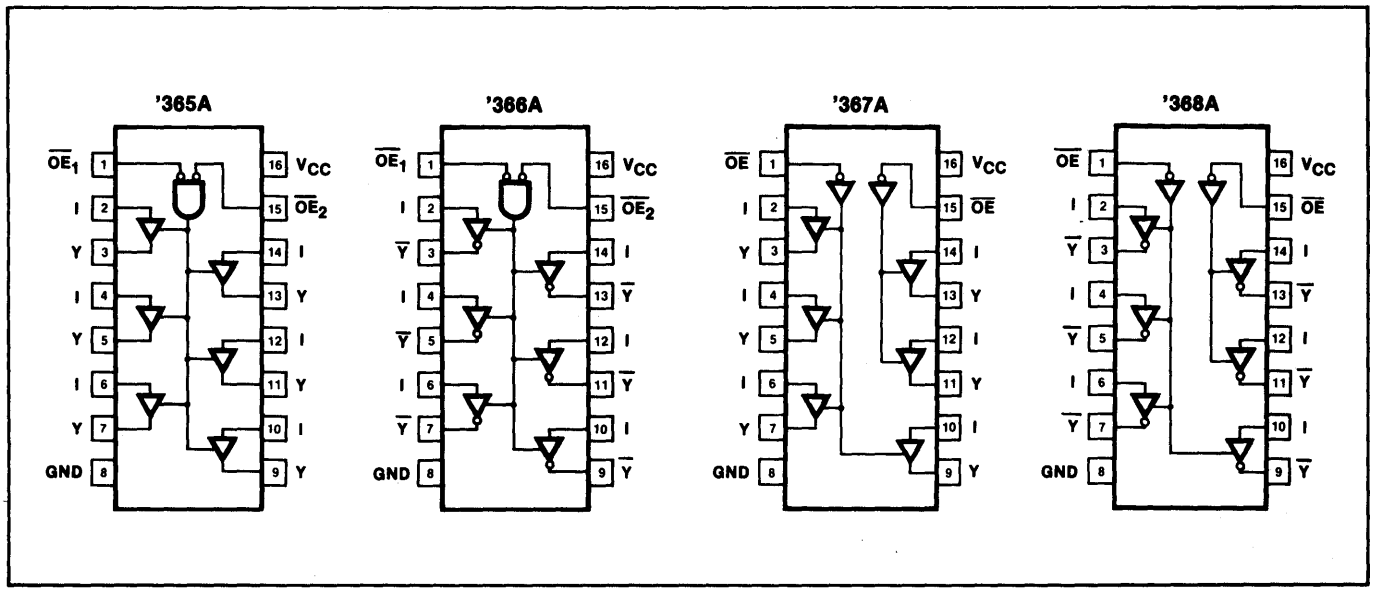
L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

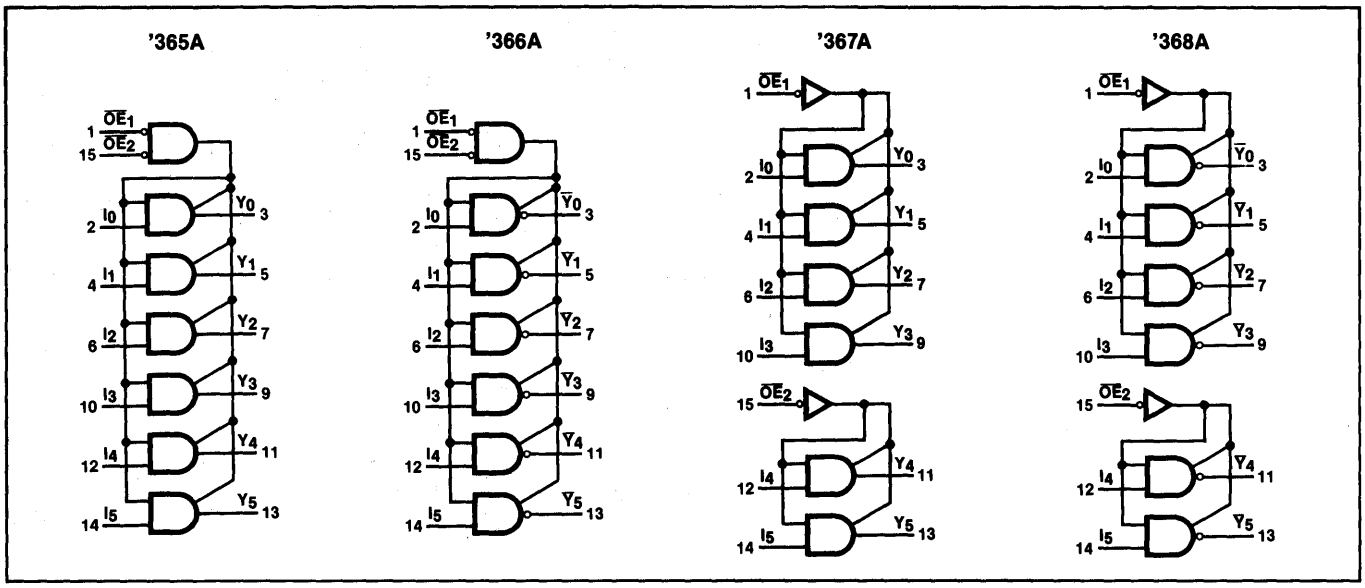
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	20ul	30LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.0mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA

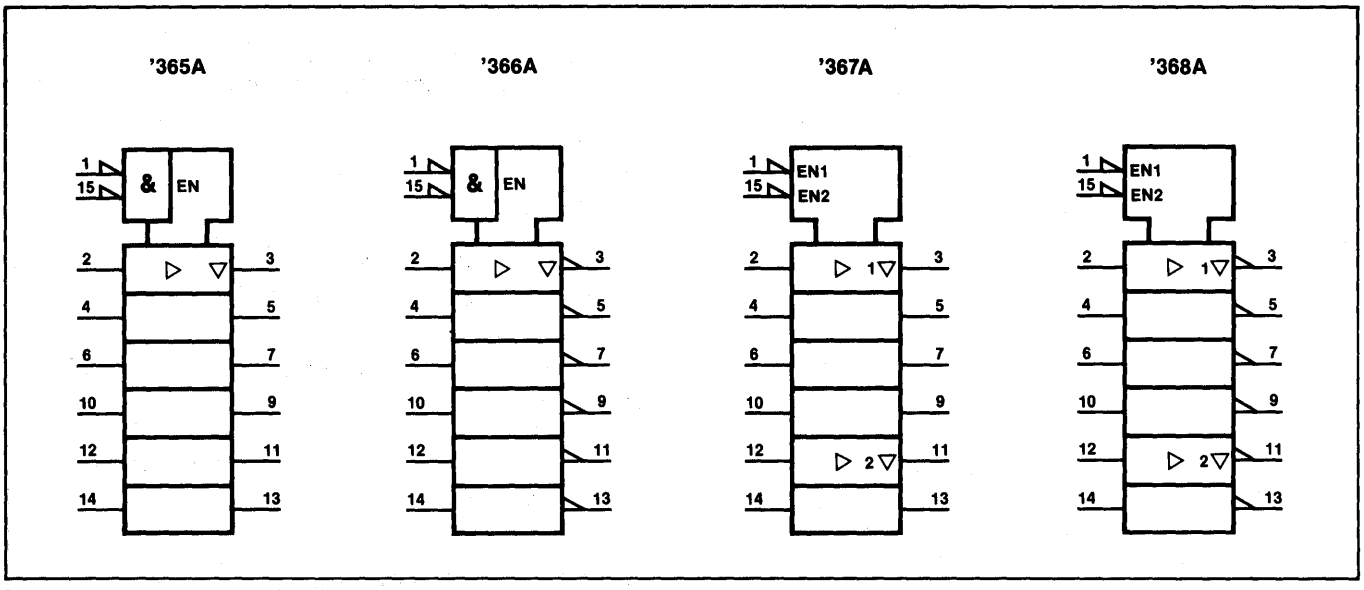
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

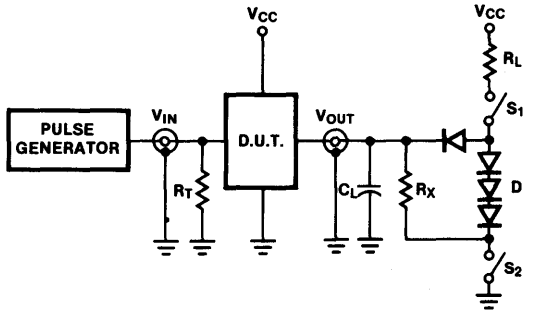
	PARAMETER	54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0			−1.0	mA
		Com'l			−5.2			−2.6	mA
I_{OL}	LOW-level output current	Mil			32			12	mA
		Com'l			32			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

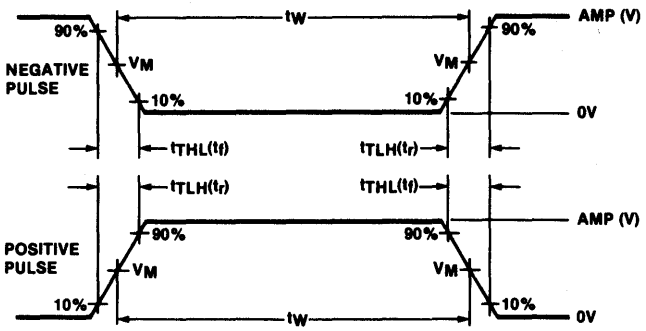


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74365A, '366A, '367A, '368A			54/74LS365A, '366A, '367A, '368A			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.3		2.4	3.3		V
				Com'l	2.4	3.1		2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4		0.25	0.4	V
				Com'l			0.4		0.35	0.5	V
			I_{OL} = 12mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 2.4V					40			20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 0.4V					-40			-20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	I inputs, V_I = 0.5V Either $\overline{OE}$ input at 2.0V Does not apply to 'LS365A or 'LS367A				-40			-20	μA
			I inputs V_I = 0.4V Both $\overline{OE}$ inputs at 0.4V				-1.6			-0.4	mA
			$\overline{OE}$ inputs V_I = 0.4V				-1.6			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-130	-30		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	'365A, '367A			65	85		14	24	mA
			'366A, '368A			59	77		12	21	mA

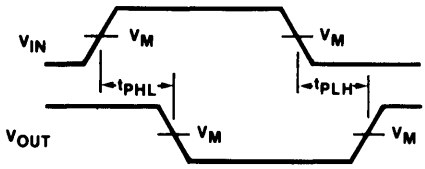
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Data inputs grounded and Output Enable inputs at 4.5V.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS		54/74 C_L = 50pF, R_L = 400Ω		54LS/74LS C_L = 45pF, R_L = 667Ω		UNIT
				Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '366A, '368A			17 16		15 18	ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '365A, '367A			16 22		16 22	ns
t_{PZH}	Enable to HIGH	Waveform 3			35		35	ns
t_{PZL}	Enable to LOW	Waveform 4	'365A, '367A		37		40	ns
			'366A, '368A		37		45	ns
t_{PHZ}	Disable from HIGH	Waveform 3, C_L = 5pF	'365A, '367A		11		30	ns
			'366A, '368A		11		32	ns
t_{PLZ}	Disable from LOW	Waveform 4, C_L = 5pF			27		35	ns

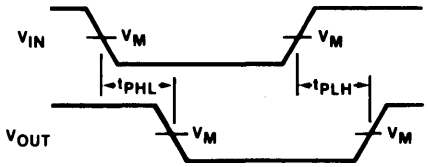
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



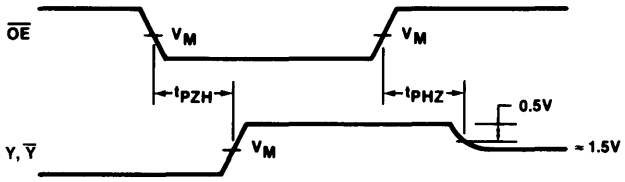
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



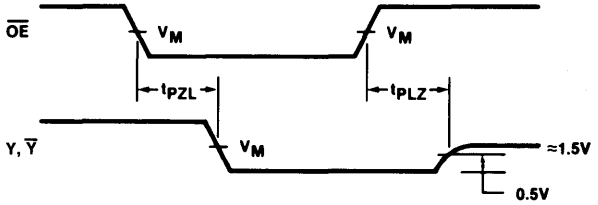
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

'373 Octal Transparent Latch With 3-State Outputs
'374 Octal D Flip-Flop With 3-State Outputs

- **8-bit transparent latch — '373**
- **8-bit positive, edge-triggered register — '374**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS373	19ns	24mA
74S373	10ns	105mA
74LS374	19ns	27mA
74S374	8ns	116mA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

NOTE
Where a 54/74S unit load (Sul) is 50μA I_{IH} and $-$ 2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and $-$ 0.4mA I_{IL}.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic	N74LS373N • N74S373N N74LS374N • N74S374N	
Ceramic DIP	N74LS373F • N74S373F N74LS374F • N74S374F	S54LS373F • S54S373F S54LS374F • S54S374F

DESCRIPTION

The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

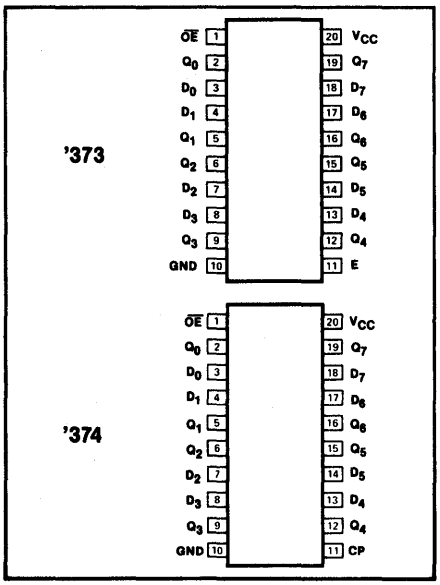
The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

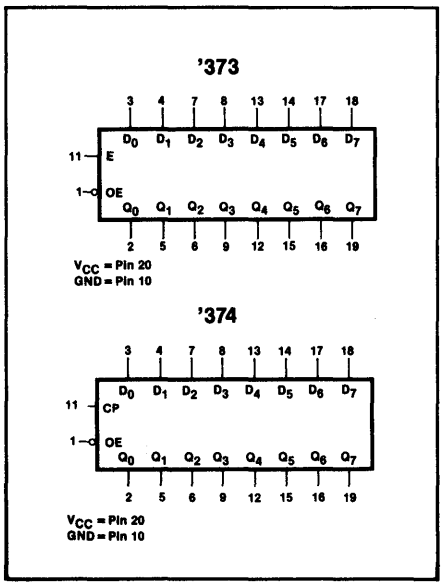
The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

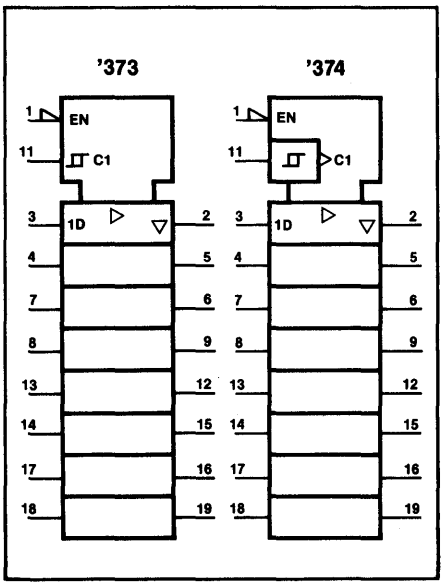
PIN CONFIGURATION



LOGIC SYMBOL

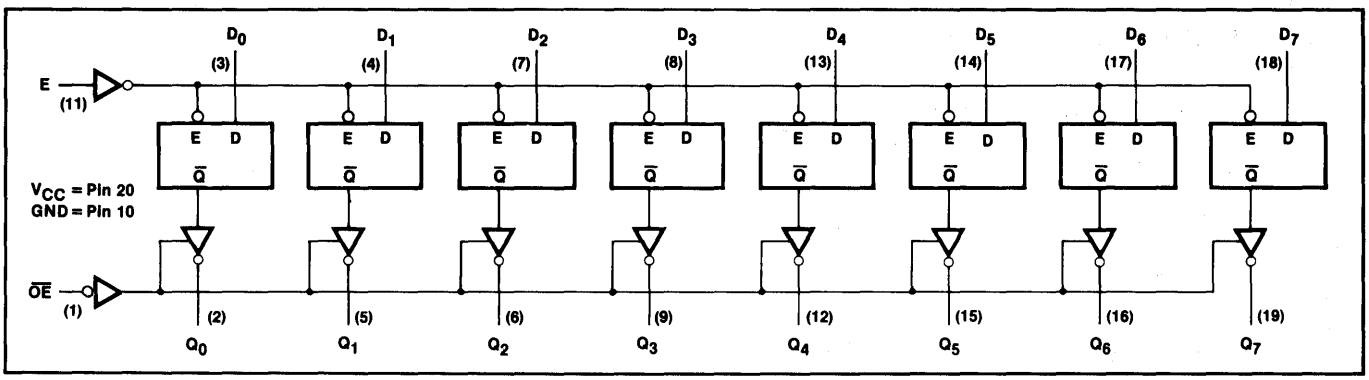


LOGIC SYMBOL (IEEE/IEC)

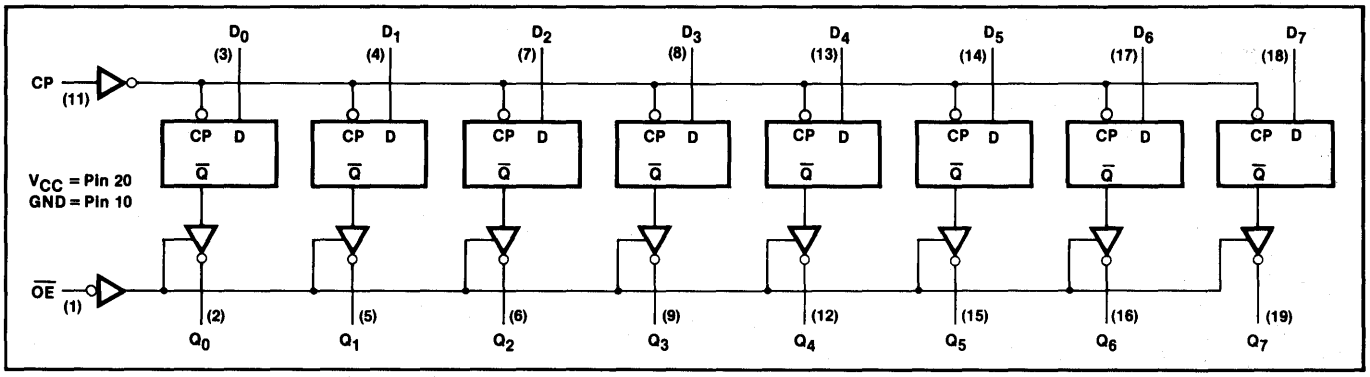


The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



LOGIC DIAGRAM, '374



MODE SELECT—FUNCTION TABLE, '373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0-Q_7
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

MODE SELECT—FUNCTION TABLE, '374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state.	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0			−2.0	mA
		Com'l			−2.6			−6.5	mA
I_{OL}	LOW-level output current	Mil			12			20	mA
		Com'l			24			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS373, 374			54/74S373, 374			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.4	3.0		V
				Com'l	2.4	3.1		2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[4]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5			− 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.7V				20				μA
			V_O = 2.4V							50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 0.4V				− 20				μA
			V_O = 0.5V							− 50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V				0.1				mA
			V_I = 5.5V							1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				− 0.4				mA
			V_I = 0.5V							− 0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			− 30		− 130	− 40		− 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCZ}	$\overline{OE}$ = 4.5V 'LS373		24	40				mA
			I_{CCL}	$\overline{OE}$ = 0V 'S373					105	160	mA
			I_{CCZ}	$\overline{OE}$ = 4.5V 'LS374		27	40				mA
			I_{CCL}	All inputs grounded 'S374					102	140	mA
			I_{CCZ}	CP, $\overline{OE}$ = 4.0V, D inputs = GND 'S374					131	180	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

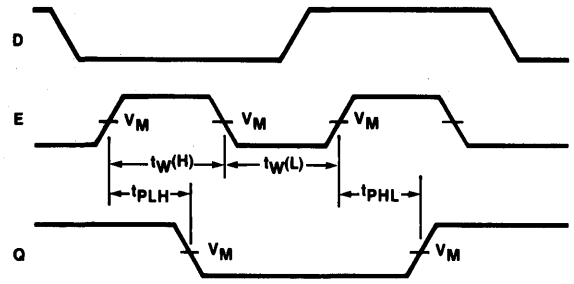
AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			C_L = 45pF, R_L = 667Ω		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, '374	35		75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1, '373		30 30		14 18	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, '373		18 18		9 13	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, '374		28 28		15 17	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		28		15	ns
t_{PZL}	Enable time to LOW level	Waveform 3, '373 '374		36 28		18 18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		20		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		25		12	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

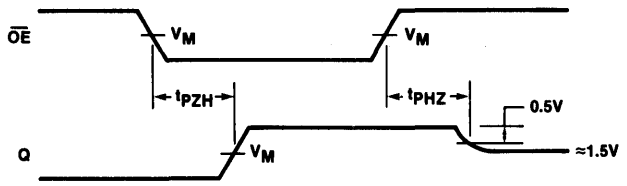
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



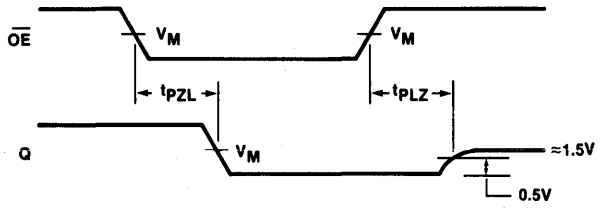
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



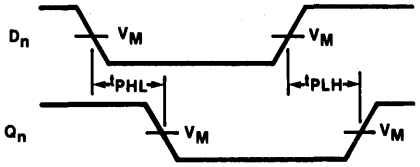
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



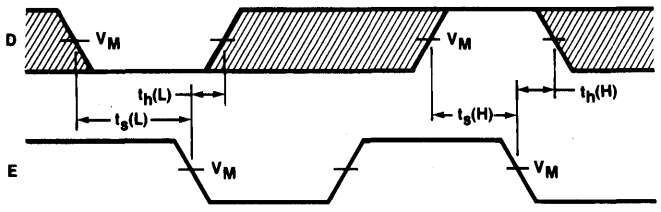
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



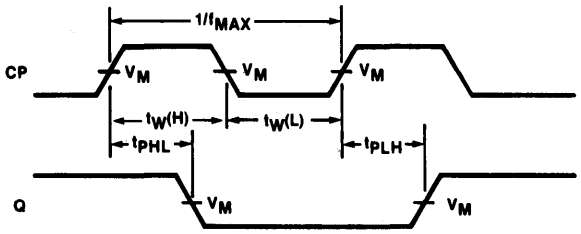
Waveform 4

DATA SETUP AND HOLD TIMES



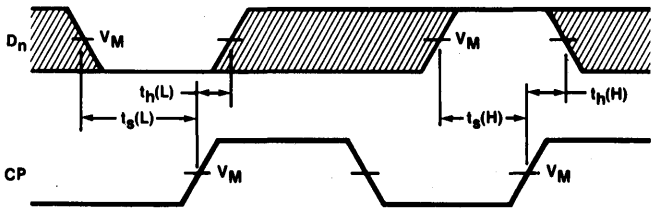
Waveform 5

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

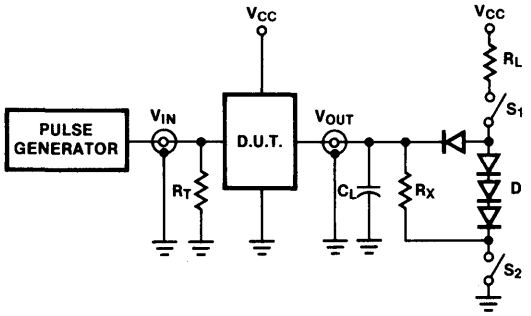
V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			Min	Max	Min	Max	
$t_W(H)$ $t_W(L)$	Latch Enable pulse width	Waveform 1, '373	15 15		6 7.3		ns
t_s	Setup time, Data to Latch Enable	Waveform 5, '373	5		0		ns
t_h	Hold time, Data to Latch Enable	Waveform 5, '373	20		10		ns
$t_W(H)$ $t_W(L)$	Clock pulse width	Waveform 6, '374	15 15		6 7.3		ns
t_s	Setup time, Data to Clock	Waveform 7, '374	20		5		ns
t_h	Hold time, Data to Clock	Waveform 7, '374	0		2		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



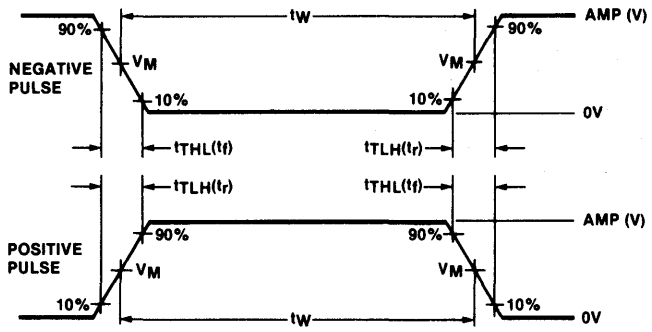
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal D Flip-Flop With Clock Enable

- **Ideal for addressable register applications**
- **Clock Enable for address and data synchronization applications**
- **Eight edge-triggered D flip-flops**
- **Buffered common clock**
- **Slim 20-pin plastic and ceramic DIP packages**
- **See '273 for Master Reset version**
- **See '373 for transparent latch version**
- **See '374 for 3-state version**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS377	40MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS377N	
Ceramic DIP	N74LS377F	S54LS377F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	10LSul

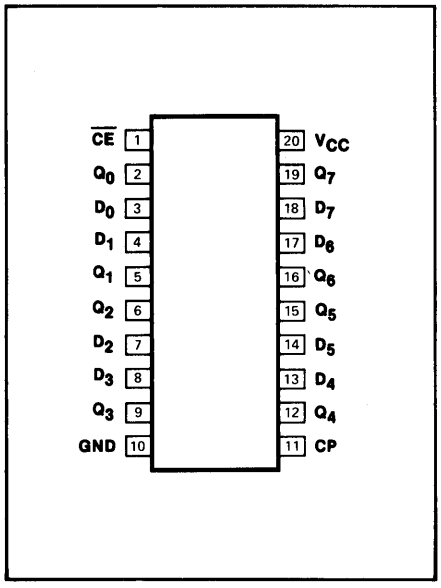
NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

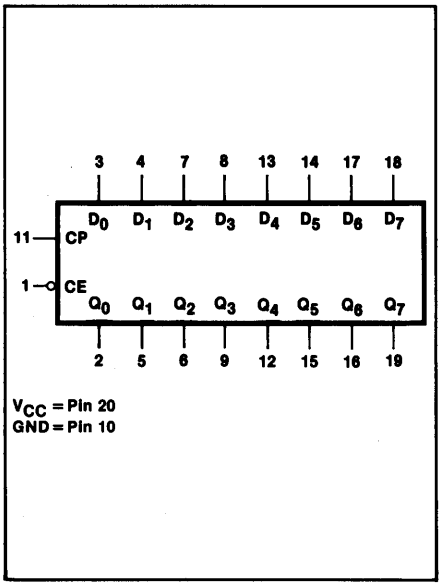
The '377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

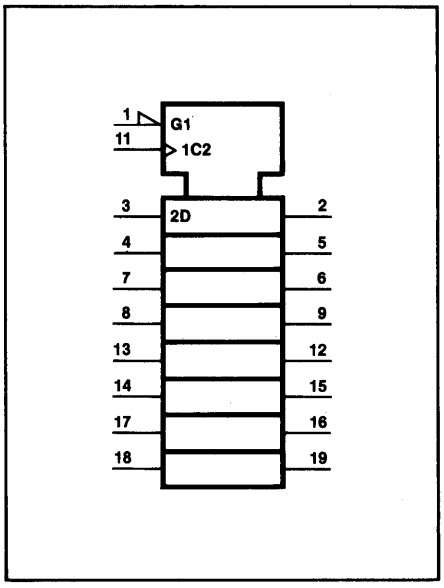
PIN CONFIGURATION



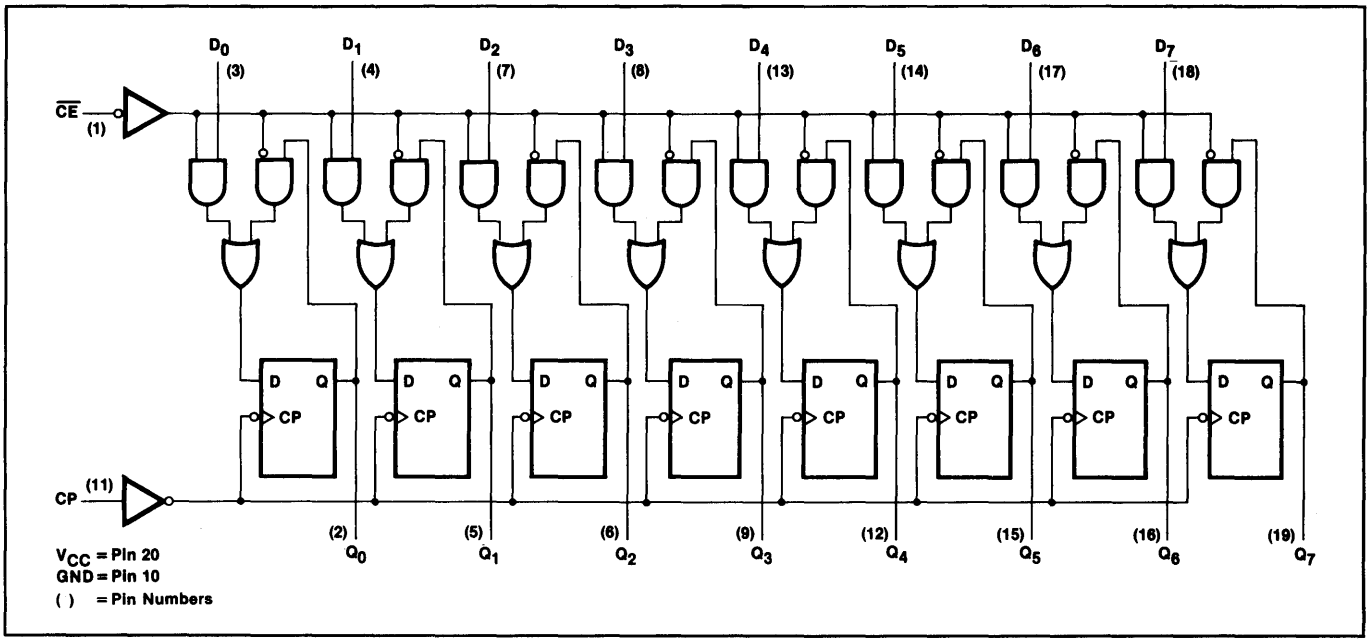
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS377			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.5		V
				Com'l	2.7	3.5		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		18	28	mA
			I_{CCL}	Outputs LOW		22	35	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open and ground applied to all Data and Enable inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			C_L = 15pF, R_L = 2kΩ		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 27	ns

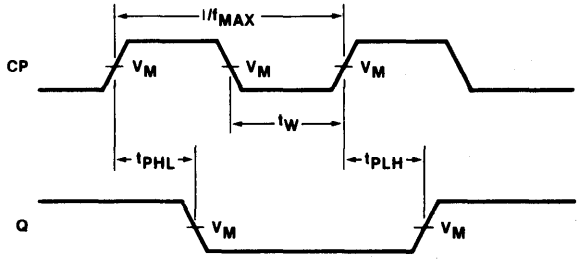
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	20		ns
t_s	Setup time, Data to CP	Waveform 2	20		ns
t_h	Hold time, Data to CP	Waveform 2	5		ns
t_s	Setup time, $\overline{CE}$ to CP	Waveform 2	20		ns
t_h	Hold time, $\overline{CE}$ to CP	Waveform 2	5		ns

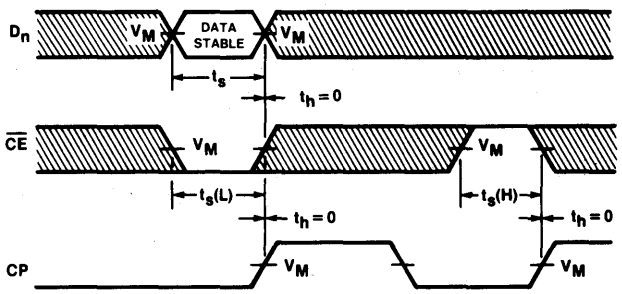
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA AND CLOCK ENABLE SETUP AND HOLD TIMES

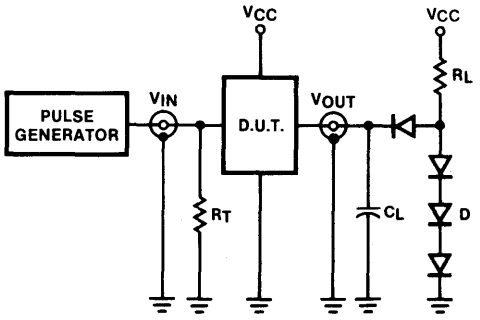


Waveform 2

$V_M = 1.5V$ for 54/74 and 54/74S; $V_M = 1.3V$ for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

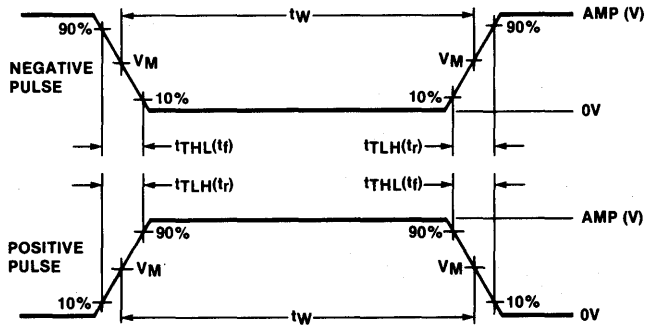
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOP 54/74S534

Octal D Flip-Flop With 3-State Outputs

- **8-bit positive, edge-triggered register**
- **Inverting outputs**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S534	8ns	116mA

DESCRIPTION

The '534 is an 8-bit, edge-triggered register coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's $\overline{Q}$ output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

ORDERING CODE

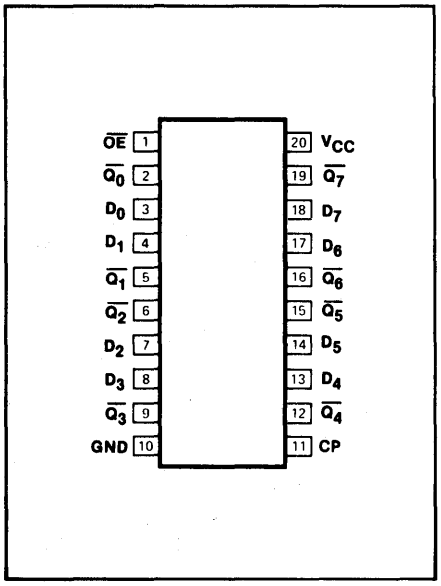
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S534N	
Ceramic DIP	N74S534F	S54S534F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

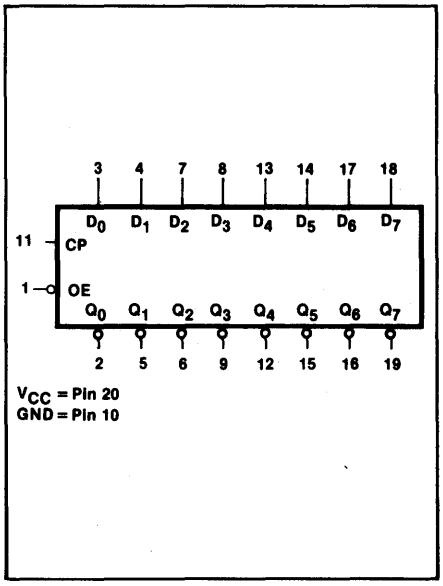
PINS	DESCRIPTION	54/74S
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
Where a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

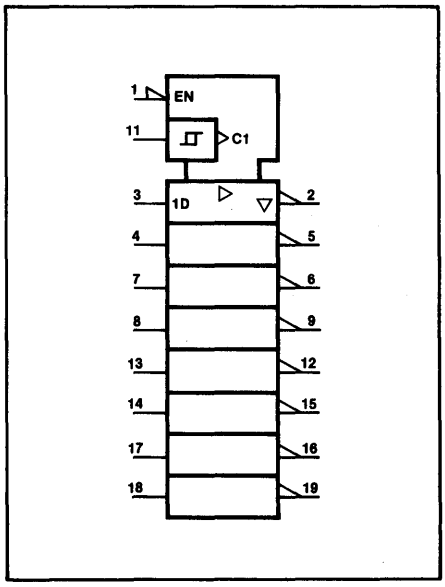
PIN CONFIGURATION



LOGIC SYMBOL

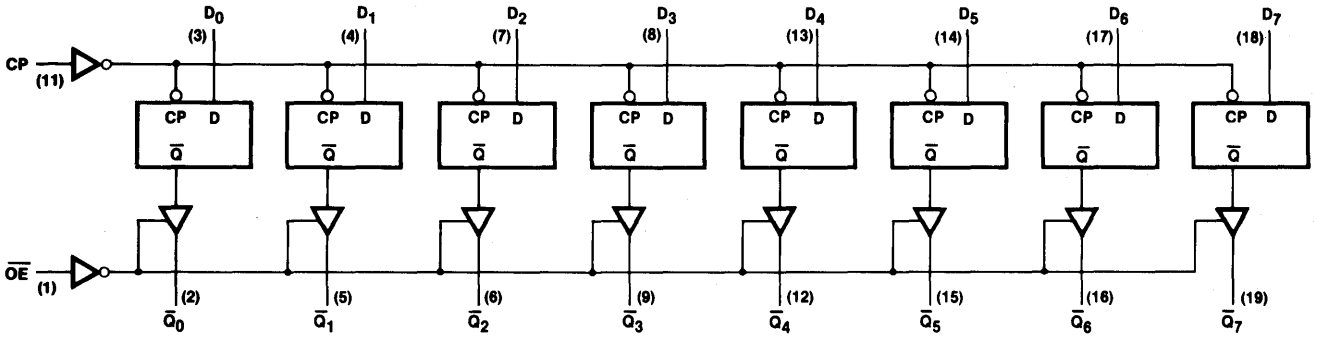


LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOP 54/74S534

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Load register and disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state.	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74S			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0	mA
		Com'l			−6.5	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

FLIP-FLOP 54/74S534

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74S534 Min	54/74S534 Typ[2]	54/74S534 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.0		V
				Com'l	2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.5[4]	V
				Com'l			0.5	V
			I_{OL} = 12mA	74LS				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.7V					μA
			V_O = 2.4V				50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 0.4V					μA
			V_O = 0.5V				-50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V					mA
			V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V					mA
			V_I = 0.5V				-0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-100	mA
I_{CC}	Supply Current (total)	V_{CC} = MAX	I_{CCL}	All inputs grounded		102	140	mA
			I_{CCZ}	CP, $\overline{OE}$ = 4.0V, D inputs = GND		131	180	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54S/74S C_L = 15pF, R_L = 280Ω Min	54S/74S C_L = 15pF, R_L = 280Ω Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 3	75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 3		15 17	ns
t_{PZH}	Enable time to HIGH level	Waveform 1		15	ns
t_{PZL}	Enable time to LOW level	Waveform 2		18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 1, C_L = 5pF		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 2, C_L = 5pF		12	ns

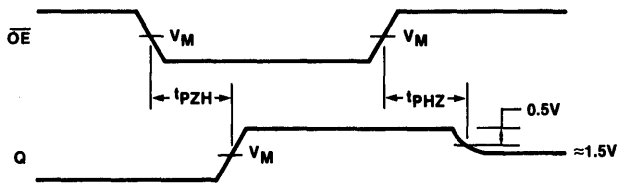
AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54S/74S Min	54S/74S Max	UNIT
$t_{W(H)}$ $t_{W(L)}$	Clock pulse width	Waveform 3	6 7.3		ns
t_s	Setup time, Data to Clock	Waveform 4	5		ns
t_h	Hold time, Data to Clock	Waveform 4	2		ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

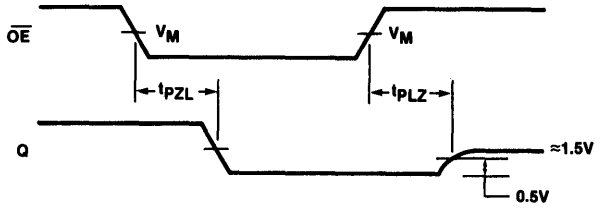
AC WAVEFORMS

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



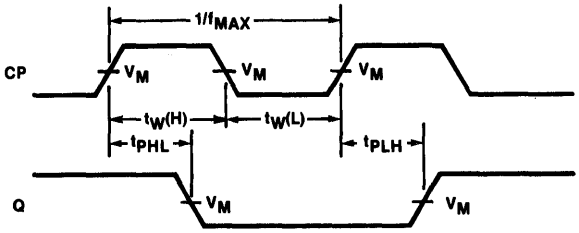
Waveform 1

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



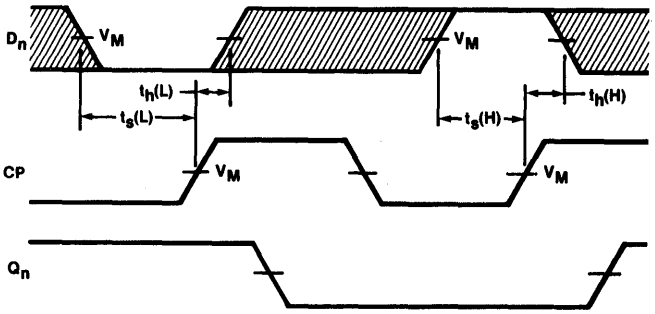
Waveform 2

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 3

DATA SETUP AND HOLD TIMES

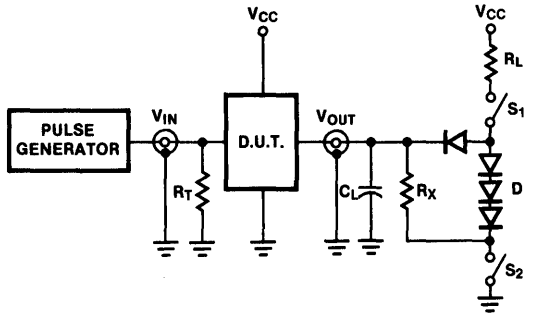


Waveform 4

V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



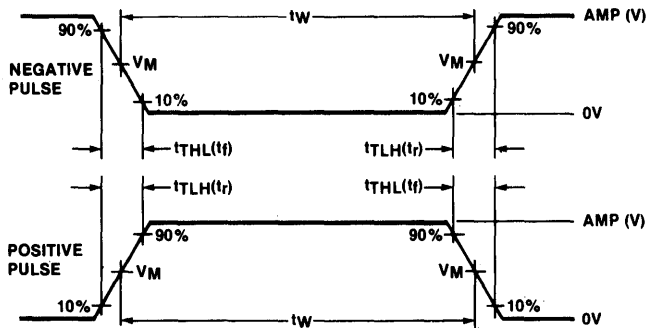
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSCEIVER 54/74LS640, 74LS640-1

Inverting Octal Bus Transceiver (3-State)

- **Octal bidirectional bus interface**
- **Inverting 3-State buffer outputs**
- **PNP inputs for reduced loading**
- **Hysteresis on all inputs**
- **48mA sink capability ('LS640-1)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS640 & -1	7ns	58mA

DESCRIPTION

The 'LS640 is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. In addition, the 74LS640-1 features a 48mA sink current capability. The device features a Chip Enable ($\overline{CE}$) input for easy cascading and a Send/Receive (S/$\overline{R}$) input for direction control. All inputs have hysteresis built in to minimize ac noise effects.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS640N N74LS640-1N	
Ceramic DIP	N74LS640F N74LS640-1F	S54LS640F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

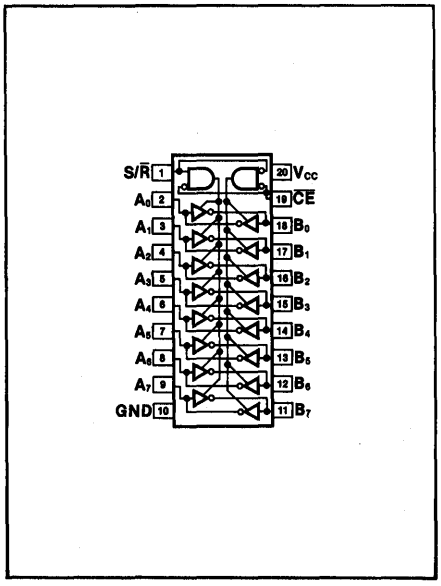
NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

FUNCTION TABLE

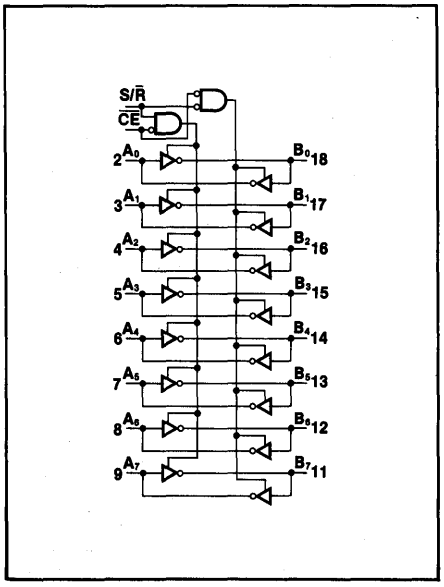
INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = $\overline{B}$	INPUTS
L	H	INPUTS	B = $\overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

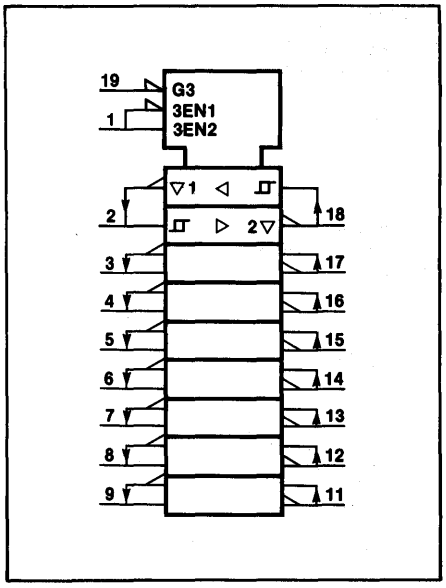
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS & -1	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

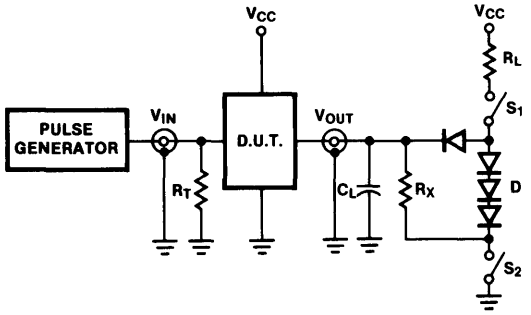
NOTE
V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS & -1			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.5	V
		Com'l			+0.6	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
		74LS-1 only			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

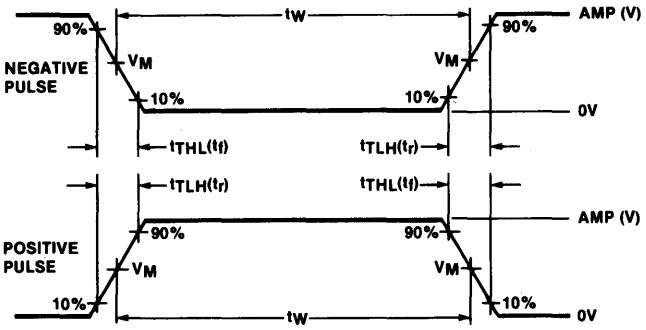


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

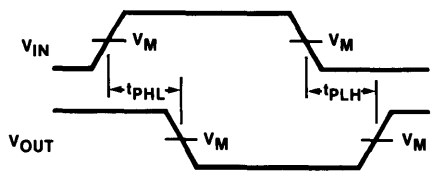
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless range otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/74LS640			74LS640-1			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis (V_{T+}-T_{T-})	V_{CC} = MIN, A or B input		Mil	0.1	0.4					V
				Com'l	0.2	0.4		0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX		2.0			2.0			V
			I_{OH} = −3mA		2.4	3.4		2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 12mA	Mil		0.25	0.4				V
				Com'l		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA	74LS		0.35	0.5		0.35	0.5	V
			I_{OL} = 48mA						0.4	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, $\overline{CE}$ input = 2.0V, V_O = 2.7V					20			20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, $\overline{CE}$ input = 2.0V, V_O = 0.4V					-400			-400	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A or B input			0.1			0.1	mA
			V_I = 7.0V	S/$\overline{R}$ or $\overline{CE}$ input			0.1			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-0.4			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-130	-40		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		48	70		48	70	mA
			I_{CCL}	Outputs LOW		62	90		62	90	mA
			I_{CCZ}	Outputs OFF		64	95		64	95	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open.

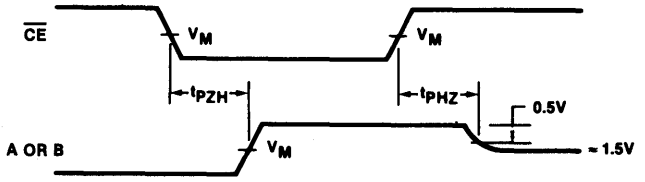
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

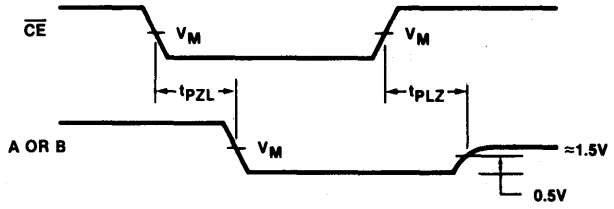
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54/74LS & -1		UNIT
		$C_L = 45pF$, $R_L = 667\Omega$		
		Min	Max	
t_{PLH} Propagation delay t_{PHL} A input to B output	Waveform 1		10 15	ns
t_{PLH} Propagation delay t_{PHL} B input to A output	Waveform 1		10 15	ns
t_{PZH} Enable to HIGH $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 2		40	ns
t_{PZH} Enable to HIGH $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 2		40	ns
t_{PZL} Enable to LOW $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 3		40	ns
t_{PZL} Enable to LOW $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 3		40	ns
t_{PHZ} Disable from HIGH $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 2, $C_L = 5pF$		25	ns
t_{PHZ} Disable from HIGH $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 2, $C_L = 5pF$		25	ns
t_{PLZ} Disable from LOW $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 3, $C_L = 5pF$		25	ns
t_{PLZ} Disable from LOW $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 3, $C_L = 5pF$		25	ns

TRANSCEIVERS 54/74LS641, LS642, 74LS641-1, LS642-1

Octal Bus Transceiver (Open Collector)

- **Octal bidirectional bus interface**
- **Open Collector Outputs**
  - **— 'LS641, non-inverting**
  - **— 'LS642, inverting**
- **PNP inputs for reduced loading**
- **Hysteresis on all inputs**
- **48mA sink capability ('LS641-1, LS642-1)**

TYPE	TYPICAL PROPAGATION DELAY (A to B)	TYPICAL SUPPLY CURRENT (Total)
74LS641 & -1	17ns	58mA
74LS642 & -1	17ns	58mA

FUNCTION TABLE, 'LS641

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	(Z)	(Z)

FUNCTION TABLE, 'LS642

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = $\overline{B}$	INPUTS
L	H	INPUTS	B = $\overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

ORDERING CODE

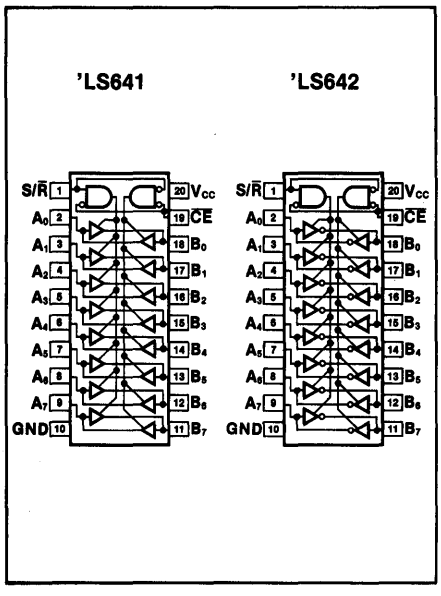
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS641N N74LS641-1N N74LS642N N74LS642-1N	
Ceramic DIP	N74LS641F N74LS641-1F N74LS642F N74LS642-1F	S54LS641F S54LS642F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

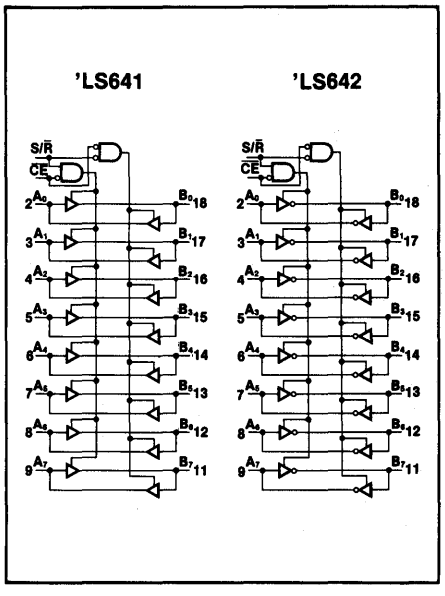
PINS	DESCRIPTION	54/74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

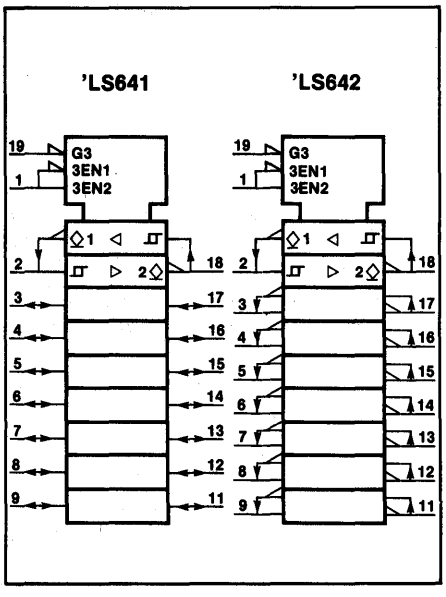
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS & -1	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

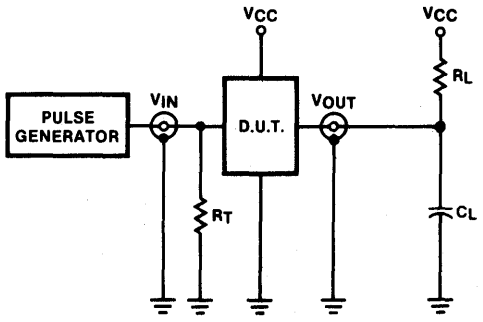
NOTE
V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS & -1			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.5	V
		Com'l			+0.6	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage				5.5	V
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
		74LS-1 only			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

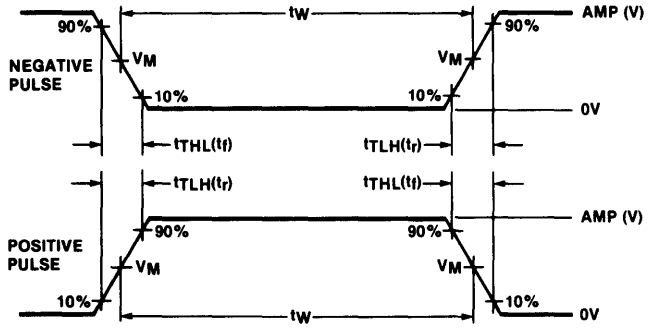
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

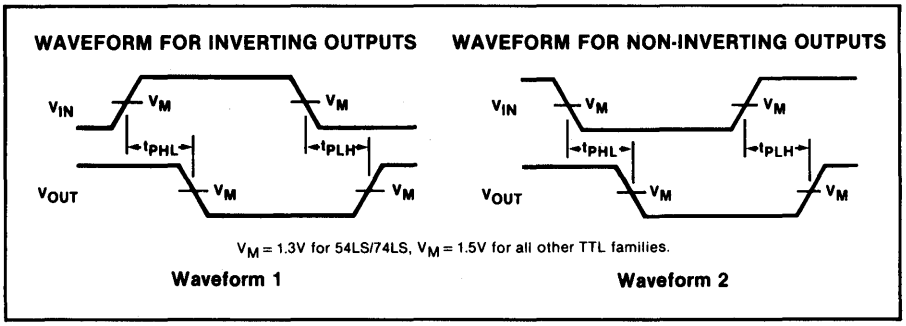
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless range otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/74LS641 54/74LS642			74LS641-1 74LS642-2			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN, A or B input		Mil	0.1	0.4					V
				Com'l	0.2	0.4		0.2	0.4		V
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					100			100	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 12mA	Mil		0.25	0.4				V
				Com'l		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA	74LS		0.35	0.5		0.35	0.5	V
			I_{OL} = 48mA						0.4	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A or B input			0.1			0.1	mA
			V_I = 7.0V	S/$\overline{R}$ or $\overline{CE}$ input			0.1			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-0.4			-0.4	mA
I_{CC}	Supply current[3] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		48	70		48	70	mA
			I_{CCL}	Outputs LOW		62	90		62	90	mA
			I_{CCZ}	Outputs OFF		64	95		64	95	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C
3. Measure I_{CC} with outputs open.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS641 & -1 C_L = 45pF, R_L = 667Ω		54/74LS642 & -1 C_L = 45pF, R_L = 667Ω		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A input to B output	Waveform 2, 'LS641 Waveform 1, 'LS642		25 25		25 25	ns
t_{PLH} t_{PHL}	Propagation delay B input to A output	Waveform 2, 'LS641 Waveform 1, 'LS642		25 25		25 25	ns
t_{PLH}	Propagation delay $\overline{CE}$, S/$\overline{R}$ inputs to A output $\overline{CE}$ input to B output S/$\overline{R}$ input to B output	 Waveform 1 Waveform 1 Waveform 2		 40 40 40		 40 40 40	ns
t_{PHL}	Propagation delay $\overline{CE}$, S/$\overline{R}$ inputs to A output $\overline{CE}$ input to B output S/$\overline{R}$ input to B output	 Waveform 2 Waveform 2 Waveform 1		 50 50 50		 60 60 60	ns

TRANSCEIVER 54/74LS645, 74LS645-1

Octal Bus Transceiver (3-State)

- **Octal bidirectional bus interface**
- **3-State buffer outputs**
- **PNP inputs for reduced loading**
- **Hysteresis on all inputs**
- **48mA sink capability ('LS645-1)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS645 & -1	10ns	58mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS645N N74LS645-1N	
Ceramic DIP	N74LS645F N74LS645-1F	S54LS645F

DESCRIPTION

The 'LS645 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. In addition, the 74LS645-1 features a 48mA sink current capability. The device features a Chip Enable ($\overline{CE}$) input for easy cascading and a Send/Receive (S/R) input for direction control. All inputs have hysteresis built in to minimize ac noise effects.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

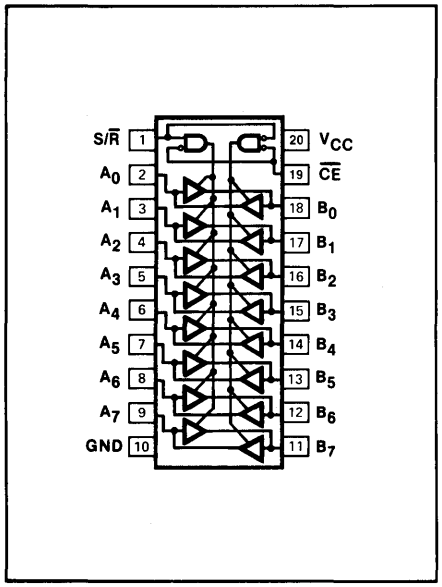
NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

FUNCTION TABLE

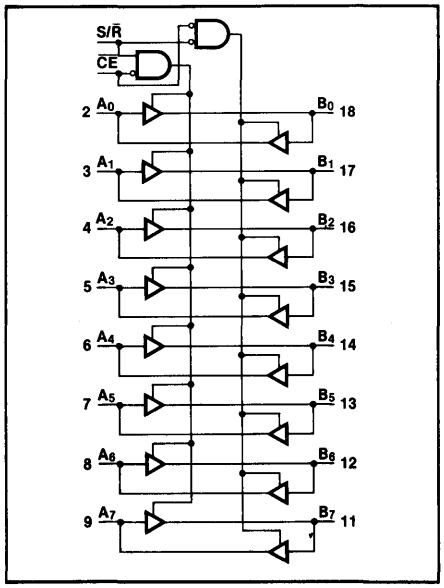
INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

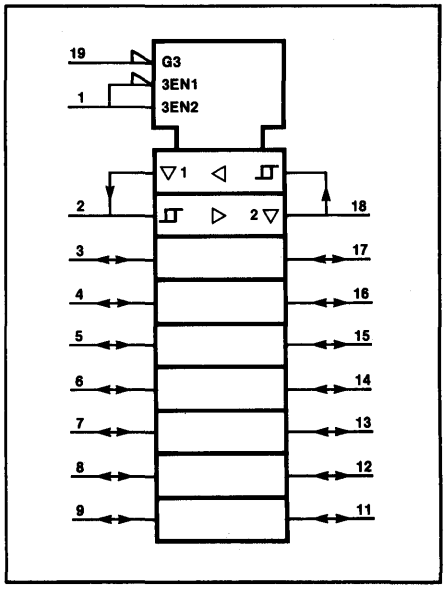
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVER 54/74LS645, 74LS645-1

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS & -1	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

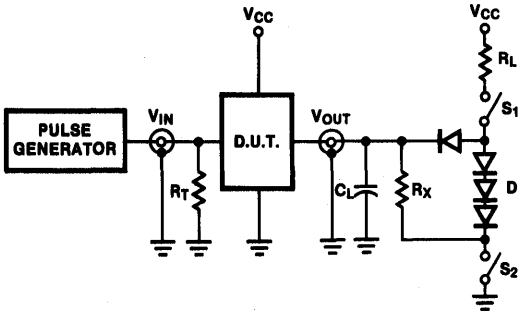
NOTE
V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS & -1			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.5	V
		Com'l			+0.6	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
		74LS-1 only			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

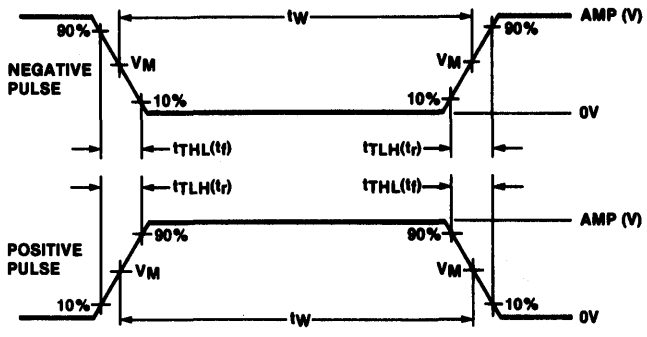


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless range otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/74LS645			74LS645-1			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis (V_{T+}-T_{T-})	V_{CC} = MIN, A or B input		Mil	0.1	0.4					V
				Com'l	0.2	0.4		0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX		2.0			2.0			V
			I_{OH} = −3mA		2.4	3.4		2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 12mA	Mil		0.25	0.4				V
				Com'l		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA	74LS		0.35	0.5		0.35	0.5	V
			I_{OL} = 48mA						0.4	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, $\overline{CE}$ input = 2.0V, V_O = 2.7V					20			20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, $\overline{CE}$ input = 2.0V, V_O = 0.4V					-400			-400	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A or B input			0.1			0.1	mA
			V_I = 7.0V	S/$\overline{R}$ or $\overline{CE}$ input			0.1			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-0.4			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-130	-40		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		48	70		48	70	mA
			I_{CCL}	Outputs LOW		62	90		62	90	mA
			I_{CCZ}	Outputs OFF		64	95		64	95	mA

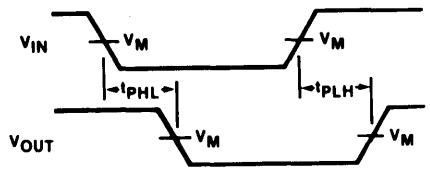
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54/74LS & -1 $C_L = 45pF$, $R_L = 667\Omega$		UNIT
		Min	Max	
t_{PLH} Propagation delay t_{PHL} A input to B output	Waveform 1		15 15	ns
t_{PLH} Propagation delay t_{PHL} B input to A output	Waveform 1		15 15	ns
t_{PZH} Enable to HIGH $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 2		40	ns
t_{PZH} Enable to HIGH $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 2		40	ns
t_{PZL} Enable to LOW $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 3		40	ns
t_{PZL} Enable to LOW $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 3		40	ns
t_{PHZ} Disable from HIGH $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 2, $C_L = 5pF$		25	ns
t_{PHZ} Disable from HIGH $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 2, $C_L = 5pF$		25	ns
t_{PLZ} Disable from LOW $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 3, $C_L = 5pF$		25	ns
t_{PLZ} Disable from LOW $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 3, $C_L = 5pF$		25	ns

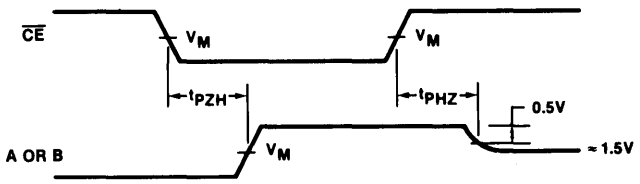
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

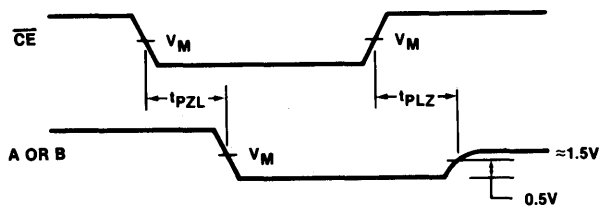
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

BUS TRANSCEIVERS 8T26A, 28

3-State Quad Bus Transceiver

- **High speed Schottky quad transceivers**
- **48mA LOW-state drive**
- **200μA bus loading**
- **Ideal for:**
  - **Half-duplex data transmission**
  - **Memory interface buffers**
  - **Data routing in bus oriented systems**
  - **High current drivers**
  - **MOS/CMOS-to-TTL interface**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T26A	7ns	48mA
N8T28	10ns	67mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N8T26AN • N8T28N	
Ceramic DIP	N8T26AF • N8T28F	S8T26AF • S8T28F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	N8T	S8T
I_N	Input	0.5SuI	0.5SuI
D/E, R/E	Inputs	0.5SuI	0.5SuI
D_{OUT}	Output	24SuI	16SuI
R_{OUT}	Output	10SuI	6SuI

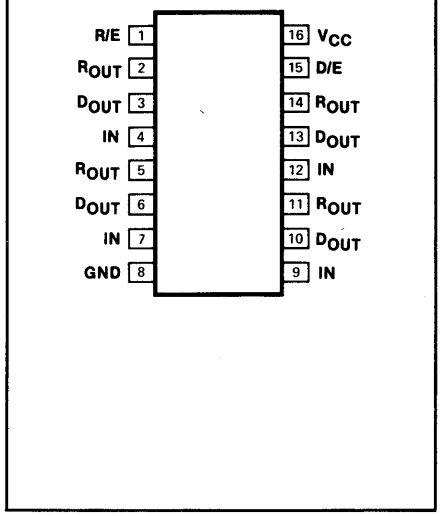
NOTE
A 54/74S unit load (SuI) is 50μA I_{IH} and −2.0mA I_{IL}.

DESCRIPTION

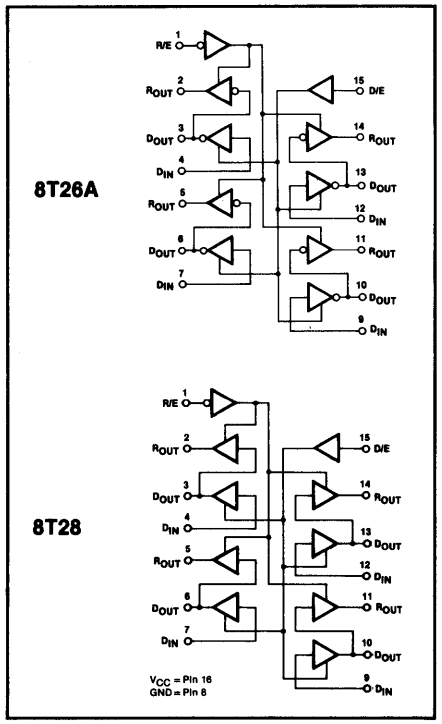
The 8T26A/28 consists of four pairs of 3-state logic elements configured as quad bus drivers/receivers, along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the 8T26A/28 from conventional multi-IC implementations. In addition, the 8T26/28's ultra high speed while driving heavy bus capacitance (300pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

Both the driver and receiver gates have 3-State outputs and low-current PNP inputs. 3-State outputs provide the high switching speeds of totem-pole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200μA maximum.

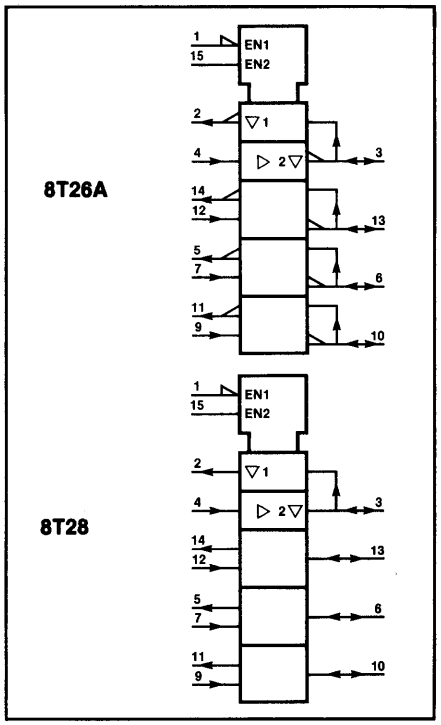
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8T	N8T	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
I_{OL}	Continuous	100	100	m A
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER				8T			UNIT
				Min	Nom	Max	
V_{CC}	Supply Voltage		Mil	4.5	5.0	5.5	V
			Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage			2.0			V
V_{IL}	LOW-level input voltage		Mil			+0.8	V
			Com'l			+0.8	V
I_{IK}	Input clamp current					−18	mA
I_{OH}	HIGH-level output current	Driver	Mil			−2	mA
			Com'l			−10	mA
I_{OL}	LOW-level output current	Driver	Mil			32	mA
			Com'l			48	mA
		Receiver	Mil			12	mA
			Com'l			20	mA
T_A	Operating free-air temperature		Mil	−55		+125	°C
			Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		N8T26A, N8T28		S8T26A, S8T28		UNIT
				Min	Max	Min	Max	
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		2.0		2.0		V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage			0.8		0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = MIN, I_{IK} = −18mA			-1.2		-1.2	V
V_{BD}	Input breakdown voltage	V_{CC} = MAX, I_I = 10mA		5.5		5.5		V
V_{OH}	HIGH-level output voltage, Driver outputs	V_{CC} = MIN	I_{OH} = −10mA	2.4				V
			I_{OH} = −2mA			2.4		V
V_{OH}	HIGH-level output voltage, Receiver outputs	V_{CC} = MIN, I_{OH} = −100μA		3.25				V
		V_{CC} = 5.0V, I_{OH} = −100μA				3.0		V
V_{OL}	LOW-level output voltage, Driver outputs	V_{CC} = MIN	I_{OL} = 48mA		0.5			V
			I_{OL} = 32mA				0.5	V
V_{OL}	LOW-level output voltage, Receiver outputs	V_{CC} = MIN	I_{OL} = 20mA		0.5			V
			I_{OL} = 12mA				0.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.4V			100		100	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.5V			-100		-100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 4.5V			25		25	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	Driver, Receiver		-200		-200	μA
			Disabled		-25		-25	μA
I_{OS}	Short-circuit output current[2]	V_{CC} = MAX	Driver	-50	-150	-50	-150	mA
			Receiver	-30	-100	-30	-100	mA
I_{CC}	Supply current	V_{CC} = MAX	8T26A		87		87	mA
			8T28		110		110	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

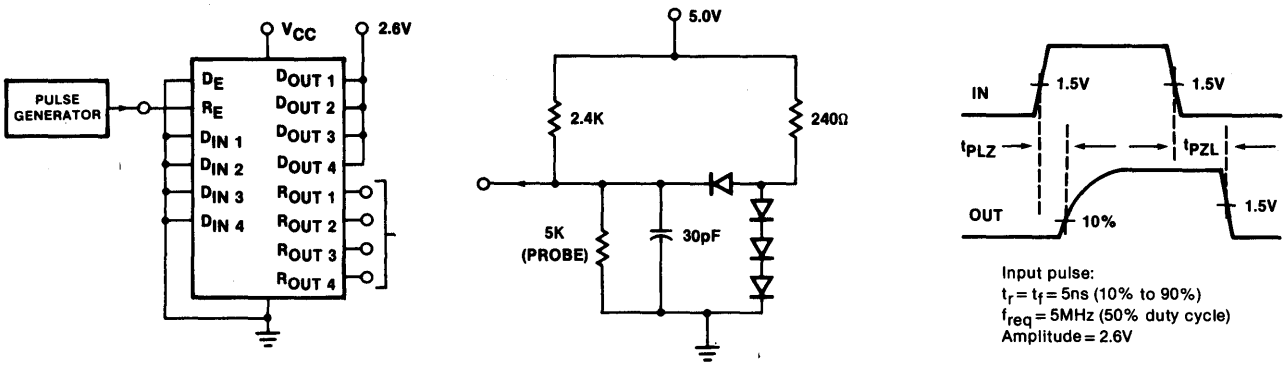
AC ELECTRICAL CHARACTERISTICS T_A° = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	8T26A		8T28		UNIT
			Min	Max	Min	Max	
t_{PHL}	Propagation delay, D_{OUT} to R_{OUT}	C_L = 30pF		14		17	ns
t_{PHL}	Propagation delay, D_{IN} to D_{OUT}	C_L = 300pF		14		17	ns
t_{PLH}	Propagation delay, D_{OUT} to R_{OUT}	C_L = 30pF		14		17	ns
t_{PLH}	Propagation delay, D_{IN} to D_{OUT}	C_L = 300pF		14		17	ns
t_{PZL}	Data enable to Data output, High Z to 0	C_L = 300pF		25		28	ns
t_{PLZ}	Data enable to Data output, 0 to High Z	C_L = 300pF		20		23	ns
t_{PZL}	Receive enable to Receive output, High Z to 0	C_L = 30pF		20		23	ns
t_{PLZ}	Receive enable to Receive output, 0 to High Z	C_L = 30pF		15		18	ns

TEST CIRCUITS AND WAVEFORMS

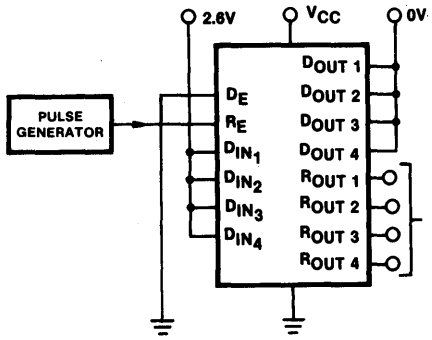
DISABLE AND ENABLE TIME
RECEIVE ENABLE TO RECEIVE OUTPUT

8T26A

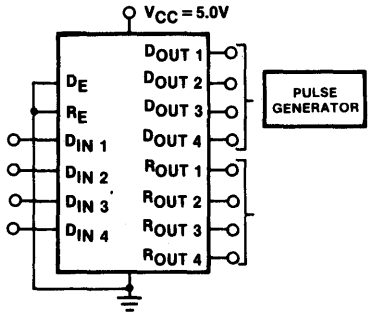


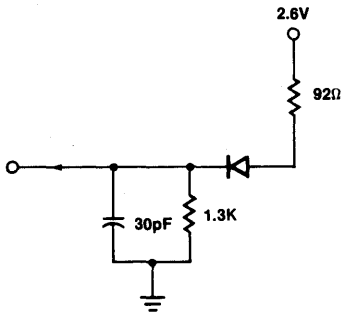
Input pulse:
$t_r = t_f = 5ns$ (10% to 90%)
$f_{req} = 5MHz$ (50% duty cycle)
Amplitude = 2.6V

8T28

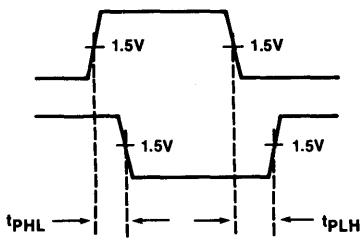


PROPAGATION DELAY
D_{OUT} TO R_{OUT}



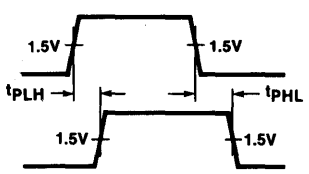


8T26A



Input pulse:
$t_r = t_f = 5ns$ (10% to 90%)
$f_{req} = 5MHz$ (50% duty cycle)
Amplitude = 2.6V

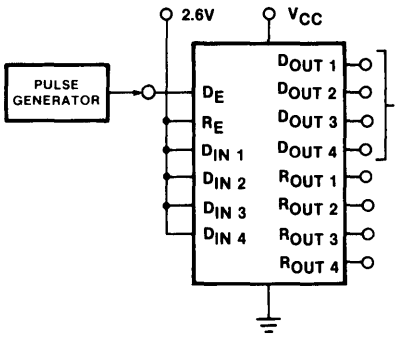
8T28

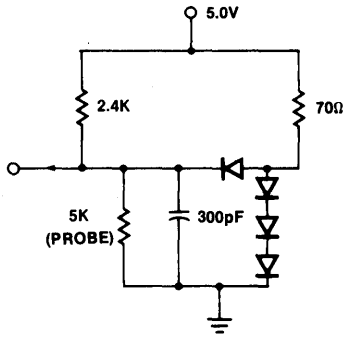


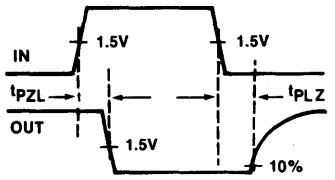
TEST CIRCUITS AND WAVEFORMS (Continued)

DISABLE AND ENABLE TIME
DATA ENABLE TO DATA OUTPUT

8T26A

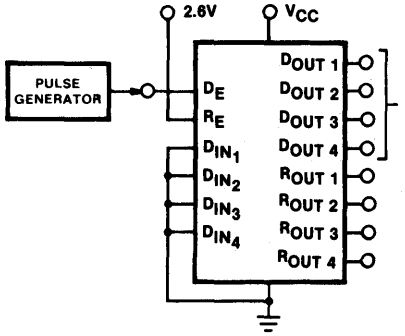




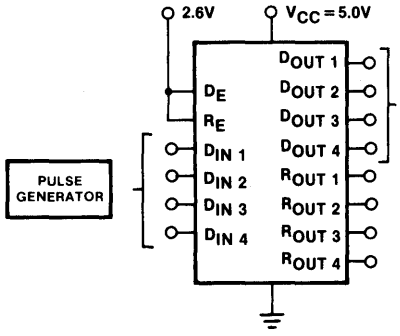


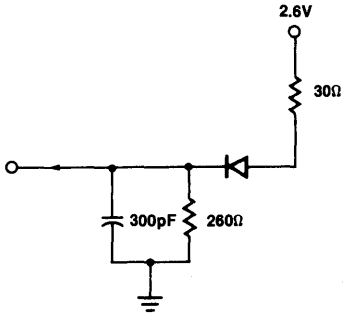
Input pulse:
$t_r = t_f = 5ns$ (10% to 90%)
freq = 5MHz (50% duty cycle)
Amplitude = 2.6V

8T28

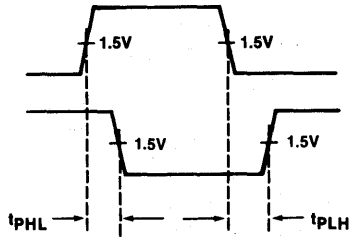


PROPAGATION DELAY
D_{IN} TO D_{OUT}

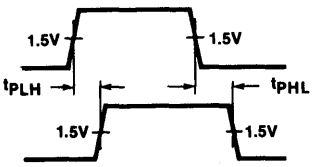




8T26A



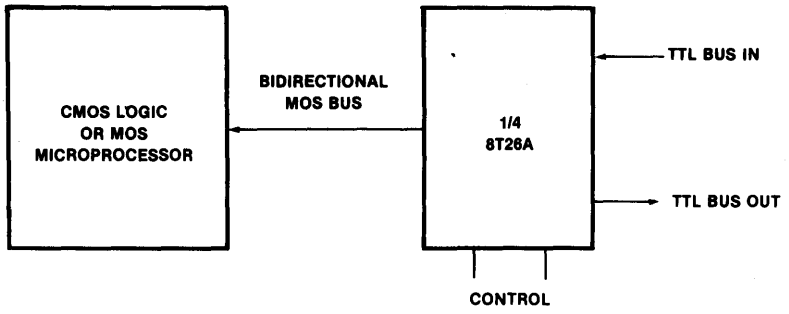
8T28



Input pulse:
$t_r = t_f = 5ns$ (10% to 90%)
$f_{req} = 10MHz$ (50% duty cycle)
Amplitude = 2.6V

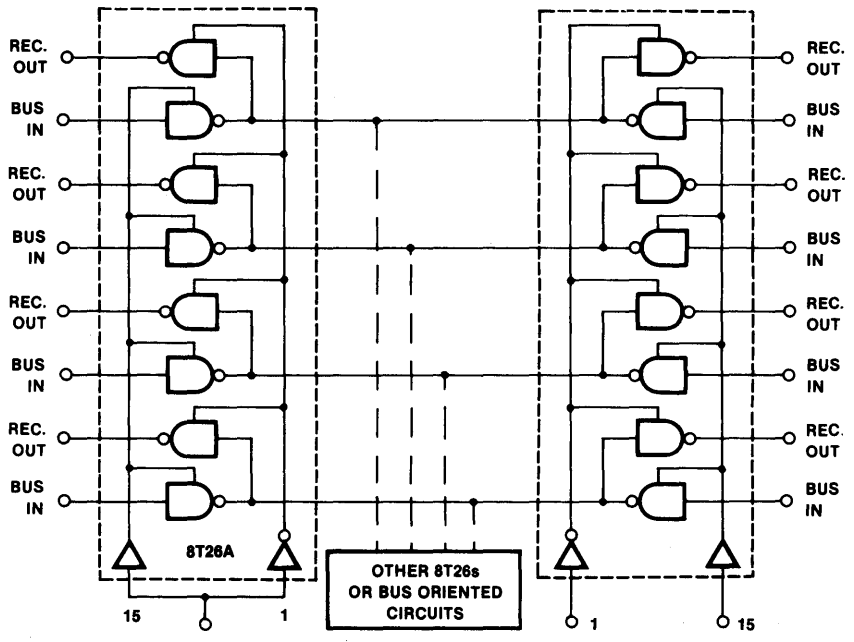
TYPICAL APPLICATION

BIDIRECTIONAL MOS
CMOS to TTL Interface



TYPICAL APPLICATION

BIDIRECTIONAL DATA BUS



Control lines may be tied together, such that logical "1" transmit, logical "0" receive.

Logical "0" = active
Logical "11" = Hi-z

Logical "1" = active
Logical "0" = Hi-z

HEX BUFFERS/INVERTERS 8T95, 96, 97, 98

High Speed Hex 3-State Buffers
High Speed Hex 3-State Inverters

DESCRIPTION

Each of the 3-state bus interface elements described herein has low current PNP inputs and is designed with Schottky TTL technology for ultra high speed. The devices are used to convert TTL/DTL or MOS/CMOS to 3-state TTL bus levels. For maximum systems flexibility, the 8T95 and 8T97 do so without logic inversion, whereas the 8T96 and 8T98 provide the logical complement of the input. The 8T95 and 8T96 feature a common control line for all six devices, whereas the 8T97 and 8T98 have control lines for four devices from one input and two from another input.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T95	8ns	65mA
N8T96	6.5ns	59mA
N8T97	8ns	65mA
N8T98	6.5ns	59mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N8T95N • N8T96N N8T97N • N8T98N	
Ceramic DIP	N8T95F • N8T96F N8T97F • N8T98F	S8T95F • S8T98F S8T97F •

FUNCTION TABLE—8T95

INPUTS			OUTPUT
DIS_1	DIS_2	I	Y
L	L	L	L
L	L	H	H
X	H	X	(Z)
H	X	X	(Z)

L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
DIS	Input	1Sul
I	Input	1Sul
Y	Output	24Sul

NOTE
A 54/74S unit load (ul) is 50μA I_{IH} and −2.0mA I_{IL}.

FUNCTION TABLE—8T96

INPUTS			OUTPUT
DIS_1	DIS_2	I	$\overline{Y}$
L	L	L	H
L	L	H	L
X	H	X	(Z)
H	X	X	(Z)

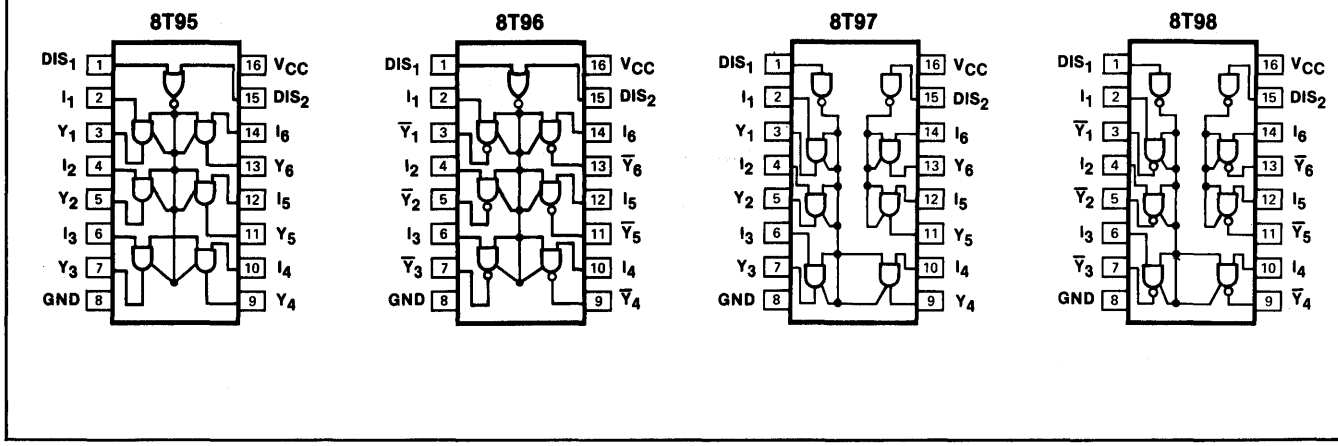
FUNCTION TABLE—8T97

INPUTS		OUTPUT
DIS	I	Y
L	L	L
L	H	H
H	X	(Z)

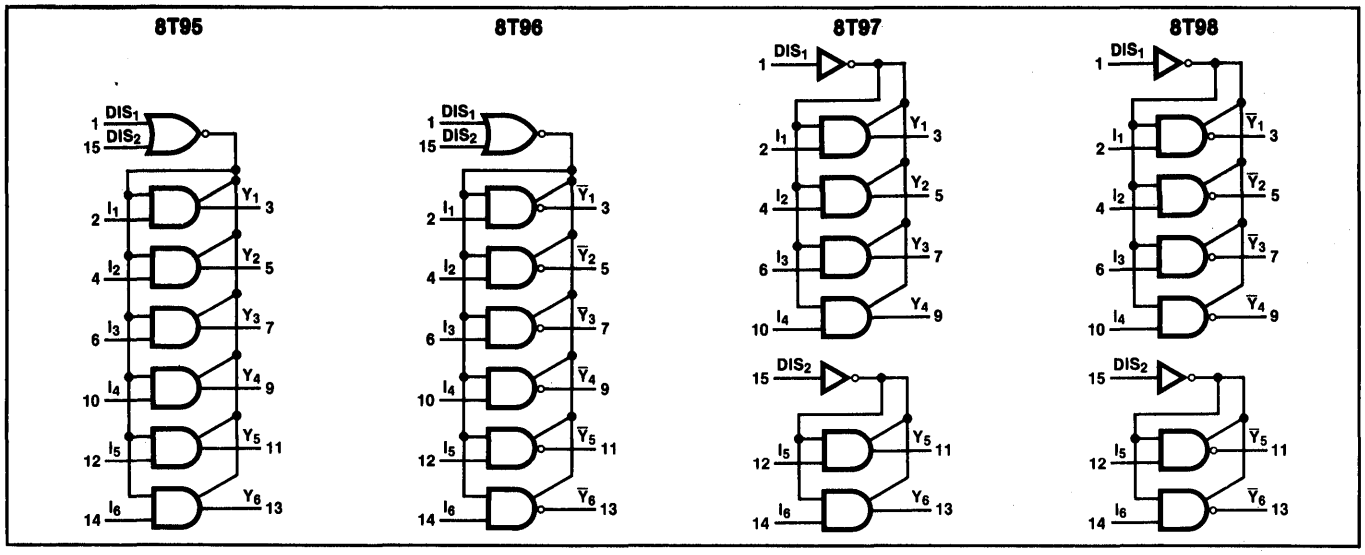
FUNCTION TABLE—8T98

INPUTS		OUTPUT
DIS	I	$\overline{Y}$
L	L	H
L	H	L
H	X	(Z)

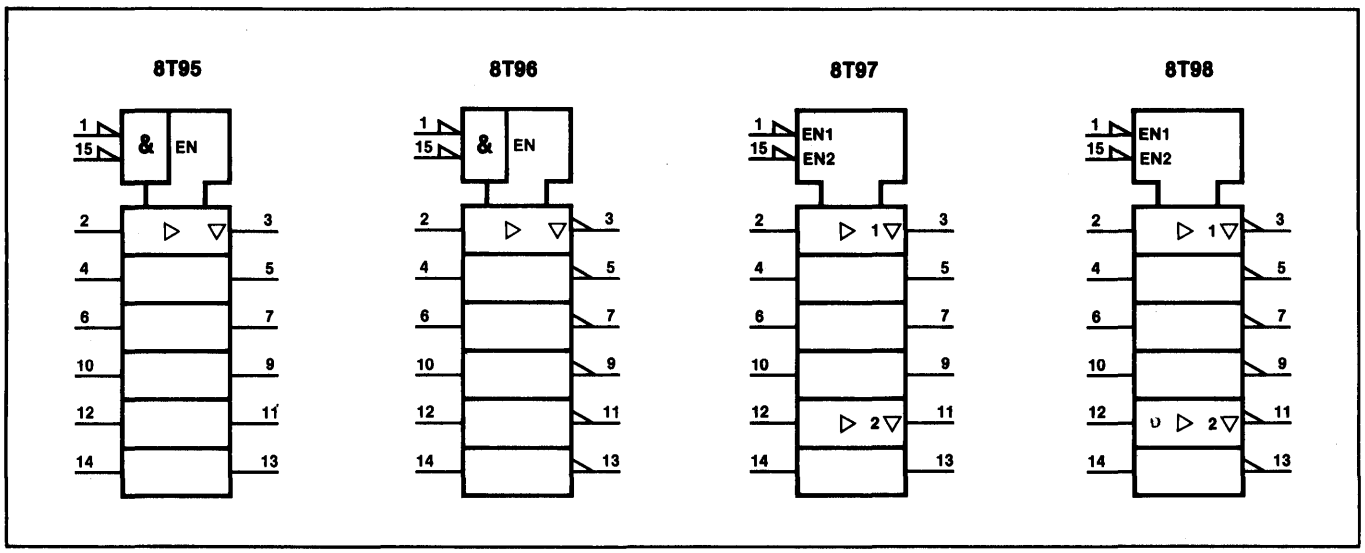
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

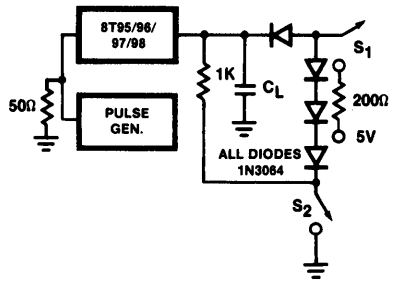
PARAMETER		S8T	N8T	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
I_{OL}	Continuous	100	100	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			8T			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−5.2	μA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.7V for S8T only.

TEST CIRCUIT



Input Characteristics
PA = 3V, = 1MHz $t_r = t_f \leq 10$ns (10% to 90%)
C_L includes probe and jig capacitance.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted.)

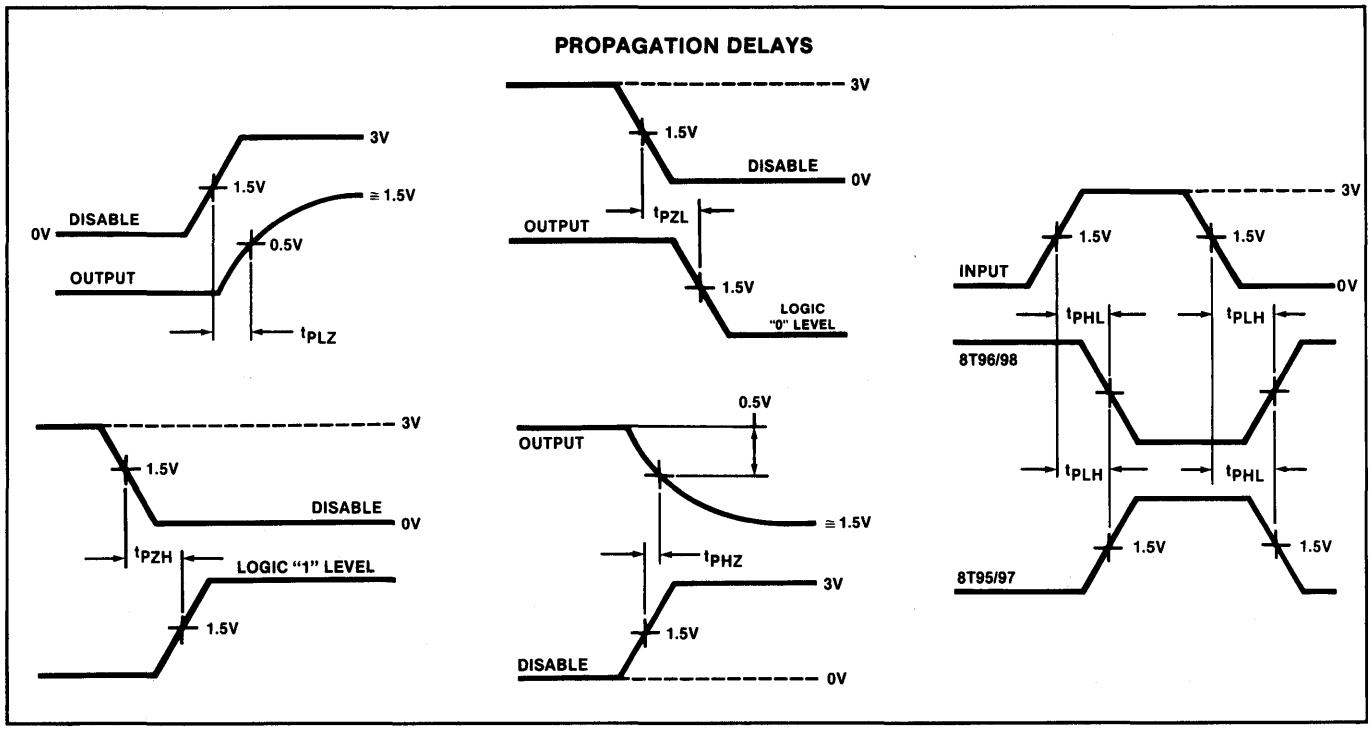
PARAMETER		TEST CONDITIONS[1]		8T95/97		8T96/98		UNIT
				Min	Max	Min	Max	
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		2.0		2.0		V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage			0.8		0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = MIN, I_{IK} = −12mA			-1.5		-1.5	V
V_{BD}	Input breakdown voltage	V_{CC} = MAX, I_I = 1mA		5.5		5.5		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, I_{OH} = −5.2mA		2.4		2.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, I_{OL} = 48mA			0.5[3]		0.5[3]	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.4V			40		40	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.5V			-40		-40	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V			40		40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	Disable = 0.5V		-400		-400	μA
			Disable = 2.0V		-40		-40	μA
I_{OS}	Short-circuit output current[2]	V_{CC} = MAX		-40	-115	-40	-115	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			98		89	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with V_{OUT} = +0.5V and $V_{CC} = V_{CC}$ MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
3. V_{OL} = +0.45V MAX for S8T at T_A = +125°C only.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	8T95/97 $R_L = 200\Omega$		8T96/98 $R_L = 200\Omega$		UNIT
			Min	Max	Min	Max	
t_{PLH}	Propagation delay Data inputs to Data outputs	S_1, S_2 are closed, $C_L = 50pF$	3	12	4	11	ns
t_{PHL}	Propagation delay Data inputs to Data outputs	S_1, S_2 are closed, $C_L = 50pF$	3	13	3	10	ns
t_{PZH}	Disable to outputs High Z to Logic "1"	S_1 is open, S_2 is closed, $C_L = 50pF$	8	25	7	22	ns
t_{PZL}	Disable to outputs High Z to Logic "0"	S_1 is closed, S_2 is open, $C_L = 50pF$	12	25	11	24	ns
t_{PHZ}	Disable to outputs Logic "1" to High Z	S_1, S_2 are closed, $C_L = 5pF$	3	10	3	10	ns
t_{PLZ}	Disable to outputs Logic "0" to High Z	S_1, S_1 are closed, $C_L = 5pF$	3	12	5	16	ns

AC WAVEFORMS



TRANSCEIVER 8T125

Octal 3-State Transceiver

- **Octal bidirectional bus interface**
- **3-State buffer outputs**
- **PNP inputs for reduced loading**
- **Hysteresis on all inputs**
- **Pin compatible with 54LS/74LS245**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T125	7.5ns	50mA

DESCRIPTION

The 8T125 is an octal transceiver featuring inverting 3-State bus-compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable input for easy cascading and a Send/Receive input for direction control. All inputs have hysteresis built in to minimize ac noise effects.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N8T125N	
Ceramic DIP	N8T125F	S8T125F

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = $\overline{B}$	INPUTS
L	H	INPUT	B = $\overline{A}$
H	X	(Z)	(Z)

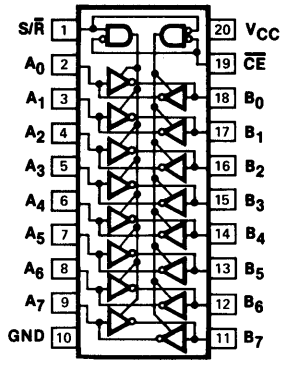
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

INPUT AND OUTUT LOADING AND FAN-OUT TABLE

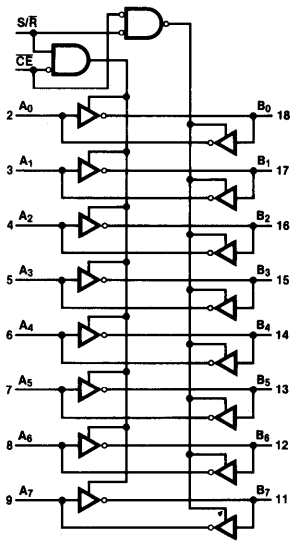
PINS	DESCRIPTION	8T125
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

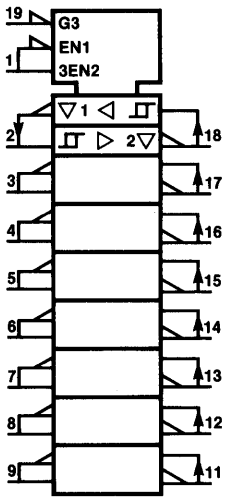
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVER 8T125

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

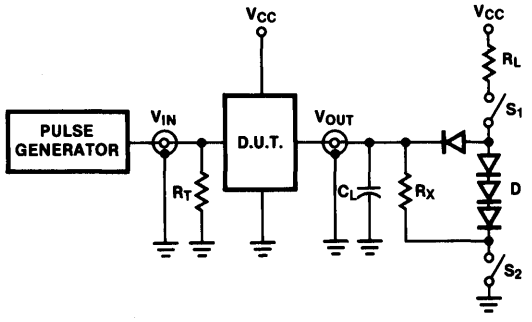
PARAMETER			S8T	N8T	UNIT
V_{CC}	Supply voltage		7.0	7.0	V
V_{IN}	Input voltage	Transceiver inputs	−0.5 to +5.5	−0.5 to +5.5	V
		Non-Transceiver inputs	−0.5 to +7.0	−0.5 to +7.0	V
I_{OL}	Continuous		50	50	m A
I_{IN}	Input current		−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range		−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			8T			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



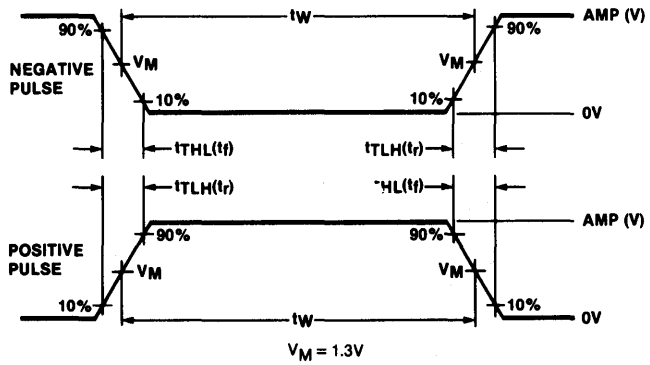
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8T	3.0V	1MHz	500ns	15ns	6ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			8T125 Min	8T125 Max	UNIT
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN			0.2		V
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage			2.0		V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = MIN, I_{IK} = −18mA				−1.5	V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN	I_{OH} = −2.0mA	Mil	2.4		V
			I_{OH} = −3.0mA	Com'l	2.4		V
			I_{OH} = −12mA	Mil	2.0		V
			I_{OH} = −15mA	Com'l	2.0		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN	I_{OL} = 12mA	Mil		0.4	V
				Com'l		0.4	V
			I_{OL} = 24mA	Com'l		0.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.4V				20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.4V				−200	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				100	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−200	μA
I_{OS}	Short-circuit output current[2]	V_{CC} = MAX			−40	−120	mA
I_{CCH}	Supply current HIGH	V_{CC} = MAX, outputs HIGH				70	mA
I_{CCL}	Supply current LOW	V_{CC} = MAX, outputs LOW				90	mA
I_{CCZ}	Supply current "off"	V_{CC} = MAX, outputs "off"				95	mA

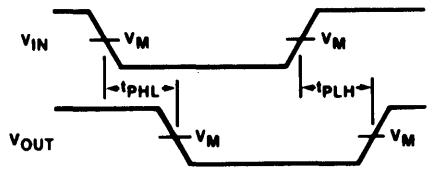
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	8T R_L = 667Ω Min	8T R_L = 667Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Input to output	Waveform 1, C_L = 45pF		12 12	ns
t_{PZH}	Enable to HIGH	Waveform 2, C_L = 45pF		40	ns
t_{PZL}	Enable to LOW	Waveform 3, C_L = 45pF		40	ns
t_{PHZ}	Disable from HIGH	Waveform 2, C_L = 5pF		25	ns
t_{PLZ}	Disable from LOW	Waveform 3, C_L = 5pF		25	ns

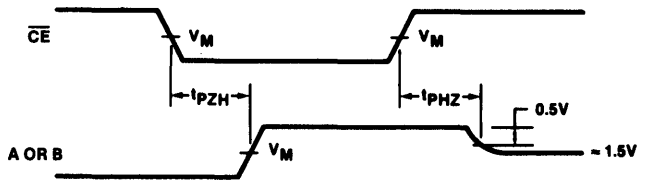
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

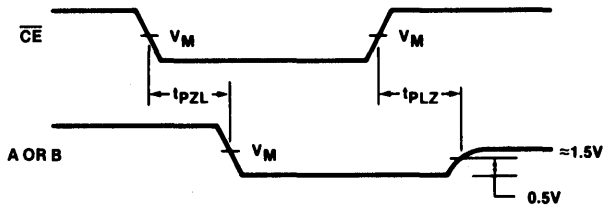
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

$V_M = 1.3V$

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

TRANSCEIVERS 8T126, 127, 128, 129

Quad, 3-State Transceivers

DESCRIPTION

The 8T126 through 8T129 are quad transceivers designed to handle many bus interface applications. The devices feature 3-State outputs on both send and receive buffers, and pnp transistors on all inputs to reduce input LOW loading requirements.

The 8T126 and 8T128 feature a 3.4V minimum V_{OH} level on the receiver for MOS interface applications. The send and receive buffers have separate Enable inputs for independent control.

The 8T127 and 8T129 feature full 24mA drive in both send and receive buffers. These devices have a common Chip Enable input for easy cascading and a Send/Receive input for direction control.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T126	10ns (Data)	17mA
N8T127	9ns (Data)	21mA
N8T128	10ns (Data)	17mA
N8T129	9ns (Data)	21mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic	N8T126N • N8T127N N8T128N • N8T129N	
Ceramic DIP	N8T126F • N8T127F N8T128F • N8T129F	S8T126F • S8T127F S8T128F • S8T129F
Flatpack		S8T126W • S8T127W S8T128W • S8T129W

FUNCTION TABLES

8T126

INPUTS			RECVR. OUT	BUS I/O
SE	$\overline{RE}$	D_n	A_n	B_n
L	L	X	A = $\overline{B}$	INPUTS
L	H	X	(Z)	(Z)
H	H	L	(Z)	H
H	H	H	(Z)	L
H	L	L	L	H
H	L	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(X) = HIGH imedance "off" state

8T127

INPUTS			RECVR. OUT	BUS I/O
$\overline{CE}$	S/$\overline{R}$	D_n	A_n	B_n
L	L	X	A = $\overline{B}$	INPUTS
L	H	L	(Z)	H
L	H	H	(Z)	L
H	X	X	(Z)	(Z)

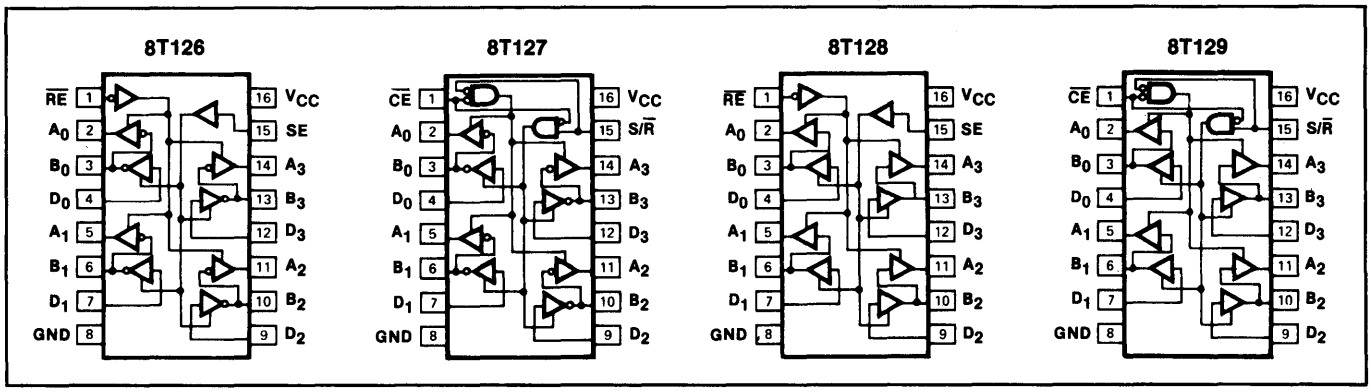
8T128

INPUTS			RECVR. OUT	BUS I/O
SE	$\overline{RE}$	D_n	A_n	B_n
L	L	X	A = B	INPUTS
L	H	X	(Z)	(Z)
H	H	L	(Z)	L
H	H	H	(Z)	H
H	L	L	L	L
H	L	H	H	H

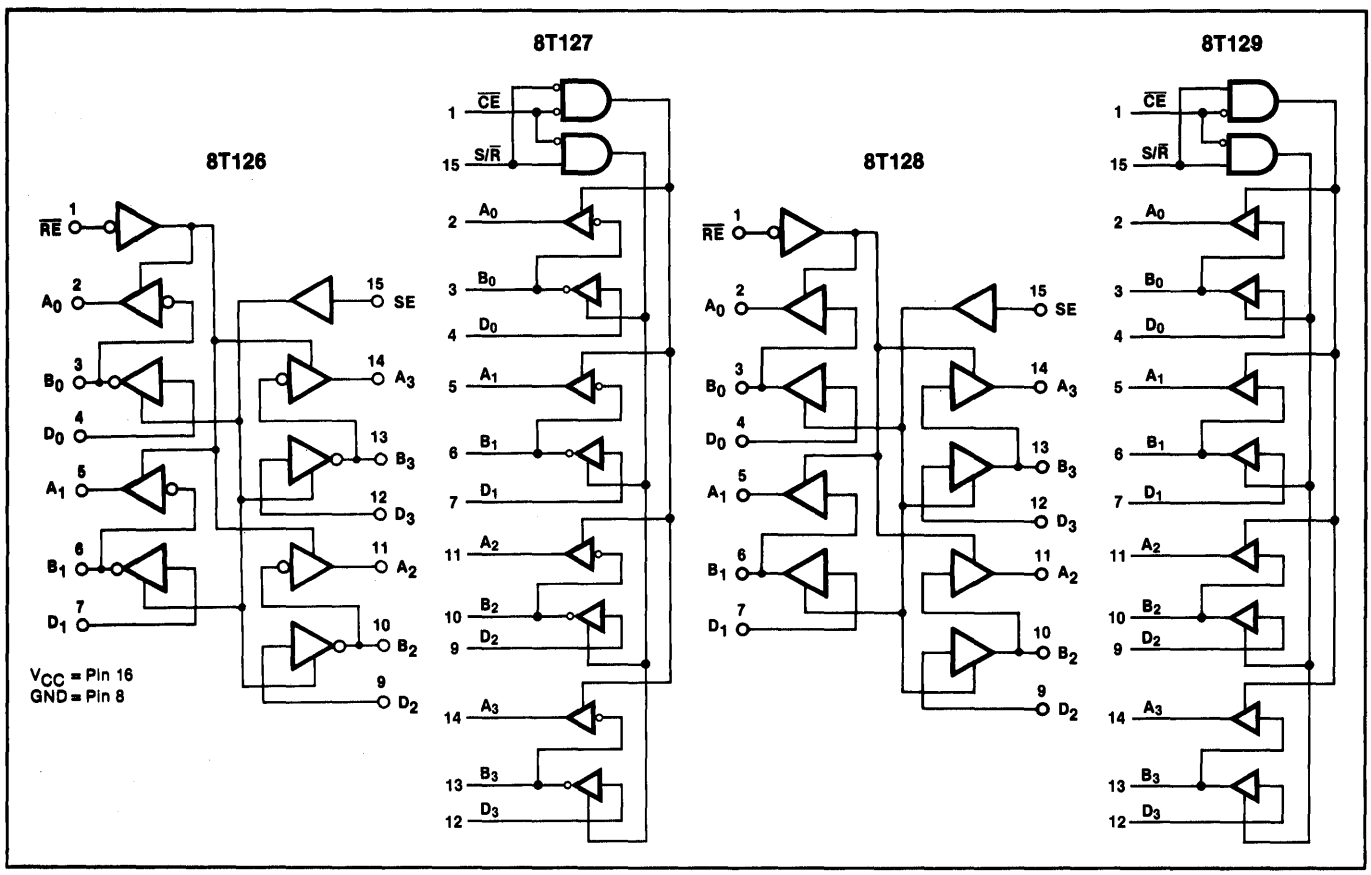
8T129

INPUTS			RECVR. OUT	BUS I/O
$\overline{CE}$	S/$\overline{R}$	D_n	A_n	B_n
L	L	X	A = B	INPUTS
L	H	L	(Z)	L
L	H	H	(Z)	H
H	X	X	(Z)	(Z)

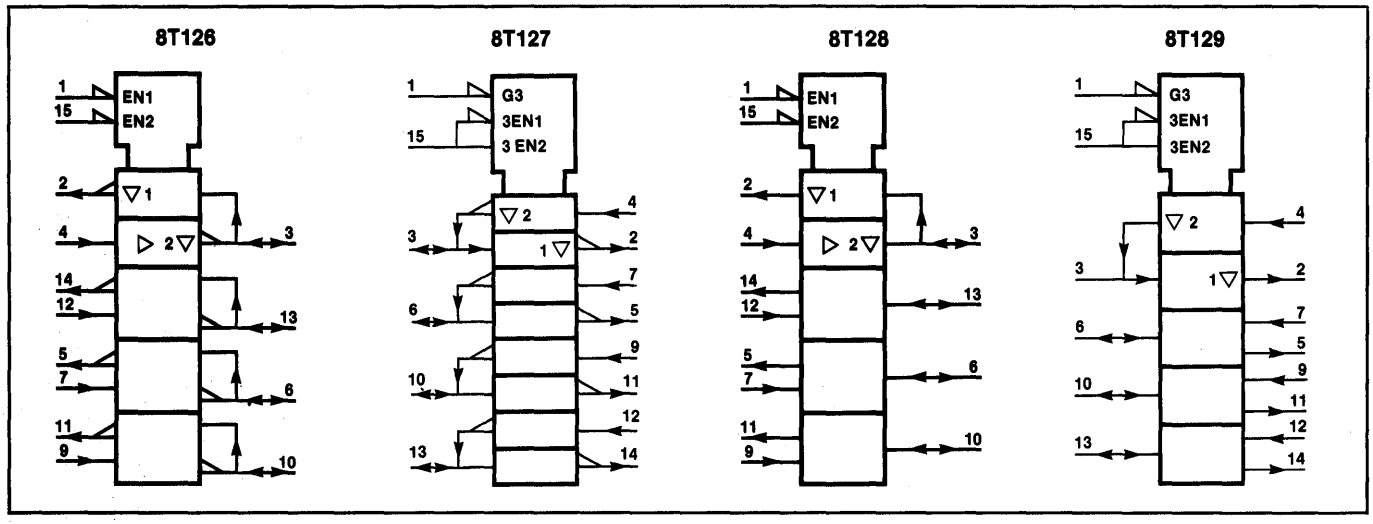
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER			S8T	N8T	UNIT
V_{CC}	Supply voltage		7.0	7.0	V
V_{IN}	Input voltage	Transceiver inputs	−0.5 to +5.5	−0.5 to +5.5	V
		Non-Transceiver inputs	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current		−30 to +1	−30 to +1	mA
I_{OL}	Continuous		50	50	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range		−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETERS				8T126/8T128			8T127/8T129			UNIT
				Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage		Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
			Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage			2.0			2.0			V
V_{IL}	LOW-level input voltage		Mil			0.7			0.7	V
			Com'l			0.8			0.8	V
I_{IK}	Input clamp current					−18			−18	mA
I_{OH}	HIGH-level output current	Bus	Mil			−2.0			−2.0	mA
			Com'l			−5.2			−5.2	mA
		Receiver	Mil			−1.0			−2.0	mA
			Com'l			−2.6			−5.2	mA
I_{OL}	LOW-level output current	Bus	Mil, Com'l			12			12	mA
			Com'l			24			24	mA
		Receiver	Mil, Com'l			6			12	mA
			Com'l			12			24	mA
T_A	Operating free-air temperature		Mil	−55		+125	−55		+125	°C
			Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			8T126/8T128		8T127/8T129		UNIT
					Min	Max	Min	Max	
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage			2.0		2.0		V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		Mil		0.7		0.7	V
				Com'l		0.8		0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = MIN, I_{IK} = −18mA				−1.5		−1.5	V
V_{OH}	HIGH-level output voltage, Bus outputs	V_{CC} = MIN	I_{OH} = −2.0mA	Mil	2.4		2.4		V
			I_{OH} = −5.2mA	Com'l	2.4		2.4		V
V_{OH}	HIGH-level output voltage, Receiver outputs	V_{CC} = MIN, V_{IN} = V_{IL}, or V_{IH} per Function Table	I_{OH} = −100μA	Mil	3.1				V
			I_{OH} = −100μA	Com'l	3.4				V
			I_{OH} = −1.0mA	Mil	2.4				V
			I_{OH} = −2.0mA	Mil			2.4		V
			I_{OH} = −2.6mA	Com'l	2.4				V
			I_{OH} = −5.2mA	Com'l			2.4		V
V_{OL}	LOW-level output voltage, Bus outputs	V_{CC} = MIN	I_{OL} = 12mA	Mil & Com'l		0.4		0.4	V
			I_{OL} = 24mA	Com'l		0.5		0.5	V
V_{OL}	LOW-level output voltage, Receiver outputs	V_{CC} = MIN	I_{OL} = 6mA	Mil & Com'l		0.4			V
			I_{OL} = 12mA	Mil & Com'l				0.4	V
			I_{OL} = 12mA	Com'l		0.5			V
			I_{OL} = 24mA	Com'l				0.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.4V				20		20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied, Receiver outputs	V_{CC} = MAX, V_O = 0.4V				−20		−20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied, Bus outputs	V_{CC} = MAX, V_O = 0.4V				−100		−200	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				20		20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	Bus inputs	V_I = 5.5V		100		100	μA
			Others	V_I = 7.0V		100		100	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−100		−200	μA
I_{OS}	Short-circuit output current[2]	V_{CC} = MAX			−40	−120	−40	−120	mA
I_{CCH}	Supply current HIGH	V_{CC} = MAX, outputs HIGH				26		36	mA
I_{CCL}	Supply current LOW	V_{CC} = MAX, outputs LOW				30		42	mA
I_{CCZ}	Supply current "off"	V_{CC} = MAX, outputs "off"				36		44	mA

NOTES

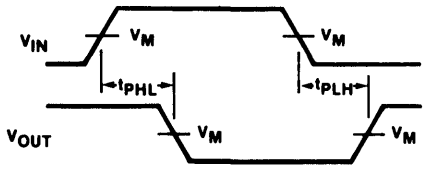
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	8T126/8T128		8T127/8T129		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Bus output	Waveforms 1 & 2, $C_L = 100pF$, $R_L = 667\Omega$		20 30		20 30	ns
t_{PLH} t_{PHL}	Propagation delay Bus to Receiver output	Waveforms 1 & 2, $C_L = 50pF$, $R_L = 667\Omega$		20 30		20 25	ns
t_{PZH}	Enable to HIGH for Bus output	Waveform 3, $C_L = 100pF$, $R_L = 667\Omega$		30		35	ns
t_{PZH}	Enable to HIGH for Receiver output	Waveform 3, $C_L = 50pF$, $R_L = 667\Omega$		25		30	ns
t_{PZL}	Enable to LOW for Bus output	Waveform 4, $C_L = 100pF$, $R_L = 667\Omega$		35		35	ns
t_{PZL}	Enable to LOW for Receiver output	Waveform 4, $C_L = 50pF$, $R_L = 667\Omega$		30		30	ns
t_{PHZ}	Disable from HIGH	Waveform 3, $C_L = 5pF$, $R_L = 667\Omega$, Com'l		25		25	ns
		Waveform 3, $C_L = 50pF$, $R_L = 667\Omega$, Mil		63		63	ns
		Waveform 3, $C_L = 100pF$, $R_L = 667\Omega$, Mil		102		102	ns
t_{PLZ}	Disable from LOW	Waveform 4, $C_L = 5pF$, $R_L = 667\Omega$, Com'l		25		25	ns
		Waveform 4, $C_L = 50pF$, $R_L = 667\Omega$, Mil		29		29	ns
		Waveform 4, $C_L = 100pF$, $R_L = 667\Omega$, Mil		33		33	ns

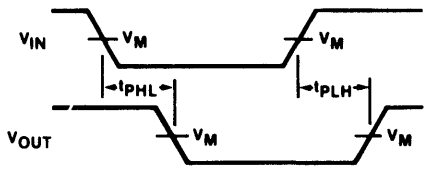
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

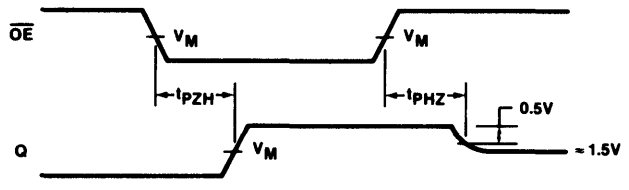
WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 2

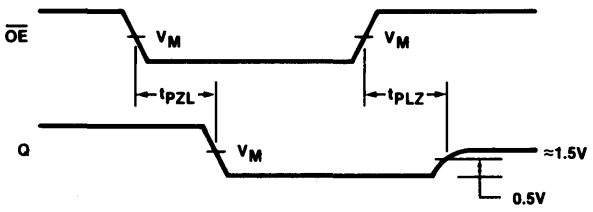
$V_M = 1.3V$

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

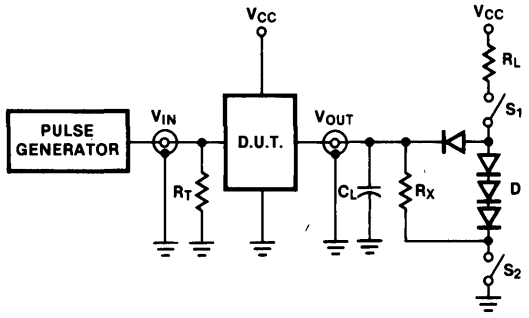
3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



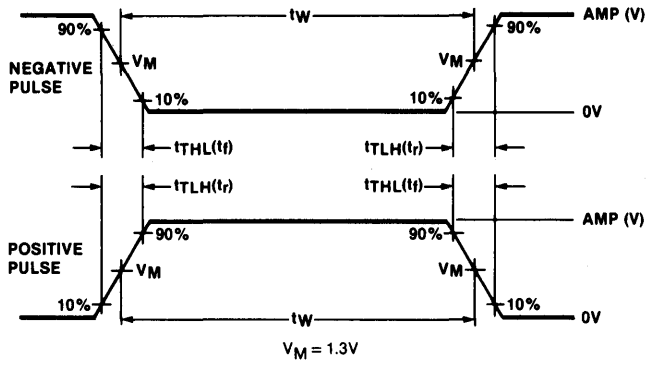
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8T	3.0V	1MHz	500ns	15ns	6ns

8TS805 Octal Transparent Latch With 3-State Outputs
8TS806 Octal D Flip-Flop With 3-State Outputs

- **8-bit transparent latch — 8TS805**
- **8-bit positive, edge-triggered register — 8TS806**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
8TS805	10ns	105mA
8TS806	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N8TS805N • N8TS806N	
Ceramic DIP	N8TS805F • N8TS806F	S8TS805F • S8TS806F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8TS
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
An 8TS unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

DESCRIPTION

The 8TS805 is an octal, transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

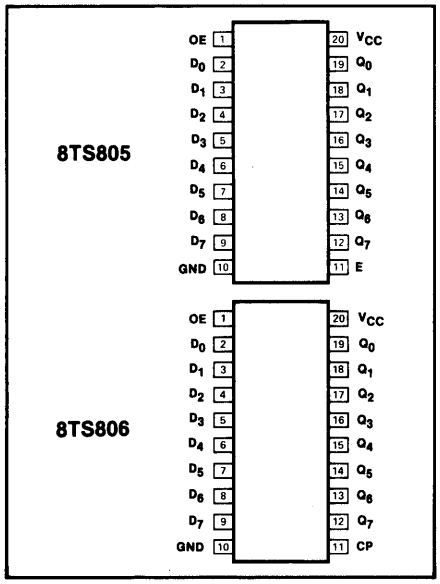
The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

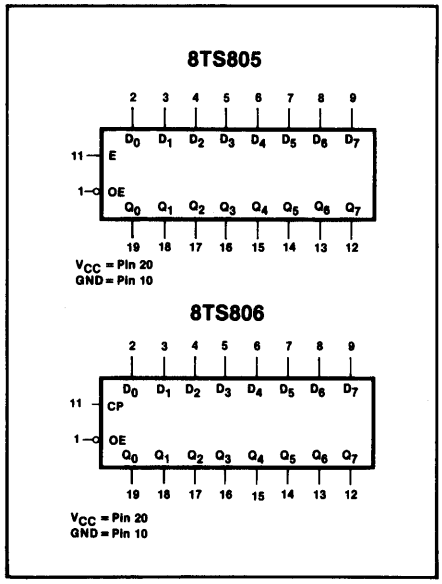
The 8TS806 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

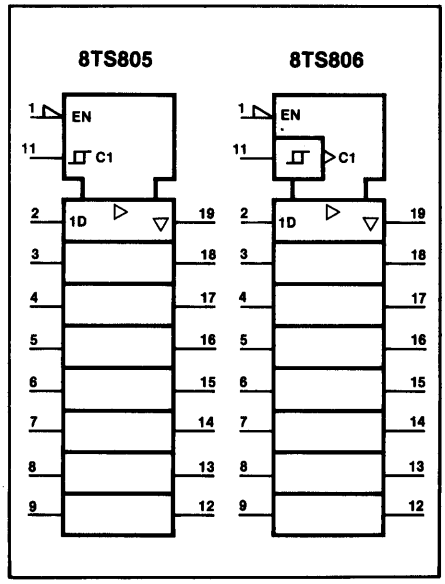
PIN CONFIGURATION



LOGIC SYMBOL



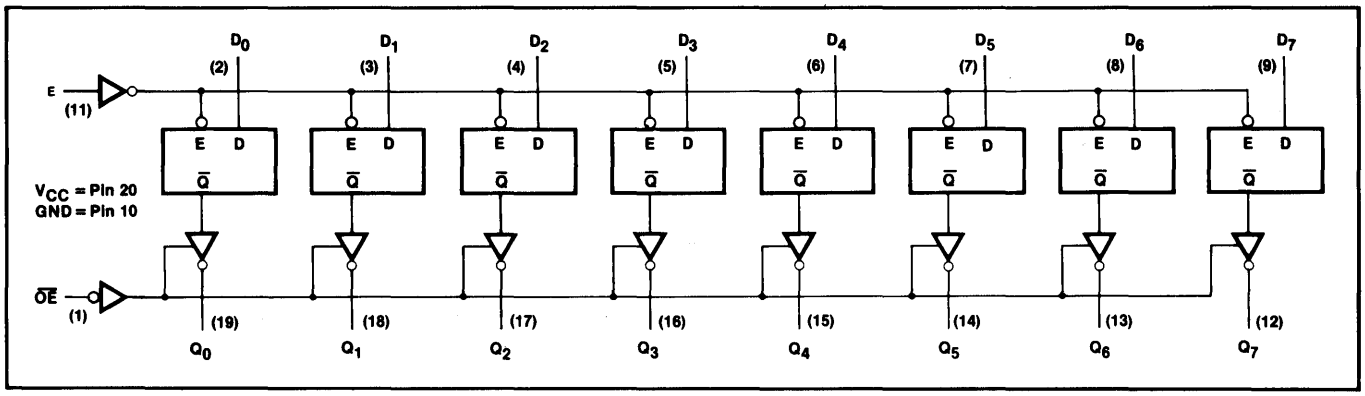
LOGIC SYMBOL (IEEE/IEC)



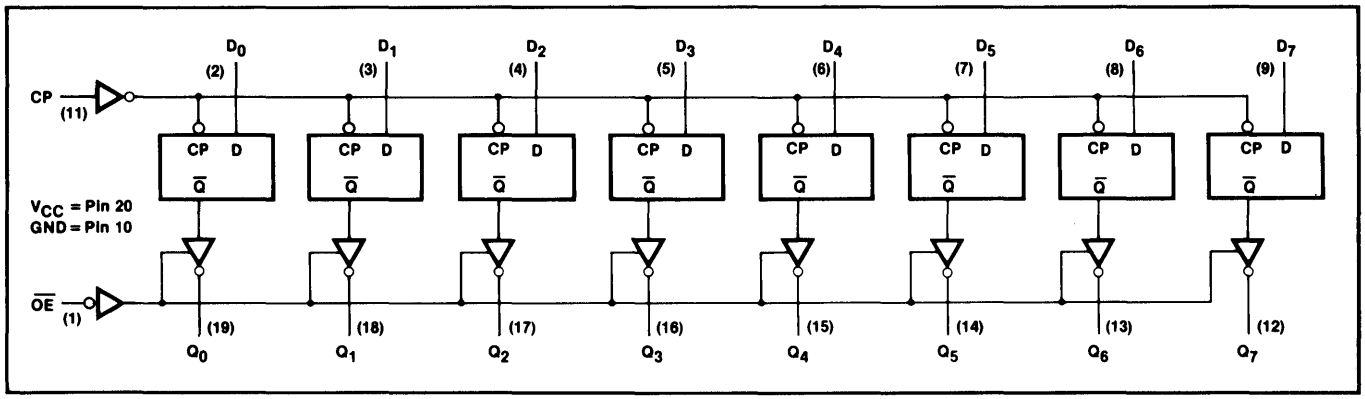
LATCHES/FLIP-FLOPS 8TS805, 806

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 8TS805



LOGIC DIAGRAM, 8TS806



MODE SELECT—FUNCTION TABLE, 8TS805

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0-Q_7
Enable and read register	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	(Z) (Z)

MODE SELECT—FUNCTION TABLE, 8TS806

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW OE transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW OE transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8TS	N8TS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state.	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			8TS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0	mA
		Com'l			−6.5	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.7V MAX for S8TS at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			8TS805, 806			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.0		V
				Com'l	2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.5[4]	V
				Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					-50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					-0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCL}	8TS805		105	160	mA
			I_{CCL}	All inputs grounded, 8TS806		102	140	mA
			I_{CCZ}	CP, $\overline{OE}$ = 4.0V, D inputs = GND, 8TS806		131	180	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = +0.45V MAX for S8TS at T_A = +125°C only.

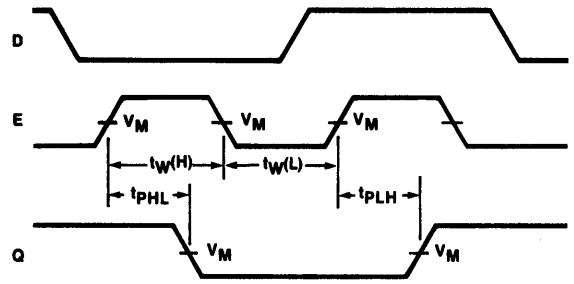
AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	8TS		UNIT
			C_L = 15pF, R_L = 280Ω		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, 8TS806	75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1, 8TS805		14 18	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, 8TS805		9 13	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, 8TS806		15 17	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		15	ns
t_{PZL}	Enable time to LOW level	Waveform 3 8TS805 8TS806		18 18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		12	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

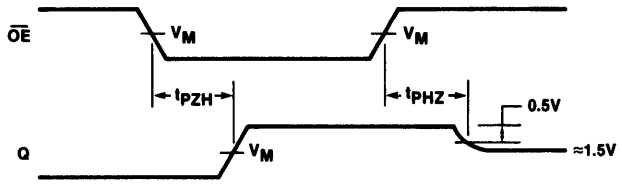
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



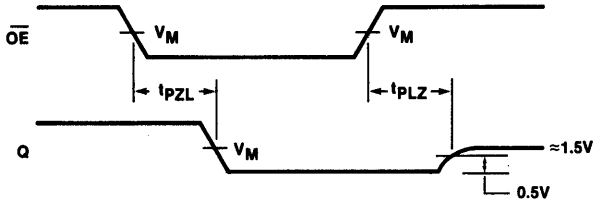
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



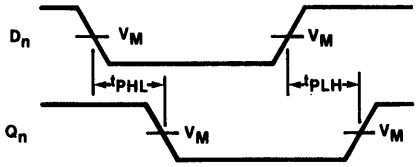
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



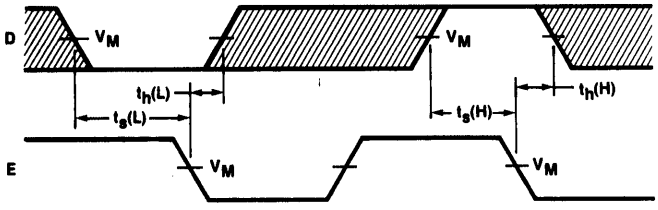
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



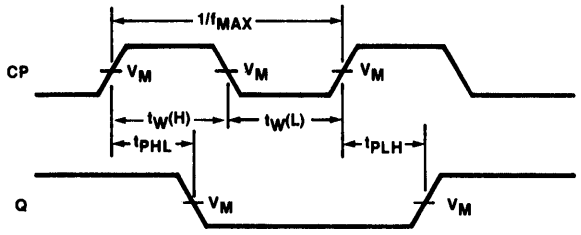
Waveform 4

DATA SETUP AND HOLD TIMES



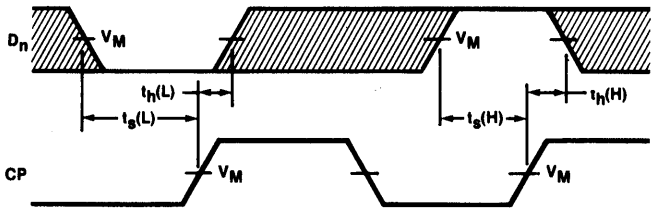
Waveform 5

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

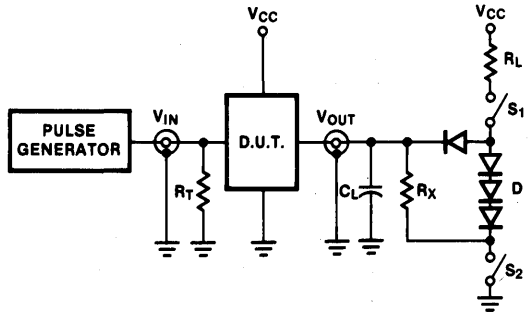
V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	8TS		UNIT
			Min	Max	
$t_{W(H)}$ $t_{W(L)}$	Latch Enable pulse width	Waveform 1, 8TS805	6 7.3		ns
t_s	Setup time, Data to Latch Enable	Waveform 5, 8TS805	0		ns
t_h	Hold time, Data to Latch Enable	Waveform 5, 8TS805	10		ns
$t_{W(H)}$ $t_{W(L)}$	Clock pulse width	Waveform 6, 8TS806	6 7.3		ns
t_s	Setup time, Data to Clock	Waveform 7, 8TS806	5		ns
t_h	Hold time, Data to Clock	Waveform 7, 8TS806	2		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



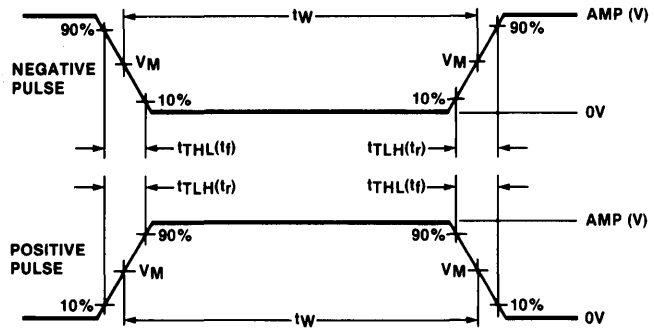
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8TS	3.0V	1MHz	500ns	2.5ns	2.5ns

'807 Octal Transparent Latch With 3-State Outputs
'808 Octal D Flip-Flop With 3-State Outputs

- 8-bit transparent latch — 8TS807
- 8-bit positive, edge-triggered register — 8TS808
- 3-State inverting output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
8TS807	10ns	105mA
8TS808	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N8TS807N • N8TS808N	
Ceramic DIP	N8TS807F • N8TS808F	S8TS807F • S8TS808F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8TS
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
An 8TS unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

DESCRIPTION

The 8TS807 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

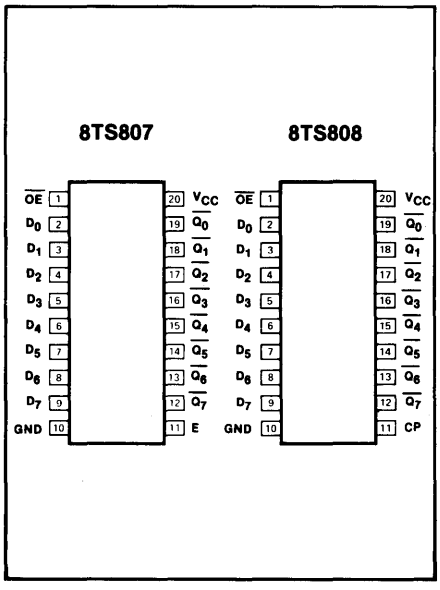
The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

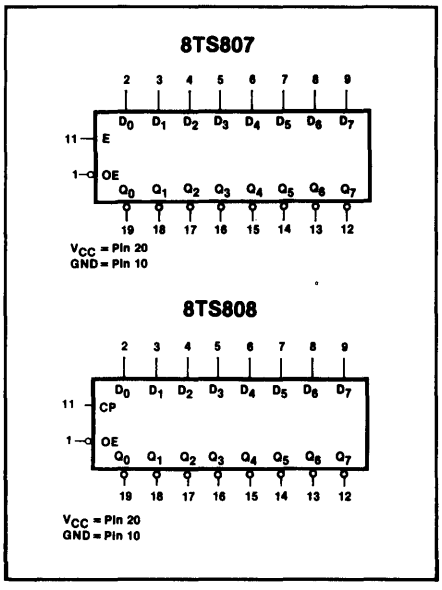
The 8TS808 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The

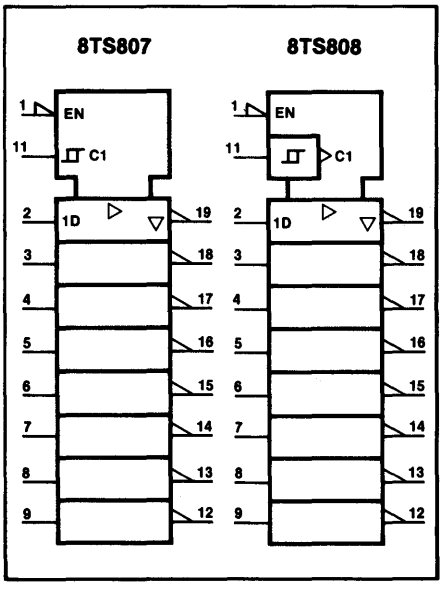
PIN CONFIGURATION



LOGIC SYMBOL

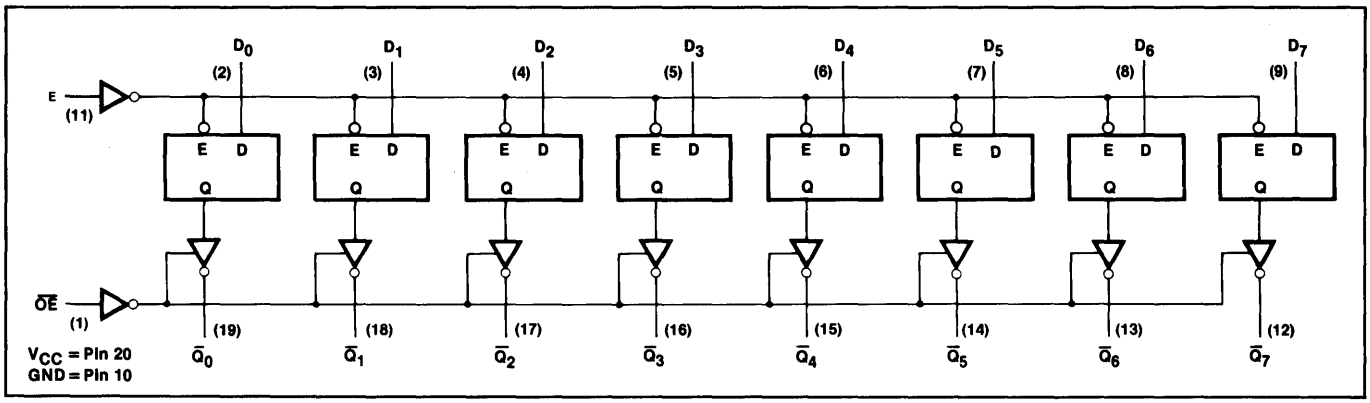


LOGIC SYMBOL (IEEE/IEC)

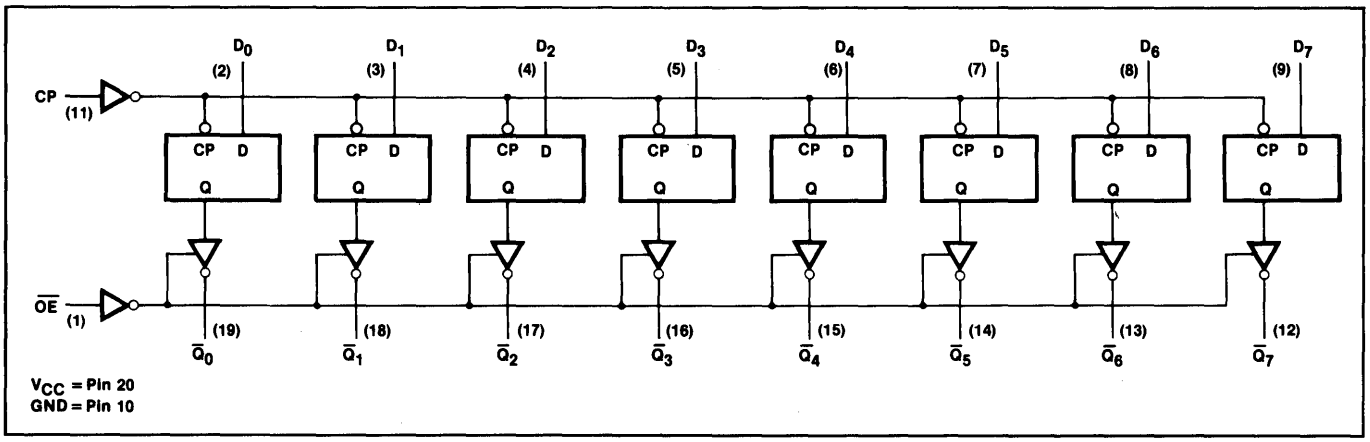


active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 8TS807



LOGIC DIAGRAM, 8TS808



MODE SELECT—FUNCTION TABLE, 8TS807

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0-Q_7
Enable and read register	L	H	L	L	H
	L	H	H	H	L
Latch and read register	L	L	l	L	H
	L	L	h	H	L
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

MODE SELECT—FUNCTION TABLE, 8TS808

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Load register and disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8TS	N8TS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			8TS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0	mA
		Com'l			−6.5	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.7V MAX for S8TS at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			8TS807, 808			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.0		V
				Com'l	2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.5[4]	V
				Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					−0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCL}	8TS807		105	160	mA
			I_{CCL}	All inputs grounded, 8TS808		102	140	mA
			I_{CCZ}	CP, $\overline{OE}$ = 4.0V, D inputs = GND, 8TS807		131	180	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = +0.45V MAX for S8TS at T_A = +125°C only.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	8TS $C_L = 15pF$, $R_L = 280\Omega$ Min	8TS $C_L = 15pF$, $R_L = 280\Omega$ Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 6, 8TS808	75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1, 8TS807		14 18	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, 8TS807		9 13	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, 8TS808		15 17	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		15	ns
t_{PZL}	Enable time to LOW level	Waveform 3 8TS807 8TS808		18 18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, $C_L = 5pF$		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, $C_L = 5pF$		12	ns

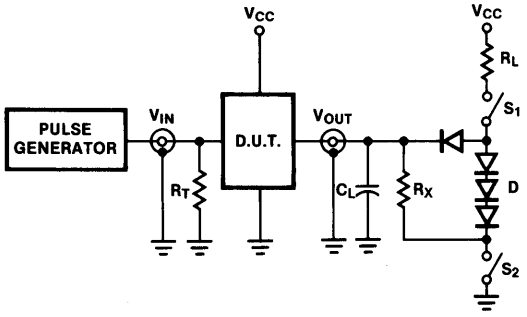
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	8TS Min	8TS Max	UNIT
$t_W(H)$ $t_W(L)$	Latch Enable pulse width	Waveform 1, 8TS807	6 7.3		ns
t_s	Setup time, Data to Latch Enable	Waveform 5, 8TS807	0		ns
t_h	Hold time, Data to Latch Enable	Waveform 5, 8TS807	10		ns
$t_W(H)$ $t_W(L)$	Clock pulse width	Waveform 6, 8TS808	6 7.3		ns
t_s	Setup time, Data to Clock	Waveform 7, 8TS808	5		ns
t_h	Hold time, Data to Clock	Waveform 7, 8TS808	2		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



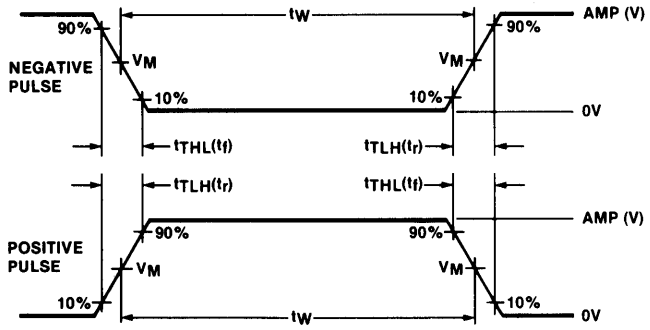
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

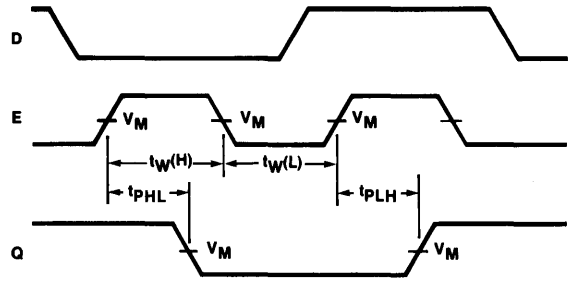


V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8TS	3.0V	1MHz	500ns	2.5ns	2.5ns

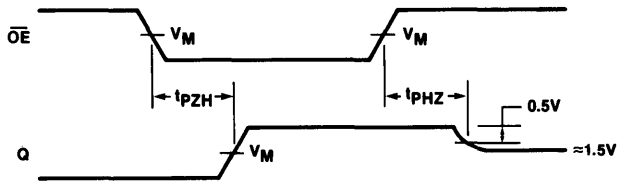
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



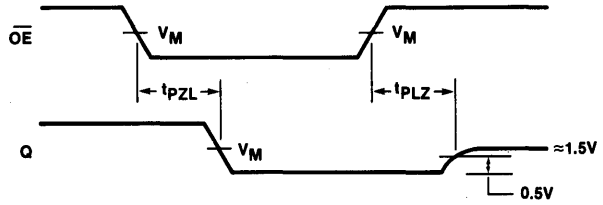
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



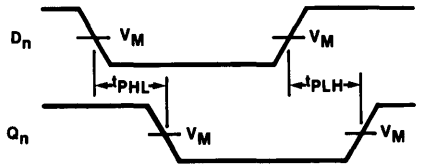
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



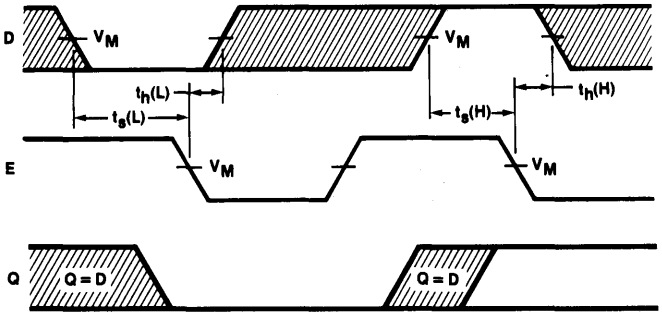
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



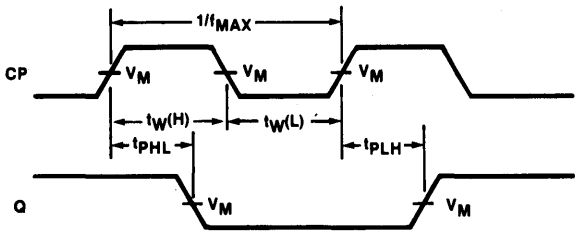
Waveform 4

DATA SETUP AND HOLD TIMES



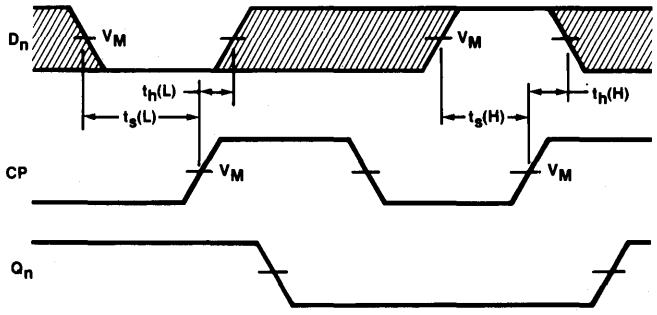
Waveform 5

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

LATCH 8TS809

Octal Transparent Latch With Inverting 3-State Outputs

- **8-bit transparent latch**
- **3-State inverting output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
8TS809	10ns	105mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N8TS809N	
Ceramic DIP	N8TS809F	S8TS809F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8TS
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
An 8TS unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

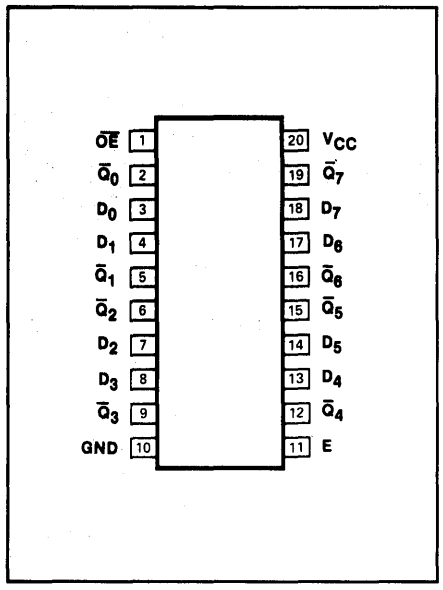
DESCRIPTION

The 8TS809 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

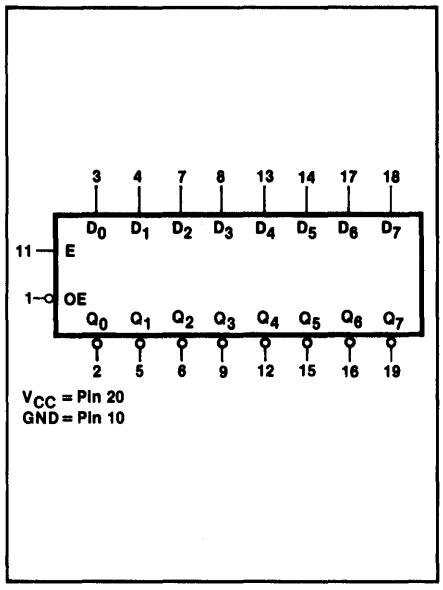
The data on the D inputs are transferred to the inverting latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

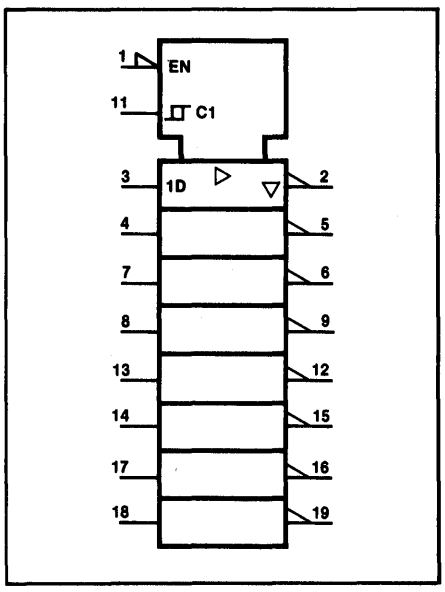
PIN CONFIGURATION



LOGIC SYMBOL

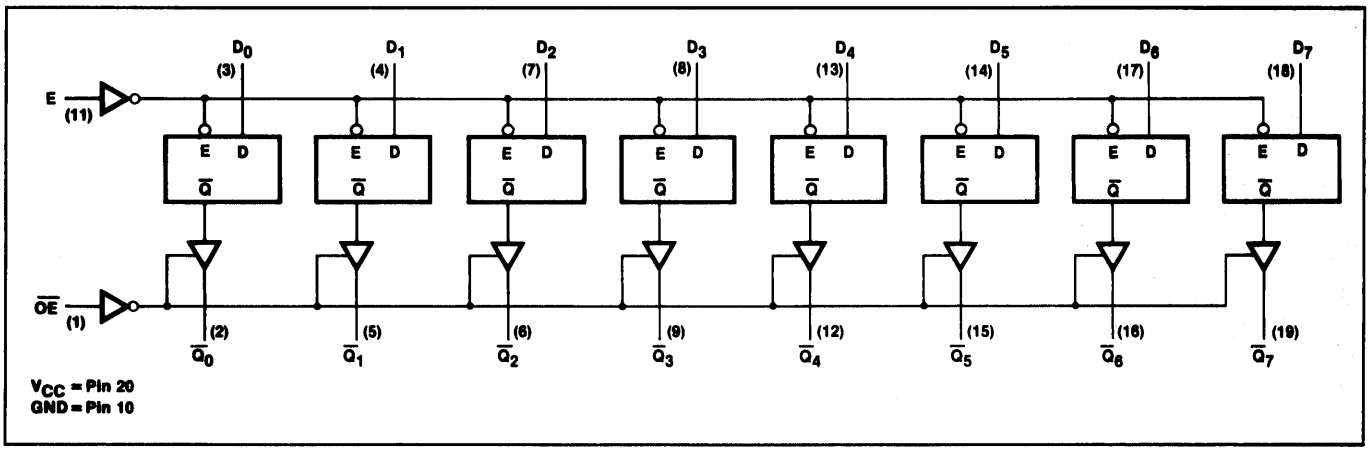


LOGIC SYMBOL (IEEE/IEC)



LATCH 8TS809

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0-Q_7
Enable and read register	L L	H H	L H	L H	H L
Latch and read register	L L	L L	l h	L H	H L
Latch register and disable outputs	H H	L L	l h	L H	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW enable transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8TS	N8TS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

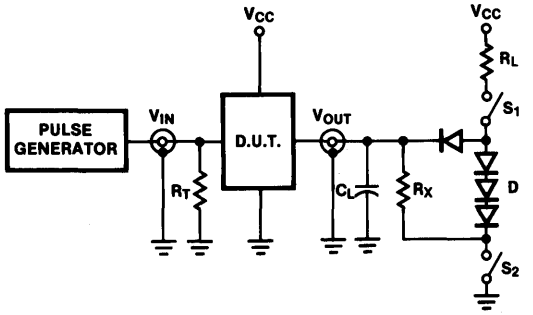
RECOMMENDED OPERATING CONDITIONS

PARAMETER			8TS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0	mA
		Com'l			−6.5	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.7V MAX for S8TS at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

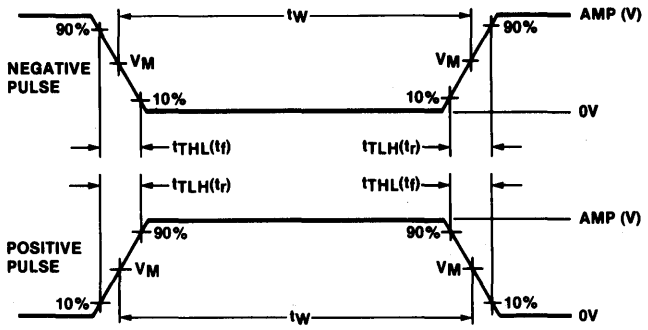


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8TS	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			8TS809			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.0		V
				Com'l	2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.5[4]	V
				Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					-50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					-0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-100	mA
I_{CCL}	Supply current (total)	V_{CC} = MAX				105	160	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = +0.45V MAX for S8TS at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

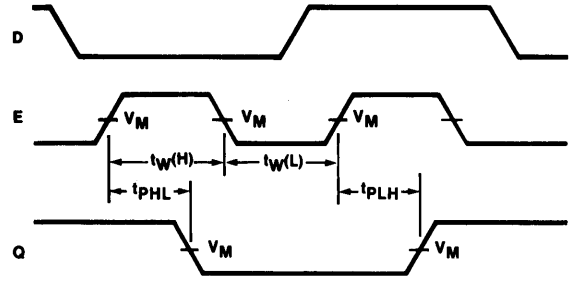
PARAMETER		TEST CONDITIONS	8TS		UNIT
			C_L = 15pF, R_L = 280Ω		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1		14 18	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4		9 13	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		15	ns
t_{PZL}	Enable time to LOW level	Waveform 3		18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		12	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	8TS		UNIT
			Min	Max	
$t_{W(H)}$ $t_{W(L)}$	Latch Enable pulse width	Waveform 1	6 7.3		ns
t_s	Setup time, Data to Latch Enable	Waveform 5	0		ns
t_h	Hold time, Data to Latch Enable	Waveform 5	10		ns

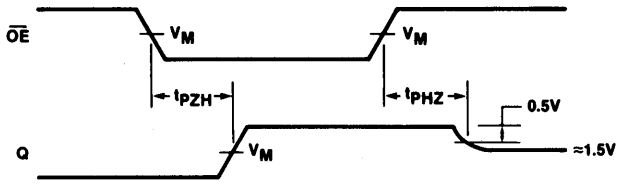
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



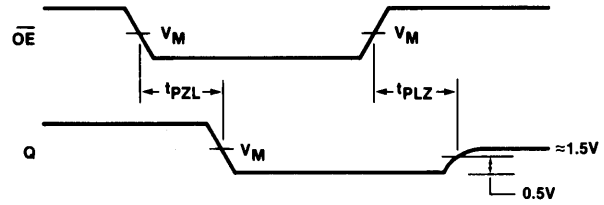
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



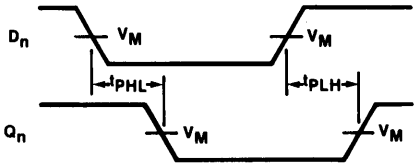
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



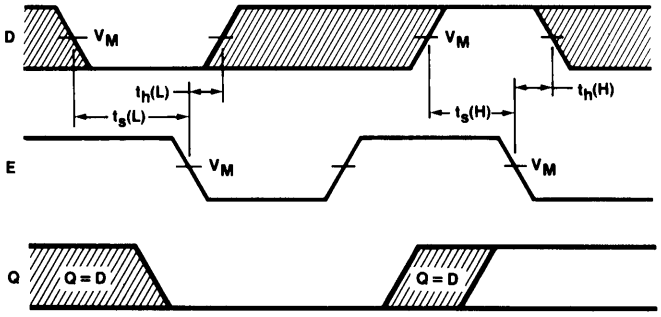
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



Waveform 4

DATA SETUP AND HOLD TIMES



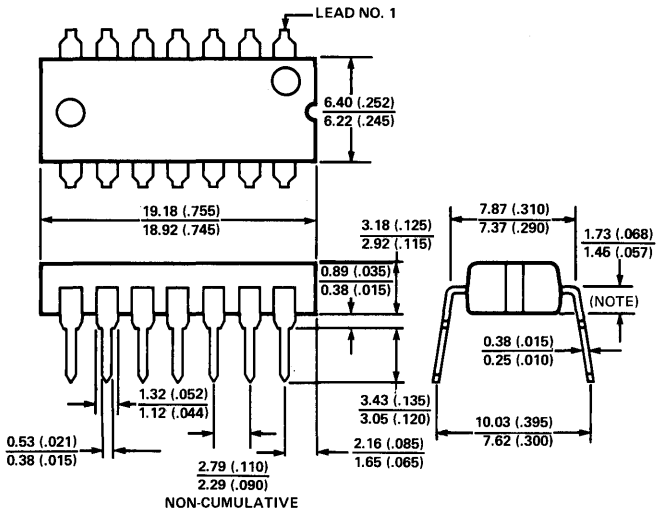
Waveform 5

$V_M = 1.5V$

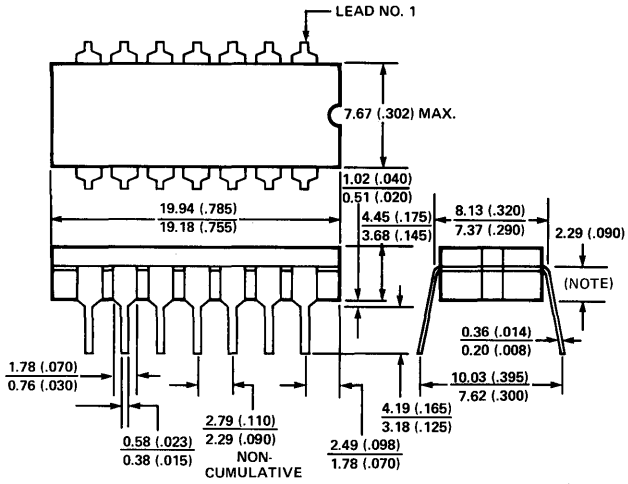
The shaded areas indicate when the input is permitted to change for predictable output performance.

PACKAGE OUTLINES

N PACKAGE (PLASTIC)



F PACKAGE (CERDIP)



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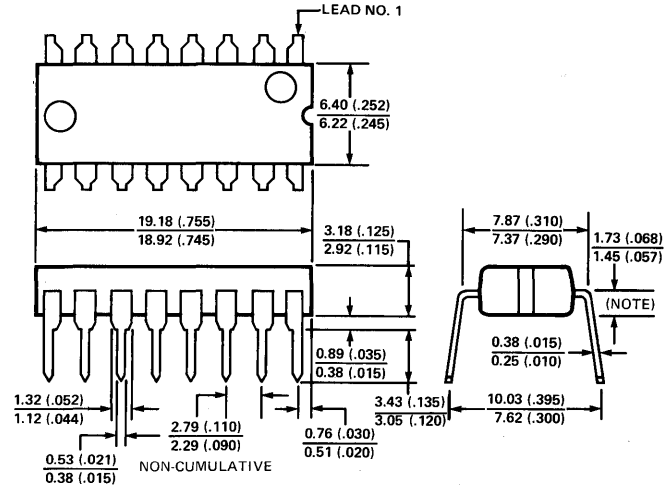

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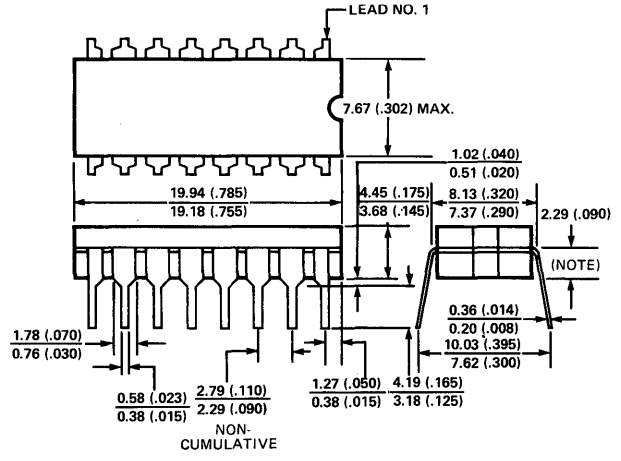
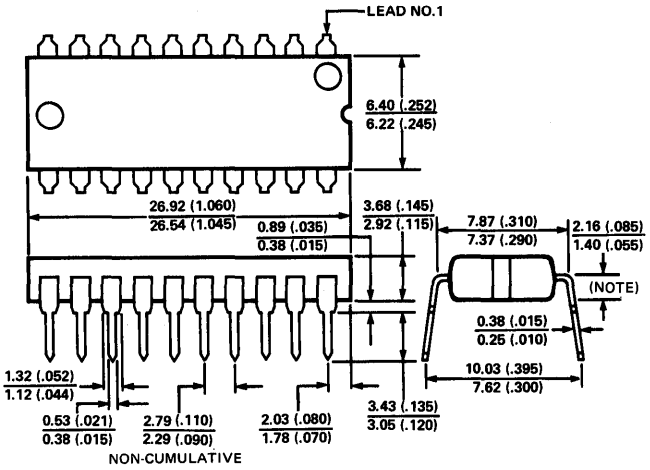


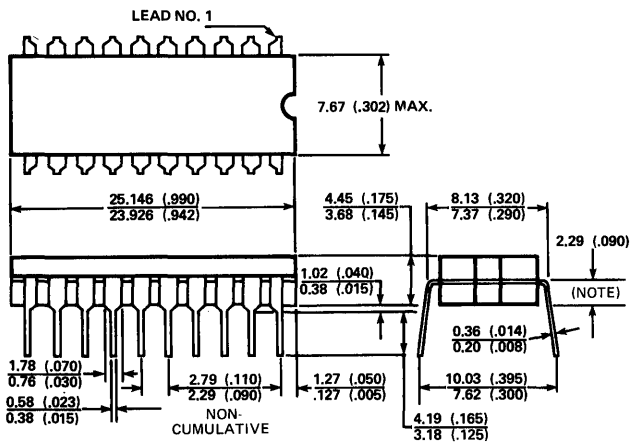
NOTE
Lead spacing shall be measured within this zone.
a. Shoulder and lead tip dimensions are to centerline of leads.

PACKAGE OUTLINES

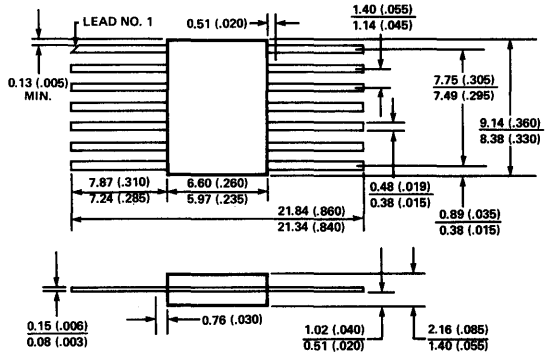
N PACKAGE (PLASTIC)



F PACKAGE (CERDIP)



W PACKAGE (FLAT PAC)



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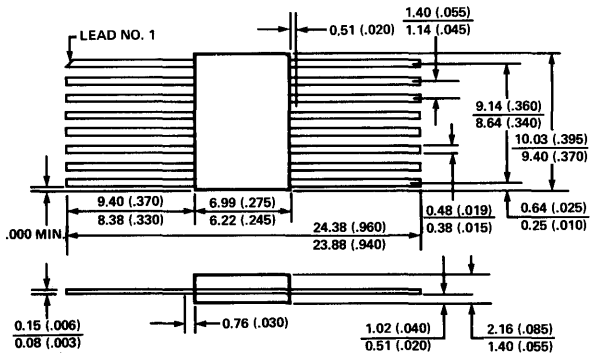

NOTE
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a. Shoulder and lead tip dimensions are to centerline of leads.

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Signetics Corporation
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