Signetics

MOS Microprocessor Data Manual 1982

Microprocessor Data Manual
1982

Contents

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PART NUMBER CONVERSION NOTICE

New part numbers have been assigned to products contained in this data manual. Conversion from old part numbers to new part numbers is shown below.

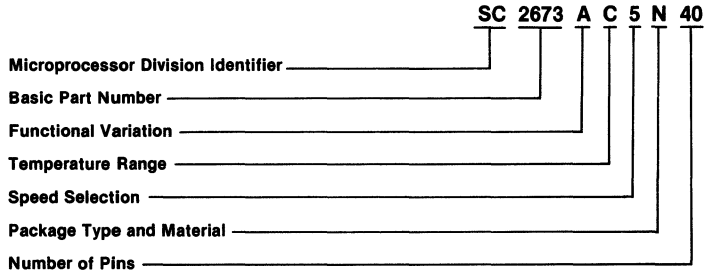
NEW NUMBER	OLD NUMBER
SC2621CSI14	2621I
SC2621CSN14	2621N
SC2622CSI14	2622I
SC2622CSN14	2622N
SC2636CSI40	2636I
SC2636CSN40	2636N
SC2637CSI40	2637I
SC2637CSN40	2637N
SC2650ACSI40	2650AI
SC2650ACSN40	2650AN
SC2650AC1I40	2650A-1I
SC2650AC1N40	2650A-1N
SC2651CSI28	2651I
SC2651CSN28	2651N
SC2652C1I40	2652I
SC2652C1N40	2652N
SC2652C2I40	2652-1I
SC2652C2N40	2652-1N

NEW NUMBER	OLD NUMBER
SC2653CSI16	2653I
SC2653CSN16	2653N
SC2661ACSI28	2661-1I
SC2661BCSI28	2661-2I
SC2661CCSI28	2661-3I
SC2661ACSN28	2661-1N
SC2661BCSN28	2661-2N
SC2661CCSN28	2661-3N
SC2670*CSI28	2670I
SC2670*CSN28	2670N
SC2671ACSI40	2671I
SC2671ACSN40	2671N
SC2672C4I40	2672I
SC2672C4N40	2672N
SC2673BC5I40	2673I
SC2673BC5N40	2673N
SC2673AC5I40	2673AI
SC2673AC5N40	2673AN

*See Data Sheet

PART NUMBERING SYSTEM

The following example illustrates the meaning of the various fields in the part number:



DEFINITION OF TERMS

Microprocessor Products

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Section 1
Data Communications

PROGRAMMABLE COMMUNICATIONS INTERFACE (PCI) SC2651

DESCRIPTION

The Signetics 2651 PCI is a universal synchronous/asychronous data communications controller chip designed for microcomputer systems. It interfaces directly to the Signetics 2650 microprocessor and may be used in a polled or interrupt driven system environment. The 2651 accepts programmed instructions from the microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

The PCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The 2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The PCI is constructed using Signetics n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

FEATURES

- **Synchronous operation**
  - **5 to 8-bit characters**
  - **Single or double SYN operation**
  - **Internal character synchronization**
  - **Transparent or non-transparent mode**
  - **Automatic SYN or DLE-SYN insertion**
  - **SYN or DLE stripping**
  - **Odd, even, or no parity**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 1M bps (1X clock)**
- **Asynchronous operation**
  - **5 to 8-bit characters**
  - **1, 1 1/2 or 2 stop bits**
  - **Odd, even, or no parity**
  - **Parity, overrun and framing error detection**
  - **Line break detection and generation**
  - **False start bit detection**
  - **Automatic serial echo mode**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 1M bps (1X clock)**
    - **dc to 62.5K bps (16X clock)**
    - **dc to 15.625K bps (64X clock)**

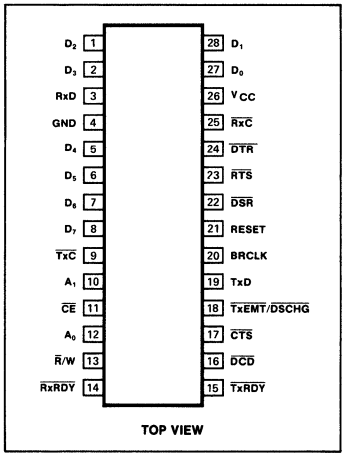
OTHER FEATURES

- **Internal or external baud rate clock**
- **16 internal rates-50 to 19,200 baud**
- **Double buffered transmitter and receiver**
- **Full or half duplex operation**
- **Fully compatible with 2650 CPU**
- **TTL compatible inputs and outputs**
- **Single 5V power supply**
- **No system clock required**
- **28-pin dual in-line package**

APPLICATIONS

- **Intelligent terminals**
- **Network processors**
- **Front end processors**
- **Remote data concentrators**
- **Computer to computer links**
- **Serial peripherals**

PIN CONFIGURATION



TOP VIEW

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
27,28,1,2, 5-8	D_0-D_7	8-bit data bus	I/O
21	RESET	Reset	I
12,10	A_0-A_1	Internal register select lines	I
13	$\overline{R}$/W	Read or write command	I
11	$\overline{CE}$	Chip enable input	I
22	$\overline{DSR}$	Data set ready	I
24	$\overline{DTR}$	Data terminal ready	O
23	$\overline{RTS}$	Request to send	O
17	$\overline{CTS}$	Clear to send	I
16	$\overline{DCD}$	Data carrier detected	I
18	$\overline{TxEMT/DSCHG}$	Transmitter empty or data set change	O
9	$\overline{TxC}$	Transmitter clock	I/O
25	$\overline{RxC}$	Receiver clock	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	$\overline{TxRDY}$	Transmitter ready	O
14	$\overline{RxRDY}$	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5V supply	I
4	GND	Ground	I

ORDERING CODE

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V ±5%, T_A = 0°C to 70°C
Plastic DIP	SC2651CSN28
Ceramic DIP	SC2651CSI28

SEE 2661 FOR ENHANCED PART.

BAUD RATE	THEORETICAL FREQUENCY 16X CLOCK	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
50	0.8 KHz	0.8 KHz	--	6336
75	1.2	1.2	--	4224
110	1.76	1.76	--	2880
134.5	2.152	2.1523	0.016	2355
150	2.4	2.4	--	2112
300	4.8	4.8	--	1056
600	9.6	9.6	--	528
1200	19.2	19.2	--	264
1800	28.8	28.8	--	176
2000	32.0	32.081	0.253	158
2400	38.4	38.4	--	132
3600	57.6	57.6	--	88
4800	76.8	76.8	--	66
7200	115.2	115.2	--	44
9600	153.6	153.6	--	33
19200*	307.2	316.8	3.125	16

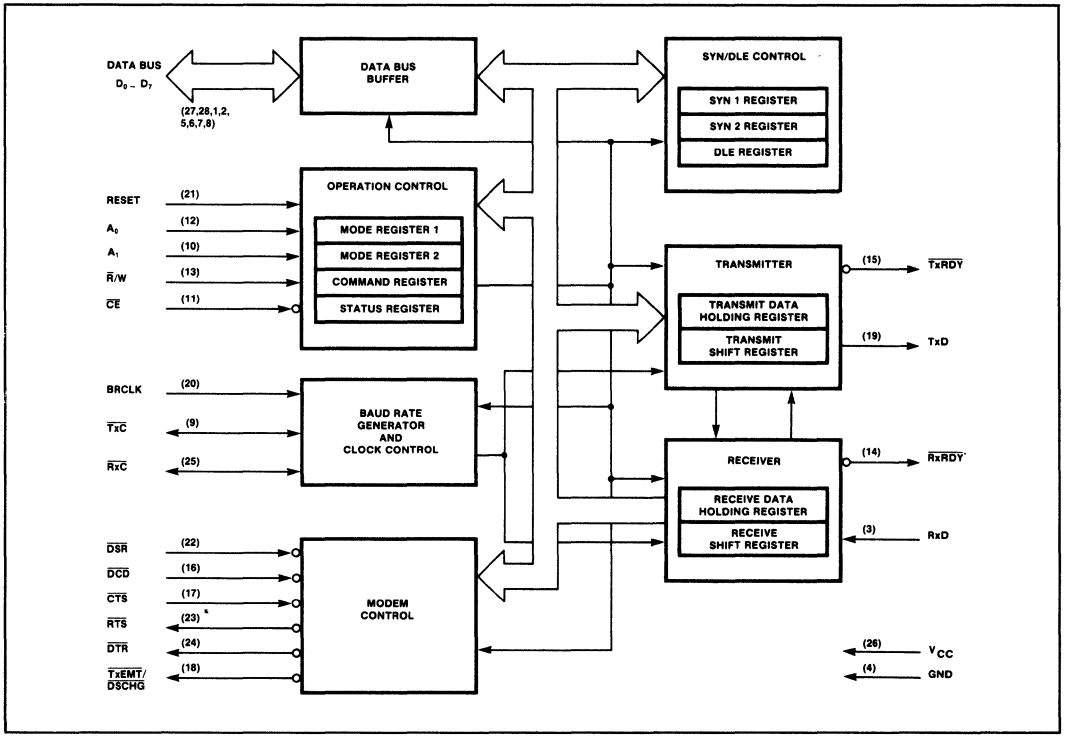
NOTE
*Error at 19200 can be reduced to zero by using crystal frequency 4 9152MHz
16X clock is used in asynchronous mode. In synchronous mode, clock multiplier is 1X

Table 1 BAUD RATE GENERATOR CHARACTERISTICS
Crystal Frequency = 5.0688MHz

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
V_{CC}	26	I	+5V supply input
GND	4	I	Ground
RESET	21	I	A high on this input performs a master reset on the 2651. This signal asynchronously terminates any device activity and clears the Mode, Command and Status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A_1-A_0	10,12	I	Address lines used to select internal PCI registers.
$\overline{R}/W$	13	I	Read command when low, write command when high.
$\overline{CE}$	11	I	Chip enable command. When low, indicates that control and data lines to the PCI are valid and that the operation specified by the $\overline{R}/W$, A_1 and A_0 inputs should be performed. When high, places the D_0-D_7 lines in the tri-state condition.
D_7-D_0	8,7,6,5, 2,1,28,27	I/O	8-bit, three-state data bus used to transfer commands, data and status between PCI and the CPU. D_0 is the least significant bit; D_7 the most significant bit.
$\overline{TxRDY}$	15	O	This output is the complement of Status Register bit SR0. When low, it indicates that the Transmit Data Holding Register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	14	O	This output is the complement of Status Register bit SR1. When low, it indicates that the Receive Data Holding Register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT}/\overline{DSCHG}$	18	O	This output is the complement of Status Register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the Status Register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

Table 2 CPU-RELATED SIGNALS

BLOCK DIAGRAM



BLOCK DIAGRAM

The PCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains Mode Registers 1 and 2, the Command Register, and the Status Register. Details of register addressing and protocol are presented in the PCI Programming section of this data sheet.

Timing

The PCI contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. See Table 1.

Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The Transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

INTERFACE SIGNALS

The PCI interface signals can be grouped into two types: the CPU-related signals (shown in Table 2), which interface the 2651 to the microprocessor system, and the device-related signals (shown in Table 3), which are used to interface to the communications device or system.

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
BRCLK	20	I	5.0688MHz clock input to the internal baud rate generator. Not required if external receiver and transmitter clocks are used.
$\overline{RxC}$	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by Mode Register 1. Data is sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin becomes an output at 1X the programmed baud rate.*
$\overline{TxC}$	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by Mode Register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin becomes an output at 1X the programmed baud rate.*
RxD	3	I	Serial data input to the receiver. "Mark" is high, "Space" is low.
TxD	19	O	Serial data output from the transmitter. "Mark" is high, "Space" is low. Held in Mark condition when the transmitter is disabled.
$\overline{DSR}$	22	I	General purpose input which can be used for Data Set Ready or Ring Indicator condition. Its complement appears as Status Register bit SR7. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{DCD}$	16	I	Data Carrier Detect input. Must be low in order for the receiver to operate. Its complement appears as Status Register bit SR6. Causes a low output on $\overline{TxEMT/DSCHG}$ when its state changes.
$\overline{CTS}$	17	I	Clear to Send input. Must be low in order for the transmitter to operate. If it goes high during transmission, the character in the Transmit Shift Register will be transmitted before termination
$\overline{DTR}$	24	O	General purpose output which is the complement of Command Register bit CR1. Normally used to indicate Data Terminal Ready.
$\overline{RTS}$	23	O	General purpose output which is the complement of Command Register bit CR5. Normally used to indicate Request to Send.

NOTE
*$\overline{RxC}$ and $\overline{TxC}$ outputs have short circuit protection max C_L 100pf

Table 3 DEVICE-RELATED SIGNALS

OPERATION

The functional operation of the 2651 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the PCI Programming section of this data sheet.

After programming, the PCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The 2651 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and the stop bit(s) have been assembled. The data is then transferred to the Receive Data Holding Register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the Holding Register are set to zero. The Parity Error, Framing Error, and Overrun Error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If a break condition is detected (RxD is low for the entire character as well as the stop bit(s)), only one character consisting of all zeros (with the FE status bit set) will be transferred to the Holding Register. The RxD input must return to a high condition before a search for the next start bit begins.

When the PCI is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN (CR2) In this mode, as data is shifted into the Receiver Shift Register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the PCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization). When synchronization has been achieved, the PCI continues to assemble characters and transfer them to the Holding Register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the Holding Register. Note that the SYN characters used to establish initial synchronization are not transferred to the Holding Register in any case.

Transmitter

The PCI is conditioned to transmit data when the $\overline{CTS}$ input is low and the TxEN command register bit is set. The 2651 indicates to the CPU that it can accept a character for transmission by setting the TxRDY

status bit and asserting the $\overline{\text{TxRDY}}$ output. When the CPU writes a character into the Transmit Data Holding Register, these conditions are negated. Data is transferred from the Holding Register to the Transmit Shift Register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the Transmit Holding Register, the TxD output remains in the marking (high) condition and the $\overline{\text{TxEMT/DSCHG}}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the Holding Register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the Send Break command bit high.

In the synchronous mode, when the 2651 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the PCI unless the CPU fails to send a new character to the PCI by the time the transmitter has completed sending the previous character.

Since synchronous communication does not allow gaps between characters, the PCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the Transmit Data Holding Register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in THR.

PCI PROGRAMMING

Prior to initiating data communications, the 2651 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The PCI can be reconfigured at any time during program execution. However, if the change has an effect on the reception of a character the receiver should be disabled. Alternatively if

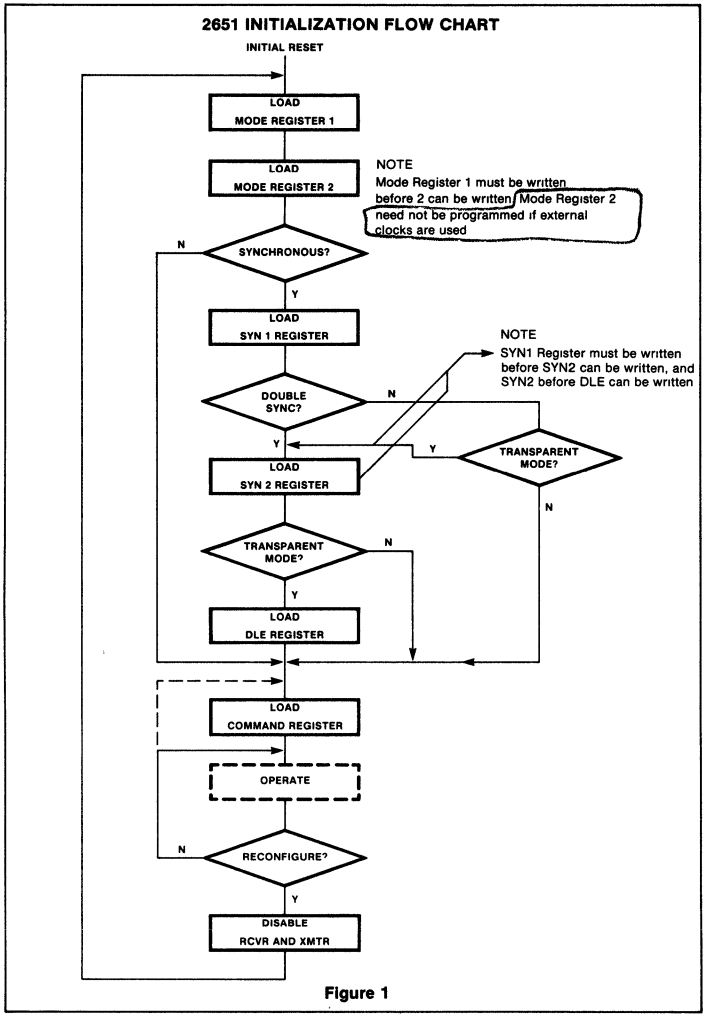


Figure 1

$\overline{CE}$	A_1	A_0	$\overline{R}/W$	FUNCTION
1	X	X	X	Tri-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers 1/2
0	1	0	1	Write mode registers 1/2
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE
See AC Characteristics section for timing requirements

Table 4 2651 REGISTER ADDRESSING

the change is made 1½ RxC periods after RxRDY goes active it will affect the next character assembly A flowchart of the initialization process appears in Figure 1.

The internal registers of the PCI are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A_1 and A_0 inputs. The conditions necessary to address each register are shown in Table 4.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions $A_1=0$, $A_0=1$, and $\overline{R}/W=1$. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses Mode Register 1, and a subsequent operation addresses Mode Register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register The pointers are reset to SYN1 Register and Mode Register 1 by a RESET input or by performing a "Read Command Register" operation, but are unaffected by any other read or write operation.

The 2651 register formats are summarized in Tables 5, 6, 7 and 8. Mode Registers 1 and 2 define the general operational characteristics of the PCI, while the Command Register controls the operation within this basic frame-work. The PCI indicates its status in the Status Register. These registers are cleared when a RESET input is applied.

Mode Register 1 (MR1)

Table 5 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25

MR13 and MR12 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asychronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits (If 1X baud rate is programmed, 1 5 stop bits defaults to 1 stop bits on transmit). In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1-SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill and SYN Detect, but the normal synchronization sequence is used Also DLE stripping and DLE Detect (with MR14 = 0) are enabled

Mode Register 2 (MR2)

Table 6 illustrates Mode Register 2. MR23, MR22, MR21, and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable. When driven by a 5.0688 MHz input at the BRCLK input (pin 20), the BRG output has zero error except at 134.5, 2000, and 19,200 baud, which have errors of +0.016%, +0.235%, and +3.125% respectively.

MR25 and MR24 select either the BRG or the external inputs $\overline{TxC}$ and $\overline{RxC}$ as the clock source for the transmitter and receiver, respectively. If the BRG clock is selected,

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
ASYNCH: STOP BIT LENGTH 00 = INVALID 01 = 1 STOP BIT 10 = 1½ STOP BITS 11 = 2 STOP BITS		0 = ODD 1 = EVEN	0 = DISABLED 1 = ENABLED	00 = 5 BITS 01 = 6 BITS 10 = 7 BITS 11 = 8 BITS		00 = SYNCHRONOUS 1X RATE 01 = ASYNCHRONOUS 1X RATE 10 = ASYNCHRONOUS 16X RATE 11 = ASYNCHRONOUS 64X RATE	
SYNCH: NUMBER OF SYN CHAR 0 = DOUBLE SYN 1 = SINGLE SYN	SYNCH: TRANSPARENCY CONTROL 0 = NORMAL 1 = TRANSPARENT						

NOTE
Baud rate factor in asynchronous applies only if external clock is selected Factor is 16X if internal clock is selected Mode must be selected (MR11, MR10) in any case

Table 5 MODE REGISTER 1 (MR1)

MR27	MR26	MR25	MR24	MR23	MR22	MR21	MR20
		Transmitter Clock	Receiver Clock	Baud Rate Selection			
NOT USED		0 = EXTERNAL 1 = INTERNAL	0 = EXTERNAL 1 = INTERNAL	0000 = 50 BAUD 0001 = 75 0010 = 110 0011 = 134 5 0100 = 150 0101 = 300 0110 = 600 0111 = 1200		1000 = 1800 BAUD 1001 = 2000 1010 = 2400 1011 = 3600 1100 = 4800 1101 = 7200 1110 = 9600 1111 = 19,200	

Table 6 MODE REGISTER 2 (MR2)

the baud rate factor in asynchronous mode is 16X regardless of the factor selected by MR11 and MR10. In addition, the corresponding clock pin provides an output at 1X the baud rate.

Command Register (CR)

Table 7 illustrates Command Register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge Disabling the receiver causes $\overline{RxRDY}$ to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the Transmit Shift Register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high) while the $\overline{TxRDY}$ and $\overline{TxEMT}$ will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected.

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs is the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for a least one bit time before beginning transmission of the next character in the Transmit Data Holding Register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the Transmit Data Holding Register. CR3 should be reset in response to the next TxRDY.

Setting CR4 causes the error flags in the Status Register (SR3, SR4, and SR5) to be cleared This is a one time command There is no internal latch for this bit.

The PCI can operate in one of four submodes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the Mode and Status Register instructions.

In asynchronous mode, CR7-CR6 = 01 places the PCI in the Automatic Echo mode. Clocked, regenerated received data is automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in Automatic Echo mode:

1 Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output
2 The transmitter is clocked by the receive clock
3. $\overline{TxRDY}$ output = 1.
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored

In synchronous mode, CR7-CR6 = 01 places the PCI in the Automatic SYN/DLE Stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16 = 10), characters in the data stream matching SYN1 are not transferred to the Receive Data Holding Register (RHR)
2. In the non-transparent, double SYN mode (MR17-MR16 = 00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR However, only the first SYN1 of an SYN1-SYN1 pair is stripped
3 In transparent mode (MR16 =1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped

Note that Automatic Stripping mode does not affect the setting of the DLE Detect and SYN Detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured In Local Loop Back mode (CR7-CR6 = 10), the following loops are connected internally:

1 The transmitter output is connected to the receiver input
2 $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$
3 The receiver is clocked by the transmit clock
4 The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high
5 The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored

Additional requirements to operate in the Local Loop Back mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the PCI.

The second diagnostic mode is the Remote Loop Back mode (CR7-CR6 = 11) In this mode·

1. Data assembled by the receiver is automatically placed in the Transmit Holding Register and retransmitted by the transmitter on the TxD output
2 The transmitter is clocked by the receive clock
3 No data is sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4 The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held high
5. CR1 (TxEN) is ignored
6 All other signals operate normally

Status Register

The data contained in the Status Register (as shown in Table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the Transmitter Ready (TxRDY) status bit It, and its corresponding output, are valid only when the transmitter is enabled If equal to 0, it indicates that the Transmit Data Holding Register has been loaded by the CPU and the data has not been transferred to the Transmit Shift Register. If set equal to 1, it indicates that the Holding Register is ready to accept data from the CPU. This bit is initially set when the Transmitter is enabled by CR0, unless a character

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode		Request to Send	Reset Error		Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00 = NORMAL OPERATION 01 = ASYNCH. AUTOMATIC ECHO MODE SYNCH SYN AND/OR DLE STRIPPING MODE 10 = LOCAL LOOP BACK 11 = REMOTE LOOP BACK		0 = FORCE $\overline{RTS}$ OUTPUT HIGH 1 = FORCE $\overline{RTS}$ OUTPUT LOW	0 = NORMAL 1 = RESET ERROR FLAG IN STATUS REG (FE, OE, PE/DLE DETECT)	**ASYNCH: FORCE BREAK** 0 = NORMAL 1 = FORCE BREAK **SYNCH: SEND DLE** 0 = NORMAL 1 = SEND DLE	0 = DISABLE 1 = ENABLE	0 = FORCE $\overline{DTR}$ OUTPUT HIGH 1 = FORCE $\overline{DTR}$ OUTPUT LOW	0 = DISABLE 1 = ENABLE

Table 7 COMMAND REGISTER (CR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrrun**	**PE/DLE Detect**	**TxEMT/DSCHG**	**RxRDY**	**TxRDY**
0 = $\overline{DSR}$ INPUT IS HIGH 1 = $\overline{DSR}$ INPUT IS LOW	0 = $\overline{DCD}$ INPUT IS HIGH 1 = $\overline{DCD}$ INPUT IS LOW	**ASYNCH:** 0 = NORMAL 1 = FRAMING ERROR **SYNCH:** 0 = NORMAL 1 = SYN CHAR DETECTED	0 = NORMAL 1 = OVERRUN ERROR	**ASYNCH:** 0 = NORMAL 1 = PARITY ERROR **SYNCH:** 0 = NORMAL 1 = PARITY ERROR OR DLE CHAR RECEIVED	0 = NORMAL 1 = CHANGE IN $\overline{DSR}$ OR $\overline{DCD}$, OR TRANSMIT SHIFT REGISTER IS EMPTY	0 = RECEIVE HOLDING REG EMPTY 1 = RECEIVE HOLDING REG HAS DATA	0 = TRANSMIT HOLDING REG BUSY 1 = TRANSMIT HOLDING REG EMPTY

Table 8 STATUS REGISTER (SR)

has previously been loaded into the Holding Register. It is not set when the Automatic Echo or Remote Loop Back modes are programmed. When this bit is set, the $\overline{TxRDY}$ output pin is low. In the Automatic Echo and Remote Loop Back modes, the output is held high.

SR1, the Receiver Ready (RxRDY) status bit, indicates the condition of the Receive Data Holding Register. If set, it indicates that a character has been loaded into the Holding Register from the Receive Shift Register and is ready to be read by the CPU. If equal to zero, there is no new character in the Holding Register. This bit is cleared when the CPU reads the Receive Data Holding Register or when the receiver is disabled by CR2. When set, the $\overline{RxRDY}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs or that the Transmit Shift Register has completed transmission of a character and no new character has been loaded into the Transmit Data Holding Register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the Transmit Data Holding Register. The DSCHG condition is enabled when TxEN=1 or RxEN=1. It is cleared when the Status Register is read by the CPU. When SR2 is set, the TxEMT/DSCHG output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching the DLE Register has been received. However, only the first DLE of two successive DLEs will set SR3. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

The Overrun Error status bit, SR4, indicates that the previous character loaded into the Receive Holding Register was not read by the CPU at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled and by the Reset Error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by the programmed number of stop bits. (If 1.5 stop bits are programmed, only the first stop bit is checked.) If RHR = 0 when SR5 = 1 a break condition is present. In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character is single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the Reset Error command is given in asynchronous mode, and when the Status Register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the conditions of the $\overline{DCD}$ and $\overline{DSR}$ inputs respectively. A low input sets its corresponding status bit and a high input clears it.

DC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ [4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low				0.8	
V_{IH}	High		2.0			
	Output voltage					V
V_{OL}	Low	$I_{OL} = 1.6mA$			0.4	
V_{OH}	High	$I_{OH} = -100\mu A$	2.4			
I_{IL}	Input leakage current	$V_{IN} = 0$ to 5.25V	-10		10	μA
Tristate	Output leakage current					μA
I_{LH}	Data bus high	$V_O = 4.0V$	-10		10	
I_{LL}	Data bus low	$V_O = 0.45V$	-10		10	
I_{CC}	Power supply current				150	mA

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	-65 to +150	°C
All voltages with respect to ground[3]	-0.5 to +6.0	V

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6]

	PARAMETER	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
	Pulse width					ns
t_{RES}	Reset		1000			
t_{CE}	Chip enable		300			
	Setup and hold time					ns
t_{AS}	Address setup		20			
t_{AH}	Address hold		20			
t_{CS}	$\overline{R}$/W control setup		20			
t_{CH}	$\overline{R}$/W control hold		20			
t_{DS}	Data setup for write		225			
t_{DH}	Data hold for write		0			
t_{RXS}	Rx data setup		300			
t_{RXH}	Rx data hold		350			
t_{DD}	Data delay time for read	$C_L = 100pF$			250	ns
t_{DF}	Data bus floating time for read	$C_L = 100pF$			150	ns
t_{CED}	$\overline{CE}$ to $\overline{CE}$ delay		700			ns
	Input clock frequency					MHz
f_{BRG}	Baud rate generator		1.0	5.0688	5.0738	
$f_{R/T}$[10]	$\overline{TxC}$ or $\overline{RxC}$		dc		1.0	
	Clock width					ns
t_{BRH}[9]	Baud rate high		70			
t_{BRL}[9]	Baud rate low		70			
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ high		500			
$t_{R/TL}$[10]	$\overline{TxC}$ or $\overline{RxC}$ low		500			
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$	$C_L = 100pF$			650	ns
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output[8]	$C_L = 100pF$		0		ns

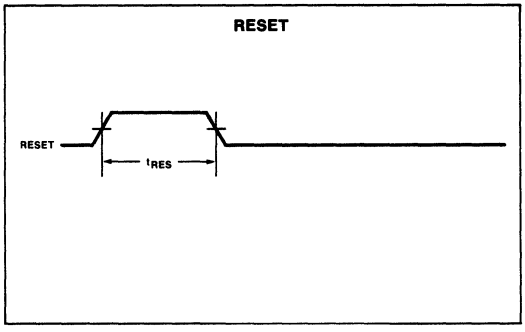
NOTES

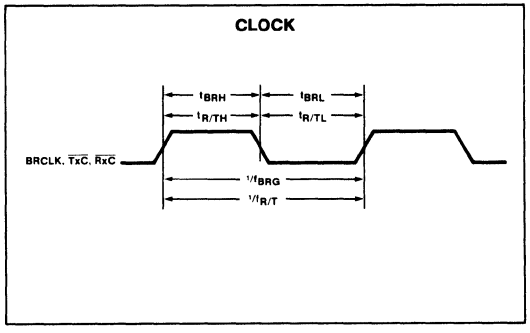
1 Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied
2 For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient (IQ ceramic package)
3 This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima
4. Parameters are valid over operating temperature range unless otherwise specified
5 All voltage measurements are referenced to ground All time measurements are at the 50% level for inputs (except t_{BRH} and T_{BRL}) and at 0 8V and 2 0V for outputs Input levels for testing are 0 45V and 2 4V
6 Typical values are at +25° C, typical supply voltages and typical processing parameters
7 $\overline{TxRDY}$, $\overline{RxRDY}$ and $\overline{TxEMT}/\overline{DSCHG}$ outputs are open drain
8 Parameter applies when internal transmitter clock is used
9 Under test conditions of 5 0688 MHz f_{BRG} t_{BRH} and t_{BRL} measured at V_{IH} and V_{IL} respectively
10 $f_{R/T}$ and $t_{R/TL}$ shown for all modes except Local Loopback For Local Loopback mode $f_{R/T}$ = 0 7 MHz and $t_{R/TL}$ = 700ns min

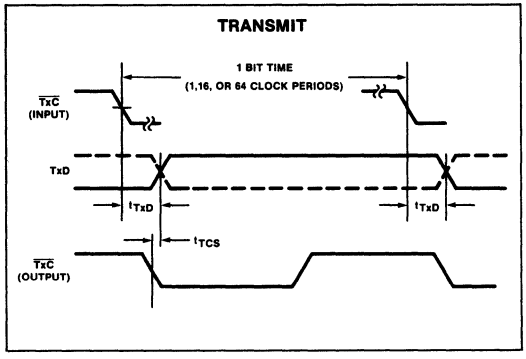
CAPACITANCE $T_A = 25°C$, $V_{CC} = 0V$

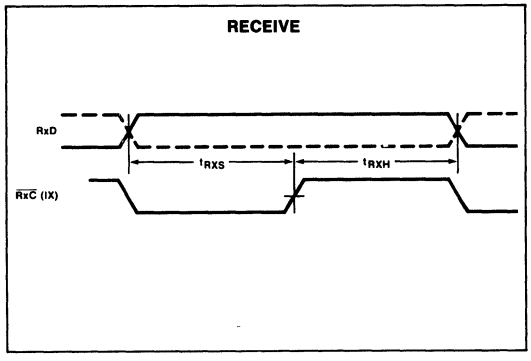
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Capacitance					pF
C_{IN}	Input	fc = 1MHz			20	
C_{OUT}	Output	Unmeasured pins tied to ground			20	
$C_{I/O}$	Input/Output				20	

TIMING DIAGRAMS



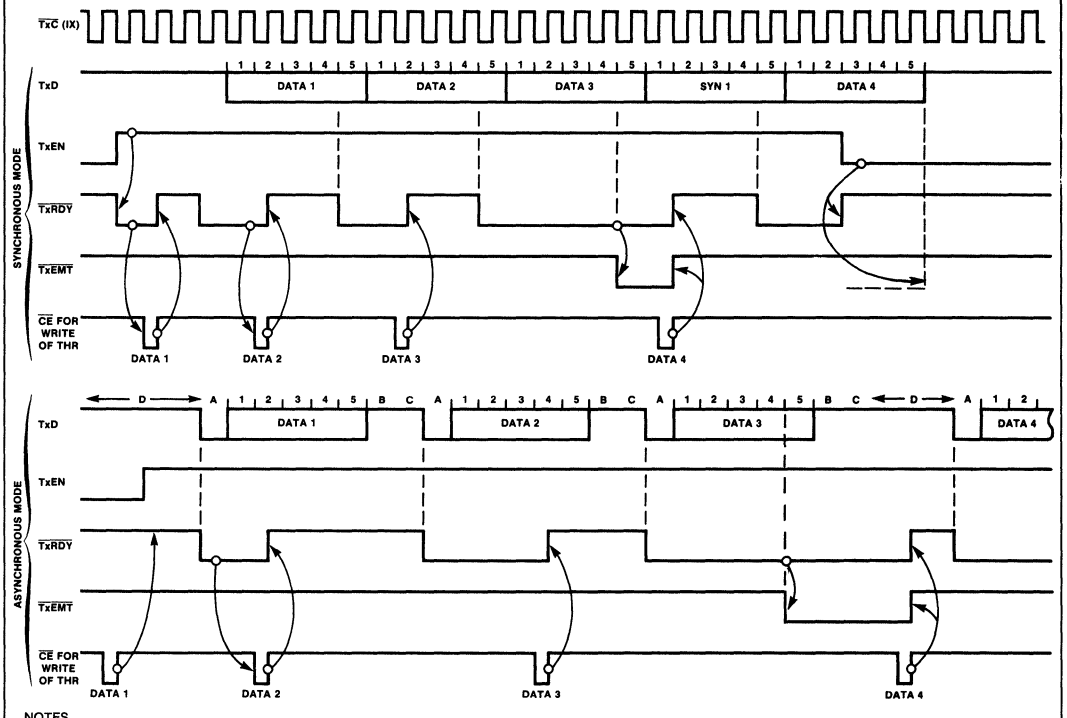






TIMING DIAGRAMS (Cont'd)

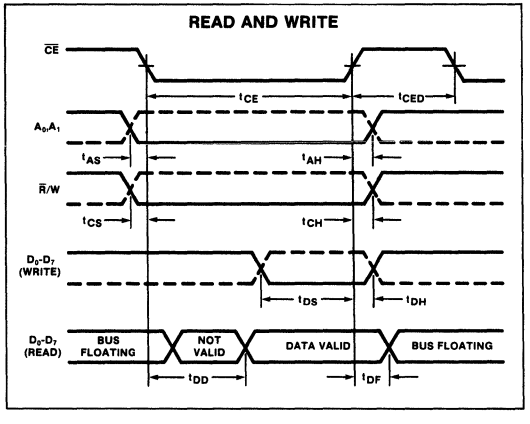
TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



NOTES

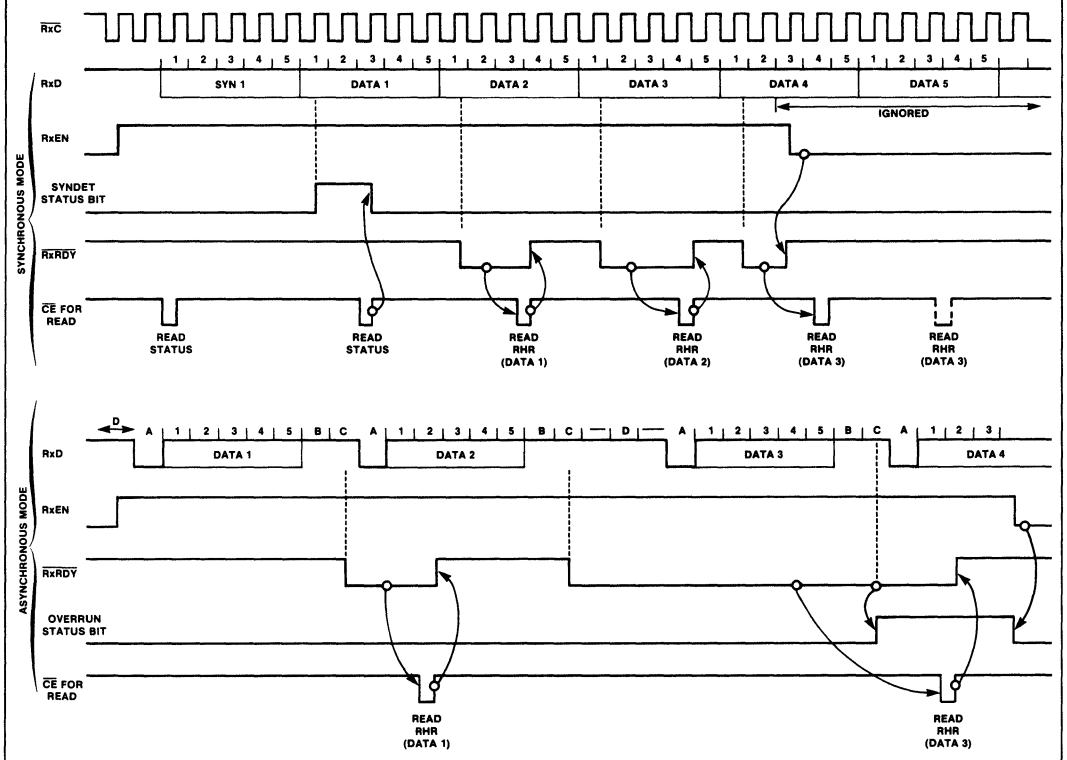
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit



TIMING DIAGRAMS (Cont'd)

RxRDY (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])

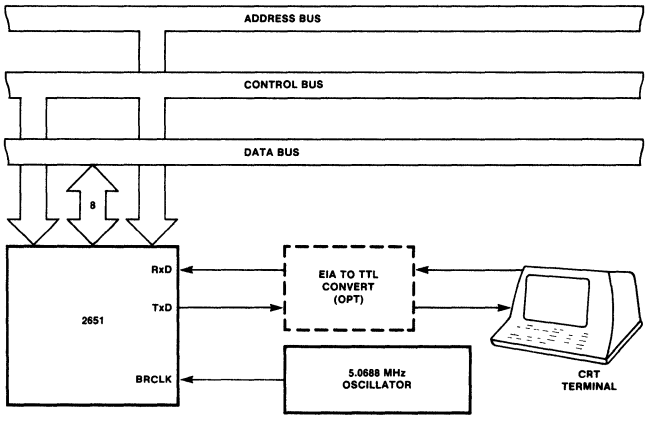


NOTES

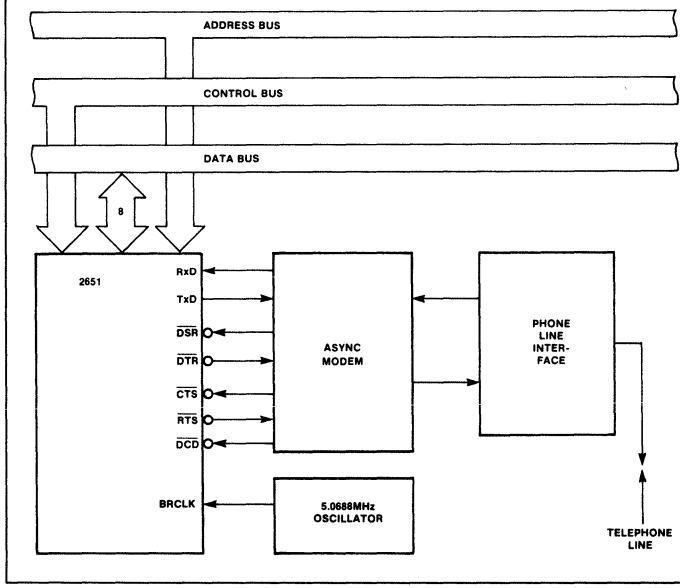
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition

TYPICAL APPLICATIONS

ASYNCHRONOUS INTERFACE TO CRT TERMINAL

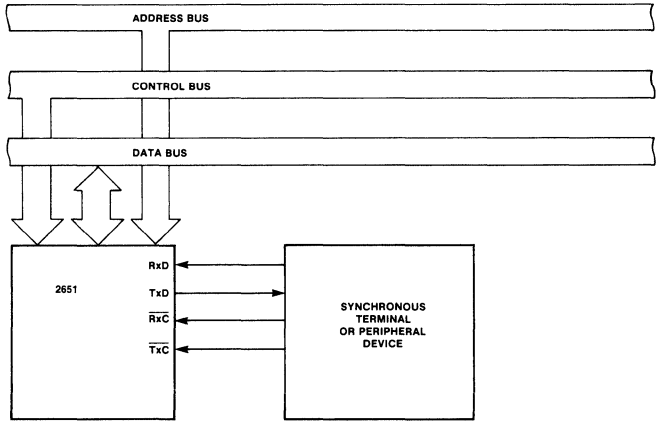


ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

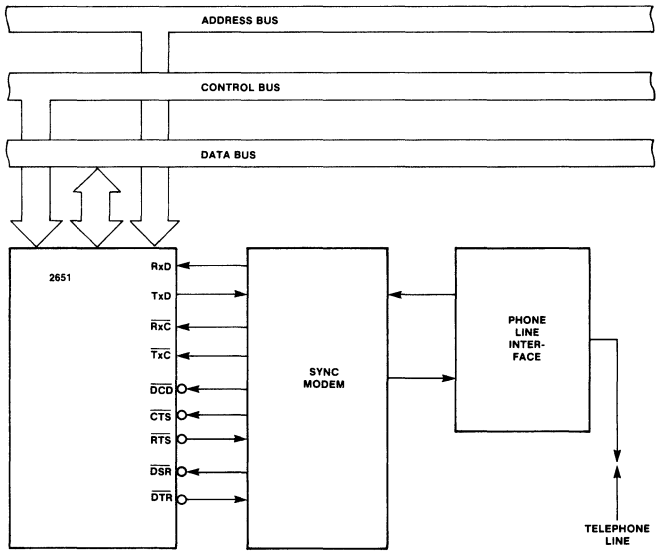


TYPICAL APPLICATIONS (Cont'd)

SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



Manufacturer reserves the right to make design and process changes and improvements.

MULTI-PROTOCOL COMMUNICATIONS CONTROLLER (MPCC) SC2652

DESCRIPTION

The 2652 Multi-Protocol Communications Controller (MPCC) is a monolithic n-channel MOS LSI circuit that formats, transmits and receives synchronous serial data while supporting bit-oriented or byte control protocols. The chip is TTL compatible, operates from a single +5V supply, and can interface to a processor with an 8 or 16-bit bidirectional data bus

FEATURES

- **DC to 1Mbps data rate, 2652-1 to 2Mbps**
- **Bit-oriented protocols (BOP): SDLC, ADCCP, HDLC**
- **Byte-control protocols (BCP): DDCMP, BISYNC (external CRC)**
- **Programmable operation**
  - **8 or 16-bit tri-state data bus**
  - **Error control—CRC or VRC or none**
  - **Character length—1 to 8 bits for BOP or 5 to 8 bits for BCP**
  - **SYNC or secondary station address comparison for BCP-BOP**
  - **Idle transmission of SYNC/FLAG or MARK for BCP-BOP**
- **Automatic detection and generation of special BOP control sequences, i.e., FLAG, ABORT, GA**
- **Zero insertion and deletion for BOP**
- **Short character detection for last BOP data character**
- **SYNC generation, detection, and stripping for BCP**
- **Maintenance Mode for self-testing**
- **TTL compatible**
- **Single +5V supply**

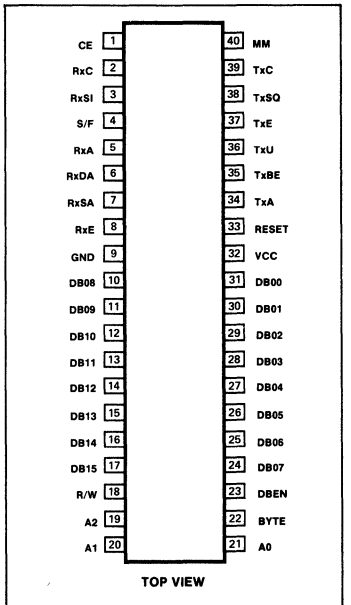
APPLICATIONS

- **Intelligent terminals**
- **Line controllers**
- **Network processors**
- **Front end communications**
- **Remote data concentrators**
- **Communication test equipment**
- **Computer to computer links**

ORDERING CODE

PACKAGE	V_{CC} = 5V ±5%, T_A = 0°C to 70°C	
	1.0MHz Clock Max	2.0MHz Clock Max
Ceramic DIP	SC2652C1I40	SC2652C2I40
Plastic DIP	SC2652C1N40	SC2652C2N40

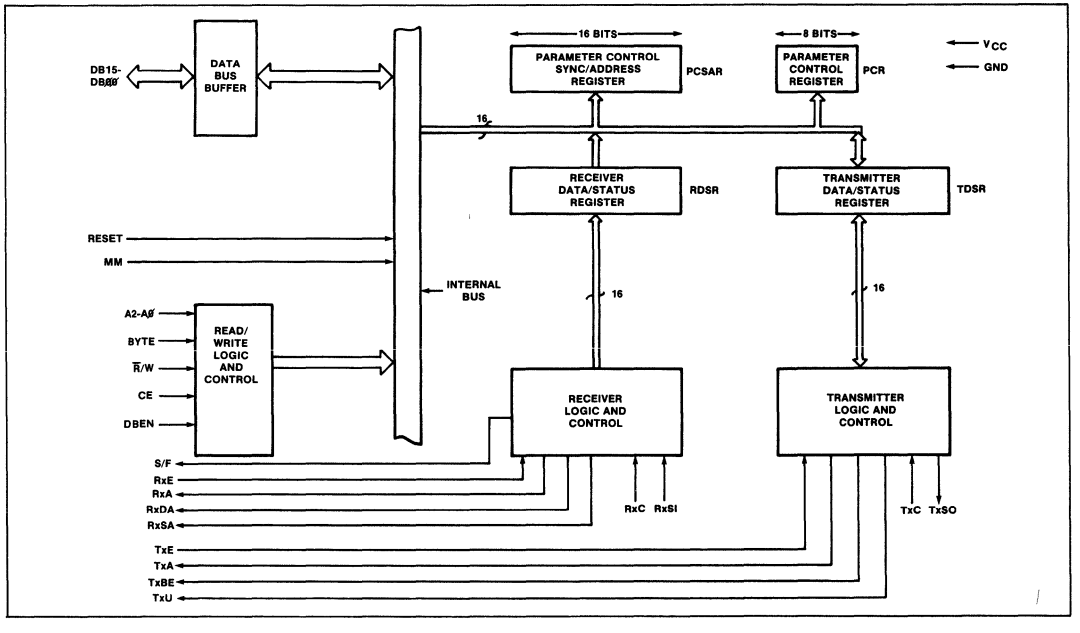
PIN CONFIGURATION



TOP VIEW

NOTE
00 is least significant bit, highest number (that is, DB15, A2) is most significant bit

BLOCK DIAGRAM



PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB15-DB00	17-10 24-31	I/O	**Data Bus:** DB07-DB00 contain bidirectional data while DB15-DB08 contain control and status information to or from the processor. Corresponding bits of the high and low order bytes can be WIRE OR'ed onto an 8-bit bus. The data bus is floating if either CE or DBEN are low.
A2-A0	19-21	I	**Address Bus:** A2-A0 select internal registers. The four 16-bit registers can be addressed on a word or byte basis. See Register Address section.
BYTE	22	I	**Byte:** Single byte (8 bit) data bus transfers are specified when this input is high. A low level specifies 16 bit data bus transfers.
CE	1	I	**Chip Enable:** A high input permits a data bus operation when DBEN is activated.
$\overline{R}$/W	18	I	**Read/Write:** $\overline{R}$/W controls the direction of data bus transfer. When high, the data is to be loaded into the addressed register A low input causes the contents of the addressed register to be presented on the data bus.
DBEN	23	I	**Data Bus Enable:** After A2-A0, CE, BYTE and $\overline{R}$/W are set up, DBEN may be strobed. During a read, the 3-state data bus (DB) is enabled with information for the processor. During a write, the stable data is loaded into the addressed register and TxBE will be reset if TDSR was addressed
RESET	33	I	**Reset:** A high level initializes all internal registers (to zero) and timing.
MM	40	I	**Maintenance Mode:** MM internally gates TxSO back to RxSI and $\overline{TxC}$ to RxC for off line diagnostic purposes. The RxC and RxSI inputs are disabled and TxSO is high when MM is asserted.
RxE	8	I	**Receiver Enable:** A high level input permits the processing of RxSI data. A low level disables the receiver logic and initializes all receiver registers and timing
RxA	5	O	**Receiver Active:** RxA is asserted when the first data character of a message is ready for the processor In the BOP mode this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if strip-SYNC ($PCSAR_{13}$) is set, the first non-SYNC character is the first data character; if strip-SYNC is zero, the character following the second SYNC is the first data character. In the BOP mode, the closing FLAG resets RxA In the BCP mode, RxA is reset by a low level at RxE.
RxDA*	6	O	**Receiver Data Available:** RxDA is asserted when an assembled character is in $RDSR_L$ and is ready to be presented to the processor. This output is reset when $RDSR_L$ is read.
RxC	2	I	**Receiver Clock:** RxC(1X) provides timing for the receiver logic. The positive going edge shifts serial data into the RxSR from RxSI.
S/F	4	O	**SYNC/FLAG:** S/F is asserted for one RxC clock time when a SYNC or FLAG character is detected
RxSA*	7	O	**Receiver Status Available:** RxSA is asserted when there is a zero to one transition of any bit in $RDSR_H$ except for RSOM. It is cleared when $RDSR_H$ is read.
RxSI	3	I	**Receiver Serial Input:** RxSI is the received serial data. Mark = '1', space = '0'
TxE	37	I	**Transmitter Enable:** A high level input enables the transmitter data path between $TDSR_L$ and TxSO At the end of a message, a low level input causes TxSO = 1 (mark) and TxA = 0 after the closing FLAG (BOP) or last character (BCP) is output on TxSO.
TxA	34	O	**Transmitter Active:** TxA is asserted after TSOM ($TDSR_8$) is set and TxE is raised. This output will reset when TxE is low and the closing FLAG (BOP) or last character (BCP) has been output on TxSO.
TxBE*	35	O	**Transmitter Buffer Empty:** TxBE is asserted when the TDSR is ready to be loaded with new control information or data. The processor should respond by loading the TDSR which resets TxBE.
TxU*	36	O	**Transmitter Underrun:** TxU is asserted during a transmit sequence when the service of TxBE has been delayed for one character time. This indicates the processor is not keeping up with the transmitter Line fill depends on $PCSAR_{11}$. TxU is reset by RESET or setting of TSOM ($TDSR_8$), synchronized by the falling edge of TxC.
TxC	39	I	**Transmitter Clock:** TxC (1X) provides timing for the transmitter logic. The positive going edge shifts data out of the TxSR to TxSO.
TxSO	38	O	**Transmitter Serial Output.** TxSO is the transmitted serial data. Mark = '1', space = '0'.
V_{CC}	32	I	**+5V:** Power supply.
GND	9	I	**Ground:** 0V reference ground.

*Indicates possible interrupt signal

REGISTERS		NO. OF BITS	DESCRIPTION*
Addressable			
PCSAR	Parameter Control Sync/Address Register	16	$PCSAR_H$ and PCR contain parameters common to the receiver and transmitter. $PCSAR_L$ contains a programmable SYNC character (BCP) or secondary station address (BOP)
PCR	Parameter Control Register	8	
RDSR	Receive Data/Status Register	16	$RDSR_H$ contains receiver status information. $RDSR_L$ = RxDB contains the received assembled character.
TDSR	Transmit Data/Status Register	16	$TDSR_H$ contains transmitter command and status information. TDSRL = TxDB contains the character to be transmitted.
Internal			
CCSR	Control Character Shift Register	8	These registers are used for character assembly (CCSR, HSR, RxSR), disassembly (TxSR), and CRC accumulation/generation (RxCRC, TxCRC).
HSR	Holding Shift Register	16	
RxSR	Receiver Shift Register	8	
TxSR	Transmitter Shift Register	8	
RxCRC	Receiver CRC Accumulation Register	16	
TxCRC	Transmitter CRC Generation Register	16	

NOTE

*H = High byte - bits 15-8
L = Low byte - bits 7-0

Table 1 GLOSSARY

CHARACTER	DESCRIPTION
FCS	Frame Check Sequence is transmitted/received as 16 bits following the last data character of a BOP message. The divisor is usually CRC-CCITT ($X^{16}+X^{12}+X^5+1$) with dividend preset to 1's but can be otherwise determined by ECM. The inverted remainder is transmitted as the FCS.
BCC	Block Check Character is transmitted/received as two successive characters following the last data character of a BCP message. The polynomial is CRC-16 ($X^{16}+X^{15}+X^2+1$) or CRC-CCITT with dividend preset to 0's (as specified by ECM). The true remainder is transmitted as the BCC.

Table 2 ERROR CONTROL

FUNCTIONAL DESCRIPTION

The MPCC can be functionally partitioned into receiver logic, transmitter logic, registers that can be read or loaded by the processor, and data bus control circuitry. The register bit formats are shown in figure 1 while the receiver and transmitter data paths are depicted in figures 2 and 3.

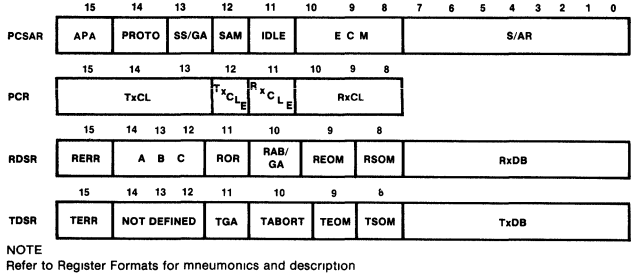
OPERATION	BIT PATTERN	FUNCTION
BOP		
FLAG	01111110	Frame message
ABORT	11111111 generation 01111111 detection	Terminate communication
GA	01111111	Terminate loop mode repeater function
Address	($PCSAR_L$)[1]	Secondary station address
BCP		
SYNC	($PCSAR_L$) or (TxDB)[2] generation	Character synchronization

NOTES

1 ( ) refers to contents of
2 For IDLE = 0 or 1 respectively

Table 3 SPECIAL CHARACTERS

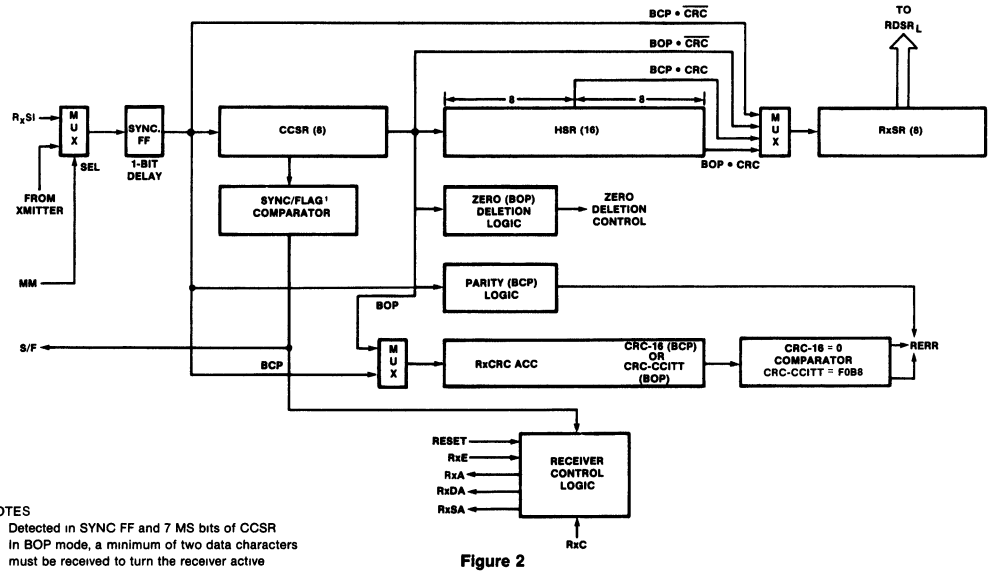
SHORT FORM REGISTER BIT FORMATS



NOTE
Refer to Register Formats for mneumonics and description

Figure 1

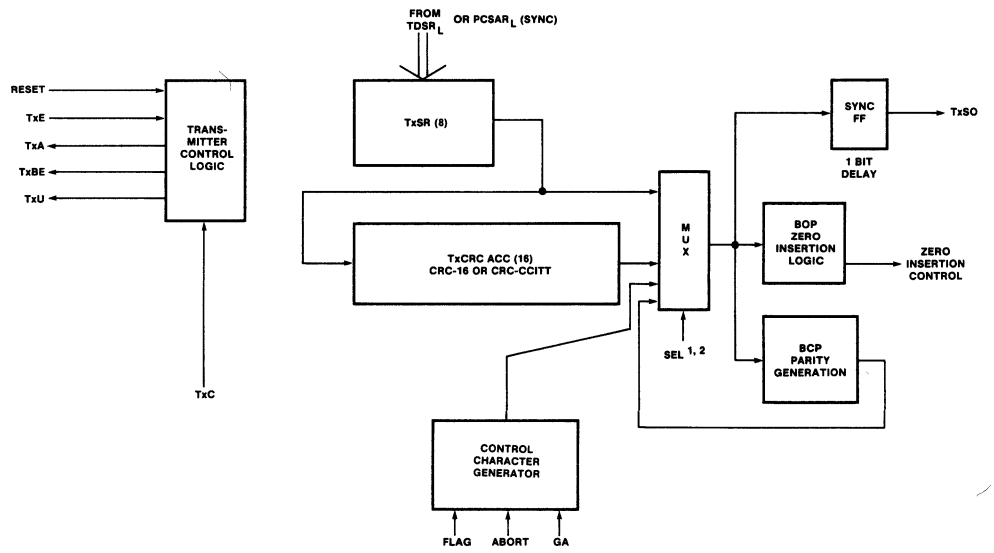
MPCC RECEIVER DATA PATH



NOTES
1 Detected in SYNC FF and 7 MS bits of CCSR
2. In BOP mode, a minimum of two data characters must be received to turn the receiver active

Figure 2

MPCC TRANSMITTER DATA PATH



NOTES
1 TxCRC selected if TEOM = 1 and the last data character has been shifted out of TxSR
2 In BCP, parity selected will be generated after each character is shifted out of TxSR

Figure 3

RECEIVER OPERATION

General

After initializing the parameter control registers (PCSAR and PCR), the RxE input must be set high to enable the receiver data path. The serial data on the RxSI is synchronized and shifted into an 8-bit Control Character Shift Register (CCSR) on the rising edge of RxC. A comparison between CCSR contents and the FLAG (BOP) or SYNC (BCP) character is made until a match is found. At that time, the S/F output is asserted for one RxC time and the 16-bit Holding Shift Register (HSR) is enabled. The receiver then operates as described below.

BOP Operation

A flow chart of receiver operation in BOP mode appears in figure 4. Zero deletion (after five ones are received) is implemented on the received serial data so that a data character will not be interpreted as a FLAG, ABORT, or GA Bits following the FLAG are shifted through the CCSR, HSR, and into the Receiver Shift Register (RxSR). A character will be assembled in the RxSR and transferred to the $RDSR_L$ for presentation to the processor At that time the RxDA output will be asserted and the processor must take the character no later than one RxC time after the next character is assembled in the RxSR. If not, an overrun ($RDSR_{11} = 1$) will occur and succeeding characters will be lost.

The first character following the FLAG is the secondary station address. If the MPCC is a secondary station ($PCSAR_{12} = 1$), the contents of RxSR are compared with the address stored in $PCSAR_L$. A match indicates the forthcoming message is intended for the station; the RxA output is asserted, the character is loaded into $RDSR_L$, RxDA is asserted and the Receive Start of Message bit (RSOM) is set. No match indicates that another station is being addressed and the receiver searches for the next FLAG.

If the MPCC is a primary station ($PCSAR_{12} = 0$), no secondary address check is made, RxA is asserted and RSOM is set once the first non-FLAG character has been loaded into $RDSR_L$ and RxDA has been asserted. Extended address field can be supported by software if $PCSAR_{12} = 0$

When the 8 bits following the address character have been loaded into $RDSR_L$ and RxDA has been asserted, RSOM will be cleared. The processor should read this 8-bit character and interpret it as the Control field.

Received serial data that follows is read and interpreted as the Information field by the processor. It will be assembled into character lengths as specified by PCR_{8-10}. As

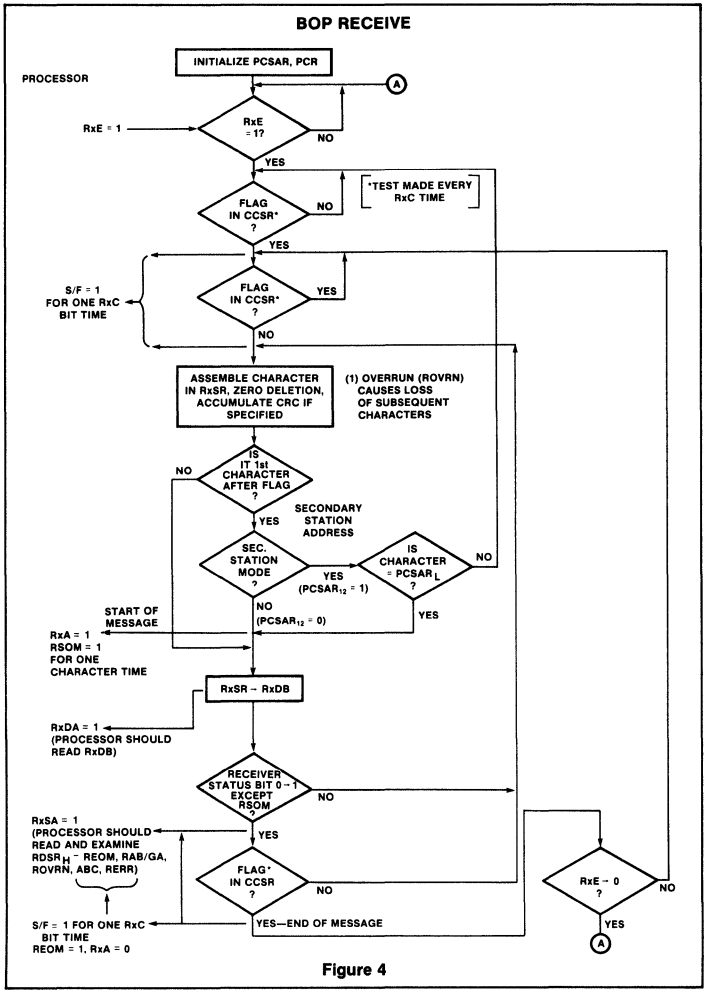


Figure 4

before, RxDA is asserted each time a character has been transferred into $RDSR_L$ and is cleared when $RDSR_L$ is read by the processor $RDSR_H$ should only be read when RxSA is asserted. This occurs on a zero to one transition of any bit in $RDSR_H$ except for RSOM. RxSA and all bits in $RDSR_H$ except RSOM are cleared when $RDSR_H$ is read The processor should check $RDSR_{9-15}$ each time RxSA is asserted. If $RDSR_9$ is set, then $RDSR_{12-15}$ should be examined

Receiver character length may be changed dynamically in response to RxDA: read the character in RxDB and write the new character length into RxCL. The character length will be changed on the next receiver character boundary. A received residual (short) character will be transferred into RxDB after the previous character in RxDB has been read, i.e. there will not be an overrun. In general the last two characters are protected from overrun.

The CRC-CCITT, if specified by $PCSAR_{8-10}$, is accumulated in RxCRC on each character following the FLAG. When the closing FLAG is detected in the CCSR, the received CRC is in the 16-bit HSR. At that time, the Receive End of Message bit (REOM) will be set; RxSA and RxDA will be asserted. The

processor should read the last data character in $RDSR_L$ and the receiver status in $RDSR_{9-15}$. If $RDSR_{15} = 1$, there has been a transmission error; the accumulated CRC-CCITT is incorrect. If $RDSR_{12-14} \neq 0$, the last data character is not of prescribed length. Neither the received CRC nor closing FLAG are presented to the processor. The processor may drop RxE or leave it active at the end of the received message.

BCP Operation

The operation of the receiver in BCP mode is shown in figure 5. The receiver initially searches for two successive SYNC characters, of length specified by PCR_{8-10}, that match the contents of PCSARL. The next non-SYNC character or next SYNC character, if stripping is not specified ($PCSAR_{13}$ = 0), causes RxA to be asserted and enables the receiver data path. Once enabled, all characters are assembled in RxSR and loaded into $RDSR_L$. RxDA is active when a character is available in $RDSR_L$ RxSA is active on a 0 to 1 transition of any bit in $RDSR_H$. The signals are cleared when $RDSR_L$ or $RDSR_H$ are read respectively

If CRC-16 error control is specified by $PCSAR_{8-10}$, the processor must determine the last character received prior to the CRC field. When that character is loaded into $RDSR_L$ and RxDA is asserted, the received CRC will be in CCSR and HSR_L. To check for a transmission error, the processor must read the receiver status ($RDSR_H$) and examine $RDSR_{15}$. This bit will be set for one character time if an error free message has been received. If $RDSR_{15} = 0$, the CRC-16 is in error. The state of RDSR15 in BCP CRC mode does not set RxSA. Note that this bit should be examined only at the end of a message. The accumulated CRC will include all characters starting with the first non-SYNC character if $PCSAR_{13} = 1$, or the character after the opening two SYNC's if $PCSAR_{13}$ = 0. This necessitates external CRC generation/checking when supporting IBM's BISYNC. This can be accomplished using the Signetics 2653 Polynomial Generator/Checker. See Typical Applications.

If VRC had been selected for error control, parity (odd or even) is regenerated on each character and checked when the parity bit is received. A discrepancy causes $RDSR_{15}$ to be set and RxSA to be asserted. This must be sensed by the processor. The received parity bit is stripped before the character is presented to the processor.

When the processor has read the last character of the message, it should drop RxE which disables the receiver logic and initializes all receiver registers and timing.

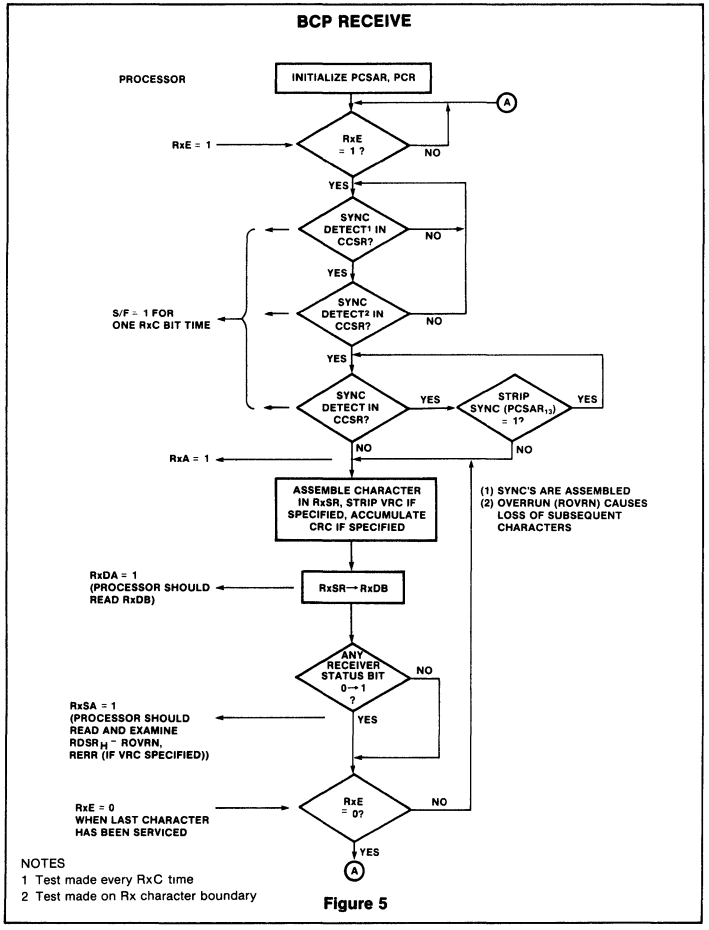


Figure 5

TRANSMITTER OPERATION

General

After the parameter control registers (PCSAR and PCR) have been initialized, TxSO is held at mark until TSOM ($TDSR_8$) is set and TxE is raised. Then, transmitter operation depends on protocol mode.

BOP Operation

Transmitter operation for BOP is shown in figure 6. A FLAG is sent after the processor sets the Transmit Start of Message bit (TSOM) and raises TxE. The FLAG is used to synchronize the message that follows. TxA will also be asserted. When TxBE is asserted by the MPCC, the processor should load $TDSR_L$ with the first character of the message. TSOM should be cleared at the same time $TDSR_L$ is loaded (16-bit data bus) or immediately thereafter (8-bit data bus). FLAGs are sent as long as TSOM = 1 For counting the number of FLAGs, the processor should reassert TSOM in response to the assertion of TxBE.

All succeeding characters are loaded into $TDSR_L$ by the processor when TxBE = 1. Each character is serialized in TxSR and transmitted on TxSO. Internal zero insertion logic stuffs a "0" into the serial bit stream after five successive "1s" are sent. This insures a data character will not match a FLAG, ABORT, or GA reserved control character. As each character is transmitted, the Frame Check Sequence (FCS) is gener-

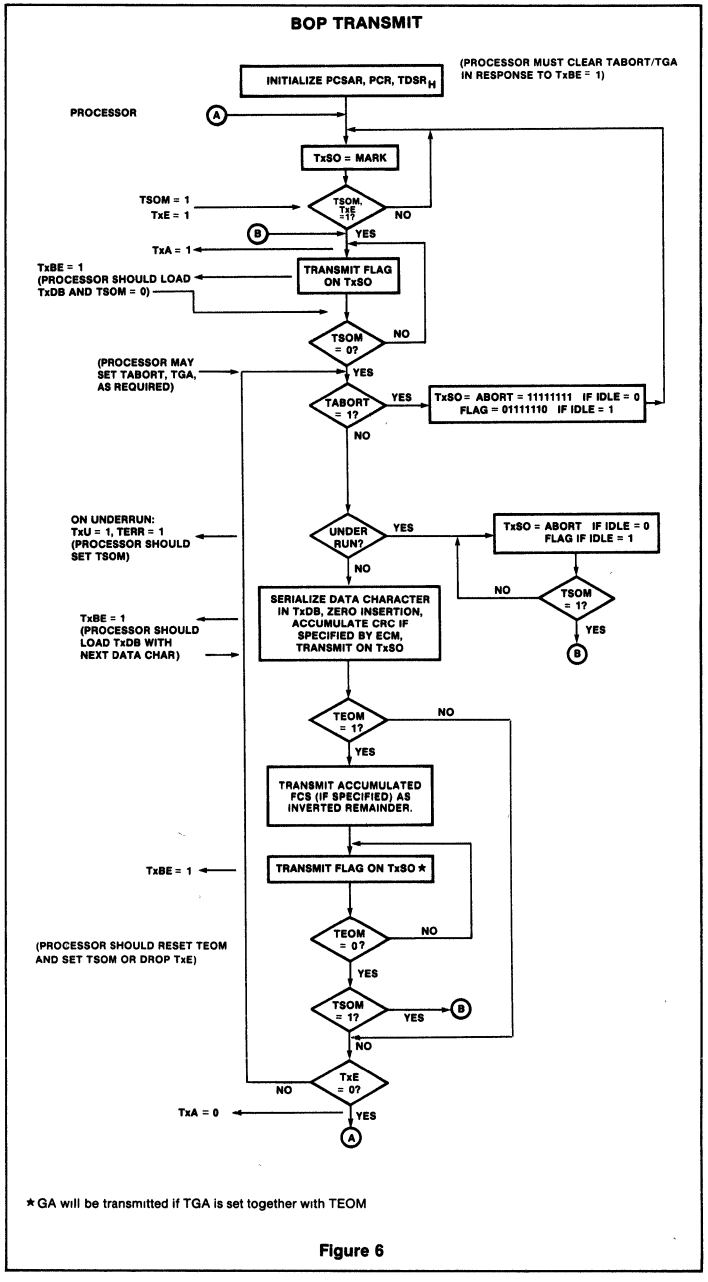


Figure 6

ated as specified by Error Control Mode ($PCSAR_{8-10}$). The FCS should be the CRC-CCITT polynomial ($X^{16}+X^{12}+X^5+1$) preset to 1s. If an underrun occurs (processor is not keeping up with the transmitter), TxU and TERR ($TDSR_{15}$) will be asserted with ABORT or FLAG used as the TxSO line fill depending on the state of IDLE ($PCSAR_{11}$). The processor must set TSOM to reset the underrun condition. To retransmit the message, the processor should proceed with the normal start of message sequence.

A residual character of 1 to 7 bits may be transmitted at the end of the Information field. In response to TxBE, write the residual character length into TxCL and load TxDB with the residual character. Dynamic alteration of character length should be done in exactly the same sequence. The character length will be changed on the next transmit character boundary.

After the last data character has been loaded into $TDSR_L$ and sent to TxSR (TxBE = 1), the processor should set TEOM ($TDSR_9$). The MPCC will finish transmitting the last character followed by the FCS and the closing FLAG. The processor should clear TEOM and drop TxE when the next TxBE is asserted. This corresponds to the start of closing FLAG transmission. When TxE has been dropped, TxA will be low $1\frac{1}{2}$ bit times after the last bit of the closing FLAG has been transmitted. TxSO will be marked after the closing FLAG has been transmitted.

If TxE and TEOM are high, the transmitter continues to send FLAGs. The processor may initiate the next message by resetting TEOM and setting TSOM, or by loading $TDSR_L$ with a data character and then simply resetting TEOM (without setting TSOM).

BCP Operation

Transmitter operation for BCP mode is shown in figure 7. TxA will be asserted after TSOM = 1 and TxE is raised. At that time SYNC characters are sent from $PCSAR_L$ or $TDSR_L$ (IDLE = 0 or 1) as long as TSOM = 1. TxBE is asserted at the start of transmission of the first SYNC character. For counting the number of SYNC's, the processor should reassert TSOM in response to the assertion of TxBE. When TSOM = 0 transmission is from $TDSR_L$, which must be loaded with characters from the processor each time TxBE is asserted. If this loading is delayed for more than one character time, an underrun results: TxU and TERR are asserted and the TxSO line fill depend on IDLE ($PCSAR_{11}$). The processor must set TSOM

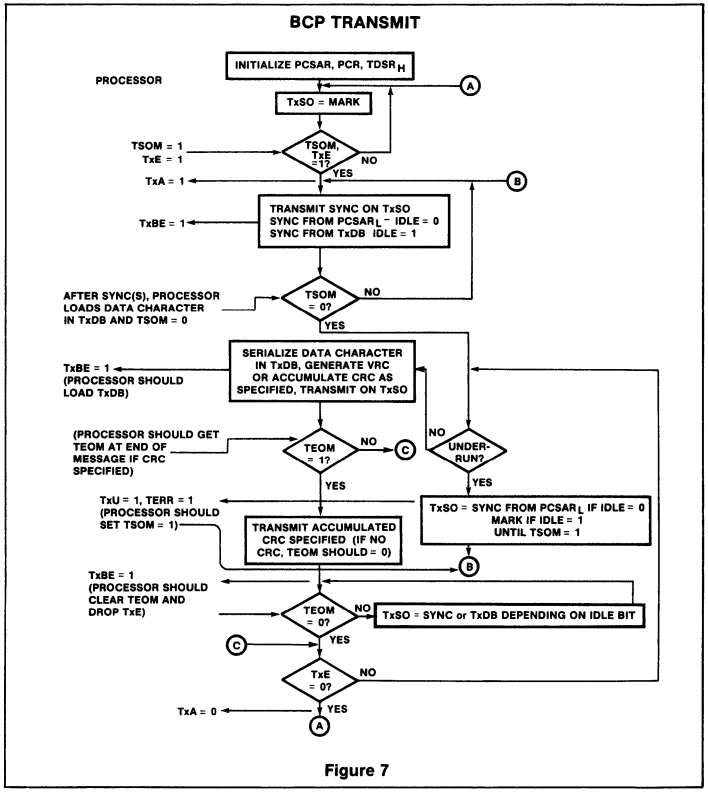


Figure 7

and retransmit the message to recover This is not compatible with IBM's BISYNC, so that the user must not underrun when supporting that protocol.

CRC-16, if specified by $PCSAR_{8-10}$, is generated on each character transmitted from $TDSR_L$ when TSOM = 0. The processor must set TEOM = 1 after the last data character has been sent to TxSR (TxBE = 1). The MPCC will finish transmitting the last data character and the CRC-16 field before sending SYNC characters which are transmitted as long as TEOM = 1. If SYNCs are not desired after CRC-16 transmission, the processor should clear TEOM and lower TxE when the TxBE corresponding to the start of CRC-16 transmission is asserted. When TEOM = 0, the line is marked and a new message may be iniated by setting TSOM and raising TxE.

If VRC is specified, it is generated on each data character and the data character length must not exceed 7 bits For software LRC or CRC, TEOM should be set only if SYNC's are required at the end of the message block.

Special Case

The capability to transmit 16 spaces is provided for line turnaround in half duplex mode or for a control recovery situation. This is achieved by setting TSOM and TEOM, clearing TEOM when TxBE = 1, and proceeding as required.

PROGRAMMING

Prior to initiating data transmission or reception, PCSAR and PCR must be loaded with control information from the processor. The contents of these registers (see Register Format section) will configure the MPCC for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is disabled.

The default value for all registers is zero. This corresponds to BOP, primary station mode, 8-bit character length, FCS = CRC-CCITT preset to 1s.

For BOP mode the character length register (PCR) may be set to the desired values during system initialization. The address and control fields will automatically be 8-bits. If a residual character is to be transmitted, TxCL should be changed to the residual character length prior to transmission of that character

DATA BUS CONTROL

The processor must set up the MPCC register address (A2-A0), chip enable (CE), byte select (BYTE), and read/write ($\overline{R}$/W) inputs before each data bus transfer operation.

During a read operation ($\overline{R}$/W = 0), the leading edge of DBEN will initiate an MPCC read cycle. The addressed register will place its contents on the data bus. If BYTE = 1, the 8-bit byte is placed on DB15-08 or DB07-00 depending on the H/L status of the register addressed. Unused bits in $RDSR_L$ are zero. If BYTE = 0, all 16 bits (DB15-00) contain MPCC information. The trailing edge of DBEN will reset RxDA and/or RxSA if $RDSR_L$ or $RDSR_H$ is addressed respectively.

DBEN acts as the enable and strobe so that the MPCC will not begin its internal read cycle until DBEN is asserted.

During a write operation ($\overline{R}$/W = 1), data must be stable on DB_{15-08} and/or DB_{07-00} prior to the leading edge of DBEN. The stable data is strobed into the addressed register by DBEN. TxBE will be cleared if the addressed register was $TDSR_H$ or $TDSR_L$.

	A2	A1	A0	REGISTER
BYTE = 0	16-BIT DATA BUS = DB_{15} - DB_{00}			
	0	0	X	RDSR
	0	1	X	TDSR
	1	0	X	PCSAR
	1	1	X	PCR*
BYTE = 1	8-BIT DATA BUS = DB_{7-0} or DB_{15-8}**			
	0	0	0	$RDSR_L$
	0	0	1	$RDSR_H$
	0	1	0	$TDSR_L$
	0	1	1	$TDSR_H$
	1	0	0	$PCSAR_L$
	1	0	1	$PCSAR_H$
	1	1	0	PCR_L*
	1	1	1	PCR_H

NOTES

* PCR lower byte does not exist It will be all "0"s when read

** Corresponding high and low order pins must be tied together

Table 4 MPCC REGISTER ADDRESSING

BIT	NAME	MODE	FUNCTION
00-07	Not Defined		
08-10	RxCL	BOP/BCP	Receiver Character Length is loaded by the processor when RxCLE = 0. The character length is valid after transmission of single byte address and control fields have been received.

10	9	8	Char. length (bits)
0	0	0	8
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

11	RxCLE	BOP/BCP	Receiver Character Length Enable should be zero when the processor loads RxCL. The remaining bits of PCR are not affected during loading. Always 0 when read.
12	TxCLE	BOP/BCP	Transmitter Character Length Enable should be zero when the processor loads TxCL. The remaining bits of PCR are not affected during loading. Always 0 when read.
13-15	TxCL	BOP/BCP	Transmitter Character Length is loaded by the processor when TxCLE = 0. Character bit length specification format is identical to RxCL It is valid after transmission of single byte address and control fields

Table 5 PARAMETER CONTROL REGISTER (PCR)-(R/W)

BIT	NAME	MODE	FUNCTION
00-07	S/AR	BOP	SYNC/ADDRESS Register. Contains the secondary station address if the MPCC is a secondary station. The contents of this register is compared with the first received non-FLAG character to determine if the message is meant for this station.
		BCP	SYNC character is loaded into this register by the processor It is used for receive and transmit bit synchronization with bit length specified by RxCL and TxCL
08-10	ECM	BOP/BCP	**Error Control Mode** / **10** / **9** / **8** / **Suggested Mode** / **Char. length** CRC-CCITT preset to 1's 0 0 0 BOP 1-8 CRC-CCITT preset to 0's 0 0 1 BCP 8 Not used 0 1 0 --- CRC-16 preset to 0's 0 1 1 BCP 8 VRC odd 1 0 0 BCP 5-7 VRC even 1 0 1 BCP 5-7 Not used 1 1 0 --- No error control 1 1 1 BCP/BOP 5-8 ECM should be loaded by the processor during initialization or when both data paths are idle.
11	IDLE		Determines line fill character to be used if transmitter underrun occurs (TxU asserted and TERR set) and transmission of special characters for BOP/BCP.
		BOP	IDLE = 0, transmit ABORT characters during underrun and when TABORT = 1 IDLE = 1, transmit FLAG characters during underrun and when TABORT = 1
		BCP	IDLE = 0 transmit initial SYNC characters and underrun line fill characters from the S/AR IDLE = 1 transmit initial SYNC characters from TxDB and marks TxSO during underrun.
12	SAM	BOP	Secondary Address Mode = 1 if the MPCC is a secondary station This facilitates automatic recognition of the received secondary station address When transmitting, the processor must load the secondary address into TxDB SAM = 0 inhibits the received secondary address comparison which serves to activate the receiver after the first non-FLAG character has been received
13	SS/GA		Strip SYNC/Go Ahead Operation depends on mode.
		BOP	SS/GA = 1 is used for loop mode only and enables GA detection. When a GA is detected as a closing character, REOM and RAB/GA will be set and the processor should terminate the repeater function SS/GA = 0 is the normal mode which enables ABORT detection. It causes the receiver to terminate the frame upon detection of an ABORT or FLAG
		BCP	SS/GA = 1, causes the receiver to strip SYNC's immediately following the first two SYNC's detected SYNC's in the middle of a message will not be stripped SS/GA = 0, presents any SYNC's after the initial two SYNC's to the processor
14	PROTO		Determines MPCC Protocol mode
		BOP	PROTO = 0
		BCP	PROTO = 1
15	APA	BOP	All Parties Address. If this bit is set, the receiver data path is enabled by an address field of '11111111' as well as the normal secondary station address

Table 6 PARAMETER CONTROL SYNC/ADDRESS REGISTER (PCSAR)-(R/W)

BIT	NAME	MODE	FUNCTION
00-07	TxDB	BOP/BCP	Transmit Data Buffer. Contains processor loaded characters to be serialized in TxSR and transmitted on TxSO.
08	TSOM		Transmitter Start of Message. Set by the processor to initiate message transmission provided TxE = 1.
		BOP	TSOM = 1 generates FLAGs. When TSOM = 0 transmission is from TxDB and FCS generation (if specified) begins. FCS, as specified by $PCSAR_{8\text{-}10}$, should be CRC-CCITT preset to 1's.
		BCP	TSOM = 1 generates SYNCs from $PCSAR_L$ or transmits from TxDB for IDLE = 0 or 1 respectively When TSOM = 0 transmission is from TxDB and CRC generation (if specified) begins

Table 7 TRANSMIT DATA/STATUS REGISTER (TDSR) (R/W except TDSR 15)

BIT	NAME	MODE	FUNCTION
09	TEOM		Transmit End of Message. Used to terminate a transmitted message.
		BOP	TEOM = 1 causes the FCS and the closing FLAG to be transmitted following the transmission of the data character in TxSR. FLAGs are transmitted until TEOM = 0. ABORT or GA are transmitted if TABORT or TGA are set when TEOM = 1.
		BCP	TEOM = 1 causes CRC-16 to be transmitted (if selected) followed by SYNCs from $PCSAR_L$ or TxDB (IDLE = 0 or 1). Clearing TEOM prior to the end of CRC-16 transmission (when TxBE = 1) causes TxSO to be marked following the CRC-16. TxE must be dropped before a new message can be initiated. If CRC is not selected, TEOM should not be set.
10	TABORT	BOP	Transmitter Abort = 1 will cause ABORT or FLAG to be sent (IDLE = 0 or 1) after the current character is transmitted. (ABORT = 11111111)
11	TGA	BOP	Transmit Go Ahead (GA) instead of FLAG when TEOM = 1. This facilitates repeater termination in loop mode. (GA = 01111111)
12-14	Not Defined		
15	TERR	Read only	Transmitter Error = 1 indicates the TxDB has not been loaded in time (one character time $-1/2$ TxC period after TxBE is asserted) to maintain continuous transmission. TxU will be asserted to inform the processor of this condition. TERR is cleared by setting TSOM. See timing diagram.
		BOP	ABORT's or FLAG's are sent as fill characters (IDLE = 0 or 1)
		BCP	SYNC's or MARK's are sent as fill characters (IDLE = 0 or 1). For IDLE = 1 the last character before underrun is not valid.

Table 7 TRANSMIT DATA/STATUS REGISTER (TDSR) (R/W except TDSR 15) (Cont'd)

BIT	NAME	MODE	FUNCTION
00-07	RxDB	BOP/BCP	Receiver Data Buffer. Contains assembled characters from the RxSR If VRC is specified, the parity bit is stripped.
08	RSOM	BOP	Receiver Start of Message = 1 when a FLAG followed by a non-FLAG has been received and the latter character matches the secondary station address if SAM = 1. RxA will be asserted when RSOM = 1. RSOM resets itself after one character time and has no effect on RxSA.
09	REOM	BOP	Receiver End of Message = 1 when the closing FLAG is detected and the last data character is loaded into RxDB or when an ABORT/GA character is received. REOM is cleared on reading $RDSR_H$, reset operation, or dropping of RxE.
10	RAB/GA	BOP	Received ABORT or GA character = 1 when the receiver senses an ABORT character if SS/GA = 0 or a GA character if SS/GA = 1 RAB/GA is cleared on reading $RDSR_H$, reset operation, or dropping of RxE. A received ABORT does not set RxDA.
11	ROR	BOP/BCP	Receiver Overrun = 1 indicates the processor has not read last character in the RxDB within one character time $+1/2$ RxC period after RxDA is asserted. Subsequent characters will be lost. ROR is cleared on reading $RDSR_H$, reset operation, or dropping of RxE.
12-14	ABC	BOP	Assembled Bit Count. Specifies the number of bits in the last received data character of a message and should be examined by the processor when REOM = 1 (RxDA and RxSA asserted). ABC = 0 indicates the message was terminated (by a FLAG or GA) on a character boundary as specified by PCR_{8-10}. Otherwise, ABC = number of bits in the last data character. ABC is cleared when $RDSR_H$ is read, reset operation, or dropping RxE. The residual character is right justified in $RDSR_L$.
15	RERR	BOP/BCP	Receiver Error indicator should be examined by the processor when REOM = 1 in BOP, or when the processor determines the last data character of the message in BCP with CRC or when RxSA is set in BCP with VRC. CRC-CCITT preset to 1's/0's as specified by $PCSAR_{8-10}$: RERR = 1 indicates FCS error (CRC ≠ F0B8/≠ 0) RERR = 0 indicates FCS received correctly (CRC = F0B /=0) CRC-16 preset to 0's on 8-bit data characters specified by $PSCAR_{8-10}$: RERR = 1 indicates CRC-16 received correctly (CRC = 0). RERR = 0 indicates CRC-16 error (CRC ≠ 0) VRC specified by $PCSAR_{8-10}$: RERR = 1 indicates VRC error RERR = 0 indicates VRC is correct

Table 8 RECEIVER DATA/STATUS REGISTER (RDSR)-(Read Only)

1

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C
	Input or output voltages with respect to GND[3]	-0.3 to +15	V
V_{CC}	With respect to GND	-0.3 to+7	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$[4,5]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low				0.8	
V_{IH}	High		2.0			
	Output voltage					V
V_{OL}	Low	$I_{OL} = 1.6mA$			0.4	
V_{OH}	High	$I_{OH} = -100\mu A$	2.4			
I_{CC}	Power supply current	$V_{CC} = 5.25V$, $T_A = 0°C$			150	mA
	Leakage current					μA
I_{IL}	Input	$V_{IN} = 0$ to 5.25V			10	
I_{OL}	Output	$V_{OUT} = 0$ to 5.25V			10	
	Capacitance					pF
C_{IN}	Input	$V_{IN} = 0V$, f = 1MHz			20	
C_{OUT}	Output	$V_{OUT} = 0V$, f = 1MHz			20	

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$[4, 5, 6]

PARAMETER		2652			2652-1			UNIT
		Min	Typ	Max	Min	Typ	Max	
	Setup and hold time							ns
t_{ACS}	Address/control setup	50			50			
t_{ACH}	Address/control hold	0			0			
t_{DS}	Data bus setup (write)	50			50			
t_{DH}	Data bus hold (write)	0			0			
t_{RXS}	Receiver serial data setup	150			150			
t_{RXH}	Receive serial data hold	150			150			
	Pulse width							ns
t_{RES}	RESET	250			250			
t_{DBEN}	DBEN	250		m[7]	200		m[7]	
	Delay time							ns
t_{DD}	Data bus (read)			200			170	
t_{TXD}	Transmit serial data			325			250	
t_{DBEND}	DBEN to DBEN delay	200			200			
t_{DF}	Data bus float time (read)			150			150	ns
f	Clock (RxC, TxC) frequency			1.0			2.0	MHz
t_{CLK1}	Clock high (MM = 0)	340			165			ns
t_{CLK1}	Clock high (MM = 1)	490			240			
t_{CLK0}	Clock low	490			240			

NOTES

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied

2 For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient (IQ ceramic package)

3 This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima

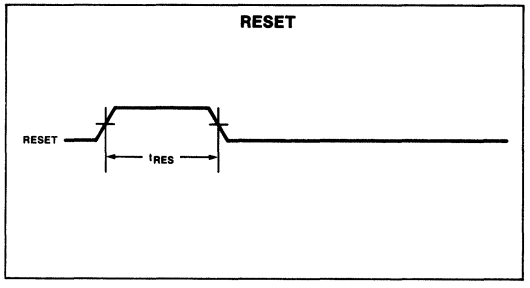
4 Parameters are valid over operating temperature range unless otherwise specified

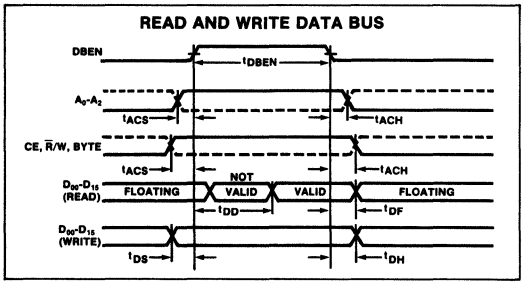
5 All voltage measurements are referenced to ground All time measurements are at 0 8V or 2.0V. Input voltage levels for testing are 0.4V and 2.4V.

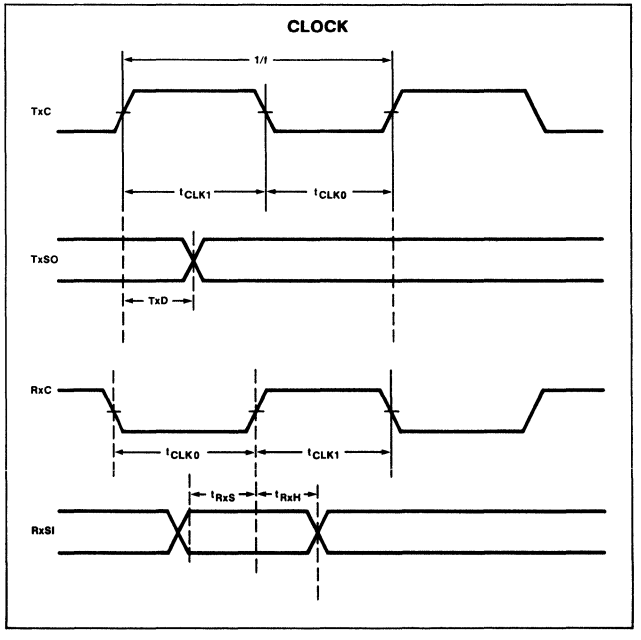
6 Output load C_L = 100pF.

7 m = TxC low and applies to writing to $TDSR_H$ only

TIMING DIAGRAMS

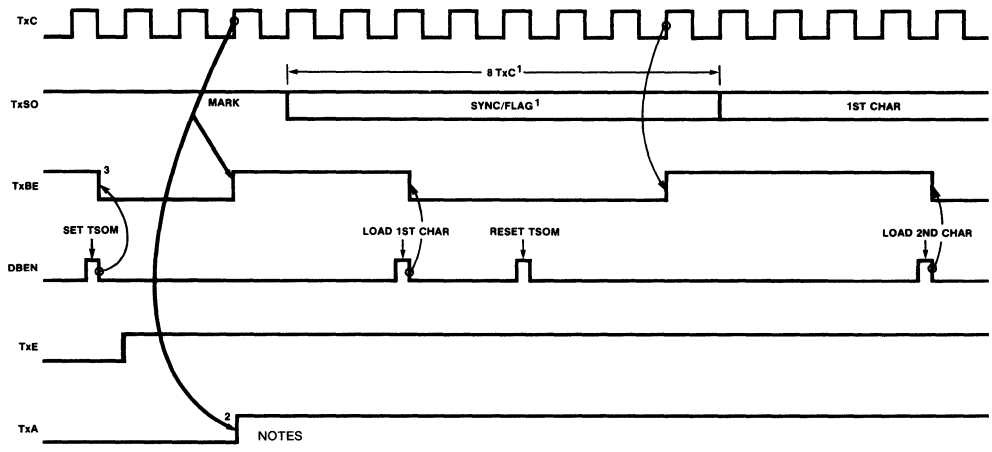






TIMING DIAGRAMS (Cont'd)

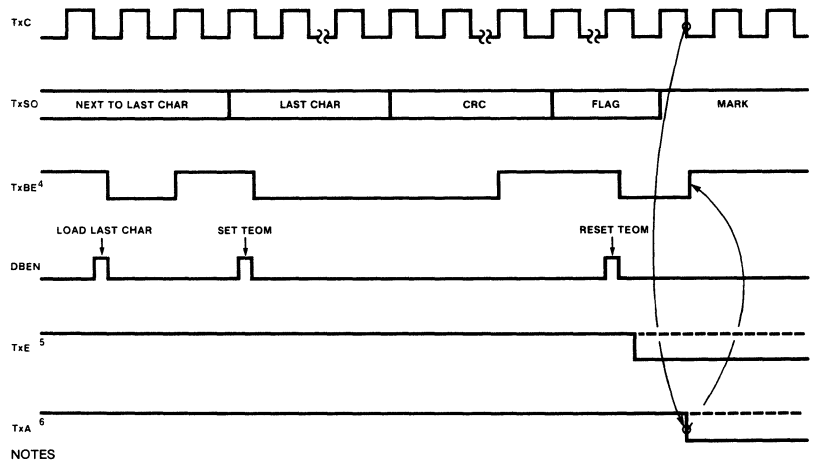
TRANSMIT—START OF MESSAGE



NOTES

1 SYNC may be 5 to 8 bits and will contain parity bit as specified
2 TxA goes high relative to TxC rising edge after TSOM has been set and TxE has been raised
3 TxBE goes low relative to DBEN falling edge on the first write transfer into TDSR. It is reasserted 1 TxC time before the first bit of the transmitted SYNC/FLAG TxBE then goes low relative to DBEN falling edge when writing into $TDSR_H$ and/or $TDSR_L$ It is reasserted on the rising edge of the TxC that corresponds to the transmission of the last bit of each character, except in BOP mode when the CRC is to be sent as the next character (see Transmit Timing—End of Message)

TRANSMIT—END OF BOP MESSAGE

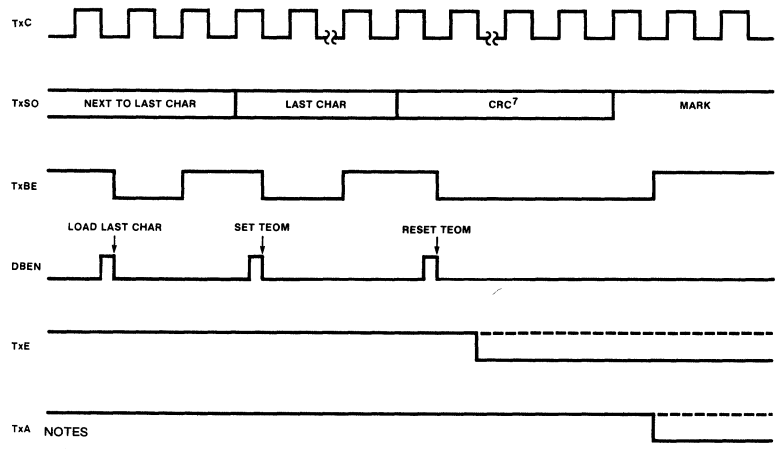


NOTES

4 TxBE goes low relative to the falling edge of DBEN corresponding to loading $TDSR_{H/L}$ It goes high one TxC before character transmission begins and also when TxA has been dropped
5 TxE can be dropped before resetting TEOM if TxBE (corresponding to the closing FLAG) is high Alternatively TxE can remain high and a new message initiated
6 TxA goes low after TxE has been dropped and 1 1/2 TxC's after the last bit of the closing FLAG has been transmitted.

TIMING DIAGRAMS (Cont'd)

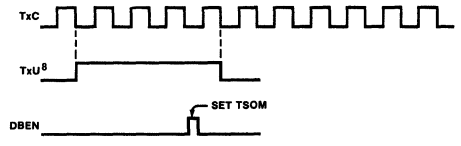
TRANSMIT TIMING—END OF BCP MESSAGE



NOTES

7 When 2652 generated CRC is not required, TEOM should only be set if SYNCs are to follow the message block In that case, TxE should be dropped in response to TxBE (which corresponds to the start of transmission of the last character) When CRC is required, TxE must be dropped before CRC transmission is complete Otherwise, the contents of TxDB will be shifted out on TxSO This facilitates transmission of contiguous messages

TRANSMIT UNDERRUN



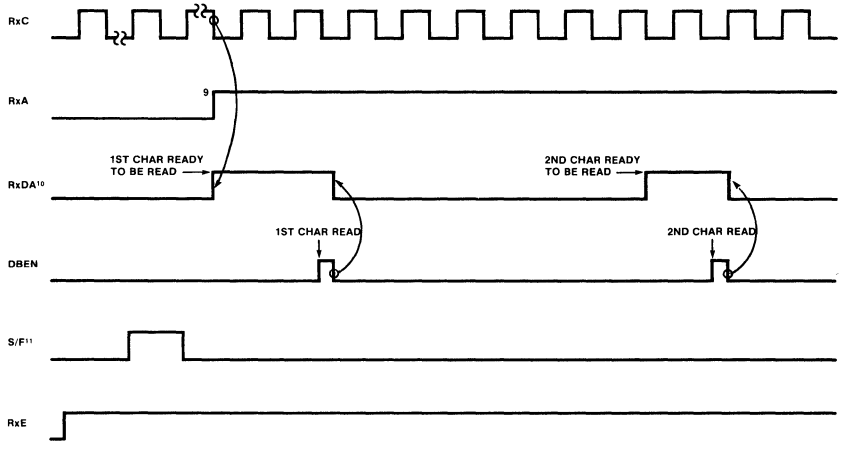
NOTES

8 TxU goes active relative to TxC falling edge if TxBE has not been serviced after n-1/2 TxC times (where n = transmit character length) TxU is reset on the TxC falling edge following assertion of the TSOM command

9 An underrun will occur at the next character boundary if TEOM is reset and the transmitter remains enabled, unless the TSOM command is asserted or a character is loaded into the TxDB

TIMING DIAGRAMS (Cont'd)

RECEIVE—START OF MESSAGE



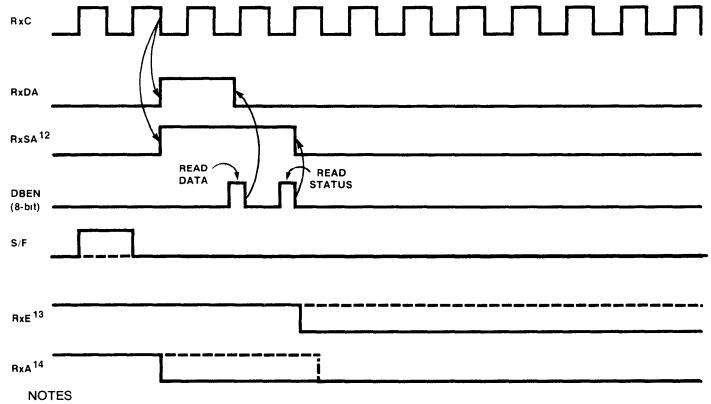
NOTES

9 RxA goes high relative to falling edge of RxC when RxE is high and
- a A data character following two SYNC's is in RxDB (BCP mode)
- b Character following FLAG is in RxDB (BOP primary station mode)
- c Character following FLAG is in RxDB and character matches the secondary station address or All Parties Address (BOP secondary station mode)

10 RxDA goes high on RxC falling edge when a character in RxDB is ready to be read It comes up before RxSA and goes low on the falling edge of DBEN when RxDB is read

11 S/F goes high relative to rising edge of RxC anytime a SYNC (BCP) or FLAG (BOP) is detected

RECEIVE END OF MESSAGE



NOTES

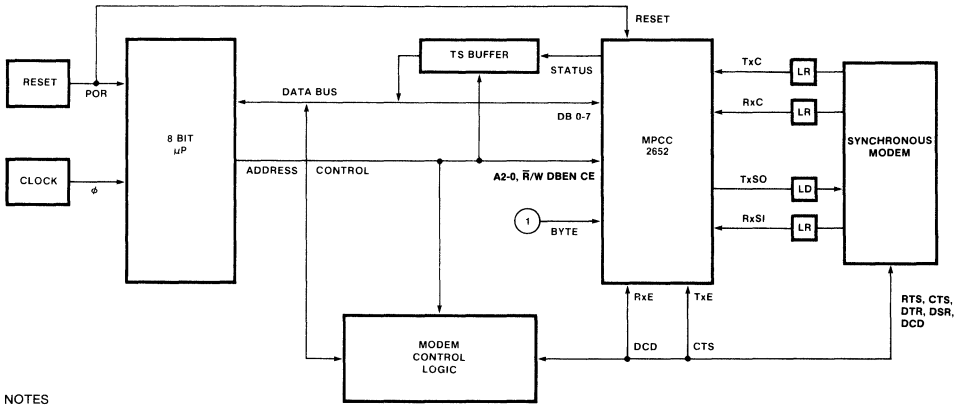
12 At the end of a BOP message, RxSA goes high when FLAG detection (S/F = 1) forces REOM to be set Processor should read the last data character ($RDSR_L$) and status ($RDSR_H$) which resets RxDA and RxSA respectively For BCP end of message, RxSA may not be set and S/F = 0 The processor should read the last data character and status

13 RxE must be dropped for BCP with non-contiguous messages It may be left on at the end of a BOP message (see BOP Receive Operation)

14 RxA is reset relative to the falling edge of RxC after the closing FLAG of a BOP message (REOM = 1 and RxSA active,) or when RxE is dropped

TYPICAL APPLICATIONS

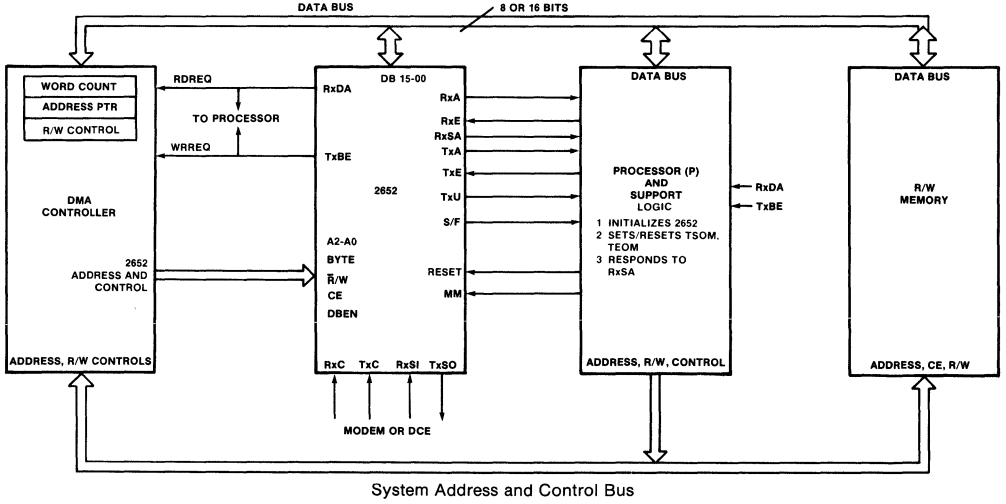
2652 MPCC MICROPROCESSOR INTERFACE



NOTES

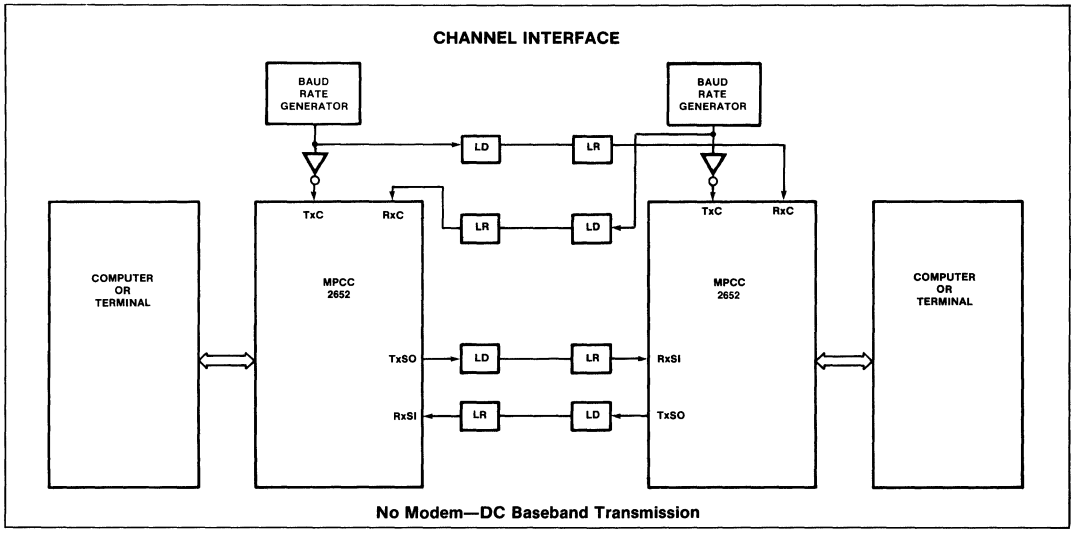
1 Possible μP interrupt requests are
RxDA, RxSA, TxBE, TxU
2 Other 2652 status signals and possible uses are
S/F line idle indicator, frame delimiter
RxA handshake on RxE, line turn around control
TxA handshake on TxE, line turn around control
3 Line Drivers/Receivers (LD/LR) convert EIA to TTL voltages and vice-versa
4 RTS should be dropped after the CRC (BCP) or FLAG (BOP) has been transmitted
This forces CTS low and TxE low
5 Corresponding high and low order bits of DB must be OR tied

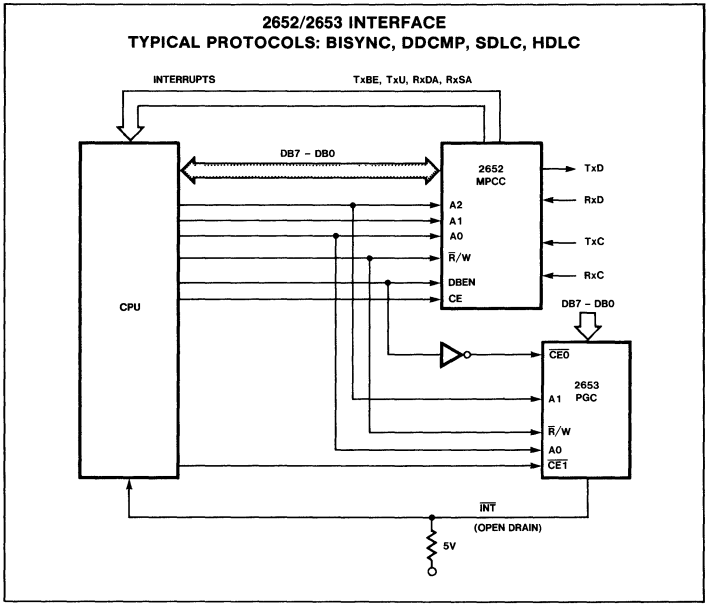
DMA/PROCESSOR INTERFACE



For non-DMA operation, TxBE and RxDA are sent to the processor which then loads or reads data characters as required

TYPICAL APPLICATIONS (Cont'd)





POLYNOMIAL GENERATOR CHECKER (PGC) SC2653

DESCRIPTION

The Signetics 2653 Polynomial Generator Checker (PGC) is a polynomial generator checker/character comparator circuit that complements a receiver/transmitter (R/T or USART/USRT/UART) in the support of character oriented data link controls. Table 1 defines many of the more commonly used PGC terms and abbreviations.

Parallel data characters transferred between the CPU and R/T are monitored by the PGC which performs block check character (BCC) and parity (VRC) generation/checking, single character detection, and two character sequence detection. Since the PGC operates on parallel characters, the data transmission format may be serial (synchronous or asynchronous) or parallel.

There are four modes of BCC accumulation and each mode can select one of three polynomials to compute the BCC. In the BISYNC normal and transparent modes, the PGC determines which characters are to be accumulated and which characters are to be excluded from the accumulation. The block terminating characters and the initiation and termination of BISYNC transparent text can be detected and an interrupt generated. The single interrupt output represents the inclusive OR of four maskable status conditions.

In the automatic accumulation mode, all characters are accumulated while the single accumulate mode requires a specific accumulation command for each character to be accumulated.

Character accumulation control and character comparisons are facilitated by a character class array which places each of 128 characters into one of four character classes. The four classes are normal, SYN/BISYNC not included, block terminating character (BTC)/search character (SC), and secondary search character (SSC).

Additional PGC applications include off-line R/T operation where the BCC is generated on data not sent to the R/T, BCC multiplexing by sharing the PGC among several R/Ts and reading/writing the partial BCC accumulation on a character by character basis, VRC generation/checking on characters appearing on a bidirectional data bus, and programmable character comparisons or searches.

PGC operation is half duplex (either receive or transmit, one way or two way alternate). Full duplex (two way simultaneous) is achieved by using two PGCs. The device is directly compatible with the Signetics 2651 Programmable Communications Interface (PCI) and 2661 Enhanced Programmable Communications Interface (EPCI). When used in BISYNC modes with the 2661, software requirements are minimized by the 2653-2661 control character comparisons, character sequence comparisons, and automatic DLE insertion/detection.

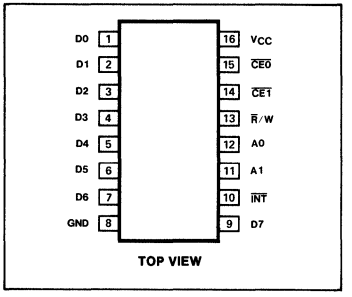
Other bus oriented R/Ts can be interfaced to the PGC with a minimum of external circuitry. See figure 1 for a typical system configuration.

This NMOS LSI circuit is TTL compatible, operates from a single + 5V supply and is contained in a 16 pin dual in line package.

FEATURES

- **Parallel Block Check Character accumulation/checking: CRC-16, CRC-12, LRC-8**
- **BISYNC normal and transparent modes**
- **Automatic or single character accumulation modes**
- **Character detection - up to 128 characters**
- **Two character sequence detection; examples: DLE-STX, ACK 0, ACK 1, WACK, RVI, DISC, WBT**
- **6, 7, or 8-bit characters**
- **VRC generation/checking on data bus**
- **Four maskable interrupt conditions**
- **Four classes of characters**
- **Internal power-on reset**
- **Maximum character accumulation rate of 500 kHz (4 Mbps)**
- **Directly compatible with Signetics 2651, 2652 and 2661**
- **No system clock required**
- **TTL compatible inputs and outputs**
- **Single 5V supply**
- **16-pin dual in line package**

PIN CONFIGURATION



TOP VIEW

APPLICATIONS

- **Character oriented data link control:**
  - **-dedicated to one USART/USRT**
  - **-multiplexed among several USART/USRTs**
- **Automated BISYNC with 2661 (minimal software intervention)**
- **BCC and VRC generation/detection on a block of memory or peripheral data**
- **Programmable character array comparator**

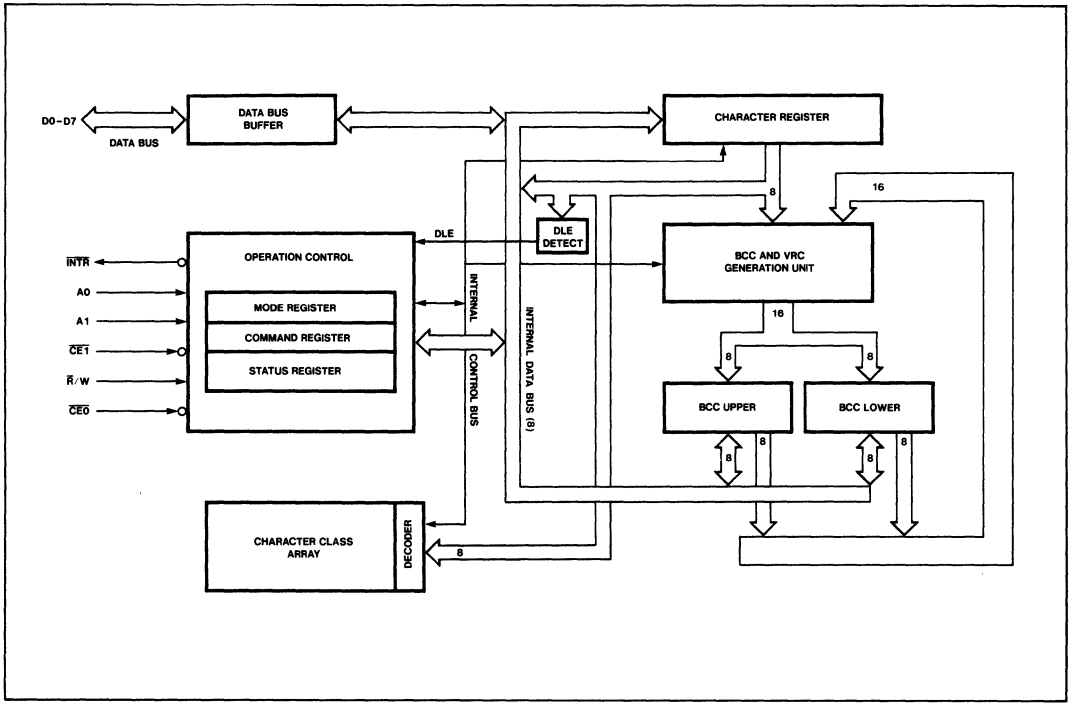
BLOCK DIAGRAM

The PGC consists of six major sections. These are the operation control, character class array, DLE ROM, character register, BCC and parity generators, and BCC registers. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the CPU data bus via a data bus buffer.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%, T_A = 0°C to 70°C
Ceramic DIP	SC2653CSI16
Plastic DIP	SC2653CSN16

BLOCK DIAGRAM



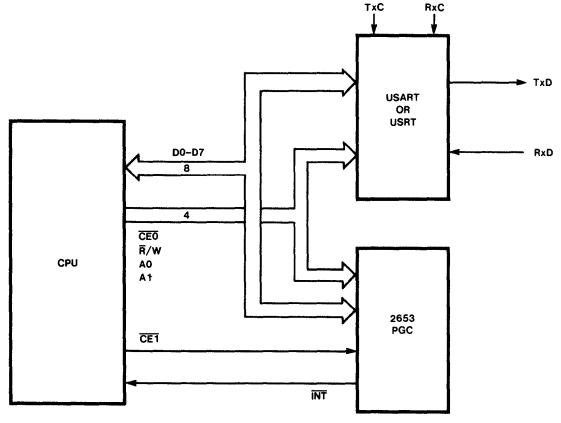
PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
VCC	16	I	**+5V:** Power supply
GND	8	I	Ground
A1-A0	11,12	I	**Address Lines:** Used to select internal PGC registers or character class array
R/W	13	I	**Read/Write:** Read command when low, write command when high
CE0	15	I	**Chip Enable:** Connected to chip enable input of a receiver/transmitter (R/T) circuit. It is used to strobe data being transferred between the CPU and the R/T into the PGC character register.
CE1	14	I	**Chip Enable:** Used in conjunction with the R/W signal to enable the transfer of data between the PGC and the CPU or DMA controller and to initialize the PGC registers.
D7-D0	9,7-1	I/O	**Data Bus:** 8-bit three-state bidirectional bus used to transfer data to or from the PGC via CE0 or CE1. All data, mode words, command words, and status information are transferred on this bus. D0 is the least significant bit; D7 is the most significant bit.
INT	10	O	**Interrupt:** Open drain active low interrupt output that signals the CPU that one or more maskable conditions are true: BCC error, VRC error, BTC/SC detect, SSC detect. The true conditions can be determined by reading the status register which in turn deactivates INT. A power on, clear BCC, or master reset command causes INT to be inactive (high).

Table 1. GLOSSARY

TERM/ABBREVIATION	DEFINITION
BCC	Block check character
BTC	Block terminating character
SC	Search character
SSC	Second search character (preceded by DLE)
CRC-16	$X^{16} + X^{15} + X^2 + 1$ divisor, dividend pre-cleared
CRC-12	$X^{12} + X^{11} + X^3 + X^2 + X + 1$ divisor, dividend pre-cleared
LRC-8	Horizontal parity on least significant 7 bits; vertical parity on most significant bit
VRC	Vertical redundancy check (character parity)
R/T	Receiver/transmitter circuit. Also known as USART/USRT/UART/PCI/MPCC
BISYNC	IBM binary synchronous communications (BSC), ANSI X3.28, ISO 1745
MSB	Most significant bit
LSB	Least significant bit
Rx	Receive
Tx	Transmit

TYPICAL SYSTEM CONFIGURATION



NOTES
1 Open drain $\overline{INT}$ may be OR tied with 2651 PCI, 2661 EPCI, or other open drain interrupt outputs
2 No external circuitry necessary if 2651 or 2661 is the USART

Figure 1

Operation Control Unit

This functional block stores configuration and operation instructions from the CPU and generates appropriate signals to control the device operation. It also contains read and write circuits to permit communications between the CPU and the PGC registers via the data bus. The mode, command, and status registers are in this logic block.

Character Register

Characters to be considered for BCC generation, parity generation and checking, or character comparisons are loaded into this register by either $\overline{CE0}$ or $\overline{CE1}$. This register serves as an input to the BCC and VRC generator, where the accumulation and parity generation takes place. The character register also serves as the input for character class array and DLE comparisons.

Character Class Array

This 128 x 2 array holds the character class associated with each of 128 possible 7-bit characters. The array is zero after a master reset. When the character class array is loaded (see PGC Addressing), the character on the data bus is placed in the class specified by the contents of command register bits CR2 and CR3. The PGC uses these two command bits to represent four different character classes. These are:

1. Normal class (included in the accumulation)
2. SYN character/BISYNC not included class
3. Block terminating character/search class
4. Second search character class (preceded by DLE)

These encoded character classes are used by the PGC:

1. To control the BCC accumulation of associated characters in BISYNC modes only. BCC accumulation in automatic or single accumulation modes is carried out independent of the character classes.
2. To detect characters and two character sequences in all modes of accumulation and to set the control character detect bits in the status register.

It should be noted that any number of characters (up to 128 for CRC-16 or LRC-8; up to 64 for CRC-12) can be put into any one class.

If VRC is specified along with CRC-16 then the least significant 7 bits of the character are used for character array comparison. If VRC is not enabled, but CRC-16 is, the MSB of the character then determines whether a

character comparison is to take place. If the MSB is 0, the comparison takes place; if the MSB is 1, the comparison does not take place and the character is processed as though it were in the normal class. This enables the PGC to detect all communication control characters and DLE-SSC sequences.

Only the first 64 locations of the array are accessed if CRC-12 is selected. The user should right justify each six bit character (D0-D5) to be written into the character class array. Bit 6 must be zero.

If VRC is enabled, the generated parity becomes the most significant bit of the character to be compared. VRC is not allowed in BISYNC transparent mode.

The method in which the character register contents is compared against the character class array depends on the BCC polynomial chosen. Figure 2 illustrates the comparison process.

DLE Read Only Memory

The DLE characters are stored internally and are selected by the error polynomial as follows:

CRC-12: 01 1111
LCR-8 or CRC-16:
No VRC or odd VRC: 0001 0000
Even VRC 1001 0000

BCC and Parity Generator

This functional block performs all the necessary computation to generate and update the BCC accumulation on a character by character basis. It contains the three generator polynomials (CRC-16, CRC-12, and LRC-8) that can be selected to compute the BCC. This block also checks and generates odd or even parity for 7-bit (ASCII) characters.

BCC Registers

This block consists of two 8-bit registers (BCC upper and BCC lower) which contain the high and low order bytes of the BCC accumulation. The result of the accumulation from the BCC and parity generator is stored in these registers. A recirculating register address pointer is initialized by a power on, master reset, or clear BCC command. The pointer alternately selects BCC upper and lower on successive BCC register accesses for CRC-16 or CRC-12. For LRC-8, BCC upper is always selected.

BCC upper and lower are cleared by a clear BCC or master reset command. The highest term of the BCC polynomial is always represented by bit 0 of BCC upper; the lowest term is always represented by bit 7 of BCC lower (see figure 3, Orientation of BCC Polynomials.)

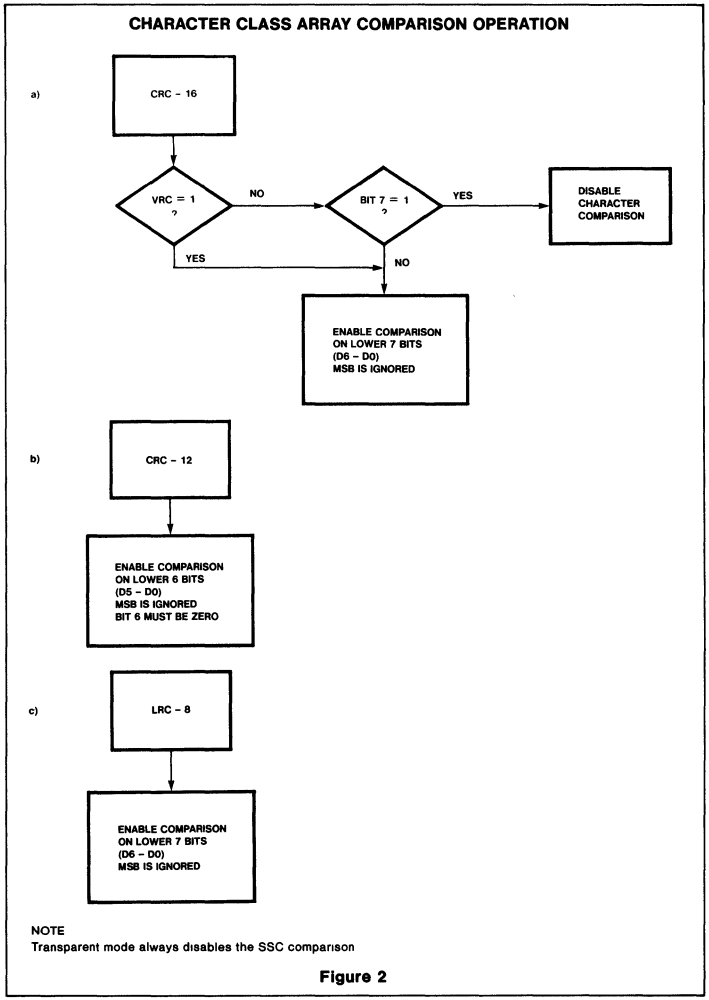


Figure 2

The length of the block check character depends on the error checking polynomial that is selected. If LRC-8 is chosen, the BCC result is stored entirely in BCC upper. The BCC lower remains unchanged from previous setting. Both BCC registers are used when CRC-16 is specified. When CRC-12 is selected, the block check character is 12 bits long. The six least significant bits of the BCC are stored in the least significant bits of the BCC lower. The remaining upper six bits of the BCC are stored in least significant bits of BCC upper. The two most significant bits in each BCC register are filled with zero.

The BCC register(s) are read by the CPU after the last data character is transmitted. They can then be sent to the R/T to complete a transmitted block of data. These registers are read and loaded when one PGC is time-shared by several R/Ts. Refer to Applications Information - Multiplexed PGC.

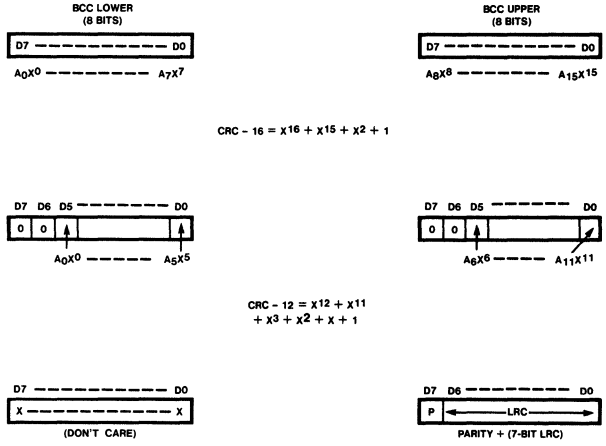
PGC Addressing

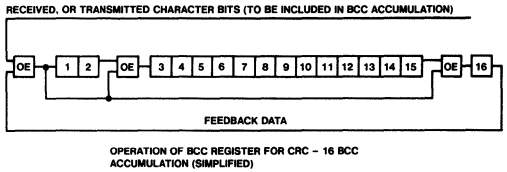
All internal registers and the character class array are selected by the unique address codes shown in table 2.

ORIENTATION OF BCC POLYNOMIALS

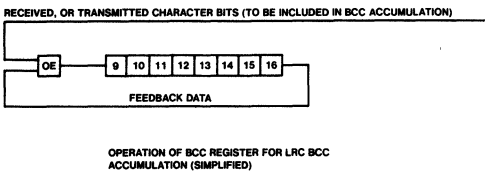
$$\frac{M(X)}{G(X)} = Q(X) + \frac{R(X)}{G(X)}, \quad \text{WHERE } R(X) = A_n X^n + A_{n-1}X^{n-1} \cdots + A_0 X^0$$

M (X) · BINARY POLYNOMIAL (DATA STREAM)
G (X) FIXED DIVISOR TO GENERATE BCC
Q (X) · QUOTIENT AFTER BCC GENERATION
R (X) REMAINDER AFTER BCC GENERATION





OPERATION OF BCC REGISTER FOR CRC - 16 BCC ACCUMULATION (SIMPLIFIED)



OPERATION OF BCC REGISTER FOR LRC BCC ACCUMULATION (SIMPLIFIED)

Figure 3

Table 2. ADDRESS CODES

$\overline{CE0}$	$\overline{CE1}$	A1	A0	$\overline{R}/W$	FUNCTION
0	0	X	X	X	Operation not guaranteed
0	1	0	0	0	If MR2 = 0 load data bus into character register If MR2 = 1 PGC not selected[1]
0	1	0	0	1	If MR2 = 1 load data bus into character register If MR2 = 0 PGC not selected[1]
0	1	0	1	X	PGC not selected[1]
0	1	1	0	X	PGC not selected[1]
0	1	1	1	X	PGC not selected[1]
1	0	0	0	0	Read character register
1	0	0	0	1	Load data bus into character register if MR1,0 $\neq$ 00[2]; write character class array using CR3, CR2 class code if MR1,0 = 00[3,4]
1	0	0	1	0	Read Status register
1	0	0	1	1	Write command register
1	0	1	0	0	Read mode register
1	0	1	0	1	Write mode register
1	0	1	1	0	Read BCC upper/lower[5]
1	0	1	1	1	Write BCC upper/lower[5]
1	1	X	X	X	PGC not selected[1]

NOTES
1 Data bus is 3-state
2 Character will not be accumulated unless MR3 = 1
3. Character will not be accumulated even if MR3 = 1
4 The mode bits MR1 and MR0 are cleared to 00 by power-on-reset, master reset, or by loading the mode register bits MR1 and MR0
5 Recirculating internal pointer selects BCC Upper on first access, BCC lower on next access for all BCCs except for LRC-8; in case of LRC-8, the pointer only selects BCC upper.

INTERFACE SIGNALS AND TIMING

PGC data transfers are controlled by A1, A0, and $\overline{R}/W$ which must be stable prior to the active low going chip enable pulse. $\overline{CE0}$ is used for PGC monitoring of data transfers between a CPU/DMA controller and a R/T; $\overline{CE1}$ is used for direct CPU-to-PGC transfers. MR3 must be set prior to loading the character register in order to accumulate or compare characters via $\overline{CE1}$. The active low (leading) edge of chip enable initiates a PGC read/write cycle; the rising (trailing) edge ends the cycle and also serves as a write strobe.

When loading the character, mode, or command register, the data bus is strobed into the selected register on the trailing (rising) edge of the appropriate $\overline{CE}$. When writing into the character class array, the data on the bus (the special character) is placed in the class specified by command register bits CR3 and CR2.

Characters are transferred into the character register when $\overline{CE0}$ is active (low) depending on the state of MR2 and the $\overline{R}/W$ input. Characters from the R/T are loaded into the character register when in receive mode (MR2 = 0 and $\overline{R}/W$ = 0) while CPU/DMA characters are loaded into the character register when in transmit mode (MR2 = 1 and $\overline{R}/W$ = 1). The time between consecutive chip enables is given by t_{CEC} or t_{CED}.

The open drain active low interrupt signal ($\overline{INT}$) goes active whenever one or more of four maskable status conditions (SR0-SR3) are true (= 1). A status read deactivates $\overline{INT}$.

The same techniques used in interfacing the 2651 PCI to 8-bit microprocessors can be used to interface the 2653 PGC (consult Application Note M22). Note that when addressing the R/T's holding registers, the PGC pins must have A1,A0 = 00 and that the address and $\overline{R}/W$ signals must be stable (set up) prior to the active low chip enable. When using the 2651 or 2661 as the R/T, the PGC's A1, A0, $\overline{R}/W$, and $\overline{CE0}$ are directly connected to comparable 2651 or 2661 signals. Schematics of a 2653 monitoring data transfers to/from the Signetics 2651/2661 and 2652 are shown in figures 4 and 5.

An alternate interfacing technique is to treat the PGC as an independent peripheral device. This necessitates a write character register instruction after the CPU reads or writes a character to or from the R/T.

2651 OR 2661/2653 INTERFACE

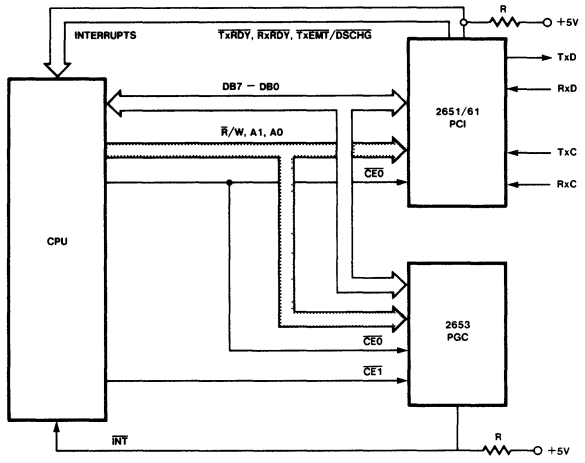


Figure 4

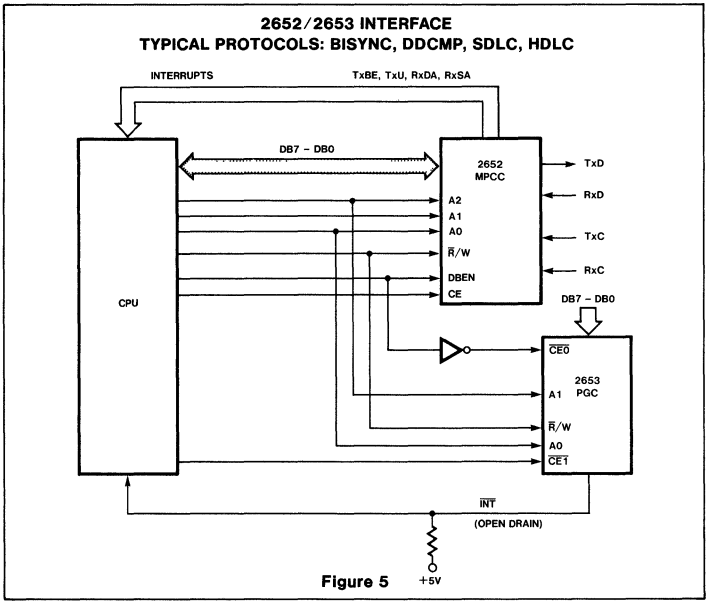


Figure 5

PGC PROGRAMMING

The PGC operational mode must be initially programmed by the CPU (see figure 6). The mode register, command register and character class array should be written into, after a power-on-reset or a master reset command. The character class array should be programmed only for the classes pertinent to the application. After a master reset, the character class array is zero which places all characters in the normal class (included in the BCC accumulation).

OPERATION

The PGC should be initially configured by the CPU (via $\overline{CE1}$) prior to systems operation. This is done by loading the mode register, command register and character class array (see PGC PROGRAMMING). Characters may then be loaded into the character register for BCC accumulation, VRC generation/checking, BTC/SC and DLE-SSC comparisons. See table 3 for a summary of BCC accumulation modes.

BCC accumulation depends on the mode selected.

BISYNC Normal

In BISYNC normal mode, all characters loaded into the character register are accumulated except those in the SYN/BISYNC not included class. During receive (MR2 = 0), a BTC/SC match will cause the BCC accumulation to stop after the next one (LRC-8) or two (CRC-12 or CRC-16) characters have been accumulated. At that time, if the BCC accumulation does not equal zero, the BCC error bit (SR0) will be set and $\overline{INT}$ will go active if the corresponding mask bit (CR4) is enabled (= 1). In transmit (MR2 = 1), the BCC accumulation is automatically stopped once the BTC/SC character has been accumulated. The CPU must read the BCC upper and BCC lower (CRC-12 or CRC-16) register(s) and transmit them to the R/T.

Note that the received BCCs are not subject to VRC if CRC-16 is selected. If LRC-8 is selected, the received BCC is subject to VRC. An incorrect result will set the VRC error bit (SR1). After its accumulation, the least significant 7 bits of BCC upper are checked and a non-zero result will set the BCC error bit (SR0). BCCs are not checked against the character class array nor are they compared to the DLE ROM.

Second search character (SSC) detection is enabled so that a DLE-STX or two character communication control sequence can be detected.

Table 3. SUMMARY OF BCC ACCUMULATION MODES

ACCUMULATION MODES	START ACCUMULATION	STOP ACCUMULATION	CHARACTERS EXCLUDED FROM ACCUMULATION
BISYNC normal and BISYNC transparent	Clear BCC registers command Mode register is loaded with BISYNC or automatic mode Start accumulation command Load BCC registers	After BTC has been detected and received BCC is accumulated After transmitted BTC has been accumulated Single mode is selected	SYN/BISYNC not included class in normal mode DLE-SYN/not included class and first DLE of a DLE non SYN pair in transparent mode These characters are not excluded if preceded by an odd number of DLEs
Automatic	Same as above	Single mode selected	None
Single	Start accumulation command	After each character has been accumulated	Up to user who must generate start accumulation command for each character to be included

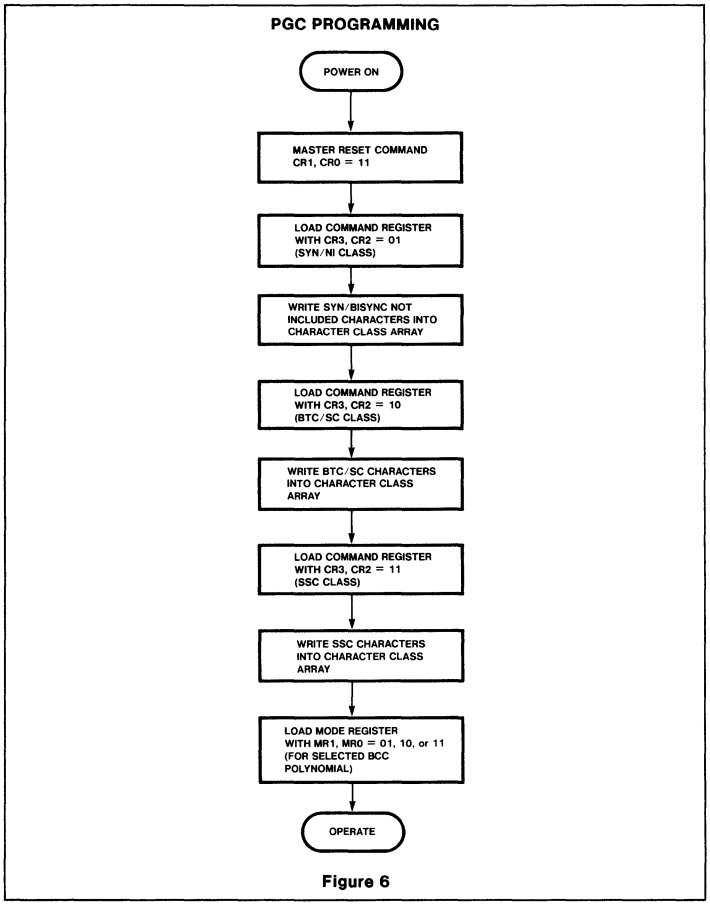
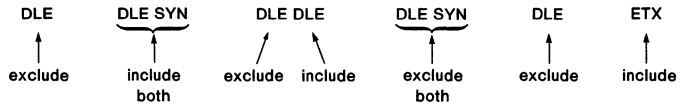


Figure 6

BISYNC Transparent

BISYNC transparent mode should be used for data blocks beginning with DLE-STX if the DLEs are transferred between CPU and R/T ($\overline{CE0}$) or CPU and PGC ($\overline{CE1}$), i.e., DLEs are *not* stripped. VRC should be disabled in this mode. Characters excluded from the BCC accumulation are the first DLE of a DLE-non SYN sequence pair and the DLE-SYN sequence if not preceded by an odd number of DLEs. For example, consider the following transparent mode character string:



In receive and transmit modes, the termination of BCC accumulation works exactly as in BISYNC normal, except that the BTC/SC must be immediately preceded by an odd number of DLEs to be identified as a BTC/SC.

Second search character detection is not enabled in BISYNC transparent.

After a BTC/SC class character is detected by the PGC when receiving in either BISYNC mode, the following one or two characters are accumulated (depending on LRC-8 or CRC-12/16, respectively) and the PGC will automatically stop further accumulation. However, *the PGC can continue the accumulation* if a start accumulate command is issued or either BISYNC mode is loaded into the mode register. The start accumulate command should be given to the PGC before loading the character that follows the detected BTC/SC. This procedure enables a special search character to be detected (the BTC/SC detect bit (SR2) will be set and an interrupt generated if CR6 = 1) with the BCC accumulation continuing (see figures 7 and 8).

Automatic Accumulate

All characters loaded into the character register are accumulated, BTC/SC and SSC detection is enabled. The BCC accumulation is not automatically terminated. (The CPU must use single accumulate mode to stop the accumulation). When in receive mode, the BCC error bit (SR0) is set/reset after accumulating each character so that the CPU must examine this bit after the last character is accumulated. SR0 = 0 if the accumulated remainder in the BCC register(s) is zero; otherwise SR0 = 1. Examples of use of automatic accumulate mode usage include an R/T (2651/2661) in transparent DLE/SYN strip mode and asynchronous/synchronous/parallel DDCMP.

Single Accumulate

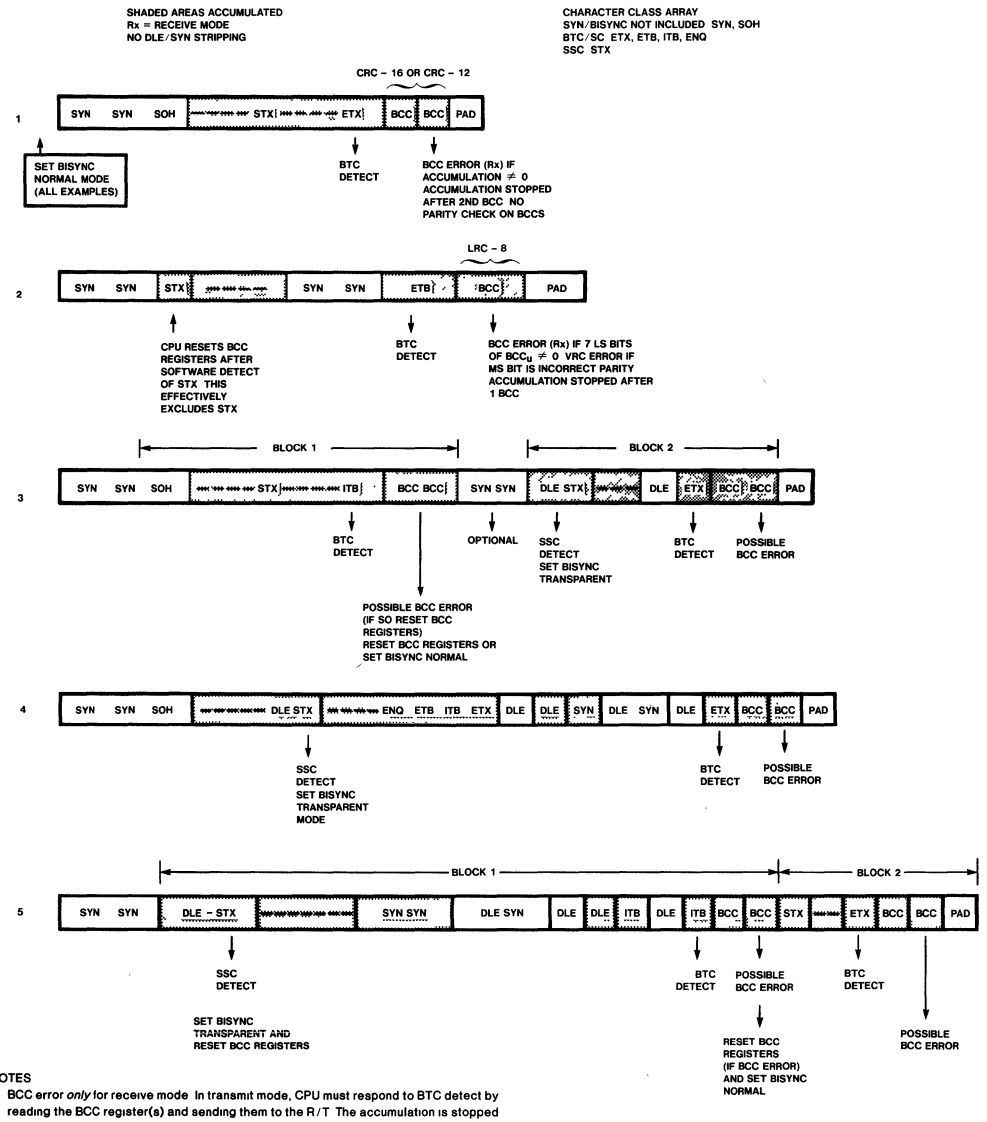
All characters for which a start accumulate command (CR1, CR0 = 01) is given are accumulated and compared against the character class array. If not given, the BCC accumulation is not updated and BTC/SC and SSC detection is disabled. Operation in this mode is otherwise identical to automatic accumulate.

Single accumulate mode can be used to selectively accumulate characters under CPU control or to accumulate characters that were unintentionally excluded in one of the other modes.

Polynomial Selection and DLE Comparison

The BCC polynomial may be CRC-16, CRC-12 or LRC-8. The cyclic redundancy check (CRC) is generated by dividing the binary value of a character in the character register by the selected polynomial. The quotient is discarded and the remainder is used as the BCC (two 6-bit characters for CRC-12, two 8-bit characters for CRC-16). CRC-16 uses all 8 bits of each BCC register. CRC-12 uses the least significant 6 bits of the BCC registers. The two most significant bits of the BCC registers are cleared to zero whenever CRC-12 is selected (see figure 3).

EXAMPLES - BISYNC TEXT MESSAGE BCC ACCUMULATION



NOTES

1. BCC error *only* for receive mode In transmit mode, CPU must respond to BTC detect by reading the BCC register(s) and sending them to the R/T The accumulation is stopped after the BTC is accumulated
2. ENQ (DLE-ENQ) in a text message should be treated as an abort
3. Opening SYNs may be stripped by the R/T
4. The single accumulate mode and command can be used to accumulate a character that inadvertently was excluded (For example, the DLE of a DLE-STX if the PGC was in transparent mode and there was not a line turnaround prior to the DLE) The single accumulation should be done using $\overline{CET}$ after the BCC(s) have been accumulated

Figure 7

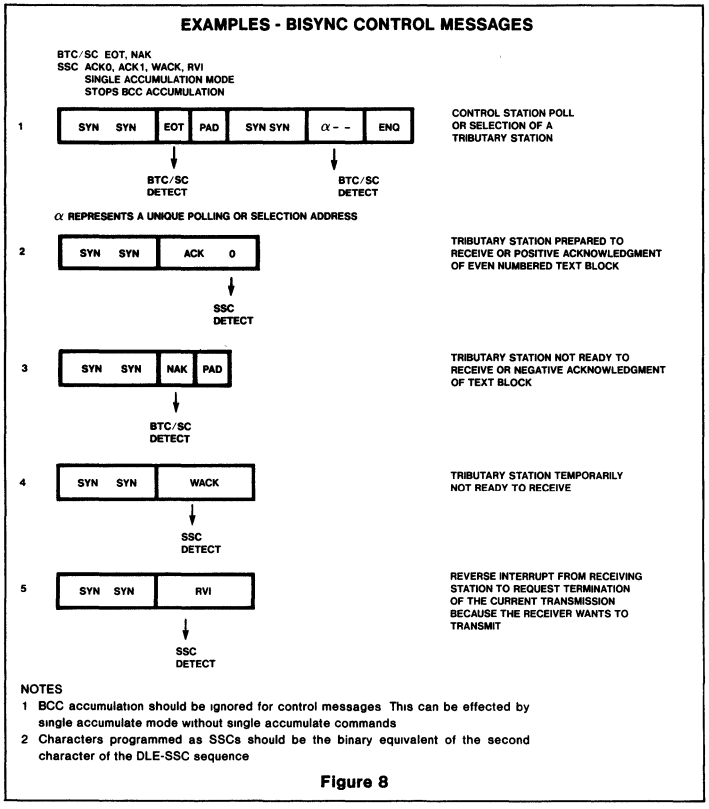


Figure 8

When the PGC is in receive mode (MR2 = 0), the received BCC will be accumulated. The result will be zero for an error free message.

CRC-12 is used with 6-bit codes. The internal 6-bit transcode DLE character hex 1F is selected by CRC-12. VRC should be disabled (MR4 = 0) for CRC-12 operation. The two most significant bits of the character register are ignored when compared to the internal 6-bit DLE. When the character is checked against the character class array, the MSB is ignored and the next MSB (bit 6) is assumed to be zero. If CRC-12 is specified, the user must write to the character class array with bit 6 cleared.

CRC-16 or LRC-8 implies the use of ASCII or EBCDIC although any 7-bit plus parity or 8-bit no parity code may be used (with DLE = hex 10 or hex 90). The DLE character compare is on an 8-bit basis with the generated parity (if VRC is enabled) as the MSB. When the character is compared against the character class array, the MSB is not used. This may result in a false BTC or SSC detection if there is a VRC error. However, the VRC error bit (SR1) will be set under that condition.

The LRC-8 is generated by the exclusive OR of the 7 least significant bits of the character register and the BCC upper. The most significant bit of the LRC-8 check character is a vertical odd/even parity bit (MR5 = 0/1), which is generated on the least significant bits of that character. The selection of LRC-8 implies VRC is enabled and that only the BCC upper is used for the BCC accumulation. The BCC lower remains unchanged from previous setting.

VRC Generation and Detection

Parity (VRC) is enabled by MR4 and specified as odd or even by MR5. VRC should be disabled when in BISYNC transparent mode and whenever CRC-12 or CRC-16 (EBCDIC) is selected as the BCC polynomial. MR4 = 1 enables VRC generation and detection for *both* receive and transmit operations. Characters loaded into the character register will have VRC generated on the least significant 7 bits with the generated parity bit written into the character register MSB. If the generated parity does not match the MSB of the loaded character, the VRC error bit (SR1) is set and $\overline{INT}$ asserted if the corresponding mask bit was enabled (CR5 = 1). Thus, if 7-bit characters are to be transmitted with VRC, CR5 should be zero and SR1 ignored. 8-bit characters with a VRC bit in the MSB position are parity checked by the PGC in both transmit (to R/T) and receive (from R/T) modes, i.e., the PGC operates as a data bus parity checker.

CHARACTER CLASSES

Normal (Included in the Accumulation)

Any character that belongs to this class is normal data, i.e., the character is not a communication control or other special character. Characters in this class are always accumulated in BISYNC, automatic and single accumulation modes.

SYN Character/BISYNC Not Included

SYN characters are never accumulated in BISYNC normal accumulation mode. In BISYNC transparent accumulation mode, the DLE-SYN character pair is not accumulated, but a SYN not preceded by a DLE is accumulated. (DLE is implied as an odd number of DLEs).

Block Terminating Character (BTC)/Search Character (SC)

BTC/SC characters have two functions in the PGC: termination of BCC accumulation and character detection. In BISYNC transparent mode, a BTC/SC must be preceded by an odd number of DLEs to be recognized.

- **Termination of BCC Accumulation**

  In BISYNC normal and transparent accumulation modes, the PGC will stop the accumulation upon the detection of the BTC/SC character. Examples of BTCs are ETX, ETB, ITB, ENQ.

  In receive mode, the accumulation is stopped after the following one (LRC-8) or two (CRC-12, CRC-16) character(s) have been accumulated. In transmit mode, the accumulation is stopped after the BTC/SC character has been accumulated. The BTC/SC character is always accumulated in all of the accumulation modes.

- **Character Detection**
  BTC/SC characters will be detected in any of the four accumulation modes when that character is being accumulated. The BTC/SC status bit (SR2) is set on detection. Since detection also stops BISYNC BCC accumulation, the BISYNC accumulation must be restarted if the character is not a BTC. This can be effected by loading BISYNC mode into the mode register or generating a start accumulation command.

Second Search Character Class (SSC)

Control functions in character oriented data link control procedures can be represented by a sequence of two characters, the first character being a DLE. Examples include ACK0, ACK1, WACK, RVI, DISC, WBT and the initiation of transparent text (DLE-STX). The PGC will detect such sequences, except in BISYNC transparent mode, when an SSC class character is being accumulated after being immediately preceded by an odd number of DLEs. Under those conditions, the SSC status bit (SR3) will be set.

The SSC character is always accumulated in all of the accumulation modes.

REGISTER BIT DESCRIPTION

The operation of the PGC is determined by programming the mode register and the command register. The status register provides feedback on potential interrupt conditions. Formats of these registers are shown in table 4.

Table 4. PGC REGISTER BIT FORMATS

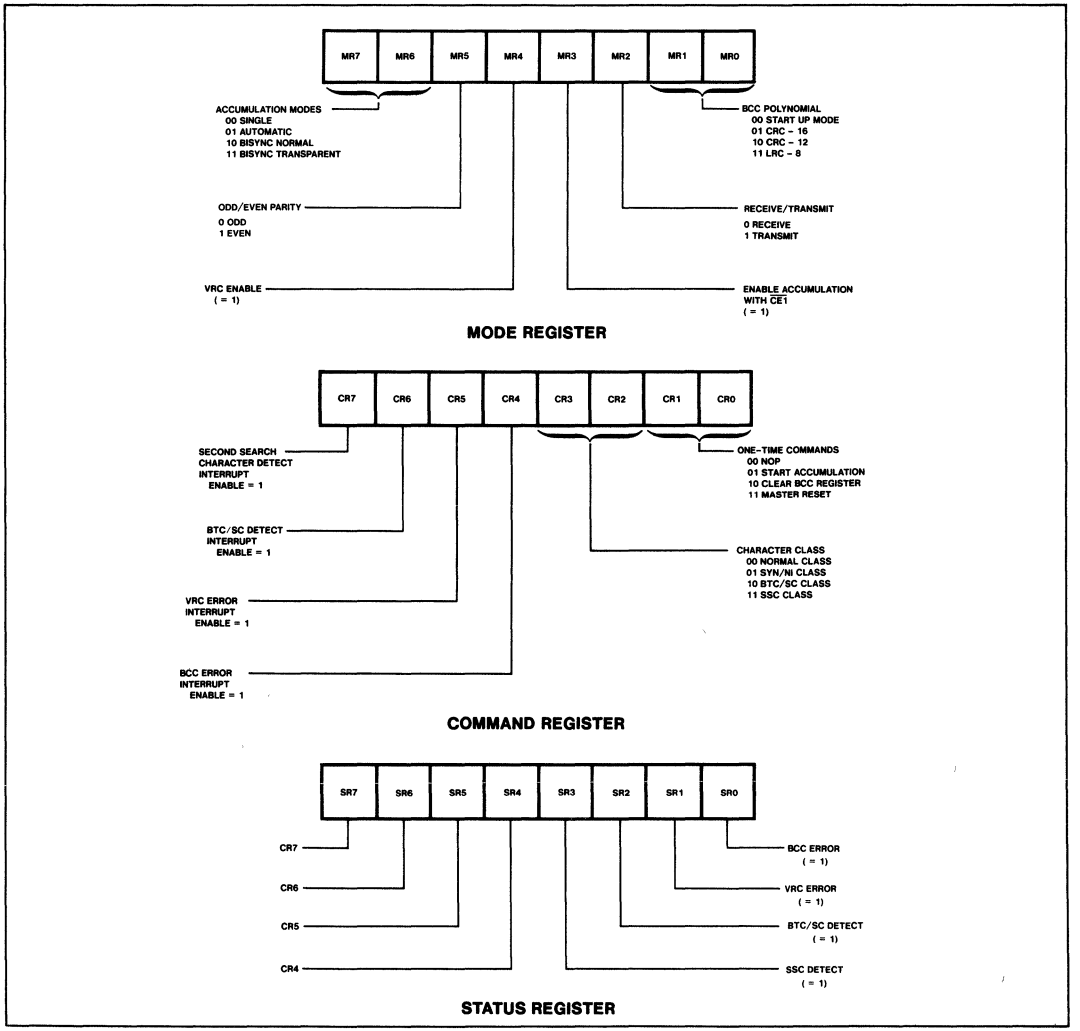


Table 5. BCC ACCUMULATION BY CHARACTER CLASS

CR3	CR2	CLASS	BISYNC NORMAL	BISYNC TRANSPARENT	AUTOMATIC ACCUM	SINGLE ACCUM
0	0	Normal	Yes	Yes	Yes	Yes
0	1	SYN/BISYNC not included	No	Yes, unless preceded by an odd number of DLEs	Yes	Yes
1	0	BTC/SC	Yes	Yes	Yes	Yes
1	1	SSC*	Yes	Yes	Yes	Yes

NOTE
*Preceded by DLE

Mode Register

The mode register defines general PGC operation characteristics. MR1 and MR0 = 00 permit the character class array to be programmed. These bits will be zero after a power on or master reset command. After the character class array is programmed, these bits should be set to 01, 10, or 11 to select the CRC-16, CRC-12 or LRC-8 polynomials.

MR2 (Tx/$\overline{Rx}$) determines whether or not the PGC is to generate (Tx) or generate and check (Rx) the BCC. It is used with $\overline{R}$/W to determine if the data bus is to be loaded into the character register when $\overline{CE0}$, $\overline{CE1}$, A1, A0 = 0100.

If MR2 = 1: 1) the PGC will generate the BCC, but will never set the BCC error bit (SR0). 2) If the $\overline{R}$/W pin is high when $\overline{CE0}$, $\overline{CE1}$, A1, A0 = 0100, then the data bus will be loaded into the character register. If $\overline{R}$/W is low under these conditions, the PGC is not selected.

If MR2 = 0: 1) the PGC will accumulate the BCC and set the BCC error bit (SR0) when appropriate. 2) If the $\overline{R}$/W pin is low when $\overline{CE0}$, $\overline{CE1}$, A1, A0 = 0100, then the data bus will be loaded into the character register. If $\overline{R}$/W is high under these conditions, the PGC is not selected.

MR3 is a $\overline{CE1}$ accumulate/compare enable bit. If MR3 = 0, characters loaded into the character register by $\overline{CE1}$ are *not* accumulated, checked against the character class array, or compared to the DLE ROM. Parity will be generated and checked if VRC is enabled (MR4 = 1). The primary use of MR3 = 0 is to generate parity on a 7-bit character which is to be transmitted to an R/T. The CPU loads the character register with the 7-bit character and reads the 8-bit VRC generated character via $\overline{CE1}$. This 8-bit character is then transferred to the R/T via $\overline{CE0}$. Another application of MR3 = 0 is for a CPU to interleave parity checking on memory data ($\overline{CE1}$) with on line R/T data transfers ($\overline{CE0}$).

If MR3 = 1, characters loaded into the character register by $\overline{CE1}$ will be accumulated (according to the BCC accumulation mode selected) and compared against the character class array and DLE ROM. This bit setting should be used when the CPU/DMA controller sends data characters to be accumulated or compared to the PGC and the R/T is inactive (off line). If the R/T were active, then a DLE or BTC loaded into the character register via $\overline{CE0}$ would cause incorrect accumulation and character comparisons if the next character was loaded via $\overline{CE1}$.

MR4 is a VRC enable bit. If MR4 = 1, VRC is enabled as odd/even by MR5. VRC is generated on the 7 LS bits of the character and the MS bit is checked against the generated parity. If not equal, SR1 is set. If MR4 = 0, VRC is not enabled. MR4 = 0 is used for BISYNC transparent mode with ASCII code, and for both BISYNC modes for EBCDIC and SBT.

MR5 is an odd/even VRC bit. If MR5 = 1, the total number of 1 bits in the character including the parity bit is even. If MR5 = 0, the total number of bits is odd. This bit is ignored if MR4 = 0.

MR7, MR6 select the BCC accumulation mode. These modes have been previously discussed in the operation section.

Command Register

The command register contains four interrupt enables, a 2-bit character class code used when programming the character class array, and 2 bits that specify three one time commands and a NOP.

CR1, CR0 = 00 is a NOP. This bit setting is used when changing CR7-CR2 without affecting any of the 3 one time commands.

CR1, CR0 = 01 is a start BCC accumulation command. In single accumulation mode, the character accumulated is the character that is in the character register at the time the command is given. The accumulation stops immediately after the character has been accumulated. If the command is given in either of the BISYNC or automatic accumulation modes, it enables the PGC to accumulate the BCC starting with the *next* character loaded into the character register. This is a means of restarting a BISYNC normal accumulation after detection of a BTC/SC that is not a valid BTC (example; CR, LF, TAB). In all accumulation modes, a previously detected DLE will not be cancelled by this command.

CR1, CR0 = 10 is a clear BCC registers command. Both BCC registers are cleared along with the associated internal pointer and SR0-SR3. The pointer points to BCC upper. $\overline{INT}$ is forced high. This command permits BCC accumulation, starting with the next character loaded into the character register in BISYNC or auto modes. Single accumulate mode requires a start BCC accumulation command.

CR1, CR0 = 11 is a master reset command. All internal registers (except the character register), the internal pointer, and the entire character class array are cleared. $\overline{INT}$ is forced high.

CR3 and CR2 are used for programming the character class array. During a write character class array instruction, the character corresponding to the 7 LS bits of the data bus is placed in the class contained in CR3 and CR2. The encoded character classes control the accumulation of the associated character as shown in table 5.

Detection operates under the conditions shown in table 6.

Table 6. BTC/SC AND SSC DETECTION CONDITIONS

CLASS	BISYNC NORMAL	BISYNC TRANSPARENT	AUTO ACCUM	SINGLE ACCUM
BTC/SC	Yes	Yes*	Yes	Yes †
SSC	Yes*	No	Yes*	Yes*†

NOTES
* Only if immediately preceded by an odd number of DLEs
† Start accumulate command necessary for detection

CR7, CR6, CR5, CR4 are interrupt enables that individually enable/disable $\overline{INT}$ when the corresponding status register condition is true (set). Each bit is set in order to enable $\overline{INT}$ upon the condition. Each bit is reset to disable $\overline{INT}$ upon the condition. The state of these bits may be read via the status register (SR7, SR6, SR5, SR4).

The corresponding status bits (SR3, SR2, SR1, SR0) are set independent of the interrupt enables. The bit assignments are:

CR4 - BCC error interrupt enable

CR5 - VRC error interrupt enable

CR6 - BTC/SC detect interrupt enable

CR7 - DLE-SSC detect interrupt enable

Status Register

This register reflects the status of the 4 conditions that are potential interrupt ($\overline{INT}$) sources and the 4 interrupt enables in the command register. A status register read clears SR0, SR1, SR2, SR3 and deactivates $\overline{INT}$. These bits are also cleared by a master reset or clear BCC command.

SR0 is a BCC error bit. This bit can only be set in receive mode (MR2 = 0). In BISYNC normal and BISYNC transparent modes, SR0 will be set/reset once the accumulation has been stopped by the detection of the BTC/SC character and accumulation of the BCC(s).

In automatic and single accumulate modes, SR0 is set/reset after each character in the character register has been accumulated.

The rules for the detection of a BCC error are:

SR0 = 1	LRC-8: 7 least significant bits of BCC upper ≠ 0 CRC-12, CRC-16: BCC upper *or* BCC lower ≠ 0
SR0 = 0	LRC-8: 7 least significant bits of BCC upper = 0 CRC-12, CRC-16: BCC upper *and* BCC lower = 0

SR1 is a VRC error bit. When set, this bit reports a character parity error (on receive or transmit) when parity is enabled (MR4 = 1). Parity is odd/even as specified by MR5. The parity bit will be regenerated in the character register.

SR2 is a BTC/SC detect bit. When set, this bit indicates the character being accumulated is of the BTC/SC class for BISYNC normal, automatic and single accumulate modes. In BISYNC transparent mode, the BTC/SC character being accumulated must be *immediately* preceded by an odd number of DLEs for this bit to be set.

SR3 is a DLE SSC detect bit. This bit can only be set when in BISYNC normal, auto, or single accumulate modes. When set, it indicates that the character being accumulated is of the SSC class when that character was *immediately* preceded by an odd number of DLEs.

SR7, SR6, SR5, SR4 are interrupt enables. These 4 bits reflect the state of the interrupt enable command bits CR7, CR6, CR5, and CR4, as follows:

SR4 - BCC error

SR5 - VRC error

SR6 - BTC/SC detect

SR7 - SSC detect

APPLICATIONS INFORMATION

Dedicated PGC

The most efficient use of the 2653 is to dedicate one to each R/T for two way alternate (half duplex) operation or two to each R/T for two way simultaneous (full duplex) operation (see figure 9). The CPU configures each PGC (using $\overline{CE1}$) by initializing the mode register, command register, and character class array. Data transfers to or from the R/T can then be on a DMA basis with each receiver holding register ready signal used as a read request (RREQ) and each transmit holding register available signal used as a write request (WREQ) to the DMA controller. The CPU needs only to respond to enabled interrupts from each of the PGCs. The individual $\overline{INT}$ outputs can be wire-OR'd into a single CPU interrupt ($\overline{INTRPT}$) with one pull up resistor. Each PGC in this system has a unique address that is decoded into the respective chip enables.

The CPU or DMA controller could send a block of memory data to the PGC to be error checked without sending that data to the R/T. In that case, $\overline{CE1}$ is used.

Multiplexed PGC

One PGC may be time-shared among a few R/Ts if the CPU saves and restores the mode register and partial BCC result in the BCC registers. These registers are accessed via $\overline{CE1}$. There must be a separate save area for each R/T (serial channel) and a channel pointer indicating the last R/T that transferred or received a data character (see figure 10).

The loading of the BCC registers will clear SR0-SR3 and all previously detected special characters, i.e., DLE, BTC/SC, BCC (BISYNC modes). The BCC accumulation will start again when the next character is loaded into the character register in all accumulation modes except single. That mode requires a start accumulation command.

Figures 11 and 12 represent software flow diagrams for transmit and receive service requests. Note that interrupts from all other R/Ts must be masked during a read or write to the BCC registers so as not to affect the internal BCC address pointer. It is recommended that all R/T interrupts be masked while servicing an interrupt that accesses any PGC register.

BISYNC Operation

Table 7 is a concise listing of 2651/2661 operating modes with recommended corresponding 2653 BCC accumulation modes.

Character Comparator

The PGC can be used as a programmable data bus character comparator which monitors data bus transfers (CPU↔peripheral, CPU↔CPU, CPU↔memory, memory↔peripheral (via DMA)). The user selectively loads the character class array with BTC/SC and SSC characters to be compared. Status bits will be set and an interrupt can be generated upon SC and DLE - SSC detection. A match on one to 128 different characters or DLE - SSC sequences can be programmed.

Figure 13 depicts an arrangement where the DMA controller or slave CPU handles data bus transfers, the PGC interrogates the data bus, and the host CPU responds to PGC interrupts.

Table 7. BISYNC (ANSI 3.28, ISO 1745) Modes for 2651/2661 and 2653

2651/2661 OPERATING MODES	2653 BCC ACCUMULATION MODE
Sync normal non-strip	BISYNC normal
Sync transparent non-strip	BISYNC transparent
Normal SYN/DLE strip[1]	BISYNC normal
Transparent SYN/DLE strip[1]	Automatic accumulate[2]
Async (with SYN/DLE characters)	BISYNC normal

NOTES

1 CPU should switch to non-strip mode after BTC detect Otherwise a received BCC could be inadvertently stripped

2 SSC detect should be ignored.

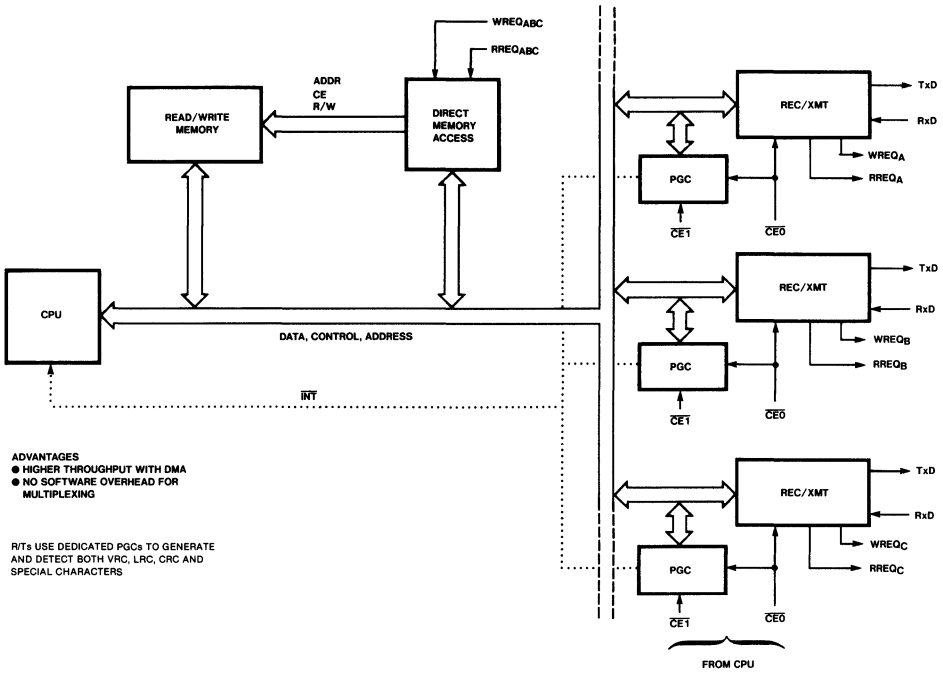


Figure 9

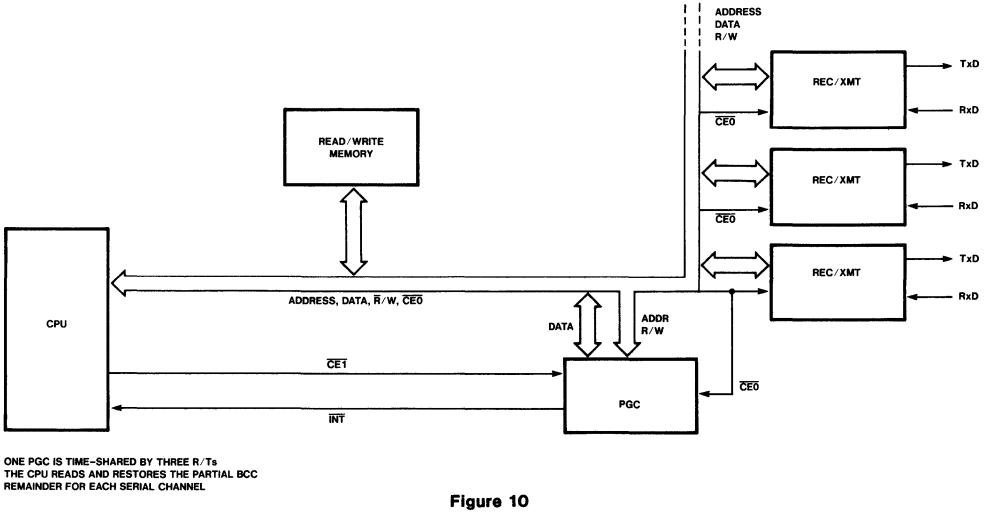


Figure 10

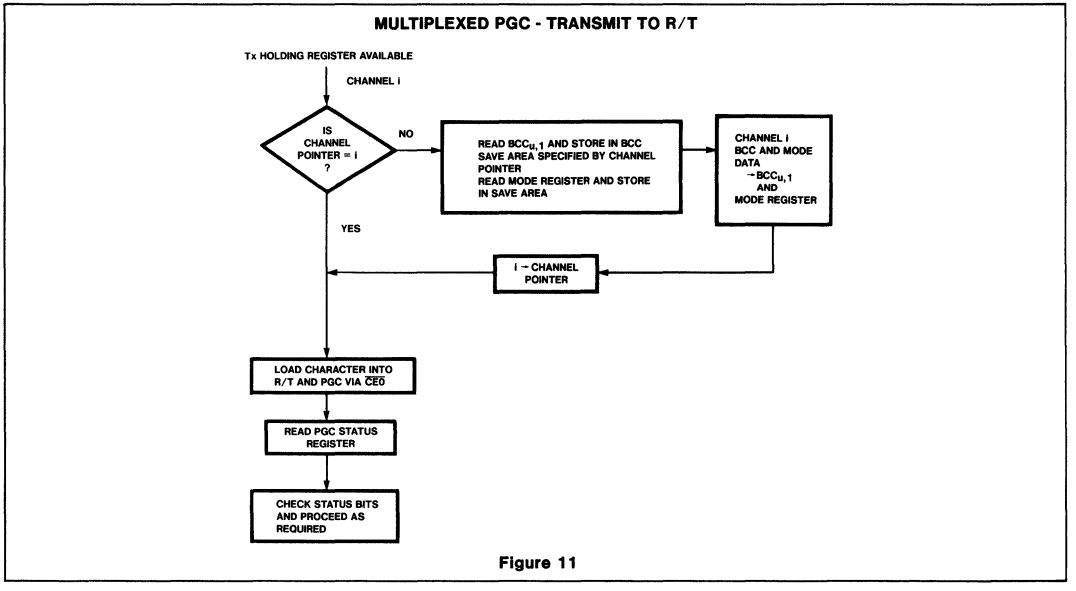


Figure 11

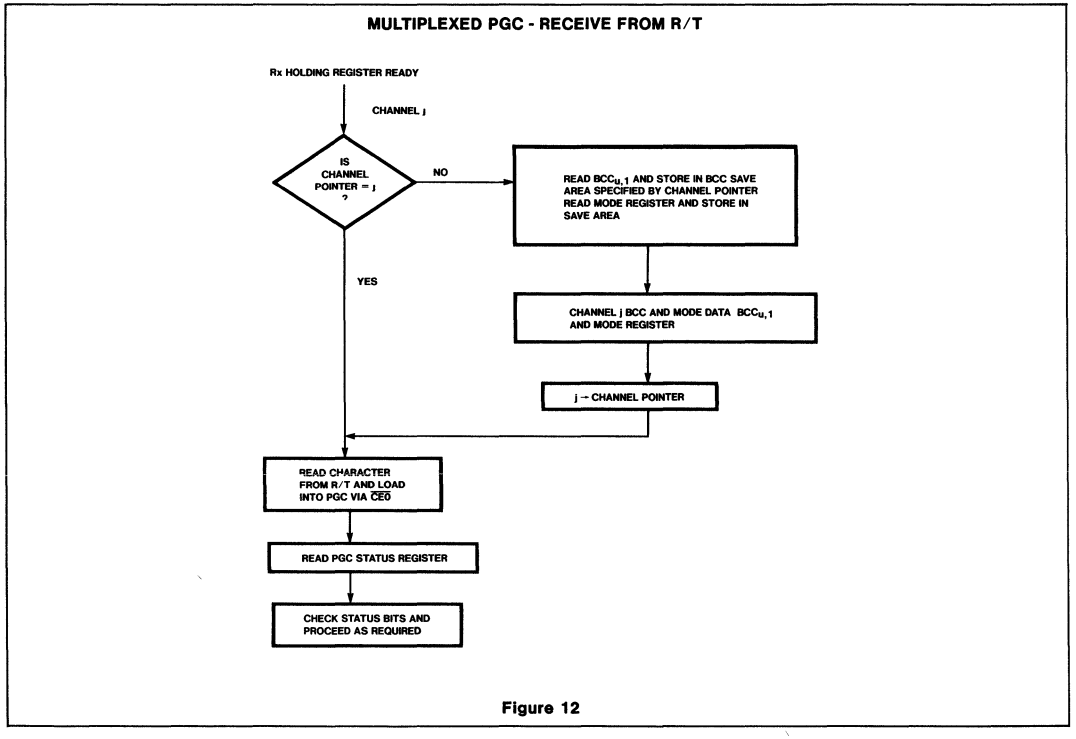
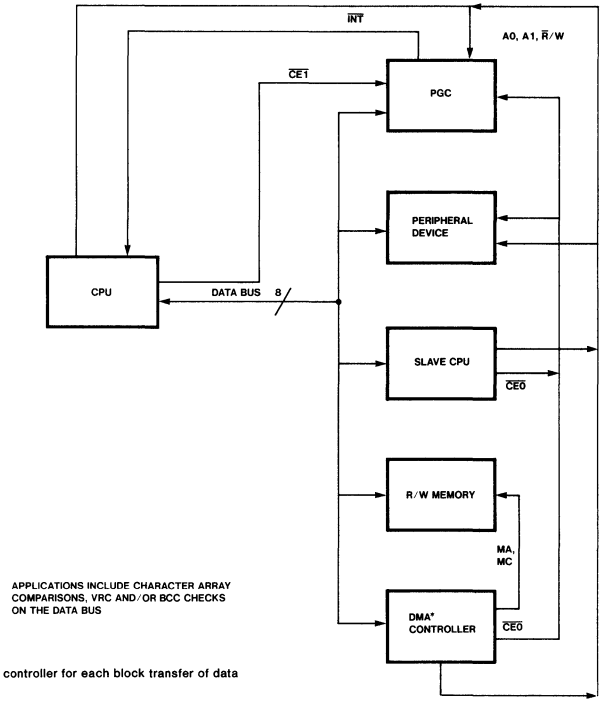


Figure 12

PGC DATA BUS MONITORING WITH DMA TRANSFERS



NOTE

*CPU initializes DMA controller for each block transfer of data

Figure 13

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	-65 to +150	°C
All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation sections of this specification is not implied

2 For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and thermal resistance of 80°C/W junction to ambient (ceramic package) or 137°C/W (plastic package)

3 This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge However, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low				0.8	
V_{IH}	High		2.0			
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.2mA		0.25	0.45	
V_{OH}	High	I_{OH} = −400μA	2.4	2.8		
I_{IL}	Input load current	V_{IN} = 0 to 5.5V			10	μA
	Output leakage current					μA
I_{LD}	Data bus	V_{OUT} = 4.0V			10	
I_{LO}	Open drain	V_{OUT} = 4.0V			10	
I_{CC}	Power supply current			45	75	mA

AC CHARACTERISTICS T_A = 0° to +70°C, V_{CC} = 5V ± 5%[1, 2, 3]

PARAMETER		LIMITS		UNIT
		Min	Max	
t_{CE}	Chip enable pulse width	250		ns
t_{CED}	Chip enable period D	1750		ns
t_{CEC}[4]	Chip enable period C	1750		ns
t_{AS}	Address setup	10		ns
t_{AH}	Address hold	10		ns
t_{CS}	Control setup	10		ns
t_{CH}	Control hold	10		ns
t_{DS}[5]	Data setup	150		ns
t_{DH}	Data hold	10		ns
t_{DD}[6]	Data delay time for read		200	ns
t_{DF}[6]	Data bus floating time for read		100	ns
t_{INTL}[7]	Interrupt low delay		1600	ns
t_{INTH}[7]	Interrupt high delay		600	ns

NOTES

1. Parameters are valid over operating temperature range unless otherwise specified.
2. All voltage measurements are referenced to ground. All time measurements are at 50% level for inputs and at the 0.8V or 2.0V level for outputs. Input levels for testing are 0.45V and 2.4V.
3. Typical values are at +25°C, typical supply voltages and typical processing parameters.
4. t_{CEC} = 600ns during PGC initialization when no BCC accumulation is in progress.
5. t_{DS} = 50ns whenever $\overline{CE0}$ is used.
6. Test conditions: C_L = 150 pF.
7. $\overline{INT}$ is an open drain output.

PGC TIMING

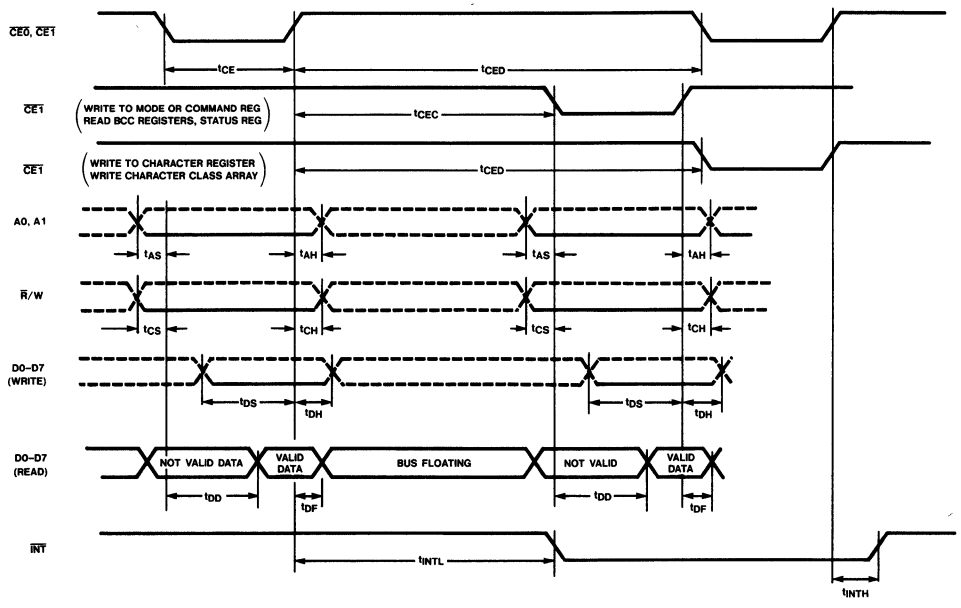


Figure 14

ENHANCED PROGRAMMABLE COMMUNICATIONS INTERFACE (EPCI) SC2661

DESCRIPTION

The Signetics 2661 EPCI is a universal synchronous/asynchronous data communications controller chip that is an enhanced pin compatible version of the 2651. It interfaces directly to most 8-bit microprocessors and may be used in a polled or interrupt driven system environment. The 2661 accepts programmed instructions from the microprocessor while supporting many serial data communications disciplines—synchronous and asynchronous—in the full or half-duplex mode. Special support for BISYNC is provided.

The EPCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The 2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the EPCI (A, B, C) has a different set of baud rates.

The EPCI is constructed using Signetics n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

FEATURES

- **Synchronous operation**
  - **5 to 8-bit characters plus parity**
  - **Single or double SYN operation**
  - **Internal or external character synchronization**
  - **Transparent or non-transparent mode**
  - **Transparent mode DLE stuffing (Tx) and detection (Rx)**
  - **Automatic SYN or DLE-SYN insertion**
  - **SYN, DLE and DLE-SYN stripping**
  - **Odd, even, or no parity**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 1M bps (1X clock)**
- **Asynchronous operation**
  - **5 to 8-bit characters plus parity**
  - **1, 1½ or 2 stop bits transmitted**
  - **Odd, even, or no parity**
  - **Parity, overrun and framing error detection**
  - **Line break detection and generation**
  - **False start bit detection**
  - **Automatic serial echo mode (echoplex)**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 1M bps (1X clock)**
    dc to 62.5K bps (16X clock)
    dc to 15.625K bps (64X clock)

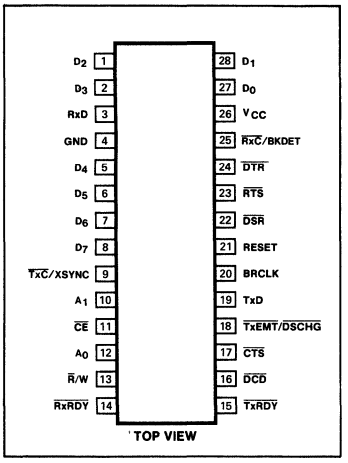
OTHER FEATURES

- **Internal or external baud rate clock**
- **3 baud rate sets**
- **16 internal rates for each set**
- **Double buffered transmitter and receiver**
- **Dynamic character length switching**
- **Full or half duplex operation**
- **Fully compatible with 2650 CPU**
- **TTL compatible inputs and outputs**
- **RxC and TxC pins are short circuit protected**
- **3 open drain MOS outputs can be wire-ORed**
- **Single 5V power supply**
- **No system clock required**
- **28-pin dual in-line package**

APPLICATIONS

- **Intelligent terminals**
- **Network processors**
- **Front end processors**
- **Remote data concentrators**
- **Computer to computer links**
- **Serial peripherals**
- **BISYNC adaptors**

PIN CONFIGURATION



ORDERING CODE

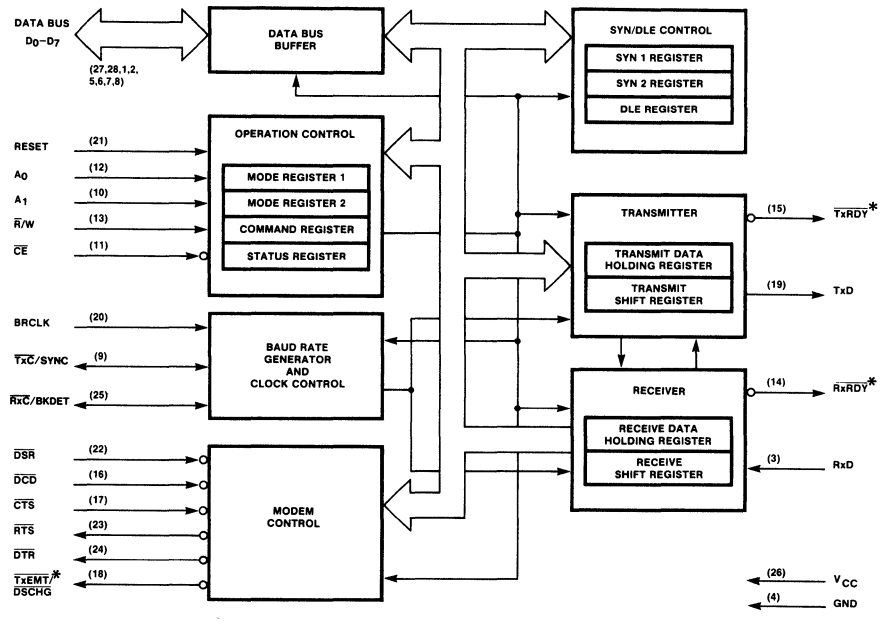
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%, T_A = 0°C to 70°C	
Ceramic DIP	SC2661ACSI28 SC2661BCSI28 SC2661CCSI28	See table 1 for baud rates
Plastic DIP	SC2661ACSN28 SC2661BCSN28 SC2661CCSN28	See table 1 for baud rates

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
27,28,1, 2,5-8	D_0-D_7	8-bit data bus	I/O
21	RESET	Reset	I
12,10	A_0-A_1	Internal register select lines	I
13	$\overline{R}/W$	Read or write command	I
11	$\overline{CE}$	Chip enable input	I
22	$\overline{DSR}$	Data set ready	I
24	$\overline{DTR}$	Data terminal ready	O
23	$\overline{RTS}$	Request to send	O
17	$\overline{CTS}$	Clear to send	I
16	$\overline{DCD}$	Data carrier detected	I
18	$\overline{TxEMT}/\overline{DSCHG}$	Transmitter empty or data set change	O
9	$\overline{TxC}$/XSYNC	Transmitter clock/external SYNC	I/O
25	$\overline{RxC}$/BKDET	Receiver clock/break detect	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	$\overline{TxRDY}$	Transmitter ready	O
14	$\overline{RxRDY}$	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5V supply	I
4	GND	Ground	I

ENHANCED PROGRAMMABLE COMMUNICATIONS INTERFACE (EPCI) SC2661

BLOCK DIAGRAM



NOTE
* Open drain output pin

BLOCK DIAGRAM

The EPCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register. Details of register addressing and protocol are presented in the EPCI programming section of this data sheet.

Table 1 BAUD RATE GENERATOR CHARACTERISTICS SC2661A (BRCLK = 4.9152MHz)

MR23–20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	-	6144
0001	75	1.2	-	4096
0010	110	1.7598	−0.01	2793
0011	134.5	2.152	-	2284
0100	150	2.4	-	2048
0101	200	3.2	-	1536
0110	300	4.8	-	1024
0111	600	9.6	-	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	-	256
1010	1800	28.7438	−0.19	171
1011	2000	31.9168	−0.26	154
1100	2400	38.4	-	128
1101	4800	76.8	-	64
1110	9600	153.6	-	32
1111	19200	307.2	-	16

Timing

The EPCI contains a baud rate generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. See table 1.

Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

Table 1 BAUD RATE GENERATOR CHRACTERISTICS (Cont'd)

SC2661B (BRCLK = 4.9152MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	-	6144
0010	75	1.2	-	4096
0011	110	1.7598	−0.01	2793
0100	134.5	2.152	-	2284
0101	150	2.4	-	2048
0110	300	4.8	-	1024
0111	600	9.6	-	512
1000	1200	19.2	-	256
1001	1800	28.7438	−0.19	171
1010	2000	31.9168	−0.26	154
1011	2400	38.4	-	128
1100	4800	76.8	-	64
1101	9600	153.6	-	32
1110	19200	307.2	-	16
1111	38400	614.4	-	8

SC2661C (BRCLK = 5.0688MHz)

MR23-20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	-	6336
0001	75	1.2	-	4224
0010	110	1.76	-	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	-	2112
0101	300	4.8	-	1056
0110	600	9.6	-	528
0111	1200	19.2	-	264
1000	1800	28.8	-	176
1001	2000	32.081	0.253	158
1010	2400	38.4	-	132
1011	3600	57.6	-	88
1100	4800	76.8	-	66
1101	7200	115.2	-	44
1110	9600	153.6	-	33
1111	19200	316.8	3.125	16

NOTE
16X clock is used in asynchronous mode In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC

Table 2 CPU-RELATED SIGNALS

PIN NAME	PIN NO.	INPUT/ OUTPUT	FUNCTION
V_{CC}	26	I	+5V supply input
GND	4	I	Ground
RESET	21	I	A high on this input performs a master reset on the 2661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words.
A_1-A_0	10,12	I	Address lines used to select internal EPCI registers.
$\overline{R}/W$	13	I	Read command when low, write command when high.
$\overline{CE}$	11	I	Chip enable command. When low, indicates that control and data lines to the EPCI are valid and that the operation specified by the $\overline{R}/W$, A_1 and A_0 inputs should be performed. When high, places the D_0-D_7 lines in the three-state condition.
D_7-D_0	8,7,6,5, 2,1,28,17	I/O	8-bit, three-state data bus used to transfer commands, data and status between EPCI and the CPU. D_0 is the least significant bit; D_7 the most significant bit.
$\overline{TxRDY}$	15	O	This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$	14	O	This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT}$/ $\overline{DSCHG}$	18	O	This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the status register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU.

OPERATION

The functional operation of the 2661 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the EPCI programming section of the data sheet.

After programming, the EPCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words.

Receiver

The 2661 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high to low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data are then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit SR5 set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the break detection timing diagram.

Table 3 DEVICE-RELATED SIGNALS

PIN NAME	PIN NO.	INPUT/ OUTPUT	FUNCTION
BRCLK	20	I	Clock input to the internal baud rate generator (see table 1). Not required if external receiver and transmitter clocks are used.
*$\overline{RxC}$/BKDET	25	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output pin.
*$\overline{TxC}$/XSYNC	9	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted. Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input.
RxD	3	I	Serial data input to the receiver. "Mark" is high, "space" is low.
TxD	19	O	Serial data output from the transmitter. "Mark" is high, "space" is low. Held in mark condition when the transmitter is disabled.
$\overline{DSR}$	22	I	General purpose input which can be used for data set ready or ring indicator condition. Its complement appears as status register bit SR7. Causes a low output on $\overline{TxEMT}$/$\overline{DSCHG}$ when its state changes if CR2 or CR0 = 1.
$\overline{DCD}$	16	I	Data carrier detect input. Must be low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a low output on $\overline{TxEMT}$/$\overline{DSCHG}$ when its state changes if CR2 or CR0 = 1. If $\overline{DCD}$ goes high while receiving, the RxC is internally inhibited.
$\overline{CTS}$	17	I	Clear to send input. Must be low in order for the transmitter to operate. If it goes high during transmission, the character in the transmit shift register will be transmitted before termination.
$\overline{DTR}$	24	O	General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready.
$\overline{RTS}$	23	O	General purpose output which is the complement of command register bit CR5. Normally used to indicate request to send. If the transmit shift register is not empty when CR5 is reset (1 to 0), then $\overline{RTS}$ will go high one TxC time after the last serial bit is transmitted.

NOTE
*$\overline{RxC}$ and $\overline{TxC}$ outputs have short circuit protection max. C_L = 100pF Outputs become open circuited upon detection of a zero pulled high or a one pulled low.

When the EPCI is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN(CR2). In this mode, as data are shifted into the receiver shift register a bit at a time, the contents of the register are compared to the contents of the SYN1 register If the two are not equal, the next bit is shifted in and the comparison is repeated. When the two registers match, the hunt mode is terminated and character assembly mode begins If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the EPCI returns to the hunt mode. (Note that the sequence SYN1-SYN1-SYN2 will not achieve synchronization.) When synchronization has been achieved, the EPCI continues to assemble characters and transfer them to the holding register, setting the RxRDY status bit and asserting the $\overline{RxRDY}$ output each time a character is transferred. The PE and OE status bits are set as appropriate. Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit. If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case.

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27-MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse. Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read. Refer to XSYNC timing diagram.

Transmitter

The EPCI is conditioned to transmit data when the $\overline{CTS}$ input is low and the TxEN command register bit is set. The 2661 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{TxRDY}$ output When the CPU writes a character into the transmit data holding register, these conditions are negated. Data are transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again Thus, one full character time of buffering is provided.

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first. It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the $\overline{TxEMT}/\overline{DSCHG}$ output and its corresponding status bit are asserted. Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the send break command bit (CR3) high.

In the synchronous mode, when the 2661 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted. No extra bits (other than parity, if commanded) are generated by the EPCI unless the CPU fails to send a new character to the EPCI by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the EPCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1-SYN2 doublets, or DLE-SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the transmit data holding register. If the SEND DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the THR.

EPCI PROGRAMMING

Prior to initiating data communications, the 2661 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The EPCI can be reconfigured at any time during program execution. A flowchart of the intialization process appears in figure 1.

The internal registers of the EPCI are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A_1 and A_0 inputs. The conditions necessary to address each register are shown in table 4.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions $A_1 = 0$, $A_0 = 1$, and

Table 4 2661 REGISTER ADDRESSING

$\overline{CE}$	A_1	A_0	$\overline{R}/W$	FUNCTION
1	X	X	X	Three-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode registers ½
0	1	0	1	Write mode registers ½
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE
See AC characteristics section for timing requirements

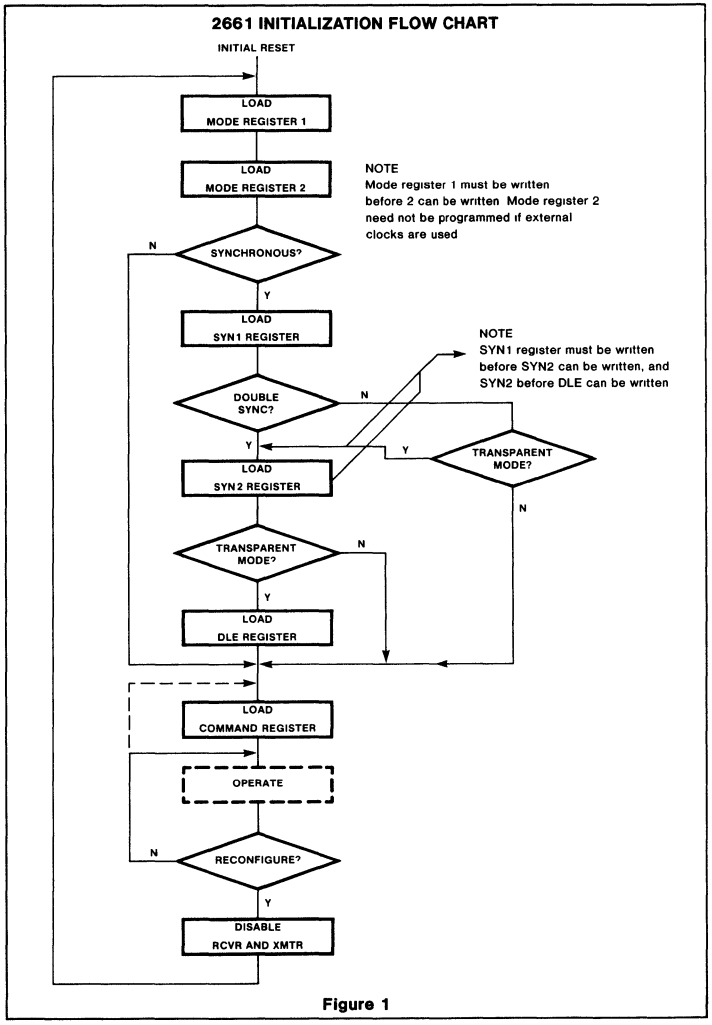


Figure 1

$\overline{R}/W$ = 1. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses mode register 1, and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 register and mode register 1 by a RESET input or by performing a read command register operation, but are unaffected by any other read or write operation.

The 2661 register formats are summarized in tables 5, 6, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the EPCI, while the command register controls the operation within this basic framework. The EPCI indicates its status in the status register. These registers are cleared when a RESET input is applied.

Mode Register 1 (MR1)

Table 5 illustrates Mode Register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies synchronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7 or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 1X baud rate is programmed, 1.5 stop bits defaults to 1 stop bits on transmit.) In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1-SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE-SYN1 is used for character fill and SYN detect, but the normal synchronization sequence is used to establish character sync. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also, DLE stripping and DLE detect (with MR14 = 0) are enabled.

The bits in the mode register affecting character assembly and disassembly (MR12-MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver; therefore in synchronous mode, changes should be made only in half duplex mode (RxEN = 1 or TxEN = 1, but not both simultaneously = 1). In asynchronous mode, character changes should be made when RxEN and TxEN=0 or when TxEN = 1 and the transmitter is marking in half duplex mode (RxEN = 0).

To effect assembly/disassembly of the next received/transmitted character, MR12-15 must be changed within n bit times of the active going state of $\overline{RxRDY}/\overline{TxRDY}$. Transparent and non-transparent mode changes (MR16) must occur within n-1 bit times of the character to be affected when the receiver or transmitter is active. (n = smaller of the new and old character lengths.)

Mode Register 2 (MR2)

Table 6 illustrates mode register 2. MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each EPCI version (−1, −2, −3). Version 1 and 2 specify a 4.9152 MHz TTL input at BRCLK (pin 20); version 3 specifies a 5.0688 MHz input which is identical to the Signetics 2651. MR23-20 are don't cares if external clocks are selected (MR25-MR24 = 0). The individual rates are given in table 1.

MR24-MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 9 and 25. Refer to table 6.

Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go high (inactive). If the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state

Table 5 MODE REGISTER 1 (MR 1)

MR17 MR16		MR15	MR14	MR13 MR12	MR11 MR10
Sync/Async		Parity Type	Parity Control	Character Length	Mode and Baud Rate Factor
Async: Stop Bit Length 00 = Invalid 01 = 1 stop bit 10 = 1½ stop bits 11 = 2 stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits	00 = Synchronous 1X rate 01 = Asynchronous 1X rate 10 = Asynchronous 16X rate 11 = Asynchronous 64X rate
Sync: Number of SYN char 0 = Double SYN 1 = Single SYN	**Sync: Transparency Control** 0 = Normal 1 = Transparent				

NOTE
Baud rate factor in asynchronous applies only if external clock is selected Factor is 16X if internal clock is selected Mode must be selected (MR11, MR10) in any case

1

Table 6 MODE REGISTER 2 (MR2)

MR27–MR24											MR23–MR20
	TxC	RxC	Pin 9	Pin 25		TxC	RxC	Pin 9	Pin 25	Mode	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	XSYNC[1]	RxC/TxC	sync	
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	async	
0010	I	E	1X	RxC	1010	I	E	XSYNC[1]	RxC	sync	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	async	See baud rates in table 1
0100	E	E	TxC	RxC	1100	E	E	XSYNC[1]	RxC/TxC	sync	
0101	E	I	TxC	16X	1101	E	I	TxC	BKDET	async	
0110	I	E	16X	RxC	1110	I	E	XSYNC[1]	RxC	sync	
0111	I	I	16X	16X	1111	I	I	16X	BKDET	async	

NOTES
1 When pin 9 is programmed as XSYNC input, SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled.
E = External clock
I = Internal clock (BRG)
1X and 16X are clock outputs

Table 7 COMMAND REGISTER (CR)

CR7 CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode	Request To Send	Reset Error	Sync/Async	Receive Control (RxEN)	Data Terminal Ready	Transmit Control (TxEN)
00 = Normal operation 01 = Async: Automatic echo mode Sync: SYN and/or DLE stripping mode 10 = Local loop back 11 = Remote loop back	0 = Force $\overline{RTS}$ output high one clock time after TxSR serialization 1 = Force $\overline{RTS}$ output low	0 = Normal 1 = Reset error flags in status register (FE, OE, PE/DLE detect)	**Async:** **Force break** 0 = Normal 1 = Force break	0 = Disable 1 = Enable	0 = Force $\overline{DTR}$ output high 1 = Force $\overline{DTR}$ output low	0 = Disable 1 = Enable
			Sync: **Send DLE** 0 = Normal 1 = Send DLE			

Table 8 STATUS REGISTER (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	Data Carrier Detect	FE/SYN Detect	Overrun	PE/DLE Detect	TxEMT/DSCHG	RxRDY	TxRDY
0 = $\overline{DSR}$ input is high 1 = $\overline{DSR}$ input is low	0 = $\overline{DCD}$ input is high 1 = $\overline{DCD}$ input is low	**Async:** 0 = Normal 1 = Framing Error	0 = Normal 1 = Overrun Error	**Async:** 0 = Normal 1 = Parity error	0 = Normal 1 = Change in $\overline{DSR}$, or $\overline{DCD}$, or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register empty
		Sync: 0 = Normal 1 = SYN detected		**Sync:** 0 = Normal 1 = Parity error or DLE received			

(high) while $\overline{TxRDY}$ and $\overline{TxEMT}$ will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. A 0 to 1 transition of CR2 will initiate start bit search (async) or hunt mode (sync).

Bits CR1 (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the transmit data holding register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the transmit data holding register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE—non-DLE character sequences.

Setting CR4 causes the error flags in the status register (SR3, SR4, and SR5) to be cleared. This is a one time command. There is no internal latch for this bit.

Table 9 SC2661 EPCI vs SC2651 PCI

FEATURE	EPCI	PCI
1. MR2 Bit 6, 7	Control pin 9, 25	Not used
2. DLE detect-SR3	SR3 = 0 for DLE-DLE, DLE-SYNC1	SR3 = 1 for DLE-DLE, DLE-SYNC1
3. Reset of SR3, DLE detect	Second character after DLE, or receiver disable, or CR4 = 1	Receiver disable, or CR4 = 1
4. Send DLE-CR3	One time command	Reset via CR3 on next $\overline{TxRDY}$
5. DLE stuffing in transparent mode	Automatic DLE stuffing when DLE is loaded except if CR3 = 1	None
6. SYNC1 stripping in double sync non-transparent mode	All SYNC1	First SYNC1 of pair
7. Baud rate versions	Three	One
8. Terminate ASYNC transmission (drop RTS)	Reset CR5 in response to $\overline{TxRDY}$ changing from 1 to 0	Reset CR0 when $\overline{TxEMT}$ goes from 1 to 0. Then reset CR5 when $\overline{TxEMT}$ goes from 0 to 1
9. Break detect	Pin 25[1]	FE and null character
10. Stop bit searched	One	Two
11. External jam sync	Pin 9[2]	No
12. Data bus timing	Improved over 2651	—
13. Data bus drivers	Sink 2.2mA	Sink 1.6mA
	Source 400μA	Source 100μA

NOTES
1. Internal BRG used for RxC.
2. Internal BRG used for TxC

When CR5 (RTS) is set, the $\overline{RTS}$ pin is forced low and the transmit serial logic is enabled. A 1 to 0 transition of CR5 will cause $\overline{RTS}$ to go high (inactive) one TxC time after the last serial bit has been transmitted (if the transmit shift register was not empty).

The EPCI can operate in one of four sub-modes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7-CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the mode and status register instructions.

In asynchronous mode, CR7-CR6 = 01 places the EPCI in the automatic echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ output = 1.
4. The $\overline{TxEMT}/\overline{DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7-CR6 = 01 places the EPCI in the automatic SYN/DLE stripping mode. The exact action taken depends on the setting of bits MR17 and MR16:

1. In the non-transparent, single SYN mode (MR17-MR16 = 10), characters in the data stream matching SYN1 are not transferred to the receive data holding register (RHR).
2. In the non-transparent, double SYN mode (MR17-MR16 = 00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR.
3. In transparent mode (MR16 = 1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that automatic stripping mode does not affect the setting of the DLE detect and SYN detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In local loop back mode (CR7-CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the local loop back mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the EPCI.

The second diagnostic mode is the remote loop back mode (CR7-CR6 = 11). In this mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data are sent to the local CPU, but the error status conditions (PE, OE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT}/\overline{DSCHG}$ outputs are held high.
5. CR1 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the status register (as shown in table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the transmitter ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the transmit data holding register has been loaded by the CPU and the data has not been transferred to the transmit shift register. If set equal to 1, it indicates that the holding register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the $\overline{TxRDY}$ output pin is low. In

the automatic echo and remote loop back modes, the output is held high.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to zero, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{RxRDY}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs (when CR2 or CR0 = 1) or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The DSCHG condition is enabled when TxEN = 1 or RxEN = 1. It is cleared when the status register is read by the CPU. If the status register is read twice and SR2 = 1 while SR6 and SR7 remain unchanged, then a TxEMT condition exists. When SR2 is set, the $\overline{TxEMT}/\overline{DSCHG}$ output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching DLE register was received and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into RHR, when the receiver is disabled, or by a reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not read by the CPU at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled or by the reset error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by a stop bit, i.e., only the first stop bit is checked. If RHR = 0 when SR5 = 1, a break condition is present. In synchronous non-transparent mode (MR16 = 0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1-SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1-SYN2) and, after synchronization has been achieved, when a DLE-SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, or when the status register is read by the CPU in the synchronous mode.

SR6 and SR7 reflect the conditions of the $\overline{DCD}$ and $\overline{DSR}$ inputs respectively. A low input sets its corresponding status bit, and a high input clears it.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.5 to +6.0	V

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% [4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low				0.8	
V_{IH}	High		2.0			
	Output voltage					V
V_{OL}	Low	I_{OL} = 2.2mA			0.4	
V_{OH}[7]	High	I_{OH} = −400μA	2.4			
I_{IL}	Input leakage current	V_{IN} = 0 to 5.5 V			10	μA
	3-state output leakage current					μA
I_{LH}	Data bus high	V_O = 4.0V			10	
I_{LL}	Data bus low	V_O = 0.45V			10	
I_{CC}	Power supply current				150	mA

CAPACITANCE T_A = 25°C, V_{CC} = 0V

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Capacitance					pF
C_{IN}	Input				20	
C_{OUT}	Output	fc = 1MHz			20	
$C_{I/O}$	Input/Output	Unmeasured pins tied to ground			20	

Notes on following page

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% [4,5,6]

	PARAMETER	TEST CONDITIONS	Min	Typ	Max	UNIT
	Pulse width					ns
t_{RES}	Reset		1000			
t_{CE}	Chip enable		250			
	Setup and hold time					ns
t_{AS}	Address setup		10			
t_{AH}	Address hold		10			
t_{CS}	$\overline{R}$/W control setup		10			
t_{CH}	$\overline{R}$/W control hold		10			
t_{DS}	Data setup for write		150			
t_{DH}	Data hold for write		0			
t_{RXS}	Rx data setup		300			
t_{RXH}	Rx data hold		350			
t_{DD}	Data delay time for read	C_L = 150pF			200	ns
t_{DF}	Data bus floating time for read	C_L = 150pF			100	
t_{CED}	CE to CE delay		600			
	Input clock frequency					MHz
f_{BRG}	Baud rate generator (2661A,B)		1.0	4.9152	4.9202	
f_{BRG}	Baud rate generator (2661C)		1.0	5.0688	5.0738	
$f_{R/T}$ [10]	$\overline{TxC}$ or $\overline{RxC}$		dc		1.0	
	Clock width					ns
t_{BRH} [9]	Baud rate high (2661A,B)		75			
t_{BRH} [9]	Baud rate high (2661C)		70			
t_{BRL} [9]	Baud rate low (2661A,B)		75			
t_{BRL} [9]	Baud rate low (2661C)		70			
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ high		480			
$t_{R/TL}$ [10]	$\overline{TxC}$ or $\overline{RxC}$ low		480			
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$	C_L = 150pF			650	ns
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output [8]	C_L = 150pF		0		

1 Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied

2 For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient (IQ ceramic package)

3 This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima

4 Parameters are valid over operating temperature range unless otherwise specified.

5. All voltage measurements are referenced to ground All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0 8V and 2 0V for outputs Input levels swing between 0 4V and 2.4V, with a transition time of 20 ns maximum

6 Typical values are at +20°C, typical supply voltages and typical processing parameters

7 $\overline{TxRDY}$, $\overline{RxRDY}$ and $\overline{TxEMT/DSCHG}$ outputs are open drain

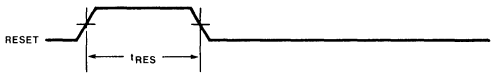
8. Parameter applies when internal transmitter clock is used

9 Under test conditions of 5.0688 MHz f_{BRG} (2661C) and 4 9152 MHz f_{BRG} (2661A,B), t_{BRH} and t_{BRL} measured at V_{IH} and V_{IL} respectively

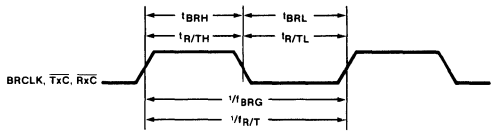
10 In asynchronous local loopback mode, using 1X clock, the following parameters apply:
$f_{R/T}$ = 0 83 MHz max
$t_{R/TL}$ = 700 ns min

TIMING DIAGRAMS

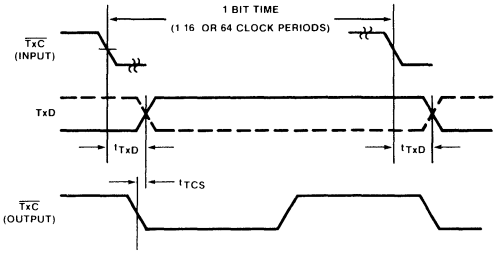
RESET



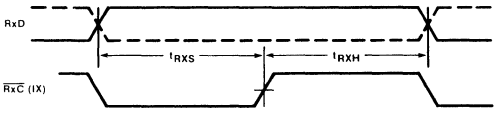
CLOCK



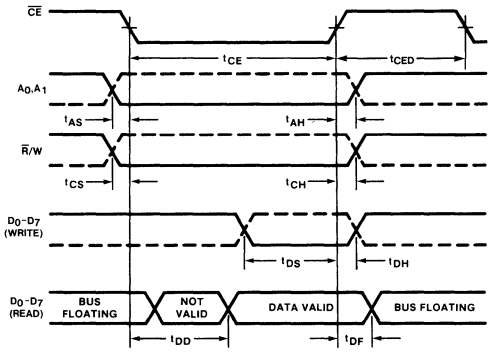
TRANSMIT



RECEIVE

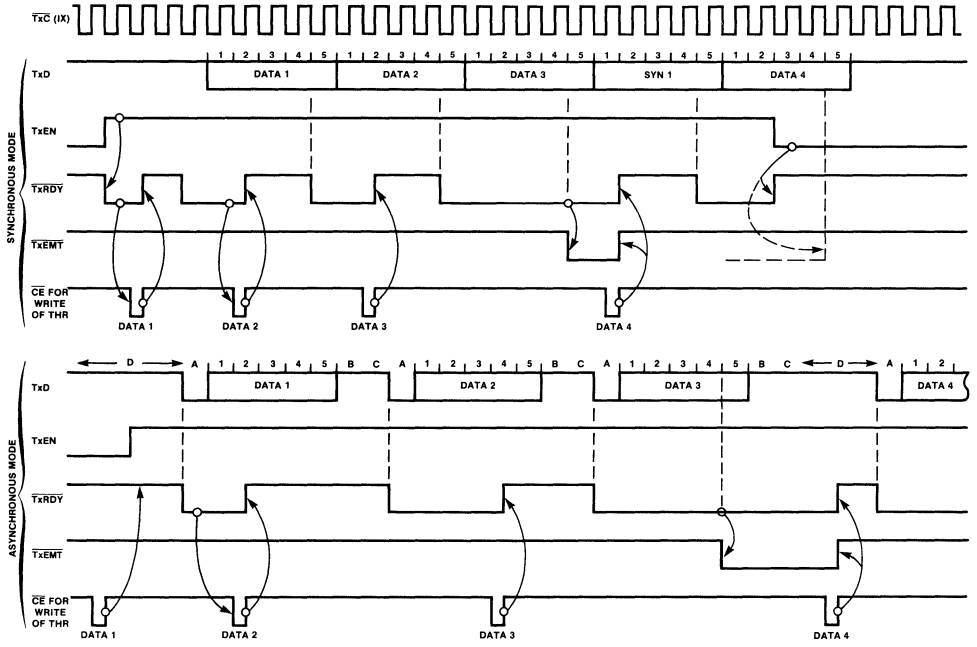


READ AND WRITE



TIMING DIAGRAMS (Cont'd)

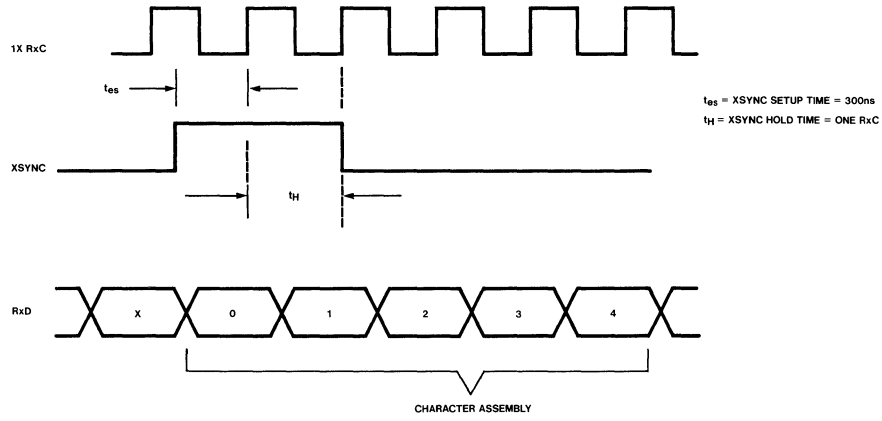
TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



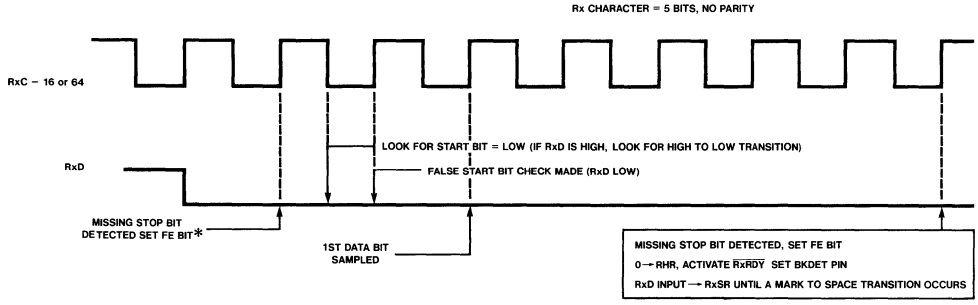
NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or, if parity is enabled, at the beginning of the parity bit

TIMING DIAGRAMS (Cont'd)

EXTERNAL SYNCHRONIZATION WITH XSYNC



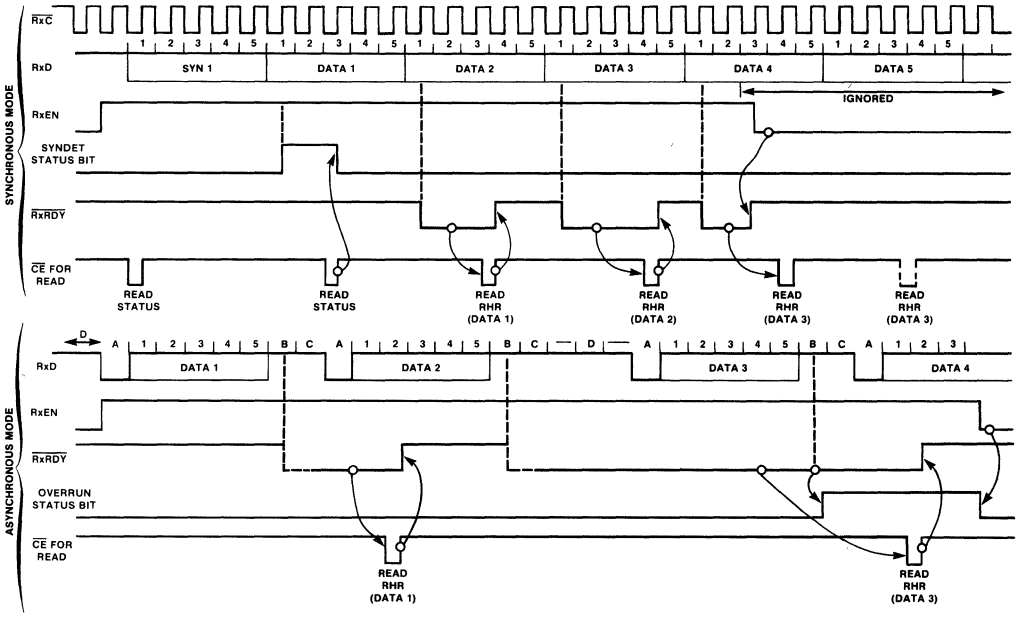
BREAK DETECTION TIMING



NOTE
* If the stop bit is present, the start bit search will commence immediately

TIMING DIAGRAMS (Cont'd)

RxRDY (Shown for 5-bit characters, no parity, 2 stops bits [in asynchronous mode])

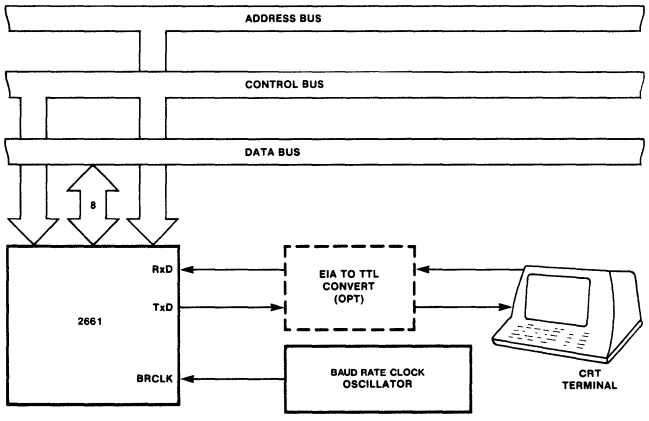


NOTES
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
Only one stop bit is detected

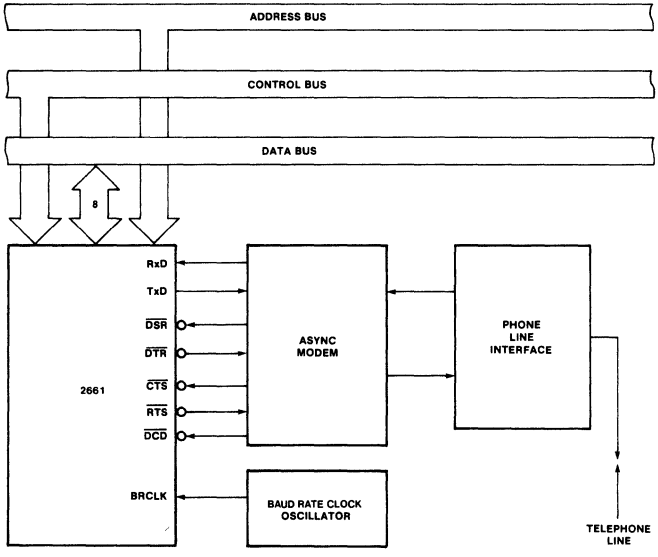
1

TYPICAL APPLICATIONS

ASYNCHRONOUS INTERFACE TO CRT TERMINAL

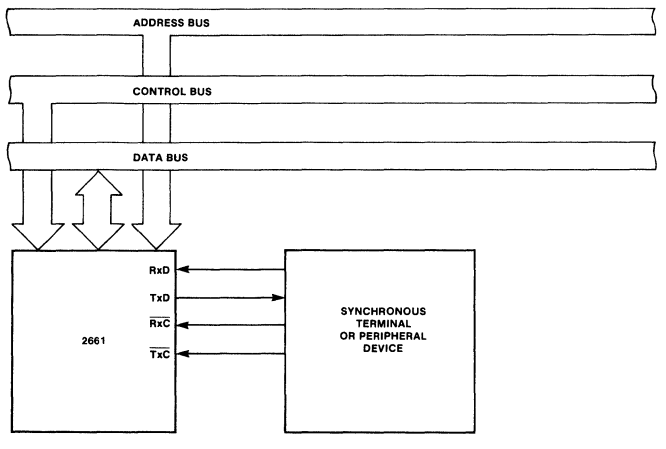


ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

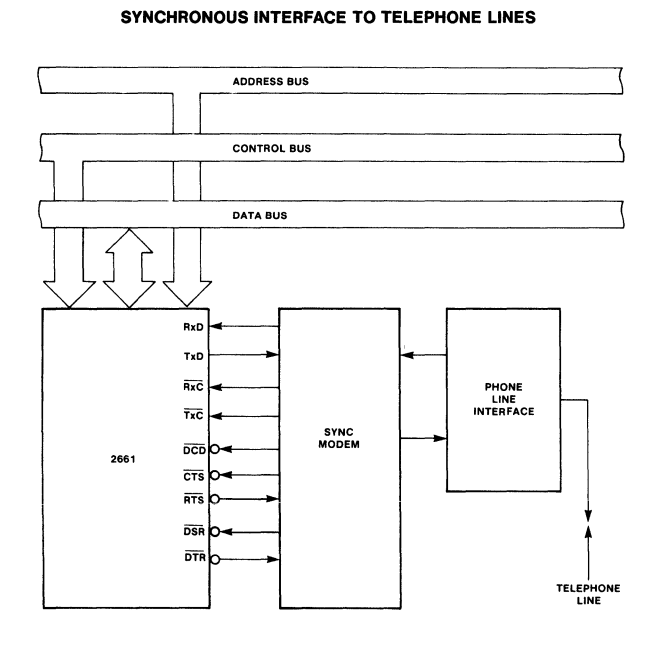


TYPICAL APPLICATIONS (Cont'd)

SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SC2681 SERIES

Preview

DESCRIPTION

The Signetics SC2681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single chip MOS-LSI communications device that provides two independent full-duplex asynchronous receiver/transmitter channels in a single package. It interfaces directly with microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of eighteen fixed baud rates, a 16x clock derived from a programmable counter/timer, or an external 1x or 16x clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a flow control capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

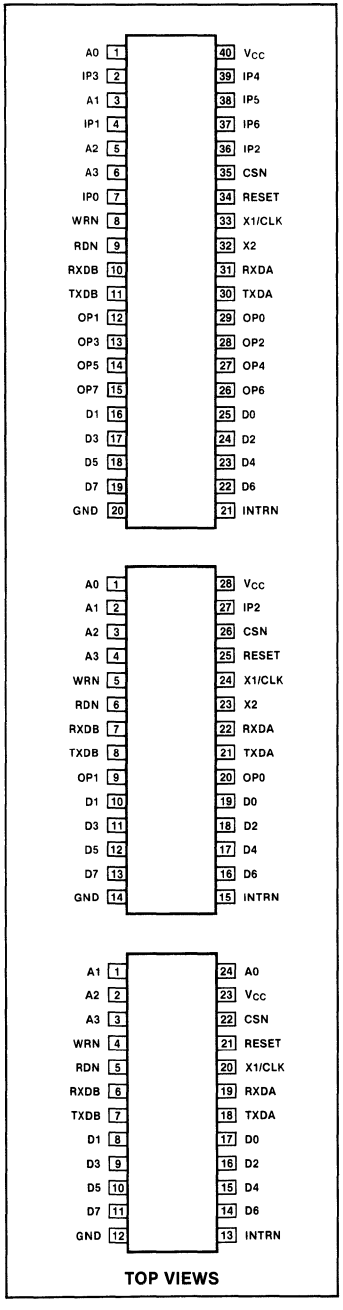
Also provided on the SC2681 are a multipurpose 7-bit input port and a multipurpose 8-bit output port. These can be used as general purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SC2681 is available in three package versions to satisfy various system requirements: 40-pin and 28-pin, both 0.6″ wide DIPs, and a compact 24-pin, 0.4″ wide, DIP.

FEATURES

- **Dual full-duplex asynchronous receiver/transmiter**
- **Quadruple buffered receiver data registers**
- **Programmable data format**
  - **—5 to 8 data bits plus parity**
  - **—Odd, even, no parity or force parity**
  - **—1, 1.5 or 2 stop bits programmable in 1/16 bit increments**
- **Programmable baud rate for each receiver and transmiter selectable from:**
  - **—18 fixed rates: 50 to 38.4K baud**
  - **—One user defined rate derived from programmable timer/counter**
  - **—External 1x or 16x clock**
- **Parity, framing, and overrun error detection**
- **False start bit detection**
- **Line break detection and generation**
- **Programmable channel mode**
  - **—Normal (full duplex)**
  - **—Automatic echo**
  - **—Local loopback**
  - **—Remote loopback**
- **Multi-function programmable 16-bit counter/timer**
- **Multi-function 7-bit input port**
  - **—Can serve as clock or control inputs**
  - **—Change of state detection on four inputs**
- **Multi-function 8-bit output port**
  - **—Individual bit set/reset capability**
  - **—Outputs can be programmed to be status/interrupt signals**
- **Versatile interrupt system**
  - **—Single interrupt output with eight maskable interrupting conditions**
  - **—Output port can be configured to provide a total of up to six separate wire-OR'able interrupt outputs**
- **Maximum data transfer: 1X — 1MB/sec, 16X — 125KB/sec**
- **Automatic wake-up mode for multidrop applications**
- **Start-end break interrupt/status**
- **Detects break which originates in the middle of a character**
- **On-chip crystal oscillator**
- **TTL compatible**
- **Single +5V power supply**

PIN CONFIGURATION



TOP VIEWS

ORDERING CODE

PACKAGES	V_{CC} = 5V ±5%, T_A = 0°C to 70°C		
	24 Pin[1]	28 Pin[2]	40 Pin[2]
Ceramic DIP	SC2681CSI24	SC2681CSI28	SC2681CSI40
Plastic DIP	SC2681CSN24	SC2681CSN28	SC2681CSN40

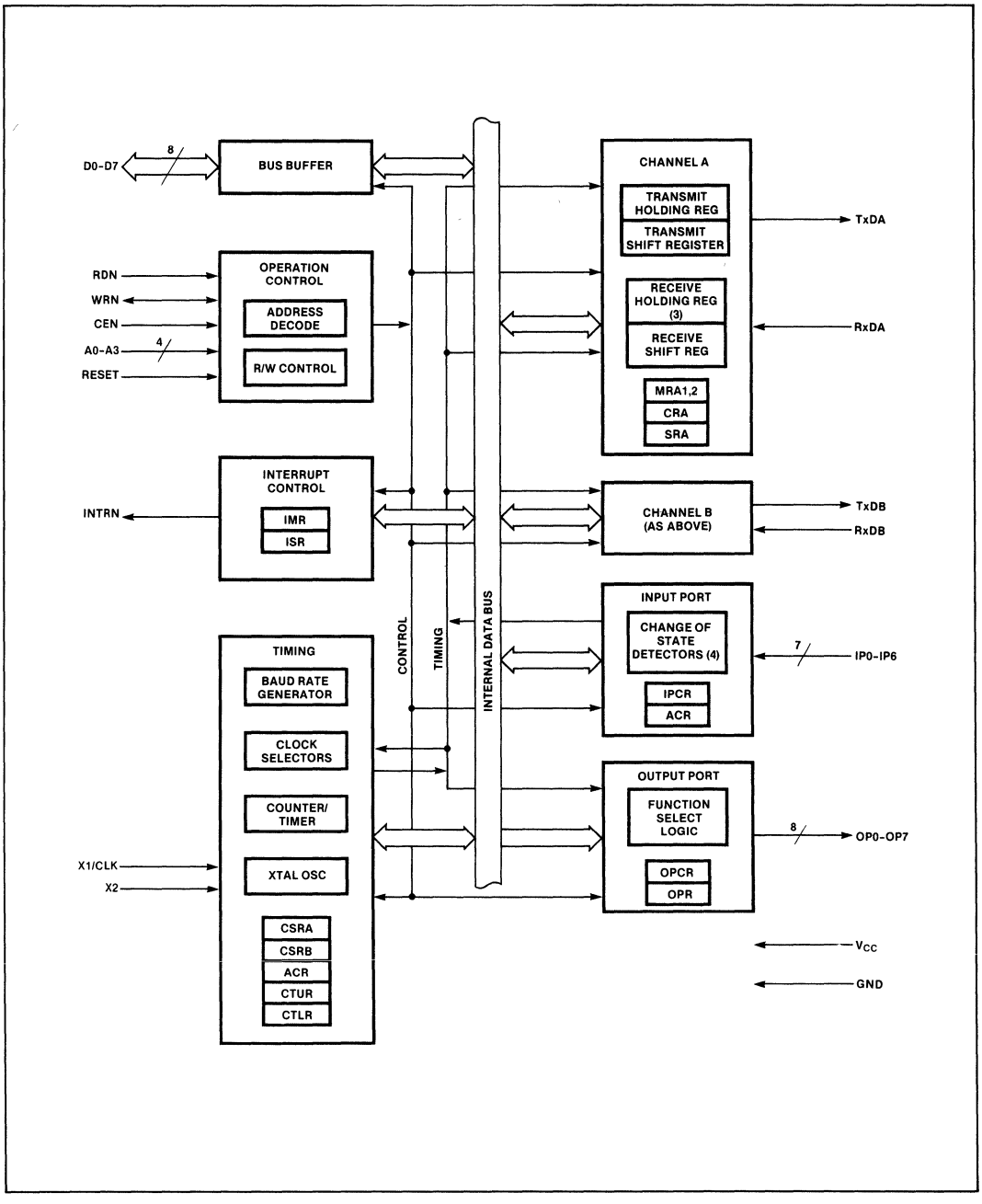
[1] 400 mil wide DIP

[2] 600 mil wide DIP

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SC2681 SERIES

Preview

BLOCK DIAGRAM



Preview

PIN DESIGNATION

MNEMONIC	APPLICABLE			TYPE	NAME AND FUNCTION
	40	28	24		
D0-D7	X	X	X	I/O	**Data Bus:** Bidirectional 3-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	I	**Chip Enable:** Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When high, places the D0-D7 lines in the 3-state condition.
WRN	X	X	X	I	**Write Strobe:** When low and CEN is also low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	I	**Read Strobe:** When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	X	I	**Reset:** A high level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state.
INTRN	X	X	X	O	**Interrupt Request:** Active low, open drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times.
X2	X	X		I	**Crystal 2:** Connection for other side of the crystal. Should be open if crystal is not used.
RxDA	X	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
RxDB	X	X	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
TxDA	X	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
TxDB	X	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
OP0	X	X		O	**Output 0:** General purpose output, or channel A request to send (RTSAN, active low). Can be deactivated on receive or transmit.
OP1	X	X		O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active low). Can be deactivated on receive or transmit.
OP2	X	X		O	**Output 2:** General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	X			O	**Output 3:** General purpose output, or open drain, active low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	X			O	**Output 4:** General purpose output, or channel A open drain, active low, RxRDYA/FFULLA output.
OP5	X			O	**Output 5:** General purpose output, or channel B open drain, active low, RxRDYB/FFULLB output.
OP6	X			O	**Output 6:** General purpose output, or channel A open drain, active low, TxRDYA output.
OP7	X			O	**Output 7:** General purpose output, or channel B open drain, active low, TxRDYB output.
IP0	X			I	**Input 0:** General purpose input, or channel A clear to send active low input (CTSAN).
IP1	X			I	**Input 1:** General purpose input, or channel B clear to send active low input (CTSBN).
IP2	X	X		I	**Input 2:** General purpose input, or counter/timer external clock input.
IP3	X			I	**Input 3:** General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.

Preview

PIN DESIGNATION (Continued)

MNEMONIC	APPLICABLE			TYPE	NAME AND FUNCTION
	40	28	24		
IP4	X			I	**Input 4:** General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X			I	**Input 5:** General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X			I	**Input 6:** General purpose input or channel B receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X	X	I	**Power Supply:** +5V supply input
GND	X	X	X	I	**Ground**

BLOCK DIAGRAM

The 2681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications channels A and B, input port and output port. Refer to the block diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active low interrupt output (INTRN) is provided which is activated upon the occurence of any of eight internal events. Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitters, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the baud rate generator (BRG), the counter/timer, and other internal circuits. A clock signal within the limits specified in the specifications section of this data sheet must always be supplied to the DUART.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. The clock outputs from the BRG are at 16X the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or an external timing signal.

The counter/timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the 2681 comprises a full duplex asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched 7-bit port can be read by the CPU by performing a read operation at address D_{16}. A high input results in a logic 1 while a low input results in a logic 0. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1, and IP0. A high-to-low or low-to-high transition of these inputs lasting longer than 25-50μs will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt to the CPU.

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Output Port

The 8-bit multi-purpose output port can be used as a general purpose output port, in which case the outputs are the complements of the output port register (OPR). OPR[n] = 1 results in OP[n] = low and vice-versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address E_{16} with the accompanying data specifying the bits to be set (1 = set, 0 = no change). Likewise, a bit is reset by a write at address F_{16} with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can be also individually assigned specific functions by appropriate programming of the channel A mode registers (MR1A, MR2A), the channel B mode registers (MR1B, MR2B), and the output port configuration register (OPCR).

OPERATION

Transmitter

The 2681 is conditioned to transmit data when the transmitter is enabled through the command register. The 2681 indicates to the CPU that it is ready to accept a character by setting the TxRDY bit in the status register. This condition can be programmed to generate an interrupt request at OP6 or OP7 and INTRN. When a character is loaded into the transmit holding register (THR), the above conditions are negated. Data is transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character. The TxRDY conditions are then asserted again which means one full character time of buffering is provided. Characters cannot be loaded into the THR while the transmitter is disabled.

The transmitter converts the parallel data from the CPU to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the THR, the TxD output remains high and the TxEMT bit in the status register (SR) will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the THR. If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out. The transmitter can be forced to send a continuous low condition by issuing a send break command.

The transmitter can be reset through a software command. If it is reset, operation ceases immediately and the transmitter must be enabled through the command register before resuming operation. If CTS operation is enabled, the CTSN input must be low in order for the character to be transmitted. if it goes high in the middle of a transmission, the character in the shift register is transmitted and TxDA then remains in the marking state until CTSN goes low. The transmitter can also control the deactivation of the RTSN output. If programmed, the RTSN output will be reset one bit time after the character in the transmit shift register and transmit holding register (if any) are completely transmitted, if the transmitter has been disabled.

Receiver

The 2681 is conditioned to receive data when enabled through the command register. The receiver looks for a high to low (mark to space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled each 16X clock for 7-1/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled high, the start bit is invalid and the search for a valid start bit begins again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the receive holding register (RHR) and the RxRDY bit in the SR is set to a 1. This condition can be programmed to generate an interrupt at OP4 or OP5 and INTRN. If the character length is less than eight bits, the most significant unused bits in the RHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (framing error) and RxD remains low for one half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

The parity error, framing error, overrun error and received break state (if any) are strobed into the SR at the received character boundary, before the RxRDY status bit is set. If a break condition is detected (RxD is low for the entire character including the stop bit), a character consisting of all zeros will be loaded into the RHR and the received break bit in the SR is set to 1 The RxD input must return to a high condition for at least one-half bit time before a search for the next start bit begins.

The RHR consists of a first-in-first-out (FIFO) stack with a capacity of three characters. Data is loaded from the receive shift register into the topmost empty position of the FIFO. The RxRDY bit in the status register is set whenever one or more characters are available to be read, and a FFULL status bit is set if all three stack positions are filled with data. Either of these bits can be selected to cause an interrupt. A read of the RHR outputs the data at the top of the FIFO. After the read cycle, the data FIFO and its associated status bits (see below) are 'popped' thus emptying a FIFO position for new data.

In addition to the data word, three status bits (parity error, framing error, and received break) are also appended to each data character in the FIFO (overrun is not). Status can be provided in two ways, as programmed by the error mode control bit in the mode register. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these three bits is the logical OR of the status for all characters coming to the top of the FIFO since the last 'reset error' command was issued. In either mode reading the SR does not affect the FIFO. The FIFO is 'popped' only when the RHR is read. Therefore the status register should be read prior to reading the FIFO.

If the FIFO is full when a new character is received, that character is held in the receive shift register until a FIFO position is available. If an additional character is received while this state exits, the contents of the FIFO are not affected: the character previously in the shift register is lost and the overrun error status bit (SR[4]) will be set upon receipt of the start bit of the new (overruning) character.

The receiver can control the deactivation of RTS. If programmed to operate in this mode, the RTSN output will be negated when a valid start bit was received and the FIFO is full. When a FIFO position becomes available, the RTSN output will be re-asserted automatically. This feature can be used to prevent an overrun, in the

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receiver, by connecting the RTSN output to the CTSN input of the transmitting device.

If the receiver is disabled, the FIFO characters can be read. However, no additional characters can be received until the receiver is enabled again. If the receiver is reset, the FIFO and all of the receiver status, and the corresponding output ports and interrupt are reset. No additional characters can be received until the receiver is enabled again.

Multidrop Mode

The DUART is equipped with a wake up mode used for multidrop applications. This mode is selected by programming bits MR1A[4:3] or MR1B[4:3] to '11' for channels A and B respectively. In this mode of operation, a 'master' station transmits an address character followed by data characters for the addressed 'slave' station. The slave stations, with receivers that are normally disabled, examine the received data stream and 'wake-up' the CPU (by setting RxRDY) only upon receipt of an address character. The CPU compares the received address to its station address and enables the receiver if it wishes to receive the subsequent data characters. Upon receipt of another address character, the CPU may disable the receiver to initiate the process again.

A transmitted character consists of a start bit, the programmed number of data bits, an address/data (A/D) bit, and the programmed number of stop bits. The polarity of the transmitted A/D bit is selected by the CPU by programming bit MR1A[2]/MR1B[2]. MR1A[2]/MR1B[2] = 0 transmits a zero in the A/D bit position, which identifies the corresponding data bits as data, while MR1A[2]/MR1B[2] = 1 transmits a one in the A/D bit position, which identifies the corresponding data bits as an address. The CPU should program the mode register prior to loading the corresponding data bits into the THR.

In this mode, the receiver continuously looks at the received data stream, whether it is enabled or disabled. If disabled, it sets the RxRDY status bit and loads the character into the RHR FIFO if the received A/D bit is a one (address tag), but discards the received character if the received A/D bit is a zero (data tag). If enabled, all received characters are transferred to the CPU via the RHR. In either case, the data bits are loaded into the data FIFO while the A/D bit is loaded into the status FIFO position normally used for parity error (SRA[5] or SRB[5]). Framing error, overrun error, and break detect operate normally whether or not the receiver is enabled.

PROGRAMMING

The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The addressing of the registers is described in table 1.

The contents of certain control registers are initialized to zero on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems. For example, changing the number of bits per character while the transmitter is active may cause the transmission of an incorrect character. In general, the contents of the MR, the CSR, and the OPCR should only be changed while the receiver(s) and transmitter(s) are not enabled, and certain changes to the ACR should only be made while the C/T is stopped.

Mode registers 1 and 2 of each channel are accessed via independent auxiliary pointers. The pointer is set to MR1x by RESET or by issuing a 'reset pointer' command via the corresponding command register. Any read or write of the mode register while the pointer is at MR1x switches the pointer to MR2x. The pointer then remains at MR2x, so that subsequent accesses are always to MR2x unless the pointer is reset to MR1x as described above.

Mode, command, clock select, and status registers are duplicated for each channel to provide total independent operation and control. Refer to table 2 for register bit descriptions.

MR1A — Channel A Mode Register 1

MR1A is accessed when the channel A MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRA. After reading or writing MR1A, the pointer will point to MR2A.

MR1A[7] — Channel A Receiver Request-to-Send Control — This bit controls the deactivation of the RTSAN output (OP0) by the receiver. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR1A[7] = 1 causes RTSAN to be negated upon receipt of a valid start bit if the channel A FIFO is full. However, OPR[0] is not reset and RTSAN will be asserted again when an empty FIFO position is available. This feature can be used for flow control to prevent overrun in the receiver by using the RTSAN output signal to control the CTSN input of the transmitting device.

MR1A[6] — Channel A Receiver Interrupt Select — This bit selects either the channel A receiver ready status (RXRDY) or the channel A FIFO full status (FFULL) to be used for CPU interrupts. It also causes the selected bit to be output on OP4 if it is programmed as an interrupt output via the OPCR.

MR1A[5] — Channel A Error Mode Select — This bit selects the operating mode of the three FIFOed status bits (FE, PE, received break) for channel A. In the 'character' mode, status is provided on a character-by-character basis: the status applies only to the character at the top of the FIFO. In the 'block' mode, the status provided in the SR for these bits is the ac-

Table 1. 2681 REGISTER ADDRESSING

A3	A2	A1	A0	READ (RDN = 0)	WRITE (WRN = 0)
0	0	0	0	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
0	0	0	1	Status Register A (SRA)	Clock Select Reg. A (CSRA)
0	0	1	0	*Reserved*	Command Register A (CRA)
0	0	1	1	RX Holding Register A (RHRA)	TX Holding Register A (THRA)
0	1	0	0	Input Port Change Reg. (IPCR)	Aux. Control Register (ACR)
0	1	0	1	Interrupt Status Reg. (ISR)	Interrupt Mask Reg. (IMR)
0	1	1	0	Counter/Timer Upper (CTU)	C/T Upper Register (CTUR)
0	1	1	1	Counter/Timer Lower (CTL)	C/T Lower Register (CTLR)
1	0	0	0	Mode Register B (MR1B, MR2B)	Mode Register B (MR1B, MR2B)
1	0	0	1	Status Register B (SRB)	Clock Select Reg. B (CSRB)
1	0	1	0	*Reserved*	Command Register B (CRB)
1	0	1	1	RX Holding Register B (RHRB)	TX Holding Register B (THRB)
1	1	0	0	*Reserved*	*Reserved*
1	1	0	1	Input Port	Output Port Conf. Reg. (OPCR)
1	1	1	0	Start Counter Command	Set Output Port Bits Command
1	1	1	1	Stop Counter Command	Reset Output Port Bits Command

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Table 2. REGISTER BIT FORMATS

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	RX RTS CONTROL	RX INT SELECT	ERROR MODE	PARITY MODE		PARITY TYPE	BITS PER CHAR.	
MR1A MR1B	0 = no 1 = yes	0 = RXRDY 1 = FFULL	0 = char 1 = block	00 = with parity 01 = force parity 10 = no parity 11 = special mode		0 = even 1 = odd	00 = 5 01 = 6 10 = 7 11 = 8	

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	CHANNEL MODE		Tx RTS CONTROL	CTS ENABLE Tx	STOP BIT LENGTH*			
MR2A MR2B	00 = Normal 01 = Auto echo 10 = Local loop 11 = Remote loop		0 = no 1 = yes	0 = no 1 = yes	0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750	4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000	8 = 1.563 9 = 1.625 A = 1.688 B = 1.750	C = 1.813 D = 1.875 E = 1.938 F = 2.000

*Add 0.5 to values shown for 0-7 if channel is programmed for 5 bits/char

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CSRA CSRB	RECEIVER CLOCK SELECT				TRANSMITTER CLOCK SELECT			
	See text				See text			

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CRA CRB	not used— must be 0	MISCELLANEOUS COMMANDS			DISABLE Tx	ENABLE Tx	DISABLE Rx	ENABLE Rx
		See text			0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	RECEIVED BREAK	FRAMING ERROR	PARITY ERROR	OVERRUN ERROR	TxEMT	TxRDY	FFULL	RxRDY
SRA SRB	0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes *	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

*These status bits are appended to the corresponding data character in the receive FIFO A read of the status register provides these bits (7 5) from the top of the FIFO together with bits 4 0 These bits are cleared by a 'reset error status' command In character mode they are discarded when the corresponding data character is read from the FIFO

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	OP7	OP6	OP5	OP4	OP3		OP2	
OPCR	0 = OPR[7] 1 = TxRDYB	0 = OPR[6] 1 = TxRDYA	0 = OPR[5] 1 = RxRDY/ FFULLB	0 = OPR[4] 1 = RxRDY/ FFULLA	00 = OPR[3] 01 = C/T OUTPUT 10 = TxCB (1X) 11 = RxCB (1X)		00 = OPR[2] 01 = TxCA (16X) 10 = TxCA (1X) 11 = RxCA (1X)	

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	BRG SET SELECT	COUNTER/TIMER MODE AND SOURCE			DELTA IP3 INT	DELTA IP2 INT	DELTA IP1 INT	DELTA IP0 INT
ACR	0 = set1 1 = set2	See table 4			0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
	DELTA IP3	DELTA IP2	DELTA IP1	DELTA IP0	IP3	IP2	IP1	IP0
IPCR	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = low 1 = high	0 = low 1 = high	0 = low 1 = high	0 = low 1 = high

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Table 2. REGISTER BIT FORMATS (continued)

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ISR	INPUT PORT CHANGE	DELTA BREAK B	RxRDY/ FFULLB	TxRDYB	COUNTER READY	DELTA BREAK A	RxRDY/ FFULLA	TxRDYA
	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes	0 = no 1 = yes

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
IMR	IN. PORT CHANGE INT	DELTA BREAK B INT	RxRDY/ FFULLB INT	TxRDYB INT	COUNTER READY INT	DELTA BREAK A INT	RxRDY/ FFULLA INT	TxRDYA INT
	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on	0 = off 1 = on

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTUR	C/T[15]	C/T[14]	C/T[13]	C/T[12]	C/T[11]	C/T[10]	C/T[9]	C/T[8]

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CTLR	C/T[7]	C/T[6]	C/T[5]	C/T[4]	C/T[3]	C/T[2]	C/T[1]	C/T[0]

cumulation (logical OR) of the status for all characters coming to the top of the FIFO since the last 'reset error' command for channel A was issued.

MR1A[4:3] — Channel A Parity Mode Select — If 'with parity' or 'force parity' is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR1A[4:3] = 11 selects channel A to operate in the special multidrop mode described in the Operation section.

MR1A[2] — Channel A Parity Type Select — This bit selects the parity type (odd or even) if the 'with parity' mode is programmed by MR1A[4:3], and the polarity of the forced parity bit if the 'force parity' mode is programmed. It has no effect if the 'no parity' mode is programmed. In the special multidrop mode it selects the polarity of the A/D bit.

MR1A[1:0] — Channel A Bits per Character Select — This field selects the number of data bits per character to be transmitted and received. The character length does not include the start, parity, and stop bits.

MR2A — Channel A Mode Register 2

MR2A is accessed when the channel A MR pointer points to MR2, which occurs after any access to MR1A. Accesses to MR2A do not change the pointer.

MR2A[7:6] — Channel A Mode Select — Each channel of the DUART can operate in one of four modes. MR2A[7:6] = 00 is the normal mode, with the transmitter and receiver operating independently. MR2A[7:6] = 01 places the channel in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The channel A TxRDY and TxEMT status bits are inactive.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Character framing is checked, but the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.
8. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

Two diagnostic modes can also be configured. MR2A[7:6] = 10 selects local loopback mode. In this mode:

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxDA output is held high.
4. The RxDA input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode, selected by MR2A[7:6] = 11. In this mode:

1. Received data is reclocked and retransmitted on the TxDA output.
2. The receive clock is used for the transmitter.

Preview

3. Received data is not sent to the local CPU, and the error status conditions are inactive.
4. The received parity is not checked and is not regenerated for transmission, i.e., transmitted parity bit is as received.
5. The receiver must be enabled.
6. Character framing is not checked, and the stop bits are retransmitted as received.
7. A received break is echoed as received until the next valid start bit is detected.

The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character. Likewise, if a mode is deselected, the device will switch out of the mode immediately. An exception to this is switching out of autoecho or remote loopback modes: if the de-selection occurs just after the receiver has sampled the stop bit (indicated in autoecho by assertion of RxRDY), and the transmitter is enabled, the transmitter will remain in autoecho mode until the entire stop bit has been retransmitted.

MR2A[5] — Channel A Transmitter Request-to-Send Control — This bit controls the deactivation of the RTSAN output (OP0) by the transmitter. This output is normally asserted by setting OPR[0] and negated by resetting OPR[0]. MR2A[5] = 1 causes OPR[0] to be reset automatically one bit time after the characters in the channel A transmit shift register and in the THR, if any, are completely transmitted, including the programmed number of stop bits, if the transmitter is not enabled. This feature can be used to automatically terminate the transmission of a message as follows:

1. Program auto-reset mode: MR2A[5] = 1.
2. Enable transmitter.
3. Assert RTSAN: OPR[0] = 1.
4. Send message.
5. Disable transmitter after the last character is loaded into the channel A THR.
6. The last character will be transmitted and OPR[0] will be reset one bit time after the last stop bit, causing RTSAN to be negated.

MR2A[4] — Channel A Clear-to-Send Control — If this bit is 0, CTSAN has no effect on the transmitter. If this bit is a 1, the transmitter checks the state of CTSAN (IP0) each time it is ready to send a character. If IP0 is asserted (low), the character is transmitted. If it is negated (high), the TxDA output remains in the marking state and the transmission is delayed until CTSAN goes low. Changes in CTSAN while a character is being transmitted do not affect the transmission of that character.

MR2A[3:0] — Channel A Stop Bit Length Select — This field programs the length of the stop bit appended to the transmitted character. Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16 bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16 bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled) in all cases.

If an external 1X clock is used for the transmitter, MR2A[3] = 0 selects one stop bit and MR2A[3] = 1 selects two stop bits to be transmitted.

MR1B — Channel B Mode Register 1

MR1B is accessed when the channel B MR pointer points to MR1. The pointer is set to MR1 by RESET or by a 'set pointer' command applied via CRB. After reading or writing MR1B, the pointer will point to MR2B.

The bit definitions for this register are identical to the bit definitions for MR1A, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

MR2B — Channel B Mode Register 2

MR2B is accessed when the channel B MR pointer points to MR2, which occurs after any access to MR1B. Accesses to MR2B do not change the pointer.

The bit definitions for this register are identical to the bit definitions for MR2A, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

CSRA — Channel A Clock Select Register

CSRA[7:4] — Channel A Receiver Clock Select — This field selects the baud rate clock for the channel A receiver as follows:

CSRA[7:4]	Baud Rate ACR[7] = 0	Baud Rate ACR[7] = 1
0 0 0 0	50	75
0 0 0 1	110	110
0 0 1 0	134.5	134.5
0 0 1 1	200	150
0 1 0 0	300	300
0 1 0 1	600	600
0 1 1 0	1,200	1,200
0 1 1 1	1,050	2,000
1 0 0 0	2,400	2,400
1 0 0 1	4,800	4,800
1 0 1 0	7,200	1,800
1 0 1 1	9,600	9,600
1 1 0 0	38.4K	19.2K
1 1 0 1	Timer	Timer
1 1 1 0	IP4—16X	IP4—16X
1 1 1 1	IP4—1X	IP4—1X

The receiver clock is always a 16X clock except for CSRA[7:4] = 1111.

CSRA[3:0] — Channel A Transmitter Clock Select — This field selects the baud rate clock for the channel A transmitter. The field definition is as per CSRA[7:4] except as follows:

CSRA[3:0]	Baud Rate ACR[7] = 0	Baud Rate ACR[7] = 1
1 1 1 0	IP3—16X	IP3—16X
1 1 1 1	IP3—1X	IP3—1X

The transmitter clock is always a 16X clock except for CSRA[3:0] = 1111.

CSRB — Channel B Clock Select Register — Access Type: Write Only

CSRB[7:4] — Channel B Receiver Clock Select — This field selects the baud rate clock for the channel B receiver. The field definition is as per CSRA[7:4] except as follows:

CSRB[7:4]	Baud Rate ACR[7] = 0	Baud Rate ACR[7] = 1
1 1 1 0	IP6—16X	IP6—16X
1 1 1 1	IP6—1X	IP6—1X

The receiver clock is always a 16X clock except for CSRB[7:4] = 1111.

CSRB[3:0] — Channel B Transmitter Clock Select — This field selects the baud rate clock for the channel B transmitter. The field definition is as per CSRA[7:4] except as follows:

CSRB[3:0]	Baud Rate ACR[7] = 0	Baud Rate ACR[7] = 1
1 1 1 0	IP5—16X	IP5—16X
1 1 1 1	IP5—1X	IP5—1X

The transmitter clock is always a 16X clock except for CSRB[3:0] = 1111.

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CRA — Channel A Command Register

CRA is a register used to supply commands to channel A. Multiple commands can be specified in a single write to CRA as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

CRA[6:4] — Channel A Miscellaneous Commands — The encoded value of this field may be used to specify a single command as follows:

CRA[6:4]	COMMAND
0 0 0	No command.
0 0 1	Reset MR pointer. Causes the channel A MR pointer to point to MR1.
0 1 0	Reset receiver. Resets the channel A receiver as if a hardware reset had been applied. The receiver is disabled and the FIFO is flushed.
0 1 1	Reset transmitter. Resets the channel A transmitter as if a hardware reset had been applied.
1 0 0	Reset error status. Clears the channel A Received Break, Parity Error, Framing Error, and Overrun Error bits in the status register (SRA[7:4]). Used in character mode to clear OE status (although RB, PE, and FE bits will also be cleared) and in block mode to clear all error status after a block of data has been received.
1 0 1	Reset channel A break change interrupt. Causes the channel A break detect change bit in the interrupt status register (ISR[2]) to be cleared to zero.
1 1 0	Start break. Forces the TXDA output low (spacing). If the transmitter is empty the start of the break condition will be delayed up to two bit times. If the transmitter is active the break begins when transmission of the character is completed. If a character is in the THR, the start of the break will be delayed until that character, or any others loaded subsequently are transmitted. The transmitter must be enabled for this command to be accepted.
1 1 1	Stop Break. The TXDA line will go high (marking) within two bit times. TXDA will remain high for one bit time before the next character, if any, is transmitted.

CRA[3] — Disable Channel A Transmitter — This command terminates transmitter operation and resets the TxRDY and TxEMT status bits. However, if a character is being transmitted or if a character is in the THR when the transmitter is disabled, the transmission of the character(s) is completed before assuming the inactive state.

CRA[2] — Enable Channel A Transmitter — Enables operation of the channel A transmitter. The TxRDY status bit will be asserted.

CRA[1] — Disable Channel A Receiver — This command terminates operation of the receiver immediately — a character being received will be lost. The command has no effect on the receiver status bits or any other control registers. If the special multidrop mode is programmed, the receiver operates even if it is disabled. See Operation section.

CRA[0] — Enable Channel A Receiver — Enables operation of the channel A receiver. If not in the special wakeup mode, this also forces the receiver into the search for start-bit state.

CRB — Channel B Command Register

CRB is a register used to supply commands to channel B. Multiple commands can be specified in a single write to CRB as long as the commands are non-conflicting, e.g., the 'enable transmitter' and 'reset transmitter' commands cannot be specified in a single command word.

The bit definitions for this register are identical to the bit definitions for CRA, except that all control actions apply to the channel B receiver and transmitter and the corresponding inputs and outputs.

SRA — Channel A Status Register

SRA[7] — Channel A Received Break — This bit indicates that an all zero character of the programmed length has been received without a stop bit. Only a single FIFO position is occupied when a break is received: further entries to the FIFO are inhibited until the RxDA line returns to the marking state for at least one-half a bit time (two successive edges of the internal or external 1x clock). When this bit is set, the channel A 'change in break' bit in the ISR (ISR[2]) is set. ISR[2] is also set when the end of the break condition, as defined above, is detected.

The break detect circuitry can detect breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until at least the end of the next character time in order for it to be detected.

SRA[6] — Channel A Framing Error — This bit, when set, indicates that a stop bit was not detected when the corresponding data character in the FIFO was received. The stop bit check is made in the middle of the first stop bit position.

SRA[5] — Channel A Parity Error — This bit is set when the 'with parity' or 'force parity' mode is programmed and the corresponding character in the FIFO was received with incorrect parity.

In the special multidrop mode the parity error bit stores the received A/D bit.

SRA[4] — Channel A Overrun Error — This bit, when set, indicates that one or more characters in the received data stream have been lost. It is set upon receipt of a new character when the FIFO is full and a character is already in the receive shift register waiting for an empty FIFO position. When this occurs, the character in the receive shift register (and its break detect, parity error and framing error status, if any) is lost.

This bit is cleared by a 'reset error status' command.

SRA[3] — Channel A Transmitter Empty (TxEMTA) — This bit will be set when the channel A transmitter underruns, i.e., both the transmit holding register (THR) and the transmit shift register are empty. It is set after transmission of the last stop bit of a character if no character is in the THR awaiting transmission. It is reset when the THR is loaded by the CPU or when the transmitter is disabled.

SRA[2] — Channel A Transmitter Ready (TxRDYA) — This bit, when set, indicates that the THR is empty and ready to be loaded with a character. This bit is cleared when the THR is loaded by the CPU and is set when the character is transferred to the transmit shift register. TxRDY is reset when the transmitter is disabled and is set when the transmitter is first enabled, viz., characters loaded into the THR while the transmitter is disabled will not be transmitted.

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SRA[1] — Channel A FIFO Full (FFULLA) — This bit is set when a character is transferred from the receive shift register to the receive FIFO and the transfer causes the FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, FFULL will not be reset when the CPU reads the RHR.

SRA[0] — Channel A Receiver Ready (RxRDYA) — This bit indicates that a character has been received and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR, if after this read there are no more characters still in the FIFO.

SRB — Channel B Status Register

The bit definitions for this register are identical to the bit definitions for SRA, except that all status applies to the channel B receiver and transmitter and the corresponding inputs and outputs.

OPCR — Output Port Configuration Register

OPCR[7] — OP7 Output Select — This bit programs the OP7 output to provide one of the following:

- The complement of OPR[7]
- The channel B transmitter interrupt output, which is the complement of TxRDYB. When in this mode OP7 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[6] — OP6 Output Select — This bit programs the OP6 output to provide one of the followng:

- The complement of OPR[6]
- The channel A transmitter interrupt output, which is the complement of TxRDYA. When in this mode OP6 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[5] — OP5 Output Select — This bit programs the OP5 output to provide one of the following:

- The complement of OPR[5]
- The channel B receiver interrupt output, which is the complement of ISR[5]. When in this mode OP5 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[4] — OP4 Output Select — This bit programs the OP4 output to provide one of the following:

- The complement of OPR[4]
- The channel A receiver interrupt output, which is the complement of ISR[1]. When in this mode OP4 acts as an open collector output. Note that this output is not masked by the contents of the IMR.

OPCR[3:2] — OP3 Output Select — This field programs the OP3 output to provide one of the following:

- The complement of OPR[3]
- The counter/timer output, in which case OP3 acts as an open collector output. In the timer mode, this output is a square wave at the programmed frequency. In the counter mode, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state when the counter is stopped by a stop counter command. Note that this output is not masked by the contents of the IMR.
- The 1X clock for the channel B transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the channel B receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

OPCR[1:0] — OP2 Output Select — This field programs the OP2 output to provide one of the following:

- The complement of OPR[2]
- The 16X clock for the channel A transmitter. This is the clock selected by CSRA[3:0], and will be a 1X clock if CSRA[3:0] = 1111.
- The 1X clock for the channel A transmitter, which is the clock that shifts the transmitted data. If data is not being transmitted, a free running 1X clock is output.
- The 1X clock for the channel A receiver, which is the clock that samples the received data. If data is not being received, a free running 1X clock is output.

ACR — Auxiliary Control Register

ACR[7] — Baud Rate Generator Set Select — This bit selects one of two sets of baud rates to be generated by the BRG:

Set 1: 50, 110, 134.5, 200, 300, 600, 1.05K, 1.2K, 2.4K, 4.8K, 7.2K, 9.6K, and 38.4K baud.

Set 2: 75, 110, 134.5, 150, 300, 600, 1.2K, 1.8K, 2.0K, 2.4K, 4.8K, 9.6K, and 19.2K baud.

The selected set of rates is available for use by the channel A and B receivers and transmitters as described in CSRA and CSRB. Baud rate generator characteristics are given in table 3.

Table 3. BAUD RATE GENERATOR CHARACTERISTICS CRYSTAL OR CLOCK = 3.6864MHz

NOMINAL RATE (BAUD)	ACTUAL 16X CLOCK (KHz)	ERROR (PERCENT)
50	0.8	0
75	1.2	0
110	1.759	-0.069
134.5	2.153	0.059
150	2.4	0
200	3.2	0
300	4.8	0
600	9.6	0
1050	16.756	-0.260
1200	19.2	0
1800	28.8	0
2000	32.056	0.175
2400	38.4	0
4800	76.8	0
7200	115.2	0
9600	153.6	0
19.2K	307.2	0
38.4K	614.4	0

NOTE
Duty cycle of 16X clock is 50% ± 1%

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ACR[6:4]—Counter/Timer Mode and Clock Source Select — This field selects the operating mode of the counter/timer and its clock source as shown in table 4.

ACR[3:0] — IP3, IP2, IP1, IPO Change of State Interrupt Enable — This field selects which bits of the Input Port Change register (IPCR) cause the input change bit in the interrupt status register (ISR[7]) to be set. If a bit is in the 'on' state, the setting of the corresponding bit in the IPCR will also result in the setting of ISR[7], which results in the generation of an interrupt output if IMR[7] = 1. If a bit is in the 'off' state, the setting of that bit in the IPCR has no effect on ISR[7].

Table 4. ACR [6:4] FIELD DEFINITION

ACR[6:4]	MODE	CLOCK SOURCE
0 0 0	Counter	External (IP2)
0 0 1	Counter	TXCA — 1X clock of channel A transmitter
0 1 0	Counter	TXCB — 1X clock of channel B transmitter
0 1 1	Counter	Crystal or external clock (X1/CLK) divided by 16
1 0 0	Timer	External (IP2)
1 0 1	Timer	External (IP2) divided by 16
1 1 0	Timer	Crystal or external clock (X1/CLK)
1 1 1	Timer	Crystal or external clock (X1/CLK) divided by 16

IPCR — Input Port Change Register

IPCR[7:4] — IP3, IP2, IP1, IP0 Change of State — These bits are set when a change of state, as defined in the Input Port section of this data sheet, occurs at the respective input pins. They are cleared when the IPCR is read by the CPU. A read of the IPCR also clears ISR[7], the input change bit in the interrupt status register.

The setting of these bits can be programmed to generate an interrupt to the CPU.

IPCR[3:0] — IP3, IP2, IP1, IP0 Current State — These bits provide the current state of the respective inputs. The information is unlatched and reflects the state of the input pins at the time the IPCR is read.

ISR — Interrupt Status Register

This register provides the status of all potential interrupt sources. The contents of this register are masked by the interrupt mask register (IMR). If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the reading of the ISR — the true status will be provided regardless of the contents of the IMR. The contents of this register are initialized to 00_{16} when the DUART is reset.

ISR[7] — Input Port Change Status — This bit is a '1' when a change of state has occurred at the IP0, IP1, IP2, or IP3 inputs and that event has been selected to cause an interrupt by the programming of ACR[3:0]. The bit is cleared when the CPU reads the IPCR.

ISR[6] — Channel B Change in Break — This bit, when set, indicates that the channel B receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a channel B 'reset break change interrupt' command.

ISR[5] — Channel B Receiver Ready or FIFO Full — The function of this bit is programmed by MR2B[5]. If programmed as receiver ready, it indicates that a character has been received in channel B and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the channel B FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[4] — Channel B Transmitter Ready — This bit is a duplicate of TxRDYB (SRB[2]).

ISR[3] — Counter Ready — In the counter mode, this bit is set when the counter reaches terminal count and is reset when the counter is stopped by a stop counter command.

In the timer mode, this bit is set once each cycle of the generated square wave (every other time that the counter/timer reaches zero count). The bit is reset by a stop counter command. The command, however, does not stop the counter/timer.

ISR[2] — Channel A Change in Break — This bit, when set, indicates that the channel A receiver has detected the beginning or the end of a received break. It is reset when the CPU issues a channel A 'reset break change interrupt' command.

ISR[1] — Channel A Receiver Ready or FIFO Full — The function of this bit is programmed by MR2A[5]. If programmed as receiver ready, it indicates that a character has been received in channel A and is waiting in the FIFO to be read by the CPU. It is set when the character is transferred from the receive shift register to the FIFO and reset when the CPU reads the RHR. If after this read there are more characters still in the FIFO the bit will be set again after the FIFO is 'popped'. If programmed as FIFO full, it is set when a character is transferred from the receive holding register to the receive FIFO and the transfer causes the channel A FIFO to become full, i.e., all three FIFO positions are occupied. It is reset when the CPU reads the RHR. If a character is waiting in the receive shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

ISR[0] — Channel A Transmitter Ready — This bit is a duplicate of TxRDYA (SRA[2]).

IMR — Interrupt Mask Register

The programming of this register selects which bits in the ISR cause an interrupt output. If a bit in the ISR is a '1' and the corresponding bit in the IMR is also a '1', the INTRN output will be asserted. If the corresponding bit in the IMR is a zero, the state of the bit in the ISR has no effect on the INTRN output. Note that the IMR does not mask the programmable interrupt outputs OP3-OP7 or the reading of the ISR.

Preview

CTUR and CTLR — Counter/Timer Registers

The CTUR and CTLR hold the eight MSB's and eight LSB's respectively of the value to be used by the counter/timer in either the counter or timer modes of operation.

In the timer (programmable divider) mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. If the value in CTUR or CTLR is changed, the current half-period will not be affected, but subsequent half periods will be. In this mode the C/T runs continuously. Receipt of a start counter command (read with A3-A0 = 1111) causes the counter to terminate the current timing cycle and to begin a new cycle using the values in CTUR and CTLR. The counter ready status bit (ISR[3]) is set once each cycle of the square wave. The bit is reset by a stop counter command (read with A3-A0 = 1110). The command, however, does not stop the C/T. The generated square wave is output on OP3 if it is programmed to be the C/T output.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the CPU. Counting begins upon receipt of a start counter command. Upon reaching terminal count (0000_{16}), the counter ready interrupt bit (ISR[3]) is set. The counter continues counting past the terminal count until stopped by the CPU. If OP3 is programmed to be the output of the C/T, the output remains high until terminal count is reached, at which time it goes low. The output returns to the high state and ISR[3] is cleared when the counter is stopped by a stop counter command. The CPU may change the values of CTUR and CTLR at any time, but the new count becomes effective only on the next start counter command. If new values have not been loaded, the previous count values are preserved and used for the next count cycle.

In the counter mode, the current value of the upper and lower 8 bits of the counter may be read by the CPU. It is recommended that the counter be stopped when reading to prevent potential problems which may occur if a carry from the lower 8-bits to the upper 8-bits occurs between the times that both halves of the counter are read. However, note that a subsequent start counter command will cause the counter to begin a new count cycle using the values in CTUR and CTLR.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.5 to +6.0	V

NOTES

1 Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied

2 For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient for ceramic package (116°C/W for plastic package)

3 This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6]

	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage (except X1/CLK)		2.0			V
V_{IH}	Input high voltage (X1/CLK)		3.0			V
V_{OL}	Output low voltage	$I_{OL} = 2.4mA$			0.4	V
V_{OH}	Output high voltage (except o.c. outputs)	$I_{OH} = -400\mu A$	2.4			V
I_{IL}	Input leakage current	$V_{IN} = 0$ to V_{CC}	−10		10	μA
I_{LL}	Data bus 3-state leakage current	$V_O = 0$ to V_{CC}	−10		10	μA
I_{OC}	Open collector output leakage current	$V_O = 0$ to V_{CC}	−10		10	μA
I_{CC}	Power supply current				150	mA

NOTES

4 Parameters are valid over specified temperature range

5 All voltage measurements are referenced to ground (GND) For testing, all input signals swing between 0 4V and 2 4V with a transition time of 20ns maximum All time measurements are referenced at input voltages of 0 8V and 2 0V and output voltages of 0 8V and 2 0V as appropriate

6 Typical values are at +25°C, typical supply voltages, and typical processing parameters

DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SC2681 SERIES

Preview

AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6,7]

PARAMETER	TENTATIVE LIMITS			UNIT
	Min	Typ	Max	
Reset Timing (figure 1)				
t_{RES} RESET pulse width	1.0			μs
Bus Timing (figure 2)[8]				
t_{AS} A0-A3 setup time to RDN, WRN low	10			ns
t_{AH} A0-A3 hold time from RDN, WRN high	10			ns
t_{CS} CEN setup time to RDN, WRN low	0			ns
t_{CH} CEN hold time from RDN, WRN high	0			ns
t_{RW} WRN, RDN pulse width	225			ns
t_{DD} Data valid after RDN low			150	ns
t_{DF} Data bus floating after RDN high			100	ns
t_{DS} Data setup time before WRN high	100			ns
t_{DH} Data hold time after WRN high	0			ns
t_{CC} Time between READs and/or WRITEs	600			ns
Port Timing (figure 3)[8]				
t_{PS} Port input setup time before RDN low	0			ns
t_{PH} Port input hold time after RDN high	0			ns
t_{PD} Port output valid after WRN high			400	ns
Interrupt Timing (figure 4)				
t_{IR} INTRN (or OP3-OP7 when used as interrupts) high from:				
Read RHR (RXRDY/FFULL interrupt)			300	ns
Write THR (TXRDY interrupt)			300	ns
Reset command (delta break interrupt)			300	ns
Stop C/T command (counter interrupt)			300	ns
Read IPCR (input port change interrupt)			300	ns
Write IMR (clear of interrupt mask bit)			200	ns
Clock Timing (figure 5)				
t_{CLK} X1/CLK high or low time	100			ns
f_{CLK} X1/CLK frequency	2.0	3.6864	4.0	MHz
t_{CTC} CTCLK (IP2) high or low time	200			ns
f_{CTC} CTCLK (IP2) frequency	0		2.0	MHz
t_{RX} RxC high or low time	220			ns
f_{RX} RxC frequency (16X)	0		2.0	MHz
(1X)	0		1.0	MHz
t_{TX} TxC high or low time	220			ns
f_{TX} TxC frequency (16X)	0		2.0	MHz
(1X)	0		1.0	MHz
Transmitter Timing (figure 6)				
t_{TXD} TxD output delay from TxC low			350	ns
t_{TCS} TxC output skew from TxD output data	−75	0	75	ns
Receiver Timing (figure 7)				
t_{RXS} RxD data setup time to RXC high	200			ns
t_{RXH} RxD data hold time from RXC high	200			ns

NOTES

4 Parameters are valid over specified temperature range

5 All voltage measurements are referenced to ground (GND) For testing, all input signals swing between 0 4V and 2 4V with a transition time of 20ns maximum All time measurements are referenced at input voltages of 0 8V and 2 0V and output voltages of 0 8V and 2 0V as appropriate

6 Typical values are at +25°C, typical supply voltages, and typical processing parameters

7 Test condition for outputs $C_L = 150pF$

8 Timing is illustrated and referenced to the WRN and RDN inputs The device may also be operated with CEN as the 'strobing' input. In this case, all timing specifications apply referenced to the falling and rising edges of CEN

Preview

1

RESET TIMING

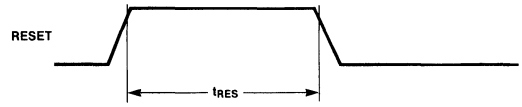


FIGURE 1

BUS TIMING

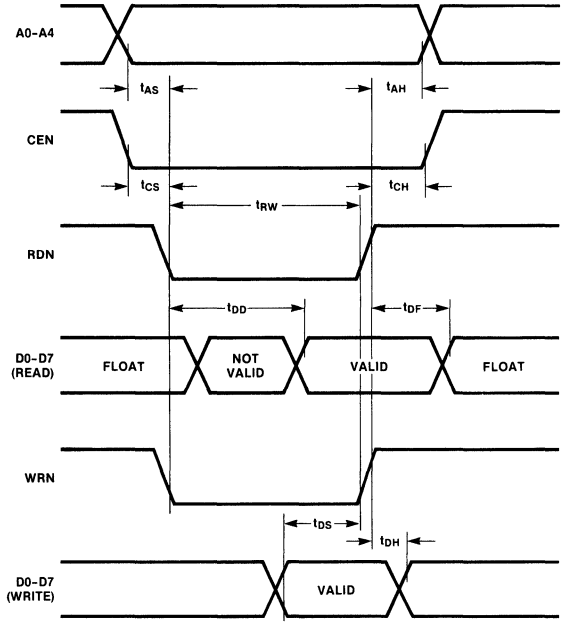


FIGURE 2

Preview

PORT TIMING

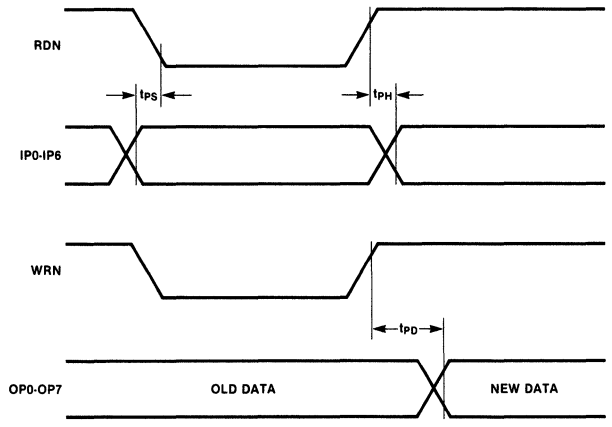


FIGURE 3

INTERRUPT TIMING

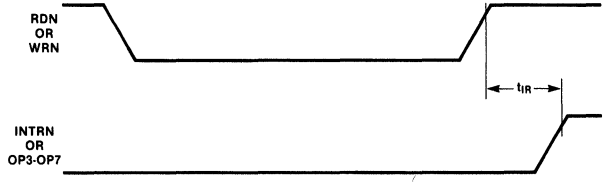


FIGURE 4

CLOCK TIMING

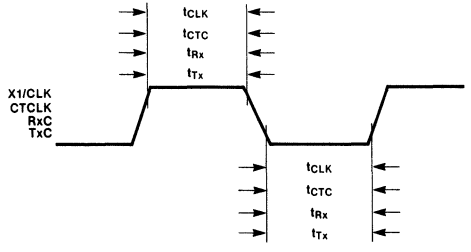


FIGURE 5

Preview

1

TRANSMIT

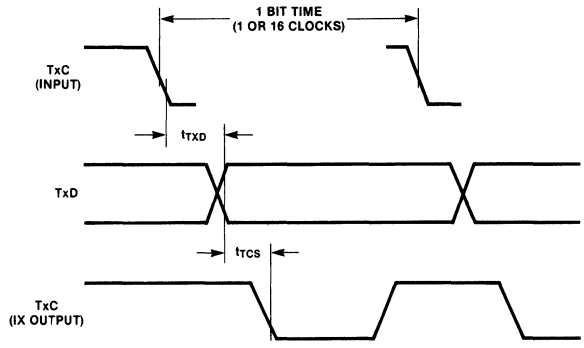


FIGURE 6

RECEIVE

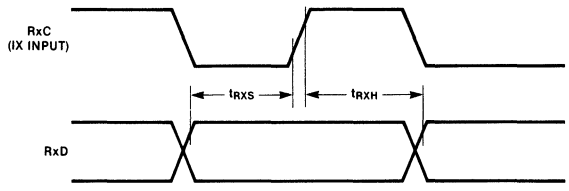
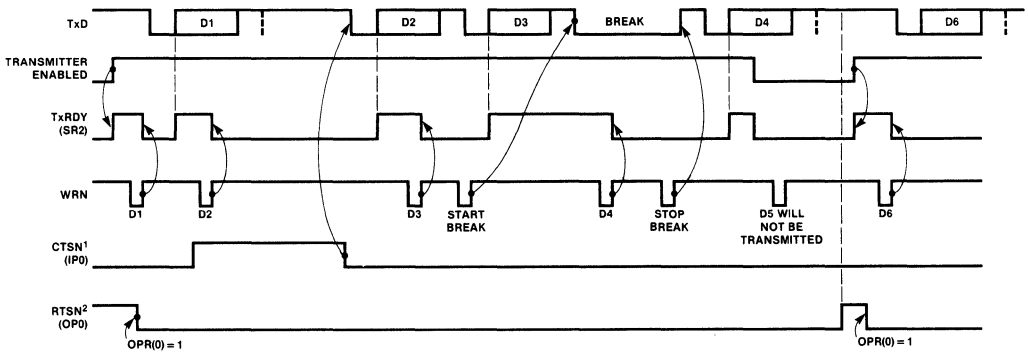


FIGURE 7

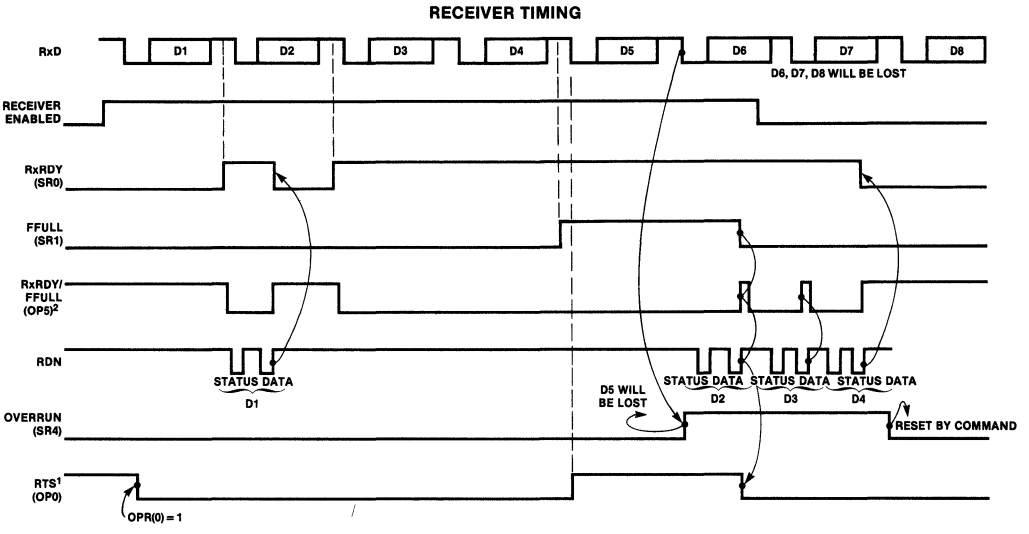
TRANSMITTER TIMING



NOTES
1. TIMING SHOWN FOR MR2(4) = 1
2 TIMING SHOWN FOR MR2(5) = 1

FIGURE 8

Preview



NOTES
1. TIMING SHOWN FOR MR1(7) = 1.
2. SHOWN FOR OPCR(4) = 1 AND MR1(6) = 0.

FIGURE 9

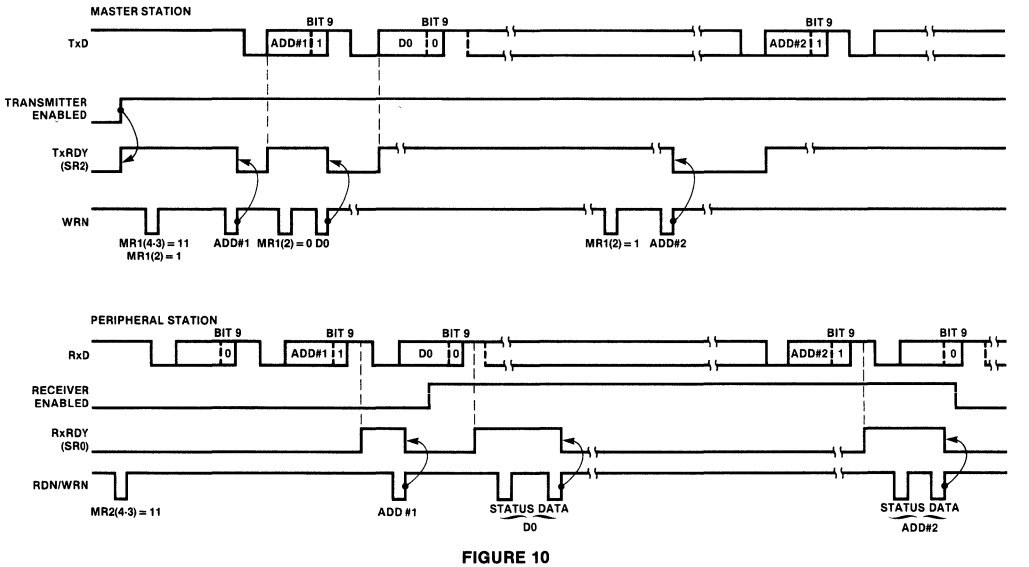


FIGURE 10

Section 2
Video Display

DISPLAY CHARACTER AND GRAPHICS GENERATOR (DCGG) SC2670

Preliminary

DESCRIPTION

The Signetics Display Character and Graphics Generator (DCGG) is a mask-programmable 11,648-bit line select character generator. It contains 128 10X9 characters placed in a 10X16 matrix, and has the capability of shifting certain characters, such as j, y, g, p and q, that normally extend below the baseline. Character shifting, previously requiring additional external circuitry, is now accomplished internally by the DCGG; effectively, the 9 active lines are lowered within the matrix to compensate for the character's position.

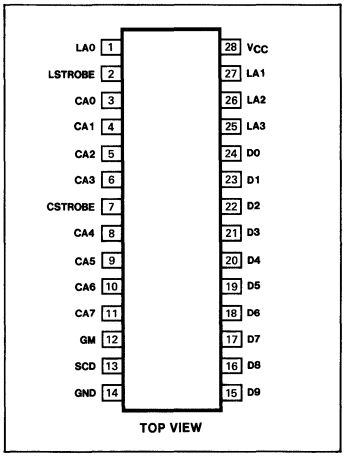
Seven bits of an 8-bit address code are used to select 1 of the 128 available characters. The eighth bit functions as a chip enable signal. Each character is defined by a pattern of logic Is and Os stored in a 10X9 matrix. When a specific 4-bit binary line address code is applied, a word of 10 parallel bits appears at the output. The lines can be sequentially selected, providing a 9-word sequence of 10 parallel bits per word for each character selected by the address inputs. As the line address inputs are sequentially addressed, the device will automatically place the 10X9 character in 1 of 2 preprogrammed positions on the 16-line matrix with the positions defined by the 4-line address inputs. One or more of the 10 parallel outputs can be used as control signals to selectively enable functions such as half-dot shift, color selection, etc.

The 2670 DCGG includes latches to store the character address and line address data. A control input to inhibit character data output for certain groups of characters is also provided. The 2670 also includes a graphics capability, wherein the 8-bit character code is translated directly into 256 possible user programmable graphic patterns. Thus, the DCGG can generate data for 384 distinct patterns, of which 128 are defined by the mask programmable ROM. See figure 1 for a typical applications display.

FEATURES

- 128 10X9 matrix characters
- 256 graphic characters
- Optional thin graphics for forms
- Character and line address latches
- Internal descend logic
- 300nsec character select access maximum
- Control character output inhibit logic
- Static operation—no clocks required
- Single 5V power supply
- TTL compatible inputs and outputs

PIN CONFIGURATION



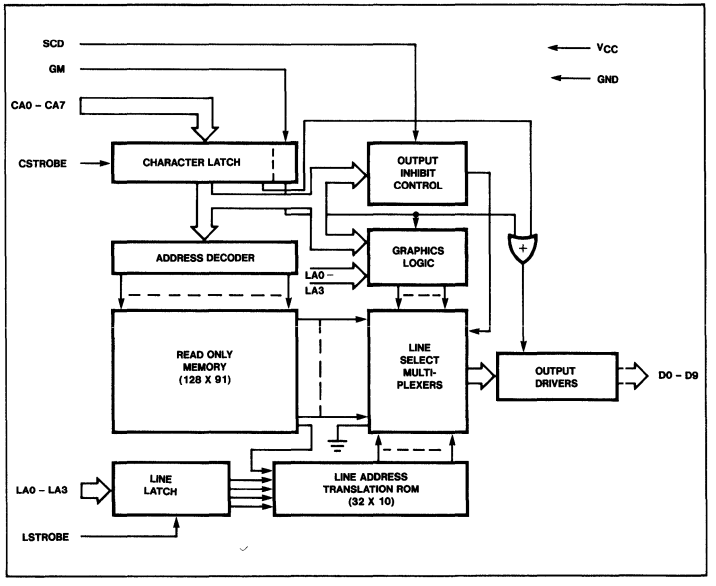
TOP VIEW

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%, T_A = 0°C to 70°C
Ceramic DIP	SC2670*CSI28
Plastic DIP	SC2670*CSN28

NOTE
Substitute letter corresponding to standard font for '*' in part number for standard parts See back of data sheet Contact sales office for custom ROM patterns

BLOCK DIAGRAM



DISPLAY CHARACTER AND GRAPHICS GENERATOR (DCGG) SC2670

Preliminary

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
CA0-CA7	3-6, 8-11	I	**Character Address:** Eight bit code specifies the character or graphic pattern for which matrix data is to be supplied. In character mode (GM=0), CA0 thru CA6 select one of the 128 ROM-defined characters and CA7 is a chip enable. The outputs are active when CA7=1 and are tri-stated when CA7=0. In graphics mode (GM=1), the outputs are active and CA0 thru CA7 select one of 256 possible graphic patterns to be output.
CSTROBE	7	I	**Character Strobe:** Used to store the character address (CA0 thru CA7) and graphics mode (GM) inputs into the character latch Data is latched on the negative going edge of CSTROBE
GM	12	I	**Graphics Mode:** GM=0 (low) selects character mode, GM=1 (high) selects graphics mode
LA0-LA3	1, 25-27	I	**Line Address:** In character mode, selects one of the 16 lines of matrix data for the selected character to appear at the 10 outputs. LA0 is the LSB and LA3 is the MSB. The input codes which cause each of the nine lines of character data to be output are specified as part of the programming data for both non-shifted and shifted fonts. Cycling through the nine specified counts at the LA0 thru LA3 inputs cause successive lines of data to be output on D0 thru D9 The 7 non-specified codes for both non-shifted and shifted characters cause blanks (logic zeros) to be output. In graphics mode, the line address gates the latched graphics data directly to the outputs
LSTROBE	2	I	**Line Strobe:** Used to store the line address data (LA0 thru LA3) in the line address latch Data is latched on the negative going edge of LSTROBE
SCD	13	I	**Selected Character Disable:** In character mode, a high level at this input causes all outputs (regardless of line address) to be blanks (zeros) for characters for which CA6 and CA5 are both 0. A low level input selects normal operation. Inoperative in the graphics mode.
D9-D0	15-24	O	**Data Outputs:** Provide the data for the specified character and line.
V_{CC}	28	I	+5V power supply
GND	14	I	Ground.

TYPICAL APPLICATION

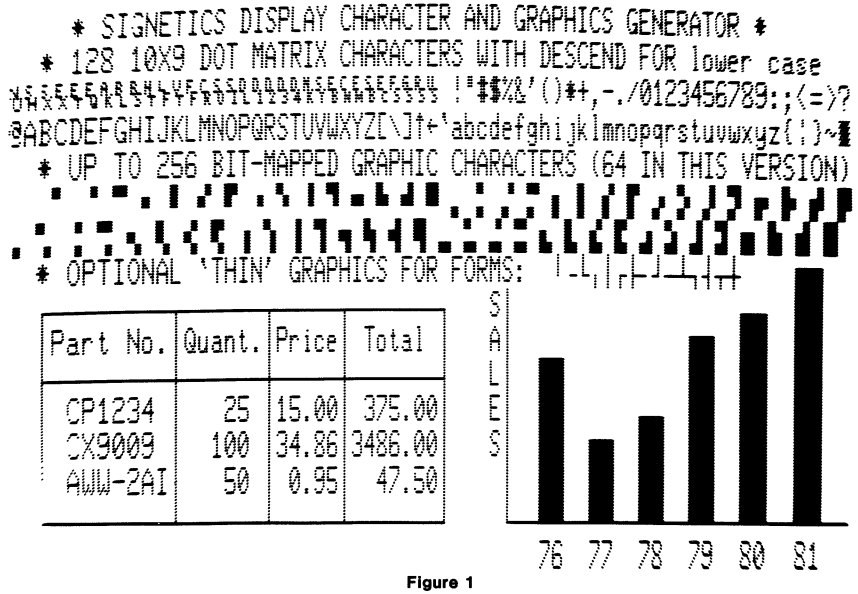


Figure 1

DISPLAY CHARACTER AND GRAPHICS GENERATOR (DCGG) SC2670

Preliminary

FUNCTIONAL DESCRIPTION

The DCGG consists of nine major sections. Line and character codes are strobed into the line and character latches. The character latch outputs are presented to the three sources of data; the ROM through an address decoder, the graphics logic, and the output inhibit control. The output inhibit control (together with the SCD input) suppresses the ROM data for selected character codes. The outputs from the line latch drive the line address translation ROM which maps the character ROM data onto 9 of 16 line positions. Finally, the line select multiplexers route the ROM or graphics data to the output drivers on D0 through D9.

Character Latch

The character latch is a 9-bit edge triggered latch used to store the character address (CA0 thru CA7) and graphics mode (GM) inputs. The data is stored on the falling edge of CSTROBE. Seven latched addresses (CA0 thru CA6) are inputs to the ROM character address decoder. In character mode (GM=0), CA7 operates as a chip enable. The output drivers are enabled when CA7=1 and are tri-stated when CA7=0. In graphics mode (GM=1), the output drivers are always enabled and the CA0 thru CA7 outputs of the latch are used to generate graphic symbols.

Character Address Decoder

This circuit decodes the 7-bit character address from the character latch to select one of the 128 character fonts stored in the ROM section of the DCGG.

Read Only Memory

The 11,648-bit ROM stores the fonts for the 128 matrix-defined characters. The data for each character consists of 91 bits. Ninety bits represent the 10X9 matrix and one bit specifies whether the character data is output at the normal (unshifted) lines or at the descended (shifted) lines. The 90 data bit outputs are supplied to the line select multiplexers. The descend control bit is an input to the line address translation ROM.

Graphics Logic

When the GM input is zero (low), the DCGG operates in the character mode. When it is one (high), it operates in the graphics mode. In graphics mode, output data is generated by the graphics logic instead of the ROM. The graphics logic maps the latched character address (CA0 thru CA7) to the outputs (D0 thru D9) as a function of line address (LA0 thru LA3). For any particular line address value, two of the CA bits are output: CA0, CA2, CA4 or CA6 is output on D0 thru D4 and CA1, CA3, CA5 or CA7 is output on D5 thru D9. The outputs are paired: When CA0 is output on D0 thru D4, CA1 is output on D5 thru D9 and likewise for CA2-CA3, CA4-CA5 and CA6-CA7.

A ROM within the graphics logic allows the specific line numbers for which each pair of bits is output to be specified by the customer. Figure 2 illustrates the general format for graphics symbols and an example where (CA7 thru CA0) = H'65'. The outputs from the graphics logic go to the line select multiplexers. The multiplexers route the graphic symbol data to the outputs when GM = 1.

Thin Graphics Option

As a customer specified option, 16 of the possible graphic codes (H'80' to H'8F') may be used to generate the special graphic characters illustrated in figure 3. For each of these characters, the vertical component appears on the D4 output. The horizontal component occurs on L_H which is specified by the customer. The vertical components specified by CA0 and CA2 are output for line addresses zero thru L_H and L_H thru fifteen, respectively.

Line Select Multiplexers

The ten line select multiplexers select ROM data as specified by the line address translation ROM when GM=0, or graphics data when GM=1. The inputs to each multiplexer are the nine line outputs from the ROM, an output from the graphics logic and a logic zero (ground).

Output Drivers

Ten output drivers with 3-state capability serve as buffers between the line select multiplexers and external logic. The 3-state control input to these drivers is supplied from the CA7 latch when GM=0. When GM=1, the outputs are always active.

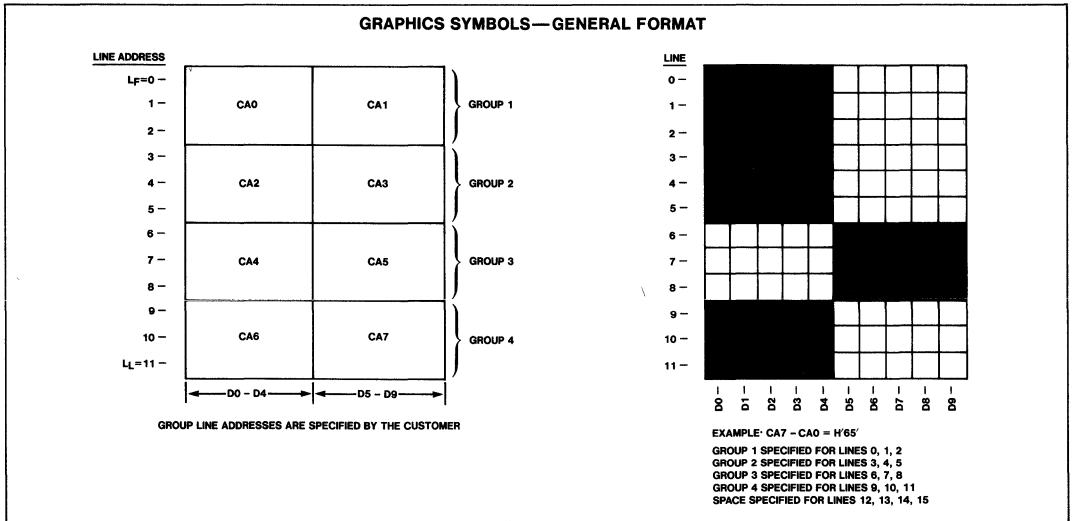


Figure 2

Preliminary

Output Inhibit Control

The output inhibit control logic operates only if GM=0. It causes the output of the line select multiplexers to be logic zero if the SCD input is high and CA6 and CA5 of the latched character address are 00. If the SCD input is low, normal operation occurs. (This feature is useful in ASCII coded applications to selectively disable character generation for non-displayable characters such as line feed, carriage return, etc.)

Line Address Latch

The line address latch is a 4-bit latch used to store the line address (LA0-LA3). The data is stored on the negative edge of the LSTROBE input.

Line Address Translation ROM

This 32X10 ROM translates the 5-bit code consisting of the 4 outputs from the line address latch and the descend control bit from the ROM into a 1-of-10 code for the line select multiplexers. Programming information provided by the customer specifies the address which selects each line of ROM data for both shifted and non-shifted characters. Thus, there are nine line addresses which select ROM data for unshifted characters and nine addresses for shifted characters. These combinations are usually specified by the customer in either ascending or descending order. For the remaining 14 codes (7 each for unshifted and shifted characters), the translation ROM forces zeros at the outputs of the line select multiplexers.

This circuitry only operates if GM=0. When GM=1, the line select multiplexers are forced to select the outputs from the graphics logic.

Figure 4 shows an example of data outputs where the customer has specified line 14 as the first line for unshifted characters, line 11 as the first line for shifted characters and line address combinations in descending order.

CUSTOM PATTERN PROGRAMMING INSTRUCTIONS

A computer-aided technique utilizing punched computer cards is employed to specify a custom version of the 2670. This technique requires that the customer supply Signetics with a deck of standard 80-column computer cards describing the data to be stored in the ROM array, the programmable line address translation ROM, thin graphics option, and the graphics line font translation ROM.

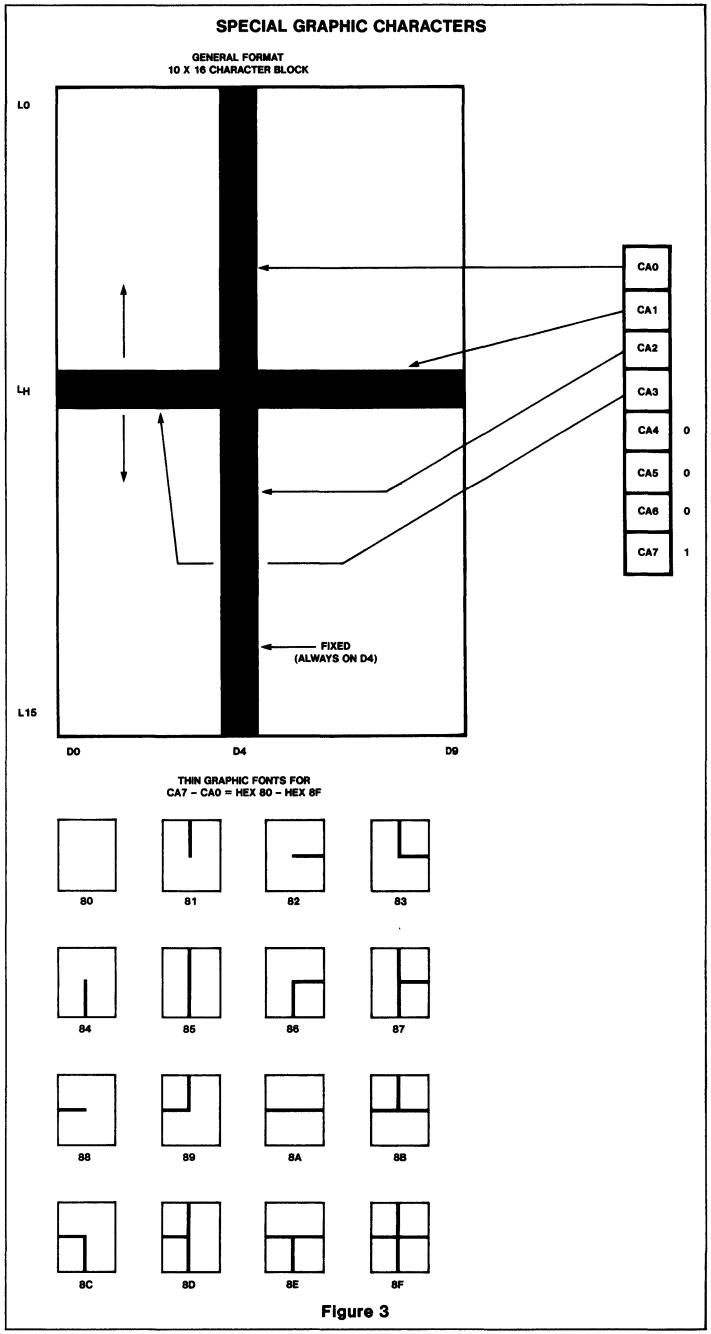


Figure 3

Preliminary

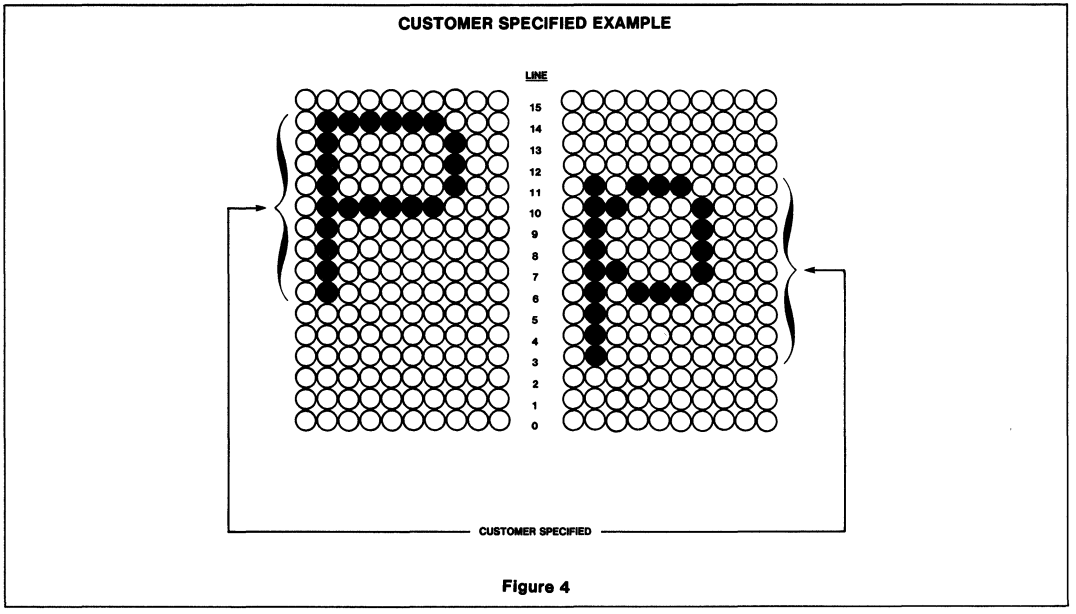


Figure 4

On receipt of a card deck, Signetics will translate the card deck to a truth table using the Signetics Computer Aided Design (CAD) facility. The truth table and font diagrams will then be sent to the customer for final approval. On receipt of final approval, Signetics will produce masks and proceed with manufacturing.

Programming information can also be input on TTY 7-level tape as card images. Each card image must be terminated with a carriage return-line feed. An EOT character must signify the end of the data set.

Customer identification cards are always labeled with a C in column 1. For customer identification, four cards are required. Any number of additional customer identification cards are permitted. The following data should be included:

CUSTOMER ID CARD #1

COLUMN	DATA
1	C
2	blank
3-9	2670/CP
10-14	blank
15-70	Company name/ company part number
71-80	blank

CUSTOMER ID CARD #2

COLUMN	DATA
1	C
2	blank
3-70	Customer contact person name/ phone number
71-80	blank

CUSTOMER ID CARD #3

COLUMN	DATA
1	C
2	blank
3-70	Customer address
71-80	blank

CUSTOMER ID CARD #4

COLUMN	DATA
1	C
2	blank
3-70	Customer city, state, zip code
71-80	blank

CUSTOMER ID CARD #5 THRU N

COLUMN	DATA
1	C
2	blank
3-70	Any information desired
71-80	blank

Preliminary

The following masking information cards must be included:

Mask Information Card #1: Shift and Nonshift Character Translation Data

COLUMN	DATA
1-9	NONSHIFT=
10	Line address in hex which outputs the first font word for nonshifted ROM fonts
11	,
12	Line address in hex which outputs the second font word for nonshifted ROM fonts
13	,
14	third
15	,
16	fourth
17	,
18	fifth
19	,
20	sixth
21	,
22	seventh
23	,
24	eighth
25	,
26	ninth
27-29	blank
30-35	SHIFT=
36	Line address in hex which outputs the first font word for shifted ROM fonts
37	,
38	second
39	,
40	third
41	,
42	fourth
43	,
44	fifth
45	,
46	sixth
47	,
48	seventh
49	,
50	eighth
51	,
52	ninth
53-59	blank
60[1]	0 or 1
61-64	blank
65[2]	0 or 1
66-80	blank

NOTES
1 Column 60 specifies the font truth table horizontal format 0 specifies left to right printing of D0 thru D9 1 specifies D9 thru D0
2 Column 65 specifies the font truth table vertical printout format 0 specifies top to bottom printing of line address hex 0 thru F 1 specifies hex F thru 0

MASK INFORMATION CARD #2: Graphics Translation Data

COLUMN	DATA
1-14	THIN GRAPHICS=
15-17	YES or NOØ, where Ø = blank. Specifies whether graphics address hex 80 thru hex 8F will select the special thin graphics font.
18-19	blank
20-23	HOR=
24	The line address in hex for the horizontal segments of line graphics fonts. Leave blank if columns 15 thru 17 are NO
25-29	blank
30-45	Graphics group number 1 or 2 or 3 or 4 or blank. Columns 30 thru 45 correspond to line address hex 0 thru hex F respectively. The group number specified in each column will cause the graphics data generated by that group to be output at the corresponding line address. A blank specifies no data for that address.
46-80	blank

MASK INFORMATION CARD #3 THRU #130: ROM Font Data

COLUMN	DATA
1-2	Character address in hex (CA6 thru CA0)*
3	blank
4	S for shifted; N for nonshifted.
5	blank
6-8	Data for first ROM font word in hex (D9 thru D0).
9	blank
10-12	second
13	blank
14-16	third
17	blank
18-20	fourth
21	blank
22-24	fifth
25	blank
26-28	sixth
29	blank
30-32	seventh
33	blank
34-36	eighth
37	blank
38-40	ninth
41-80	blank

NOTE
*A separate card is required for each character address hex 00 thru hex 7F

Preliminary

Printouts

Signetics will translate the card deck to the following printouts to be submitted to the customer for approval:

- **A repeat of all customer information.**
- **A separate font drawing for each of the 128 ROM characters and 256 graphics fonts. The font drawings are positioned on a 10 × 16 matrix as specified by the customer's translation data.**

SAMPLE CARD DECK INPUT

```
SIGNETICS C  2670/CP1000PA  2670 TEST RUN  04/16/79

THIN GRAPHICS=YES  HOR=7      1111222233334444
NONSHIFT=1,2,3,4,5,6,7,8,9    SHIFT=3,4,5,6,7,8,9,A,B        0    0
00 N 022 026 02A n32 0AA 088 088 088 070        40 N 078 084 082 nCA 08A 072 002 084 078
01 N 01C 002 00C n10 08E 088 0F8 088 088        41 N 010 028 044 n82 082 0FE 082 082 082
02 N 01C 002 00C n10 08E 050 020 050 088        42 N 03E 044 084 n44 03C 044 084 044 03E
03 N 01E 002 00E n02 09E 050 020 050 088        43 N 078 084 002 n02 002 002 002 084 078
04 N 01E 002 00E n02 01E 0F8 020 020 020        44 N 03E 044 084 n84 084 084 084 044 03E
05 N 01E 002 00E n02 06E 090 090 0D0 0E0        45 N 0FE 002 002 n02 03E 002 002 002 0FE
06 N 00C 012 01E n12 092 050 030 050 090        46 N 0FE 002 002 n02 03E 002 002 002 002
07 N 00E 012 00E n12 00E 010 010 010 0F0        47 N 078 084 002 n02 002 0E2 082 0C4 088
08 N 00E 012 00E 012 0EE 010 060 080 070        48 N 082 082 082 n82 0FE 082 082 082 082
09 N 012 012 01E n12 012 0F8 020 020 020        49 N 07C 010 010 n10 010 010 010 010 07C
0A N 002 002 002 n1E 0F0 010 070 010 010        4A N 0E0 040 040 n40 040 040 042 042 03C
0B N 022 022 022 n14 008 0F8 020 020 020        4B N 082 042 022 n12 00A 016 022 042 082
0C N 01E 002 00E n02 0F2 010 070 010 010        4C N 002 002 002 n02 002 002 002 002 07E
0D N 01C 002 002 n02 07C 090 070 050 090        4D N 082 0C6 0AA n92 092 082 082 082 082
0E N 01C 002 00C n10 06E 090 090 090 060        4E N 082 082 086 n8A 092 0A2 0C2 082 082
0F N 01C 002 00C n10 0EE 040 040 040 0E0        4F N 038 044 082 n82 082 082 082 044 038
10 N 00E 012 012 n12 00E 010 010 010 0F0        50 N 07E 082 082 n82 07E 002 002 002 002
11 N 00E 012 012 n12 04E 060 040 040 0E0        51 N 038 044 082 n82 082 092 0A2 044 0B8
12 N 00E 012 012 n12 06E 090 040 020 0F0        52 N 07E 082 082 n82 07E 012 022 042 082
13 N 00E 012 012 n12 06E 080 060 080 070        53 N 078 084 002 n04 038 040 080 042 03C
14 N 00E 012 012 n12 04E 060 050 0F8 040        54 N 0FE 010 010 n10 010 010 010 010 010
15 N 012 016 01A n12 092 050 030 050 090        55 N 082 082 082 n82 082 082 082 044 038
16 N 01C 002 00C n10 08E 050 020 020 020        56 N 082 082 082 n44 044 028 028 010 010
17 N 01E 002 00E n02 07E 090 070 090 070        57 N 082 082 082 n82 082 092 092 0AA 044
18 N 01C 002 002 n02 01C 090 0P0 0D0 090        58 N 082 082 044 n28 010 028 044 082 082
19 N 01E 002 00E n02 01E 088 0D8 0A8 088        59 N 082 082 044 n28 010 010 010 010 010
1A N 01C 002 00C n10 07E 090 070 090 070        5A N 0FE 080 040 n20 010 008 004 002 0FE
1B N 01E 002 00E n02 01E 0E0 010 010 0E0        5B N 07C 004 004 n04 004 004 004 004 07C
1C N 01E 002 00E n02 0E2 010 060 080 070        5C N 000 002 004 n08 010 020 040 080 000
1D N 01C 002 01A n12 0EC 010 060 080 070        5D N 07C 040 040 n40 040 040 040 040 07C
1E N 00E 012 00E n0A 0F2 010 060 080 070        5E N 010 038 054 n10 010 010 010 010 010
1F N 012 012 012 n12 0EC 010 060 080 070        5F N 000 000 008 n04 0FE 004 008 000 000
20 N 000 000 000 n00 000 000 000 000 000        60 N 018 018 010 n20 000 000 000 000 000
21 N 010 010 010 n10 010 000 000 010 010        61 N 000 000 000 n3C 040 07C 042 042 0BC
22 N 028 028 028 n28 000 000 000 000 000        62 N 002 002 002 n3A 046 042 042 046 03A
23 N 028 028 0FE n28 028 028 0FE 028 028        63 N 000 000 000 n3C 042 002 002 042 03C
24 N 028 0FC 02A n2A 07C 0A8 0A8 07E 028        64 N 040 040 040 n5C 062 042 042 062 05C
25 N 004 08A 044 n20 010 008 044 0A2 040        65 N 000 000 000 n3C 042 07E 002 002 03C
26 N 00C 012 012 n0C 00C 012 0A2 042 0BC        66 N 030 048 008 n08 03E 008 008 008 008
27 N 018 018 008 n04 000 000 000 000 000        67 S 000 05C 062 n42 062 05C 040 042 03C
28 N 020 010 008 n08 008 008 008 010 020        68 N 002 002 002 n3A 046 042 042 042 042
29 N 008 010 020 n20 020 020 020 010 008        69 N 000 010 000 n18 010 010 010 010 038
2A N 000 010 054 n38 0FE 038 054 010 000        6A S 000 060 040 n40 040 040 040 044 038
2B N 000 010 010 n10 0FE 010 010 010 000        6B N 002 002 002 n22 012 00A 016 022 042
2C S 000 000 000 n00 000 018 018 008 004        6C N 018 010 010 n10 010 010 010 010 038
2D N 000 000 000 n00 0FE 000 000 000 000        6D N 000 000 000 n6A 096 092 092 092 092
2E N 000 000 000 n00 000 000 000 018 018        6E N 000 000 000 n3A 046 042 042 042 042
2F N 000 080 040 n20 010 008 004 002 000        6F N 000 000 000 n3C 042 042 042 042 03C
30 N 038 044 0C2 nA2 092 08A 086 044 038        70 S 000 03A 046 n42 046 03A 002 002 002
31 N 010 018 014 n10 010 010 010 010 07C        71 S 000 05C 062 n42 062 05C 040 040 040
32 N 07C 082 080 n40 038 004 002 002 0FE        72 N 000 000 000 n3A 046 002 002 002 002
33 N 07C 082 080 n80 070 080 080 082 07C        73 N 000 000 000 n3C 042 00C 030 042 03C
34 N 040 060 050 n48 044 0FE 040 040 040        74 N 000 008 008 n1C 008 008 008 048 030
35 N 0FE 002 002 n02 07E 080 080 082 07C        75 N 000 000 000 n42 042 042 042 062 05C
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37 N 0FE 080 080 n40 020 010 008 004 002        77 N 000 000 000 n82 082 092 092 092 06C
38 N 07C 082 082 n44 038 044 082 082 07C        78 N 000 000 000 n42 024 018 018 024 042
39 N 07C 082 082 nC2 0BC 080 080 042 03C        79 S 000 042 042 n42 062 05C 040 042 03C
3A N 000 000 000 n18 018 000 000 018 018        7A N 000 000 000 n7E 020 010 008 004 07E
3B S 000 018 018 n00 000 018 018 008 004        7B N 030 008 008 n08 004 008 008 008 030
3C N 020 010 008 n04 002 004 008 010 020        7C N 010 010 010 n00 000 000 010 010 010
3D N 000 000 000 nFE 000 000 0FE 000 000        7D N 018 020 020 n20 040 020 020 020 018
3E N 008 010 020 n40 080 040 020 010 008        7E N 000 000 000 n0C 092 060 000 000 000
3F N 07C 082 082 n80 060 010 010 000 010        7F N 0AA 054 0AA n54 0AA 054 0AA 054 0AA
```

DISPLAY CHARACTER AND GRAPHICS GENERATOR (DCGG) SC2670

Preliminary

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Supply voltage	6.0	V
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.3 to +6.0	V

NOTES
1 Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied
2 For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient (ceramic package)
3 This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge Nonetheless it is suggested that conventional precautions be taken to avoid applying any voltages larger than the maxima

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% [1,2,3]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage		0		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
V_{OL}	Output low voltage	I_O = 1.6mA	0		0.45	V
V_{OH}	Output high voltage	I_O = −100μA	2.4		V_{CC}	V
I_{IL}	Input leakage current	V_{IN} = 0 to 4.25V			10	μA
I_{OL}	Output leakage current	V_O = 0.4 to 4V			±10	μA
I_{CC}	Supply current	V_{CC} = 5.25V		50	100	mA
C_{IN}	Input capacitance	All other pins grounded			10	pF
C_{OUT}	Output capacitance				15	pF

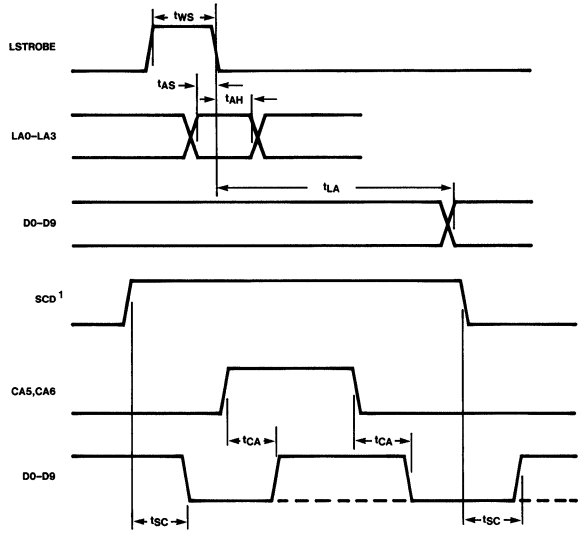
AC CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ± 5% [1,2,3]

PARAMETER		TENTATIVE LIMITS		UNIT
		Min	Max	
t_{WS}	Strobe pulse width	100		ns
t_{AS}	Address setup	50		ns
t_{AH}	Address hold	25		ns
t_{CA}	Character select access		300	ns
t_{LA}	Line select access		500	ns
t_{SEL}	Chip select delay[4]		250	ns
t_{DES}	Chip deselect delay[4]		200	ns
t_{SC}	Special character blank/unblank time		1	μs

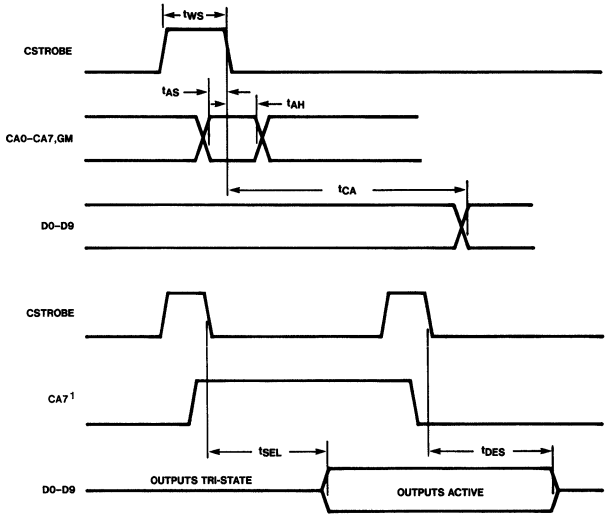
NOTES
1 Parameters are valid over operating temperature range unless otherwise specified
2 All voltage measurements are referenced to ground All time measurements are at 50% level for inputs and at the 0 8V or 2 0V level for outputs Input levels are 0 45V and 2 4V
3 Typical values are at +25°C, typical supply voltages and typical processing parameters
4 Test conditions C_L = 100pF and 1 TTL load

Preliminary

TIMING DIAGRAMS

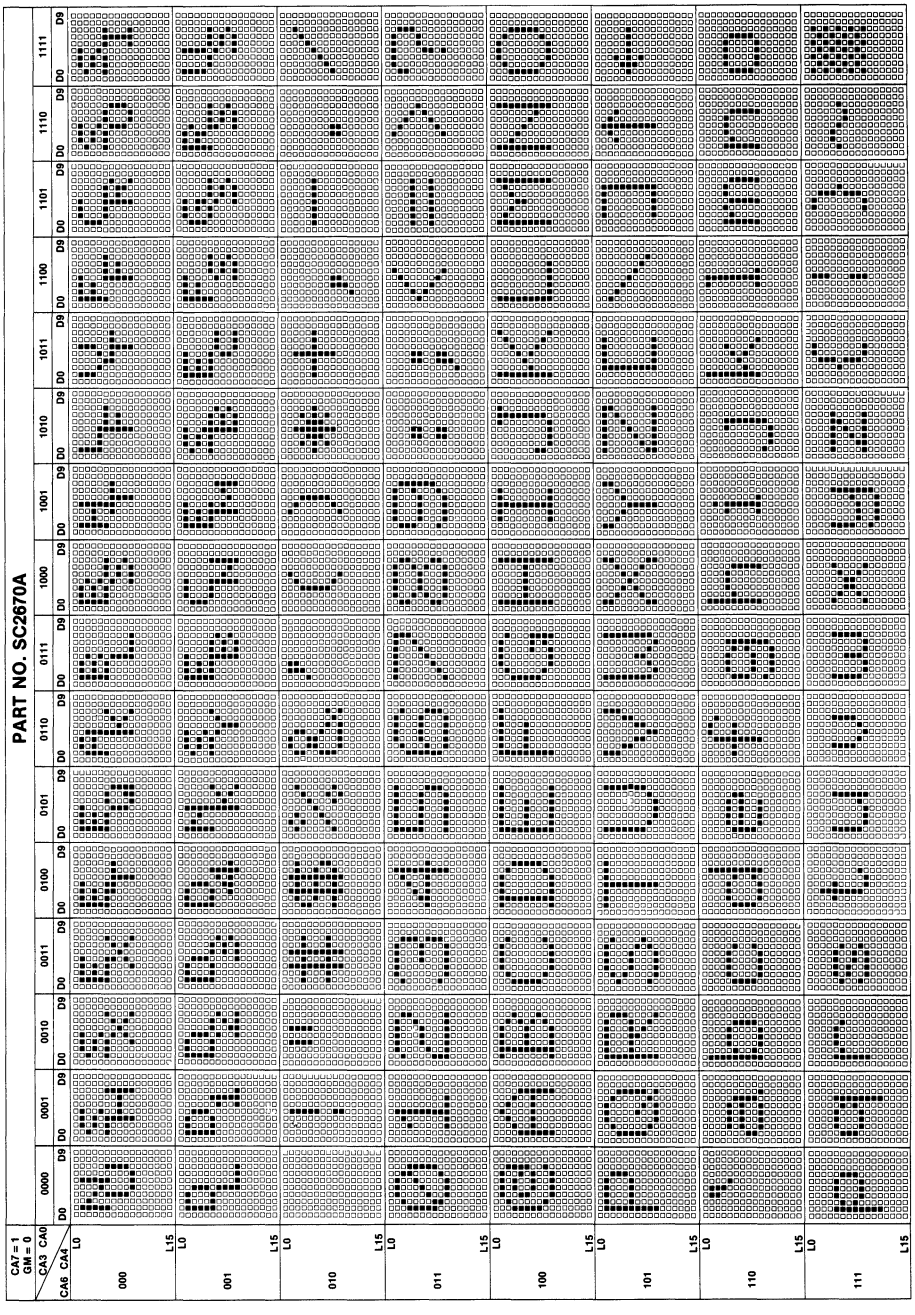


NOTE
1 WHEN GM=1, SCD INPUT IS INACTIVE



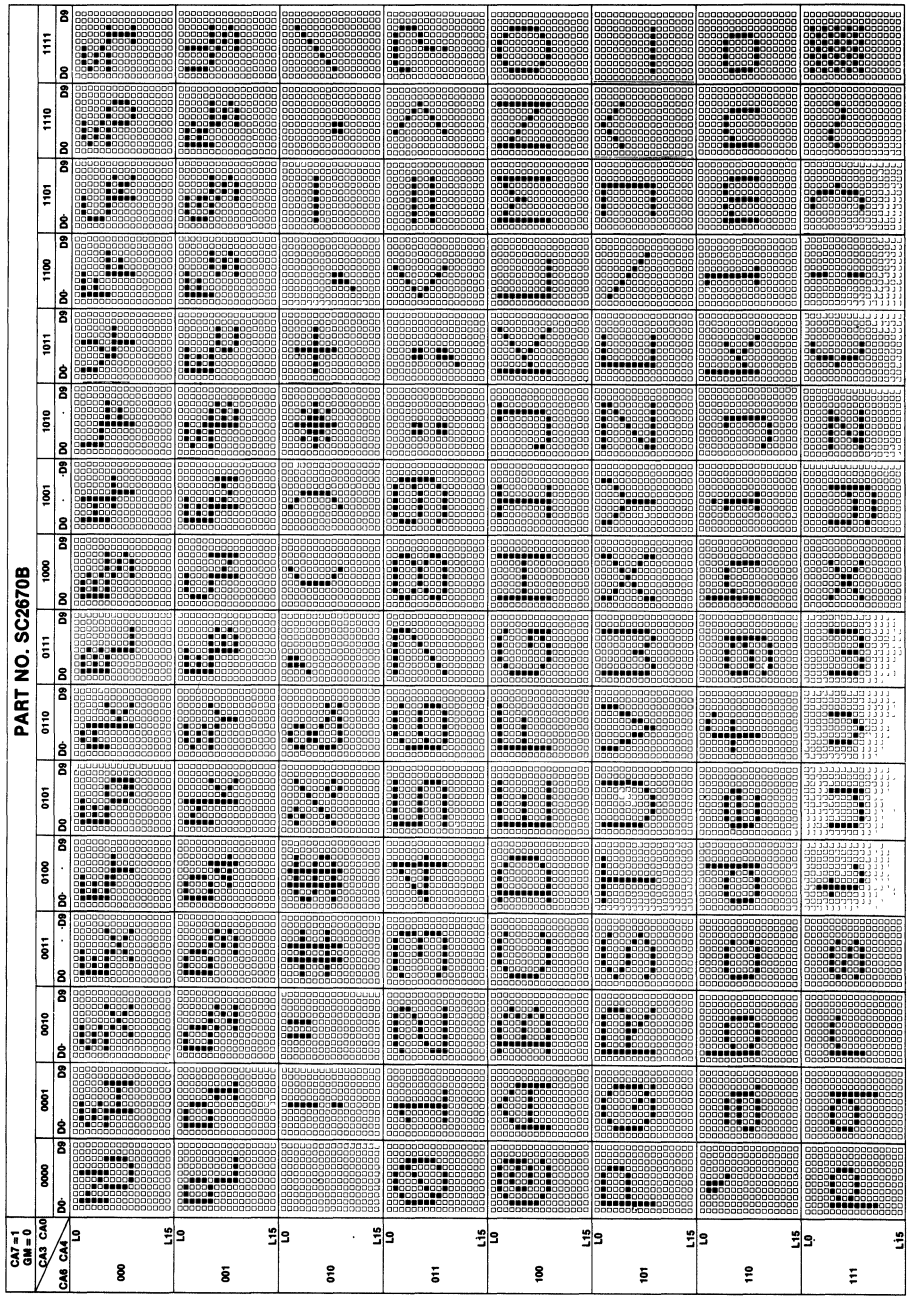
NOTE
1 CA7 OPERATES AS OUTPUT ENABLE ONLY IN CHARACTER MODE (GM=0)

Preliminary



DISPLAY CHARACTER AND GRAPHICS GENERATOR (DCGG) SC2670

Preliminary



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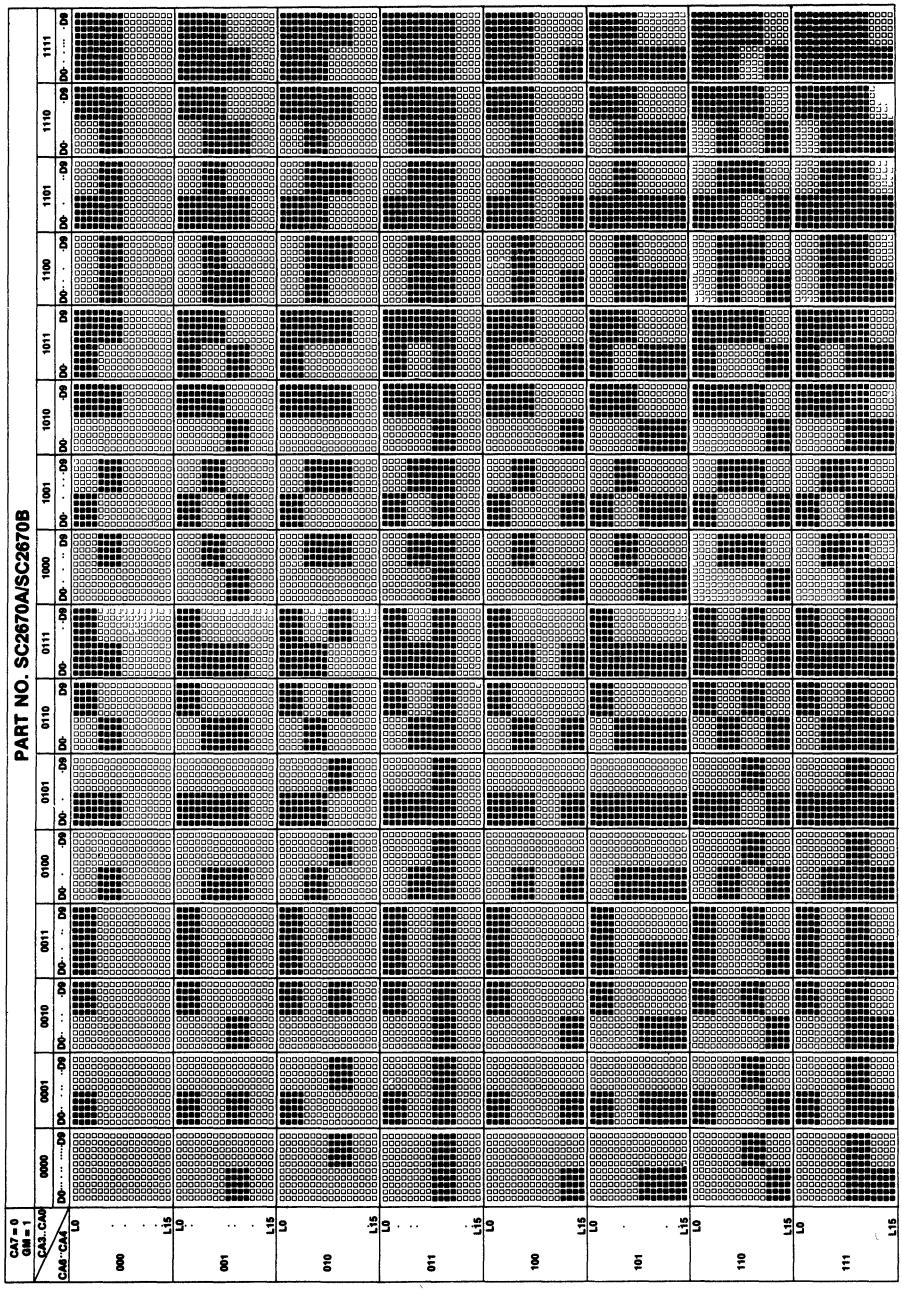
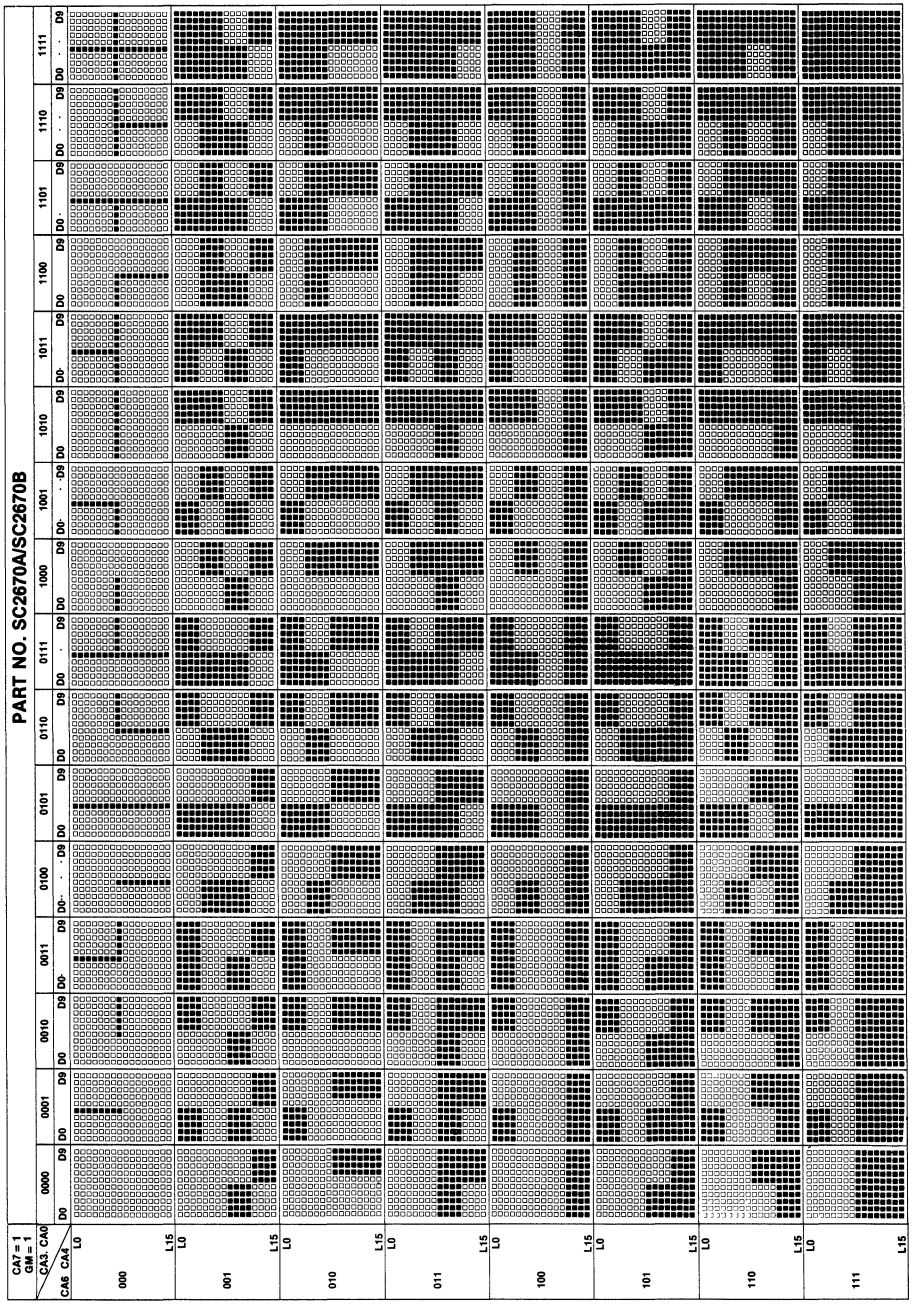


DISPLAY CHARACTER AND GRAPHICS GENERATOR (DCGG) SC2670

Preliminary



PROGRAMMABLE KEYBOARD & COMM CONTROLLER (PKCC) SC2671

Preliminary

DESCRIPTION

The Signetics 2671 Programmable Keyboard and Communications Controller (PKCC) is an MOS LSI device which provides a versatile keyboard encoder and an independent full duplex asynchronous communications controller. It is intended for use in microprocessor based systems and provides an eight bit data bus interface.

The keyboard encoder handles the scanning, debounce, and encoding of a keyboard matrix with a maximum of 128 keys. It provides four levels of key encoding corresponding to the separate SHIFT and CONTROL input combinations. Four keyboard rollover modes can be programmed including provisions for up to 16 latched keys. Control outputs are provided for interfacing with contact or capacitive keyboards. An eight bit keyboard status register provides status information to the CPU.

The receiver section of the communications controller accepts serial data from the RxD pin and converts it to parallel data characters. Simultaneously, the transmitter section accepts parallel data from the data bus and outputs serialized data onto the TxD pin. Received data is checked for parity and framing errors, and break conditions are flagged. Character lengths can be programmed as 5, 6, 7, or 8 bits not including parity, start or stop bits. An internal baud rate generator (BRG) with 16 divider ratios can be used to derive the receive and/or transmit clocks. The BRG can accept an external clock or operate directly from a crystal. An eight bit communications status register provides status information to the CPU.

The PKCC has an interrupt mask register to selectively enable certain keyboard and communications status bits to generate interrupts. Priority encoded interrupt vectoring is available. Upon receipt of an interrupt acknowledge, an interrupt vector will be output on D0-D7 reflecting the source of the interrupt. The interrupt source can also be read from an interrupt status register.

FEATURES

- **Keyboard interface**
  - **Contact or capacitive keyboard**
  - **Up to 128 keys on an 8 X 16 matrix**
  - **Encoded or unencoded operation**
  - **Four code levels per key**
  - **Latched key option—separate depress and release codes**
  - **Programmable scan rate and debounce time**
  - **Programmable rollover modes**
  - **Programmable auto-repeat for selected keys**
  - **Tone output—two frequencies**
- **Asynchronous communication interface**
  - **Internal baud rate generator—16 rates**
  - **Full duplex operation**
  - **Detection of start and end of break**
  - **Programmable break generation**
  - **Programmable character parameters**
  - **Auto-echo and maintenance loopback modes**
- **Polled or interrupt operation**
- **Interrupt priority controller and vector generator**
- **Operates directly from crystal or external clocks**
- **TTL compatible**
- **Single +5 volt power supply**
- **40 pin dual in-line package**

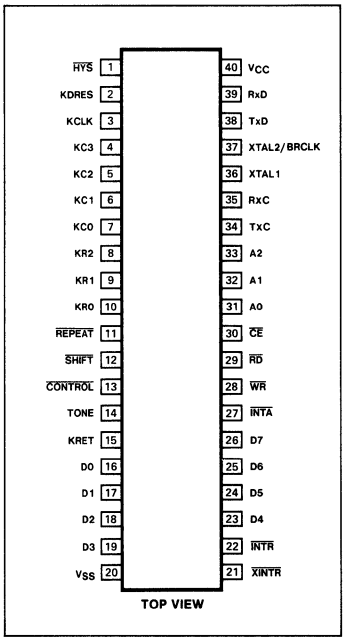
APPLICATIONS

- **CRT terminals**
- **Hard copy terminals**
- **Word processing systems**
- **Data entry terminals**
- **Small business computers**

FUNCTIONAL DESCRIPTION

The PKCC consists of six major sections (see block diagram). These are the transmitter, receiver, timing, operation control, keyboard encoder, and a priority encoded interrupt control unit. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a bidirectional data bus buffer.

PIN CONFIGURATION



TOP VIEW

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers KMR and CMR, the command decoder, and status registers KSR and CSR. Details of operating modes and status information are presented in the Operation section of this data sheet. The register addressing is specified in table 1.

Timing

The PKCC contains a baud rate generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 baud rates, any of which can be selected for full duplex operation. The external clock to the baud rate generator can be applied directly to the XTAL2 input (see figure 21) or can be generated internally by connecting a crystal across the XTAL1, XTAL2 input pins. The clock input is also utilized by the keyboard encoder section. Thus, a clock must be provided even if external transmitter and receiver clocks are used.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC}= 5V ±5%, T_A= 0°C to 70°C
Ceramic DIP	SC2671ACSI40
Plastic DIP	SC2671ACSN40

PROGRAMMABLE KEYBOARD & COMM CONTROLLER (PKCC) SC2671

Preliminary

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
D0-D7	16-19, 23-26	I/O	**Data Bus:** 8-bit three-state bidirectional data bus. All data, command and status transfers are made using this bus. D0 is the least significant bit; D7 is the most significant bit.
A0-A2	31-33	I	**Address Lines:** Used to select internal PKCC registers or commands.
$\overline{RD}$	29	I	**Read Strobe:** When low, gates the selected PKCC register onto the data bus if $\overline{CE}$ is also low.
$\overline{WR}$	28	I	**Write Strobe:** When low, gates the contents of the data bus into the selected PKCC register if $\overline{CE}$ is also low.
$\overline{CE}$	30	I	**Chip Enable:** When high, places the D0-D7 output drivers in a three-state condition. If $\overline{CE}$ is low, data transfers are enabled in conjuction with the $\overline{RD}$ and $\overline{WR}$ inputs.
$\overline{INTR}$	22	O	**Interrupt Request:** Several conditions may be programmed to request an interrupt to the CPU. It is an active low open-drain output. This pin will be inactive after power on reset or a master reset command.
$\overline{INTA}$	27	I	**Interrupt Acknowledge:** Used to indicate that an interrupt request has been accepted by the CPU. When $\overline{INTA}$ goes low, the PKCC outputs an 8-bit address vector on D0-D7 corresponding to the highest priority interrupt currently active.
$\overline{XINTR}$	21	I	**External Interrupt:** An active low external interrupt input to the PKCC interrupt priority resolver.
TxC	34	I/O	**Transmitter Clock:** The function of this pin depends on bit 7 of the baud rate control register (BRR7). If external transmitter clock is selected (BRR7 = 0), it is an input for the transmitter clock. If internal transmitter clock is selected (BRR7 = 1), this pin is an output which is a multiple of the actual baud rate (1X, 16X) as selected by BRR5. The data is transmitted on the falling edge of TxC. It is an input after power on and after master reset or communications reset commands.
RxC	35	I/O	**Receiver Clock:** The function of this pin depends on BRR6. If external receiver clock is selected (BRR6 = 0), it is an input for the receiver clock. If internal receiver clock is selected (BRR6 = 1), this pin is an output which is a multiple of the actual baud rate (1X, 16X) as selected by BRR4. The received data is sampled on the rising edge of RxC. It is an input after power on and after master reset or communications reset commands.
TxD	38	O	**Transmitter Data:** This output is the transmitted serial data; the least significant bit is transmitted first. This pin is high after power on reset or a reset command that affects the transmitter.
RxD	39	I	**Receiver Data:** This input is the serial data input to the receiver. The least significant bit is received first.
XTAL1 XTAL2/BRCLK	36,37	I	**Connections for Crystal:** Provides an on-chip clock generator for the internal baud rate generator and the keyboard interface logic. If an external clock is provided, use XTAL2 as the clock input. See figures 20 and 21. All timing parameters such as keyboard scan time, tone frequency, and baud rate assume a clock input at the specified BRG input frequency. If this frequency is different, the timing parameters will vary proportionately.
KR0-KR2	10-8	O	**Keyboard Row Scan:** Decoded externally; selects one of eight rows.
KC0-KC3	7-4	O	**Keyboard Column Scan:** Decoded externally; selects one of 16 columns.
KRET	15	I	**Key Return:** An active high level indicates that the key being scanned is closed.
$\overline{SHIFT}$	12	I	**SHIFT Key:** Active low input from the SHIFT key. The combination of $\overline{SHIFT}$ and $\overline{CONTROL}$ inputs select one of four possible codes from the internal key encoding ROM.
$\overline{CONTROL}$	13	I	**CONTROL Key:** Active low input from the CONTROL key. The combination of $\overline{SHIFT}$ and $\overline{CONTROL}$ inputs select one of four possible codes from the internal key encoding ROM.

PIN DESIGNATION (Cont.)

$\overline{\text{REPEAT}}$	11	I	**REPEAT Key:** Active low input from the $\overline{\text{REPEAT}}$ key. Causes the key depression currently active to be repeated at a rate of approximately 15 times per second.
KCLK	3	O	**Keyboard Clock:** High frequency (approximately 400 kHz) output used to scan capacitive keyboards.
KDRES	2	O	**Key Detect Reset:** Resets the analog detector before scanning a key. Used for capacitive keyboards.
$\overline{\text{HYS}}$	1	O	**Hysteresis Output:** Sent to the analog detector for capacitive keyboard applications. A low indicates the key currently being scanned has been recognized on previous scan cycles.
TONE	14	O	**Square Wave Output:** Used for tone generation.
V_{CC}	40	I	+5V power supply.
V_{SS}	20	I	Ground.

Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for break conditions, framing and parity errors, and loads an "assembled" character in the receive holding register for access by the CPU.

Transmitter

The transmitter accepts parallel data loaded by the CPU into the transmit holding register and converts it to a serial bit stream framed by the start bit, calculated parity bit (if specified), and stop bit(s). The composite serial stream of data is transmitted on the TxD output pin.

Keyboard Encoder

The keyboard encoder provides encoded scanning signals for a matrix keyboard. Key depressions are detected on the KRET input. The debounced and verified key codes (or matrix addresses) are loaded into the key holding register for access by the CPU. Figures 1 and 2 illustrate the PKCC interface to contact and capacitive keyboards, respectively.

Interrupt Control

The interrupt controller unit contains a software programmable interrupt mask register which selectively enables status conditions from the keyboard encoder and communication controller to generate interrupts. The interrupts are priority encoded and individually generate an eight bit vector which is output on the data bus in response to a CPU interrupt acknowledge on the $\overline{\text{INTA}}$ input pin.

$\overline{\text{CE}}$	A2	A1	A0	$\overline{\text{RD}}/\overline{\text{WR}}$	FUNCTION
1	X	X	X	X	Three-state data bus
0	0	0	0	$\overline{\text{WR}}$	Reset command (see table 6)
0	0	0	0	$\overline{\text{RD}}$	Read interrupt status register (ISR)
0	0	0	1	$\overline{\text{RD}}$, $\overline{\text{WR}}$	Read/write communications mode register (CMR)
0	0	1	0	$\overline{\text{WR}}$	Write transmit holding register (TxHR)
0	0	1	0	$\overline{\text{RD}}$	Read receiver holding register (RxHR)
0	0	1	1	$\overline{\text{WR}}$	Write baud rate mode register (BRR)
0	0	1	1	$\overline{\text{RD}}$	Read communications status register (CSR)
0	1	0	0	$\overline{\text{RD}}$,$\overline{\text{WR}}$	Read/write interrupt mask register (IMR)
0	1	0	1	$\overline{\text{RD}}$, $\overline{\text{WR}}$	Read/write keyboard mode register (KMR)
0	1	1	0	$\overline{\text{RD}}$	Read keyboard holding register (KHR)
0	1	1	1	$\overline{\text{RD}}$	Read keyboard status register (KSR)
0	1	1	1	$\overline{\text{WR}}$	Miscellaneous commands (see description)

NOTE
X = don't care.

Table 1. 2671 REGISTER ADDRESSING

OPERATION

Keyboard Encoder

The keyboard is continuously scanned by KC0-KC3 and KR0-KR2 which are decoded externally to handle 128 possible keys (see figures 1 and 2). KC0-KC3 select one of 16 columns and KR0-KR2 multiplex the eight row return lines into the KRET pin. Debouncing is accomplished by remembering a 1 state at the KRET pin when a key is being addressed and verifying it one scan later. Once the key is verified, a key code is loaded into the keyboard data register (KDR). If the keyboard holding register (KHR) is empty, the contents of the KDR will be transferred to the KHR immediately; if the KHR is full (i.e., the CPU has not read the previous key code), the transfer will be held off until the KHR is read. The data transfer to the KHR causes keyboard data ready (KRDY) to be set in the keyboard status register.

For capacitive keyboards, the high frequency output KCLK can be used to gate the column scan to the keyboard (see figure 2). The key detector reset (KDRES) output resets the analog detector prior to scanning each key location. The output from the analog multiplexer is sensed and then latched in the analog detector. The $\overline{\text{HYS}}$ output controls the sense level. A 0 will lower the sense level causing hysteresis, and a 1 will raise the sense level with no hysteresis.

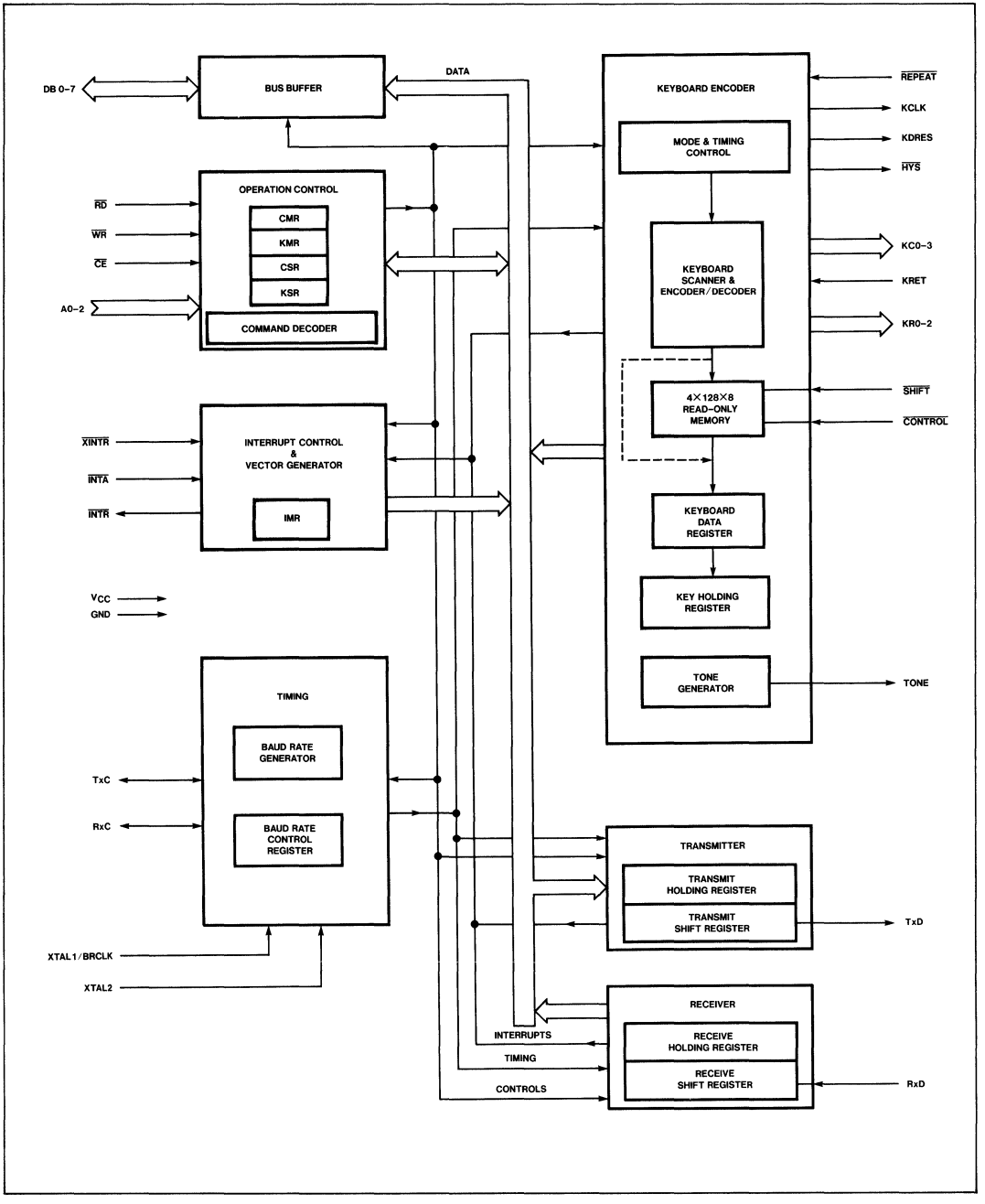
The $\overline{\text{REPEAT}}$ input enables the keyboard logic to recognize any key repeatedly, 15 times per second. Additionally, certain keys can be programmed to repeat automatically if depressed for more than one-half second.

A square wave is output on the TONE pin when the CPU issues a ring tone command to the PKCC.

PROGRAMMABLE KEYBOARD & COMM CONTROLLER (PKCC) SC2671

Preliminary

BLOCK DIAGRAM



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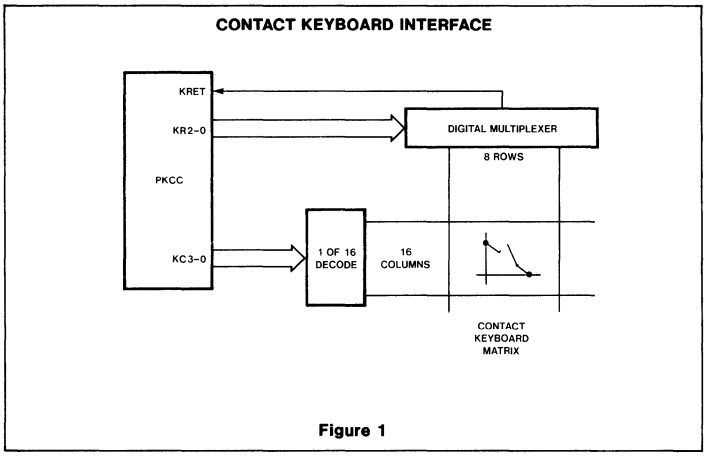


Figure 1

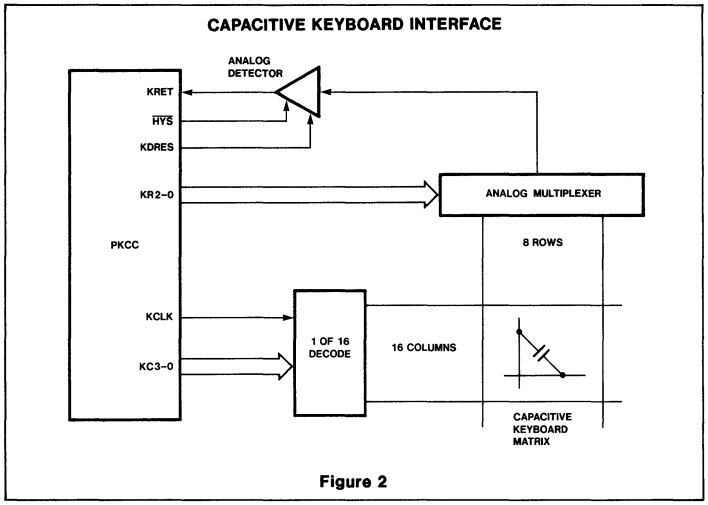


Figure 2

Keyboard Mode Register

Operating modes are selected by programming the keyboard mode register (KMR), whose format is illustrated in figure 3.

Bit KMR7 is used for testing the device. For normal operation, this bit should always be written to a 0.

Bits KMR6-KMR5 select the rollover modes for keyboard processing:

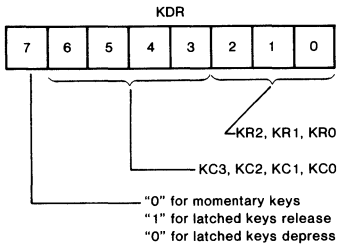
N-key Rollover: In this mode, the code corresponding to each key depression is loaded into the KDR as soon as that key is debounced, independent of the release of other keys. Two or more closures occurring within one scan cycle are considered to be simultaneous, which will set keyboard error in the keyboard status register (KSR1). As soon as the keyboard holding register is empty, the code in the KDR is transferred to the KHR and the KRDY status bit is set (KSR0).

N-Key Rollover With Latched Keys: This mode is the same as regular N-key rollover, except that the keys which are assigned to row 0 of the keyboard matrix (KR2-KR0 = 000) produce a code both when depressed and when released. The codes are independent of the states of the inputs at $\overline{\text{SHIFT}}$ and $\overline{\text{CONTROL}}$. If one or more of the latched keys are depressed when the keyboard is enabled (after a keyboard reset), the corresponding codes will be sent out as the keys are scanned and debounced. Note that simultaneous latched keys will not set KERR (KSR1) and that latched keys will not be auto-repeat and will not be affected by the $\overline{\text{REPEAT}}$ input.

Two-Key Rollover: The first key code is loaded into the KDR immediately and the second code is loaded only after the first key is released. Simultaneous keys will set KERR (KSR1). If three or more keys remain closed at any given time, the KERR bit will also be set. All keys must then be released before the next KRET will be processed.

Two-Key Inhibit: All keys must be released between keystrokes; otherwise, KERR (KSR1) will be set.

Bit KMR4 specifies the key encoding mode. Each key is assigned four 8-bit codes, corresponding to the states of the $\overline{\text{SHIFT}}$ and $\overline{\text{CONTROL}}$ inputs. If the encoded mode is programmed, the row/column address of the detected key is used to load one of the four key codes into the KDR. See table 2 for key code assignments. If the non-encoded mode is programmed, the row/column address is loaded directly into the KDR with the following format:



Preliminary

COLUMN (KC3-KC0)	ROW (KR2-KR0) 0	1	2	3	4	5	6	7
0	E0	C0	1B ESC	09 HT	1F US	1A SUB	30 0	2B +
	F0	D0	1B ESC	09 HT	1F US	1A SUB	30 0	3B ;
	E0	C0	1B ESC	09 * HT	1F US	5A Z	30 0	2B +
	F0	D0	1B ESC	09 * HT	1F US	7A z	30 0	3B ;
1	E1	C1	21 !	11 DC1	01 SOH	18 CAN	3D =	2A *
	F1	D1	31 1	11 DC1	01 SOH	18 CAN	2D —	3A :
	E1	C1	21 !	51 Q	41 A	58 X	3D * =	2A *
	F1	D1	31 1	71 q	61 a	78 x	2D * —	3A :
2	E2	C2	22 "	17 ETB	13 DC3	03 ETX	1E RS	1F US
	F2	D2	32 2	17 ETB	13 DC3	03 ETX	1E RS	1F US
	E2	C2	22 "	57 W	53 S	43 C	7E ~	7F * DEL
	F2	D2	32 2	77 w	73 s	63 c	5E ↑	5F * —
3	E3	C3	23 #	05 ENQ	04 EOT	16 SYN	1C FS	1B ESC
	F3	D3	33 3	05 ENQ	04 EOT	16 SYN	1C FS	1B ESC
	E3	C3	23 #	45 E	44 D	56 V	7C ¦	7B {
	F3	D3	33 3	65 e	64 d	76 v	5C \	5B [
4	E4	C4	24 $	12 DC2	06 ACK	02 STX	08 BS	1D GS
	F4	D4	34 4	12 DC2	06 ACK	02 STX	08 BS	1D GS
	E4	C4	24 $	52 R	46 F	42 B	08 * BS	7D }
	F4	D4	34 4	72 r	66 f	62 b	08 * BS	5D]
5	E5	C5	25 %	14 DC4	07 BEL	0E SO	10 DLE	08 BS
	F5	D5	35 5	14 DC4	07 BEL	0E SO	10 DLE	08 BS
	E5	C5	25 %	54 T	47 G	4E N	50 P	08 BS
	F5	D5	35 5	74 t	67 g	6E n	70 p	08 * BS
6	E6	C6	26 &	19 EM	08 BS	0D CR	00 NUL	09 HT
	F6	D6	36 6	19 EM	08 BS	0D CR	00 NUL	09 HT
	E6	C6	26 &	59 Y	48 H	4D M	60 '	09 * HT
	F6	D6	36 6	79 y	68 h	6D m	40 @	09 * HT
7	E7	C7	27 '	15 NAK	0A LF	3C <	7F DEL	20 SP
	F7	D7	37 7	15 NAK	0A LF	2C ,	7F DEL	20 SP
	E7	C7	27 '	55 U	4A J	3C <	7F DEL	20 * SP
	F7	D7	37 7	75 u	6A j	2C ,	7F DEL	20 * SP
8	E8	C8	28 (	09 HT	0B VT	3E >	0A LF	0B VT
	F8	D8	38 8	09 HT	0B VT	2E .	0A LF	0B VT
	E8	C8	28 (	49 I	4B K	3E >	0A LF	0B * VT
	F8	D8	38 8	69 i	6B k	2E .	0A LF	0B * VT
9	E9	C9	29)	0F SI	0C FF	3F ?	0D CR	0A LF
	F9	D9	39 9	0F SI	0C FF	2F /	0D CR	0A LF
	E9	C9	29)	4F O	4C L	3F ?	0D CR	0A * LF
	F9	D9	39 9	6F o	6C l	2F /	0D CR	0A * LF
A	EA	CA	37 7	34 4	31 1	30 0	A0	A6
	FA	DA	37 7	34 4	31 1	30 0	B0	B6
	EA	CA	37 7	34 4	31 1	30 0	A0	A6
	FA	DA	37 7	34 4	31 1	30 0	B0	B6
B	EB	CB	38 8	35 5	32 2	2E .	A1	A7
	FB	DB	38 8	35 5	32 2	2E .	B1	B7
	EB	CB	38 8	35 5	32 2	2E .	A1	A7
	FB	DB	38 8	35 5	32 2	2E .	B1	B7
C	EC	CC	39 9	36 6	33 3	BF	A2	A8
	FC	DC	39 9	36 6	33 3	AF	B2	B8
	EC	CC	39 9	36 6	33 3	9F	A2	A8
	FC	DC	39 9	36 6	33 3	8F	B2	B8
D	ED	CD	90	93	82	95	A3	A9
	FD	DD	90	93	82	95	B3	B9
	ED	CD	90	93	82 *	95	A3 *	A9 *
	FD	DD	90	93	82 *	95	B3 *	B9 *
E	EE	CE	91	80	84	81	A4	AA
	FE	DE	91	80	84	81	B4	BA
	EE	CE	91	80 *	84	81 *	A4 *	AA *
	FE	DE	91	80 *	84	81 *	B4 *	BA *
F	EF	CF	92	94	83	96	A5	AB
	FF	DF	92	94	83	96	B5	BB
	EF	CF	92	94	83 *	96	A5 *	AB *
	FF	DF	92	94	83 *	96	B5 *	BB *

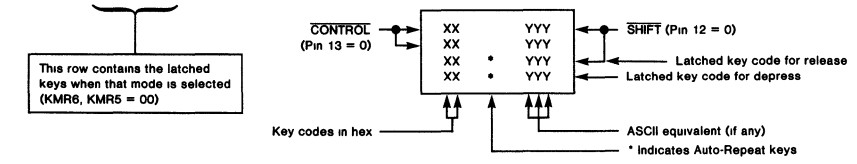


TABLE 2. Standard Key Codes (HEX)

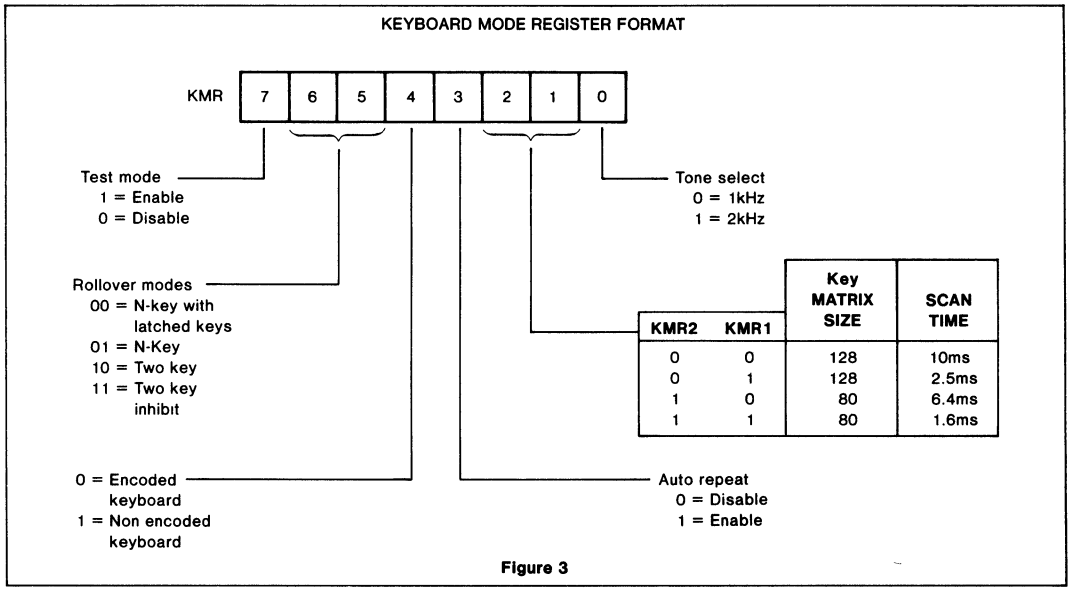


Figure 3

Bit KMR3 enables the auto-repeat mode. In this mode, if a key that is programmed for auto-repeat is depressed for longer than one-half second, the key code will be loaded into the KDR approximately 15 times per second until that key is released. Only the non-control key codes will auto-repeat, i.e. $\overline{\text{CONTROL}}$ = 1. Table 2 specifies the auto-repeat keys.

KMR2 and KMR1 select the key matrix size and debounce time (scan rate). The keyboard row outputs (KR2, KR1, KR0) always scan from 0 to 7. The column outputs (KC3, KC2, KC1, KC0) scan from 0 to 15 for a 128 key matrix and from 0 to 9 for an 80 key matrix.

KMR0 selects between a 1kHz and 2kHz frequency to be output on the TONE pin in response to a ring tone command.

Keyboard Status Register

The keyboard status register (KSR) provides operational feedback to the CPU. Its format is illustrated in figure 4.

KSR7, 6 and 4 reflect the state of the inputs at the corresponding pins. $\overline{\text{CONTROL}}$ and $\overline{\text{SHIFT}}$ are latched at the time the key is accepted. As the verified codes are loaded into the KDR, the corresponding states of $\overline{\text{CONTROL}}$ and $\overline{\text{SHIFT}}$ are loaded into the KSR. $\overline{\text{REPEAT}}$ is updated on every matrix sample. The status bits are the complements of the input levels.

KSR5 reflects the state of the internal shift lock flag which is controlled by the set/reset shift lock commands.

KSR3 indicates that the keyboard controller is enabled. It is controlled by the set/clear keyboard enable command.

Keyboard overrun (KSR2) is set when both the KHR and KDR are full and a third key is validated. The original content of the KHR is preserved and the content of the KDR is overwritten with the new key code. This bit can be specified (by IMR1) to generate an interrupt and is cleared by the reset command with D2 = 1.

Keyboard error (KSR1) is set when the operator depresses more keys than are allowed in the selected rollover mode, or when keys are depressed simultaneously (within one scan cycle). This bit can be specified (by IMR3) to generate an interrupt and is cleared by the reset command with D1 = 1.

Keyboard data ready (KSR0) is set when the key code or address is transferred from the KDR to the KHR. This bit can be specified (by IMR2) to generate an interrupt. It is cleared when the CPU reads the KHR.

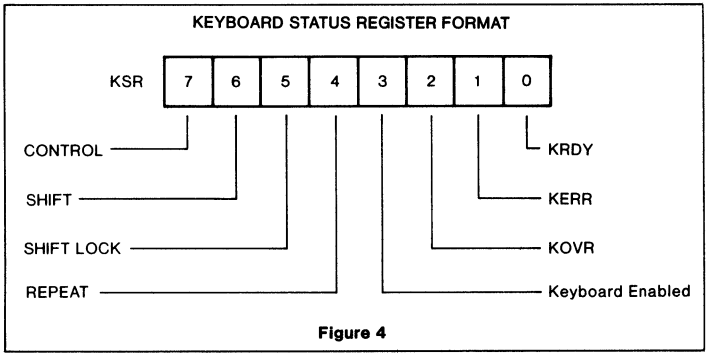


Figure 4

PROGRAMMABLE KEYBOARD & COMM CONTROLLER (PKCC) SC2671

Preliminary

Communications Controller

The communications controller section of the PKCC comprises a full duplex asynchronous receiver/transmitter (UART) with a baud rate generator. Registers associated with these elements are the communications mode register (CMR), the baud rate control register (BRR), and the communications status register (CSR).

Receiver

The receiver accepts serial data on the RxD pin, converts the serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition, and presents the assembled character to the CPU. The receiver looks for a high to low (mark to space) transition of the start bit on the RxD input pin. If a transition is detected, the state of the RxD pin is sampled again after a delay of one half of the bit time. If RxD is then high, the start bit is invalid and the search for a valid start bit begins again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input at one bit time intervals at the theoretical center of the bit, until the proper number of data bits and the parity bit (if any) have been assembled, and one stop bit has been detected. The least significant bit is received first. The data is then transferred to the receive holding register (RxHR) and the RxRDY bit in the CSR is set to a 1. If the character length is less than eight bits, the most significant unused bits in the RxHR are set to zero.

After the stop bit is detected, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e. framing error) and RxD remains low for one half of the bit period after the stop bit was sampled, then the space is interpreted as a start bit.

The parity error, framing error and overrun error (if any) are strobed into the CSR at the received character boundary. If a break condition is detected (RxD is low for the entire character including the stop bit) only one character consisting of all zeros will be transferred to the RxHR and the received break bit in the CSR is set to 1 (RxRDY is not set when a break is received). The RxD input must return to a high condition for one bit time before a search for the next start bit begins.

Transmitter

The transmitter accepts parallel data from the CPU and converts it to a serial bit stream on the TxD output pin. It automatically sends a start bit followed by the data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Following the transmission of the stop bits, if a new character is not available in the transmit holding register (TxHR), the TxD output remains high and the TxEMT bit in the CSR will be set to 1. Transmission resumes and the TxEMT bit is cleared when the CPU loads a new character into the TxHR. The transmitter can be forced to send a continous low condition by a transmit break command.

If the transmitter is disabled, it continues operating until the character currently being transmitted is completely sent out.

Communication Mode Register

Figure 5 illustrates the bit format of the CMR, which controls the operational mode of the communications controller and the character parameters.

Bits CMR1-CMR0 select a character length of 5, 6, 7, or 8 bits. The character length does not include the parity, start, or stop bits.

CMR2 selects the transmitted character framing as one or two stop bits. The receiver always checks for one stop bit.

The parity format is selected by bits CMR4 and CMR3. If parity or force parity is selected, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. CMR5 selects odd or even parity and determines the polarity of the parity bit in the force parity mode.

The bits in the mode register affecting character assembly and disassembly (CMR5-CMR0) can be changed dynamically and affect the characters currently being assembled in RxSR and transmitted by TxSR. To affect assembly of a received character, the CMR must be updated within n −1 bit times of the receipt of that character's start bit. To affect a transmitted character, the CMR must be updated within n −1 bit times of transmitting that character's start bit. (n = the smaller of the new and old character lengths).

The UART can operate in one of four modes, as illustrated in figure 6. The operating modes are selected by bits CMR7 and CMR6, which should only be changed when both the transmitter and receiver are disabled. CMR7-CMR6 = 00 is the normal mode, with the transmitter and receiver operating independently. CMR7-CMR6 = 01 places the UART in the automatic echo mode, which automatically retransmits the received data. The following conditions are true while in automatic echo mode:

1. Data assembled by the receiver is automatically placed in the transmit holding register and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. Status bit TxRDY is not set. TxEMT operates normally.
5. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
6. Only the first character of a break condition is echoed; the TxD output will go high until the next received character is assembled.
7. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

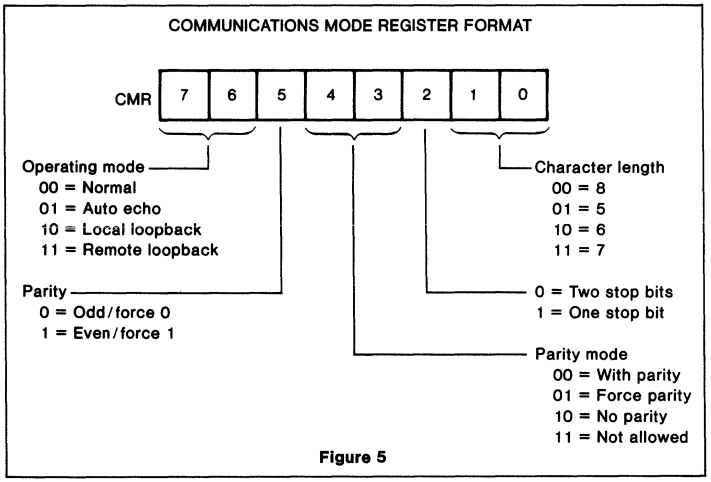
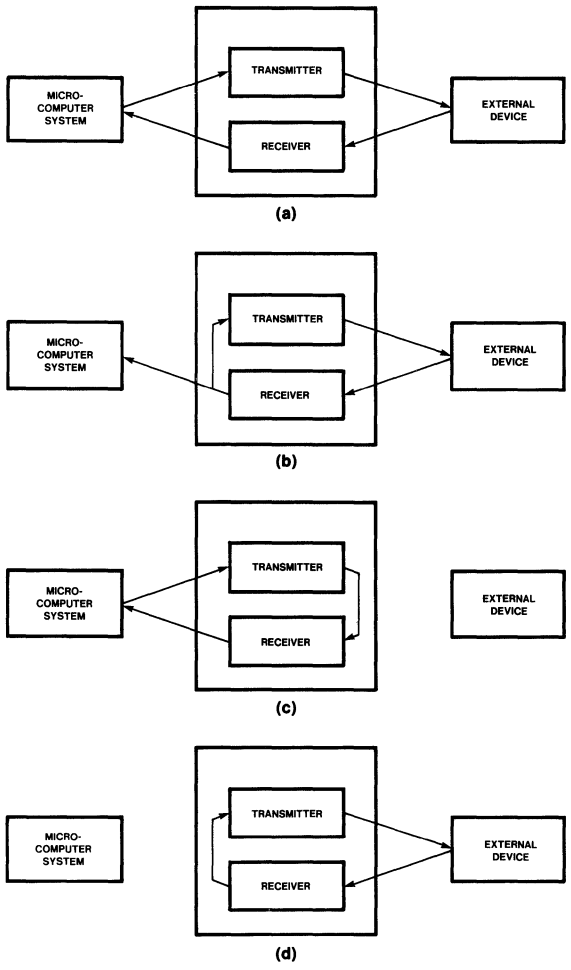


Figure 5



(a) Normal operating mode
(b) Automatic echo mode
(c) Local loopback mode
(d) Remote loopback mode

Figure 6

Two diagnostic modes can also be configured. In local loopback mode (CMR7-CMR6 = 10):

1. The transmitter output is internally connected to the receiver input.
2. The transmit clock is used for the receiver.
3. The TxD output is held high.
4. The RxD input is ignored.
5. The transmitter must be enabled, but the receiver need not be enabled.
6. CPU to transmitter and receiver communications continue normally.

The second diagnostic mode is the remote loopback mode (CMR7-CMR6 = 11). In this mode:

1. Data assembled by the receiver is automatically placed in the transmit holding register and retransmitted on the TxD output.
2. The receive clock is used for the transmitter.
3. No data is sent to the local CPU, but the error status conditions (parity and framing) are set if required.
4. The received parity is checked, but is not regenerated for transmission, i.e., transmitted parity bit is as received.
5. The receiver must be enabled, but the transmitter need not be enabled.

Baud Rate Control Register

The baud rate control register (BRR) controls the frequency generated by the baud rate generator (BRG) and the clock source used by the receiver and transmitter Its format is illustrated in figure 7.

BRR3-BRR0 select one of sixteen frequencies to be generated by the BRG. See table 3.

BRR7 and BRR6 select the source of the transmit and receive clocks. If external clocks are chosen, (BRR7 = 0 or BRR6 = 0), then the clock rate factor is determined by BRR5 and BRR4. The external clock input(s) should be the desired baud rate multiplied by the clock rate factor.

If internal clock(s) are specified, (BRR7 = 1 or BRR6 = 1), the clock is supplied by the internal baud rate generator at the selected baud rate. The clock rate factor for internally generated clocks is always 16. Pins 35 and 34 become outputs for transmit or receive clocks, respectively. See table 4 for the description and selection of these outputs.

BAUD RATE CONTROL REGISTER FORMAT

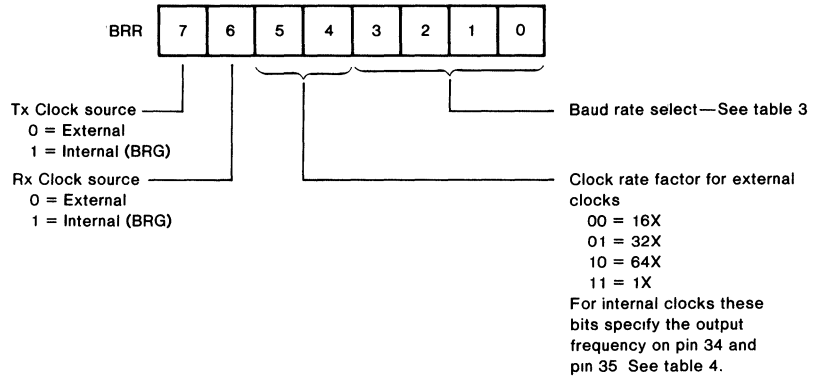


Figure 7

BRR3-0	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8 kHz	—	6144
0001	110	1.7598	−0.01	2793
0010	134.5	2.152	—	2284
0011	150	2.4	—	2048
0100	200	3.2	—	1536
0101	300	4.8	—	1024
0110	600	9.6	—	512
0111	1050	16.8329	+0.20	292
1000	1200	19.2	—	256
1001	1800	28.7438	−0.20	171
1010	2000	31.9168	−0.26	154
1011	2400	38.4	—	128
1100	4800	76.8	—	64
1101	9600	153.6	—	32
1110	19200	307.2	—	16
1111	38400	614.4	—	8

Table 3. BAUD RATE GENERATOR CHARACTERISTICS (BRCLK = 4.9152MHz)

BRR7-BRR4	CLOCK SOURCE TxC	CLOCK SOURCE RxC	PIN FUNCTIONS PIN 34	PIN FUNCTIONS PIN 35	BRR3-BRR0 BAUD RATE SELECTION
00**	E	E	TxC	RxC	The baud rates are listed in table 3.
01**	E	I	TxC	1X	
10**	I	E	16X	RxC	
1100	I	I	1X	1X	
1101	I	I	1X	16X	
1110	I	I	16X	1X	
1111	I	I	16X	16X	

NOTES

1 ** = Clock rate factor for external clocks 00 = 16X
01 = 32X
10 = 64X
11 = 1X

2 E = External clock.

3. I = Internal clock (BRG)

4 1X and 16X are clock outputs at 1 or 16 times the actual baud rate For receive, the 1X output is the actual data sample clock

5 BRR7-BRR6 = 01 or 10 not permitted in automatic echo or remote loopback modes unless BRR5-BRR4 = 00

Table 4. BAUD RATE CONTROL REGISTER

Communications Status Register

Figure 8 illustrates the bit format of the communications status register (CSR), which provides UART status to the CPU.

Receiver ready (CSR0) indicates that a received character is assembled and transferred to the RxHR and is ready to be read by the CPU. This bit can be specified (by IMR0) to generate an interrupt and is reset by reading the RxHR.

Transmitter ready (CSR1) indicates that the TxHR is empty and ready to be loaded with a character. This bit will be cleared when the TxHR is loaded and has not yet transferred the character to the transmit shift register (TxSR). TxRDY is reset when the transmitter is disabled. It will be set when the transmitter is enabled, provided that no data was loaded into the TxHR during the time the transmitter was disabled. This bit can be specified (by IMR7) to generate an interrupt.

Transmitter empty (CSR2) indicates that the transmitter has underrun, i.e., both the TxHR and TxSR are empty. This bit can only be set after transmission of at least one character, and is cleared when the TxHR is loaded by the CPU. TxEMT is reset when the transmitter is disabled. This bit can be specified (by IMR6) to generate an interrupt.

CSR3 will be set when the PKCC receives a command to transmit a break. This bit will be cleared after the break is completed.

Received break (CSR4) indicates that an all zero character of the programmed length has been received without a stop bit. Breaks originating in the middle of a received character can be detected. This bit is cleared when RxD returns to a high state for at least one bit time.

Receiver overrun (CSR5) indicates that the previous character in the RxHR has not been read by the CPU and that a new character has been loaded into the RxHR. This bit is cleared by a reset command with D3 = 1.

Framing error (CSR6) indicates that the stop bit has not been detected. The stop bit check is made in the middle of the first stop bit position. This bit is cleared by a reset command with D3 = 1.

Parity error (CSR7) indicates that a character was received with incorrect parity when 'with parity' or 'force parity' is enabled. This bit is cleared by a reset command with D3 = 1.

Interrupt Controller

The 2671 contains a maskable interrupt status register (ISR) which can be enabled to generate an active low interrupt request on the $\overline{INTR}$ output. The eight interrupt conditions in the ISR are individually enabled by writing a 1 into the corresponding bit of the interrupt mask register (IMR).

Each of the interrupt conditions is assigned a priority and a vector. When an enabled ISR bit is set, the 2671 asserts the $\overline{INTR}$ output. If the CPU activates the $\overline{INTA}$ input, the 2671 responds by placing the corresponding 8-bit vector on the data bus (D7-D0). If multiple interrupts are pending, the vector corresponds to the condition with the highest priority. The interrupt will persist until all pending interrupt conditions are cleared.

The ISR can also be polled by reading at address A2-A0 = 000. All pending interrupt conditions which are enabled by the IMR will be read independent of priority.

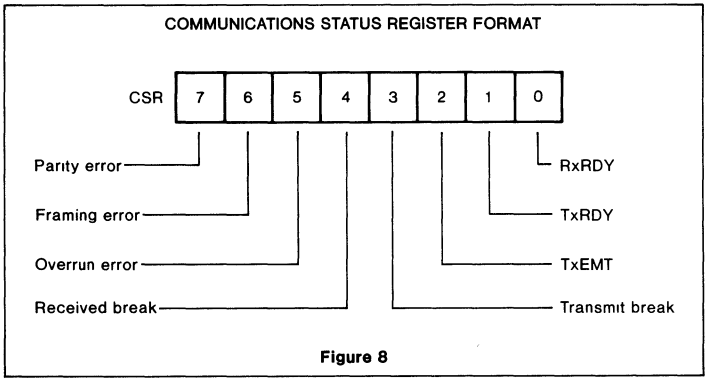


Figure 8

The bit assignments of the ISR and IMR and corresponding vectors and priorities are listed in table 5.

COMMANDS

In addition to the control exercised by programming of the PKCC control registers, several functions can be performed by executing command operations. There are two classes of commands which are initiated by writing to the 2671 at address A2-A0 = 000 (reset command) and address A2-A0 = 111 (miscellaneous commands). Individual commands are specified by the bit pattern on the data bus (D7-D0).

Reset Commands

The reset command bit format is illustrated in figure 9 and the detail command descriptions are given in table 6.

A reset command with D7-D0 = 111XXXX1 is a master reset for the 2671. This command must be given following a power on condition to release the internal power on reset latch which deactivates the 2671 on power up.

Miscellaneous Commands

The miscellaneous command format is illustrated in figure 10.

The transmit break commands force a break (steady low output) on the TxD pin immediately or after the character in the TxSR (if any) is transmitted. A timed break lasts for approximately 200ms, and a character break lasts for one character time including parity and stop bit time. In either case, TxRDY (CSR1) will be set at the beginning of the break which can be extended indefinitely (by 200ms or one character time increments) by reasserting the command in response to TxRDY. Note that these commands reset TxRDY. When a transmit break command is asserted, CSR3 will be set. This bit will be cleared after the break is completed.

The ring tone commands cause the tone generator to output a square wave on the TONE output . The tone durations are specified by the commands:

Ring tone short = 25ms
Ring tone long = 100ms

The tone frequency is either 1kHz or 2kHz, as specified by KMR0.

BIT IN IMR/ISR	INTERRUPT CONDITION	PRIORITY	VECTOR ON D7-D0 BINARY	HEX	CONDITION RESET BY:
IMR0/ISR0	RxRDY	1	11001111	CF	Read RxHR
IMR1/ISR1	KOVR	2	11010111	D7	Reset CMD (D2 = 1)
IMR2/ISR2	KRDY	3	11011111	DF	Read KHR
IMR3/ISR3	KERR	4	11100111	E7	Reset CMD (D1 = 1)
IMR4/ISR4	XINT[1]	5	11101111	EF	External
IMR5/ISR5	ΔBREAK[2]	6	11110111	F7	Reset CMD (D4 = 1)
IMR6/ISR6	TxEMT	7	11000111	C7	Load TxHR
IMR7/ISR7	TxRDY	8	11000111	C7	Load TxHR

NOTES
1 XINT is an input from an external interrupt source, active low (pin 21).
2 ΔBREAK refers to the change of a received break condition

Table 5. INTERRUPT MASK REGISTER (IMR) AND INTERRUPT STATUS REGISTER (ISR)

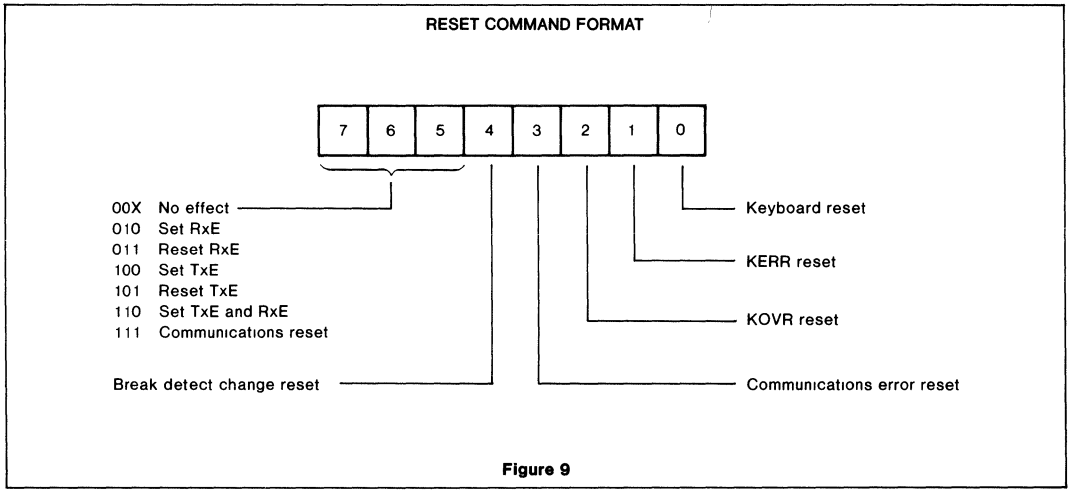


Figure 9

COMMAND	RESETS	COMMENTS
Keyboard reset	KMR7-KMR0 KSR5, KSR3-KSR0 IMR3-IMR1	The keyboard controller is reset, ignoring the input at KRET.
KERR reset	KSR1	Keyboard error status bit reset.
KOVR reset	KSR2	Keyboard overrun status bit reset.
Communications error reset	CSR7-CSR5	Resets the receiver overrun, parity, and framing error status bits.
Break detect change reset	ISR5	Resets the break detect change bit in the interrupt status register.
Set RxE	See note.	Enables receiver operation.
Reset RxE	CSR7-CSR4, CSR0 See note.	Disables the receiver
Set TxE	See note.	Enables transmitter operation
Reset TxE	CSR3-CSR1 See note.	Disables the transmitter Sets the TxD output to a 1 after transmitting the character in TxSR.
Communications reset	CMR, CSR, BRR, TxE, RxE, IMR7-IMR5, IMR0	Resets the communication controller. The RxD input is ignored and the TxD output is set to a 1.
Master reset	CMR, CSR, BRR, TxE, RxE, KMR, KSR5, KSR3-KSR0, IMR7-IMR0. Releases the internally latched power on reset.	Resets the keyboard and communication controllers. Inputs at KRET and RxD are ignored and the TxD output is set to a 1.

NOTE
Command does not affect the CMR or the BRR

Table 6. RESET COMMAND DESCRIPTION

The set/clear shift lock commands control the state of the internal shift lock flip flop. When shift lock is set, the keyboard controller encodes all key depressions as if the $\overline{\text{SHIFT}}$ input was asserted. The state of the shift lock flip flop is reflected in KSR5.

The set keyboard enable command enables the keyboard controller and sets KSR3 in the keyboard status register. The clear keyboard enable command resets KSR3 and disables key processing at the KRET input. The keyboard controller is not reset by this command, and the current state of the keyboard (key depressions and latched key states) is preserved internally When the keyboard is subsequently enabled, key processing resumes, old and new keys are debounced, and latched keys are encoded if there has been a change in their state.

MASK PROGRAMMABLE OPTIONS

Characteristics of certain portions of the PKCC are internally programmed by means of a read only memory. The items which can be programmed are·

- Key codes
- Auto-repeat keys
- Scan times, tone frequency, and tone duration
- Baud rates
- Interrupt vectors

Consult your local Signetics representative for costs, minimum quantities, and data submission requirements for customized versions of the PKCC.

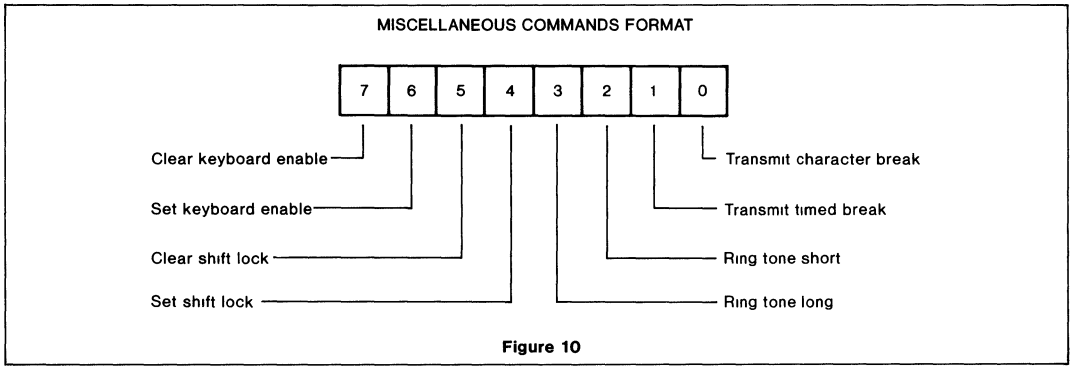


Figure 10

PROGRAMMABLE KEYBOARD & COMM CONTROLLER (PKCC) SC2671

Preliminary

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.5 to +6.0	V

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±5%[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage	Except XTAL1 (see note 13)	2.0			V
V_{OL}	Output low voltage	I_{OL} = 1.6mA			0.4	V
V_{OH}	Output high voltage (except $\overline{INTR}$)	I_{OH} = −100μA	2.4			V
I_{IL}	Input leakage current	V_{IN} = 0 to V_{CC}	−10		10	μA
I_{LL}	Data bus 3-state leakage current	V_O = 0 to V_{CC}	−10		10	μA
I_{CC}	Power supply current				150	mA

AC ELECTRICAL CHARACTERISTICS T_A = 0° to +70°C, V_{CC} = 5V ±5%[4,5,6]

PARAMETER		TEST CONDITIONS	TENTATIVE LIMITS			UNIT
			Min	Typ	Max	
Read timing[7]						
t_{AS}	Address setup to $\overline{RD}$		50			ns
t_{CS}	$\overline{CE}$ setup to $\overline{RD}$		50			ns
t_{PW}	$\overline{RD}$ pulse width		250			ns
t_{AH}	Address hold from $\overline{RD}$		20			ns
t_{CH}	$\overline{CE}$ hold from $\overline{RD}$		0			ns
t_{DD}	Data delay for read	C_L = 150pF			200	ns
t_{DF}	Data bus floating time for read	C_L = 150pF	10		100	ns
t_{AD}	Access delay from any read to next read or write		250			ns
Write timing[8]						
t_{AS}	Address setup to $\overline{WR}$		50			ns
t_{CS}	$\overline{CE}$ setup to $\overline{WR}$		50			ns
t_{PW}	$\overline{WR}$ pulse width		250			ns
t_{AH}	Address hold from $\overline{WR}$		20			ns
t_{CH}	$\overline{CE}$ hold from $\overline{WR}$		0			ns
t_{DS}	Data setup		100			ns
t_{DH}	Data hold		0			ns
t_{AD}	Access delay from any write to next read or write		250			ns
t_{AD}	Access delay from reset command to next read or write		1.0			μs

NOTES

1 Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied

2 For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 55°C/W junction to ambient (IWA ceramic package)

3 This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima

4. Parameters are valid over operating temperature range unless otherwise specified.

5 All voltage measurements are referenced to ground (V_{SS}). All input signals swing between 0.4V and 2 4V with a transition time of 20ns maximum and time measurements are referenced at input voltages of 0.8V, 2 0V and at output voltages of 0.8V, 2.0V as appropriate, unless otherwise specified

6 Typical values are at +25°C, typical supply voltages and typical processing parameters

7. See figure 11.

8 See figure 12.

Preliminary

AC ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER		TEST CONDITIONS	TENTATIVE LIMITS			UNIT
			Min	Typ	Max	
Interrupt acknowledge timing[9]						
t_{PWI}	$\overline{INTA}$ pulse width		300			ns
t_{DDI}	Data delay time for interrupt vector	C_L = 150pF			250	ns
t_{DFI}	Data bus floating time after $\overline{INTA}$	C_L = 150pF	10		100	ns
t_{ADI}	$\overline{INTA}$ to $\overline{INTA}$ access delay		300			ns
$\overline{INTR}$ reset timing[10]						
t_{RI}	$\overline{INTR}$ delay from:					
	Read RxHR (RxRDY)				400	ns
	Read KHR (KRDY)				400	ns
	Reset commands (KOVR,KERR,BREAK)				450	ns
	Load TxHR (TxEMT,TxRDY)				400	ns
	Mask bit reset				300	ns
Keyboard timing[11]						
f_{KCLK}	KCLK frequency			409		kHz
t_{KBD}	KR_i, KC_j to KRET sample delay:					
	FAST SCAN		12.0			µs
	SLOW SCAN		55.0			µs
t_{POS}	Scan time per matrix position:					
	FAST SCAN			20		µs
	SLOW SCAN			80		µs
t_{KRD}	KDRES delay from KCLK	C_L = 150pF			400	ns
t_{KRH}	KDRES hold from KCLK	C_L = 150pF			400	ns
t_{HYSD}	$\overline{HYS}$ delay from KCLK	C_L = 150pF			600	ns
t_{RCD}	KR_i, KC_j delay from KCLK	C_L = 150pF			400	ns
UART timing[12]						
t_{RXS}	RxD setup time		200			ns
t_{RxH}	RxD hold time		200			ns
t_{TxD}	TxD delay from falling edge of TxC	C_L = 150pF			300	ns
t_{TCS}	Skew between TxD transition and falling edge of TxC output	C_L = 150pF		0		ns
t_{BRH}	XTAL1 clock high[13]		70			ns
t_{BRL}	XTAL1 clock low[13]		70			ns
f_{BRG}	BRG input frequency		1.0	4.9152	5.075	MHz
$f_{R/T}$	TxC or RxC input frequency	Clock rate factor = 16X, 32X, 64X			1.3	MHz
$f_{R/T}$	TxC or RxC input frequency	Clock rate factor = 1X			1.0	MHz
$t_{R/TH}$	TxC or RxC clock high		350			ns
$t_{R/TL}$	TxC or RxC clock low		350			ns

NOTES
9 See figure 13
10 See figure 14
11 See figure 15 and 16
12 See figure 17, 18, and 19.
13 See figures 20 and 21 for XTAL1, XTAL2 connections for driving XTAL2 with an external clock Input levels for XTAL1 and XTAL2 are $V_{IL} \leq 0.8V$, $V_{IH} \geq 4.0V$, and t_{BRL} and t_{BRH} are measured at these levels

READ TIMING

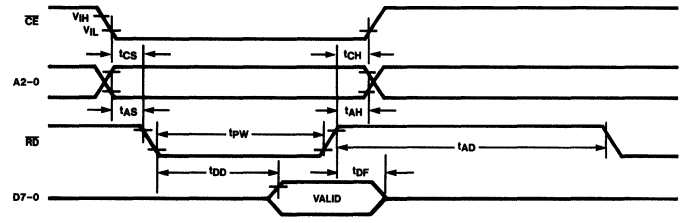


Figure 11

WRITE TIMING

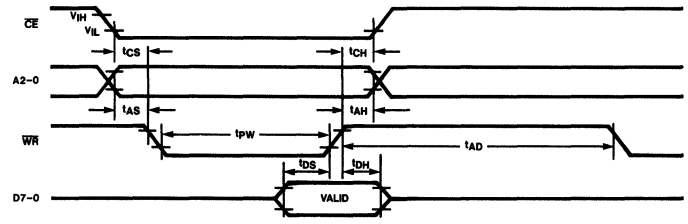


Figure 12

INTERRUPT ACKNOWLEDGE TIMING

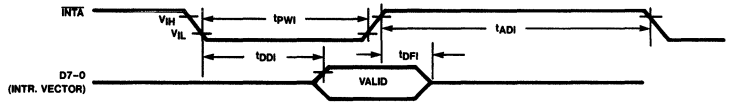


Figure 13

INTERRUPT RESET TIMING

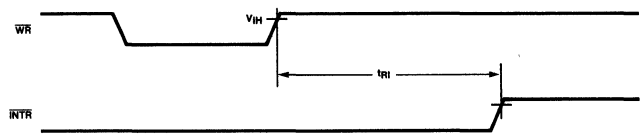
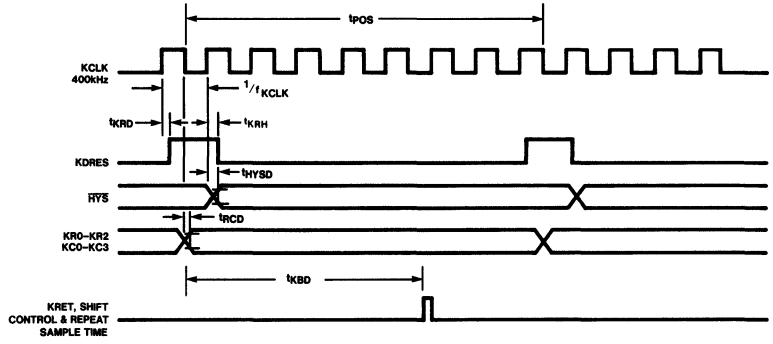


Figure 14

KEYBOARD SCAN TIMING



NOTE
SCAN TIMING SHOWN IS FOR FAST SCAN (KMR1 = 1). FOR SLOW SCAN (KMR1 = 0) ALL SIGNALS EXCEPT KCLK RUN AT ¼ THE SHOWN RATES.

Figure 15

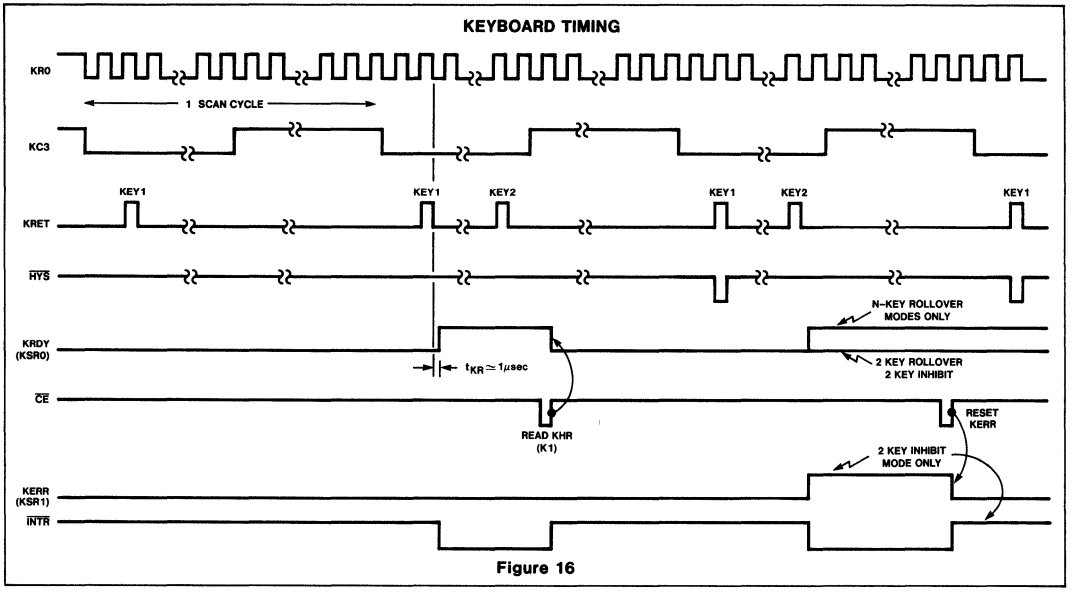


Figure 16

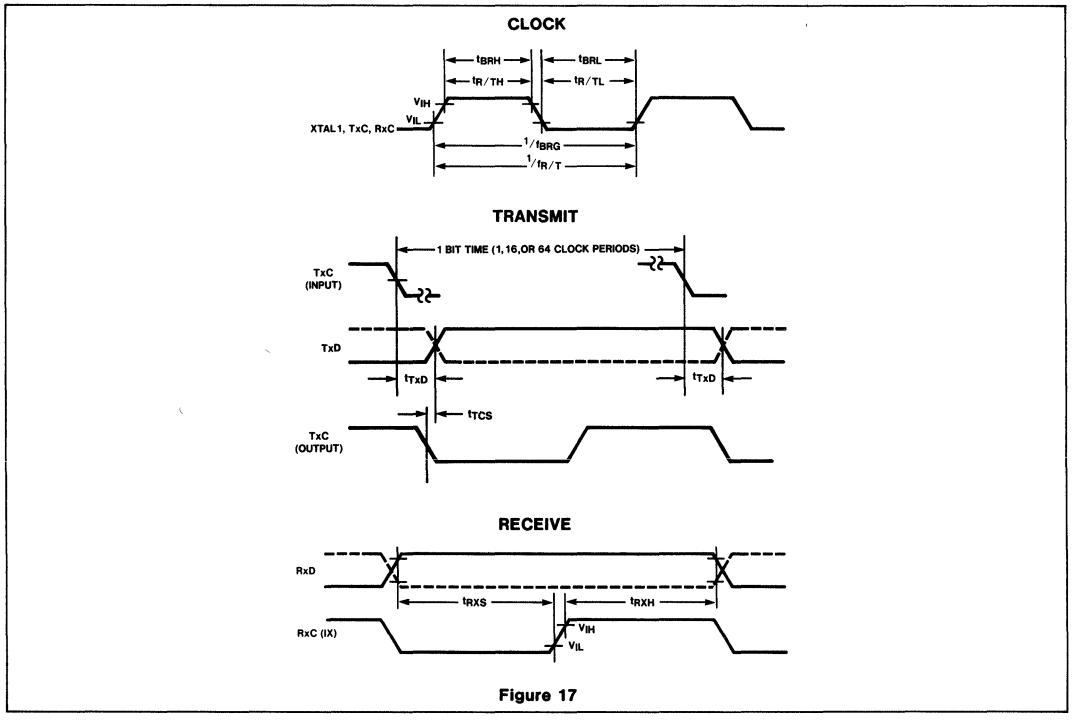


Figure 17

TRANSMITTER TIMING
(5-BIT CHARACTERS, NO PARITY, 2 STOP BITS)

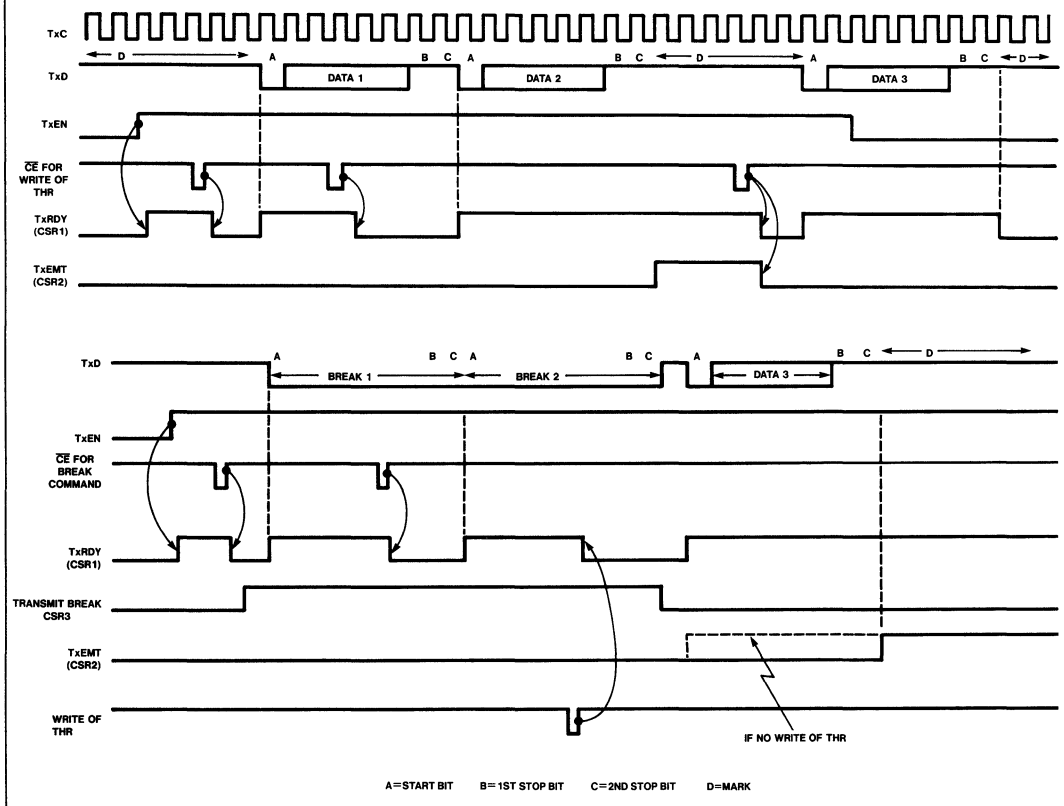


Figure 18

RECEIVER TIMING
(5-BIT CHARACTERS, NO PARITY, 2 STOP BITS)

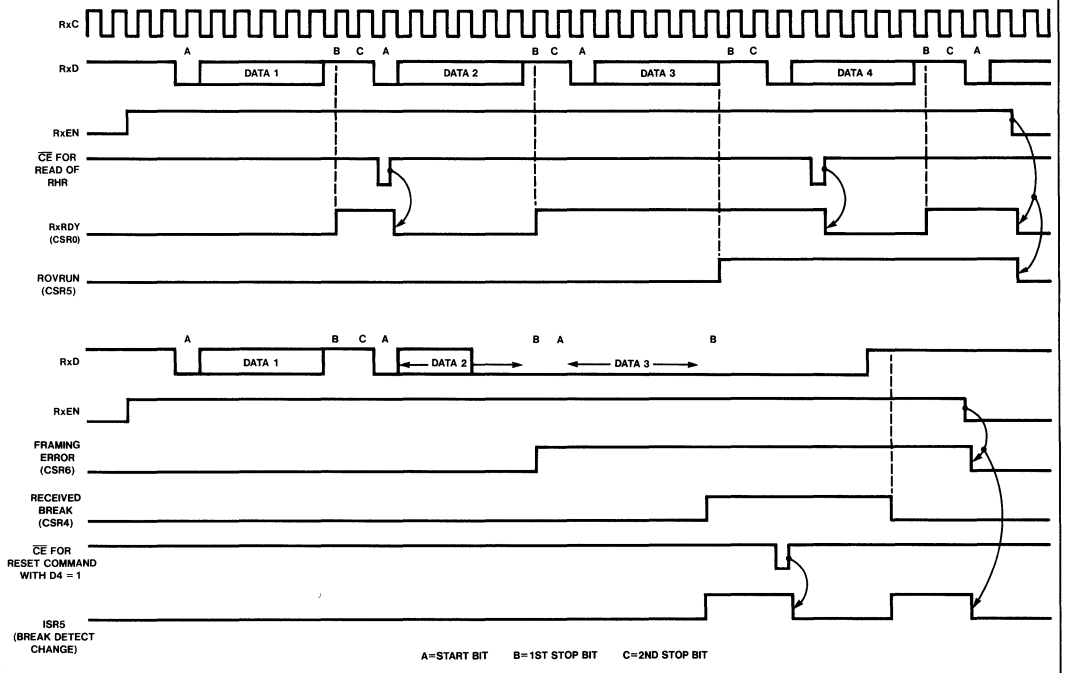


Figure 19

CRYSTAL CONNECTIONS BRG CLOCK

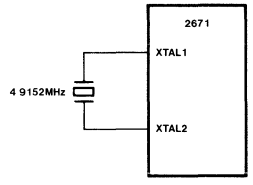


Figure 20

CONNECTION FOR EXTERNAL BRG CLOCK SOURCE

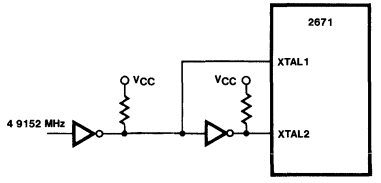


Figure 21

	7	6	5	4	3	2	1	0
KMR	Test mode 1 = Enable 0 = Disable	Rollover modes 00 = N-key with latched keys 01 = N-key 10 = Two keys 11 = Two key inhibit		Keyboard 0 = Encoded 1 = Non encoded	Auto repeat 0 = Disable 1 = Enable	KMR2 / KMR1 0 0 0 1 1 0 1 1	Key Matrix Size / Scan Time 128 10ms 128 2.5ms 80 6.4ms 80 1.6ms	Tone select 0 = 1kHz 1 = 2kHz
KSR	CONTROL	SHIFT	SHIFT LOCK	REPEAT	Keyboard Enabled	KOVR	KERR	KRDY
CMR	Operating Mode 00 = Normal 01 = Auto echo 10 = Local loopback 11 = Remote loopback		Parity 0 = Odd/ force 0 1 = Even/ force 1	Parity Mode 00 = With parity 01 = Force parity 10 = No parity 11 = Not allowed		Stop Bits 0 = Two 1 = One	Character Length 00 = 8 01 = 5 10 = 6 11 = 7	
BRR	Tx Clock source 0 = External 1 = Internal (BRG)	Rx Clock source 0 = External 1 = Internal (BRG)	Clock rate factor for external clocks 00 = 16X 01 = 32X 10 = 64X 11 = 1X For internal clocks these bits specify the output frequency on pins 34 and 35 (table 4).	Baud rate select (BRR3 - BRR0 in hex) 0 = 50 1 = 110 2 = 134.5 3 = 150	4 = 200 5 = 300 6 = 600 7 = 1050	8 = 1200 9 = 1800 A = 2000 B = 2400	C = 4800 D = 9600 E = 19200 F = 38400 (BRCLK = 4.9152MHz)	
CSR	Parity error	Framing error	Overrun error	Received break	Transmit break	TxEMT	TxRDY	RxRDY
IMR/ISR	TxRDY	TxEMT	BREAK CHANGE	XINT	KERR	KRDY	KOVR	RxRDY
Reset Command Format	00X = No effect 010 = Set RxE 011 = Reset RxE 100 = Set TxE 101 = Reset TxE 110 = Set TxE and RxE 111 = Communications reset			Break detect change reset	Communications error reset	KOVR reset	KERR reset	Keyboard reset
Miscellaneous Commands Format	Clear keyboard enable	Set keyboard enable	Clear shift lock	Set shift lock	Ring tone long	Ring tone short	Transmit timed break	Transmit character break

Table 7. Register Format Summary

PROGRAMMABLE VIDEO TIMING CONTROLLER (PVTC) SC2672

Preliminary

DESCRIPTION

The Signetics 2672 Programmable Video Timing Controller (PVTC) is a programmable device designed for use in CRT terminals and display systems that employ raster scan techniques. The PVTC generates the vertical and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT monitor. It provides consecutive addressing to a user specified display buffer memory domain and controls the CPU-display buffer interface for various buffer configuration modes. A variety of operating modes, display formats, and timing profiles can be implemented by programming the control registers in the PVTC.

A minimum CRT terminal system configuration consists of a PVTC, a 2671 Keyboard and Communication Controller (PKCC), a 2670 Display Character and Graphics Generator (DCGG), a 2673 Video and Attributes Controller (VAC), a single chip microcomputer such as the 8048, a display buffer RAM, and a small amount of TTL for miscellaneous address decoding, interface, and control. Typically, the package count for a minimum system is between 15 and 20 devices; system complexity can be enhanced by upgrading the microprocessor and expanding via the system address and data busses.

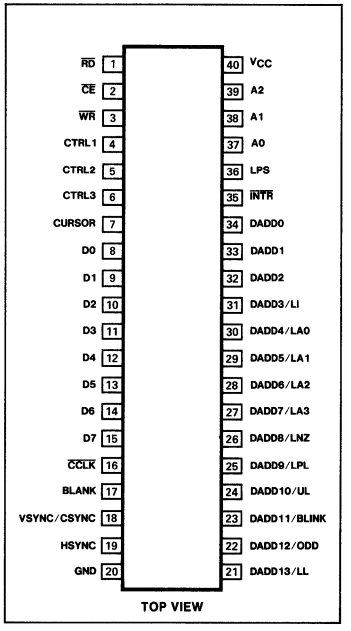
FEATURES

- 4MHz character rate
- Up to 256 characters per row
- 1 to 16 raster lines per character row
- Up to 128 character rows per frame
- Programmable horizontal and vertical sync generators
- Interlaced or non-interlaced operation
- Up to 16K RAM addressing for multiple page operation
- Automatic wraparound of RAM
- Addressable incrementable and readable cursor
- Programmable cursor size, position, and blink
- Split screen and horizontal scroll capability
- Light pen register
- Selectable buffer interface modes
- Dynamic RAM refresh
- Completely TTL compatible
- Single +5 volt power supply
- Power on reset circuit

APPLICATIONS

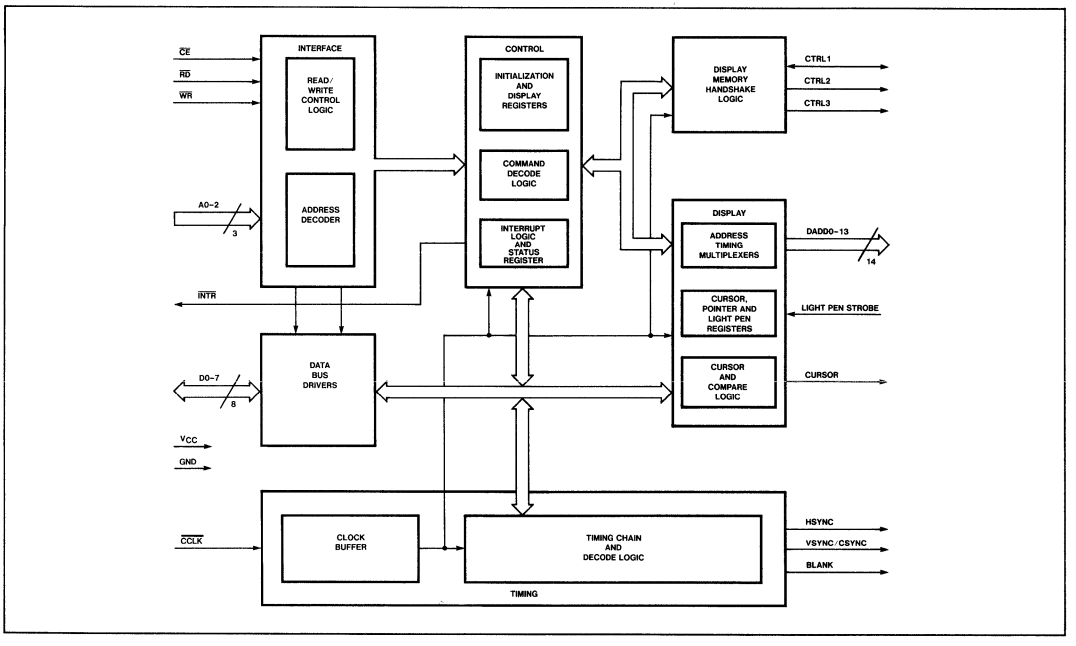
- CRT terminals
- Word processing systems
- Small business computers
- Home Computers

PIN CONFIGURATION



TOP VIEW

BLOCK DIAGRAM



PROGRAMMABLE VIDEO TIMING CONTROLLER (PVTC) SC2672

Preliminary

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%, T_A = 0°C to 70°C
Ceramic DIP	SC2672C4I40
Plastic DIP	SC2672C4N40

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
A0–A2	37–39	I	**Address Lines:** Used to select PVTC internal registers for read/write operations and for commands.
D0–D7	8–15	I/O	**8–Bit Bidirectional Three–State Data Bus.** Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the PVTC takeplace over this bus. The direction of the transfer is controlled by the $\overline{RD}$ and $\overline{WR}$ inputs when the $\overline{CE}$ input is low. When the $\overline{CE}$ input is high, the data bus is in the three–state condition.
$\overline{RD}$	1	I	**Read Strobe:** Active low input. A low on this pin while $\overline{CE}$ is low causes the contents of the register selected by A0–A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of $\overline{RD}$.
$\overline{WR}$	3	I	**Write Strobe:** Active low input. A low on this pin while $\overline{CE}$ is also low causes the contents of the data bus to be transferred to the register selected by A0–A2. The transfer occurs on the trailing (rising) edge of $\overline{WR}$.
$\overline{CE}$	2	I	**Chip Enable:** Active low input. When low, data transfers between the CPU and the PVTC are enabled on D0–D7 as controlled by the $\overline{WR}$, $\overline{RD}$, and A0–A2 inputs. When $\overline{CE}$ is high, the PVTC is effectively isolated from the data bus and D0–D7 are placed in the three–state condition.
$\overline{CCLK}$	16	I	**Character Clock:** Timing signal derived from the video dot clock which is used to synchronize the PVTC's timing functions.
HSYNC	19	O	**Horizontal Sync:** Active high output which provides video horizontal sync pulses. The timing parameters are programmable.
VSYNC/CSYNC	18	O	**Vertical Sync/Composite Sync:** A control bit selects either vertical or composite sync pulses on this active high output. When CSYNC is selected, equalization pulses are included. The timing parameters are programmable.
BLANK	17	O	**Blank:** This active high output defines the horizontal and vertical borders of the display. Display control signals which are output on DADD3 thru DADD13 are valid on the trailing edge of BLANK.
CURSOR	7	O	**Cursor Gate:** This active high output becomes active for a specified number of scan lines when the address contained in the cursor registers match the address output on DADD0 thru DADD13. The first and last lines of the cursor and a blink option are programmable.
$\overline{INTR}$	35	O	**Interrupt Request:** Open drain output which supplies an active low interrupt request from any of five maskable sources. This pin is inactive after power on reset or a master reset command.
LPS	36	I	**Light Pen Strobe:** Positive edge triggered input indicating a light pen hit. Causes the current value of the display address to be strobed into the light pen register.
CTRL1	4	I/O	**Handshake Control 1:** In independent mode, provides an active low write data buffer ($\overline{WDB}$) output which strobes data from the interface latch into the display memory. In transparent and shared modes, this is an active low processor bus request ($\overline{PBREQ}$) input which indicates that the CPU desires to access the display memory. This control output has no meaning in row buffer mode
CTRL2	5	O	**Handshake Control 2:** In independent mode, provides an active low read data buffer ($\overline{RDB}$) output which strobes data from the display memory into the interface latch. In transparent and shared modes, this is an active low bus external enable ($\overline{BEXT}$) output which indicates that the PVTC has relinquished control of the display memory (DADD0–DADD13 are in the three–state condition) in response to a CPU bus request. $\overline{BEXT}$ also goes low in response to a 'display off and float DADD' command. In row buffer mode, it is an active low bus request ($\overline{BREQ}$) output which halts the CPU during a line DMA.

PROGRAMMABLE VIDEO TIMING CONTROLLER (PVTC) SC2672

Preliminary

PIN DESIGNATION (cont.)

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
CTRL3	6	O	**Handshake Control 3:** In independent mode, provides the active low buffer chip enable ($\overline{BCE}$) signal to the display memory. In transparent and shared modes, provides an active low bus acknowledge ($\overline{BACK}$) output which serves as a ready signal to the CPU in response to a processor bus request. In row buffer mode, this is an active high memory bus control (MBC) output which configures the system for the DMA transfer of one row of character codes from system memory to the row display buffer.
DADD0–DADD13	34–21	O	**Display Address:** Used by the PVTC to address up to 16K of display memory. These outputs are floated at various times depending on the buffer mode. Various control signals are multiplexed on DADD3 thru DADD13 and are valid at the trailing edge of BLANK. These control signals are: **DADD3/LI** **Line Interlace:** Replaces DADD4/LA0 as the least significant line address for interlaced sync and video applications. A low indicates an even row of an even field or an odd row of an odd field. **DADD4–DADD7/LA0–LA3** **Line Address:** Provides the number of the current scan line within each character row. **DADD8/LNZ** **Line Zero:** Asserted before the first scan line in each character row. **DADD9/LPL** **Light Pen Line:** Asserted before the scan line which matches the programmed light pen line position (line 3, 5, 7, or 9). **DADD10/UL** **Underline:** Asserted before the scan line which matches the programmed underline position (line 0 thru 15). **DADD11/BLINK** **Blink frequency:** Provides an output divided down from the vertical sync rate. **DADD12/ODD** **Odd Field:** Active high signal which is asserted before each scan line of the odd field when interlace is specified. **DADD13/LL** **Last Line:** Asserted before the last scan line of each character row.
V_{CC}	40	I	**Power Supply:** +5 volts ± 5% power input.
GND	20	I	**Ground:** Signal and power ground input.

FUNCTIONAL DESCRIPTION

As shown on the block diagram, the PVTC contains the following major blocks:

- Data bus buffer
- Interface Logic
- Operation Control
- Timing
- Display Control
- Buffer Control

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the PVTC.

Interface Logic

The interface logic contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are as shown in table 1.

Table 1 PVTC ADDRESSING

A2	A1	A0	READ (RD=0)	WRITE (WR=0)
0	0	0	Interrupt register	Initialization registers[1]
0	0	1	Status register	Command register
0	1	0	Screen start address lower register	Screen start address lower reg.
0	1	1	Screen start address upper register	Screen start address upper reg.
1	0	0	Cursor address lower register	Cursor address lower register
1	0	1	Cursor address upper register	Cursor address upper register
1	1	0	Light pen address lower register	Display pointer address lower reg.
1	1	1	Light pen address upper register	Display pointer address upper reg

NOTE

1 There are 11 initialization registers which are accessed sequentially via a single address The PVTC maintains an internal pointer to these registers which is incremented after each write at this address until the last register (IR10, the split screen register) is accessed. The pointer then continues to point to the split screen register Upon power–up or a master reset command, the internal pointer is reset to point to the first register (IR0) of the initialization register group The internal pointer can also be preset to any register of the group via the 'load IR address pointer' command

PROGRAMMABLE VIDEO TIMING CONTROLLER (PVTC) SC2672

Preliminary

Operation Control

The operation control section decodes configuration and operation commands from the CPU and generates appropriate signals to other internal sections to control the overall device operation. It contains the timing and display registers which configure the display format and operating mode, the interrupt logic, and the status register which provides operational feedback to the CPU.

Timing

The timing section contains the counters and decoding logic necessary to generate the monitor timing outputs and to control the display format. These timing parameters are selected by programming of the initialization registers.

Display Control

The display control section generates linear addressing for up to 16K bytes of display memory. Internal comparators limit the portion of the memory which is displayed to programmed values. Additional functions performed in this section include cursor positioning, storage of light pen 'hit' location, and address comparisons required for generation of timing signals and the split screen interrupt.

Buffer Control

The buffer control section generates three signals which control the transfer of data between the CPU and the display buffer memory. Four system configurations requiring four different 'handshaking' schemes are supported. These are described below.

SYSTEM CONFIGURATIONS

Figure 1 illustrates the block diagram of a typical display terminal using the Signetics 2670, 2671, 2672, and 2673 CRT terminal devices. In this system, the CPU examines inputs from the data communications line and the keyboard and places the data to be displayed in the display buffer memory. This buffer is typically a RAM which holds the data for a single or multiple screenload (page) or for a single character row.

The PVTC supports four common system configurations of display buffer memory, designated the independent, transparent, shared, and row buffer modes. The first three modes utilize a single or multiple page RAM and differ primarily in the means used to transfer display data between the RAM and the CPU. The row buffer mode makes use of a single row buffer (which can be a shift register or a small RAM) that is updated in real time to contain the appropriate display data.

The user programs bits 0 and 1 of IR0 to select the mode best suited for the system environment. The CNTRL1–3 outputs perform different functions for each mode and are named accordingly in the description of each mode.

Independent Mode

The CPU to RAM interface configuration for this mode is illustrated in figure 2. Transfer of data between the CPU and display memory is accomplished via a bidirectional latched port and is controlled by the signals read data buffer ($\overline{RDB}$), write data buffer ($\overline{WDB}$), and buffer chip enable ($\overline{BCE}$). This mode provides a non–contention type of operation that does not require address multiplexers. The CPU does not address the memory directly—the read or write operation is performed at the address contained in the cursor address register or the pointer address register as specified by the CPU. The PVTC enacts the data transfers during blanking intervals in order to prevent visual disturbances of the displayed data.

CRT TERMINAL BLOCK DIAGRAM

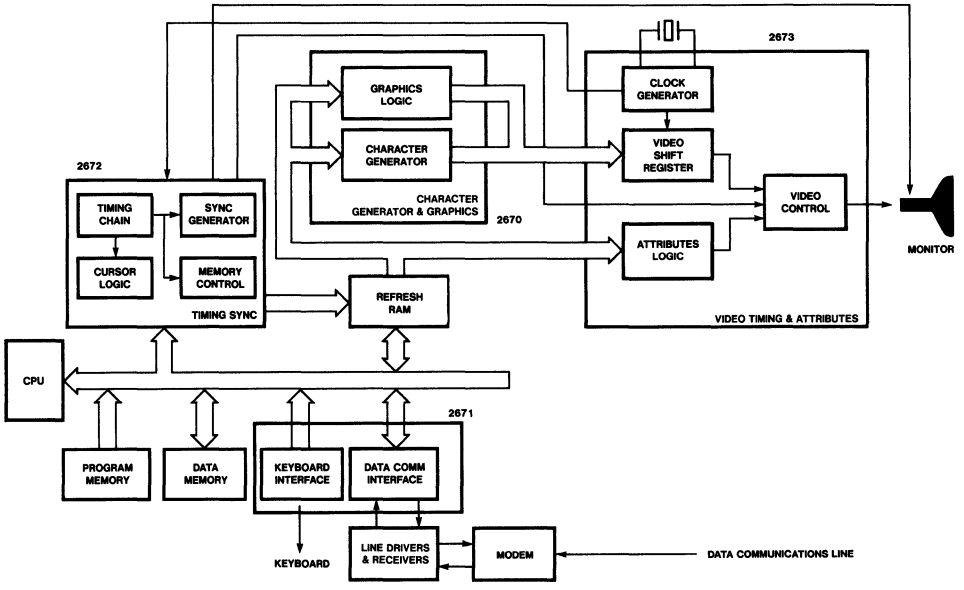


Figure 1

PROGRAMMABLE VIDEO TIMING CONTROLLER (PVTC) SC2672

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The CPU manages the data transfers by supplying commands to the PVTC. The commands used are:

1. Read/Write at pointer address.
2. Read/Write at cursor address (with optional increment of address)
3. Write from cursor address to pointer address.

The operational sequence for a write operation is:

1. CPU checks RDFLG status bit to assure that any previous operation has been completed.
2. CPU loads data to be written to display memory into the interface latch.
3. CPU writes address into cursor or pointer registers.
4. CPU issues 'write at cursor with/without increment' or 'write at pointer' command.
5. PVTC generates control signals and outputs specified address to perform requested operation. Data is copied from the interface latch into the memory.
6. PVTC sets RDFLG status to indicate that the write is completed

Similarly, a read operation proceeds as follows:

1. Steps 1 and 3 as above.
2. CPU issues 'read at cursor with/without increment' or 'read at pointer' command.
3. PVTC generates control signals and outputs specified address to perform requested operation. Data is copied from memory to the interface latch and PVTC sets RDFLG status to indicate that the read is completed.
4 CPU checks RDFLG status to see if operation is completed.
5. CPU reads data from interface latch.

Loading the same data into a block of display memory is accomplished via the 'write from cursor to pointer' command:

1 CPU checks RDFLG status bit to assure that any previous operation has been completed.
2. CPU loads data to be written to display memory into the interface latch.

INDEPENDENT BUFFER MODE CONFIGURATION

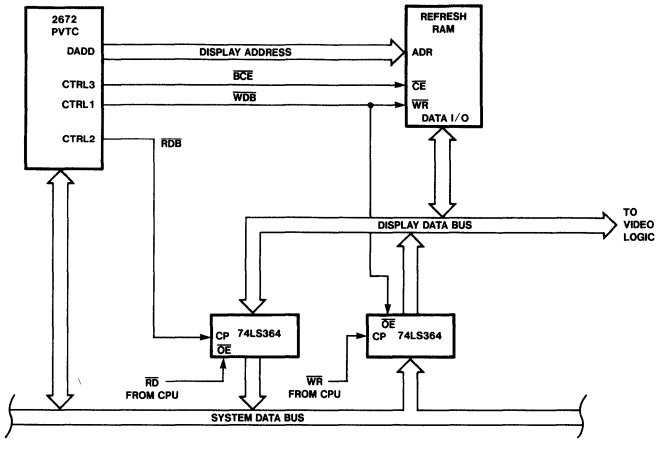


Figure 2

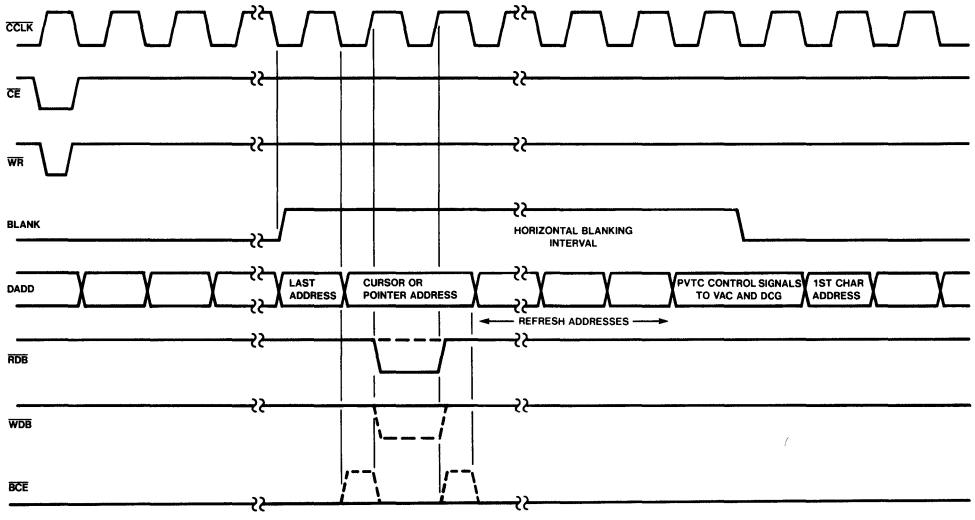
3. CPU writes beginning address of memory block into cursor address register and ending address of block into pointer address register.
4. CPU issues 'write from cursor to pointer' command.
5. PVTC generates control signals and outputs block addresses to copy data from the interface latch into the specified block of memory.
6. PVTC sets RDFLG status to indicate that the block write is completed.

Similar sequences can be implemented on an interrupt driven basis using the READY interrupt output to advise the CPU that a previously requested command has been completed.

Two timing sequences are possible for the 'read/write at cursor/pointer' commands. If the command is given during the active display window (defined as first scan line of the first character row to the last scan line of the last character row), the operation takes place during the next horizontal blanking interval, as illustrated in figure 3. If the command is given during the vertical blanking interval, or while the display has been commanded blanked, the operation takes place immediately. In the latter case, the execution time for the command is approximately one microsecond plus six (6) character clocks (see figure 4).

Timing for the 'write from cursor to pointer' operation is shown in figure 5. The BLANK output is asserted automatically and remains asserted until the vertical retrace interval following completion of the command. The memory is filled at a rate of one location per two character times, plus a small amount of overhead.

READ/WRITE AT CURSOR/POINTER COMMAND TIMING
(Command received during active display window)



NOTE
Write waveforms shown in dotted lines

Figure 3

READ/WRITE AT CURSOR/POINTER COMMAND TIMING
(Command received while display is blanked)

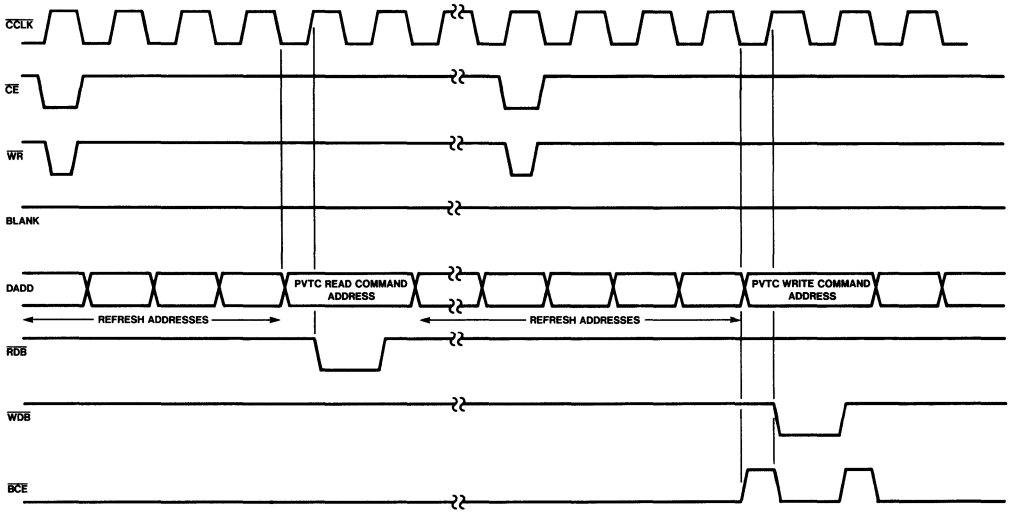


Figure 4

Preliminary

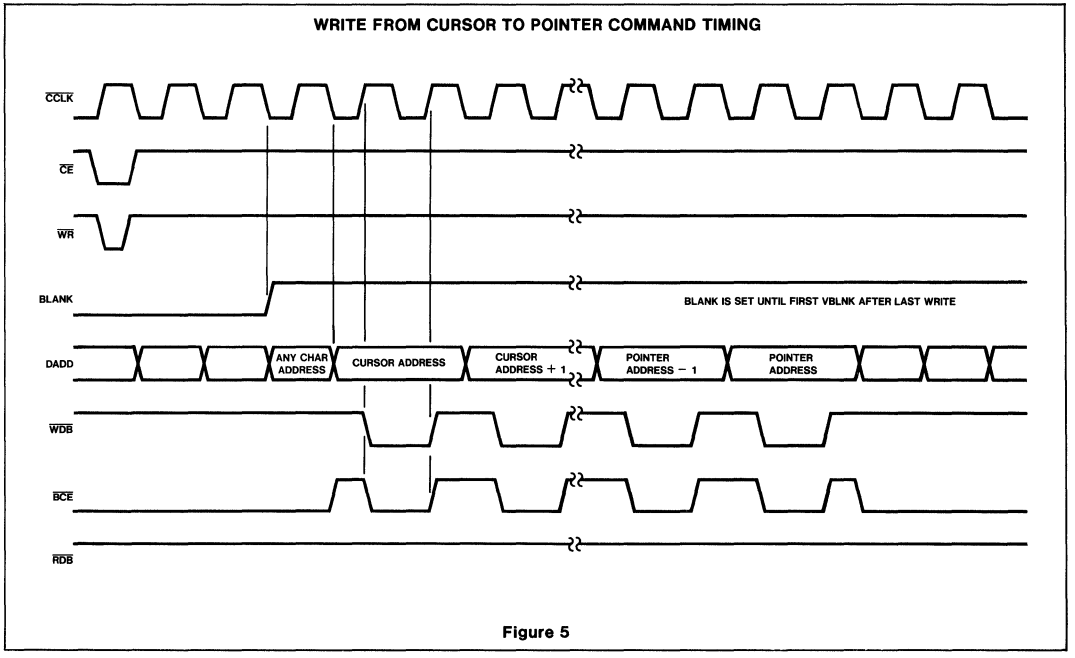


Figure 5

Shared and Transparent Buffer Modes

In these modes the display buffer RAM is a part of the CPU memory domain and is addressed directly by the CPU. Both modes use the same hardware configuration with the CPU accessing the display buffer via three-state drivers (see figure 6). The processor bus request ($\overline{PBREQ}$) control signal informs the PVTC that the CPU is requesting access to the display buffer. In response to this request, the PVTC raises bus acknowledge ($\overline{BACK}$) until its bus external ($\overline{BEXT}$) output has freed the display address and data busses for CPU access. $\overline{BACK}$, which can be used as a 'hold' input to the CPU, is then lowered to indicate that the CPU can access the buffer

In transparent mode, the PVTC delays the granting of the buffer to the CPU until a vertical or horizontal blanking interval, thereby causing minimum disturbance of the display. In shared mode, the PVTC will blank the display and grant immediate access to the CPU. Timing for these modes is illustrated in figures 7, 8, and 9

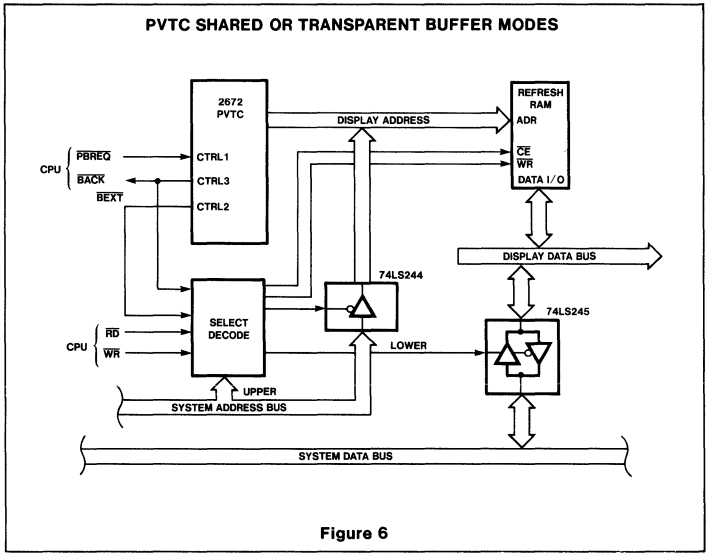
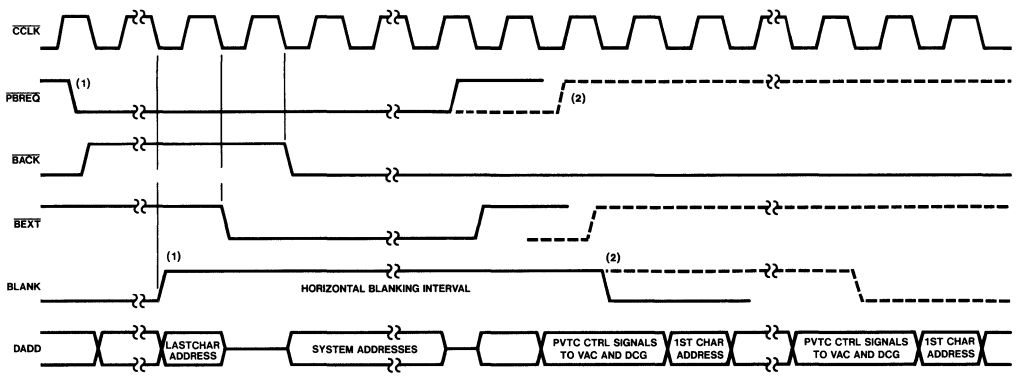


Figure 6

TRANSPARENT BUFFER MODE TIMING

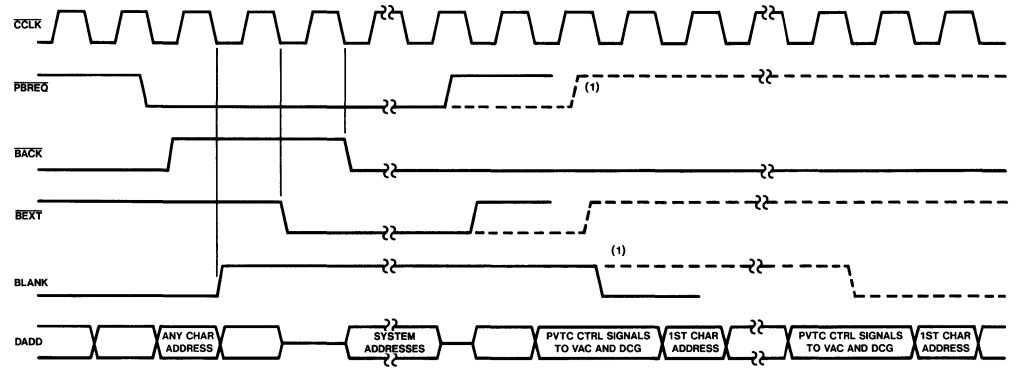


NOTES
1 $\overline{\text{PBREQ}}$ must be asserted prior to the rising edge of BLANK in order for sequence to begin during that blanking period

2 If $\overline{\text{PBREQ}}$ is negated after the next to last $\overline{\text{CCLK}}$ of the horizontal blanking interval, the next scan line will also be blanked

Figure 7

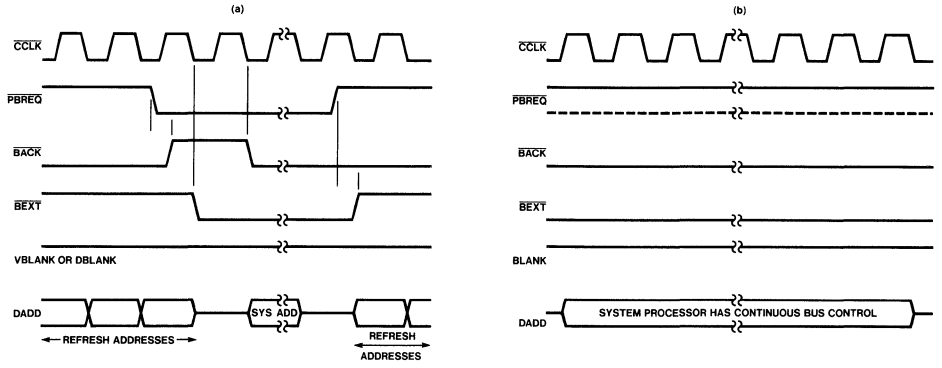
SHARED BUFFER MODE TIMING



NOTE
1 If $\overline{\text{PBREQ}}$ is negated after the next to last $\overline{\text{CCLK}}$ of the horizontal blanking interval, the next scan line will also be blanked

Figure 8

SHARED AND TRANSPARENT MODE TIMING



a) During Vertical Blank or after 'display off' command

b) After 'display off and 3–state' command

Figure 9

Row Buffer Mode

Figures 10 and 11 show the timing and a typical hardware implementation for the row buffer mode. During the first scan line (line 0) of each character row, the PVTC halts the CPU and DMA's the next row of character data from the system memory to the row buffer memory. The PVTC then releases the CPU and displays the row buffer data for the programmed number of scan lines. The bus request control ($\overline{BREQ}$) signal informs the CPU that character addresses and the memory bus control (MBC) signal will start at the next falling edge of BLANK. The CPU must release the address and data busses before this time to prevent bus contention. After the row of character data is transferred to the CPU, $\overline{BREQ}$ returns high to grant memory control back to the CPU.

ROW BUFFER MODE CONFIGURATION

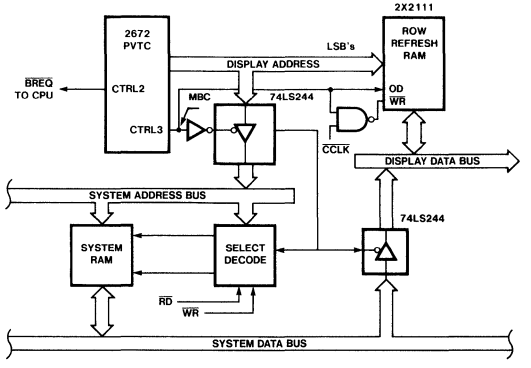


Figure 10

ROW BUFFER MODE TIMING

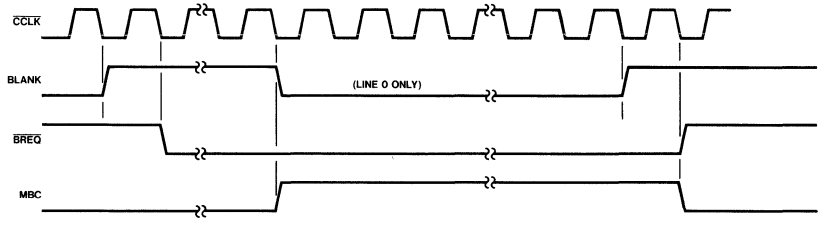


Figure 11

Preliminary

OPERATION

After power is applied, the PVTC will be in an inactive state. Two consecutive 'master reset' commands are necessary to release this circuitry and ready the PVTC for operation. Two register groups exist within the PVTC: the initialization registers and the display control registers. The initialization registers select the system configuration, monitor timing, cursor shape, display memory domain, and screen format. These are loaded first and normally require no modification except for certain special visual effects. The display control registers specify the memory address of the base character (upper left corner of screen), the cursor position, and the pointer address for independent memory access mode. These usually require modification during operation.

After initial loading of the two register groups, the PVTC is ready to control the monitor screen. Prior to executing the PVTC commands which turn on the display and cursor, the user should load the display memory with the first data to be displayed. During operation, the PVTC will sequentially address the display memory within the limits programmed into its registers. The memory outputs character codes to the system character and graphics generation logic, where they are converted to the serial video stream necessary to display the data on the CRT. The user effects changes to the display by modifying the contents of the display memory, the PVTC display control and command registers, and the initialization registers, if required. Interrupts and status conditions generated by the PVTC supply the 'handshaking' information necessary for the CPU to effect the display changes in the proper time frame.

INITIALIZATION REGISTERS

There are 11 initialization registers (IR0–IR10) which are accessed sequentially via a single address. The PVTC maintains an internal pointer to these registers which is incremented after each write at this address until the last register (IR10, the split screen register) is accessed. The pointer then continues to point to the split screen register. Upon power–up or a master reset command, the internal pointer is reset to point to the first register (IR0) of the initialization register group. The internal pointer can also be preset to any register of the group via the 'load IR address pointer' command These registers are write only and are used to specify parameters such as the system configuration, display format, cursor shape, and monitor timing. Register formats are shown in figure 12

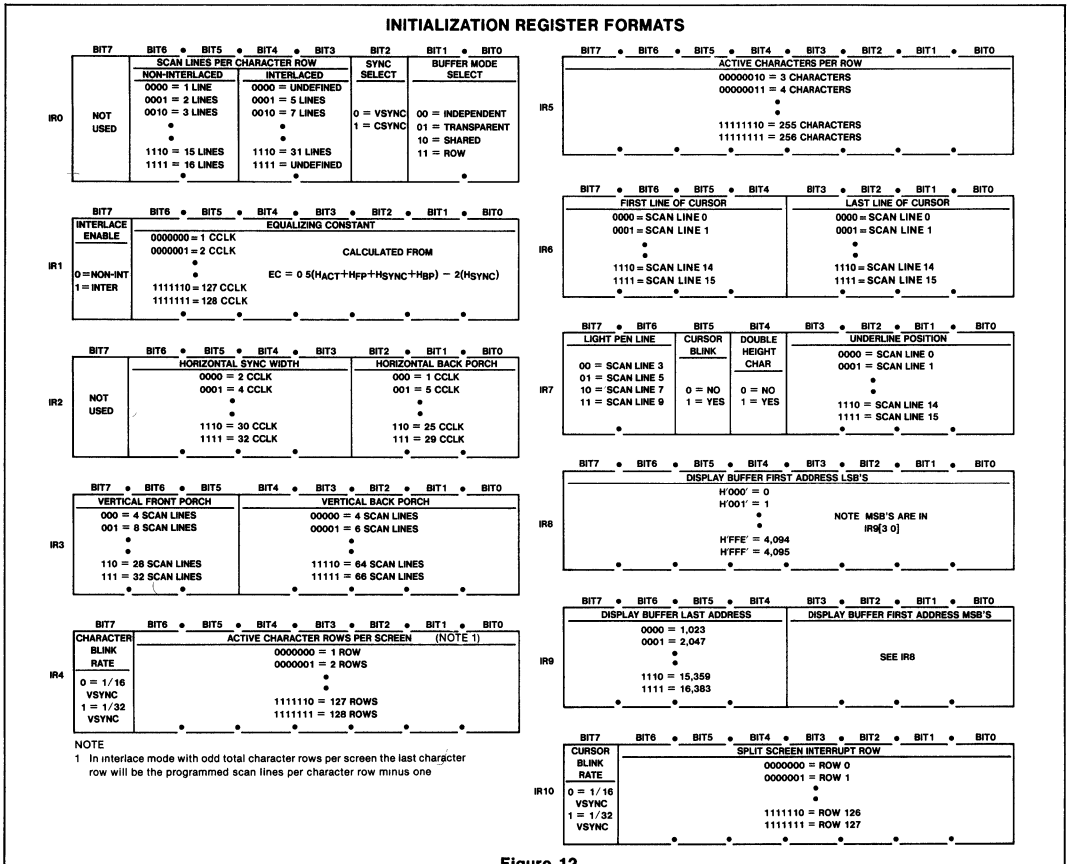


Figure 12

PROGRAMMABLE VIDEO TIMING CONTROLLER (PVTC) SC2672

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IR0[6:3]—Scan Lines per Character Row

Both interlaced and non-interlaced scanning are supported by the PVTC. For interlaced mode, two different formats can be implemented, depending on the interconnection between the PVTC and the character generator (see IR1[7]). This field defines the number of scan lines used to compose a character row for each technique. As scanning occurs, the scan line count is output on the LA0–LA3 and LI pins.

IR0[2]—VS/CS Enable

This bit selects either vertical sync pulses or composite sync pulses on the VSYNC/CSYNC output (pin 18). The composite sync waveform conforms to EIA RS170 standards, with the vertical interval composed of six equalizing pulses, six vertical sync pulses, and six more equalizing pulses.

IR0[1:0]—Buffer Mode Select

Four buffer memory modes may be selectively enabled to accommodate the desired system configuration. See System Configuration.

IR1[7]—Interlace Enable

Specifies interlaced or noninterlaced timing operation. Two modes of interlaced operation are available, depending on whether L0–L3 or LI, L0–L2 are used as the line address for the character generator The resulting displays are shown in figure 13.

For 'interlaced sync' operation, the same information is displayed in both odd and even fields, resulting in enhanced readability. The PVTC outputs successive line numbers in ascending order on the LA0–LA3 lines, one per scan line for each field.

The 'interlaced sync and video' format doubles the character density on the screen The PVTC outputs successive line numbers in ascending order on the LI, LA0–LA2 lines, one per scan line for each field, but alternates beginning the count with even and odd line numbers. This displays the odd field with even scan lines in even character rows and odd scan lines in odd character rows, and the even field with odd scan lines in even character rows and even scan lines on odd character rows. This provides balanced beam currents in the odd and even fields, thus minimizing character variations due to different loading of the CRT anode supply between fields.

IR1[6:0]—Equalizing Constant

This field indirectly defines the horizontal front porch and is used internally to generate the equalizing pulses for the RS170 compatible CSYNC. The value for this field is the total number of character clocks ($\overline{CCLK}$) during a horizontal line period divided by two, minus two times the number of character clocks in the horizontal sync pulse.

$$EC = \frac{H_{ACT} + H_{FP} + H_{SYNC} + H_{BP}}{2} - 2(H_{SYNC})$$

The definition of the individual parameters is illustrated in figure 14.

Note that when using the 2673 VAC, it will delay the blank pulse three $\overline{CCLK}$s relative to the HSYNC pulse.

IR2[6:3]—Horizontal Sync Pulse Width

This field specifies the width of the HSYNC pulse in $\overline{CCLK}$ periods.

IR2[2:0]—Horizontal Back Porch

This field defines the number of CCLKs between the trailing edge of HSYNC and the trailing edge of BLANK.

IR3[7:5]—Vertical Front Porch

Programs the number of scan line periods between the rising edges of BLANK and VSYNC during a vertical retrace interval. The width of the VSYNC pulse is fixed at three scan lines.

IR3[4:0]—Vertical Back Porch

This field determines the number of scan line periods between the falling edges of the VSYNC and BLANK outputs.

IR4[7]—Character Blink Rate

Specifies the frequency for the character blink attribute timing. The blink rate can be specified as 1/16 or 1/32 of the vertical field rate. The timing signal has a duty cycle of 75% and is multiplexed onto the DADD11/BLINK output at the falling edge of each BLANK.

IR4[6:0]—Character Rows Per Screen

This field defines the number of character rows to be displayed This value multiplied by the scan lines per character row, plus the vertical front and back porch values, and the vertical sync pulse width (three scan lines) is the vertical scan period in scan lines.

IR5[7:0]—Active Characters Per Row

This field determines the number of characters to be displayed on each row of the CRT screen. The sum of this value, the horizontal front porch, the horizontal sync width, and the horizontal back porch is the horizontal scan period in $\overline{CCLK}$s.

IR6[7:4], IR6[3:0]—First and Last Scan Line of Cursor

These two fields specify the height and position of the cursor on the character block. The 'first' line is the topmost line when scanning from the top to the bottom of the screen.

IR7[7:6]—Light Pen Line Position

This field defines which of four scan lines of the character row will be used for the light pen strike-thru attribute by the 2673 VAC. The timing signal is multiplexed onto the DADD9/LPL output during the falling edge of BLANK.

IR7[5]—Cursor Blink Enable

This bit controls whether or not the cursor output pin will be blinked at the selected rate (IR10[7]). The blink duty cycle for the cursor is 50%.

IR7[4]—Double Height Character Row Enable

If enabled, the number of each scan line will be repeated twice in succession, causing the height of the character row to double. This bit can be changed at any time but will only become effective at the beginning of the character row following the time it is changed. This allows selected character rows to be of double height. The split screen interrupt can be used to notify the CPU when to effectuate changes to this bit. For each double height row which replaces a normal row, one row count should be subtracted from the 'character rows per screen' field (IR4) to maintain the same total number of scan lines per field.

IR7[3:0]—Underline Position

This field defines which scan line of the character row will be used for the underline attribute by the 2673 VAC. The timing signal is multiplexed onto the DADD10/UL output during the falling edge of BLANK.

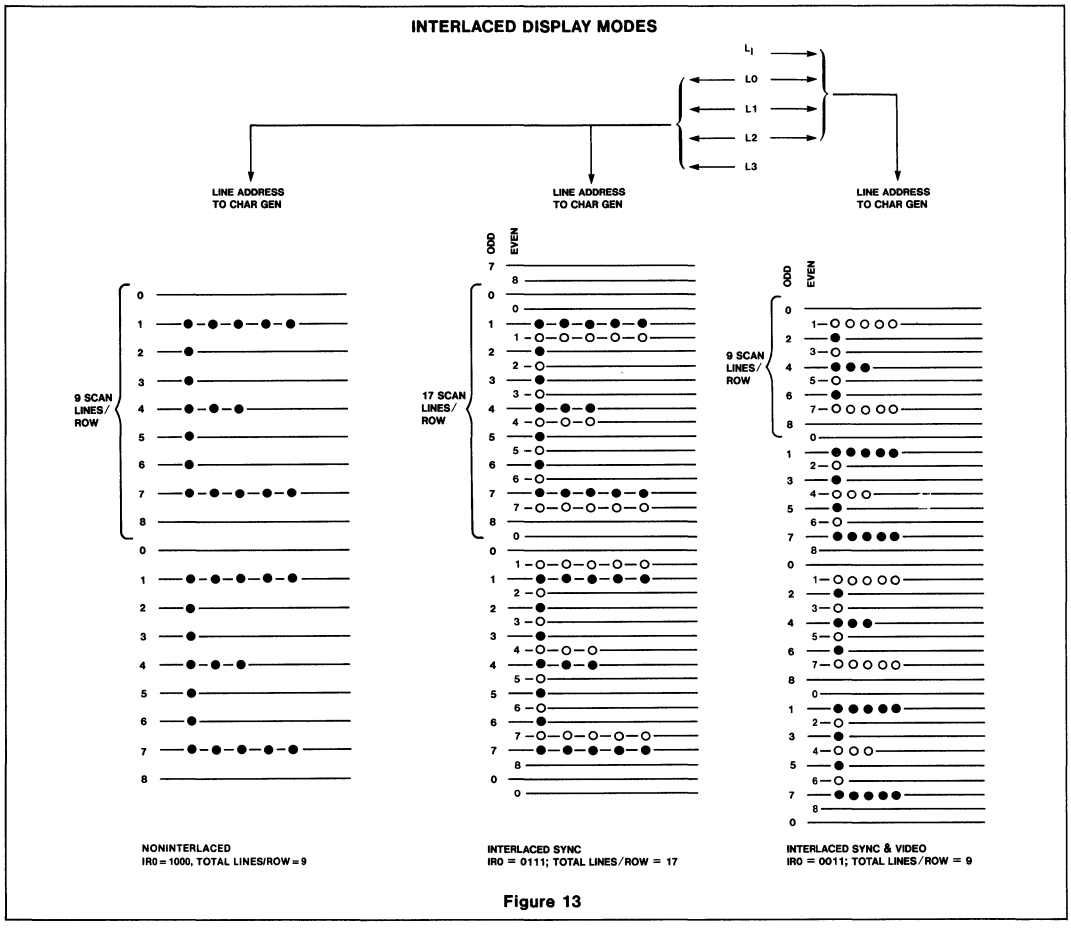

Figure 13

IR9[3:0], IR8[7:0]—Display Buffer First Address
IR9[7:4]—Display Buffer Last Address

These two fields define the area within the buffer memory where the display data will reside When the data at the 'display buffer last address' is displayed, the PVTC will wrap—around and obtain the data to be displayed at the next screen position from the 'display buffer first address'. If 'last address' is the end of a character row and a new screen start address has been loaded into the screen start register, or if 'last address' is the last character position of the screen, the next data is obtained from the address contained in the screen start register.

Note that there is no restriction in displaying data from other areas of the addressable memory. Normally, the area between these two bounds is used for data which can be overwritten (e.g., as a result of scrolling), while data that is not to be overwritten would be contained outside these bounds and accessed by means of the split screen interrupt feature of the PVTC.

IR10[7] — Cursor Blink Rate

The cursor blink rate can be specified at 1/16 or 1/32 of the vertical scan frequency. Blink is effective only if blink is enabled by IR7[5].

IR10[6:0]—Split Screen Interrupt

The split screen interrupt can be used to provide special screen effects such as a row of double height characters or to change the normal addressing sequence of the display memory. The contents of this field is compared, in real time, to the current character row number. Upon a match, the PVTC sets the split screen status bit, and issues an interrupt request if so programmed The status change/interrupt request is made at the beginning of scan line zero of the split screen character row.

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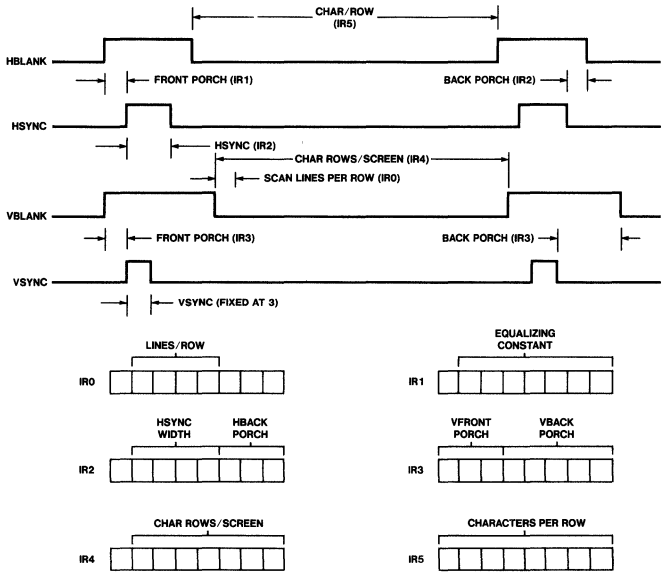

Figure 14

Timing Considerations

Normally, the contents of the initialization registers are not changed during operation. However, this may be necessary to implement special display features such as multiple cursors, smooth scrolling, horizontal scrolling, and double height character rows. Table 2 describes timing details for these registers which should be considered when implementing these features.

Table 2 TIMING CONSIDERATIONS

PARAMETER	TIMING CONSIDERATIONS
First line of cursor Last line of cursor Light pen line Underline	These parameters must be established at a minimum of two character times prior to their occurence.
Double height characters	Set/reset during the character row prior to the row which is to be/not to be double height
Cursor blink Cursor blink rate Character blink rate	New values become effective within one field after values are changed
Split screen interrupt row	Change anytime prior to line zero of desired row
Character rows per screen	Change only during vertical blanking period
Vertical front porch	Change prior to first line of V_{FP}
Vertical back porch	Change prior to fourth line after V_{SYNC}
Screen start register	Change prior to the horizontal blanking interval of the last line of character row before row where new value is to be used

Preliminary

DISPLAY CONTROL REGISTERS

There are nine registers in this group, each with an individual address. Their formats are illustrated in figure 15. The command register is used to invoke one of 16 possible PVTC commands as described in the COMMANDS section of this data sheet. The remaining registers in the group store address values which specify the cursor and buffer pointer locations, the location of the first character to be displayed on the screen, and the location of a light pen 'hit'. With the exception of the light pen register, the user initializes these registers after powering on the system and changes their values to control the data which is displayed.

Screen Start Registers

The screen start registers contain the address of the first character of the first row (upper left corner of the active display). At the beginning of the first scan line of the first row, this address is transferred to the row start register (RSR) and into the memory address counter (MAC). The counter is then advanced sequentially at the character rate the number of times programmed into the active characters per row register (IR5), thus reaching the address of the last character of the row plus one. At the beginning of each subsequent scan line of the first row, the MAC is reloaded from the RSR and the above sequence is repeated. At the end of the last scan line of the first row, the contents of the MAC is loaded into the RSR to serve as the starting memory address for the second character row. This process is repeated for the programmed number of rows per screen. Thus, the data in the display memory is displayed sequentially starting from the address contained in the screen start register. After the ensuing vertical retrace interval, the entire process repeats again.

The sequential operation described above will be modified upon the occurence of either of two events. First, if during the incrementing of the memory address counter the 'display buffer last address' (IR9[7:4]) is reached, the MAC will be loaded from the 'display buffer first address' register (IR9[3:0], IR8[7:0]) at the next character clock. Sequential operation will then resume starting from this address. This wraparound operation allows portions of the display buffer to be used for purposes other than storage of displayable data and is completely automatic without any CPU intervention (see figure 16a).

The sequential row to row addressing can also be modified under CPU control. If the contents of the screen start register (upper, lower, or both) are changed during any character row (say row 'n'), the starting address of the next character row (row 'n + 1') will be the new value of the screen start register and addressing will continue sequentially from there. This allows features such as split screen operation, partial scroll, or status line display to be implemented. The split screen interrupt feature of the PVTC is useful in controlling this type of operation. Note that in order to obtain the correct screen display, the screen start register must be reloaded with the original value prior to the end of the vertical retrace. See figure 16b.

During vertical blanking the address counter operation is modified by stopping the automatic load of the contents of the RSR into the counter, thereby allowing the address outputs to free–run. This allows dynamic memory refresh to occur during the vertical retrace interval. The refresh addressing starts at the last address displayed on the screen and increments by one for each character clock during the retrace interval. If the display buffer last address is encountered, refreshing continues from the display buffer first address.

Cursor Address Registers

The contents of these registers defines the buffer memory address of the cursor. If enabled, the cursor output will be asserted when the memory address counter matches the value of the cursor address registers. The cursor address registers may be read or written by the CPU or incremented via the 'increment cursor address' command. In independent buffer mode, these registers define a buffer memory address for PVTC controlled access in response to 'read/write at cursor with/without increment' commands, or the first address to be used in executing the 'write from cursor to pointer' command.

Display Pointer Address Registers

These registers define a buffer memory address for PVTC controlled accesses in response to 'read/write at pointer' commands They also define the last buffer memory address to be written for the 'write from cursor to pointer' command.

Light Pen Address Registers

If the light pen input is enabled, these registers are used to store the current character address upon receipt of a light pen strobe input. Several sources of delay between the display of a character upon the screen and the receipt of a light pen hit can be expected to exist in a system environment. These delays include address pipelining in the character generation circuits, delays in the video generation circuits, and delays in the light detection circuitry itself These delays cause the value stored in the light pen register to differ from the actual address of the character at which the light pen hit actually was detected. Software must be used to correct this condition.

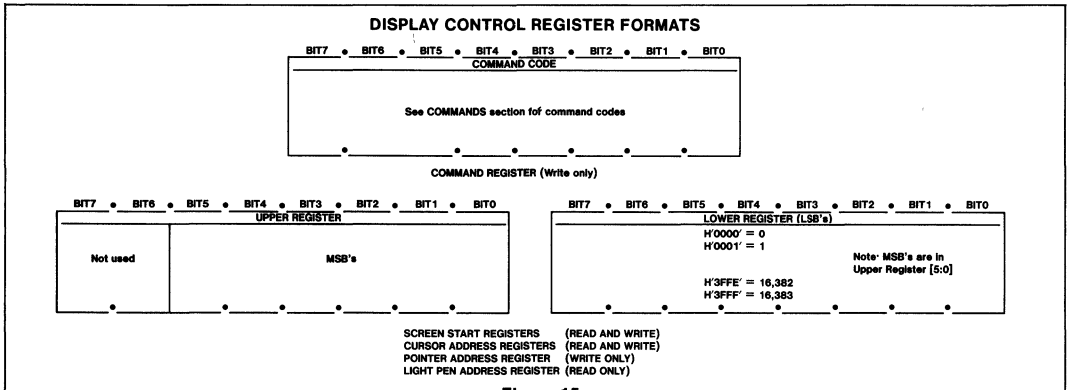

Figure 15

PROGRAMMABLE VIDEO TIMING CONTROLLER (PVTC) SC2672

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INTERRUPT/STATUS REGISTERS

The interrupt and status registers provide information to the CPU to allow it to interact with the PVTC to effect desired changes to implement various display operations. The interrupt register provides information on five possible interrupting conditions, as shown in figure 17. These conditions may be selectively enabled or disabled (masked) from causing interrupts by certain PVTC commands. An interrupt condition which is enabled (mask bit equal to one) will cause the $\overline{INTR}$ output to be asserted and will cause the corresponding bit in the interrupt register to be set upon occurrence of the interrupting condition. An interrupt condition which is disabled (mask bit equal to zero) has no effect on either the $\overline{INTR}$ output or the interrupt register.

The status register provides six bits of status information: the five possible interrupting conditions plus the NOT BUSY bit. For this register, however, the contents are not effected by the state of the mask bits.

Descriptions of each interrupt/status register bit follow. Unless otherwise indicated, a bit, once set, will remain set until reset by the CPU by issuing a 'reset interrupt/status bits' command. The bits are also reset by a 'master reset' command and upon power–up.

SR[5] – RDFLG

This bit is present in the status register only. A zero indicates that the PVTC is currently executing the previously issued command. A one indicates that the PVTC is ready to accept a new command.

I/SR[4] – VBLANK

Indicates the beginning of a vertical blanking interval. Is set to a one at the beginning of the first scan line of the vertical front porch.

I/SR[3] – Line Zero

Is set to a one at the beginning of the first scan line (line 0) of each active character row.

I/SR[2] – Split Screen

This bit is set when a match occurs between the current character row number and the value contained in the split screen interrupt register, IR10[6:0]. The equality condition is only checked at the beginning of line zero of each character row. This bit is reset when either of the screen start registers is loaded by the CPU.

I/SR[1] – Ready

Certain PVTC commands affect the display and may require the PVTC to wait for a blanking interval before enacting the command. This bit is set to one when execution of the command has been completed. No command should be invoked until the prior command is completed.

I/SR[0] – Light Pen

A one indicates that a light pen hit has occurred and that the contents of the light pen register have been updated. This bit will be reset when either of the light pen registers is read.

DISPLAY ADDRESSING OPERATION

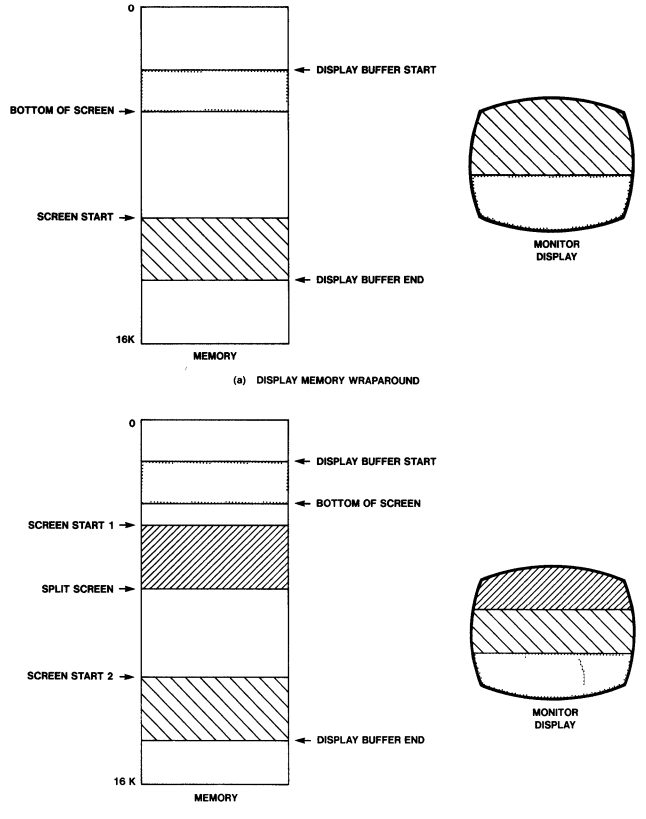

Figure 16

INTERRUPT AND STATUS REGISTER FORMAT

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
		RDFLG	VBLANK	LINE ZERO	SPLIT SCREEN	READY	LIGHT PEN
Not used always read as 0		0 = Busy 1 = Ready *	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Busy 1 = Ready	0 = No 1 = Yes

NOTE
*Status register only Always 0 when reading interrupt register

Figure 17

PROGRAMMABLE VIDEO TIMING CONTROLLER (PVTC) SC2672

Preliminary

COMMANDS

The PVTC commands are divided into two classes the instantaneous commands, which are executed immediately after they are invoked, and the delayed commands which may need to wait for a blanking interval prior to their execution. Command formats are shown in table 3. The commands are asserted by performing a write operation to the command register with the appropriate bit pattern as the data byte.

Instantaneous Commands

The instantaneous commands are executed immediately after the trailing edge of the $\overline{WR}$ pulse during which the command is issued. These commands do not affect the state of the RDFLG or READY interrupt/status bits. However, a command should not be invoked if the RDFLG bit is low

Master Reset

This command initializes the PVTC and may be invoked at any time to return the PVTC to its initial state. Upon power–up, two successive master reset commands must be applied to release the PVTC's internal power on circuits. In transparent and shared buffer modes, the CNTRL1 input must be high when the command is issued. The command causes the following·

1. VSYNC and HSYNC are driven low for the duration of RESET and BLANK goes high. BLANK remains high until a 'display on' command is received.
2. The interrupt and status bits and masks are set to zero, except for the RDFLG flag which is set to a one.
3. The transparent mode, cursoroff, display off, and light pen disable states are set.
4. The initialization register pointer is set to address IR0.

Load IR Address

This command is used to preset the initialization register pointer with the value 'V' defined by D3–D0. Allowable values are 0 to 10.

Enable Light Pen

After invoking this command, receipt of a light pen strobe input will cause the light pen register to be loaded with the current buffer memory address and the corresponding interrupt and status flag to be set Once loaded, further loads are inhibited until either one of the light pen registers are read or a reset function is performed.

Disable Light Pen

Light pen hits will not be recognized.

Display Off

Asserts the BLANK output The DADD0 thru DADD13 display address bus outputs may be optionally placed in the three–state condition by setting bit 2 to a '1' when invoking the command.

Table 3. PVTC Command Formats

D7	D6	D5	D4	D3	D2	D1	D0	Hex	COMMAND
Instantaneous Commands:									
0	0	0	0	0	0	0	0		Master reset
0	0	0	1	V	V	V	V		Load IR pointer with value V (V = 0 to 10)
0	0	1	d	d	d	1	0[1]		Disable light pen
0	0	1	d	d	d	1	1[2]		Enable light pen
0	0	1	d	1	N	d	0[1]		Display off. Float DADD bus if N = 1
0	0	1	d	1	N	d	1[2]		Display on Next field (N = 1) or scan line (N = 0)
0	0	1	1	d	d	d	0[1]		Cursor off
0	0	1	1	d	d	d	1[2]		Cursor on
0	1	0	N	N	N	N	N		Reset interrupt/status Bit reset where N = 1
1	0	0	N	N	N	N	N		Disable interrupt· Disable where N = 1
0	1	1	N	N	N	N	N		Enable interrupt· Enables interupts and resets the corresponding interrupt/status bits where N = 1
			V B	L Z	S S	R D	L P		
Delayed Commands:								Hex	
1	0	1	0	0	1	0	0	A4	Read at pointer address
1	0	1	0	0	0	1	0	A2	Write at pointer address
1	0	1	0	1	0	0	1	A9	Increment cursor address
1	0	1	0	1	1	0	0	AC	Read at cursor address
1	0	1	0	1	0	1	0	AA	Write at cursor address
1	0	1	0	1	1	0	1	AD	Read at cursor address and increment address
1	0	1	0	1	0	1	1	AB	Write at cursor address and increment address
1	0	1	1	1	0	1	1	BB	Write from cursor address to pointer address

NOTES
1 Any combination of these three commands is valid
2 Any combination of these three commands is valid
3 d = don't care

Display On

Restores normal blanking operation either at the beginning of the next field (bit 2 = 1) or at the beginning of the next scan line (bit 2 = 0). Also returns the DADD0–DADD13 drivers to their active state

Cursor Off

Disables cursor operation. Cursor output is placed in the low state.

Cursor On

Enables normal cursor operation.

Reset Interrupt/Status Bits

This command resets the designated bits in the interrupt and status registers. The bit positions correspond to the bit positions in the registers:

Bit 0 – Light pen
Bit 1 – Ready
Bit 2 – Split screen
Bit 3 – Line zero
Bit 4 – Vertical blank

Disable Interrupts

Sets the interrupt mask to zeros for the designated conditions, thus disabling these conditions from asserting the $\overline{INTR}$ output. Bit position correspondence is as above.

Enable Interrupts

Resets the selected interrupt and status register bits and writes the associated interrupt mask bits to a one. This enables the corresponding conditions to assert the $\overline{INTR}$ output Bit position correspondence is as above

Delayed Commands

This group of commands is utilized for the independent buffer mode of operation, although the 'increment cursor' command can also be used in other modes. With the exception of the 'write from cursor to pointer' and 'increment cursor' commands, all the commands of this type will be executed immediately or will be delayed depending on when the command is invoked. If invoked during the active screen time, the command is executed at the next horizontal blanking interval. If invoked during a vertical retrace interval or a 'display off' state, the command is executed immediately.

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The 'increment cursor' and 'write from cursor to pointer' commands are executed immediately after they are issued. 'Increment cursor' requires approximately three $\overline{CCLK}$ periods for completion. 'Write from cursor to pointer' asserts the BLANK output during its execution. BLANK will not be released until the beginning of the vertical blanking interval following the last write operation. A second 'write from cursor to pointer' command should not be issued until this time.

In all cases, the PVTC will assert the READY/RDFLG status to signify completion of the command. No other commands should be given until the current command is completed. Therefore, the READY interrupt or RDFLG status flag should be used for handshaking control between the PVTC and CPU when using these commands.

Read/Write at Pointer

Transfers data between the display buffer and the bus interface latch using the address contained in the pointer register.

Read/Write at Cursor

Transfers data between the display buffer and the bus interface latch using the address contained in the cursor register.

Increment Cursor

Adds one (modulo 16K) to the cursor address register.

Read/Write at Cursor and Increment

Transfers data between the display buffer and the bus interface latch using the address contained in the cursor register and then adds one (modulo 16K) to the cursor address register.

Write from Cursor to Pointer

Writes the data contained in the bus interface latch into the block of display memory designated by the the cursor address and pointer address registers, inclusive. After completion of the command, the pointer address will be unchanged, but the cursor register contents will be equal to the pointer address.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.5 to +6.0	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2.0			V
V_{OL}	Output low voltage	I_{OL} = 1 6mA			0.4	V
V_{OH}	Output high voltage (except $\overline{INTR}$ output)	$I_{OH} = -100$ uA	2.4			V
I_{IL}	Input leakage current	$V_{IN} = 0$ to V_{CC}	−10		10	μA
I_{LL}	Data bus 3—state leakage current	$V_O = 0$ to V_{CC}	−10		10	μA
I_{OD}	$\overline{INTR}$ open drain output leakage current	$V_O = 0$ to V_{CC}			10	μA
I_{CC}	Power supply current				160	mA

NOTES
See next page

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AC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$[4,5,6,7,8]

PARAMETER		TEST CONDITIONS	TENTATIVE LIMITS			UNIT
			Min	Typ	Max	
Bus Timing (Fig. 18)[9]						
t_{AS}	A0–A2 setup time to $\overline{WR}$, $\overline{RD}$ low		30			ns
t_{AH}	A0–A2 hold time from $\overline{WR}$, $\overline{RD}$ high		0			ns
t_{CS}	$\overline{CE}$ setup time to $\overline{WR}$, $\overline{RD}$ low		0			ns
t_{CH}	$\overline{CE}$ hold time from $\overline{WR}$, $\overline{RD}$ high		0			ns
t_{RW}	$\overline{WR}$, $\overline{RD}$ pulse width		250			ns
t_{DD}	Data valid after $\overline{RD}$ low				200	ns
t_{DF}	Data bus floating after $\overline{RD}$ high				100	ns
t_{DS}	Data setup time to $\overline{WR}$ high		150			ns
t_{DH}	Data hold time from $\overline{WR}$ high		0			ns
t_{CC}	Time between READs and/or WRITEs[10]		600			ns
$\overline{CCLK}$ Timing (Fig. 19)						
t_{CCP}	$\overline{CCLK}$ period		250			ns
t_{CCH}	$\overline{CCLK}$ high time		100			ns
t_{CCL}	$\overline{CCLK}$ low time		100			ns
t_{CCD}	Output delay from $\overline{CCLK}$ edge				150	ns
Other Timings (Fig. 20)						
t_{RDL}	READY/RDFLG low from $\overline{WR}$ high[9]				600	ns
t_{BAK}	$\overline{BACK}$ high from $\overline{PBREQ}$ low				150	ns
t_{BXT}	$\overline{BEXT}$ high from $\overline{PBREQ}$ high				150	ns
t_{LPS}	Light pen strobe setup time to $\overline{CCLK}$ low		120			ns
t_{LPH}	Light pen strobe hold time from $\overline{CCLK}$ low		−10			ns
t_{IRL}	$\overline{INTR}$ low from $\overline{CCLK}$ low				150	ns
t_{IRH}	$\overline{INTR}$ high from $\overline{WR}$, $\overline{RD}$ high[9]				600	ns

Notes:

1 Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is a stress rating only and functional operation of the device at these or at any other condition above those in the operation section of this specification is not implied

2 For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 55°C/W junction to ambient (IWA ceramic package)

3 This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima

4 Parameters are valid over specified temperature range

5 All voltage measurements are referenced to ground (GND)

6 Typical values are at +25°C, typical supply voltages, and typical processing parameters

7 For testing, all input signals swing between 0 4V and 2 4V with a transition time of 20ns maximum All time measurements are referenced at input voltages of 0 8V and 2 0V and output voltages of 0 8V and 2 0V as appropriate

8 Test condition for outputs C_L = 150pF

9 Timing is illustrated and specified referenced to $\overline{WR}$ and $\overline{RD}$ inputs Device may also be operated with $\overline{CE}$ as the 'strobing' input In this case, all timing specifications apply referenced to falling and rising edges of $\overline{CE}$

10 1 microsecond minimum after 'master reset' command

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BUS TIMING

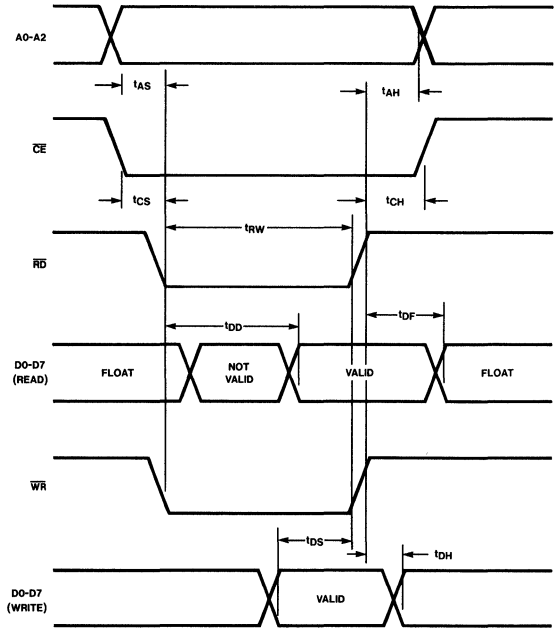
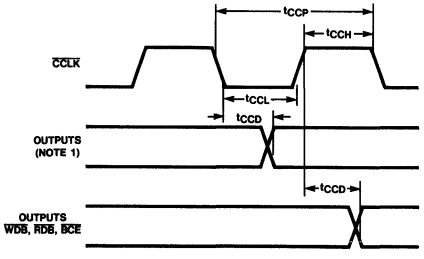


Figure 18

CCLK TIMING



NOTES
1 DADD0-DADD13, BLANK, HSYNC, CSYNC/VSYNC, CURSOR, BEXT, BREQ, BCE, MBC, BACK

2 BCE changes state on both CCLK edges—(see Figures 3 and 4)

Figure 19

OTHER TIMINGS

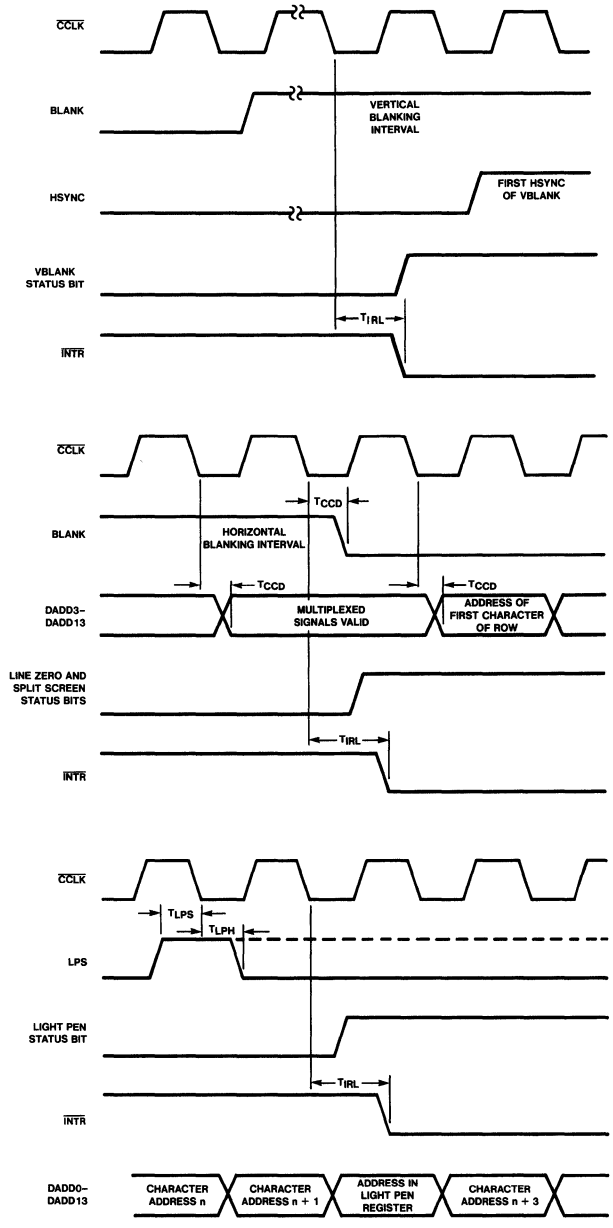


Figure 20

OTHER TIMINGS (Continued)

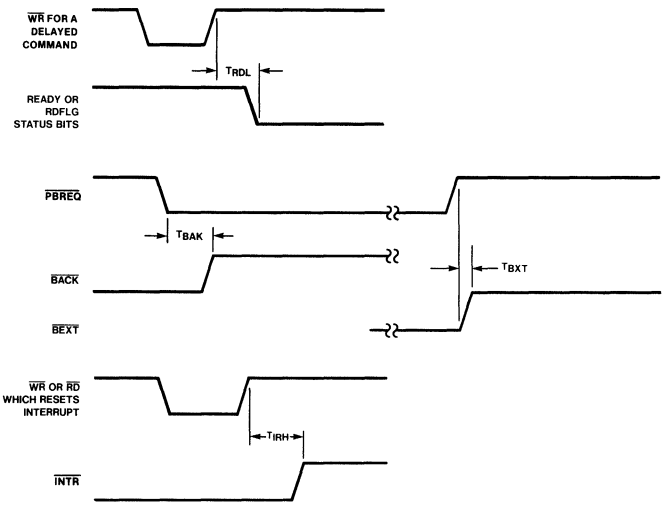
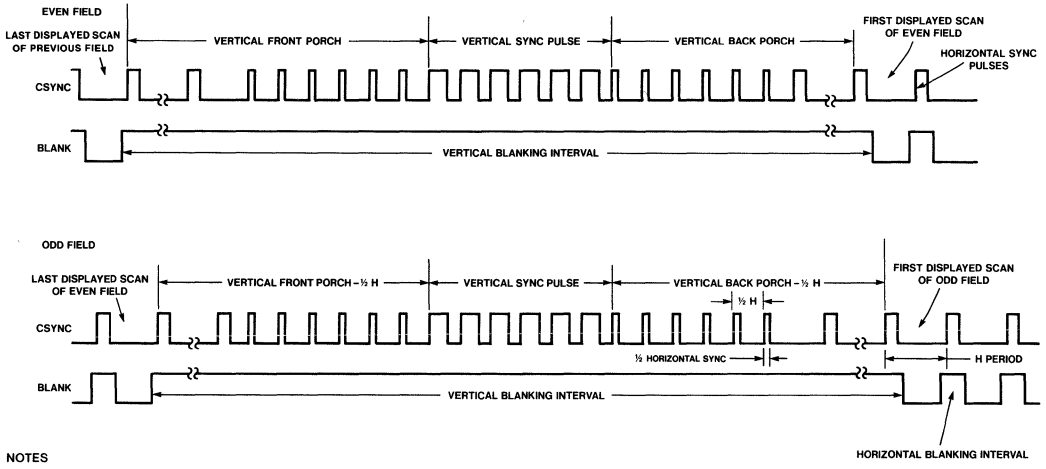


Figure 20

COMPOSITE SYNC TIMING



NOTES

1 In non-interlaced operation the even field is repeated continuously, and the odd field is not

2 In interlaced operation the even field alternates with the odd field

Figure 21

VIDEO ATTRIBUTES CONTROLLER (VAC) SC2673

Preliminary

DESCRIPTION

The Signetics 2673A and 2673B Video Attributes Controllers (VAC) are bipolar LSI devices designed for CRT terminals and display systems that employ raster scan techniques. Each contains a high speed video shift register, field and character attributes logic, attribute latch, cursor format logic and half dot shift control.

The VAC provides control of visual attributes on a field or character by character. Internal logic preserves field attribute data from character row to character row so that an attribute byte is not required at the beginning of each row. The 2673B provides for reverse video, blank (non-display), blink, underline and highlight attributes and a graphic smode attribute to work in conjunction with the Signetics 2670 Display Character and Graphics Generator (DCGG). The 2673A substitutes a light pen (strike-thru) attribute for the graphics attribute.

The horizontal dot frequency is the basic timing input to the VAC. Internally, this clock is divided down to provide a character clock output for system synchronization. Up to ten bits of video dot data are parallel loaded into the video shift register on each character boundary. The video data is shifted out on three outputs at the dot frequency. On the VIDEO output, the data is presented as a three level signal representing low, medium and high intensities. The three intensities are also encoded on two TTL compatible video outputs. Light or dark screen background can be selected.

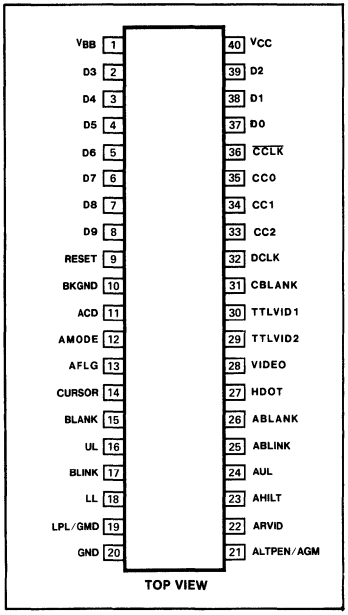
FEATURES

- **25MHz video dot rate**
- **Three level current driven (75 ohms) video output**
- **Three level encoded TTL video outputs**
- **Character/field attribute logic**
  - **Reverse video**
  - **Character blank**
  - **Character blink**
  - **Underline**
  - **Highlight**
  - **Light pen strike-thru or graphics control**
- **Field attributes extend from row to row**
- **Light or dark field**
- **Cursor reverse video logic**
- **Up to 10 dots per character**
- **Composite blanking for light field retrace**
- **Optional field graphics control output**
- **High speed bipolar design**
- **40 pin dual in-line package**
- **TTL compatible**
- **Compatible with Signetics 2672 PVTC and 2670 DCGG**

APPLICATIONS

- **CRT terminals**
- **Word processing systems**
- **Small business computers**

PIN CONFIGURATION

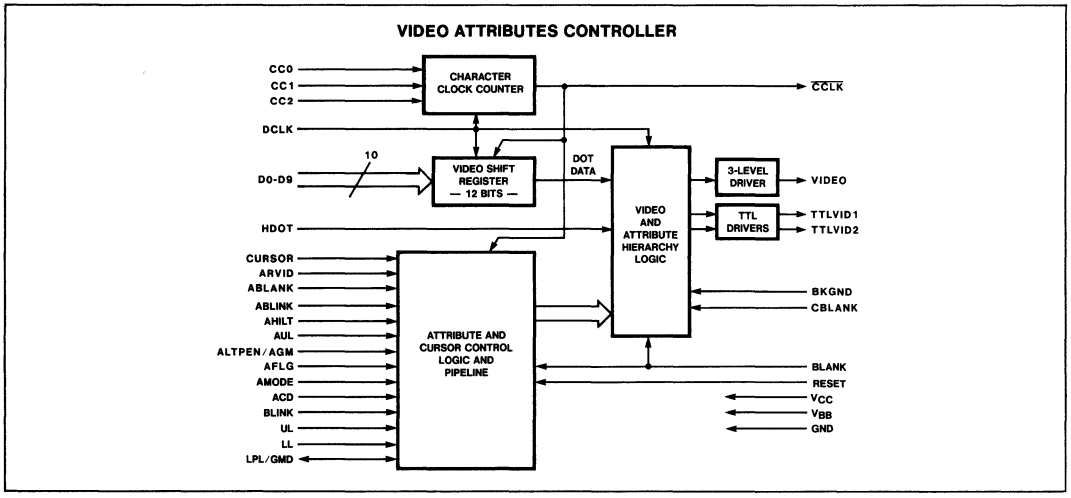


TOP VIEW

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%, V_{BB} = 1.5V ± 10%, T_A = 0°C to 70°C	
	GRAPHICS ATTRIBUTE	LIGHT PEN ATTRIBUTE
Ceramic DIP	SC2673BC5I40	SC2673AC5I40
Plastic DIP	SC2673BC5N40	SC2673AC5N40

BLOCK DIAGRAM



VIDEO ATTRIBUTES CONTROLLER (VAC) SC2673

Preliminary

PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DCLK	32	I	**Dot Clock:** Dot frequency input. Video output shift rate.
$\overline{CCLK}$	36	O	**Character Clock:** A submultiple of DCLK. The frequency ranges from one sixth to one twelfth of DCLK, as determined by the state of the CC0-CC2 inputs.
CC2-CC0	33-35	I	**Character Clock Control:** The logic state on these three static inputs determine the internal divide factor for the $\overline{CCLK}$ output rate. Character clock rates of 6 thru 12 dots per character may be specified.
D0-D9	37-39, 2-8	I	**Dot Data Input:** These are parallel inputs corresponding to the character/graphic symbol dot data for a given scan line. These inputs are strobed into the video shift register on the falling edge of each character clock.
HDOT	27	I	**Half Dot Shift:** When this input is high, the serial video output is delayed by one half dot time. This input is latched on the falling edge of each character clock.
CURSOR	14	I	**Cursor Timing:** This input provides the timing for the cursor video. When high, effectively reverses the intensities of the video and attributes. Cursor position, shape, and blink rate are controlled by this input.
BKGND	10	I	**Background Intensity:** Specifies light or dark video during BLANK and character fields. Affects the intensities of all attributes.
BLANK	15	I	**Screen Blank:** When high, this input forces the video outputs to the level specified by the BKGND input (either high or low intensity). Not effective when CBLANK is high.
CBLANK	31	I	**Composite Blank:** Used with the TTL video outputs only. When high, this input forces the video outputs to a low intensity state for retrace blanking. When BKGND input is low, or when using video outputs, this input may be tied low.
ARVID	22	I	**Reverse Video Attribute:** The intensity of the associated character or field video is reversed. All other attributes are effectively reversed.
AHILT	23	I	**Highlight Attribute:** All dot video (including underline) of the associated character or field is highlighted with respect to the BKGND input and the reverse video attribute.
ABLANK	26	I	**Blank Attribute:** Generates a blank space in the associated character or field. The blank space intensity is determined by the BKGND input, the reverse video attribute, and the CURSOR input.
ABLINK	25	I	**Blink Attribute:** The associated character or field video is driven to the intensity determined by BKGND and the reverse video attribute when the BLINK input is high.
AUL	24	I	**Underline Attribute:** Specifies a line to be displayed on the character or field. The line is specified by the UL input. All other attributes apply to the underline video.
ALTPEN/AGM	21	I	**Light Pen Attribute (2673A):** Specifies a highlighted line to be displayed on the character or field. The line is specified by the LPL input.
		I	**Attribute Graphics Mode (2673):** This input is latched and synchronized to provide a field GMD output for the 2670 DCGG.
AMODE	12	I	**Attribute Mode:** Specifies character (AMODE = 0) or field (AMODE = 1) attributes mode.
AFLG	13	I	**Attributes Flag:** The VAC samples and latches the attributes inputs when this input is high. If field attributes are specified (AMODE = 1), the attributes are double buffered on a row basis. Thus, each scan line of every character row will start with the attributes that were valid at the end of the previous row.
ACD	11	I	**Attribute Control Display:** In field attributes mode (AMODE = 1), if ACD = 0, the first character in each new attribute field (the attribute control character) will be suppressed and only the attributes will be displayed. If ACD = 1, the first character and the attributes are displayed. This input has no effect in character mode (AMODE = 0).

VIDEO ATTRIBUTES CONTROLLER (VAC) SC2673

Preliminary

PIN DESIGNATION (continued)

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
BLINK	17	I	**Blink:** This input is sampled on the falling edge of BLANK to provide the blink rate for the character blink attribute It should be a submultiple of the frame rate
UL	16	I	**Underline:** Indicates the scan line(s) for the underline attribute. Latched on the falling edge of BLANK.
LPL/GMD	19	I	**Light Pen Line (2673A):** Indicates the scan line(s) for the light pen strike-thru attribute. Latched on the falling edge of BLANK.
		O	**Graphics Mode (2673):** This output provides a synchronized, latched, field graphics mode corresponding to the AGM input This output can be used to control the GM input on the 2670 DCGG.
LL	18	I	**Last Line:** Indicates the last scan line of each character row Used internally to extend field attributes across row boundaries Latched on the falling edge of BLANK. This input has no effect in character mode (AMODE = 0).
VIDEO	28	O	**Video:** A three level serial video output which corresponds to the composite dot pattern of characters, attributes and cursor.
TTLVID1	30	O	**TTL Video 1:** This output corresponds to the serial, non-highlighted video dot pattern
TTLVID2	29	O	**TTL Video 2:** This output corresponds to the highlighted serial video dot pattern Should be used with TTLVID1 to decode a composite video of three intensities
RESET	9	I	**Manual Reset:** This active high input initializes the internal logic and resets the attribute latches. Normally used for testing.
V_{CC}	40	I	**Power Supply:** +5 Volts ± 5%
V_{BB}	1	I	**Bias Supply:** +1.5 Volts ± 10%
GND	20	I	**Ground:** 0V reference

FUNCTIONAL DESCRIPTION

The VAC consists of four major sections (see block diagram). The high speed dot clock input is divided internally to provide a character clock for system timing. The parallel dot data is loaded into the video shift register on each character boundary and shifted into the video logic block at the dot rate. The six attribute inputs are latched internally and combined with the serial dot data to provide a three level video source for the monitor.

			$\overline{CCLK}$	
CC2	CC1	CC0	DOTS/CHARACTER	DUTY CYCLE
0	0	0	6	3/3
0	0	1	6	3/3
0	1	0	7	4/3
0	1	1	8	4/4
1	0	0	9	5/4
1	0	1	10	5/5
1	1	0	11	6/5
1	1	1	12	6/6

A separate BLANK input defines the active screen area. When BLANK = 0, the video levels are derived internally by the combinations of dot data, attributes, cursor, and the state of the BKGND input. Either black or white background can be selected. Symbols (dot data) are normally gray and can be highlighted to white or black as shown in figure 1. Note that the VIDEO output is inverted as referenced to the TTL video outputs.

During the inactive screen area (BLANK = 1), the video level produced by the TTL outputs is either white (BKGND = 1) or black (BKGND = 0). A separate composite blank (CBLANK) input is provided to suppress raster retrace video when white background is specified. During the inactive screen area (BLANK = 1), the video level produced by the VIDEO output is either black (BKGND = 1) or white (BKGND = 0). For the latter case, raster retrace video suppression is accomplished by raising the BKGND input during horizontal and vertical retrace intervals For black background, tie BKGND high. Tie CBLANK input low for both cases.

Character Clock Counter

The character clock counter divides the frequency on the DCLK input to generate the character clock ($\overline{CCLK}$). The divide factor is specified by the clock control inputs (CC0-CC2) as follows:

Video Shift Register

On each character boundary, the parallel data (D0-D9) is loaded into the video shift register. The data is shifted out least significant bit first (D0) by the DCLK. If 11 or 12 dots/character are specified (CC2-CC0 = 110 or 111), a 0 (blank dot) is always shifted out before D0. For 12 dots/character, a 0 is also shifted out after D9. The serial dot data is shifted into the video logic where it is combined with the cursor and attributes to encode three levels of video.

Attribute and Cursor Control

The VAC visual attributes capabilities include: reverse video, character blank, blink, underline, highlight, and light pen strike-thru. The six attributes and the three attribute control inputs (AMODE, AFLG, and ACD) are clocked into the VAC on the falling edge of $\overline{CCLK}$. If AFLG is high, the attributes are latched internally and are effective for either one character time (AMODE = 0) or until another set of attributes is latched (AMODE = 1). The attributes set is double buffered on a row by row basis internally. Using this technique, field attributes can extend across character row boundaries thereby

VIDEO ATTRIBUTES CONTROLLER (VAC) SC2673

Preliminary

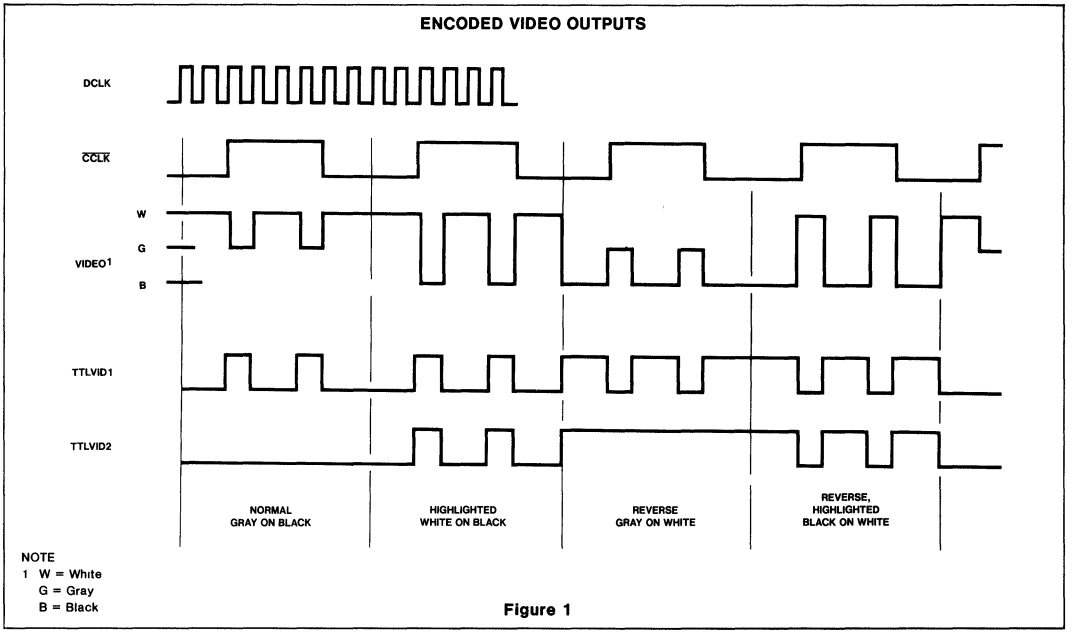


Figure 1

eliminating the necessity of starting each row with an attribute set.

When field attribute mode is selected, (AMODE = 1), the VAC will accommodate two attribute storage configurations. In one configuration, the attribute control data is stored in the refresh RAM, taking the place of the first character code in the field to be affected. For this mode, the ACD input is tied low and blank characters will be displayed in the screen positions occupied by the attribute data (see figure 10). In the second configuration, (ACD = 1), the character codes and attribute data are presented to the VAC in parallel. In this mode, dot data is displayed at each character position (see figure 11).

The CURSOR and the attribute input signals are pipelined internally to allow for system propagations (one $\overline{CCLK}$ for refresh RAM, one $\overline{CCLK}$ for dot generator). The attribute timing signals BLINK, UL, LPL and LL are clocked into the VAC at the beginning of each scan line by the falling edge of the BLANK input. Thus, these signals must be in their proper state at the falling edge of BLANK preceding the scan line at which they are to be active (see figure 4).

Video Logic

The serial dot data and the pipelined cursor and attributes are combined to generate the three level current source on the VIDEO output. The three levels (white, gray, and black) are also encoded on the two TTL compatible outputs TTLVID1 and TTLVID2. The three levels are encoded as shown.

TTLVID2	TTLVID1	INTENSITY
0	0	Black (or CBLANK)
0	1	Gray (on black surround)
1	0	Gray (on white surround)
1	1	White

NOTE
The TTLVID1 output can be used independently to generate a two level non-highlighted video

The video is normally shifted out on the leading edge of the DCLK. When the HDOT input is asserted, the corresponding dot data is delayed by one-half DCLK. This half dot shifting, when used on selected lines of character video, can be used to effect eye-pleasing character rounding as shown in figure 2.

Attribute Hierarchy

The video of each character block consists of four components as shown in figure 3.

Symbol video is generated from the dot data inputs D0-D9.

Underline video is enabled by the AUL attribute and is generated when the UL timing input is active. Underline and symbol video are always the same intensity.

Strike-thru video is enabled by the ALTPEN attribute and is generated when the LPL timing input is active. This video is always highlighted and takes precedence over the symbol and underline video. This feature applies to the 2673A only.

Surround video is the absence of symbol, underline and strike-thru video or the presence of the non-display attributes (ABLANK or ABLINK • BLINK).

The relative intensities of the four video components are determined by the remaining attributes (AHILT, ABLANK, ABLINK, ARVID) and the BKGND and CURSOR inputs as illustrated in table 1.

VIDEO ATTRIBUTES CONTROLLER (VAC) SC2673

Preliminary

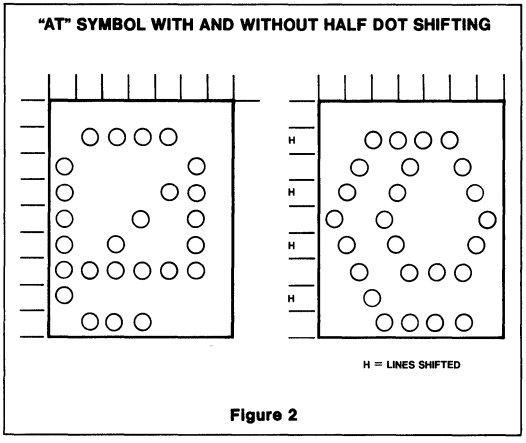


Figure 2

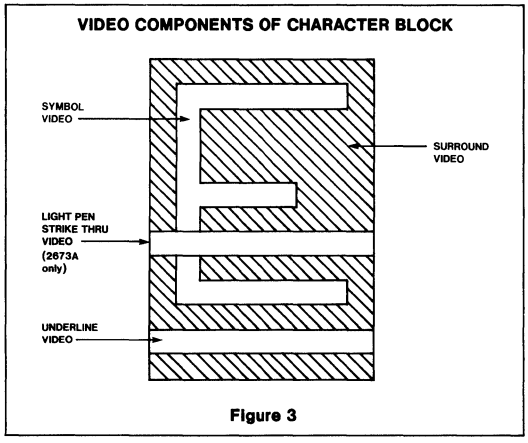


Figure 3

ATTRIBUTES AND CONTROL INPUTS d = don't care				RELATIVE VIDEO INTENSITIES W = White, B = Black, G = Gray		
BKGND[5]	REVERSE[1]	NON-DISPLAY[2]	AHILT	STRIKE THRU VIDEO[3]	SYMBOL OR UNDERLINE VIDEO[3,4]	SURROUND VIDEO[3]
0	0	0	0	W	G	B
0	0	0	1	W	W	B
0	0	1	d	B	B	B
0	1	0	0	B	G	W
0	1	0	1	B	B	W
0	1	1	d	W	W	W
1	0	0	0	B	G	W
1	0	0	1	B	B	W
1	0	1	d	W	W	W
1	1	0	0	W	G	B
1	1	0	1	W	W	B
1	1	1	d	B	B	B

NOTES
1 Reverse = ARVID • $\overline{\text{CURSOR}}$ + $\overline{\text{ARVID}}$ • CURSOR
2 Non-display = ABLANK + ABLINK • BLINK
3 See figure 3
4 Symbol and underline video are always the same intensity
5 Reverse sense for VIDEO output

Table 1. ATTRIBUTES HIERARCHY

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground	−0.5 to +6.0	V

NOTES
1 Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device This is stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2 For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 60°C/W junction to ambient (ceramic package)

VIDEO ATTRIBUTES CONTROLLER (VAC) SC2673

Preliminary

DC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{BB} = +1.5V ±10%[3,4,5]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		2.0			V
V_{OL}	Output low voltage (except VIDEO)	I_{OL} = 1.6mA			0.4	V
V_{OH}	Output high voltage (except VIDEO)	I_{OH} = −100μA	2.4			V
V_B	VIDEO black level	R_L = 75Ω to GND		0		V
V_G	VIDEO gray level	R_L = 75Ω to GND		0.225		V
V_W	VIDEO white level	R_L = 75Ω to GND		0.50		V
I_{IL}	Input low current	V_{IN} = 0.4V			−400/ −800[10]	μA
I_{IH}	Input high current	V_{IN} = 2.4V			20/40[10]	μA
I_{CC}	V_{CC} supply current	V_{IN} = 0V, V_{CC} = max			50	mA
I_{BB}	V_{BB} supply current	V_{BB} = max			100	mA

AC ELECTRICAL CHARACTERISTICS T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{BB} = +1.5V ±10%[3,4,5]

PARAMETER		TEST CONDITIONS	TENTATIVE LIMITS			UNIT
			Min	Typ	Max	
Dot clock[6]						
t_D	frequency				25	MHz
t_{DH}	high		15			ns
t_{DL}	low		15			ns
Setup times to $\overline{CCLK}$[7]						
t_{BS}	BLANK		35			ns
t_{SC}	BLINK, UL, LPL, LL (ref to BLANK)		20			ns
t_{SA}	Attributes		35			ns
t_{SD}	Dot data D0-D9		70			ns
t_{SK}	CURSOR		35			ns
t_{FS}	AFLG		50			ns
t_{SH}	HDOT		35			ns
Hold times from $\overline{CCLK}$[7]						
t_{HC}	BLINK, UL, LPL, LL (ref to BLANK)		20			ns
t_{HA}	Attributes		35			ns
t_{HD}	Dot data D0-D9		0			ns
t_{HK}	CURSOR		35			ns
t_{FH}	AFLG		50			ns
t_{HH}	HDOT		35			ns
Setup times to DCLK[8]						
t_{SG}	BKGND		15			ns
t_{SB}	CBLANK		15			ns
Hold times from DCLK[8]						
t_{HG}	BKGND		15			ns
t_{HB}	CBLANK		15			ns
Delay times[9]		C_L = 150pF				
t_{DGM}	GMD from DCLK				60	ns
t_{DC}	CCLK from DCLK				60	ns
t_{DV}	VIDEO, TTLVID1, and TTLVID2 from DCLK				75	ns

NOTES

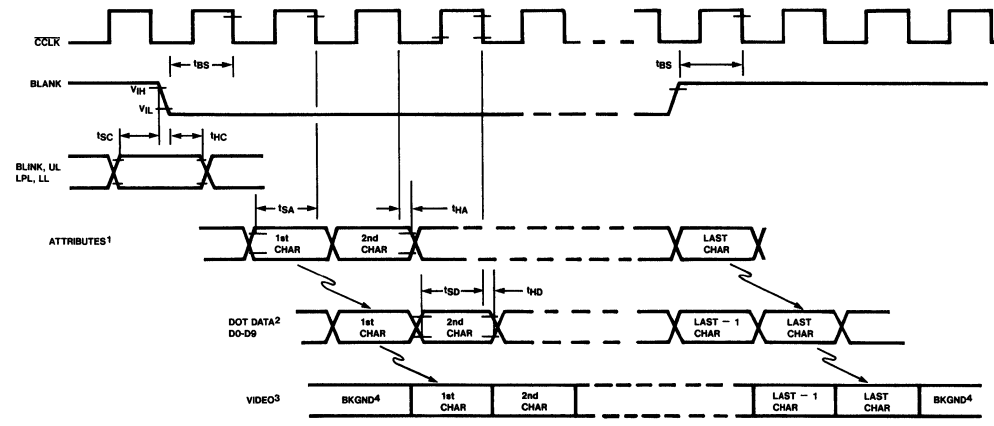
3 Parameters are valid over operating temperature range unless otherwise specified.

4. All voltage measurements are referenced to ground (V_{SS}). All input signals swing between 0 4V and 2 4V All time measurements are referenced at input voltages of 0.8V, 2.0V and at output voltages of 0 8V, 2.0V as appropriate.

5 Typical values are at +25°C, typical supply voltages and typical processing parameters

6. See figure 7. Half dot shift feature 18MHz max
7. See figures 4, 5, 6, and 9
8. See figure 8
9 See figures 6 and 7.
10 For DCLK input

VAC PIPELINE TIMING



NOTES
1. Attributes include: ABLINK, ABLANK, ARVID, AUL, AHILT, and ALTPEN.
2. One $\overline{CCLK}$ delay for dot data (obtained from delay through character generator).
3. See figure 7 for detail timing of VIDEO, TTLVID1, TTLVID2.
4. Non-active scan time. VIDEO reverts to polarity selected by the BKGND input.

Figure 4

CURSOR PIPELINE TIMING

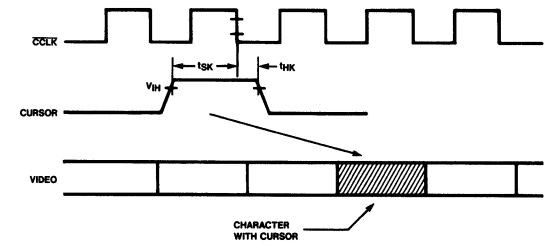
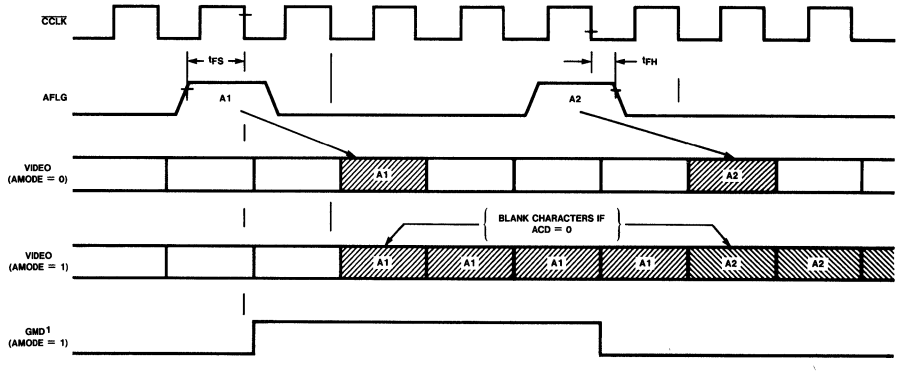


Figure 5

Preliminary

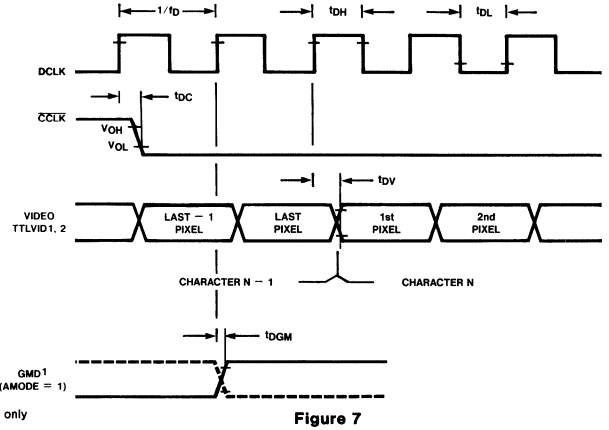
CHARACTER (AMODE = 0), FIELD (AMODE = 1), AND GMD ATTRIBUTE TIMING



NOTE
1 GMD output in 2673 version only See figure 7 for detail timing

Figure 6

VIDEO AND GMD PIPELINE TIMING



NOTE
1 GMD output in 2673 version only

Figure 7

BKGND AND CBLANK TIMING DURING INACTIVE SCAN TIME (BLANK = 1)

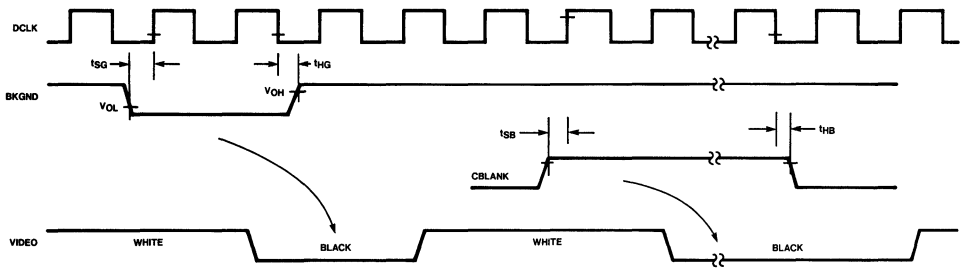


Figure 8

HALF DOT SHIFT TIMING

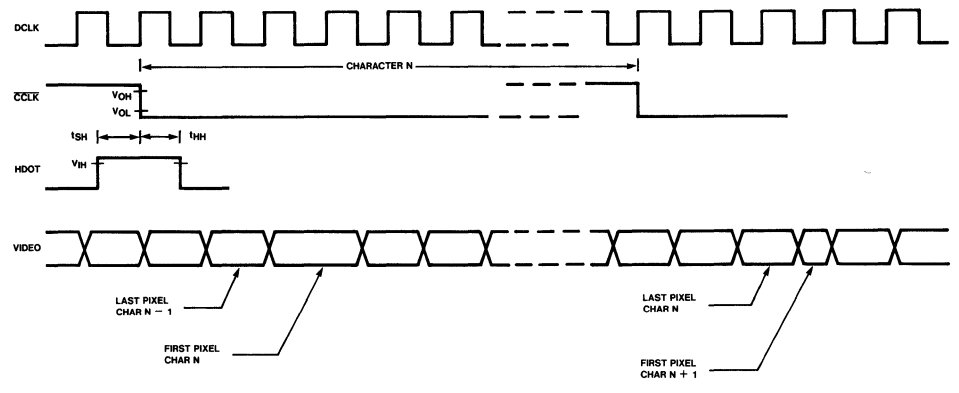


Figure 9

Preliminary

SYSTEM BLOCK DIAGRAM OF THE 2673 IN FIELD ATTRIBUTE MODE USING THE NARROW RAM (8 WIDE) CONFIGURATION

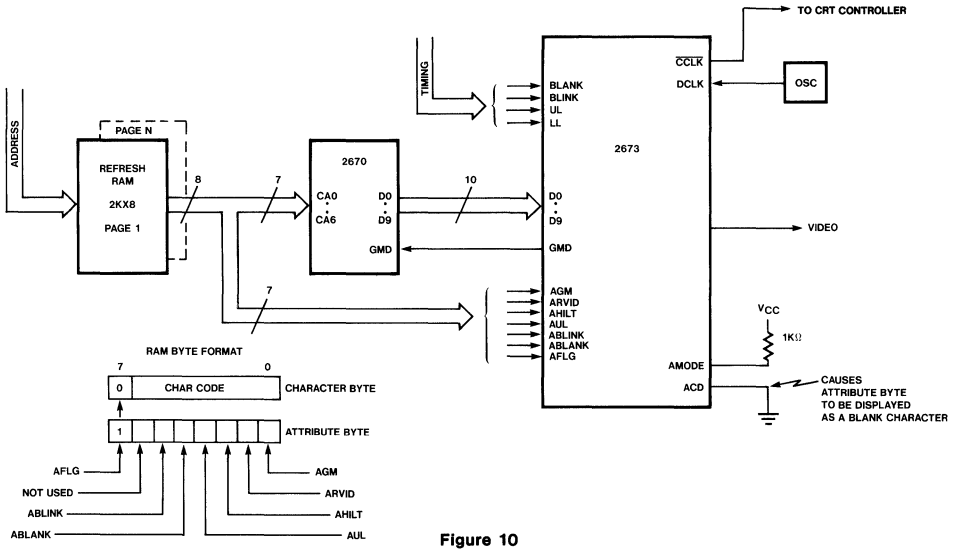
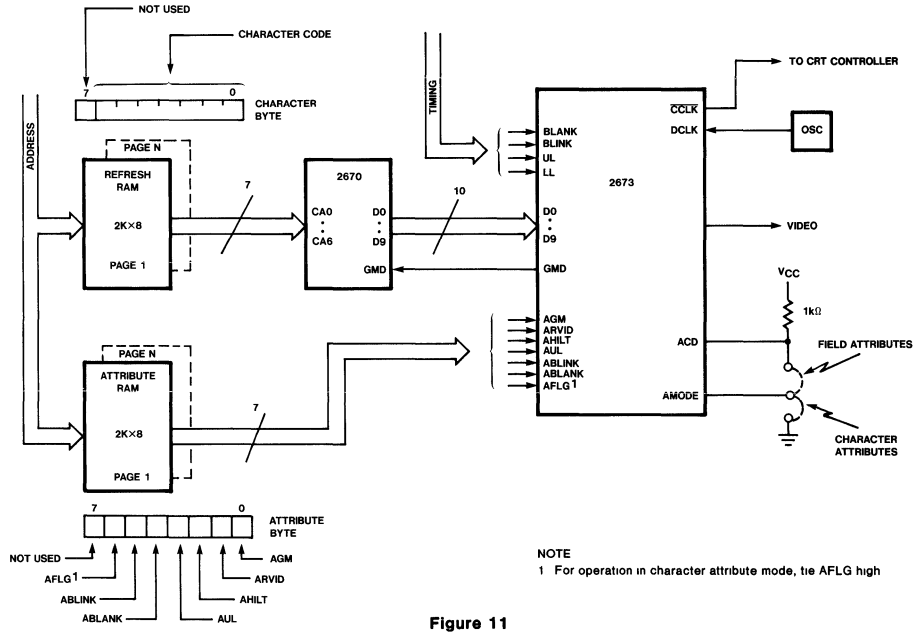


Figure 10

SYSTEM BLOCK DIAGRAM OF THE 2673 IN FIELD OR CHARACTER ATTRIBUTE MODE USING THE WIDE RAM CONFIGURATION



NOTE
1 For operation in character attribute mode, tie AFLG high

Figure 11

VIDEO OUTPUT STAGES OF THE 2673

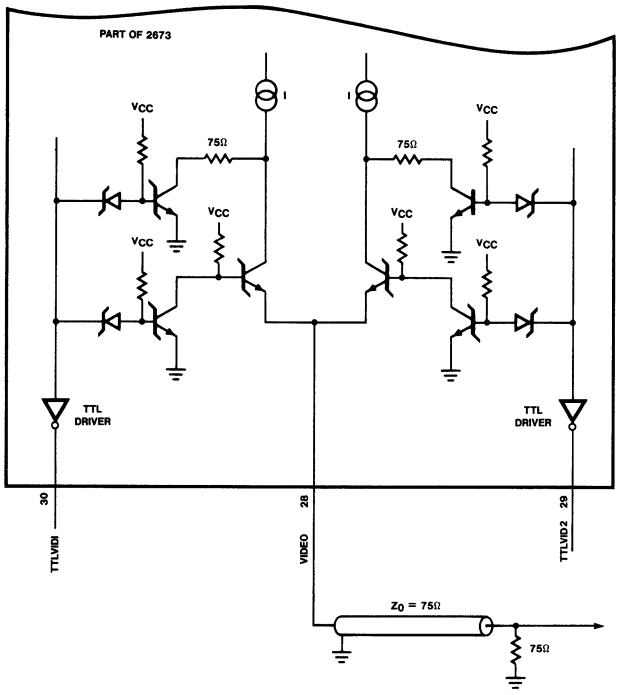


Figure 12

VIDEOTEXT TIMING CHAIN (VTC) SAA5020/SAA5025

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

DESCRIPTION

The Signetics SAA5020/SAA5025 Videotext Timing Chains (VTIC) are MOS N-channel integrated circuits which perform the timing functions necessary for the display of viewdata and teletext information on an interlaced or non-interlaced CRT monitor.

The SAA5020/SAA5025 are compatible with the British videotext standards, currently implemented in systems such as Prestel, Ceefax, and Oracle. The SAA5020 is intended for use with PAL (625 line) television standards, while the SAA5025 is intended for use with systems employing the NTSC (525 line) television standard.

The basic input to the VTIC is a 6MHz clock signal. This is subdivided internally to produce various synchronized timing outputs including the character and dot rate clocks for the character generator, a composite sync output for the monitor, and row address outputs and a column address clock for the display memory.

Several versions of the VTIC are available to meet the requirements of various applications. Basic characteristics of the variants are:

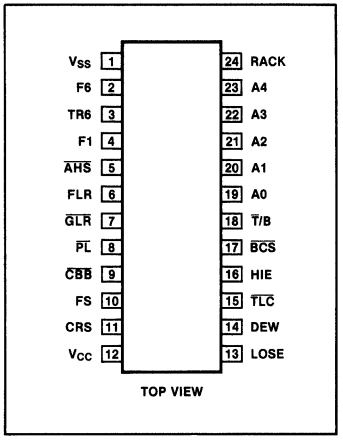
TYPE	LINES	ROWS	LINES/ROW
SAA5020	625	24	10
SAA5025A	525	20	10
SAA5025B	525	24	10
SAA5025C	525	24	8

The VTIC operates from a single 5-volt power supply and is packaged in a 24-pin dual-in-line package.

FEATURES

- **Compatible with British videotext standards**
- **625 line (PAL) and 525 line (NTSC) versions**
- **40 characters per row, 20 or 24 rows per screen**
- **Sync inputs allow synchronization with other video sources**
- **Composite sync output**
- **Display addressing outputs**
- **Double height character capability**
- **Character rounding output to SAA5050**
- **Single 5-volt power supply**

PIN CONFIGURATION

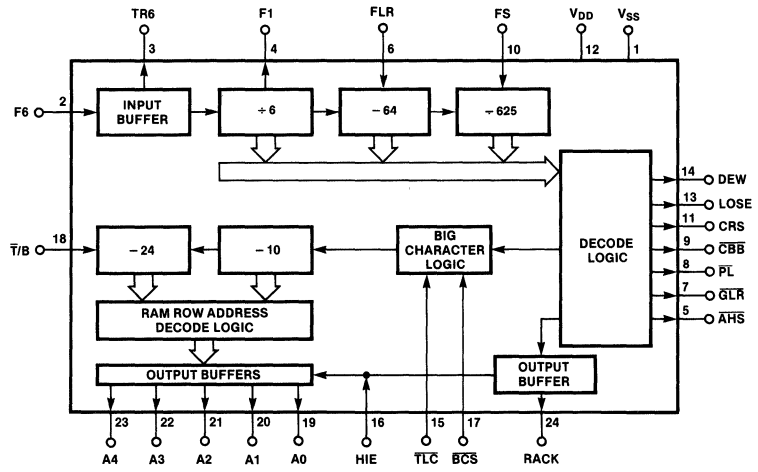


TOP VIEW

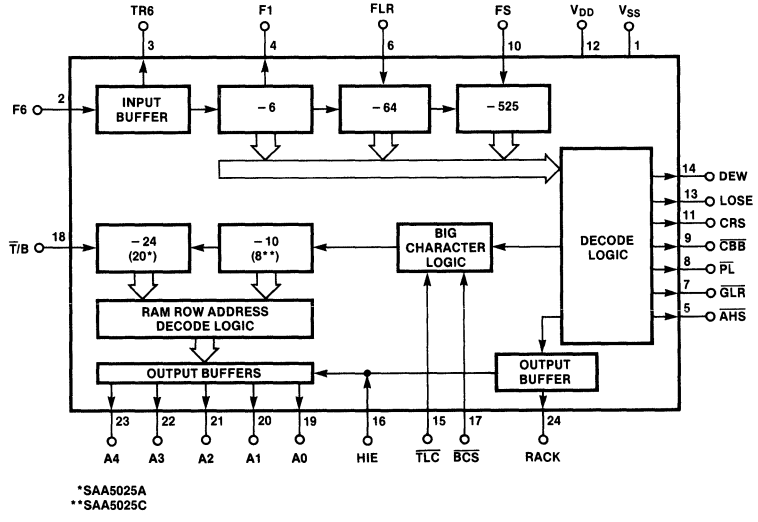
PIN DESIGNATION

MNEMONIC	PIN	TYPE	FUNCTION
F6	2	I	**6MHz input.** Master clock signal used to derive the basic timing for the display.
TR6	3	O	**6MHz output.** Buffered 6MHz dot rate clock output to the SAA5050 character generator.
F1	4	O	**1MHz output.** Character clock rate output signal, synchronous with TR6, to the character generator and other external circuits.
$\overline{AHS}$	5	O	**After hours sync.** Active low composite sync output to the display.
FLR	6	I	**Fast line reset.** Input used to reset the internal line rate counter.
$\overline{GLR}$	7	O	**General line reset.** Line frequency active low signal used for reset and clock functions in the character generator and other external circuits.
$\overline{PL}$	8	O	**Phase lock.** Line frequency active low output to the teletext video processor used to phase lock the 6MHz display clock to the incoming television video signal.
$\overline{CBB}$	9	O	**Color burst blanking.** Active low output to the teletext video processor.
FS	10	I	**Field sync.** Input signal used to reset the field rate counter to maintain correct field sync with incoming video.
CRS	11	O	**Character rounding select.** Output used by the character generator for character rounding.
LOSE	13	O	**Load output shift register enable.** Output signal to the SAA5050 character generator used to reset internal control flip-flops prior to the start of each line and to define the character display period.
DEW	14	O	**Data entry window.** Output required by the teletext acquisition circuit and character generator which defines the period during which data may be extracted from the incoming TV signal and written into page memory.
$\overline{TLC}$	15	I	**Transmitted large character.** Input from the character generator used to enable the correct display of large characters under attribute control.
HIE	16	I	**High impedance enable.** A high input switches the A0-A4 and RACK outputs to their high impedance state.
$\overline{BCS}$	17	I	**Big character select.** When low causes all characters to be displayed at double height. Used in conjunction with $\overline{T}$/B input.
$\overline{T}$/B	18	I	**Top or bottom select.** When BCS is low this input controls the row address outputs to cause the top half to be displayed when low and the bottom half to be displayed when high.
A0-A4	19-23	O	**Display memory row address.** Provides a binary count sequence during the display period which is incremented every 10 (8 for SAA5025C) lines in normal character mode and every 20 (16 for SAA5025C) lines in large character mode. If any row contains attributed large characters the address is incremented by two after 20 (16) lines.
RACK	24	O	**Column address clock.** 1MHz clock used to clock the RAM column address counter. It occurs only during the active display period of each scan line.
V_{CC}	12	I	**+5 volts power input.**
V_{SS}	1	I	**Signal and power ground.**

SAA5020 BLOCK DIAGRAM



SAA5025 BLOCK DIAGRAM



VIDEOTEXT CHARACTER GENERATOR (VCG) SAA5050 SERIES

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

DESCRIPTION

The Signetics SAA5050 Series Videotext Character Generators (VCG) are MOS N-channel integrated circuits which perform the attribute decoding and character generation functions necessary for the display of viewdata and teletext information on a color or black and white CRT monitor. They are compatible with the British viedotext standards, currently implemented in systems such as Prestel, Ceefax, and Oracle.

The VCG incorporates a character generator read only memory (ROM), decoding for the 32 videotext control and attribute characters, video shift registers, and decoding for some of the remote control functions generated by compatible remote control circuits. The circuit generates 96 alphanumeric and 64 graphic characters.

The basic input to the VCG is character data from the display page memory. Each character code defines a dot matrix pattern. Each character block is six dots wide and ten TV lines high, with dot rate of 6MHz and character period of one microsecond. Alphanumeric characters are generated on a 5 x 9 matrix, allowing space for lower case descenders, with one dot between characters and one TV line between character rows. The alphanumeric characters are rounded, i.e. a half dot is inserted before or after a whole dot during the interlace frame of the TV picture in the presence of a diagonal in the character matrix.

Each of the 64 graphic characters is decoded to form a 2 x 3 block arrangement which occupies the complete 6 x 10 matrix. Graphic characters may be either contiguous or separated.

The character video signals comprise a monochrome signal and RGB signals for a color monitor. The monochrome data signal can be used to inlay characters into TV video. A blanking output is provided to blank out the TV picture signal for inserted box applications.

The SAA5050 series devices are functionally identical except for the character font stored in the character generator ROM. The part types currently available are:

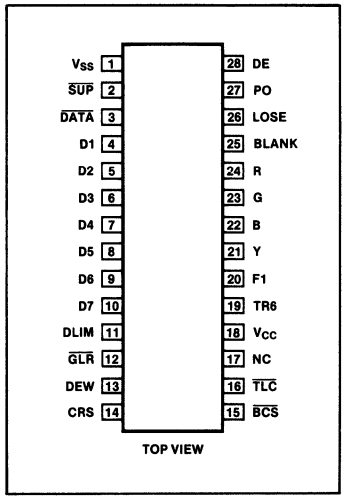
TYPE	CHARACTER SET
SAA5050	English
SAA5051	German
SAA5052	Swedish
SAA5055	American

The VCG operates from a single 5-volt power supply and is packaged in a 28-pin dual-in-line package.

FEATURES

- **Compatible with British videotext standards**
- **40 characters per row, 10 or 20 scan lines per row**
- **96 alphanumeric characters with rounding**
- **64 graphic characters, contiguous or separated**
- **Double height and blinking character capability**
- **Decoding of control and attribute characters**
- **Decoding of remote control commands**
- **RGB and monochrome outputs**
- **Overlay and inserted box capability**
- **Single 5-volt power supply**

PIN CONFIGURATION

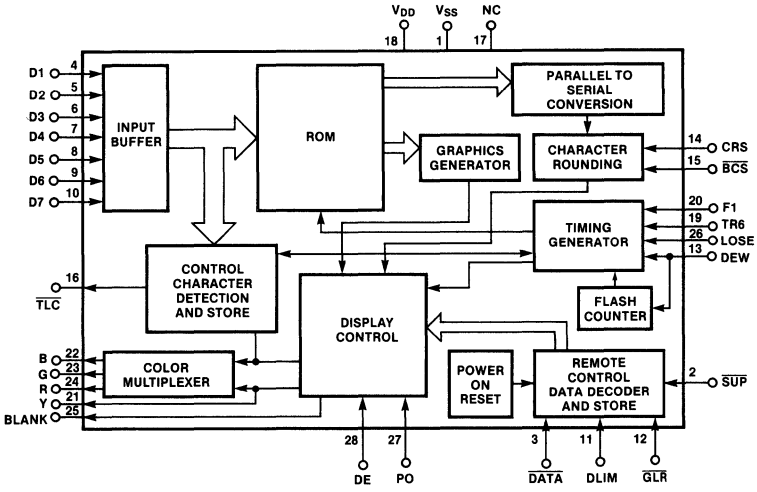


TOP VIEW

PIN DESIGNATION

MNEMONIC	PIN	TYPE	FUNCTION
$\overline{SUP}$	2	I/O	**Superimpose.** As an open drain output, it is low when the superimpose mode is selected to allow contrast reduction of the TV picture if required. As an input, if held low, the internal 'TV mode' flip-flop is held in the 'text' state. This is for VDU applications when remote control is not used.
$\overline{DATA}$	3	I	**Remote control data.** This input accepts a 7-bit serial data stream from the remote control decoder.
D1-D7	4-10	I	**Character code.** 7-bit parallel code from the page memory which specifies alphanumeric, graphic, or control characters.
DLIM	11	I	**Remote control clock.** Clock used to sample the input at the DATA pin. The positive edge of every second clock pulse is at the nominal center of the data bit.
$\overline{GLR}$	12	I	**General line reset.** Active low input from the SAA5020/SAA5025 VTIC used for internal synchronization of remote control data signals.
DEW	13	I	**Data entry window.** Input from the SAA5020/SAA5025 VTIC used to reset the ROM row address counter prior to the display period. Also used to derive the character blink period.
CRS	14	I	**Character rounding select.** Input from the SAA5020/SAA5025 VTIC used to effect rounding of characters.
$\overline{BCS}$	15	I	**Big character select.** When low causes all characters to be displayed at double height.
$\overline{TLC}$	16	O	**Transmitted large character.** Output to the VTIC used to enable the correct display of large characters under attribute control.
TR6	19	I	**Dot rate clock.** 6MHz clock from the VTIC.
F1	20	I	**Character rate clock.** 1MHz clock from the VTIC used to latch the incoming character data and to synchronize internal circuits.
Y	21	O	**Monochrome output.** Open drain serial video output which is in the high state whenever an alphanumeric or graphic character is required on the display.
B,G,R	22-24	O	**Blue, green, and red outputs.** Open drain serial video outputs to the monitor drive circuits. They are high whenever the corresponding color gun is to be active. The video is a composite of background and foreground (character) information.
BLANK	25	O	**Blanking.** Open drain output which provides TV picture blanking. It is active for a duration of a box when the PO and DE inputs are on. It is also activated permanently when no TV picture is required (PO low).
LOSE	26	I	**Load output shift register enable.** Input signal from the VTIC used to reset internal control flip-flops prior to the start of each line and to define the character display period.
PO	27	I	**Picture on.** Input used to control the character video and blanking outputs. When high, only text in boxes is displayed unless in superimpose mode. The input is high for TV picture video on, low for picture off.
DE	28	I	**Display enable.** Input used to control the videotext display. High for display on, low for display off.
V_{CC}	18	I	**+5 volts power input.**
V_{SS}	1	I	**Signal and power ground.**

SAA5050 BLOCK DIAGRAM



SAA5050 CHARACTER SET

BITS b7 b6 b5 / b4 b3 b2 b1 / ROW	COL 0 (0 0 0)	COL 1 (0 0 1)	COL 2 (0 1 0)	COL 2a	COL 3 (0 1 1)	COL 3a	COL 4 (1 0 0)	COL 5 (1 0 1)	COL 6 (1 1 0)	COL 6a	COL 7 (1 1 1)	COL 7a
0 0 0 0 0	NUL*	DLE*			0		@	P	—		p	
0 0 0 1 1	ALPHA^{n} RED	GRAPHICS RED	!		1		A	Q	a		q	
0 0 1 0 2	ALPHA^{n} GREEN	GRAPHICS GREEN	"		2		B	R	b		r	
0 0 1 1 3	ALPHA^{n} YELLOW	GRAPHICS YELLOW	£		3		C	S	c		s	
0 1 0 0 4	ALPHA^{n} BLUE	GRAPHICS BLUE	$		4		D	T	d		t	
0 1 0 1 5	ALPHA^{n} MAGENTA	GRAPHICS MAGENTA	%		5		E	U	e		u	
0 1 1 0 6	ALPHA^{n} CYAN	GRAPHICS CYAN	&		6		F	V	f		v	
0 1 1 1 7	ALPHA^{n}** WHITE	GRAPHICS WHITE	'		7		G	W	g		w	
1 0 0 0 8	FLASH	CONCEAL DISPLAY	(		8		H	X	h		x	
1 0 0 1 9	STEADY**	CONTIGUOUS** GRAPHICS	)		9		I	Y	i		y	
1 0 1 0 10	END BOX**	SEPARATED GRAPHICS	*		:		J	Z	j		z	
1 0 1 1 11	START FOX	ESC*	+		;		K	←	k		¼	
1 1 0 0 12	NORMAL** HEIGHT	BLACK** BACKGROUND	,		<		L	½	l		‖	
1 1 0 1 13	DOUBLE HEIGHT	NEW BACKGROUND	-		=		M	→	m		¾	
1 1 1 0 14	S0*	HOLD GRAPHICS	.		>		N	↑	n		÷	
1 1 1 1 15	S1*	RELEASE** GRAPHICS	/		?		O	#	o		■	

Control characters shown in columns 0 and 1 are normally displayed as spaces.
The SAA5050 character set is shown as an example

*These control characters are reserved for compatibility with other codes

**These control characters are presumed before each row beings

□ Character rectangle

Black represents display color

White represents background

VIEWDATA INPUT/OUTPUT PERIPHERAL (VIOP) SAA5070

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

DESCRIPTION

The Signetics SAA5070 Viewdata Input/Output Peripheral (VIOP) is a complex microprocessor peripheral integrated circuit intended for use in wired communications systems, notably viewdata systems such as Prestel in the UK and Antiope in France. It is implemented in N-channel MOS technology and packaged in a 40-pin dual-in-line package.

The VIOP provides several peripheral functions required in viewdata terminals. It contains an autodialing circuit, a 1200 baud demodulator and asynchronous receiver, and a 75 baud modulator and asynchronous transmitter. The 75 baud modulator and asynchronous transmitter can be programmed to operate at 1200 baud for use on private telecommunications systems.

The input to the VIOP's demodulator is a filtered and squared FSK signal from the phone line. This signal is internally processed to produce a pseudo-analog output signal which, after external filtering and squaring, serves as the input to the line receiver. The modulator generates a pseudo-analog output from a serial shift register which is loaded with patterns from an internal ROM. Each sine wave cycle is comprised of a 92-bit pattern which provides a suitable FSK signal output with minimal external filtering. The sine wave frequency is determined by the selected baud rate and the value of the transmitted data.

The device also includes a tape interface circuit suitable for the recording and retrieval of character codes of pages of text from an audio cassette recorder. This is performed at 1300 baud using a modified 'Kansas City' standard.

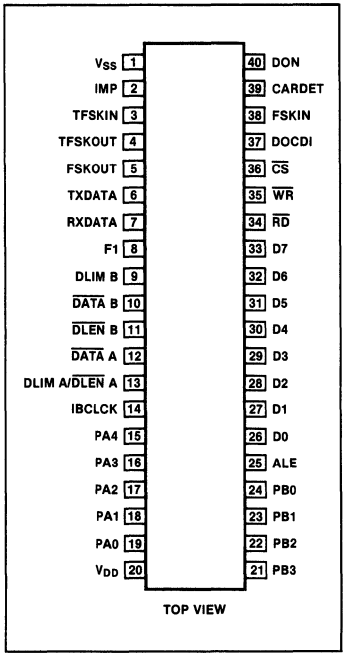
Other on-chip facilities include 1.5 and 60 second timers and two general purpose quasi-bidirectional input/output ports. One port could, for example, be used as an interface to a nonvolatile RAM that stores telephone numbers for autodialing and user passwords, while the second port could be used for display control functions.

The SAA5070 has been partitioned for flexibility of use. For example, an external modem can be used in conjunction with the internal receiver and transmitter, or the internal modem can be used independently of the internal receiver and transmitter.

FEATURES

- **Multiplexed address/data bus compatible with SC80 and SC84 Series microcomputers**
- **Modem**
  - **— 1200 baud demodulator**
  - **— 75/1200 baud modulator**
- **Line asynchronous receiver and transmitter**
- **Autodialing circuit**
- **Tape recorder 1300 baud modem (modified KC standard)**
- **Tape recorder asynchronous receiver and transmitter**
- **Remote control receiver and transmitter**
- **1.5 and 60 second timers**
- **Two general purpose I/O ports**

PIN CONFIGURATION

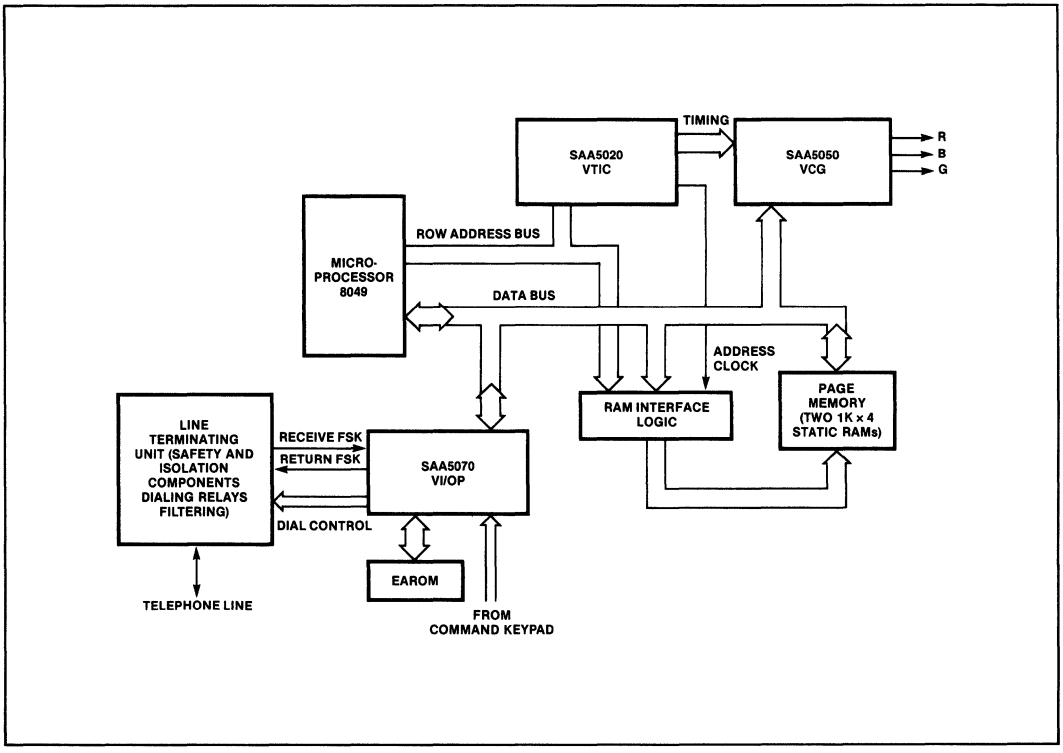


TOP VIEW

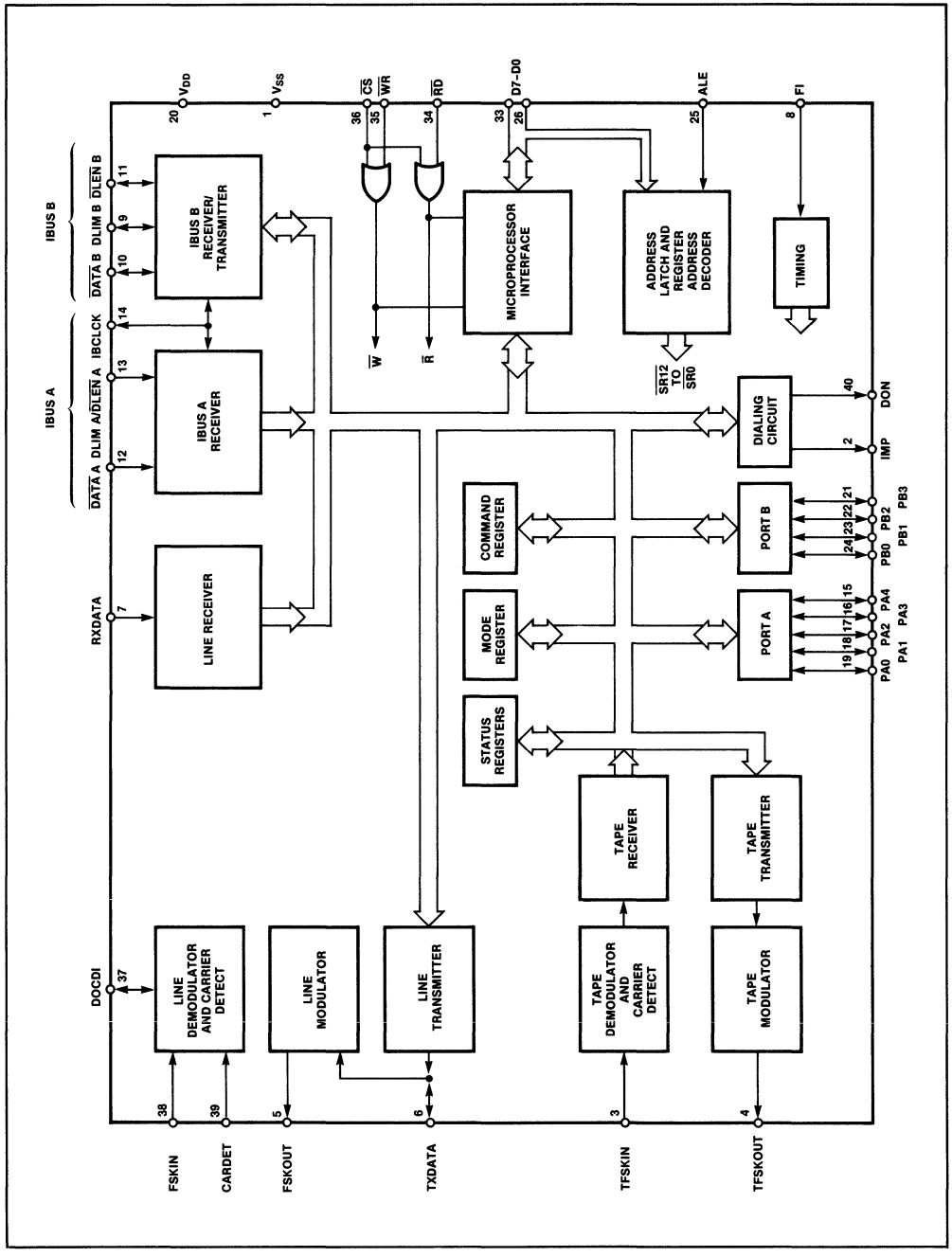
PIN DESIGNATION

MNEMONIC	PIN	TYPE	FUNCTIONS
V_{SS}	1	I	Signal and power ground
IMP	2	O	Dialing pulse output
TFSKIN	3	I	FSK input from tape player
TFSKOUT	4	O	FSK output to tape recorder
FSKOUT	5	O	Line modulator output
TXDATA	6	I/O	Line transmitter output or modulator input
RXDATA	7	I	Line data input
F1	8	I	1MHz clock input
DLIMB	9	I/O	Remote control receiver B clock input or transmitter B clock output
$\overline{\text{DATAB}}$	10	I/O	Remote control receiver B data input or transmitter B data output
$\overline{\text{DLENB}}$	11	I/O	Remote control receiver B bus enable input or transmitter B bus enable output
$\overline{\text{DATAA}}$	12	I	Remote control receiver A data input
DLIMA/$\overline{\text{DLENA}}$	13	I	Remote control receiver A clock or bus enable input
IBCLCK	14	I/O	62.5kHz clock input or output
PA4-PA0	15-19	I/O	General purpose I/O port A
V_{CC}	20	I	+ 5-volt power input
PB3-PB0	24-21	I/O	General purpose I/O port B
ALE	25	I	Address latch enable input from microprocessor
D0-D7	26-33	I/O	8-bit bidirectional address/data bus
$\overline{\text{RD}}$	34	I	Read strobe
$\overline{\text{WR}}$	35	I	Write strobe
$\overline{\text{CS}}$	36	I	Chip select
DOCDI	37	I/O	Line demodulator output or external carrier detect input
FSKIN	38	I	Filtered and squared line FSK input
CARDET	39	I	Unfiltered line FSK input
DON	40	O	Dialing in progress output

BLOCK DIAGRAM OF TYPICAL VIEWDATA RECEIVER



SIMPLIFIED BLOCK DIAGRAM



Section 3
Single Chip Microcomputers

SINGLE CHIP 8-BIT MICROCOMPUTERS SC80 SERIES

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

DESCRIPTION

The Signetics SC80 Series microcomputers are self-contained, 8-bit processors which contain the system timing, control logic, RAM data memory, ROM program memory (8048/49/50 only), and I/O lines necessary to implement dedicated control functions. All SC80 Series devices are pin and program compatible, differing only in the size of the on-board program ROM and data RAM, as follows:

TYPE	RAM SIZE	ROM SIZE
8048	64 × 8	1K × 8
8049	128 × 8	2K × 8
8050	256 × 8	4K × 8
8035	64 × 8	—
8039	128 × 8	—
8040	256 × 8	—

Program memory can be expanded externally up to a maximum total of 4K bytes without paging. Data memory can also be expanded externally. I/O capabilities can be expanded using standard devices or the 8243 I/O expander.

The SC80 Series processors are designed to be efficient control processors as well as arithmetic processors. They provide an instruction set which allows the user to directly set and reset individual lines within its I/O ports as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions make these processors very efficient in implementing standard logic functions. Also, special attention has been given to code efficiency. Over 70% of the instructions are a single byte long and all others are only 2 bytes long.

An on-chip 8-bit counter is provided which can count, under program control, either internal clock pulses (with a divide by 32 prescaler) or external events. The counter can be programmed to cause an interrupt on terminal count.

FEATURES

- **8-bit CPU, ROM, RAM, I/O in a 40-pin package**
- **24 quasi bidirectional I/O lines**
- **Two test inputs**
- **Internal counter/timer**
- **Single-level vectored interrupts: external, counter/timer**
- **Over 90 instructions, 70% single byte**
- **1.36μs or 2.5μs instruction cycle, all instructions one or two cycles**
- **Expandable memory and I/O**
- **Low voltage standby**
- **TTL compatible inputs and outputs**
- **Single +5V power supply**

FUNCTIONAL DESCRIPTION

The following is a general functional description of the SC80 Series microcomputers. Refer to the block diagram.

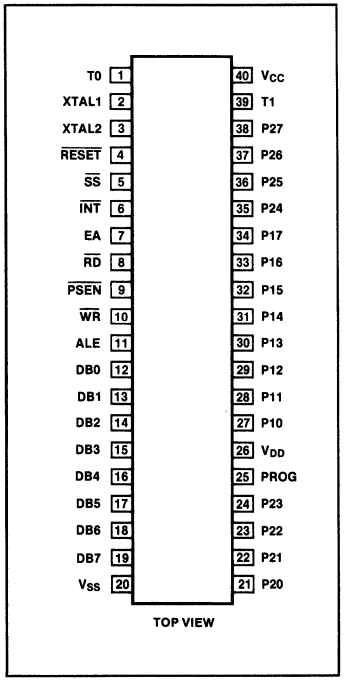
PROGRAM MEMORY

Resident program memory consists of up to 4K bytes of ROM. The program memory is divided into pages of 256 bytes each. As shown in the memory map, figure 1, program memory is also divided into two 2048-byte banks, MB0 and MB1. 4096 bytes can be addressed directly. If more memory is required, an I/O port can be used to address locations over 4095.

There are three locations in program memory of special importance. These locations contain the first instruction to be executed upon the occurrence of one of three events.

LOCATION	EVENT
0	Activation then deactivation of the $\overline{\text{RESET}}$ line.
3	Activation of the $\overline{\text{INT}}$ line when the external interrupt is enabled.
7	An overflow of the timer/counter if the T/C interrupt is enabled.

PIN CONFIGURATION

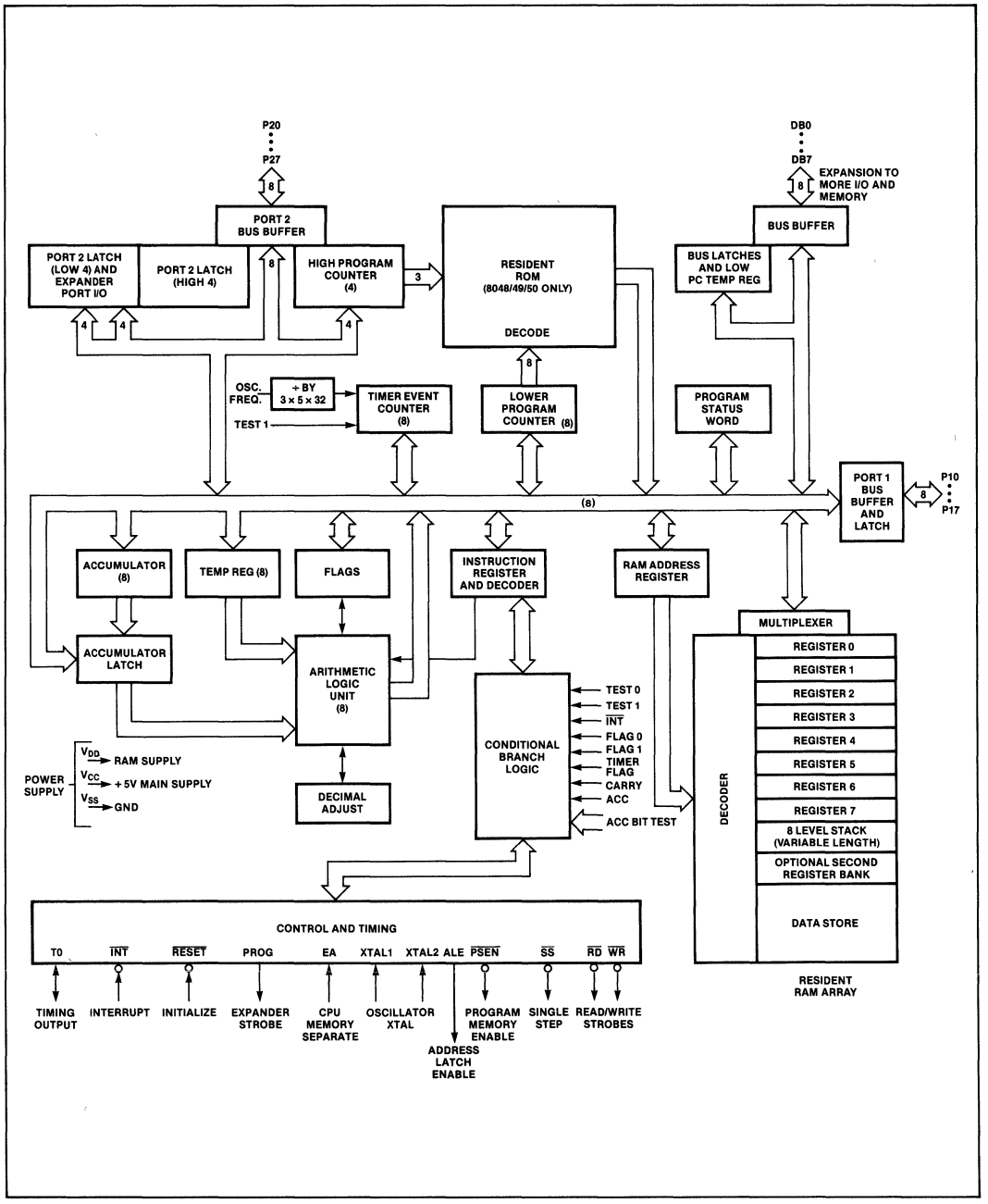


PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB0-DB7	12-19	I/O	**Bus.** Bidirectional I/O port can be read from or written into using the $\overline{RD}$ or $\overline{WR}$ strobes. This port can also be statically latched. Contains the 8 lower address bits during an access of external memory and receives the addressed instruction under control of $\overline{PSEN}$. $\overline{PSEN}$, ALE, $\overline{RD}$, and $\overline{WR}$ determine whether the access is an instruction fetch or a RAM read/write.
P10-P17	27-34	I/O	**Port 1.** 8-bit quasi-bidirectional I/O port.[1]
P20-P27	21-24, 35-38	I/O	**Port 2.** 8-bit quasi-bidirectional I/O port.[1] P20-P23 contain the 4 higher order address bits during an access of external program memory and also serve as a 4-bit I/O expander bus for the 8243.
PROG	25	I/O	**Output strobe** (active low) for the 8243 I/O expander.
T0	1	I/O	**Input pin** sensed using the JT0 and JNT0 instructions. **Clock output pin** when designated as such by the ENT0 CLK instruction.
T1	39	I	**Input pin** sensed using the JT1 and JNT1 instructions. Can be designated as the timer/counter input by the STRT CNT instruction.
$\overline{INT}$	6	I	**Interrupt input pin.** When low causes interrupt if interrupt is enabled. Can also be used as an input which is testable with the JNI instruction. Interrupt is disabled during and after a $\overline{RESET}$.
$\overline{RESET}$	4	I	**Reset input pin** is that used to initialize the microcomputer. Active low. Internal pullup ~75kΩ[2]. During program verification the address is latched by a "0" to "1" transition on $\overline{RESET}$ and the data at the addressed location is output on BUS.
ALE	11	O	**Address latch enable.** Occurs each clock cycle and is useful for clocking and sampling. During external program or data memory access, ALE is used to strobe the address information multiplexed on the DB0-DB7 outputs.
$\overline{RD}$	8	O	**Read strobe.** Active low strobe used to gate data onto BUS lines when reading from an external source.
$\overline{WR}$	10	O	**Write strobe.** Active low strobe used to write data from BUS lines to an external destination.
EA	7	I	**External access input.** When high forces instruction fetches from external memory. Internal pullup ~10MΩ.
$\overline{PSEN}$	9	O	**Program store enable.** Active low strobe that occurs only during a fetch from external program memory.
$\overline{SS}$	5	I	**Single step.** Active low input which is used with ALE to cause the microcomputer to execute a single instruction. Internal pullup ~300kΩ.
XTAL1	2	I	**One side of crystal** (or L) input for internal oscillator. Can also be used as an input for an external timing source[2].
XTAL2	3	I	**Other side of crystal.**
V_{SS}	20	I	**Circuit ground.**
V_{CC}	40	I	**Power input,** +5VDC.
V_{DD}	26	I	**RAM power input;** low power standby pin.

NOTES
1 Each pin on these ports can be assigned, under program control, to be an input or an output A pin is designated as an input by writing a logic "1" to the pin $\overline{RESET}$ sets all pins to the input mode Each pin has an internal pullup of approximately 50kΩ
2 Non-standard TTL V_{IH}

BLOCK DIAGRAM



DATA MEMORY

Resident data memory, as shown in figure 2, consists of up to 256 bytes of RAM. All locations are indirectly addressable by either of two RAM pointer registers at locations 0 and 1. The first eight locations of RAM (0-7) are designated as working registers and are directly addressable by several instructions.

By selecting register bank 1, RAM locations 24-31 become the working registers, replacing those in register bank 0 (0-7). RAM locations 8-23 are designated as the stack. Two locations (bytes) are used per CALL, allowing nesting of up to eight subroutines.

If additional RAM is required, up to 256 bytes may be added and addressed directly using the MOVX instructions. If more RAM is required an I/O port can be used to select one (256-byte) bank of external memory at a time.

PROGRAM COUNTER AND STACK

The Program Counter (PC) is a 12-bit counter/register that points to the location from which the next instruction is to be fetched. The 8048 and 8049 will automatically address exernal memory when the boundary of their internal memory is exceeded. All processors access external memory if EA is high.

An interrupt or CALL to a subroutine causes the contents of the program counter to be stored in one of the 8 register pairs of the program counter stack. The pair to be used is determined by a 3-bit stack pointer which is part of the Program Status Word (PSW). Data RAM locations 8 through 23 are available as stack registers and are used to store the program counter and 4 bits of PSW. The stack pointer, when initialized to 000, points to RAM locations 8 and 9. The first subroutine jump or interrupt results in the program counter contents being transferred to locations 8 and 9 of the RAM array. The stack pointer is then incremented by one to point to locations 10 and 11 in anticipation of another CALL. Nesting of subroutines within subroutines can continue up to eight times without overflowing the stack. If overflow does occur the deepest address stored (location 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111.

The end of a subroutine, which is signalled by a return instruction (RET or RETR), causes the stack pointer to be decremented and the contents of the resulting register pair to be transferred to the program counter.

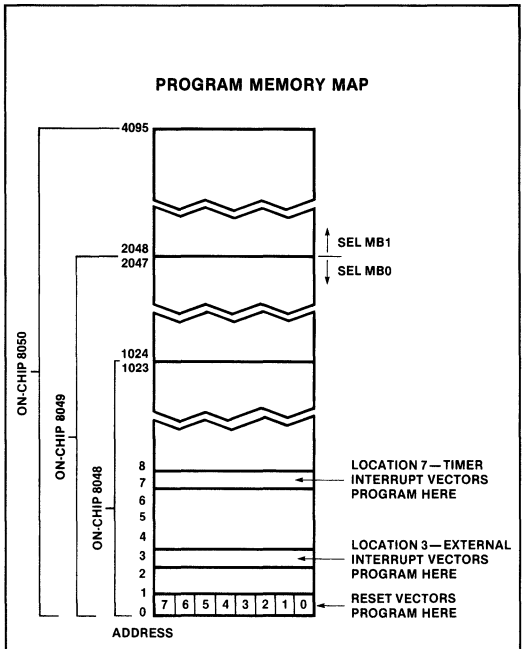


Figure 1

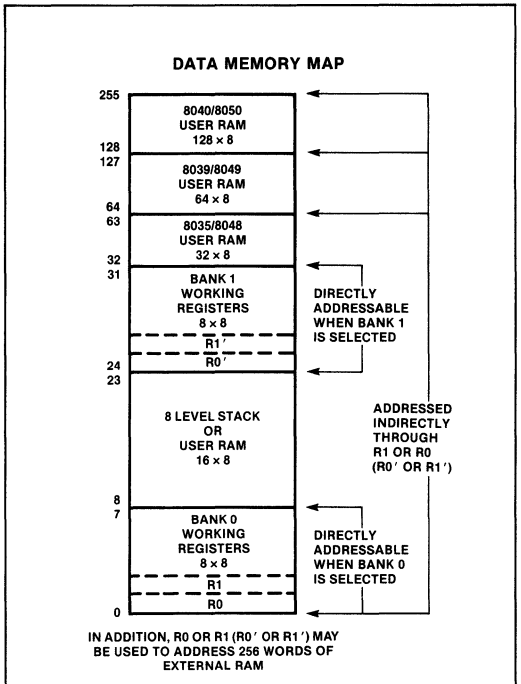


Figure 2

SINGLE CHIP 8-BIT MICROCOMPUTERS SC84 SERIES

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

DESCRIPTION

The Signetics SC84 Series microcomputers are self-contained 8-bit processors which contain the system timing, control logic, RAM data memory, ROM program memory, and serial and parallel I/O lines necessary to implement dedicated control functions. All SC84 Series devices are pin and program compatible, differing only in the size of the on-board program ROM and data RAM, as follows:

TYPE	RAM SIZE	ROM SIZE
8400	128 x 8	—
8405	32 x 8	512 x 8
8410	64 x 8	1K x 8
8420	64 x 8	1K x 8
8440	128 x 8	4K x 8

The 8400 is a ROM-less piggyback version which can be used with standard EPROMs for emulating any of the other devices of the family.

The SC84 Series processors are designed to be efficient control processors as well as arithmetic processors. They provide an instruction set which allows the user to directly set and reset individual lines within its I/O ports as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions make these processors very efficient in implementing standard logic functions. Also, special attention has been given to code efficiency. Over 70% of the instructions are a single byte long and all others are only 2 bytes long. The instruction set is based on that of the SC80 Series.

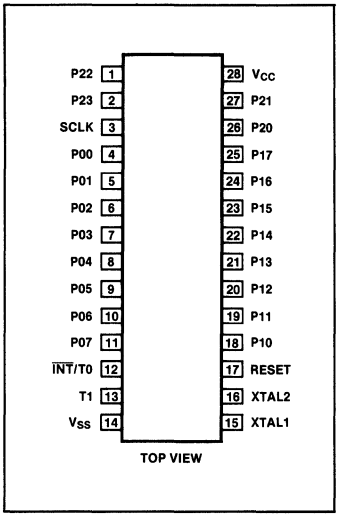
A special feature of the SC84 Series is the serial I/O interface. This eliminates the heavy processing load imposed upon a normal microcomputer performing serial data transfer, and facilitates the design of multi-microcomputer systems using serial communications.

An on-chip 8-bit counter is provided which can count, under program control, either internal clock pulses (with an optional divide by 32 prescaler) or external events. The counter can be programmed to cause an interrupt on terminal count.

FEATURES

- **8-bit CPU, ROM, RAM, I/O in a 28-pin package**
- **20 quasi bidirectional I/O lines**
- **Two test inputs, one with zero voltage crossover detection**
- **Serial I/O hardware**
- **Internal counter/timer**
- **Single-level vectored interrupts: external, counter/timer, serial I/O**
- **Over 90 instructions, 70% single byte**
- **6.77μs instruction cycle, all instructions one or two cycles**
- **High current drive on four outputs**
- **TTL compatible inputs and outputs**
- **Single +5V power supply**

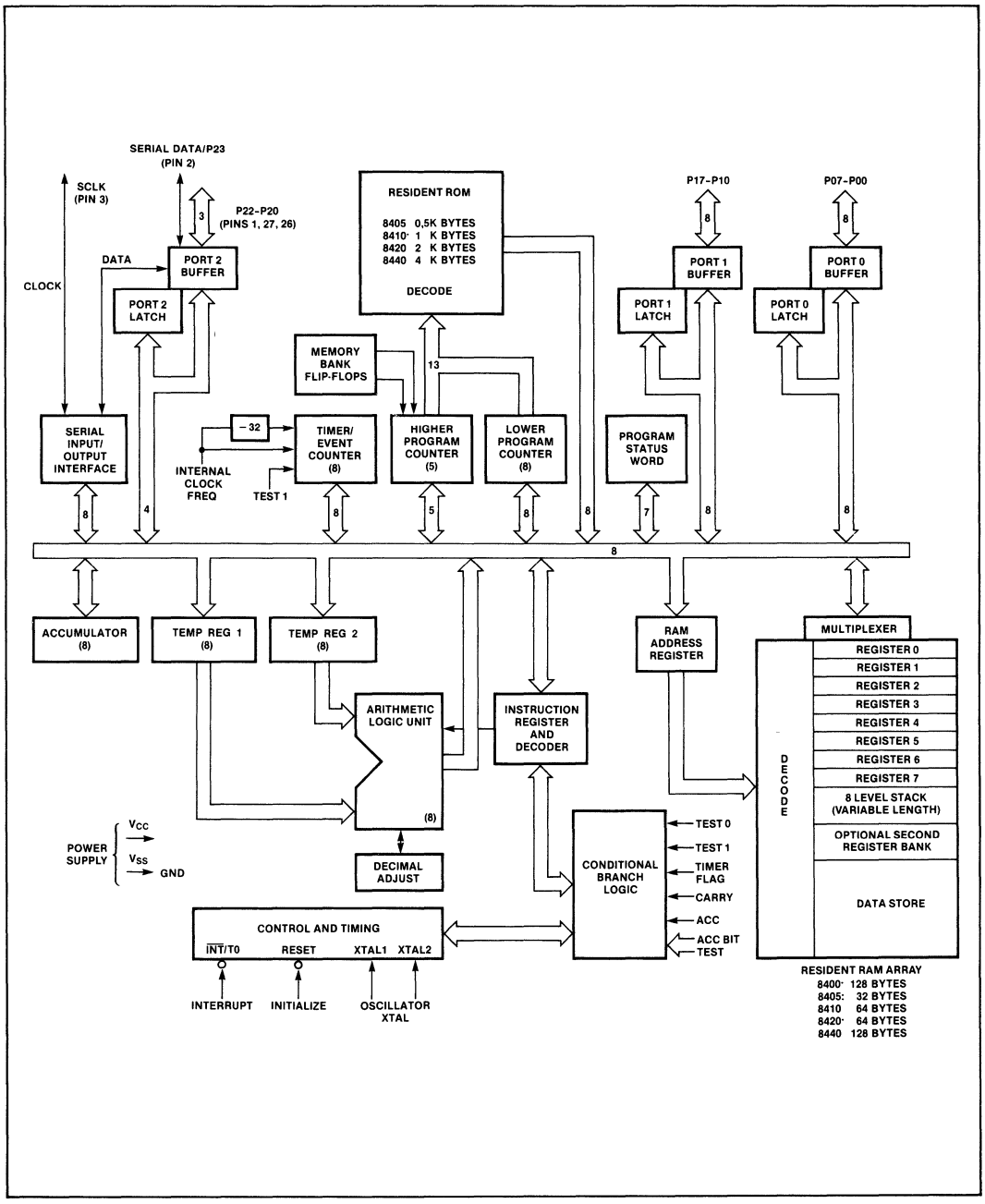
PIN CONFIGURATION



PIN DESIGNATION

MNEMONIC	PIN	FUNCTION
P00-P07	4-11	8-bit quasi bidirectional I/O port (Port 0)
P10-P17	18-25	8-bit quasi bidirectional I/O port (Port 1)
P20-P23	26,27,1,2	4-bit quasi bidirectional I/O port (Port 2); P23 is the serial data input/output in serial I/O mode
SCLK	3	Bidirectional clock for serial I/O
$\overline{INT}$/T0	12	External interrupt input (active low); testable using the JT0, JNT0 instructions.
T1	13	Input pin testable using the JT1, JNT1 instructions. Can be designated the event counter input, using the STRT CNT instruction. Also allows zero crossover sensing of slowly moving AC inputs.
RESET	17	Input. Used to initialize the processor (active high).
XTAL1	15	Connection to timing component (usually a crystal) which determines the frequency of the internal oscillator. Also the input for an external clock source.
XTAL2	16	Connection to other side of timing component.
V_{SS}	14	Ground
V_{CC}	28	+5V power supply

BLOCK DIAGRAM



Serial I/O

The 8400 serial I/O interface has been designed to eliminate the heavy processing load imposed upon a normal microcomputer performing serial data transfer. Whereas a normal microcomputer must regularly monitor the serial dat bus for the presence of data, the 8400 serial I/O interface detects, receives and converts the serial data stream into parallel format without interrupting the execution of the current program. An interrupt is sent to the microcomputer only when a complete byte is received. Then, the microcomputer reads the data byte in one instruction. Likewise, for transmission, the serial I/O interface performs parallel-to-serial conversion and subsequent serial output of the data and the microcomputer is only interrupted in the execution of its programmed tasks when a complete byte has been transmitted.

The design of the 8400 serial I/O system allows any number of 8400 devices to be interconnected by the two-line serial bus. The ability of any two devices to communicate, without interrupting the operation of any other devices on the bus, is an outstanding attribute of the system. This is achieved by allocating a specific 7-bit address to each device and providing a system whereby a device reacts only to messages prefixed with its own address or the 'general call' address. Address recognition is performed by the interface hardware so that operation of the microcomputer need only be interrupted when a valid address has been received. This saves significant processing time and memory space compared with a conventional microcomputer employing a software serial interface. When the addressing facility is not required, for instance in a system with only two microcomputers, direct data transfer without addressing can be performed.

In multimaster systems, an automatically invoked arbitration procedure prevents two or more devices from continuing simultaneous transmission.

Serial I/O Interface

Figure 1 shows the serial I/O interface. The clock line of the serial bus has exclusive use of pin 3 (SCLK), while the data line shares pin 2 (serial data) with the I/O line P23 of Port 2. When the serial I/O is enabled, P23 is disabled as a parallel port line.

The microcomputer and interface communicate via the internal microcomputer bus and the serial interrupt request line. Data and information controlling the operation of the interface are stored in four registers:

- Data shift register S0
- Serial I/O interface status word S1
- Serial clock control word S2
- Address register.

I/O LOGIC DIAGRAM

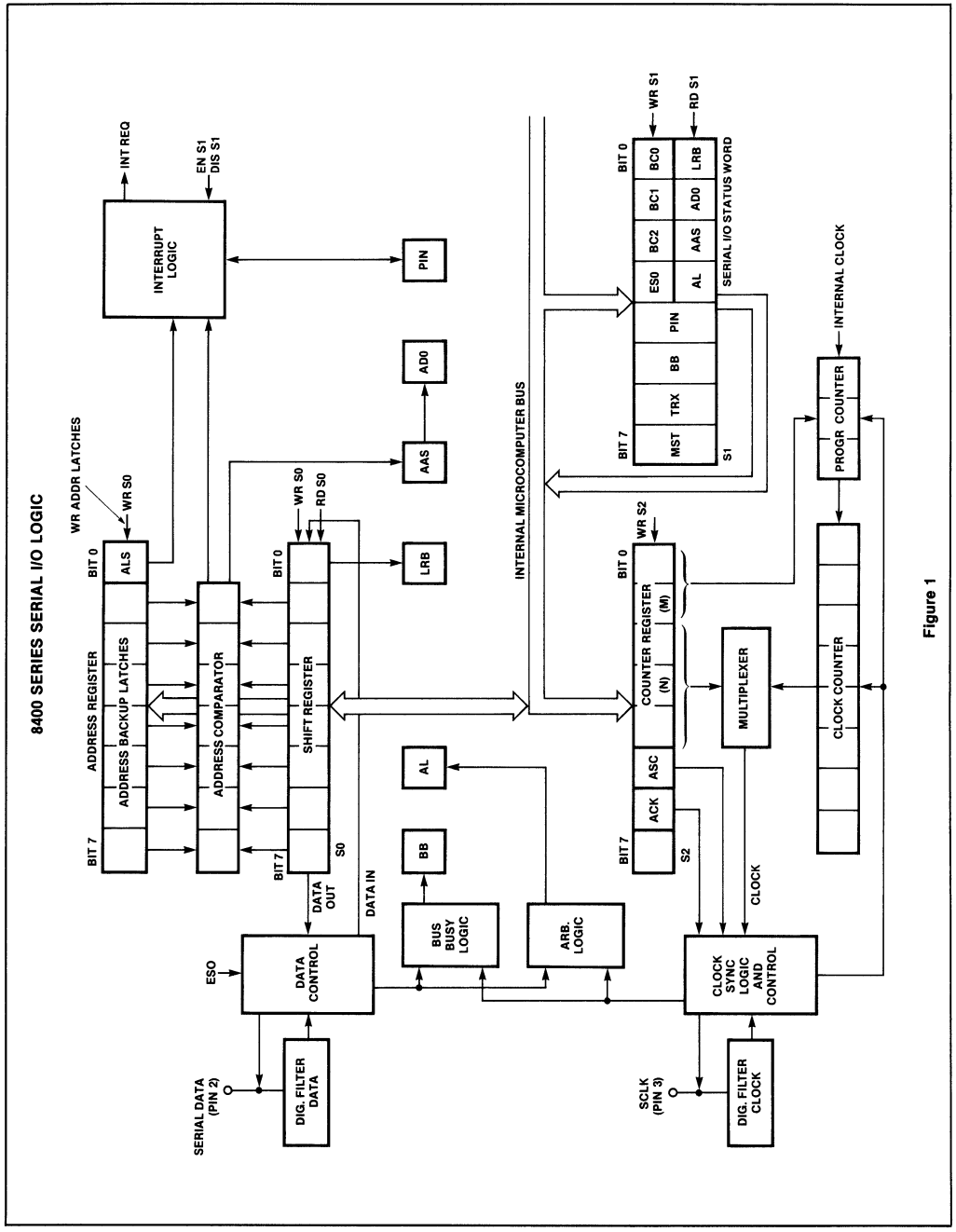


Figure 1

Section 4
SC68000 16-Bit Family

16-BIT MICROPROCESSOR SC68000

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

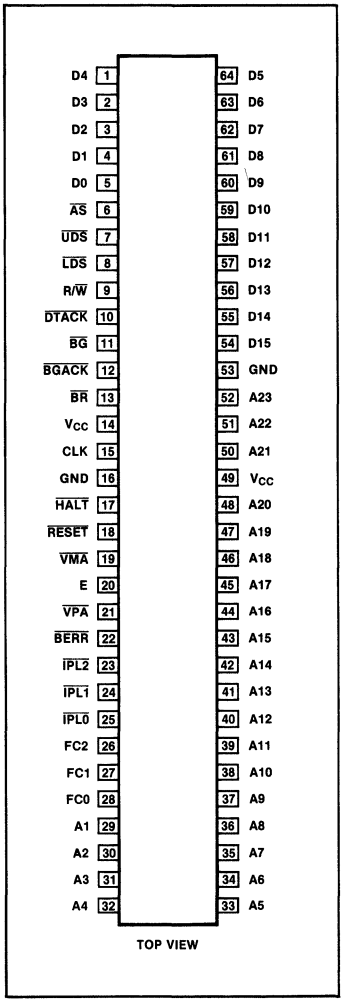
DESCRIPTION

Advances in semiconductor technology have provided the capability to place on a single chip a microprocessor at least an order of magnitude higher in performance and circuit complexity than has been previously available. The SC68000 is the first of a family of such VLSI microprocessors from Signetics. It combines state-of-the-art technology and advanced circuit design techniques with computer sciences to achieve an architecturally advanced 16-bit microprocessing unit. The SC68000 offers seventeen 32-bit registers in addition to the 32-bit program counter and a 16-bit status register (see the programming model in figure 1). The first eight registers (D0–D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) data operations. The second set of seven registers (A0–A6) and the system stack pointer can be used as software stack pointers and base address registers. In addition, these registers can be used for word and long word address operations. All 17 registers can be used as index registers.

FEATURES

- **32-bit data and address registers**
- **16-megabyte direct addressing range**
- **56 powerful instruction types**
- **Operations on five main data types**
- **Memory mapped I/O**
- **14 addressing modes**

PIN CONFIGURATION



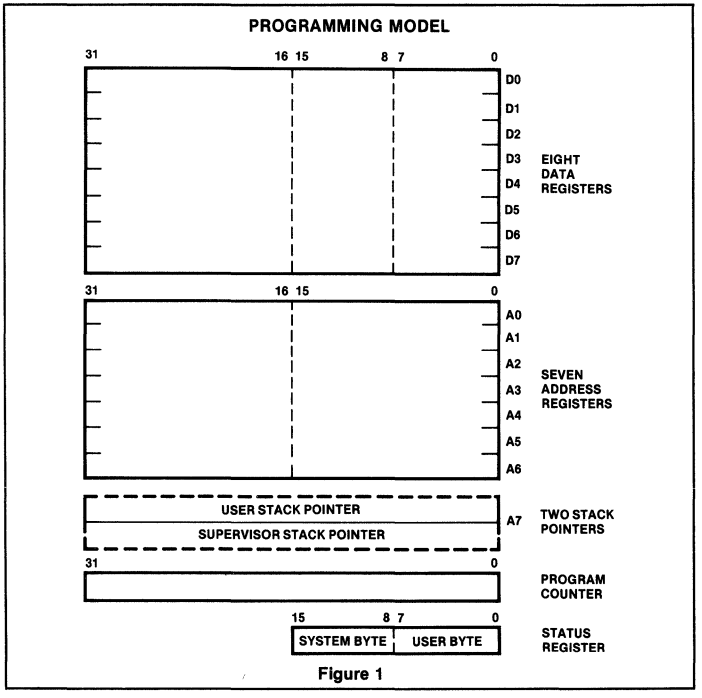


Figure 1

A 23-bit address bus provides a memory addressing range of greater than 16 megabytes. This large range of addressing capability, coupled with a memory management unit, allows large, modular programs to be developed and operated without resorting to cumbersome and time consuming software bookkeeping and paging techniques.

Five basic data types are supported:

- Bits
- BCD digits (4 bits)
- Bytes (8 bits)
- Word (16 bits)
- Long words (32 bits)

In addition, operations on other data types, such as memory addresses, status word data, etc., are provided for in the instruction set. The 14 addressing modes (see table 1) include six basic types:

- Register direct
- Register indirect
- Absolute
- Immediate
- Program counter relative
- Implied

Included in the register indirect addressing modes is the capability to do postincrementing, predecrementing, offsetting, and indexing. Program counter relative mode can also be modified via indexing and offsetting.

Table 1. DATA ADDRESSING MODES

MODE	GENERATION
Register Direct Addressing	
Data Register Direct	EA = Dn
Address Register Direct	EA = An
Absolute Data Addressing	
Absolute Short	EA = (Next Word)
Absolute Long	EA = (Next Two Words)
Program Counter Relative Addressing	
Relative with Offset	EA = (PC) + d_{16}
Relative with Index and Offset	EA = (PC) + (Xn) + d_8
Register Indirect Addressing	
Register Indirect	EA = (An)
Postincrement Register Indirect	EA = (An), An ← An + N
Predecrement Register Indirect	An ← An − N, EA = (An)
Register Indirect with Offset	EA = (An) + d_{16}
Indexed Register Indirect with Offset	EA = (An) + (Xn) + d_8
Immediate Data Addressing	
Immediate	DATA = Next Word(s)
Quick Immediate	Inherent Data
Implied Addressing	
Implied Register	EA = SR, USP, SP, PC

NOTES
EA = Effective Address
An = Address Register
Dn = Data Register
Xn = Address or Data Register used as Index Register
SR = Status Register
PC = Program Counter
( ) = Contents of
d_8 = 8-bit Offset (displacement)
d_{16} = 16-bit Offset (displacement)
N = 1 for Byte, 2 for Words and 4 for Long Words
← = Replaces

4

The SC68000 instruction set is shown in table 2. Some additional instructions are variations, or subsets, of these and appear in table 3. Special emphasis has been given to the instruction set's support of structured high-level languages to facilitate ease of programming. Each instruction, with a few exceptions, operates on bytes, words, and long words, and most instructions can use any of the 14 addressing modes. Combining instruction types, data types, and addressing modes, over 1000 useful instructions are provided. These instructions include signed and unsigned multiply and divide, 'quick' arithmetic operations, BCD arithmetic and expanded operations (through traps).

Table 2. INSTRUCTION SET

MNEMONIC	DESCRIPTION
ABCD	Add Decimal with Extend
ADD	Add
AND	Logical AND
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
B_{CC}	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register against Bounds
CLR	Clear Operand
CMP	Compare
DB_{CC}	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive OR
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MOVEM	Move Multiple Registers
MOVEP	Move Peripheral Data
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	One's Complement
OR	Logical OR
PEA	Push Effective Address
RESET	Reset External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
S_{CC}	Set Conditional
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

Table 3. VARIATIONS OF INSTRUCTION TYPES

INSTRUCTION TYPE	VARIATION	DESCRIPTION
ADD	ADD	Add
	ADDA	Add Address
	ADDQ	Add Quick
	ADDI	Add Immediate
	ADDX	Add with Extend
AND	AND	Logical AND
	ANDI	AND Immediate
CMP	CMP	Compare
	CMPA	Compare Address
	CMPM	Compare Memory
	CMPI	Compare Immediate
EOR	EOR	Exclusive OR
	EORI	Exclusive OR Immediate
MOVE	MOVE	Move
	MOVEA	Move Address
	MOVEQ	Move Quick
	MOVE from SR	Move from Status Register
	MOVE to SR	Move to Status Register
	MOVE to CCR	Move to Condition Codes
	MOVE USP	Move User Stack Pointer
NEG	NEG	Negate
	NEGX	Negate with Extend
OR	OR	Logical OR
	ORI	OR Immediate
SUB	SUB	Subtract
	SUBA	Subtract Address
	SUBI	Subtract Immediate
	SUBQ	Subtract Quick
	SUBX	Subtract with Extend

INTELLIGENT PERIPHERAL CONTROLLER SC68120

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

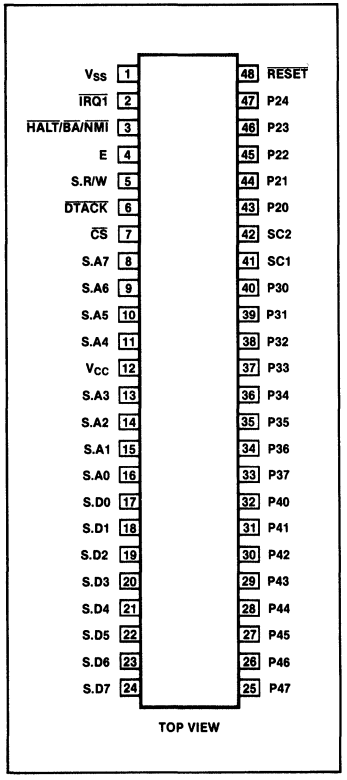
DESCRIPTION

The SC68120 Intelligent Peripheral Controller (IPC) is a general-purpose, user-programmable peripheral controller. It contains a system interface, an 8-bit CPU, a serial communications interface, 21 parallel I/O lines, a 16-bit timer, 2048 bytes of ROM, and eight operating modes. In addition, the SC68120 features 128 bytes of dual-ported RAM and six semaphore registers that are accessible to both the internal CPU and an external processor or device through the system interface. The SC68120 provides all the control signals necessary to interface with the asynchronous bus of the SC68000.

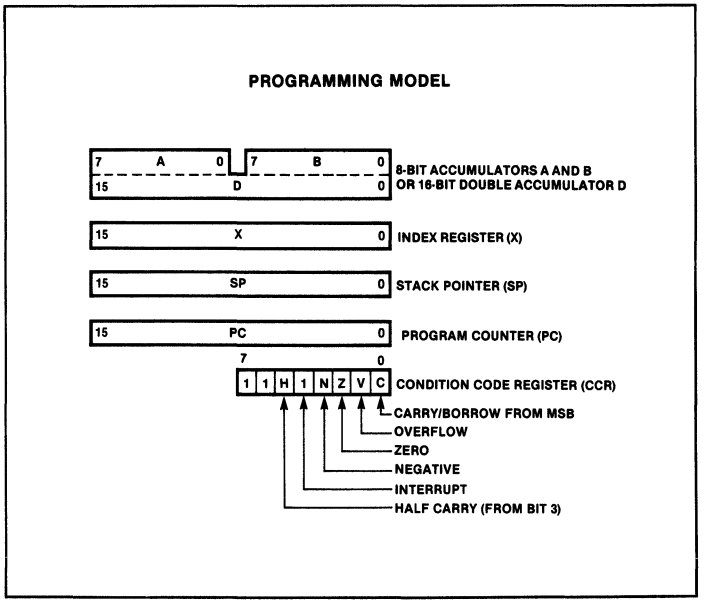
FEATURES

- **Bus compatible with the 16-bit SC68000 and with 8-bit microprocessors**
- **Bus compatible with 8-bit peripherals**
- **TTL compatible I/O**
- **8-bit CPU**
- **2K bytes ROM**
- **128 bytes dual-ported RAM**
- **Six shared semaphore registers**
- **16-bit timer**
- **21 parallel I/O and two handshake lines**
- **Serial communications interface**
- **Interrupt capability**
- **Operates in single-chip mode or expandable to 64K-byte addressing range**
- **DMA capability**
- **8 x 8-bit multiply**

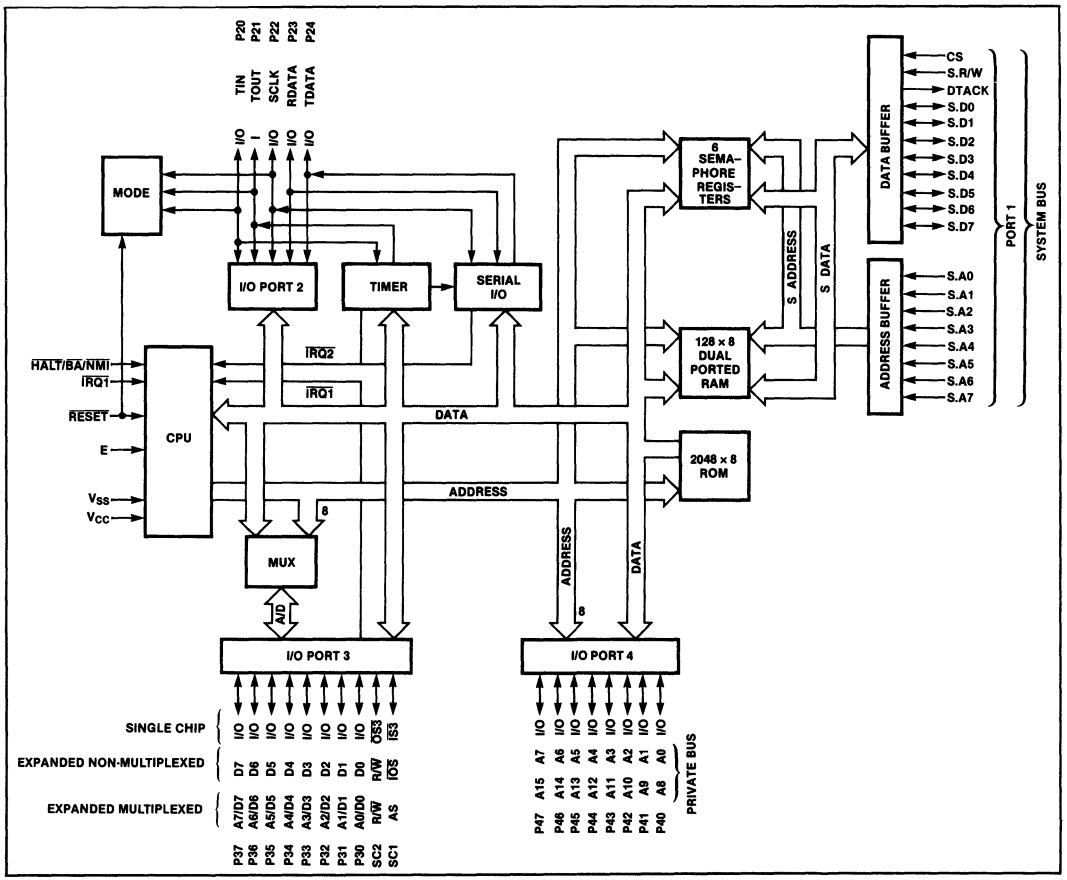
PIN CONFIGURATION



TOP VIEW



BLOCK DIAGRAM



SUMMARY OF OPERATING MODES

Common to all modes:

- System bus interface
- Reserved register area
- Six semaphore registers
- I/O port 2
- 16-bit programmable timer
- Serial communications interface
- 128 bytes of dual-ported RAM

Single chip mode — Mode 7
- 2048 bytes of ROM (internal)
- Port 3 is a parallel I/O port with two control lines
- Port 4 is a parallel I/O port
- SC1 is input strobe 3 (IS3)
- SC2 is output strobe 3 (OS3)

Expanded non-multiplexed mode — Mode 5
- 2048 bytes of ROM (internal)
- 256 bytes of external memory space
- Port 3 is an 8-bit data bus
- Port 4 is an address bus
- SC1 is input/output select (IOS)
- SC2 is read/write (R/W)

Expanded multiplexed modes — Modes 1, 2, 3, 6
- Four memory space options (64K address space);
  - (1) MDOS compatible
  - (2) No ROM
  - (3) External vector space
  - (4) ROM with partial address bus
- External memory space accessed through:
  - Port 3 as a multiplexed address/data bus
  - Port 4 as an address bus (high)
- SC1 is address strobe (AS) input
- SC2 is read/write (R/W)

Test modes — Modes 0, 4
- Expanded multiplexed test mode — may be used to test RAM and ROM
- Single chip and non-multiplexed test mode — may be used to test ports 3 and 4 as I/O ports

PARALLEL INTERFACE/TIMER SC68230

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

DESCRIPTION

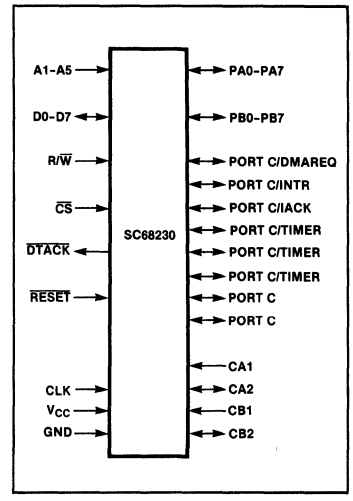
The SC68230 Parallel Interface/Timer (PI/T) is a general-purpose, programmable parallel interface device which meets most system parallel I/O and timing needs. The parallel interfaces of the PI/T may be used to connect a wide variety of peripheral devices to the SC68000 bus. The PI/T can be programmed to generate interrupt requests to the SC68000, or DMA requests to the SC68450 Direct Memory Access Controller, on demand of the peripheral. No external logic is needed to connect the PI/T to the DMAC or to the SC68000. The PI/T also provides complete port and timer status information.

The SC68230 contains two multi-mode, double-buffered I/O ports (Port A and Port B), a third 8-bit I/O port, and a 24-bit programmable timer. The PI/T also contains flexible prioritization logic for generating unique interrupt vectors. Autovectored interrupts are also supported. Port C pins provide either another port pin or special functions consisting of interrupt, timer, or direct memory access control lines.

FEATURES

- **24 programmable I/O lines**
- **Port modes include:**
  - **Bit mode**
  - **Unidirectional 8-bit mode**
  - **Unidirectional 16-bit mode**
  - **Bidirectional 8-bit mode**
  - **Bidirectional 16-bit mode**
- **Selectable handshaking modes**
- **24-bit programmable timer**
- **Several timer modes**
- **Contains interrupt prioritization logic**
- **Unique interrupt vectors for each source**
- **Supports interrupt and DMA service requests**
- **Contains port and timer status registers**
- **SC68000 bus compatible**

FUNCTIONAL DIAGRAM



DMA CONTROLLER SC68450

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

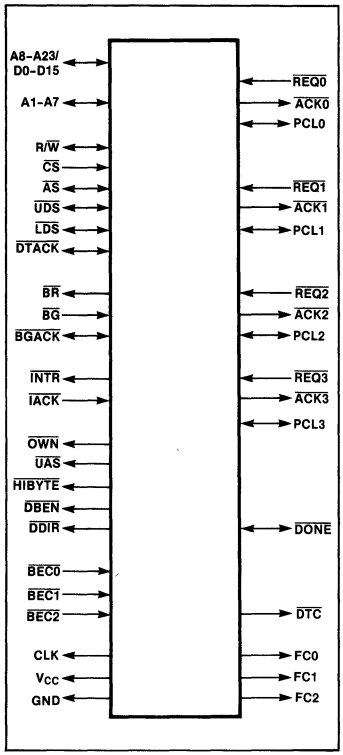
DESCRIPTION

The SC68450 Direct Memory Access Controller (DMAC) offers the system designer unparalleled performance where both speed and flexibility in data transfer are required. Sophisticated chaining techniques, memory-to-memory block transfers, and variable bus bandwidth utilization result in optimum data transfers. Internal 32-bit address registers provide upward software compatibility with future SC68000 family processors

FEATURES

- **Compatible with both SC68000 family and 8-bit peripherals**
- **Four fully-independent channels**
- **Single or dual address transfers**
- **Byte, word, or long word transfers**
- **Memory-to-memory block transfers**
- **Supports both chained and unchained operations**
- **Transfer rates up to 4 megabytes per second**
- **Supports vectored interrupts**
- **Supports array or linked array chaining**
- **16-bit data bus**
- **Programmable priorities**

FUNCTIONAL DIAGRAM



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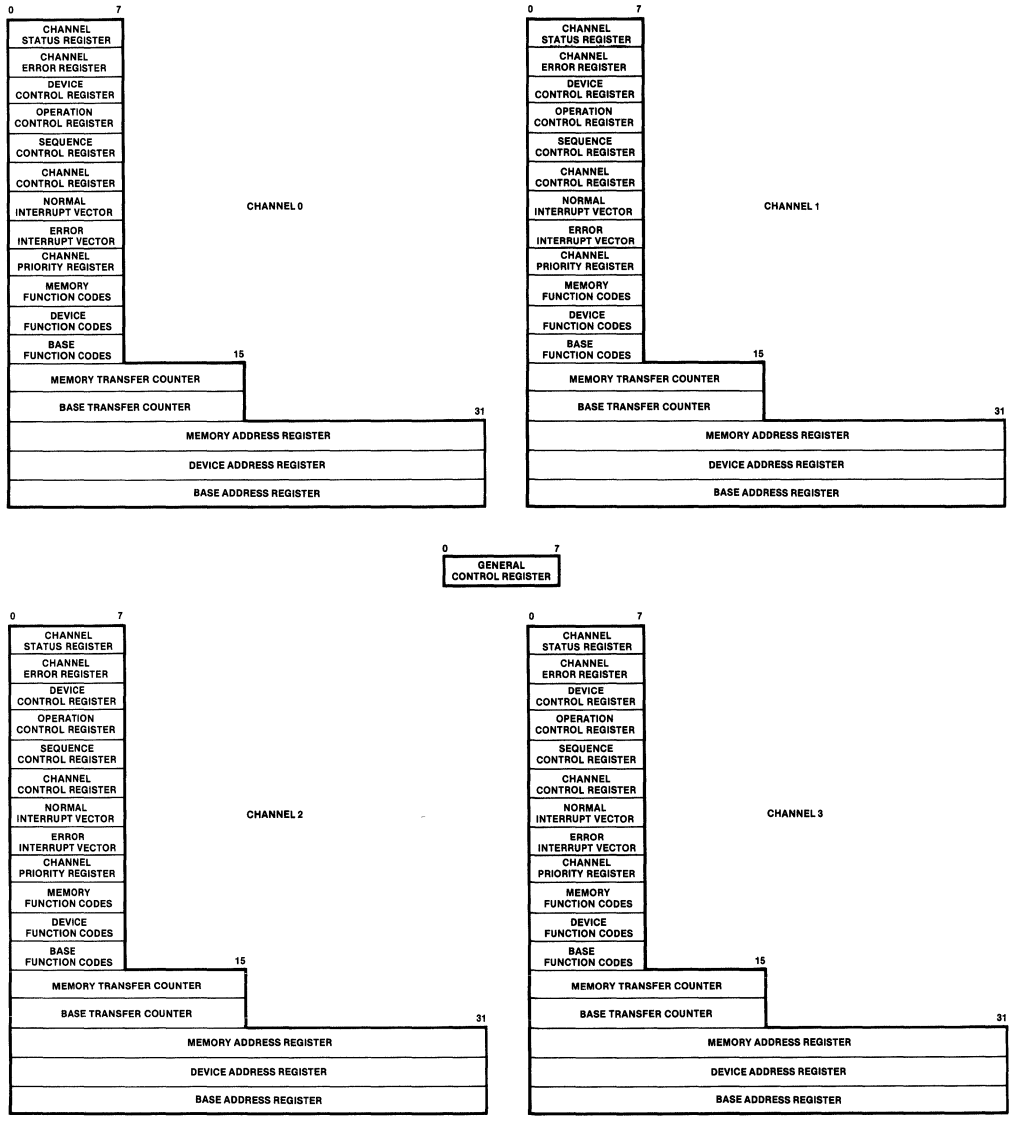
INTERNAL ORGANIZATION



MEMORY MANAGEMENT UNIT SC68451

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

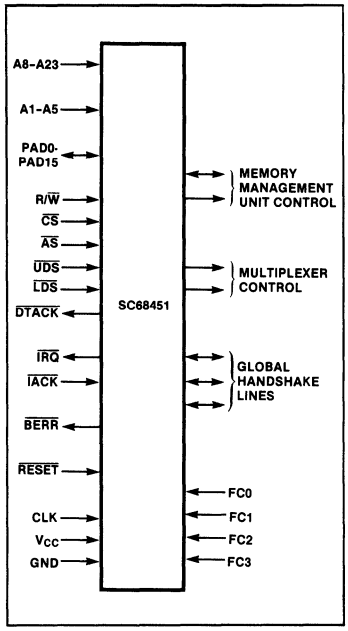
DESCRIPTION

The SC68451 Memory Management Unit (MMU) provides address translation and protection of the 16-megabyte addressing space of the SC68000. The MMU can be accessed by any potential bus master, such as instruction set processors, or DMA controllers. Each bus master (or processor) in the SC68000 family provides a function code and an address during each bus cycle. The function code specifies an address space while the address specifies a location within that address space. The function codes are provided by the SC68000 to distinguish between program and data spaces as well as supervisor and user spaces. This separation of address spaces provides the basis of protection in an operating system. By simplifying the programming model of the address space, the MMU also increases the reliability of a complex multiprocess system.

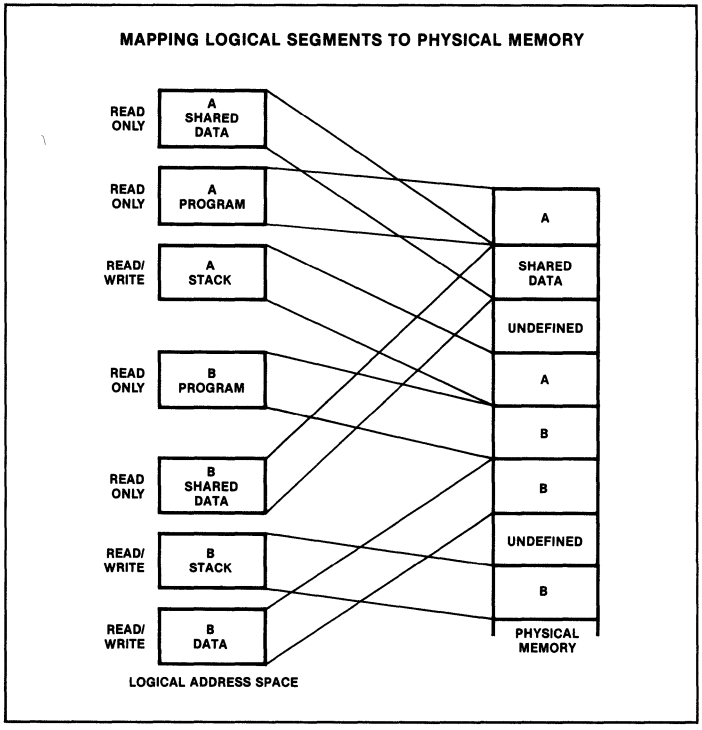
FEATURES

- **Separates address spaces of system and user resources**
- **Provides write protection**
- **Increases system reliability**
- **Provides efficient memory allocation**
- **Allows interprocess communication through shared resources**
- **Simplifies programming model of address space**
- **Minimizes operating system overhead with quick context switches**
- **32 segments with variable segment sizes**
- **Multiple MMU system capability**
- **Supports both paging and segmentation**
- **DMA compatible**
- **Provides virtual memory support**
- **SC68000 bus compatible**

FUNCTIONAL DIAGRAM



MAPPING LOGICAL SEGMENTS TO PHYSICAL MEMORY



DUAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART) SC68681

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

DESCRIPTION

The Signetics SC68681 Dual Universal Asynchronous Receiver/Transmitter (DUART) is a single chip MOS-LSI communications device that provides two independent, full-duplex, asynchronous receiver/transmitter channels in a 40-pin package. It interfaces directly with the SC68000 16-bit CPU and other microprocessors and may be used in a polled or interrupt driven system.

The operating mode and data format of each channel can be programmed independently. Additionally, each receiver and transmitter can select its operating speed as one of 18 fixed baud rates, a 16× clock derived from a programmable counter/timer, or an external 1× or 16× clock. The baud rate generator and counter/timer can operate directly from a crystal or from external clock inputs. The ability to independently program the operating speed of the receiver and transmitter make the DUART particularly attractive for dual-speed channel applications such as clustered terminal systems.

Each receiver is quadruply buffered to minimize the potential of receiver overrun or to reduce interrupt overhead in interrupt driven systems. In addition, a handshaking capability is provided to disable a remote DUART transmitter when the buffer of the receiving device is full.

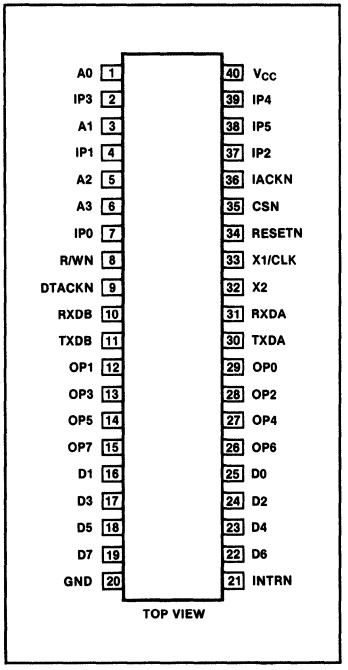
Also provided on the SC68681 are a multipurpose 6-bit input port and a multipurpose 8-bit output port. These can be used as general-purpose I/O ports or can be assigned specific functions (such as clock inputs or status/interrupt outputs) under program control.

The SC68681 is similar to the Signetics SC2681, differing primarily in that the SC68681 bus interface is compatible with the SC68000 16-bit microprocessor. Refer to the SC2681 data sheet for operational details.

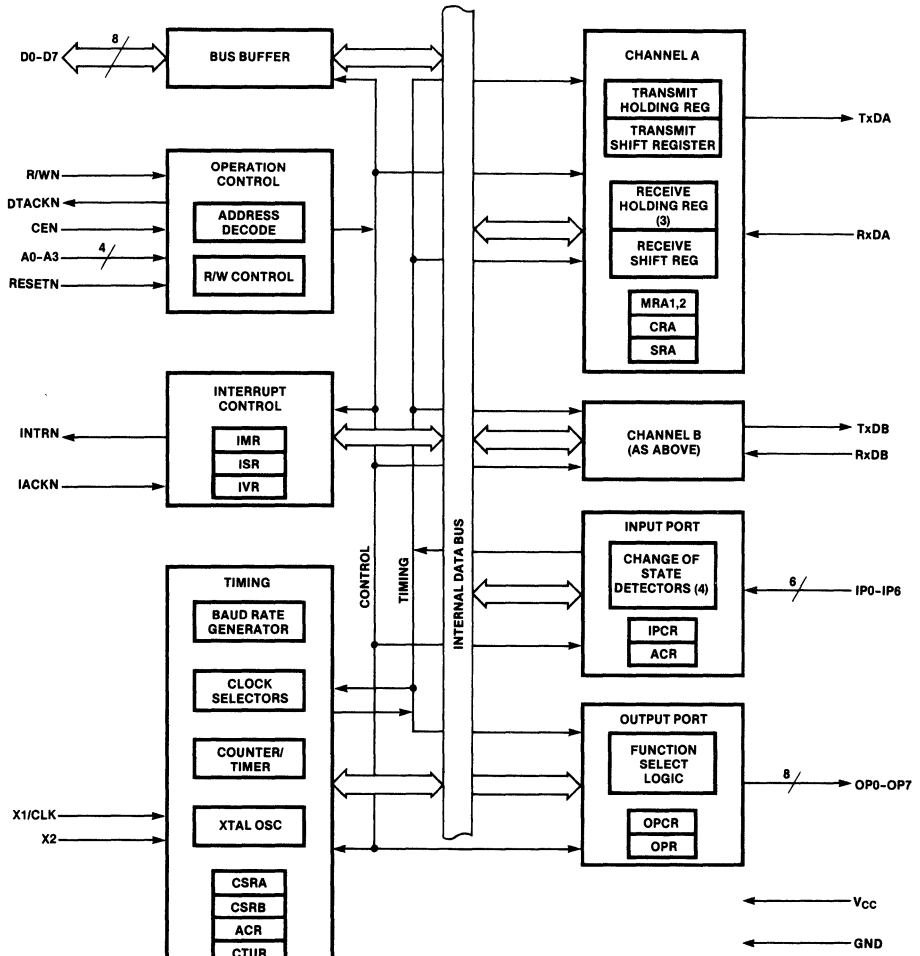
FEATURES

- **SC68000 compatible bus interface**
- **Dual, full-duplex, asynchronous receiver/transmitter**
- **Quadruple buffered receiver data registers**
- **Programmable data format**
  - **— 5 to 8 data bits plus parity**
  - **— Odd, even, no parity or force parity**
  - **— 1, 1.5 or 2 stop bits programmable in 1/16-bit increments**
- **Programmable baud rate for each receiver and transmitter selectable from**
  - **— 18 fixed rates: 50 to 38.4K baud**
  - **— One user-defined rate derived from programmable timer/counter**
  - **— External 1X or 16X clock**
- **Parity, framing, and overrun error detection**
- **False start bit detection**
- **Line brake detection and generation**
- **Programmable channel mode**
  - **— Normal (full duplex)**
  - **— Automatic echo**
  - **— Local loopback**
  - **— Remote loopback**
- **Multi-function programmable 16-bit counter/timer**
- **Multi-function 6-bit input port**
  - **— Can serve as clock or control inputs**
  - **— Change of state detection on four inputs**
- **Multi-function 8-bit output port**
  - **— Individual bit set/reset capability**
  - **— Outputs can be programmed to be status/interrupt signals**
- **Versatile interrupt system**
  - **— Single interrupt output with eight maskable interrupting conditions**
  - **— Interrupt vector output on interrupt acknowledge**
  - **— Output port can be configured to provide a total of up to six separate wire-OR'able interrupt outputs**
- **Maximum data transfer: 1X — 1MB/sec, 16X — 125KB/sec**
- **Automatic wake-up mode for multidrop applications**
- **Start-end break interrupt/status**
- **Detects break which originates in the middle of a character**
- **On-chip crystal oscillator**
- **TTL compatible**
- **Single +5V power supply**

PIN CONFIGURATION



BLOCK DIAGRAM



BLOCK DIAGRAM

The SC68681 DUART consists of the following eight major sections: data bus buffer, operation control, interrupt control, timing, communications channels A and B, input port and output port. Refer to the block diagram.

Data Bus Buffer

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the DUART.

Operation Control

The operation control logic receives operation commands from the CPU and generates appropriate signals to internal sections to control device operation. It contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer.

Interrupt Control

A single active-low interrupt output (INTRN) is provided which is activated upon the occurrence of any of eight internal events. Upon receiving an interrupt acknowledge from the CPU, the SC68681 responds by placing a programmable 8-bit interrupt vector on the data bus.

Associated with the interrupt system are the interrupt mask register (IMR) and the interrupt status register (ISR). The IMR may be programmed to select only certain conditions to cause INTRN to be asserted. The ISR can be read by the CPU to determine all currently active interrupting conditions.

Outputs OP3-OP7 can be programmed to provide discrete interrupt outputs for the transmitters, receivers, and counter/timer.

Timing Circuits

The timing block consists of a crystal oscillator, a baud rate generator, a programmable 16-bit counter/timer, and four clock selectors. The crystal oscillator operates directly from a 3.6864MHz crystal connected across the X1/CLK and X2 inputs. If an external clock of the appropriate frequency is available, it may be connected to X1/CLK. The clock serves as the basic timing reference for the baud rate generator (BRG), the timer/counter, and other internal circuits. A clock signal must always be supplied to the DUART.

The baud rate generator operates from the oscillator or external clock input and is capable of generating 18 commonly used data communications baud rates ranging from 50 to 38.4K baud. The clock outputs from the BRG are at 16X, the actual baud rate. The counter/timer can be used as a timer to produce a 16X clock for any other baud rate by counting down the crystal clock or an external clock. The four clock selectors allow the independent selection, for each receiver and transmitter, of any of these baud rates or an external timing signal.

The counter/timer (C/T) can be programmed to use one of several timing sources as its input. The output of the C/T is available to the clock selectors and can also be programmed to be output at OP3. In the counter mode, the contents of the C/T can be read by the CPU and it can be stopped and started under program control. In the timer mode, the C/T acts as a programmable divider.

Communications Channels A and B

Each communications channel of the SC68681 comprises a full-duplex, asynchronous receiver/transmitter (UART). The operating frequency for each receiver and transmitter can be selected independently from the baud rate generator, the counter timer, or from an external input.

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits and outputs a composite serial stream of data on the TxD output pin. The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for start bit, stop bit, parity bit (if any), or break condition and sends an assembled character to the CPU.

Input Port

The inputs to this unlatched port can be read by the CPU by performing a read operation at address D_{16}. A high input results in a logic 1 while a low input results in a logic 0. The pins of this port can also serve as auxiliary inputs to certain portions of the DUART logic.

Four change-of-state detectors are provided which are associated with inputs IP3, IP2, IP1, and IP0. A high-to-low or low-to-high transition of these inputs lasting longer than 25-50μs will set the corresponding bit in the input port change register. The bits are cleared when the register is read by the CPU. Any change of state can also be programmed to generate an interrupt to the CPU.

Output Port

The 8-bit multi-purpose output port can be used as a general-purpose output port, in which case the outputs are the complements of the output port register (OPR). OPR[n] = 1 results in OPn = low and vice-versa. Bits of the OPR can be individually set and reset. A bit is set by performing a write operation at address E_{16} with the accompanying data specifying the bits to be set (1 = set, 0 = no change). Likewise, a bit is reset by a write at address F_{16} with the accompanying data specifying the bits to be reset (1 = reset, 0 = no change).

Outputs can also be individually assigned specific functions by appropriate programming of the channel A mode registers (MR1A, MR2A), the channel B mode registers (MR1B, MR2B), and the output port configuration register (OPCR).

Section 5
Video Game

UNIVERSAL SYNC GENERATORS (USG) SC2621(PAL), SC2622(NTSC)

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

DESCRIPTION

The Signetics 2621 Universal Sync Generator (USG) provides the timing and control signals necessary for generating and displaying TV video information in the PAL format.

The USG accepts a single 3.55MHz input clock and generates various timing outputs including vertical, horizontal and composite blanking, composite sync and color burst flag. Several auxiliary clock outputs are also provided.

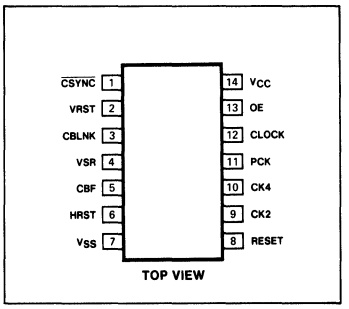
The USG is primarily intended for use in microprocessor-controlled video games. A typical game configuration consists of a 2621 USG, a 2650A microprocessor, a 2636 Programmable Video Interface, a 2616 16K ROM, and digital video summer circuitry.

The 2621 is constructed using Signetics silicon gate N-channel depletion load technology and operates from a single +5 volt power supply.

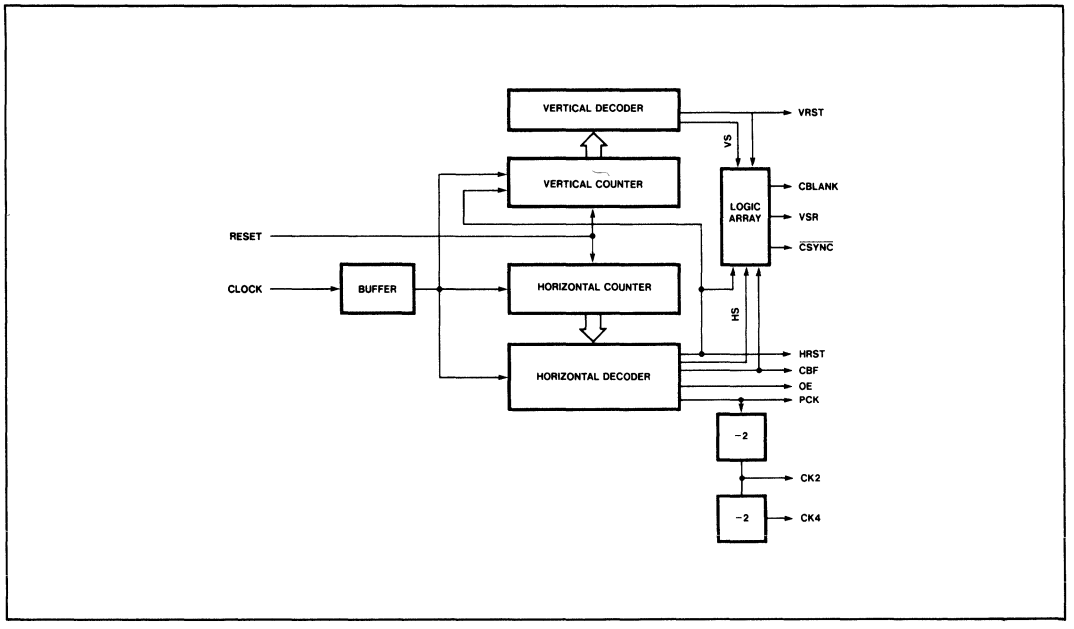
The Signetics 2622 Universal Sync Generator (USG) provides the timing and control signals necessary for generating and displaying TV video information in the NTSC format.

The USG accepts a single 3.5795MHz input clock and generates various timing outputs including vertical, horizontal, and composite blanking, composite sync and color burst flag. Several auxiliary clock outputs are also provided. The USG is primarily intended for use in microprocessor-controlled video games. A typical game configuration consists of a 2622 USG, a 2650A microprocessor, a 2636 Programmable Video Interface, a 2616 16K ROM, and video summer circuitry. The 2622 is constructed using Signetics silicon gate N-channel depletion load technology and operates from a single +5 volt power supply.

PIN CONFIGURATION



BLOCK DIAGRAM



PROGRAMMABLE VIDEO INTERFACE (PVI) SC2636

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

DESCRIPTION

The Signetics 2636 Programmable Video Interface (PVI) is intended for use in microprocessor-controlled game systems, and provides all of the common game circuits on a single chip. Circuits are provided for player inputs, background, moving objects, scoring, and audio signals.

A typical system configuration consists of five LSI circuits: a PVI, a 2616 16K ROM, an NE549 Digital Video Summer (DVS) a Universal Sync Generator (USG), and a 2650A microprocessor.

Additional PVIs as well as random logic can easily be interfaced to enhance game complexity. Since the system is microprocessor based, the actual game itself need not be "hardwired" into the system. Game definition is completely contained in the ROM. To change games, one simply replaces one ROM with another. Each ROM can contain several games, depending on game complexity and similarity between games.

The 2636 PVI is constructed using Signetics' silicon gate N-Channel depletion load technology and operates from a single +5 volt power supply.

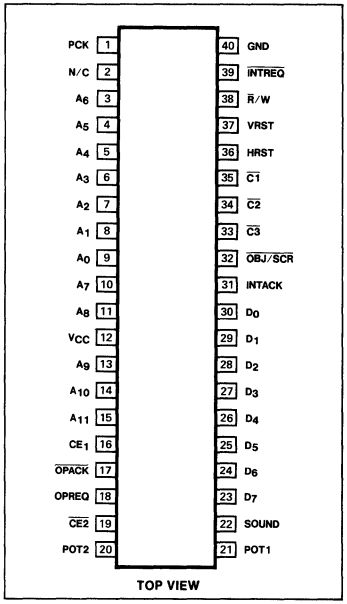
FEATURES

- **Four general-purpose, RAM-resident object modules**
- **Object duplication permitting generation of up to 80 object images on the screen**
- **280ns object resolution**
- **Object size and position under program control**
- **Programmable score**
- **Programmable sound**
- **Programmable background**
- **Eight programmable colors with multiple brightness levels**
- **37-byte scratch pad memory**
- **Chip Enable outputs for system ROMs and PROMs**
- **I/O facilities for switch scanning and potentiometer inputs**
- **Wire-OR expansion capability to multiple PVIs**
- **Forty-pin dual-in-line package**

APPLICATIONS

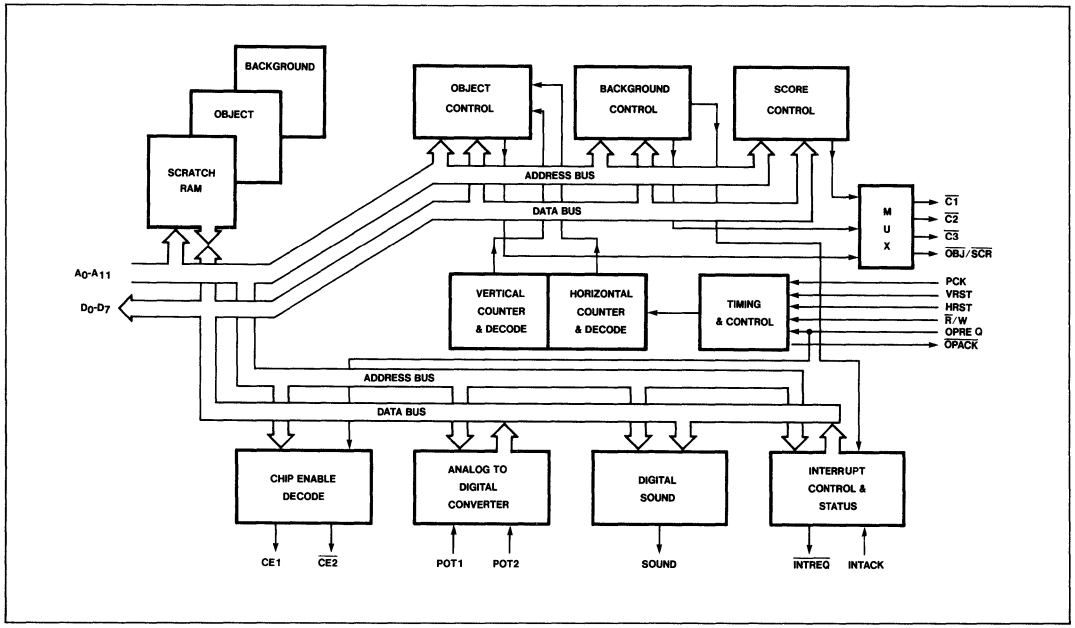
- **Consumer programmable video games**
- **Arcade games**
- **Simulators**
- **Special purpose graphic displays**
- **Home computer center**

PIN CONFIGURATION



TOP VIEW

PVI BLOCK DIAGRAM



UNIVERSAL VIDEO INTERFACE (UVI) SC2637

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

DESCRIPTION

The Signetics 2637 Universal Video Interface (UVI), using a new design approach, enables a microprocessor based system to be interfaced more efficiently with a color or black and white television receiver or monitor. For the first time, the 2637 UVI combines an object oriented approach with character generation (alphanumerics or other displayable forms) plus RAM-mapped color graphics.

The UVI's primary use is in microprocessor controlled home computers or game systems, however, it may also be used in other applications where the display of alphanumeric and graphics data is desired. In particular, the UVI has been designed to require a minimum of support components thereby allowing a system configuration that is optimized for the user's needs.

The UVI reads data and operational commands from a memory and produces video signals that result in the generation of alphanumeric or graphics color TV displays. Many of the common display circuits have been incorporated in a single chip, including:

- Analog to digital converters which accept potentiometer inputs
- Alphanumeric and special character generators
- Moving object circuits
- Audio signal generators

With the 2637, a typical system configuration consists of a UVI, a 2616/2632 ROM, a 2622 (NTSC) or 2621 (PAL) Universal Sync Generator (USG), a 2650 series microprocessor, four 2112 RAMs, and video summing circuitry. Additional UVIs, Programmable Video Interfaces (PVIs), as well as random logic can be interfaced to enhance game or system complexity.

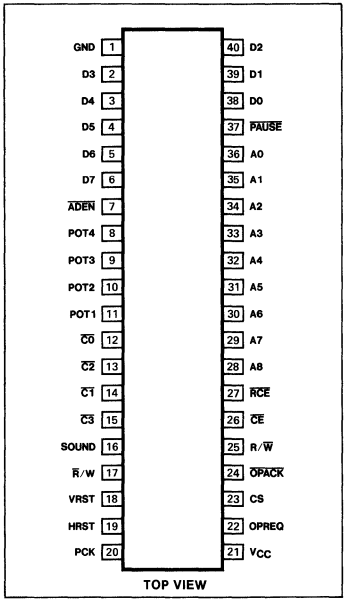
FEATURES

- **Four general purpose, RAM-resident objects**
- **280nsec object resolution**
- **Object size and position under program control**
- **Programmable multi-level sound and noise generators**
- **16 characters per display row**
- **13 or 26 character rows per screen**
- **40 alphanumeric characters**
- **16 background characters**
- **8 program definable characters**
- **64 graphics characters**
- **8 programmable color codes**
- **Chip enable outputs for I/O logic**
- **I/O facilities for switch scanning and potentiometer (RC) inputs**
- **Operates with both U.S. and European standards**
- **Single +5 volt power supply**
- **Forty-pin package**

APPLICATIONS

- **Video games**
- **Home computers**
- **Communications terminals**
- **Educational systems**
- **Process control displays**
- **Medical electronics**

PIN CONFIGURATION



TOP VIEW

UVI FUNCTIONAL DESCRIPTION

The 2637 UVI is a bus oriented device with address and data busses controlling the flow of data between the user's system and the UVI (see block diagram). Both the address and data busses are bidirectional.

The basic clock frequency and the horizontal and vertical reset signals to the UVI drive vertical and horizontal counters. The two counters provide the UVI with a Cartesian coordinate representation of the television screen, i.e., each counter pair describes a unique point on the screen. Typically these clock and reset signals are provided by a universal sync generator circuit.

A/D Block

The A/D Block converts the analog potentiometer position information into binary data which can be read by the system's CPU. Only two of the four potentiometers are active at any given time.

Address Block

The address block provides chip enable outputs for external RAMs and I/O buffers.

Sound Block

The sound block is a multi-level square wave generator sending out pulses at a user programmable audio frequency. Random noise is also generated and can be mixed with the audio frequency for simulating crowd noise, explosions, etc.

Internal Status Block

The internal status block accumulates status information which can be read by the CPU; for example, collisions

Color Mux System

The color multiplexer generates the color codes for characters, objects, and screen.

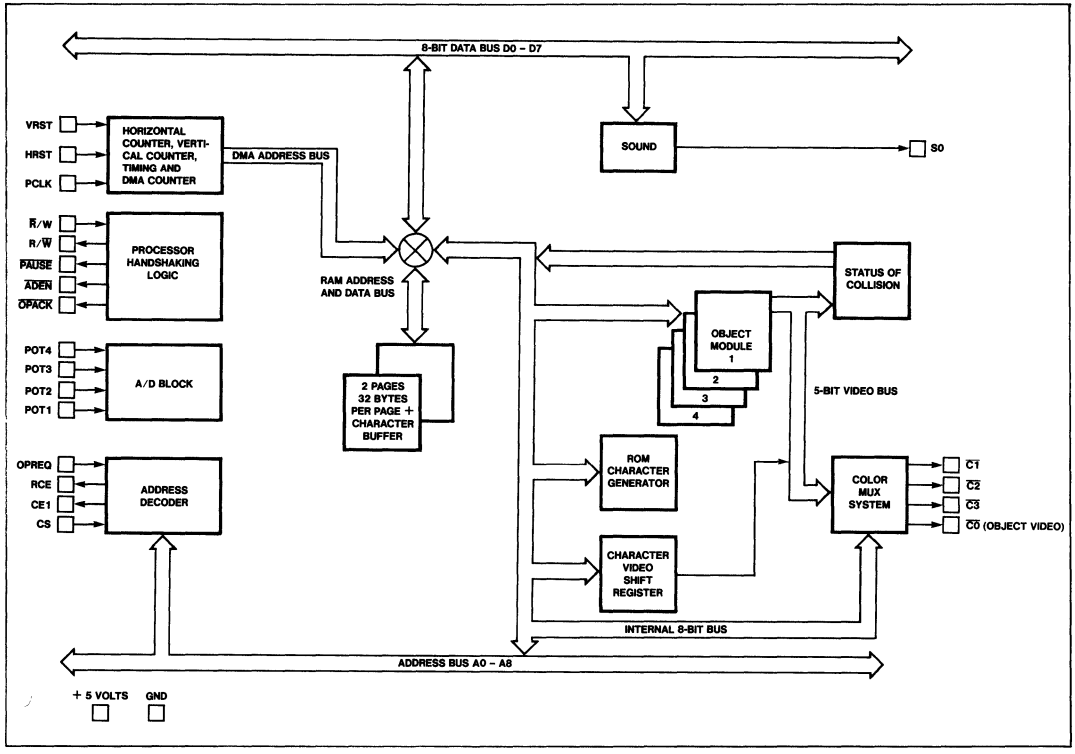
ROM Character Generator

The ROM character generator stores the character fonts.

RAM

The 64 bytes of RAM stores eight programmable character/object fonts

BLOCK DIAGRAM



5

MICROPROCESSOR SC2650A

PRODUCT BRIEF, contact your Signetics sales offices for complete information.

DESCRIPTION

The Signetics 2650A series are 8-bit general purpose microprocessors constructed using Signetics n-channel silicon gate MOS technology. The 2650 series executes a fixed instruction set, with each instruction being one to three bytes in length.

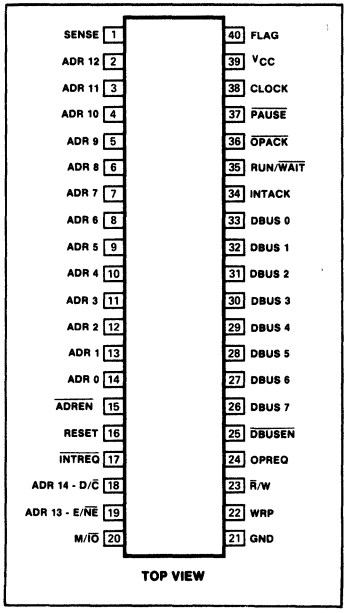
The 2650 instruction set consists of many powerful instructions which are all easily understood and are typical of larger computers. There are one-, two-, and three-byte instructions as a result of the multiplicity of addressing modes.

Addressing range of these processors is 32K bytes of memory and 258 I/O devices. A single level hardware vectored interrupt capability is provided.

FEATURES

- **Static 8 bit parallel NMOS microprocessor**
- **Single power supply of +5 volts**
- **TTL level single phase clock**
- **TLL compatible inputs and outputs**
- **Variable length instructions of 1, 2 or 3 bytes**
- **32K byte addressing range**
- **Coding efficiency with multiple addressing modes**
- **Synchronous or asynchronous memory and I/O interface**
- **Interfaces directly with industry standard memories**
- **Single bit serial I/O path**
- **Seven 8 bit addressable general purpose registers**
- **Vectored interrupt**
- **Subroutine return address stack**

PIN CONFIGURATION



MICROPROCESSOR BLOCK DIAGRAM

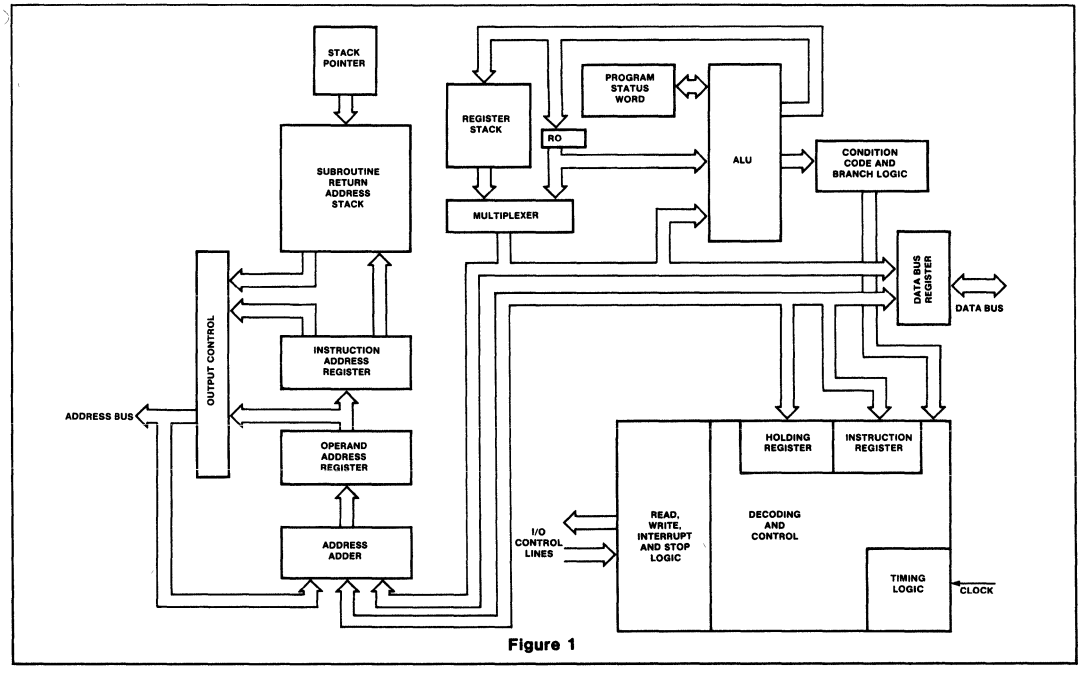


Figure 1

PIN DESIGNATION

MNEMONIC	NUMBER	NAME	TYPE	FUNCTION
ADR0-ADR12	14-2	Address lines	O	Low order memory address lines for instruction or operand fetch. ADR0 is the least significant bit and ADR12 is the most significant bit. ADR0 through ADR7 are also used as the I/O device address for extended I/O instructions.
ADR13-E/$\overline{NE}$	19	Address 13-Extended/Non extended	O	Low order memory page address line during memory reference instructions. For I/O instructions this line discriminates between extended and non-extended I/O instructions.
ADR14-D/$\overline{C}$	18	Address 14-Data/Control	O	High order memory page address line during memory reference instructions. It also serves as the I/O device address for non-extended I/O instructions.
$\overline{ADREN}$	15	Address enable	I	Active low input allowing 3-state control of the address bus ADR0-ADR12.
DBUS0-DBUS7	33-26	Data bus	I/O	These lines provide communication between the CPU, Memory, and I/O devices for instruction and data transfers.
$\overline{DBUSEN}$	25	Data bus enable	I	This active low input allows tri-state control of the data bus.
OPREQ	24	Operation request	O	Indicates to external devices that all address, data and control information is valid.
$\overline{OPACK}$	36	Operation acknowledge	I	Active low input indicating completion of an external operation. This allows asynchronous functioning of external devices.
M/$\overline{IO}$	20	Memory/input-output	O	Indicates whether the current operation references memory or I/O.
$\overline{R}$/W	23	Read/Write	O	Indicates a read or a write operation.
WRP	22	Write pulse	O	This is a timing signal from the 2650 that provides a positive-going pulse during each requested write operation (memory or I/O) and a high level during read operations.
SENSE	1	Sense	I	The sense bit in the PSU reflects the logic state of the sense input to the processor at pin #1.
FLAG	40	Flag	O	The flag bit in the PSU is tied to a latch that drives the flag output at pin #40.
$\overline{INTREQ}$	17	Interrupt request	I	This active low input line indicates to the processor that an external device is requesting service. The processor will recognize this signal at the end of the current instruction if the interrupt inhibit status bit is zero.
INTACK	34	Interrupt acknowledge	O	This line indicates that the 2650 is ready to receive the interrupt vector (relative address byte) from the interrupting device.
$\overline{PAUSE}$	37	Pause	I	This active low input is used to suspend processor operation at the end of the current instruction.
RUN/$\overline{WAIT}$	35	Run/Wait	O	This output is a processor status indicator. During normal operation this line is high. If the processor is halted either by executing a halt instruction or by a low input on the pause line, the run/wait line will go low.
RESET	16	Reset	I	Resets the instruction address register to zero. Clears interrupt inhibit.
CLOCK	38	Clock	I	A positive going pulse train that determines the instruction execution time.
V_{CC}	39	+5V supply	I	+5V power
GND	21	Ground	I	Ground

5

FUNCTIONAL DESCRIPTION

The 2650 series processors are general purpose, single chip, fixed instruction set, parallel 8-bit binary processors. A general purpose processor can perform any data manipulations through execution of a stored sequence of machine instructions. The processor has been designed to closely resemble conventional binary computers, but executes variable length instructions of one to three bytes in length.

The 2650 series contains a total of seven general purpose registers, each eight bits long. They may be used as source or destination for arithmetic operations, as index registers, and for I/O transfers.

The processor can address up to 32,768 bytes of memory in four pages of 8,192 bytes each. The processor instructions are one, two, or three bytes long, depending on the instruction. Variable length instructions tend to conserve memory space since a one-or-two byte instruction may often be used rather than a three byte instruction. The first byte of each instruction always specifies the operation to be performed and the addressing mode to be used. Most instructions use six of the first eight bits for this purpose, with the remaining two bits forming the register field. Some instructions use the full eight bits as an operation code.

The data bus and address signals are tristate to provide convenience in system design. Memory and I/O interface signals are asynchronous so that direct memory access (DMA) and multiprocessor operations are easy to implement.

The block diagram for the 2650 series (figure 1) shows the major internal components and the data paths that interconnect them. In order for the processor to execute an instruction, it performs the following general steps:

1. The instruction address register provides an address for memory.
2. The first byte of an instruction is fetched from memory and stored in the instruction register.
3. The instruction register (IR) is decoded to determine the type of instruction and the addressing mode.
4. If an operand from memory is required, the operand address is resolved and loaded into the operand address register.
5. The operand is fetched from memory and the operation is executed.
6. The first byte of the next instruction is fetched.

The instruction register holds the first byte of each instruction and directs the subsequent operations required to execute each instruction. The IR contents are decoded and used in conjunction with the timing information to control the activation and sequencing of all the other elements on the chip. The holding register is used in some multiple-byte instructions to contain further instruction information and partial absolute addresses.

The arithmetic logic unit (ALU) is used to perform all of the data manipulation operations, including load, store, add, subtract, AND, inclusive OR, exclusive OR, compare, rotate, increment and decrement. It contains and controls the carry bit, the overflow bit, the interdigit carry and the condition code register.

The register stack contains six registers that are organized into two banks of three registers each. The register select bit picks one of the two banks to be accessed by instructions. In order to accommodate the register-to register instructions, register zero (R0) is outside the array. Thus, register zero is always available along with one set of three registers.

The address adder is used to increment the instruction address and to calculate relative and indexed addresses.

The instruction address register holds the address of the next instruction byte to be accessed. The operand address register stores operand addresses and sometimes contains intermediate results during effective address calculations.

The return address stack (RAS) is a last in, first out (LIFO) storage which receives the return address whenever a branch-to-subroutine instruction is executed. When a return instruction is executed, the RAS provides the last return address for the processor's IAR. The stack contains eight levels of storage so that subroutines may be nested up to eight levels deep. The stack pointer is a three bit wraparound counter that indicates the next available level in the stack. It always points to the current address.

PROGRAM STATUS WORD

The program status word (PSW) is a major feature of the 2650 which greatly increases its flexibility and processing power. The PSW is a special purpose register within the processor that contains status and control bits.

It is divided into two bytes called the program status upper (PSU) and program status lower (PSL). The PSW bits may be tested, loaded, stored, preset, or cleared using the instructions which affect the PSW. The bits are utilized as shown in table 1.

Table 1 PROGRAM STATUS WORD

PSU0,1,2	SP	Pointer for the return address stack.
PSU3,4		Not used. These bits are always zero.
PSU5	II	Used to inhibit recognition of additional Interrupts.
PSU6	F	Flag is a latch directly driving the flag output.
PSU7	S	Sense equals the state of the sense input.
PSL0	C	Carry stores any carry from the high-order bit of ALU.
PSL1	COM	Compare determines if a logical or arithmetic comparison is to be made.
PSL2	OVF	Overflow is set if a two's complement overflow occurs.
PSL3	WC	With carry determines if the carry is used in arithmetic and rotate instructions.
PSL4	RS	Register select identifies which bank of 3 GP registers is being used.
PSL5	IDC	Inter digit carry stores the bit-3 to bit-4 carry in arithmetic operations.
PSL6,7	CC	Condition code is affected by compare, test and arithmetic instructions.

PSU

7	6	5	4	3	2	1	0
S	F	II	—	—	SP2	SP1	SP0

S Sense
F Flag
II Interrupt inhibit
SP2 Stack pointer two
SP1 Stack pointer one
SP0 Stack pointer zero

PSL

7	6	5	4	3	2	1	0
CC1	CC0	IDC	RS	WC	OVF	COM	C

CC1 Condition code one
CC0 Condition code zero
IDC Interdigit carry
RS Register bank select
WC With/without carry
OVF Overflow
COM Logical arithmetic compare
C Carry/borrow

INPUT/OUTPUT INTERFACE

The 2650 series microprocessor has a set of versatile I/O instructions and can perform I/O operations in a variety of ways. One-and two byte I/O instructions are provided, as well as a special single-bit I/O facility. The I/O modes provided by the 2650 are designated as data, control, and extended I/O.

Data or control I/O instructions, also called non-extended I/O instructions, are one byte long. Any general purpose register can be used as the source or destination. A special control line indicates if either a data or control instruction is being executed.

Extended I/O is a two-byte read or write instruction. Execution of an extended I/O instruction will cause an 8-bit address, taken from the second byte of the instruction, to be placed on the low order eight address lines. The data, which can originate or terminate with any general purpose register, is placed on the data bus. This type of I/O can be used to simultaneously select a device and send data to it.

Memory reference instructions that address data outside of physical memory may also be used for I/O operations. When an instruction is executed, the address may be decoded by the I/O device rather than memory.

MEMORY INTERFACE

The memory interface consists of the address bus, the 8-bit data bus and several signals that operate in an interlocked or handshaking mode.

The write pulse signal is designed to be used as a memory strobe signal for any memory type. It has been particularly optimized to be used as the chip enable or read/write signal.

INTERRUPT HANDLING CAPABILITY

The 2650 series has a single level hardware vectored interrupt capability. When an interrupt occurs, the processor finishes the current instruction and sets the interrupt inhibit bit in the PSW. The processor then executes a branch to subroutine relative to location zero (ZBSR) instruction and sends out interrupt acknowledge and operation request signals. On receipt of the INTACK signal, the interrupting device inputs an 8-bit address, the interrupt vector, on the data bus. The relative and relative indirect addressing modes combined with this 8-bit address allow interrupt service routines to begin at any addressable memory location.

INSTRUCTION SET

The 2650 instruction set consists of many powerful instructions which are all easily understood and are typical of larger computers. There are one-, two-, and three-byte instructions as a result of the multiplicity of addressing modes.

Automatic incrementing or decrementing of an index register is available in the arithmetic indexed instructions. All of the branch instructions except indexed branching can be conditional.

Register-to-register instructions are one byte; register-to-storage instructions are two or three bytes long. The two-byte register-to-memory instructions are either immediate or relative addressing types.

Section 6
Application Notes

INTERFACE TECHNIQUES FOR THE 2651 PCI — App Note M22

INTRODUCTION

The Signetics 2651 Programmable Communications Interface (PCI) is a universal synchronous/asynchronous data communications controller chip designed for microcomputer systems. The 2651 accepts programmed instructions from a microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

Although designed primarily to interface to a 2650 microprocessor, the 2651 can be easily integrated into systems employing other CPUs. This application note describes methods to interface the PCI to 8080A, SC/MP, Z80, 8085, and 6800-based microcomputer systems

INTERFACE SIGNALS

The PCI interface signals can be grouped into two types· the CPU-related signals, which interface the 2651 to the microprocessor system, and the device-related signals, which are used to interface to the communications device or system. The functions of the CPU-related signals of interest in this application note are detailed in Table 1 Timing signals for the CPU-PCI interface are illustrated in Figure 1, with relevant specifications summarized in Table 2

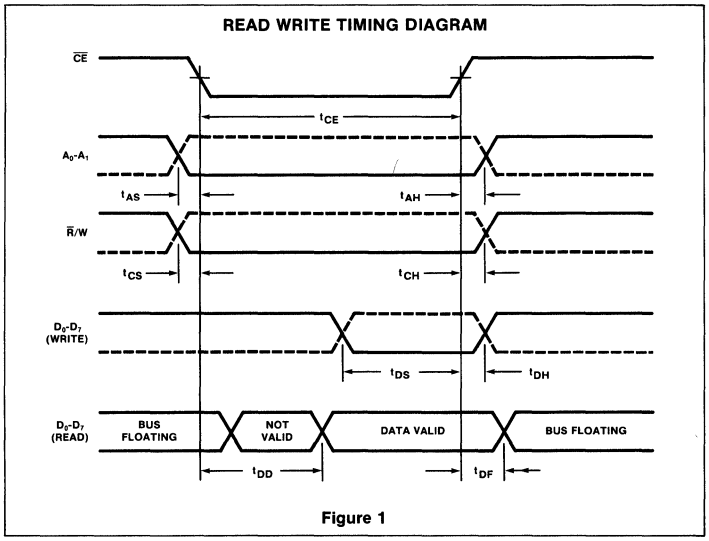


Figure 1

PIN NAME	PIN NO.	INPUT/OUTPUT	FUNCTION
A_1-A_0	10,12	I	Address lines used to select internal PCI registers
$\overline{R}/W$	13	I	Read command when low, write command when high.
$\overline{CE}$	11	I	Chip enable command When low, indicates that control and data lines to the PCI are valid and that the operation specified by the $\overline{R}/W$, A_1 and A_0 inputs should be performed. When high, places the D_0-D_7 lines in the tri-state condition.
D_7-D_0	8,7,6,5, 2,1,28,27	I/O	8-bit, three-state data bus used to transfer commands, data and status between PCI and the CPU. D_0 is the least significant bit, D_7 the most significant bit

Table 1 CPU-RELATED INTERFACE SIGNALS

PARAMETER		TEST CONDITIONS[1]	LIMITS Min	LIMITS Max	UNIT
t_{CE}	Chip enable pulse width		300		ns
	Setup and hold time				ns
t_{AS}	Address setup		20		
t_{AH}	Address hold		20		
t_{CS}	R/W control setup		20		
t_{CH}	R/W control hold		20		
t_{DS}	Data setup for write		225		
t_{DH}	Data hold for write		0		
t_{DD}	Data delay time for read	C_L = 100pF		250	ns
t_{DF}	Data bus floating time for read	C_L = 100pF		150	ns

Table 2 AC ELECTRICAL CHARACTERISTICS FOR CPU INTERFACE SIGNALS

NOTES
1 T_A = 0°C to +70°C, V_{CC} = 5V ±5%
2 Parametric values listed are from 2651 data sheet Consult latest data sheet for possible changes to specifications

2650 INTERFACE

The 2651 is designed to interface directly to the 2650 microprocessor bus The PCI may be addressed via the 2650 extended I/O instructions or it may be memory mapped, in which case it is addressed using the 2650 memory reference instructions. As shown in Figure 2, the 2651 chip enable (CE) input is generated by "NANDing" OPREQ with the appropriate control signals (depending on the addressing mode used) and the higher order address lines required to select the PCI.

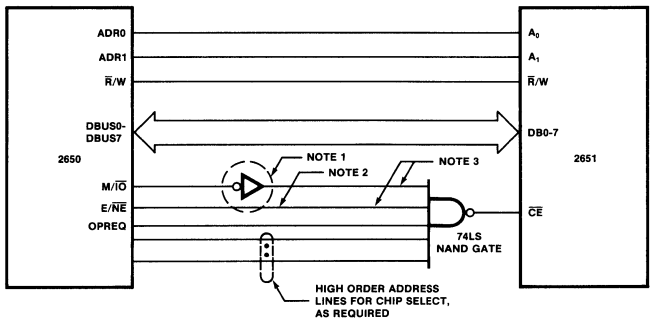
8080A INTERFACE

With regard to interfacing to the 2651, the major difference between a 2650 CPU and an 8080A system consisting of an 8080A CPU, 8224 Clock Generator, and 8228/38 System Controller (Figure 3) is the absence of a combined read/write signal suitable for the 2651 R/W input. Instead, the 8080A system provides separate IOR and IOW (or MEMR and MEMW) outputs which specify both the direction of data flow and the data transfer timing

The simplest way to accomplish the interface is to utilize an address line from the 8080A for the R/W input and to 'OR' the IOR and IOW (or MEMR and MEMW) signals for ultimate use as the 2651 chip enable signal, as illustrated in Figure 4 The only impact on system design is that the software must specify a different address to read the PCI mode or command registers than to write the same registers The selection of these addresses must result in a '0' at the R/W input for read operations and a '1' for write operations The resulting register addressing and function are summarized in Table 3

An analysis of the timing characteristics for the recommended configuration shows that adequate margins exist to satisfy both the 2651 and the 8080A specifications at the minimum 8080A clock period of 480ns The timing waveforms and calculations for the read and write cycles are shown in Figures 5 and 6.

2650-2651 INTERFACE



NOTES

1 Inverter required only if 2651 addressing is by extended I/O instructions (Write, Read)
2 This input required only if 2651 addressing is by extended I/O instructions and non-extended addressing is also used in the system
3 These inputs not required if all I/O addressing is memory mapped

Figure 2

OPERATION	A_2 (R/W)	A_1	A_0	REGISTER
READ	0	0	0	Receive Holding Register
	0	0	1	Status Register
	0	1	0	Mode Registers 1/2
	0	1	1	Command Register
WRITE	1	0	0	Transmit Holding Register
	1	0	1	SYN1/SYN2/DLE Registers
	1	1	0	Mode Registers 1/2
	1	1	1	Command Register

Table 3 PCI REGISTER ADDRESSING FOR 8080A INTERFACE

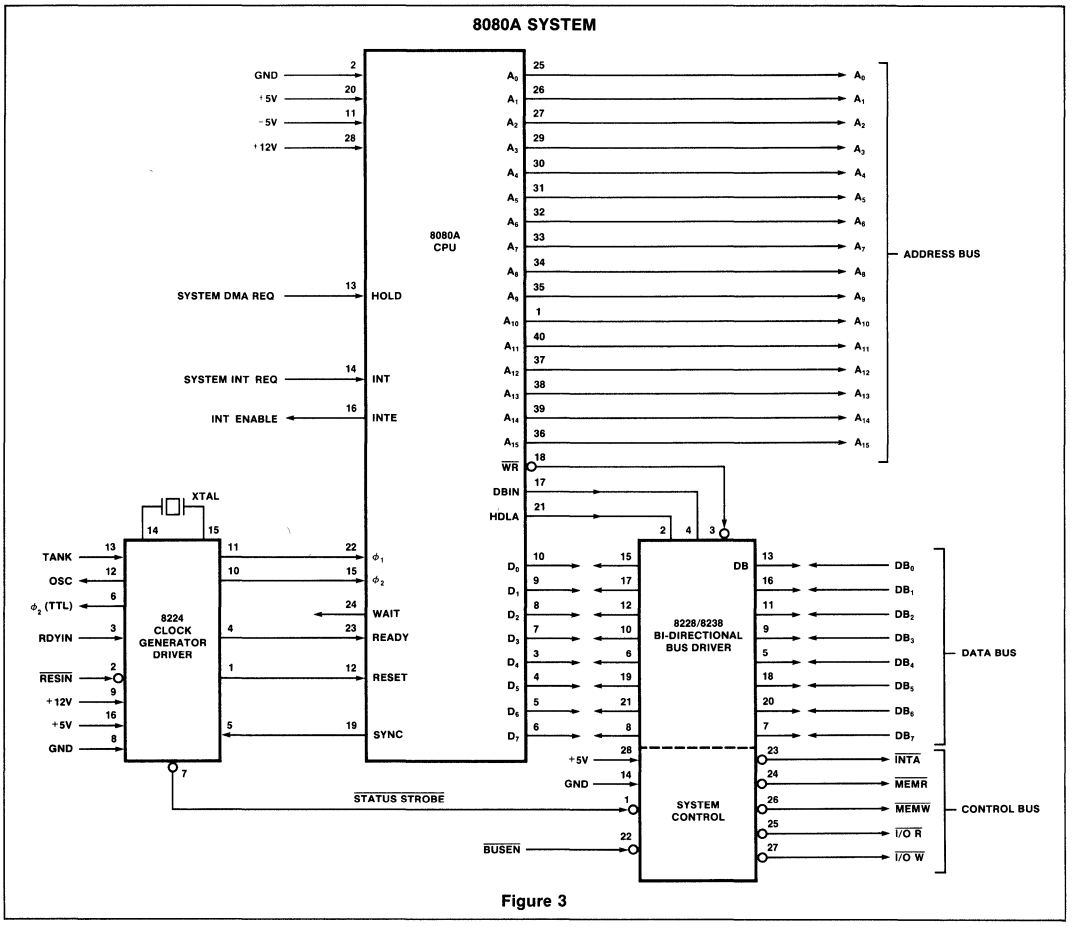


Figure 3

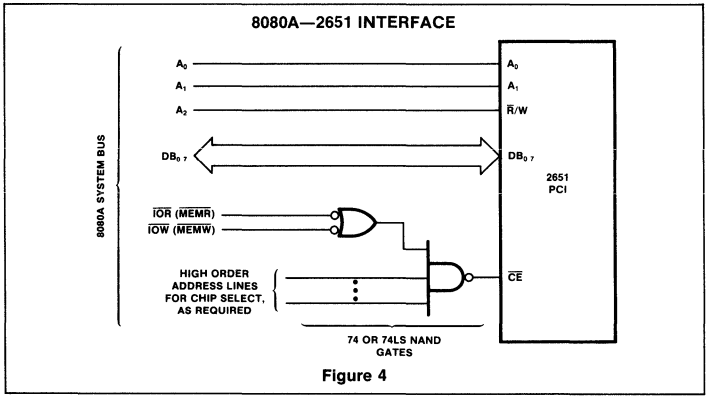
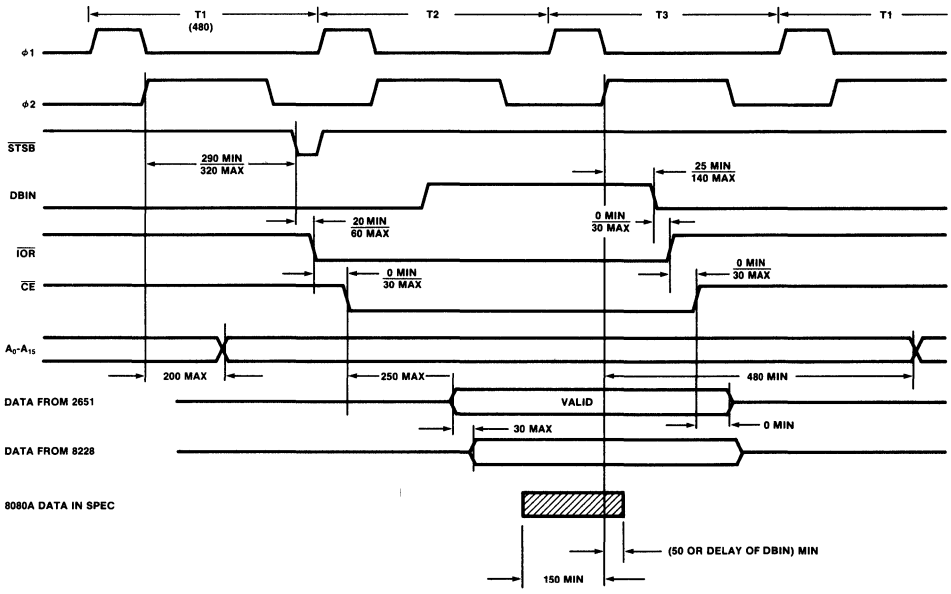


Figure 4

8080A—2651 READ TIMING



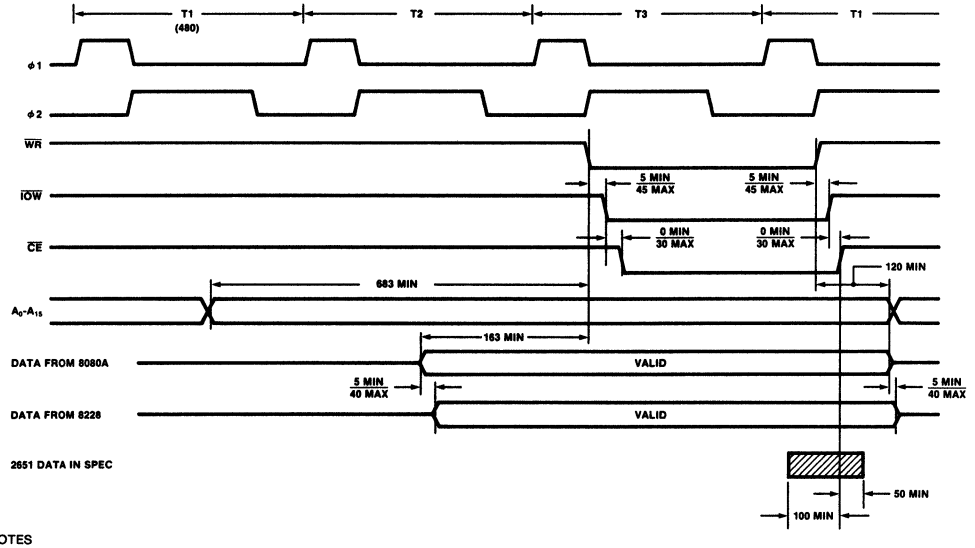
NOTES

1 All times in nanoseconds
2 Delay from φ2 of T1 to A_0, A_1, R/W = 200ns Max } t_{AS}, t_{CS} for 2651
Delay from φ2 of T1 to CE input = 310ns Min } are satisfied
3 Delay from φ2 of T3 to A_0, A_1, R/W changing = 480ns Min } t_{AH}, t_{CH} for 2651
Delay from φ2 of T3 to CE changing = 200ns Max } are satisfied
4 Delay from φ2 of T1 to 8080A data bus valid = 690ns Max } t_{DS1}, t_{DS2} for
Time from φ2 of T1 to 8080A data required = 810ns Max } 8080A are satisfied

Figure 5

6

8080A—2651 WRITE TIMING

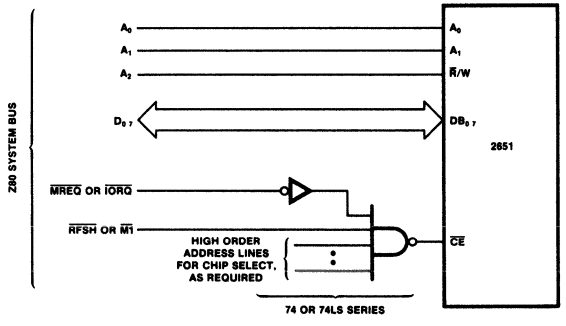


NOTES

1 All times in nanoseconds.
2 Time prior to $\overline{WR}$ A_0, A_1, R/W valid = 683ns Min } t_{AS}, t_{CS} for 2651 are satisfied
Time after $\overline{WR}$ $\overline{CE}$ valid = 5ns Min }
3 Time after $\overline{WR}$ A_0, A_1, R/W valid = 120ns Min } t_{AH}, t_{CH} for 2651 are satisfied
Delay from $\overline{WR}$ to $\overline{CE}$ = 75ns Min }
4. Data available to 2651 prior to $\overline{CE}$, therefore t_{DS} for 2651 is satisfied
5. Time after $\overline{WR}$ data available at 2651 = 125ns Min } t_{DH} for 2651 is satisfied
Delay from $\overline{WR}$ to $\overline{CE}$ = 75ns Max }

Figure 6

Z80—2651 INTERFACE



NOTE:
$\overline{MREQ}$, $\overline{RFSH}$ used for memory mapped I/O
$\overline{IORQ}$, $\overline{M1}$ used for standard I/O

Figure 7

Z80 INTERFACE

The Z80 CPU provides separate $\overline{RD}$ and $\overline{WR}$ signals to indicate read and write operations respectively. In addition, an $\overline{MREQ}$ signal (for memory operations) or an $\overline{IORQ}$ signal (for I/O operations) are also provided. Although the $\overline{RD}$ signal could logically be used as the R/W input for the 2651, with either $\overline{MREQ}$ or $\overline{IORQ}$ used as the $\overline{CE}$ input, as appropriate, the Z80 timing specifications are such that the control hold time specification (t_{CH}) for the 2651 could not be guaranteed.

To overcome this problem, a technique utilizing an address line for the R/W input is recommended, as previously discussed for the 8080A interface.

Interfaces for memory mapped and I/O mapped operations are shown in Figure 7. The $\overline{M1}$ signal inhibits 2651 operation during interrupt acknowledge cycles. Similarly, $\overline{RFSH}$ inhibits operation of the 2651 during memory refresh cycles. A detailed timing analysis shows that all pertinent 2651 and Z80 timing specifications are satisfied with the techniques illustrated.

SC/MP II INTERFACE

The bus interface signals for the SC/MP II are similar to those previously described for the 8080A and Z80, except that only memory reference operations are available. Again, a technique using an address line for the 2651 $\overline{R}$/W input is recommended, as shown in Figure 8. All timing requirements for the 2651 and SC/MP II are easily satisfied.

6800 INTERFACE

The 6800 microprocessor provides a R/W signal which, when inverted, is suitable for use by the 2651. The remainder of the interface logic required consists of gating of the appropriate bus signals to generate the $\overline{CE}$ signal for the 2651, as shown in Figure 9.

The only timing parameter which is not easily satisfied is the write data hold time for the 2651 (t_{DH}), which is specified at 0ns minimum. The 6800 specifications guarantee only a minimum of 10ns data hold time with respect to the DBE processor input, which is normally the $\phi 2$ clock. To guarantee worst-case operation, the DBE signal should be skewed with respect to $\phi 2$ to guarantee the minimum data hold time at the 2651. Consult the M6800 System Design Data Manual for detailed information.

8085 INTERFACE

The bus signals of an 8085 microcomputer system are similar to those of the 8080A system shown in Figure 3. The major differences are the multiplexing of the eight least significant bits of address on the data bus and the use of an IO/$\overline{M}$ control line to distinguish between memory and I/O references.

Since a single $\overline{R}$/W control line is not available, the same addressing technique for the 2651 registers as described for the 8080A interface is recommended. Thus, the interface will be similar to the one shown in Figure 4

If I/O addressing is used, A0-A2 in Figure 4 can be replaced by the non-multiplexed higher order address lines A8-A10, since the 8085 provides the I/O address on both A0-A7 and A8-A15 during an INPUT and OUTPUT instruction. In addition, the inverted IO/$\overline{M}$ signal must be used as an input to the final NAND gate.

If memory addressing is used for the 2651, A0-A2 must be obtained by demultiplexing from the address/data bus through an external latch clocked by the ALE timing signal. If IO addressing is also used in the system, the M/$\overline{IO}$ signal must be used in the final NAND gate.

The 8085 timing specifications are such that all 2651 requirements are easily satisfied. Similarly, the 2651 timing satisfies the 8085 requirements.

SC/MP II—2651 INTERFACE

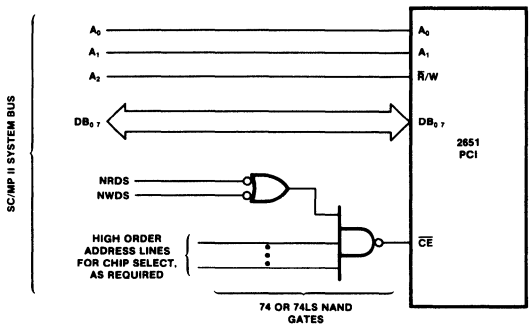


Figure 8

6800—2651 INTERFACE

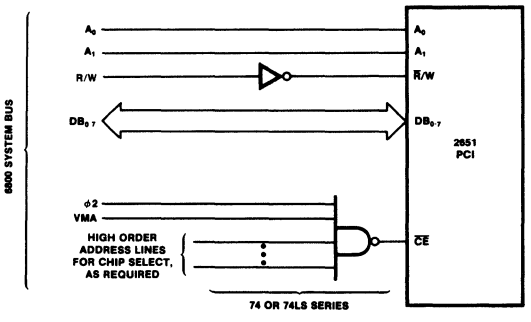


Figure 9

REFERENCES

1. Signetics 2651 PCI Specification
2. Signetics MP8080A Microprocessor Specification
3. Signetics SC/MP II (ISP-8A/600) Microprocessor Specification
4. Zilog Z80 CPU Product Specification
5. Intel Data Catalog, 1977
6. Intel MCS 85 User's Manual
7. Motorola M6800 Microcomputer System Design Data

The 2651 PCI supports IBM's Binary Synchronous Communications (BISYNC) protocol, with SYN and DLE character stripping, DLE generation, and a transparent mode of operation Please refer to the 2651 data sheet when reading this application note

OPERATION IN THE NORMAL (NON-TRANSPARENT) MODE

Initialization

Initialize the internal PCI mode and command registers as follows:

MR17 = 0 Double SYN (even though the same SYN character is used)

MR16 = 0 Non-transparent mode

MR15-12 = See table 1

MR11-10 = 00 Synchronous mode, 1X clock

MR25 = 0 or 1 External/Internal TxC

MR24 = 0 External RxC (supplied by modem).

MR23-20 = 0000 thru 1111 Set for desired baud rate if internal TxC is used.

CR7-6 = 00 or 01 Normal or SYN and DLE stripping mode (depends on software)

The SYN1 and SYN2 registers should be loaded with the appropriate SYN character for the code set in use The DLE register should be loaded if operation in the transparent mode is required

SYN Character Transmission and Reception

When the PCI transmitter is initially enabled (CR0 = 1), the TxD output remains high until the first character to be transmitted (usually a SYN or PAD) is loaded into the THR Subsequent to this, the PCI will automatically fill gaps by transmitting a character pair consisting of the contents of the SYN1 register followed by the contents of the SYN2 register (DLE-SYN1 in transparent mode)

The receiver enters the hunt mode on a 0-to-1 transition of RxEN (CR2). If in the normal mode (CR7-6 = 00), receipt of a SYN character should be checked by doing a software comparison. If SYN/DLE stripping is selected (CR7-6 = 01), then SYN detect (SR5) indicates SYN character reception since the SYN characters will be stripped

CODE SET	FORMAT	MR15	MR14	MR13	MR12
EBCDIC	8 bits, no parity	X[2]	0	1	1
ASCII	7 bits, odd parity	0	1	1	0
SBT[1]	6 bits, no parity	X	0	0	0

NOTES
1 Six-Bit Transcode
2 X = Don't care

Table 1 INITIALIZATION REQUIREMENTS vs CODE SET

Transmission Code	No Transparency	Transparency Operating	Transparency Not Operating
EBCDIC	CRC-16	CRC-16	CRC-16
ASCII	VRC-LRC	CRC-16	VRC-CRC-16
SBT	CRC-12	CRC-12	CRC-12

Table 2 ERROR CHECKING REQUIREMENTS FOR BSC

The processor can read SR5 after $\overline{\text{RxRDY}}$ goes active to indicate that the first non-SYN character is in the RHR

Error Checking

The type of error checking depends on the information code set used. VRC and LRC are used with non-transparent mode ASCII, CRC-12 is used with six-bit transcode, CRC-16 is used with EBCDIC, and VRC and CRC-16 are used with ASCII if a transparent mode is supported This is summarized in table 2

The 2651 PCI is capable of performing VRC generation, detection and stripping. The BCC (LRC or CRC) must be computed using software or external hardware (see section on BCC Generation/Checking)

Each block of data transmitted is error-checked at the receiver. The receiving station normally replies with ACK 0 or ACK 1 (data accepted, continue sending) or with NAK (data not accepted, i.e , a transmission error was detected, retransmit the block). There is no error correction.

The three error-checking methods used in conjunction with BISYNC are VRC, LRC and CRC. These are defined below.

VRC (vertical redundancy check) is an odd-parity check performed on each data character and the LRC character. It is disabled during operation in the transparent mode

LRC (longitudinal redundancy check) is a horizontal parity check on all data bits within the message block. It is transmitted as a single BCC (block check character) immediately following an ETB, ETX, or ITB character. The receiver compares the transmitted BCC with its accumulated BCC. An equal comparison indicates a good reception of the previous block.

CRC (cyclic redundancy check) is a division performed by the transmitting and receiving stations using the numeric binary value of the message as a dividend The dividend is initially zero. The constant divisor is either $X^{16} + X^{15} + X^2 + X^1$ (CRC-16), or $X^{12} + X^{11} + X^3 + X^2 + X + 1$ (CRC-12). The quotient is discarded and the remainder is retained as the two-byte BCC

The BCC accumulation (LRC or CRC) is reset by the first STX or SOH after line turnaround. Thereafter, all characters except SYN and DLE (but not the second DLE-DLE in transparent mode) are included in the accumulation At the end of an intermediate block (ITB-BCC), the accumulation resets and starts again with the next received STX or SOH or DLE-STX in the transparent mode.

OPERATION IN THE TRANSPARENT MODE

BSC incorporates a submode called "transparent mode " This mode allows communication of pure data (such as binary files) instead of information code characters. Operation in the transparent mode is initiated by transmission (reception) of a DLE-STX sequence and terminated by a closing DLE-ETX, DLE-ETB, or DLE-ITB sequence. While in the transparent mode, the following procedures apply:

- Parity (VRC) is disabled and the character length is changed to 8 bits This applies only to ASCII code. For EBCDIC code, VRC is never enabled.

- DLE-SYN is used for line fill instead of SYN-SYN
- Any control character transmitted must be preceded by a DLE
- If a data byte identical to a DLE is to be transmitted, it must be preceded by another DLE

Transparent Mode Bit MR16 = 1 results in

Receiver: Enables DLE stripping if CR7-6 = 01 and a DLE is received.

Enables DLE detect bit (SR3) if a DLE is received

Enables SYN detect bit (SR5) on receipt of DLE-SYN1 after synchronization has been achieved.

Transmitter: DLE-SYN1 is used as line fill during underrun.

Initiating the Transparent Mode

Receiver: Detects DLE-STX sequence in software and sets MR16, if desired

If ASCII code is used, then parity control (MR14) should be disabled, and the character length (MR13-12) should match the transparent data (usually 8 bits).

If the mode register is changed (as prescribed) ½ to 1½ RxC times after $\overline{\text{RxRDY}}$ goes active, the character being assembled in the receiver shift register will be of the new length and parity setting. Otherwise, the new mode characteristics apply to the next character to be assembled.

Transmitter: Sends DLE-STX sequence from THR, and then sets transparent mode (MR16). If ASCII code is used, then MR14 will be disabled and MR13-12 should match the transparent data character length (usually 8 bits) The mode register may be changed within n TxC times after $\overline{\text{TxRDY}}$ goes active, where n = the character length in the non-transparent mode (assuming transparent mode character length is greater) This ensures that the character loaded into THR will be transmitted with the new character length and parity setting

Use of PCI Transparent Mode Features

- Send DLE (CR3) Command

To ensure that there is no transmitter underrun between a DLE and the control character or DLE character to follow, the send DLE bit may be used. The sequence of operations is as follows:

1) Set CR3 in response to $\overline{\text{TxRDY}}$ and then load THR with the control or DLE character to follow This ensures that a DLE will precede the character loaded
2) Reset CR3 on the next $\overline{\text{TxRDY}}$, and then load THR with the next character to be transmitted.

Alternatively, the DLE character could be loaded into THR without using CR3 if there is no possibility of underrun.

- DLE detect (SR3) Status Bit

The DLE Detect bit is set when parity is disabled (MR14 = 0), the transparent mode is selected (MR16 = 1), and a DLE character has been assembled in the receiver shift register. A reset error command (CR4) must be issued to clear the DLE detect condition. If DLE stripping is not selected (CR7-6 = 00), then DLE detection could be done by software comparison on a character-by-character basis

- SYN/DLE Stripping Mode

If CR7-6 = 01 in the synchronous mode, then SYN and odd DLE characters are stripped from the receiver holding register The second DLE of a DLE-DLE pair is not stripped This mode is not recommended for transparent mode.

Returning to Normal Operation

1) Normal operation is resumed after a DLE-ETX, DLE-ETB, or DLE-ITB sequence is received or transmitted.
2) MR16, MR14, and MR13-12 must be changed if they were altered when entering the transparent mode Mode register 1 should be addressed with TxEN — RxEN = 0

BCC GENERATION/CHECKING

The 2653 PGC can be effectively used as a parallel CRC/LRC generator/checker and also serve as a programmable single and DLE two character sequence detector Figure 1 demonstrates the 2651/2653 bus interface. Consult the 2653 data sheet in order to properly utilize that device

For BISYNC non-transparent messages, the 2651 can be programmed to strip received SYN characters which are not usually stored in main memory. Stripping mode should be terminated upon the PGC's detection of a BTC (block terminating character) or a DLE-STX SCC (second search character) In the first case, a block check character could match a SYN; in the second case the PGC needs to see all received transparent data characters in order to calculate the CRC/LRC and detect the BTC properly

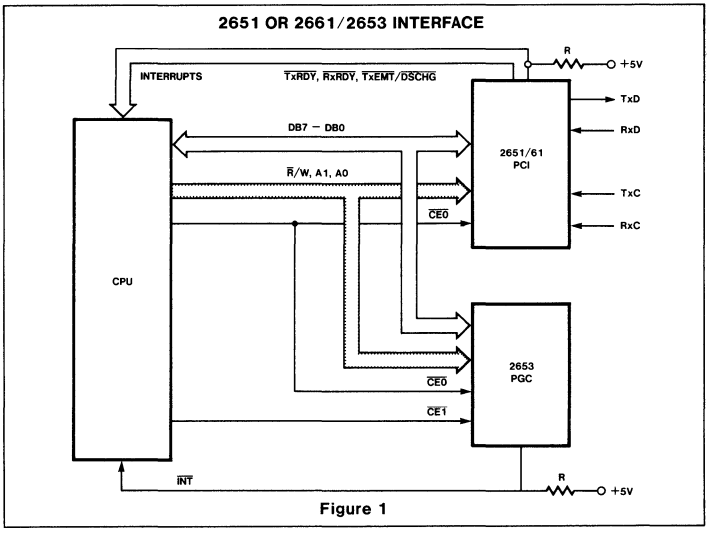


Figure 1

INTRODUCTION

The Signetics 2651 Programmable Communications Interface (PCI) is a universal synchronous/asynchronous data communications controller chip designed for use with microcomputers and minicomputers The 2651 accepts programmed instructions from a CPU and supports many serial data communications disciplines, both synchronous and asynchronous, in full or half-duplex, including IBM's Binary Synchronous Communications Protocol (BISYNC) The reader is referred to the 2651 Data Sheet for general specifications and to applications memo M22 for interface techniques with such microprocessors as 8080A, SC/MP, Z80, 8085, and 6800 Techniques for using the 2651 PCI to support BISYNC are detailed in application memo M24. The purpose of this applications memo is to assist the designer by demonstrating various interface and operational procedures which have been successful with the 2651 While we have tried to cover several possibilities in each procedure, the techniques shown should not be construed to be constraining and the designer is encouraged to develop whatever interface techniques best fit his application.

PROCEDURES FOR TERMINATING TRANSMISSION

FULL DUPLEX (RTS always true)

1 Load last character into THR in response to $\overline{\text{TxRDY}}$ going active low
2. Disable TxEN (0→CR0) in response to the next $\overline{\text{TxRDY}}$. This will cause $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ to remain in the high state after the last character (in TxSR) is serialized.

HALF DUPLEX (RTS true when transmitting; false otherwise)

Synchronous—use a closing PAD

1 Load an all 1's PAD character into THR in response to $\overline{\text{TxRDY}}$ At this time the previous (last) data character is in TxSR being serialized
2. Disable TxEN as above In this case, the last data character has been transmitted when $\overline{\text{TxRDY}}$ goes active.
3. Drop RTS (0→CR5). One or more bits of the PAD character will be transmitted on TxD before the $\overline{\text{RTS}}$ pin (23) goes high

Asynchronous—wait for $\overline{\text{TxEMT}}$

1 Load last character into THR in response to $\overline{\text{TxRDY}}$
2 Mask out the $\overline{\text{TxRDY}}$ interrupt condition by externally disabling it This can be done through a gate, interrupt controller chip, or CPU mask flip-flop. Note that $\overline{\text{TxRDY}}$ and $\overline{\text{TxEMT}}$ cannot be tied together (see Figure 1)
3 Drop RTS in response to the next $\overline{\text{TxEMT}}$. $\overline{\text{TxEMT}}$ going active indicates that the last character has been transmitted The TxD state will be marked hold one bit time after $\overline{\text{TxEMT}}$ goes active

PCI INTERRUPT REQUESTS $\overline{\text{IR1}}$ AND $\overline{\text{IR2}}$ WHEN $\overline{\text{TxEMT}}$/DSCHG MUST BE SEPARATED FROM $\overline{\text{TxRDY}}$

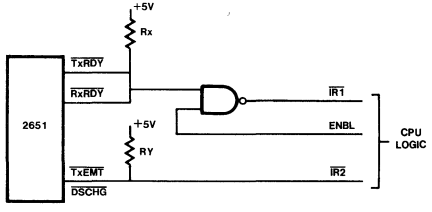


Figure 1

DISTINGUISHING BETWEEN TxEMT AND DSCHG CONDITIONS

The DSCHG condition goes active on a state change of either the $\overline{\text{DCD}}$ or $\overline{\text{DSR}}$ pin(s) provided either RxEN or TxEN = 1 but not in local loopback mode The DCD and DSR status bits (SR6, SR7) reflect the pin status at the time the status register is read, i e., they are not latched. A Status Read will clear the DSCHG condition.

The TxEMT condition goes active during transmitter underrun. The condition is immediately reset when a character is loaded into THR It is reset after the linefill is sent once the transmitter is disabled (TxEN = 0)

Since both of these conditions share a pin (18) and a status register bit (SR2), it is necessary to determine which or both conditions are present when the pin/status bit is active (Figure 2)

FLOWCHART TO DISTINGUISH BETWEEN TxEMT & DSCHG

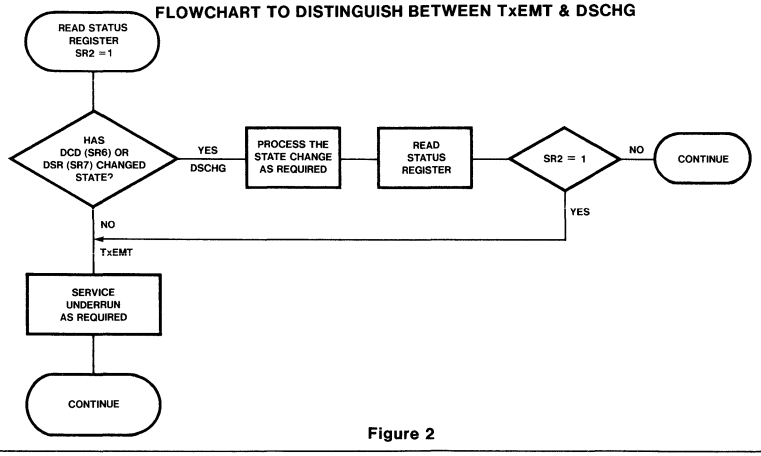


Figure 2

GENERATING CORRECT INITIALIZATION STATE OF TxD

After a power-on or RESET all Mode register bits will be zero Specifically, MR25 will select external TxC The TxD pin requires at least one high to low transition on $\overline{TxC}$ for TxD to go high. Without a $\overline{TxC}$ input, a break (all zeros) may be transmitted This presents a problem in asynchronous mode when using the internal BRG (MR25 = 1) To circumvent the problem, the user may take one of the following actions:

a) Generate one high to low transition on $\overline{TxC}$ during a power on or RESET
b) Input a system clock or the BRCLK into $\overline{TxC}$ through a 1K resistor.
c) Inclusive OR $\overline{RTS}$ and TxD to produce the Tx serial data to the modem
d) Use external logic (Figure 3) to insure TxD comes up in the "1" state.

LOGIC TO GUARANTEE TxD = 1 ON POWER UP OR RESET

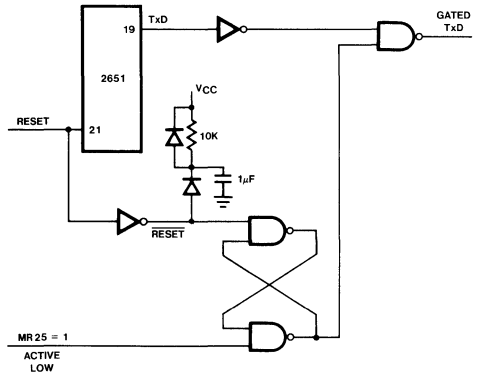


Figure 3

USING THE PCI BEYOND THE SPECIFIED SERIAL DATA RATE

If local loopback is not required, the PCI will operate correctly if the $\overline{RxC}$ high and low times are equal to or greater than 500 ns. A 1 Mbps DC baseband link between two PCI's is therefore quite acceptable. The only requirement is a synchronizing flip flop at the transmitter to compensate for the uncertainty in $t_{\overline{TXD}}$, the TxD delay from the falling edge of $\overline{TxC}$. That time can be anywhere from 150 ns to 650 ns (Fig. 4).

1Mbps DC BASEBAND LINK

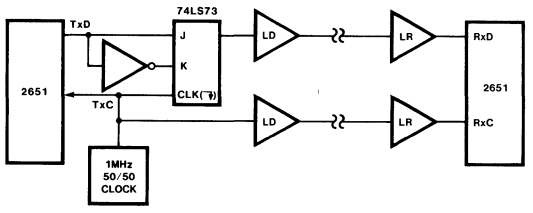


Figure 4

ANALYSIS OF PULL UP RESISTOR VALUES FOR 2651 PCI WIRE-OR OF OPEN DRAIN OUTPUTS

This discussion is intended to assist the user in determining pull up resistor values for open drain output $\overline{TxRDY}$, $\overline{RxRDY}$, $\overline{TxEMT/DSCHG}$ shown in Figure 1 (Rx, Ry)

1. Rx min wish to maintain acceptable "0" V output

$$Rx_{min} = \frac{V_{CC}\ max - V_{OL}\ max}{I_{OL} max + I_{IL}\ \mu P} = \frac{(5\ 25 - 45)\ volts}{(1\ 6 + 01)mA} = \frac{4\ 8}{1\ 61}\ k\Omega$$

only one output sinking (low) = 3kΩ

2. Rx max wish to maintain acceptable "1" V output

$$Rx_{max} = \frac{V_{CC}\ max - V_{OH}\ min}{3 \times I_{OH} - I_{IL}\ \mu P} = \frac{(4\ 75 - 2\ 4)V}{(3x\ 01 - 01)mA} = 117\ 5k\Omega$$

all outputs sourcing (high)

USING THE 2653 POLYNOMIAL GENERATOR AND CHECKER App Note 400

INTRODUCTION

When transferring data via a data communications link using any protocol, the only way to ensure a correct transfer is to perform error checking on the messages being exchanged. Error checking can be accomplished through vertical, longitudinal and cyclic redundancy checks, special character recognition and transparent operating modes. If the error checking is performed correctly, the result is an accurate transfer of data from station to station. The checking technique can be performed by software only, but this may result in a reduction of the maximum channel speed, may reduce the number of channels which can be handled by the CPU, or may limit the supplementary tasks which can be performed by the CPU. The most efficient way to accomplish error checking is to use a combination of hardware and software.

The Signetics 2653 Polynomial Generator and Checker (PGC) is designed to provide the above error checking capability while operating with asynchronous, synchronous or parallel receivers or transmitters at a speed of up to 500K characters per second. The PGC is a device that monitors parallel data transferred between a CPU or memory and a serial receiver/transmitter (R/T, UART, USRT, etc.) or other bus oriented device. Operation is two-way alternate (half-duplex) in that the PGC is selected to receive characters either from the R/T or from the CPU. Full duplex operation is achieved by using two PGCs. A unique feature of the 2653 is its 'character class array', a 128x2 RAM which is used to classify received characters into one of four types - normal, sync/not included, block terminating character, and secondary search character. The received characters may be block checked and/or compared to the special characters preloaded into the character class array. In addition to the block check character (BCC) generation, the PGC is capable of single character detection, two character sequence detection and parity generation and checking. All operating modes are software programmable and can be changed for each application. Figure 1 illustrates the block diagram of the PGC, while figure 2 describes the formats of the registers used to program its operation.[1]

The block check character (BCC), which the 2653 computes from monitoring the 8-bit data bus, takes the form of a cyclic redundancy check (CRC) on specified characters. The CRC is a reliable method of detecting errors in received serial data streams and is employed in almost all synchronous data communications protocols. The PGC can compute the BCC in four modes: BISYNC normal, BISYNC transparent, automatic accumulate, and single accumulate. In each of these modes, one of three error polynomials (CRC-16, CRC-12, and LRC-8) can be selected. In either of the BISYNC modes, the 'intelligence' provided by the character comparison capability within the chip enables it to know which characters to include and which to exclude from the BCC accumulation. Additionally, block terminating characters can be detected as well as the initiation and termination of BISYNC transparent mode. As a result, it can handle character oriented processing for IBM BISYNC, ANSI 3.28, ISO 1745, DEC DDCMP, and other disciplines.

[1]See the 2653 data sheet for full operational description.

BLOCK DIAGRAM

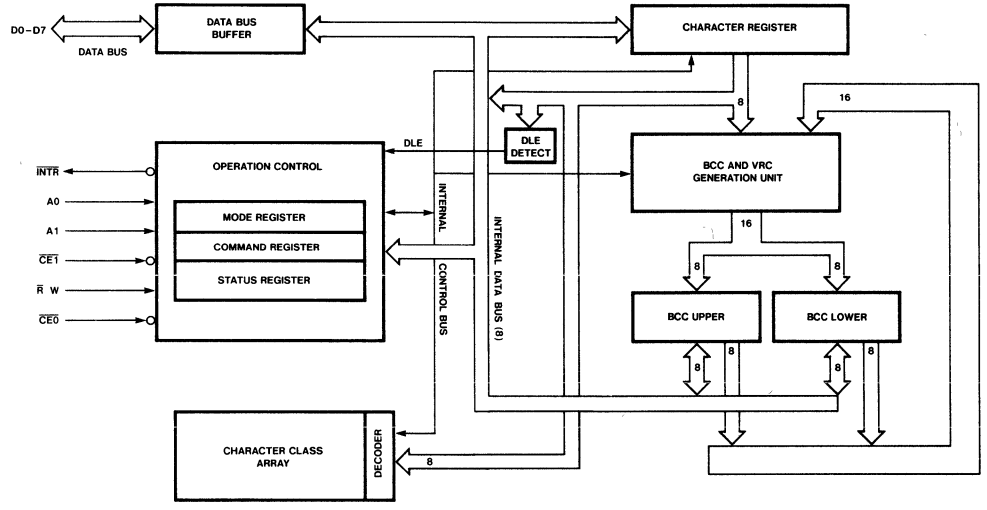
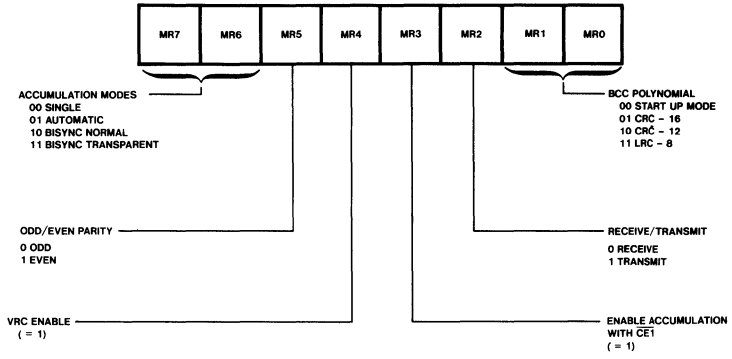
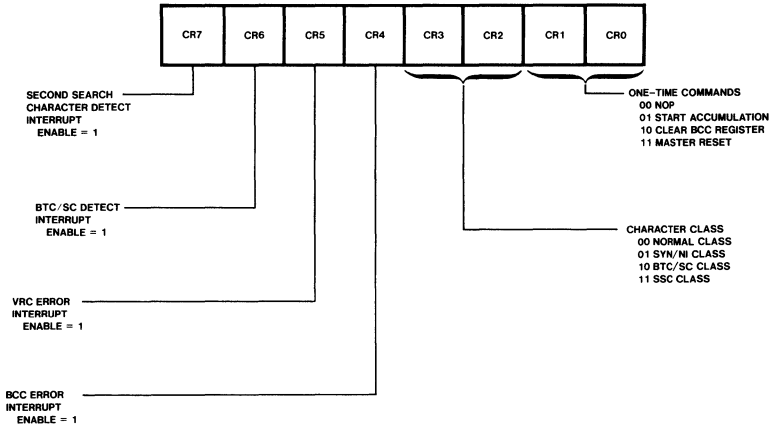


Figure 1

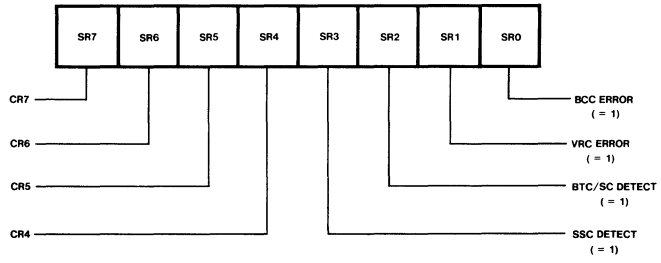
PGC REGISTER BIT FORMATS



MODE REGISTER



COMMAND REGISTER



STATUS REGISTER

Figure 2

USING THE 2653 POLYNOMIAL GENERATOR AND CHECKER App Note 400

A companion chip, the Signetics 2661 Enhanced Programmable Communications Interface (EPCI), directly combines with the 2653 to effect a synchronous/asynchronous character oriented communications link. If a complete multi-protocol interface is desired, it can be obtained using the PGC in conjunction with the Signetics 2652 Multi-Protocol Communications Controller (MPCC).

PROTOCOLS

Protocols provide the necessary ground rules to assure the orderly and accurate transfer of data between digital equipments. Data communications protocols are becoming increasingly important as the terminal population increases, distributed processing becomes widespread, and new communications technologies, such as packet switching and satellite links, become commonplace.

The protocols associated with the data communications have been classified into several major levels, or layers, that define various functions and operations. Each level is designed to be functionally independent of the others, but each depends on the correct operation of the previous level to operate. The protocols embodied in these levels range from those that define the physical and electrical links, e.g. RS232C and CCITT V.35, to those which are responsible for functions such as message buffering, code conversion, recognizing and reporting faulty conditions in terminals or lines, communication with the host mainframe, and management of the communication network. These protocols are implemented by software packages such as IBM's Systems Network Architecture (SNA), CCITT's X.25, and DEC's DECnet.

In the remainder of this application note, we shall concern ourselves with data link control protocols (DLC's), which are the sets of rules necessary for effective communications between terminals and computers over conventional communications channels. DLC's are concerned with handling the communications link itself and moving information across it efficiently and accurately.

The basic functions of a DLC are to:

1. Establish and terminate a connection between two stations.
2. Assure message integrity through error detection, requests for retransmission, and positive or negative acknowledgments.
3. Identify sender and receiver through polling or selection.
4. Handle special control functions such as requests for status, station reset, reset acknowledge, start, start acknowledge, and disconnect.

Data link controls can be classified into character oriented protocols (COPs) and bit oriented protocols (BOPs). COPs can be further subdivided into byte control protocols (BCPs) and character count protocols (CCPs).

BISYNC TEXT MESSAGE FORMAT

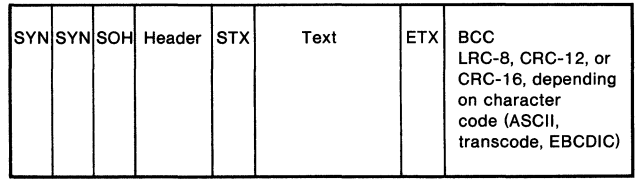


Figure 3

BYTE CONTROL PROTOCOLS

In BCPs, a defined set of communication control characters effects the orderly operation of the data link. IBM BISYNC, ANSI 3.28 and ISO 1745 are all byte controlled. Control characters and two character sequences configure and manage the data link between sender and receiver. Control messages or acknowledgements consist of one or two characters while data messages usually contain less than 1,000 characters. For text messages, shown in figure 3, an optional header may precede each text (information) block. The entire message block is error checked based on the information code set used (ASCII, EBCDIC, SBT) and the operational status of a transparent text mode. The transparent text mode is a means of identifying pure data characters from the characters of the information code set. For example, packed BCD, floating point numbers or memory image data would be sent in the transparent mode such that the receiver would not interpret that data as code set characters. Transparent mode is initiated by the sequence DLE-STX and terminated by a DLE followed by a block terminating character (ETX, ETB, ITB, or ENQ).

Byte controlled protocols utilize a stop and wait automatic repeat request (ARQ) which limits operation to two way alternate (half duplex). Each transmitted message block must be acknowledged before the next message may be sent. A negative acknowledgement is achieved by sending a NAK, a positive acknowledgement is sent as an ACK0 or ACK1 for even and odd blocks respectively. The acknowledgement is sent after one or more Block Check Characters (BCCs) have been received and checked (one character for LRC-8, two characters for CRC-12 or CRC-16). Table 1 presents error checking requirements for byte controlled protocols.

For control and acknowledgement messages the receiving processor must detect various single and two character sequences. These are defined in tables 2 and 3.

Table 1 ERROR CHECKING REQUIREMENTS FOR BISYNC/ANSI 3.28

Information Code	No Transparency	Transparency Operating	Transparency Not Operating
EBCDIC	CRC-16	CRC-16	CRC-16
ASCII	VRC-LRC	CRC-16	VRC-CRC-16
SBT	CRC-12	CRC-12	CRC-12

Table 2 COMMUNICATION CONTROL CHARACTERS FOR BISYNC

Mnemonic	Name	Function
SOH	Start of heading	Start of message which is used as heading.
STX	Start of text	Start of any message. Information code characters follow.
ETX	End of text	Signals the end of a text. BCC(s) follow.
ETB	End of transmittal block	Signals the end of a transmittal block. BCC(s) follow.
EOT	End of transmission	If used by the master, it signals the end of a transmission. As a slave response, it indicates an abnormal termination of the transmission (abort). In multipoint systems, it is used by the control station to activate address decoding functions within the tributary stations.
NAK	Negative acknowledgement	Signals back to the master station that the last data block was not accepted. It may also represent a negative response to an initialize sequence, i.e. not ready.
ENQ	Enquiry	Request to send back status, or abort a block of transmitted data. Also used by the master station to end a polling sequence.
ITB	Intermediate block	Blocks of the received message are released to the program via intermediate interrupts for faster processing. BCC(s) follow the ITB.
DLE	Data link escape	Used as leader in control sequences (see table 3).
ACK	Acknowledgement	Used as DLE trailers in control sequences (see table 3).
SYN	Synchronization character	SYN-SYN establishes character synchronization. Inserted automatically into the data stream by the transmitter. Does not enter main storage of the receiver.

Table 3 BISYNC CONTROL CHARACTER SEQUENCES

Mnemonic	Function
DLE-RVI	Indicates to the transmitting station that the receiving station wants to transmit data. Implies acknowledgement of last received block.
DLE-SAK	Indicates to the transmitter that the last message was received free of errors, but the receiver cannot continue.
DLE-STX	Enters transparent text mode. Allows all 256 characters to be used as data.
DLE-EOT	Disconnect sequence on a switched network.
DLE-ETX	End-of-text signal in transparent mode. BCCs follow.
DLE-ETB	End-of-transmittal-block signal in transparent mode. BCCs follow.
DLE-ITB	Intermediate-block-checking signal in transparent text mode. BCCs follow.
DLE-0/1	Used as positive reply to even/odd blocks respectively.
DLE-ENQ	Aborts block of transparent data. BCCs do not follow.
SYN-SYN	Establishes character synchronization. Automatically inserted into the data stream during underrun in normal text mode. Used to maintain synchronization, and to recognize line interruptions. Does not enter main storage of receiver.
DLE-SYN	Automatically inserted into the data stream during underrun in transparent text mode. Used to maintain synchronization, and to recognize line interruptions. Does not enter main storage of receiver.
DLE-WBT	Signals to the transmitting station that the last block was received correctly, but the receiver cannot continue immediately because other operations have to be performed first.
STX-ENQ	Temporary text delay. Abort sequence used by the master station to announce an abnormal termination of the transmission.

Character Count Protocols

Digital Equipment Corporation's DDCMP and its associated versions used by Bell Labs are character count protocols. A character count specifies the number of data characters in the information field of a message: positional significance is used to identify control information in the header of the block which is verified by a separate cyclic redundancy check. There are three control characters in DDCMP (SOH, ENQ, DLE) - each identifies the start of a different type of message. Figure 4 depicts the DDCMP text message format.

A "go back N blocks" type of error control is used in this protocol. Up to 255 blocks may remain outstanding before an acknowledgement is required. This is achieved by separate 8-bit send and receive block counts. When an acknowledgement is sent the received block count indicates the number of message blocks correctly received. This is compared with the send block count. The difference, if any, is the number of blocks that must be retransmitted.

Bit Oriented Protocols

BOPs make use of only two or three specific control characters for operation of the data link. These characters are used to delimit the beginning (FLAG) and end (FLAG, ABORT, GA) of a message frame. Upon receipt of the opening FLAG, positional signficance is used to delineate the bit sequence that follows into prescribed fields, as shown in figure 5. These fields area address, control, information, and frame check sequence. The address, control, and frame check field are fixed length; the information field is variable and may be zero. Examples of BOPs are IBM's Synchronous Data Link Control (SDLC), ANSI's Advanced Data Communication Control Procedures (ADCCP), ISO's High-Level Data Link Control (HDLC), Burroughs' Data Link Control (BDLC), and various other protocols developed by computer mainframe manufacturers. All of the above mentioned protocols are similar and can be treated as subsets of ADCCP. BOPs also utilize a "go back N" type of error control.

2653 FUNCTIONS AND APPLICATIONS

BCC Accumulation

The primary function of the PGC is the accumulation of the BCC for character oriented protocol (BCP and CCP) messages. As described previously, there are four modes of BCC accumulation and each mode can select one of three generating polynomials to compute the BCC(s). The polynomials are $x^{16}+x^{15}+x^2+1$ (CRC-16), $x^{12}+x^3+x^2+x+1$ (CRC-12), and x^8+1 (LRC-8). The four accumulation modes are BISYNC normal, BISYNC transparent, automatic accumulate and single accumulate.

In **BISYNC normal** mode, all characters loaded into the PGC's character register are accumulated except those in the SYN/Not Included class. During receive operations, a detected block terminating character (BTC) will cause the BCC accumulation to stop after the next one (LRC-8) or two (CRC-12 or CRC-16)

DDCMP MESSAGE FORMAT

SYN	SYN	SOH	Count (14 bits)	Flags (2 bits)	Response (8 bits)	Sequence (8 bits)	Address (8 bits)	CRC-16 (16 bits)	Information (any number of 8 bit characters)	CRC-16 (16 bits)

Figure 4

BIT ORIENTED PROTOCOL (BOP) MESSAGE FORMAT

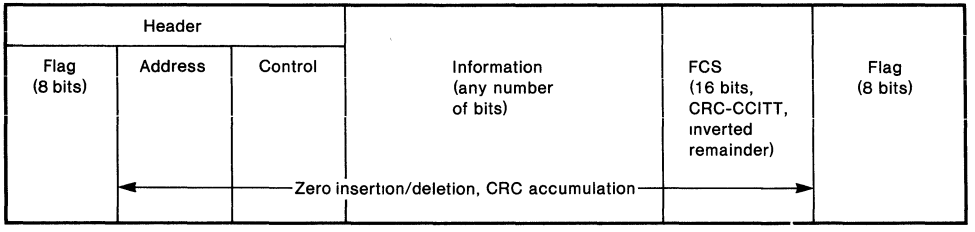


Figure 5

characters have been accumulated. At that time, if the BCC accumulation does not equal zero there has been a block check error. The BCC error bit will be set and an interrupt generated if the corresponding mask bit was enabled. In transmit mode, the BCC accumulation is automatically stopped once the BTC character has been accumulated. The CPU must read the BCC upper and BCC lower (for CRC-12 or CRC-16 only) register(s) and transmit them to the R/T or parallel peripheral. Since the accumulation has been stopped, the transfer of the first BCC to the R/T will not effect BCC lower. This assures that the second BCC will be correct when it is read by the CPU.

Note that BCCs are not checked against the character class array nor are they compared to the DLE ROM. This prevents false character detections when transmitting or receiving BCCs.

Second search character (SSC) detection is enabled in BISYNC normal allowing a two character communication control sequence such as DLE-STX to be detected.

In **BISYNC transparent** mode characters excluded from the BCC accumulation are the first DLE of a DLE-DLE pair, the DLE of a DLE-BTC pair, or DLE-SYN sequences (the SYN is also excluded).

In receive and transmit modes, the termination of BCC accumulation works exactly as in BISYNC normal, except that the BTC must be immediately preceded by an odd number of DLEs to be properly identified.

Second search character detection is not enabled in BISYNC transparent since DLE-SSC sequences are only valid in BISYNC normal mode.

In **Automatic accumulate** mode all characters loaded into the character register are accumulated; BTC and SSC detection is enabled and the BCC accumulation is not automatically terminated. The CPU must use single accumulate mode to stop the accumulation. When in receive mode, the BCC error bit is set/reset after accumulating each character so that the CPU must examine this bit after the last character is accumulated.

Examples of use of the automatic accumulate mode are a system where the R/T (2651/2661) operates with DLE/SYN stripping or in support of character count protocols such as DDCMP.

In **Single accumulate** mode all characters are accumulated, but only after an accumulate command is given by the CPU. If not given, the BCC accumulation is stopped. Operation in this mode is otherwise identical to automatic accumulate. Single accumulate mode can be used to selectively accumulate characters under CPU control or to accumulate characters that were unintentionally excluded in one of the other modes.

Figures 6 and 7 illustrate the operation of the 2653 on various types of text and control messages.

Some Other Applications

The PGC can be employed in a variety of applications other than a dedicated BCC generator for a single channel. For example, it can be multiplexed among several data channels, used as a programmable character comparator or it can be used to check parity on a system address or data bus. A brief description of each of these applications is given below.

a. MULTIPLEXED PGC

One PGC may be time-shared among a few R/T's if the CPU saves and restores the mode register and partial BCC result in the BCC registers. These registers are accessed via CE1. There must be separate save area for each R/T (serial channel) and a channel pointer indicating the last R/T that transferred or received a data character (see figure 8).

The loading of the BCC registers will clear SRO-SR3 and all previously detected special characters, i.e., DLE, BTC/SC, BCC (BISYNC modes). The BCC accumulation will start again when the next character is loaded into the character register in all accumulation modes except single. That mode requires a start accumulation command.

b. CHARACTER COMPARATOR

The PGC can be used as a programmable data bus character comparator which monitors data bus character transfers (CPU to peripheral, CPU to CPU, CPU to memory, memory to peripheral via DMA). The user selectively loads the character class array with BTC/SC and SSC characters to be compared. Status bits will be set and an interrupt can be generated upon SC and DLE-SSC detection. A match on one to 128 different characters or DLE-SSC sequences can be programmed.

Figure 9 depicts an arrangement where the DMA controller or slave CPU handles data bus transfers, the PGC interrogates the data bus, and the host CPU responds to PGC interrupts.

c. BUS PARITY CHECKER

The PGC can be used to check the parity of transactions on a system's data bus. The processor first writes control information into the PGC via the CE1 pin. All other bus operations are then checked for parity with external address decoding used to generate an active low CE0. Bus parity checking is useful in data transfers between CPU and peripherals or memory and CPU. Some computers check parity on both halves of a 16-bit word during all system bus transfers.

MULTI-PROTOCOL SYNCHRONOUS CHIP SET

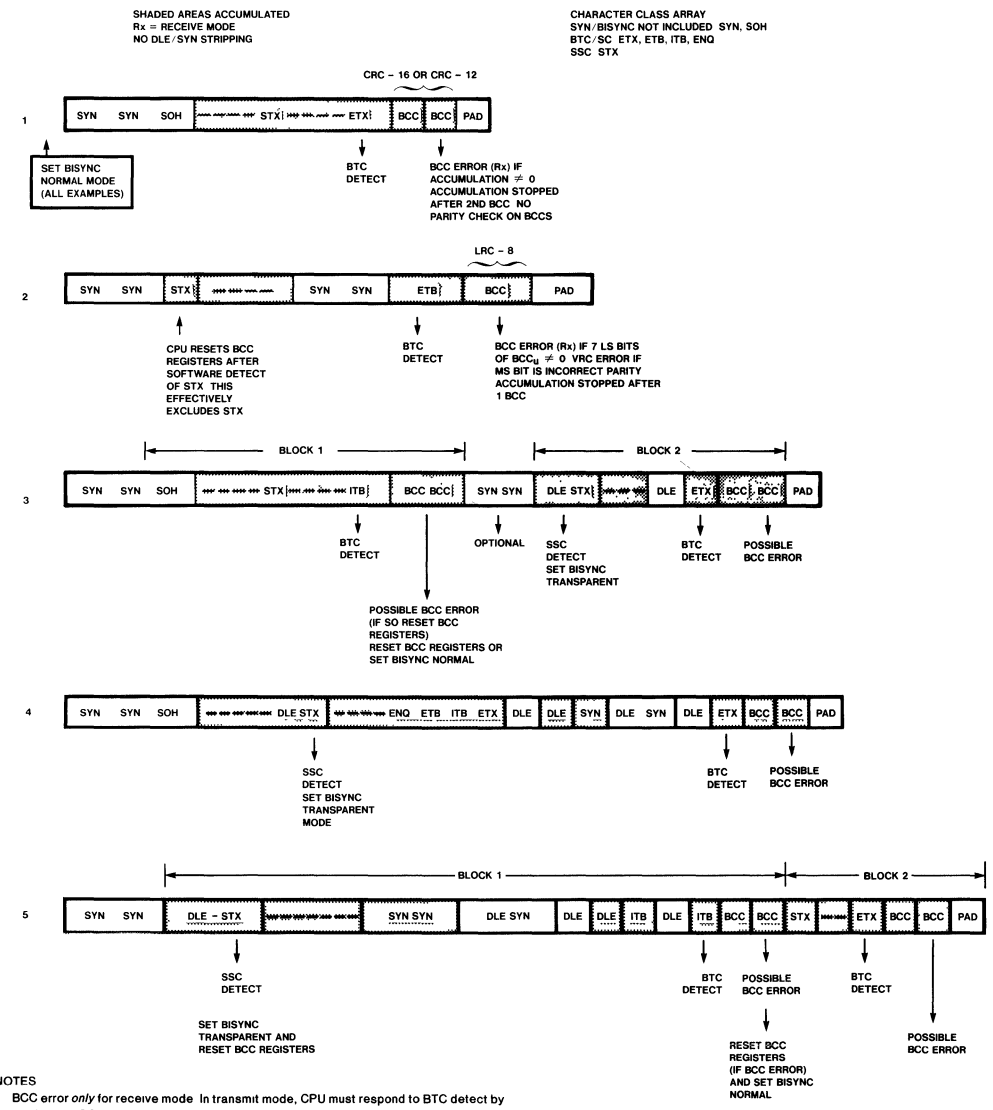
The Signetics 2652 Multi-Protocol Communications Controller (2652), originally targeted for bit oriented protocols and DDCMP, can send and receive EBCDIC, ASCII, and SBT data. However, the 2652 doesn't support many of the functions of byte controlled protocols. In particular, the 2652 has no way of knowing which characters to include or exclude in the BCC accumulation. This makes the on board CRC-16 generator/checker useless for BISYNC. Furthermore, there are no provisions in the 2652 for transparent mode DLE handling, special character detection or two character sequence detection. But the PGC encompasses all of these missing functions! Thus, the 2652 - 2653 combination can totally support character controlled protocols as well as bit oriented and character count disciplines. The PGC can be used for single character compares in SDLC/HDLC or DDCMP applications to reduce software overhead.

As shown in figure 10, only a single inverter is required to interface the 2652 and 2653 such that 2652 data bus transfers are monitored.

A BISYNC/ASYNC CHIP SET

Although the 2653 complements any R/T in the support of character controlled protocols it is optimized for use with the Signetics 2661 Enhanced Programmable Communications Interface (EPCI). That device is a USART with on chip baud rate generator that has special features for BISYNC. There are two loadable SYN

EXAMPLES — BISYNC TEXT MESSAGE BCC ACCUMULATION

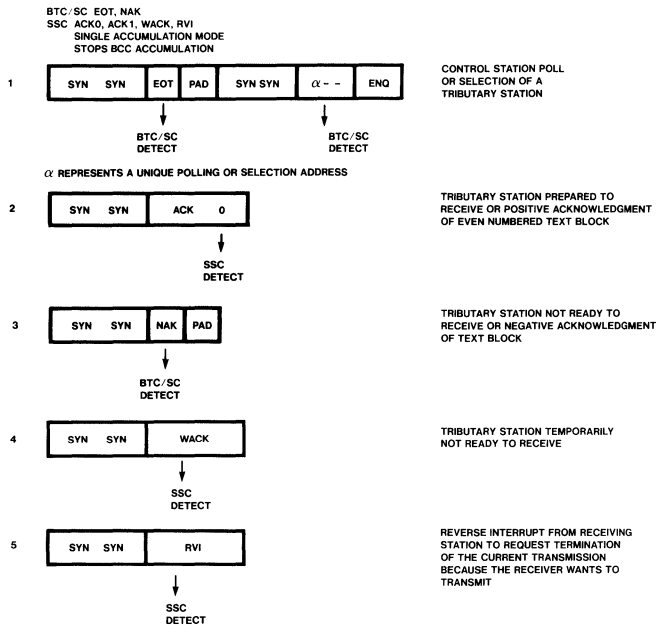


NOTES

1 BCC error *only* for receive mode In transmit mode, CPU must respond to BTC detect by reading the BCC register(s) and sending them to the R/T The accumulation is stopped after the BTC is accumulated
2 ENQ (DLE-ENQ) in a text message should be treated as an abort
3 Opening SYNs may be stripped by the R/T
4 The single accumulate mode and command can be used to accumulate a character that inadvertently was excluded (For example, the DLE of a DLE-STX if the PGC was in transparent mode and there was not a line turnaround prior to the DLE) The single accumulation should be done using $\overline{CE1}$ after the BCC(s) have been accumulated

Figure 6

EXAMPLES — BISYNC CONTROL MESSAGES



NOTES
1 BCC accumulation should be ignored for control messages This can be effected by single accumulate mode without single accumulate commands
2 Characters programmed as SSCs should be the binary equivalent of the second character of the DLE-SSC sequence

Figure 7

registers and a loadable DLE Register in the EPCI. Figure 11 is a schematic showing the 2653 and 2661 interfaced to an 8-bit CPU.

A transparent operating mode causes the EPCI to automatically change the detected synchronization sequence and underrun linefill from SYN-SYN to DLE-SYN. This is necessary to prevent an unrecoverable problem at the receiver. If a USART sent or received the normal mode SYN-SYN sequence it would be interpreted as transparent data rather than actual synchronization information.

Another transparent mode function is detecting and stripping received DLE's. Normally a software job, this task is completely and properly handled by the 2661. The DLE Detect status bit is even automatically reset at the proper time.

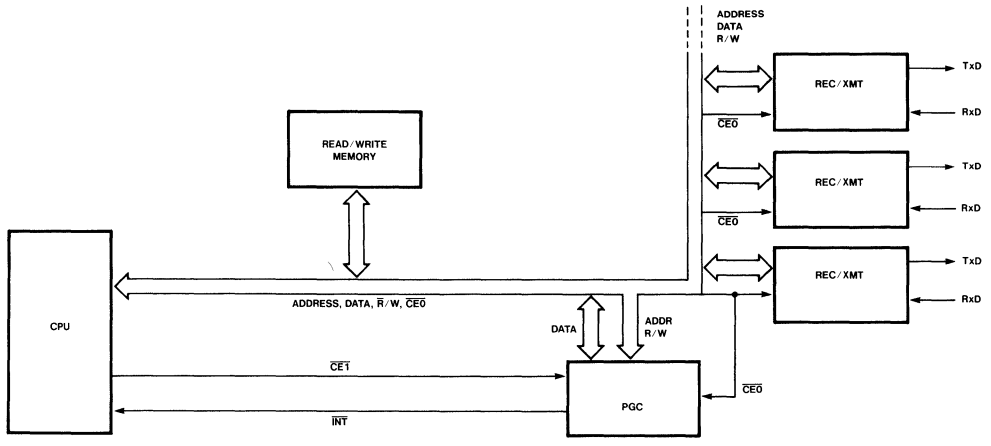
A Send DLE command in the 2661's transmitter can be used to prevent a possible underrun between the DLE and a subsequent control character. Such an underrun would cause an incorrect control sequence to be transmitted. For example, consider an underrun between a DLE-STX, the sequence used to enter transparent mode. The transmitted sequence becomes DLE-SYN-SYN-STX. But a DLE-SYN is illegal unless transparent mode has been entered. Furthermore, the STX would set normal text mode not transparent mode.

FLOW CHARTS FOR BISYNC OPERATION

Figures 12 through 15 illustrate functional flow charts for the operation of the 2653 - 2661 pair in BISYNC. The intent of these flow charts is to illustrate the procedures required when receiving and transmitting BISYNC text messages in both normal and transparent modes of operation It is not implied that the actual software program to handle these tasks necessarily follow the flow charts step by step. In an actual application, an interrupt driven structure would be more appropriate. Assumptions are half-duplex operation (normal for the BISYNC protocol) and use of the EBCDIC code.

The receive flow, figure 12, starts with initialization of the PGC and EPCI for the normal mode Modem handshaking is then performed. Upon detection of carrier, indicated by assertion of the 2661's DCD status bit, the receiver is enabled, the PGC is setup for receive, and miscellaneous flags are reset. Data is then read from the 2661 receive holding register and acted upon according to the BISYNC protocol The

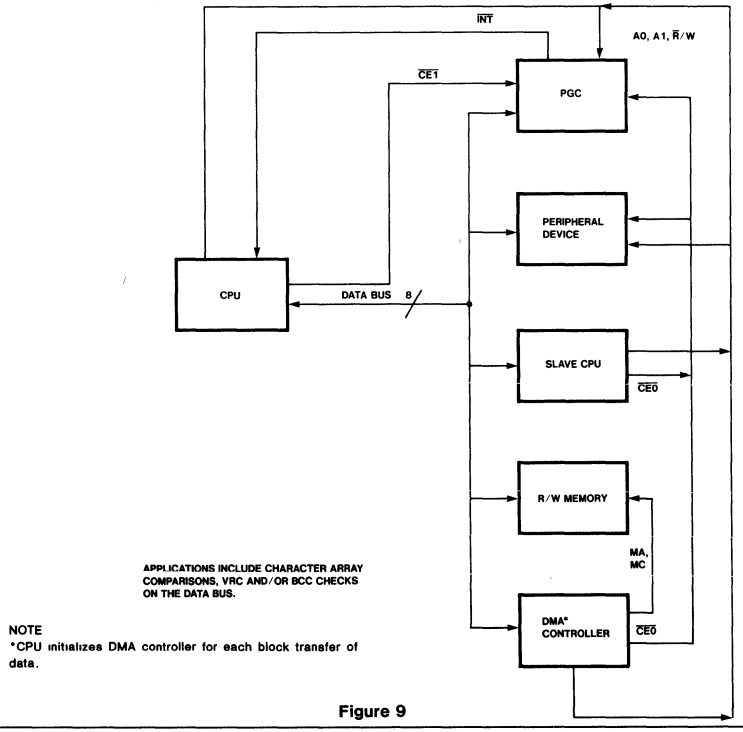
PGC SERVICES MULTIPLE RECEIVERS/TRANSMITTERS



ONE PGC IS TIME-SHARED BY THREE R/Ts
THE CPU READS AND RESTORES THE PARTIAL BCC REMAINDER FOR EACH SERIAL CHANNEL

Figure 8

PGC DATA BUS MONITORING WITH DMA TRANSFERS



APPLICATIONS INCLUDE CHARACTER ARRAY COMPARISONS, VRC AND/OR BCC CHECKS ON THE DATA BUS.

NOTE
*CPU initializes DMA controller for each block transfer of data.

Figure 9

2652/2653 INTERFACE
TYPICAL PROTOCOLS: BISYNC, DDCMP, SDLC, HDLC

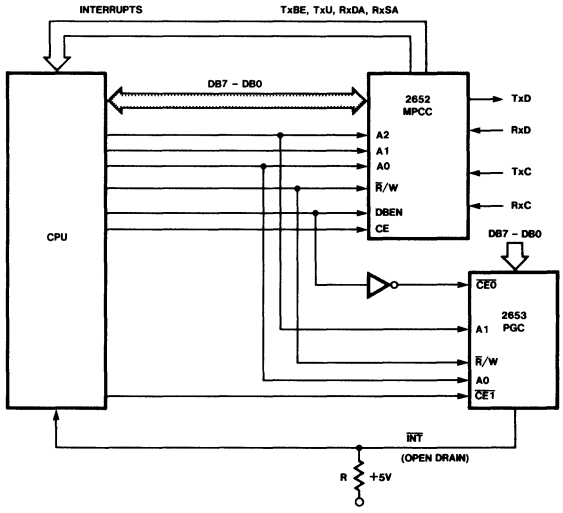


Figure 10

2651 OR 2661/2653 INTERFACE

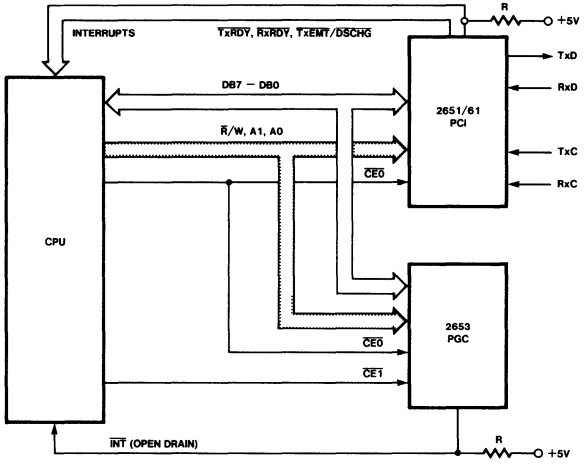


Figure 11

PGC status flags are utilized to determine if and when the transmission switches to transparent mode, and to determine the receipt of a block terminating character (BTC). The two characters following the BTC are the Block Check Character. After these are received, the PGC status register is examined to determine if a BCC error has occured.

The data stored in the buffer will be stripped of all sync characters. DLEs are not stripped. Although the 2661 includes a DLE stripping capability, this feature is not employed because the DLEs must be 'seen' by the PGC in order for it to accumulate the BCC correctly. The CPU must remove the extraneous DLEs which may be imbedded in a transparent block of text.

The transmit flow chart, figure 13, operates on a block of data placed in a buffer area by the controlling CPU. This data must include the SYNs to be sent at the initiation of transmission and the DLEs that form part of a two character control sequence. DLEs in a transparent block of text need not be doubled up - the EPCI will automatically add a DLE if one is loaded into its THR while operating in transparent mode. A character counter assists the software to determine when a DLE is really part of a BTC (in transparent mode).

After initialization of the PGC and EPCI and establishment of the modem connection, the data is pulled from the buffer and transmitted. If a DLE is detected in the data stream, and that character is part of a two character control sequence, the 'send DLE' feature of the PCI is used to avoid underrun between the two characters. Since the DLE is not transferred to the EPCI via the data bus, this requires that an extra DLE be accumulated in the PGC. This is done by use of the PGC's capability to accumulate characters loaded via CE1. When a BTC is detected by the PGC, the two BCC characters are read from the BCC registers and transferred to the EPCI for transmission.

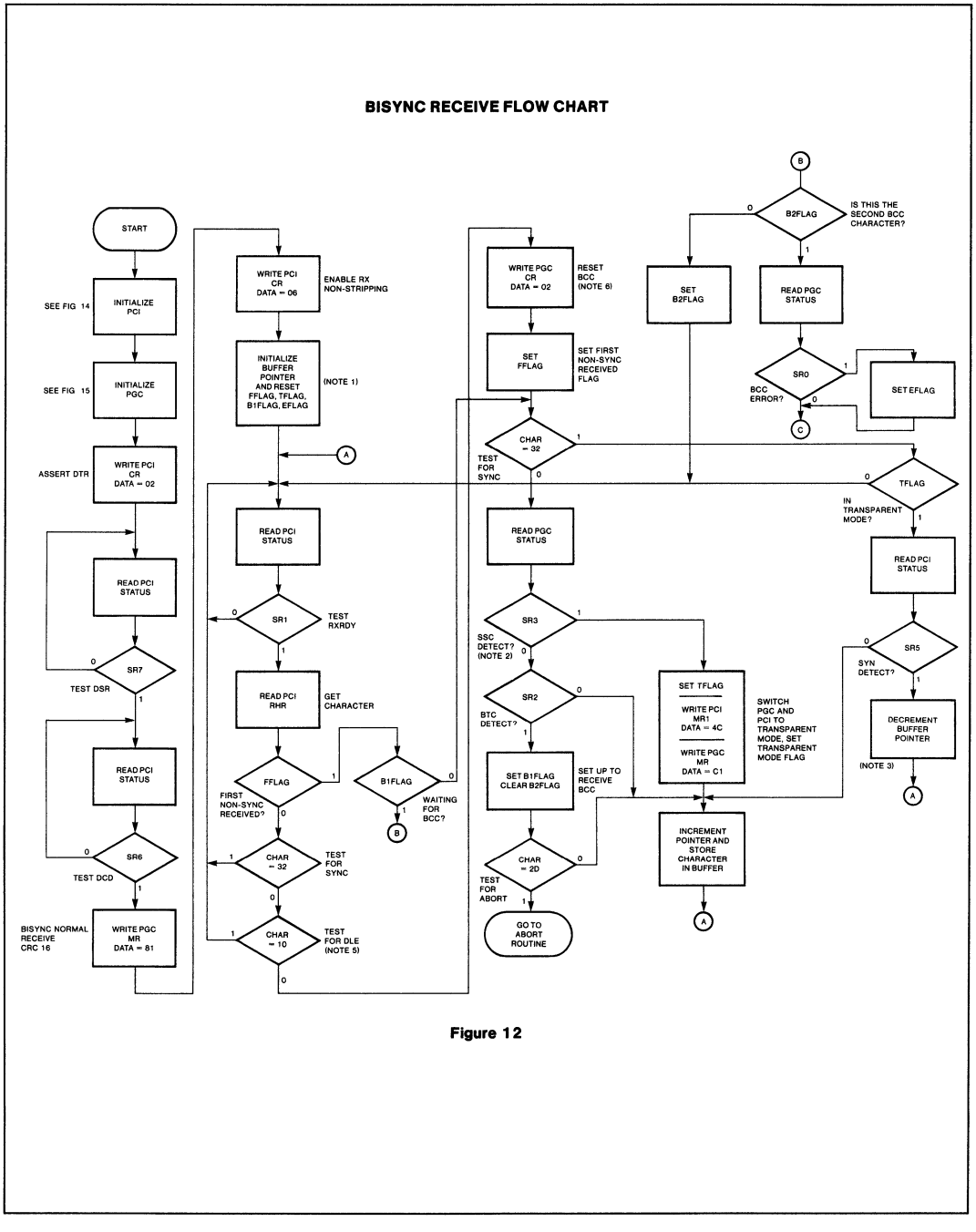
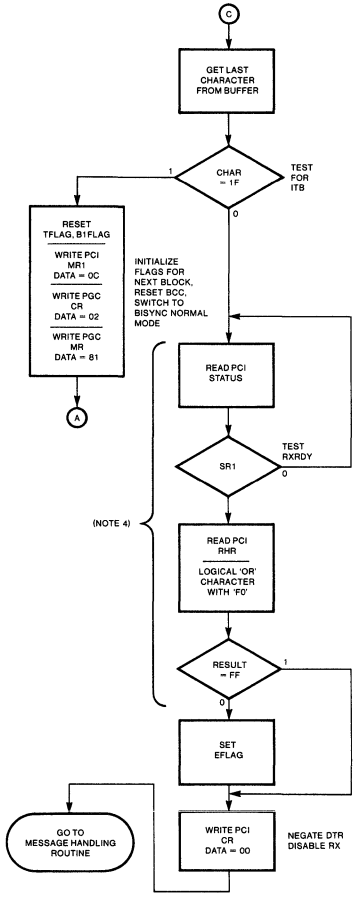

BISYNC RECEIVE FLOW CHART
START
SEE FIG 14
INITIALIZE PCI
SEE FIG 15
INITIALIZE PGC
ASSERT DTR
WRITE PCI CR DATA = 02
READ PCI STATUS
SR7
TEST DSR
READ PCI STATUS
SR6
TEST DCD
BISYNC NORMAL RECEIVE CRC 16
WRITE PGC MR DATA = 81
WRITE PCI CR DATA = 06
ENABLE RX NON-STRIPPING
INITIALIZE BUFFER POINTER AND RESET FFLAG, TFLAG, B1FLAG, EFLAG
(NOTE 1)
A
READ PCI STATUS
SR1
TEST RXRDY
READ PCI RHR
GET CHARACTER
FFLAG
FIRST NON-SYNC RECEIVED?
B1FLAG
WAITING FOR BCC?
B
CHAR = 32
TEST FOR SYNC
CHAR = 10
TEST FOR DLE (NOTE 5)
WRITE PGC CR DATA = 02
RESET BCC (NOTE 6)
SET FFLAG
SET FIRST NON-SYNC RECEIVED FLAG
CHAR = 32
TEST FOR SYNC
READ PGC STATUS
SR3
SSC DETECT? (NOTE 2)
SR2
BTC DETECT?
SET B1FLAG CLEAR B2FLAG
SET UP TO RECEIVE BCC
CHAR = 2D
TEST FOR ABORT
GO TO ABORT ROUTINE
B
B2FLAG
IS THIS THE SECOND BCC CHARACTER?
SET B2FLAG
READ PGC STATUS
SR0
BCC ERROR?
C
SET EFLAG
TFLAG
IN TRANSPARENT MODE?
SET TFLAG
WRITE PCI MR1 DATA = 4C
WRITE PGC MR DATA = C1
SWITCH PGC AND PCI TO TRANSPARENT MODE, SET TRANSPARENT MODE FLAG
INCREMENT POINTER AND STORE CHARACTER IN BUFFER
A
READ PCI STATUS
SR5
SYN DETECT?
DECREMENT BUFFER POINTER
(NOTE 3)
A

Figure 12

BISYNC RECEIVE FLOW CHART CONTINUED



BISYNC RECEIVE FLOW CHART NOTES

1 FFLAG = the first non-sync character has been received

TFLAG = operating in transparent mode

EFLAG = BCC or PAD error

B1FLAG = Received block terminating character (BTC) Awaiting BCC

B2FLAG = Received first BCC character Awaiting second BCC

2 SSC detect is disabled by PGC while in transparent mode

3 Pointer is decremented to overwrite previously stored 'DLE' which was part of a 'DLE-SYN' line fill

4 Test for closing PAD of at least four ones at end of message

5 If first non-sync character is a 'DLE', the message will start with 'DLE-STX' (transparent mode) FFLAG is not set in this case since both these characters are excluded from the accumulation

6 First non-sync character of a new message, or first two if message starts in transparent mode, are excluded from the BCC accumulation

Figure 12 continued

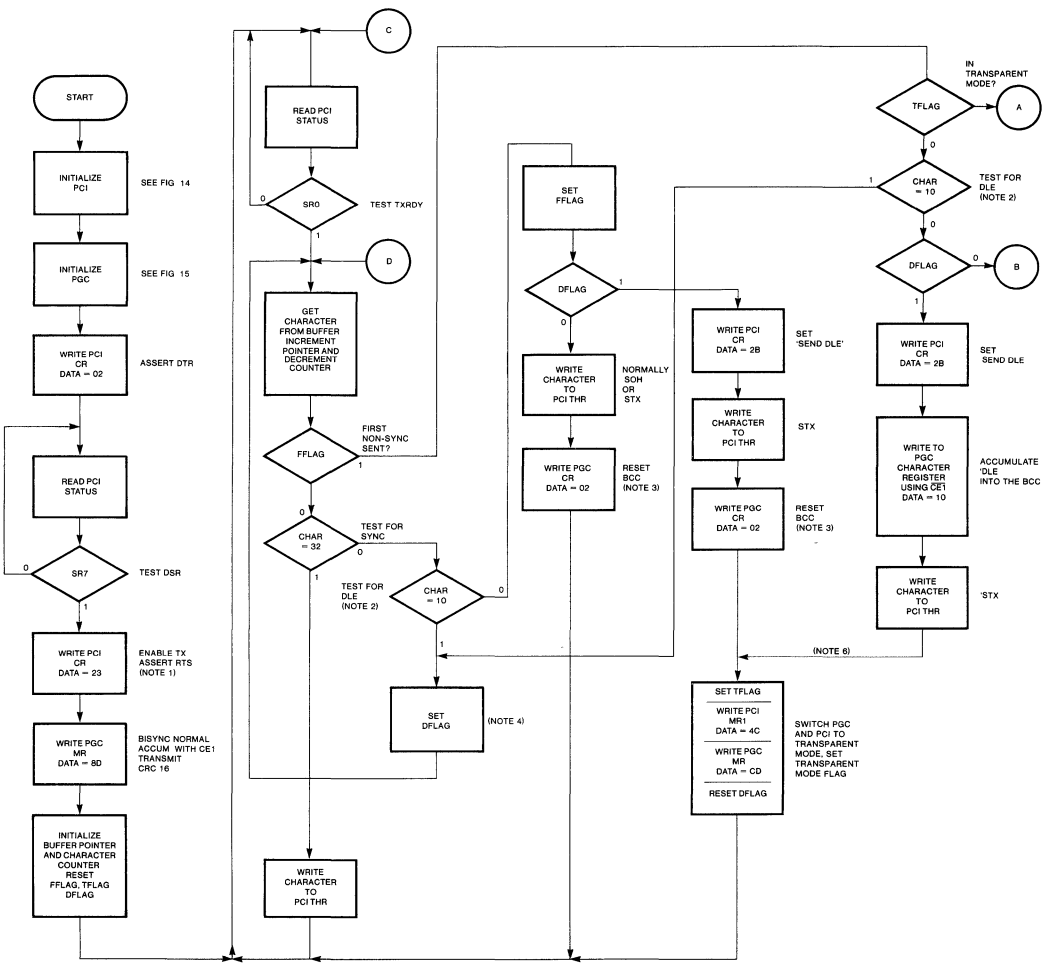
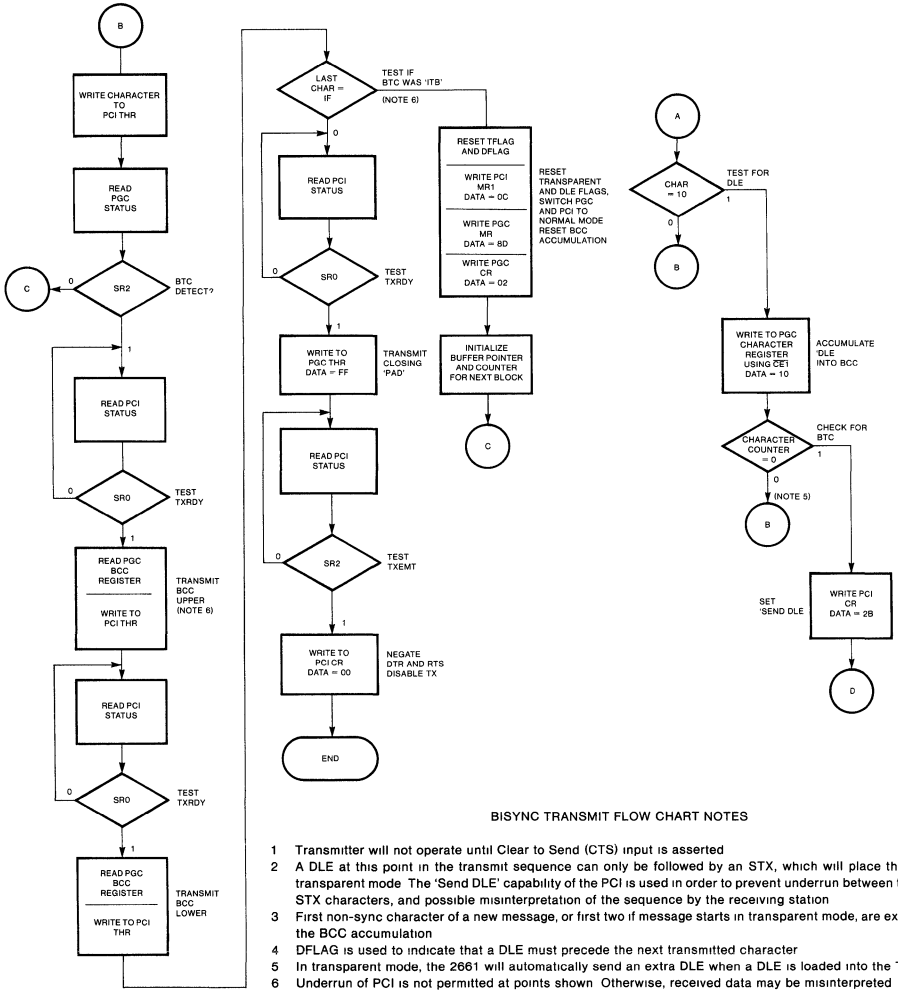

BISYNC TRANSMIT FLOW CHART
START
INITIALIZE PCI
SEE FIG 14
INITIALIZE PGC
SEE FIG 15
WRITE PCI CR DATA = 02
ASSERT DTR
READ PCI STATUS
SR7
TEST DSR
WRITE PCI CR DATA = 23
ENABLE TX ASSERT RTS (NOTE 1)
WRITE PGC MR DATA = 8D
BISYNC NORMAL ACCUM. WITH CE1 TRANSMIT CRC 16
INITIALIZE BUFFER POINTER AND CHARACTER COUNTER RESET FFLAG, TFLAG DFLAG
C
READ PCI STATUS
SR0
TEST TXRDY
D
GET CHARACTER FROM BUFFER INCREMENT POINTER AND DECREMENT COUNTER
FFLAG
FIRST NON-SYNC SENT?
CHAR = 32
TEST FOR SYNC
TEST FOR DLE (NOTE 2)
CHAR = 10
SET DFLAG
(NOTE 4)
WRITE CHARACTER TO PCI THR
SET FFLAG
DFLAG
WRITE CHARACTER TO PCI THR
NORMALLY SOH OR STX
WRITE PGC CR DATA = 02
RESET BCC (NOTE 3)
IN TRANSPARENT MODE?
TFLAG
A
CHAR = 10
TEST FOR DLE (NOTE 2)
DFLAG
B
WRITE PCI CR DATA = 2B
SET SEND DLE
WRITE TO PGC CHARACTER REGISTER USING CE1 DATA = 10
ACCUMULATE DLE INTO THE BCC
WRITE CHARACTER TO PCI THR
STX
WRITE PCI CR DATA = 2B
SET 'SEND DLE'
WRITE CHARACTER TO PCI THR
STX
WRITE PGC CR DATA = 02
RESET BCC (NOTE 3)
(NOTE 6)
SET TFLAG
WRITE PCI MR1 DATA = 4C
WRITE PGC MR DATA = CD
RESET DFLAG
SWITCH PGC AND PCI TO TRANSPARENT MODE, SET TRANSPARENT MODE FLAG

Figure 13

BISYNC TRANSMIT FLOW CHART CONTINUED



BISYNC TRANSMIT FLOW CHART NOTES

1 Transmitter will not operate until Clear to Send (CTS) input is asserted
2 A DLE at this point in the transmit sequence can only be followed by an STX, which will place the system in transparent mode The 'Send DLE' capability of the PCI is used in order to prevent underrun between the DLE and STX characters, and possible misinterpretation of the sequence by the receiving station
3 First non-sync character of a new message, or first two if message starts in transparent mode, are excluded from the BCC accumulation
4 DFLAG is used to indicate that a DLE must precede the next transmitted character
5 In transparent mode, the 2661 will automatically send an extra DLE when a DLE is loaded into the THR
6 Underrun of PCI is not permitted at points shown Otherwise, received data may be misinterpreted

Figure 13 continued

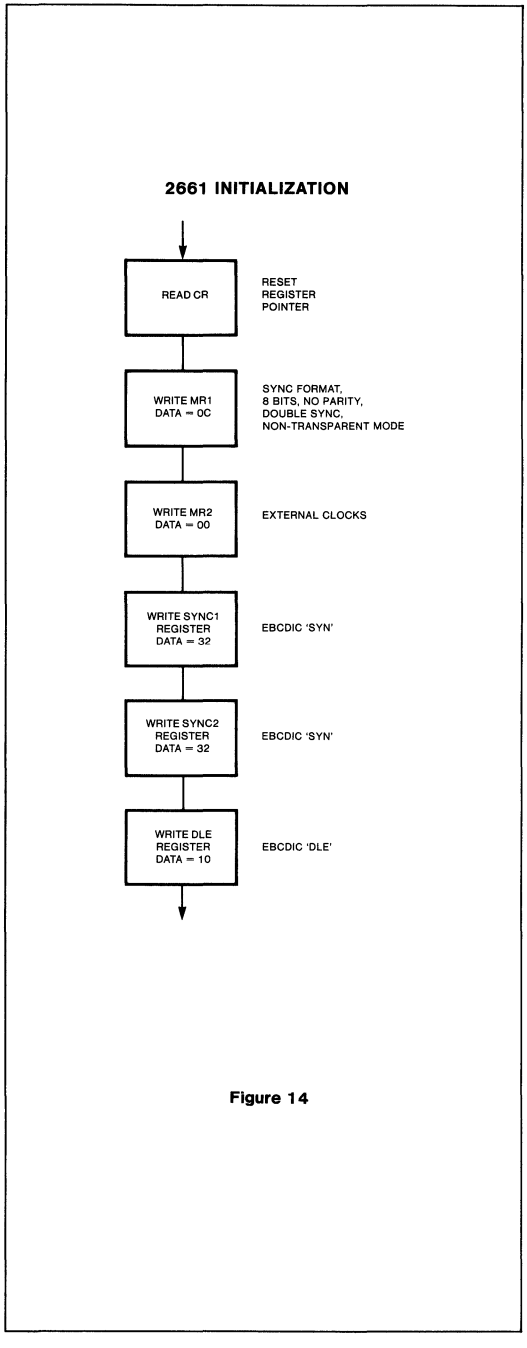


Figure 14

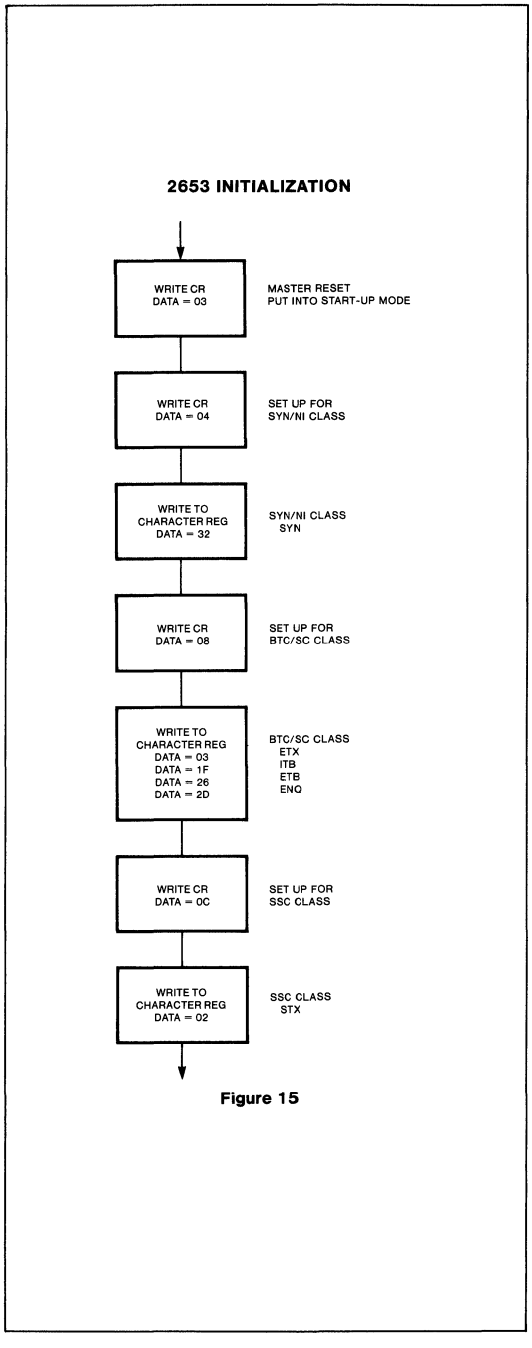


Figure 15

USING THE 2670/71/72/73 CRT TERMINAL CHIP SET App Note 401

INTRODUCTION

Microprocessors and LSI have had a dramatic impact on the implementation and capabilities of alphanumeric CRT terminals. The first generation of CRT terminals were little more than 'glass teletypes'. Current designs, implemented with microprocessors, are characterized by an abundance of sophisticated features that were previously not economically feasible: a universal hardware design that can adapt to different user requirements simply by changing software or firmware; programmability to provide end users with the flexibility to execute specialized routines; and local intelligence and storage which off-loads the host CPU by permitting data manipulation and verification at the terminal site.

Just as the impact of microcomputers has been felt in the functional capabilities of terminals, advances in semiconductor technology have revolutionized the hardware implementation. Designs that previously consisted of 100 to 200 ICs can now be realized with a few dozen MSI and LSI devices. The majority of the LSI manufacturers' effort with respect to CRT terminals has been concentrated in the 'CRT controller' area. These circuits provide the character timing, display addressing, and sync generation functions required by all terminals. However, these controllers need to be supported by many other external circuits to implement a complete terminal.

The purpose of this application note is to provide information on the use of four new Signetics CRT terminal products which, when combined with standard CPUs, memories, and TTL, allow the implementation of a wide spectrum of CRT terminal capabilities in as few as 15 total packages. These devices are:

- 2670 Display Character and Graphics Generator (DCGG)
- 2671 Programmable Keyboard and Communications Controller (PKCC)
- 2672 Programmable Video Timing Controller (PVTC)
- 2673 Video and Attributes Controller (VAC)

MAJOR ELEMENTS OF A CRT TERMINAL

Figure 1 shows the major elements of a typical low-end microcomputer-based CRT terminal. In this system, the CPU examines inputs from the data communications line and the keyboard and places the data to be displayed in a display buffer memory, which is typically a RAM which holds the data for a single or multiple screenload (page) or for a single character row. High-end ('smart' and 'intelligent') terminals start with the same base, but append additional circuits to provide more features and capabilities. The following sections describe the functions of each of the major blocks.

Character Timing and Sync Generation

The major function of this block is to generate the horizontal and vertical timing signals required to produce the TV raster on the CRT monitor. Other functions include the generation of display memory addresses in synchronism with the monitor scan and in accordance with a defined screen format (characters per row, scan lines per row and rows per screen), generation of a cursor signal at the appropriate scan position, and generation of video blanking signals during retrace intervals.

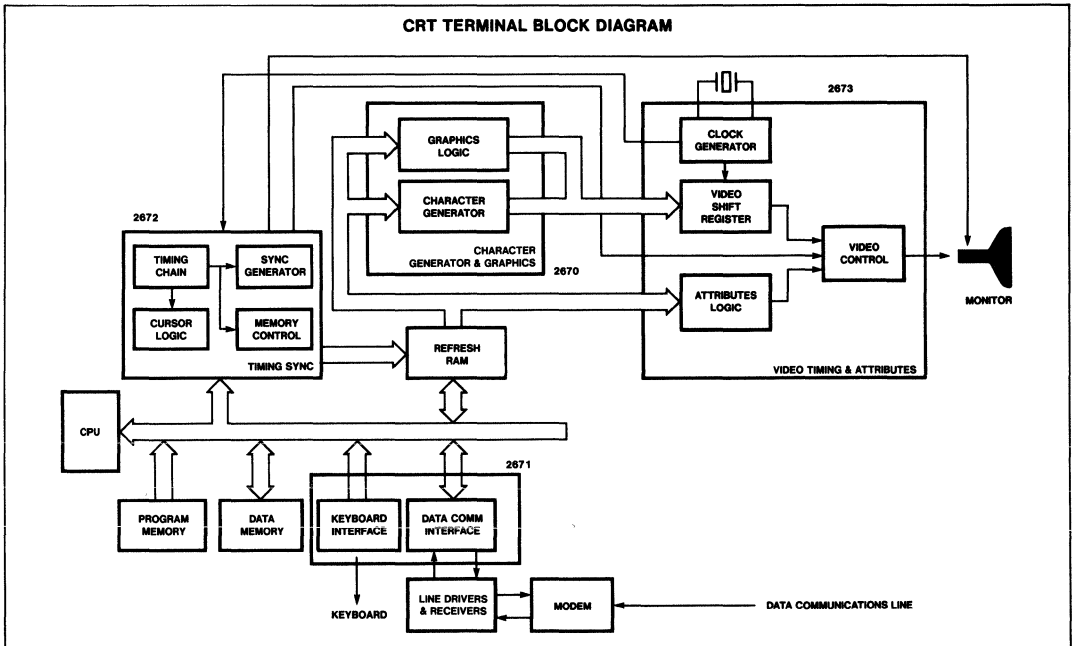


Figure 1

I/O Interface

In its simplest form, this block provides an interface to a keyboard to identify the key depressed and a serial communications link, normally operating in an asynchronous format, between the terminal and the host computer. Although these functions could be performed programmatically by the terminal CPU system, removing these functions to intelligent controllers unburden the system CPU and allow it to be used more effectively to provide additional features with a relatively small cost impact.

Character and Graphics Generation

These circuits convert the data stored in the display memory to the line by line dot patterns required to display the data on the CRT monitor.

Video Timing and Visual Attributes

This section contains the high speed (dot rate) circuits necessary to convert the parallel data from the character and graphics generation circuits to the serial video stream required by the CRT. Also included are circuits to sum visual display attributes such as blinking, high/low intensity, reverse video, and underlining into the video stream.

SIGNETICS' CRT CHIP SET

As mentioned previously, the Signetics CRT 'set' consists of four circuits. The functions of these circuits correspond closely to the four major CRT terminal blocks described above. The circuits have been partitioned so as to allow each to be used independent of the others, allow several alternative methods of implementing the display memory interface so that the hardware can be tailored to the system requirements, provide a full complement of programmable capabilities, and minimize the number of support circuits required.

The following sections give a brief description of each of the circuits. The reader is referred to the individual data sheets for full operational details.

2672 Programmable Video Timing Controller (PVTC)

The 2672 PVTC, figure 2, is a programmable device designed for use in CRT terminals and display systems that employ raster scan techniques. The PVTC generates the vertical and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT monitor. Also, the 2672 provides consecutive addressing to a user specified display buffer memory domain and controls the CPU-display buffer interface for various buffer configuration modes. A variety of operating modes, display formats, and timing profiles can be implemented by programming the control registers in the PVTC.

The CPU initializes the 2672 control and timing registers for the desired timing profiles and memory configuration. The PVTC provides the handshake control for CPU access to the display buffer. One of four memory access modes may be programmed: independent mode, trans-

6

2672 PROGRAMMABLE VIDEO TIMING CONTROLLER

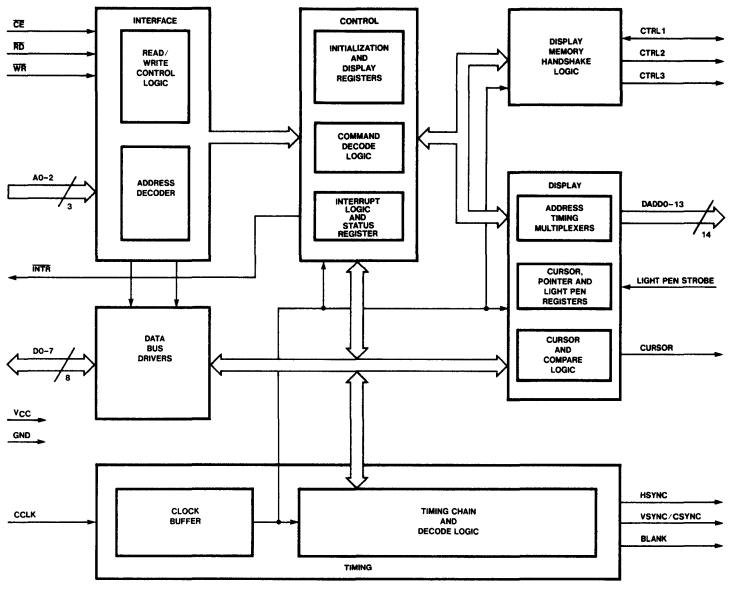


Figure 2

parent mode, shared mode, and row mode. These modes are described in the System Configurations section of this application note.

In all modes, the PVTC provides addresses for the display buffer which outputs the character codes to the 2670 Display Character and Graphics Generator (DCGG) and visual attribute codes to the 2673 Video Attributes Controller (VAC). The DCGG and PVTC supply the dot data and sync timing to the VAC which generates the serialized video.

Programmable features of the PVTC include screen format (characters/row, rows/screen, scan lines/row), horizontal and vertical timing parameters, cursor type (block or underline) and blink rate, character blink rate, interlaced or non-interlaced operation, and single or double height characters.

The PVTC is capable of producing interrupts based upon several internal conditions. By using these interrupts (or by polling the equivalent status register) display features such as non-consecutive buffer addressing for split screen operation, multiple cursors, horizontal and vertical scrolling, and smooth vertical scroll can be implemented.

2671 Programmable Keyboard and Communications Controller (PKCC)

The 2671, figure 3, is an MOS LSI device which provides a versatile keyboard interface and also functions as an asynchronous communications controller. It is intended for use in microprocessor based systems and provides an eight bit data bus interface.

The keyboard controller handles the scanning, debounce, and encoding of mechanical or capacitive keyboards with a maximum of 128 keys utilizing any of four programmable rollover modes. A mask programmable ROM provides four levels of key encoding, corresponding to the separate shift and control input combinations. An eight bit keyboard status register transmits status information to the CPU. Programmable features include rollover mode, scan rate and debounce time, coded or uncoded operation, and automatic repeat operation.

The communications section of the PKCC is a universal asynchronous receiver and transmitter (UART). The receiver accepts serial input data and converts it to parallel data characters. Simultaneously, the transmitter accepts parallel data from the CPU data bus and outputs it in serialized form. Received data is checked for parity and framing errors, and break conditions are flagged. Character lengths can be programmed as 5, 6, 7, or 8 bits not including parity, start or stop bits. An internal baud rate generator (BRG) operating from an external clock or directly from a crystal can be used to derive one of sixteen receive and/or transmit clocks. An eight bit communications status register provides status information to the CPU.

The PKCC has an interrupt mask register to selectively enable keyboard and communications status bits to generate interrupts. Priority encoded interrupt vectoring is available. Upon receipt of an interrupt acknowledge, a mask programmable interrupt vector will be output on the data bus reflecting the source of the interrupt. The mask enabled interrupt sources can also be read directly.

2670 Display Character and Graphics Generator (DCGG)

The DCGG, figure 4, is a mask-programmable 11,648-bit line select character generator. It contains 128 10x9 characters placed in a 10x16 matrix, and has the capability of shifting certain characters, such as j, y, g, p and q, that normally extend below the baseline; effectively, the 9 active lines are lowered within the matrix to compensate for the character's position.

Seven bits of an 8-bit address code are used to select 1 of the 128 available characters. The eighth bit functions as a chip enable signal. Each character is defined by a pattern of logic 1s and 0s stored in a 10x9 matrix. When a specific 4-bit binary line address code is applied, a word of 10 parallel bits appears to the output. The lines can be sequentially selected, providing a 9-word sequence of 10 parallel bits per word for each character selected by the address inputs. As the line address inputs are sequentially addressed, the device will automatically place the 10x9 character in 1 of 2 preprogrammed positions on the 16-line matrix with the positions defined by the 4-line address inputs. One or more of the 10 parallel outputs can be used as control signals to selectively enable functions such as half-dot shift, color selection, etc.

The 2670 DCGG includes latches to store the character address and line address data. A control input to inhibit character data output for certain groups of characters is also provided. The 2670 also includes a graphics capability, wherein the 8-bit character code is translated directly into 256 possible user programmable graphic patterns. Thus, the DCGG can generate data for 384 distinct patterns, of which 128 are defined by the mask programmable ROM.

2673 Video and Attributes Controller (VAC)

The 2673, figure 5, is a bipolar LSI device designed for CRT terminals and display systems that employ raster scan techniques. It contains a high speed video shift register, field and character attributes logic, attribute latch, cursor format logic and half dot shift control, and can be programmed for a light or dark screen background.

The VAC visual attribute capabilities are reverse video, character blank, blink, underline, highlight, and light pen strike-thru or, optionally, graphics. Each attribute has a separate control input which is latched internally when the AFLAG input is asserted. If the AMODE input is low, the attributes are valid for one character time. If AMODE is high, the attributes remain valid until the field is terminated by strobing in a new attributes set. The attributes are double buffered on a row by row basis internally so that field attributes can extend across character row boundaries thereby eliminating the necessity of starting each row with an attribute set

The horizontal dot frequency is the basic timing input element to the VAC; internally, this clock is divided down to provide a character clock output for system synchronization. Ten bits of dot data are parallel loaded into the video shift register on each character boundary. The video data is shifted out on three outputs at the dot frequency. On the video output, the video is presented as a three level signal representing low, medium and high intensities, and the three intensities are also encoded on the two TTL compatible video outputs.

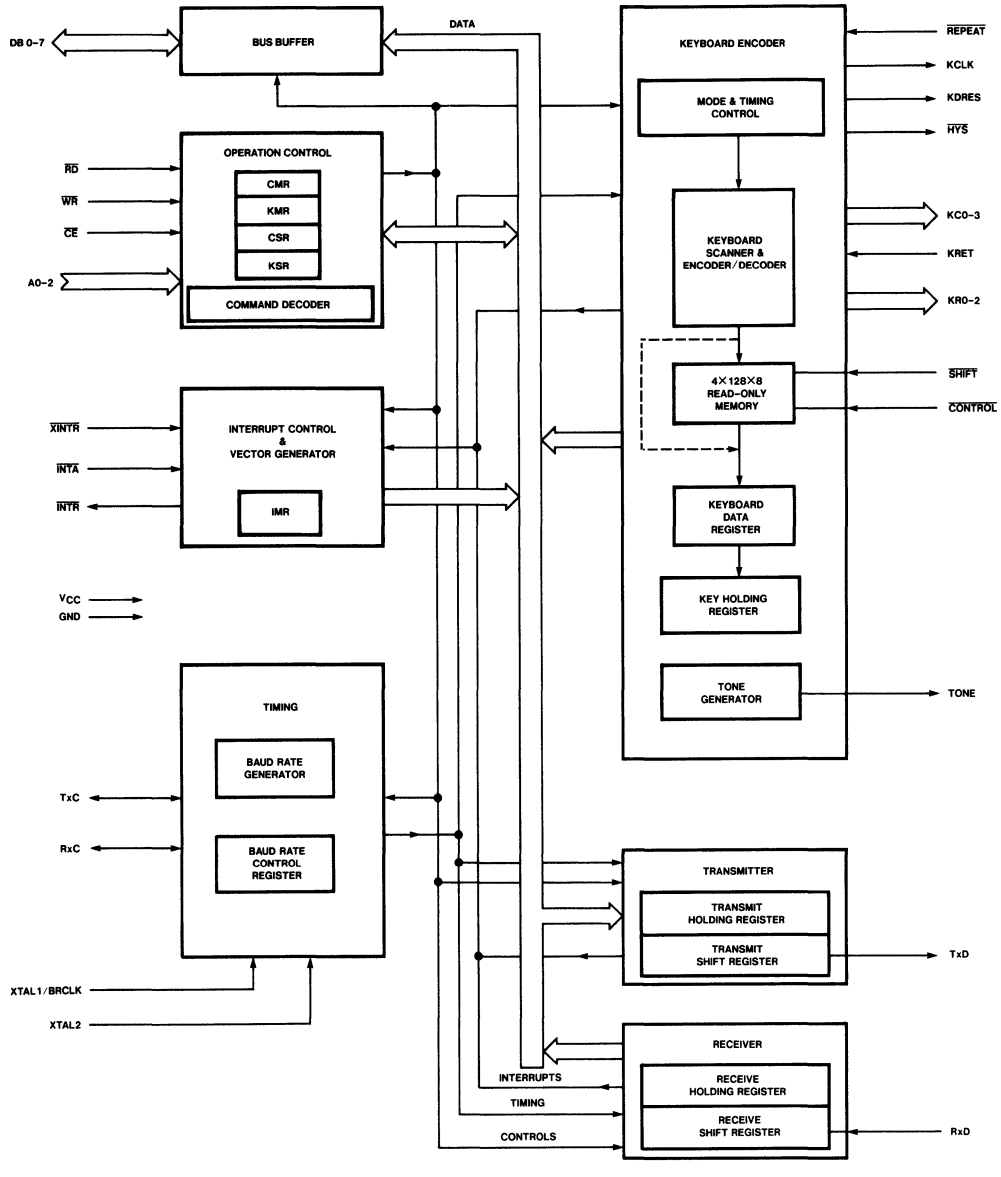

2671 PROGRAMMABLE KEYBOARD AND COMMUNICATIONS CONTROLLER
DB 0-7
BUS BUFFER
DATA
KEYBOARD ENCODER
REPEAT
KCLK
KDRES
HYS
MODE & TIMING CONTROL
OPERATION CONTROL
RD
WR
CE
A0-2
CMR
KMR
CSR
KSR
COMMAND DECODER
KEYBOARD SCANNER & ENCODER/DECODER
KC0-3
KRET
KR0-2
4X128X8 READ-ONLY MEMORY
SHIFT
CONTROL
XINTR
INTA
INTR
INTERRUPT CONTROL & VECTOR GENERATOR
IMR
KEYBOARD DATA REGISTER
KEY HOLDING REGISTER
VCC
GND
TONE GENERATOR
TONE
TIMING
BAUD RATE GENERATOR
TxC
RxC
BAUD RATE CONTROL REGISTER
TRANSMITTER
TRANSMIT HOLDING REGISTER
TRANSMIT SHIFT REGISTER
TxD
XTAL1/BRCLK
XTAL2
RECEIVER
RECEIVE HOLDING REGISTER
RECEIVE SHIFT REGISTER
RxD
INTERRUPTS
TIMING
CONTROLS

Figure 3

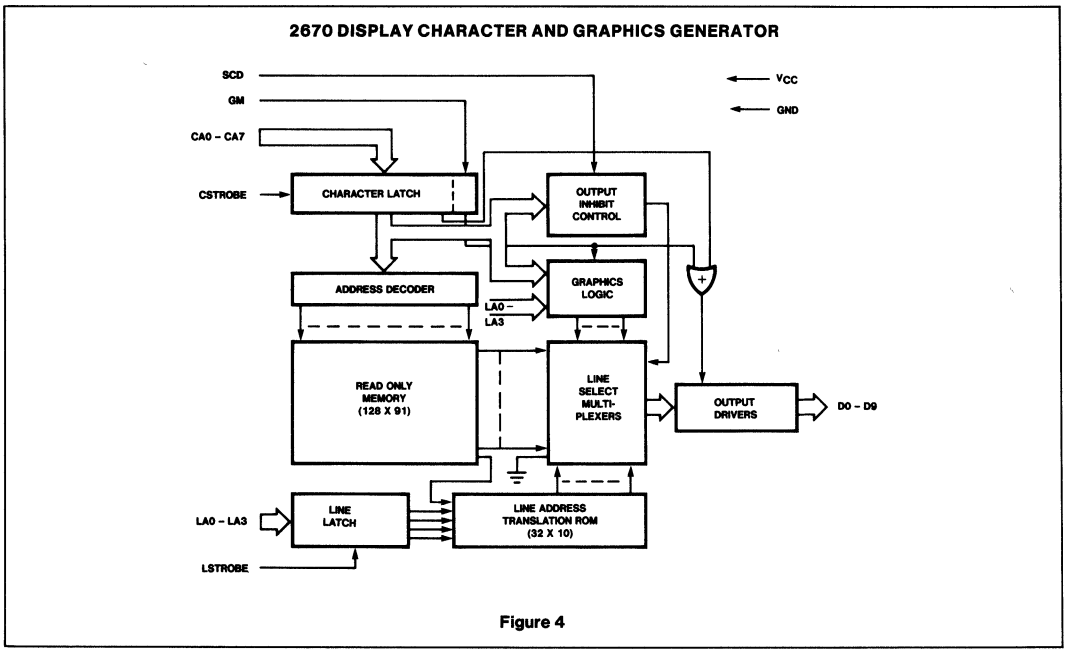


Figure 4

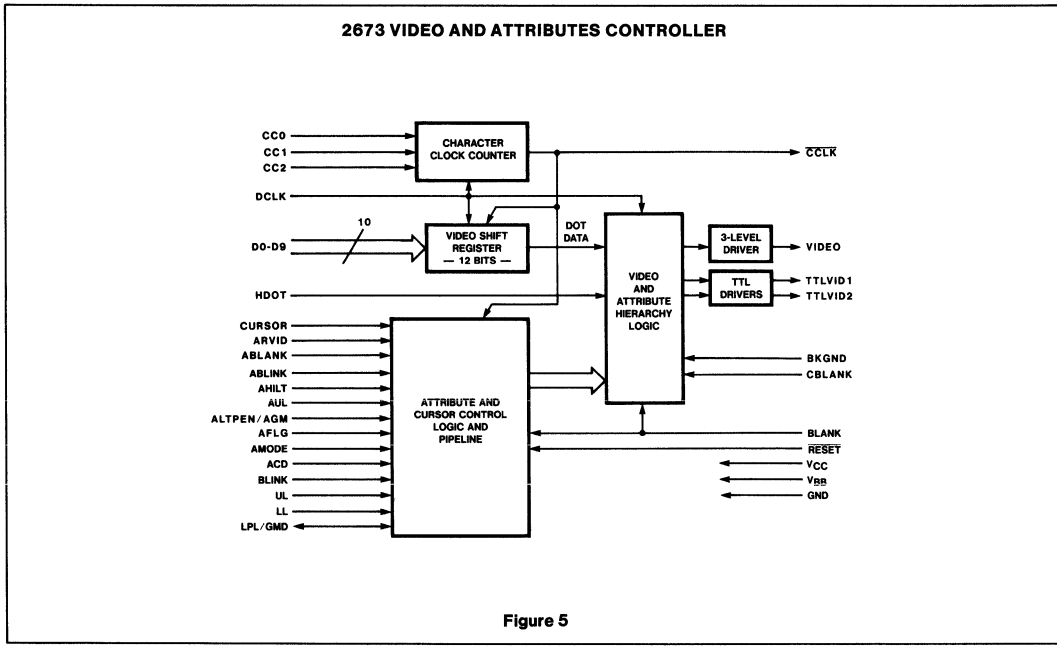


Figure 5

SYSTEM CONFIGURATIONS

The PVTC supports four common system configurations of display buffer memory interface, designated the independent, transparent, shared, and row buffer modes. The first three modes utilize a single or multiple page RAM and differ primarily in the means used to transfer display data between the RAM and the CPU. The row buffer mode makes use of a single row buffer (which can be a shift register or a small RAM) that is updated in real time to contain the appropriate display data.

Independent Mode

The CPU to RAM interface configuration for this mode is illustrated in figure 6. Transfer of data between the CPU and display memory is accomplished via a bidirectional latched port and is controlled by the PVTC signals read data buffer ($\overline{RDB}$), write data buffer ($\overline{WDB}$), and buffer chip enable ($\overline{BCE}$). This mode provides a non-contention type of operation that does not require address multiplexers. The CPU does not address the memory directly - the read or write operation is performed at the address contained in the cursor address register or the pointer address register as specified by the CPU. The PVTC enacts the data transfers during blanking intervals in order to prevent visual disturbances of the displayed data.

The CPU manages the data transfers by supplying commands to the PVTC. The commands used are:

1. Read/Write at pointer address.
2. Read/Write at cursor address (with optional increment of address).
3. Write from cursor address to pointer address.

The operational sequence for a write to memory operation is:

1. The CPU loads data to be written into the display memory into the interface latch.
2. The CPU writes the destination address into the PVTC's cursor or pointer registers.
3. The CPU checks the PVTC 'RDFLG' status bit to assure that any previous operation has been completed.
4. The CPU issues a 'write at cursor with/without increment' or a 'write at pointer' command to the PVTC.
5. The PVTC negates 'RDFLG', outputs the specified address, and generates control signals to perform requested operation. Data is copied from the interface latch into the memory.
6. The PVTC sets its 'RDFLG' status to indicate that the write operation is completed.

Similarly, a read operation proceeds as follows:

1. Steps 2 and 3 as above.
2. The CPU issues a 'read at cursor with/without increment' or 'read at pointer' command.
3. The PVTC negates 'RDFLG', outputs the specified address, and generates control signals to perform the read operation. Data is copied from the memory to the interface latch and the PVTC sets its 'RDFLG' status to indicate that the operation is completed.
4. The CPU checks the 'RDFLG' status to see if the read is completed.
5. The CPU reads the data from the interface latch.

Loading the same data into a block of display memory is accomplished via the 'write from cursor to pointer' command:

1. The CPU loads the data to be written into the display memory into the interface latch.
2. The CPU writes the beginning address of the memory block into the PVTC's cursor address register and the ending address of the block into the pointer address register.
3. The CPU checks the 'RDFLG' status bit to assure that any previous operation has been completed.
4. The CPU issues a 'write from cursor to pointer' command to the PVTC.

INDEPENDENT BUFFER MODE CONFIGURATION

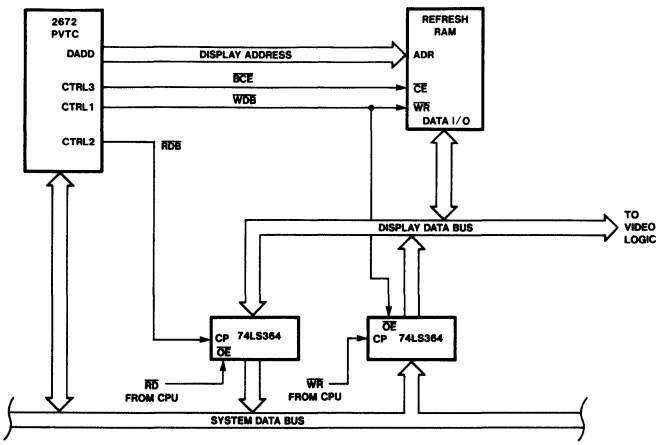


Figure 6

5. The PVTC negates 'RDFLG' and outputs block addresses and control signals to copy the data from the interface latch into the specified block of memory.
6. The PVTC sets its 'RDFLG' status to indicate that the block write is completed.

Similar sequences can be implemented on an interrupt driven basis using the READY interrupt output from the PVTC to inform the CPU that a previously requested command has been completed.

Two timing sequences are possible for the 'read/write at cursor/pointer' commands. If the command is given during the active display window (defined as first scan line of the first character row to the last scan line of the last character row), the operation takes place during the next horizontal blanking interval. If the command is given during the vertical blanking interval, or while the display has been commanded blanked, the operation takes place immediately.

For the 'write from cursor to pointer' operation, the PVTC's BLANK output is asserted automatically and remains asserted until the vertical retrace interval following completion of the command. The memory is filled at a rate of one location per two character times, plus a small amount of overhead.

Shared and Transparent Buffer Modes

In these modes the display buffer RAM is a part of the CPU memory domain and is addressed directly by the CPU. Both modes use the same hardware configuration with the CPU accessing the display buffer via three-state drivers (see figure 7). The processor bus request ($\overline{PBREQ}$) control signal informs the PVTC that the CPU is requesting access to the display buffer. In response to this request, the PVTC raises bus acknowledge ($\overline{BACK}$) until its bus external ($\overline{BEXT}$) output has freed the display address and data busses for CPU access. $\overline{BACK}$, which can be used as a 'hold' input to the CPU, is then lowered to indicate that the CPU can access the buffer.

In transparent mode, the PVTC delays the granting of the buffer to the CPU until a vertical or horizontal blanking interval, thereby causing minimum disturbance of the display. In shared mode, the PVTC will blank the display and grant immediate access to the CPU.

Row Buffer Mode

Figure 8 shows the hardware implementation for the row buffer mode. During the first scan line (line 0) of each character row, the PVTC halts the CPU and DMA's the next row of character data from the system memory to the row buffer memory. The PVTC then releases the CPU and displays the row buffer data for the programmed number of scan lines. The bus request ($\overline{BREQ}$) control signal informs the CPU that character addresses and the memory bus control (MBC) signal will start at the next falling edge of BLANK. The CPU must release the address and data busses before this time to prevent bus

PVTC SHARED OR TRANSPARENT BUFFER MODES

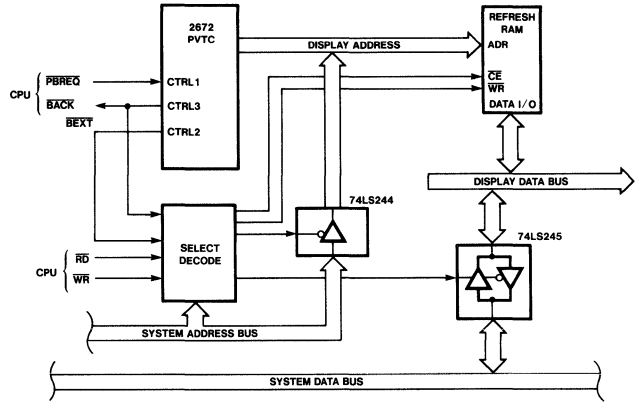


Figure 7

ROW BUFFER MODE CONFIGURATION

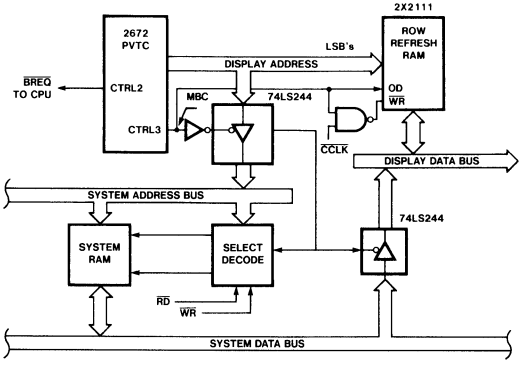


Figure 8

contention. After the row of character data is transferred to the CPU, BREQ returns high to grant memory control back to the CPU.

A MINIMUM CHIP COUNT TERMINAL IMPLEMENTATION

Figure 9 is the schematic of a minimum chip count CRT terminal using the four CRT set devices. Only 15 IC packages are required for the complete implementation, including all keyboard encoding and RS-232 level conversion for the serial interface. Despite this low chip count the terminal is capable of providing an impressive array of features including:

Display Format·
- 24 or 25 character rows
- 80 characters per row

Character Format.
- 7x9 dot matrix character in a 9x12 character block
- 96 ASCII alphanumeric characters
- 32 special symbols
- Block graphics
- Line drawing character set

Cursor·
- Underline or block cursor
- Optional blinking

Keyboard:
- 128 keys maximum
- Non-encoded
- Cursor control keys
- Numeric keypad

Serial Interface·
- Full or half duplex
- RS-232 compatible
- 16 baud rates with internal baud rate generator
- Character or block transmission

Operating Modes:
- Normal
- Transparent (displays graphic and control characters)
- Page or scroll with optional smooth scroll

Visual Attributes.
- Blink
- Reverse video
- Highlight
- Underline
- Non-display

The system utilizes the independent buffer mode to minimize hardware requirements. The dual port interface to the 2Kx8 display buffer is via a Signetics 8X31 bidirectional latch This may be replaced by a unidirectional latch such as the 74LS374 if reading of the RAM's contents by the CPU is not required.

The operating program for the terminal is contained in the internal ROM of the 8049 microcomputer, which also provides the RAM required by the system program. Since the majority of the terminal's features are tailored by firmware, the ROM size can be increased, either internally or externally, to support additional functions.[1]

BASIC TERMINAL SOFTWARE

The software for a microcomputer based terminal is closely tied to the system hardware configuration and its characteristics. If an interrupt driven mode of operation is desired, the system hardware/software design must be capable of prioritizing the interrupts so that the system will correctly service interrupts from different sources. In a typical system, there are three interrupt sources· the keyboard, the communications interface, and the video timing controller. The latter must usually be assigned the highest priority since failure to service an interrupt from the video timing controller on a timely basis may result in visual perturbations on the display The keyboard and datacomm interrupts can, in most cases, absorb some time delay before they are serviced since they include one or more levels of data buffers.

[1]A pre-programmed 8049 microcomputer containing the operating firmware for this terminal will be available from Signetics.

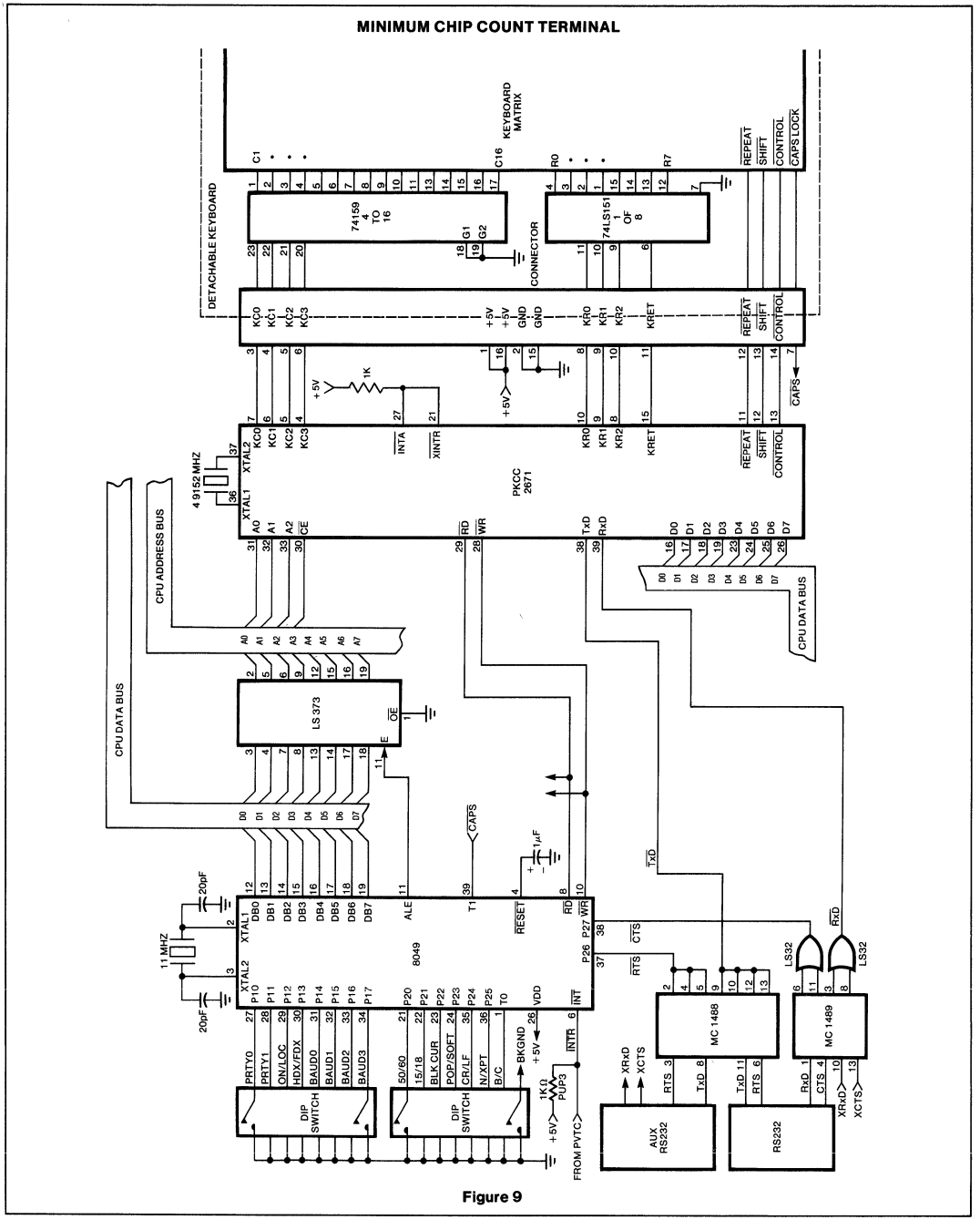

MINIMUM CHIP COUNT TERMINAL
DETACHABLE KEYBOARD
KEYBOARD MATRIX
CONNECTOR
74159 4 TO 16
74LS151 1 OF 8
REPEAT
SHIFT
CONTROL
CAPS LOCK
PKCC 2671
4 9152 MHZ
CPU ADDRESS BUS
CPU DATA BUS
LS 373
8049
11 MHZ
20pF
1µF
DIP SWITCH
AUX RS232
RS232
MC 1488
MC 1489
LS32
FROM PVTC

Figure 9

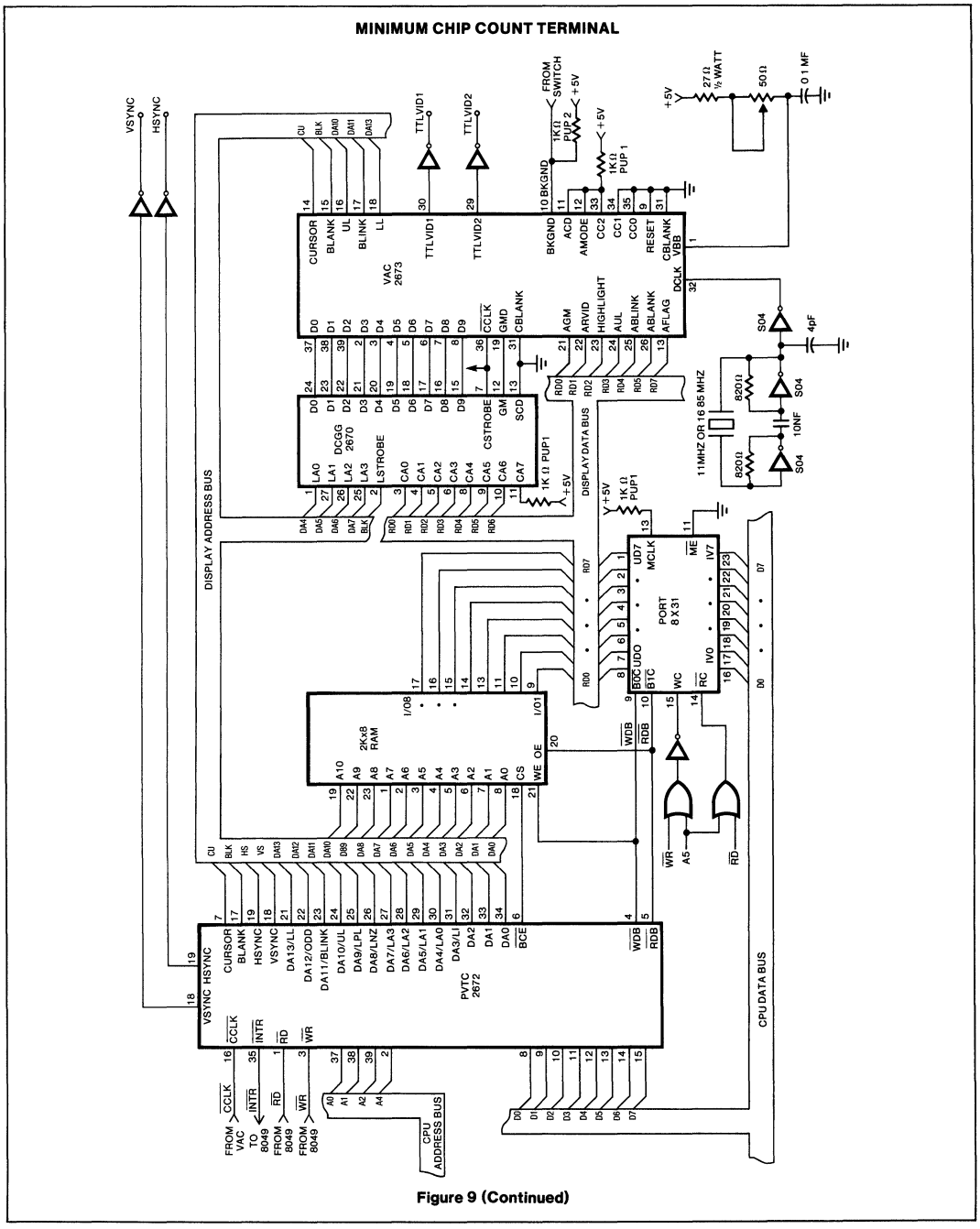


Figure 9 (Continued)

Often, a multi-level interrupt structure will be required so that a high priority interrupt requiring immediate service can be serviced even while the system is in the process of servicing a lower priority interrupt.

A simplified flowchart for the software for an interrupt driven terminal is shown in figure 10. After application of power, the microprocessor first performs a system initialization routine which consists of five parts:

1. Clear the microcomputer's scratchpad RAM.
2. Initialize the 2672 PVTC for the desired screen format, monitor timing parameters, cursor parameters, and display start address.
3. Clear the CRT display by loading a non display-code (usually an ASCII 'space', 20 hex) into the buffer memory.
4. Initialize the 2671 PKCC for the desired keyboard and serial interface modes.
5. Read any mode switches (e.g., full or half duplex, baud rate, cursor type, etc.) and set system parameters as required.

The processor can now enable its interrupts and wait in a loop until an interrupt is received. When this happens, the processor first determines the source of the interrupt and then performs the required system operation.

An interrupt from the CRT timing controller usually indicates that some information is required for proper screen refresh operation. For example, the PVTC may issue a 'split screen' interrupt to indicate that a new address must be loaded into its screen start registers in order for the next character row to be displayed from other than the next sequential address in memory. The CPU must service this interrupt within a finite time in order for the display to operate correctly.

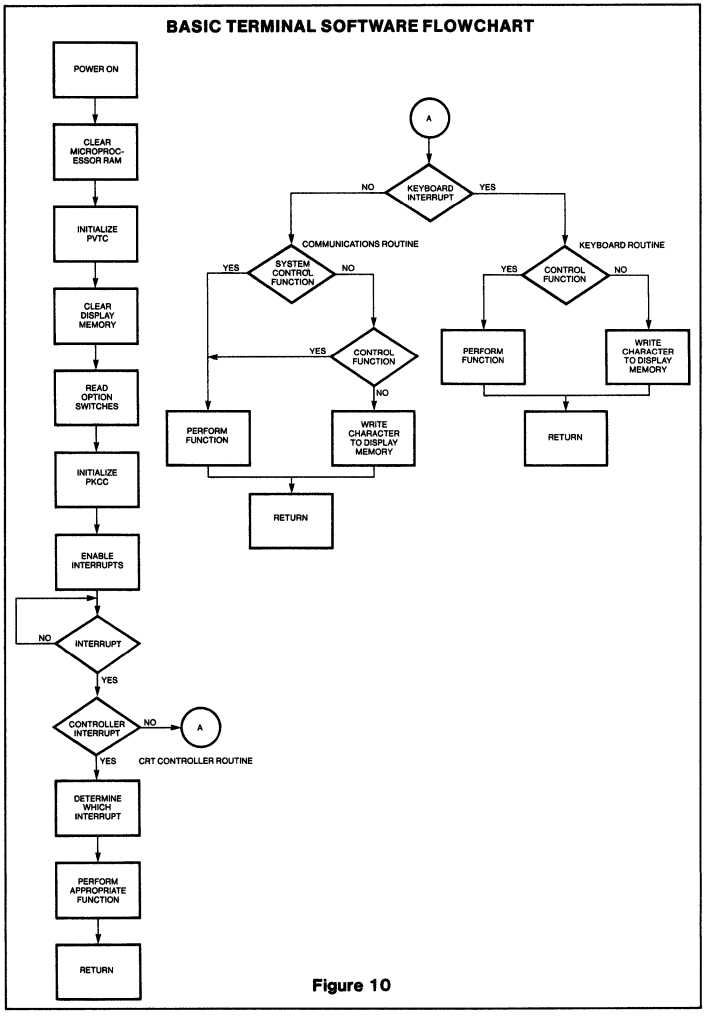


Figure 10

An interrupt from the keyboard interface may be either a displayable character or a control function. Displayable characters are usually transmitted to the host computer and also placed into the buffer memory for display on the terminal. Certain control characters, such as cursor control keys or keyboard error codes, may cause only local actions, while others will also require transmission to the host.

An interrupt from the data communications interface may also be a displayable character or a system control character. In either case the microprocessor must determine the type of character and perform the necessary system operation.

A DESIGN EXAMPLE

A fully operational emulation of an IBM 3101 terminal was designed and constructed using the Signetics CRT chip set. The terminal incorporates the majority of the 3101's functions. Selected functions were not incorporated due to program memory limitations. For example, the tabbing functions were developed and tested but were left out in deference to the block transmission functions. More features could have been included by selecting another of the numerous microprocessor devices on the market with greater program memory capacity. Major features of the terminal are summarized in table 1.[1]

[1]A data package for the design, including details of operation, schematic, and program listing, is available upon request by writing to:
Signetics Corporation
Microprocessor Applications Dept.
Mail Station 12-76
P.O. Box 409
Sunnyvale, CA 94086

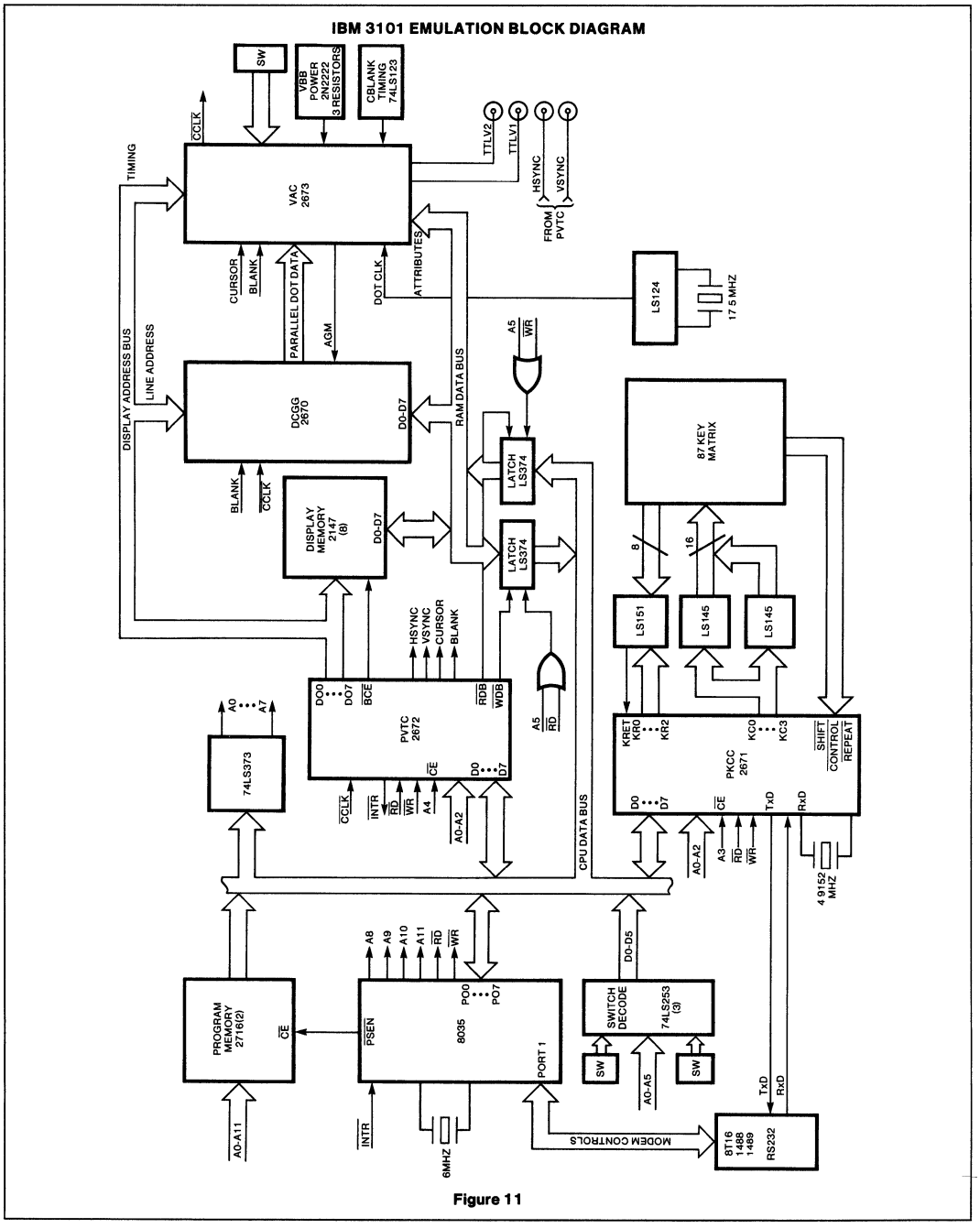

IBM 3101 EMULATION BLOCK DIAGRAM
SW
VBB POWER 2N2222 3 RESISTORS
CBLANK TIMING 74LS123
CCLK
TTLV2
TTLV1
HSYNC
VSYNC
FROM PVTC
TIMING
VAC 2673
CURSOR
BLANK
PARALLEL DOT DATA
AGM
DOT CLK
ATTRIBUTES
LS124
17 5 MHZ
DISPLAY ADDRESS BUS
LINE ADDRESS
DCGG 2670
D0-D7
RAM DATA BUS
A5
WR
LATCH LS374
87 KEY MATRIX
DISPLAY MEMORY 2147 (8)
8
16
LS151
LS145
LS145
HSYNC
VSYNC
CURSOR
BLANK
PVTC 2672
RDB
WDB
BCE
A0 ••• A7
74LS373
CCLK
INTR
RD
WR
A4
A0-A2
CE
A5
RD
KRET
KR0 ••• KR2
KC0 ••• KC3
SHIFT
CONTROL
REPEAT
PKCC 2671
TxD
RxD
CPU DATA BUS
A3
4 9152 MHZ
A8
A9
A10
A11
PROGRAM MEMORY 2716(2)
PSEN
8035
PORT 1
SWITCH DECODE
74LS253 (3)
SW
A0-A5
A0-A11
6MHZ
MODEM CONTROLS
8T16 1488 1489
RS232

Figure 11

Table 1 — TERMINAL FEATURES

Display Screen Format
- 2000 character screen capacity (25 rows x 80 columns)
- Operator information area (25th line)
- Block-shaped cursor with optional blinking

Displayable Graphic Set
- 95 ASCII characters for non-transparent mode
- 128 characters for transparent mode
- 7x9 character matrix in 9x12 field

Keyboard
- 63-key main keyboard
- 12-key control key cluster
- 12-key numeric keypad
- Keyboard lock/unlock under software control
- Keyboard clicker
- Typamatic operation

Edit Functions
- Cursor controls: up, down, left, right, home
- Cursor address read and write
- Erase functions: erase EOL, erase EOS, clear screen

Visual Attributes
- Highlighted field
- Blinking field
- Non-displayed field
- Underlined field

Modes of Operation
- Transmission modes: character or block (page or line)
- Normal or transparent

Line Protocol
- Asynchronous
- 7-bit ASCII with programmable parity
- One or two stop bits
- Full or half duplex
- Online or local
- Programmable line turnaround character for block mode (EOT/ETX/CR/XOFF)
- EIA RS232 interface
- Communication line speed: 50 to 9,600 baud

Screen Refresh Rate
- 60 Hz

Terminal Hardware

The block diagram of the 8035 based terminal is illustrated in figure 11. It is an expanded version of the logic shown in figure 9, the major difference being a larger display RAM, to provide up to two pages of screen data, and the addition of several input ports to handle the large number of option and set-up switches. The terminal's software is contained in 4K of program storage external to the 8035

The 2672 PVTC is programmed to operate in the independent buffer mode with the CPU isolated from the display RAM by two 74LS364 eight-bit latches, which provide the path for data transfers between the CPU and RAM. The PVTC, responding to commands from the CPU, completely controls the data transfer To avoid display interference, the PVTC is instructed to complete the access during a blanking interval. For massive display updates (clear screen, load form, etc.) the PVTC is instructed to blank the display and service the data transfer immediately and continuously. Additional memory contention circuitry is not necessary since the PVTC provides all of the timing and addressing (via cursor and pointer) necessary to complete the transfer. An interrupt from the PVTC informs the CPU when an operation is completed.

The PVTC addresses the display buffer memory, which contains both character and attribute data. An attribute byte is identified by the software by setting bit 7 of the byte to a logic 1. The RAM data outputs are applied to the 2670 DCGG, which provides the character dot data information, and to the 2673 VAC.

The VAC is hardwired to operate in the field attributes mode for this application. An attribute character occupies a screen position but is not displayed unless the ACD input to the VAC is asserted. Bit 7 of the character byte identifies a character as an attribute character if it is a 1. When bit 7 on the RAM data bus is a 1, the attribute byte is latched into the VAC to begin a new attributes field. Since the attributes are double buffered in the VAC, only one byte (at any character position) is required to specify a field.

The bipolar VAC circuit serializes the dot data from the DCGG into a 17.5 MHz data stream for the monitor. Two TTL-level video outputs provide three levels of video: black, white, and gray.

The PKCC provides the asynchronous data communications link at one of sixteen selectable baud rates. The PKCC addresses two 74LS145s which act as a 4-to-16 decoder to drive a 16x8 matrix keyboard. Key depressions are detected on the KRET input from a 74LS151 8-to-1 multiplexer. Each key depression is debounced, encoded according to the states of the SHIFT and CONTROL inputs, and presented to the CPU. Repeat and 'typomatic' (auto-repeat) functions are processed automatically by the PKCC.

Timing Calculations

One of the tasks required in the design phase of the terminal is the selection of a suitable monitor and calculation of the PVTC register values to provide suitable drive signals for the selected monitor.

The selection process begins with calculation of the required horizontal scan frequency. Each character will be contained in a 9 dot by 12 line field. Since there are 25 display rows, the total number of active scan lines will be 12 x 25, or 300. To this we must add some number of scan lines for the vertical retrace, which is typically 5 to 10 percent of the active scan lines. For a screen refresh rate of 60 Hz, this yields

H frequency = (60)(300)(1.1) = 18,900 Hz.

A Motorola monitor was selected for the application. The major timing specifications for the monitor are:

Horizontal frequency: 18.72 KHz ± 500 Hz
Horizontal retrace: 8 us max
Horizontal sync width: 4 us min
Vertical frequency: 50/60 Hz
Vertical retrace: 750 us max
Vertical sync width: 50 us min

Monitor timing definitions are shown in figure 12. The worksheet illustrated in table 2 can be used to compute the required timing and associated PVTC register values. Some rough guesses are required initially and several iterations through the worksheet will usually be required to arrive at final values. For example, the character clock period must be known to select the horizontal front porch (HFP), sync width (HSYNC), and back porch (HBP) values. An estimate of the character period can be made initially as follows:

Horizontal period = 1/18,900 = 52.9 us
Horizontal active = total - blank = 52.9 — 10 = 42.9 us
Character period = 42.9/80 = 0.53 us approximately

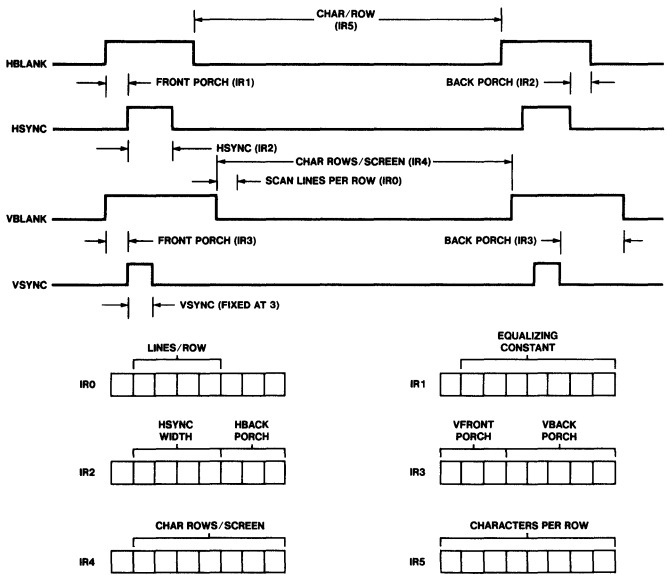


Figure 12

In calculating horizontal timing, an approximate ratio for the HFP, HSYNC, and HBP of 1:2:2 respectively is recommended.

Table 2 contains the final values selected for the application.

Memory Allocation

The 4K bytes of available buffer memory were allocated as follows (all addresses are in hex):

- 0000 to 004F: display data for row 25, status line
- 0050 to 0075: not used
- 0076 to 007F: CPU scratchpad
- 0080 to 07FF: display data for rows 1 to 24
- 0800 to 0FFF: not used, available for second page of display data

The PVTC's 'display buffer first address' and 'display buffer last address' registers are loaded with the values 0080 and 07FF respectively so as to cause this portion of the RAM to act as a circular buffer. Initially the display data is organized in the RAM as follows:

- 0080 to 00CF: row 1 data
- 00D0 to 011F: row 2 data

⋮

- 07B0 to 07FF: row 24 data

When a scroll operation is required, the CPU changes the value in the PVTC's 'screen start' register from 0080 to 00D0. This effectively shifts the displayed data up one row. Upon reaching the specified last buffer address (which is now the last character in row 23), the PVTC automatically changes the addressing sequence to resume starting at 0080 for the 24th row. The display data is now organized:

- 00D0 to 011F: row 1 data
- 0120 to 016F: row 2 data

⋮

- 07B0 to 07FF: row 23 data
- 0080 to 00CF: row 24 data

The CPU can clear the previous data in 0080 to 00CF so that a blank row appears in the 24th position.

The status line (row 25) data is kept in a separate section of RAM to eliminate the necessity of moving the data whenever the scrolling operation described above occurs. Thus, the PVTC must be instructed to change its addressing sequence at the beginning of the 25th row. This is accomplished by use of the split screen row interrupt capability. IR10, the 'split screen interrupt row' register, is initialized so as to cause an interrupt to be issued at the beginning of row 24 The CPU responds to this interrupt by changing the value in the screen start register to 0000. The PVTC then uses this value as the starting address of the next (25th) row, causing the status line to be displayed in that position. The CPU must re-load the screen start register before the end of the vertical blanking interval with the correct value for the first character to be displayed on the screen.

Terminal Software

Because the 8035 microcomputer used in the terminal provides only a single interrupt level, a totally interrupt driven software design could not be used. The interrupt was assigned to the PVTC to service the split screen interrupt described above and the operations required to implement the smooth scroll feature The keyboard and datacomm functions are serviced by polling the PKCC status register. Both the keyboard interface and UART receiver are double buffered in the PKCC, preventing overrun even if they are not serviced immediately.

The program generally follows the typical program flow described previously. At system reset the 8035 interrupts are dis-

Table 2 — CRT TIMING WORKSHEET

1.	HORIZONTAL CHARACTER BLOCK (no of dots)	9	
2.	VERTICAL CHARACTER BLOCK (no. of scan lines)	12	(IR0)
3.	VERTICAL REFRESH RATE, Hz	60	
4.	CHARACTERS PER ROW	80	(IR5)
5.	CHARACTER ROWS PER SCREEN	25	(IR4)
6	TOTAL ACTIVE VIDEO SCAN LINES (step 2 x step 5)	300	
7.	VERTICAL FRONT PORCH (no of scan lines)	4	(IR3)
8.	VERTICAL BACK PORCH (no. of scan lines)	12	(IR3)
9.	VERTICAL RETRACE INTERVAL (step 8 + 3)	15	
10	TOTAL SCAN LINES PER FRAME (add steps 6, 7, and 9)	319	
11	HORIZONTAL LINE RATE, KHz (step 3 x step 10)	19.14	
12.	HORIZONTAL FRONT PORCH (character time units)	5	
13.	HORIZONTAL SYNC WIDTH (character time units)	8	(IR2)
14.	HORIZONTAL BACK PORCH (character time units)	9	(IR2)
15.	HORIZONTAL RETRACE INTERVAL (step 13 + step 14)	17	
16.	TOTAL CHARACTER TIME UNITS IN ONE HORIZONTAL SCAN LINE (add steps 4, 12, 13, and 14)	102	
17.	EQUALIZING CONSTANT ([step 16 / 2] — [2 x step 13])	35	(IR1)
18.	CHARACTER CLOCK RATE, MHz (step 16 x step 11)	1.95228	
19.	CHARACTER PERIOD, us (1 / step 18)	0 512	
20	SCAN LINE PERIOD, us (step 19 x step 16)	53.27	
21.	DOT CLOCK RATE, MHz (step 18 x step 1)	17 57052	

	PARAMETER	SPEC	ACTUAL
A.	HORIZONTAL RATE, KHz	18.72 ± 0.5	19 14
B.	HORIZONTAL RETRACE TIME, us	8	8.7
C.	HORIZONTAL SYNC WIDTH	4	4.1
D	VERTICAL RATE, Hz	50 - 60	60
E	VERTICAL RETRACE TIME, us	750	784
F	VERTICAL SYNC WIDTH, us	50	157

abled, data memory and display memory are cleared to zeroes, and both the PVTC and PKCC are master reset through software commands The system option switches are then read and stored and the PVTC and PKCC internal registers are initilized for the selected operation Finally, the initial data for the status line is loaded, the PVTC, UART, and keyboard are enabled, and the CPU interrupt is enabled.

The program then enters a loop where the PKCC is checked for keyboard or UART entries. If an entry has occurred, the character is fetched and stored in a software controlled FIFO (first-in-first-out) memory which is eight bytes deep for both receiving or transmitting characters (the need for the FIFO is described below). If either FIFO has an entry, the program proceeds to a character recognition routine which checks for the type of character (displayable or control) and the appropriate handling subroutine (ESC sequence, control sequence, cursor control, character display, etc.) is called. If the FIFO's are empty, the polling routine checks the option switches for any changes since reset entry and if so reconfigures the system as necessary.

The need from the FIFOs results from the method used to effect the clear row function required when a scroll is performed Although the PVTC includes a 'clear from cursor to pointer' command that can be used to clear a block of memory rapidly, the display is temporarily blanked during this operation. This would cause undesirable flashes on the display. Instead, the program does the function by a repetitive loop using the 'write at cursor and increment' command. Since the write occurs only once per scan line during the active display window, a worst case total of approximately 80 scan line times is required to execute the routine. This would limit the maximum received character rate to approximately one per 80 scan lines or about 240 characters per second (2400 baud). To overcome this limitation, the PKCC is also polled each time through the clear line subroutine loop, and any entries from the receiver or keyboard are stored in the appropriate FIFO. Since the FIFO is eight deep, this allows eight characters to be received in the same time, increasing the maximum baud rate to 19,200. (Other program limitations actually reduce the maximum baud rate to 9600 baud) However, this does not increase the rate at which characters which cause a scroll function to occur, such as a line feed, can be received. Each character of this type must be followed by 'fill' characters in order for data rates higher than 2400 baud to be used

An interrupt from the PVTC will occur when the display scan reaches the row count programmed in its split screen address register, row address 24 (for the 24th row). In response to the interrupt, the CPU loads the screen start registers with the address of the status line (0000) and enables the PVTC's line zero interrupt. This causes another interrupt at the beginning of display of the status line. At this time the CPU reloads the screen start register with the proper address to begin the next display frame and disables the line zero interrupt.

If scrolling is required the screen start register value is incremented by 80 (popping off the top row) and the effective bottom row cleared to nulls. If soft scrolling is

selected, additional functions are performed during the interrupt routines. To begin the operation, the line zero interrupt routine adds ten lines to the vertical back porch. This causes the next active screen display to begin ten scan lines later than normal and gives the effect of the display moving up two scan lines (12 lines per character row - 10) instead of jumping up 12 lines. If nothing else were changed, however, the bottom of the display would move down ten lines. Thus, during the row 24 interrupt the number of scan lines per character row is changed to two (12-10), causing only the first two scan lines of that row to be shown. The next line zero interrupt (at row 25) restores the lines per row count back to 12 to keep the whole status line showing, and now changes the vertical back porch to 8. The display moves up two more scan lines and at the next row 24 interrupt four scan lines are shown The process continues in this manner, providing the effect of the entire display, except for the status line, smoothly scrolling up over a selected interval of six frames, or one tenth of a second

2661 OPERATING MODE SWITCHING PROCEDURES App Note 402

INTRODUCTION

This application note describes procedures for switching the operating mode of the Signetics' 2661 Enhanced Programmable Communications Interface (EPCI) from echoplex or remote loopback mode to normal operation and vice-versa.

ECHOPLEX (AUTOMATIC ECHO) MODE TO NORMAL OPERATION

The echoplex operation is initiated by setting command register bits CR7:CR6 = 01, and CR2 (receiver enable bit) = 1. Echoplex operation is terminated by resetting CR2 to zero. To ensure the proper transmission of the last received character, no change of operating mode should be made until the end of that character. However, if mode switching is necessary in certain applications, the following procedure is recommended to ensure no garbling on the last transmitted character. Two potential problems may arise: the calculated parity instead of the received parity may be transmitted, and data rate may be shortened or lengthened.

The procedure provides the necessary handshaking to avoid these potential problems by making use of the $\overline{\text{TXEMT}}$/$\overline{\text{DSCHG}}$ pin or of the status register bit 2, SR2, to indicate the end of the parity bit or the first stop bit, depending on whether one or two stop bits are selected (MR17:MR16 = 01 or 11). The procedure causes $\overline{\text{TXEMT}}$/$\overline{\text{DSCHG}}$ to be driven to its active state only at the completion of the last character, as shown in figure 1.

The recommended sequence of operation is as follows:

1. Wait for RXRDY (either RXRDY interrupt or status read). This is necessary for the assembly of the last character to be completed and to ensure the transfer of this character to the transmitter.
2. Enable the transmitter by setting CR0 to one.
3. Disable the receiver by setting CR2 to zero.
4. Wait for TXEMT (either $\overline{\text{TXEMT}}$/$\overline{\text{DSCHG}}$ interrupt or status read). At this point, the parity bit or the first stop bit (if two stop bits are selected) has been sent out.
5. Change mode from echoplex to normal.
6. Load new character into the transmit holding register, THR. Further communication between the 2661 chip and the CPU will resume as normal - that is, $\overline{\text{TXRDY}}$ is driven active to indicate that the THR is available for new data and $\overline{\text{TXEMT}}$ is driven active upon underrun condition.

Note that the $\overline{\text{TXEMT}}$ pin is not driven active in echoplex mode. It is optionally driven active when the above steps are followed, particularly the transmitter being enabled as indicated in step 2. Because the transmitter relies on CR0 = 1 and CR2 = 0 to drive $\overline{\text{TXEMT}}$ active, it is necessary to set CR0 to zero in echoplex mode if it is desired not to drive $\overline{\text{TXEMT}}$ active. CR0, transmitter enable, is ignored for data transmission in echoplex mode. It is, however, used to determine whether $\overline{\text{TXEMT}}$ should be driven active.

If frequent mode switching is anticipated and it is desired to drive $\overline{\text{TXEMT}}$ active, step 2 of the above procedure could be skipped, provided that the echoplex operation is initiated by enabling both the receiver and the transmitter - that is, CR2:CR0 = 11.

The $\overline{\text{TXEMT}}$ timing shown above is only applicable when switching modes. Note that in normal operation, $\overline{\text{TXEMT}}$ is driven active at the beginning of the last data bit or parity bit upon underrun condition.

$\overline{\text{TXEMT}}$/$\overline{\text{DSCHG}}$ OPERATION FOR ECHOPLEX MODE SWITCHING

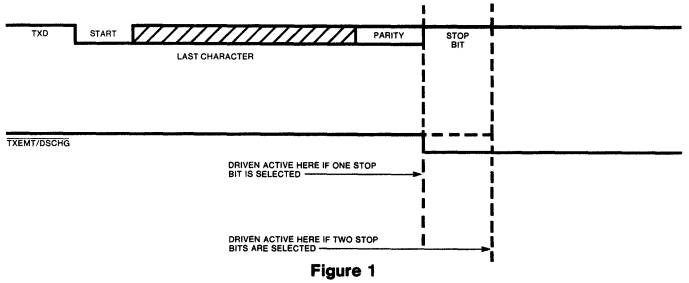


Figure 1

SWITCHING FROM NORMAL TO ECHOPLEX OR REMOTE LOOPBACK

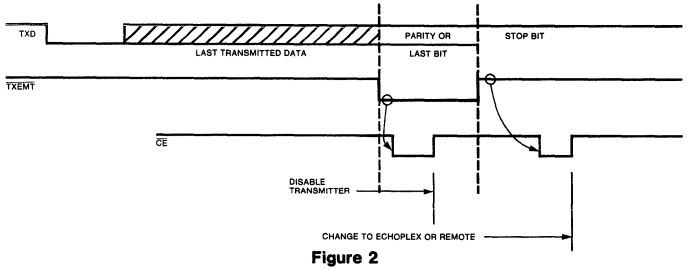


Figure 2

REMOTE LOOP BACK MODE TO NORMAL OPERATION

The procedure is similar to the procedure for echoplex to normal, with the following exceptions:

1. No handshaking with RXRDY is required.
2. During step 3 of the previous procedure, CR2 goes to zero, and CR7:CR6 should be simultaneously changed from 11 to 01 (remote to echoplex). This is necessary because the logic implemented to drive $\overline{\text{TXEMT}}$ active relies on echoplex information. However, this requirement does not need additional service from the controller because remote-to-echoplex switching is done at the same time as disabling the receiver.

NORMAL OPERATION TO ECHOPLEX OR REMOTE

To avoid garbling the last transmitted data, a mode switch from normal operation to echoplex or remote operation should be performed as follows:

1. Wait for TXEMT (either $\overline{\text{TXEMT}}$/$\overline{\text{DSCHG}}$ interrupt or status read) to be asserted.
2. Disable the transmitter by setting CR0 to zero.
3. Wait for TXEMT to be negated.
4. Change the mode from normal operation to echoplex or remote.

The timing is illustrated in figure 2.

Section 7
Appendices

PACKAGE OUTLINES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to center-line of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

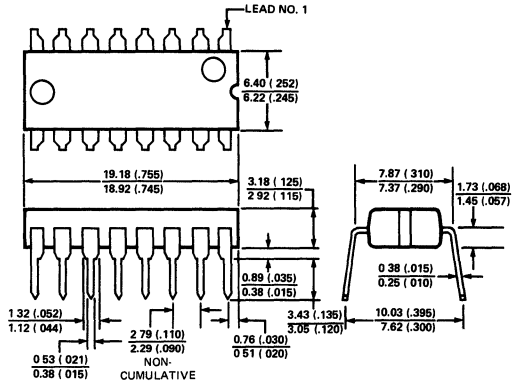
5. Lead material: Alloy 42 (Nickel/Iron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

Hermetic Only

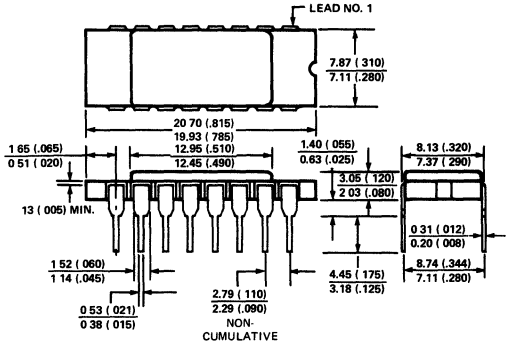
9. Lead material
   a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
   b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated, or solder dipped.
   c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
10. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
11. Lid Material
    a. Nickel or tin plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
    d. BeO ceramic with glass seal.
12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
13. Recommended minimum offset before lead bend.
14. Maximum glass climb 0.010 inches.
15. Maximum glass climb or lid skew is 0.010 inches.
16. Typical four places.
17. Dimension also applies to seating plane.

PACKAGE OUTLINES

N PACKAGE — PLASTIC (16-PIN)



I PACKAGE — HERMETIC (16-PIN)



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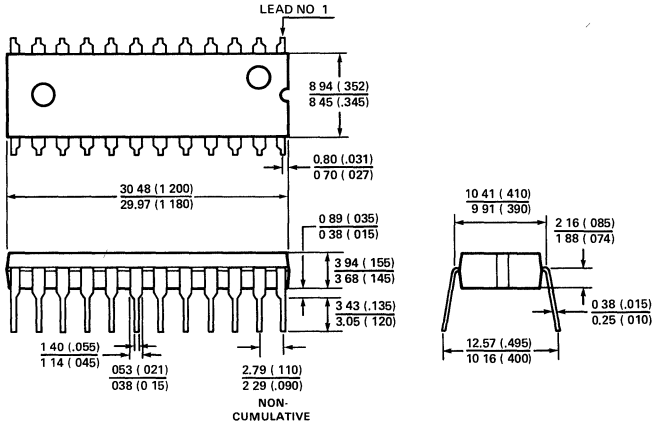
PACKAGE OUTLINES

N PACKAGE — PLASTIC SLIM LINE
(24-PIN)



I PACKAGE — HERMETIC SLIM LINE
(24-PIN)

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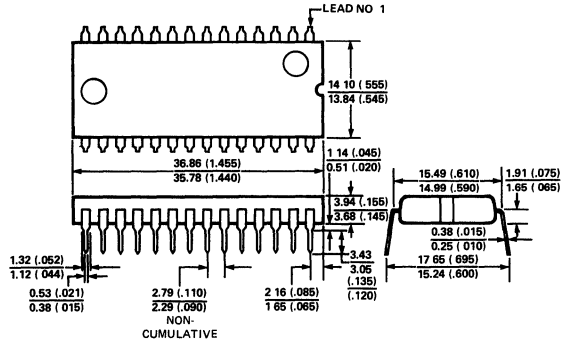
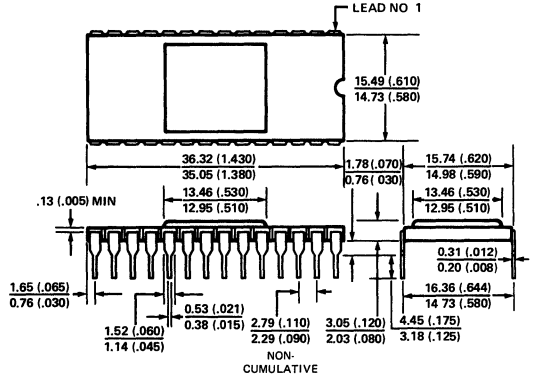
PACKAGE OUTLINES

N PACKAGE — PLASTIC (28-PIN)



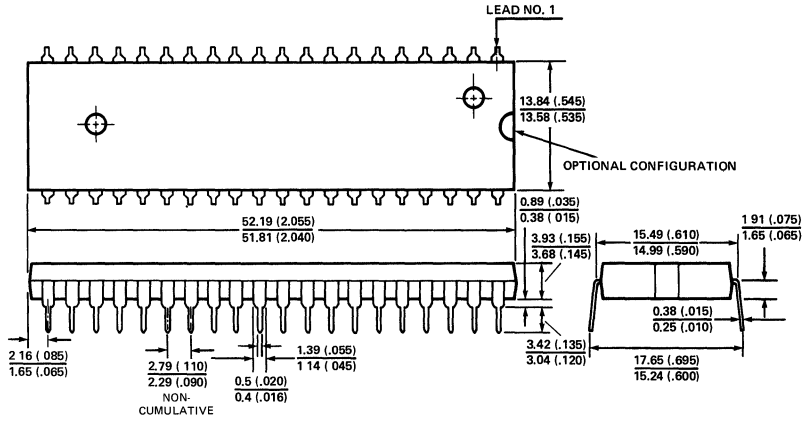
I PACKAGE — HERMETIC (28-PIN)



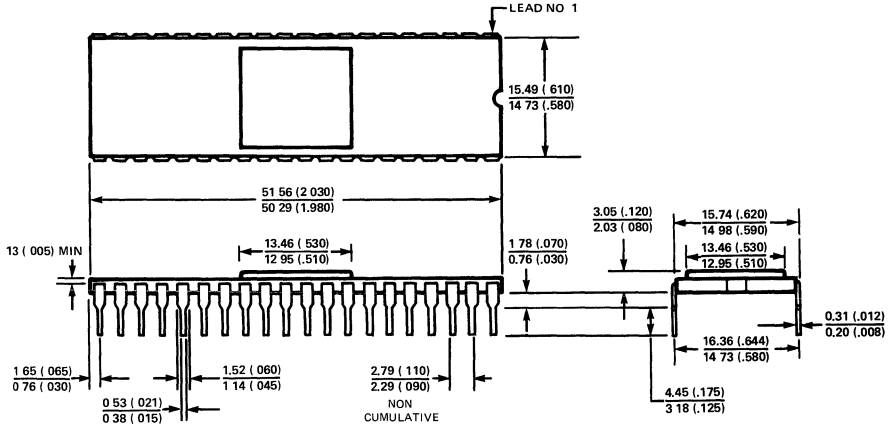
7

PACKAGE OUTLINES

N PACKAGE — PLASTIC
(40-PIN)



I PACKAGE — HERMETIC
(40-PIN)



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