Signetics
Fiber Optic
Communication
Data and
Applications

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Fiber Optic Communication Data And Applications

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Preface

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The Fiber Optic Communication Data and Application manual contains up–to–date device data and application information for the Signetics/Amperex/Philips chipset. The chipset is designed for use in point–to–point communication over the fiber optic medium. For your convenience, we have included information on the integrated circuits as well as the optoelectronic devices necessary for your application.

All devices included in this manual are available now. If you are interested in sampling these devices, please fill out the business reply card located in the back of this manual and forward it to Signetics. Upon receipt of your request form, your name and interest information will be placed into our Corporate database. This will be used to direct product updates to you.

We hope that you will find this manual informative and useful in your design activity. If you have any comments or questions, please feel free to contact **Signetics Linear Division, Fiber Optics Marketing at (408) 991–4730.**

ABOUT THIS MANUAL

This manual is organized in 5 different sections:

Section 1, Introduction, deals with the various communication standards and their application over the fiber optic medium, the generic point–to–point communication block diagram, the various fiber optic characteristics and our product offering described in this manual.

Section 2, Transmitter, describes a 50Mb/s, TTL single 5V supply fiber optic transmitter. The transmitter is based around the 74F3040 Line Driver.

Section 3, Receiver Data Recovery, describes various implementations utilizing our family of Transimpedance Amplifiers (NE5210, NE5211, NE5212) and Postamplifiers (NE5214, NE5217). This section also contains Application Note AN1435, describing the family of Transimpedance Amplifiers, an article reprint describing the postamplifiers, and a collection of up–to–date data sheets.

Section 4, Receiver Clock Recovery, describes a small scale integration clock recovery implementation using the NE568 Phase–Locked Loop. A second, NE564–based clock recovery implementation for T1 (1.544Mb/s) transmission, is described within AN182. Relevant data sheets are also included.

Section 5, Analog Video Transmission, describes a complete fiber optic link for transmitting video and audio information. It also contains the data sheets relevant to the video transmission. Data sheets for the products used in the audio transmission can be found in Signetics' three volume set of Linear Data Manuals.

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DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Section 1
Introduction

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Author: N. G. Damouny

Section 1
Introduction

COMMUNICATION/ INFORMATION TRANSFER

The need for information transfer is crystal clear and affects our daily activities. The information can represent Voice, Video, Data, etc. The public telephone network is a prime example of a world-wide Voice (and in some cases, Data) Communication network. Community Antenna Television (CATV), on the other hand, is a good example of an analog video distribution system.

When talking about Data Communication, for example, one cannot ignore the importance of standardized interfaces. One prime example is the well established EIA RS232 standard interface. Such an interface allows the system integrator to mix and match various vendor equipment and yet be able to interconnect them easily because they talk the same language.

Some of the key Standards Organizations are listed below:

Standards Organizations

International Standards Organizations:	
CCITT	Comite Consultatif Internationale de Telegraphique Telephonique
IEC	International Electrotechnical Commission
ISO	International Standards Organization

Multi-National Standards Organizations:	
CEPT	European Post and Telegraph Committee
ECMA	European Computer Manufacturing Association

National Standards Organizations:	
ANSI*	American National Standards Institute
IEEE	Institute of Electrical and Electronic Engineers
EIA	Electronic Industries Association

*Note: Any formal submission of EIA or IEEE standard documents to the International standard body (CCITT, IEC or ISO) will be through ANSI.

THE OPEN SYSTEMS INTERCONNECT (OSI) MODEL

Since one important objective of a communication network, for example a Local Area Network (LAN), is to allow dissimilar equipment to communicate easily, a strong need for uniform protocols and interfaces arose. This was addressed by the International Standards Organization (ISO) and the result was the Open Systems Interconnect (OSI) model. The ISO OSI 7-Layer model defines a hierarchical structure of tasks with defined interfaces between the various tasks; each addresses, specifically, how each task (or layer) interacts with the next higher and the next lower task.

The OSI tasks are specified in 7 layers (see Figure 1). Any communication node within a network (a computer,

terminal, peripheral equipment) shall implement all 7-layers especially if nodes from dissimilar LANs need to communicate intelligently.

Physical Layer
Specifies the electrical and mechanical requirement for transmitting *bits* across the underlying physical transmission medium (twisted-pair wires, coaxial cable, fiber optics, etc.). It deals with voltage levels, connector

USER APPLICATION SOFTWARE

	7	APPLICATION
	6	PRESENTATION
DATA FORMAT:	5	SESSION
MESSAGE _ _	4	TRANSPORT
PACKETS _ _	3	NETWORK
FRAMES _ _	2	DATA LINK
BITS_ _	1	PHYSICAL

SOFTWARE IMPLEMENTATION

HARDWARE DEPENDENT

PHYSICAL TRANSMISSION MEDIUM

Figure 1. The Open Systems Interconnect (OSI) Reference Model

issues and handshake protocols. An example is the RS232 protocol. Line drivers, receivers, and modem transceivers reside in this layer.

Data Link Layer
Deals with the way a communication node can access the underlying physical medium which is a common resource, e.g., Token passing and CSMA/CD (Carrier Sense Multiple Access with Collision Detect). Other functions implemented in this layer are clock recovery, error detection and correction, and data encoding and decoding. The data in this layer is represented by a *frame*. UARTS (Universal Asynchronous Receiver Transmitter), microcontrollers, and microprocessors all reside in this layer.

Network Layer
In this layer, frames are assembled to form *packets* and packets are disas-

sembled to form frames. Each packet has a sequence number and contains routing information through the packet-switched LAN.

Transport Layer
In this layer, packets are assembled to form *messages* and messages are disassembled to form packets. End-to-end message flow, routing, and message integrity are handled by this layer.

Session Layer
Responsible for setting up and terminating communication sessions in the network, e.g., log-on and log-off procedure.

Presentation Layer
This layer performs Code conversions and format translation; e.g., ASCII-to-EBCDIC conversion, also, line and page length and data encryption/decryption.

Application Layer
Includes the software driver needed to interact with the user's application program. Example services supported are Electronic Mail, file transfer, etc.

COMMUNICATION STANDARDS EXAMPLES

Dealing with creating Local Area Network (LAN) Standards are IEEE and ANSI. It was about 8 years ago when the two organizations agreed upon assigning LANs with less than 20Mb/s bit-rate to IEEE and greater than 50Mb/s to ANSI.

IEEE 802 LAN Standards Effort

In 1980 IEEE formed a standards Project (P802) to develop LAN standards with data rates up to 20Mb/s. Today the IEEE 802 Committee is a very efficient standards organization, meeting 3 times a year and consisting of 9 sub-committees:

+ 802.1 System Management
+ 802.2 Logical Link Control
+ 802.3 CSMA/CD Ethernet
+ 802.4 Token Bus
+ 802.5 Token Ring
+ 802.6 Metropolitan Area Network
+ 802.7 Broadband Technical Advisory Group
+ 802.8 Fiber OpticTechnical Advisory Group
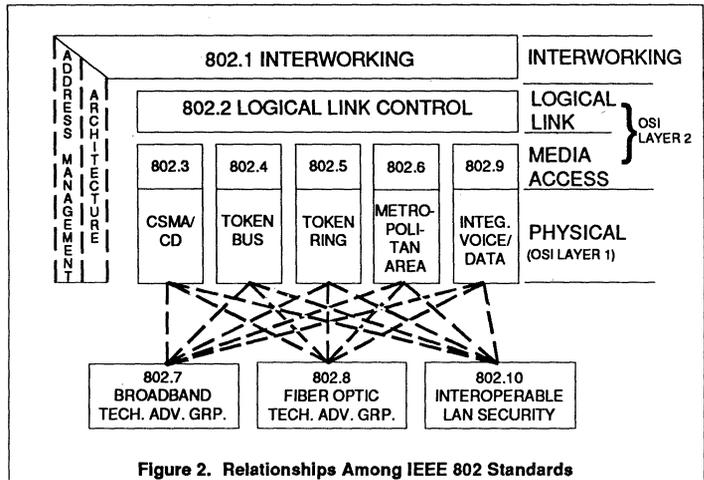
Figure 2. Relationships Among IEEE 802 Standards

+ 802.9 Integrated Voice and Data
+ 802.10 Standard for Interoperable LAN Security

These sub-committees only deal with the bottom two layers (Physical and Data Link) of the 7-layer OSI model.

Figure 2 depicts the relationship between the various IEEE 802 sub-committees. IEEE 802.3, .4, .5, .6 and .8 deals with the Physical Layer (Layer 1) and that part of Layer 2 dealing with the control procedure that a communication node needs to follow in order to access the shared communication channel (Bus or Ring). Transmission media first considered were coaxial cable and twisted-pair wires. Most recent activities are also dealing with fiber optics and through-air transmission.

IEEE 802.3 specifies a bus architecture using Collision Sense Multiple Access with Collision Detect, CSMA/CD, protocol. The bit rate is 10Mb/s and is Manchester encoded. This subcommittee houses not only the well-established "Ethernet", but also "Cheapernet", "STARLAN", "STARLAN 10" (or 10 Base T, 10Mb/s over the ordinary telephone wire-pair) and the newly formed "FOSTAR", or 10 Base F, specifying a 10Mb/s Star network over fiber optic cable.

IEEE 802.4 specifies a bus architecture with a token (a pre-determined sequence of bits) passing protocol. The node (or station) with the token is the bus master. The bus master re-

leases the token when it is finished transmitting and has received an acknowledgement from the destination. It then passes the token to the next node. General Motors Manufacturing Automation Protocol (GM MAP) specifies all 7 OSI layers, the bottom 2 layers of which are based on IEEE 802.4 standards.

IEEE 802.5 specifies a ring architecture with a token-passing access protocol. This architecture is fully backed by IBM and is sometimes referred to as IBM token ring network. The IEEE 802.5 deals with unshielded and shielded voice-grade twisted-pair lines with bit rates of 4Mb/s and 16Mb/s, respectively. The token ring architecture is very important since it represents an easy upgrade to fiber optic-based networks. This is particularly true since fiber optics can only be used in networks where a point-to-point communication scheme is utilized. (See fiber optic section for more detail.) This is why this architecture has been adopted by the high speed (100Mb/s) fiber optic-based network, FDDI (Fiber Distributed Data Interface).

Technical and Office Protocols (TOP), developed by Boeing, specifies all 7 OSI layers, in which the bottom 2 layers permit the use of CSMA/CD and token-passing on either a bus or a ring configuration, respectively. (IEEE 802.3, .4 or .5 compatible).

IEEE 802.6 is the Metropolitan Area Network (MAN) Sub-committee. This

is not quite a LAN since it covers large geographical areas. It also violates the 20Mb/s limit set by IEEE charter. It was in November 1987 when the Australian QPSX (Queued Packet and Synchronous Switch) proposal was adopted by IEEE 802.6. This is a dual bus architecture operating in opposite direction at 155Mb/s and utilizing fiber optic. This bit rate was selected to insure compatibilities with two other, and related, on-going standards efforts; Broadband Integrated Services Digital Network (BISDN) and Synchronous Optical Network (SONET).

IEEE 802.9 is the Integrated Voice and Data LAN (IVD LAN) Sub-committee. The intent here is to have a LAN that is ISDN compatible. This LAN not only utilizes packet-switching (for data), but will also utilize circuit-switching for digitized voice.

There are two Technical Advisory Groups (TAGs): one for broadband transmission technique (IEEE 802.7) and the second for utilizing fiber optics as the transmission medium (IEEE 802.8).

IEEE802.10 was formed in July, 1988 to study LAN interoperability security.

Finally, the IEEE 802.2 sub-committee specifies the logical link control procedure residing in layer 2 while the IEEE 802.1 sub-committee deals with architectural issues, address routing, and other LANs interworking issues.

It should be noted that the IEEE 802 Committee is the *mother committee* for all LAN standards-setting activities. This includes national activities such as ANSI's FDDI and various military LAN activities, and international activities such as the ISO 8802 series of standards.

ANSI FDDI Standards Effort

As was mentioned before, the American National Standard Institute (ANSI) charter is to develop LAN standards in excess of 50Mb/s data rates.

ANSI's primary effort in LANs is taking place under the X3T9.5 Sub-committee work, namely FDDI or Fiber Distributed Data Interface. This high speed, fiber-based LAN will facilitate comput-

NOTE: FDDI SPECIFIES LAYER 1 AND HALF OF LAYER 2 OF THE ISO OSI 7-LAYER MODEL

Figure 3. Fiber Distributed Data Interface (FDDI)
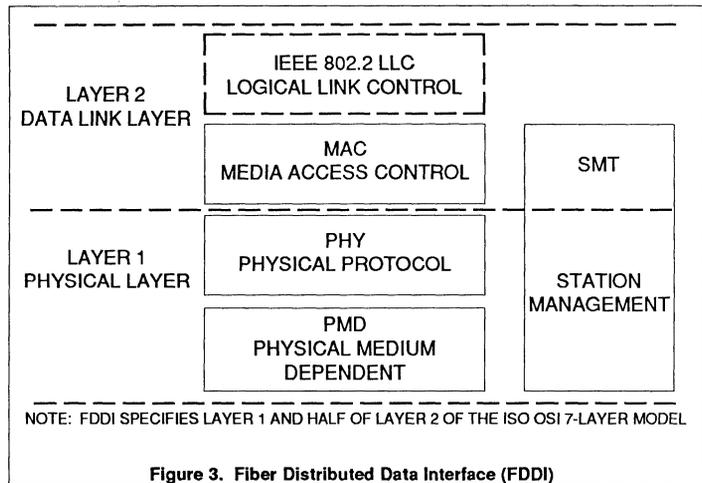
ers-to-high-speed peripherals communication and can serve as a backbone LAN interconnect.

FDDI specifies the Physical Layer (Layer 1) and a portion of Layer 2. It specifies the use of IEEE 802.2 for Logical Link Control (LLC).

Figure 3 depicts the 4 entities constituting a FDDI-compatible station (or node). These are the Physical Medium Dependent (PMD), Physical Protocol (PHY), Media Access Control (MAC) and Station Management (SMT):

Physical Media Dependent (PMD) specifying:
+ Cable plant
+ Media Interface Connector (MIC)
+ Media Signal Interface
+ Bypass capability

Physical Layer Interface (PHY) dealing with:
+ 4B NRZ to 5B NRZI, and vice versa, conversion
+ Clock recovery and synchronization
+ Serial to parallel and parallel to serial conversion
Media Access Control (MAC) performs:
+ Token Management
+ Creates packets around data to be transmitted and strips data out from incoming packets
+ Error checking and recovery

Station Management (SMT):
+ Performs connection

management
+ Fault detection and isolation
+ Various services for PMD, PHY and MAC

Some of the FDDI key specifications are:

+ Dual Token-passing (IEEE 802.5 compatible) counter rotating rings (Primary and Secondary rings) at 100Mb/s data rate. (The encoding scheme used requires a baud rate of 125Mbaud.)
+ Max ring latency is 2ms. Max distance between any two nodes is 2km.
+ Multi-mode fiber cable 62.5/125 micron (core/cladding diameter; see fiber section).
+ Photoemitter is 1300nm LED and photodetector is 1300nm PIN (Positive-Intrinsic-Negative) diode.
+ Bit Error Rate (BER) is 2.5×10^{-10} at min power.

A separate study group, within X3T9.5 Subcommittee, is looking at utilizing Single Mode fiber cables to extend the distance between any two nodes to the 10's of kilometers at the same bit rate of 100Mb/s and the same BER of 2.5×10^{-10}.

The above mentioned FDDI was conceived to provide a standardized mechanism allowing the exchange of high speed digital data between computers and high speed peripherals or, as a backbone network interconnecting various, similar or dissimilar, LANs.

FDDI-II is an enhanced FDDI allowing the high speed transfer (still 100Mb/s) of not only digital data, but also digitized voice and video. Both voice and video signals are *isochronous*.

FDDI-II, therefore, accomodates both packet-switching (for data) and circuit-switching for voice and video. The architecture for FDDI-II is very similar to that of FDDI, but with the addition of a "Hybrid Ring Control" (HRC) block which multiplexes and de-multiplexes both packet and isochronous data into and out of the ring.

SAFENET: Survivable Adaptable Fiber Optic Embedded Network

The Survivable Adaptable Fiber Optic Embedded Network, SAFENET, is an emerging Military communication standard.

SAFENET is a LAN-based system that can be used by the Navy for ship-board applications or by the Air Force for avionics applications.

SAFENET selection criteria has been:
+ The network to be defined should not be proprietary. This requires standardization.
+ The network should have wide acceptance in the commercial sector.
+ The network should be realized in the 1990s.
+ The Media Access Control must be deterministic.
+ High throughput and a low-latency medium must be available for future system expansion.
+ Chipsets must be available in the near term for testing.
+ The network must be adaptable to either a wire or fiber optic medium.
+ The network must have a robust reconfiguration scheme and must be survivable through several levels of failure.

The next generation SAFENET, known as SAFENET 2, will be compatible with the Fiber Distributed Data Interface (FDDI) standard.

SONET: Synchronous Optical Networks

The Synchronous Optical Networks, SONET, standards are being devel-

oped by the T1X1 Committee of the American National Standard Institute, ANSI.

SONET specifies the standards for Telecommunications digital hierarchy optical interface rates and formats, and specifies how to map various digital services into SONET payloads. SONET also covers the physical specifications which will permit optical transmission devices (i.e., cable facilities, line apparatus and terminal equipment) to achieve transmission compatibility at an arbitrary *optical interface* point.

Standard Optical Carrier (OC) rates specified by SONET are:

OC Level	Line Rate (Mb/s)
OC-1	51.840
OC-3	155.520
OC-9	466.560
OC-12	622.080
OC-18	933.120
OC-24	1244.160
OC-36	1866.240
OC-48	2488.320

Various equipment in the digital hierarchy can add-drop multiplex DS3 (Digital Signal 3 or 44.736Mb/s) and SONET OC-M signals onto an OC-N line where N>M.

FIBER OPTIC-BASED COMMUNICATION

As we discussed earlier, few standard activities have mandated the use of fiber optics as the transmission medium. IEEE802.6 MAN, ANSI FDDI and ANSI FDDI-II are such standards activities. Other IEEE 802 sub-committees are looking at standardizing on their own fiber optic-based versions. You might ask, "Why fiber at less than 20Mb/s?" Well, large bandwidth is only one of many advantages of using fiber optic. Smaller size, lighter weight, no RFI (Radio Frequency Interference), no EMI (Electro Magnetic Interference) and high security are other advantages that can represent greater value to some applications, for example, the Military communication market.

To date, the biggest fiber optic market has been the Telecom market. It should be noted here that "biggest"

means longest, i.e., thousands of miles of fiber-cable installation. To a semiconductor supplier such as Signetics, the number of stations (not the length) is what counts. This is especially true for fiber optic-based communication since, even repeaters rarely exist. For example, in the trans-Atlantic Fiber Optic link, the distance between repeaters is about 40km at a bit rate of over 400Mb/s. (Compare this with T1 transmission where repeaters are needed every 6,000 ft. at T1 rate of 1.544Mb/s).

Another piece of market data is that Single-Mode (SM) fiber cables are more widely used than Multi-Mode (MM) fiber cables. This to-date information is true since the majority of the telecom installations are laying down SM fiber cables for longer distance, higher-bit rate applications, and room for future expansion. Most LAN applications, on the other hand, specify the use of multi-mode fibers, for cost/performance reasons.

We have just heard about Single Mode and Multi Mode fibers. What are these and what are the other basics and terminologies about fiber optic communications?

Topology and Fiber Optic Characteristics

Fiber Optic Communication Links

+ Fiber optic links are usually *one way* (Simplex) communication links. In order to have a full-duplex (two-way, simultaneous) communication, two fiber optic links are needed; one for each direction. (Please note that the use of a single fiber cable for two way communication has been demonstrated in the military Fiber Optic Guided Missile (FOG-M) program in which signals are transmitted from the missile nose cone sensor back to the command center at a different wavelength than the command data traveling in the other direction. The other technique used for two-way communication over a single fiber cable is through the use of the Ping-Pong protocol in which only one transmitter is active at a time.)

+ Fiber optic link bandwidth is characterized by MHz.km. For example, a

fiber optic cable with 700MHz.km implies that a link of 1km, using this cable, will have a bandwidth of 700MHz, whereas, a 2km link will only have 350MHz bandwidth.

✦ Fiber optic-based transmission dictates point-to-point type network architecture. This is due to the fact that it is not easy to tap-off energy from the fiber optic cable. The use of passive optical couplers/splitters is prohibitive for links greater than a few 100 feet. Such de-

EXAMPLES ARE THE IEEE802.5 TOKEN RING AND THE ANSI FDDI NETWORKS

Figure 4. Ring Topology

EXAMPLE IS THE IEEE802.3 ETHERNET ON FIBER. IN THIS CASE, THE HUB CAN BE ACTIVE OR PASSIVE (PHOTONIC SWITCHING)

Figure 5. Star Topology

vices are not economical and they require relatively very large optical energy at the transmitter. As a result, the two widely used topologies for fiber optic-based communication are the Ring and

the Star. (See Figures 4 and 5.)
✦ The *link budget* in fiber optic-based communication refers to the available power budget, in db, for a given fiber link. For example, for a fiber optic link with the following characteristics:
Transmitter output power = -20dBm min; -14dBm max
Receiver input sensitivity = -31dBm min; -14dBm max

The Link Budget is:
$$-20\text{dBm} - (-31)\text{dBm} = 11\text{dB}$$

(XMT)   (RCV)

This budget of 11dB is allocated to the optical cable loss, connector losses, photoemitter coupling loss, etc. Note that the above power figures take into account an ideal link with a zero power link budget(Max. Transmit power ≅ Max. Receiver power = -14dBm). The above specifications are real and reflect the actual FDDI power specifications.

Multi-Mode (MM) and Single-Mode (SM) Fibers

Fiber optic cables consist of a glass silica core and cladding and a protective jacket referred to as the sheath. (See Figure 7).

Both the core and cladding are made of the same material (silica). The only difference is that a dopant is added to one or the other. This process allows light to

be reflected at the core/cladding boundary and, hence, propagate down the axis of the fiber.

There are two major fiber optic cable categories:

1. Multi-Mode fiber:
✦ A mode represents a unique solution to the "scalar wave equation". A typical 62.5/125 micron fiber has around 400 modes at 1300nm wavelength.
✦ Multi-mode fibers require the use of LEDs as photoemitters.
✦ Typical core/cladding diameter is 62.5/125 micron in the US and 50/125 micron in Japan. Older but common values include 100/140 micron.
✦ Multi-mode fiber has a much smaller bandwidth distance (MHz.km) parameter than Single-mode fiber. This is because Single-mode fiber uses a coherent light source (Laser) and introduces fewer losses than multi-mode fiber.

2. Single-Mode fiber:
✦ Has only one mode at wavelengths above a certain value called the "cut-off wavelength".
✦ Requires the use of laser diodes.
✦ Typical core/cladding diameter is 8/125 micron.
✦ Used in applications requiring larger bandwidth and longer distances between consecutive stations.
✦ Single-mode/laser assembly is more expensive than multi-mode/LED assembly.

Optical Wavelength, Photoemitters and Photodetectors

✦ The visible light has wavelengths in the region between 390nm (blue light) and 780nm (red light)
✦ The "near infra-red" region includes wavelengths in the range of 800 to 1600nm. This is the range fiber optic transmission is using today.
✦ There are 3 distinct wavelengths of major concern: 850nm, 1310nm and 1550nm. (Figure 6)
✦ 850nm wavelength has been very widely used. The cable loss is a little over 2dB/km. Optoelectric devices at this wavelength are very economical and have proven to be very reliable. Most of the installations, to date, use 850nm.
✦ 1310nm is one point in the loss curve (Figure 6) at which the loss is minimal. FDDI is specifying the use of 1300nm.

Figure 6. Silica Fiber Optic Cable

Figure 7. Cross-Section of an Optical Fiber Cable
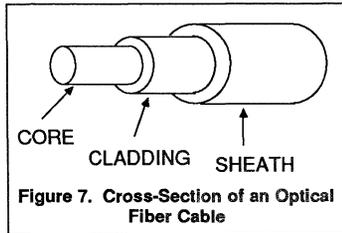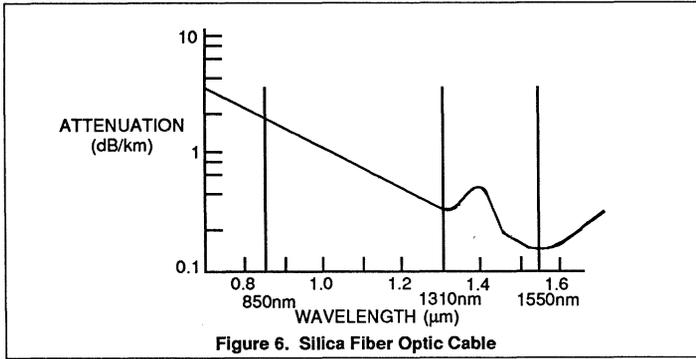
✦ 1550nm is yet a lower dip in the loss curve and represents a very low loss condition (less than 0.2dB/km). Considerable research is done at this wavelength. Available devices are still relatively expensive.
✦ Photoemitters (or light sources) can be either a LED (Light Emitting Diode) or a Laser. LEDs are lower in cost and more reliable, but emit a non-coherent light. Lasers, on the other hand, emit a coherent light and are used with single-mode fibers. The problem with lasers is their lack of stability with temperature variations and bias voltage, and they are more expensive. Since light is emitted from both sides of the laser, the one side that is not coupled to the fiber cable is fed into a local photodetector to monitor the laser output power. This is referred to as Automatic Power Control (APC). (Compare this with Automatic Gain Control [AGC]).

✦ Photodetectors can be either a PIN (Positive-Intrinsic-Negative) diode or an APD (Avalanche Photo Diode). The latter provides not only detection, but also gain, and is used when greater receiver sensitivities are needed. The problems with APDs are not only the cost, but also the added circuitry required to stabilize it. This is necessary because APDs are very bias-voltage sensitive.

Point-to-Point Communication

✦ Fiber optic communication links utilize fiber optic cables as the transmission medium. Serial binary electrical data (TTL or ECL levels) at the transmitting station (or node) is converted into optical energy carrying photons, through the use of Electrical-to-Optical (E/O) converters (see Figure 8). On the receive side, incident photons are converted into serial binary electrical data (TTL or ECL levels, depending on which levels were used at the transmitter) through the use of Optical-to-Electrical (O/E) converters (see Figure 8).

Any fiber optic communication link will need this dual conversion process. The E/O and O/E modules can then be universally applied to any communication network utilizing fiber optic as the transmission medium.

The E/O module consists of an LED/Laser driver and a photoemitter (LED or Laser). The O/E module consists of a photodetector, a preamplification/post amplification stage and a clock recovery circuit to recover the clock from the received data.

Product Offerings and Applications

The product offerings, at present, focus on the chipset required to implement the point-to-point fiber optic communication link. The interface is TTL compatible and requires a single 5V supply. The integrated circuits perform the LED driver, pre and postamplifier and clock recovery functions. The optoelectronic devices are the photemitter and photodetector.

The integrated circuits, described in this manual, can be used in any fiber optic-based system: 660, 780, 850, 1300 or 1550nm wavelength, with LED or laser photoemitter, PIN or APD photodetector, single or multi mode optical fiber cable.

Since all of the application work described in this manual was performed using 850nm optoelectronic devices, only those devices have been listed in the book. It should be noted, however, that Philips/Amperex offers a complete line of optoelectronic devices. For more information on these devices, please contact (in the USA) Amperex Optoelectronics Division at (401) 232-0500. In Europe, Japan, and Southeast Asia, please contact the local Philips components sales office.

Figure 9 depicts a typical fiber optic-based, point-to-point communication

E/O (ELECTRICAL/OPTICAL) CONVERTER = LED/LASER DRIVER + LED/LASER

O/E (OPTICAL/ELECTRICAL) CONVERTER = PIN/APD DIODE + PREAMP + POST AMP + CLOCK RECOVERY

Figure 8. Typical Fiber Optic-Based Communication Link

1-8
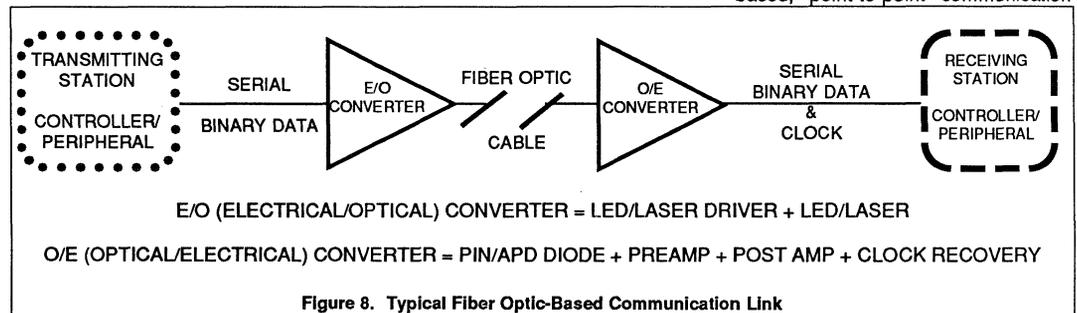
link. the transmitter consists of the LED driver, for example, the 74F3040 and the CQF41 850nm LED. The receiver consists of a 850nm PIN diode, the BPF31, a transimpedance amplifier, a postamplifier and a Phase-Locked Loop-based clock recovery/retiming function. Table 1 depicts the trans-impedance amplifier family, while Table 2 lists the post amplifier family.

Example applications for the chipset include:

◆ **Local Area Network:**
Ethernet
Token Bus
Token Ring
Metropolitan Area Network (MAN)

◆ **Telecommunications:**
T1 Multiplexers (1.544Mb/s)
DS3 (44.736Mb/s)
Synchronous Optical Network (SONET)
Broadband ISDN

◆ **Military:**
High Speed Data Bus
Token Passing Multiplexed Bus
Survivable Adaptable Fiber Optic
Embedded Network (SAFENET)

◆ **Consumer:**
Automotive
Community Antenna Television (CATV)
Digital Audio
Fiber to the home

Table 1. Wideband Transimpedance Amplifier Family

Part	Transresistance kΩ (typ.)	Bandwidth -3dB (typ.)	Input Noise Current (typ.)	Max. Input Current
NE5212	14	140MHz	2.5pA/√Hz	±120μA
NE5211	28	180MHz	1.8pA/√Hz	±60μA
NE5210	7	280MHz	3.5pA/√Hz	±240μA

Table 2. Post Amplifiers With Link Status Indicator Output

Part	Bandwidth -3dB (typ.)	Interface	Application
NE5214	75MHz	TTL	$2^7 - 1$
NE5217	75MHz	TTL	$2^{23} - 1$
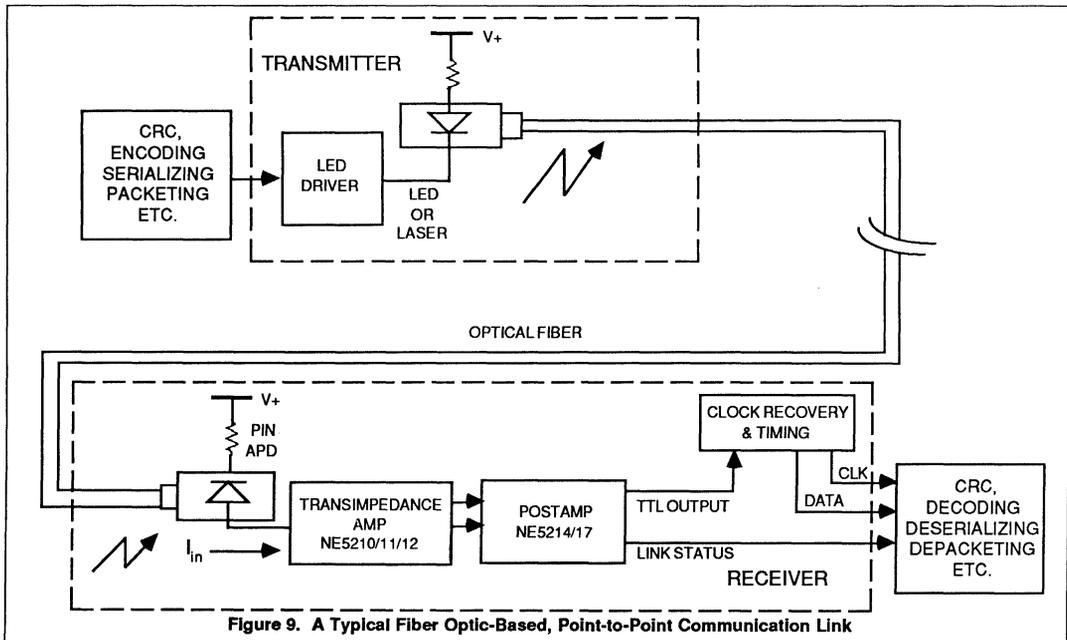
Figure 9. A Typical Fiber Optic-Based, Point-to-Point Communication Link

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Section 2
Fiber Optic Transmitter

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AB1121
50Mb/s LED Driver for Fiber Optic Communications

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Application Brief

Author : P. Shah

INTRODUCTION
The virtues of fiber optic data communications have been discussed earlier in great detail in several publications. This applications brief will address the transmitter aspect of the fiber optic system, specifically the LED driver with a TTL interface. Since most TTL systems are limited to 50Mb/s data rates, this application brief will also focus on the same data rate, although enough applications information will be given to tailor the system performance to any data rate within the frequency limits of the devices.

SYSTEM REQUIREMENT
A simplified block diagram of the transmitter is shown in Figure 1. It depicts a current source driving the anode of an LED when the input data is a logic HIGH
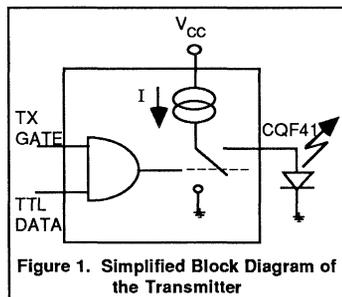

Figure 1. Simplified Block Diagram of the Transmitter

and switched to ground when the input data is a logic LOW. It also shows a Tx Gate which enables the transmitter when asserted HIGH. This is a very simplistic diagram, but later on some of the major issues regarding the design of the transmitter will be discussed in detail. In designing the transmitter several parameters should be considered, viz. optical rise time, optical fall time, optical pulsewidth distortion at the output, optical power output, optical peaking, optical overshoots and undershoots, etc. It should also be noted that an LED is a non-linear device with non-uniform impedance and non-linear transfer characteristics. Due to these characteristics the LEDs are harder to turn off than to turn on and the phenomenon commonly associated with the difficulty in turning-off the LED is referred to as the long-tailed response of an LED. All these characteristics of the LED necessitate a driver circuit which is capable of delivering more than 60mA of current into a low impedance LED with extremely fast electrical rise and fall time.

TRANSMITTER DESIGN
Reviewing the specifications of 74F3040, the FAST TTL 30Ω line driver, indicates that it has several desirable characteristics which make it suitable as an LED

driver with TTL interface. The totem pole output on 74F3040 is capable of sourcing >60mA and sinking >120mA of current from the low impedance load. The electrical rise and fall times are less than 2ns and the t_{PLH} and t_{PHL} are fairly matched. The 74F3040 from Signetics has several attributes which make it suitable for this application. At V_O = 1.5V, the output resistance is about 23Ω. The slope of the sourcing and sinking currents extended to zero output current switched between the supply rails is very linear which improves the incident wave switching performance. The unique design of the totem pole output eliminates output current spiking or current feedthrough. The 74F3040 also has a patented low impedance voltage reference (LIVR) for input speed up and output noise immunity improvement. There is also a patented active pull-off (APO) circuit consisting of a dynamic base discharge and quiescent pull-off network for the output pull-down transistor. This network eliminates any totem pole feedthrough currents. Further information on the 74F3040 can be obtained from applications note AN213 of the Signetics FAST Data Manual.

The complete schematic of the LED driver is shown in Figure 2. The pull-up

NOTES: $R_A = 14\Omega$
$R_B = 4\Omega$
$R_C = 90\Omega$
$C_A = 250pF$
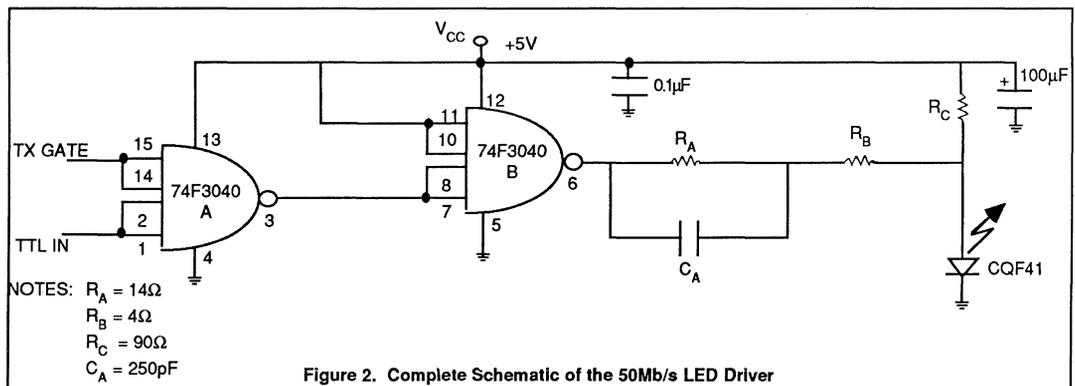
Figure 2. Complete Schematic of the 50Mb/s LED Driver

A 50Mb/s LED Driver for Fiber Optic Communications AB1121

transistor of the totem pole output is used to turn on the LED and the pull-down transistor is used to turn off the LED. The lower impedance and higher current handling capability of the saturated pull-down transistor is used as an effective method of transferring the charge from the LED's anode to ground as its dynamic resistance increases during turn-off. The slightly higher output impedance of the pull-up stage ensures that the LED is not over peaked during the less difficult turn-on transition. This asymmetric current handling capability of the output stage with its variable impedance substantially reduces the pulsewidth distortion and long-tailed response. As the signal propagates through two NAND gates, each transition passes through the high-to-low and low-to-high transition once, normalizing the total propagation delay through the circuit. The t_{PLH} and t_{PHL} for the entire system are equal and thus the duty cycle distortion is reduced.

In order to further improve the optical performance, prebiasing and drive current peaking, or precharging, techniques are used. Prebiasing is needed to apply a small amount of current to the LED when it is in the off state. This prebias current prevents the junction and parasitic capacitances from discharging completely when the LED is in the off state and reduces the amount of charge that the driver must transfer to turn the LED on again. Drive current peaking, or precharging, refers to momentary increase in the LED forward current that is provided by the totem pole output stage during the rising and falling edges of the current pulses that are used to modulate the LED. If the time constant of the precharging circuit is approximately equal to the minority carriers lifetime of the LED used, then this momentary increase in the current will improve the optical rise time and fall time of the LED without causing excessive ringing in the optical pulses. Overshoot and undershoot in the transmitter optical output, which result due to excessive LED peaking, can combine with noise at the fiber optic receiver and cause errors if they cross the decision threshold of the comparator at the receiver. Excessive peaking during the turn off transition could cause the LED to become reverse biased and

degrade the turn on time. The resistors R_A, R_B and R_C and the capacitor C_A are used for the prebiasing and precharging of the LED. Basic circuit analysis techniques can be employed to define the equations for these components. The values of these components can be calculated using the following equations.

$$R_C = \frac{(V_{CC} - V_{FON})}{I_{FON}} + \quad \text{Equation 1}$$
$$3.2 \frac{(V_{CC} - V_{FON} - 1.4)}{I_{FON}}$$

where V_{FON} = Forward ON voltage of the LED and I_{FON} = Forward ON current of the LED at V_{FON}

$$R_O = \frac{(R_C - 32)}{3.2} \quad \text{Equation 2}$$

where $R_O = R_A + R_B$ Equation 3

$$R_A = \frac{(R_O + 10)}{2}$$

$$R_B = R_A - 10 \quad \text{Equation 4}$$

$$C_A = \frac{4ns}{R_A} \quad \text{Equation 5}$$

CALCULATIONS
The schematic shown in Figure 2 was tried with several different LEDs and a listing of these LEDs in given at the end of the applications brief. The Philips LED CQF41 will be considered here as an example for the calculations. (The CQF40/41 is included in this volume.) From the transfer characteristics of CQF41 it is seen that V_{FON} = 1.8V at 100mA and the LED has maximum power output of 0.8mW at 100mA. Using these values of V_{FON} and I_{FON} in Equation 1, R_C = 90Ω. Using Equations 2, 3, 4 and 5 the values of R_O = 18Ω, R_A=14Ω, R_B=4Ω and C_A=250 pF. These values were used in the applications board and the following results are discussed.

RESULTS
The printed circuit board layout for the transmitter is shown in Figure 3 and the test and measurement setup for the applications characterization is shown in Figure 4. Figure 5 shows the optical output signal for a 50Mb/s 1-0 alternat-

ing pattern. The fiber optic link is about 1 meter long. The fiber type is 50/100μm with SMA connectors at each end. The losses due to the connectors are about 1.5dB. It can be seen that the peak-to-peak optical output power at the end of the short SMA link is 18.74 μW. The rise time is 3.964 ns and the fall time is 4.041ns. The pulsewidth is 19.55ns and so the pulsewidth distortion is about 2.25%.

To improve the performance of the system, a higher speed LED can be used with all the passive components in surface mount packages to reduce the lead inductances. The traces on the printed circuit board should also be shortened. The 74F3040 is capable of >100 Mb/s NRZ data rates, although extremely fast LEDs would be needed for fast rise and fall time and minimum pulsewidth distortion.

CONCLUSION
A 50Mb/s TTL input fiber optic transmitter was explained in detail. A complete schematic was given with its printed circuit board layout. The results obtained from this board were illustrated. The performance was given with suggestions for further improvement.

APPENDIX
The following LEDs have been tested with the given transmitter design. The selection of the LEDs is left to indiviual applications requirements. Some devices have higher power output but lower data rates; others have lower power but are capable of higher data rates.

LED	Manufacturer
CQF24	Philips/Amperex
CQF30	Philips/Amperex
CQF31	Philips/Amperex
CQF40	Philips/Amperex
CQF41	Philips/Amperex
CQF42	Philips/Amperex

A 50Mb/s LED Driver for Fiber Optic Communications

AB1121

NOTE: Contact factory for actual dimensions.
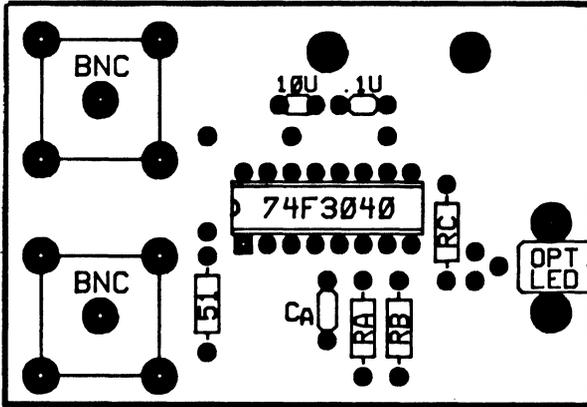
3a. Component Layout
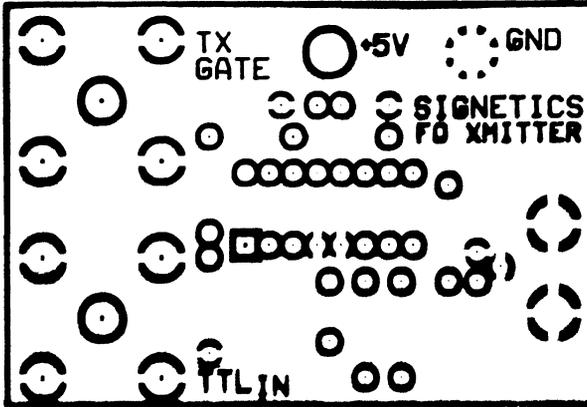
3b. Top View
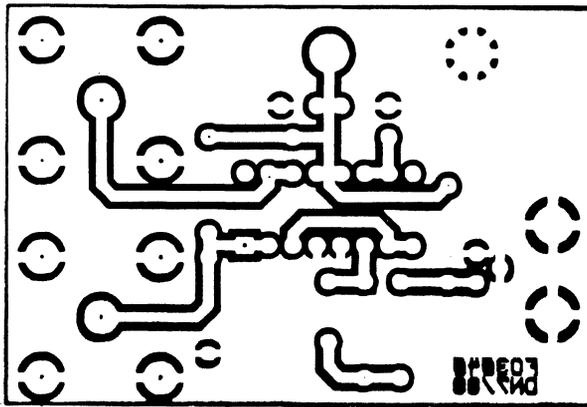
3c. Bottom View

Figure 3. Printed Circuit Board Layout

A 50Mb/s LED Driver for Fiber Optic Communications   AB1121
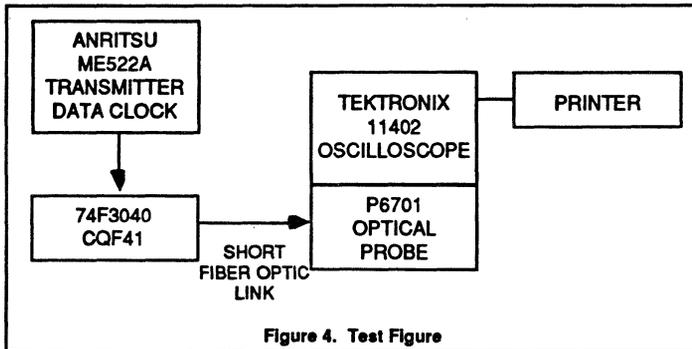
Figure 4. Test Figure
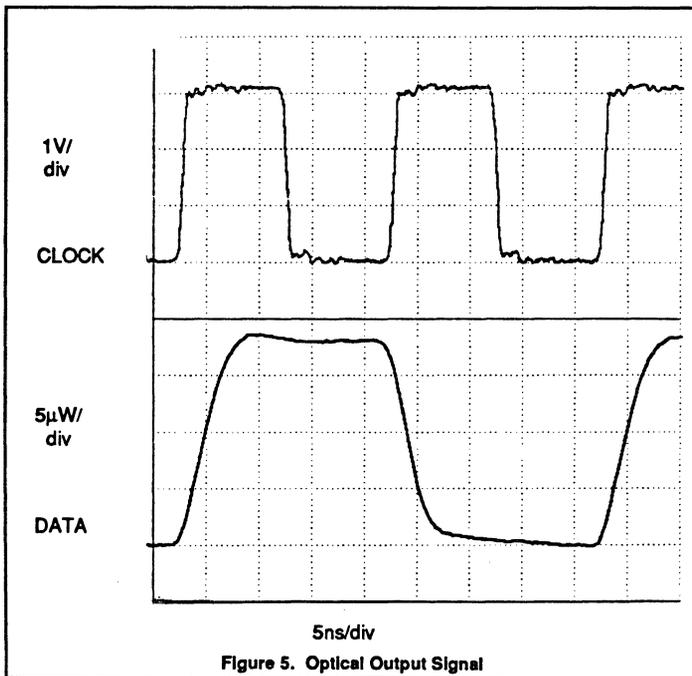
Figure 5. Optical Output Signal

Rise	Fall	Frequency	Main Size	
			5ns/div	
3.964ns	4.041ns	24.97MHz	Main Pos	
			-26ns	
Width	Peak-Peak	RMS	Remove Wfm 2	Pan/ Zoom
19.55ns	18.74µW	17.34µW	Avg (L4) Main	Off

Signetics

FAST Products

FEATURES

- 30Ω line driver
- 160mA output drive capability in the Low state
- 67mA output drive capability in the High state
- High speed
- Facilitates incident wave switching
- 3nh lead inductance each on V_{CC} and GND when both side pins are used

DESCRIPTION

The 74F3040 is a high current Line Driver composed of two 4-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 'F3040 is 67mA source and 160mA sink with a V_{CC} as low as 4.5V. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30 ohms. This is applicable with any combination of outputs using continuous duty. The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices, Performance may be improved by full or partial line termination.

FAST 74F3040
30Ω Line Driver

Dual 4-Input NAND 30Ω Line Driver

Product Specification

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F3040	3.7 ns	7.5 mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic DIP	N74F3040N
16-Pin Plastic SO	N74F3040D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{na}, D_{nb}, D_{nc}, D_{nd}	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{Q}_n$	Data output	3350/266	67mA/160mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

D_{0a} [1]	[16] NC
D_{0b} [2]	[15] D_{0d}
$\overline{Q}_0$ [3]	[14] D_{0c}
GND [4]	[13] V_{CC}
GND [5]	[12] V_{CC}
$\overline{Q}_1$ [6]	[11] D_{1d}
D_{1a} [7]	[10] D_{1c}
D_{1b} [8]	[9] NC

TOP VIEW

LOGIC SYMBOL

1 2 14 15 7 8 10 11

D_{0a} D_{0b} D_{0c} D_{0d} D_{1a} D_{1b} D_{1c} D_{1d}

Q_0 Q_1

3   6

V_{CC} = Pin 12, 13
GND = Pin 4, 5
NC = Pin 9, 16
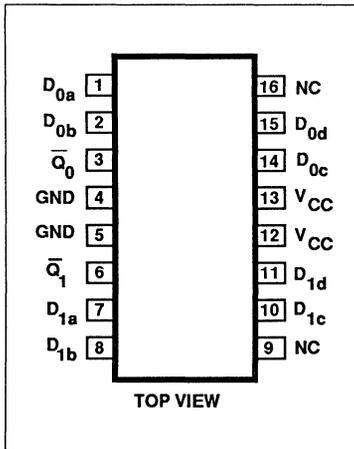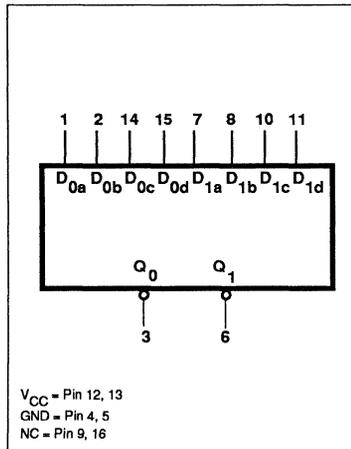
LOGIC SYMBOL (IEEE/IEC)

1
2
14
15
7
8
10
11

& ▷

3

6
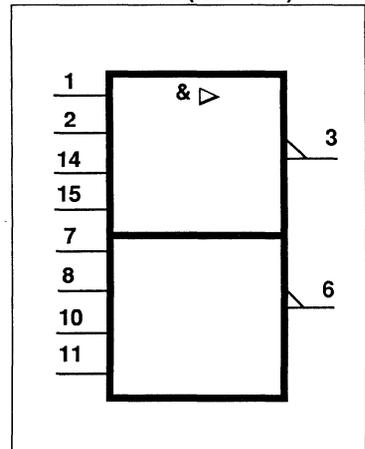
30Ω Line Driver

FAST 74F3040

LOGIC DIAGRAM

V_{CC} = Pin 12, 13
GND = Pin 4, 5
NC = Pin 9, 16
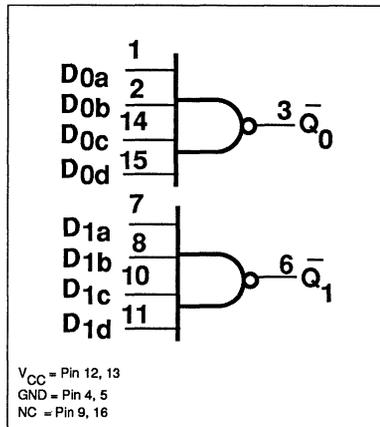
FUNCTION TABLE

INPUTS				OUTPUT
D_{na}	D_{nb}	D_{nc}	D_{nd}	$\overline{Q}_n$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't carre

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-67	mA
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	0		70	°C

30Ω Line Driver

FAST 74F3040

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OH} = -45mA	±10%V_{CC}	2.5			V
			I_{OH1} = -67mA[3]	±5%V_{CC}	2.7			V
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.42	0.55	V
			I_{OL1} = 160mA[4]	±5%V_{CC}			0.80	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V					-0.6	mA
I_O	Output current[5]	V_{CC} = MAX, V_O = 2.25V			-80		-180	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			2.0	4.0	mA
		I_{CCL}				14	20	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH1} is the current necessary to guarantee the Low to High transition in a 30 ohm transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30 ohm transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_{na}, D_{nb}, D_{nc}, D_{nd} to $\overline{Q}_n$	Waveform 1	2.5 1.0	4.5 2.5	6.5 4.5	2.5 1.0	7.0 5.0	ns

AC WAVEFORMS

Waveform 1. Propagation Delay for Inputs to Outputs

NOTE: For all waveforms, V_M = 1.5V.
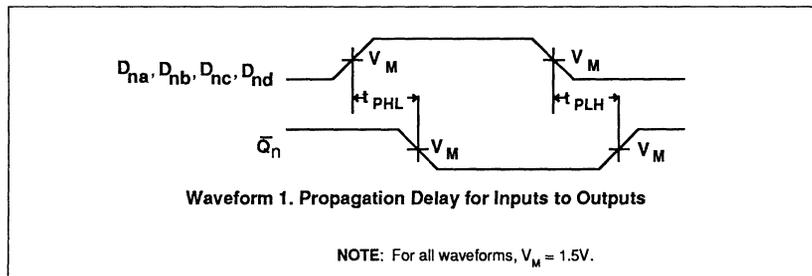
30Ω Line Driver

FAST 74F3040

TEST CIRCUIT AND WAVEFORMS
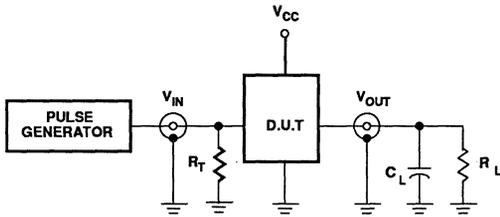
Test Circuit For Totem-Pole Outputs

$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
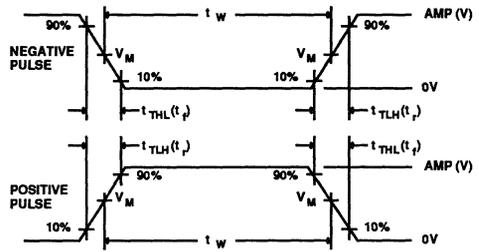
FAMILY	INPUT PULSE REQUIREMENTS					
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

Signetics

FAST 74F5300/NE5300

LED Driver

Objective Specification

Communications and Industrial Products Group

DESCRIPTION
The 74F5300/NE5300 is an LED driver designed for use in fiber optics links.

The TTL input buffer accepts TTL data. A Logic High on the Enable pin enables the buffer to drive the output driver ampliier. The output driver ampliier is capable of sourcing more than 60mA and sinking more than 120mA from low impedances.

The high current output driver has been designed to deal with transmission line effects of high speed switching systems with fast rising and falling edges. The performance of the system can be enhanced by matching impedance at the output for proper termination.

FEATURES
- **TTL inputs**
- **Output enable control**
- **Single supply**
- **High current source and sink capability**

APPLICATIONS
- **High speed serial data communication**
- **Fiber optic data links**
- **Local area and metropolitan area networks**
- **Digital television**
- **PBX systems**

ASSOCIATED PRODUCTS
- **NE5210, NE5211, NE5212 transimpedance amplifiers**
- **NE5214, NE5217 postamplifiers with link status indicator**

PIN CONFIGURATION

D Package

V_{CC}	1	8 V_{CC}
ENABLE	2	7 GND
INPUT	3	6 OUTPUT
GND	4	5 GND

TOP VIEW
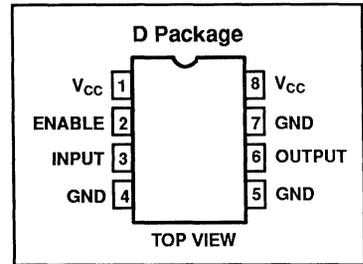
ORDERING INFORMATION

DESCRIPTION	VOLTAGE/TEMPERATURE RANGE	ORDER CODE
8–Pin Plastic SO	$V_{CC} = 5V \pm 10\%$; $T_A = 0$ to $+70°C$	74F5300D/NE5300D

BLOCK DIAGRAM
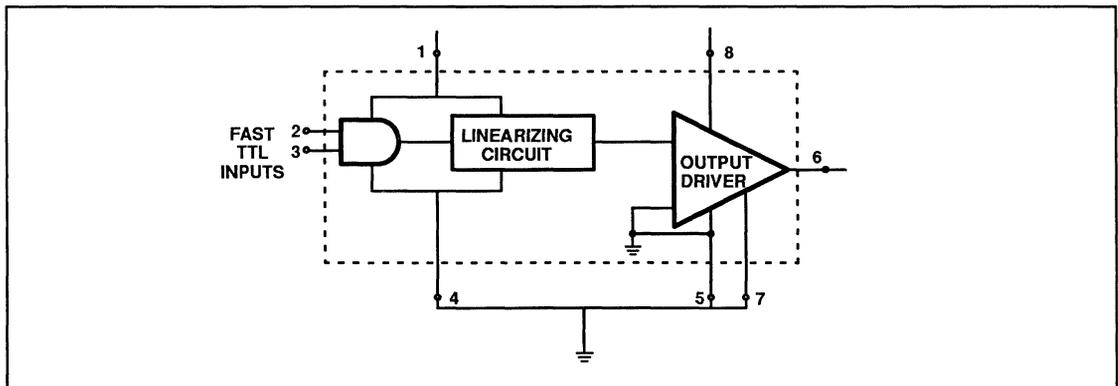
LED Driver

74F5300/NE5300

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	320	mA
T_A	Operating ambient temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
θ_{JA}	Thermal impedance		

RECOMMENDED OPERATING CONDITIONS Typical values are at V_{CC} = 5V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply voltage range		4.5	5.0	5.5	V
V_{IH}	Input current range		2.0			V
V_{IL}	Input voltage to the driver output stages				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High level output current[1]				−67	mA
I_{OL}	Low level output current				120	mA
T_A	Operating ambient temperature range		0		70	°C

NOTES:
1. The device is not short–circuit protected.

DC ELECTRICAL CHARACTERISTICS T_A = +25°C; V_{CC} = 5V; C_L = 50pF; R_L = 100Ω; unless otherwise stated.

V_{OH}	High level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = MAX					
V_{OL}	Low level output current	V_{CC} = MIN V_{IL} = MAX V_{IH} = MIN	I_{OL} = 100mA	±10%V_{CC}		0.42	0.55	V
			I_{OL} = 120mA	±10%V_{CC}		0.45	0.60	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			−0.73	−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	μA
I_{IH}	High level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = MAX			2.0	4.0	mA
		I_{CCL}				8.0	12	mA

LED Driver

74F5300/NE5300

AC ELECTRICAL CHARACTERISTICS $T_A = +25^\circ C$; $V_{CC} = 5V$; $C_L = 50pF$; $R_L = 100\Omega$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
t_{PLH}	Propagation delay D to Q	Waveform 1	2.5	3.6	3.5	ns
t_{PHL}			2.5	3.6	3.5	ns
d_{TPW}	Pulse width distortion			0.4		ns
t_R	Rise time 10% to 90%	Test circuits and waveforms		1.2		ns
t_F	Fall time 90% to 10%	Test circuits and waveforms		1.2		ns

AC WAVEFORMS

NOTE: For all waveforms, $V_M = 1.5V$

Propagation Delay for Input to Output

TEST CIRCUIT AND WAVEFORMS

Test Circuit

$V_M = 1.5V$
Input Pulse Definition

DEFINITIONS
R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns

LED Driver   74F5300/NE5300

TYPICAL APPLICATION DIAGRAM

Signetics

Linear Products
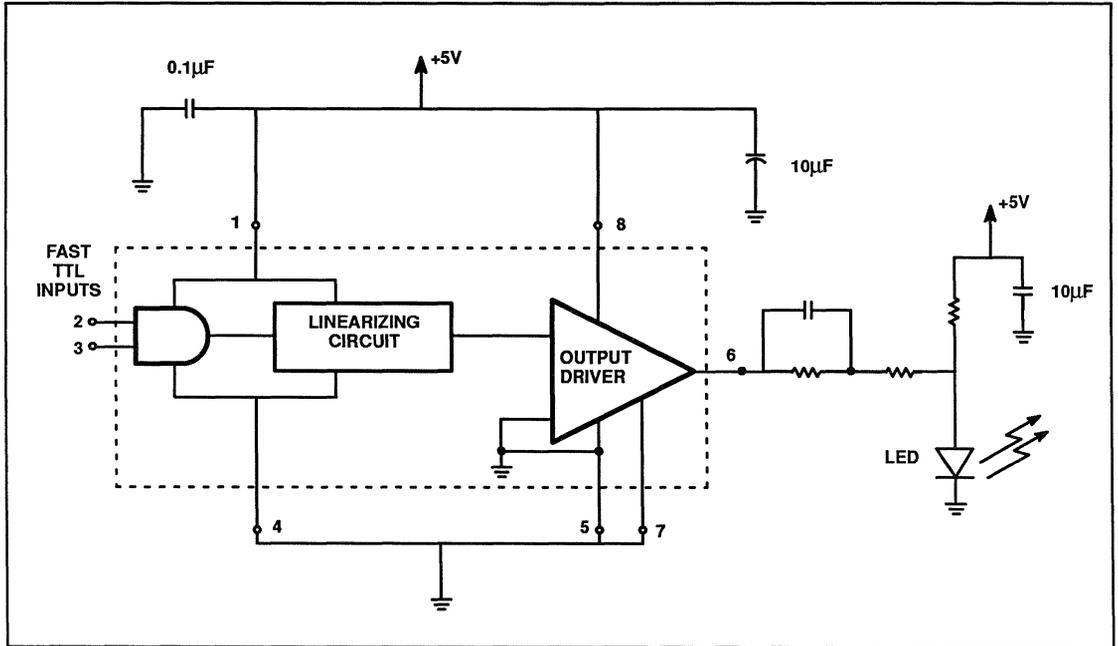
Section 3
Fiber Optic Receiver, Data Recovery

INDEX

A LOW COST 100M BAUD FIBER OPTIC RECEIVER

William D. Mack, Robert G. Meyer, and Ki Y. Suh

LINEAR DIVISION

ABSTRACT

A two-chip receiver with minimum external component count has been designed for low cost fiber optic applications to 100M Baud (50MHz). The receiver is divided into pre- and post-amplifier ICs for stability reasons. The preamplifier IC features low noise with a differential transresistance design. The post-amplifier IC incorporates an auto-zeroed first stage with noise shaping, a high-gain symmetrical-limiting amplifier, and a matched rise/fall time TTL output buffer. A wide-band full-wave rectifier functions as a link-status indicator. To insure stability a surface mount (also called Small Outline {SO}) package is used. To maintain low cost these ICs are fabricated in a standard volume-production bipolar process using 2μ lithography and achieving 8GHz F_T's.

Introduction/System Overview

The merits of fiber optics as a local-area network (LAN) medium are well known: ease of installation, light weight, noise immunity, security and high speed[1]. However, the installed base of fiber optic LANs is small due to the recent emergence of the technology and the lack of suitable low-cost electronics[2]. Receiver and transmitter designs using discrete components have been used for many systems[3] but are often complicated to use. Board-level products using off-the-shelf ICs greatly simplified the system designer's task, but these solutions were for low data rates (20M Baud) and were still costly[4]. IC designs up to 200M Baud have been demonstrated, but require specialized packaging and are intended for captive markets.[5]

This paper will focus on low-cost electronics for the receiver function in the 1 – 100M Baud range. In a typical application (Figure 1), a low cost PIN (Positive-Intrinsic-Negative) diode such as the Hewlett Packard HFBR2208 or United Technologies HR026 receives an optical pulse from a fiber optic cable typically employed in Local Area Network applications.

FIBER OPTIC RECEIVER

Figure 1. Low Cost Fiber Optics Receiver

The received signal in the – 35dBm optical (average) to – 9dBm range is converted into a small unipolar current by the PIN diode. The PIN diode then feeds its signal current to a preamplifier such as the **NE5212**. This low-noise preamp provides single-ended to differential conversion (for noise immunity), wide bandwidth, and good supply rejection. Application information for this part has appeared in last year's FOCLAN paper "A Low-Cost, High-Performance, Monolithic Trans-Impedance Preamplifier for Fiber Optic Receivers" by Burgyan et al[6].

The preamplifier output is fed to a high-gain limiting amplifier, simply known as the *post amp*. The receiver is divided into pre- and post-amplifier ICs so that package and board parasitic capacitances will not make the system oscillate. The post amp must provide gain with good linearity for small signals and limiting for large signals. Typically, inputs between 2mVPP and 800mVPP must be handled.

The **NE5214/NE5217** postamplifiers are low cost ICs that provide up to 60dB of gain at 50MHz to bring milli-volt level signals up to TTL levels. The postamplifier IC incorporates an auto-zeroed first stage with noise shaping, a high-gain symmetrical-limiting amplifier, and a matched rise/fall time TTL output buffer. A secondary amplifier chain functions as a link-status indicator. To insure stability a surface mount (also called Small Outline {SO}) package is used with the additional benefit of low automated assembly cost.

NE5214/NE5217 Block Diagram

The circuit is divided into eight amplifier blocks (Figure 2). The forward path is made up of a cascade of limiting stages: A1 – A2 – A8. This is the main signal path with A1 bringing the differential input signal up to a workable level and A2 squaring this into an ECL signal. A8 then provides a Schmitt Trigger function and a matched rise/fall time TTL output. The difference between the NE5214 and NE5217 is that the pins between A2 and A8 are accessible in the NE5217 only. This means a larger package (24 pins versus 20 pins), but allows the Schmitt trigger to be operated for Non-Return to Zero (NRZ) input coding.

The A3 – A4 – A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It provides a TTL "FLAG" signal (by way of amplifier A4) when the input is below a user adjustable threshold. It also drives an external LED to the ON state when the input signal is above the threshold. In a typical application the FLAG output is tied back to the TTL input 'JAM' (amplifier A6). This forces the overall chip output 'VOUT' into a Low state when no signal is present. This is a link-status function to detect broken fibers, low signal, inactive transmitters, etc.

FIBER OPTIC POST-AMP

NE5214

Figure 2. NE5214 in an SO-20 Package

A1 Amplifier

A1 is broken into two low-gain stages in cascade to maintain signal linearity at low levels (Figure 3). The first stage provides most of the amplification as well as providing a limiting function for large signals. Local series feedback is used to broadband and linearize the second stage. The amplifier can handle signals from 1mVPP to 1VPP, a 60dB range. Limiting for large signals is an inherent feature with the bipolar differential amplifier stages used. The overall amplifier has 20dB gain for small signals, decreasing to 2dB attenuation for 1VPP signals. Fully differential inputs and outputs are used to provide noise immunity to other high speed/large amplitude signals present on the same chip and/or board. Bandwidth is typically 75MHz with two real poles providing noise filtering above 50MHz.
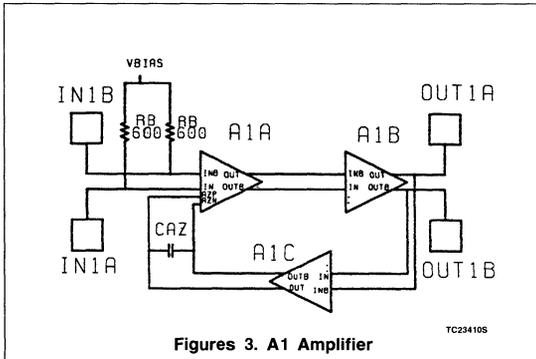
Figures 3. A1 Amplifier
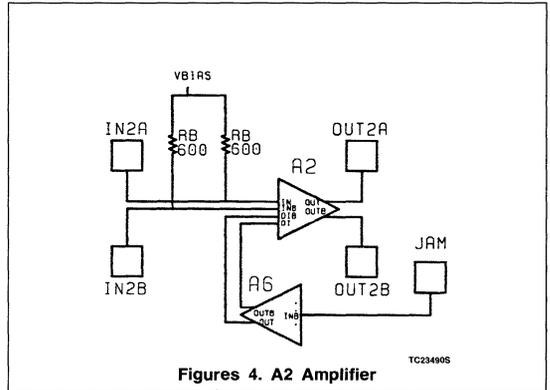
Figures 4. A2 Amplifier

A special Auto Zero (AZ) loop allows the NE5214/17 to be *directly* connected to the NE5212 preamplifier without coupling capacitors. This AZ loop cancels the NE5212 DC offset, NE5214/17-A1 offset, and more importantly the signal dependent offset created by the unipolar (optical) to bipolar (electrical) conversion in the PIN diode/preamplifier system. The AZ capacitor must be 1000pF or more to compensate this negative feedback loop. The AZ loop sets a zero in the frequency response to the A1 amplifier and this time constant must be less than one third of the shortest time between successive edges of the signal. To disable the AZ function the AZ pins can be shorted together. In that case the signal inputs must be AC coupled, and the amplifier will provide its own DC biasing through resistors RB.

A2 Amplifier

The A2 amplifier is a two-stage low-offset differential in/out amplifier with 38dB of gain (Figure 4). A2 is operated without feedback and thus functions as a comparator/limiter. Input offset is less than 1mV and the bandwidth is approximately 100MHz. The inputs may be DC driven from the A1 amplifier or NE5212, or AC coupled from any source. A unique feature of the A2 circuit is the "JAM" function. The A2 output is jammed into a logical Low state (OUT2A = Low, OUT2B = High) when the user controllable JAM pin is taken High. When JAM is Low, A2 functions as an amplifier. This JAM function provides a means to eliminate output *Jabber* for low or no signal conditions. In conjunction with the FLAG signal this provides the overall receiver with a squelch or mute function.

A1 to A2 Interface

Conveniently located pins allow direct coupling of A1 to A2 for systems where only modest sensitivity is required. For maximum sensitivity some sort of noise filtering can be applied between A1 and A2. All filtering should be done differentially to maintain power-supply and common-mode rejection as high as possible. A2 outputs should be well shielded from A1 inputs to prevent coupling and oscillation. Figure 5 shows a simple RC lowpass filter combined with coupling capacitors that provides bandpass action around 10MHz. This will improve the sensitivity for 20M Baud applications (*Ethernet on Fiber*). Optimal filtering may include LC networks or equalization filters, depending on the application. Care must be taken to load A1 and A2 symmetrically to prevent either amplifier from oscillating. Minor imbalances may also produce slew rate distortions leading to eye pattern closure (pulse width distortion). These asymmetries will lead to higher Bit Error Rate (BER) for a given input optical power.
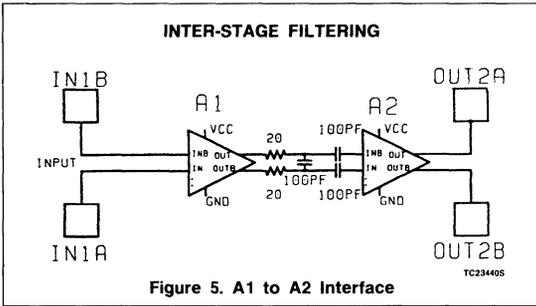
Figure 5. A1 to A2 Interface

A3 Peak Detector

The inputs from A2 are also routed to the full-wave rectifier A3 (see Figure 6). The greater of the positive or negative peak of the applied signal is then compared to a user defined threshold. This difference signal is then amplified further, finally charging the internal 10pF capacitor C_{D1}. The threshold is set by the user via a resistor from 'THRESH' to VCC. An internal threshold (at A2's input) is developed as

$$VTH = [(VCC - 0.7V)/(RTH \text{ parallel } 67K)] * 250$$

To refer this threshold to the input of A1 divide the threshold by a factor of ten (20dB).

The squared-up difference signal between the input and threshold charges the internal C_{D1} capacitor to an ECL logic High (0.8V below VCC) when sufficient input-signal amplitude is present.

LINK STATUS CIRCUITRY
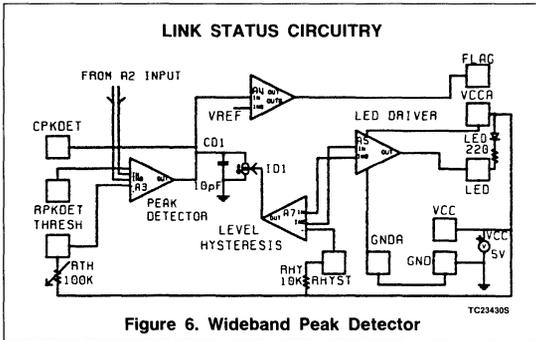
Figure 6. Wideband Peak Detector

Under no-signal conditions C_{D1} will discharge via an internal current source I_{D1}. The discharge current is given as

$$I_{D1} = (VCC - 0.7V)/(Rpeak \text{ parallel } 67K)$$

Therefore the user can control the decay time of the peak detector. This is important when bursty data is present, and when framing and preambles are used. The delay through the peak detector path must be short enough to catch the first data bits transmitted, but not so fast as to lose the final data bits of a frame. Further user control of the peak detector is achieved by supplementing the internal capacitor with external capacitance (ex. 100pF). This gives better immunity to the peak detector system to external noise sources, glitches, etc, so long as the capacitor is returned to a quiet ground.

Following A3 is a comparator A4 to sense whether signal is present, ($V_{CD1} > 3.7V$), or signal is absent ($V_{CD1} < 3.7V$). A4 then outputs a TTL compatible 'FLAG' signal (fanout of two) with 'FLAG' High warning of a low/no signal condition. Additionally, A4 signals A5 which

produces pull down current for an external LED. This output is an open collector with 125 ohms of limiting resistance that turns the LED *ON* when signal is present. External resistance may be added in series with the LED (pulled up to VCC) to lower the LED current/brightness.

To avoid jitter in the operation of the peak detector a user controllable hysteresis is provided. The hysteresis is approximately

Hysteresis = 1.42 [(VCC - 0.7V)/(RHYS parallel 67K)]

Grounding 'RHYST' will disable this function, while leaving 'RHYST' open will apply an insignificantly small amount of hysteresis.

A8 Schmitt Trigger/TTL Output Stage

Input Section In the NE5214 the outputs from A2 are internally connected to the Schmitt trigger input of A8. However, this DC coupling renders the Schmitt trigger inoperative, and the input section of A8 functions as a unity gain amplifier. The NE5217 provides pin outs for the A2 outputs and A8 inputs (see Figure 2). The user has the choice of DC or AC coupling between these amplifiers. If DC coupled, the operation will be essentially the same as the NE5214; however noise pickup may be more severe. AC coupling A2 to A8 will invoke the Schmitt-trigger function, thereby providing immunity to noise-induced output-switching.

Correct setting of the full-wave rectifier threshold is imperative to eliminate this unwanted output. Also, the Schmitt trigger allows the last state (digital data at this point) to be held indefinitely when no signal is present. This is useful in non-50% duty cycle systems such as NRZ. Holding the last state and decreasing the noise-induced switching has a sensitivity penalty however. The threshold for switching A8 is approximately 20mV for DC coupling and 400mV for AC coupling (half of ECL swing).

Output Section The A8 output stage converts internal differential ECL signals to a single ended TTL output. The output is designed for a minimum fanout of five (5). Optimization of rise and fall time was a prime design goal. Mismatches in rise and fall times were minimized to eliminate pulse width distortion that would compromise eye pattern openings and Bit Error Rate (BER). Rise/fall times are typically 3ns ± 0.5ns. For best performance the output should be loaded with less than 10pF. The output will drive up to 100pF, but square-wave response will include overshoot.

Power Supplies

Separate digital and analog power supplies are employed to minimize high amplitude digital signals from corrupting the low level analog signals. 'VCC' and 'GND' are used for low level signals and must be separated from 'VCCA' and 'GNDA', which are used for the main TTL output 'VOUT' as well as the 'LED' and 'FLAG' outputs.

Technology

The synergy of MOS processing techniques and bipolar transistor performance has led to the development of a truly rugged, high performance *bipolar* process. Conservative 2μ design-rules with shallow (non-poly) emitters yield 8.5GHz F_T with an LV_{CEO} greater than 6 volts. Outstanding performance, reliability, and repeatability are key features of this technology. Inclusion of low series-resistance bipolar diodes provides superior electro-static discharge protection. A die photograph of the postamplifier IC is shown in Figure 7.

Package technology plays a dramatic role in the operation of these wide-band, high-gain ICs. The equivalent voltage gain of the NE5212/ NE5214 system is approximately 100dB, with an overall bandwidth of 50MHz. This is an astronomically high 5000GHz of gain-bandwidth that must be handled on one board. Separation of the system into two chips was necessary *independent* of IC technology. Use of surface-mount (SO) packages allowed parasitic capacitance to be controlled to the level of 10fF input-to-output on each chip. Physical separation between chips was also required for system stability.
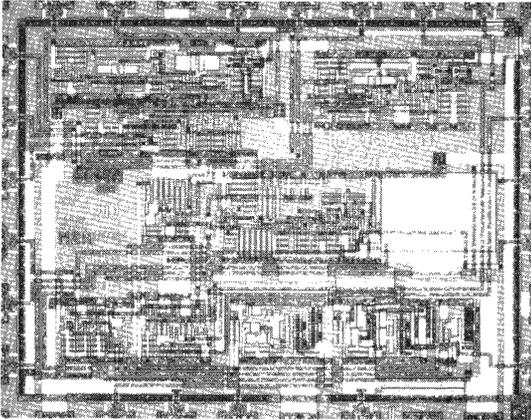
Figure 7. Die Photograph of Postamplifier

Figure 8. Eye Pattern at 50M Baud

System Performance

With the **NE5212** preamplifier and **NE5214/17** postamplifiers many optical receivers can be designed. A simple system using the HFBR2208 PIN diode (λ = 820nm) and a NE5212 directly coupled to a NE5214 has been operated at 100M Baud. Sensitivity is −26.0dBm for a Bit-Error-Rate (BER) of 10^{-9} or better using a 2^{23}-1 Psuedo-Random Bit-Stream (PRBS) with binary NRZ encoding. Operation at 50M Baud showed a sensitivity of −28.6dBm under the same conditions (Figure 8). Less deterioration of the eye pattern is seen. Noise filtering for 20M Baud applications would lead to further improvements in sensitivity. Experienced users have reported up to −36.5dBm sensitivity with 26dB dynamic range using these chips with optimal equalization.

Conclusion

A *low-cost* two-chip fiber optic receiver for 1M–100M Baud applications has been designed in a standard bipolar process. The system architecture is flexible and controllable by the user. Depending on the application, sensitivity in the −25dBm to −35dBm range has been achieved. Surface-mount packages have been employed for their low parasitic capacitance and low automated assembly costs. Power supply requirements are 26mA for the preamp and 40mA for the post-amp from a single 5V source. External component count has been minimized by an on-chip auto-zero loop. Electrostatic Discharge (ESD) protection is employed on all pins to provide *greater* than 2000V protection using the Human Body Model. This combination of features is unequaled by any commercially available fiber optic receiver.

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Signetics

AB1432
50Mb/s Fiber Optic Receivers

Application Brief

Linear Products

Author: G. Lane

INTRODUCTION

This application brief describes the use of four Signetics devices specifically designed for use as fiber optic receiver components.

In order to simplify the design process for a prospective user, two typical fiber optic receivers were designed, built, and tested. The design criteria for these receivers is a maximum of 50Mb/s data rate non-return-to-zero (NRZ) format, optical wavelength of 850nm, and readily available components.

The two receivers are topologically similar; the difference between them is in performance, which will be pointed out in the specific discussion of each receiver. For ease of explanation, two sets of schematic diagrams are used. The first is a signal-only diagram used in the description of the circuit operation. The second, and complete set, shows the peripheral components and the power supply decoupling networks.

The choice of which preamplifier to use with which postamplifier is determined by the task to be accomplished. Selections were made for the two test receivers: One receiver combination (NE5211/NE5214) was chosen for long haul, i.e., greatest gain, and a short (2^7-1)-Pseudo Random Bit Sequence (PRBS). The other combination (NE5210/NE5217) was chosen for short haul, longer (2^{23}-1) PRBS operation. That is not to say other combinations cannot exist; the choice is made dependent upon the application. The optical source used in the evaluation of the receivers is the transmitter, described in AB1121. SMA connectors were used throughout, with the exception of the step attenuator (see Figure 1 for complete test set-up description). The test set-up shown in Figure 1 provides measurement capability of optical power, Bit-Error-Rate (BER), and eye pattern (duty cycle distortion).
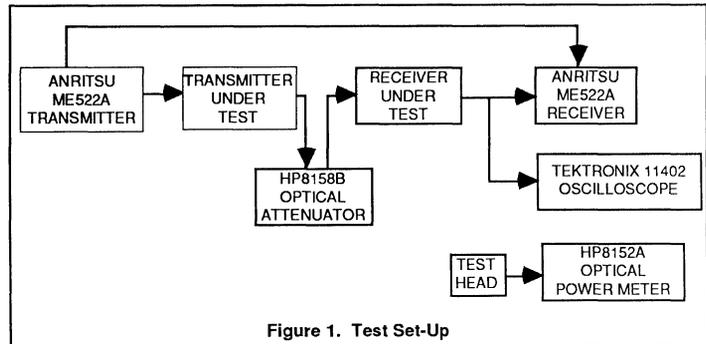
Figure 1. Test Set-Up

RECEIVER 1

The first receiver (Receiver 1) is shown in Figure 2. The optical signal is coupled to the PIN diode. Current flowing in the diode also flows into the input of the NE5211 preamplifier. The preamplifier is a fixed gain block that has a 28kΩ differential transimpedance and does a single-ended to differential conversion. With the signal in differential form, greater noise immunity is assured. The second stage, or postamplifier (NE5214), in-

cludes a gain block, auto-zero circuit, detection and limiting. The auto-zero circuit allows DC coupling of the preamplifier and the postamplifier and cancels the signal dependent offset due to the optical-to-electrical conversion. The auto-zero capacitor must be 1000pF or greater for proper operation. The peak detector has an external threshold adjustment, R_{TH}, allowing the system designer to tailor the threshold to the

individual's need. Hysteresis is included to minimize jitter introduced by the peak detector, and an external resistor, R_{HYS}, is used to set the amount of hysteresis desired. The output stage provides a single-ended TTL data signal with matched rise and fall times to minimize duty cycle distortion. The decoupling networks are shown in the complete schematic, Figure 3. Because this receiver has gain >100dB and very wide bandwidth, great care must be taken in both the physical layout and decoupling of the stages.

The printed circuit layout shown in Figure 4 may not be optimum; it serves only to demonstrate capability. For higher performance, a different layout and shielding between the detector leads and the preamplifier, and between the preamplifier and the post amplifier, may be in order. The decoupling networks

Figure 2. Receiver 1

50Mb/s Fiber Optic Receivers   AB1432

cannot be disposed of; the value of the passive components may change to fit a particular need, but overall they are necessary. Another feature of all of the devices is the grounding pins which are available to separate input grounds and output grounds, high level grounds and low level grounds. These grounds need to be given careful consideration when laying out a circuit.

Results

Receiver 1 was built using the layout shown in Figure 4. Input power (P_{IN}) (minimum) was measured for PRBS lengths of 2^7-1 and 2^{23}-1 with the following conditions: BER = 10^{-9}, R_{TH} = 39K, R_{HYS} = 5K;

The results obtained were:

P_{IN} dBm optical = -32dBm for PRBS of 2^7-1

P_{IN} dBm optical = -20dBm for PRBS of 2^{23}-1

Actual eye patterns are shown in Figure 5a and b, for PRBS of 2^7-1, P_{IN} = -32dBm and PRBS of 2^{23}-1, P_{IN} = -20dBm, respectively.

To demonstrate threshold and hysteresis, a pair of curves were generated by measuring input power required for the signal to fall just below the threshold (signal loss), then measuring P_{IN} to just exceed the threshold (regain signal) for different valves of R_{TH}. The value of R_{HYS} is kept at a constant value of 5kΩ. These curves are shown in Figure 6.

Receiver 2

Receiver 2, Figure 7, is similar to Receiver 1, topologically. Optical power is coupled to the PIN photodetector diode, which is directly coupled to the NE5210. The NE5210 is a fixed 7kΩ differential transimpedance gain block with a differential output for noise immunity. The post amplifier, NE5217, is DC coupled to the preamplifier. The NE5217 also has an auto-zero circuit allowing direct coupling and cancellation of signal dependent offsets. The peak detector has its threshold externally adjustable by means of R_{TH}, and hysteresis for detector jitter reduction is adjustable using R_{HYS}. Curves are available in the data

sheets for both R_{TH} and R_{HYS}. The NE5217 has a built-in Schmitt trigger, which requires coupling, capacitors, C_{S1} and C_{S2} as shown in Figure 7. The Schmitt trigger allows this device to function with longer PRBS NRZ signals by holding the last state until a change is made. The penalty is that an internal threshold is moved from 20mV to 400mV. The complete schematic is shown in Figure 8. The discussion of grounding and layout for Receiver 1 holds true for Receiver 2. A well thought out layout will produce superior results.

Results

Receiver 2 was built using the layout shown in Figure 9. The same measurements were made as with Receiver 1. Input power minimum was measured for PRBS lengths of 2^7-1, and 2^{23}-1 with BER = 10^{-9}, R_{TH} = 39K and R_{HYS} = 5K.

The results obtained were:

P_{IN} dBm optical = -30dBm for PRBS of 2^7-1

P_{IN} dBm optical = -21dBm for PRBS of 2^{23}-1

The actual eye patterns are shown in Figure 10a and b, for PRBS of 2^7-1 and 2^{23}-1, respectively.

The curves showing power input (P_{IN}) required for the signal to fall just below the threshold (signal loss) and P_{IN} required to just exceed the threshold (regain signal) for different values of R_{TH}, are shown in Figure 11. The value of R_{HYS} is kept at a constant value of 5K.

NOTE: Recall that the transimpedance of the NE5210 is 1/4 the transimpedance of the NE5211 when comparing the results.

CONCLUSION

Two 50Mb/s fiber optic receivers were presented along with full schematic diagrams and printed circuit layouts. Individual circuit descriptions were given, along with suggestions of how further performance improvement could be gained. Performance characteristics were shown for each circuit under actual operating conditions.

NOTE: The available bandwidth of both receivers is far greater than necessary for the applications shown. Capacitor C_1, shown in all schematic diagrams, serves to limit the overall bandwidth to 60MHz.

R1:	100Ω	SURFACE MOUNT	
R2:	220Ω	±5%	1/8W
R3:	47kΩ	±5%	1/8W
R4:	5.1kΩ	±5%	1/8W
C1:	47µF	±20% 16V	TANTALUM
C2, 4 , 6, 11, 13:	.01µF	CHIP CAP	
C3, 10 ,12:	10µF	±20% 16V	TANTALUM
C5:	1.0µF	CHIP CAP	
C8, 14 ,15:	.1µF	CHIP CAP	
L1, 2, 3:	10µH	INDUCTOR	
D1:	LED		
PHOTO DIODE:	AMPEREX - BPF31		
SMA CONNECTOR (1):	E.F. JOHNSON		
TURRET TERMINALS (2)			

50Mb/s Fiber Optic Receivers

AB1432

GND   +5V

TTL OUT

Top View

Bottom View

Figure 4. Circuit Board Layout for NE5211/NE5214

50Mb/s Fiber Optic Receivers

500mV/div

5ns/division

a. PRBS of 2^7-1

500mV/div

5ns/division
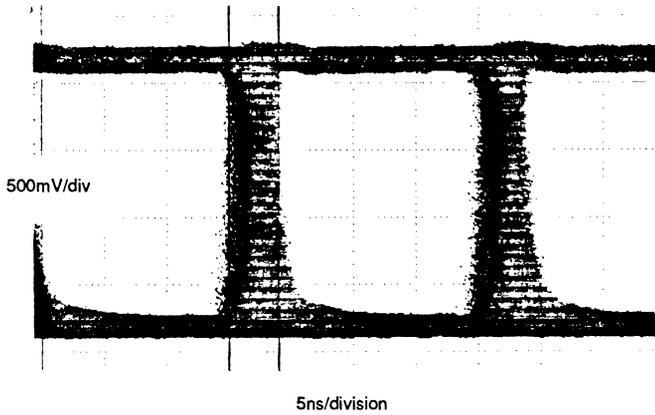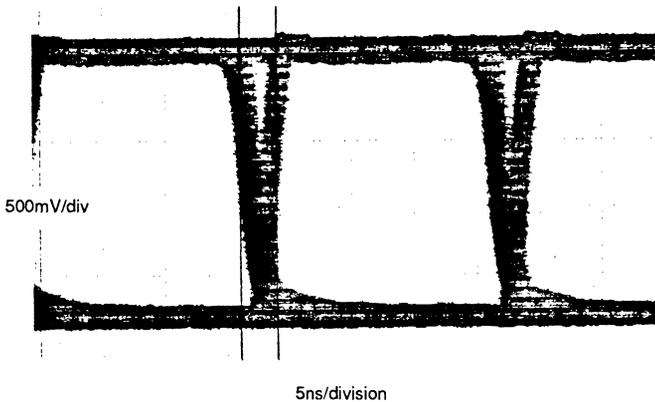
b. PRBS of 2^{23}-1

Figure 5. Eye Patterns for Receiver 1

50Mb/s Fiber Optic Receivers
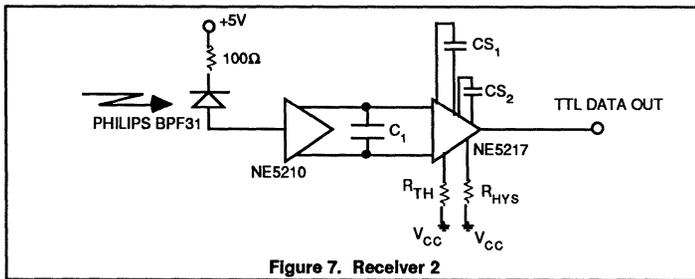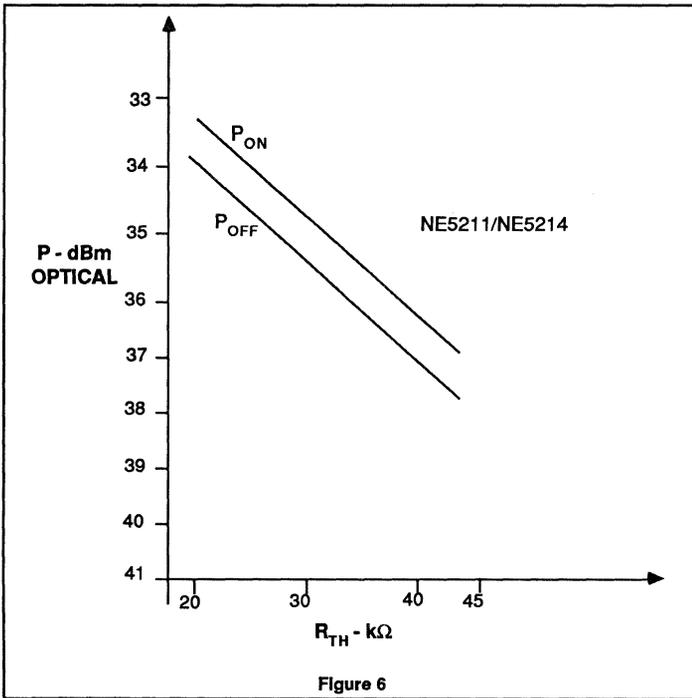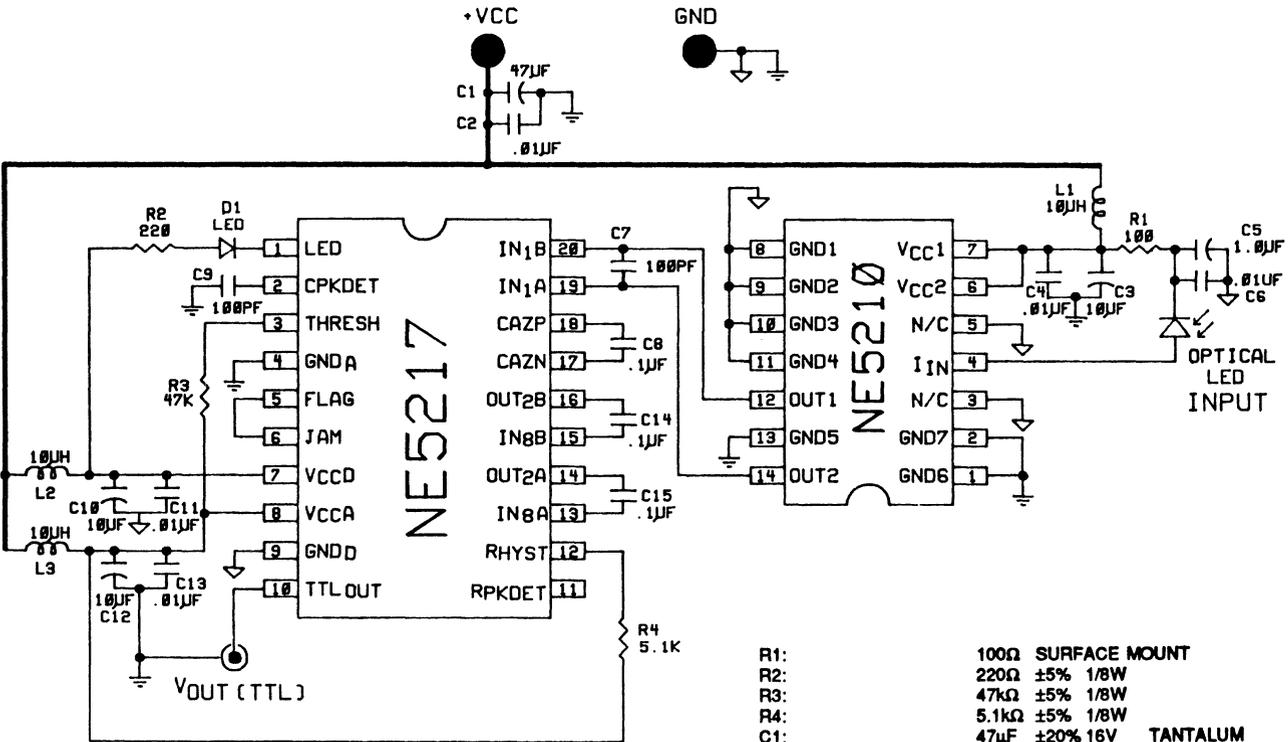
AB1432

Figure 6

Figure 7. Receiver 2

Figure 8.

R1:	100Ω	SURFACE MOUNT	
R2:	220Ω	±5% 1/8W	
R3:	47kΩ	±5% 1/8W	
R4:	5.1kΩ	±5% 1/8W	
C1:	47μF	±20% 16V	TANTALUM
C2, 4 , 6, 11, 13:	.01μF	CHIP CAP	
C3, 10 ,12:	10μF	±20% 16V	TANTALUM
C5:	1.0μF	CHIP CAP	
C8, 14 ,15:	.1μF	CHIP CAP	
L1, 2, 3:	10μH	INDUCTOR	
D1:	LED		
PHOTO DIODE:	AMPEREX - BPF31		
SMA CONNECTOR (1):	E.F. JOHNSON		
TURRET TERMINALS (2)			

50Mb/s Fiber Optic Receivers
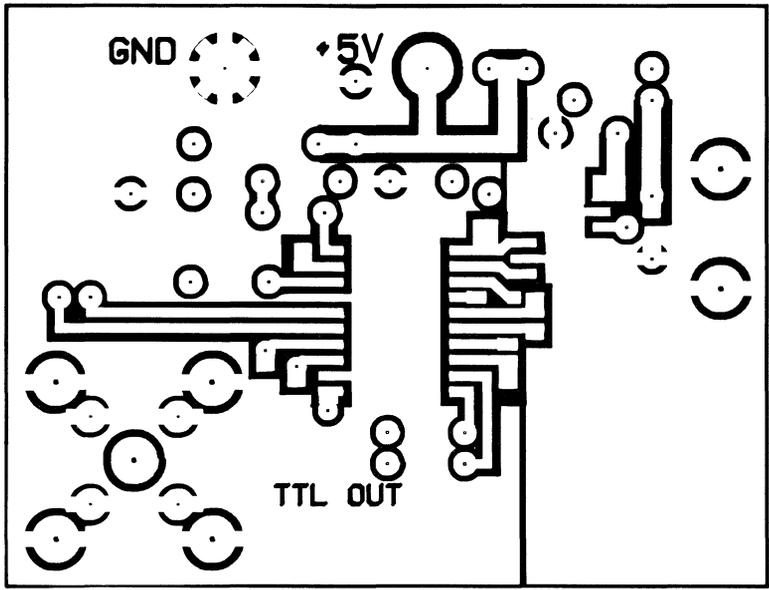
AB1432

Top View
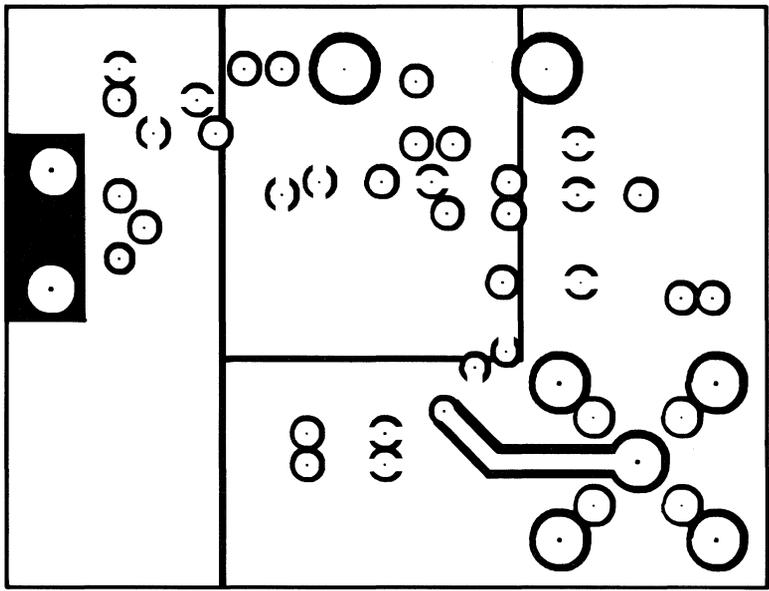
Bottom View

Figure 9. Circuit Board Layout for NE5210/NE5217

50Mb/s Fiber Optic Receivers

500mV/div

5ns/division

a. PRBS of 2^7-1

500mV/div

5ns/division
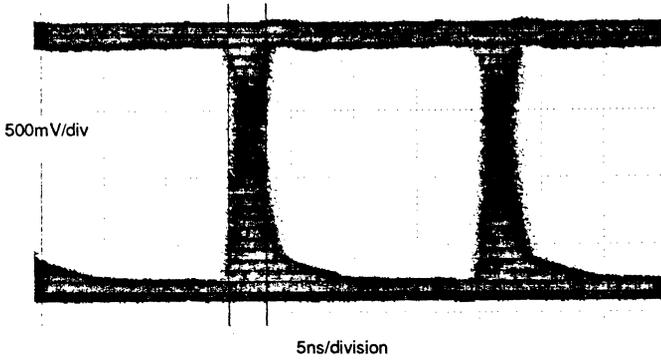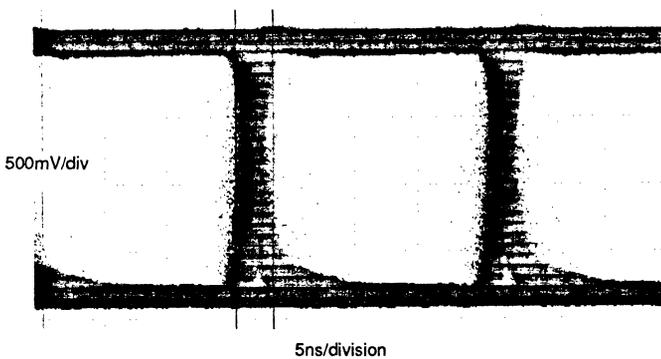
b. PRBS of 2^{23}-1

Figure 10. Eye Patterns for Receiver 2

50Mb/s Fiber Optic Receivers   AB1432

Figure 11
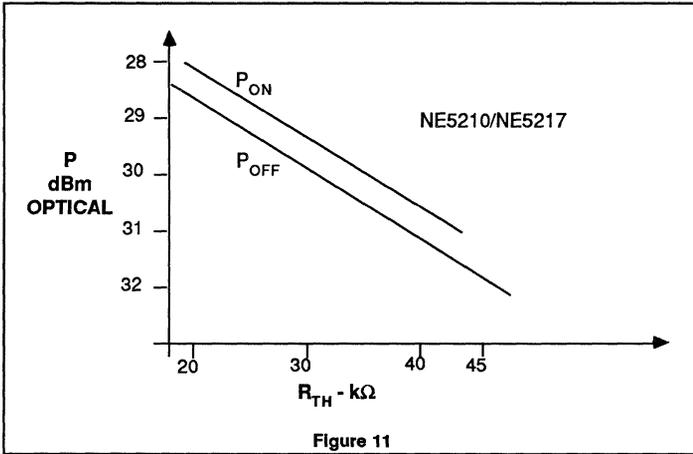
Signetics

AN1435
A Family of Wide Band Low Noise Transimpedance Amplifiers NE5210, NE5211 and NE5212

Application Note

Despite numerous advantages, the relatively high cost of fiber-optic transmission prevented its wide-spread industrial acceptance. High bandwidth-distance products, a prerequisite for cost-effectiveness, could not be achieved with relatively inexpensive components. The latest technological advances on both transmitter and receiver sides, however, are about to change that.

Transmitter
Starting at the transmitter side (Figure 1), the two major problems of the past were the lack of inexpensive, light emitting diode (LED) transmitters, capable of 10 — 20MHz modulation rates, and the compounded problem of cost and reliability of laser diodes, required for large channel capacity, single mode, long-distance systems.

In examining the present status of the fiber-optic industry we observe, however, that new generations of LEDs, used in most *short-range*, multimode transmitters, can achieve wide modulation bandwidths, enabling system designers to develop cost-effective systems. For example, commercially available 820–850 nanometer AlGaAs surface emitting devices have significantly decreased in price and can be used up to and beyond 100MHz (200 MBaud). InGaAsP LEDs can be used in the 1.3μm range. Their highly doped versions can be modulated up to bandwidths of several hundred MHz at the expense of lower output power.

InGaAsP laser diodes can go well beyond 1GHz. Their higher output power and an order of magnitude narrower spectral widths make these devices the ideal choice for *long-range*, very high data rate telecommunication systems.

Receiver
The key to cost effectiveness at the receiver side is the ability to offer monolithic IC building blocks that can match those high transmitter data rates with bandwidth, large dynamic range and low noise. These kinds of IC building blocks weren't readily available in the past. Consequently, system designers had to choose between limiting data rates to below 20 MBaud or using costly hybrid modules.

Signetics' solution to the problem is the introduction of a family of transimpedance amplifiers (TIA). These are the NE5210, NE5211 and NE5212.

Although the real meaning is different, "trans-resistance" and "trans-impedance" are, in

practice, used interchangeably. These names designate that these types of amplifiers are current-driven at their inputs and generate voltage at their outputs. The transfer function is therefore a ratio of output voltage to input current with dimensions of ohms. Since the input is current driven, the input resistance must be low, which means low input voltage swings, no capacitive charge/discharge currents and wide frequency response with a generous phase margin. Alternative approaches to the TIA, such as high input impedance FET preamplifiers with a shunt input resistor, tend to be more bandwidth limited. They exhibit integrating characteristics, and therefore must be equalized by a differentiating second stage to achieve broad frequency response. The integrating input stage, however, is prone to overload with signals that have high low-frequency content. If the amplifier overloads for any reason, the integrated waveform cannot be restored by differentiation and dynamic range suffers despite the low noise characteristics. Since the transimpedance configuration does not have this problem, its superior dynamic range, inherently large bandwidth and compatibility with low cost IC technologies make it an attractive approach.

Transimpedance Amplifier Family
The NE5210, NE5211 and NE5212 TIA is a low noise, wide band integrated circuit with single signal input and differential outputs, ideally suited for fiber optic receivers, both digital and analog, in addition to many other RF applications. Table 1 depicts the differences between the three amplifiers. As shown in Figure 2, a differential output configuration was chosen to achieve good power supply rejection ratio and to provide ease of interface with ECL type postamplifier circuitry. The input stage (A1) has a low noise shunt-series feedback configuration. The open loop gain of A1 (R_F = infinite) is about 70; there-

fore, we can assume with good approximation an input stage transresistance equal to the value of R_F. Since the second stage differential amplifier (A2) and the output emitter followers (A3 and A4) have a voltage gain of about two, the input to output transresistance is twice the value of R_F. The single-ended transresistance is half of this value.

Returning to the input stage (Figure 3), a simple analysis can be used to determine the performance of the TIA. The input resistance, R_{IN}, can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}}$$

For the NE5210: $R_{IN} \simeq \dfrac{3.6k}{1 + 70} = 60\Omega$

For the NE5211: $R_{IN} \simeq \dfrac{14.4k}{1 + 70} = 200\Omega$

For the NE5212: $R_{IN} \simeq \dfrac{7.2k}{1 + 70} = 110\Omega$

Typical input capacitance of the TIA, C_{IN}, are 7.5pF, 4pF and 10pF for NE5210, NE5211 and NE5212 respectively.

Thus, while neglecting driving source and stray capacitances, R_{IN} and C_{IN} will form the dominant hole of the entire amplifier:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}} \begin{array}{l} = 350\text{MHz (NE5210)} \\ = 200\text{MHz (NE5211)} \\ = 145\text{MHz (NE5212)} \end{array}$$

Although significantly wider bandwidths could have been achieved by a cascode input stage configuration, the present solution has the advantage of a very uniform, highly de-sensitized frequency response because the Miller-effect dominates over external photodiode and stray capacitances. Consequently, the NE5210, NE5211, NE5212 will be relatively insensitive to PIN photodiode source capacitance variations. Since the dominant pole of the amplifier is at the input node, PIN diode

Table 1. Wideband Transimpedance Amplifier Family

PART	DIFFERENTIAL TRANSRESISTANCE KΩ (typ.)	BANDWIDTH −3dB (typ.)	INPUT NOISE CURRENT (typ.)	MAX. INPUT CURRENT
NE5212	14	140MHz	2.5pA/√Hz	± 120μA
NE5211	28	180MHz	1.8pA/√Hz	± 60μA
NE5210	7	280MHz	3.5pA/√Hz	± 240μA

A Family of Wide Band Low Noise Transimpedance Amplifiers NE5210, NE5211 and NE5212

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source capacitance will not degrade phase margin.

Package Parasitics

Package parasitics, particularly ground-lead inductances and parasitic capacitances, can significantly degrade frequency response. To minimize parasitics, multiple grounds are used in order to minimize ground wire-bond inductances.

Further bandwidth modifications can be achieved by a small capacitance between input and output or input and ground. Since each of the NE5210, NE5211 and NE5212 has differential outputs, both peaking and attenuating type frequency response shaping are possible.

Fighting Noise

Since most currently installed and planned fiber optic systems use non-coherent transmission and detect incident optical power, receiver noise performance becomes important. The NE5210, NE5211 and NE5212 go a long way towards solving this problem. Their input stage configurations achieve a respectably low input referred noise current spectral density of 3.5pA/$\sqrt{Hz}$ for the NE5210, 1.8pA/$\sqrt{Hz}$ for the NE5211 and 2.5pA/$\sqrt{Hz}$ for the NE5212, measured at 10MHz. This low value is nearly flat over the entire bandwidth. The transresistance configuration assures that the external high value bias resistors, often required for photodiode biasing, will not contribute to total system noise. As shown in the following equation, the equivalent input $_{RMS}$ noise current is determined by the quiescent operating point of Q_1, the feedback resistor, R_F, and the bandwidth, Δf *, however, it is not dependent on the internal Miller-capacitance. The noise current equation is then

$$\overline{i_{eq2}} = 4kT\frac{\Delta f}{R_F} + 2q\,I_{BQ1}\,\Delta f$$

$$+ 2q\,I_{CQ1}\frac{1}{g_{m1}}\,\omega^2\,(C_S + C_{\pi1})^2\,\Delta f$$

$$+ 4kT\,r_{bQ1}\,\omega^2\,C_S^2\,\Delta f$$

The resulting integrated noise over 100MHz with $C_S = 1pF$ is

    40nA for NE5210
    21nA for NE5211
    32nA for NE5212

Testing the NE5212

The remaining portion of this paper deals specifically with the NE5212 and is directly applicable to the NE5211 and the NE5210.

Connecting the NE5212 in an actual fiber optic preamplifier configuration, dynamic range, transient response, noise and overload recovery tests are easily measured (Figure 4). In order to replicate actual parasitic capacitances, effects of the photodiode bias network and circuit layout effects, the test circuit should closely resemble the real application conditions. If the intention is to use the device in die form, then the actual hybrid circuit mounting techniques should be used while testing.

In the test circuit shown, an 850nm modulated laser light source feeds an HP-HFBR2202 PIN photodiode which is mounted in close proximity to the NE5212 input. The R-C filter in series with the photodiode eliminates possible disturbances from the power supply. Both differential outputs are AC coupled through 33Ω resistors in order to match to the 50Ω test system. In most applications these matching resistors are unnecessary. Performance evaluation in the linear region, including amplitude and phase response and power supply rejection, can be accomplished by a network analyzer and S parameter test set (Figure 5). The simple equations given in the figure for the calculation of transresistance, R_T, are accurate for $R \gg R_{IN}$, where R_{IN} is the input resistance of the NE5212.

General Purpose RF Applications

Besides the main fiber-optic receiver applications, many other interesting possibilities exist for the NE5212. Simplicity and ease-of-use are the prevailing characteristics of this device. For instance, amplifiers with 20dB gain can be built requiring only one external gain setting resistor (Figure 6). The voltage gain of the differential configuration with no load at the outputs can be calculated as follows:

$$V_{OUT} = I_{IN} \times R_T = \frac{V_{IN}}{R_S + R + R_{IN}}\,R_T \text{ and}$$

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_T}{R_S + R + R_{IN}}$$

where R_S is the signal-source resistance, R is the external gain setting resistor and R_{IN} is the input resistance of the NE5212. Substituting the actual values:

$$A_V = \frac{14000}{R_S + R + 110}$$

where all values are in ohms. The graph of Figure 6 is an experimental verification of this formula in a single-ended, 50Ω system, using the test configuration of Figure 5. Note the 6dB loss due to the single-ended configuration and another 6dB due to the 50Ω load. As

in all other RF applications, attention to power supply bypassing clean grounds and minimization of input stray capacitances are required for optimum performance.

Another useful application of the NE5212 is as a voltage controlled amplifier, using a DMOS FET device biased into the linear region (Figure 7). An operational amplifier with supply-to-ground output swing and supply-to-ground input common mode range (such as the Signetics NE5230) can provide adequate gate control voltage even with a single 5V power supply. This type of circuit can have 25dB AGC range at 50MHz and 45dB at 10MHz with less than 1% harmonic content. AGC range is determined by the ON-resistance range of the FET and capacitive drain to source feedthrough. If lowest RF feedthrough were required, the FET should be used in a shunt configuration rather than in a series.

Turning towards an entirely different area of application, where contrary to the NE5212's capabilities, poor phase margins are mandatory, a simple crystal oscillator with buffered output can be built using a minimum number of external components (Figure 8). The feedback signal is taken from the non-inverting output, while the inverting output provides a low impedance (15Ω) output drive. The crystal operates in its series resonance mode. Figure 9 shows a varactor tuned version with a large tuning range. In Figure 10 the circuit has been optimized for stability at the expense of tuning range.

In RF amplifier applications it is often desirable to limit the amplifier bandwidth in order to minimize noise and RFI. The 100-150MHz bandwidth of the NE5212 can be easily modified by connecting a capacitor to the input pin. The device bandwidth then becomes

$$f_{-3dB} = \frac{1}{2\pi\,R_{IN}\,(C_{IN} + C_{EXT})}$$

where R_{IN} is the input resistance, C_{IN} is the input capacitance as specified in the data sheet and C_{EXT} is the external capacitance. For example, a $C_{EXT} = 33pF$ will reduce the amplifier bandwidth to 42MHz with a single pole roll-off. The penalty is an increase in noise current. The transfer curve is shown in Figure 11. Another way to limit the bandwidth is to connect a capacitor across the differential output. Single-ended to differential conversion is another useful application for the device. Impedance matching is easily accomplished by resistors connected in series with the outputs.

A Family of Wide Band Low Noise Transimpedance Amplifiers NE5210, NE5211 and NE5212

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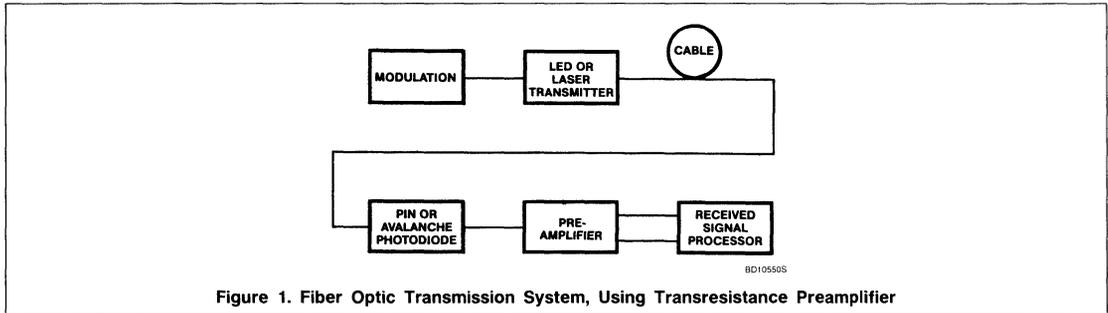
Figure 1. Fiber Optic Transmission System, Using Transresistance Preamplifier
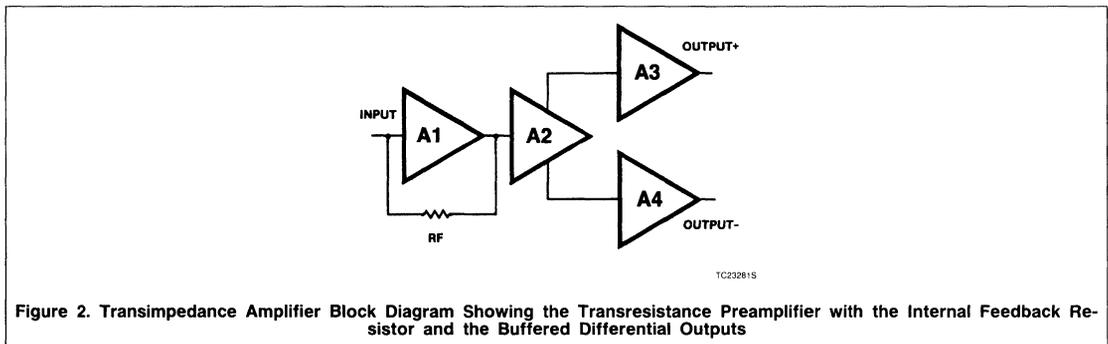

Figure 2. Transimpedance Amplifier Block Diagram Showing the Transresistance Preamplifier with the Internal Feedback Resistor and the Buffered Differential Outputs
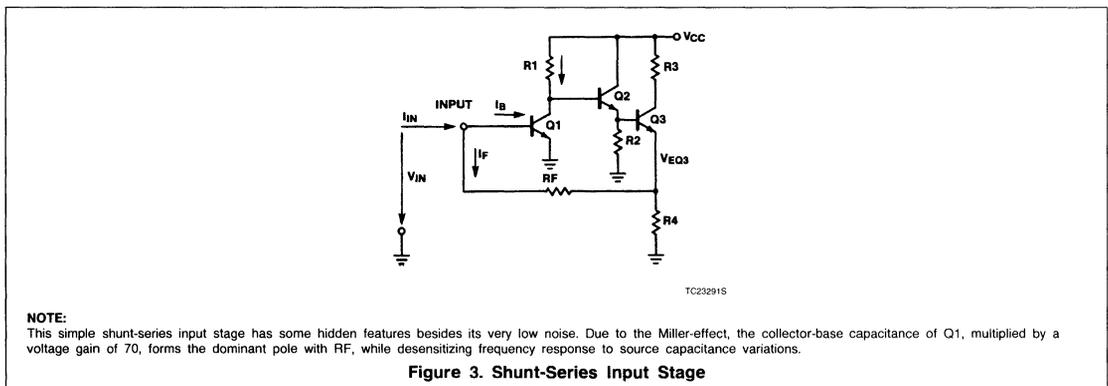

NOTE:
This simple shunt-series input stage has some hidden features besides its very low noise. Due to the Miller-effect, the collector-base capacitance of Q1, multiplied by a voltage gain of 70, forms the dominant pole with RF, while desensitizing frequency response to source capacitance variations.

Figure 3. Shunt-Series Input Stage

A Family of Wide Band Low Noise Transimpedance Amplifiers NE5210, NE5211 and NE5212

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a. Stimulus

b. Response

Figure 4. Dynamic Range, Impulse Response and Noise Test Circuit
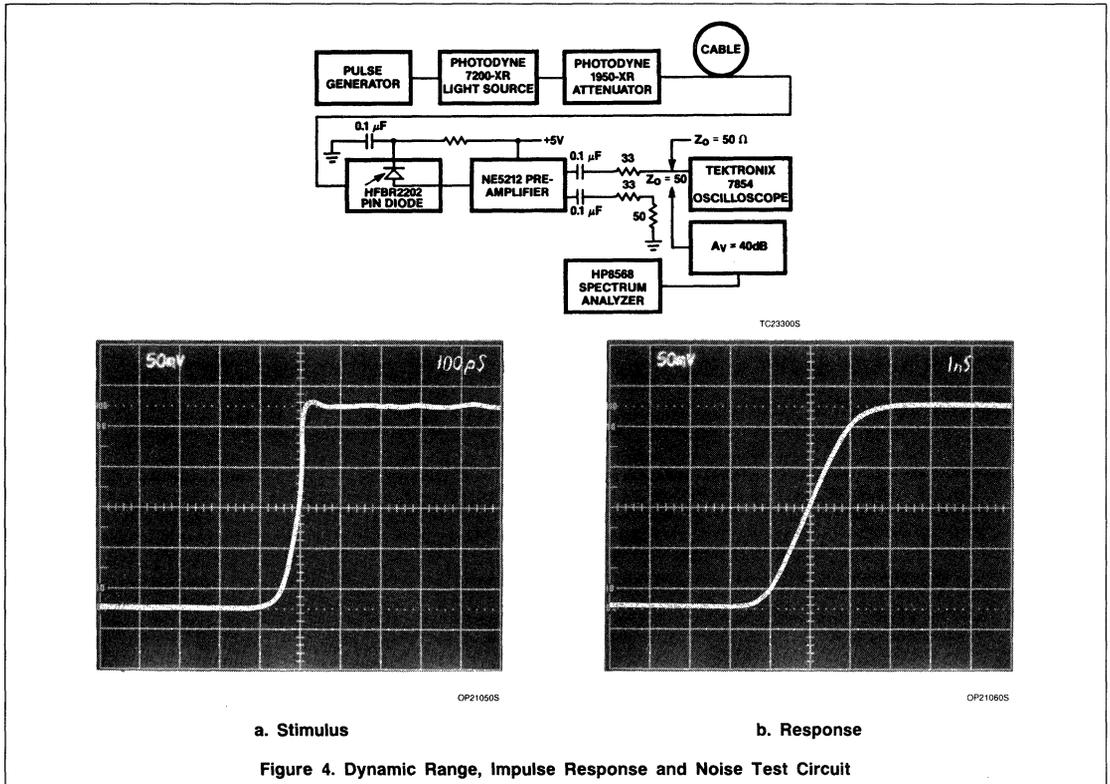
A Family of Wide Band Low Noise Transimpedance Amplifiers NE5210, NE5211 and NE5212

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SINGLE ENDED		DIFFERENTIAL	
$R_t = \dfrac{V_{OUT}}{V_{IN}}$	$R = 2 X S_{21} \cdot R$	$R_t = \dfrac{V_{OUT}}{V_{IN}}$	$R = 4 \cdot S_{21} \cdot R$
$R_o = Z_o \left\| \dfrac{1+S_{22}}{1-S_{22}} \right\| -33$		$R_o = 2Z_o \left\| \dfrac{1+S_{22}}{1-S_{22}} \right\| -66$	
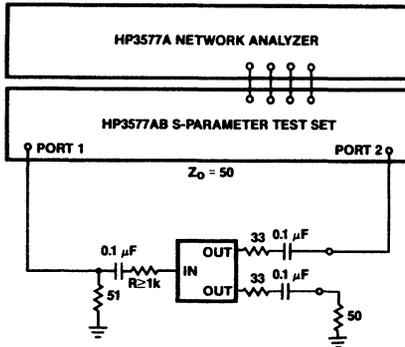
TC23321S

NOTE:
The frequency response can be conveniently measured with an S-parameter network analyzer. The 1kΩ input resistor acts as a voltage-to-current converter and the resistors at the output do the impedance matching. The curves show a smooth, wide band response with ample phase margin. Transresistance and output resistance can be calculated from the S-parameters as shown in the table.

Figure 5. Frequency Response and Group Delay Test Circuit
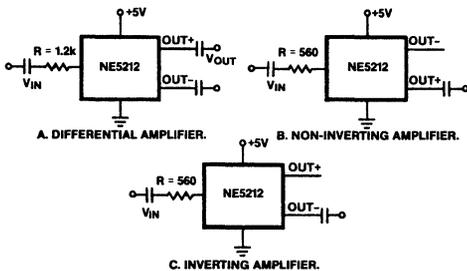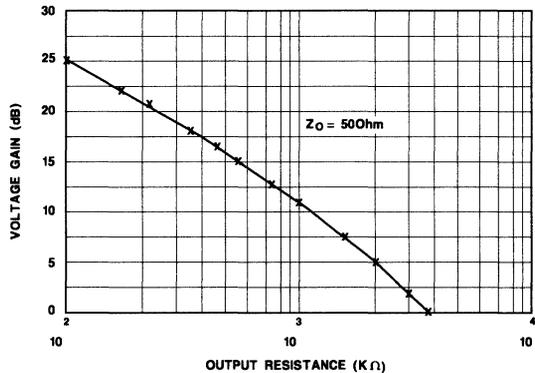
b. Non-Inverting Amplifier
Single-Ended Gain vs Output Resistance

NOTE:
A 150MHz, 20dB amplifier requires only one external gain setting resistor. Differential or single-ended operation with or without inversion is possible.

Figure 6. 20dB Amplifier Configurations

A Family of Wide Band Low Noise Transimpedance Amplifiers NE5210, NE5211 and NE5212
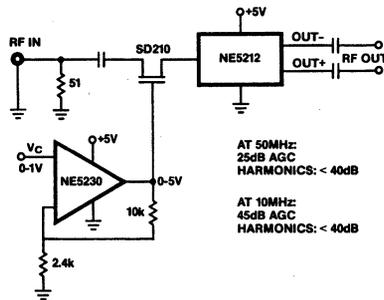
NOTE:
This variable gain RF amplifier has less than 1% distortion, 25dB range at 50MHz and 45dB range at 10MHz, with a 0 – 1V control signal.

Figure 7. Amplifier with Gain Control
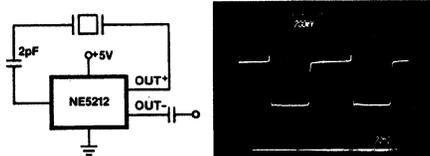
NOTE:
This 16MHz crystal oscillator has minimum component count and operates in the series resonant mode. Output provides independent 50Ω drive capability.

Figure 8. 16MHz Crystal Oscillator
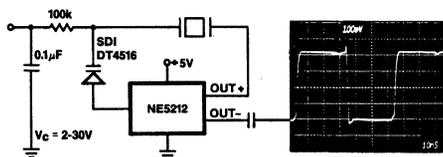
NOTE:
Varactor tuned crystal oscillator with 0.28% tuning range.

Figure 9. Varactor-Tuned Crystal Oscillator

# A Family of Wide Band Low Noise Transimpedance Amplifiers NE5210, NE5211 and NE5212
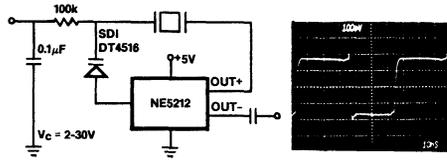
NOTE:
Varactor tuned oscillator with 1ppm/V supply sensitivity.

Figure 10. Varactor-Tuned Oscillator with 1ppm/V Supply Sensitivity
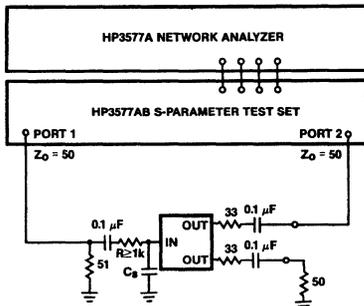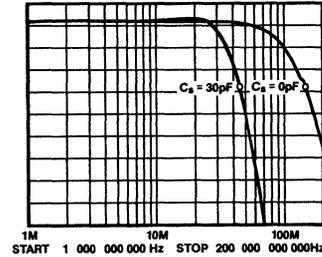
NOTE:
Setting bandwidth with shunt input capacitor, C_S.

Figure 11. Setting Bandwidth with C_S

Signetics

Linear Products

NE5210
Transimpedance Amplifier (280MHz)

Preliminary Specification

DESCRIPTION

The NE5210 is a 7kΩ transimpedance wide band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber-optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

FEATURES

- **Low noise: 3.5pA/√Hz**
- **Single 5V supply**
- **Large bandwidth: 280MHz**
- **Differential outputs**
- **Low input/output impedances**
- **High power supply rejection ratio**
- **High overload threshold current**
- **Wide dynamic range**
- **7kΩ differential transresistance**

APPLICATIONS

- **Fiber-optic receivers, analog and digital**
- **Current-to-voltage converters**
- **Wideband gain block**
- **Medical and scientific instrumentation**
- **Sensor preamplifiers**
- **Single-ended to differential conversion**
- **Low noise RF amplifiers**
- **RF signal processing**

PIN CONFIGURATION

D Package

GND$_2$ [1]	[14] OUT (−)
GND$_2$ [2]	[13] GND$_2$
NC [3]	[12] OUT (+)
I$_{IN}$ [4]	[11] GND$_1$
NC [5]	[10] GND$_1$
V$_{CC1}$ [6]	[9] GND$_1$
V$_{CC2}$ [7]	[8] GND$_1$

TOP VIEW   CD13240S
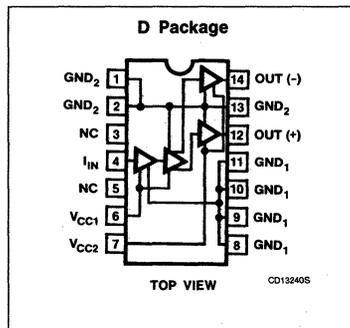
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5210D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V$_{CC}$	Power supply	6	V
T$_A$	Operating ambient temperature range	0 to +70	°C
T$_J$	Operating junction temperature range	−55 to +150	°C
T$_{STG}$	Storage temperature range	−65 to +150	°C
P$_{DMAX}$	Power dissipation T$_A$ = 25°C (still air)[1]	1.0	W
I$_{INMAX}$	Maximum input current[2]	5	mA

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance: θ$_{JA}$ = 125°C/W.
2. The use of a pull-up resistor to V$_{CC}$ for the PIN diode, is recommended.

Transimpedance Amplifier (280MHz)

NE5210

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range	0 to +70	°C
T_J	Junction temperature range	0 to +90	°C

DC ELECTRICAL CHARACTERISTICS
Min and Max limits apply over operating temperature range at $V_{CC} = 5V$, unless otherwise specified. Typical data applies at $V_{CC} = 5V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	V
V_{OS}	Output offset voltage			0	80	mV
I_{CC}	Supply current		21	26	32	mA
I_{OMAX}	Output sink/source current[1]		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	± 120	± 160		μA
I_{INMAX}	Maximum input current overload threshold	Test Circuit 8, Procedure 4	± 160	± 240		μA

NOTE:
1. Test condition: output quiescent voltage variation is less than 100mV for 3mA load current.

Transimpedance Amplifier (280MHz)

NE5210

AC ELECTRICAL CHARACTERISTICS Typical data and Min/Max limits apply at $V_{CC} = 5V$ and $T_A = 25°C$.

| SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$ Test Circuit 8, Procedure 1	4.9	7	10	$k\Omega$
R_O	Output resistance (differential output)	DC tested	16	30	42	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	2.45	3.5	5	$k\Omega$
R_O	Output resistance (single-ended output)	DC tested	8	15	21	Ω
f_{3dB}	Bandwidth (−3dB)	Test Circuit 1, $T_A = 25°C$	200	280		MHz
R_{IN}	Input resistance			60		Ω
C_{IN}	Input capacitance			7.5		pF
$\Delta R / \Delta V$	Transresistance power supply sensitivity	$V_{CC} = 5 \pm 0.5V$		9.6	20	%/V
$\Delta R / \Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\ MAX} - T_{A\ MIN}$		0.05	0.1	%/°C
I_N	RMS noise current spectral density (referred to input)	$f = 10MHz$, $T_A = 25°C$, Test Circuit 2		3.5	6	$pA/\sqrt{Hz}$
I_T	Integrated RMS noise current over the bandwidth (referred to input) $C_S = 0$[1]	$T_A = 25°C$ Test Circuit 2				
		$\Delta f = 100MHz$		37		nA
		$\Delta f = 200MHz$		56		nA
		$\Delta f = 300MHz$		71		nA
	$C_S = 1$	$\Delta f = 100MHz$		40		nA
		$\Delta f = 200MHz$		66		nA
		$\Delta f = 300MHz$		89		nA
PSRR	Power supply rejection ratio[2] ($V_{CC1} = V_{CC2}$)	Dc tested, $\Delta V_{CC} = 0.1V$ Equivalent AC test circuit 3	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, $\Delta V_{CC} = 0.1V$ Equivalent AC test circuit 4	20	36		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, $\Delta V_{CC} = 0.1V$ Equivalent AC test circuit 5		65		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	$f = 0.1MHz$, Test Circuit 6		23		dB
V_{OMAX}	Maximum output voltage swing differential	$R_L = \infty$ Test Circuit 8, Procedure 3	2.4	3.2		V_{P-P}
V_{INMAX}	Maximum input amplitude for output duty cycle of $50 \pm 5\%$[3]	Test Circuit 7	650			mV_{P-P}
t_R	Rise time for 50 mV_{P-P} output signal[4]	Test Circuit 7		0.8	1.2	ns

NOTES:
1. Package parasitic capacitance amounts to about 0.2pF.
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} line.
3. Guaranteed by linearity and overload tests.
4. t_R defined as 20 – 80% rise time. It is guaranteed by a -3dB bandwidth test.

Transimpedance Amplifier (280MHz)

NE5210

TEST CIRCUITS

|	SINGLE-ENDED	DIFFERENTIAL
	$R_T \cong \dfrac{V_{OUT}}{V_{IN}}$ $R = 2 \times S21 \times R$	$R_T = \dfrac{V_{OUT}}{V_{IN}}$ $R = 4 \times S21 \times R$
	$R_O \cong Z_O \left| \dfrac{1+S22}{1-S22} \right| - 33$	$R_O = 2Z_O \left| \dfrac{1+S22}{1-S22} \right| - 66$
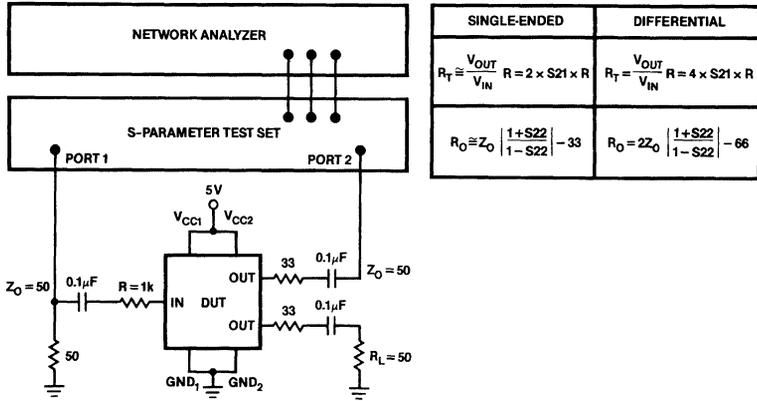
Test Circuit 1

TC22561S

**Test Circuit 2**

TC22551S
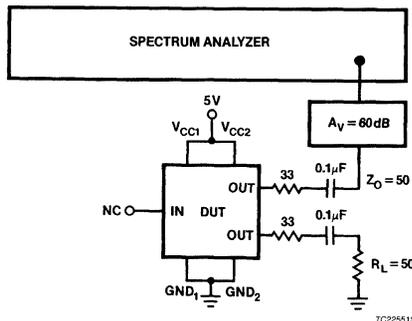
Transimpedance Amplifier (280MHz)

NE5210

TEST CIRCUITS (Continued)
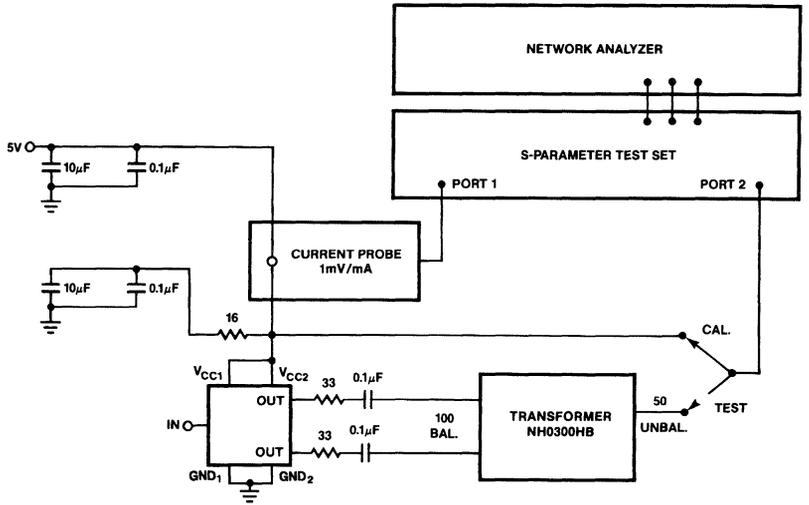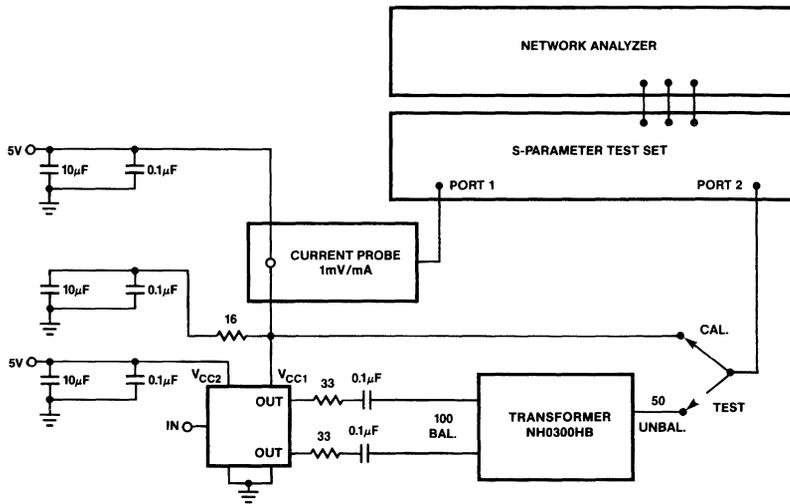
Test Circuit 3

Test Circuit 4

Transimpedance Amplifier (280MHz)

NE5210

TEST CIRCUITS (Continued)
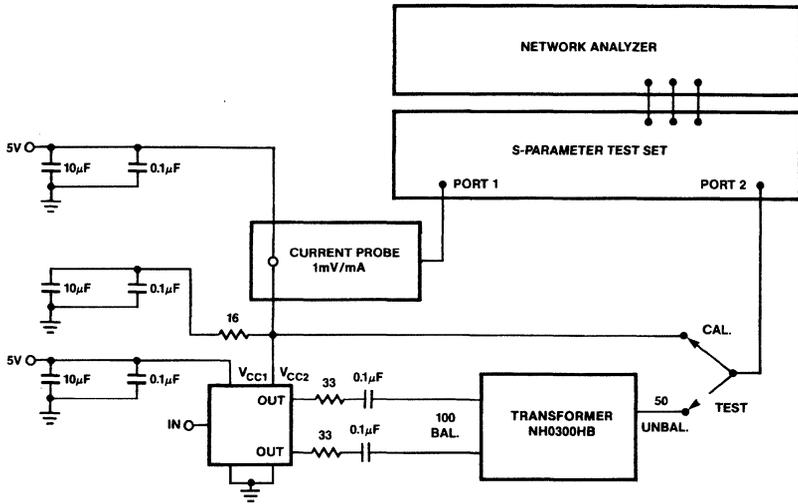
Test Circuit 5
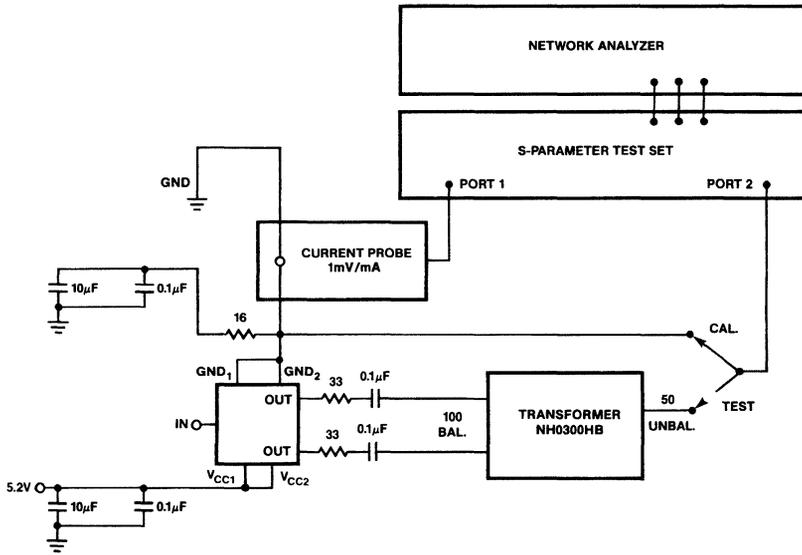
Test Circuit 6

Transimpedance Amplifier (280MHz) NE5210

TEST CIRCUITS (Continued)
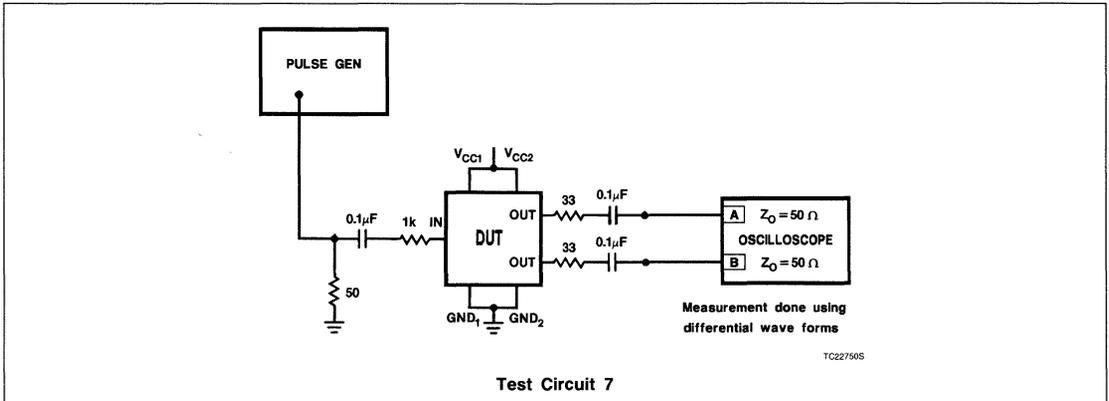
Test Circuit 7

# Transimpedance Amplifier (280MHz)

NE5210

TEST CIRCUITS (Continued)

**Typical Differential Output Voltage
vs Current Input**
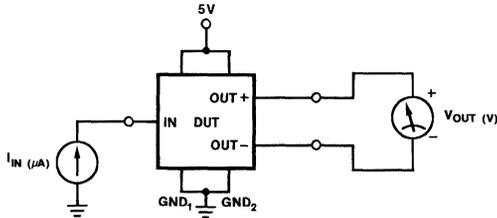
TC23460S
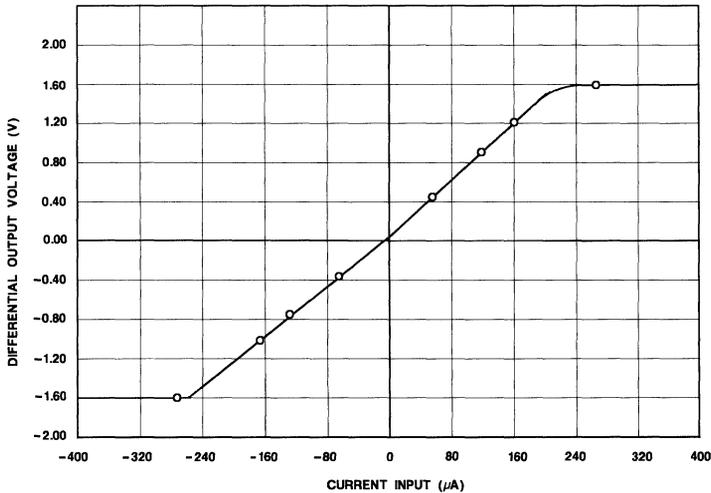
OP20990S

NE5210 TEST CONDITIONS

Procedure 1 R_T measured at 60μA
$R_T = (V_{O1} - V_{O2})/(+60μA - (-60μA))$
Where: V_{O1} Measured at $I_{IN} = +60μA$
V_{O2} Measured at $I_{IN} = -60μA$

Procedure 2   Linearity = $1 - ABS((V_{OA} - V_{OB})/(V_{O3} - V_{O4}))$
Where: V_{O3} Measured at $I_{IN} = +120μA$
V_{O4} Measured at $I_{IN} = -120μA$
$V_{OA} = R_T$ * $(+120μA) + V_{O8}$
$V_{OB} = R_T$ * $(-120μA) + V_{O8}$

Procedure 3 $V_{OMAX} = V_{O7} - V_{O8}$
Where: V_{O7} Measured at $I_{IN} = +260μA$
V_{O8} Measured at $I_{IN} = -260μA$

Procedure 4 $I_{IN\ MAX}$ Test Pass Conditions:
$V_{O7} - V_{O5} > 20mV$ and $V_{O6} - V_{O5} > 20mV$
Where: V_{O5} Measured at $I_{IN} = +160μA$
V_{O6} Measured at $I_{IN} = -160μA$
V_{O7} Measured at $I_{IN} = +260μA$
V_{O8} Measured at $I_{IN} = -260μA$

Test Circuit 8

Transimpedance Amplifier (280MHz)

NE5210

TYPICAL PERFORMANCE CHARACTERISTICS

NE5210 Supply Current vs Temperature

OP21580S

NE5210 Output Bias Voltage vs Temperature

OP21590S

Output Voltage vs Input Current

OP21610S

NE5210 Input Bias Voltage vs Temperature

OP21620S

NE5210 Output Bias Voltage vs Temperature

OP21630S

Differential Output Voltage vs Input Current

OP21640S

NE5210 Output Offset Voltage vs Temperature

OP21680S

NE5210 Differential Output Swing vs Temperature

OP21690S

Differential Output Voltage vs Input Current

OP21700S

Transimpedance Amplifier (280MHz)

# NE5210

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency


OP21710S

Gain vs Frequency

OP21720S

NE5210 Differential Transresistance vs Temperature

OP21730S

Gain vs Frequency

OP21740S

Gain vs Frequency

OP21750S
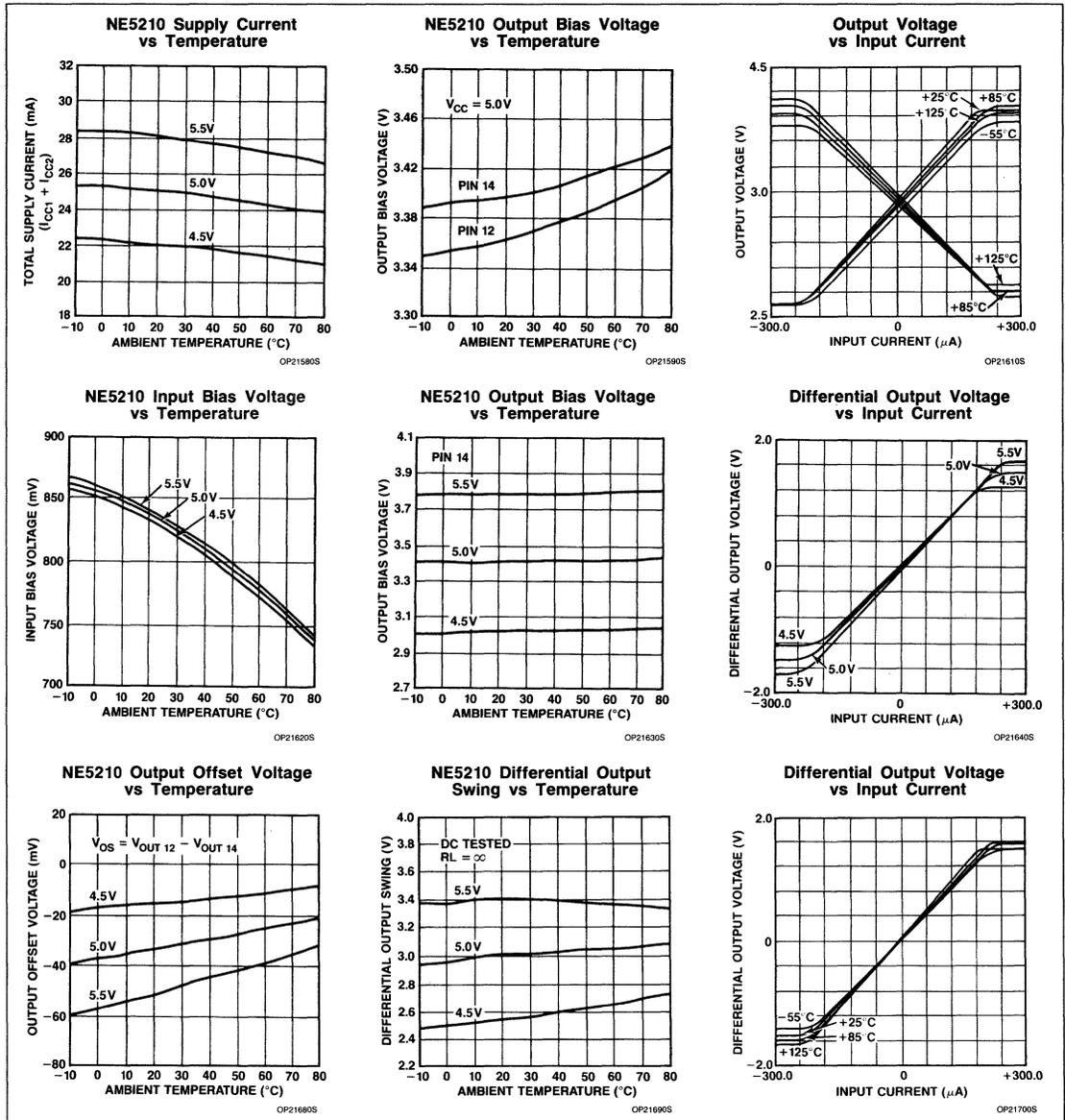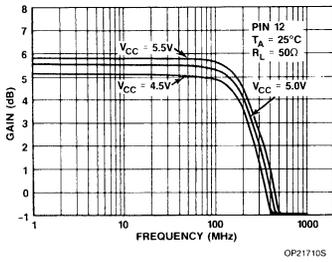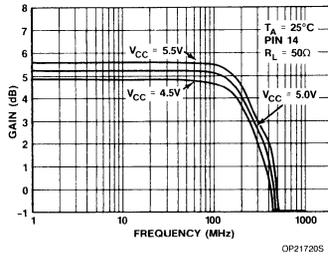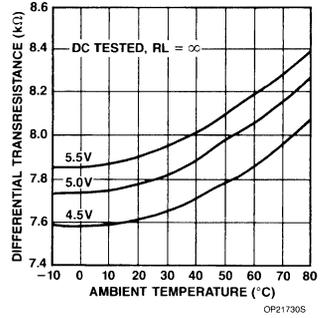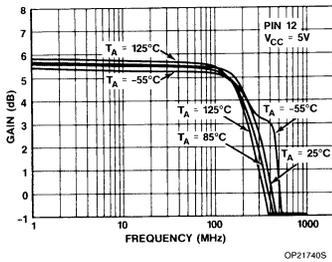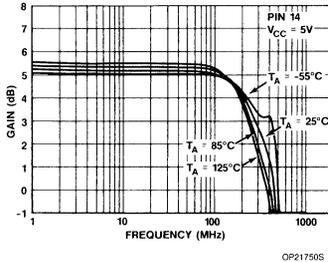
NE5210 Bandwidth vs Temperature

OP21760S

Gain and Phase Shift vs Frequency

OP21770S

Gain and Phase Shift vs Frequency

OP21780S
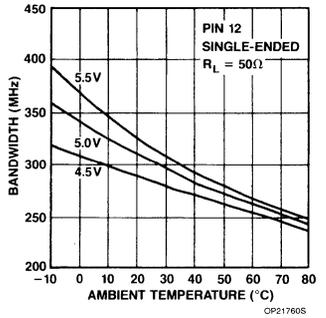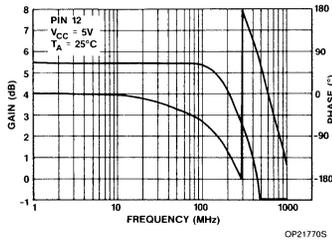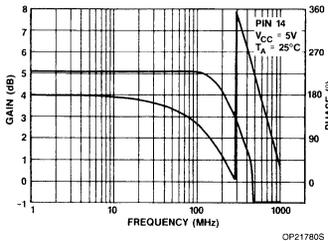
NE5210 Typical Bandwidth Distribution (70 Parts from 4 Wafer Lots)
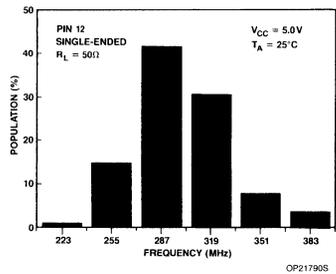
OP21790S

Transimpedance Amplifier (280MHz)
NE5210

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

NE5210 Output Resistance vs Temperature
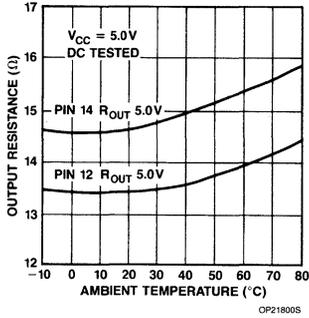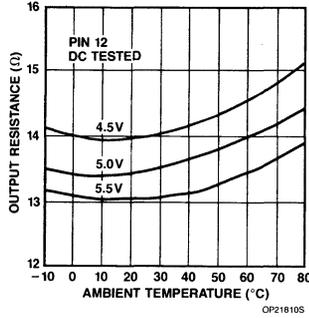
OP21800S

NE5210 Output Resistance vs Temperature

OP21810S

NE5210 Output Resistance vs Temperature

OP21820S

Output Resistance vs Frequency

OP21830S
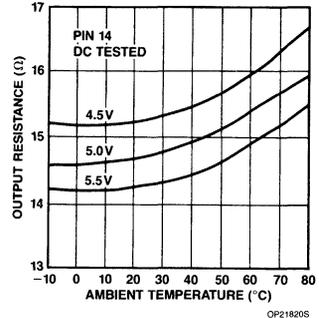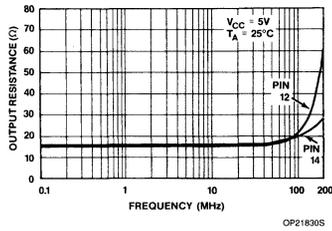
NE5210 Power Supply Rejection Ratio vs Temperature

OP21840S

Group Delay

OP21850S

Output Step Response

OP21860S
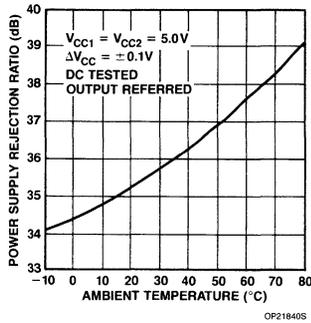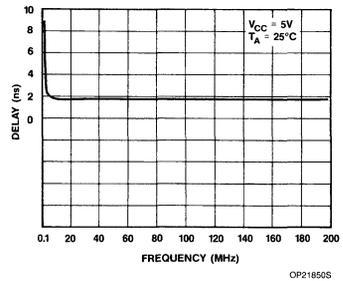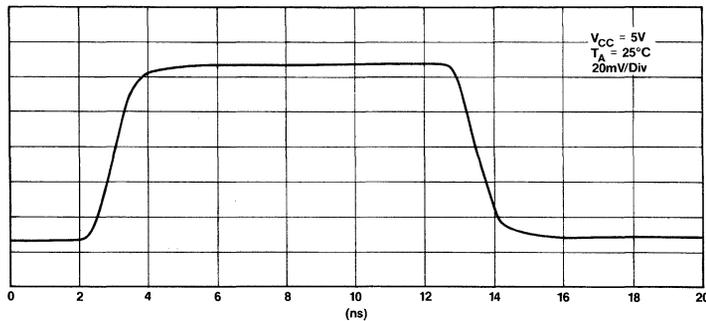
Transimpedance Amplifier (280MHz)

NE5210

THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5210 is a wide bandwidth (typically 280MHz) transimpedance amplifier designed primarily for input currents requiring a large dynamic range, such as those produced by a laser diode. The maximum input current before output stage clipping occurs at typically 240μA. The NE5210 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, $R_F = 3.6k\Omega$. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT}(diff)}{I_{IN}} = 2R_F = 2(3.6K) = 7.2k\Omega.$$

The single-ended transresistance of the amplifier is typically 3.6kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, $A_{VOL} \approx 70$. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15}–Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q_{11}–Q_{12} which are biased by constant current sources. The collectors of Q_{11}–Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended.


Figure 1. NE5210 – Block Diagram

For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 7.5pF, assuming that $C_S = 0$ where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{3.6k}{71} = 51\Omega.$$

More exact calculations would yield a higher value of 60Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi \, R_{IN} \, C_{IN}}.$$

Assuming typical values for $R_F = 3.6k\Omega$, $R_{IN} = 60\Omega$, $C_{IN} = 7.5pF$

$$f_{-3dB} = \frac{1}{2\pi \, 7.5pF \, 60} = 354MHz.$$

The operating point of Q1, Figure 2, has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, $R_{IN} = 60\Omega$ then the total input capacitance, $C_{IN} = (1 + 7.5)$ pF which will lead to only a 12% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 3.5pA/$\sqrt{Hz}$. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 66nA in a 200MHz bandwidth.

DYNAMIC RANGE CALCULATIONS

The electrical dynamic range can be defined as the ratio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming $I_{INMAX} = 240\mu$A and a wideband noise of $I_{EQ} = 66nA_{RMS}$ for an external source capacitance of $C_S = 1pF$.

Transimpedance Amplifier (280MHz)

NE5210
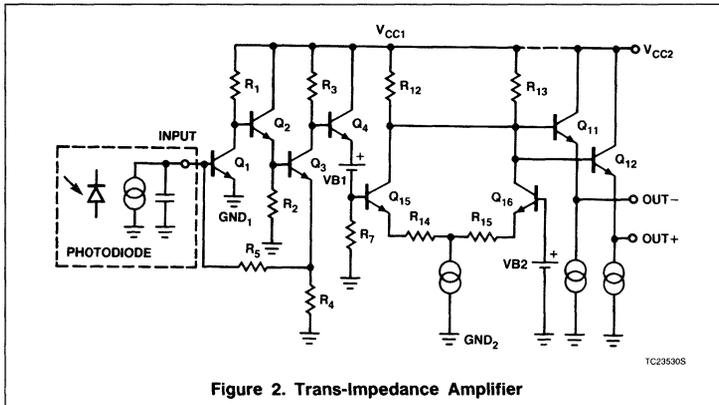
Figure 2. Trans-Impedance Amplifier

Figure 3. Shunt-Series Input Stage

$$D_E = \frac{(\text{Max. input current})}{(\text{Peak noise current})}$$

$$= 20 \ \log \frac{(240 \times 10^{-6})}{(\sqrt{2} \ 66 \times 10^{-9})}$$

$$= 20 \ \log \frac{(240\mu A)}{(93nA)} = 68dB.$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

Energy of one Photon $= \dfrac{hc}{\lambda}$ watt sec (Joule)

Where h = Planck's Constant = 6.6×10^{-34} Joule sec.
 c = speed of light = 3×10^8 mt/sec
 c/λ = optical frequency

No. of incident photons/sec $= \dfrac{P}{\dfrac{hc}{\lambda}}$ where P = optical incident power

No. of generated electrons/sec $= \eta \cdot \dfrac{P}{\dfrac{hc}{\lambda}}$

where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole pairs}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \frac{P}{\dfrac{hc}{\lambda}} \cdot e \ \text{Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

Responsivity $R = \dfrac{\eta \cdot e}{\dfrac{hc}{\lambda}}$ Amp/watt

$I = P \cdot R$

Assuming a data rate of 400 Mbaud (Bandwidth, B = 200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{I_{EQ}}{qB} = \frac{66 \times 10^{-9}}{(1.6 \times 10^{-19})(200 \times 10^6)} = 2063$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12 \frac{hc}{\lambda} B \ Z = 12 \ 2.3 \times 10^{-19}$$
$$200 \times 10^6 \ 2063$$
$$= 1139nW = -29.4dBm,$$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum input current to the NE5210, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{1139 \times 10^{-9} \times 1.6 \times 10^{-19}}{2.3 \times 10^{-19}}$$

$$= 792nA.$$

Choosing the maximum peak overload current of $I_{avMAX} = 240\mu A$, the maximum mean optical power is:

$$P_{avMAX} = \frac{hc}{\lambda} \frac{I_{avMAX}}{q} = \frac{2.3 \times 10^{-19}}{1.6 \times 10^{-19}} 240 \times 10^{-6}$$
$$= 345mW \ \text{or} \ -4.6dBm.$$

Thus the optical dynamic range, D_o is:

$$D_o = P_{avMAX} - P_{avMIN} = -4.6 - (-29.4) = 24.8dB.$$

This represents the maximum limit attainable with the NE5210 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 850nm wavelength.

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5210 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout so that Ground 1 and Ground 2 have very low impedance paths has produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near

Transimpedance Amplifier (280MHz)

NE5210

800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1μF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of

0.1μF capacitors with 10μF tantalum capacitors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 4 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the NE5210 and the NE5214 post amplifier.


Figure 4. A 50Mb/s TTL Fiber Optic Receiver Using NE5210/NE5214

Signetics

NE/SA5211
Transimpedance Amplifier (180MHz)

Preliminary Specification

Linear Products

DESCRIPTION
The NE/SA5211 is a 28kΩ transimpedance, wide-band, low noise amplifier with differential outputs, particularly suitable for signal recovery in fiber optic receivers. The part is ideally suited for many other RF applications as a general purpose gain block.

FEATURES
- **Extremely low noise: 1.8pA/√Hz**
- **Single 5V supply**
- **Large bandwidth: 180MHz**
- **Differential outputs**
- **Low input/output impedances**
- **High power supply rejection ratio**
- **28kΩ differential transresistance**

APPLICATIONS
- **Fiber optic receivers, analog and digital**
- **Current-to-voltage converters**
- **Wide-band gain block**
- **Medical and scientific Instrumentation**
- **Sensor preamplifiers**
- **Single-ended to differential conversion**
- **Low noise RF amplifiers**
- **RF signal processing**

PIN CONFIGURATION

D Package

Pin	Name		Pin	Name
1	GND_2		14	OUT (−)
2	GND_2		13	GND_2
3	NC		12	OUT (+)
4	I_{IN}		11	GND_1
5	NC		10	GND_1
6	V_{CC1}		9	GND_1
7	V_{CC2}		8	GND_1

CD13240S

TOP VIEW
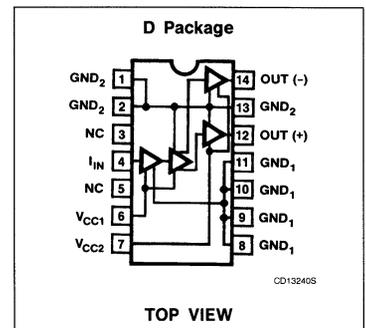
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE5211D
14-Pin Plastic SO	−40 to +85°C	SA5211D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5211	SA5211	
V_{CC}	Power supply	6	6	V
T_A	Operating ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	−55 to +150	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	−65 to +150	°C
$P_{D\ MAX}$	Power dissipation, T_A = 25°C (still-air)[1]	1.0	1.0	W
$I_{IN\ MAX}$	Maximum input current[2]	5	5	mA

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance:
   θ_{JA} = 125°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode, is recommended.

Transimpedance Amplifier (180MHz)

NE/SA5211

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	4.5 to 5.5	V
T_A	Ambient temperature range NE Grade SA Grade	0 to +70 −40 to +85	°C °C
T_J	Junction temperature range NE Grade SA Grade	0 to +90 −40 to +105	°C °C

DC ELECTRICAL CHARACTERISTICS
Min and Max limits apply over operating temperature at $V_{CC} = 5V$, unless otherwise specified. Typical data apply at $V_{CC} = 5V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5211			SA5211			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	0.55	0.8	1.00	V
$V_{O\pm}$	Output bias voltage		2.8	3.4	3.7	2.7	3.4	3.7	V
V_{OS}	Output offset voltage			0	120		0	130	mV
I_{CC}	Supply current		21	24	30	20	26	31	mA
I_{OMAX}	Output sink/source current[1]		3	4		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 8, Procedure 2	±30	±40		±20	±40		µA
$I_{IN\ MAX}$	Maximum input current overload threshold	Test Circuit 8, Procedure 4	±40	±60		±30	±60		µA

NOTE:
1. Test condition: output quiescent voltage variation is less than 100mV for 3mA load current.

Transimpedance Amplifier (180MHz)   NE/SA5211

AC ELECTRICAL CHARACTERISTICS Typical data and Min and Max limits apply at V_{CC} = 5V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5211			SA5211			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested $R_L = \infty$ Test Circuit 8, Procedure 1	22	28	35	21	28	36	kΩ
R_O	Output resistance (differentialoutput)	DC tested		30			30		Ω
R_T	Transresistance (single-ended output)	DC tested $R_L = \infty$	11	14	17.5	10.5	14	18.0	kΩ
R_O	Output resistance (single-ended output)	DC tested		15			15		Ω
f_{3dB}	Bandwidth (–3dB)	T_A = 25°C Test circuit 1		180			180		MHz
R_{IN}	Input resistance			200			200		Ω
C_{IN}	Input capacitance			4			4		pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	V_{CC} = 5± 0.5V		3.7			3.7		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	$\Delta T_A = T_{A\ MAX} - T_{A\ MIN}$		0.025			0.025		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 f = 10MHz T_A = 25°C		1.8			1.8		pA/$\sqrt{Hz}$
I_T	Integrated RMS noise current over the bandwidth (referred to input)	T_A = 25°C Test Circuit 2							
	$C_S = 0$[1]	Δf = 50MHz Δf = 100MHz Δf = 200MHz		13 20 35			13 20 35		nA nA nA
	$C_S = 1pF$	Δf = 50MHz Δf = 100MHz Δf = 200MHz		13 21 41			13 21 41		nA nA nA
PSRR	Power supply rejection ratio[2] ($V_{CC1} = V_{CC2}$)	DC tested, ΔV_{CC} = .01V Equivalent AC Test Circuit 3	26	32		23	32		dB
PSRR	Power supply rejection ratio[2] (V_{CC1})	DC tested, ΔV_{CC} = .01V Equivalent AC Test Circuit 4	26	32		23	32		dB
PSRR	Power supply rejection ratio[2] (V_{CC2})	DC tested, ΔV_{CC} = .01V Equivalent AC Test Circuit 5	45	65		45	65		dB
PSRR	Power supply rejection ratio (ECL configuration)[2]	f = 0.1MHz Test Circuit 6		23			23		dB
V_{OMAX}	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 8, Procedure 3	2.4	3.2		1.7	3.2		V_{P-P}
$V_{IN\ MAX}$	Maximum input amplitude for output duty cycle of 50± 5%[3]	Test Circuit 7	160			160			mV$_{P-P}$
t_R	Rise time for 50mV output signal[4]	Test Circuit 7		0.8	1.2		0.8	1.8	ns

NOTES:
1. Package parasitic capacitance amounts to about 0.2pF.
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} lines.
3. Guaranteed by linearity and overload tests.
4. t_R defined as 20 – 80% rise time. It is guaranteed by –3dB bandwidth test.

Transimpedance Amplifier (180MHz)   NE/SA5211

TEST CIRCUITS

SINGLE-ENDED	DIFFERENTIAL
$R_T \cong \dfrac{V_{OUT}}{V_{IN}} \; R = 2 \times S21 \times R$	$R_T = \dfrac{V_{OUT}}{V_{IN}} \; R = 4 \times S21 \times R$
$R_O \cong Z_O \left\| \dfrac{1+S22}{1-S22} \right\| - 33$	$R_O = 2Z_O \left\| \dfrac{1+S22}{1-S22} \right\| - 66$

TC22561S

Test Circuit 1

Test Circuit 2

TC22551S

Transimpedance Amplifier (180MHz)

NE/SA5211

TEST CIRCUITS (Continued)

Test Circuit 3

Test Circuit 4

Transimpedance Amplifier (180MHz)

NE/SA5211

TEST CIRCUITS (Continued)

Test Circuit 5

Test Circuit 6

Transimpedance Amplifier (180MHz)   NE/SA5211

TEST CIRCUITS (Continued)

Test Circuit 7

Transimpedance Amplifier (180MHz)

NE/SA5211

TEST CIRCUITS (Continued)

TC23461S

Typical V_O (Differential) vs I_{IN}

OP20990S

NE5211 TEST CONDITIONS

Procedure 1	R_T measured at $15\mu A$ $R_T = (V_{O1} - V_{O2})/(+15\mu A - (-15\mu A))$ Where: V_{O1} Measured at $I_{IN} = +15\mu A$ V_{O2} Measured at $I_{IN} = -15\mu A$
Procedure 2	Linearity $= 1 - ABS((V_{OA} - V_{OB})/(V_{O3} - V_{O4}))$ Where: V_{O3} Measured at $I_{IN} = +30\mu A$ V_{O4} Measured at $I_{IN} = -30\mu A$ $V_{OA} = R_T * (+30\mu A) + V_{O8}$ $V_{OB} = R_T * (-30\mu A) + V_{O8}$
Procedure 3	$V_{OMAX} = V_{O7} - V_{O8}$ Where: V_{O7} Measured at $I_{IN} = +65\mu A$ V_{O8} Measured at $I_{IN} = -65\mu A$
Procedure 4	$I_{IN\ MAX}$ Test Pass Conditions: $V_{O7} - V_{O5} > 50mV$ and $V_{O6} - V_{O5} > 50mV$ Where: V_{O5} Measured at $I_{IN} = +40\mu A$ V_{O6} Measured at $I_{IN} = -40\mu A$ V_{O7} Measured at $I_{IN} = +65\mu A$ V_{O8} Measured at $I_{IN} = -65\mu A$

Test Circuit 8

Transimpedance Amplifier (180MHz)

NE/SA5211

TYPICAL PERFORMANCE CHARACTERISTICS

NE5211 Supply Current vs Temperature

OP21310S

NE5211 Output Bias Voltage vs Temperature

OP21320S

Output Voltage vs Input Current

OP21330S

NE5211 Input Bias Voltage vs Temperature

OP21340S

NE5211 Output Bias Voltage vs Temperature

OP21350S

Differential Output Voltage vs Input Current

OP21360S

NE5211 Output Offset Voltage vs Temperature

OP21370S

NE5211 Differential Output Swing vs Temperature

OP21380S

Differential Output Voltage vs Input Current

OP21390S

Transimpedance Amplifier (180MHz)

NE/SA5211

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency

OP21400S

Gain vs Frequency

OP21410S

NE5211 Differential Transresistance vs Temperature

OP21420S

Gain vs Frequency

OP21430S

Gain vs Frequency

OP21440S

NE5211 Typical Bandwidth Distribution (70 Parts from 3 Wafer Lots)

OP21450S

NE5211 Bandwidth vs Temperature

OP21460S

Gain and Phase Shift vs Frequency

OP21470S

Gain and Phase Shift vs Frequency

OP21480S

Transimpedance Amplifier (180MHz)   NE/SA5211

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

NE5211 Output Resistance vs Temperature
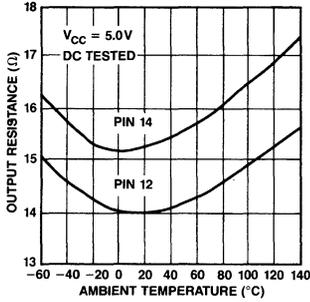
OP21490S

NE5211 Output Resistance vs Temperature
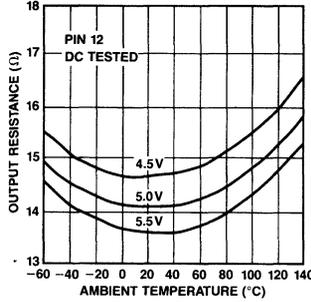
OP21500S

NE5211 Output Resistance vs Temperature
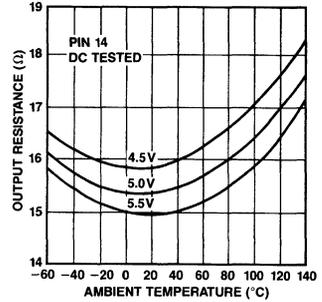
OP21510S

Output Resistance vs Frequency
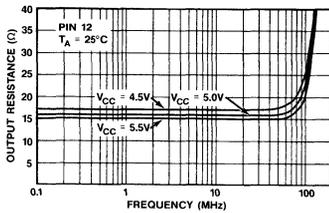
OP21520S

Output Resistance vs Frequency
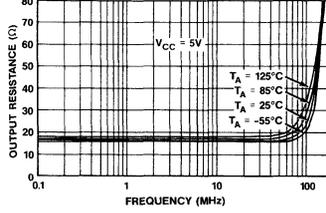
OP21530S

Output Resistance vs Frequency
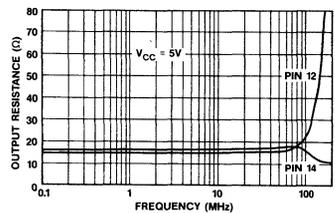
OP21540S

### NE5211 Power Supply Rejection Ratio vs Temperature
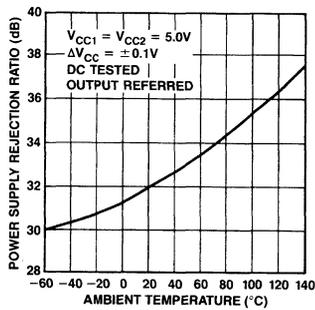

OP21550S

Group Delay vs Frequency
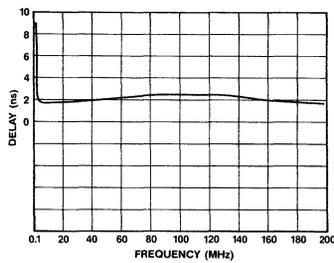
OP21560S

Transimpedance Amplifier (180MHz)

NE/SA5211

TYPICAL PERFORMANCE CHARACTERISTICS   (Continued)

Output Step Response

$V_{CC} = 5V$
$T_A = 25°C$
20mV/Div

OP21570S
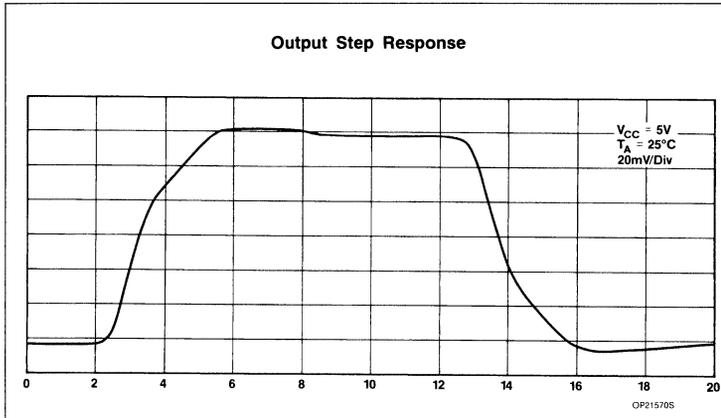
THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber-optic receivers. The NE5211 is a wide bandwidth (typically 180MHz) transimpedance amplifier designed primarily for high sensitivity. The maximum input current before output stage clipping occurs at typically 50μA. The NE5211 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q_3 is approximately the value of the feedback resistor, $R_F = 14.4k\Omega$. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT \, (diff)}}{I_{IN}} = 2R_F = 2(14.4k) = 28.8k\Omega.$$

The single-ended transresistance of the amplifier is typically 14.4kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to

Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, $A_{VOL} \approx 70$. The emitter follower Q_2 minimizes loading on Q_1. The transistor Q_4, resistor R_7, and V_{B1} provide level shifting and interface with the Q_{15}–Q_{16} differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q_{11}–Q_{12} which are biased by constant current sources. The collectors of Q_{11}–Q_{12} are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.

BANDWIDTH CALCULATIONS

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 4pF, assuming that $C_S = 0$ where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{14.4k}{71} = 203\Omega.$$

More exact calculations would yield a value of 200Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi \, R_{IN} \, C_{IN}}.$$

Assuming typical values for $R_F = 14.4k\Omega$, $R_{IN} = 200\Omega$, $C_{IN} = 4pF$:

$$f_{-3dB} = \frac{1}{2\pi \, 4pF \, 200} = 200MHz.$$

The operating point of Q1 has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, $R_{IN} = 200\Omega$ then the total input capacitance, $C_{IN} = (1 + 4)pF$ which will lead to only a 20% bandwidth reduction.

NOISE

Most of the currently installed fiber-optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very important. The input stage achieves a low input referred noise current (spectral density) of 1.8pA/$\sqrt{Hz}$. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input $_{RMS}$ noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 41nA in a 200MHz bandwidth for $C_S = 1pF$.

DYNAMIC RANGE

The electrical dynamic range can be defined as the radio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming $I_{INMAX} = 60\mu$A and a wideband noise of $I_{EQ} = 41nA_{RMS}$ for an external source capacitance of $C_S = 1pF$.

$$D_E = \frac{(Max. \; input \; current)}{(Peak \; noise \; current)}$$

Transimpedance Amplifier (180MHz)

NE/SA5211

$$= 20 \; \log \; \frac{(60 \times 10^{-6})}{(\sqrt{2} \; 41 \times 10^{-9})}$$

$$= 20 \; \log \frac{(60 \mu A)}{(58nA)} = 60dB.$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

Energy of one photon $= \dfrac{hc}{\lambda}$ watt sec (Joule)

Where h = Planck's Constant = 6.6×10^{-34} Joule sec.

c = speed of light = 3×10^8 mt/sec

c/λ = optical frequency

No. of incident photons/sec $= \dfrac{P}{hc}$ where P = optical incident power $\dfrac{}{\lambda}$

No. of generated electrons/sec $= \eta \cdot \dfrac{P}{hc}$ $\dfrac{}{\lambda}$

Where η = quantum efficiency

$= \dfrac{\text{no. of generated electron hole pairs}}{\text{no. of incident photons}}$

$\therefore \; I = \eta \cdot \dfrac{P}{hc} \cdot e$ Amps (Coulombs/sec.) $\dfrac{}{\lambda}$

where e = electron charge = 1.6×10^{-19} Coulombs

Responsivity $R = \dfrac{\eta \cdot e}{hc}$ Amp/watt $\dfrac{}{\lambda}$

$I = P \cdot R$

Assuming a data rate of 400 Mbaud (Bandwidth, B = 200MHz), the noise parameter Z may be calculated as:[1]

$$Z = \frac{i_{eq}}{qB} = \frac{41 \times 10^{-9}}{(1.6 \times 10^{-19})(200 \times 10^6)} = 1281$$

where Z is the ratio of $_{RMS}$ noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12 \; \frac{hc}{\lambda} \; B \; Z = 12 \; 2.3 \times 10^{-19}$$

200×10^6 $1281 = 707nW = -31.5dBm$,

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum

input current to the NE5210, at this input power is:

$$I_{avMIN} = q P_{avMIN} \frac{\lambda}{hc}$$

$$= \frac{707 \times 10^{-9} \times 1.6 \times 10^{-19}}{2.3 \times 10^{-19}}$$

$$= 492nA.$$

Choosing the maximum peak overload current of $I_{avMAX} = 60 \mu A$, the maximum mean optical power is:

$$P_{avMAX} = \frac{hc}{\lambda} \frac{I_{avMAX}}{q} = \frac{2.3 \times 10^{-19}}{1.6 \times 10^{-19}} 60 \times 10^{-6}$$

$$= 86mW \text{ or } -10.6dBm.$$

Thus the optical dynamic range, D_o is:

$$D_o = P_{avMAX} - P_{avMIN} = -31.5 - (-10.6)$$
$$= 20.8dB.$$

This represents the maximum limit attainable with the NE5211 operating at 200MHz band-

width, with a half mark/half space digital transmission at 820nm wavelength.

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5211 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout such that Ground 1 and Ground 2 have very low impedance paths have produced the best results. This was accomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe

Figure 1. NESA5211 Block Diagram

Figure 2. Trans-Impedance Amplifier

1. S. D. Personick, *Optical Fiber Transmission Systems*, Plenum Press, NY, 1981, Chapter 3.

Transimpedance Amplifier (180MHz)

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and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photo-diode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality 0.1μF high-frequency capacitor be inserted between V_{CC1} and V_{CC2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of 0.1μF capacitors with 10μF tantalum capaci-

tors from each supply, V_{CC1} and V_{CC2}, to the ground plane should provide adequate de-coupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

Figure 4 depicts a 50Mb/s TTL fiber-optic receiver using the BPF31, 850nm LED, the NE5211 and the NE5214 post amplifier. For more information on this circuit, please refer to Application Brief AB1432.

Figure 3. Shunt-Series Input Stage

Figure 4. A 50Mb/s Fiber Optic Receiver Using NE5211/NE5214

Signetics
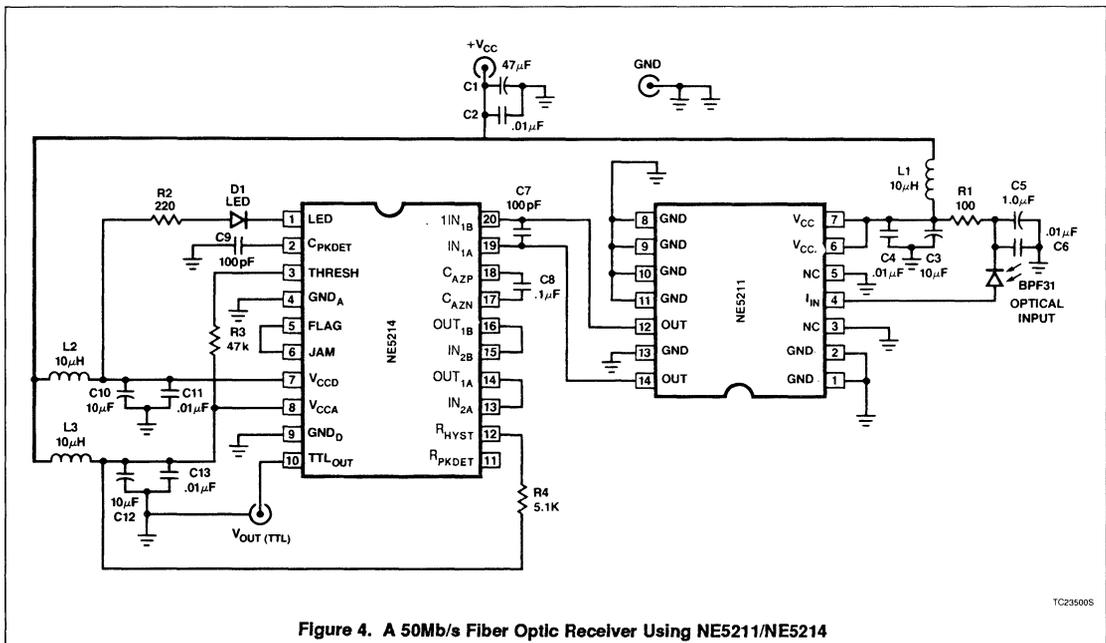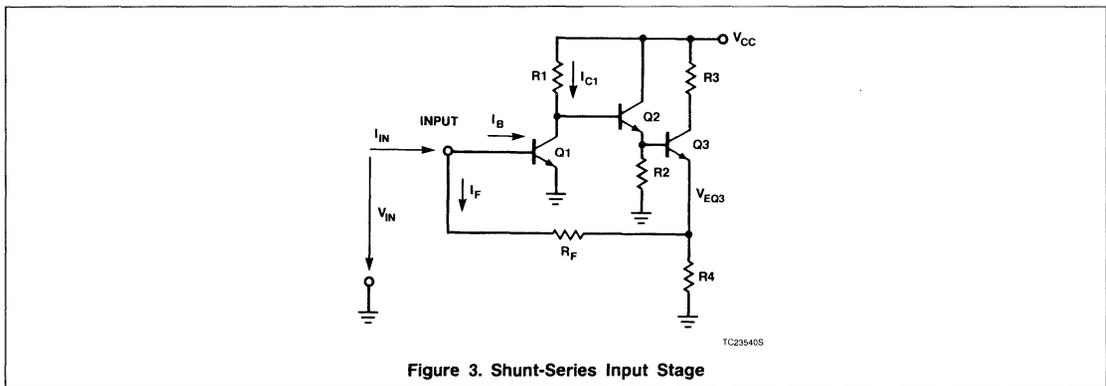
NE/SA/SE5212
Transimpedance Amplifier (140MHz)

Product Specification

DESCRIPTION

The NE/SA/SE5212 is a 14kΩ transimpedance, wideband, low noise differential output amplifier, particularly suitable for signal recovery in fiber optic receivers and in any other applications where very low signal levels obtained from high-impedance sources need to be amplified.

FEATURES

- **Extremely low noise: 2.5pA/$\sqrt{Hz}$**
- **Single 5V supply**
- **Large bandwidth: 140MHz**
- **Differential outputs**
- **Low input/output impedances**
- **High-power supply rejection ratio**
- **14kΩ differential transresistance**

APPLICATIONS

- **Fiber-optic receivers, analog and digital**
- **Current-to-voltage converters**
- **Wideband gain block**
- **Medical and scientific instrumentation**
- **Sensor preamplifiers**
- **Single-ended to differential conversion**
- **Low noise RF amplifiers**
- **RF signal processing**

PIN CONFIGURATION

N, FE, D Packages

Pin		Pin	
I_{IN}	1	8	GND_2
V_{CC}	2	7	OUT (−)
GND_1	3	6	GND_2
GND_1	4	5	OUT (+)

CD13250S
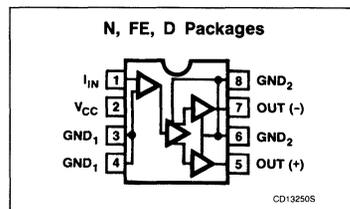
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE5212N
8-Pin Plastic SO	0 to +70°C	NE5212D
8-Pin Ceramic DIP	0 to +70°C	NE5212FE
8-Pin Plastic SO	−40°C to +85°C	SA5212D
8-Pin Plastic DIP	−40°C to +85°C	SA5212N
8-Pin Ceramic DIP	−40°C to +85°C	SA5212FE
8-Pin Plastic DIP	−55°C to +125°C	SE5212N
8-Pin Ceramic DIP	−55°C to +125°C	SE5212FE

Transimpedance Amplifier (140MHz)   NE/SA/SE5212

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING			UNIT
		NE5212	SA5212	SE5212	
V_{CC}	Power Supply	6	6	6	V
$P_{D\ MAX}$	Power dissipation, $T_A = 25°C$ (still air)[1] 8-Pin Plastic DIP 8-Pin Plastic SO 8-Pin Cerdip	1100 750 750	1100 750 750	1100 750 750	mW mW mw
$I_{IN\ MAX}$	Maximum input current[2]	5	5	5	mA
T_A	Operating ambient temperature range	0 to 70	−40 to 85	−55 to 125	°C
T_J	Operating junction	−55 to 150	−55 to 150	−55 to 150	°C
T_{STG}	Storage temperature range	−65 to 150	−65 to 150	−65 to 150	°C

NOTES:
1. Maximum dissipation is determined by the operating ambient temperature and the thermal resistance:
   8-Pin Plastic DIP: 110°C/W
   8-Pin Plastic SO: 160°C/W
   8-Pin Cerdip: 165°C/W
2. The use of a pull-up resistor to V_{CC}, for the PIN diode, is recommended

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	4.5 to 5.5	V
T_A	Ambient temperature ranges NE Grade SA Grade SE Grade	0 to +70 −40 to +85 −55 to +125	°C °C °C
T_J	Junction temperature ranges NE Grade SA Grade SE Grade	0 to +90 −40 to +105 −55 to +145	°C °C °C

DC ELECTRICAL CHARACTERISTICS
Minimum and Maximum limits apply over operating temperature range at $V_{CC} = 5V$, unless otherwise specified. Typical data applies at $V_{CC} = 5V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5212			SA/SE5212			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{IN}	Input bias voltage		0.6	0.8	0.95	0.55	0.8	1.05	V
$V_{O\pm}$	Output bias voltage		2.8	3.3	3.7	2.5	3.3	3.8	V
V_{OS}	Output offset voltage				80			120	mV
I_{CC}	Supply current		21	26	32	20	26	33	mA
I_{OMAX}	Output sink/source current		3	4		3	4		mA
I_{IN}	Input current (2% linearity)	Test Circuit 6, Procedure 2	±60	±80		±40	±80		µA
$I_{N\ MAX}$	Maximum input current overload threshold	Test Circuit 6, Procedure 4	±80	±120		±60	±120		µA

Transimpedance Amplifier (140MHz)

NE/SA/SE5212

AC ELECTRICAL CHARACTERISTICS Minimum and Maximum limits apply over operating temperature range at $V_{CC} = 5V$, unless otherwise specified. Typical data applies at $V_{CC} = 5V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5212			SA/SE5212			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_T	Transresistance (differential output)	DC tested, $R_L = \infty$ Test Circuit 6, Procedure 1	9.8	14	18.2	9.0	14	19	$k\Omega$
R_O	Output resistance (differential output)	DC tested	14	30	42	14	30	46	Ω
R_T	Transresistance (single-ended output)	DC tested, $R_L = \infty$	4.9	7	9.1	4.5	7	9.5	$k\Omega$
R_O	Output resistance (single-ended output)	DC tested	7	15	21	7	15	23	Ω
f_{3dB}	Bandwidth (−3dB)	Test Circuit 1 D package, $T_A = 25°C$ N, FE packages, $T_A = 25°C$	100 100	140 120		100 100	140 120		MHz MHz
R_{IN}	Input resistance		75	110	143	70	110	150	Ω
C_{IN}	Input capacitance			10	15		10	18	pF
$\Delta R/\Delta V$	Transresistance power supply sensitivity	$V_{CC} = 5 \pm 0.5V$		9.6			9.6		%/V
$\Delta R/\Delta T$	Transresistance ambient temperature sensitivity	D package $\Delta T_A = T_{A\ MAX} - T_{A\ MIN}$		0.05			0.05		%/°C
I_N	RMS noise current spectral density (referred to input)	Test Circuit 2 $f = 10MHz$ $T_A = 25°C$		2.5			2.5		$pA/\sqrt{Hz}$
I_T	Integrated RMS noise current over the bandwidth (referred to input) $C_S = 0$[1]	$T_A = 25°C$ Test Circuit 2 $\Delta f = 50MHz$ $\Delta f = 100MHz$ $\Delta f = 200MHz$		20 27 40			20 27 40		nA nA nA
		$C_S = 1pF$ $\Delta f = 50MHz$ $\Delta f = 100MHz$ $\Delta f = 200MHz$		22 32 52			22 32 52		nA nA nA
PSRR	Power supply rejection ratio[2]	Any package DC tested $\Delta V_{CC} = 0.1V$ Equivalent AC Test Circuit 3	26	33		20	33		dB
PSRR	Power supply rejection ratio[2] (ECL configuration)	Any package $f = 0.1MHz$[1] Test Circuit 4		23			23		dB
$V_{O\ MAX}$	Maximum differential output voltage swing	$R_L = \infty$ Test Circuit 6, Procedure 3	2.4	3.2		1.7	3.2		V_{P-P}
$V_{IN\ MAX}$	Maximum input amplitude for output duty cycle of $50 \pm 5\%$[3]	Test Circuit 5		325			325		mV_{P-P}
t_R	Rise time for 50mV output signal[4]	Test Circuit 5		2.0			2.0		ns

NOTES:
1. Package parasitic capacitance amounts to about 0.2pF.
2. PSRR is output referenced and is circuit board layout dependent at higher frequencies. For best performance use RF filter in V_{CC} line.
3. Guaranteed by linearity and over load tests.
4. t_R defined as 20 – 80% rise time. It is guaranteed by −3dB bandwidth test.

Transimpedance Amplifier (140MHz)

NE/SA/SE5212

TEST CIRCUITS

SINGLE-ENDED	DIFFERENTIAL
$R_t = \dfrac{V_{OUT}}{V_{IN}}\,R = 2 \times S21 \times R$	$R_t \simeq \dfrac{V_{OUT}}{V_{IN}}\,R = 4 \times S21 \times R$
$R_O = Z_O\left\|\dfrac{1 + S22}{1 - S22}\right\| - 33$	$R_O = 2Z_O\left\|\dfrac{1 + S22}{1 - S22}\right\| - 66$

Test Circuit 1

Test Circuit 2

Test Circuit 3

Transimpedance Amplifier (140MHz)
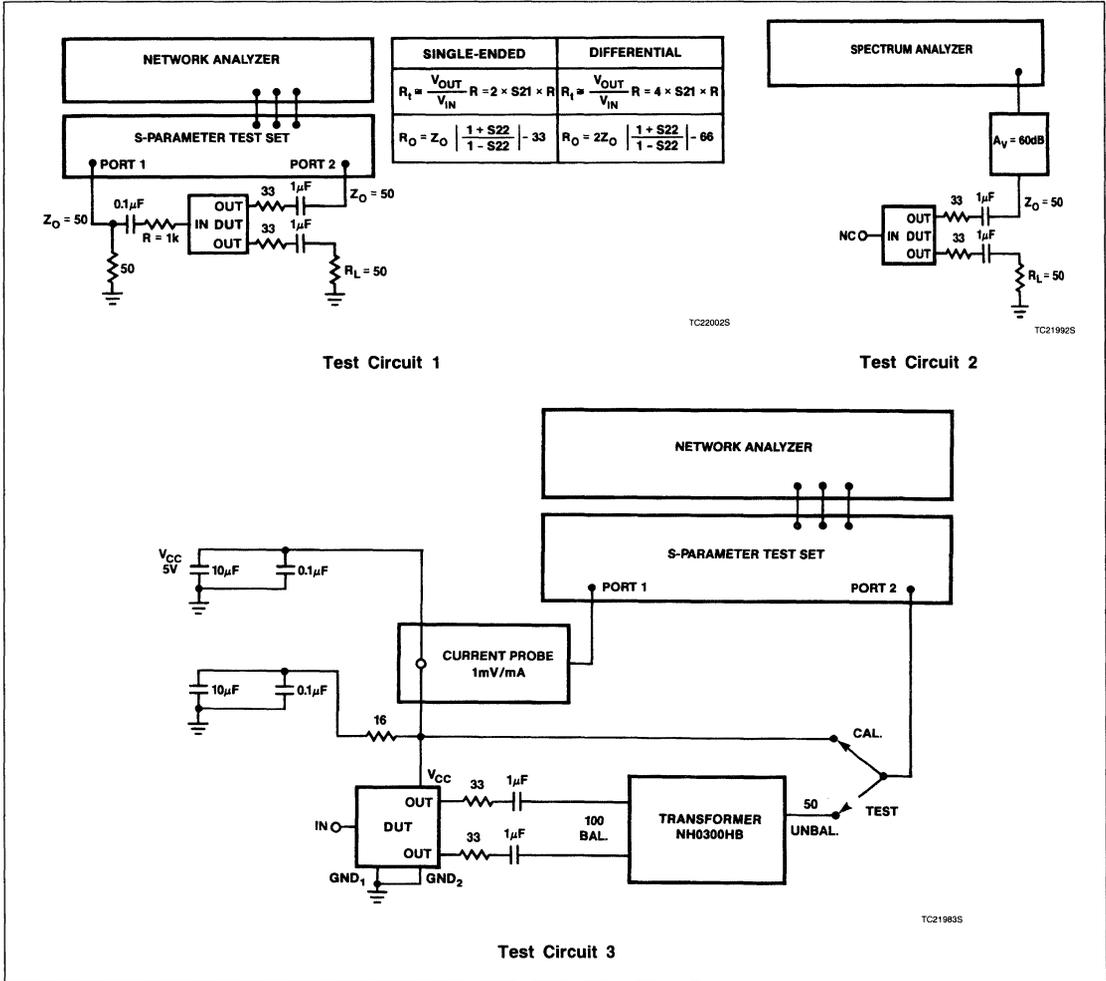
NE/SA/SE5212

TEST CIRCUITS (Continued)

Test Circuit 4
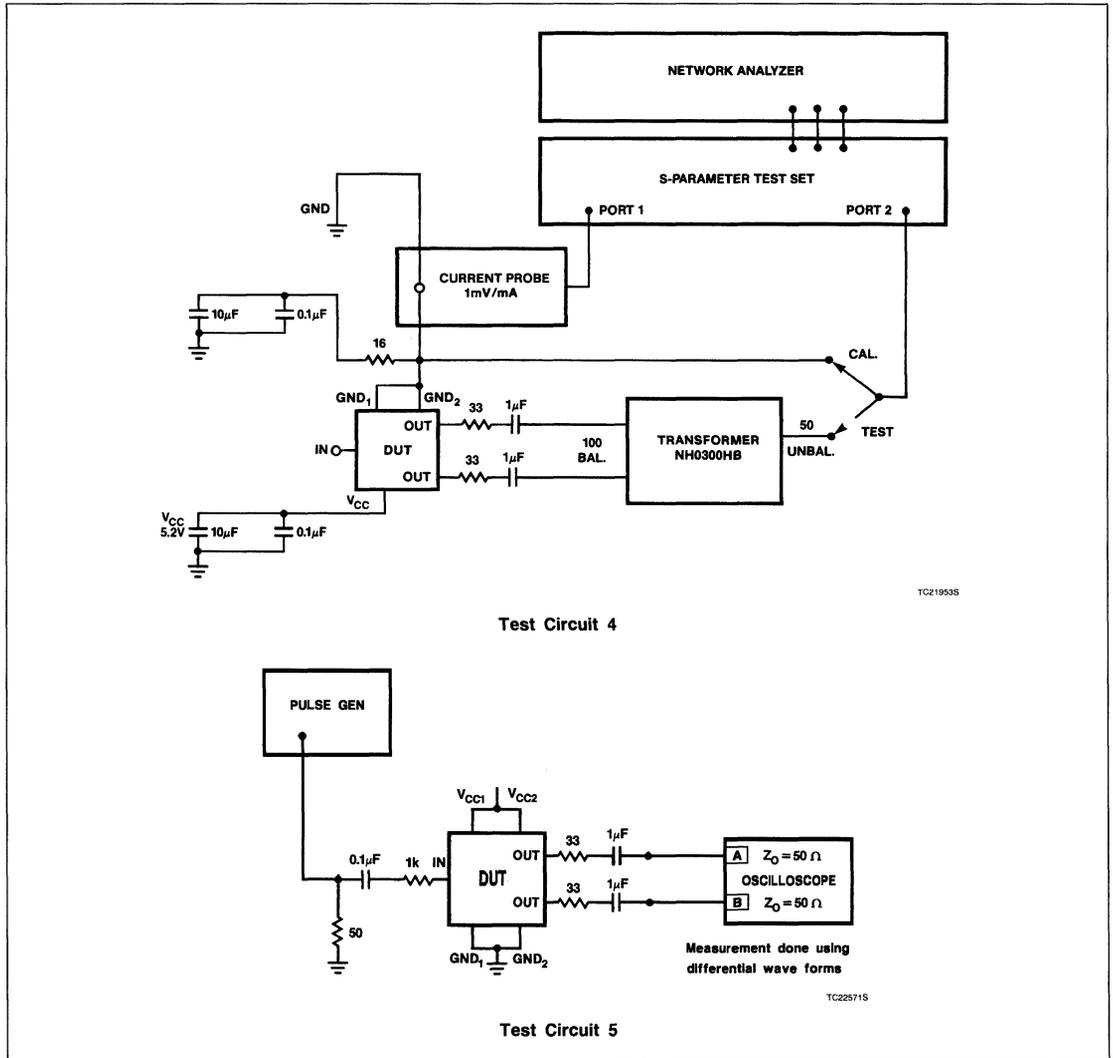
Test Circuit 5

Transimpedance Amplifier (140MHz)

NE/SA/SE5212

TEST CIRCUITS (Continued)

TC23462S

Typical V_O (Differential) vs I_{IN}

OP20990S

NE5212 TEST CONDITIONS

|	
Procedure 1	R_T measured at $30\mu A$ $R_T = (V_{O1} - V_{O2})/(+30\mu A - (-30\mu A))$ Where: V_{O1} Measured at $I_{IN} = +30\mu A$ V_{O2} Measured at $I_{IN} = -30\mu A$
Procedure 2	Linearity $= 1 - ABS((V_{OA} - V_{OB}/(V_{O3} - V_{O4}))$ Where: V_{O3} Measured at $I_{IN} = +60\mu A$ V_{O4} Measured at $I_{IN} = -60\mu A$ $V_{OA} = R_T \ * \ (+60\mu A) + V_{O8}$ $V_{OB} = R_T \ * \ (-60\mu A) + V_{O8}$
Procedure 3	$V_{OMAX} = V_{O7} - V_{O8}$ Where: V_{O7} Measured at $I_{IN} = +130\mu A$ V_{O8} Measured at $I_{IN} = -130\mu A$
Procedure 4	$I_{IN\ MAX}$ Test Pass Conditions: $V_{O7} - V_{O5} > 50mV$ and $V_{O6} - V_{O5} > 50mV$ Where: V_{O5} Measured at $I_{IN} = +80\mu A$ V_{O6} Measured at $I_{IN} = -80\mu A$ V_{O7} Measured at $I_{IN} = +130\mu A$ V_{O8} Measured at $I_{IN} = -130\mu A$

Test Circuit 6

Transimpedance Amplifier (140MHz)

NE/SA/SE5212

TYPICAL PERFORMANCE CHARACTERISTICS

NE5212 Supply Current vs Temperature

V_{CC} = 5.0V

SUPPLY CURRENT (mA) vs AMBIENT TEMPERATURE (°C)

OP21070S

NE5212 Output Bias Voltage vs Temperature

V_{CC} = 5.0V

INPUT BIAS VOLTAGE (mV) vs AMBIENT TEMPERATURE (°C)

OP21080S

NE5212 Output Bias Voltage vs Temperature

V_{CC} = 5.0V

PIN 5
PIN 7

OUTPUT BIAS VOLTAGE (V) vs AMBIENT TEMPERATURE (°C)

OP21090S

NE5212 Differential Output Swing vs Temperature

V_{CC} = 5.0V
DC TESTED
RL = ∞

DIFFERENTIAL OUTPUT SWING (V) vs AMBIENT TEMPERATURE (°C)

OP21100S

NE5212 Output Offset Voltage vs Temperature

V_{CC} = 5.0V
V_{OS} = V_{OUT5} − V_{OUT7}

OUTPUT OFFSET VOLTAGE (mV) vs AMBIENT TEMPERATURE (°C)

OP21110S

NE5212 Differential Transresistance vs Temperature

V_{CC} = 5.0V
DC TESTED
RL = ∞

DIFFERENTIAL TRANSRESISTANCE (kΩ) vs AMBIENT TEMPERATURE (°C)

OP21120S

NE5212 Power Supply Rejection Ratio vs Temperature

V_{CC} = 5.0V
ΔV_{CC} = ±0.1V
DC TESTED
OUTPUT REFERRED

POWER SUPPLY REJECTION RATIO (dB) vs AMBIENT TEMPERATURE (°C)

OP21130S

NE5212 Output Resistance vs Temperature

V_{CC} = 5.0V
DC TESTED

PIN 7
PIN 5

OUTPUT RESISTANCE (Ω) vs AMBIENT TEMPERATURE (°C)

OP21140S

NE5212 Typical Bandwidth Distribution (75 Parts from 3 Wafer Lots)

PIN 5
SINGLE-ENDED
R_L = 50Ω

N, F PKG
V_{CC} = 5.0V
T_A = 25°C

POPULATION (%) vs FREQUENCY (MHz)

112.5 122.5 132.5 142.5 152.5 162.5

OP21150S

Transimpedance Amplifier (140MHz)

NE/SA/SE5212

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency

OP21160S

Gain vs Frequency

OP21170S

Output Resistance vs Frequency

OP21180S

Output Resistance vs Frequency

OP21190S

Gain vs Frequency OP21230S

OP21200S

Gain vs Frequency OP21240S

OP21210S

Gain and Phase Shift vs Frequency

OP21220S

Gain and Phase Shift vs Frequency

Gain and Phase Shift vs Frequency

Transimpedance Amplifier (140MHz)

NE/SA/SE5212

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain and Phase Shift vs Frequency

OP21250S

Differential Output Voltage vs Input Current

OP21260S

Differential Output Voltage vs Input Current

OP21270S

Output Voltage vs Input Current

OP21250S

Group Delay vs Frequency

OP21260S

Output Step Response

OP21300S

Transimpedance Amplifier (140MHz)

NE/SA/SE5212

THEORY OF OPERATION

Transimpedance amplifiers have been widely used as the preamplifier in fiber optic receivers. The NE5212 is a wide bandwidth (typically 130MHz) transimpedance amplifier designed primarily for high sensitivity. The maximum input current before output stage clipping occurs at typically 120μA. The NE5212 is a bipolar transimpedance amplifier which is current driven at the input and generates a differential voltage signal at the outputs. The forward transfer function is therefore a ratio of the differential output voltage to a given input current with the dimensions of ohms. The main feature of this amplifier is a wideband, low-noise input stage which is desensitized to photodiode capacitance variations. When connected to a photodiode of a few picoFarads, the frequency response will not be degraded significantly. Except for the input stage, the entire signal path is differential to provide improved power-supply rejection and ease of interface to ECL type circuitry. A block diagram of the circuit is shown in Figure 1. The input stage (A1) employs shunt-series feedback to stabilize the current gain of the amplifier. The transresistance of the amplifier from the current source to the emitter of Q3 is approximately the value of the feedback resistor, $R_F = 7.2k\Omega$. The gain from the second stage (A2) and emitter followers (A3 and A4) is about two. Therefore, the differential transresistance of the entire amplifier, R_T is

$$R_T = \frac{V_{OUT}(diff)}{I_{IN}} = 2R_F = 2(7.2k) = 14.4k\Omega.$$

The single-ended transresistance of the amplifier is typically 7.2kΩ.

The simplified schematic in Figure 2 shows how an input current is converted to a differential output voltage. The amplifier has a single input for current which is referenced to Ground 1. An input current from a laser diode, for example, will be converted into a voltage by the feedback resistor R_F. The transistor Q1 provides most of the open loop gain of the circuit, $A_{VOL} \approx 70$. The emitter follower Q2 minimizes loading on Q1. The transistor Q4, resistor R7, and V_{B1} provide level shifting and interface with the Q15–Q16 differential pair of the second stage which is biased with an internal reference, V_{B2}. The differential outputs are derived from emitter followers Q11–Q12 which are biased by constant current sources. The collectors of Q11–Q12 are bonded to an external pin, V_{CC2}, in order to reduce the feedback to the input stage. The output impedance is about 17Ω single-ended. For ease of performance evaluation, a 33Ω resistor is used in series with each output to match to a 50Ω test system.


Figure 1. NE5212 – Block Diagram
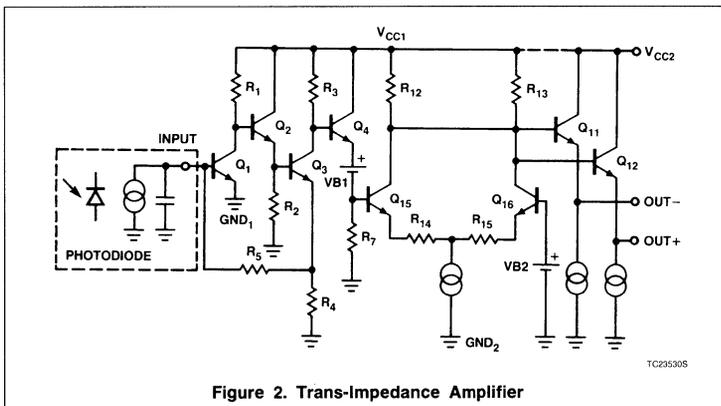
Figure 2. Trans-Impedance Amplifier

BANDWIDTH CALCULATIONS:

The input stage, shown in Figure 3, employs shunt-series feedback to stabilize the current gain of the amplifier. A simplified analysis can determine the performance of the amplifier. The equivalent input capacitance, C_{IN}, in parallel with the source, I_S, is approximately 10pF, assuming that $C_S = 0$ where C_S is the external source capacitance.

Since the input is driven by a current source the input must have a low input resistance. The input resistance, R_{IN}, is the ratio of the incremental input voltage, V_{IN}, to the corresponding input current, I_{IN} and can be calculated as:

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{R_F}{1 + A_{VOL}} = \frac{7.2k}{70} = 103\Omega.$$

More exact calculations would yield a value of 110Ω.

Thus C_{IN} and R_{IN} will form the dominant pole of the entire amplifier;

$$f_{-3dB} = \frac{1}{2\pi \ R_{IN} \ C_{IN}}.$$

Assuming typical values for $R_F = 7.2k\Omega$, $R_{IN} = 110\Omega$, $C_{IN} = 10pF$:

$$f_{-3dB} = \frac{1}{2\pi \ 110 \ 10 \times 10^{-12}} = 145MHz.$$

The operating point of Q1 has been optimized for the lowest current noise without introducing a second dominant pole in the pass-band. All poles associated with subsequent stages have been kept at sufficiently high enough frequencies to yield an overall single pole response. Although wider bandwidths have been achieved by using a cascode input stage configuration, the present solution has the advantage of a very uniform, highly desensitized frequency response because the Miller effect dominates over the external photodiode and stray capacitances. For example, assuming a source capacitance of 1pF, input stage voltage gain of 70, $R_{IN} = 110\Omega$ then the total input capacitance, $C_{IN} = (1 + 10)$ pF which will lead to only a 9% bandwidth reduction.

NOISE

Most of the currently installed fiber optic systems use non-coherent transmission and detect incident optical power. Therefore, receiver noise performance becomes very im-

Transimpedance Amplifier (140MHz)

NE/SA/SE5212

Figure 3. Shunt-Series Input Stage

portant. The input stage achieves a low input referred noise current (spectral density) of $2.5pA/\sqrt{Hz}$. The transresistance configuration assures that the external high value bias resistors often required for photodiode biasing will not contribute to the total noise system noise. The equivalent input RMS noise current is strongly determined by the quiescent current of Q_1, the feedback resistor R_F, and the bandwidth; however, it is not dependent upon the internal Miller-capacitance. The measured wideband noise was 52nA in a 200MHz bandwidth for $C_S = 1pF$.

DYNAMIC RANGE:

The electrical dynamic range can be defined as the radio of maximum input current to the peak noise current:

Electrical dynamic range, D_E, in a 200MHz bandwidth assuming $I_{INMAX} = 120\mu A$ and a wideband noise of $I_{EQ} = 52nA_{RMS}$ for an external source capacitance of $C_S = 1pF$.

$$D_E = \frac{(\text{Max. input current})}{(\text{Peak noise current})}$$

$$= 20 \ \log \ \frac{(120 \times 10^{-6})}{(\sqrt{2} \ 52 \times 10^{-9})}$$

$$= 20 \ \log \ \frac{(120\mu A)}{(73nA)} = 64dB.$$

In order to calculate the optical dynamic range the incident optical power must be considered.

For a given wavelength λ;

Energy of one photon $= \dfrac{hc}{\lambda}$ watt sec (Joule)

Where h = Planck's Constant = 6.6×10^{-34} Joule sec.
    c = speed of light = 3×10^8 mt/sec
    c/λ = optical frequency

No. of incident photons/sec $= \dfrac{P}{hc}$ where P = optical incident power λ

No. of generated electrons/sec $= \eta \cdot \dfrac{P}{hc}$ λ

Where η = quantum efficiency

$$= \frac{\text{no. of generated electron hole pairs}}{\text{no. of incident photons}}$$

$$\therefore I = \eta \cdot \dfrac{P}{\lambda} \cdot hc \cdot e \text{ Amps (Coulombs/sec.)}$$

where e = electron charge = 1.6×10^{-19} Coulombs

Responsivity $R = \dfrac{\eta \cdot e}{\dfrac{hc}{\lambda}}$ Amp/watt

$I = P \cdot R$

Assuming a data rate of 400 Mbaud (Bandwidth, B = 200MHz), the noise parameter Z may be calculated as:

$$Z = \frac{i_{eq}}{qB} = \frac{52 \times 10^{-9}}{(1.6 \times 10^{-19}) (200 \times 10^6)} = 1625$$

where Z is the ratio of RMS noise output to the peak response to a single hole-electron pair. Assuming 100% photodetector quantum efficiency, half mark/half space digital transmission, 850nm lightwave and using Gaussian approximation, the minimum required optical power to achieve 10^{-9} BER is:

$$P_{avMIN} = 12 \ \frac{hc}{\lambda} \ B \ Z = 12 \ 2.3 \times 10^{-19}$$

$200 \times 10^6 \ 1625 = 897nW = -30.5dBm,$

where h is Planck's Constant, c is the speed of light, λ is the wavelength. The minimum

a. Non-Inverting 20dB Amplifier

b. Inverting 20dB Amplifier

c. Differential 20dB Amplifier
Figure 4

input current to the NE5212, at this input power is:

$$I_{avMIN} = qP_{avMIN}\frac{\lambda}{hc}$$

$$= \frac{897 \times 10^{-9} \times 1.6 \times 10^{-19}}{2.3 \times 10^{-19}}$$

$$= 624nA.$$

Choosing the maximum peak overload current of $I_{avMAX} = 120\mu A$, the maximum mean optical power is:

$$P_{avMAX} = \frac{hc \ I_{avMAX}}{\lambda \ q} = \frac{2.3 \times 10^{-19}}{1.6 \times 10^{-19}} = 120 \times 10^{-6}$$

$$= 86mW \text{ or } -7.6 \text{ dBm.}$$

Thus the optical dynamic range, D_o is:

$$D_o = P_{avMAX} - P_{avMIN} = -30.5 - (-7.6) = 22.8dB.$$

This represents the maximum limit attainable with the NE5212 operating at 200MHz bandwidth, with a half mark/half space digital transmission at 820nm wavelength.

[1] S. D. Personick, *Optical Fiber Transmission Systems,* Plenum Press, NY, 1981, Chapter 3.

Transimpedance Amplifier (140MHz)

NE/SA/SE5212

Figure 5. Variable Gain Circuit

APPLICATION INFORMATION

Package parasitics, particularly ground lead inductances and parasitic capacitances, can significantly degrade the frequency response. Since the NE5212 has differential outputs which can feed back signals to the input by parasitic package or board layout capacitances, both peaking and attenuating type frequency response shaping is possible. Constructing the board layout such that Ground 1 and Ground 2 have very low impedance paths have produced the best results. This was acomplished by adding a ground-plane stripe underneath the device connecting Ground 1, Pins 8–11, and Ground 2, Pins 1 and 2 on opposite ends of the SO14 package. This ground-plane stripe also provides isolation between the output return currents flowing to either V_{CC2} or Ground 2 and the input photodiode currents to flowing to Ground 1. Without this ground-plane stripe and with large lead inductances on the board, the part may be unstable and oscillate near 800MHz. The easiest way to realize that the part is not functioning normally is to measure the DC voltages at the outputs. If they are not close to their quiescent values of 3.3V (for a 5V supply), then the circuit may be oscillating. Input pin layout necessitates that the photodiode be physically very close to the input and Ground 1. Connecting Pins 3 and 5 to Ground 1 will tend to shield the input but it will also tend to increase the capacitance on the input and slightly reduce the bandwidth.

As with any high-frequency device, some precautions must be observed in order to enjoy reliable performance. The first of these is the use of a well-regulated power supply. The supply must be capable of providing

varying amounts of current without significantly changing the voltage level. Proper supply bypassing requires that a good quality $0.1\mu F$ high-frequency capacitor be inserted between V_{cc1} and V_{cc2}, preferably a chip capacitor, as close to the package pins as possible. Also, the parallel combination of $0.1\mu F$ capacitors with $10\mu F$ tantalum capacitors from each supply, V_{cc1} and V_{cc2}, to the ground plane should provide adequate decoupling. Some applications may require an RF choke in series with the power supply line. Separate analog and digital ground leads must be maintained and printed circuit board ground plane should be employed whenever possible.

BASIC CONFIGURATION

A trans resistance amplifier is a current-to-voltage converter. The forward transfer function then is defined as voltage out divided by current in, and is stated in ohms. The lower the source resistance, the higher the gain. The NE5212 has a differential transresistance of $14k\Omega$ typically and a single-ended transresistance of $7k\Omega$ typically. The device has two outputs: inverting and non-inverting. The output voltage in the differential output mode is twice that of the output voltage in the single-ended mode. Although the device can be used without coupling capacitors, more care is required to avoid upsetting the internal bias nodes of the device. Figure 4 shows some basic configurations.

VARIABLE GAIN

Figure 5 shows a variable gain circuit using the NE5212 and the NE5230 low voltage op

amp. This op amp is configured in a non-inverting gain of five. The output drives the gate of the SD210 DMOS FET. The series resistance of the FET changes with this output voltage which in turn changes the gain of the NE5212. This circuit has a distortion of less than 1% and a 25dB range, from $-42.2dBm$ to $-15.9dBm$ at 50MHz, and a 45dB range, from $-60dBm$ to $-14.9dBm$ at 10MHz with 0 to 1V of control voltage at V_C.

16MHz CRYSTAL OSCILLATOR

Figure 6 shows a 16MHz crystal oscillator operating in the series resonant mode using the NE5212. The non-inverting input is fed back to the input of the NE5212 in series with a 2pF capacitor. The output is taken from the inverting output.
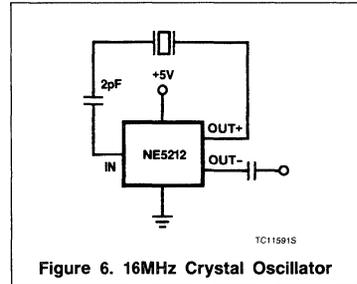

Figure 6. 16MHz Crystal Oscillator

DIGITAL FIBER OPTIC RECEIVER

Figures 7 and 8 show a fiber optic receiver using off-the-shelf components.

The receiver shown in Figure 7 uses the NE5212, the Signetics 10116 ECL line receiver, and Philips/Amperex BPF31 PIN diode. The circuit is a capacitor-coupled receiver and utilizes positive feedback in the last stage to provide the hysteresis. The amount of hysteresis can be tailored to the individual application by changing the values of the feedback resistors to maintain the desired balance between noise immunity and sensitivity. At room temperature, the circuit operates at 50Mbaud with a BER of 10E-10 and over the automotive temperature range at 40Mbaud with a BER of 10E-9. Higher speed experimental diodes have been used to operate this circuit at 220Mbaud with a BER of 10E-10.

Figure 8 depicts a TTL receiver using the NE5212 and the NE5214 fast amplifier system along with the Philips/Amperex PIN diode. The system shown is optimized for 50 Mb/s Non Return to Zero (NRZ) data. A link status indication is provided along with a jamming function when the input level is below a user-programmable threshold level.

# Transimpedance Amplifier (140MHz)

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NOTE:
1. Tie all V_{BB} points together.
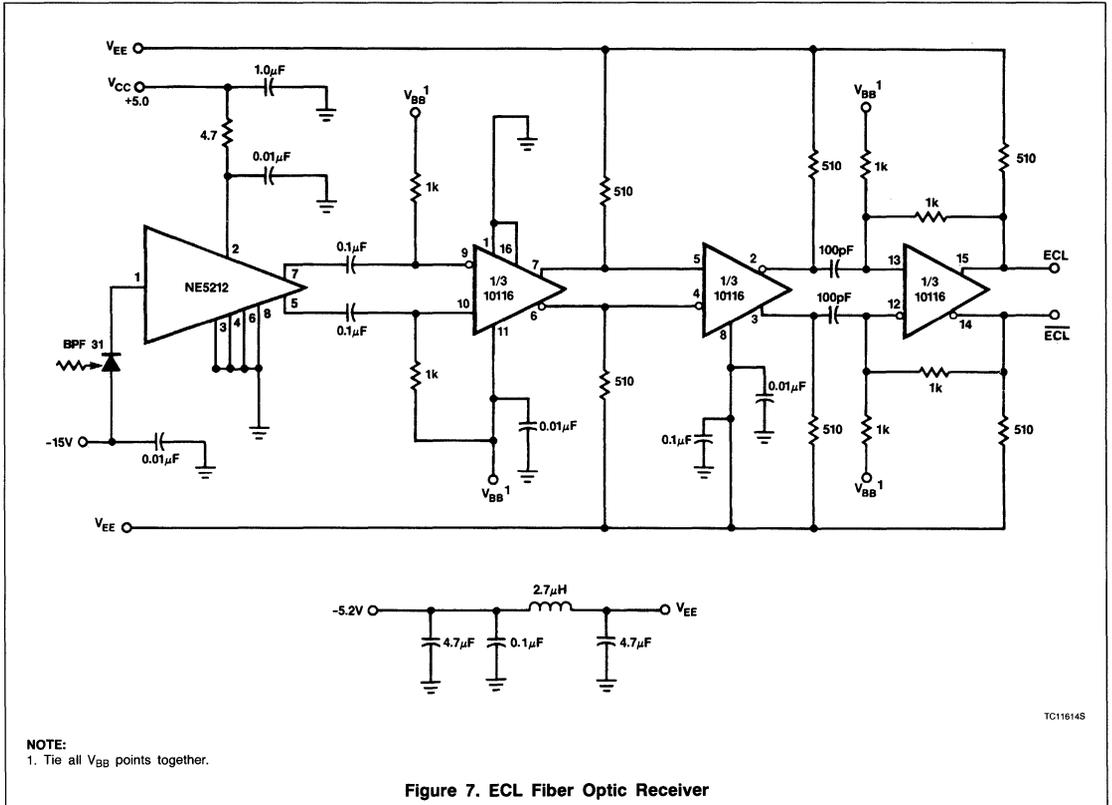
Figure 7. ECL Fiber Optic Receiver

Transimpedance Amplifier (140MHz)

NE/SA/SE5212
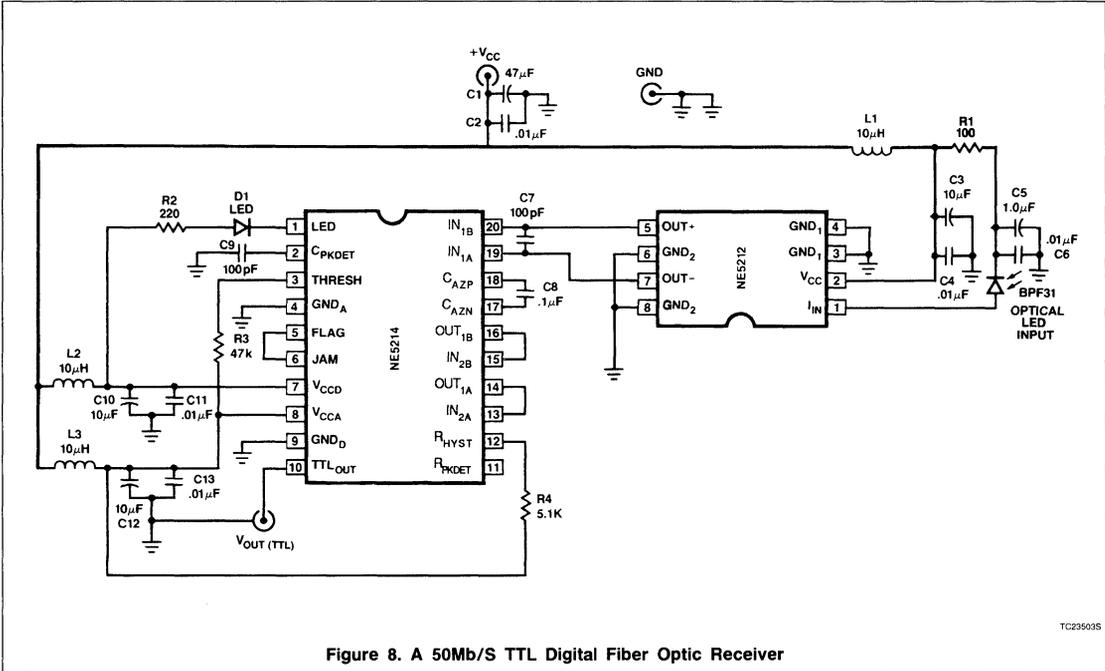
Figure 8. A 50Mb/S TTL Digital Fiber Optic Receiver

TC23503S

Signetics

NE/SA5214 Fiber Optic Postamplifier with Link Status Indicator

Preliminary Specification

Linear Products

DESCRIPTION

THE NE/SA5214 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5214 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212 transimpedance amplifiers. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide noise filtering, adjustable input thresholds and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, insuring a low Bit Error Rate (BER). An Auto-Zero loop can be used to minimize the number of external coupling capacitors to one. A signal absent flag indicates when signals are below threshold. Additionally, the low signal condition forces the overall TTL output to a logical Low level. User interaction with this "jamming" system is available. The NE/SA5214 is packaged in a standard 20-pin surface-mount package and typically consumes 42mA from a standard 5V supply. The NE/SA5214 is designed as a companion to the NE/SA5211/5212 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the postamplifier inputs. The NE/SA5212/5214 or NE/SA5211/5214 combinations convert nanoamps of photodetector current into standard digital TTL levels.

FEATURES

- **Postamp for the NE/SA5211/5212 preamplifier family**
- **Wideband operation: typical 75MHz (100MBaud NRZ)**
- **Interstage filtering/equalization possible**
- **Single 5V supply**
- **Low signal flag**
- **Low signal output disable**
- **Link status threshold and hysteresis programmable**
- **LED driver (normally ON with above threshold signal)**
- **Fully differential for excellent PSRR**
- **Auto-zero loop for DC offset cancellation**
- **2kV ElectroStatic Discharge (ESD) protection**

APPLICATIONS

- **Fiber optics**
- **Communication links in Industrial and/or Telecom environment with high EMI/RFI**
- **Local Area Networks (LAN)**
- **Metropolitan Area Networks (MAN)**
- **Synchronous Optical Networks (SONET)**
- **RF limiter**

PIN CONFIGURATION

D¹ Package

Pin	Left		Right	Pin
1	LED		IN$_{1B}$	20
2	C$_{PKDET}$		IN$_{1A}$	19
3	THRESH		C$_{AZP}$	18
4	GND$_A$		C$_{AZN}$	17
5	FLAG		OUT$_{1B}$	16
6	JAM		IN$_{2B}$	15
7	V$_{CCD}$		OUT$_{1A}$	14
8	V$_{CCA}$		IN$_{2A}$	13
9	GND$_D$		R$_{HYST}$	12
10	V$_{OUT}$		R$_{PKDET}$	11

TOP VIEW

CD15320S

NOTE:
1. SOL — Released in large SO package only.

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED driver. Open collector output transistor with 125Ω series limiting resistor. An above threshold signal turns this transistor ON.
2	C$_{PKDET}$	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND$_A$	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is LOW, there is data present above the threshold. This pin is normally connected to the JAM pin and has a TTL fanout of two.
6	JAM	Input to inhibit data flow. Sending the pin HIGH forces TTL DATA OUT ON, Pin 10, LOW. This pin is normally connected to the FLAG pin and is TTL-compatible.
7	V$_{CCD}$	Power supply pin for the digital portion of the chip.
8	V$_{CCA}$	Power supply pin for the analog portion of the chip.
9	GND$_D$	Device digital ground pin.
10	V$_{OUT}$	TTL output pin with a fanout of five.
11	R$_{PKDET}$	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C$_{PKDET}$.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL	0 to +70°C	NE5214D
20-Pin Plastic SOL	−40°C to +85°C	SA5214D

Postamplifier with Link Status Indicator   NE/SA5214 Fiber Optic

PIN CONFIGURATION (cont.)

PIN NO.	SYMBOL	DESCRIPTION
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{2A}	Non-inverting input to amplifier A2.
14	OUT_{1A}	Non-inverting output of amplifier A1.
15	IN_{2B}	Inverting input to amplifier A2.
16	OUT_{1B}	Inverting output of amplifier A1.
17	C_{AZN}	Auto-Zero capacitor pin (Negative terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
18	C_{AZP}	Auto-Zero capacitor pin (Positive terminal). The value of this capacitor determines the low-end frequency response of the preamp A1.
19	IN_{1A}	Non-inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM

BD02882S

Postamplifier with Link Status Indicator   NE/SA5214 Fiber Optic

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	−55 to +150	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	−65 to +150	°C
P_D	Power dissipation	300	300	mW
V_{IJ}	Jam input voltage	−0.5 to 5.5	−0.5 to 5.5	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5214	SA5214	
V_{CCA}	Supply voltage	4.75 to 5.25	4.75 to 5.25	V
V_{CCD}	Power supply	4.75 to 5.25	4.75 to 5.25	V
T_A	Ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	0 to +95	−40 to +110	°C
P_D	Power dissipation	250	250	mW

DC ELECTRICAL CHARACTERISTICS
Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	36		30	37.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (+/− inputs)		3.16	3.4	3.63	3.13	3.4	3.65	V
V_{O1}	A1 output bias voltage (+/− outputs)		3.17	3.8	4.45	3.10	3.8	4.50	V
A_{V1}	A1 DC gain (without Auto-Zero)			30			30		dB
$A1_{PSRR}$	A1 PSRR (v_{CCA}, V_{CCD})	$V_{CCA} = V_{CCD} = 4.75$ to $5.25V$		60			60		dB
$A1_{CMRR}$	A1 CMRR	$\Delta V_{CM} = 200mV$		60			60		dB
V_{I2}	A2 input bias voltage (+/− inputs)		3.59	3.7	3.85	3.56	3.7	3.86	V
V_{OH}	High-level TTL output voltage	$I_{OH} = −200\mu A$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level TTL output voltage	$I_{OL} = 8mA$		0.3	0.4		0.3	0.4	V
I_{OH}	High-level TTL output current	$V_{OUT} = 2.4V$		−40	−26		−40	−24.4	mA
I_{OL}	Low-level TTL output current	$V_{OUT} = 0.4V$	8.0	30		7.0	30		mA

Postamplifier with Link Status Indicator   NE/SA5214 Fiber Optic

DC ELECTRICAL CHARACTERISTICS (Continued) Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
I_{OS}	Short-circuit TTL output current	$V_{OUT} = 0.0V$		−95			−95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	RPKDET	Pin 11 Open		0.72			0.72		V
V_{RHYST}	RHYST bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High-level jam input voltage		2.0			2.0			V
V_{ILJ}	Low-level jam input voltage				0.8			0.8	V
I_{IHJ}	High-level jam input current	$V_{IJ} = 2.7V$			20			30	μA
I_{ILJ}	Low-level jam input current	$V_{IJ} = 0.4V$	−450	−240		−485	−240		μA
V_{OHF}	High-level flag output voltage	$I_{OH} = −80\mu A$	2.4	3.8		2.4	3.8		V
V_{OLF}	Low-level flag output voltage	$I_{OL} = 3.2mA$		0.33	0.4		0.33	0.4	V
I_{OHF}	High-level flag output current	$V_{OUT} = 2.4V$		−18	−5.3		−18	−5	mA
I_{OLF}	Low-level flag output current	$V_{OUT} = 0.4V$	3.6	10		3.25	10		mA
I_{SCF}	Short-circuit flag output current	$V_{OUT} = 0.0V$	−60	−40	−25	−61	−40	−26	mA
I_{LEDH}	LED ON maximum sink current	$V_{LED} = 3.0V$	13	22	80	8	22	80	mA

AC ELECTRICAL CHARACTERISTICS Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test circuit	60	75		60	75		MHz
BW_{A1}	Small signal bandwidth (differential OUT_1/IN_1)	Test circuit		75			75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test Circuit		1.6			1.6		V_{P-P}
V_{INL}	Minimum Functional A1 input signal (single ended)	Test Circuit[1]		12			12		mV_{P-P}
R_{IN1}	Input resistance (differential at IN_1)			1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN2}	Input resistance (differential at IN_2)			1200			1200		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF

Postamplifier with Link Status Indicator NE/SA5214 Fiber Optic

AC ELECTRICAL CHARACTERISTICS (Continued) Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS						UNIT
			NE5214			SA5214			
			Min	Typ	Max	Min	Typ	Max	
R_{OUT1}	Output resistance (differential at OUT_1)			25			25		Ω
C_{OUT1}	Output capacitance (differential at OUT_1)			2			2		pF
V_{HYS}	Hysteresis voltage	Test circuit		3			3		mV_{P-P}
V_{THR}	Threshold voltage range (FLAG ON)	Test circuit, @ 50MHz $R_{RHYST}=5k$ $R_{THRESH} = 47k$		12			12		mV_{P-P}
t_{TLH}	TTL Output Rise Time 20% to 80%	Test Circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test Circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	$50mV_{P-P}$, 1010. . .input Distortion = $\left| \frac{T_H - T_L}{T_H + T_L} \right| 10^2$	2.5				2.5		%

NOTE:
1. The NE/SA5214 is capable of detecting a much lower input level. Operation under $12mV_{P-P}$ cannot be guaranteed by present day automatic testers.
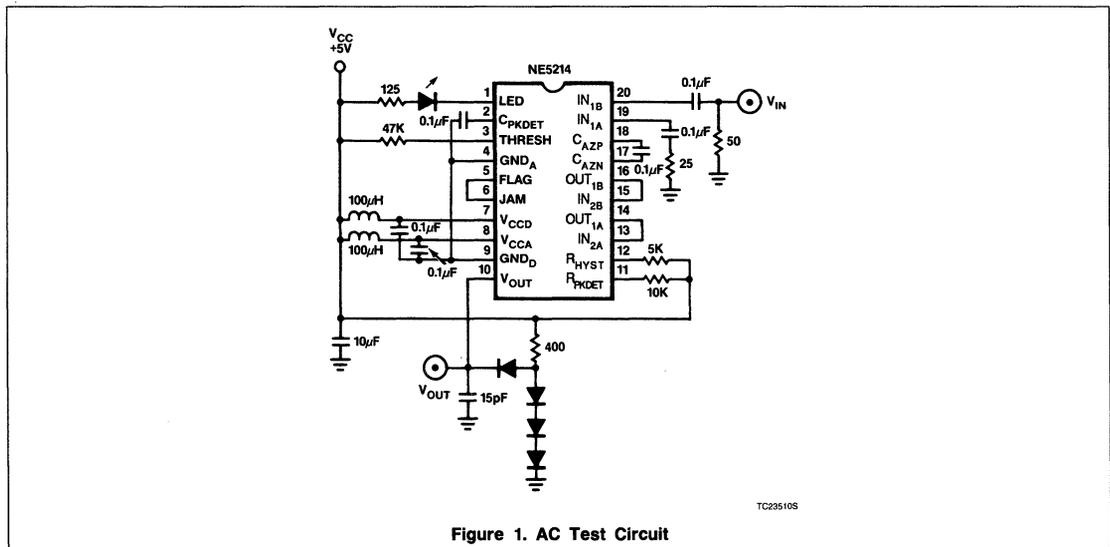
Figure 1. AC Test Circuit

Postamplifier with Link Status Indicator

NE/SA5214 Fiber Optic

TYPICAL PERFORMANCE CHARACTERISTICS

Analog Supply Current vs Temperature
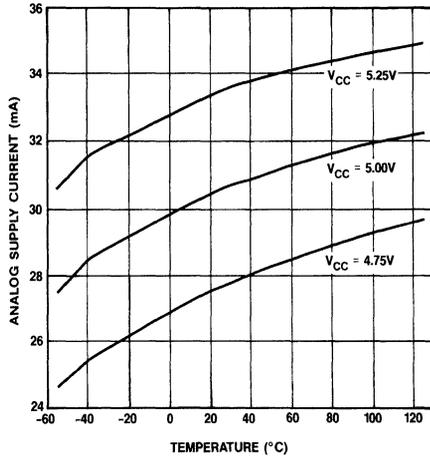
OP21040S

Digital Supply Current vs Temperature
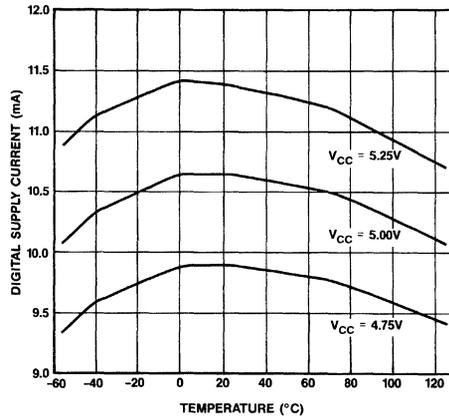
OP21030S

Threshold Voltage vs R_{THRESH}
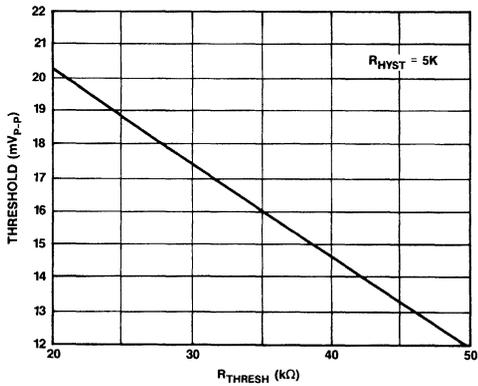
OP21010S

Hysteresis Voltage vs R_{HYST}
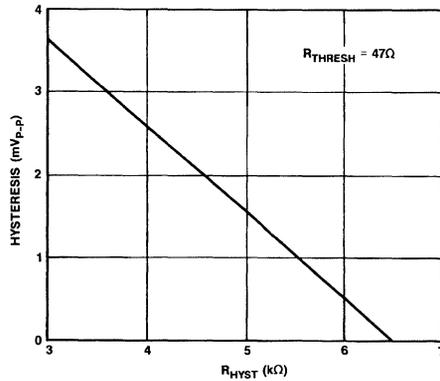
OP21020S

Postamplifier with Link Status Indicator   NE/SA5214 Fiber Optic

THEORY OF OPERATION AND APPLICATION INFORMATION

The NE 5214 postamplifier system is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

The NE5214 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3-A4-A7 path performs a wideband full-wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL HIGH on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on-chip LED driver turns the external LED to the ON state when

the input signal is above the threshold. In a typical application the "FLAG" output is tied back to the "JAM" input; this forces the TTL data OUT into a LOW state when no signal is present at the input.

An auto zero loop allows the NE5214 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212 without coupling capacitors. This auto-zero loop cancels the transimpedance amplifier's DC offset, the NE5214 A1 offset, and the data-dependent offset in the PIN diode/transimpedance amplifier combination. For more information on the NE5214 Theory of Operation, please refer to paper titled "A Low Cost 100 MBaud Fiber-Optic Receiver" by W. Mack et al.

A typical application of the NE5214 postamplifier is depicted in Figure 2. The system uses the NE5211 transimpedance amplifier which has a 28k differential transimpedance gain and a −3dB bandwidth of 140MHz. This typical application is optimized for a 50 Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.

For more information on this application, please refer to AB 1432.

NOTE:
The NE5211/NE5214 combination can operate at data rates in excess of 100Mb/s NRZ.

Figure 2. A 50Mb/s Fiber Optic Receiver

Signetics
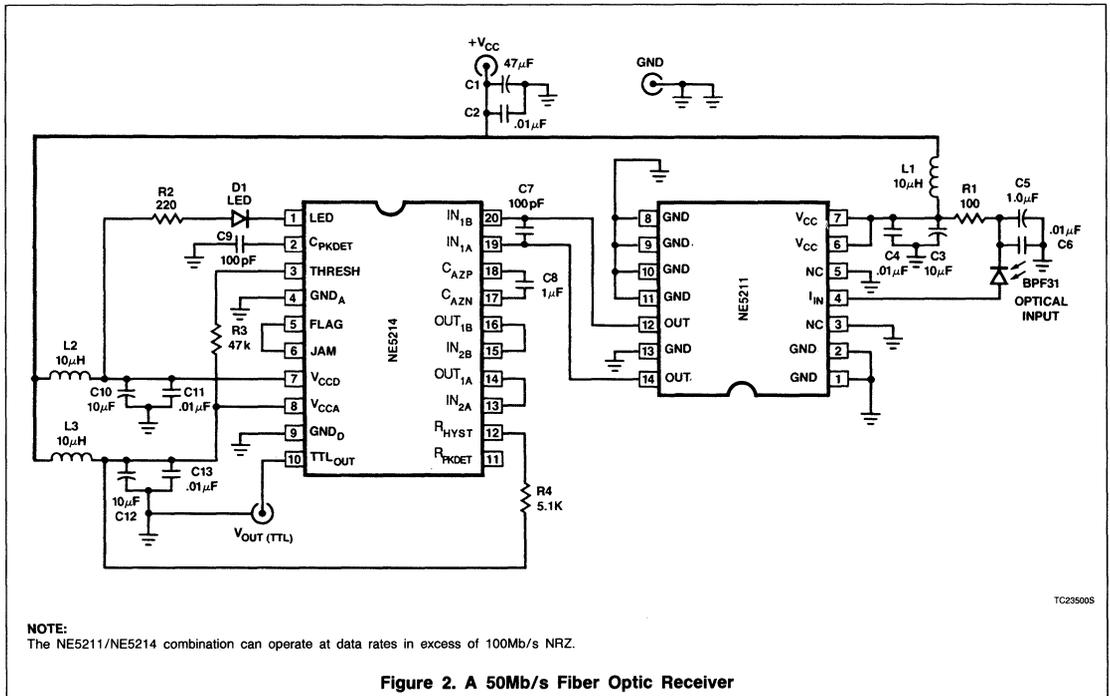
Linear Products

NE/SA5217

Postamplifier with Link Status Indicator

Preliminary Specification

DESCRIPTION

The NE/SA5217 is a 75MHz postamplifier system designed to accept low level high-speed signals. These signals are converted into a TTL level at the output. The NE5217 can be DC coupled with the previous transimpedance stage using NE5210, NE5211 or NE5212 transimpedance amplifiers. The main difference between the NE5217 and the NE5214 is that the NE5217 does not make the output of A1 and input of A2 accessible; instead, it brings out the output of A2 and the input of A8, thus activating the on-chip Schmitt trigger function by connecting two external capacitors. The result is that a much longer string of 1s and 0s, in the bit stream, can be tolerated. This "system on a chip" features an auto-zeroed first stage with noise shaping, a symmetrical limiting second stage, and a matched rise/fall time TTL output buffer. The system is user-configurable to provide adjustable input thresholds and hysteresis. The threshold capability allows the user to maximize signal-to-noise ratio, thereby insuring a Low Bit Error Rate (BER). An auto-zero loop can be used to replace two input coupling capacitors with a single auto-zero (AZ) capacitor. A signal absent flag indicates when signals are below threshold. The low signal condition forces the TTL output to the last logic state. User interaction with this "jamming" system is available. The NE/SA5217 is packaged in a standard 20-pin surface-mount package and typically consumes 40mA from a standard 5V supply. The NE/SA5217 is designed as companion to the NE/SA5211/5212 and NE5210 transimpedance amplifiers. These differential preamplifiers may be directly coupled to the postamplifier inputs. The NE5210/5217, NE/SA5211/5217,

NE/SA5212/5214 or NE/SA5212/5217 combinations convert nanoamps of photodetector current into standard digital TTL levels.

FEATURES

- **Postamp for the NE/SA5211/ 5212, NE5210 preamplifier family**
- **Wideband operation: typical 75MHz (150MBaud NRZ)**
- **Interstage filtering/equalization possible**
- **Single 5V supply**
- **Low signal flag**
- **Output disable**
- **Link status threshold and hysteresis programmable**
- **LED driver (normally On with above threshold signal)**
- **Fully differential for excellent PSRR**
- **Auto-zero loop for DC offset cancellation**
- **2kV ElectroStatic Discharge (ESD) protection**
- **Good for $2^{23}-1$ pseudo random bit stream**

APPLICATIONS

- **Fiber optics**
- **Communication links in Industrial and/or Telecom environment with high EMI/RFI**
- **Local Area Networks (LAN)**
- **Synchronous Optical Networks (SONET) STS-1**
- **RF limiter**

PIN CONFIGURATION
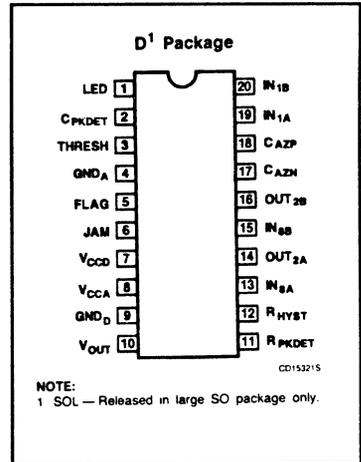
D[1] Package

LED	[1]	[20]	IN$_{1B}$
C$_{PKDET}$	[2]	[19]	IN$_{1A}$
THRESH	[3]	[18]	C$_{AZP}$
GND$_A$	[4]	[17]	C$_{AZN}$
FLAG	[5]	[16]	OUT$_{2B}$
JAM	[6]	[15]	IN$_{8B}$
V$_{CCD}$	[7]	[14]	OUT$_{2A}$
V$_{CCA}$	[8]	[13]	IN$_{8A}$
GND$_D$	[9]	[12]	R$_{HYST}$
V$_{OUT}$	[10]	[11]	R$_{PKDET}$

CD15321S

NOTE:
1 SOL — Released in large SO package only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20–Pin Plastic SOL	0 to +70°C	NE5217D
20–Pin Plastic SOL	–40 to +85°C	SA5217D

Postamplifier with Link Status Indicator   NE/SA5217

PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
1	LED	Output for the LED drive. Open–collector output transistor with 125 Ω series limiting resistor. An above threshold signal turns this transistor On.
2	C_{PKDET}	Capacitor for the peak detector. The value of this capacitor determines the detector response time to the signal, supplementing the internal 10pF capacitor.
3	THRESH	Peak detector threshold resistor. The value of this resistor determines the threshold level of the peak detector.
4	GND_A	Device analog ground pin.
5	FLAG	Peak detector digital output. When this output is Low, there is data present above the threshold. This pin is normally connected to the JAM pin and has a fanout of two.
6	JAM	Input to inhibit data flow. Sending this pin High latches TTL Data Out to the last logic state. This pin is normally connected to the FLAG pin and is TTL compatible.
7	V_{CCD}	Power supply pin for the digital portion of the chip.
8	V_{CCA}	Power supply pin for the analog portion of the chip.
9	GND_D	Device digital ground pin.
10	V_{OUT}	TTL output pin with a fanout of five.
11	R_{PKDET}	Peak detector current resistor. The value of this resistor determines the amount of discharge current available to the peak detector capacitor, C_{PKDET}.
12	R_{HYST}	Peak detector hysteresis resistor. The value of this resistor determines the amount of hysteresis in the peak detector.
13	IN_{8A}	Non–inverting input to amplifier A8.
14	OUT_{2A}	Non–inverting output of amplifier A2.
15	IN_{8B}	Inverting input to amplifier A8.
16	OUT_{2B}	Inverting output to amplifier A2.
17	C_{AZN}	Auto–Zero capacitor pin (Negative terminal). The value of this capacitor determines the low–end frequency response of the preamp A1.
18	C_{AZP}	Auto–Zero capacitor pin (Positive terminal). The value of this capacitor determines the low–end frequency response of the preamp A1.
19	IN_{1A}	Non–inverting input of the preamp A1.
20	IN_{1B}	Inverting input of the preamp A1.

BLOCK DIAGRAM

Postamplifier with Link Status Indicator

NE/SA5217

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING		UNIT
		NE5217	SA5217	
V_{CCA}	Power supply	+6	+6	V
V_{CCD}	Power supply	+6	+6	V
T_A	Operating ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	−55 to +150	−55 to +150	°C
T_{STG}	Storage temperature range	−65 to +150	−65 to +150	°C
P_D	Power dissipation	1.4	1.4	W
V_{IJ}	Jam input voltage	−0.5 to 5.5	−0.5 to 5.5	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING		UNIT
		NE5217	SA5217	
V_{CCA}	Power supply	4.5 to 5.5	4.5 to 5.5	V
V_{CCD}	Power supply	4.5 to 5.5	4.5 to 5.5	V
T_A	Operating ambient temperature range	0 to +70	−40 to +85	°C
T_J	Operating junction temperature range	0 to +95	−40 to +110	°C
P_D	Power dissipation	300	300	mW

DC ELECTRICAL CHARACTERISTICS
Min and Max limits apply over the operating temperature range at $V_{CCA} = V_{CCD} = +5.0V$ unless otherwise specified. Typical data applies at $V_{CCA} = V_{CCD} = +5.0V$ and $T_A = 25°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5217			SA5217			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{CCA}	Analog supply current			30	36		30	37.2	mA
I_{CCD}	Digital supply current (TTL, Flag, LED)			10	13.3		10	13.5	mA
V_{I1}	A1 input bias voltage (A, B inputs)		3.16	3.4	3.63	3.13	3.4	3.65	V
V_{O2}	A2 output bias voltage (A, B outputs)		3.14	3.80	4.42	3.07	3.80	4.47	V
V_{I8L}	A8 input bias voltage Low (A, B inputs)		3.40	3.55	3.68	3.40	3.55	3.68	V
V_{I8H}	A8 input bias voltage High (A. B inputs)		3.70	3.91	4.10	3.68	3.91	4.12	V
V_{OH}	High–level TTL output voltage	$I_{OH} = -200\mu A$	2.4	3.4		2.4	3.4		V
V_{OL}	Low–level TTL output voltage	$I_{OL} = 8mA$		0.3	0.4		0.3	0.4	V
I_{OH}	High–level TTL output current	$V_{OUT} = 2.4V$		−40	−26.4		−40	−24.4	μA
I_{OL}	Low–level TTL output current	$V_{OUT} = 0.4V$	8.0	30		7.0	30		mA
I_{OS}	Short circuit TTL output current	$V_{OUT} = 0.0V$		−95			−95		mA
V_{THRESH}	Threshold bias voltage	Pin 3 Open		0.75			0.75		V
V_{RPKDET}	Peak detector bias voltage	Pin 11 Open		0.72			0.72		V
V_{RHYST}	Hysteresis resistor bias voltage	Pin 12 Open		0.72			0.72		V
V_{IHJ}	High–level jam input voltage		2.0			2.0			V
V_{ILJ}	Low–level jam input voltage				0.8			0.8	V
I_{IHJ}	High–level jam input current	$V_{IJ} = 2.7V$			20			30	μA
I_{ILJ}	Low–level jam input current	$V_{IJ} = 0.4V$	−450	−240		−485	−240		μA
V_{OHF}	High–level flag output voltage	$I_{OH} = -80\mu A$	2.4	3.8		2.4	3.8		V
V_{OLF}	Low–level flag output voltage	$I_{OL} = 3.2mA$		0.33	0.4		0.33	0.4	V

Postamplifier with Link Status Indicator

NE/SA5217

DC ELECTRICAL CHARACTERISTICS (Continued) Min and Max limits apply over the operating temperature range at V_{CCA} = V_{CCD} = +5.0 unless otherwise specified. Typical data applies at V_{CCA} = V_{CCD} = +5.0V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5217			SA5217			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{OHF}	High–level flag output current	V_{OUT} = 2.4V		–18	–5.3		–18	–5	mA
I_{OLF}	Low–level flag output current	V_{OUT} = 0.4V	3.6	10		3.25	10		mA
I_{SCF}	Short–circuit flag output current	V_{OUT} = 0.0V	–60	–40	–25	–61	–40	–26	mA
I_{LEDH}	LED On maximum sink current	V_{LED} = 3.0V		22	80		22	80	mA

AC ELECTRICAL CHARACTERISTICS Min and Max limits apply over the operating temperature range at V_{CCA} = V_{CCD} = +5.0V unless otherwise specified. Typical data applies at V_{CCA} = V_{CCD} = +5.0V and T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	NE5217			SA5217			UNIT
			Min	Typ	Max	Min	Typ	Max	
f_{OP}	Maximum operating frequency	Test circuit	60	75		60	75		MHz
V_{INH}	Maximum Functional A1 input signal (single ended)	Test circuit		1.6			1.6		$V_{P–P}$
V_{INL}	Minimum Functional A1 input signal (single ended)	Test circuit		6			6		$mV_{P–P}$
	Minimum Functional A1 input signal (differential)			3			3		$mV_{P–P}$
	Minimum input sensitivity for output BER $\leq$ 10^{-9} (single ended)	PRBS = $2^{23}-1$		9			9		$mV_{P–P}$
	Minimum input sensitivity for output BER $\leq$ 10^{-9} (differential)			4.5			4.5		$mV_{P–P}$
R_{IN1}	Input resistance (differential at IN_1)			1200			1200		Ω
C_{IN1}	Input capacitance (differential at IN_1)			2			2		pF
R_{IN8}	Input resistance (differential at IN_8)			2000			2000		Ω
C_{IN2}	Input capacitance (differential at IN_2)			2			2		pF
R_{OUT2}	Output resistance (differential at OUT_2)			25			25		Ω
C_{OUT2}	Output capacitance (differential at OUT_2)			2			2		pF
V_{HYS}	Hysteresis voltage range (single ended)	Test circuit, T_A = 25°C		10			10		$mV_{P–P}$
	Hysteresis voltage range (differential)	R_{HYST} = 4K R_{THRESH} = 33K		5			5		$mV_{P–P}$
V_{THR}	Threshold voltage (single ended)	(FLAG Low) Test circuit, @ 50MHz		19			19		$mV_{P–P}$
	Threshold voltage (differential)	R_{RHYST} = 4K R_{THRESH} = 33K		9.5			9.5		$mV_{P–P}$
t_{TLH}	TTL Output Rise Time 20% to 80%	Test circuit		1.3			1.3		ns
t_{THL}	TTL Output Fall Time 80% to 20%	Test circuit		1.2			1.2		ns
t_{RFD}	t_{TLH}/t_{THL} mismatch			0.1			0.1		ns
t_{PWD}	Pulse width distortion of output	50m$V_{P–P}$, 1010. . .input Distortion = $\dfrac{T_H - T_L}{T_H + T_L} 10^2$		TBD			TBD		%

Postamplifier with Link Status Indicator
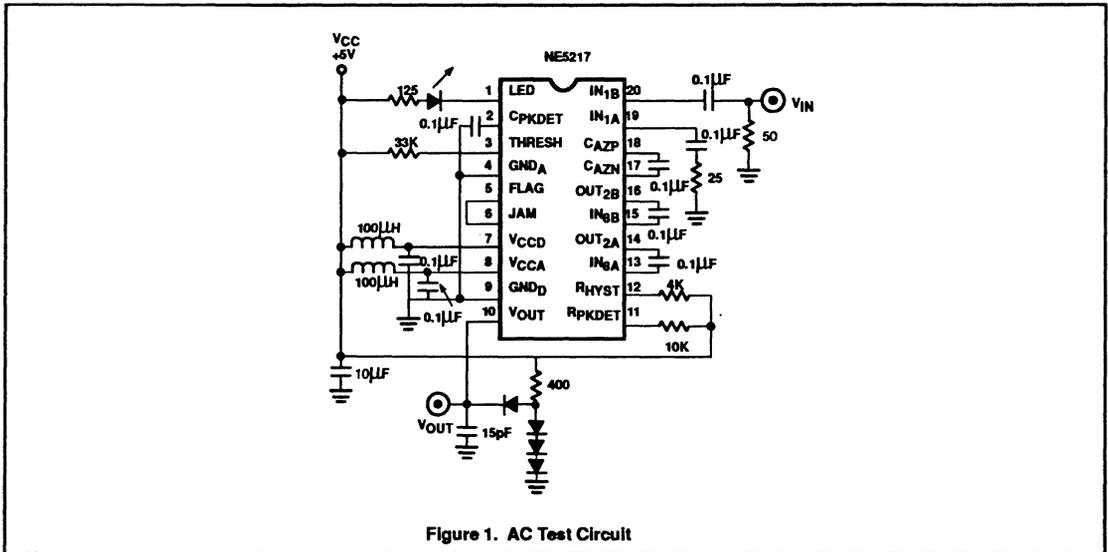
NE/SA5217

Figure 1. AC Test Circuit

TYPICAL PERFORMANCE CHARACTERISTICS
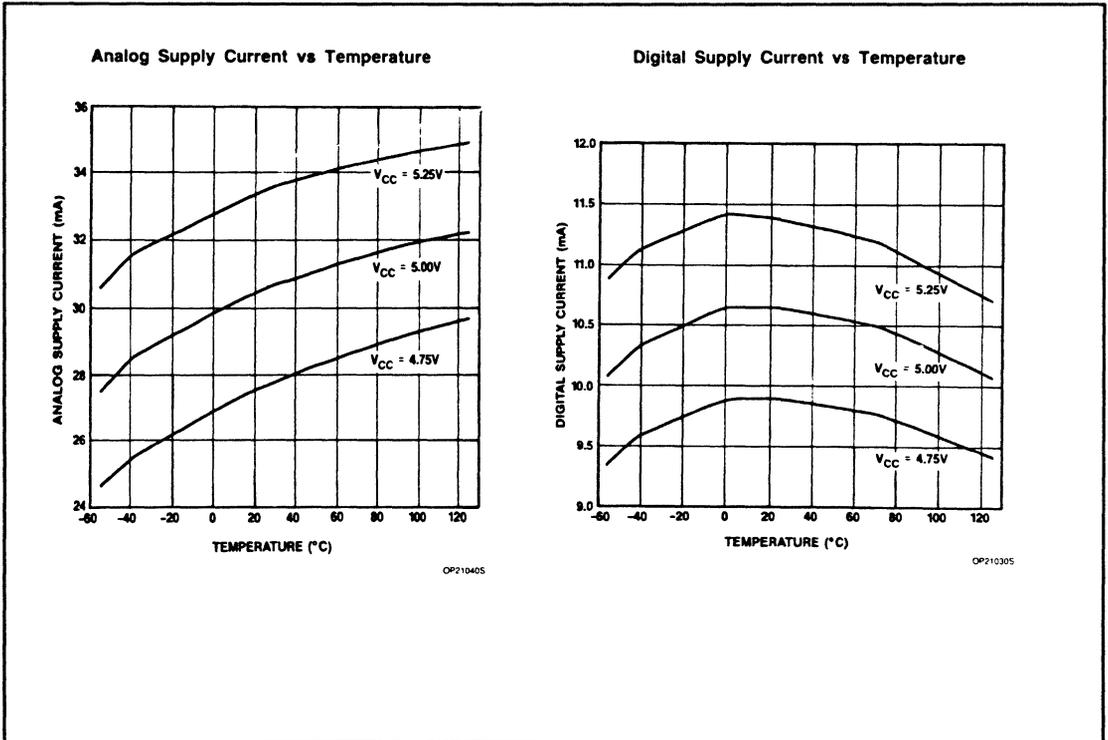
Postamplifier with Link Status Indicator

NE/SA5217

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Threshold vs R_{THRESH} for Different Values of R_{HYST} (Driven Single Ended)

$V_{CC} = 5V$
$T_A = 27°C$
F = 60MHz

THRESHOLD (mV_{P-P})

2k
3k
4k
5k
6k

R_{THRESH} (kΩ)

On/Off Voltage vs R_{THRESH} (Driven Single Ended)

$V_{CC} = 5V$
$T_A = 27°C$
F = 60MHz
$R_{HYST} = 4k$

V_{IN} (mV_{P-P})

ON
OFF

R_{THRESH} (kΩ)

Postamplifier with Link Status Indicator

NE/SA5217

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Hysteresis vs R_{THRESH} for Different Values of R_{HYST} (Driven Single Ended)

Hysteresis and Forward Active Region
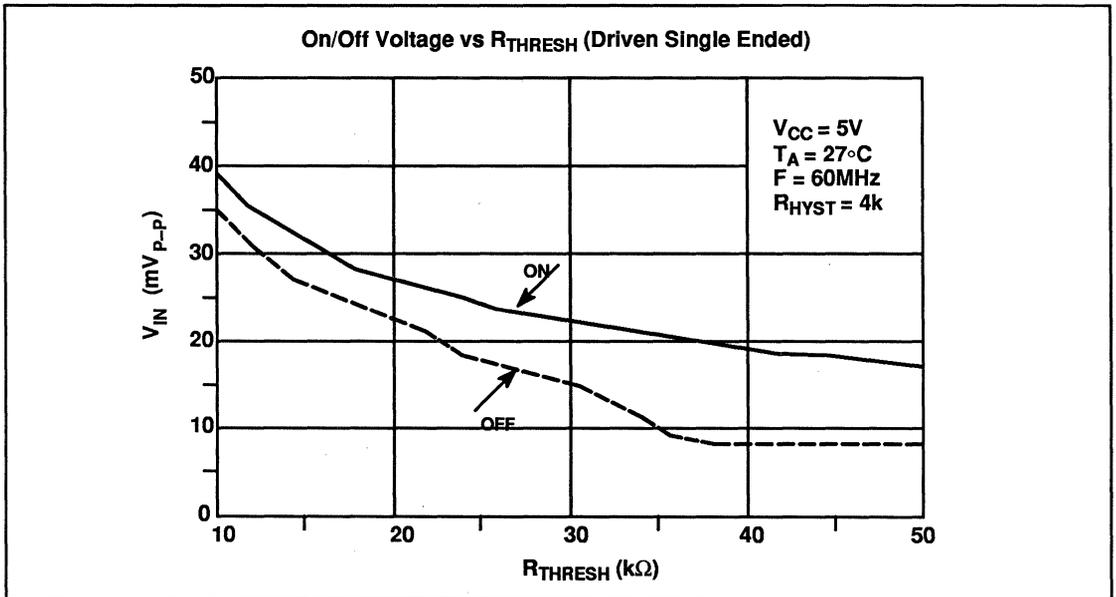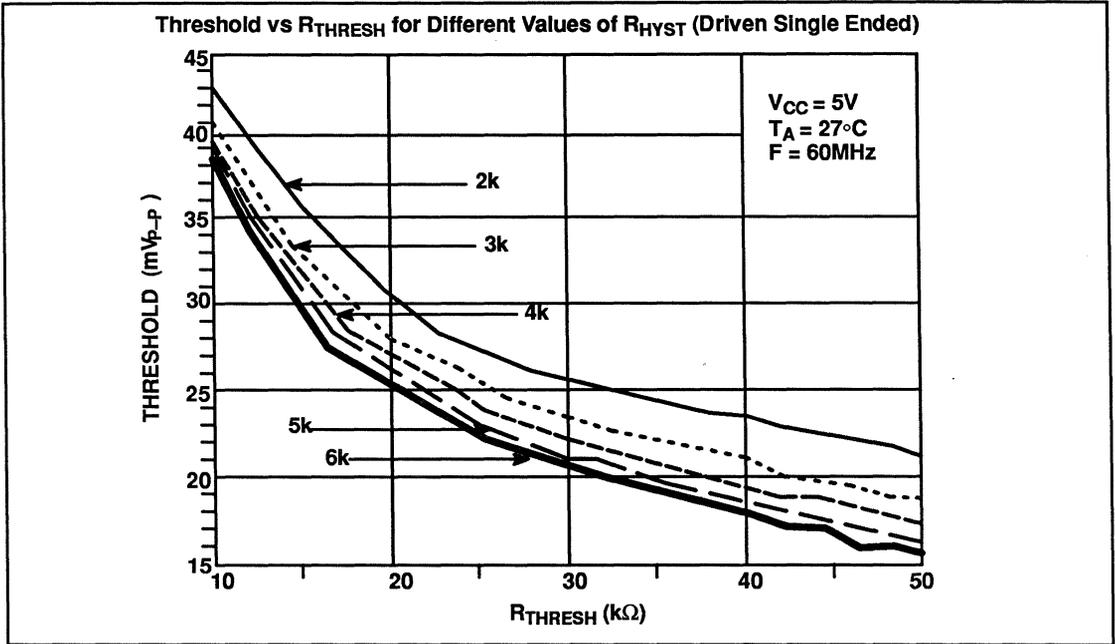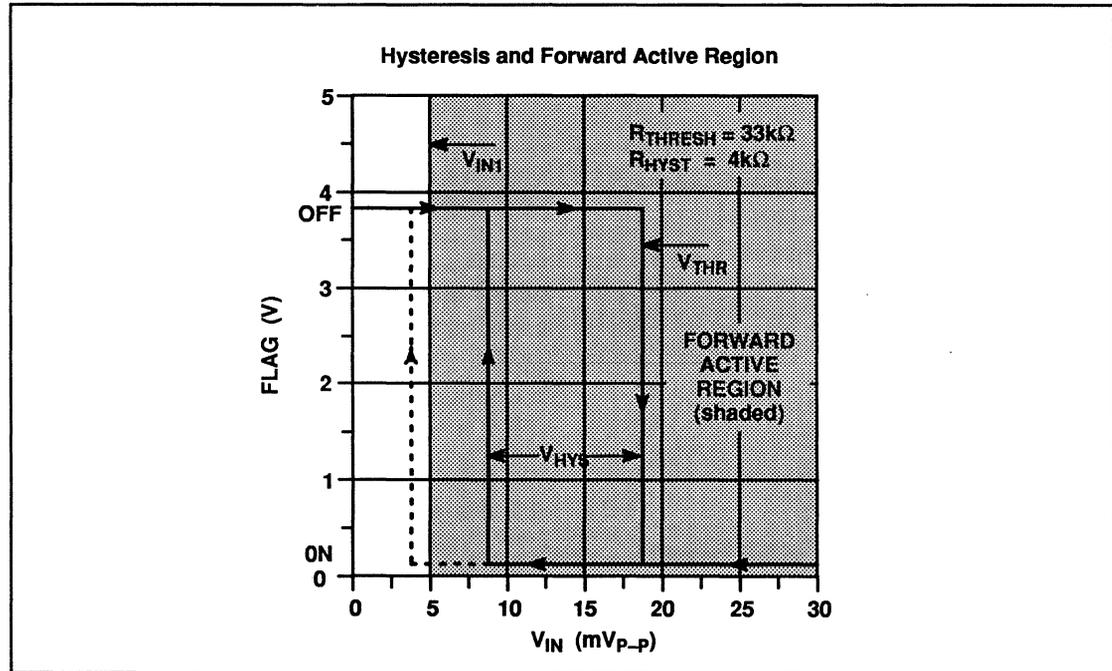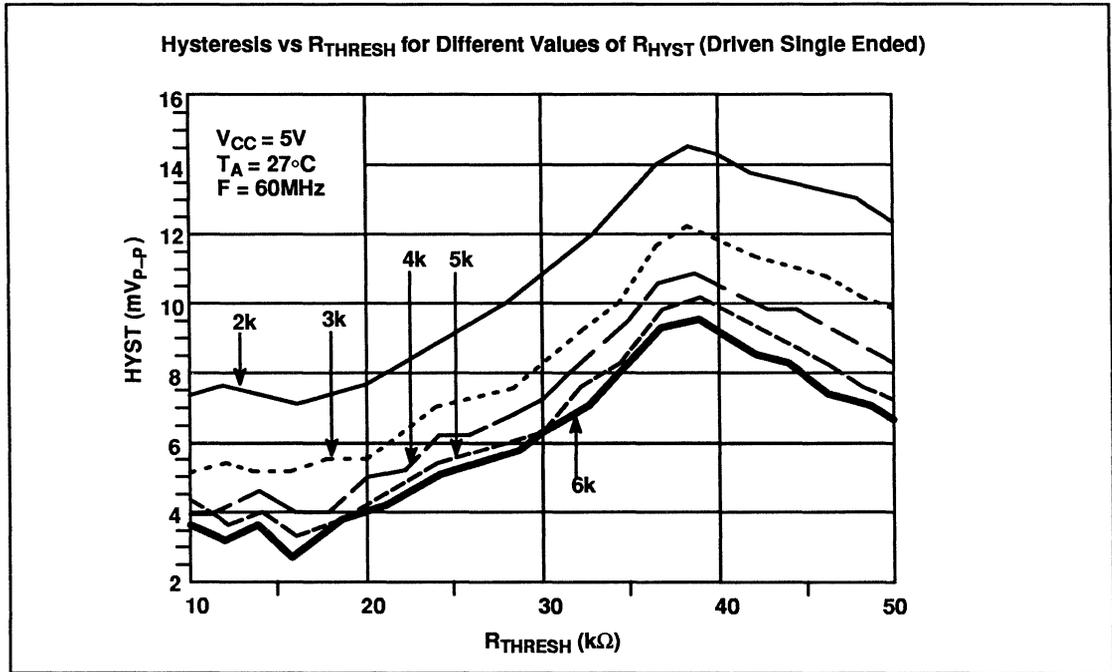
Postamplifier with Link Status Indicator

NE/SA5217

THEORY OF OPERATION AND APPLICATION

The NE5217 postamplifier is a highly integrated chip that provides up to 60dB of gain at 60MHz, to bring mV level signals up to TTL levels.

The NE5217 contains eight amplifier blocks (see Block Diagram). The main signal path is made up of a cascade of limiting stages: A1, A2 and A8. The A3–A4–A7 path performs a wideband full–wave rectification of the input signal with adjustable hysteresis and decay times. It outputs a TTL High on the "FLAG" output (Pin 5) when the input is below a user adjustable threshold. An on–chip LED driver turns the external LED to the On state when the input signal is above the threshold. In a typical application the "FLAG" output is tied back to the "JAM" input; forcing the "JAM" input to TTL High will latch the TTL Data Out at the last logical state.

Threshold voltage and hysteresis voltage range are adjustable with resistors R_{THRESH} and R_{HYST}. The typical values given in the data sheet will result in performance shown in the graph "Hysteresis and Forward Active Region". A minority of parts may be sensitive enough that FLAG High (Off) occurs below the minimum functional input signal level, V_{IN1}. This condition is shown by the dotted line in the graph. Such parts may require adjustment of R_{THRESH} if it is important to guarantee that an output signal is present for the full hysteresis range. If this is not important, R_{THRESH} may be adjusted to give a FLAG Low for lower level input signals.

An auto–zero loop allows the NE5217 to be directly connected to a transimpedance amplifier such as the NE5210, NE5211, or NE5212 without coupling capacitors. This auto–zero loop cancels the transimpedance amplifier's DC offset, the NE5217 A1 offset,

and the data–dependent offset in the PIN diode/transimpedance amplifier combination. For more information on the NE5217 Theory of Operation, please refer to paper titled "A Low Cost 100MBaud Fiber Optic Receiver" by W. Mack, et. al.

A typical application of the NE5217 postamplifier is depicted in Figure 2. The system uses the NE5210 transimpedance amplifier which has a 28k differential transimpedance gain and a –3dB bandwidth of 140MHz. this typical application is optimized for a 50Mb/s Non Return to Zero (NRZ) bit stream.

As the system's gain bandwidth product is very high, it is crucial to employ good RF design and printed circuit board layout techniques to prevent the system from becoming unstable.

For more information on this application, please refer to Application Brief AB1432.

NOTE:
THE NE5210/NE5217 combination can operate at data rates in excess of 100Mb/s NRZ

Figure 2. A 50Mb/s Fiber Optic Receiver

Signetics

Linear Products
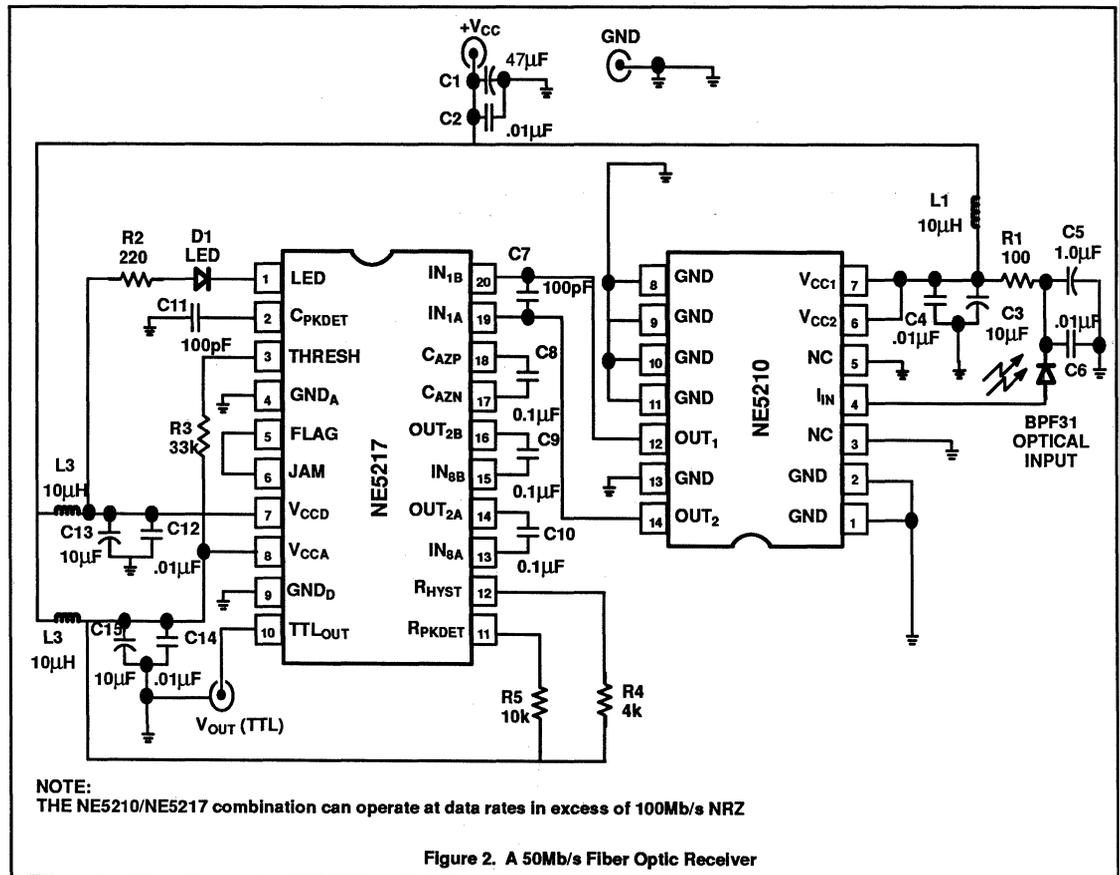
Section 4
Fiber Optic Receiver, Clock Recovery

INDEX

Signetics

AN1883
100Mb/s Clock Recovery and Data Retiming Using the NE568

Linear Products

Application Note

Author: M. Kolluri

INTRODUCTION

The increased volume of information flow in today's systems requires the use of high speed data communication networks. The wide bandwidth and low attenuation characteristic of optical fibers has made it the media of choice at these high data rates.

In a typical fiber optic receiver, the received optical signal is first converted to an electrical signal by an optical detector such as a PIN diode. The electrical signal from the PIN diode is amplified to provide ECL level data output.

The received ECL level data output is likely to have a significant amount of phase jitter due to noise and other system imperfections. Since a separate clock signal is not transmitted, it has to be derived from the received data stream, which is then used to sample and retime the data to present a low-jitter recovered data output. The received ECL level data stream is then applied to a clock recovery and data retiming system, which will be described below, to provide a complete fiber optic receiver system.

A typical fiber optic receiver system is shown in Figure 1.

CLOCK RECOVERY AND DATA RETIMING

Optimum detection of a digital data stream requires a local clock which is in close phase agreement with the received pulse train. Unipolar nonreturn-to-zero (NRZ) signals are widely used in digital data transmission. The transmitted signal is a random pulse train having regularly spaced pulse positions which are filled, or not, at random as shown in Figure 2. The spectrum of a random NRZ signal has a spectral null at the bit frequency.

Figure 2. NRZ Pulse Train

DATA 1 0 0 1 1 1 0 1 1 0 1 1 0 0

Bit Frequency $f_B = \frac{1}{T}$

However, it is possible to generate the required spectral component at the bit frequency from the incoming data stream since the information exists in the locations in time of the data transitions. The incoming data stream is first applied to a transition detector circuit to generate "transition pulses". The original message sequence is transformed by this circuit into a new sequence in which a pulse is associated with each "0-1" or "1-0" transition of the original message.

Random data with a mean transition density of 50% will produce a strong spectral component at the bit frequency.

A phase-locked loop (PLL) is used to lock onto the spectral component at the bit frequency in the transition pulses to generate the required clock signal. Long strings of zeros and ones can be tolerated since the PLL can lock onto a small spectral component at the bit frequency. The system to be described below can capture and maintain lock with a pseudo-random sequence of $(2^{23} - 1)$.

NE568-BASED SYSTEM

Figure 3 is a simplified block diagram of a 100Mb/s clock recovery and data retiming system that was implemented
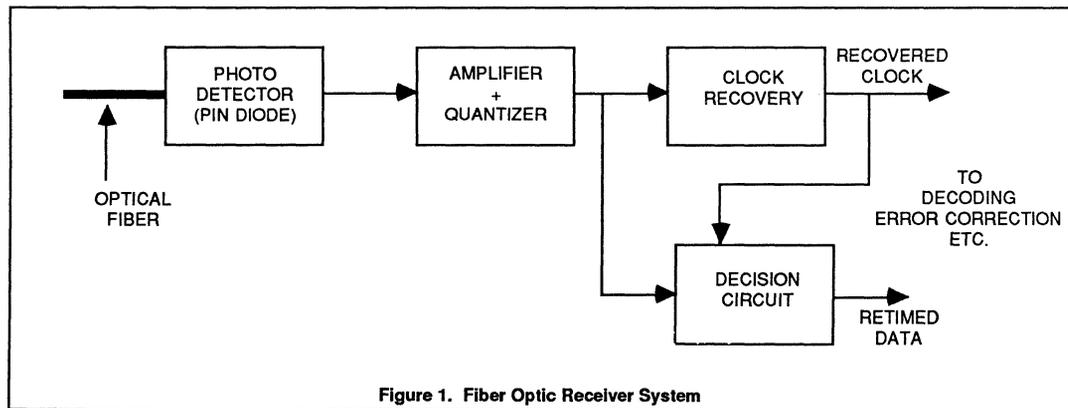
Figure 1. Fiber Optic Receiver System

100Mb/s Clock Recovery and Data Retiming Using the NE568 AN1883
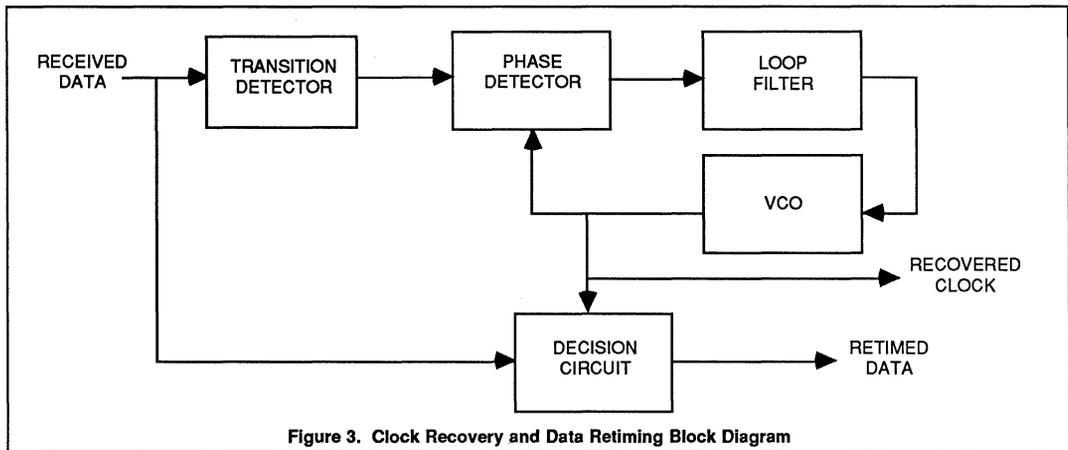
Figure 3. Clock Recovery and Data Retiming Block Diagram

using the VCO of the NE568.

The transition detector, phase comparator, and the decision circuit for retiming the data were implemented using standard ECL 10K and 100K components. This implementation is powered by a single -5.2V supply and the inputs and outputs are ECL compatible. The func-

tional blocks used in this circuit are described below.

Transition Detector

The transition pulses are obtained by a logical operation of the received signal and the received signal with delay. The implementation is shown in Figure 4a. The incoming signal is delayed by E1

and E2 and is one of the inputs to E3; the other input to E3 is the incoming signal. The output of E3 is a transition pulse for each "0-1" or "1-0" transition of the received signal. The width of the transition pulse is determined by the delay through E1 and E2. The waveforms shown in Figure 4b illustrate this process.
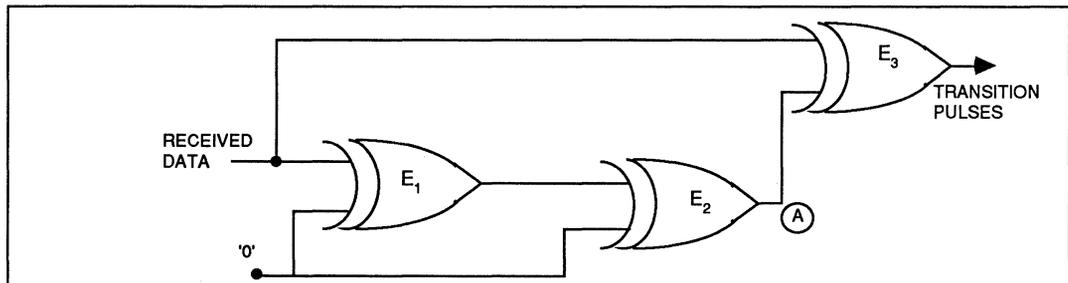
Figure 4a. Transition Detector
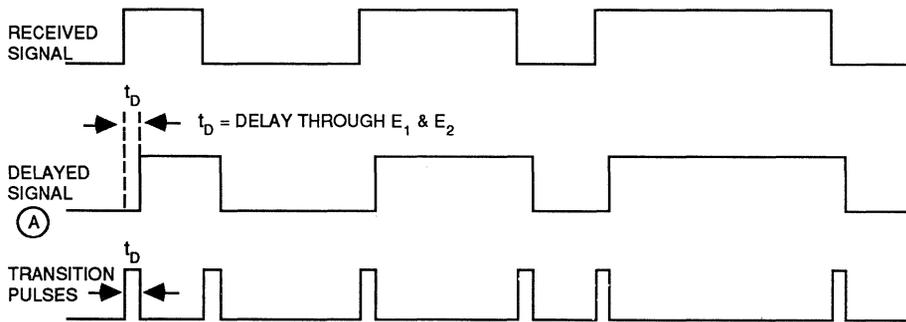
Figure 4b. Transition Detector Waveforms

100Mb/s Clock Recovery and Data Retiming Using the NE568   AN1883

CLK

PUMP
DOWN

CLK

PUMP
UP

TRANSITION
PULSE
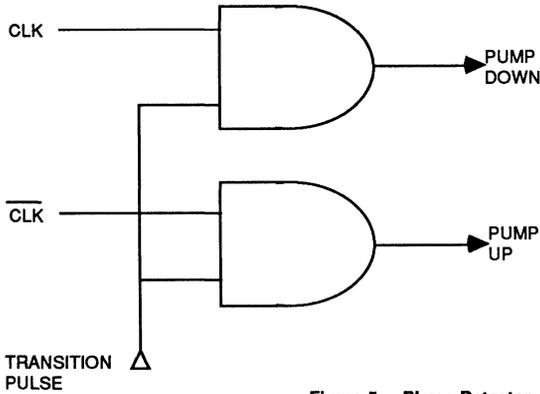
Figure 5a. Phase Detector

CLK

CLK

TRANSITION
PULSE

PUMP
DOWN

PUMP
UP
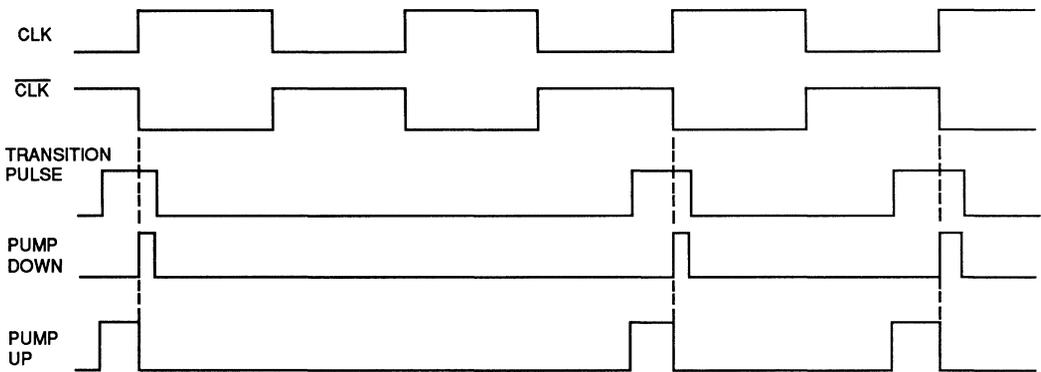
Figure 5b. Phase Detector Waveforms; VCO Too Slow

CLK

CLK

TRANSITION
PULSE

PUMP
DOWN

PUMP
UP
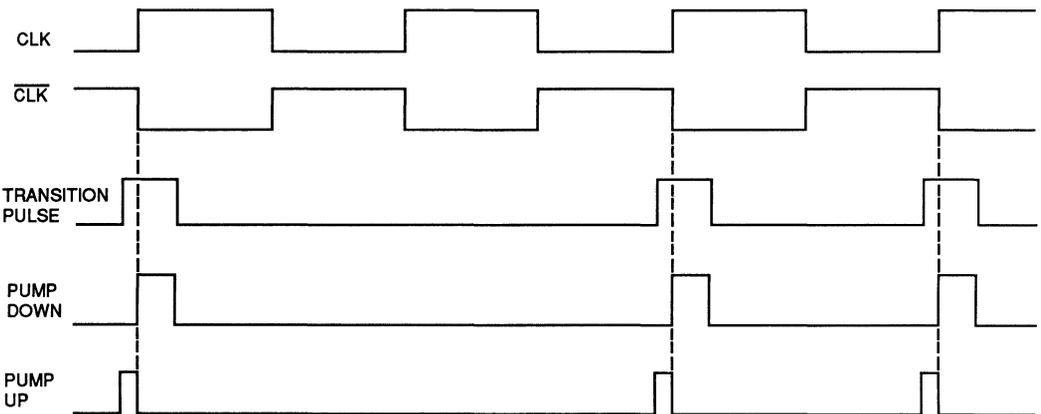
Figure 5c. Phase Detector Waveforms; VCO Too Fast

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Phase Detector

The phase detector in the NE568 is a double-balanced modulator. If this phase detector were used in clock recovery applications with potentially long strings of zeros and ones, the phase detector output would be a replica of the clock waveform in the absence of data transitions. Any asymmetry in it can result in a DC offset when there are no data transitions. In order to avoid these problems with the internal phase detector, an external phase detector was implemented using ECL gates as shown in Figure 5a. The difference in the width of the "Pump-Up" and "Pump-Down" signals is proportional to the phase difference between the transition pulses and the VCO (see Figures 5b & 5c). In the absence of transition pulses, both the "Pump-Up" and "Pump-Down" signals are low, thus making the system insensitive to clock asymmetry.

Loop Filter and Amplifier

In clock recovery applications the PLL acts as a narrowband filter centered at the bit frequency. In a typical digital transmission system, the transition points are displaced from their ideal positions by a random amount due to noise and other system imperfections. The spectral component of this jitter, which is within the bandwidth of the PLL, will contribute to jitter in the recovered clock. While reducing the bandwidth of the PLL is essential to minimizing the jitter, a compromise must be made so that it is wide enough to allow capture

and maintain lock. This implementation allows a capture range of ±4% which allows for the temperature drift in the VCO. The output amplifier of the NE568 is used to implement an active filter in this application.

Voltage Controlled Oscillator (NE568)

The NE568 is used as a VCO in this implementation. A block diagram of the NE568 is shown in Figure 6. The oscillator is a current-controlled multivibrator in which the current control affects the charge/discharge rate of the timing capacitor. The control signal voltage from the phase comparator and loop filter is conditioned by a V/I converter in the NE568 to produce a linear change in frequency over a large control voltage range. The free-running frequency of the oscillator depends on the value of the timing capacitor between Pins 4 and 5. The value of the timing capacitor depends on internal resistive components and current sources. When $R7=2.5k\Omega$ and $R11=2.5k\Omega$, a close approximation of the correct capacitor value for a free-running frequency of f_o is $C_T = (0.0034/f_o)$ Farads. A more detailed description of the NE568 is included in the product data sheet.

Decision Circuit

In a typical receiver there is likely to be a significant amount of phase jitter on the received data stream, as was discussed earlier. The narrowband filtering

action of the PLL provides a recovered clock with substantially lowered jitter. By sampling the jittered data stream at the center of the eye opening, the jitter on the retimed data is reduced to be nearly the same as that of the recovered clock. The decision circuit is a D-type flip-flop, which is latched by the recovered clock. The output of the flip-flop is the retimed data which is synchronous with the recovered clock.

SYSTEM DESCRIPTION

Figure 7 is the complete schematic of the 100Mb/s clock recovery and data retiming system implementation.

In order to achieve optimum performance, careful attention is required in the layout. The regulated V_{EE} power supply (-5.2V) and the termination voltage V_T (-2.0V) should have adequate bypassing. Surface mount capacitors and resistors are highly recommended as a starting point. The layout should have good ground planes and short interconnecting traces.

Circuit Adjustments

The free-running frequency of the VCO is set by choosing the appropriate timing capacitor ($C_T = 34.2pF$ for 100MHz). The free-running frequency can be adjusted to exactly match the incoming bit frequency by adjusting FREQ. ADJ. trim pot with no signal input. The duty cycle of the clock can be adjusted by the DUTY CYCLE ADJ. trim pot to obtain a


Figure 6. NE568 Block Diagram

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V_{EE} (-VE POWER SUPPLY) = -5.2V R_T (TERMINATION RESISTORS) = 51Ω
V_T (TERMINATION VOLTAGE) = -2V   R1, R2, R3, R4 = 1.32kΩ
C1, C2 = 100pF   R5, R6 = 511Ω
C3, C4 = 2.4µF   R7 = 5kΩ
C5 = 100pF   R8 = 1kΩ
C_T = 34.2pF   R9, R10 = 820Ω
C_B (BYPASS) = 0.1µF   R11 = 2.5kΩ
C_{AC} (COUPLING) = 0.1µF

Figure 7. 100Mb/s Clock Recovery and Data Retiming System

symmetric clock waveform.

The lag-lead filter network (R1-R6 and C1-C4) determines the loop bandwidth of the PLL. The values used are to attain a capture range of ±4MHz.

Minor adjustments to the capture range and the loop bandwith can be achieved by changing C3 and C4.

Measured Performance
The performance of the system was tested with an ECL level, 100Mb/s, (2^{23} - 1) pseudo-random sequence, NRZ signal, with the free-running frequency of the VCO adjusted to 100MHz. The bit

pattern was 7.2×10^{11} bits in length. The peak-to-peak jitter on the recovered clock was 1.0ns as shown in Figure 8. The offset of the recovered clock from the ideal sampling point, which is the center of the eye opening, was only 0.2ns as shown in Figure 9. In order to verify the system operation with an offset between the bit frequency and the VCO free-running, as would be expected due to the variation of the VCO with temperature and other effects, the bit frequency was changed to 103Mb/s. With a frequency thus offset by 3% the peak-to-peak jitter increased only slightly to 1.2ns as shown in Figure 10.

The delay of the retimed data to the recovered clock was 2.2ns (see Figure 11), which is primarily the delay through the decision flip-flop.

Operation at Other Bit Frequencies
The circuit was built and tested to perform the clock recovery and data retiming function for a 100Mb/s system. The same circuit could easily be modified for use at other data rates by replacing the timing capacitor for the appropriate VCO free-running frequency and will achieve similar performance. The above implementation was also tested at 50Mb/s and yielded similar results. At speeds of

100Mb/s Clock Recovery and Data Retiming Using the NE568   AN1883

100Mb/s, the use of ECL logic is highly desirable especially in the phase detector which requires that the CLK and CLK signals have minimal skew. Implementation of this circuit in a TTL environment, though, requires that significant attention be paid to matching the skews, propagation delays and rise times in the signal path, especially for CLK and CLK signals.

A COMPLETE FIBER OPTIC RECEIVER

Figure 12 is a suggested implementation of a complete fiber optic receiver using the clock recovery and data retiming circuit, described above, and other receiver components that were specifically designed for fiber optic data communication links. The received optical signal is first converted to an electrical one by an optical detector such as a PIN diode. A transimpedance amplifier, such as the NE5211, converts the single-ended current output of the PIN diode into a differential voltage output suitable for further processing. The NE5211 outputs are fed to a high-gain limiting amplifier such as the NE5214 to provide TTL level logic outputs.

The TTL logic outputs can then be applied through a TTL-ECL level translator to the clock recovery and data retiming system, described above, to provide a complete fiber optic receiver system.

NOTE: Skew Between Transmit and Receive Clocks
       is Due to Unequal Cable Length.

**Figure 8. Jitter in the Recovered Clock (Bottom Trace).
Transmit Clock (Top Trace).**

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Figure 9. Recovered Clock Alignment Offset (Bottom Trace).
100Mb/s, $(2^{23}-1)$ Pseudo-Random Sequence. Received Data (Top Trace).

Figure 10. Jitter In Recovered Clock (Bottom Trace) with 3% Frequency Offset.

100Mb/s Clock Recovery and Data Retiming Using the NE568   AN1883

Figure 11. Recovered Clock (Top Trace)
Retimed Data (Bottom Trace)

Figure 12. Complete Fiber Optic Receiver System
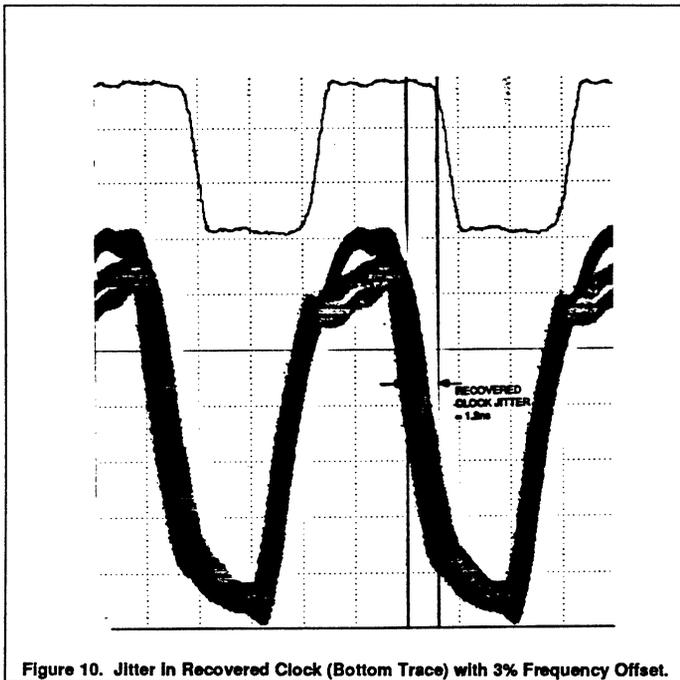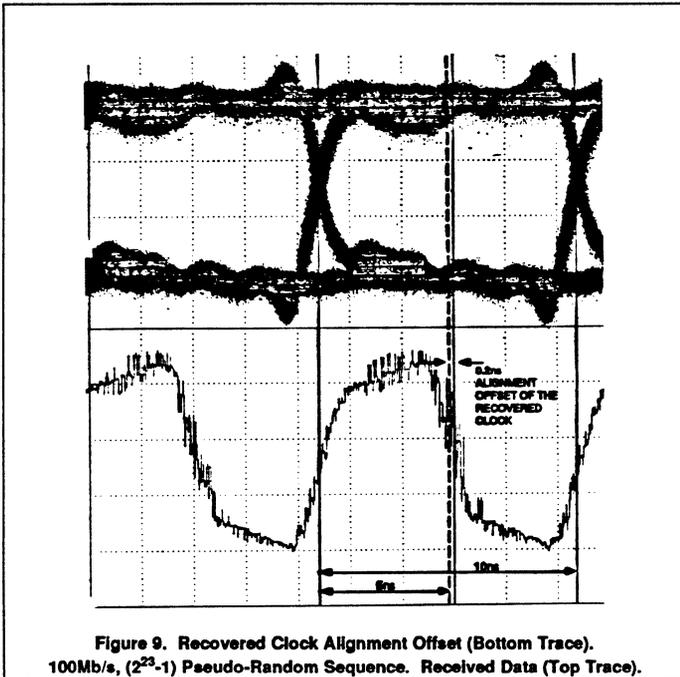
Linear Products

Author: Les Hadley

INTRODUCTION
In order to obtain a local clock signal in Multiplexed Data Transmission systems, a phase and frequency coherent method of signal extraction is required. A Master-Slave system using the quartz crystal as the primary frequency determining element in a phase-lock loop VCO is used to reproduce a phase coherent clock from an asynchronous Data Stream.

The NE564, a versatile phase-locked loop (PLL) operating at frequencies to 50MHz, has inputs and outputs designed to be TTL compatible. The Signetics NE564 is used to generate the phase-locked, crystal-stabilized clock reference signal.

Its particular adaptation, for use with a crystal-controlled VCO instead of the usual RC control elements, requires a brief review of the principles of the Phase-Lock Loop design.

The NE564 Phase-Locked Loop is a fully contained system, including limiter, phase detector, VCO, DC amplifiers, DC retriever and output comparator (reference Figure 1). For the clock regeneration system to be discussed, the portions of the NE564 implemented are the input limiter, phase detector and VCO.

The signal limiter amplifies low level inputs (until saturation is reached, which is typically 60mV$_{P-P}$ for the NE564). The signal limiter output is fed to the phase detector, where the "unknown" input is compared to the "known" VCO frequency of the NE564. The differential error signal that is generated is fed through a DC amplifier and a voltage-to-current converter. The change in the current generated forces the VCO frequency to vary in its frequency and/or phase relationship, such that a θ of 90° lagging is obtained (the actual phase relationship may be somewhat less than 90° depending upon the $K_d K_o$ (gain) product of the NE564 at the operating frequency and bias current). The external filtering incorporated at Pins 4 and 5 control the dynamic frequency response and loop stability criteria.

The NE564 is a first order system; therefore, the use of single capacitors (at Pins 4 and 5) will automatically create a "second-order" system. An RC series filter combination will cause a lead-lag condition that will permit dynamic selectivity, along with closed-loop stability.

LOOP GAIN FUNCTIONS
The phase detector conversion gain (K_d) and the VCO conversion gain (K_o) determine, in large part, the lock range, capture range and linearity characteristics of the NE564. These device parameters are both dependent upon bias current and operating frequency. Some typical curves for each of the parameters are shown for the NE564 in Figures 2 and 3.

THE CLOCK REGENERATOR CIRCUIT
The basic building blocks of the clock regenerator circuit are shown in Figure 4. The PLL is shown as a frequency multiplier incorporating a divide by "N" in the VCO phase detector feedback loop. The functions of the ringing circuit and the NE527 high-speed comparator will be discussed later.

The waveforms of Figure 5 indicate the waveforms transmitted over a T1 line. The bipolar signal transmitted has "no" DC components induced in the transmission line (reference should be made to the effect of normal mode and common effects on signal information). When transmitted over telephone wire pairs, the resultant signal (at the receive end) will have been degraded in both waveshape and signal-to-noise ratios. Typical attenuation factors for a T1 line are −30dB per 6000 feet.

In addition, pair-to-pair crosstalk can degrade signal-to-noise ratios. The energy transmitted in the bipolar system of signal transfer is centered at 772kHz (generated by the bit format).

At the receiving end the bipolar signal information is converted to a unipolar pulse train after being amplified, filtered and fed through an automatic level control circuit. Some types
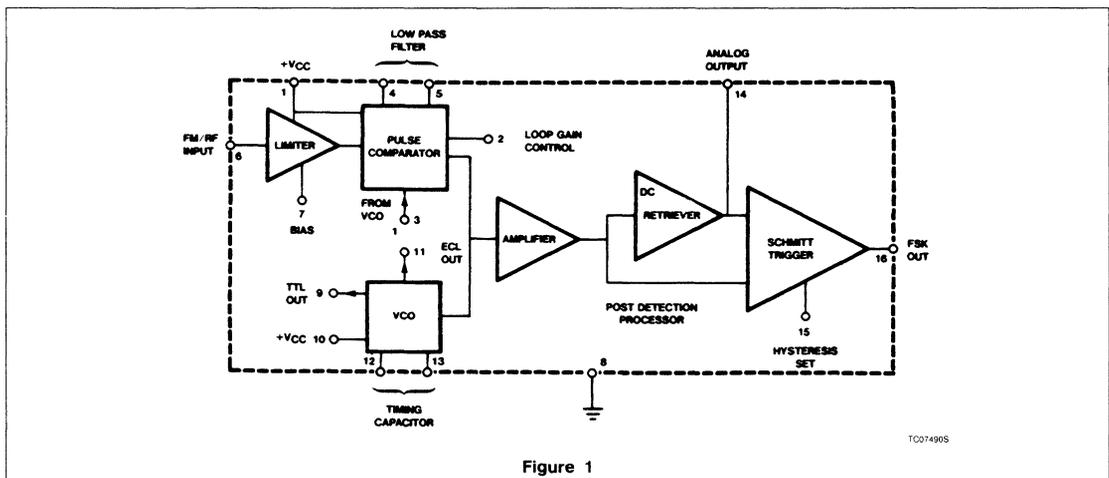

Figure 1

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)
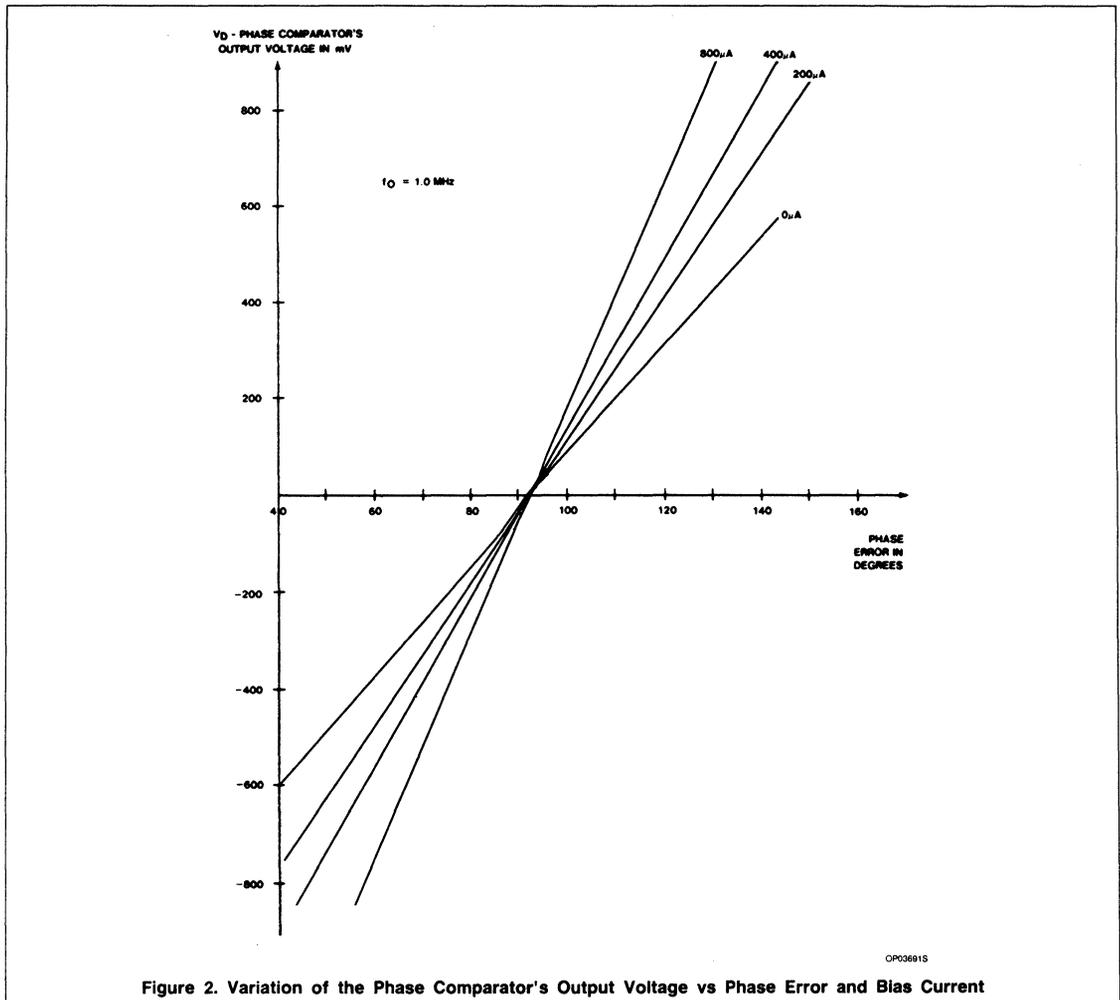
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Figure 2. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current

# Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

Figure 3. VCO Output Frequency as a Function of Input Voltage and Bias Current
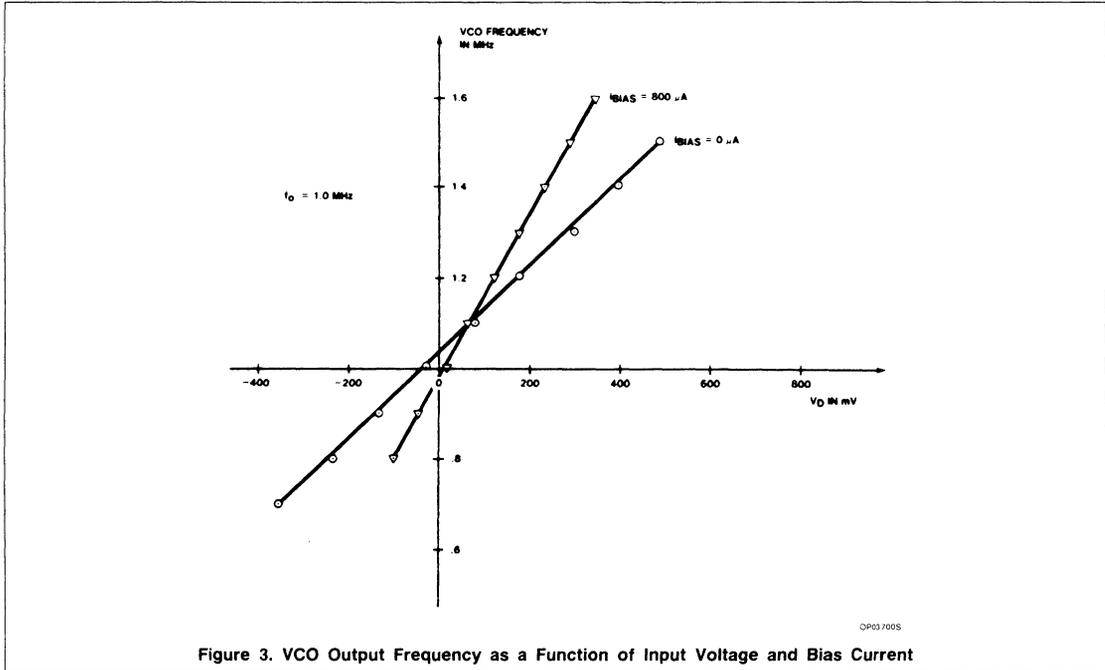
of PCM systems use the rectified and filtered DC (average) to control the phase of the regenerator clock; however, in newer systems, bipolar signals are preprocessed (or preconditioned) by terminal common equipment resulting in unipolar information.

T1 Data Transmission

The bipolar signal, as transmitted on a T1 line, appears below with the original binary, converted unipolar and clock waveform (reference Figure 5).

The bipolar signal, when transmitted over standard wire pairs, will be degraded both in wave shape and signal-to-noise by the time it reaches the signal repeater. This is due to the attenuation factor of the cable which is nearly −30dB for 6000 ft. In addition, pair to pair crosstalk degrades signal-to-noise. The energy in the transmitted bipolar signal is centered at 772kHz due to the particular bit format. Bipolar signals have no DC offset.

At each receiving station the bipolar signal is amplified, filtered and fed through an automatic level control circuit. A full wave rectified signal is then sent to the clock regeneration circuit. This is essentially the format followed by some of the original T1 repeater equipment. The clock regeneration circuit described here could be adapted to this system.

Figure 4
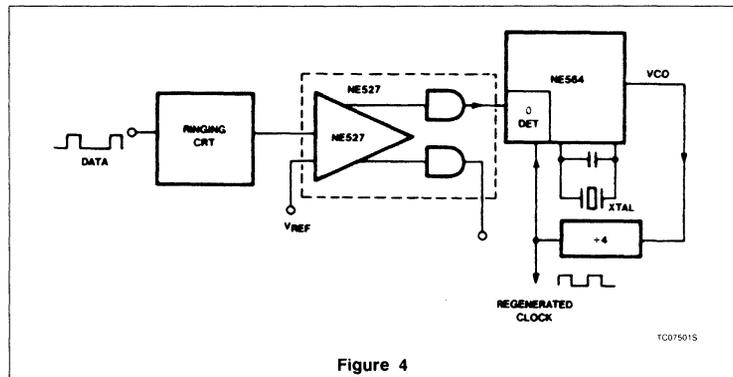
THE T1 SPECTRUM

The bipolar signal is similar to NRZ data in that it does not contain carrier information. In order to give the PLL coherent frequency information sufficient to obtain "capture" and lock, carrier components must be obtained from the data stream. The time duration of the frequency information fed to the PLL is also important in order to obtain accurate and stable information to update the PLL. In order to begin the extraction of frequency information, the positive-going portions of the bipolar data signals are used to drive a class "C"

transistor tank circuit (reference Figure 4) which is sharply tuned to the basic clock frequency (1.544MHz). Each positive half cycle of data then starts a wave train of coherent information which is phase synchronous with each succeeding positive data bit. When the LC tank is optimally tuned, relatively extended periods without data bits can be tolerated with minimal loss of frequency and phase information. The combination of good short-term frequency stability of the high "Q" LC tank, coupled with the long-term stability of the crystal-controlled VCO, is the founda-

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

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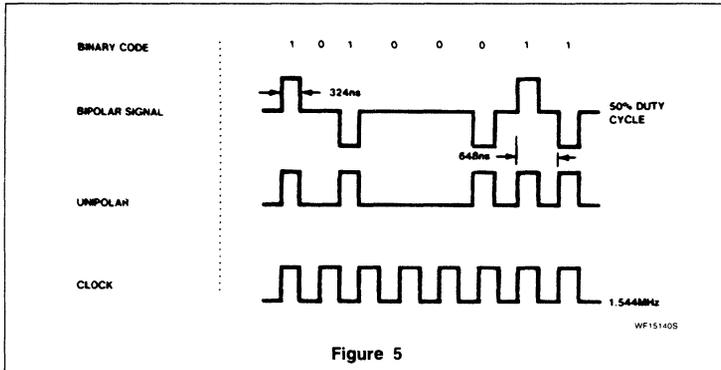
Figure 5
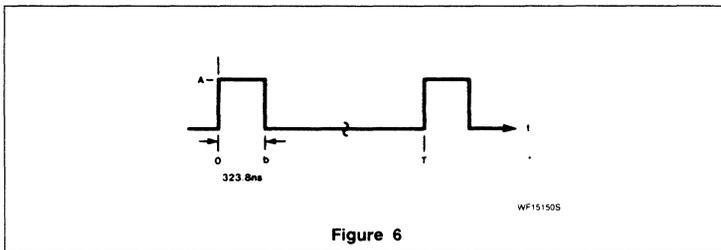
Figure 6

tion of the NE564 clock regeneration system accuracy.

It must be emphasized that data pulse synchronization of the preprocessing circuit must be frequency coherent with the fundamental period of the time base to be extracted. That is, if the time period of the clock is $1/f_C = T$, where f_C is the clock frequency, then the spacing between any positive code bit sequence must be $n \times T$ (reference Figure 6).

Looking at the spectral analysis of the relative energy available to the clock extraction circuitry (with a worst-case duty cycle of 1 of 16) will demonstrate the need for enchancing the particular desired frequency component before applying the signal to the Phase-Lock Loop. For $f_O = 1.544MHz$, the period is $T = 647.67ns$. The pulse or bit width is 323.8ns.

Here the bit duration 323.8ns = b. The Fourier expansion of the discrete spectrum is related by the following equation:

$$F_{(n)} = \frac{(Ab)}{T} \left| \frac{\sin(\frac{n\pi b}{t})}{\frac{n\pi b}{t}} \right| \quad n = 0, 1, 2 \dots \quad (1)$$

The basic frequency component resulting from various bit spacing factors is defined by the equation

$$f = \frac{1}{T} \quad (2)$$

where $f \leqslant f_O = 1.544MHz$.

If we consider the special case of a single pulse present out of 16 bipolar or 32NRZ periods, then

    $T = 16$ bipolar bit times
       $= 16 \times 647.67ns = 10.36\mu s$
    $f = 96.5kHz$

Accordingly, the spectral lines will be spaced in multiples of 96.5kHz. The spectrum for this

particular worst case condition is shown in Figure 7 below.

Solving equation 1 for the relative amplitude of the 1.544MHz spectral component with the pulse spacing shown,

$$F_{(16)}(\frac{Ab}{T}) \left| \frac{\sin(\frac{16\pi b}{t})}{(\frac{16\pi b}{t})} \right|$$

where $T = 2nb$, $n = 16$.

$$= (\frac{Ab}{(2)(16)b}) \frac{\sin(\frac{16\pi b}{32b})}{(\frac{16\pi b}{32b})} = \frac{A}{32} \frac{2}{\pi}$$

$$= (0.02)A$$
$$= -34dB$$

It is evident that as the bit spacing increases to the point where f_O is the 16th harmonic of the fundamental, very little f_O energy is available to drive a phase-lock regeneration circuit. $F_{(16)}$ is also ineffective since it is an even subharmonic of f_O. The PLL will not normally lock to even harmonics; in fact, an error signal is produced which tends to force the VCO out of lock. This fact further stresses the need for preprocessing in the frequency domain. The class "C" pulsed resonant tank significantly multiplies the magnitude of the f_O spectral component and filters out unwanted subharmonics.

The loop error voltage available from the phase detector for phase correction of the VCO is directly related to the product of the incoming coherent spectral energy multiplied in the balanced mixer with the reference signal derived from the VCO. Since the phase error information is integrated in the loop filters, the instantaneous magnitude of the DC error voltage is proportional to the time integral of coherent mixer products. Thus, as the magnitude and time duration of the desired frequency component is increased in the
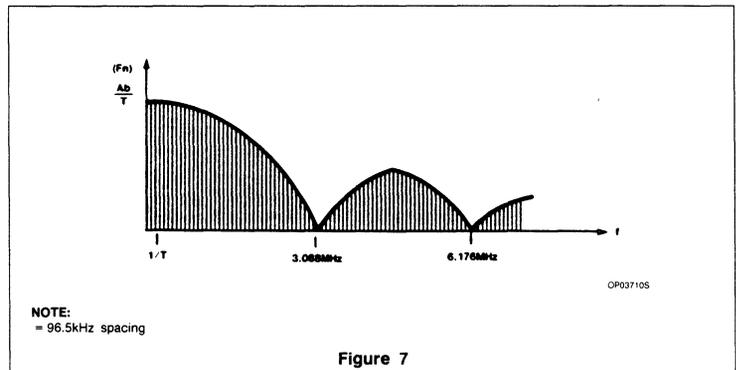
NOTE:
= 96.5kHz spacing

Figure 7

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

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preprocessing circuitry, the VCO phase accuracy is greatly improved. Capture time is obviously enhanced also.

The signal from the tuned tank is buffered by a FET follower N-channel enhancement mode device (reference Figure 12). This provides power gain with virtually no loading on the tank circuit and avoids degrading the "Q". The NE527 comparator is used to provide waveform shaping and symmetry correction. The voltage threshold is set up by a resistive divider with adjustment set for equal duty cycle symmetry. (Note: Recent tests have shown that best crystal lock range symmetry is achieved when the input signal to Pin 6 of the NE564 is maintained at a level between 500 to 800mVP-P.) The coupling network provides the necessary attenuation plus a low impedance signal source which is critical to good Phase Detector operation.

In the particular circuit shown in Figure 12, the 1.544MHz information is applied to the phase detector input of the NE564 Phase-Lock Loop. The VCO, however, is operated at four (4) times this frequency in order to take advantage of economical and readily available crystals. The VCO signal is fed through a divide-by-four counter (74HCT73) to provide the Phase Detector reference and final regenerated clock signal. To avoid loading, the clock signal (1.544MHz) is buffered by the 75451 peripheral driver which provides a high-speed open collector TTL output. The input signal is AC coupled in order to reduce DC bias errors in the Phase Detector caused by "O" level variations.
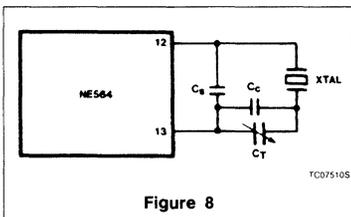
Figure 8

The Crystal[1]

The crystal used was chosen to match the NE564 VCO drive characteristics. It is an "AT" cut oscillator crystal which operates near the anti-resonate or "parallel" mode in this circuit. The crystal may have to be fine-tuned, as indicated in Figure 8. The pulling characteristic of the crystal is adequate to allow for 0 to 70°C operational drift plus initial and aging accuracy tolerance factors and still retain lock between master and slave station VCXOs. The average lock range at room temperature with one of sixteen data bits present is typically 1000Hz for a 6.176MHz crystal with a capture range greater than 500Hz.

For VCO operation at 6.176MHz, C_S is 22pF, C_C is 18pF, and C_t, a 1 – 8pF trimmer capacitor (reference Figure 8).

NE564 CRYSTAL-CONTROLLED VCO

As shown in Figure 8, the crystal is operated with a series capacitor. When properly trimmed, this allows the crystal to operate near the series resonant mode. A crystal manufactured to operate in the series resonant mode will do so only if it sees a pure resistance looking into the oscillator terminals. The circuit below shows an oscillator which looks inductive with the equivalent crystal circuit and trimmer capacitor C_t (reference Figure 9).

If L_o is small and the internal gain of the device high over a wide frequency range, L_o may resonate with the C_o of the crystal at a very high frequency. Under certain conditions the circuit may even tend to operate in the 3rd overtone mode unless measures are taken to roll-off the circuit gain. This is the purpose of C_s in Figure 8. Since the gain of the VCO is a factor in spurious oscillation, the current injected into Pin 2 will also have an effect in this respect. (K_o increases with I_2). At higher operating frequencies this parameter may become more critical in attaining stable start ups in the desired frequency mode. Obviously the size of C_s must be smaller than the value needed to cause free running near the desired frequency without the crystal connected.

CRYSTAL SPECIFICATION

Crystals may be manufactured to operate in either the series mode with no external capacitance (purely resistive load) or in the parallel mode with a specified value of load capacitance. The 564 tends to operate at a frequency above the specified value when a series mode crystal is used. For a design

frequency of 6.176000MHz and zero load capacitance. Referring to Figure 8, for $C_s = 10pF$ and $C_T = 10pF$ the average center frequency for an NE564 sample measured in the lab was 6181.192kHz. For the same C_s, but with C_T equal to 60pF, f_O measured 6176.565kHz. A second crystal showed a spread of 6176.600kHz to 6180.855kHz. The effect of the VCO was to pull the crystal to a frequency above its design value. This effect is then nearly tuned out by the external capacitances C_S and C_T. If C_T is sufficiently increased, the crystal will see a purely resistive load and operate at its rated frequency.

A second approach is to specify a crystal which is to operate near the anti-resonate or parallel mode. Normally this is done with a certain value of external load capacitance specified by the customer which matches the existing circuit parameters. The maximum difference between series and parallel resonance for any crystal is 0.5% of f_O (series resonant mode); for $f_r = 6.126MHz$, 0.5% of $f_r = 30kHz$. The usual value would be lower than this.

$$f_a = f_r \sqrt{1 + \frac{1}{r_O}}$$

r_O = electromechanical coupling factor, f_a = parallel resonant frequency). The particular cut of the crystal material determines the drift response over temperature. For oscillator applications, the AT cut offers the best overall stability over a wide frequency and temperature range. Final design uses second approach.

For a stability or total tolerance of ± 15ppm over the rated operating range of –20°C to + 70°C, a certain manufacturer's crystal actually performed as shown above (Refer to Figure 11).

Calibration accuracy is the allowable frequency tolerance at the reference temperature, i.e., ± 10ppm @ 25°C.
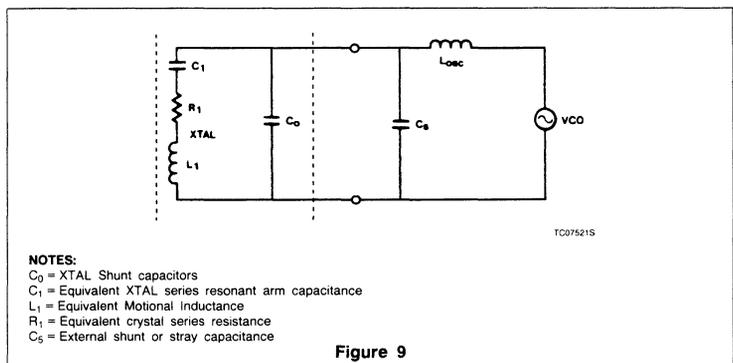
NOTES:
C_0 = XTAL Shunt capacitors
C_1 = Equivalent XTAL series resonant arm capacitance
L_1 = Equivalent Motional Inductance
R_1 = Equivalent crystal series resistance
C_S = External shunt or stray capacitance

Figure 9

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

NOTES:
C_1 = Motional capacitance
C_0 = Shunt capacitance
R_1 = Equivalent Resistance
L_1 = Equivalent inductance

TC07530S

Figure 10. Basic Crystal Equivalent Circuit

WF15160S

Figure 11. Design Example
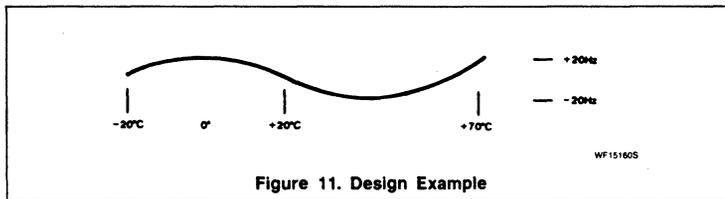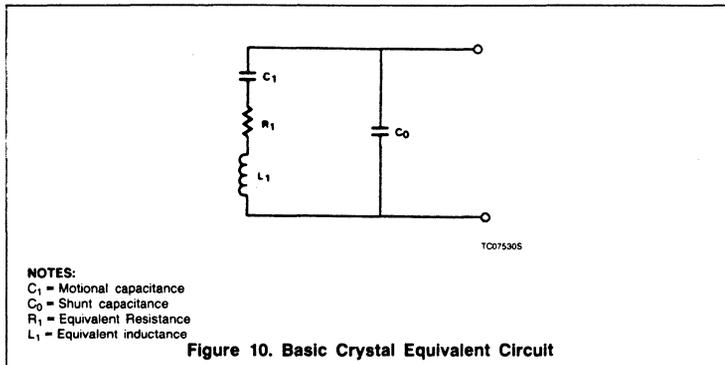
Using our reference crystal of 6.176MHz and the above specifications, the crystal limits over a 1 year period would be:

Temperature
stability: ± 15ppm × 6.176
                  = ± 93Hz

Calibration
tolerance: ± 10ppm × 6.176
                  = ± 62Hz
@ 25°C

Long term drift: ± 2ppm × 1 × 6.176
                  = ± 12Hz

Total: (± 167Hz)

The above figure of ± 167Hz then determines the capture and lock range over which two crystal stabilized VCOs must track under worst case conditions when the exact same crystal specifications are used for master and slave units within an operational system.

Crystal Specifications

'AT' Cut Oscillator Type

Fundamental mode operation HC-33 Case (Standard)

Calibration tolerance:
± 10ppm @ 25°C

Temperature stability:
± 15ppm; −15°C to +65°C

Circuit operating condition:
Parallel resonance

Frequency specified: 6.176000MHz

Part designation:
Croven #A330 DEF-32 or equivalent

Setup Procedure

Referring to Figure 12, the following setup procedure will aid the user in establishing proper circuit operation.

Regulated supply voltage of +5V and −6V are required. Current drain on the +5V line is ~ 100mA, and 6mA for the −6V.

With proper voltage applied, (1) First check the supply currents to be sure they are in the range indicated above. (2) Check the operation of the NE564 VCXO by looking at Pin 9 with an oscilloscope (see Figure 13). A reasonably symmetric square wave should be present, having a frequency near 6.1MHz. (3) Attach a DVM across the 2k resistor which feeds Pin 2 of the NE564 and adjust for a reading of 2.00V, indicating a 1mA $_{DC}$ current flowing into Pin 2 (The (+) lead of the DVM should be connected to the end of the 2k resistor which ties to the wiper of the 10k pot and the (−) lead to Pin 2 of the 564; reference Figure 14). (4) The exact center frequency is set by adjusting C_t, the crystal trimmer cap, for exactly 6.176000MHz with no signal input (this sets the center frequency of the VCXO to free-run in the center of the capture range). (5) Enable strobe 'A' and 'B' with a +2.7V min. to +5V max. level. Apply a standard 1.544MBS NRZ data signal to the input terminal, terminated in 50Ω. The amplitude should be +3 to +5V (0 to peak). Set the duty cycle for 1 bit in a 16-bit period. Note the data

generator must be driven from a crystal-controlled master oscillator also adjusted for a center data rate of 1.544 000MBS. Monitor the buffered output of the ringing circuit with a scope connected to the source of the SD213 (Figure 15). The waveform should appear as in Figure 17. (6) Adjust tank trimmer cap C_T for a maximum amplitude and note that the cycle period should be 647ns. (7) Now monitor the comparator output signal at Pin 7 and adjust R_t for a 50% duty cycle. The same signal will appear at Pin 5 of the NE527 except it will be inverted. The signal on Pin 7 of the NE527 and Pin 6 of the NE564 should appear as shown in Figure 19. Now attach one lead of a dual-trace scope to Pin 7 of the NE527 and the other to Pin 3 of the NE564 as shown (Figure 16).

The two signals should be in phase-locked with an approximate 90° differential as shown in Figure 20 (data signal applied to @ 1.544MBS). If lock does not occur, a slight trimming of the crystal trimmer C_T should correct for slight differences in master-to-slave crystal tolerance. It is recommended that master and slave crystals be of the exact same design and specification to insure optimal tracking over time and temperature. A recommended manufacturer and part number appears at the end of this application note for your convenience.

Once lock is attained, move one lead of the dual-trace scope to the buffered output of the 75451 Pin 3, leaving the other scope probe on Pin 6 of the NE564. The phase-locked waveform should appear as in Figure 25. If a data word generator is being used, you may check overall operation for various bit patterns by synchronizing the scope trigger on the "end of word" pulse, then observe the phase error effect as different combinations are fed in.

PHASE JITTER

When operating with real-time data transmission, the PLL loop filters must be optimized to minimize regenerated clock jitter. A good grade of mylar capacitor is recommended as connected to Pins 4 and 5 of the NE564. A simple pair of shunt-connected loop filter caps of 0.33μF to 0.76μF was found to be adequate.

Figure 12. Data Transmission System Clock Regenerator
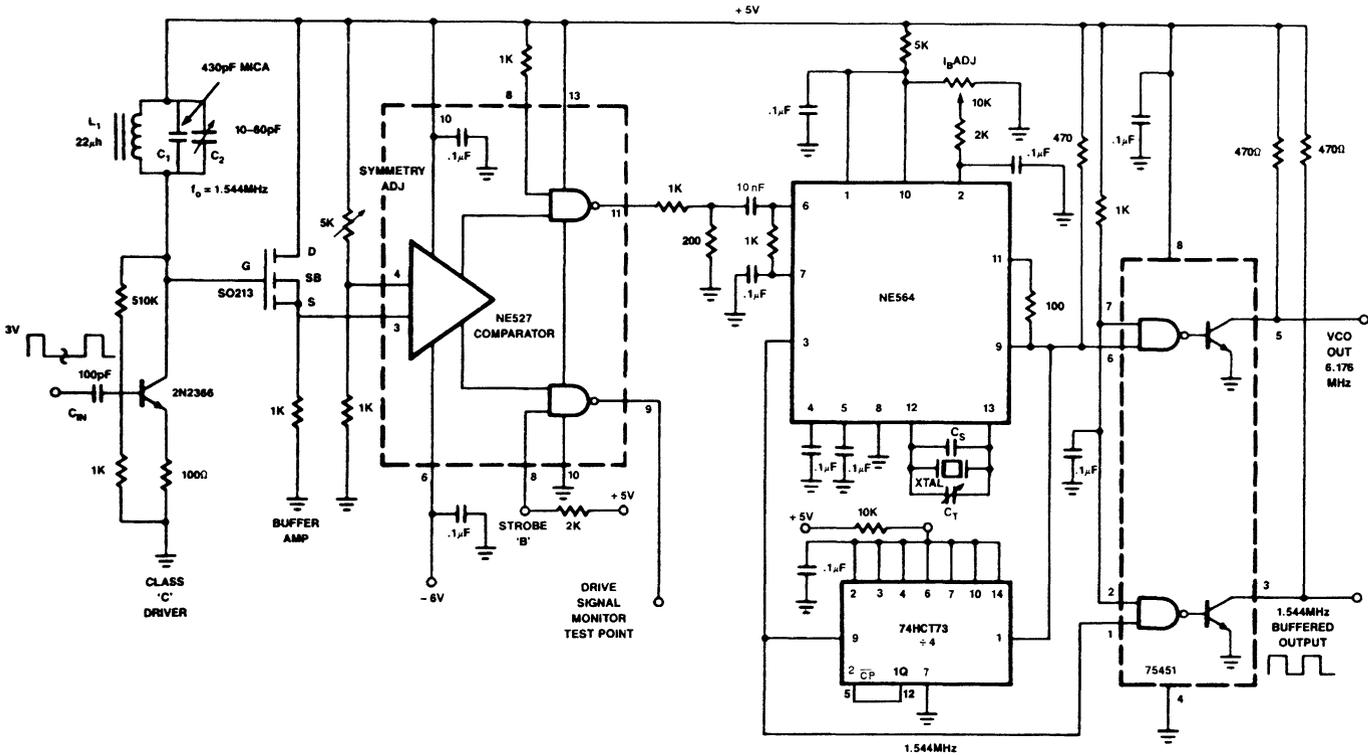
NOTES:
C_S = 100pF
C_T = 1–8pF trimmer
XTAL = crven A330 Def-32
       'AT' cut oscillator or equivalent
crystal f_O = 6.176000MHz

TC21291S

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)
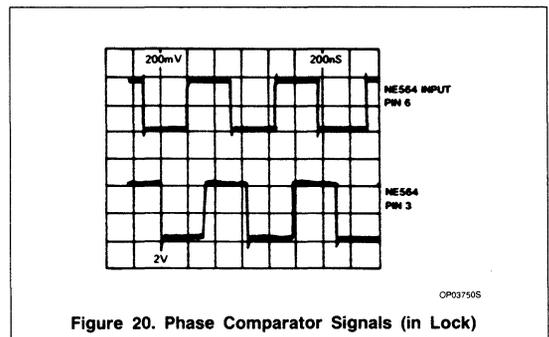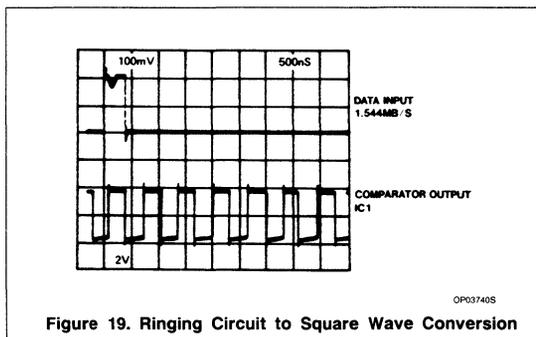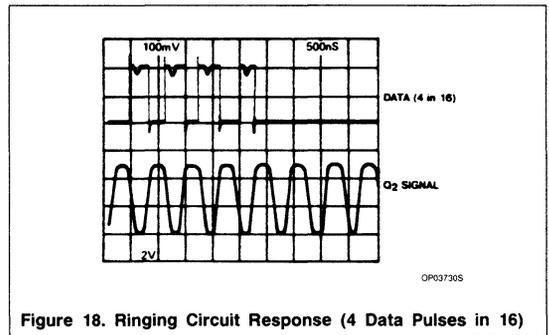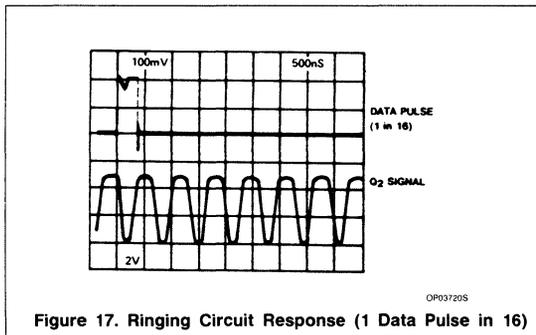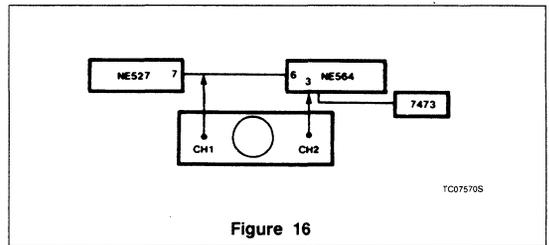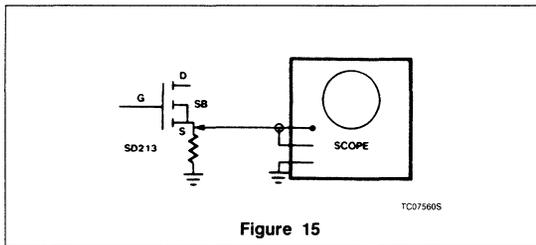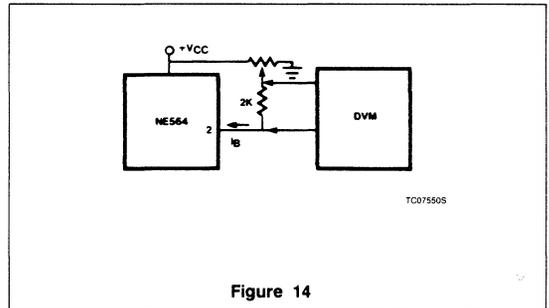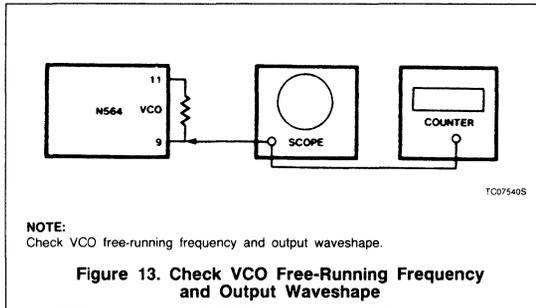
NOTE:
Check VCO free-running frequency and output waveshape.

Figure 13. Check VCO Free-Running Frequency and Output Waveshape

Figure 14

Figure 15

Figure 16

Figure 17. Ringing Circuit Response (1 Data Pulse in 16)

Figure 18. Ringing Circuit Response (4 Data Pulses in 16)

Figure 19. Ringing Circuit to Square Wave Conversion

Figure 20. Phase Comparator Signals (in Lock)

Clock Regenerator With Crystal-Controlled Phase-Locked VCO (NE564)

AN182

OP03760S
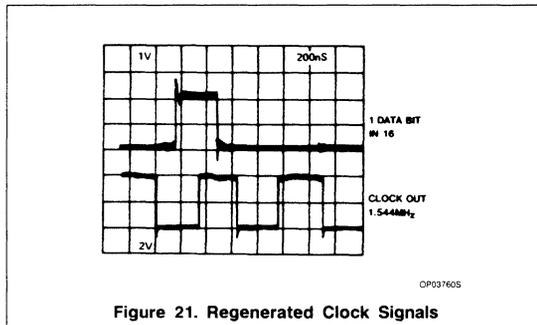
Figure 21. Regenerated Clock Signals

OP03770S
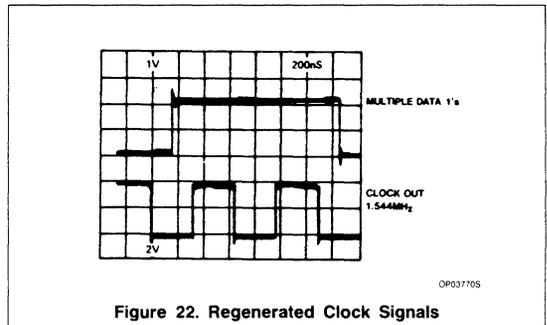
Figure 22. Regenerated Clock Signals

OP03780S
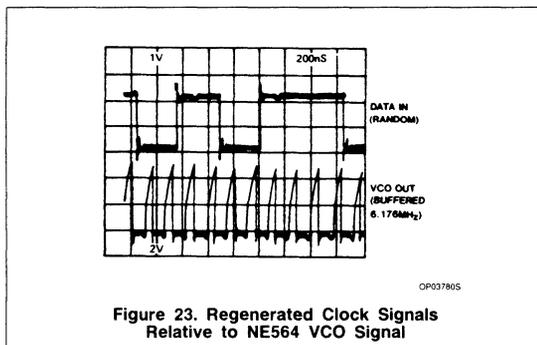
Figure 23. Regenerated Clock Signals Relative to NE564 VCO Signal

OP03790S
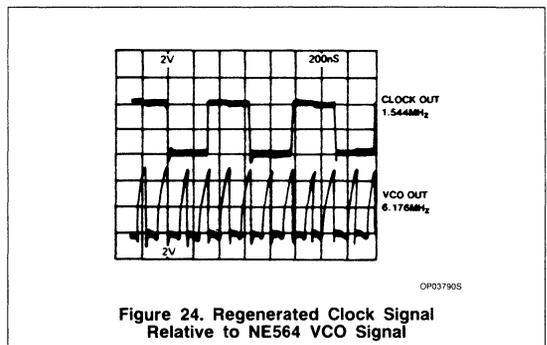
Figure 24. Regenerated Clock Signal Relative to NE564 VCO Signal

OP03800S
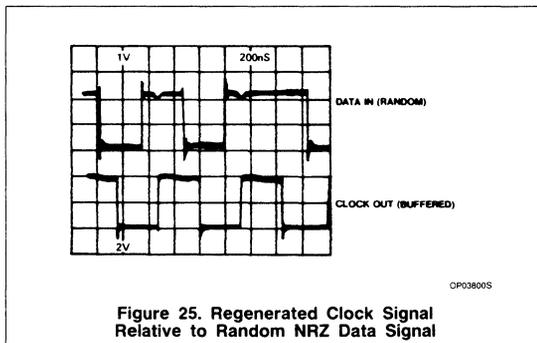
Figure 25. Regenerated Clock Signal Relative to Random NRZ Data Signal

NOTES:
1. Recent versions of this circuit no longer require series capacitors C_C and C_T. See Figure 12.
2. Input levels to the NE564 have been reduced for this application to $\simeq$ 800mVp-p. See Figure 12.
3. Improved operation regarding clock jitter is obtained by carefully decoupling the divider counter ICs and the PLL's V_{CC} line. This is accomplished by adding a small series "R" into the V_{CC} line with the bypass capacitor to ground.

References
1. "Fourier Analysis" by Hwei P. Hsu. Simon & Schuster Tech Outlines
2. "Pulse and Digital Circuits" by Millman and Taub McGraw Hill
3. "Phaselock Techniques" by Floyd M. Gardner Wiley, 1966

Signetics

NE/SE564
Phase-Locked Loop

Product Specification

Linear Products

DESCRIPTION

The NE564 is a versatile, high guaranteed frequency phase-locked loop designed for operation up to 50MHz. As shown in the Block Diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

FEATURES

- **Operation with single 5V supply**
- **TTL-compatible inputs and outputs**
- **Guaranteed operation to 50MHz**
- **External loop gain control**
- **Reduced carrier feedthrough**
- **No elaborate filtering needed in FSK applications**
- **Can be used as a modulator**
- **Variable loop gain (externally controlled)**

APPLICATIONS

- **High-speed modems**
- **FSK receivers and transmitters**
- **Frequency synthesizers**
- **Signal generators**
- **Various satcom/TV systems**

PIN CONFIGURATION

D, F, N Packages

Pin	Label		Pin	Label
1	V+		16	TTL OUTPUT
2	LOOP GAIN CONTROL		15	HYSTERESIS SET
3	INPUT TO PHASE COMPARATOR FROM VCO		14	ANALOG OUTPUT
4	LOOP FILTER		13	FREQ. SET CAP.
5	LOOP FILTER		12	FREQ. SET CAP.
6	FM/RF INPUT		11	VCO OUTPUT #2
7	BIAS FILTER		10	V+
8	GROUND		9	VCO OUTPUT TTL

TOP VIEW

CD11151S
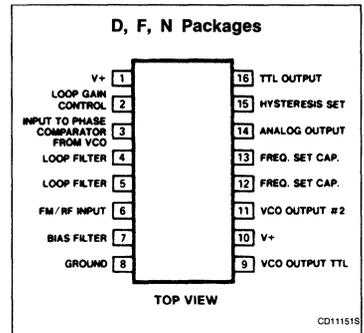
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic SO	0 to +70°C	NE564D
16-Pin Plastic DIP	0 to +70°C	NE564N
16-Pin Plastic DIP	−55°C to +125°C	SE564N
16-Pin Cerdip	−55°C to +125°C	SE564F

BLOCK DIAGRAM

BD07550S
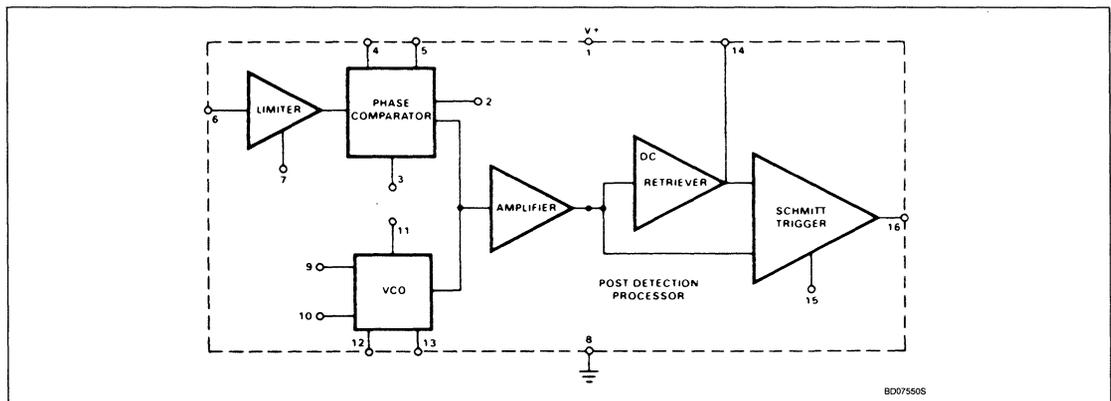
Phase-Locked Loop

NE/SE564

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+	Supply voltage Pin 1 Pin 10	 14 6	V
I_{OUT}	(Sink) Max (Pin 9)	10	mA
P_D	Power dissipation	600	mW
T_A	Operating ambient temperature NE SE	 0 to +70 −55 to +125	°C
T_{STG}	Storage temperature	−65 to +150	°C

NOTE:
Operation above 5V will require heatsinking of the case.

DC AND AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V, T_A = 25°C, f_O = 5MHz, I_2 = 400µA, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Maximum VCO frequency	C_1 = 0 (stray)	50	65		45	60		MHz
	Lock range	Input ≥ 200mV$_{RMS}$ T_A = 25°C T_A = 125°C T_A = −55°C T_A = 0°C T_A = 70°C	40 20 50	70 30 80		40	70 70 40		% of f_O
	Capture range	Input ≥ 200mV$_{RMS}$, R_2 = 27Ω	20	30		20	30		% of f_O
	VCO frequency drift with temperature	f_O = 5MHz, T_A = −55°C to +125°C T_A = 0 to +70°C = 0 to +70°C f_O = 500kHz, T_A = −55°C to +125°C T_A = 0 to +70°C	 300	500 300	1500 800		 600 500		PPM/°C
	VCO free-running frequency	C_1 = 91pF R_C = 100Ω "Internal"	4	5	6	3.5	5	6.5	MHz
	VCO frequency change with supply voltage	V_{CC} = 4.5V to 5.5V		3	8		3	8	% of f_O
	Demodulated output voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 2%T = 25°C 1%T = 25°C 1%T = 0°C 1%T = −55°C 1%T = 70°C 1%T = 125°C	16 8 6 12	28 14 10 16		16 8	28 14 13 15		mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$ mV$_{RMS}$
	Distortion	Deviation: 1% to 8%		1			1		%
S/N	Signal-to-noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
	AM rejection	Std. condition, 30% AM		35			35		dB
	Demodulated output at operating voltage	Modulation frequency: 1kHz f_O = 5MHz, input deviation: 1% V_{CC} = 4.5V V_{CC} = 5.5V	7 8	12 14		7 8	12 14		mV$_{RMS}$ mV$_{RMS}$
I_{CC}	Supply current	V_{CC} = 5V I_1, I_{10}		45	60		45	60	mA
	Output "1" output leakage current "0" output voltage	V_{OUT} = 5V, Pins 16, 9 I_{OUT} = 2mA, Pins 16, 9 I_{OUT} = 6mA, Pins 16, 9		1 0.3 0.4	20 0.6 0.8		1 0.3 0.4	20 0.6 0.8	µA V V

Phase-Locked Loop
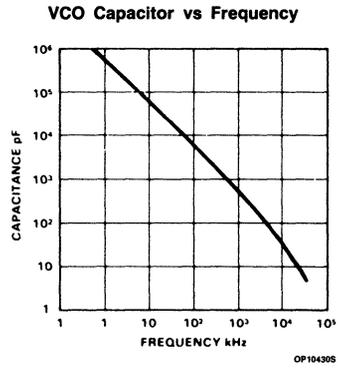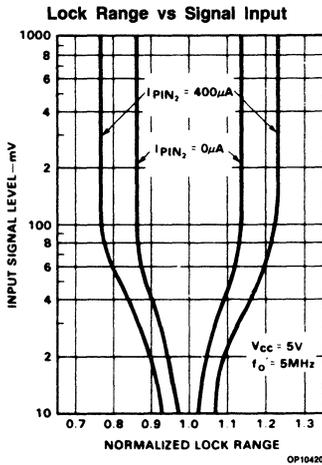
NE/SE564

TYPICAL PERFORMANCE CHARACTERISTICS

Lock Range vs Signal Input

OP10420S

VCO Capacitor vs Frequency

OP10430S

Typical Normalized VCO Frequency as a Function of Pin 2 Bias Current

OP10440S

Typical Normalized VCO Frequency as a Function of Pin 2 Bias Current

OP10450S

Normalized VCO Frequency as a Function of Temperature

OP10460S

Phase-Locked Loop

NE/SE564

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current (K_D)

VCO Output Frequency as a Function of Input Voltage and Bias Current (K_O)
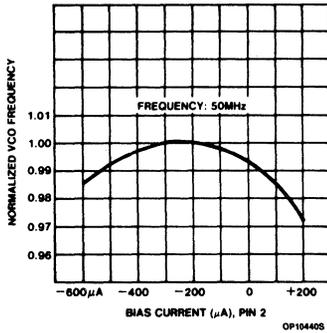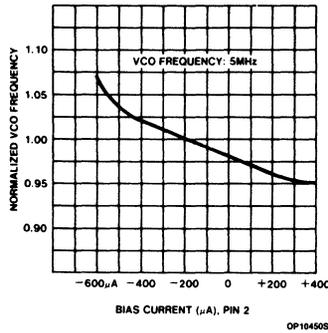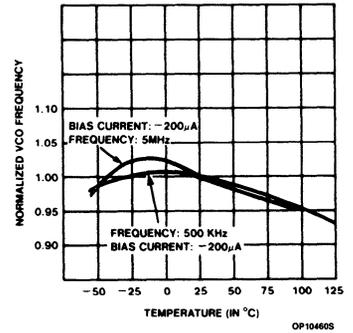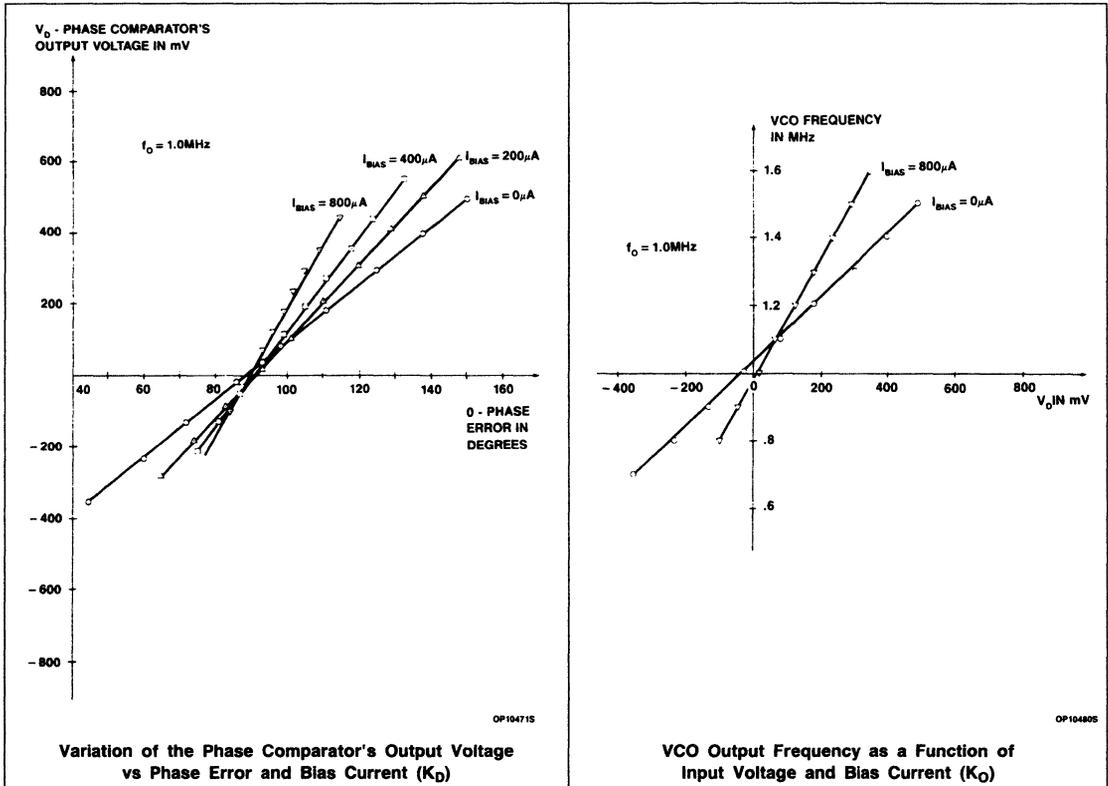
TEST CIRCUIT
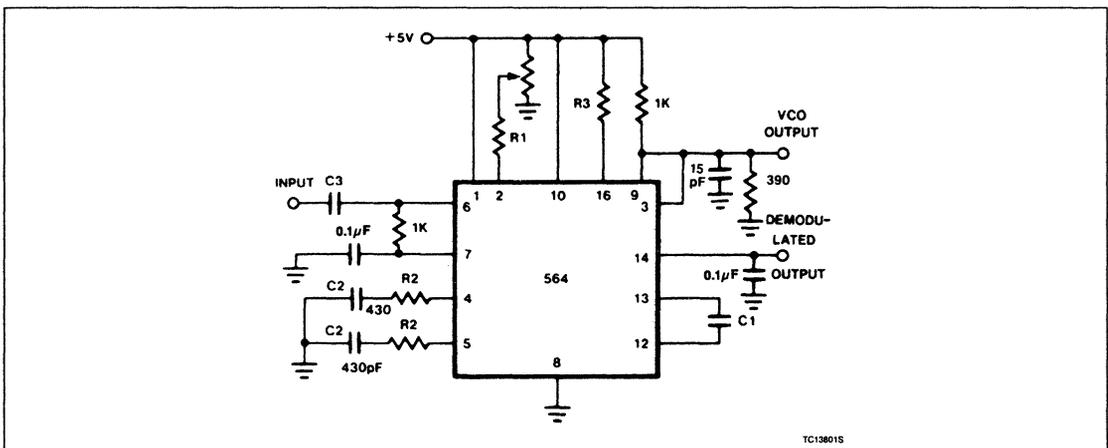
Phase-Locked Loop

NE/SE564

FUNCTIONAL DESCRIPTION (Figure 1)

The NE564 is a monolithic phase-locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz.

In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{IN} - f_O)}{K_{VCO}} \qquad (1)$$

K_{VCO} = conversion gain of the VCO

f_{IN} = frequency of the input signal

f_O = free-running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{IN} from f_O. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at Pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free-running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the DC levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow-band signals where the deviation in f_{IN} itself may be less than the change in f_O due to temperature. This effect can be eliminated if the DC or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the DC levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high-frequency performance, an emitter-coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources $Q_{25} - Q_{26}$ form the basic oscillator. The approximate free-running frequency of the oscillator is shown in the following equation:

$$f_O \simeq \frac{1}{22\ R_C\ (C_1 + C_S)} \qquad (2)$$

EQUIVALENT SCHEMATIC
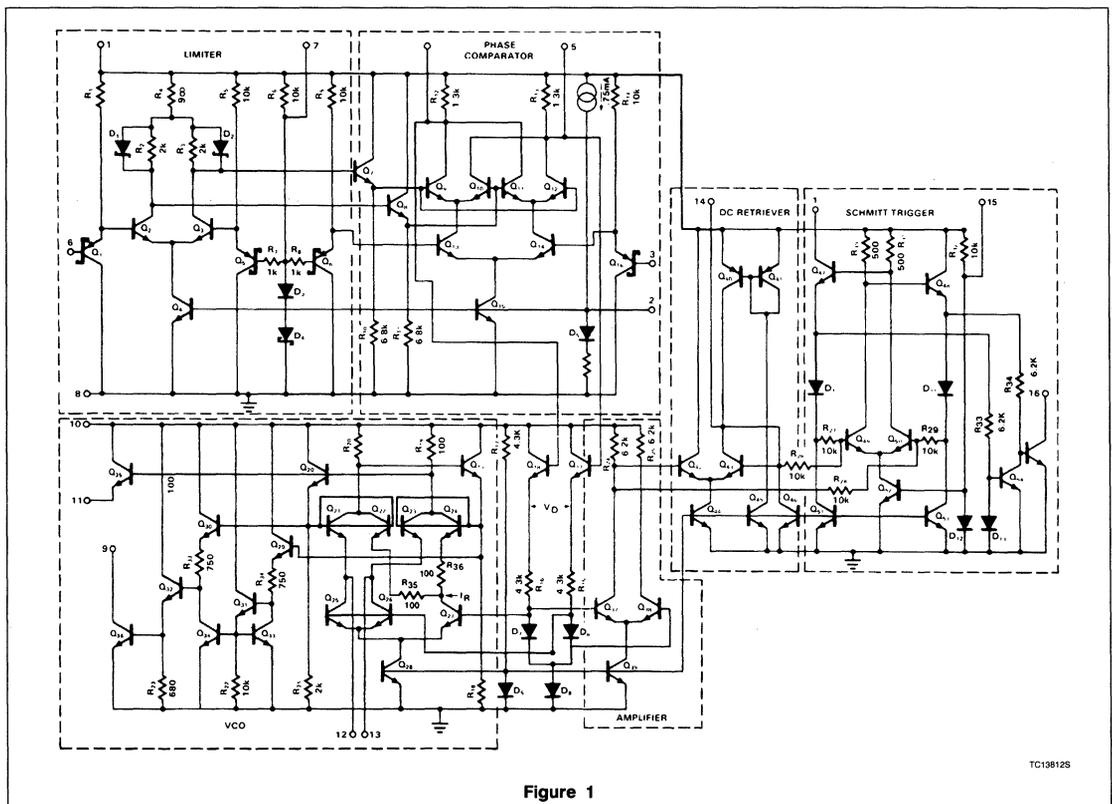
Figure 1

Phase-Locked Loop

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)

C_1 = external frequency setting capacitor

C_S = stray capacitance

Variation of V_D (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section
The phase comparator consists of a double-balanced modulator with a limiter amplifier to improve AM rejection. Schottky-clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at Pin 2.

Post Detection Processor Section
The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a DC retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the DC retriever is formed by the transductance am-
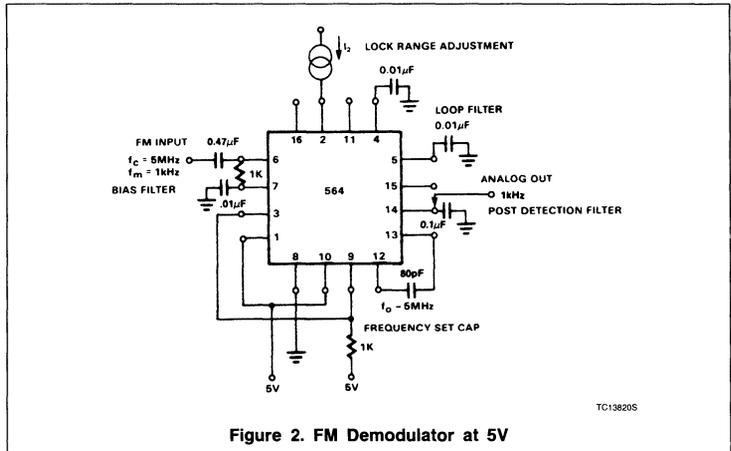
Figure 2. FM Demodulator at 5V

plifier $Q_{42} - Q_{43}$ together with an external capacitor which is connected at the amplifier output (Pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_M}{C_2} V_{IN} dt \qquad (3)$$

g_M = transconductance of the amplifier

C_2 = capacitor at the output (Pin 14)

V_{IN} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the DC or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of $Q_{49} - Q_{50}$ with positive feedback being provided by $Q_{47} - Q_{48}$. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a DC control, provides symmetric variation around the nominal value.

Design Formula
The free-running frequency of the VCO is shown by the following equation:

$$f_O \simeq \frac{1}{22\ R_C\ (C_1 + C_S)} \qquad (4)$$

$R_C = 100\Omega$

C_1 = external cap in farads

C_S = stray capacitance
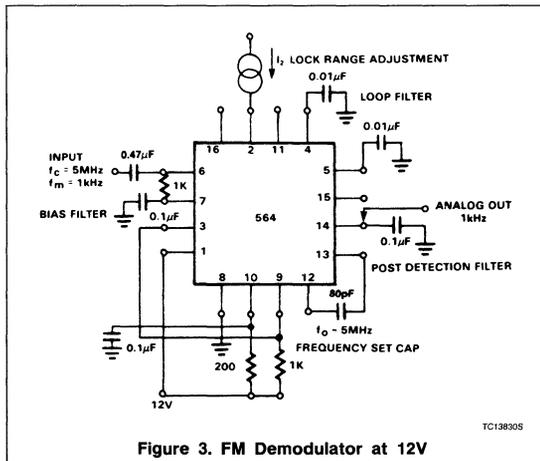
**Figure 3. FM Demodulator at 12V**
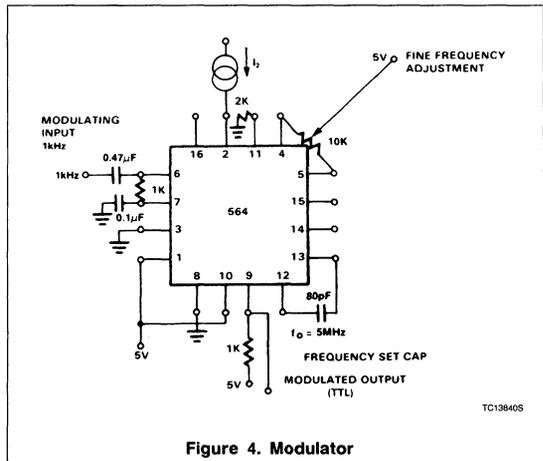
Figure 4. Modulator

Phase-Locked Loop

NE/SE564

The loop filter diagram shown is explained by the following equation:

$$F_S = \frac{1}{1 + sRC_3} \text{ (First Order)} \qquad (5)$$

$$R = R_{12} = R_{13} = 1.3k\Omega \text{ (Internal)*}$$

By adding capacitors to Pins 4 and 5, a pole is added to the loop transfer function at

$$\omega = \frac{1}{RC_3}$$

NOTE:
*Refer to Figure 1.

APPLICATIONS

FM Demodulator
The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in Figures 2 and 3, respectively. The input signal is AC coupled with the output signal being extracted at Pin 14. Loop filtering is provided by the capacitors at Pins 4 and 5 with additional filtering being provided by the capacitor at Pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal

the frequency deviation in the input signal should be 1% or higher.

Modulation Techniques
The NE564 phase-locked loop can be modulated at either the loop filter ports (Pins 4 and 5) or the input port (Pin 6) as shown in Figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in Figure 5. This curve will be appropriate for signals injected into Pins 4 and 5 as shown in Figure 4.

FSK Demodulation
The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5V power supply. Demodulated DC voltages associated with the mark and space frequencies are recovered with a single external capacitor in a DC retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high-frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 5 shows a high-frequency FSK decoder designed for input frequency deviations of ± 1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from Figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_O' to 10.8MHz.

The lock range graph indicates that the ± 1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero Pin 2 bias current. (While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_O' frequencies).

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 7 for 20k, 500k, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators' output voltages with respect to each other and to the FSK output. The high-frequency sum components of the input and VCO frequency also are visible as noise on the phase comparator's outputs.
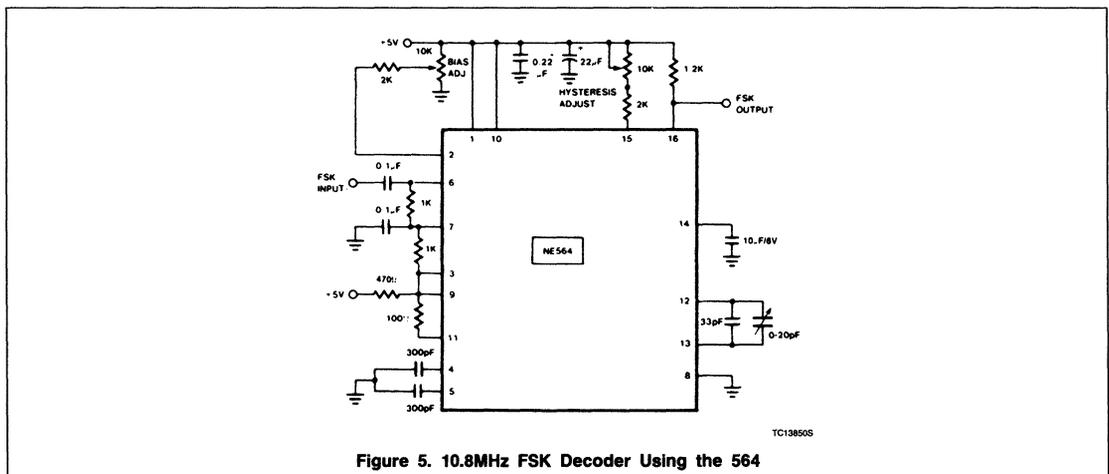

Figure 5. 10.8MHz FSK Decoder Using the 564

a. Data Rate = 20k Baud

WF17950S

b. Data Rate = 500k Baud

WF17960S

c. Data Rate = 2.0m Baud

WF17970S

NOTES:
1. Top trace = Pin 4
2. Center trace = Pin 5
3. Bottom trace = Pin 16

Figure 6. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs
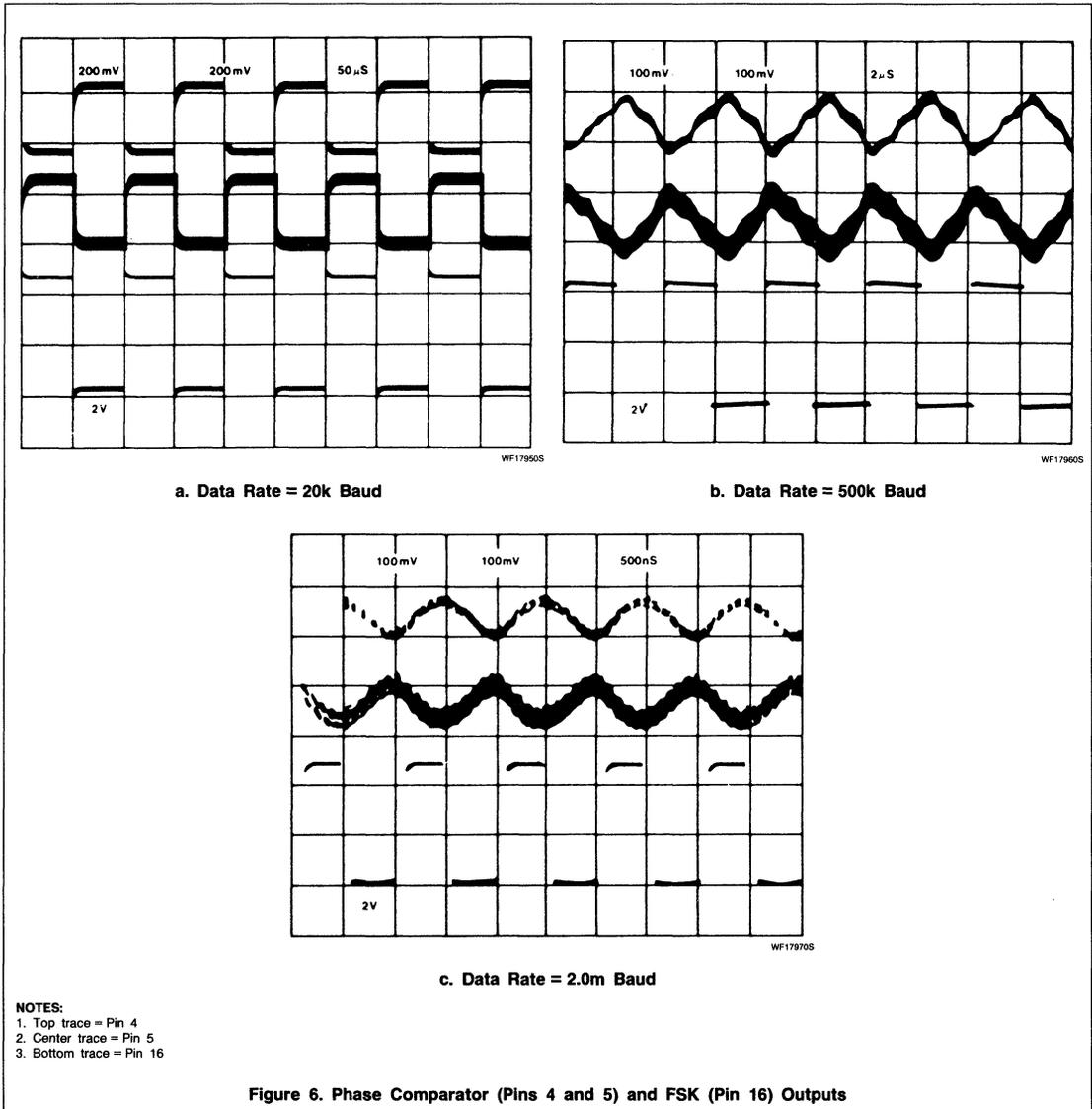
OUTLINE OF SETUP PROCEDURE

1. Determine operating frequency of the VCO:

   If ÷ N in feedback loop, then
   $f_O = N \times f_{IN}$.

2. Calculate value of the VCO frequency set capacitor:

   $$C_O \simeq \frac{1}{2200 \, f_O}$$

3. Set I_2 (current sinking into Pin 2) for $\cong$ 100μA. After operation is obtained, this value may be adjusted for best dynamic behavior.

4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to φ det.). Adjust C_O trim or frequency adj. Pins 4 – 5 for exact center frequency, if needed.

5. Close loop and inject input signal to Pin 6. Monitor Pins 3 and 6 with two-channel

scope. Lock should occur with $\Delta\phi_{3-6}$ equal to 90° (phase error).

6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pins 4 and 5. (See PLL application section).

7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not 50% in

Phase-Locked Loop

duty cycle, DC offsets will occur in the loop which tend to create an artificial or biased VCO offset.

8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of $10 - 50\mu F$ on Pins

4, 5. Also, careful supply decoupling may be necessary. This includes the counter chain V_{CC} lines.
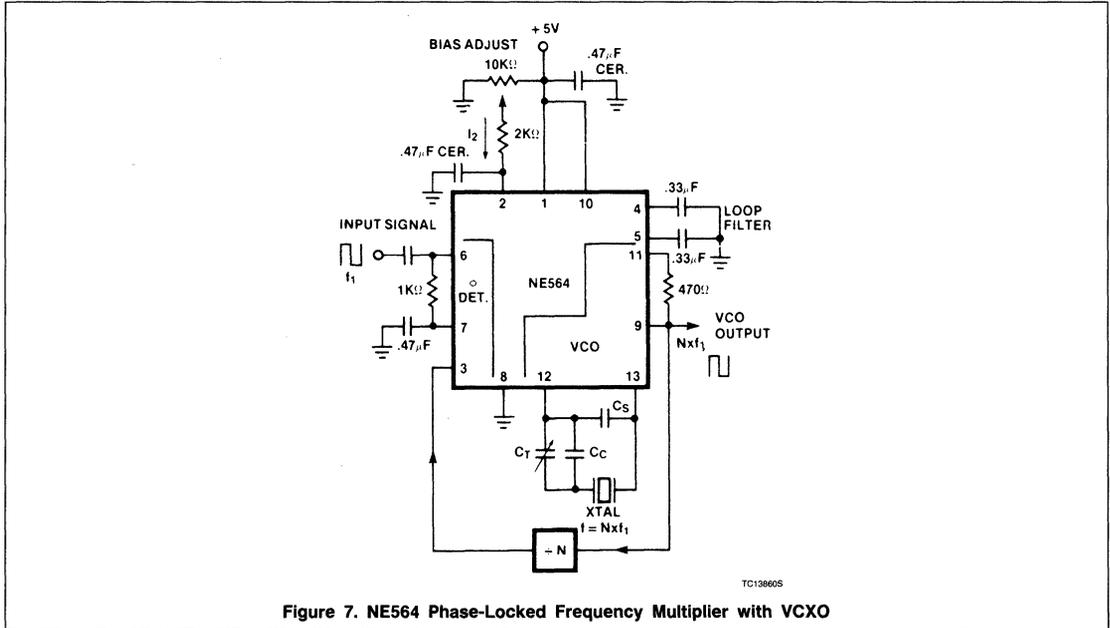
Figure 7. NE564 Phase-Locked Frequency Multiplier with VCXO

Signetics

AN179
Circuit Description of the NE564

Application Note

Linear Products

CIRCUIT DESCRIPTION Of The NE564

The 564 contains the functional blocks shown in Figure 1. In addition to the normal PLL functions of phase comparator, VCO, amplifier and low-pass filter, the 564 has internal circuitry for an input signal limiter, a DC retriever, and a Schmitt trigger. The complete circuit for the 564 is shown in Figure 1.

Limiter

The input limiter functions to produce a near constant amplitude output that serves as the input for the phase comparator. Eliminating amplitude variations in the FM input signal improves the AM rejection of the PLL. Additional features of the 564's limiter are that it is capable of accepting TTL signals, operates at high frequencies up to 50MHz, and remains

functional with variable supply voltages between 5 and 12V.*

Signal limiting is accomplished in the 564 with a differential amplifier whose output voltage is clipped by diodes D_1 and D_2 (see Figure 2). Schottky diodes are used because their limiting occurs between 0.3 to 0.4V instead of the 0.6 to 0.7V for regular IC diodes. This lower limiting level is helpful in biasing, especially for 5V operation. When limiting, the DC voltage across R_2 R_3 remains at the Schottky diode voltage. Good high-frequency performance for Q_2 and Q_3 is achieved with current levels in the low mA range. Current-source biasing is established via the current mirror of D_5 and Q_4 (See Figure 1).

Base biasing for Q_3 is of concern because of the nature of the input signal which can be either a TTL digital signal of 0 to 5V amplitude

or a low-level, AC coupled analog signal. Compatibility for either type is achieved by modifying the limiter of Figure 2 with the addition of the vertical Schottky PNP transistors Q_1 and Q_5 as shown in Figure 3. The input signal voltage appears as a collector-base voltage for Q_1, which presents no problems for either high TTL level inputs or low-level analog inputs. Q_5 is in turn diode-biased by D_3 and D_4 (see Figure 1) which places the base voltages of Q_1 and Q_5 at approximately 1.0V. This same biasing network establishes a 1.3V bias at the base of Q_{13} for biasing the phase comparator section. A differential output signal from the input limiter is applied to one input of the phase comparator (Q_9 through Q_{12}) after buffering the level shifting through the $Q_7 - Q_8$ emitter-followers.

*When operating above 5V$_{DC}$, a limiting resistor must be used from V$_{CC}$ to Pin 10 of the 564.
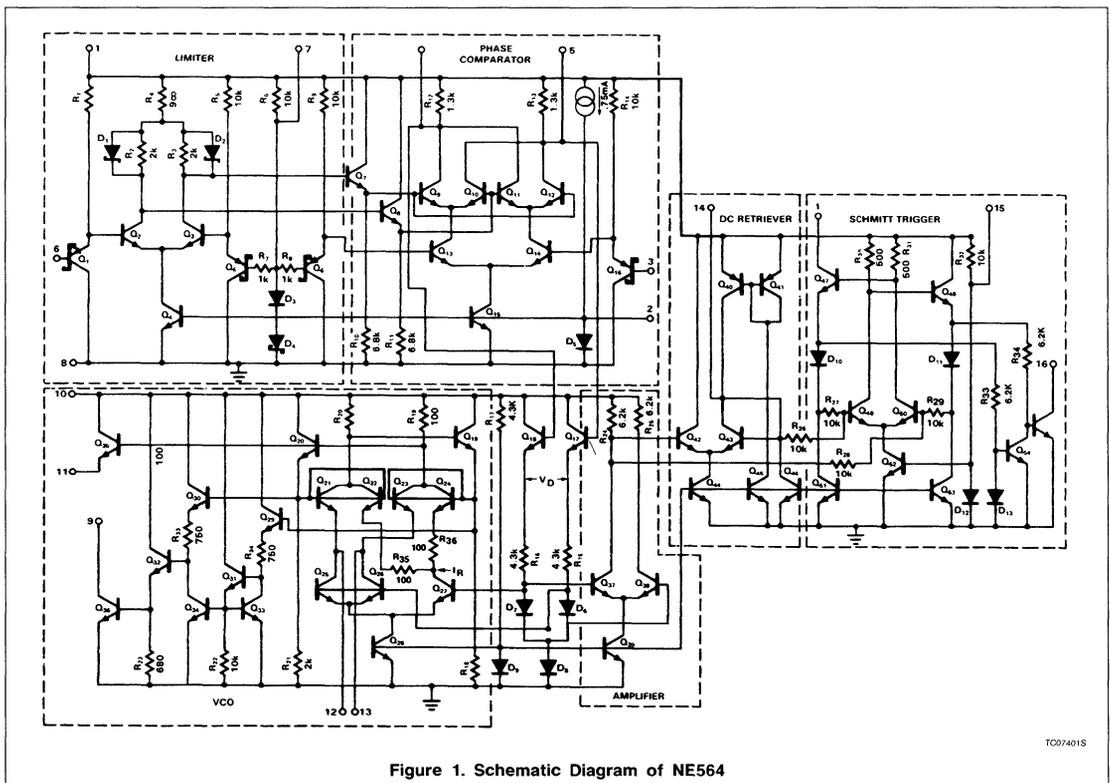
Figure 1. Schematic Diagram of NE564

TC07401S

# Circuit Description of the NE564
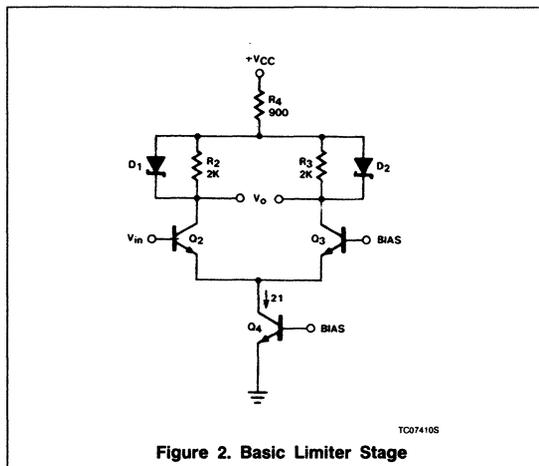
Figure 2. Basic Limiter Stage
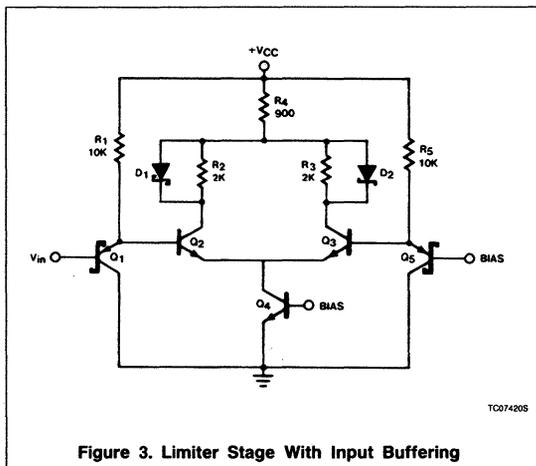
Figure 3. Limiter Stage With Input Buffering

Phase Comparator

The phase comparator section of the 564 is shown in Figure 4. It is basically the conventional, double-balanced mixer commonly used in PLL circuits, with a few exceptions. The transconductance, g_M, for the $Q_{13} - Q_{14}$ differential amplifier is directly proportional to the mirror current in Q_{15}. Thus, by externally sinking or sourcing current at Pin 2, g_M can be changed to alter the phase comparator's conversion gain, K_d. The nominal current injected into this node by the internal current source is 0.75mA for 5V operation. If the current is externally removed by gating, the phase comparator can be disabled and the VCO will operate at its free-running frequency.
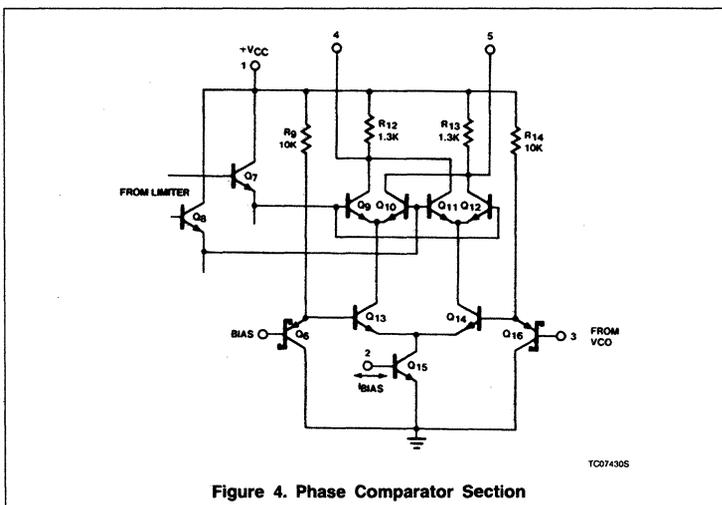
Figure 4. Phase Comparator Section

Circuit Description of the NE564
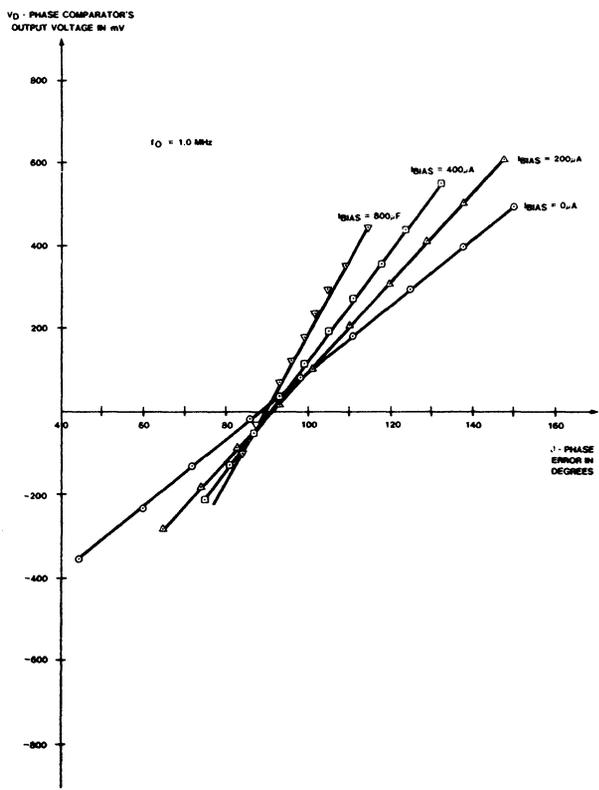
Figure 5. Variation of the Phase Comparator's Output Voltage vs Phase Error and Bias Current

Circuit Description of the NE564

AN179
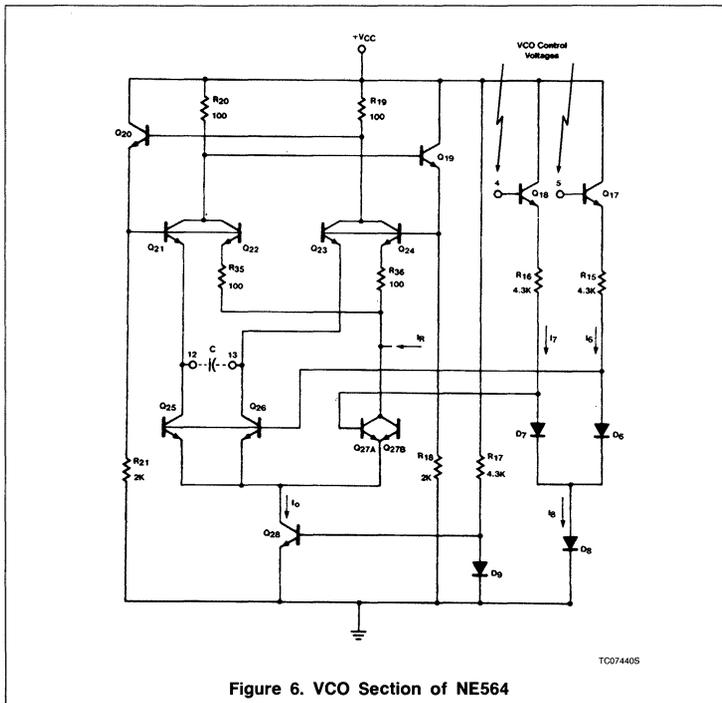
Figure 6. VCO Section of NE564
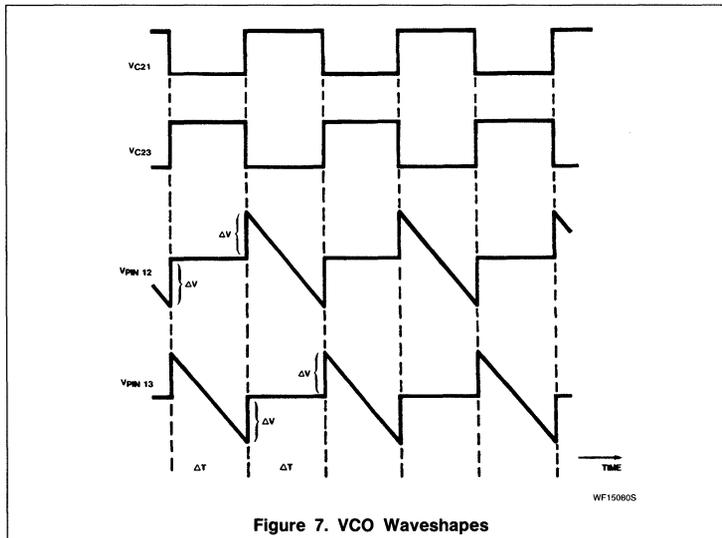
Figure 7. VCO Waveshapes

The variation of K_d with bias current at Pin 2 is shown in the experimental results of Figure 5. Note that the inherent 90° phase error in the loop produces an approximate zero-phase comparator output voltage. For any particular bias current, the slope of the line is the K_d conversion gain for the phase comparator. Numerically the data of Figure 5 can be expressed as

$$K_d \simeq 0.46 \left(\frac{\text{volts}}{\text{rad}} \right)$$

$$+ 7.3 \times 10^{-4} \left(\frac{\text{volts}}{\text{rad} \times \mu A} \right) \times I_{BIAS} \ (\mu A)$$

$$(1)$$

Equation 1 is valid for bias current less than $800\mu A$ where saturation occurs within the phase comparator.

The current level established in Q_{15} of Figure 3 determines all other quiescent currents in the phase comparator (Q_9 through Q_{14}). Currents through R_{12} and R_{13} set the common-mode output voltage from the phase comparator (Pins 4 and 5). Since this common-mode voltage is applied to the VCO to establish its quiescent currents, the VCO conversion gain (K_o) also depends upon the bias current at Pin 2.

VCO

The VCO is of the basic emitter-coupled astable type with several modifications included to achieve the high frequency, TTL compatible operation while maintaining low frequency drift with temperature changes. The basic oscillator in Figure 6 consists of Q_{19}, Q_{20}, Q_{21}, and Q_{23} with current sinks of Q_{25} and Q_{26}. The master current sink of Q_{28} keeps the total current constant by altering the ratio of currents in $Q_{25} - Q_{26}$ and the dummy current sink of Q_{27}.

The input drive voltage for the VCO is made up of common-mode and difference-mode components from the phase comparator. After buffering the level shifting through $Q_{17} - Q_{18}$ and $R_{15} - R_{16}$, the VCO control voltage is applied differentially to the base of Q_{27} and to the common bases of Q_{25} and Q_{26}.

The VCO control voltages from the phase comparator are the Pin 4 and Pin 5 voltages or

$$V_4 = V_{C9} = V_{B18} = V_{CM} + \tfrac{1}{2}V_{DM} \qquad (2)$$

$$V_5 = V_{C12} = V_{B17} = V_{CM} - \tfrac{1}{2}V_{DM} \qquad (3)$$

where V_{CM} and V_{DM} are the respective common-mode and difference-mode voltages.

Circuit Description of the NE564

Emitter-followers Q_{17} and Q_{18} convert these control voltages into control currents through D_6 and D_7 of the form

$$I_6 = \frac{1}{R_{15}}\left[V_{CM} - \tfrac{1}{2}V_{DM} - 3 \; V_{BE}\right] \quad (4)$$

$$I_7 = \frac{1}{R_{16}}\left[V_{CM} + \tfrac{1}{2}V_{DM} - 3V_{BE}\right] \quad (5)$$

These individual currents are summed in D_8 and become with $R_{15} = R_{16} = R$.

$$I_8 = I = I_6 + I_7 = \tfrac{2}{R}(V_{CM} - 3 \; V_{BE}) \quad (6)$$

Writing I_6 and I_7 as functions of the total I current gives

$$I_6 = \frac{1}{2}(1 - \frac{V_{DM}}{RI}) \quad (7)$$

$$I_7 = \frac{1}{2}(1 + \frac{V_{DM}}{RI}) \quad (8)$$

Now consider variations in I_6 and I_7 while I remains constant.

Let 'x' indicate the current imbalance such that

$$I_6 = (1 - x)I = \frac{1}{2}(1 - \frac{V_{DM}}{RI}) \quad (9)$$

$$I_7 = xI = \frac{1}{2}(1 + \frac{V_{DM}}{RI}) \quad (10)$$

where $0 \leqslant x \leqslant 1$. Thus x is defined to be

$$x = \frac{1}{2}(1 + \frac{V_{DM}}{RI}) \quad (11)$$

Currents I_6 and I_7 establish proportional currents in Q_{25}, Q_{26}, and Q_{27} in a manner similar to the analysis above since the current in Q_{28} is a constant, or

$$I_O = I_{C28} = I_{E25} + I_{E26} + _{E27A} + I_{E27B}$$

It can be shown that the $D_7 - D_8$ diode pair will cause identical differential currents to be reflected in both the $Q_{25} - Q_{26}$ and the $Q_{27A} - Q_{27B}$ differential amplifier pairs. Consequently, the constant-current of I_O, jointly shared by the differential amplifier pairs, will divide in each pair with the same x factor imbalance as in Equation 11.

$$I_{E25} + I_{E26} = xI_O \quad (12)$$

$$I_{E25} = I_{E26} = \frac{x}{2}I_O \quad (13)$$

$$I_{E27A} + I_{E27B} = (1 - x)I_O \quad (14)$$

$$I_{E27A} = I_{E27B} = (\frac{1 - x}{2})I_O \quad (15)$$

Now consider placing a capacitor between the collectors of Q_{25} and Q_{26} (Pins 12 and 13). Oscillation will occur with the capacitor alternately being charged by Q_{21} and Q_{23} and constantly discharged by Q_{25} and Q_{26}. When the Q_{21} and Q_{22} pair conducts, Q_{23} and Q_{24} will be off, causing a negative ramp voltage to appear at Pin 13 and a constant voltage at Pin 12 as shown in Figure 7. During the next half-cycle, the transistor roles and voltages are reversed. Capacitor discharge is via Q_{25} and Q_{26}, which act as constant-current sinks with current amplitudes as in Equation 13.

During each half-cycle, the capacitor voltage changes linearly by $2\Delta V$ volts in ΔT seconds where

$$\Delta V = 2R_{20}I_O\left(\frac{x}{2} + \frac{1 - x}{2}\right) = R_{20}I_O \quad (16)$$

and

$$\Delta T = \frac{C2\Delta V}{I_{E25}}. \quad (17)$$

Combining these two equations with Equation 13 gives a half period of

$$\Delta T = \frac{4C \; R_{20}}{x} \quad (18)$$

Utilizing Equation 11 with the ΔT expression gives the desired VCO frequency expression of

$$f_O = f_O'(1 + \frac{V_{DM}}{RI}) = f_O'\left[\frac{V_{DM}}{2(V_{CM} - 3 \; V_{BE})}\right] \quad (19)$$

where f_O' is the VCO's free-running frequency given by

$$f_O' = \frac{1}{22 \; R_{20}C} \quad (20)$$

Equation 19 shows that the oscillator frequency is a linear function of the differential voltage from the phase comparator. Resistors R_{35} and R_{36} function to insure that an initial current imbalance exists between the $Q_{25} - Q_{26}$ transistor pair and the dummy Q_{27}. This imbalance insures that the oscillator is self-starting when power is first applied to the circuit.

The VCO conversion gain is determined as

$$K_o = \frac{\partial f_O}{\partial V_{DM}} = \frac{f_O'}{RI} \; Hz/V \quad (21)$$

which is valid as long as the transistor's V_{BE} changes are small with respect to the common-mode voltage. Both f_O and K_o are in-


VCO FREQUENCY
IN MHz

$I_{BIAS} = 800 \, \mu A$

$I_{BIAS} = 0 \, \mu A$

$f_o = 1.0$ MHz

V_D IN mV

OP03620S
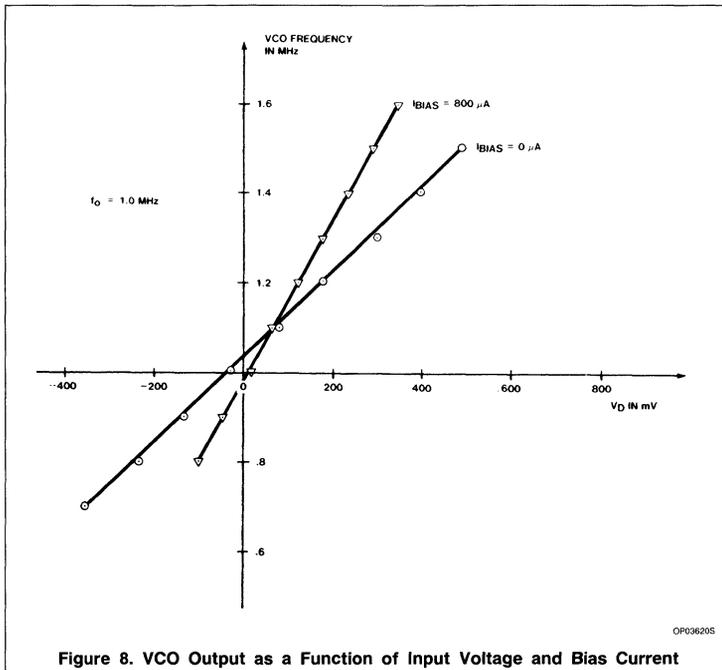
Figure 8. VCO Output as a Function of Input Voltage and Bias Current

Circuit Description of the NE564

AN179
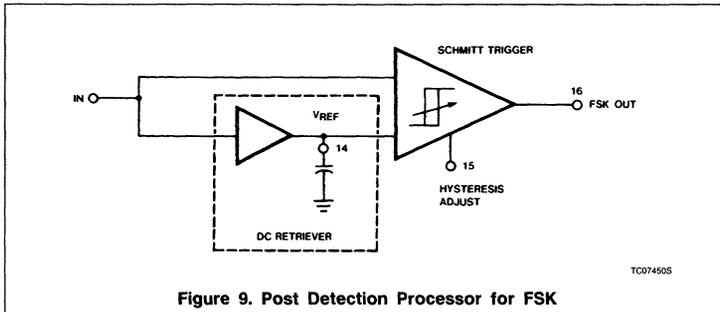
Figure 9. Post Detection Processor for FSK

versely proportional to R, which has a strong positive temperature coefficient. An internal current I_R having an equal and opposite negative temperature coefficient is inserted into the VCO as shown in Figure 6.

Experimental determination of K_o can be found from the data of Figure 8 where K_o is the slope of either line. Numerically these results are for $I_{BIAS} = 0$.

$$K_o = 0.95 \frac{MHz}{V} = 5.9 \times 10^6 \frac{rad}{volt\text{-}sec}$$
(22)

and for $I_{BIAS} = 800\mu A$

$$K_o = 1.7 \frac{MHz}{V} = 10.45 \times 10^6 \frac{rad}{volt\text{-}sec}$$
(23)

It must be noted that the specific values obtained for K_o in the manner above are valid only for the 1.0MHz free-running frequency where the data was taken. However, good estimates for K_o at other free-running frequencies can be obtained by linearly scaling K_o to the desired f_O'. Thus, it is sometimes convenient to define a normalized K_o as

$$K_{o(norm)} = \frac{K_o}{f_O'} = 5.9 \frac{rad}{V} (I_{BIAS} = 0)$$

$$= 10.45 \frac{rad}{V} (I_{BIAS} = 800\mu A)$$
(24)

The K_o estimate for any bias then can be obtained by multiplying the normalized conversion gain by the desired free-running frequency, or

$$K_o(any\ f_O') = K_{o(norm)} f_O'.$$
(25)

The additional VCO circuitry of Q_{29} through Q_{36} functions to produce the TTL and ECL compatible outputs at Pins 9 and 11.

Amplifier
The difference-mode voltage from the phase comparator is extracted and amplified by the amplifier in Figure 1. The single-ended output from this amplifier serves as input signals for both the Schmitt Trigger and a second differential amplifier. Low-pass filtering with a large capacitance at Pin 14 produces a stable DC reference level as the second input to the Schmitt Trigger. When the PLL is locked, the voltage at Pin 14 is directly proportional to the difference between the input frequency and f_O'. Thus Pin 14 provides the demodulated output for an FM input signal.

Schmitt Trigger
In FSK applications, the Pin 14 voltage will assume two different voltage levels corresponding to the mark and space input frequencies. A voltage comparator could be used to sense and convert these two voltage levels to logic compatible levels. However, at high data rates, V_{DM} will contain a consider-

able amount of carrier signal which can be removed by extensive filtering. Normally this complex filtering requires quite a few components, most all of which are external to the monolithic PLL. Also, since the control voltage for the comparator depends upon K_o and the deviations of the mark and space frequencies from f_O', the filtering has to be optimized for each different system utilized. However the necessary DC reference level for the comparator is present in the PLL but buried in carrier-frequency feedthrough which appears as noise in the system. A Schmitt trigger with variable hysteresis can be used successfully to decode the FSK data without the need for extensive filtering.

Consider the system shown in Figure 9 where the input signal is the single-ended output derived from the amplifier section of the 564. The DC retriever functions to establish a DC reference voltage for the Schmitt trigger. The upper and lower trigger points are adjustable externally around the reference voltage giving the variable hysteresis. For very low data rates, carrier feedthrough will be negligible and the ideal situation depicted in Figure 10 results. Increased data rate produces carrier feedthrough shown in Figure 10b, where false FSK outputs result because the feedthrough amplitude exceeds the hysteresis voltage. Having the capability to increase the hysteresis, as in Figure 10c, produces the desired FSK output in the presence of carrier feedthrough.

Another important factor to be considered is the temperature drift of the f_O' in the VCO. Small changes in f_O' will change the DC level of the input voltage to the Schmitt trigger. This DC voltage shift would produce errors in the FSK output in narrow-band systems where the mark and space deviations in f_{IN} are less than the f_O' change with temperature. However, this effect can be eliminated if the DC or average value of the amplifier signal is retrieved and used as the reference voltage for the Schmitt trigger. In this manner, variations in the f_O' with temperature do not affect the FSK output.

Circuit Description of the NE564

a. Low Data Rates With Negligible Carrier Feedthrough

b. False FSK Outputs Due to Feedthrough and Low Hysteresis

c. Increased Hysteresis Restores Proper FSK Output
in the Presence of Feedthrough

Figure 10. Waveshapes for FSK Decoding in the Post Detection Processor

Signetics
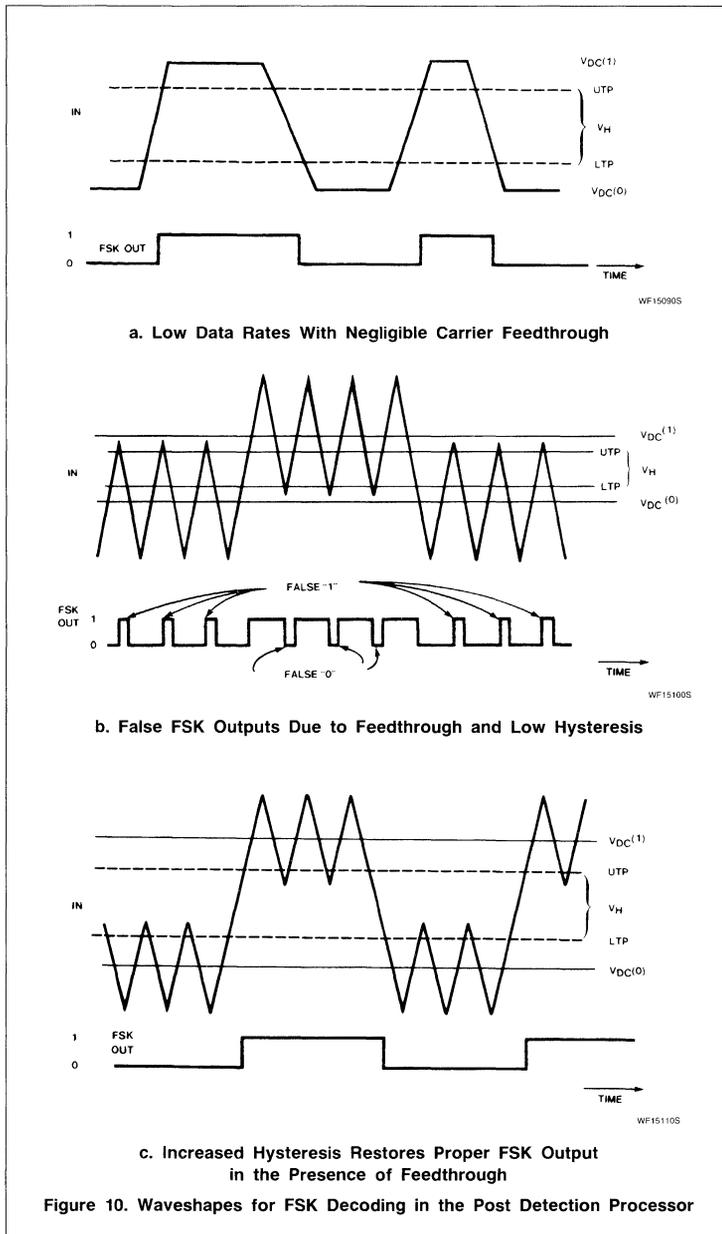
NE568
150MHz Phase-Locked Loop

Preliminary Specification

Linear Products

DESCRIPTION

The NE568 is a monolithic phase-locked loop (PLL) which operates from 1Hz to frequencies in excess of 150MHz. The integrated circuit consists of a limiting amplifier, a current-controlled oscillator (ICO), a phase detector, a level shift circuit, V/I and I/V converters, an output buffer, and bias circuitry with temperature and frequency compensating characteristics. The design of the NE568 is particularly well-suited for demodulation of FM signals with extremely large deviation in systems which require a highly linear output. In satellite receiver applications with a 70MHz IF, the NE568 will demodulate ± 20% deviations with less than 1.0% typical non-linearity. In addition to high linearity, the circuit has a loop filter which can be configured with series or shunt elements to optimize loop dynamic performance. The NE568 is available in 20-pin dual in-line and 20-pin SO (surface-mounted) plastic packages.

FEATURES

- Operation to 150MHz
- High linearity buffered output
- Series or shunt loop filter component capability
- Temperature compensated

APPLICATIONS

- Satellite receivers
- Fiber-optic video links
- VHF FSK demodulators
- Clock recovery

PIN CONFIGURATION

D, N Packages

V_{CC2}	1	20	LF1
GND2	2	19	LF2
GND1	3	18	LF3
TCAP1	4	17	LF4
TCAP2	5	16	FREQ ADJ
GND1	6	15	OUT_{FILT}
V_{CC1}	7	14	V_{OUT}
REFBYP	8	13	TC_{ADJ2}
PNPBYP	9	12	TC_{ADJ1}
INPBYP	10	11	V_{IN}

TOP VIEW

CD13070S
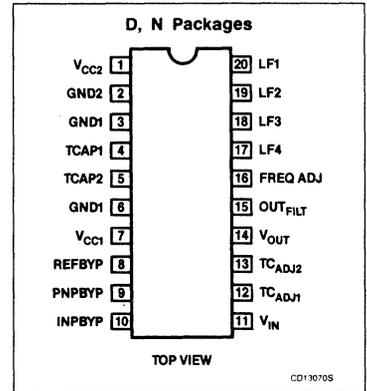
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic SOL Package	0 to +70°C	NE568D
20-Pin Plastic DIP	0 to +70°C	NE568N

BLOCK DIAGRAM

BD09501S
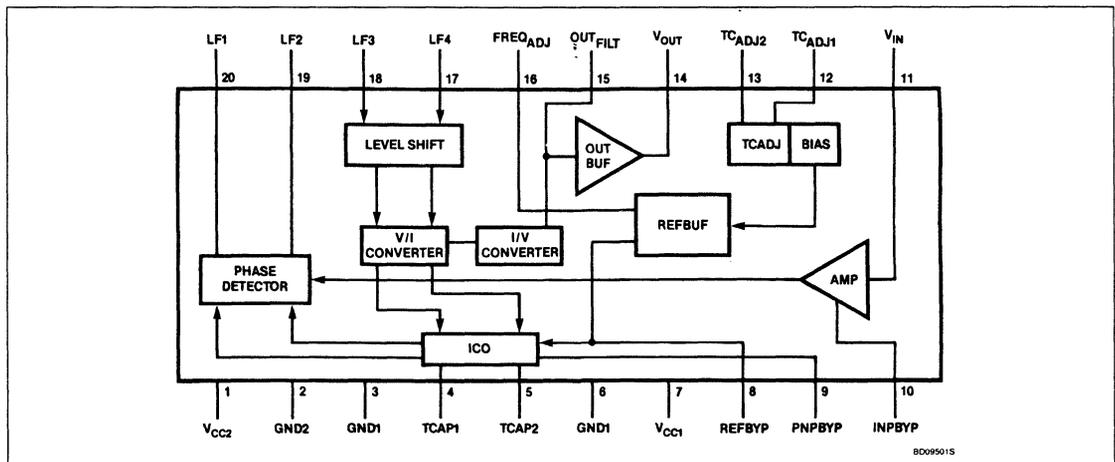
150MHz Phase-Locked Loop   NE568

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	6	V
T_A	Operating free-air ambient temperature range	0 to +70	°C
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
P_{DMAX}	Maximum power dissipation	500	mW

ELECTRICAL CHARACTERISTICS

The electrical characteristics listed below are actual tests (unless otherwise stated) performed on each device with an automatic IC tester prior to shipment. Performance of the device in automated test setup is not necessarily optimum. The NE568 is layout-sensitive. Evaluation of performance for correlation to the data sheet should be done with the circuit and layout of Figures 1 – 3 with the evaluation unit soldered in place. (Do not use a socket!)

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$, $f_O = 70MHz$, Test Circuit Figure 1, $f_{IN} = -20dBm$, $R_4 = 0\Omega$ (ground), unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{CC}	Supply current			60	75	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{OSC}	Maximum oscillator operating frequency[3]		150			MHz
	Input signal level		50 −20[1]		2000 +10	mV$_{P-P}$ dBm
BW	Demodulated bandwidth			f_O/7		MHz
	Non-linearity[5]	Dev = ± 20%, Input = −20dBm		1.0	4.0	%
	Lock range[2]	Input = −20dBm	± 25	± 35		% of f_O
	Capture range[2]	Input = −20dBm	± 20	± 30		% of f_O
	TC of f_O	Figure 1		100		ppm/°C
R_{IN}	Input resistance[4]		1			kΩ
	Output impedance			6		Ω
	Demodulated V_{OUT}	Dev = ± 20% of f_O measured at Pin 14	0.40	0.52		V$_{P-P}$
	AM rejection	$V_{IN} = -20dBm$ (30% AM) referred to ± 20% deviation		50		dB
f_O	Distribution[6]	Centered at 70MHz, $R_2 = 1.2k\Omega$, $C_2 = 17pF$, $R_4 = 0\Omega$ ($C_2 + C_{STRAY} = 20pF$)	−15	0	+15	%
f_O	Drift with supply	4.75V to 5.25V		1		%/V

NOTES:
1. Signal level to assure all published parameters. Device will continue to function at lower levels with varying performance.
2. Limits are set symmetrical to f_O. Actual characteristics may have asymmetry beyond the specified limits.
3. Not 100% tested, but guaranteed by design.
4. Input impedance depends on package and layout capacitance. See Figures 4 and 5.
5. Linearity is tested with incremental changes in input frequency and measurement of the DC output voltage at Pin 14 (V_{OUT}). Nonlinearity is then calculated from a straight line over the deviation range specified.
6. Free-running frequency is measured as feedthrough to Pin 14 (V_{OUT}) with no input signal applied.

# 150MHz Phase-Locked Loop   NE568
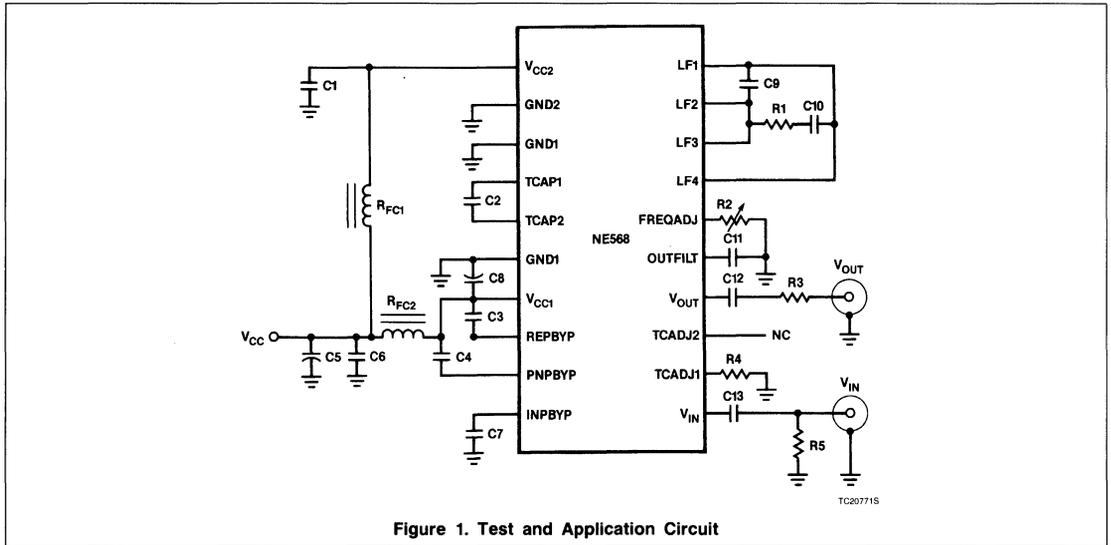
Figure 1. Test and Application Circuit

FUNCTIONAL DESCRIPTION

The NE568 is a high-performance phase-locked loop (PLL). The circuit consists of conventional PLL elements, with special circuitry for linearized demodulated output, and high-frequency performance. The process used has NPN transistors with $f_T > 6GHz$. The high gain and bandwidth of these transistors make careful attention to layout and bypass critical for optimum performance. The performance of the PLL cannot be evaluated independent of the layout. The use of the application layout in this data sheet and surface-mount capacitors are highly recommended as a starting point.

The input to the PLL is through a limiting amplifier with a gain of 200. The input of this amplifier is differential (Pins 10 and 11). For single-ended applications, the input must be coupled through a DC-blocking capacitor with low impedance at the frequency of interest. The single-ended input is normally applied to Pin 11 with Pin 10 AC-bypassed with a low-impedance capacitor. The input impedance is characteristically slightly above 500Ω. Impedance match is not necessary, but loading the signal source should be avoided. When the source is 50 or 75Ω, a DC-blocking capacitor is usually all that is needed.

Input amplification is low enough to assure reasonable response time in the case of large signals, but high enough for good AM rejection. After amplification, the input signal drives one port of a multiplier-cell phase detector. The other port is driven by the current-controlled oscillator (ICO). The output of the phase comparator is a voltage proportional to the phase difference of the input and

ICO signals. The error signal is filtered with a low-pass filter to provide a DC-correction voltage, and this voltage is converted to a current which is applied to the ICO, shifting the frequency in the direction which causes the input and ICO to have a 90° phase relationship.

The oscillator is a current-controlled multivibrator. The current control affects the charge/discharge rate of the timing capacitor. It is common for this type of oscillator to be referred to as a voltage-controlled oscillator (VCO), because the output of the phase comparator and the loop filter is a voltage. To control the frequency of an integrated ICO multivibrator, the control signal must be conditioned by a voltage-to-current converter. In the NE568, special circuitry predistorts the control signal to make the change in frequency a linear function over a large control-voltage range.

The free-running frequency of the oscillator depends on the value of the timing capacitor connected between Pins 4 and 5. The value of the timing capacitor depends on internal resistive components and current sources. When $R_2 = 1.2k\Omega$ and $R_4 = 0\Omega$, a very close approximation of the correct capacitor value is:

$$C^* = \frac{0.0014}{f_O} \, F$$

where

$$C^* = C_2 + C_{STRAY}.$$

The temperature-compensation resistor, R_4, affects the actual value of capacitance. This equation is normalized to 70MHz. See Figure 6 for correction factors.

The loop filter determines the dynamic characteristics of the loop. In most PLLs, the phase detector outputs are internally connected to the ICO inputs. The NE568 was designed with filter output to input connections from Pins 20 (ϕ DET) to 17 (ICO), and Pins 19 (ϕ DET) to 18 (ICO) external. This allows the use of both series and shunt loop-filter elements. The loop constants are:

$K_D = 0.127V/Radian$ (Phase Detector Constant)

$K_O = 4.2 \times 10^9 \, \dfrac{Radians}{V\text{-}sec}$ (ICO Constant)

The loop filter determines the general characteristics of the loop. Capacitors C_9, C_{10}, and resistor R_1, control the transient output of the phase detector. Capacitor C_9 suppresses 70MHz feedthrough by interaction with 100Ω load resistors internal to the phase detector.

$$C_9 = \frac{1}{2\pi \, (50)(f_O)} \, F$$

At 70MHz, the calculated value is 45pF. Empirical results with the test and application board were improved when a 56pF capacitor was used.

The natural frequency for the loop filter is set by C_{10} and R_1. If the center frequency of the loop is 70MHz and the full demodulated bandwidth is desired, i.e., $f_{BW} = f_O/7 = 10MHz$, and a value for R_1 is chosen, the value of C_{10} can be calculated.

$$C_{10} = \frac{1}{2\pi \, R_1 f_{BW}} \, F$$

150MHz Phase-Locked Loop   NE568

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568D

C_1	100nF	± 10%	Ceramic chip	1206
$C_2{}^1$	18pF	± 2%	Ceramic chip	0805
$C_2{}^2$	34pF	± 2%	Ceramic OR chip	
C_3	100nF	± 10%	Ceramic chip	1206
C_4	100nF	± 10%	Ceramic chip	1206
C_5	6.8μF	± 10%	Tantalum	35V
C_6	100nF	± 10%	Ceramic chip	1206
C_7	100nF	± 10%	Ceramic chip	1206
C_8	100nF	± 10%	Ceramic chip	1206
C_9	56pF	± 2%	Ceramic chip	0805 or 1206
C_{10}	560pF	± 2%	Ceramic chip	0805 or 1206
C_{11}	47pF	± 2%	Ceramic chip	0805 or 1206
C_{12}	100nF	± 10%	Ceramic chip	1206
C_{13}	100nF	± 10%	Ceramic chip	1206
R_1	27Ω	± 10%	Chip	1/8W
R_2	1.2kΩ		Trim pot	1/8W
$R_3{}^3$	43Ω	± 10%	Chip	1/8W
$R_4{}^4$	4.7kΩ	± 10%	Chip	1/8W
$R_5{}^3$	50Ω	± 10%	Chip	1/8W
$RFC_1{}^5$	10μH	± 10%	Surface mount	
$RFC_2{}^5$	10μH	± 10%	Surface mount	

NOTES:
1. $C_2 + C_{STRAY} = 20pF$.
2. $C_2 + C_{STRAY} = 36pF$ for temperature-compensated configuration with $R_4 = 4.7k\Omega$.
3. $R_3 = 62\Omega$, $R_5 = 75\Omega$ for 75Ω application.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 18pF$.
5. 0Ω chip resistors (jumpers) may be substituted with minor degradation of performance.

For the test circuit, R_1 was chosen to be 27Ω. The calculated value of C_{10} is 590pF; 560pF was chosen as a production value. (In actual satellite receiver applications, improved video with low carrier/noise has been observed with a wider loop-filter bandwidth.)

A typical application of the NE568 is demodulation of FM signals. In this mode of operation, a second single-pole filter is available at Pin 15 to minimize high frequency feed-through to the output. The roll-off frequency is set by an internal resistor of 350Ω ± 20%, and an external capacitor from Pin 15 to ground. The value of the capacitor is:

$$C11 = \frac{1}{2\pi \, (350)f_{BW}} \text{ F}$$

Two final components complete the active part of the circuitry. A resistor from Pin 12 to ground sets the temperature stability of the circuit, and a potentiometer from Pin 16 to ground permits fine tuning of the free-running oscillator frequency. The Pin 16 potentiometer is normally 1.2kΩ. Adjusting this resistance controls current sources which affect the charge and discharge rates of the timing capacitor and, thus, the frequency. The value of the temperature stability resistor is chosen from the graph in Figure 6; the respective timing capacitor needs to be changed.

The final consideration is bypass capacitors for the supply lines. The capacitors should be ceramic chips, preferably surface-mount types. They must be kept very close to the device. The capacitors from Pins 8 and 9 return to V_{CC1} before being bypassed with a separate capacitor to ground. This assures that no differential loops are created which might cause instability. The layouts for the test circuits are recommended.


a. Component Side Top of Board   b. Back of Board

NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent. Mount on bottom (back) of board. Add stand-off in each corner.
2. Back and top side ground must be connected at 8 point minimum.

Figure 2
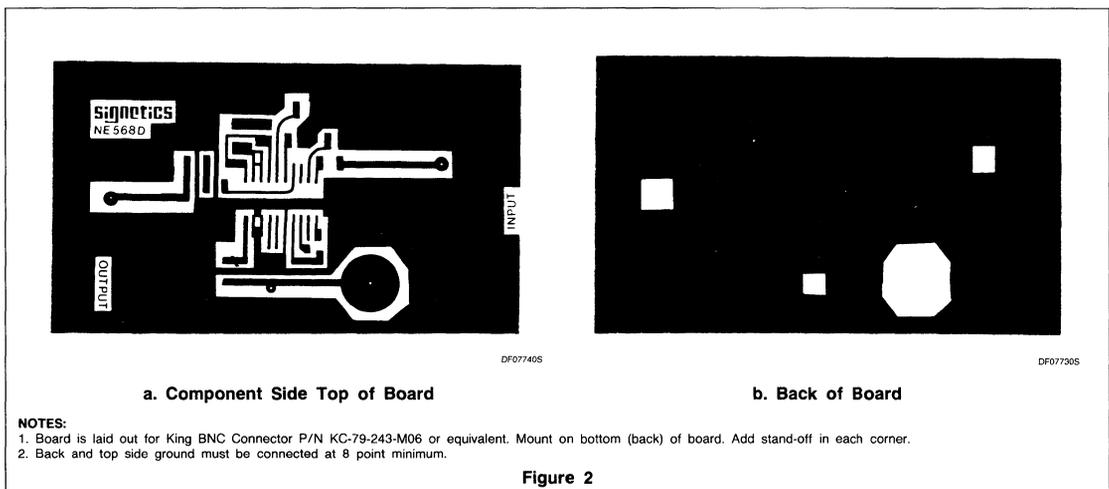
150MHz Phase-Locked Loop

NE568

PARTS LIST AND LAYOUT 70MHz APPLICATION NE568N

C_1	100nF	±10%	Ceramic chip	50V
C_2[1]	17pF	±2%	Ceramic OR chip	50V
C_2[2]	34pF	±2%	Ceramic chip	0805
C_3	100nF	±10%	Ceramic chip	50V
C_4	100nF	±10%	Ceramic chip	50V
C_5	6.8μF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic OR chip	50V
C_7	100nF	±10%	Ceramic chip	50V
C_8	100nF	±10%	Ceramic chip	50V
C_9	56pF	±2%	Ceramic chip	50V
C_{10}	560pF	±2%	Ceramic chip	50V
C_{11}	47pF	±2%	Ceramic OR chip	50V
C_{12}	100nF	±10%	Ceramic OR chip	50V
C_{13}	100nF	±10%	Ceramic OR chip	50V
R_1	27Ω	±10%	Carbon	¼W
R_2	1.2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Carbon	¼W
R_4[4]	4.7kΩ	±10%	Carbon	¼W
R_5[3]	50Ω	±10%	Carbon	¼W
RFC_1	10μH	±10%		
RFC_2	10μH	±10%		

NOTES:
1. $C_2 + C_{STRAY} = 20pF$ for test configuration with $R_4 = 0Ω$.
2. $C_2 = 34pF$ for temperature-compensated configuration with $R_4 = 4.7kΩ$.
3. For 50Ω setup. $R_1 = 62Ω$; $R_3 = 75Ω$ for 75Ω applications.
4. For test configuration $R_4 = 0Ω$ (GND) and $C_2 = 17pF$.

DF07750S

DF07760S

a. Component Side for Leaded Components   **b. Solder Side of Board and Chip Capacitors**

NOTES:
1. Board is laid out for King BNC Connector P/N KC-79-243-M06 or equivalent mounted on the component side of the board.
2. Component side and solder side ground planes must be connected at 8 points minimum.
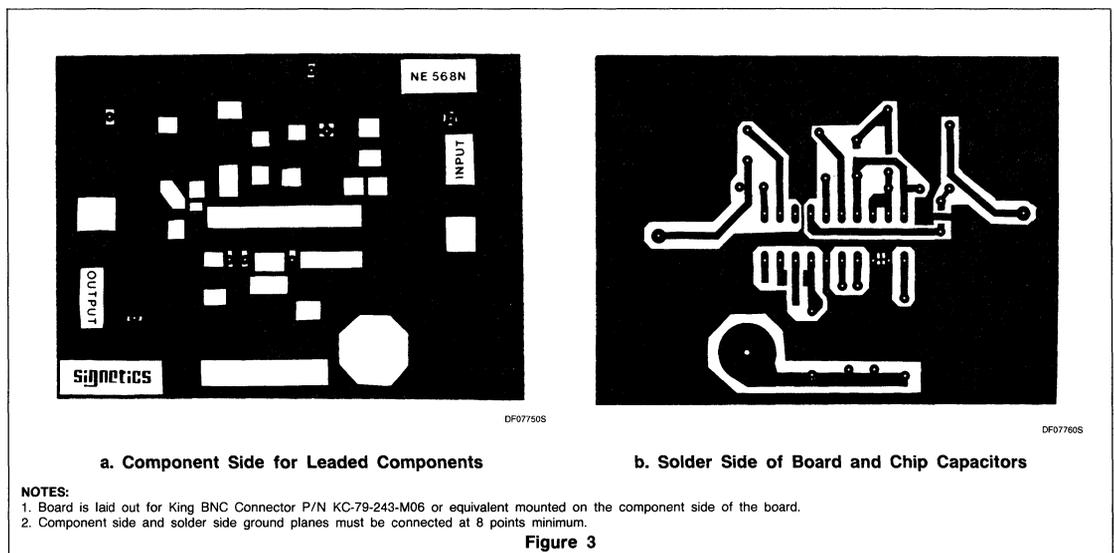
Figure 3

150MHz Phase-Locked Loop
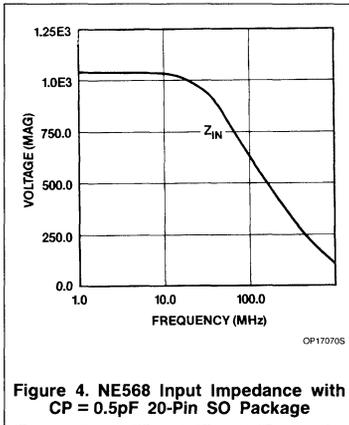
NE568

Figure 4. NE568 Input Impedance with CP = 0.5pF 20-Pin SO Package
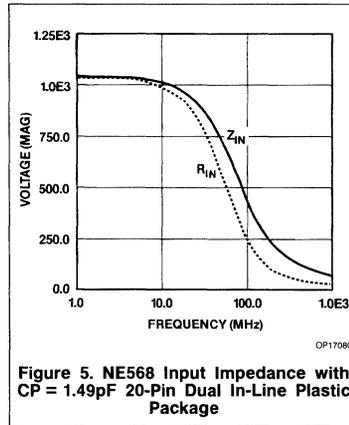
Figure 5. NE568 Input Impedance with CP = 1.49pF 20-Pin Dual In-Line Plastic Package
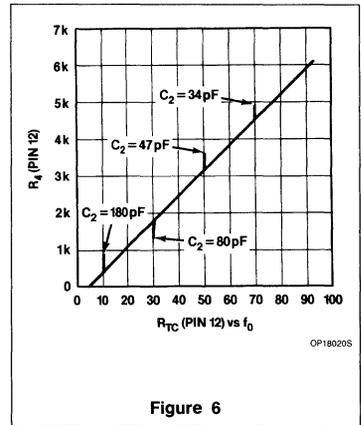
Figure 6
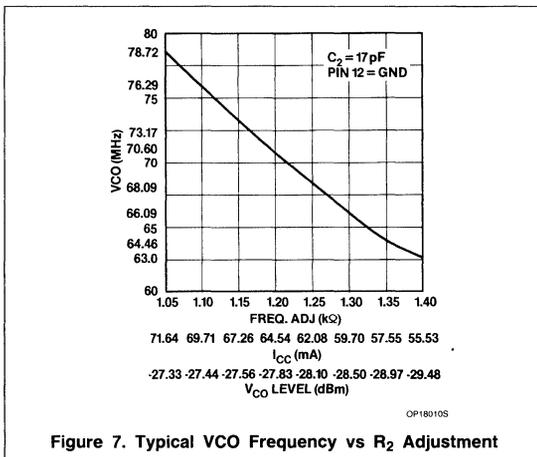
Figure 7. Typical VCO Frequency vs R_2 Adjustment
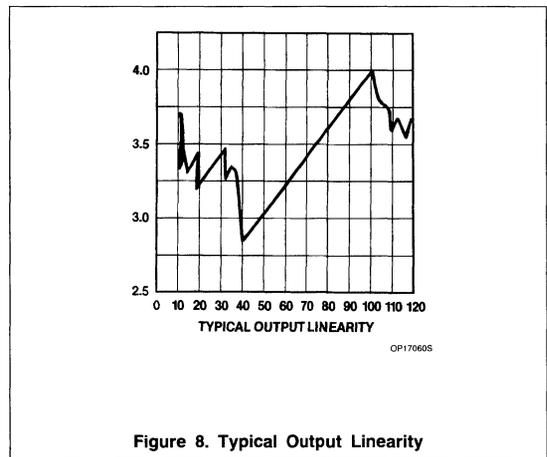
Figure 8. Typical Output Linearity

Signetics

Linear Products

Section 5
Analog Video
Transmission

INDEX

Signetics

AN1434
A Phase Locked Fiber Optic System Using FM Modulation

Application Note

Linear Products

Author: L. Hadley

SYSTEM OPERATION SUMMARY

The purpose of the fiber link is to transmit broadband video and sound over moderate distances (2.5km) with existing low cost components and minimal complexity.

Figure 1 depicts a complete system implementation. The application makes use of a very wideband VCO to generate an FM modulated carrier at 28.6MHz followed by a fast TTL LED driver to emit saturated 850nm light signals for entry into the glass fiber. A PIN diode receiver is coupled to a 140MHz bandwidth transimpedance preamplifier for increasing the detected signal amplitude and then fed to a phase-locked loop demodulator for recovering the original modulation signals.

The wideband FM sound subcarrier (150kHz deviation) is summed with baseband video at 10.7MHz and transmitted at a reduced level relative to the 3.58MHz color reference signal. Cross modulation between sound and picture information is minimized in this way. FM demodulation of the sound subcarrier is accomplished after passing through an IF gain block by a quadrature-type phase discriminator. The present sound circuit does not automatically frequency-lock to the transmitted subcarrier, but is fixed-tuned to 10.7MHz. A tracking PLL sound demodulator could be used to eliminate drift problems between transmitted sound subcarrier and the receiver in future designs.

SYSTEM DESCRIPTION AND OPERATION

Transmitter Unit: Video Channel

The transmitter circuit consists of a wideband differential amplifier (NE592), a VCO (NE564) and an LED driver, the NE522 high speed comparator. (See Figure 2) The video signal is AC coupled into the modulator preamplifier and fol-

lowed by a sync tip clamp to provide DC restoration of the composite video signal and to prevent variation of modulation deviation with varying picture content. (A complete video clamp and sync processor may be designed using the TDA9045 and TDA2595 combination.[1] This particular application is not tested at the time of this publication.)

A video signal level of 250 to 300mV peak is required to maintain optimum picture modulation. Since there is no AGC circuit in this particular design, this is a critical parameter and must be controlled to prevent overmodulation and picture degradation. Addition of an AGC using the above-mentioned parts would be a definite improvement for varying input level video. Using the present limited design, however, -10dB of attenuation was used with a 1V peak NTSC signal source at 75Ω. This is the common level available from most standard video signal systems.

Frequency compensation (pre-emphasis) is inserted in the form of a passive RC lead network at the Pin 14 input to the NE592 differential amplifier. This compensates for degenerative frequency distortion and provides better color balance in transmission.

The main FM modulator consists of an NE564 used only as a linear wideband VCO. The other sections of the device are not used. Differential DC coupling to the VCO terminals is attained via the loop filter terminals, Pins 4 and 5. The NE564 VCO is designed as a differential current-controlled balanced multivibrator. It possesses an extremely linear transfer function as illustrated in Figure 3. The graph shows how the VCO frequency varies with applied DC voltage across Pins 4 and 5. The VCO center frequency is determined by value of the capacitance across Pins 12 and 13. In this particular example, the transmitter

and receiver VCO are set to 28.6MHz. The slope of the VCO transfer function is termed K_O and is measured in radians per second per volt or simply Hertz per volt. Thus, to obtain the magnitude of the differential voltage for a given frequency deviation the relationship below is used:

$$V_{D(Volts\,DC)} = \frac{\Delta f}{k_O}\frac{MHz}{MHz/V}$$

$$I_{B2} = Constant$$

K_O is dependent upon the control bias generator current at Pin 2 as is noted from the graph. Higher current into Pin 2 results in a higher conversion gain, K_O. For a center frequency of 1MHz and an 800μA bias current into Pin 2, K_O is 1.7MHz/V across Pins 4 and 5 (V_D).

The value of K_O also increases linearly with center frequency so that at 30MHz K_O becomes 30 X 1.7 or 51MHz/V. Note that in this application the bias current is set at 320μA; that is the device is sinking current into Pin 2. This lowers K_O below the given value for 800μA shown on the graph in Figure 3 and requires a higher number of V/MHz to modulate the VCO. The signal to the VCO is DC coupled from the differential output of the NE592 in order to preserve bandwidth and to maintain proper biasing relative to the NE564.

In order to calculate the approximate frequency deviation, a linear relationship between ΔK_O and ΔI_{B2} is assumed. Estimating K_O at a Pin 2 bias of 320μA as opposed to 800μA is carried out with the following relationship:

$$k_O = \left|\frac{(1.7 - 0.95)\times 320}{2\times 800} + 0.95\right|$$

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Composite Video

0V

Input

Video Amplifier (NE592)

28.6MHz Wideband FM Modulator (NE564)

Bandpass Filter

Optical Modulator (NE522)

+V

CQF24

Alternate

74F3040 (1/2)

Sync Tip DC Clamp

10.7MHz Sound Sub Carrier FM Modulator (NE564)

NE575 Compressor 2:1

Video Input

Audio Input

Optical Interface Fiber

+V

BPF24

Fiber Input 850nM

Trans-Impedance Amp (NE5212)

28.6MHz PLL Demodula-tor (NE564)

Gain = 4 Buffer Amp (NE5539)

Video

75Ω Output

Band Pass Filter 10.7MHz

10.7MHz Sound IF Detector (NE604A)

Carrier Det. LED

Audio Amplifier TDA1521

L

Speaker

R

DC Volume Control

+V

Tone Control

Balance Control

Figure 1.   Video Fiber Transmission System

A Phase Locked Fiber Optic System Using FM Modulation

Figure 2a. LED Driver

*Note: An alternate LED driver which uses the 74F3040 line driver was incorporated in this particular application example. The 74F3040 has a higher current rating, but not the variable threshold capabilities of the NE522. The LED diode is operated in the saturated on-off mode for best signal to noise.

Figure 2. Fiber Optic Transmitter Block Diagram

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- ≈ 1.1MHz / V @ 1 MHz
- ≈ 33MHz / V @ 30 MHz

The measured differential voltage between Pins 4 and 5 for normal operating signal levels and standard NTSC color bars transmitted, is 80mV$_{P-P}$. The estimated total deviation is then 1.3MHz. This results in a video channel bandwidth for the 3.58MHz color signal of approximately:

- ≈ 2(1.3 + 3.58) MHz
- ≈ 9.8 MHz

This is rather a small deviation for wideband video transmission. The decision was made to use the 2nd harmonic of the fundamental VCO frequency to obtain twice the deviation. The VCO modulator is then set at an I_B of 320μA which provides sufficient 2nd harmonic content for this to operate successfully. This is shown in Figure 5 with the fundamental at 14.3MHz with the middle spectral plot showing required 28.6MHz carrier harmonic with improved deviation ratio. Pin 2 bias is set at approximately 320μA. The NE564 supply voltage is 5.00V.

Total FM Signal Bandwidth

For a total video bandwidth of 4.2MHz the transmission bandwidth is:
BW = 2X2(1.3 + 4.2) = 22MHz

Note that a bandpass filter could be installed in the signal path between the NE592 preamp/buffer to reduce noise bandwidth, but improvement was not tried. Adequate signal space for the baseband video and the 10.7MHz subcarrier would be 11MHz. Filter characteristics must provide good differential gain and phase response.

A second bandpass filter may be added in the path between the modulator and the LED driver stage with 22MHz bandwidth. This would improve the overall video signal-to-noise ratio.

The NE592 is biased with +5V and -1.8V to achieve the critical dynamic swing to properly slew the VCO over the required range without sacrificing faithful waveform reproduction in the transformation to linear FM modulation. Video signals contain both very low and high frequencies which are transient and phase

Figure 3. NE564 VCO Transfer Function- K$_o$
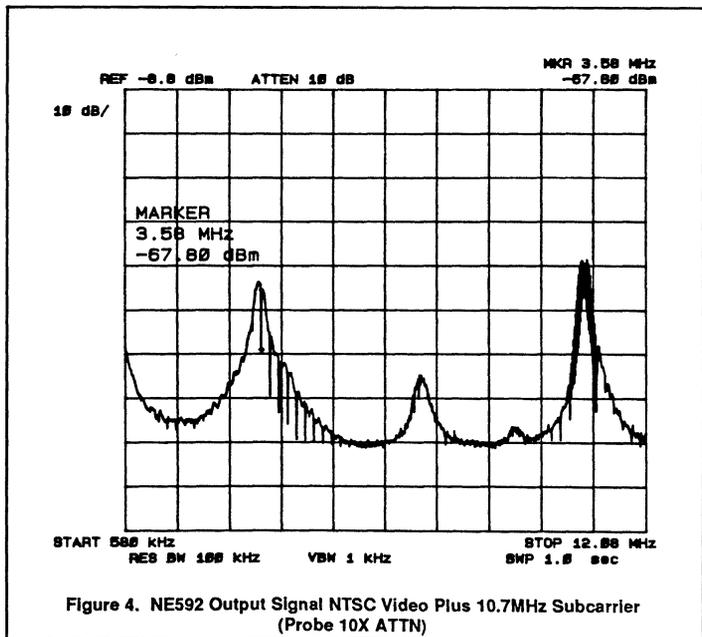
Figure 4. NE592 Output Signal NTSC Video Plus 10.7MHz Subcarrier
(Probe 10X ATTN)

A Phase Locked Fiber Optic System Using FM Modulation   AN1434

REF −8.8 dBm   ATTEN 18 dB

MKR 28.64 MHz
−29.66 dBm

18 dB/

MARKER
28 64 MHz
−29 60 dB

START 8.72 MHz
RES BW 300 kHz   VBW 100 kHz

STOP 48.72 MHz
SWP 28 msec

Figure 5. Transmitter PLL Output with NTSC Color Bar Test Pattern Input (Input video -10dB attenuation below 1V peak)(10X FET Probe at Pin 9 NE564)

REF −8.8 dBm   ATTEN 18 dB

MKR 28.64 MHz
−33.78 dBm

18 dB/

SWEEPTIME
150 msec

START 23.02 MHz
RFR BW 100 kHz   VBW 300 kHz

STOP 35.02 MHz
RWP 150 msec

Figure 6. Transmitter LED Drive Spectrum with 10.7MHz Sound Subcarrier and NTSC Video Test Signal Input (10X ATTN)

sensitive. The unused input pins to the phase detector, Pins 6 and 7, are tied together with a 1kΩ resistor and Pin 7 bypassed to ground. Pin 3 is grounded.

The 28.6MHz FM signal from the NE564 is taken from the Pin 9 open collector VCO output port which requires a 470Ω pull-up resistor to 5V. A 100Ω resistor is added to Pin 11 to improve the fall time of the output waveform. The signal is then fed into the NE522(74F3040) high speed comparator where a threshold level is set up on the inverting terminal to provide duty cycle adjustment and noise threshold. The NE522 has an open collector output which lends itself easily to driving the LED transmitter diode (CQF24); the 74F3040 has a source-sink output stage which requires that the LED be connected as shown in Figure 1A.

The CQF24 generates 850nm optical energy with a typical rise and fall time of 10ns. It is rated at 250mW dissipation and 100mA continuous current.

Spectral frequency plots taken under normal operating conditions with NTSC color bar signal input for the sections of the transmitter described above appear in Figures 4 through 6.
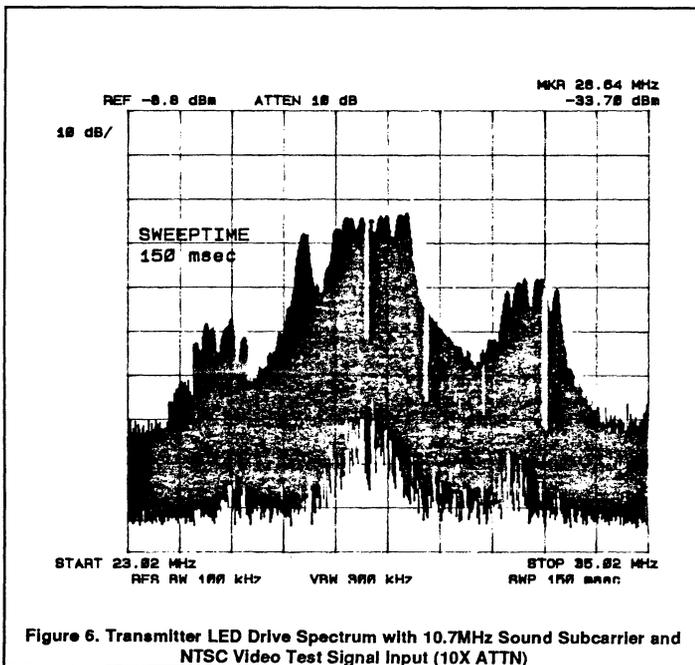
The Sound Channel
As shown in the block diagram in Figure 2, audio input is fed through a 2:1 compressor which consists of the NE575 low voltage compandor. This device compresses all audio signals according to the transfer function shown in Figure 7. It is required to limit the peak FM deviation for the 10.7MHz VCO to ±75kHz for 0dBV input (1V_{IN} 600Ω RMS). Audio compression also improves intelligibility in systems with limited signal-to-noise ratio. This device, NE575, operates at unity gain for an input level of 100mV_{RMS} audio input which is 0dB for the NE575. The 2:1 compression factor refers to the AC signal level in dB above or below 100mV_{RMS}.[2] Output from the NE575 is fed to the second NE564 modulator with a VCO center frequency set at 10.7MHz. Refer to Figure 8 for typical circuit diagram. The 10.7MHz subcarrier is fed to the NE592 for summing with the main baseband video signal. The level of the sound subcarrier is adjusted to a level

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20dB below the 3.58MHz color video sideband (28.6MHz signal) by adjustment of the output level potentiometer at the emitter follower, Q1. (See Figure 9.) This can be accomplished most easily by monitoring the combined 28.6MHz signal from the main modulator (Pin 9, NE564) using a spectrum analyzer. The 10.7MHz carrier deviation is adjusted using 0dBm (775mV$_{RMS}$ into 600Ω) input to the compressor at 1kHz and adjusting the deviation with the input potentiometer, R7, which feeds the NE564 (see Figure 9 for the 10.7MHz schematic) . Figure 10 displays the proper frequency deviation spectrum as set by the R7 adjustment. A 0dBm (775mV) input to the compressor is 18dB above the compandor 100mV reference level and the compressor will reduce this +18dB input level to approximately 280mV$_{RMS}$ at the NE575 output on Pin 14. The pot, R7, provides the calibration adjustment for maximum 10.7MHz deviation.

The actual 10.7MHz level to the 30MHz modulator is set by pot R8 and is adjusted by monitoring the spectral level at the output, Pin 9 , of the NE564 with a sprectum analyzer. The relative sound carrier (lower 28.6MHz sideband) is set approximately 20dB below the 3.58MHz color reference signal. This is accomplished by first noting the sideband level of the video information (Figure 5), removing the video modulation and setting the 10.7MHz level with R8 on the sound modulator board.

THE RECEIVER UNIT

Light energy from the fiber optic cable is fed to the BPF24 PIN diode and transformed to a small current typically in the 1 to 5μA range. This photodiode current carries all of the FM carrier information in the signal bandwidth of approximatey 22MHz centered at 28.6MHz. The photocurrent is now amplified and transformed into a differential signal voltage by the NE5212 transimpedance amplifier (Pin 1 input). In this particular application, however, the output is not used differentially, but a single-ended signal is taken from Pin 5 of the NE5212 and AC coupled to Pin 6 of the NE564.

The NE5212 has a differential transresistance of 14k. This translates to 14mV/μA of input current, yielding 35mV of dif-

Figure 7. NE575 Compressor Transfer Function
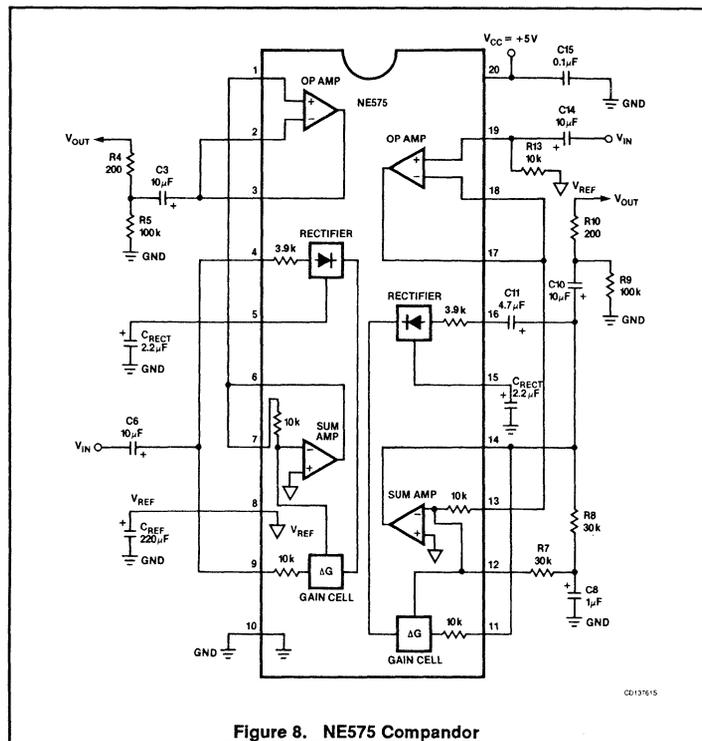
Figure 8. NE575 Compandor
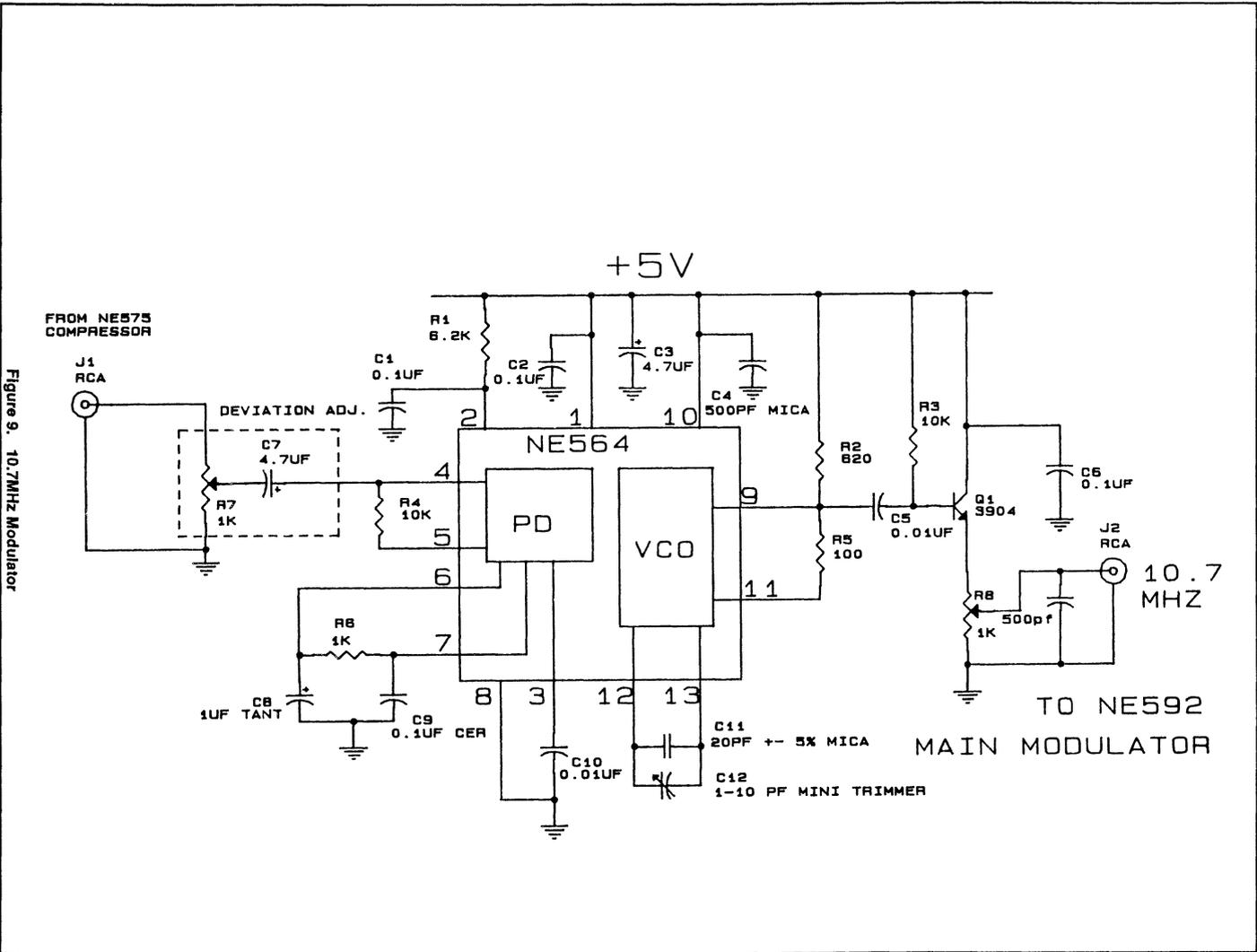
Figure 9.   10.7MHz Modulator

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ferential output voltage for 2.5μA input current. Since the device is used single ended, only half, or 17.5mV, output is available to drive the phase detector of the NE564. (See Figure 12 for actual output signal from NE5212) The low signal level (about 1mV) input to the PLL makes it necessary to run the gain-setting bias at a higher level than usual; this, in addition to the wide bandwidth requirements, results in a bias current of 2.2mA sinking into Pin 2 of the NE564. Another modification to the nominal NE564 operating conditions is the choice of a higher supply voltage on the phase detector portion of the device (+ 8V on Pin 1) to increase the linearity and dynamic range for fast video signals. The VCO section is supplied from +8V through a 200Ω dropping resistor and operates on 4.5V at Pin 10. (Note that the absolute maximum voltages for the phase detector and VCO are 14 and 6V, respectively.)

VCO Frequency Adjustment

The NE564 receiver PLL is operated at the same frequency as the 2nd harmonic of the transmitter fundamental, 28.6MHz. Prior to making any adjust-
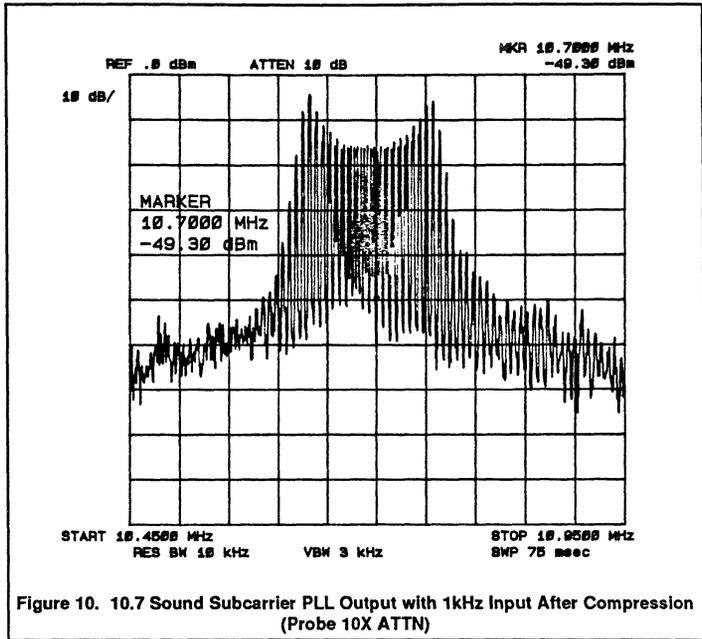
Figure 10. 10.7 Sound Subcarrier PLL Output with 1kHz Input After Compression (Probe 10X ATTN)
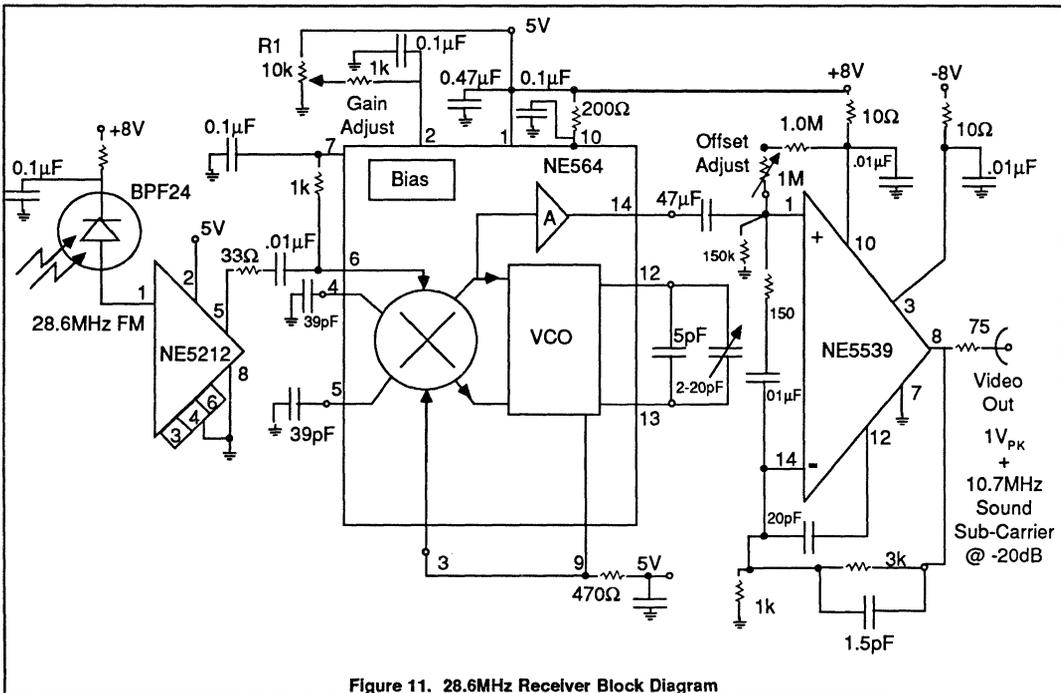
Figure 11. 28.6MHz Receiver Block Diagram

Figure 12. Receiver NE5212 Output at 28.6MHz with NTSC Color Bars and 5km Optical Attenuation (Probe 10X ATTN)

Figure 13. Receiver PLL Spectrum Frequency with No Signal from Fiber (Probe 10X ATTN)
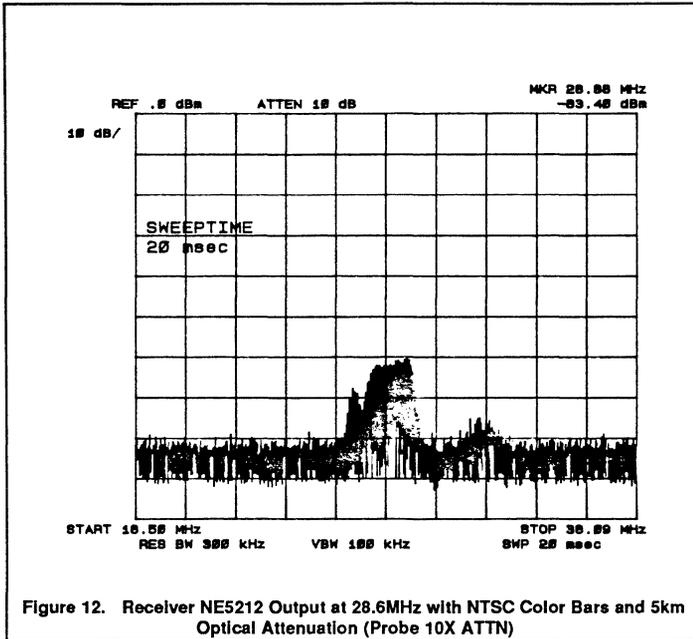
ments, the bias current to Pin 2 is set to 2.2mA. The spectrum of the receiver VCO without a fiber link signal, fiber disconnected, is shown in Figure 13. When making the initial center frequency adjustment to the VCO trimmer cap (NE564 Pin 12, 13, 2-20pF), the fiber cable is disconnected. (Note that a thermal stabilization time of 1 hour is recommended prior to any transmitter or receiver calibration adjustments).

With the link connected and a proper signal present at the input to the NE564 Pin 6, the PLL will lock onto and track the incoming wideband FM signal. (See Figure 14 for VCO spectrum.) Note that the unwanted harmonic signals, number one and three, have not been filtered out in this application example.

The demodulated baseband video plus 10.7MHz signal then appears on the analog output port, Pin 14. A wideband amplifier with low differential gain and phase error (NE5539) is used to boost the combined signal with the composite video level raised to 1V peak into 75Ω. The actual measured value of the video using an NTSC color bar signal is $1V_{p-p}$ on the output port. The NE564 output to the NE5539 from Pin 14 is 250 mV_{p-p}.
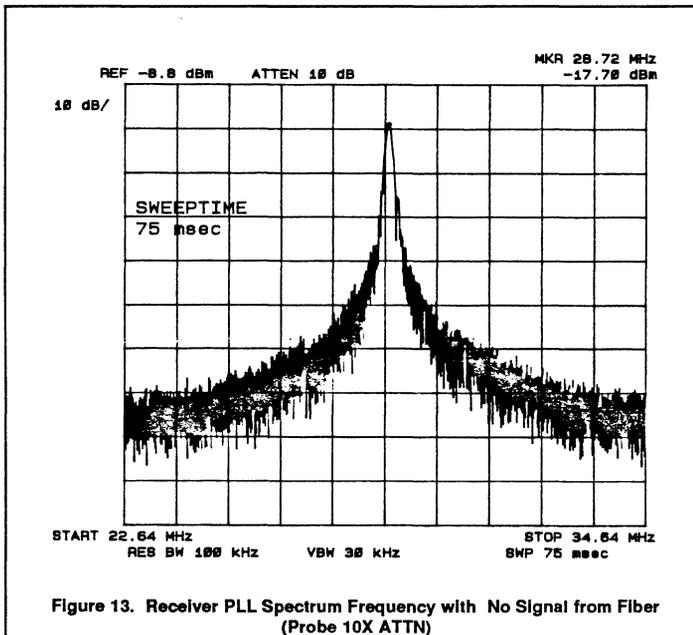
Figure 15 shows the composite baseband video plus 10.7MHz subcarrier spectrum.

The final stage of the video channel is the NE5539 which drives directly into the video monitor. Biasing the DC offset of the post amplifier is necessary to prevent sync distortion and optimum video response. This is accomplished by adjusting R2 (1MΩ pot on Pin 1 of NE5539) for 0V average at the output. Note that a lead-lag network is connected across Pins 1 and 14 to stabilize the op amp which has a closed loop bandwidth of approximately 100MHz for a closed loop gain of 4. This excessive bandwidth creates noise in the picture information and is reduced by the 20pF capacitor from Pin 12 to 14.   (See Figure 11.)

Sound Channel Operation and Adjustment
A portion of the output signal from the

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NE5539 is also sent to the NE604A to be amplified and demodulated (see Figure 16). The composite signal contains both the video and the 10.7MHz subcarrier. A ceramic 10.7MHz bandpass filter is used before the NE604A to remove all but the subcarrier. The NE604A contains a high gain IF amplifier and an LC quadrature detector for demodulating the FM sound information.

Adjustment of the sound channel is carried out after the system has been on for an hour to allow thermal stabilization. A 1kHz test signal is injected into the audio input port of the NE575 compressor board and set to $775mV_{RMS}$ terminated in 600Ω. Using a spectrum analyzer, adjust R7 while observing the 10.7MHz output on a spectrum analyzer and set the deviation for 150kHz maximum. At this point make sure that the 10.7MHz VCO (NE564) is on frequency, and make any trim adjustments to the VCO trim capacitor. Finally, adjust R8 for a carrier amplitude by monitoring the output of the transmitter VCO lower sideband, and set the 10.7MHz signal 20dB below the 3.58MHz sideband relative to 28.6MHz. The last adjustment is the setting of the quadrature coil on the NE604A demodulator for maximum sound with the best signal to noise. (Refer to Figure 17 for the input signal spectrum to the NE604A).

CONCLUSION
The system example described is capable of demonstrating single channel color video and sound transmission over 850nm glass or plastic fiber optic cable of ≥2.5km. Signal transmission is of adequate quality for industrial inspection, security, and other applications of this limited nature. The most notable feature is its minimal cost. It is not meant to be used in broadcast quality environments. The user is invited to make improvements and alterations to the system to attain greater stability and higher quality. The audio amplifier and control section shown in Figure 1 is not included in this applications note. For further detail on the audio portion and applications examples, please refer to Section 7 of the Signetics Linear Data Manual, Volume 1, *Communications*.

Suggested areas of improvement are 1.

Figure 14. 28.6MHz Receiver PLL VCO Spectrum with Link Phase-Locked and 5km Optical Attenuation (Probe 10X ATTN)


Figure 15. NE5539 Postamplifier Spectrum Baseband Video and 10.7MHz Subcarrier (Probe 10X ATTN)
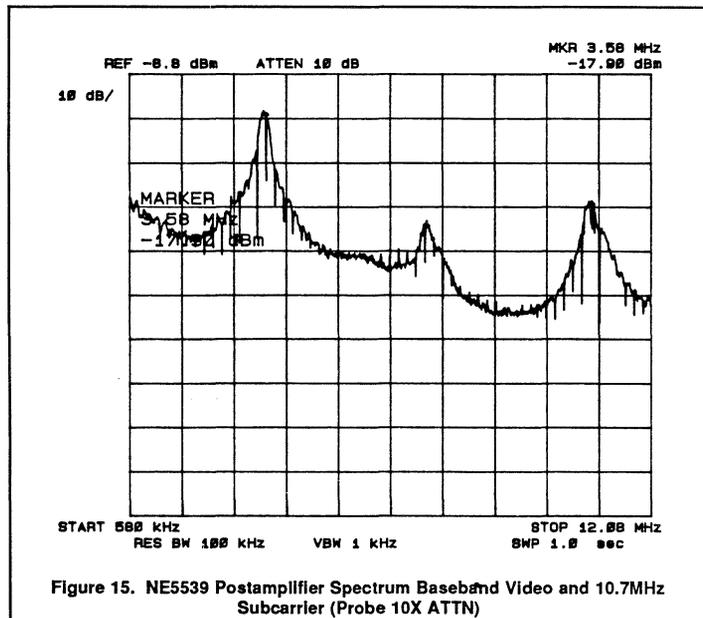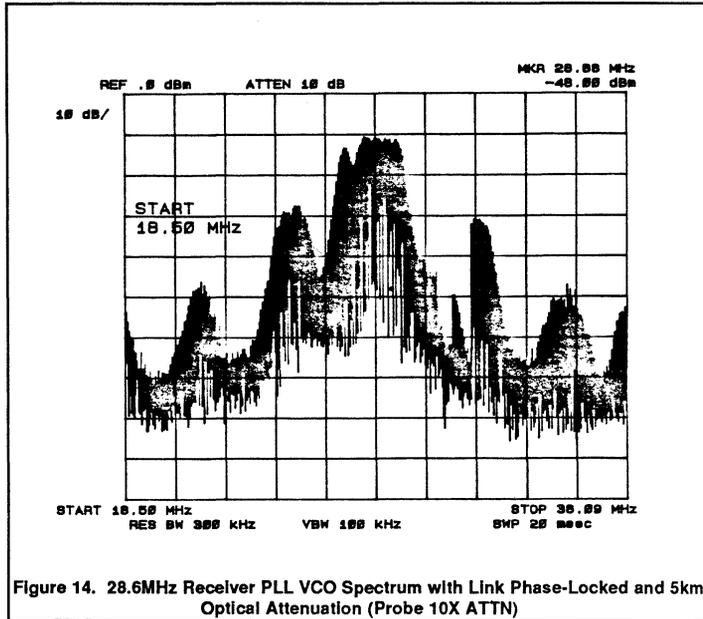
# A Phase Locked Fiber Optic System Using FM Modulation   AN1434
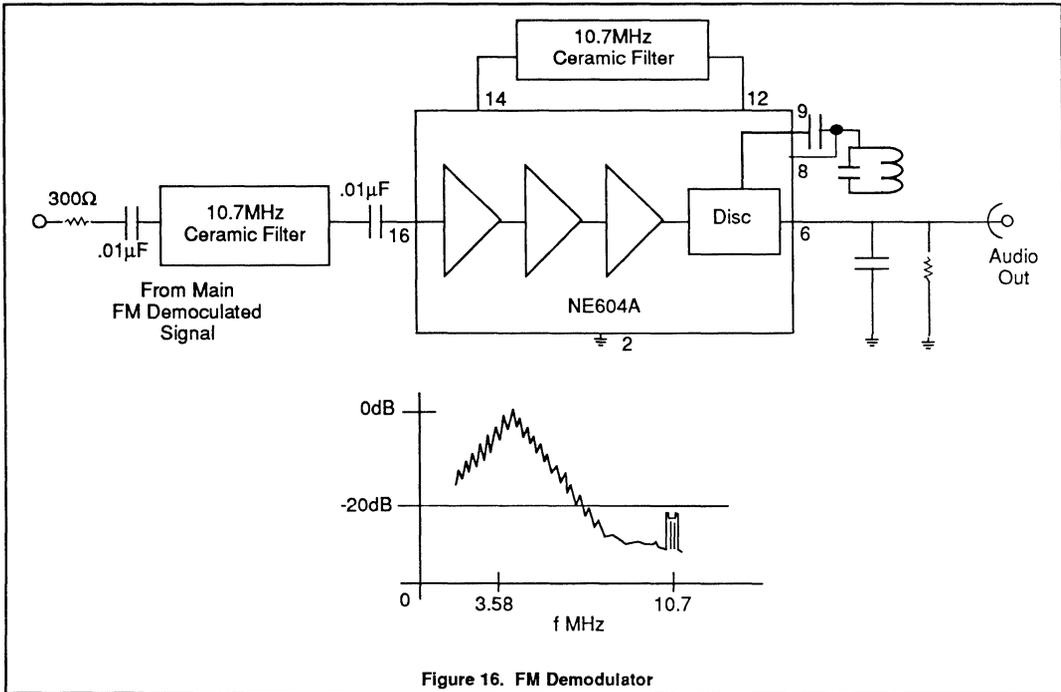
Figure 16. FM Demodulator

The addition of bandpass filters to improve transmitter and receiver signal-to-noise, 2. Video sync tip or black level clamp with AGC at transmitter modulation input, 3. Addition of an AGC stage after the receiver transimpedance amplifier to improve optical path dynamic range.

Power Supply Requirements
The regulated voltages required to operate the system are as follows:

+ 5.00V
- 5.00V
+ 8.00V
- 8.00V

Test Equipment
1. HP8568B Spectrum Analyzer
2. Tektronix PC6202 FET Probe 10X
3. Philips 5510 Color Generator

Footnotes
1. Signetics Linear Data Manual, Volume 1, Communications, 1987.
2. *Ibid.*
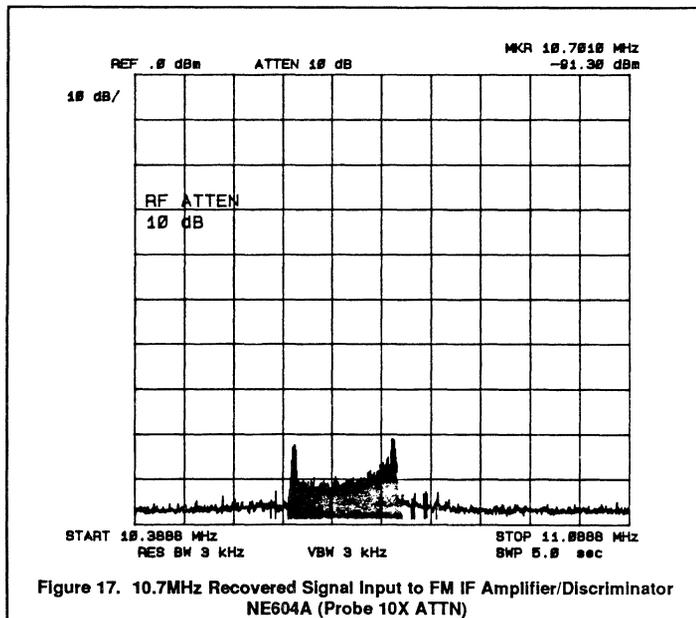
Figure 17. 10.7MHz Recovered Signal Input to FM IF Amplifier/Discriminator NE604A (Probe 10X ATTN)

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Roden, Martin S., *Analog and Digital Communications Systems*, 2nd Edition; Prentice Hall, 1985.

Signetics, *Linear Data Manual, Volume 1, Communications,* 1987.
1. AN140: Compensation Techniques for Use with the NE/SE5539
2. AN175: Automatic Level Control: NE572
3. AN176: Compandor Cookbook
4. AN179: Circuit Description of the NE564
5. AN1991: Audio Decibel Level Detector with Meter Drive (NE604)

Signetics, *Linear Data Manual, Volume 3, Communications,* 1987.

AN146:   Wideband FM Composite Video Fiber Optic Link, Signetics 1985

Signetics

NE/SE522
High-Speed Dual-Differential Comparator/Sense Amp

Product Specification

Linear Products

FEATURES
- 15ns maximum guaranteed propagation delay
- 20μA maximum input bias current
- TTL-compatible strobes and outputs
- Large common-mode input voltage range
- Operates from standard supply voltages

APPLICATIONS
- MOS memory sense amp
- A-to-D conversion
- High-speed line receiver

PIN CONFIGURATION

D, F, N Packages

INPUT 1A	1	14 V-
INPUT 1B	2	13 V
NC	3	12 INPUT 2A
OUTPUT 1Y	4	11 INPUT 2B
STROBE 1G	5	10 NC
STROBE S	6	9 OUTPUT 2Y
GROUND	7	8 STROBE 2G

Top View

BLOCK DIAGRAM

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Cerdip	0 to 70°C	NE522F
14-Pin Cerdip	−55°C to 125°C	SE522F
14-Pin Plastic DIP	0 to +70°C	NE522N
14-Pin Plastic SO	0 to 70°C	NE522D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V+ V−	Supply voltage Positive Negative	 +7 −7	V
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage Common-mode Strobe/gate	 ±5 +5.25	V
P_D	Power dissipation	600	mW
T_A	Operating temperature range NE522 SE522	0 to 70 −55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C
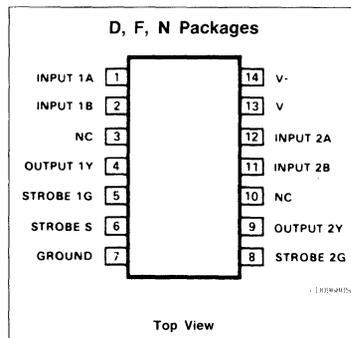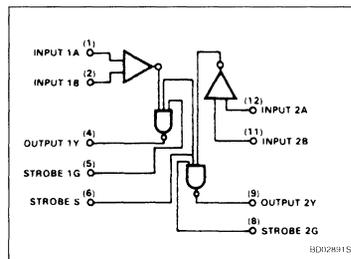
High-Speed Dual-Differential Comparator/Sense Amp

NE/SE522

EQUIVALENT SCHEMATIC
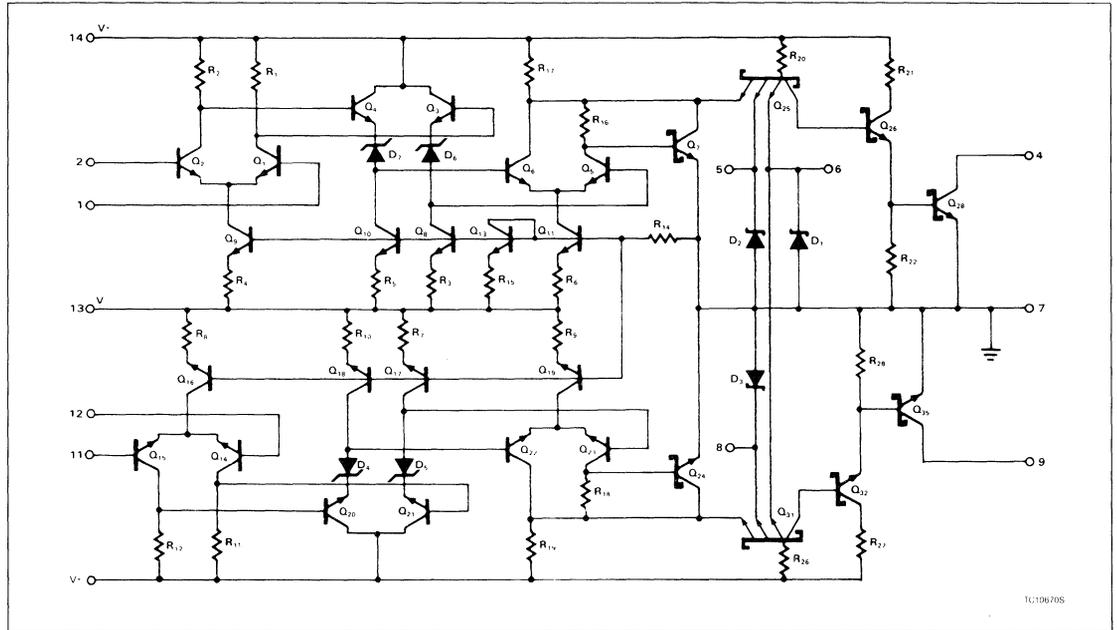
High-Speed Dual-Differential Comparator/Sense Amp   NE/SE522

DC ELECTRICAL CHARACTERISTICS (SE522)±5V ± 10%, $T_A = -55$ to +125°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage At 25°C Over temperature range	V+ = + 4.5V, V− = −4.5V		6	7.5 15	mV
I_{BIAS}	Input bias current At 25°C Over temperature range	V+ = + 5.5V, V− = −5.5V		7.5	20 40	μA
I_{OS}	Input offset current At 25°C Over temperature range	V+ = + 5.5V, V− = −5.5V		1.0	5 12	μA
V_{CM}	Common-mode voltage range	V+ = + 4.5V, V− = −4.5V	± 3			V
V_{IL}	Low level input Voltage at 25°C Over temperature				0.8 0.7	V
V_{IH}	High level temperature		2.0			V
I_{IH}	Input current High	V+ = + 5.5V, V− = −5.5V V_{IH} = 2.7V 1G or 2G strobe Common strobe S			50 100	μA μA
I_{IL}	Low input current	V_{IL} = 0.5V 1G 2G strobe Common strobe S			−2 −4	mA mA
V_{OL}	Output voltage Low	V+ = + 4.5V, V− = −4.5V I_{OL} = 20mA, T_A = 25°C I_{OL} = 10mA			0.5 0.5	V
I_{OH}	Output current High	V_{CC+} = + 4.5, V_{CC-} = −4.5V, V_{OH} = 5.5V			250	μA
V+ V−	Supply voltage Positive Negative		4.5 −4.5	5.0 −5.0	5.5 −5.5	V
I_{CC+} I_{CC-}	Supply current Positive Negative	V+ = 5.5V, V− = −5.5V, T_A = 25°C		27 −15	35 −28	mA

High-Speed Dual-Differential Comparator/Sense Amp

NE/SE522

DC ELECTRICAL CHARACTERISTICS (NE522)± 5V ± 5%, T_A = 0 to +70°C, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage At 25°C Over temperature range	V+ = +4.75V, V− = −4.75V		6	7.5 10	mV
I_{BIAS}	Input bias current At 25°C Over temperature range	V+ = +5.25V, V− = −5.25V		7.5	20 40	μA
I_{OS}	Input offset current At 25°C Over temperature range	V+ = +5.25V, V− = −5.25V		1.0	5 12	μA
V_{CM}	Common-mode voltage range	V+ = +4.75V, V− = −4.75V	± 3			V
I_{IH}	Input current High	V+ = +5.25V, V− = −5.25V V_{IH} = 2.7V 1G or 2G strobe Common strobe S			50 100	μA μA
I_{IL}	Low	V_{IL} = 0.5V 1G 2G strobe Common strobe S			−2.0 −4.0	mA mA
V_{OL}	Output voltage low	V+ = +5.25V, V− = −5.25V, $V_{I(S)}$ = 2.0V I_{LOAD} = 20mA			0.5	V
I_{OH}	Output current high High	V_{CC+} = +4.75 $V_{CC−}$ = −4.75V, V_{OH} = 5.25V			250	μA
V+ V−	Supply Voltage Positive Negative		4.75 −4.75	5.0 −5.0	5.25 −5.25	V
I_{CC+} $I_{CC−}$	Supply current Positive Negative	V+ = 5.25V, V− = −5.25V, T_A = 25°C		27 −15	35 −28	mA

High-Speed Dual-Differential Comparator/Sense Amp

NE/SE522

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $R_L = 280\Omega$, $C_L = 15pF$

SYMBOL	PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
I_R	Input resistance				4		$k\Omega$
I_C	Input capacitance				3		pF
Large-signal switching speed							
$t_{PLH(D)}$	Propagation delay						
$t_{PHL(D)}$	Low to high[1]	Amp	Output		10	15	
$t_{PLH(S)}$	High to low[1]	Amp	Output		8	12	ns
$t_{PHL(S)}$	Low to high[2]	Strobe	Output		6	13	
	High to low[2]	Strobe	Output		5	9	
f_{MAX}	Maximum operating frequency			25	35		MHz

NOTES:
1. Response time measured from 0V point of $\pm 100mV_{P-P}$ 10MHz square wave to the 1.5V point of the output.
2. Response time measured from 1.5V point of the input to 1.5V point of the output.

LOGIC FUNCTION TABLE

V_{ID} (A^+, B^-)	STRS	STRG	Output Transistor
$< -V_{OS}$	H	H	ON
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined
$> V_{OS}$	H	H	OFF
X	L	X	OFF
X	X	L	OFF

High-Speed Dual-Differential Comparator/Sense Amp

NE/SE522

TYPICAL PERFORMANCE CHARACTERISTICS

Response Time for Various Input Overdrives
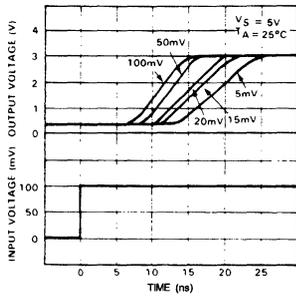
OP06701S

Response Time for Various Input Overdrives
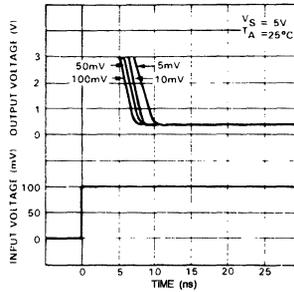
OP06711S

Response Time vs Temperature
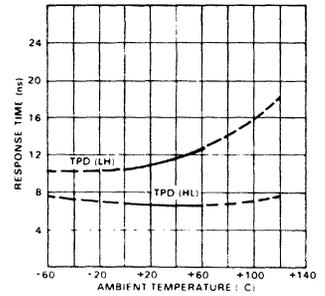

OP06721S

Propagation Delay for Various Input Voltages
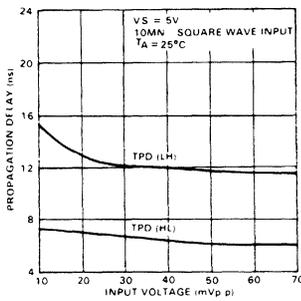

OP06731S

Propagation Delay for Various Input Voltages
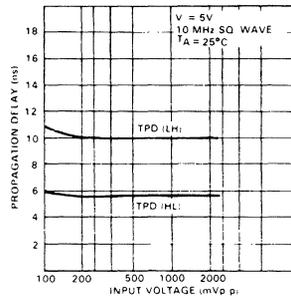
OP06741S

Input Bias Current vs Ambient Temperature
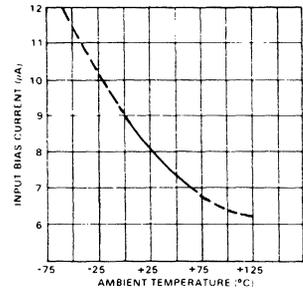
OP06751S

Input Offset Current vs Ambient Temperature
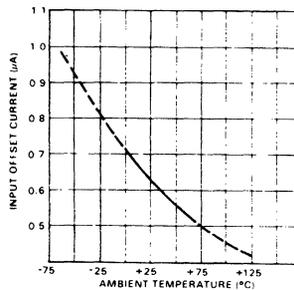
OP06761S

Signetics

NE/SA/SE592
Video Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE/SA/SE592 is a monolithic, two-stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high-pass, low-pass, or band-pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.
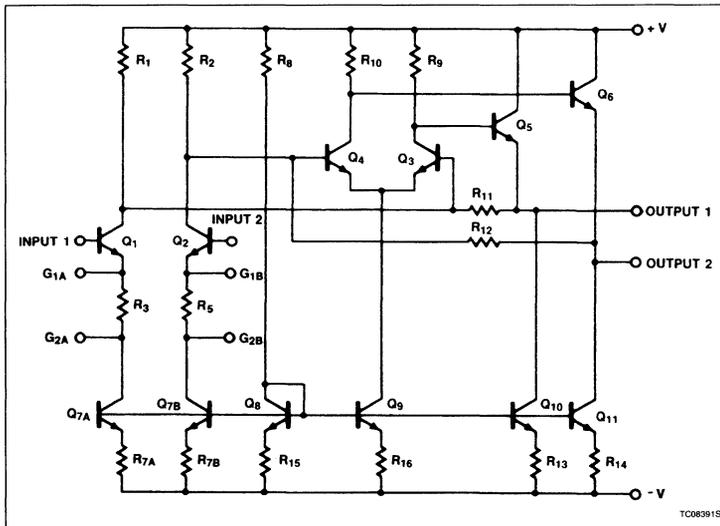
FEATURES

- **120MHz unity gain bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**
- **MIL-STD processing available**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

PIN CONFIGURATIONS

D, F, N Packages

INPUT 2	1	14 INPUT 1
NC	2	13 NC
G$_{2B}$ GAIN SELECT	3	12 G$_{2A}$ GAIN SELECT
G$_{1B}$ GAIN SELECT	4	11 G$_{1A}$ GAIN SELECT
V –	5	10 V +
NC	6	9 NC
OUTPUT 2	7	8 OUTPUT 1

TOP VIEW   CD09790S

H Package*

G$_{2A}$ GAIN SELECT

INPUT 1, G$_{1A}$ GAIN SELECT, INPUT 2, V +, G$_{2B}$ GAIN SELECT, OUTPUT 1, G$_{1B}$ GAIN SELECT, OUTPUT 2, V –
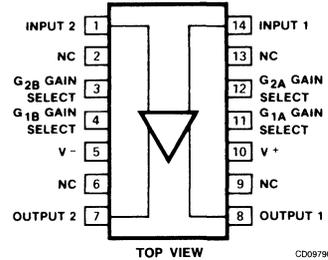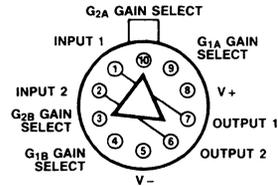
CD09800S

NOTES:
Pin 5 connected to case.
*Metal cans (H) not recommended for new designs.

D, F, N, Packages

INPUT 2	1	8 INPUT 1
G$_{1B}$ GAIN SELECT	2	7 G$_{1A}$ GAIN SELECT
V –	3	6 V +
OUTPUT 2	4	5 OUTPUT 1

TOP VIEW   CD09810S

EQUIVALENT CIRCUIT

TC08391S
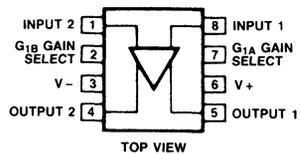
Video Amplifier

NE/SA/SE592

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE592N14
14-Pin Cerdip	0 to +70°C	NE592F14
14-Pin Cerdip	−55°C to +125°C	SE592F14
14-Pin SO	0 to +70°C	NE592D14
8-Pin Plastic DIP	0 to +70°C	NE592N8
8-Pin Cerdip	−55°C to +125°C	SE592F8
8-Pin Plastic DIP	−40°C to +85°C	SA592N8
8-Pin SO	0 to +70°C	NE592D8
8-Pin SO	−40°C to +85°C	SA592D8
10-Lead Metal Can	0 to +70°C	NE592H
10-Lead Metal Can	−55°C to +125°C	SE592H

NOTE:
N8, N14, D8 and D14 package parts also available in "High" gain version by adding "H" before package designation, i.e., NE592HD8.

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$, unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	±8	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Common-mode input voltage	±6	V
I_{OUT}	Output current	10	mA
T_A	Operating ambient temperature range SE592 NE592	 −40 to +85 0 to +70	 °C °C
T_{STG}	Storage temperature range	−65 to +150	°C
$P_{D\ MAX}$	Maximum power dissipation, $T_A = 25°C$ (still air)[1] F-14 package F-8 package D-14 package D-8 package H package N-14 package N-8 package	 1.17 0.79 0.98 0.79 0.83 1.44 1.17	 W W W W W W W

NOTE:
1. Derate above 25°C at the following rates:
   F-14 package at 9.3mW/°C
   F-8 package at 6.3mW/°C
   D-14 package at 7.8mW/°C
   D-8 package at 6.3mW/°C
   H package at 6.7mW/°C
   N-14 package at 11.5mW/°C
   N-8 package at 9.3mW/°C

Video Amplifier

NE/SA/SE592

DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

| SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P\text{-}P}$							
	Gain 1[1]		250	400	600	300	400	500	V/V
	Gain 2[2, 4]		80	100	120	90	100	110	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance								
	Gain 1[1]			4.0			4.0		$k\Omega$
	Gain 2[2, 4]		10	30		20	30		$k\Omega$
C_{IN}	Input capacitance[2]	Gain 2[4]		2.0			2.0		pF
I_{OS}	Input offset current			0.4	5.0		0.4	3.0	μA
I_{BIAS}	Input bias current			9.0	30		9.0	20	μA
V_{NOISE}	Input noise voltage	BW 1kHz to 10MHz		12			12		μV_{RMS}
V_{IN}	Input voltage range		± 1.0			± 1.0			V
CMRR	Common-mode rejection ratio								
	Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	60	86		60	86		dB
	Gain 2[4]	$V_{CM} \pm 1V$, $f = 5MHz$		60			60		dB
PSRR	Supply voltage rejection ratio								
	Gain 2[4]	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.0	V
	Gain 3[3]	$R_L = \infty$		0.35	0.75		0.35	0.75	V
V_{CM}	Output common-mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V
R_{OUT}	Output resistance			20			20		Ω
I_{CC}	Power supply current	$R_L = \infty$		18	24		18	24	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

Video Amplifier

NE/SA/SE592

DC ELECTRICAL CHARACTERISTICS

$V_{SS} = \pm 6V$, $V_{CM} = 0$, $0°C \leqslant T_A \leqslant 70°C$ for NE592; $-40°C \leqslant T_A \leqslant 85°C$ for SA592, $-55°C \leqslant T_A \leqslant 125°C$ for SE592, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Differential voltage gain, standard part	$R_L = 2k\Omega$, $V_{OUT} = 3V_{P-P}$							
	Gain 1[1]		250		600	200		600	V/V
	Gain 2[2, 4]		80		120	80		120	V/V
	High gain part		400	500	600				V/V
R_{IN}	Input resistance Gain 2[2, 4]		8.0			8.0			$k\Omega$
I_{OS}	Input offset current				6.0			5.0	μA
I_{BIAS}	Input bias current				40			40	μA
V_{IN}	Input voltage range		± 1.0			± 1.0			V
CMRR	Common-mode rejection ratio Gain 2[4]	$V_{CM} \pm 1V$, $f < 100kHz$	50			50			dB
PSRR	Supply voltage rejection ratio Gain 2[4]	$\Delta V_S = \pm 0.5V$	50			50			dB
V_{OS}	Output offset voltage								
	Gain 1	$R_L = \infty$			1.5			1.5	V
	Gain 2[4]	$R_L = \infty$			1.5			1.2	V
	Gain 3[3]	$R_L = \infty$			1.0			1.0	V
V_{OUT}	Output voltage swing differential	$R_L = 2k\Omega$	2.8			2.5			V
I_{CC}	Power supply current	$R_L = \infty$			27			27	mA

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

AC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$, unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

SYMBOL	PARAMETER	TEST CONDITIONS	NE/SA592			SE592			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth								
	Gain 1[1]			40			40		MHz
	Gain 2[2, 4]			90			90		MHz
t_R	Rise time	$V_{OUT} = 1V_{P-P}$							
	Gain 1[1]			10.5			10.5		ns
	Gain 2[2, 4]			4.5	12		4.5	10	ns
t_{PD}	Propagation delay	$V_{OUT} = 1V_{P-P}$							
	Gain 1[1]			7.5			7.5		ns
	Gain 2[2, 4]			6.0	10		6.0	10	ns

NOTES:
1. Gain select Pins G_{1A} and G_{1B} connected together.
2. Gain select Pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 10- and 14-pin versions only.

Video Amplifier   NE/SA/SE592

TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Rejection Ratio as a Function of Frequency
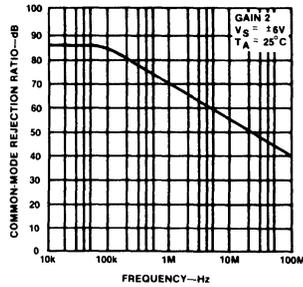
OP04421S

### Output Voltage Swing as a Function of Frequency
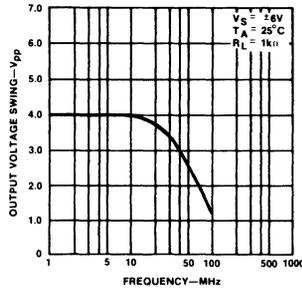

OP04430S
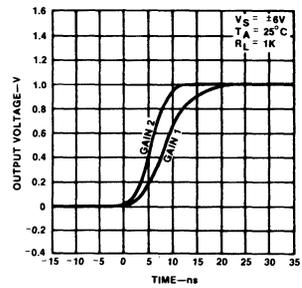
Pulse Response


OP04440S

Differential Overdrive Recovery Time
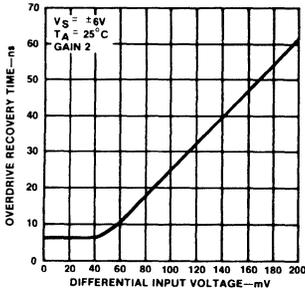
OP04450S

Pulse Response as a Function of Supply Voltage
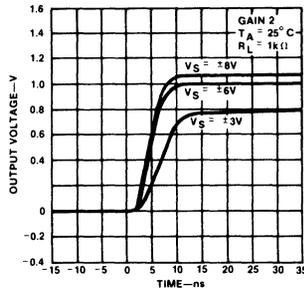

OP04460S

Pulse Response as a Function of Temperature
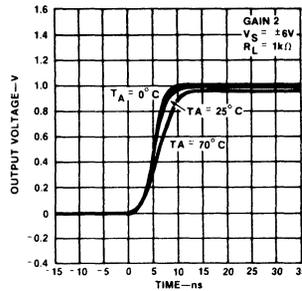
OP04470S

Voltage Gain as a Function of Temperature
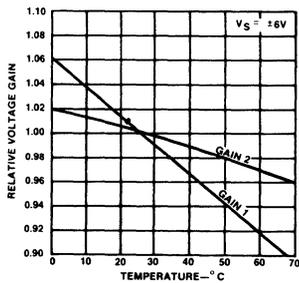
OP04480S
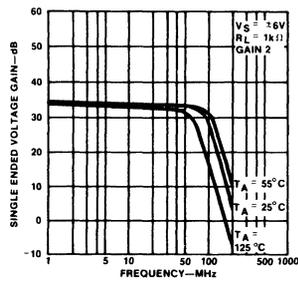
Gain vs Frequency as a Function of Temperature

OP04490S

Voltage Gain as a Function of Supply Voltage
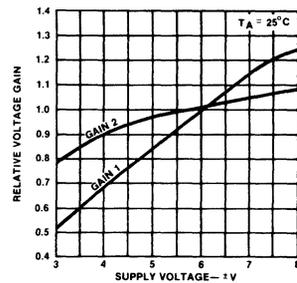
OP04500S

Video Amplifier

NE/SA/SE592

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Gain vs Frequency as a Function of Supply Voltage

OP04510S

Voltage Gain Adjust Circuit

$V_S = \pm 6V$ $T_A = 25°C$

OP04521S

Voltage Gain as a Function of RADJ (Figure 3)

OP04530S

Supply Current as a Function of Temperature

OP04540S

Supply Current as a Function of Supply Voltage

OP04550S

Output Voltage and Current Swing as a Function of Supply Voltage

OP04560S

Output Voltage Swing as a Function of Load Resistance

OP04570S

Input Resistance as a Function of Temperature

OP04580S

Input Noise Voltage as a Function of Source Resistance
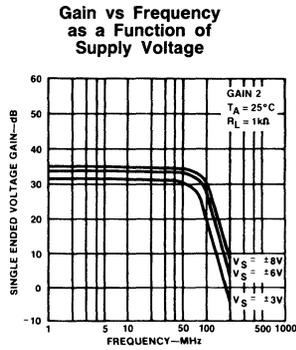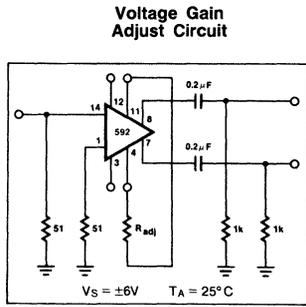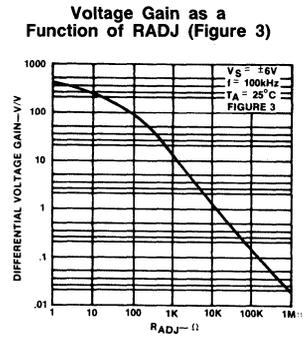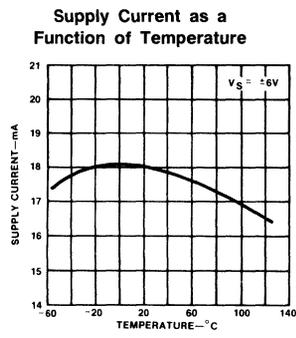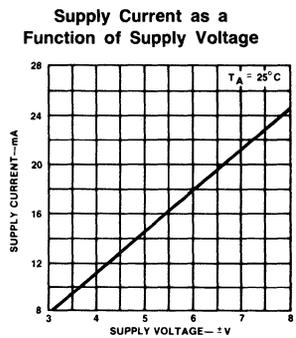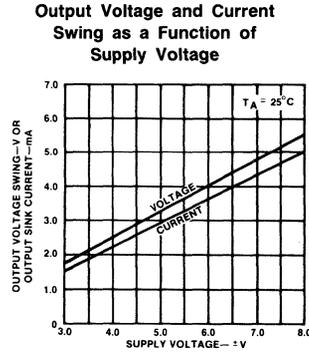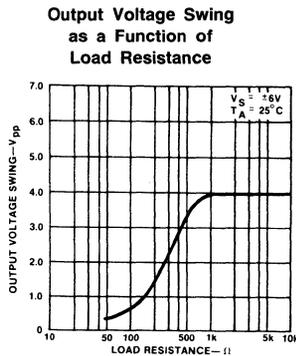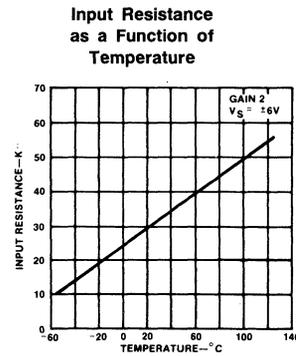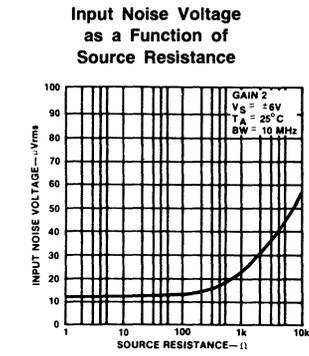
OP04590S

Video Amplifier

NE/SA/SE592

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Phase Shift as a Function of Frequency
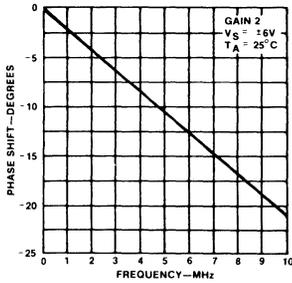
OP04600S

### Phase Shift as a Function of Frequency
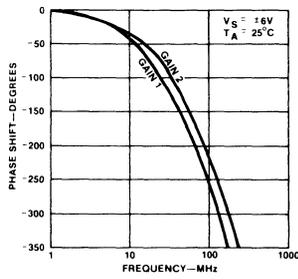
OP04610S

Voltage Gain as a Function of Frequency
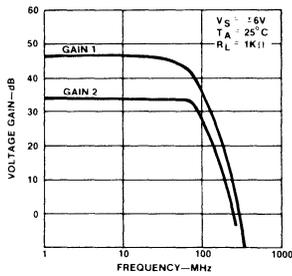
OP04620S

### Voltage Gain as a Function of Frequency (All Gain Select Pins Open)
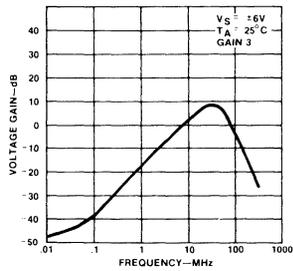
OP04630S

TEST CIRCUITS $T_A = 25°C$, unless otherwise specified.
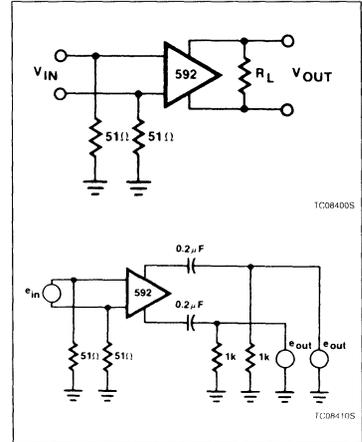
Video Amplifier

NE/SA/SE592

TYPICAL APPLICATIONS
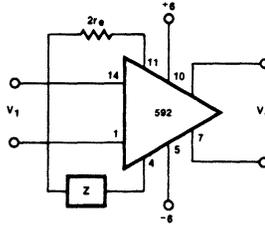
TC08420S

NOTE:

$$\frac{V_0(s)}{V_1(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

Basic Configuration
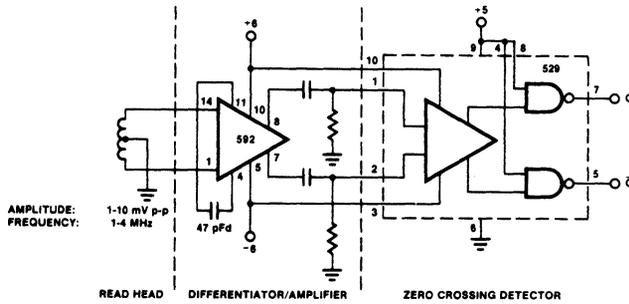
AMPLITUDE: 1-10 mV p-p
FREQUENCY: 1-4 MHz

READ HEAD   DIFFERENTIATOR/AMPLIFIER   ZERO CROSSING DETECTOR

TC08430S

Disc/Tape Phase-Modulated Readback Systems
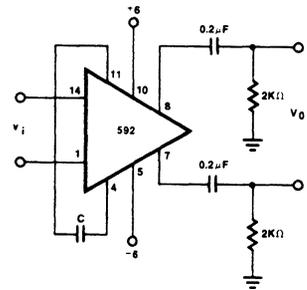
TC08440S

NOTE:
For frequency $F_1 << \frac{1}{2}\pi (32) C$

$$V_0 \cong 1.4 \times 10^4 C \frac{dVi}{dT}$$

**Differentiation with High
Common-Mode Noise Rejection**

Video Amplifier

NE/SA/SE592

FILTER NETWORKS

Z NETWORK	FILTER TYPE	V_0 (s) TRANSFER V_1 (s) FUNCTION
R — L (resistor, inductor in series)	LOW PASS	$\dfrac{1.4 \times 10^4}{L}\left[\dfrac{1}{s + R/L}\right]$
R — C (resistor, capacitor in series)	HIGH PASS	$\dfrac{1.4 \times 10^4}{R}\left[\dfrac{s}{s + 1/RC}\right]$
R — L — C (resistor, inductor, capacitor in series)	BAND PASS	$\dfrac{1.4 \times 10^4}{L}\left[\dfrac{s}{s^2 + R/L\,s + 1/LC}\right]$
R with L parallel C (band reject network)	BAND REJECT	$\dfrac{1.4 \times 10^4}{R}\left[\dfrac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$
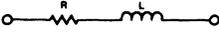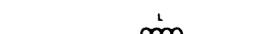
TC08422S

NOTES:
In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.
$S = j\omega$
$\omega = 2\pi f$

Signetics

Linear Products

NE/SA/SE5205
Wide-band High-Frequency Amplifier

Product Specification

DESCRIPTION
The NE/SA/SE5205 is a high-frequency amplifier with a fixed insertion gain of 20dB. The gain is flat to ±0.5dB from DC to 450MHz, and the −3dB bandwidth is greater than 600MHz in the EC package. This performance makes the amplifier ideal for cable TV applications. For lower frequency applications, the part is also available in industrial standard dual in-line and small outline packages. The NE/SA/SE5205 operates with a single supply of 6V, and only draws 24mA of supply current, which is much less than comparable hybrid parts. The noise figure is 4.8dB in a 75Ω system and 6dB in a 50Ω system.

Until now, most RF or high-frequency designers had to settle for discrete or hybrid solutions to their amplification problems. Most of these solutions required trade-offs that the designer had to accept in order to use high-frequency gain stages. These include high-power consumption, large component count, transformers, large packages with heat sinks, and high part cost. The NE/SA/SE5205 solves these problems by incorporating a wide-band amplifier on a single monolithic chip.

The part is well matched to 50 or 75Ω input and output impedances. The Standing Wave Ratios in 50 and 75Ω systems do not exceed 1.5 on either the input or output from DC to the −3dB bandwidth limit.

Since the part is a small monolithic IC die, problems such as stray capacitance are minimized. The die size is small enough to fit into a very cost-effective 8-pin small-outline (SO) package to further reduce parasitic effects. A TO-46 metal can is also available that has a case connection for RF grounding which increases the −3dB frequency to 600MHz. The Cerdip package is hermetically sealed, and can operate over the full −55°C to +125°C range.

No external components are needed other than AC coupling capacitors because the NE/SA/SE5205 is internally compensated and matched to 50 and 75Ω. The amplifier has very good distortion specifications, with second and third-order intermodulation intercepts of +24dBm and +17dBm respectively at 100MHz.

The device is ideally suited for 75Ω cable television applications such as decoder boxes, satellite receiver/decoders, and front-end amplifiers for TV receivers. It is also useful for amplified splitters and antenna amplifiers.

The part is matched well for 50Ω test equipment such as signal generators, oscilloscopes, frequency counters and all kinds of signal analyzers. Other applications at 50Ω include mobile radio, CB radio and data/video transmission in fiber optics, as well as broad-band LANs and telecom systems. A gain greater than 20dB can be achieved by cascading additional NE/SA/SE5205s in series as required, without any degradation in amplifier stability.

FEATURES
- **600MHz bandwidth**
- **20dB insertion gain**
- **4.8dB (6dB) noise figure**
  $Z_O = 75Ω$ ($Z_O = 50Ω$)
- **No external components required**
- **Input and output impedances matched to 50/75Ω systems**
- **Surface mount package available**
- **MIL-STD processing available**

APPLICATIONS
- **75Ω cable TV decoder boxes**
- **Antenna amplifiers**
- **Amplified splitters**
- **Signal generators**
- **Frequency counters**
- **Oscilloscopes**
- **Signal analyzers**
- **Broad-band LANs**
- **Fiber-optics**
- **Modems**
- **Mobile radio**
- **Security systems**
- **Telecommunications**

PIN CONFIGURATIONS

N, FE, D Packages

V_{CC} 1	8 V_{CC}
V_{IN} 2	7 V_{OUT}
GND 3	6 GND
GND 4	5 GND

20dB

TOP VIEW

CD12760S

EC Package

V_{OUT} (1)   (4) GND
V_{CC} (2)   (3) V_{IN}

20dB

CD09850S

NOTE:
Tab denotes Pin 1.
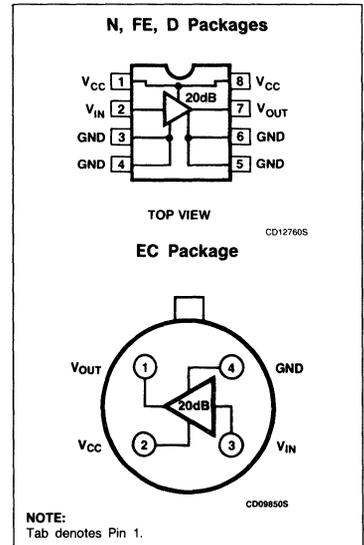
Wide-band High-Frequency Amplifier   NE/SA/SE5205

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5205D
4-Pin Metal can	0 to +70°C	NE5205EC
8-Pin Cerdip	0 to +70°C	NE5205FE
8-Pin Plastic DIP	0 to +70°C	NE5205N
8-Pin Plastic SO	−40°C to +85°C	SA5205D
8-Pin Plastic DIP	−40°C to +85°C	SA5205N
8-Pin Cerdip	−40°C to +85°C	SA5205FE
8-Pin Cerdip	−55°C to +125°C	SE5205FE
8-Pin Plastic DIP	−55°C to +125°C	SE5205N

EQUIVALENT SCHEMATIC

TC08490S
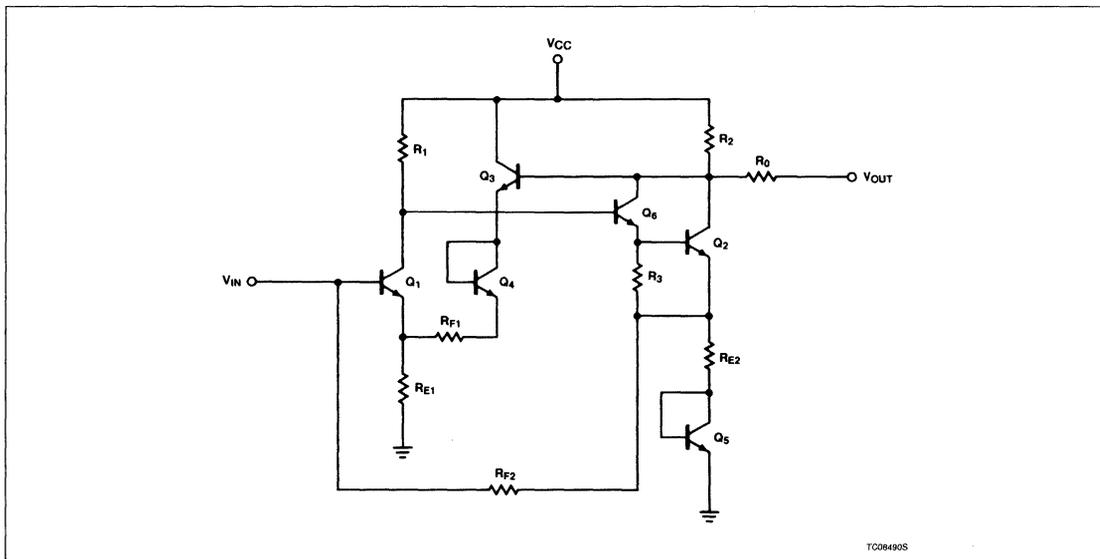
Wide-band High-Frequency Amplifier

NE/SA/SE5205

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	9	V
V_{AC}	AC input voltage	5	V_{P-P}
T_A	Operating ambient temperature range NE grade SA grade SE grade	0 to +70 −40 to +85 −55 to +125	°C °C °C
P_{DMAX}	Maximum power dissipation, $T_A = 25°C$ (still-air)[1, 2] FE package N package D package EC package	780 1160 780 1250	mW mW mW mW

NOTES:
1. Derate above 25°C, at the following rates:
   FE package at 6.2mW/°C
   N package at 9.3mW/°C
   D package at 6.2mW/°C
   EC package at 10.0mW/°C
2. See "Power Dissipation Considerations" section.

DC ELECTRICAL CHARACTERISTICS at $V_{CC} = 6V$, $Z_S = Z_L = Z_O = 50\Omega$ and $T_A = 25°C$, in all packages, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Operating supply voltage range	Over temperature	5 5		6.5 6.5	5 5		8 8	V V
I_{CC}	Supply current	Over temperature	20 19	24	30 31	20 19	24	30 31	mA mA
S21	Insertion gain	f = 100MHz Over temperature	17 16.5	19	21 21.5	17 16.5	19	21 21.5	dB
S11	Input return loss	f = 100MHz D, N, FE		25			25		dB
		DC − f_{MAX} D, N, FE	12			12			dB
S11	Input return loss	f = 100MHz EC package					24		dB
		DC − f_{MAX} EC				10			dB
S22	Output return loss	f = 100MHz D, N, FE		27			27		dB
		DC − f_{MAX}	12			12			dB
S22	Output return loss	f = 100MHz EC package					26		dB
		DC − F_{MAX}				10			dB
S12	Isolation	f = 100MHz		−25			−25		dB
		DC − f_{MAX}	−18			−18			dB
t_R	Rise time			5			5		ps
	Propagation delay			5			5		ps

Wide-band High-Frequency Amplifier

NE/SA/SE5205

DC ELECTRICAL CHARACTERISTICS at V_{CC} = 6V, Z_S = Z_L = Z_O = 50Ω and T_A = 25°C, in all packages, unless otherwise specified.

| SYMBOL	PARAMETER	TEST CONDITIONS	SE5205			NE/SA5205			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Bandwidth	± 0.5dB D, N					450		MHz
f_{MAX}	Bandwidth	± 0.5dB EC					500		MHz
f_{MAX}	Bandwidth	± 0.5dB FE		300			300		MHz
f_{MAX}	Bandwidth	−3dB D, N				550			MHz
f_{MAX}	Bandwidth	−3dB EC				600			MHz
f_{MAX}	Bandwidth	−3dB FE	400			400			MHz
	Noise figure (75Ω)	f = 100MHz		4.8			4.8		dB
	Noise figure (50Ω)	f = 100MHz		6.0			6.0		dB
	Saturated output power	f = 100MHz		+ 7.0			+ 7.0		dBm
	1dB gain compression	f = 100MHz		+ 4.0			+ 4.0		dBm
	Third-order intermodulation intercept (output)	f = 100MHz		+ 17			+ 17		dBm
	Second-order intermodulation intercept (output)	f = 100MHz		+ 24			+ 24		dBm
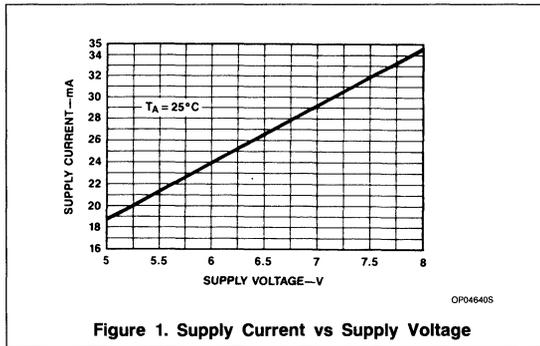
Figure 1. Supply Current vs Supply Voltage
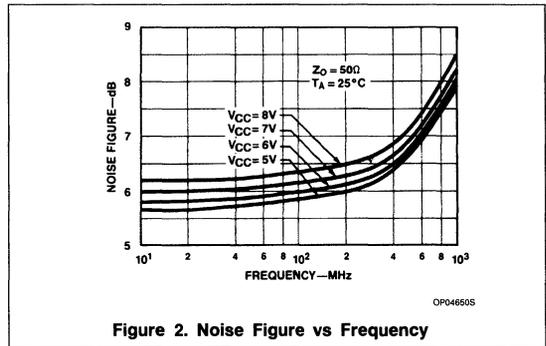
Figure 2. Noise Figure vs Frequency
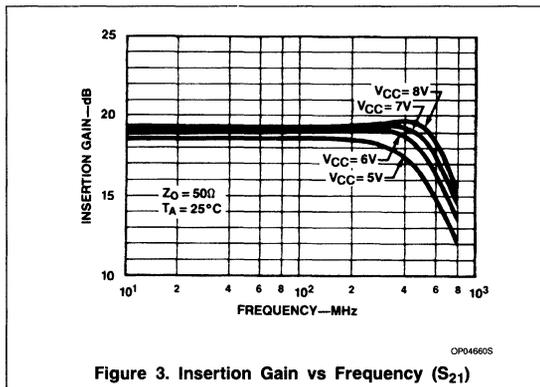
Figure 3. Insertion Gain vs Frequency (S_{21})
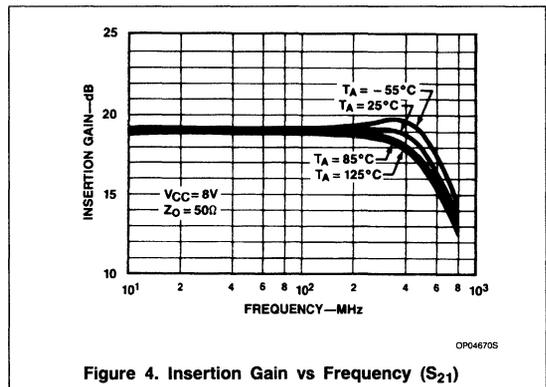
Figure 4. Insertion Gain vs Frequency (S_{21})
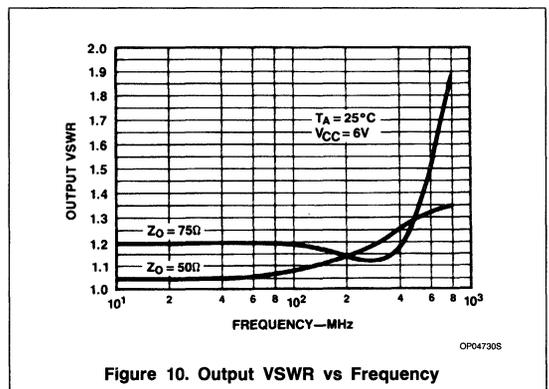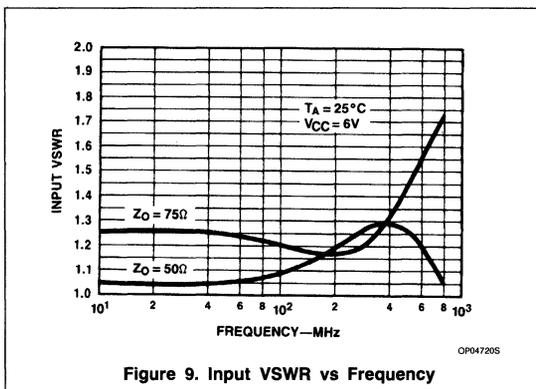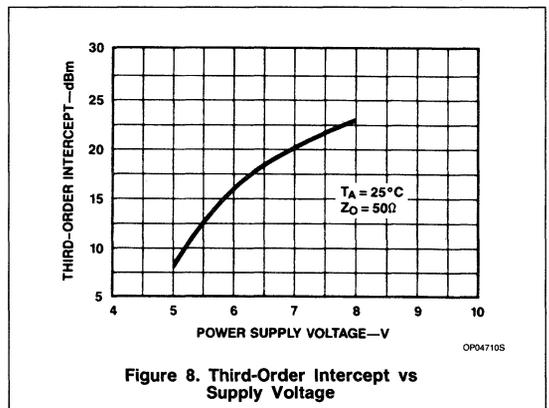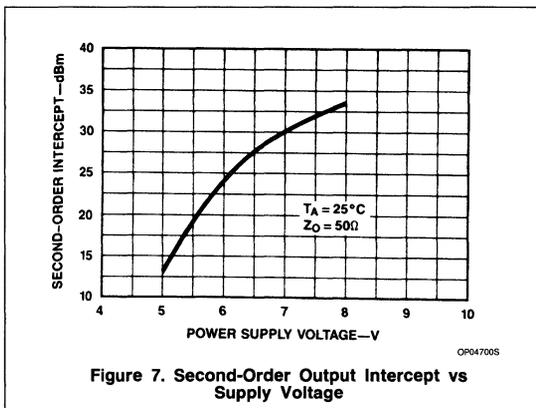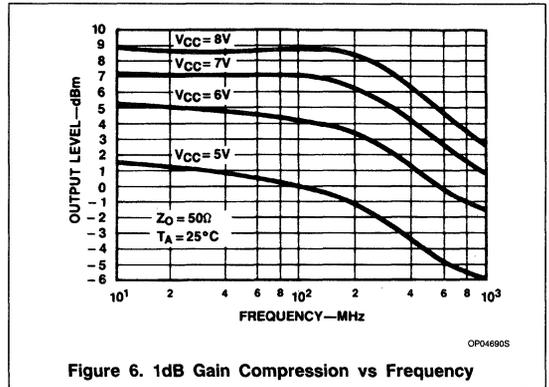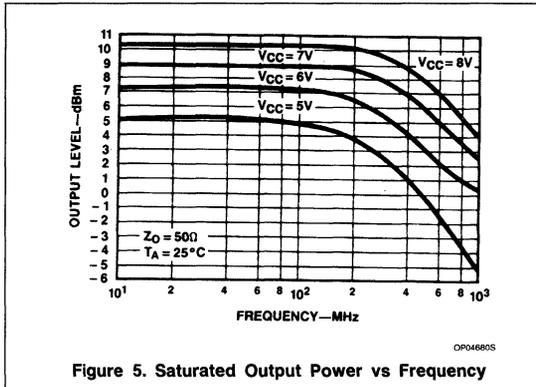
Wide-band High-Frequency Amplifier

NE/SA/SE5205

Figure 5. Saturated Output Power vs Frequency

Figure 6. 1dB Gain Compression vs Frequency

Figure 7. Second-Order Output Intercept vs Supply Voltage

Figure 8. Third-Order Intercept vs Supply Voltage

Figure 9. Input VSWR vs Frequency

Figure 10. Output VSWR vs Frequency

Wide-band High-Frequency Amplifier

NE/SA/SE5205

Figure 11. Input (S_{11}) and Output (S_{22}) Return Loss vs Frequency

Figure 12. Isolation vs Frequency (S_{12})

Figure 13. Insertion Gain vs Frequency (S_{21})

Figure 14. Insertion Gain vs Frequency (S_{21})
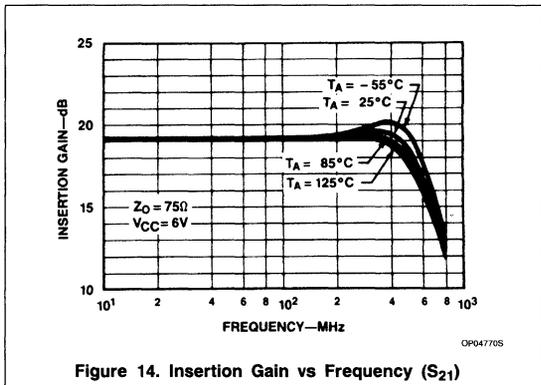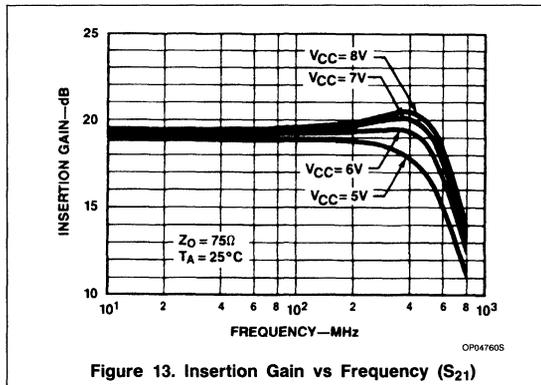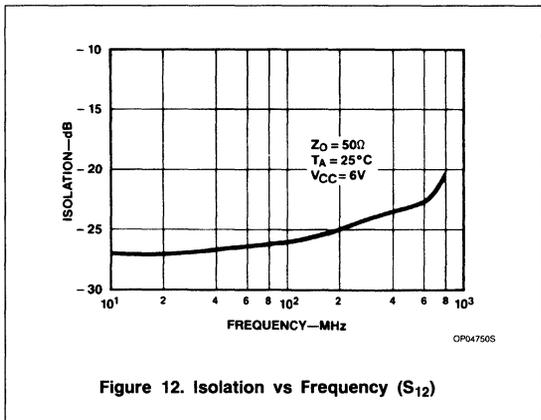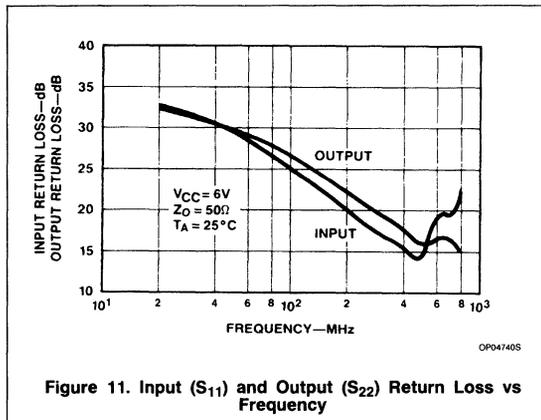
Wide-band High-Frequency Amplifier

NE/SA/SE5205

THEORY OF OPERATION

The design is based on the use of multiple feedback loops to provide wide-band gain together with good noise figure and terminal impedance matches. Referring to the circuit schematic in Figure 15, the gain is set primarily by the equation:

$$\frac{V_{OUT}}{V_{IN}} = (R_{F1} + R_{E1})/R_{E1} \qquad (1)$$

which is series-shunt feedback. There is also shunt-series feedback due to R_{F2} and R_{E2} which aids in producing wideband terminal impedances without the need for low value input shunting resistors that would degrade the noise figure. For optimum noise performance, R_{E1} and the base resistance of Q_1 are kept as low as possible while R_{F2} is maximized.

The noise figure is given by the following equation:

$$NF =$$

$$10 \ Log \left\{ 1 + \frac{\left[r_b + R_{E1} + \frac{KT}{2qI_{C1}} \right]}{R_0} \right\} \ dB \qquad (2)$$

where $I_{C1} = 5.5mA$, $R_{E1} = 12\Omega$, $r_b = 130\Omega$, $KT/q = 26mV$ at $25°C$ and $R_0 = 50$ for a 50Ω system and 75 for a 75Ω system.

The DC input voltage level V_{IN} can be determined by the equation:

$$V_{IN} = V_{BE1} + (I_{C1} + I_{C3}) \ R_{E1}$$

where $R_{E1} = 12\Omega$, $V_{BE} = 0.8V$, $I_{C1} = 5mA$ and $I_{C3} = 7mA$ (currents rated at $V_{CC} = 6V$). Under the above conditions, V_{IN} is approximately equal to 1V.

Level shifting is achieved by emitter-follower Q_3 and diode Q_4 which provide shunt feedback to the emitter of Q_1 via R_{F1}. The use of an emitter-follower buffer in this feedback loop essentially eliminates problems of shunt feedback loading on the output. The value of $R_{F1} = 140\Omega$ is chosen to give the desired nominal gain. The DC output voltage V_{OUT} can be determined by:

$$V_{OUT} = V_{CC} - (I_{C2} + I_{C6})R2, \qquad (4)$$

where $V_{CC} = 6V$, $R_2 = 225\Omega$, $I_{C2} = 7mA$ and $I_{C6} = 5mA$.

From here it can be seen that the output voltage is approximately 3.3V to give relatively equal positive and negative output swings. Diode Q_5 is included for bias purposes to allow direct coupling of R_{F2} to the base of Q_1. The dual feedback loops stabilize the DC operating point of the amplifier.

The output stage is a Darlington pair (Q_6 and Q_2) which increases the DC bias voltage on the input stage (Q_1) to a more desirable value, and also increases the feedback loop gain. Resistor R_0 optimizes the output VSWR (Voltage Standing Wave Ratio). Inductors L_1 and L_2 are bondwire and lead inductances which are roughly 3nH. These improve the high-frequency impedance matches at input and output by partially resonating with 0.5pF of pad and package capacitance.

POWER DISSIPATION CONSIDERATIONS

When using the part at elevated temperature, the engineer should consider the power dissipation capabilities of each package.

At the nominal supply voltage of 6V, the typical supply current is 25mA (30mA Max). For operation at supply voltages other than 6V, see Figure 1 for I_{CC} versus V_{CC} curves. The supply current is inversely proportional to temperature and varies no more than 1mA between 25°C and either temperature extreme. The change is 0.1% per °C over the range.

The recommended operating temperature ranges are air-mount specifications. Better heat sinking benefits can be realized by mounting the D and EC package body against the PC board plane.
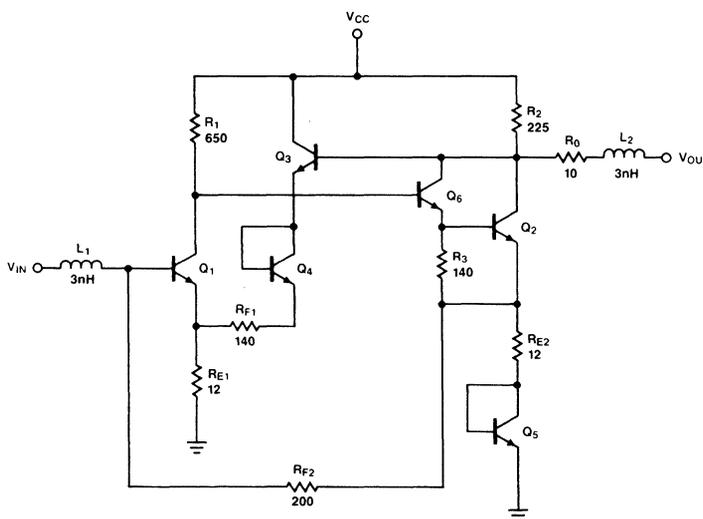

Figure 15. Schematic Diagram

Wide-band High-Frequency Amplifier

NE/SA/SE5205

PC BOARD MOUNTING

In order to realize satisfactory mounting of the NE5205 to a PC board, certain techniques need to be utilized. The board must be double-sided with copper and all pins must be soldered to their respective areas (i.e., all GND and V_{CC} pins on the SO package). In addition, if the EC package is used, the case should be soldered to the ground plane. The power supply should be decoupled with a capacitor as close to the V_{CC} pins as possible and an RF choke should be inserted between the supply and the device. Caution should be exercised in the connection of input and output pins. Standard microstrip should be observed wherever possible. There should be no solder bumps or burrs or any obstructions in the signal path to cause launching problems. The path should be as straight as possible and lead lengths as short as possible from the part to the cable connection. Another important consideration is that the input and output should be AC coupled. This is because at $V_{CC} = 6V$, the input is approximately at 1V while the output is at 3.3V. The output must be decoupled into a low impedance system or the DC bias on the output of the amplifier will be loaded down causing loss of output power. The easiest way to decouple the entire amplifier is by soldering a high frequency chip capacitor directly to the input and output pins of the device. This circuit is shown in Figure 16. Follow these recommendations to get the best frequency response and noise immunity. The board design is as important as the integrated circuit design itself.

SCATTERING PARAMETERS

The primary specifications for the NE/SA/SE5205 are listed as S-parameters. S-parameters are measurements of incident and reflected currents and voltages between the source, amplifier and load as well as transmission losses. The parameters for a two-port network are defined in Figure 17.
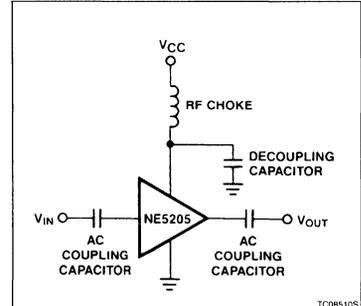

Figure 16. Circuit Schematic for Coupling and Power Supply Decoupling
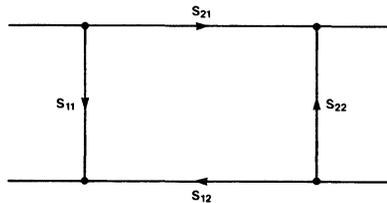
Figure 17a. Two-Port Network Defined

S_{11} — INPUT RETURN LOSS

$$S_{11} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM INPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT INPUT PORT}}}$$

S_{12} — REVERSE TRANSMISSION LOSS OR ISOLATION

$$S_{12} \equiv \sqrt{\text{REVERSE TRANSDUCER POWER GAIN}}$$

S_{21} — FORWARD TRANSMISSION LOSS OR INSERTION GAIN

$$S_{21} \equiv \sqrt{\text{TRANSDUCER POWER GAIN}}$$

S_{22} — OUTPUT RETURN LOSS

$$S_{22} \equiv \sqrt{\frac{\text{POWER REFLECTED FROM OUTPUT PORT}}{\text{POWER AVAILABLE FROM GENERATOR AT OUTPUT PORT}}}$$

Figure 17b

Actual S-parameter measurements using an HP network analyzer (model 8505A) and an HP S-parameter tester (models 8503A/B) are shown in Figure 18.

Values for the figures below are measured and specified in the data sheet to ease adaptation and comparison of the NE/SA/SE5205 to other high-frequency amplifiers.

Wide-band High-Frequency Amplifier

NE/SA/SE5205

50Ω System

a. Insertion Gain vs Frequency (S₂₁)

75Ω System

b. Insertion Gain vs Frequency (S₂₁)

c. Isolation vs Frequency (S₁₂)

d. S₁₂ Isolation vs Frequency

e. Input (S₁₁) and Output (S₂₂) Return Loss vs
Frequency

f. Input (S₁₁) and Output (S₂₂) Return Loss vs
Frequency

Figure 18
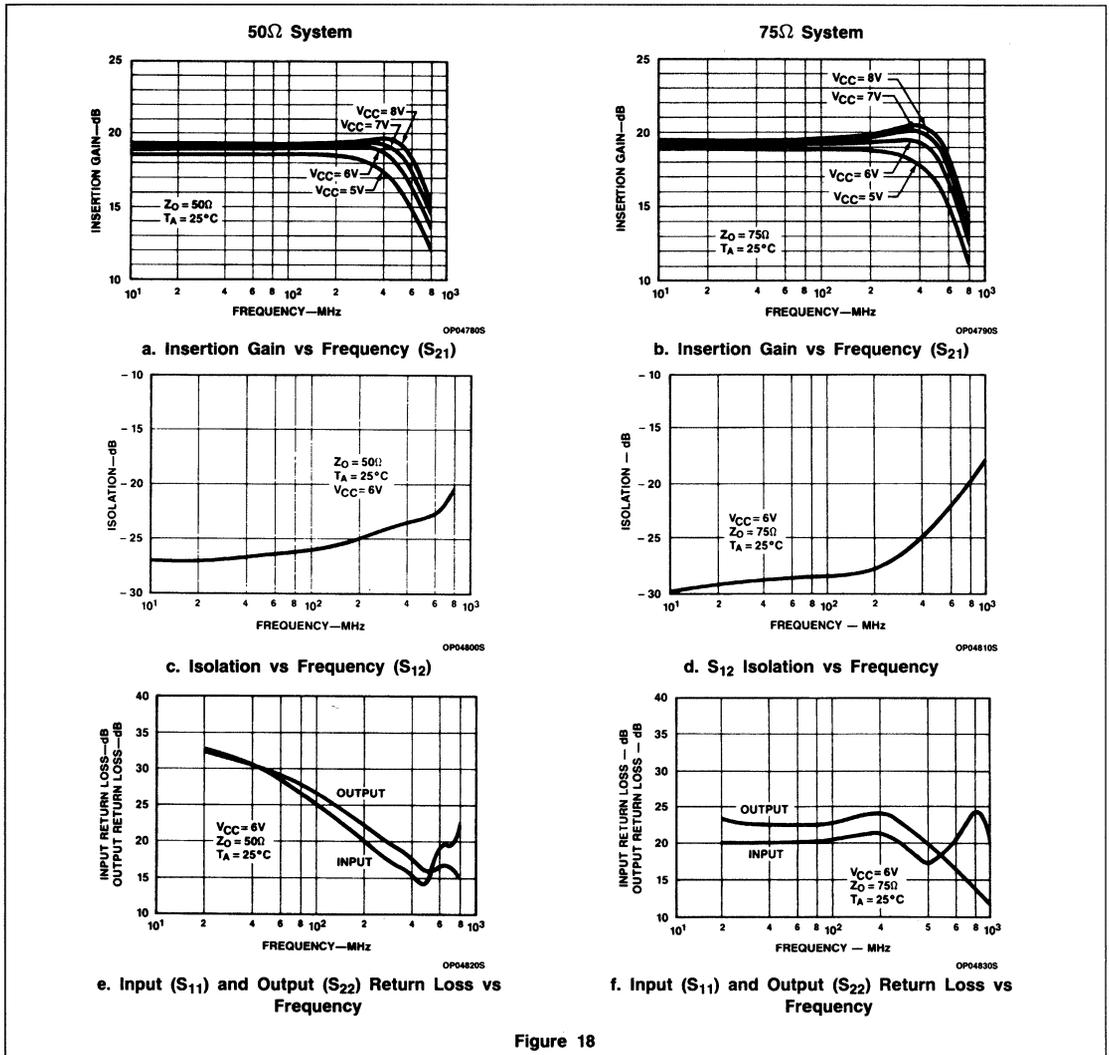
Wide-band High-Frequency Amplifier

NE/SA/SE5205

The most important parameter is S_{21}. It is defined as the square root of the power gain, and, in decibels, is equal to voltage gain as shown below:

$Z_D = Z_{IN} = Z_{OUT}$ for the NE/SA/SE5205

$$P_{IN} = \frac{V_{IN}^2}{Z_D} \quad \boxed{\begin{array}{c} NE/SA/ \\ SE5205 \\ Z_D \end{array}} \quad P_{OUT} = \frac{V_{OUT}^2}{Z_D}$$
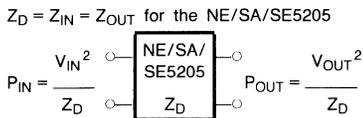
$$\therefore \frac{P_{OUT}}{P_{IN}} = \frac{\dfrac{V_{OUT}^2}{Z_D}}{\dfrac{V_{IN}^2}{Z_D}} = \frac{V_{OUT}^2}{V_{IN}^2} = P_I$$

$$P_I = V_I^2$$

P_I = Insertion Power Gain

V_I = Insertion Voltage Gain

Measured value for the NE/SA/SE5205 = $|S_{21}|^2 = 100$

$$\therefore P_I = \frac{P_{OUT}}{P_{IN}} = |S_{21}|^2 = 100$$

and $V_I = \dfrac{V_{OUT}}{V_{IN}} = \sqrt{P_I} = S_{21} = 10$

In decibels:

$P_{I(dB)} = 10 \text{ Log } |S_{21}|^2 = 20dB$

$V_{I(dB)} = 20 \text{ Log } S_{21} = 20dB$

$\therefore P_{I(dB)} = V_{I(dB)} = S_{21(dB)} = 20dB$

Also measured on the same system are the respective voltage standing wave ratios. These are shown in Figure 19. The VSWR can be seen to be below 1.5 across the entire operational frequency range.

Relationships exist between the input and output return losses and the voltage standing wave ratios. These relationships are as follows:

INPUT RETURN LOSS = $S_{11}dB$
  $S_{11}dB = 20 \text{ Log } |S_{11}|$

OUTPUT RETURN LOSS = $S_{22}dB$
  $S_{22}dB = 20 \text{ Log } |S_{22}|$

INPUT VSWR = $\dfrac{|1 + S_{11}|}{|1 - S_{11}|} \leqslant 1.5$

OUTPUT VSWR = $\dfrac{|1 + S_{22}|}{|1 - S_{22}|} \leqslant 1.5$

1dB GAIN COMPRESSION AND SATURATED OUTPUT POWER

The 1dB gain compression is a measurement of the output power level where the small-signal insertion gain magnitude decreases 1dB from its low power value. The decrease is due to nonlinearities in the amplifier, an indication of the point of transition between small-signal operation and the large signal mode.

The saturated output power is a measure of the amplifier's ability to deliver power into an external load. It is the value of the amplifier's output power when the input is heavily overdriven. This includes the sum of the power in all harmonics.

INTERMODULATION INTERCEPT TESTS

The intermodulation intercept is an expression of the low level linearity of the amplifier. The intermodulation ratio is the difference in dB between the fundamental output signal level and the generated distortion product level. The relationship between intercept and intermodulation ratio is illustrated in Figure 20, which shows product output levels plotted versus the level of the fundamental output for two equal strength output signals at different frequencies. The upper line shows the fundamental output plotted against itself with a 1dB

to 1dB slope. The second and third order products lie below the fundamentals and exhibit a 2:1 and 3:1 slope, respectively.

The intercept point for either product is the intersection of the extensions of the product curve with the fundamental output.

The intercept point is determined by measuring the intermodulation ratio at a single output level and projecting along the appropriate product slope to the point of intersection with the fundamental. When the intercept point is known, the intermodulation ratio can be determined by the reverse process. The second order IMR is equal to the difference between the second order intercept and the fundamental output level. The third order IMR is equal to twice the difference between the third order intercept and the fundamental output level. These are expressed as:

$IP_2 = P_{OUT} + IMR_2$

$IP_3 = P_{OUT} + IMR_3/2$

where P_{OUT} is the power level in dBm of each of a pair of equal level fundamental output signals, IP_2 and IP_3 are the second and third order output intercepts in dBm, and IMR_2 and IMR_3 are the second and third order intermodulation ratios in dB. The intermodulation intercept is an indicator of intermodulation performance only in the small signal operating range of the amplifier. Above some output level which is below the 1dB compression point, the active device moves into large-signal operation. At this point the intermodulation products no longer follow the straight line output slopes, and the intercept description is no longer valid. It is therefore important to measure IP_2 and IP_3 at output levels well below 1dB compression. One must be careful, however, not to select too low levels because the test equipment may not be able to recover the signal from the noise. For the NE/SA/SE5205 we have chosen an output level of $-10.5dBm$ with fundamental frequencies of 100.000 and 100.01MHz, respectively.

a. Input VSWR vs Frequency

b. Output VSWR vs Frequency

Figure 19. Input/Output VSWR vs Frequency
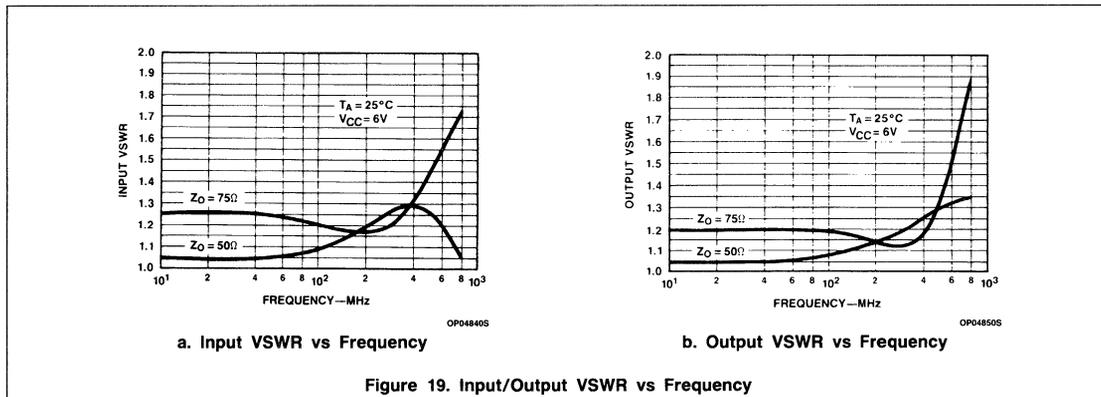
Wide-band High-Frequency Amplifier

NE/SA/SE5205

ADDITIONAL READING ON SCATTERING PARAMETERS

For more information regarding S-parameters, please refer to *High-Frequency Amplifiers* by Ralph S. Carson of the University of Missouri, Rolla, Copyright 1985; published by John Wiley & Sons, Inc.

"S-Parameter Techniques for Faster, More Accurate Network Design", HP App Note 95-1, Richard W. Anderson, 1967, HP Journal.

"S-Parameter Design", HP App Note 154, 1972.

OP04860S

Figure 20

Signetics
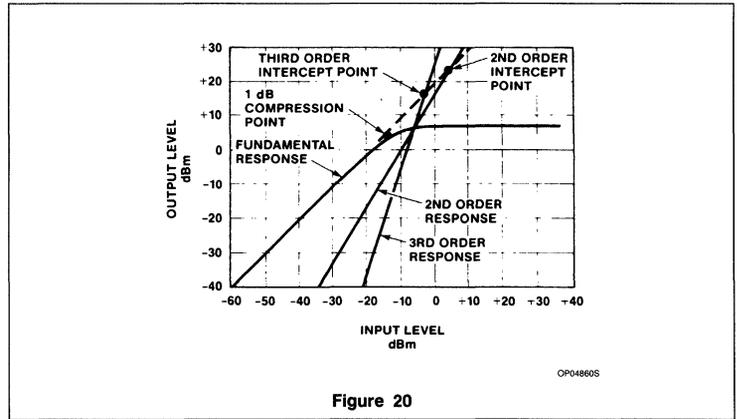
Linear Products

NE/SE5539
High Frequency Operational Amplifier

Product Specification

DESCRIPTION

The NE/SE5539 is a very wide band-width, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter-follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed-loop gains, both inverting and non-inverting, to meet specific design requirements.

FEATURES
* **Bandwidth**
  - **Unity gain – 350MHz**
  - **Full power – 48MHz**
  - **GBW – 1.2 GHz at 17dB**
* **Slew rate: 600/Vμs**
* **A_{VOL}: 52dB typical**
* **Low noise – 4nV/$\sqrt{Hz}$ typical**
* **MIL-STD processing available**

APPLICATIONS
* **High speed datacomm**
* **Video monitors & TV**
* **Satellite communications**
* **Image processing**
* **RF instrumentation & oscillators**
* **Magnetic storage**
* **Military communications**

PIN CONFIGURATION
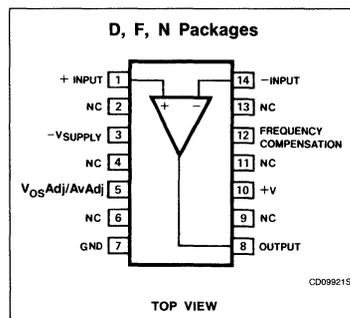
D, F, N Packages

Pin	Signal	Pin	Signal
1	+ INPUT	14	– INPUT
2	NC	13	NC
3	– V SUPPLY	12	FREQUENCY COMPENSATION
4	NC	11	NC
5	V_{OS} Adj/Av Adj	10	+V
6	NC	9	NC
7	GND	8	OUTPUT

TOP VIEW

CD09921S

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	0 to +70°C	NE5539N
14-Pin Plastic SO	0 to +70°C	NE5539D
14-Pin Cerdip	0 to +70°C	NE5539F
14-Pin Plastic DIP	–55°C to +125°C	SE5539N
14-Pin Cerdip	–55°C to +125°C	SE5539F

ABSOLUTE MAXIMUM RATINGS[1]

| SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	± 12	V

P_{DMAX}	Maximum power dissipation, T_A = 25°C (still-air)[2]
	  F package
	  N package
	  D package
		
		1.17
		1.45
		0.99
			
			W
			W
			W

T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Max junction temperature	150	°C

T_A	Operating temperature range
	  NE
	  SE
		
		0 to 70
		–55 to +125
			
			°C
			°C

T_{SOLD}	Lead temperature (10sec max)	300	°C

NOTES:
1. Differential input voltage should not exceed 0.25V to prevent excessive input bias current and common-mode voltage 2.5V. These voltage limits may be exceeded if current is limited to less than 10mA.
2. Derate above 25°C, at the following rates:
   F package at 9.3 mW/°C
   N package at 11.6 mW/°C
   D package at 7.9 mW/°C

High Frequency Operational Amplifier   NE/SE5539

EQUIVALENT CIRCUIT

TC08730S
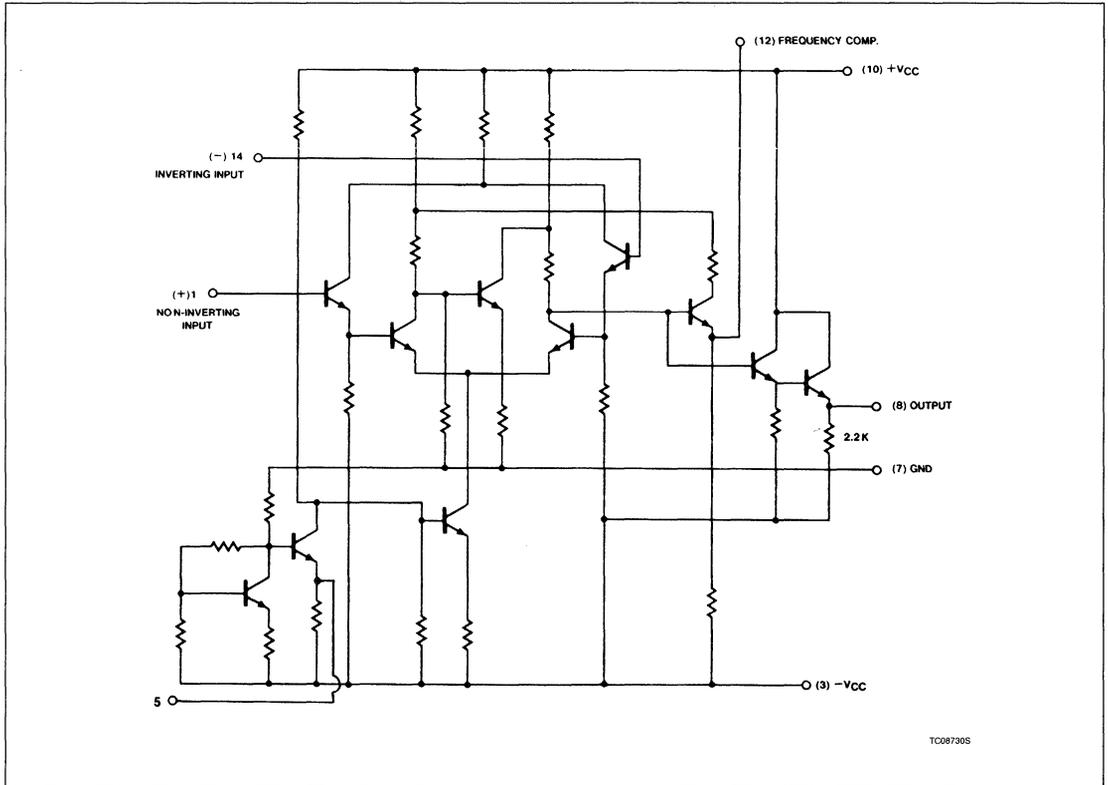
DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
	$\Delta V_{OS}/\Delta T$				5			5		$\mu V/°C$
I_{OS}	Input offset current		Over temp		0.1	3				μA
			$T_A = 25°C$		0.1	1			2	
	$\Delta I_{OS}/\Delta T$				0.5			0.5		$nA/°C$
I_B	Input bias current		Over temp		6	25				μA
			$T_A = 25°C$		5	13		5	20	
	$\Delta I_B/\Delta T$				10			10		$nA/°C$
CMRR	Common-mode rejection ratio	$F = 1kHz$, $R_S = 100\Omega$, $V_{CM} \pm 1.7V$		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		$k\Omega$
R_{OUT}	Output impedance				10			10		Ω

High Frequency Operational Amplifier

NE/SE5539

DC ELECTRICAL CHARACTERISTICS (Continued) $V_{CC} = \pm 8V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$	+ Swing				+ 2.3	+ 2.7		V
			−Swing				−1.7	−2.2		
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ to GND	Over temp + Swing	+ 2.3	+ 3.0					V
			−Swing	−1.5	−2.1					
			$T_A = 25°C$ + Swing	+ 2.5	+ 3.1					V
			−Swing	−2.0	−2.7					
$I_{CC}+$	Positive supply current	$V_O = 0$, $R_1 = \infty$	Over temp		14	18				mA
			$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_O = 0$, $R_1 = \infty$	Over temp		11	15				mA
			$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$	Over temp		300	1000				μV/V
			$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_O = + 2.3V$, $-1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$					47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = + 2.3V$, $-1.7V$ $R_L = 2\Omega$ to GND	$T_A = 25°C$				47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = + 2.5V$, $-2.0V$ $R_L = 2k\Omega$ to GND	Over temp	46		60				dB
			$T_A = 25°C$	48	53	58				

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS		SE5539			UNIT
				Min	Typ	Max	
V_{OS}	Input offset voltage		Over temp		2	5	mV
			$T_A = 25°C$		2	3	
I_{OS}	Input offset current		Over temp		0.1	3	μA
			$T_A = 25°C$		0.1	1	
I_B	Input bias current		Over temp		5	20	μA
			$T_A = 25°C$		4	10	
CMRR	Common-mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$		70	85		dB
$I_{CC}+$	Positive supply current		Over temp		11	14	mA
			$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current		Over temp		8	11	mA
			$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$	Over temp		300	1000	μV/V
			$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp + Swing	+ 1.4	+ 2.0		V
			−Swing	−1.1	−1.7		
			$T_A = 25°C$ + Swing	+ 1.5	+ 2.0		
			−Swing	−1.4	−1.8		

High Frequency Operational Amplifier

NE/SE5539

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
			Min	Typ	Max	Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$, $V_0 = 0.1$ V_{P-P}		1200			1200		MHz
	Small-signal bandwidth	$A_{CL} = 2$, $R_L = 150\Omega^1$		110			110		MHz
t_S	Settling time	$A_{CL} = 2$, $R_L = 150\Omega^1$		15			15		ns
SR	Slew rate	$A_{CL} = 2$, $R_L = 150\Omega^1$		600			600		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2$, $R_L = 150\Omega^1$		7			7		ns
	Full power response	$A_{CL} = 2$, $R_L = 150\Omega^1$		48			48		MHz
	Full power response	$A_V = 7$, $R_L = 150\Omega^1$		20			20		MHz
	Input noise voltage	$R_S = 50\Omega$, 1MHz		4			4		nV/$\sqrt{Hz}$
	Input noise current	1MHz		6			6		pA/$\sqrt{Hz}$

NOTE:
1. External compensation.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE5539			UNIT
			Min	Typ	Max	
BW	Gain bandwidth product	$A_{CL} = 7$		700		MHz
	Small-signal bandwidth	$A_{CL} = 2^1$		120		MHz
t_S	Settling time	$A_{CL} = 2^1$		23		ns
SR	Slew rate	$A_{CL} = 2^1$		330		V/μs
t_{PD}	Propagation delay	$A_{CL} = 2^1$		4.5		ns
	Full power response	$A_{CL} = 2^1$		20		MHz

NOTE:
1. External compensation.

TYPICAL PERFORMANCE CURVES


NE5539 Open-Loop Phase

NE5539 Open-Loop Gain
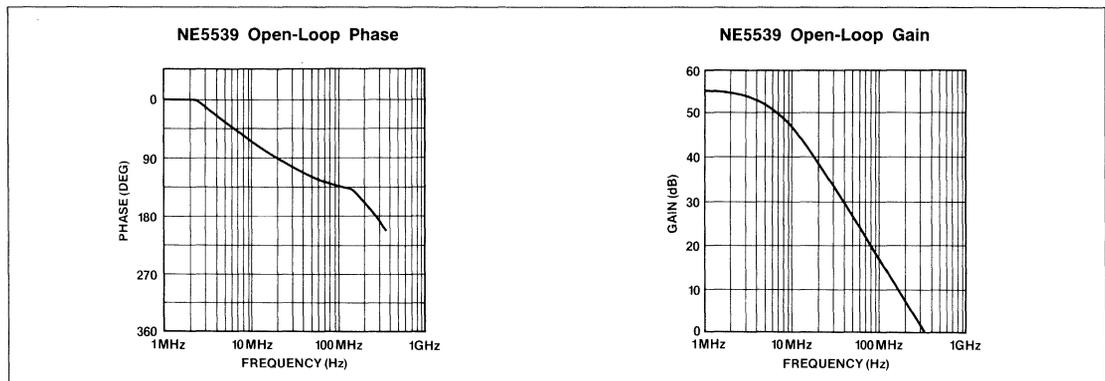
High Frequency Operational Amplifier

NE/SE5539

TYPICAL PERFORMANCE CURVES (Continued)

Power Bandwidth (SE)

OP05202S
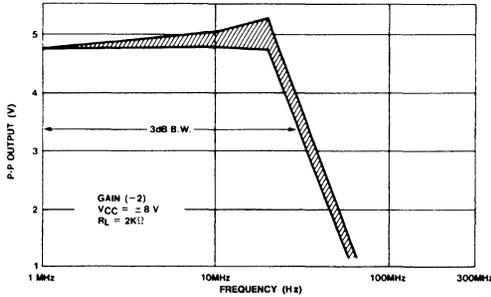
Power Bandwidth (NE)


OP05212S
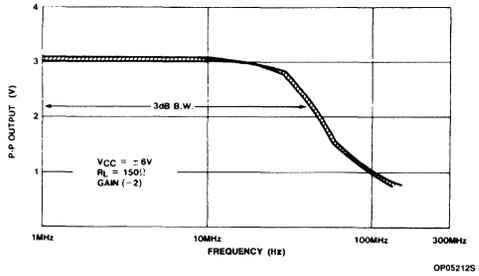
SE5539 Open-Loop Gain vs Frequency


OP05222S

Power Bandwidth

OP05231S
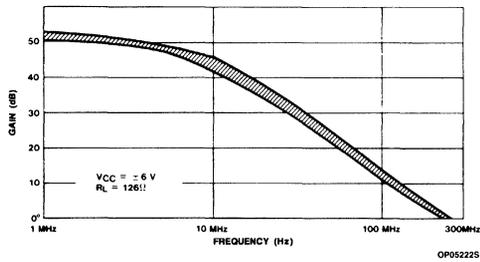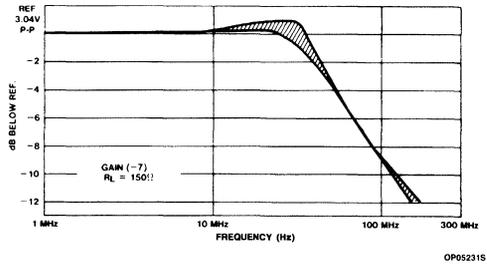
SE5539 Open-Loop Phase vs Frequency
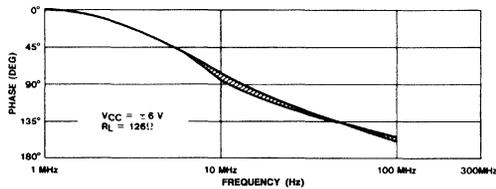
Gain Bandwidth Product vs Frequency

OP05251S
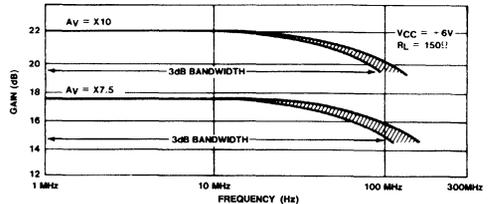
NOTE

Indicates typical
distribution $-55°C \leq T_A \leq 125°C$

OP05241S

High Frequency Operational Amplifier

NE/SE5539

CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide-gain bandwidth amplifier, the physical circuit layout is extremely critical. Breadboarding is not recommended. A double-sided copper-clad printed cirucit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.


TC08740S

NOTES:
R_1 = 75Ω 5% CARBON
R_2 = 75Ω 5% CARBON
R_3 = 75Ω 5% CARBON
R_4 = 36k 5% CARBON

R_5 = 20k TRIMPOT (CERMET)
R_F = 1.5k (28dB GAIN)
R_6 = 470Ω 5% CARBON

RFC 3T # 26 BUSS WIRE ON
FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)

Top Plane Copper[1] (Component Side)	Component Side (Component Layout)	Bottom Plane Copper[1]
DF05910S	DF05920S	DF05930S

NOTES:
(X) indicates ground connection to top plane.
*R_6 is on bottom side.

NOTE:
1. Bond edges of top and bottom ground plane copper.

Figure 1. 28dB Non-Inverting Amp Sample PC Layout

High Frequency Operational Amplifier

NE/SE5539

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown in Figure 2 along with vector-scope[1] photographs showing the amplifier differential gain and phase response to a standard five-step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of approximately 10 (20dB).

NOTE:
1. The input signal was 200mV and the output 2V. V_{CC} was ±8V.
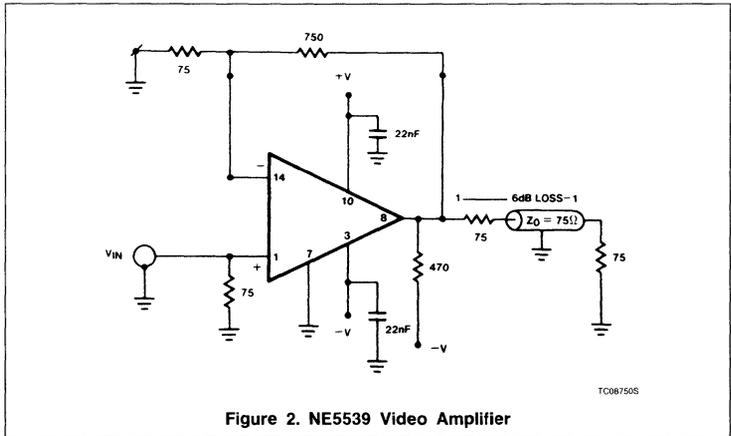

**Figure 2. NE5539 Video Amplifier**
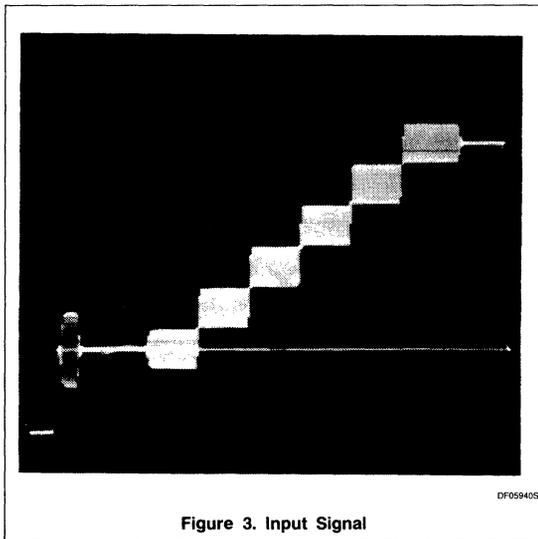
Figure 3. Input Signal
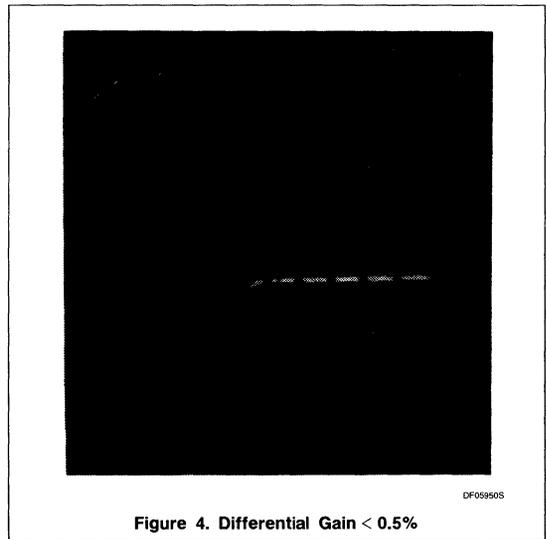
Figure 4. Differential Gain < 0.5%

NOTE:
Instruments used for these measurements were Tektronix 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

High Frequency Operational Amplifier

NE/SE5539
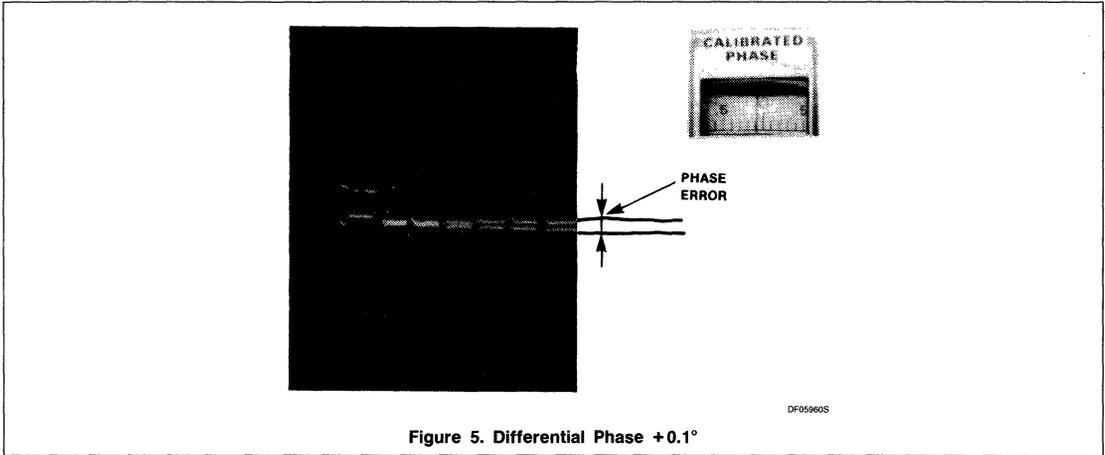
Figure 5. Differential Phase +0.1°

APPLICATIONS
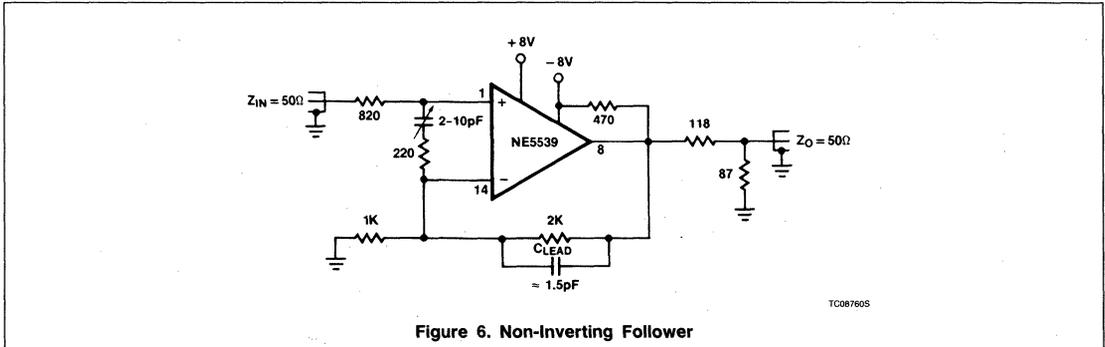
Figure 6. Non-Inverting Follower
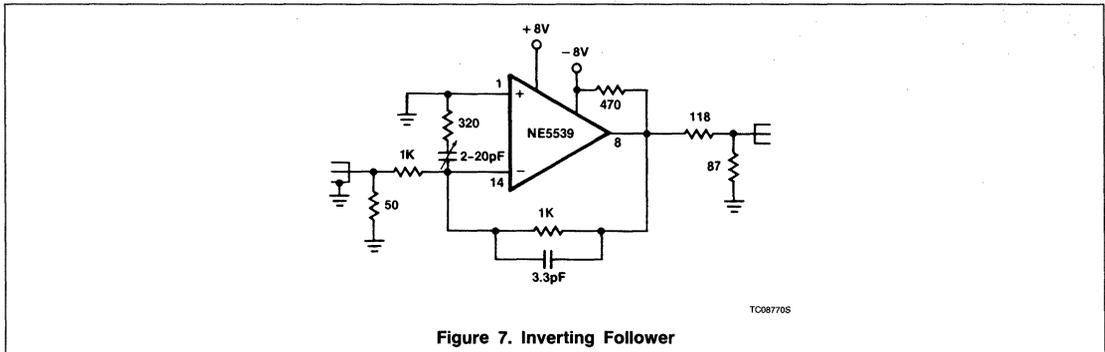
Figure 7. Inverting Follower

Signetics

Linear Products

Section 6
Sales Offices &
Ordering Information

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Signetics

Sales Offices, Representatives & Distributors

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