Signetics Military Products Handbook, Volume 2

Signetics

Philips Components

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Signetics

Military Products

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LIFE SUPPORT APPLICATIONS

Signetics Products are not designed for use in life support appliances, devices, or systems where malfunction of a Signetics Product can reasonably be expected to result in a personal injury. Signetics customers using or selling Signetics' Products for use in such applications do so at their own risk and agree to fully indemnify Signetics for any damages resulting from such improper use or sale.

Signetics registers eligible circuits under
the Semiconductor Chip Protection Act.

Preface

Military Products

Signetics, since 1961, has been dedicated to manufacturing integrated circuits to the stringent requirements of the Defense and Aerospace Industries. Today, the commitment to this charter is evidenced by our continuing efforts to offer state-of-the-art processes and product technologies which result in unequalled overall product reliability.

As further evidence of the Signetics commitment to serve the specific needs of the Military and Aerospace marketplaces, all of the Signetics fabrication facilities are JAN certified. We also maintain a separate marketing and manufacturing organization dedicated to servicing the special needs of the Defense and Aerospace community.

Our mission is one of total customer satisfaction by providing industry leading products and uncompromised quality and responsiveness.

Signetics

Military Products

Product Status

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Signetics

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Quality and Reliability

Military Products

SIGNETICS MILITARY PRODUCT QUALITY

Signetics Quality leadership begins with the Industry's first zero defect warranty. If a single defect is found in any lot that we ship, the entire lot may be sent back to the factory.

Since 1984, Signetics has adopted zero accept sampling plans in electrical, mechanical, and hermetic acceptance testing. Zero accept lot acceptance rates are typically 99.5% with any lot in which a defect is found being rescreened or scrapped.

The Department of Defense has issued contractor/vendor correlated quality objectives of less than 100 ppm in 1990. Signetics Estimated Process Quality (EPQ) has been well under 100 ppm since 1987

SIGNETICS PPM PROGRAM

Signetics offers a unique PPM Program to all customers who are willing to commit resources to defect reduction. The program contains five basic steps:

1) The customer assigns an engineering contact to work defect analysis with a Signetics Quality Assurance Engineer (QAE).
2) Measurements are established at the customer's facility summarizing inspection data by product, test quantity and reported defects.
3) Each month this data is analyzed, compared to Signetics data, and a Parieto Analysis is generated to identify the top 10 suspect device types measured in ppm by Signetics QAE.
4) The customer agrees to send all defects found of these device types to the Signetics Assigned QAE regardless of lot dispositioning. (If the entire lot is returned, the defects remain segregated with the lot.)
5) Signetics will retest each and every reported defect and, if invalid, will return the devices to the customer's contact with complete variables data to substantiate the invalidation. If valid, Signetics will implement corrective action.

This process iteration continues until corrective action is complete. The next 10 suspect devices are then determined and the process is repeated until the overall customer ppm measurement agrees with Signetics data.

SIGNETICS SHIP-TO-STOCK (STS) PROGRAM

Customers who have demonstrated the effectiveness of the PPM program may choose to reduce incoming inspection sampling, implement skip-lot sampling, or discontinue inspection completely. Signetics offers a proven STS program which provides for mutually agreeable device types to be shipped and received directly to the customer's stock with reduced or no receiving inspection. Signetics ppm database, as validated through the PPM Program, is monitored by Signetics QAE to assure continued defect-free performance. Acceptable candidates for STS are selected from the customer and Signetics ppm databases, where performance by device is agreed to be below 100 ppm (this is an arbitrary limit which can be negotiated with each customer).

Signetics QAE will again perform a Parieto Analysis based on device type, quantity shipped/received, and the reported defect levels. Those devices with a history of over 1000 devices shipped (again, arbitrary) and under 100 ppm are candidates for STS. Written agreement from the customer initiates the system. Shipments of STS certified material are uniquely labeled by Signetics for easy recognition by the customer's receiving group. Signetics QAE will continue to monitor the performance of these device types to assure less than 100 ppm defective on an ongoing basis. Should the Signetics performance exceed 100 ppm in a rolling 3 month period, Signetics will formally notify the customer that the device has been removed from STS and the customer's receiving inspection should be resumed. Similarly, the customer may abandon the system at any time, for any reason, simply by notifying the Signetics QAE.

Signetics Commercial Divisions have successfully implemented STS programs at over 112 customer locations, involving over 6200 device types. These customers enjoy the benefit of lower cost-of-ownership, reduced competition, and increased profits. STS is our customers reward for their investment in the PPM Program.

SIGNETICS JUST-IN-TIME (JIT) PROGRAM

A further customer benefit of the PPM and STS Programs is the Just-in-Time Program. The Signetics JIT program supplements STS to assure defect-free, on-time delivery, while minimizing the customer's inventory. JIT is available to any participating STS customer, but only on those STS device types which are also on the customer's Volume Purchase Agreement (VPA) with Signetics. A firm VPA release of 6 months minimum will assure monthly, bi-weekly, or weekly defect-free shipments to the customer's stock. Contact Military Marketing for more information.

SIGNETICS MILITARY PRODUCTS RELIABILITY

Signetics Reliability Assurance is involved throughout the initial design and process definition, characterization, product release, and production phases. Reliability organizations exist in each product group of Signetics, as well as in a Central Reliability group which establishes reliability standards and ongoing stress evaluation programs. A well-defined reliability program not only assures quality and quality-over-time, but provides dependability, lower cost of ownership, and technical responsiveness to our customers.

Each Military product, new process, or revised product released to production must first pass the rigid commercial reliability standards, and then be qualified to Military Standards. Each Military die family and package type are subjected to MIL-STD-883, Method 5005 Group C and D (die and packages, respectively) to demonstrate its suitability for Military usage. Thereafter, Quality Conformance Inspections conducted on each microcircuit group and package type on an annual basis, per paragraph 1.2.1 of MIL-STD-883.

The Corporate SURE Program also continuously monitors Commercial products with respect to processes and packages. The Military and SURE data bases together assure the Industry's highest reliable products. Further detail on the Signetics SURE Program may be found in any Signetics Commercial Data Manual, or contact your local sales representative to obtain a SURE Reliability Report.

SIGNETICS MILITARY QUALITY IMPROVEMENT PROCESS

In 1980, Signetics recognized the need to improve product quality from the 10,000 ppm level to below 100 ppm. As evidenced by the preceding sections, the Quality Improvement Process has more than achieved that initial ppm quality goal. Today, Signetics strives to demonstrate continuous improvement in all business measures, including quality and service.

Product Description

Military Products

MILITARY STANDARD PRODUCTS

The Signetics standard product line offering includes JAN qualified Class S and Class B products, Standard Military and DESC Drawings, and Class B and C vendor standard products.

All Signetics standard products are 100% screened to the requirements of the most current issue of MIL-STD-883, Method 5004, and periodically sampled to Quality Conformance Inspection (QCI), Method 5005. Signetics utilizes alternate Group A and alternate Group B for all product lines. The details of these test methods, as well as additional related requirements of MIL-M-38510 and MIL-STD-883, are not repeated herein so as to not mislead our customers by errors or omission of requirements included in those specifications.

This product description supersedes all prior dated Military Product literature, including commercial data books containing Military Product electrical characteristics, flow descriptions, and package physical dimensions.

JAN Qualified Products

Signetics JAN Class S and Class B products are produced on government certified production lines and are qualified by the Defense Electronics Supply Center (DESC) in Dayton, Ohio.

JAN Class S products represent the highest level of quality and reliability as prescribed by MIL-STD-454, Requirement 64 and by MIL-HDBK-217, and are recommended for use in the most critical of applications such as manned space and satellite use.

JAN Class B products are the procurement preference for all general Military applications such as avionics, missiles, computers, launch control, fire control, and critical ground support electronics.

JAN qualified products are fabricated, assembled, tested, and inspected in U.S. Government certified facilities in Sunnyvale, California, Orem, Utah, and Albuquerque, New Mexico.

DESC prohibits any customer imposed deviations or waivers on procurement of JAN products. Products must conform completely to government specifications and are verified by Signetics Quality Control.

JAN qualified products are listed on the Qualified Products List, QPL-38510, issued periodically by DESC. For current QPL information, customers may contact their local sales representative, Military Marketing or directly with DESC-EQM at (513) 296-6355. The JAN products listed herein should be considered valid only on its date of publication.

These categories of product conform to quality Levels S and B of MIL-HDBK-217 ($\pi_Q = 0.25$ for Class S, 1.0 for Class B).

Standard Military Drawing (SMD)

DESC selected item drawings (mini-specs) were produced by DESC-ECS during the period of 1976-1986 to serve as an interim standard for use prior to the publication of a JAN detailed slash sheet.

Standard Military Drawings (SMD), introduced in 1986, fulfill the same needs as DESC Drawings, but are streamlined about the general requirements of compliant non-JAN device types as defined by MIL-STD-883, Paragraph 1.2.1.

Until a qualified JAN device is available, the SMD serves as the Class B standard procurement preference as defined by MIL-STD-454, Requirement 64.

All Signetics products offered as SMD's fully conform with MIL-STD-883, Paragraph 1.2.1 and to the detailed drawing. Final electrical, Group A, and end-point electrical tests are defined by the SMD.

Many SMD products are dual-marked with the Signetics Class B standard product part number.

This category of product conforms to Quality Level B-1 of MIL-HDBK-217 ($\pi_Q = 2.0$)

Signetics Class B Standard Products

Signetics Class B Vendor Standard products are offered for use when JAN products are not qualified on the QPL, when SMD products are not available, or when program requirements allow the use of vendor standard products.

All Class B standard products are compliant to MIL-STD-883, general provisions Paragraph 1.2.1 for non-JAN devices. No claims by Signetics are otherwise made of equivalence to JAN products or to MIL-M-38510. Signetics standard products also conform with JEDEC Publication 101.

Electrical specifications are as included in the most current Signetics Military Data Manual.

- 100% final electrical tests include all data manual parameter limits, test conditions, and temperatures applicable to Subgroups 1, 2, 3, 7, 8, and 9 of MIL-STD-883, Method 5004 for digital products, or to Subgroups 1, 2, 3, 4, and 9 for Linear products.
- Alternate Group A sample electrical inspection tests include applicable final electrical subgroups as well as all other Data Manual parameters with specified minimum or maximum limits.
- End-point electrical tests used for QCI inspection sampling (Groups C and D) are those Data Manual parameter limits, test conditions, and temperatures applicable to the Group A Subgroups specified in the most similar associated detail specification (slashsheet).

Electrical parameters which have no specified minimum or maximum limits (typical performance only) are not tested. Parameters which have limits specified at 25°C only, are tested only at that temperature. Detailed parameter assignment to Group A subgroups and other test details are contained in documented Signetics internal Product Electrical specifications, and are available upon request. Actual test program symbolics are available for customer review at the factory, but are considered proprietary and will not be copied or otherwise distributed outside of Signetics.

Waivers or deviations deemed necessary in contracts must be processed in accordance with MIL-STD-480.

Package types which do not have case outline letters assigned in MIL-M-38510, Appendix C, are assigned case outline letters per JEDEC Publication 101.

The Signetics standard Product Assurance Plan documentation is available for customer review at the factory.

This category of product conforms to quality level B-1 of MIL-HDBK-217 ($\pi_Q = 2.0$).

Product Description

General Information

- All Signetics products are considered sensitive to electrostatic discharge (ESD), regardless of ESD category. In-process factory ESD controls are maintained from die attach through shipping. Devices are packed in protective tubes or magazines, enclosed in a Faraday shield container, and labeled in accordance with MIL-STD-129.

  WARNING: Devices may be degraded or destroyed if proper ESD handling techniques are not used when opening the shipping container. The Signetics warranty is void if product is not properly protected.

ESD Information

- Signetics products which have been classified for electrostatic discharge sensitivity (ESDS) according to MIL-STD-883, T/M3015, are described in the product listings of the current Military Product Reference Guide. Class 1 devices are further described by the highest level that samples were found acceptable at 1kV, 500V, and 250V. For information regarding products not yet classified, please contact Military Marketing.
- All Signetics production areas, critical support areas, subcontract test labs, and authorized distributor stocking locations are certified and periodically self-audited by Signetics Quality Assurance.
- Government Source Inspection (GSI) is provided on JAN qualified products by the Defense Contract Administration Services (DCAS). GSI services for all other non-JAN products must be delegated by the customer's Contracting Officer.
- Customer Source Inspection (CSI) which is contractually required on standard products is restricted to final documentation review only (Signetics does not identify work-in-process by customer). For custom or semi-custom products, CSI is permissible at any in-process operation.
- Source or Spec Control Drawings (SCD), Altered Item Drawings, and Selected Item Drawings (SID) are acceptable for review. The Signetics review guidelines reflect the standard requirements of MIL-STD-883, Paragraph 1.2.1.
- Signetics is agreeable to customer imposed qualification, First Article, or MIL-M-38510 QCI requirements on non-JAN products. Contact the factory for price and delivery information.
- Purchase order directed standard data pack requirements are acceptable for screening or QCI attribute data for all products. Contact the factory for price and delivery information.
- Signetics offers a one year limited warranty from the time of delivery to the customer on standard products for performance, workmanship, and conformance to the applicable product specifications. Products procured through Signetics authorized distributors are similarly under warranty for one year from the time of delivery to the customer. This warranty is not transferable through multiple distributor transactions, and is invalid for any product which is delivered by or transferred through a non-authorized distributor, broker or test laboratory.
- The Signetics warranty is invalid if the customer or his subcontractor subject the product to alteration (e.g., marking, lead cutting) or stresses beyond the capability of the product. Where environmental stress screening is contractually required, it is strongly recommended that Signetics be consulted as to the ability of the devices to survive the stresses, and that the test laboratory be certified by the customer's QA organization.
- Signetics recognizes that many government contracts require current lead finish solderability acceptance testing on every lot, and/or 100% solder coat rework.

  Because all Signetics products are solder coated after burn-in and prior to shipment, we recommend that the rework of solder coat not be attempted by our customers or their subcontractors.

  WARNING: Device seal integrity may be downgraded or destroyed if proper controls to avoid extreme thermal shock are not employed during solder coat. The Signetics warranty is void if product is damaged in solder coat rework.

  Solderability acceptance testing per MIL-STD-2000 and/or WS6536 can be performed by Signetics as a line-item lot test charge, if required. See the SOW-2000 Testing Statement included in this section.
- All products are marked with a unique country of origin code identifying the assembly plant location. The code "USA" signifies assembly in our Orem, Utah facility, and the code "THAI" signifies assembly in our Bangkok, Thailand facility.
- The Signetics plant address information is as follows:

Company Headquarters
Signetics Company
811 E. Arques Avenue
P.O. Box 3409
Sunnyvale, Ca 94088-3409
Telephone: (408) 991-2000
Telex: 172-243

Stateside Manufacturing
Signetics Company
1275 S. 800 East Street
Orem, Utah 84058
Telephone: (801) 225-6600

Offshore Manufacturing
Signetics Thailand Co. LTD.
303 Chaeng Wattana Road
Bangkhen
Bangkok, Thailand
Telephone: 66-2-521-0653

SOW-2000
Solderability Acceptance Testing

Statement of Work

FEATURES

- **Complies with MIL-STD-2000 solderability requirements**
- **Complies with WS6536E/I solderability requirements**
- **Maximizes component "Shelf Life"**

ORDERING INFORMATION

LINE ITEM	SOW-2000
When the line item stated above is entered in conjunction with a valid part number, Signetics will apply the requirement of this statement of work to that item per ship date requested.	

DESCRIPTION

MIL-STD-2000 (dated January 1989) and/or the Weapons Specification WS6536E/I (dated March 1986) is often imposed on semiconductor products with respect to solderability of lead finish. Signetics Military Products has generated a standard flow to generate an economic solution to meet these solderability requirements. Since the testing is performed just prior to shipment component shelf life is maximized.

STATEMENT OF WORK

	DESCRIPTION
1)	All components will be shipped with a hot solder dip lead finish that conforms with MIL-M-38510/P3.5.6.3.4 and MIL-STD-2000/P5.4.4..2, method 4A. This lead finish is applied over bare base metal and after the burn-in operation. Seal date codes will be no older than 3 years.
2)	Each lot and sublot required to meet the customer scheduled deliveries (each line item), will be submitted to solderability testing within 30 calendar days of the line item shipment. A lot test charge will be entered with each line item to ensure the factory is aware of the special test requirement, this line item will reference SOW-2000.
3)	The solderability test will be performed in accordance with MIL-STD-883/M2003, except aging will be 8-12 hours instead of the 4-8 hours prescribed by 883. The sample size shall be based on an AQL of 1.0% per MIL-STD-105, level S-2, which is a sample of 13 devices, test all leads, C=0. The test sample will be selected from shippable units, packaged separately, and delivered with the line item.
4)	A separate C of C will be prepared that certifies solderability acceptance; the test attributes and date of testing; the date of the soldercoat application; and stating compliance to MIL-M-38510/P3.5.6.3.4b and MIL-STD-2000/P5.4.4.1, 5.4.4.3(4a), and 5.4.13 and WS6536/P4.3.7
5)	A separate packing label will be placed on each intermediate container (the box that contains a single lot of tubes/magazines), with the date of soldercoat application and the date of solderability acceptance.

Ordering Information

Military Products

For standard products, customers shall specify the complete part number as listed in the product description herein or in the Signetics published price book. Use of the lead finish designator "X" is highly recommended for procurement, as it simplifies multisource procurements from manufacturers who may process devices with different lead finishes. The actual lead finish designator is marked on the product and on the shipping documents. Use of the Signetics factory number (i.e., JB54LS161AF or RB54LS161AF) is not recommended due to possible errors in order entry transposition.

For non-standard products, customers shall specify the SCD number and drawing revision.

For all products, purchase order options include:

- Source Inspection; Government (GSI) and/or Customer (CSI). A letter of delegation (DCAS) and source point description must accompany the purchase order prior to order entry.
- Special packing or packaging.
- Data packs; For Class B and C product, two options may be specified: Screening and Group A attribute data (supplied as a single data set), and/or Quality Conformance Inspection (QCI) attribute data (includes QCI groups B, C and D). For JAN Class S products, data packs include screening attributes, QCI attributes, and all variables data (SEM photographs or X-ray film are not included).

Coding Explanation

Military Products

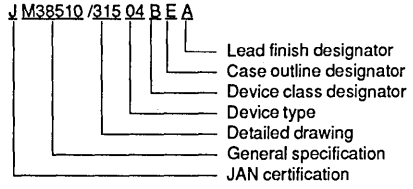
All products, whether JAN or standard product, are marked with the following information: per MIL-M-38510:

- ESD identifying triangle(s).
- Signetics manufacturer's identification logo:

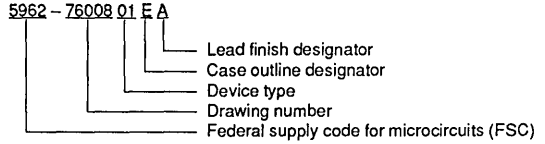
- Compliant product identifier, "C", per MIL-STD-883, 1.2.1. Not applicable to JAN or Class C products. This identifier is included on date codes after 8749.
- Inspection lot identification seal date code.
- Signetics manufacturer's designing symbol per NAVSHIPS 0967-190-4010. The Signetics manufacturer's designating symbol are the characters "DKB".
- Country of origin, "USA" or "THAI".
- Part number.
- The Pin 1 index point for most packages is found as a part of the package construction (i.e., the dual-in-line notch, the flat pack Pin 1 enlargement, or the leadless chip carrier elongated Pin 1 base terminal or chamfered package corner). The ESD identifying symbol is located in the Pin 1 quadrant, but not necessarily adjacent to Pin 1. For leadless chip carriers, the ESD identifier is located on the top surface at Pin 1.

The following examples illustrate the part marking system for 54LS161A standard product.

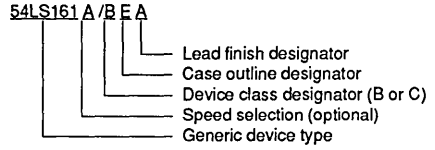
- For JAN products, the part number is per MIL-M-38510 and detailed device specification.



- For Standard Military Drawing products, the part number is per the drawing.



- For Signetics Vendor Standard Products, the part number is as listed in this product description or in published price lists.



Packaging Information

Military Products

SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

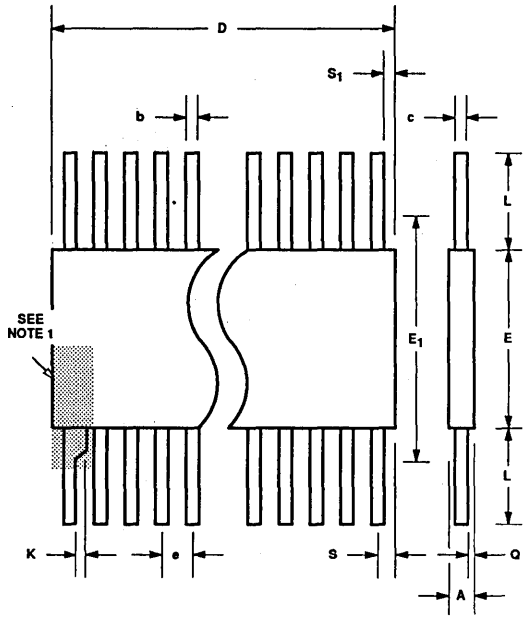
Table 1.

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt[4]
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X[2]	28
24DIP6	D-3	J	28
28DIP6	D-10	X[2]	28
40DIP6	D-5	Q	28
48DIP6	D-14[1]	X[2]	28
50DIP9	D-12[1]	X[2]	28
64DIP9	D-13[1]	X[2]	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y[2]	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y[2]	22
52FLAT	Y-1[1]	Y[2]	22
18LLCC	C-9	U[2]	20
20LLCC	C-2[3]	2	20
28LLCC	C-4[3]	3	20
32LLCC	C-12	U[2]	20
44LLCC	C-5	U[2]	20
68LLCC	C-7	U[2]	20
68PGA	P-AB	Z[2]	20
84PGA	P-AB	Z[2]	20

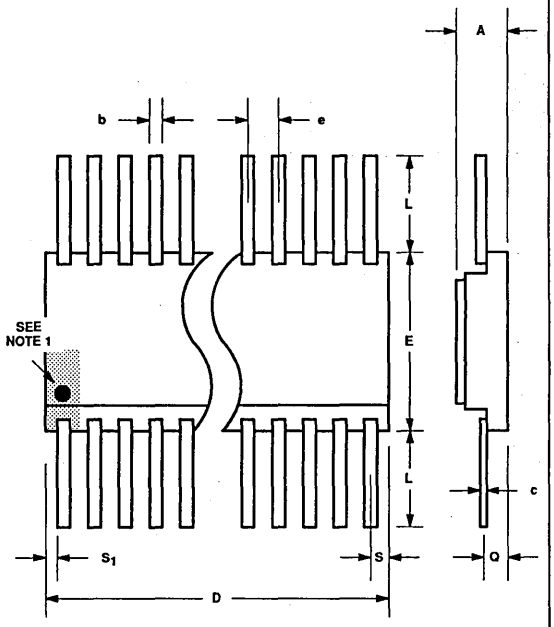
NOTES:
1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

Packaging Information

CASE OUTLINES Y (FLAT PACKAGES)



Configuration 1



Configuration 2

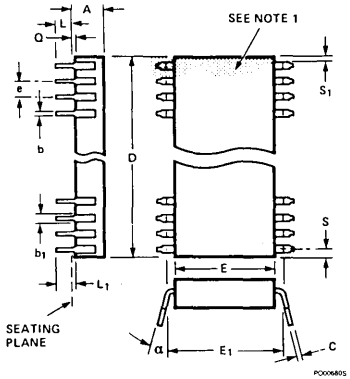
NOTES:

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counter-clockwise (as viewed from the top of the device.
2. This dimension allows for off-center lid, meniscus and glass overrun.
3. The reference pin spacing is 0.050 between center-lines. Each pin centerline is located within ±0.005 of its logitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish

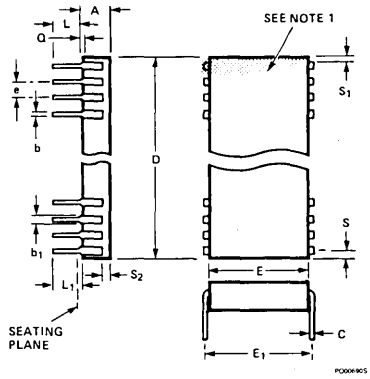
OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	
b	0.015	0.026	6
c	0.008	0.015	6
D	–	1.330	2
E	0.620	0.660	
e	0.050BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	–	0.045	5
S1	0.005	–	5

Packaging Information

CASE OUTLINES X (DUAL IN-LINE PACKAGES)



Configuration 1

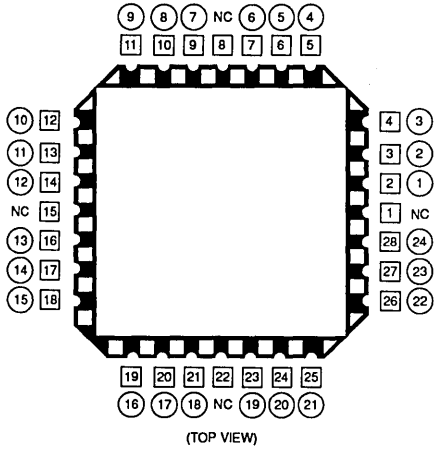


Configuration 2

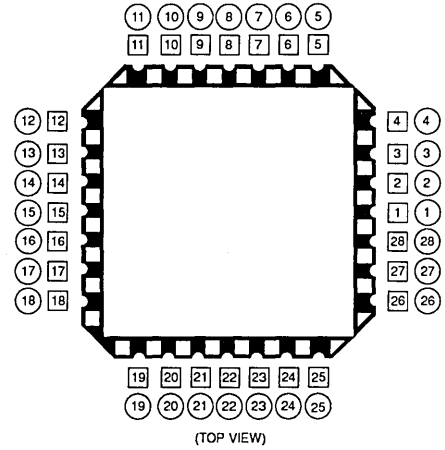
1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

Packaging Information

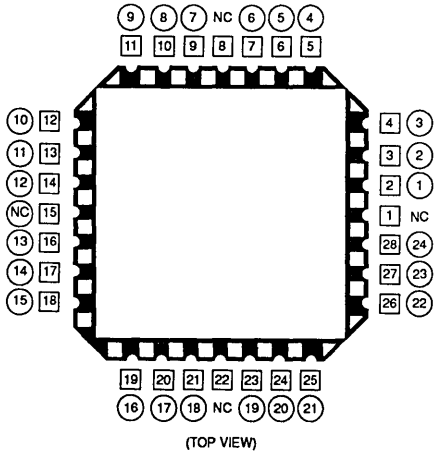
LEADLESS CHIP CARRIER (LLCC) PINOUTS



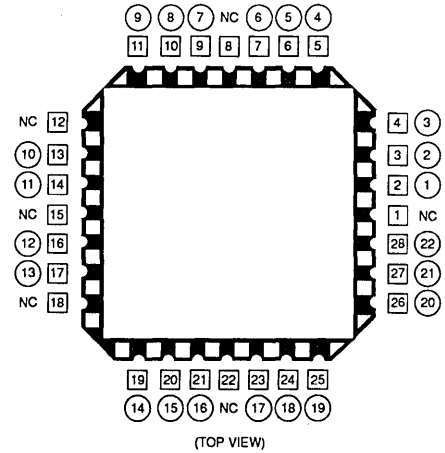
24-Lead Logic Pinout for 28 Terminal Chip Carrier



28-Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24-Lead Memory Pinout for 28 Terminal Chip Carrier

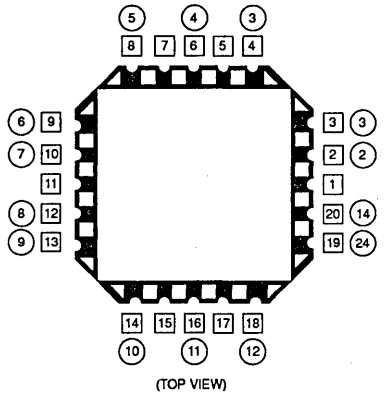


22-Lead Memory Pinout for 28 Terminal Chip Carrier

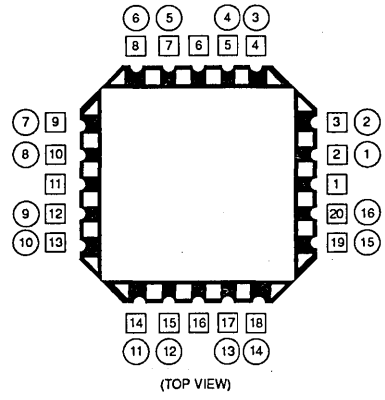
□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect

Packaging Information

LEADLESS CHIP CARRIER (LLCC) PINOUTS



14-Pin Logic Pinout for 20 Terminal Chip Carrier



16-Pin Logic Pinout for 20 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number

Test Guidelines

Military Products

TEST GUIDELINES

This data book has been prepared by the Signetics Military Products Group with the intention of describing both the requirements or limits of the devices contained within and the specific conditions which will be employed to meet the requirements. To ensure the accuracy of both the test program and the data sheets, the Quality and Reliability Group for the Military Group has performed at 100% audit of all such material and continues to monitor the process through approval of all test programs and data sheet ECNs (Engineering Change Notices).

There are some test condition details which can be best described in an overview section such as this. They are:

Logic Products

1. Functional Test
   - A) Consists of applying specific Logic patterns to the device inputs while verifying the correct output states.
   - B) Uses Logic levels where $V_I = V_{OL}$ or V_{OH}.
   - C) Is generally performed with no output load.
2. F_{MAX} Measurement
   - A) Is performed at the specified clock frequency and consists of ensuring that the device does function. There are no constraints on Pulse Rise Time, Fall Time or Setup and Hold conditions. This test can be best described as a "Toggle" test run at the maximum device specified frequency.
3. AC Parametric Measurements
   - A) Signetics has upgraded the AC specifications of the gold-doped (TTL), Low Power Schottky (LS) and Schottky (S) devices by adding in 50pF limit tables that apply over temperature. The data sheet indicates that these new limits are presently guaranteed, but Signetics Military Group is generating and implementing test capabilities and will be actually performing these new limit conditions within the next year. During the interim, Signetics will be performing testing to either the 15pF or 50pF output load and limits specified. Currently the ATE (Automatic Test equipment) being employed actually have test head/load board capacitances that exceed 50pF.
   - B) While performing any specific AC test (e.g., t_{PLH}), test conditions not intended to be measured at this point, but which could affect the result due to the testing environment will be set at a non-critical condition (e.g., setup and hold). In other words, critical (spec) test conditions will be generally restricted to only the parameter under test.
4. I_{CC} Measurements
   - A) The input voltage conditions while performing this test is either greater than or equal to 4.0V (High State) or equal to Ground (Low State). Any I_{CC} measurement which requires clocking will be so noted in the data sheet.

Signetics

Military Products

Section 2
EPROM Data Sheets

INDEX

Signetics

27C64A

64K CMOS UV Erasable PROM (8K × 8)

Product Specification

Military Application Specific Products

DESCRIPTION

The Signetics 27C64A CMOS EPROM is 64K-Bit 5V only memory organized as 8192 words of 8 bits, employing advanced CMOS circuitry for systems requiring high-power, high performance speeds and immunity to noise

The 27C64A has a non-multiplexed addressing interface and is pin compatible with the standard 2764.

The 27C64A achieves both high performance (200ns access time) and low power consumption (10mA active current maximum, CMOS inputs) making it ideal for high performance portable equipment.

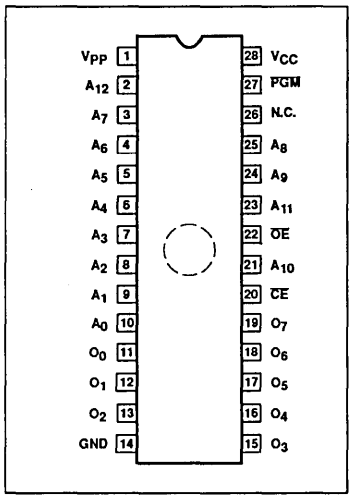
The highest degree of protection against latch-up is achieved through EPI (Epitaxial) processing. Prevention of latch-up is provided for stresses up to 100mA on address and data pins for -1V to V_{CC} + 1V.

The 27C64A is programmed with standard EPROM programmers and the intelligent programming algorithm may be utilized.

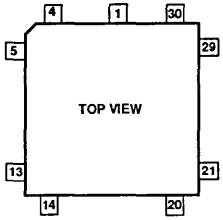
FEATURES

- **CMOS microcontroller and microprocessor compatible**
  - **Universal 28- and 32-Pin memory site, 2-line control**
- **Low power consumption**
  - **10mA maximum active current**
  - **100μA maximum standby current**
- **Noise immunity features**
  - **±10% supply voltage**
  - **Maximum latch-up immunity through epitaxial processing**
- **Fast, reliable intelligent programming**
  - **Programs in under one minute**
  - **12.5V_{PP}**

CERDIP PIN CONFIGURATION



LLCC PIN CONFIGURATION



PIN / FUNCTION

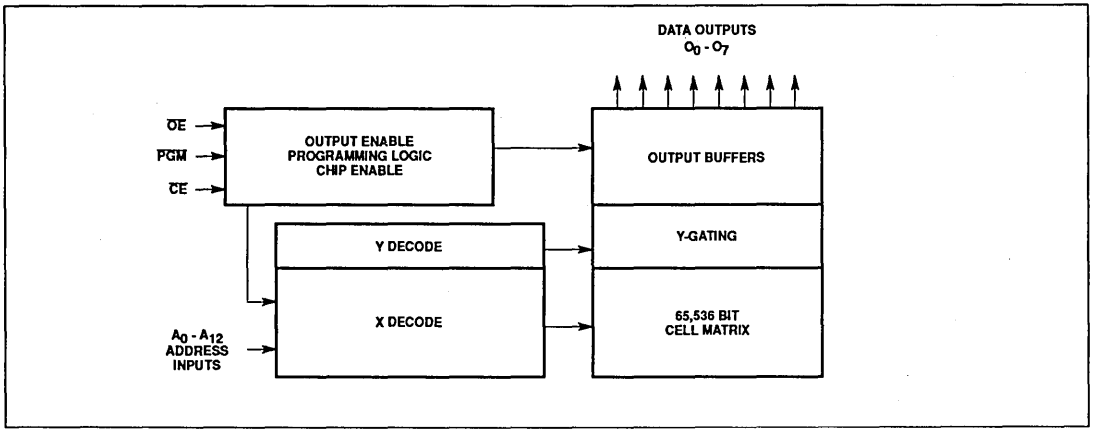
1	NC	12	NC	23	$\overline{CE}$
2	V_{PP}	13	O_0	24	A_{10}
3	A_{12}	14	O_1	25	$\overline{OE}$
4	A_7	15	O_2	26	NC
5	A_6	16	V_{SS}	27	A_{11}
6	A_5	17	NC	28	A_9
7	A_4	18	O_3	29	A_8
8	A_3	19	O_4	30	NC
9	A_2	20	O_5	31	$\overline{PGM}$
10	A_1	21	O_6	32	V_{CC}
11	A_0	22	O_7		

PIN NAMES

A_0 - A_{12}	Addresses
O_0 - O_7	Outputs
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{PGM}$	Program Strobe
NC	No connect
GND	Ground
V_{PP}	Program Voltage
V_{CC}	Power Supply

64K CMOS UV Erasable PROM (8K×8) — 27C64A

BLOCK DIAGRAM



ORDERING INFORMATION

PACKAGES	ORDER CODE			
	150ns	200ns	250ns	350ns
28-Pin Ceramic DIP w/Quartz Window	27C64A/BXA-15	27C64A/BXA-20	27C64A/BXA-25	27C64A/BXA-35
28-Pin Ceramic DIP w/o Quartz Window[1]	27C64A/BXA-15 OT	27C64A/BXA-20 OT	27C64A/BXA-25 OT	27C64A/BXA-35 OT
32-Pin Rectangular LLCC w/Quartz Window	27C64A/BUA-15	27C64A/BUA-20	27C64A/BUA-25	27C64A/BUA-35

ABSOLUTE MAXIMUM RATINGS[2]

SYMBOL	PARAMETER	RATING	UNIT
T_{STG}	Storage temperature range	-65 to +125	°C
V_I, V_O	Voltage on any pin with respect to ground	-2.0 to V_{CC} +7V	V
V_I	Voltage on $\overline{CE}$ pin with respect to ground	-2.0 to +13.5	V
V_{PP}	Supply voltage with respect to ground during programming	-2.0 to 14.0	V
T_C	Operating temperature during read	-55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}[3]	High-level input voltage		2.0		V_{CC} + 0.5[9]	V
V_{IH}[3]	High-level input voltage CMOS	$V_{PP} = V_{CC}$	V_{CC} - 0.2		V_{CC} + 0.2[9]	V
V_{IL}[3]	Low-level input voltage	$V_{PP} = V_{CC}$	-0.5[9]		0.8	V
V_{IL}[3]	Low-level input voltage CMOS	$V_{PP} = V_{CC}$	-0.2[9]		0.2	V
I_{OH}	High-level output current				-400	µA
I_{OL}	Low-level output current				2.1	mA
V_{PP}	V_{PP} read voltage[8]		V_{CC} - 0.7		V_{CC}	V
T_A	Operating temperature range		-55		+125	°C

64K CMOS UV Erasable PROM (8K×8) — 27C64A

DC ELECTRICAL CHARACTERISTICS -55 °C ≤ T_C ≤ + 125°C, V_{CC} = 5V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS	27C64A-15, -20, -25			27C64A-35			UNIT
			Min	Typ[4]	Max	Min	Typ[4]	Max	
I_{LIH}	Input leakage current	$V_I = V_{CC}$ = Max		0.01	+1.0		0.01	+1.0	µA
I_{LIL}		V_I = 0.0V			-1.0			-1.0	
I_{OIH}	Output leakage current	$V_I = V_{CC}$ = Max		0.01	+1.0		0.01	+1.0	µA
I_{OIL}		V_I = 0.0V			-1.0			-1.0	
I_{CC}[5,7] TTL	Operating supply current TTL inputs	$\overline{CE} = \overline{OE} - V_{IL}$, $V_{PP} = V_{CC}$, O_{0-7} = 0mA			30.0			25.0	mA
I_{CC}[5,7] CMOS	Operating supply current	$\overline{CE} = \overline{OE} - V_{IL}$, $V_{PP} = V_{CC}$ = Max, O_{0-7} = 0mA			10.0			10.0	mA
I_{SB}[5] TTL	Standby supply current TTL inputs	$\overline{CE} = V_{IH}$, V_{CC} = Max			1.0			1.0	mA
I_{SB}[5,6] CMOS	Standby supply current CMOS inputs	$\overline{CE} = V_{CC}$ = Max			100.0			140.0	µA
I_{PP}[7]	V_{PP} read current	$V_{PP} = V_{CC}$ = Max			100.0			100.0	µA
V_{IL} V_{IL}	Input Low voltage (TTL) Input Low voltage (CMOS)	$V_{PP} = V_{CC}$ = Max $V_{PP} = V_{CC}$ = Max	-0.5[10] -0.2[10]		+0.8 +0.2	-0.5[10] -0.2[10]		+0.8 +0.2	V V
V_{IH}	Input High voltage	$V_{PP} = V_{CC}$ = Min	2.0		V_{CC} + 0.5[10]	2.0		V_{CC} + 0.5[10]	V
V_{IH}	Input High voltage (CMOS)	$V_{PP} = V_{CC}$ = Min	V_{CC} - 0.2		V_{CC} + 0.2[10]	V_{CC} - 0.2		V_{CC} + 0.2[10]	V
V_{OL}	Output Low voltage	I_{OL} = Max, V_{CC} = Min			0.45			0.45	V
V_{OH}	Output High voltage	I_{OH} = Max, V_{CC} = Min	2.4			2.4			V
I_{OS}[8]	Output short-circuit current	V_{CC} = Max			-100.0			-100.0	mA

CAPACITANCE T_A = 25°C, f = 1.0MHz[10]

SYMBOL	PARAMETER	TEST CONDITIONS	MAX	UNIT
C_I	Address/control capacitance	V_I = 0V	6	pF
C_O	Output capacitance	V_O = 0V	12	pF

READ MODES

MODE	PINS				
	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	OUTPUTS (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_O
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X[12]	X[12]	V_{CC}	Hi-Z

READ MODE

The 27C64A has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C64A has a Standby mode which reduces the maximum V_{CC} current to 100µA. The device is placed in the Standby mode when $\overline{CE}$ pin is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

64K CMOS UV Erasable PROM (8K×8) — 27C64A

READ OPERATION - AC CHARACTERISTICS $-55\,°C \leq T_C \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

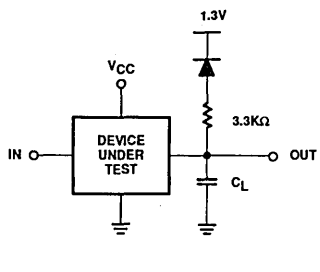
VERSIONS		27C64A-15		27C64A-20		27C64A-25		27C64A-35		UNIT
SYMBOL	CHARACTERISTIC[11]	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to output delay		150		200		250		350	ns
t_{CE}	$\overline{CE}$ to output delay		150		200		250		350	ns
t_{OE}	$\overline{OE}$ to output delay		65		75		100		120	ns
t_{OP}[10]	$\overline{OE}$ or $\overline{CE}$ High to output Hi-Z		40		55		55		75	ns
t_{OH}[10]	Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ change - whichever is first	0		0		0		0		ns

ERASURE CHARACTERISTICS

The recommended erasure procedure for the 27C64A is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15Wsec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000µW/cm² power rating. The 27C64A should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C64A can be exposed to without damage is 7258µW/cm² (1 week @ 12,000Wsec/cm²). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

The erasure characteristics of the 27C64A are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C64A in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C64A is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

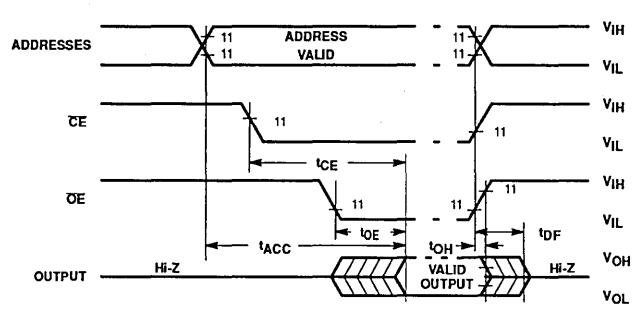
AC TESTING LOAD CIRCUIT



NOTE:
C_C = 100pF AND INCLUDES JIG CAPACITANCE

Figure 1. Test Configuration

AC WAVEFORMS



Input Pulse Characteristics: $t_r, t_f \leq 5ns$, P_{RR} = 1MHz; for measurement points see Note 11.

PROGRAMMING MODES

MODES	PINS							
	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	A_9 (24)	A_0 (10)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
Intelligent programming	V_{IL}	V_{IH}	V_{IL}	X[12]	X[12]	V_{PP}	6.0V[15]	D_1
Program verify	V_{IH}	V_{IL}	V_{IH}	X[12]	X[12]	V_{PP}	6.0V[15]	D_0
Program inhibit	V_{IH}	V_{IH}	X	X[12]	X[12]	V_{PP}	6.0V[15]	Hi-Z
Intelligent identifier-manufacturer[14]	V_{IL}	V_{IL}	V_{IL}	V_H[13]	V_{IL}	V_{CC}	V_{CC}	15H
Intelligent identifier[14]	V_{IL}	V_{IL}	V_{IL}	V_H[13]	V_{IH}	V_{CC}	V_{CC}	OBH

64K CMOS UV Erasable PROM (8K×8) — 27C64A

CMOS NOISE CHARACTERISTICS

Special epitaxial processing techniques have enabled Signetics to build CMOS with features adding to system reliability. These include Input/Output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100mA and voltages from -1V to V_{CC} + 1V.

Additionally, the V_{PP} (Programming) pin is designed to resist latch-up to the 14V maximum device limit.

PROGRAMMING

Caution: Exceeding 14.0V on V_{PP} pin may permanently damage the 27C64A.

Initially, and after each erasure, all bits of the 27C64A are in the "1" state. Data is introduced by selectively programming "0" into the desired bit locations. Although only "0" will be programmed, both "1" and "0" can be present in the data word. The only way to change an "0" to a "1" is by ultraviolet light erasure.

The 27C64A is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

INTELLIGENT PROGRAMMING ALGORITHM

The 27C64A intelligent programming algorithms rapidly program Signetics CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of five minutes. Actual programming times may vary due to differences in programming equipment.

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flow-chart of the 27C64A intelligent program algorithm is shown in Figure 2.

The intelligent programming algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{PGM}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3Xms. X is a duration counter and is equal to the number of the initial 1ms pulses applied to a particular 27C64A location, before a correct verify occurs. Up to 25 1ms pulses per byte are provided for before the overprogram is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V.

When the intelligent programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5.0V.

PROGRAM INHIBIT

Programming of multiple 27C64A EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits other 27C64A EPROMs from being programmed.

Except for $\overline{CE}$, all inputs of the parallel 27C64A's may be common. A TTL low-level pulse applied to the $\overline{PGM}$ and $\overline{CE}$ input with V_{PP} at 12.5V will program the selected 27C64A.

VERIFY

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL} and $\overline{PGM}$ at V_{IH}. Data should be verified a minimum of T_{OEV} after the falling edge of $\overline{OE}$.

INTELLIGENT IDENTIFIER MODE

The intelligent identifier mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27C64A.

To activate this mode the programming equipment must force 11.5V to 12.5V on address line A_9 of the 27C64A. Two bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during intelligent identifier mode.

INTELLIGENT PROGRAMMING ALGORITHM DC PROGRAMMING CHARACTERISTICS

T_A = 25°C ± 5°C, V_{CC} = 6.0V ± 0.25V, V_{PP} = 12.5V ± 0.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
I_I	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input low level (all inputs		-0.1	0.8	V
V_{IH}	Input High level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low voltage during verify	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High voltage during verify	I_{OH} = -2.5mA	3.5		V
I_{CC2}	V_{CC} supply current	$O_0 - O_7$ = 0mA		30	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		30	mA

AC PROGRAMMING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS[16]	LIMITS			UNIT
			Min	Typ	Max	
t_{CES}	$\overline{CE}$ setup time		2			µs
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP}[19]	$\overline{OE}$ High to output float delay		0		130	µs
t_{VPS}	V_{PP} setup time		2			µs
t_{VCS}	V_{CC} setup time		2			µs
t_{PW}	$\overline{PGM}$ initial program pulse width	(See note 17)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{PGM}$ overprogram pulse width	(See note 18)	2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

NOTES:
1. Erase characteristics do not apply for one time programming (OT).
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Minimum DC input voltage is -0.5V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Typical limits are at V_{CC} = 5V, T_A = + 25°C.
5. TTL inputs: spec V_{IL}, V_{IH} levels;
   CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
6. $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
7. Maximum active power usage is the sum I_{PP} + I_{CC}.
8. Output shorted for no more than one second. No more than one output shorted at a time.
9. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}.
10. Guaranteed, but not tested.
11. AC characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V. Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.
12. X can be V_{IL} or V_{IH}.
13. V_H = 12.0V ± 0.5V.
14. A_1 - A_8, A_{10} - A_{12} = V_{IL}.
15. V_{CC} = 6.0V ± 0.25V.
16. AC Conditions of Test:
    Input Rise and Fall Times (100% to 90%): 20ns
    Input Pulse Levels: 0.45V to 2.4V
    Input Timing Reference Level: 0.8V to 2.0V
    Output Timing Reference Level: 0.8V to 2.0V
17. Initial Program Pulse width tolerance is 1msec ± 5%.
18. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
19. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven (see Timing Diagram).

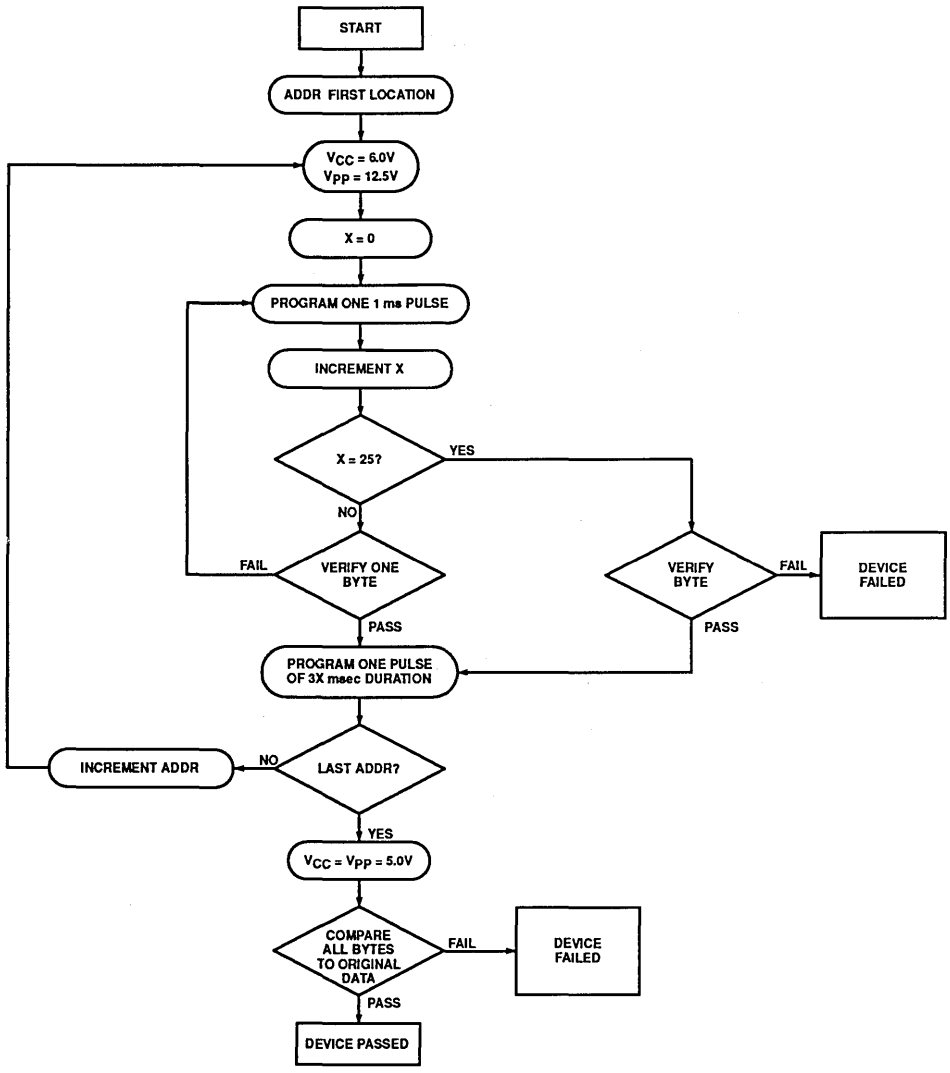
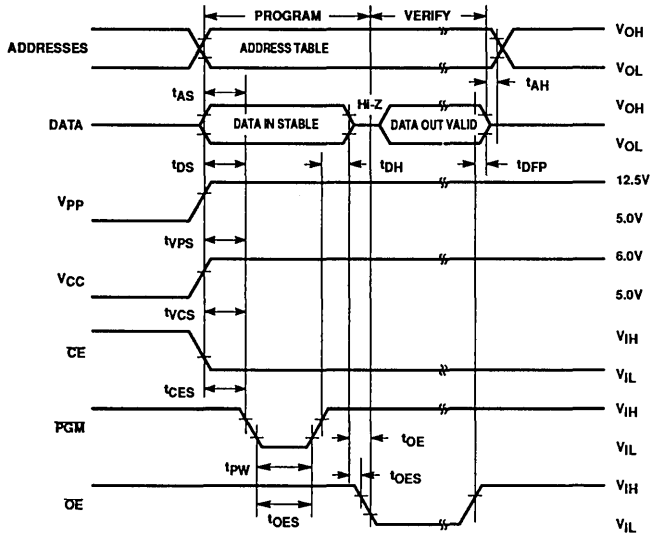


Figure 2. Intelligent Programming Flowchart



NOTES:

1. The Input Timing Regerence Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming 27C64A, a 0.1uF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

Figure 3. Intelligent Programming Waveform

Signetics

27C256

256K CMOS UV Erasable PROM (32K × 8)

Product Specification

Military Application Specific Products

DESCRIPTION

The Signetics 27C256 CMOS EPROMs are 256K-Bit 5V only memories organized as 32,768 words of 8 bits. They employ advanced CMOS circuitry for systems requiring low-power, high-performance speeds and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug compatible with the industry standard 27256.

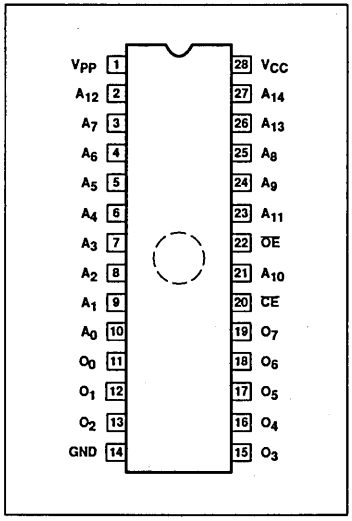
The 27C256 achieves both high-performance and low power consumption (10mA active current maximum, CMOS inputs), making them ideal for high-performance, portable equipment.

It is programmed with standard EPROM programmers and the intelligent programming algorithm may be utilized.

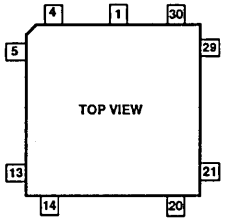
FEATURES

- **CMOS/NMOS microcontroller and microprocessor compatible**
  - **Universal 28- or 32-Pin memory site, 2-line control**
- **Low power consumption**
- **Noise Immunity features**
  - **±10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**
- **Fast, reliable intelligent programming**
  - **12.5V V_{PP}, HCMOS 11-E compatible**

CERDIP PIN CONFIGURATION



LLCC PIN CONFIGURATION



PIN/FUNCTION

1	NC	12	NC	23	$\overline{OE}$
2	V_{PP}	13	O_0	24	A_{10}
3	A_{12}	14	O_1	25	$\overline{CE}$
4	A_7	15	O_2	26	NC
5	A_6	16	V_{SS}	27	A_{11}
6	A_5	17	NC	28	A_9
7	A_4	18	O_3	29	A_8
8	A_3	19	O_4	30	A_{13}
9	A_2	20	O_5	31	A_{14}
10	A_1	21	O_6	32	V_{CC}
11	A_0	22	O_7		

PIN NAMES

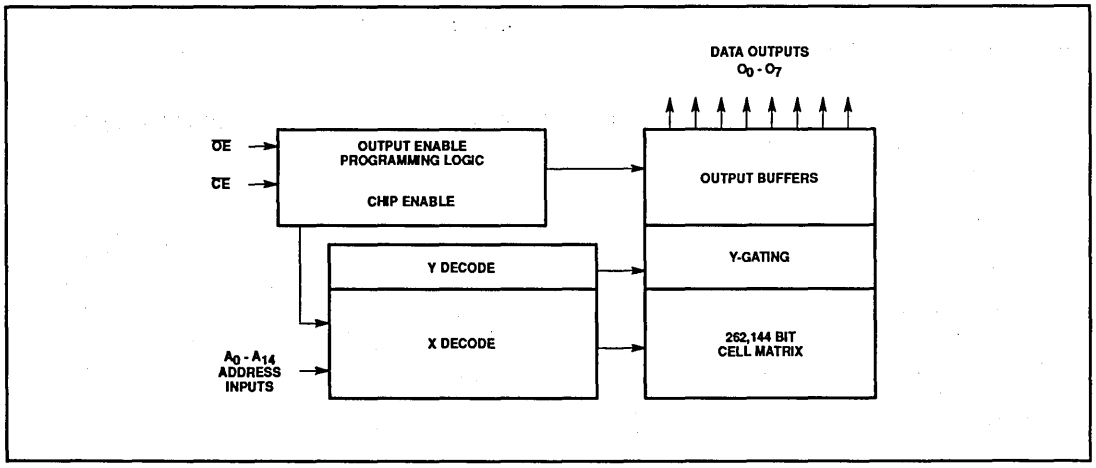
A_0 - A_{14}	Addresses
O_0 - O_7	Outputs
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
GND	Ground
V_{PP}	Program Voltage
V_{CC}	Power Supply

ORDERING INFORMATION

PACKAGES	ORDER CODE		
	150ns	200ns	250ns
28-Pin Ceramic DIP w/Quartz Window	27C256/BXA-15	27C256/BXA-20	27C256/BXA-25
28-Pin Ceramic DIP w/o Quartz Window[1]	27C256/BXA-15 OT	27C256/BXA-20 OT	27C256/BXA-25 OT
32-Pin Rectangular LLCC w/Quartz Window	27C256/BUA-15	27C256/BUA-20	27C256/BUA-25

256K CMOS UV Erasable PROM (32K x 8) 27C256

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[2]

SYMBOL	PARAMETER	RATING	UNIT
T_{STG}	Storage temperature range	-65 to +150	°C
V_I, V_O	Voltage on any pin with respect to ground	-2.0 to V_{CC} +7V	V
V_I	Voltage on $\overline{CE}$ Pin with respect to ground	-2.0 to +13.5	V
V_{PP}	Supply voltage with respect to ground during programming	-2.0 to 14.0	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}[3]	High-level input voltage	2.0		V_{CC} + 0.5[12]	V
V_{IH}[3]	High-level input voltage CMOS $V_{PP} = V_{CC}$	V_{CC} - 0.2		V_{CC} + 0.2[12]	V
V_{IL}[3]	Low-level input voltage $V_{PP} = V_{CC}$	-0.5[12]		0.8	V
V_{IL}[3]	Low-level input voltage CMOS $V_{PP} = V_{CC}$	-0.2[12]		0.2	V
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			2.1	mA
V_{PP}	V_{PP} read voltage [8]	V_{CC} - 0.7		V_{CC}	V
T_A	Operating temperature range	-55		+125	°C

256K CMOS UV Erasable PROM (32K x 8) 27C256

READ OPERATION DC CHARACTERISTICS $-55\,°C \leq T_A \leq +125°C$, $V_{CC} = 5V \pm 10\%$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[4]	Max	
I_{LIH}	Input leakage current	$V_I = V_{CC}$ = Max		0.01	+1.0	µA
I_{LIL}		V_I = 0.0V			-1.0	µA
I_{OIH}	Output leakage current	$V_I = V_{CC}$ = Max		0.01	+1.0	µA
I_{OIL}		V_I = 0.0V			-1.0	µA
$I_{CC}TTL$[6,8]	Operating current TTL inputs	$\overline{CE} = \overline{OE}$ - V_{IL}, $V_{PP} = V_{CC}$ - Max $O_0 - O_7$ = 0mA			30	mA
$I_{CC}CMOS$[6,8]	Operating current CMOS inputs	$\overline{CE} = \overline{OE}$ - V_{IL}, $V_{PP} = V_{CC}$ - Max $O_0 - O_7$ = 0mA			10	mA
$I_{SB}TTL$[8]	Standby current TTL inputs	$\overline{CE} = V_{IH}$			2	mA
$I_{SB}CMOS$[5]	Standby current CMOS inputs	$\overline{CE} = V_{IH}$			100	µA
I_{PP}[8]	V_{PP} read current	$V_{PP} = V_{CC}$ = Max			200	µA
V_{IL}[9]	Input Low voltage (TTL) Input Low voltage (CMOS)	$V_{PP} = V_{CC}$	-0.5[10] -0.2[10]		0.8 0.2	V V
V_{IH}[9]	Input High voltage (TTL) Input High voltage (CMOS)	$V_{PP} = V_{CC}$	2.0 V_{CC} -0.2		V_{CC} + 0.5[10] V_{CC} + 0.2[10]	V V
V_{OL}	Output Low voltage	I_{OL} = Max			0.45	V
V_{OH}	Output High voltage	I_{OH} = Max	2.4			V
I_{OS}[7]	Output short-circuit current				-100	mA

CAPACITANCE T_A = 25°C, f = 1.0MHz

SYMBOL	PARAMETER	TEST CONDITIONS	MAX	UNIT
C_I[10]	Address/control capacitance	V_I = 0V	6	pF
C_O[10]	Output capacitance	V_O = 0V	12	pF

READ MODES

MODE	PINS			
	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	OUTPUTS (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{CC}	D_O
Output disable	V_{IL}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X	V_{CC}	Hi-Z

256K CMOS UV Erasable PROM (32K x 8) — 27C256

READ MODE

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of $t_{\overline{OE}}$ from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

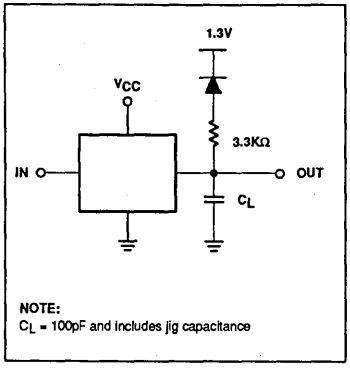
STANDBY MODE

The 27C256 has a Standby mode which reduces the maximum CMOS V current to 100µA. The device is placed in the Standby mode when Pin 20 is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

READ OPERATION - AC CHARACTERISTICS $-55\,°C \leq T_A \leq +125°C,\ 4.5V \leq V_{CC} \leq 5.5V$[12]

SYMBOL	PARAMETER	27C256-15		27C256-20		27C256-25		UNIT
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to output delay		150		200		250	ns
t_{CE}	$\overline{CE}$ to output delay		150		200		250	ns
t_{OE}	$\overline{OE}$ to output delay		65		75		100	ns
t_{DF}[10]	$\overline{OE}$ or $\overline{CE}$ High to output Hi-Z		45		55		60	ns
t_{OH}[10]	Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ change - whichever is first	0		0		0		ns

AC TESTING LOAD CIRCUIT



NOTE:
C_L = 100pF and includes jig capacitance

SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer - the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the devices. The associated transient voltage peaks can be suppressed by complying with Two-Line Control and by properly selected decoupling capacitors.

It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PC board traces.

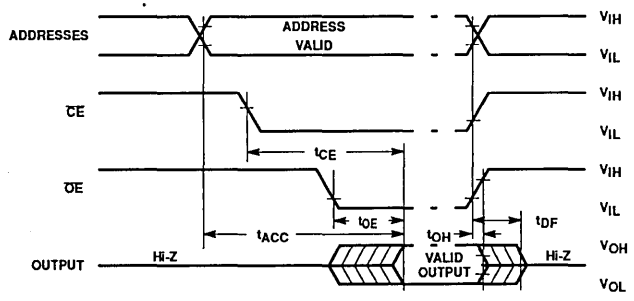
ERASURE CHARACTERISTICS

The erasure characteristics of the 27C256 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å Range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C256 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C256 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 27C256 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The 27C256 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C256 can be exposed to without damage is 7258W/cm^2 (1 week @ 1200µW/cm^2). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

256K CMOS UV Erasable PROM (32K x 8) 27C256

AC WAVEFORMS



Input Pulse Characteristics: t_r, $T_f \leq 5ns$, P_{RR} = 1MHz

PROGRAMMING MODES

MODES	PINS						
	$\overline{CE}$ (20)	$\overline{OE}$ (22)	A_9 (24)	A_0 (10)	V_{PP} (1)	V_{CC} (28)	OUTPUTS (11-13, 15-19)
Intelligent programming	V_{IL}	V_{IH}	X^{13}	X^{13}	V_{PP}	6.0V[16]	D_1
Program verify	V_{IH}	V_{IL}	X^{13}	X^{13}	V_{PP}	6.0V[16]	D_2
Program inhibit	V_{IH}	V_{IH}	X^{13}	X^{13}	V_{PP}	6.0V[16]	Hi-Z
Intelligent identifier-manufacturer[15]	V_{IL}	V_{IL}	V_H[14]	V_{IL}	V_{CC}	V_{CC}	15H
Intelligent identifier[15]	V_{IL}	V_{IL}	V_H[14]	V_{IH}	V_{CC}	V_{CC}	8CH

CMOS NOISE CHARACTERISTICS

Special epitaphial processing techniques have enabled Signetics to build CMOS with features adding to system reliability. These include Input/Output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100mA and voltages from -1V to V_{CC} + 1V.

Additionally, the V_{PP} (Programming) pin is designed to resist latch-up to the 14V maximum device limit.

PROGRAMMING

Caution: Exceeding 14.0V on V_{PP} Pin may permanently damage the 27C256.

Initially, and after each erasure, all bits of the 27C256 are in the "1" state. Data is introduced by selectively programming "0" into the desired bit location. Although only "0" will be programmed, both "1" and "0" can be present in the data word. The only way to change an "0" to a "1" is by ultraviolet light erasure.

The 27C256 is in the programming mode when the V_{PP} input is at 12.5V and $\overline{CE}$ is at TTL-Low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

INTELLIGENT PROGRAMMING™ ALGORITHM

The 27C256 intelligent programming algorithms rapidly program Signetics CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of five minutes. Actual programming times may vary due to differences in programming equipment.

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flow-chart of the 27C256 intelligent program algorithm is shown in Figure 1.

The intelligent programming algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3Xms. X is a duration counter and is equal to the number of the initial 2ms pulses applied to a particular 27C256 location, before a correct verify occurs. Up to 25 1ms pulses per byte are provided for before the overprogram is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V.

When the intelligent programming cycle has been completed, all bytes should be compared to the original data with V_{CC} = 5.0V.

PROGRAM INHIBIT

Programming of multiple 27C256 EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits other 27C256 EPROMs from being programmed.

Except for $\overline{OE}$ or $\overline{CE}$, all inputs of the parallel 27C256s may be common. A TTL low-level pulse applied to the $\overline{CE}$ or ALE/$\overline{CE}$ input with V_{PP} at 12.5V will program the selected 27C256.

VERIFY

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at V_{IL} and $\overline{CE}$ at V_{IH} and V_{PP} at 12.5V.

Data should be verified a minimum of T_{OEV} after the falling edge of $\overline{OE}$.

256K CMOS UV Erasable PROM (32K x 8) 27C256

INTELLIGENT IDENTIFIER MODE

The intelligent identifier mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27C256.

To activate this mode the programming equipment must force 11.5V to 12.5V on address line A_9 of the 27C256. Two bytes may then be sequenced from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during intelligent identifier mode.

INTELLIGENT PROGRAMMING ALGORITHM DC PROGRAMMING CHARACTERISTICS

T_A = 25°C ± 5°C, V_{CC} = 6.0V ± 0.25V, V_{PP} = 12.5V ± 0.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
I_{IH}	Input current (all inputs)	$V_{IN} = V_{IL}$ or V_{IH}		1.0	µA
V_{IL}	Input Low level (all inputs)		-0.1	0.8	V
V_{IH}	Input High level		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low voltage during verify	I_{OL} = 2.1mA		0.45	V
V_{OH}	Output High voltage during verify	I_{OH} = -2.5mA	3.5		V
I_{CC2}	V_{CC} supply current	$O_0 - O_7$ = 0mA		30	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		50	mA

AC PROGRAMMING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS[17]	LIMITS			UNIT
			Min	Typ	Max	
t_{CES}	$\overline{CE}$ setup time		2			µs
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP}[20]	$\overline{OE}$ High to output float delay		0		130	µs
t_{VPS}	V_{PP} setup time		2			µs
t_{VCS}	V_{CC} setup time		2			µs
t_{PW}	$\overline{CE}$ initial program pulse width	(See note 18)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ overprogram pulse width	(See note 19)	2.85		78.75	ms
t_{OE}	Data valid from $\overline{OE}$				150	ns

NOTES:

1. Erase characteristics do not apply for one time programming (OT).
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Minimum DC input voltage is -0.5V. during transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Typical limits are at V_{CC} = 5V, T_A = + 25°C.
5. Other inputs can have any value within spec.
6. Maximum active power usage is the sum $I_{PP} + I_{CC}$ and is measured at 5MHz.
7. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
8. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}. Also, V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
9. TTL inputs: spec TTL at V_{IL}, V_{IH} levels. CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
10. Guaranteed, but not tested.
11. X can be V_{IH} or V_{IL}.
12. AC characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V. Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.
13. X can be V_{IL} or V_{IH}.
14. V_H = 12.0V ± 0.5V.
15. $A_1 - A_9$, $A_{10} - A_{12} = V_{IL}$.

16. V_{CC} = 6.0V ± 0.25V.
17. AC Conditions of Test:
    Input Rise and Fall Times (100% to 90%): 20ns
    Input Pulse Levels: 0.45V to 2.4V
    Input Timing Reference Level: 0.8V to 2.0V
    Output Timing Reference Level: 0.8V to 2.0V
18. Initial Program Pulse width tolerance is 1msec ± 5%.
19. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
20. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven (see Timing Diagram).

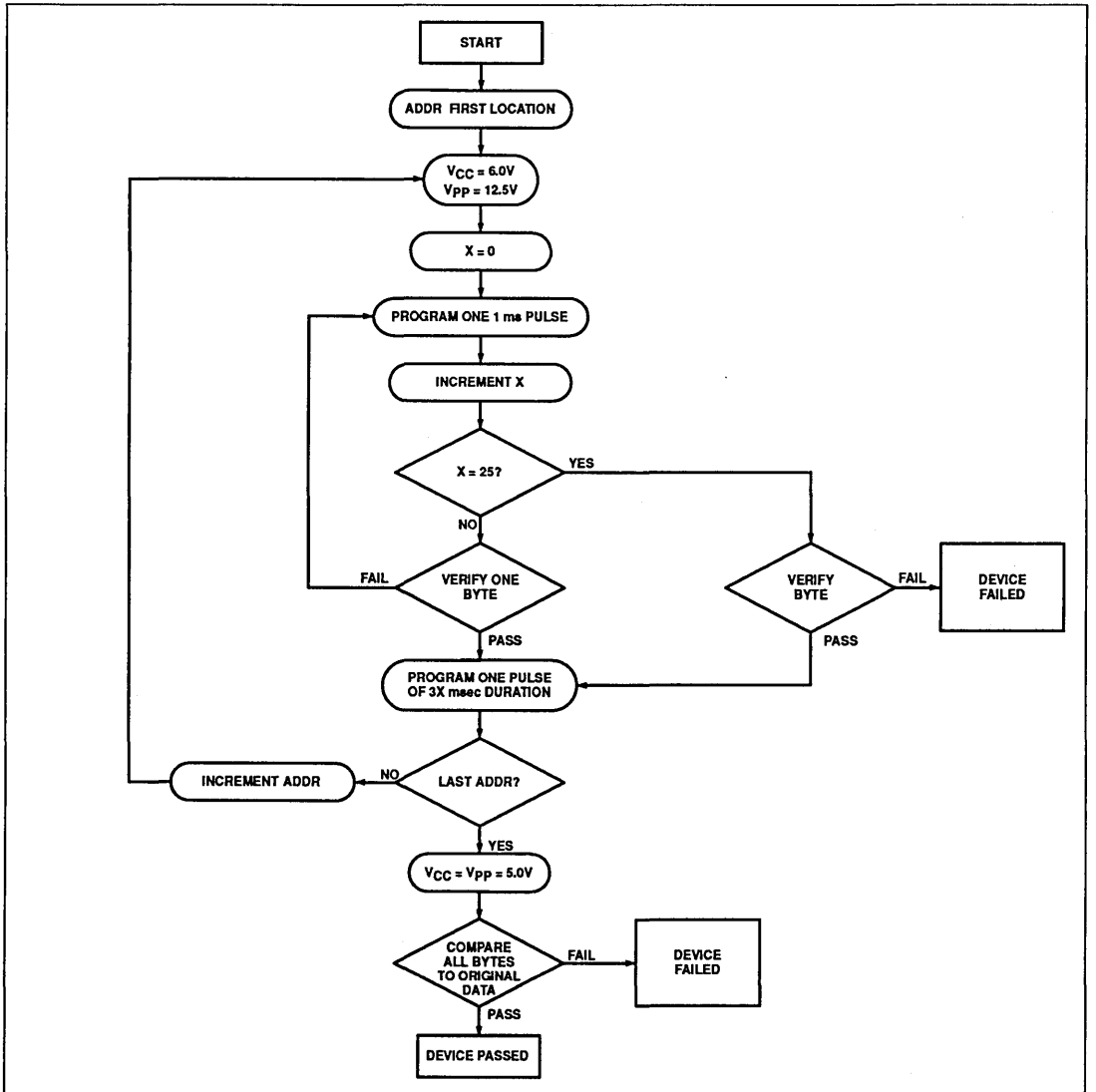
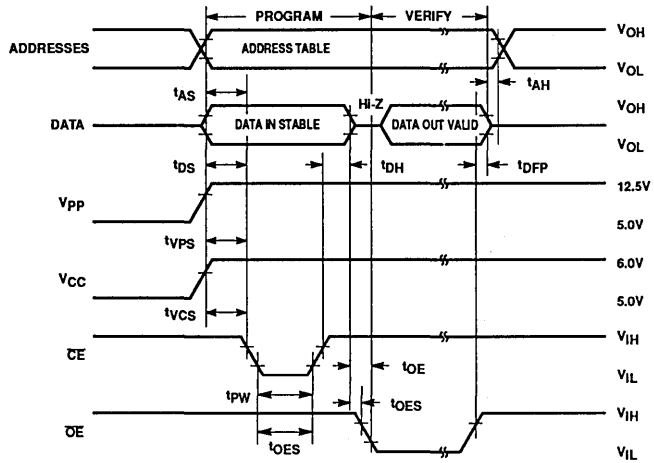


Figure 1. Intelligent Programming Flowchart



NOTES:
1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}, input pulse levels are 0.45V and 2.4V.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming 27C256, a 0.1uF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.

Figure 2. Intelligent Programming Waveforms

Signetics

27C512
512K CMOS UV Erasable PROM (64K × 8)

Military Standard Products

Product Specification

DESCRIPTION

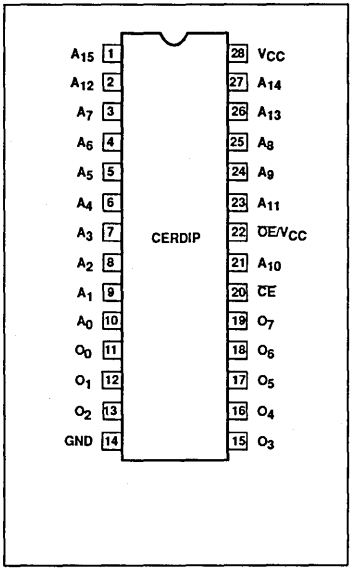
The Signetics 27C512 CMOS EPROM is a 512K-bit, 5V-only memory organized as 65,536 words of 8 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds and immunity to noise. The 27C512 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27512.

The 27C512, available in a ceramic DIP package, achieves both high performance and low power consumption, making it ideal for high-performance, portable equipment. This device can be programmed with standard EPROM programmers.

FEATURES

- **CMOS/NMOS microcontroller and microprocessor compatible**
  - **Universal 28-pin memory site, 2-line control**
- **Low power consumption**
- **Noise Immunity features**
  - **±10% V_{CC} tolerance**
  - **Maximum latch-up immunity through epitaxial processing**
- **Fast, reliable intelligent programming**
  - **12.5V V_{PP}, HCMOS 11-E compatible**

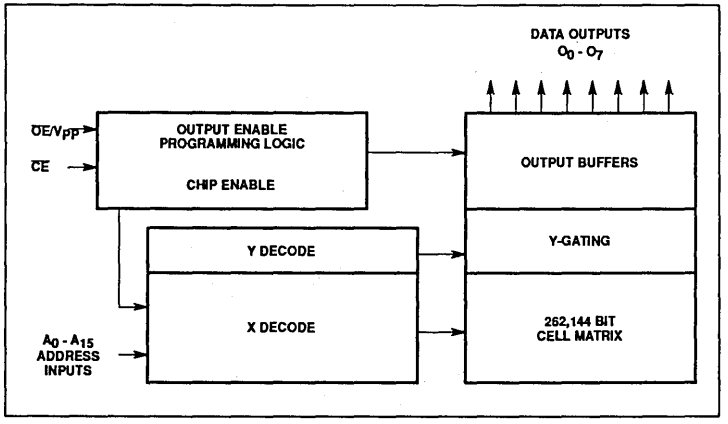
PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	ORDER CODE		
	170ns	200ns	250ns
28-Pin Ceramic DIP w/Quartz Window	27C512/BXA-17	27C512/BXA-20	27C512/BXA-25

BLOCK DIAGRAM



PIN NAMES

$A_0 - A_{15}$	Addresses
$O_0 - O_7$	Outputs
$\overline{OE}/V_{CC}$	Output Enable/ Programming Voltage
$\overline{CE}$	Chip Enable
GND	Ground
V_{CC}	Power Supply

512K CMOS UV Erasable PROM (64K×8) — 27C512

ABSOLUTE MAXIMUM RATINGS[2]

SYMBOL	PARAMETER	RATING	UNIT
T_{STG}	Storage temperature range	-65 to +150	°C
V_I, V_O	Voltage on any pin with respect to ground	-2.0 to V_{CC} +1.0	V
V_I	Voltage on $\overline{CE}$ Pin with respect to ground	-2.0 to +13.5	V
V_{PP}	Supply voltage with respect to ground during programming	-2.0 to 14.0	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}[3,9]	High-level input voltage	2.0		V_{CC} +0.5[12,10]	V
V_{IH}[3,9]	High-level input voltage CMOS	V_{CC} -0.2		V_{CC} +0.2[12,10]	V
V_{IL}[3,9]	Low-level input voltage	-0.5[12,10]		0.8	V
V_{IL}[3,9]	Low-level input voltage CMOS	-0.2[12,10]		0.2	V
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			2.1	mA
T_A	Operating temperature range	-55		+125	°C

READ OPERATION DC CHARACTERISTICS -55 °C ≤ T_A ≤ + 125°C, V_{CC} = 5V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[4]	Max	
I_{LIH}	Input leakage current	$V_I = V_{CC}$ = Max		0.01	10	µA
I_{LIL}		V_I = 0.0V, V_{CC} = Max			-10	µA
I_{OIH}	Output leakage current	$V_I = V_{CC}$ = Max		0.01	+1.0	µA
I_{OIL}		V_I = 0.0V, V_{CC} = Max			-1.0	µA
$I_{CC}TTL$[6,8]	Operating current TTL inputs	$\overline{CE}$ = $\overline{OE}$ - V_{IL}, $V_{PP} = V_{CC}$ = Max O_0 - O_7 = 0mA, f = $1/T_{ACC\ Max}$			30	mA
$I_{SB}TTL$[8]	Standby current TTL inputs	$\overline{CE} = V_{IH}$, V_{CC} = Max			2	mA
$I_{SB}CMOS$[5]	Standby current CMOS inputs	$\overline{CE} = V_{IH}$, V_{CC} = Max			100	µA
V_{OL}	Output Low voltage	I_{OL} = Max, V_{CC} = Min			0.45	V
V_{OH}	Output High voltage	I_{OH} = Max, V_{CC} = Min	2.4			V
I_{OS}[7]	Output short-circuit current	V_{CC} = Max, I_O = 0V			-100	mA

CAPACITANCE T_A = 25°C, f = 1.0MHz

SYMBOL	PARAMETER	CONDITIONS	MAX	UNIT
C_I[10]	Address/control capacitance	V_I = 0V	6	pF
C_O[10]	Output capacitance	V_O = 0V	12	pF
C_{IN}[10]	$\overline{OE}/V_{PP}$	V_I = 0V	25	pF

512K CMOS UV Erasable PROM (64K×8) — 27C512

READ OPERATION – AC CHARACTERISTICS $-55\,°C \leq T_A \leq +125°C, 4.5V \leq V_{CC} \leq 5.5V$[12]

SYMBOL	PARAMETER	27C512-17		27C512-20		27C512-25		UNITS
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to output delay		170		200		250	ns
t_{CE}	$\overline{CE}$ to output delay		170		200		250	ns
t_{OE}	$\overline{OE}$ to output delay		60		75		100	ns
t_{OP}[10]	$\overline{OE}$ or $\overline{CE}$ High to output Hi-Z		50		55		60	ns
t_{OH}[10]	Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ change - whichever is first	0		0		0		ns

NOTES:
1. Erase characteristics do not apply for one time programming (OT).
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Minimum DC input voltage is -0.5V. during transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Typical limits are at V_{CC} = 5V, T_A = + 25°C.
5. Other inputs can have any value within spec.
6. Maximum active power usage is the sum $I_{PP} + I_{CC}$ and is measured at 5MHz.
7. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
8. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
9. TTL inputs: spec TTL at V_{IL}, V_{IH} levels. CMOS inputs: GND ± 0.2V to V_{CC} ± 0.2V.
10. Guaranteed, but not tested.
11. X can be V_{IH} or V_{IL}.
12. AC characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V. Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V.

DEVICE OPERATION – START

MODE	$\overline{CE}$	$\overline{OE}/V_{PP}$	OUTPUT
Read	V_{IL}	V_{IL}	D_{OUT}
Output disable	V_{IL}	V_{IH}	Hi-Z
Standby	V_{IH}	X[11]	HI-Z

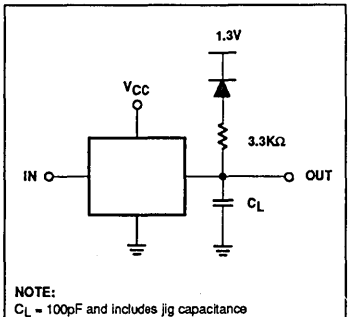
READ MODE

The 27C512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable $\overline{OE}/V_{PP}$ is the output control and should be used to gate data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}/V_{PP}$, assuming that $\overline{CE}$ has been Low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The 27C512 has a standby mode which reduces the maximum V_{CC} current to 100µA. It is placed in the Standby mode when $\overline{CE}$ is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}/V_{PP}$ pin.

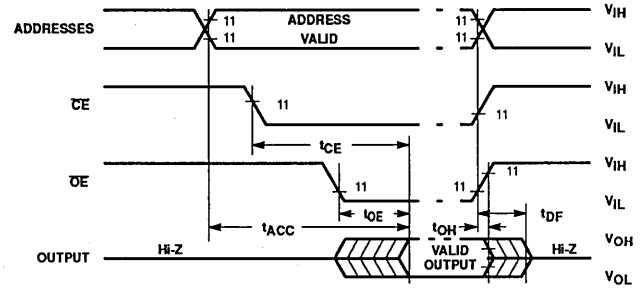
AC TESTING LOAD CIRCUIT



NOTE:
C_L = 100pF and includes jig capacitance

512K CMOS UV Erasable PROM (64K×8) — 27C512

AC VOLTAGE WAVEFORMS



Input Pulse Characteristics: t_r, $t_f \leq 5$ns, P_{RR} = 1MHz; for measurement points see Note 11.

PROGRAMMING INFORMATION

Complete programming system specifications for the quick-pulse programming program method are available upon request from Signetics Military Marketing.

Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of PROM programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers offering equipment certified by Signetics is available upon request from Signetics Military Memory Marketing.

PROGRAMMING THE 27C512

Caution: Exceeding 14.0V on $\overline{OE}/V_{PP}$ Pin may permanently damage the 27C512.

The 27C512 Quick Pulse programming algorithms rapidly program CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Actual programming times may vary due to differences in programming equipment.

Initially, all bits of the 27C512 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word.

The 27C512 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 12.75V and $\overline{CE}$ is at TTL Logic Low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

INTELLIGENT IDENTIFIER

The intelligent identifier provides the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is functional in the 25°±5°C ambient temperature range. To activate this mode, the equipment must force 11.5V to 12.5V on address A_9 of the 27C512. Two bytes may then be read from the device outputs by toggling address line A_0 from V_{IL} to V_{IH}. The $\overline{CE}$, $\overline{OE}/V_{PP}$ and all other address lines must be at V_{IL} during interrogation.

The identifier information for Signetics 27C512 is as follows:

When $A_0 = V_{IL}$ data is "Manufacturer"	$15_{(HEX)}$
When $A_0 = V_{IH}$ data is "Product"	$1D_{(HEX)}$

ERASURE CHARACTERISTICS

The erasure characteristics of the 27C512 are such that erasure begins to occur upon exposure to light with wavelengths shorter than aproximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C512 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C512 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure or the windowless OTP device can be used.

The recommended erasure procedure for the 27C512 is exposure to shortwave ultraviolet light which has a wave length of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The 27C512 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C512 can be exposed to without damage is 7258W/cm^2 (1 week @ 1200µW/cm^2). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

Signetics

27HC641

64K-Bit CMOS PROM (8K × 8)

Product Specification

Military CMOS Memory Products

DESCRIPTION

The 27HC641 is a CMOS, high-speed UV erasable, electronically programmed Read Only Memory. It is organized as 8192 words of 8 bits and operates from a single 5 volts +/– 10% power supply. All outputs offer 3-State operation and are fully TTL compatible.

The 27HC641 uses advanced CMOS circuitry which allows operation at bipolar PROM speeds while consuming lower power. The highest degree of protection against latch-up is achieved through epitaxial processing, simplifying the design of electronic equipment which is subject to a high noise environment.

The 27HC641 is available in the industry standard 24-pin Dual-In-Line (DIP) package with the same pin out as most 64K bipolar PROMs, thereby making it easier to upgrade systems currently using higher power bipolar PROMs, and allowing the designer to provide a lower power memory system solution. Also available in a standard 32-Pin LLCC.

FEATURES

- **Address access times 55ns and 70ns**
- **Max operating ICC of 110mA**
- **3-State outputs**
- **Direct replacement of Bipolar PROMs**
- **Programmed on industry standard EPROM programmers**
- **Fully TTL compatible**

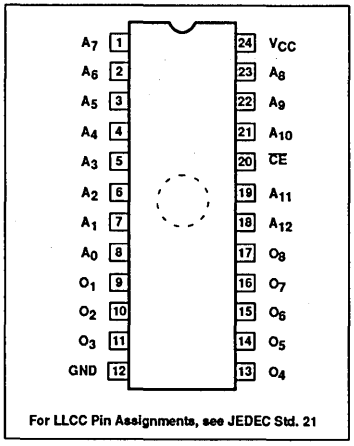
APPLICATIONS

- **Prototyping and volume production**
- **High performance memory systems**
- **Sequential controllers**
- **Microprogramming**
- **Random Logic Replacement**

ORDERING INFORMATION

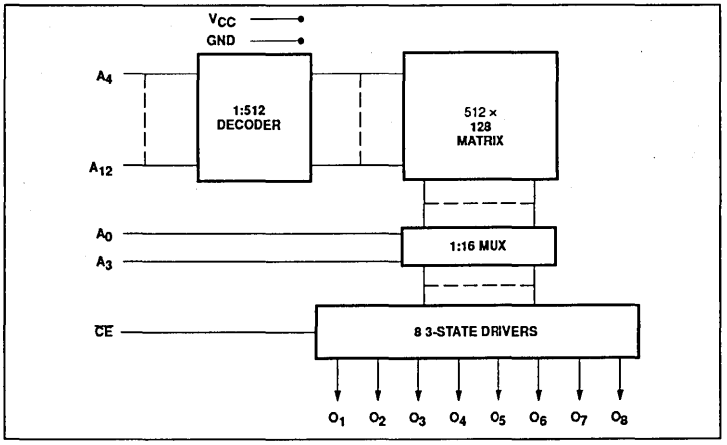
DESCRIPTION	ORDER CODE	
	55 nsec	70 nsec
24-Pin 600mil wide Cerdip w/Quartz Window	27HC641/BJA-55	27HC641/BJA-70
24-Pin Cerdip w/o Window[1]	27HC641/BXA-55 OT	27HC641/BXA-70 OT
28-Pin LLCC w/Quartz Window	27HC641/B3A-55	27HC641/B3A-70

PIN CONFIGURATION



For LLCC Pin Assignments, see JEDEC Std. 21

BLOCK DIAGRAM



64K-Bit CMOS PROM (8K × 8) — 27HC641

ABSOLUTE MAXIMUM RATINGS[2]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
V_I[3]	Voltage on $\overline{CE}$ pin with respect to GND	-0.5 to +13.5	V
V_I[3]	Voltage on any other pin with respect to GND	-0.5 to +7	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input voltage High	2.0		V_{CC} + 1	V
V_{IL}	Input voltage Low	-0.1		0.8	V

DC CHARACTERISTICS -55° ≤ T_A ≤ + 125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
I_{IL}	Input leakage current Low	V_I =+0.45V, V_{CC} = Max		±10	µA
I_{IH}	Input leakage current High	V_I = V_{CC}, V_{CC} = Max		±10	µA
I_{OZ}	Output current Hi-Z State	V_O = 0.45V, V_{CC} = Max		-10	µA
		V_O = V_{CC}, V_{CC} = Max		10	µA
V_{OL}	Output voltage Low	V_{CC} = Min, I_{OL} = 16mA		0.45	V
V_{OH}	Output voltage High	V_{CC} = Min, I_{OH} = -2mA	2.4		V
I_{CC}	Supply current	V_{CC} - Max		110	mA
V_{IK}	Input clamp voltage (All input pins except $\overline{CE}$)	V_I = -18mA, V_{CC} = Min		-1.2	V
V_{IK}	Input clamp voltage ($\overline{CE}$)	V_I = -12mA, V_{CC} = Min		-1.2	V
I_{OS}	Short circuit output current[6]	V_O = 0V, V_{CC} = Max	-10	-85	mA
C_{IN}	Input capacitance[4]	V_{IN} = 0V, V_{CC} = Nom		10	pF
C_{OUT}	Output capacitance[4]	V_{OUT} = 0V, V_{CC} = Nom		15	pF

AC ELECTRICAL CHARACTERISTICS[5] -55° ≤ T_A ≤ + 125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	-55 LIMITS		-70 LIMITS		UNIT
		Min	Max	Min	Max	
t_{AA}	Address access time		55		70	ns
t_{CE}	Chip enable access time		35		40	ns
t_{CD}	Output disable time from chip enable		35		40	ns

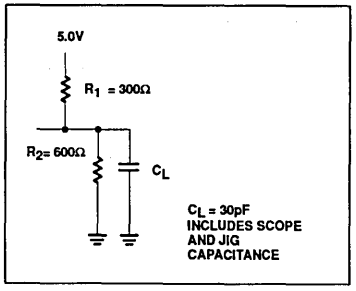
64K-Bit CMOS PROM (8K × 8) — 27HC641

AC ELECTRICALS DURING PROGRAMMING T_A=25° C ± 5°C, V_{CC} = 5V± 5%, V_{PP} = 12.5V ± 0.5V

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
t_W	Write pulse width	10		ms
t_R	Rise time	10		µs
t_F	Fall time	10		µs
t_{AS}	Address setup time	10		µs
t_{DS}	Data setup time	10		µs
t_{CS}	Chip enable setup time	10		µs
t_{AH}	Address hold time	10		µs
t_{DH}	Data hold time	10		µs
t_{CH}	Chip enable hold time	10		µs

NOTES:
1. Erase characteristics do not apply for one time programming (OT).
2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied.
3. Minimum DC input voltage is -0.5V during transitions. The inputs may undershoot to -2.0V for periods less than 20ns.
4. C_{IN} and C_{OUT} are measured initially and after any design changes which may affect capacitance.
5. Test conditions (C_L = 30pF, R_1 = 300Ω, and R_2 = 600Ω.).
6. Duration of short circuit should not exceed 1 second and short only one output at a time.

EQUIVALENT AC TEST LOAD CIRCUIT



ERASURE CHARACTERISTICS

The 27HC641 is erased by exposure to ultraviolet light. The recommended erasure procedure is exposure to short-wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12,000µW/cm^2 power rating.

The 27HC641 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27HC641 can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000µW/cm^2). Exposure of this CMOS EPROM to high-intensity UV light for longer periods may cause permanent damage. Some erasure may occur with exposure to light sources having wavelengths shorter than 4000 (Å) such as sunlight or fluorescent light. For maximum system reliability, precautions should be taken by placing opaque labels over the quartz window when used in these environments.

PROGRAMMING THE 27HC641

Initially, and after each erasure, all bits of the 27HC641 are in an undefined state. Data is introduced by programming "1"s and "0"s into the desired bit locations. Both "1"s and "0"s must be present in the data word to define each bit. The only way to change a bit to the opposite state is by ultraviolet light erasure and programming it to the desired state.

The 27HC641 is in the programming mode when the Output Enable ($\overline{G}$) pin is at 12.5V. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

INTELLIGENT IDENTIFIER

The intelligent identifier mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the 27HC641.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A_9 (Pin 22) of the 27HC641. Two bytes may then be read from the device outputs by toggling address line A_0 (Pin 8) from V_{IL} to V_{IH}. The $\overline{G}$ and all other address lines must be held at V_{IL} during interrogation.

The identifier information for Signetics 27HC641 is as follows:

When $A_0 = V_{IL}$
data is "Manufacturer" $15_{[HEX]}$
When $A_0 = V_{IH}$
data is "Product" $21_{[HEX]}$

PROGRAMMING INFORMATION

Complete programming system specifications for the Programming Algorithm are available upon request form Signetics Memory Marketing.

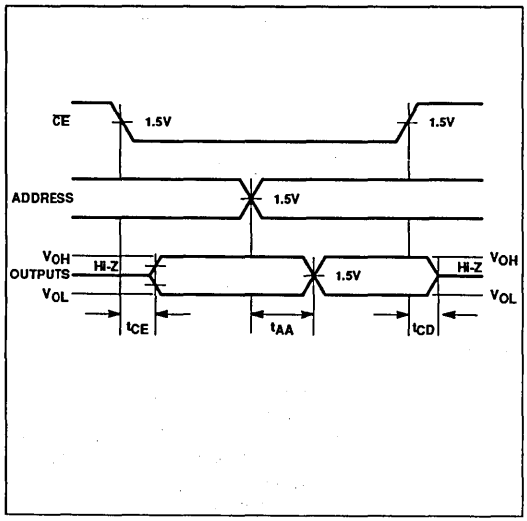
Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of PROM programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers offering equipment certified by Signetics is available upon request from Signetics Memory Marketing.

64K-Bit CMOS PROM (8K × 8) 27HC641

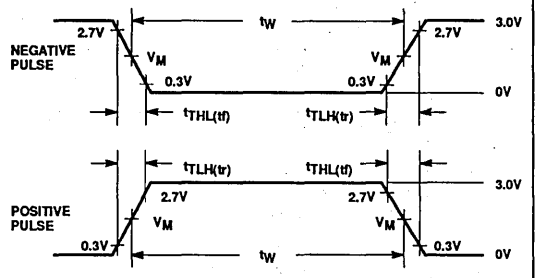
SIGNETICS DISCOURAGES THE CONSTRUCTION AND USE OF "HOMEMADE" PROGRAMMING EQUIPMENT

In order to consistently achieve excellent programming yields, periodic calibration of the programming equipment is required. Consult the equipment manufacturer for the recommended calibration interval. Signetics warranty for programmability extends only to product that has been programmed on certified equipment that has been serviced to the manufacturer's recommendations.

AC VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Signetics

Section 3
FAST Data Sheets

Military Products

INDEX

Signetics

54F00
Gate

Quad Two-Input NAND Gate

Product Specification

Military Logic Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F00/BCA
14-Pin Ceramic Flat Pack	54F00/BDA
20-Pin Ceramic LLCC	54F00/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

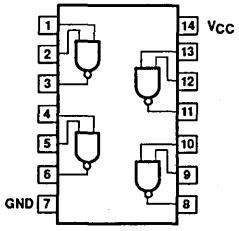
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

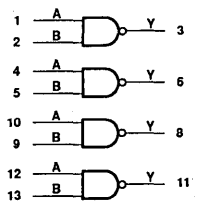
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60	-80	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	V_I = GND		1.9	2.8	mA
		I_{CCL}		$V_I \geq$ 4.0V		6.8	10.2	mA

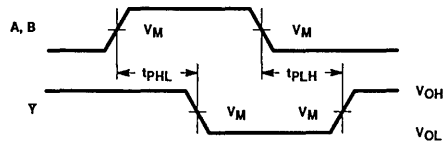
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	2.4 2.0	3.7 3.2	5.0 4.3	2.0 1.2	7.0 6.5	ns ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

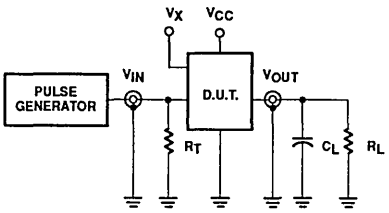
AC WAVE FORMS



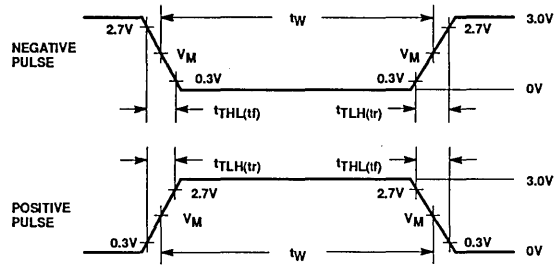
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F02
Gate

Quad Two-Input NOR Gate

Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	L
H	L	L
H	H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F02/BCA
14-Pin Ceramic Flat Pack	54F02/BDA
20-Pin Ceramic LLCC	54F02/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Output	50/33	1.0mA/20mA

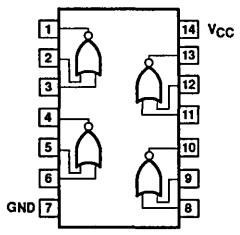
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

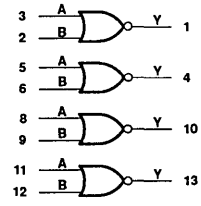
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V		5	100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V	-60	-80	-150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = Max		3.0	5.6	mA
		I_{CCL}			7.0	13	mA

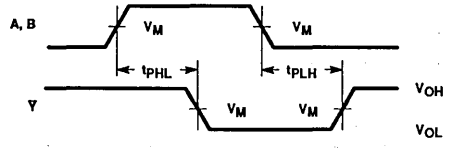
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	2.5 2.0	4.4 3.2	5.5 4.3	2.5 1.5	7.5 6.5	ns ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

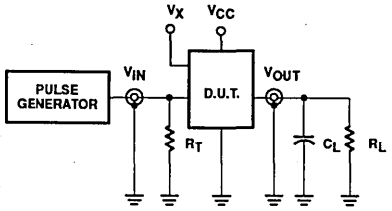
AC WAVEFORM



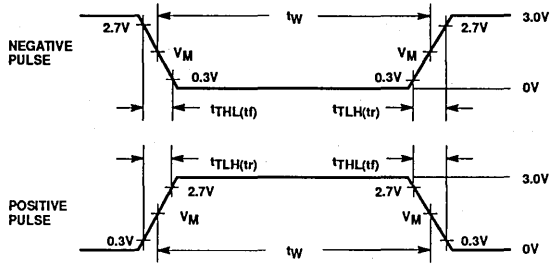
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54F04
Inverter

Hex Inverter

Product Specification

FUNCTION TABLE

INPUT	OUTPUT
A	$\overline{Y}$
L H	H L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F04/BCA
14-Pin Ceramic Flat Pack	54F04/BDA
20-Pin Ceramic LLCC	54F04/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Outputs	50/33	1.0mA/20mA

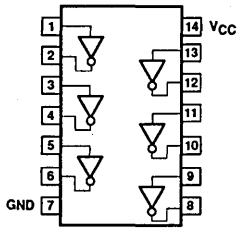
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

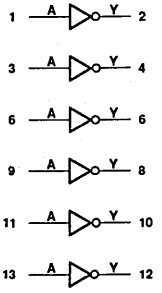
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60	-85	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	V_I = GND		2.8	4.2	mA
		I_{CCL}		$V_I \geq$ 4.0V		10.2	15.3	mA

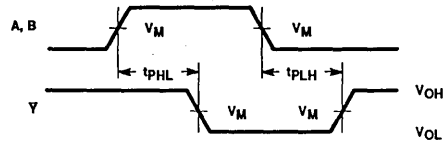
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.4	3.7	5.0	1.5	7.0	ns
t_{PHL}	A to $\overline{Y}$		1.5	3.2	4.3	1.1	6.5	ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

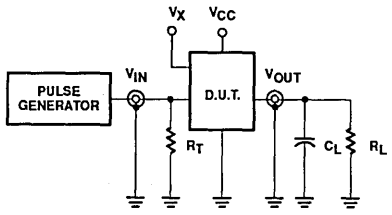
AC WAVEFORM



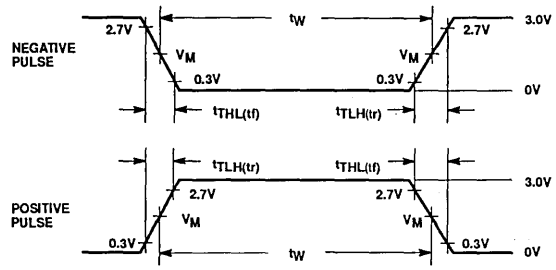
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F08
Gate

Quad Two-Input AND Gate

Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F08/BCA
14-Pin Ceramic Flat Pack	54F08/BDA
20-Pin Ceramic LLCC	54F08/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

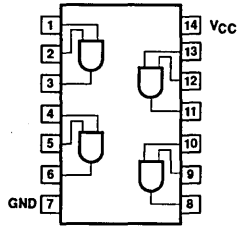
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

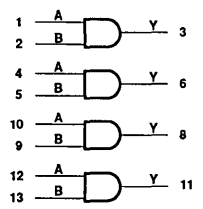
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			5	100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60	-90	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	$V_I \geq 4.0V$		5.5	8.3	mA
		I_{CCL}		V_I = GND		8.6	12.9	mA

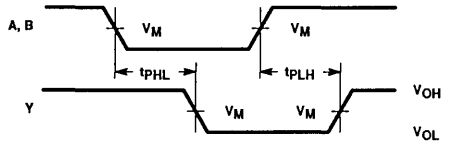
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to Y	Waveform 1	3.0 2.5	4.2 4.0	5.6 5.3	2.5 2.0	7.5 7.5	ns ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

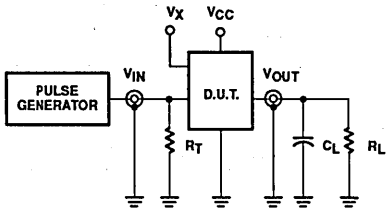
AC WAVEFORM



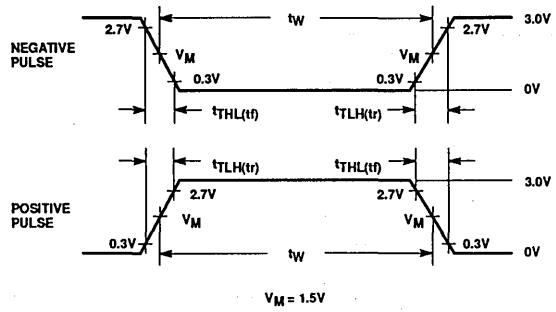
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. For Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F10, 54F11
Gates

Triple Three-Input NAND ('F10) AND ('F11) Gates

Product Specification

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Y('F10)	Y('F11)
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F10/BCA, 54F11/BCA
14-Pin Ceramic Flat Pack	54F10/BDA, 54F11/BDA
20-Pin Ceramic LLCC	54F10/B2A, 54F11/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A - C	Inputs	1.0/1.0	20µA/0.6mA
Y, $\overline{Y}$	Output	50/33	1.0mA/20mA

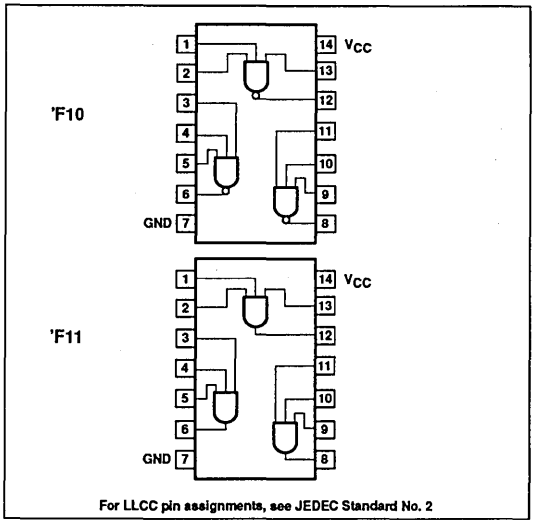
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

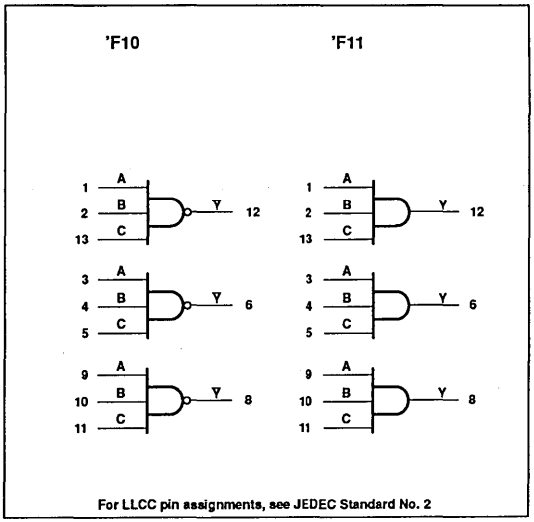
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage			V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage			V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current			V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current			V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]			V_{CC} = Max, V_O = 0.0V		-60	-75	-150	mA
I_{CC}	Supply current (total)	'F10	I_{CCH}	V_{CC} = Max	V_I = GND		1.8	2.1	mA
			I_{CCL}		$V_I \geq 4.0V$		6.0	7.7	mA
		'F11	I_{CCH}		$V_I \geq 4.0V$		4.7	6.2	mA
			I_{CCL}		V_I = GND		7.2	9.7	mA

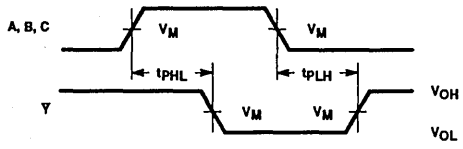
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic".)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A, B, C to Y	Waveform 1 'F10	2.4	3.7	5.0	2.0	7.0	ns
t_{PHL}			2.0	3.2	4.3	1.5	6.5	ns
t_{PLH}	Propagation delay A, B, C to Y	Waveform 2 'F11	3.0	4.2	5.6	2.5	7.5	ns
t_{PHL}			2.5	4.1	5.5	2.0	7.5	ns

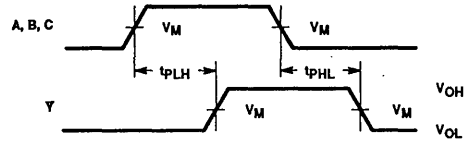
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

AC WAVEFORMS



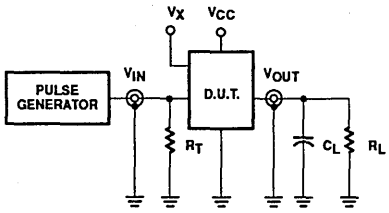
'F10
Waveform 1. For Inverting Outputs



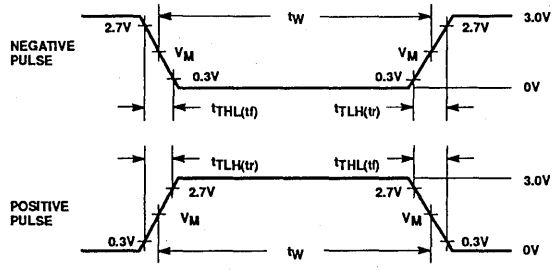
'F11
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

54F14
Schmitt Trigger

Hex Inverter Schmitt Trigger

Product Specification

Military Logic Products

DESCRIPTION

The 54F14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

FUNCTION TABLE

INPUTS	OUTPUT
A	$\overline{Y}$
0	1
1	0

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F14/BCA
Ceramic Flat Pack	54F14/BDA
Ceramic LLCC	54F14/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Outputs	50/33	1.0mA/20mA

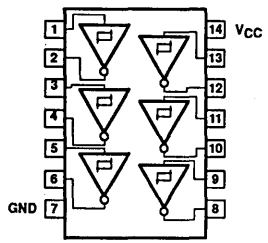
NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

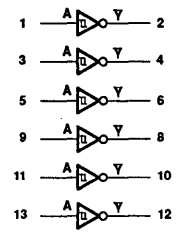
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

Schmitt Trigger | 54F14

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{T+}	Positive-going threshold		V_{CC} = 5.0V		1.4	1.7	2.0	V
V_{T-}	Negative-going threshold		V_{CC} = 5.0V		0.7	0.9	1.1	V
ΔV_T	Hysteresis (V_{T+} - V_{T-})		V_{CC} = 5.0V		0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC} = Min, V_I = V_{T-MIN}, I_{OH} = Max		2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_I = V_{T+MAX}, I_{OL} = Max			.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{T+}	Input current at positive-going threshold		V_{CC} = 5.0V, V_I = V_{T+}			0.0		µA
I_{T-}	Input current at negative-going threshold		V_{CC} = 5.0V, V_I = V_{T-}			175		µA
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			5	100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.2	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-60	-135	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	V_{IN} = GND		13	22	mA
		I_{CCL}		V_{IN} = 4.5V		23	32	mA

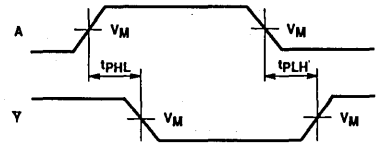
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to $\overline{Y}$	Waveform 1	4.0 3.5	6.5 5.0	8.5 6.5	3.0 3.5	12.0 9.0	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Schmitt Trigger | 54F14

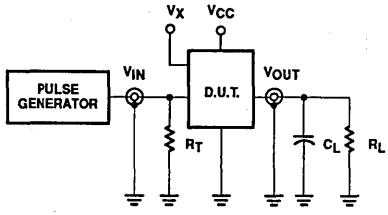
AC WAVEFORM



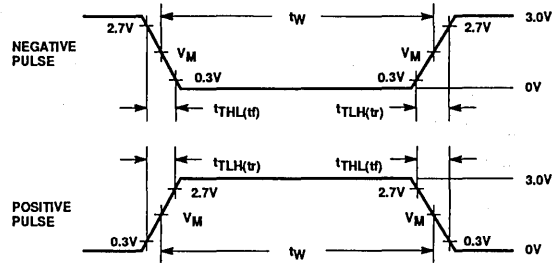
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F20
Gate

Dual Four-Input NAND Gate

Product Specification

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	$\overline{Y}$
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F20/BCA
14-Pin Ceramic SO	54F20/BDA
Ceramic LLCC	54F20/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D	Inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Outputs	50/33	1.0mA/20mA

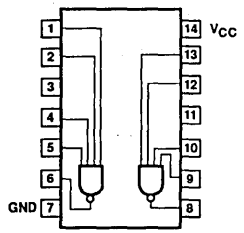
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range)

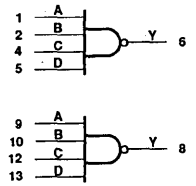
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-55 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

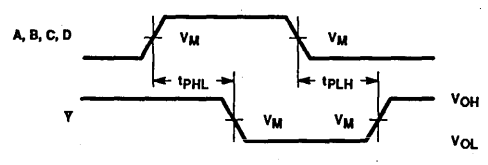
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			5	100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60	-85	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	V_I = GND		0.9	1.4	mA
		I_{CCL}		$V_I \geq$ 4.0V		3.4	5.1	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.4	3.7	5.0	2.0	7.0	ns
t_{PHL}	A, B, C, D to $\overline{Y}$		2.0	3.2	4.3	1.5	6.5	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

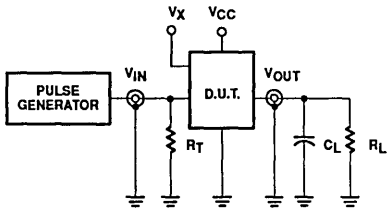
AC WAVEFORM



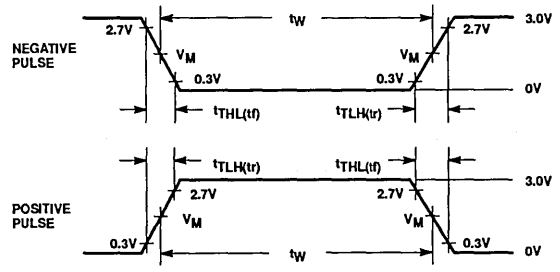
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

54F32
Gate

Quad Two-Input OR Gate

Product Specification

Military Logic Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F32/BCA
14-Pin Ceramic Flat Pack	54F32/BDA
20-Pin Ceramic LLCC	54F32/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/1.0	20μA/0.6mA
Y	Outputs	50/33	1.0mA/20mA

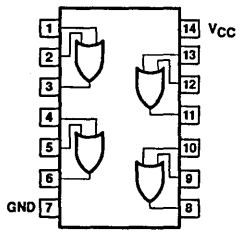
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

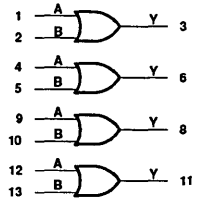
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

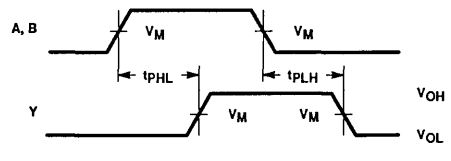
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input clamp current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60	-90	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	$V_I \geq 4.0V$		6.1	9.2	mA
		I_{CCL}		V_I = GND		10.3	15.5	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to Y	Waveform 1	3.0 3.0	4.2 4.0	5.6 5.3	3.0 3.0	6.6 6.3	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

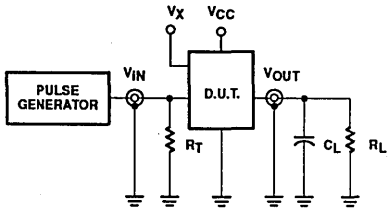
AC WAVEFORM



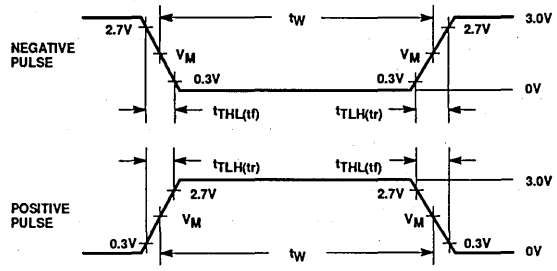
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. For Non-Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F37
Buffer

Quad Two-Input NAND Buffer

Product Specification

FUNCTION TABLE

INPUTS		OUTPUTS
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F37/BCA
14-Pin Ceramic FlatPack	54F37/BDA
20-Pin Ceramic LLCC	54F37/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Data inputs	1.0/2.0	20μA/1.2mA
$\overline{Y}$	Data outputs	600/80	12mA/48mA

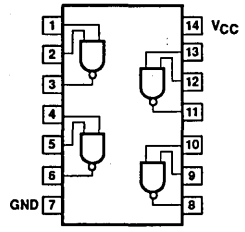
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High State and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

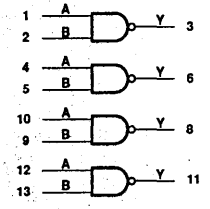
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-1	mA
I_{OH2}	High-level output current			-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = MIN	I_{OH1} = -1mA	2.5			V
				I_{OH2} = -12mA	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 48mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			5	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.4	-1.2	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	V_{IN} = GND		3	6	mA
		I_{CCL}		V_{IN} = 4.5V		23	33	mA

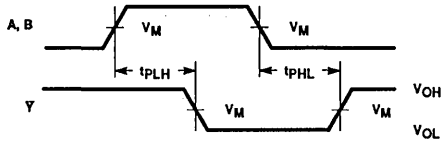
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic."

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A, B to $\overline{Y}$	Waveform 1	2.5	3.5	5.5	1.5	8.0	ns
t_{PHL}			1.5	2.5	4.5	1.0	5.5	ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

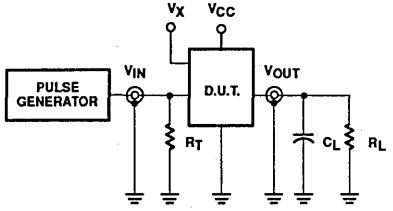
AC WAVEFORM



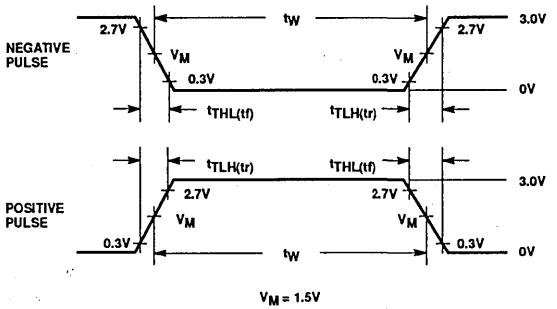
Waveform 1. For Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

Signetics

54F38
Buffer

Quad Two-Input NAND Buffer (Open Collector)

Product Specification

Military Logic Products

FUNCTION TABLE

INPUTS		OUTPUTS
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F38/BCA
Ceramic Flat Pack	54F38/BDA
Ceramic LLCC	54F38/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Inputs	1.0/2.0	20μA/1.2mA
$\overline{Y}$	Outputs	OC*/80	OC*/48mA

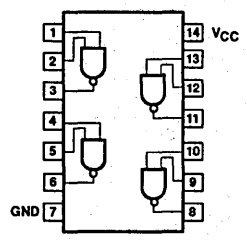
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High State and 0.6mA in the Low state.
*OC = Open Collector

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

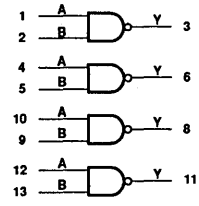
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	128	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, V_{OH} = Max				250	µA
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = 48mA			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at others maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			5	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.6	-1.2	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	V_I = GND		4	7	mA
		I_{CCL}		$V_I \geq$ 4.0V		22	30	mA

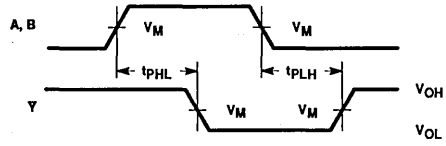
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	7.5 1.5	10 3.0	12.5 5.0	7.0 1.0	14.5 6.0	ns ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. When using open collector parts, the value of the pull-up resistor greatly affects the value of the TPLH. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the TPLH up to 50% with only a slight increase in the TPHL. However, if the value of the pull-up resistor is changed, the user must make certain that the total IOL current through the resistor, plus the total IIL's of the receivers does not exceed the IOL maximum specification.

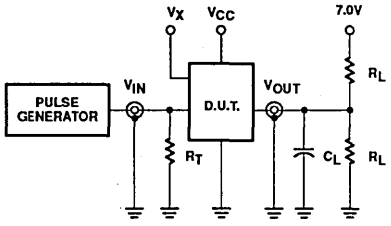
AC WAVEFORM



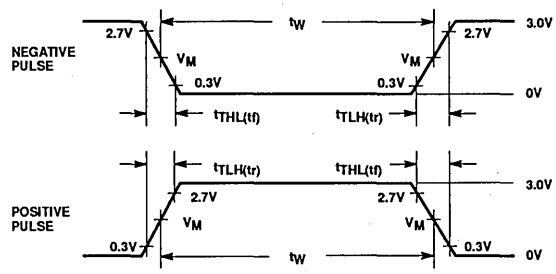
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. Propagation Delay Input to Output

TEST CIRCUIT AND WAVEFORM



Test Circuit for Open Collecor Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

54F51
Gate

Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-Invert Gate

Product Specification

Military Logic Products

FUNCTION TABLE
For 3-Input Gates

INPUTS						OUTPUT
A	B	C	D	E	F	1$\overline{Y}$
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE
For 2-Input Gates

INPUTS				OUTPUT
A	B	C	D	1$\overline{Y}$
H	H	X	X	L
X	X	H	H	L
All other combinations				H

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F51/BCA
14-Pin Ceramic FlatPack	54F51/BDA
20-Pin Ceramic LLCC	54F51/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

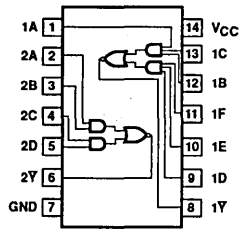
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B, C, D, E, F	Data inputs	1.0/1.0	20μA/0.6mA
1$\overline{Y}$, 2$\overline{Y}$	Data outputs	50/33	1mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High State and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS
(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

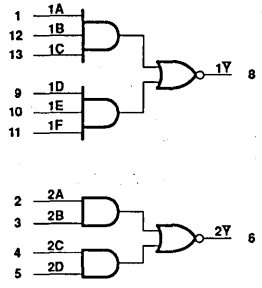
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max, V_I = GND		1.8	3.0	mA
		I_{CCL}	V_{CC} = Max, $V_I \geq$ 4.0V		5.5	7.5	mA

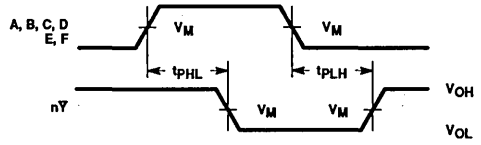
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.0	3.5	5.5	1.5	7.5	ns
t_{PHL}	A, B, C, D, E, F to nȲ		1.0	2.5	4.0	1.0	5.0	ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

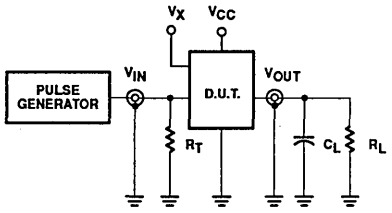
AC WAVEFORM



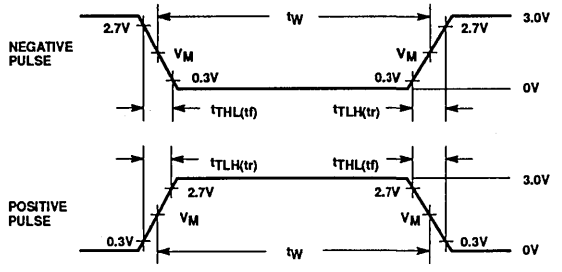
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. Propagation Delay Input to Output

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F64
Gate

Four-Two-Three-Two-Input AND-OR-Invert Gate

Product Specification

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F64/BCA
14-Pin Ceramic Flat Pack	54F64/BDA
20-Pin Ceramic LLCC	54F64/B2A

FUNCTION TABLE

INPUTS											OUTPUT
A	B	C	D	E	F	G	H	J	K	L	Ȳ
H	H	X	X	X	X	X	X	X	X	X	L
X	X	H	H	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

H = High voltage level
L = Low voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A - L	Inputs	1.0/1.0	20μA/0.6mA
Ȳ	Outputs	50/33	1.0mA/20mA

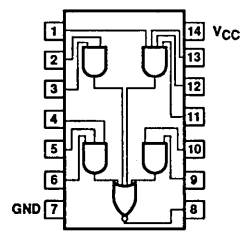
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

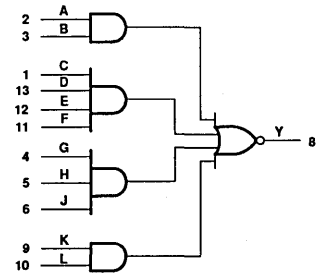
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60	-80	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	V_I = GND		1.9	2.8	mA
		I_{CCL}		$V_I \geq$ 4.0V		3.1	4.7	mA

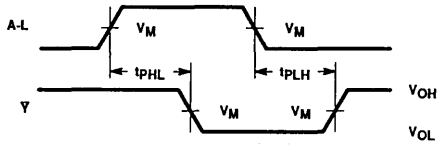
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A-L to $\overline{Y}$	Waveform 1	1.5 1.5	4.6 3.2	6.0 4.5	1.0 1.0	8.0 6.5	ns ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

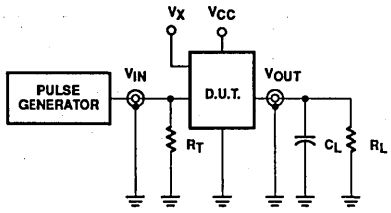
AC WAVEFORM



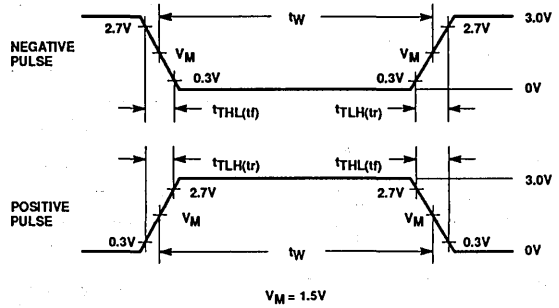
NOTE: For all waveforms, V_M = 1.5V.

Waveform 1. For Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

t_{TLH}, t_{THL} = Values should be less than or equal to the table entries.

V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F74
Flip-Flop

Dual D-Type Flip-Flop

Product Specification

DESCRIPTION

The 54F74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The D inputs must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

See 54F5074 for metastable immune version.

ORDERING INFORMATION

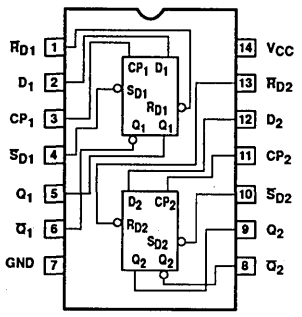
DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F74/BCA
14-Pin Ceramic FlatPack	54F74/BDA
20-Pin Ceramic LLCC	54F74/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_1, D_2	Data inputs	1.0/1.0	20μA/0.6mA
CP_1, CP_2	Clock pulse inputs (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset inputs (active Low)	1.0/3.0	20μA/1.8mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set inputs (active Low)	1.0/3.0	20μA/1.8mA
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

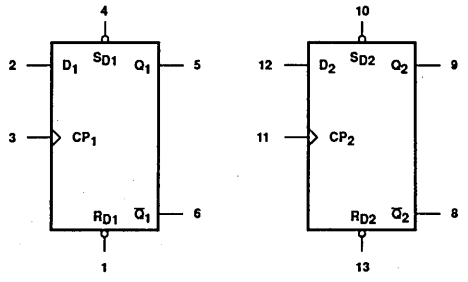
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2.

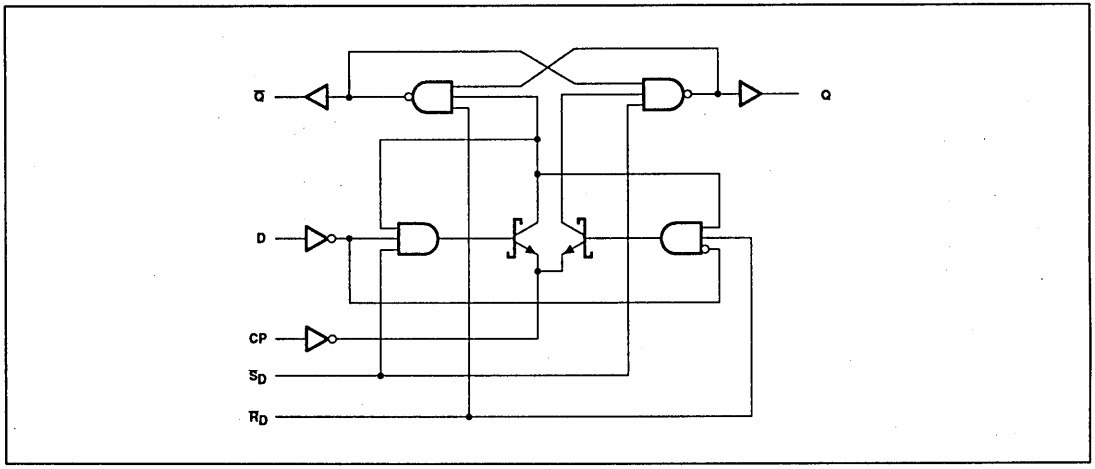
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2.

Flip-Flop | 54F74

LOGIC DIAGRAM



MODE SELECT – FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined[1]	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

NOTE:
1. Both outputs will be High if both $\overline{S}_D$ and $\overline{R}_D$ go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

Flip-Flop 54F74

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			5	100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	All inputs		1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V	D, CP inputs		-0.4	-0.6	mA
			$\overline{R}_D$, $\overline{S}_D$ inputs		-1.3	-1.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max, V_O = 0.0V		-60	-85	-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			11.5	16	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = 25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55 TO +125°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	3.8 4.4	5.3 6.2	6.8 8.0	3.5 3.7	8.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{SD}_n$ or $\overline{RD}_n$ to Q_n, $\overline{Q}_n$	Waveform 2	3.2 3.5	4.6 7.0	6.1 9.0	3.2 3.5	8.0 11.5	ns ns

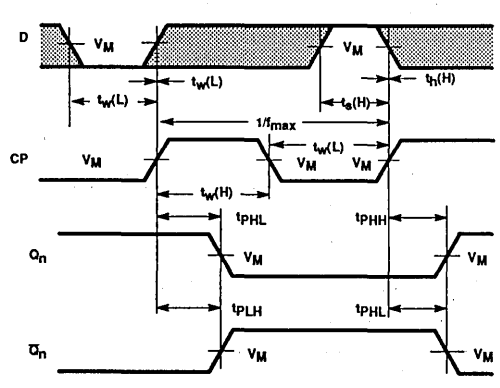
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V and T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.
5. These parameters are guaranteed, but not tested.

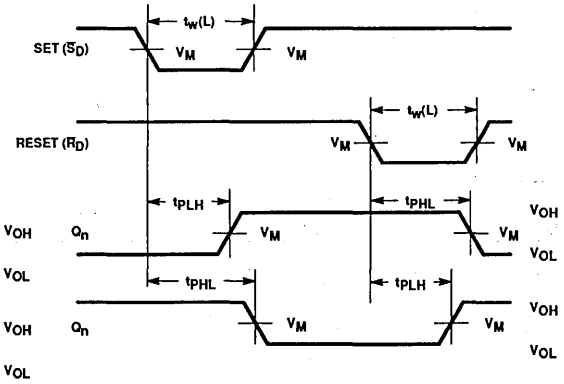
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			$T_A = 25°C$, $V_{CC} = +5.0V$, $C_L = 50pF$, $R_L = 500\Omega$			$T_A = -55$ TO $+125°C$, $V_{CC} = +5.0V \pm 10\%$, $C_L = 50pF$, $R_L = 500\Omega$		
			Min	Typ	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Setup time High or Low D_n to CP	Waveform 1	2.0 3.0			3.0 4.0		ns ns
$t_H(H)$ $t_H(L)$	Hold time High or Low D_n to CP	Waveform 1	1.0 1.0			2.0 2.0		ns ns
$t_W(H)$ $t_W(L)$	Clock pulse width High or Low	Waveform 1	4.0 5.0			4.0 6.0		ns ns
$t_W(L)$	$\overline{R}_D$ or $\overline{S}_D$ pulse width, Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time, $\overline{R}_D$ or $\overline{S}_D$ to CP	Waveform 3	2.0			3.0		ns

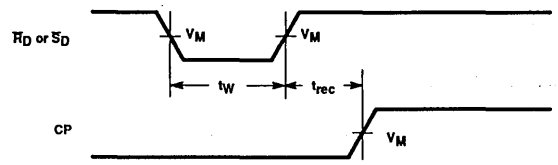
AC WAVEFORMS



Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width



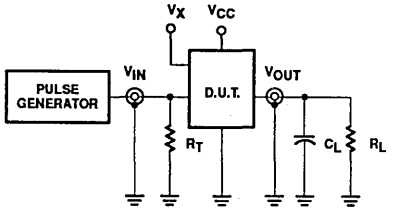
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths



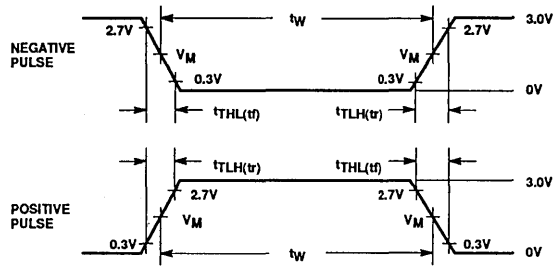
Waveform 3. Recovery Time

NOTE: For all waveforms, $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

54F109
Flip-Flop

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop

Product Specification

Military Logic Products

DESCRIPTION

The 54F109 is a dual positive edge-triggered J$\overline{K}$-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs, and complementary $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the Clock Input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Function Table. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition of the positive-going pulse.

The J and $\overline{K}$ inputs must be stable just one setup time prior to the Low-to-High transition of the Clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.8V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

ORDERING INFORMATION

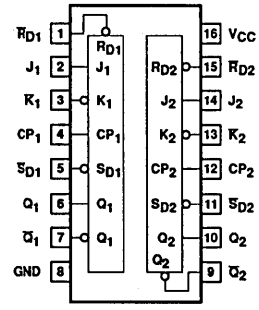
DESCRIPTION	ORDER CODE
Ceramic DIP	54F109/BEA
Ceramic Flat Pack	54F109/BFA
20-Pin Ceramic LLCC	54F109/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_1 - J_2, $\overline{K}_1$ - $\overline{K}_2$	Data inputs	1.0/1.0	20µA/0.6mA
CP_1, CP_2	Clock pulse inputs (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset inputs (active Low)	1.0/3.0	20µA/1.8mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set inputs (active Low)	1.0/3.0	20µA/1.8mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

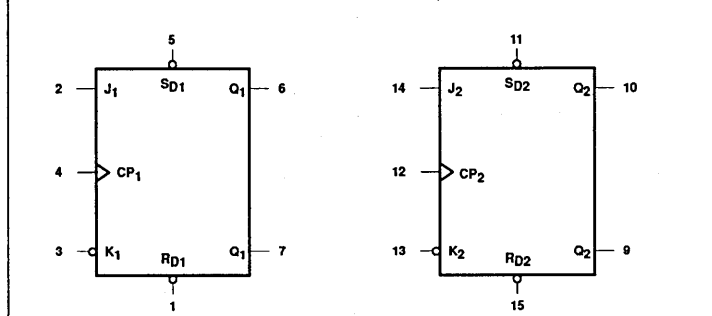
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



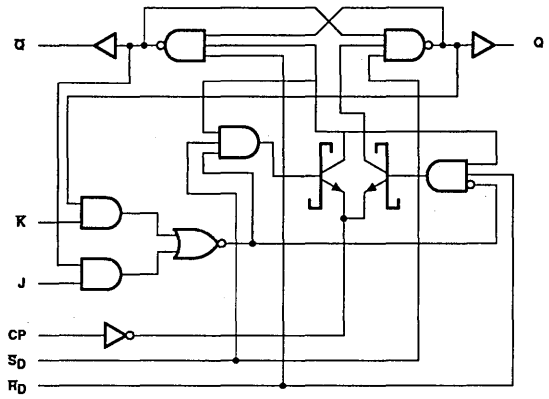
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2.

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (Note)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	↑	l	l	L	H
Load "1" (Set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = High voltage level steady state
L = Low voltage level steady state
h = High voltage level one setup time prior to the Low-to-High Clock transition
l = Low voltage level one setup time prior to the Low-to-High Clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High Clock transition
↑ = Low-to-High Clock transition

NOTE:
Both outputs will be High if both $\overline{S}_D$ and $\overline{R}_D$ go Low simultaneously.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			20.0	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	J, $\overline{K}$, CP inputs	V_{CC} = Max, V_I = 2.7V		1	20	µA
		$\overline{S}_D$, $\overline{R}_D$ inputs			1	20	µA
I_{IL}	Low-level input current	J, $\overline{K}$, CP inputs	V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
		$\overline{S}_D$, $\overline{R}_D$ inputs			-1.3	-1.8	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V	-60	-85	-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = Max		12.3	17	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing & Specifying FAST Logic."

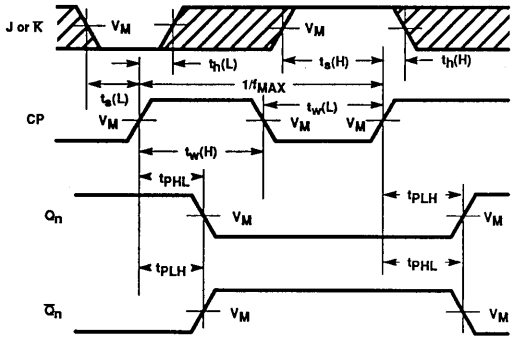
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	125		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	Waveform 1	3.8 4.4	5.3 6.2	7.0 8.0	3.8 4.4	9.0 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to Q_n, $\overline{Q}_n$	Waveform 2	3.2 3.5	5.2 7.0	7.0 9.0	2.8 3.5	9.0 11.5	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.
5. These parameters are guaranteed, but not tested.

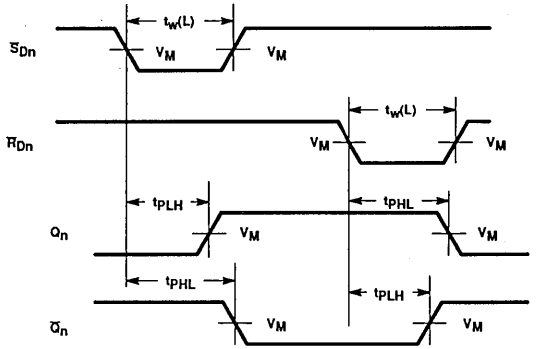
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time High or Low, J or $\overline{K}$ to CP	Waveform 1	3.0 3.0			5.0 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low, J or $\overline{K}$ to CP	Waveform 1	1.0 1.0			1.0 1.0		ns ns
$t_w(H)$ $t_w(L)$	Clock pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns ns
$t_w(L)$	Set or Reset pulse width, Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time, Set or Reset to clock	Waveform 3	2.0			2.0		ns

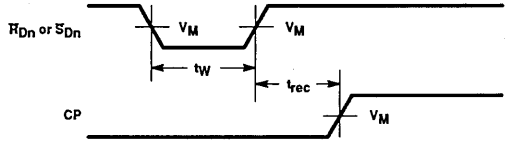
AC WAVEFORMS



Waveform 1. Clock to Output Delays, Data Set-Up and Hold Times, Clock Pulse Width



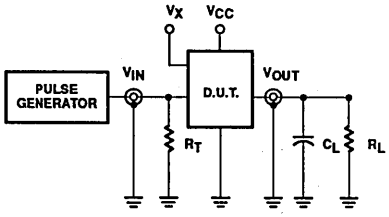
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths



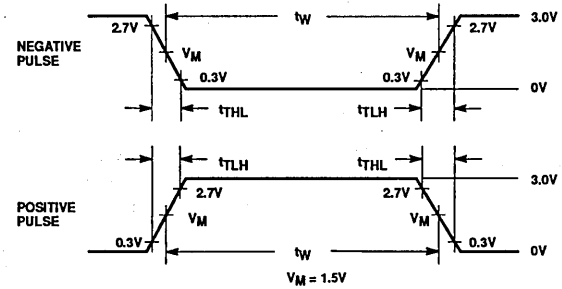
Waveform 3. Recovery Time

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

54F112
Dual J-K Negative Edge-Triggered Flip-Flop

Product Specification

Military Logic Products

DESCRIPTION

The 54F112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A High level on the Clock ($\overline{CP}$) input enables the J and K inputs, and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is High and the flip-flop will perform according to Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the High-to-Low transition of $\overline{CP}$.

ORDERING INFORMATION

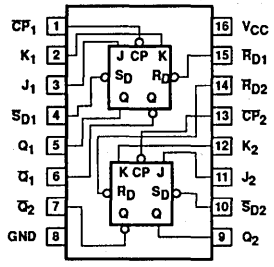
DESCRIPTION	ORDER CODE
Ceramic DIP	54F112/BEA
Ceramic Flat Pack	54F112/BFA
Ceramic LLCC	54F112/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_1, J_2, K_1, K_2	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}_1$, $\overline{CP}_2$	Clock pulse inputs (active falling edge)	1.0/4.0	20μA/2.4mA
$\overline{R}_{D1}$, $\overline{R}_{D2}$	Reset input (active Low)	1.0/5	20μA/3.0mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Set input (active Low)	1.0/5	20μA/3.0mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

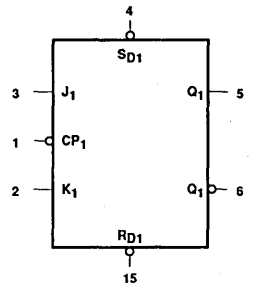
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as; 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments see Jedec Std. No. 2

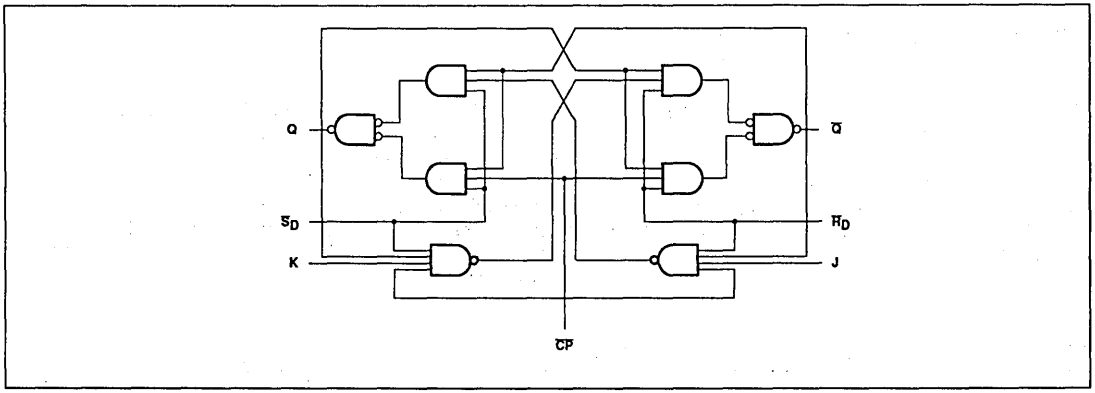
LOGIC SYMBOL



For LLCC pin assignments see Jedec Std. No. 2

Flip-Flop | 54F112

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	H	H	$\overline{q}$	q
Load "0" (reset)	H	H	↓	l	h	L	H
Load "1" (set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

NOTE:
Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.
H = High voltage level steady state
h = High voltage level one setup time prior to the High-to-Low Clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the High-to-Low Clock transition
q = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Low-level output voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	J_n, K_n	V_{CC} = Max, V_I = 7.0V			100	µA
		$\overline{R}_{Dn}$, $\overline{S}_{Dn}$				100	µA
		$\overline{CP}_n$				100	µA
I_{IH1}	High-level input current	J_n, K_n	V_{CC} = Max, V_I = 2.7V			20	µA
		$\overline{R}_{Dn}$, $\overline{S}_{Dn}$				20	µA
		$\overline{CP}_n$				20	µA
I_{IL}	Low-level input current	J_n, K_n	V_{CC} = Max, V_I = 0.5V			-0.6	mA
		$\overline{R}_{Dn}$, $\overline{S}_{Dn}$				-3.0	mA
		$\overline{CP}_n$				-2.4	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = Max		12	19	mA

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	4.0 3.5			5.0 4.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	0.0 0.0			0.0 0.0		ns ns
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ pulse width	Waveform 1	4.5 4.5			5.0 5.0		ns ns
$t_w(L)$	RD_n or SD_n pulse width	Waveform 2	4.5			5.0		ns
t_{rec}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to $\overline{CP}_n$	Waveform 3 & 4	4.0			5.0		ns ns

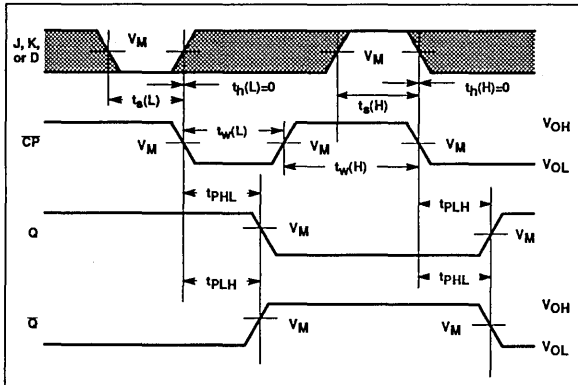
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	90	130		90[5]		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Qn, $\overline{Q}$n	Waveform 1	2.0 2.0	5.0 5.0	6.5 6.5	2.0 2.0	7.5 7.5	ns ns
t_{PHL}	Propagation delay $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to Q_n, $\overline{Q}_n$	Waveform 2	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	7.5 7.5	ns ns

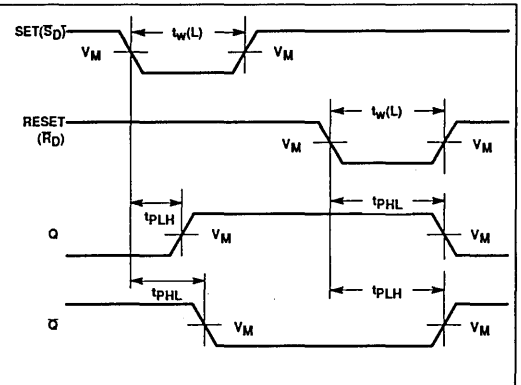
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.
5. Parameter guaranteed, but not tested.

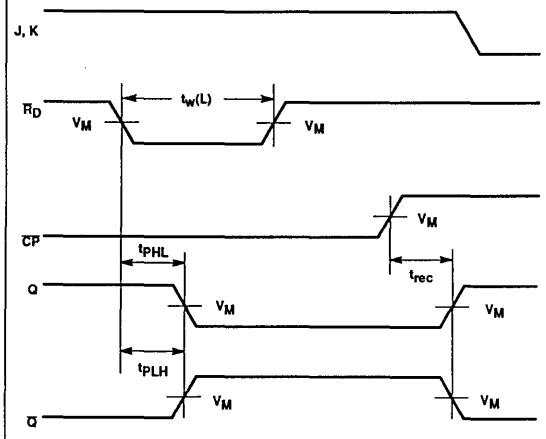
AC WAVEFORMS



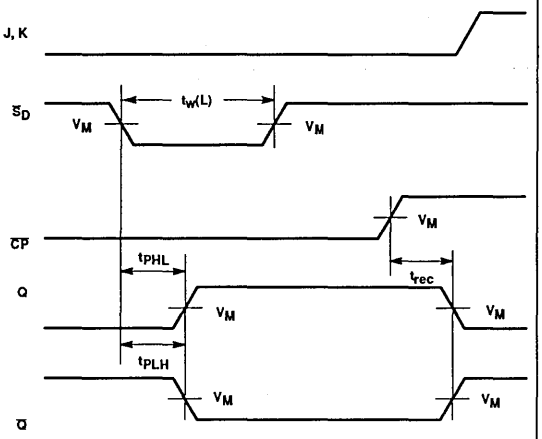
Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width



Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths



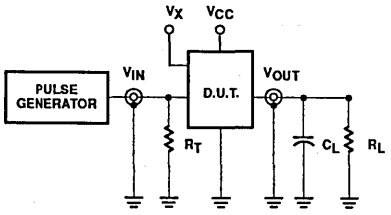
Waveform 3. Propagation Delay for Reset to Output, Reset Pulse Width, and Recovery Time for Reset to Clock



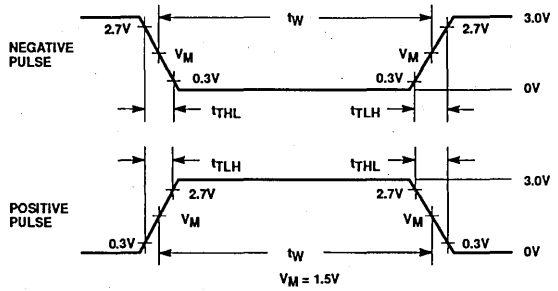
Waveform 4. Propagation Delay for Set to Output, Set Pulse Width, and Recovery Time for Set to Clock

$V_M = 1.5V$

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F113
Flip-Flop

Dual J-K Negative Edge-Triggered Flip-Flop Without Reset

Product Specification

DESCRIPTION

The 54F113 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Set and Clock inputs. The asynchronous Set ($\overline{S}_D$) input, when Low, forces the outputs to the steady state levels as shown in the Funcion Table regardless of the levels at the other inputs.

A High level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is High and the flip-flop will perform according to Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the High-to-Low transition of $\overline{CP}$.

ORDERING INFORMATION

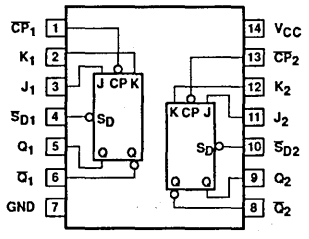
DESCRIPTION	ORDER CODE
Ceramic DIP	54F113/BCA
Ceramic Flat Pack	54F113/BDA
Ceramic LLCC	54F113/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
J_1, J_2, K_1, K_2	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}_1$, $\overline{CP}_2$	Clock pulse inputs (active falling edge)	1.0/4.0	20μA/2.4mA
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct set inputs (active Low)	1.0/5	20μA/3.0mA
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	50/33	1.0mA/20mA

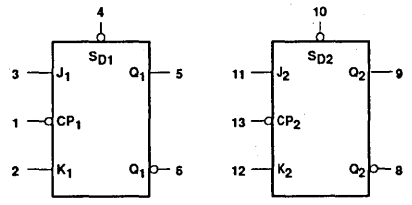
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments see JEDEC Standard No. 2

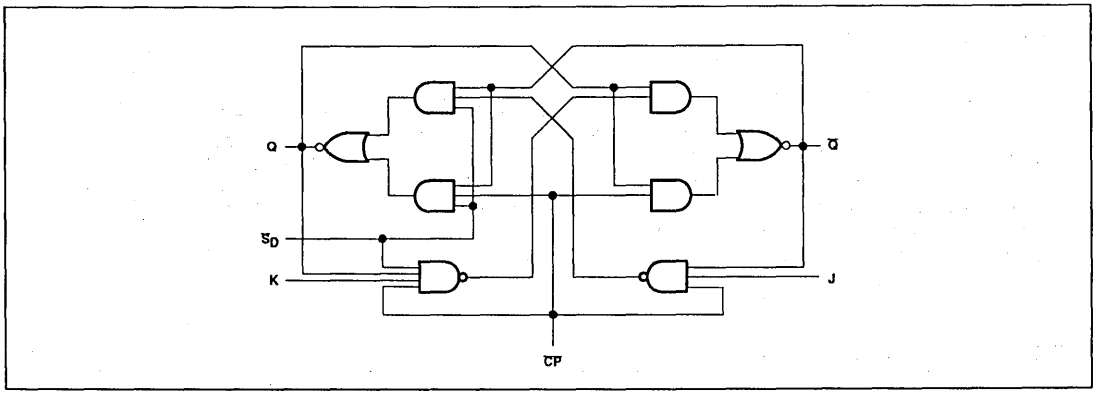
LOGIC SYMBOL



For LLCC pin assignments see JEDEC Standard No. 2

Flip-Flop | 54F113

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

H = High voltage level steady state.
h = High voltage level one setup time prior to the High-to-Low Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the High-to-Low Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low Clock transition.
X = Don't Care.
↓ = High-to-Low Clock transition.
Asynchronous input:
Low input to $\overline{S}_D$ set Q to High level
Set is independent of clock.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

Flip-Flop | 54F113

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	J_n, K_n	V_{CC} = Max, V_I = 7.0V			100	µA
		$\overline{S}_{Dn}$				100	µA
		$\overline{CP}_n$				100	µA
I_{IH1}	High-level input current	J_n, K_n	V_{CC} = Max, V_I = 2.7V			20	µA
		$\overline{S}_{Dn}$				20	µA
		$\overline{CP}_n$				20	µA
I_{IL}	Low-level input current	J_n, K_n	V_{CC} = Max, V_I = 0.5V			-0.6	mA
		$\overline{S}_{Dn}$				-3.0	mA
		$\overline{CP}_n$				-2.4	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = Max		15	21	mA

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	4.0 3.5			6.0 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low J_n or K_n to $\overline{CP}_n$	Waveform 1	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	$\overline{CP}_n$ pulse width	Waveform 1	4.5 4.5			5.0 5.0		ns ns
$t_w(L)$	SD_n pulse width	Waveform 2	4.5			5.0		ns
t_{rec}	Recovery time $\overline{S}_{Dn}$ to $\overline{CP}_n$	Waveform 2	4.5			6.0		ns

AC ELECTRICAL CHARACTERISTICS

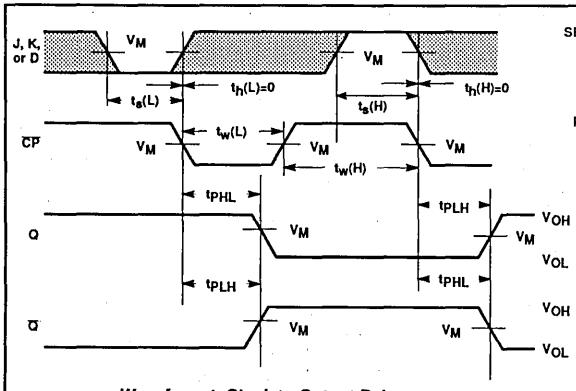
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	85	100		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Qn, $\overline{Q}$n	Waveform 1	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	8.0 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$ to Q_n, $\overline{Q}_n$	Waveform 2	2.0 2.0	4.5 4.5	6.5 6.5	2.0 2.0	8.5 8.5	ns ns

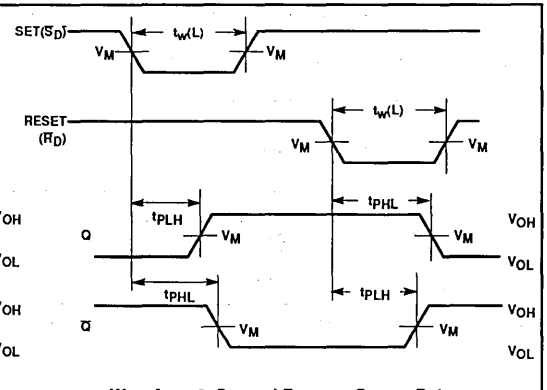
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width

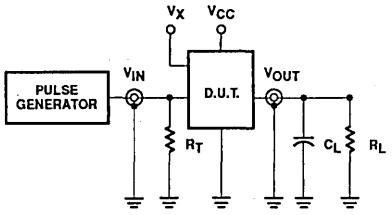


Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths

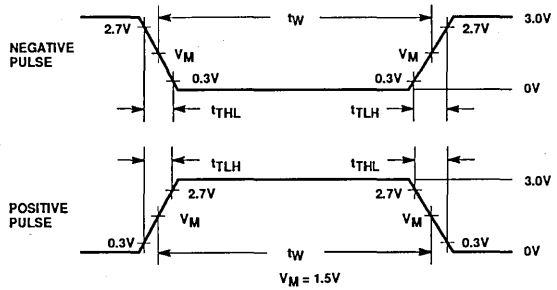
NOTE: For all waveforms V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Flip-Flop | 54F113

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F125
Buffer

Quad Buffer (3-State)

Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**

FUNCTION TABLE

INPUTS		OUTPUT
$\overline{C}$	A	Y
L	L	L
L	H	H
H	X	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F125/BCA
Ceramic Flat Pack	54F125/BDA
Ceramic LLCC	54F125/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
1A - 4A	Data inputs	1.0/0.033	20μA/20μA
$\overline{1C}$ - $\overline{4C}$	3-State output enable input	1.0/0.033	20μA/20μA
1Y - 4Y	Data outputs	600/80	12mA/48mA

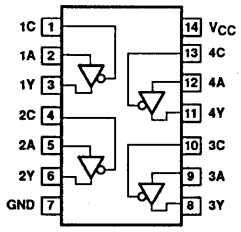
NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

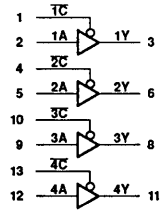
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

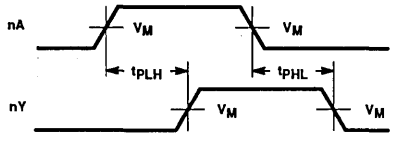
SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max,	I_{OH} = -3mA	2.4			V
		V_{IH} = Min	I_{OH} = Max	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 48mA		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V				-20	µA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-100	-150	-225	mA
I_{CC}	Supply Current[4] (total) I_{CCH}	V_{CC} = Max	$\overline{nC}$ = GND, nA = 4.5V		17	24	mA
	I_{CCL}		$\overline{nC}$ = nA = GND		28	40	mA
	I_{CCZ}		$\overline{nC}$ = nA = 4.5V		25	35	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

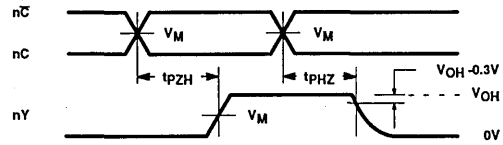
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA to nY	Waveform 1	2.0 3.0	4.0 5.5	6.0 7.5	2.0 3.0	7.0 8.5	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 2 Waveform 3	3.5 4.0	5.5 6.0	7.5 8.0	3.5 4.0	9.0 9.5	ns
t_{PHZ} t_{PLZ}	Output disable time From High and Low level	Waveform 2 Waveform 3	1.5 1.5	3.5 3.5	5.0 5.5	1.5 1.5	6.5 7.5	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open.

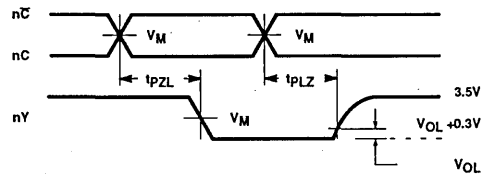
AC WAVEFORMS



Waveform 1. Propagation Delay For Input to Output



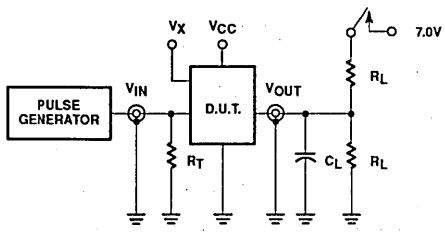
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



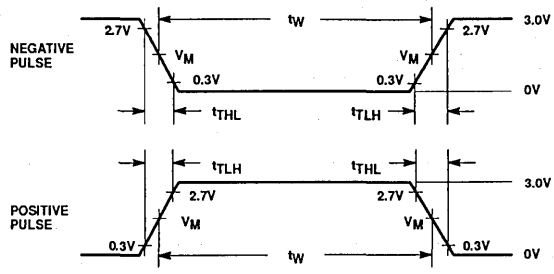
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

54F126
Buffer

Quad Buffer (3-State)

Objective Specification

Military Logic Products

FEATURES

- **High impedance NPN base inputs for reduced loading (20μA in High and Low states)**

FUNCTION TABLE

INPUTS		OUTPUT
C	A	Y
H	L	L
H	H	H
L	X	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
Z = High Impedance

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F126/BCA
Ceramic Flat Pack	54F126/BDA
Ceramic LLCC	54F126/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
1A - 4A	Data inputs	1.0/0.033	20μA/20μA
$\overline{1C}$ - $\overline{4C}$	3-State output enable input	1.0/0.033	20μA/20μA
1Y - 4Y	Data outputs	600/80	12mA/48mA

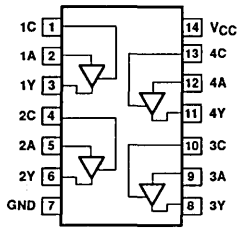
NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

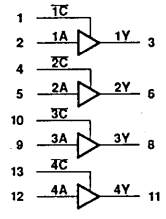
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

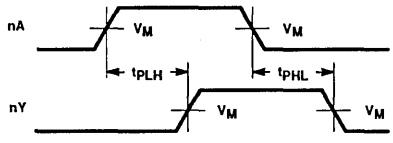
SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max,	I_{OH} = -3mA	2.4			V
		V_{IH} = Min	I_{OH} = Max	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 48mA		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V				-20	µA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-100	-150	-225	mA
I_{CC}	Supply Current[4] (total)	I_{CCH}	C_N = D_N = 4.5V		20	30	mA
		I_{CCL}	C_N = 4.5V, D_N = GND		32	48	mA
		I_{CCZ}	C_N = GND, D_N = 4.5V		26	39	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

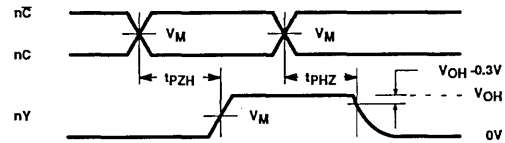
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay nA to nY	Waveform 1	2.0 3.0	4.0 5.5	6.5 8.0	2.0 3.0	7.5 9.0	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 2 Waveform 3	4.0 4.0	6.0 6.0	7.5 8.0	3.5 3.5	9.0 9.0	ns
t_{PHZ} t_{PLZ}	Output disable time From High and Low level	Waveform 2 Waveform 3	2.0 3.0	4.5 5.5	6.5 7.5	2.0 2.5	9.0 10.5	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open.

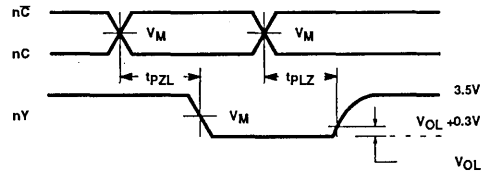
AC WAVEFORMS



Waveform 1. Propagation Delay For Input to Output



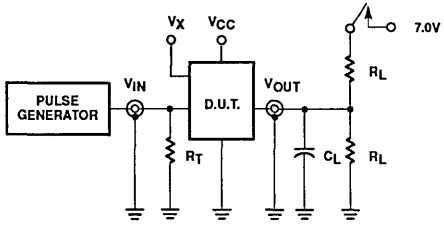
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



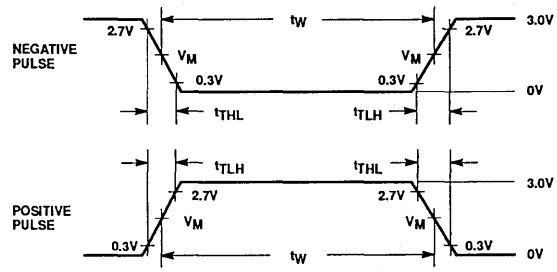
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs and Open Collector Outputs



VM = 1.5V

Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

54F138
Decoder/Demultiplexer

1-of-8 Decoder/Demultiplexer

Product Specification

Military Logic Products

FEATURES

- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **High-speed replacement for Intel 3205**

DESCRIPTION

The 54F138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active Low outputs ($\overline{O}_0$ - $\overline{O}_7$). The device features three Enable inputs; two active Low ($\overline{E}_1$, $\overline{E}_2$) and one active High (E_3). Every output will be High unless $\overline{E}_1$ and $\overline{E}_2$ are Low and E_3 is High. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 54F138's and one inverter.

The device can be used as an eight output demultiplexer by using one of the active Low Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active High or active Low state.

ORDERING INFORMATION

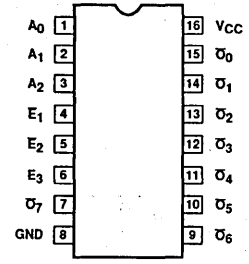
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F138/BEA
16-Pin Ceramic FlatPack	54F138/BFA
20-Pin Ceramic LLCC	54F138/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_2	Address inputs	1.0/1.0	20µA/0.6mA
$\overline{E}_1$ - $\overline{E}_2$	Enable inputs (active Low)	1.0/1.0	20µA/0.6mA
E_3	Enable input (active High)	1.0/1,0	20µA/0.6mA
$\overline{O}_0$ - $\overline{O}_7$	Outputs (active Low)	50/33	1.0mA/20mA

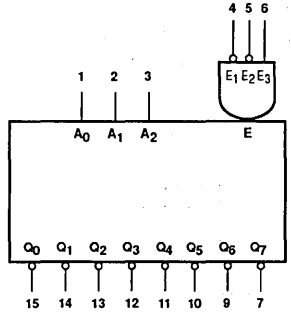
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

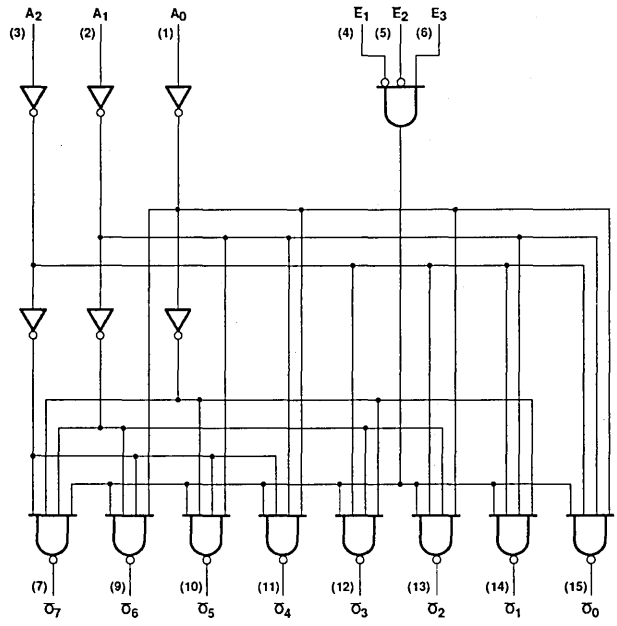
Decoder/Demultiplexer 54F138

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

LOGIC DIAGRAM



( ) = Pin number
V_{CC} = Pin 16
GND = Pin 8

For LLCC pin assignments, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max, V_O = 0.0V	-60	-90	-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max, V_I = ≥ 4.0V		13	20	mA

AC ELECTRICAL CHARACTERISTICS

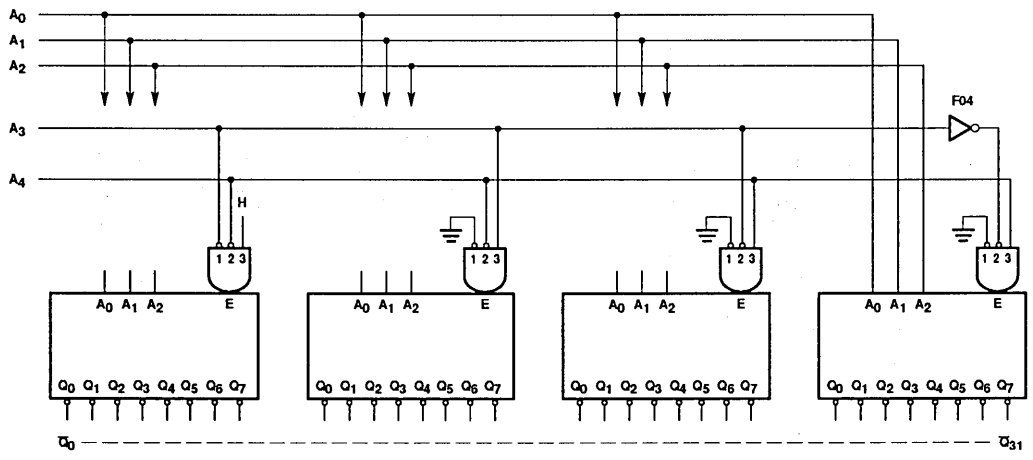
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output A_n to $\overline{O}_n$	Waveform 1 and 2	3.5 4.0	5.6 6.1	7.0 8.0	2.9 3.5	12.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	Waveform 2	3.5 3.0	6.4 5.3	7.0 7.0	3.0 3.0	11.0 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay E_3 to $\overline{O}_n$	Waveform 1	4.0 3.5	8.2 5.6	8.0 7.5	4.0 3.5	12.5 8.5	ns ns

NOTES:

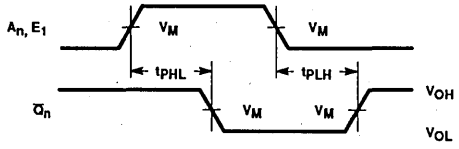
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open.

APPLICATION

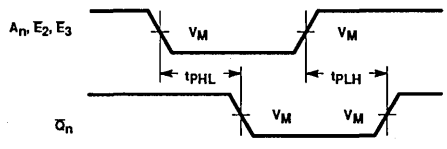


Expansion to 1-of-32 Decoding

AC WAVEFORMS



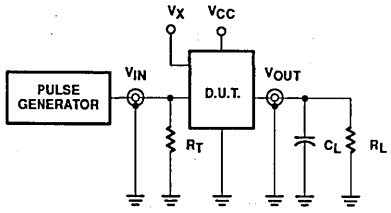
Waveform 1. For Inverting Outputs



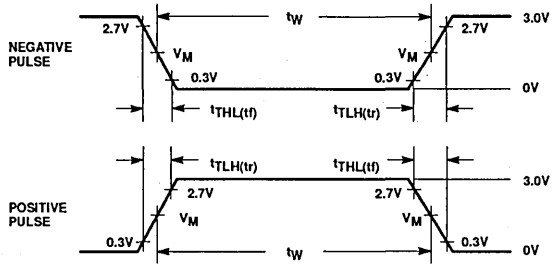
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F139
Decoder/Demultiplexer

Dual 1-of-4 Decoder/Demultiplexer

Product Specification

FEATURES
- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Multifunction capability**

DESCRIPTION
The 54F139 is a high-speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_0, A_1) and providing four mutually exclusive active Low outputs ($\overline{O}_{0n}$ - $\overline{O}_{3n}$). Each decoder has an active Low Enable ($\overline{E}$). When $\overline{E}$ is High, every output is forced High. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

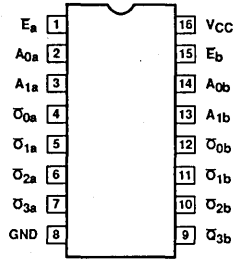
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F139/BEA
16-Pin Ceramic FlatPack	54F139/BFA
20-Pin Ceramic LLCC	54F139/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_{na} - A_{nb}	Address inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_a$ - $\overline{E}_b$	Enable inputs	1.0/1.0	20μA/0.6mA
$\overline{O}_{0a}$ - $\overline{O}_{3a}$, $\overline{O}_{0b}$ - $\overline{O}_{3b}$	Outputs	50/33	1.0mA/20mA

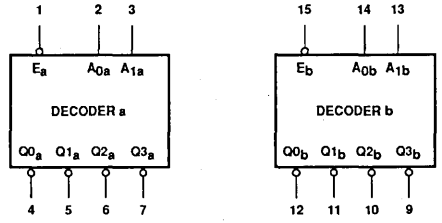
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

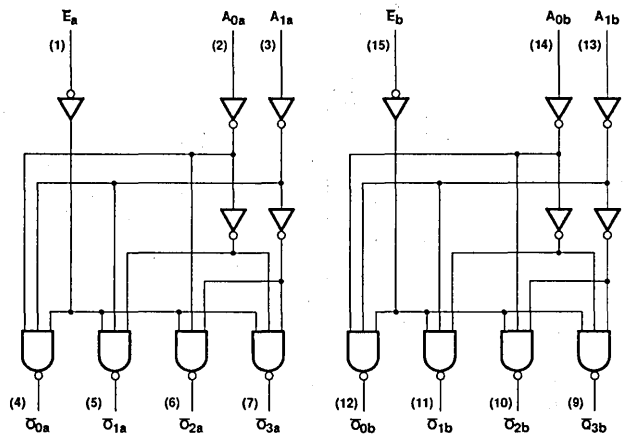
LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC pin assignments, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

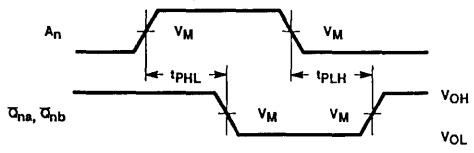
SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max, V_O = 0.0V	-60	-90	-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max		13	20	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

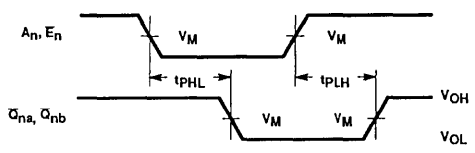
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_0 to A_1 to $\overline{Q}_{na}$, $\overline{Q}_{nb}$	Waveform 1 and 2	3.5 4.0	5.3 6.1	7.0 8.0	2.5 3.5	12.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay E_n to $\overline{Q}_{na}$, $\overline{Q}_{nb}$	Waveform 2	3.5 3.0	5.4 4.7	7.0 6.5	3.0 2.5	9.0 8.0	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. To measure I_{CC}, outputs must be open, V_{IH} on all inputs = 4.5V.

AC WAVEFORMS



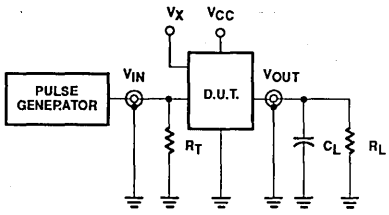
Waveform 1. For Inverting Outputs



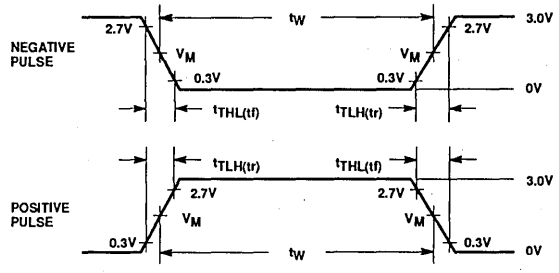
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F148
Encoder

8-Input Priority Encoder

Product Specification

FEATURES

- **Code conversions**
- **Multi-channel D/A converter**
- **Decimal-to-BCD converter**
- **Cascading for priority encoding of "N" bits**
- **Input enable capability**
- **Priority encoding — automatic selection of highest priority-input line**
- **Output enable — active Low when all inputs High**
- **Group signal output — active when any input is Low**

DESCRIPTION

The 54F148 8-input priority encoder accepts data from eight active-Low inputs and provides a binary representation on the three active-Low outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I}_7$ having the highest priority.

A High on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (High) state and allow new data to settle without producing erroneous information at the outputs.

ORDERING INFORMATION

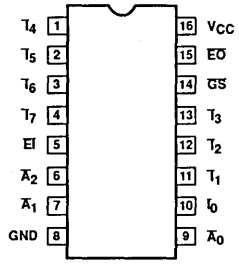
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F148/BEA
16-Pin Ceramic FlatPack	54F148/BFA
20-Pin Ceramic LLCC	54F148/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{I}_0$ - $\overline{I}_7$	Priority inputs (active Low)	1.0/1.0	20μA/1.2mA
$\overline{I}_0$	Priority input (active Low)	1.0/2.0	20μA/0.6mA
$\overline{EI}$	Enable input (active Low)	1.0/2.0	20μA/1.2mA
$\overline{EO}$	Enable output (active Low)	50/33	1.0mA/20mA
$\overline{GS}$	Group select output (active Low)	50/33	1.0mA/20mA
$\overline{A}_0$ - $\overline{A}_2$	Address outputs (active Low)	50/33	1.0mA/20mA

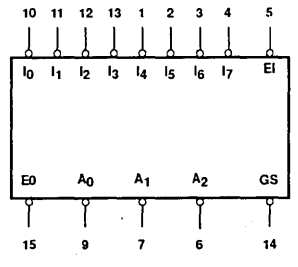
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

Encoder 54F148

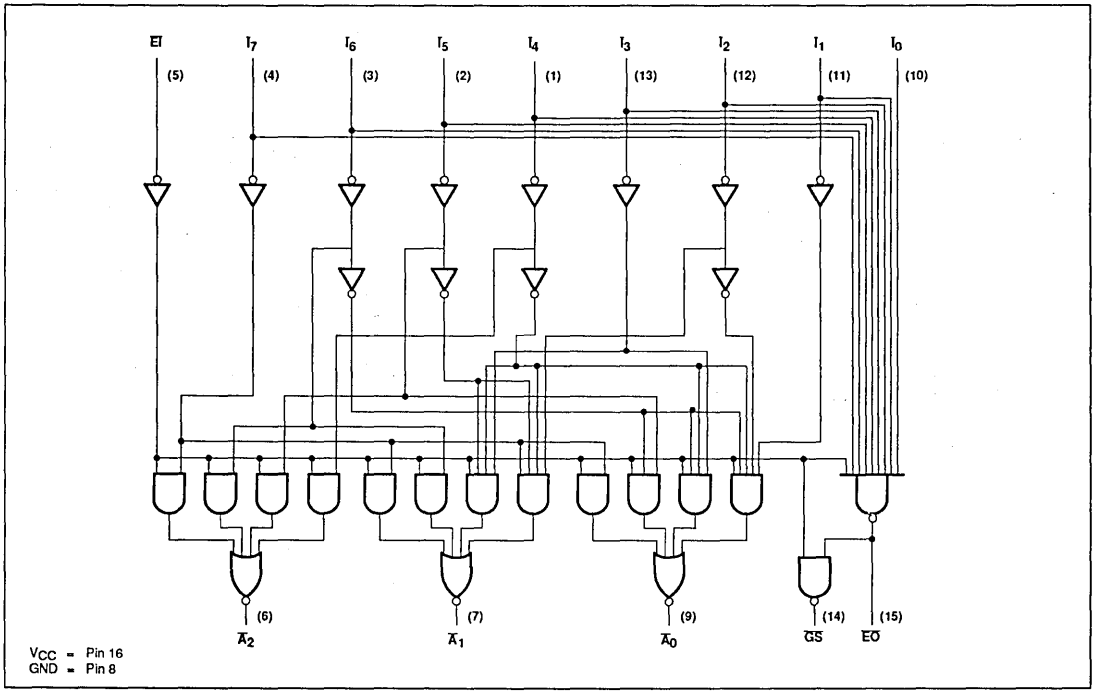
A Group Signal ($\overline{GS}$) output and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active-Low when any input is Low; this indicates when any input is active. The $\overline{EO}$ is active-Low when all inputs are High. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are active-High when the Enable Input is High.

FUNCTION TABLE

INPUTS									OUTPUTS				
$\overline{EI}$	$\overline{I_0}$	$\overline{I_1}$	$\overline{I_2}$	$\overline{I_3}$	$\overline{I_4}$	$\overline{I_5}$	$\overline{I_6}$	$\overline{I_7}$	$\overline{GS}$	$\overline{A_0}$	$\overline{A_1}$	$\overline{A_2}$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = High voltage level
L = Low voltage level
X = Don't care

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V		5	100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current	$\overline{I_0}$, $\overline{EI}$	V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
		$\overline{I_1}$ - $\overline{I_7}$			-0.8	-1.2	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60	-80	-150	mA
I_{CC}	Supply current (total)		V_{CC} = Max		23	35	mA

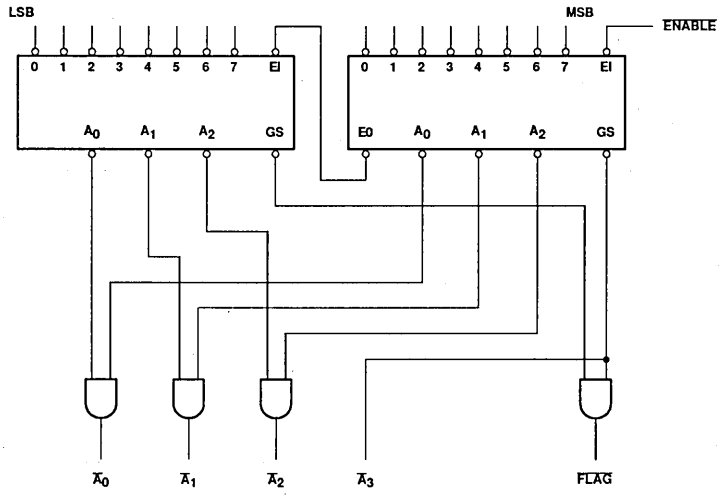
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{I_n}$ input to $\overline{A_n}$	Waveform 2	3.5 4.0	6.0 6.0	9.0 10.5	3.5 4.0	11.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I_n}$ input to $\overline{EO}$	Waveform 1	2.0 2.5	3.5 4.5	6.5 7.5	2.0 2.5	8.5 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I_n}$ input to $\overline{GS}$	Waveform 2	2.0 2.0	4.0 6.0	9.0 8.0	2.0 2.0	11.0 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ input to $\overline{A_n}$	Waveform 2	3.5 3.0	6.0 6.5	8.5 8.0	3.5 3.0	10.5 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ input to $\overline{GS}$	Waveform 2	2.5 3.0	4.5 6.5	7.0 7.5	2.5 3.0	9.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ input to $\overline{EO}$	Waveform 2	3.0 4.5	5.0 7.0	7.0 10.5	3.0 4.5	9.0 13.0	ns ns

NOTES:

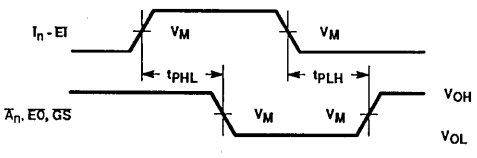
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

APPLICATION

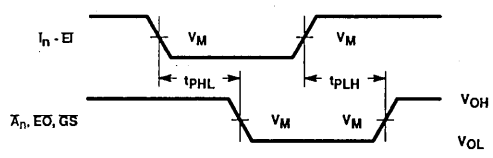


16-Input Priority Encoder

AC WAVEFORMS



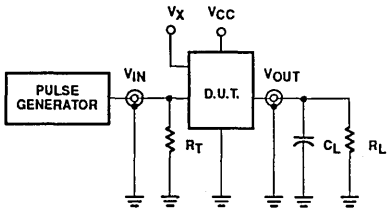
Waveform 1. For Inverting Outputs



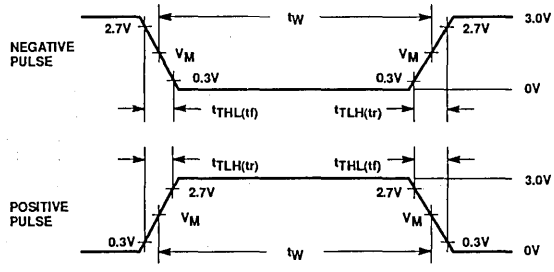
Waveform 2. For Non-Inverting Outputs

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

54F154
1-of-16 Decoder/Demultiplexer

Military Logic Products

Product Specification

FEATURES
- **16-line demultiplexing capability**
- **Mutually exclusive outputs**
- **2-input enable gate for strobing or expansion**

DESCRIPTION
The 54F154 decoder accepts four active High binary address inputs and provides 16 mutually exclusive active Low outputs. The 2-input Enable ($\overline{E}_0$ - $\overline{E}_1$) gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The Enable gate has two ANDed inputs which must be Low to enable the outputs.

The 54F154 can be used as a 1-of-16 demultiplexer by using one of the Enable inputs as the multiplexed data input. When the other Enable is Low, the addressed output will follow the state of the applied data.

ORDERING INFORMATION

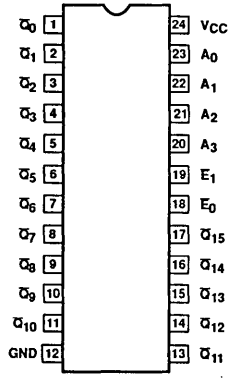
DESCRIPTION	ORDER CODE
Ceramic DIP	54F154/BLA
Ceramic Flat Pack	54F154/BKA
Ceramic LLCC	54F154/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_3	Data Inputs	1.0/1.0	20μA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Enable Inputs	1.0/1.0	20μA/0.6mA
$\overline{O}_0$ - $\overline{O}_{15}$	Data outputs	50/33	1.0mA/20mA

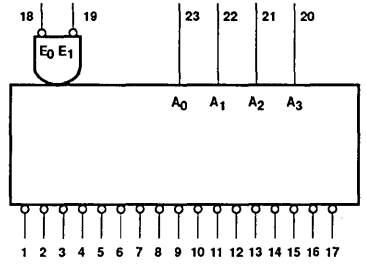
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

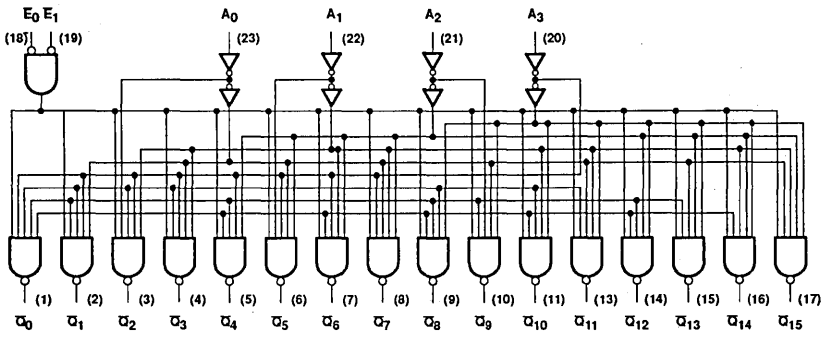
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

Decoder/Demultiplexer 54F154

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

FUNCTION TABLE

INPUTS						OUTPUTS														
$\overline{E}_0$	$\overline{E}_1$	A_3	A_2	A_1	A_0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	$\overline{O}_8$	$\overline{O}_9$	$\overline{O}_{10}$	$\overline{O}_{11}$	$\overline{O}_{12}$	$\overline{O}_{13}$	$\overline{O}_{14}$	$\overline{O}_{15}$
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	μA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage[4]	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			100	μA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V			-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = Max, Inputs = GND, Outputs open		26	40	mA

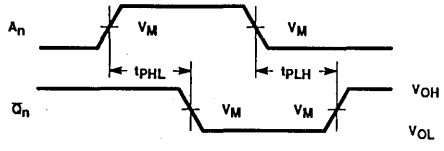
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{O}_n$	Waveform 1	2.0 3.5	5.0 6.5	9.5 10.0	1.5 3.0	11.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_n$ to $\overline{O}_n$	Waveform 2	2.0 4.0	4.0 6.0	7.5 9.0	1.5 3.5	9.0 10.5	ns ns

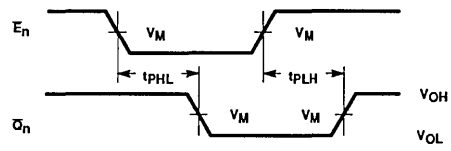
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable condition and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions for V_{IH} = 2.2V. However, the specified test limits and conditions are guaranteed.

AC WAVEFORMS



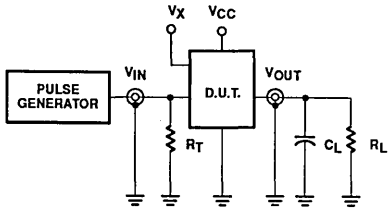
Waveform 1. Propagation Delay, Address to Output



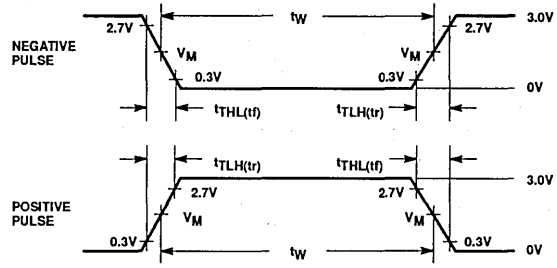
Waveform 2. Propagation Delay, Enable to Output

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

Signetics

54F157A, 54F158A
Data Selectors/Multiplexers

54F157A Quad 2-Input Data Selector/Multiplexer (Non-Inverted)
54F158A Quad 2-Input Data Selector/Multiplexer (Inverted)

Military FAST Products

Product Specification

DESCRIPTION

The 54F157A is a high-speed quad 2-input multiplexer which selects 4 bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active Low. When $\overline{E}$ is High all of the outputs (Y) are forced Low regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 54F157A. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$Y_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$Y_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Y_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$Y_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

The 54F158A is similar but has inverting outputs:

$$\overline{Y}_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$\overline{Y}_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Y}_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$\overline{Y}_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F157A/BEA, 54F158A/BEA
16-Pin Ceramic FlatPack	54F157A/BFA, 54F158A/BFA
20-Pin Ceramic LLCC	54F157A/B2A, 54F158A/B2A

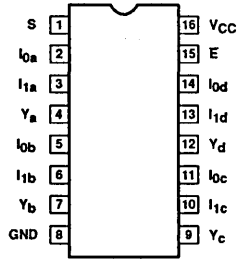
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
All	Inputs	1.0/1.0	20μA/0.6mA
Y_a - Y_d, $\overline{Y}_a$ - $\overline{Y}_d$	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

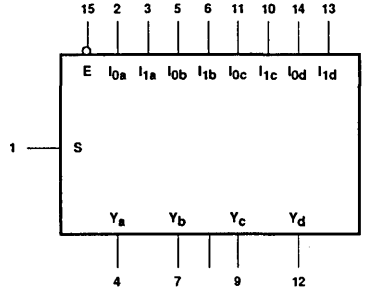
54F157A



For LLCC pin assignments, see JEDEC Standard No. 2

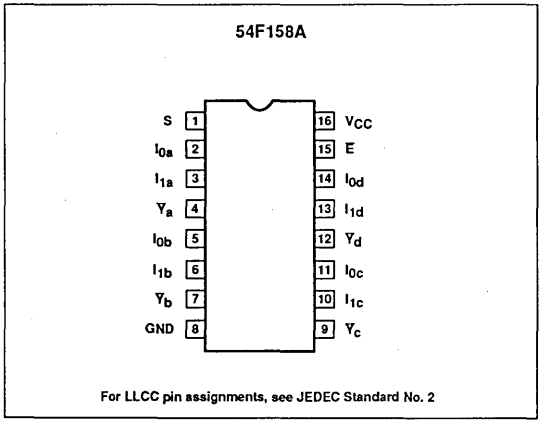
LOGIC SYMBOL

54F157A



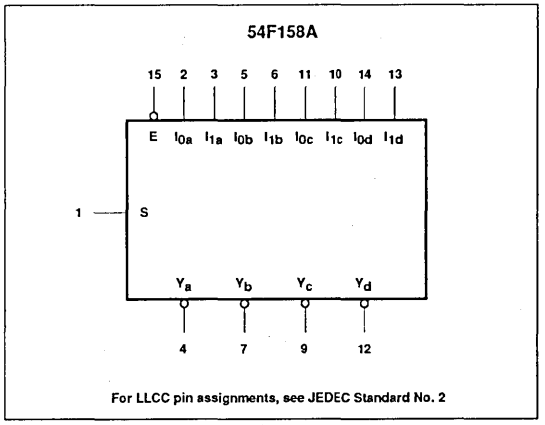
For LLCC pin assignments, see JEDEC Standard No. 2

PIN CONFIGURATION



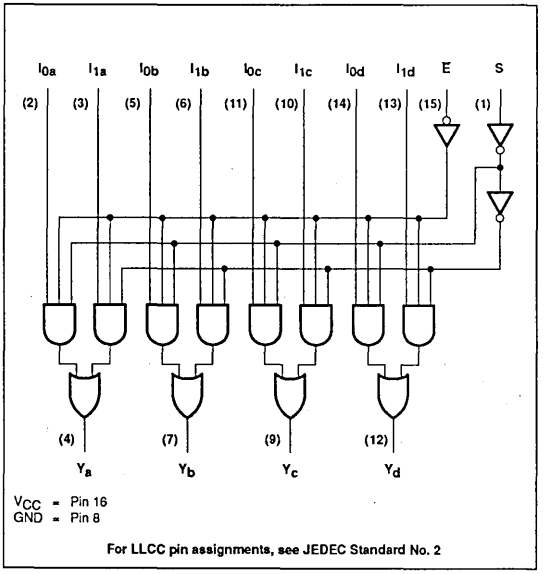
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



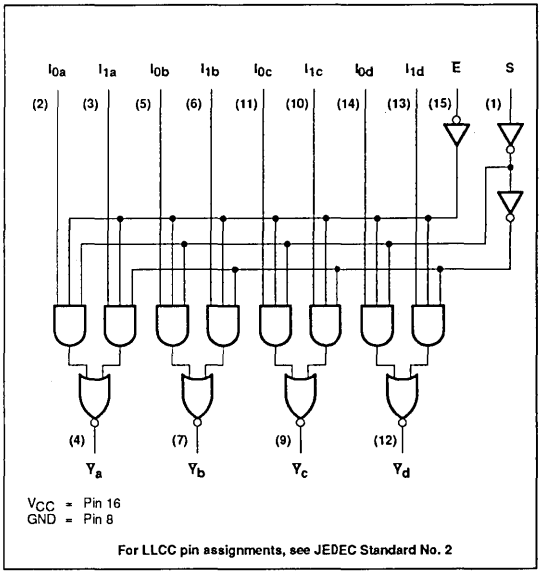
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM 54F157A



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM, 54F158A



For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE, 54F157A

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE, 54F158A

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V		5	100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V	-60	-80	-150	mA
I_{CC}	Supply current[4] (total)	'F157A	V_{CC} = Max		15.0	23.0	mA
		'F158A			10.0	15.0	mA

AC ELECTRICAL CHARACTERISTICS

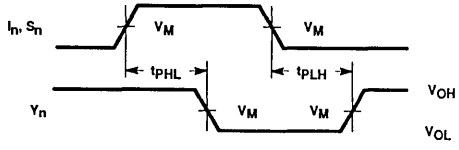
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	'F157A	Waveform 2	3.5 2.5	4.5 3.5	6.5 5.0	2.5 1.5	8.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	'F157A	Waveform 1	5.0 4.0	7.5 5.0	9.0 6.5	5.0 3.5	12.5 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	'F157A	Waveform 2	5.5 4.5	7.5 6.0	10.0 7.5	5.0 4.0	12.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	'F158A	Waveform 3	3.0 1.5	4.0 2.5	6.0 4.0	2.5 1.0	9.0 5.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	'F158A	Waveform 4	4.0 5.0	5.5 6.0	7.0 7.5	4.0 5.0	8.0 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	'F158A	Waveform 3	4.5 4.0	6.5 5.5	8.5 7.5	4.0 3.5	12.0 10.0	ns ns

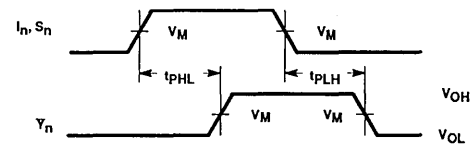
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

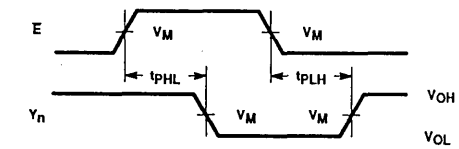
AC WAVEFORMS



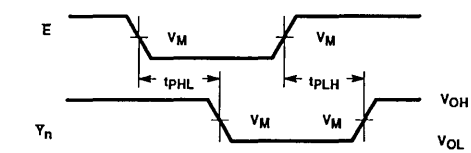
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



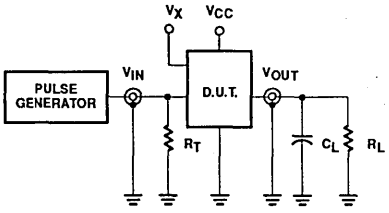
Waveform 3. For Inverting Outputs



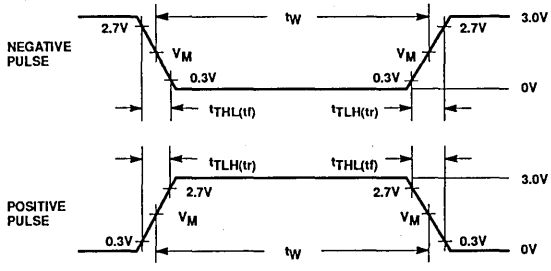
Waveform 4. For Non-Inverting Outputs

NOTE: For all waveforms V_M = 1.5V.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military FAST Products

54F161A, 54F163A
Counters

4-Bit Binary Counters

Product Specification

FEATURES

- **Synchronous counting and loading**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous reset (54F161A)**
- **Synchronous reset (54F163A)**
- **High-speed synchronous expansion**
- **Typical count rate of 120MHz**

DESCRIPTION

Synchronous 4-bit (54F161A, 54F163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F161A/BEA 54F163A/BEA
Ceramic Flat Pack	54F161A/BFA 54F163A/BFA
20-Pin Ceramic LLCC	54F161A/B2A 54F163A/B2A

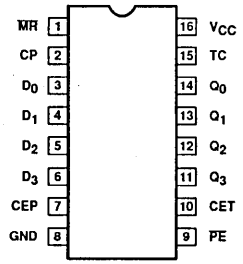
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CEP	Count enable parallel input	1.0/1.0	20μA/0.6mA
CET	Count enable trickle input	1.0/2.0	20μA/1.2mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous master reset input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous reset input (active Low)	1.0/2.0	20μA/1.2mA
D_0 - D_3	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input (active Low)	1.0/2.0	20μA/1.2mA
Q_0 - Q_3	Flip-flop outputs	50/33	1.0mA/20mA
tC	Terminal count output	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

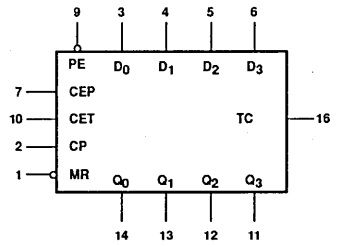
54F161A



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

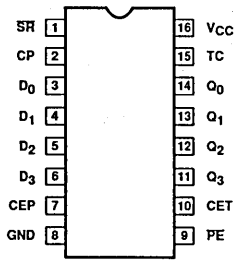
54F161A



For LLCC pin assignments, see JEDEC Standard No. 2

PIN CONFIGURATION

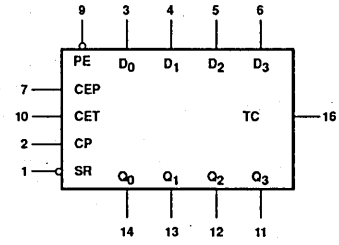
54F163A



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

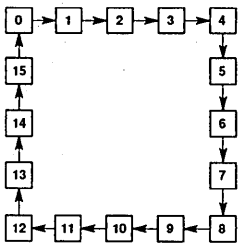
54F163A



For LLCC pin assignments, see JEDEC Standard No. 2

STATE DIAGRAM

Logic Equations: Count Enable =
CEP·CET·PE
TC = $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$



The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the positive-going edge of the clock (providing that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) in 54F161A to Low levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 54F163A, the clear function is synchronous. A Low level at the Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels after the next positive-going transition on the Clock (CP) input (providing that the setup and hold requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure B).

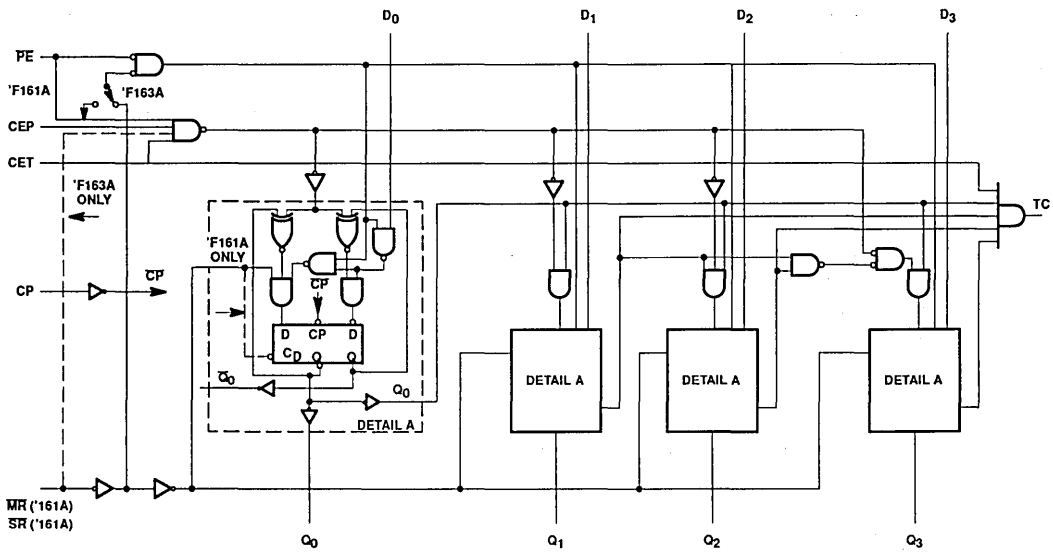
For conventional operation of 54F161A and 54F163A, the following transitions should be avoided:

1. High-to-Low transition on the CEP or CET input if Clock is Low.
2. Low-to-High transition on the Parallel Enable input when CP is Low, if the count enables and $\overline{MR}$ are High at or before the transition.

For 54F163A there is an additional transition to be avoided:

3. Low-to-high transition on the $\overline{MR}$ input when Clock is Low, if the Enable and $\overline{PE}$ inputs are High at or before the transition. The TC output is subject to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

LOGIC DIAGRAM



NOTE:
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT — FUNCTION TABLE, 54F161A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(1)
Count	H	↑	h	h	h	X	count	(1)
Hold (do nothing)	H	X	l	X	h	X	q_n	(1)
	H	X	X	l[2]	h	X	q_n	L

MODE SELECT — FUNCTION TABLE, 54F163A

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{SR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h	↑	X	X	l	l	L	L
	h	↑	X	X	l	h	H	(2)
Count	h	↑	h	h	h	X	count	(2)
Hold (do nothing)	h	X	l	X	h	X	q_n	(2)
	h	X	X	l	h	X	q_n	L

H = High voltage level steady state
L = Low voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
l = Low voltage level one setup time prior to Low-to-High clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

NOTES:
(1) The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 54F161A)
(2) The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 54F163A)

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			20.0	ma
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	$\overline{CET}$, $\overline{SR}$, $\overline{PE}$	V_{CC} = Max, V_I = 2.7V			40	µA
		Other inputs				20	µA
I_{IL}	Low-level input current	$\overline{CET}$, $\overline{SR}$, $\overline{PE}$	V_{CC} = Max, V_I = 0.5V			-1.2	mA
		Other inputs				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = Max			55	mA
		I_{CCL}				55	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		75[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1 $\overline{PE}$ = High	2.0 3.5	4.0 7.0	6.0 10.0	2.0 3.5	7.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1 $\overline{PE}$ = Low	2.5 4.0	4.0 6.0	7.0 8.5	2.0 4.0	8.5 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	5.0 5.0	10.0 14.0	14.0 16.0	5.0 5.0	16.5 18.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	Waveform 2	2.5 2.5	4.5 4.5	7.5 7.5	2.5 2.5	9.0 9.0	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n (54F161A)	Waveform 3	5.5	9.0	12.0	5.5	14.0	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC (54F161A)	Waveform 3	4.5		11.5	4.5	14.0	ns

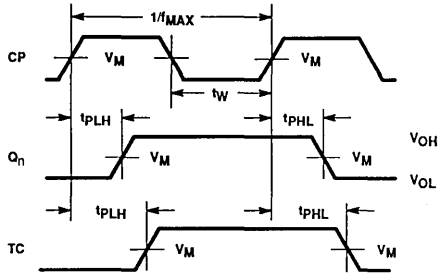
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 5	5.0 5.0			5.5 5.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 5	2.0 2.0			2.5 2.5		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 5 or 6	11.0 8.5			13.5 10.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 5 or 6	2.0 0			2.0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low CEP or CET to CP	Waveform 4	11.0 5.0			13.0 6.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low CEP or CET to CP	Waveform 4	2.0 0			2.0 0		ns ns
$t_w(H)$ $t_w(L)$	Clock pulse width (load), High or Low	Waveform 1	6.5 3.5			9.0 4.0		ns ns
$t_w(H)$ $t_w(L)$	Clock pulse width (count), High or Low	Waveform 1	6.5 3.5			9.0 4.0		ns ns
$t_w(L)$	$\overline{MR}$ pulse width Low (54F161A)	Waveform 3	5.0			9.5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP (54F161A)	Waveform 3	6.0			6.0		ns

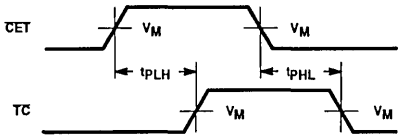
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CCH} is measured with $\overline{PE}$ input High, again with $\overline{PE}$ input Low, all other inputs High and outputs open. I_{CCL} is measured with Clock input High, again with Clock input Low all other inputs Low, and outputs open.
5. These parameters are guaranteed, but not tested.

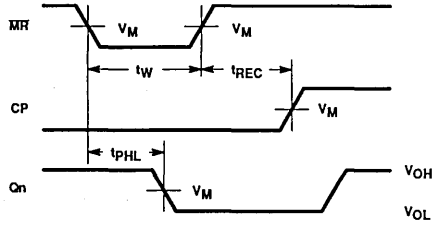
AC WAVEFORMS



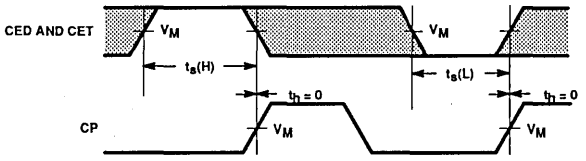
Waveform 1. Clock to Output Delays, Maximum Clock Frequency, and Clock Pulse Width



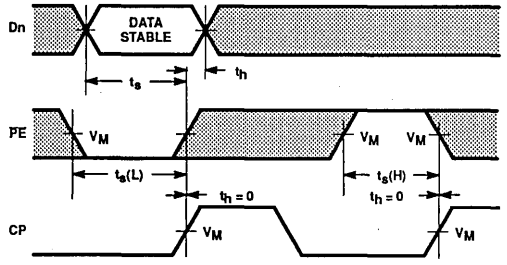
Waveform 2. Propagation Delays CET Input to TC Output



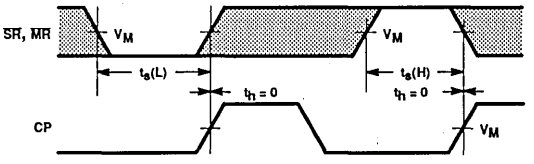
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time (54F161A)



Waveform 4. CEP and CET Setup and Hold Times



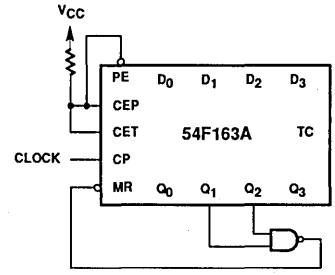
Waveform 5. Parallel Data and Parallel Enable Setup and Hold Times



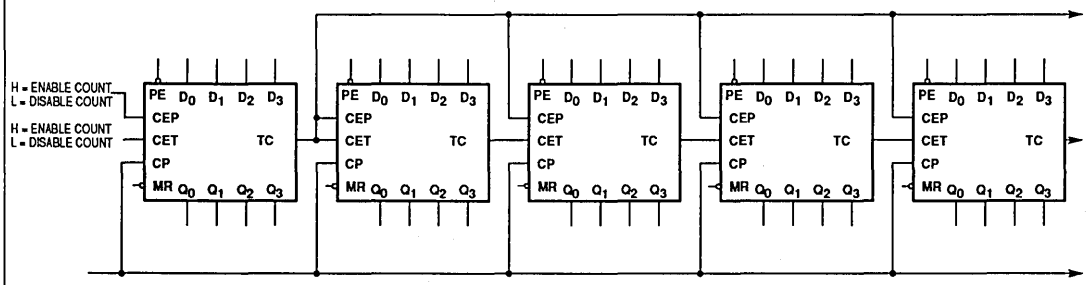
Waveform 6. Synchronous Reset Setup, Pulse Width and Hold Times (54F163A)

8NOTE: For all waveforms V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

APPLICATION DIAGRAM

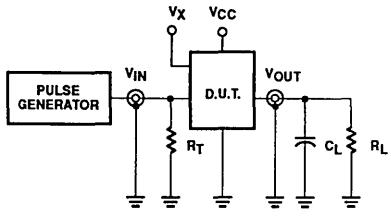


a. A Maximum Count Modifying Scheme
Terminal Count = 6

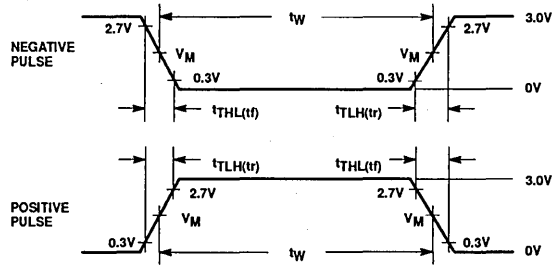


b. Synchronous Multistage Counting Scheme

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F164
Shift Register

8-Bit Serial-In Parallel-Out Shift Register

Product Specification

FEATURES

- **Gated serial data inputs**
- **Typical shift frequency of 90 MHz**
- **Asynchronous master reset**
- **Fully buffered Clock and Data inputs**
- **Fully synchronous data transfers**

DESCRIPTION

The 54F164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (Dsa · Dsb); either input can be used as an active High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two data inputs (Dsa · Dsb) that existed one set-up time before the rising clock edge. A Low level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

ORDERING INFORMATION

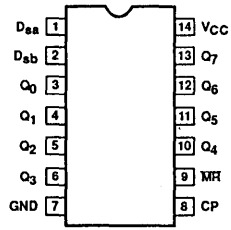
DESCRIPTION	ORDER CODE
Ceramic DIP	54F164/BCA
Ceramic Flat Pack	54F164/BDA
Ceramic LLCC	54F164/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_{sa}, D_{sb}	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (active Low)	1.0/1.0	20μA/0.6mA
Q_0 - Q_7	Outputs	50/33	1.0mA/20mA

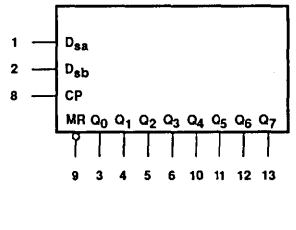
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

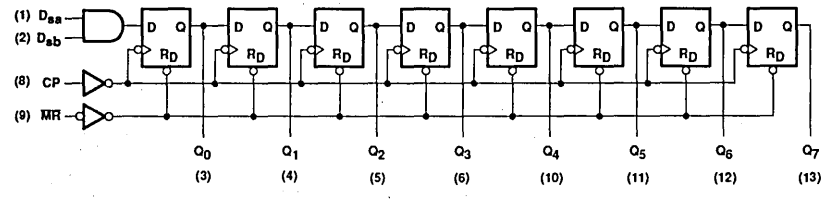
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

Shift Register | 54F164

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1	—	Q_7
Reset	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q_0	—	q_6
	H	↑	l	h	L	q_0	—	q_6
	H	↑	h	l	L	q_0	—	q_6
	H	↑	h	h	H	q_0	—	q_6

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High Clock transition
q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High Clock transition
X = Don't care
↑ = Low-to-High Clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V		5	100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-60	-80	-150	mA
I_{CC}	Supply current (total)	V_{CC} = Max		33	50	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	80	90		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.5 5.0	6.0 7.5	8.0 11.0	4.5 5.0	10 13	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	5.5	10.5	13	5.5	14	ns

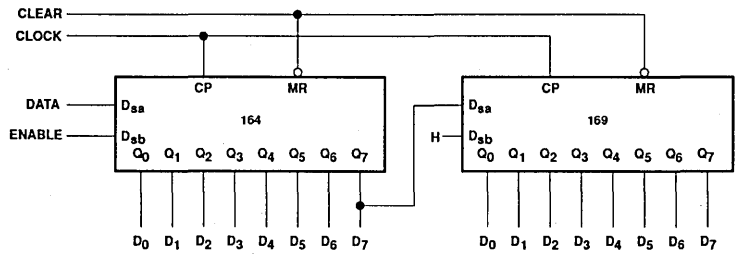
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time High or Low A or B to CP	Waveform 3	7.0 7.0			7.0 7.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low A or B to CP		1.0 1.0			1.0 1.0		ns ns
t_w(H) t_w(L)	CP pulse width, High or Low	Waveform 1	4.0 7.0			4.0 7.0		ns ns
t_w(L)	$\overline{MR}$ pulse width Low	Waveform 2	7.0			7.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.0			9.0		ns

NOTES:

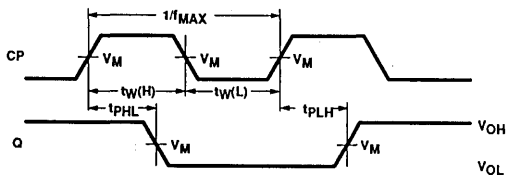
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type per the functional table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the serial inputs grounded, the clock input at 2.4V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.
5. Parameter guaranteed, but not tested.

APPLICATION DIAGRAM

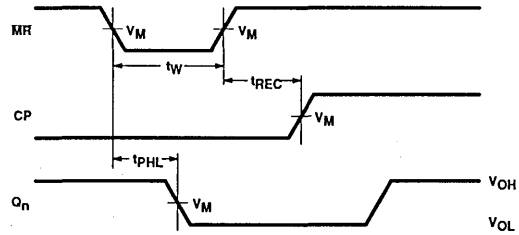


NOTE:
The 54F164 can be cascaded to form synchronous shift registers of longer length.
Here, two devices are combined to form a 16-bit shift register.

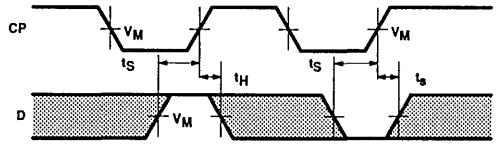
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



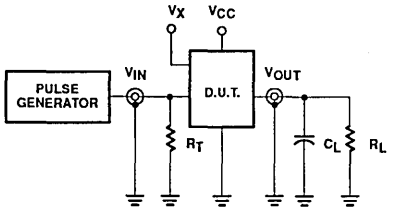
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



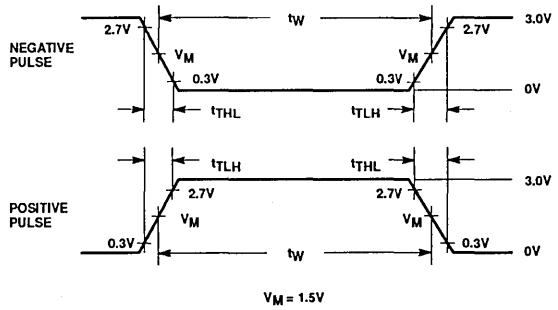
Waveform 3. Data Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

54F169
Counter

4-Bit Up/Down Binary Synchronous Counter

Product Specification

FEATURES

- **Synchronous counting and loading**
- **Up/Down counting**
- **Modulo 16 binary counter**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Built-in lookahead carry capability**
- **Presettable for programmable operation**

DESCRIPTION

The 54F169 is a synchronous, presettable Modulo 16 up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the Low-to-High transition of the clock.

ORDERING INFORMATION

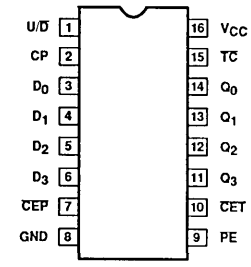
DESCRIPTION	ORDER CODE
Ceramic DIP	54F169/BEA
Ceramic Flat Pack	54F169/BFA
Ceramic LLCC	54F169/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CEP}$	Count enable parallel input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active Low)	1.0/2.0	20μA/1.2mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
D_0 - D_3	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input (active Low)	1.0/1.0	20μA/0.6mA
U/$\overline{D}$	Up/down count control input	1.0/1.0	20μA/0.6mA
Q_0 - Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

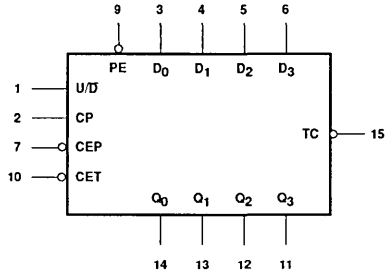
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A Low level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

The direction of counting is controlled by the Up/Down (U/$\overline{D}$) input; a High will cause the count to increase, a Low will cause the count to decrease.

The carry lookahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET}$·$\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be Low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal to the High level portion of the Q_0 output. This Low level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure 1 for the fast synchronous multi-stage counting connections.

FUNCTIONAL DESCRIPTION

The 54F169 uses edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the Clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is Low, the data on the D_0 - D_3 inputs enter the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be Low and $\overline{PE}$ must be High; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally High and goes Low, provided that $\overline{CET}$ is Low, when a counter reaches zero in the Count Down mode or reaches 15 in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP}$·$\overline{CET}$·$\overline{PE}$

2) Up: $\overline{TC} = Q_0 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$

3) Down: $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/\overline{D}) \cdot \overline{CET}$

MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	ACTION ON RISING CLOCK EDGE
L	X	X	X	Load ($D_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = High Voltage
L = Low Voltage Level
X = Don't care

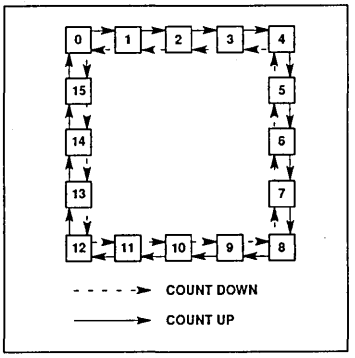
MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel load	↑	X	X	X	l	l	L	(1)
	↑	X	X	X	l	h	H	(1)
Count Up	↑	h	l	l	h	X	Count Up	(1)
Count Down	↑	l	l	l	h	X	Count Down	(1)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(1)
	↑	X	X	h	h	X	q_n	H

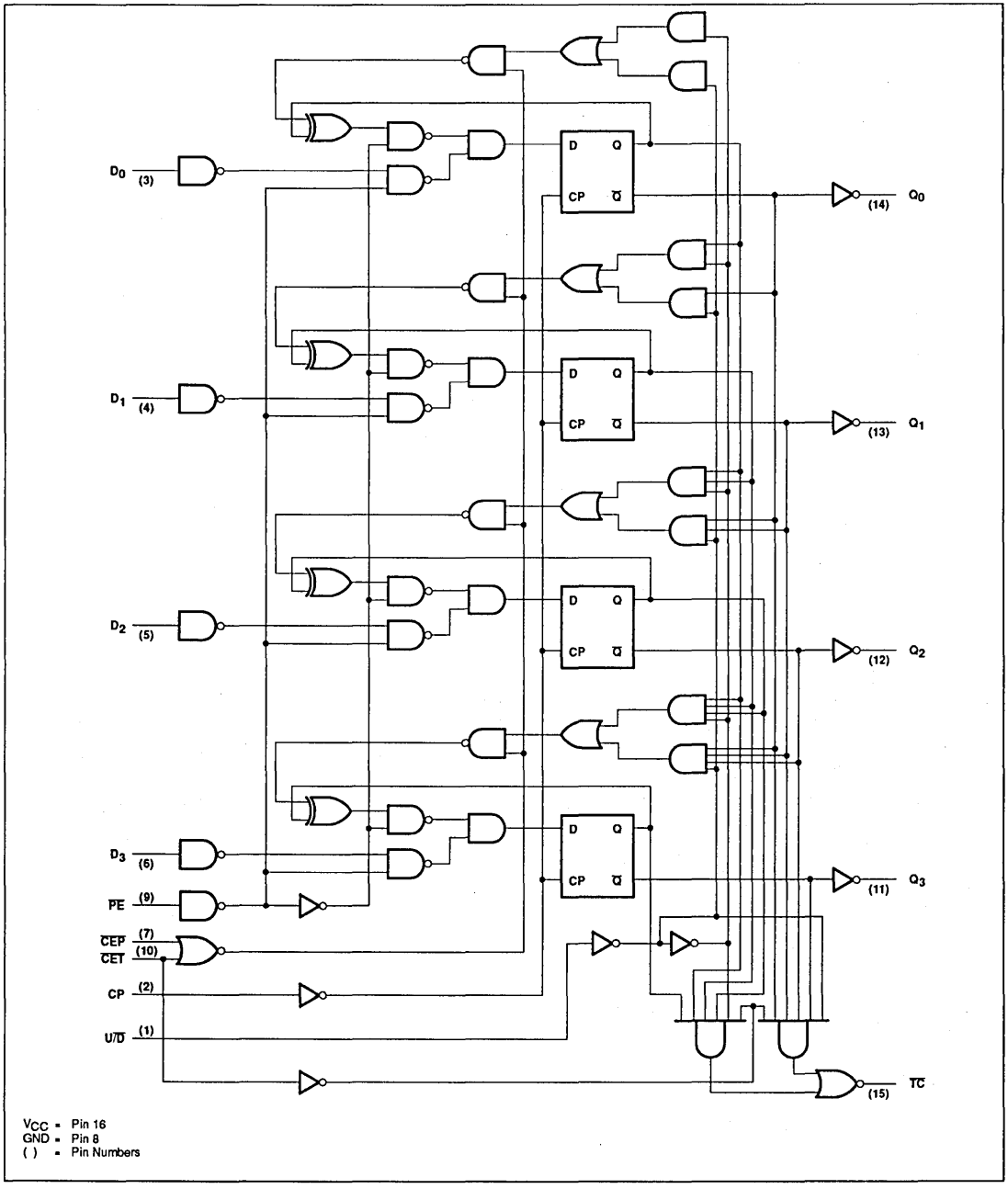
H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

NOTE:
1. The $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL).

STATE DIAGRAM



LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin Numbers

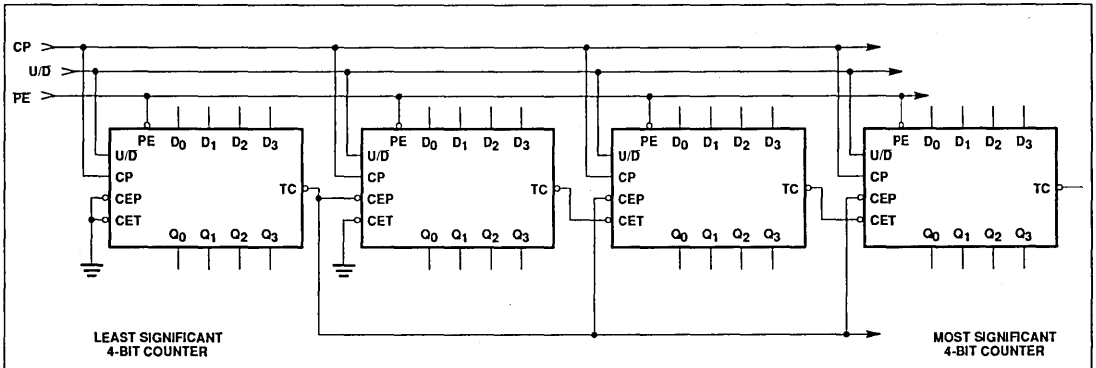


Figure 1. Synchronous Multistage Counting Scheme

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OH} = Max	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH1}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH2}	High-level input current		V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level intput current	$\overline{CET}$ input	V_{CC} = Max, V_I = 0.5V			-1.2	mA
		Other inputs				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = Max		35	52	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	90	115		75		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, High or Low)	Waveform 1	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	9.5 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 4.0	12.0 8.5	15.5 11.0	5.5 4.0	18.0 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	2.5 2.5	4.5 6.0	6.0 8.0	2.5 2.5	7.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 3	3.5 4.0	8.5 8.0	12.0 10.5	3.5 4.0	16.5 13.0	ns ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 4	4.0 4.0			4.5 4.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 4	3.0 3.0			3.5 3.5		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 5.0			5.5 5.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low $\overline{PE}$ to CP	Waveform 4	8.0 8.0			9.0 9.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low U/$\overline{D}$ to CP	Waveform 6	11.0 7.0			12.5 8.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP	Waveform 6	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP pulse width High or Low	Waveform 1	5.0 5.0			5.5 5.5		ns ns

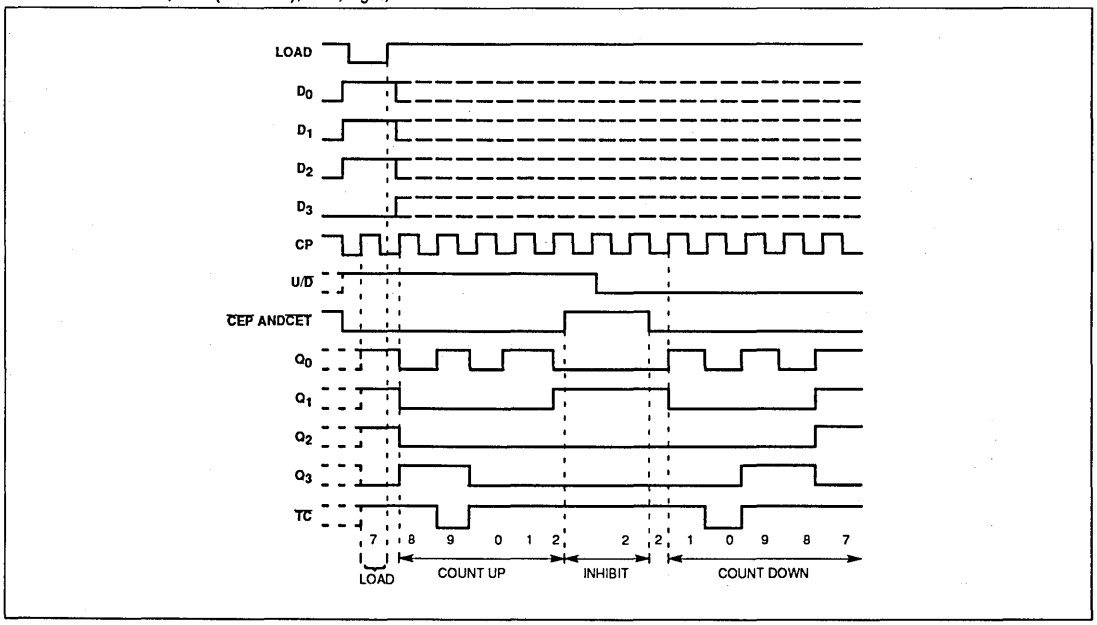
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after applying a momentary ≥ 4.0V, then ground to the clock input with all other inputs grounded and outputs open.

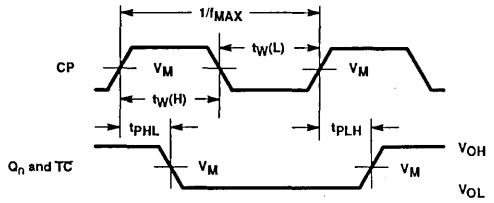
WAVEFORM (Typical Load, Count, and Inhibit Sequences)

Illustrated below is the following sequence for the 54F168. The operation of the 54F169 is similar.

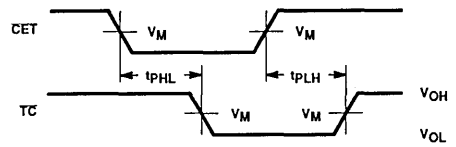
1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



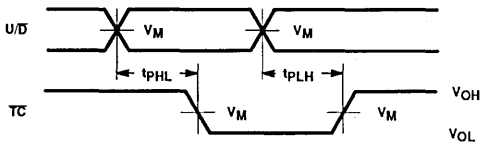
AC WAVEFORMS



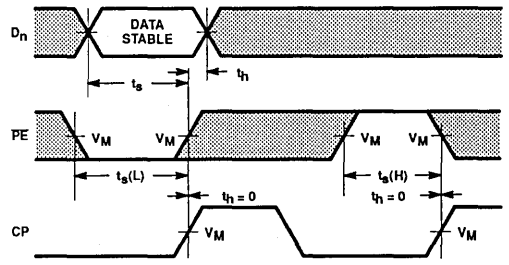
Waveform 1. Clock to Output Delays and Clock Pulse Width



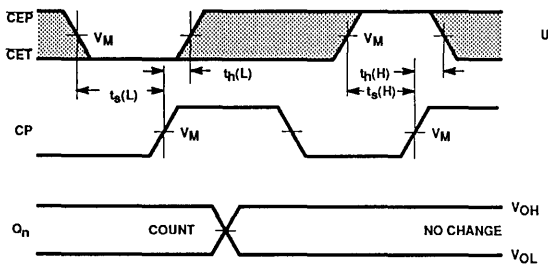
Waveform 2. Propagation Delays CET Input to Terminal Count Output



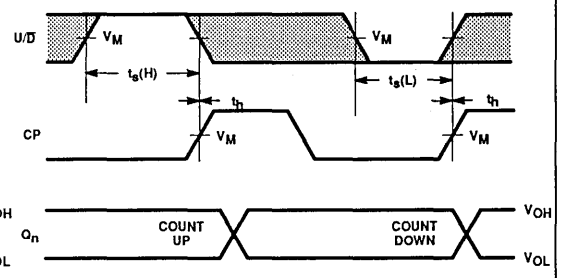
Waveform 3. Propagation Delays U/D Control to Terminal Count Output



Waveform 4. Parallel Data and Parallel Enable Set-up and Hold Times



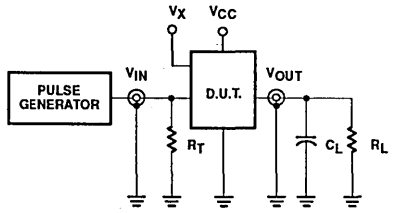
Waveform 5. Count Enable Set-Up and Hold Times



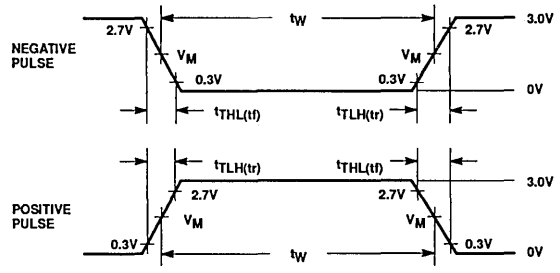
Waveform 6. Up/Down Control Set-Up and Hold Times

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

54F173
Flip-Flop

Quad D-Type Flip-Flop (3-State)

Product Specification

DESCRIPTION

The 54F173 is a high-speed 4-bit parallel load register with clock enable control, 3-State buffered outputs and Master Reset (MR). When the two clock Enable ($\overline{E}_0$ and $\overline{E}_1$) inputs are Low, the data on the D inputs is loaded into the register simultaneously with Low-to-High Clock (CP) transition. When one or both $\overline{E}$ inputs are High one setup time before the Low-to-High clock transition, the register retains the previous data. Clock (CP) is a fully triggered input.

The Master Reset (MR) is an active High asynchronous input. When the MR is High, all four flip-flops are reset (outputs Low) independently of any other input condition. The 3-State output buffers are controlled by a 2-input NOR gate. When both Output Enable ($\overline{OE}_0$ and $\overline{OE}_1$) inputs are Low, the data in the register is presented at the Q outputs. When one or both OE inputs are High, the outputs are forced to a High impedance "off" state. The 3-State output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

FEATURES

- **Edge-triggered D-type register**
- **Gated clock enable for held "do nothing" mode**
- **3-State output buffers**
- **Gated output enable control**
- **Speed upgrade of N8T10 and current sink upgrade**
- **Controlled output edges to minimize ground bounce**
- **48mA sinking capability**

ORDERING INFORMATION

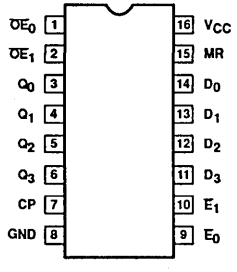
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F173/BEA
16-Pin Ceramic FlatPack	54F173/BFA
20-Pin Ceramic LLCC	54F173/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20µA/0.6mA
CP	Clock input	1.0/1.0	20µA/0.6mA
$\overline{E}_0$, $\overline{E}_1$	Clock Enable input	1.0/1.0	20µA/0.6mA
MR	Master Reset input	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable input	1.0/1.0	20µA/0.6mA
Q_0 - Q_3	Data outputs	600/80	12mA/48mA

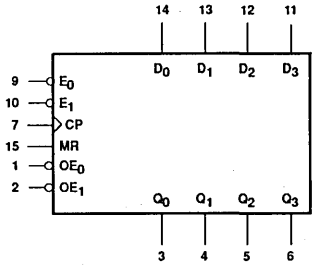
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



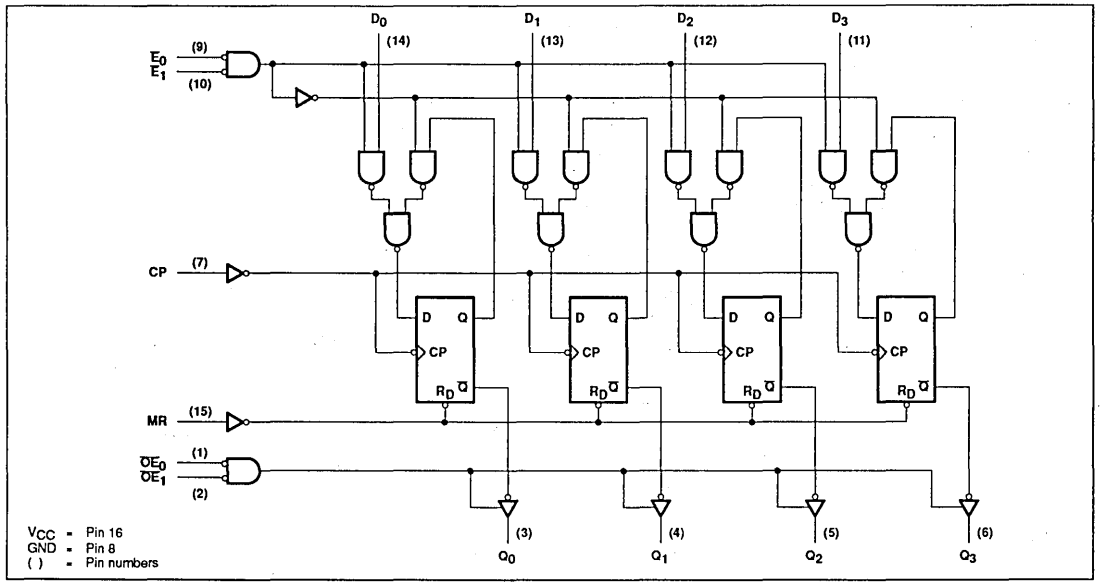
For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_0$	$\overline{E}_1$	D_R	Q_R (Register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (do nothing)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	Q_R (Register)	$\overline{OE}_0$	$\overline{OE}_1$	Q_R
Read	L	L	L	L
	H	L	L	H
Disabled	X	H	X	(Z)
	X	X	H	(Z)

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the Low-to-High clock transition
X = Don't care
(Z) = High impedance "off" state
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min,	I_{OH} = Max	2.0			V
			V_{IL} = Max,	I_{OH} = -1mA	2.5			V
			V_{IH} = Min	I_{OH} = -3mA	2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max			0.38	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = Max, V_I = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = Max, V_I = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			19	26	mA
		I_{CCL}				27	37	mA
		I_{CCZ}				23	32	mA

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	105	125		80[4]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.5 6.0	6.5 8.0	9.0 10.5	4.0 5.5	10.0 11.5	ns ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 2	6.5	8.5	11.5	6.0	12.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	Waveform 4 Waveform 5	3.5 5.5	5.0 7.0	8.0 10.0	2.5 4.5	8.5 11.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	Waveform 4 Waveform 5	1.5 3.0	3.5 5.0	7.0 8.5	1.0 2.5	8.0 9.0	ns ns
t_{TLH} t_{THL}	Output Transition Time 10% to 90%, 90% to 10%	Waveform 4 Waveform 5	4.0 2.0	7.5 5.0	10.0[4] 8.0[4]	4.0 2.0	11.0[4] 8.5[4]	ns ns

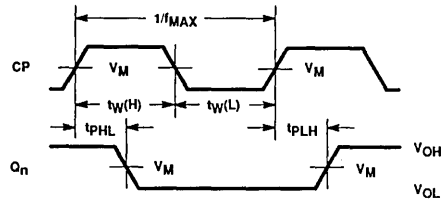
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time D_n to CP	Waveform 3	2.5 2.5			3.0 4.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP	Waveform 3	0 0			2.0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{E}_n$ to CP	Waveform 3	4.5 7.5			5.0 8.5		ns ns
$t_h(H)$ $t_h(L)$	Setup time $\overline{E}_n$ to CP	Waveform 3	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 6.0			3.0 6.0		ns ns
$t_w(H)$	MR pulse width High	Waveform 2	3.5			3.5		ns
t_{rec}	Recovery time MR to CP	Waveform 2	4.5			5.5		ns

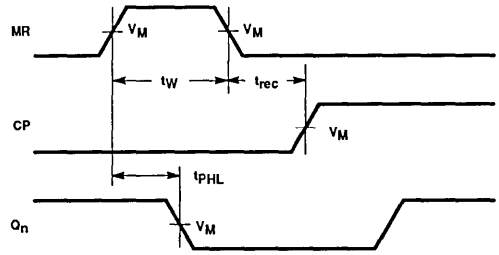
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable conditions and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.
4. These parameters are guaranteed, but not tested.

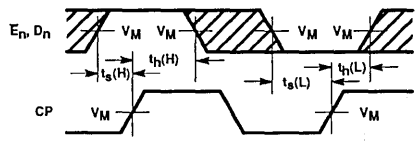
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock and Enable Inputs to Outputs, Clock and Enable Widths and Maximum Clock Frequency

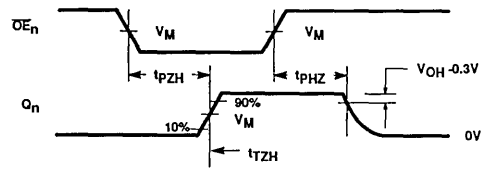


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

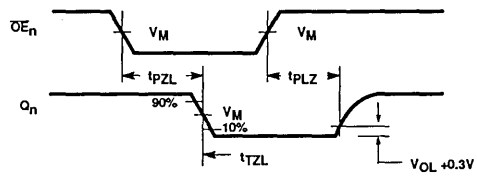


The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Data and Select Setup and Hold Times



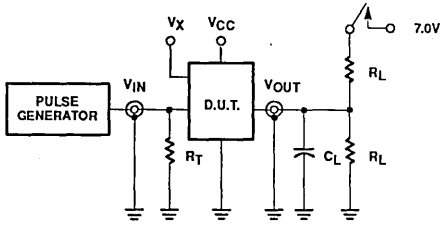
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



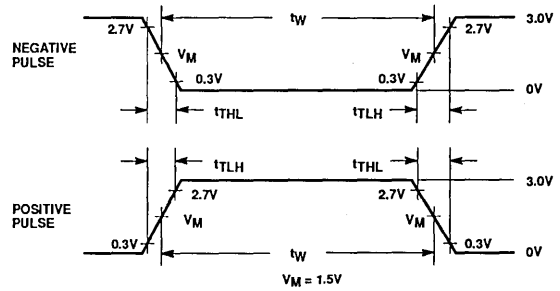
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

VM = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

54F174
Flip-Flop

Hex D Flip-Flops

Product Specification

Military Logic Products

FEATURES

- **Six edge-triggered D-type flip-flops**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**

DESCRIPTION

The 54F174 has six edge-triggered flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independent of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where true outputs only are required, and the Clock and Master Reset are common to all storage elements.

ORDERING INFORMATION

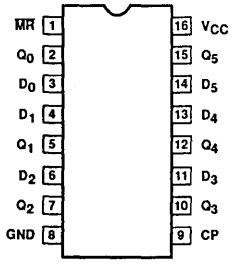
DESCRIPTION	ORDER CODE
Ceramic DIP	54F174/BEA
Ceramic Flat Pack	54F174/BFA
Ceramic LLCC	54F174/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_5	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse inputs (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/5	20μA/0.6mA
Q_0 - Q_5	Data outputs	50/33	1.0mA/20mA

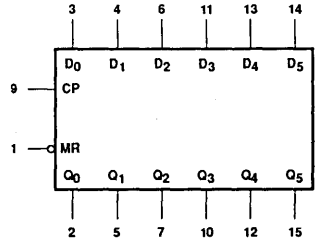
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

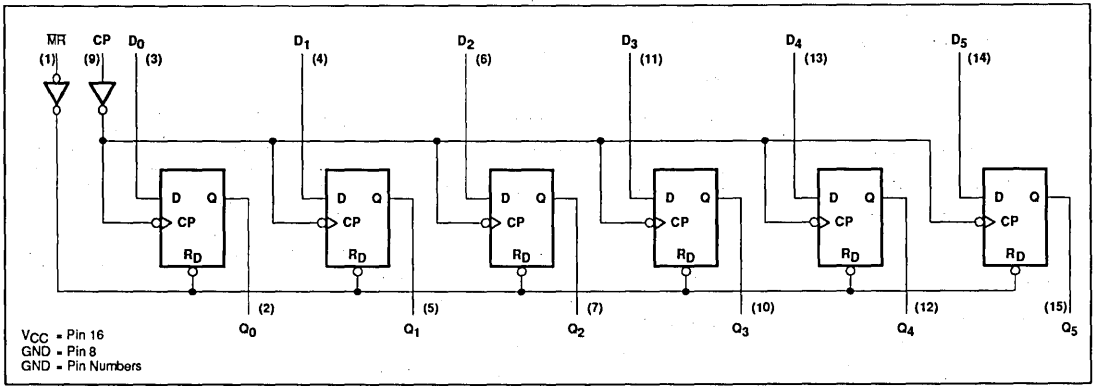
LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

Flip-Flop | 54F174

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = High voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the Low-to-High Clock transition.
X = Don't Care.
↑ = Low-to-High Clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-60	-80	-150	mA
I_{CC}	Supply current (total)	V_{CC} = Max, D_n = $\overline{MR}$ = 4.5V, CP = ↑		35	45	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

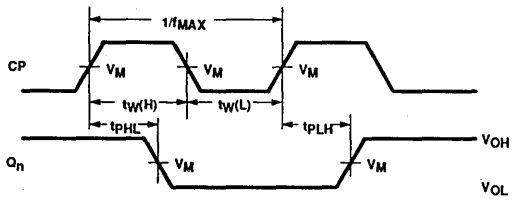
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	80	100		80		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_n	Waveform 1	3.5 4.5	5.5 6.0	8.0 10.0	3.0 4.0	9.5 11.5	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	5.0	8.5	14.0	4.5	15.5	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

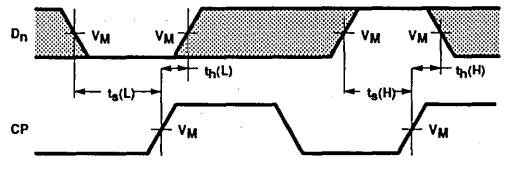
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 2	4.0 4.0			4.0 4.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	Waveform 2	0 0			0 0		ns ns
t_w(H) t_w(L)	CP pulse width, High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns ns
t_w(L)	$\overline{MR}$ pulse width Low	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			6.0		ns

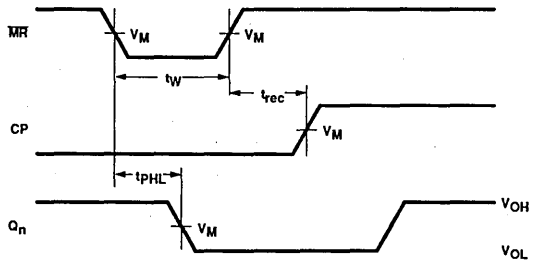
AC WAVEFORMS



Waveform 1. Clock to Output Delays, Clock Pulse Width, and Maximum Clock Frequency



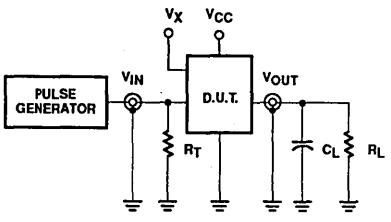
Waveform 2. Data Setup and Hold Times



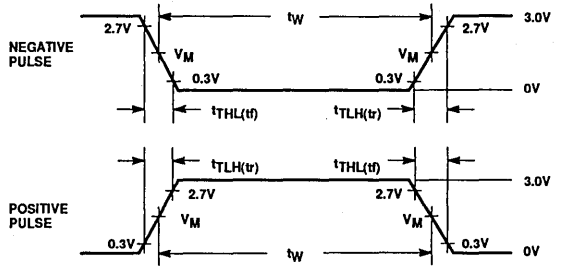
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

54F175
Flip-Flop

Quad D Flip-Flop

Product Specification

Military Logic Products

FEATURES

- **Four edge-triggered D flip-flops**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**
- **True and complementary output**

DESCRIPTION

The 54F175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced LOW independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

ORDERING INFORMATION

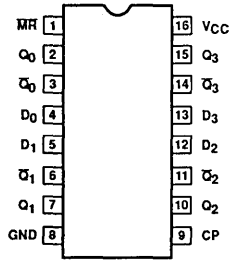
DESCRIPTION	ORDER CODE
Ceramic DIP	54F175/BEA
Ceramic Flat Pack	54F175/BFA
Ceramic LLCC	54F175/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset input (active Low)	1.0/1.0	20μA/0.6mA
Q_0 - Q_3	True outputs	50/33	1.0mA/20mA
$\overline{Q}_0$ - $\overline{Q}_3$	Complementary outputs	50/33	1.0mA/20mA

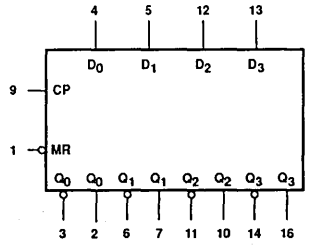
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

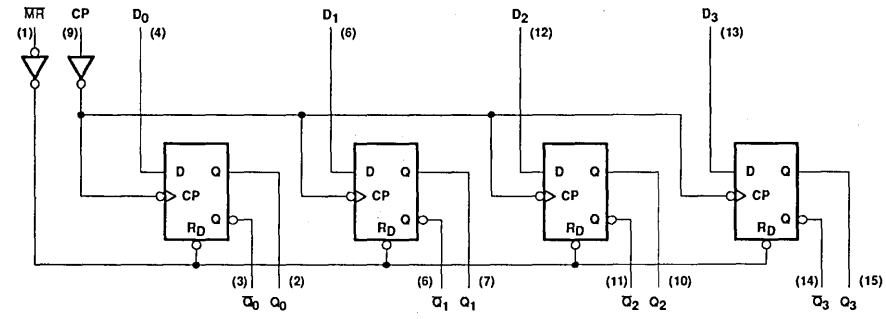
LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

Flip-Flop | 54F175

LOGIC DIAGRAM



For LLCC pin assignment, see JEDEC Standard No. 2.

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = High voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the Low-to-High Clock transition.
X = Don't Care.
↑ = Low-to-High Clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1,4]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = Max, D_n = $\overline{MR} \geq 4.0V$, CP = ↑		25	34	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	100	140		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	Waveform 1	4.0 4.0	5.0 6.5	6.5 8.5	3.5 4.0	8.5 10.5	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 3	4.5	9.0	11.5	4.5	15	ns
t_{PLH}	Propagation delay $\overline{MR}$ to $\overline{Q}_n$	Waveform 3	4.0	6.5	8.0	4.0	10	ns

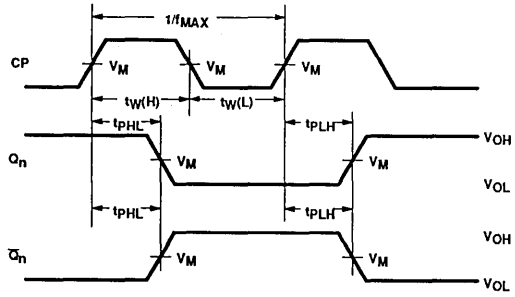
NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. When testing devices to the functional table specified refer to the "Recommended Operating Conditions Section" of Application Note 202, "Testing and Specifying FAST Logic".
5. These parameters are guaranteed, but not tested.

Flip-Flop | 54F175

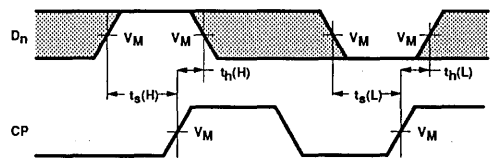
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	3.0 3.0			3.0 3.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns ns
$t_w(L)$	$\overline{MR}$ pulse width Low	Waveform 3	5.0			5.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			5.0		ns

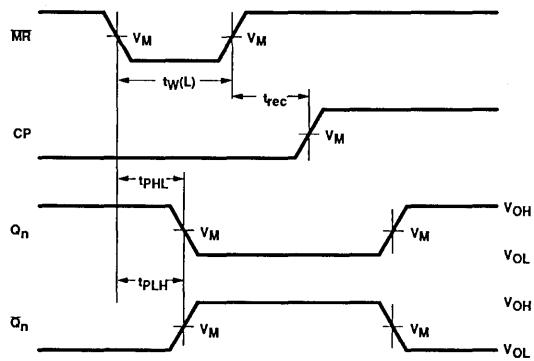
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



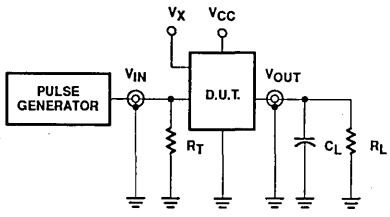
Waveform 2. Data Setup and Hold Times



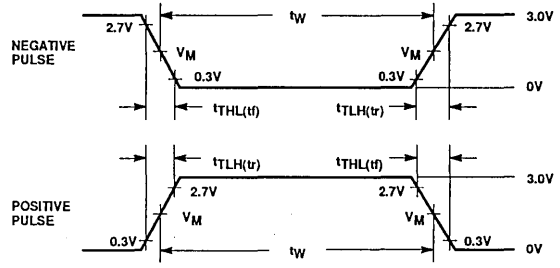
Waveform 3. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

NOTE: For all waveforms V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F181
Arithmetic Logic Unit

4-Bit Arithmetic Logic Unit

Product Specification

FEATURES

- **Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations**
- **Full lookahead carry for high-speed arithmetic operation on long words**
- **40% faster than 54S181 with only 30% 54S181 power consumption**

DESCRIPTION

The 54F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0 - S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active High or active Low operands. The Function Table lists these operations.

ORDERING INFORMATION

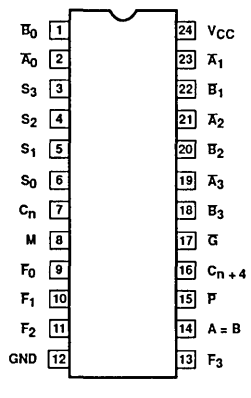
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP (300mil)	54F181/BLA
24-Pin Ceramic DIP (600mil)	54F181/BJA
24-Pin Ceramic FlatPack	54F181/BSA
24-Pin Ceramic LLCC	54F181/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
M	Mode control input	1.0/1.0	20μA/0.6mA
$\overline{A}_0$ - $\overline{A}_3$, $\overline{B}_0$ - $\overline{B}_3$	Operand Inputs	1.0/1.0	20μA/0.6mA
S_0 - S_3	Function select inputs	1.0/1.0	20μA/0.6mA
C_n	Carry input	1.0/1.0	20μA/0.6mA
C_{n+4}	Carry output	50/33	1.0mA/20mA
A = B	Compare output	*OC/33	*OC/20mA
$\overline{F}_0$ - $\overline{F}_3$	Outputs	50/33	1.0mA/20mA
$\overline{G}$	Carry generate output	50/33	1.0mA/20m/A
$\overline{P}$	Carry propagate output	50/33	1.0mA/20mA

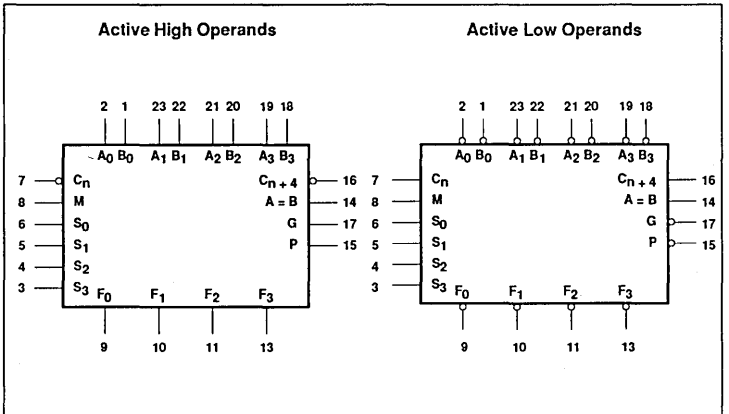
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.
*OC = Open collector

PIN CONFIGURATION



For LLCC Pin Assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignments, see JEDEC Standard No. 2

Arithmetic Logic Unit | 54F181

When the Mode Control input (M) is High, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the 54F182 carry lookahead circuit. One carry lookahead package is required for each group of four 54F181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes High when all four $\overline{F}$ outputs are High and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open collector and can be wired - AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active Low inputs producing active Low outputs or with active High inputs producing active High outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

MODE SELECT — FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M = H)	Arithmetic ** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	Logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}+B$	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	$A+\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

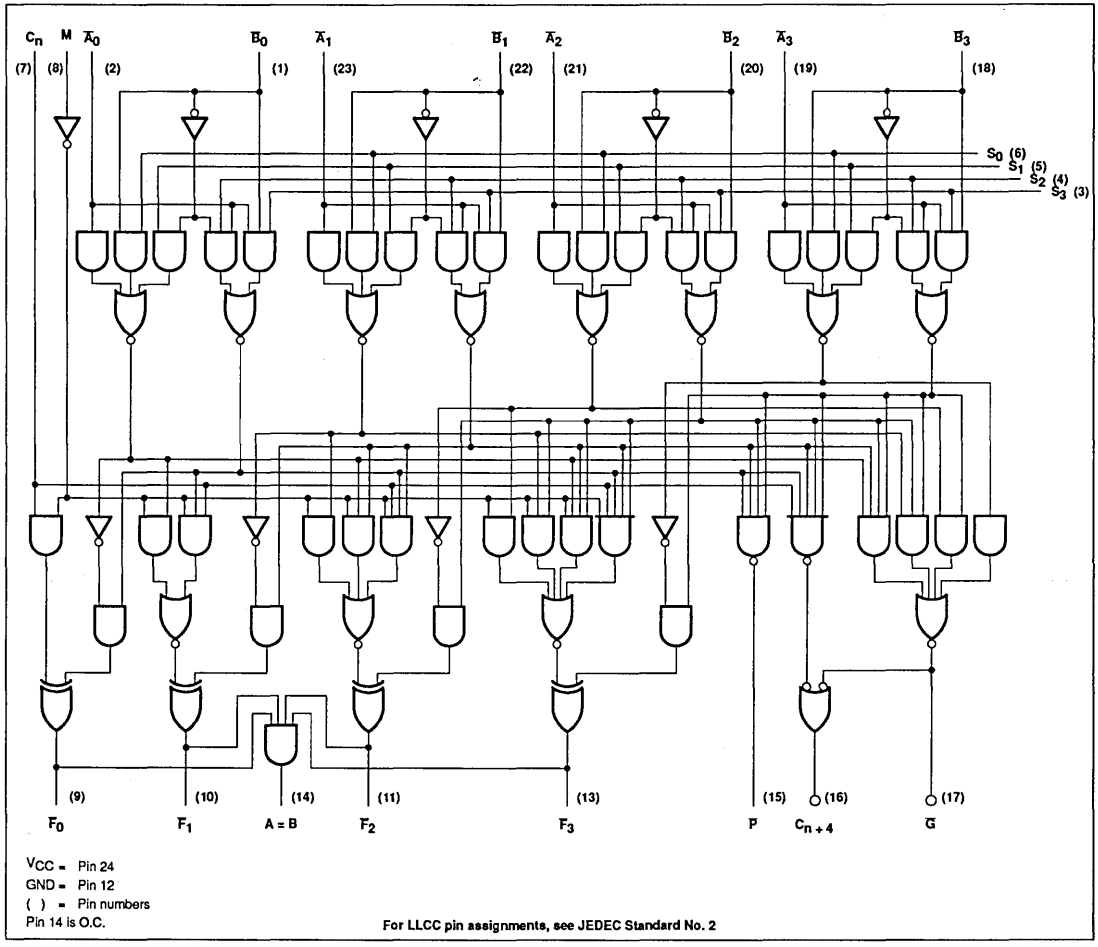
L = Low voltage level
H = High voltage level
* Each bit is shifted to the next more significant position.
** Arithmetic operations expressed in 2s complement notation.

MODE SELECT — FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M = H)	Arithmetic ** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A} + B$	$A\overline{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\overline{A + B}$	A plus $(A + \overline{B})$
L	H	L	H	$\overline{B}$	AB plus $(A + \overline{B})$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	$A + \overline{B}$	$A + \overline{B}$
H	L	L	L	$\overline{A}B$	A plus (A + B)
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	$A\overline{B}$	AB plus A
H	H	H	L	AB	$A\overline{B}$ plus A
H	H	H	H	A	A

L = Low voltage level
H = High voltage level
* Each bit is shifted to the next more significant position.
** Arithmetic operations expressed in 2s complement notation.

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers
Pin 14 is O.C.

For LLCC pin assignments, see JEDEC Standard No. 2

SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

SYMBOL	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_1$	$\overline{B}_1$	None	Remaining $\overline{A}$ and B	C_N	$\overline{F}_1$
t_{PLH} t_{PHL}	$\overline{B}_1$	$\overline{A}_1$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_1$
t_{PLH} t_{PHL}	$\overline{A}_1$	$\overline{B}_1$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_1$	$\overline{A}_1$	**None**	**None**	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_1$	None	$\overline{B}_1$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_1$	None	$\overline{A}_1$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_1$	None	$\overline{B}_1$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_1$	None	$\overline{A}_1$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

SUM MODE TEST TABLE II

FUNCTION INPUTS: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

SYMBOL	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_1$	None	$\overline{B}_1$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_1$
t_{PLH} t_{PHL}	$\overline{B}_1$	$\overline{A}_1$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_1$
t_{PLH} t_{PHL}	$\overline{A}_1$	None	$\overline{B}_1$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_1$	$\overline{A}_1$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_1$	$\overline{B}_1$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_1$	None	$\overline{A}_1$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_1$	None	$\overline{B}_1$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}_1$	$\overline{A}_1$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}_1$	$\overline{B}_1$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_1$	None	$\overline{A}_1$	None	Remaining $\overline{A}$ and $\overline{B}_1$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

SUM MODE TEST TABLE III

SYMBOL	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_1$	$\overline{B}_1$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	F_1	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	$\overline{B}_1$	$\overline{A}_1$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	F_1	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.50	5.0	5.50	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output current	A = B			4.5	V
I_{OH}	High-level output current	Any output except A = B			-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Any output except A = B	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OH} = Max		2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH1}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH2}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level intput current		V_{CC} = Max, V_I = 0.5V	Mode input			-0.6	mA
				A or B inputs			-1.8	mA
				S inputs			-2.4	mA
				Carry input			-3.0	mA
I_{OH}	High-level output current	A = B only	V_{CC} = Max, V_{IH} = Min, V_{IL} = Max, V_{OH} = 4.5V				250	µA
I_{OS}	Short-circuit output current[3]	Any output except A = B	V_{CC} = Max		-60	-80	-150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = Max	$S_0 - S_3 = M = \overline{A}_0 - \overline{A}_3 \geq 4.0V$ $B_0 - B_3 = C_n$ = GND		43	65	mA
		I_{CCL}		$S_0 - S_3 = M = \geq 4.0V$ $B_0 - B_3 = C_n = \overline{A}_0 - \overline{A}_3$ = GND		43	65	mA

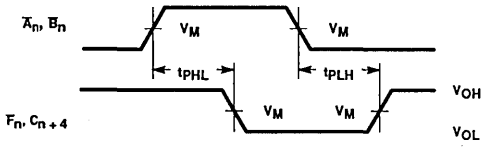
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with all outputs open.

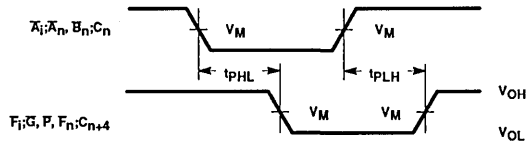
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS				LIMITS					UNIT
		Mode	Table	Wave-form	Conditions	T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55 to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
						Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Sum Diff	I II	2	M = 0V	3.0 3.0	6.4 6.1	8.5 8.0	3.0 3.0	12.0 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Sum	I	1	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	5.0 5.0	10.0 9.4	13.0 12.0	5.0 5.0	18.0 17.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to C_{n+4}	Diff	II	4	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	5.0 5.0	10.8 10.0	14.0 13.0	5.0 5.0	19.5 18.0	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	Diff Sum	II I	2	M = 0V	3.0 3.0	6.7 6.5	8.5 8.5	3.0 3.0	12.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Sum	I	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	3.0 3.0	5.7 5.8	7.5 7.5	3.0 3.0	10.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{G}$	Diff	II	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	3.0 3.0	6.5 7.3	8.5 9.5	3.0 3.0	12.0 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Sum	I	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	3.0 3.0	5.0 5.5	7.0 7.5	3.0 3.0	10.0 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{P}$	Diff	II	3	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	4.0 4.0	5.8 6.5	7.5 8.5	3.0 3.0	10.5 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	I	2	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$	3.0 3.0	7.0 7.2	9.0 10.0	3.0 3.0	12.5 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Diff	II	3	$M = S_0 = S_3 = 0V$ $S_1 = S_2 = 4.5V$	3.0 3.0	8.2 8.0	11.0 11.0	3.0 3.0	14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	Sum		1, 2		4.0 4.0	8.0 7.8	10.5 10.0	3.0 3.0	15.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to $\overline{F}_n$	Diff		1, 2		4.5 4.5	9.4 9.4	12.0 12.0	3.0 3.0	17.0 17.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to$\overline{F}_i$	Logic	III	3	M = 4.5V	4.0 4.0	6.0 6.0	9.0 10.0	3.0 3.0	12.5 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ or $\overline{B}_n$ to A = B	Diff	II	3	$M = S_0 = S_3 = 0V$ $S_1 = S_2 = 4.5V$	11.0 7.0	18.5 9.8	27.0 12.5	10.0 6.0	32.0 18.0	ns ns

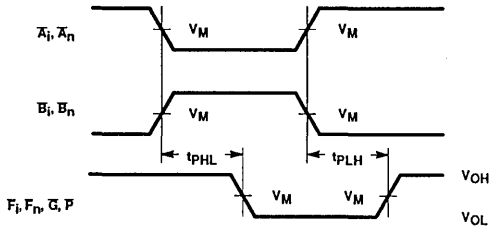
AC WAVEFORMS



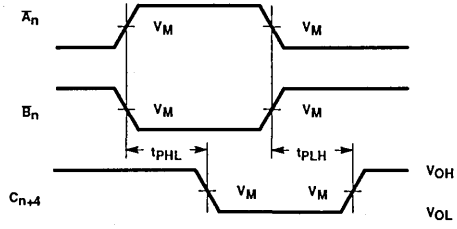
Waveform 1. Propagation Delay for Operands to Carry Output and Outputs



Waveform 2. Propagation Delays for Carry Input to Carry Output, Carry Input to Outputs, and Operands to Carry Generate Operands to Carry Generate and Carry Propagate Outputs



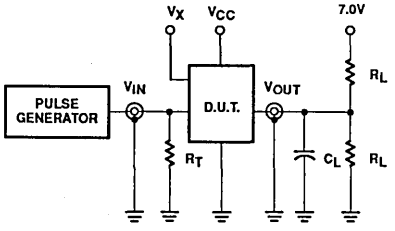
Waveform 3. Propagation Delay for Operands to Carry Generate and Propagate Outputs, Operands to A = B Output, and Outputs



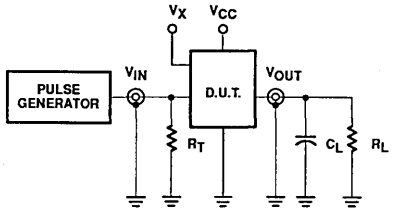
Waveform 4. Propagation Delays for Operands to Carry Output

NOTE: For all waveforms, V_M = 1.5V

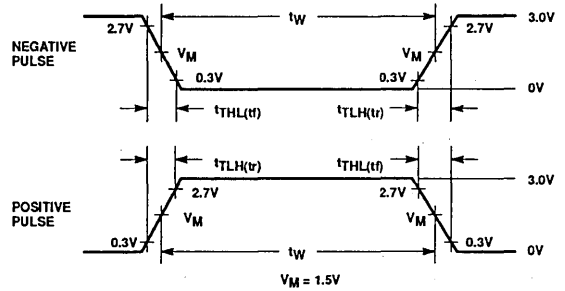
TEST CIRCUITS AND WAVEFORM



Test Circuit for Open-Collector Outputs



Test Circuit for Totem Pole Outputs



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

54F190, 54F191
Counters

54F190 Asynchronous Presettable BCD/Decade Up/Down Counter
54F191 Asynchronous Presettable 4-Bit Binary Up/Down Counter

Military FAST Products

Product Specification

FEATURES

- **Synchronous, reversible counting**
- **BCD/decade — 54F190**
  4-bit binary — 54F191
- **Asynchronous parallel load capability**
- **Count enable control for synchronous expansion**
- **Single up/down control input**

DESCRIPTION

The 54F190 is an asynchronous presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The 54F191 is similar, but is a 4-bit binary counter.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F190/BEA 54F191/BEA
Ceramic Flat Pack	54F190/BFA 54F191/BFA
Ceramic LLCC	54F190/B2A 54F191/B2A

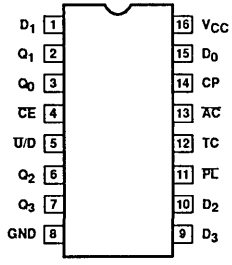
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CE}$	Count enable input (active low)	1.0/3.0	20μA/1.8mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
D_0 - D_3	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Asynchronous parallel load input (active low)	1.0/1.0	20μA/0.6mA
U/D	Up/down count control input	1.0/1.0	20μA/0.6mA
Q_0 - Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{RC}$	Ripple clock output (active low)	50/33	1.0mA/20mA
TC	Terminal count output (active high)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

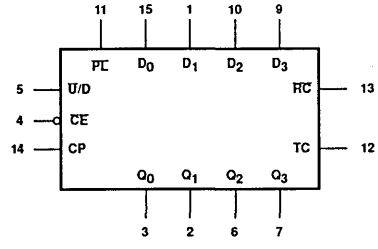
54F190



For LLCC Pin Assignments see JEDEC Standard No. 2

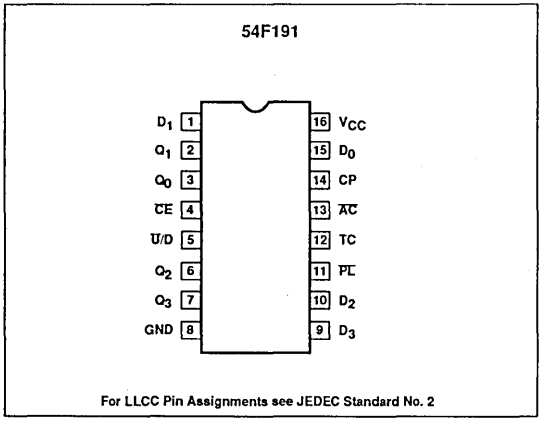
LOGIC SYMBOL

54F190

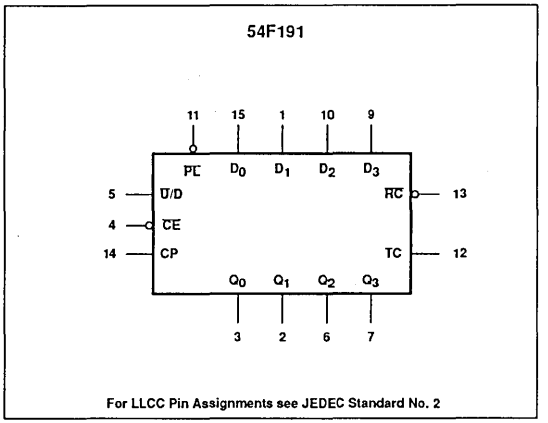


For LLCC Pin Assignments see JEDEC Standard No. 2

PIN CONFIGURATION



LOGIC SYMBOL



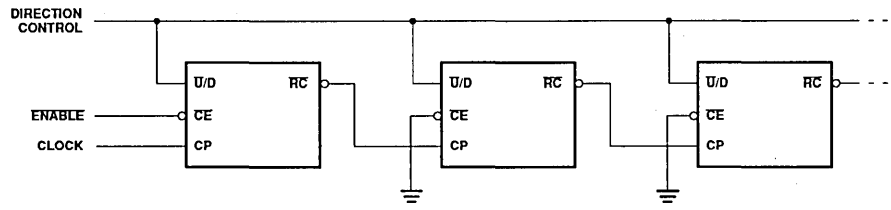
Counting is inhibited by a High level on the Count Enable ($\overline{CE}$) input. When $\overline{CE}$ is Low, internal state changes are initiated.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally Low and goes High when a circuit reaches zero in the count-down mode or reaches "9" in the count-up mode for 54F190 and reaches "15" in the count-up mode for 54F191. The TC output will remain High until a state change occurs, either by counting or presetting, or until U/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

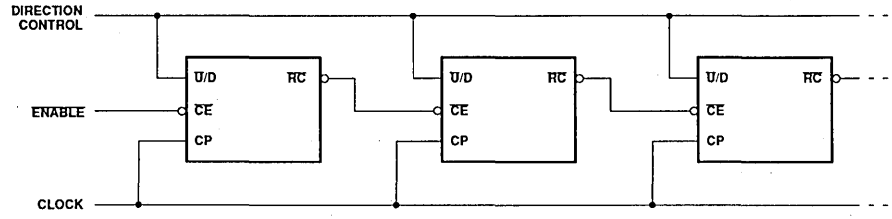
The TC signal is used internally to enable the $\overline{RC}$ output. When TC is High and $\overline{CE}$ is Low, the $\overline{RC}$ follows the Clock Pulse (CP) delayed by two gate delays. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multi-stage counters, as indicated in Figures 1a and 1b. In Figure 1a, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure 1b shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High. Since the $\overline{RC}$ output of any package goes High shortly after its CP input goes High, there is no such restriction on the High state duration of the clock.

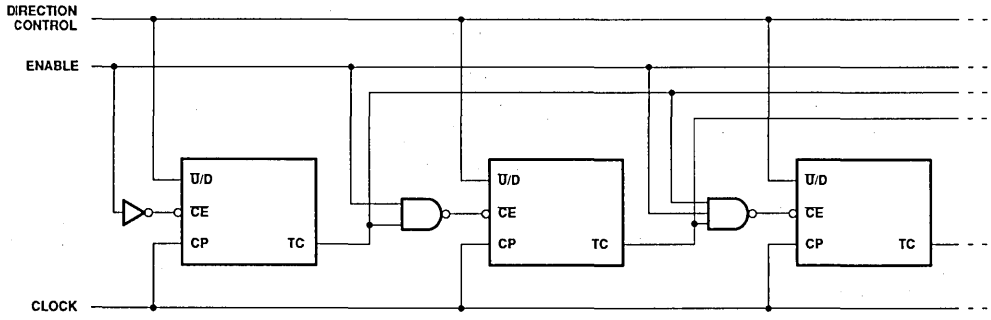
In Figure 1c, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure 1a and 1b does not apply.



a. N-Stage Counter Using Ripple Clock



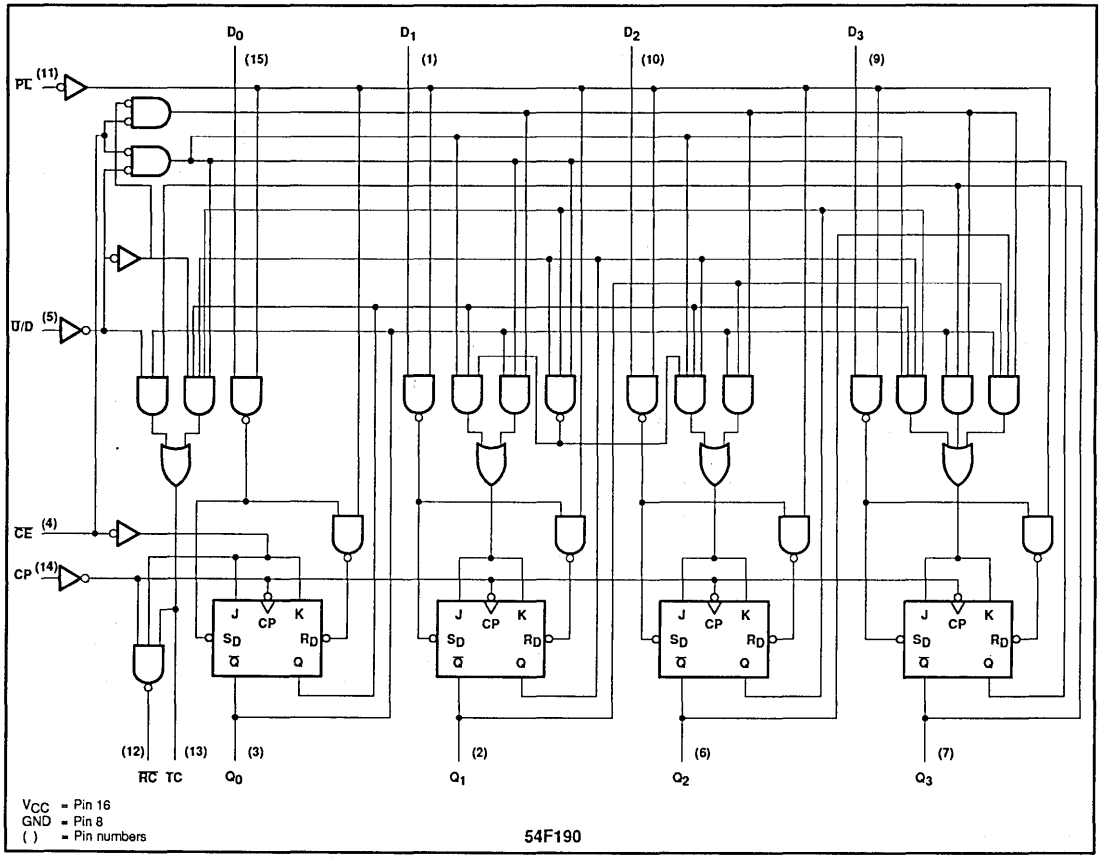
b. Synchronous N-Stage Counter Using Ripple Carry Borrow



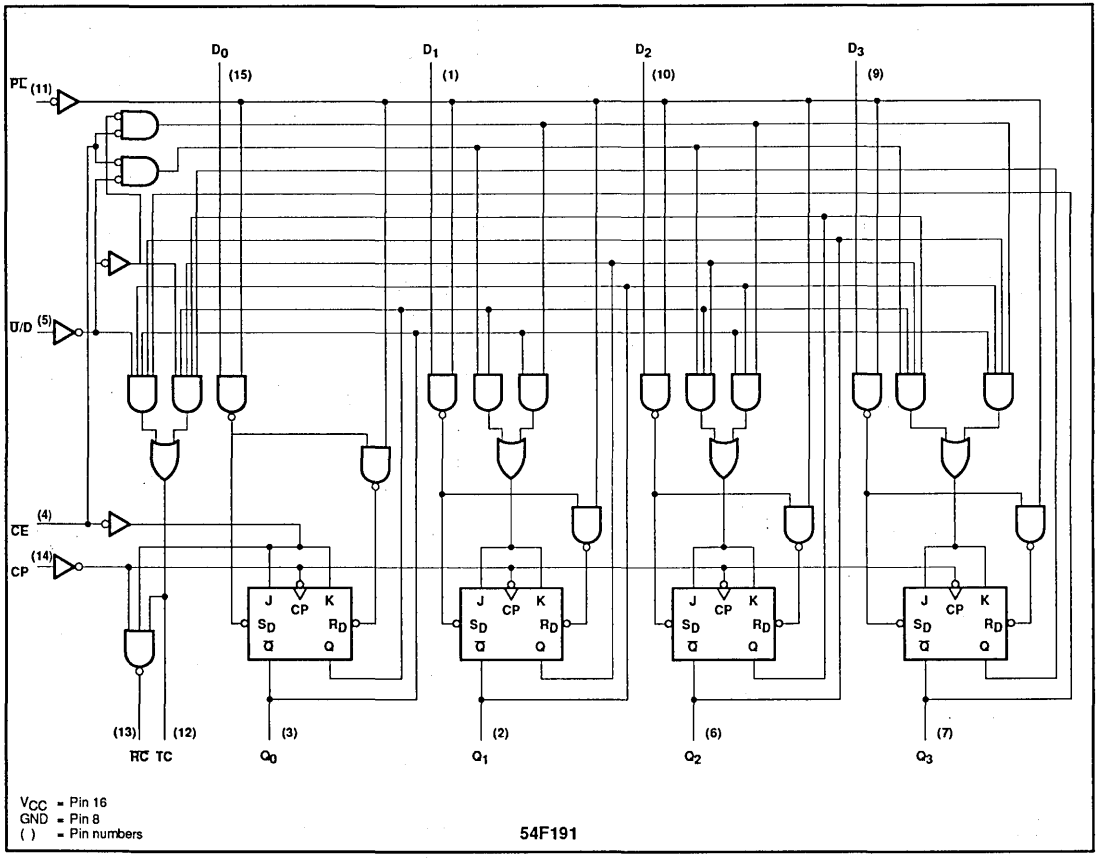
c. Synchronous N-Stage Counter with Parallel Gated Carry Borrow

Figure 1

LOGIC DIAGRAM



LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE, 54F190, 54F191

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	U/D	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L L	X X	X X	X X	L H	L H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE, 54F190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
U/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊔	H	X	X	H	↓	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	↓	⊔

TC AND $\overline{RC}$ FUNCTION TABLE, 54F191

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
U/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	↓	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	↓	⊔

H = High voltage level steady state
L = Low voltage level steady state
l = Low voltage level one set-up time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
⊔ = Low pulse
↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	$\overline{CE}$ input	V_{CC} = Max, V_I = 7.0V			0.3	mA
		Other inputs				0.1	mA
I_{IH1}	High-level input current	$\overline{CE}$ input	V_{CC} = Max, V_I = 2.7V			60	µA
		Other inputs				20	µA
I_{IL}	Low-level input current	$\overline{CE}$ input	V_{CC} = Max, V_I = 0.5V			-1.8	mA
		Other inputs				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = Max		38	55	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency (Q_n)	Waveform 1	100	125		80[5]		MHz
f_{MAX}	Maximum clock frequency ($\overline{RC}$)	Waveform 2	85	95		75[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	2.5 5.0	4.5 7.5	8.0 11.5	2.0 5.0	8.5 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	Waveform 1	6.5 6.0	9.0 8.0	12.5 11.0	6.0 6.0	13.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{RC}$	Waveform 2	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	8.0 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$	Waveform 2	2.0 3.0	4.0 5.0	7.0 7.5	2.0 3.0	7.5 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/D to $\overline{RC}$	Waveform 2	8.0 4.5	11.0 7.5	16.0 10.5	8.0 4.0	17.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/D to TC	Waveform 4	4.0 3.0	6.5 6.0	9.5 9.5	3.0 3.0	10.5 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 3	2.0 6.5	4.0 9.0	7.0 12.0	1.5 6.5	7.5 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n	Waveform 5	4.5 5.5	6.5 8.0	9.5 11.5	4.0 5.0	11.0 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{RC}$	Waveform 3 Waveform 4	6.0 6.0	14.0 11.0	18.0 13.5	6.0 6.0	21.0 15.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to TC	Waveform 3 Waveform 4	5.5 6.5	9.5 9.5	13.0 13.0	5.0 6.0	14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to TC	Waveform 5	5.5 6.0	8.5 10.5	12.0 13.5	5.5 6.0	14.5 15.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{RC}$	Waveform 5	8.5 7.5	16.0 10.0	18.5 13.0	8.5 7.0	22.0 14.5	ns ns

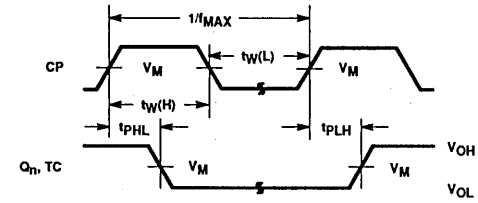
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 6.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 3.0		ns ns
$t_s(L)$	Setup time, High or Low $\overline{CE}$ to CP	Waveform 6	10.0			10.0		ns
$t_h(L)$	Hold time, High or Low $\overline{CE}$ to CP	Waveform 6	0			0.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{U}$/D to CP	Waveform 6	12.0 12.0			12.0 12.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{U}$/D to CP	Waveform 6	0 0			0 0		ns ns
$t_w(L)$	$\overline{PL}$ Pulse width	Waveform 5	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	CP Pulse width	Waveform 1	3.5 6.0			3.5 6.0		ns ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 5	6.0			8.0		ns

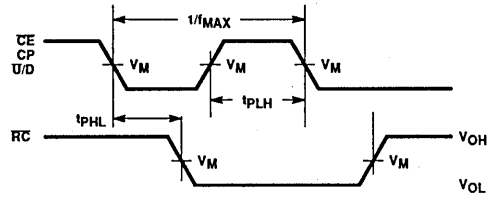
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.
5. These parameters are guaranteed, but not tested.

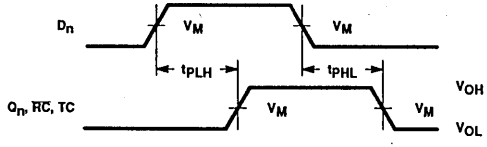
AC WAVEFORMS



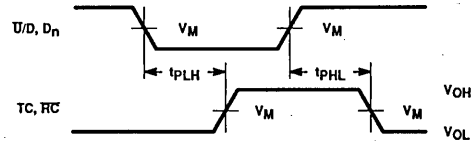
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Frequency.



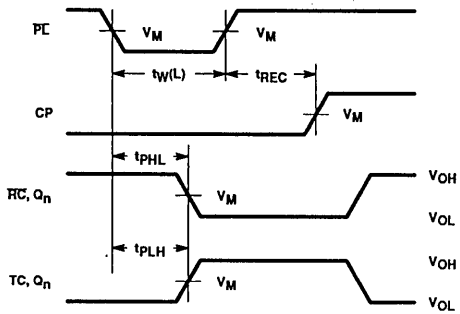
Waveform 2. Propagation Delay, Clock or Clock Enable to Ripple Clock Output and Maximum Clock Frequency



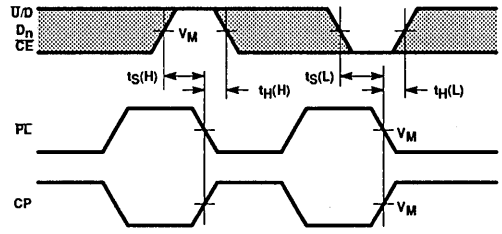
Waveform 3. Non-Inverting Propagation Delays



Waveform 4. Inverting Propagation Delay



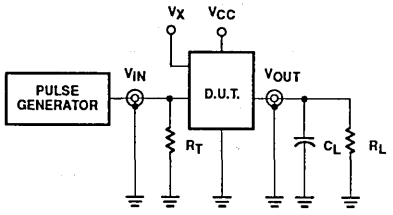
Waveform 5. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time



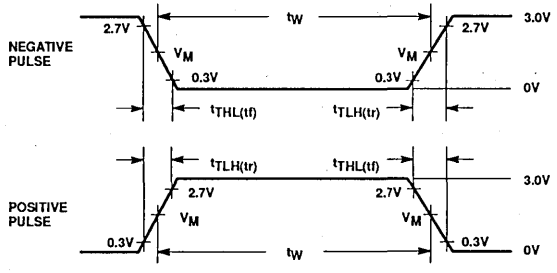
Waveform 6. Set-Up Time and Hold Time for D_n to $\overline{PL}$, $\overline{U}/D$ to CP and $\overline{CE}$ to CP

V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

Signetics

54F193
Counter

Synchronous Presettable 4-Bit Binary Down Counter

Product Specification

Military FAST Products

FEATURES

- **Synchronous reversible 4-bit binary counting**
- **Asynchronous parallel load**
- **Asynchronous reset (clear)**
- **Expandable without external logic**

DESCRIPTION

The 54F193 is a 4-bit synchronous up/down counter in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the Low-to-High transition of either Clock input. If the CP_U clock is pulsed while CP_D is held High, the device will count up ... if CP_D is pulsed while CP_U is held High, the device will count down. Only one Clock input can be held High at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin — it may also be loaded in parallel by activating the asynchronous parallel load pin.

ORDERING INFORMATION

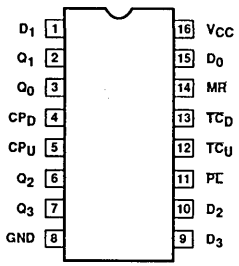
DESCRIPTION	ORDER CODE
Ceramic DIP	54F193/BEA
Ceramic Flat Pack	54F193/BFA
20-Pin Ceramic LLCC	54F193/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CP_U	Count up clock input (active rising edge)	1.0/2.0	20μA/1.2mA
CP_D	Count down clock input (active rising edge)	1.0/2.0	20μA/1.2mA
MR	Asynchronous master reset input (active High)	1.0/1.0	20μA/0.6mA
$\overline{PL}$	Asynchronous parallel load input (active Low)	1.0/1.0	20μA/0.6mA
D_0 - D_3	Parallel data inputs	1.0/1.0	20μA/0.6mA
Q_0 - Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}_D$	Terminal count down (borrow) output (active Low)	50/33	1.0mA/20mA
$\overline{TC}_U$	Terminal count up (carry) output (active Low)	50/33	1.0mA/20mA

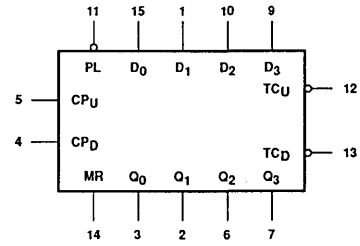
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

For LLCC pin assignments, see JEDEC Standard No. 2

Counter | 54F193

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

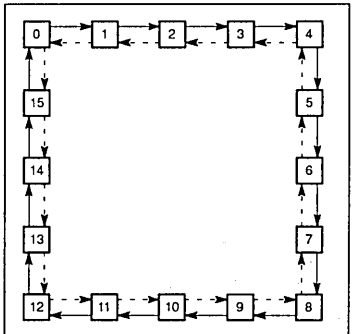
Each flip-flop contains JK feedback from slave to master, such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held High while counting with the other, because the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally High. When the circuit has reached the maximum count state of 15, the next High-to-Low transition of CP_U will cause $\overline{TC}_U$ to go Low. $\overline{TC}_U$ will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go Low when the circuit is in the zero state and the CP_D goes Low. The $\overline{TC}$ outputs can be used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load ($\overline{PL}$) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs Low. If one of the Clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of that clock will be interpreted as a legitimate signal and will be counted.

STATE DIAGRAM

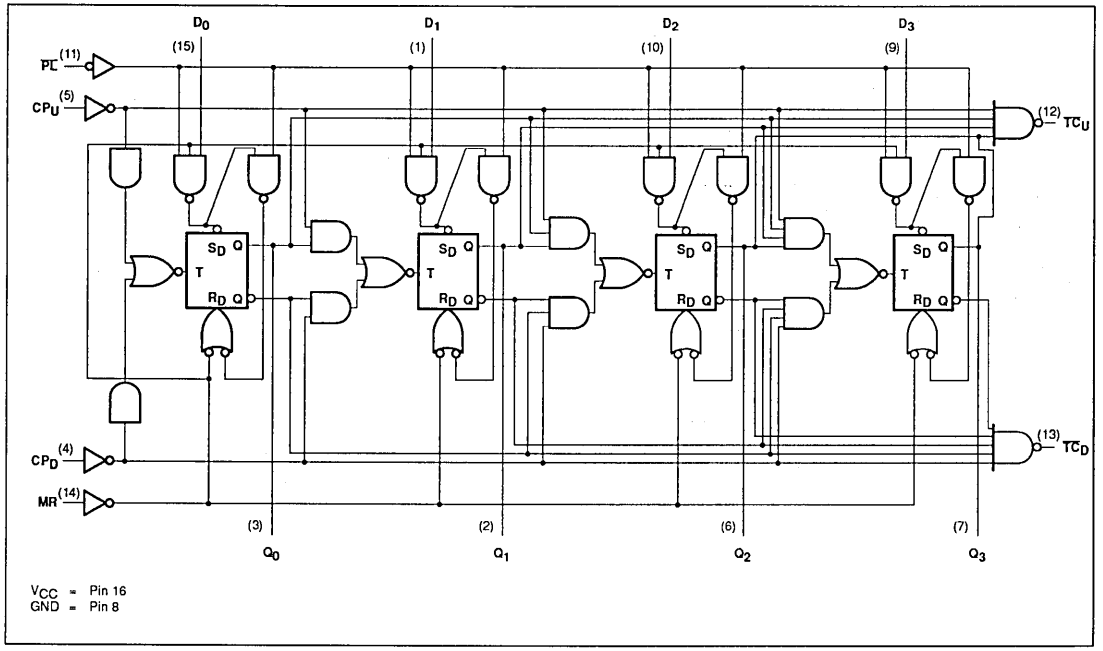


$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$

$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

Logic Equations for Terminal Count

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC_U}$	$\overline{TC_D}$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H[1]	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H[2]

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

NOTES:
1. TC_U = CP_U at terminal count up (HHHH).
2. TC_D = CP_D at terminal count down (LLLL).

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			.35	.5	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V	CP_U, CP_D			-1.8	mA
			Other inputs		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-60		-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			32	50	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 2	2.5 3.0	5.5 5.0	8.5 8.0	2.5 3.0	9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n	Waveform 1	2.5 5.0	5.5 8.5	8.5 12.0	3.0 6.0	9.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 4	2.0 6.0	4.0 9.5	7.0 13.5	1.5 6.0	7.5 15.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Q_n	Waveform 3	4.5 5.5	6.5 8.5	10.0 12.0	4.0 5.0	11.0 13.0	ns ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 5	5.0	7.5	11.0	5.5	12.5	ns
t_{PLH}	Propagation delay MR to $\overline{TC}_U$	Waveform 5	6.0	8.5	12.0	5.5	12.5	ns
t_{PHL}	Propagation delay MR to $\overline{TC}_D$	Waveform 5	5.0	7.5	11.0	5.0	11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 3	6.0 6.0	9.5 9.0	13.5 12.0	6.0 6.0	15.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 4	5.5 4.5	9.0 8.5	13.0 12.5	5.0 4.5	14.0 13.5	ns ns

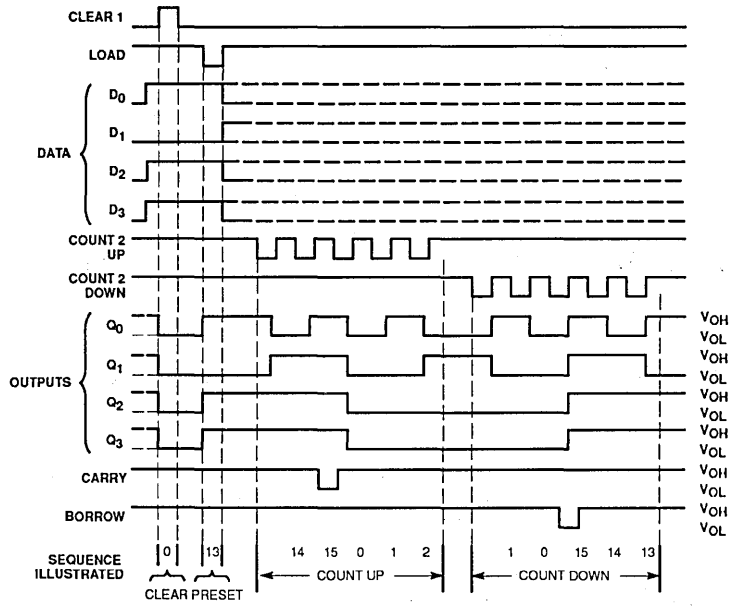
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns ns
$t_w(L)$	$\overline{PL}$ Pulse width Low	Waveform 1	6.0			6.0		ns
$t_w(H)$ $t_w(L)$	CP_U or CP_D Pulse width High or Low	Waveform 1	3.5 5.0			3.5 5.0		ns ns
$t_w(L)$	CP_U or CP_D Pulse width Low (Change of direction)	Waveform 1	10.0			10.0		ns
$t_w(H)$	MR Pulse width High	Waveform 5	6.0			6.0		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP_U or CP_D	Waveform 3	6.0			8.0		ns
t_{rec}	Recovery time MR to CP_U or CP_D	Waveform 5	4.0			4.0		ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CCH} with parallel load and Master Reset inputs grounded, all other inputs at 4.5V and all outputs open.

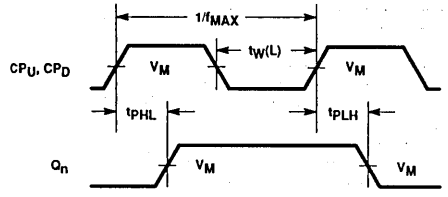
FUNCTIONAL WAVEFORM (Typical clear, load, and count sequences)



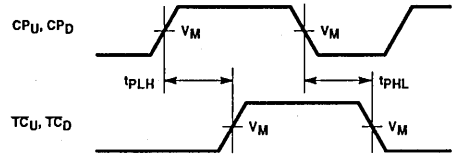
NOTES:
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be High; when counting down, count-up input must be High.

Binary Counter

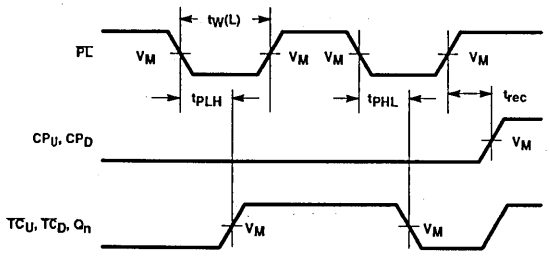
AC WAVEFORMS



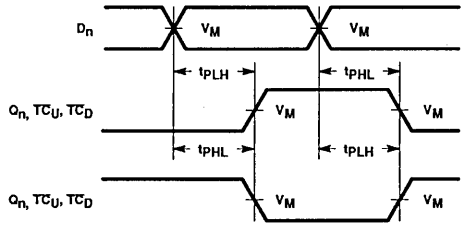
Waveform 1. Propagation Delay, Clock Input to Output, Clock Width and Maximum Clock



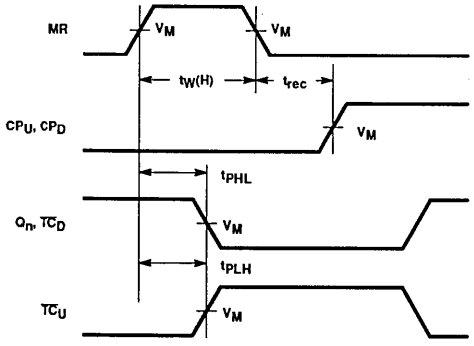
Waveform 2. Propagation Delay, Clock Pulse to Terminal Count



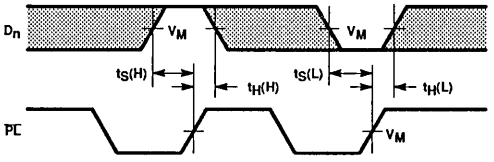
Waveform 3. Parallel Load Pulse Width, Parallel Load to Output Delays, and Parallel Load to Clock Recovery Time



Waveform 4. Propagation Delay, Data to Flip-Flop Outputs, Terminal Count Up and Down Outputs



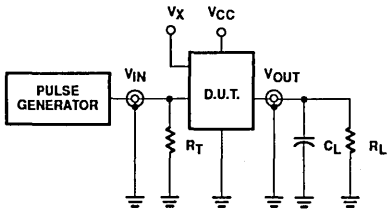
Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery



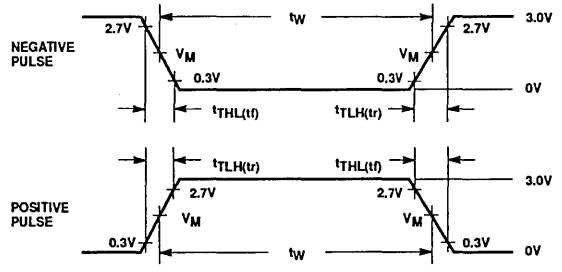
Waveform 6. Setup Time and Hold Time for D_n to $\overline{PL}$

$V_M = 1.5V$

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

54F194
Shift Register

4-Bit Bidirectional Universal Shift Register

Product Specification

Military FAST Products

FEATURES

- **Shift left and shift right capability**
- **Synchronous parallel and serial data transfers**
- **Easily expanded for both serial and parallel operation**
- **Asynchronous Master Reset**
- **Hold (do nothing) mode**

DESCRIPTION

The functional characteristics of the 54F194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 9ns (typical), making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

ORDERING INFORMATION

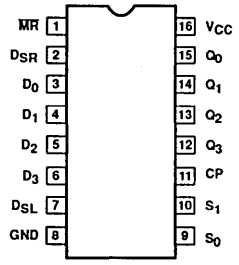
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F194/BEA
16-Pin Ceramic FlatPack	54F194/BFA
20-Pin Ceramic LLCC	54F194/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode control inputs	1.0/1.0	20μA/0.6mA
D_{SR}	Serial data input (shift right)	1.0/1.0	20μA/0.6mA
D_{SL}	Serial data input (shift left)	1.0/1.0	20μA/0.6mA
C_P	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Asynchronous master reset (active Low)	1.0/1.0	20μA/0.6mA
Q_0 - Q_3	Parallel outputs	50/33	1.0mA/20mA

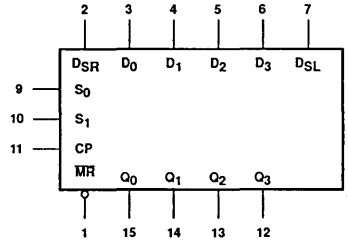
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

Shift Register 54F194

The 54F194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right $Q_0 \rightarrow Q_1$, etc.), or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode Select and Data inputs on the 54F194 are edge-triggered, responding only to the Low-to-High transition of the Clock (CP). therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. Signals on the Select, Parallel Data (D_0 - D_3) and Serial Data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only the recommended setup and hold times, with respect to the clock rising edge, are observed.

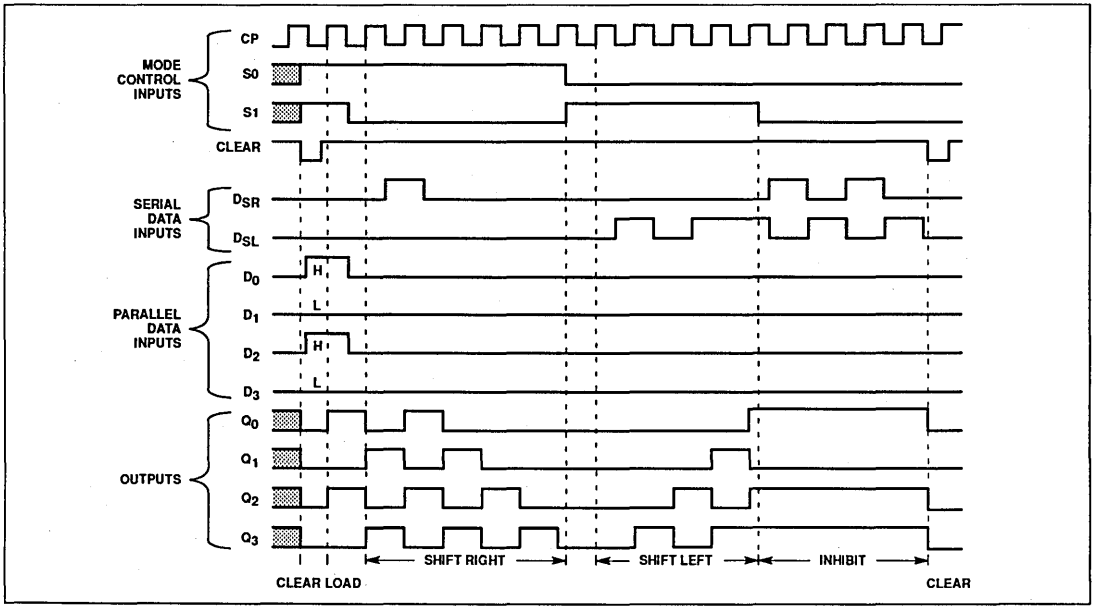
The four Parallel Data inputs (D_0 - D_3) are D-type inputs. Data appearing on D_0 - D_3 inputs when S_0 and S_1 are High is transferred to the Q_0 - Q_3 outputs respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

MODE SELECT — FUNCTION TABLE

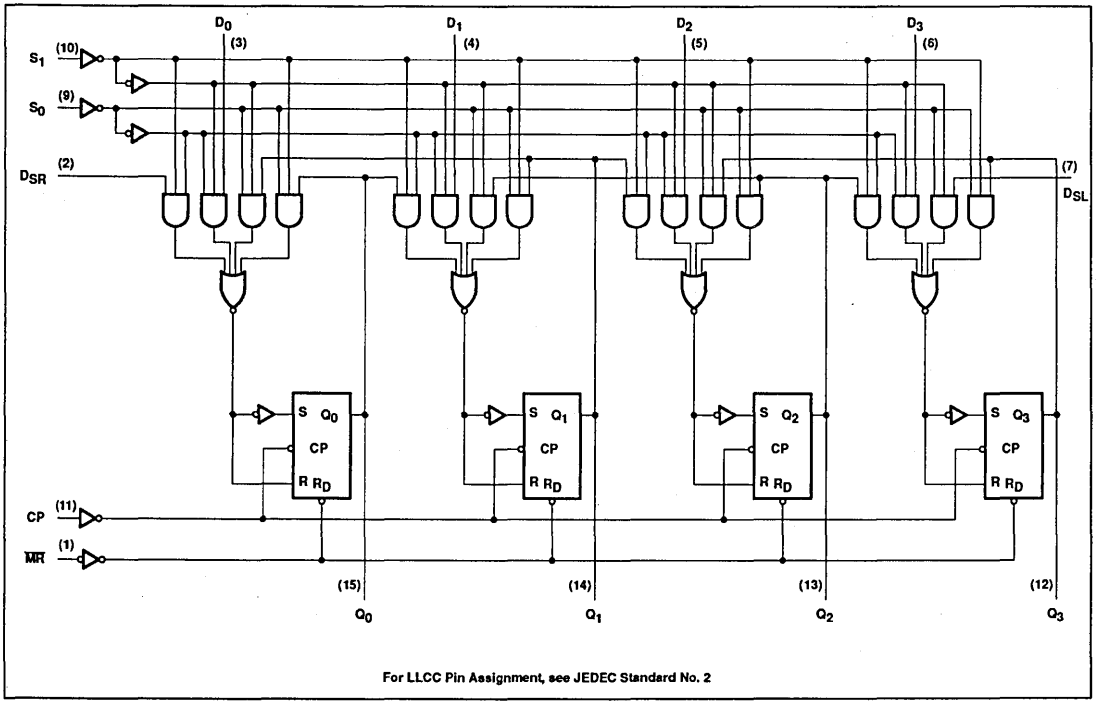
OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift left	↑	H	h	l	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift right	↑	H	l	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
d_n(q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



LOGIC DIAGRAM



For LLCC Pin Assignment, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage[3]	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = +7.0V		5	100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[4]	V_{CC} = Max, V_O = 0.0V	-60	-90	-150	mA
I_{CC}	Supply current[5] (total)	V_{CC} = Max		33	46	mA

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	150		90[6]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Qn	Waveform 1	3.5 3.5	5.2 5.5	7.0 7.0	3.0 3.0	8.5 8.5	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.5	8.6	12	4.5	14.5	ns

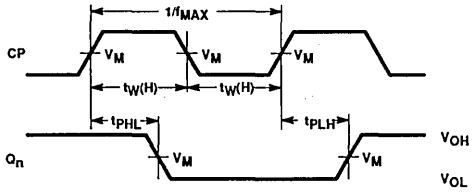
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, D_0 - D_3 to CP D_{SR}, D_{SL} to CP	Waveform 3	4.0 4.0			4.0 4.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_0 - D_3 to CP, D_{SR}, D_{SL} to CP		0 0			1.0 1.0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 4	8.0 8.0			9.5 8.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP		0 0			0 0		ns ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	7.0			9.0		ns
$t_w(H)$	CP pulse width, High	Waveform 1	5.0			5.5		ns
$t_w(L)$	$\overline{MR}$ pulse width, Low	Waveform 2	5.0			5.0		ns

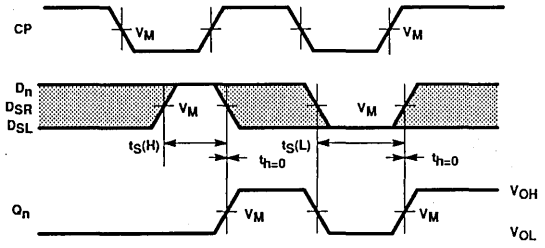
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Output High state will change to Low state if an external voltage of less than 0.0V is applied.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. With all outputs open, D inputs grounded and ≥4.0V applied to S_0, S_1 MR and the serial inputs, I_{CC} is tested with a momentary ground, then ≥4.0V applied to CP.
6. These parameters are guaranteed, but not tested.

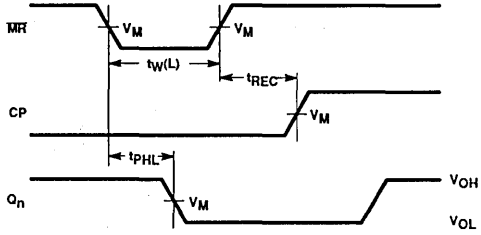
AC WAVEFORMS



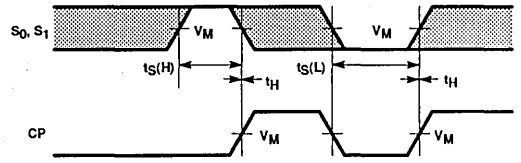
Waveform 1. Clock to Output Delays and Clock Pulse Width



Waveform 2. Data Setup and Hold Times



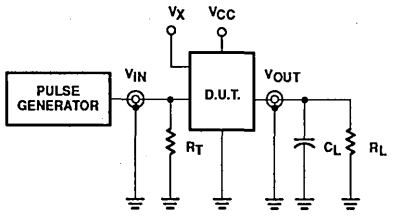
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



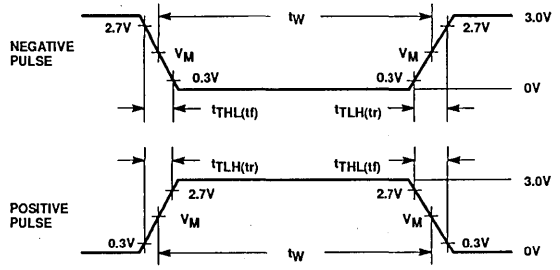
Waveform 4. Setup and Hold Times for S_0 and S_1 Inputs

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

54F198
Shift Register

8-Bit Bidirectional Universal Shift Register

Product Specification

Military FAST Products

FEATURES

- **Buffered clock and control inputs**
- **Shift right, shift left, and parallel load capability**
- **Asynchronous Master Reset**

DESCRIPTION

The 54F198, Bidirectional Universal Shift Register is designed to incorporate virtually all of the features a system designer may want in a shift register. This circuit features parallel inputs and outputs, shift right and shift left serial inputs, operating mode select inputs, and a direct overriding master reset input. The register has four distinct modes of operation:

Parallel (broadside) load
Shift right (in the direction Q_0 toward Q_7)
Shift left (in the direction Q_7 toward Q_0)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the 8 bits of data and taking both mode control inputs, S_0 and S_1, High. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

ORDERING INFORMATION

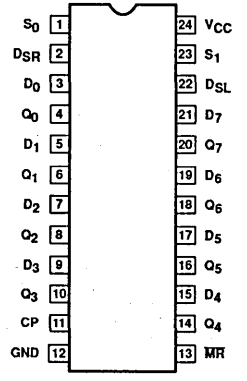
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54F198/BLA
24-Pin Ceramic FlatPack	54F198/BKA
28-Pin Ceramic LLCC	54F198/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Parallel data inputs	1.0/1.0	20μA/0.6mA
D_{SR}	Serial data input (Shift Right)	1.0/1.0	20μA/0.6mA
D_{SL}	Serial data input (Shift Left)	1.0/1.0	20μA/0.6mA
S_0, S_1	Mode Select inputs	1.0/1.0	20μA/0.6mA
C_P	Clock pulse input (Active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master reset input (Active Low)	1.0/1.0	20μA/0.6mA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

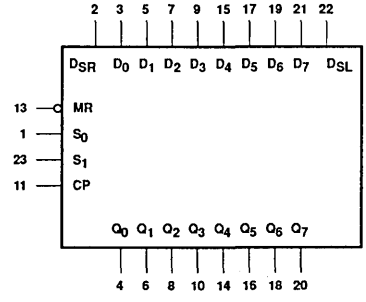
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



VCC = Pin 24
GND = Pin 12

For LLCC pin assignments, see JEDEC Standard No. 2

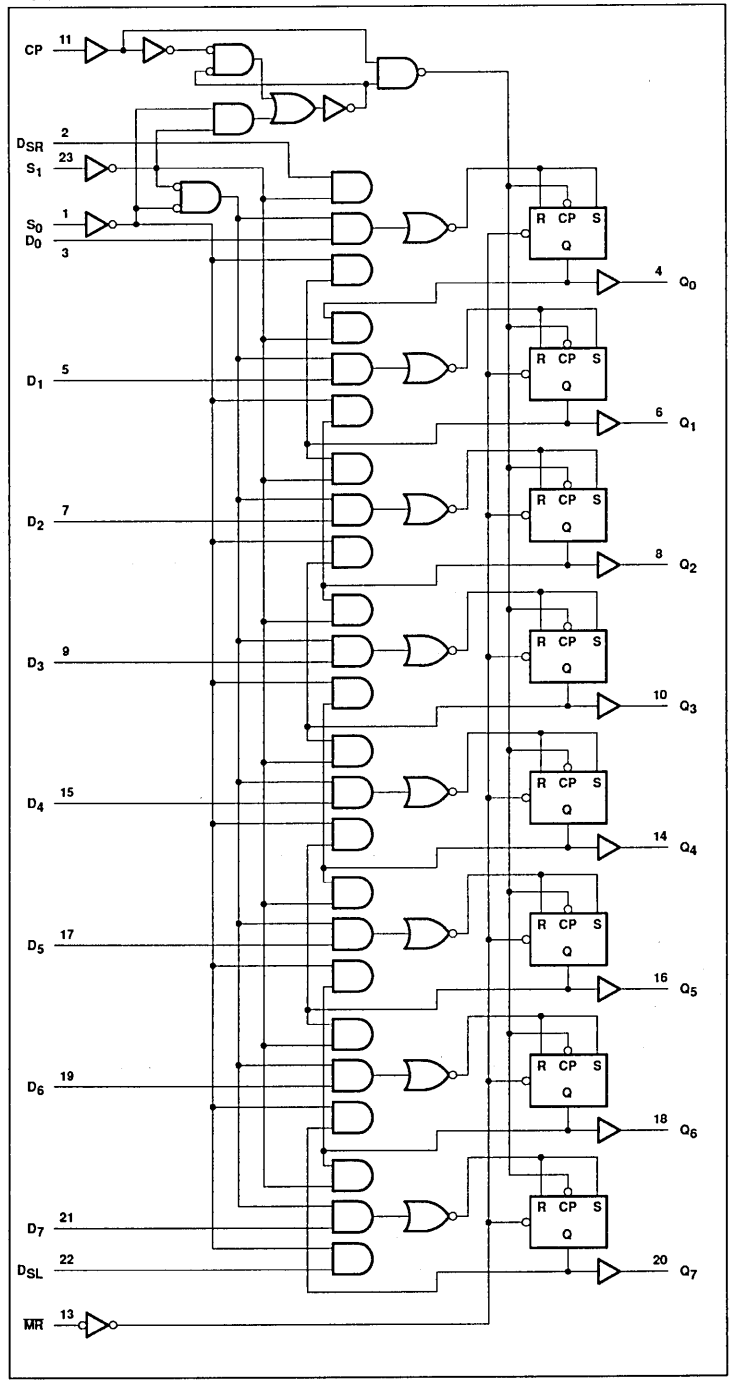
Shift Register

54F198

Shift right is accomplished synchronously, with the rising edge of the clock pulse when S_0 is High and S_1 is Low. Serial data for this mode is entered at the right data input (D_{SR}). When S_0 is Low and S_1 is High, data shifts left synchronously and new data is entered at the shift-left serial input (D_{SL}).

Clocking of the flip-flops is inhibited when both mode control inputs are Low.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS							OUTPUTS				
$\overline{MR}$	Mode		CP	Serial		Parallel					
	S_0	S_1		Left	Right	0...7	Q_0	Q_1	...	Q_6	Q_7
L	X	X	X	X	X	X	L	L		L	L
H	X	X	L	X	X	X	Q_{00}	Q_{10}		Q_{60}	Q_{70}
H	H	H	↑	X	X	0 ... 7	0	1		6	7
H	H	L	↑	X	H	X	H	Q_{0n}		Q_{5n}	Q_{6n}
H	H	L	↑	X	L	X	L	Q_{0n}		Q_{5n}	Q_{6n}
H	L	H	↑	H	X	X	Q_{1n}	Q_{2n}		Q_{7n}	H
H	L	H	↑	L	X	X	Q_{1n}	Q_{2n}		Q_{7n}	L
H	L	L	X	X	X	X	Q_{00}	Q_{10}		Q_{60}	Q_{70}

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High transition of designated input
0...7 = The level of steady input at inputs 0 through 7, respectively
Q_{00}, Q_{10}, Q_{60}, Q_{70} = The level of Q_0, Q_1, Q_6, Q_7, respectively, before the indicated steady state input conditions were established.
Q_{0n}, Q_{1n}, Q_{6n}, Q_{7n} = The level of Q_0, Q_1, Q_6, Q_7, respectively, before the most recent Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max		70	100	mA
		I_{CCL}			75	110	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80	95		70[4]		MHz
t_{PLH} t_{PHL}	Propagation delay CP input to Q_n	Waveform 1	5.0 6.0	7.5 8.5	10.0 11.0	4.5 5.5	12.0 13.0	ns ns
t_{PHL}	Propagation delay	Waveform 3	5.0	7.5	10.0	4.5	13.0	ns

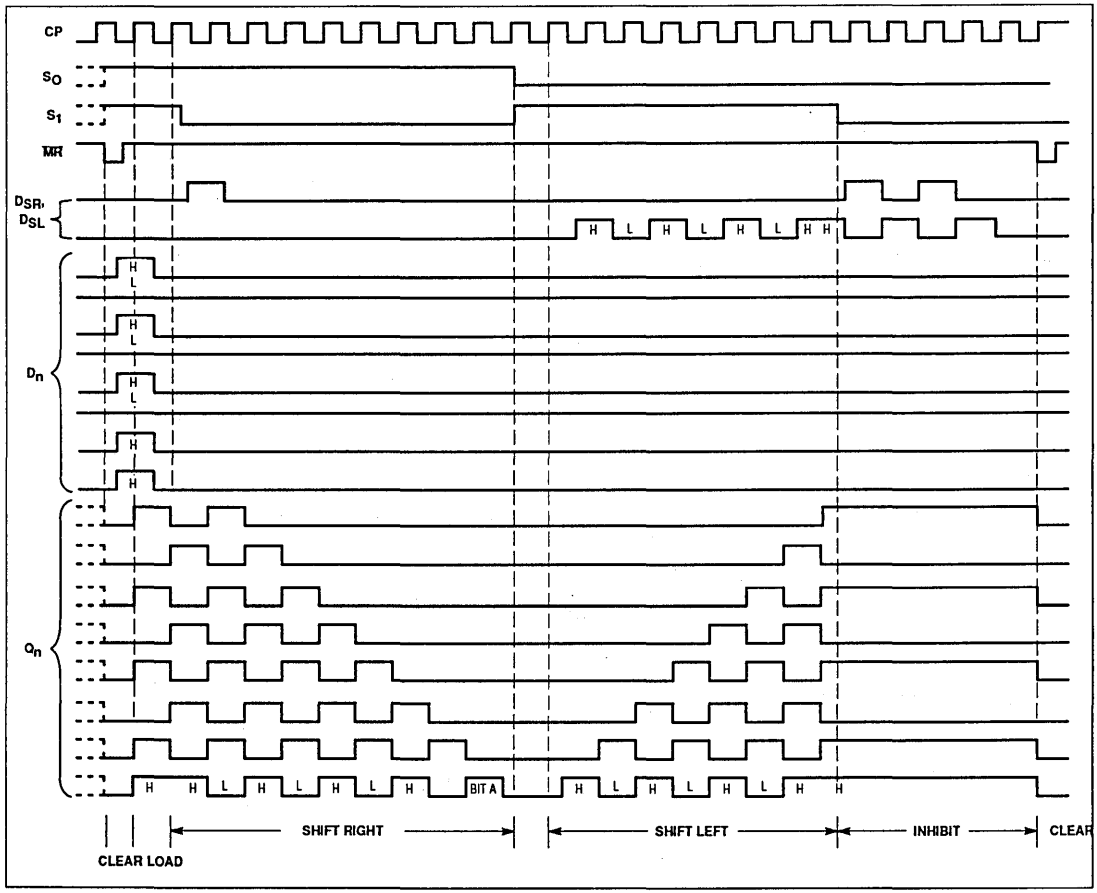
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	0.0 3.0			1.0 3.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	0.0 3.5			2.5 5.0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 3.0			1.5 3.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_{SR}, D_{SL} to CP	Waveform 2	0.0 2.5			1.5 3.5		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 2	9.0 6.0			11.0 7.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 2	0.0 0.0			0.0 0.0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width High or Low	Waveform 1	5.0 5.0			6.0 6.0		ns ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 3	5.0			6.0		ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 3	5.0			6.5		ns

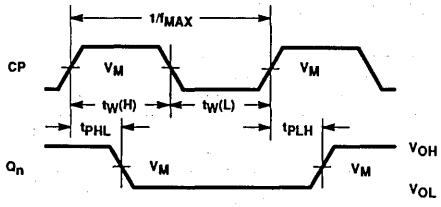
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. These parameters are guaranteed, but not tested.

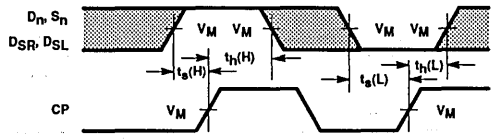
TYPICAL TIMING DIAGRAM



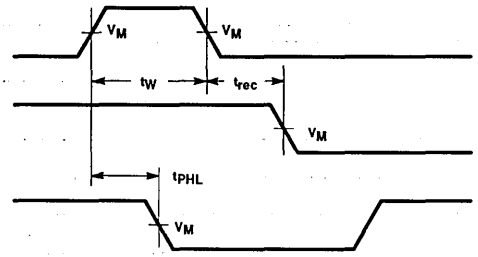
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths, and Maximum Clock Frequency



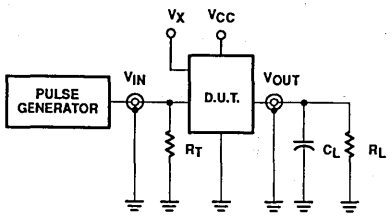
Waveform 2. Setup and Hold Times



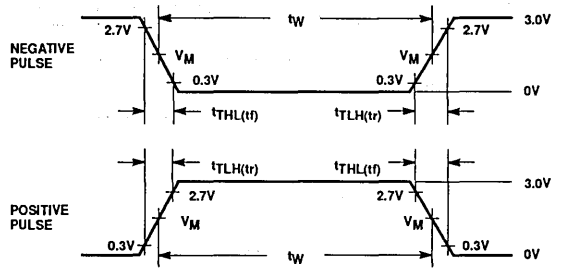
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F240/54F241
Buffers

54F240 Octal Inverting Buffer, 3-State
54F241 Octal Buffer, 3-State

Product Specification

DESCRIPTION

The 54F240 and 54F241 are octal buffers that are ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 48mA and sourcing up to 12mA, producing very good capacitive drive characteristics. The device features two output enables, ($\overline{OE}$), each controlling four of the 3-state outputs.

FEATURES

- **3-state buffer outputs sink 48mA and source 12mA**
- **Octal bus interface**

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F240/BRA, 54F241/BRA
Ceramic Flat Pack	54F240/BSA, 54F241/BSA
Ceramic LLCC	54F240/B2A, 54F241/B2A

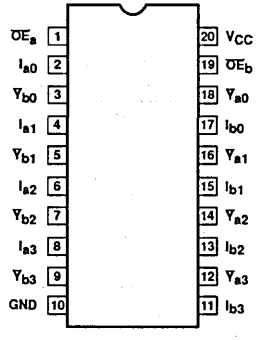
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{aN} - I_{bN}	Data inputs (54F240)	1.0/1.67	20μA/1.0mA
I_{aN} - I_{bN}	Data inputs (54F241)	1.0/2.67	20μA/1.6mA
$\overline{OE}_a$, $\overline{OE}_b$	Output Enable inputs (Active High)	1.0/1.67	20μA/1.0mA
OE_b	3-State Output Enable input (Active Low)	1.0/1.67	20μA/1.0mA
$\overline{Y}_{an}$, $\overline{Y}_{bn}$	Data outputs (54F240)	600/80	12mA/48mA
Y_{an}, Y_{bn}	Data outputs (54F241)	600/80	12mA/48mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

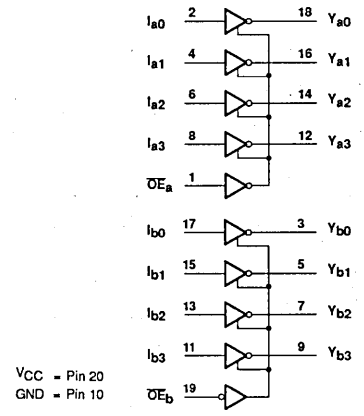
54F240



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

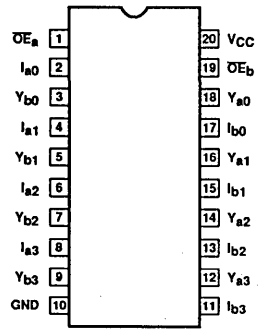
54F240



For LLCC pin assignments, see JEDEC Standard No. 2

PIN CONFIGURATION

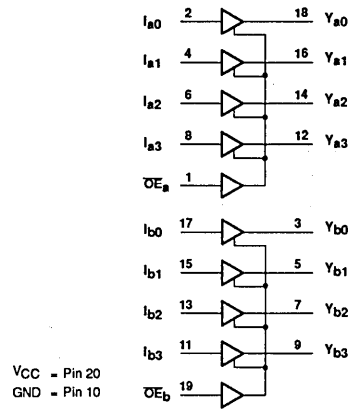
54F241



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

54F241



For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE, 54F240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "OFF" state

FUNCTION TABLE, 54F241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "OFF" state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-1	mA
I_{OH2}	High-level output current			-3	mA
I_{OH3}	High-level output current			-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

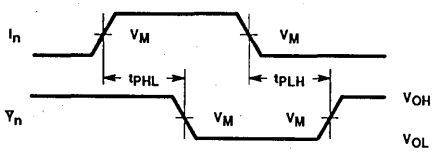
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min,	I_{OH1} = -1mA	2.5			V
			V_{IL} = Max,	I_{OH2} = -3mA	2.4			V
			V_{IH} = Min	I_{OH3} = -12mA	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				0.1	mA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current	'F240 All inputs 'F241 $\overline{OE}_a$, $\overline{OE}_b$	V_{CC} = Max, V_I = 0.5V			-0.6	-1.0	mA
		'F241 I_{an}, I_{bn}				-0.6	-1.6	mA
I_{OZH}	Off-state output current		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-100	-150	-225	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = Max 54F240			12	29	mA
		I_{CCL}				50	75	mA
		I_{CCZ}				35	63	mA
		I_{CCH}	V_{CC} = Max 54F241			40	60	mA
		I_{CCL}				60	90	mA
		I_{CCZ}				60	90	mA

AC ELECTRICAL CHARACTERISTICS

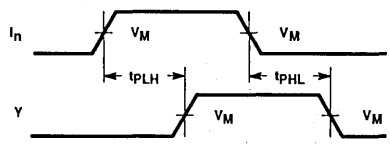
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output (54F240)	Waveform 1	3.0 2.0	4.5 3.0	6.5 4.5	3.0 1.5	9.0 5.5	ns ns
t_{PZH} t_{PZL}	Output Enable time (54F240)	Waveform 3 Waveform 4	3.0 4.5	5.0 6.5	7.5 8.5	2.0 4.0	9.5 10.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time (54F240)	Waveform 3 Waveform 4	3.0 3.0	5.5 5.0	7.0 7.0	2.5 2.5	8.0 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output (54F241)	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.5 2.5	6.5 7.0	ns ns
t_{PZH} t_{PZL}	Output Enable time (54F241)	Waveform 3 Waveform 4	2.0 2.0	4.0 5.0	5.7 7.0	2.0 2.0	7.0 8.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time (54F241)	Waveform 3 Waveform 4	2.0 2.0	4.0 4.0	6.0 6.0	2.0 2.0	7.0 7.5	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and the functional table for the applicable operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time.
4. I_{CC} is measured with outputs open.

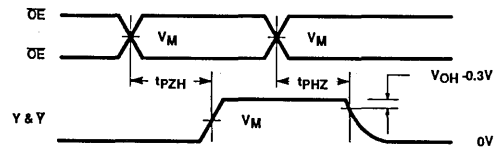
AC WAVEFORMS



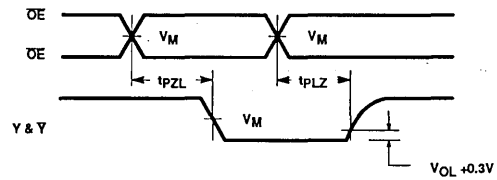
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



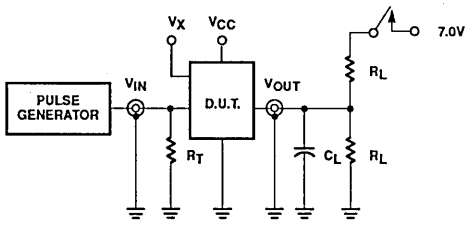
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



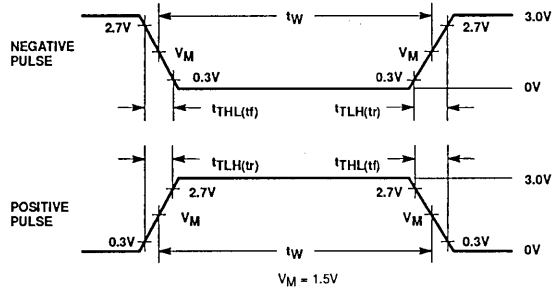
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

Military Logic Products

54F244
Buffer

Octal Buffer (3-State)

Product Specification

FEATURES

- **Octal bus interface**
- **3-State buffer outputs sink 48mA**
- **12mA source current**

DESCRIPTION

The 54F244 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 48mA and sourcing up to 12mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}$, each controlling four of the 3-State outputs.

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z)= High impedance (off) state

ORDERING INFORMATION

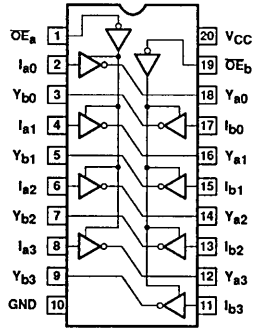
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F244/BRA
20-Pin Ceramic FlatPack	54F244/BSA
20-Pin Ceramic LLCC	54F244/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_a$	3-State output enable input (active Low)	1.0/1.67	20μA/1.0mA
$\overline{OE}_b$	3-State output enable input (active Low)	1.0/1.67	20μA/1.0mA
I_{a0} - I_{a3}, I_{b0} - I_{b3}	Data inputs	1.0/2.67	20μA/1.6mA
Y_{a0} - Y_{a3}, Y_{b0} - Y_{b3}	Data outputs	600/80	12mA/48mA

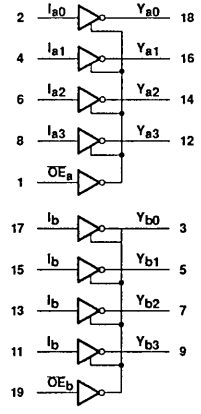
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-1	mA
I_{OH2}	High-level output current			-3	mA
I_{OH3}	High-level output current			-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH1} = -1mA	2.5			V
				I_{OH2} = -3mA	2.4			V
				I_{OH3} = -12mA	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, $I_I = I_{IK}$			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current	$\overline{OE}_a$, $\overline{OE}_b$	V_{CC} = Max, V_I = 0.5V			-0.7	-1.0	mA
		$I_a0 - I_a3$, $I_b0 - I_b3$				-0.6	-1.6	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-100	-150	-225	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = Max			40	60	mA
		I_{CCL}				60	90	mA
		I_{CCZ}				60	90	mA

AC ELECTRICAL CHARACTERISTICS

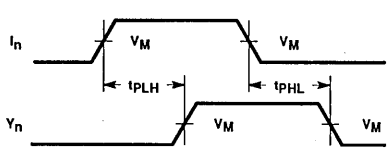
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic."

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1	2.5	4.0	5.2	2.5	6.5	ns
t_{PHL}	Propagation delay	Waveform 1	2.5	4.0	5.2	2.5	7.0	ns
t_{PZH}	Enable to High	Waveform 2	2.0	4.3	6.0	2.0	7.5	ns
t_{PZL}	Enable to Low	Waveform 3	2.0	5.0	7.0	2.0	8.5	ns
t_{PHZ}	Disable from High	Waveform 2	2.0	3.5	6.0	2.0	7.0	ns
t_{PLZ}	Disable from Low	Waveform 3	2.0	4.0	6.0	2.0	7.5	ns

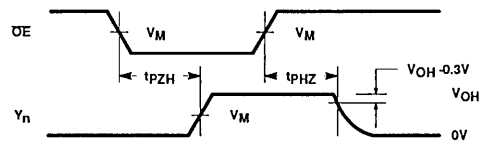
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and functional table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs open.

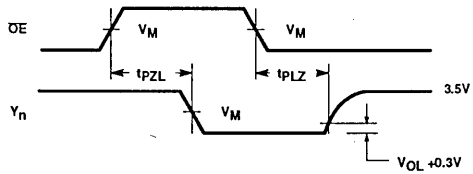
AC WAVEFORMS



Waveform 1. For Non-Inverting Outputs



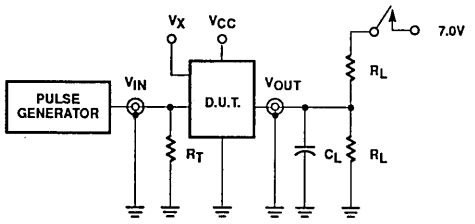
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



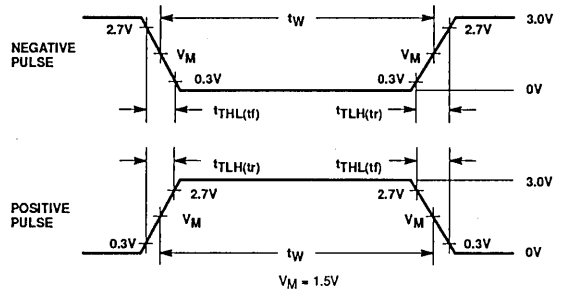
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed
	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

Military Logic Products

54F245
Transceiver

Octal Transceiver (3-State)

Product Specification

FEATURES

- **Octal bidirectional bus interface**
- **3-State buffer outputs sink 48mA**
- **12mA source current**
- **Outputs are placed in Hi-Z state during power-off conditions**

DESCRIPTION

The 54F245 is an octal transceiver featuring noninverting 3-State bus compatible outputs in both send and receive directions. The B side outputs are all capable of sinking 48mA and sourcing up to 12mA, producing very good capacitive drive characteristics. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Send/Receive (T/$\overline{R}$) input for directional control. The 3-State outputs, B_0 - B_7, have been designed to prevent output bus loading if the power is removed from the device.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F245/BRA
20-Pin Ceramic FlatPack	54F245/BSA
20-Pin Ceramic LLCC	54F245/B2A

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	T/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUT	B = A
H	X	(Z)	(Z)

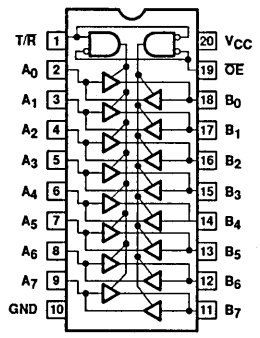
H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance "off" state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}$	Output enable input (active Low)	2.0/2.0	40µA/1.2mA
T/$\overline{R}$	Send receive input	2.0/2.0	40µA/1.2mA
A_0 - A_7	3-State A data inputs	3.5/1.67	70µA/1.0mA
B_0 - B_7	3-State B data inputs	3.5/1.67	70µA/1.0mA
A_0 - A_7	3-State A data outputs	150/33	3.0mA/20mA
B_0 - B_7	3-State B data outputs	600/80	12mA/48mA

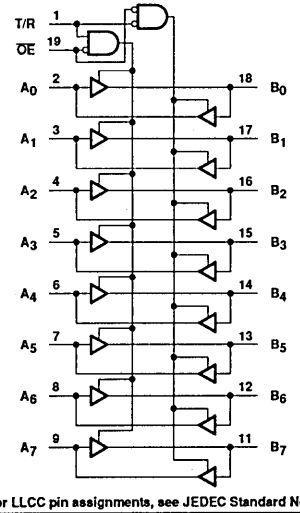
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_I	Input voltage range		-0.5 to +7.0	V
I_I	Input current range		-30 to +5	mA
V_O	Voltage applied to output in High output state range		-0.5 to +5.5	V
I_O	Current applied to output in Low output state	$A_0 - A_7$	40	mA
		$B_0 - B_7$	96	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH1}	High-level output current	$A_0 - A_7, B_0 - B_7$			-1	mA
I_{OH2}	High-level output current	$A_0 - A_7, B_0 - B_7$			-3	mA
I_{OH3}	High-level output current	$B_0 - B_7$			-12	mA
I_{OL}	Low-level output current	$A_0 - A_7$			20	mA
		$B_0 - B_7$			48	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

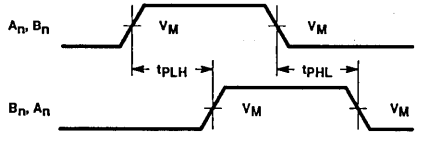
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_0 - A_7, B_0 - B_7	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH2} = -3mA	2.4	3.4		V
				I_{OH1} = -1mA	2.5			V
		B_0 - B_7		I_{OH3} = -12mA	2.0	3.4		V
V_{OL}	Low-level output voltage	A_0 - A_7	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = 20mA			0.35	0.50	V
		B_0 - B_7	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = 48mA			0.35	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH1}	Input current at maximum input voltage	$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0V, V_I = 7.0V				100	µA
			V_{CC} = 0V, V_I = 2.7V				20	µA
		A_0 - A_7, B_0 - B_7	V_{CC} = 5.5V, V_I = 5.5V, $\overline{OE}$ = ≤0.8V				1.0	mA
I_{IH2}	High-level input current $\overline{OE}$ and T/$\overline{R}$ only	$\overline{OE}$	V_{CC} = Max, V_I = 2.7V	T/$\overline{R}$ ≤0.8V			40	µA
		T/$\overline{R}$		$\overline{OE}$ ≤0.8V			40	µA
I_{IL1}	Low-level input current	A_0 - A_7,	V_{CC} = 5.5V, T/$\overline{R}$ = 5.5V, $\overline{OE}$ = GND				-600	µA
		B_0 - B_7	V_{CC} = 5.5V, T/$\overline{R}$ = GND, $\overline{OE}$ = GND				-600	µA
I_{IL2}	Low-level input current $\overline{OE}$ and T/$\overline{R}$ only	$\overline{OE}$	V_{CC} = Max, V_I = 0.5V	T/$\overline{R}$ ≤0.8V		-0.75	-1.2	mA
		T/$\overline{R}$		$\overline{OE}$ ≤0.8V		-0.75	-1.2	mA
I_{OZH} + I_{IH}	Off-state output current High-level voltage applied		V_{CC} = Max, $\overline{OE}$ = 2.0V, V_I = 2.7V			0	70	µA
I_{OZL} + I_{IL}	Off-state output current Low-level voltage applied		V_{CC} = Max, $\overline{OE}$ = 2.0V, V_I = 0.5V				-600	µA
I_{OS}	Short-circuit output current[3]	A_0 - A_7	V_{CC} = Max		-60		-150	mA
		B_0 - B_7			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	V_{IH} ≥4.0V		85	114	mA
		I_{CCL}		V_{IH} = GND		100	125	mA
		I_{CCZ}		V_{IH} ≥4.0V		110	140	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

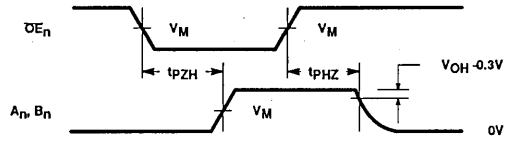
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 1	2.5 2.5	3.5 4.0	5.5 6.0	2.0 2.0	7.5 7.5	ns ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 2 Waveform 3	2.0 3.5	7.0 6.5	7.5 7.5	2.0 3.5	11.0 10.0	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 2 Waveform 3	3.0 2.0	4.5 4.0	6.5 6.0	3.0 2.0	8.0 8.5	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

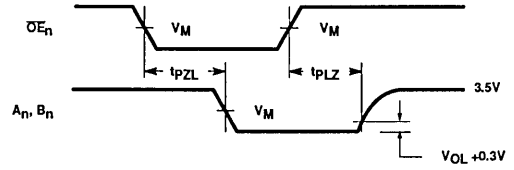
AC WAVEFORMS



Waveform 1. Propagation Delay for Data to Output



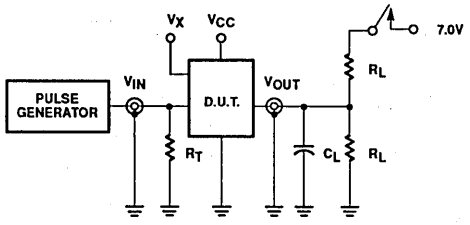
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



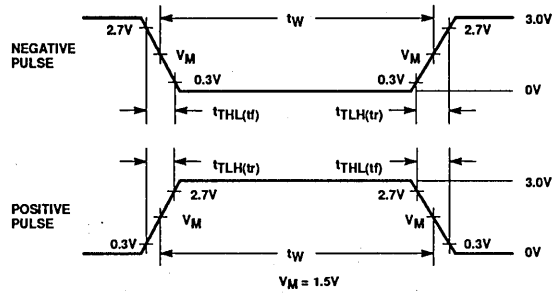
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

54F253
Multiplexer

Dual 4-Input Multiplexer (3-State)

Product Specification

Military Logic Products

FEATURES

- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable Inputs**

DESCRIPTION

The 54F253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S_0, S_1). When the individual Output Enable (E_{0a}, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are High, the outputs are forced to a High impedance (Hi-Z) state.

The 54F253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs.

All but one device must be in the High impedance state to avoid high currents exceeding the maximum ratings. If the outputs of the 3-State devices are tied together Design of the Output Enable signals must ensure that there is no overlap.

ORDERING INFORMATION

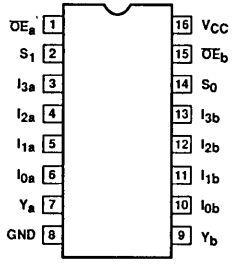
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F253/BEA
16-Pin Ceramic FlatPack	54F253/BFA
16-Pin Ceramic LLCC	54F253/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a} - I_{3a}	Port A data inputs	1.0/1.0	20μA/0.6mA
I_{0b} - I_{3b}	Port B data inputs	1.0/1.0	20μA/0.6mA
S_0 - S_1	Common select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}_a$	Port A output enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}_b$	Port B output enable input (active Low)	1.0/1.0	20μA/0.6mA
Y_a, Y_b	3-State outputs	50/33	1.0mA/20mA

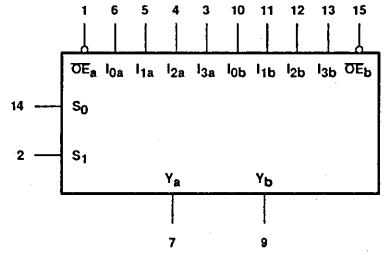
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



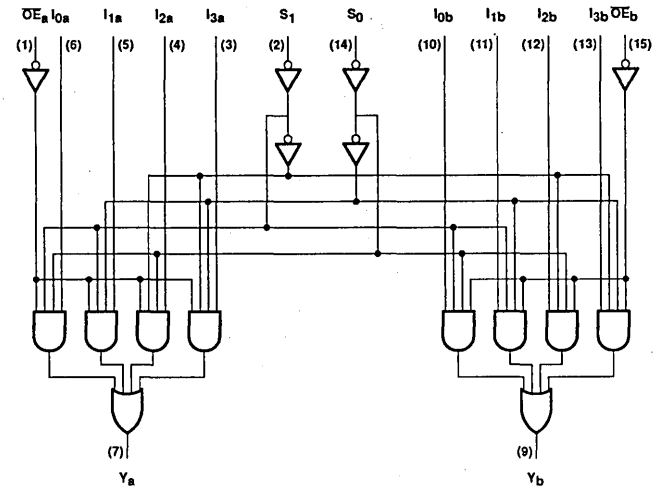
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC Pin Assignment, See JEDEC Standard No. 2

FUNCTION TABLE

INPUTS						OUTPUT	
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH2}	High-level output current			-3	mA
I_{OH1}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH2} = -3mA	2.4			V
			I_{OH1} = -1mA	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OZH}	Off-state output current High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-60	-80	-150	mA
I_{CC}	Supply current[4] (total) I_{CCH}	V_{CC} = Max	$\overline{OE}_n$ = GND; S_n = $I_n \geq$ 4.0V		10	16	mA
	I_{CCL}		$\overline{OE}_n$ = S_n = I_n = GND		12	23	mA
	I_{CCZ}		$\overline{OE}_n \geq$ 4.0V; I_n = S_n = GND		14	23	mA

AC ELECTRICAL CHARACTERISTICS

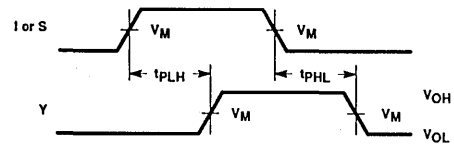
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1	3.0 3.0	4.5 5.0	7.0 7.0	2.5 2.5	9.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1	5.5 4.5	7.5 8.5	12.5 11.0	3.5 2.5	15.0 14.0	ns ns
t_{PZH}	Output enable time to High level	Waveform 2	3.0	6.5	9.0	2.5	10.5	ns
t_{PZL}	Output enable time to Low level	Waveform 3	3.0	6.5	9.5	2.5	11.0	ns
t_{PHZ}	Output disable time from High level	Waveform 2 Waveform 3	2.0	3.5	5.0	2.0	6.5	ns
t_{PLZ}	Output disable time from Low level	Waveform 3 Waveform 4	2.0	3.0	6.0	2.0	9.0	ns

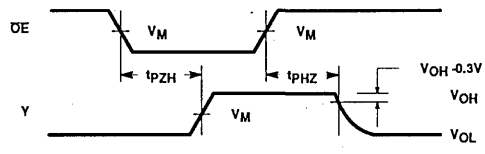
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with outputs opened.

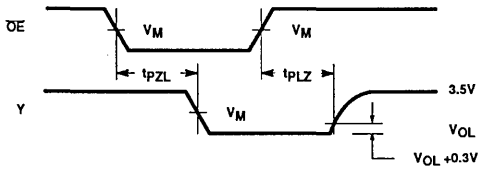
AC WAVEFORMS



Waveform 1. Propagation Delay Data and Select to Output



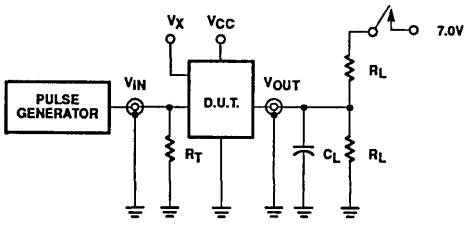
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



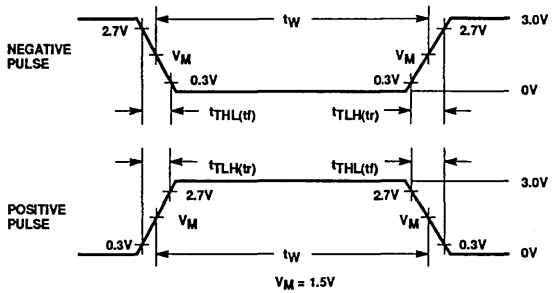
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per Function Table.

54F257A
Data Selector/Multiplexer

Quad 2-Line to 1-Line Data Selector/Multiplexer (3-State)

Product Specification

FEATURES
- **Multifunction capability**
- **Non-inverting data path**
- **3-State outputs**
- **See 54F258A for inverting version**

DESCRIPTION
The 54F257A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is Low and the I_1 inputs are selected when the Select input is High. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The 54F257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a High impedance "off" state when the Output Enable input ($\overline{OE}$) is High. All but one device must be in the High impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

ORDERING INFORMATION

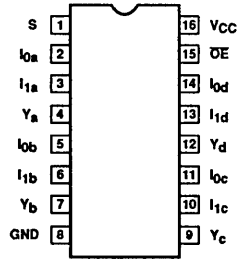
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F257A/BEA
16-Pin Ceramic FlatPack	54F257A/BFA
16-Pin Ceramic LLCC	54F257A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n} - I_{1n}	Data inputs	1.0/1.0	20µA/0.6mA
S	Common select input	1.0/1.0	20µA/0.6mA
$\overline{OE}$	Enable input (active Low)	1.0/1.0	20µA/0.6mA
Y_a, Y_d	Data outputs	150/33	3.0mA/20mA

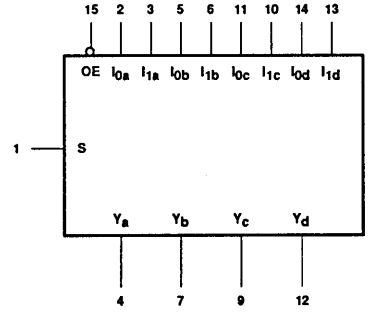
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

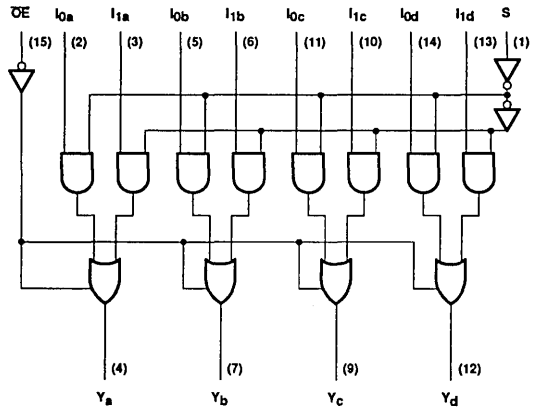
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

Data Selector/Multiplexer | 54F257A

LOGIC DIAGRAM



For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH2}	High-level output current			-3.0	mA
I_{OH1}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max,	I_{OH2} = -3mA	2.4			V
			V_{IH} = Min	I_{OH1} = -1mA	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	µA
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60	-80	-150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = Max			9.0	15.0	mA
		I_{CCL}				14.5	22.0	mA
		I_{CCZ}				15.0	23.0	mA

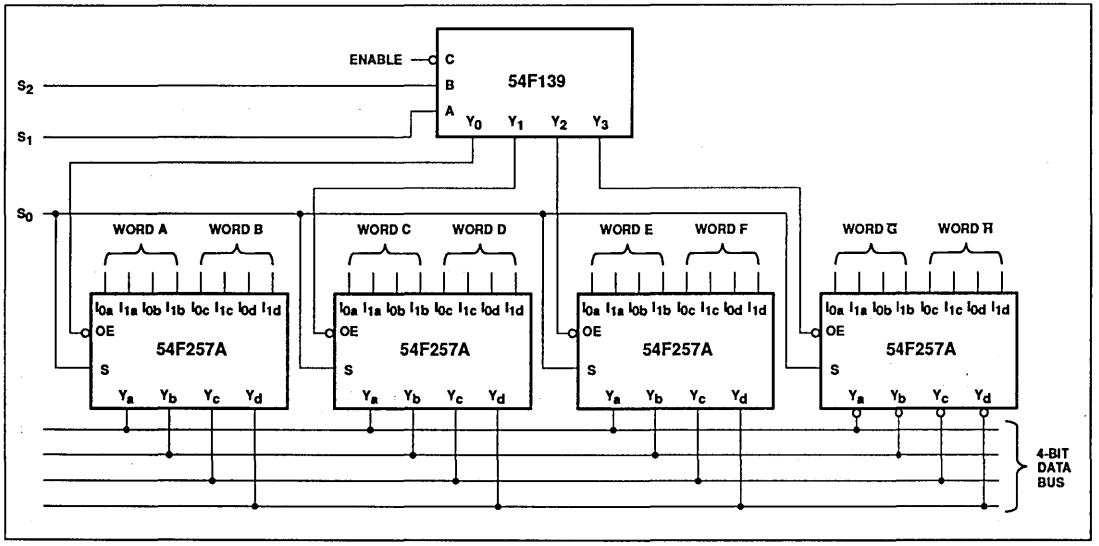
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_{na}, I_{nb} to Y_n	Waveform 1	3.0 2.0	4.5 3.5	6.0 5.0	3.0 1.5	8.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay S to Y_n	Waveform 1	4.5 4.0	7.5 5.5	9.5 7.0	4.5 4.0	11.5 9.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 2 Waveform 3	2.5 2.5	6.5 6.0	7.5 7.5	2.5 2.5	9.5 9.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low	Waveform 2 Waveform 3	2.0 2.0	4.0 3.5	5.5 5.5	2.0 2.0	6.5 6.5	ns ns

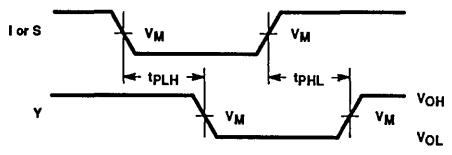
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. At typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with all outputs open and inputs grounded.

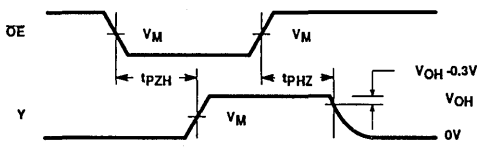
APPLICATIONS



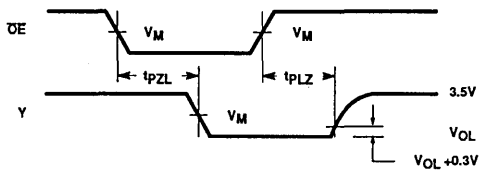
AC WAVEFORMS



Waveform 1. Propagation Delay Data and Select to Output



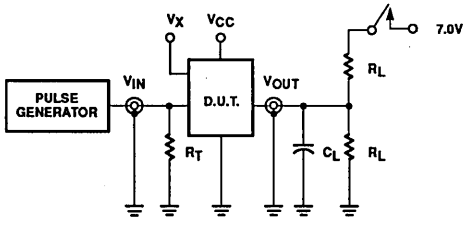
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



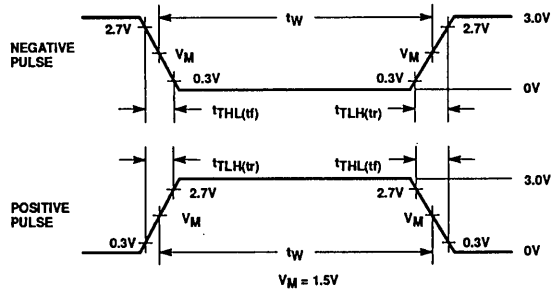
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per Function Table.

Signetics

54F258A
Data Selector/Multiplexer

Quad 2-Line to 1-Line Data Selector/Multiplexer (3-State)

Product Specification

Military Logic Products

FEATURES
- **Multifunction capability**
- **Non-inverting data path**
- **3-State outputs**
- **See 54F257A for non-inverting version**

DESCRIPTION
The 54F258A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Select input (S). The I_{0n} inputs are selected when the Select input is Low and the I_{1n} inputs are selected when the Select input is High. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The 54F258A is the logical implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic level supplied to the Select input. Outputs are forced to a High impedance "off" state when the Output Enable input ($\overline{OE}$) is high. All but one device must be in the High impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

ORDERING INFORMATION

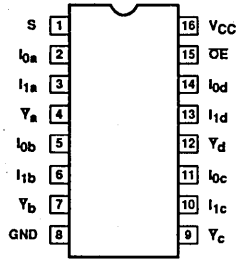
DESCRIPTION	ORDER CODE
Ceramic DIP	54F258A/BEA
Ceramic Flat Pack	54F258A/BFA
Ceramic LLCC	54F258A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0n} • I_{1n}	Data inputs	1.0/1.0	20μA/0.6mA
S	Common select input	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{Y}_a$ - $\overline{Y}_d$	Data outputs	150/40	3.0mA/20mA

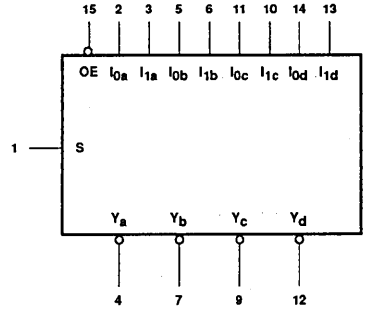
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

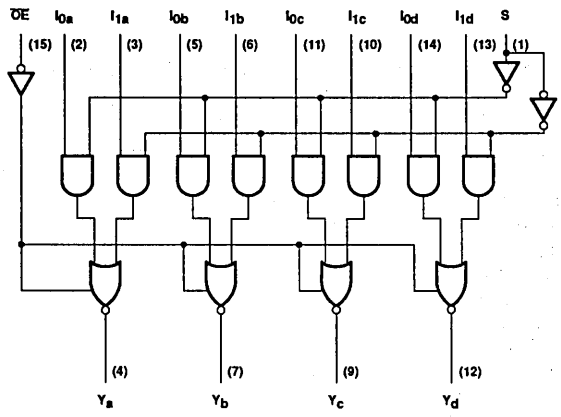
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

Data Selector/Multiplexer | 54F258A

LOGIC DIAGRAM



LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE

INPUTS				OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH2}	High-level output current			-3.0	mA
I_{OH1}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max,	I_{OH2} = -3mA	2.4			V
			V_{IH} = Min	I_{OH1} = -1mA	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-60	-80	-150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = Max			8.5	11.5	mA
		I_{CCL}				17.0	23.0	mA
		I_{CCZ}				16.0	22.0	mA

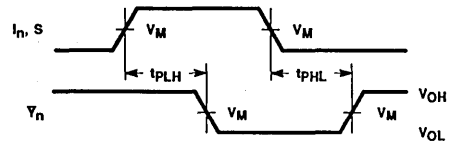
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$	Waveform 1	3.0 1.0	4.5 2.5	6.0 4.0	2.0 1.0	8.0 5.0	ns ns
t_{PLH} t_{PHL}	Propagation delay S to $\overline{Y}_n$	Waveform 1	3.5 2.5	6.5 6.0	8.0 8.0	3.5 2.5	10.0 10.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 2 Waveform 3	4.0 4.0	6.0 5.5	7.5 7.5	3.5 3.5	9.5 9.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low	Waveform 2 Waveform 3	2.0 2.0	3.5 3.5	5.5 5.5	2.0 2.0	7.0 6.5	ns ns

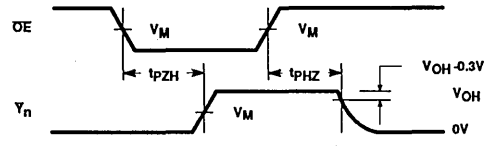
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. At typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with all outputs open.

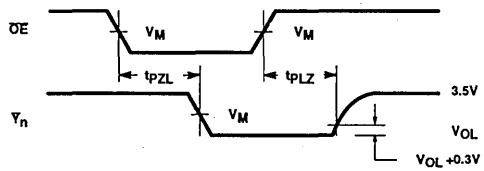
AC WAVEFORMS



Waveform 1. Propagation Delay Data and Select to Output



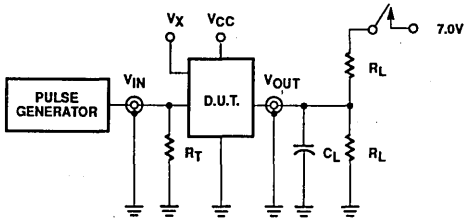
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



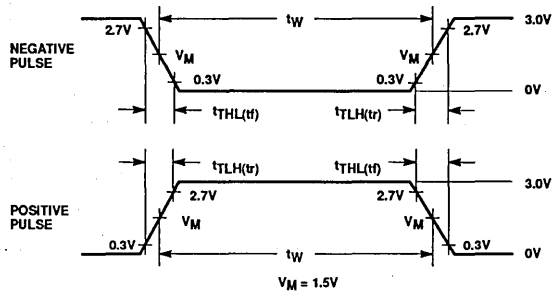
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per Function Table.

Signetics

Military Logic Products

54F259
Latch

8-Bit Addressable Latch

Product Specification

FEATURES

- **Combines demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common Clear input**
- **Useful as a 1-of-8 active High decoder**

DESCRIPTION

The 54F259 addressable latch has four distinct modes of operation that are selectable by controlling the Master Reset and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the store mode, all latches remain in their previous states and are unaffected by the Data or Address inputs.

To eliminate the possibility of entering erroneous data in the latches, the enable should be held High (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode ($\overline{MR}$ = $\overline{E}$ = Low), addressed outputs will follow the level of the D inputs, with all other outputs Low. In the Master Reset mode, all outputs are Low and unaffected by the Address and Data inputs.

ORDERING INFORMATION

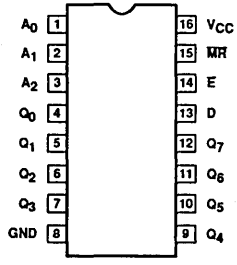
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F259/BEA
16-Pin Ceramic Flat Pack	54F259/BFA
20-Pin Ceramic LLCC	54F259/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{MR}$, $\overline{E}$	Master reset, enable inputs	1.0/1.0	20μA/0.6mA
A_0, A_2	Address Inputs	1.0/1.0	20μA/0.6mA
D	Data input	1.0/1.0	20μA/0.6mA
Q_0 - Q_7	Outputs	50/33	1mA/20mA

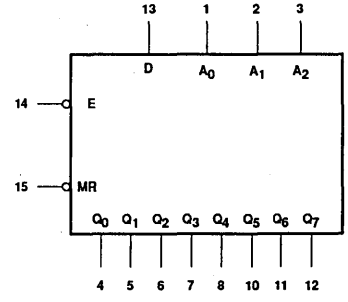
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



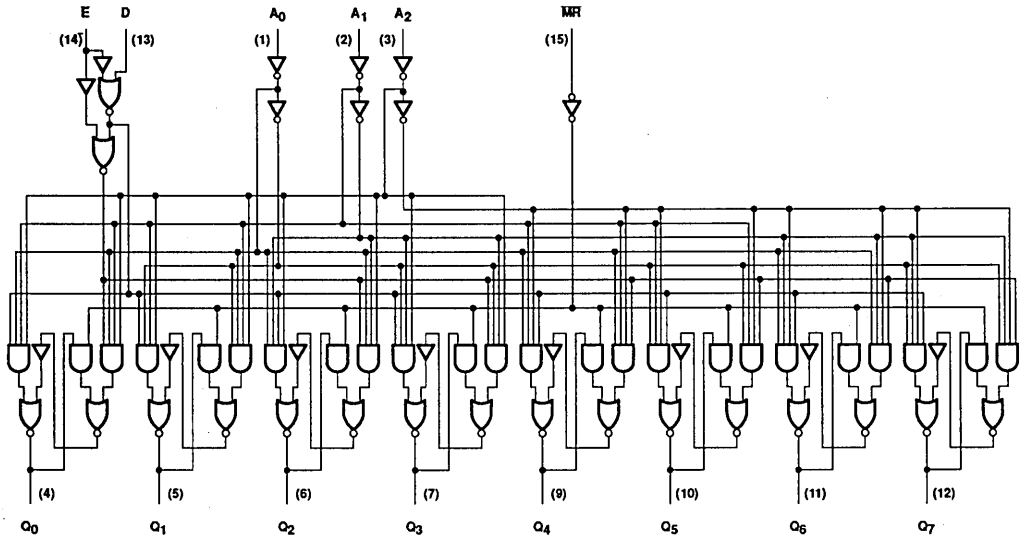
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC pin assignments, see JEDEC Standard No. 2

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS							
	$\overline{MR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplexer (active High decoder when D = H	L	L	d	L	L		Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	L	L	d	H	H	L	L	L	L	L	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable latch	H	L	d	L	L	L	Q = d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q = d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q = d	q_3	q_4	q_5	q_6	q_7
	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q = d

H = High voltage level steady state.
L = Low voltage level steady state.
X = Don't care.
d = High or Low data one set-up time prior to the Low-to-High Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max		24	46	mA
		I_{CCL}			37	75	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D to Q_n	Waveform 2	4.0 3.0	7.0 5.0	9.0 7.0	4.0 2.5	13.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n	Waveform 1	4.5 3.0	8.0 5.0	10.5 7.0	4.5 3.0	14.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 3	5.0 4.0	10.0 8.5	14.0 9.5	5.0 4.0	14.5 12.0	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 4	5.0	7.0	9.0	5.0	14.0	ns

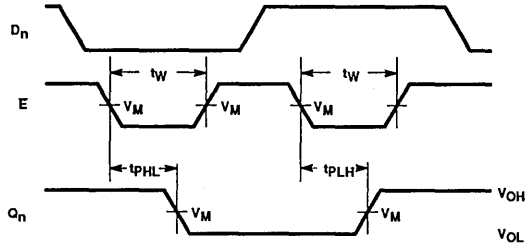
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D to $\overline{E}$	Waveform 5	3.0 6.5			3.0 8.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D to $\overline{E}$	Waveform 5	0 0			0 0		ns ns
t_s	Setup time, High or Low A_n to $\overline{E}$[4]	Waveform 6	2.0			2.0		ns
t_g	Hold time, High or Low A_n to $\overline{E}$[5]	Waveform 6	0			1.0		ns
t_w	$\overline{E}$ pulse width	Waveform 1	7.5			8.0		ns
t_w	$\overline{MR}$ pulse width	Waveform 4	3.0			4.0		ns

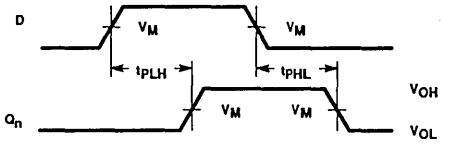
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. The Address to Enable setup time is the time before the High-to-Low Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
5. The Address to Enable hold time is the time after the Low-to-High Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

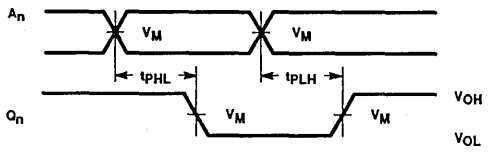
AC WAVEFORMS



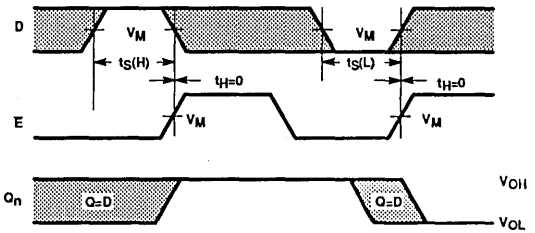
Waveform 1. Propagation Delay Enable to Output and Enable Pulse Width



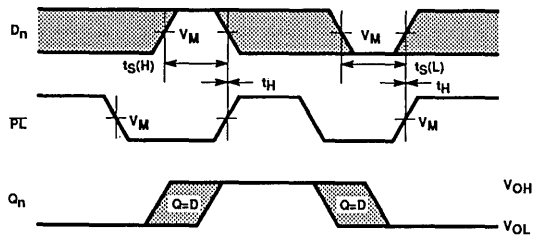
Waveform 2. Propagation Delay Data to Output



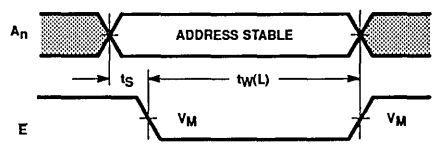
Waveform 3. Propagation Delay Address to Output



Waveform 4. Master Reset to Output Delay and Master Reset Pulse Width



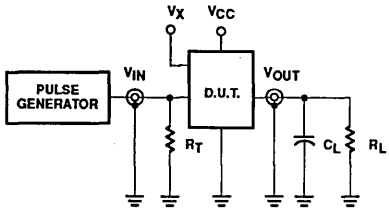
Waveform 5. Data Setup and Hold Times



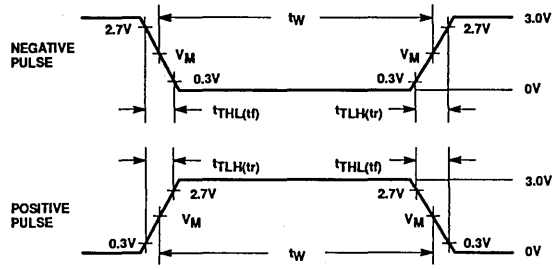
Waveform 6. Address Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F269
8-Bit Counter

8-Bit Bidirectional Binary Counter

Product Specification

FEATURES
- **Synchronous counting and loading**
- **Built-in lookahead carry capability**
- **Count frequency 115MHz typ**
- **Supply current 95mA typ**

DESCRIPTION
The 54F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

ORDERING INFORMATION

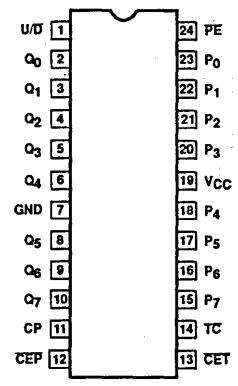
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54F269/BLA
24-Pin Ceramic Flat Pack	54F269/BKA
28-Pin Ceramic LLCC	54F269/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

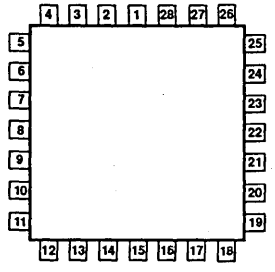
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	HIGH/LOW LOAD VALUE
P_0 - P_7	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{PE}$	Parallel enable input (active Low)	1.0/1.0	20μA/0.6mA
U/$\overline{D}$	Up-Down count control input	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count enable parallel input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count enable trickle input (active Low)	1.0/1.0	20μA/0.6mA
CP	Clock input	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1mA/20mA
Q_0 - Q_7	Flip-flop outputs	50/33	1mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



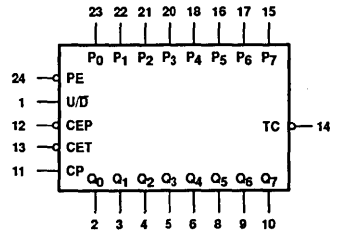
LLCC PIN CONFIGURATION



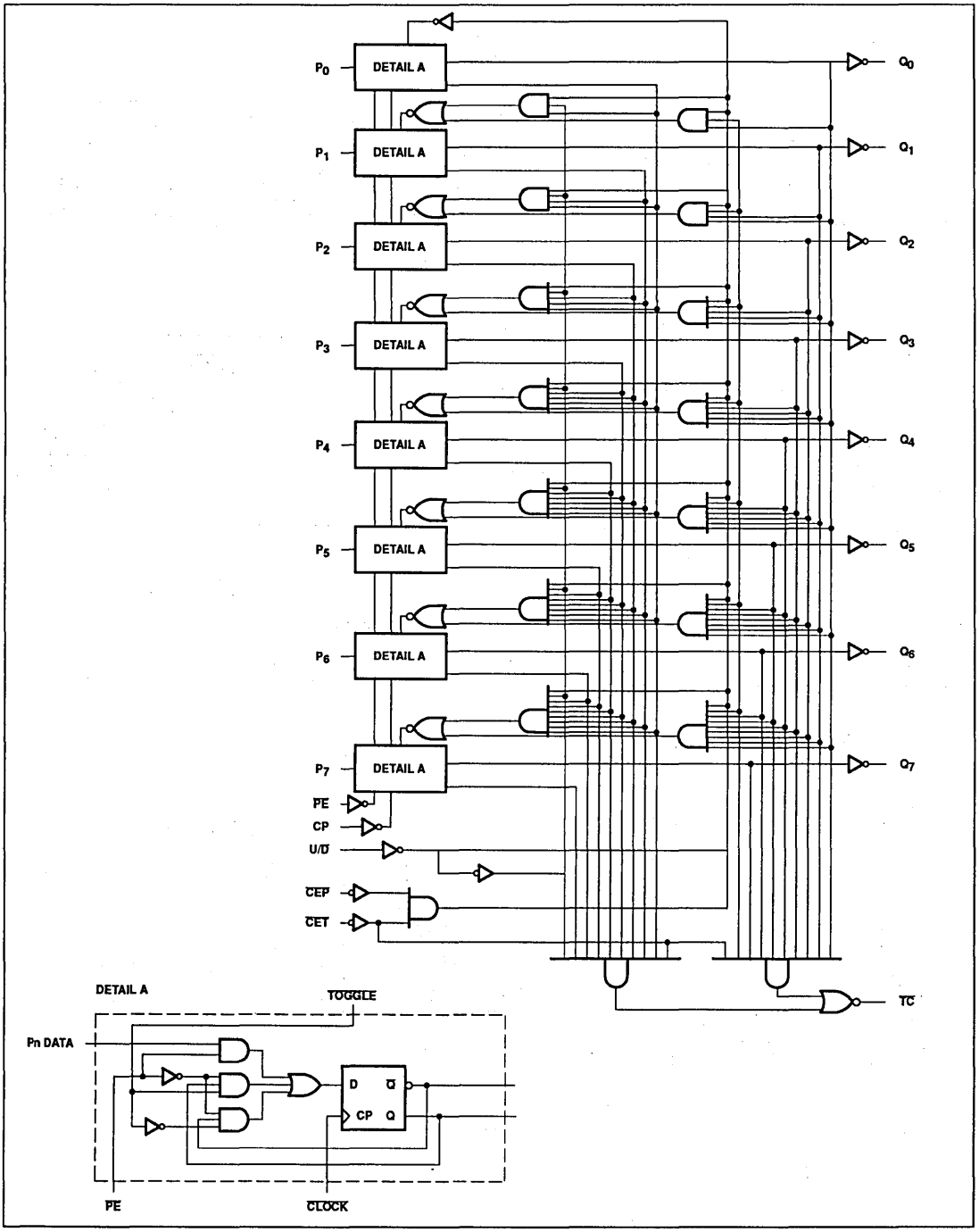
PIN/FUNCTION

1	NC	11	Q6	21	P4
2	U/$\overline{D}$	12	Q7	22	NC
3	Q0	13	CP	23	Vcc
4	Q1	14	$\overline{CEP}$	24	P3
5	Q2	15	NC	25	P2
6	Q3	16	$\overline{CET}$	26	P1
7	Q4	17	TC	27	P0
8	NC	18	P7	28	$\overline{PE}$
9	GND	19	P6		
10	Q5	20	P5		

LOGIC SYMBOL



LOGIC DIAGRAM

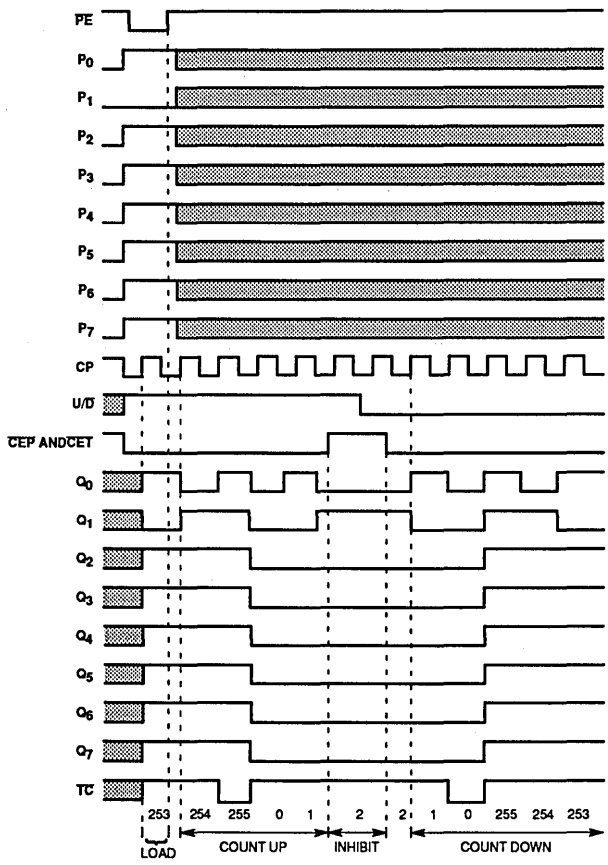


FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	P_n	Q_n	$\overline{TC}$
Parallel load	↑	X	X	X	l	l	L	(a)
	↑	X	X	X	l	h	H	(a)
Count Up	↑	h	l	l	h	X	Count Up	(a)
Count Down	↑	l	l	l	h	X	Count Down	(a)
Hold	↑	X	h	X	h	X	q_n	(a)
do nothing	↑	X	X	h	h	X	q_n	H

H = High voltage level steady state.
h = High voltage level one set-up time prior to the Low-to-High clock transition.
L = Low voltage level steady state.
l = Low voltage level one set-up time prior to the Low-to-High clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition.
↑ = Low-to-High clock transition
(a) = The $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count. Terminal Count Up is with all Q_n outputs High and Terminal Count Down is with all Qn outputs Low.

TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.50	5.0	5.5	V
V_{IH}	High-level input voltage[4]	2.0			V
V_{IL}	Low-level input voltage[4]			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = -Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min		2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level intput current		V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-60	-115	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	$\overline{PE}$ = $\overline{CET}$ = $\overline{CEP}$ = U/$\overline{D}$ = GND, P_n=4.5V, CP = ↑ , Outputs Open		93	120	mA
		I_{CCL}		$\overline{PE}$ = $\overline{CET}$ = $\overline{CEP}$ = U/$\overline{D}$ = GND, CP = ↑ Outputs Open		98	125	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		85		MHz
t_{PLH} t_{pPHL}	Propagation delay CP to Q_n (Load)	Waveform 1 $\overline{PE}$ = Low	3.5 4.0	6.0 6.5	9.0 8.5	3.5 4.0	10.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n (Count)	Waveform 1 $\overline{PE}$ = High	3.5 4.5	5.5 7.5	8.0 10.5	3.5 4.5	9.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 6.0	6.5 8.0	9.5 10.0	4.5 5.5	10.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.5 3.0	6.5 7.0	9.0 10.5	3.5 3.0	10.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 3	3.5 4.5	7.5 7.0	9.5 9.5	3.5 4.5	10.0 11.0	ns ns

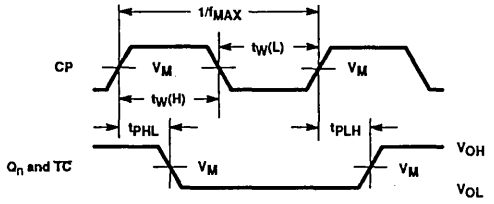
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low P_n to CP	Waveform 4	1.5 2.0			1.5 2.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low P_n to CP	Waveform 4	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low $\overline{PE}$ to CP	Waveform 4	5.0 5.0			8.5 9.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP	Waveform 4	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low $\overline{CET}$, $\overline{CEP}$ to CP	Waveform 5	4.5 6.5			8.0 10.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$, $\overline{CEP}$ to CP	Waveform 5	1.0 1.0			1.0 1.0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low U/$\overline{D}$ to CP	Waveform 6	7.0 5.5			12.5 12.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP	Waveform 6	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	Clock pulse width High or Low	Waveform 1	3.5 3.5			3.5 4.0		ns ns

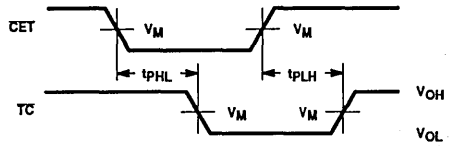
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. When testing devices to the functional table specified refer to the 'Recommended Operating Conditions' section of Application Note 202, "Testing and Specifying FAST Logic".

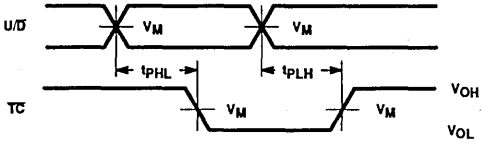
AC WAVEFORMS



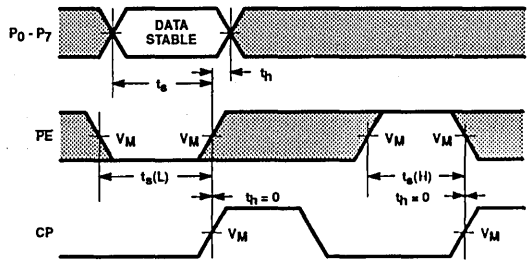
Waveform 1. Clock to Output Delays and Clock Pulse Width



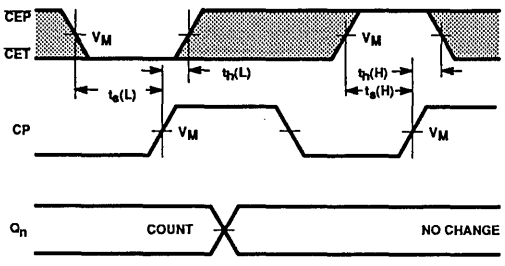
Waveform 2. Propagation Delays CET Input to Terminal Count Output



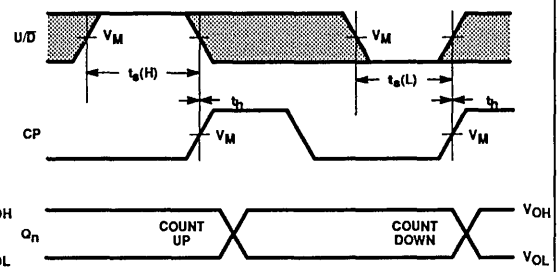
Waveform 3. Propagation Delays U/D Control to Terminal Count Output



Waveform 4. Parallel Data and Parallel Enable Set-up and Hold Times



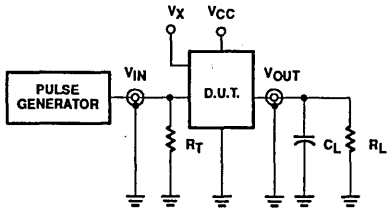
Waveform 5. Count Enable Set-Up and Hold Times



Waveform 6. Up/Down Control Set-Up and Hold Times

NOTE: For all waveforms, $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable output performance.

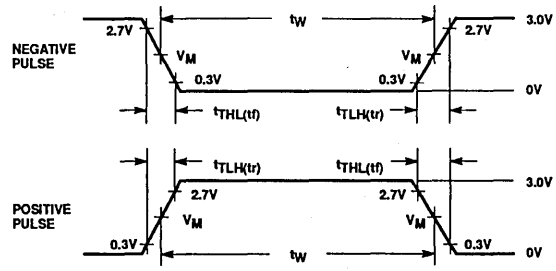
TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.



V_M = 1.5V

Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F273
Flip-Flop

Octal D Flip-Flop

Product Specification

DESCRIPTION

The 54F273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP)) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Ideal buffer for MOS microprocessor or memory**
- **Eight edge-triggered D-type flip-flops**
- **Buffered common Clock**
- **Buffered, asynchronous Master Reset**
- **See 54F377 for Clock Enable version**
- **See 54F373 for transparent latch version**
- **See 54F374 for 3-State version**

ORDERING INFORMATION

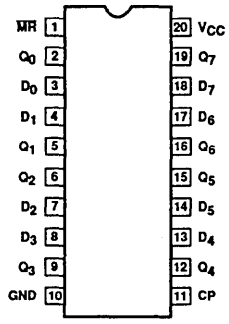
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F273/BRA
20-Pin Ceramic FlatPack	54F273/BSA
20-Pin Ceramic LLCC	54F273/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset (active-Low)	1.0/0.033	20μA/20μA
CP	Clock Pulse input (active rising edge)	1.0/0.033	20μA/20μA
Q_0 - Q_7	Data outputs	50/33	1.0mA/20mA

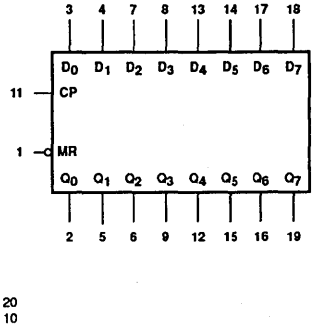
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC Pin Assignments, see JEDEC Standard No. 2

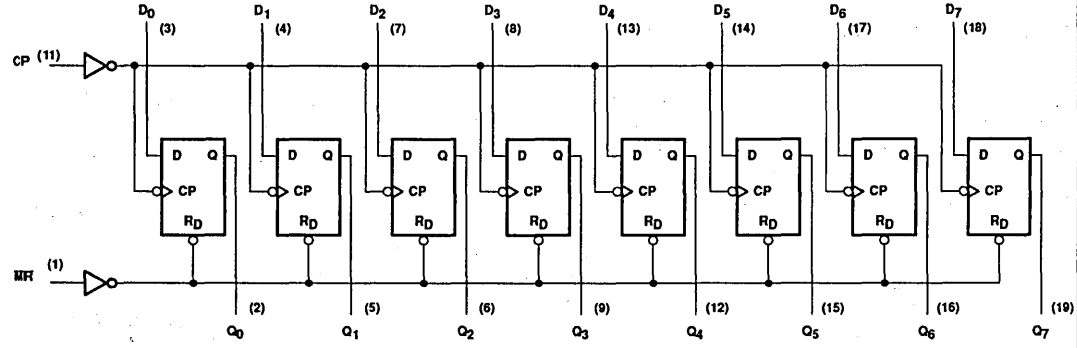
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

For LLCC Pin Assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS	
	$\overline{MR}$	CP	D_N	Q_N
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = High voltage level steady state
h = High voltage level one setup time prior to the High-to-Low Clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the High-to-Low Clock transition
X = Don't care
↑ = Low-to-High Clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{MR}$ & CP inputs[3]	V_{IH} = 4.5V, V_{IL} = 0.0V	V_{CC} = Min, I_{OH} = Max	2.5			V
		Other inputs	V_{IH} = Min, V_{IL} = Max					
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V[7]				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V[7]				20	µA
I_{IL}	Low-level intput current		V_{CC} = Max, V_I = 0.5V[7]				-20	µA
I_{OS}	Short-circuit output current[4]		V_{CC} = Max		-60		-150	mA
I_{CC}	Supply current[5] (total)	I_{CCH}	V_{CC} = Max, V_I = 4.5V			65	85	mA
		I_{CCL}	V_{CC} = Max, V_I = 0.0V			68	88	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	130	145		110[6]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	4.0 4.0	7.5 7.5	9.5 9.5	3.5 3.0	11.5 12.0	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	Waveform 2	4.5	7.0	9.5	3.0	12.0	ns

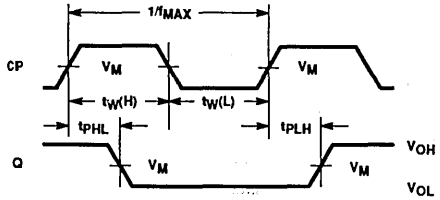
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	Waveform 3	3.0 3.0			3.0 4.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	Waveform 3	0 0			1.0 1.0		ns ns
t_{rec}	Recovery time $\overline{MR}$ to CP	Waveform 2	8.0			9.0		ns
t_w(H) t_w(L)	Clock pulse width High or Low	Waveform 1	4.0 5.0			6.0 6.0		ns ns
t_w(L)	Master Reset pulse width	Waveform 2	3.5			4.5		ns

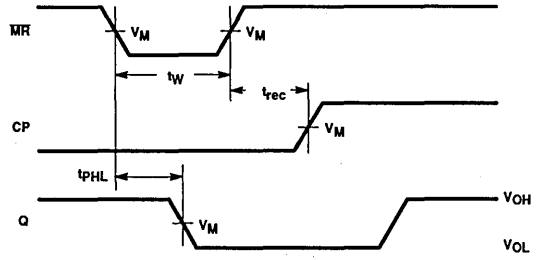
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under Recommended Operating Conditions for the applicable type, and Function Table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. To reduce the effect of external noise during test.
4. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests I_{OS} tests should be performed last.
5. Measure I_{CC} after a momentary ground, then 4.5V applied to clock with all outputs open and 4.5V applied to the Master Reset input.
6. This parameter is guaranteed, but not tested.
7. All input ≥4.5V except as noted.

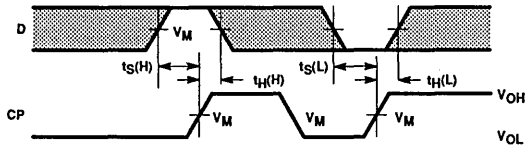
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



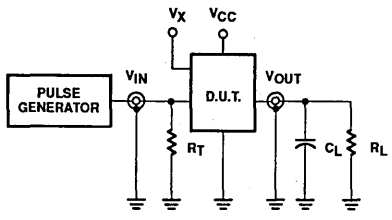
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



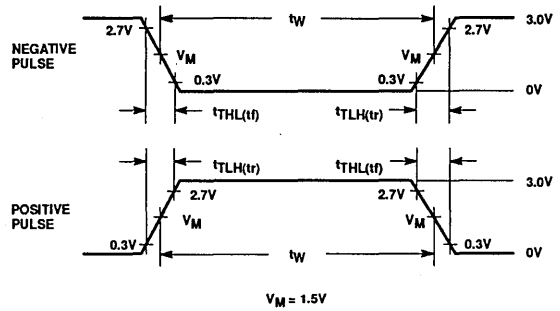
Waveform 3. Data Setup and Hold Times

NOTE: For all waveforms V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F280A, 54F280B
Parity Generator Checker

9-Bit Odd/Even Parity Generator/Checker

Product Specification

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **Buffered inputs — one normalized load**
- **Word length easily expanded by cascading**

DESCRIPTION

The 54F280A, 54F280B are 9-bit parity generators or checkers commonly used to detect errors in high-speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even parity output (Σ_E) is High when an even number of Data inputs (I_0 - I_8) are High. The odd parity output (Σ_O) is High when an odd number of Data inputs are High.

Expansion to larger word sizes is accomplished by tying the Even outputs (Σ_E) of up to nine parallel devices to the Data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 25ns with the 54F280A, 54F280B.

The 54F280B is a speed enhanced version with better t_{PLH} to t_{PHL} matching.

ORDERING INFORMATION

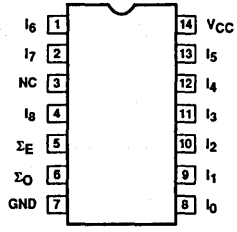
DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54F280A/BCA 54F280B/BCA
14-Pin Ceramic FlatPack	54F280A/BDA 54F280B/BDA
14-Pin Ceramic LLCC	54F280A/B2A 54F280B/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_0 - I_8	Data inputs	1.0/0.033	20μA/20μA
Σ_E, Σ_O	Parity outputs	50/33	1.0mA/20mA

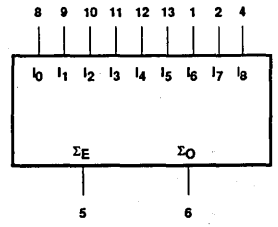
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

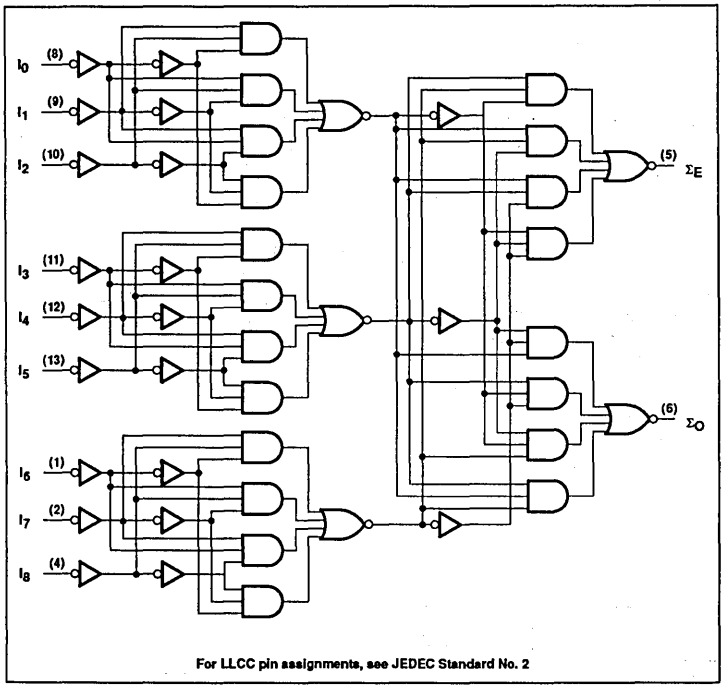


For LLCC pin assignments, see JEDEC Standard No. 2

Parity Generator Checker

54F280A, 54F280B

LOGIC DIAGRAM



For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE

INPUTS	OUTPUTS	
Number of High Data Inputs (I_0 - I_8)	Σ_E	Σ_O
Even — 0, 2, 4, 6, 8	H	L
Odd — 1, 3, 5, 7, 9	L	H

H = High voltage level
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{Ih} = Min, I_{OL} = Max		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		4.0	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V		-0.1	-20	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max, V_O = 0.0V	-60	-114	-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max		26	35	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS – 54F280A					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_E	Waveform 1, 2	5.0 4.0	7.0 11.1	9.0 13.0	4.0 4.0	11.0 17.0	ns ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_O	Waveform 1, 2	5.0 5.0	8.6 9.1	10.5 11.0	4.0 4.0	12.0 16.0	ns ns

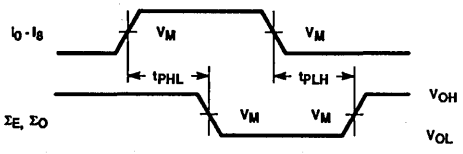
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS – 54F280B					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_E	Waveform 1, 2	4.0 4.0	6.5 7.0	9.0 10.0	3.0 3.5	11.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay I_0 - I_8 to Σ_O	Waveform 1, 2	4.0 4.0	6.5 7.0	9.0 10.0	3.0 3.5	11.0 12.0	ns ns

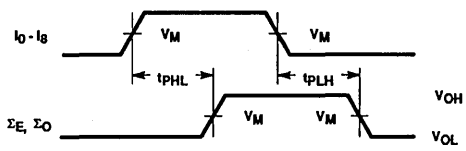
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with all outputs open.

AC WAVEFORMS



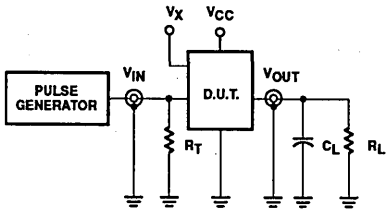
Waveform 1. Waveform for Inverting Outputs



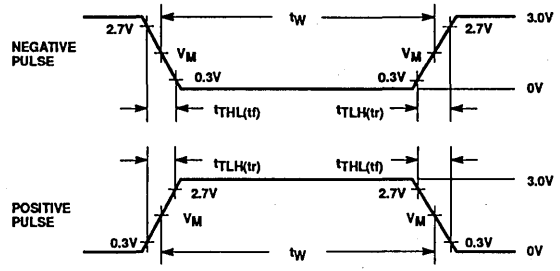
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F299
Register

8-Input Universal Shift/Storage Register (3-State)

Product Specification

FEATURES

- **Common parallel I/O for reduced pin count**
- **Additional serial inputs and outputs for expansion**
- **Four operating modes; Shift left, shift right, load and store**
- **3-State outputs for bus-oriented applications**

DESCRIPTION

The 54F299 is an 8-bit universal shift/storage register with 3-State outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0 and Q_7 to allow easy serial cascading. A separate active-Low Master Reset is used to reset the register.

ORDERING INFORMATION

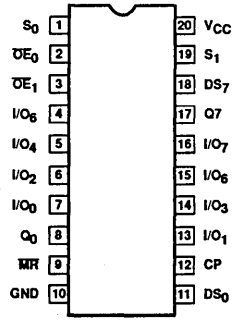
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F299/BRA
20-Pin Flat Pack	54F299/BSA
20-Pin Ceramic LLCC	54F299/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CP	Clock pulse input (Active rising edge)	1.0/1.0	20µA/0.6mA
DS_0	Serial data input for right shift	1.0/1.0	20µA/0.6mA
DS_7	Serial data input for left shift	1.0/1.0	20µA/0.6mA
S_0, S_1	Mode select inputs	1.0/2.0	20µA/0.6mA
$\overline{MR}$	Asynchronous Master Reset input	1.0/1.0	20µA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable input (Active Low)	1.0/1.0	20µA/0.6mA
I/O_n	Parallel data inputs or 3-State parallel outputs	3.5/1.0 150/33	70µA/0.6mA 3.0mA/20mA
Q_0, Q_7	Serial outputs	50/33	1.0mA/20mA

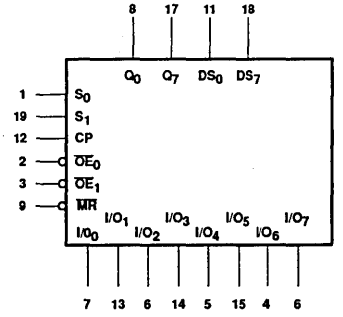
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High State and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see Jedec Standard No. 2

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

For LLCC pin assignments, see Jedec Standard No. 2

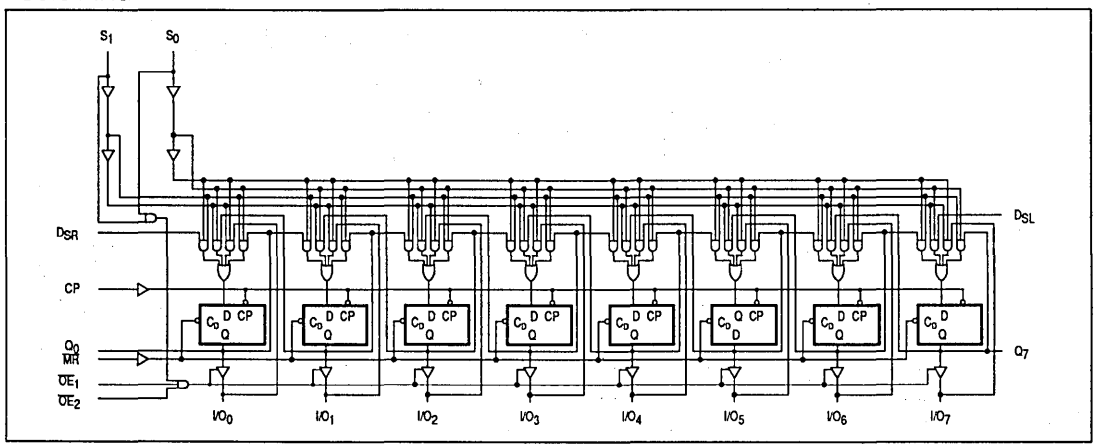
Register | 54F299

The 54F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. the type of operation is determined by S_0 and S_1, as shown in the Function Table. All flip-flop outputs are brought out through 3-State buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A Low signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended set-up and hold times, relative to the rising edge of CP, are observed.

A High signal on either OE_0 or OE1 disables the 3-State buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-State buffers are also disabled by High signals on both S_0 and S_1 in preparation for a parallel load operation.

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
$\overline{MR}$	$\overline{OE}_n$	S_1	S_0	CP	
L	L	X	X	X	Asynchronous Reset; Q_0 - Q_7 = Low
H	L	H	H	↑	Parallel load; $I/O_n \rightarrow Q_n$
H	L	L	H	↑	Shift right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	L	H	L	↑	Shift left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	L	X	Hold
X	H	X	X	X	Outputs Disabled

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_I	Input voltage range		-0.5 to +7.0	V
I_I	Input current range		-30 to +5	mA
V_O	Voltage applied to output in High output state range		-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	Q_0 - Q_7	40	mA
		I/O_n	40	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q_0, Q_7			-1	mA
		I/O_n			-3	mA
I_{OL}	Low-level output current	Q_0, Q_7			28	mA
		I/O_n			20	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	Q_0, Q_7	V_{CC} = Min, V_{IL} = Max	I_{OH} = -1mA	2.5			V
		I/O_n	V_{IH} = Min	I_{OH} = -3mA	2.4			V
				I_{OH} = -1mA	2.5	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			.35	.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	others	V_{CC} = 0V, V_I = 7.0V				100	µA
		I/O_n	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current	S_0, S_1	V_{CC} = Max, V_I = 0.5V				-1.2	mA
		others				-0.4	-0.6	mA
I_{OZH} + I_{IH}	Off-state output current High-level voltage applied	I/O_n only	V_{CC} = Max, V_I = 2.7V				70	µA
I_{OZL} + I_{IL}	Off-state output current Low-level voltage applied	I/O_n only	V_{CC} = Max, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			50	85	mA
		I_{CCL}				64	85	mA
		I_{CCZ}				60	85	mA

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	85	115		85[4]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_0 or Q_7	Waveform 1	3.5 4.5	5.0 6.0	7.0 8.0	3.5 4.5	9.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.0 5.0	6.0 6.5	9.0 9.0	4.0 5.0	11.0 11.5	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_0 or Q_7	Waveform 2	5.5	7.5	9.5	5.5	11.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.5	7.5	10.0	5.5	11.5	ns
t_{PZH} t_{PZL}	Output Enable time S_n, $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	3.5 4.0	6.0 7.5	8.0 10.0	3.5 4.0	10.0 12.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time S_n, $\overline{OE}$ to I/O_n	Waveform 4 Waveform 5	2.5 1.5	4.5 2.5	7.0 5.5	2.5 1.5	9.0 7.5	ns ns

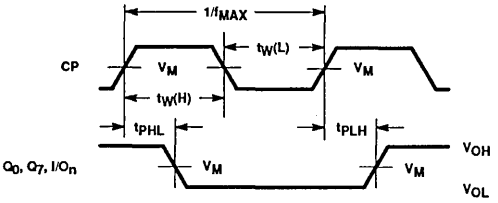
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_0 or S_1 to CP	Waveform 3	7.0 5.0			8.5 7.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_0 or S_1 to CP	Waveform 3	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low I/O_n, DS_0 or DS_1 to CP	Waveform 3	3.0 3.0			3.0 4.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n, DS_0, or DS_1 to CP	Waveform 3	0 0			0 0		ns ns
t_w	CP Pulse width	Waveform 1	4.0			4.0		ns
$t_w(L)$	$\overline{MR}$ Pulse width, Low	Waveform 2	4.0			4.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	4.0			4.0		ns

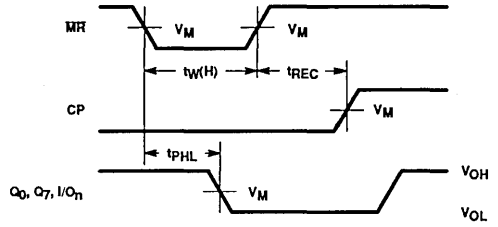
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Guaranteed and not tested parameter.

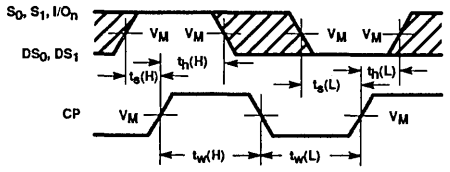
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Frequency

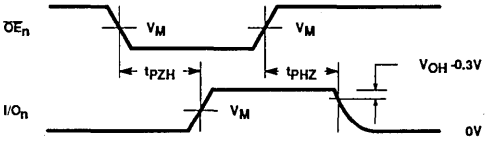


Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time.

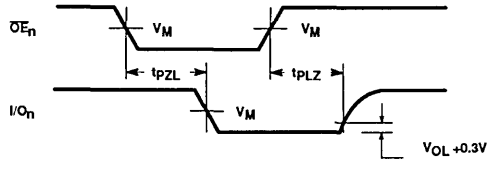


The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3. Data and Select Setup and Hold Times



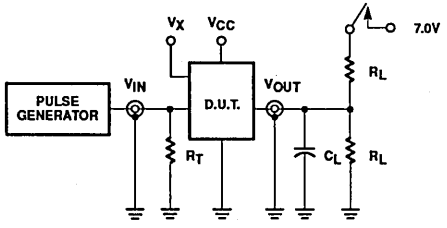
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



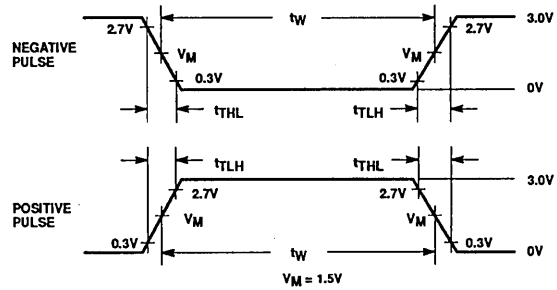
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

Military Logic Products

54F350
Shifter

4-Bit Shifter (3-State)

Product Specification

FEATURES

- **Shifts 4 bits of data to 0, 1, 2, 3 places under control of two select lines**
- **3-State outputs for bus organized systems**

DESCRIPTION

The 54F350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers.

The 54F350 can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical – with logic zeros filled in at either end of the shifting field.
2. Arithmetic – where the sign bit is extended during a shift down.
3. End around – where the data word forms a continuous loop.

The 3-State outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active Low Output Enable ($\overline{OE}$) input controls the state of the outputs. The outputs are in the High impedance "off" state when $\overline{OE}$ is High, and they are active when $\overline{OE}$ is Low.

ORDERING INFORMATION

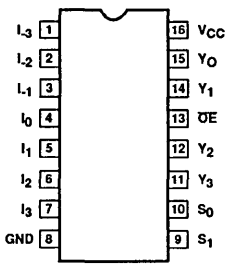
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F350/BEA
16-Pin Ceramic FlatPack	54F350/BFA
20-Pin Ceramic LLCC	54F350/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
S_0, S_1	Select inputs	1.0/2.0	20μA/1.2mA
I_{-3} - I_3	Data inputs	1.0/2.0	20μA/1.2mA
$\overline{OE}$	Output enable input (Active Low)	1.0/2.0	20μA/1.2mA
Y_0 - Y_3	3-State outputs	150/33.3	3.0mA/20mA

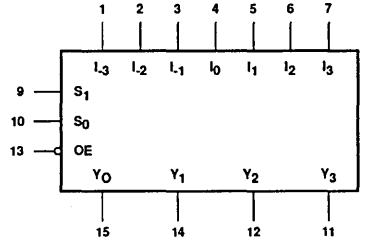
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High State and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

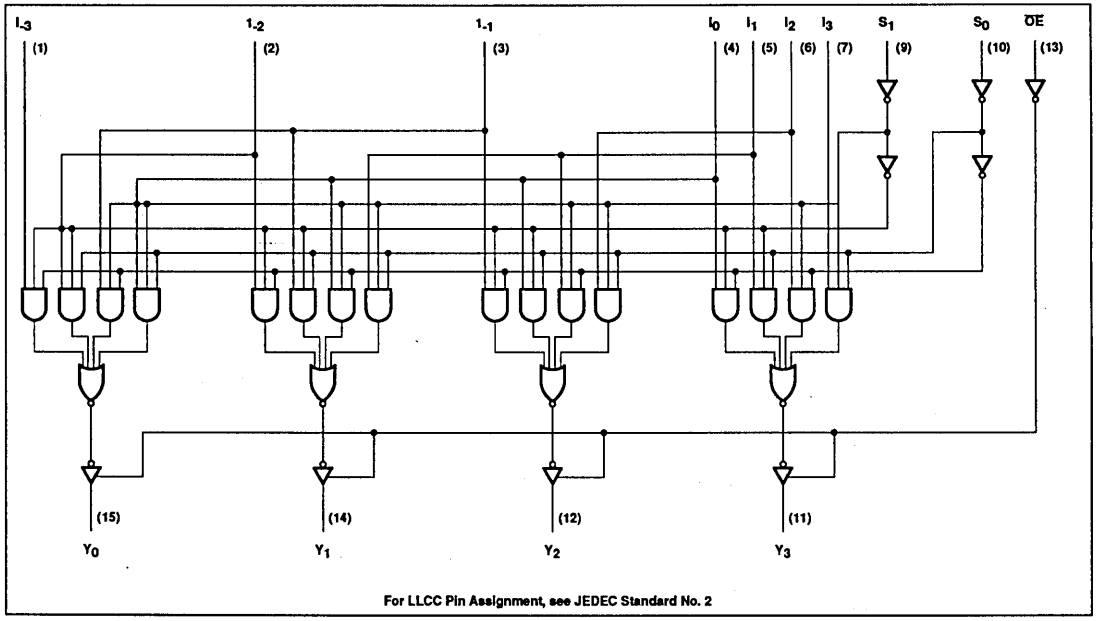
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

Shifter | 54F350

LOGIC DIAGRAM



For LLCC Pin Assignment, see JEDEC Standard No. 2

FUNCTION TABLE

$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state
D_n = High or Low state of referenced I_n input

LOGIC EQUATIONS

$$Y_0 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_0 + S_0 \cdot \overline{S}_1 \cdot I_{-1} + \overline{S}_0 \cdot S_1 \cdot I_{-2} + S_0 \cdot S_1 \cdot I_{-3}$$
$$Y_1 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_1 + S_0 \cdot \overline{S}_1 \cdot I_0 + \overline{S}_0 \cdot S_1 L_1 + S_0 \cdot S_1 \cdot L_2$$
$$Y_2 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_2 + S_0 \cdot \overline{S}_1 \cdot I_1 + \overline{S}_0 \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot L_1$$
$$Y_3 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_3 + S_0 \cdot \overline{S}_1 \cdot I_2 + \overline{S}_0 \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0$$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH2}	High-level output current			-3	mA
I_{OH1}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH2}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH2} = -3mA	2.4			V
V_{OH1}	High-level output voltage			I_{OH1} = -1mA	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.9	-1.2	mA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60	-90	-150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = Max			22	35	mA
		I_{CCL}				26	41	mA
		I_{CCZ}				26	42	mA

AC ELECTRICAL CHARACTERISTICS

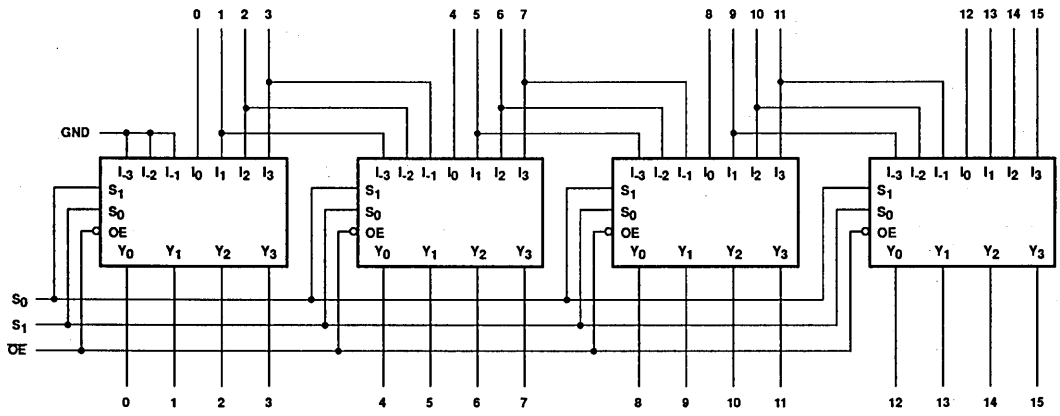
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic."

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 2.5	4.5 4.0	6.0 5.5	3.0 2.5	7.0 6.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Y_n	Waveform 1	4.0 3.0	7.8 6.5	10 8.5	4.0 3.0	11 9.5	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 2 Waveform 3	2.5 4.0	5.0 7.0	7.0 9.0	2.5 4.0	10 10	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 2 Waveform 3	2.0 2.0	3.9 4.0	5.5 5.5	2.0 2.0	6.5 6.5	ns ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

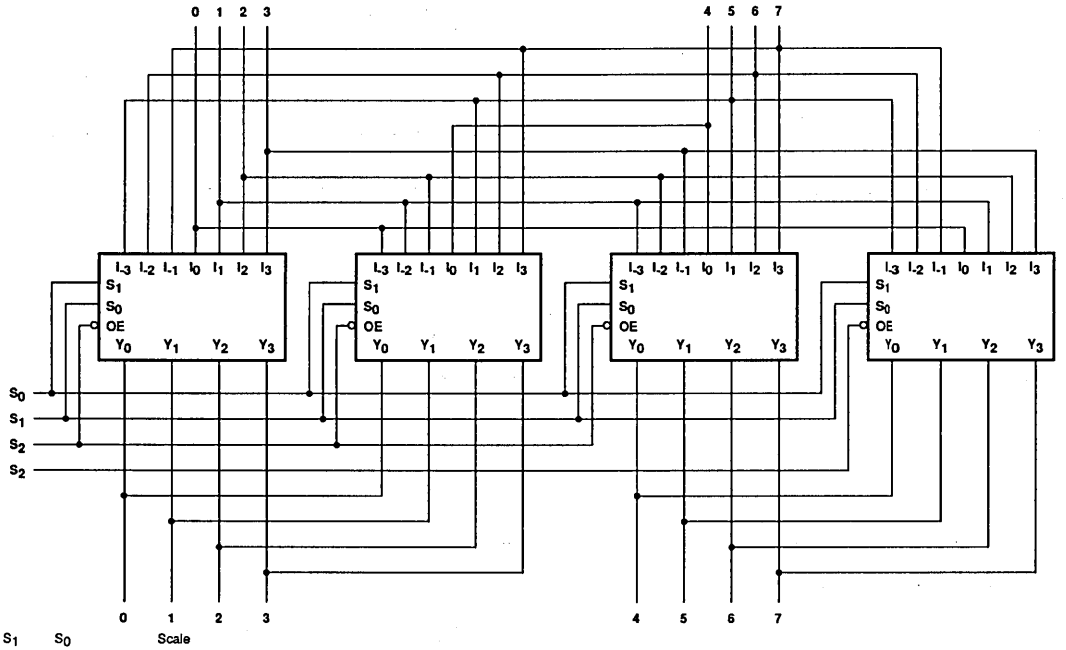
APPLICATIONS



S_2	S_1S_0	
L	L L	No shift
L	L H	Shift end around 1
L	H L	Shift end around 2
L	H H	Shift end around 3
H	L L	Shift end around 4
H	L H	Shift end around 5
H	H L	Shift end around 6
H	H H	Shift end around 7

8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places

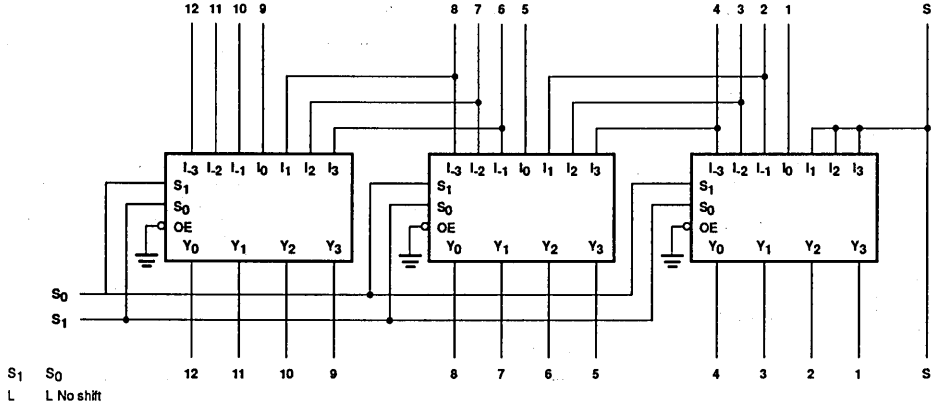
APPLICATIONS (Continued)



S_1	S_0	Scale
L	L+8	1/8
L	H+4	1/4
H	L+2	1/2
H	H No change	1

13-Bit Two's Complement Scaler

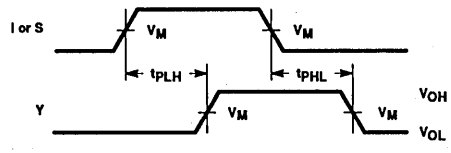
APPLICATIONS (Continued)



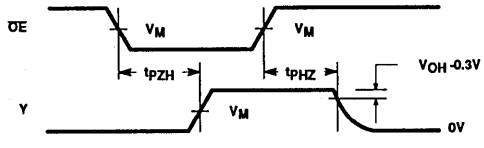
S_1	S_0
L	L No shift
L	H Shift 1 place
H	L Shift 2 places
H	H Shift 3 places

16-Bit Shift Up 0, 1, 2, or 3 Places

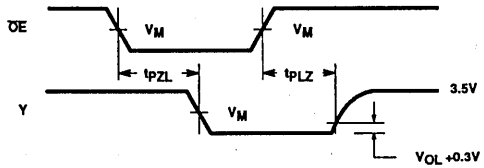
AC WAVEFORMS



Waveform 1. Propagation Delay Data and Select to Output



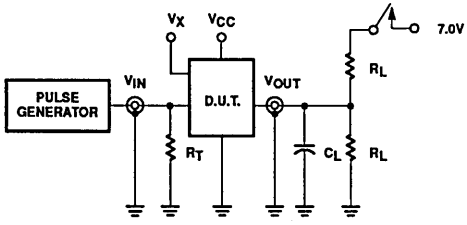
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



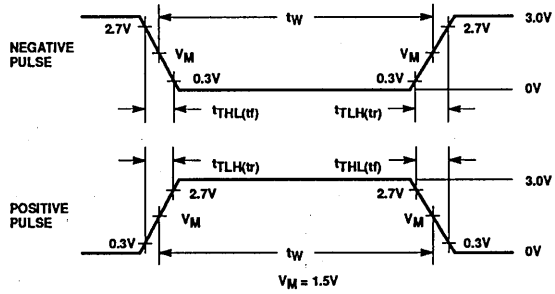
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per Function Table.

Signetics

54F367
Buffer/Driver

Hex Buffer/Driver (3-State)

Product Specification

Military Logic Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in Low and High states)**
- **3-State buffer outputs sink 48mA**
- **High-speed**
- **Bus oriented**

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}_n$	I	Y_n
L	L	L
L	H	H
H	X	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z)= High impedance (off) state

ORDERING INFORMATION

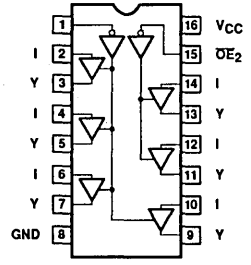
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F367/BEA
16-Pin Ceramic Flat Pack	54F367/BFA
20-Pin Ceramic LLCC	54F367/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_1$, $\overline{OE}_2$	3-State output enable input (active Low)	1.0/0.033	20μA/20μA
I_0 - I_5	Inputs	1.0/0.033	20μA/20μA
Y_0 - Y_5	Outputs	600/80	12mA/48mA

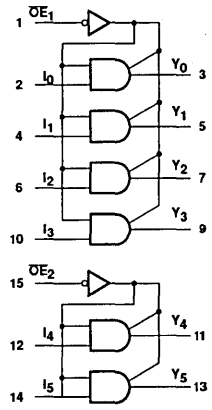
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to 5.5	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-1	mA
I_{OH2}	High-level output current			-3	mA
I_{OH3}	High-level output current			-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min,	I_{OH1} = -1mA	2.5			V
			V_{IL} = Max,	I_{OH2} = -3mA	2.4			V
			V_{IH} = Min	I_{OH3} = -12mA	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-1	-20	µA
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			25	35	mA
		I_{CCL}				47	62	mA
		I_{CCZ}				35	48	mA

AC ELECTRICAL CHARACTERISTICS

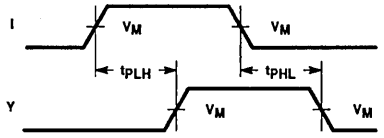
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic."

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	Waveform 1	3.0 3.0	4.5 5.5	6.5 7.0	3.0 3.0	8.0 8.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 2 & 3	3.0 3.0	5.5 6.5	7.5 8.5	3.0 3.0	9.0 10.0	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High to Low level	Waveform 2 & 3	2.5 2.5	4.5 4.0	6.5 6.0	2.5 2.0	7.5 7.0	ns ns

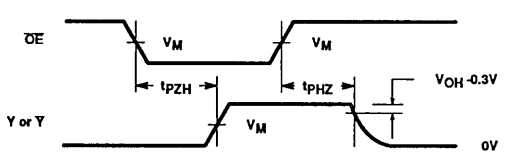
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

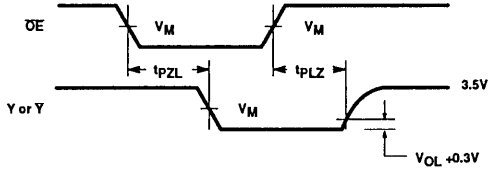
AC WAVEFORMS



Waveform 1. For Non-Inverting Outputs



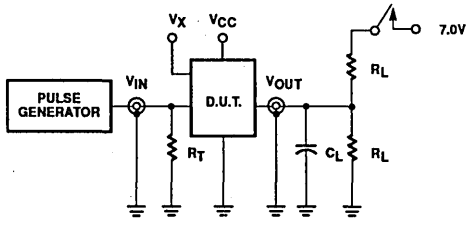
Waveform 2. 3-State Output Enable time to High level and Output Disable time from High level



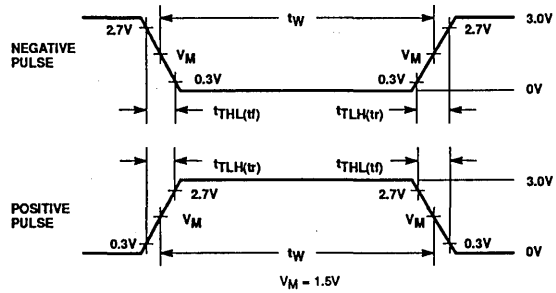
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

Military FAST Products

54F373, 54F374
Latches/Flip-Flops

54F373 Octal Transparent Latch (3-State)
54F374 Octal D Flip-Flop (3-State)

Product Specification

FEATURES

- **8-bit transparent latch — 54F373**
- **8-bit positive, edge-triggered register — 54F374**
- **3-State output buffers**
- **Common 3-State output enable**
- **Independent register and 3-State buffer operation**
- **See 54F573 for broadside pinout version of the 54F373**
- **See 54F574 for broadside pinout version of the 54F374**

DESCRIPTION

The 54F373 is an octal transparent latch coupled to eight 3-State output buffers.

The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one set-up time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

ORDERING INFORMATION

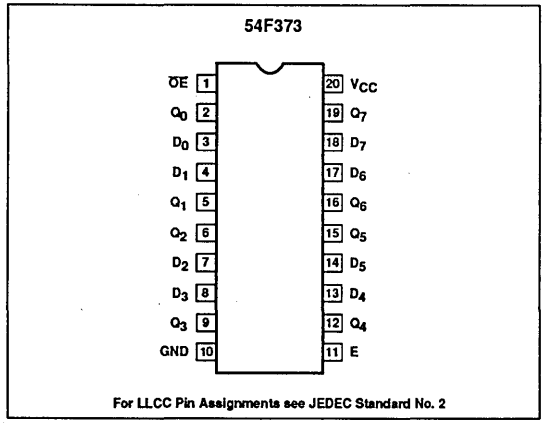
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F373/BRA, 54F374/BRA
20-Pin Ceramic FlatPack	54F373/BSA, 54F374/BSA
20-Pin Ceramic LLCC	54F373/B2A, 54F374/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

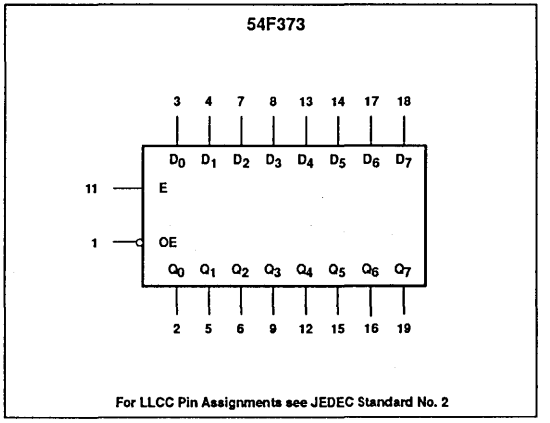
PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20μA/0.6mA
E (54F373)	Latch enable input (active High)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20μA/0.6mA
CP (54F374)	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
Q_0 - Q_7	3-State outputs	150/33	3mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

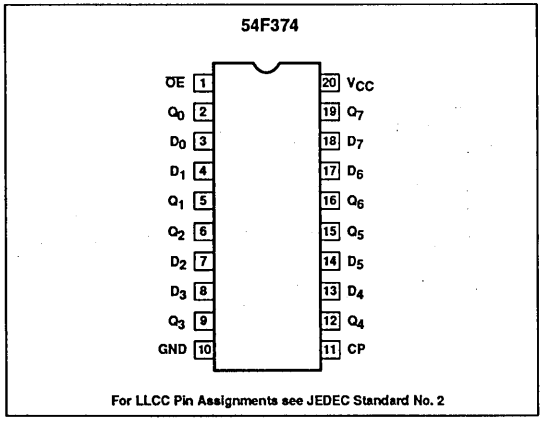
PIN CONFIGURATION



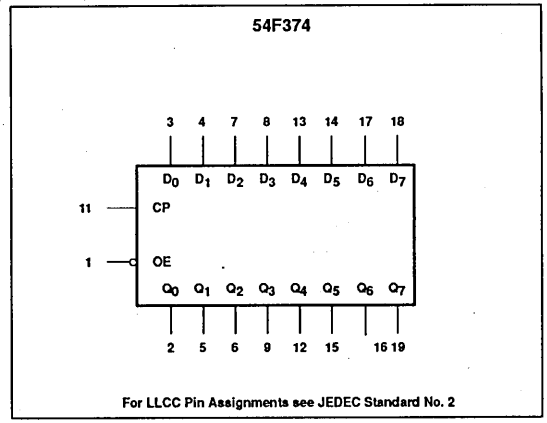
LOGIC SYMBOL



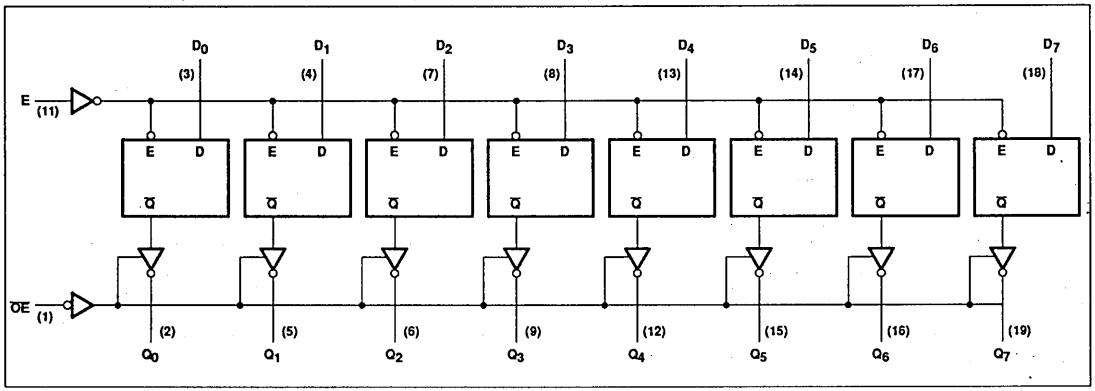
PIN CONFIGURATION



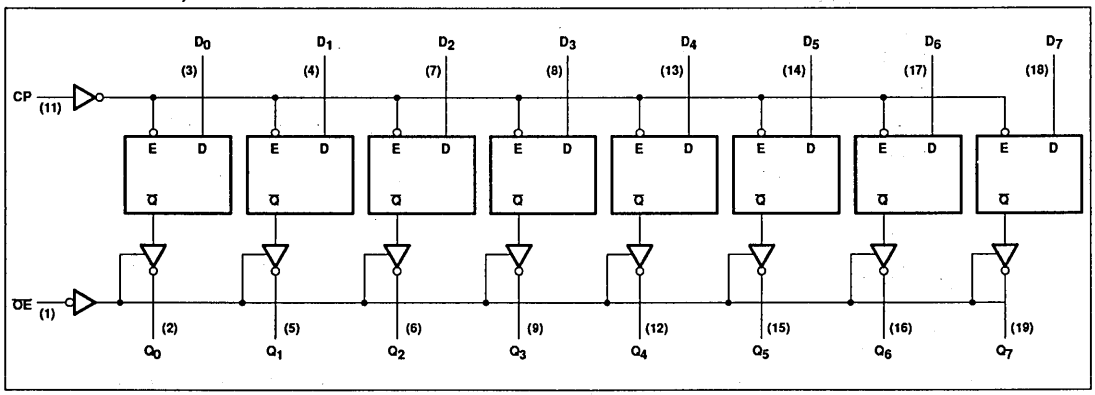
LOGIC SYMBOL



LOGIC DIAGRAM, 54F373



LOGIC DIAGRAM, 54F374



When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

The 54F374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT — FUNCTION TABLE, 54F373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		$Q_0 - Q_7$
Enable and read register	L L	H H	X X	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	X X	X X	X X	(Z) (Z)

MODE SELECT — FUNCTION TABLE, 54F374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$Q_0 - Q_7$
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	X X	X X	X X	(Z) (Z)

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition or High-to-Low E transition
L = Low voltage level
X = Don't care
l = Low voltage level one setup time prior to Low-to-High clock transition or High-to-Low E transition
(Z) = High impedance "off" state
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-1	mA
I_{OH2}	High-level output current			-3	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max	I_{OH1} = -1mA	2.5			V
				I_{OH2} = -3mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60		-150	mA
I_{CC}	Supply current (total)	54F373	V_{CC} = Max	I_{CCZ} $\overline{OE} \geq 4.0V$, D inputs = E = GND		35	55	mA
		54F374		I_{CCZ} CP ≥ 4.0V, D inputs = GND		57	86	mA

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	54F374	Waveform 6	100			60		MHz
t_{PLH} t_{PHL}	Propagation delay E to Q_n	54F373	Waveform 1	3.0 2.0	9.0 4.0	11.5 7.0	3.0 2.0	15.0 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	54F373	Waveform 4	3.0 2.0	5.3 3.7	7.0 5.0	3.0 1.7	8.5 6.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	54F374	Waveform 6	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.5 11.5	ns ns
t_{PZH}	Output enable time to High level	54F373 54F374	Waveform 2	2.0 2.0	5.0 9.0	11.0 11.5	2.0 2.0	13.5 14.0	ns ns
t_{PZL}	Output enable time to Low level	54F373 54F374	Waveform 3	2.0 2.0	5.6 5.3	7.5 7.5	2.0 2.0	10.0 10.0	ns ns
t_{PHZ}	Output disable time from High level	54F373 54F374	Waveform 2	2.0 2.0	4.5 5.3	6.5 7.0	2.0 2.0	10.0 8.0	ns ns
t_{PLZ}	Output disable time from Low level	54F373 54F374	Waveform 3	2.0 2.0	3.8 4.3	5.0 5.5	2.0 2.0	7.0 7.5	ns ns

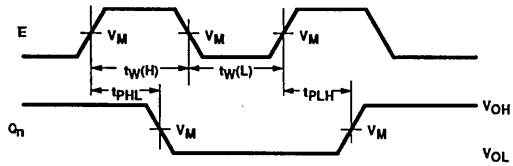
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low D_n to E	54F373	Waveform 5	2.0 2.0			2.0 2.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low D_n to E	54F373	Waveform 5	3.0 3.0			3.0 3.0		ns ns
t_w(H) t_w(L)	Clock pulse width	54F374	Waveform 6	7.0 6.0			7.0 6.0		ns ns
t_s(H) t_s(L)	Setup time, High or Low D_n to CP	54F374	Waveform 7	2.0 2.0			2.5 2.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low D_n to CP	54F374	Waveform 7	2.0 2.0			2.0 2.5		ns ns
t_w(H) t_w(L)	Latch enable pulse width	54F373	Waveform 1	6.0 6.0			6.0 6.0		ns ns

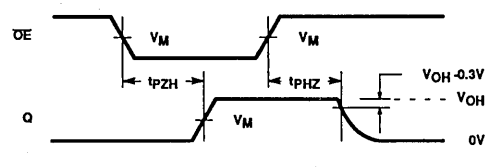
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

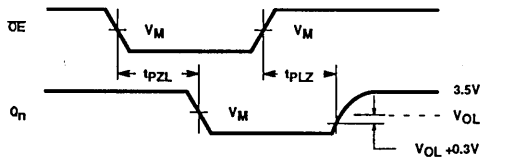
AC WAVEFORMS



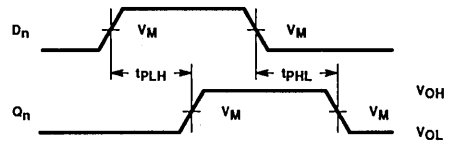
Waveform 1. Latch Enable to Output Delays and Latch Enable Pulse Width



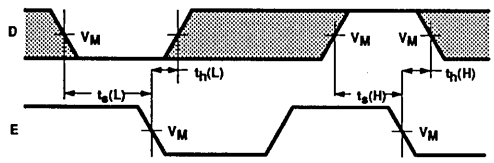
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



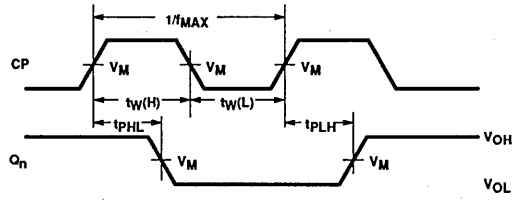
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



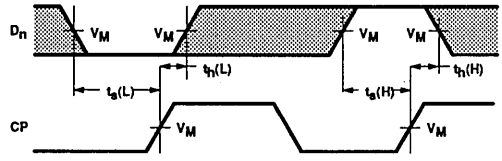
Waveform 4. Propagation Delay Data to Q Outputs



Waveform 5. Data Setup and Hold Times



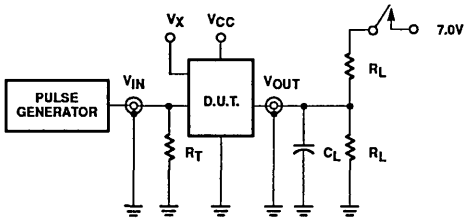
Waveform 6. Clock to Output Delays and Pulse Width



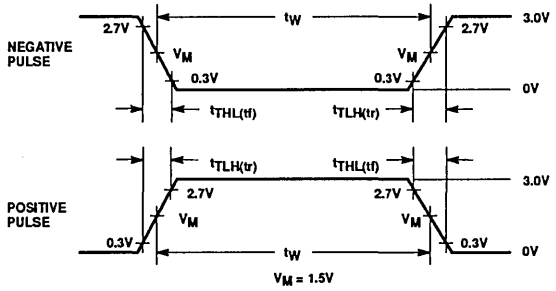
Waveform 7. Data Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All others	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	t_W	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per Function Table.

54F398, 54F399
Registers

54F398 – Quad 2-Port Register w/ True & Complementary Outputs
54F399 – Quad 2-Port Register

Product Specification

Military FAST Products

FEATURES

- **Select inputs from two data sources**
- **Fully positive edge-triggered operation**
- **Both True and Complementary outputs – 54F398**

DESCRIPTION

The 54F398 and 54F399 are the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 54F399 is the 16-pin version of the 54F398, with only the Q outputs of the flip-flops available.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F398/BRA 54F399/BEA
Ceramic Flat Pack	54F398/BSA 54F399/BFA
Ceramic LLCC	54F398/B2A 54F399/B2A

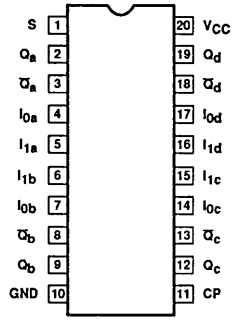
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_{0a} - I_{0d}	Data inputs from source 0	1.0/1.0	20µA/0.6mA
I_{1a} - I_{1d}	Data inputs from source 1	1.0/1.0	20µA/0.6mA
S	Common select input	1.0/1.0	20µA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20µA/0.6mA
Q_a - Q_d	Register true outputs	50/33	1.0mA/20mA
$\overline{Q}_a$ - $\overline{Q}_d$	Register complementary outputs (54F398)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

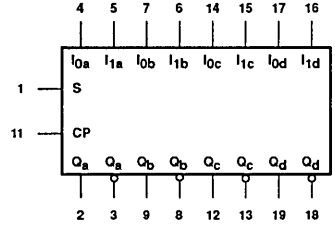
54F398



For LLCC pin assignments, see JEDEC Standard No. 2

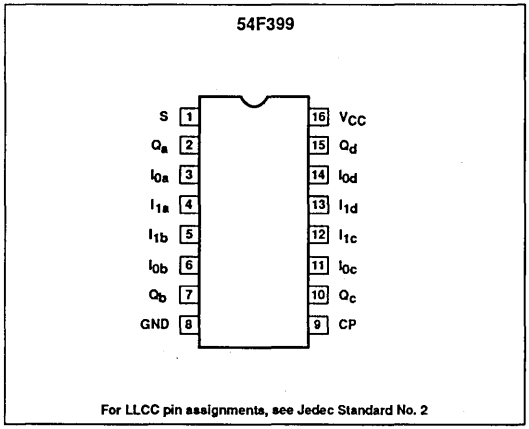
LOGIC SYMBOL

54F398

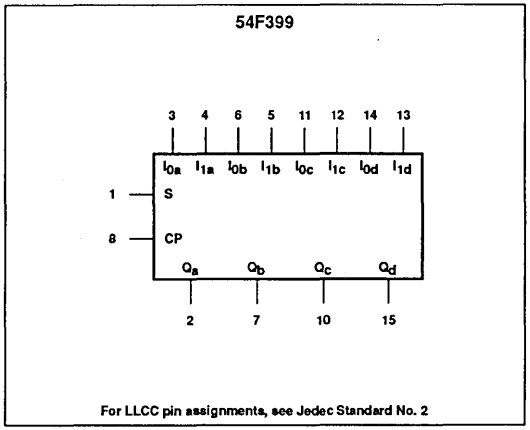


For LLCC pin assignments, see JEDEC Standard No. 2

PIN CONFIGURATION



LOGIC SYMBOL



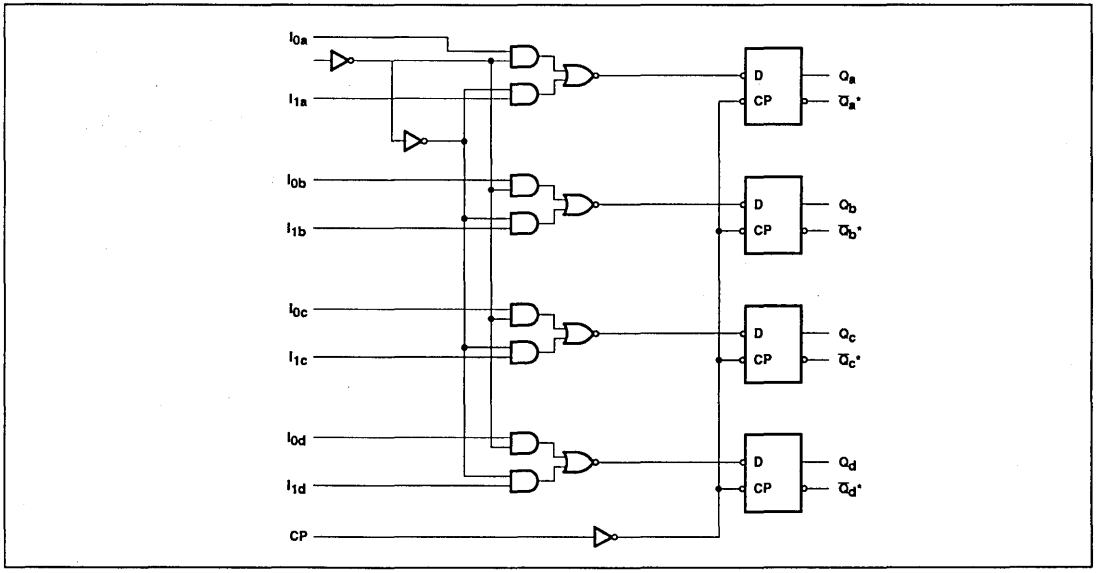
The 54F398 and 54F399 are high-speed quad 2-port registers. They select 4 bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the Low-to-High transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a set-up time prior to and hold time after the Low-to-High transition of the Clock input for predictable operation. The 54F398 has both Q and $\overline{Q}$ outputs.

FUNCTION TABLE

INPUTS			OUTPUTS	
S	I_0	I_1	Q	$\overline{Q}$*
l	l	X	L	H
l	h	X	H	L
h	X	l	L	H
h	X	h	H	L

*54F398 only
l = Low voltage level one setup time prior to Low-to-High clock transition
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
H = High voltage level
X = Don't care

LOGIC DIAGRAM (54F398 only)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OH} = Max, V_{IH} = Min	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current[4] (total)	54F398	V_{CC} = Max		25	38	mA
		54F399			22	34	mA

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

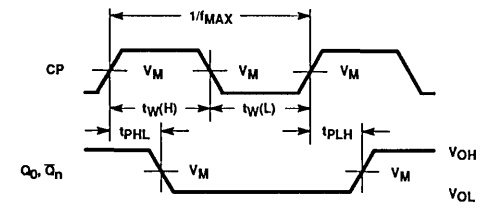
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	120		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q or $\overline{Q}$	Waveform 1	3.0 3.0	5.7 6.5	7.5 8.5	3.0 3.0	9.5 10.5	ns ns

AC SETUP REQUIREMENTS

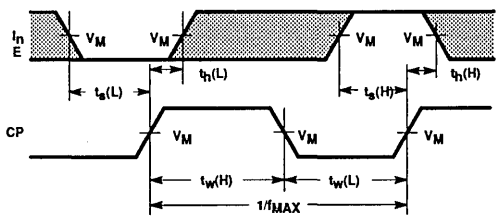
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time, High or Low I_n to CP	Waveform 2	3.0 3.0			4.5 4.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I_n to CP	Waveform 2	1..0 1.0			1.5 1.5		ns ns
$t_s(H)$ $t_s(L)$	Set-up time, High or Low S to CP	Waveform 2	7.5 7.5			10.5 10.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S to CP	Waveform 2	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	4.0 6.0			4.0 7.0		ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS} the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests I_{OS} tests should be performed last.
4. V_{IN} = High; apply 3V, 0V, 3V to CP then make measurement.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



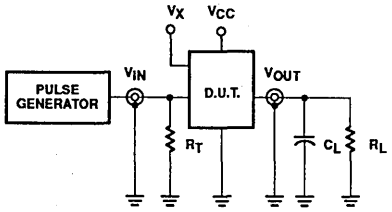
Waveform 1. Clock to Output Delays and Clock Pulse Width



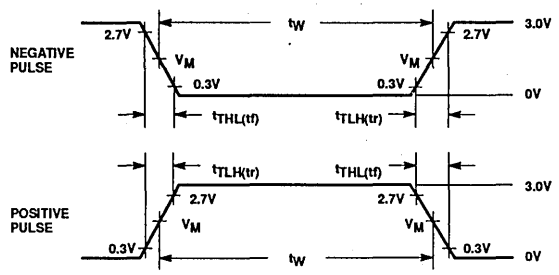
Waveform 2. Data Setup and Hold Times

NOTE: For all waveforms V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F432
Latch

Multi-Mode Buffered Latch, INV (3-State)

Product Specification

FEATURES

- **Status flip-flop for interrupt commands**
- **Asynchronous or latched receiver mode**
- **Inverting**
- **3-State outputs**
- **300mil-wide Slim DIP package**
- **Functional equivalent to Intel 8212 except that 54F432 has inverting outputs**

DESCRIPTION

The 54F432 has 8 data latches with 3-State output buffers. Also included is a status flip-flop for providing service-busy or request-interrupt commands. Separate Mode (M) and Select ($\overline{S}_0$, S_1) inputs allow data to be stored with the outputs enabled or disabled. The device can also be operated in a fully transparent mode.

This device is functionally equivalent to the Intel 8212 except that the 54F432 has inverting outputs.

ORDERING INFORMATION

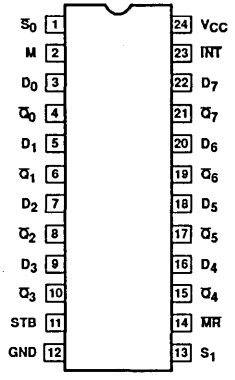
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54F432/BLA
24-Pin Ceramic FlatPack	54F432/BKA
28-Pin Ceramic LLCC	54F432/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20µA/0.6mA
$\overline{S}_0$, S_1	Select inputs	1.0/1.0	20µA/0.6mA
STB	Strobe input	1.0/1.0	20µA/0.6mA
M	Mode Control input	1.0/1.0	20µA/0.6mA
$\overline{MR}$	Master Reset input	1.0/1.0	20µA/0.6mA
$\overline{INT}$	Interrupt output	50/33	1.0mA/20mA
Q_0 - Q_7	Data latched outputs	150/33	3.0mA/20mA

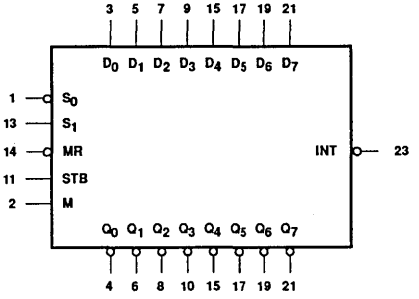
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



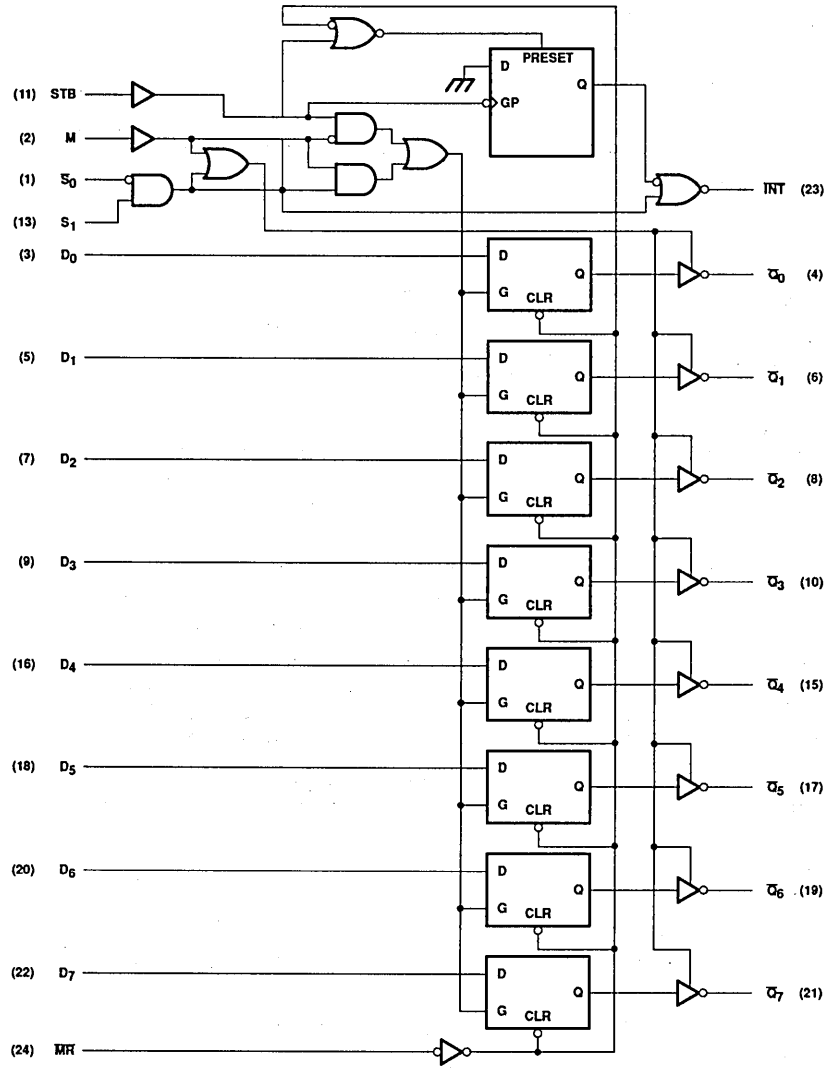
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC Pin Assignment, see JEDEC Standard No. 2

Latch | 54F432

FUNCTIONAL DESCRIPTION

This high-performance eight-bit parallel expandable buffer register incorporates mode selection inputs and an edge-trigger status flip-flop designed specifically for implementing bus organized input/output ports. The 3-State data outputs can be connected to a common data bus and controlled from the appropriate select inputs to receive or transmit data. An integral status flip-flop provides busy or request interrupt commands.

The eight data latches are fully transparent when the internal gate enable input, G, is High and the outputs are enabled. Latch transparency is selected by the mode control (M), select ($\overline{S}_0$ and S_1), and the strobe (STB) inputs and during transparency each data output (Q_n) follows its respective data input (D_n). This mode of operation can be terminated by clearing, deselecting, or holding the data latches.

An input mode or an output mode is selectable from the M input. In the input mode, M=L, the eight data latch inputs are enabled when the strobe is High regardless of device selection. If selected during an input mode, the outputs will follow the data inputs. When the strobe input is taken Low, the latches will store the most recently set up data.

In the output mode, M=H, the output buffers are enabled regardless of any other control input. During the output mode the content of the register is under control of the select ($\overline{S}_0$ and S_1) inputs. See the Data Latches Function Table.

STATUS FLIP-FLOP FUNCTION TABLE

INPUTS				OUTPUT
$\overline{MR}$	$\overline{S}_0$	S_1	STB	$\overline{INT}$
L	H	X	X	H
L	X	L	X	H
H	X	X	↓	L
H	L	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low clock transition

DATA LATCHES FUNCTION TABLE

INPUTS					DATA IN	DATA OUT	OPERATING MODE
$\overline{MR}$	M	$\overline{S}_0$	S_1	STB			
L	H	H	X	X	X	H	Clear
L	L	L	H	L	X	H	
X	L	X	L	X	X	Z	De-select
X	L	H	X	X	X	Z	
H	H	H	X	X	X	$\overline{Q}_0$	Hold
H	L	L	H	L	X	$\overline{Q}_0$	
H	H	L	H	X	L	H	Data Bus
H	H	L	H	X	H	L	
H	L	L	H	H	L	H	Data Bus
H	L	L	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_I	Input voltage range		-0.5 to +7.0	V
I_I	Input current range		-30 to +5	mA
V_O	Voltage applied to output in High output state range		-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	$\overline{INT}$	40	mA
		Q_0 - Q_7	40	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{INT}$			-1.0	mA
		Q_0, Q_7			-3.0	mA
I_{OL}	Low-level output current	$\overline{INT}$			20	mA
		Q_0, Q_7			20	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max,	I_{OH} = -1mA	2.5			V
		V_{IH} = Min	I_{OH} = -3mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max	±10% V_{CC}		.35	.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH}	High-level input current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OZH}	Off-state output current High-level voltage applied	V_{CC} = Max, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current Low-level voltage applied	V_{CC} = Max, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max, V_O = 0.0V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max		40	55	mA
		I_{CCL}			50	70	mA
		I_{CCZ}			50	65	mA

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 2	4.5 2.5	7.5 4.5	10.5 7.0	4.0 2.5	13.0 6.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$, S_1 or STB to Q_n	Waveform 1, 2	8.5 6.0	14.0 9.5	17.0 13.0	8.0 5.5	24.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_0$ or S_1 to $\overline{INT}$	Waveform 1, 2	3.0 3.5	6.0 6.5	9.5 10.0	2.5 3.0	10.5 10.5	ns ns
t_{PLH}	Propagation delay $\overline{MP}$ to Q_n	Waveform 2	8.0	12.0	16.0	7.5	18.5	ns
t_{PHL}	Propagation delay STB to $\overline{INT}$	Waveform 2	7.0	10.0	13.5	6.5	14.5	ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{S}_0$ or S_1 to Q_n	Waveform 5 Waveform 6	6.0 6.0	9.0 11.0	12.5 14.0	5.5 5.5	15.5 15.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level $\overline{S}_0$ or S_1 to Q_n	Waveform 5 Waveform 6	4.0 6.0	7.5 11.5	11.5 15.0	3.5 5.5	12.5 17.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level M to Q_n	Waveform 5 Waveform 6	5.0 6.0	7.5 8.0	11.0 11.5	4.5 5.5	12.0 13.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level M to Q_n	Waveform 5 Waveform 6	3.5 6.0	6.0 10.0	9.5 13.0	3.0 5.5	10.5 15.0	ns ns

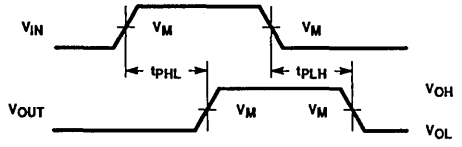
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to $\overline{S}_0$, S_1, STB or M	Waveform 3	0 0			1.0 1.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to $\overline{S}_0$, S_1, STB or M	Waveform 3	9.0 8.0			9.5 9.5		ns ns
$t_w(H)$ $t_w(L)$	$\overline{S}_0$, S_1 or STB Pulse width High or Low	Waveform 3	8.0 8.0			9.0 9.0		ns ns
$t_w(L)$	$\overline{MR}$ Pulse width	Waveform 4	8.0			9.0		ns
t_{rec}	Recovery time	Waveform 4	0			0		ns

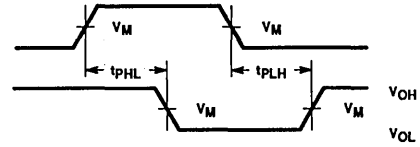
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

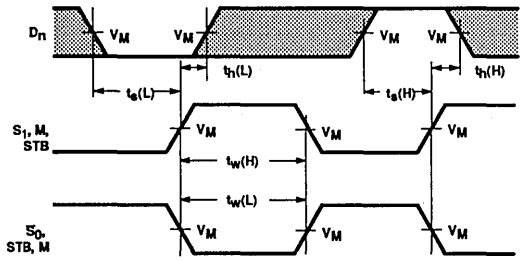
AC WAVEFORMS



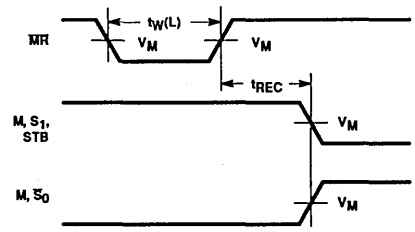
Waveform 1. Propagation Delay for Non-Inverting Outputs



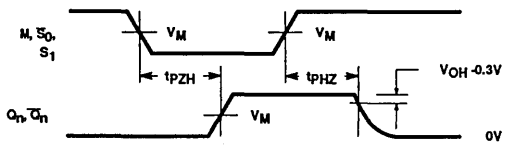
Waveform 2. Propagation Delay for Inverting Outputs



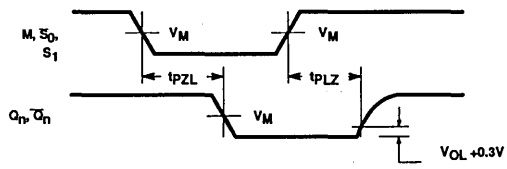
Waveform 3. Setup and Hold Times



Waveform 4. Recovery Times



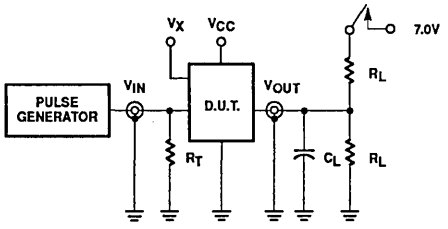
Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



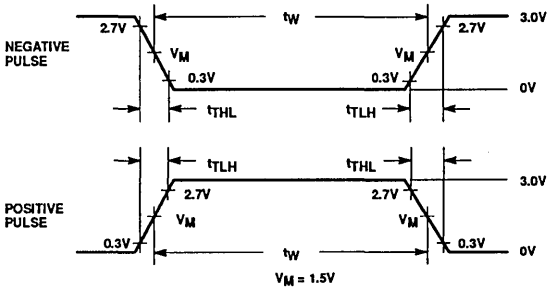
Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

54F455, 54F456
Buffers/Drivers

54F455 Octal Buffer/Line Driver with Parity, Inverting (3-State)
54F456 Octal Buffer/Line Driver with Parity, Non-Inverting (3-State)

Military Logic Products

Product Specification

FEATURES

- High impedance NPN base inputs for reduced loading (20μA in High and Low states)
- 54F455 combines 54F240 and 54F280A functions in one package
- 54F456 combines 54F241 and 54F280A functions in one package
- 54F455A and 54F456A are center pin versions of the 54F655A and 54F656A respectively
- 54F455 Inverting
  54F456 Non-Inverting
- 3-State outputs sink 48mA and source 12mA
- 24-pin slim DIP (300 mil) package
- Inputs on one side and outputs on the other side simplify PC board layout
- Center power and ground to reduce ground bounce and system noise

DESCRIPTION

The 54F455 and 54F456 are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

ORDERING INFORMATION

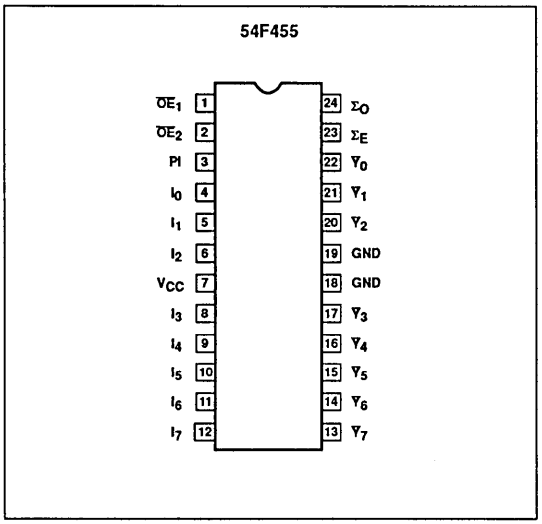
DESCRIPTION	ORDER CODE
Ceramic DIP	54F455/BLA 54F456/BLA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

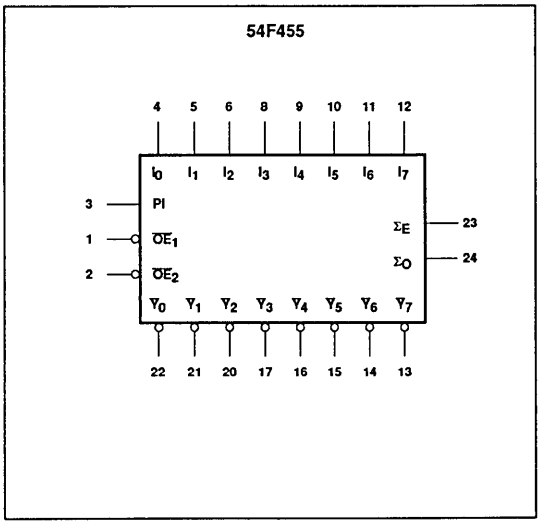
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_n	Data inputs	1.0/0.033	20μA/20μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_1$, $\overline{OE}_2$	3-State output enable inputs (active Low)	1.0/0.033	20μA/20μA
$\overline{Y}_n$	Data outputs ((54F455)	600/80	12mA/48mA
Y_n	Data outputs (54F456)	600/80	12mA/48mA
Σ_E, Σ_O	Parity outputs	600/80	12mA/48mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High State and 0.6mA in the Low state.

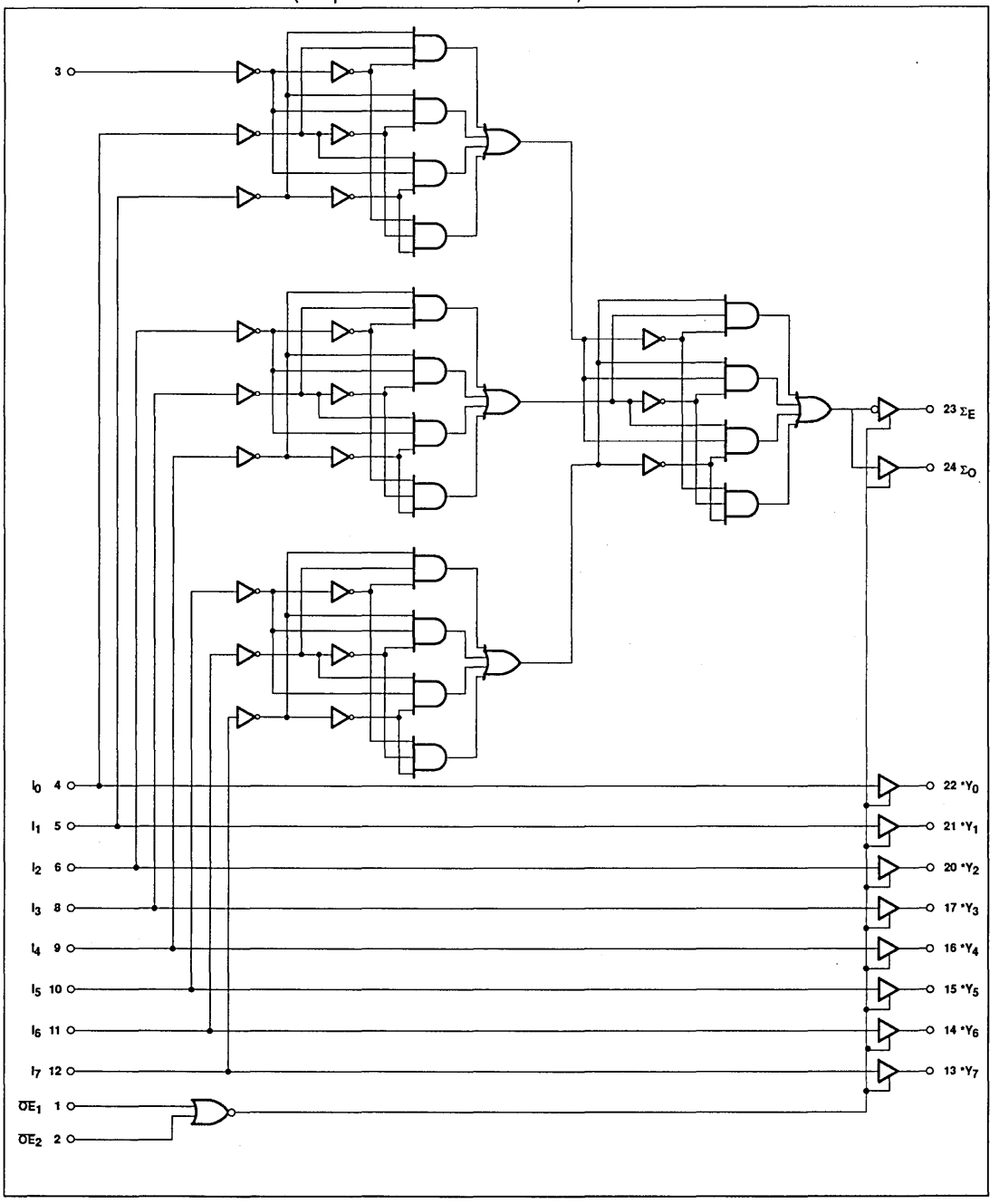
PIN CONFIGURATION



LOGIC SYMBOL

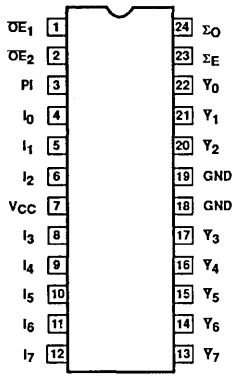


LOGIC DIAGRAM FOR 54F456 (*outputs are inverted for 54F455)



PIN CONFIGURATION

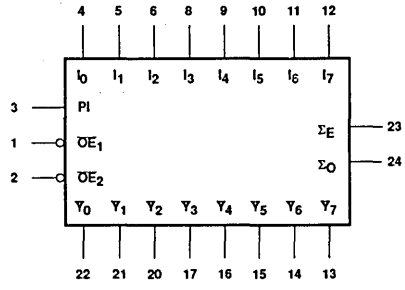
54F456



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

54F456



For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLES

INPUTS			DATA OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I_N	54F455	54F456
L	L	L	H	L
L	L	H	L	H
H	X	X	(Z)	(Z)
X	H	X	(Z)	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance level

INPUTS	PARITY OUTPUTS	
Number of inputs, High (PI, I_0 - I_7)	Σ_E	Σ_O
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = High	Z	Z

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-1	mA
I_{OH2}	High-level output current			-3	mA
I_{OH3}	High-level output current			-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

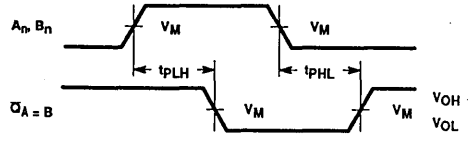
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH2} = -3mA	2.4			V
				I_{OH1} = -1mA	2.5			V
				I_{OH3} = -12mA	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = 48mA			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V				-20	µA
I_{OZH}	Off-state current High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				50	µA
I_{OZL}	Off-state current Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			50	80	mA
		I_{CCL}				78	110	mA
		I_{CCZ}				63	90	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

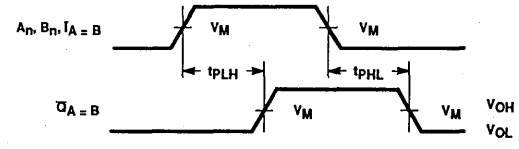
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n (54F455)	Waveform 1	2.0 1.0	4.5 2.0	6.5 4.0	2.0 1.0	8.0 5.5	ns ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n (54F456)	Waveform 2	2.0 2.5	4.5 5.0	6.5 7.0	2.0 2.5	7.5 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E, Σ_O	Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.5 5.5	15.0 18.0	ns ns
t_{PZH} t_{PZL}	Enable time to High level Enable time to Low level	Waveform 3 Waveform 4	4.0 4.5	7.0 8.0	9.5 10.5	3.0 4.5	11.5 13.5	ns ns
t_{PLH} t_{PHL}	Disable time from High level Disable time from Low level	Waveform 3 Waveform 4	1.5 2.0	4.0 5.0	6.5 7.5	1.5 2.0	8.0 9.0	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

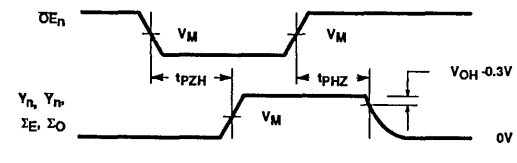
AC WAVEFORMS



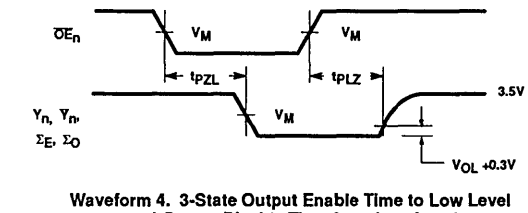
Waveform 1. Propagation Delay for I_n to Σ_E, Σ_O, Y_n



Waveform 2. Propagation Delay for I_n to Σ_E, Σ_O, Y_n



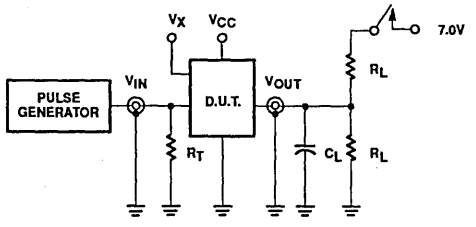
Waveform 3. 3-State Output Enable time to High level and Output Disable time from High level



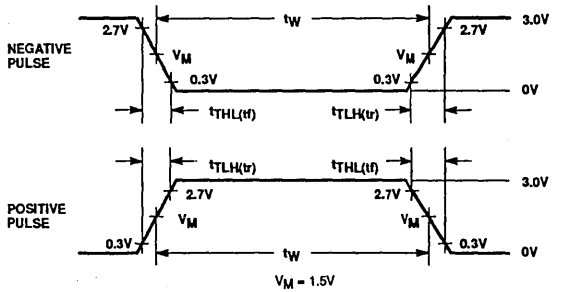
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

54F521
Comparator

8-Bit Identity Comparator

Product Specification

Military FAST Products

FEATURES

- **Compares two 8-bit words in 6.5ns typical**
- **Expandable to any word length**

DESCRIPTION

The 54F521 is an expandable 8-bit comparator. It compares two words of up to 8 bits each and provides a Low output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active-Low enable input.

ORDERING INFORMATION

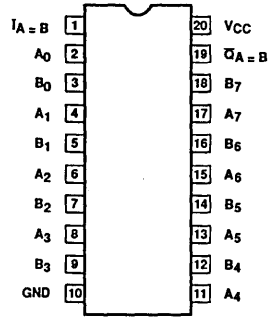
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F521/BRA
20-Pin Ceramic FlatPack	54F521/BSA
20-Pin Ceramic LLCC	54F521/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$A_0 - A_7$	Word A inputs	1.0/1.0	20μA/0.6mA
$B_0 - B_7$	Word B inputs	1.0/1.0	20μA/0.6mA
$\overline{I}_{A=B}$	Expansion or enable input (active Low)	1.0/1.0	20μA/0.6mA
$\overline{O}_{A=B}$	Identity output (active Low)	50/33	1.0mA/20mA

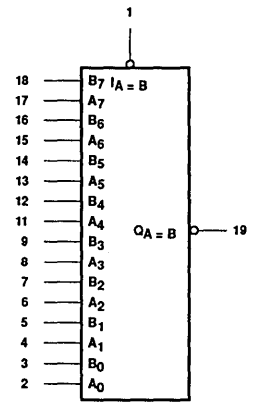
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

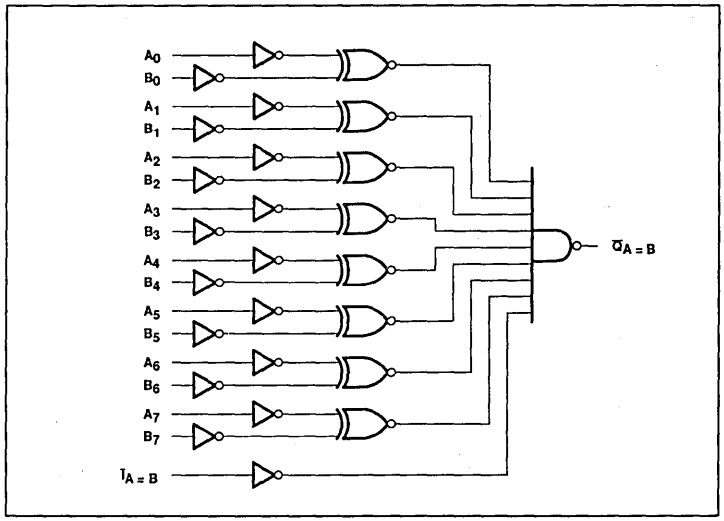
Comparator | 54F521

TRUTH TABLE

INPUTS		OUTPUT
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

H = High voltage level
L = Low voltage level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V		1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V	-60	-90	-150	mA
I_{CC}	Supply current[4] (total)	I_{CCH}	V_{CC} = Max		24	36	mA
		I_{CCL}			15.5	23	mA

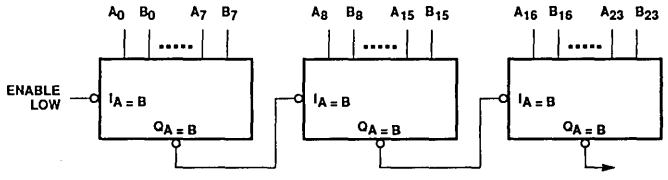
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n or B_n to $\overline{Q}_{A=B}$	Waveform 1, 2	3.5 2.5	8.0 8.0	9.5 9.0	3.5 2.5	20.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ to $\overline{Q}_{A=B}$	Waveform 2	3.0 3.5	5.0 6.5	6.5 7.0	3.0 3.5	12.0 9.0	ns ns

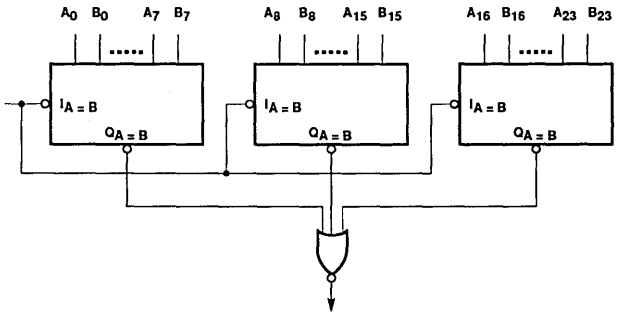
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS} the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests I_{OS} tests should be performed last.
4. For I_{CCH} all inputs are grounded except B_0 can be any one input, which is at ≥ 4.0V. For I_{CCL} all inputs are grounded.

APPLICATION DIAGRAMS

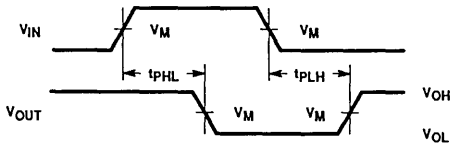


Ripple Expansion

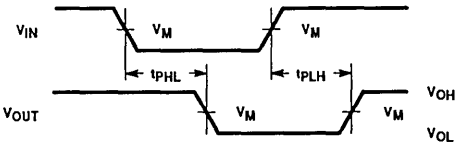


Parallel Expansion

AC WAVEFORMS



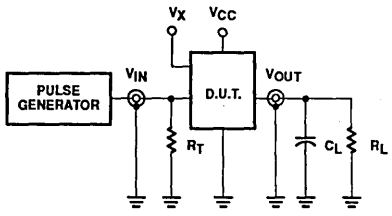
Waveform 1. Waveform for Inverting Outputs



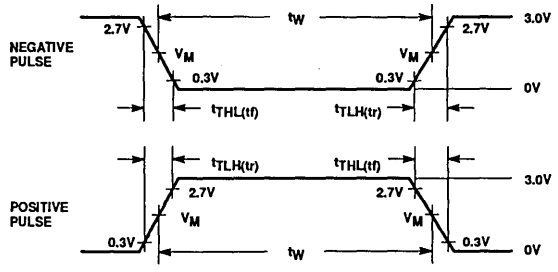
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

54F534
Latch/Flip-Flop

54F534 Octal D Flip-Flop (3-State)

Product Specification

Military Logic Products

FEATURES

- **8-bit positive edge-triggered register**
- **3-State inverting output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

DESCRIPTION

The 54F534 is an 8-bit edge-triggered register coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause the clocking operation.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{CE}$ is Low, data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

ORDERING INFORMATION

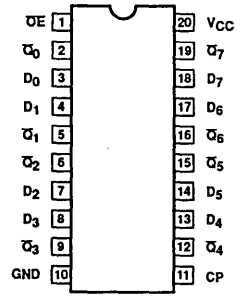
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F534/BRA
20-Pin Ceramic FlatPack	54F534/BSA
20-Pin Ceramic LLCC	54F534/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{O}_0$ - $\overline{O}_7$	3-State outputs	150/33	3mA/20mA

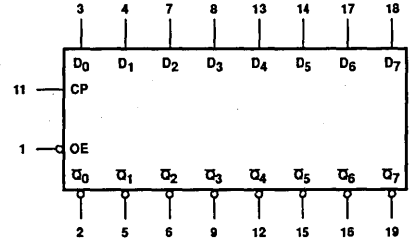
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

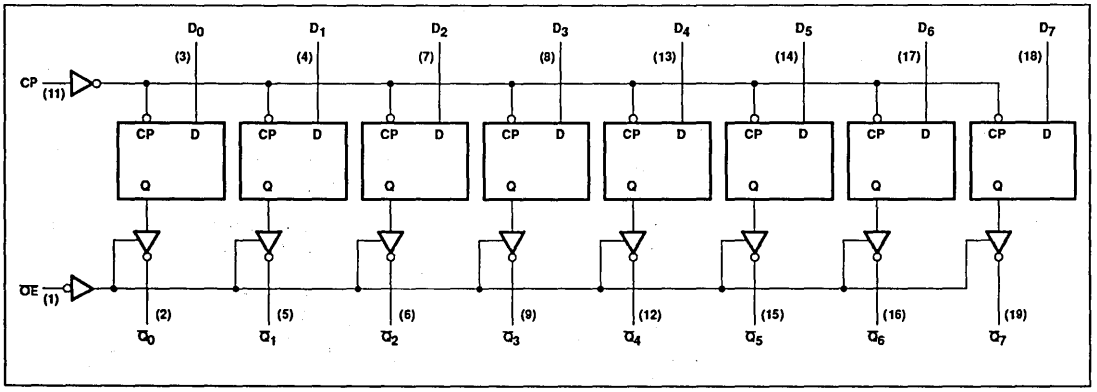
LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

Latch/Flip-Flop 54F534

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		$\overline{O}_0 - \overline{O}_7$
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High Clock transition or High-to-Low $\overline{OE}$ transition
L = Low voltage level
X = Don't Care.
l = Low voltage level one setup time prior to the Low-to-High Clock transition or High-to-Low CP transition
(Z) = High impedance "off" state
↑ = Low-to-High Clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage[5]	2.0			V
V_{IL}	Low-level input voltage[5]			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH2}	High-level output current			-3.0	mA
I_{OH1}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Max,	I_{OH2} = -3mA	2.4			V
		V_{IH} = Min	I_{OH1} = -1mA	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max, V_O = 0.0V		-60	-90	-150	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			55	86	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

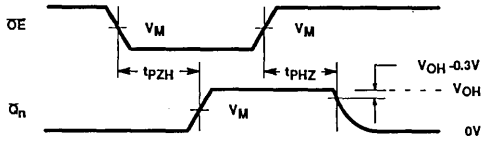
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 3	100			60		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{O}_n$	Waveform 3	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.5 11.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 1 Waveform 2	2.0 2.0	9.0 5.8	11.5 7.5	2.0 2.0	14.0 10.0	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 1 Waveform 2	2.0 2.0	5.3 4.3	7.0 5.5	2.0 2.0	8.0 7.5	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CCZ} with $\overline{OE}$ inputs ≥ 4.0V and D_n inputs at ground and all outputs open.
5. When testing devices to the Functional Table specified, refer to the "Recommended Operating Conditions" section of the Application Note 202, "Testing and Specifying FAST Logic."

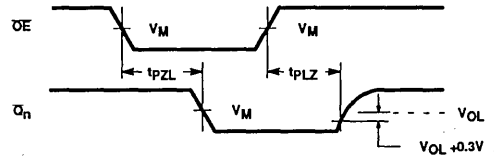
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, D_n to CP	Waveform 4	2.0 2.0			2.0 2.0		ns ns
t_h(H) t_h(L)	Hold time, D_n to CP	Waveform 4	2.0 2.0			2.0 2.0		ns ns
t_w(H) t_w(L)	CP pulse width, High or Low	Waveform 3	7.0 6.0			7.0 6.0		ns ns

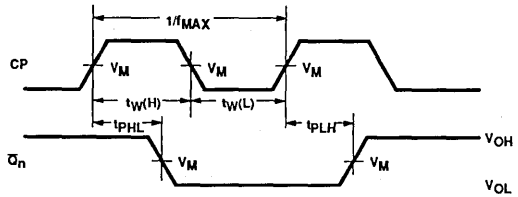
AC WAVEFORMS



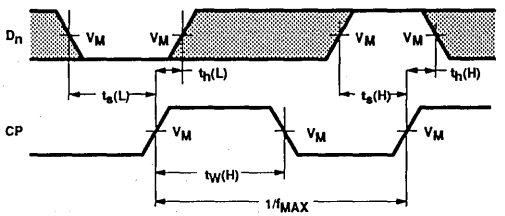
Waveform 1. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



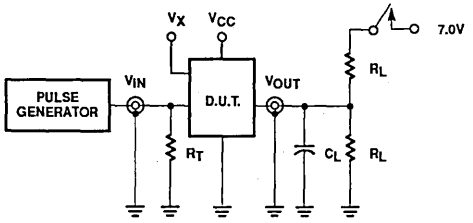
Waveform 3. Clock to Output Delays and Clock Pulse Width



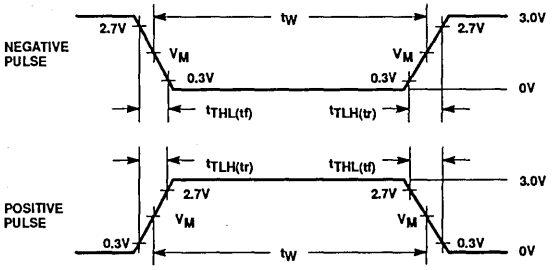
Waveform 4. Data Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All others	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	t_W	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per Function Table.

Signetics

54F538
Decoder

1-of-8 Decoder (3-State)

Product Specification

Military Logic Product

DESCRIPTION

The 54F538 decoder/demultiplexer accepts three address (A_0 - A_3) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control (P) input determines whether the outputs are active Low or active High. The 54F538 has 3-State outputs and a High signal on the Output Enables ($\overline{OE}n$) will force all outputs to the high impedance state. Two active High and two active Low Enable inputs are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

ORDERING INFORMATION

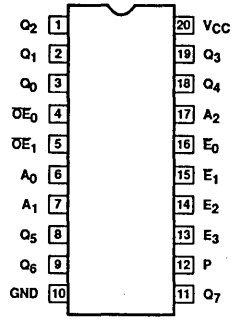
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F538/BRA
20-Pin Ceramic FlatPack	54F538/BSA
20-Pin Ceramic LLCC	54F538/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_2	Address inputs	1.0/1.0	20μA/0.6mA
E_0, E_1	Enable input (Active Low)	1.0/1.0	20μA/0.6mA
E_2, E_3	Enable input (Active High)	1.0/1.0	20μA/0.6mA
P	Polarity control input	1.0/1.0	20μA/0.6mA
$\overline{OE}_0$, $\overline{OE}_1$	Output enable input (Active Low)	1.0/1.0	20μA/0.6mA
Q_0 - Q_7	Data outputs	150/33	3.0mA/20mA

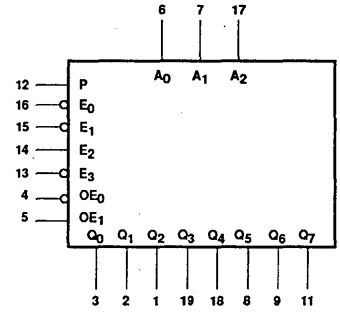
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

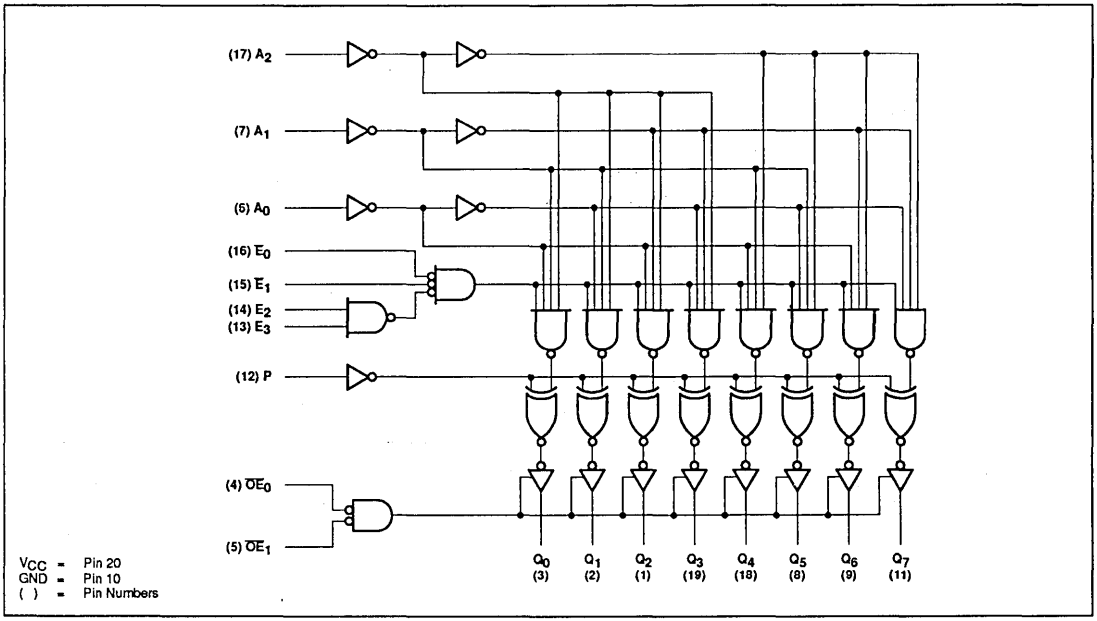


VCC = Pin 20
GND = Pin 10

For LLCC pin assignments, see JEDEC Standard No. 2

Decoder | 54F538

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS								OPERATING MODE
$\overline{OE}_0$	$\overline{OE}_1$	$\overline{E}_0$	$\overline{E}_1$	E_2	E_3	A_2	A_1	A_0	Q_0	Q_1	Q2	Q3	Q4	Q5	Q6	Q7	
H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	High Impedance
X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	
L	L	H	X	X	X	X	X	X	Outputs equal P input								Disable
L	L	X	H	X	X	X	X	X									
L	L	X	X	L	X	X	X	X									
L	L	X	X	X	L	X	X	X									
L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L	Active High output (P = L)
L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L	
L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L	
L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L	
L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L	
L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L	
L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L	
L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H	
L	L	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	Active Low output (P = H)
L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H	
L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	
L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	48	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	ma
I_{OH1}	High-level output current			-1.0	mA
I_{OH2}	High-level output current			-3.0	mA
I_{OL}	Low-level output current			20.0	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

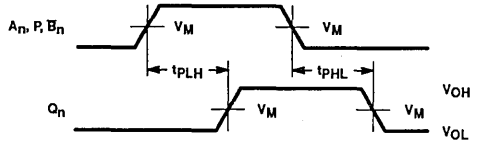
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max,	I_{OH1} = -1.0mA	2.5			V
			V_{IH} = Min	I_{OH2} = -3.0mA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state current High-level voltage applied		V_{CC} = Max, V_O = 2.7V				50	µA
I_{OZL}	Off-state current Low-level voltage applied		V_{CC} = Max, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-60		-150	mA
I_{CC}	Supply current	I_{CCH}	V_{CC} = Max			30	40	mA
		I_{CCL}				35	50	mA
		I_{CCZ}				35	50	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic.")

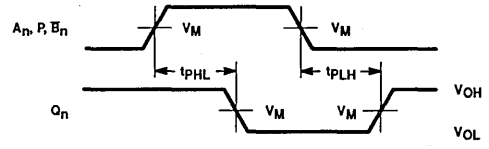
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Q_n	Waveform 1, 2	5.5 3.0	6.5 7.5	13.0 12.5	5.0 3.0	14.0 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_0$ or $\overline{E}_1$ to Q_n	Waveform 1, 2	5.5 3.0	8.5 7.5	12.0 12.0	5.0 3.0	13.0 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_2$ or $\overline{E}_3$ to Q_n	Waveform 1, 2	6.5 4.0	9.0 7.0	12.5 12.5	5.5 3.5	13.5 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay P to Q_n	Waveform 1, 2	4.5 3.5	9.5 6.5	15.0 10.0	4.0 3.5	16.5 10.5	ns ns
t_{PZL} t_{PZL}	Output Enable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	2.5 6.5	5.5 9.5	9.5 13.5	2.0 6.0	11.0 15.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}_0$ or $\overline{OE}_1$ to Q_n	Waveform 3 Waveform 4	1.0 1.0	3.0 3.5	6.0 8.5	1.0 1.0	7.0 9.5	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value under the recommended operating conditions for the applicable conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

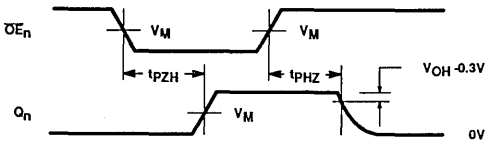
AC WAVEFORMS



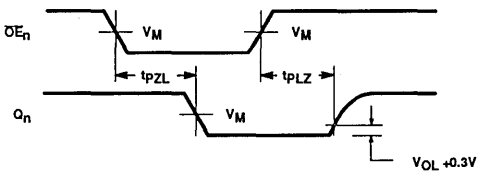
Waveform 1. Propagation Delay for Non-Inverting Outputs



Waveform 2. Propagation Delay for Inverting Outputs



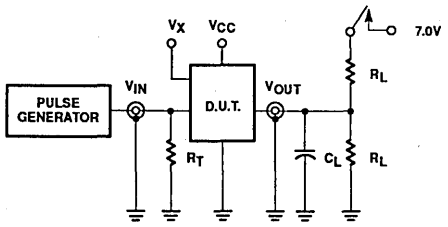
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



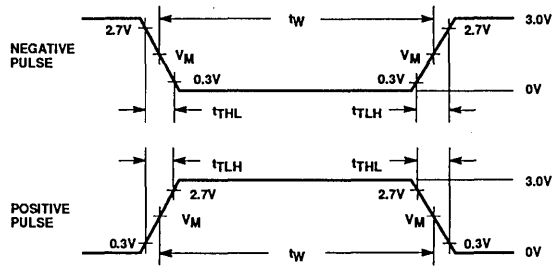
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

Military Logic Products

54F543, 54F544
Transceiver

54F543 Non-Inverting Octal Registered Transceiver (3-State)
54F544 Inverting Octal Registered Transceiver (3-State)

Product Specification

FEATURES

- **Combines 54F245 and 54F373 type functions in one chip**
- **8-bit octal transceiver with D-type latch**
- **54F543 Non-inverting**
  54F455 Inverting
- **Back-to-back Registers for storage**
- **Separate controls for data flow in each direction**
- **A outputs sink 20mA and source 3mA**
- **B outptus sink 48 mA and source 12mA**
- **300 mil wide 24-pin Slim DIP**
- **3-State outputs for bus-oriented applications**

DESCRIPTION

The 54F543 and 54F544 Octal Registered Transceivers contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enables ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enables ($\overline{OEAB}$, $\overline{OEBA}$) are provided for each register to permit independent control of inputting and outputting in either direction. While the 54F543 has non-inverting data path, the 54F544 inverts data in both directions. The A outputs are guaranteed to sink 20mA, while the B outputs are rated for 48mA.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54F543/BLA 54F544/BLA
Ceramic Flat Pack	54F543/BKA 54F544/BKA
Ceramic LLCC	54F543/B3A 54F544/B3A

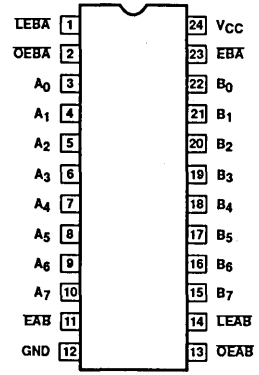
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7 (54F543)	Port A, 3-State inputs	3.5/1.0	70μA/0.6mA
B_0 - B_7 (54F543)	Port B, 3-State inputs	3.5/1.0	70μA/0.6mA
$\overline{A}_0$ - $\overline{A}_7$ (54F544)	Port $\overline{A}$, 3-State inputs	3.5/1.0	70μA/0.6mA
$\overline{B}_0$ - $\overline{B}_7$ (54F544)	Port $\overline{B}$, 3-State inputs	3.5/1.0	70μA/0.6mA
$\overline{OEAB}$	A-to-B Output Enable input (Active Low)	1.0/1.0	20μA/0.6mA
$\overline{OEBA}$	A-to-B Output Enable input (Active Low)	1.0/1.0	20μA/0.6mA
$\overline{EAB}$	A-to-B Enable input (Active Low)	1.0/2.0	20μA/1.2mA
$\overline{EBA}$	A-to-B Enable input (Active Low)	1.0/2.0	20μA/1.2mA
$\overline{LEAB}$	A-to-B Latch Enable input (Active Low)	1.0/1.0	20μA/0.6mA
$\overline{LEBA}$	A-to-B Latch Enable input (Active Low)	1.0/1.0	20μA/0.6mA
A_0 - A_7 (54F543)	Port A, 3-State outpus	150/33	3.0mA/20mA
B_0 - B_7 (54F543)	Port B, 3-State outputs	600/80	12mA/48mA
$\overline{A}_0$ - $\overline{A}_7$ (54F544)	Port $\overline{A}$, 3-State outputs	150/33	3.0mA/20mA
$\overline{B}_0$ - $\overline{B}_7$ (54F544)	Port $\overline{B}$, 3-State outputs	600/80	12mA/48mA

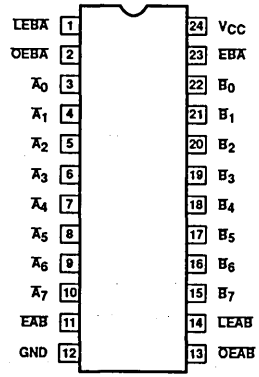
NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High State and 0.6mA in the Low state.

PIN CONFIGURATION

54F543

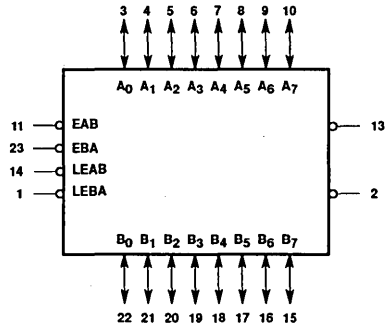


54F544



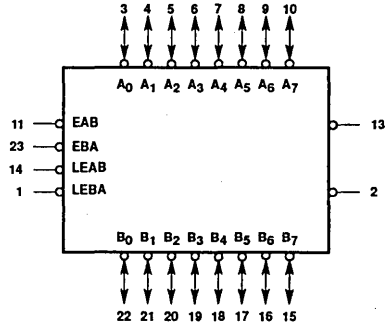
LOGIC SYMBOL

54F543



VCC = Pin 24
GND = Pin 12

54F544



VCC = Pin 24
GND = Pin 12

FUNCTIONAL DESCRIPTION

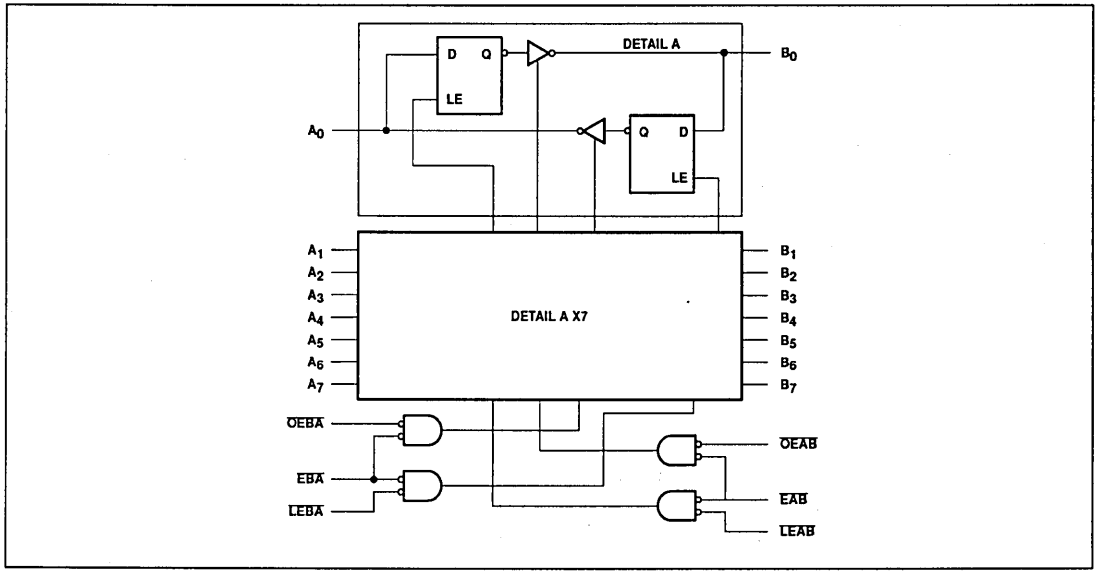
The 54F543 and 54F544 contain two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) input must be Low in order to enter data from A_0 - A_7 or take data from B_0 - B_7,, as indicated in the Function Table. With $\overline{EAB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent Low-to-High transition for the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-State B output buffers are active and reflect the data present at the outputs of the A latches. Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

FUNCTION TABLE

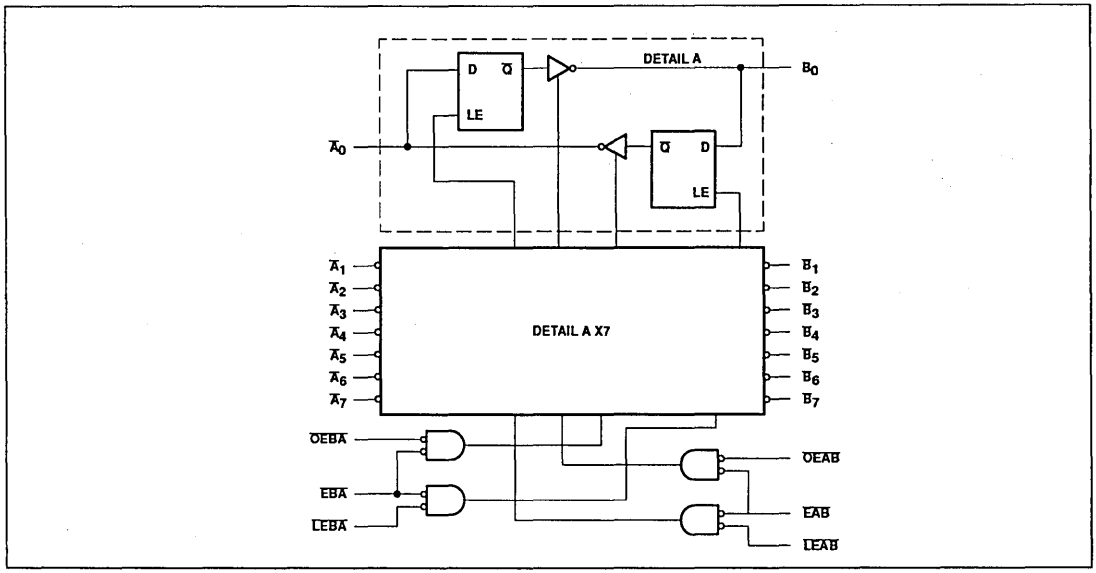
INPUTS				OUTPUTS		STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	DATA	54F543	54F544	
H	X	X	X	Z	Z	Disabled
X	H	X	X	Z	Z	Disabled
L	↑	L	h	Z	Z	Disable + Latch
L	↑	L	l	Z	Z	Disable + Latch
L	L	↑	h	H	L	Latch + Display
	L	↑	l	L	H	Disable + Latch
L	L	H	X	NC	NC	Hold

H = High voltage level
L = Low voltage level
h = High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ = Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$
X = Don't care
NC = No change
Z = High impedance state

LOGIC DIAGRAM FOR 54F543



LOGIC DIAGRAM FOR 54F544



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_I	Input voltage		-0.5 to +7.0	V
I_I	Input current		-30 to +5	mA
V_O	Voltage applied to output in High output state range		-0.5 to +5.5	V
I_O	Current applied to output in Low output state	A_0 - A_7, $\overline{A}_0$ - $\overline{A}_7$	40	mA
		B_0 - B_7, $\overline{B}_0$ - $\overline{B}_7$	96	mA
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH1}	High-level output current				-1	mA
I_{OH2}	High-level output current				-3	mA
I_{OH3}	High-level output current	B_0 - B_7, $\overline{B}_0$ - $\overline{B}_7$			-12	mA
I_{OL}	Low-level output current	A_0 - A_7, $\overline{A}_0$ - $\overline{A}_7$			20	V
		B_0 - B_7, $\overline{B}_0$ - $\overline{B}_7$			48	V
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output to voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH2} = -3mA	2.4			V
				I_{OH1} = -1mA	2.5			V
				I_{OH} = -12mA B_0 - B_7 and $\overline{B}_0$ - $\overline{B}_7$ only	2.0			V
V_{OL}	Low-level output voltage	A_0 - A_7, $\overline{A}_0$ - $\overline{A}_7$	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 20mA		.35	50	V
		B_0 - B_7, B_0 - $\overline{B}_7$		I_{OL} = 48mA		.35	50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I - I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input	$\overline{OEAB}$, $\overline{OEBA}$, $\overline{EAB}$ $\overline{EBA}$, $\overline{LEAB}$, $\overline{LEBA}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		others	V_{CC} = 5.5V, V_I = 5.5V				1.0	mA
I_{IH}	High-level input current		V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	others	V_{CC} = Max, V_I = 0.5V				-0.6	mA
		$\overline{EAB}$, $\overline{EBA}$					-1.2	mA
I_{IH} + I_{OZH}	Off-state current High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_I = 2.7V				70	µA
I_{IL} + I_{OZL}	Off-state current Low level voltage applied		V_{CC} = Max, V_{IH} = Min, V_I = 0.5V				-600	µA
I_{OS}	Short-circuit output current[3]	A_0 - A_7, $\overline{A}_0$ - $\overline{A}_7$	V_{CC} = Max		-60		-150	mA
		B_0 - B_7, $\overline{B}_0$ - $\overline{B}_7$			-100		-225	mA
I_{CC}	Supply current (total)	54F543	V_{CC} = Max	I_{CCH}		67	100	mA
				I_{CCL}		83	125	mA
				I_{CCZ}		83	125	mA
		54F544		I_{CCH}		80	110	mA
				I_{CCL}		105	140	mA
				I_{CCZ}		100	135	mA

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	54F543 LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	3.5 3.0	5.5 5.0	8.5 8.0	3.0 2.5	10.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.0 2.5	4.0 4.5	7.0 7.5	1.5 2.5	8.5 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEBA}$ to A_n	Waveform 1, 2	5.0 4.0	7.0 6.0	10.0 9.0	4.5 4.0	12.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LEAB}$ to B_n	Waveform 1, 2	6.0 4.5	8.5 5.5	11.5 9.5	5.5 4.0	14.0 11.0	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 4 Waveform 5	2.0 3.5	4.0 5.0	7.5 9.5	1.5 3.0	9.0 11.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n	Waveform 4 Waveform 5	1.0 1.5	3.0 4.0	6.5 8.5	1.0 1.0	8.5 9.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ or $\overline{EAB}$ to A_n or B_n	Waveform 4 Waveform 5	4.5 5.5	7.0 7.5	10.5 11.0	4.0 5.0	13.0 13.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ or $\overline{EAB}$ to A_n or B_n	Waveform 4 Waveform 5	2.5 2.0	5.0 7.0	8.5 11.0	2.0 1.5	10.5 13.0	ns ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	54F543 LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to $\overline{LEAB}$ or $\overline{LEBA}$ A_n or B_n to $\overline{EAB}$ or $\overline{EBA}$	Waveform 3	3.0 3.5			3.0 3.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to $\overline{LEAB}$ or $\overline{LEBA}$ A_n or B_n to $\overline{EAB}$ or $\overline{EBA}$	Waveform 3	3.0 3.0			3.0 3.0		ns ns
$t_w(L)$	Latch enable pulse width	Waveform 3	4.0			4.5		ns

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	54F544 LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation dealy A_n to B_n or $\overline{B}_n$ to $\overline{A}_n$	Waveform 1	3.0 3.0	6.5 5.0	9.5 8.0	3.0 3.0	11.5 9.5	ns ns
t_{PLH} t_{PHL}	Propagation dealy $\overline{LEBA}$ to A_n	Waveform 1, 2	4.0 4.0	7.0 7.0	9.5 9.5	4.0 4.0	11.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation dealy $\overline{LEAB}$ to B_n	Waveform 1, 2	5.0 4.0	8.0 7.5	11.5 9.5	4.0 4.0	13.5 11.5	ns ns
t_{PZH} t_{PZL}	Ouput Enable time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	3.0 4.0	5.0 7.0	8.0 10.0	2.5 4.0	9.5 11.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OEBA}$ or $\overline{OEAB}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	1.0 2.5	4.0 5.5	6.5 9.0	1.0 2.5	8.0 10.0	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{EBA}$ or $\overline{EAB}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	4.0 4.5	7.0 8.0	9.5 11.0	4.0 4.5	11.5 13.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{EBA}$ or $\overline{EAB}$ to $\overline{A}_n$ or $\overline{B}_n$	Waveform 4 Waveform 5	2.5 2.5	5.0 8.5	8.0 11.5	2.0 2.0	10.0 13.5	ns ns

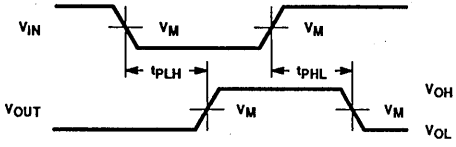
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	54F544 LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$T_S(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to $\overline{LEAB}$ or $\overline{LEBA}$ A_n or B_n to $\overline{EAB}$ or $\overline{EBA}$	Waveform 3	3.0 3.0			3.0 4.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to $\overline{LEAB}$ or $\overline{LEBA}$ A_n or B_n to $\overline{EAB}$ or $\overline{EBA}$	Waveform 3	3.0 3.0			3.0 4.0		ns ns
$t_w(L)$	Pulse width Latch enable	Waveform 3	4.0			4.5		ns

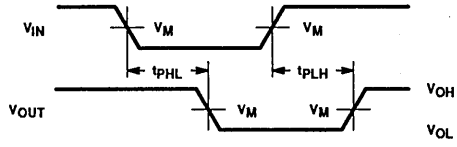
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

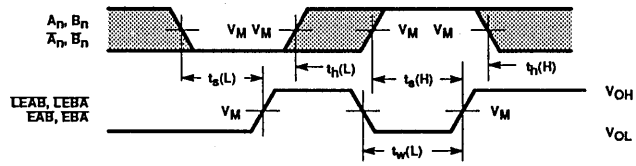
AC WAVEFORMS



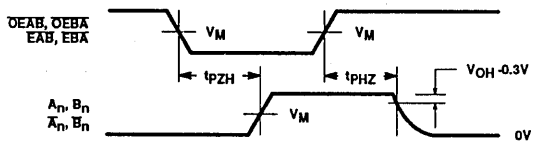
Waveform 1. Propagation Delay for Inverting Outputs



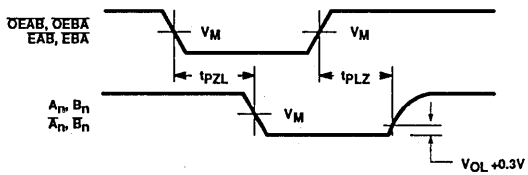
Waveform 2. Propagation Delay for Non-Inverting Outputs



Waveform 3. Propagation Delay for Data to Output, Data Setup Time and Hold Times, and Latch Enable Pulse Width



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: V_M = 1.5V
The shaded areas indicate when the input is permitted tochange for predictable output performance.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-3	mA
I_{OH2}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH1}	2.4			V
					I_{OH2}	2.5	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = Min, V_{IL} = Max , V_{IH} = Min, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage			V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current			V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = Max, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = Max, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, High-level voltage applied			V_{CC} = Max, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = Max		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	'F573	V_{CC} = Max			30	40	mA
		I_{CCL}					35	50	mA
		I_{CCZ}					40	60	mA
		I_{CCH}	'F574	V_{CC} = Max			45	65	mA
		I_{CCL}					50	70	mA
		I_{CCZ}					55	90	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n		Waveform 2	3.0 1.0	5.5 3.5	8.0 6.0	2.5 1.0	9.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n		Waveform 1	4.5 3.0	8.5 5.0	11.5 7.0	6.0 2.5	13.5 8.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F573	Waveform 4 Waveform 5	2.5 2.5	5.5 5.5	9.5 8.0	2.0 2.0	11.0 9.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 5.5	ns ns
f_{MAX}	Maximum Clock frequency		Waveform 1	110	125		100[4]		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n		Waveform 1	4.0 4.0	5.5 6.0	8.5 8.5	3.0 3.0	9.5 9.5	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F574	Waveform 4 Waveform 5	2.5 3.0	4.5 6.0	8.0 8.5	2.0 3.0	9.0 9.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level		Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns ns

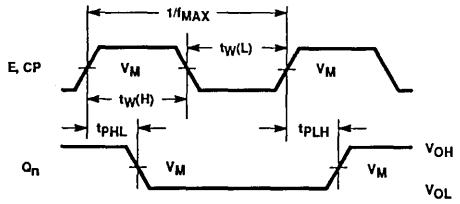
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E		Waveform 3	0.0 0.0			0.0 1.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E	'F573	Waveform 3	2.5 4.0			3.0 5.0		ns ns
$t_w(H)$ $t_w(L)$	E Pulse width, High or Low		Waveform 1	4.0 4.0			4.0 4.0		ns ns
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP		Waveform 3	2.0 2.0			2.5 2.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP	'F574	Waveform 3	1.5 1.5			2.0 2.0		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low		Waveform 1	3.0 4.5			3.0 4.5		ns ns

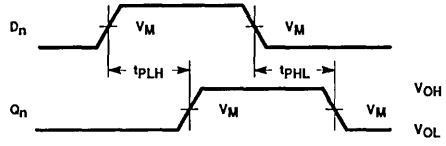
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. This parameter is guaranteed, but not tested.

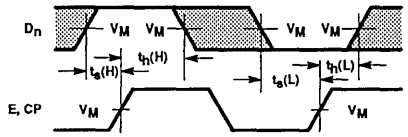
AC WAVEFORMS



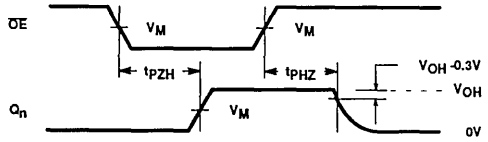
Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable and Clock Pulse Widths and Maximum Clock Frequency



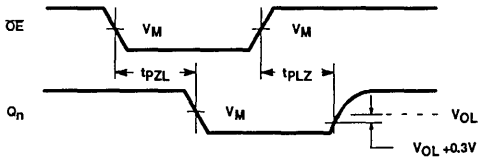
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times



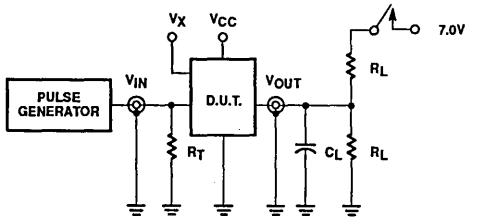
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



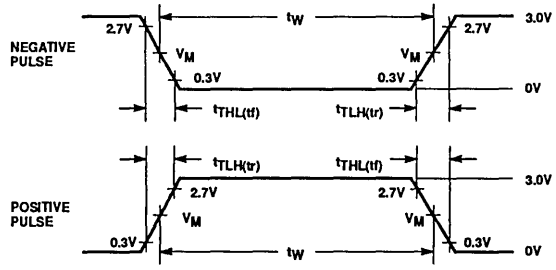
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	t_W	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

Military Logic Products

54F579
Counter

8-Bit Bidirectional Binary Counter (3-State)

Product Specification

DESCRIPTION

The 54F579 is a fully synchronous 8-stage Up/Down Counter with multiplexed 3-State I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry look-ahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, except for the case of asynchronous reset, are initiated by the rising edge of the clock. $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

FEATURES

- **Fully synchronous operation**
- **Multiplexed 3-state I/O ports for bus oriented applications**
- **Built in cascading carry capability**
- **U/$\overline{D}$ pin to control direction of counting**
- **Separate pins for Master reset and Synchronous operation**
- **Center power pins to reduce effects of package inductance**
- **Count frequency 115MHZ typ**
- **Supply current 100mA typ**
- **See 54F269 for 24-pin separate I/O port version**
- **See 54F779 for 16-pin version**

ORDERING INFORMATION

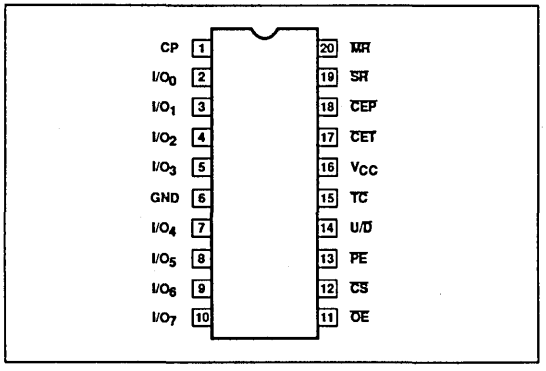
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F579/BRA
20-Pin Flat Pack	54F579/BSA
20-Pin LLCC	54F579/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

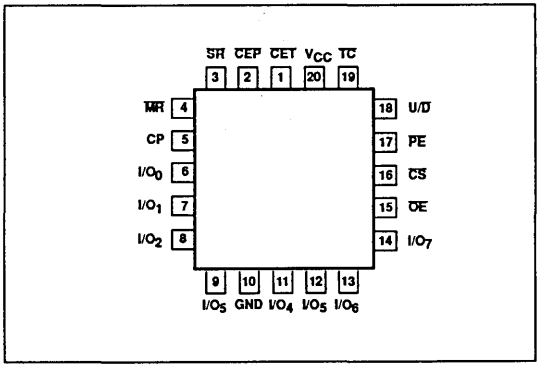
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_n	Data Inputs	3.5/1.0	70μA/0.6mA
	Data Outputs	150/40	3.0mA/20mA
$\overline{PE}$	Parallel Enable Input (Active Low)	1.0/1.0	20μA/0.6mA
U/$\overline{D}$	Up/Down Count Control Input	1.0/1.0	20μA/0.6mA
$\overline{MR}$	Master Reset Input (Active Low)	1.0/1.0	20μA/0.6mA
$\overline{SR}$	Synchronous Reset Input (Active Low)	1.0/1.0	20μA/0.6mA
$\overline{CEP}$	Count Enable Parallel Input (Active Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count Enable Trickle Input (Active Low)	1.0/1.0	20μA/0.6mA
$\overline{CS}$	Chip Select Input (Active Low)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable Input (Active Low)	1.0/1.0	20μA/0.6mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal Count Output (Active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

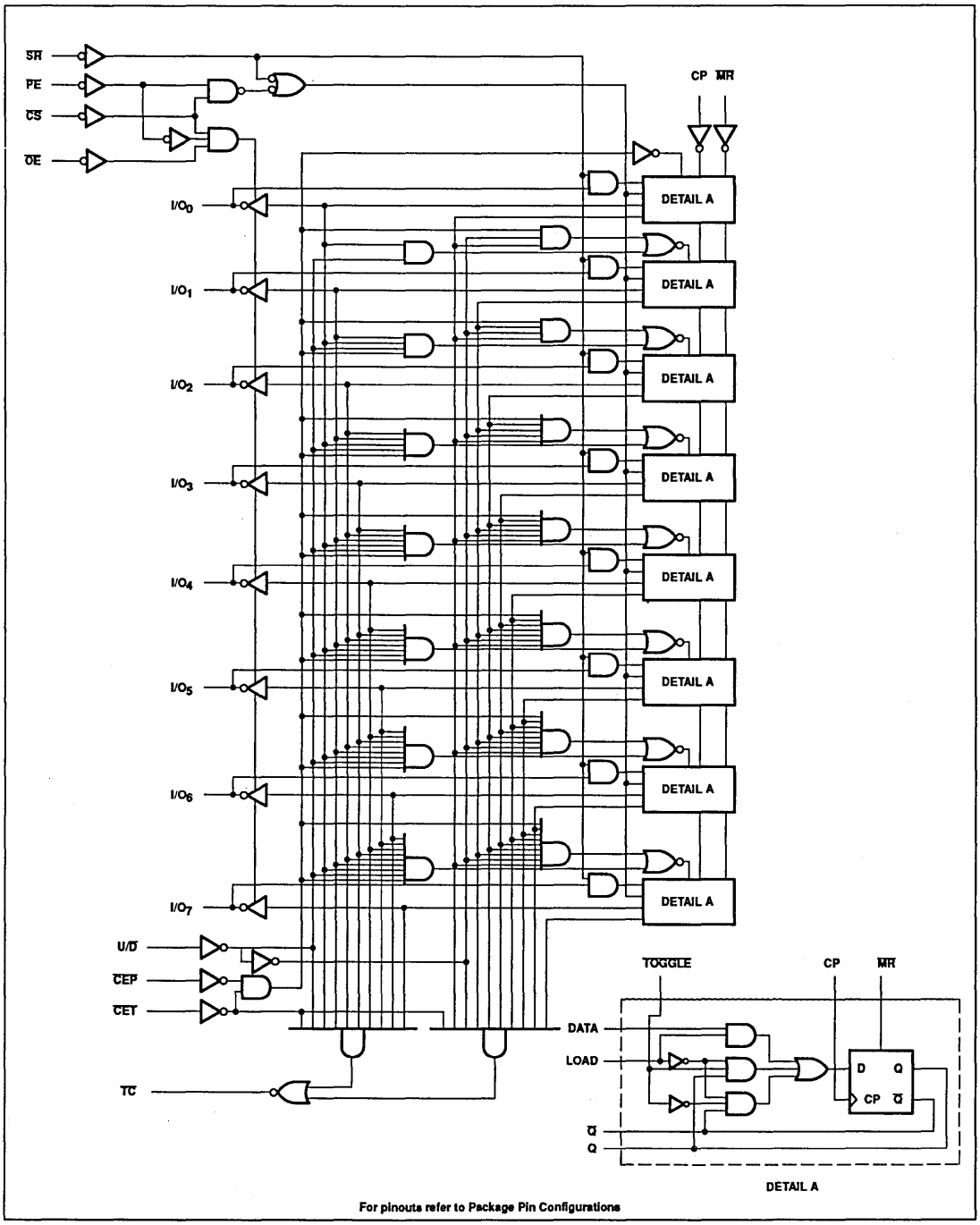
CERDIP PIN CONFIGURATION



LLCC PIN CONFIGURATION



LOGIC DIAGRAM



For pinouts refer to Package Pin Configurations

FUNCTION TABLE

INPUTS									OPERATING MODE
$\overline{MR}$	$\overline{SR}$	$\overline{CS}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	$\overline{OE}$	$\overline{CP}$	
X	X	H	X	X	X	X	X	X	I/O_0 to I/O_7 in high impedance ($\overline{PE}$ disabled)
X	X	L	H	X	X	X	H	X	I/O_0 to I/O_7 in high impedance
X	X	L	H	X	X	X	L	X	Flip-flop output appears on I/O lines
L	X	X	X	X	X	X	X	X	Asynchronous reset for all flip-flops
H	L	X	X	X	X	X	X	↑	Synchronous reset for all flip-flops
H	H	L	L	X	X	X	X	↑	Parallel load all flip-flops
H	H	(not LL)		H	X	X	X	↑	Hold
H	H	(not LL)		X	H	X	X	↑	Hold ($\overline{TC}$ held High)
H	H	(not LL)		L	L	H	X	↑	Count up
H	H	(not LL)		L	L	L	X	↑	Count down

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
(not LL) = $\overline{CS}$ and $\overline{PE}$ should never be Low voltage level at the same time

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage[4]		2.0			V
V_{IL}	Low-level input voltage[4]				0.8	V
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	$\overline{TC}$			-1	mA
		I/O_n			-3	mA
					-1	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1, 4]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = Min,	I_{OH} = -1mA	2.5			V
		I/O_n	V_{IL} = Max,	I_{OH} = -3mA	2.4	3.3		V
			V_{IH} = Min	I_{OH} = -1mA	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	I/O_n	V_{CC} = Max, V_I = 5.5V				1	mA
		others	V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current	except I/O_n	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V				0.6	mA
I_{OZH} + I_{IH}	Off-state current High-level voltage applied	I/O_n	V_{CC} = Max, V_{IH} = Min, V_I = 2.7V				70	µA
I_{OZL} + I_{IL}	Off-state current Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_I = 0.5V				-600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			95	135	mA
		I_{CCL}				105	145	mA
		I_{CCZ}				105	150	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		80[5]		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	5.0 5.0	7.5 7.5	10.5 10.5	4.5 5.0	23.0 12.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	5.5 5.5	7.5 7.5	10.0 10.0	5.0 5.0	19.5 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	Waveform 4	3.5 4.5	5.5 6.5	8.0 8.0	3.5 4.5	12.5 10.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 3	3.5 3.5	5.5 6.0	7.0 8.0	3.5 3.5	9.5 9.0	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to I/O_n	Waveform 2	5.0	7.0	9.0	5.0	11.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level $\overline{CS}$, $\overline{PE}$, I/O_n	Waveform 6 Waveform 7	3.0 6.5	6.0 9.0	7.5 9.5	3.0 5.5	10.0 12.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{CS}$, $\overline{PE}$, I/O_n	Waveform 6 Waveform 7	5.0 6.5	6.0 8.5	10.5 10.5	3.5 5.5	12.5 13.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level $\overline{OE}$, to I/O_n	Waveform 6 Waveform 7	1.0 2.5	2.5 5.0	4.0 7.0	1.0 2.0	8.0 10.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level $\overline{OE}$ to I/O_n	Waveform 6 Waveform 7	4.0 5.0	6.5 6.5	8.5 9.5	3.5 4.5	11.0 11.5	ns ns

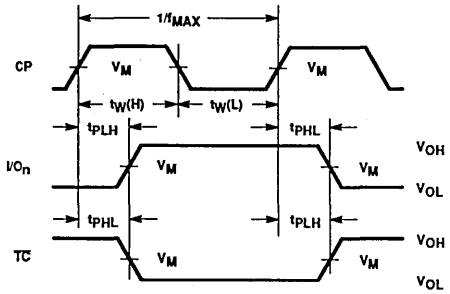
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 5	3.0 3.0			4.0 4.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	9.5 9.5			11.0 13.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$, $\overline{SR}$ or $\overline{CS}$ to CP	Waveform 5	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	5.0 9.0			7.5 11.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP	Waveform 5	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	Clock Pulse width	Waveform 1	4.5 4.5			6.0 6.0		ns ns
$t_w(L)$	$\overline{MR}$ Pulse width	Waveform 2	3.0			3.0		ns
t_{rec}	Recovery time	Waveform 2	4.0			5.0		ns

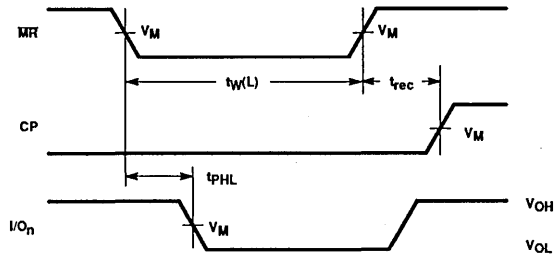
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under Recommended Operating Conditions for the applicable type and the Function Table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. When testing devices to the Functional Table specified, refer to the 'Recommended Operating Conditions' section of Application Note 202, "Testing and Specifying FAST Logic".
5. This parameter is guaranteed, but not tested.

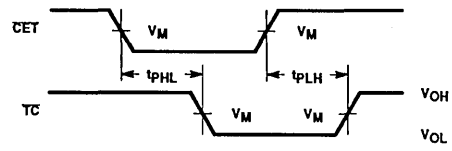
AC WAVEFORMS



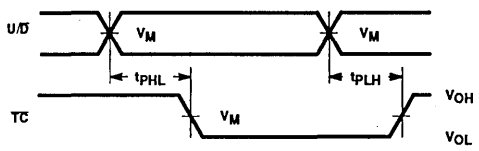
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width and Maximum Clock Frequency



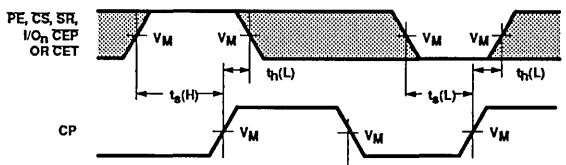
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



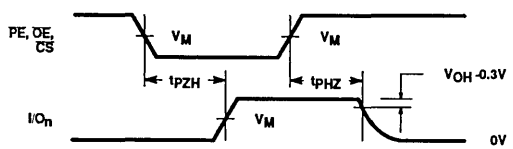
Waveform 3. Propagation Delay $\overline{CET}$ Input to Terminal Count Output



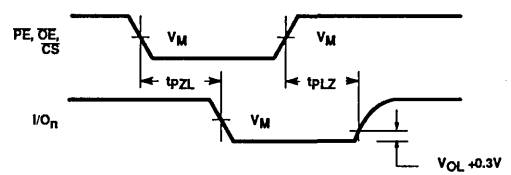
Waveform 4. Propagation Delay, U/$\overline{D}$ Input to Terminal Count Output



Waveform 5. Data Setup and Hold Times



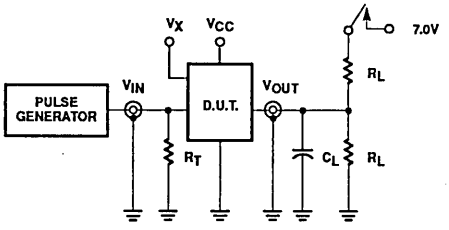
Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level



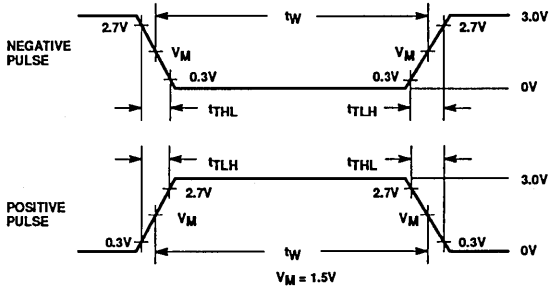
Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

54F620, 54F623
Transceivers

54F620 – Inverting 3-State Octal Bus Transceiver
54F623 – Non-Inverting 3-State Octal Bus Transceiver

Product Specification

Military FAST Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal bidirectional bus interface**
- **3-State buffer outputs sink 48mA and source 12mA**
  - **54F620, inverting**
  - **54F623, non-inverting**

DESCRIPTION

The 54F623 is an octal transceiver featuring non-inverting 3-State bus-compatible outputs in both send and receive directions. The outputs are capable of sinking 48mA and sourcing up to 12mA, providing very good capacitive drive characteristics. The 54F620 is an inverting version of the 54F623.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F620/BRA 54F623/BRA
20-Pin Ceramic FlatPack	54F620/BSA 54F623/BSA
20-Pin Ceramic LLCC	54F620/B2A 54F623/B2A

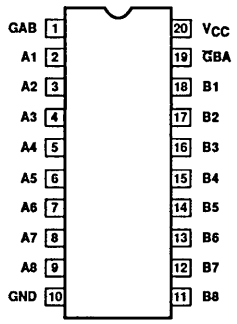
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_1 - A_8, B_1 - B_8	Data inputs	3.5/0.116	70μA/70μA
$\overline{GBA}$, GAB	3-State output enable inputs (active Low)	1.0/0.033	20μA/20μA
A_1 - A_8	Data outputs	150/40	3mA/24mA
B_1 - B_8	Data outputs	600/80	12mA/48mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

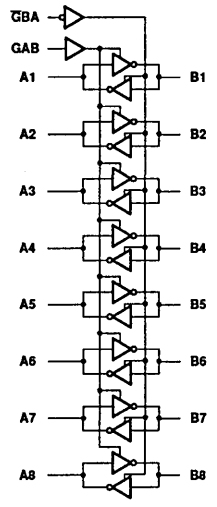
54F620



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

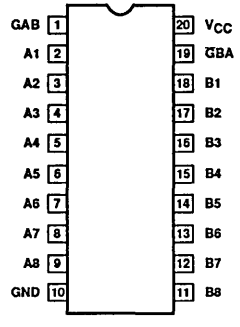
54F620



For LLCC pin assignments, see JEDEC Standard No. 2

PIN CONFIGURATION

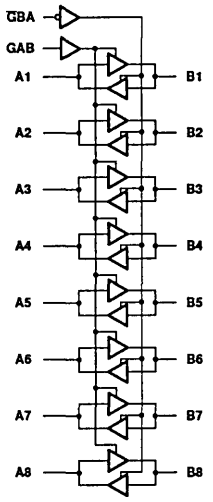
54F623



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

54F623



For LLCC pin assignments, see JEDEC Standard No. 2

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the Enable inputs ($\overline{GBA}$ and GAB). The Enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the 54F620 and 54F623 the capability to store data by the simultaneous enabling of $\overline{GBA}$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of the bus lines are at high impedance, both sets of bus lines (16 in all) will remain in their last states.

FUNCTION TABLE

ENABLE	INPUTS	OPERATION	
$\overline{GBA}$	GAB	54F620	54F623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Z	Z
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

H = High voltage level
L = Low voltage level
Z = High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_I	Input voltage range		-0.5 to +7.0	V
I_I	Input current range		-30 to +5.0	mA
V_O	Voltage applied to output in High output state range		-0.5 to +5.5	V
I_O	Current applied to output in Low output state	$A_1 - A_8$	40	mA
		$B_1 - B_8$	96	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage[5]		2.0			V
V_{IL}	Low-level input voltage[5]				0.7	V
I_{IK}	Input clamp current				-18	mA
I_{OH2}	High-level output current	A_1 - A_8			-3.0	mA
I_{OH1}		B_1 - B_8			-1.0	mA
I_{OH3}	High-level output current	B_1 - B_8			-12.0	mA
I_{OL}	Low-level output current	A_1 - A_8			20.0	mA
		B_1 - B_8			48.0	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		A_1 - A_8	V_{CC} = Min,	I_{OH2} = -3mA	2.4			V
			B_1 - B_8	V_{IL} = Max,	I_{OH1} = -1mA	2.5	3.4		V
			B_1 - B_8	V_{IH} = Min	I_{OH3} = -12mA	2.0			V
V_{OL}	Low-level output voltage		A_1 - A_8	V_{CC} = Min, V_{IL} = Max,	I_{OL} = 20mA		0.35	0.50	V
			B_1 - B_8	V_{IH} = Min	I_{OL} = 48mA		0.40	0.55	V
V_{IK}	Input clamp voltage			V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at		$\overline{G}BA$, GAB	V_{CC} = 0.0V, V_I = 7.0V				100	µA
	maximum input voltage		Others	V_{CC} = 5.5V, V_I = 5.5V				1	mA
I_{IH1}	High-level input current		$\overline{G}BA$, GAB	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		only	V_{CC} = Max, V_I = 0.5V				-20	µA
I_{OZH} +I_{IH}	Off-state current High-level voltage applied		A_1 - A_8 B_1 - B_8	V_{CC} = Max, V_O = 2.7V				70	µA
I_{OLZ} + I_{IL}	Off-state current Low-level voltage applied			V_{CC} = Max, V_O = 0.5V				-70	µA
I_{OS}	Short-circuit		A_1 - A_8	V_{CC} = Max		-60		-150	mA
	output current[3]		B1 - B8			-100		-225	mA
I_{CC}	Supply current (total)	F620	I_{CCH}	V_{CC} = Max	$\overline{G}BA$ = GAB = 4.5V; A_1 - A_8 = GND		70	92	mA
			I_{CCL}		$\overline{G}BA$ = GAB = 4.5V; A_1 - A_8 = 4.5V		84	110	mA
			I_{CCZ}		GAB = GND; $\overline{G}BA$ = A_1 - A_8 = 4.5V		70	92	mA
		F623	I_{CCH}		$\overline{G}BA$ = GAB = 4.5V; A_1 - A_8 = 4.5V		110	140	mA
			I_{CCL}		$\overline{G}BA$ = GAB = 4.5V; A_1 - A_8 = GND		110	140	mA
			I_{CCZ}		GAB = GND; $\overline{G}BA$ = A_1 - A_8 = 4.5V		99	130	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	54F620 LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	8.5 5.5	ns ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	2.5 1.0	4.5 2.5	6.5 4.5	2.0 1.0	8.5 5.5	ns ns
t_{PZH} t_{PZL}	Output enable to High or Low level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	3.0 4.0	7.5 7.5	10.5 10.5	2.5 3.5	12.5 12.5	ns ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	2.5 2.0	4.5 4.5	7.5 7.0	2.0 1.5	9.0 8.0	ns ns
t_{PZH} t_{PZL}	Output enable to High or Low level GAB To B_n	Waveform 3 Waveform 4	4.5 4.5	7.5 7.5	10.5 10.0	4.0 4.0	12.5 12.0	ns ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level GAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.5 6.5	9.5 9.5	2.5 3.5	12.0 11.5	ns ns

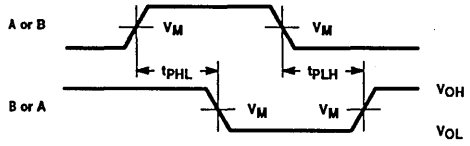
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	54F623 LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 2	2.0 3.0	4.0 5.0	5.5 7.0	2.0 2.5	7.0 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 2	2.0 2.5	4.0 4.5	5.5 6.5	2.0 2.5	7.5 8.0	ns ns
t_{PZH} t_{PZL}	Output enable to High or Low level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	5.0 5.0	8.5 7.5	10.5 9.5	5.0 5.0	13.5 11.0	ns ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level $\overline{G}BA$ to A_n	Waveform 3 Waveform 4	2.5 2.5	4.5 4.5	6.5 6.5	2.5 2.5	10.0 7.5	ns ns
t_{PZH} t_{PZL}	Output enable to High or Low level GAB To B_n	Waveform 3 Waveform 4	5.0 4.5	8.0 7.0	10.0 9.0	5.0 4.5	12.5 10.0	ns ns
t_{PHZ} t_{PLZ}	Output disable from High or Low level GAB to B_n	Waveform 3 Waveform 4	3.0 4.0	6.0 7.0	8.5 9.0	3.0 4.0	11.5 11.0	ns ns

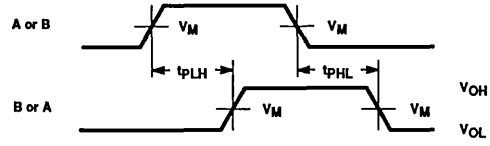
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with outputs open.
5. When testing devices to the functional table specified, refer to the 'Recommended Operating Conditions' section of Application Note 202, "Testing and Specifying FAST Logic".

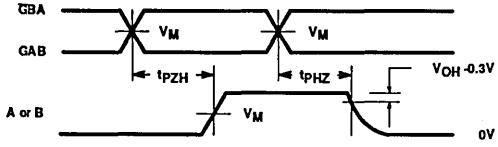
AC WAVEFORMS



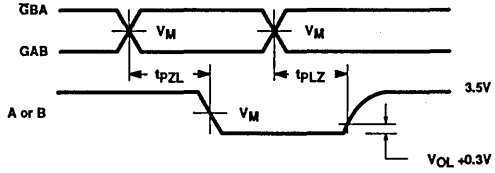
Waveform 1. For Inverting Outputs



Waveform 2. For non-Inverting Outputs



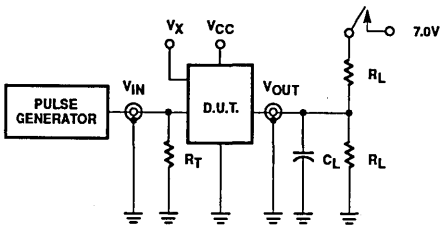
Waveform 3. 3-State Output Enable Time to High Level Output Disable Time from High Level



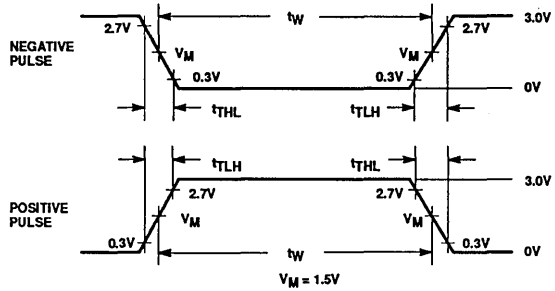
Waveform 4. 3-State Output Enable Time to Low Level Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

Military Logic Products

54F640
Transceiver

Octal Bus Transceiver, Inverting (3-State)

Product Specification

FEATURES

- **High impedance NPN base inputs for reduced loading (70μA in High and Low states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Inverting version of 54F245**
- **Octal bidirectional bus interface**
- **3-State buffer outputs sink 48mA and source 12mA**

DESCRIPTION

The 54F640 is an octal transceiver featuring inverting 3-State bus-compatible outputs in both send and receive directions.

The B_1 - B_8 outputs are capable of sinking 48mA and sourcing 12mA, providing very good capacitive drive characteristics.

The octal bus transceivers are designed for asynchronous two-way communication between data busses.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F650/BRA
20-Pin Ceramic Flat Pack	54F640/BSA
20-Pin Ceramic LLCC	54F640/B2A

FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus $\overline{B}$ data to Bus A
L	H	Bus $\overline{A}$ data to Bus B
H	X	(Z)

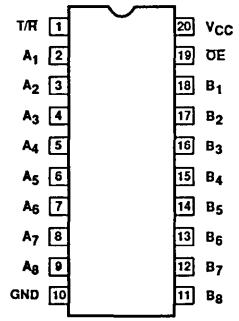
H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_1 - A_8, B_1 - B_8	Data inputs	3.5/0.115	70μA/70μA
T/$\overline{R}$	Transmit/receive input	2.0/0.067	40μA/40μA
$\overline{OE}$	Output enable inputs (active Low)	2.0/0.67	40μA/40μA
A_1 - A_8	Data outputs	150/33.3	3mA/20mA
B_1 - B_8	Data outputs	600/80	12mA/48mA

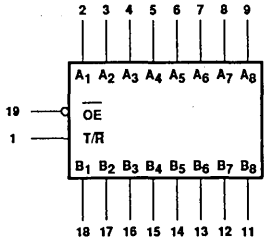
NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



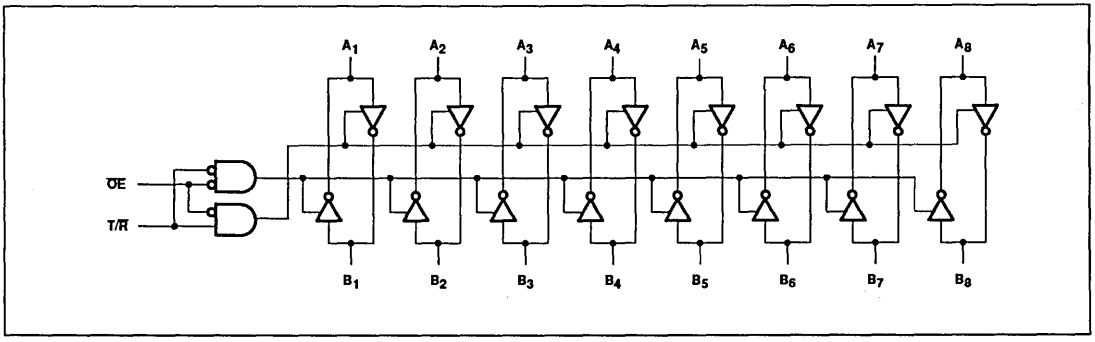
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_I	Input voltage range		-0.5 to +7.0	V
I_I	Input current range		-30 to +5	mA
V_O	Voltage applied to output in High output state range		-0.5 to +5.5	V
I_O	Current applied to output in Low output state	A_1 - A_8	40	mA
		B_1 - B_8	96	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.50	5.0	5.50	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH1}	High-level output current				-1	mA
I_{OH2}	High-level output current				-3	mA
I_{OH3}	High-level output current	B_1 - B_8			-12	mA
I_{OL}	Low-level output current	A_1 - A_8			20	mA
		B_1 - B_8			48	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	A_1 - A_8	V_{CC} = Min,	I_{OH1} = -1mA	2.5			V
		B_1 - B_8	V_{IL} = Max,	I_{OH2} = -3mA	2.4			V
		B_1 - B_8	V_{IH} = Min	I_{OH3} = -12mA	2.0			V
V_{OL}	Low-level output voltage	A_1 - A_8	V_{CC} = Min,	I_{OL} = 20mA		0.35	0.50	V
		B_1 - B_8	V_{IL} = Max, V_{IH} = Min	I_{OL} = 40mA		0.40	0.55	V
V_{IK}	Input clamp voltage		V_{cc} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	A_1-A_8 B_1-B_8	V_{CC} = 5.5V, V_I = 5.5V				1.0	mA
		$\overline{OE}$, T/$\overline{R}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH1}	High-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = Max, V_I = 2.7V				40	µA
I_{IL}	Low-level input current	$\overline{OE}$, T/$\overline{R}$ only	V_{CC} = Max, V_I = 0.5V				-40	µA
I_{IH}+ I_{OZH}	Off-state current High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_1 = 2.7V				70	µA
I_{IL}+ I_{OZL}	Off-state current Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_1 = 0.5V				-70	µA
I_{OS}	Short-circuit output current[3]	A_1-A_8	V_{CC} = Max		-60		-150	mA
		B_1-B_8			-100		-225	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max	T/$\overline{R}$=A_1-A_8=4.5V;$\overline{OE}$=GND		66	85	mA
		I_{CCL}		$\overline{OE}$ = T/$\overline{R}$ = B_1 - B_8 = GND		91	120	mA
		I_{CCZ}		$\overline{OE}$ = 4.5V; T/$\overline{R}$ = B_1-B_8=GND		78	102	mA

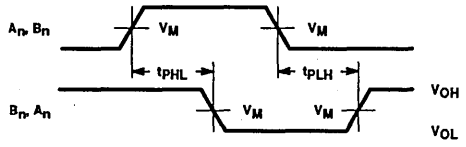
AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH}	Propagation delay A_n to B_n, B_n to A_n	Waveform 1	2.0	4.5	7.0	2.0	8.0	ns
t_{PHL}			1.0	2.5	5.0	1.0	5.5	ns
t_{PZH}	Output enable time to High or Low level	Waveform 2	6.0	9.0	11.0	5.0	13.0	ns
t_{PZL}		Waveform 3	6.0	9.0	11.0	6.0	11.5	ns
t_{PHZ}	Output disable time from High or Low level	Waveform 2	2.5	5.5	8.0	2.5	9.0	ns
t_{PLZ}		Waveform 3	2.0	4.5	7.0	2.0	7.5	ns

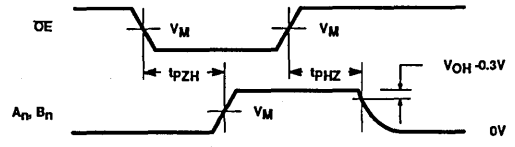
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests I_{OS} tests should be performed last.

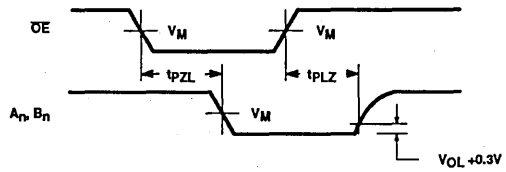
AC WAVEFORMS



Waveform 1. Propagation Delays for A_n to B_n or B_n to A_n



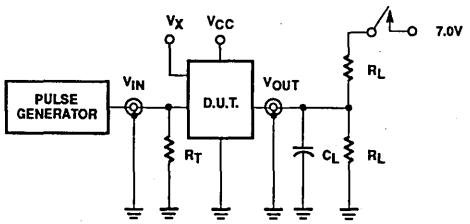
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



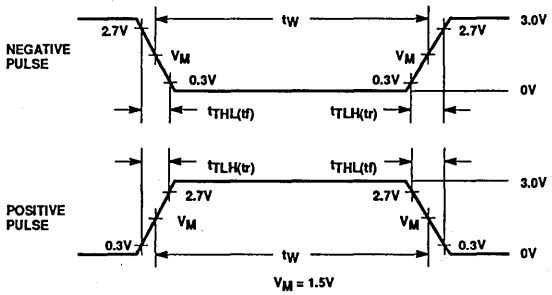
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per Function Table.

Signetics

Military Logic Products

54F646A
Transceiver/Register

Octal Transceiver/Register, Non-Inverting (3-State)

Objective Specification

FEATURES

- **Combines 54F245 and 54F374 type functions in one chip**
- **High impedance base inputs for reduced loading (70μA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Non-inverting data paths**
- **Controlled ramp outputs**
- **3-state outputs**
- **300 mil wide 24-pin Slim Dip package**

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54F646A/BLA

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT (TOTAL)
54F646A	185MHz	105mA

DESCRIPTION

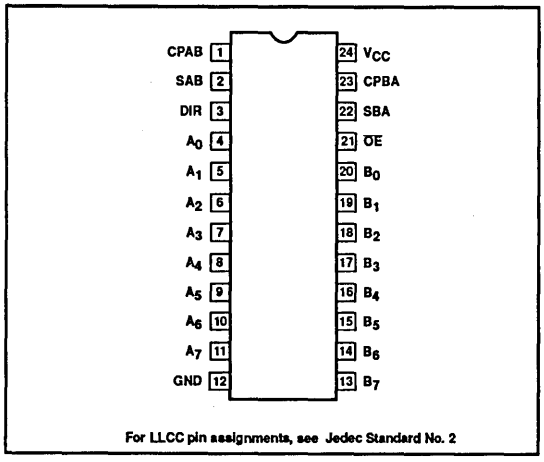
The 54F646A Transceiver/Register consists of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7, B_0 - B_7	A and B inputs	3.5/0.166	70μA/70μA
CPAB	A-to-B clock input	1.0/0.033	20μA/20μA
CPBA	B-to-A clock input	1.0/0.033	20μA/20μA
SAB	A-to-B select input	1.0/0.033	20μA/20μA
SBA	B-to-A select input	1.0/0.033	20μA/20μA
DIR	Data flow directional control enable input	1.0/0.066	20μA/40μA
$\overline{OE}$	Output Enable input	1.0/0.066	20μA/40μA
A_0 - A_7, B_0 - B_7	Outputs	750/80	15mA/48mA

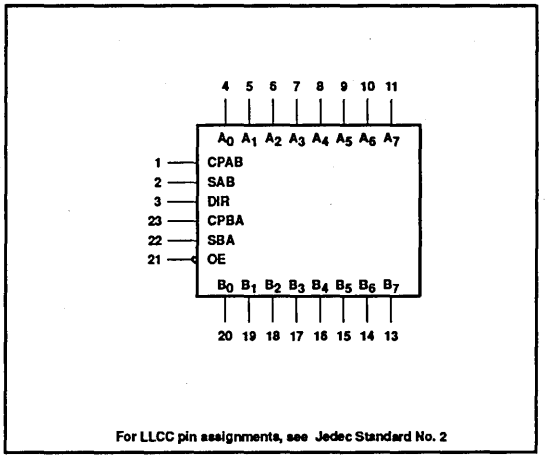
NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see Jedec Standard No. 2

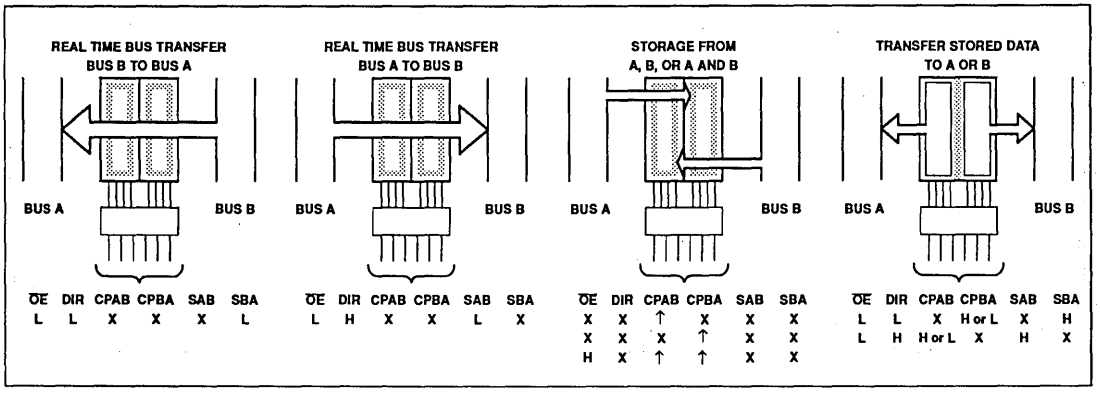
LOGIC SYMBOL



For LLCC pin assignments, see Jedec Standard No. 2

Transceiver/Register | 54F646A

The select (SAB, SBA) pins determine whether data is stored or transfered through the device in real-time. The DIR determines which bus will receive data when the $\overline{OE}$ is Low. In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses, A or B may be driven at a time. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 54F646A.

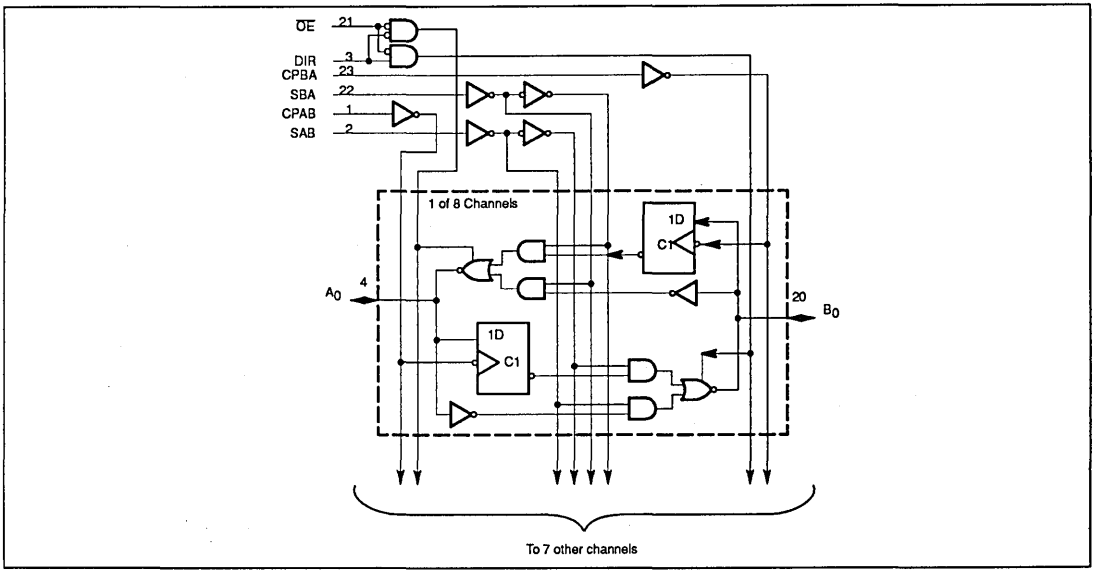


FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition
* = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enable, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	36	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-15	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max,	I_{OH} = -3mA	2.4			V
			V_{IH} = Min	I_{OH} = -15mA	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max	I_{OL} = 24mA		0.38	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at	others	V_{CC} = 0.0, V_I = 7.0V				100	µA
	maximum input voltage	A_0-A_7, B_0-B_7	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High-level input current	$\overline{OE}$ DIR CBAB, CPBA SAB, SBA	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{OE}$ DIR	V_{CC} = Max, V_I = 0.5V				-40	µA
		CBAB, CPBA SAB, SBA	V_{CC} = Max, V_I = 0.5V				-20	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = Max, V_O = 2.7V				70	µA
I_{OZH} + I_{IL}	Off-state output current, Low-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = Max, V_O = 0.5V				-70	µA
I_O	Output current[4]		V_{CC} = Max, V_O = 2.25V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			100	155	mA
		I_{CCL}				110	165	mA
		I_{CCZ}				105	160	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	165	185		125		MHz
t_{PLH}	Propagation delay CPAB or CPBA tp A_n or B_n	Waveform 1	5.5	7.0	10.0	4.0	11.5	ns
t_{PHL}			4.5	7.0	9.5	3.5	10.5	ns
t_{PLH}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2, 3	4.0	6.0	9.0	3.0	10.5	ns
t_{PHL}			2.0	5.0	8.0	1.5	9.0	ns
t_{PLH}	Propagation dealy SAB or SBA to A_n or B_n	Waveform 2, 3	4.5	6.5	9.5	3.5	11..0	ns
t_{PHL}			3.5	8.0	10.0	2.5	12.5	ns
t_{PZH}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5	3.0	5.0	7.5	2.0	9.0	ns
t_{PZL}		Waveform 6	3.0	5.5	8.0	2.0	10.0	ns
t_{PZH}	Output Enable time DIR to A_n or B_n	Waveform 5	3.0	5.0	8.0	2.5	9.0	ns
t_{PZL}		Waveform 6	3.5	6.0	8.5	3.0	11.0	ns
t_{PHZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5	1.5	5.0	7.5	1.0	11.0	ns
t_{PLZ}		Waveform 6	2.5	6.5	9.0	1.5	11.5	ns
t_{PHZ}	Output Disable time DIR to A_n or B_n	Waveform 5	2.0	4.5	7.5	1.0	8.5	ns
t_{PLZ}		Waveform 6	3.0	5.0	8.0	1.5	9.0	ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	3.5 4.0			4.5 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 3.5			5.0 4.0		ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. The output condition has been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Signetics

54F655A, 54F656A
Buffers/Drivers

54F655A Octal Buffer/Line Driver with Parity, Inverting (3-State)
54F656A Octal Buffer/Line Driver with Parity, Non-Inverting (3-State)

Product Specification

Military Logic Products

FEATURES

- Significantly improved AC performance over 54F655 and 54F656
- High impedance NPN base input for reduced loading (20μA in High and Low states)
- Ideal in applications where high output drive and light bus loading are required (I_{IL} is 20μA vs FAST std of 600μA)
- 54F655A combines 54F240 and 54F280 functions in one package
- 54F656A combines 54F244 and 54F280A functions in one package
- 54F655A Inverting
  54F656A Non-Inverting
- 3-State outputs sink 48mA
- Inputs source 12mA
- Inputs on one side and outputs on the other side simplify PC board layout
- Combined functions reduce part count and enhance system performance

DESCRIPTION

The 54F655A and 54F65A are octal buffers and line drivers with parity generation/checking designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. These parts include parity generator/checker to improve PC board density.

ORDERING INFORMATION

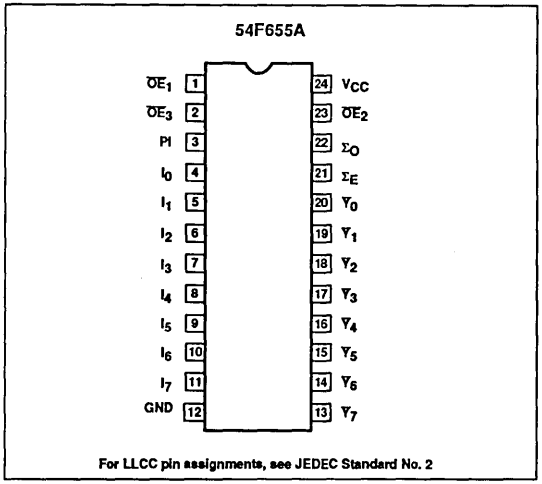
DESCRIPTION	ORDER CODE
Ceramic DIP	54F655A/BLA 54F656A/BLA
Ceramic Flat Pack	54F655A/BKA 54F656A/BKA
28-Pin Ceramic LLCC	54F655A/B3A 54F656A/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I_n	Data inputs	1.0/0.033	20μA/20μA
PI	Parity input	1.0/0.033	20μA/20μA
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	3-State output enable inputs (active Low)	1.0/0.033	20μA/20μA
$\overline{Y}_n$	Data outputs ((54F655A)	600/80	12mA/48mA
Y_n	Data outputs (54F656A)	600/80	12mA/48mA
Σ_E, Σ_O	Parity outputs	600/80	12mA/48mA

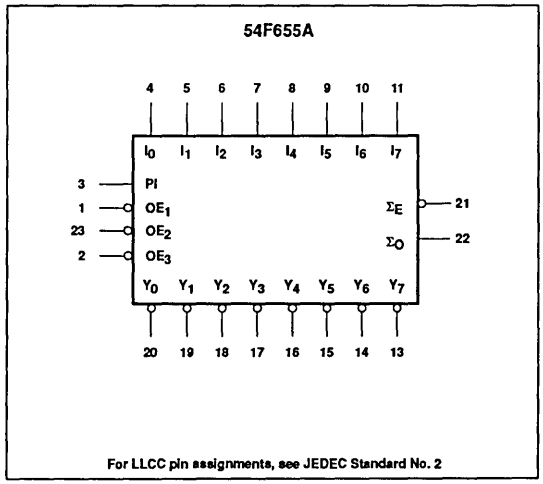
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High State and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

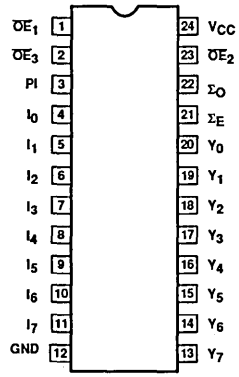
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

PIN CONFIGURATION

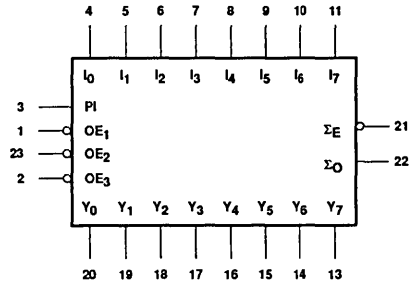
54F656A



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

54F656A



For LLCC pin assignments, see JEDEC Standard No. 2

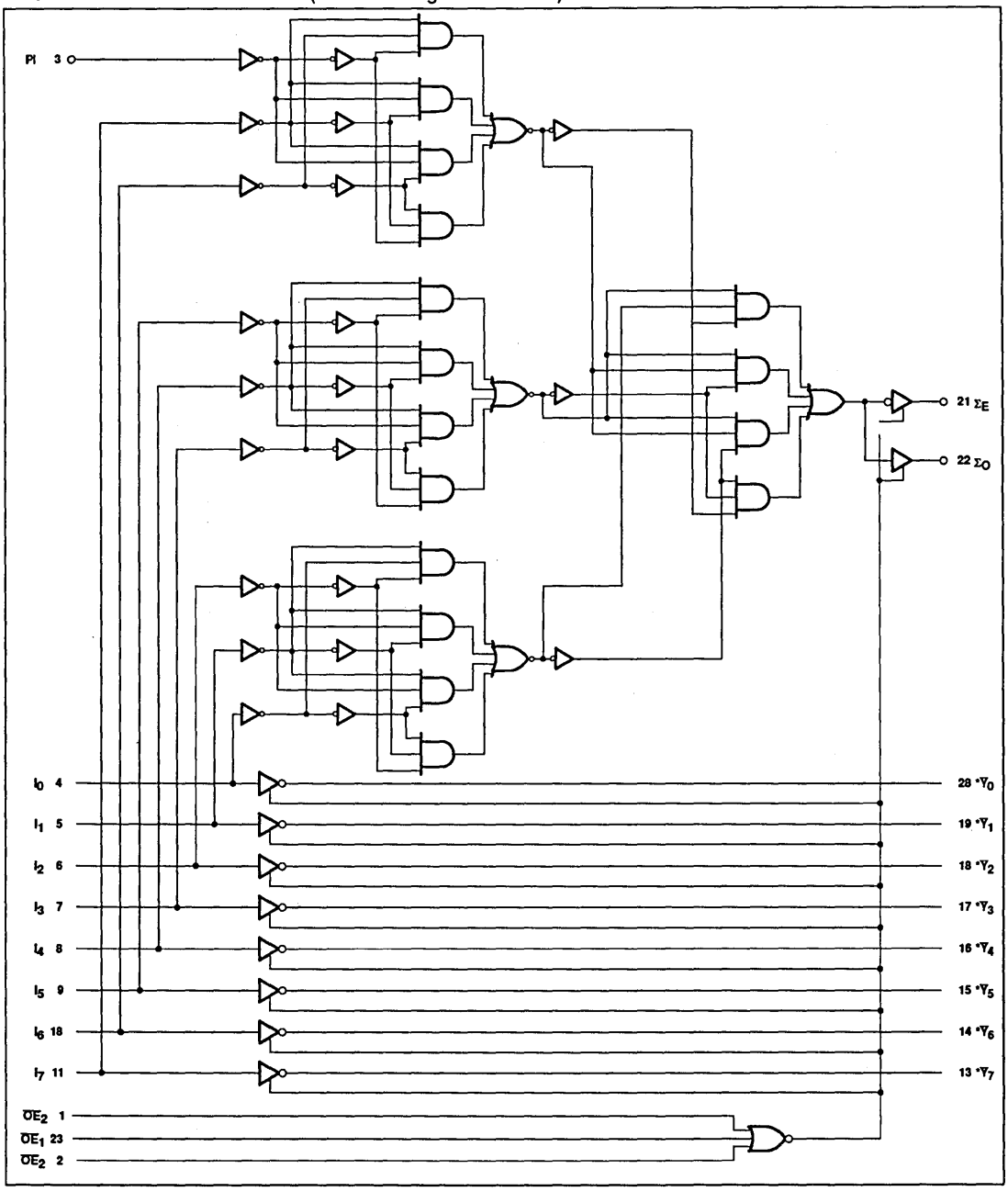
FUNCTION TABLES

INPUTS				DATA OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	I_N	54F655A	54F656A
L	L	L	L	H	L
L	L	L	H	L	H
H	X	X	X	Z	Z
X	H	X	X	Z	Z
X	X	H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance state

INPUTS	PARITY OUTPUTS	
Number of inputs, High (PI, I_0 - I_7)	Σ_E	Σ_O
Even - 0, 2, 4, 6, 8	H	L
Odd - 1, 3, 5, 7, 9	L	H
Any $\overline{OE}$ = High	(Z)	(Z)

LOGIC DIAGRAM FOR 54F655A (Non–inverting For 54F656A)



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current	-3		-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH} = Min	2.4			V
			I_{OH} =Max	2.0			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V			-1	-20	µA
I_{OZH}	Off-state current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				50	µA
I_{OZL}	Off-state current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max, V_O = 0.0V		-100		-225	mA
I_{CC}	Supply current (total)		I_{CCH}		50	80	mA
		V_{CC} = Max	I_{CCL}		78	110	mA
			I_{CCZ}		63	90	mA

AC ELECTRICAL CHARACTERISTICS

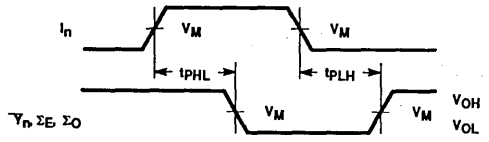
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Type	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay I_n to $\overline{Y}_n$ (54F655A)	Waveform 1	2.0 1.0	4.5 2.5	6.5 4.0	2.0 1.0	8.0 5.5	ns ns
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n (54F656A)	Waveform 2	2.0 2.5	4.0 5.5	6.5 7.0	2.0 2.5	7.5 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay I_n to Σ_E, Σ_O	Waveform 1, 2	5.5 5.5	10.0 11.0	13.0 14.5	5.0 5.0	16.0 20.0	ns ns
t_{PZH} t_{PZL}	Output enable time to High or Low level	Waveform 3 Waveform 4	4.0 4.5	7.0 8.0	10.5 11.0	4.0 4.5	12.0 13.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	1.5 2.0	4.5 5.0	8.0 8.0	1.5 2.0	10.0 10.0	ns ns

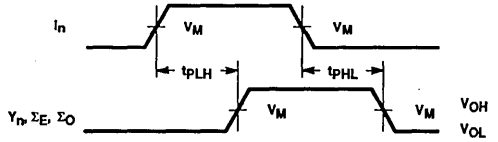
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under the recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

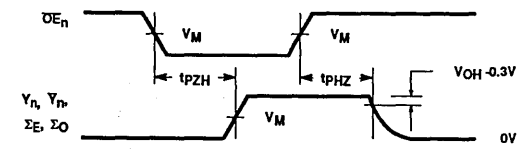
AC WAVEFORMS



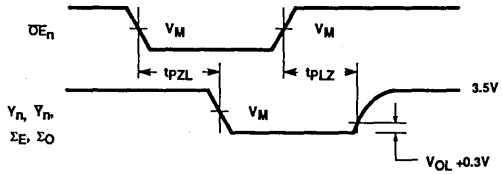
Waveform 1. Clock to Output Delays and Clock Pulse Width



Waveform 2. Propagation Delay for I_n to Y_n, Σ_E, Σ_O.



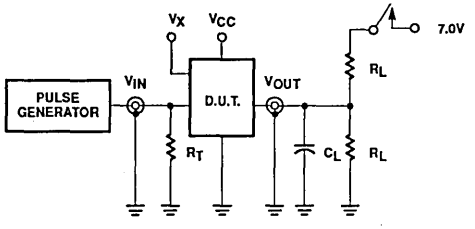
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



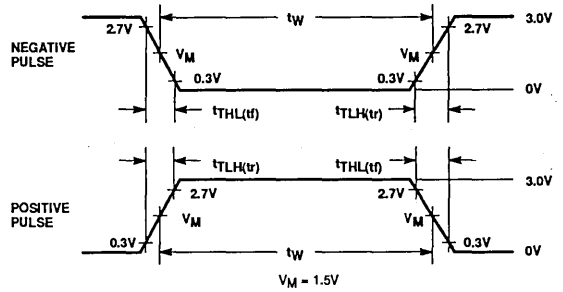
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

Military Logic Products

54F657
Transceiver

Octal Bidirectional Transceiver With 8-Bit Parity Generator/Checker (3-State Outputs)

Product Specification

FEATURES

- **High-impedance NPN base input for reduced loading (20 in High and Low states)**
- **Ideal in applications where high output drive and light bus loading are required (I_{IL} is 20μA vs FAST std of 600μA)**
- **24-pin slim dip (300-mil) package**
- **3-State outputs**
- **Outputs sink 48mA**
- **12mA source current**
- **Input diodes for termination effects**

DESCRIPTION

The 54F657 contains eight non-inverting buffers with 3-State outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 20mA at the A ports and 48mA at the B ports. The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active High) enables data from A ports to B ports; Receive (active Low) enables data from B ports to A ports.

ORDERING INFORMATION

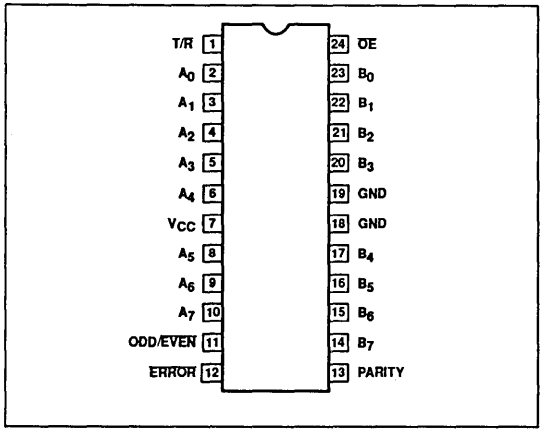
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54F657/BLA
24-Pin Ceramic FlatPack	54F657/BKA
28-Pin Ceramic LLCC	54F657/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

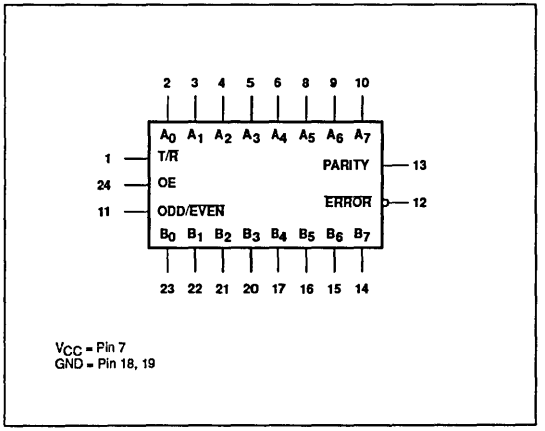
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A ports 3-State inputs	5.0/0.167	100μA/100μA
B_0 - B_7	B ports 3-State inputs	3.5/0.117	70μA/70μA
PARITY	Parity input	3.5/0.117	70μA/70μA
T/$\overline{R}$	Transmit/receive input	2.0/0.066	40μA/40μA
$\overline{ODD}$/EVEN	ODD/EVEN input	1.0/0.033	20μA/20μA
$\overline{OE}$	Output enable input (active Low)	2.0/0.066	40μA/40μA
A_0 - A_7	A ports 3-State outputs	150/33.3	3mA/20mA
B_0 - B_7	B ports 3-State outputs	600/80	12mA/48mA
PARITY	Parity output	150/33.3	3mA/20mA
$\overline{ERROR}$	Error output	150/33.3	3mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as 20μA in the High state and 0.6mA in the Low state.

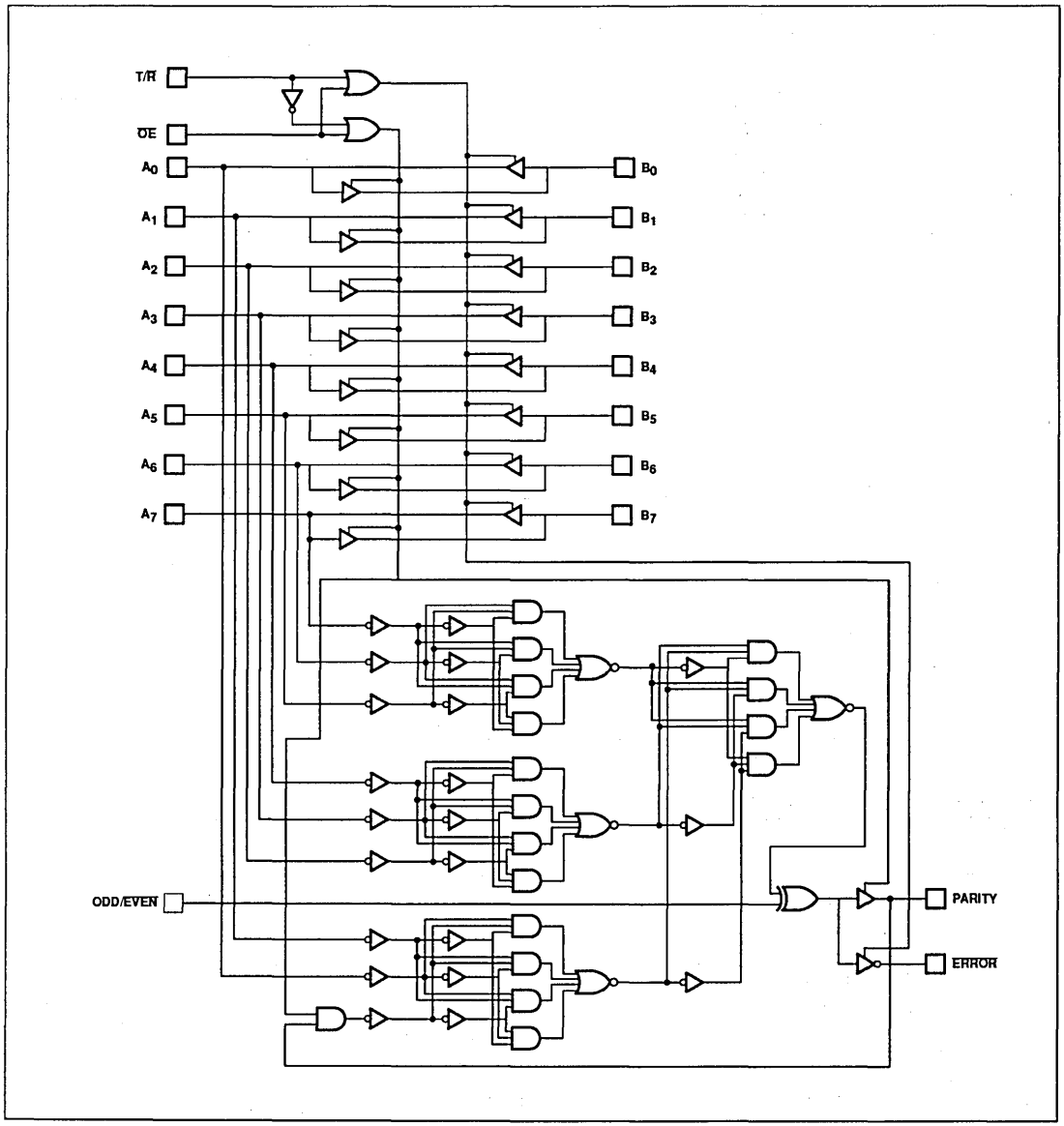
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC DIAGRAM



The Output Enable inputs disable both the A and B ports by placing them in a High-Z condition when either the $\overline{OE}$ input is High or the $\overline{OE}$ input is Low.

The parity generator detects whether an even or odd number of bits on the A ports are High, depending on the condition of the Parity Select input. If the Even input is active High and an even number of A inputs are High, the Parity output is High. The parity of the data received on the B ports is compared with the Parity Select input and the Error output is Low if not equal.

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUTPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/EVEN	PARITY	$\overline{ERROR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	(Z)	Transmit
	L	H	L	L	(Z)	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	(Z)	Transmit
	L	H	L	H	(Z)	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	(Z)	(Z)	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z)= High impedance state

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_I	Input voltage range		-0.5 to +7.0	V
I_I	Input current range		-30 to +5	mA
V_O	Voltage applied to output in Huigh output state range		-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	A_0 - A_7	40	mA
		B_0 - B_7, PARITY, $\overline{ERROR}$	96	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage[4]		2.0			V
V_{IL}	Low-level input voltage[4]				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH2}	High-level output current	A_0 - A_7 & B_0 -B_7			-3	mA
		B_0 - B_7, PARITY, $\overline{ERROR}$			-12	mA
I_{OH1}	High-level output current	A_0 - A_7 & B_0 - B_7			-1	mA
I_{OL}	Low-level output current	A_0 - A_7			20	mA
		B_0 - B_7, PARITY, $\overline{ERROR}$			48	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	All outputs	V_{CC} = Min,	I_{OH} = -3mA	2.4			V
			V_{IL} = Max,	I_{OH} = -1mA	2.5	3.4		V
		B_0 - B_7, PARITY $\overline{\text{ERROR}}$	V_{IH} = Min	I_{OH} = -12mA	2.0			V
V_{OL}	Low-level output voltage	A_0 - A_7	V_{CC} = Min,	I_{OL} = 20mA		.35	.50	V
		B_0 - B_7, PARITY $\overline{\text{ERROR}}$	V_{IL} = Max, V_{IH} = Min	I_{OL} = 48mA		.40	.55	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	T/$\overline{\text{R}}$, $\overline{\text{OE}}$, ODD/$\overline{\text{EVEN}}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		A_0 - A_7	V_{CC} = 5.5V, V_I = 5.5V				2	mA
		B_0 - B_7	V_{CC} = 5.5V, V_I = 5.5V				1	mA
I_{IH1}	High-level input current	ODD/$\overline{\text{EVEN}}$	V_{CC} = Max, V_I = 2.7V				20	µA
		T/$\overline{\text{R}}$, $\overline{\text{OE}}$					40	µA
I_{IL}	Low-level input current	ODD/$\overline{\text{EVEN}}$	V_{CC} = Max, V_I = 0.5V				-20	µA
		T/$\overline{\text{R}}$, $\overline{\text{OE}}$					-40	µA
I_{IH} + I_{OZH}	Off-state current High level voltage applied	A_0 - A_7	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				100	µA
I_{IH} + I_{OZL}	Off-state current Low level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-100	µA
I_{IH} + I_{OZH}	Off-state current High level voltage applied	B_0 - B_7 PARITY	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				70	µA
I_{IH} + I_{OZL}	Off-state current Low level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-70	µA
I_{OZH}	Off-state current High level voltage applied	$\overline{\text{ERROR}}$	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				50	µA
I_{OZL}	Off-state current Low level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]	A_0 - A_7	V_{CC} = Max		-60		-150	mA
		B_0 - B_7			-100		-225	mA
I_{CC}	Supply current (total	I_{CCH}	V_{CC} = Max			90	125	mA
		I_{CCL}				106	150	mA
		I_{CCZ}				98	145	mA

AC ELECTRICAL CHARACTERISTICS

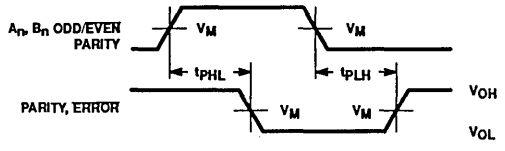
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ[2]	Max	Min	Max	
t_{PLH1} t_{PHL1}	Propagation delay A_n to B_n, B_n to A_n	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.5 8.5	ns ns
t_{PLH2} t_{PHL2}	Propagation delay A_n to PARITY	Waveform 1, 2	7.0 7.0	10.0 10.0	14.0 14.0	6.5 6.5	18.0 18.5	ns ns
t_{PLH3} t_{PHL3}	Propagation delay ODD/$\overline{EVEN}$ to PARITY, $\overline{ERROR}$	Waveform 1, 2	4.5 4.5	7.5 8.0	11.0 11.5	4.0 4.0	13.0 14.5	ns ns
t_{PLH4} t_{PHL4}	Propagation delay B_n to $\overline{ERROR}$	Waveform 1, 2	8.0 8.0	14.0 14.0	20.5 20.5	7.0 7.0	24.0 25.5	ns ns
t_{PLH5} t_{PHL5}	Propagation delay PARITY to $\overline{ERROR}$	Waveform 1, 2	8.0 8.0	11.5 12.0	15.5 15.5	7.0 7.5	18.0 19.5	ns ns
t_{PZH} t_{PZL}	Output enable time[5] to High or Low level	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.5 12.5	ns ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.5 8.0	ns ns

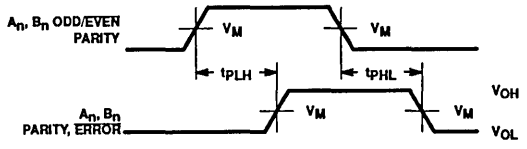
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. When testing devices to the functional table specified refer to the "Recommended Operating Conditions" section of the Applications Note 202, "Testing and Specifying FAST Logic".
5. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{ERROR}$. VALID data at the $\overline{ERROR}$ pin ≥ (B to A) + (A to PARITY).

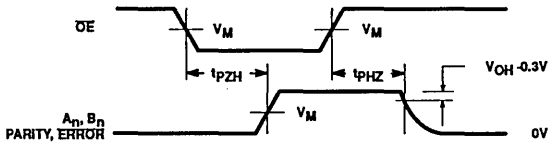
AC WAVEFORMS



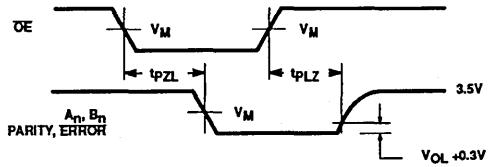
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting Outputs



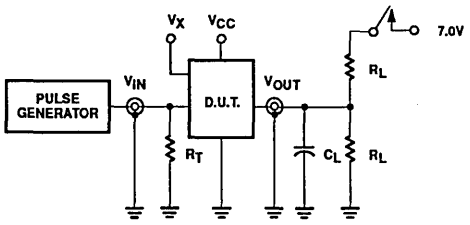
Waveform 3. 3-State Enable Time to High Level and Disable Time from High Level



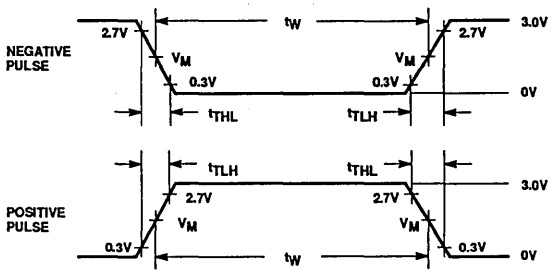
Waveform 4. 3-State Enable Time to Low Level and Disable Time from Low Level

NOTE: For all waveforms, V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at:: ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54F676
Shift Register

16-Bit Shift Register

Product Specification

Military FAST Products

FEATURES

- **16-bit parallel-to-serial conversion**
- **16-bit serial-in, serial-out**
- **Chip Select control**
- **Power supply current 48mA typical**
- **Shift frequency 110MHz typical**

DESCRIPTION

The 54F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is High, information present on the parallel data (D_0-D_{15}) inputs is entered on the falling edge of the Clock Pulse ($\overline{CP}$) input signal. When M is Low, data is shifted out of the most significant bit position while information present on the Serial (S1) input shifts into the least significant bit position. A High signal on the Chip Select ($\overline{CS}$) input prevents both parallel and serial operations.

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

Hold – a High signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the 16 registers.

Shift/Serial Load – data present on the S1 pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks, finally appearing on the SO pin.

Parallel Load – data present on P_0 - P_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

ORDERING INFORMATION

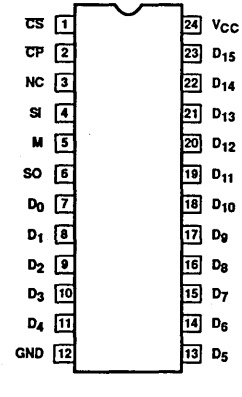
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54F676/BLA
24-Pin Ceramic Flatpack	54F676/BKA
28-Pin Ceramic LLCC	54F676/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20µA/0.6mA
SI	Serial data input	1.0/1.0	20µA/0.6mA
M	Mode select input	1.0/1.0	20µA/0.6mA
D_0 - D_{15}	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20µA/0.6mA
SO	Serial data output	50/33	1mA/20mA

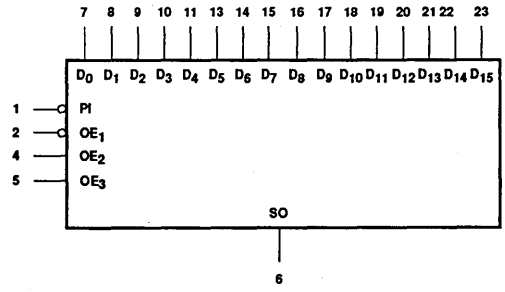
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High State and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

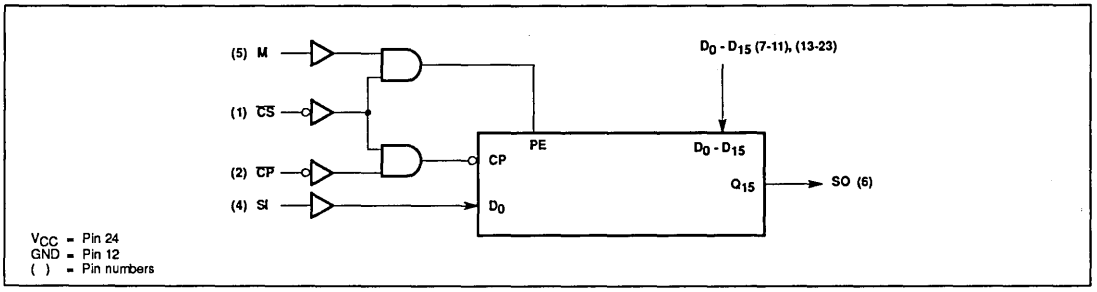
Shift Register 54F676

FUNCTION TABLE

CONTROL INPUT			OPERATING MODE
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/serial load
L	H	↓	Parallel load

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

Shift Register | 54F676

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V			-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = Max		48	72	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = 25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55 TO +125°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	110		90[4]		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SO	Waveform 1	4.5 5.0	8.0 7.0	11 12.5	4.5 5.0	12 13.5	ns

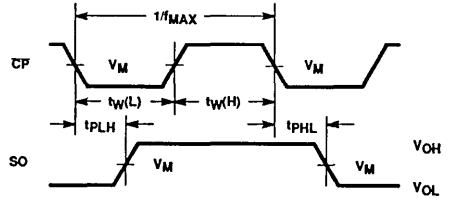
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = 25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55 TO +125°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Setup time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns ns
$t_H(H)$ $t_H(L)$	Hold time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_N $\overline{CP}$	Waveform 2	3.0 3.0			3.0 3.0		ns ns
$t_H(H)$ $t_H(L)$	Hold time, High or Low D_N $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low M to $\overline{CP}$	Waveform 2	8.0 8.0			8.0 8.0		ns ns
$t_H(H)$ $t_H(L)$	Hold time, High or Low M to $\overline{CP}$	Waveform 2	2.0 2.0			2.0 2.0		ns ns
$t_S(L)$	Setup time, Low $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		ns
$t_H(H)$	Setup time, High $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		ns
$t_W(H)$ $t_W(L)$	$\overline{CP}$ pulse width High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns ns

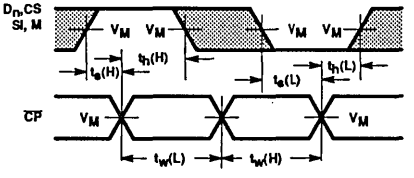
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V and T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. This test is guaranteed, but not tested.

AC WAVEFORMS



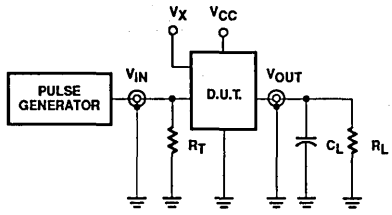
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Frequency



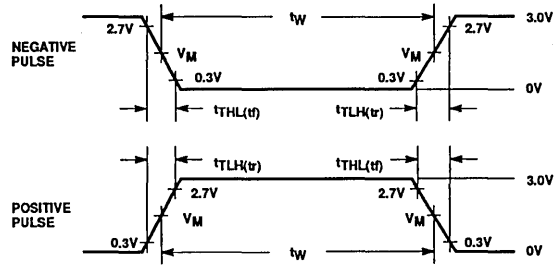
Waveform 2. Propagation Delay for Data to Output, Data and Select Setup, and Hold Times

NOTE: V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

54F776
Pi-Bus Transceiver

Octal Bidirectional Latched Transceiver

Product Specification

Military Fast Products

DESCRIPTION

The 54F776 is an octal latched transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. This bus has a loaded characteristic impedance range of 20 to 50 Ω and is terminated on each end with a 30 to 40Ω resistor.

The 54F776 is an octal bidirectional transceiver with Open-Collector B and 3-State A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100 mA from 2V and features a controlled linear ramp to minimize crosstalk and ringing on the bus.

A separate high level control voltage (V_X) is provided to prevent the A side output high level from exceeding future high density processor supply voltage levels. For 5V systems, V_X is simply tied to V_{CC}.

FEATURES

- **Latching Transceiver**
- **Controlled output ramp**
- **High drive Open-Collector output current with minimum output swing**
- **Pi-Bus specification compatible**
- **Multiple package options**
- **Controlled power on/off sequence**

ORDERING INFORMATION

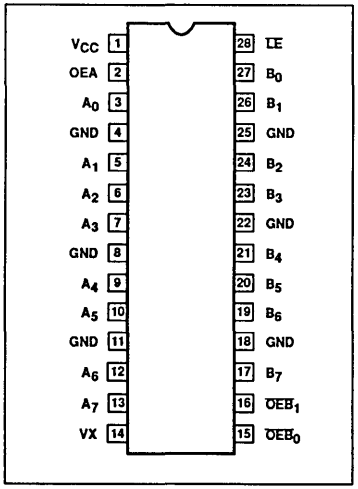
DESCRIPTION	ORDER CODE
28-Pin Ceramic DIP (600mil)	54F776/BXA
28-Pin Flatpack	54F776/BYA
28-Pin LLCC	54F776/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

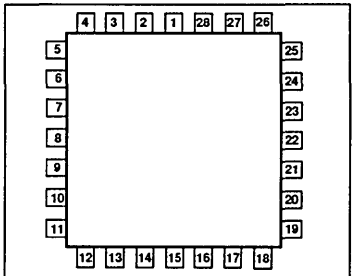
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	PNP latched input	3.5/0.1167	70μA/70μA
B_0 - B_7	Data input with threshold circuitry	5.0/0.167	100μA/100μA
OEA	A output Enable input (active-High)	1.0/0.033	20μA/20μA
$\overline{OEB}_0$, $\overline{OEB}_1$	B output Enable inputs (active-Low)	1.0/0.033	20μA/20μA
$\overline{LE}$	Latch Enable input (active-Low)	1.0/0.033	20μA/20μA
A_0 - A_7	3-State outputs	150/33.3	3mA/20mA
B_0 - B_7	Open-Collector outputs	OC*/166.7	OC*/100mA

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state. * OC = Open-Collector

PIN CONFIGURATION



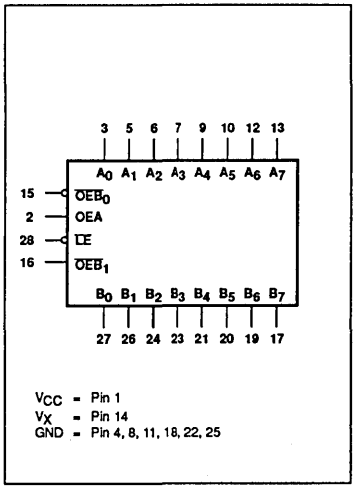
LLCC PIN CONFIGURATION



PIN/FUNCTION

1	V_{CC}	11	GND	21	B4
2	OEA	12	A6	22	GND
3	A0	13	A7	23	B3
4	GND	14	VX	24	B2
5	A1	15	$\overline{OEB}_0$	25	GND
6	A2	16	$\overline{OEB}_1$	26	B1
7	A3	17	B7	27	B0
8	GND	18	GND	28	$\overline{LE}$
9	A4	19	B6		
10	A5	20	B5		

LOGIC SYMBOL



V_{CC} = Pin 1
V_X = Pin 14
GND = Pin 4, 8, 11, 18, 22, 25

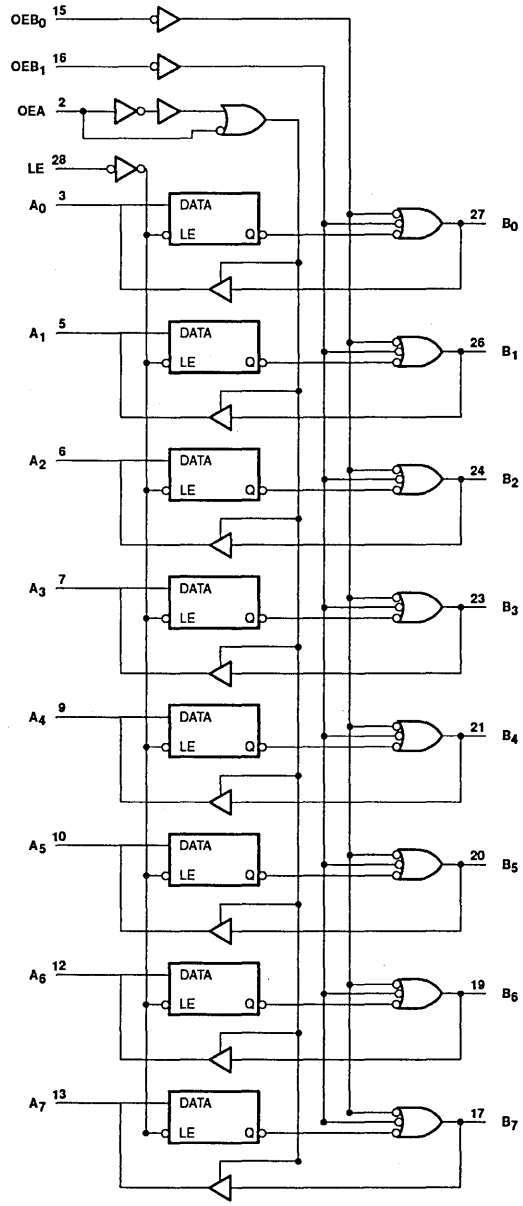
Pi-Bus Transceiver 54F776

PIN DESCRIPTION

SYMBOL	PINS	TYPE	NAME AND FUNCTION
A_0	3	I/O	PNP latched input/3-State output (with V_X control option)
A_1	5	I/O	
A_2	6	I/O	
A_3	7	I/O	
A_4	9	I/O	
A_5	10	I/O	
A_6	12	I/O	
A_7	13	I/O	
B_0	27	I/O	Data input with special threshold circuitry to reject noise/Open-Collector output High current drive
B_1	26	I/O	
B_2	24	I/O	
B_3	23	I/O	
B_4	21	I/O	
B_5	20	I/O	
B_6	19	I/O	
B_7	17	I/O	
$\overline{OEB}_0$	15	I	Enables the B outputs when both pins are Low
$\overline{OEB}_1$	16	I	
OEA	2	I	Enables the A outputs when High
$\overline{LE}$	28	I	Latched when High (a special delay feature is built in for proper enabling times)
V_X	14	I	Clamping voltage keeping V_{OH} from rising above V_X ($V_X = V_{CC}$ for normal use)

Pi-Bus Transceiver | 54F776

LOGIC DIAGRAM



V_{CC} = Pin 1
V_X = Pin 14
GND = 4, 8, 11, 18, 22, 25

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_X	V_{OH} output level control voltage (A outputs)		-0.5 to +7.0	V
V_I	Input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	-0.5 to +7.0	V
		A_0 - A_7, B_0 - B_7	-0.5 to 5.5	V
I_I	Input current		-40 to +5	mA
V_O	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	B_0 - B_7	200	mA
		A_0 - A_7	40	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B_0 - B_7	2.0			V
		B_0 - B_7[4]	1.60			
V_{IL}	Low-level input voltage	Except B_0 - B_7			0.8	V
		B_0 - B_7[4]			1.45	
I_{IK}	Input clamp current	Except A_0 - A_7			-18	mA
		A_0 - A_7			-40	mA
I_{OH}	High-level output current	A_0 - A_7			-3	mA
I_{OL}	Low-level output current	A_0 - A_7			20	mA
		B_0 - B_7			100	
T_A	Operating free-air temperature range		-55		+125	°C

Pi-Bus Transceiver | 54F776

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current	B_0 - B_7	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2.0V, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A_0 - A_7	V_{CC} = Min, V_{IL} = Max	I_{OH} = -3mA, V_X = V_{CC}	2.5	2.9	V_{CC}	V
			V_{IH} = Min	I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A_0 - A_7	V_{CC} = Min, V_{IL} = Max	I_{OL} = 20mA, V_X = V_{CC}		0.3	0.5	V
		B_0 - B_7	V_{IH} = Min	I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A_0 - A_7	V_{CC} = Min, I_I = I_{IK}				-0.5	V
		Except A_0 - A_7	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{IH2}	Input current at maximum input voltage	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = Max, V_I = 7.0V			1	100	µA
		A_0 - A_7	V_{CC} = Max, V_I = 5.5V			0.01	1	mA
		B_0 - B_7	V_{CC} = Max, V_I = 5.5V			0.01	1	mA
I_{IH1}	High-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = Max, V_I = 2.7V				20	µA
		B_0 - B_7	V_{CC} = Max, V_I = 2.1V				100	µA
I_{IL}	Low-level input current	$\overline{OEB}_n$, OEA, $\overline{LE}$	V_{CC} = Max, V_I = 0.5V				-20	µA
		B_0 - B_7	V_{CC} = Max, V_I = 0.3V				-100	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_7	V_{CC} = Max, V_O = 2.7V				70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_7	V_{CC} = Max, V_O = 0.5V				-70	µA
I_X	High-level control current		V_{CC} = Max, V_X = V_{CC}, $\overline{LE}$ = OEA = $\overline{OEB}_n$ = 2.7V, A_0 - A_7 = 2.7V, B_0 - B_7 = 2.0V		-100		100	µA
			V_{CC} = Max, V_X = 3.13V & 3.47V, $\overline{LE}$ = OEA = 2.7V, $\overline{OEB}_n$ = A_0 - A_7 = 2.7V, B_0 - B_7 = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	A_0 - A_7 only	V_{CC} = Max, B_n = 1.6V, OEA = 2.0V, $\overline{OEB}_n$ = 2.7V		-60	-75	-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max				100	mA
		I_{CCL}	V_{CC} = Max, V_{IL} = 0.5V				145	mA
		I_{CCZ}	V_{CC} = Max, V_{IL} = 0.5V				100	mA
I_{OFF}	Power-off output current	B_0 - B_7	B_n = 2.1V, V_{CC} = 0.0V, V_{IL} = Max, V_{IH} = Min				100	µA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A SIDE LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = 5V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B to A	Waveform 1, 2	5.5 6.0	7.5 8.5	12.0 10.5	4.5 6.0	13.0 11.5	ns ns
t_{PZH} t_{PZL}	Output Enable time from High or Low OEA to A	Waveform 3, 4	8.0 8.5	10.5 12.0	14.5 14.5	7.0 8.5	16.5 18.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low OEA to A	Waveform 3, 4	2.0 2.0	4.5 4.5	7.0 7.5	2.0 2.0	7.5 8.0	ns ns

SYMBOL	PARAMETER	TEST CONDITION	B SIDE LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_A = -55°C to +125°C, V_{CC} = 5V ± 10%, C_D = 30pF, R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A to B	Waveform 1, 2	2.0 3.5	4.0 5.5	7.0 8.0	1.5 2.5	9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}$ to B	Waveform 1, 2	3.0 4.0	5.0 6.0	8.5 9.0	2.0 3.0	11.5 9.5	ns ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}_n$ to B	Waveform 1, 2	2.0 4.5	4.5 7.5	7.5 10.0	1.5 3.5	8.5 10.5	ns ns
t_{TLH} t_{THL}	Transition time, B side 1.3V to 1.7V, 1.7V to 1.3V	Test Circuit and Waveform	0.5 0.5	2.0 2.0	4.5 4.5	0.5 0.5	4.5 4.5	ns ns

AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_D = 30pF, R_U = 9Ω			T_A = -55°C to +125°C, V_{CC} = 5V ± 10%, C_D = 30pF, R_u = 9Ω		
			Min	Typ	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Set-up time A to $\overline{LE}$	Waveform 5	5.0 5.0			5.0 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time A to $\overline{LE}$	Waveform 5	0.0 0.0			0.0 0.0		ns ns
$t_w(L)$	$\overline{LE}$ Pulse width Low	Waveform 5	10.0			10.0		ns

NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode. Unless otherwise specified, $V_X = V_{CC}$ for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} = 1.9V and for V_{IL} = 1.2V, however, the specified test limits and conditions are guaranteed.

Pi-Bus Transceiver | 54F776

FUNCTION TABLE

INPUTS						LATCH	OUTPUTS		MODE
A_n	B_n(3)	$\overline{LE}$	OEA	$\overline{OEB}_0$	$\overline{OEB}_1$	STATE	A_n	B_n	
H	X	L	L	L	L	H	Z	H	A 3-State, Data from A to B
L	X	L	L	L	L	L	Z	L	
X	X	H	L	L	L	Q_n	Z	Q_n	A 3-State, Latched data to B
-	-	L	H	L	L	(1)	(1)	(1)	Feedback: A to B, B to A
-	H	H	H	L	L	H(2)	H	Off(2)	Preconditioned Latch enabling data
-	L	H	H	L	L	H(2)	L	Off(2)	transfer from B to A
-	-	H	H	L	L	Q_n	Q_n	Q_n	Latch state to A and B
H	X	L	L	H	X	H	Z	Off	B Off and A 3-State
L	X	L	L	H	X	L	Z	Off	
X	X	H	L	H	X	Q_n	Z	Off	
-	H	L	H	H	X	H	H	Off	B Off, Data from B to A
-	L	L	H	H	X	L	L	Off	
-	H	H	H	H	X	Q_n	H	Off	
-	L	H	H	H	X	Q_n	L	Off	
H	X	L	L	X	H	H	Z	Off	B Off and A 3-State
L	X	L	L	X	H	L	Z	Off	
X	X	H	L	X	H	Q_n	Z	Off	
-	H	L	H	X	H	H	H	Off	B Off, Data from B to A
-	L	L	H	X	H	L	L	Off	
-	H	H	H	X	H	Q_n	H	Off	
-	L	H	H	X	H	Q_n	L	Off	

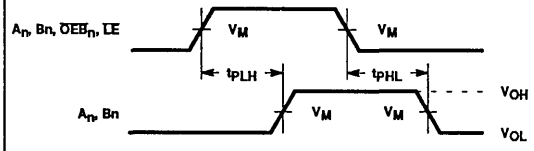
NOTES:
H = High voltage level
L = Low voltage level
X = Don't care
- = Input not externally driven
Z = High Impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transititon
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}_0$ and $\overline{OEB}_1$ are Low and $\overline{LE}$ is High
(3) = Precaution should be taken to insure that the B inputs do not float. If they do, they are equal to a Low state
off = Applies to "B" (OC) outputs only. Indicates that the outputs are turned off

CONTROLLED POWER SEQUENCING OPERATION

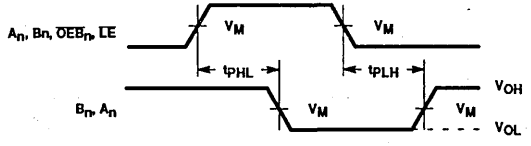
The F776 has a design feature which controls the output transitions during power up (or down). There are two possible conditions that occur.

6. When $\overline{LE}$ = Low and $\overline{OEB}_n$ = Low, the B outputs are disabled until the $\overline{LE}$ circuit can take control. This feature insures that the B outputs will follow the A inputs and allow only one transition during power up (or down).
7. If $\overline{LE}$ = High or $\overline{OEB}_n$ = High, then the B outputs will remain disabled during power up (or down).

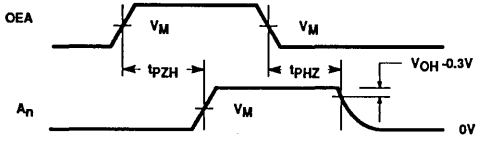
AC WAVEFORMS



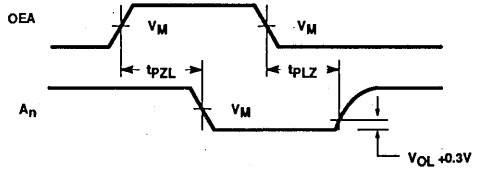
Waveform 1. Propagation Delay for Data to Output



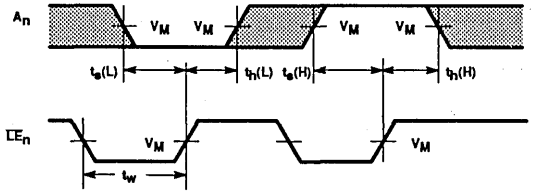
Waveform 2. Propagation Delay for Data to Output



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



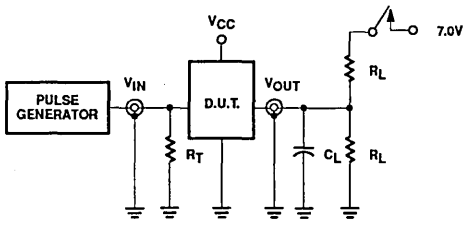
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



Waveform 5. Data Setup and Hold Times

NOTE: For all waveforms $V_M = 1.5V$
The shaded areas indicate when the input is permitted to change for predictable output performance.

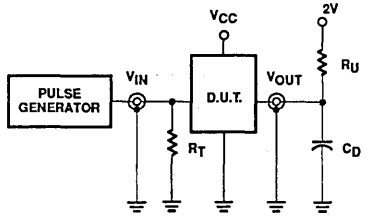
TEST CIRCUITS AND WAVEFORM



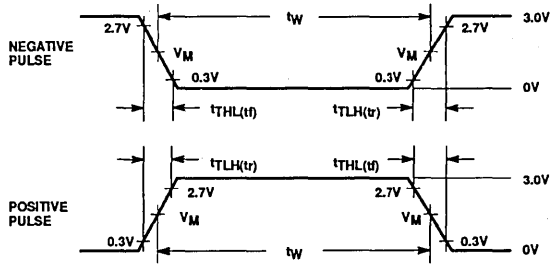
Test Circuit for 3-State Outputs on A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open



Test Circuit for 3-State Outputs on B Port



Input Pulse Definition

FAMILY 54F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Side	3.0V	0.0V	1MHz	500ns	≤2.5ns	≤2.5ns
B Side	2.0V	1.0V	1MHz	500ns	≤4.0ns	≤4.0ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capicitance includes jig and probe capicitance; see AC Characteristics for value.
R_U = Pull up resistor; see AC Characteristics for value.

Signetics

54F777

Triple Bidirectional Latched Bus Transceiver

(3-State + Open Collector)

Product Specification

Military FAST Products

FEATURES

- **Latching Transceiver**
- **High drive open collector output current with minimum output swing**
- **Compatible with Test Mode (TM) Bus specification**
- **Controlled output ramp**
- **Multiple package options**

DESCRIPTION

The 54F777 is a triple bidirectional latched Bus transceiver and is intended to provide the electrical interface to a high performance wired-OR bus. This bus has a loaded characteristics impedance range of 20 to 50 ohms and is terminated on each end with a 30 to 40 ohm resistor.

The 54F777 is a triple bidirectional transceiver with open collector B and 3-state A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100 mA from 2 volts to minimize crosstalk and ringing on the bus.

A separate output threshold clamp voltage (V_X) is provided to prevent the A port output High level from exceeding future high density processor supply voltage levels. For 5 volt systems, V_X is simply tied to V_{CC}.

ORDERING INFORMATION

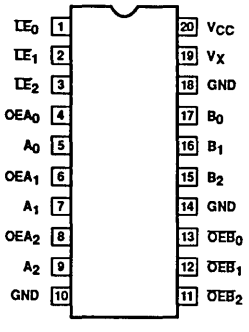
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP (300mil)	54F777/BRA
20-Pin Flat Pack	54F777/BSA
20-Pin Ceramic LLCC	54F777/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_2	PNP latched inputs	3.5/0.117	70μA/70μA
B_0 - B_2	Data inputs with threshold circuitry	5.0/0.167	100μA/100μA
OEA_0 - OEA_2	A Output Enable inputs (active High)	1.0/0.033	20μA/20μA
$\overline{OEB}_0$ - $\overline{OEB}_2$	B Output Enable inputs (active Low)	1.0/0.033	20μA/20μA
$\overline{LE}_0$ - $\overline{LE}_2$	Latch Enable inputs (active Low)	1.0/0.033	20μA/20μA
A_0 - A_2	3-State outputs	150/40	3mA/24mA
B_0 - B_2	Open collector outputs	OC*/166.7	OC*/100mA

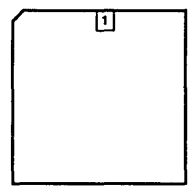
NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
* OC = Open Collector

PIN CONFIGURATION



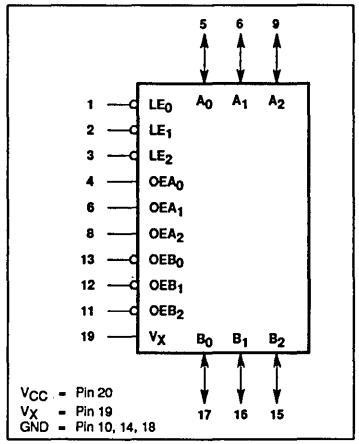
For LLCC Pin Assignment, see JEDEC Std. No. 2

PIN CONFIGURATION LLCC

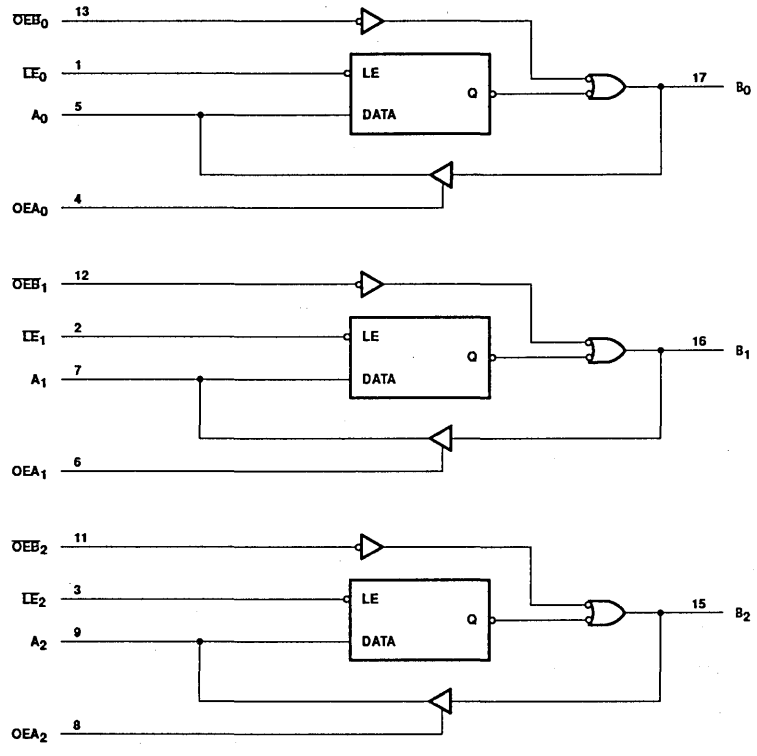


PIN	Function	Pin	Function
1	$\overline{LE}_0$	11	$\overline{OEB}_2$
2	$\overline{LE}_1$	12	$\overline{OEB}_1$
3	$\overline{LE}_2$	13	$\overline{OEB}_0$
4	OEA_0	14	GND
5	A_0	15	B_2
6	OEA_1	16	B_1
7	A_1	17	B_0
8	OEA_2	18	GND
9	A_2	19	V_X
10	GND	20	V_{CC}

LOGIC SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 20
V_X = Pin 19
GND = Pin 10, 14, 18

FUNCTION TABLE

INPUTS					LATCH STATE	OUTPUTS		MODE
A_n	B_n*	$\overline{LE}_n$	OEA_n	$\overline{OEB}_n$		A_n	B_n	
H	X	L	L	L	H	Z	H**	A 3-state, Data From A To B
L	X	L	L	L	L	Z	L	
X	X	H	L	L	Q_n	Z	Q_n	A 3-state, Latched data to B
-	-	L	H	L	(1)	(1)	(1)	Feedback: A to B, B to A
-	H	H	H	L	H(2)	H	Z(2)	Preconditioned Latch enabling data transfer from B to A
-	L	H	H	L	H(2)	L	Z(2)	
-	-	H	H	L	Q_n	Q_n	Q_n	Latch state to A and B
H	X	L	L	H	H	Z	Z	B and A 3-state
L	X	L	L	H	L	Z	Z	
X	X	H	L	H	Q_n	Z	Z	
-	H	L	H	H	H	H	Z	B 3-state, Data from B to A
-	L	L	H	H	L	L	Z	
-	H	H	H	H	Q_n	H	Z	
-	L	H	H	H	Q_n	L	Z	

H = High voltage level
L = Low voltage level
X = Don't care
- = Input not externally driven
Z = High impedance (off) state
Q_n = High or Low voltage level one setup time prior to the Low-to-High $\overline{LE}$ transition
(1) = Condition will cause a feedback loop path; A to B and B to A
(2) = The latch must be preconditioned such that B inputs may assume a High or Low level while $\overline{OEB}_0$ and $\overline{OEB}_1$ are Low and $\overline{LE}$ is High
H** = Goes to level of pullup voltage
B* = Precaution should be taken to insure the B inputs do not float. If they do they are equal to Low state

NOTE: Each latch is independent. The latches may be run in any combination of modes.

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_X	Threshold control		-0.5 to +7.0	V
V_{IN}	Input voltage range	$\overline{OEB}_n$, OEA_n, $\overline{LE}n$	-0.5 to +7.0	V
		A_0 -A_2, B_0 - B_2	-0.5 to +5.5	V
I_{IN}	Input current range		-30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state range		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0 - A_2	40	mA
		B_0 - B_2	200	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage	Except B_0 - B_2	2.0			V
		B_0 - B_2	1.60			V
V_{IL}	Low-level input voltage	Except B_0 - B_2			0.8	V
		B_0 - B_2			1.43	V
I_{IK}	Input clamp current	Except A_0 - A_2			-18	mA
		A_0 - A_2			-40	mA
I_{OH}	High-level output current	A_0 - A_2			-3	mA
I_{OL}	Low-level output current	A_0 - A_2			20	mA
		B_0 - B_2			90	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High level output current	B_0 - B_2	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min, V_{OH} = 2.1V				100	µA
I_{OFF}	Power-off output current	B_0 - B_2	V_{CC} = 0.0V, V_{IL} = Max, V_{IH} = Min, V_{OH} = 2.1V				100	µA
V_{OH}	High-level output voltage	A_0 - A_2[4]	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OH} = -3mA, V_X = V_{CC}	2.4	2.5	V_{CC}	V
				I_{OH} = -0.4mA, V_X = 3.13V & 3.47V	2.5		V_X	V
V_{OL}	Low-level output voltage	A_0 - A_2[4]	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 20mA, V_X = V_{CC}			0.50	V
		B_0 - B_2		I_{OL} = 100mA			1.15	V
				I_{OL} = 4mA	0.40			V
V_{IK}	Input clamp voltage	A_0 - A_2	V_{CC} = Min, I_I = I_{IK}				-0.5	V
		Except A_0 - A_2					-1.2	V
I_I	Input current at maximum input voltage	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} = Max, V_I = 7.0V				100	µA
		A_0 - A_2, B_0 - B2	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High-level input current	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} = Max, V_I = 2.7V, B_n - A_n = 0V				20	µA
		B_0 - B_2	V_{CC} = Max, V_I = 2.1V				100	µA
I_{IL}	Low-level input current	$\overline{OEB}_n$, OEA_n, $\overline{LE}_n$	V_{CC} = Max, V_I = 0.5V				-20	µA
		B_0 - B_2	V_{CC} = Max, V_I = 0.3V				-100	µA
I_{OZH} + I_{IH}	Off-state current, High-level voltage applied	A_0 - A_2	V_{CC} = Max, V_O = 2.7V				70	µA
I_{OZL} + I_{IL}	Off-state current, Low-level voltage applied	A_0 - A_2	V_{CC} = Max, V_O = 0.5V				-70	µA
I_X	High-level control current		V_{CC} = Max, V_X = V_{CC}, $\overline{LE}$ = OEA_n = $\overline{OEB}_n$ = 2.7V, A_0 - A_2 = 2.7V, B_0 - B_2 = 2.0V		-100		100	µA
			V_{CC} = Max, V_X = 3.13V & 3.47V $\overline{LE}$ = OEA_n = $\overline{OEB}_n$ = 2.7V, A_0 -A_7 = 2.7V, B_0 - B_2 = 2.0V		-10		10	mA
I_{OS}	Short-circuit output current[3]	A_0 - A_2 only	V_{CC} = Max, B_n = 1.8V, OEA_n = 2.0V, $\overline{OEB}_n$ =2.7V		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			40	60	mA
		I_{CCL}	V_{CC} = Max, V_{IL} = 0.5V			55	80	mA
		I_{CCZ}				45	67	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	A PORT LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay B_n to A_n	Waveform 1	8.5 7.5	10.5 9.5	13.0 12.0	5.0 7.5	15.0 14.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low $\overline{OEA}_n$ to A_n	Waveform 3, 4	8.0 9.0	10.0 11.0	13.0 14.0	7.0 8.0	16.0 16.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low $\overline{OEA}_n$ to A_n	Waveform 3, 4	1.5 1.5	3.0 3.0	6.0 6.0	1.0 1.0	6.5 6.5	ns ns
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**B PORT LIMITS**					**UNIT**
			T_A = +25°C, V_{CC} = +5.0V, C_D = 30pF, R_U = 9Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_D = 30pF, R_U = 9Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	Waveform 1	3.0 5.0	4.5 6.5	7.0 9.0	1.5 4.0	10 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{LE}_n$ to B_n	Waveform 1	3.5 5.5	5.5 7.5	8.0 10.5	2.0 5.0	11.5 12.0	ns ns
t_{PLH} t_{PHL}	Enable/disable time $\overline{OEB}_n$ to B_n	Waveform 1	3.0 6.0	5.0 8.0	7.5 10.5	2.0 5.5	10.0 12.5	ns ns
t_{PLH} t_{PHL}	Transition time, B Port 1.3V to 1.7V, 1.7V to 1.3V	Test Circuit and Waveform	0.5[5] 0.5[5]	4.0 2.0	4.5[5] 4.5[5]	0.5[5] 0.5[5]	7.0[5] 4.5[5]	ns ns

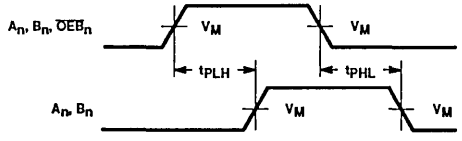
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time A_n to $\overline{LE}_n$	Waveform 2	4.0 4.5			4.5 4.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time A_n to $\overline{LE}_n$	Waveform 2	0.0 0.0			0.0 0.0		ns ns
$t_w(L)$	$\overline{LE}_n$ Pulse width, Low	Waveform 2	5.5			7.0		ns

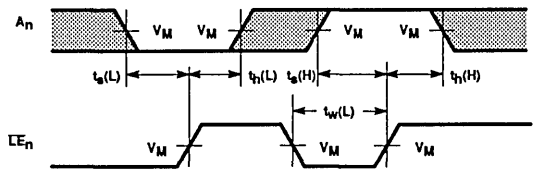
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type. Unless otherwise specified, $V_X = V_{CC}$ for all test conditions.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Due to test equipment limitations, actual test conditions are for V_{IH} = 1.8V and V_{IL} = 1.3V.
5. Guaranteed, but not tested.

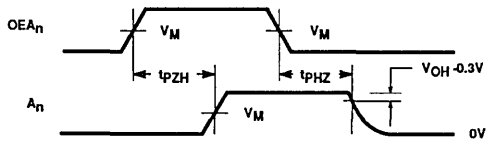
AC WAVEFORMS



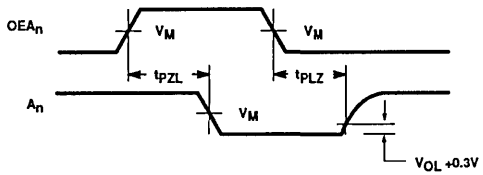
Waveform 1. Propagation Delayfor Data to Output and Enable/Disable Time $\overline{OEB}_n$ to B_n



Waveform 2. Data Setup and Hold Times and $\overline{LE}$ Pulse Width



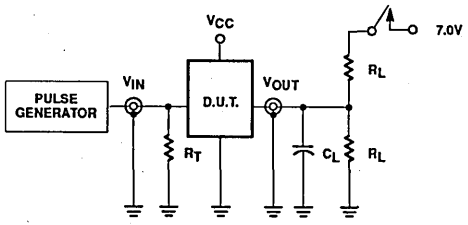
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

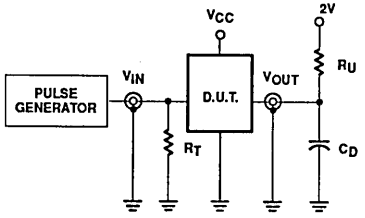
TEST CIRCUIT AND WAVEFORMS



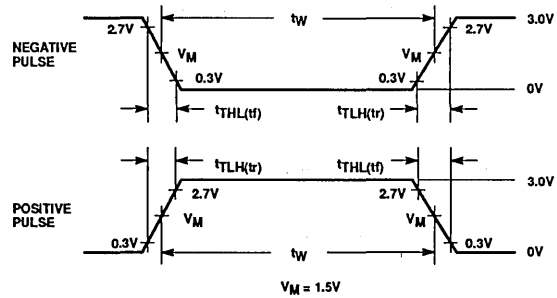
Test Circuit for 3-State Outputs on A Port

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed
	open



Test Circuit for 3-State Outputs on B Port



Input Pulse Definition

FAMILY 54F	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	t_W	t_{TLH}	t_{THL}
A Side	3.0V	0.0V	1MHz	500ns	≤2.5ns	≤2.5ns
B Side	2.0V	1.0V	1MHz	500ns	≤4.0ns	≤4.0ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
C_D = Load capicitance includes jig and probe capicitance; see AC Characteristics for value.
R_U = Pull up resistor; see AC Characteristics for value.

Signetics

Military Logic Products

54F779
Counter

8-Bit Bidirectional Binary Counter (3-State)

Product Specification

FEATURES

- **Multiplexed 3-state I/O ports for bus oriented applications**
- **Built-in carry look-ahead capability**
- **Center power pins to reduce efforts of package inductance**
- **Count frequency: 145 MHz typical**
- **Supply current: 90mA typical**
- **See 54F269 for 24-pin separate I/O port version**
- **See 54F579 for 20-pin version**

DESCRIPTION

The 54F779 is a fully synchronous 8-state up/down counter with multiplexed 3-state I/O ports for bus-oriented applications.

All functions (hold, count up, count down, synchronous load) are controlled by two Select pins (S_0 and S_1). The device also features carry look-ahead for easy cascading. All state changes are initiated by the rising edge of the clock.

When $\overline{CET}$ is High the data outputs are held in their current state and $\overline{TC}$ is held High. The $\overline{TC}$ output is not recommended for use as a clock or asynchronous reset due to the possibility of decoding spikes.

ORDERING INFORMATION

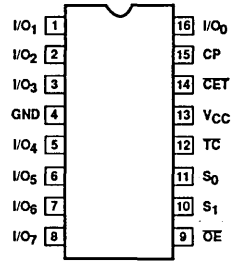
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F779/BEA
16-Pin Ceramic Flat Pack	54F779/BFA
20-Pin Ceramic LLCC	54F779/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

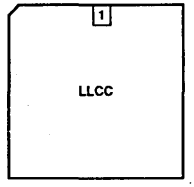
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I/O_0	Data inputs	3.5/1.0	70μA/0.6mA
	Data outputs	150/40	3mA/20mA
S_0, S_1	Select inputs	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output Enable input (Active Low)	1.0/1.0	20μA/0.6mA
$\overline{CET}$	Count Enable Trickle input (Active Low)	1.0/1.0	20μA/0.6mA
CP	Clock pulse input (Active rising edge)	1.0/1.0	20μA/0.6mA
$\overline{TC}$	Terminal count output (Active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

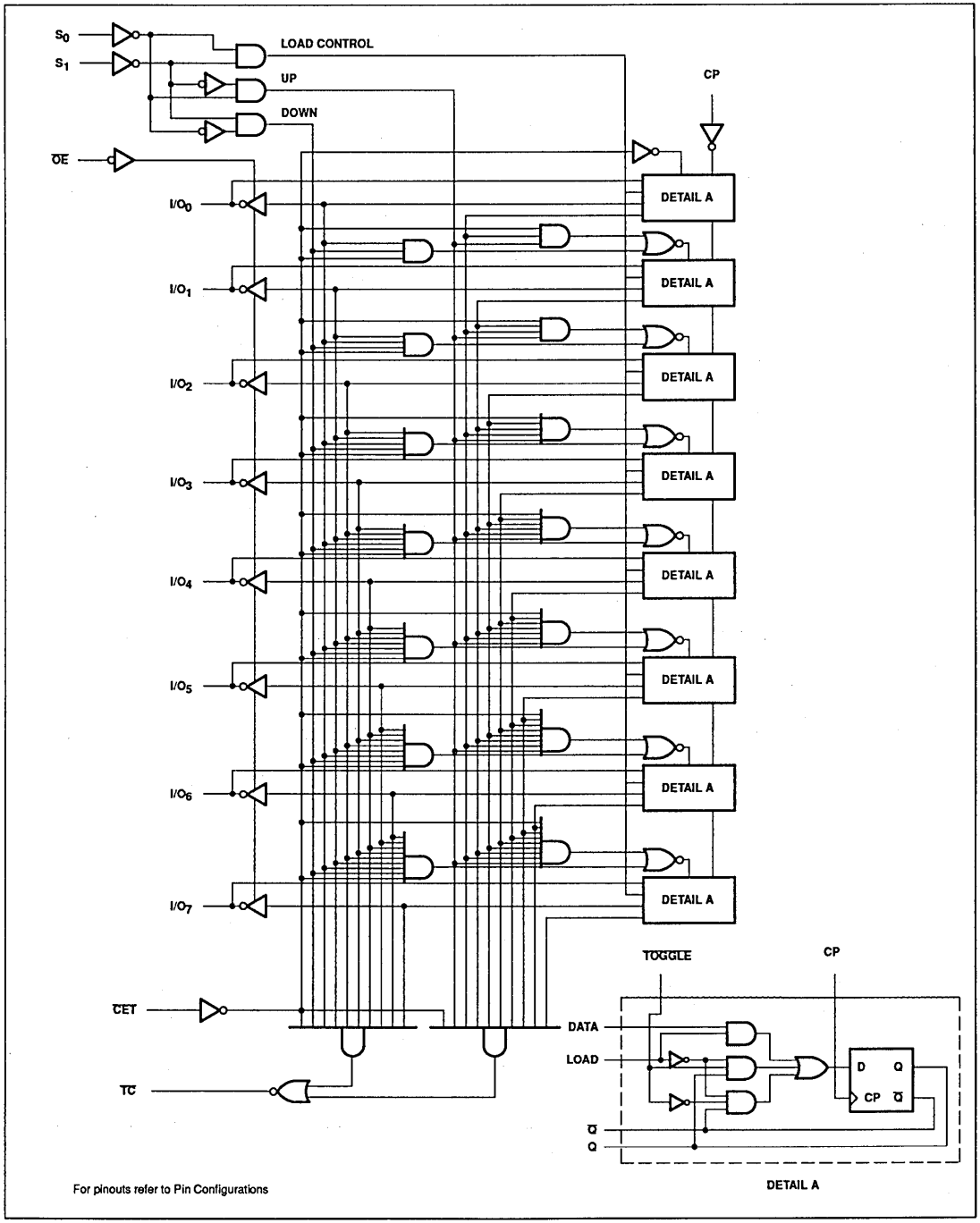


PIN CONFIGURATION



PIN	Function	Pin	Function
1	NC	11	I/O_4
2	$\overline{CET}$	12	I/O_5
3	CP	13	I/O_6
4	I/O_0	14	I/O_7
5	NC	15	$\overline{OE}$
6	NC	16	NC
7	I/O_1	17	S_1
8	I/O_2	18	S_0
9	I/O_3	19	$\overline{TC}$
10	GND	20	V_{CC}

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OPERATING MODE
S_1	S_0	$\overline{CET}$	$\overline{OE}$	CP	
X	X	X	H	X	I/O_0 to I/O_7 in Hi-Z
X	X	X	L	X	Flip-flop output appears on I/O_n lines
L	L	X	H	↑	Parallel load all flip-flops
(not LL)		H	X	↑	Hold ($\overline{TC}$ held High)
H	L	L	X	↑	Count up
L	H	L	X	↑	Count down

H = High voltage level steady state
L = Low voltage level steady state
X = Don't care
↑ = Low-to-High clock transition
(not LL) = S_0 and S_1 should never be Low voltage level at the same time in hold mode only

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage[4]		2.0			V
V_{IL}	Low-level input voltage[4]				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	$\overline{TC}$, I/O_n			-1.0	mA
		I/O_n			-3.0	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	$\overline{TC}$	V_{CC} = Min,	I_{OH} = -1mA	2.5			V
		I/O_n	V_{IL} = Max,	I_{OH} = -3mA	2.4			V
			V_{IH} = Min	I_{OH} = -1mA	2.5	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, I_{OL} = Max, V_{IH} = Min			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum	I/O_n	V_{CC} = Max, V_I = 5.5V				1.0	mA
	input voltage	others	V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current	except	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	I/O_n	V_{CC} = Max, V_I = 0.5V				-0.6	mA
I_{OZH} + I_{IH}	Off-state current High-level voltage applied	I/O_n	V_{CC} = Max, V_{IH} = Min, V_I = 2.7V				70	µA
I_{OZL} + I_{IL}	Off-state current Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_I = 0.5V				-600	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			82	116	mA
		I_{CCL}				91	128	mA
		I_{CCZ}				97	136	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	125	145		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to I/O_n	Waveform 1	4.5 5.5	7.0 8.0	10.5 10.5	4.5 5.5	11.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$	Waveform 1	4.5 4.5	7.0 7.0	9.0 9.0	4.5 4.5	10.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 2	3.0 3.0	4.5 5.5	6.5 7.5	2.5 2.5	8.5 8.5	ns ns
t_{PZH} t_{PZL}	Enable time to High or Low level	Waveform 4 Waveform 5	2.5 4.5	4.5 6.5	7.0 9.0	2.5 4.5	9.0 10.0	ns ns
t_{PHZ} t_{PLZ}	Disable time from High	Waveform 4 Waveform 5	1.0 1.0	3.0 4.0	6.5 7.0	1.0 1.0	9.0 9.0	ns ns

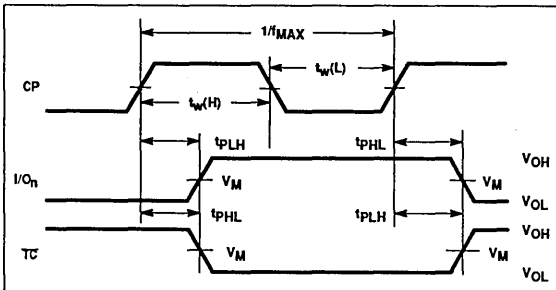
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low I/O_n to CP	Waveform 3	5.0 5.0			5.0 5.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low I/O_n to CP	Waveform 3	1.0 1.0			1.0 1.0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CET}$ to CP	Waveform 3	5.0 7.0			8.0 10.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CET}$ to CP	Waveform 3	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low S_n to CP	Waveform 3	8.0 8.0			11.0 11.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low S_n to CP	Waveform 3	0 0			0 0		ns ns
$t_w(H)$ $t_w(L)$	CP pulse width	Waveform 1	4.0 4.0			4.0 5.0		ns ns

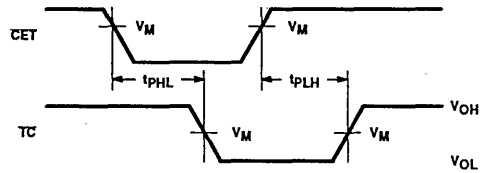
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.
4. When testing devices to the functional table specified, refer to the 'Recommended Operating Conditions' section of Application Note 202, "Testing and Specifying FAST Logic".

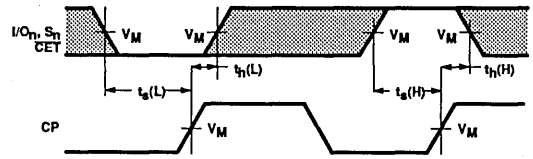
AC WAVEFORMS



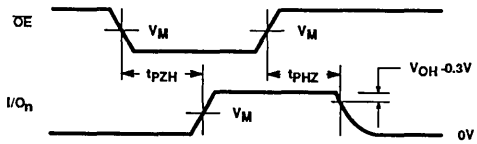
Waveform 1. Propagation Delay, Clock Input to Output Clock Widths and Maximum Clock Frequency



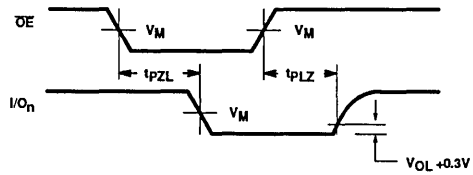
Waveform 2. Propagation Delay, $\overline{CET}$ Input to Terminal Count Output



Waveform 3. Set-up and Hold times



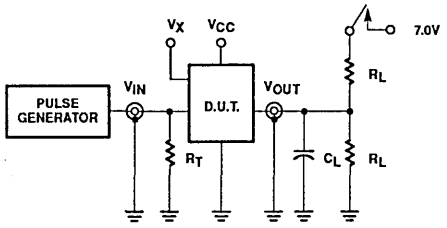
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



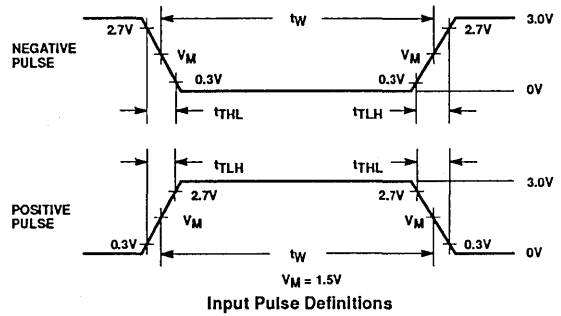
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: For all waveforms V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

54F1240
Buffers

54F1240 Octal Inverter Buffer (3-State)

Product Specification

Military Logic Products

FEATURES

- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Low power, light bus loading**
- **Functional pin for pin equivalent of 54F240**
- **1/30th the bus loading of 54F240**
- **Provides ideal interface and increases fan-out of MOS microprocessors**
- **Octal bus interface**
- **3-State buffer outputs sink 48mA**
- **12mA source current**

DESCRIPTION

The 54F1240 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are capable of sinking 48mA and sourcing up to 12mA, producing very good capacitive drive characteristics. The device features two Output Enables, $\overline{OE}_n$, each controlling four of the 3-State outputs.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54F1240/BRA
20-Pin Ceramic FlatPack	54F1240/BSA
20-Pin Ceramic LLCC	54F1240/B2A

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_{an}$	$\overline{Y}_{bn}$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

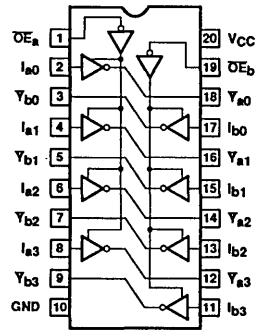
H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance (OFF) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{OE}_a$, $\overline{OE}_b$	3-State output enable input (active-Low)	1.0/0.033	20μA/20μA
OE_b	3-State output enable input (active-High)	1.0/0.033	20μA/20μA
I_{a0} - I_{a3}, I_{b0} - I_{b3}	Data inputs	1.0/0.033	20μA/20μA
$\overline{Y}_{a0}$ - $\overline{Y}_{a3}$, $\overline{Y}_{b0}$ - $\overline{Y}_{b3}$	Data outputs	600/80	12mA/48mA

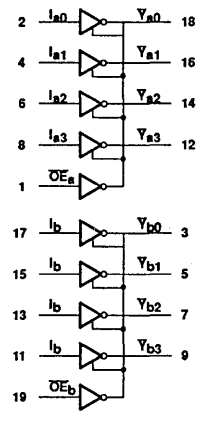
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	96	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage[4]	2.0			V
V_{IL}	Low-level input voltage[4]			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-1	mA
I_{OH2}	High-level output current			-3	mA
I_{OH3}	High-level output current			-12	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min,	I_{OH2} = -3mA	2.4			V
			V_{IL} = Max,	I_{OH1} = -1mA	2.5	3.4		V
			V_{IH} = Min	I_{OH3} = -12mA	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} =48mA		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = 0.0V, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-1	-20	µA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			2	50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V			-2	-50	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max		-100		-225	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			22	30	mA
		I_{CCL}				58	75	mA
		I_{CCZ}				44	58	mA

AC ELECTRICAL CHARACTERISTICS

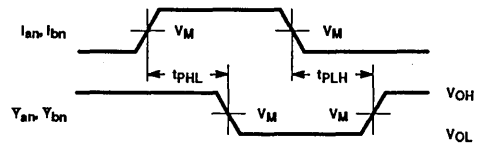
(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1	3.0 1.5	4.5 2.5	6.5 4.5	2.5 1.5	8.0 5.5	ns
t_{PZH} t_{PZL}	Data to output Output enable time	Waveform 2 Waveform 3	3.0 4.0	5.5 70	7.5 9.0	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output disable time From High or Low	Waveform 2 Waveform 3	2.0 2.0	4.0 4.0	6.0 5.5	2.0 2.0	7.0 6.5	ns

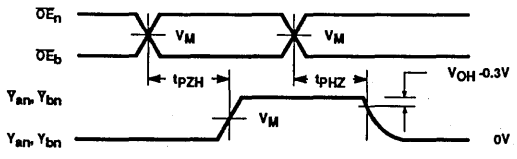
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. When testing devices to the functional table specified refer to the 'Recommended Operating Conditions' section of Applications Note 202, "Testing and Specifying FAST™ Logic".

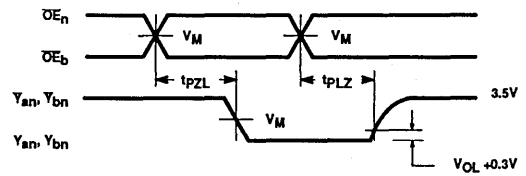
AC WAVEFORMS



Waveform 1. Propagation Delay Data to Output



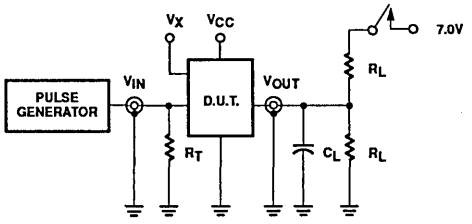
Waveform 2. 3-State Output Enable Time To High Level And Output Disable Time From High Level



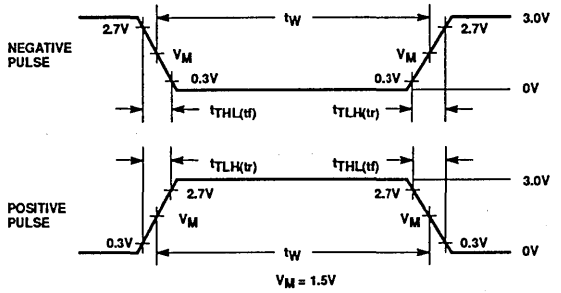
Waveform 3. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	closed open

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

54F3037
30Ω Line Driver

Quad 2-Input NAND 30Ω Line Driver

Product Specification

Military Logic Products

FEATURES

- **30Ω line driver**
- **160mA output drive capability in the Low-state**
- **67mA output drive capability in the High-state**
- **High speed**
- **Facilitates incident wave switching**
- **3nh lead inductance each on V_{CC} and GND when both side pins are used**

DESCRIPTION

The 54F3037 is a high current Line driver composed of four 2-input NAND gates. It has been designed to deal with the transmission line effects of PC boards which appear when fast edge rates are used.

The drive capability of the 54F3037 is 67mA source and 160mA sink with a V_{CC} as low as 4.5 volts. This guarantees incident wave switching with V_{OH} not less than 2.0V and V_{OL} not more than 0.8V while driving impedances as low as 30Ω. This is applicable with any combination of outputs using continuous duty.

The propagation delay of the part is minimally affected by reflections when terminated only by the TTL inputs of other devices. Performance may be improved by full or partial line termination.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F3037/BEA
16-Pin Ceramic FlatPack	54F3037/BFA
20-pin Ceramic LLCC	54F3037/B2A

FUNCTION TABLE

INPUTS		OUTPUT
A	B	$\overline{Y}$
L	L	H
L	H	H
H	L	H
H	H	L

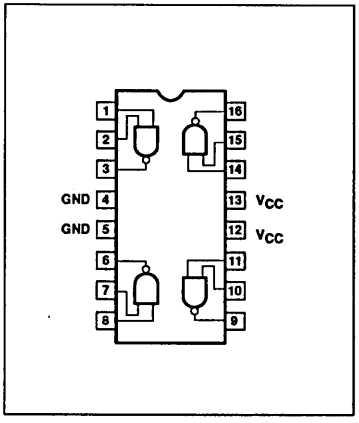
H = High voltage level
L = Low voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

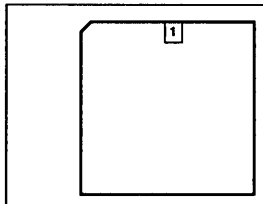
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A, B	Data inputs	1.0/1.0	20μA/0.6mA
$\overline{Y}$	Data outputs	3350/266	67mA/160mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High-state and 0.6mA in the Low-state.

PIN CONFIGURATION

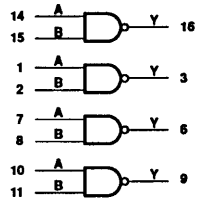


LLCC PIN CONFIGURATION



PIN	FUNCTION	PIN	FUNCTION
1	N/C	11	N/C
2	V_{CC}	12	GND
3	INPUT	13	OUTPUT
4	INPUT	14	INPUT
5	OUTPUT	15	INPUT
6	N/C	16	N/C
7	INPUT	17	OUTPUT
8	INPUT	18	INPUT
9	OUTPUT	19	INPUT
10	GND	20	V_{CC}

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
I_O	Current applied to output in Low output state	320	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-67	mA
I_{OL}	Low-level output current			160	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

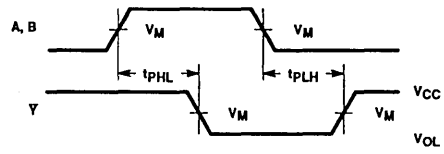
SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max,	I_{OH} = -45mA	2.5			V
			V_{IH} = Min	I_{OH1} = -67mA[3]	2.0			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max,	I_{OL} = 100mA		.40	.55	V
			V_{IH} = Min	I_{OL} = 160mA[4]			.80	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V			-0.4	-0.6	mA
I_O[5]	Short-circuit output current		V_{CC} = Max, V_O = 2.25V		-60		-200	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			3.5	9.0	mA
		I_{CCL}				27	40	mA

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202 "Testing and Specifying FAST Logic."

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A, B to $\overline{Y}$	Waveform 1	1.0 1.0	4.5 3.0	6.0 6.0	1.0 1.0	7.0 6.0	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OH1} is the current necessary to guarantee the Low to High transition in a 30Ω transmission line on the incident wave.
4. I_{OL1} is the current necessary to guarantee the High to Low transition in a 30Ω transmission line on the incident wave.
5. I_O is tested under conditions that produce current approximately one half of the true short-circuit output current (I_{OS}).

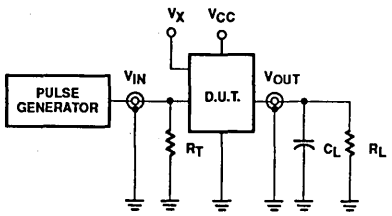
AC WAVEFORM



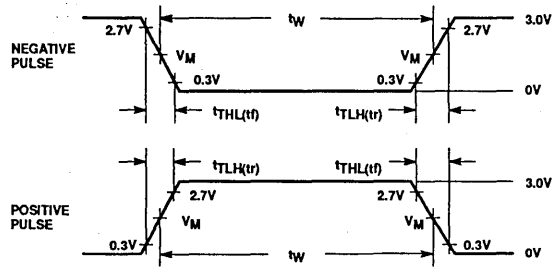
Waveform 1. For Non-Inverting Outputs

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F5074
Flip-Flop

Synchronizing Dual D-Type Flip-Flop with Metastable Immune Characteristics

Objective Specification

FEATURES

- **Metastable Immune Characteristics**
- **Propagation delay skew and output to output skew guaranteed less than 1.5ns**

DESCRIPTION

The 54F5074 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also true and complementary outputs.

Set ($\overline{S}_{Dn}$) and Reset ($\overline{R}_{Dn}$) are asynchronous active-Low inputs and operate independently of the Clock (CP_n) input. Data must be stable just one setup time prior to the Low-to-High transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the D_n input may be changed without affecting the levels of the output.

The 54F5074 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup and hold times are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 54F5074 are $\tau \cong 135ps$ and $T_o \cong 9.8 \times 10^6$ sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_o represents a function of the measurement of the propensity of a latch to enter a metastable state.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F5074/BEA

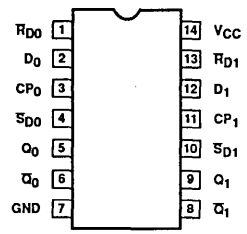
TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
54F5074	120MHZ	20mA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

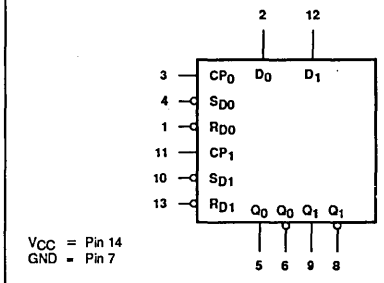
PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0, D_1	Data inputs	1.0/0.417	20μA/250μA
CP_0, CP_1	Clock inputs (active rising edge)	1.0/0.033	20μA/20μA
$\overline{S}_{D0}$, $\overline{S}_{D1}$	Set inputs (active Low)	1.0/0.033	20μA/20μA
$\overline{R}_{D0}$, $\overline{R}_{D1}$	Reset inputs (active Low)	1.0/0.033	20μA/20μA
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data outputs	750/33	15mA/20mA

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION



LOGIC SYMBOL



Metastable Immune Characteristics

Signetics uses the term 'metastable immune' to describe characteristics of some of the products in its FAST family. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations. This claim is easily verified on the 54F5074. By running two independent signal generators (see Figure 1) at nearly the same frequency (in this case 10 MHz clock and 10.02 MHz data) the device-under-test can often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistance to the $\overline{Q}$ output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

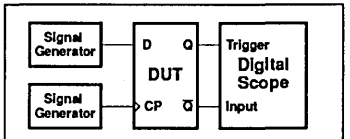


Figure 1. Test Setup

When the device-under-test is a 54F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Figure 2.

Figure 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5 volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output

COMPARISON OF METASTABLE IMMUNE AND NON-IMMUNE CHARACTERISTICS

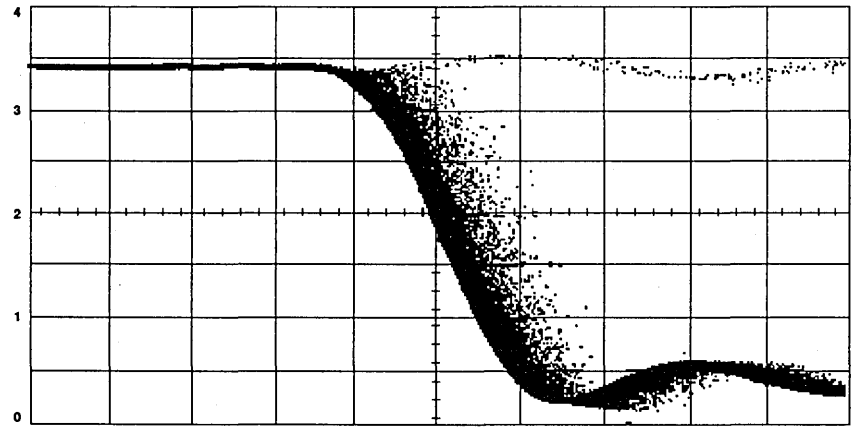


Figure 2. 54F74 $\overline{Q}$ Output Triggered by Q Output, Setup and Hold Times Violated

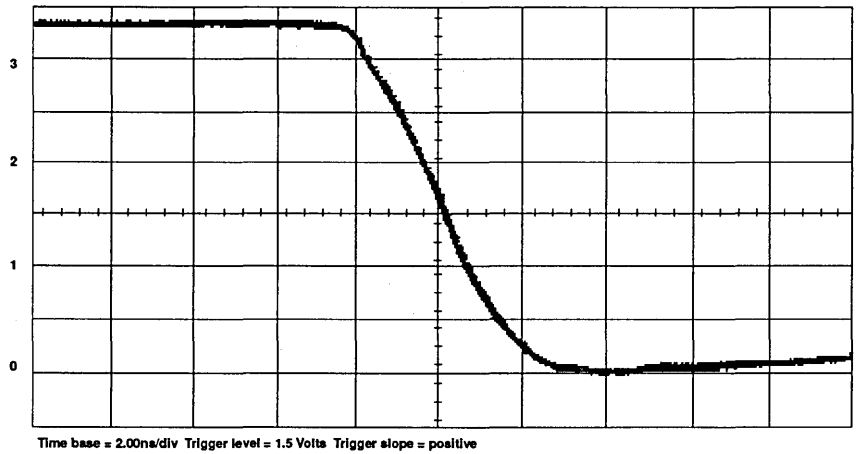


Figure 3. 54F74 $\overline{Q}$ Output Triggered by Q Output, Setup and Hold Times Violated

did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

When the device-under-test is a metastable immune part, such as the 54F5074, the waveform will appear as in Figure 3. The 54F5074 $\overline{Q}$ output will not vary with respect to the Q trigger point even when the part is driven into a metastable state. Any tendency towards internal metastability is resolved by Signetics patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased Clock-to-Q/$\overline{Q}$ propagation delay. This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_o.

The metastability characteristics of the 54F5074 and related part types represent state-of-the-art in TTL technology.

After determining the T_o and τ of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 54F5074 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 54F5074 10 nanoseconds after the clock edge. He simply plugs his numbers into the equation following:

$$MTBF = e^{(t'/\tau)}/T_o f_C f_I$$

In this formula, f_C is the frequency of the clock, F_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t'>h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency or 20mHz because input events consist of both low and high data transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Figure 4 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula the actual MTBF is 1.51×10^{10} seconds or about 480 years.

MEAN TIME BETWEEN FAILURES (MTBF) vs. t'

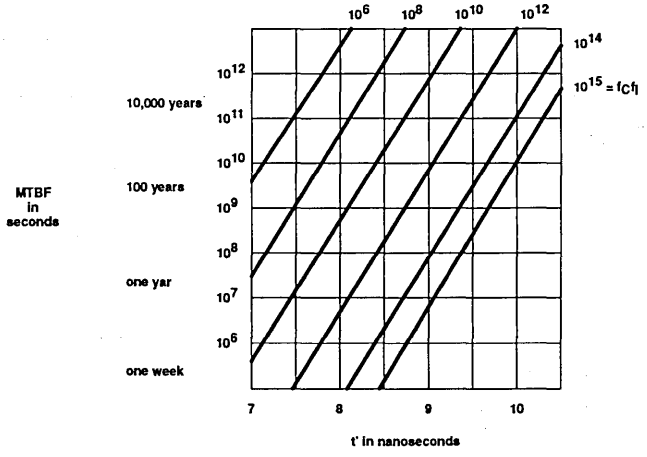


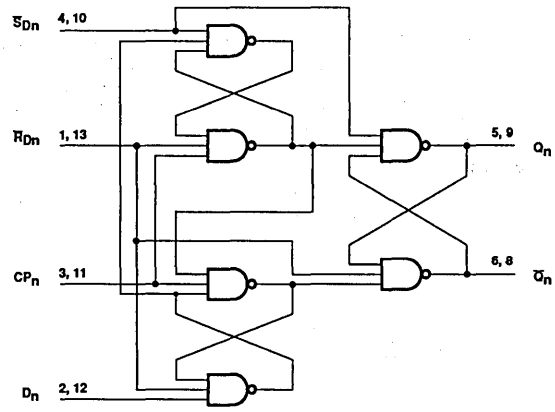
Figure 4. MTBF vs. t' for 54F5074 at τ = 135ps and $T_o = 9.8 \times 10^6$ sec

TYPICAL VALUES FOR τ AND To AT VARIOUS V_{CC}s AND TEMPERATURES

	-55°C		0°C		25°C		70°C		125°C	
	τ	T_o	τ	T_o	τ	T_o	τ	T_o	τ	T_o
5.5V	105ps	1.4×10^{13} sec	125ps	1.0×10^9 sec	138ps	5.4×10^6 sec	160ps	1.7×10^5 sec	215ps	18 sec
5.0V	110ps	1.3×10^{15} sec	115ps	1.3×10^{10} sec	135ps	9.8×10^6 sec	167ps	3.9×10^4 sec	200ps	9.5×10^2 sec
4.5V	110ps	2.0×10^{18} sec	115ps	3.4×10^{13} sec	132ps	5.1×10^8 sec	175ps	7.3×10^4 sec	220ps	3.0×10^2 sec

Flip-Flop | 54F5074

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
$\overline{S}_{Dn}$	$\overline{R}_{Dn}$	CP_n	D_n	Q_n	$\overline{Q}_n$	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Reset
L	L	X	X	H	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↥	X	NC	NC	Hold

H = High voltage level
h = High voltage level one setup time prior to Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to Low-to-High clock transition
NC = No change from the previous setup
X = Don't care
↑ = Low-to-High clock transition
↥ = Not a Low-to-High clock transition
* = This setup is unstable and will change when either Set or Reset return to the level

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_{IN}	Input voltage range	-0.5 to +7.0	V
I_{IN}	Input current range	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C

Flip-Flop | 54F5074

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH}	High-level input current		V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current	D_n	V_{CC} = Max, V_I = 0.5V			-250	µA
		CP_n, $\overline{S}_{Dn}$, $\overline{R}_{Dn}$				-20	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = Max		20	33	mA

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs High in turn.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	105	120		65		MHz
t_{PLH} t_{PHL}	Propagation delay CP_n to Q_n or $\overline{Q}_n$	Waveform 1	2.0 2.0	3.9 3.9	6.0 6.0	1.5 2.0	7.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_{Dn}$, $\overline{R}_{Dn}$ to Q_n or $\overline{Q}_n$	Waveform 2	3.0 3.0	4.5 5.0	7.5 7.5	2.5 2.5	9.0 9.5	ns ns
t_{PS}	Propagation delay Skew[1,3]	Waveform 4			1.0		1.0	ns
t_{OS}	Output to output Skew[2,3]	Waveform 4			1.5		1.5	ns

NOTE:
1. $|t_{PLH}$ actual - t_{PHL} actual$|$ for any output.
2. $|t_{PN}$ actual - t_{PM} actual$|$ for any output compared to any other output where N and M are either LH or HL.
3. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

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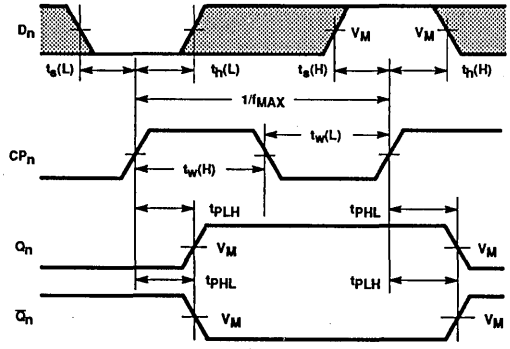
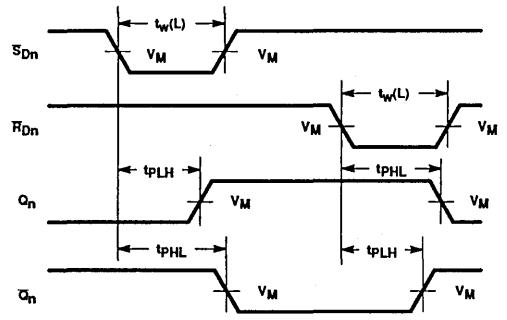
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP_n	Waveform 1	1.5 1.5			2.0 2.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP_n	Waveform 1	1.0 1.0			2.0 1.5		ns ns
$t_w(H)$ $t_w(L)$	CP Pulse width, High or Low	Waveform 1	3.0 4.0			4.0 6.0		ns ns
$t_w(L)$	$\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ Pulse width, Low	Waveform 2	3.0			4.0		ns
t_{REC}	Recovery time $\overline{S}_{Dn}$ or $\overline{R}_{Dn}$ to CP_n	Waveform 3	3.0			4.0		ns

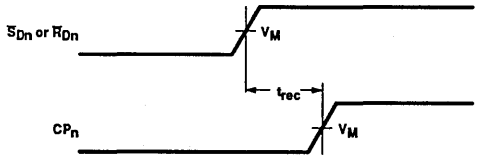
AC WAVEFORMS



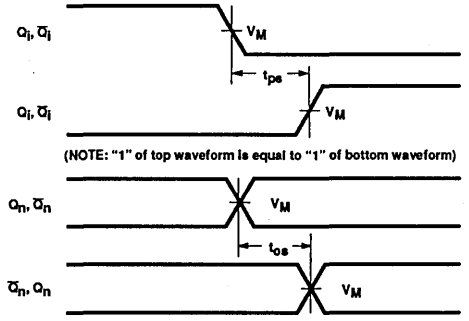
Waveform 1. Propagation Delay for Data to Output, Data Setup Time and Hold Times and Clock Width



Waveform 2. Propagation Delay for Set and Reset to Output, Set and Reset Pulse Width



Waveform 3. Recovery Time for Set or Reset to Clock



Waveform 4. Propagation Delay Skew and Output to Output Skew

NOTE: For all waveforms V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

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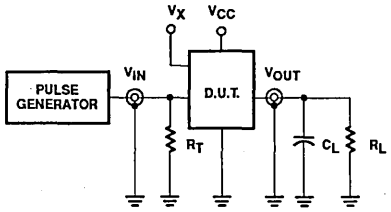
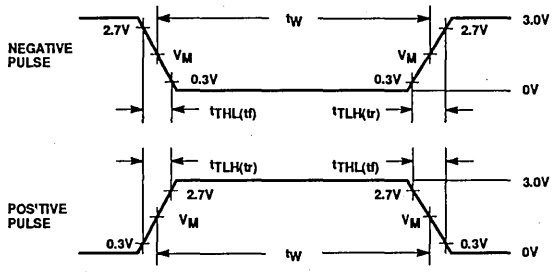
TEST CIRCUITS AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



$V_M = 1.5V$

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F30244
Line Driver

Octal High Current Buffer/Line & Backplane Driver, NINV (30 Ω O.C.)

Product Specification

DESCRIPTION

This device is a high current Open-Collector Octal Buffer composed of eight non-inverting drivers.

This device has non-inverting paths with two Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) each controlling four outputs.

The driver is designed to deal with the low impedance transmission line effects found on printed circuit boards when fast edge rates are used.

The 130mA IOL provides ample power to achieve TTL switching on the incident wave voltage.

FEATURES

- **Ideal for driving transmission lines or backplanes. 130mA I_{OL} ideal for low-impedance applications with impedance as low as 30Ω.**
- **High-impedance NPN base inputs for reduced loading (20μA in High and Low states)**
- **Ideal for applications which require high output drive and minimal bus loading**
- **"Flow through" pinout**
- **Open-Collector outputs sink 130mA**
- **Multiple side pins are used for V_{CC} and GND to reduce lead inductance (improves speed and noise immunity)**
- **24-pin Slim DIP package**

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54F30244/BLA
24-Pin Ceramic Flatpack	54F30244/BKA
28-Pin Ceramic LLCC	54F30244/B3A

FUNCTION TABLE

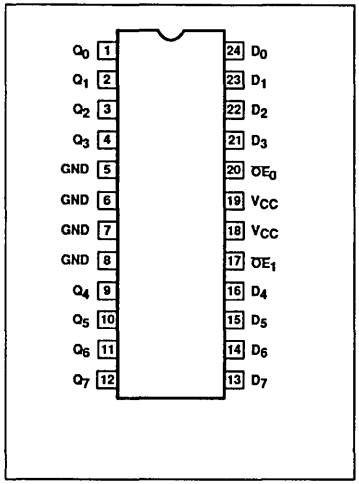
INPUTS		OUTPUTS
$\overline{OE}_R$	D_R	Q_R
L	L	L
L	H	H
H	X	OFF

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

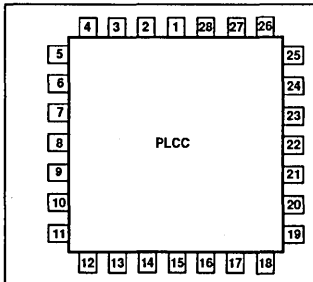
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data Inputs	1.0/0.033	20μA/20μA
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable Inputs, (Active Low)	1.0/0.033	20μA/20μA
Q_0 - Q_7	Data Outputs	OC*/216.7	OC*/130mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state. OC* = Open Collector

PIN CONFIGURATION



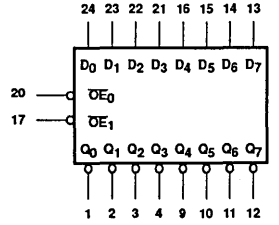
LLCC PIN CONFIGURATION



PIN/FUNCTION

1	NC	11	Q4	21	Vcc
2	Q0	12	Q5	22	NC
3	Q1	13	Q6	23	Vcc
4	Q2	14	Q7	24	$\overline{OE0}$
5	Q3	15	NC	25	D3
6	GND	16	D7	26	D2
7	GND	17	D6	27	D1
8	NC	18	D5	28	D0
9	GND	19	D4		
10	GND	20	$\overline{OET}$		

LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	260	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			130	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, V_{OH} = Max				250	µA
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max,	I_{OL} = 100mA		.35	.50	V
			V_{IH} = Min	I_{OL1} = 130mA[3]		.35	.55	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage		V_{CC} = 0.0, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V				-20	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			19	27	mA
		I_{CCL}				70	100	mA

NOTES:

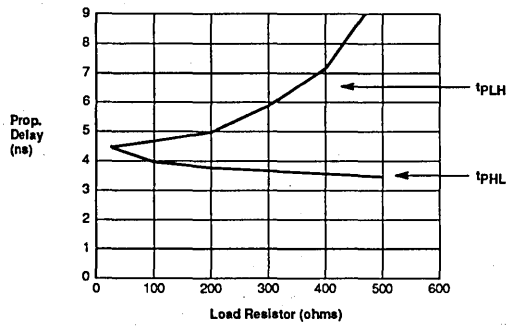
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OL1} is the current necessary to guarantee the High and Low transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS

(When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 1	4.0 3.0	10.5 5.5	14.5 9.0	4.0 3.0	15.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to Q_n	Waveform 1	4.0 3.5	9.5 6.0	14.0 9.0	4.0 3.5	14.5 10.5	ns ns

AC CHARACTERISTICS

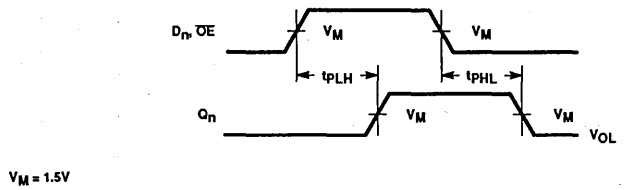


Typical Propagation Delay vs. Lead Resistor

NOTES:

When using open collector parts, the value of the pull-up resistor greatly affects the value of the T_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the T_{PLH} up to 50% with only a slight increase in the T_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and, thus the total I_{IL} of the receivers does not exceed the I_{OL} maximum specification.

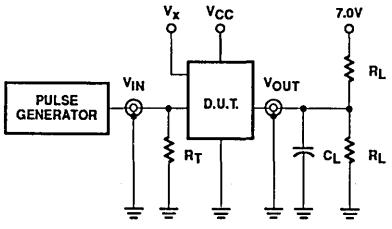
AC WAVEFORMS



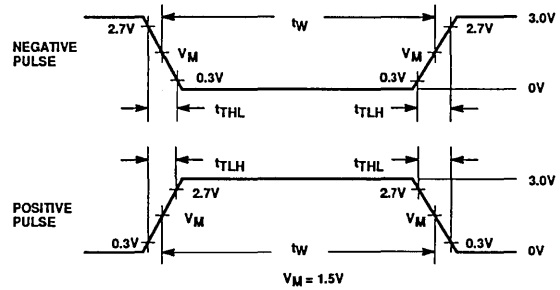
V_M = 1.5V

Waveform 1. Propagation Delay, Data and Output Enable to Outputs

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at:: ≤0.8V, ≥2.7V or open per Function Table.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**t_W**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

Signetics

Military Logic Products

54F30245
Transceiver

Octal Transmission Line/Backplane Transceiver, NINV (30 Ω O.C. w/ Enable + 3-State)

Product Specification

DESCRIPTION

The 54F30245 is a high current Octal Transceiver and has non-inverting paths.

The B outputs are open collector with 130mA I_{OL} while the A outputs are 3-State with 20mA I_{OL}. The transceiver is designed to deal with the low impedance transmission line effects found on printed circuit boards when fast edge rates are used.

The 130mA I_{OL} provides ample power to achieve TTL switching on the incident wave.

FEATURES

- **High-impedance NPN base inputs for reduced loading**
- **Ideal for applications which require high output drive and minimal bus loading**
- **Octal bidirectional bus interface**
- **Choice of outputs Open collector (B_0 - B_7) and 3-States (A_0 - A_7)**
- **Open collector outputs sink 130mA**
- **130mA I_{OL} ideal for low impedance applications and transmission line effects with impedance as low as 30Ω**
- **3-State outputs sink 20mA**
- **Multiple side pins are used for V_{CC} and GND to reduce lead inductance (Improves speed and noise immunity)**
- **Flow through pinout structure facilitates PC board layout**

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

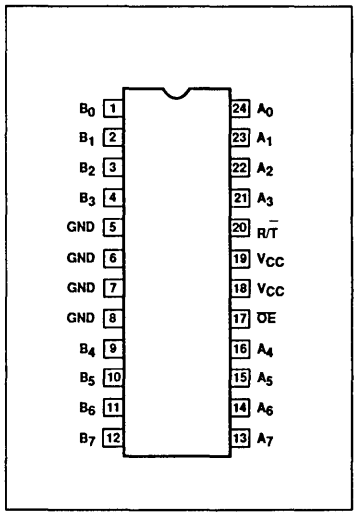
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	Data Inputs	3.5/0.12	70μA/70μA
B_0 - B_7	Data Inputs	3.5/1.0	70μA/0.6mA
$\overline{OE}$	Output Enable Inputs (Active Low)	1.0/0.033	20μA/20μA
$\overline{R/T}$	Receive/Transmit Input	1.0/0.033	20μA/20μA
A_0 - A_7	Data Outputs (3-State)	150/33.3	3mA/20mA
B_0 - B_7	Data Outputs (OC*)	OC*/216.6	OC*/130mA

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.
OC* = Open Collector

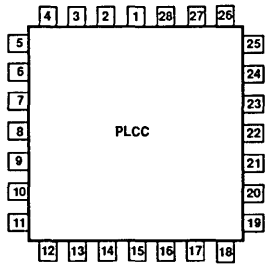
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic Dip	54F30245/BLA
24-Pin Ceramic Flat Pack	54F30245/BKA
28-Pin Ceramic LLCC	54F30245/B3A

PIN CONFIGURATION



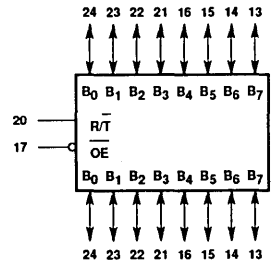
LLCC PIN CONFIGURATION



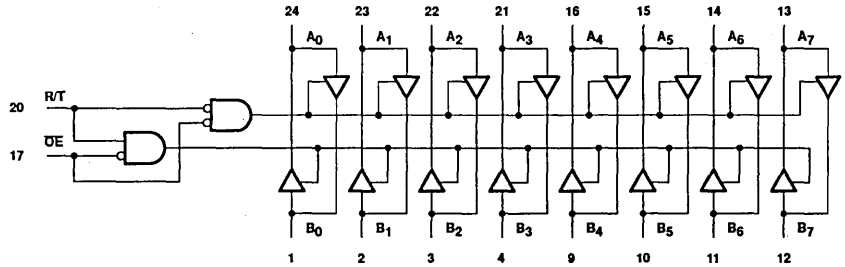
PIN/FUNCTION

1	NC	11	B4	21	Vcc
2	B0	12	B5	22	NC
3	B1	13	B6	23	Vcc
4	B2	14	B7	24	R/T
5	B3	15	NC	25	A3
6	GND	16	A7	26	A2
7	GND	17	A6	27	A1
8	NC	18	A5	28	A0
9	GND	19	A4		
10	GND	20	OE		

LOGIC SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 18, 19
GND = Pin 5, 6, 7, 8

FUNCTION TABLE

INPUTS			
$\overline{OE}$	R/T	A_n	B_n
L	H	A = B	Inputs
L	L	Inputs	B = A
H	X	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage range		-0.5 to +7.0	V
V_I	Input voltage range		-0.5 to +7.0	V
I_I	Input current range		-30 to +5	mA
V_O	Voltage applied to output in High output state range		-0.5 to +5.5	V
I_O	Current applied to output in Low output state	B_0 - B_7	260	mA
		A_0 - A_7	40	mA
T_{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High-level output voltage	B_0 - B_7			4.5	V
I_{OH1}	High-level output current	A_0 - A_7			-1	mA
I_{OH2}	High-level output current	A_0 - A_7			-3	mA
I_{OL}	Low-level output current	B_0 - B_7			130	mA
		A_0 - A_7			20	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
I_{OH}	High-level output current	B_0 - B_7	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, V_{OH} = Max				250	µA
V_{OH}	High-level output voltage	A_0 - A_7	V_{CC} = Min, V_{IL} = Max,	I_{OH2} = -3mA	2.4			V
		R/T, $\overline{OE}$	V_{IH} = Min	I_{OH1} = -1mA	2.5	3.4		V
V_{OL}	Low-level output voltage	A_0 - A_7 R/T, $\overline{OE}$	V_{CC} = Min, V_{IL} = Max,	I_{OL} = 20mA		.35	.50	V
V_{OL}	Low-level output voltage	B_0 - B_7	V_{IH} = Min	I_{OL} = 100mA		.40	.50	V
				I_{OL1} = 130mA[4]			.80	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	R/T, $\overline{OE}$	V_{CC} = 0.0V, V_I = 7.0V				100	µA
		A_n, B_n	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	R/T, $\overline{OE}$	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IH3}	High-level input current	B_0 - B_7	V_{CC} = Max, V_I = 2.7V				70	µA
I_{IL}	Low-level input current	R/T, $\overline{OE}$	V_{CC} = Max, V_I = 0.5V				-20	µA
		B_0 - B_7					-600	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0 - A_7	V_{CC} = Max, V_O = 2.7V				70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied	A_0 - A_7	V_{CC} = Max, V_O = 0.5V				-70	µA
I_{OS}	Short circuit output current[3]	A_0 - A_7	V_{CC} = Max		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} = Max			45	70	mA
		I_{CCL}				85	135	mA
		I_{CCZ}				55	75	mA

NOTES:

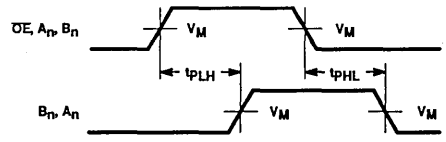
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable conditions and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.
4. I_{OL1} is the current necessary to guarantee the High-to-Low transition in a 30Ω transmission line on the incident wave.

AC ELECTRICAL CHARACTERISTICS (When measured in accordance with the procedures outlined in Signetics LOGIC App Note 202, "Testing and Specifying FAST Logic.")

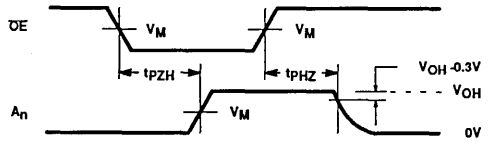
SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
*t_{PLH} t_{PHL}	Propagation delay A_n to B_n		Waveform 1	7.5 3.0	9.5 5.5	13.5 6.5	7.0 3.0	13.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to A_n		Waveform 1	2.0 1.0	3.5 2.5	6.5 5.5	1.5 1.0	7.0 5.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{OE}$ to B_n	B_n outputs	Waveform 1	7.0 3.5	9.5 5.5	12.5 8.5	7.0 3.5	13.0 9.5	ns
t_{PZH} t_{PZL}	Output Enable time from High-to-Low	A_n outputs	Waveform 2 Waveform 3	2.5 2.0	4.5 4.0	7.5 8.0	2.0 1.5	8.5 8.5	ns
t_{PHZ} t_{PLZ}	Output Enable time from High-to-Low	A_n outputs	Waveform 2 Waveform 3	1.5 1.0	3.5 3.5	6.5 6.5	1.0 1.0	7.5 7.0	ns

* See Figure A for Open Collector Output Information

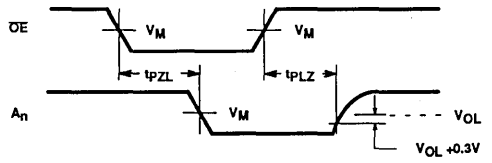
AC WAVEFORMS



Waveform 1. Propagation Delay, Data and Output Enable to Outputs



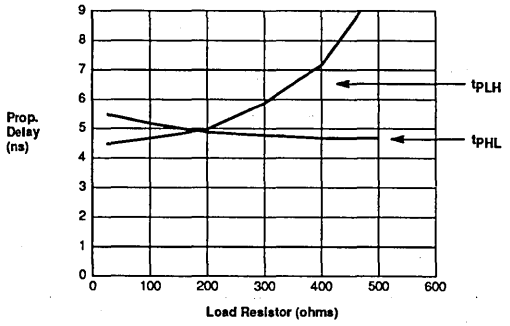
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

V_M = 1.5V

TYPICAL PROPAGATION DELAYS vs. LOAD RESISTOR FOR OPEN COLLECTOR OUTPUTS

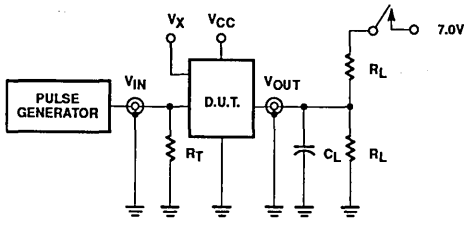


NOTES:

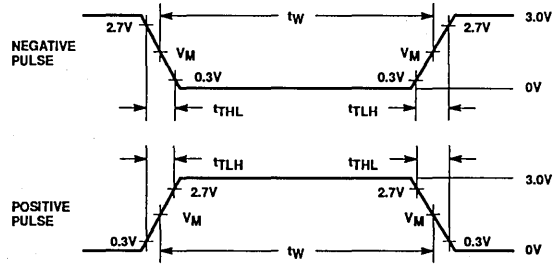
When using open collector parts, the value of the pull-up resistor greatly affects the value of the T_{PLH}. For example, changing the specified pull-up resistor value from 500Ω to 100Ω will improve the T_{PLH} up to 50% with only a slight increase in the T_{PHL}. However, if the value of the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and, thus the total I_{IL} of the receivers does not exceed the I_{OL} maximum specification.

Figure A

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

TEST POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
O_C	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

Section 4
TTL Data Sheets

Military Products

INDEX

Signetics

5400, 54LS00, 54S00
Gates

Quad Two-Input NAND Gates

Product Specification

Military Logic Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	PIN CONFIGURATION	ORDER CODE
Ceramic DIP	Figure A	5400/BCA, 54LS00/BCA, 54S00/BCA
Ceramic Flat Pack	Figure A	54LS00/BDA, 54S00/BDA
	Figure B	5400/BDA
Ceramic LLCC	See Note	54LS00/B2A, 54S00/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54S	54LS
A, B	Inputs	1UL	1SUL	1LSUL
Y	Output	10UL	10SUL	10LSUL

NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}, a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_L, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION

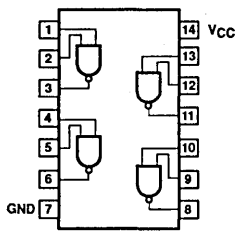


Figure A

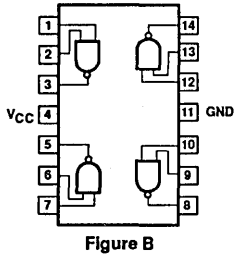
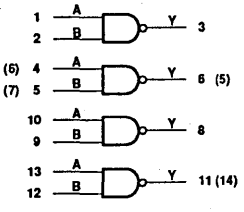


Figure B

For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



( ) = Flat Pack Figure B

For LLCC pin assignments, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS Over operating free-air temperature range unless otherwise noted

SYMBOL	PARAMETER	54	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_{STG}	Storage temperature range	-65 to +150			°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54			54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			2.0			V
V_{IL}	Low-level input voltage			+0.8			+0.7			+0.8	V
I_{IK}	Input clamp current			-12			-18			-18	mA
I_{OH}	High-level output current			-400			-400			-1000	µA
I_{OL}	Low-level output current			16			4			20	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS Over recommended operating free-air temperature range unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS[1]		5400			54LS00			54S00			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, I_{OL} = Max			0.2	0.4		0.25	0.4			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V			1.0						1.0	mA
			V_I = 7.0V						0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V			40							µA
			V_I = 2.7V						20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V			-1.6			-0.4				mA
			V_I = 0.5V									-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-55	-20		-100	-40		-110	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High		4	8		0.8	1.6		10	16	mA
			I_{CCL} Outputs LOW		12	22		2.4	4.4		20	36	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	54[4]		54LS		54S		UNIT
			$C_L = 15pF$		$C_L = 15pF$		$C_L = 15pF$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 15		15 15		4.5 5.0	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

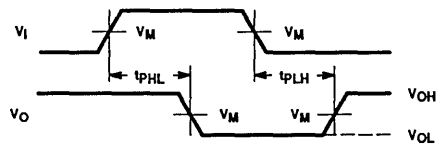
SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS[4]		54S[4]		UNIT
			$C_L = 50pF$		$C_L = 50pF$		$C_L = 50pF$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		26 19		20 20		7.0 7.5	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[4]

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		54S		UNIT
			$C_L = 50pF$		$C_L = 50pF$		$C_L = 50pF$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		34 25		26 26		9 9	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable typo and function table operating mode.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time, and duration of the short should not exceed one second.
4. These parameters are guaranteed, but not tested.

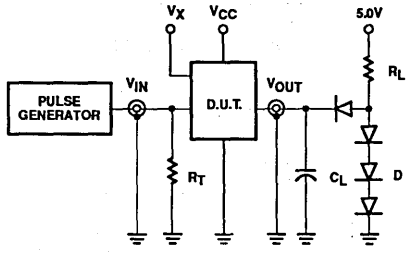
AC WAVEFORM



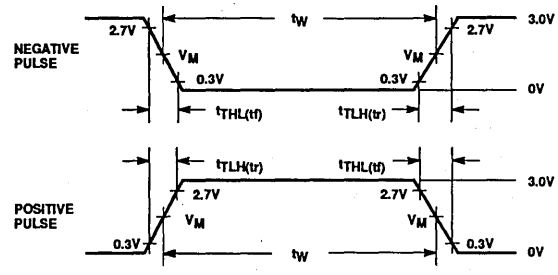
Waveform 1. Waveform for Inverting Outputs

NOTE: $V_M = 1.3V$ for 54LS/S; $V_M = 1.5V$ for all other TTL families.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS02, 54S02
Gates

Quad Two-Input NOR Gate

Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION.

DESCRIPTION	ORDER CODE
Ceramic DIP	54LS02/BCA, 54S02/BCA
Ceramic Flat Pack	54LS02/BDA, 54S02/BDA
Ceramic LLCC	54LS02/B2A, 54S02/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

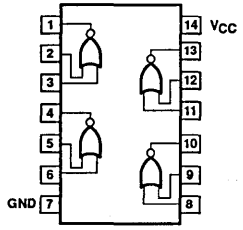
PINS	DESCRIPTION	54S	54LS
A, B	Inputs	1SUL	1LSUL
Y	Output	10SUL	10LSUL

NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

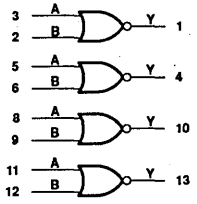
SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +5.5	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		54LS			54S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			2.0			V
V_{IL}	Low-level input voltage				+0.7			+0.8	V
		+125°C			+0.7			+0.7	V
I_{IK}	Input clamp current				-18			-18	mA
I_{OH}	High-level output current				-400			-1000	µA
I_{OL}	Low-level output current				4			20	mA
T_A	Operating free-air temperature range		-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54LS02			54S02			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max			0.25	0.4			0.5	V
		I_{OL} = Max	+125°C			0.4			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V						1.0	mA
			V_I = 7.0V			0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V			-0.4				mA
			V_I = 0.5V						-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	-40		-100	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High		1.6	3.2		17	29	mA
			I_{CCL} Outputs Low		2.8	5.4		26	45	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		15 15		5.5 5.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[4]

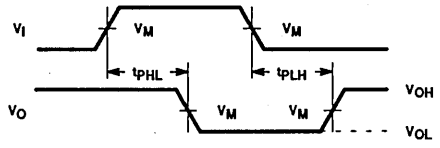
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		20 20		7.0 7.0	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[4]

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		26 26		9.0 9.0	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. These parameters are guaranteed, but not tested.

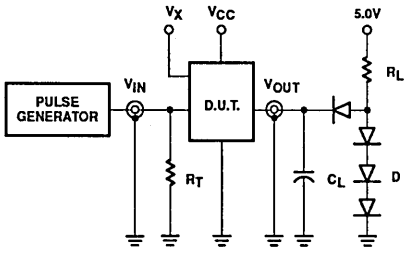
AC WAVEFORM



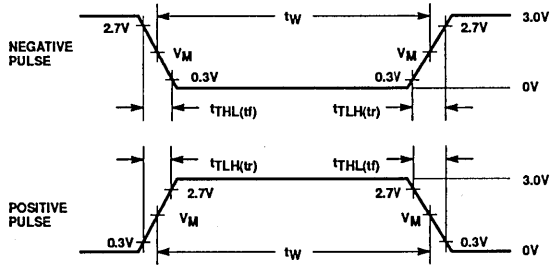
Waveform 1. Waveform for Inverting Outputs

NOTE: V_M = 1.3V for 54LS, V_M = 1.5V for all other TTL families.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

5404, 54LS04, 54S04
Inverters

Hex Inverter

Product Specification

Military Logic Products

FUNCTION TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	PIN CONFIGURATION	ORDER CODE
Ceramic DIP	Figure A	5404/BCA, 54LS04/BCA, 54S04/BCA
Ceramic Flat Pack	Figure A	54LS04/BDA, 54S04/BDA
	Figure B	5404/BDA
Ceramic LLCC	See Jedec Standard No. 2	54LS04/B2A, 54S04/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54S	54LS
A	Input	1UL	1SUL	1LSUL
Y	Output	10UL	10SUL	10LSUL

NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6 mA I_{IL}, a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0 mA I_{IL}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION

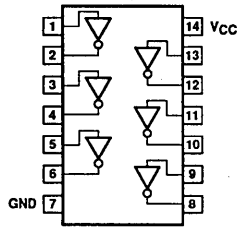


Figure A

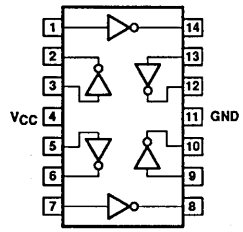
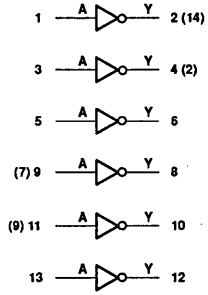


Figure B

For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



( ) = Flat Pack Figure B

For LLCC pin assignments, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS Over operating free-air temperature range unless otherwise noted

SYMBOL	PARAMETER	54	54LS	54S	UNIT
V_{CC}	Supply voltage range	7.0	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_{STG}	Storage temperature range	-65 to +150			°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54			54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			2.0			V
V_{IL}	Low-level input voltage			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current			-12			-18			-18	mA
I_{OH}	High-level output voltage			-400			-400			-1000	µA
I_{OL}	Low-level output current			16			4			20	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS Over recommended operating free-air temperature range unless otherwise noted

SYMBOL	PARAMETER	TEST CONDITIONS[1]		5400			54LS00			54S00			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, I_{OL} = Max			0.2	0.4		0.25	0.4			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V			1.0						1.0	mA
			V_I = 7.0V						0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V			40							µA
			V_I = 2.7V						20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V			-1.6			-0.4				mA
			V_I = 0.5V									-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-55	-20		-100	-40		-110	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High		6	12		1.2	2.4		15	24	mA
			I_{CCL} Outputs Low		18	33		3.6	6.6		30	54	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	54[4]		54LS		54S		UNIT
			$C_L = 15pF$		$C_L = 15pF$		$C_L = 15pF$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 15		15 15		4.5 5.0	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

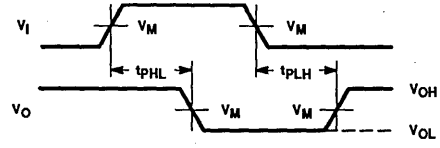
SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS[4]		54S[4]		UNIT
			$C_L = 50pF$		$C_L = 50pF$		$C_L = 50pF$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		26 19		20 20		7.0 7.5	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[4]

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		54S		UNIT
			$C_L = 15pF$		$C_L = 15pF$		$C_L = 15pF$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		34 25		26 26		9.0 9.0	ns ns

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time, and duration of the short should not exceed one second.
4. These parameters are guaranteed, but not tested.

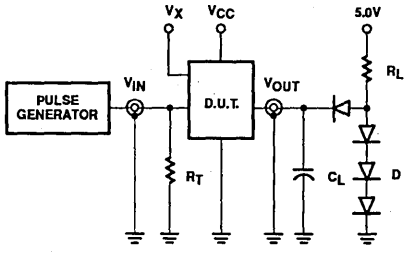
AC WAVEFORM



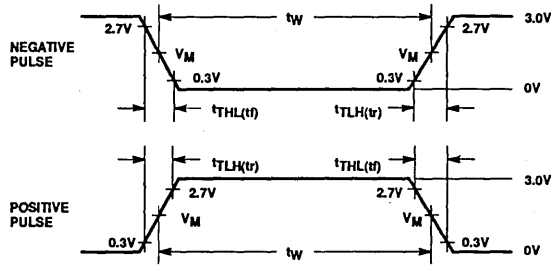
Waveform 1. Waveform for Inverting Outputs

NOTE: V_M = 1.3V for 54LS; V_M = 1.5V for all other TTL families

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

54LS08, 54S08
Gates

Quad Two-Input AND Gates

Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54LS08/BCA, 54S08/BCA
Ceramic Flat Pack	54LS08/BDA, 54S08/BDA
Ceramic LLCC	54LS08/B2A, 54S08/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

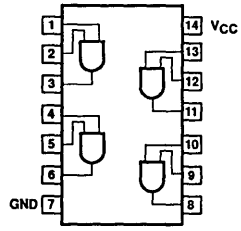
PINS	DESCRIPTION	54S	54LS
A, B	Inputs	1SUL	1LSUL
Y	Output	10SUL	10LSUL

NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

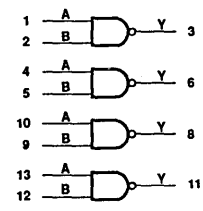
SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +6.5	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.7			+0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-400			-1000	µA
I_{OL}	Low-level output current			4			20	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54LS08			54S08			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, I_{OH} = Max		2.5	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V						1.0	mA
			V_I = 7.0V			0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V			-0.4				mA
			V_I = 0.5V						-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-110	-40		-100	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High		2.4	4.8		18	32	mA
			I_{CCL} Outputs Low		4.4	8.8		32	57	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS[4]		54S		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		15 20		7.0 7.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

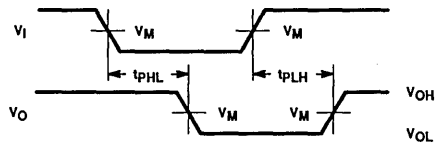
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S[4]		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		20 25		9.0 11.0	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[4]

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		26 33		12 14	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. These parameters are guaranteed, but not tested.

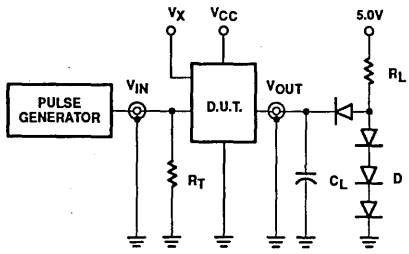
AC WAVEFORM



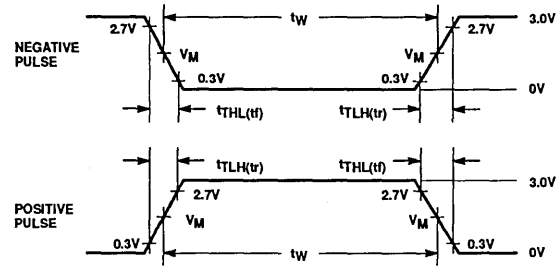
NOTE: V_M = 1.3V for 54LS, V_M = 1.5V for all other TTL families.

Waveform 1. Waveform for Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS10, 54S10, 54S11
Gates

Triple Three-Input NAND ('10), AND ('11) Gates

Product Specification

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Y('10)	Y('11)
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54LS10/BCA, 54S10/BCA, 54S11/BCA
Ceramic Flat Pack	54LS10/BDA, 54S10/BDA, 54S11/BDA
Ceramic LLCC	54LS10/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S	54LS
A - C	Inputs	1SUL	1LSUL
Y	Output	10SUL	10LSUL

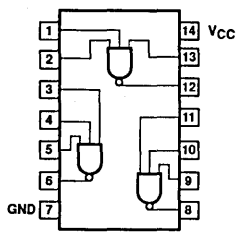
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +5.5	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

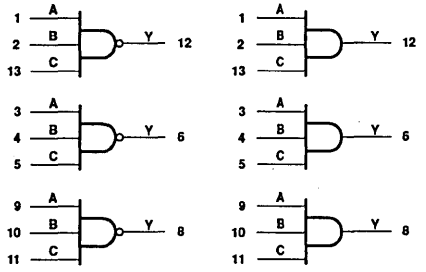
PIN CONFIGURATION

'10, '11



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		54LS			54S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			2.0			V
V_{IL}	Low-level input voltage				+0.7			+0.8	V
		+125°C			+0.7			+0.7	V
I_{IK}	Input clamp current				-18			-18	mA
I_{OH}	High-level output current				-400			-1000	µA
I_{OL}	Low-level output current				4			20	mA
T_A	Operating free-air temperature range		-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			54LS10			54S10, 54S11			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OH} = Max			2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	I_{OL} = Max, V_{CC} = Min, V_{IH} = Min, V_{IL} = Max				0.25	0.4			0.5	V
			+125°C				0.4			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.7V				20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V				-0.4				mA
			V_I = 0.5V							-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		'10	-20		-100	-40		-110	mA
				'11	-20		-100	-40		-100	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High	'10		0.6	1.2		7.5	12	mA
			I_{CCL} Outputs Low			1.8	3.3		15	27	mA
			I_{CCH} Outputs High	'11					13.5	24	mA
			I_{CCL} Outputs Low						24	42	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[4]

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1 - '10		15 15		4.5 5.0	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2 - '11		15 20		7.0 7.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

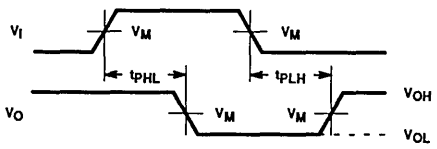
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1 - '10		15 17		7.0 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2 - '11		20 25		9 11	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[4]

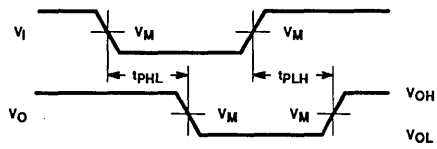
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1 - '10		20 24		9 9	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2 - '11		26 33		12 14	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. These parameters are guaranteed, but not tested.

AC WAVEFORMS



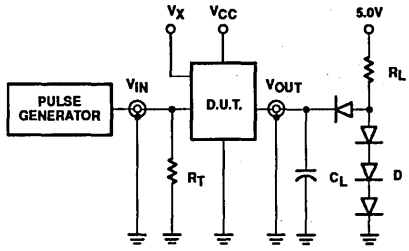
Waveform 1. Waveform for Inverting Outputs '10



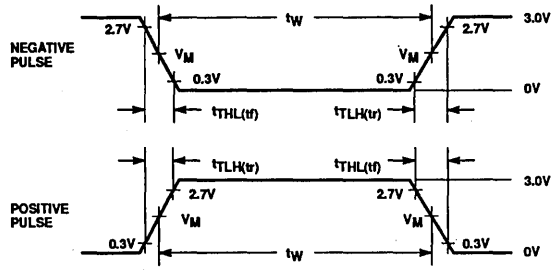
Waveform 2. Waveform for Non-Inverting Outputs '11

NOTE: V_M = 1.3V for 54LS, V_M = 1.5V for all other TTL families

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS14
Schmitt Trigger

Hex Inverter Schmitt Trigger

Product Specification

DESCRIPTION

The 54LS14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

FUNCTION TABLE

INPUTS	OUTPUT
A	Y
0	1
1	0

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54LS14/BCA
Ceramic Flat Pack	54LS14/BDA
Ceramic LLCC	54LS14/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

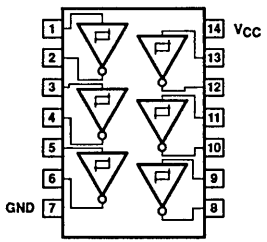
PINS	DESCRIPTION	54LS
A	Inputs	1LSUL
Y	Outputs	10LSUL

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

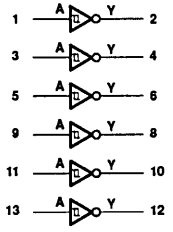
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	+7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V		1.4	1.6	1.9	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V		0.5	0.8	1.0	V
ΔV_T	Hysteresis (V_{T+} - V_{T-})	V_{CC} = 5.0V		0.4	0.8		V
V_{OH}	High-level output voltage	V_{CC} = Min, V_I = V_{T-MIN}, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_I = T_{T+MAX}, I_{OL} = Max			0.35	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, V_I = V_{T+}			-0.14		mA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, V_I = V_{T-}			-0.18		mA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V				0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V				-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH}	Outputs HIGH	8.6	16	mA
			I_{CCL}	Outputs LOW	12	21	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 15pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 22	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[4]

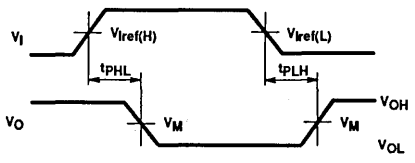
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		27 27	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[4]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		35 35	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. These parameters are guaranteed, but not tested.

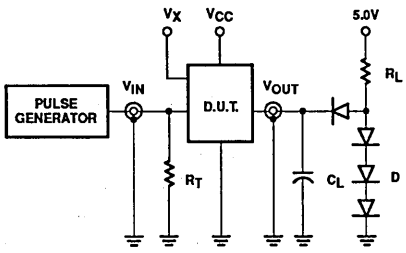
AC WAVEFORM



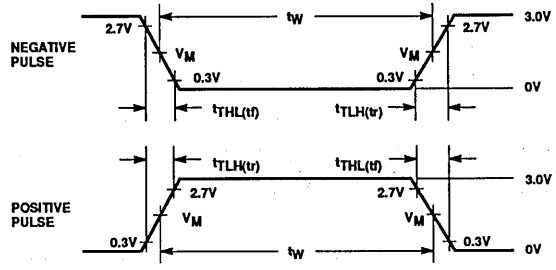
Waveform 1. For Inverting Outputs

NOTE: $V_M = 1.3V$ for 54LS, $V_{Iref(H)} = 1.6V$, $V_{Iref(L)} = 0.8V$.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



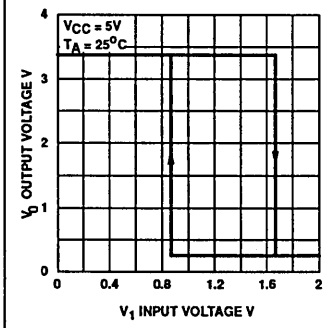
Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

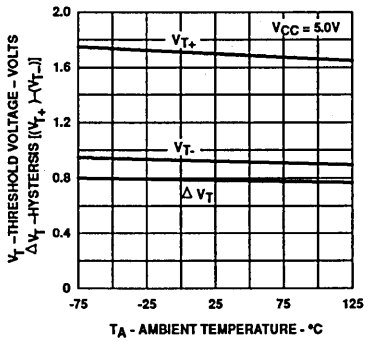
DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

TYPICAL PERFORMANCE CHARACTERISTICS

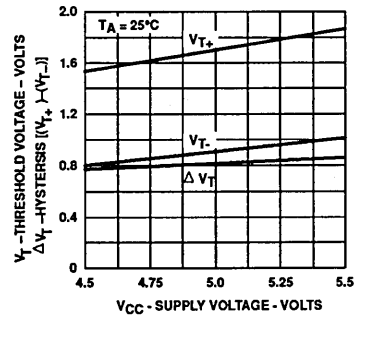
V_I vs. V_O Transfer Function



Threshold Voltage and Hysteresis vs. Ambient Temperature



Threshold Voltage and Hysteresi



Signetics

Military Logic Products

54LS20, 54S20
Gates

Dual Four-Input NAND Gates

Product Specification

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54LS20/BCA, 54S20/BCA
Ceramic Flat Pack	54LS20/BDA, 54S20/BDA
Ceramic LLCC	54LS20/B2A, 54S20/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

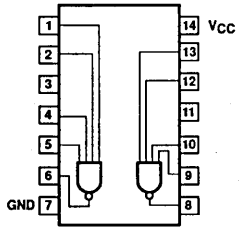
PINS	DESCRIPTION	54S	54LS
A - D	Inputs	1SUL	1LSUL
Y	Output	10SUL	10LSUL

NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

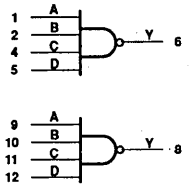
SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +5.5	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		54LS			54S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			2.0			V
V_{IL}	Low-level input voltage				+0.7			+0.8	V
		+125°C			+0.7			+0.7	V
I_{IK}	Input clamp current				-18			-18	mA
I_{OH}	High-level output current				-400			-1000	µA
I_{OL}	Low-level output current				4			20	mA
T_A	Operating free-air temperature range		-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54LS20			54S20			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OH} = Max		2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,			0.25	0.4			0.5	V
		I_{OL} = Max	+125°C			0.4			0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V						1.0	mA
			V_I = 7.0V			0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V			-0.4				mA
			V_I = 0.5V						-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	-40		-110	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High		0.4	0.8		5	8	mA
			I_{CCL} Outputs Low		1.2	2.2		10	18	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[4]

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		15 15		4.5 5.0	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

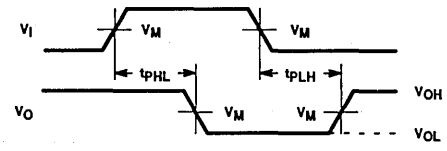
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		20 20		7.0 7.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[4]

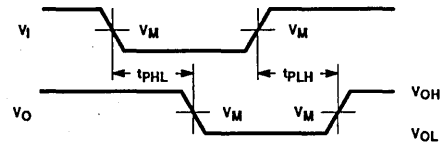
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		26 26		9.0 9.0	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. These parameters are guaranteed, but not tested.

AC WAVEFORM



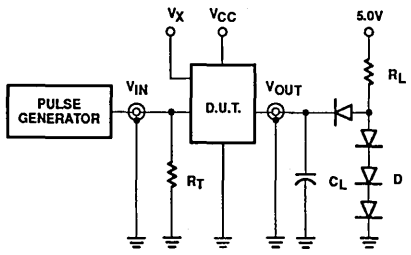
Waveform 1. Waveform for Inverting Outputs



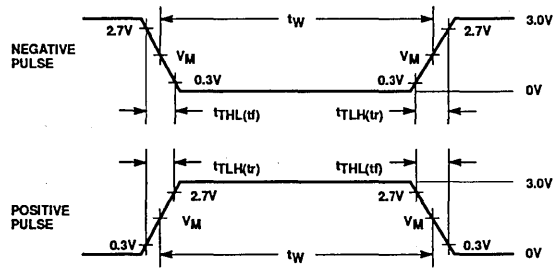
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.3V for 54LS, V_M = 1.5V for all other TTL families.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

5432
Gates

Quad Two-Input OR Gate

Product Specification

Military Logic Products

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	5432/BCA
14-Pin Ceramic Flat Pack	5432/BDA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

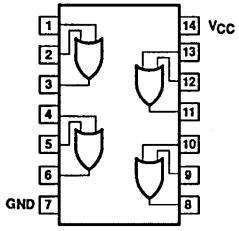
PINS	DESCRIPTION	54
A, B	Inputs	1UL
Y	Output	10UL

NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}.

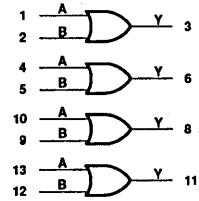
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



LOGIC SYMBOL



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-12	mA
I_{OH}	High-level output current			-800	µA
I_{OL}	Low-level output current			16	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, I_{OH} = Max		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max			0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-55	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High		15	22	mA
			I_{CCL} Outputs Low		23	38	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[4]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		15 22	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

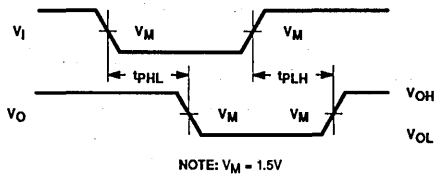
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		19 26	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[4]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		25 34	ns ns

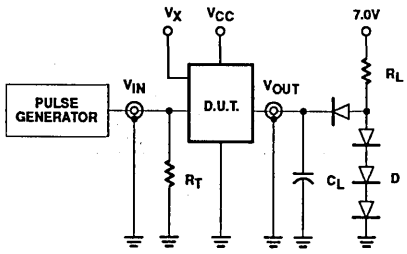
NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. These parameters are guaranteed, but not tested.

AC WAVEFORM

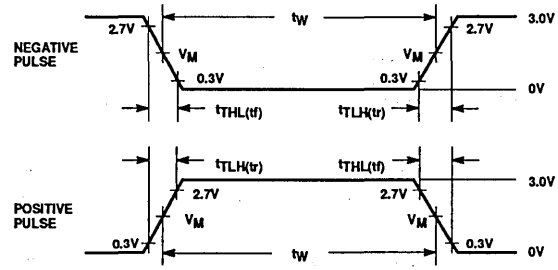


Waveform 1. Waveform for Inverting Output

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54S40
Buffer

Dual Four-Input NAND Buffer

Product Specification

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54S40/BCA
Ceramic Flat Pack	54S40/BDA
Ceramic LLCC	54S40/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

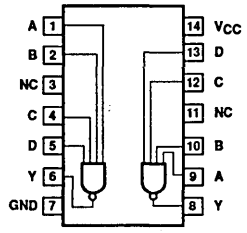
PINS	DESCRIPTION	54S
A - D	Inputs	2SUL
Y	Output	30SUL

NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

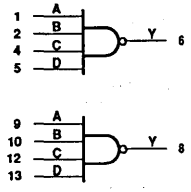
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
	+125°C			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3000	µA
I_{OL}	Low-level output current			60	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min,				0.5	V
		I_{OL} = Max	+125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				100	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V				-4.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-50		-225	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High		10	18	mA
			I_{CCL} Outputs Low		25	44	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

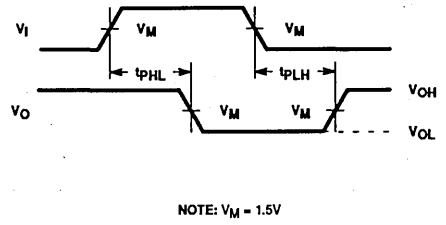
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		6.5 6.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[4]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		8.5 8.5	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. The 54S40 test time for I_{OS} should not exceed 100ms.
4. These parameters are guaranteed, but not tested.

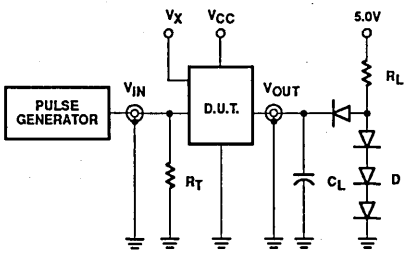
AC WAVEFORM



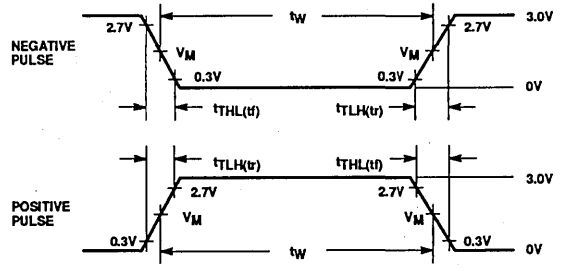
NOTE: V_M = 1.5V

Waveform 1. Waveform for Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	93Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54S51
Gate

Dual 2-Wide 2-Input AND-OR-Invert Gate

Product Specification

Military Logic Products

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H X	H X	X H	X H	L L
All other combinations				H

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54S51/BCA
Ceramic Flat Pack	54S51/BDA
Ceramic LLCC	54S51/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

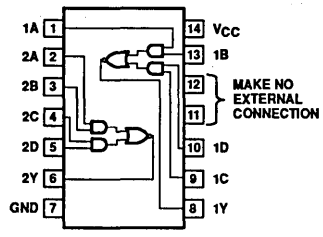
PINS	DESCRIPTION	54S
All	Inputs	1SUL
Y	Output	10SUL

NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

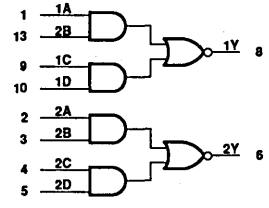
SYMBOL	PARAMETER	54S	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +6.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1000	µA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, I_{OL} = Max				0.5	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V				-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-40		-100	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High		8.2	17.8	mA
			I_{CCL} Outputs Low		13.6	22	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		5.5 5.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[4]

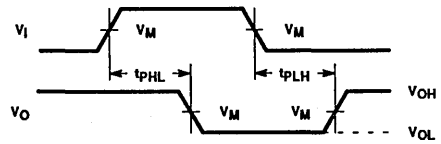
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		7.0 8.0	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[4]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		9.0 10.0	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. These parameters are guaranteed, but not tested.

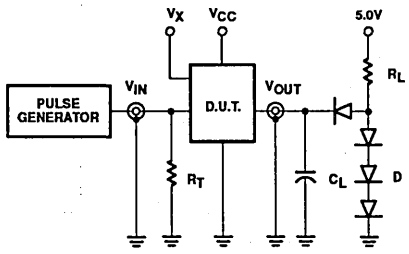
AC WAVEFORM



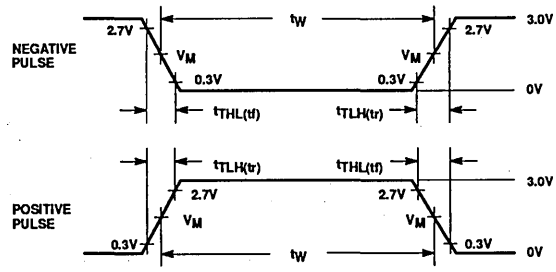
NOTE: V_M = 1.5V

Waveform 1. Waveform for Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS74A, 54S74
Flip-Flops

Dual D-Type Flip-Flops

Product Specification

DESCRIPTION

The 54LS74A, 54S74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-Low inputs and operate independently of the clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. The D inputs must be stable one setup time prior to the Low-to-High clock transition for predictable operation. Although the Clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock-to-output delay time for reliable operation.

ORDERING INFORMATION

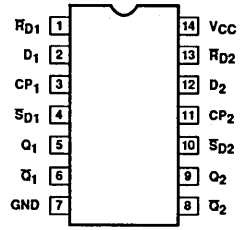
DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54LS74A/BCA 54S74/BCA
14-Pin Ceramic FlatPack	54LS74A/BDA 54S74/BDA
14-Pin Ceramic LLCC	54LS74A/B2A 54S74/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S	54LS
D	Input	1SUL	1LSUL
$\overline{R}_D$	Input	3SUL	2LSUL
$\overline{S}_D$	Input	2SUL	2LSUL
CP	Input	2SUL	1LSUL
Q, $\overline{Q}$	Outputs	10SUL	10LSUL

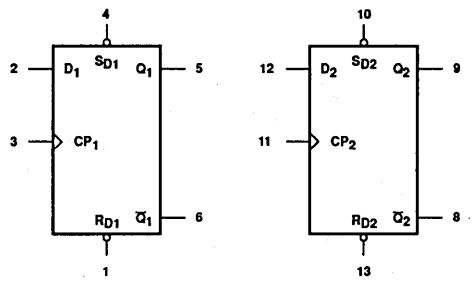
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}, and 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



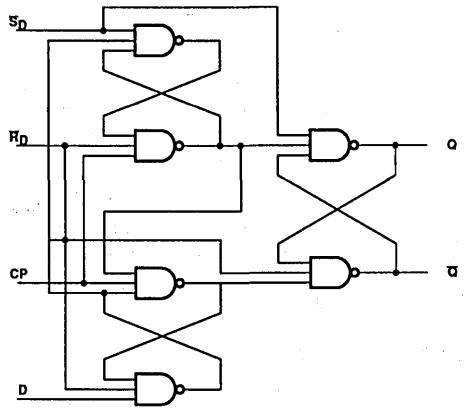
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined(1)	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = High voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the Low-to-High clock transition.
X = Don't care.
↑ = Low-to-High clock transition.

NOTE:
(1) Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +5.5	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		54LS			54S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			2.0			V
V_{IL}	Low-level input voltage				+0.7			+0.8	V
		+125°C			+0.7			+0.7	V
I_{IK}	Input clamp current				-18			-18	mA
I_{OH}	High-level output current				-400			-1000	µA
I_{OL}	Low-level output current				4			20	mA
T_A	Operating free-air temperature range		-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			54LS74A			54S74			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max			2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,				0.25	0.4			0.5	V
		I_{OL} = Max	+125 °C				0.4			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V							1.0	mA
			V_I = 7.0V	D input			0.1				mA
				$\overline{R}_D$ input			0.2				mA
				$\overline{S}_D$ input			0.2				mA
				CP input			0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		D input			20			50	µA
				$\overline{R}_D$ input			40			150	µA
				$\overline{S}_D$ input			40			100	µA
				CP input			20			100	µA
I_{IL}	Low-level input current[5]	V_{CC} = Max	V_I = 0.4V	D input			-0.4				mA
				$\overline{R}_D$ input			-0.8				mA
				$\overline{S}_D$ input			-0.8				mA
				CP input			-0.4				mA
			V_I = 0.5V	D input						-2	mA
				$\overline{R}_D$ input						-6	mA
				$\overline{S}_D$ input						-4	mA
				CP input						-4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-20		-100	-40		-110	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max				4	8		30	50	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[6]

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			$C_L = 15pF$		$C_L = 15pF$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		25 40		9 9	ns ns
t_{PLH}	Propagation delay	Waveform 2		25		6	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = High		40		13.5	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = Low		40		8	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_w(H)$	Clock pulse width (High)	Waveform 1	25		6		ns
$t_w(L)$	Clock pulse width (Low)	Waveform 1			7.3		ns
$t_w(L)$	Set or reset pulse width (Low)	Waveform 2	25		7		ns
$t_s(H)$	Setup time (High) data to clock	Waveform 1	20		3		ns
$t_s(L)$	Setup time (Low) data to clock	Waveform 1	20		3		ns
t_h	Hold time data to clock	Waveform 1	5		2		ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			$C_L = 50pF$		$C_L = 50pF$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		30 45		13 10	ns ns
t_{PLH}	Propagation delay	Waveform 2		30		8.0	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = High		45		16	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = Low		45		10	ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[6]

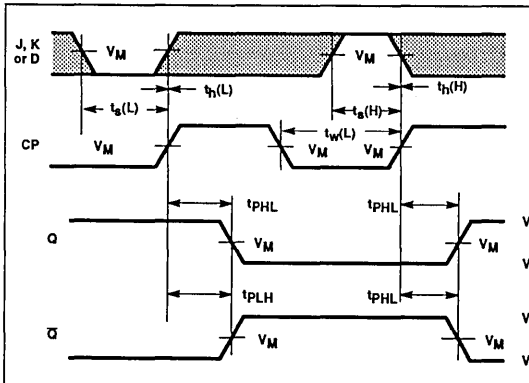
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			$C_L = 50pF$		$C_L = 50pF$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		55		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		39 59		16 13	ns ns
t_{PLH}	Propagation delay	Waveform 2		39		10	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = High		59		19	ns
t_{PHL}	Set or Reset to output	Waveform 2 CP = Low		59		13	ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

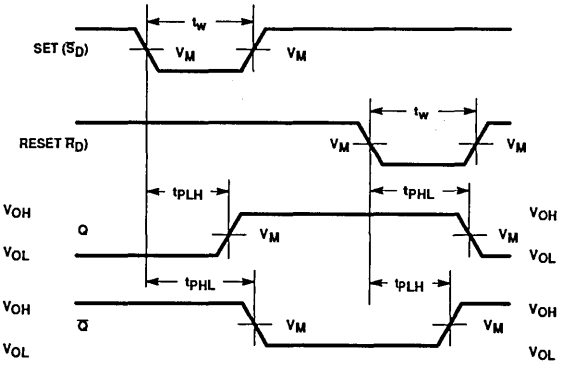
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_w(H)$	Clock pulse width (High)	Waveform 1	25		8		ns
$t_w(L)$	Clock pulse width (Low)	Waveform 1			10		ns
$t_w(L)$	Set or reset pulse width (Low)	Waveform 2	35		10		ns
$t_s(H)$	Setup time (High) data to clock	Waveform 1	20		4		ns
$t_s(L)$	Setup time (Low) data to clock	Waveform 1	20		4		ns
t_h	Hold time data to clock	Waveform 1	5		2		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and $\overline{Q}$ outputs High in turn.
5. Set is tested with reset High and reset is tested with set High.
6. These parameters are guaranteed, but not tested.

AC WAVEFORMS



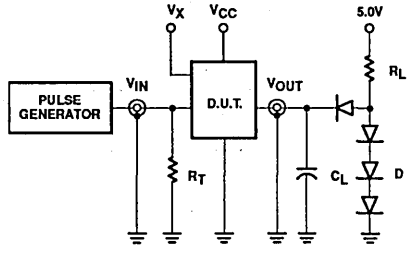
Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width



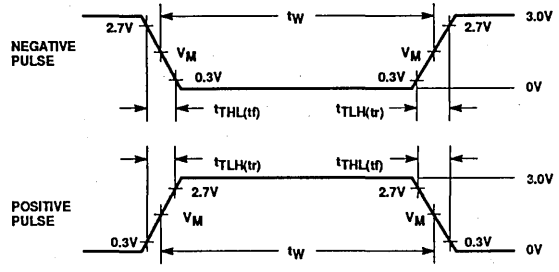
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths

NOTE: V_M = 1.3V for 54LS; V_M = 1.5V for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS75
Latch

Quad Bistable Latch

Product Specification

FEATURES

- **4-bit bistable latch**

DESCRIPTION

The 54LS75 has four bistable latches. Each 2-bit latch is controlled by an active High Enable input (E). When E is High the data enters the latch and appears at the Q output. The Q outputs follow the Data inputs as long as E is High. The data on the D inputs one setup time before the High-to-Low transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is Low.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS75/BEA
16-Pin Ceramic FlatPack	54LS75/BFA
16-Pin Ceramic LLCC	54LS75/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

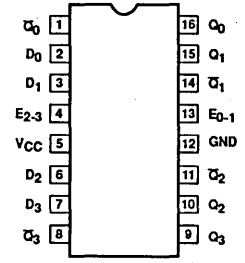
PINS	DESCRIPTION	54LS
D	Input	1LSUL
E	Input	4LSUL
All	Outputs	10LSUL

NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

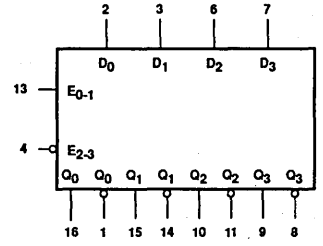
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

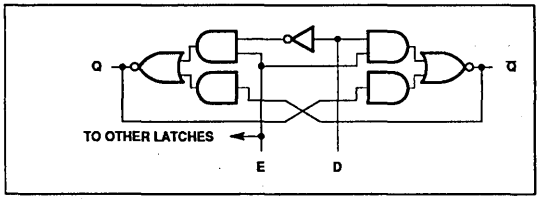
LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

Latch | 54LS75

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUT	
	E	D	Q	$\overline{Q}$
Data enabled	H H	L H	L H	H L
Data latched	L	X	q	$\overline{q}$

H = High voltage level
L = Low voltage level
X = Don't care
q = lower case letters indicate the state of referenced output one setup time prior to the High-to-Low Enable transition.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V	D inputs			0.1	mA
			E inputs			0.4	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	D inputs			20	µA
			E inputs			80	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V	D inputs			-0.4	mA
			E inputs			-1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			6.3	12	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Q output	Waveform 1		27 17	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Q}$ output	Waveform 2		20 15	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to Q output	Waveform 3		27 25	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Q}$ output	Waveform 3		30 15	ns ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Enable pulse width	Waveform 3	20		ns
t_s	Setup time, data to enable	Waveform 4	20		ns
t_h	Hold time, data to enable	Waveform 4	5.0		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Q output	Waveform 1		32 22	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Q}$ output	Waveform 2		25 20	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to Q output	Waveform 3		32 30	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Q}$ output	Waveform 3		35 20	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Q output	Waveform 1		42 29	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Q}$ output	Waveform 2		33 26	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to Q output	Waveform 3		42 39	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Q}$ output	Waveform 3		45.5 26.0	ns ns

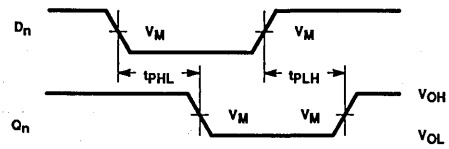
AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Enable pulse width	Waveform 3	20		ns
t_s	Setup time, data to enable	Waveform 4	20		ns
t_h	Hold time, data to enable	Waveform 4	5.0		ns

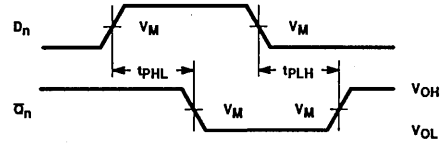
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.
5. These parameters are guaranteed, but not tested.

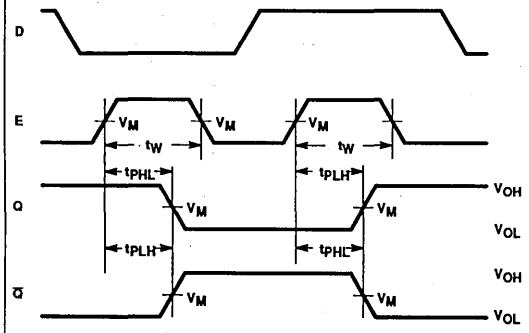
AC WAVEFORMS



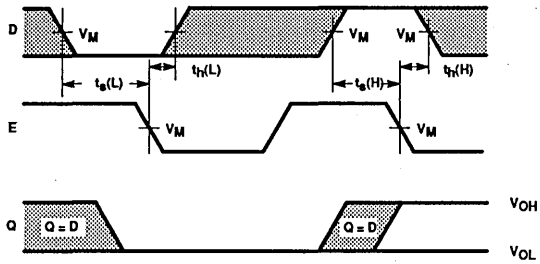
Waveform 1. Propagation Delay Data to Q Outputs



Waveform 2. Propagation Delay Data to Q̄ Outputs



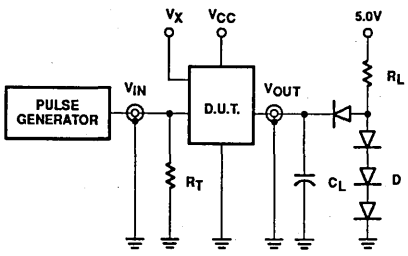
Waveform 3. Latch Enable to Output Delays and Latch Enable Pulse Width



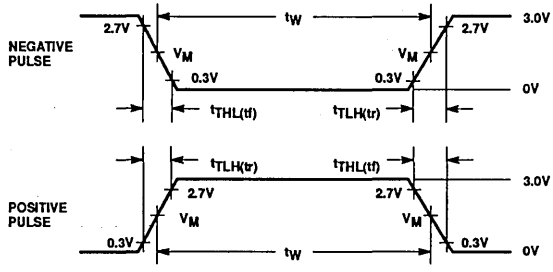
Waveform 4. Data Setup and Hold Times

NOTE: V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

5485, 54LS85, 54S85
Comparators

4-Bit Magnitude Comparators

Product Specification

FEATURES

- **Magnitude comparison of any binary words**
- **Serial or parallel expansion without extra gating**
- **Use 54S85 for very high-speed comparisons**

DESCRIPTION

The '85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A_0 - A_3) and (B_0 - B_3), where A_3 and B_3 are the most significant bits.

The operation of the '85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme.

ORDERING INFORMATION

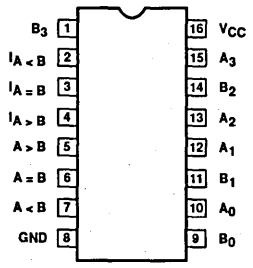
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS85/BEA 54S85/BEA 5485/BEA
16-Pin Ceramic FlatPack	54LS85/BFA 5485/BFA
16-Pin Ceramic LLCC	54LS85/B2A 54S85/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54S	54LS
A_0 - A_3, B_0 - B_3, $I_{A=B}$	Inputs	3UL	3SUL	3LSUL
$I_{A<B}$, $I_{A>B}$	Inputs	1UL	1SUL	1LSUL
A = B, A < B, A > B	Outputs	10UL	10SUL	10LSUL

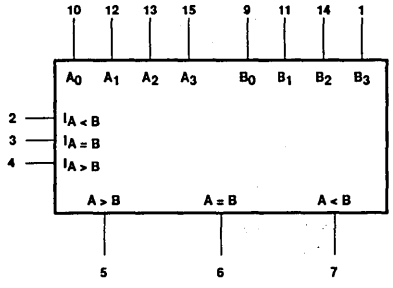
NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}, a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}, and 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



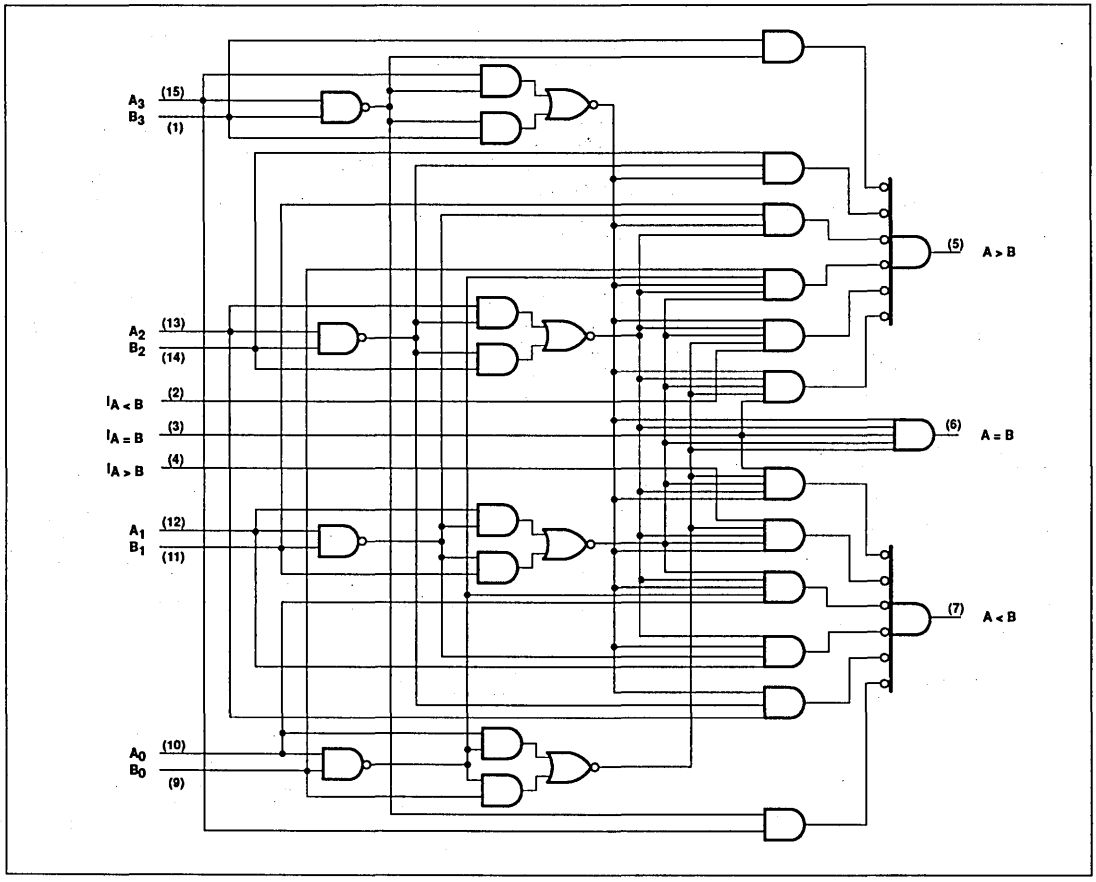
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A > B, A = B and A < B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = Low, $I_{A=B}$ = High, and $I_{A<B}$ = Low.

The parallel expansion scheme shown in Figure 1 demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ Low. The '85 can be used as a 5-bit comparator only when the outputs are used to drive the (A_0 - A_3) and (B_0 - B_3) inputs of another '85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A > B	A < B	A = B
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

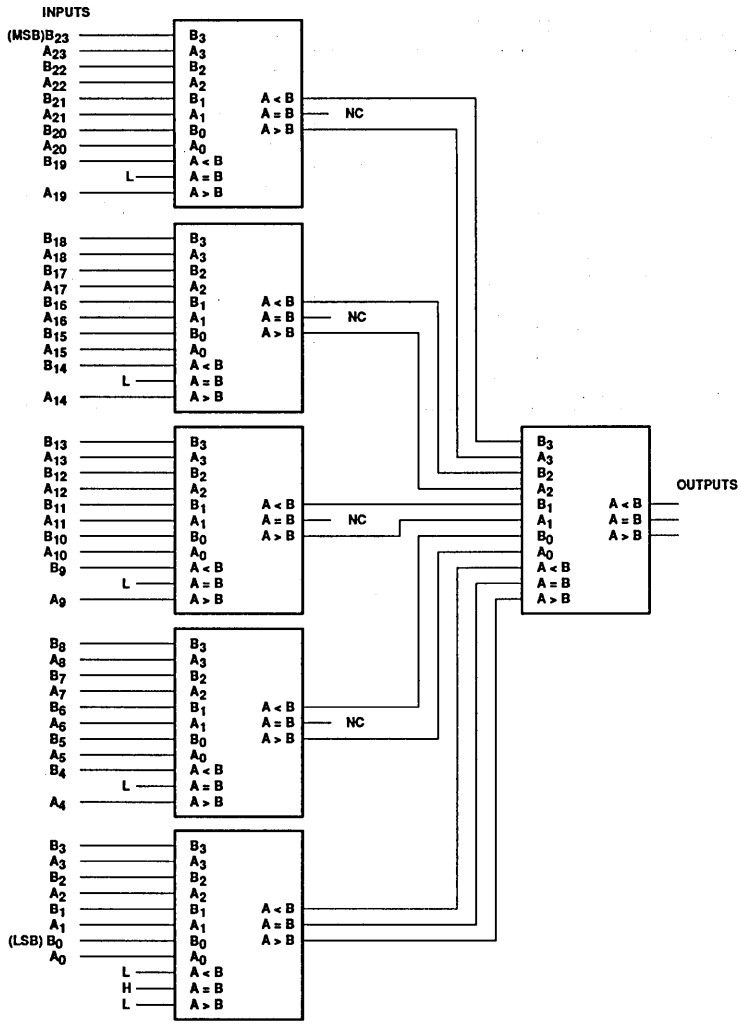


Figure 1. Comparison of Two 24-Bit Words

Table 1.

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS		
		54	54S	54LS
1 - 4 Bits	1	23ns	12ns	23ns
5 - 25 Bits	2 - 6	40ns	22ns	46ns
25 - 120 Bits	8 - 31	63ns	34ns	69ns

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150			°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		54			54LS			54S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			2.0			2.0			V
V_{IL}	Low-level input voltage				+0.8			+0.7			+0.8	V
		+125°C			+0.8			+0.7			+0.7	V
I_{IK}	Input clamp current				-12			-18			-18	mA
I_{OH}	High-level output current				-400			-400			-1000	µA
I_{OL}	Low-level output current				16			4			20	mA
T_A	Operating free-air temperature range		-55		+125	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			5485			54LS85			54S85			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max			2.4	3.4		2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max				0.2	0.4		0.25	0.4			0.5	V
				+125°C			0.4			0.4			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5			-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V	$I_{A<B}$, $I_{A>B}$						0.1				mA
				Other inputs						0.3				mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V	$I_{A<B}$, $I_{A>B}$			40							µA
				Other inputs			120							µA
			V_I = 2.7V	$I_{A<B}$, $I_{A>B}$						20			50	µA
				Other inputs						60			150	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V	$I_{A<B}$, $I_{A>B}$			-1.6			-0.4				mA
				Other inputs			-4.8			-1.2				mA
			V_I = 0.5V	$I_{A<B}$, $I_{A>B}$									-2.0	mA
				Other inputs									-6.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-18		-55	-20		-100	-40		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max				55	88		10.4	20		73	115	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS[5]		54S[5]		UNIT
			C_L = 15pF		C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B input to A < B, A > B output	Waveform 1 3 logic levels		26 30		36 30		16 16.5	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output	Waveform 2 4 logic levels		35 30		45 45		18 16.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ input to A > B output	Waveform 1 1 logic level		11 17		22 17		7.5 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ input to A = B output	Waveform 2 2 logic levels		20 17		20 26		10.5 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ input to A < B output	Waveform 1 1 logic level		11 17		22 17		7.5 8.5	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

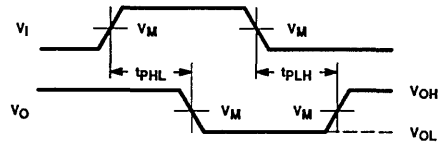
SYMBOL	PARAMETER	TEST CONDITIONS	54[5]		54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B input to A < B, A > B output	Waveform 1 3 logic levels		30 34		41 35		19.0 19.5	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output	Waveform 2 4 logic levels		39 34		50 50		19.5 19.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ input to A > B output	Waveform 1 1 logic level		15 21		27 22		9.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ input to A = B output	Waveform 2 2 logic levels		24 21		25 31		13.0 9.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ input to A < B output	Waveform 1 1 logic level		15 21		27 22		9.5 10.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V

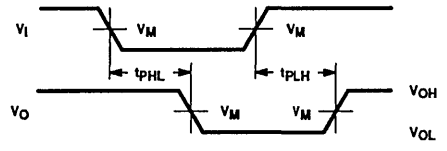
SYMBOL	PARAMETER	TEST CONDITIONS	54[5]		54LS[5]		54S[5]		UNIT
			C_L = 50pF		C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B input to A < B, A > B output	Waveform 1 3 logic levels		39 44		53 46		23 24	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output	Waveform 2 4 logic levels		51 44		65 65		25 24	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ input to A > B output	Waveform 1 1 logic level		20 27		35 29		11.5 13	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ input to A = B output	Waveform 2 2 logic levels		31 27		33 40		16 12	ns ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ input to A < B output	Waveform 1 1 logic level		20 27		35 29		11.5 13	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open, A = B grounded, and all other inputs at ≥ 4.0V.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



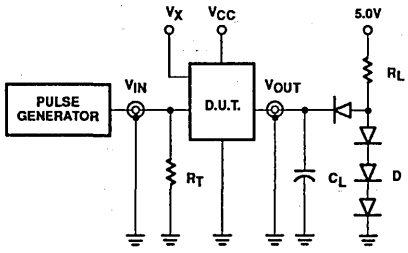
Waveform 1. Waveform for Inverting Outputs



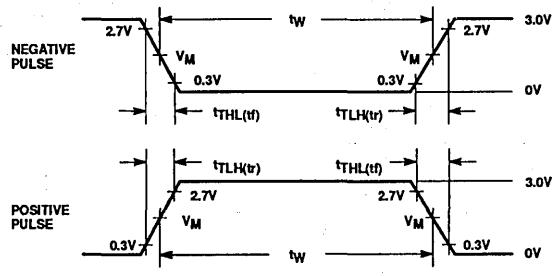
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.3V for 54LS, V_M = 1.5V for all other TTL families.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS86, 54S86
Gates

Quad Two-Input Exclusive-OR Gates

Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54LS86/BCA, 54S86/BCA
14-Pin Ceramic Flat Pack	54LS86/BDA, 54S86/BDA
Ceramic LLCC	54LS86/B2A, 54S86/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

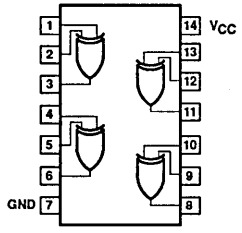
PINS	DESCRIPTION	54S	54LS
A, B	Inputs	1SUL	1LSUL
Y	Output	10SUL	10LSUL

NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

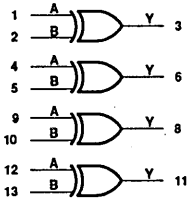
SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +5.5	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		54LS			54S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			2.0			V
V_{IL}	Low-level input voltage				+0.7			+0.8	V
		+125°C			+0.7			+0.7	V
I_{IK}	Input clamp current				-18			-18	mA
I_{OH}	High-level output current				-400			-1000	µA
I_{OL}	Low-level output current				4			20	mA
T_A	Operating free-air temperature range		-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free–air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54LS86			54S86			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,			0.25	0.4			0.5	V
		I_{OL} = Max	+125°C			0.4			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V						1.0	mA
			V_I = 7.0V			0.2				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				40			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V			-0.8				mA
			V_I = 0.5V						-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-110	-40		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			0.1	10		50	75	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S[5]		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to output	Other input Low Waveform 2		23 17		10.5 10	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Other input High Waveform 1		30 22		10.5 10	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

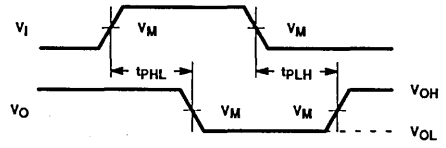
SYMBOL	PARAMETER	TEST CONDITIONS	54LS[5]		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to output	Other input Low Waveform 2		25 22		12.5 12	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Other input High Waveform 1		35 27		12.5 12	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = –55°C and + 125°C, V_{CC} = 5.0V[5]

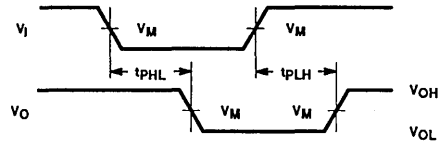
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to output	Other input Low Waveform 2		33 29		16.5 15.5	ns ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Other input High Waveform 1		46 35		16.5 15.5	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with inputs grounded and outputs open.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



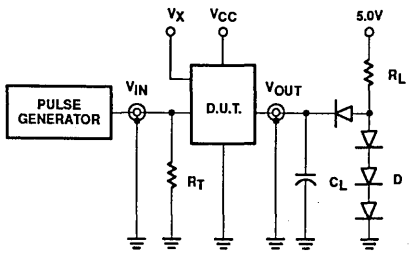
Waveform 1. Waveform for Inverting Outputs



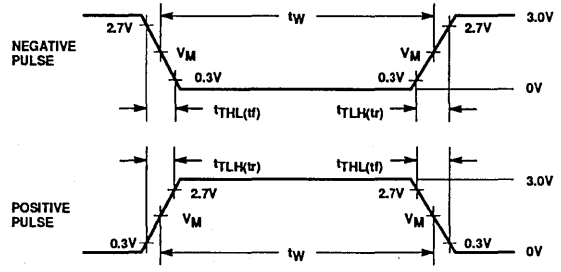
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.3V for 54LS, V_M = 1.5V for all other TTL families.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

5493
Counter

4-Bit Binary Ripple Counter

Product Specification

Military Logic Products

DESCRIPTION

The 5493 is a 4-bit, ripple-type Binary Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate Clock input to initiate state changes of the counter on the High-to-Low clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \bullet MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q_0 must be connected externally to input $\overline{CP}_1$.

The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_0, Q_1, Q_2 and Q_3 outputs as shown in the Function Table.

As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

ORDERING INFORMATION

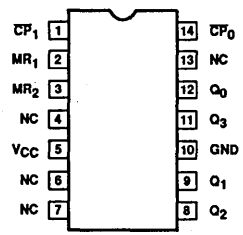
DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	5493/BCA
14-Pin Ceramic FlatPack	5493/BDA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54
MR	Master reset inputs	1UL
$\overline{CP}_0$	Input	2UL
$\overline{CP}_1$	Input	2UL
Q_0 - Q_3	Outputs	10UL

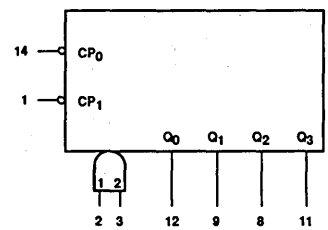
NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}.

PIN CONFIGURATION



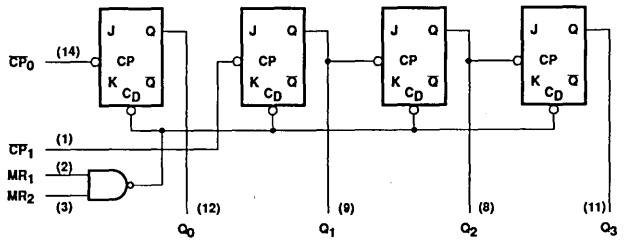
For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC DIAGRAM



( ) = Pin number
V_{CC} = Pin 5
GND = Pin 10

FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q_0 connected to input $\overline{CP}_1$.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-12	mA
I_{OH}	High-level output current			-800	µA
I_{OL}	Low-level output current			16	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input currrent	V_{CC} = Max, V_I = 2.4V	MR inputs			40	µA
			$\overline{CP}_0$, $\overline{CP}_1$ inputs			80	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V	MR inputs			-1.6	mA
			$\overline{CP}_0$ input			-3.2	mA
			$\overline{CP}_1$ input			-3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-18		-55	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			28	46	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
f_{MAX} f_{MAX}	$\overline{CP}_0$ input count frequency $\overline{CP}_1$ input count frequency	Waveform 1	10 10		MHz MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_0 output	Waveform 1		33 33	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_1 output	Waveform 1		33 33	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_2 output	Waveform 1		67 67	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_3 output	Waveform 1		102 102	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_3 output	Waveform 1		135 135	ns ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMIT		UNIT
			Min	Max	
t_W	$\overline{CP}_0$ pulse width	Waveform 1	50		ns
t_W	$\overline{CP}_1$ pulse width	Waveform 1	50		ns
t_W	MR pulse width	Waveform 2	50		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX} f_{MAX}	$\overline{CP}_0$ input count frequency $\overline{CP}_1$ input count frequency	Waveform 1	10 10		MHz MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_0 output	Waveform 1		37 37	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_1 output	Waveform 1		37 37	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_2 output	Waveform 1		71 71	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_3 output	Waveform 1		106 106	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_3 output	Waveform 1		143 143	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

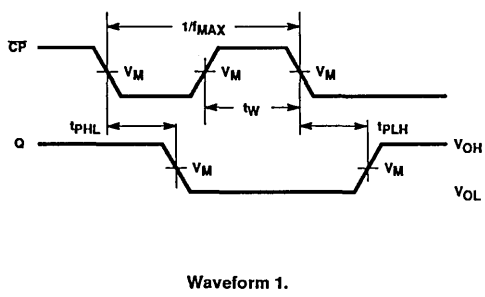
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX} f_{MAX}	$\overline{CP}_0$ input count frequency $\overline{CP}_1$ input count frequency	Waveform 1	10 10		MHz MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_0 output	Waveform 1		48 48	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_1 output	Waveform 1		48 48	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_2 output	Waveform 1		87 87	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_3 output	Waveform 1		138 138	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_3 output	Waveform 1		186 186	ns ns

AC SETUP REQUIREMENTS T_A = -55°C and + 125°C, V_{CC} = 5.0V[5]

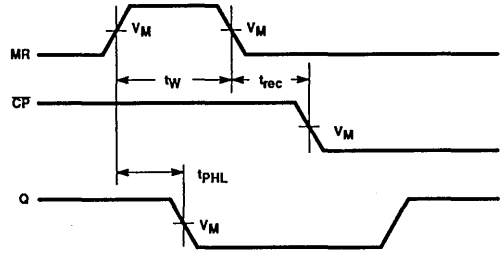
SYMBOL	PARAMETER	TEST CONDITIONS	LIMIT		UNIT
			Min	Max	
t_W	$\overline{CP}_0$ pulse width	Waveform 1	50		ns
t_W	$\overline{CP}_1$ pulse width	Waveform 1	50		ns
t_W	MR pulse width	Waveform 2	50		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection $\geq$ 4.0V, and all other inputs grounded.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



Waveform 1.

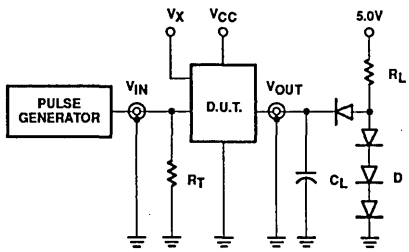


Waveform 2.

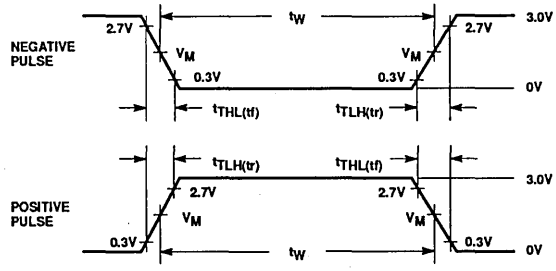
NOTE: V_M = 1.5V

The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS109
Flip-Flop

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop

Product Specification

DESCRIPTION

The 54LS109 is a dual positive edge-triggered J$\overline{K}$-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs; also complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active Low inputs and operate independently of the Clock input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Mode Select-Truth Table.

The J and $\overline{K}$ inputs must be stable just one set-up time prior to the Low-to-High transition of the Clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.7V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

ORDERING INFORMATION

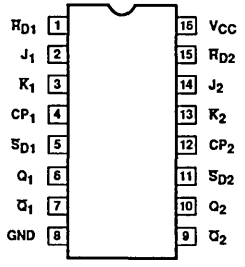
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS109/BEA
16-Pin Ceramic FlatPack	54LS109/BFA
16-Pin Ceramic LLCC	54LS109/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
CP	Clock input	1LSUL
$\overline{R}_D$	Reset input	2LSUL
$\overline{S}_D$	Set input	2LSUL
J, $\overline{K}$	Data inputs	1LSUL
Q, $\overline{Q}$	Outputs	10LSUL

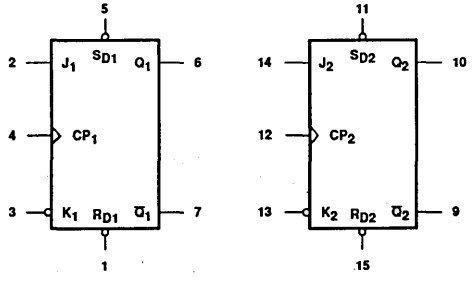
NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

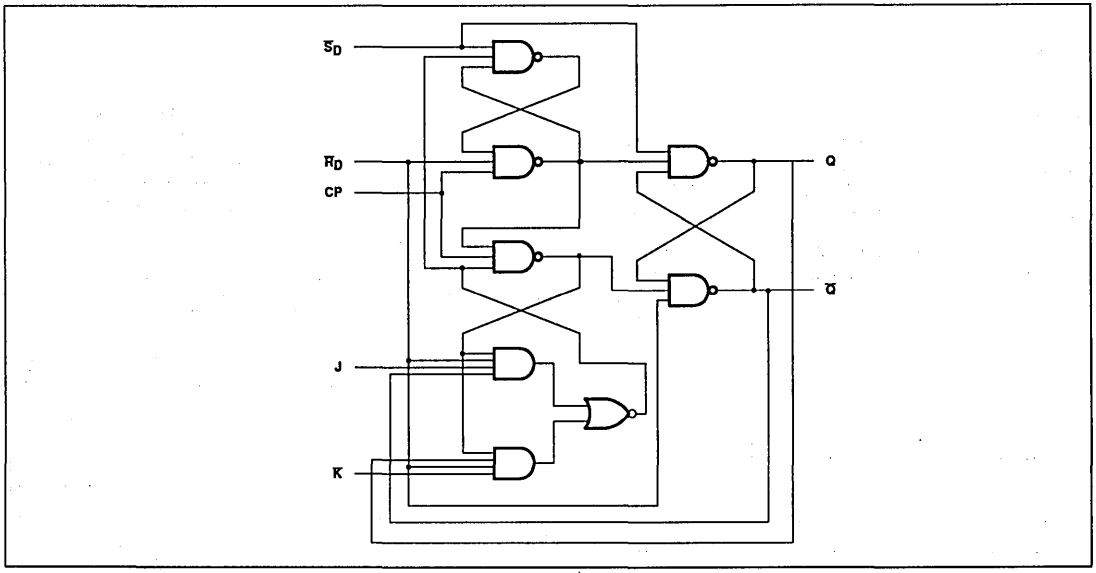
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

Flip-Flop | 54LS109

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (note)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load "0" (reset)	H	H	↑	l	l	L	H
Load "1" (set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = High voltage level steady state.
L = Low voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High Clock transition.
l = Low voltage one setup time prior to the Low-to-High Clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High Clock transition.
↑ = Low-to-High Clock transition.

NOTE: Both outputs will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V	J, $\overline{K}$ inputs			0.1	mA
			$\overline{R}_D$, $\overline{S}_D$ inputs			0.2	mA
			CP inputs			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	J, $\overline{K}$ inputs			20	µA
			$\overline{R}_D$, $\overline{S}_D$ inputs			40	µA
			CP inputs			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V	J, $\overline{K}$ inputs			-0.4	mA
			$\overline{R}_D$, inputs			-0.8	mA
			$\overline{S}_D$ inputs			-0.8	mA
			CP inputs			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			4	8	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		25 40	ns ns
t_{PLH} t_{PHL}	Propagation delay Reset to output	Waveform 2		25 40	ns ns
t_{PLH} t_{PHL}	Propagation delay Set to output	Waveform 2		25 40	ns ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMIT		UNIT
			Min	Max	
t_w(H)	Clock pulse width (High)	Waveform 1	25		ns
t_w(L)	Clock pulse width (Low)	Waveform 1	15		ns
t_w(L)	Set or reset pulse width (Low)	Waveform 2	25		ns
t_s	Set-up time J or $\overline{K}$ to clock	Waveform 1	20		ns
t_h	Hold time J or $\overline{K}$ to clock	Waveform 1	5.0		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		30 45	ns ns
t_{PLH} t_{PHL}	Propagation delay Reset to output	Waveform 2		30 45	ns ns
t_{PLH} t_{PHL}	Propagation delay Set to output	Waveform 2		30 45	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[5]

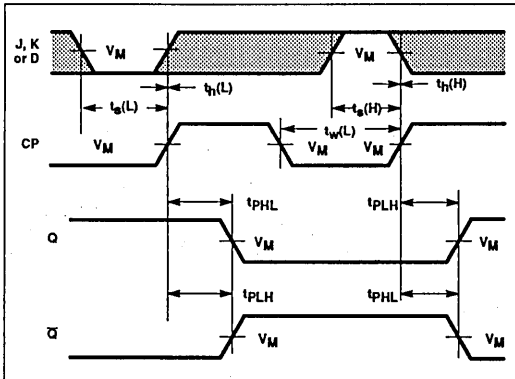
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		39 59	ns ns
t_{PLH} t_{PHL}	Propagation delay Reset to output	Waveform 2		39 59	ns ns
t_{PLH} t_{PHL}	Propagation delay Set to output	Waveform 2		39 59	ns ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

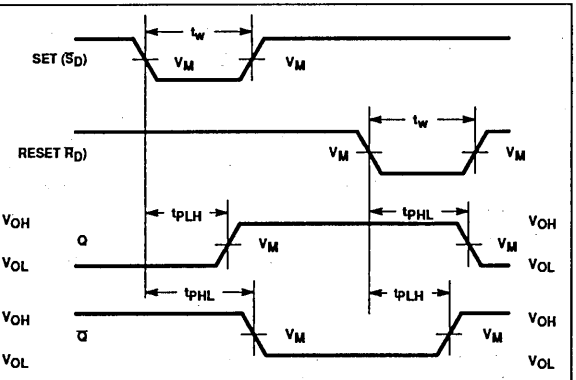
SYMBOL	PARAMETER	TEST CONDITIONS	LIMIT		UNIT
			Min	Max	
t_w(H)	Clock pulse width (High)	Waveform 1	25		ns
t_w(L)	Clock pulse width (Low)	Waveform 1	25		ns
t_w(L)	Set or reset pulse width (Low)	Waveform 2	25		ns
t_s	Set-up time J or $\overline{K}$ to clock	Waveform 1	25		ns
t_h	Hold time J or $\overline{K}$ to clock	Waveform 1	5.0		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



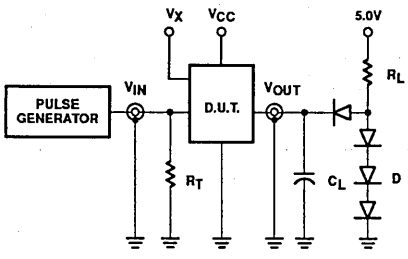
Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width



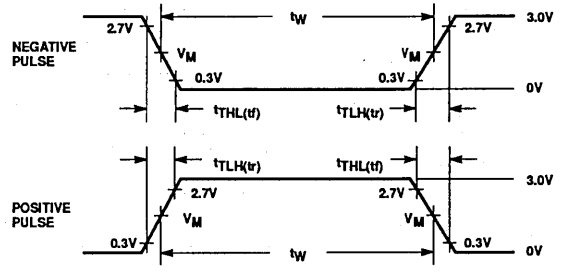
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths

NOTE: V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54S112
Flip-Flop

Dual J-K Edge-Triggered Flip-Flop

Product Specification

Military Logic Products

DESCRIPTION

The 54S112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when Low, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A High level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is High and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the High-to-Low transition of $\overline{CP}$.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54S112/BEA
16-Pin Ceramic FlatPack	54S112/BFA
16-Pin Ceramic LLCC	54S112/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

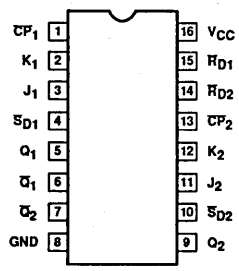
PINS	DESCRIPTION	54S
$\overline{CP}$	Clock input	2SUL
$\overline{R}_D$, $\overline{S}_D$	Reset and Set inputs	3.5SUL
J, K	Data inputs	1SUL
Q, $\overline{Q}$	Outputs	10SUL

NOTE: A 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

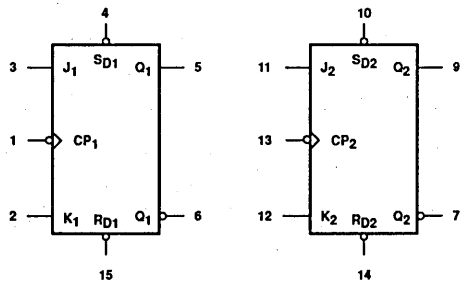
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +125	°C

PIN CONFIGURATION



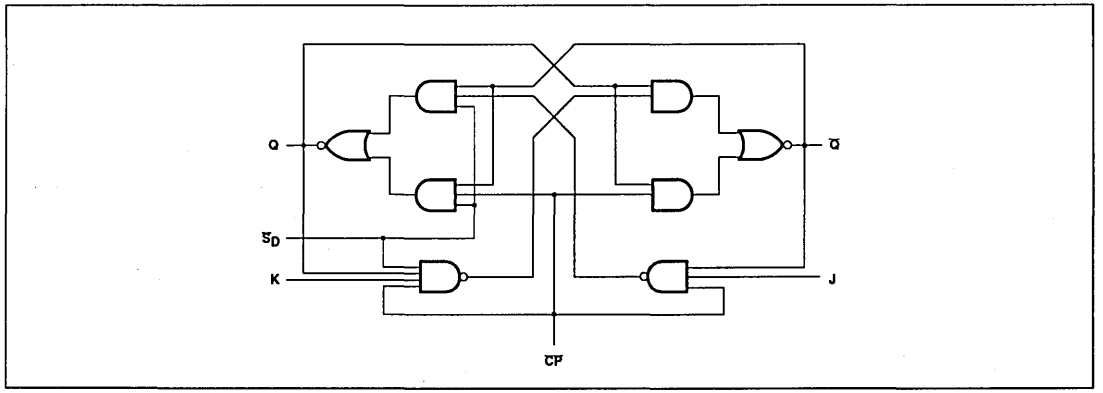
For LLCC Pin Assignment, see Jedec Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignment, see Jedec Standard No. 2

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous reset (clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = High voltage level steady state.
h = High voltage level one setup time prior to the High-to-Low Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the High-to-Low Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low Clock transition.
X = Don't Care.
↓ = High-to-Low Clock transition.

NOTE:
Both outpus will be High while both $\overline{S}_D$ and $\overline{R}_D$ are Low, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go High simultaneously.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
	+125°C			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1000	µA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max				0.5	V
			+125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	J, K inputs			50	µA
			$\overline{R}_D$, $\overline{S}_D$ inputs			100	µA
			$\overline{CP}$ inputs			100	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V	J, K inputs			-1.6	mA
			$\overline{R}_D$, $\overline{S}_D$ inputs			-7	mA
			$\overline{CP}$ inputs			-4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-40		-110	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			15	50	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		7.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_D$ or $\overline{R}_D$ to output	Waveform 2		7.0 7.0	ns ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_w(H)	Clock pulse width (High)	Waveform 1	6.0		ns
t_w(L)	Clock pulse width (Low)	Waveform 1	6.5		ns
t_w(L)	Set or reset pulse width (Low)	Waveform 2	8.0		ns
t_s	Setup time J or K to clock	Waveform 1	4.0		ns
t_h	Hold time J or K to clock	Waveform 1	0		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	80		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_D$ or $\overline{R}_D$ to output	Waveform 2		9.0 9.0	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

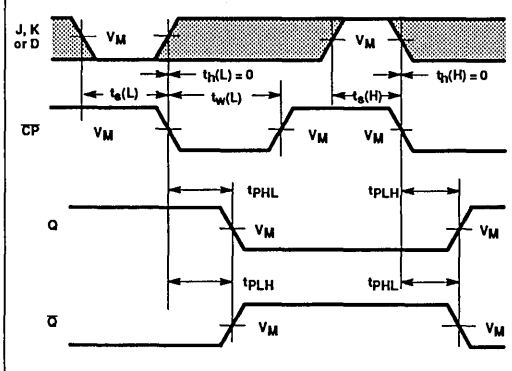
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	60		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		11.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_D$ or $\overline{R}_D$ to output	Waveform 2		11.0 11.0	ns ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

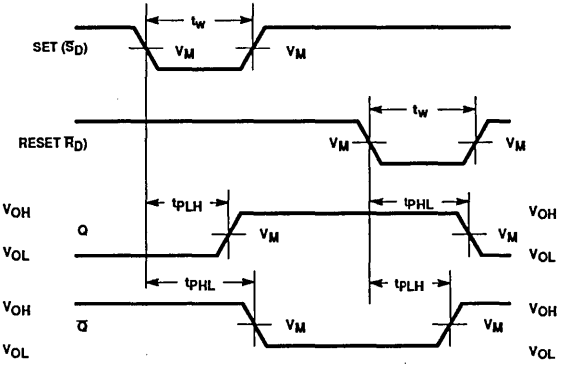
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_w(H)	Clock pulse width (High)	Waveform 1	10		ns
t_w(L)	Clock pulse width (Low)	Waveform 1	10		ns
t_w(L)	Set or reset pulse width (Low)	Waveform 2	10		ns
t_s	Setup time J or K to clock	Waveform 1	9.0		ns
t_h	Hold time J or K to clock	Waveform 1	2		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs High in turn.
5. These parameters are guaranteed, but not0 tested.

AC WAVEFORMS



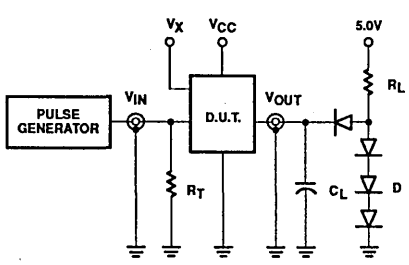
Waveform 1. Clock to Output Delays, Data Setup and Hold Times, Clock Pulse Width



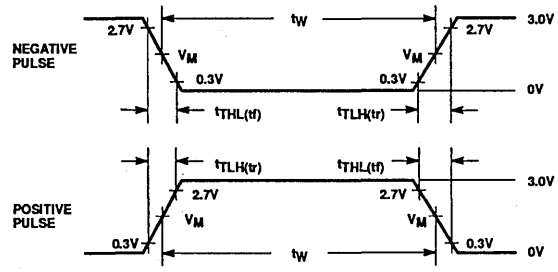
Waveform 2. Set and Reset to Output Delays, Set and Reset Pulse Widths

NOTE: V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54123
Multivibrator

Dual Retriggerable Monostable Multivibrator

Product Specification

Military Logic Products

FEATURES

- **DC triggered from active High or active Low inputs**
- **Retriggerable for very long pulses – up to 100% duty cycle**
- **Direct reset terminates output pulse**
- **Compensated for V_{CC} and temperature variations**

DESCRIPTION

The 54123 is a dual retriggerable monostable multivibrator with output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance (R_{ext}) and capacitance (C_{ext}) values. Once triggered, the basic pulse width may be extended by retriggering the gated active Low going edge input ($\overline{A}$) or the active High going edge input (B), or be reduced by use of the overriding acting Low reset.

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq 1000pf$, see Figure A.

When $C_{ext} > 1000pf$, the output pulse width is defined as:

$$t_W = 0.28\ R_{ext} \cdot C_{ext} \left(1 + \frac{0.7}{R_{ext}}\right)$$

The external resistance and capacitance are normally connected as shown in Figure B. If any electrolytic capacitor is to be used with an inverse voltage rating of less than 1V then Figure C should be used. (Inverse voltage rating of an electrolytic is normally specified at 5% of the forward voltage rating.) If the inverse voltage rating is 1V or more (this includes a 100% safety margin), then Figure B can be used. Note that if Figure C is used, the timing equations change as follows:

$$t_W \cong 0.25\ R_{ext} \cdot C_{ext} \left(1 + \frac{0.7}{R_{ext}}\right)$$

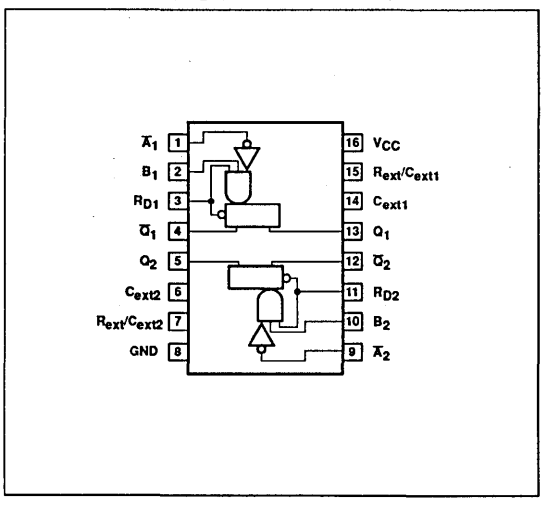
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54123/BEA

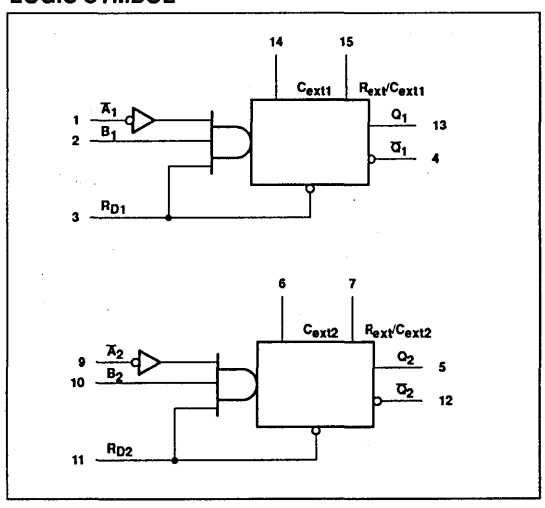
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V	Voltage applied to output in High outpt state range	-0.5 to $+V_{CC}$	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



LOGIC SYMBOL



Multivibrator 54123

FUNCTION TABLE

INPUTS			OUTPUTS	
R_D	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High transition
↓ = High-to-Low transition
⎍ = One High-level pulse
⎎ = One Low-level pulse

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54(U.L.)
$\overline{A}$, B	Inputs	1.0
R_D	Input	1.0
Q, $\overline{Q}$	Outputs	10

NOTE: A 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-12	mA
I_{OH}	High-level output current			-800	μA
I_{OL}	Low-level output current			16	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage[5]	V_{CC} = Min, I_{OH} = Max		2.4	3.4		V
V_{OL}	Low-level output voltage[5]	V_{CC} = Min, I_{OL} = Max			0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.4V	$\overline{A}$, B inputs			40	μA
			R_D inputs			80	μA
I_{IL}	High-level input current	V_{CC} = Max, V_I = 0.4V	$\overline{A}$, B inputs			-1.6	mA
			R_D inputs			-3.2	mA
I_{OS}	Short-circuit output current[3,5]	V_{CC} = Max		-10		-40	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	Quiescent		46	66	mA
			Triggered		46	66	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[6]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 15pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ input to Q & $\overline{Q}$ output	Waveform 1 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		33 40	ns ns
t_{PLH} t_{PHL}	Propagation delay B input to Q & $\overline{Q}$ output	Waveform 2 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		28 36	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{R}_D$ input to Q & $\overline{Q}$ output	Waveform 3 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		40 27	ns ns
t_WQ	Minimum Q pulse width	Waveforms 1 & 2 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		65	ns
t_WQ	Output pulse width	Waveforms 1 & 2 $C_{ext} = 1000pF$, $R_{ext} = 10k\Omega$	2.76	3.37	µS

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Minimum input pulse width	Waveforms 1, 2 & 3	40		ns
R_{ext}	External timing resistor range		5.0	25	kΩ
C_{ext}	External timing capacitance range		No restriction		pF
$C_{Rx/Cx}$	Stray capacitance to GND at R_{ext}/C_{ext} terminal			50	pF

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ input to Q & $\overline{Q}$ output	Waveform 1 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		37 44	ns ns
t_{PLH} t_{PHL}	Propagation delay B input to Q & $\overline{Q}$ output	Waveform 2 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		32 40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{R}_D$ input to Q & $\overline{Q}$ output	Waveform 3 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		44 31	ns ns
t_WQ	Minimum Q pulse width	Waveforms 1 & 2 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		65	ns
t_WQ	Output pulse width	Waveforms 1 & 2 $C_{ext} = 1000pF$, $R_{ext} = 10k\Omega$	2.76	3.37	µS

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[6]

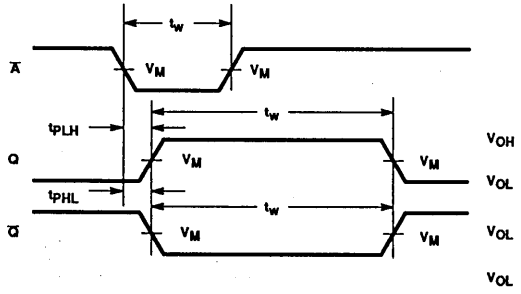
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ input to Q & $\overline{Q}$ output	Waveform 1 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		48 57	ns ns
t_{PLH} t_{PHL}	Propagation delay B input to Q & $\overline{Q}$ output	Waveform 2 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		42 52	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{R}_D$ input to Q & $\overline{Q}$ output	Waveform 3 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		57 40	ns ns
t_wQ	Minimum Q pulse width	Waveforms 1 & 2 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		75	ns
t_wQ	Output pulse width	Waveforms 1 & 2 $C_{ext} = 1000pF$, $R_{ext} = 10k\Omega$	2.5	3.62	µs

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

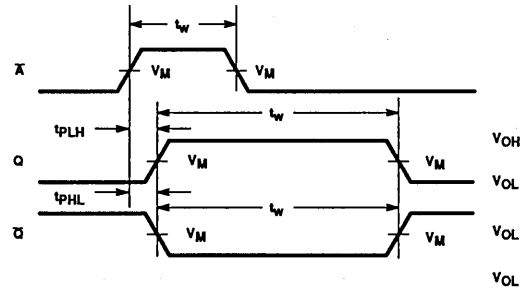
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Minimum input pulse width	Waveforms 1, 2 & 3	60		ns
R_{ext}	External timing resistor range		5.0	25	kΩ
				50	kΩ
C_{ext}	External timing capacitance range		No restriction		pF
$C_{Rx/Cx}$	Stray capacitance to GND at R_{ext}/C_{ext} terminal			50	pF

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Quiescent I_{CC} is measure (after being reset) with 2.4V applied to both R_D and $\overline{A}$ inputs, B inputs grounded and all outputs open. Triggered I_{CC} is measured with 2.4V applied to all R_D and B inputs, $\overline{A}$ inputs grounded and all outputs open. For both measurements, C_{ext} = 0.02μF and R_{ext} = 25kΩ. Autotester may measure I_{CC} by alternative means. I_{CC} triggered, ground C_{ext}, R/C open or high. I_{CC} quiescent open C_{ext} pin.
5. Ground C_{ext} to measure V_{OH} at Q, V_{OH} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. These parameters are guaranteed, but not tested.

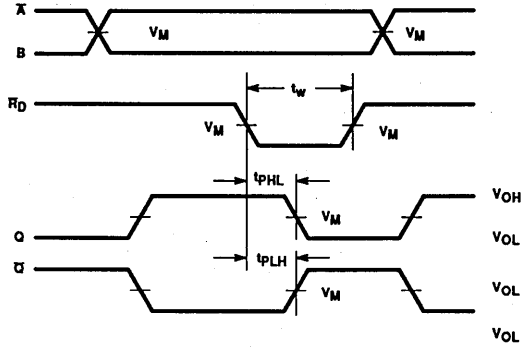
AC WAVEFORMS



Waveform 1. Propagation Delay $\overline{A}$ Input to Q and $\overline{Q}$ Outputs, and Input and Output Pulse Widths



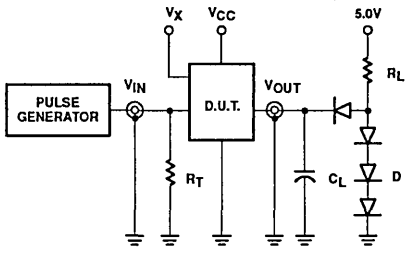
Waveform 2. Propagation Delay B Input to Q and $\overline{Q}$ Outputs, and Input and Output Pulse Widths



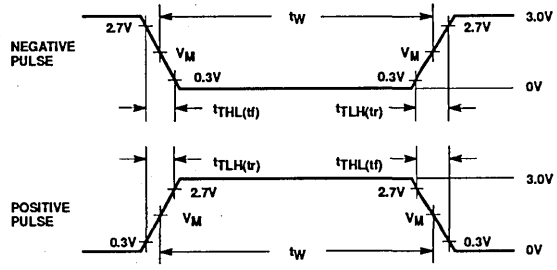
Waveform 3. Direct Reset Delays

NOTE: V_M = 1.5V for 54

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

TYPICAL PERFORMANCE CHARACTERISTICS

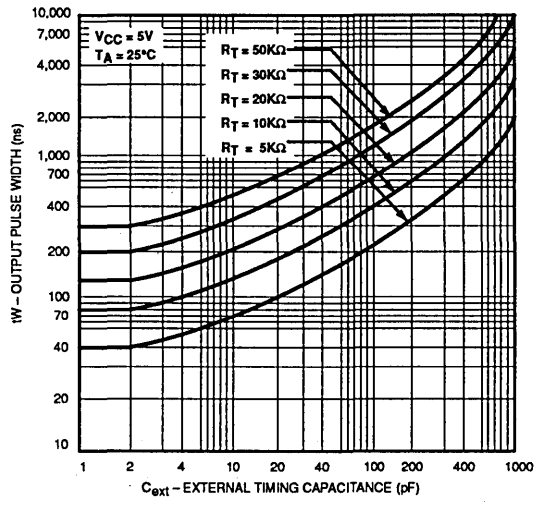


Figure A

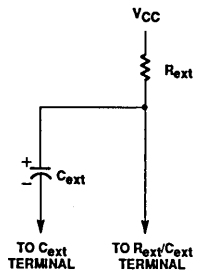


Figure B

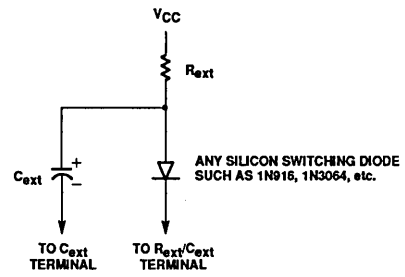


Figure C

Signetics

Military Logic Products

54LS125
Buffer

Quad 3-State Buffer

Product Specification

FUNCTION TABLE

INPUTS		OUTPUT
C	A	Y
L	L	H
L	H	H
H	X	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off)

ORDERING INFORMATION.

DESCRIPTION	ORDER CODE
Ceramic DIP	54LS125/BCA
Ceramic Flat Pack	54LS125/BDA
Ceramic LLCC	54LS125/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

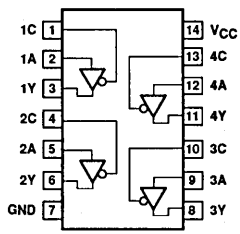
PINS	DESCRIPTION	54LS
All	Inputs	1LSUL
All	Outputs	30LSUL

NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

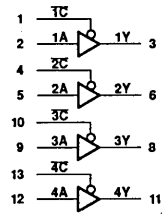
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-1.5	V
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_{IL} = Max, V_O = 2.4V			20	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_{IL} = Max, V_O = 0.4V			-20	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-40		-130	mA
I_{CC}	Supply current (total)	V_{CC} = Max		11	20	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

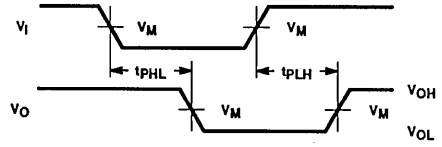
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		15 18	ns ns
t_{PZH}	Enable to High	Waveform 2		20	ns
t_{PZL}	Enable to Low	Waveform 3		25	ns
t_{PHZ}	Disable from High	Waveform 2, C_L = 5pF		20	ns
t_{PLZ}	Disable from Low	Waveform 3, C_L = 5pF		20	ns
t_{PHZ}	Disable from High	Waveform 2, C_L = 50pF		36	ns
t_{PLZ}	Disable from Low	Waveform 3, C_L = 50pF		22	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[4]

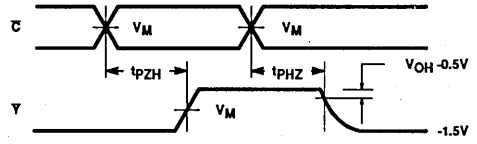
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		20 24	ns ns
t_{PZH}	Enable to High	Waveform 2		26	ns
t_{PZL}	Enable to Low	Waveform 3		33	ns
t_{PHZ}	Disable from High	Waveform 2, C_L = 5pF		26	ns
t_{PLZ}	Disable from Low	Waveform 3, C_L = 5pF		26	ns
t_{PHZ}	Disable from High	Waveform 2, C_L = 50pF		47	ns
t_{PLZ}	Disable from Low	Waveform 3, C_L = 50pF		29	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
4. These parameters are guaranteed, but not tested.

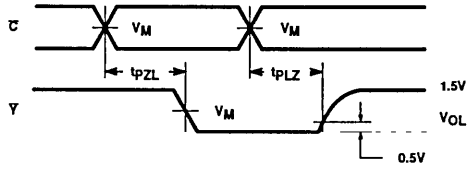
AC WAVEFORMS



Waveform 1. Waveform for Non-Inverting Outputs



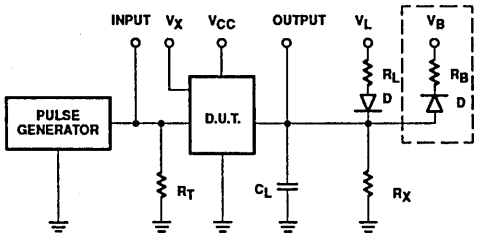
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



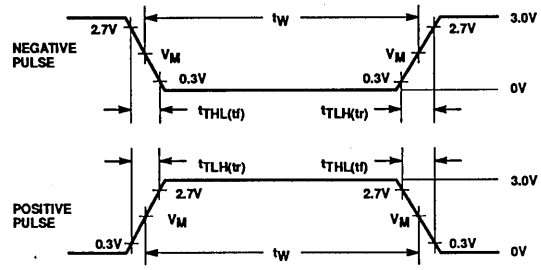
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns

Optional load for 54LSXXX only: R_B = 631°C; V_B = 5.5V for all tests except T_{PHZ}: V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54S133
Gate

13-Input NAND Gate

Product Specification

FUNCTION TABLE

INPUTS	OUTPUT
A . . M	Ȳ
H . . H	L
one input = L	H

H = High voltage level
L = Low voltage level

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54S133/BEA
Ceramic Flat Pack	54S133BFA
Ceramic LLCC	54S133/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

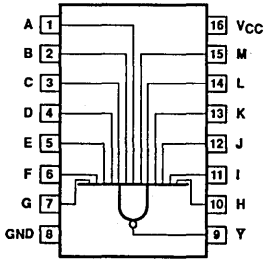
PINS	DESCRIPTION	54S
All	Inputs	1SUL
Ȳ	Output	10SUL

NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

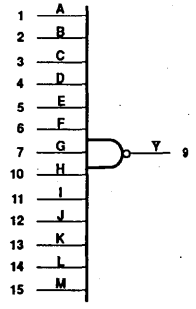
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				+0.8	V
		+125°C			+0.7	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-1000	µA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min,				0.5	V
		I_{OL} = Max	+125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V				-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-40		-110	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High		3	5	mA
			I_{CCL} Outputs Low		5.5	10	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		6.0 7.0	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[4]

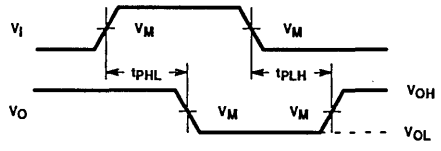
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		8.5 9.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[4]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		11.0 12.0	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. These parameters are guaranteed, but not tested.

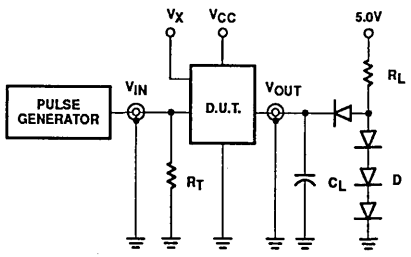
AC WAVEFORM



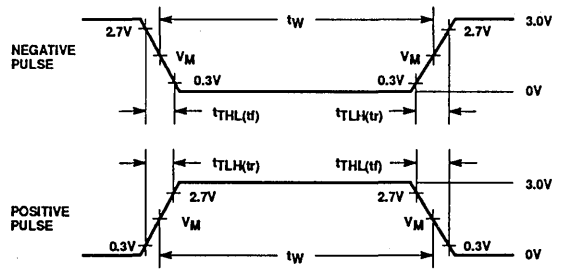
NOTE: V_M = 1.5V

Waveform 1. Waveform for Inverting Outputs

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

54LS138, 54S138
Decoders/Demultiplexers

1-of-8 Decoder/Demultiplexer

Product Specification

Military Logic Products

FEATURES

- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Direct replacement for Intel S205**

DESCRIPTION

The '138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active Low outputs ($\overline{0}$ - $\overline{7}$). The device features three Enable inputs: two active Low (E_1, E_2) and one active High (E_3). Every output will be High unless $\overline{E}_1$ and $\overline{E}_2$ are Low and E_3 is High. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active Low Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active High or active Low state.

ORDERING INFORMATION

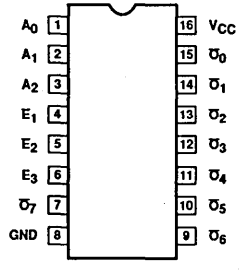
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS138/BEA, 54S138/BEA
16-Pin Ceramic FlatPack	54LS138/BFA, 54S138/BFA
16-Pin Ceramic LLCC	54LS138/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S	54LS
All	Inputs	1SUL	1LSUL
All	Outputs	10SUL	10LSUL

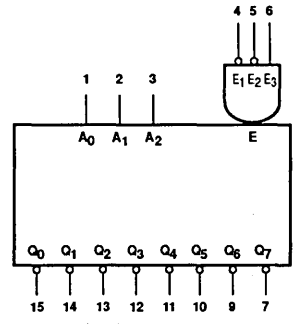
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}, and 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



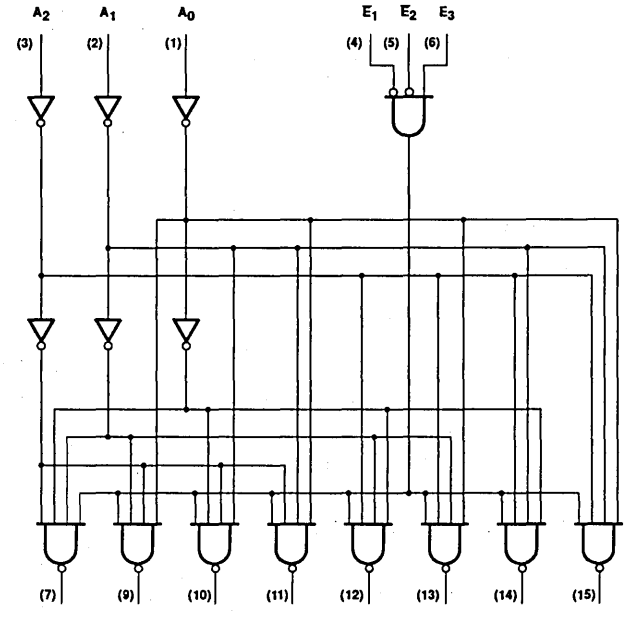
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



( ) = Pin number
V_{CC} = Pin 16
GND = Pin 8

For LLCC pin assignments, see JEDEC Standard No. 2.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150		°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.7			+0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-400			-1000	µA
I_{OL}	Low-level output current			4			20	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54LS138			54S138			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V						1.0	mA
			V_I = 7.0V			0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V			-0.4				mA
			V_I = 0.5V						-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	-40		-110	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			6.3	10		49	74	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS[5]		54S		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		20 41		7 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		27 39		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		18 32		8 11	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1 3 logic levels		26 38		11 11	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

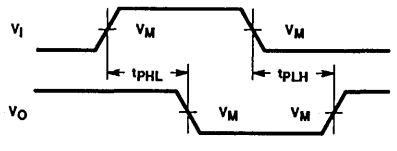
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S[5]		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		25 46		9.5 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		32 44		14.5 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		23 37		10.5 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1 3 logic levels		31 43		13.5 13.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

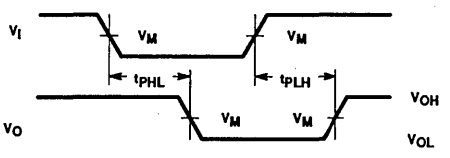
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		32 59		12.5 17	ns ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		41 57		19 19	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		30 48		13.5 17.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1 3 logic levels		40 56		17.5 17.5	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. To measure I_{CC}, outputs must be enabled and open.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



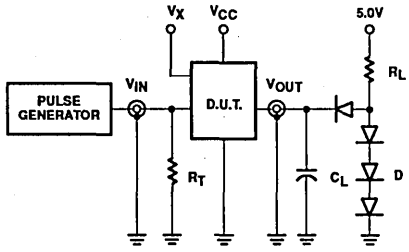
Waveform 1. Waveform for Inverting Outputs



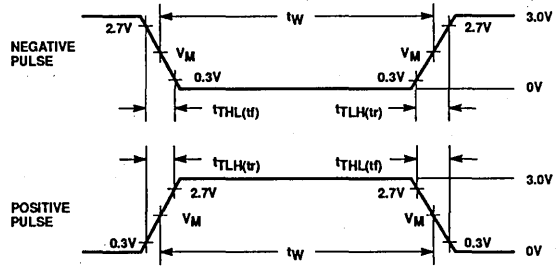
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.3V for 54LS, V_M = 1.5V for all other TTL families.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54S140
Line Driver

Dual Four-Input NAND 50Ω Line Driver

Product Specification

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	$\overline{Y}$
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
Ceramic DIP	54S140/BCA
Ceramic Flat Pack	54S140/BDA
Ceramic LLCC	54S140/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

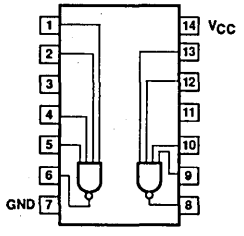
PINS	DESCRIPTION	54S
A - D	Inputs	2SUL
$\overline{Y}$	Output	30SUL

NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

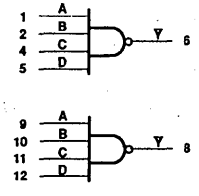
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
	+125°C			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-40	mA
I_{OL}	Low-level output current			60	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = -3mA		2.5	3.4		V
		V_{CC} = Min, V_{IL} = 0.5V, R_O = 50Ω to ground		2.0			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min,				0.5	V
		I_O = Max	+125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				100	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V				-4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-50		-225	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High		10	18	mA
			I_{CCL} Outputs Low		25	44	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

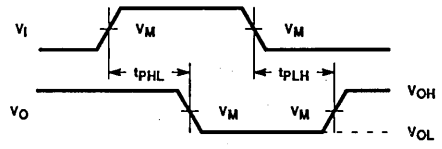
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		6.5 6.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[4]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		8.5 8.5	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed 100 milliseconds.
4. These parameters are guaranteed, but not tested.

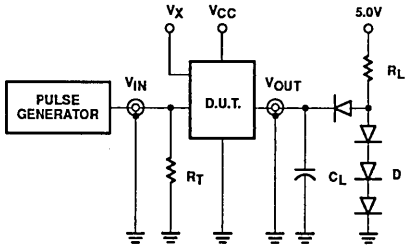
AC WAVEFORM



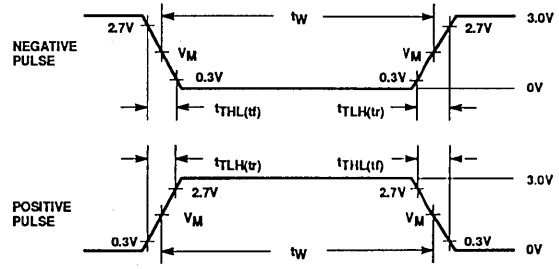
Waveform 1. Waveform for Inverting Outputs

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	93Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54S151
Multiplexer

8-Input Multiplexer

Product Specification

FEATURES
- **Multifunction capability**
- **Complementary outputs**
- **See '251 for 3-State version**

DESCRIPTION
The 54S151 is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs (S_0, S_1, S_2). True (Y) and Complement ($\overline{Y}$) outputs are both provided. The Enable input ($\overline{E}$) is active Low. When $\overline{E}$ is High, the $\overline{Y}$ output is High and the Y output is Low, regardless of all other inputs. The logic function provide at the output is:

$$Y = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

In one package the 54S151 provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and ita negation with correct manipulation.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54S151/BEA
16-Pin Ceramic FlatPack	54S151/BFA
20-Pin Ceramic LLCC	54S151/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

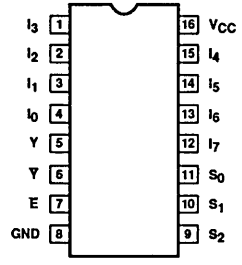
PINS	DESCRIPTION	54S
All	Inputs	1SUL
All	Outputs	10SUL

NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

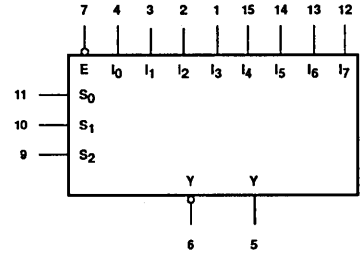
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



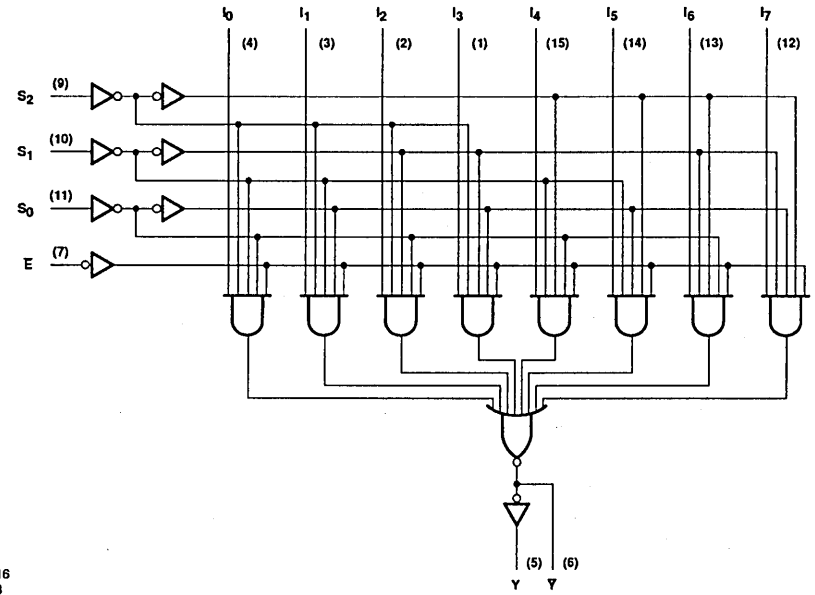
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin number

For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
	+125°C			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1000	µA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,			0.5	V
		I_{OL} = Max, +125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			50	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V			-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-40		-110	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max		45	70	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to Y output	Waveform 2		18 18	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to $\overline{Y}$ output	Waveform 1		15 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to Y output	Waveform 1		16.5 18	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Y}$ output	Waveform 2		13 12	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Y output	Waveform 2		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Y}$ output	Waveform 1		7.0 7.0	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -25°C, V_{CC} = 5.0V[5]

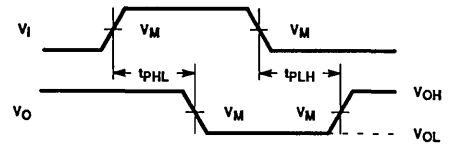
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to Y output	Waveform 2		20.5 20.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to $\overline{Y}$ output	Waveform 1		17.5 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to Y output	Waveform 1		19.0 20.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Y}$ output	Waveform 2		15.5 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Y output	Waveform 2		14.5 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Y}$ output	Waveform 1		9.5 9.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

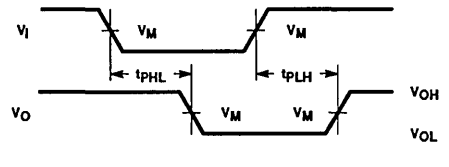
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to Y output	Waveform 2		27 27	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to $\overline{Y}$ output	Waveform 1		23 21	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to Y output	Waveform 1		25 27	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Y}$ output	Waveform 2		20 19	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Y output	Waveform 2		19 19	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Y}$ output	Waveform 1		12 12	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs ≥ 4.0 and all inputs open.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



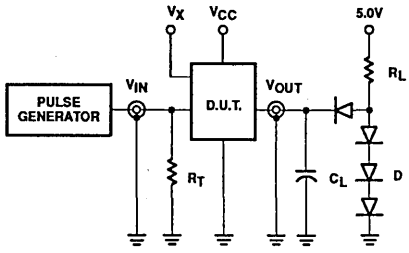
Waveform 1. Waveform for Inverting Outputs



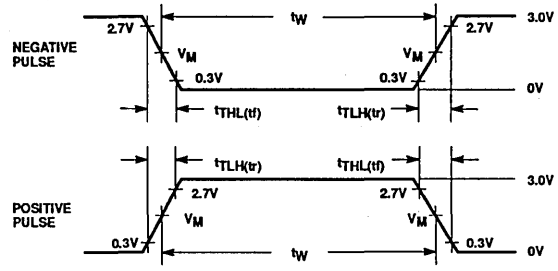
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54S153
Multiplexer

Dual 4-Line to 1-Line Multiplexer

Product Specification

FEATURES
- **Non-Inverting outputs**
- **Separate enable for each section**
- **Common select inputs**
- **See '253 for 3-State version**

DESCRIPTION
The 54S153 is a dual 4-input multiplexer that can select 2 bits of data from up to eight (8) sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active Low Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced Low when the corresponding Enables ($\overline{E}_a$, $\overline{E}_b$) are High.

$$Y_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_2)$$

$$Y_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_2)$$

The 54S153 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

ORDERING INFORMATION

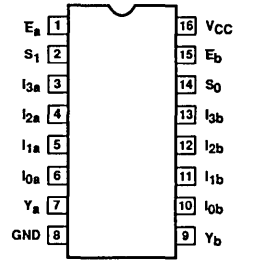
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54S153/BEA
16-Pin Ceramic FlatPack	54S153/BFA
16-Pin Ceramic LLCC	54S153/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S
All	Inputs	1SUL
All	Outputs	10SUL

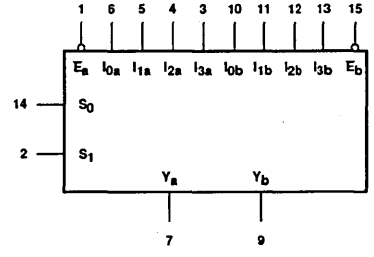
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

PIN CONFIGURATION



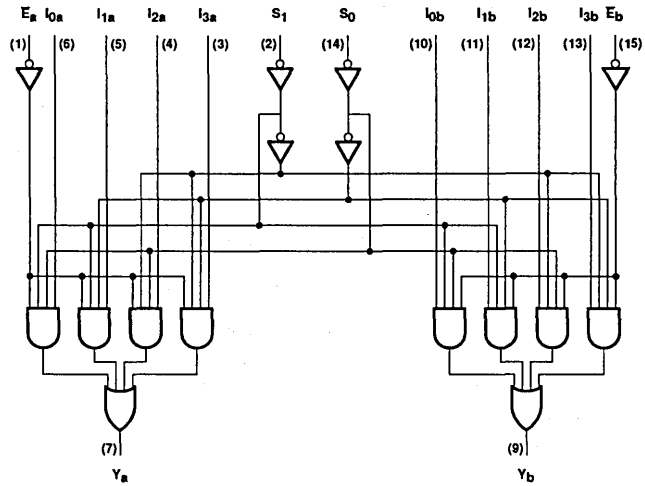
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

For LLCC Pin Assignment, See JEDEC Standard No. 2

FUNCTION TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				+0.8	V
		+125°C			+0.7	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-1000	µA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,				0.5	V
		I_{OL} = Max	+125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V				-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-40		-110	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			45	70	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 2		18 18	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1		15 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2		9 9	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

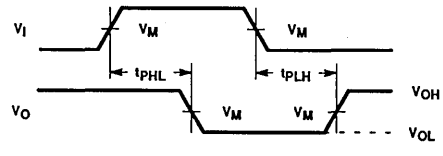
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 2		20.5 20.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1		17.5 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2		11.5 11.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

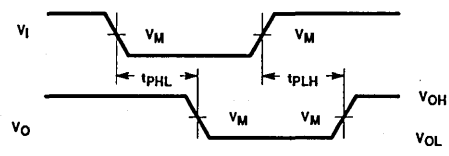
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 2		27 27	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1		23 21	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2		15 15	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



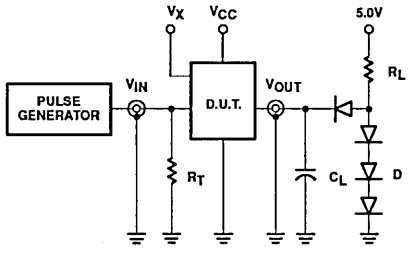
Waveform 1. Waveform for Inverting Outputs



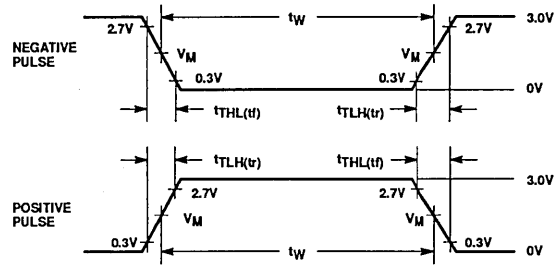
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54LS154
Decoder/Demultiplexer

1-of-16 Decoder/Demultiplexer

Product Specification

Military Logic Products

FEATURES
- **16-line demultiplexing capability**
- **Mutually exclusive outputs**
- **2-input enable gate for strobing or expansion**

DESCRIPTION
The 54LS154 decoder accepts four active High binary address inputs and provides 16 mutually exclusive active Low outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The enable gate has two AND'ed inputs which must be Low to enable the outputs.

The 54LS154 can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is Low, the addressed output will follow the state of the applied data.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54LS154/BJA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

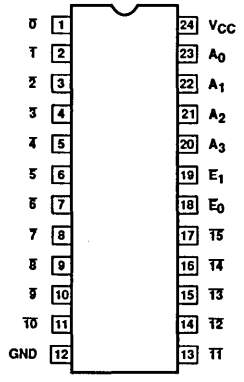
PINS	DESCRIPTION	54LS
All	Inputs	1LSUL
All	Outputs	10LSUL

NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

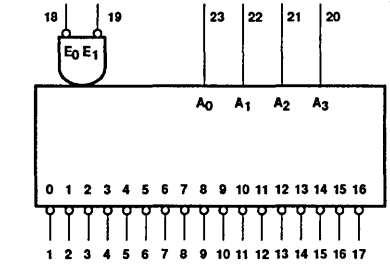
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION

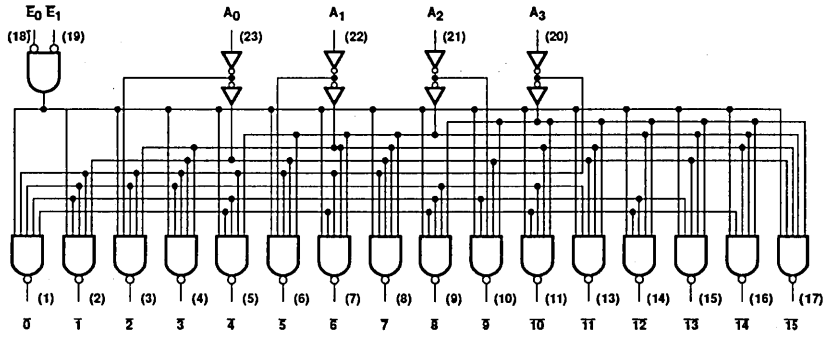


LOGIC SYMBOL



Decoder/Demultiplexer 54LS154

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

FUNCTION TABLE

INPUTS						OUTPUT														
E_0	E_1	A_3	A_2	A_1	A_0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-15		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max		9	14	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1		36 33	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2		30 27	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1		41 38	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2		35 32	ns ns

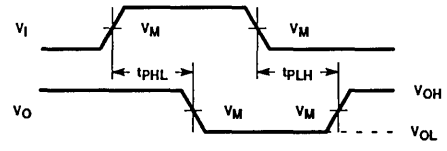
AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1		53 49	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2		46 42	ns ns

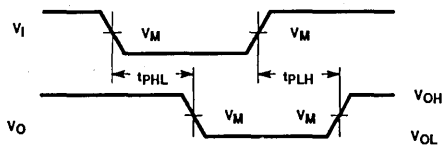
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



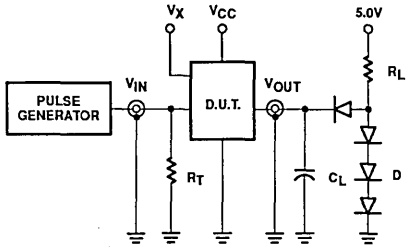
Waveform 1. Waveform for Inverting Outputs



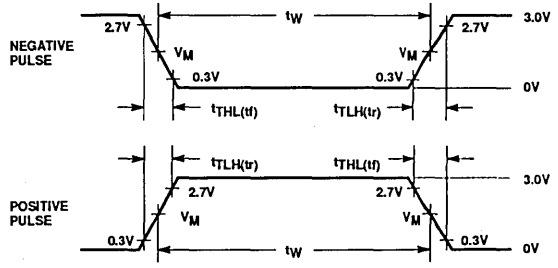
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.3V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54S157, 54S158
Data Selectors/Multiplexers

54S157 Quad 2-Input Data Selector/Multiplexer (Non-Inverted)
54S158 Quad 2-Input Data Selector/Multiplexer (Inverted)

Product Specification

Military Logic Products

DESCRIPTION

The 54S157 is a quad 2-input multiplexer which selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active Low. When $\overline{E}$ is High, all of the outputs (Y) are forced Low regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the 54S157. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$Y_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$Y_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Y_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$Y_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

The 54S158 is similar but has inverting outputs:

$$\overline{Y}_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$\overline{Y}_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Y}_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$\overline{Y}_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

ORDERING INFORMATION

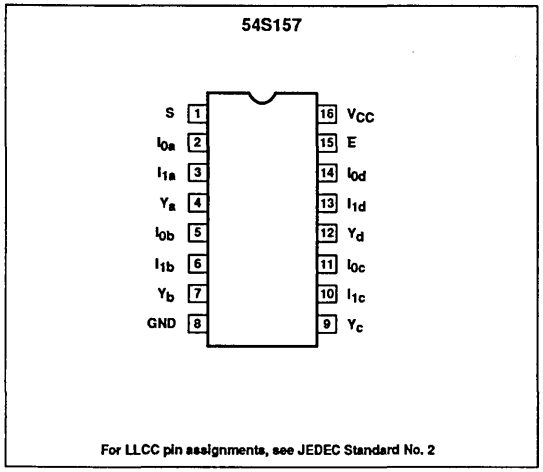
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54S157/BEA, 54S158/BEA
16-Pin Ceramic FlatPack	54S157/BFA, 54S158/BFA
20-Pin Ceramic LLCC	54S157/B2A, 54S158/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S
S, $\overline{E}$	Inputs	2SUL
Data	Inputs	1SUL
All	Outputs	10SUL

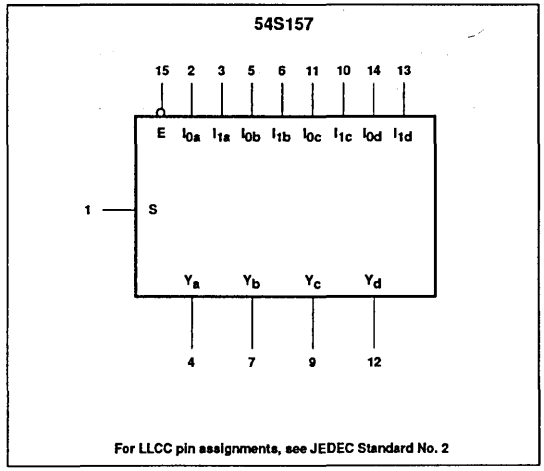
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

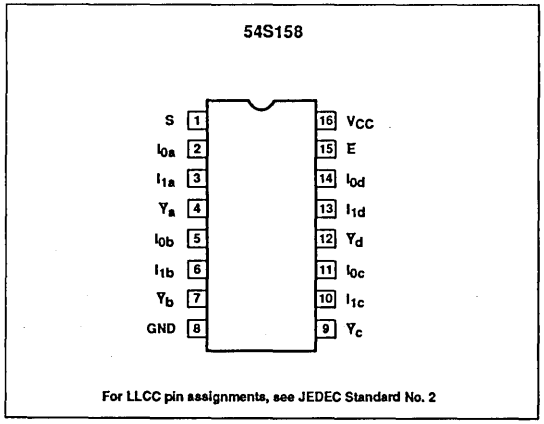
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

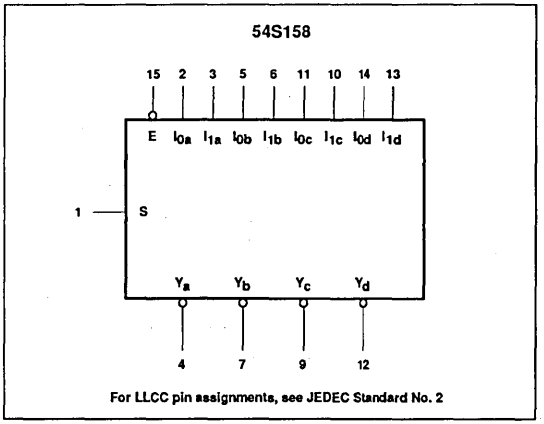
Data Selectors/Multiplexers | 54S157, 54S158

PIN CONFIGURATION



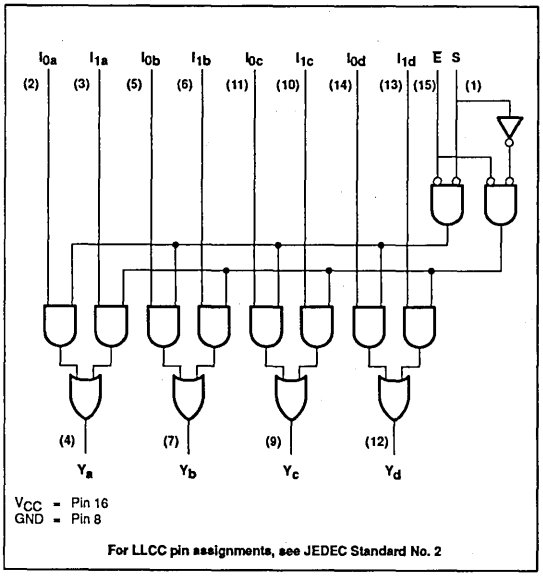
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



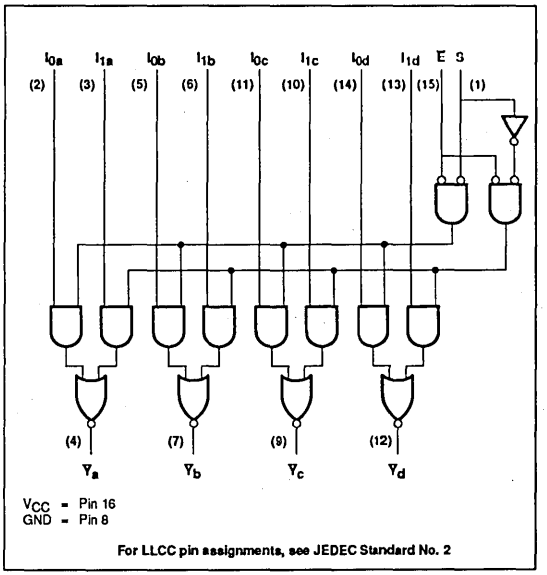
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM 54F157



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM, 54F158



For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE, 54F157

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE, 54F158

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				+0.8	V
		+125°C			+0.7	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-1000	µA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min,				0.5	V
		V_{IL} = Max	+125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	S, $\overline{E}$ inputs			100	µA
			Data inputs			50	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V	S, $\overline{E}$ inputs			-4	mA
			Data inputs			-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-40		-110	mA
I_{CC}	Supply current[4,5] (total)	V_{CC} = Max	54S157 All inputs ≥ 4.0V		50	78	mA
			54S158 All inputs ≥ 4.0V		39	61	mA
			54S158 I_{0a}, I_{0b}, I_{0c}, I_{0d} at ≥ 4.0V – other inputs at 0V		41	81	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 15pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2, 54S157		7.5 6.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1, 54S157		12.5 12	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 2, 54S157		15 15	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 3, 54S158		6.0 6.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 4, 54S158		11.5 12	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 3, 54S158		12 12	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[6]

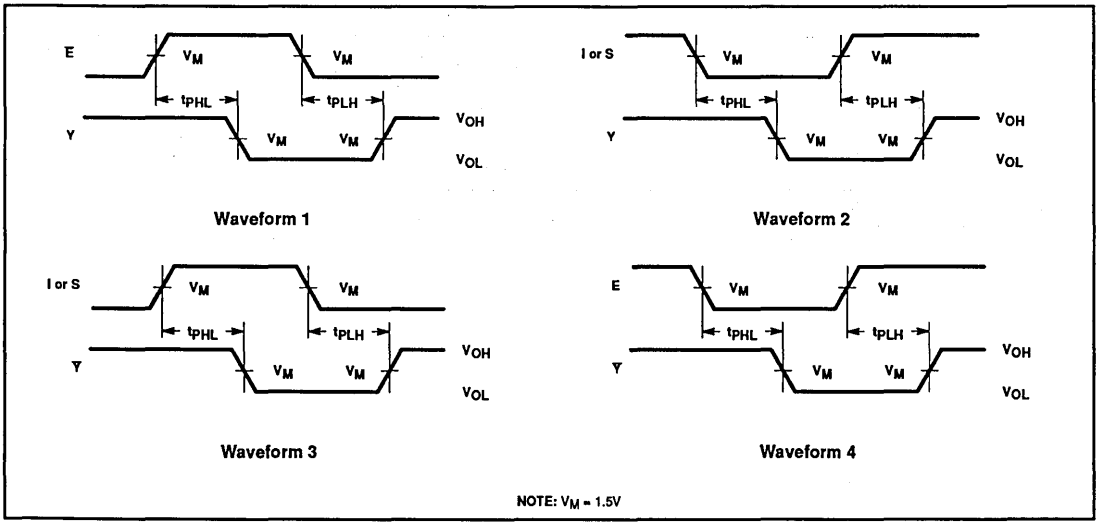
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2, 54S157		10.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1, 54S157		15.0 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 2, 54S157		17.5 17.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 3, 54S158		8.5 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 4, 54S158		14.0 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 3, 54S158		14.5 14.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

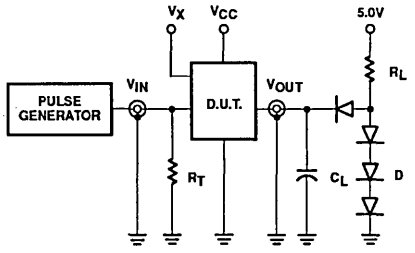
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2, 54S157		13.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1, 54S157		20.0 19.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 2, 54S157		23.0 23.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 3, 54S158		11.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 4, 54S158		18.0 19.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 3, 54S158		19.0 19.0	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with ≥ 4.0V applied to all inputs and all outputs open.
5. I_{CC} is measured with all outputs open.
6. These parameters are guaranteed, but not tested.

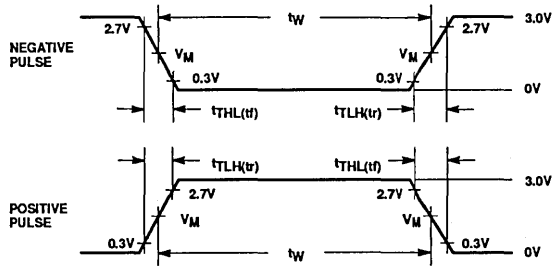
AC WAVEFORMS



TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54161, 54163, 54LS161A, 54LS163A
Counters

4-Bit Binary Counters

Product Specification

FEATURES

- **Synchronous counting and loading**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous reset ('161)**
- **Synchronous reset ('163)**
- **Hysteresis on Clock input (LS only)**

DESCRIPTION

Synchronous and 4-bit (54161, 54LS161A, 54163, 54LS163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the positive-going edge of the clock (providing that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

ORDERING INFORMATION

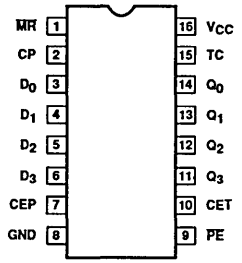
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS161A/BEA 54161/BEA 54LS163A/BEA 54163/BEA
16-Pin Ceramic FlatPack	54LS161A/BFA 54161/BFA 54LS163A/BFA 54163/BFA
20-Pin Ceramic LLCC	54LS161A/B2A 54LS163A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54LS
CP, CET	Inputs	2UL	2LSUL
D, CEP	Inputs	1UL	1LSUL
$\overline{PE}$	Input	1UL	2LSUL
All	Outputs	10UL	10LSUL
$\overline{MR}$	Input ('161)	1UL	1LSUL
$\overline{MR}$	Input ('163)	1UL	2LSUL

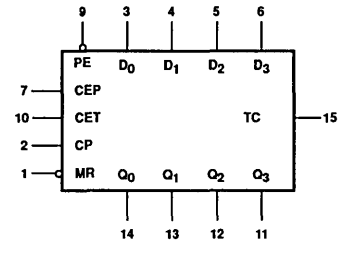
NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

For LLCC pin assignments, see JEDEC Standard No. 2

A Low level at the Master Reset ($\overline{MR}$) input set all four outputs of the flip-flops (Q_0 - Q_3) in 54161, and 54LS161A to Low levels regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 54163, and 54LS163A, the clear function is synchronous. A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels after the next positive-going transition on the Clock (CP) input (providing that the setup and hold requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. The synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure 1).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure 2).

For conventional operation of 54161 and 54163, the following transitions should be avoided.

1. High-to-Low transition on the CEP or CET input if clock is Low.
2. Low-to-High transitions on the Parallel Enable input when CP is Low, if the count enables and $\overline{MR}$ are High at or before the transition.

For 54163 there is an additional transition to be avoided.

3. Low-to-High transition on the $\overline{MR}$ input when clock is Low, if the Enable and $\overline{PE}$ inputs are High at or before the transition.

These restrictions are not applicable to 54LS161A and 54LS163A.

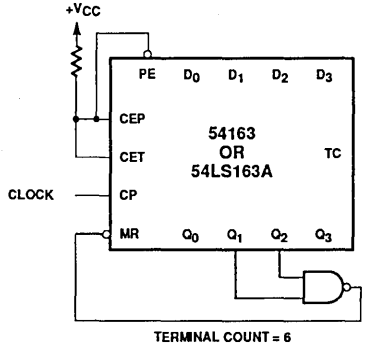
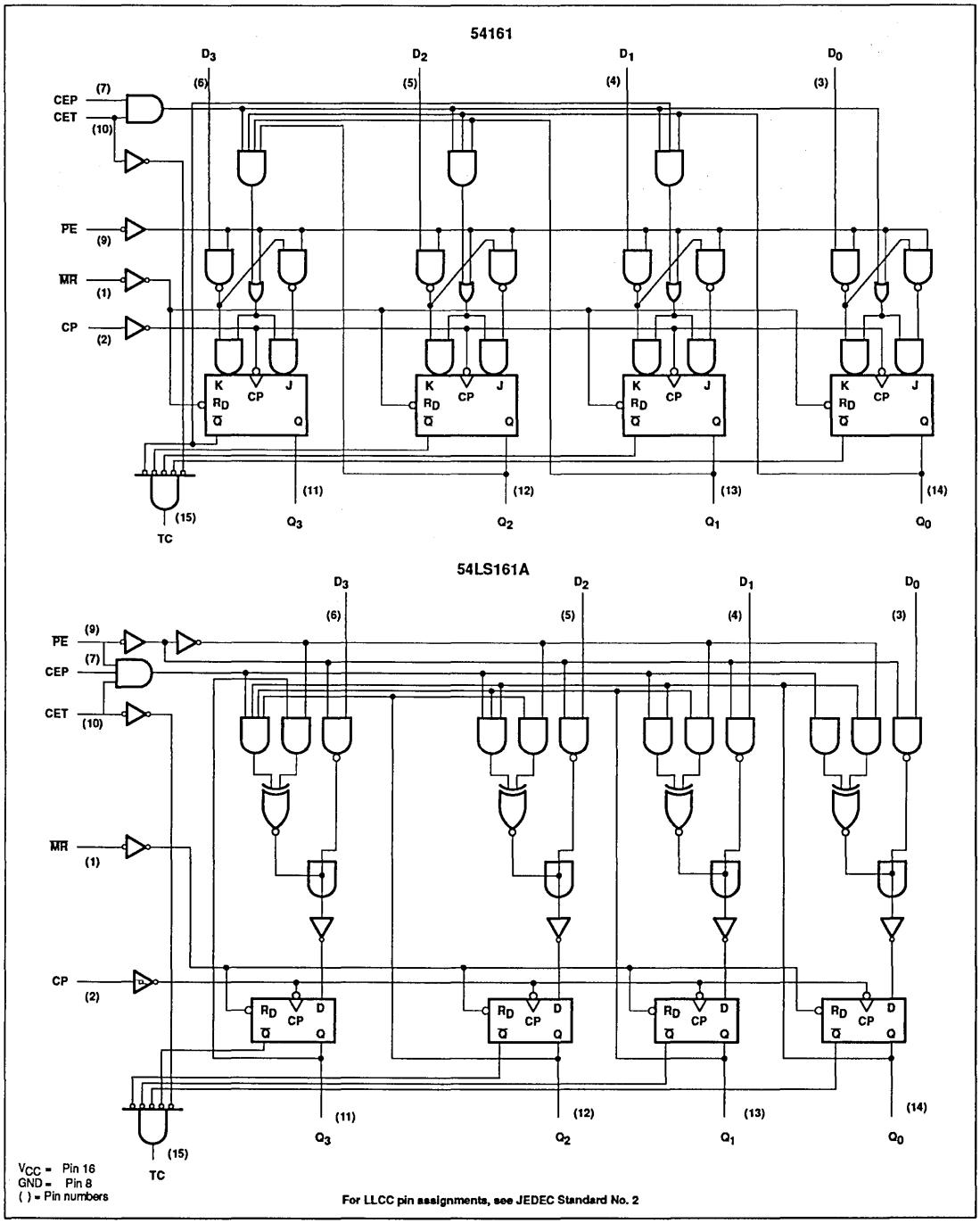
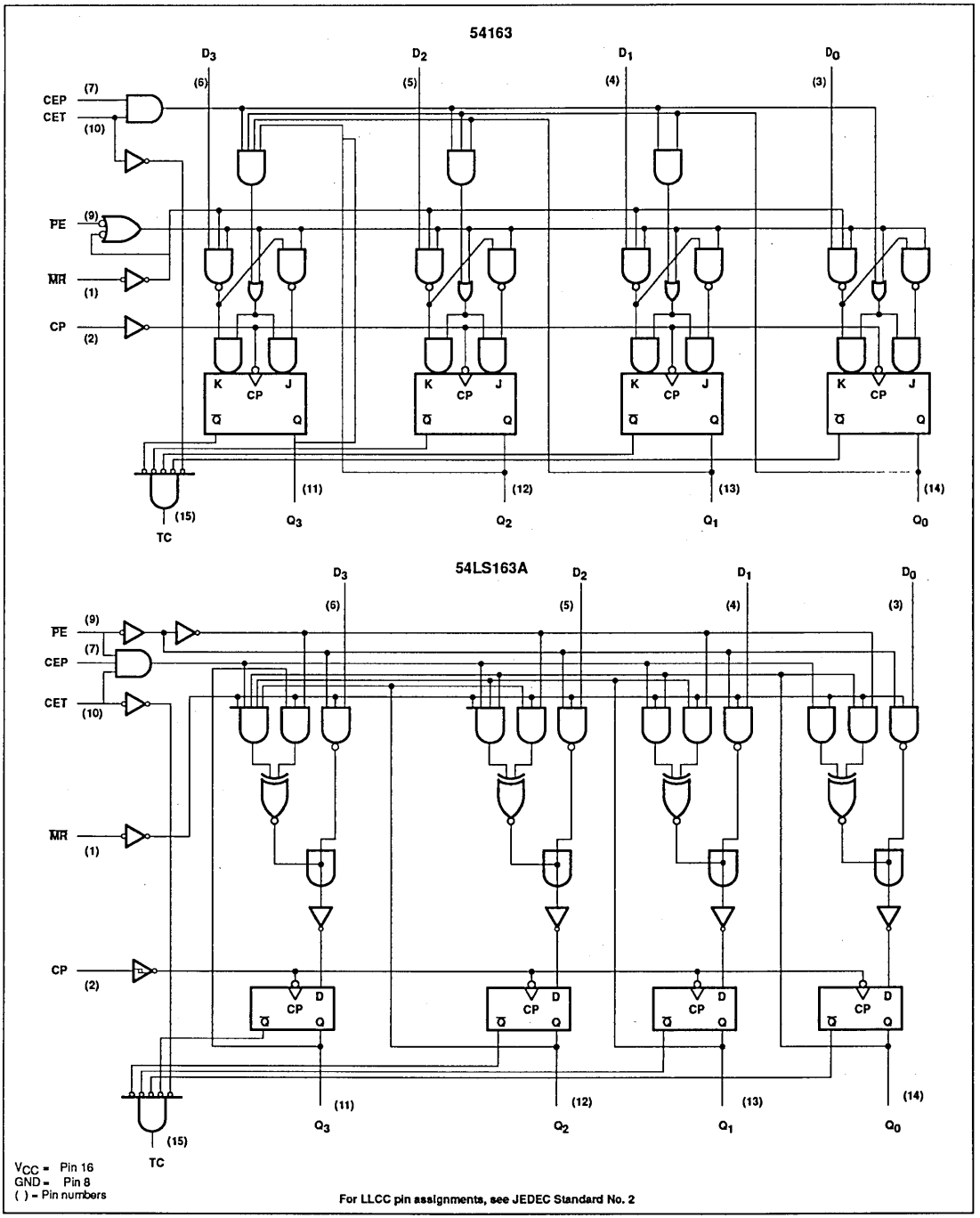


Figure 1

LOGIC DIAGRAMS



LOGIC DIAGRAMS



MODE SELECT — FUNCTION TABLE, '161

OPERATING MODE	INPUTS						OUTPUT	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(a)
Count	H	↑	h	h	h[c]	X	count	(a)
Hold (do nothing)	H	X	l[b]	X	h[c]	X	q_n	(a)
	H	X	X	l[b]	h[c]	X	q_n	L

MODE SELECT — FUNCTION TABLE, '163

OPERATING MODE	INPUTS						OUTPUT	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	l	↑	X	X	X	X	L	L
Parallel load	h[f]	↑	X	X	l	l	L	L
	h[f]	↑	X	X	l	h	H	(d)
Count	h[f]	↑	h	h	h[f]	X	count	(d)
Hold (do nothing)	h[f]	X	l[e]	X	h[f]	X	q_n	(d)
	h[f]	X	X	l[e]	h[f]	X	q_n	L

H = High voltage level steady state
L = Low voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

NOTES:
(a) The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 54161)
(b) The High-to-Low transition of CEP or CET on the 54161 should only occur while CP is High for conventional operation
(c) The Low-to-High transition of $\overline{PE}$ on the 54161 should only occur while CP is High for conventional operation
(d) The TC output is High when CET is High and the counter is at Terminal Count (HHHH for '163)
(e) The High-to-Low transition of CEP or CET on the 54163 should only occur while CP is High for conventional operation
(f) The Low-to-High transition of $\overline{PE}$ or $\overline{MR}$ on the 54163 should only occur while CP is High for conventional operation

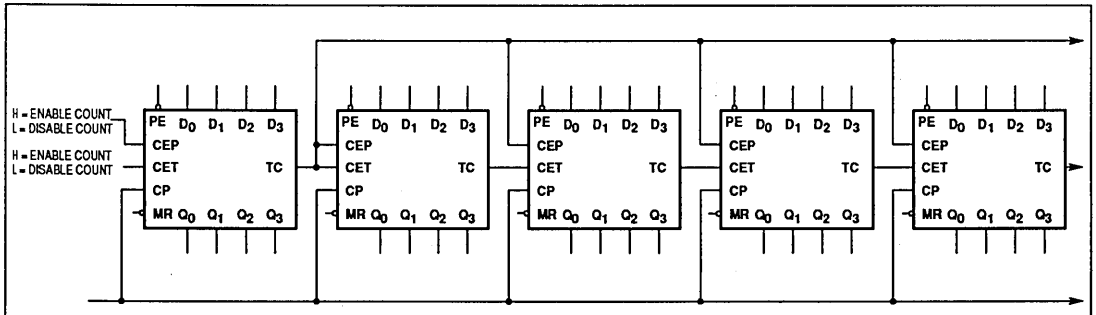


Figure 2. Synchronous Multistage Counting Scheme

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54	54LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54			54LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.8			+0.7	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	High-level output current			-800			-400	µA
I_{OL}	Low-level output current			16			4	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			54161, '163			54LS161A, '163A			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max			2.4	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max				0.2	0.4		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5			-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V				1.0				mA
			V_I = 7.0V	D, CEP						0.1	mA
				PE, CP, CET						0.2	mA
				MR, ('LS161A)						0.1	mA
				MR, ('LS163A)						0.2	mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V	CP, CET			80				µA
				Other inputs			40				µA
			V_I = 2.7V	D, CEP						20	µA
				PE, CP, CET						40	µA
				MR, ('LS161A)						20	µA
				MR, ('LS163A)						40	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V	CP, CET			-3.2				mA
				Other inputs			-1.6				mA
			V_I = 0.4V	D, CEP						-0.4	mA
				PE, CP, CET						-0.8	mA
				MR, ('LS161A)						-0.4	mA
				MR, ('LS163A)						-0.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-20		-57	-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	I_{CCH}	All outputs High		59	85		18	31	mA
			I_{CCL}	All outputs Low		63	91		19	32	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[6]

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			$C_L = 15pF$		$C_L = 15pF$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to terminal count	Waveform 1		35 35		35 35	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = High		20 23		24 27	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = Low		25 29		24 27	ns ns
t_{PLH} t_{PHL}	Propagation delay CET input to TC output	Waveform 2		16 16		16 16	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q outputs ('161)	Waveform 3		38		28	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			Min	Max	Min	Max	
$t_W(L)$	Clock pulse width (Low)	Waveform 1	25		25		ns
t_W	Master Reset pulse width ('161)	Waveform 3	20		20		ns
t_W	Master Reset pulse width ('163)	Waveform 6	20		20		ns
t_s	Setup time, data to clock	Waveform 5	20		20		ns
t_h	Hold time, data to clock[5]	Waveform 5	3		3		ns
t_s	Setup time, CEP or CET to clock	Waveform 4	20		20		ns
t_h	Hold time, CEP or CET to clock	Waveform 4	0		0		ns
t_s	Setup time, $\overline{PE}$ to clock	Waveform 5	25		20		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 5	0		0		ns
t_s	Setup time, $\overline{MR}$ to clock ('163)	Waveform 6	20		20		ns
t_h	Hold time, $\overline{MR}$ to clock ('163)	Waveform 6	0		0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		15		ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			$C_L = 50pF$		$C_L = 50pF$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	20		22		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to terminal count	Waveform 1		39 39		40 40	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = High		24 27		29 32	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = Low		29 33		29 32	ns ns
t_{PLH} t_{PHL}	Propagation delay CET input to TC output	Waveform 2		20 20		19 19	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q outputs ('161)	Waveform 3		42		33	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

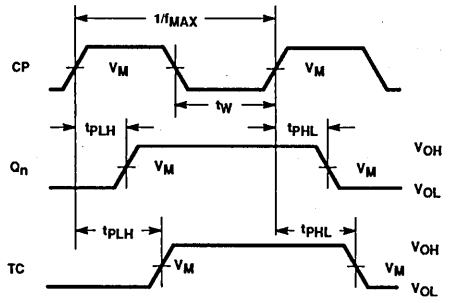
SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		22		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to terminal count	Waveform 1		51 51		52 52	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = High		31 35		38 42	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = Low		38 43		38 42	ns ns
t_{PLH} t_{PHL}	Propagation delay CET input to TC output	Waveform 2		26 26		25 25	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q outputs ('161)	Waveform 3		55		43	ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

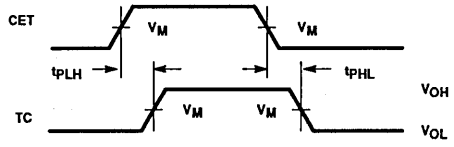
SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			Min	Max	Min	Max	
$t_W(L)$	Clock pulse width (Low)	Waveform 1	25		25		ns
t_W	Master Reset pulse width ('161)	Waveform 3	20		25		ns
t_W	Master Reset pulse width ('163)	Waveform 6	20		25		ns
t_s	Setup time, data to clock	Waveform 5	20		25		ns
t_h	Hold time, data to clock[5]	Waveform 5	5		5		ns
t_s	Setup time, CEP or CET to clock	Waveform 4	20		20		ns
t_h	Hold time, CEP or CET to clock	Waveform 4	0		0		ns
t_s	Setup time, $\overline{PE}$ to clock	Waveform 5	25		20		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 5	0		0		ns
t_s	Setup time, $\overline{MR}$ to clock ('163)	Waveform 6	20		20		ns
t_h	Hold time, $\overline{MR}$ to clock ('163)	Waveform 6	0		0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		15		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CCH} is measured with $\overline{PE}$ input High, again with $\overline{PE}$ input Low, all other inputs High and output open. I_{CCL} is measured with Clock input High, again with Clock input Low, all other inputs low and outputs open.
5. For 15ns rise time only, Hold time must be increased by 0.3ns for each nanosecond decrease in rise time.
6. These parameters are guaranteed, but not tested.

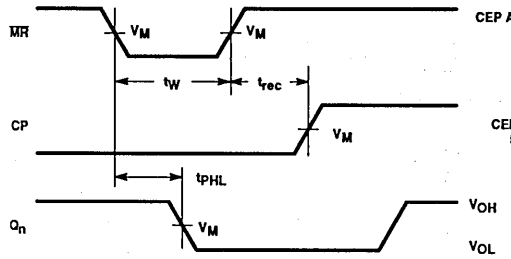
AC WAVEFORMS



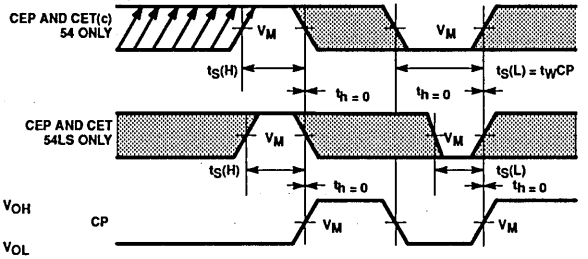
Waveform 1. Clock to Output Delays, Maximum Frequency, and Clock Pulse Width



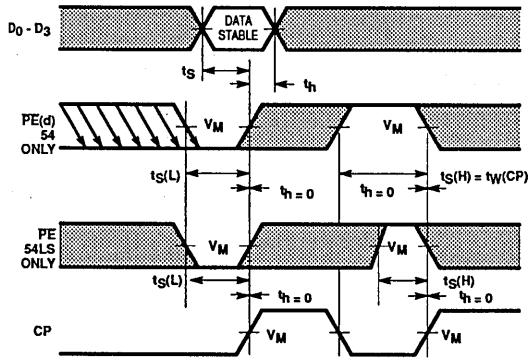
Waveform 2. Propagation Delays CET Input to TC Output



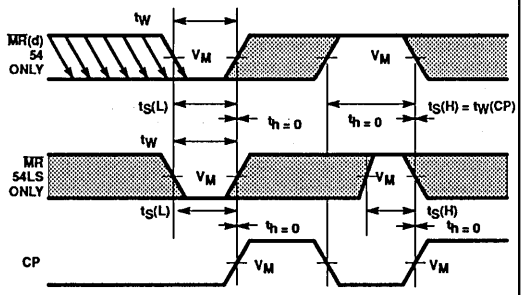
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time ('161)



Waveform 4. CEP and CET Setup and Hold Times



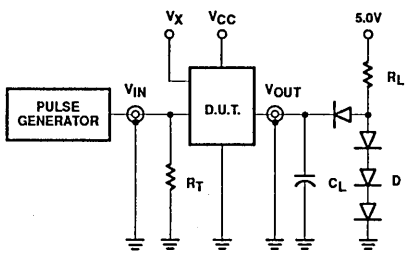
Waveform 5. Parallel Data and Parallel Enable Setup and Hold Times



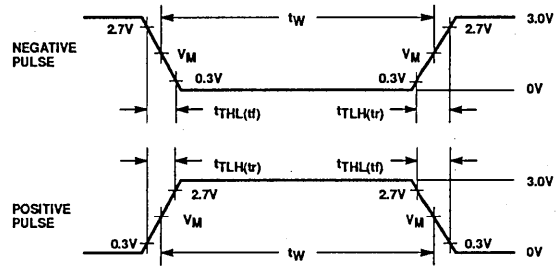
Waveform 6. Synchronous Reset Setup, Pulse Width and Hold Times ('163)

NOTE: V_M = 1.5V for 54; V_M = 1.3 for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54164, 54LS164
Shift Registers

8-Bit Serial-In Parallel-Out Shift Registers

Product Specification

Military Logic Products

FEATURES

- **Gated serial data inputs**
- **Typical shift frequency of 36MHz**
- **Asynchronous Master Reset**
- **Fully buffered clock and data inputs**

DESCRIPTION

The 54164 and 54LS164 are 8-bit edge-triggered shift registers with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an Active-High enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one setup time before the rising clock edge. A Low-level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

ORDERING INFORMATION

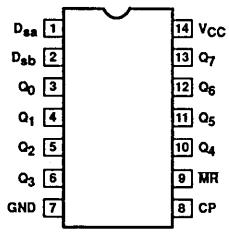
DESCRIPTION	ORDER CODE
Ceramic DIP	54LS164/BCA, 54164/BCA
Ceramic Flat Pack	54LS164/BDA
Ceramic LLCC	54LS164/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54LS
All	Inputs	1UL	1LSUL
All	Outputs	5UL	10LSUL

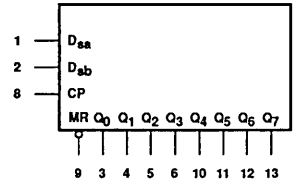
NOTE: Where a 54 Unit Load (UL) is understood to be 40µA I_{IH} and -1.6mA I_{IL}, and a 54LS Unit Load (LSUL) is 20µA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

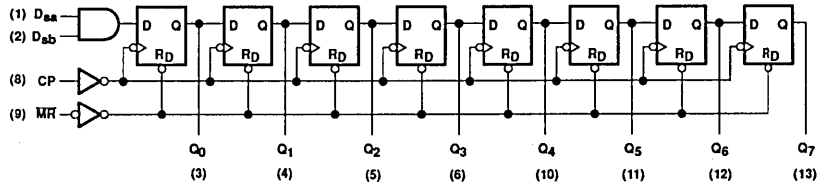


VCC = Pin 14
GND = Pin 7

For LLCC pin assignments, see JEDEC Standard No. 2

Shift Registers | 54164, 54LS164

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

For LLCC pin assignments, see JEDEC Standard No. 2

MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1	—	Q_7
Reset	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q_0	—	q_6
	H	↑	l	h	L	q_0	—	q_6
	H	↑	h	l	L	q_0	—	q_6
	H	↑	h	h	H	q_0	—	q_6

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High Clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High Clock transition
q = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the Low-to-High Clock transition
X = Don't care
↑ = Low-to-High Clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54164	54LS164	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

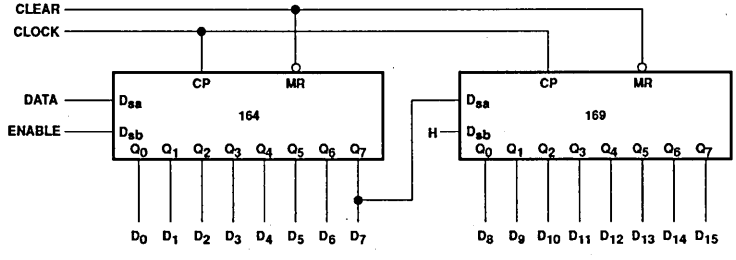
RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54164			54LS164			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.8			+0.7	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	High-level output current			-400			-400	µA
I_{OL}	Low-level output current			8			4	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54164			54LS164			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.2	0.4		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V			1.0				mA
			V_I = 7.0V						0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V			40				µA
			V_I = 2.7V						20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V				-1.6			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-10		-27.5	-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			37	54		16	27	mA

APPLICATION DIAGRAM



The '164 can be cascaded to form synchronous shift registers of longer length. Here, two devices are combined to form a 16-bit shift register.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54164		54LS164		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 32		27 32	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		36		36	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54164		54LS164		UNIT
			Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	20		20		ns
t_W	$\overline{MR}$ pulse width	Waveform 2	20		20		ns
t_S	Setup time data to clock	Waveform 3	15		15		ns
t_H	Hold time data to clock	Waveform 3	5.0		5.0		ns
t_{REC}	$\overline{MR}$ clock recovery time	Waveform 2	30		30		ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	54164		54LS164		UNIT
			$C_L = 50pF$		$C_L = 50pF$		
			Min	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	22		22		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		34 41		31 36	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		46		40	ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54164		54LS164		UNIT
			$C_L = 50pF$		$C_L = 50pF$		
			Min	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	18		20		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		31 48		40 47	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		55		52	ns

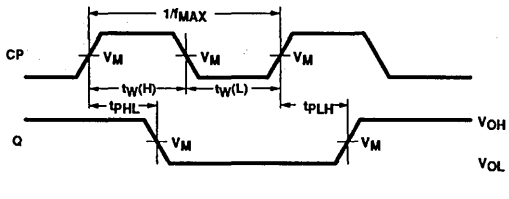
AC SETUP REQUIREMENTS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54164		54LS164		UNIT
			Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	30		20		ns
t_W	$\overline{MR}$ pulse width	Waveform 2	50		25		ns
t_S	Setup time data to clock	Waveform 3	15		20		ns
t_H	Hold time data to clock	Waveform 3	10		10		ns
t_{REC}	$\overline{MR}$ clock recovery time	Waveform 2	30		30		ns

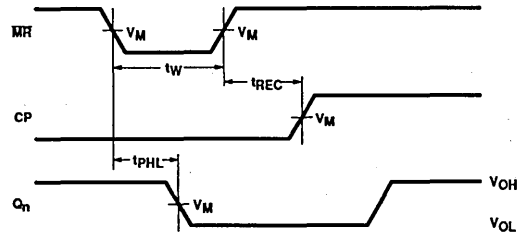
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with the Serial inputs grounded, the Clock input at 2.4V, and a momentary ground, then ≥4.0V applied to Master Reset, and all outputs open.
5. These parameters are guaranteed, but not tested.

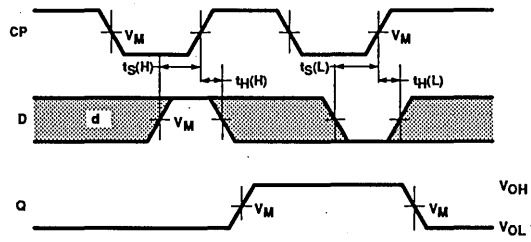
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



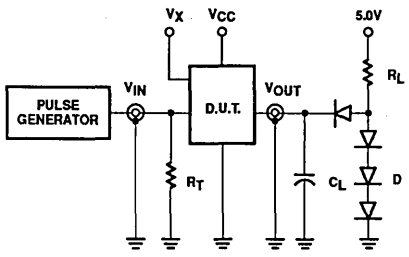
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



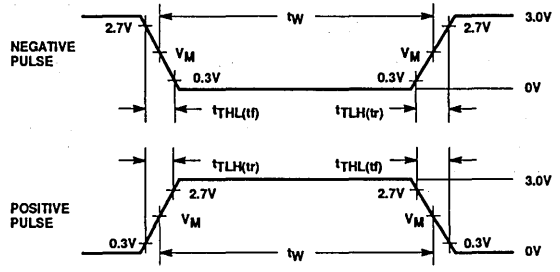
Waveform 3. Data Setup and Hold Times

NOTE: For all waveforms, V_M = 1.5V for 54; V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS173
Flip-Flop

Quad D-Type Flip-Flop with 3-State Outputs

Product Specification

FEATURES

- **Edge-triggered D-type register**
- **Gated input enable for hold "do nothing" mode**
- **3-State output buffers**
- **Gated output enable control**
- **Pin compatible with the 8T10 and DM8551**

DESCRIPTION

The 54LS173 is a 4-bit parallel load register with clock enable control, 3-State buffered outputs and master reset. When the two Clock Enable ($\overline{E}_1$ and $\overline{E}_2$) inputs are Low, the data on the D inputs is loaded into the register synchronously with the Low-to-High Clock (CP) transition. When one or both $\overline{E}$ inputs are High one setup time before the Low-to-High clock transition, the register will retain the previous data. Data inputs and Clock Enable inputs are fully edge triggered and must be stable only one setup time before the Low-to-High clock transition.

The Master Reset (MR) is an active High asynchronous input. When the MR is High, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-State output buffers are controlled by a 2-input NOR gate. When both Output Enable ($\overline{OE}_1$ and $\overline{OE}_2$) inputs are Low, the data in the register is presented at the Q outputs. When one or both $\overline{OE}$ inputs is High, the outputs are forced to a High impedance "off" state. The 3-State output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

ORDERING INFORMATION

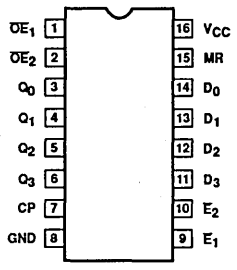
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS173/BEA
16-Pin Ceramic FlatPack	54LS173/BFA
16-Pin Ceramic LLCC	54LS173/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
All	Inputs	1LSUL
All	Outputs	30LSUL

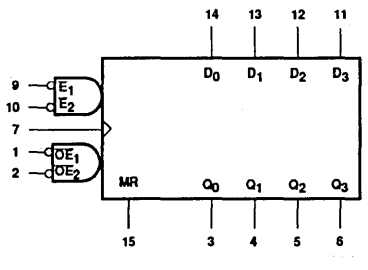
NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



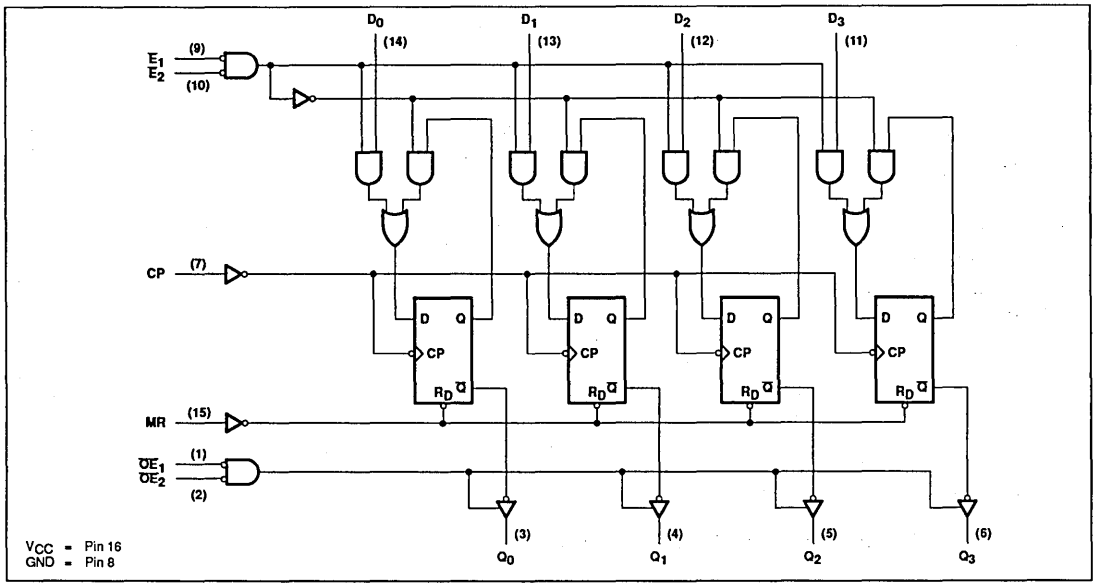
For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Q_n (Register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (no change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS
	Q_n (Register)	$\overline{OE}_1$	$\overline{OE}_2$	Q_0, Q_1, Q_2, Q_3
Read	L	L	L	L
	H	L	L	H
Disabled	X	H	X	(Z)
	X	X	H	(Z)

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
q_n = Lower case letters indicate the state of the referenced input (or output) on setup time prior to the Low-to-High clock transition
X = Don't care
(Z) = High impedance "off" state
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.6	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.30	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-1.5	V
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V			20	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.4V			-20	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-30		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max		20	30	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		25 30	ns ns
t_{PHL}	Propagation delay, MR to output	Waveform 4		35	ns
t_{PZH}	Output enable to High level	Waveform 2		23	ns
t_{PZL}	Output enable to Low level	Waveform 3		27	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 5pF[5]		17	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 5pF[5]		17	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 50pF		33	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 50pF		19	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W(CP)	Clock pulse width	Waveform 1	20		ns
t_W(MR)	MR pulse width	Waveform 4	20		ns
t_s(D)	Setup time, data to clock	Waveform 5	17		ns
t_h(D)	Hold time, data to clock	Waveform 5	0		ns
t_s(E)	Setup time, enable to clock	Waveform 5	35		ns
t_h(E)	Hold time, enable to clock	Waveform 5	0		ns
t_{rec}(MR)	Recovery time, Master Reset to clock	Waveform 4	17		ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

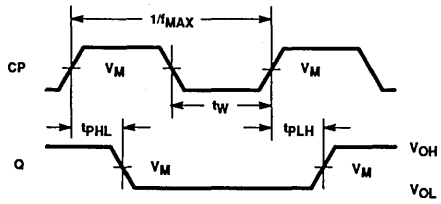
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	20		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		32 39	ns ns
t_{PHL}	Propagation delay, MR to output	Waveform 4		45	ns
t_{PZH}	Output enable to High level	Waveform 2		30	ns
t_{PZL}	Output enable to Low level	Waveform 3		35	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 5pF[5]		22	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 5pF[5]		22	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 50pF		43	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 50pF		24	ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C[6]

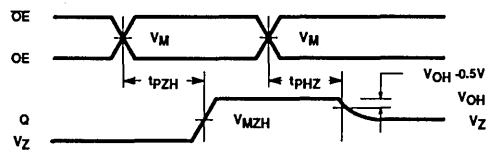
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W(CP)	Clock pulse width	Waveform 1	22		ns
t_W(MR)	MR pulse width	Waveform 4	20		ns
t_s(D)	Setup time, data to clock	Waveform 5	24		ns
t_h(D)	Hold time, data to clock	Waveform 5	5		ns
t_s(E)	Setup time, enable to clock	Waveform 5	35		ns
t_h(E)	Hold time, enable to clock	Waveform 5	0		ns
t_{rec}(MR)	Recovery time, Master Reset to clock	Waveform 4	17		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with MR grounded following momentary connection $\geq$ 4.0V, $\overline{OE}_2$, E_1, E_2 and all Data inputs grounded, CP and $\overline{OE}_1 \geq$ 4.0V, and all outputs open.
5. Guaranteed by the 50pF limit, but not tested.
6. These parameters are guaranteed, but not tested.

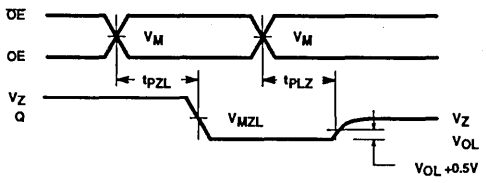
AC WAVEFORMS



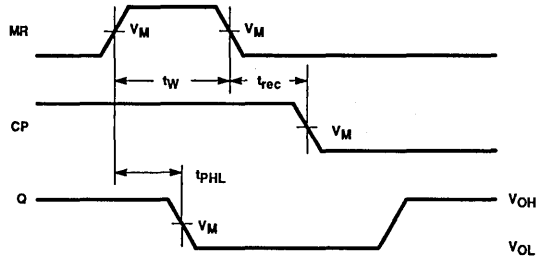
Waveform 1. Clock to Output Delays and Clock Pulse Width



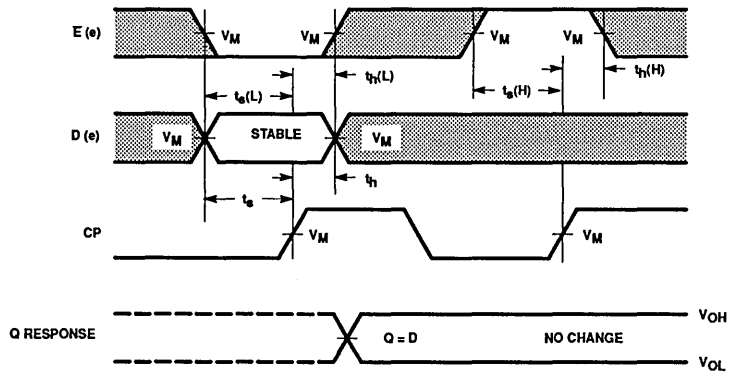
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level



Waveform 4. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

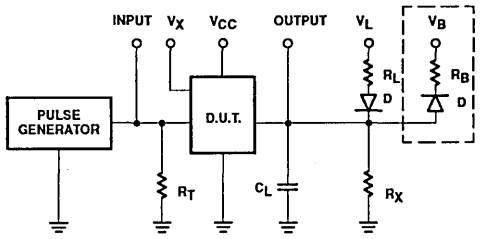


Waveform 5. Setup (t_S) and Hold (t_h) Times for Data (D) and Enable (E) Inputs

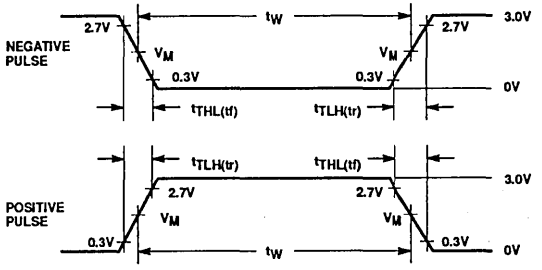
NOTE: The shaded areas indicate when the input is permitted to change for predictable output performances.

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54174, 54LS174, 54S174
Flip-Flops

Hex D Flip-Flops

Product Specification

FEATURES
- **Six edge-triggered D-type flip-flops**
- **Three speed-power ranges available**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**

DESCRIPTION
The 54174, 54LS174 and 54S174 have six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

ORDERING INFORMATION

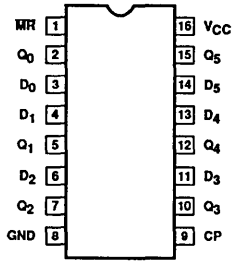
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS174/BEA, 54S174/BEA, 54174/BEA
16-Pin Ceramic FlatPack	54LS174/BFA, 54S174/BFA, 54174/BFA
16-Pin Ceramic LLCC	54LS174/B2A, 54S174/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54S	54LS
All	Inputs	1UL	1SUL	1LSUL
Q_0 - Q_5	Outputs	10UL	10SUL	10LSUL

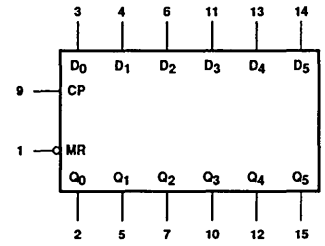
NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}, a 54S Unit Load (SUL) is 50 μA I_{IH} and -2.0mA I_{IL}, and 54LS Unit Load (LSUL) is 20 μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

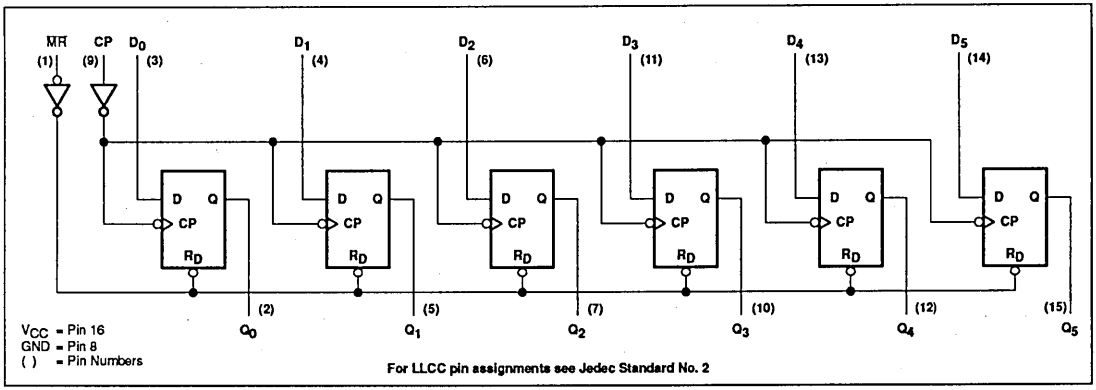
LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150			°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54			54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			2.0			V
V_{IL}	Low-level input voltage			+0.8			+0.7			+0.8	V
I_{IK}	Input clamp current			-12			-18			-18	mA
I_{OH}	High-level output current			-800			-400			-1000	µA
I_{OL}	Low-level output current			16			4			20	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54174			54LS174			54S174			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4		0.25	0.4			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.5			-1.2	V
I_{IH2}	Input current at max-	V_{CC} = Max	V_I = 5.5V			1.0						1.0	mA
	imum input voltage		V_I = 7.0V						0.1				mA
I_{IH1}	High-level	V_{CC} = Max	V_I = 2.4V			40							µA
	input current		V_I = 2.7V						20			50	µA
I_{IL}	Low-level	V_{CC} = Max	V_I = 0.4V			-1.6			-0.4				mA
	input current		V_I = 0.5V									-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-57	-20		-100	-40		-110	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			45	65		16	26		90	144	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54[5]		54LS[5]		54S		UNIT
			C_L = 15pF		C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		30 35		30 30		13 17	ns ns
t_{PHL}	Propagation $\overline{MR}$ delay to output	Waveform 3		35		35		22	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		54S		UNIT
			Min	Max	Min	Max	Min	Max	
t_w(L)	Clock pulse width (Low)	Waveform 1	20		20		7.0		ns
t_w	Master Reset pulse width	Waveform 3	20		20		10		ns
t_s	Setup time, data to CP	Waveform 2	20		20		5.0		ns
t_h	Hold time, data to CP	Waveform 2	5		5		3.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		25		5.0		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		54S[5]		UNIT
			C_L = 50pF		C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		34 39		35 35		14.0 19.0	ns ns
t_{PHL}	Propagation $\overline{MR}$ delay to output	Waveform 3		39		40		24.0	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		55		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		44 51		46 46		17 23	ns ns
t_{PHL}	Propagation $\overline{MR}$ delay to output	Waveform 3		51		52		29	ns

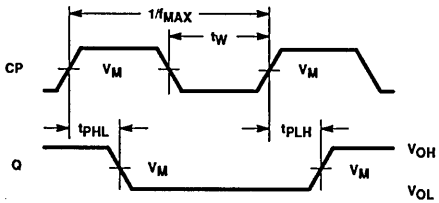
AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		54S		UNIT
			Min	Max	Min	Max	Min	Max	
t_w(L)	Clock pulse width (Low)	Waveform 1	20		30		10		ns
t_w	Master Reset pulse width	Waveform 3	30		35		10		ns
t_s	Setup time, data to CP	Waveform 2	25		20		7		ns
t_h	Hold time, data to CP	Waveform 2	5		5		5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	30		25		7		ns

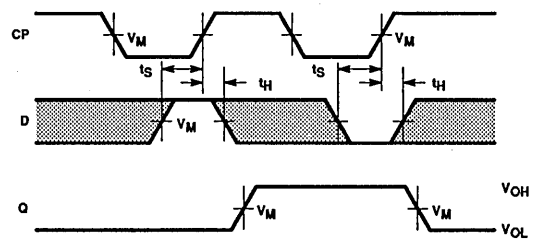
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after a momentary ground, then ≥ 4.0V is applied to Clock, with ≥ 4.0V applied to all Data and $\overline{MR}$ inputs and all outputs open.
5. These parameters are guaranteed, but not tested.

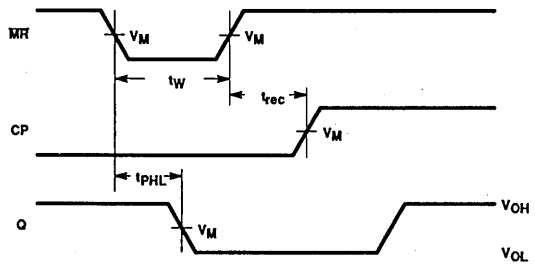
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



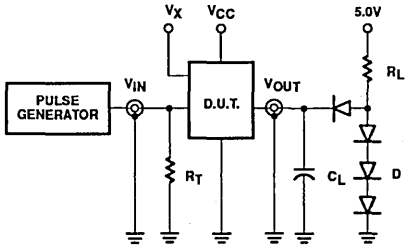
Waveform 2. Data Setup and Hold Times



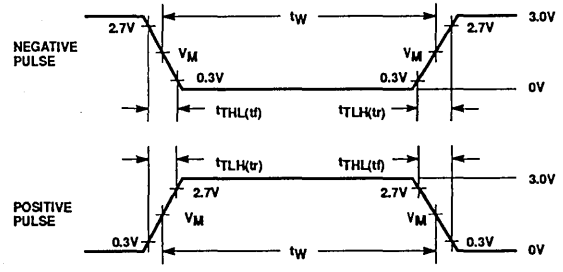
Waveform 3. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

NOTE: For all waveforms V_M = 1.5V for 54 and 54S; V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

54175, 54LS175
Flip-Flops

Quad D Flip-Flops

Product Specification

FEATURES

- **Four edge-triggered D flip-flops**
- **Three speed-power ranges available**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**

DESCRIPTION

The 54175 and 54LS175 are quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

ORDERING INFORMATION

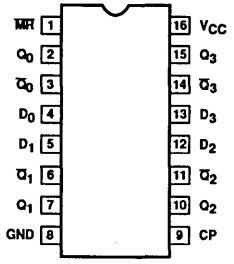
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54175/BEA 54LS175/BEA
16-Pin Ceramic FlatPack	54175/BFA 54LS175/BFA
16-Pin Ceramic LLCC	54LS175/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54LS
All	Inputs	1UL	1LSUL
All	Outputs	10UL	10LSUL

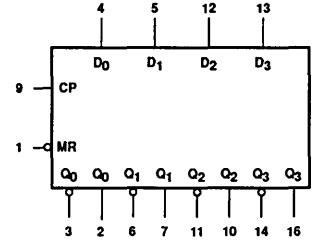
NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

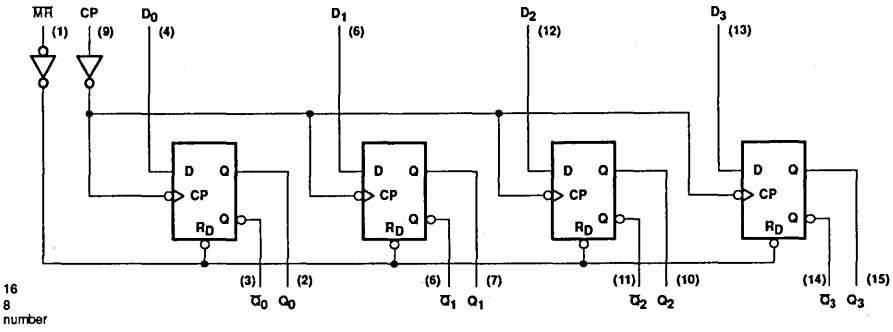
LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC pinout see JEDEC Standard No. 2

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High Clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High Clock transition
X = Don't Care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54	54LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	-30 to +1.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54			54LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.8			+0.7	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	High-level output current			-800			-400	µA
I_{OL}	Low-level output current			16			4	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54175			54LS175			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.2	0.4		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V			1.0				mA
			V_I = 7.0V						0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V			40				µA
			V_I = 2.7V						20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V				-1.6			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-57	-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			30	45		11	18	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54[5]		54LS		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to outputs	Waveform 1		30 35		25 25	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to outputs	Waveform 3		25 35		30 30	ns ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			Min	Max	Min	Max	
t_w	Clock pulse width	Waveform 1	20		20		ns
t_w	Master Reset pulse width	Waveform 3	20		20		ns
t_s(H)	Setup time, High data to CP	Waveform 2	20		20		ns
t_h(H)	Hold time, High data to CP	Waveform 2	5		5		ns
t_s(L)	Setup time, Low data to CP	Waveform 2	20		20		ns
t_h(L)	Hold time, Low data to CP	Waveform 2	5		5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		25		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS[5]		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to outputs	Waveform 1		34 39		30 30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to outputs	Waveform 3		29 39		35 35	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

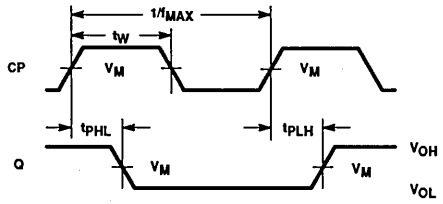
SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to outputs	Waveform 1		44 51		39 39	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to outputs	Waveform 3		33 51		46 46	ns ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

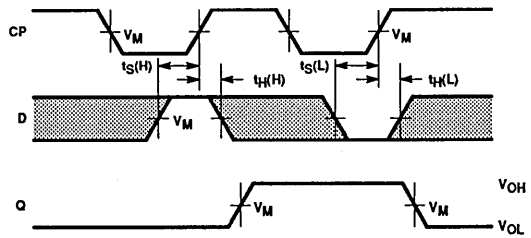
SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			Min	Max	Min	Max	
t_w	Clock pulse width	Waveform 1	20		20		ns
t_w	Master Reset pulse width	Waveform 3	20		20		ns
t_s(H)	Setup time, High data to CP	Waveform 2	20		20		ns
t_h(H)	Hold time, High data to CP	Waveform 2	5		5		ns
t_s(L)	Setup time, Low data to CP	Waveform 2	20		20		ns
t_h(L)	Hold time, Low data to CP	Waveform 2	5		5		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		25		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open and ≥4.0V applied to all Data and Master Reset inputs, I_{CC} is measured after a momentary ground, then 4.0V is applied to clock.
5. These parameters are guaranteed, but not tested.

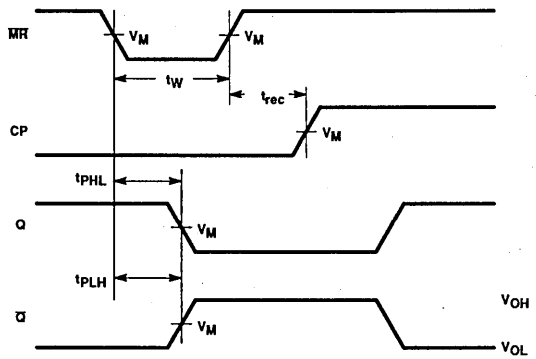
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



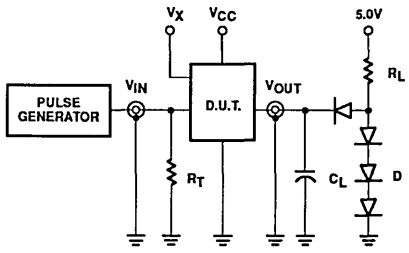
Waveform 2. Data Setup and Hold Times



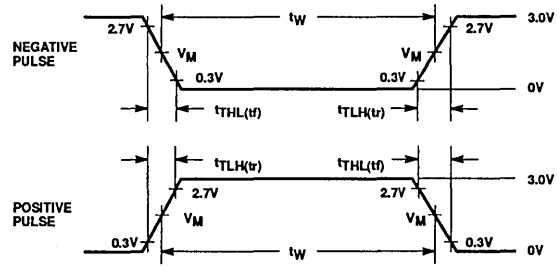
Waveform 3. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

NOTE: For all waveforms V_M = 1.5V for 54 and 54S; V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54S181
Arithmetic Logic Unit

4-Bit Arithmetic Logic Unit

Product Specification

Military Logic Products

FEATURES

- **Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations**
- **Full lookahead carry for high-speed arithmetic operation on long words**

DESCRIPTION

The 54S181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0-S_3) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active High or active Low operands. The Function Table list these operations.

ORDERING INFORMATION

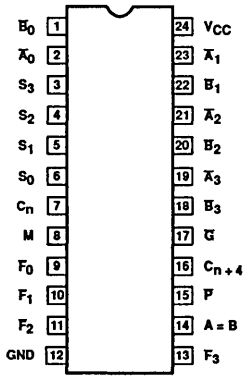
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54S181/BJA
24-Pin Ceramic FlatPack	54S181/BKA
28-Pin Ceramic LLCC	54S181/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S
Mode	Input	1SUL
$\overline{A}$ or $\overline{B}$	Inputs	3SUL
S	Inputs	4SUL
Carry	Input	5SUL
F_0-F_3 = B, C_{n+4}	Outputs	10SUL
$\overline{G}$	Output	10SUL
$\overline{P}$	Output	10SUL

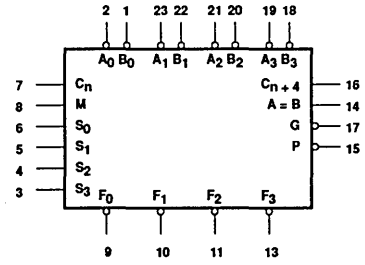
NOTE: Where a 54S Unit Load (SUL) IS 50μA I_{IH} and -2.0mA I_{IL}.

PIN CONFIGURATION



For LLCC Pin Assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignments, see JEDEC Standard No. 2

When the Mode Control Input (M) is High, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the '182 carry lookahead circuit. One carry lookahead package is required for each group of four '181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

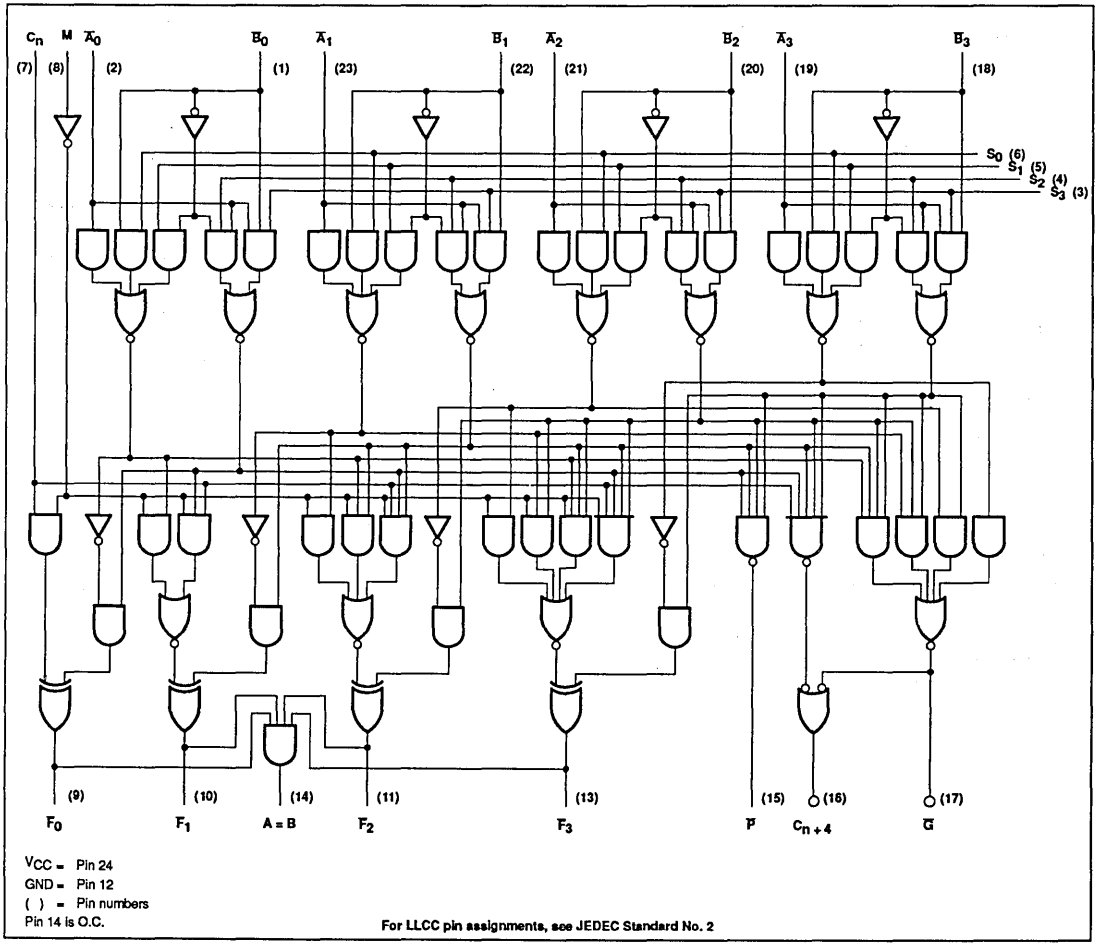
The A = B output from the device goes High when all four $\overline{F}$ outputs are High and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is not underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active Low inputs producing active Low outputs or with active High inputs producing active High outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

LOGIC DIAGRAM



VCC = Pin 24
GND = Pin 12
( ) = Pin numbers
Pin 14 is O.C.

For LLCC pin assignments, see JEDEC Standard No. 2

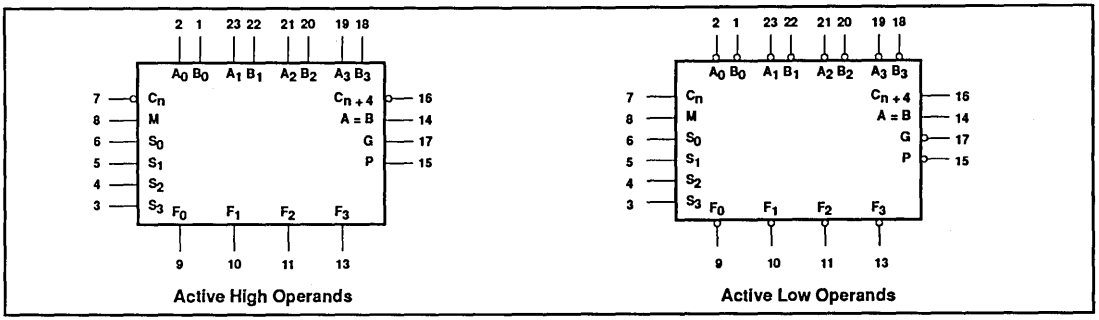
MODE SELECT — FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M = H)	Arithmetic ** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	Logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	A ⊕ B	A minus B minus 1
L	H	H	H	A$\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}$ + B	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	A + $\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

MODE SELECT — FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	Logic (M = H)	Arithmetic ** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}$ + B	A$\overline{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$
H	L	L	L	$\overline{A}$B	A plus (A + B)
H	L	L	H	A ⊕ B	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A
H	H	H	L	AB	A$\overline{B}$ plus A
H	H	H	H	A	A

L = Low voltage
H = High voltage level
* = Each bit is shifted to the next more significant position.
** = Arithmetic operations expressed in 2s complement notation.



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				+0.8	V
		+125°			+0.7	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current except A = B				-1000	µA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		-55		+125	°C

SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = 1$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 1	Apply GND	Apply 1	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{N+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_N	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

NOTE:

1. $2.7V \leq HI \leq V_{CC}$

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_0 = S_3 = 1$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 1	Apply GND	Apply 1	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PHL} t_{PHL}	C_N	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 1	Apply GND	Apply 1	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	F_i	$S_1 = S_2 = M = 1$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	F_i	$S_1 = S_2 = M = 1$ $S_0 = S_3 = 0V$

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	Any output except $\overline{A}$ = B	2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,				0.5	V
		I_{OH} = Max	+125°			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, $I_I = I_{IK}$				-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V	Mode input			1.0	mA
			$\overline{A}$ or $\overline{B}$ inputs			1.0	mA
			S inputs			1.0	mA
			Carry input			1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	Mode input			50	µA
			$\overline{A}$ or $\overline{B}$ inputs			150	µA
			S inputs			200	µA
			Carry input			250	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V	Mode input			-2	mA
			$\overline{A}$ or $\overline{B}$ inputs			-6	mA
			S inputs			-8	mA
			Carry input			-10	mA
I_{OH}	High-level output current	V_{IH} = Min, V_I = Max, V_{OH} = 5.5V A = B only				250	µA
I_{OS}	Short-circuti output current[4]	V_{CC} = Max Any output except A = B		-40		-100	mA
I_{CC}	Supply current[5] (total)	V_{CC} = Max	Note 5a		120	220	mA
			Note 5b		120	220	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 15pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		10.5 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}$ outputs	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	$M = S_0 = S_3 - 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		15 15	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		15 15	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A_i}$ or $\overline{B_i}$ inputs to $\overline{F_i}$ outputs	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		16.5 16.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A_i}$ or $\overline{B_i}$ inputs to $\overline{F_i}$ outputs	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		20 22	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A_i}$ or $\overline{B_i}$ inputs to $\overline{F_i}$ outputs	M = 4.5V, Logic Mode see Waveform 2 and Table III		20 22	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output	$M = 0V$, $S_0 = S_3 = 4.5V$, $S_1 = S_2 = 0V$ Sum Mode, see Waveform 1 and Table I		18.5 18.5	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} outputs	$M = 0V$, $S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 4 and Table II		23 23	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to A = B output	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		23 30	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[6]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		13.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}$ outputs	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	$M = S_0 = S_3 - 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		18.0 18.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		18.0 18.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	$M = S_1 = S_2 = 0V$, $S_0 = S_3 = 4.5V$ Sum Mode, see Waveform 2 and Table I		20.0 20.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		23.0 25.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = 4.5V, Logic Mode see Waveform 2 and Table III		24.0 26.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output	$M = 0V$, $S_0 = S_3 = 4.5V$, $S_1 = S_2 = 0V$ Sum Mode, see Waveform 1 and Table I		23.0 23.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} outputs	$M = 0V$, $S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 4 and Table II		27.0 26.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to A = B output	$M = S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$ Diff Mode, see Waveform 3 and Table II		27.0 33	ns ns

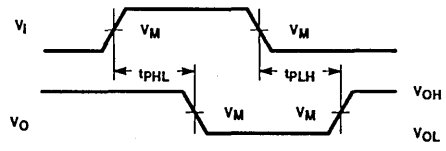
AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		14.5 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}$ outputs	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		16.0 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		16.0 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	M = S_0 = S_3 - 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		20.0 20.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		16.0 16.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		20.0 20.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A_i}$ or $\overline{B_i}$ inputs to $\overline{F_i}$ outputs	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		23.0 23.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A_i}$ or $\overline{B_i}$ inputs to $\overline{F_i}$ outputs	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		26.0 28.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A_i}$ or $\overline{B_i}$ inputs to $\overline{F_i}$ outputs	M = 4.5V, Logic Mode see Waveform 2 and Table III		26.0 28.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output	M = 0V, S_0 = S_3 = 4.5V, S_1 = S_2 = 0V Sum Mode, see Waveform 1 and Table I		25.0 25.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} outputs	M = 0V, S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 4 and Table II		29.0 29.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ or $\overline{B}$ inputs to A = B output	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		29.0 36.0	ns ns

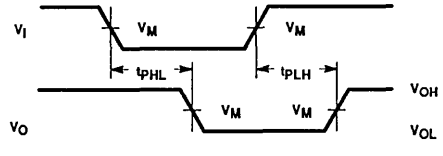
NOTES:

2. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
3. All typical values are at V_{CC} = 5V, T_A = 25°C.
4. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
5. I_{CC} is measured with the following conditions:
   a. S_0 through S_3, M, and A inputs are ≥ 4.0V, other inputs grounded, all outputs open.
   b. S_0 through S_3 and M inputs are ≥ 4.0V, other inputs grounded, all outputs open.
6. These parameters are guaranteed, but not tested.

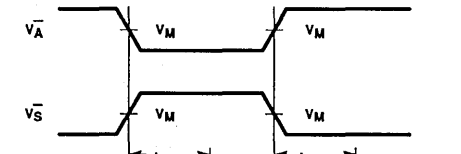
AC WAVEFORMS



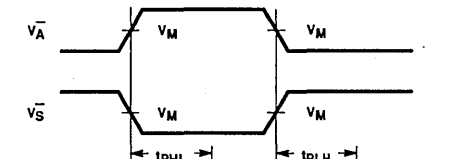
Waveform 1



Waveform 2



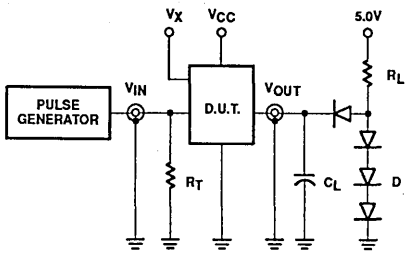
Waveform 3



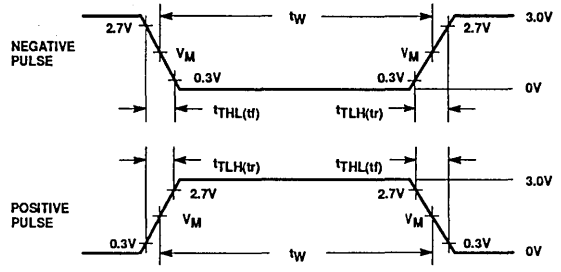
Waveform 4

NOTE: V_M = 1.5V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	280kΩ	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS191
Counter

Presettable 4-Bit Binary Up/Down Counter

Product Specification

FEATURES

- **Synchronous, reversible counting**
- **4-bit binary counter**
- **Asynchronous parallel load capability**
- **Count enable control for synchronous expansion**
- **Single Up/Down control input**

DESCRIPTION

The 54LS191 is an asynchronously presettable up/down 4-bit binary counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is Low. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a High level on the Count Enable ($\overline{CE}$) input. When $\overline{CE}$ is Low, internal state changes are initiated synchronously by the Low-to-High transition of the Clock input. The Up/Down ($\overline{U}$/D) input signal determines the direction of counting as indicated in the Mode Select Table. The $\overline{CE}$ input may go Low when the clock is in either state, however, the Low-to-High $\overline{CE}$ transition must occur only when the clock is High. Also, the $\overline{U}$/D input should be changed only when either $\overline{CE}$ or CP is High.

Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally Low and goes High when a circuit reaches zero in the count-down mode or reaches "15" in the count-up mode for 54LS191. The TC output will remain High until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

The TC signal is used internally to enable the $\overline{RC}$ output. When TC is High and $\overline{CE}$ is Low, the RC follows the Clock Pulse (CP) delayed by two gate delays. The $\overline{RC}$ output essentially duplicates the Low clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multi-stage counters, as indicated in Figures A and B. In Figure A, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a High signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The time skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

ORDERING INFORMATION

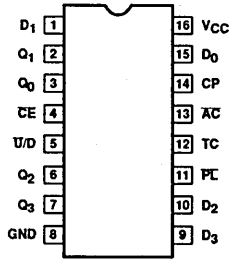
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS191/BEA
16-Pin Ceramic FlatPack	54LS191/BFA
20-Pin Ceramic LLCC	54LS191/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
$\overline{CE}$	Input	3LSUL
Other	Inputs	1LSUL
All	Outputs	10LSUL

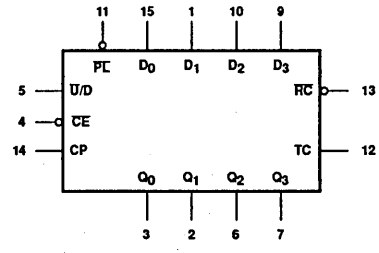
NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

Figure B shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The Low state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes High, there is no such restriction on the High state duration of the clock.

In Figure C, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure A and B does not apply.

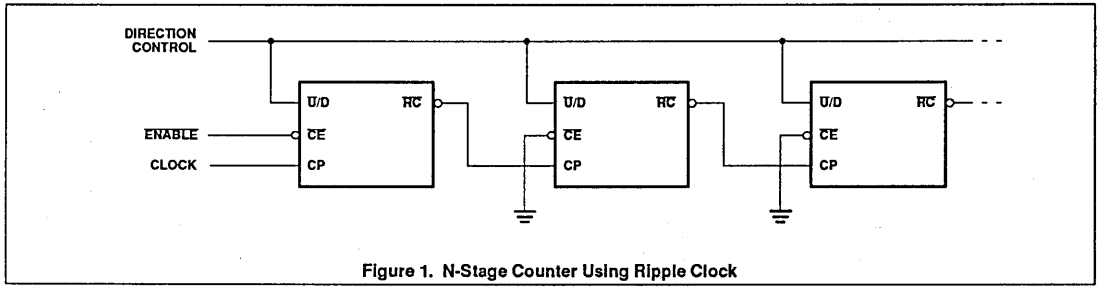


Figure 1. N-Stage Counter Using Ripple Clock

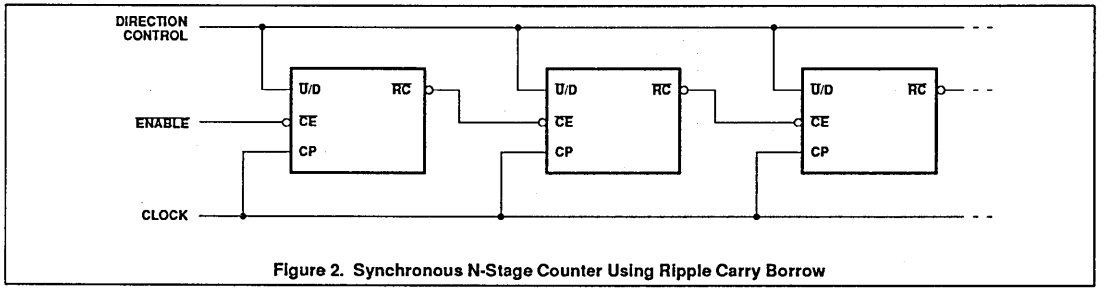


Figure 2. Synchronous N-Stage Counter Using Ripple Carry Borrow

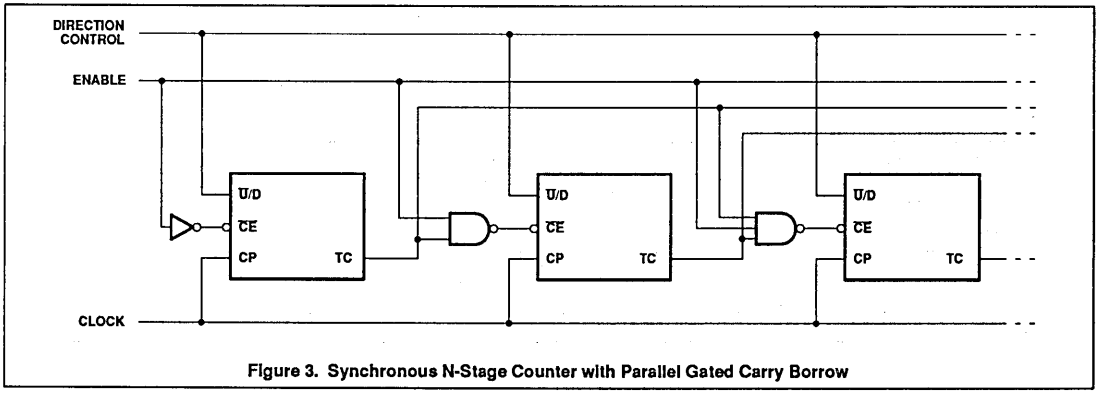
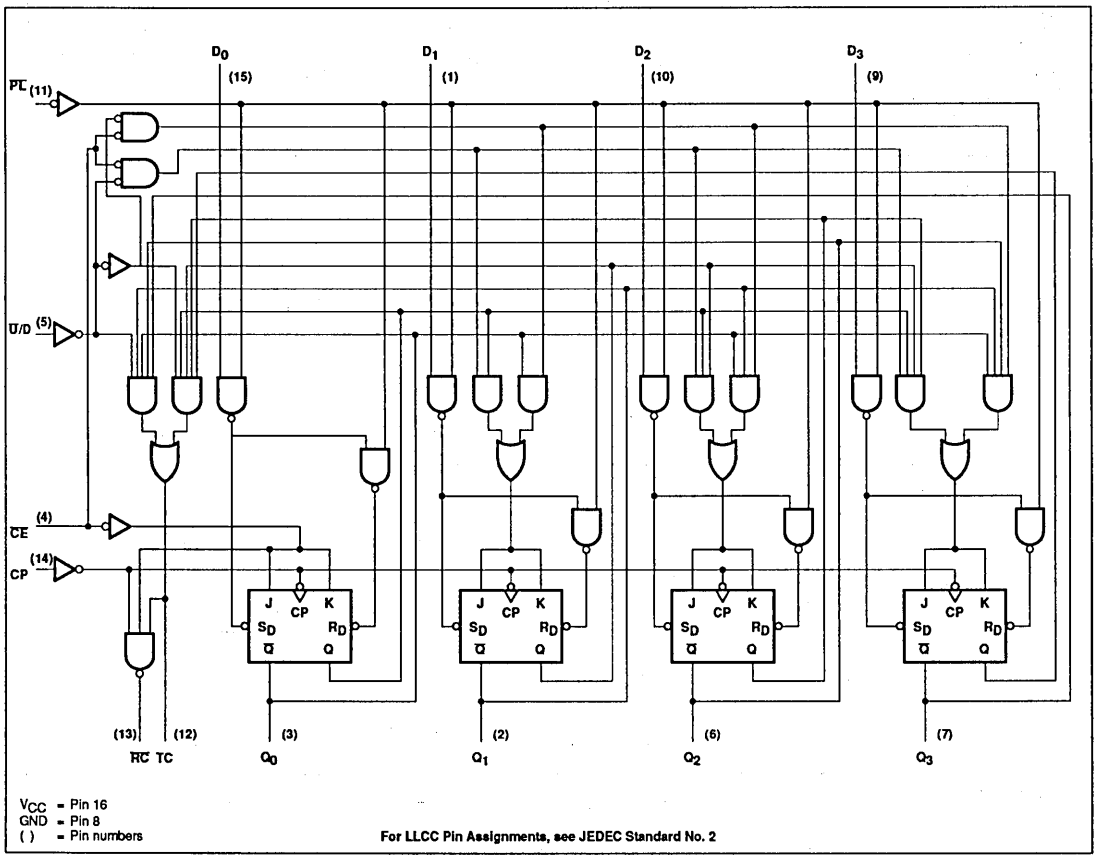


Figure 3. Synchronous N-Stage Counter with Parallel Gated Carry Borrow

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	U/D	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L L	X X	X X	X X	L H	L H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊔	H	H	H	H	⌐	⊔
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	⌐	⊔

H = High voltage level steady state
L = Low voltage level steady state
I = Low voltage level one set-up time prior to Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
⊔ = Low pulse
⌐ = TC goes Low on a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V	$\overline{CE}$ input			0.3	mA
			Other inputs			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	$\overline{CE}$ input			60	µA
			Other inputs			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V	$\overline{CE}$ input			-1.2	mA
			Other inputs			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			20	35	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 15pF$		
			Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	20		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Q output	Waveform 1		24 36	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to $\overline{RC}$ output	Waveform 2		20 24	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to TC output	Waveform 1		42 52	ns ns
t_{PLH} t_{PHL}	Propagation delay U/D to $\overline{RC}$ output	Waveform 7		45 45	ns ns
t_{PLH} t_{PHL}	Propagation delay U/D to TC output	Waveform 7		33 33	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Q outputs	Waveform 3		32 40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to any output	Waveform 4		33 50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$ output	Waveform 2		33 33	ns ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	CP pulse width	Waveform 1	25		ns
t_W	$\overline{PL}$ pulse width	Waveform 5	35		ns
t_s	Setup time, data to $\overline{PL}$	Waveform 6	20		ns
t_h	Hold time, data to $\overline{PL}$	Waveform 6	5		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 5	40		ns
$t_s(L)$	Setup time, Low $\overline{CE}$ to clock	Waveform 8	40		ns
$t_h(L)$	Hold time, Low $\overline{CE}$ to clock	Waveform 8	0		ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	20		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Q output	Waveform 1		29 41	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to $\overline{RC}$ output	Waveform 2		25 29	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to TC output	Waveform 1		47 57	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to $\overline{RC}$ output	Waveform 7		50 50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to TC output	Waveform 7		38 38	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Q outputs	Waveform 3		37 45	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to any output	Waveform 4		38 55	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$ output	Waveform 2		38 38	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[5]

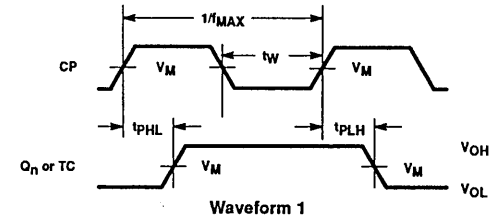
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	20		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Q output	Waveform 1		38 53	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to $\overline{RC}$ output	Waveform 2		33 38	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to TC output	Waveform 1		61 74	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to $\overline{RC}$ output	Waveform 7		65 65	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}/D$ to TC output	Waveform 7		49 49	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Q outputs	Waveform 3		49 59	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to any output	Waveform 4		49 72	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$ output	Waveform 2		49 49	ns ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

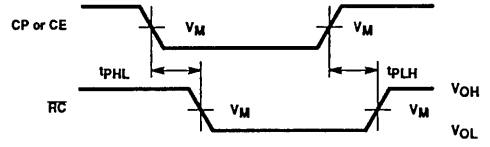
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	CP pulse width	Waveform 1	25		ns
t_W	$\overline{PL}$ pulse width	Waveform 5	30		ns
t_s	Setup time, data to $\overline{PL}$	Waveform 6	20		ns
t_h	Hold time, data to $\overline{PL}$	Waveform 6	5		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 5	40		ns
$t_s(L)$	Setup time, Low $\overline{CE}$ to clock	Waveform 8	40		ns
$t_h(L)$	Hold time, Low $\overline{CE}$ to clock	Waveform 8	0		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.
5. These parameters are guaranteed, but not tested.

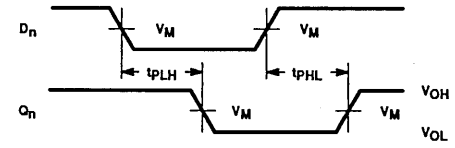
AC WAVEFORMS



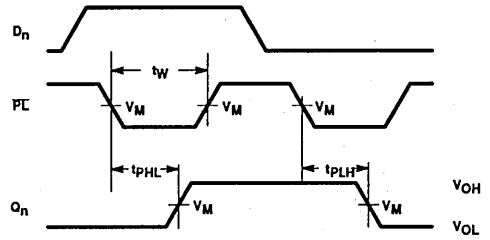
Waveform 1



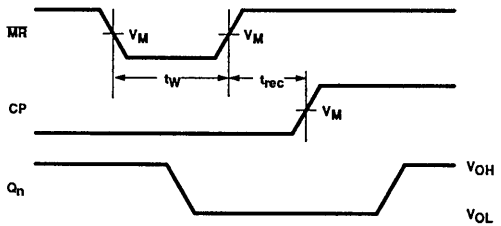
Waveform 2



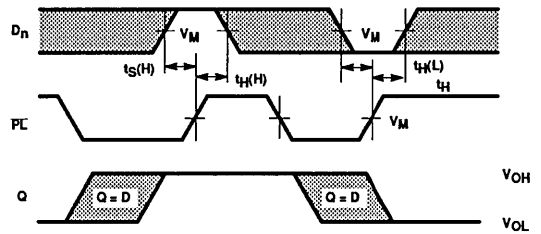
Waveform 3



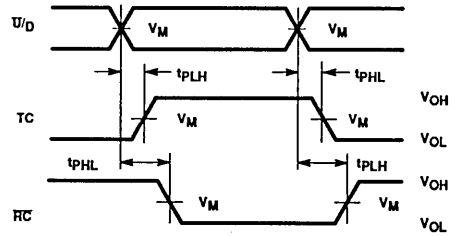
Waveform 4



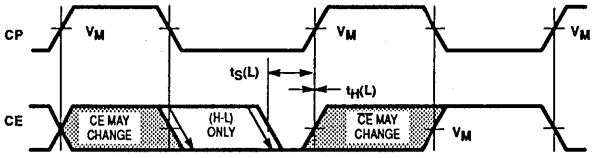
Waveform 5



Waveform 6



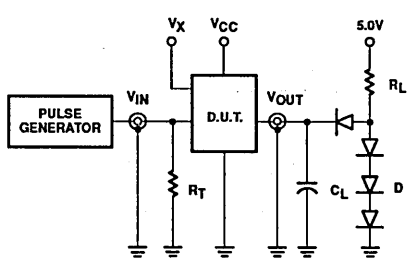
Waveform 7



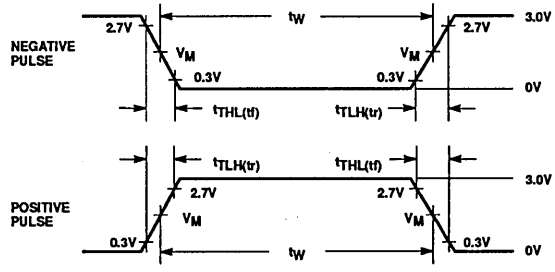
Waveform 8

NOTE: V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54193, 54LS193
Counters

Presettable 4-Bit Binary Up/Down Counters

Product Specification

FEATURES

- **Synchronous reversible 4-bit binary counting**
- **Asynchronous parallel load**
- **Asynchronous reset (clear)**
- **Expandable without external logic**

DESCRIPTION

The 54193 and 54LS193 are 4-bit synchronous up/down counters – that count in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the Low-to-High transition of either Clock input. If the CP_U clock is pulsed while CP_D is held High, the device will count up ... if CP_D is pulsed while the CP_U is held High, the device will count down. Only one Clock input can be held High at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin – it may also be loaded in parallel by activating the asynchronous parallel load pin.

ORDERING INFORMATION

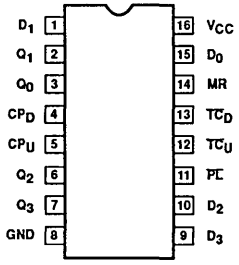
DESCRIPTION	ORDER CODE
Ceramic DIP	54193/BEA 54LS193/BEA
Ceramic Flat Pack	54193/BFA 54LS193/BFA
Ceramic LLCC	54LS193/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54LS
All	Inputs	1UL	1LSUL
All	Outputs	10UL	10LSUL

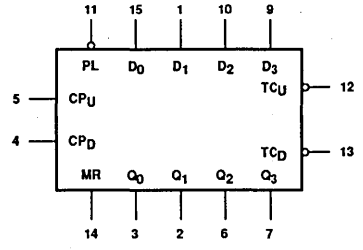
NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see Jedec Standard No. 2

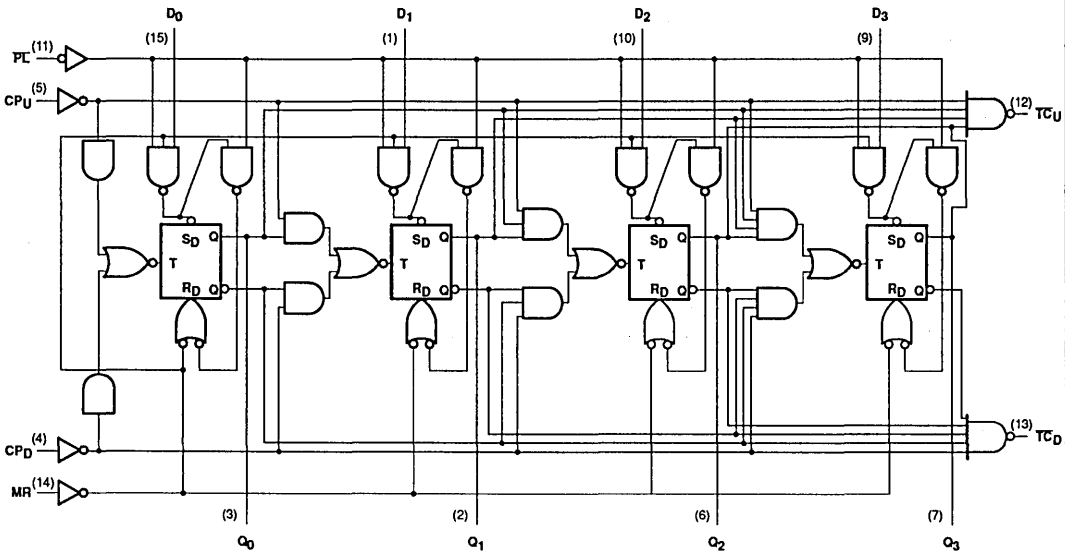
LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

For LLCC pin assignments, see Jedec Standard No. 2

LOGIC DIAGRAM



For LLCC pin assignments, see Jedec Standard No. 2

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count-up and count-down functions.

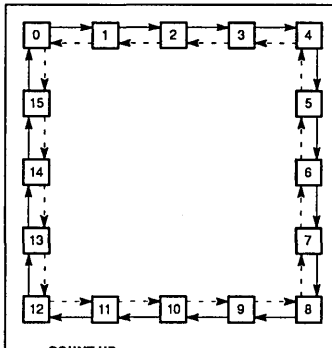
Each flip-flop contains JK feedback from slave to master, such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held High while counting with the other, because the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count down ($\overline{TC}_D$) outputs are normally High. When the circuit has reached the maximum count state of the next High-to-Low transition of CP_U will cause $\overline{TC}_U$ to go Low. $\overline{TC}_U$ will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go Low when the circuit is in the zero state and the CP_D goes Low. The $\overline{TC}$ outputs can be used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load ($\overline{PL}$) input is Low. A High level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs Low. If one of the Clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of that clock will be interpreted as a legitimate signal and will be counted.

STATE DIAGRAM



$\overline{TC}_U = Q_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_U$

$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$

Logic Equations for Terminal Count

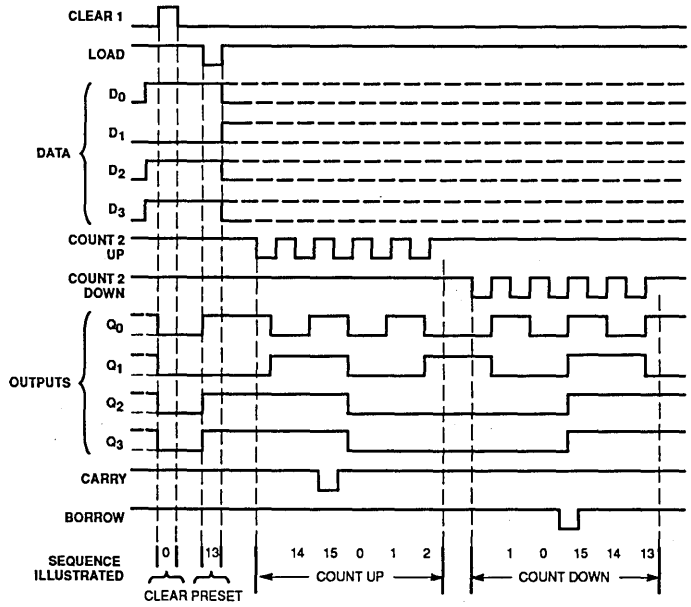
MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	$\overline{MR}$	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC_U}$	$\overline{TC_D}$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H[c]	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H[d]

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

NOTES:
c. TC_U = CP_U at terminal count up (HHHH)
d. TC_D = CP_D at terminal count down (LLLL)

FUNCTIONAL WAVEFORMS Typical clear, load, and count sequences



NOTES:
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be high; when counting down, count-up input must be high.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54	54LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to $+V_{CC}$	-0.5 to $+V_{CC}$	V
T_{STG}	Storage temperature range	-65 to +150		°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54			54LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.8			+0.7	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	High-level output current			-800			-400	µA
I_{OL}	Low-level output current			16			4	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54193			54LS193			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.2	0.4		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V			1.0				mA
			V_I = 7.0V						0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V			40				µA
			V_I = 2.7V						20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V				-1.6			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-65	-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			65	89		19	34	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U input to $\overline{TC}_U$ output	Waveform 2		26 24		26 24	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_D input to $\overline{TC}_D$ output	Waveform 2		24 24		24 24	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n outputs	Waveform 1		38 47		38 47	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ input to Q_n output	Waveform 3		40 40		40 40	ns ns
t_{PHL}	Propagation delay MR to output	Waveform 4		35		35	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			Min	Max	Min	Max	
t_W	CP_U pulse width	Waveform 1	20		20		ns
t_W	CP_D pulse width	Waveform 1	20		20		ns
t_W	$\overline{PL}$ pulse width	Waveform 3	20		20		ns
t_W	MR pulse width	Waveform 4	20		20		ns
t_s	Setup time, data to $\overline{PL}$	Waveform 5	20		20		ns
t_h	Hold time, data to $\overline{PL}$	Waveform 5	0		5		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 3	40		40		ns
t_{rec}	Recovery time, MR to CP	Waveform 4	40		40		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U input to $\overline{TC}_U$ output	Waveform 2		30 28		31 29	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_D input to $\overline{TC}_D$ output	Waveform 2		28 28		29 29	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n outputs	Waveform 1		42 51		43 52	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ input to Q_n output	Waveform 3		44 44		45 45	ns ns
t_{PHL}	Propagation delay MR to output	Waveform 4		39		40	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

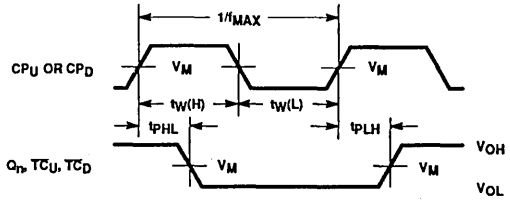
SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U input to $\overline{TC}_U$ output	Waveform 2		39 36		40 38	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_D input to $\overline{TC}_D$ output	Waveform 2		36 36		38 38	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n outputs	Waveform 1		55 66		56 68	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ input to Q_n output	Waveform 3		57 57		59 59	ns ns
t_{PHL}	Propagation delay, MR to output	Waveform 4		51		52	ns

AC SETUP REQUIREQUENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

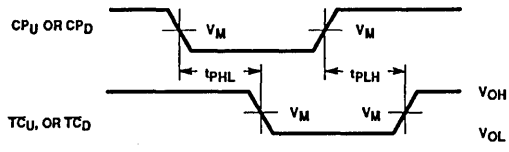
SYMBOL	PARAMETER	TEST CONDITIONS	54		54LS		UNIT
			Min	Max	Min	Max	
t_W	CP_U pulse width	Waveform 1	26		20		ns
t_W	CP_D pulse width	Waveform 1	26		20		ns
t_W	$\overline{PL}$ pulse width	Waveform 3	20		20		ns
t_W	MR pulse width	Waveform 4	20		20		ns
t_s	Setup time, data to $\overline{PL}$	Waveform 5	20		30		ns
t_h	Hold time, data to $\overline{PL}$	Waveform 5	0		10		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 3	40		40		ns
t_{rec}	Recovery time, MR to CP	Waveform 4	40		40		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short should not exceed one second.
4. Measure I_{CC} with Parallel Load and Master Reset inputs grounded, all other outputs ≥4.0V and all outputs open.
5. These parameters are guaranteed, but not tested.

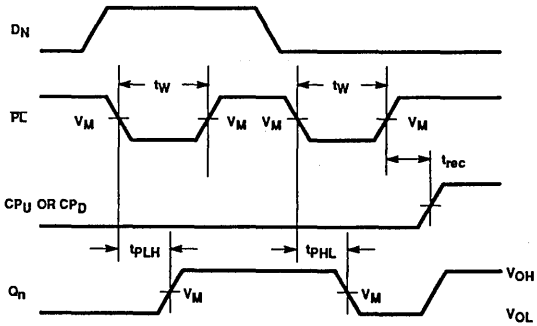
AC WAVEFORMS



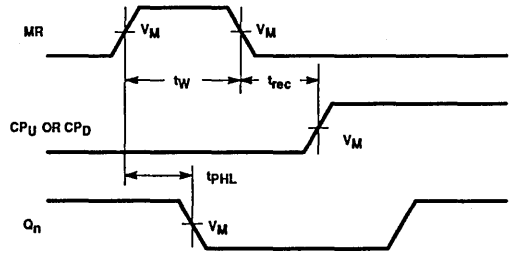
Waveform 1. Clock to Output Delays and Clock Pulse Width



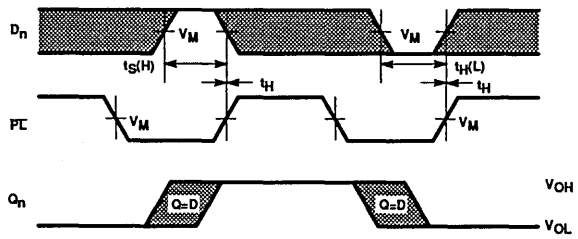
Waveform 2. Clock to Terminal Count Delays



Waveform 3. Parallel Load Pulse Width, Parallel Load to Output Delays, and Parallel Load to Clock Recovery Time



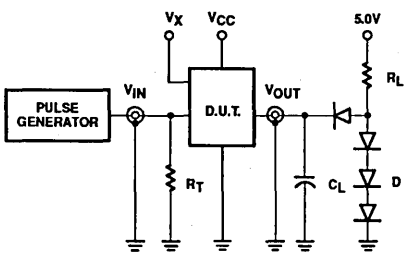
Waveform 4. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



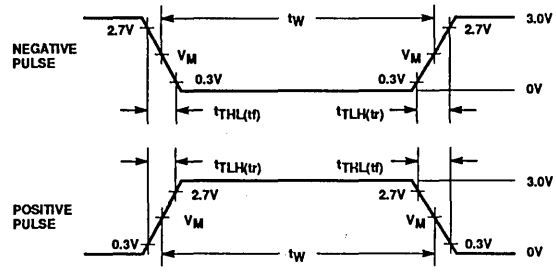
Waveform 5. Setup and Hold Times Data to Parallel Load (PL)

NOTE: V_M = 1.3V for 54LS; V_M = 1.5V for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



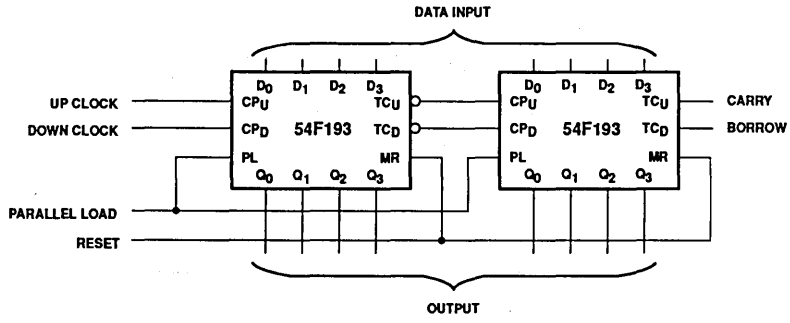
Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per Function Table.

APPLICATION DIAGRAM



8-Bit Up/Down Counter With Parallel Load

Signetics

Military Logic Products

54194
Shift Register

4-Bit Bidirectional Universal Shift Register

Product Specification

FEATURES

- **Buffered clock and control inputs**
- **Shift left and shift right capability**
- **Synchronous parallel and serial data transfers**
- **Easily expanded for both serial and parallel operation**
- **Asynchronous master reset**
- **Hold (do nothing) mode**

DESCRIPTION

The functional characteristics of the 54194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 20ns (typical), making the device especially useful for implementing very high-speed CPUs, or for memory buffer registers.

ORDERING INFORMATION

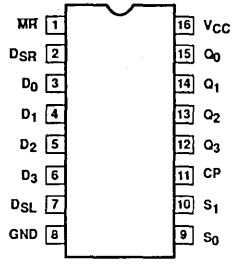
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54194/BEA
Ceramic Flat Pack	54194/BFA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54
All	Inputs	1UL
Q_0 - Q_3	Outputs	10UL

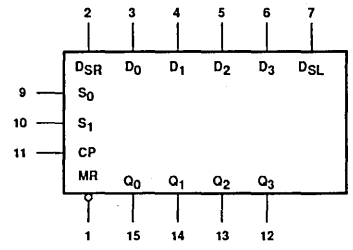
NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH} and -1.6mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see Jedec Standard No. 2

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

For LLCC pin assignments, see Jedec Standard No. 2

Shift Register | 54194

The 54194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or right to left (shift left, $Q_3 \rightarrow Q_2$, etc.), or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are Low, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

The Mode Select inputs of the 54194 are gated with the clock and should be changed from High-to-Low only while the Clock input is High.

The four parallel data inputs (D_0 - D_3) are D-type inputs. Data appearing on D_0 - D_3 inputs when S_0 and S_1 are High is transferred to the Q_0 - Q_3 outputs, respectively, following the next Low-to-High transition of the clock. When Low, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs Low.

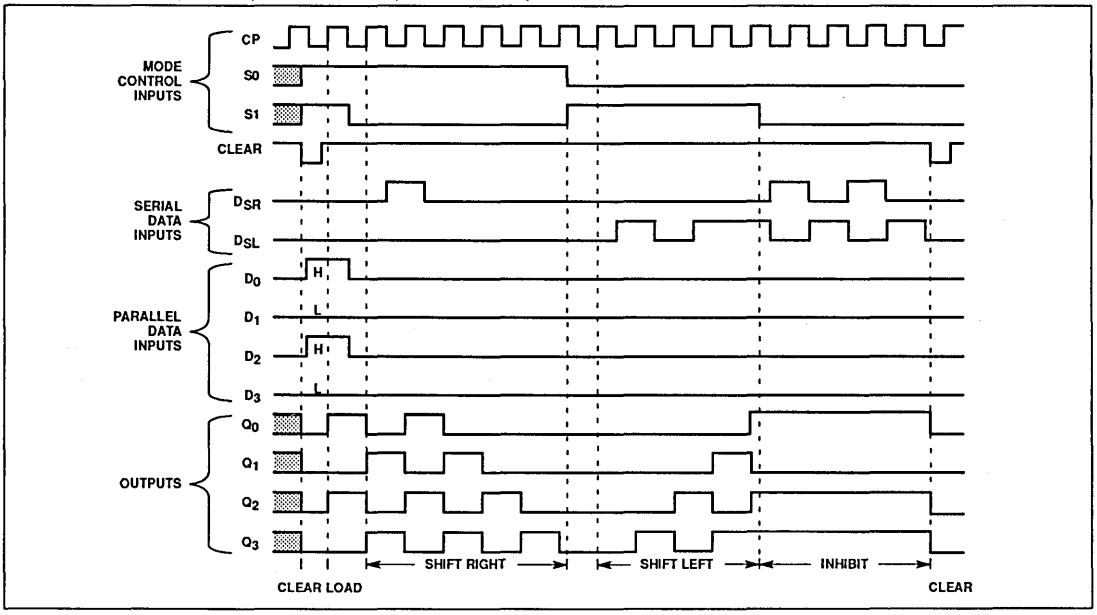
MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l[a]	l[a]	X	X	X	q_0	q_1	q_2	q_3
Shift left	↑	H	h	l[a]	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l[a]	X	h	X	q_1	q_2	q_3	H
Shift right	↑	H	l[a]	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l[a]	h	h	X	X	H	q_0	q_1	q_2
Parallel load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the Low-to-High clock transition
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

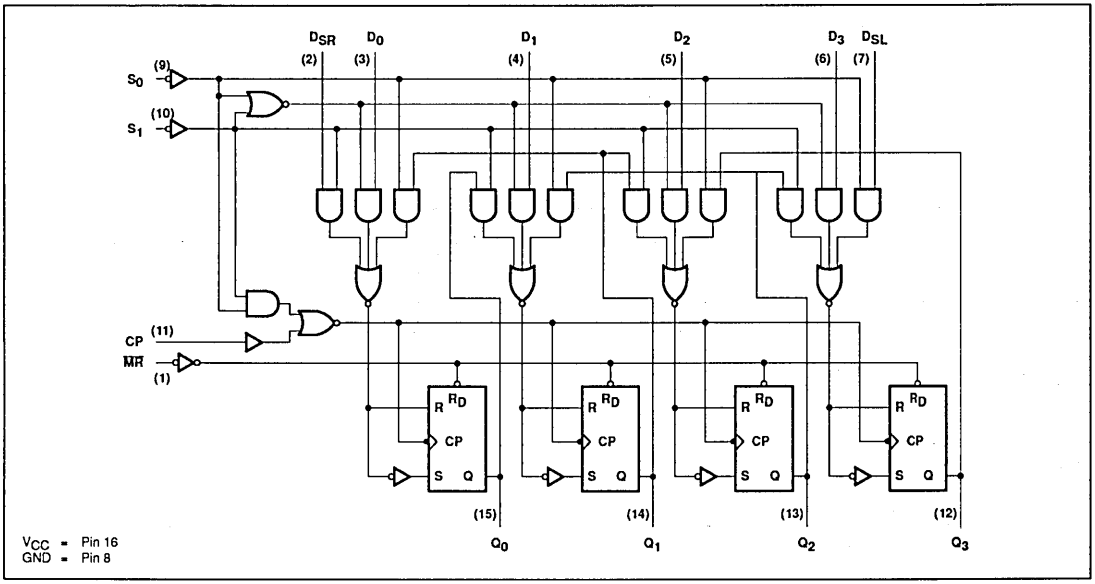
NOTE:
a. The High-to-Low transition of the S_0 and S_1 inputs on the 54194 should only take place while CP is High for conventional operation.

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



Shift Register | 54194

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-12	mA
I_{OH}	High-level output voltage			-800	µA
I_{OL}	Low-level output current			16	mA
T_A	Operating free-air temperature range	-55		+125	°C

Shift Register | 54194

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V			-1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-20		-57	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max		39	63	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS C_L = 15pF		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		22 26	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		37	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
$t_W(H)$	Clock pulse width High	Waveform 1	20		ns
$t_W(L)$	$\overline{MR}$ pulse width, Low	Waveform 2	20		ns
t_s	Setup time, data to clock	Waveform 3	20		ns
t_h	Hold time, data to clock	Waveform 3	0		ns
$t_s(L)$	Setup time Low, S_n to CP[(a)]	Waveform 4	30		ns
$t_s(H)$	Setup time High, S_N to CP	Waveform 4	30		ns
t_h	Hold time, S_n to CP	Waveform 4	0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	25		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS C_L = 50pF		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		26 30	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		41	ns

Shift Register | 54194

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

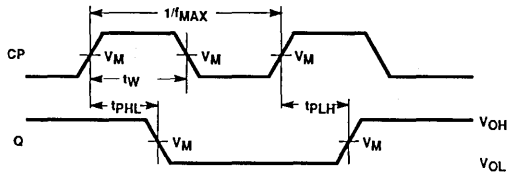
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS C_L = 50pF		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		34 39	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		53	ns

AC SETUP REQUIREQUENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

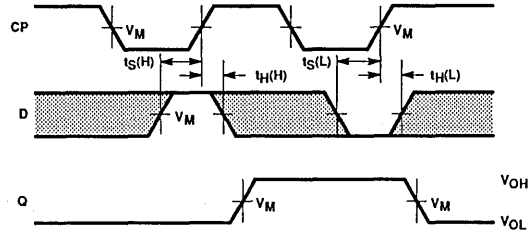
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
$t_W(H)$	Clock pulse width, High	Waveform 1	20		ns
$t_W(L)$	$\overline{MR}$ pulse width, Low	Waveform 2	20		ns
t_s	Setup time, data to clock	Waveform 3	20		ns
t_h	Hold time, data to clock	Waveform 3	7		ns
$t_s(L)$	Setup time Low, S_n to CP[a]	Waveform 4	30		ns
$t_s(H)$	Setup time High, S_N to CP	Waveform 4	30		ns
t_h	Hold time, S_n to CP	Waveform 4	7		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	25		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short curcuit should not exceed one second.
4. With all outputs open, D_i inputs grounded and ≥4.0V applied to S_0, S_1, $\overline{MR}$ and the serial inputs, I_{CC} is tested with a momentary ground, then ≥4.0V applied to CP.
5. These parameters are guaranteed, but not tested.

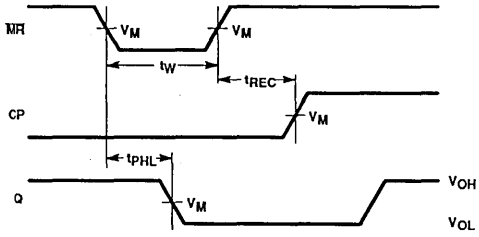
AC WAVEFORMS



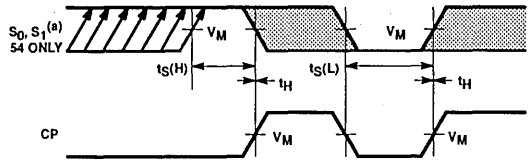
Waveform 1. Clock to Output Delays and Clock Pulse Width



Waveform 2. Data Setup and Hold Times



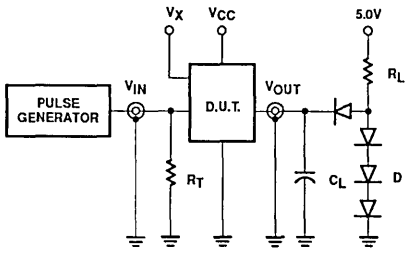
Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



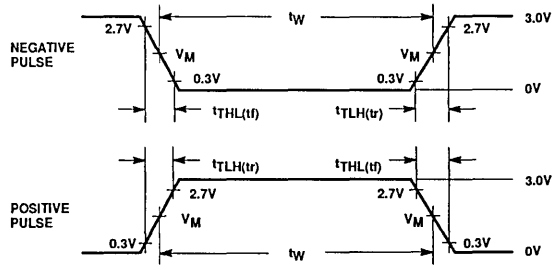
Waveform 4. Setup and Hold Times for S_0 and S_1 Inputs

NOTES: For all waveforms, V_M = 1.5V for 54S
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54XXX	400Ω	1.5V	1MHz	500ns	≤7ns	≤7ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54LS195A
Shift Register

4-Bit Parallel Access Shift Register

Product Specification

Military Logic Products

FEATURES

- **Buffered clock and control inputs**
- **Shift right and parallel load capability**
- **J-$\overline{K}$ (D) inputs to first stage**
- **Complement output from last stage**
- **Asynchronous Master Reset**

DESCRIPTION

The functional characteristics of the 54LS195A 4-bit Parallel Access Shift register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The 54LS195A operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input.

Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is High, and is shifted 1 bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each Low-to-High clock transition. The J and $\overline{K}$ inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D type input for general applications. The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is Low. After the Low-to-High clock transition, data on the parallel inputs (D_0 - D_3) is transferred to the respective Q_0 - Q_3 outputs.

Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1}) inputs and holding the $\overline{PE}$ input low.

ORDERING INFORMATION

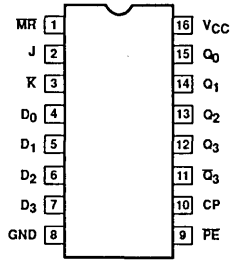
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS195A/BEA
Ceramic Flat Pack	54LS195A/BFA
Ceramic LLCC	54LS195A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
All	Inputs	1LSUL
All	Outputs	10LSUL

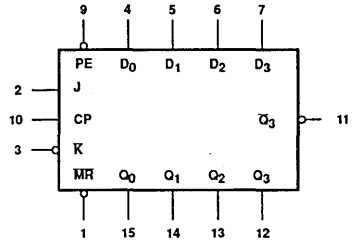
NOTE: Where a 54LS Unit Load (LSUL) is understood to be 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

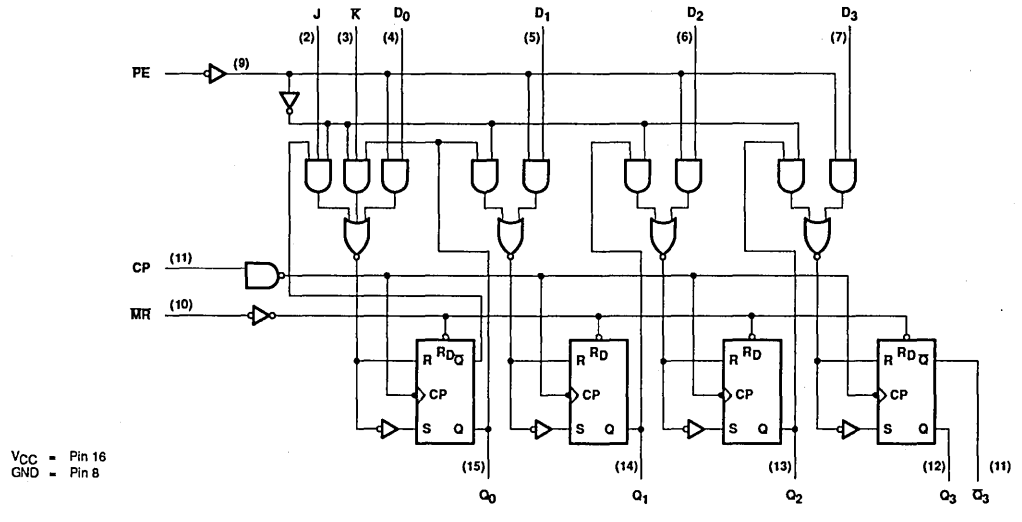
For LLCC pin assignments, see JEDEC Standard No. 2

Shift Register | 54LS195A

All parallel and serial data transfers are synchronous, occuring after each Low-to-High clock transition. The 54LS195 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the setup and release time requirements.

A Low on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs Low, independent of any other input condition. The $\overline{MR}$ on the 54LS195 is gated with the clock. Therefore, the Low-to-High $\overline{MR}$ transition should only occur while the clock is Low to avoid false clocking on the 54LS195.

LOGIC DIAGRAM



For LLCC Pin Assignments, see JEDEC Standard No. 2

MODE SELECT — FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
Shift, set first stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, reset first stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, toggle first stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, retain first stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H = High voltage level
L = Low voltage level
X = Don't care
l = Low voltage level one setup time prior to the Low-to-High clock transition
h = High voltage level one setup time prior to the Low-to-High clock transition
$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the Low-to-High clock transition
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max	2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}			-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max		14	21	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		22 26	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		30	ns

AC SETUP REQUIREMENTS T_A 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	16		ns
t_W	Master Reset pulse width	Waveform 2	12		ns
t_s	Setup time, J, $\overline{K}$ and data to clock	Waveform 3	15		ns
t_h	Hold time, J, $\overline{K}$ and data to clock	Waveform 3	0		ns
t_s	Setup time, $\overline{PE}$ to clock	Waveform 4	25		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 4	0		ns
t_{rec}	Recovery time, $\overline{MR}$ to clock	Waveform 2	25		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 31	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		35	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		35 40	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		46	ns

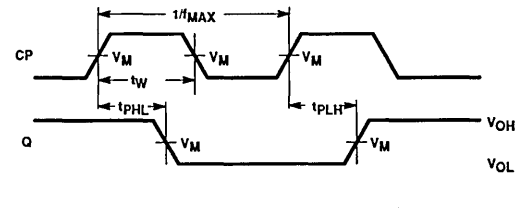
AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	18		ns
t_W	Master Reset pulse width	Waveform 2	12		ns
t_s	Setup time, J, $\overline{K}$ and data to clock	Waveform 3	20		ns
t_h	Hold time, J, $\overline{K}$ and data to clock	Waveform 3	10		ns
t_s	Setup time, $\overline{PE}$ to clock	Waveform 4	25		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 4	10		ns
t_{rec}	Recovery time, $\overline{MR}$ to clock	Waveform 2	25		ns

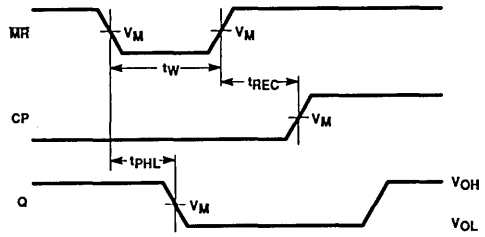
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open, $\overline{PE}$ grounded, and $\geq$ 4.0V applied to the J, $\overline{K}$, and Data inputs, I_{CC} is measured by applying a momentary ground, followed by $\geq$ 4.0V to $\overline{MR}$, and then a momentary ground, followed by $\geq$ 4.0V to clock.
5. These parameters are guaranteed, but not tested.

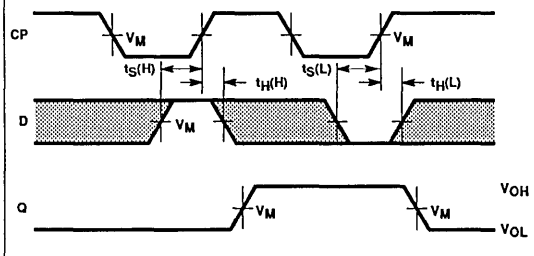
AC WAVEFORMS



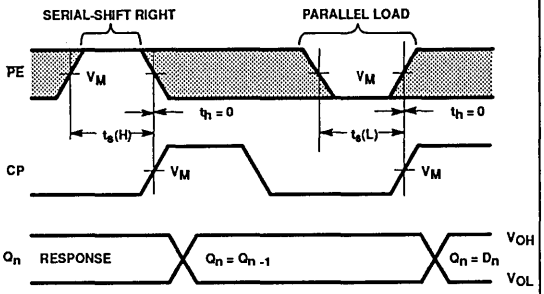
Waveform 1. Clock to Output Delays and Clock Pulse Width



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



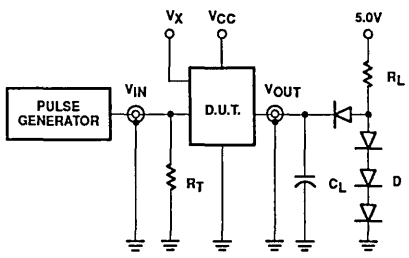
Waveform 3. Data Setup and Hold Times



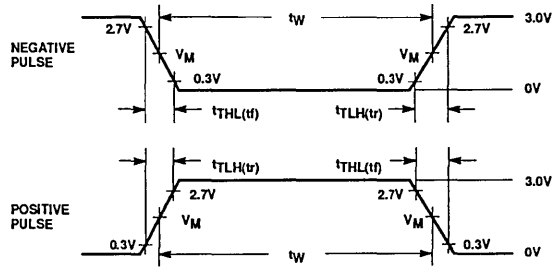
Waveform 4. Setup and Hold Times Parallel Enable to Clock

NOTE: V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS197
Counter

Presettable 4-Bit Binary Ripple Counter

Product Specification

FEATURES

- **High speed 4-bit binary counting**
- **Asynchronous parallel load for presetting counter**
- **Overriding Master Reset**
- **Buffered Q_0 output drives $\overline{CP}_1$ input plus standard fan-out**

DESCRIPTION

The 54LS197 is an asynchronously presettable binary ripple counter partitioned into divide-by-2 and divide-by-8 sections with each section having a separate Clock input. Stage changes are initiated in the counting modes by the High-to-Low transition of the Clock inputs, however, state changes of the Q outputs do not occur simultaneously because of the internal ripple delays. Designers should keep in mind when using external logic to decode the Q outputs, that the unequal delays can lead to decoding spikes, and thus a decoded signal should not be used as a strobe or clock.

The Q_0 flip-flop is triggered by the $\overline{CP}_0$ input while the $\overline{CP}_1$ input triggers the divide-by-8 section.

The device has an asynchronous active-Low Master Reset ($\overline{MR}$) input which overrides all other inputs and forces all outputs Low. The counter is also asynchronously presettable. A Low on the Parallel Load ($\overline{PL}$) input overrides the Clock inputs and loads the data from parallel Data (D_0 - D_3) inputs into the flip-flops. The counter acts as a transparent latch while the $\overline{PL}$ is Low and any change in the D_n inputs will be reflected in the outputs.

ORDERING INFORMATION

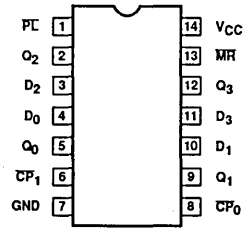
DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54LS197/BCA
14-Pin Ceramic FlatPack	54LS197/BDA
20-Pin Ceramic LLCC	54LS197/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
$\overline{CP}_0$	Clock input	6LSUL
$\overline{CP}_1$	Clock input	3.5LSUL
All	Other inputs	1LSUL
Q_0 - Q_3	Outputs	10LSUL

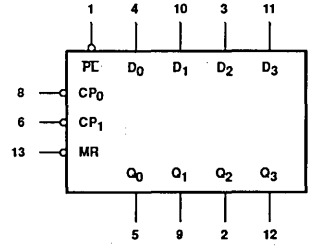
NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

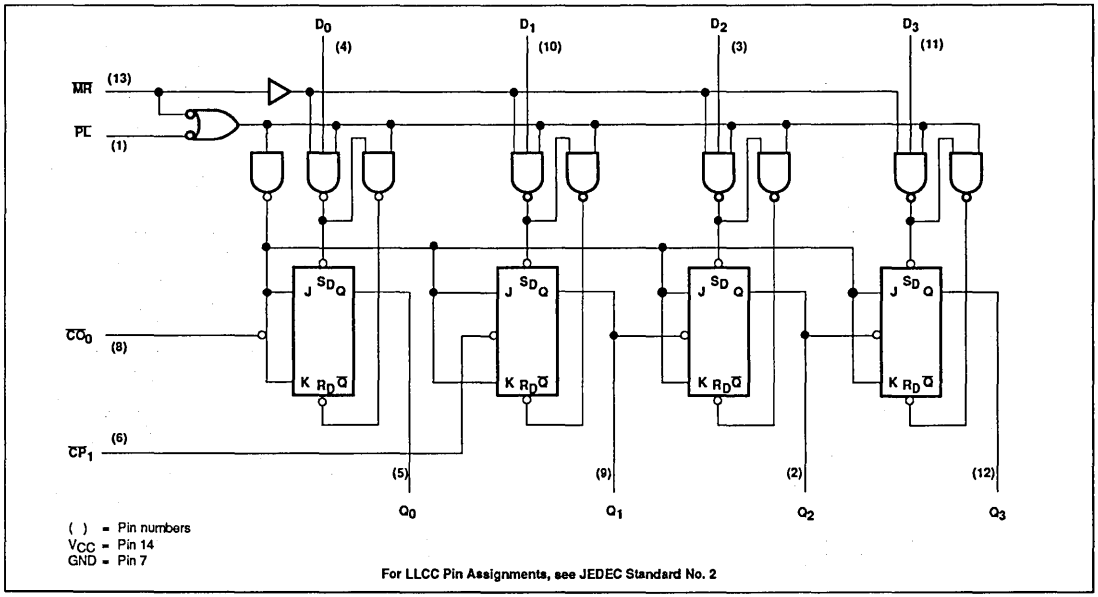
LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7

For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC Pin Assignments, see JEDEC Standard No. 2

COUNT SEQUENCE

COUNT	4-BIT BINARY[1]			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE: Q_0 connected to input $\overline{CP}_1$; input applied to $\overline{CP}_0$

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUT
	$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	D_n	Q_n
Reset (clear)	L	X	X	X	L
Parallel load	H H	L L	X X	L H	L H
Count	H	H	↓	X	count

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V	D_0 - D_3, $\overline{PL}$			0.1	mA
			$\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$			0.2	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	D_0 - D_3, $\overline{PL}$			20	µA
			$\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$			40	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V	D_0 - D_3, $\overline{PL}$			-0.4	mA
			$\overline{MR}$ input			-0.8	mA
			$\overline{CP_0}$ input			-2.4	mA
			$\overline{CP_1}$ input			-1.3	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			16	27	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS $C_L = 15pF$ Min	LIMITS $C_L = 15pF$ Max	UNIT
f_{MAX}	Maximum count frequency	Waveform 1	$\overline{CP}_0$	30		MHz
			$\overline{CP}_1$	15		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ to Q_0	Waveform 1			15 21	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_1	Waveform 1			19 35	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_2	Waveform 1			51 63	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_3	Waveform 1			78 95	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2			27 44	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to output	Waveform 3			39 45	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 4			51	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS		LIMIT Min	LIMIT Max	UNIT
t_W	Clock pulse width	Waveform 1	$\overline{CP}_0$	20		ns
			$\overline{CP}_1$	30		ns
t_W	$\overline{MR}$ pulse width	Waveform 4		15		ns
t_W	$\overline{PL}$ pulse width	Waveform 3		20		ns
$t_s(H)$	Setup time High data to $\overline{PL}$	Waveform 5		10		ns
$t_h(H)$	Hold time High data to $\overline{PL}$	Waveform 5		20		ns
$t_s(L)$	Setup time Low data to $\overline{PL}$	Waveform 5		15		ns
$t_h(L)$	Hold time Low data to $\overline{PL}$	Waveform 5		20		ns
t_{rec}	Recovery time, $\overline{MR}$ to $\overline{CP}$	Waveform 4		30		ns
t_{rec}	Recovery time, $\overline{PL}$ to $\overline{CP}$	Waveform 3		30		ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[5]

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS $C_L = 50pF$ Min	LIMITS $C_L = 50pF$ Max	UNIT
f_{MAX}	Maximum count frequency	Waveform 1	$\overline{CP}_0$	30		MHz
			$\overline{CP}_1$	15		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ to Q_0	Waveform 1			20 26	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_1	Waveform 1			24 40	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_2	Waveform 1			56 68	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_3	Waveform 1			83 100	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2			32 49	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to output	Waveform 3			44 50	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 4			56	ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[5]

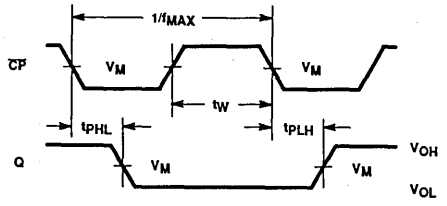
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS $C_L = 50pF$ Min	LIMITS $C_L = 50pF$ Max	UNIT
f_{MAX}	Maximum count frequency	Waveform 1	$\overline{CP}_0$	30		MHz
			$\overline{CP}_1$	15		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ to Q_0	Waveform 1			26 34	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_1	Waveform 1			31 52	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_2	Waveform 1			73 88	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_3	Waveform 1			108 130	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2			42 64	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to output	Waveform 3			57 65	ns ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 4			73	ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

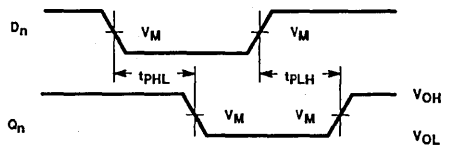
SYMBOL	PARAMETER	TEST CONDITIONS		LIMIT		UNIT
				Min	Max	
t_W	Clock pulse width	Waveform 1	$\overline{CP}_0$	20		ns
			$\overline{CP}_1$	30		ns
t_W	$\overline{MR}$ pulse width	Waveform 4		20		ns
t_W	$\overline{PL}$ pulse width	Waveform 3		20		ns
t_s(H)	Setup time High data to $\overline{PL}$	Waveform 5		10		ns
t_h(H)	Hold time High data to $\overline{PL}$	Waveform 5		20		ns
t_s(L)	Setup time Low data to $\overline{PL}$	Waveform 5		15		ns
t_h(L))	Hold time Low data to $\overline{PL}$	Waveform 5		20		ns
t_{rec}	Recovery time, $\overline{MR}$ to $\overline{CP}$	Waveform 4		30		ns
t_{rec}	Recovery time, $\overline{PL}$ to $\overline{CP}$	Waveform 3		30		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.
5. These parameters are guaranteed, but not tested.

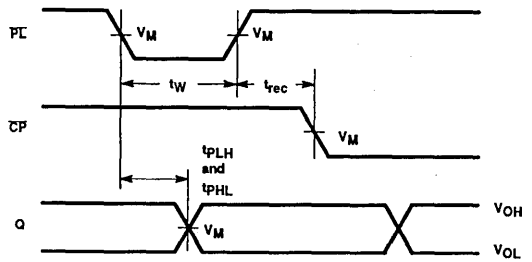
AC WAVEFORMS



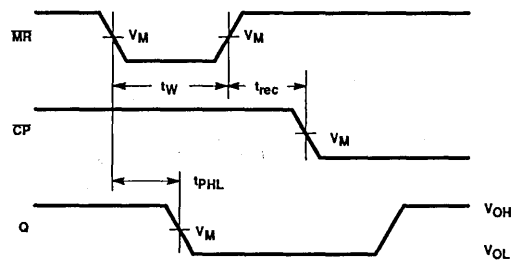
Waveform 1. Clock to Output Delays and Clock Pulse Width



Waveform 2. Parallel Data to Output Delays

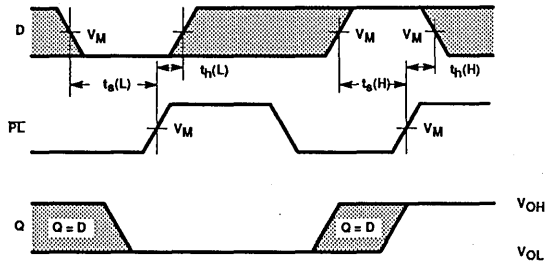


Waveform 3. Parallel Load Pulse Width, Parallel Load to Output Delay and Parallel Load to Clock Recovery Time



Waveform 4. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

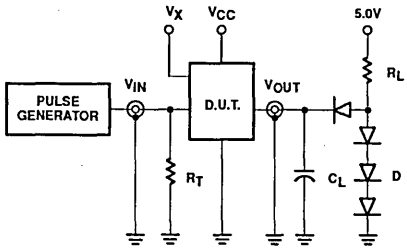
AC WAVEFORMS (Continued)



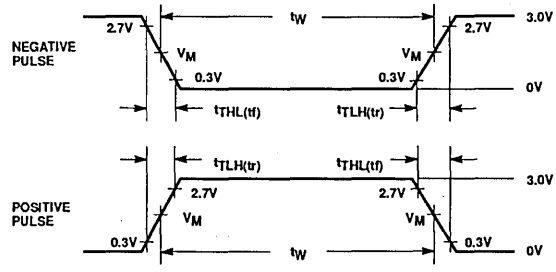
Waveform 5. Data Setup and Hold Times

NOTE: For all waveforms, V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS240, 54LS241, 54S240, 54S241

Buffers

'240 Octal Inverter Buffer (3-State)
'241 Octal Buffer (3-State)
Product Specification

FUNCTION TABLE '240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z)= High impedance (off) state

FUNCTION TABLE '241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z)= High impedance (off) state

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54LS240/BRA 54S240/BRA 54LS241/BRA 54S241/BRA
20-Pin Ceramic FlatPack	54LS240/BSA 54S240/BSA 54LS241/BSA 54S241/BSA
20-Pin Ceramic LLCC	54LS240/B2A 54S240/B2A 54LS241/B2A 54LS241/B2A

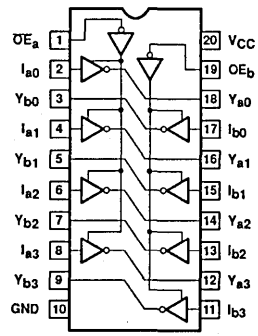
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S	54LS
I_{a0} - I_{a3}, I_{b0} - I_{b3}	Inputs	1SUL	1LSUL
$\overline{OE}_a$, $\overline{OE}_b$, OE_b	Inputs	1SUL	1LSUL
All	Outputs	24SUL	32LSUL

NOTE: A 54S Unit Load (SUL) is 50μA I_{IH}, and -2.0mA I_{IL} and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION

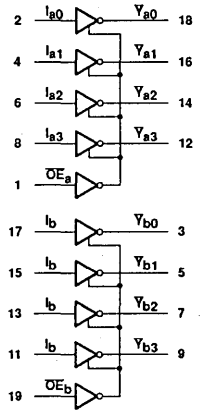
'240



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

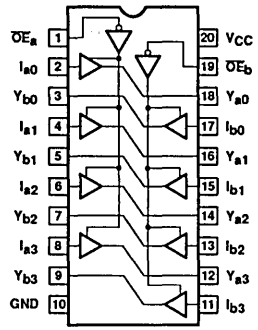
'240



For LLCC pin assignments, see JEDEC Standard No. 2

PIN CONFIGURATION

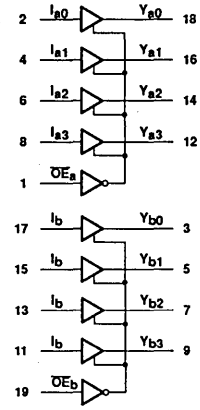
'241



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

'241



For LLCC pin assignments, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +5.5	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.7			+0.8	V
	+125°C			+0.7			+0.7	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-12			-12	mA
I_{OL}	Low-level output current			12			48	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			54LS240, 241			54S240, 241			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)[6]	V_{CC} = Min			0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max			2.0			2.0			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = -3mA			2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max					0.4			0.55	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5			-1.2	V
I_{OZH}	Offstate output current,	V_{CC} = Max, V_{IH} = Min,	V_O = 2.4V							50	µA
	High-level voltage applied	V_{IL} = Max	V_O = 2.7V				20				µA
I_{OZL}	Offstate output current,	V_{CC} = Max, V_{IH} = Min,	V_O = 2.4V				-20				µA
	Low-level voltage applied	V_{IL} = Max	V_O = 0.5V							-50	µA
I_{IH2}	Input current at maximum	V_{CC} = Max	V_I = 5.5V							1.0	mA
	input voltage		V_I = 7.0V				0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V					20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V				-0.2				mA
			V_I = 0.5V	$I_{a0} - I_{a3}$, $I_{b0} - I_{b3}$ inputs						-400	µA
				$\overline{OE_a}$, $\overline{OE_b}$, OE_b inputs						-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-40		-130	-80		-180	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	I_{CCH}	'LS240		17	27				mA
			I_{CCL}			26	44				mA
			I_{CCZ}			29	60				mA
			I_{CCH}	'LS241		17	27				mA
			I_{CCL}			27	46				mA
			I_{CCZ}			32	54				mA
			I_{CCH}	'S240					80	123	mA
			I_{CCL}						100	145	mA
			I_{CCZ}						100	145	mA
			I_{CCH}	'S241					95	147	mA
			I_{CCL}						120	170	mA
			I_{CCZ}						120	170	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

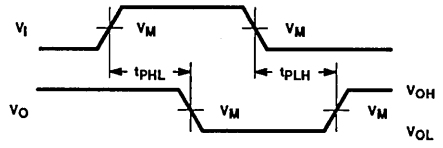
SYMBOL	PARAMETER	TEST CONDITIONS		54LS		54S		UNIT
				$C_L = 50pF$		$C_L = 50pF$		
				Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '240			14 18		7 7	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '241			18 18		9 9	ns ns
t_{PZH}	Enable to High	Waveform 3	LS		30			ns
			'S240				10	ns
			'S241				12	ns
t_{PZL}	Enable to Low	Waveform 4			30		15	ns
t_{PHZ}	Disable from High	Waveform 3, $C_L = 5pF$[5]			18		9	ns
t_{PLZ}	Disable from Low	Waveform 4, $C_L = 5pF$[5]			25		15	ns
t_{PHZ}	Disable from High	Waveform 3, $C_L = 50pF$			34		14	ns
t_{PLZ}	Disable from Low	Waveform 4, $C_L = 50pF$			27		16.5	ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[6]

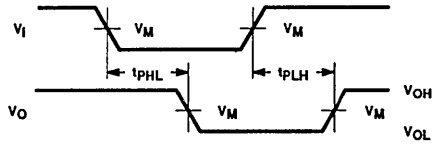
SYMBOL	PARAMETER	TEST CONDITIONS		54LS		54S		UNIT
				$C_L = 50pF$		$C_L = 50pF$		
				Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '240			18 23		9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '241			23 23		16 12	ns ns
t_{PZH}	Enable to High	Waveform 3	LS		39			ns
			'S240				13	ns
			'S241				20	ns
t_{PZL}	Enable to Low	Waveform 4			39		20	ns
t_{PHZ}	Disable from High	Waveform 3, $C_L = 5pF$[5]			23		12	ns
t_{PLZ}	Disable from Low	Waveform 4, $C_L = 5pF$[5]			33		20	ns
t_{PHZ}	Disable from High	Waveform 3, $C_L = 50pF$			44		18	ns
t_{PLZ}	Disable from Low	Waveform 4, $C_L = 50pF$			35		22	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open.
5. Guaranteed by 50pF limits, but not tested.
6. These parameters are guaranteed, but not tested.

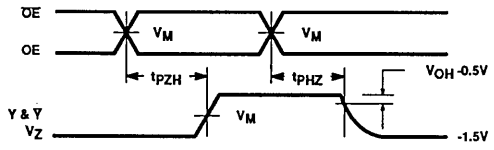
AC WAVEFORMS



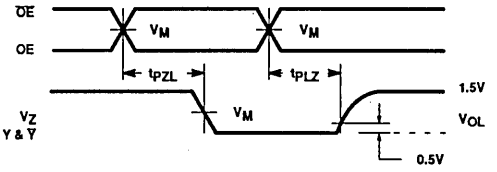
Waveform 1. Waveform for Inverting Outputs



Waveform 2. Waveform for Non-Inverting Outputs



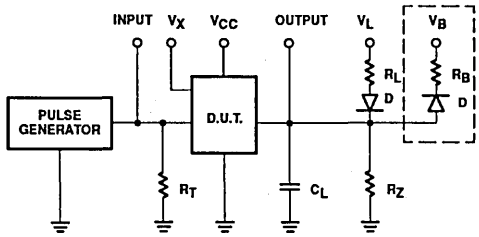
Waveform 3. 3-State Enable Time to High Level and Disable Time from High Level



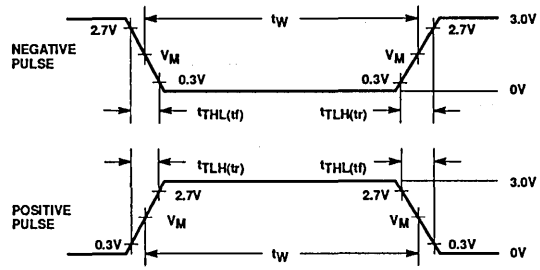
Waveform 4. 3-State Enable Time to Low Level and Disable Time from Low Level

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V
54SXXX	1.5V	0.7V	2.0V	1.65V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	82Ω	560Ω	2.5V	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS244, 54S244
Buffers

Octal Buffers (3-State)

Product Specification

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54LS244/BRA, 54S244/BRA
20-Pin Ceramic Flat Pack	54LS244/BSA, 54S244/BSA
20-Pin Ceramic LLCC	54LS244/B2A, 54S244/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

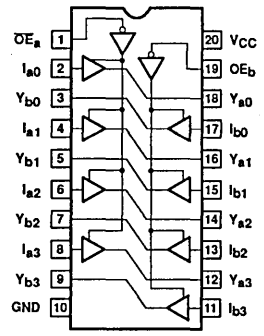
PINS	DESCRIPTION	54S	54LS
All	Inputs	1SUL	1LSUL
All	Output	24SUL	30LSUL

NOTE: A 54S Unit Load (SUL) is a 50μA I_{IH}, and -2.0mA I_{IL}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

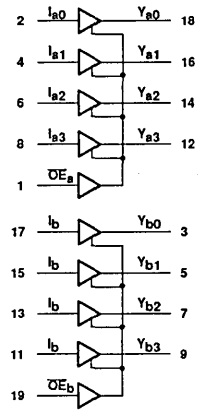
SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.7			+0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-12			-12	mA
I_{OL}	Low-level output current			12			48	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			54LS240, 241			54S240, 241			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)[5]	V_{CC} = Min			0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max			2.0			2.0			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = -3mA			2.4	3.4		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max					0.4			0.55	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5			-1.2	V
I_{OZH}	Offstate output current,	V_{CC} = Max, V_{IH} = Min,		V_O = 2.7V			20				µA
	High-level voltage applied	V_{IL} = Max		V_O = 2.4V						50	µA
I_{OZL}	Offstate output current,	V_{CC} = Max, V_{IH} = Min,		V_O = 0.4V			-20				µA
	Low-level voltage applied	V_{IL} = Max		V_O = 0.5V						-50	µA
I_{IH2}	Input current at maximum	V_{CC} = Max		V_I = 5.5V						1.0	mA
	input voltage			V_I = 7.0V			0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V					20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V				-0.2				mA
			V_I = 0.5V	$\overline{OE}$ inputs						-2.0	mA
				Other inputs						-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-40		-130	-80		-180	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	I_{CCH}	Outputs High		17	27		95	147	mA
			I_{CCL}	Outputs Low		27	46		120	170	mA
			I_{CCZ}	Outputs Off		32	54		120	170	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

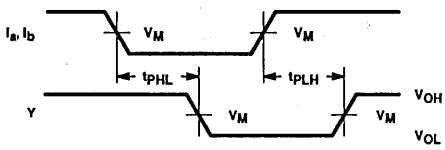
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			$C_L = 50pF$		$C_L = 50pF$		
			Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1		18		9	ns
t_{PHL}	Propagation delay	Waveform 1		18		9	ns
t_{PZH}	Enable to High	Waveform 2		23		12	ns
t_{PZL}	Enable to Low	Waveform 3		30		15	ns
t_{PHZ}	Disable from High	Waveform 2, $C_L = 5pF$[6]		18		9	ns
t_{PLZ}	Disable from Low	Waveform 3, $C_L = 5pF$[6]		25		15	ns
t_{PHZ}	Disable from High	Waveform 2, $C_L = 50pF$		34		14	ns
t_{PLZ}	Disable from Low	Waveform 3, $C_L = 50pF$		27		16.5	ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[5]

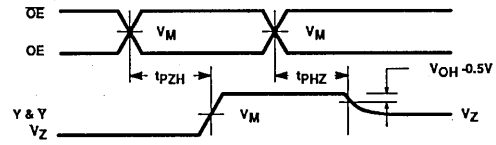
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			$C_L = 50pF$		$C_L = 50pF$		
			Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1		23		16	ns
t_{PHL}	Propagation delay	Waveform 1		23		12	ns
t_{PZH}	Enable to High	Waveform 2		30		16	ns
t_{PZL}	Enable to Low	Waveform 3		39		20	ns
t_{PHZ}	Disable from High	Waveform 2, $C_L = 5pF$[6]		24		12	ns
t_{PLZ}	Disable from Low	Waveform 3, $C_L = 5pF$[6]		33		20	ns
t_{PHZ}	Disable from High	Waveform 2, $C_L = 50pF$		44		18	ns
t_{PLZ}	Disable from Low	Waveform 3, $C_L = 50pF$		35		22	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open.
5. These parameters are guaranteed, but not tested.
6. Guaranteed by 50pF limits, but not tested.

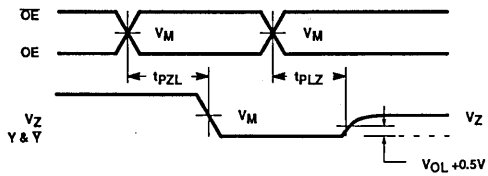
AC WAVEFORMS



Waveform 1. Waveform for Non-Inverting Outputs



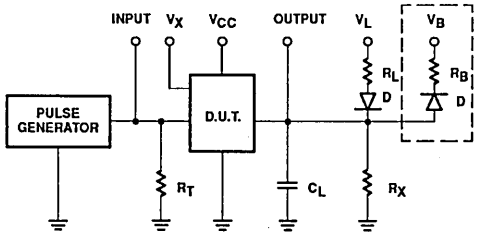
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



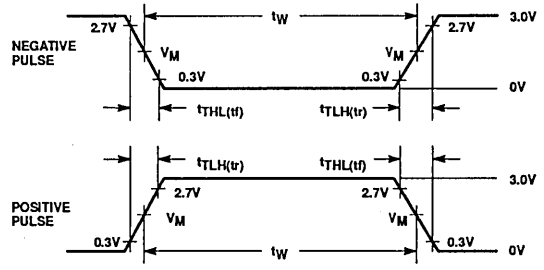
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V
54SXXX	1.5V	0.7V	2.0V	1.65V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	82Ω	560Ω	2.5V	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS245
Transceiver

Octal Transceiver (3-State)

Product Specification

FEATURES
- **Octal bidirectional bus interface**
- **3-State buffer outputs**
- **PNP inputs for reduced loading**
- **Hysteresis on all Data inputs**

DESCRIPTION
The 54LS245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 12mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable ($\overline{CE}$) input for easy cascading and a Send/Receive (S/$\overline{R}$) input for direction control. All data inputs have hysteresis built in to minimize AC noise effects.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54LS245/BRA
20-Pin Ceramic FlatPack	54LS245/BSA
20-Pin Ceramic LLCC	54LS245/B2A

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUT
L	H	INPUT	B = A
H	X	(Z)	(Z)

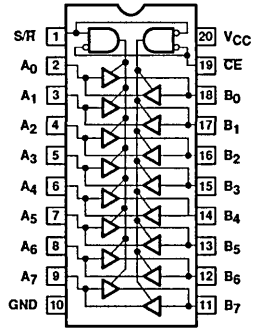
H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
All	Inputs	1LSUL
All	Outputs	30LSUL

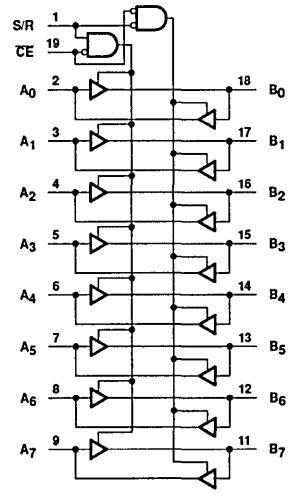
NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-12	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
ΔV_T	Hysteresis (V_{T+} - V_{T-})[5]	V_{CC} = Min			0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max			2.0			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = -3mA			2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max					0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5	V
I_{OZH}	Offstate output current, High-level voltage applied	V_{CC} = Max, V_O = 2.7V, $\overline{CE}$ = 2.0V					20	µA
I_{OZL}	Offstate output current, Low-level voltage applied	V_{CC} = Max, V_O = 0.4V, $\overline{CE}$ = 2.0V					-20	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V	A, B inputs			0.1	mA
			V_I = 7.0V	S/$\overline{R}$, $\overline{CE}$ inputs			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V					-0.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-40		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	I_{CCH}	Outputs High		48	70	mA
			I_{CCL}	Outputs Low		62	90	mA
			I_{CCZ}	Outputs Off		64	95	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

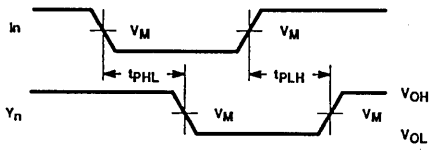
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITSS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH}	Propagation delay	Waveform 1		12	ns
t_{PHL}	Propagation delay	Waveform 1		12	ns
t_{PZH}	Enable to High	Waveform 2		40	ns
t_{PZL}	Enable to Low	Waveform 3		40	ns
t_{PHZ}	Disable from High	Waveform 2, C_L = 5pF[6]		25	ns
t_{PLZ}	Disable from Low	Waveform 3, C_L = 5pF[6]		25	ns
t_{PHZ}	Disable from High	Waveform 2, C_L = 50pF		30	ns
t_{PLZ}	Disable from Low	Waveform 3, C_L = 50pF		27	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[5]

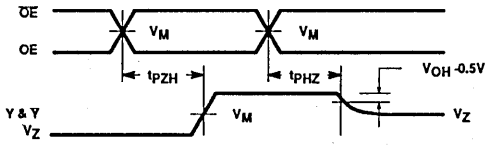
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITSS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH}	Propagation delay	Waveform 1		16	ns
t_{PHL}	Propagation delay	Waveform 1		16	ns
t_{PZH}	Enable to High	Waveform 2		52	ns
t_{PZL}	Enable to Low	Waveform 3		52	ns
t_{PHZ}	Disable from High	Waveform 2, C_L = 5pF[6]		33	ns
t_{PLZ}	Disable from Low	Waveform 3, C_L = 5pF[6]		33	ns
t_{PHZ}	Disable from High	Waveform 2, C_L = 50pF		39	ns
t_{PLZ}	Disable from Low	Waveform 3, C_L = 50pF		35	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open.
5. These parameters are guaranteed, but not tested.
6. Guaranteed by the 50pF limits, but not tested.

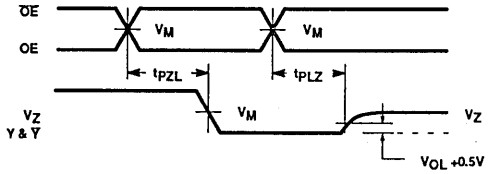
AC WAVEFORMS



Waveform 1. Waveform for Non-Inverting Outputs



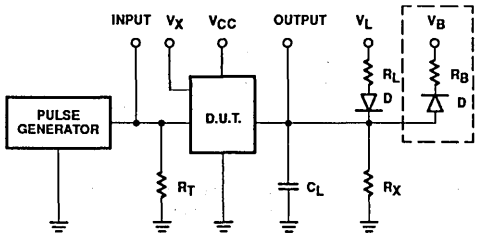
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



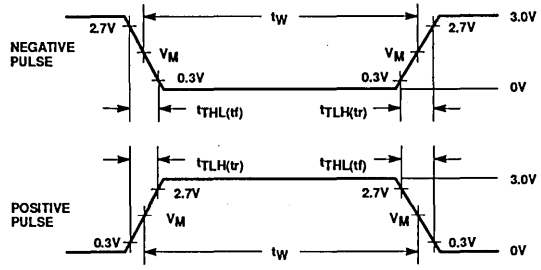
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54S251
Multiplexer

8-Input Multiplexer (3-State)

Product Specification

FEATURES

- **High-speed 8-to-1 multiplexing**
- **True and complement outputs**
- **Both outputs are 3-State for further multiplexer expansion**
- **3-State outputs are buffer type**

DESCRIPTION

The 54S251 is a logical implementation of a single-pole, 8-position switch with the state of three Select inputs (S_0, S_1, S_2) controlling the switch position. Assertion (Y) and Negation ($\overline{Y}$) outputs are both provided. The Output Enable input ($\overline{OE}$) is active Low. The logic function provided at the output, when activated, is:

$$Y = \overline{OE} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

Both outputs are in the High impedance (Hi-Z) state when the output enable is High, allowing multiplexer expansion by tying the outputs of up to 128 devices together. All but one device must be in the High impedance state to avoid high currents that would exceed the maximum ratings, when the outputs of the 3-State devices are tied together. Design of the output enable signals must ensure there is no overlap in the active Low portion of the enable voltages.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54S251/BEA
16-Pin Ceramic FlatPack	54S251/BFA
20-Pin Ceramic LLCC	54S251/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

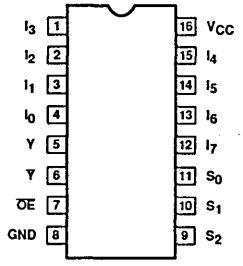
PINS	DESCRIPTION	54S
All	Inputs	1SUL
All	Outputs	10SUL

NOTE: A 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

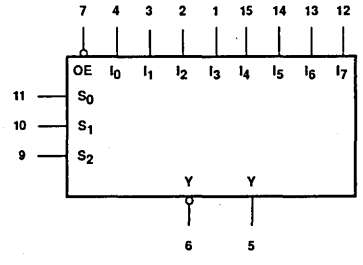
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



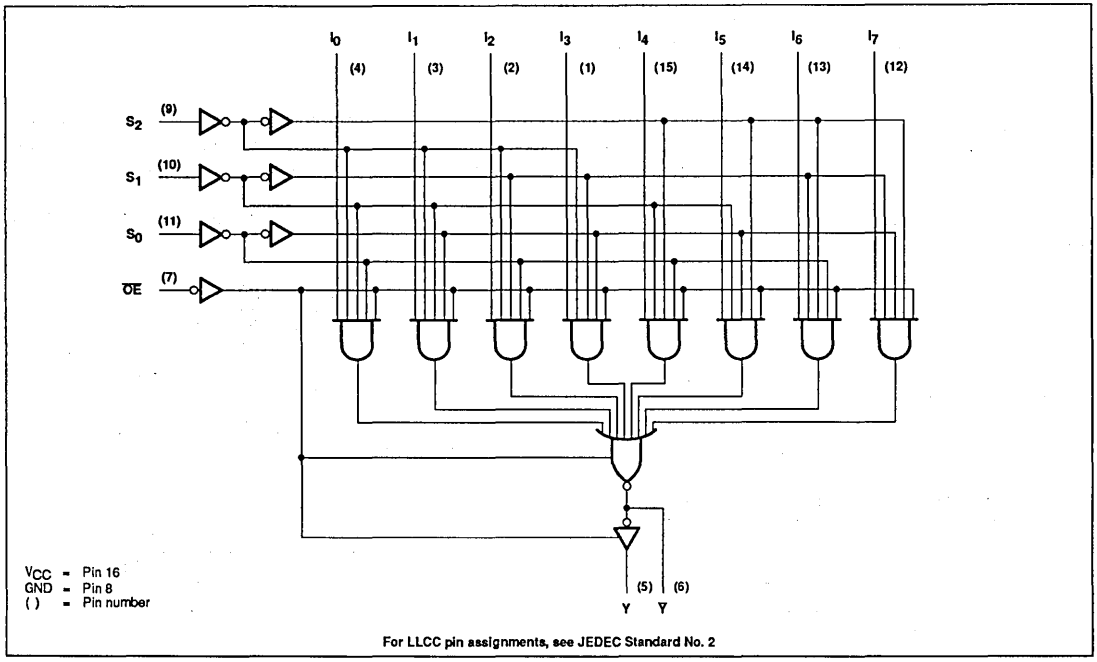
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
	+125°C			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.0	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,				0.5	V
		I_{OL} = Max	+125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.4V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V				-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-40		-110	mA
I_{CC}	Supply current (total)	V_{CC} = Max	Outputs Low				mA
			Outputs High			85	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to Y output	Waveform 2		18 19.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to $\overline{Y}$ output	Waveform 1		15 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Y output	Waveform 2		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Y}$ output	Waveform 1		7.0 7.0	ns ns
t_{PZH}	Output enable to High level	Waveform 3 – C_L = 50pF		19.5	ns
t_{PZL}	Output enable to Low level	Waveform 4 – C_L = 50pF		21	ns
t_{PHZ}	Output disable from High level	Waveform 3 – C_L = 5pF[5]		8.5	ns
t_{PLZ}	Output disable from Low level	Waveform 4 – C_L = 5pF[5]		14	ns
t_{PHZ}	Output disable from High level	Waveform 3 – C_L = 50pF		13.5	ns
t_{PLZ}	Output disable from Low level	Waveform 4 – C_L = 50pF		15.5	ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[6]

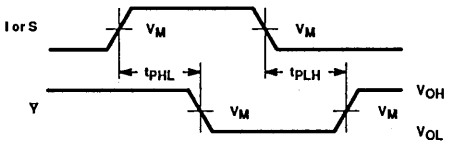
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to Y output	Waveform 2		20.0 21.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to $\overline{Y}$ output	Waveform 1		17.0 15.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Y output	Waveform 2		14.0 14.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Y}$ output	Waveform 1		9.0 9.0	ns ns
t_{PZH}	Output enable to High level	Waveform 3 – C_L = 50pF		19.5	ns
t_{PZL}	Output enable to Low level	Waveform 4 – C_L = 50pF		21.0	ns
t_{PHZ}	Output disable from High level	Waveform 3 – C_L = 5pF[5]		11.0	ns
t_{PLZ}	Output disable from Low level	Waveform 4 – C_L = 5pF[5]		16.5	ns
t_{PHZ}	Output disable from High level	Waveform 3 – C_L = 50pF		21.0	ns
t_{PLZ}	Output disable from Low level	Waveform 4 – C_L = 50pF		17.0	ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[6]

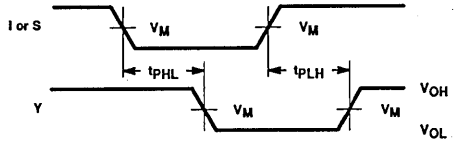
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to Y output	Waveform 2		26 28	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to $\overline{Y}$ output	Waveform 1		22 20	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to Y output	Waveform 2		18 18	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Y}$ output	Waveform 1		11.5 11.5	ns ns
t_{PZH}	Output enable to High level	Waveform 3 – C_L = 50pF		25.5	ns
t_{PZL}	Output enable to Low level	Waveform 4 – C_L = 50pF		27.5	ns
t_{PHZ}	Output disable from High level	Waveform 3 – C_L = 5pF[5]		14	ns
t_{PLZ}	Output disable from Low level	Waveform 4 – C_L = 5pF[5]		22	ns
t_{PHZ}	Output disable from High level	Waveform 3 – C_L = 50pF		24	ns
t_{PLZ}	Output disable from Low level	Waveform 4 – C_L = 50pF		22	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs $\geq 4.0V$ and all inputs open.
5. Guaranteed by the 50pF limits, but not tested.
6. These parameters are guaranteed, but not tested.

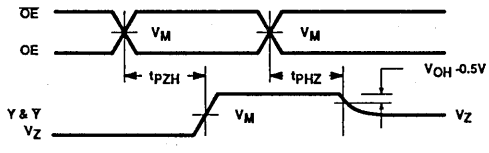
AC WAVEFORMS



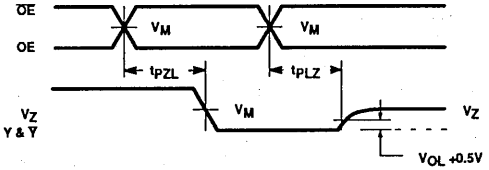
Waveform 1. Waveform for Inverting Outputs



Waveform 2. Waveform for Non-Inverting Outputs



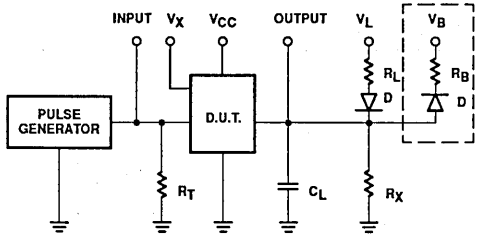
Waveform 3. 3-State Enable Time to High Level and Disable Time from High Level



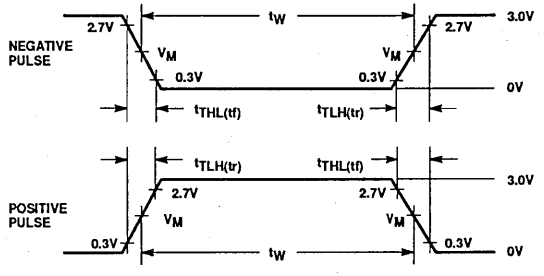
Waveform 4. 3-State Enable Time to Low Level and Disable Time from Low Level

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54SXXX	1.5V	0.7V	2.0V	1.65V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R1	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	82Ω	560Ω	2.5V	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54S253
Multiplexer

Dual 4-Input Multiplexer (3-State)

Product Specification

Military Logic Products

FEATURES

- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable inputs**

DESCRIPTION

The 54S253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are High, the outputs are forced to a High impedance (Hi-Z) state.

The 54S253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs. Logic equations for the outputs are shown below:

$$Y_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} V \overline{S}_1 \cdot S_0 + 1_{2a} \cdot S_1 \cdot + I_{3a} \cdot S_1 S_0)$$

$$Y_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 S_0)$$

All but one device must be in the High impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

ORDERING INFORMATION

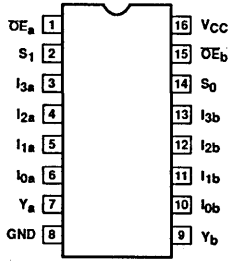
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54S253/BEA
16-Pin Ceramic FlatPack	54S253/BFA
20-Pin Ceramic LLCC	54S253/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S
All	Inputs	1SUL
All	Outputs	10SUL

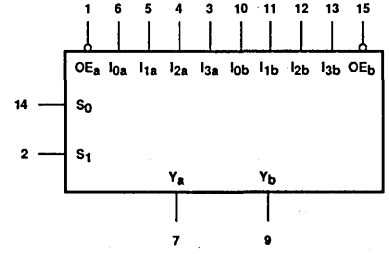
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

PIN CONFIGURATION



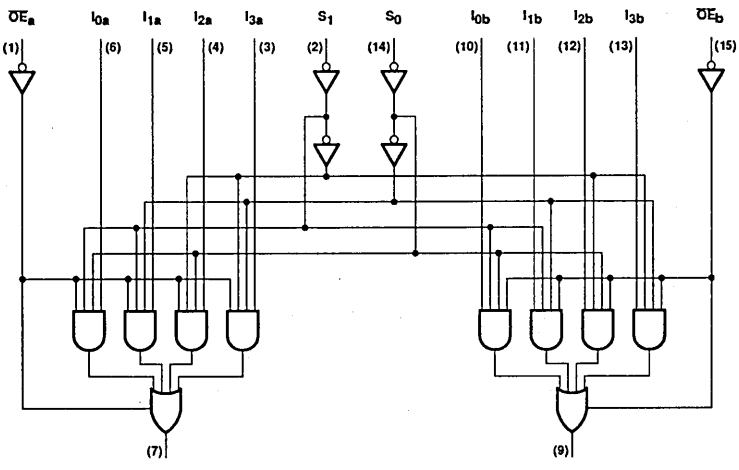
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC Pin Assignment, See JEDEC Standard No. 2

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
	+125°C			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.0	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,				0.5	V
		I_{OL} = Max	+125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.4V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V				-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-40		-110	mA
I_{CCH}	Supply current[4] (total)	V_{CC} = Max	Condition 1			70	mA
I_{CCL}	Supply current[4] (total)	V_{CC} = Max	Condition 2			80	mA
I_{CCZ}	Supply current[4] (total)	V_{CC} = Max	Condition 3			100	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		18 18	ns ns
t_{PZH}	Output enable to High level	Waveform 2		13	ns
t_{PZL}	Output enable to Low level	Waveform 3		14	ns
t_{PHZ}	Output disable from High level	Waveform 2 – C_L = 5pF[5]		8.5	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – C_L = 5pF[5]		14	ns
t_{PHZ}	Output disable from High level	Waveform 2 – C_L = 50pF		13.5	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – C_L = 50pF		15.5	ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[6]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		11.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		20.5 20.5	ns ns
t_{PZH}	Output enable to High level	Waveform 2		15.5	ns
t_{PZL}	Output enable to Low level	Waveform 3		16.5	ns
t_{PHZ}	Output disable from High level	Waveform 2 – $C_L = 5pF$[5]		8.5	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – $C_L = 5pF$[5]		14	ns
t_{PHZ}	Output disable from High level	Waveform 2 – $C_L = 50pF$		13.5	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – $C_L = 50pF$		15.5	ns

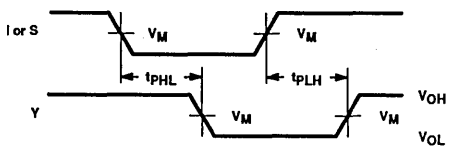
AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[6]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		15 15	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		27 27	ns ns
t_{PZH}	Output enable to High level	Waveform 2		20	ns
t_{PZL}	Output enable to Low level	Waveform 3		21	ns
t_{PHZ}	Output disable from High level	Waveform 2 – $C_L = 5pF$[5]		11	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – $C_L = 5pF$[5]		18	ns
t_{PHZ}	Output disable from High level	Waveform 2 – $C_L = 50pF$		18	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – $C_L = 50pF$		20	ns

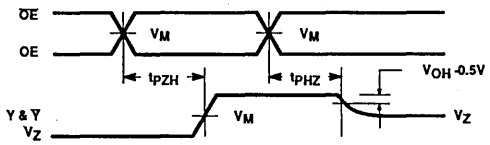
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured under the following conditions with the outputs open: *Condition* 1: All inputs grounded. *Condition* 2: All inputs at $\geq 4.0V$ except $\overline{OE}$ which is grounded. *Condition* 3: $\overline{OE} \geq 4.0V$ all inputs grounded.
5. Guaranteed by the 50pF limits, but not tested.
6. These parameters are guaranteed, but not tested.

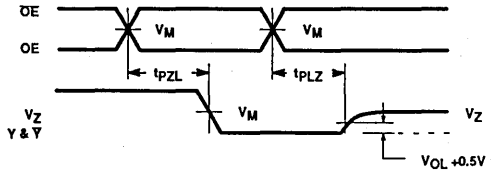
AC WAVEFORMS



Waveform 1. Waveform for Non-Inverting Outputs



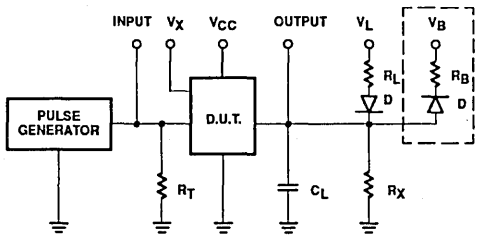
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



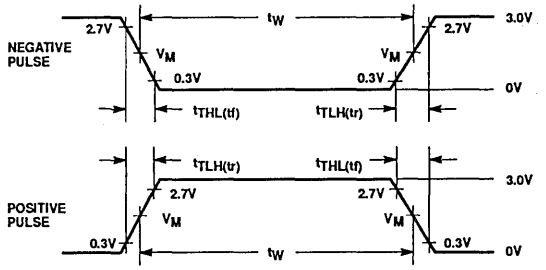
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54SXXX	1.5V	0.7V	2.0V	1.65V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	82Ω	560Ω	2.5V	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54LS257A
Data Selector/Multiplexer

Quad 2-Line to 1-Line Data Selector/Multiplexer (3-State)

Product Specification

Military Logic Products

FEATURES
- **Multifunction capability**
- **Non-inverting data path**
- **3-State outputs**

DESCRIPTION
The 54LS257 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is Low and the I_1 inputs are selected when the Select input is High. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The 54LS257A is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a High impedance "off" state when the Output Enable input ($\overline{OE}$) is High. All but one device must be in the High impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

ORDERING INFORMATION

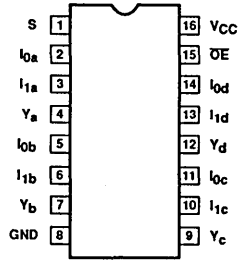
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS257A/BEA
16-Pin Ceramic FlatPack	54LS257A/BFA
20-Pin Ceramic LLCC	54LS257A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
S	Inputs	2LSUL
Other	Inputs	1LSUL
All	Outputs	30LSUL

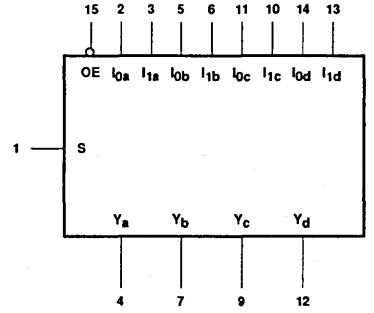
NOTE: A 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

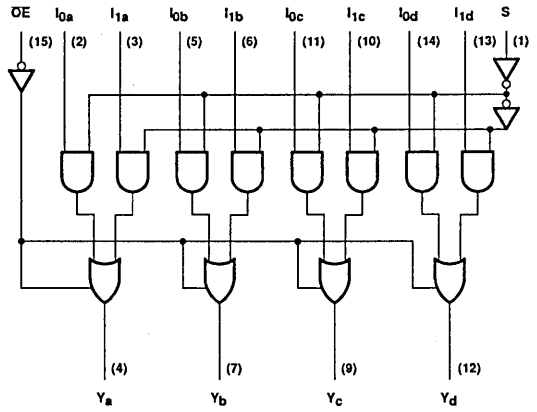
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

Data Selector/Multiplexer | 54LS257A

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{OZH}	Offstate output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				20	µA
I_{OZL}	Offstate output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.4V				-20	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V	S input			0.2	mA
			Other inputs			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	S input			40	µA
			Other inputs			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V	S input			-0.8	mA
			Other inputs			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-30		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	I_{CCH} Outputs High		6.2	10	mA
			I_{CCL} Outputs Low		10	16	mA
			I_{CCZ} Outputs Off		12	19	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

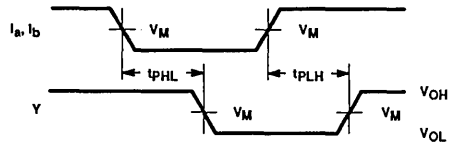
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		18 18	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		21 21	ns
t_{PZH}	Output enable to High level	Waveform 2		30	ns
t_{PZL}	Output enable to Low level	Waveform 3		30	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 5pF[5]		30	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 5pF[5]		25	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 50pF		46	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 50pF		27	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[6]

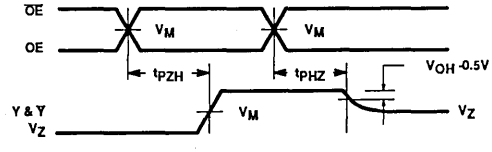
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		23 23	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		27 27	ns
t_{PZH}	Output enable to High level	Waveform 2		39	ns
t_{PZL}	Output enable to Low level	Waveform 3		39	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 5pF[5]		39	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 5pF[5]		33	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 50pF		60	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 50pF		35	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all outputs open and all possible inputs grounded while achieving the stated output conditions.
5. Guaranteed by the 50pF limits, but not tested.
6. These parameters are guaranteed, but not tested.

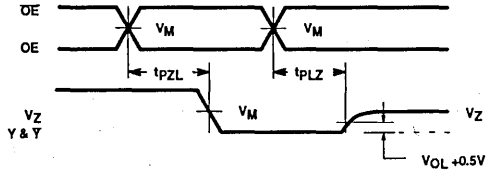
AC WAVEFORMS



Waveform 1. Waveform for Non-Inverting Outputs



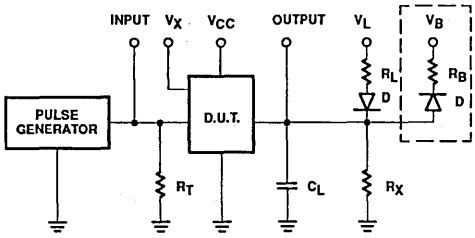
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



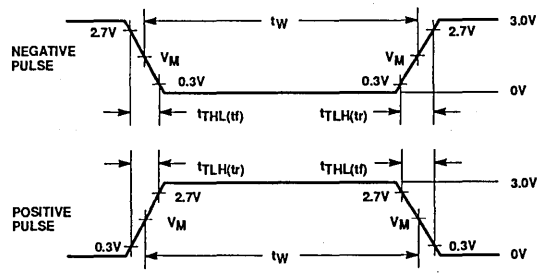
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

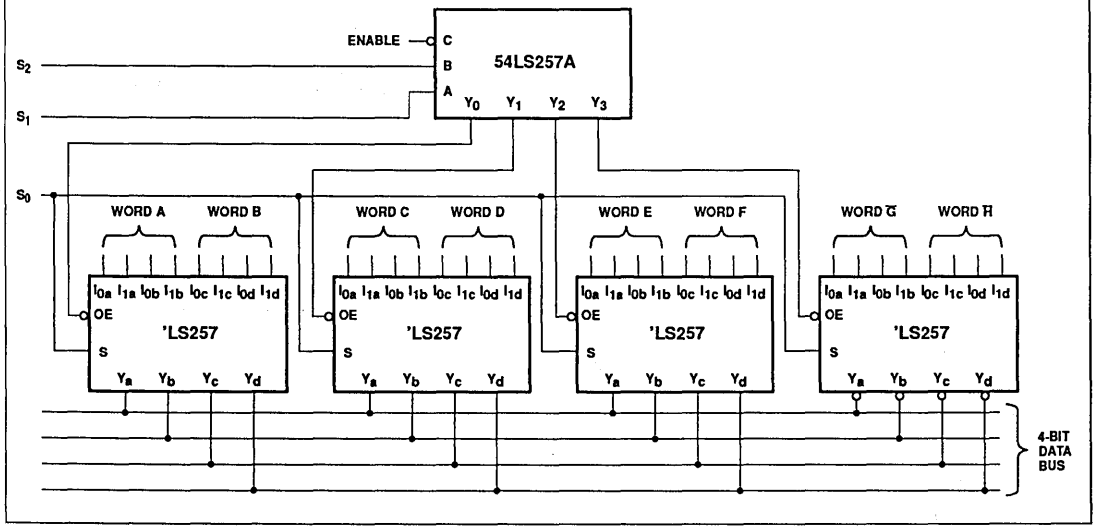
FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

APPLICATION DIAGRAM



Signetics

54LS258A
Data Selector/Multiplexer

Quad 2-Line to 1-Line Data Selector/Multiplexer (3-State)

Product Specification

Military Logic Products

FEATURES
- **Multifunction capability**
- **Inverting data path**
- **3-State outputs**
- **See 54LS257 for non-inverting version**

DESCRIPTION
The 54LS258A has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is Low and the I_1 inputs are selected when the Select input is High. Data appears at the outputs in inverted (complementary) form.

The 54LS258A is the logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a High impedance "off" state when the Output Enable input ($\overline{OE}$) is High. All but one device must be in the High impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-State devices are tied together.

ORDERING INFORMATION

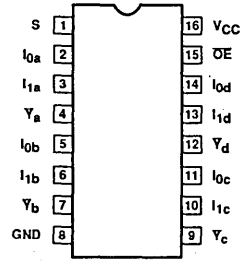
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS258A/BEA
16-Pin Ceramic FlatPack	54LS258A/BFA
20-Pin Ceramic LLCC	54LS258A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
S	Inputs	2LSUL
Other	Inputs	1LSUL
All	Outputs	30LSUL

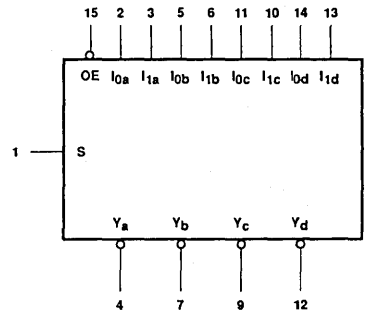
NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

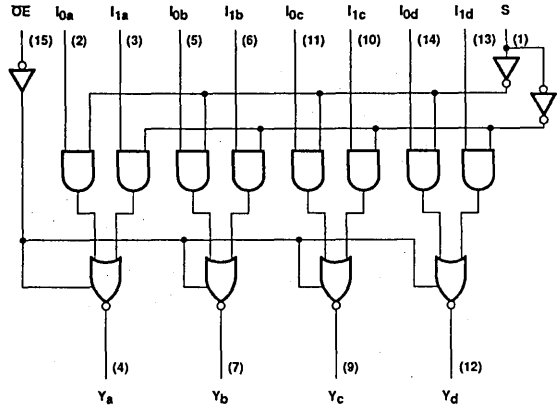
LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

Data Selector/Multiplexer | 54LS258A

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

Data Selector/Multiplexer | 54LS258A

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{OZH}	Offstate output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				20	µA
I_{OZL}	Offstate output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.4V				-20	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V	S input			0.2	mA
			Other inputs			0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	S input			40	µA
			Other inputs			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V	S input			-0.8	mA
			Other inputs			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-30		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	I_{CCH} Outputs High		4	7	mA
			I_{CCL} Outputs Low		8.8	14	mA
			I_{CCZ} Outputs Off		12	19	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4		18 18	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1 & 4		21 21	ns
t_{PZH}	Output enable to High level	Waveform 2		30	ns
t_{PZL}	Output enable to Low level	Waveform 3		30	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 5pF[5]		30	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 5pF[5]		25	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 50pF		46	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 50pF		27	ns

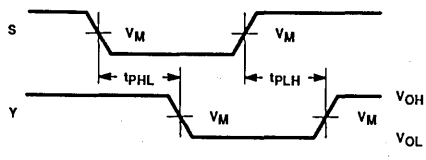
Data Selector/Multiplexer | 54LS258A

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[6]

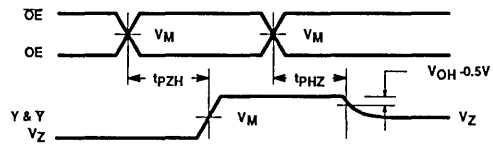
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4		23 23	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1 & 4		27 27	ns
t_{PZH}	Output enable to High level	Waveform 2		39	ns
t_{PZL}	Output enable to Low level	Waveform 3		39	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 5pF[5]		39	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 5pF[5]		33	ns
t_{PHZ}	Output disable from High level	Waveform 2, C_L = 50pF		60	ns
t_{PLZ}	Output disable from Low level	Waveform 3, C_L = 50pF		35	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all outputs open and all possible inputs grounded while achieving the stated output conditions.
5. Guaranteed by the 50pF limits, but not tested.
6. These parameters are guaranteed, but not tested.

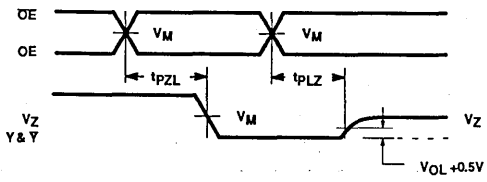
AC WAVEFORMS



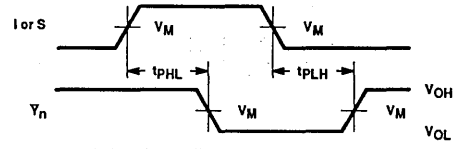
Waveform 1. Waveform for Non-Inverting Outputs



Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



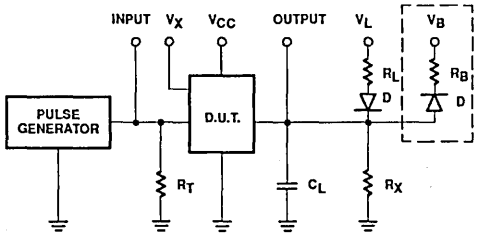
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level



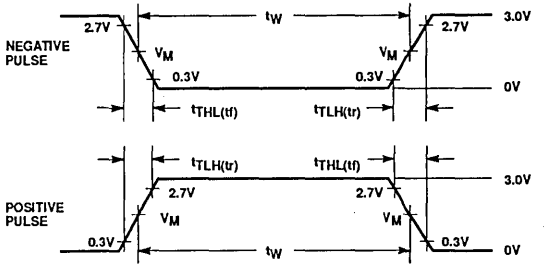
Waveform 4. Waveform for Inverting Outputs

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS273, 54S273
Flip-Flops

Octal D Flip-Flops

Product Specification

FEATURES

- **Ideal buffer for MOS microprocessor or memory**
- **Eight edge-triggered D flip-flops**
- **High-speed Schottky version available**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**
- **Slim 20-pin plastic and ceramic DIP packages**
- **See '377 for Clock Enable version**
- **See '373 for transparent latch version**
- **See '374 for 3-State version**

DESCRIPTION

The '273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

ORDERING INFORMATION

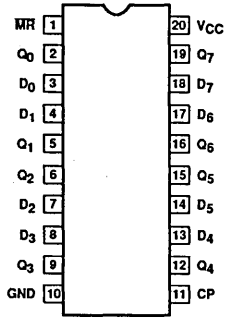
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54LS273/BRA 54S273/BRA
20-Pin Ceramic FlatPack	54LS273/BSA 54S273/BSA
20-Pin Ceramic LLCC	54LS273/B2A 54S273/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S	54LS
All	Inputs	1SUL	1LSUL
All	Outputs	10SUL	10LSUL

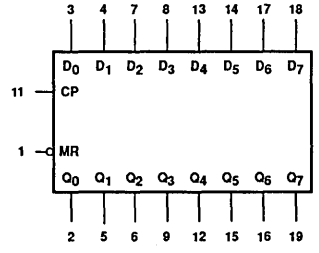
NOTE: A 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL} and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC Pin Assignments, see JEDEC Standard No. 2

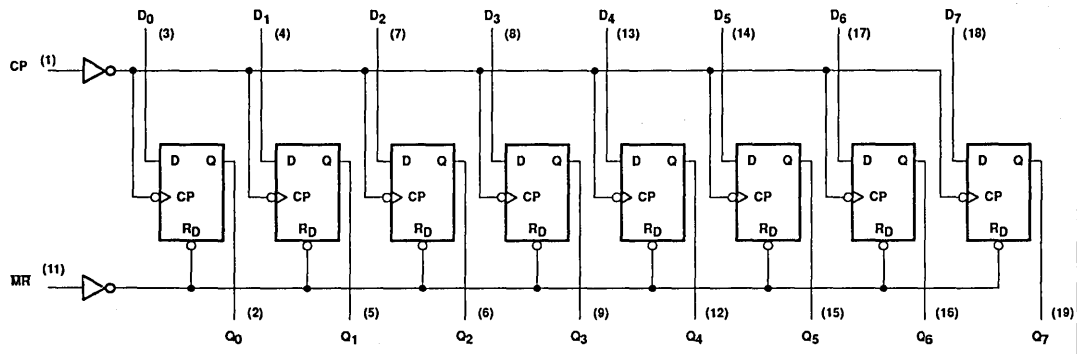
LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

For LLCC Pin Assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



V_{CC} = Pin 20
GND = Pin 10
( ) = Pin number

For LLCC pin assignments, see JEDEC Standard No. 2

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = High voltage level steady state.
h = High voltage level one setup time prior to the Low-to-High Clock transition.
L = Low voltage level steady state.
l = Low voltage level one setup time prior to the Low-to-High Clock transition.
X = Don't Care.
↑ = Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +5.5	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		54LS			54S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			2.0			V
V_{IL}	Low-level input voltage				+0.7			+0.8	V
		+125°C			+0.7			+0.7	V
I_{IK}	Input clamp current				-18			-18	mA
I_{OH}	High-level output current				-400			-1000	µA
I_{OL}	Low-level output current				4			20	mA
T_A	Operating free-air temperature range		-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54LS273			54S273			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		2.5			V
V_O	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,			0.25	0.4			0.5	V
		I_{OL} = Max	+125°C			0.4			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.2	V
I_{IH2}	Input current at maximum	V_{CC} = Max	V_I = 5.5V						1.0	mA
	input voltage		V_I = 7.0V			0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V			-0.4				mA
			V_I = 0.5V						-2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	-40		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			17	27		109	150	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 27		15 15	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		27		15	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_W(L)$	Clock pulse width (Low)	Waveform 1	20		7.0		ns
t_W	Master Reset pulse width	Waveform 2	20		10		ns
$t_s(H)$	Setup time, High data to CP	Waveform 3	20		5.0		ns
$t_h(H)$	Hold time, High data to CP	Waveform 3	5.0		3.0		ns
$t_s(L)$	Setup time, Low data to CP	Waveform 3	20		5.0		ns
$t_h(L)$	Hold time, Low data to CP	Waveform 3	5.0		3.0		ns
t_{rec}	Recovery time, MR to CP	Waveform 2	25		5.0		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		32 32		17.5 17.5	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		32		17.5	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

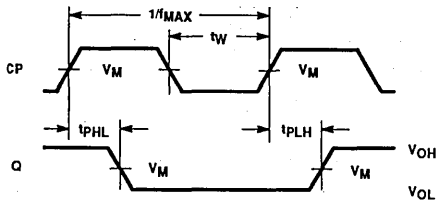
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		42 42		23 23	ns ns
t_{PLH}	Propagation delay $\overline{MR}$ to output	Waveform 2		42		23	ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

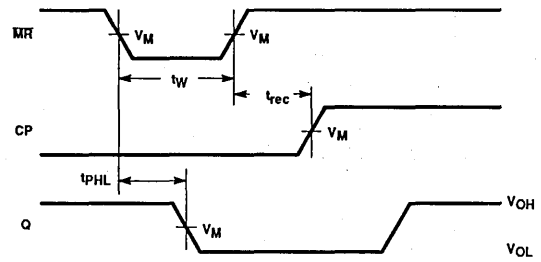
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_W(L)$	Clock pulse width (Low)	Waveform 1	20		7.0		ns
t_W	Master Reset pulse width	Waveform 2	20		10		ns
$t_s(H)$	Setup time, High data to CP	Waveform 3	20		5.0		ns
$t_h(H)$	Hold time, High data to CP	Waveform 3	5.0		3.0		ns
$t_s(L)$	Setup time, Low data to CP	Waveform 3	20		5.0		ns
$t_h(L)$	Hold time, Low data to CP	Waveform 3	5.0		3.0		ns
t_{rec}	Recovery time, MR to CP	Waveform 2	25		5.0		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} after a momentary ground, then ≥4.0V is applied to clock with all outputs open and ≥4.0V applied to all Data inputs and the Master Reset input.
5. These parameters are guaranteed, but not tested.

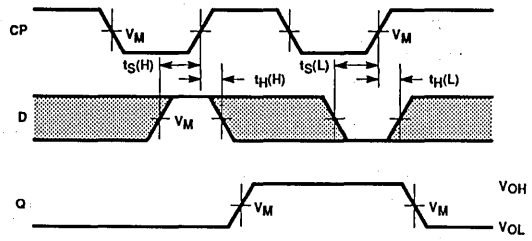
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



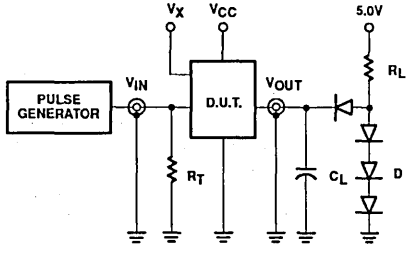
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



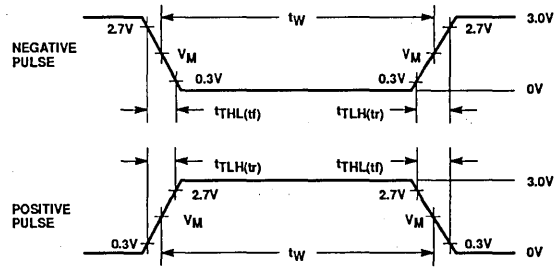
Waveform 3. Data Setup and Hold Times

NOTE: V_M = 1.5V for 54S; V_M = 1.3V for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS295B
Shift Register

4-Bit Shift Register with 3-State Outputs

Product Specification

FEATURES

- **4-bit parallel load shift register**
- **Independent 3-State buffer outputs**
- **See '395 for serial expansion and Master Reset version**

DESCRIPTION

The 54LS295B is a 4-bit Shift Register with serial and parallel synchronous operating modes and four 3-State buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is High, data is loaded from the Parallel Data outputs (D_0 - D_3) into the register synchronous with the High-to-Low transition of the Clock input ($\overline{CP}$). When PE is Low, the data at the Serial Data input (D_S) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative transition of the clock. The PE and Data inputs are fully edge-triggered and must be stable only one setup time prior to the High-to-Low transition of the clock.

The 3-State output buffers are designed to drive heavily loaded 3-State buses or large capacitive loads. The active High Output Enable (OE) controls all four 3-State buffers independent of the register operation. When OE is High the data in the register appears at the outputs. When OE is Low the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

ORDERING INFORMATION

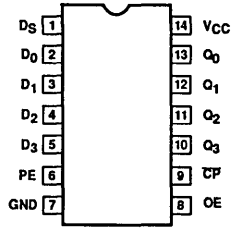
DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54LS295B/BCA
14-Pin Ceramic FlatPack	54LS295B/BDA
20-Pin Ceramic LLCC	54LS295B/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
All	Inputs	1LSUL
All	Outputs	30LSUL

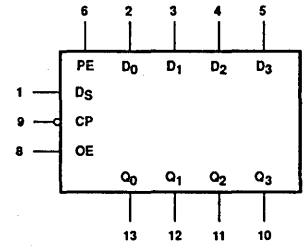
NOTE: A 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2.

LOGIC SYMBOL

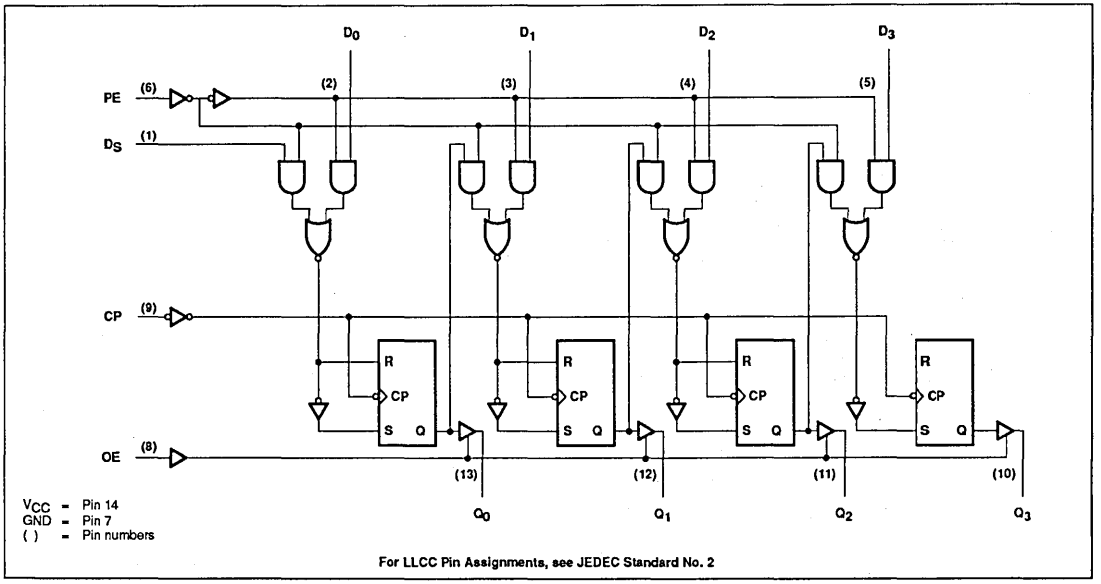


VCC = Pin 14
GND = Pin 7

For LLCC pin assignments, see JEDEC Standard No. 2.

Shift Register | 54LS295B

LOGIC DIAGRAM



For LLCC Pin Assignments, see JEDEC Standard No. 2

MODE SELECT — FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS				REGISTER OUTPUTS			
	$\overline{CP}$	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Shift right	↓	l	l	X	L	q_0	q_1	q_2
	↓	l	h	X	H	q_0	q_1	q_2
Parallel load	↓	h	X	l	L	L	L	L
	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	OE	Q_n (Register)	Q_0, Q_1, Q_2, Q_3
Read	H	L	L
	H	H	H
Disabled	L	X	(Z)

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low clock transition
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low clock transition
X = Don't care
(Z) = High impedance "off" state
↓ = High-to-Low transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1.0	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{OZH}	Offstate output current, High-level voltage applied	V_{CC} = Max, V_{IL} = Max, V_O = 2.7V				20	µA
I_{OZL}	Offstate output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.4V				-20	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V				0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V				-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-30		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	Condition 1		16	29	mA
			Condition 2		17	33	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	30		MHz
t_{PHL} t_{PLH}	Propagation delay Clock to output	Waveform 1		23 30	ns ns
t_{PZH}	Enable time to High level	Waveform 2		26	ns
t_{PZL}	Enable time to Low level	Waveform 3		30	ns
t_{PHZ}	Disable time from High level	Waveform 2, $C_L = 5pF$[5]		20	ns
t_{PLZ}	Disable time from Low level	Waveform 3, $C_L = 5pF$[5]		20	ns
t_{PHZ}	Disable time from High level	Waveform 2, $C_L = 50pF$		36	ns
t_{PLZ}	Disable time from Low level	Waveform 3, $C_L = 50pF$		22	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	16		ns
t_S	Setup time, data to clock	Waveform 4	20		ns
t_h	Hold time, data to clock	Waveform 4	20		ns
t_S	Setup time, PE to clock	Waveform 4	20		ns
t_h	Hold time, PE to clock	Waveform 4	10		ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[6]

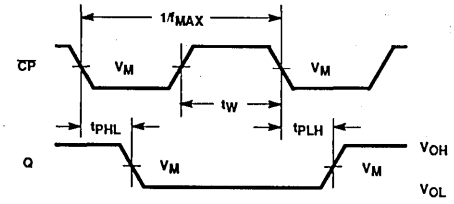
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$, $R_L = 110\Omega$		
			Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1[1]	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		30 39	ns ns
t_{PZH}	Enable time to High level	Waveform 2		34	ns
t_{PZL}	Enable time to Low level	Waveform 3		39	ns
t_{PHZ}	Disable time from High level	Waveform 2, $C_L = 5pF$[5]		26	ns
t_{PLZ}	Disable time from Low level	Waveform 3, $C_L = 5pF$[5]		26	ns
t_{PHZ}	Disable time from High level	Waveform 2, $C_L = 50pF$		47	ns
t_{PLZ}	Disable time from Low level	Waveform 3, $C_L = 50pF$		29	ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

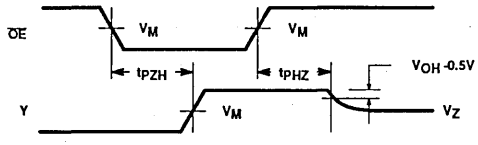
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	25		ns
t_S	Setup time, data to clock	Waveform 4	20		ns
t_h	Hold time, data to clock	Waveform 4	20		ns
t_S	Setup time, PE to clock	Waveform 4	20		ns
t_h	Hold time, PE to clock	Waveform 4	20		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open, D_S and PE at ≥ 4.0V, and the Data inputs grounded under the following conditions: *Condition 1:* OE at ≥ 4.0V and a momentary 3V, then ground, applied to Clock input. *Condition 2:* OE and Clock input grounded.
5. Guaranteed by the 50pF limits, but not tested.
6. These parameters are guaranteed, but not tested.

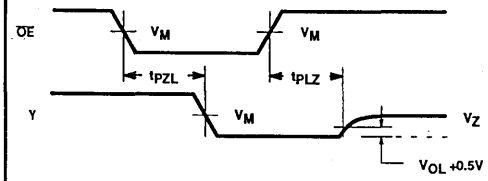
AC WAVEFORMS



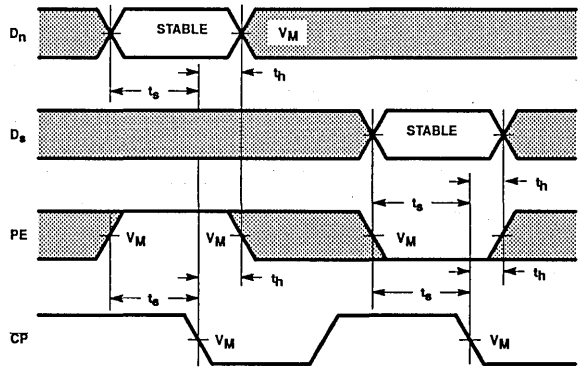
Waveform 1. Clock to Output Delays and Clock Pulse Width



Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



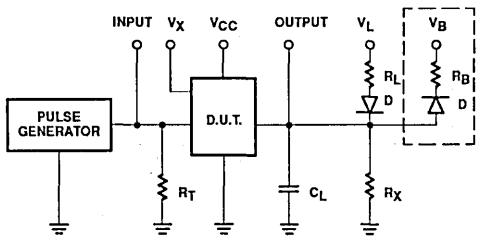
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level



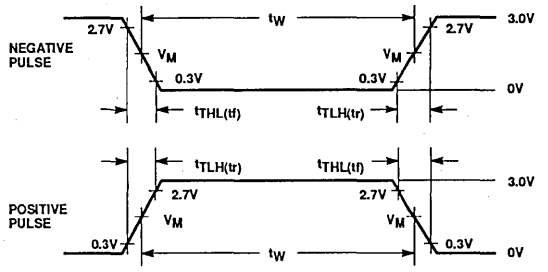
Waveform 4. Parallel Enable and Data Setup and Hold Times

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R1	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54365A, 54367A, 54368A, 54LS365A, 54LS367A

Buffers/Drivers

'365A, '367A Hex Buffer/Driver (3-State)
'368A Hex Inverter Buffer (3-State)

Product Specification

FUNCTION TABLE '365A

INPUTS			OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I	Y	$\overline{Y}$
L	L	L	L	H
L	L	H	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

FUNCTION TABLE '367A, '368A

INPUTS		OUTPUTS	
$\overline{OE}_1$	I	Y	$\overline{Y}$
L	L	L	H
L	H	H	L
H	X	(Z)	(Z)

L = Low voltage level
H = High voltage level
X = Don't care
(Z) = High impedance (off) state

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS365A/BEA, 54365A/BEA 54LS367A/BEA, 54367A/BEA 54368A/BEA
16-Pin Ceramic Flat Pack	54LS365A/BFA, 54LS367A/BFA
16-Pin Ceramic LLCC	54LS365A/B2A, 54LS367A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54	54LS
All	Inputs	1UL	1LSUL
All	Outputs	20UL	30LSUL

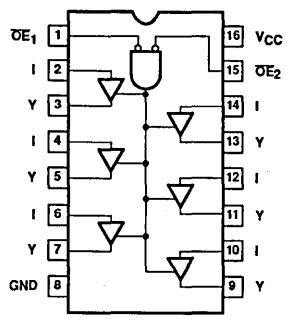
NOTE: Where a 54 Unit Load (UL) is understood to be 40μA I_{IH}, and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

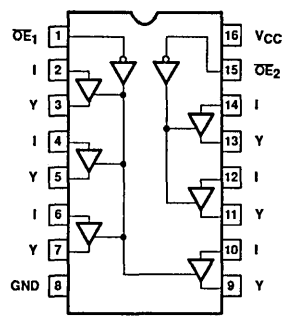
SYMBOL	PARAMETER	54	54LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +5.5	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

PIN CONFIGURATION

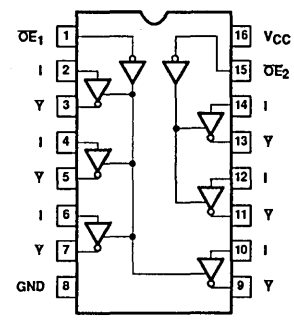
'365A



'367A



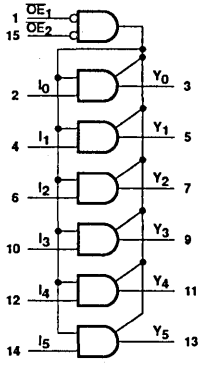
'368A



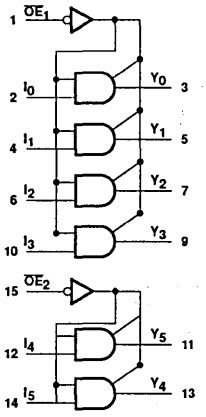
For LLCC Pin Assignments, see JEDEC Standard No. 2

LOGIC SYMBOL

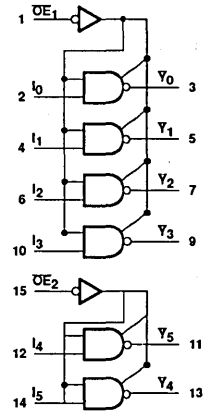
'365A



'367A



'368A



For LLCC Pin Assignment, see JEDEC Standard No. 2

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54			54LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.8			+0.7	V
I_{IK}	Input clamp current			-12			-18	mA
I_{OH}	High-level output current			-2.0			-1.0	mA
I_{OL}	Low-level output current			32			12	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54365A, '367A, '368A			54LS365A, '367A			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max				0.4		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.5	V
I_{OZH}	Off-state output current High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_{IL} = Max, V_O = 2.4V				40			20	µA
I_{OZL}	Off-state output current Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_{IL} = Max, V_O = 0.4V				-40			-20	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V			1.0				mA
			V_I = 7.0V						0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max	V_I = 2.4V			40				µA
			V_I = 2.7V						20	µA
I_{IL}	Low-level input current	V_{CC} = Max	I inputs, V_I = 0.5V Either $\overline{OE}$ input at 2.0V (Does not aply to 'LS365A or 'LS367A)			-40				µA
			I inputs, V_I = 0.4V Both $\overline{OE}$ inputs at 0.4V			-1.6			-0.4	mA
			$\overline{OE}$ inputs V_I = 0.4V			-1.6			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-40		-130	-30		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	'365A, 367A		65	85		14	24	mA
			'368A		59	77		12	21	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

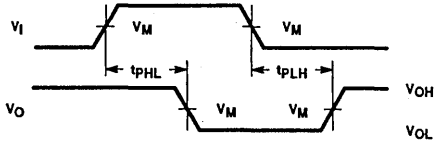
SYMBOL	PARAMETER	TEST CONDITIONS		54		54LS		UNIT
				C_L = 50pF		C_L = 50pF		
				Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '368A			17 16		15 18	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '365A, '367A			16 22		16 22	ns ns
t_{PZH}	Enable to High	Waveform 3			35		35	ns
t_{PZL}	Enable to Low	Waveform 4	'365A, '367A		37		40	ns
			'368A		37		45	ns
t_{PHZ}	Disable from High	Waveform 3, C_L = 5pF[5]	'365A, '367A		11		30	ns
			'368A		11		32	ns
t_{PLZ}	Disable from Low	Waveform 4, C_L = 5pF[5]			27		35	ns
t_{PHZ}	Disable from High	Waveform 3, C_L = 50pF	'365A, '367A		21		48	ns
			'368A		21		48	ns
t_{PLZ}	Disable from Low	Waveform 4, C_L = 50pF			28		37	ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and + 125°C, V_{CC} = 5.0V[6]

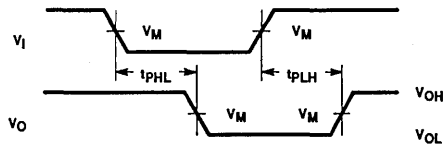
SYMBOL	PARAMETER	TEST CONDITIONS		54		54LS		UNIT
				C_L = 50pF		C_L = 50pF		
				Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '368A			22 21		20 23	ns ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '365A, '367A			21 27		21 29	ns ns
t_{PZH}	Enable to High	Waveform 3			40		40	ns
t_{PZL}	Enable to Low	Waveform 4	'365A, '367A		42		52	ns
			'368A		42		59	ns
t_{PHZ}	Disable from High	Waveform 3, C_L = 5pF[5]	'365A, '367A		16		39	ns
			'368A		16		42	ns
t_{PLZ}	Disable from Low	Waveform 4, C_L = 5pF[5]			30		40	ns
t_{PHZ}	Disable from High	Waveform 3, C_L = 50pF	'365A, '367A		20		60	ns
			'368A		20		62	ns
t_{PLZ}	Disable from Low	Waveform 4, C_L = 50pF			32		48	ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Data inputs grounded and Output Enable inputs ≥ 4.0V.
5. Guaranteed by 50pF limits, but not tested.
6. These parameters are guaranteed, but not tested.

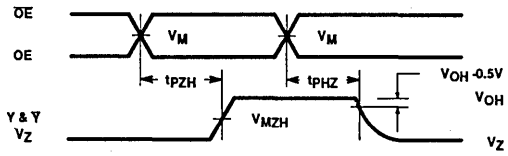
AC WAVEFORMS



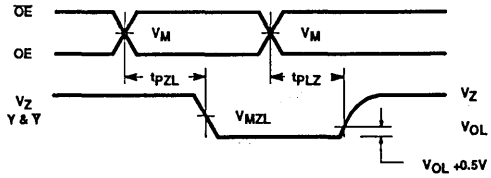
Waveform 1. Waveform for Inverting Outputs



Waveform 2. Waveform for Non-Inverting Outputs



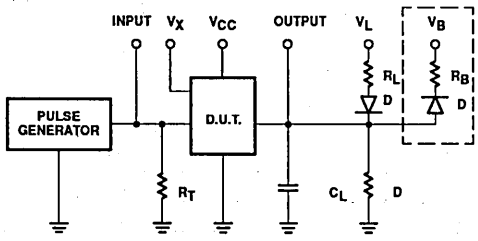
Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



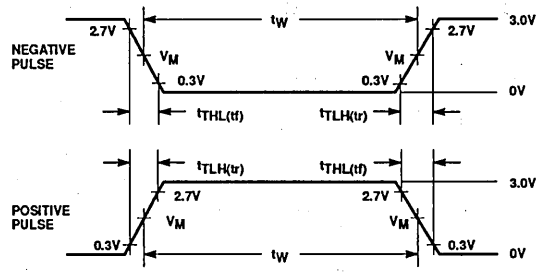
Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V
54XXX	1.5V	0.7V	1.9V	1.45V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R1	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns
54XXX	31Ω	1.2kΩ	2.1V	1.5V	1MHz	500ns	≤7ns	≤7ns

Optional load for 54LSXXX only: $R_B = 631\Omega$; $V_B = 5.5V$ for all tests except T_{PHZ}; $V_B = -0.6V$ for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS373, 54LS374, 54S373, 54S374

Latches/Flip-Flops

'373 Octal Transparent Latch with 3-State Outputs
'374 Octal D Flip-Flop with 3-State Outputs
Product Specification

FEATURES

- **8-bit transparent latch — '373**
- **8-bit positive, edge-triggered register — '374**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

DESCRIPTION

The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

ORDERING INFORMATION

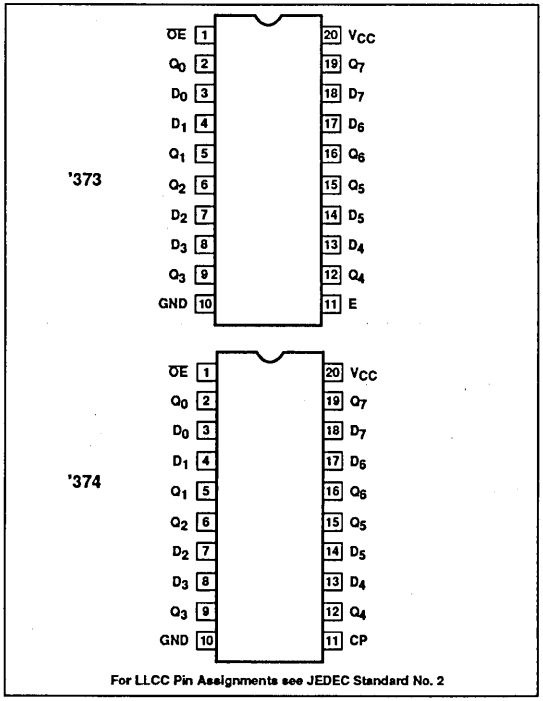
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54LS373/BRA 54S373/BRA 54LS374/BRA 54S374/BRA
20-Pin Ceramic FlatPack	54LS373/BSA 54S373/BSA 54LS374/BSA 54S374/BSA
20-Pin Ceramic LLCC	54LS373/B2A 54S373/B2A 54LS374/B2A 54S374/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S	54LS
All	Inputs	1SUL	1LSUL
All	Outputs	10SUL	30LSUL

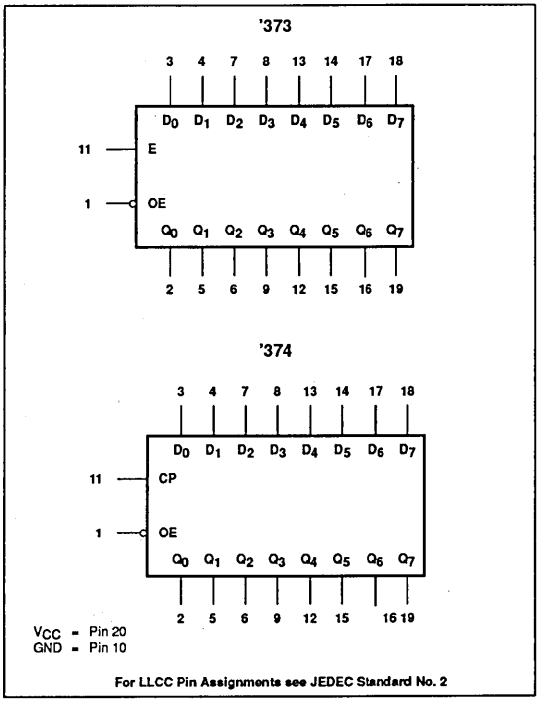
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL} and a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data present one setup time before the High-to-Low enable transition. The enable gate has hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

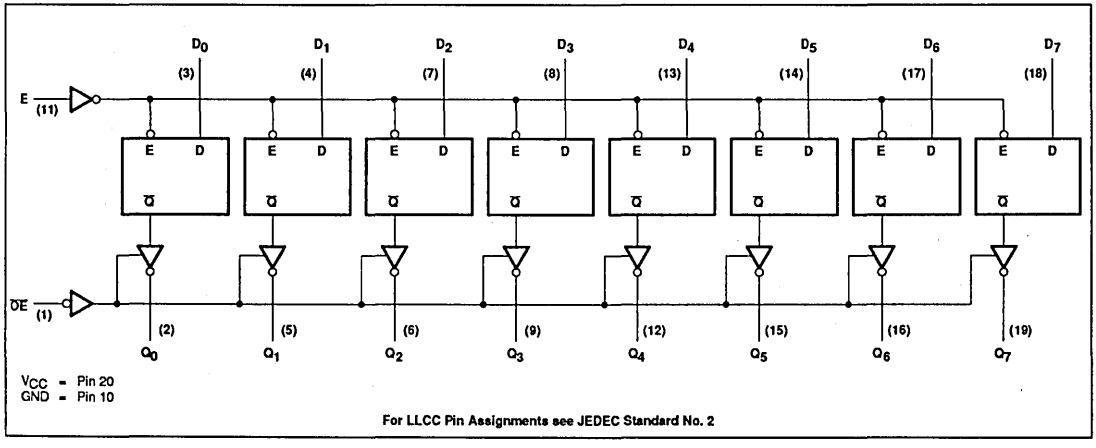
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

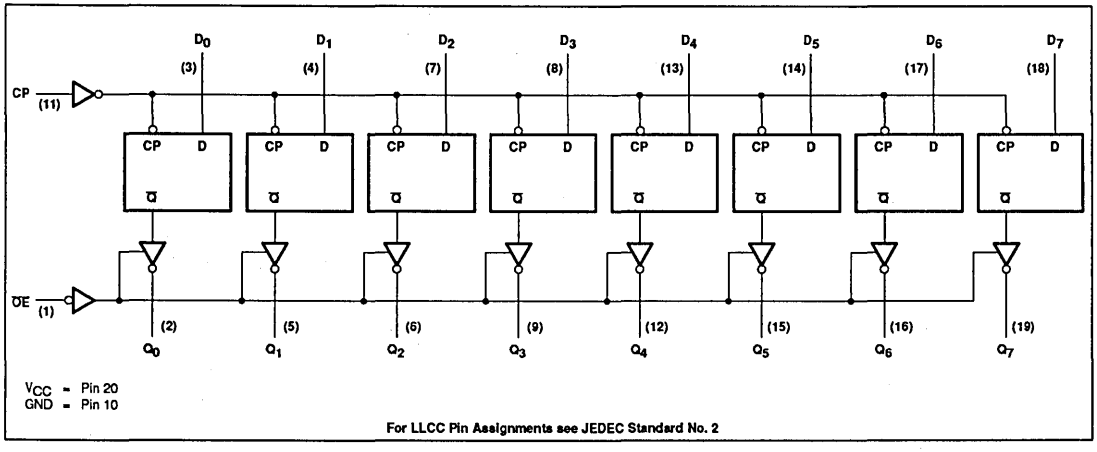
The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC DIAGRAM, ' 374



For LLCC Pin Assignments see JEDEC Standard No. 2

MODE SELECT — FUNCTION TABLE '373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0 - Q_7
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

MODE SELECT — FUNCTION TABLE '374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0 - Q_7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = High voltage level
h = High voltage level one setup time prior to the Low-to-High clock transition or High-to-Low $\overline{OE}$ transition
L = Low voltage level
X = Don't care
l = Low voltage level one setup time prior to Low-to-High clock transition or High-to-Low $\overline{OE}$ transition
(Z) = High impedance "off" state
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.7			+0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-1.0			-2.0	mA
I_{OL}	Low-level output current			12			20	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			54LS373, 374			54S373, 374			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC}=Min, V_{IH}=Min, V_{IL}=Max, I_{OH}=Max			2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IH}=Min, V_{IL}=Max, I_{OL}=Max				0.25	0.4			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5			-1.2	V
I_{IZH}	Off-state output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min	V_O = 2.7V				20				µA
			V_O = 2.4V							50	µA
I_{IZL}	Off-state output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min	V_O = 0.4V				-20				µA
			V_O = 0.5V							-50	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 7.0V				0.1				mA
			V_I = 5.5V							1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V					20			50	µA
I_{IL}	Low level input current	V_{CC} = Max	V_I = 0.4V				-400				µA
			V_I = 0.5V							0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-30		-130	-40		-100	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCZ}	$\overline{OE}$ ≥4.0V 'LS373		24	40				mA
			I_{CCL}	$\overline{OE}$ = 0V 'S373					105	160	mA
			I_{CCZ}	$\overline{OE}$ ≥4.0V 'LS374		27	40				mA
			I_{CCL}	All inputs grounded 'S374					102	140	mA
			I_{CCZ}	CP, $\overline{OE}$ ≥4.0V 'S374 D inputs = GND					131	180	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54S373, 374 C_L = 15pF		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, '374	75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch enable to output	Waveform 1, '373		14 18	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, '373		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, '374		15 17	ns ns
t_{PZH}	Enable time to High level	Waveform 2		15	ns
t_{PZL}	Enable time to Low level	Waveform 3, '373, '374		18 18	ns ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 5pF[4]		9	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 5pF[4]		12	ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 50pF		14	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 50pF		13.5	ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS373, 374		54S373, 374[5]		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, '374	35		75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch enable to output	Waveform 1, '373		30 30		16.5 20.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, '373		18 18		14.5 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, '374		28 28		17.5 19.5	ns ns
t_{PZH}	Enable time to High level	Waveform 2		28		17.5	ns
t_{PZL}	Enable time to Low level	Waveform 3, '373, '374		36 28		20.5 20.5	ns ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 5pF[4]		20		9	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 5pF[4]		25		12	ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 50pF		36		14	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 50pF		27		13.5	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_{W(H)}$ $t_{W(L)}$	Latch enable pulse width	Waveform 1, '373	15 15		6 7.3		ns ns
t_s	Setup time, data to latch enable	Waveform 5, '373	5		0		ns
t_h	Hold time, data to latch enable	Waveform 5, '373	20		10		ns
$t_{W(H)}$ $t_{W(L)}$	Clock pulse width	Waveform 6, '374	15 15		6 7.3		ns ns
t_s	Setup time, data to clock	Waveform 7, '374	20		5		ns
t_h	Hold time, data to clock	Waveform 7, '374	0		2		ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

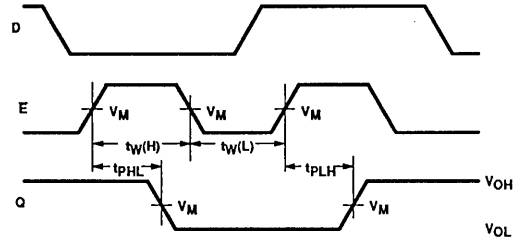
SYMBOL	PARAMETER	TEST CONDITIONS	54LS373, 374		54S373, 374[5]		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, '374	26		75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch enable to output	Waveform 1, '373		39 39		21 27	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, '373		23 23		16 16	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, '374		36 36		23 25	ns ns
t_{PZH}	Enable time to High level	Waveform 2		36		23	ns
t_{PZL}	Enable time to Low level	Waveform 3, '373, '374		47 36		27 27	ns ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 5pF[4]		25		12	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 5pF[4]		33		16	ns
t_{PHZ}	Disable time from High level	Waveform 2, C_L = 50pF		47		18.5	ns
t_{PLZ}	Disable time from Low level	Waveform 3, C_L = 50pF		35		18	ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

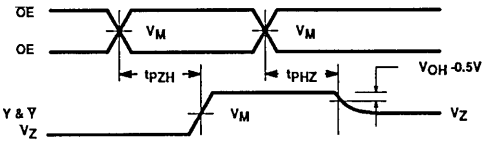
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_W(H)$ $t_W(L)$	Latch enable pulse width	Waveform 1, '373	15 15		6 7.3		ns ns
t_s	Setup time, data to latch enable	Waveform 5, '373	5		0		ns
t_h	Hold time, data to latch enable	Waveform 5, '373	20		15		ns
$t_W(H)$ $t_W(L)$	Clock pulse width	Waveform 6, '374	15 15		6 7.3		ns ns
t_s	Setup time, data to clock	Waveform 7, '374	20		5		ns
t_h	Hold time, data to clock	Waveform 7, '374	5		2		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Guaranteed by the 50pF limits, but not tested.
5. These parameters are guaranteed, but not tested.

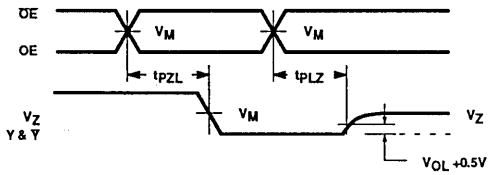
AC WAVEFORMS



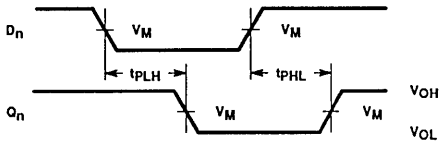
Waveform 1. Latch Enable to Output Delays and Latch Enable Pulse Width



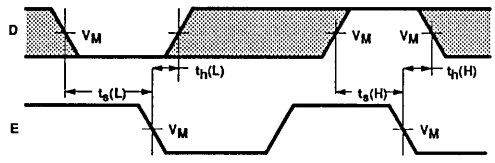
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



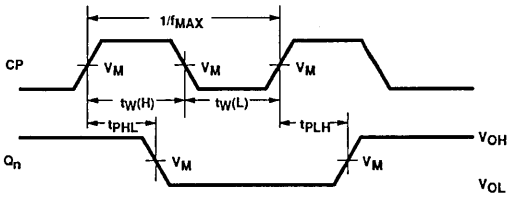
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level



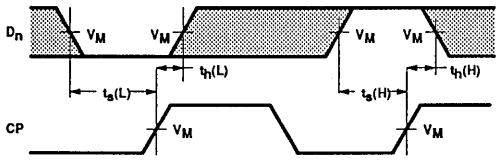
Waveform 4. Propagation Delay Data to Q Outputs



Waveform 5. Data Setup and Hold Times



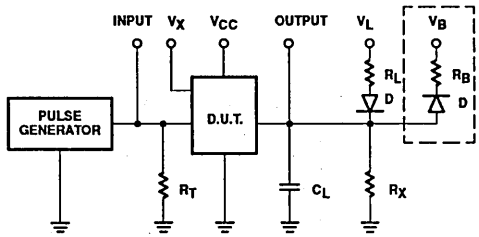
Waveform 6. Clock to Output Delays and Pulse Width



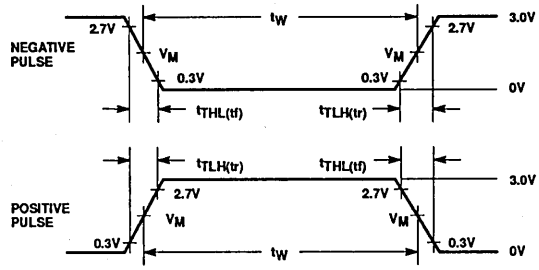
Waveform 7. Data Setup and Hold Times

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V
54SXXX	1.5V	0.7V	2.0V	1.65V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	82Ω	560Ω	2.5V	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

Optional load for 54LSXXX only: $R_B = 631\Omega$; $V_B = 5.5V$ for all tests except T_{PHZ}; $V_B = -0.6V$ for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

Military Logic Products

54LS377
Flip-Flop

Octal D Flip-Flop With Clock Enable

Product Specification

FEATURES

- **Ideal for addressable register applications**
- **Clock Enable for address and data synchronization applications**
- **Eight edge-triggered D flip-flops**
- **Buffered common clock**
- **Slim 20-pin plastic and ceramic DIP packages**
- **See '273 for Master Reset version**
- **See '373 for transparent latch version**
- **See '374 for 3-State version**

DESCRIPTION

The 54LS377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is Low.

The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the Low-to-High clock transition for predictable operation.

ORDERING INFORMATION

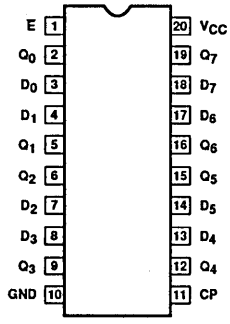
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54LS377/BRA
20-Pin Ceramic FlatPack	54LS377/BSA
20-Pin Ceramic LLCC	54LS377/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
All	Inputs	1LSUL
All	Outputs	10LSUL

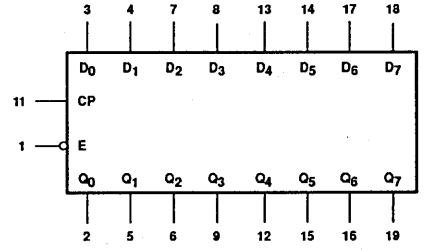
NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

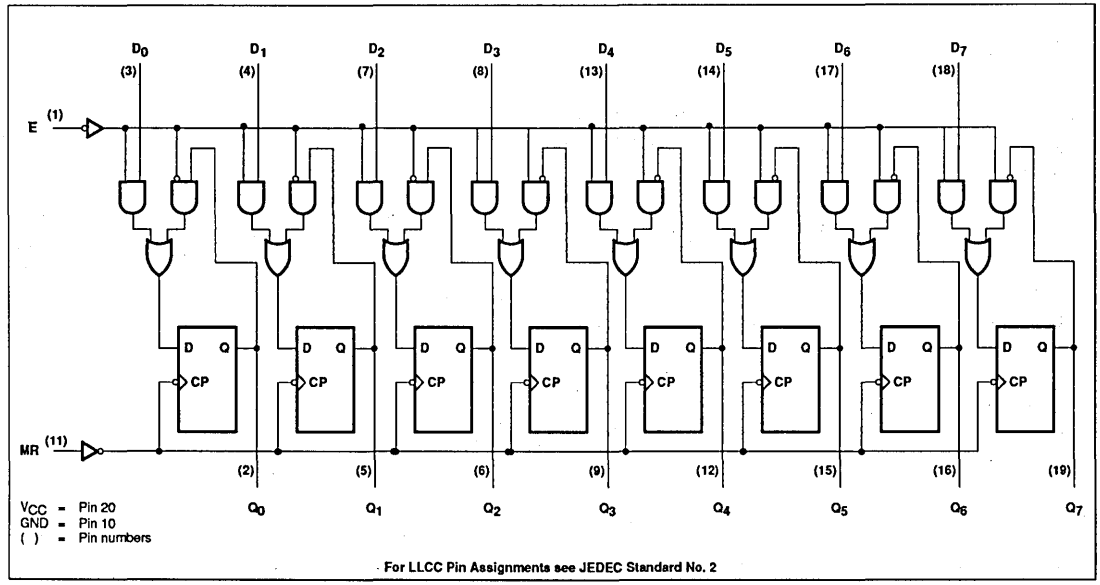
LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

For LLCC Pin Assignments see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC Pin Assignments see JEDEC Standard No. 2

MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	↑	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = High voltage level steady state
h = High voltage level one setup time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one setup time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V				0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V				-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	mA
I_{CC}	Supply current (total)	V_{CC} = Max	I_{CCH} Outputs High		18	28	mA
			I_{CCL} Outputs Low		22	35	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 27	ns ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
$t_{W}(L)$	Clock pulse width (Low)	Waveform 1	20		ns
t_s	Setup, data to CP	Waveform 2	20		ns
t_h	Hold time, data to CP	Waveform 2	5		ns
t_s	Setup time, $\overline{CE}$ to CP	Waveform 2	20		ns
t_h	Hold time, $\overline{CE}$ to CP	Waveform 2	5		ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		32 32	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

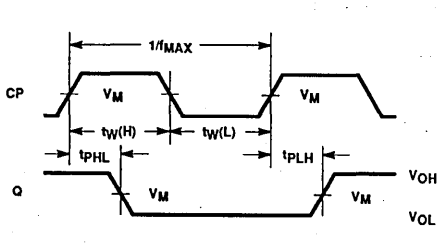
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		42 42	ns ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V[5]

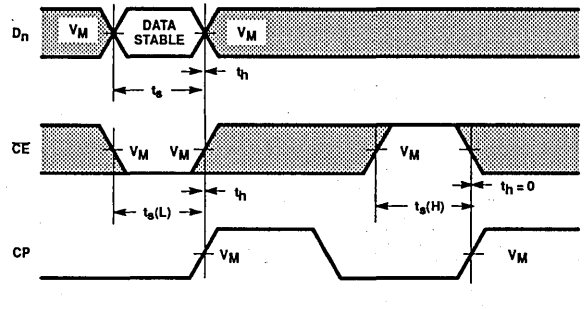
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
$t_{W}(L)$	Clock pulse width (Low)	Waveform 1	20		ns
t_s	Setup, data to CP	Waveform 2	20		ns
t_h	Hold time, data to CP	Waveform 2	5		ns
t_s	Setup time, $\overline{CE}$ to CP	Waveform 2	20		ns
t_h	Hold time, $\overline{CE}$ to CP	Waveform 2	5		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



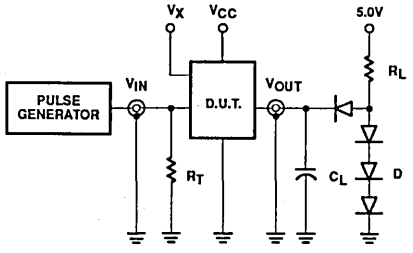
Waveform 1. Clock to Output Delays and Clock Pulse Width



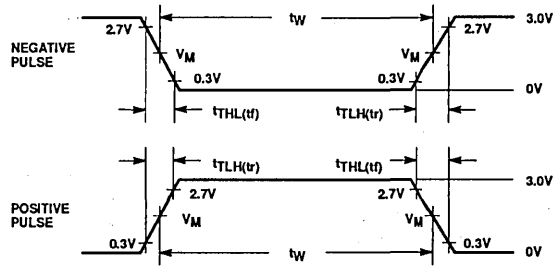
Waveform 2. Data and Clock Enable Setup and Hold Times

NOTE: V_M = 1.3V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0KΩ	1.3V	1MHz	500ns	≤15ns	≤6ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54LS393
Counter

Dual 4-Bit Binary Ripple Counter

Product Specification

Military Logic Products

FEATURES

- **Two 4-bit binary counters**
- **Divide-by any binary module up to 28 in one package**
- **Two Master Resets to clear each 4-bit counter individually**

DESCRIPTION

The 54LS393 is a Dual 4-bit Binary Ripple Counter with separate Clock and Master Reset inputs to each counter. The operation of each half of the '393 is the same as the '93 except no external clock connections are required. The counters are triggered by a High-to-Low transition of the Clock ($\overline{CP}_a$ and $\overline{CP}_b$) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The Master Resets (MR_a and MR_b) are active-High asynchronous inputs to each 4-bit counter identified by the "a" and "b" suffixes in the Pin Configuration. A High level on the MR input overrides the clock and sets the outputs Low.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
14-Pin Ceramic DIP	54LS393/BCA
14-Pin Ceramic Flat Pack	54LS393/BDA
14-Pin Ceramic LLCC	54LS393/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
MR	Master reset input	1LSUL
$\overline{CP}$	Clock input	4LSUL
Q	Output	10LSUL

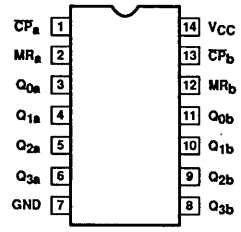
NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

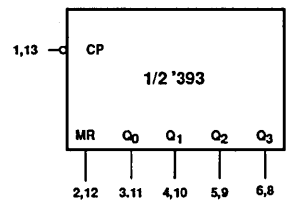
NOTE: V_I limited to +5.5V on $\overline{CP}$ input only.

PIN CONFIGURATION



For LLCC Pin Assignments see JEDEC Standard No. 2

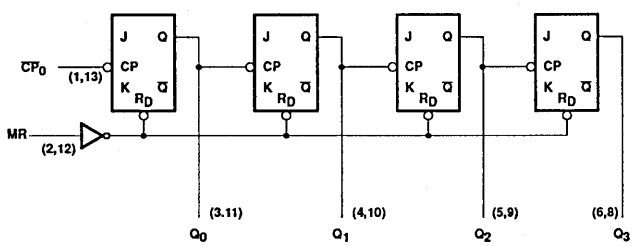
LOGIC SYMBOL



For LLCC Pin Assignments see JEDEC Standard No. 2

Counter | 54LS393

LOGIC DIAGRAM



VCC = Pin 14
GND = Pin 7
( ) = Pin number

For LLCC Pin Assignments, see JEDEC Standard No. 2

COUNT SEQUENCE FOR 1/2 THE '393

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = High voltage level
L = Low voltage level

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-400	µA
I_{OL}	Low-level output current			4	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max			2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max				0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}					-1.5	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 7.0V	MR input			0.1	mA
			V_I = 5.5V	$\overline{CP}$ input			0.2	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V		MR inputs			20	µA
				$\overline{CP}$ input			100	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V		MR input			-0.4	mA
				$\overline{CP}$ input			-1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max			-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max				15	26	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[5]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS $C_L = 15pF$		UNIT
			Min	Max	
f_{MAX}	$\overline{CP}$ input count frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_0	Waveform 1		20 20	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_3	Waveform 1		60 60	ns ns
t_{PHL}	Propagation delay, MR to Q	Waveform 2		39	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMIT		UNIT
			Min	Max	
t_W	$\overline{CP}$ pulse width	Waveform 1	20		ns
t_W	MR pulse width	Waveform 2	20		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2	25		ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS $C_L = 50pF$		UNIT
			Min	Max	
f_{MAX}	$\overline{CP}$ input count frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_0	Waveform 1		25 25	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_3	Waveform 1		65 65	ns ns
t_{PHL}	Propagation delay, MR to Q	Waveform 2		44	ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[5]

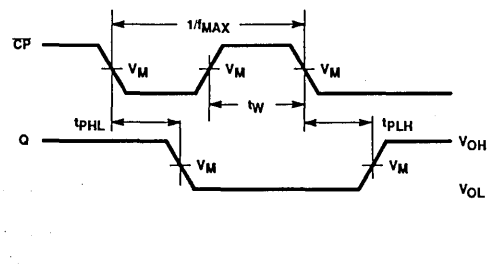
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS $C_L = 50pF$		UNIT
			Min	Max	
f_{MAX}	$\overline{CP}$ input count frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_0	Waveform 1		33 33	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_3	Waveform 1		85 85	ns ns
t_{PHL}	Propagation delay, MR to Q	Waveform 2		57	ns

AC SETUP REQUIREMENTS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[5]

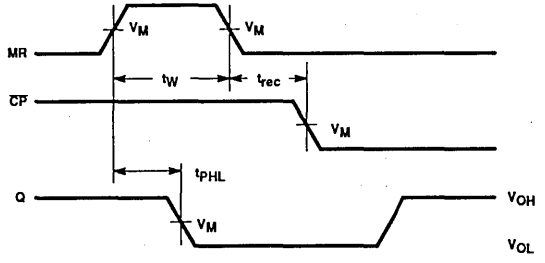
SYMBOL	PARAMETER	TEST CONDITIONS	LIMIT		UNIT
			Min	Max	
t_W	$\overline{CP}$ pulse width	Waveform 1	20		ns
t_W	MR pulse width	Waveform 2	20		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2	25		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with both MR inputs grounded following momentary connection to $\geq 4.0V$, all other inputs grounded and all outputs open.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



Waveform 1

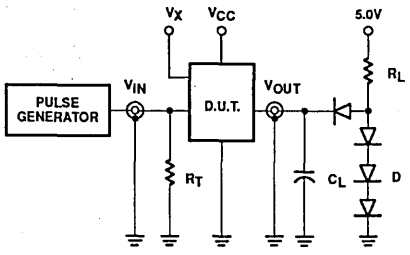


Waveform 2

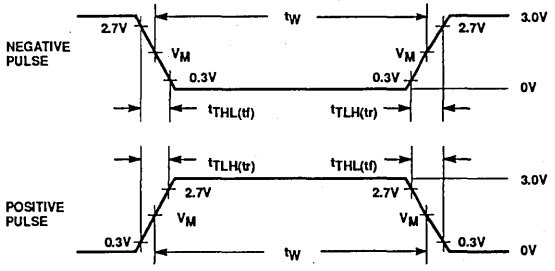
NOTE: V_M = 1.3V for 54LS

The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Function Table.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

54LS395A
Shift Register

4-Bit Cascadable Shift Register With 3-State Outputs

Product Specification

Military Logic Products

FEATURES

- **4-bit parallel load shift register**
- **Independent 3-State buffer outputs**
- **Separate Q_3 output for serial expansion**
- **Asynchronous master reset**

DESCRIPTION

The 54LS395 is a 4-bit Shift Register with serial and parallel synchronous operating modes and four 3-State buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is High, data is loaded from the Parallel Data inputs (D_0 - D_3) into the register synchronous with the High-to-Low transition of the Clock input ($\overline{CP}$). When PE is Low, the data at the Serial Data input (D_S) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable only one setup prior to the High-to-Low transition of the clock.

The Master Reset ($\overline{MR}$) is an asynchronous active-Low input. When Low, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, or large capacitive loads. The active-Low Output Enable ($\overline{OE}$) controls all four 3-State buffers independent of the register operation. The data in the register appears at the outputs when $\overline{OE}$ is Low. The outputs are in the High impedance "off" state, which means they will neither drive nor load the bus when $\overline{OE}$ is High. The output from the last stage is brought out separately. This output (Q_3) is tied to the Serial Data input (D_S) of the next register for serial expansion applications. The Q_3 output is not affected by the 3-State buffer operation.

ORDERING INFORMATION

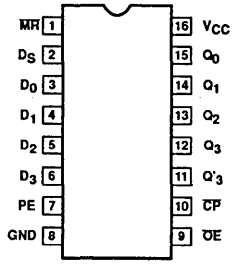
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS395A/BEA
16-Pin Ceramic FlatPack	54LS395A/BFA
16-Pin Ceramic LLCC	54LS395A/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54LS
All	Inputs	1LSUL
Q_0 - Q_3	Outputs	30LSUL
Q_3	Output	10LSUL

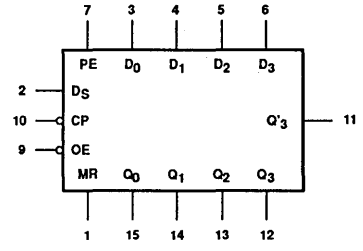
NOTE: Where a 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

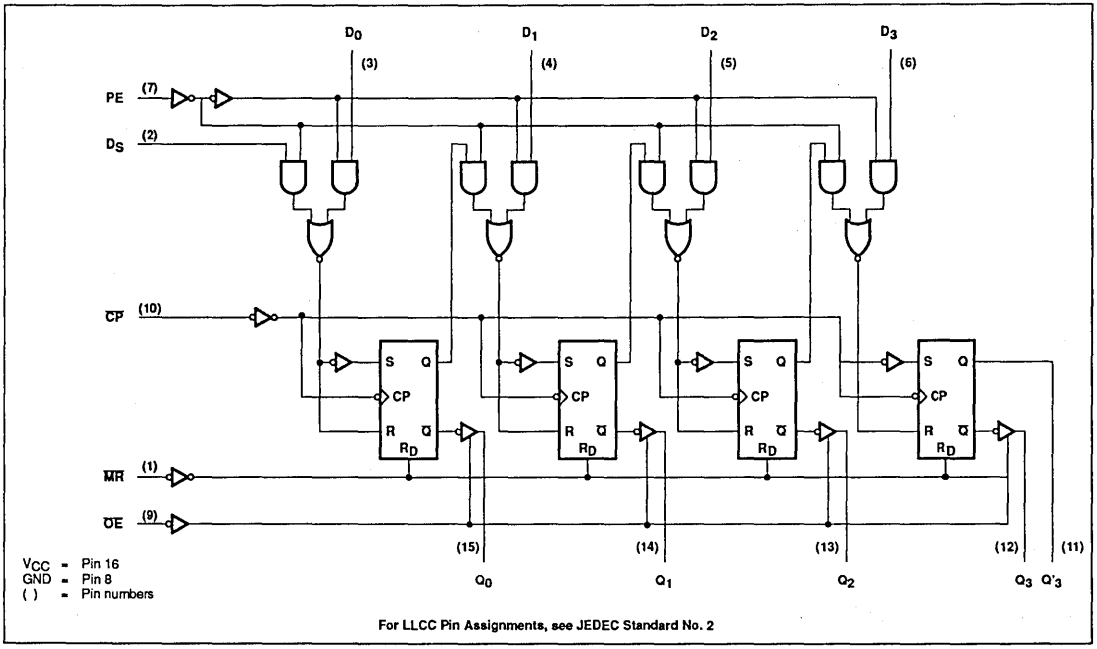
LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC Pin Assignments, see JEDEC Standard No. 2

FUNCTION TABLE

RESISTER OPERATING MODES	INPUTS					OUTPUTS			
	$\overline{MR}$	$\overline{CP}$	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift right	H	↓	l	l	X	L	q_0	q_1	q_2
	H	↓	l	h	X	H	q_0	q_1	q_2
Parallel load	H	↓	h	X	l	L	L	L	L
	H	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS	
	$\overline{OE}$	Q_n (Register)	Q_0, Q_1, Q_2, Q_3	Q'_3
Read	L	L	L	L
	L	H	H	H
Disable buffers	H	L	(Z)	L
	H	H	(Z)	H

H = High voltage level
h = High voltage level one setup time prior to the High-to-Low clock transition
L = Low voltage level
l = Low voltage level one setup time prior to the High-to-Low clock transition
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the High-to-Low clock transition
X = Don't care
(Z) = High impedance "off" state
↓ = High-to-Low transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				+0.7	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Q'_3			-400	µA
		Q_0 - Q_3			-1.0	mA
I_{OL}	Low-level output current	Q'_3			4	mA
		Q_0 - Q_3			12	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min,	Q_3	2.5	3.4		V
		V_{IL} = Max, I_{OH} = Max	Q_0, Q_1, Q_2, Q_3	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max Q_0, Q_1, Q_2, Q_3			0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5	V
I_{OZH}	Offstate output current, High-level voltage applied	V_{CC} = Min, V_{IH} = Min, V_O = 2.7V Q_0, Q_1, Q_2, Q_3				20	µA
I_{OZL}	Offstate output current, Low-level voltage applied	V_{CC} = Min, V_{IH} = Min, V_O = 0.4V Q_0, Q_1, Q_2, Q_3				-20	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V				0.1	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V				-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	Q'_3	-20		-100	mA
			Q_0, Q_1, Q_2, Q_3	-30		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max	Condition 1		19	34	mA
			Condition 2		19	31	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to buffer outputs	Waveform 1		30 30	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q'_3 output	Waveform 1		30 30	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		35	ns
t_{PZH}	Enable time to High level	Waveform 3		25	ns
t_{PZL}	Enable time to Low level	Waveform 4		25	ns
t_{PHZ}	Disable time from High level	Waveform 3, $C_L = 5pF$[5]		17	ns
t_{PLZ}	Disable time from Low level	Waveform 4, $C_L = 5pF$[5]		20	ns
t_{PHZ}	Disable time from High level	Waveform 3, $C_L = 50pF$		33	ns
t_{PLZ}	Disable time from Low level	Waveform 4, $C_L = 50pF$		22	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	20		ns
t_W	Master reset pulse width	Waveform 2	25		ns
t_S	Setup time, data to clock	Waveform 5	20		ns
t_h	Hold time, data to clock	Waveform 5	10		ns
t_S	Setup time, PE to clock	Waveform 5	40		ns
t_h	Hold time, PE to clock	Waveform 5	10		ns
t_{rec}	Recovery time, $\overline{MR}$ to clock	Waveform 2	30		ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[6]

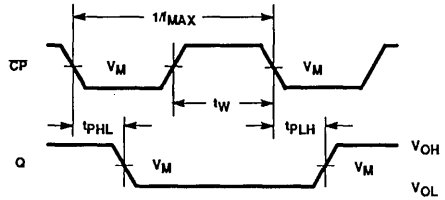
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to buffer outputs	Waveform 1		39 39	ns ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q_3 output	Waveform 1		39 39	ns ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		46	ns
t_{PZH}	Enable time to High level	Waveform 3		33	ns
t_{PZL}	Enable time to Low level	Waveform 4		33	ns
t_{PHZ}	Disable time from High level	Waveform 3, $C_L = 5pF$[5]		22	ns
t_{PLZ}	Disable time from Low level	Waveform 4, $C_L = 5pF$[5]		26	ns
t_{PHZ}	Disable time from High level	Waveform 3, $C_L = 50pF$		43	ns
t_{PLZ}	Disable time from Low level	Waveform 4, $C_L = 50pF$		29	ns

AC SETUP REQUIREMENTS T_A = -55°C and +125°C, V_{CC} = 5.0V

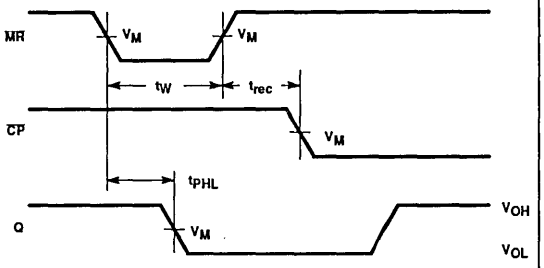
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	20		ns
t_W	Master reset pulse width	Waveform 2	25		ns
t_S	Setup time, data to clock	Waveform 5	20		ns
t_h	Hold time, data to clock	Waveform 5	10		ns
t_S	Setup time, PE to clock	Waveform 5	40		ns
t_h	Hold time, PE to clock	Waveform 5	10		ns
t_{rec}	Recovery time, $\overline{MR}$ to clock	Waveform 2	30		ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with D_S and Master Reset at $\geq$ 4.0V. The Data inputs grounded and outputs open under the following conditions: *Condition 1:* $\overline{OE}$ at $\geq$ 4.0V. A momentary 3V, then ground, applied to $\overline{CP}$. *Condition 2:* Ground $\overline{OE}$ and $\overline{CP}$ inputs.
5. Guaranteed by the 50pF limits, but not tested.
6. These parameters are guaranteed, but not tested.

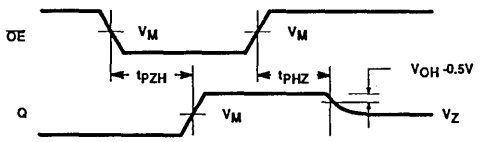
AC WAVEFORMS



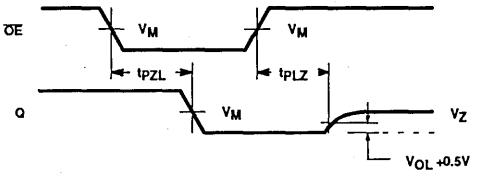
Waveform 1. Clock to Output Delays and Clock Pulse Width



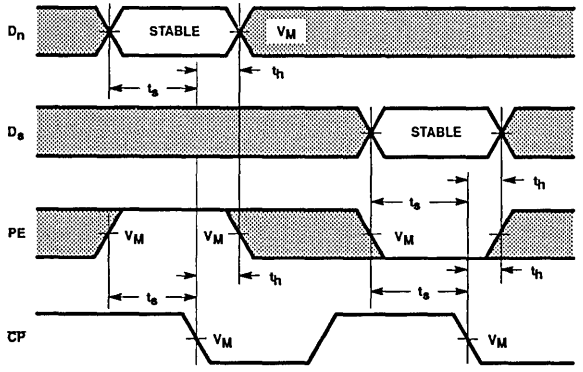
Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. 3-State Enable Time to High Level and Disable Time from High Level



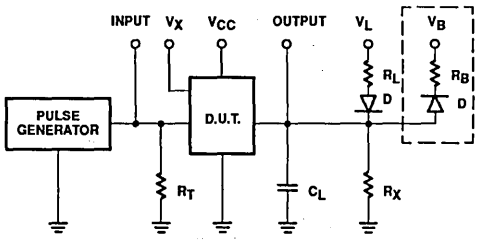
Waveform 4. 3-State Enable Time to Low Level and Disable Time from Low Level



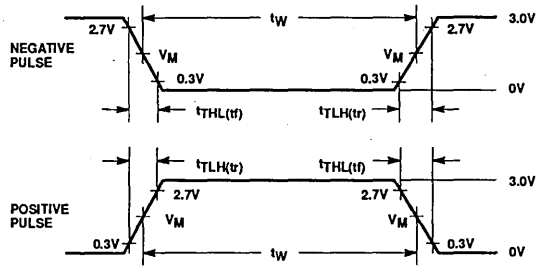
Waveform 5. Parallel Enable and Data Setup and Hold Times

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54LSXXX	1.3V	0.7V	1.9V	1.45V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	110Ω	2.4kΩ	2.1V	1.3V	1MHz	500ns	≤15ns	≤6ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.

Signetics

8T09
Quad Bus Driver

3-State Quad Bus Driver

Product Specification

Military Logic Products

FEATURES

- **High speed**
- **Quad bus driver**
- **30mA Low-state drive**
- **300pF load driving capability**

DESCRIPTION

The 8T09 is a high-speed quad bus driver device for applications requiring up to 25 loads interconnected on a single bus.

The 3-state outputs present high-impedance to the bus when disabled (control input "1"), and active drive when enabled (control input "0"). This eliminates the resistor pullup requirement while providing performance superior to open collector schemes. Each output can sink 30mA and drive 300pF loading with guaranteed propagation delay less than 30 nanoseconds.

ORDERING INFORMATION

DESCRIPTION	PIN CONFIGURATION	ORDER CODE
Ceramic DIP	Figure A	8T09/BCA
Ceramic Flatpack	Figure B	8T09/BDA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
Data	Input	1UL
Disable	Input	1UL
3, 6, 8, 11	Output	10UL

NOTE: A Unit Load (UL) is 40μA I_{IH} and -1.6mA I_{IL}.

FUNCTION TABLE

DATA	DISABLE	OUTPUT
0	0	1
1	0	0
0	1	Hi-Z
1	1	Hi-Z

PIN CONFIGURATION

Figure A

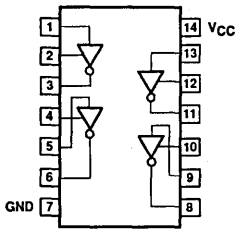
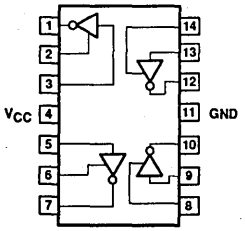
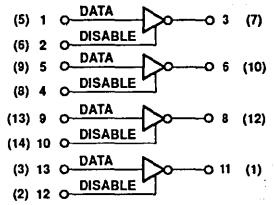


Figure B



LOGIC SYMBOL



VCC = Pin 14
GND = Pin 7
( ) = Figure B

Quad Bus Driver | 8T09

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.7	V
I_{IK}	Input clamp current			-12	mA
I_{OH}	High-level output current			-5.2	mA
I_{OL}	Low-level output current			30	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS		UNIT
			Min	Max	
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IK} = -12mA		-1.5	V
V_{OH}	High-level output voltage	V_{CC} = Min, I_{OH} = -5.2 mA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = 30mA		0.4	V
I_{IH}	High-level input current	V_{CC} = Max, V_I = 4.5V		40	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.4V		-2	mA
I_{OZH}	Offstate output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.4V		40	µA
I_{OZL}	Offstate output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.4V		-40	µA
I_{OS}	Short-circuit output current[2]	V_{CC} = Max	-40	-120	mA
I_{CC}	Supply current (total)	V_{CC} = 5.25V		65	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

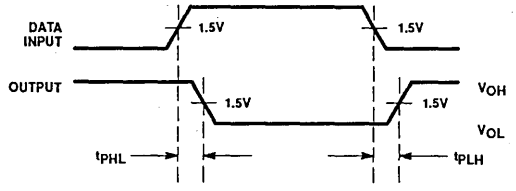
SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS		UNIT
				Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Figure 1	C_L = 30pF C_L = 300pF		10 20	ns ns
t_{PZH}	Enable to High	Figure 3	C_L = 30pF C_L = 300pF		14 22	ns ns
t_{PZL}	Enable to Low	Figure 2	C_L = 30pF C_L = 300pF		14 22	ns ns
t_{PHZ}	Disable from High	Figure 3	C_L = 30pF C_L = 300pF		14 22	ns ns
t_{PLZ}	Disable from Low	Figure 2	C_L = 30pF C_L = 300pF		14 22	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[3]

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS		UNIT
				Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Figure 1	C_L = 30pF C_L = 300pF		13 26	ns ns
t_{PZH}	Enable to High	Figure 3	C_L = 30pF C_L = 300pF		18 28	ns ns
t_{PZL}	Enable to Low	Figure 2	C_L = 30pF C_L = 300pF		18 28	ns ns
t_{PHZ}	Disable from High	Figure 3	C_L = 30pF C_L = 300pF		18 28	ns ns
t_{PLZ}	Disable from Low	Figure 2	C_L = 30pF C_L = 300pF		18 28	ns ns

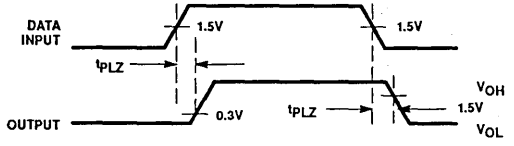
NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. Not more than one output should be shorted at a time and duration of the short circuit should not exceed on second.
3. These parameters are guaranteed, but not tested.

AC TEST CIRCUITS AND WAVEFORMS



INPUT PULSE:
$t_r = t_f \leq$ 5ns (0.3V TO 2.7V)
FREQ. = 1MHz (50% DUTY CYCLE)
AMP. = 2.6V

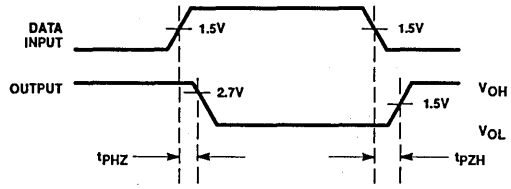
Figure 1. Propagation Delay (Data to Output)



INPUT PULSE:
$t_r = t_f \leq$ 5ns (0.3V TO 2.7V)
FREQ. = 100kHz
AMP. = 2.6V

Figure 2. Propagation Delay ("0" to HI-Z, t_{PLZ}; HI-Z to 0, t_{PZL})

AC TEST CIRCUITS AND WAVEFORMS (Continued)

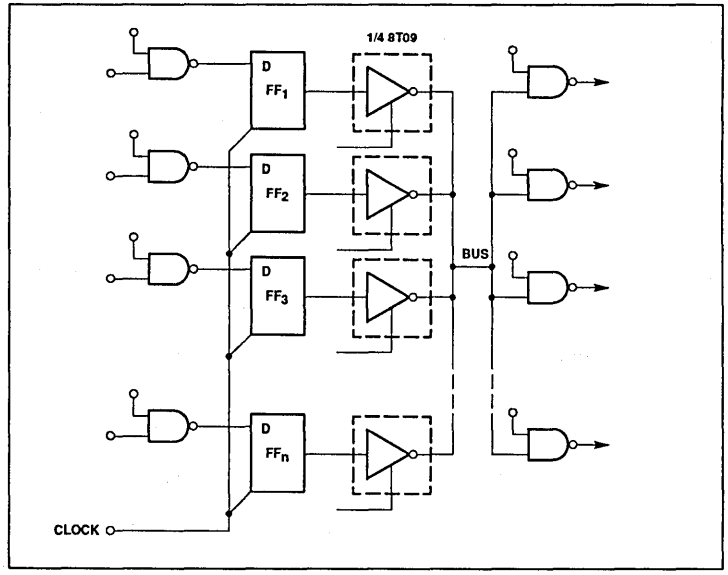


INPUT PULSE:
$t_r = t_f \leq 5ns$ (0.3V TO 2.7V)
FREQ. = 200kHz
AMP. = 2.6V

Figure 3. Propagation Delay ("1" to Hi-Z, t_{PHZ}; Hi-Z to 1, t_{PZH})

TYPICAL APPLICATIONS

The figure to right illustrates usage of the 8T09 in data processing logic. For example, FF_1 thru FF_n may represent bit X in each of several functions in a minicomputer (accumulators, MQ register, index registers, indirect address registers, etc.). Transfer from any source to any load, including transfers from one register to another, can take place along the single path labeled "BUS".



Signetics

8T26A
Bus Transceiver

3-State Quad Bus Transceiver

Product Specification

Military Logic Products

FEATURES
- **High-speed Schottky quad transceiver**
- **32mA Low-state drive**
- **200μA bus loading**
- **Ideal for:**
  - **Half-duplex data transmission**
  - **Memory interface buffers**
  - **Data routing in bus oriented systems**
  - **High current drivers**
  - **MOS/CMOS-to-TTL interface**

DESCRIPTION
The 8T26A consists of four pairs of 3-State logic elements configured as quad bus drivers/receivers, along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the 8T26 from conventional multi-IC implementations. In addition, the 8T26As ultra high-speed while driving heavy bus capacitance (300pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

Both the driver and receiver gates have 3-State outputs and low-current PNP inputs. 3-State outputs provide the high switching speeds of totem-pole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200μA maximum.

ORDERING INFORMATION

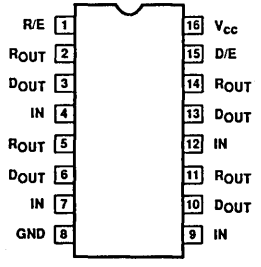
DESCRIPTION	ORDER CODE
Ceramic DIP	8T26A/BEA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

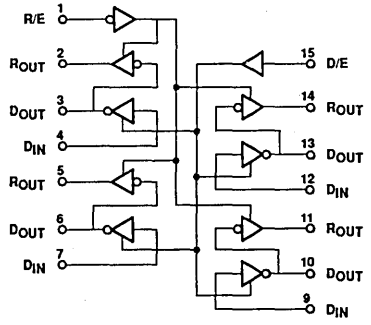
PINS	DESCRIPTION	8T
I_N	Input	0.5SUL
D/E, R/E	Inputs	0.5SUL
D_{OUT}	Output	16SUL
R_{OUT}	Output	6SUL

NOTE: A Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

PIN CONFIGURATION



LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
I_{OL}	Continuous range	100	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				+0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	Driver			-2	µA
I_{OL}	Low-level output current	Driver			32	mA
		Receiver			12	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS		UNIT
				Min	Max	
V_{IH}	Input High voltage	Guaranteed input High threshold voltage		2.0		V
V_{IL}	Input Low voltage	Guaranteed input Low threshold voltage			0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = Min, I_{IK} = -18mA			-1.2	V
V_{BD}	Input breakdown voltage	V_{CC} = Max, I_I = 1mA		5.5		V
V_{OH}	High-level output voltage, Driver outputs	V_{CC} = Min, I_{OH} = -2mA		2.4		V
V_{OH}	High-level output voltage, Receiver outputs	V_{CC} = 5.0V, I_{OH} = -100µA		3.0		V
V_{OL}	Low-level output voltage, Driver outputs	V_{CC} = Min, I_{OL} = 32mA			0.5	V
V_{OL}	Low-level output voltage, Receiver outputs	V_{CC} = Min, I_{OL} = 12mA			0.5	V
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = Max, V_O = 2.4V			100	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = Max, V_O = 0.5V			-100	µA
I_{IH}	High-level input current	V_{CC} = Max, V_I = 4.5V			25	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V	Driver, receiver		-200	µA
			Disabled		-25	µA
I_{OS}	Short-circuit output current[2]	V_{CC} = Max	Driver	-50	-150	mA
			Receiver	-30	-100	mA
I_{CC}	Supply current	V_{CC} = Max			87	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

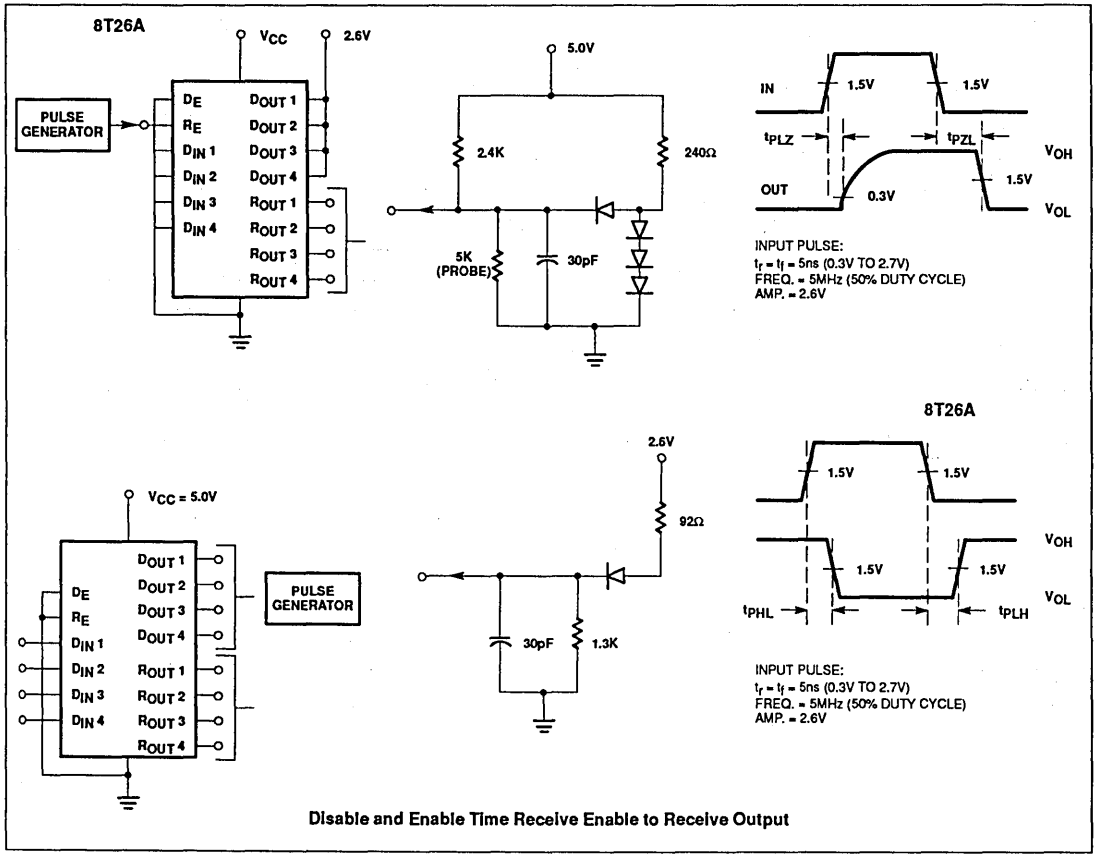
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_{PHL}	Propagation delay, D_{OUT} to R_{OUT}	$C_L = 30pF$		14	ns
t_{PHL}	Propagation delay, D_{IN} to D_{OUT}	$C_L = 300pF$		14	ns
t_{PLH}	Propagation delay, D_{OUT} to R_{OUT}	$C_L = 30pF$		14	ns
t_{PLH}	Propagation delay, D_{IN} to D_{OUT}	$C_L = 300pF$		14	ns
t_{PZL}	Data enable to data output, Hi-Z to 0	$C_L = 300pF$		25	ns
t_{PLZ}	Data enable to data output, 0 to Hi-Z	$C_L = 300pF$		20	ns
t_{PZL}	Receive enable to receive output, Hi-Z to 0	$C_L = 30pF$		20	ns
t_{PLZ}	Receive enable to receive output, 0 to Hi-Z	$C_L = 30pF$		15	ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[3]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			Min	Max	
t_{PHL}	Propagation delay, D_{OUT} to R_{OUT}	$C_L = 30pF$		18	ns
t_{PHL}	Propagation delay, D_{IN} to D_{OUT}	$C_L = 300pF$		18	ns
t_{PLH}	Propagation delay, D_{OUT} to R_{OUT}	$C_L = 30pF$		18	ns
t_{PLH}	Propagation delay, D_{IN} to D_{OUT}	$C_L = 300pF$		18	ns
t_{PZL}	Data enable to data output, Hi-Z to 0	$C_L = 300pF$		35	ns
t_{PLZ}	Data enable to data output, 0 to Hi-Z	$C_L = 300pF$		26	ns
t_{PZL}	Receive enable to receive output, Hi-Z to 0	$C_L = 30pF$		38	ns
t_{PLZ}	Receive enable to receive output, 0 to Hi-Z	$C_L = 30pF$		19	ns

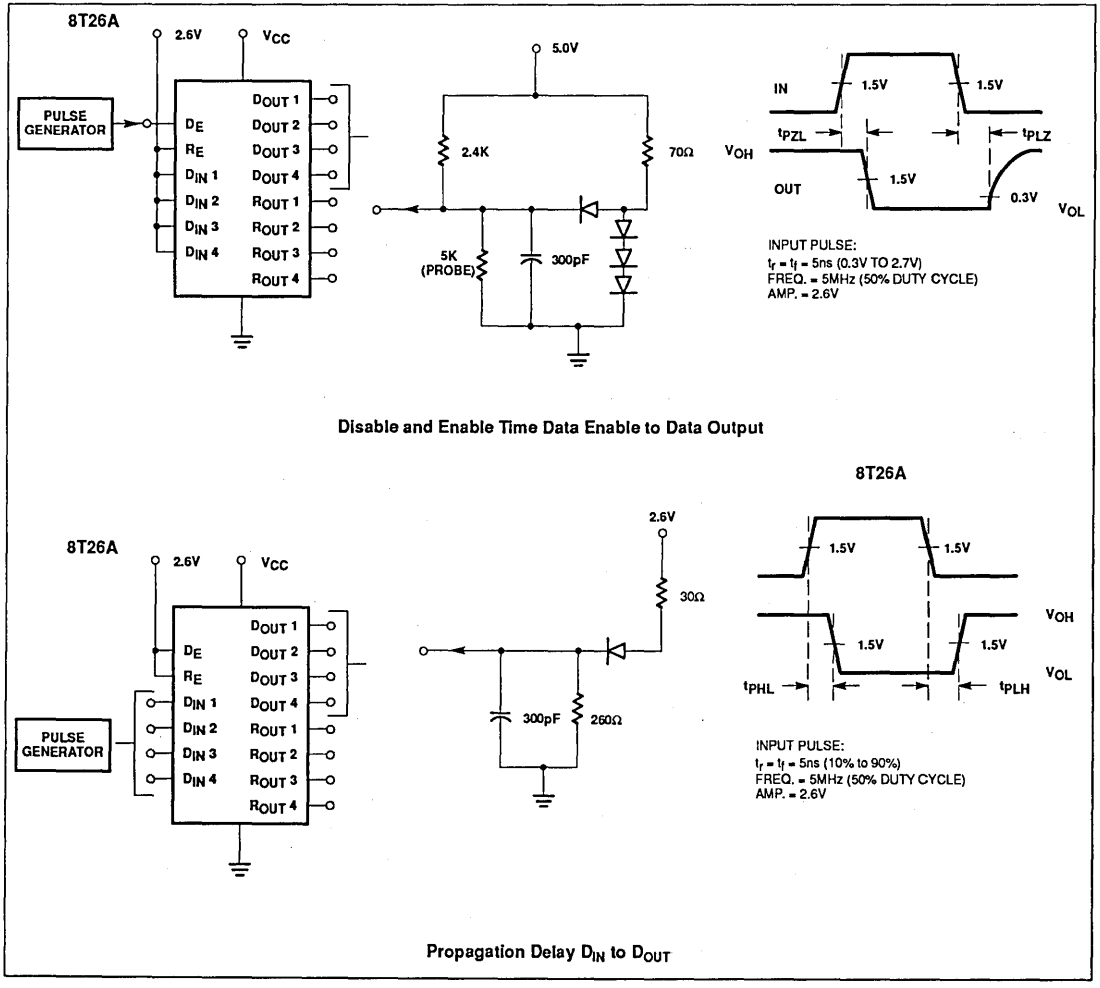
NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
3. These parameters are guaranteed, but not tested.

TEST CIRCUITS AND WAVEFORMS

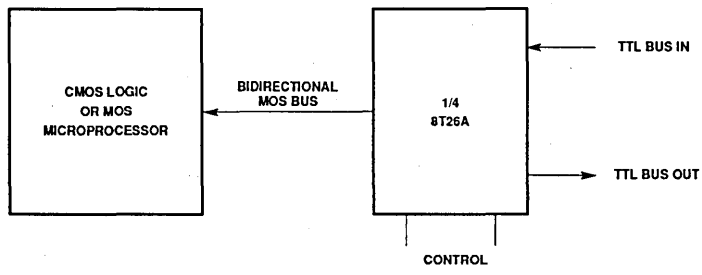


Disable and Enable Time Receive Enable to Receive Output

TEST CIRCUITS AND WAVEFORMS (Continued)

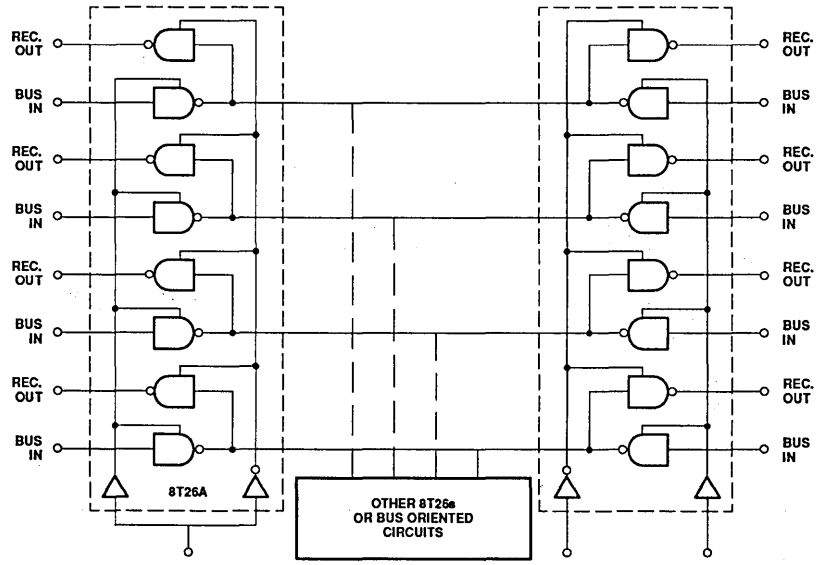


TYPICAL APPLICATION



Bidirectional MOS
CMOS to TTL Interface

TYPICAL APPLICATION



Control lines may be tied together, such that logical "1" transmit, logical "0" receive.
Logical "0" = active
Logical "1" = active
Logical "11" = Hi-Z
Logical "0" = Hi-Z

Bidirectional Data Bus

Signetics

8X60
FIFO RAM Controller (FRC)

Military
Customer Specific Products

Product Specification

FEATURES
- **12-Bit FIFO address generator**
- **Data rate exceeding 8MHz**
- **Asynchronous Read/Write operations**
- **3-State address outputs**
- **User-defined word width**
- **Specifically designed for use with high-speed bipolar RAMs (adaptable for use with MOS RAMs)**
- **TTL input and output**
- **16mA Address-drive capability**

USE AND APPLICATION
- **Interface between independently-clocked systems**
- **Buffer memories for disk and/or tape**
- **Data communication concentrators**
- **CPU/terminal buffering**
- **DMA applications**
- **CRT terminals**

FUNCTIONAL OPERATION
The FRC operates in either of two basic modes — **write** into the FIFO buffer memory or **read** from the FIFO buffer memory. These two operations are described in subsequent paragraphs and the complete sequence is summarized in Table 1. Typical Write/Read timing relationships, arbitration logic, and chip-enable control are shown in the Timing Diagrams.

PRODUCT DESCRIPTION
The Signetics 8X60 FIFO RAM Controller (FRC) is an address and status generator designed to implement a high-speed/high-capacity First-In/First-Out (FIFO) stack utilizing standard off-the-shelf RAMs — see **Applications** on the last page of this data sheet. The FRC can control up to 4096 words of buffer memory; intermediate buffer sizes can be selected — refer to the memory length table on the next page. Built-in arbitration logic handles read/write operations on a first-come/first-serve basis.

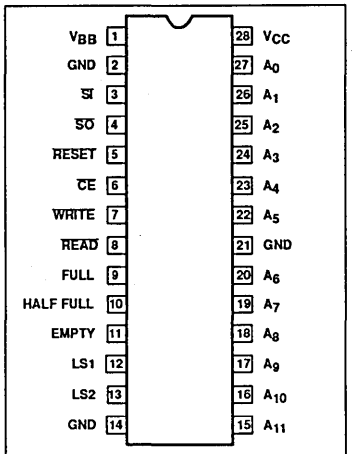
As shown in Figure 1, the FRC consists of:
- A 12-bit write address generation counter (counter #1) and a 12-bit read address generation counter (counter #2).
- A 12-bit up/down status counter (counter #3).
- Twelve 3-State address drivers.
- Control logic.

The two address counters, #1 and #2, respectively, are used to generate write and read addresses; the outputs of these counters are multiplexed to the 3-State address drivers. Counter #3 generates **full, empty**, and **half full** status.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-Pin DIP 600mil-wide	8X60/BXA
28-Pin LLCC	8X60/B3A

PIN CONFIGURATION



PIN NO.	IDENTIFIER	FUNCTION
1	V_{BB}	Supply voltage for internal circuits.
2, 14, 21	GND	Circuit ground.
3	$\overline{SI}$	Shift-In request for write cycle; active-low input.
4	$\overline{SO}$	Shift-Out request for read cycle; active-low input.
5	$\overline{RESET}$	Active-low master reset input.
6	$\overline{CE}$	Active-low chip enable input.
7	$\overline{WRITE}$	Write cycle address valid; active-low output.
8	$\overline{READ}$	Read cycle address valid; active-low output.
9	FULL	Memory full status output; also, override input capability. Active when high.
10	HALF FULL	Memory half-full status output; active-high.
11	EMPTY	Memory empty status output; also, override input capability. Active when high.
12	LS1	Least significant bit (LSB) of the memory length select input.
13	LS2	Most significant bit (MSB) of the memory length select input.
15-20 22-27	A_{11}-A_0	3-State address outputs; A_0 = LSB.
28	V_{CC}	Supply voltage.

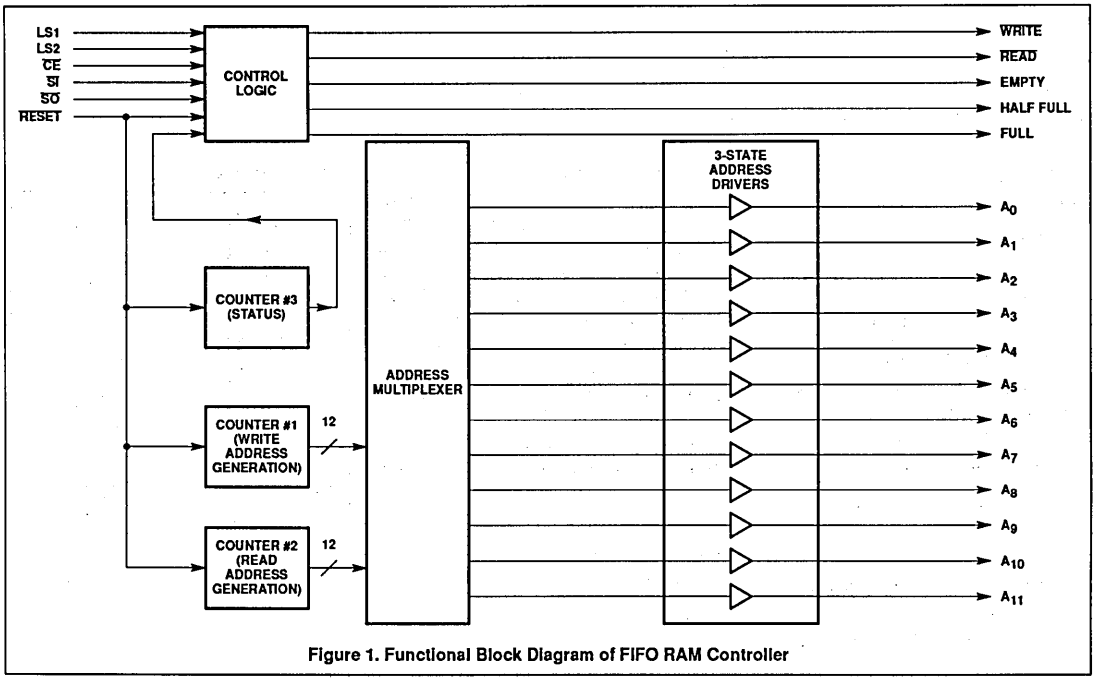


Figure 1. Functional Block Diagram of FIFO RAM Controller

FIFO BUFFER MEMORY — WRITE CYCLE

To perform a write operation, $\overline{SO}$ must be High and SI must be Low. When these conditions exist and other control parameters (Table 1) are satisfied, the write address in Counter #1 (Figure 1) is output to the address bus via the multiplexer and $\overline{WRITE}$ output goes Low. (**Note**. Normally, the $\overline{WRITE}$ output goes Low after the address output becomes state — refer to **WRITE Cycle Timing Diagram**. The $\overline{WRITE}$ output may then act as a **write** or **chip** enable for the RAMs that are used to implement the memory.

When the **write** cycle is ended ($\overline{SI}$ is forced High), the $\overline{WRITE}$ output goes High, the address output buffers return to a High- impedance state. Counter #1 (Write Address Generation) and Counter #3 (Status) are both incremented, and Counter #2 (Read Address Generation) remains unchanged.

FIFO BUFFER MEMORY - READ CYCLE

To perform a read operation, $\overline{SI}$ must be High and $\overline{SO}$ must be Low. When these conditions exist and other control parameters (Table 1) are satisfied, the read address contained in Counter #2 (Figure 1) is output to the address bus and the $\overline{READ}$ output goes Low. When the **read** cycle is ended ($\overline{SO}$ is forced High) the $\overline{READ}$ output goes High, the output buffers return to a High-impedance state. Counter #2 (Read Address Generation) is incremented. Counter #3 (Status) is decremented, and Counter #1 (Write Address Generation) remains unchanged.

MEMORY LENGTH

LS1	LS2	HALF LENGTH	FULL LENGTH
L	L	2048	4096
H	L	32	64
L	H	512	1024
H	H	128	256

CONTROL LOGIC

To prevent the possibility of operational conflicts, $\overline{SI}$ and $\overline{SO}$ are treated on a first-come/first-served basis; these two input signals are controlled by internal arbitration logic — refer to the applicable **Timing Diagrams** and **AC Characteristics** for functional and timing relationships. If one cycle is requested while the other cycle is in progress, the requested cycle will commence as soon as the current-cycle is complete (provided other control parameters are satisfied).

As shown in the accompanying diagram, the buffer length of the FIFO memory can be hardware-selected via the Length Select (LS1, LS2) Inputs. When less than the maximum length is selected, the unused High-order bits of the address outputs are held in the High-impedance state.

Generation of the status output signals (HALF FULL, FULL and EMPTY) is a function of the Length Select (LS1, LS2) inputs and the current state of Status Counter #3. In general, the status outputs reflect the conditions that follow:

- **HALF FULL** — this status output signals goes High on the positive-going edge of $\overline{SI}$ if the MSB of the selected length of Counter #3 becomes a "1". The HALF FULL signal will go from High-to-Low on the positive-going edge of $\overline{SO}$ when, after the **read** cycle, the selected length of Counter #3 changes from "100 ... 00" to "011 ... 11". For example, if the selected memory length is 256 words (FULL = 256), then HALF FULL = 128 words; hence, on the positive-going edge of $\overline{SO}$ when Counter #3 reaches a count of 127, the HALF FULL output will go from High-to-Low.

FIFO RAM Controller (FRC) 8X60

- **FULL** — this signal serves both as a status output and as an override input. The FULL signal goes High on the negative-going edge of $\overline{SI}$ if all bits of Counter #3 for selected length are equal to "1". The FULL output goes from High-to-Low on the negative-going edge of $\overline{SO}$.
- **EMPTY** — this signal also serves as a status output and as an override input. On the negative-going edge of $\overline{SO}$, the EMPTY output is driven High if Status Counter #3 contains a value of "1"; on the positive-going edge of $\overline{SO}$, the counter is decremented to "0". The EMPTY output goes from High-to-Low on the negative-going edge of $\overline{SI}$.

Once the FULL signal is High, further Write Cycle Requests ($\overline{SI}$ = low) are ignored; similarly, once the EMPTY signal is High, further Read Cycle requests ($\overline{SO}$ = low) are ignored. However, to accommodate diversified applications, the FULL and EMPTY outputs are open-collector with on-chip 4.7K passive pull-up resistors. If either the FULL or EMPTY pins are forced Low via external control, the corresponding **write** or **read** cycle may resume (provided external FULL or EMPTY input is held Low until the corresponding $\overline{WRITE}$ or $\overline{READ}$ output goes Low) and the address/status counters will continue normal operation* — refer to Table 1.

The user must force the $\overline{RESET}$ input Low to initialize the chip. (**Note.** If the $\overline{RESET}$ signal is driven Low during a **write** or **read** cycle, the address output may have a short period of uncertainty before assuming a high-impedance state.) The following actions occur when $\overline{RESET}$ is active:

- All internal counters are set to "0".
- All address output lines are forced to the high-impedance state.
- HALF FULL and FULL outputs are forced Low.
- $\overline{WRITE}$, $\overline{READ}$, and EMPTY outputs are forced high.

When $\overline{CE}$ is High, the address output lines are forced to the high-impedance state, further **write** or **read** cycle requests are ignored, and all counters remain unchanged. If $\overline{CE}$ switches from Low-to-High during a **write** or **read** cycle, the cycle in progress is always completed before the disabled state is entered. For details of these operations, refer to the timing information shown later in this data sheet.

* Refer to **Note** on inside back cover

Table 1. Summary of Operation

INPUTS				INITIAL	RESULTING OUTPUTS			COMMENTS
$\overline{RESET}$	$\overline{CE}$	$\overline{SI}$	$\overline{SO}$	CONDITIONS	$\overline{WRITE}$	$\overline{READ}$	Address Bus	
L	X	X	X		H	H	Hi-Z	Reset all counters to 0.
H	X	H	H		H	H	Hi-Z	No action
H	L	L	H	FULL = L	L	L	Write address from Ctr #1	Shift into FIFO stack (Write Cycle)
H	L	L	H	FULL = H	H	H	Hi-Z	Stack full (write inhibited)
H	L	H	L	EMPTY = L	H	L	Read address from Ctr #2	Shift out of FIFO stack (Read Cycle)
H	L	H	L	EMPTY = H	H	H	Hi-Z	Stack empty (read inhibited)
H	L	L	↓	Write cycle in progress	L	H	Write address from Ctr #1	Continue write cycle (until $\overline{SI}$ goes high)
H	L	↓	L	Read cycle in progress	H	L	Read address from Ctr #2	Continue read cycle (until $\overline{SO}$ goes high)
H	L	L	L	EMPTY = H	L	H	Write address from Ctr #1	Shift in (read inhibited)
H	L	L	L	FULL = H	H	L	Read address from Ctr #2	Shift out (write inhibited)
H	L	↑	H	Write cycle in progress	↑	H	Goes to Hi-Z	Increment write address counter #1 and status counter #3
H	L	H	↑	Read cycle in progress	H	↑	Goes to Hi-Z	Increment read address counter #2; decrement status counter #3
H	L	↑	L	Write cycle in progress[1]	↑	↓	Changes to read address from Ctr #2	Increment write address counter #1 and status counter #3
H	L	L	↑	Read cycle in progress[2]	↓	↑	Changes to write address from Ctr #1	Increment read address counter #2; decrement status counter #3
H	H	↓	H		H	H	Hi-Z	Chip disabled
H	H	H	↓		H	H	Hi-Z	Chip disabled
H	↑	L	X	FULL = L; write cycle begun[1]	L	H	Write address from Ctr #1	Continue write cycle (until $\overline{SI}$ goes high)
H	↑	L	X	EMPTY = L; read cycle begun[2]	H	L	Read address from Ctr #2	Continue read cycle (until $\overline{SO}$ goes high)
H	↓	L	L	FULL = L; EMPTY = L	-	-	-	This set of conditions should be avoided

NOTES:
1. Write cycle will occur if either $\overline{SI}$ goes Low before $\overline{SO}$ goes Low or EMPTY = H when $\overline{SO}$ goes Low.
2. Read cycle will occur if either $\overline{SO}$ goes Low before $\overline{SI}$ goes Low or FULL = H when $\overline{SI}$ goes Low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{BB}	Supply voltage for internal circuits	+4	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Off-state output voltage	+5.5	V_{DC}
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V, -55°C \leq T_C \leq +125°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{IH}	High level input voltage[3]		2.0			V
V_{IL}	Low level input voltage				0.8	V
V_{OH}	High level output voltage: All outputs except FULL and EMPTY	V_{CC} = Min; I_{OH} = -2.6mA	2.5			V
V_{OL}	Low level output voltage: Address Bus, WRITE, READ	V_{CC} = Min; I_{OL} = 16mA		0.38	0.5	V
V_{OL}	HALF FULL, FULL, and EMPTY	V_{CC} = Min; I_{OL} = 8mA		0.35	0.5	V
V_{IK}	Diode clamp voltage: All inputs except FULL and EMPTY	V_{CC} = Min; I_{IK} = -18mA		-0.8	-1.5	V
I_{IH}	High level input current: All inputs except FULL and EMPTY	V_{CC} = Max; V_{IH} = 2.7V		0.1	20	µA
I_{IH}	FULL and EMPTY	V_{CC} = Max; V_{IH} = 2.7V; stack FULL or stack EMPTY[3]		-470	-900	µA
I_{IL}	Low level input current: All inputs except FULL and EMPTY	V_{CC} = Max; V_{IL} = 0.4V		-0.17	-0.4	mA
I_{IL}	FULL and EMPTY	V_{CC} = Max; V_{IL} = 0.4V; Stack FULL or Stack EMPTY		-1.12	-1.8	mA
I_{OH}	High level output current: FULL, EMPTY	V_{CC} = Min; V_{OH} = V_{CC} (Min)		15	100	µA
I_{OZH}	Hi-Z output current (HIGH); address bus (3-State)	V_{CC} = Max; V_{OUT} - 2.4V		0.9	20	µA
I_{OZL}	Hi-Z output current (LOW); address bus (3-State)	V_{CC} = Max; V_{OUT} = 0.5V		-0.6	-20	µA
I_I	Input leakage current: All inputs except FULL and EMPTY	V_{CC} = Max; V_{IN} = 5.5V		0.03	0.1	mA
I_{OS}	Short-circuit output current: address bus and HALF FULL	V_{CC} = Max; V_{OH} = 0V	-15	-68	-100	mA
I_{OS}	WRITE, READ	V_{CC} = Max; V_{OH} = 0V	-40	-73	-100	mA
I_{CC}	Supply current from V_{CC}	V_{CC} = Max; Address Bus = Hi-Z; -55°C →		81	140	mA
		+25°C →		81	122	mA
		+125°C →		81	100	mA
I_{BB}	Supply current from V_{BB}	V_{BB} = Max; -55°C →		63	100	mA
		+25°C →		63	95.5	mA
		+125°C →		63	90	mA

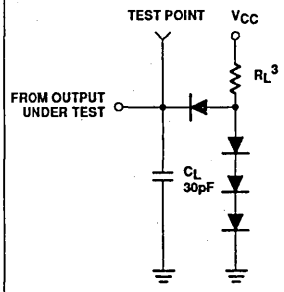
AC ELECTRICAL CHARACTERISTICS $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_C \le +125°C$

SYMBOL	PARAMETERS	REFERENCES		TEST CONDITIONS	LIMITS			UNIT
		From	To		Min	Typ	Max	
Pulse Widths								
T_{LH}	$\overline{SI}$ high	↑$\overline{SI}$	↓$\overline{SI}$	Stack approaching FULL[4]	30	13		ns
T_{DH}	$\overline{SO}$ high	↑$\overline{SO}$	↓$\overline{SO}$	Stack approaching EMPTY[4]	30	16		ns
Write Cycle Timing								
T_{LA}	Address stable delay	↓$\overline{SI}$	An	FULL = Low; $\overline{SO}$ = High		40	60	ns
T_{AW}	Address lead time	An	↓$\overline{WRITE}$		0			ns
T_{LAW}	$\overline{WRITE}$ output active delay	↓$\overline{SI}$	↓$\overline{WRITE}$	FULL = Low; $\overline{SO}$ = High	40	51	77	ns
T_{LW}	$\overline{WRITE}$ output inactive delay	↑$\overline{SI}$	↑$\overline{WRITE}$			3	10	ns
T_{WA}	Address lag time	↑$\overline{WRITE}$	An		20	34		ns
T_{LT}	Address output disable	↑$\overline{SI}$	An (Hi-Z)			37	65	ns
T_{LF}	FULL status active delay	↓$\overline{SI}$	↑FULL	Stack approaching FULL: $\overline{SO}$ = High		39	70	ns
T_{LE}	EMPTY status inactive delay	↓$\overline{SI}$	↓EMPTY	Stack = EMPTY		40	70	ns
T_{HFH}	HALF-FULL status active delay	↑$\overline{SI}$	↑HALF FULL	Stack approaching HALF-FULL		30	50	ns
T_{DW}	$\overline{WRITE}$ output active after read	↑$\overline{SO}$	↓$\overline{WRITE}$	Both $\overline{SI}$ & $\overline{READ}$ = Low		74	110	ns
Read Cycle Timing								
T_{DA}	Address stable delay	↓$\overline{SO}$	An	EMPTY = Low; $\overline{SI}$ = High		40	60	ns
T_{AR}	Address lead time	An	↓$\overline{READ}$		-5			ns
T_{DAR}	$\overline{READ}$ output active delay	↓$\overline{SO}$	↓$\overline{READ}$	EMPTY - Low; $\overline{SI}$ - High		48	75	ns
T_{DR}	$\overline{READ}$ output inactive delay	↑$\overline{SO}$	↑$\overline{READ}$			5	10	ns
T_{RA}	Address lag time	↑$\overline{READ}$	An		10	32		ns
T_{DT}	Address output disable	↑$\overline{SO}$	An (Hi-Z)			37	70	ns
T_{DE}	EMPTY status active delay	↓$\overline{SO}$	↑EMPTY	Stack approaching EMPTY; $\overline{SI}$ = High		38	50	ns
T_{DF}	FULL status inactive delay	↓$\overline{SO}$	↓FULL	Stack = FULL		38	65	ns
T_{HFL}	HALF-FULL status inactive delay	↑$\overline{SO}$	↓HALF FULL	Stack exactly HALF-FULL		54	85	ns
T_{LR}	$\overline{READ}$ output active after write	↑$\overline{SI}$	↓$\overline{READ}$	Both $\overline{SO}$ & $\overline{WRITE}$ = Low		70	100	ns
Chip Enable Timing (Write)								
T_{HEW}	Chip enable hold time[5]	↓$\overline{SI}$	↑$\overline{CE}$	FULL = Low; $\overline{SO}$ = High		1	10	ns
T_{SEW}	Chip disable set-up time[6]	↑$\overline{CE}$	↓$\overline{SI}$	FULL = Low; $\overline{SO}$ = High	10	1		ns
T_{PEW}	Chip enable delay time	↓$\overline{CE}$	↓$\overline{WRITE}$	FULL = Low; $\overline{SI}$ = Low; $\overline{SO}$ - High		69	110	ns
Chip Enable Timing (Read)								
T_{HER}	Chip enable hold time[5]	↓$\overline{SO}$	↑$\overline{CE}$	EMPTY = Low; $\overline{SI}$ = High		1	12	ns
T_{SER}	Chip disable set-up time[6]	↑$\overline{CE}$	↓$\overline{SO}$	EMPTY = Low; $\overline{SI}$ = High	10	1		ns
T_{PER}	Chip enable delay time	↓$\overline{CE}$	↓$\overline{READ}$	EMPTY = Low; $\overline{SO}$ = Low; $\overline{SI}$ = High		64	105	ns
Reset Timing								
T_{RR}	$\overline{RESET}$ recovery	↑$\overline{RESET}$	↓$\overline{WRITE}$	$\overline{SI}$ = Low		57	85	ns
T_{RL}	$\overline{RESET}$ pulse width (low)	↓$\overline{RESET}$	↑$\overline{RESET}$		25	8		ns
Full/Empty Override Timing								
T_{FW}	Override recovery for FULL	↓FULL	↓$\overline{WRITE}$	Stack = Full; $\overline{SI}$ = Low; $\overline{SO}$ = High		70	110	ns
T_{ER}	Override recovery for EMPTY	↓EMPTY	↓$\overline{READ}$	Stack = EMPTY; $\overline{SO}$ = Low; $\overline{SI}$ = High		65	105	ns

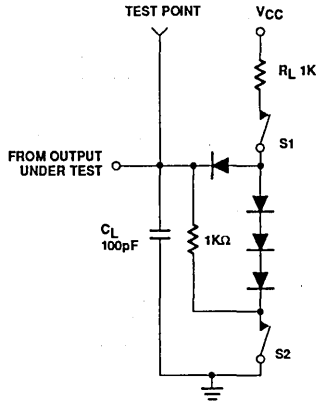
NOTES:
1. V_{BB} should be obtained from a regulated 1.5V supply.
2. Typical limits are: V_{CC} = 5.0V; T_A = 25°C.
3. Because of the internal pull-up resistor on the FULL and EMPTY pins, a negative current is required to force the required voltage.
4. Such that write/read request is inhibited after stack becomes full/empty.
5. The earliest rising edge of $\overline{CE}$ such that the $\overline{WRITE}$ or $\overline{READ}$ output always occurs.
6. The latest rising edge of $\overline{CE}$ such that the $\overline{WRITE}$ or $\overline{READ}$ output never occurs.

AC TEST CIRCUITS

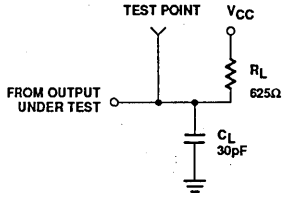
APPLICABLE PINS: WRITE (7), READ (8), HALF FULL (10)



APPLICABLE PINS: An (15-20, 22-27)



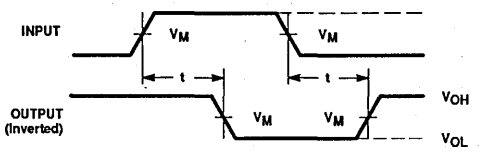
APPLICABLE PINS: FULL (8) AND EMPTY (11)



OUTPUT STATE		SWITCH POSITION	
FROM	TO	S1	S2
Low	High	Closed	Closed
High	Low	Closed	Closed
High	Hi-Z	Closed	Closed
Low	Hi-Z	Closed	Closed
Hi-Z	High	Open	Closed
Hi-Z	Low	Closed	Open

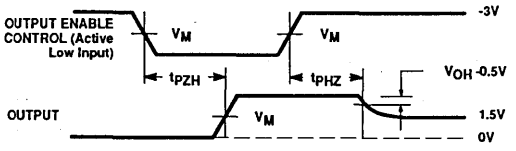
NOTES:
1. In all cases C_L includes probe and jig capacitance.
2. All diodes are 1N916, 1N3064, or equivalent.
3. For READ and WRITE outputs R_L = 280Ω; for HALF FULL output, R_L = 2kΩ.

AC TEST WAVEFORMS

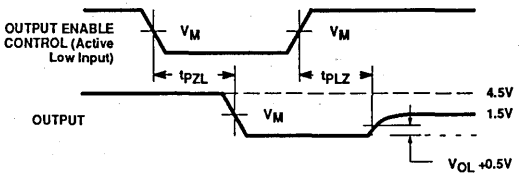


NOTE: Pulse widths and Setup/Hold times are measured using the same reference points as above waveform.

Propagation Delay
(Typical Example)



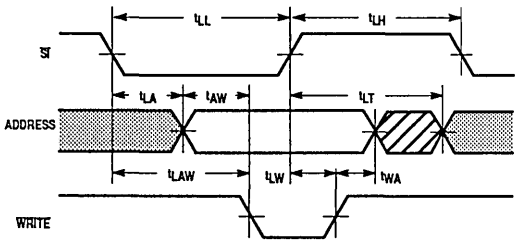
3-State Enable Time to Low Level and Disable Time from Low Level



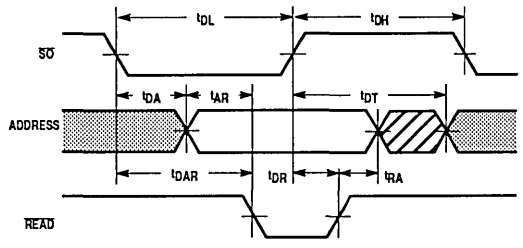
3-State Enable Time to High Level and Disable Time from High Level

NOTE: For all waveforms, V_M = 1.5

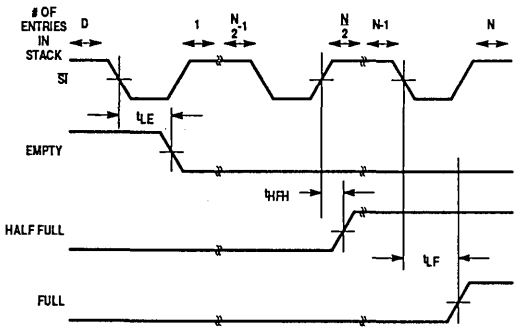
TIMING DIAGRAMS



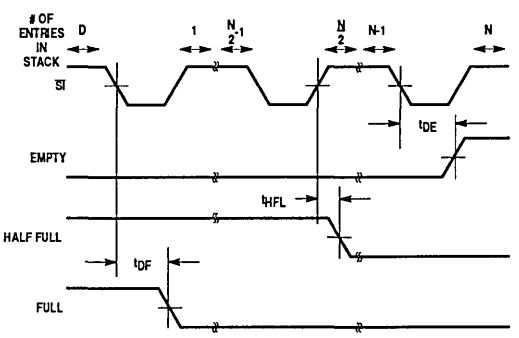
Write Cycle Timing



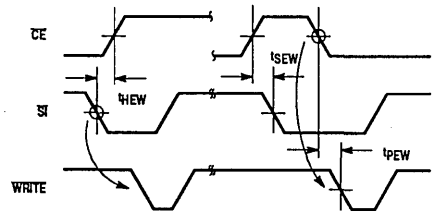
Read Cycle Timing



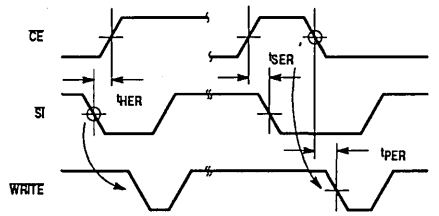
Status Output Timing-Write



Status Output Timing-Read



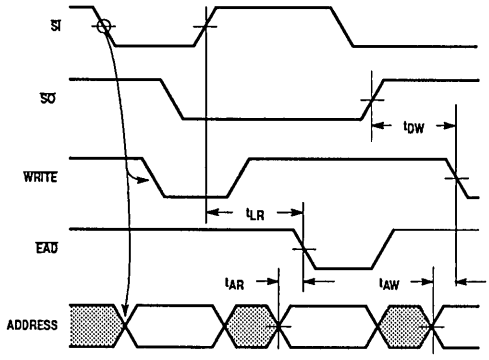
Chip Enable Timing Write *



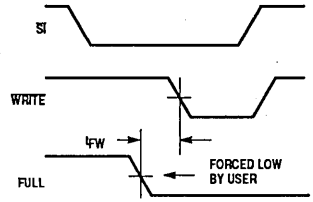
Chip Enable Timing Read[1]

NOTE:
The rising edge of $\overline{CE}$ should not occur within 10-nanoseconds before or after a falling edge of $\overline{SI}$ or $\overline{SO}$.

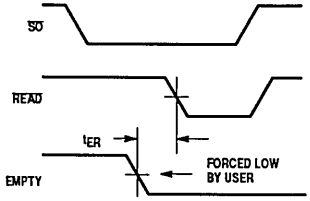
TIMING DIAGRAMS (Continued)



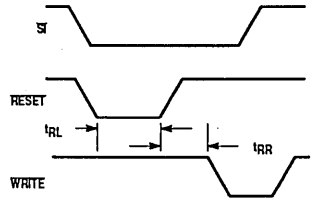
Change of Cycle Timing



Full Override Timing



Empty Override Timing



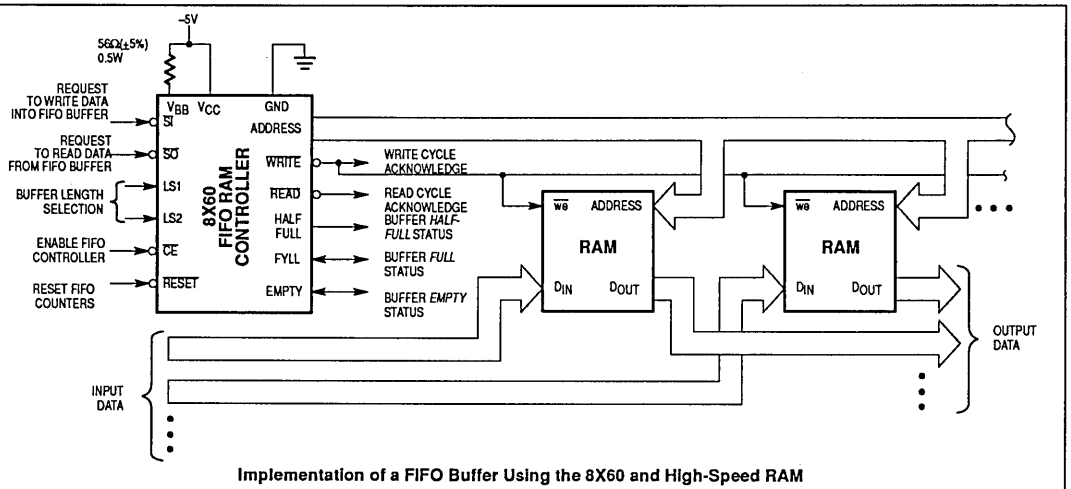
Reset Timing

KEY:

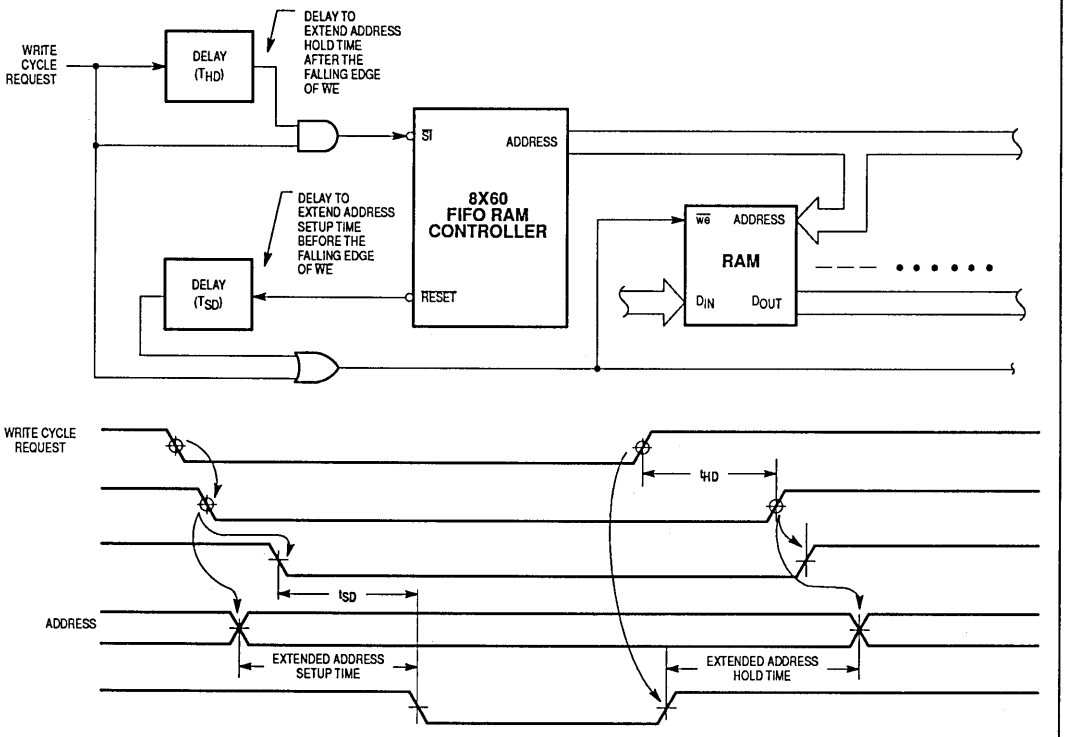
High-impedance state

Changing data

APPLICATIONS



Implementation of a FIFO Buffer Using the 8X60 and High-Speed RAM



Using 8X60 With High-Density MOS RAMs

Signetics

Section 5
RAM Data Sheets

Military Products

INDEX

Signetics

82S09

576-Bit TTL Bipolar RAM (64 × 9)

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch pad, push down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09 features Open collector outputs, chip enable input, and a very low current PNP input structure to enhance memory expansion.

FEATURES

- **Address access time: 80ns max**
- **Write cycle time: 80ns max**
- **Input loading: -150μA max**
- **On-chip address decoding**
- **Schottky clamped**
- **Fully TTL compatible**
- **Output is Non-Blanked during Write**
- **One chip enable input**
- **Outputs: Open collector**

APPLICATIONS

- **Buffer memory**
- **Control register**
- **FIFO memory**
- **Push down stack**
- **Scratch pad**

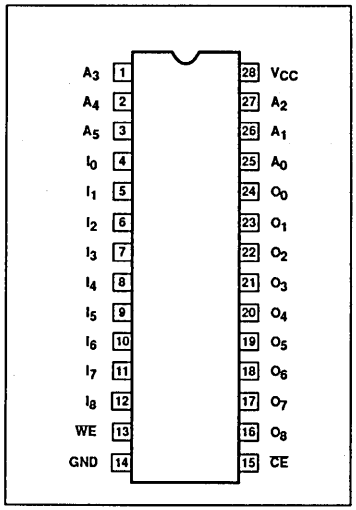
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Ceramic Dual-In-Line 600mil-wide	82S09/BXA
28-pin Ceramic Flat Pack	82S09/BYA

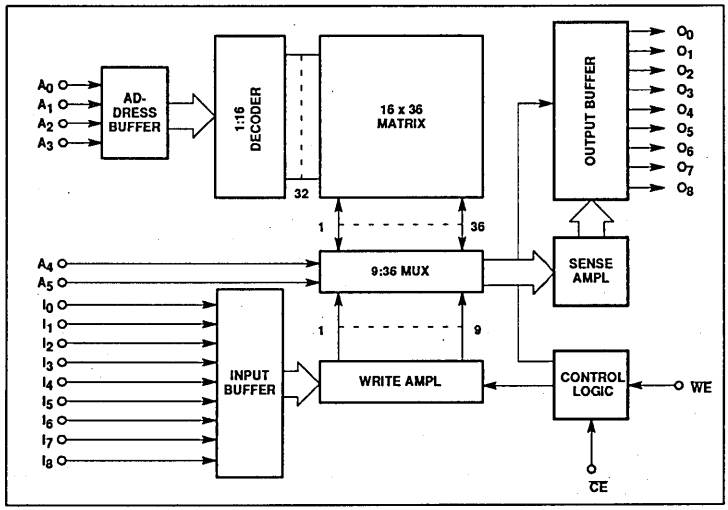
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High	+5.5	V_{DC}
T_A	Operating temperature range[7]	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



576-Bit TTL Bipolar RAM (64 × 9) — 82S09

DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C[7], 4.75V ≤ V_{CC} ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
Input voltage[1]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.2			V
V_{IK}	Clamp[2]	V_{CC} = 4.75V, I_I = -18mA			-1.5	V
Output voltage[1]						
V_{OL}	Low[3]	V_{CC} = 4.75V I_{OL} = 8.0mA			0.5	V
Input current						
I_{IL}	Low	V_{CC} = 5.25V V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
I_{CLK}	Leakage[4]	V_{CC} = 5.25V V_O = 5.5V			60	µA
Supply current[5]						
I_{CC}		V_{CC} = 5.25V			200	mA
Capacitance[8]						
C_{IN}	Input	V_{CC} = 5.0V V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	I_N	O_N
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	1

X = Don't care

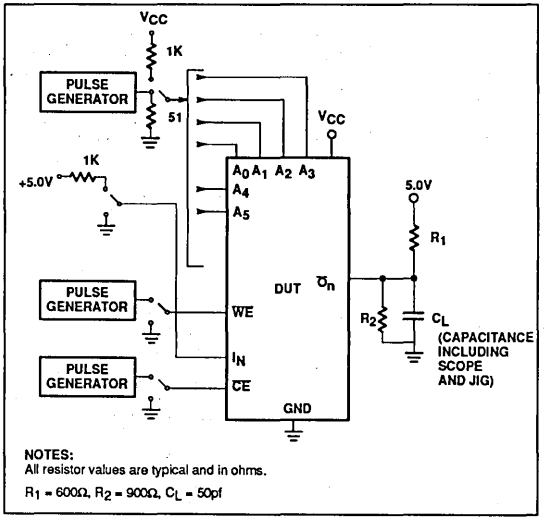
AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C[7], 4.75V ≤ V_{CC} ≤ 5.25V

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
t_{AA}	Address access time					80	ns
t_{CE}	Chip Enable access time					50	ns
t_{CD}	Disable time	Output	Chip Enable			50	ns
t_{WA}	Valid disable time	Output	Write Enable			80	ns
t_{WSA}	Setup time	Write Enable	Address	10			ns
t_{WHA}	Hold time			15			ns
t_{WSD}	Setup time	Write Enable	Data in	50			ns
t_{WHD}	Hold time			5			ns
t_{WSC}	Setup time	Write Enable	$\overline{CE}$	10			ns
t_{WHC}	Hold time			10			ns
t_{WP}	Write Enable pulse width[6]			50			ns

NOTES:
1. All voltage values are with respect to network ground.
2. Test each input one at a time.
3. Measured with the logic low stored. Output sink current is applied through a resistor to V_{CC}.
4. Measured with V_{IH} applied to $\overline{CE}$.
5. I_{CC} is measured with the write enable and chip enable input grounded, all other inputs at 4.5V, and the outputs open.
6. Minimum required to guarantee a Write into the slowest bit.
7. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
8. Guaranteed, but not tested.

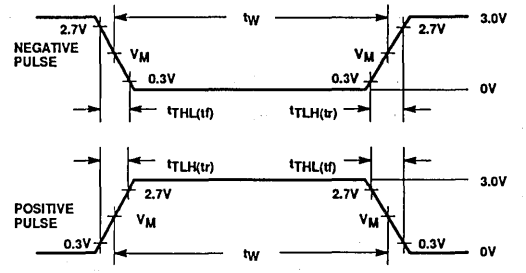
576-Bit TTL Bipolar RAM (64 × 9) — 82S09

TEST LOAD CIRCUIT



NOTES:
All resistor values are typical and in ohms.
R_1 = 600Ω, R_2 = 900Ω, C_L = 50pf

VOLTAGE WAVEFORMS

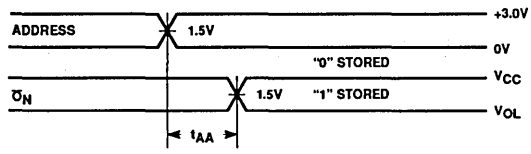


Input Pulse Definition

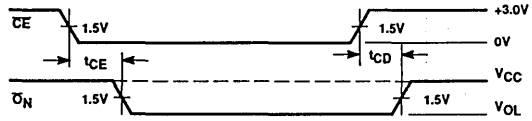
INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

576-Bit TTL Bipolar RAM (64 × 9) — 82S09

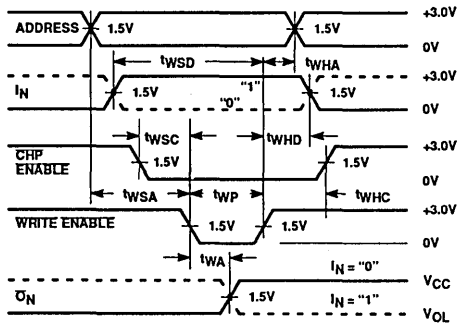
TIMING DIAGRAMS



Read Cycle



Address Access Time
Chip Enable/Disable Times



Write Cycle

MEMORY TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
t_{AA}	Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
t_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
t_{WHD}	Required delay between end of Write Enable pulse and end of valid input Data.
t_{WP}	Width of Write Enable pulse.
t_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.
t_{WSD}	Required delay between beginning of valid Data input and end of Write Enable pulse.
t_{WD}	Delay between beginning of Write Enable pulse and when Data Output goes high (blanks).
t_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
t_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.
t_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming address still valid.)
t_{WA}	Delay between beginning of Write Enable pulse and when data output reflects complement of data input.

Signetics

82S16
256-Bit TTL Bipolar RAM

Military
Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S16 is a Read/Write memory array which features 3-State outputs for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading.

During Write operation the logical state of the output follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

The 82S16 has fast Read access and Write cycle times, and thus is ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

FEATURES

- **Address access time: 70ns max**
- **Write cycle time: 70ns max**
- **Input loading: -250mA max**
- **Output follows complement of data input during Write**
- **Three chip enable inputs**
- **On-chip address decoding**
- **Output: 3-State**
- **Schottky clamped**
- **TTL compatible**

APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

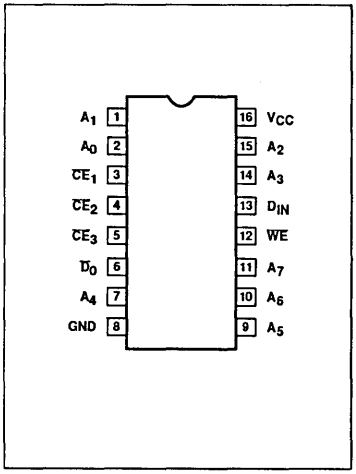
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic Dual-In-Line 300mil-wide	82S16/BEA
Ceramic Flat Pack	82S16/BFA

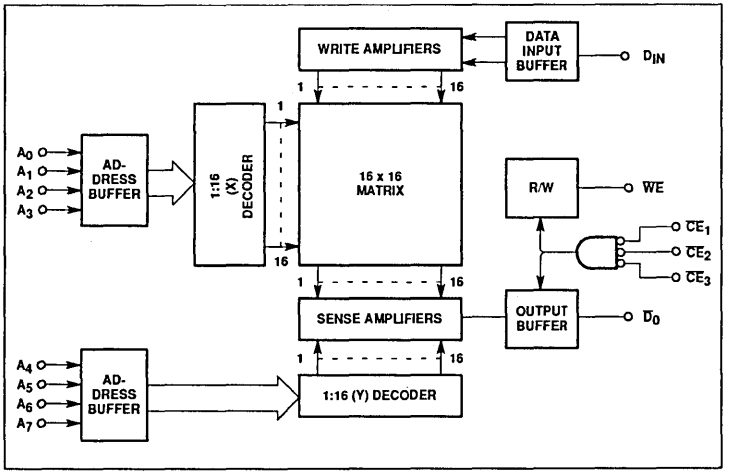
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V
V_I	Input voltage	+5.5	V
V_O	Output voltage High	+5.5	V
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar RAM (256 × 1) — 82S16

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage[2]						
V_{IH}	High		2.0			V
V_{IL}	Low				0.8	V
V_{IK}	Clamp[3]	V_{CC} = 4.75V, I_I = -18mA		-1.0	-1.5	V
Output voltage[2]						
		V_{CC} = 4.75V				
V_{OH}	High	I_{OH} = -3.2mA	2.4			V
V_{OL}	Low[5]	I_{OL} = 16mA		0.35	0.5	V
Input current[3]						
		V_{CC} = 5.25V				
I_{IH}	High	V_I = 5.5V		1	25	µA
I_{IL}	Low	V_I = 0.45V		-10	-250	µA
Output current						
		V_O = 5.5V		1	50	µA
I_{OZ}	Hi-Z State[6]	V_O = 0.45V		-1	-50	µA
I_{OS}	Short circuit[7]	V_{CC} = 5.25V, V_O = 0V	-15		-70	µA
Supply current[8]						
I_{CC}		V_{CC} = 5.25V		80	120	mA
Capacitance[10]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	D_{OUT}
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	Hi-Z

* "0" = All $\overline{CE}$ inputs Low: "1" = One or more $\overline{CE}$ inputs High. X = Don't care.

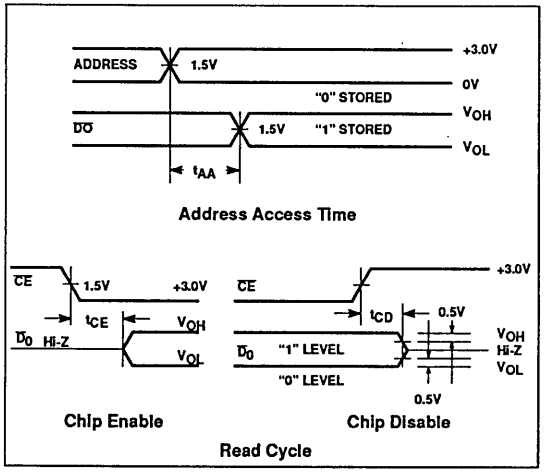
256-Bit TTL Bipolar RAM (256 × 1) — 82S16

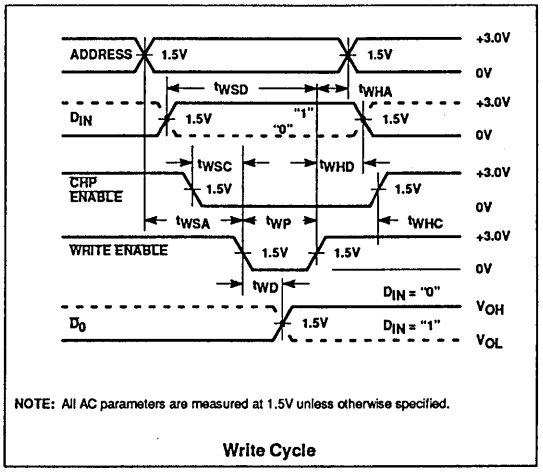
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.75V \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[1]	Max	
t_{AA}	Address access time	Output	Address		40	70	ns
t_{CE}	Chip enable access time	Output	Chip enable		30	40	ns
t_{CD}	Disable time[10]	Output	Chip enable		30	40	ns
t_{WD}	Valid time disable time[10]	Output	Write enable		30	55	ns
t_{WSA}	Setup time	Write enable	Address	20	5		ns
t_{WHA}	Hold time			10	0		ns
t_{WSD}	Setup time	Write enable	Data in	50	30		ns
t_{WHD}	Hold time			10	0		ns
t_{WSC}	Setup time	Write enable	$\overline{CE}$	10	0		ns
t_{WHC}	Hold time			10	0		ns
t_{WP}	Write enable pulse width[9]			40	15		ns

NOTES:
1. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE}1$, $\overline{CE}2$, and $\overline{CE}3$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE}1$, $\overline{CE}2$, and $\overline{CE}3$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.0V and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. Guaranteed, but not tested.

TIMING DIAGRAMS





MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of chip enable low (with address valid) and when data output becomes valid.

T_{CD} Delay between when chip enable becomes high and data output is in off state.

T_{AA} Delay between beginning of valid address (with chip enable low) and when data output becomes valid.

T_{WSC} Required delay between beginning of valid chip enable and beginning of Write enable pulse.

T_{WHD} Required delay between end of Write enable pulse and of valid input data.

T_{WP} Width of Write enable pulse.

T_{WSA} Required delay between beginning of valid address and beginning of Write enable pulse.

T_{WSD} Required delay between beginning of valid data input and end of Write enable pulse.

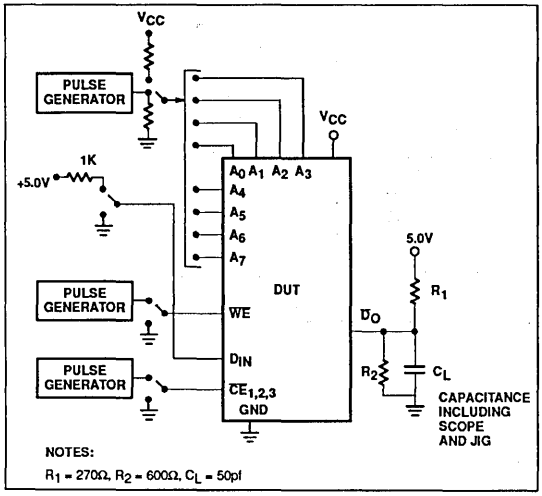
T_{WD} Delay between beginning of Write enable pulse and when data output reflects complement of data input.

T_{WHC} Required delay between end of Write enable pulse and end of chip enable.

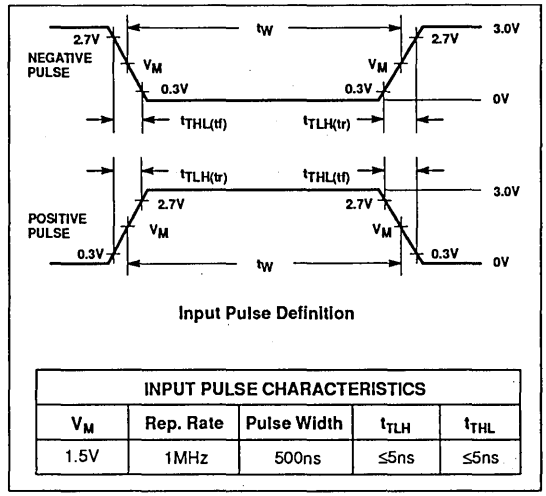
T_{WHA} Required delay between end of Write enable pulse and end of valid address.

256-Bit TTL Bipolar RAM (256 × 1) — 82S16

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Signetics

82S212/82S212-40

2304-Bit TTL Bipolar RAM (256 × 9)

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The organization of the 82S212-40 allows byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used a a tag for each word stored. The 82S212-40 is ideal for scratch pads, push down stacks, buffer memories, and other internal memory applications in which space and performance requirements dictate a wide data path in favor of word depth.

Data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of Read/Write operations using a common bus.

-55°C operation can be guaranteed after a 60 second warmup.

FEATURES

- **Address access time: 70ns max**
- **Schottky clamped TTL**
- **One chip enable input**
- **Common I/O**
  - **Inputs: PNP Buffered**
  - **Outputs: 3-State**

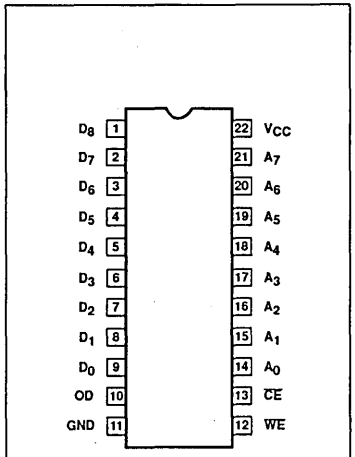
APPLICATIONS

- **Cache memory**
- **Buffer storage**
- **Writable control store**

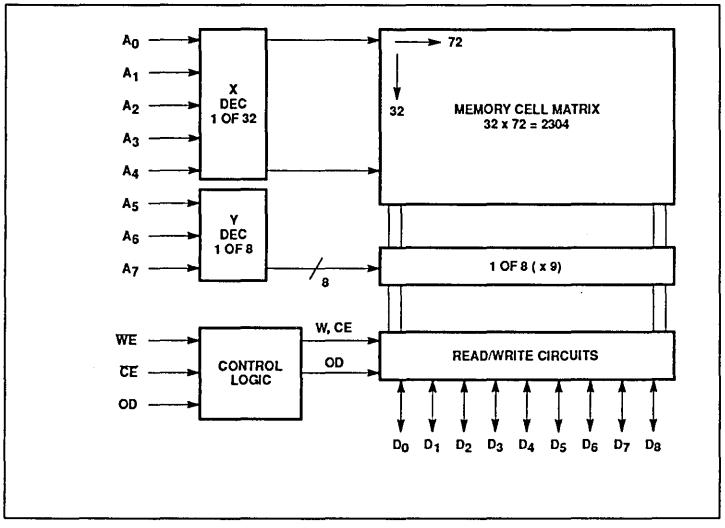
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
22-pin Ceramic Dual-In-Line 400mil-wide	82S212/ BWA-40
22-pin Ceramic Dual-In-Line 400mil-wide	82S212/BWA

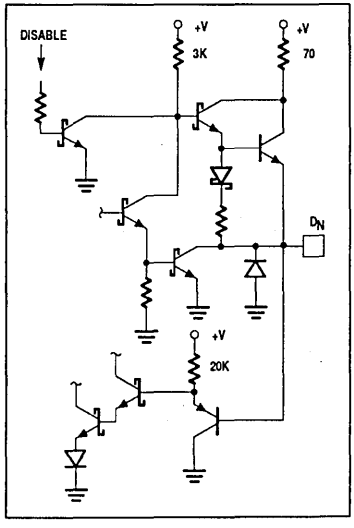
PIN CONFIGURATION



BLOCK DIAGRAM



TYPICAL I/O STRUCTURE



2304-Bit TTL Bipolar RAM (256 × 9) — 82S212/82S212-40

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Off-State Output voltage	+5.5	V_{DC}
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS[2]

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level Output current			-2	mA
I_{OL}	Low-level Output current			8	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS -40°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V[1]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[3]	Max	
Output voltage[2]						
V_{OH}	High	V_{CC} = Min, I_{OH} = Max	2.4			V
V_{OL}	Low	V_{CC} = Min, I_{OL} = Max			0.5	V
Input current						
		V_{CC} = Max				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = Max				
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, or OD = High, V_O = 5.5V			60	µA
		$\overline{CE}$ = High, or OD = High, V_O = 0.5V			-100	mA
I_{OS}	Short circuit[4, 5]	V_{CC} = Min, $\overline{CE}$ = OD = Low, V_O = 0V	-15		-80	mA
Supply current						
I_{CC}		V_{CC} = Max		135	200	mA
Capacitance[6]						
		V_{CC} = Nom				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

2304-Bit TTL Bipolar RAM (256 × 9) — 82S212/82S212-40

AC ELECTRICAL CHARACTERISTICS $-40°C \le T_A \le +125°C$, $4.75V \le V_{CC} \le 5.25V$[1]

SYMBOL	PARAMETER[1]	TO	FROM	LIMITS			UNIT
				Min	Typ[3]	Max	
t_{AA}	Address access time	Output	Address			70	ns
t_{OE} t_{CE}	Output Enable time Output Enable time	Output Output	OD Chip enable			50 50	ns ns
t_{OD} t_{CD}	Output Disable time Output Disable time	Output Output	OD Chip enable			50 50	ns ns
t_{WP}	Write Pulse width			45			ns
t_{WSC} t_{WHC}	Setup time Hold time	Write Chip enable	Chip enable Write	10 10			ns ns
t_{WSD} t_{WHD}	Setup time Hold time	Write Data	DataWrite	45 5			ns ns
t_{WSA} t_{WHA}	Setup time Hold time	Write Address	Address Write	10 15			ns ns
t_{SO} t_{HO}	Setup time (from disabled state) Hold time	Chip enable OD	OD Chip enable	5 5			ns ns

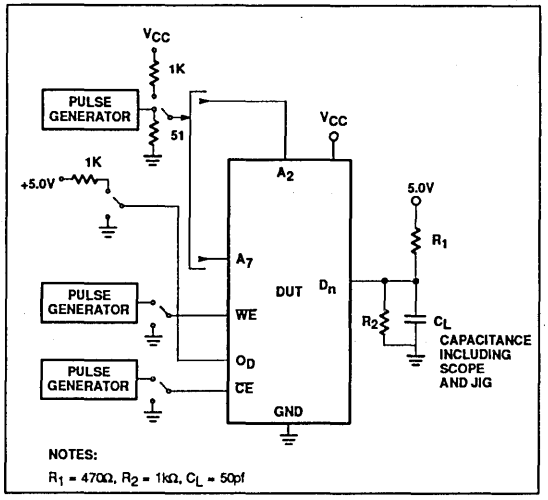
NOTES:
1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
4. Measured on one pin at a time.
5. Duration of I_{OS} test should not exceed one second.
6. Guaranteed but not tested.

TRUTH TABLE

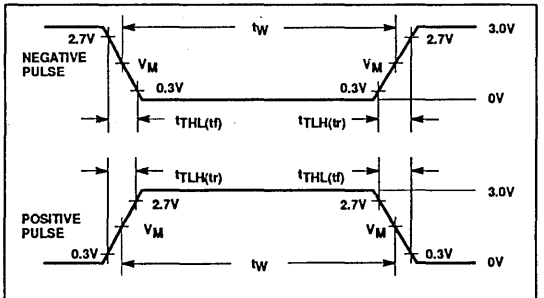
MODE	$\overline{WE}$	$\overline{CE}$	OD	D_N IN/OUT
Disable output	X	X	1	Hi-Z
Disable R/W	X	1	X	Hi-Z
Write	0	0	1	Data in
Read	1	0	0	Data out

X = Don't care

TEST LOAD CIRCUIT



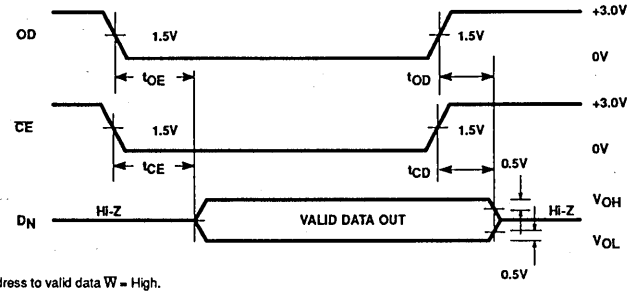
VOLTAGE WAVEFORMS



Input Pulse Definition

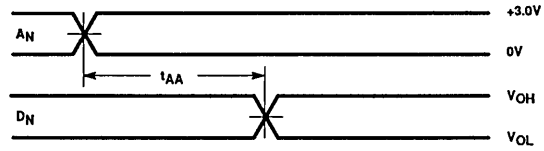
INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS

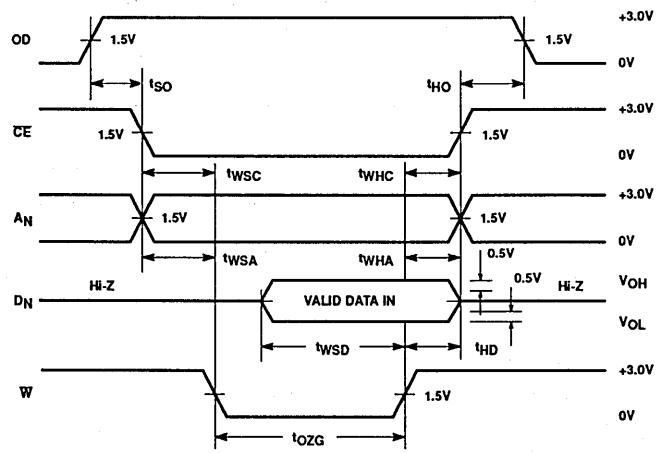


NOTE: Assumes t_{AA} from address to valid data $\overline{W}$ = High.

Enable/Disable



Read Mode



Write Mode

Signetics

54F189A

64-Bit TTL Bipolar RAM, Inverting (3-State)

Military Logic Products

Objective Specification

FEATURES

- Address access time: 9ns Max
- Power dissipation: 4.3mW/bit typ
- Schottky clamped TTL
- One chip enable
- Inverting outputs
- I/O
  - Inputs: PNP Buffered
  - Outputs: 3-State

APPLICATIONS

- Scratch pad memory
- Buffer memory
- Push down stacks
- Control store

DESCRIPTION

The 54F189A is a high speed, 64-Bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are in High impedance state whenever the Chip Enable ($\overline{CE}$) is High. The outputs are active only in the READ mode ($\overline{WE}$ = High) and the output data is the complement of the stored data.

ORDERING INFORMATION

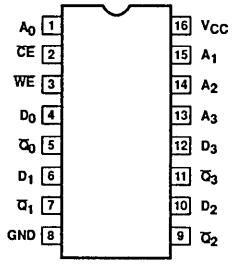
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54F189A/BEA

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

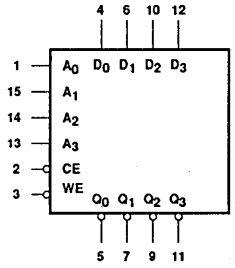
PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Data inputs	1.0/1.0	20μA/0.6mA
A_0 - A_3	Address inputs	1.0/1.0	20μA/0.6mA
$\overline{CE}$	Chip Enable input (active Low)	1.0/2.0	20μA/1.2mA
$\overline{WE}$	Write Enable input (active Low)	1.0/2.0	20μA/1.2mA
$\overline{O}_0$ - $\overline{O}_3$	Data outputs	150/40	3.0mA/24mA

NOTE: One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

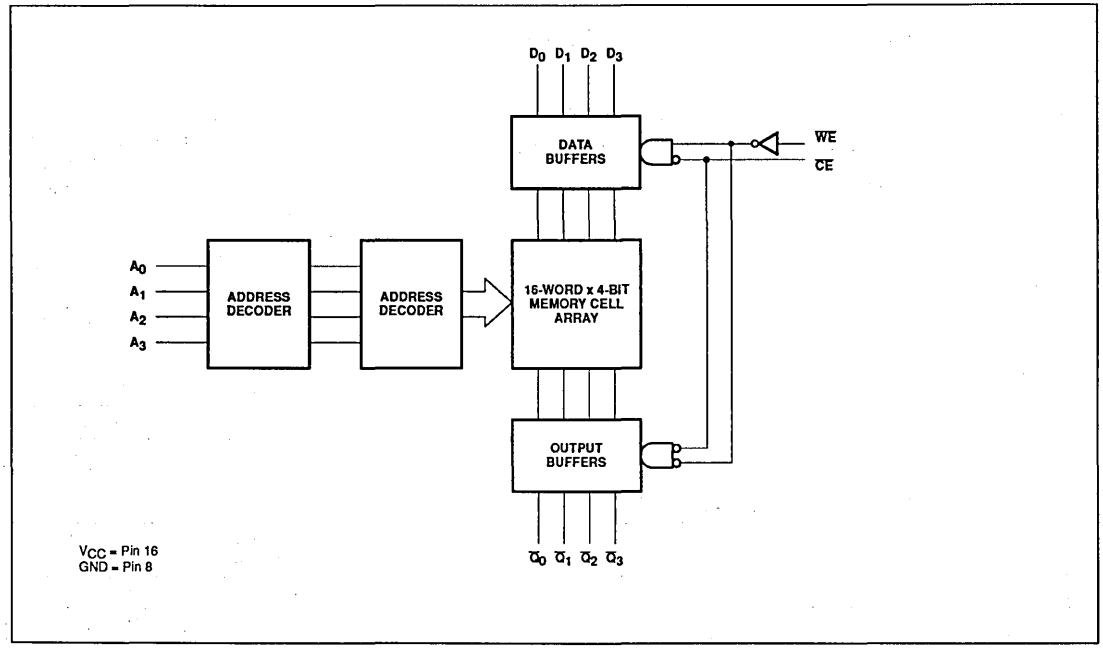


LOGIC SYMBOL



64-Bit TTL Bipolar RAM (16×4) — 54F189A

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUT	OPERATING MODE
$\overline{CE}$	$\overline{WE}$	D_n	$\overline{O}_n$	
L	H	X	Complement of stored data	Read
L	L	L	High impedance	Write "0"
L	L	H	High impedance	Write "1"
H	X	X	High impedance	Disable input

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_{IN}	Input voltage range	-0.5 to +7.0	V
I_{IN}	Input current range	-30 to +5.0	mA
V_{OUT}	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	48	mA
T_{STG}	Storage temperature range	-65 to +150	°C

64-Bit TTL Bipolar RAM (16×4) — 54F189A

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-3	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1,4]	LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OH} = Max	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH}	High-level input current		V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current	Others	V_{CC} = Max, V_I = 0.5V			-0.6	mA
		$\overline{CE}$, $\overline{WE}$				-1.2	mA
I_{OZH}	Off-state output current High-level voltage applied		V_{CC} = Max, V_O = 2.7V			50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = Max, V_O = 0.5V			-50	µA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current (total)		V_{CC} = Max, $\overline{CE}$ = $\overline{WE}$ = GND		55	85	mA
C_{IN}	Input capicitance		V_{CC} = 5V, V_{IN} = 2.0V		4		pF
C_{OUT}	Output capicitance		V_{CC} = 5V, V_{OUT} = 2.0V		7		pF

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Access time	Propagation delay A_n to $\overline{O}_n$	Waveform 1	2.5 2.0	5.0 4.5	8.0 8.0	2.5 2.0	9.0 8.5	ns ns
t_{PZH} t_{PZL}		Enable time $\overline{CE}$ to $\overline{O}_n$	Waveform 2	2.0 2.0	3.5 4.0	6.0 7.0	1.5 2.0	7.0 7.5	ns ns
t_{PHZ} t_{PLZ}	Disable time $\overline{CE}$ to $\overline{O}_n$		Waveform 3	2.5 1.5	4.5 3.0	7.0 5.5	2.0 1.0	9.0 6.0	ns ns
t_{PZH} t_{PZL}	Response time	Enable time $\overline{WE}$ to $\overline{O}_n$	Waveform 4	2.0 2.5	4.0 4.5	6.5 7.5	2.0 2.5	7.0 8.5	ns ns
t_{PHZ} t_{PLZ}	Write Recovery time	Disable time $\overline{WE}$ to $\overline{O}_n$	Waveform 4	3.5 1.5	5.5 3.5	8.5 6.5	3.0 1.5	10.0 7.5	ns ns

64-Bit TTL Bipolar RAM (16×4) — 54F189A

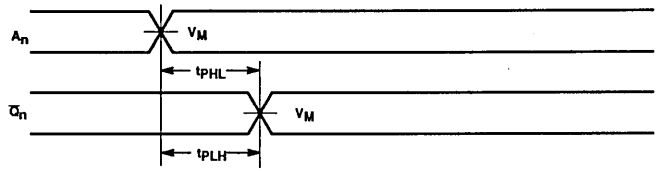
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time A_n to $\overline{WE}$	Waveform 4	4.5 4.5			5.5 5.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{WE}$ to A_n	Waveform 4	0 0			0 0		ns ns
$t_s(H)$ $t_s(L)$	Setup time D_n to $\overline{WE}$	Waveform 4	7.5 6.5			9.5 8.5		ns ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{WE}$ to D_n	Waveform 4	0 0			0 0		ns ns
$t_s(L)$	Setup time $\overline{CE}$ (falling edge) to $\overline{WE}$ (falling edge)	Waveform 4	0			0		ns
$t_h(L)$	Hold time $\overline{WE}$ (falling edge) to $\overline{CE}$ (rising edge)	Waveform 4	6.5			8.0		ns
$t_w(L)$	Pulse width, Low $\overline{WE}$	Waveform 4	7.0			8.5		ns

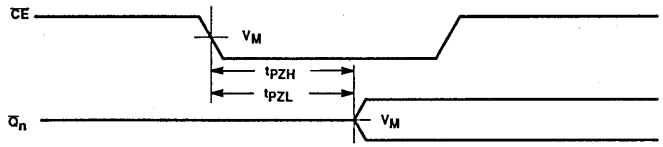
NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

64-Bit TTL Bipolar RAM (16×4) 54F189A

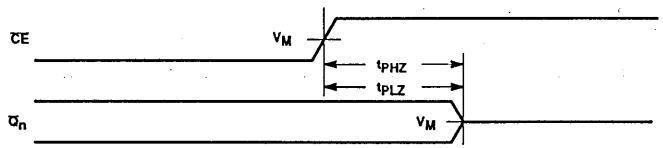
AC WAVEFORMS



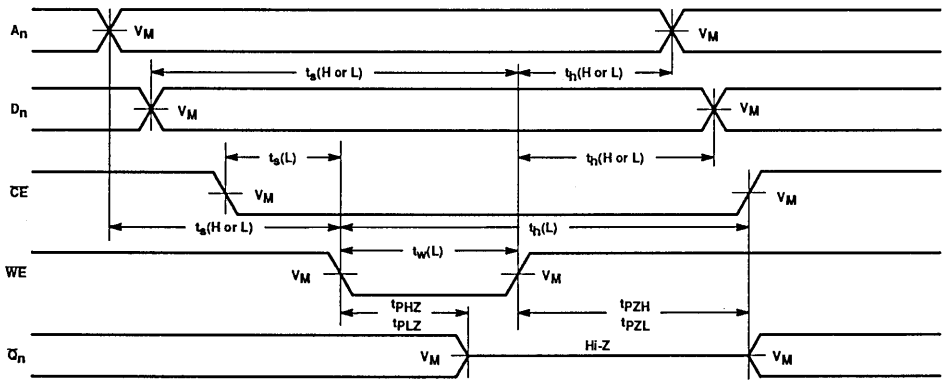
Waveform 1. Read Cycle, Address Access Time



Waveform 2. Read Cycle, Chip Enable Access Time



Waveform 3. Read Cycle, Chip Disable Time

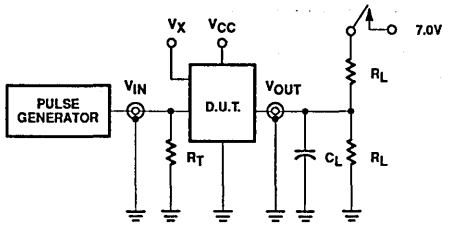


Waveform 4. Write Cycle

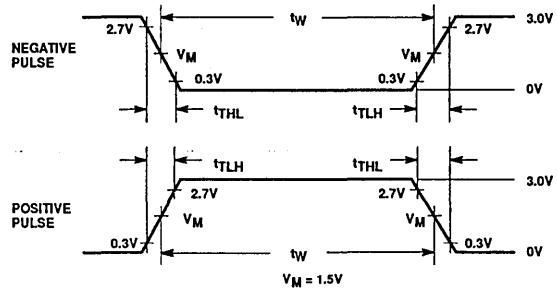
NOTE: For all waveforms V_M = 1.5V

64-Bit TTL Bipolar RAM (16×4) — 54F189A

TEST CIRCUITS AND WAVEFORMS



Test Circuit for 3-State Outputs and Open Collector Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	closed
All other	open

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.

Signetics

54S189
64-Bit TTL Bipolar RAM

Military
Bipolar Memory Products

Product Specification

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature PNP inputs and 1 chip enable line for ease of memory expansion.

During Write, the outputs of each product assume the logic state defined in the truth table.

FEATURES

- **Output access time: 50ns max**
- **Input loading: -150μA max**
- **On-chip address decoding**
- **One chip enable input**
- **Output options:**
  54S189: 3-State
- **Schottky clamped**
- **TTL compatible**

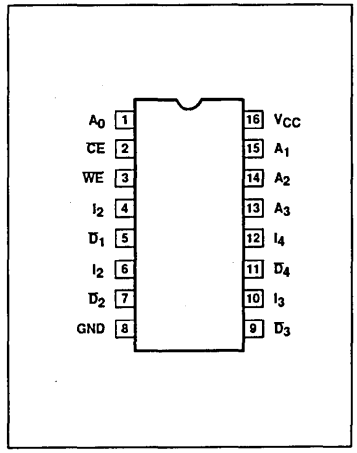
APPLICATIONS

- **Scratch pad memory**
- **Buffer memory**
- **Push down stacks**
- **Control store**

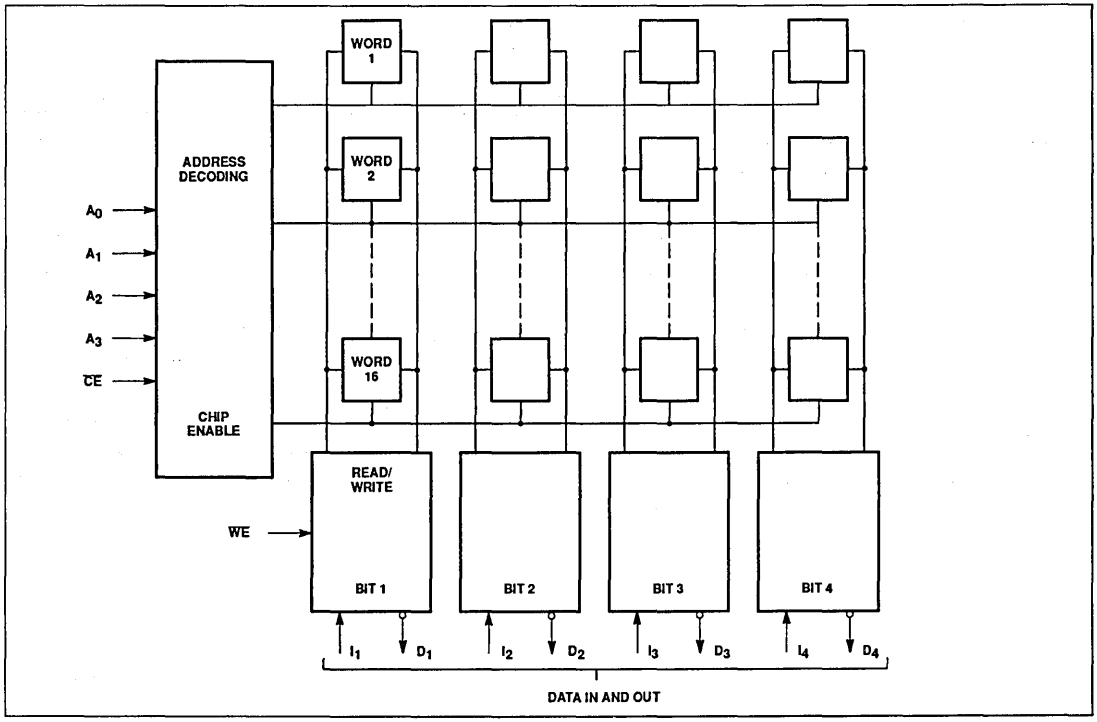
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic Dual-In-Line 300mil-wide	54S189/BEA
16-Pin Ceramic FlatPack	54S189/BFA

PIN CONFIGURATION



BLOCK DIAGRAM



64-Bit TTL Bipolar RAM (16 × 4) — 54S189

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[6]	LIMITS			UNIT
			Min	Typ[2]	Max	
Input voltage [1]						
V_{IL}	Low				0.80	V
V_{IH}	High		2.0			V
V_{IK}	Clamp[7]	I_I = -18mA, V_{CC} = 4.5V			-1.5	V
Output voltage[1]						
		$\overline{CE}$ = Low				
V_{OL}	Low[2, 3]	I_O = 16mA, V_{CC} = 4.75V			0.5	V
V_{OH}	High	I_O = -2mA	2.4			V
Input current[5]						
		V_{CC} = 5.25V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			25	µA
Output current[5]						
I_{CLK}	Leakage	$\overline{CE}$ = High, V_O = 5.5V, V_{CC} = 5.25V			100	µA
I_{OS}	Short curcuit	$\overline{CE}$ = Low, V_O = 0V	-30		-100	mA
I_{OZ}	Hi-Z	$2.4 \geq V_O \geq 0.4V$			±50	µA
Supply current[5]						
I_{CC}		V_{CC} = 5.25V			110	mA
Capacitance[6]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V, $\overline{CE}$ = High		8	13	pF

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	D_{IN}	Data Out
Read	0	1	X	Stored $\overline{Data}$
Write "0"	0	0	0	Hi-Z
Write "1"	0	0	1	Hi-Z
Disable	1	X	X	Hi-Z

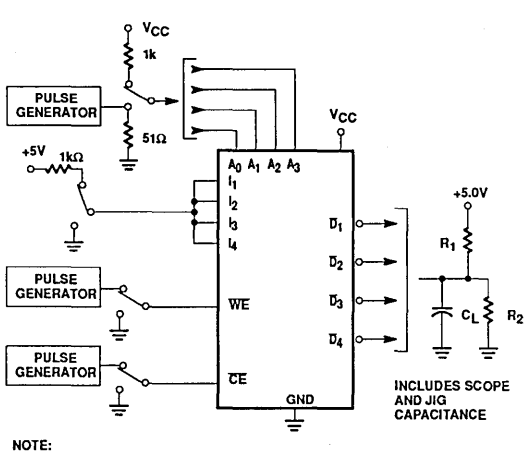
64-Bit TTL Bipolar RAM (16 × 4) — 54S189

AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

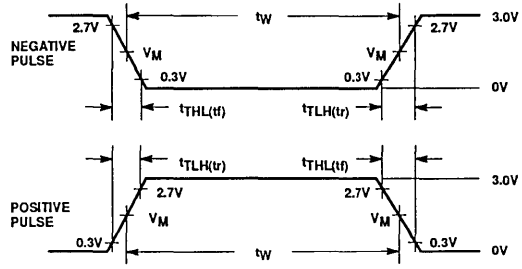
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
t_{AA} t_{CE}	Address access time Chip enable access time					50 25	ns ns
t_{CD}	Disable time	Output	Chip enable			40	ns
t_{WD}	Response time	Output	Write enable			50	ns
t_{WR}	Write recovery time					40	ns
t_{WSA} t_{WHA}	Setup time Hold time	Write enable	Address	0 10			ns ns
t_{WSD} t_{WHD}	Setup time Hold time	Write enable	Data in	30 10			ns ns
t_{WSC} t_{WHC}	Setup time Hold time	Write enable	$\overline{CE}$	0 0			ns ns
t_{WP}	Write enable pulse width[4]			30			ns

NOTES:
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in Low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. Positive logic definition: High = +5.0V, Low = GND.
7. test each input one at a time.
8. Guaranteed, but not tested.

TEST CIRCUIT AND WAVEFORMS



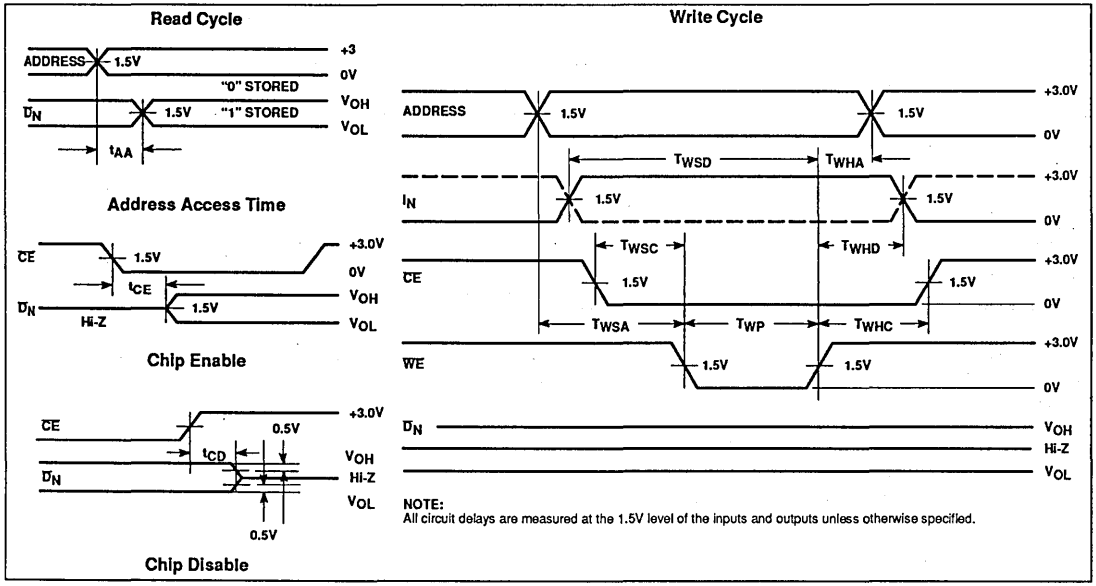
NOTE:
R_1 = 270Ω, R_2 = 600Ω, C_L = 50pF



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



NOTE:
All circuit delays are measured at the 1.5V level of the inputs and outputs unless otherwise specified.

Signetics

8X350

2K-Bit TTL Bipolar RAM (256 × 8)

Military
Bipolar Memory Products

Product Specification

DESCRIPTION

The 8X350 bipolar RAM is designed principally as a working storage element in an 8X305 based system. Internal circuitry is provided for direct use in 8X305 applications. When used with the 8X305, the RAM address and data busses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with 3-State outputs.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
22-pin Ceramic DIP 400mil-wide	8X350/BWA

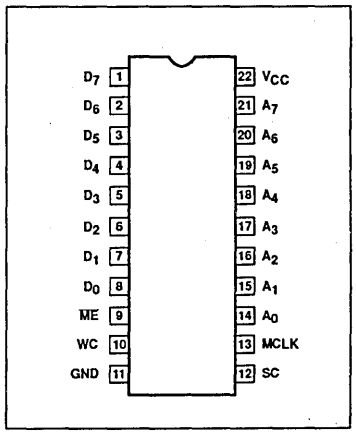
FEATURES

- On-chip address latches
- Schottky clamped
- One master enable input
- Directly interfaces with the 8X305 bipolar microprocessor with no external logic
- May be used on left or right bank
- Common I/O:
  - Inputs: PNP buffered
  - Outputs: 3-State

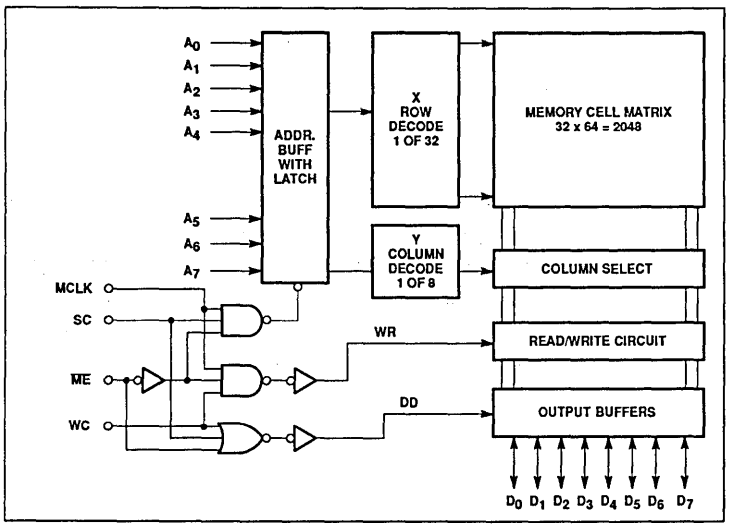
APPLICATIONS

- 8X305 working storage

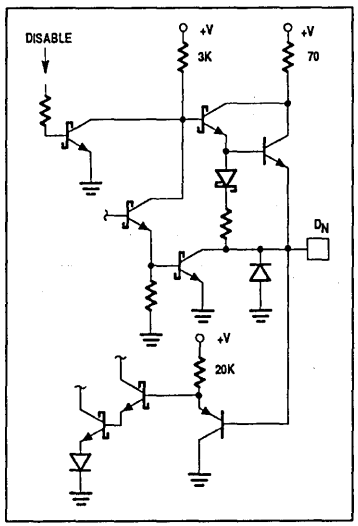
PIN CONFIGURATION



BLOCK DIAGRAM



TYPICAL I/O STRUCTURE



2K-Bit TTL Bipolar RAM (256 × 8) — 8X350

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V[2]

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp[3]	V_{CC} = 4.75V, I_I = -18mA			-1.2	V
Output voltage						
		V_{CC} = 4.75V				
V_{OL}	Low[4]	I_{OL} = 9.6mA			0.5	V
V_{OH}	High[5]	I_{OH} = -2mA	2.4			V
Input current						
		V_{CC} = 5.25V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			50	µA
Output current						
		V_{CC} = 5.25V				
I_{OZ}	Hi-Z state	$\overline{ME}$ = High, V_O = 5.5V			60	µA
		$\overline{ME}$ = High, V_O = 0.5V			-100	µA
I_{OS}	Short circuit[3, 6, 13]	SC = WC, $\overline{ME}$ = Low				
		V_{CC} = 5.25V, V_O = 0V, High stored	-15		-85	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			200	mA
Capacitance[13]						
		$\overline{ME}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

TRUTH TABLE

MODE	$\overline{ME}$	SC	WC	MCLK	BUSSED DATA/ ADDRESS LINES
Hold address Disable data out	1	X	X	X	Hi-Z data out
Input new address	0	1	0	1	Address Hi-Z
Hold address Disable data out	0	1	0	0	Hi-Z data out
Hold address Write data	0	0	1	1	Data in
Hold address Disable data out	0	0	1	0	Hi-Z data out
Hold address Read data	0	0	0	X	Data out
Undefined state[12]	0	1	1	1	
Hold address[12] Disable data out	0	1	1	0	Hi-Z data out

X = Don't care

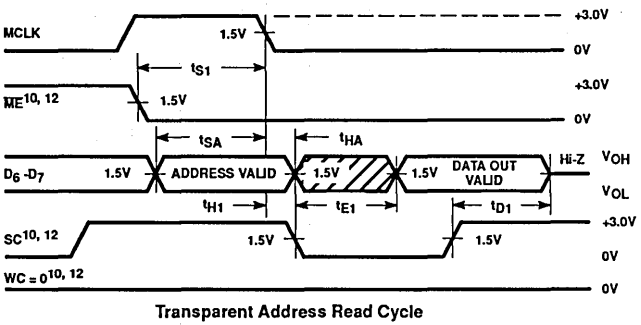
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.75V \le V_{CC} \le 5.25V$[2]

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
t_{E1} t_{E2}	Output enable time Output enable time	Data out Data out	SC- $\overline{ME}$-			40 40	ns ns
t_{D1} t_{D2}	Output disable time Output disable time	Data out Data out	SC+ $\overline{ME}$+			40 40	ns ns
t_W	Master clock pulse width[8]			50			ns
t_{SA} t_{HA}	Setup time Hold time	MCLK- Address	Address MCLK-	40 10			ns ns
t_{SD} t_{HD}	Setup time Hold time	MCLK- Data in	Data in MCLK-	45 10			ns ns
t_{S3} t_{H3}	Setup time Hold time	MCLK- $\overline{ME}$+	$\overline{ME}$- MCLK-	50 5			ns ns
t_{S1} t_{H2}	Setup time Hold time	MCLK- $\overline{ME}$-	$\overline{ME}$- MCLK-	40 5			ns ns
t_{S2} t_{H1} t_{H4}	Setup time Hold time Hold time	$\overline{ME}$- SC- WC-	SC-, WC- MCLK- MCLK-	5 5 5			ns ns ns

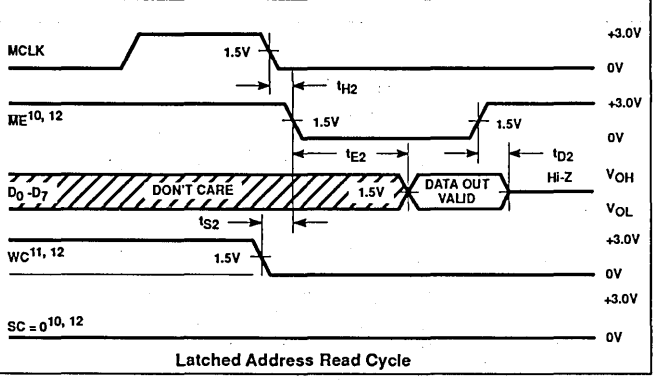
NOTES:
1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
3. Test each pin one at a time.
4. Measured with a logic Low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with a logic High stored.
6. Duration of the short circuit should not exceed 1 second.
7. I_{CC} is measured with the Write enable and Memory enable inputs grounded, all other inputs $\ge$ 4.0V and the output open.
8. Minimum required to guarantee a Write into the slowest bit.
9. Applied to the 8X305 based system with the data and address pins tied to the IV Bus.
10. SC + ME = 1 to avoid bus conflict.
11. WC + ME = 1 to avoid bus conflict.
12. The SC and WC outputs from the 8X305 are never at 1 simultaneously.
13. Guaranteed, but not tested.

2K-Bit TTL Bipolar RAM (256 × 8) — 8X350

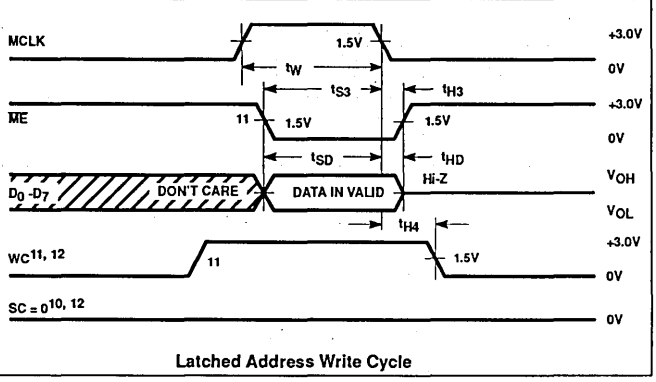
TIMING DIAGRAM



Transparent Address Read Cycle



Latched Address Read Cycle



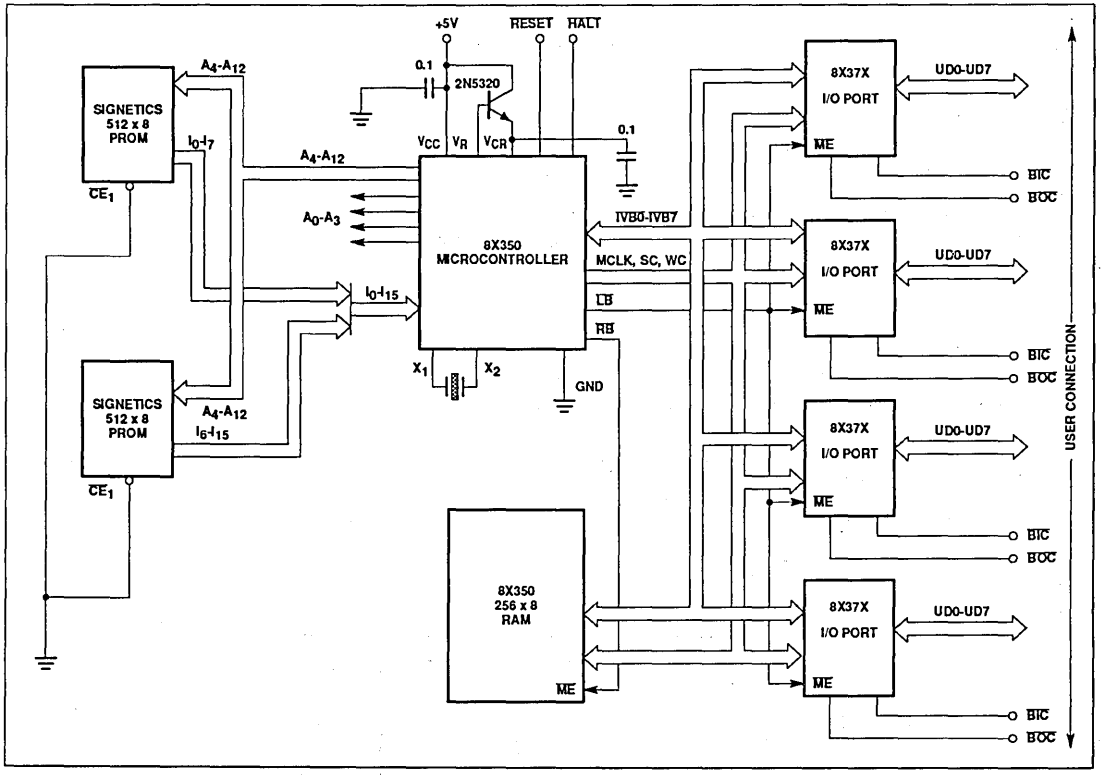
Latched Address Write Cycle

MEMORY TIMING DEFINITIONS

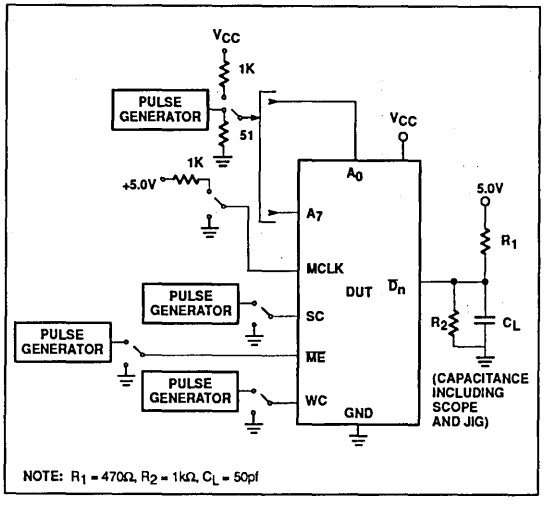
t_{S1}	Required delay between beginning of Master Enable Low and falling edge of Master Clock.
t_{SA}	Required delay between beginning of valid address and falling edge of Master Clock.
t_{E1}	Delay between beginning of Select Command Low and beginning of valid data output on the IV Bus.
t_{E2}	Delay between when Master Enable becomes Low and beginning of valid data output on the IV Bus.
t_{HA}	Required delay between falling edge of Master Clock and end of valid Address.
t_{D1}	Delay between when Select Command becomes High and end of valid data output on the IV Bus.
t_{D2}	Delay between when Master Enable becomes High and end of valid data output on the IV Bus.
t_{H1}	Required delay between falling edge of Master Clock and when Select Command becomes Low.
t_{H2}	Required delay between falling edge of Master Clock and when Master Enable becomes Low.
t_{S2}	Required delay between when Select Command or Write Command becomes Low and when Master Enable becomes Low.
t_W	Minimum width of the Master Clock pulse.
t_{SD}	Required delay between beginning of valid data input on the IV Bus and falling edge of Master Clock.
t_{S3}	Required delay between when Master Enable becomes Low and falling edge of Master Clock.
t_{HD}	Required delay between beginning of valid data input on the IV Bus.
t_{H3}	Required delay between falling edge of Master Clock and when Master Enable becomes High.
t_{H4}	Required delay between falling edge of Master Clock and when Write Command becomes Low.

2K-Bit TTL Bipolar RAM (256 × 8) — 8X350

TYPICAL 8X350 APPLICATION

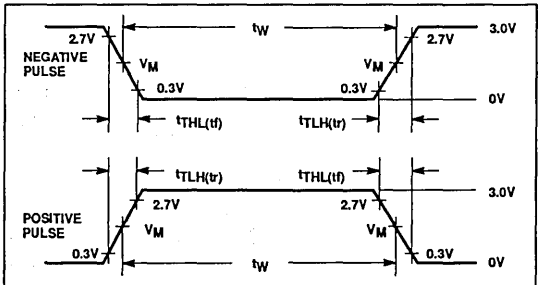


TEST LOAD CIRCUIT



NOTE: $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 50pf$

VOLTAGE WAVEFORMS



Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Signetics

8X350-40

2K-Bit TTL Bipolar RAM (256 × 8)

Military
Bipolar Memory Products

Product Specification

DESCRIPTION

The 8X350-40 bipolar RAM is designed principally as a working storage element in an 8X305 based system. Internal circuitry is provided for direct use in 8X305 applications. When used with the 8X305, the RAM address and data busses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with 3-State outputs.

-55°C operation can be guaranteed after a 60 second warmup.

FEATURES

- On-chip address latches
- Schottky clamped
- One master enable input
- Directly interfaces with the 8X305 bipolar microprocessor with no external logic
- May be used on left or right bank
- Common I/O:
  - Inputs: PNP buffered
  - Outputs: 3-State

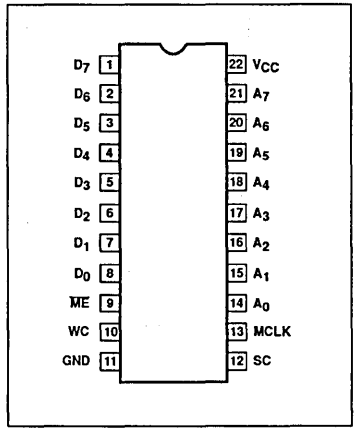
APPLICATIONS

- 8X305 working storage

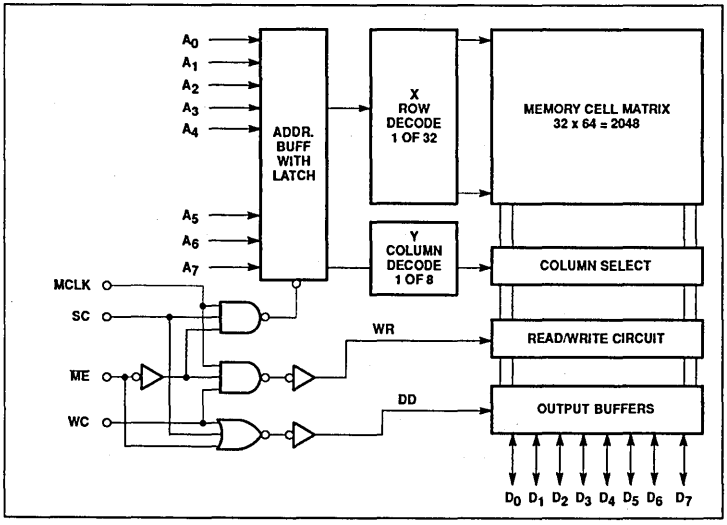
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
22-pin Ceramic DIP 400mil-wide	8X350/BWA-40

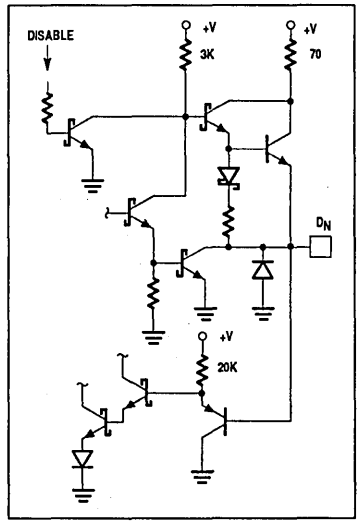
PIN CONFIGURATION



BLOCK DIAGRAM



TYPICAL I/O STRUCTURE



2K-Bit TTL Bipolar RAM (256 × 8) — 8X350-40

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High	+5.5	V_{DC}
V_O	Output voltage Off-state	+5.5	V_{DC}
T_A	Operating temperature range	-40 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS -40°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V[2]

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp[3]	V_{CC} = 4.75V, I_{IN} = -18mA			-1.2	V
Output voltage						
		V_{CC} = 4.75V				
V_{OL}	Low[4]	I_{OL} = 9.6mA			0.5	V
V_{OH}	High[5]	I_{OH} = -2mA	2.4			V
Input current						
		V_{CC} = 5.25V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			50	µA
Output current						
		V_{CC} = 5.25V				
I_{OZ}	Hi-Z state	$\overline{ME}$ = High, V_O = 5.5V			60	µA
		$\overline{ME}$ = High, V_O = 0.5V			-100	µA
I_{OS}	Short circuit[3, 6, 13]	SC = WC, $\overline{ME}$ = Low				
		V_{CC} = 5.25V, V_O = 0V, High stored	-15		-85	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			200	mA
Capacitance[13]						
		$\overline{ME}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

TRUTH TABLE

MODE	$\overline{ME}$	SC	WC	MCLK	BUSSED DATA/ ADDRESS LINES
Hold address Disable data out	1	X	X	X	Hi-Z data out
Input new address	0	1	0	1	Address Hi-Z
Hold address Disable data out	0	1	0	0	Hi-Z data out
Hold address Write data	0	0	1	1	Data in
Hold address Disable data out	0	0	1	0	Hi-Z data out
Hold address Read data	0	0	0	X	Data out
Undefined state[12]	0	1	1	1	–
Hold address[12] Disable data out	0	1	1	0	Hi-Z data out

NOTE:
X = Don't care

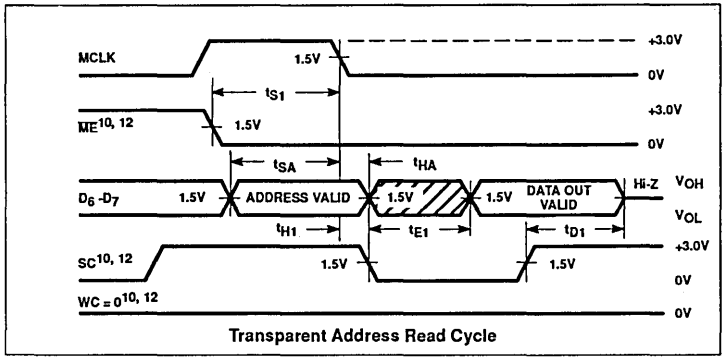
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C, 4.75V \le V_{CC} \le 5.25V$[2]

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
t_{E1} t_{E2}	Output enable time Output enable time	Data out Data out	SC- $\overline{ME}$-			40 40	ns ns
t_{D1} t_{D2}	Output disable time Output disable time	Data out Data out	SC+ $\overline{ME}$+			40 40	ns ns
t_W	Master clock pulse width[8]			50			ns
t_{SA} t_{HA}	Setup time Hold time	MCLK- Address	Address MCLK-	40 10			ns ns
t_{SD} t_{HD}	Setup time Hold time	MCLK- Data in	Data in MCLK-	45 10			ns ns
t_{S3} t_{H3}	Setup time Hold time	MCLK- $\overline{ME}$+	$\overline{ME}$- MCLK-	50 5			ns ns
t_{S1} t_{H2}	Setup time Hold time	MCLK- $\overline{ME}$-	$\overline{ME}$- MCLK-	40 5			ns ns
t_{S2} t_{H1} t_{H4}	Setup time Hold time Hold time	$\overline{ME}$- SC- WC-	SC-, WC- MCLK- MCLK-	5 5 5			ns ns ns

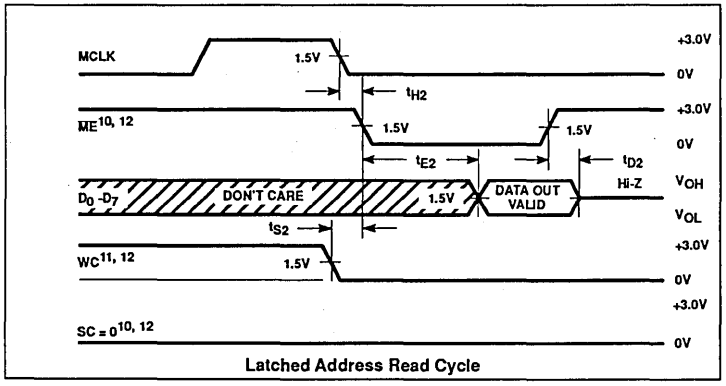
NOTES:
1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
3. Test each pin one at a time.
4. Measured with a logic Low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with a logic High stored.
6. Duration of the short circuit should not exceed 1 second.
7. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs ≥ 4.0V and the output open.
8. Minimum required to guarantee a Write into the slowest bit.
9. Applied to the 8X305 based system with the data and address pins tied to the IV Bus.
10. SC + ME = 1 to avoid bus conflict.
11. WC + ME = 1 to avoid bus conflict.
12. The SC and WC outputs from the 8X305 are never at 1 simultaneously.
13. Guaranteed, but not tested.

2K-Bit TTL Bipolar RAM (256 × 8) — 8X350-40

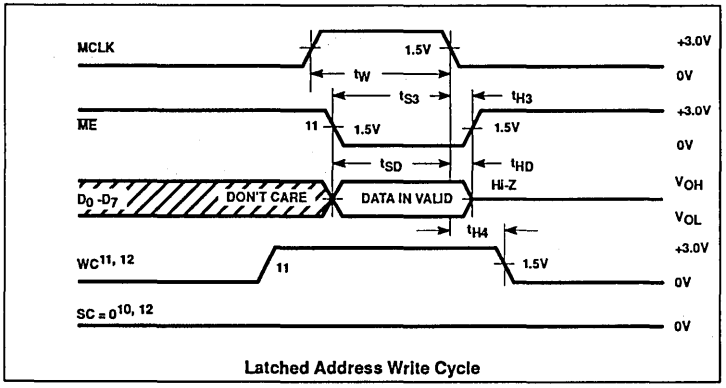
TIMING DIAGRAM



Transparent Address Read Cycle



Latched Address Read Cycle



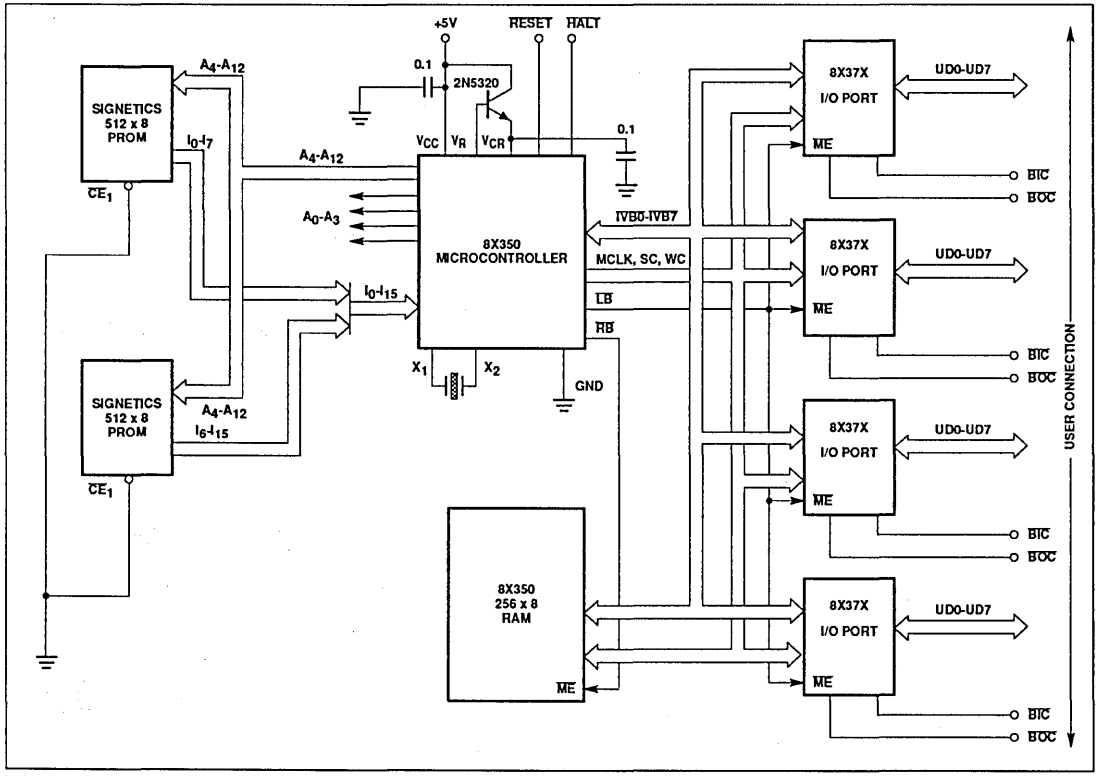
Latched Address Write Cycle

MEMORY TIMING DEFINITIONS

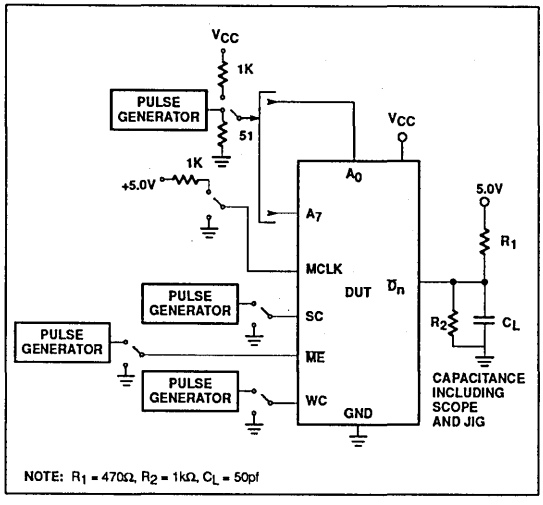
t_{S1}	Required delay between beginning of Master Enable Low and falling edge of Master Clock.
t_{SA}	Required delay between beginning of valid address and falling edge of Master Clock.
t_{E1}	Delay between beginning of Select Command Low and beginning of valid data output on the IV Bus.
t_{E2}	Delay between when Master Enable becomes Low and beginning of valid data output on the IV Bus.
t_{HA}	Required delay between falling edge of Master Clock and end of valid Address.
t_{D1}	Delay between when Select Command becomes High and end of valid data output on the IV Bus.
t_{D2}	Delay between when Master Enable becomes High and end of valid data output on the IV Bus.
t_{H1}	Required delay between falling edge of Master Clock and when Select Command becomes Low.
t_{H2}	Required delay between falling edge of Master Clock and when Master Enable becomes Low.
t_{S2}	Required delay between when Select Command or Write Command becomes Low and when Master Enable becomes Low.
t_W	Minimum width of the Master Clock pulse.
t_{SD}	Required delay between beginning of valid data input on the IV Bus and falling edge of Master Clock.
t_{S3}	Required delay between when Master Enable becomes Low and falling edge of Master Clock.
t_{HD}	Required delay between beginning of valid data input on the IV Bus.
t_{H3}	Required delay between falling edge of Master Clock and when Master Enable becomes High.
t_{H4}	Required delay between falling edge of Master Clock and when Write Command becomes Low.

2K-Bit TTL Bipolar RAM (256 × 8) — 8X350-40

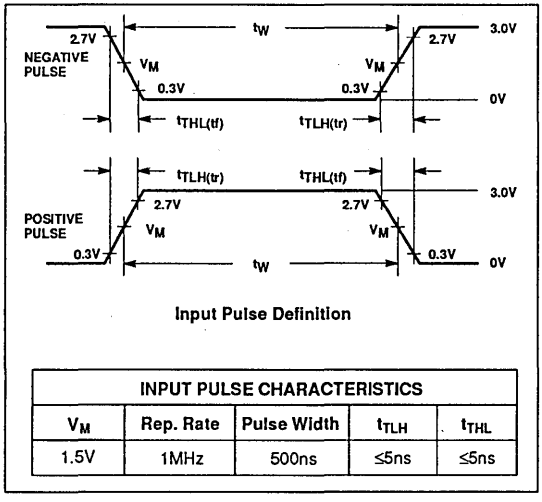
TYPICAL 8X350 APPLICATION



TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Signetics

Section 6
PROM Data Sheets

Military Products

INDEX

Signetics

82S115

4K-Bit TTL Bipolar PROM (512 × 8)

Military
Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S115 is field programmable and includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the 3-State output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe High. In this mode the bit drivers will be controlled solely by $\overline{CE}_1$ and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (High, Low, or Hi-Z) as long as Strobe is Low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the output if the chip is enabled, and causes outputs to go to the Hi-Z State if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

FEATURES

- **Address access time: 90ns max**
- **Input loading: -150μA max**
- **On-chip storage latches**
- **Schottky clamped**
- **Fully TTL compatible**
- **Outputs: 3-State**

APPLICATIONS

- **Microprogramming**
- **Hardware algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

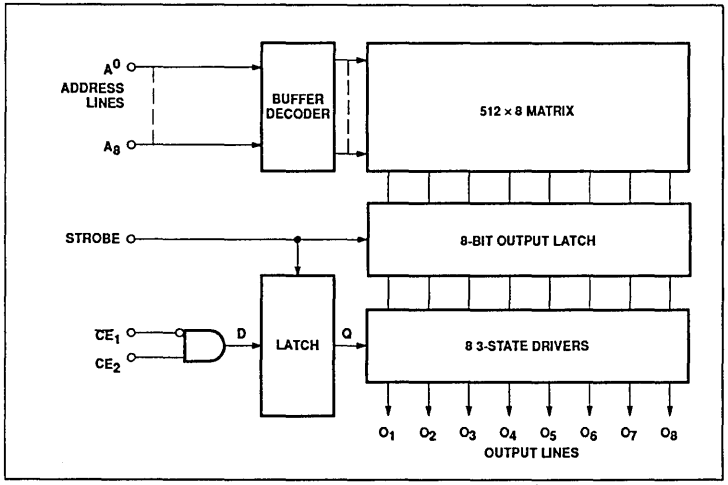
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic Dual In-Line 600mil-wide	82S115/BJA
24-Pin Ceramic FlatPack	82S115/BYA

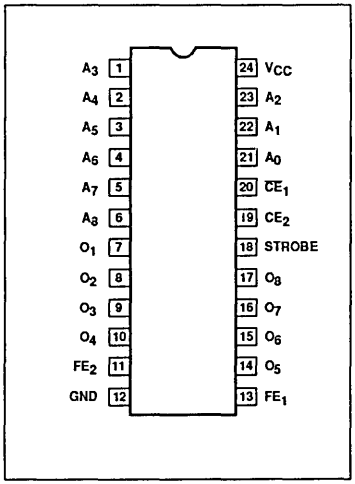
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I, V_O	Input voltage	+5.5	V_{DC}
T_A	Operating temperature range	–55 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C

BLOCK DIAGRAM



PIN CONFIGURATION



4K-Bit TTL Bipolar PROM (512 × 8) — 82S115

DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[5]	LIMITS			UNIT
			Min	Typ[8]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage						
		$\overline{CE}_1$ = Low, CE_2 = High				
V_{OL}	Low	I_O = 9.6mA		0.4	0.5	V
V_{OH}	High	V_{CC} = 4.5V, I_O = -2mA	2.4			V
Input current[5]						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			50	µA
Output current[5]						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z State	$\overline{CE}_1$ = High or CE_2 = Low, V_O = 5.5V			100	µA
		$\overline{CE}_1$ = High or CE_2 = Low, V_O = 0.5V			-100	µA
I_{OS}	Short circuit[1]	$\overline{CE}_1$ = Low, CE_2 = High, V_O = 0V, High stored	-15		-85	mA
Supply current						
$\overline{CE}_1$ $\overline{CE}_2$ I_{CC}		$\overline{CE}_1$ = High, $\overline{CE}_2$ = Low V_{CC} = 5.5V		130	185	mA
Capacitance[9]						
		$\overline{CE}_1$ = High or CE_2 = Low, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

4K-Bit TTL Bipolar PROM (512 × 8) — 82S115

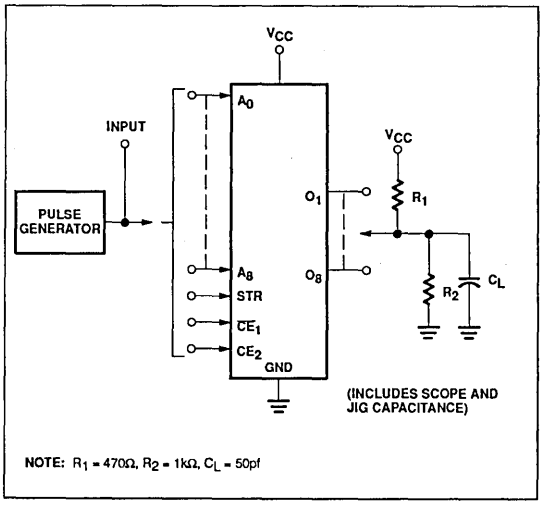
AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ[8]	Max	
t_{AA} t_{CE}	Access time[6]	Output Output	Address Chip enable	Latched or transparent Read[2, 4]		40 20	90 50	ns ns
t_{CD}	Disable time	Output	Chip disable	Latched or transparent Read[2, 4]		20	55	ns
t_{CDS} t_{CDH}	Setup time Hold time	Output	Chip enable	Latched Read only[3, 4]	50 15			
t_{ADH}	Hold time	Address	Strobe	Latched Read only[3, 4]	5	0		
t_{SW}	Strobe pulse width			Latched Read only[3, 4]	40	15		ns
t_{SL}	Strobe latch time			Latched Read only[3, 4]	90	35		ns
t_{DL}	Strobe delatch time			Latched Read only[3, 4]			45	ns

NOTES:

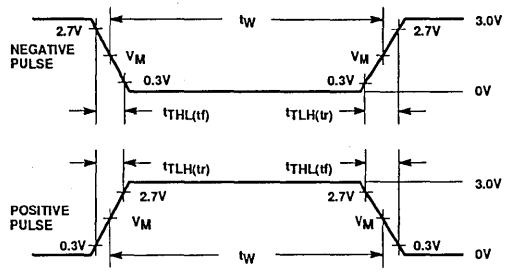
1. No more than one output should be grounded at the same time and strobe should be disabled Strobe is in the High state.
2. If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed to T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or High impedance state after it has been enabled.
3. In latched Read Mode data from any selected address will be held on the output when Strobe is lowered only when Strobe is raised will new location data be transferred and chip enable conditions be stored. the new data will appear on the outputs if the chip enable conditions enable the outputs.
4. During operation the fusing pins FE_1 and FE_2 may be grounded or left floating.
5. Positive current is defined as into the terminal referenced.
6. Tested at an address cycle time of 1µs.
7. Areas shown by crosshatch are latched data from previous address.
8. Typical values are at V_{CC} = 5V, T_A = 25°C.
9. Guaranteed, but not tested.

TEST LOAD CIRCUIT



NOTE: R_1 = 470Ω, R_2 = 1kΩ, C_L = 50pf

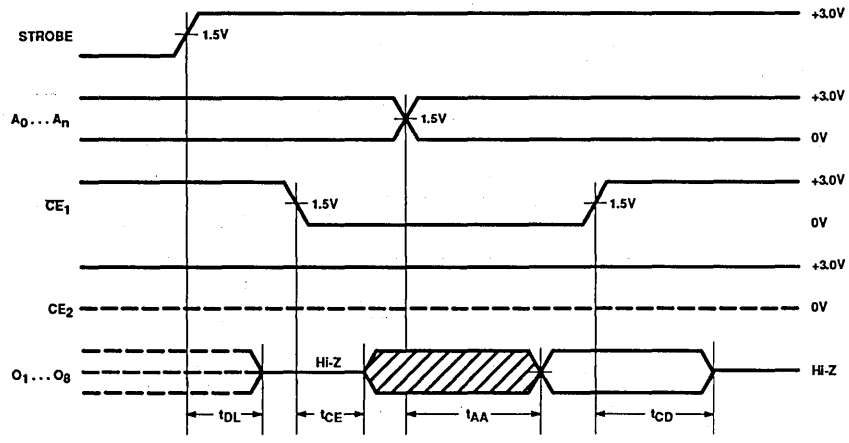
VOLTAGE WAVEFORM



Input Pulse Definition

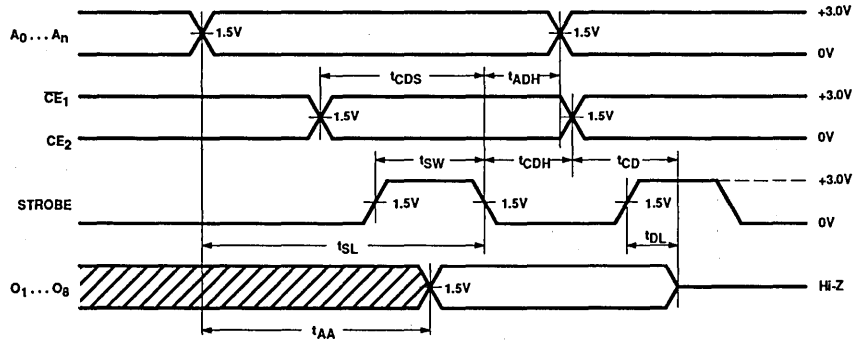
INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



NOTE:
Output latches not used.
All AC measurements at 1.5V unless otherwise specified.

Transparent Read[2,7]



NOTE:
Output latches used.
All AC measurements at 1.5V unless otherwise specified.

Latched Read[3,7]

Signetics

82S23, 82S123
256-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S23 and 82S123 are field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23 and 82S123 devices are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for memory expansion. They feature either Open collector or 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- **Address access time: 50ns max**
- **Input loading: -150μA max**
- **On-chip address decoding**
- **One chip enable input**
- **Output options:**
  - **82S23: Open collector**
  - **82S123: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

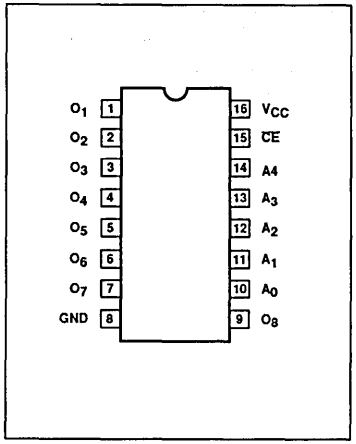
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic Dual-In-Line 300mil-wide	82S23/BEA, 82S123/BEA
16-Pin Ceramic FlatPack	82S23/BFA, 82S123/BFA

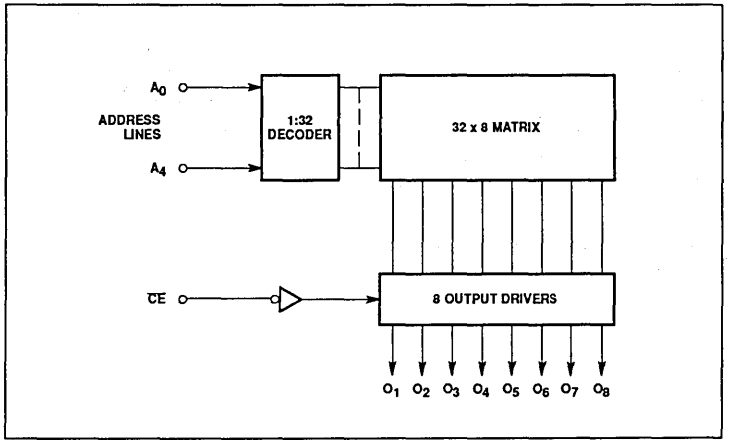
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High (82S23)	+5.5	V_{DC}
V_O	Output voltage Off-State (82S123)	+5.5	V_{DC}
T_A	Operating temperature range	–55 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar PROM (32 × 8) — 82S23, 82S123

DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA			-1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High	I_O = -2mA, V_{CC} = 4.5V	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH1}	High	V_I = 2.7V			25	µA
I_{IH2}	High	V_I = 5.5V			40	µA
Output current[1]						
		V_{CC} = 5.5V				
I_{OLK}	Leakage (82S23)	$\overline{CE}$ = High, V_O = 5.5V			40	µA
I_{OZ}	Hi-Z state (82S123)	$\overline{CE}$ = High, V_O = 5.5V			40	µA
		$\overline{CE}$ = High, V_O = 0.4V			-40	µA
I_{OS}	Short circuit (82S123)[3]	V_{CC} = 5.5V, $\overline{CE}$ = Low, V_O = 0V, High stored	-20		-100	mA
Supply current						
I_{CC}		V_{CC} = 5.5V, $\overline{CE}$ = High			110	mA
Capacitance[6]						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

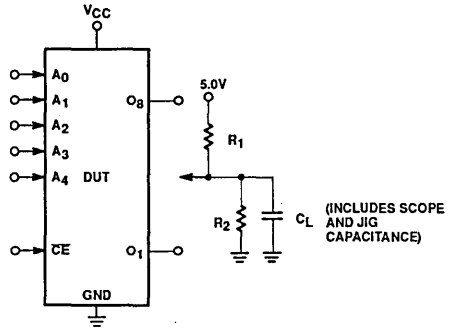
AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER			LIMITS			UNIT
		TO	FROM	Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		45	50	ns
t_{CE}	Access time[4]	Output	Chip Enable			30	ns
t_{CD}	Disable time	Output	Chip Disable			30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed but not tested.

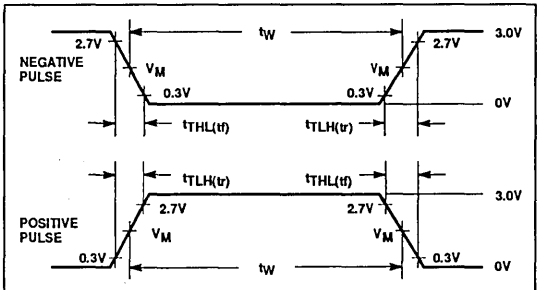
256-Bit TTL Bipolar PROM (32 × 8) — 82S23, 82S123

TEST LOAD CIRCUITS



NOTE:
R_1 = 270 Ω, R_2 = 600Ω, C_L = 50pF.

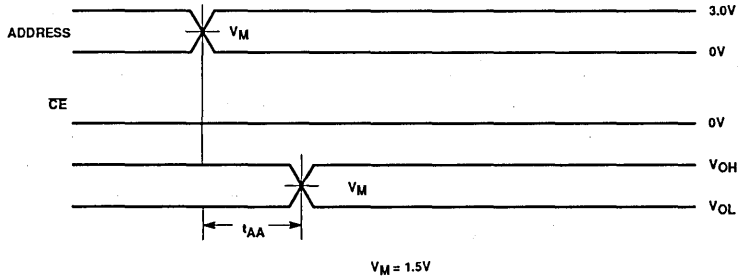
VOLTAGE WAVEFORMS

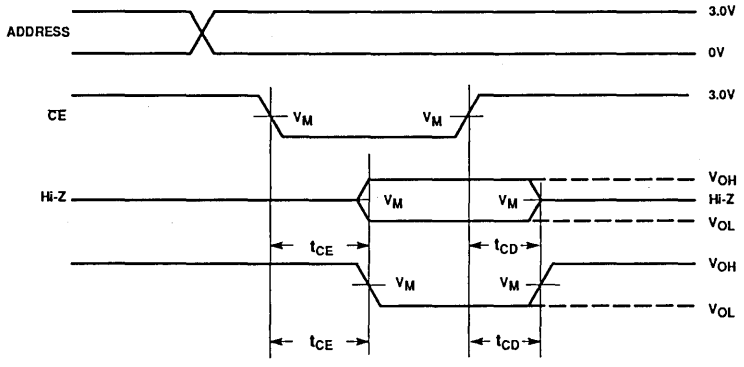


Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS





Signetics

82S23A, 82S123A

256-Bit TTL Bipolar PROM (32 × 8)

Military
Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S23A and 82S123A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23A and 82S123A devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for memory expansion. They feature either Open collector or 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 35ns max
- Input loading: -150μA max
- On-chip address decoding
- One chip enable input
- Output options:
  - -82S23A: Open collector
  - -82S123A: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Format conversion
- Hardwired algorithms
- Random logic
- Code conversion

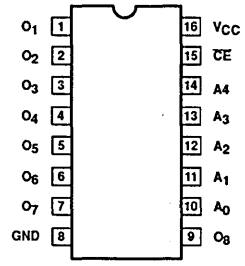
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic Dual-In-Line 300mil-wide	82S23A/BEA 82S123A/BEA
16-pin Ceramic Flat Pack	82S23A/BFA 82S123A/BFA

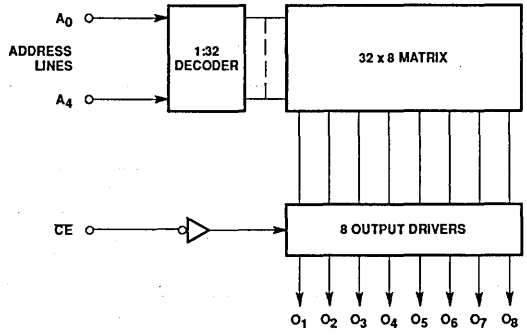
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High (82S23A)	+5.5	V_{DC}
V_O	Output voltage Off–State (82S123A)	+5.5	V_{DC}
T_A	Operating temperature range	–55 to +125	°C
T_{STG}	Storage temperature range	–65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar PROM (32 × 8) — 82S23A, 82S123A

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA			-1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High	I_O = -2mA, V_{CC} = 4.5V	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			50	µA
Output current						
		V_{CC} = 5.5V				
I_{OLK}	Leakage (82S23A)	$\overline{CE}$ = High, V_O = 5.5V			40	µA
I_{OZ}	Hi-Z state (82S123A)	$\overline{CE}$ = High, V_O = 5.5V			40	µA
		$\overline{CE}$ = High, V_O = 0.4V			-40	µA
I_{OS}	Short circuit (82S123A)[3]	V_{CC} = 5.5V, $\overline{CE}$ = Low, V_O = 0V, High stored	-20		-100	mA
Supply current						
I_{CC}		V_{CC} = 5.5V, $\overline{CE}$ = High			110	mA
Capacitance[6]						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

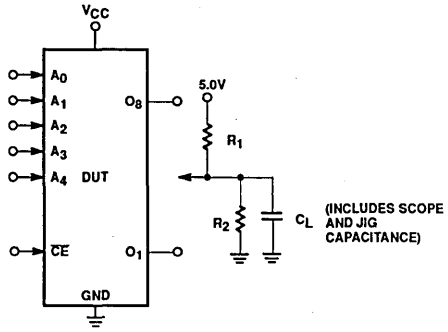
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		20	35	ns
t_{CE}		Output	Chip Enable			22	ns
t_{CD}	Disable time	Output	Chip Disable			22	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

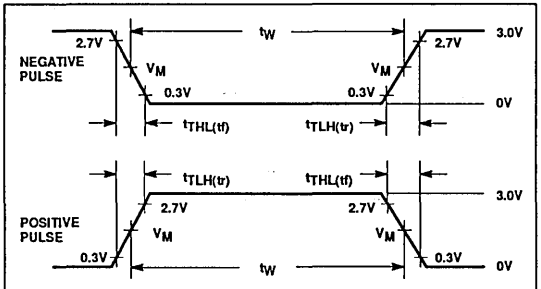
256-Bit TTL Bipolar PROM (32 × 8) — 82S23A, 82S123A

TEST LOAD CIRCUITS



NOTE:
$R_1 = 270\ \Omega$, $R_2 = 600\Omega$, $C_L = 50pF$.

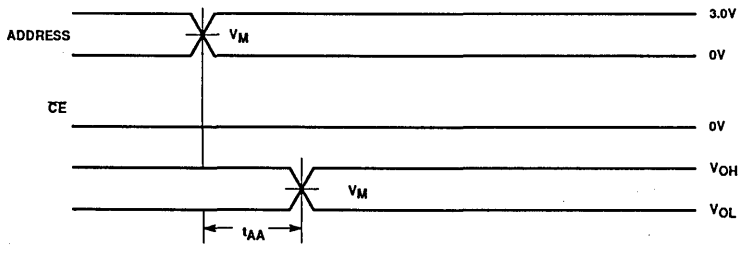
VOLTAGE WAVEFORMS



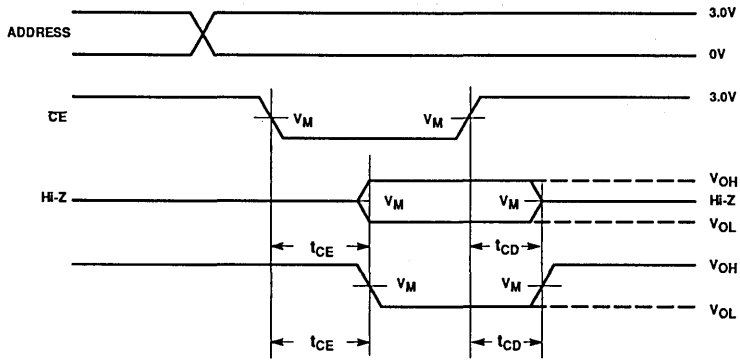
Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



$V_M = 1.5V$



$V_M = 1.5V$

Signetics

82S23B, 82S123B
256-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S23B and 82S123B are field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23B and 82S123B devices are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for memory expansion. They feature either Open collector or 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 30ns max
- Input loading: -150μA max
- On-chip address decoding
- One chip enable input
- Output options:
  - 82S23B: Open collector
  - 82S123B: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Format conversion
- Hardwired algorithms
- Random logic
- Code conversion

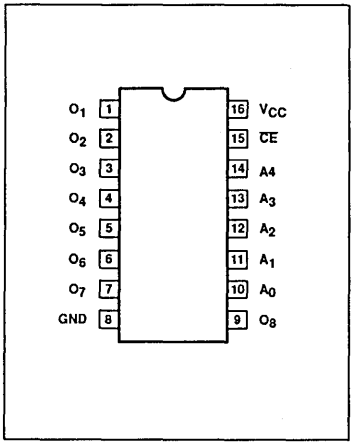
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-Pin Ceramic Dual-In-Line 300mil-wide	82S23B/BEA, 82S123B/BEA
16-Pin Ceramic FlatPack	82S23B/BFA, 82S123B/BFA

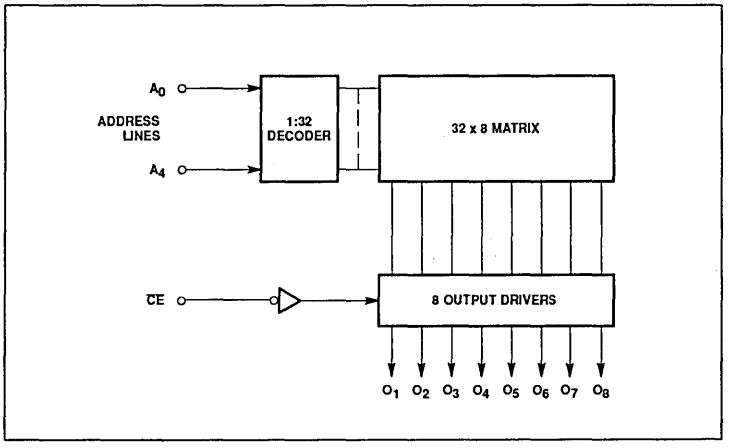
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High (82S23)	+5.5	V_{DC}
V_O	Output voltage Off-State (82S123)	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



256-Bit TTL Bipolar PROM (32 × 8) — 82S23B, 82S123B

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}[7]	Low				0.8	V
V_{IH}[7]	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA			-1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High (82S123B)	V_{CC} = 4.5V, I_O = -2mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH1}	High	V_I = 2.7V			25	µA
I_{IH2}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = 5.5V				
I_{OLK}	Leakage (82S23B)	$\overline{CE}$ = High, V_O = 5.5V			40	µA
I_{OZ}	Hi-Z state (82S123B)	$\overline{CE}$ = High, V_O = 5.5V			40	µA
		$\overline{CE}$ = High, V_O = 0.4V			-40	µA
I_{OS}	Short circuit (82S123B)[3]	V_{CC} = 5.5V, $\overline{CE}$ = Low, V_O = 0V, High stored	-20		-100	mA
Supply current						
I_{CC}		$\overline{CE}$ = High, V_{CC} = 5.5V			96	mA
Capacitance[6]						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

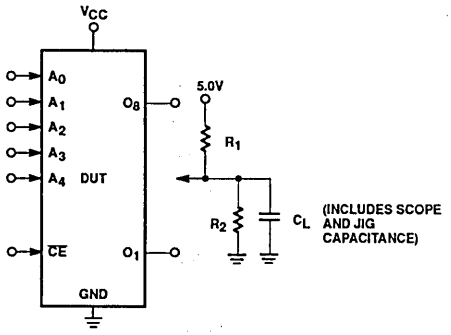
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		20	30	ns
t_{CE}	Access time[4]	Output	Chip Enable			18	ns
t_{CD}	Disable time	Output	Chip Disable			18	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed but not tested.
7. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.

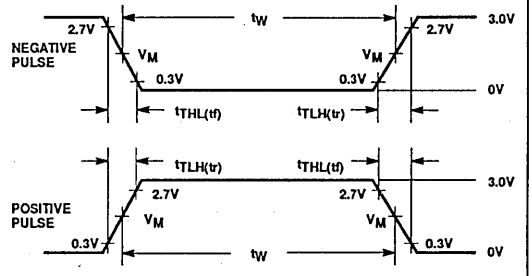
256-Bit TTL Bipolar PROM (32 × 8) — 82S23B, 82S123B

TEST LOAD CIRCUITS



NOTE:
R_1 = 270 Ω, R_2 = 600Ω, C_L = 50pF.

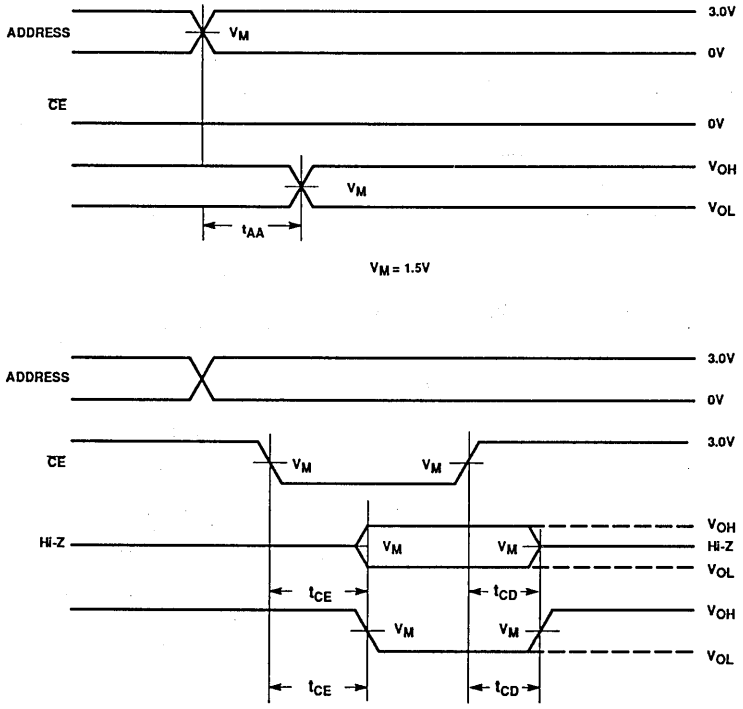
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



V_M = 1.5V

V_M = 1.5V

Signetics

82S126
82S129
1K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126 and 82S129 devices are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either Open collector or 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 60ns max
- Input loading: -150μA max
- On-chip address decoding
- Two chip enable inputs
- Output options:
  - 82S126: Open collector
  - 82S129: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

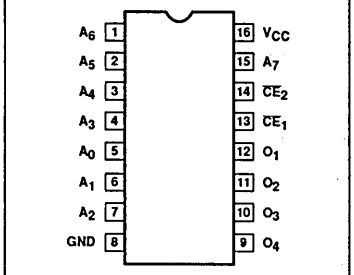
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic Dual-In-Line 300mil-wide	82S126/BEA, 82S129/BEA
16-pin Ceramic FlatPack	82S126/BFA, 82S129/BFA

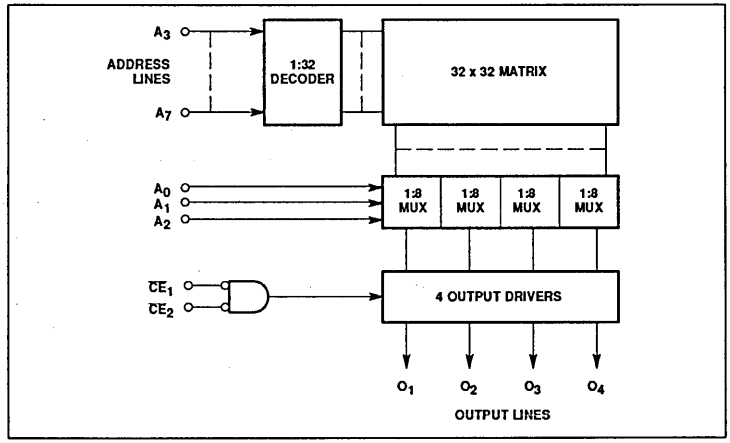
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High (82S126)	+5.5	V_{DC}
V_O	Output voltage Off-State (82S129)	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



1K-Bit TTL Bipolar PROM (256 × 4) — 82S126, 82S129

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA			-1.2	V
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High (82S129)	V_{CC} = 4.5V, I_O = -2.0mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = 5.5V				
I_{OLK}	Leakage (82S126)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_O = 5.5V			40	µA
I_{OZ}	Hi-Z state (82S129)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_O = 5.5V			40	µA
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_O = 0.4V			-40	µA
I_{OS}	Short circuit (82S129)[3]	V_{CC} = 5.5V, $\overline{CE}_{1,2}$ = Low, V_O = 0V, High stored	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{CC} = 5.5V			125	mA
Capacitance[6]						
		CE_1 or CE_2 = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

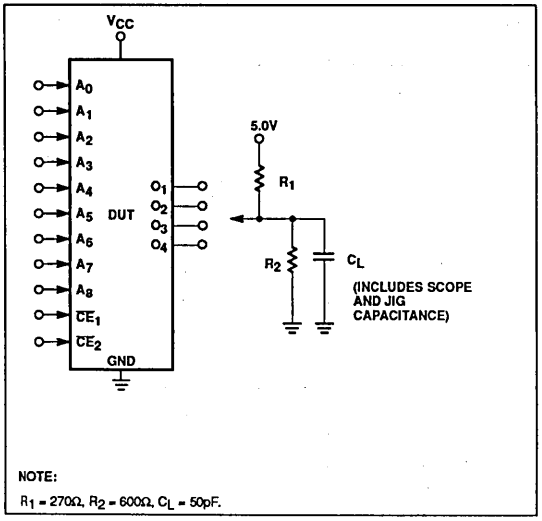
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		40	60	ns
t_{CE}	Access time[4]	Output	Chip Enable			30	ns
t_{CD}	Disable time	Output	Chip Disable			30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

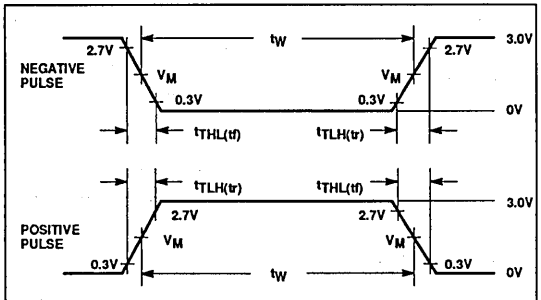
1K-Bit TTL Bipolar PROM (256 × 4) — 82S126, 82S129

TEST LOAD CIRCUITS



NOTE:
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 50pF$.

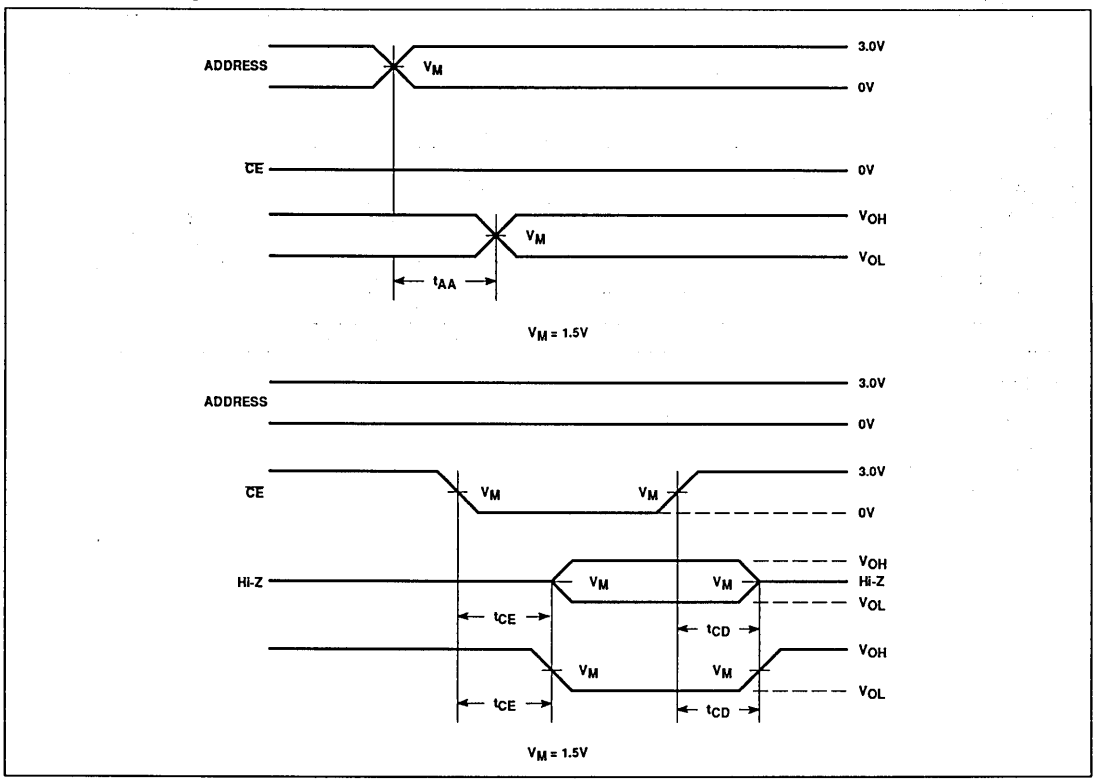
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



Signetics

82S126A
82S129A
1K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S126A and 82S129A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S126A and 82S129A devices are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either Open collector or 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 35ns max
- Input loading: -150μA max
- On-chip address decoding
- Output options:
  - 82S126A: Open collector
  - 82S129A: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

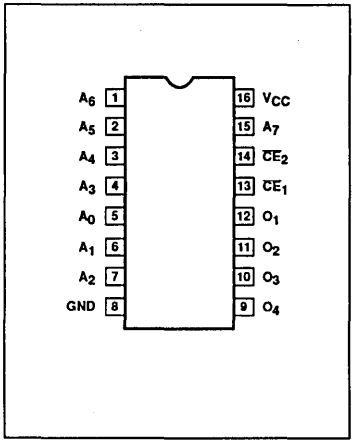
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic Dual-In-Line 300mil-wide	82S126A/BEA, 82S129A/BEA
16-pin Ceramic FlatPack	82S126A/BFA, 82S129A/BFA

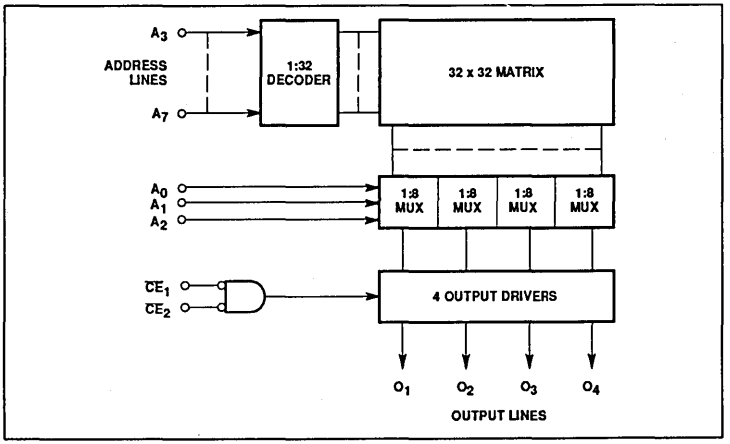
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High (82S126A)	+5.5	V_{DC}
V_O	Output voltage Off-State (82S129A)	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



1K-Bit TTL Bipolar PROM (256 × 4) — 82S126A, 82S129A

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA			-1.2	V
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High (82S129A)	V_{CC} = 4.5V, I_O = -2.0mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = 5.5V				
I_{OLK}	Leakage (82S126A)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_O = 5.5V			40	µA
I_{OZ}	Hi-Z state (82S129A)	$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_O = 5.5V			40	µA
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_O = 0.4V			-40	µA
I_{OS}	Short circuit (82S129A)[3]	V_{CC} = 5.5V, $\overline{CE}_{1,2}$ = Low, V_O = 0V, High stored	-15		-85	mA
Supply current[3]						
I_{CC}		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{CC} = 5.5V			125	mA
Capacitance[6]						
		$\overline{CE}_1$ or $\overline{CE}_2$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

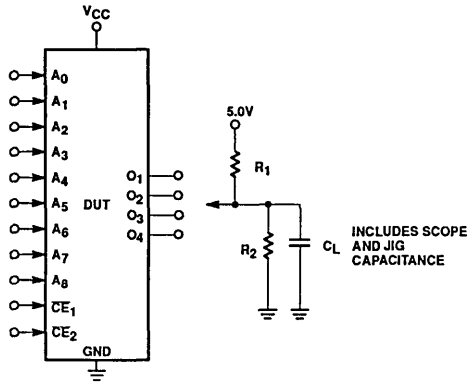
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		17	35	ns
t_{CE}	Access time[4]	Output	Chip Enable		10	20	ns
t_{CD}	Disable time	Output	Chip Disable		6	15	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

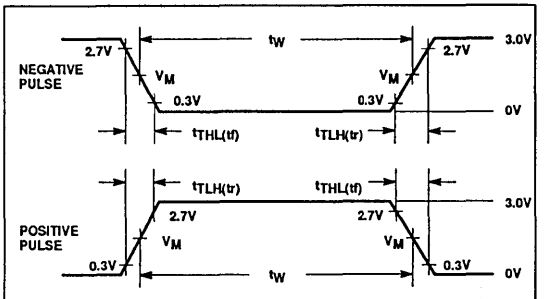
1K-Bit TTL Bipolar PROM (256 × 4) — 82S126A, 82S129A

TEST LOAD CIRCUITS



NOTE: R_1 = 270Ω, R_2 = 600Ω, C_L = 50pF.

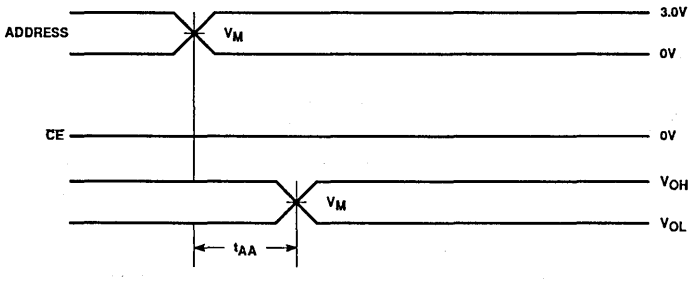
VOLTAGE WAVEFORMS



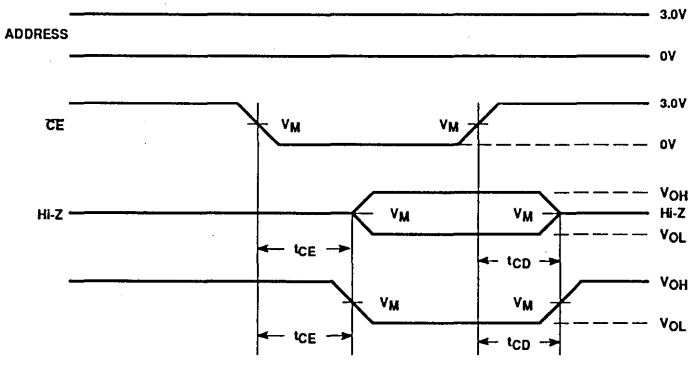
Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



V_M = 1.5V



V_M = 1.5V

Signetics

82S130
82S131
2K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S130 and the 82S131 are field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S130 and 82S131 are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either Open collector or 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 60ns max
- Input loading: -150μA max
- On-chip address decoding
- One chip enable input
- Output options:
  - 82S130: Open collector
  - 82S131: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

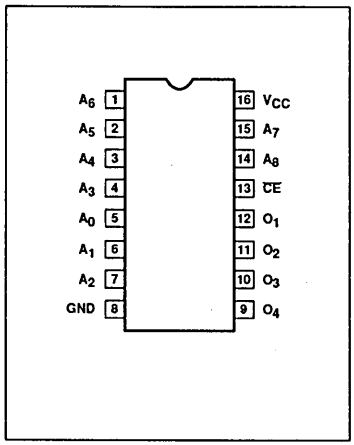
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic Dual-In-Line 300mil-wide	82S130/BEA, 82S131/BEA
16-pin Ceramic Flat Pack	82S130/BFA, 82S131/BFA

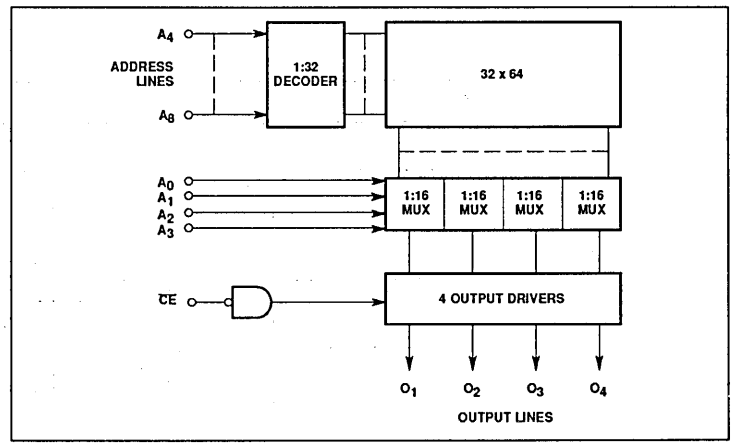
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High (82S130)	+5.5	V_{DC}
V_O	Output voltage Off-State (82S131)	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (512 × 4) — 82S130, 82S131

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low			0.8		V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA			-1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High (82S131)	V_{CC} = 4.5V, I_O = -2mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current[1]						
		V_{CC} = 5.5V				
I_{OLK}	Leakage (82S130)	$\overline{CE}$ = High, V_O = 5.5V			40	µA
I_{OZ}	Hi-Z state (82S131)	$\overline{CE}$ = High, V_O = 5.5V			40	µA
		$\overline{CE}$ = High, V_O = 0.5V			-40	µA
I_{OS}	Short circuit (82S131)[3]	V_{CC} = 5.5V, $\overline{CE}$ = Low, V_O = 0V, High stored	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}$ = High, V_{CC} = 5.5V			130	mA
Capacitance[6]						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

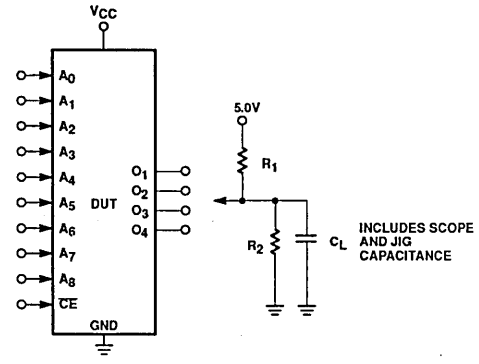
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address			60	ns
t_{CE}	Access time[4]	Output	Chip Enable			30	ns
t_{CD}	Disable time	Output	Chip Disable			30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

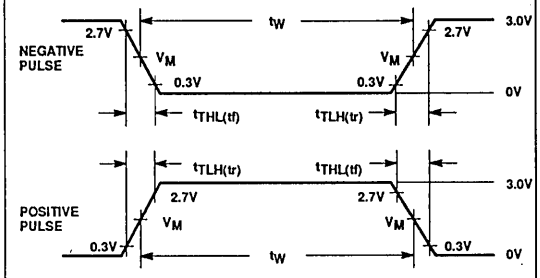
2K-Bit TTL Bipolar PROM (512 × 4) — 82S130, 82S131

TEST LOAD CIRCUITS



NOTE: $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 50pF$.

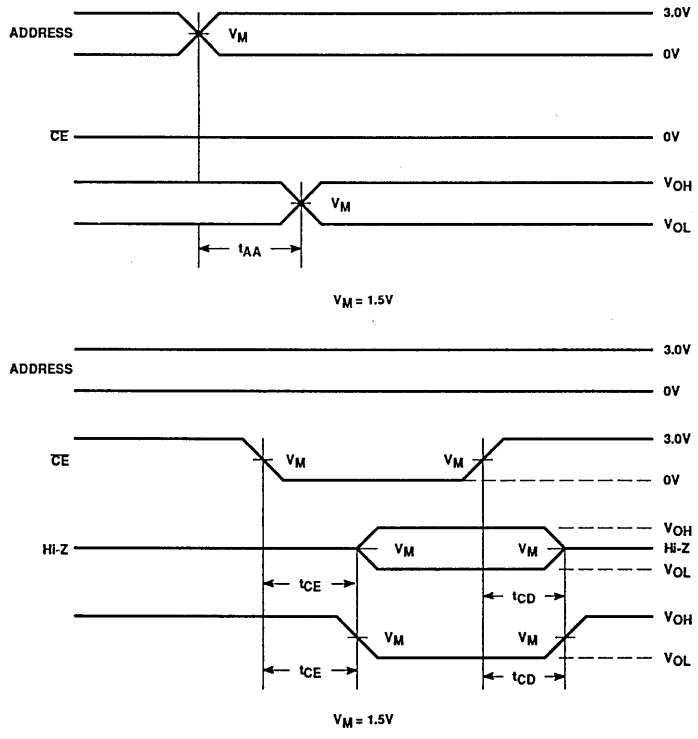
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



Signetics

82S130A
82S131A
2K-Bit TTL Bipolar PROM

Product Specification

Military Bipolar Memory Products

DESCRIPTION

The 82S130A and 82S131A are field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S130A and 82S131A are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either Open collector or 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 35ns max
- Input loading: -150μA max
- On-chip address decoding
- One chip enable input
- Output options:
  - 82S130A: Open collector
  - 82S131A: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

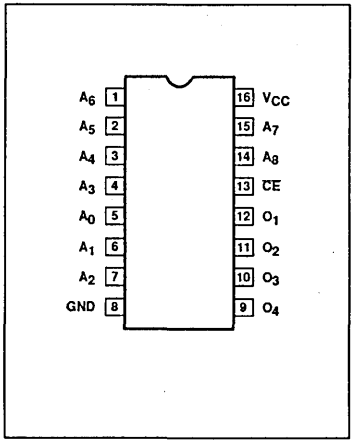
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Ceramic Dual-In-Line 300mil-wide	82S130A/BEA, 82S131A/BEA
16-pin Ceramic Flat Pack	82S130A/BFA, 82S131A/BFA

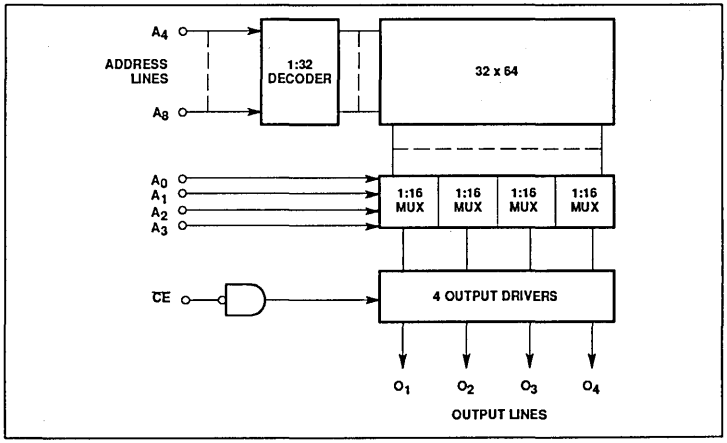
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage High (82S130A)	+5.5	V_{DC}
V_O	Output voltage Off-State (82S131A)	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



2K-Bit TTL Bipolar PROM (512 × 4) — 82S130A, 82S131A

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA			-1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High (82S131A)	V_{CC} = 4.5V, I_O = -2mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = 5.5V				
I_{OLK}	Leakage (82S130A)	$\overline{CE}$ = High, V_O = 5.5V			40	µA
I_{OZ}	Hi-Z state (82S131A)	$\overline{CE}$ = High, V_O = 5.5V			40	µA
		$\overline{CE}$ = High, V_O = 0.5V			-40	µA
I_{OS}	Short circuit (82S131A)[3]	V_{CC} = 5.5V, $\overline{CE}$ = Low, V_O = 0V, High stored	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}$ = High, V_{CC} = 5.5V			130	mA
Capacitance[6]						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

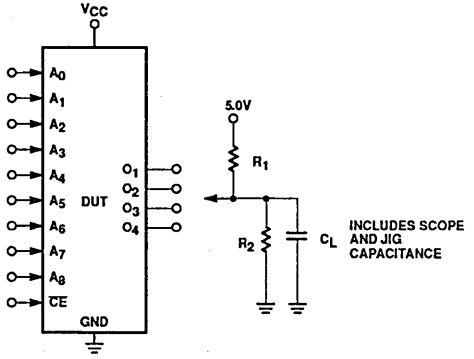
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		18	35	ns
t_{CE}	Access time[4]	Output	Chip Enable		10	20	ns
t_{CD}	Disable time	Output	Chip Disable		6	15	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

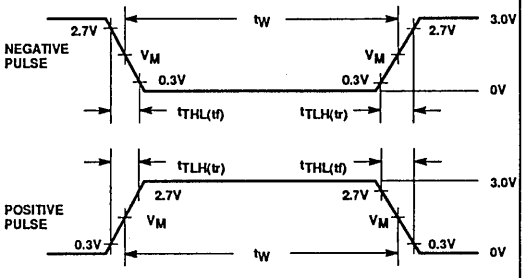
2K-Bit TTL Bipolar PROM (512 × 4) — 82S130A, 82S131A

TEST LOAD CIRCUITS



NOTE: R_1 = 270Ω, R_2 = 600Ω, C_L = 50pF.

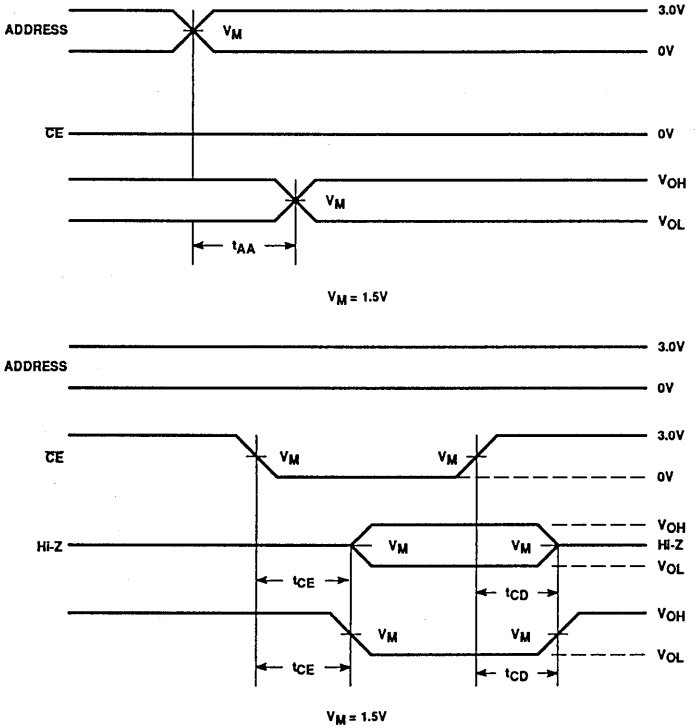
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



Signetics

82S137
4K-Bit TTL Bipolar PROM

Product Specification

Military Bipolar Memory Products

DESCRIPTION

The 82S137 is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S137 is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- **Address access time: 70ns max**
- **Input loading: -150μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**
- **Two chip enable inputs**
- **Outputs: 3-State**

APPLICATIONS

- **Sequential controllers**
- **Control store**
- **Random logic**
- **Code conversion**

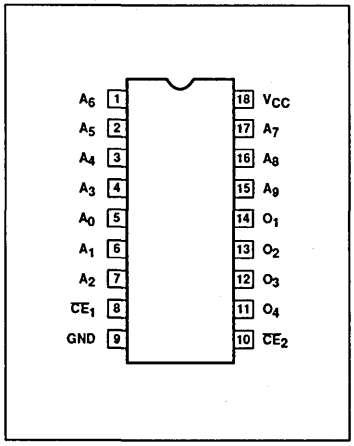
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Ceramic Dual-In-Line 300mil-wide	82S137/BVA
18-pin Ceramic FlatPack	82S137/BYA

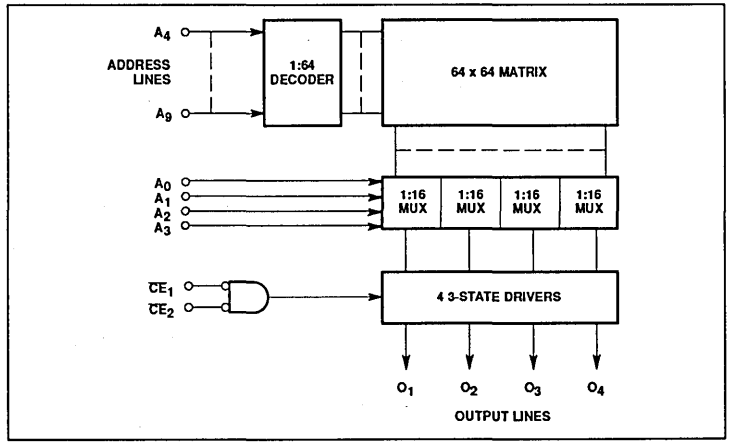
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



4K-Bit TTL Bipolar PROM (1024 × 4) — 82S137

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA			-1.2	V
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High	V_{CC} = 4.5V, I_O = -2mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z state	$\overline{CE}_{1,2}$ = High, V_O = 0.5V			-40	µA
		$\overline{CE}_{1,2}$ = High, V_O = 5.5V			40	µA
I_{OS}	Short circuit[3]	V_{CC} = 5.5V, $\overline{CE}_{1,2}$ = Low, V_O = 0V, High stored	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}_{1,2}$ = High, V_{CC} = 5.5V			140	mA
Capacitance[6]						
		$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

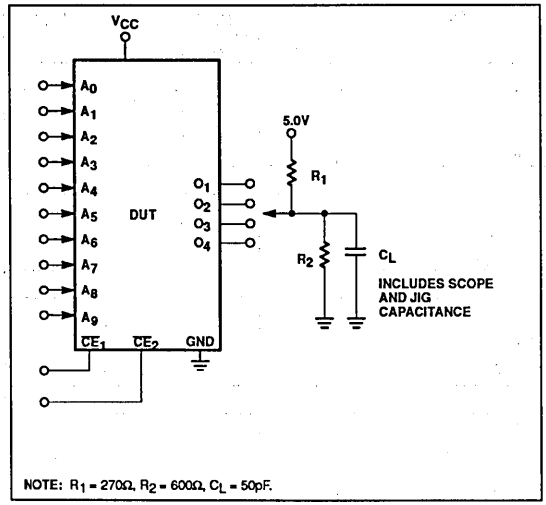
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		40	70	ns
t_{CE}	Access time[4]	Output	Chip Enable		25	30	ns
t_{CD}	Disable time	Output	Chip Disable		25	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed but not tested.

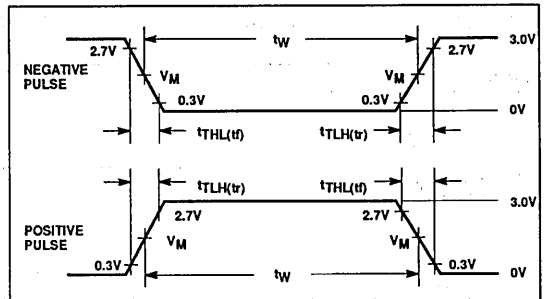
4K-Bit TTL Bipolar PROM (1024 × 4) — 82S137

TEST LOAD CIRCUITS



NOTE: $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 50pF$.

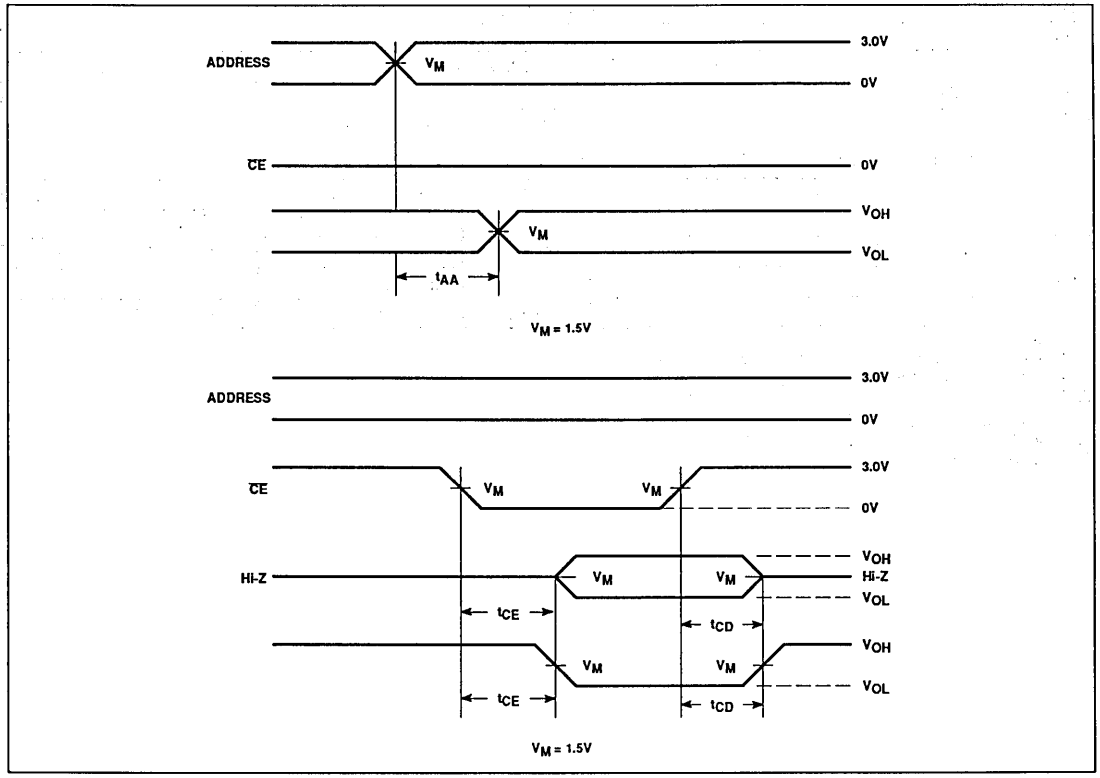
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



Signetics

82S137A
4K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S137A is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S137A is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 55ns max
- Input loading: -150μA max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- Two chip enable inputs
- Outputs: 3-State

APPLICATIONS

- Sequential controllers
- Control store
- Random logic
- Code conversion

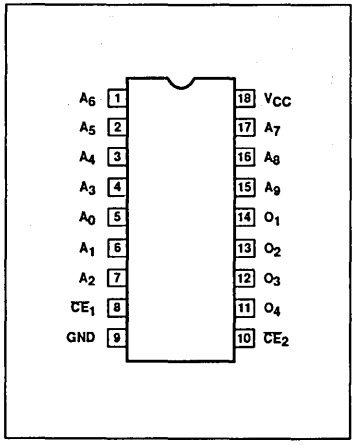
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Ceramic Dual-In-Line 300mil-wide	82S137A/BVA
18-pin Ceramic FlatPack	82S137A/BYA

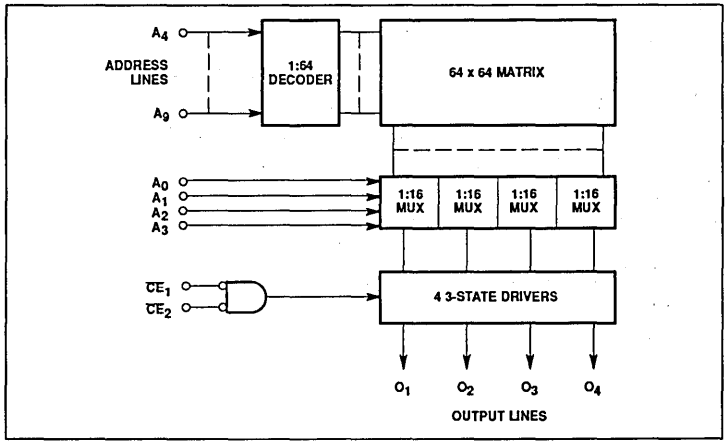
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



4K-Bit TTL Bipolar PROM (1024 × 4) — 82S137A

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage						
		$\overline{CE}_{1,2}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High	V_{CC} = 4.5V, I_O = -2mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z state	$\overline{CE}_{1,2}$ = High, V_O = 5.5V			40	µA
		$\overline{CE}_{1,2}$ = High, V_O = 0.5V			-40	µA
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, V_O = 0V V_{CC} = 5.5V, High stored	-15		-85	mA
Supply current						
I_{CC}		V_{CC} = 5.5V, $\overline{CE}_{1,2}$ = High		85	140	mA
Capacitance[6]						
		$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

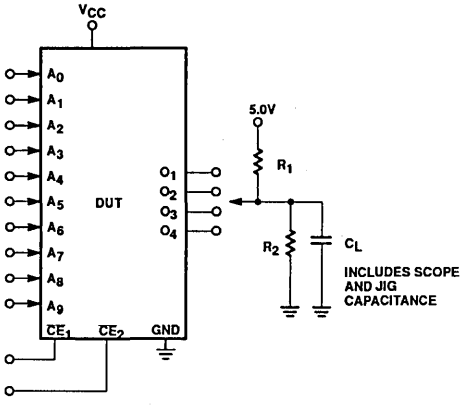
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		35	55	ns
t_{CE}	Access time[4]	Output	Chip Enable		20	30	ns
t_{CD}	Disable time	Output	Chip Disable		20	30	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

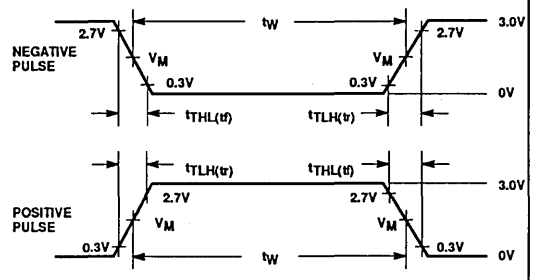
4K-Bit TTL Bipolar PROM (1024 × 4) — 82S137A

TEST LOAD CIRCUITS



NOTE: R_1 = 270Ω, R_2 = 600Ω, C_L = 50pF.

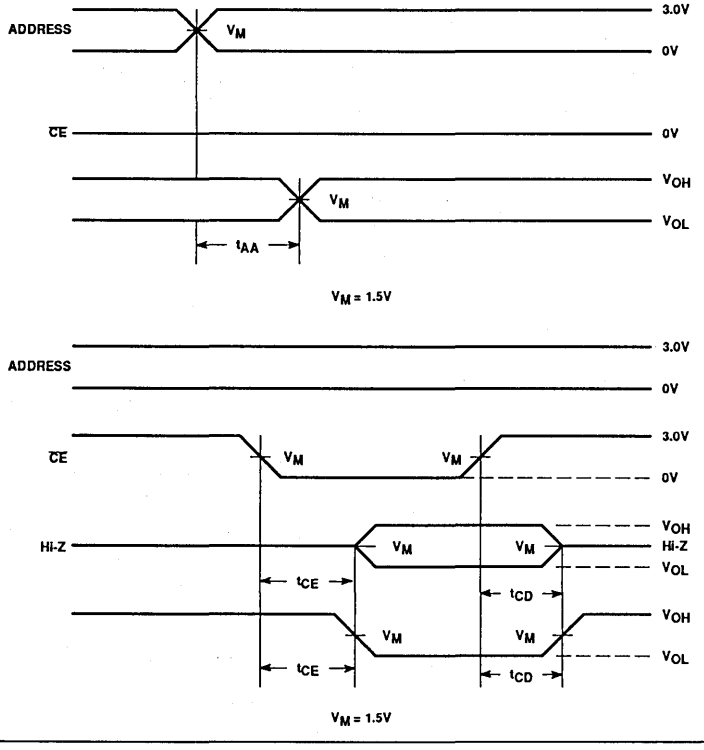
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAM



Signetics

82S141
4K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S141 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S141 includes on-chip decoding and four chip enable inputs for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 90ns max
- Input loading: -150μA max
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible
- Outputs: 3-State
- Unprogrammed outputs are Low level

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

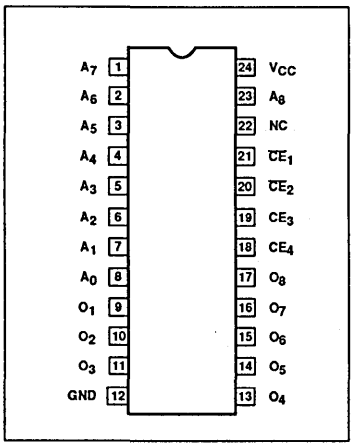
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Ceramic Dual-In-Line 600mil-wide	82S141/BJA
24-pin Ceramic Flat Pack	82S141/BKA

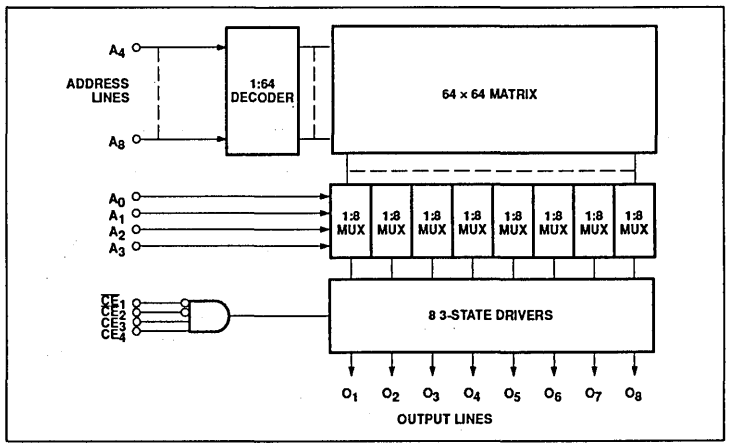
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



4K-Bit TTL Bipolar PROM (512 × 8) — 82S141

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage						
V_{OL}	Low	V_{CC} = 4.5V, $\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High I_O = 9.6mA			0.5	V
V_{OH}	High	I_O = -2mA	2.4			V
Input current						
I_{IL}	Low	V_{CC} = 5.5V V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
I_{OZ}	Hi-Z state	V_{CC} = 5.5V $\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_O = 5.5V			+40	µA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_O = 0.4V			-40	µA
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, V_O = 0V V_{CC} = 5.5V, High Stored	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low V_{CC} = 5.5V		125	165	mA
Capacitance[6]						
C_{IN}	Input	V_{CC} = 5.0V, $\overline{CE}_{1,2}$ = High V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

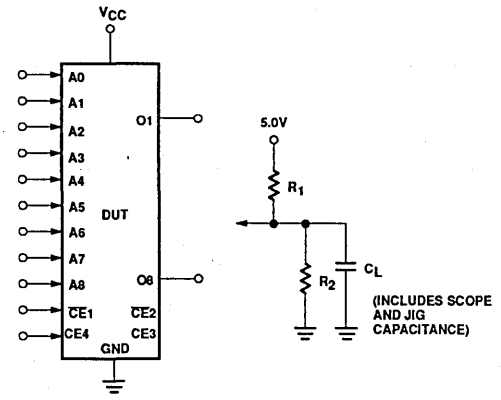
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		50	90	ns
t_{CE}		Output	Chip enable		20	50	ns
t_{CD}	Disable time	Output	Chip disable		20	50	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

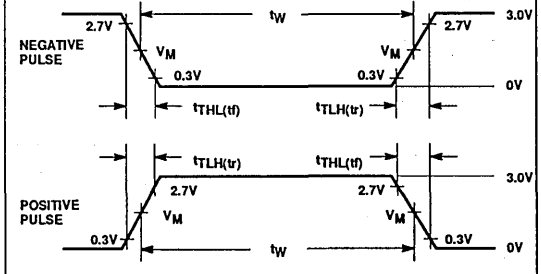
4K-Bit TTL Bipolar PROM (512 × 8) — 82S141

TEST LOAD CIRCUITS



NOTE: $R_1 = 470\Omega$, $R_2 = 1000\Omega$, $C_L = 50pF$

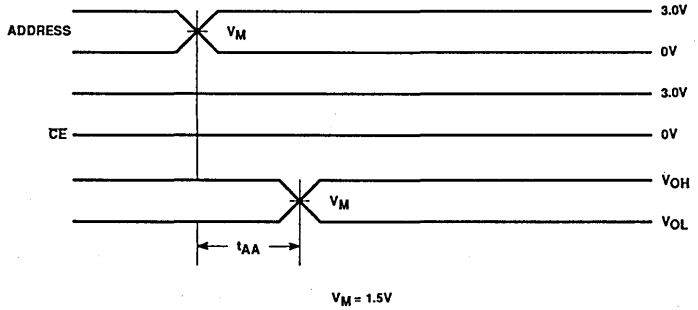
VOLTAGE WAVEFORMS



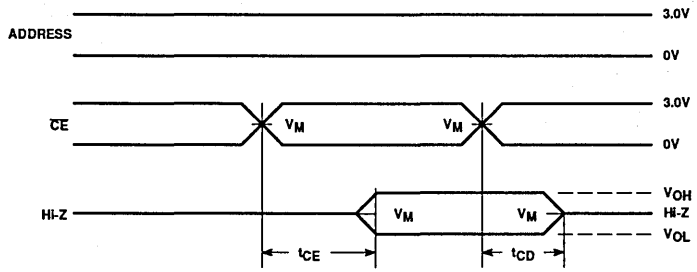
Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



$V_M = 1.5V$



$V_M = 1.5V$

Signetics

82S147
82S147A
4K-Bit TTL Bipolar PROM

Product Specification

Military Bipolar Memory Products

DESCRIPTION

The 82S147 and 82S147A are field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S147 and 82S147A include on-chip decoding and one chip enable input for ease of memory expansion, and feature 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 75ns max
- Input loading: -150μA max
- One chip enable input
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible
- Outputs: 3-State
- Unprogrammed outputs are Low level

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

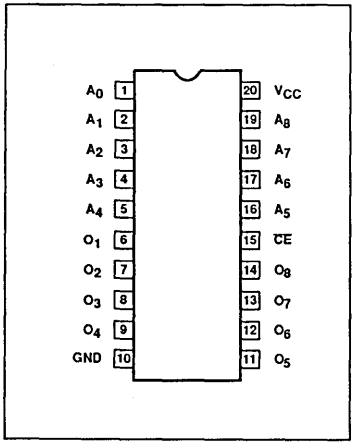
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Ceramic Dual-In-Line 300mil-wide	82S147/BRA, 82S147A/BRA

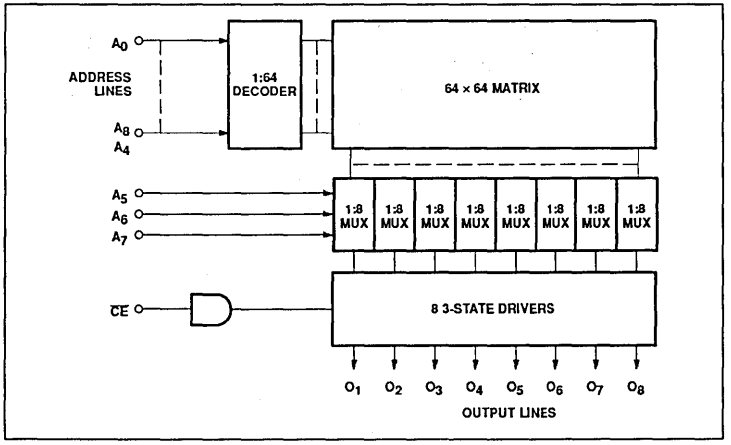
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



4K-Bit TTL Bipolar PROM (512 × 8) — 82S147, 82S147A

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{iH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage						
		V_{CC} = 4.5V, $\overline{CE}$ = Low				
V_{OL}	Low	I_O = 9.6mA			0.5	V
V_{OH}	High	I_O = -2mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z state	$\overline{CE}$ = High, V_O = 5.5V			40	µA
		$\overline{CE}$ = High, V_O = 0.5V			-40	µA
I_{OS}	Short circuit[3]	V_{CC} = 5.5V, $\overline{CE}$ = Low, V_O = 0V	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}$ = High, V_{CC} = 5.5V		125	160	mA
Capacitance[6]						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

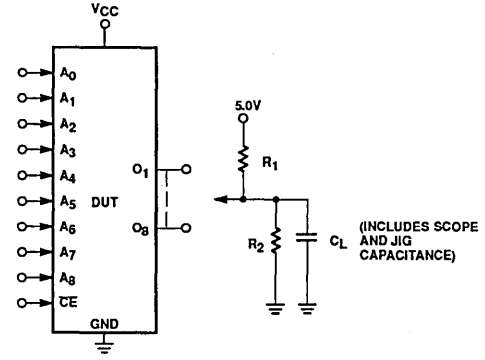
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	82S147			82S147A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		45	75		45	55	ns
t_{CE}	Access time[4]	Output	Chip Enable		20	45		20	30	ns
t_{CD}	Disable time	Output	Chip Disable		20	45		20	30	ns

NOTES:
1. All voltage values are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

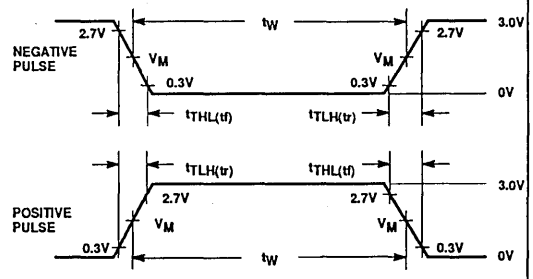
4K-Bit TTL Bipolar PROM (512 × 8) — 82S147, 82S147A

TEST LOAD CIRCUITS



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF

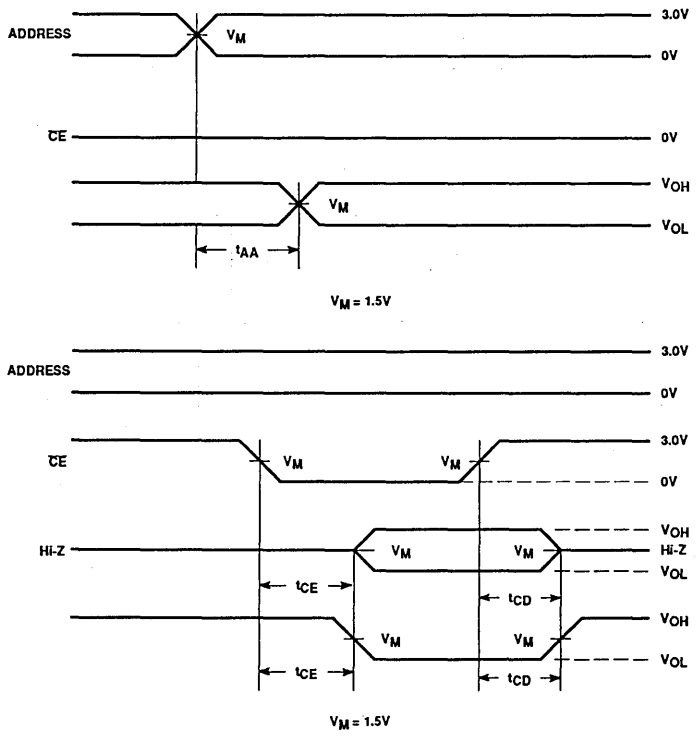
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



Signetics

82S147B

4K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S147B is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

The 82S147B includes on-chip decoding and one chip enable input for ease of memory expansion, and features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 45ns max
- Input loading: -150μA max
- One chip enable input
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible
- Outputs: 3-State
- Unprogrammed outputs are Low level

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

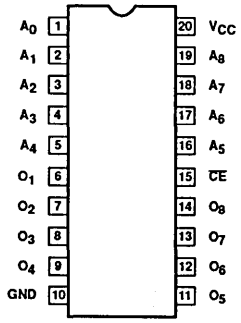
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Ceramic Dual-In-Line 300mil-wide	82S147B/BRA

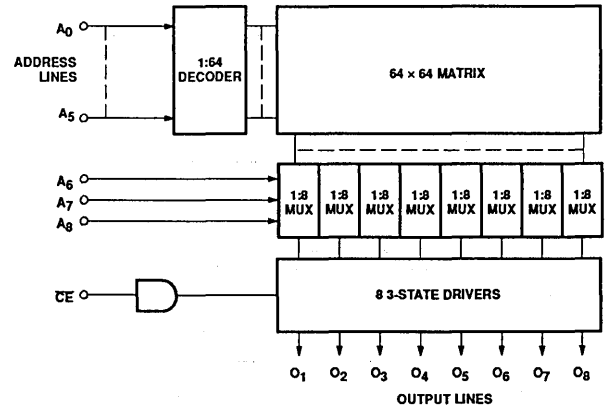
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



4K-Bit TTL Bipolar PROM (512 × 8) — 82S147B

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage range	4.5	5.0	5.5	V
V_{IH}[7]	High level Input voltage	2.0			V
V_{IL}[7]	Low level Input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High level output current			-2	mA
I_{OL}	Low level output current			9.6	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
V_{IK}	Input clamp voltage	V_{CC} = Min, I_{IK} = Max		-0.8	-1.2	V
V_{OL}	Output Low voltage	V_{CC} = Min, $\overline{CE}$ = V_{IL}, I_{OL} = Max			0.5	V
V_{OH}	Output High voltage	V_{CC} = Min, I_{OH} = Max, $\overline{CE}$ = V_{IL}	2.4			V
I_{IL}	Input Low current	V_{CC} = Max, V_I = 0.45V			-150	µA
I_{IH}	Input High current	V_I = 5.5V, V_{CC} = Max			40	µA
I_{OHZ}	Off-State Output current High level	$\overline{CE}$ = High, V_{CC} = 5.5V, V_O = 5.5V			+40	µA
I_{OLZ}	Off-State Output current Low level	V_{CC} = 5.5V, $\overline{CE}$ = High, V_O = 4.0V			-40	µA
I_{OS}	Short circuit Output current[3]	V_{CC} = 5.5V, $\overline{CE}$ = Low, V_O = 0V	-15		-85	mA
I_{CC}	Supply current	$\overline{CE}$ = High, V_{CC} = 5.5V		125	160	mA
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input Capacitance[6]	V_I = 2.0V		5	10	pF
C_{OUT}	Output Capacitance[6]	V_O = 2.0V		8	13	pF

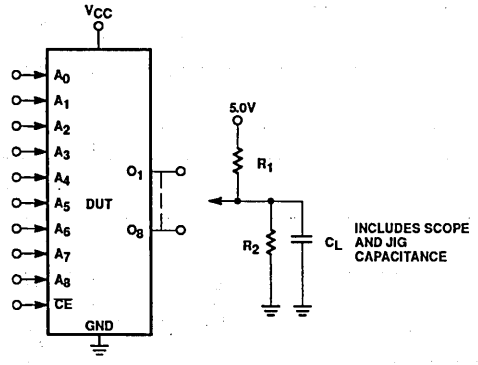
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		30	45	ns
t_{CE}	Enable time[4]	Output	Chip Enable		15	25	ns
t_{CD}	Disable time	Output	Chip Disable		15	25	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground terminal.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.
7. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.

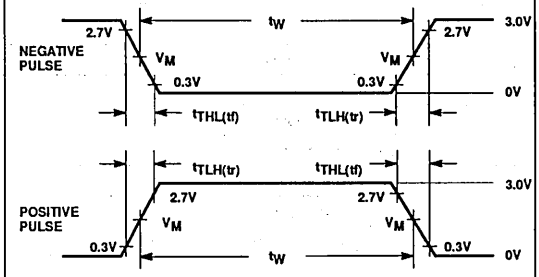
4K-Bit TTL Bipolar PROM (512 × 8) — 82S147B

TEST LOAD CIRCUITS



NOTE: $R_1 = 470\Omega$, $R_2 = 1K\Omega$, $C_L = 50pF$.

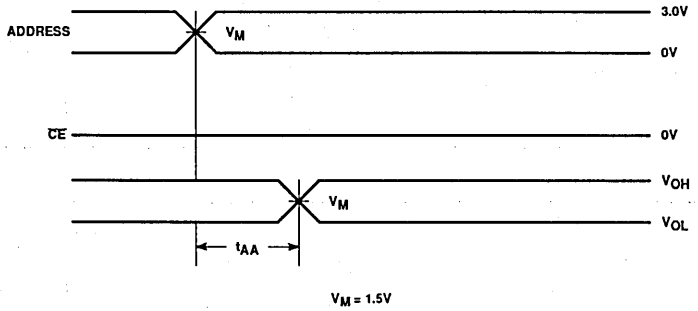
VOLTAGE WAVEFORMS



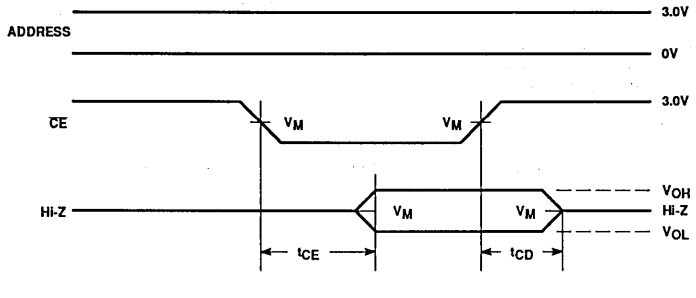
Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



$V_M = 1.5V$



$V_M = 1.5V$

Signetics

82S181
8K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S181 is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S181 is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 90ns max
- Input loading: -150μA max
- On-chip address decoding
- Four chip enable inputs
- Outputs: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

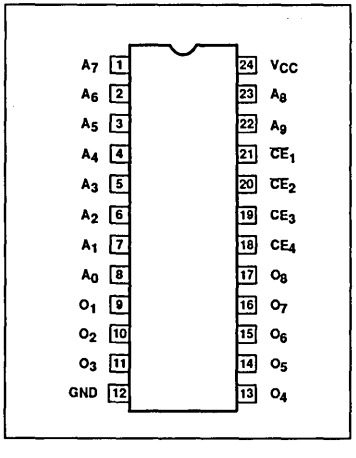
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Ceramic Dual-In-Line 600mil-wide	82S181/BJA
24-pin Ceramic Flat Pack	82S181/BKA
28-Pin Ceramic LLCC	82S181/B3A

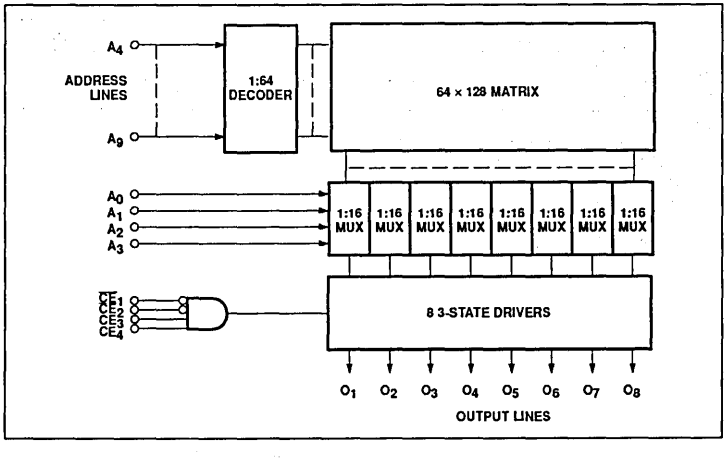
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (1024 × 8) — 82S181

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage[2]						
		V_{CC} = 4.5V $\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High				
V_{OL}	Low	I_O = 9.6mA			0.5	V
V_{OH}	High	I_O = -2mA	2.4			V
Input current[1]						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current[1]						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z state	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_O = 5.5V			40	µA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_O = 0.4V			-40	µA
I_{OS}	Short circuit	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, V_O = 0V V_{CC} = 5.5V, High stored	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}_{1,2}$ = High, $\overline{CE}_{3,4}$ = Low, V_{CC} = 5.5V		125	185	mA
Capacitance[6]						
		$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

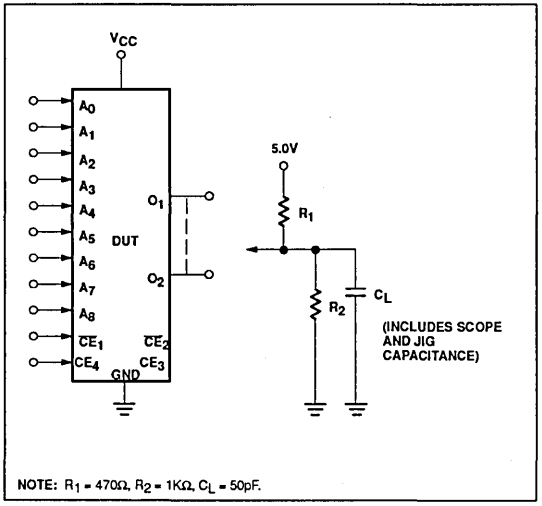
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		50	90	ns
t_{CE}	Access time[4]	Output	Chip Enable		20	50	ns
t_{CD}	Disable time	Output	Chip Disable		20	50	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

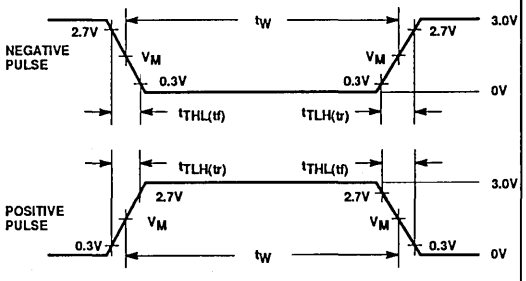
8K-Bit TTL Bipolar PROM (1024 × 8) — 82S181

TEST LOAD CIRCUITS



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF.

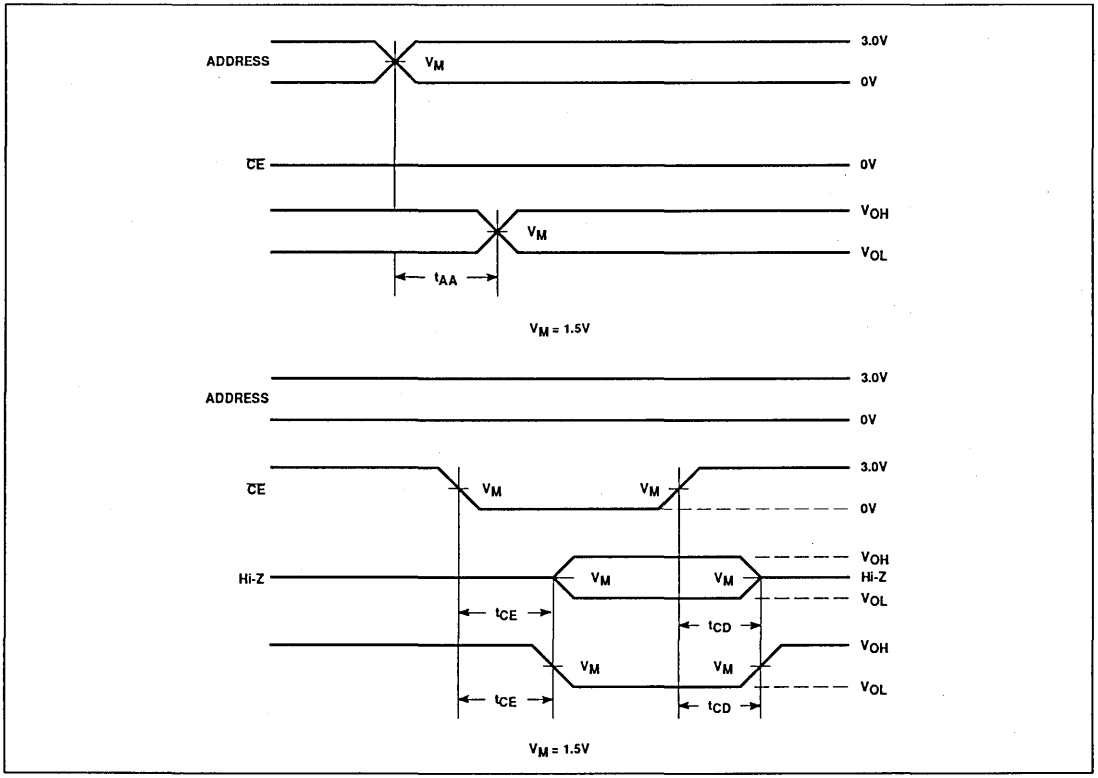
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



Signetics

82S181A

8K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S181A is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S181A is supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 55ns max
- Input loading: -150μA max
- On-chip address decoding
- Four chip enable inputs
- Outputs: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

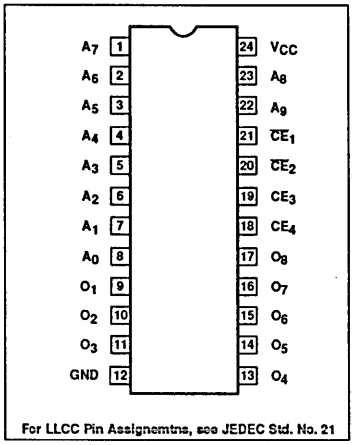
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Ceramic Dual-In-Line 600mil-wide	82S181A/BJA
24-pin Ceramic Flat Pack	82S181A/BKA
28-Pin Ceramic LLCC	82S181A/B3A

ABSOLUTE MAXIMUM RATINGS

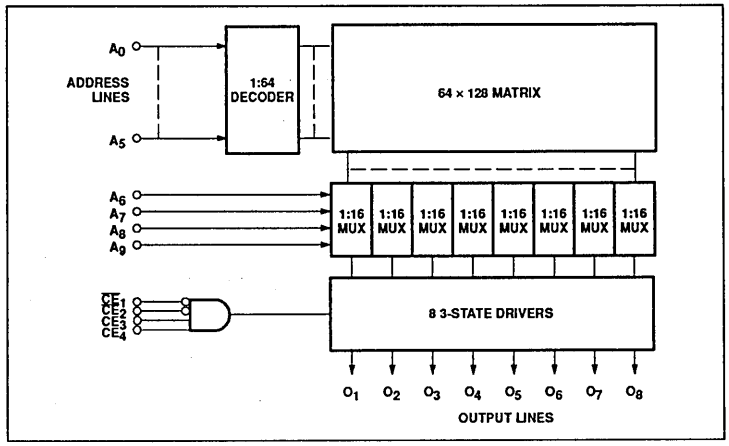
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC Pin Assignments, see JEDEC Std. No. 21

BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (1024 × 8) — 82S181A

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage[2]						
		V_{CC} = 4.5V, $\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High				
V_{OL}	Low	I_O = 9.6mA			0.5	V
V_{OH}	High	I_O = -2mA	2.4			V
Input current[1]						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current[1]						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z state	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_O = 5.5V			40	µA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_O = 0.4V			-40	µA
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, V_O = 0V V_{CC} = 5.5V, High stored	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}_{1,2}$ = High, $\overline{CE}_{3,4}$ = Low, V_{CC} = 5.5V		125	185	mA
Capacitance[6]						
		$\overline{CE}_{1,2}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

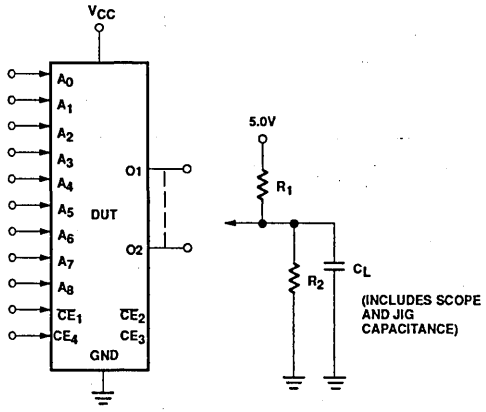
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		45	55	ns
t_{CE}	Access time[4]	Output	Chip Enable		25	40	ns
t_{CD}	Disable time	Output	Chip Disable		25	40	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

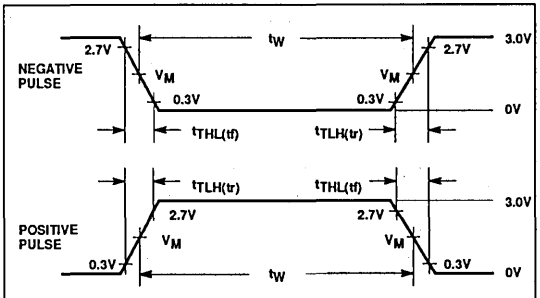
8K-Bit TTL Bipolar PROM (1024 × 8) — 82S181A

TEST LOAD CIRCUITS



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF.

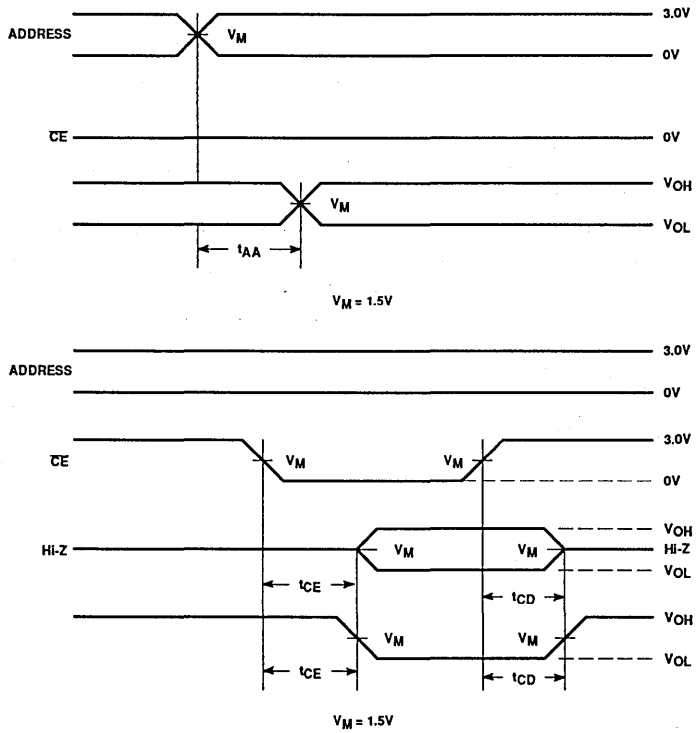
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



Signetics

82LS181

8K-Bit TTL Bipolar PROM (1024 × 8)

Military
Bipolar Memory Products

Product Specification

DESCRIPTION

The 82LS181 is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82LS181 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 120ns max
- Input loading: -150μA max
- On-chip address decoding
- Four chip enable inputs
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- Outputs: 3-State

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

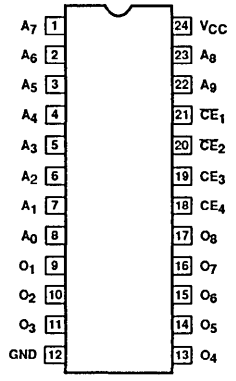
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic Dual-In-Line 600mil-wide	82LS181/BJA

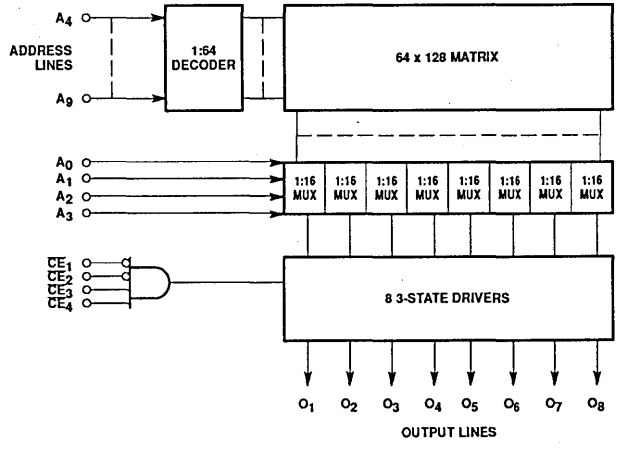
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (1024 × 8) — 82LS181

DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage[2]						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage[2]						
		V_{CC} = 4.5V, $\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High				
V_{OL}	Low	I_O = 4.8mA			0.5	V
V_{OH}	High	I_O = -1mA	2.4			V
Input current[1]						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current[1]						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z state	$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_O = 5.5V			40	µA
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_O = 0.4V			-40	µA
I_{OS}	Short circuit[3]	$\overline{CE}_{1,2}$ = Low, $CE_{3,4}$ = High, V_O = 0V, High stored	-10		-85	mA
Supply current						
I_{CC}		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_{CC} = 5.5V		60	85	mA
Capacitance[6]						
		$\overline{CE}_{1,2}$ = High, $CE_{3,4}$ = Low, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

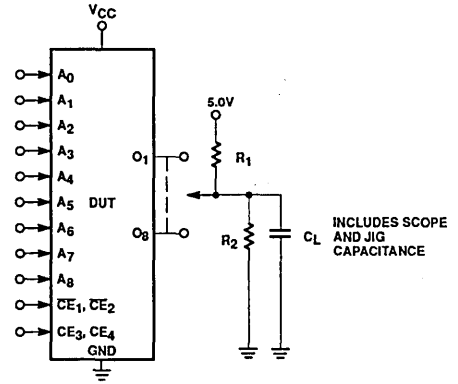
AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[8]	Max	
t_{AA}	Access time[4]	Output	Address		100	120	ns
t_{CE}		Output	Chip enable		35	50	ns
t_{CD}	Disable time	Output	Chip disable		35	50	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of the short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.
6. Guaranteed, but not tested.

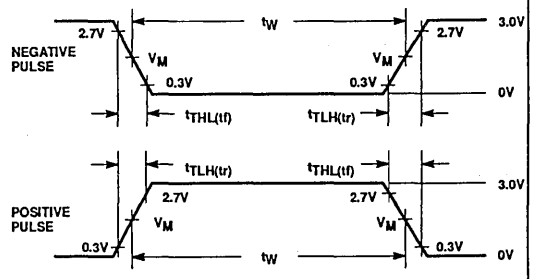
8K-Bit TTL Bipolar PROM (1024 × 8) — 82LS181

TEST LOAD CIRCUITS



NOTE:
R_1 = 1kΩ, R_2 = 3kΩ, C_L = 50pF.

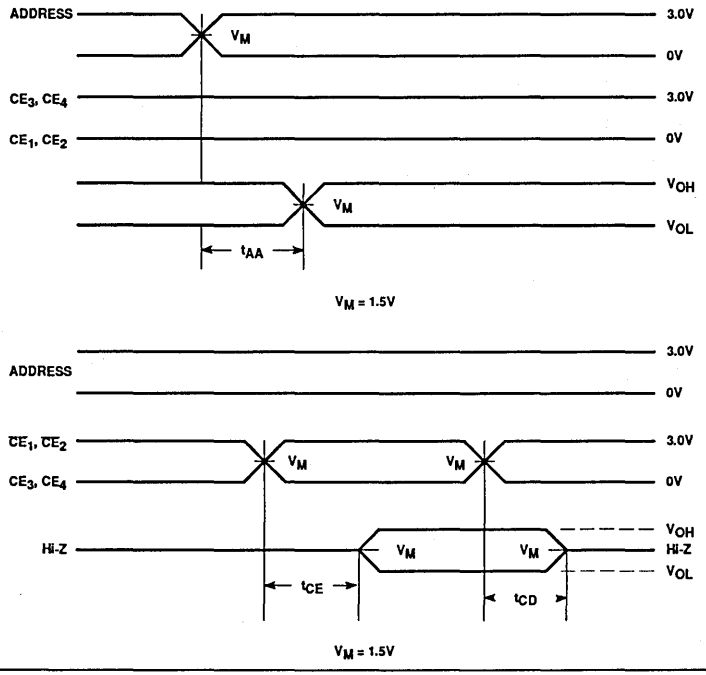
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



Signetics

82S185/185A/185B
8K-Bit TTL Bipolar PROM
(2048 × 4)

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S185 is field-programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The standard 82S185 is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and one chip enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 55ns max
- Input loading: -150μA max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- One chip enable input
- Outputs: 3-State

APPLICATIONS

- Sequential controllers
- Control store
- Random logic
- Code conversion

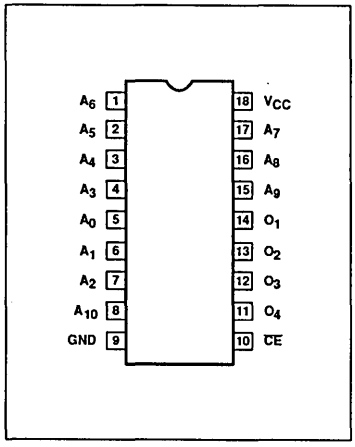
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-pin Ceramic Dual-In-Line 300mil-wide	82S185/BVA 82S185A/BVA 82S185B/BVA
18-pin Ceramic Flat Pack	82S185/BYA 82S185A/BYA 82S185B/BYA

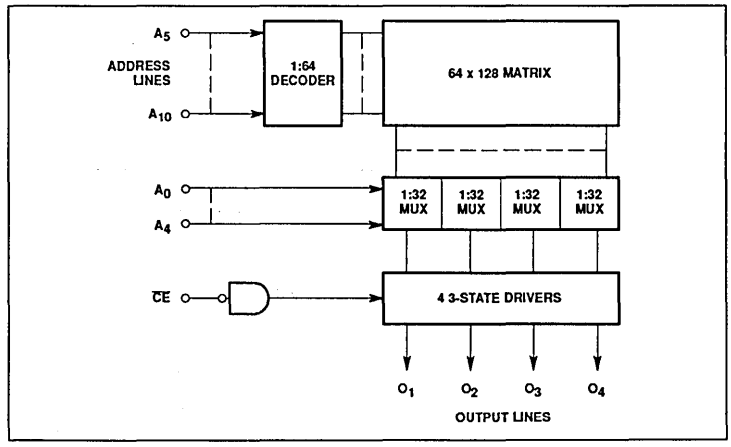
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



8K-Bit TTL Bipolar PROM (2048 × 4) — 82S185/185A/185B

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage						
		V_{CC} = 4.5V, $\overline{CE}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High	I_O = -2mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z state	$\overline{CE}$ = High, V_O = 0.4V			-40	µA
		$\overline{CE}$ = High, V_O = 5.5V			40	µA
I_{OS}	Short circuit[3]	$\overline{CE}$ = Low, V_O = 0V, High stored	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}$ = High, V_{CC} = 5.5V		90	130	mA
Capacitance[6]						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

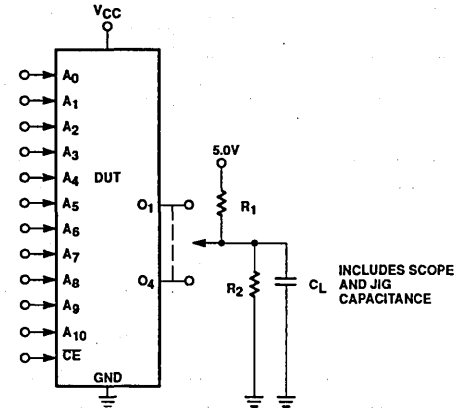
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER		TO	FROM	LIMITS			UNIT
					Min	Typ[5]	Max	
t_{AA}	Access time[4]	185	Output	Address		70	115	ns
		185A				25	55	ns
		185B				40	90	ns
t_{CE}	Access time[4]	185/185B	Output	Chip Enable		30	50	ns
		185A				15	30	ns
t_{CD}	Disable time	185/185B	Output	Chip Disable		30	50	ns
		185A				15	30	ns

NOTES:
1. All voltages are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.

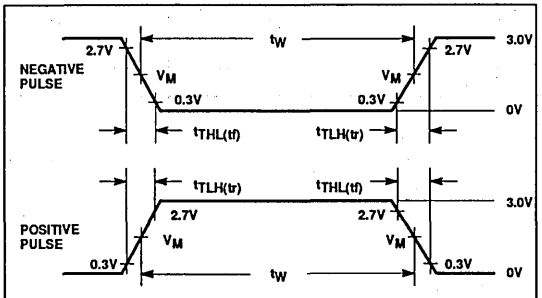
8K-Bit TTL Bipolar PROM (2048 × 4) — 82S185/185A/185B

TEST LOAD CIRCUITS



NOTE:
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 50pF$.

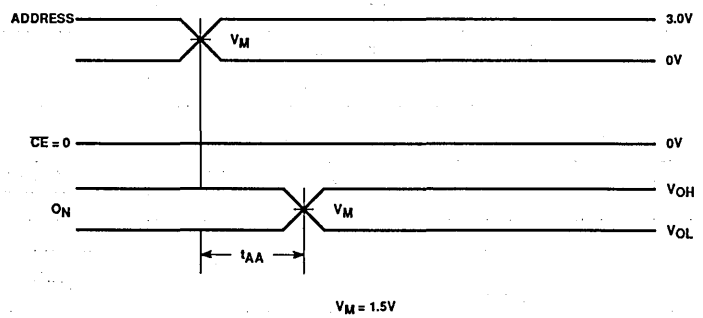
VOLTAGE WAVEFORMS

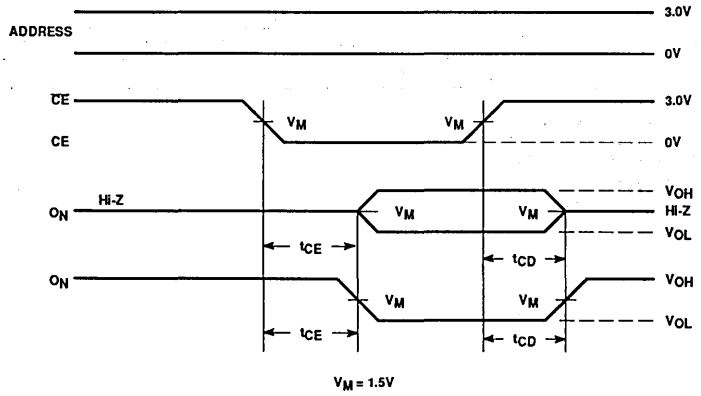


Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS





Signetics

82S191, 82S191A
16K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S191 and 82S191A are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S191 and 82S191A are supplied with all outputs at a logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time:
  - 82S191: 100ns max
  - 82S191A: 55ns max
- Input loading: -150μA max
- Three chip enable inputs
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- Outputs: 3-State

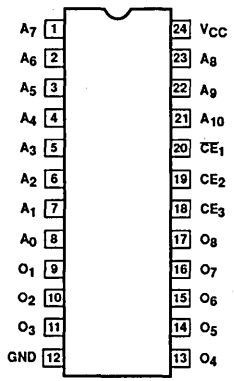
APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

ORDERING INFORMATION

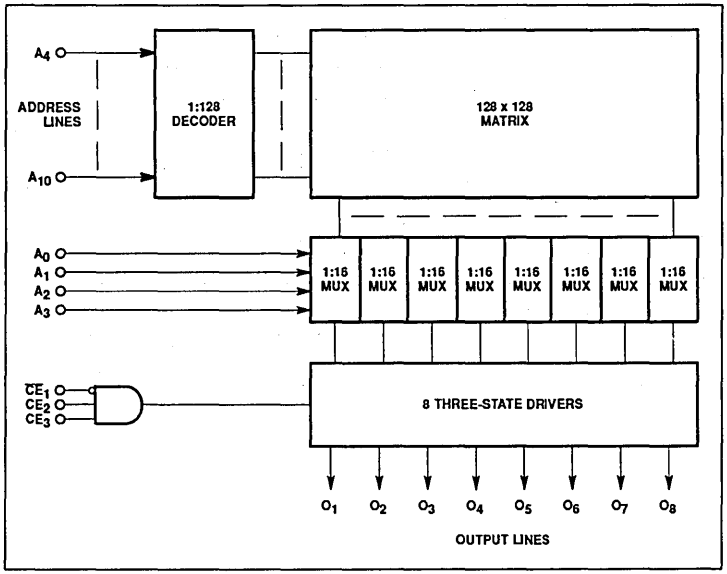
DESCRIPTION	ORDER CODE
24-pin Ceramic Dual-In-Line 600mil-wide	82S191/BJA, 82S191A/BJA
24-pin Ceramic Dual-In-Line 300mil-wide	82S191/BLA, 82S191A/BLA
24-pin Ceramic Flat Package	82S191/BKA, 82S191A/BKA
28-pin Ceramic LLCC	82S191/B3A, 82S191A/B3A

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard 21A

BLOCK DIAGRAM



16K-Bit TTL Bipolar PROM (2048 × 8) — 82S191, 82S191A

ABSOLUTE MAXIMUM RATINGS[8]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATINGS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}[7]	High level input voltage	2.0			V
V_{IL}[7]	Low level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High level output current			-2	mA
I_{OL}	Low level output current			9.6	mA
T_A	Operating free air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
V_{IK}	Input Clamp voltage	V_{CC} = Min, I_I = -18mA		-0.8	-1.2	V
V_{OL}	Low level Output voltage	V_{CC} = Min $\overline{CE}_1 = V_{IL}$, $CE_{2,3} = V_{IH}$, I_O = Max			0.5	V
V_{OH}	High level Output voltage	V_{CC} = Min, I_O = Max	2.4			V
I_{IL}[1]	Low level Input current	V_{CC} = Max, V_I = 0.45V			-150	µA
I_{IH}[1]	High level Input current	V_{CC} = Max, V_I = 5.5V			40	µA
I_{OLZ}[1]	OFF-State output current low level	V_{CC} = Max $\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_O = 0.4V			-40	µA
I_{OHZ}[1]	OFF-State output current High State	V_{CC} = Max $\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_O = 5.5V			40	µA
I_{OS}	Short circuit output current[3]	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, V_{CC} = Max, V_O = 0V	-15		-85	mA
I_{CC}	Supply current	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{CC} = Max		130	185	mA
C_{IN}[6]	Input Capacitance	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low V_{CC} = Nom, V_I = 2.0V		5	10	pF
C_{OUT}[6]	Output Capacitance	V_{CC} = Nom, $\overline{CE}_1$ = High, $CE_{2,3}$ = Low V_O = 2.0V		8	13	pF

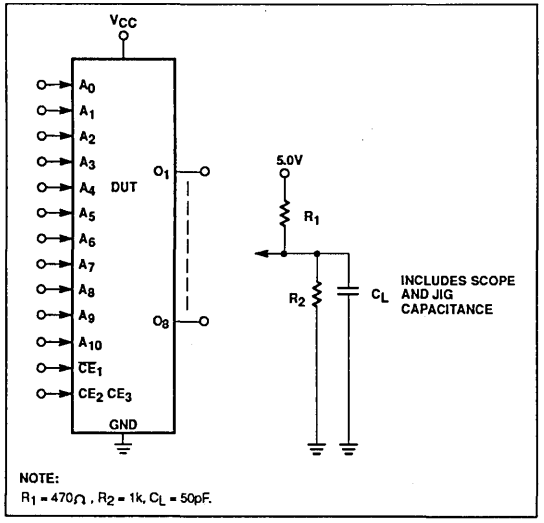
16K-Bit TTL Bipolar PROM (2048 × 8) — 82S191, 82S191A

AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	82S191			82S191A			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		50	100		50	55	ns
t_{CE}	Access time[4]	Output	Chip enable		30	50		20	30	ns
t_{CD}	Disable time	Output	Chip disable		30	50		20	30	ns

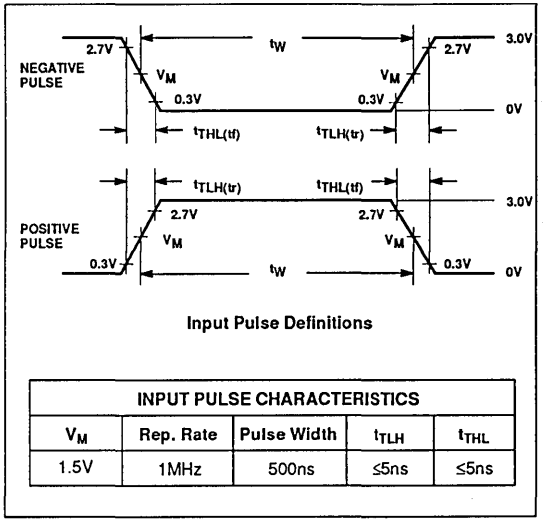
NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Guaranteed, but not tested.
7. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.
8. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TEST LOAD CIRCUITS



NOTE:
$R_1 = 470\Omega$, $R_2 = 1k$, $C_L = 50pF$.

VOLTAGE WAVEFORMS

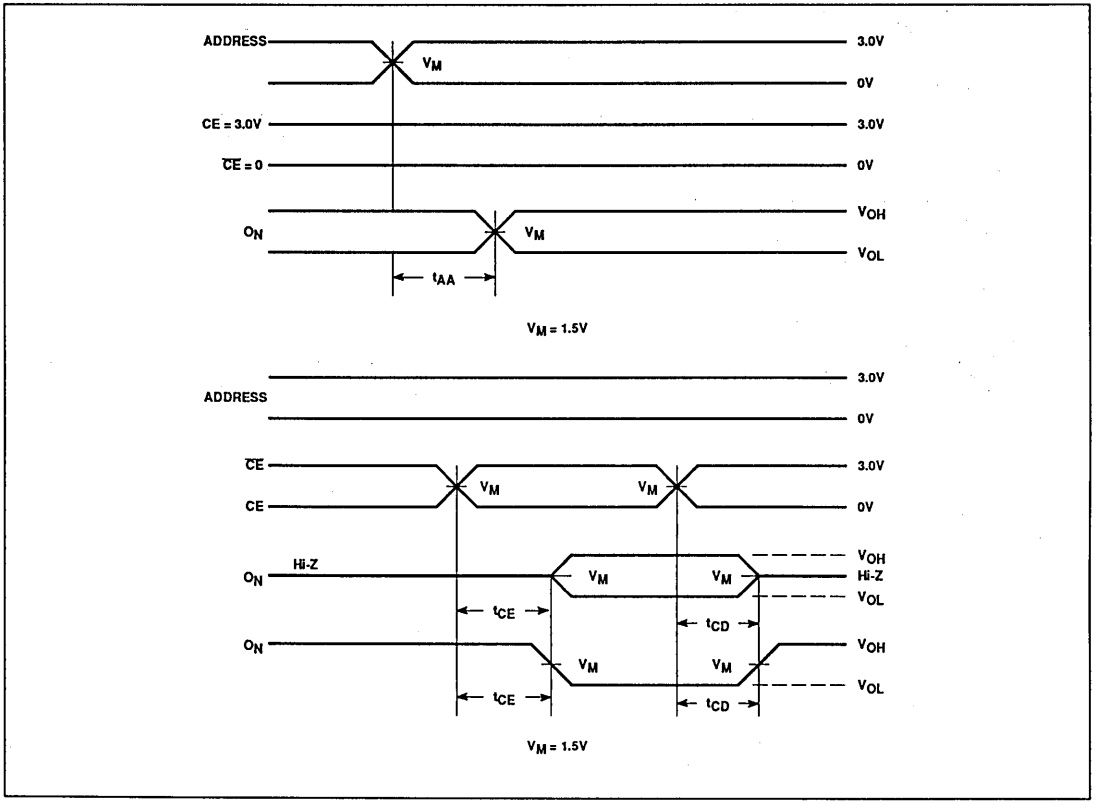


Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

16K-Bit TTL Bipolar PROM (2048 × 8) — 82S191, 82S191A

TIMING DIAGRAMS



Signetics

82HS195A

16K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82HS195A is field programmable, which means that custom patterns are immediately available by following the Generic II fusing procedure. The Signetics 82HS195A supplied with all outputs at logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and two chip enable inputs for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- **Address access time: 35ns max**
- **Input loading: -250μA max**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: 3-State**

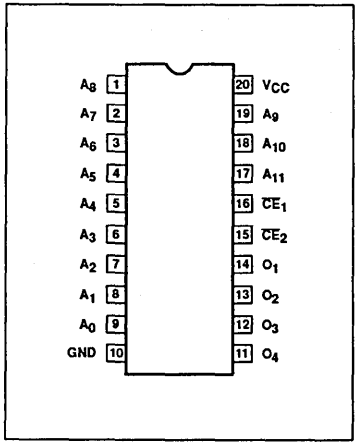
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-pin Ceramic Dual-In-Line 300mil-wide	82HS195A/BRA

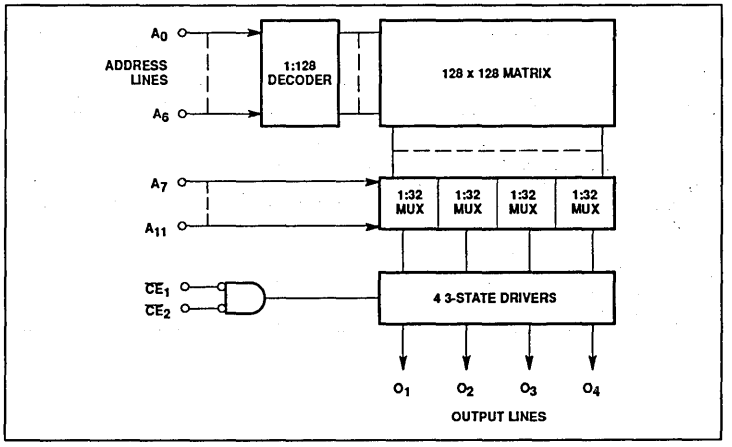
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



BLOCK DIAGRAM



16K-Bit TTL Bipolar PROM (4096 × 4) — 82HS195A

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage						
		V_{CC} = 4.5V, $\overline{CE}_1$ & $\overline{CE}_2$ = Low				
V_{OL}	Low	I_{OL} = 16mA			0.5	V
V_{OH}	High	I_{OH} = -2mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-250	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z state	$\overline{CE}_1$ & $\overline{CE}_2$ = High, V_O = 0.4V			-40	µA
		$\overline{CE}_1$ & $\overline{CE}_2$ = High, V_O = 5.5V			40	µA
I_{OS}	Short circuit[4]	V_{CC} = 5.5V, $\overline{CE}_1$ & $\overline{CE}_2$ = Low, V_O = 0V, High stored	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}_1$ + $\overline{CE}_2$ = High, V_{CC} = 5.5V		120	155	mA
Capacitance[7]						
		$\overline{CE}_1$ & $\overline{CE}_2$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

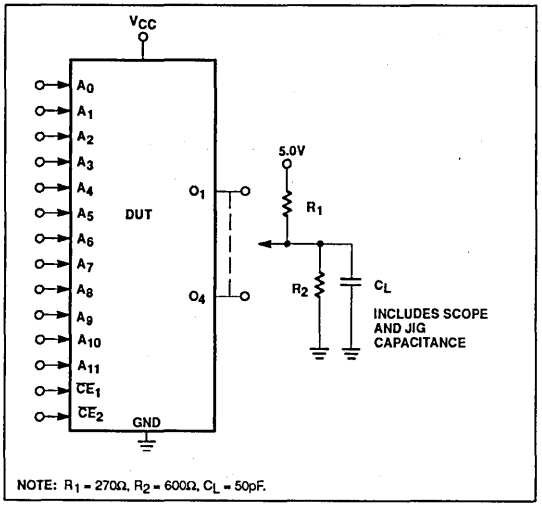
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[6]	Output	Address		35	35	ns
t_{CE}		Output	Chip enable		20	25	ns
t_{CD}	Disable time[6]	Output	Chip disable		20	25	ns

NOTES:
1. All voltages are with respect to network ground terminal.
2. Positive current is defined as into the terminal referenced.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Output shorted for no more than one second. No more than one output shorted at a time.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Tested at an address cycle time of 1µs.
7. Guaranteed, but not tested.
8. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

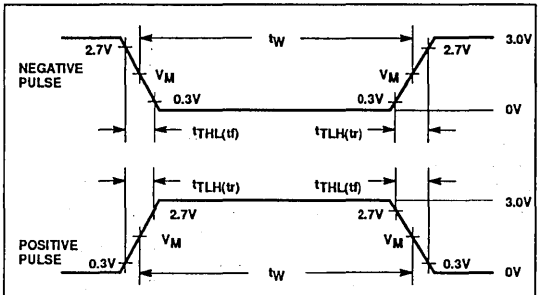
16K-Bit TTL Bipolar PROM (4096 × 4) — 82HS195A

TEST LOAD CIRCUITS



NOTE: R_1 = 270Ω, R_2 = 600Ω, C_L = 50pF.

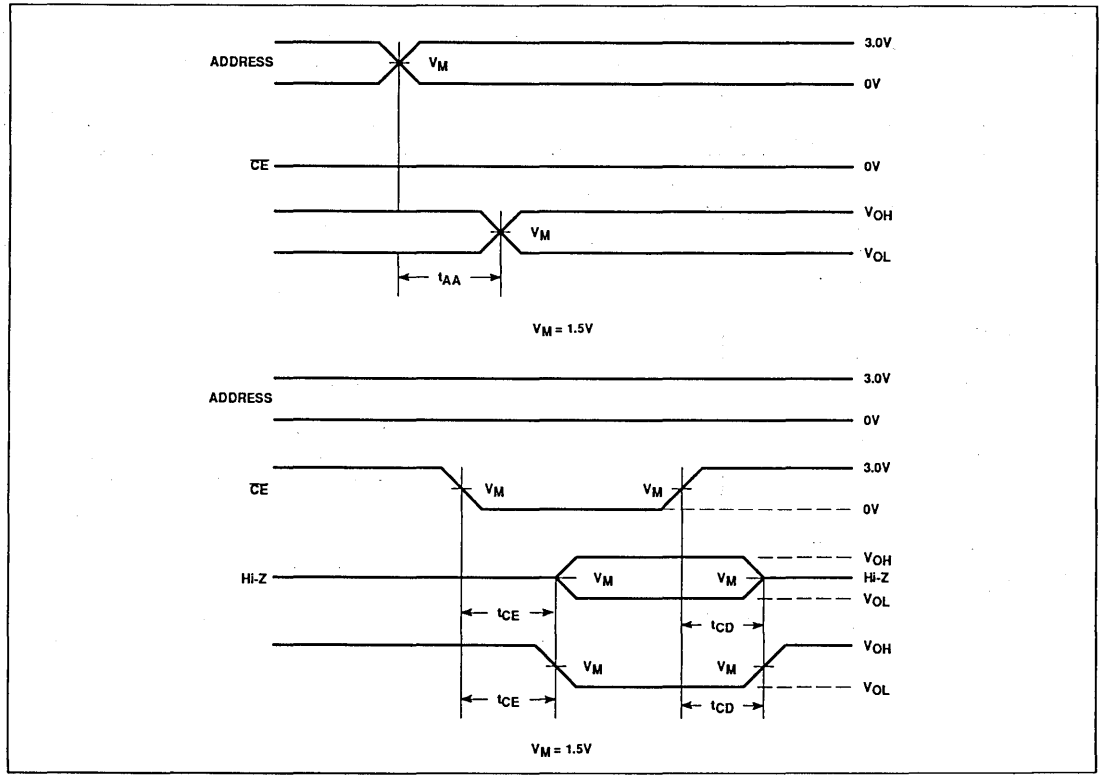
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAM



Signetics

82S291A
16K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82S291A is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82S291A is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing the vertical junction matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- Address access time: 35ns max
- Input loading: -250μA max
- Three chip enable inputs
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are High level
- Fully TTL compatible
- Outputs: 3-State

APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion
- Prototyping/volume production

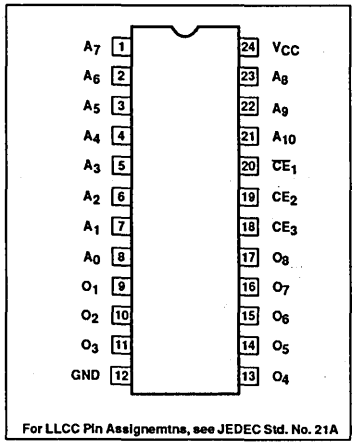
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Ceramic Dual-In-Line 300mil-wide	82S291A/BLA

ABSOLUTE MAXIMUM RATINGS

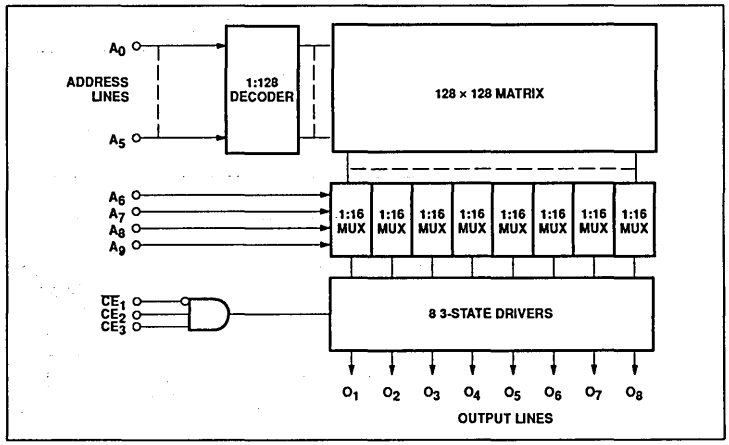
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC Pin Assignemtns, see JEDEC Std. No. 21A

BLOCK DIAGRAM



16K-Bit TTL Bipolar PROM (2048 × 8) — 82S291A

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}[7]	High-level input voltage	2.0			V
V_{IL}[7]	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2	mA
I_{OL}	Low-level output current			16	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = Max		-0.8	-1.2	V
V_{OL}	Output Low-level current	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, V_{CC} = Min, I_{OL} = Max			0.5	V
V_{OH}	Output High-level current	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, V_{CC} = Min, I_{OH} = Max	2.4			V
I_{IL}	Input Low-level current	V_{CC} = Max, V_I = 0.45V			-250	µA
I_{IH}	Input High-level current	V_{CC} = Max, V_I = 5.5V			40	µA
I_{OLZ}	Off-State output current Low-State	V_{CC} = Max, $\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_O = 0.4			-40	µA
I_{OHZ}	Off-State output current High-State	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_O = 5.5, V_{CC} = Max			40	µA
I_{OS}	Output short circuit current[3]	$\overline{CE}_1$ = Low, $CE_{2,3}$ = High, V_{CC} = Max, V_O = 0V	-15		-85	mA
I_{CC}	Supply current[8]	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{CC} = 5.5V		130	185	mA
C_{IN} C_{OUT}	Input capacitance[6] Output capacitance[6]	$\overline{CE}_1$ = High, $CE_{2,3}$ = Low, V_{CC} = 5.0V V_I = 2.0V V_O = 2.0V		5 8	10 13	pF pF

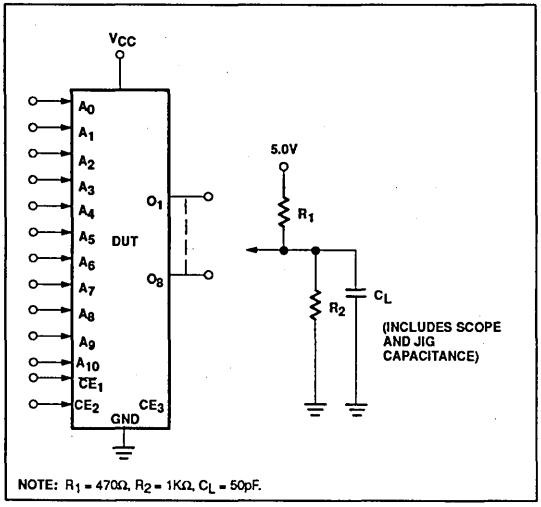
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
t_{AA}	Access time[4]	Output	Address		15	35	ns
t_{CE}	Access time[4]	Output	Chip Enable		10	20	ns
t_{CD}	Disable time	Output	Chip Disable		10	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1µs.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Guaranteed, but not tested.
7. Measured with one output switching from a logic "1" to a logic "0". These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.
8. Measured with all inputs grounded and all outputs open.

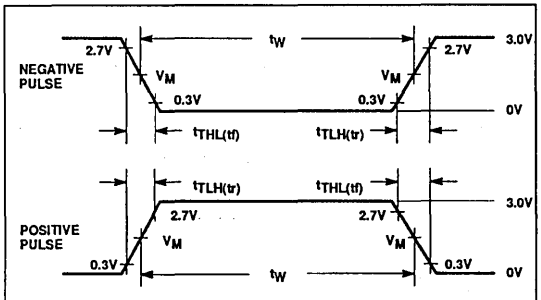
16K-Bit TTL Bipolar PROM (2048 × 8) — 82S291A

TEST LOAD CIRCUITS



NOTE: $R_1 = 470\Omega$, $R_2 = 1K\Omega$, $C_L = 50pF$.

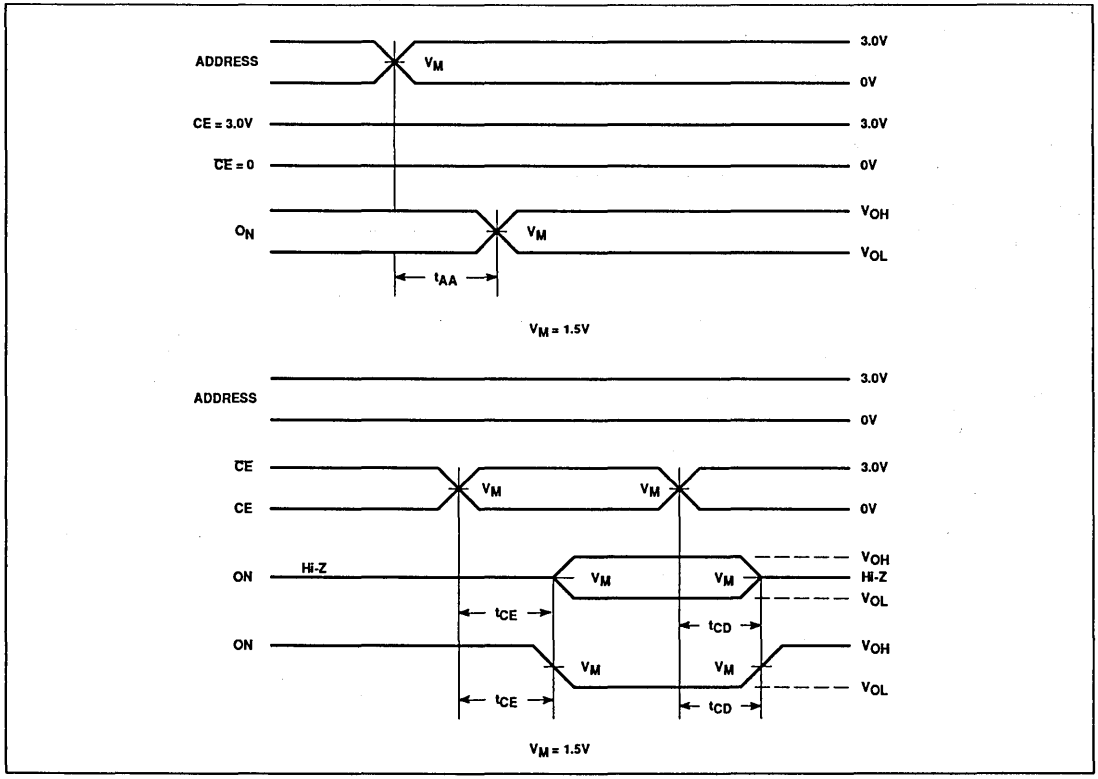
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



Signetics

82HS321A/82HS321B

32K-Bit TTL Bipolar PROM (4096 × 8)

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82HS321 is field programmable, which means that custom patterns are immediately available by following the Signetics Generic II fusing procedure. The 82HS321 is supplied with all outputs at a logical High. Outputs are programmed to a logic Low level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

FEATURES

- **Address access time:**
  - **82HS321A: 45ns max**
  - **82HS321B: 35ns max**
- **Input loading: -250μA max**
- **Two chip enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: 3-State**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

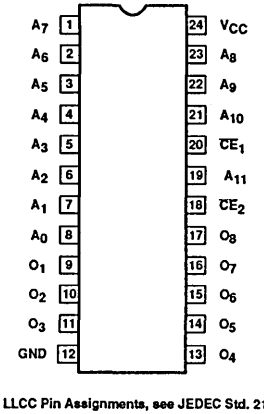
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Ceramic Dual-In-Line 600mil-wide	82HS321A/BJA 82HS321B/BJA
24-pin Ceramic Dual-In-Line 300mil-wide	82HS321B/BLA
24-pin Ceramic FlatPack	82HS321A/BKA 82HS321B/BKA
24-Pin Ceramic CLCC	82HS321A/B3A 82HS321B/B3A

ABSOLUTE MAXIMUM RATINGS

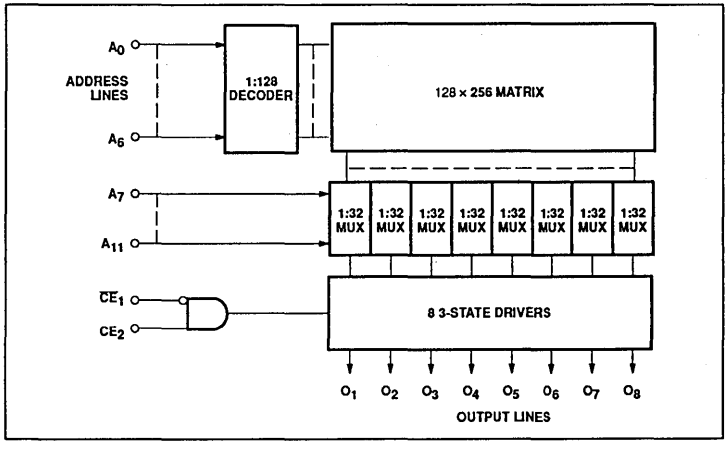
SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V
V_I	Input voltage	+5.5	V
V_O	Output voltage Off-State	+5.5	V
T_{STG}	Storage temperature range	-65 to +150	°C

PIN CONFIGURATION



For LLCC Pin Assignments, see JEDEC Std. 21

BLOCK DIAGRAM



32K-Bit TTL Bipolar PROM (4096 × 8) — 82HS321A/82HS321B

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATINGS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}[3]	High level input voltage	2.0			V
V_{IL}[3]	Low level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High level output current			-2	mA
I_{OL}	Low level output current			16	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
V_{IK}	Input Clamp voltage	V_{CC} = Min, $I_I = I_{IK}$		-0.8	-1.2	V
V_{OL}	Output Low level current	V_{CC} = Min, I_{OL} = Max, $\overline{CE}_1$ = Low, CE_2 = High			0.5	V
V_{OH}	Output High level current	V_{CC} = Min, $\overline{CE}_1$ = Low, CE_2 = High, I_{OH} = Max	2.4			V
I_{IL}	Input Low level current	V_{CC} = Max, V_I = 0.4V			-250	µA
I_{IH}	Input High level current	V_{CC} = Max, V_I = 5.5V			40	µA
I_{OLZ}	Off-State output current Low	V_{CC} = Max, $\overline{CE}_1$ = High, CE_2 = Low, V_O = 0.4V			-40	µA
I_{OHZ}	Off-State output current High	V_{CC} = Max, $\overline{CE}_1$ = High, CE_2 = Low, V_O = 5.5V			40	µA
I_{OS}	Short circuit[4]	V_{CC} = Max, $\overline{CE}_1$ = Low, CE_2 = High, V_O = 0V with stored "1"	-20		-85	mA
I_{CC}	Supply current	V_{CC} = Max, $\overline{CE}_1$ = High, CE_2 = Low		130	185	mA
C_{IN}	Input Capacitance[7]	$\overline{CE}_1$ = High, CE_2 = Low, V_{CC} = Nom, V_I = 2.0V		5	10	pF
C_{OUT}	Output Capacitance[7]	$\overline{CE}_1$ = High, CE_2 = Low, V_{CC} = Nom, V_O = 2.0V		8	13	pF

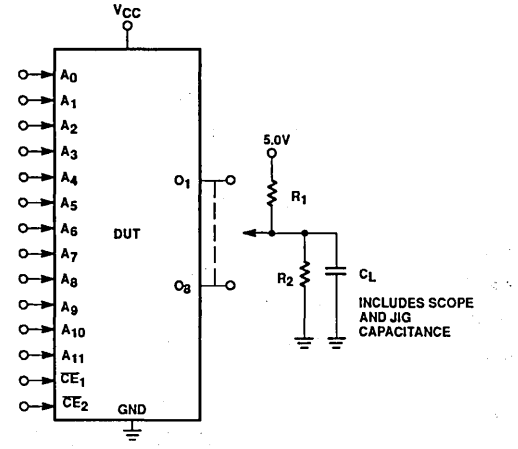
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	82HS321A			82HS321B			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
t_{AA}	Access time[6]	Output	Address		40	45		28	35	ns
t_{CE}	Access time[6]	Output	Chip enable		25	30		15	20	ns
t_{CD}	Disable time	Output	Chip disable		25	30		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching form Logic "1" to a Logic "0". These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.
4. Duration of short circuit should not exceed 1 second.
5. Typical values are at V_{CC} = 5V, T_A = +25°C.
6. Tested at an address cycle time of 1µs.
7. Guaranteed, but not tested.

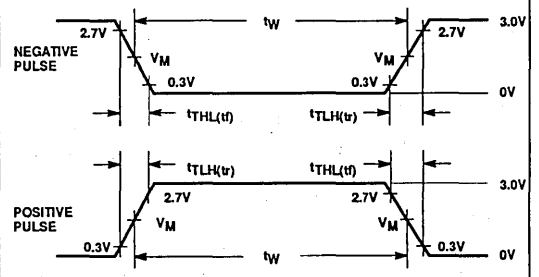
32K-Bit TTL Bipolar PROM (4096 × 8) — 82HS321A/82HS321B

TEST LOAD CIRCUITS



NOTE: $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 50pF$.

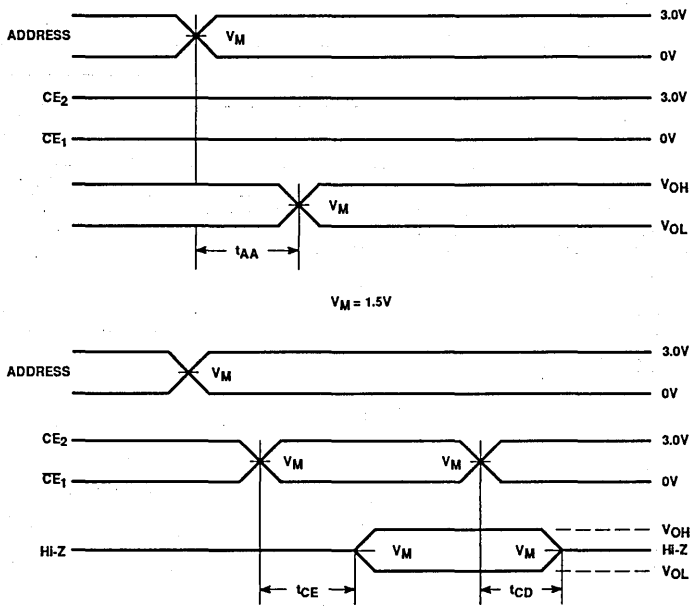
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAM



Signetics

82HS641A
82HS641B
64K-Bit TTL Bipolar PROM

Military Bipolar Memory Products

Product Specification

DESCRIPTION

The 82HS641 is field programmable which means that custom patterns are immediately available by following the Signetics Generic II fusing Procedure. The 82HS641 is supplied with all outputs at a logical High. Outputs are programmed to a logic low level at any specified address by fusing the vertical junction matrix.

This device includes on-chip address decoding with 1 chip enable input for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused applications.

FEATURES

- **Address access time:**
  82HS641A = 55ns max
  82HS641B = 45ns max
- **Input loading: -100μA max**
- **One chip enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are High level**
- **Fully TTL compatible**
- **Outputs: 3-State**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

ORDERING INFORMATION

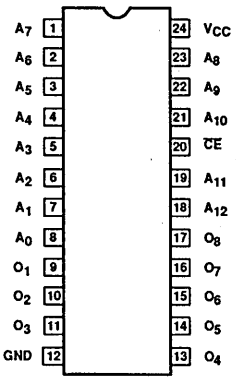
DESCRIPTION	ORDER CODE
24-pin Ceramic Dual-In-Line 600mil-wide	82HS641A/BJA 82HS641B/BJA
24-pin Ceramic LLCC	82HS641A/B3A 82HS641B/B3A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

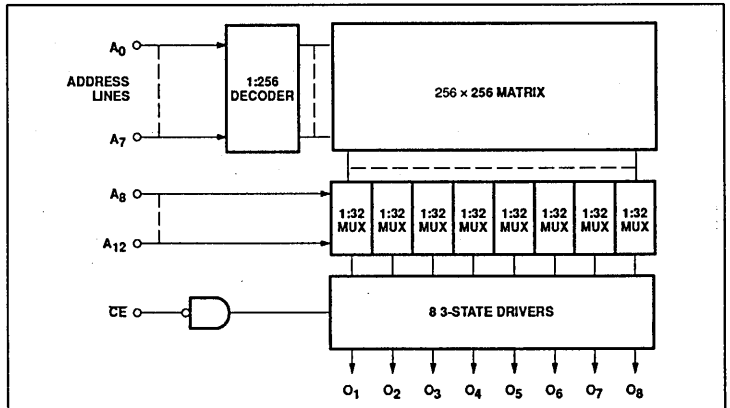
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



For LLCC Pin Assignments, see JEDEC Std. 21

BLOCK DIAGRAM



64K-Bit TTL Bipolar PROM (8192 × 8) — 82HS641A/82HS641B

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low[3]				0.8	V
V_{IH}	High[3]		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = 18mA		-0.8	-1.2	V
Output voltage						
		V_{CC} = 4.5V, $\overline{CE}$ = Low				
V_{OL}	Low	I_O = 16mA			0.5	V
V_{OH}	High	I_O = -2mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-100	µA
I_{IH}	High	V_I = 5.5V			40	µA
Output current						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z State	$\overline{CE}$ = High, V_O = 0.5V			-40	µA
		$\overline{CE}$ = High, V_O = 5.5V			+40	µA
I_{OS}	Short circuit[4]	$\overline{CE}$ = Low, V_O = 0V	-15		-85	mA
Supply current						
I_{CC}		$\overline{CE}$ = High, V_{CC} = 5.5V		130	185	mA
Capacitance[7]						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

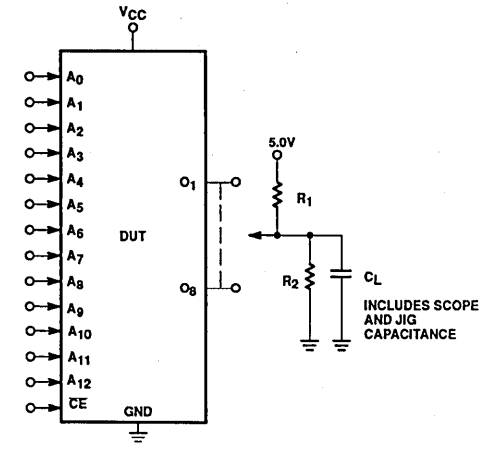
AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TO	FROM	82HS641A			82HS641B			UNIT
				Min	Typ[5]	Max	Min	Typ[5]	Max	
t_{AA}	Access time[6]	Output	Address		40	55		40	45	ns
t_{CE}	Access time[6]	Output	Chip enable		25	35		25	25	ns
t_{CD}	Disable time	Output	Chip disable		25	35		25	25	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Measured with one output switching from a Logic "1" to a Logic "0".
4. Duration of short circuit should not exceed 1 second, no more than one output shorted at a time.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.
6. Tested at an address cycle time of 1µs.
7. Guaranteed, but not tested.

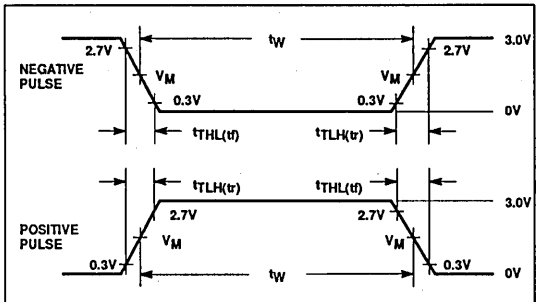
64K-Bit TTL Bipolar PROM (8192 × 8) — 82HS641A/82HS641B

TEST LOAD CIRCUITS



NOTE: $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 50pF$.

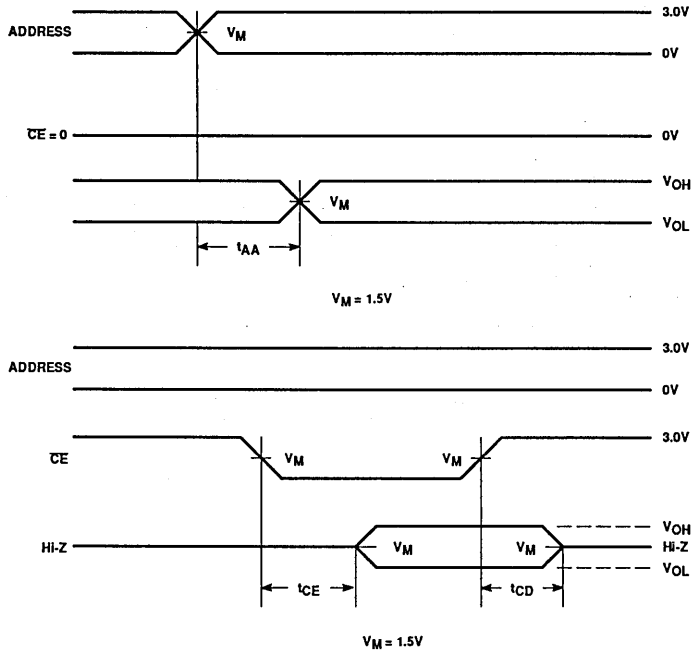
VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



Signetics

Section 7
PLD Data Sheets

Military Products

INDEX

Signetics

82S100/82S101

Field Programmable Logic Array (16 × 48 × 8)

Military
Customer Specific Products

Product Specification

DESCRIPTION

The 82S100 (3-State) and 82S101 (Open-Collector) are bipolar, Fuse Programmable Logic Arrays (FPLAs). Each device utilizes the standard AND/OR invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs ANDed together comprise one P-term. All 48 P-terms are selectively ORed to each output. The user must then only select which P-term will activate an output by disconnecting terms which do not affect the output. In addition, each output can be fused as active-HIGH (H) or active-LOW (L).

The 82S100 and 82S101 are fully TTL compatible, and include chip enable control for expansion of input variables and output inhibit. They feature either Open-Collector or 3-State outputs for ease of expansion of product terms and application in bus-organized systems.

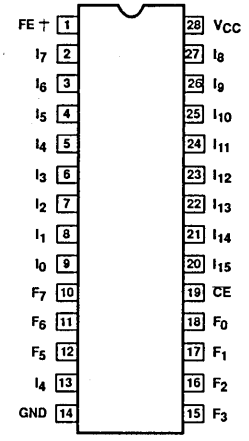
FEATURES

- Field-programmable (Ni-Cr link)
- Input variables: 16
- Output functions: 8
- Product terms: 48
- I/O propagation delay: 80ns max
- Power dissipation: 600mW typ
- Input loading: -150μA max
- Chip enable input
- Output option:
  - 82S100: 3-State
  - 82S101: Open-Collector
- Output disable function;
  - 3-State: HI-Z
  - Open-Collector: HI
- Separate I/O architecture

APPLICATION

- CRT display systems
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Data security encoders
- Fault detectors
- Frequency synthesizers
- 16-bit to 8-bit bus interface
- Random logic replacement

PIN CONFIGURATION



NOTE:
† = Open or grounded during normal operation

For LLCC Pin Assignments, see JEDEC Std. No. 21

LOGIC FUNCTION

TYPICAL PRODUCT TERM:
$Pn = A \bullet \overline{B} \bullet C \bullet D$

TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
$Z = P0 + P1 + P2 \ldots$

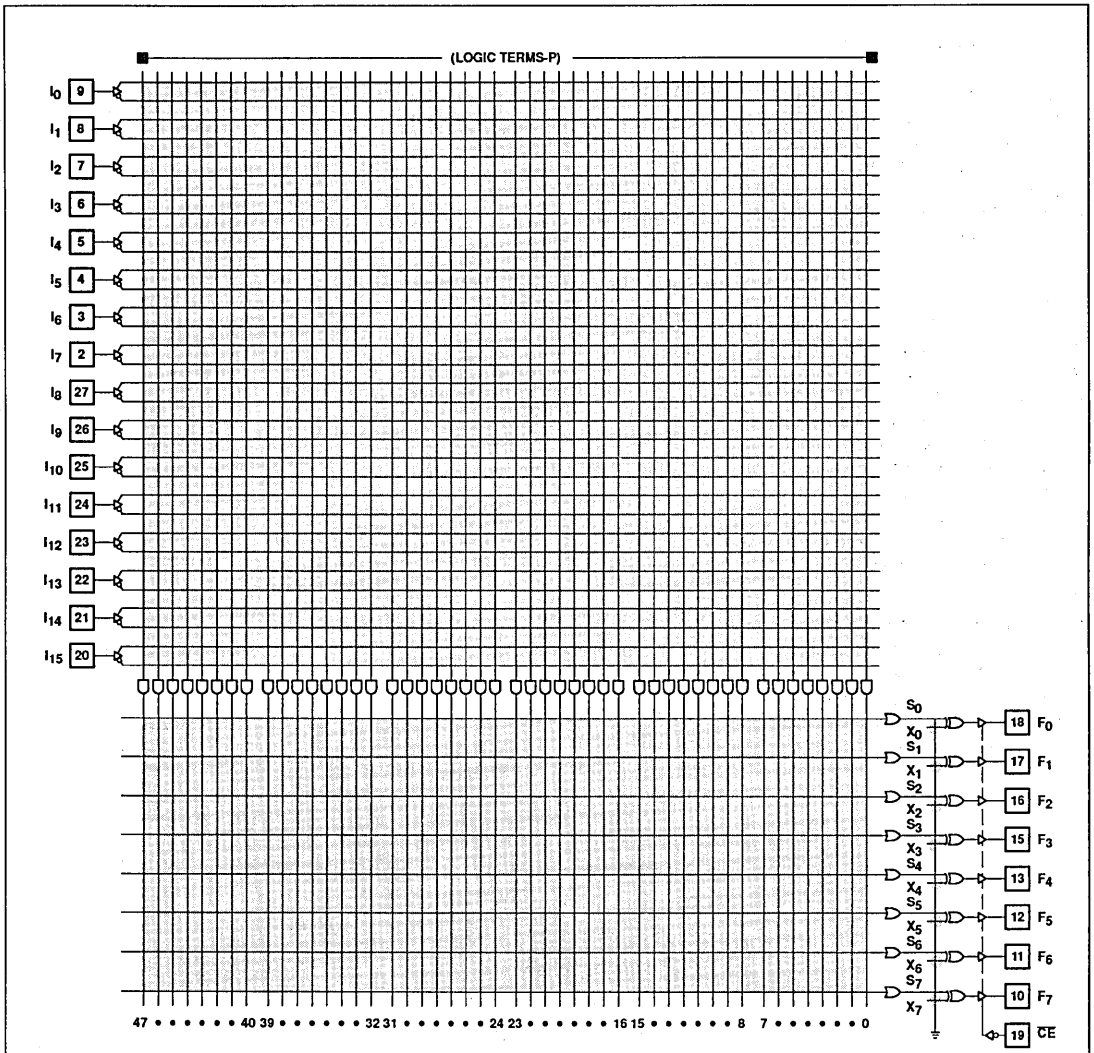
AT OUTPUT POLARITY = L
$\overline{Z} = P0 + P1 + P2 + \ldots$
$Z = \overline{P0} \bullet \overline{P1} \bullet \overline{P2} \bullet \ldots$

NOTES:
1. For each of the 8 outputs, either function Z (active-High) or $\overline{Z}$ (active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C etc. are user defined connections to fixed inputs (I) and output pins (O).

ORDERING INFORMATION

DESCRIPTION	3-STATE	OPEN-COLLECTOR
28-pin Ceramic DIP 600mil-wide	82S100/BXA	82S101/BXA
28-pin Ceramic Flat Pack	82S100/BYA	82S101/BYA
28-pin Ceramic LLCC	82S100/B3A	82S101/B3A

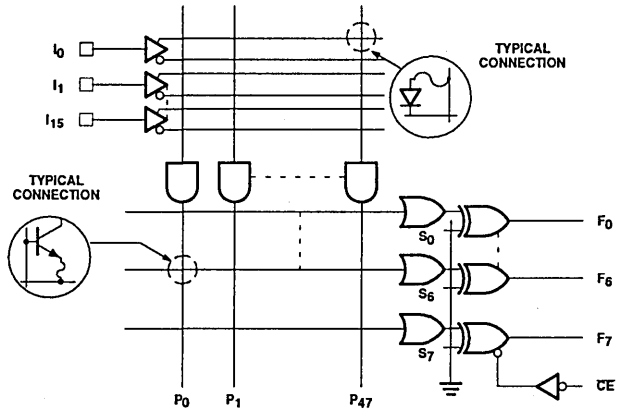
FPLA LOGIC DIAGRAM



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ◎ Programmable connection.

Field Programmable Logic Array (16 × 48 × 8) — 82S100/101

FUNCTIONAL DIAGRAM



Fusible NI-Cr link are initially intack at all array cross-points.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	V_{DC}
V_I	Input voltage	+10.0	V_{DC}
V_O	Output voltage	+5.5	V_{DC}
I_I	Input currents	-30 to +30	mA
I_O	Output currents	+100	mA
T_A	Operating Temperature range	-55 to +125	°C
T_{STG}	Storage Temperature range	-65 to +150	°C

Field Programmable Logic Array (16 × 48 × 8) — 82S100/101

DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS[3]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input Voltage						
V_{IH}	High	V_{CC} = 5.5V	2.0			V
V_{IL}	Low	V_{CC} = 4.5V			0.8	V
V_{IK}	Clamp[4]	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output Voltage						
		V_{CC} = 4.5V				V
V_{OH}	High (82S100)[5, 10]	I_{OH} = -2mA	2.4			V
V_{OL}	Low[6]	I_{OL} = 9.6mA		0.35	0.5	V
Input Current						
		V_{CC} = 5.5V				
I_{IH}	High	V_I = 5.5V		<1	50	µA
I_{IL}	Low	V_I = 0.45V		-10	-150	µA
Output Current						
		$\overline{CE}$ = HIGH, V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z State	V_O = 5.5V		1	60	µA
	(82S100)	V_O = 0.45V		-1	-60	µA
I_{OS}	Short circuit (82S100)[4, 7, 10]	$\overline{CE}$ = LOW, V_O = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = 5.5V		120	180	mA
Capacitance[9]						
		$\overline{CE}$ = HIGH				
		V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		8	13	pF
C_{OUT}	Output	V_O = 2.0V		17	22	pF

AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Propagation Delay							
T_{PD}	Input[11]	Output	Input		35	80	ns
T_{CE}	Chip enable	Output	Chip enable		15	40	
Disable Time							
T_{CD}	Chip disable	Output	Chip enable		15	40	ns

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one pin at a time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to V_{CC}.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the chip enable input at a logic high, 1_1-1_{15} = GND.
9. Guaranteed, but not tested.
10. On unprogrammed device apply 10V - 1_1-I_{15}.
11. Not testable on unprogrammed device.

Field Programmable Logic Array (16 × 48 × 8) — 82S100/101

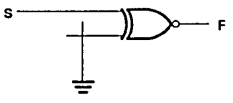
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

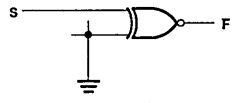
With Logic programming, the AND/OR/EX–OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table.

In this Table, the logic state or action of variables I, P and F, associated with each Sum Term S_n, is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY – (F)

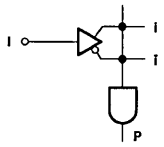


ACTIVE LEVEL	CODE
LOW	L

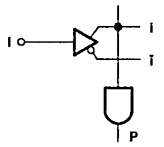


ACTIVE LEVEL	CODE
HIGH[12]	H

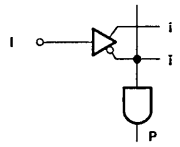
"AND" ARRAY – (I)



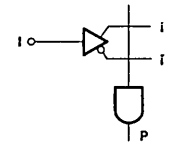
STATE	CODE
INACTIVE[12, 13]	O



STATE	CODE
I	H

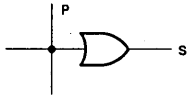


STATE	CODE
I	L

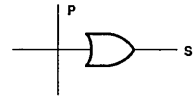


STATE	CODE
DON'T CARE	–

"OR" ARRAY – (F)



P_n STATUS	CODE
ACTIVE[12]	A



P_n STATUS	CODE
INACTIVE	•

NOTES:
12. This is the initial unprogrammed state of all links.
13. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

Field Programmable Logic Array (16 × 48 × 8) — 82S100/101

TIMING DEFINITIONS

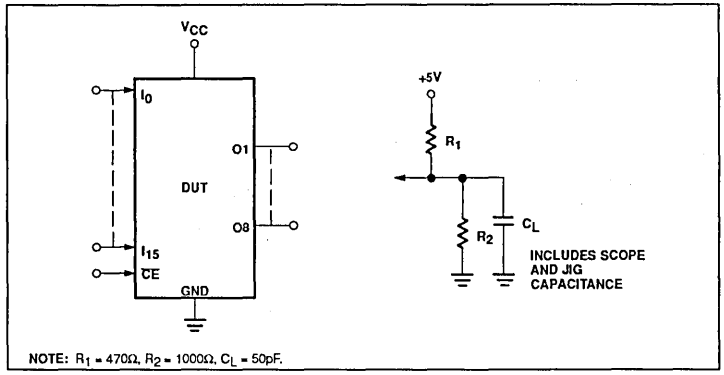
SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with input valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes High and Data Output is in Off-state (Hi-Z or High).
T_{PD}	Delay between beginning of valid input (with Chip Enable Low) and when Data Output becomes valid.

VIRGIN STATE

The 82S100/101 virgin devices are factory shipped in an unprogrammed state, characterized by:

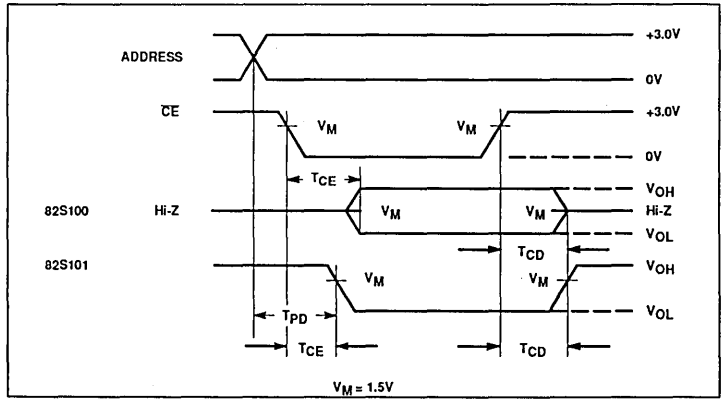
1. All internal Ni-Cr links are intact.
2. Each product term (P-term) contains both True and Complement values of every input variable I (P-terms always logically "false").
3. The "OR" Matrix contains all 48 P-terms.
4. The polarity of each output is set to active-High (Fp function).
5. All outputs are at a Low logic level.

TEST LOAD CIRCUITS

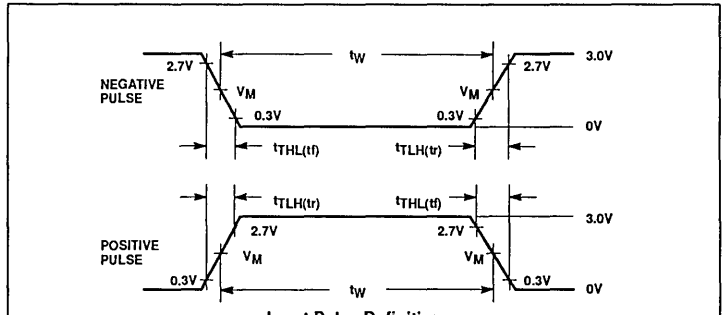


NOTE: R_1 = 470Ω, R_2 = 1000Ω, C_L = 50pF.

TIMING DIAGRAM



VOLTAGE WAVEFORM



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Signetics

82S105 (PLS105)
Field-Programmable Logic Sequencer (16 × 48 × 8)

Signetics Programmable Logic

Product Specification

Military
Application Specific Products

DESCRIPTION

The 82S105 is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6 Q_P, and 8 Q_F edge-triggered, clocked S/R flip-flops, with an asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 16 external inputs, $I_{0\text{-}15}$, with six internal inputs, $P_{0\text{-}5}$, fed back from the State Register to form up to 48 transition terms (AND terms).

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse. Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to $\overline{\text{Output Enable}}$ function, as an additional user-programmable option.

FEATURES

- **Field-programmable (Ni-Cr link)**
- **16 input variables**
- **8 output functions**
- **48 transition terms**
- **6-bit State Register**
- **8-bit Output Register**
- **Transition Complement Array**
- **Positive edge-trigger clock**
- **Programmable asynchronous preset or Output Enable**
- **Power-on preset to all "1" of internal registers**
- **f_{MAX} = 10.5MHz**
- **650mW power dissipation (typical)**
- **TTL compatible**
- **Single +5V supply**
- **3-state outputs**

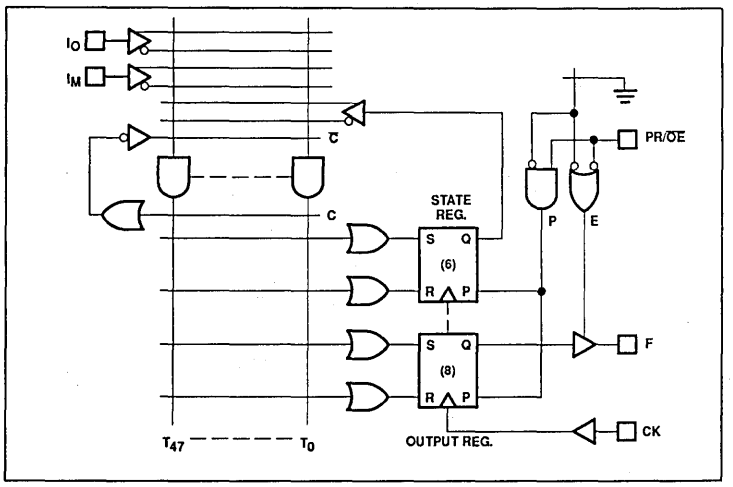
APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

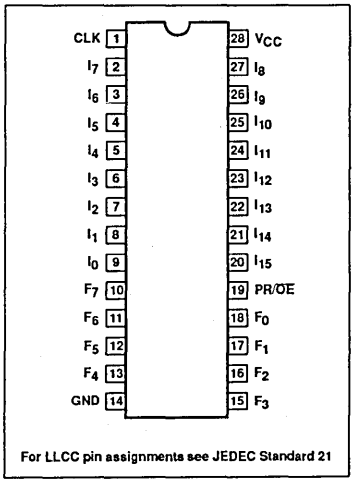
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-Pin Ceramic DIP 600mil-wide	82S105/BXA
28-Pin CLCC	82S105/B3A
28-Pin Ceramic FlatPack	82S105/BYA

FUNCTIONAL DIAGRAM



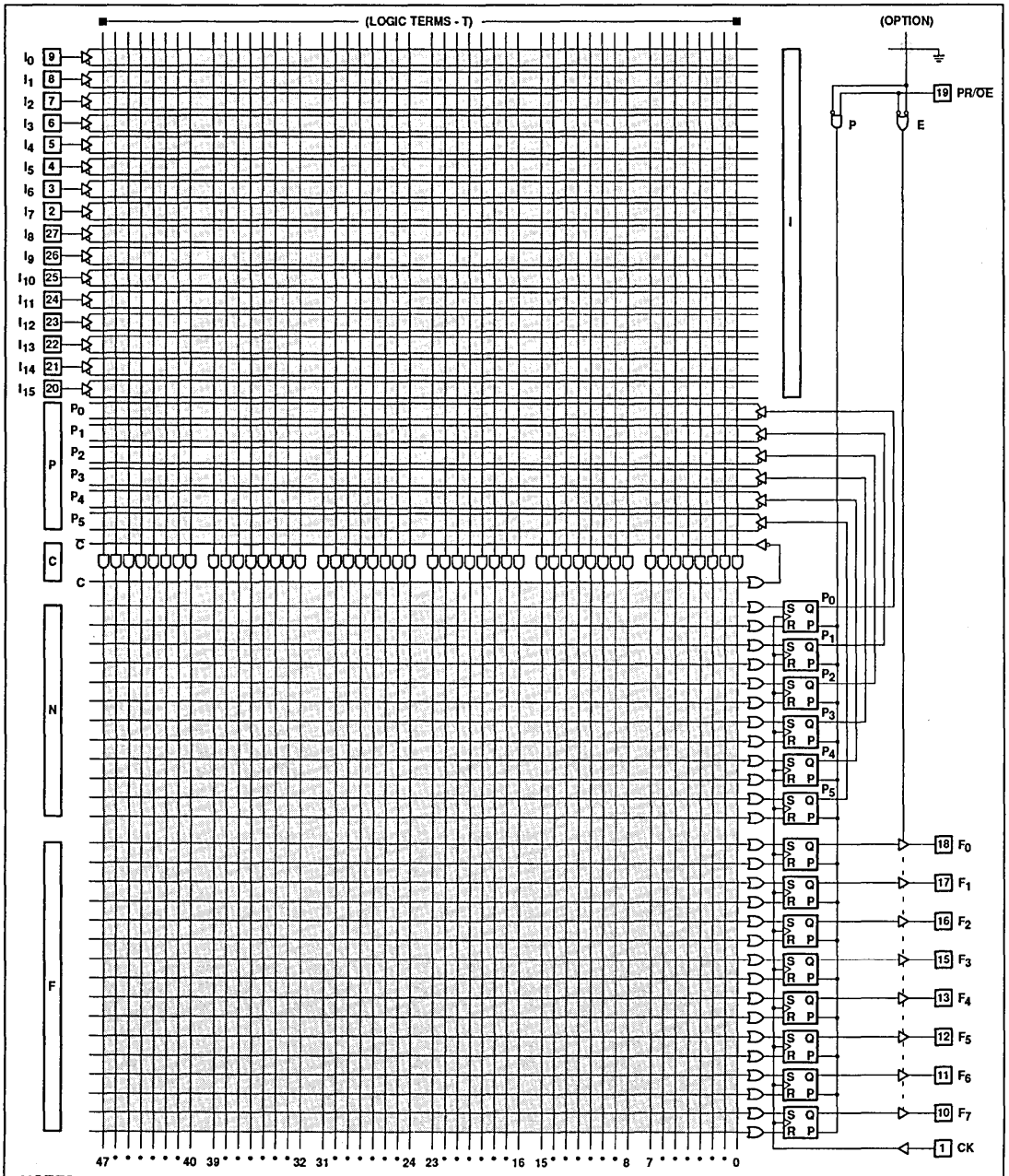
PIN CONFIGURATION



For LLCC pin assignments see JEDEC Standard 21

Field-Programmable Logic Sequencer (16 × 48 × 8) 82S105

FPLS LOGIC DIAGRAM



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ◎ Programmable connection.

Field-Programmable Logic Sequencer (16 × 48 × 8) 82S105

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2 - 8 20 - 27	I_{1-15}	**Logic Inputs:** The 15 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
9	I_0	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercised with standard TTL levels. When I_0 is held at +10V, device outputs F_{0-5} reflect the contents of State Register bits P_{0-5}. The contents of each Output Register remains unaltered.	Active-High/Low
10 - 13 15 - 18	F_{0-7}	**Logic/Diagnostic Outputs:** Eight device outputs which normally reflect the contents of Output Register bits Q_{0-7}, when enabled. When I_0 is held at +10V, $F_{0-5} = (P_{0-5})$, and $F_{6,7}$ = Logic "1".	Active-High
19	PR/$\overline{OE}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function: • **Preset:** Provides an asynchronous preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and F_{0-7} are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low. • **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers F_{0-7} from the Output Register.	Active-High (H) Active-Low (L)

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_I	Input voltage		+10.0	V_{DC}
V_O	Output voltage		+5.5	V_{DC}
I_{IK}	Input currents	-30	+30	mA
I_O	Output currents		+100	mA
T_A	Operating temperature range	-55	+125	°C
T_{STG}	Storage temperature range	-65	+150	°C

Field-Programmable Logic Sequencer (16 × 48 × 8) — 82S105

DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER[3]	TEST CONDITIONS[3]	LIMITS[3]			UNIT
			Min	Typ[2]	Max	
Input Voltage						
V_{IH}	High	V_{CC} = 5.5V	2			V
V_{IL}	Low	V_{CC} = 4.5V			0.8	V
V_{IK}	Clamp[4]	V_{CC} = Min, I_{IK} = -18mA		-0.8	-1.2	V
Output Voltage						
		V_{CC} = 4.5V				
V_{OH}	High[5]	I_{OH} = -2mA	2.4			V
V_{OL}	Low[6]	I_{OL} = 9.6mA		0.35	0.5	V
Input Current						
		V_{CC} = 5.5V				
I_{IH}	High	V_I = 5.5V		<1	50	µA
I_{IL}	Low	V_I = 0.45V		-10	-150	µA
I_{IL}	Low (CK input)	V_I = 0.45V		-50	-350	µA
Output Current						
		V_{CC} = 5.5V				
$I_{O(OFF)}$	Hi-Z state[7]	V_O = 5.5V		1	60	µA
		V_O = 0.45V		-1	-60	µA
I_{OS}	Short circuit[4,8]	V_O = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = 5.5V		120	185	mA
Capacitance[7,10]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		8	13	pF
C_{OUT}	Output	V_O = 2.0V		10	15	pF

Field-Programmable Logic Sequencer (16 × 48 × 8) — 82S105

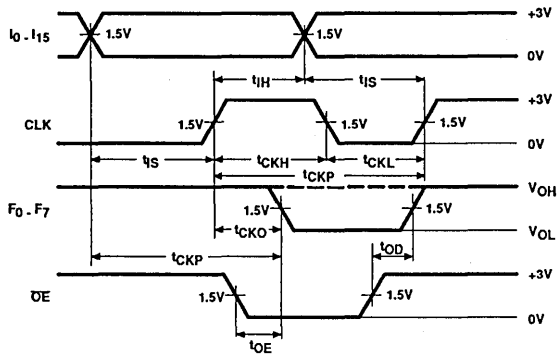
AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[11]	Max	
Pulse Width							
t_{CKH}	Clock[12] High	CK-	CK+	40	15		ns
t_{CKL}	Clock Low	CK+	CK-	40	15		ns
t_{CKP1}	Period (w/o C-array)	CK+	CK+	95	40		ns
t_{CKP2}	Period (w/C-array)[10]	CK+	CK+	135	60		ns
t_{PRH}	Preset pulse	PR+	PR-	40	15		ns
Setup Time							
t_{IS1}	Input	CK+	Input±	60			ns
t_{IS2}	Input (through Complement array)[13]	CK+	Input±	100			ns
t_{VS}	Power-on preset[13]	CK-	V_{CC}+	5	-10		ns
t_{PRS}	Preset[10]	CK-	PR-	5	-10		ns
Hold Time							
t_{IH}	Input[10]	Input±	CK+	10	-10		ns
Propagation Delay							
t_{CKO}	Clock	Output±	CK+		15	35	ns
t_{OE}	Output Enable[13]	Output-	OE-		20	40	ns
t_{OD}	Output Disable[13]	Output+	OE+		20	40	ns
t_{PR}	Preset	Output+	PR+		18	45	ns
t_{PPR}	Power-on preset[10]	Output+	V_{CC}+		0	20	ns
Frequency of Operation							
f_{MAX}	w/o C-array					10.5	MHz
f_{MAX}^C	w/C-array[10]					8.3	MHz

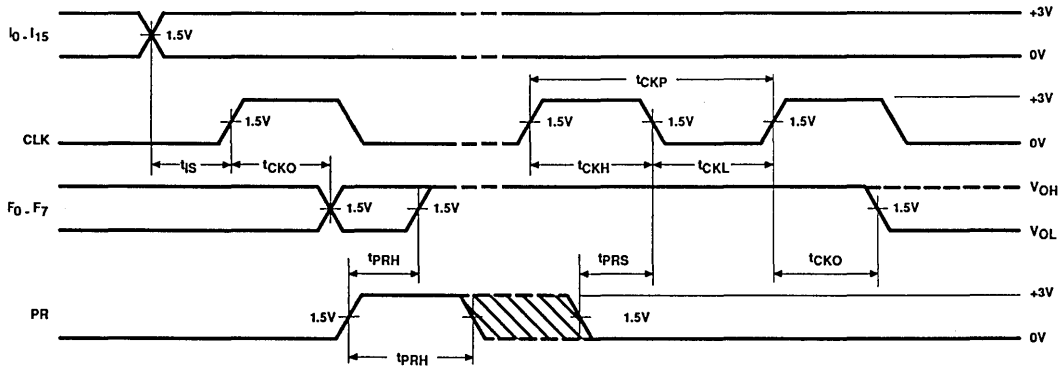
NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{OE}$ and a logic High stored, or with V_{IH} applied to PR.
6. Measured with a programmed logic condition for which the output is at a Low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to V_{CC}.
7. Measured with V_{IH} applied to PR/$\overline{OE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, the outputs open.
10. Guaranteed, but not tested.
11. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
12. To prevent spurious clocking, clock rise time (10% - 90%) $\leq$ 30ns.
13. Not testable on unprogrammed devices.

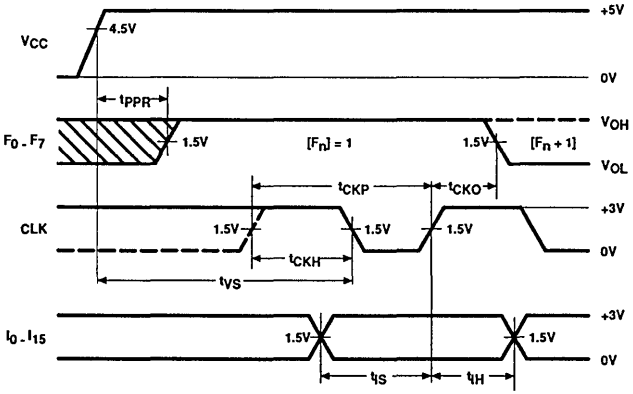
TIMING DIAGRAMS



Sequential Mode



Asynchronous Preset



Power-On Preset

Field-Programmable Logic Sequencer (16 × 48 × 8) 82S105

TIMING DEFINITIONS

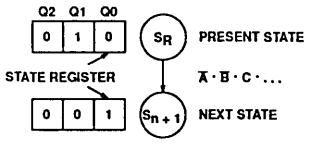
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP1}	Operating period — when not using Complement Array.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
t_{CKP2}	Operating period — when using Complement Array.
t_{IS2}	Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).

SYMBOL	PARAMETER
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of Asynchronous Preset and negative transition of Clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{CKO}	Delay between positive transition of Clock and when outputs become valid (with PR/$\overline{OE}$ Low).

SYMBOL	PARAMETER
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the Off-State.
t_{PR}	Delay between positive transition of Preset and when Outputs become valid at "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Maximum clock frequency.

LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.

   NOTE: The Test Array pattern must be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

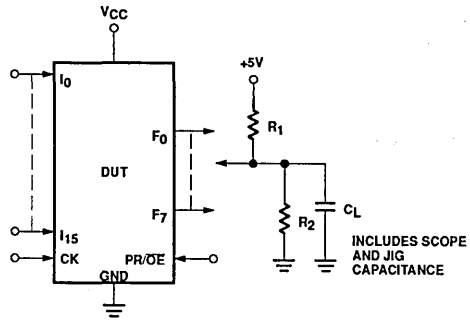
Field-Programmable Logic Sequencer (16 × 48 × 8) — 82S105

TRUTH TABLE

V_{CC}	OPTION							
	PR	$\overline{OE}$	I_0	CK	S	R	$Q_{P/F}$	F
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	*	X	X	X	Q_n	Hi-Z
		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

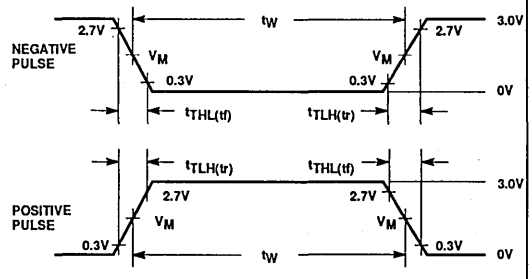
NOTES:
1. Positive Logic $S/\overline{R} = T_0 + T_1 + T_2 + ... + T_{47}$; $T_n = C(I_0\ I_1\ I_2\ ...)\ (P_0\ P_1\ ...\ P_8)$
2. Either Preset (Active-High) or $\overline{\text{Output Enable}}$ (active-Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. * = H/L/+10V.
6. X = Don't Care (≤ 5.5V).

TEST LOAD CIRCUITS



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF.

VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Field-Programmable Logic Sequencer (16 × 48 × 8) — 82S105

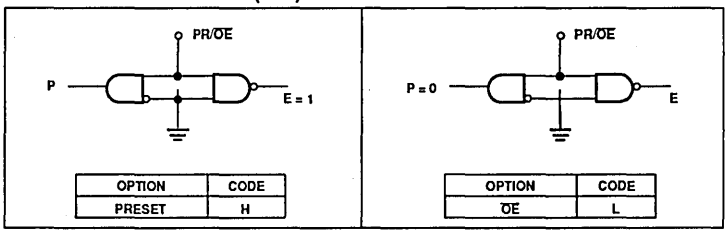
LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR gate input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Table on the following page.

In this table, the logic state or action of control variables C, I, P, N and F, associated with each Transition Term T_n is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

PRESET/OE OPTION - (P/E)

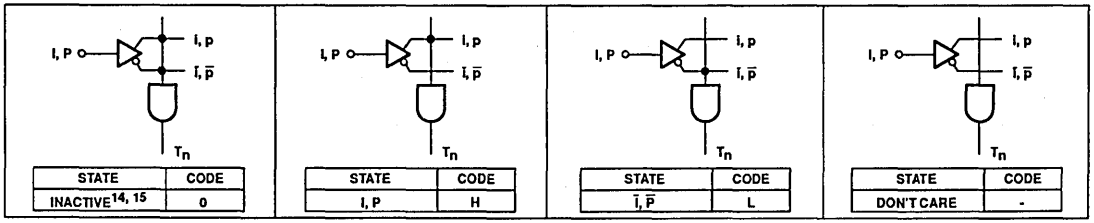


OPTION	CODE
PRESET	H

OPTION	CODE
$\overline{OE}$	L

PROGRAMMING THE 82S105:
The 82S105 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

"AND" ARRAY - (I), (P)



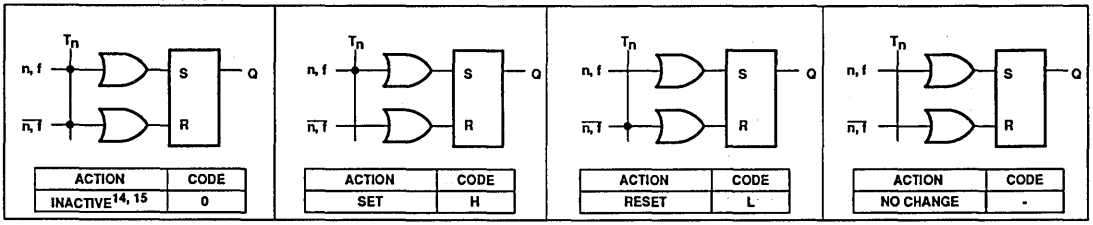
STATE	CODE
INACTIVE[14, 15]	0

STATE	CODE
I, P	H

STATE	CODE
$\overline{I}$, $\overline{P}$	L

STATE	CODE
DON'T CARE	-

"OR" ARRAY - (N), (F)



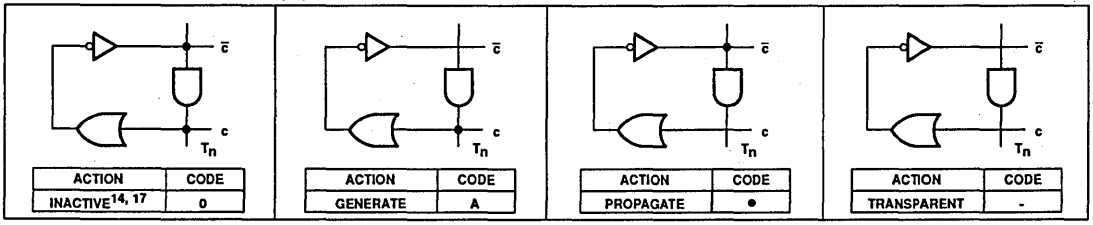
ACTION	CODE
INACTIVE[14, 15]	0

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	-

"COMPLEMENT" ARRAY - (C)



ACTION	CODE
INACTIVE[14, 17]	0

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	-

NOTES:
14. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates T_n.
15. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs are left intact.
16. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
17. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

Field-Programmable Logic Sequencer (16 × 48 × 8) — 82S105

FPLS PROGRAM TABLE

CUSTOMER NAME _____
PURCHASE ORDER # _____
SIGNETICS DEVICE # CF (XXXX)
CUSTOMER SYMBOLIZED PART # _____
TOTAL NUMBER OF PARTS _____
PROGRAM TABLE _____
REV _____
DATE _____

PROGRAM TABLE ENTRIES

AND			OR		
INACTIVE	0	C_n	INACTIVE	0	Ns, Fr
GENERATE	A		SET	H	
PROPAGATE	•		RESET	L	
TRANSPARENT	—		NO CHANGE	—	
INACTIVE	0	I_m, P_s	OPTION		
I, P	H		PRESET	H	P/E
$\overline{I}$, $\overline{P}$	L		$\overline{OE}$	L	
DON'T CARE	—				

TERM	C_n	AND: INPUT (I_m) 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	AND: PRESENT STATE (P_s) 5	4	3	2	1	0	REMARKS	OPTION (P/E) OR: NEXT STATE (Ns) 5	4	3	2	1	0	OUTPUT (Fr) 7	6	5	4	3	2	1	0
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PIN NO.		20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9													10	11	12	13	15	16	17	18
VARIABLE NAME																																					

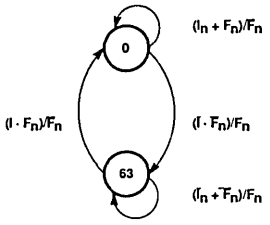
Field-Programmable Logic Sequencer (16 × 48 × 8) — 82S105

TEST ARRAY

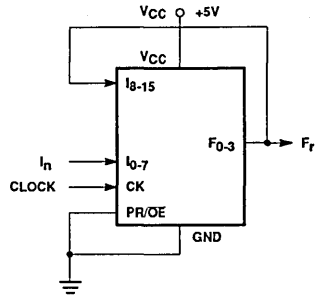
The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to I_{0-7} as shown in the test circuit timing diagram.



State Diagram



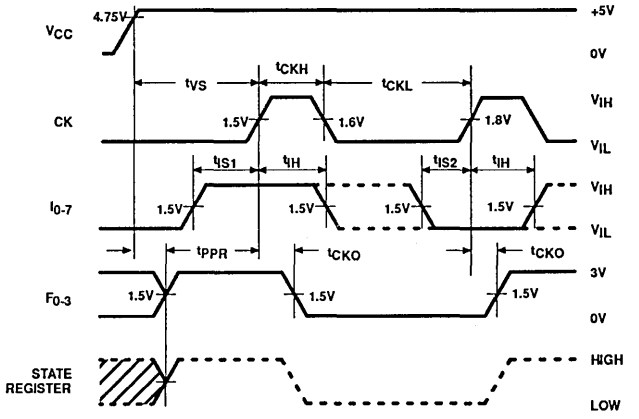
FPLS Under Test

TEST ARRAY PROGRAM

TERM	C	AND: INPUT (Im) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	AND: PRESENT STATE (Ps) 5 4 3 2 1 0	OPTION (P/E)	OR: NEXT STATE (Ns) 5 4 3 2 1 0	OR: OUTPUT (Fr) 7 6 5 4 3 2 1 0
				H		
48	A	H H H H H H H H H H H H H H H H	H H H H H H		L L L L L L	L L L L L L L L
49	•	L L L L L L L L L L L L L L L L	L L L L L L		H H H H H H	H H H H H H H H

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any Signetic's qualified programming equipment.



Test Circuit Timing Diagram

TEST ARRAY DELETED

TERM	C	AND: INPUT (Im) 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	AND: PRESENT STATE (Ps) 5 4 3 2 1 0	OPTION (P/E)	OR: NEXT STATE (Ns) 5 4 3 2 1 0	OR: OUTPUT (Fr) 7 6 5 4 3 2 1 0
				H		
48	–	H H H H H H H H H H H H H H H H	H H H H H H		– – – – – –	– – – – – – – –
49	•	L L L L L L L L L L L L L L L L	L L L L L L		– – – – – –	– – – – – – – –

Test Array Deleted

Signetics

82S153A (PLS153A)

Field Programmable Logic Array (18 × 42 × 10)

Military
Customer Specific Products

Signetics Programmable Logic

Product Specification

DESCRIPTION

The 82S153A is a two-level logic element, consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 8 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 directional control gates (D), ranging from 18 inputs to 10 outputs.

On chip T/C buffers couple either True (I,B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The 82S153A is field programmable, enabling the use to quickly generate custom patterns using standard programming equipment.

FEATURES

- Field-Programmable (Ni-Cr links)
- 8 inputs
- 42 AND gates
- 10 OR gates
- 10 bidirectional I/O lines
- Active-High or -Low outputs
- 42 Product Terms:
  - — 32 Logic Terms
  - — 10 Control Terms
- I/O propagation delay: 42ns (max)
- Input loading: -150μA (max)
- Power dissipation: 650mW (typ.)
- 3-State outputs
- TTL compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A * B * C * D * \ldots$

TYPICAL LOGIC FUNCTION:

AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L

$\overline{Z} = \overline{P0} + \overline{P1} + \overline{P2} + \ldots$

$Z = \overline{P0} * \overline{P1} * \overline{P2} \ldots$

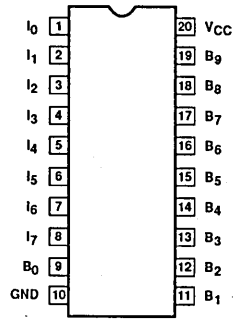
NOTES:

1. For each of the 10 outputs, either function Z (active-high) or Z (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C etc. are user defined connections to fixed inputs (I) and bidirectional pins (B).

ORDERING INFORMATION

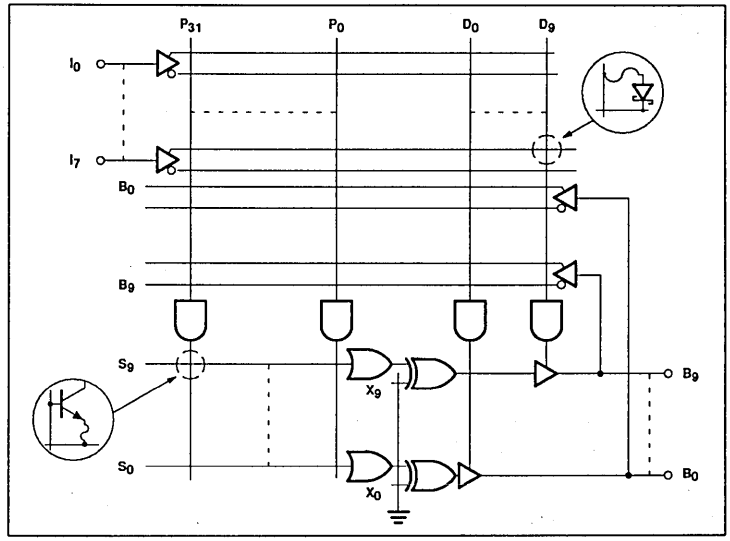
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP 300mil-wide	82S153A/BRA
20-Pin Ceramic FlatPack	82S153A/BSA
20-Pin Ceramic LLCC	82S153A/B2A

PIN CONFIGURATION



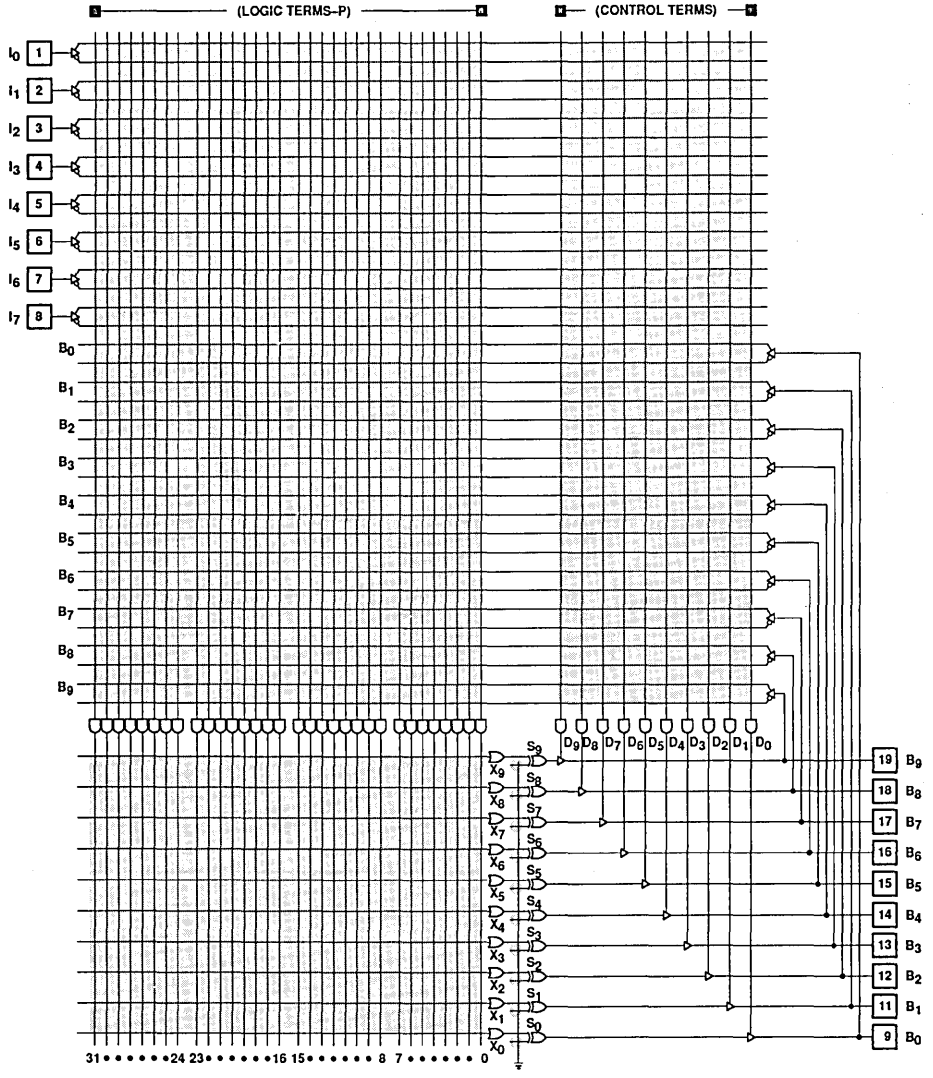
For LLCC pin assignments, see Package Section

FUNCTIONAL DIAGRAM



Field Programmable Logic Array (18 × 42 × 10) — 82S153A

FPLA LOGIC DIAGRAM



NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. ○ Programmable connection.

Field Programmable Logic Array (18 × 42 × 10) — 82S153A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply Voltage		+7	V_{DC}
V_I	Input voltage		+10.0	V_{DC}
V_O	Output voltage		+5.5	V_{DC}
I_I	Input currents	-30	+30	mA
I_O	Output currents		+100	mA
T_A	Operating Temperature Range	-55	+125	°C
T_{STG}	Storage Temperature Range	-65	+150	°C

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS[3]			UNIT
			Min	Typ[2]	Max	
Input Voltage						
V_{IL}	Low	$V_{CC} = 4.5V$			0.80	V
V_{IH}	High	$V_{CC} = 5.5V$	2.0			V
V_{IK}	Clamp[4]	$V_{CC} = 4.5V$, $I_I = -18mA$		-0.8	-1.2	V
Output Voltage						
V_{OL}	Low[5]	$V_{CC} = 4.5V$, $I_{OL} = 12mA$			0.5	V
V_{OH}	High[6]	$I_{OH} = 2mA$	2.4			V
Input current						
I_{IL}	Low	$V_{CC} = 5.5V$, $V_I = 0.45V$			-150	µA
I_{IH}	High	$V_I = 5.5V$			50	µA
Output current						
$I_{O(OFF)}$	Hi-Z state[10]	$V_{CC} = 5.5V$, $V_O = 5.5V$			110	µA
		$V_O = 0.45V$			-210	µA
I_{OS}	Short circuit[4,6,7]	$V_O = 0V$	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	$V_{CC} = 5.5V$		130	165	mA
Capacitance[12]						
C_{IN}	Input	$V_{CC} = 5V$, $V_I = 2.0V$		8	13	pF
C_B	I/O	$V_B = 2.0V$		15	20	pF

Field Programmable Logic Array (18 × 42 × 10) — 82S153A

AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

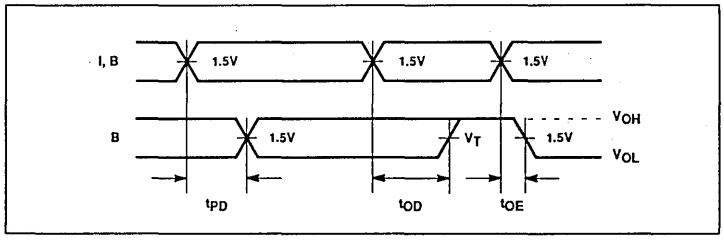
SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ[2]	Max	
t_{PD}	Propagation delay	Output ±	Input ±	C_L = 30pF		20	45	ns
t_{OE}	Output enable	Output ±	Input ±			20	40	ns
t_{OD}	Output disable[9, 11]	Output ±	Input ±	C_L = 5pF		20	40	ns

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with +10V applied to I_7.
6. Measured with +10V applied to I_{0-7}. Output sink current is supplied through a resistor to V_{CC}.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with $I_{0,1}$ grounded, I_{2-7} and B_{0-9} at 4.5V.
9. Measured at $V_T = V_{OL} + 0.5V$.
10. Leakage values are a combination of input and output leakage.
11. Not testable on unprogrammed device.
12. Guaranteed, but not tested.

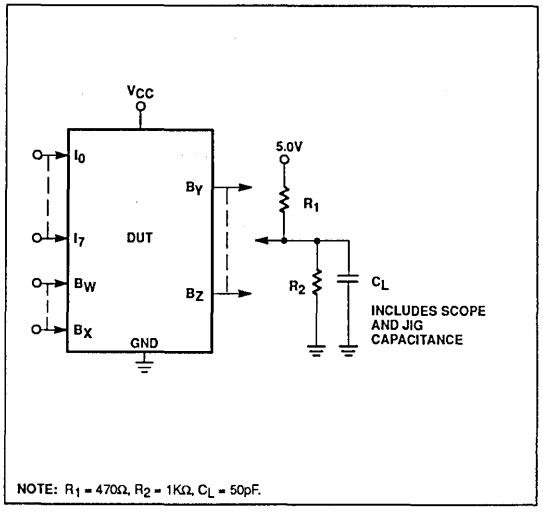
TIMING DEFINITIONS

SYMBOL	PARAMETER
T_{PD}	Propagation delay between input and output.
T_{DD}	Delay between input change and when output is off (Hi-Z or High).
T_{DE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAMS

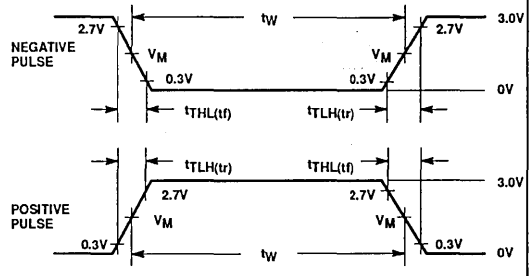


TEST LOAD CIRCUITS



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF.

VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Field Programmable Logic Array (18 × 42 × 10) — 82S153A

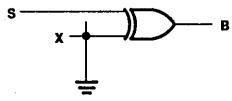
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

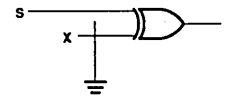
With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this table the logic state of variables I, P, and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY – (B)

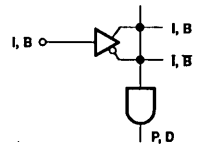


ACTIVE LEVEL	CODE
HIGH	H

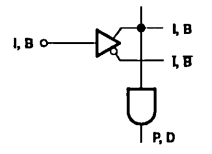


ACTIVE LEVEL	CODE
LOW	L

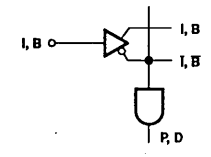
AND ARRAY – (I, B)



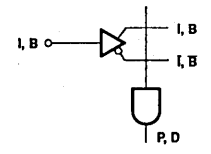
STATE	CODE
INACTIVE[13,14]	O



STATE	CODE
I, B	H

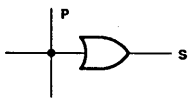


STATE	CODE
I, B	L

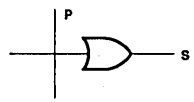


STATE	CODE
DON'T CARE	–

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE	A



P_n STATUS	CODE
INACTIVE	•

NOTES:

13. This is the initial unprogrammed state of all links.
14. Any gate P_n will be unconditioanlly inhibited if both the True and Complement of an input (either I or B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

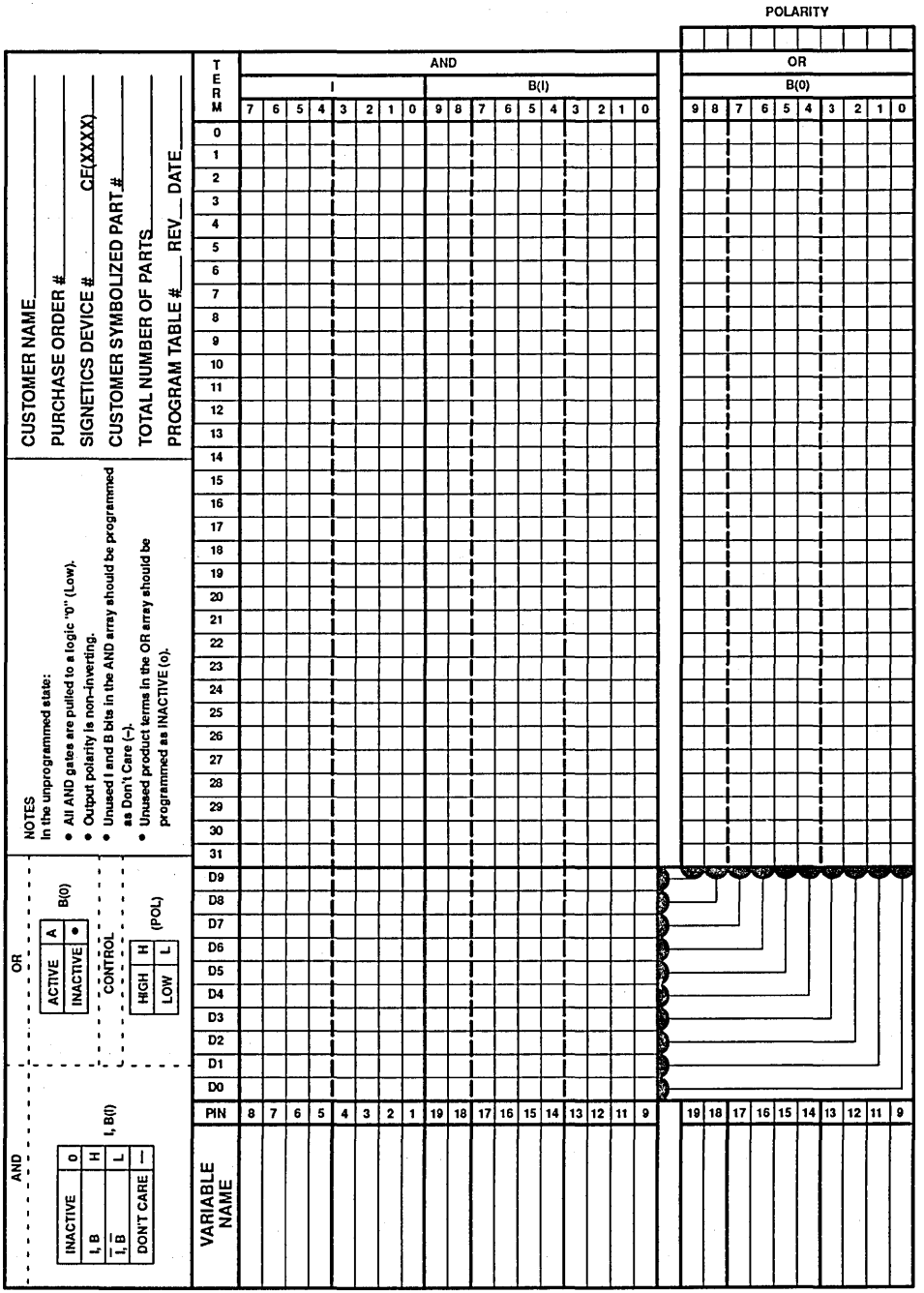
CAUTION: 82S153A TEST COLUMNS

The 82S153A incorporates two columns not shown in the logic block diagram. These columns are used for in-house testing of the device in the unprogrammed state. These columns must be disabled prior to using the 82S153A in your application. If you are using a Signetics-approved programmer, the disabling is accomplished during the device programming sequence. If these columns are not disabled, abnormal operation is possible.

Field Programmable Logic Array (18 × 42 × 10)

82S153A

FPLA PROGRAM TABLE

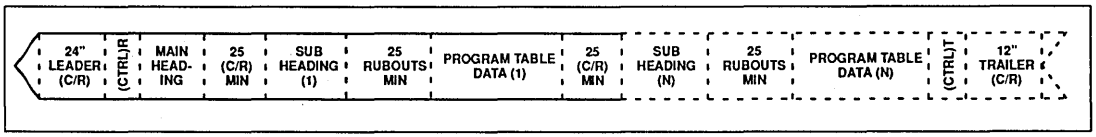


Field Programmable Logic Array (18 × 42 × 10) — 82S153A

TWX TAPE CODING (LOGIC FORMAT)

The FPLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however, limit tape length to a roll of 1.75 inch inside diameter and 4.25 outside diameter.



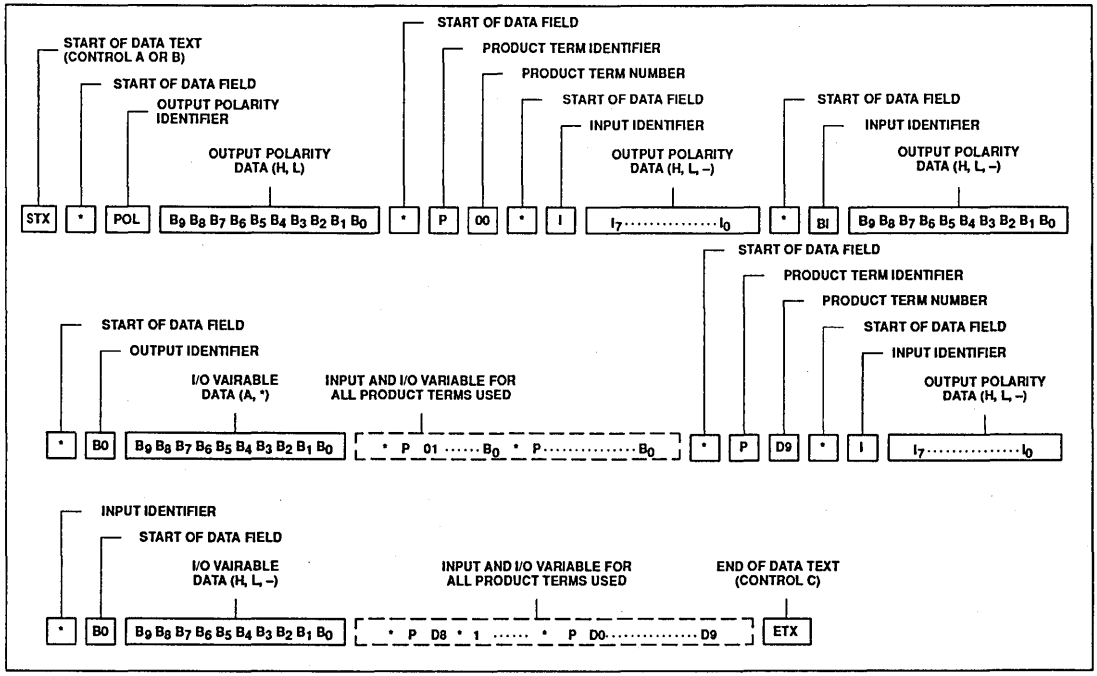
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

___1. Customer Name_____
___2. Customer TWX No._____
___3. Date_____
___4. Purchase Order No._____
___5. Number of Program Tables_____
___6. Total Number of Parts_____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

___1. Signetics Device No._____
___2. Program Table No._____
___3. Revision_____
___4. Date_____
___5. Customer Symbolized Part No._____
___6. Number of Parts_____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of output polarity, product term, and output information separated by appropriate identifiers in accordance with the following format. Entries for the data fields correspond to those defined in the Logic PROGRAM TABLE:



Signetics

PLC18V8Z
Zero Standby Power Universal PAL®-type Devices

Preliminary Specification

Signetics Military Programmable Logic

DESCRIPTION

The PLC18V8Z is a universal PAL-type device featuring high performance and virtually zero-standby power for power sensitive applications. It is a reliable, user-configurable substitute for discrete TTL/CMOS logic. While compatible with TTL and HCT it can also replace HC logic over the V_{CC} range of 4.5 to 5.5V.

The PLC18V8Z is a two-level logic element comprised of 10 inputs, 74 AND gates (product terms) and 8 output Macro cells.

Each output features an "Output Macro Cell" which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback. As a result, the it is capable of emulating all common 20-pin PAL devices to reduce documentation, inventory, and manufacturing costs.

A power-up reset function and a Register Preload function have been incorporated in the architecture to facilitate state machine design and testing.

With a standby current of less than 100µA and active power consumption of 1.5mA/MHz, the device is ideally suited for power sensitive applications in battery operated/backed portable instruments and computers.

The PLC18V8Z is also processed to industrial requirements for operation over an extended temperature range of -55°C to +125°C and supply voltage of 4.5V to 5.5V.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic Dual In-Line Package 300mil-wide	PLC18V8Z/ BRA (OT)
20-Pin Ceramic Dual In-Line Package 300mil-wide w/ quartz window	PLC18V8Z/ BRA
20-Pin Ceramic LLCC 350mil square	PLC18V8/B2A (OT)

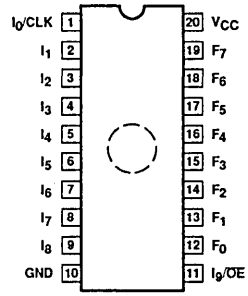
FEATURES

- **20-pin Universal Programmable Array Logic**
- **Virtually Zero-Standby-power**
- **Functional replacement for Series 20 PAL devices**
  - **I_{OL} = 24mA**
- **High-performance CMOS EPROM cell technology**
  - **Erasable**
  - **Reconfigurable**
  - **100% testable**
- **40ns Max propagation delay.**
- **Up to 18 inputs and 8 input/output macro cells**
- **Programmable output polarity**
- **Power-up reset on all registers**
- **Register Preload capability**
- **Synchronous Preset/Asynchronous Reset**
- **Security fuse to prevent duplication of proprietary designs**
- **Design support provided using AMAZE software development package and other CAD tools for PLDs**
- **Available in 300mil-wide DIP with quartz window, ceramic DIP (OTP) or LLCC (OTP)**

APPLICATIONS

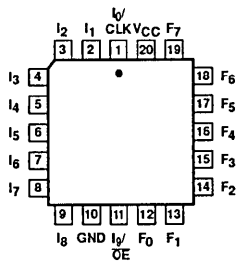
- **Battery powered instruments**
- **Laptop and pocket computers**
- **Industrial control**
- **Medical Instruments**
- **Portable communications equipment**

F and FA Packages



FA = Ceramic with Quartz Window
F = Ceramic OTP

A Package



PIN LABEL DESCRIPTIONS

I	Dedicated input
B	Bidirectional input/output
O	Dedicated output
D	Registered output (D-type flip-flop)
F	Macrocell Input/Output
CLK	Clock Input
$\overline{OE}$	Output Enable
V_{CC}	Supply Voltage
GND	Ground

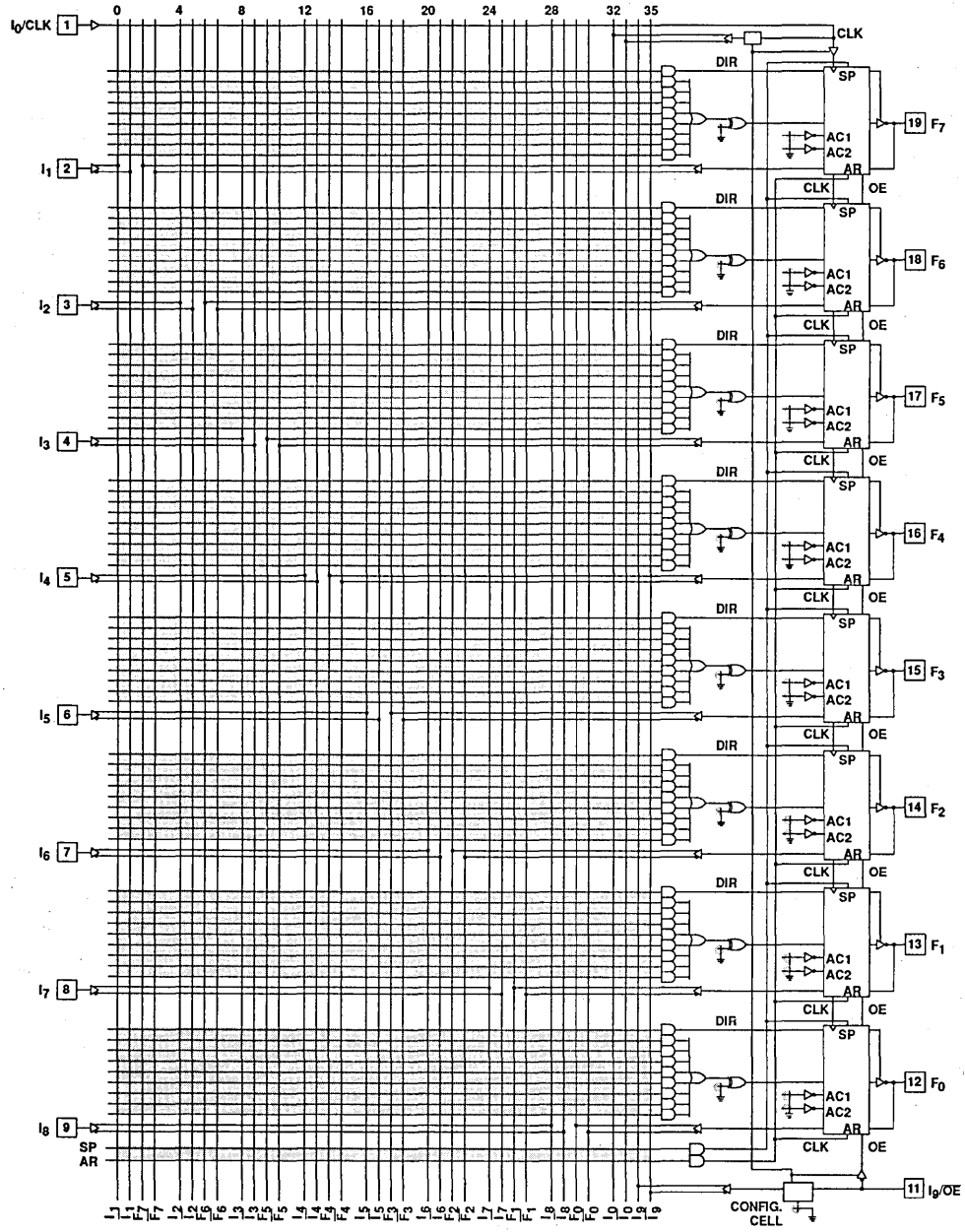
PIN CONFIGURATIONS

®PAL is a registered trademark of Monolithic Memories, Inc., a wholly owned subsidiary of Advanced Micro Devices, Inc.

Zero Standby Power Universal PAL-Type Devices

PLC18V8Z Series

LOGIC DIAGRAM



NOTES:
In the unprogrammed or virgin state:

All cells are in a conductive state.
All AND gate locations are pulled to a logic "0" (Low).
Output polarity is inverting.

Pins 1 and 11 are configured as Inputs 0 and 9, respectively, via the configuration cell. The clock and OE functions are disabled.
All output macro cells (OMC) are configured as bidirectional I/O, with the outputs disabled via the direction term.
Denotes a programmable cell location.

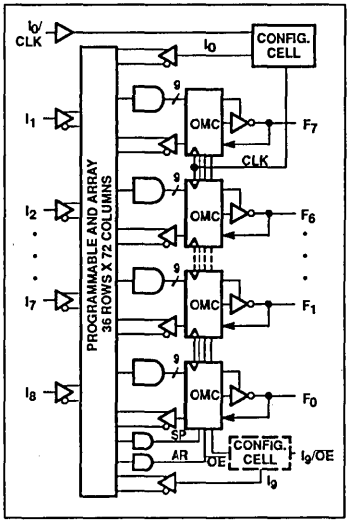
Zero Standby Power Universal PAL-Type Devices

PLC18V8Z Series

PAL DEVICE TO PLC18V8Z OUTPUT PIN CONFIGURATION CROSS REFERENCE

PIN NO.	PLC 18V8Z	16L8 16H8 16P8 16P8	16R4 16RP4	16R6 16RP6	16R8 16RP8	16L2 16H2 16P2	14L4 14H4 14P4	12L6 12H6 12P6	10L8 10H8 10P8
1	I_0/CLK	I	CLK	CLK	CLK	I	I	I	I
19	F7	B	B	B	D	I	I	I	O
18	F6	B	B	D	D	I	I	O	O
17	F5	B	D	D	D	I	O	O	O
16	F4	B	D	D	D	O	O	O	O
15	F3	B	D	D	D	O	O	O	O
14	F2	B	D	D	D	I	O	O	O
13	F1	B	B	D	D	I	I	O	O
12	F0	B	B	B	D	I	I	I	O
11	I_9/$\overline{OE}$	I	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	I	I	I	I

FUNCTIONAL DIAGRAM



The Signetics state-of-the-art Floating-Gate CMOS EPROM process yields bipolar equivalent performance at less than one-quarter the power consumption. The erasable nature of the EPROM process enables Signetics to functionally test the devices prior to shipment to the customer. Additionally, this allows Signetics to extensively stress test, as well as ensure the threshold voltage of each individual EPROM cell. 100% programming yield is subsequently guaranteed.

THE OUTPUT MACRO CELL (OMC)

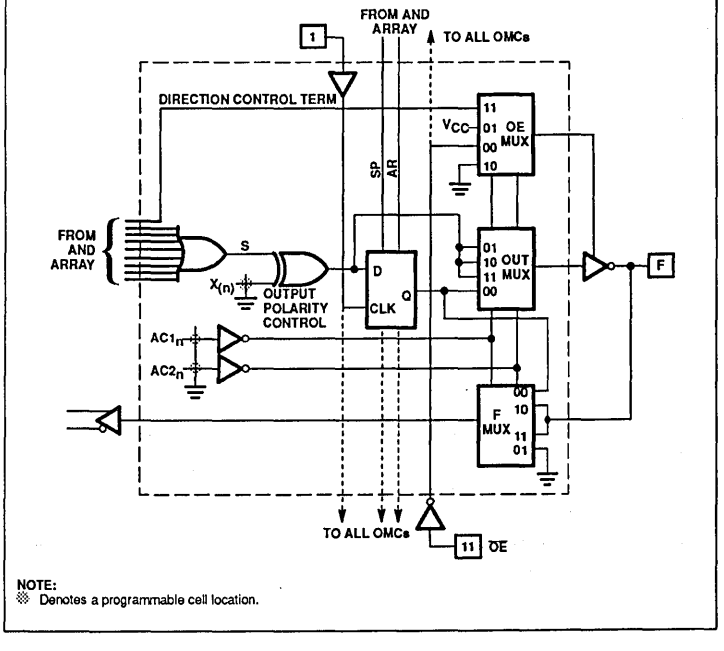
The PLC18V8Z series devices have 8 individually programmable Output Macro Cells. The 74 AND inputs (or product terms) from the programmable AND array are connected to the 8 OMCs in groups of 9. Eight of the AND terms are dedicated to logic functions; the ninth is for asynchronous direction control, which enables/disables the respective bidirectional I/O pin. Two product terms are dedicated for the Synchronous Preset and Asynchronous Reset functions.

Each OMC can be independently programmed via 16 architecture control bits, $AC1_n$ and $AC2_n$ (one pair per macro cell). Similarly, each OMC has a programmable output polarity control bit (Xn). By configuring the pair of architecture control bits according to the configuration cell table, 4 different configurations may be implemented. Note that the configuration cell is automatically programmed based on the OMC configuration.

DESIGN SECURITY

The PLC18V8Z series devices have a programmable security fuse that controls the access to the data programmed in the device. By using this programmable feature, proprietary designs implemented in the device cannot be copied or retrieved.

OUTPUT MACRO CELL (OMC)



NOTE:
▒ Denotes a programmable cell location.

Zero Standby Power Universal PAL-Type Devices

PLC18V8Z Series

CONFIGURATION CELL

A single configuration cell controls the functions of Pins 1 and 11. Refer to Functional Diagram. When the configuration cell is programmed, Pin 1 is a dedicated clock and Pin 11 is dedicated for output enable. When the configuration cell is unprogrammed, Pins 1 and 11 are both dedicated inputs. Note that the output enable for all registered OMCs is common—from Pin 11 only. Output enable control of the bidirectional I/O OMCs is provided from the AND array via the direction product term.

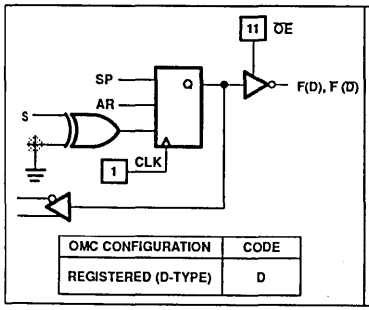
If any one OMC is configured as registered, the configuration cell will be automatically configured (via the design software) to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively. If none of the OMCs are registered, the configuration cell will be programmed such that Pins 1 and 11 are dedicated inputs. The programming codes are as follows:

Pin 1 = CLK, Pin 11 = $\overline{OE}$	L
Pin 1 and Pin 11 = Input	H

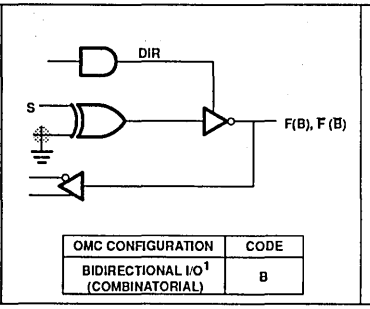
FUNCTION	CONTROL CELL CONFIGURATIONS			COMMENTS
	$AC1_1$	$AC2_N$	CONFIG. CELL	
Registered mode	Programmed	Programmed	Programmed	Dedicated clock from Pin 1. $\overline{OE}$ Control for all registerd OMCs from Pin 11 only.
Bidirectional I/O mode[1]	Unprogrammed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. 3-State control from AND array only.
Fixed input mode	Unprogrammed	Programmed	Unprogrammed	Pins 1 and 11 are dedicated inputs.
Fixed output mode	Programmed	Unprogrammed	Unprogrammed	Pins 1 and 11 are dedicated inputs. The feedback path (via F_{MUX}) is disabled.

NOTE:
1. This is the virgin state as shipped from the factory.

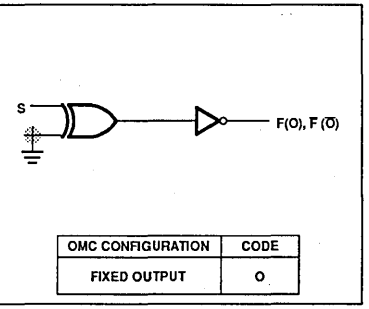
ARCHITECTURE CONTROL—AC1 and AC2



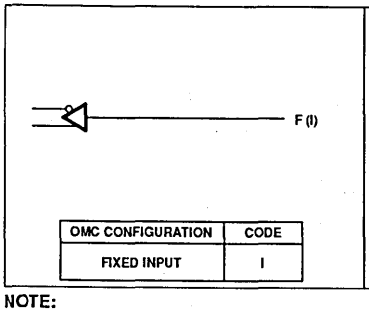
OMC CONFIGURATION	CODE
REGISTERED (D-TYPE)	D



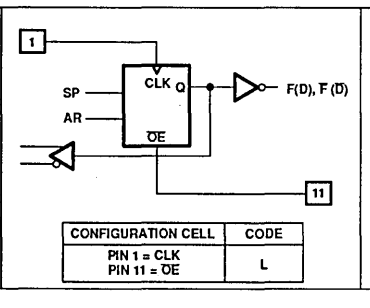
OMC CONFIGURATION	CODE
BIDIRECTIONAL I/O[1] (COMBINATORIAL)	B



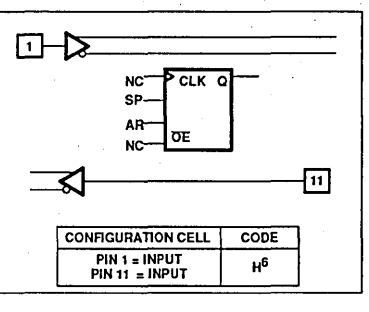
OMC CONFIGURATION	CODE
FIXED OUTPUT	O



OMC CONFIGURATION	CODE
FIXED INPUT	I



CONFIGURATION CELL	CODE
PIN 1 = CLK PIN 11 = $\overline{OE}$	L



CONFIGURATION CELL	CODE
PIN 1 = INPUT PIN 11 = INPUT	H[6]

NOTE:
A factory shipped unprogrammed device is configured such that:
1. This is the initial unprogrammed state. All cells are in a conductive state.
2. All AND gates are pulled to a logic "0" (Low).
3. Output polarity is inverting.
4. Pins 1 and 11 are configured as inputs 0 and 9. The clock and $\overline{OE}$ functions are disabled.
5. All Output Macro Cells (OMCs) are configured as bidirectional I/O, with the outputs disabled via the direction term.
6. This configuration cannot be used if any OMCs are configured as registered (Code = D). The configuration cell will be automatically configured to ensure that the clock and output enable functions are enabled on Pins 1 and 11, respectively, if any one OMC is programmed as registered.

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V_{DC}
V_{CC}	Operating supply voltage	4.5 to 5.5	V_{DC}
V_{IN}	Input voltage	-0.5 to V_{CC} + 0.5	V_{DC}
V_{OUT}	Output voltage	-0.5 to V_{CC} + 0.5	V_{DC}
I_{IN}	Input currents	-10 to +10	mA
I_{OUT}	Output currents	+24	mA
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:
1. Stresses above those listed may cause malfuncion or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ[1]	Max	
Input voltage						
V_{IL}	Low	V_{CC} = Min	-0.3		0.8	V
V_{IH}	High	V_{CC} = Max	2.0		V_{CC} + 0.3	V
Output voltage[2]						
V_{OL}	Low	V_{CC} = Min, I_{OL} = 20µA V_{CC} = Min, I_{OL} = 24mA			0.100 0.500	V V
V_{OH}	High	V_{CC} = Min, I_{OH} = -3.2mA V_{CC} = Min, I_{OH} = -20µA	2.4 V_{CC} - 0.1V			V V
Input current						
I_{IL}	Low[7]	V_{IN} = GND			-10	µA
I_{IH}	High	V_{IN} = V_{CC}			10	µA
Output current						
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND			10 -10	µA µA
I_{OS}	Short-circuit[3]	V_{OUT} = GND			-130	mA
I_{CC}	V_{CC} supply current (Standby)	V_{CC} = Max, V_{IN} = 0 or V_{CC}[8]			100	µA
I_{CC}/f	V_{CC} supply current (Active)[4]	V_{CC} = Max (CMOS inputs)[5, 6]			1.5	mA/MHz
Capacitance						
C_I	Input	V_{CC} = 5V V_{IN} = 2.0V		12	17	pF
C_B	I/O	V_B = 2.0V		15	20	pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all outputs switching.
5. ΔI_{CC}/TTL input = 2mA.
6. ΔI_{CC} vs frequency (registered configuration) = 2mA/MHz.
7. I_{IL} for Pin 1 (I_O/CLK) is ± 10µA with V_{IN} = 0.4V.
8. V_{IN} includes CLK and $\overline{OE}$ if applicable.

Zero Standby Power Universal PAL-Type Devices

PLC18V8Z Series

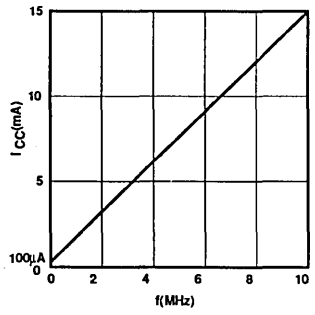


Figure 1. I_{CC} vs Frequency (Worst Case)

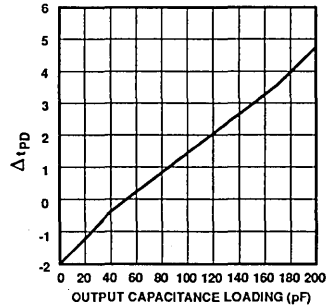


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

Zero Standby Power Universal PAL-Type Devices

PLC18V8Z Series

AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

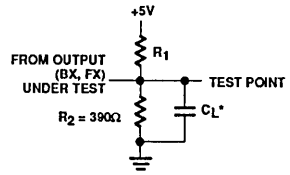
SYMBOL	PARAMETER	FROM	TO	TEST CONDITION[1]		LIMITS		UNIT
				R_1 (Ω)	C_L (pF)	Min	Max	
Pulse width								
t_{CKP}	Clock period (Minimum $t_{IS} + t_{CKO}$)	CLK +	CLK +	200	50	57		ns
t_{CKH}	Clock width High	CLK +	CLK -	200	50	25		ns
t_{CKL}	Clock width Low	CLK -	CLK +	200	50	25		ns
t_{ARW}	Async reset pulse width	I ±, F±	I $\mp$, F $\mp$			40	ns	
Hold time								
t_{IH}	Input or feedback data hold time	CLK +	Input ±	200	50	0		ns
Setup time								
t_{IS}	Input or feedback data setup time	I ±, F±	CLK +	200	50	30		ns
Propagation delay								
t_{PD}	Delay from input to active output	I ±, F±	F±	200	50		40	ns
t_{CKO}	Clock High to output valid access Time	CLK +	F±	200	50		27	ns
t_{OE1}[3]	Product term enable to outputs off	I ±, F±	F±	Active-High R = 1.5k Active-Low R = 550	50		40	ns
t_{OD1}[2]	Product term disable to outputs off	I ±, F±	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		40	ns
t_{OD2}[2]	Pin 11 output disable High to outputs off	OE -	F±	From V_{OH} R = ∞ From V_{OL} R = 200	5		30	ns
t_{OE2}[3]	Pin 11 output enable to active output	OE +	F±	Active-High R = 1.5k Active-Low R = 550	50		30	ns
t_{ARD}	Async reset delay	I ±, F±	F +				40	ns
t_{ARR}	Async reset recovery time	I ±, F±	CLK +			30		ns
t_{SPR}	Sync preset recovery time	I ±, F±	CLK +			30		ns
t_{PPR}	Power-up reset	V_{CC} +	F +				40	ns
Frequency of operation								
f_{MAX}	Maximum frequency	$1/(t_{IS} + t_{CKO})$		200	50		18	MHz

NOTES:
1. Refer also to AC Test Conditions. (Test Load Circuit)
2. 3-State levels are measured +0.5V from the active steady-state level.
3. Resistor values of 1.5k and 550W provide 3-State levels of 1.0V and 2.0V, respectively. Output timing measurements are to 1.5V level.

Zero Standby Power Universal PAL-Type Devices

PLC18V8Z Series

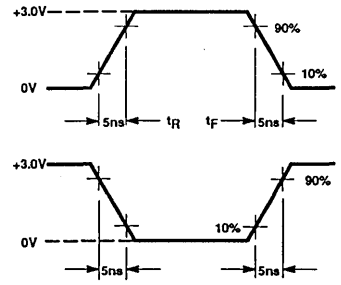
AC TEST CONDITIONS



*C_L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

Test Load Circuit

VOLTAGE WAVEFORMS



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

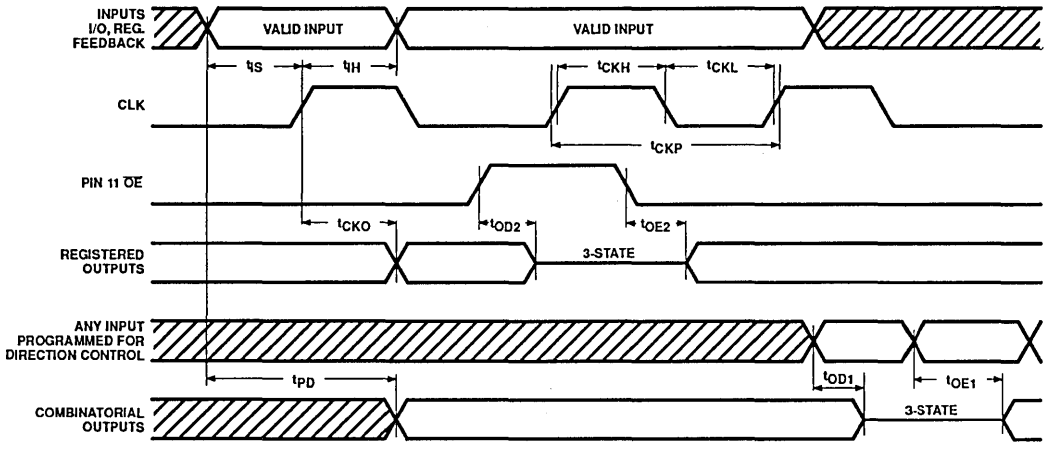
POWER-UP RESET

In order to facilitate state machine design and testing, a power-up reset function has been incorporated in the PLC18V8Z. All internal registers will reset to active-Low (logical "0") after a specified period of time (t_{PPR}). Therefore, any OMC that has been configured as a registered output will always produce an active-High on the associated output pin because of the inverted output buffer. The internal feedback (Q) of a registered OMC will also be set Low. The programmed polarity of OMC will not affect the active-High output condition during a system power-up condition.

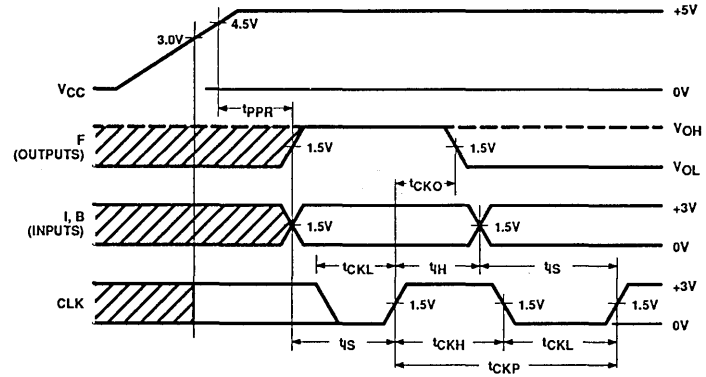
Zero Standby Power Universal PAL-Type Devices

PLC18V8Z Series

TIMING DIAGRAMS



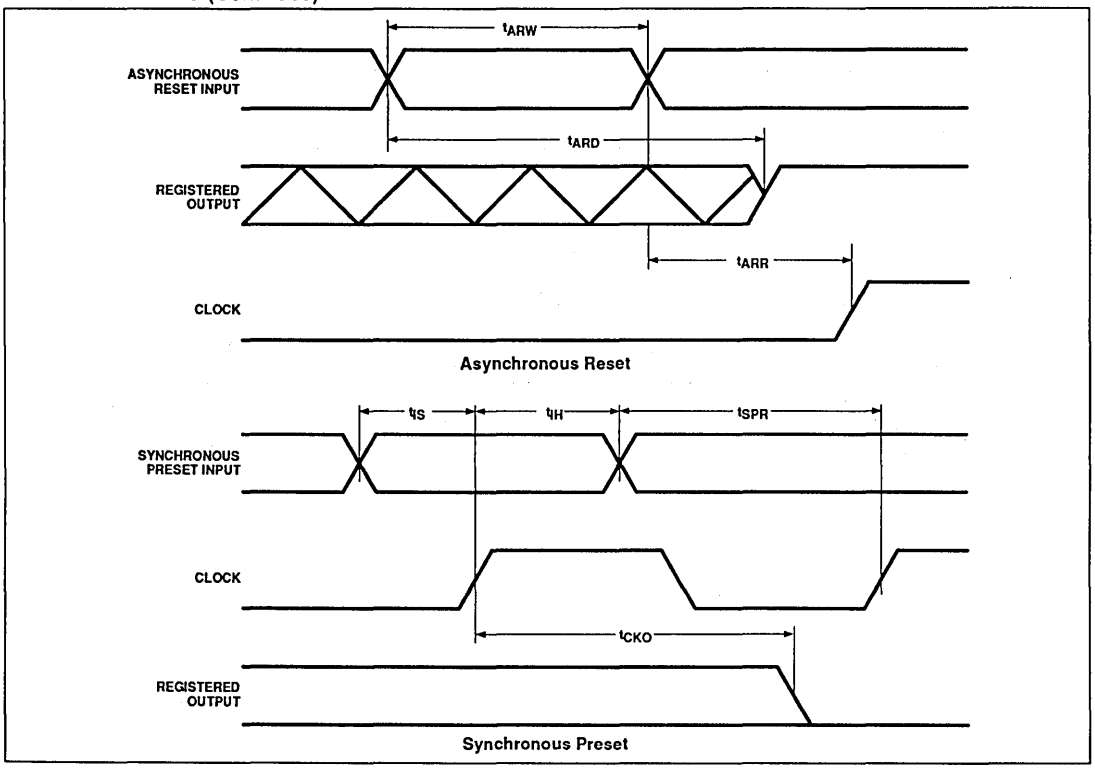
Switching Waveforms



NOTE:
Diagram presupposes that the outputs (F) are enabled. The reset occurs regardless of the output condition (enabled or disabled).

Power-Up Reset

TIMING DIAGRAMS (Continued)



REGISTER PRELOAD FUNCTION (DIAGNOSTIC MODE ONLY)

In order to facilitate the testing of state machine/controller designs, a diagnostic mode register preload feature has been incorporated into the PLC18V8Z series device. This feature enables the user to load the registers with predetermined states while a super voltage is applied to Pins 11 and 6 ($I_9/\overline{OE}$ and I_5). (See diagram for timing and sequence.)

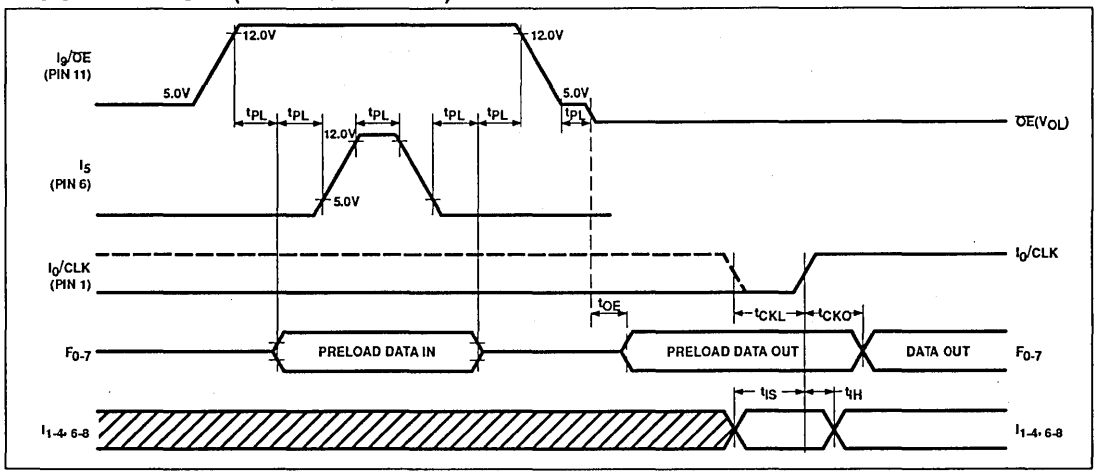
To read the data out, Pins 11 and 6 must be returned to normal TTL levels. The outputs, F_{0-7}, must be enabled in order to read data out. The Q outputs of the registers will reflect data in as input via F_{0-7} during preload. Subsequently, the register Q output via the feedback path will reflect the data in as input via F_{0-7}.

Refer to the voltage waveform for timing and voltage references. t_{PL} = 10µsec.

Zero Standby Power Universal PAL-Type Devices

PLC18V8Z Series

REGISTER PRELOAD (DIAGNOSTIC MODE)



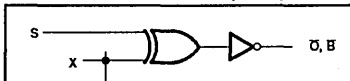
LOGIC PROGRAMMING

The PLC18V8Z can be programmed by means of Logic Programming equipment.

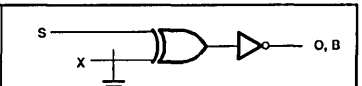
With Logic programming, the AND/OR/Ex-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table. Similarly, various OMC configurations are implemented by programming the Architecture Control bits AC1 and AC2. Note that the configuration cell is automatically programmed based on the OMC configuration.

In this table, the logic state of variables I, P and B associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY - (O, B)

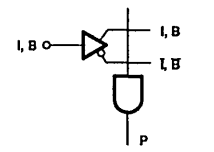


ACTIVE LEVEL	CODE
INVERTING[1]	L

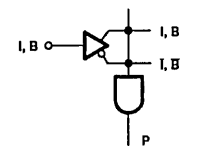


ACTIVE LEVEL	CODE
NON-INVERTING	H

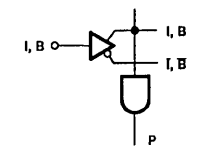
"AND" ARRAY - (I, B)



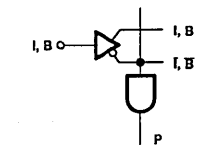
STATE	CODE
DON'T CARE	-



STATE	CODE
INACTIVE[1]	O



STATE	CODE
I, B	H



STATE	CODE
I, B	L

NOTE:

1. A factory shipped unprogrammed device is configured such that all cells are in a conductive state.

Zero Standby Power Universal PAL-Type Devices

PLC18V8Z Series

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC18V8Z Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lighting could erase a typical PLC18V8Z in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC18V8Z is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC18V8Z is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000µW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

PROGRAMMING

The PLC18V8Z35/I is programmable on conventional programmers for 20-pin PAL devices. Refer to the following charts for qualified manufacturers of programmers and software tools:

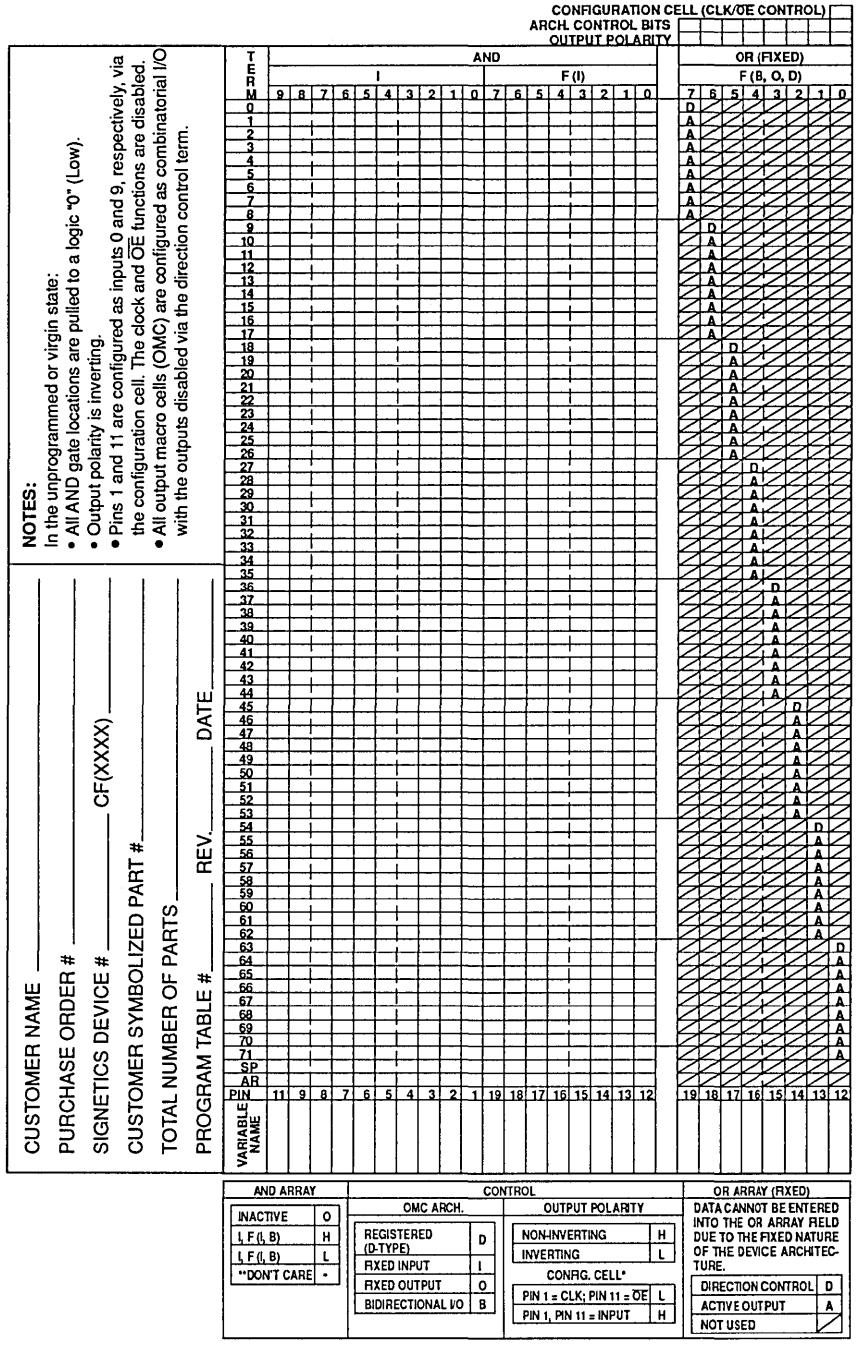
PROGRAMMER MANUFACTURER	PROGRAMMER MODEL	FAMILY/PINOUT CODES
DATA I/O CORPORATION 10525 WILLOWS ROAD, N.E. P.O. BOX 97046 REDMOND, WASHINGTON 98073-9746 (800) 247-5700	System 29B, LogicPak™ 303A-011A; V09 (DIL) 303A-011B; V04 (PLCC) UNISITE 40/48 V2.5 (DIL) Chipsite (PLCC) - TBA MODEL 60 TBA	86/4F
STAG MICROSYSTEMS, INC. 1600 WYATT DRIVE, SUITE 3 SANTA CLARA, CALIFORNIA 95054 (408) 988-1118	ZL30/30A PROGRAMMER REV. 30A34 (DIL) 30A001 Adaptor (PLCC) PPZ PROGRAMMER TBA	12/205

SOFTWARE MANUFACTURER	DEVELOPMENT SYSTEM
SIGNETICS COMPANY 811 EAST ARQUES AVENUE P.O. BOX 3409 SUNNYVALE, CALIFORNIA 94088-3409 (408) 991-2000	AMAZE SOFTWARE REV. 1.8 AND LATER
DATA I/O 10525 WILLOWS ROAD, N.E. P.O. BOX 97046 REDMOND, WASHINGTON 98073-9746 (800) 247-5700	ABEL™ SOFTWARE
LOGICAL DEVICES, INC. 1201 NORTHWEST 65TH PLACE FORT LAUDERDALE, FLORIDA 33309 (800) 331-7766	CUPL™ SOFTWARE

Zero Standby Power Universal PAL-Type Devices

PLC18V8Z Series

PROGRAM TABLE



* THE CONFIGURATION CELL IS AUTOMATICALLY PROGRAMMED BASED ON THE OMC ARCHITECTURE.
** FOR SP, AR: "-" IS NOT ALLOWED.

Signetics

PLHS18P8A

Programmable AND Array Logic (18 × 72 × 8)

Military
Standard Products

Product Specification

DESCRIPTION

The PLHS18P8A is a two-level logic element consisting of 72 AND gates and 8 OR gates with fusible connections for programming I/O polarity and direction.

All AND gates are linked to 10 inputs (I) and 8 bidirectional I/O lines (B). These yield variable I/O gate configurations via 8 directional control gates, ranging from 18 inputs to 8 outputs.

On-chip T/C buffers couple either True ($\overline{I}$, $\overline{B}$) or Complement (I, B) input polarities to all AND gates. The 72 AND gates are separated into 8 groups of 9 each. Each group of 9 is associated with one bidirectional pin. In each group, eight of the AND terms are ORed together, while the ninth is used to establish I/O direction. All outputs are individually programmable via an EX-OR gate to allow implementation of AND/OR or NAND/NOR logic functions.

In the virgin state, the AND array fuses are back-to-back CB-EB diode pairs which will act as open connections.

Current is avalanched across individual diode pairs during fusing, which essentially short circuits the EB diode and provides the connection for the associated product term.

The PLHS18P8A is field-programmable, allowing the user to quickly generate custom pattern using standard programming equipment.

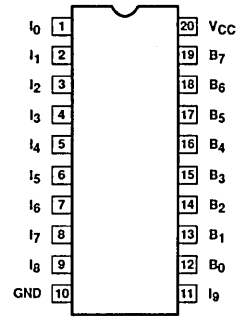
FEATURES

- **100% functionally compatible with AmPAL18P8A**
- **Field Programmable**
- **10 Inputs**
- **8 bidirectional I/O lines**
- **72 AND gates/product terms - configured into eight groups of nine**
- **Programmable output polarity (3-State output)**
- **I/O propagation delay: 30ns (max)**
- **Power dissipation: 750mW (nominal)**
- **TTL compatible**
- **Verify Lock Fuse**
- **On-chip test features for extensive AC and DC parametric testing**

APPLICATIONS

- **100% functional replacement for all 20-pin combinatorial PALs**
- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

PIN CONFIGURATION



For LLCC Pin Assignments see Jedec Standard 21A

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP 300mil-wide	PLHS18P8A/BRA
20-Pin Ceramic LLCC	PLHS18P8A/B2A
20-Pin Ceramic Flat Pack	PLHS18P8A/BSA

Programmable AND Array Logic (18 × 72 × 8) — PLHS18P8A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply voltage	-0.5	+7	V_{DC}
V_I	Input voltage range	-0.5	+5.5	V_{DC}
V_O	Output voltage range	-0.5	V_{CC}MAX	V_{DC}
V_{OUTPRG}	Output voltage range (programming)		+21	V_{DC}
I_I	Input current range	-30	+5	mA
I_O	Output current range		+100	mA
I_{OUTPGR}	Output current range (programming)		+170	mA
T_{STG}	Storage temperature range	-65	+150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	High level input voltage[3]	2.0			V
I_{IL}	Low level input voltage[3]			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High level output current			-2	mA
I_{OL}	Low level output current			24	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{IK}	Input clamp voltage	V_{CC} = Min, I_{IN} = Max		-0.9	-1.2	V
V_{OL}	Output low voltage[10]	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}[8], I_{OL} = Max			+0.50	V
V_{OH}	Output high voltage[10]	V_{CC} = Min, I_{OH} = 2.0mA, $V_{IN} = V_{IH}$ or V_{IL}	+2.4	+3.5		V
I_{IL}	Input low current	V_{CC} = Max, V_I = +0.40V		-20	-100	µA
I_{IH}	Input high current	V_{CC} = Max, V_I = +2.7V			+25	µA
I_I	Input high current	V_{CC} = Max, V_I = +5.5V			+1.0	mA
I_{OHZ}	Offstate output current high level[7]	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min[8], V_O = +2.7V			+100	µA
I_{OLZ}	Offstate output current low level[7]	V_{CC} = Max, V_O = +0.40V, V_{IL} = Max, V_{IH} = Min			-250	µA
I_{SC}	Output short circuit current[4,9]	V_{CC} = Max, V_O = +0.5V	-30	-60	-90	mA
I_{CC}	V_{CC} Supply current[6]	V_{CC} = Max		100	180	mA
C_{IN}	Input capacitance[5]	V_{CC} = +5V, V_I = 2.0V		9		pF
C_{OUT}	I/O capacitance[5]	V_{CC} = +5V, V_O = 2.0V		13		pF

Programmable AND Array Logic (18 × 72 × 8) — PLHS18P8A

AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V R1 = 200Ω, R2 = 390Ω

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ[2]	Max	
t_{PD}[11]	Propagation delay	Input ±	Output ±	C_L = 50pF		15	30	ns
t_{EA}[12]	Output enable	Input ±	Output ±	C_L = 50pF		15	30	ns
t_{ER}[12]	Output disable	Input ±	Output ±	C_L = 50pF		15	30	ns

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. Typical limits are at V_{CC} = 5.0V and T_A = +25°C.
3. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included. Testing these values requires special equipment.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_O = 0.5V has been chosen to avoid test problems caused by tester ground degradation.
5. These parameters are not tested.
6. I_{CC} is measured with all inputs grounded.
7. On unprogrammed devices, Pins 8 & 9 = 10V. On programmed device, Pin 4 = 0.4V.
8. V_{IL} and V_{IH} only tested on a programmed device.
9. Pin 11 = 10V for testing unprogrammed device.
10. Pin 11 = 0V for testing unprogrammed device.
11. t_{PD} is tested with switch S_1 closed and C_L = 50pF.
12. For Tri-state output; output enable times are tested with C_L = 50pF to the 1.5 V level, and S_1 is open of high-impedance to High tests and closed for high-impedance to Low tests. High-to-High impedance tests are made to an output voltage of V_{OH} = -0.5V with S_1 open, and Low-to-High impedance tests are made to the V_{OL} = +0.5V level with S_1 closed.

VIRGIN STATE

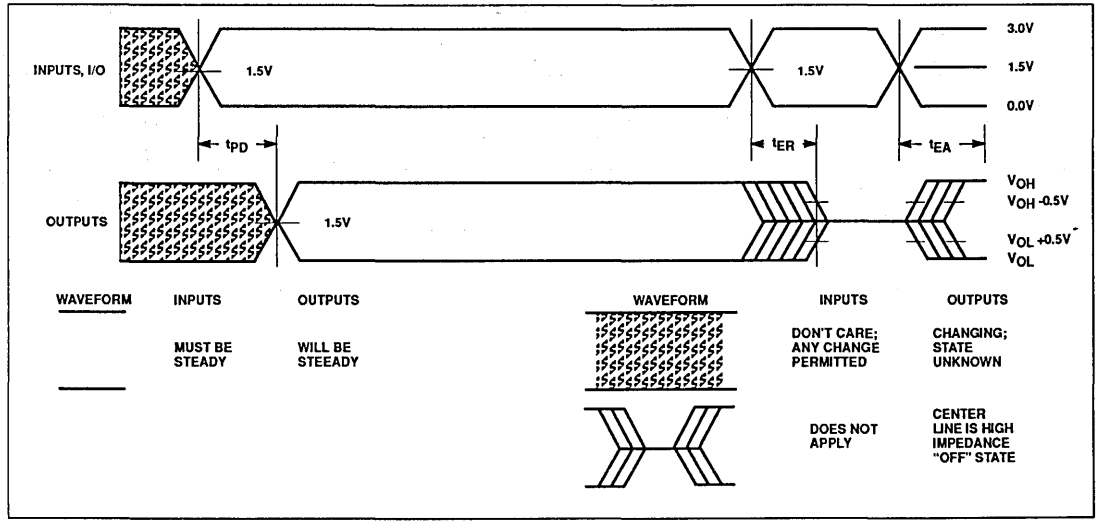
A factory shipped virgin device contains all fusible links open, such that:

1. All outputs are at "H" polarity.
2. All outputs are enabled.
3. All p-terms are enabled.

TIMING DEFINITIONS

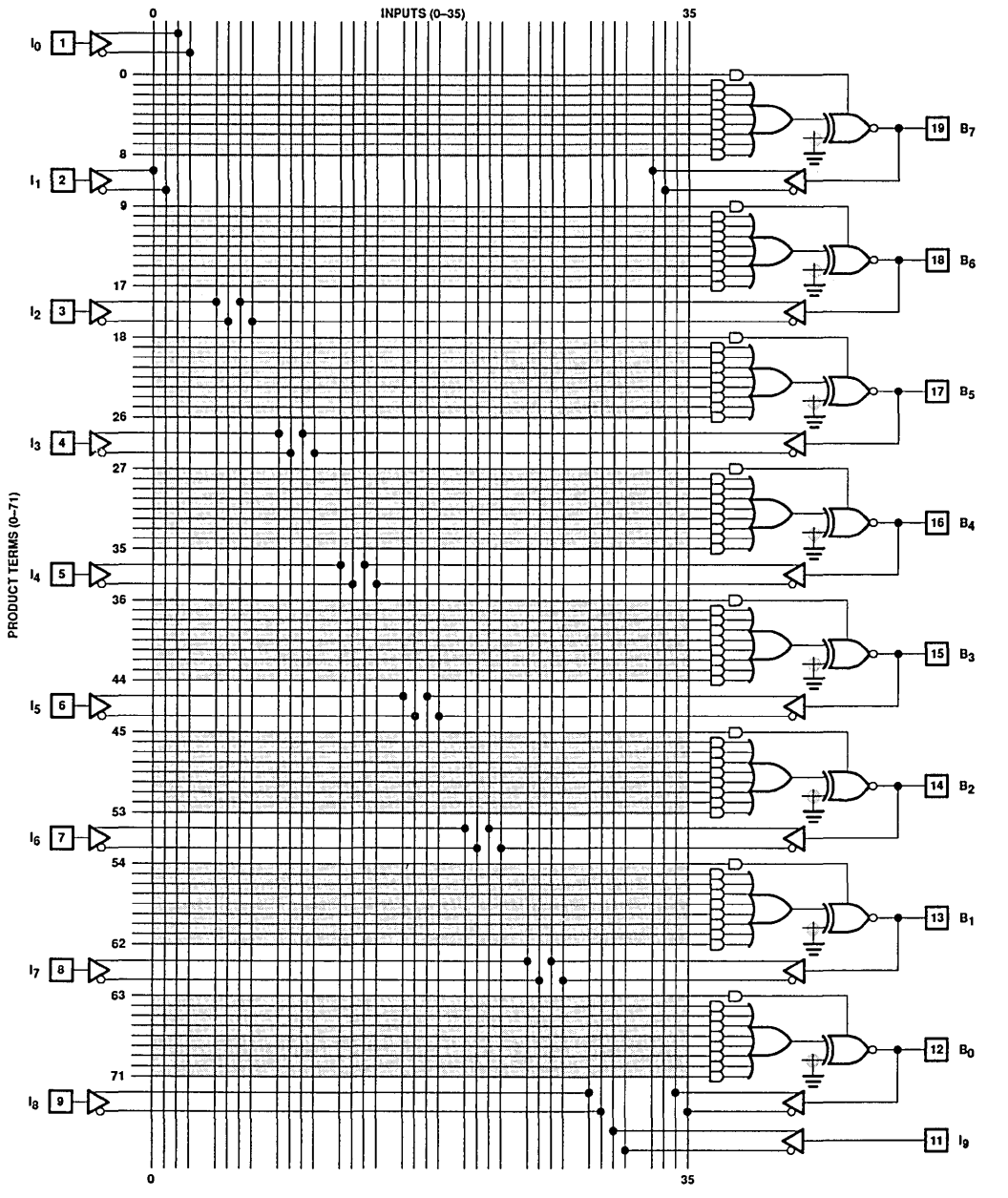
SYMBOL	PARAMETER
t_{PD}	Input to output propagation delay.
t_{ER}	Input to output disable (3-State) delay (Output Disable).
t_{EA}	Input to Output Enable delay (Output Enable).

TIMING DIAGRAM



Programmable AND Array Logic (18 × 72 × 8) — PLHS18P8A

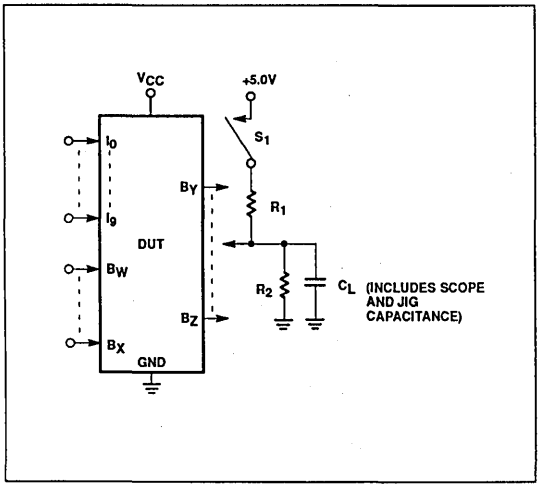
FPLA LOGIC DIAGRAM



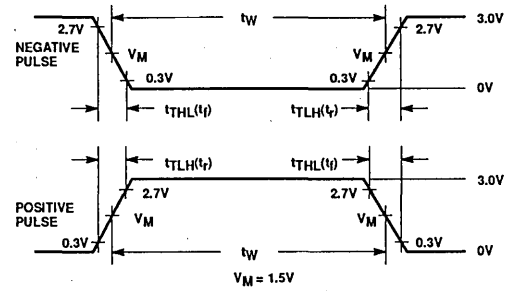
NOTES:
1. All unprogrammed or virgin "AND" gate locations are pulled to logic "1".
2. ◌ Programmable connections.

Programmable AND Array Logic (18 × 72 × 8) PLHS18P8A

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS			
Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1MHz	500ns	≤5ns	≤5ns

Signetics

PLC415
CMOS Programmable Logic Sequencer (17 × 68 × 8)

Military
Customer Specific Products

Preliminary Specification

DESCRIPTION

The PLC415 PLD is a CMOS Programmable Logic Sequencer of the Mealy type. The PLC415 is a pin-for-pin compatible, functional superset of the PLS105 and PLUS405 Bipolar Programmable Logic Sequencer devices.

The PLC415 is ideally suited for high density, power sensitive controller functions. The Power Down feature provides true CMOS standby power levels of less than 100μA. The PLC415 has been designed to accept both CMOS and TTL input levels to facilitate logic integration in almost any system environment.

The PLC415 architecture has been tailored for state machine functions. Both arrays are programmable, thus providing full interconnectability. Any one or all of the 64 AND transition terms can be connected to any (or all) of the 8 buried state and 8 output registers.

Two clock sources enable the design of 2 state machines on one chip. The J-K flip-flops provide the added flexibility of the toggle function which is indeterminate on S-R flip-flops. The programmable Initialization feature supports asynchronous initialization of the state machine to any user defined pattern. Separate INIT functions and Output Enable functions are controllable either from the array or from an external pin.

The unique Complement Array feature supports complex ELSE transition statements with a single product term. The PLC415 has 2 Complement Arrays which allows the user to design two independent complement functions. This is particularly useful if two state machines have been implemented on one chip.

FEATURES

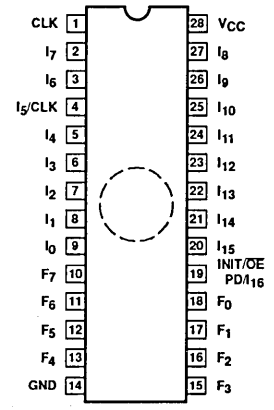
- **Pin-for-Pin compatible, functional superset of PLS105/A and PLUS405 Logic Sequencers**
- **Zero standby power of less than 100μA (worst case)**
  - **Power dissipation at f_{MAX} = 80mA (worst case)**
- **CMOS and TTL compatible**
- **Programmable asynchronous initialization and OE functions**
  - **Controllable from AND Array or external source**
- **17 input variables**
- **8 output functions**
- **68 Product Terms**
  - **64 transition terms**
  - **4 control terms**
- **8-bit State Register**
- **8-bit Output Register**
- **2 Transition Complement Arrays**
- **Multiple clocks**
- **Diagnostic test modes features for access to state and output registers**
- **Power-on preset of all registers to "1"**
- **J-K flip-flops**
  - **Automatic Hold states**
- **Security Fuse**
- **3-State outputs**

APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift Registers**

PIN CONFIGURATIONS

F, FA Package



NOTE:
FA = Ceramic with Quartz window
F = Ceramic OTP

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-Pin Ceramic DIP with window; Reprogrammable (600mil-wide)	PLC415/BXA
28-Pin Ceramic DIP; One-time Programmable (600mil-wide)	PLC415/BXA (OT)

CMOS Programmable Logic Sequencer (17 × 68 × 8) — PLC415

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK1	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers. Pin 1 only clocks P_{0-3} and F_{0-3} if Pin 4 is also being used as a clock.	Active-High (H)
2, 3, 5-9, 26-27 20-22	I_0 - I_4, I_7, I_6 I_8 - I_9 I_{13} - I_{15}	**Logic Inputs:** The 12 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L".	Active-High/Low (H/L)
4	I_5/CLK2	**Logic Input/Clock:** A user programmable function:	
		• **Logic Input:** A 13th external logic input to the AND array, as above.	Active-High/Low (H/L)
		• **Clock:** A 2nd clock for the State Registers P_{4-7} and Output Registers F_{4-7}, as above. Note that input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using Pin 4 as a Clock.	Active-High (H)
23	I_{12}	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I_{12} is held at +11V, device outputs F_0 - F_7 reflect the contents of State Register bits P_0 - P_7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
24	I_{11}	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I_{11} is held at +11V, device outputs F_0 - F_7 become direct inputs for State Register bits P_0 - P_7; a Low-to-High transition on the appropriate clock line loads the values on pins F_0 - F_7 into the State Register bits P_0 - P_7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
25	I_{10}	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL or CMOS levels. When I_{10} is held at +11V, device outputs F_0 - F_7 become direct inputs for Output Register bits Q_0 - Q_7; a Low-to-High transition on the appropriate clock line loads the values on pins F_0 - F_7 into the Output Register bits Q_0 - Q_7. The contents of each State Register remains unaltered.	Active-High/Low (H/L)
10-13 15-18	F_0 - F_7	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs:** Eight device outputs which normally reflect the contents of Output Register Bits Q_0 - Q_7, when enabled. When I_{12} is held at +11V, F_0 - F_7 = (P_0 - P_7). When I_{11} is held at +11V, F_0 - F_7 become inputs to State Register bits P_0 - P_7. When I_{10} is held at +11V, F_0 - F_7 become inputs to Output Register bits Q_0 - Q_7.	Active-High (H)
19	INIT/$\overline{OE}$ I_{16}/PD	**External Initialization, External /OE, PD or I_{16}:** A user programmable function: Only one of the four options below may be selected. Note that both Initialization and /OE options are alternately available via the AND array. (P-terms INA, INB, OEA, and OEB.)	
		• **External Initialization:** Provides an asynchronous Preset to logic "1" or Reset to logic "0" of any or all State and Output Registers, determined individually on a register-by-register basis. INIT overrides the clock, and when held High, clocking is inhibited. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after the INIT pulse goes Low. See timing diagrams for t_{NVCK} and t_{VCK}. Note that if the External Initialization option is selected, I_{16} is disabled automatically via the design software and the Power Down and External OE options are not available. Internal OE is available via P-Terms OEA and/or OEB. This option can be selected for one or both banks of registers.	Active-High (H)
		• **External Output Enable:** Provides an Output Enable/Disable function for Output Registers. Note that if the External OE option is selected, I_{16} is disabled automatically via the design software and the Power Down and External INIT options are not available. Internal INIT is available via P-terms INA and/or INB. This option can be selected for one or both banks of registers.	Active-Low (L)
		• **Power Down:** When invoked, provides a Power Down (zero power) mode. The contents of all Registers is retained, despite the toggling of the Inputs or the clocks. To obtain the lowest possible power level, all Inputs should be static and at CMOS input levels. Note that if the PD options is selected, I_{16} is disabled automatically via the design software and the External INIT and External OE options are not available. Internal INIT is available via P-terms INA and/or INB and Internal OE is available via P-terms OEA and/or OEB.	Active-High (H)
		• **Logic Input:** The 17th external logic input to the AND array as above. Note that when the I_{16} option is selected, the Power Down, External /OE and External INIT are not available. Internal OE and Internal INIT are available from P-Terms OEA/OEB and INA/INB, respectively.	Active-High/Low (H/L)

CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

TRUTH TABLE [1, 2, 3, 4, 5, 6]

V_{CC}	OPTION INIT	OPTION $\overline{OE}$	I_{10}	I_{11}	I_{12}	CK	J	K	Q_P	Q_F	F
	H		X	X	X	X	X	X	H/L	H/L	Q_F
	X		+11V	X	X	↑	X	X	Q_P	L	L
	X		+11V	X	X	↑	X	X	Q_P	H	H
	X		X	+11V	X	↑	X	X	L	Q_F	L
	X		X	+11V	X	↑	X	X	H	Q_F	H
	X		X	X	+11V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
+5V		H	X	X	X	X	X	X	Q_P	Q_F	Hi-Z
		X	+11V	X	X	↑	X	X	Q_P	L	L
		X	+11V	X	X	↑	X	X	Q_P	H	H
		X	X	+11V	X	↑	X	X	L	Q_F	L
		X	X	+11V	X	↑	X	X	H	Q_F	H
		L	X	X	+11V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	L	L	X	X	X	X	X	X	H	H	H

NOTES:

1. Positive Logic:
   S/R (or J/K) = $T_0 + T_1 + T_2 + \ldots T_{63}$
   $T_n = (C_0, C_1)(I_0, I_1, I_2, \ldots)(P_0, P_1 \ldots P_7)$
2. Either Initialization or $\overline{\text{Output Enable}}$ are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. X = Don't Care (≤5.5V)
5. H/L implies that either a High or a Low can occur, depending upon user-programmed Initialization selection (each State and Output Register individually programmable).
6. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

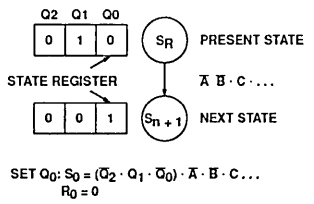
VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:

1. INIT/$\overline{OE}$/PD/I_{16} is set to INIT. In order to use the INIT function, the user must select either the PRESET or the RESET option for each flip-flop. Note that regardless of the user-programmed initialization, or even if the INIT function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are inactive (0).
3. All J/K flip-flop inputs are disabled (0).
4. The Complement Arrays are inactive.
5. Clock 1 is connected to all State and Output Registers.

LOGIC FUNCTION

Typical State Transition:



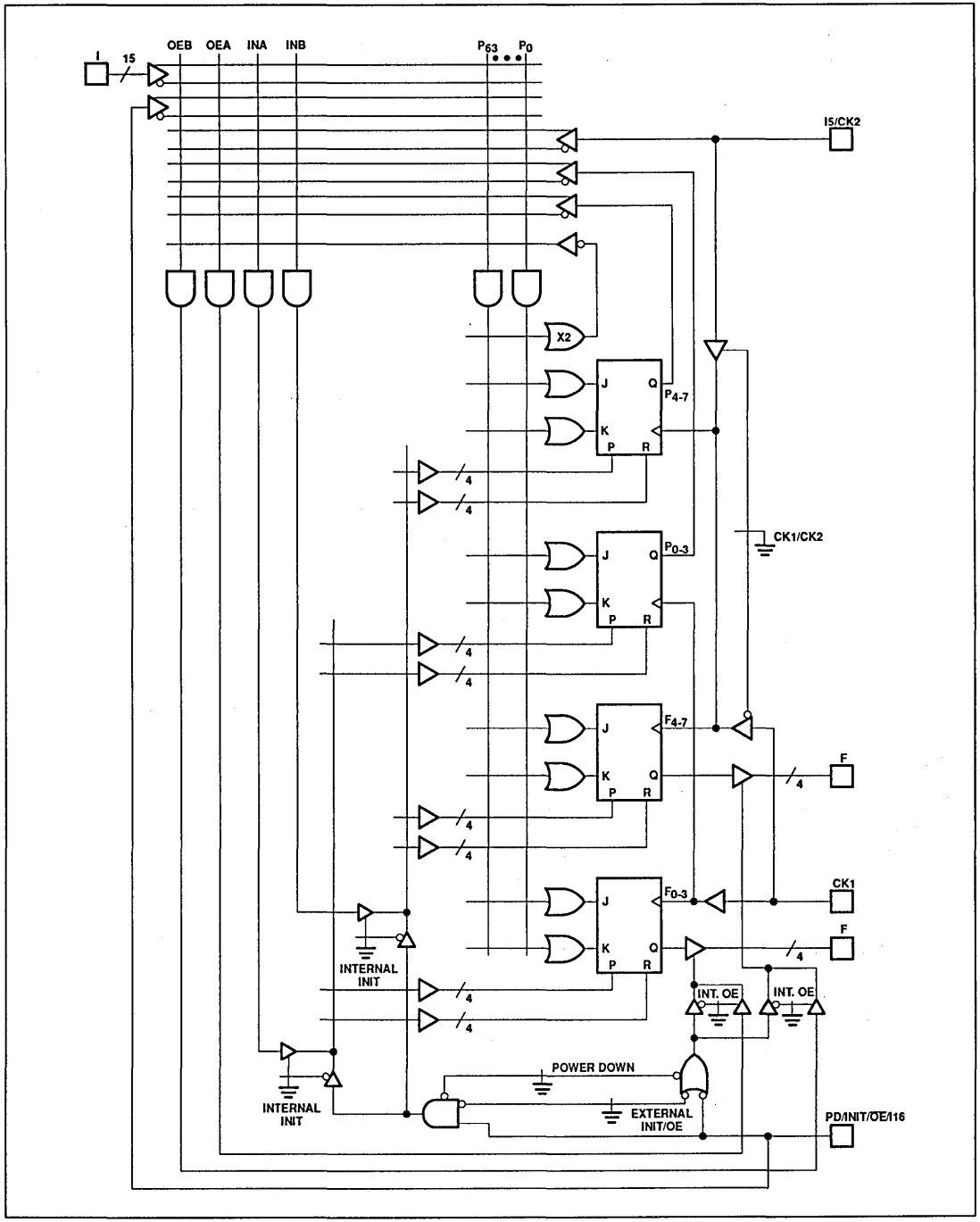
SET Q_0: $S_0 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

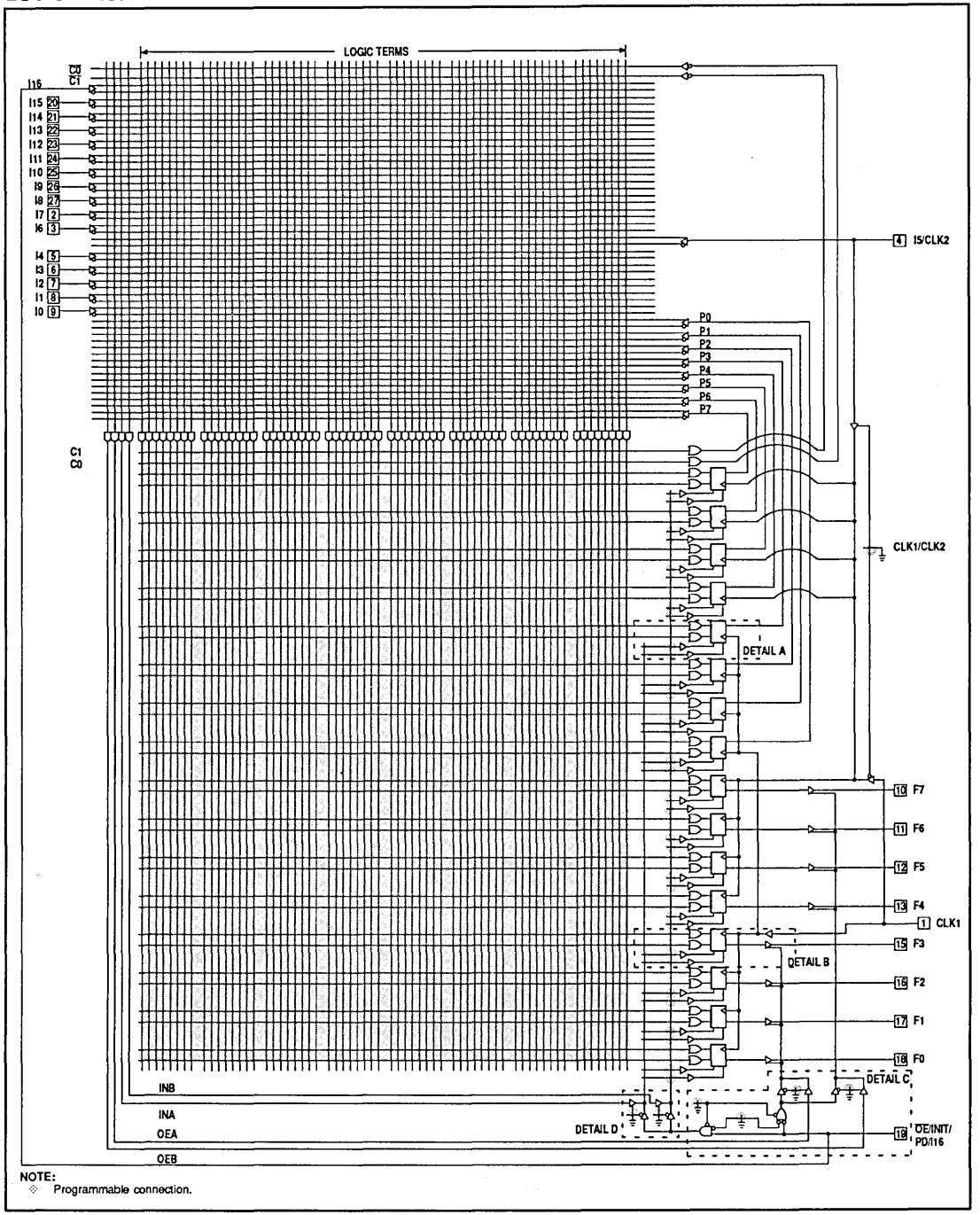
CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

FUNCTIONAL DIAGRAM



CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

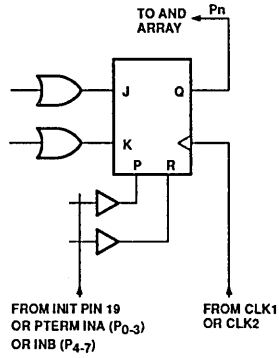
LOGIC DIAGRAM



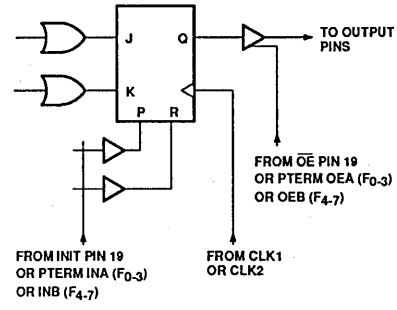
NOTE:
◈ Programmable connection.

CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

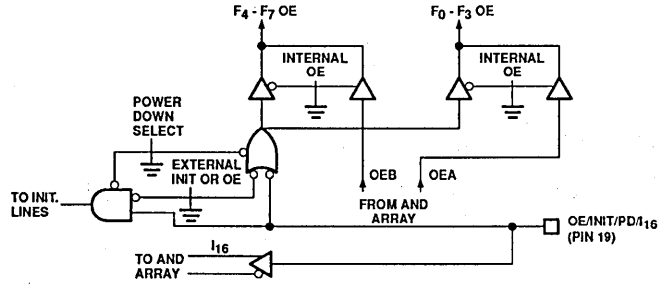
DETAILS FOR PLC415 LOGIC DIAGRAM



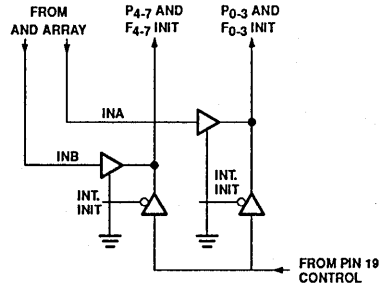
Detail A
State Registers P_0 - P_7



Detail B
Output Registers F_0 - F_7



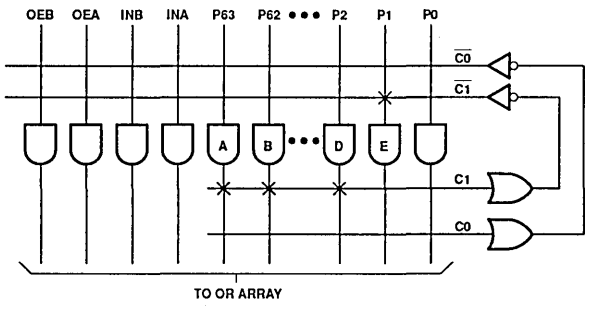
Detail C
Pin 19 Options: $\overline{OE}$, Initialization, Power Down and Input 16



Detail D
Internal and External Initialization

CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

DETAILS FOR PLC415 LOGIC DIAGRAM (Continued)



Complement Array Detail

The Complement Array is a special sequencer feature that is often used for detecting illegal states. It is also ideal for generating IF-THEN-ELSE logic statements with a minimum number of product terms.

The concept is deceptively simple. If you subscribe to the theory that the expressions (/A • /B • /C) and ($\overline{A + B + C}$) are equivalent, you will begin to see the value of this single term NOR array.

The Complement Array is a single OR gate with inputs from the AND array. The output of the Complement Array is inverted and fed back to the AND array (NOR). The output of the array will be Low if any one or more of the AND terms connected to it are active (High). If, however, all the connected terms are inactive (Low), which is a classic unknown state, the output of the Complement Array will be High.

Consider the Product Terms A, B and D that represent defined states. They are also connected to the input of the Complement Array. When the condition (not A and not B and not D) exists, the Complement Array will detect this and propagate an Active-High signal to the AND array. This signal can be connected to Product Term E, which could be used in turn to reset the state machine to a known state. Without the Complement Array, one would have to generate product terms for all unknown or illegal states. With very complex state machines, this approach can be prohibitive, both in terms of time and wasted resources.

Note that the PLC415 has 2 Complement Arrays which allow the user to design 2 independent Complement functions. This is particularly useful if 2 independent state machines have been implemented on one device.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OUT}	Output voltage	+5.5	V_{DC}
I_{IN}	Input currents	-30 to +30	mA
I_{OUT}	Output currents	+100	mA
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

NOTE:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITION		LIMITS			UNIT
				Min	Typ[1]	Max	
Input voltage[2]							
V_{IL}	Low	V_{CC} = Min		-0.3		0.8	V
V_{IH}	High	V_{CC} = Max		2.0		V_{CC} + 0.3	V
Output voltage[2]							
V_{OL}	Low	V_{CC} = Min, I_{OL} = 16mA				0.5	V
V_{OH}	High	I_{OH} = -3.2mA		2.4			V
Input current							
I_{IL}	Low	V_{IN} = GND				-10	µA
I_{IH}	High	V_{IN} = V_{CC}				10	µA
Output current							
$I_{O(OFF)}$	Hi-Z state	V_{OUT} = V_{CC} V_{OUT} = GND				10 -10	µA µA
I_{OS}	Short-circuit[3, 6]	V_{OUT} = GND				-130	mA
I_{CCSB}	V_{CC} supply current with PD asserted[7]	V_{CC} = Max, V_{IN} = 0 or V_{CC}			50	100	µA
I_{CC}	V_{CC} supply current Active[4, 5]	I_{OUT} = 0mA	at f = 1MHz			60	mA
	(TTL or CMOS Inputs)	V_{CC} = Max	at f = Max			90	mA
Capacitance							
C_I	Input	V_{CC} = 5V, V_{IN} = 2.0V			12	17	pF
C_B	I/O	V_B = 2.0V			15	20	pF

NOTES:
1. All typical values are at V_{CC} = 5V. T_A = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Duration of short-circuit should not exceed one second. Test one at a time.
4. Tested with TTL input levels: V_{IL} = 0.45V, V_{IH} = 2.4V. Measured with all inputs and outputs switching.
5. Refer to Figure 1, I_{CC} vs Frequency (worst case).
6. Refer to Figure 2 for Δt_{PD} vs output capacitance loading.
7. The outputs are automatically 3-Stated when the device is in the Power Down mode. To achieve the lowest possible current, the inputs and clocks should be at CMOS static levels.

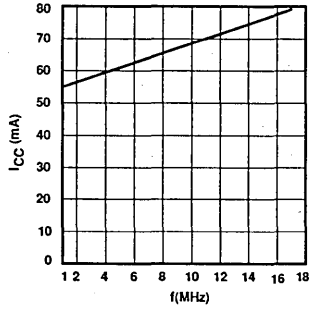


Figure 1. I_{CC} vs Frequency (Worst Case)

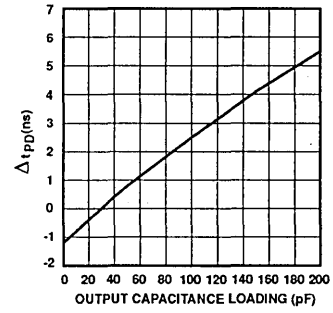


Figure 2. Δt_{PD} vs Output Capacitance Loading (Typical)

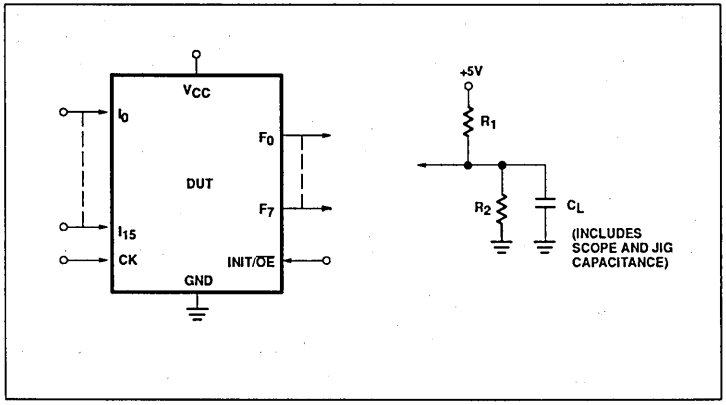
CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

AC ELECTRICAL CHARACTERISTICS $R_1 = 252\Omega$, $R_2 = 178\Omega$, $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

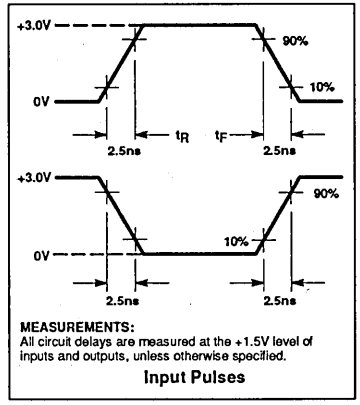
SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS			UNIT
					Min	Typ	Max	
Pulse width								
t_{CKH}	Clock High	CK+	CK-	30pF	25	10		ns
t_{CKL}	Clock Low	CK-	CK+	30pF	25	10		ns
t_{INITH}	Initialization Input pulse	INIT+	INIT-	30pF	20			ns
Set-up time								
t_{IS1}	Input	(I) +/-	CK+	30pF	45	25		ns
t_{IS2}[1]	Input through Complement array	(I) +/-	CK+	30pF	65	40		ns
t_{ISPD}	Power Down Setup (from PD pin)	PD+	CK+	30pF	38	15		ns
t_{ISPU}	Power Up Setup (from PD pin)	PD-	First Valid CK+	30pF	38	30		ns
t_{VS}[1]	Power on Preset Setup	V_{CC}+	CK-	30pF	0			ns
t_{VCK1}	Clock resume (after INIT) when using INIT pin (pin 19)	INIT-	CK-	30pF	10	-5		ns
t_{VCK2}[1]	Clock resume (after INIT) when using P-term INIT (from AND array)	(I) +/-	CK-	30pF	20	8		ns
t_{NVCK1}	Clock lockout (before INIT) when using INIT pin (pin 19)	CK-	INIT-	30pF	10	-3		ns
t_{NVCK2}[1]	Clock lockout (before INIT) when using P-term INIT (from AND array)	CK-	INIT-	30pF	0	-5		ns
Propagation delays								
t_{CKO}	Clock to Output	CK+	(F) +/-	30pF		15	30	ns
t_{PDZ}	Power Down to outputs off	PD+	Outputs Off	5pF		25	35	ns
t_{PUA1}	Power Up to outputs Active with dedicated Output Enable	PD-	Outputs Active	30pF		20	40	ns
t_{PUA2}[1]	Power Up to outputs Active with P-term Output Enable[1]	PD-	Outputs Active	30pF		37	60	ns
t_{IHPU}	Last valid clock to Power Down delay (Hold)	Last Valid Clock	PD+	30pF	25	15		ns
t_{IHPD}	First valid clock cycle before Power Up	Beginning of First Valid Clock Cycle	PD-	30pF	0	-25		ns
t_{OE1}	Output Enable: from /OE pin	OE-	Output Enabled	30pF		15	30	ns
t_{OE2}[1]	Output Enable; from P-term	(I) +/-	Output Enabled	30pF		25	40	ns
t_{OD1}	Output Disable; from /OE pin	OE+	Output Disabled	5pF		20	30	ns
t_{OD2}	Output Disable; from P-term	(I) +/-	Output Disabled	5pF		30	40	ns
t_{INIT1}	INIT to output when using INIT pin	INIT+	(F) +/-	30pF		22	35	ns
t_{INIT2}	INIT to output when using P-term INIT	(I) +/-	(F) +/-	30pF		35	45	ns
t_{PPR}[1]	Power-on Preset (F_n = 1)	V_{CC} +	(F) +	30pF			15	ns
t_{CKP1}	Registered operating period; ($t_{IS1} + t_{CKO1}$)	(I) +/-	(F) +/-	30pF		40	60	ns
t_{CKP2}[1]	Registered operating period with Complement Array ($t_{IS2} + t_{CKO1}$)	(I) +/-	(F) +/-	30pF		55	75	ns
Hold time								
t_{IH}	Input Hold	CK+	(F) +/-	30pF		-10	0	ns
Frequency of operation								
f_{CLK}	Clock (toggle) frequency	C+	C+	30pF	15	45		MHz
f_{MAX1}	Registered operating frequency ($t_{IS1} + t_{CKO1}$)	(I) +/-	(F) +/-	30pF	13.3	22		MHz
f_{MAX2}	Registered operating frequency with Complement Array ($t_{IS2} + t_{CKO1}$)	(I) +/-	(F) +/-	30pF	11.9	16.4		MHz

CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

TEST LOAD CIRCUIT



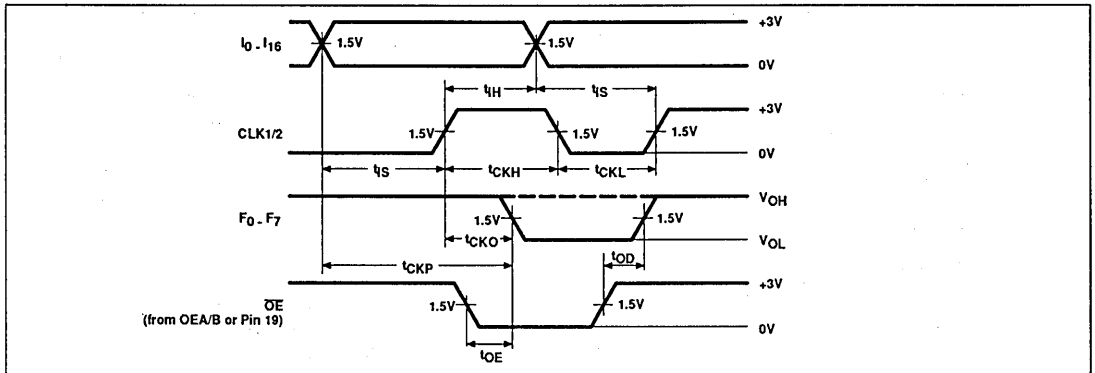
VOLTAGE WAVEFORMS



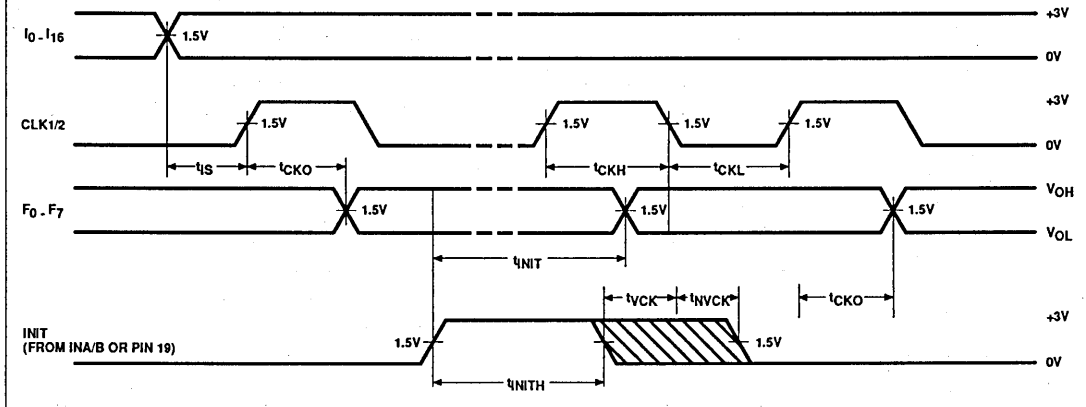
MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TIMING DIAGRAMS



Sequential Mode

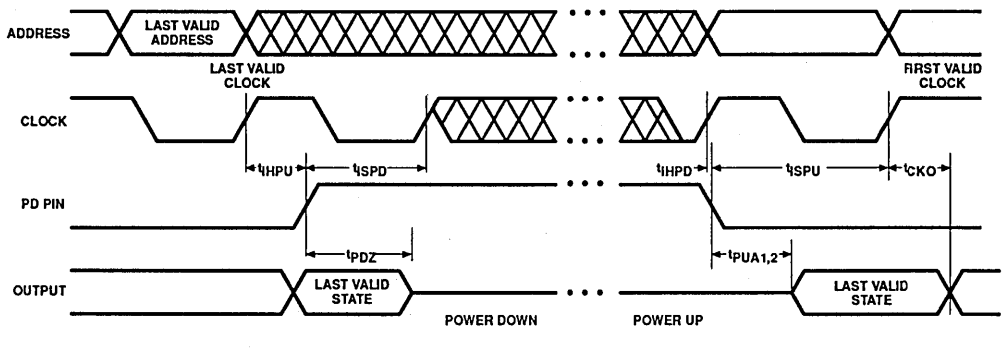


Asynchronous Initialization

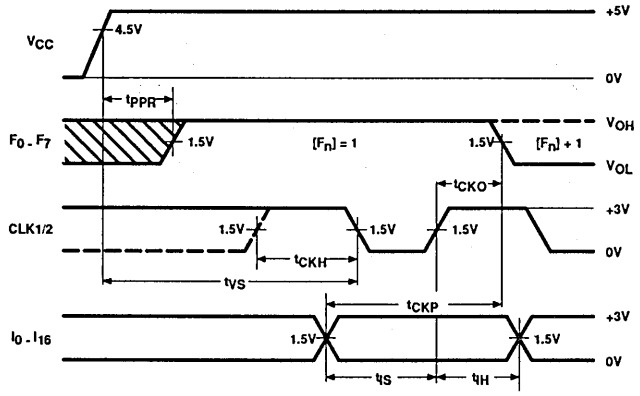
CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

The PLC415 has a unique power down feature that is ideal for power sensitive controller and state machine applications. During idle periods, the PLC415 can be powered down to a near zero power consumption level of less than 100 micro Amps. Externally controlled from Pin 19, the power down sequence first saves the data in all the State and Output registers. In order to insure that the last valid states are saved, there are certain hold times associated with the first and last valid clock edges and the Power Down input pulse. The Outputs are then automatically 3-Stated and power consumption is reduced to a minimum. Once in the power down mode, any or all of the inputs, including the clocks, may be toggled without the loss of data. To obtain the lowest possible power level, the inputs should be at static CMOS input levels during the power down period.

TIMING DIAGRAMS (Continued)



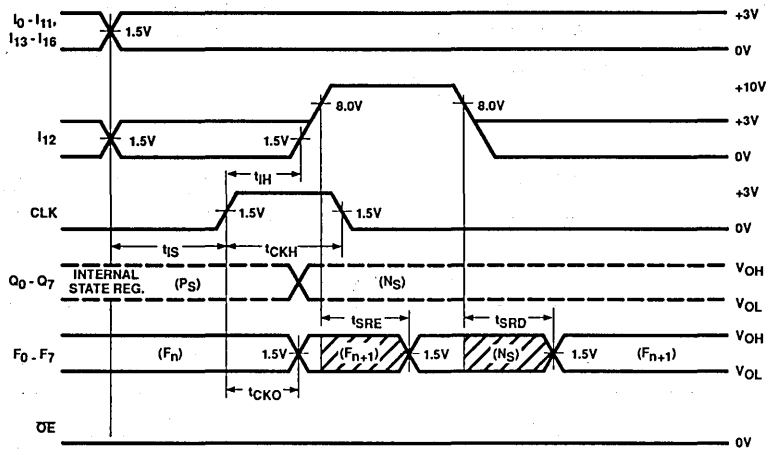
Power Down Enable and Disable



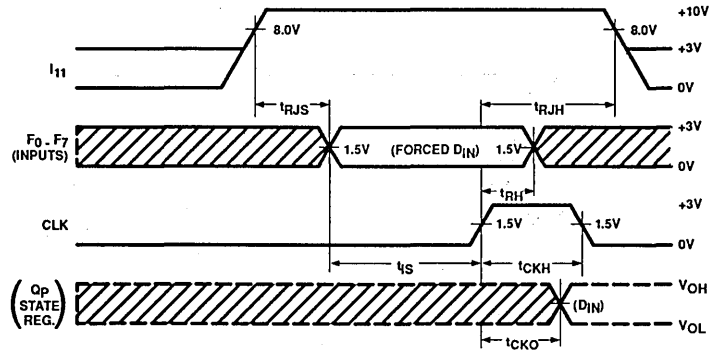
Power-On Preset

CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

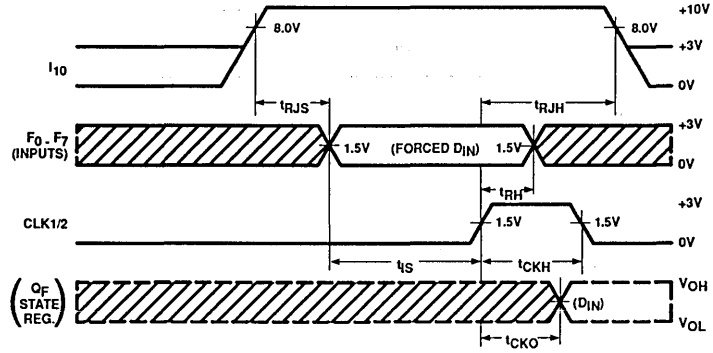
TIMING DIAGRAMS (Continued)



Diagnostic Mode—State Register Outputs



Diagnostic Mode—State Register Input Jam



Diagnostic Mode—Output Register Input Jam

CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

TIMING DEFINITIONS

SYMBOL	PARAMETER
f_{CLK}	Minimum guaranteed toggle frequency of the clock (from Clock High to Clock High).
$f_{MAX1,2}$	Minimum guaranteed operating frequency.
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP1}	Minimum guaranteed operating period - when not using Complement Array.
t_{CKP2}	Minimum guaranteed operating period - when using Complement Array.
t_{CKO}	Delay between positive transition of Clock and when Outputs become valid (with outputs enabled).
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{IHPD}	Required delay between the positive transition of the beginning of the first valid clock cycle to the beginning of Power Down Low to insure that the last valid states are intact and that the next positive transition of the clock is valid.
t_{IHPU}	Required delay between the positive transition of the last valid clock and the beginning of Power Down High to insure that last valid states are saved.
t_{INITH}	Width of initialization input pulse.
t_{INIT1}	Delay between positive transition of Initialization and when Outputs become valid when using external INIT control (from pin 19).
t_{INIT2}	Delay between positive transition of Initialization and when outputs become valid when using internal INIT control (from P-terms INA and INB).
t_{ISPD}	Required delay between the beginning of Power Down High (from pin 19) and the positive transition of the next clock to insure that the clock edge is not detected as a valid Clock and that the last valid states are saved.

SYMBOL	PARAMETER
t_{ISPU}	Required delay between the beginning of Power Down Low and the positive transition of the first valid clock.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
t_{IS2}	Required delay between beginning of valid input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{NVCK1}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization when using external INIT control (from pin 19) to guarantee that the clock edge is not detected as a valid negative transition.
t_{NVCK2}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization, when using the internal INIT control (from P-terms INA and INB), to guarantee that the clock edge is not detected as a valid negative transition.
t_{OD1}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state, when using external OE control (from pin 19).
t_{OD2}	Delay between beginning of Output Enable High and when outputs are in the OFF-State when using internal OE control (from P-terms OEA and OEB).
t_{OE1}	Delay between beginning of Output Enable Low and when Outputs become valid when using external OE control from pin 19.
t_{OE2}	Delay between beginning of Output Enable Low and when outputs become valid when using internal OE control (from P-terms OEA and OEB).
t_{PDZ}	Delay between beginning of Power Down High and when outputs are in OFF-State and the circuit is "powered down".

SYMBOL	PARAMETER
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
$t_{PUA1,2}$	Delay between beginning of Power Down Low and when outputs become Active (valid) and the circuit is "powered up". See AC Specifications.
t_{RH}	Required delay between positive transition of Clock and end of valid Input data when jamming data into State or Output Registers in diagnostic mode.
t_{RJH}	Required delay between positive transition of Clock and end of inputs I_{11} or I_{10} transition to State and Output Register Input Jam Diagnostic Modes, respectively.
t_{RJS}	Required delay between when inputs I_{11} or I_{10} transition to State and Output Register Input Jam Diagnostic Modes, respectively, and when the output pins become available as inputs.
t_{SRD}	Delay between input I_{12} transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{SRE}	Delay between input I_{12} transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{VCK1}	Required delay between negative transition of Asynchronous Initialization and negative transition of Clock preceding the first valid clock pulse when using external INIT control (pin 19).
t_{VCK2}	Required delay between the negative transition of the Asynchronous Initialization and the negative transition of the clock preceding the first valid clock pulse when using internal INIT control (from P-terms INA and INB).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.

CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

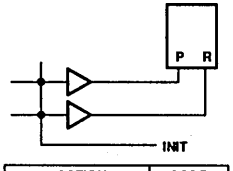
LOGIC PROGRAMMING

PLC415 logic designs can be generated using Signetics AMAZE design software or several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry format is accepted. Schematic capture entry formats are also supported.

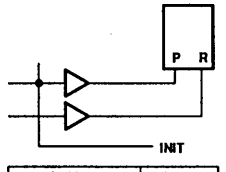
PLC415 logic designs can also be generated using the program table format detailed on the following page(s). This Program Table Entry format (PTE) is supported by the Signetics AMAZE PLD design software. AMAZE is available free of charge to qualified users.

To implement the desired logic functions, each logic variable (I, B, P, S, T, etc.) from the logic equations if assigned a symbol. TRUE, COMPLEMENT, PRESET, RESET, OUTPUT ENABLE, INACTIVE, etc., symbols are defined below.

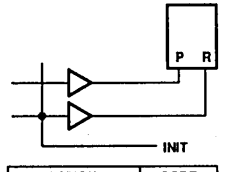
INITIALIZATION (PRESET/RESET)[11] OPTION - (P/R)



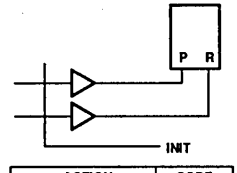
ACTION	CODE
INDETERMINATE[1,4,9]	0



ACTION	CODE
PRESET[9]	H

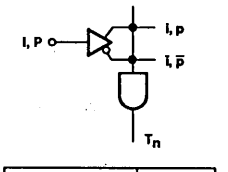


ACTION	CODE
RESET[9]	L

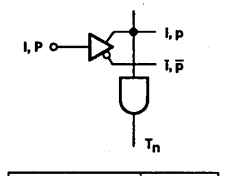


ACTION	CODE
NO INIT FUNCTION[4,9]	-

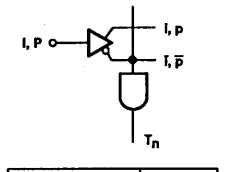
"AND" ARRAY - (I), (P)



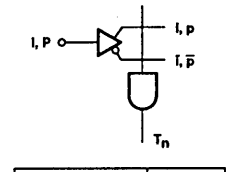
STATE	CODE
INACTIVE[1, 2]	0



STATE	CODE
I, P	H



STATE	CODE
Ī, P̄	L



STATE	CODE
DON'T CARE	-

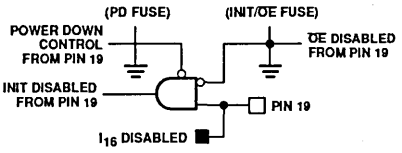
Notes are on page 872.

CMOS Programmable Logic Sequencer (17 × 68 × 8) — PLC415

LOGIC PROGRAMMING (Continued)

PIN 19 FUNCTION: POWER DOWN, INITALIZATION, $\overline{OE}$, OR INPUT

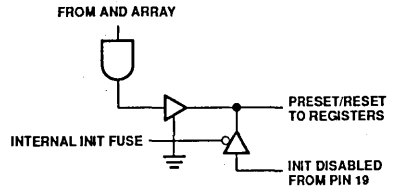
Power Down Mode



POWER DOWN FUSE	CODE
PIN 19 AS POWER DOWN	H[6]

EXTERNAL INIT/$\overline{OE}$ FUSE	CODE
EXTERNAL INIT/$\overline{OE}$ DISABLED	L

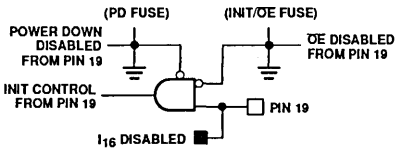
P-Term Initialization Control



INTERNAL INIT FUSES	CODE
P-TERM INIT CONTROL	H[7, 8]

POWER DOWN FUSE	CODE
POWER DOWN ENABLED OR DISABLED	H OR L

External Initialization Control

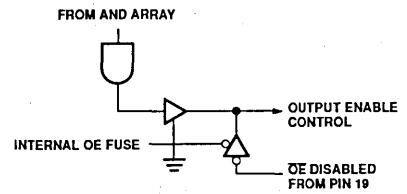


PD FUSE	CODE
POWER DOWN DISABLED	L[1]

EXTERNAL INIT/$\overline{OE}$ FUSE	CODE
PIN 19 AS EXTERNAL INIT	L[1]

INTERNAL INIT FUSES	CODE
P-TERM INIT ACTIVE OR INACTIVE	H OR L[7, 8]

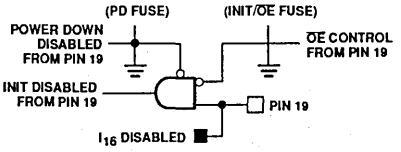
P-Term OE Control



INTERNAL OE FUSES	CODE
P-TERM OE CONTROL	H[7, 8]

POWER DOWN FUSE	CODE
POWER DOWN ENABLED OR DISABLED	H OR L

External Output Enable Control



PD FUSE	CODE
POWER DOWN DISABLED	L

EXTERNAL INIT/$\overline{OE}$ FUSE	CODE
PIN 19 AS EXTERNAL $\overline{OE}$	H

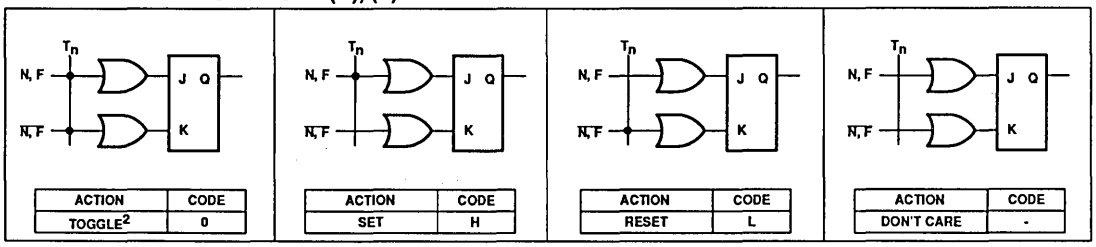
INTERNAL INIT FUSES	CODE
P-TERM $\overline{OE}$ ACTIVE OR INACTIVE	H OR L[7, 8]

Notes are on page 872.

CMOS Programmable Logic Sequencer (17 × 68 × 8) — PLC415

LOGIC PROGRAMMING (Continued)

"OR" ARRAY - J-K FUNCTION - (N), (F)



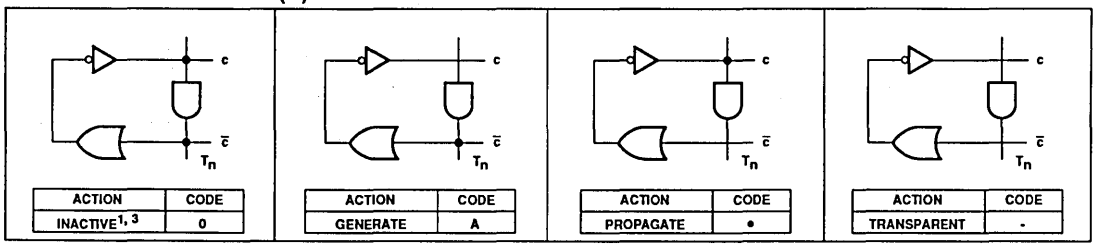
ACTION	CODE
TOGGLE[2]	0

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
DON'T CARE	-

"COMPLEMENT" ARRAY - (C)



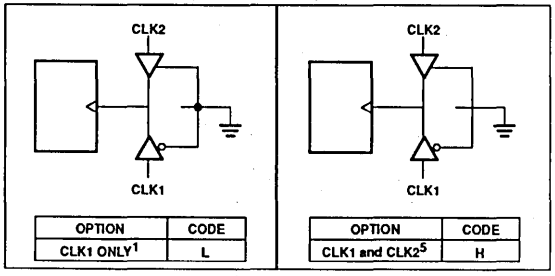
ACTION	CODE
INACTIVE[1, 3]	0

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	-

CLOCK OPTION - (CLK1/CLK2)



OPTION	CODE
CLK1 ONLY[1]	L

OPTION	CODE
CLK1 and CLK2[5]	H

NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs is left intact.
3. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.
4. These states are not allowed when using PRESET/RESET option.
5. Input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using second clock option.
6. When using Power Down feature, INPUT 16 is automatically disabled via the design software.
7. If the internal (P-term) control fuse for INIT and/or OE is programmed as Active High, the associated External Control function will be permanently disabled, regardless of the state of the External INIT/OE fuse.
8. One internal control fuse exists for each group of 8 registers. P_{0-3} and F_{0-3} are banked together in one group, as are P_{4-7} and F_{4-7}. Control can be split between the INIT/OE pin (Pin 19) and P-terms INA, INB, OEA and OEB.
9. The PLC415 also has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.
10. L = cell unprogrammed.
    H = cell programmed.
11. Inputs 10, 11 and 12 (pins 25, 24, & 23) can be used for supervoltage diagnostic mode tests. It is recommended that these inputs not be connected to product terms INA, INB, OEA or OEB if you intend to make use of the diagnostic modes due to the fact that the patterns associated with the internal INIT and OE control product terms may interfere with the diagnostic mode data loading and reading.

CMOS Programmable Logic Sequencer (17 × 68 × 8) — PLC415

PROGRAM TABLE

AND

(Im, Ps)		(Cn)	
INACTIVE	O	INACTIVE	O
I, P	H	GENERATE	A
$\bar{I}$, $\bar{P}$	L	PROPAGATE	•
DON'T CARE	–	TRANSPARENT	–

OR (Ns, Fn)

TOGGLE	O
SET	H
RESET	L
NO CHANGE	–

OPTIONS

ENTERNAL INIT	L
EXTERNAL OE	H
INTERNAL INIT/OE ENABLED	H
INTERNAL INIT/OE DISABLED	L
POWER DOWN ENABLED	H
POWER DOWN DISABLED	L
CLOCK 1 ONLY	L
CLOCK 1 AND 2	H

INITIALIZATION	
PRESET	H
RESET	L
NO INIT	–
INDETERMINATE	O

PROJECT NAME _____ DATE _____ REVISION _____

CUSTOMER NAME _____ SIGNETICS PART # _____ CUSTOMER PART # _____

TERMS	COMP. ARRAY	INTERNAL INIT INB	INTERNAL INIT INA	INTERNAL OE OEB	INTERNAL OE OEA	EXTERNAL INIT/OE	CLK 1/1&2	PD	INITIALIZATION
	NOR	AND							OR
	Cn	INPUT (Im)						PRESENT STATE (Ps)	NEXT STATE (Ns) / OUTPUT (Fn)
	C1 C0	I6 I5 I4 I3 I2 I1 I0						P7 P6 P5 P4 P3 P2 P1 P0	N7 N6 N5 N4 N3 N2 N1 N0 F7 F6 F5 F4 F3 F2 F1 F0
0									
1									
2									
3									
4									
5									
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62									
63									
INB									
OEB									
INA									
OEA									
PIN NO.		19 20 21 22 23 24 25 26 27 2 3 4 5 6 7 8 9							10 11 12 13 15 16 17 18
PIN LABELS									

NOTES:
1. In the unprogrammed state all cells are conducting. Thus, the program table for an unprogrammed device would contain "0"s for all product terms (inactive) and initialization states (indeterminate). The default or unprogrammed state of all other options is "L".
2. Unused Cn, Im and Ps cells are normally programmed as Don't Care (–).
3. Unused product terms can be left blank (inactive) for future code modification.

CMOS Programmable Logic Sequencer (17 × 68 × 8) PLC415

ERASURE CHARACTERISTICS (For Quartz Window Packages Only)

The erasure characteristics of the PLC415 Series devices are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps has wavelengths in the 3000 - 4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical PLC415 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the PLC415 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the PLC415 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15Wsec/cm^2. The erasure time with this dosage is approximately 30 to 35 minutes using an ultraviolet lamp with a 12,000μW/cm^2 power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a CMOS EPLD can be exposed to without damage is 7258Wsec/cm^2 (1 week @ 12000μW/cm^2). Exposure of these CMOS EPLDs to high intensity UV light for longer periods may cause permanent damage.

The maximum number of guaranteed erase/write cycles is 50. Data retention exceeds 20 years.

Signetics

PLHS473

Field-Programmable Logic Array ($20 \times 24 \times 11$)

Signetics Programmable Logic

Product Specification

Military Application Specific Products

DESCRIPTION

The PLHS473 is a two level logic device consisting of 24 AND gates and 22 OR gates with fusible link connections for programming I/O polarity and direction. The Signetics state-of-the-art Oxide-Isolated Bipolar process is used to produce performance not yet achieved in devices of this complexity.

All AND gates are linked to 11 input pins, 9 bidirectional I/O pins, and 2 dedicated output pins. The bidirectional pins are controlled via the OR array. Using these features, the PLHS473 can be configured with up to 20 inputs and as many as 11 outputs.

The AND array input buffers provide both the True and Complement of the inputs (I_X) and the bidirectional signals (B_X) as programmable connections to the AND gates. All 24 AND gates can then be optionally linked to all 22 OR gates (a feature known as Product Term sharing not found in PALs® or most macrocell architectures). The OR array drives 11 output buffers which can be programmed as Active-High for AND-OR functions or Active-Low for AND-NOR functions. In addition, the I/O configuration of each bidirectional pin is individually controlled by a sum-of-products (AND-OR) function which may also contain any of the 24 AND gate outputs. This allows dynamic I/O configuration of all 9 bidirectional pins.

The PLHS473 contains two new features of significance. A code verification lock has been incorporated to improve user security. The addition of three test columns and one test row enables the user to test the device in an unprogrammed state.

The PLHS473 is field programmable using Vertical Avalanche Migration Programmed (VAMP™) fuses to program the cells. This enables the generation of custom logic patterns using standard programming equipment..

FEATURES

- **Field-Programmable**
- **11 dedicated inputs**
- **2 dedicated outputs**
- **9 bidirectional I/O lines**
- **24 product terms**
- **22 OR gates**
- **I/O direction decoded in OR array**
- **Output Enable decoded in OR array**
- **I/O propagation delay: 20ns (max)**
- **Input loading: -100μA (max)**
- **Power dissipation: 700mW (typ)**
- **Security fuse**
- **Testable in unprogrammed state**
- **Programmable as 3-state or Open-Collector outputs**
- **TTL compatible**

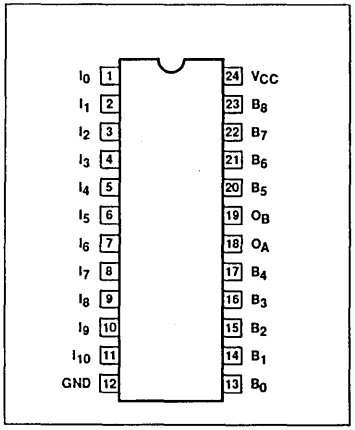
APPLICATIONS

- **Random logic**
- **Code converters**
- **Fault detectors**
- **Function generators**
- **Address mapping**
- **Multiplexing**

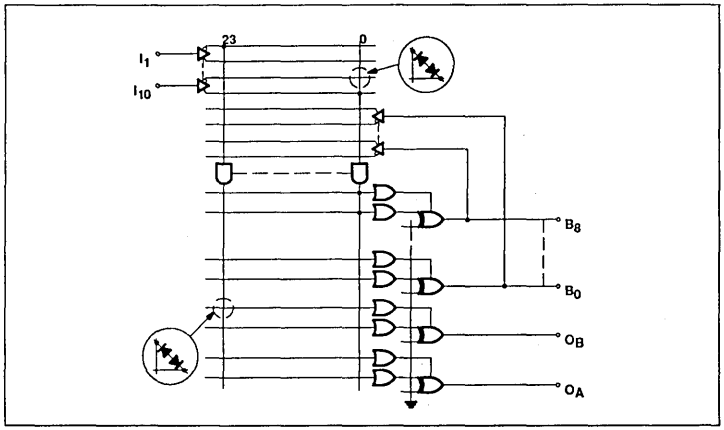
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Ceramic DIP 300mil-wide	PLHS473/BLA

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



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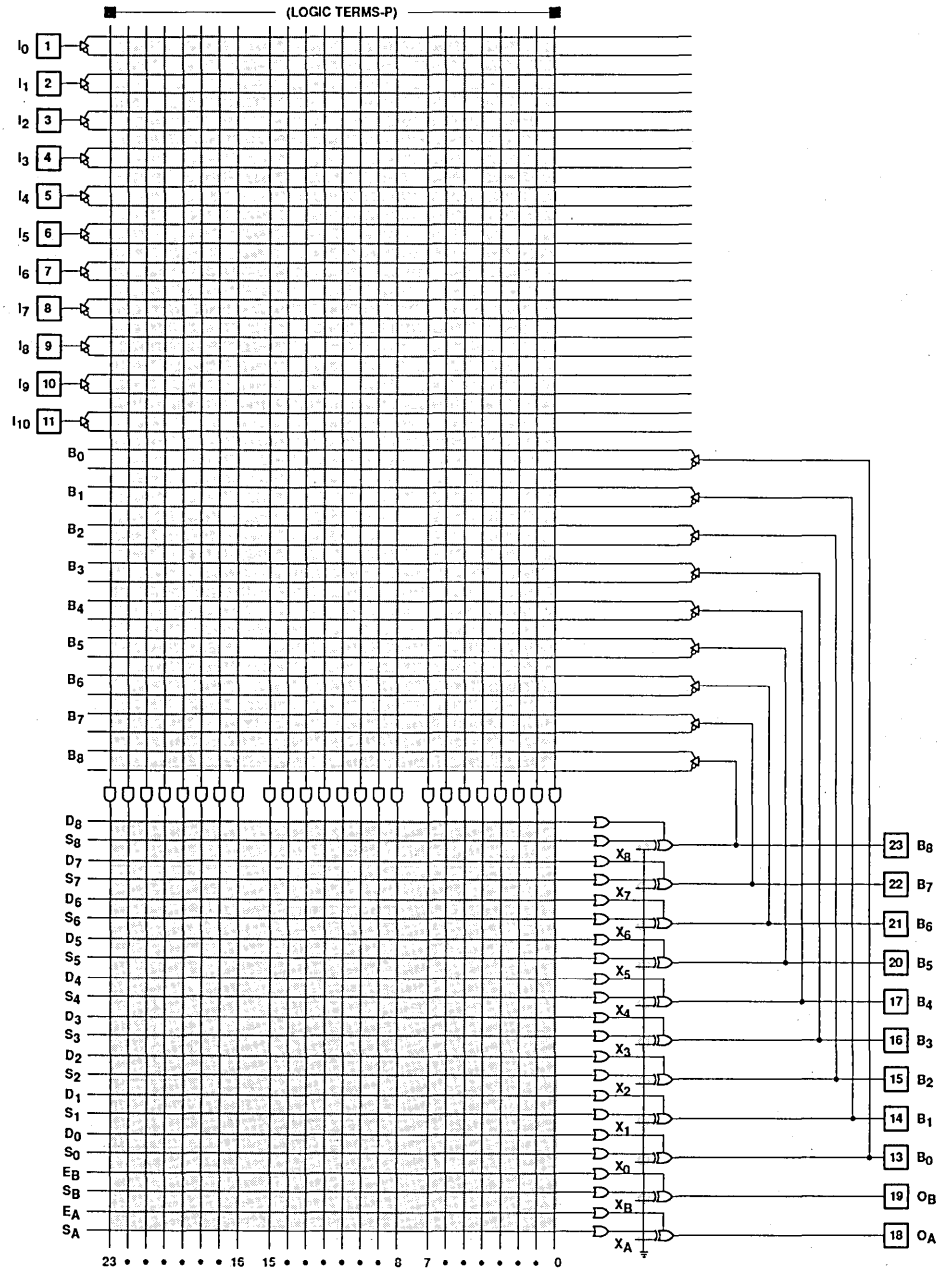
Field-Programmable Logic Array (20 × 24 × 11) PLHS473

FPLA LOGIC DIAGRAM



NOTES:
1. All unprogrammed or virgin 'AND' gate locations are pulled to logic "1".
2. All unprogrammed or virgin 'OR' gate locations are pulled to logic "0".
3. ● Programmable connection.

Field-Programmable Logic Array (20 × 24 × 11) PLHS473

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{STG}	Storage temperature range	-65	+150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}[12]	High level input voltage	2.2			V
V_{IL}[12]	Low level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High level output current			-2	mA
I_{OL}	Low level output current			15	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{IK}	Input clamp voltage[3,4]	V_{CC} = Min, I_{IN} = I_{IK}		-0.8	-1.2	V
		V_{CC} = Min, V_{IL} = Max, V_{IH} = Min				
V_{OL}	Output Low voltage[3,5]	I_{OL} = Max			0.5	V
V_{OH}	Output High voltage[3,6]	I_{OH} = Min	2.4			V
		V_{CC} = Max				
I_{IL}	Input Low current	V_{IN} = 0.45V			-100	µA
I_{IH}	Input High current	V_{IN} = 5.5V			40	µA
I_{OHZ}	Output Tri-state current[10]	V_{CC} = Max, V_{OUT} = 5.5V			40	µA
I_{OLZ}	Output Tri-state current[10]	V_{CC} = Max, V_{OUT} = 0.45V			-100	µA
I_{OS}	Output short circuit[4,6,7]	V_{CC} = Max, V_{OUT} = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		140	155	mA
		V_{CC} = 5V				
I_{IN}	Input capacitance[11]	V_{IN} = 2.0V		8	12	pF
C_B	I/O capacitance[11]	V_B = 2.0V		15	19	pF

Field-Programmable Logic Array (20 × 24 × 11) — PLHS473

AC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

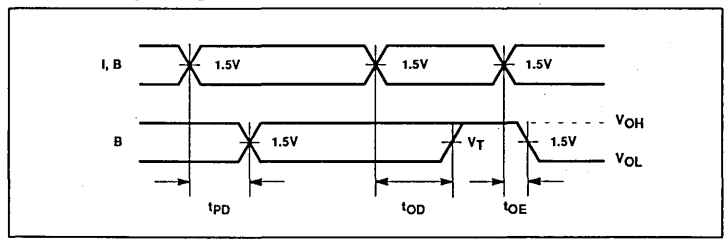
SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_{PD}	Propagation delay	Output±	Input±	C_L = 50pF		25	30	ns
t_{OE}	Output enable	Output-	Input±	C_L = 50pF		25	30	ns
t_{OD}	Output disable[9,11]	Output+	Input±	C_L = 5pF		25	30	ns

NOTES:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with Pins 1 - 5 = 0V, Pins 6, 8 = 4.5V, and Pins 7, 9 - 11 = 10V.
6. Same conditions as Note 5, except Pin 9 = 4.5V.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with all inputs and bidirectional pins at 4.5V. Part in Virgin State.
9. Measured at $V_T = V_{OL} + 0.5V$, and with C_L = 30pF.
10. Leakage values are a combination of input and output leakage.
11. Guaranteed, but not tested.
12. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.

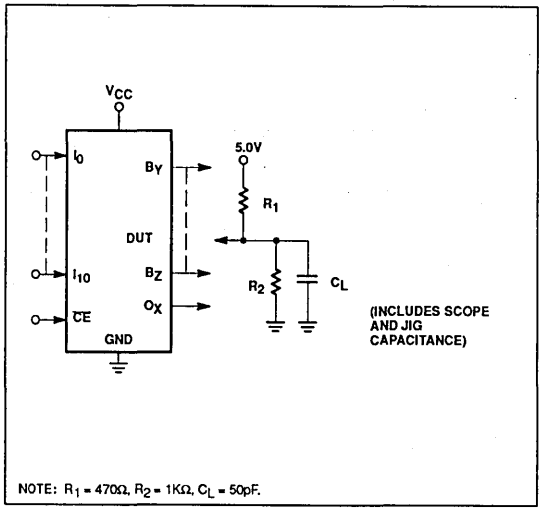
TIMING DEFINITIONS

SYMBOL	PARAMETER
T_{PD}	Propagation delay between input and output.
T_{OD}	Delay between input change and when output is off (Hi-Z or High).
T_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAMS

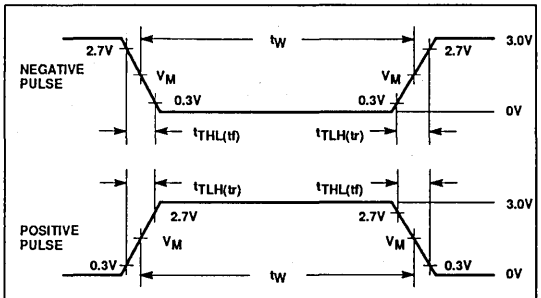


TEST LOAD CIRCUIT



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF.

VOLTAGE WAVEFORM



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Field-Programmable Logic Array (20 × 24 × 11) — PLHS473

LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this table, the logic state of variables I, P and B, associated with each SumTerm S is assigned a symbol which results in the proper fusing pattern of corresponding links, defined as follows:

LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A \bullet \overline{B} \bullet C \bullet D \bullet \ldots$

TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ldots$

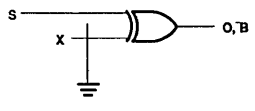
AT OUTPUT POLARITY = L

$\overline{Z} = \overline{P0 + P1 + P2 + \ldots}$

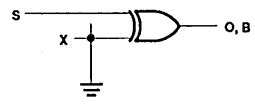
$Z = \overline{P0} \bullet \overline{P1} \bullet \overline{P2} \bullet \ldots$

NOTES:
1. For each of the 11 outputs, either function Z (Active-High) or $\overline{Z}$ (Active-Low) is avialable, but not both. The desired output polarity is programmed via the Ex-OR gates.
2. Z, A, B, C, etc., are user defined connections to fixed inputs (I), fixed output pins (O) and bidirectional pins (B).

OUTPUT POLARITY - (O, B)

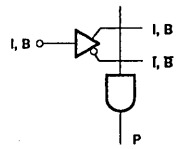


ACTIVE LEVEL	CODE
LOW[13] (INVERTING)	L

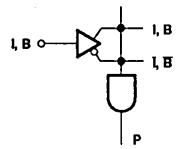


ACTIVE LEVEL	CODE
HIGH (NON-INVERTING)	H

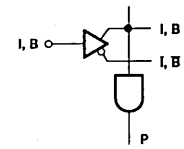
"AND" ARRAY - (I, B)



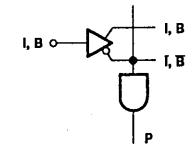
STATE	CODE
DON'T CARE[13]	-



STATE	CODE
INACTIVE[14]	O

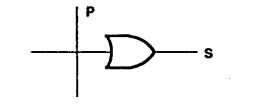


STATE	CODE
I, B	H

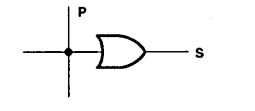


STATE	CODE
I, $\overline{B}$	L

"OR" ARRAY - (O, B)



P_n STATUS	CODE
INACTIVE[13]	•



P_n STATUS	CODE
ACTIVE	A

VIRGIN STATE

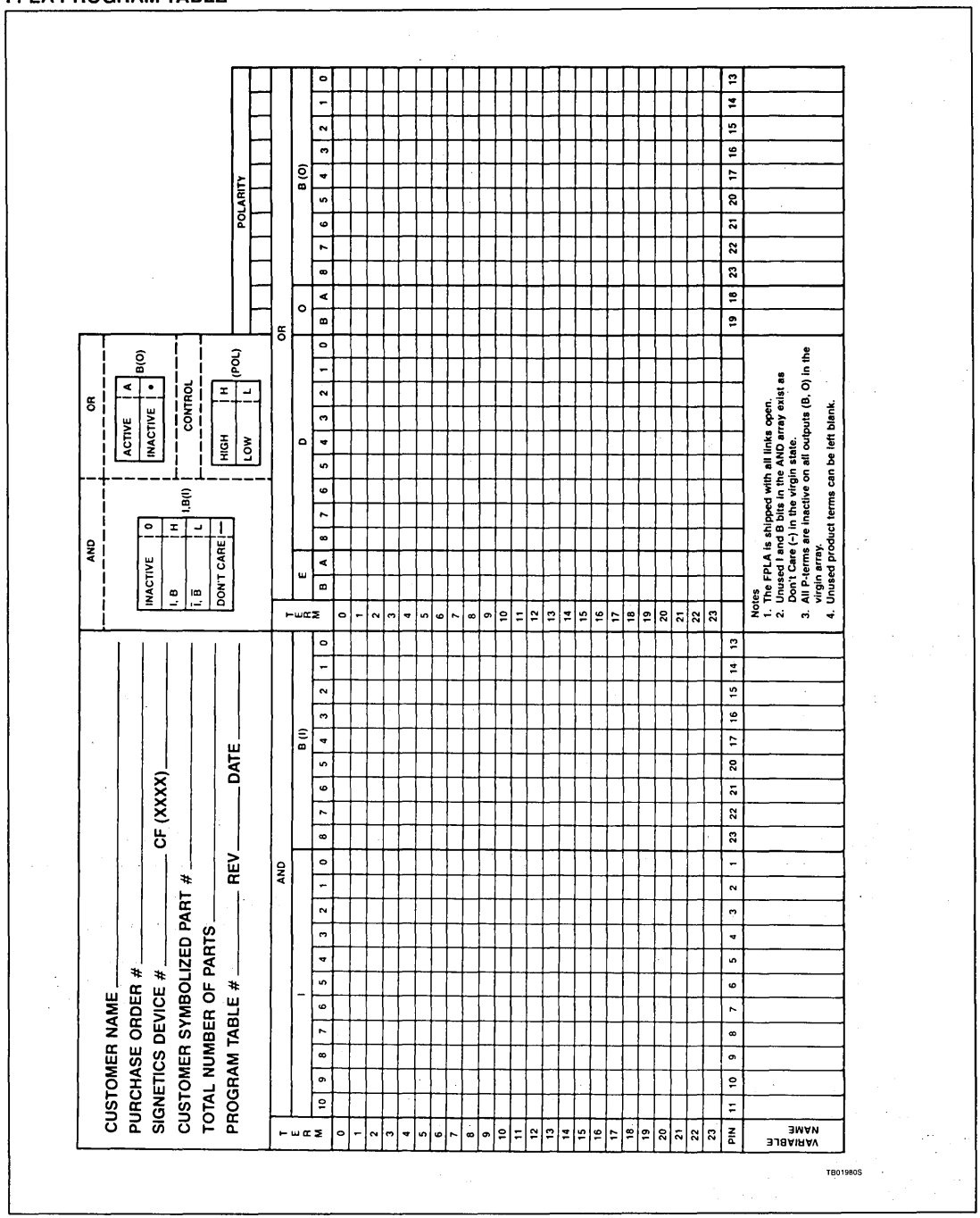
A factory shipped virgin device contains all fusible links intact, such that:
1. All outputs are at "L" polarity.
2. All P_n terms are enabled. (Don't Cares.)
3. All P_n terms are inactive on all outputs.

NOTES:
13. This is the initial unprogrammed state of all links.
14. Any gate P_n will unconditionally inhibited if the true and complement of either input (I or B) are both programmed for a connection.

Field-Programmable Logic Array (20 × 24 × 11)

PLHS473

FPLA PROGRAM TABLE



Signetics

PLHS501
Programmable Macro Logic
Random Logic Unit (32 × 72 × 24)

Product Specification

Military Application Specific Products

DESCRIPTION

The PLHS501 is a member of the Signetics Programmable Macro Logic family. PML is unique in its capability of performing other than two level logic functions without incurring I/O buffer delays. This allows the logic or system designer to imbed logical operations or macro structures within the framework of the I/O pins. Since the imbedded functions are independent of the delays created by the I/O buffers, they can be performed at speeds lesser architectures cannot reproduce.

The technique used to perform this operation is a NAND foldback network which allows the direct interconnection of any number of logic nodes within the single fuse matrix. Macros can be formed and then interconnected to the I/O structure. In addition, single-level and multi-level logic can be performed at speeds which reflect only the logic path utilized. Therefore, a single-level logic function has a very short path through the device. Additional levels incur only one NAND foldback delay per level. This delay is less than the combined delay created by previous generations of devices which stipulate that the logic signal must pass through I/O buffers after one or two levels of logic are performed.

The PLHS501 is fabricated with Signetics ZA Oxide-Isolated Bipolar Process. ZA utilizes Vertical Avalanche Migration Programmed (VAMP) fuses as programming elements. These fuses provide high programming yield and reliability. Proprietary onboard test circuitry allows the PLHS501 to be thoroughly tested prior to programming.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
64-Pin Ceramic DIP	PLHS501/BXA

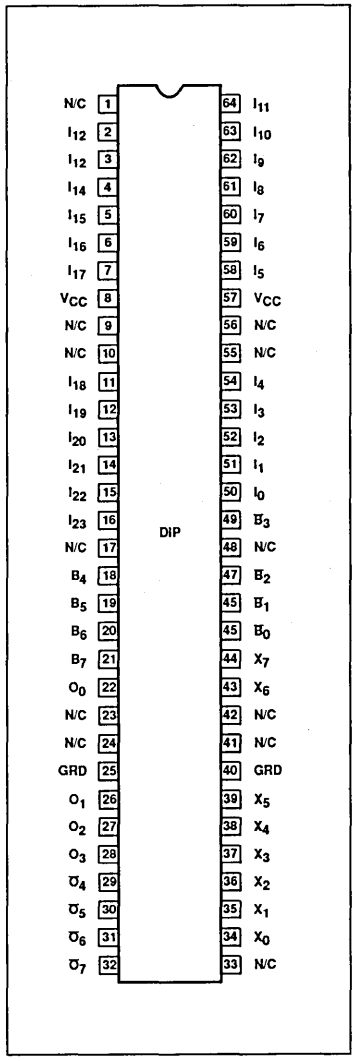
FEATURES

- Signetics NAND foldback architecture
- Field-Programmable
- 24 dedicated inputs
- Fixed and programmable output buffers
  - 8 I/O buffers
  - 8 EX-OR buffers
  - 4 active-Low buffers
  - 4 active-High buffers
- 72 Internal NAND foldback terms
- Supported by AMAZE Development System
- Testable in unprogrammed state
- Verify Lock Fuse
- TTL compatible
- Power dissipation: 1.25W (typ)
- Logic delay times
  - Single-level = 35ns (max)
  - Two-level = 45ns (max)
  - Internal NAND delay = 10ns (max)

ARCHITECTURE

- 24 dedicated Inputs: I_0 - I_{23}
- 4 active-High I/Os with individual enable: B_4 - B_7
- 4 active-Low I/Os with individual fused enable: $\overline{B}_0$ - $\overline{B}_3$
- 2 active-High output pairs; each pair with common enable: O_0 - O_3
- 2 active-Low output pairs; each pair with common enable: $\overline{O}_4$ - $\overline{O}_7$
- 4 Ex-OR output pairs; each pair with common enable: X_0 - X_7
- 72 Internal NAND foldback terms

PIN CONFIGURATION



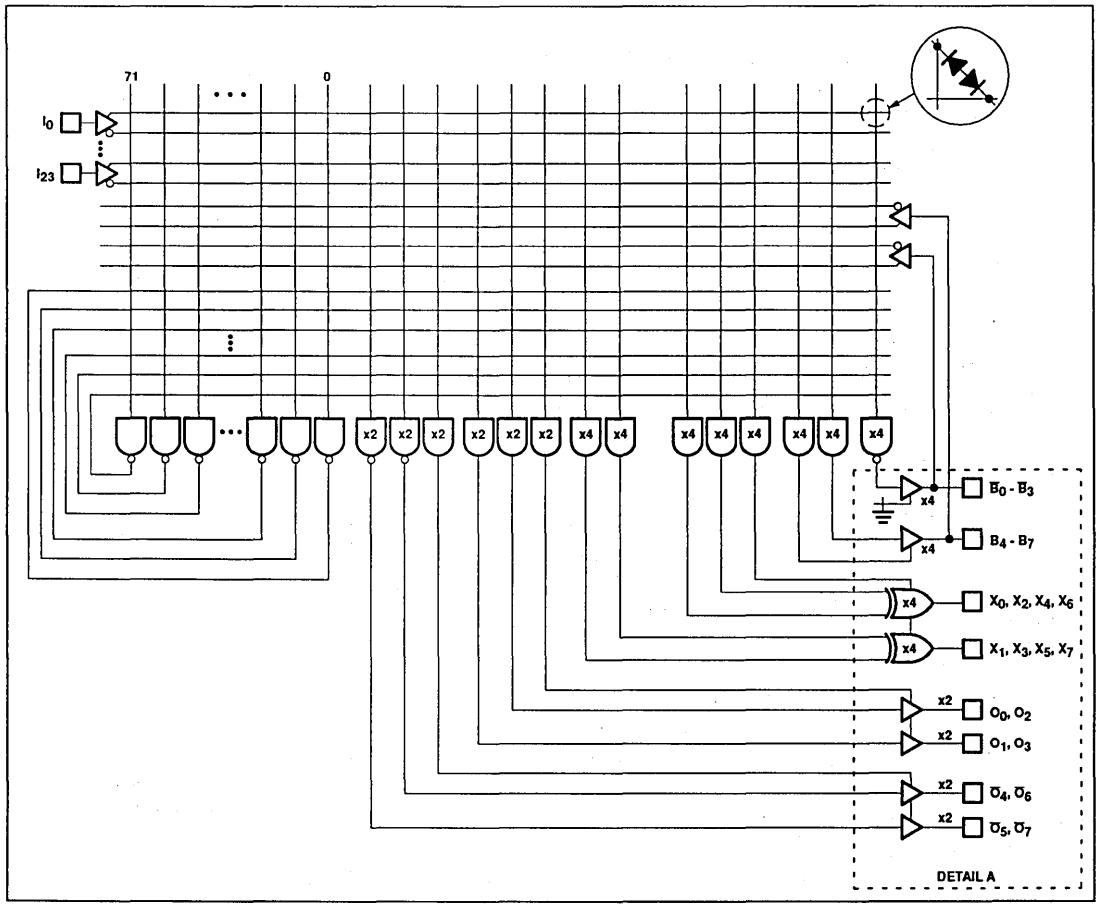
Programmable Macro Logic
Random Logic Unit (32 × 72 × 24)

PLHS501

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5V to +7.0	V
V_I	Input voltage range	-0.5V to +5.5	V
I_I	Input current range	-30 to +30	mA
V_O	Voltage range applied to output in High output state	-0.5 to +V_{CC}	V
I_O	Current range applied to output in Low output state	100	mA
T_A	Operating temperature range	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C

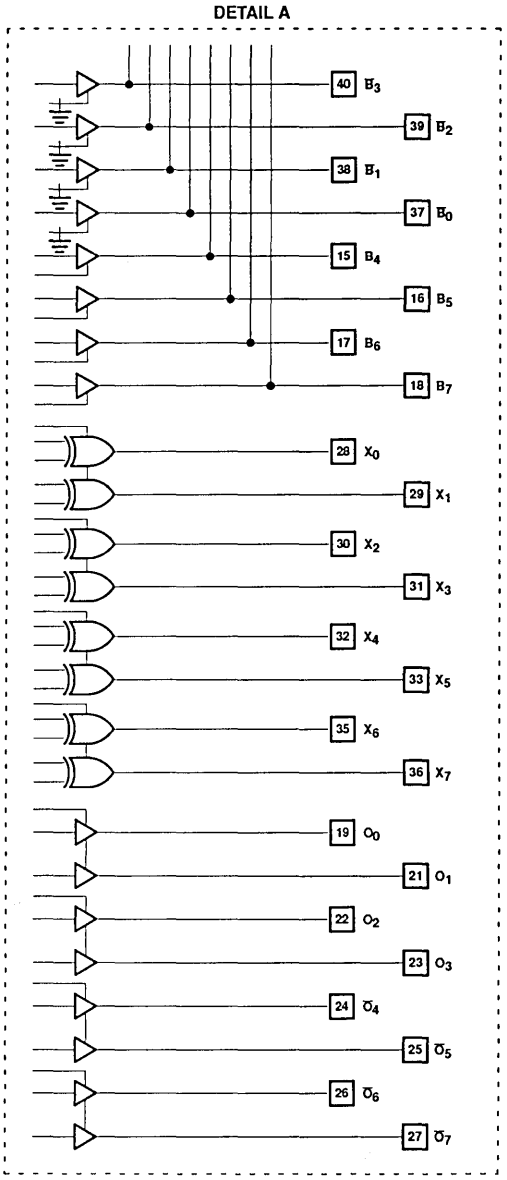
FUNCTIONAL DIAGRAM



Programmable Macro Logic
Random Logic Unit (32 × 72 × 24)

PLHS501

LOGIC DIAGRAM (Compressed)



Programmable Macro Logic
Random Logic Unit (32 × 72 × 24)

PLHS501

DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ[2]	Max	
Input Voltage[2]						
V_{IL}	Low	V_{CC} = Min			0.8	V
V_{IH}	High	V_{CC} = Max	2.0			V
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2	V
Output voltage						
V_{OL}	Low[3,5]	V_{CC} = Min I_{OL} = 10mA			.5	V
V_{OH}	High[3,6]	I_{OH} = -2mA	2.4			V
Input current						
I_{IL}	Low	V_{CC} = Max V_{IN} = 0.4V			-100	µA
I_{IH}	High	V_{IN} = 5.5V			40	µA
Output current						
$I_{O(OFF)}$	Hi-Z state[10]	V_{CC} = Max V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.4V			-140	
I_{OS}	Short circuit[4,6,7]	V_{OUT} = 0V	-15		-85	mA
I_{CC}	V_{CC} supply circuit[8]	V_{CC} = Max		225	295	mA
Capacitance						
I_{IN}	Input	V_{CC} = 5V V_{IN} = 2.0V		8		pF
C_B	I/O	V_{OUT} = 2.0V		15		pF

AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V, R_1 = 470Ω, R_2 = 1KΩ

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
	TO	FROM		Min	Typ[2]	Max	
t_{PD1}	Output ±	Input ±	C_L = 50pF			35	ns
t_{PD2}	Output ±	Input ±				35	ns
t_{PD3}	Output ±	Input ±				35	ns
t_{PD4}[11]	Output ±	Input ±				45	ns
t_{PD5}[11,12]	Output ±	Input ±				45	ns
t_{PD6}[11,12]	Output ±	Input ±				45	ns
t_{PD7}[12]	Internal				8		ns
t_{OE}	Output -	Input ±				40	ns
t_{OD}[9]	Output +	Input ±				40	ns

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. For Pins 18-22, 26-32 and 45-47, 49, V_{OL} is measured with Pins 5 and 50 = 9.5V, Pin 52 = 0V and Pins 51 and 53 = 4.5V. For Pins 34-39 and 43-44, V_{OL} is measured under same conditions EXCEPT Pin 53 = 0V.
6. V_{OH} is measured with Pins 5 and 50 = 9.5V, Pins 51 and 52 = 4.5V and Pin 53 = 0V.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with all dedicated inputs at 0V and bidirectional and output pins open.
9. Measured at V_T = V_{OL} + 0.5V, V_{OH} - 0.5V.
10. Leakage values are a combination of input and output leakage.
11. Limits are guaranteed with internal feedback buffers simultaneously switching cumulative maximum of eight outputs.
12. Only tested on a programmed device if applicable.

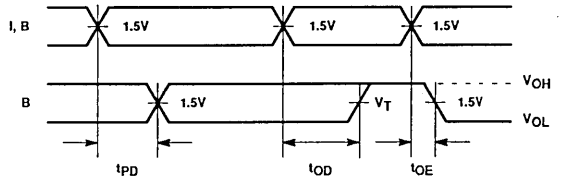
Programmable Macro Logic
Random Logic Unit (32 × 72 × 24)

PLHS501

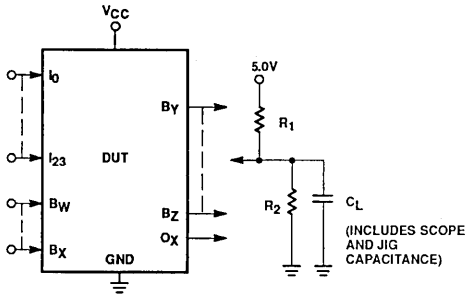
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD1}	Input to Output delay, one pass, through X outputs
t_{PD2}	Input to Output delay, one pass, through $\overline{B}$ outputs
t_{PD3}	Input to Output delay, one pass, through O, $\overline{O}$ and B outputs
t_{PD4}	Input to Output delay, two passes, through X outputs
t_{PD5}	Input to Output delay, two passes, through $\overline{B}$ outputs
t_{PD6}	Input to Output delay, two passes, through O, $\overline{O}$ and B outputs
t_{PD7}	Feedback delay per internal NAND function performed
t_{OD}	Delay between output change and when output is off (Hi-Z or High)
t_{OE}	Delay between input change and when the output reflects specified output level

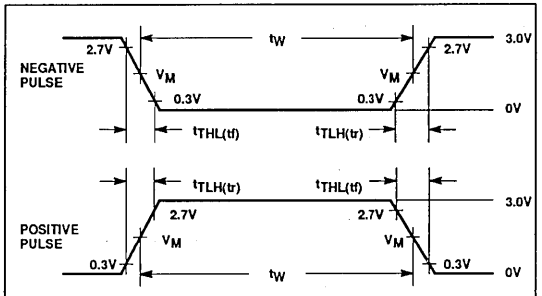
TIMING DIAGRAM



TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Signetics

PLS159A

Field-Programmable Logic Sequencer (16 × 45 × 12)

Product Specification

Military Application Specific Products

DESCRIPTION

The PLS159A is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "foldback" inverting buffer and control gate F_C. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). There are 8 dedicated inputs. These yield variable I/O gate and register configurations via control gates (D, L) ranging from 16 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 4 inputs (I), 4 bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complement Array output ($\overline{C}$). The Complement Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

FEATURES

- High-speed version of PLS159
- Field-programmable (Ni-Cr link)
- F_{MAX} = 16MHz
- 4 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 4 bidirectional I/O lines
- 8 bidirectional registers
- J-K, T, or D-type flip-flops
- Power-on reset feature on all flip-flops (F_n = 1)
- Asynchronous Preset/Reset
- Complement Array
- Active-High or -Low outputs
- Programmable $\overline{OE}$ control
- Positive edge triggered clock
- Input loading: -100μA (max)
- Power dissipation: 750mW (typ)
- TTL Compatible
- 3-State outputs

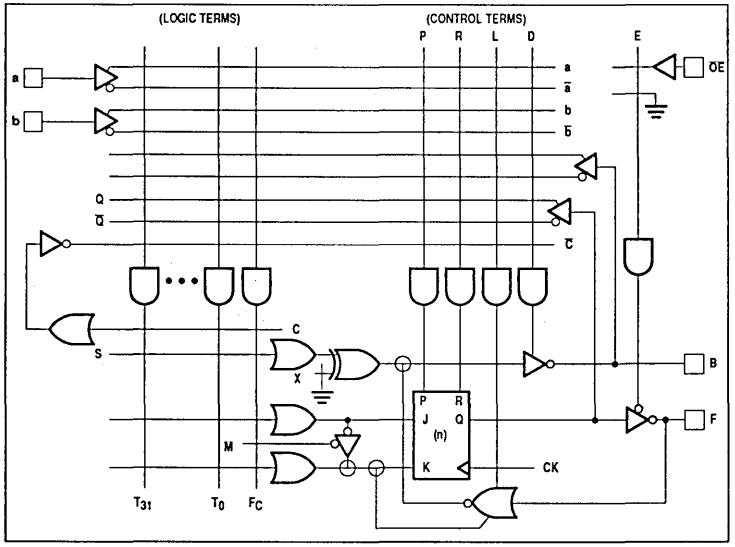
APPLICATIONS

- Random sequential logic
- Synchronous Up/Down counters
- Shift Registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

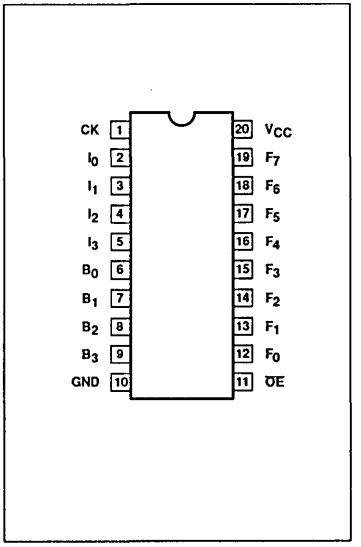
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic Dip 300mil-wide	PLS159A/BRA

FUNCTIONAL DIAGRAM



PIN CONFIGURATION



Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

On-chip T/C buffers couple either True (I, B, Q) or complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates.One group of AND gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of EX-OR gates for implementing AND-OR or AND-NOR logic functions. Another group drives the J-K inputs of all flip-flops, as well as asynchronous Preset and Reset lines (P, R).

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (B), (Q) and programmable output select lines (E).

The PLS159A is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

VIRGIN STATE

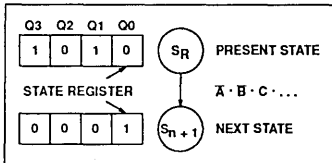
The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode unless otherwise programmed to J-K only or J-K or D (controlled).
5. All B pins are inputs and all F pins are outputs unless otherwise programmed.

CAUTION: PLS159A PROGRAMMING ALGORITHM

The programming voltage required to program the PLS159A is higher (17.5V) than that required to program the PLS159 (14.5V). Consequently, the PLS159 programming algorithm will not program the PLS159A. Please exercise caution when accessing programmer device codes to ensure that the correct algorithm is used.

LOGIC FUNCTION



SET Q_0: $J_0 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$K_0 = 0$

RESET Q_1: $J_1 = 0$
$K_1 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $J_2 = 0$
$K_2 = 0$

TOGGLE Q_3: $J_3 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$K_3 = (Q_3 \cdot \overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

NOTE:
Similar logic functions are applicable for D and T mode flip-flops.

FLIP-FLOP TRUTH TABLE

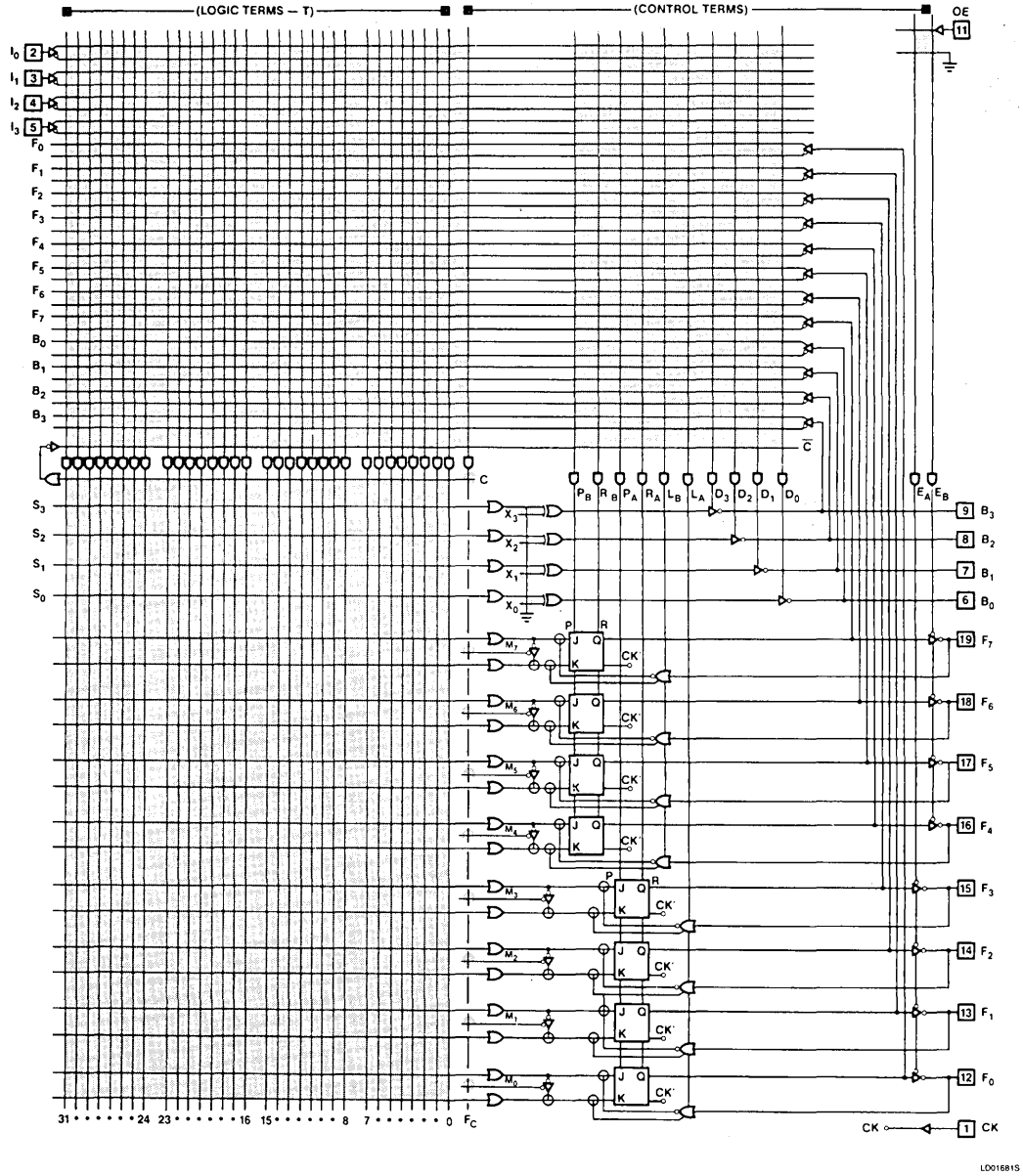
$\overline{OE}$	L	CK	P	R	J	K	Q	F
H								Hi-Z
L	X	X	L	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
+10V	X	↑	X	X	H	L	H	L**

NOTES:

1. Positive Logic:
   $J\text{-}K = T_0 + T_1 + T_2 + \ldots + T_{31}$
   $T_n = \overline{C} \cdot (I_0.I_1.I_2\ldots) \cdot (Q_0.Q_1\ldots) \cdot (B_0.B_1\ldots)$
2. ↑ denotes transition for Low to High level.
3. X = Don't care
4. * = Forced at F_n pin for loading J-K flip-flop in I/O mode. L must be enabled, and other active T_R disabled via steering input(s) I, B, or Q.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at F_n pin to load J/K flip-flop independent of program code (Diagnostic mode). 3-State B outputs.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

FPLS LOGIC DIAGRAM



NOTES:
1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. ⊗ Programmable connection.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_I	Input voltage		+5.5	V_{DC}
V_O	Output voltage		+5.5	V_{DC}
I_I	Input current	-30	+30	mA
I_O	Output current		+100	mA
T_{STG}	Storage temperature range	-65	+150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IN}[9]	High level Input voltage	2.2			V
V_{IL}[9]	Low level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High level output current			-2	mA
I_{OL}	Low level output current			10	mA
T_A	Operation free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER[3]	TEST CONDITIONS[3]	LIMIT[3]			UNIT
			Min	Typ[2]	Max	
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = Max		-0.8	-1.2	V
V_{OH}	Output High voltage	V_{CC} = Min, I_{OH} = Max	2.4			V
V_{OL}	Output Low voltage	V_{CC} = Min, I_{OL} = Max		0.35	0.5	V
I_{IH}	Input High current	V_{CC} = Max, V_I = 5.5V		<1	40	µA
I_{IL}	Input Low current	V_{CC} = Max, V_I = 0.45V		-10	-100	µA
I_{OHZ}	OFF-State output[5,8] Current High	V_{CC} = Max, V_O = 5.5V			80	µA
I_{OLZ}	OFF-State output[5,8] Current High	V_{CC} = Max, V_O = 0.45V			-140	µA
I_{OS}	Short circuit output current[4,6]	V_{CC} = Max, V_O = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		150	190	mA
C_{IN}	Input capacitance[15]	V_{CC} = 5.0V, V_I = 2.0V		8	13	pF
C_{OUT}	Output capacitance[15]	V_{CC} = 5.0V, V_O = 2.0V		15	20	pF

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

AC ELECTRICAL CHARACTERISTICS $-55^{o}C \leq T_A \leq +125^{o}C$, $4.5V \leq V_{CC} \leq 5.5V$

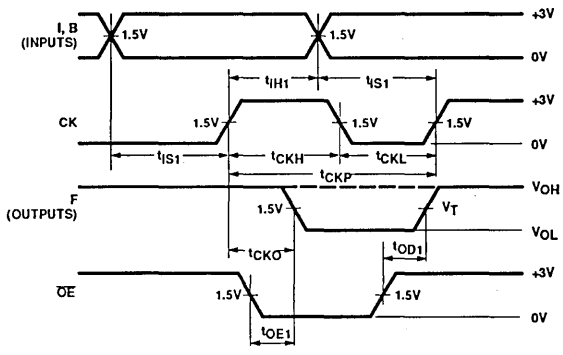
SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min[13]	Typ[2]	Max	
Pulse Width								
t_{CKH}	Clock high[10]	CK-	CK+	C_L = 50pF	20	15		ns
t_{CKL}	Clock low	CK+	CK-	C_L = 50pF	20	15		ns
t_{CKP}	CLK min Period ($t_{IS1} + t_{CKO}$)	CK+	CK+	C_L = 50pF	60	55		ns
t_{PRH}	Preset/Reset pulse	(I, B)+	(I, B)-	C_L = 30pF	35	30		ns
Setup Time								
t_{IS1}	Input	CK+	(I, B)±	C_L = 50pF	35	30		ns
t_{IS2}	Input (through F_n)	CK+	F±	C_L = 50pF	15	10		ns
t_{IS3}	Input (through Complement Array)[12,14]	CK+	(I, B)±	C_L = 50pF	55	45		ns
Hold Time								
t_{IH1}	Input	CK+	(I, B)±	C_L = 50pF	0	-5		ns
t_{IH2}	Input (through F_n)[14]	CK+	F±	C_L = 50pF	15	10		ns
Propagation Delay								
t_{CKO}	Clock	F±	CK+	C_L = 50pF		15	25	ns
t_{OE1}	Output enable[14]	F-	$\overline{OE}$-	C_L = 50pF		20	35	ns
t_{OD1}	Output disable[12,14,15]	F+	$\overline{OE}$+	C_L = 5pF		20	35	ns
t_{PD}	Output	B±	(I, B)±	C_L = 50pF		25	45	ns
t_{OE2}	Output enable[14]	B±	(I, B)+	C_L = 50pF		20	35	ns
t_{OD2}	Output disable[11,14,15]	B+	(I, B)-	C_L = 5pF		20	35	ns
t_{PRO}	Preset/Reset[14,15]	F+	(I, B)+	C_L = 50pF		35	45	ns
t_{PPR}	Power-on/preset[14,15]	F-	V_{CC}+	C_L = 50pF		0	10	ns

NOTES:

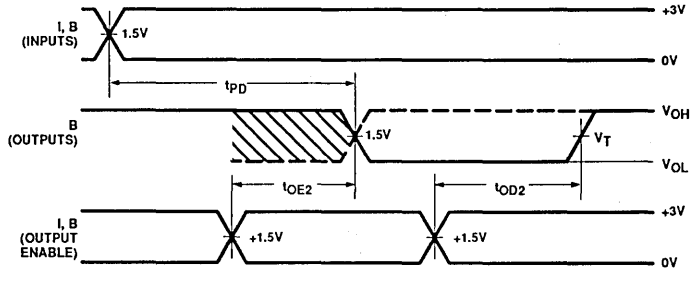
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IH} applied to $\overline{OE}$.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V, and the outputs open.
8. Leakage values are a combination of input and output leakage.
9. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.
10. To prevent spurious clocking, clock rise time (10% - 90%) ≤ 10ns.
11. Measured at $V_T = V_{OL} + 0.5V$.
12. When using the Complement Array T_{CKP} = 75ns (min).
13. Limits are guaranteed with 12 product terms maximum connected to each sum term line.
14. Not tested on an unprogrammed device.
15. Guaranteed, but not tested.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

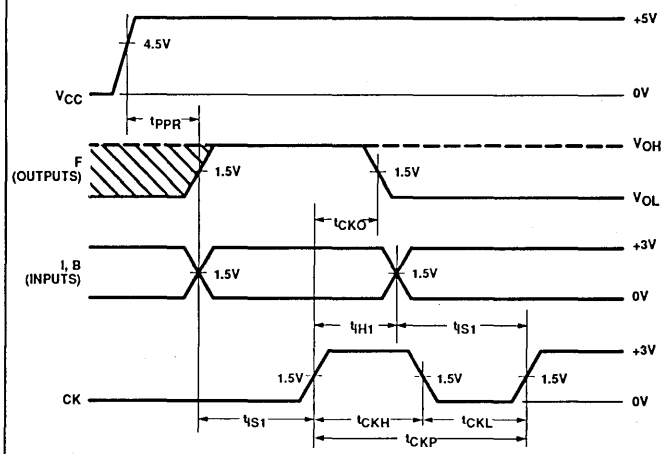
TIMING DIAGRAMS



Flip-Flop Outputs



Gate Outputs

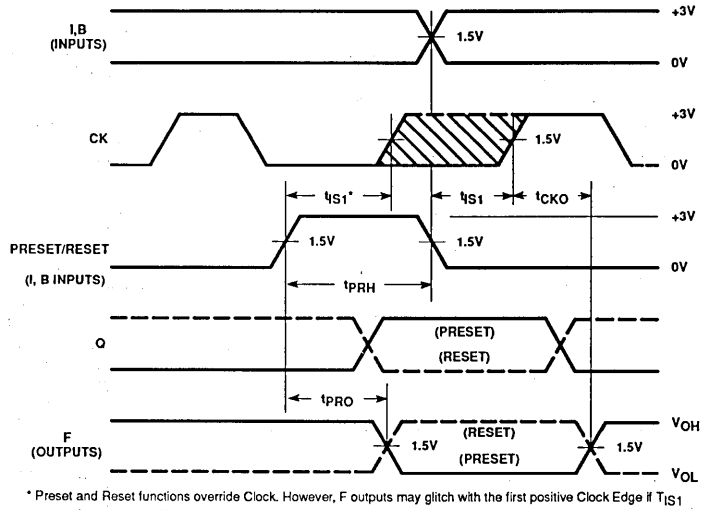


Power-On Reset

TIMING DEFINITIONS

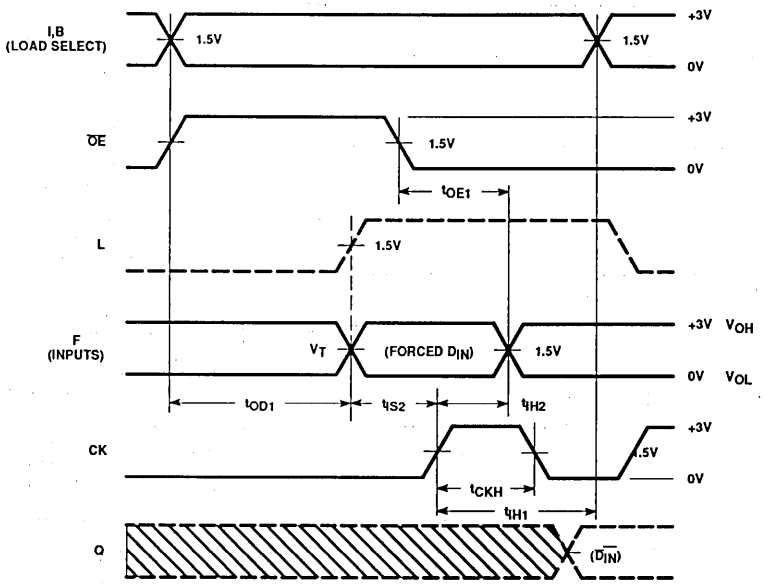
SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse when High.
t_{CKL}	Width of input clock pulse when Low.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input forced at flip-flop output pins and position transition of clock.
t_{IH1}	Required delay betweeen positive transition of clock and end of valid input data.
t_{IH2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock when outputs become valid (with $\overline{OE}$ Low).
t_{OE1}	Delay between beginning of Output Enable Low and when outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when outputs are in the Off-State.
t_{PPR}	Delay between V_{CC} (after power-on) and when flip-flop outputs become preset at "1" (internal Q outputs at "0").
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational outputs are in the Off-State.
t_{PRO}	Delay between positive transition of predefined Preset/ Reset input and when flip-flop outputs become valid.

TIMING DIAGRAMS (Continued)



* Preset and Reset functions override Clock. However, F outputs may glitch with the first positive Clock Edge if T_{IS1} cannot be guaranteed by the user.

Asynchronous Preset/Reset



Flip-Flop Input Mode

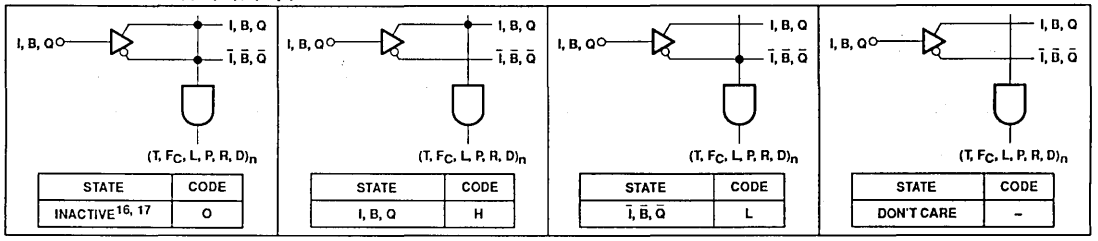
Field-Programmable Logic Sequencer (16 × 45 × 12) — PLS159A

The FPLS can be programmed by means of Logic Programming equipment.

With Logic Programming, the AND/OR-EX-OR input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Tables on the following pages.

In these Tables, the logic state or action of all I/O, control and state variables are assigned a symbol which results in the proper fusing pattern of corresponding links defined as follows:

"AND" ARRAY – (I), (B), (Qp)



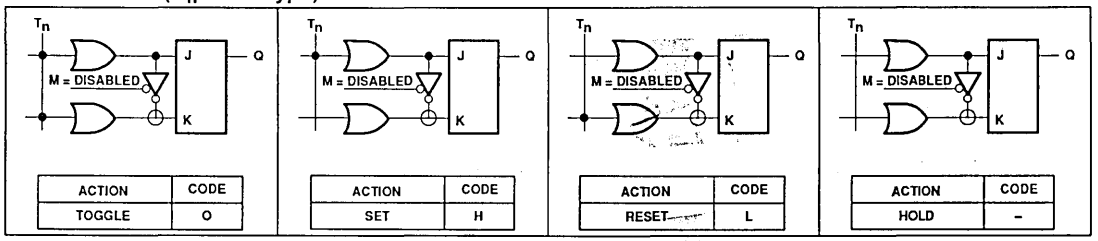
STATE	CODE
INACTIVE[16, 17]	O

STATE	CODE
I, B, Q	H

STATE	CODE
$\bar{I}, \bar{B}, \bar{Q}$	L

STATE	CODE
DON'T CARE	–

"OR" ARRAY – (Q_n = J-K Type)



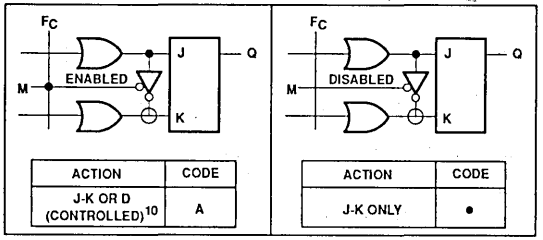
ACTION	CODE
TOGGLE	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	–

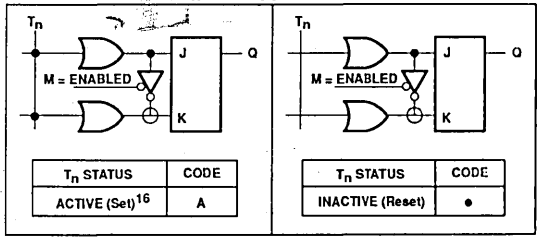
"OR" ARRAY – (F-F CONTROL MODE)



ACTION	CODE
J-K OR D (CONTROLLED)[10]	A

ACTION	CODE
J-K ONLY	•

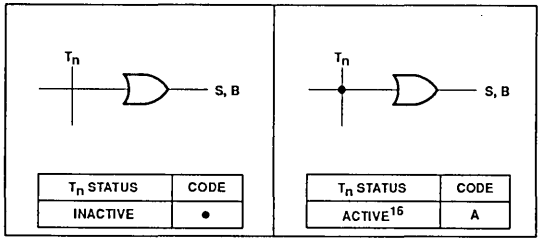
"OR" ARRAY – (Q_n = D-Type)



T_n STATUS	CODE
ACTIVE (Set)[16]	A

T_n STATUS	CODE
INACTIVE (Reset)	•

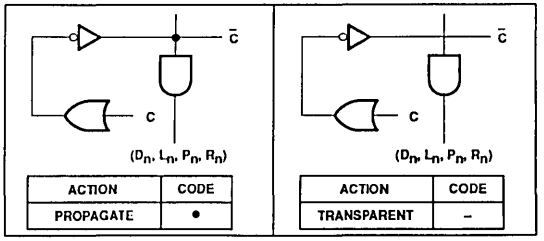
"OR" ARRAY – (S or B)



T_n STATUS	CODE
INACTIVE	•

T_n STATUS	CODE
ACTIVE[16]	A

"COMPLEMENT" ARRAY – MODE



ACTION	CODE
PROPAGATE	•

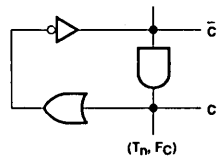
ACTION	CODE
TRANSPARENT	–

Notes on following page.

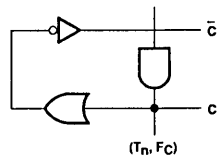
CAUTION:
THE PLS159A Programming Algorithm is different from the PLS159.

Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

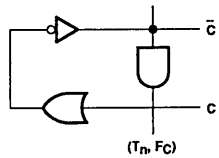
"COMPLEMENT" ARRAY – (C)



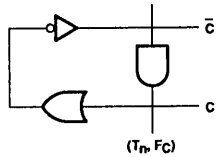
ACTION	CODE
INACTIVE[16, 18, 20]	O



ACTION	CODE
GENERATE[20]	A

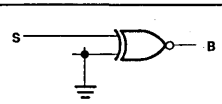


ACTION	CODE
PROPAGATE	•

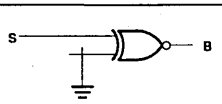


ACTION	CODE
TRANSPARENT	–

"EX-OR" ARRAY – (B)

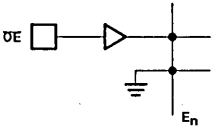


POLARITY	CODE
LOW	L

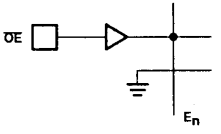


POLARITY	CODE
HIGH	H

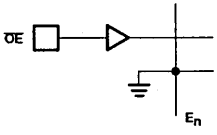
"OE" ARRAY – (E)



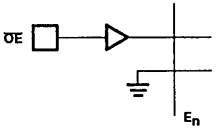
ACTION	CODE
IDLE[16, 19]	O



ACTION	CODE
CONTROL	A



ACTION	CODE
ENABLE[19]	•



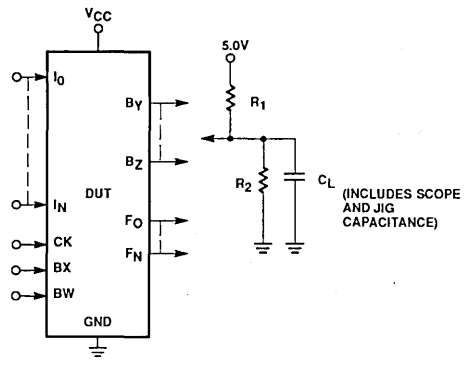
ACTION	CODE
DISABLE	–

NOTES:

16. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
17. Any gate $(T, F_C. L, P, R, D)_n$ will be unconditionally inhibited if any one of the I, B, or Q link pairs are left intact.
18. To prevent oscillations, this state is not allowed for C link, pairs coupled to active gates T_n, F_C.
19. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
20. These states are not allowed for control gates $(L, P, R, D)_n$ due to their lack of "OR" array links.

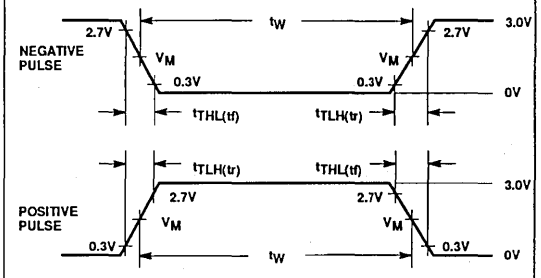
Field-Programmable Logic Sequencer (16 × 45 × 12) PLS159A

TEST LOAD CIRCUITS



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF

VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Signetics

PLS167

Field-Programmable Logic Sequencer ($14 \times 48 \times 6$)

Military
Customer Specific Products

Product Specification

DESCRIPTION

The PLS167 is a bipolar, programmable state machine of the Mealy type. The Field-Programmable Logic Sequencer (FPLS) contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 8 Q_p, and 4 Q_f edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND Array combines 14 external inputs, $I_{0\text{-}13}$, with 8 internal inputs, $P_{0\text{-}7}$, fed back from the State Register to form up to 48 transition terms (AND terms). In addition, P_0 and P_1 of the internal state register are brought off-chip to allow extending the Output Register to 6 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR Array to issue next-state and next-output commands to their respective registers on the Low to High transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to output-enable enable function, as an additional user programmable option.

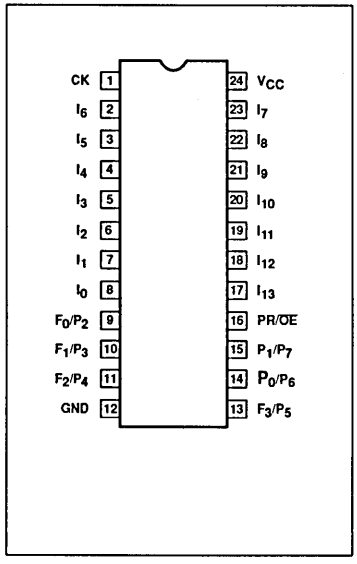
APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Security locking systems

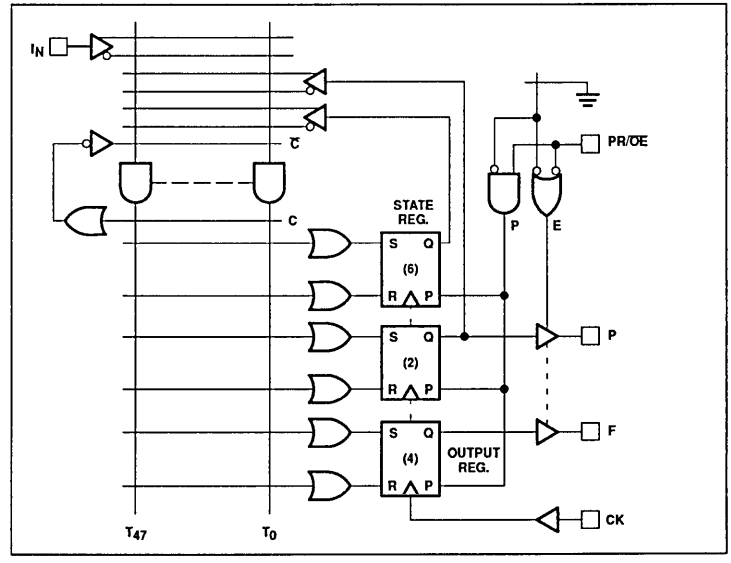
FEATURES

- Field-programmable (Ni-Cr link)
- 14 True/Complement buffered inputs
- 48 programmable AND gates
- 25 programmable OR gates
- 8-bit State Register
- 2-bit shared State/Output Register
- 4-bit Output Register
- Transition Complement Array
- Programmable asynchronous preset/output enable
- Positive edge-trigger clock
- Power-on preset to logic "1" of all registers
- Automatic logic "HOLD" state via S/R flip-flops
- On-chip Test Array
- Power: 650mW (typ)
- TTL compatible
- Tri-state outputs
- Single +5V supply
- 300mil wide 24-Pin DIP

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



Field-Programmable Logic Sequencer (14 × 48 × 6) — PLS167

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic Dip 300mil-wide	PLS167/BLA

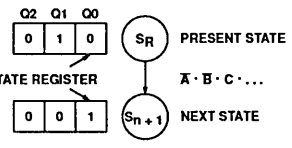
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**Clock:** The Clock input to the state and output registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2 - 7 17 - 23	I_{1-13}	**Logic Inputs:** The 13 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
8	I_0	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercised with standard TTL levels. When I_0 is held at +10V, device outputs F_{0-3} and P_{0-1} reflect the contents of state register bits P_{2-7} (see Diagnostic Output Mode diagram). The contents of flip-flops P_{0-1} and F_{0-3} remain unaltered.	Active-High/Low
9 - 11 13	F_{0-3}	**Logic/Diagnostic Outputs:** Four device outputs which normally reflect the contents of output register bits Q_{0-3} when enabled. When I_0 is held at +10V, $F_{0-3} = (P_{2-5})$.	Active-High
14 - 15	P_{0-1}	**Logic/Diagnostic Outputs:** Two register bits with shared function as least significant state register bits, or most significant output register bits. When I_0 is held at +10V, $P_{0-1} = (P_{6-7})$.	Active-High
16	PR/$\overline{OE}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function: • **Preset:** Provides an asynchronous preset to logic "1" of all state and output register bits. Preset overrides Clock, and when held High, clocking is inhibited and P_{0-1} and F_{0-3} are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low. • **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers.	Active-High (H) Active-Low (L)

Field-Programmable Logic Sequencer (14 × 48 × 6) — PLS167

LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

6. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
7. All transition terms are disabled (0).
8. All S/R flip-flop inputs are disabled (0).
9. The device can be clocked via a Test Array pre-programmed with a standard test pattern.

   NOTE: The Test Array pattern must be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

TRUTH TABLE[1, 2, 3, 4, 5, 6]

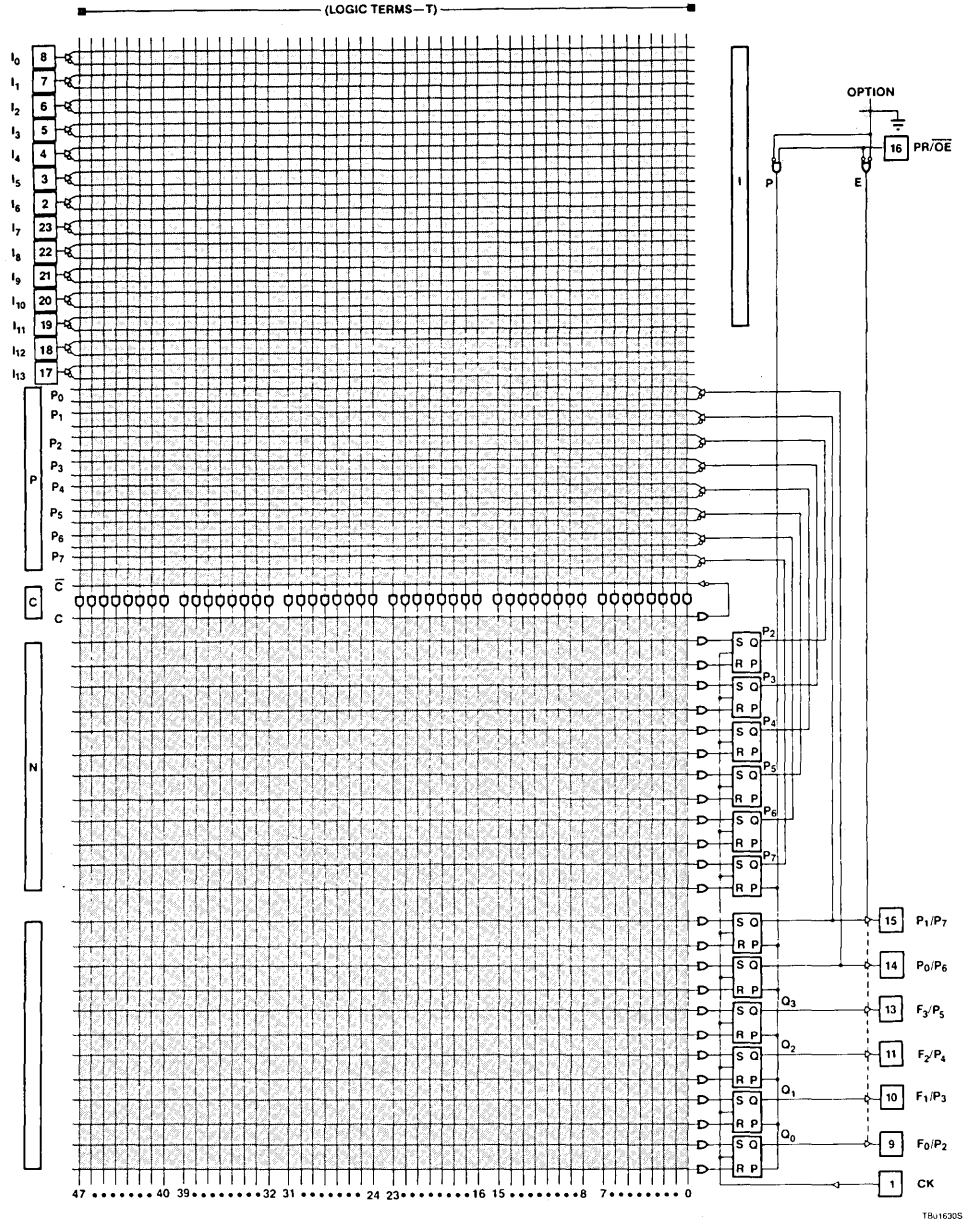
V_{CC}	OPTION PR	OPTION $\overline{OE}$	I_0	CK	S	R	$Q_{P/F}$	F
+5V	H		•	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	•	X	X	X	Q_n	Hi-Z
		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

NOTES:
1. Positive Logic
   $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$
   $T_n = C(I_0\, I_1\, I_2 \ldots)\,(P_0\, P_1 \ldots P_7)$
2. Either Preset (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. • = H/L/+10V.
6. X = Don't Care (≤ 5.5V).

Field-Programmable Logic Sequencer (14 × 48 × 6)

PLS167

FPLS LOGIC DIAGRAM



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ◎ Programmable connection.

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I	Input voltage	+10.0	V_{DC}
V_O	Output voltage	+5.5	V_{DC}
I_I	Input currents	-30 to +30	mA
I_O	Output currents	+100	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage range	4.5	5.0	5.5	V
V_{IN}[13]	High level Input voltage	2.0			V
V_{IL}[13]	Low level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High level output current			-2	mA
I_{OL}	Low level output current			9.6	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TEST CONDITIONS[1, 2]	LIMITS[3]			UNIT
			Min	Typ[2]	Max	
V_{IK}	Input clamp voltage[4]	V_{CC} = 4.5V, I_I = I_{IK}		-0.8	-1.2	V
V_{OL} V_{OH}	Low level Output Voltage[6] High level Output Voltage[5]	V_{CC} = Min I_{OL} = Max I_{OH} = Max	 2.4	0.35	0.5	V V
I_{IL}	Low Level Input current	V_{CC} = Min, V_I = 0.45V		-10	-150	µA
I_{IL}	Low (CK input) Level Input current	V_I = 0.45V, V_{CC} = Min		-50	-350	µA
I_{IH}	High level Input current	V_I = 5.5V, V_{CC} = Min		-1	50	µA
I_{OHZ}	Off-State output[7], Current High	V_{CC} = Max, V_O = 5.5V		1	60	µA
I_{OLZ}	Off-State output[7], Current Low	V_O = 0.45V, V_{CC} = Max		-1	-60	µA
I_{OS}	Short circuit output current[4,8]	V_O = 0V, V_{CC} = Max	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	185	mA
C_{IN} C_{OUT}	Input Capacitance[10] Output Capacitance[10]	V_{CC} = Nom V_I = 2.0V V_O = 2.0V		8 10	13 15	pF pF

Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167

AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$. $4.5V \leq V_{CC} \leq 5.5V$

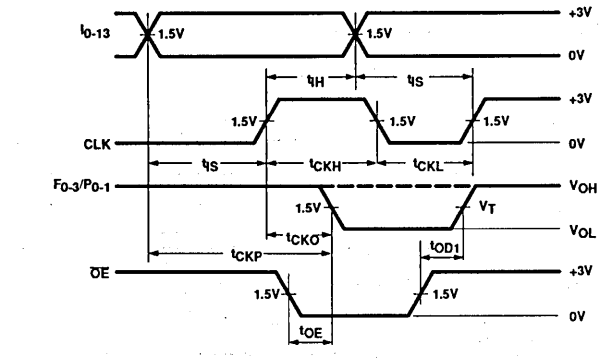
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
Pulse Width							
t_{CKH}	Clock high[11]	CK-	CK+	40	15		ns
t_{CKL}	Clock low	CK+	CK-	40	15		ns
t_{CKP1}	Period (w/o C-array)	CK+	CK+	95	40		ns
t_{CKP2}	Period (w/C-array)[10]	CK+	CK+	135	60		ns
t_{PRH}	Preset pulse	PR+	PR-	40	15		ns
Setup Time							
t_{IS1}	Input	CK+	Input±	60			ns
t_{IS2}	Input (through Complement array)[12]	CK+	Input±	100			ns
t_{VS}	Power-on preset[10]	CK-	V_{CC}+	5	-10		ns
t_{PRS}	Preset[10]	CK-	PR-	5	-10		ns
Hold Time							
t_{IH}	Input[10]	Input±	CK+	10	-10		ns
Propagation Delay							
t_{CKO}	Clock	Output±	CK+		15	35	ns
t_{OE}	Output Enable[12]	Output-	$\overline{OE}$-		20	40	ns
t_{OD}	Output Disable[12]	Output+	$\overline{OE}$+		20	40	ns
t_{PR}	Preset	Output+	PR+		18	45	ns
t_{PPR}	Power-on preset[10]	Output+	V_{CC}+		0	20	ns
Frequency of Operation							
f_{MAX}	W/O C-array					10.5	MHz
f_{MAX}^{C}	W/C-array[10]					7.4	MHz

NOTES:

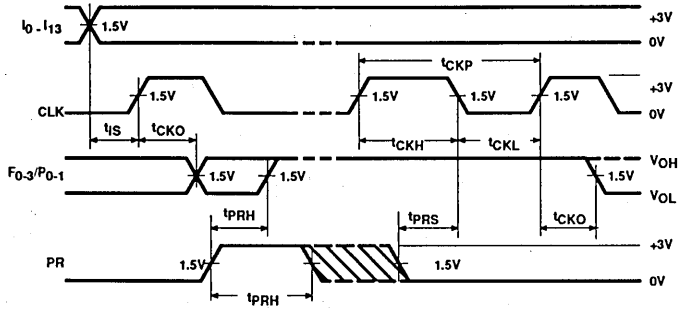
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.
6. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is supplied through a resistor to V_{CC}.
7. Measured with V_{IH} applied to PR/$\overline{OE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, the outputs open.
10. Guaranteed, but not tested.
11. To prevent spurious clocking, clock rise time (10% - 90%) ≤ 30ns.
12. Not testable on unprogrammed devices.
13. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.

Field-Programmable Logic Sequencer (14 × 48 × 6) — PLS167

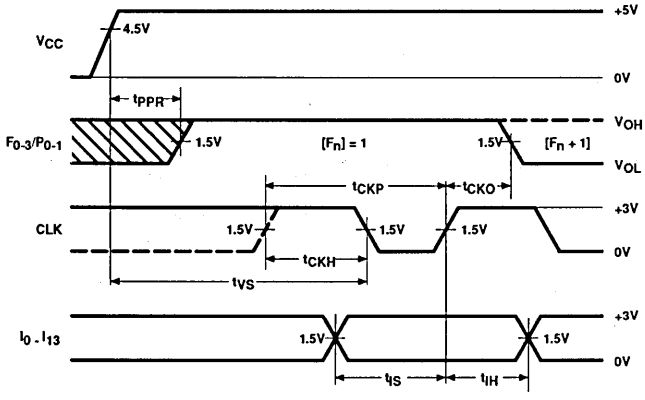
TIMING DIAGRAMS



Sequential Mode



Asynchronous Preset



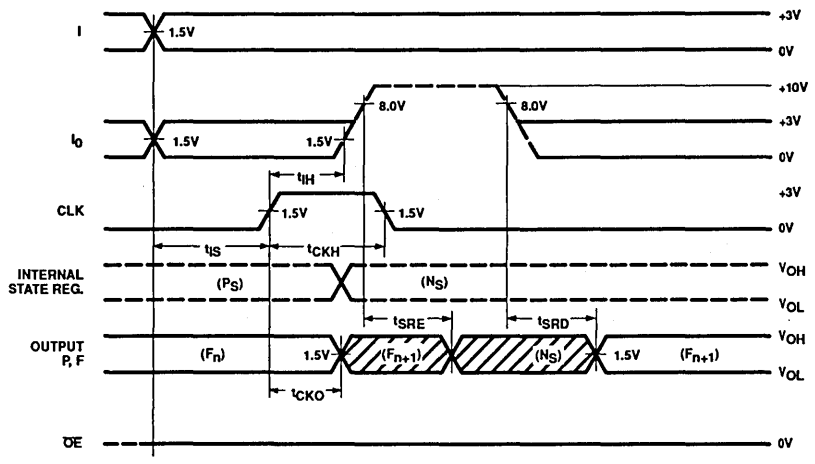
Power-On Preset

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP1}	Clock period - when not using Complement Array.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{CKP2}	Clock period - when using Complement Array.
t_{IS2}	Required delay between beginning of valid input and positive transition of clock, when using optional Complement array (two passes necessary through the AND array).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of clock and end of valid input data.
t_{CKO}	Delay between positive transition of clock and when Outputs become valid (with PR/$\overline{OE}$ Low).
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-State.
t_{PR}	Delay between positive transition of Preset and when Outputs become valid at "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Maximum clock frequency.

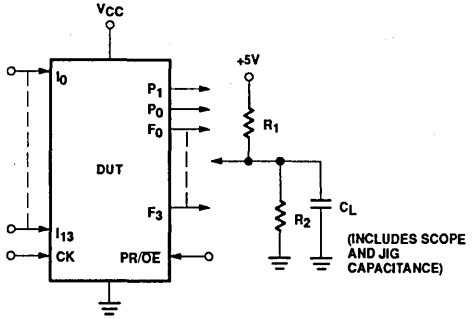
Field-Programmable Logic Sequencer (14 × 48 × 6) PLS167

TIMING DIAGRAMS (Continued)



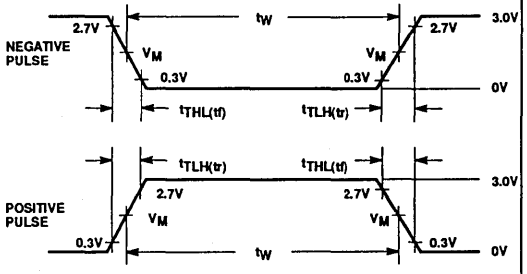
Diagnosic Output Mode

TEST LOAD CIRCUITS



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF.

VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Field-Programmable Logic Sequencer (14 × 48 × 6) — PLS167

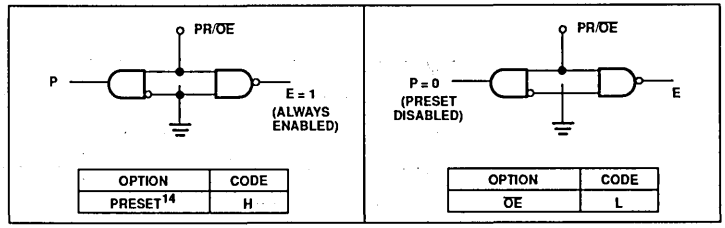
LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR gate input connections necessary to implement the desired logic function are coded directly from the State Diagram using a Program Table.

In this table, the logic state or action of control variables C, I, P, N and F, associated with each Transition Term T_n, is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

PRESET/$\overline{OE}$ OPTION - (P/E)

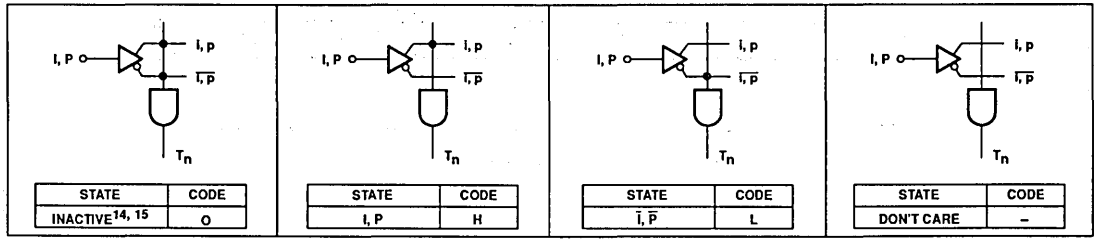


OPTION	CODE
PRESET[14]	H

OPTION	CODE
$\overline{OE}$	L

PROGRAMMING:
The PS167 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (state and output register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

"AND" ARRAY - (I), (P)



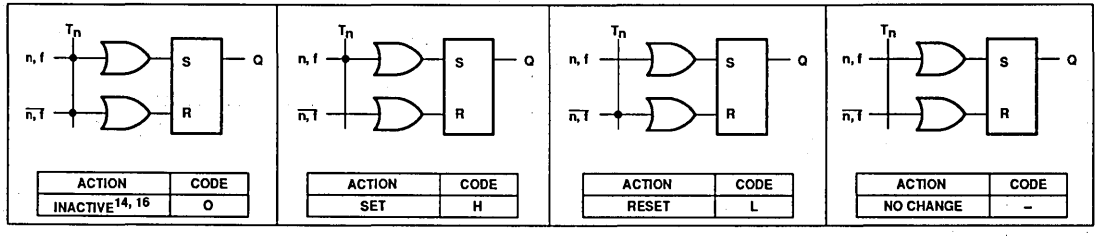
STATE	CODE
INACTIVE[14, 15]	O

STATE	CODE
I, P	H

STATE	CODE
$\overline{I, P}$	L

STATE	CODE
DON'T CARE	–

"OR" ARRAY - (F), (N)



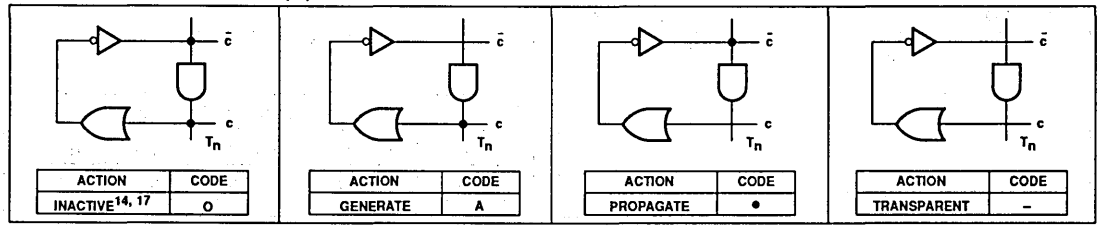
ACTION	CODE
INACTIVE[14, 16]	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	–

"COMPLEMENT" ARRAY - (C)



ACTION	CODE
INACTIVE[14, 17]	O

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

NOTES:
14. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates T_n.
15. Any gate T_n will be unconditionally inhibited if any one of ites I or P link pairs are left intact.
16. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
17. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

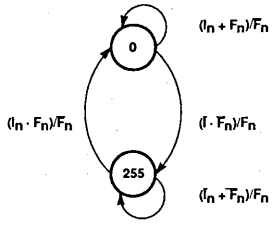
Field-Programmable Logic Sequencer (14 × 48 × 6) — PLS167

TEST ARRAY

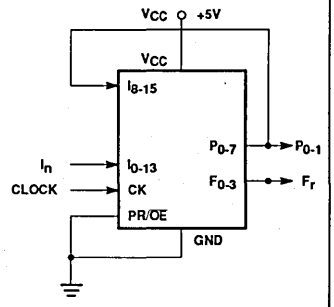
The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to $I_{0\text{-}13}$ as shown in the test circuit timing diagram.



State Diagram



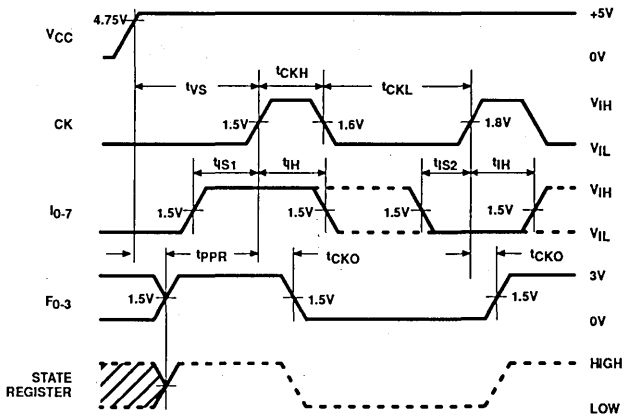
FPLS Under Test

TEST ARRAY PROGRAM

TERM	C	AND: INPUT (Im) 13 12 11 10 9 8 7 6 5 4 3 2 1 0	AND: PRESENT STATE (Ps) 7 6 5 4 3 2 1 0	OPTION (P/E) H — OR: NEXT STATE (Ns) 7 6 5 4 3 2 1 0	OR: OUTPUT (Fr) 3 2 1 0
48	A	H H H H H H H H H H H H H H	H H H H H H H H	L L L L L L L L	L L L L
49	•	L L L L L L L L L L L L L L	L L L L L L L L	H H H H H H H H	H H H H

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any Signetic's qualified programming equipment.



Test Circuit Timing Diagram

TEST ARRAY DELETED

TERM	C	AND: INPUT (Im) 13 12 11 10 9 8 7 6 5 4 3 2 1 0	AND: PRESENT STATE (Ps) 7 6 5 4 3 2 1 0	OPTION (P/E) H — OR: NEXT STATE (Ns) 7 6 5 4 3 2 1 0	OR: OUTPUT (Fr) 5 4 3 2 1 0
48	–	H H H H H H H H H H H H H H	H H H H H H H H	– – – – – – – –	– – – – – –
49	•	L L L L L L L L L L L L L L	L L L L L L L L	– – – – – – – –	– – – – – –

Test Array Deleted

Signetics

PLS168
Field Programmable Logic Sequencer (12 × 48 × 8)

Signetics Programmable Logic

Product Specification

Military
Customer Specific Products

DESCRIPTION

The PLS168 is a bipolar, programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip state and output registers. These consist respectively of 10 Q_p, and 4 Q_f edge-triggered, clocked S/R flip-flops, with an asynchronous preset option.

All flip-flops are unconditionally preset to "1" during power turn-on.

The AND array combines 12 external inputs, I_{0-11}, with 10 internal inputs, P_{0-9}, fed back from the State register to form up to 48 transition terms (AND terms). In addition, P_0-P_3 of the internal state register are brought off-chip to allow extending the output register to 8 bits, if so desired.

All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the log to high transition of the Clock pulse.

Both True and Complement transition terms can be generated by optional use of the internal variable (C) from the complement array. Also, if desired, the Preset input can be converted to output-enable function, as an additional user programmable option.

Order codes for this device are listed in the Ordering Information table.

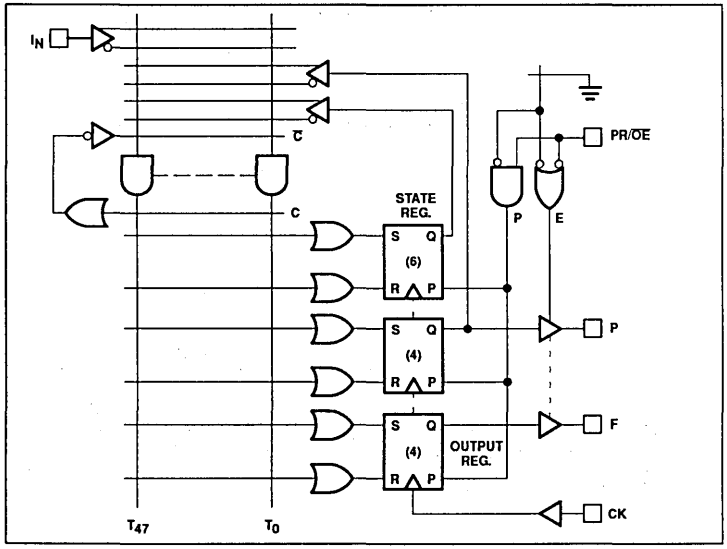
FEATURES

- Field-programmable (Ni-Cr link)
- 12 True/Complement buffered inputs
- 48 programmable AND gates
- 29 programmable OR gates
- 10-bit state register
- 4-bit shared state/output register
- 4-bit output register
- Transition complement array
- Programmable asynchronous preset/output enable
- Positive edge-trigger clock
- Power-on preset to logic "1" of all registers
- Automatic logic "HOLD" state via S/R flip-flops
- On-chip test array
- Power: 600mW
- TTL compatible
- 3-State outputs
- Single +5V supply
- 300mil-wide 24-pin DIP

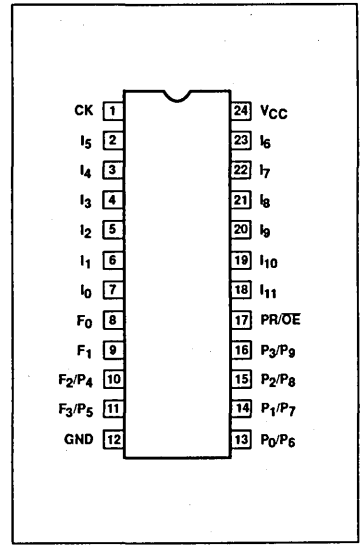
APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

FUNCTIONAL DIAGRAM



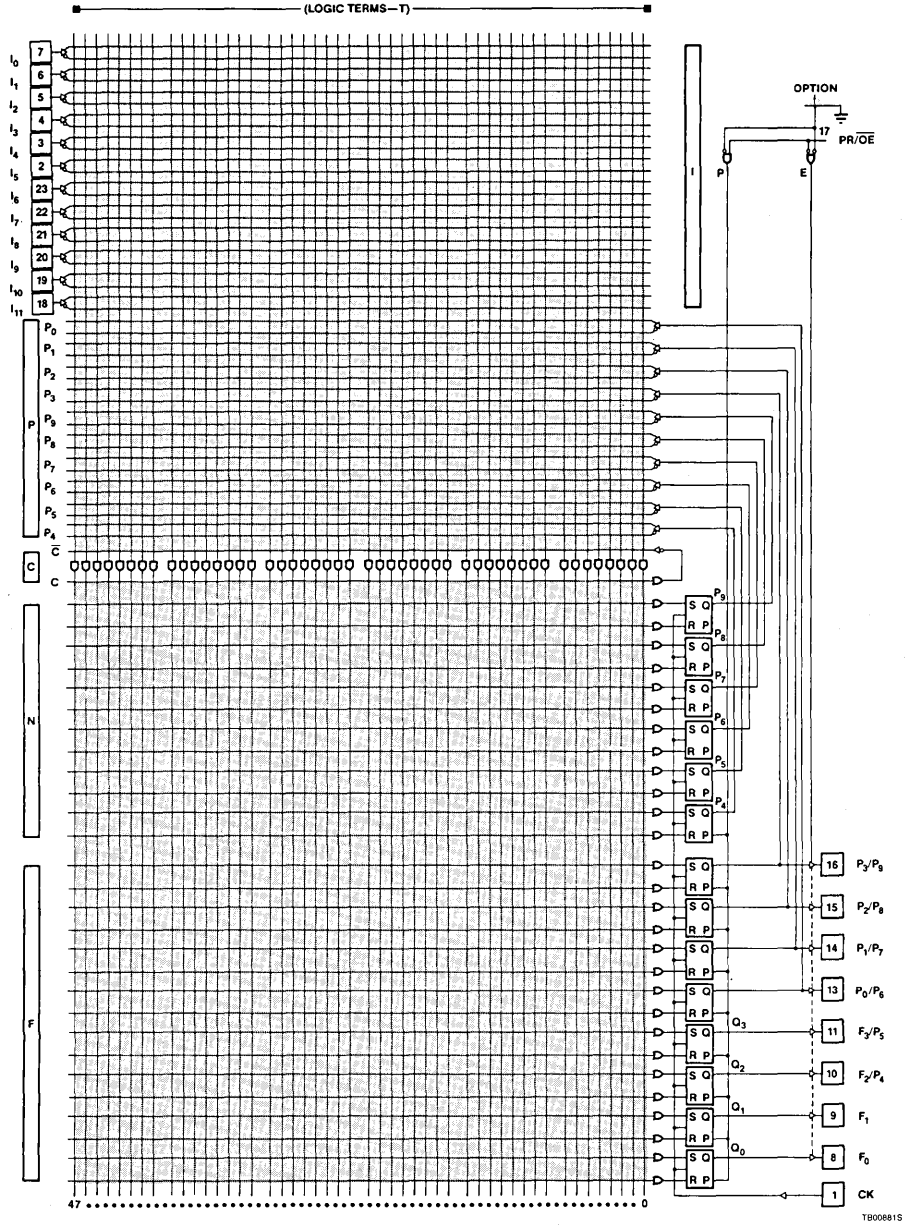
PIN CONFIGURATION



Field-Programmable Logic Sequencer (12 × 48 × 8)

PLS168

FPLS LOGIC DIAGRAM



NOTES:
1. All programmed "AND" gate locations are pulled to logic "1".
2. All programmed "OR" gate locations are pulled to logic "0".
3. ⊗ Programmable connection.

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP 300mil-wide	PLS168/BLA

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	**Clock:** The Clock input to the state and output registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2 - 7 18 - 23	I_{1-11}	**Logic Inputs:** The 11 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
7	I_0	**Logic/Diagnostic Input:** A 12th external logic input to the AND array, as above, when exercised with standard TTL levels. When I_0 is held at +10V, device outputs F_{2-3} and P_{0-3} reflect the contents of state register bits P_{4-9} (see Diagnostic Output Mode diagram on page 7). The contents of flip-flops P_{0-1} and F_{0-3} remain unaltered.	Active-High/Low
13 - 16	P_{0-3}	**Logic/Diagnostic Outputs:** Four device outputs which normally reflect the contents of state register bits P_{0-3}. When I_0 is held at +10V these pins reflect (P_6 - P_9).	Active-High
10 - 11	F_2 - F_3	**Logic/Diagnostic Outputs:** Two register bits (F_2 - F_3) which normally reflect output register bits (Q_2 - Q_3). When I_0 is held at +10V these pins reflect (P_4 - P_5).	Active-High
17	PR/$\overline{OE}$	**Preset or $\overline{\text{Output Enable}}$ Input:** A user programmable function: • **Preset:** Provides an asynchronous preset to logic "1" of all state and output register bits. Preset overrides Clock, and when held High, clocking is inhibited and P_{0-9} and F_{0-3} are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low. • **$\overline{\text{Output Enable}}$:** Provides an Output Enable function to all output buffers.	Active-High (H) Active-Low (L)
8, 9	F_0 - F_1	**Logic Output:** Two device outputs which reflect output registers Q_0 - Q_1. When I_0 is held at +10V F_0 - F_1 = Logic "1".	

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_I	Input voltage		+10.0	V_{DC}
V_O	Output voltage		+5.5	V_{DC}
I_I	Input currents	-30	+30	mA
I_O	Output currents		+100	mA
T_A	Operating Temperature range	-55	+125	°C
T_{STG}	Storage Temperature range	-65	+150	°C

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER[3]	TEST CONDITIONS[3]	LIMITS[3]			UNIT
			Min	Typ[2]	Max	
Input Voltage						
V_{IH}	High	V_{CC} = 5.5V	2			V
V_{IL}	Low	V_{CC} = 4.5V			0.8	V
V_{IK}	Clamp[4]	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output Voltage						
		V_{CC} = 4.5V				
V_{OH}	High[5]	I_{OH} = -2mA	2.4			V
V_{OL}	Low[6]	I_{OL} = 9.6mA		0.35	0.5	V
Input Current						
		V_{CC} = 5.5V				
I_{IH}	High	V_I = 5.5V		<1	50	µA
I_{IL}	Low	V_I = 0.45V		-10	-150	µA
I_{IL}	Low (CK input)	V_I = 0.45V		-50	-350	µA
Output Current						
		V_{CC} = 5.5V				
$I_{O(OFF)}$	Hi-Z state[7]	V_{CC} = 5.5V		1	60	µA
		V_O = 0.45V		-1	-60	µA
I_{OS}	Short circuit[4,8]	V_O = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = 5.5V		120	185	mA
Capacitance[7, 10]						
		V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		8	10	pF
C_{OUT}	Output	V_O = 2.0V		10	13	pF

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

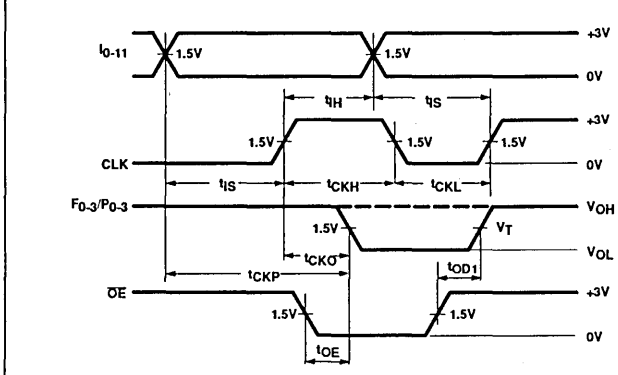
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
Pulse Width							
t_{CKH}	Clock[11] High	CK-	CK+	40	15		ns
t_{CKL}	Clock Low	CK+	CK-	40	15		ns
t_{CKP1}	Period (w/o C-array)	CK+	CK+	95	40		ns
t_{CKP2}	Period (w/C-array)[10]	CK+	CK+	135	60		ns
t_{PRH}	Preset pulse	PR+	PR-	40	15		ns
Setup Time							
t_{IS1}	Input	CK+	Input±	60			ns
t_{IS2}	Input (through Complement array)[12]	CK+	Input±	100			ns
t_{VS}	Power-on preset[10]	CK-	V_{CC}+	5	-10		ns
t_{PRS}	Preset[10]	CK-	PR-	5	-10		ns
Hold Time							
t_{IH}	Input[10]	Input±	CK+	10	-10		ns
Propagation Delay							
t_{CKO}	Clock	Output±	CK+		15	35	ns
t_{OE}	Output Enable	Output-	OE-		20	40	ns
t_{OD}	Output Disable	Output+	OE+		20	40	ns
t_{PR}	Preset	Output+	PR+		18	45	ns
t_{PPR}	Power-on preset	Output+	V_{CC}+		0	20	ns
Frequency of Operation							
f_{MAX}	w/o C-array					10.5	MHz
f_{MAX}^C	w/C-array[10]					7.4	MHz

NOTES:

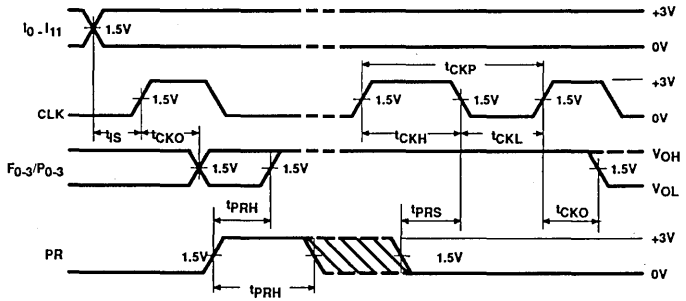
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{OE}$ and a logic High stored, or with V_{IH} applied to PR.
6. Measured with a programmed logic condition for which the output is at a Low logic level, and V_{IL} applied to PR/$\overline{OE}$ Output sink current is applied through a resistor to V_{CC}.
7. Measured with V_{IH} applied to PR/$\overline{OE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the PR/$\overline{OE}$ input grounded, all other inputs at 4.5V, ant the outputs open.
10. Guaranteed, but not tested.
11. To prevent spurious clocking, clock rise time (10% - 90%) ≤ 30ns.
12. Not testable on unprogrammed devices.

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

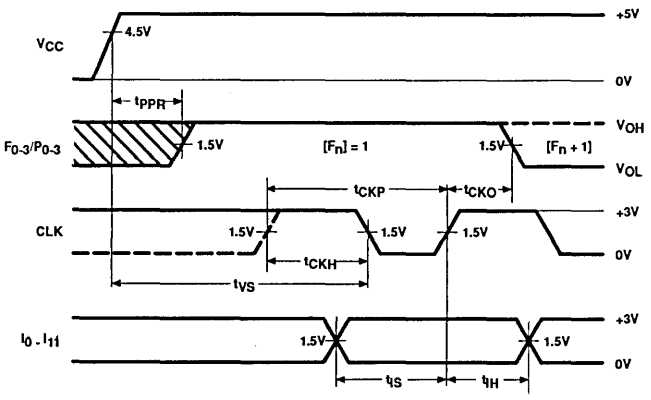
TIMING DIAGRAMS



Sequential Mode



Asynchronous Preset



Power-On Preset

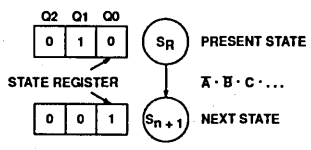
TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP1}	Clock period - when not using Complement Array.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{CKP2}	Clock period - when using Complement Array.
t_{IS2}	Required delay between beginning of valid input and positive transition of clock, when using optional Complement array (two passes necessary through the AND array).
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of clock preceding first reliable clock pulse.
t_{PRS}	Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse.
t_{IH}	Required delay between positive transition of clock and end of valid input data.
t_{CKO}	Delay between positive transition of clock and when Outputs become valid (with PR/$\overline{OE}$ Low).
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-State.
t_{PR}	Delay between positive transition of Preset and when Outputs become valid at "1".
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{PRH}	Width of preset input pulse.
f_{MAX}	Maximum clock frequency.

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

LOGIC FUNCTION

Typical State Transition:



SET Q_0: $S_0 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. PR/$\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
2. All transition terms are disabled (0).
3. All S/R flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.
   NOTE: The Test Array pattern must be deleted before incorporating a user program. This is accomplished automatically by any Signetics qualified programming equipment.

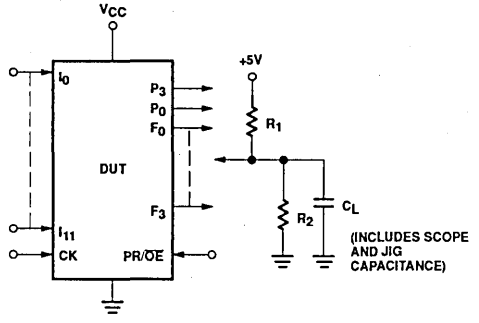
TRUTH TABLE[1, 2, 3, 4, 5, 6]

V_{CC}	OPTION PR	OPTION $\overline{OE}$	I_0	CK	S	R	$Q_{P/F}$	F
	H		•	X	X	X	H	H
	L		+10V	X	X	X	Q_n	$(Q_P)_n$
	L		X	X	X	X	Q_n	$(Q_F)_n$
		H	•	X	X	X	Q_n	Hi-Z
+5V		L	+10V	X	X	X	Q_n	$(Q_P)_n$
		L	X	X	X	X	Q_n	$(Q_F)_n$
		L	X	↑	L	L	Q_n	$(Q_F)_n$
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

NOTES:
1. Positive Logic $S/R = T_0 + T_1 + T_2 + \ldots + T_{47}$
   $T_n = C(I_0\, I_1\, I_2 \ldots)(P_0\, P_1 \ldots P_8)$
2. Either Preset (Active-High) or Output Enable (active-Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.
5. • = H/L/+10V.
6. X = Don't Care (≤ 5.5V).

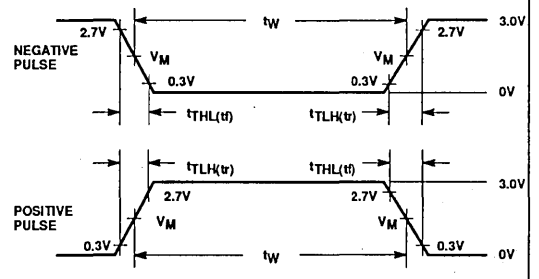
Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

TEST LOAD CIRCUITS



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF.

VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

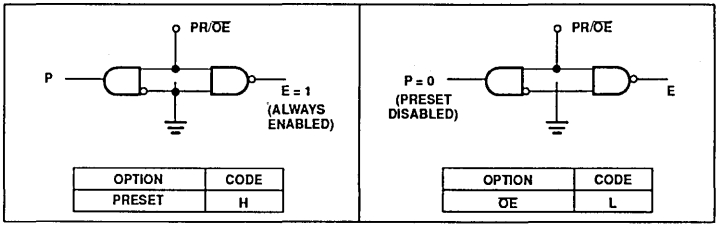
LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR gate input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Table on the following page.

In this table, the logic state or action of control variables C, I, P, N and F, associated with each Transition term T_n is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

PRESET/$\overline{OE}$ OPTION – (P/E)



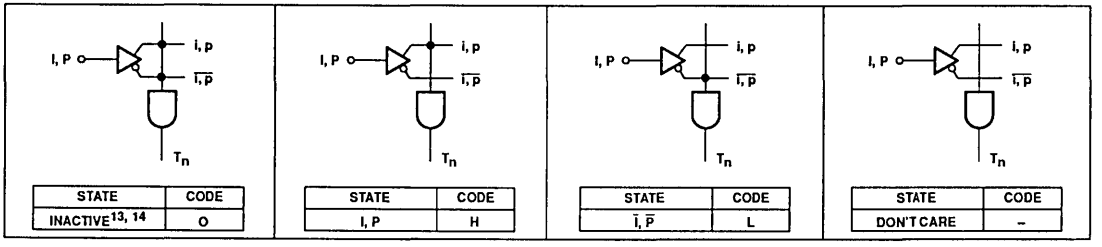
OPTION	CODE
PRESET	H

OPTION	CODE
$\overline{OE}$	L

PROGRAMMING:

The PS168 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (state and output register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

"AND" ARRAY – (I), (P)



STATE	CODE
INACTIVE[13, 14]	O

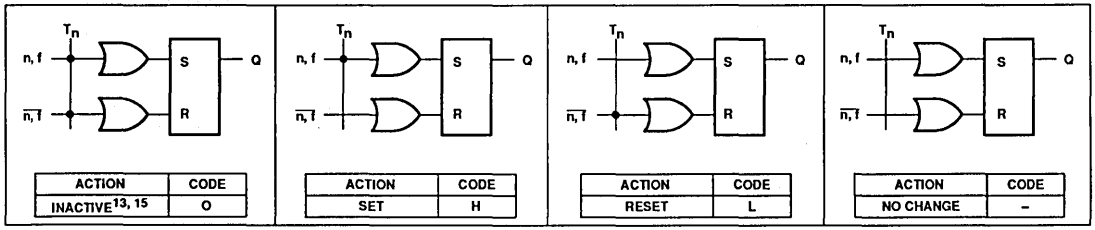
STATE	CODE
I, P	H

STATE	CODE
$\overline{I, P}$	L

STATE	CODE
DON'T CARE	–

Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

"OR" ARRAY – (N), (F)



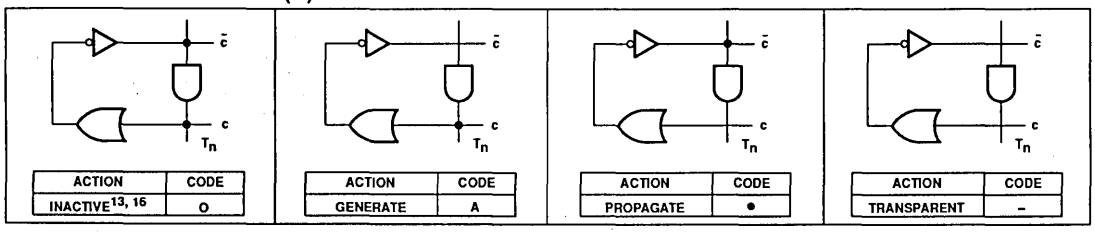
ACTION	CODE
INACTIVE[13, 15]	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	–

"COMPLEMENT" ARRAY – (C)



ACTION	CODE
INACTIVE[13, 16]	O

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

NOTES:
13. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates T_n.
14. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs are left intact.
15. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
16. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.

Field-Programmable Logic Sequencer (12 × 48 × 8)

PLS168

FPLS PROGRAM TABLE PLS168

CUSTOMER NAME _____

SIGNETICS DEVICE # _____

PROGRAM TABLE # _____

REV _____

DATE _____

AND			OR	
INACTIVE	O	C_n	INACTIVE	O	$N_s \cdot F_r$
GENERATE	A		SET	H	
PROPAGATE	+		RESET	L	
TRANSPARENT	–		NO CHANGE	–	
INACTIVE	O	$I_m \cdot P_s$	OPTION		
I, P	H		PRESET	H	P/E
I, P	L		OE	L	
DON'T CARE	–				

TERM	C_n	INPUT(Im) 11 10 9 8 7 6 5 4 3 2 1 0	PRESENT STATE (Ps) (Pz) 9 8 7 6 5 4 3 2 1 0	REMARKS	AND / OPTION (P/E) / OR — NEXT STATE (Ns) (Pz) 9 8 7 6 5 4	OUTPUT (Fr) 3 2 1 0	OUTPUT (Fr) 3 2 1 0
0							
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
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41							
42							
43							
44							
45							
46							
47							
PIN NO.		18 19 20 21 22 23 2 3 4 5 6 7				16 15 14 13 11 10 9 8	
VARIABLE NAME							

TB00891S

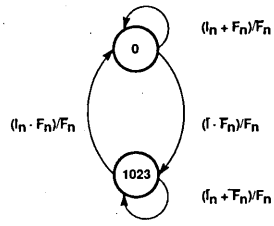
Field-Programmable Logic Sequencer (12 × 48 × 8) PLS168

TEST ARRAY

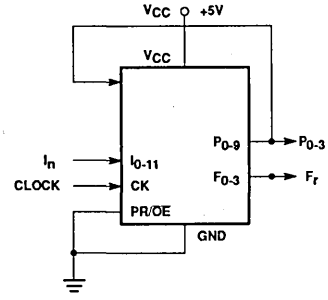
The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to $I_{0\text{-}13}$ as shown in the test circuit timing diagram.



State Diagram



FPLS Under Test

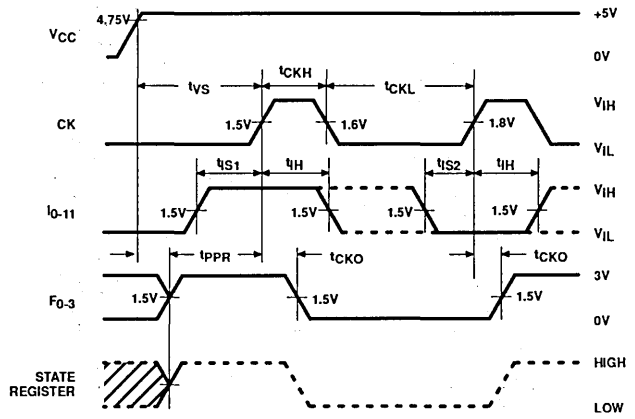
TEST ARRAY PROGRAM

TERM	C_n	AND: INPUT (In) 11 10	9	8	7	6	5	4	3	2	1	0	AND: PRESENT STATE (Ps) 9	8	7	6	5	4	3	2	1	0
48	A	H H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	•	L L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)	H
OR	
NEXT STATE (Ns) 9 8 7 6 5 4 3 2 1 0	OUTPUT (Fr) 3 2 1 0
L L L L L L L L L L	L L L L
H H H H H H H H H H	H H H H

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any Signetic's qualified programming equipment.



Test Circuit Timing Diagram

TEST ARRAY DELETED

TERM	C_n	AND: INPUT (In) 11 10	9	8	7	6	5	4	3	2	1	0	AND: PRESENT STATE (Ps) 9	8	7	6	5	4	3	2	1	0
48	–	H H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	•	L L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)	H
OR	
NEXT STATE (Ns) 9 8 7 6 5 4 3 2 1 0	OUTPUT (Fr) 3 2 1 0
– – – – – – – – – –	– – – –
– – – – – – – – – –	– – – –

Test Array Deleted

Signetics

PLS173
Field-Programmable Logic Array (22 × 42 × 10)

Signetics Programmable Logic

Product Specification

Military
Application Specific Products

DESCRIPTION

The PLS173 is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

On chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS173 is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-pin Ceramic DIP 300mil-wide	PLS173/BLA

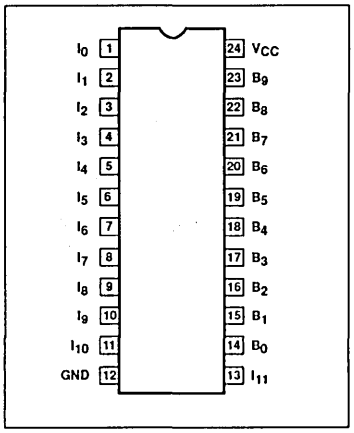
FEATURES

- Field-Programmable (Ni-Cr links)
- 12 inputs
- 42 AND gates
- 10 OR gates
- 10 bidirectional I/O lines
  - 32 Logic Terms
  - 10 Control Terms
- Power dissipation: 750mW (typ)
- Output: 3-State
- TTL compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

PIN CONFIGURATION



LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots$

TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY = L

$\overline{Z} = \overline{P0} + \overline{P1} + \overline{P2} + \ldots$

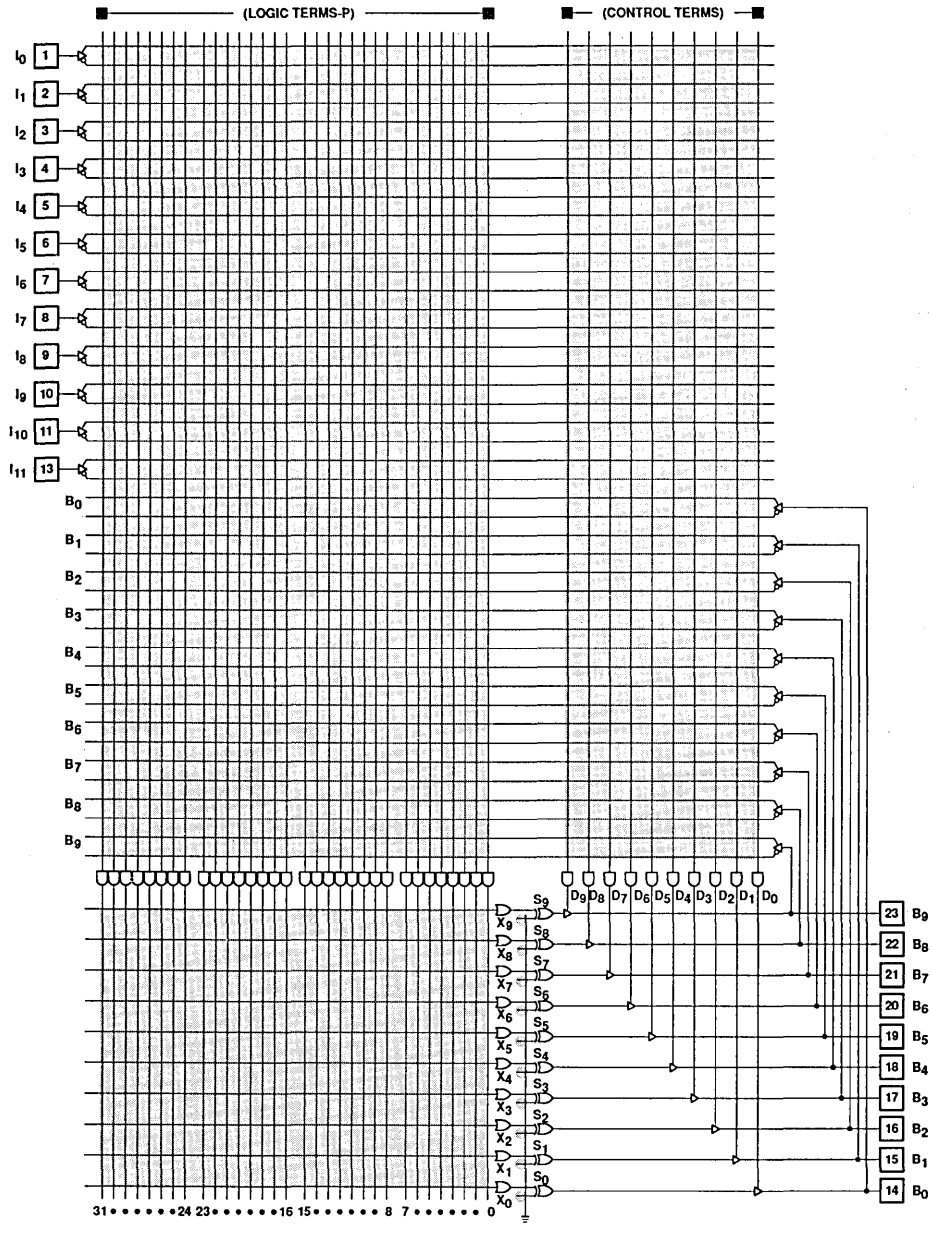
$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:

1. For each of the 10 outputs, either function Z (active-high) or $\overline{Z}$ (active-low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C, etc., are user defined connections to fixed inputs (I) and bidirectional pins (B).

Field-Programmable Logic Array (22 × 42 × 10) — PLS173

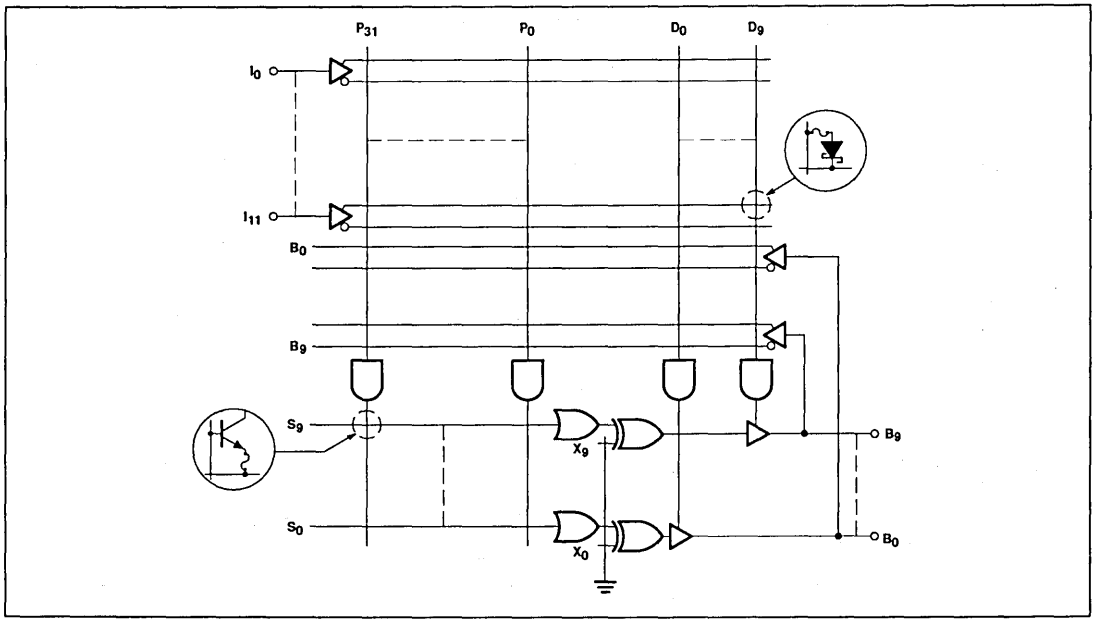
FPLA LOGIC DIAGRAM



NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. ◌ Programmable connection.

Field-Programmable Logic Array (22 × 42 × 10) — PLS173

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_I	Input voltage		+10.0	V_{DC}
V_O	Output voltage		+5.5	V_{DC}
I_I	Input currents	-30	+30	mA
I_O	Output currents		+100	mA
T_A	Operating temperature range	-55	+125	°C
T_{STG}	Storage temperature range	-65	+150	°C

Field-Programmable Logic Array (22 × 42 × 10) — PLS173

DC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER[3]	TEST CONDITIONS[3]	LIMITS[3]			UNIT
			Min	Typ[2]	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.5V			.80	V
V_{IH}	HIgh	V_{CC} = 5.5V	2.0			V
V_{IK}	Clamp[4]	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage						
		V_{CC} = 4.5V				
V_{OL}	Low[5]	I_{OL} = 12mA			0.5	V
V_{OH}	High[6]	I_{OH} = -2mA	2.4			V
Input current						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			50	µA
Output current						
		V_{CC} = 5.5V				
$I_{O(OFF)}$	Hi-Z state[10]	V_O = 5.5V			110	µA
		V_O = 0.45V			-210	µA
I_{OS}	Output short circuit[4,6,7]	V_O = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = 5.5V		150	170	mA
Capacitance[11]						
		V_{CC} = 5.0V				
C_I	Input	V_I = 2.0V		8	12	pF
C_B	I/O	V_B = 2.0V		15	19	pF

AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
t_{PD}	Propagation Delay	Output±	Input±	C_L = 50pF		20	40	ns
t_{OE}	Output Enable[12]	Output-	Input±	C_L = 50pF		20	35	ns
t_{OD}	Output Disable[9,12]	Output+	Input±	C_L = 50pF		20	35	ns

NOTES:

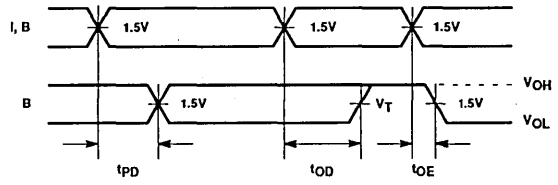
1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with Pins 1 - 5 = 0V, Pins 6 - 10 = 4.5V, Pin 11 = 0V and Pin 13 = 10V.
6. Same conditions as Note 5, except Pin 11 = +10V.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with I_0 and I_1 = 0V and I_2 - I_{11} and B_0 - B_9 = 4.5V. Part in Virgin State.
9. Measured at V_T = V_{OL} + 0.5V.
10. Leakage values are a combination of input and output leakage.
11. Guaranteed, but not tested.
12. Guaranteed but not tested in unprogrammed devices.

Field-Programmable Logic Array (22 × 42 × 10) — PLS173

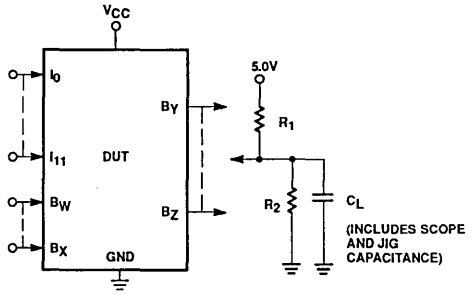
TIMING DEFINITIONS

SYMBOL	PARAMETER
T_{PD}	Propagation delay between input and output.
T_{DD}	Delay between input change and when output is off (Hi-Z or High).
T_{DE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM

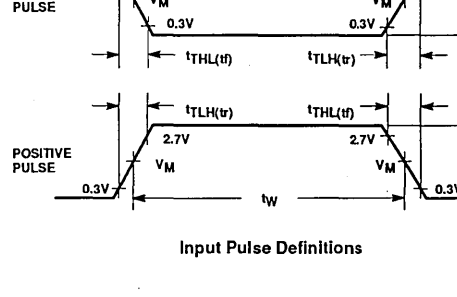


TEST LOAD CIRCUIT



NOTE: R_1 = 470Ω, R_2 = 1KΩ, C_L = 50pF.

VOLTAGE WAVEFORM



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Field-Programmable Logic Array (22 × 42 × 10) — PLS173

LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

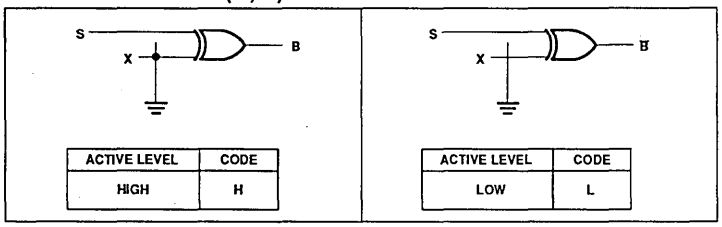
With Logic programming, the AND/OR/EX-OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table on the following page.

In this table, the logic state of variables I, P and B, associated with each Sum Term S is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

CAUTION: PLS173 TEST COLUMNS

The PLS173 incorporates two columns not shown in the logic block diagram. These columns are used for in-house testing of the device in the unprogrammed state. These columns must be disabled prior to using the PLS173 in your application. If you are using a Signetics approved programmer, the disabling is accomplished during the device programming sequence. If these columns are not disabled, abnormal operation is possible.

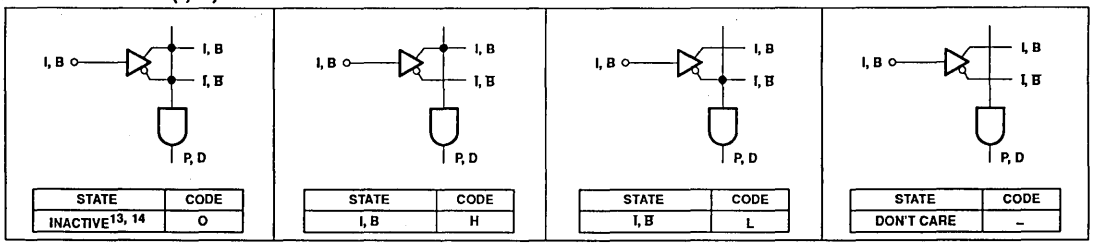
OUTPUT POLARITY - (O, B)



ACTIVE LEVEL	CODE
HIGH	H

ACTIVE LEVEL	CODE
LOW	L

"AND" ARRAY - (I, B)



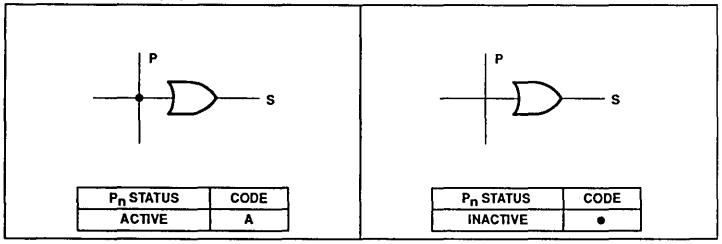
STATE	CODE
INACTIVE[13, 14]	O

STATE	CODE
I, B	H

STATE	CODE
I, B̄	L

STATE	CODE
DON'T CARE	–

"OR" ARRAY - (B)



P_n STATUS	CODE
ACTIVE	A

P_n STATUS	CODE
INACTIVE	•

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

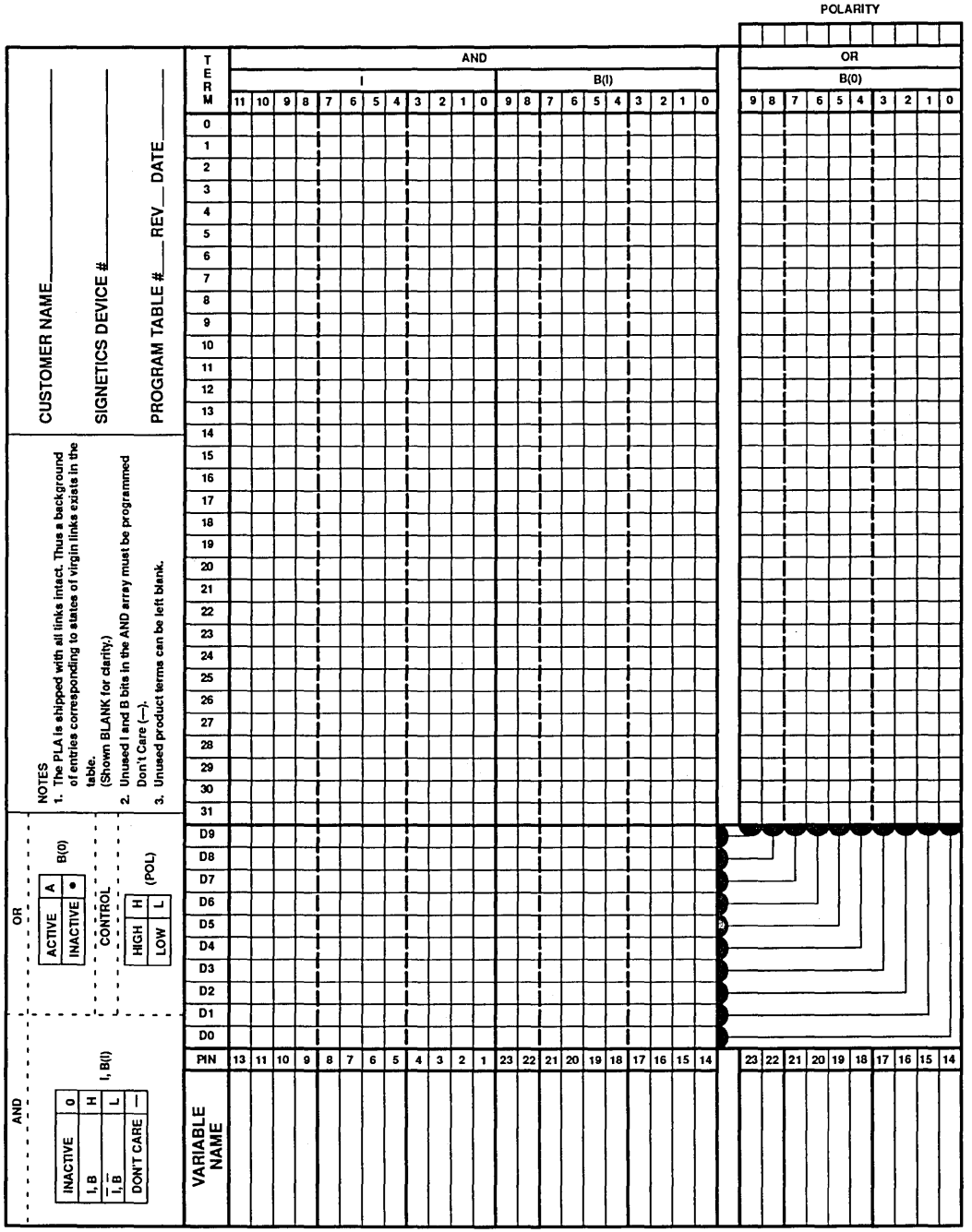
NOTES:

13. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n, D_n.
14. Any gate P_n, D_n will unconditionally inhibited if any one its (I, B) link pairs is left intact.

Field-Programmable Logic Array (22 × 42 × 10)

PLS173

FPLA PROGRAM TABLE

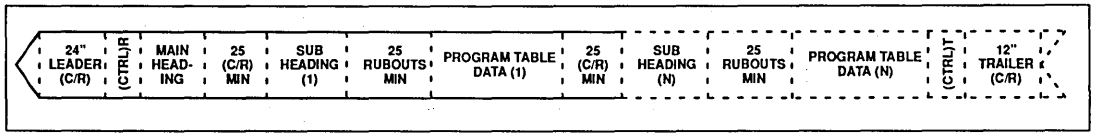


Field-Programmable Logic Array (22 × 42 × 10) PLS173

TWX TAPE CODING (LOGIC FORMAT)

The FPLA Program Table can be sent to Signetics in ASCII code format via airmail using any type of 8-level tape (paper, mylar, fanfold, etc.), or via TWX: just dial (910) 339-9283, tell the operator to turn the paper puncher on, and acknowledge. At the end of transmission instruct the operator to send tape to Signetics Order Entry.

A number of Program Tables can be sequentially assembled on a continuous tape as follows, however, limit tape length to a roll of 1.75 inch inside diameter and 4.25 outside diameter.



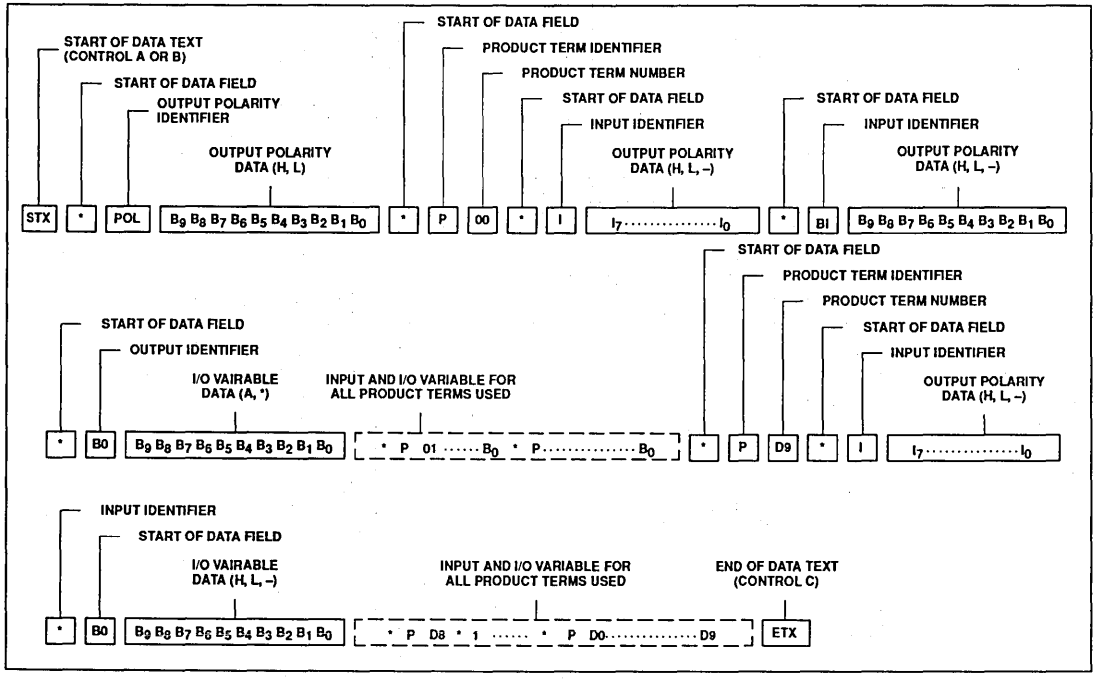
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

___1. Customer Name_____
___2. Customer TWX No._____
___3. Date_____
___4. Purchase Order No._____
___5. Number of Program Tables_____
___6. Total Number of Parts_____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

___1. Signetics Device No._____
___2. Program Table No._____
___3. Revision_____
___4. Date_____
___5. Customer Symbolized Part No._____
___6. Number of Parts_____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of output polarity, product term, and output information separated by appropriate identifiers in accordance with the following format. Entries for the data fields correspond to those defined in the Logic PROGRAM TABLE:



Signetics

PLS179

Field Programmable Logic Sequencer (20 × 45 × 12)

Product Specification

Military Standard Products

DESCRIPTION

The PLS179 is a 3-State output, registered logic element combining AND/OR gate arrays with clocked J-K flip-flops. These J-K flip-flops are dynamically convertible to D-type via a "foldback" inverting buffer and control gate F_C. It features 8 registered I/O outputs (F) in conjunction with 4 bidirectional I/O lines (B). There are 8 dedicated inputs. These yield variable I/O gate and register configurations via control gates (D, L) ranging from 20 inputs to 12 outputs.

The AND/OR arrays consist of 32 logic AND gates, 13 control AND gates, and 21 OR gates with fusible link connections for programming I/O polarity and direction. All AND gates are linked to 8 inputs (I), bidirectional I/O lines (B), internal flip-flop outputs (Q), and Complementary Array output ($\overline{C}$). The Complementary Array consists of a NOR gate optionally linked to all AND gates for generating and propagating complementary AND terms.

APPLICATIONS

- Random sequential logic
- Synchronous Up/Down counters
- Shift Registers
- Bidirectional data buffers
- Timing function generators
- System controllers/synchronizers
- Priority encoder/registers

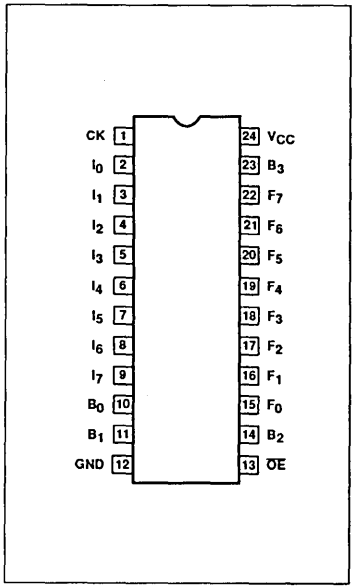
FEATURES

- Field-programmable (Ni-Cr link)
- 8 dedicated inputs
- 13 control gates
- 32 AND gates
- 21 OR gates
- 45 product terms:
  - 32 logic terms
  - 13 control terms
- 4 bidirectional I/O lines
- 8 bidirectional registers
- J/K, T, or D-type flip-flops
- Asynchronous Preset/Reset
- Complement Array
- Active high or low outputs
- Programmable $\overline{OE}$ control
- Positive edge triggered clock
- Power-on reset on flip-flop (Fn = "1")
- Power dissipation: 725mW (typ)
- TTL Compatible

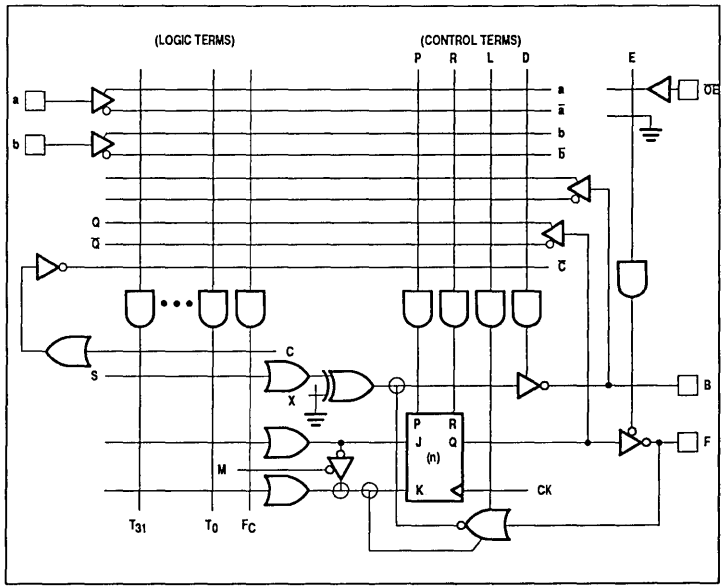
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP 300-mil wide	PLS179/BLA

PIN CONFIGURATION



FUNCTIONAL DIAGRAM



Field Programmable Logic Sequencer (20 × 45 × 12) — PLS179

On-chip T/C buffers couple either True (I, B, Q) or Complement ($\overline{I}$, $\overline{B}$, $\overline{Q}$, $\overline{C}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. One group of AND gates drives bidirectional I/O lines (B), whose output polarity is individually programmable through a set of EX-OR gates for implementing AND-OR or AND-NOR logic functions. Another group drives the J-K inputs of all flip-flops, as well as asynchronous Preset and Reset lines (P, R).

All flip-flops are positive edge-triggered and can be used as input, output or I/O (for interfacing with a bidirectional data bus) in conjunction with load control gates (L), steering inputs (I), (Q) and programmable output select lines (E).

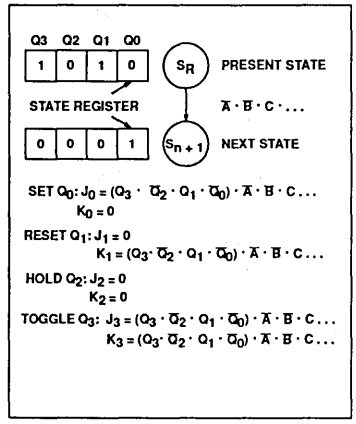
The PLS179 is field-programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

VIRGIN STATE

The factory shipped virgin device contains all fusible links intact, such that:

1. $\overline{OE}$ is always enabled.
2. Preset and Reset are always disabled.
3. All transition terms are disabled.
4. All flip-flops are in D-mode.
5. All B pins are inputs and all F pins are outputs.

LOGIC FUNCTION



NOTE:
Similar logic functions are applicable for D and T mode flip-flops.

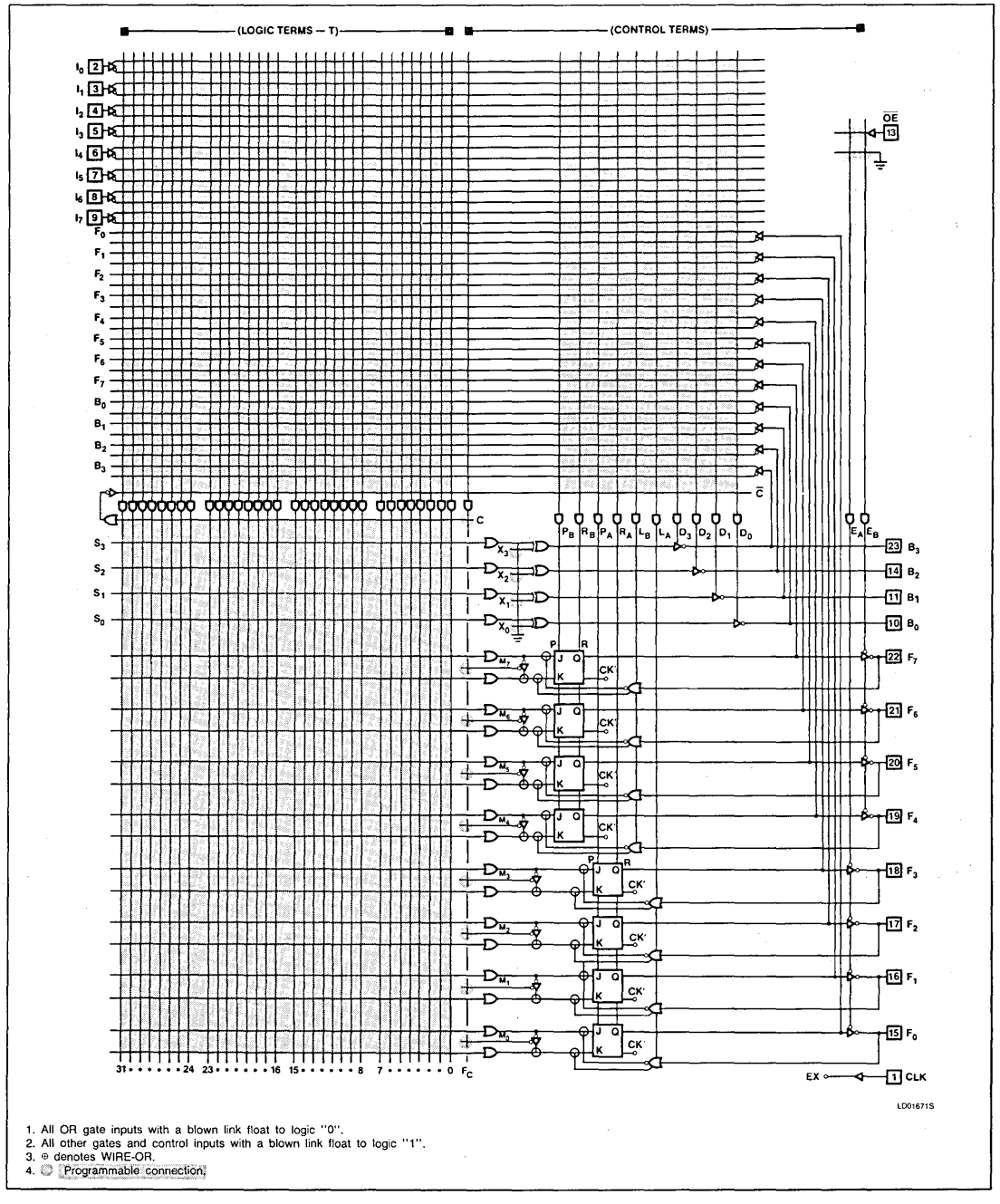
FLIP-FLOP TRUTH TABLE

$\overline{OE}$	L	CK	P	R	J	K	Q	F
H								H/Hi-Z
L	X	X	L	X	X	X	L	H
L	X	X	H	L	X	X	H	L
L	X	X	L	H	X	X	L	H
L	L	↑	L	L	L	L	Q	$\overline{Q}$
L	L	↑	L	L	L	H	L	H
L	L	↑	L	L	H	L	H	L
L	L	↑	L	L	H	H	$\overline{Q}$	Q
H	H	↑	L	L	L	H	L	H*
H	H	↑	L	L	H	L	H	L*
+10V	X	↑	X	X	L	H	L	H**
	X	↑	X	X	H	L	H	L**

NOTES:

1. Positive Logic:
   $J/K = T_0 + T_1 + T_2 + \ldots + T_{31}$
   $T_n = \overline{C} \cdot (I_0 \cdot I_1 \cdot I_2 \ldots) \cdot (Q_0 \cdot Q_1 \ldots) \cdot (B_0 \cdot B_1 \ldots)$
2. ↑ denotes transition for Low to High level.
3. X = Don't care
4. * = Forced at F_n pin for loading J/K flip-flop in I/O mode. L must be enabled, and other active T_R disabled via steering input(s) I, B, or Q.
5. At P = R = H, Q = H. The final state of Q depends on which is released first.
6. ** = Forced at F_n pin to load J/K flip-flop independent of program code (Diagnostic mode).

FPLS LOGIC DIAGRAM



1. All OR gate inputs with a blown link float to logic "0".
2. All other gates and control inputs with a blown link float to logic "1".
3. ⊕ denotes WIRE-OR.
4. ○ Programmable connection.

Field Programmable Logic Sequencer (20 × 45 × 12) PLS179

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_I	Input voltage	+10.0	V_{DC}
V_O	Output voltage	+5.5	V_{DC}
I_I	Input currents	-30 to +30	mA
I_O	Output currents	+100	mA
t_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}[15]	High-level input voltage	2.2			V
V_{IL}[15]	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2	mA
I_{OL}	Low-level output current			10.0	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C, 4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER[3]	TEST CONDITIONS[3]	LIMITS[3]			UNIT
			Min	Typ[2]	Max	
V_{IK}	Clamp Voltage	V_{CC} = Min, $I_I = I_{IK}$		-0.8	-1.2	V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = Max		0.35	0.5	V
V_{OH}	High-level output voltage	I_{OH} = Max	2.4			V
		V_{CC} = Max				
I_{IL}	Low-level output current	V_I = 0.45V		<1.0	-100	µA
I_{IL}	Low-level output current (CK input)	V_I = 0.45V		-10	-250	µA
I_{IH}	High-level output current	V_I = 5.5V		-50	40	µA
		V_{CC} = Max				
$I_{O(OFF)}$	Hi-Z State output current[5, 8]	V_O = 5.5V		1	80	µA
		V_O = 0.45V[14]			-140	µA
I_{OS}	Short circuit output current[4, 6]	V_O = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = Max		145	210	mA
		V_{CC} = Nom				
C_{IN}	Input capacitance[9]	V_I = 2.0V		8	12	pF
C_{OUT}	Output capacitance[9]	V_O = 2.0V		15	19	pF

Field Programmable Logic Sequencer (20 × 45 × 12) — PLS179

AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

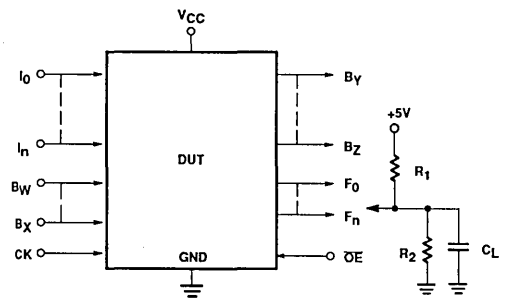
SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min[13]	Typ[2]	Max	
Pulse Width								
t_{CKH}	Clock high[10]	CK-	CK+		25	15		ns
t_{CKL}	Clock low	CK+	CK-	C_L = 50pF	25	15		ns
t_{CKP}	Period[12]	CK+	CK+		65	45		ns
t_{PRH}[14]	Preset/Reset pulse	(I,B)+	(I,B)-		45	30		ns
Setup Time								
t_{IS1}	Input	CK+	(I,B)±		40	30		ns
t_{IS2}	Input (through F_n)	CK+	F±	C_L = 50pF	25	10		ns
t_{IS3}[14]	Input (through Complement array)[12]	CK+	(I,B)±		65	45		ns
Hold Time								
t_{IH1}	Input	CK+	(I,B)±	C_L = 50pF	0	-5		ns
T_{IH2}[14]	Input (through F_n)	CK+	F±		15	10		ns
Propagation Delay								
t_{CKO}	Clock	F±	CK+			15	25	ns
t_{OE1}[14]	Output enable	F-	$\overline{OE}$-			20	35	ns
t_{OD1}[14]	Output disable[11]	F+	$\overline{OE}$+			20	35	ns
t_{PD}	Output	B±	(I,B)±			25	40	ns
t_{OE2}[14]	Output enable	B±	(I,B)+	C_L = 50pF		20	40	ns
t_{OD2}[14]	Output disable[11]	B+	(I,B)-			20	40	ns
t_{PRO}[14]	Preset/Reset	F±	(I,B)+			35	50	ns
t_{PPR}	Power-on preset	F-	V_{CC}+			0	20	ns

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_A = +25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured at V_{IH} applied to $\overline{OE}$.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with the $\overline{OE}$ input grounded, all other inputs at 4.5V, and the outputs open.
8. Leakage values are a combination of input and output leakage.
9. Guaranteed, but not tested.
10. To prevent spurious clocking, clock rise time (10% - 90%) ≤ 10ns.
11. Measured at $V_T = V_{OL} + 0.5V$.
12. When using the Complement Array T_{CKP} = 85ns (min.).
13. Limits are guaranteed with 12 product terms maximum connected to each sumterm line.
14. Not tested on an unprogrammed device.
15. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.

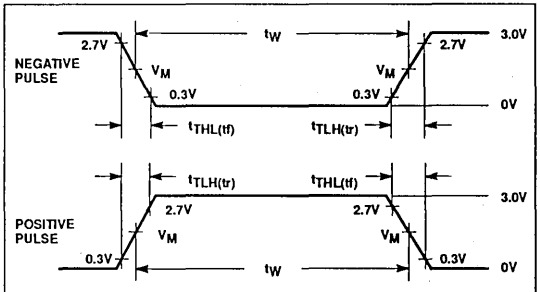
Field Programmable Logic Sequencer ($20 \times 45 \times 12$) PLS179

TEST LOAD CIRCUIT



NOTE: $R_1 = 470\Omega$, $R_2 = 1K\Omega$, $C_L = 50pF$.

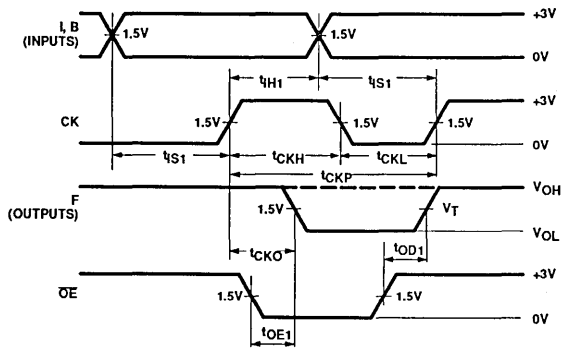
VOLTAGE WAVEFORM



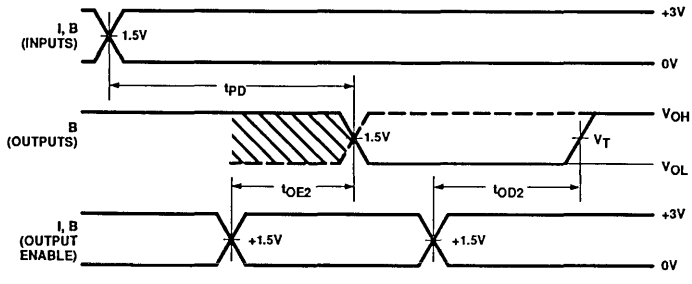
Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

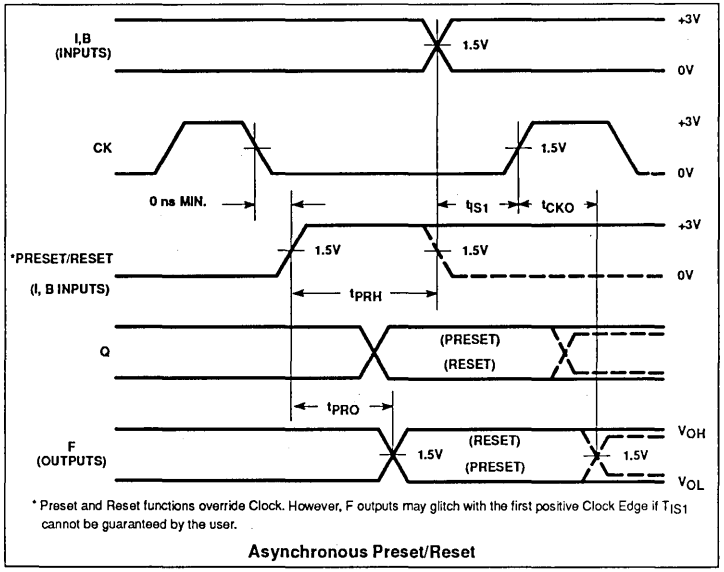
TIMING DIAGRAMS



Flip-Flop Outputs

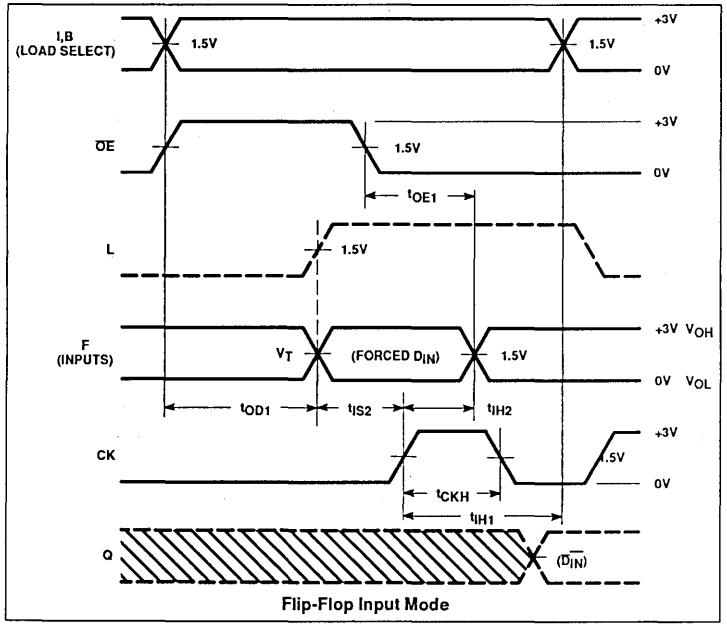


Gate Outputs



* Preset and Reset functions override Clock. However, F outputs may glitch with the first positive Clock Edge if T_{IS1} cannot be guaranteed by the user.

Asynchronous Preset/Reset



Flip-Flop Input Mode

MEMORY TIMING DEFINITIONS

t_{CKH}	Width of input clock pulse.
t_{CKL}	Interval between clock pulses.
t_{CKP}	Clock period.
t_{PRH}	Width of preset input pulse.
t_{IS1}	Required delay between beginning of valid input and positive transition of clock.
t_{IS2}	Required delay between beginning of valid input forced at flip-flop output pins, and positive transition of clock.
t_{IH1}	Required delay between positive transition of clock and end of valid input data.
t_{IH2}	Required delay between positive transition of clock and end of valid input data forced at flip-flop output pins.
t_{CKO}	Delay between positive transition of clock and when Outputs become valid (w/$\overline{OE}$ low).
t_{OE1}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{OD1}	Delay between beginning of Output Enable High and when Outputs are in the off state.
t_{PD}	Propagation delay between combinational inputs and outputs.
t_{OE2}	Delay between predefined Output Enable High, and when combinational Outputs become valid.
t_{OD2}	Delay between predefined Output Enable Low and when combinational Outputs are in the off state.
t_{PRO}	Delay between positive transition of predefined Preset/Reset input, and when flip-flop outputs become valid.

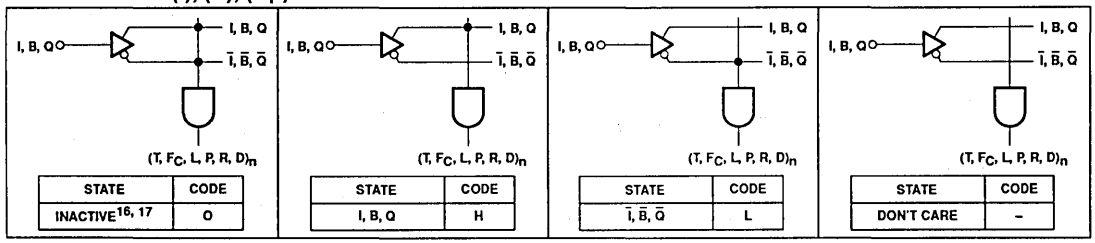
Field Programmable Logic Sequencer (20 × 45 × 12) — PLS179

The FPLS can be programmed by means of Logic Programming equipment.

With Logic Programming, the AND/OR-EX-OR input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Tables on the following pages.

In these Tables, the logic state or action of all I/O, control and state variables are assigned a symbol which results in the proper fusing pattern of corresponding links defined as follows:

"AND" ARRAY - (I), (B), (Qp)



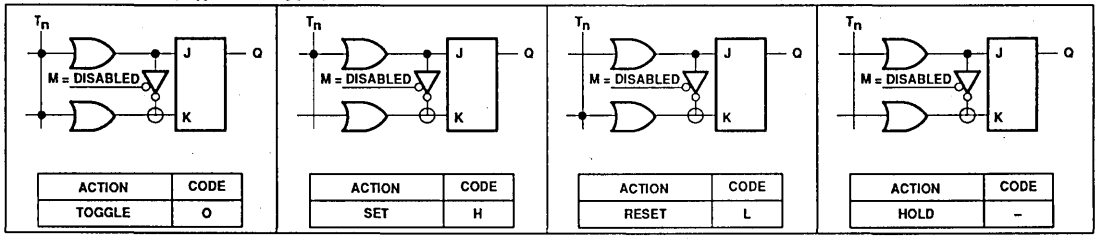
STATE	CODE
INACTIVE[16, 17]	0

STATE	CODE
I, B, Q	H

STATE	CODE
$\bar{I}, \bar{B}, \bar{Q}$	L

STATE	CODE
DON'T CARE	–

"AND" ARRAY - (Q_N = J-K Type)



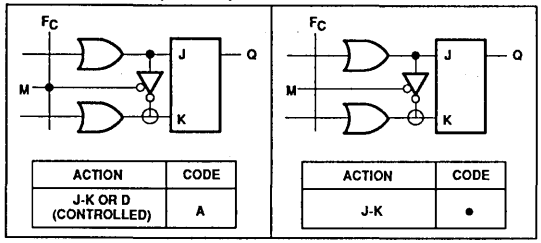
ACTION	CODE
TOGGLE	0

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
HOLD	–

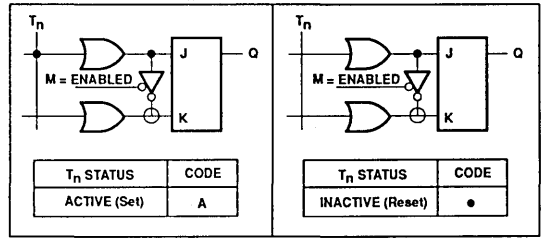
"OR" ARRAY - (MODE)



ACTION	CODE
J-K OR D (CONTROLLED)	A

ACTION	CODE
J-K	•

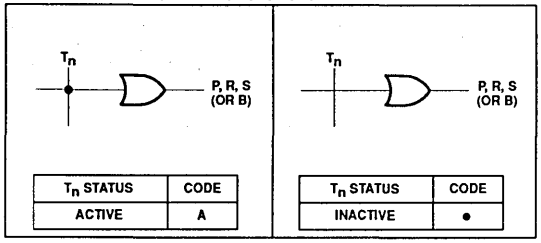
"OR" ARRAY - (Q_n = D-Type)



T_n STATUS	CODE
ACTIVE (Set)	A

T_n STATUS	CODE
INACTIVE (Reset)	•

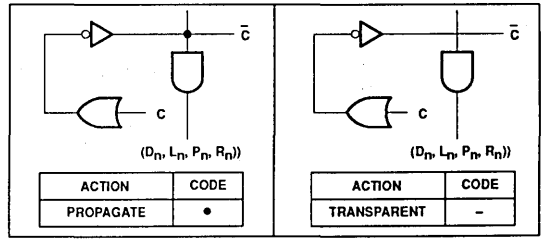
"OR" ARRAY - (S or B), (P), (R)



T_n STATUS	CODE
ACTIVE	A

T_n STATUS	CODE
INACTIVE	•

"COMPLEMENT" ARRAY - MODE

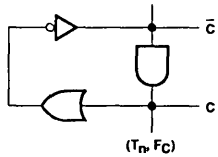


ACTION	CODE
PROPAGATE	•

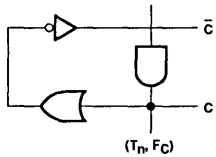
ACTION	CODE
TRANSPARENT	–

Field Programmable Logic Sequencer (20 × 45 × 12) — PLS179

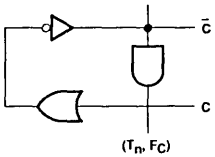
"COMPLEMENT" ARRAY - (C)



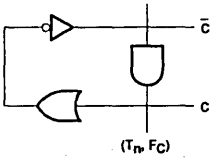
ACTION	CODE
INACTIVE[16, 18, 20]	O



ACTION	CODE
INACTIVE[20]	A

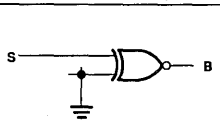


ACTION	CODE
PROPAGATE	•

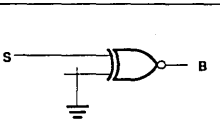


ACTION	CODE
TRANSPARENT	–

"EX-OR" ARRAY - (B)

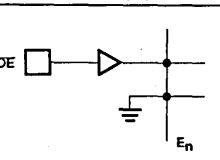


POLARITY	CODE
LOW	L

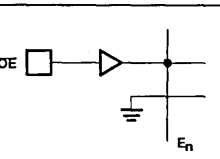


POLARITY	CODE
HIGH	H

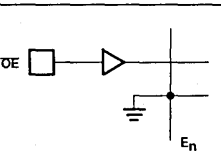
"$\overline{OE}$" ARRAY - (E)



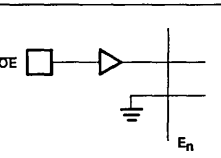
ACTION	CODE
IDLE[16, 19]	O



ACTION	CODE
CONTROL	A



ACTION	CODE
ENABLE[19]	•



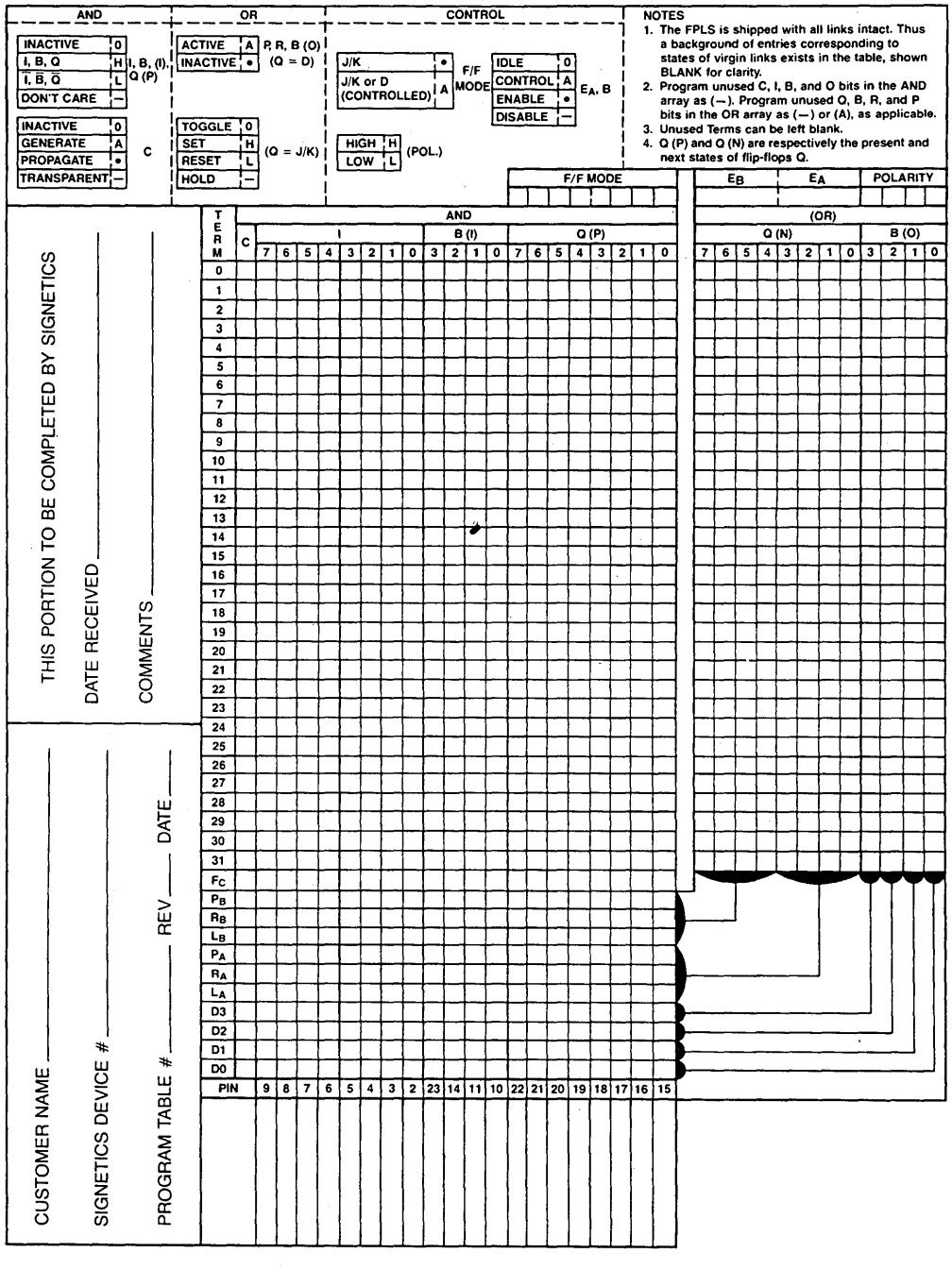
ACTION	CODE
DISABLE	–

NOTES:

16. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates.
17. Any gate $(T, F_C, L, P, R, D)_n$ will be unconditionally inhibited if any one of the I, B, or Q link pairs are left intact.
18. To prevent oscillations, this state is not allowed for C link, pairs coupled to active gates T_n, F_c.
19. E_n = O and E_n = • are logically equivalent states, since both cause F_n outputs to be unconditionally enabled.
20. These states are not allowed for control gates $(L, P, R, D)_n$ due to their lack of "OR" array links.

Field Programmable Logic Sequencer (20 × 45 × 12) — PLS179

FPLS PROGRAM TABLE



TB01712S

Signetics

PLUS405
Field-Programmable Logic Sequencer (16 × 64 × 8)

Signetics Programmable Logic
Product Specification

Military
Application Specific Products

- **Series 28**

DESCRIPTION

The PLUS405 device is a bipolar programmable state machine of the Mealy type. Both the AND and the OR arrays are user-programmable. All 64 AND gates are connected to the 16 external dedicated inputs (I_0 - I_{15}) and to the feedback paths of the 8 on-chip State Registers (Q_{P0} - Q_{P7}). Two complement arrays support complex IF-THEN-ELSE state transitions with a single product term (input variables C_0, C_1).

All state transition terms can include True, False, or Don't Care states of the controlling state variables. All AND gates are merged into the programmable OR array to issue the next-state and next-output commands to their respective register. Because the OR array is programmable, any one or all of the 64 transition terms can be connected to any or all of the State and Output Registers.

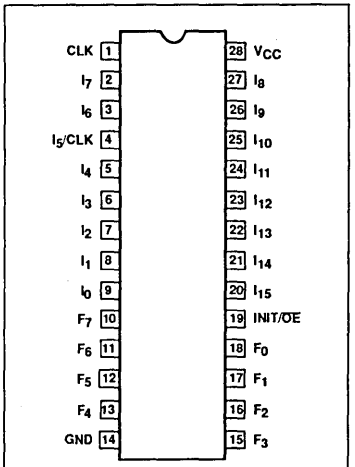
All state (Q_{P0} - Q_{P7}) and output (Q_{F0} - Q_{F7}) registers are edge-triggered, clocked J-K flip-flops, with Asynchronous Preset and Reset options. The PLUS405 architecture provides the added flexibility of the J-K toggle function which is indeterminate on S-R flip-flops. Each register may be individually programmed such that a specific Preset-Reset pattern is initialized when the initialization pin is raised to a logic level "1". This feature allows the state machine to be asynchronously initialized to known internal state and output conditions prior to proceeding through a sequence of state transitions. Upon power-up, all registers are unconditionally preset to "1". If desired, the initialization input pin (INIT) can be converted to an $\overline{\text{Output Enable}}$ ($\overline{\text{OE}}$) function as an additional user-programmable feature.

Availability of two user-programmable clocks allows the user to design two independently clocked state machine functions consisting of four state and four output bits each.

FEATURES

- **50 and 58.8MHz clock rates T_{CKM}**
- **f_{MAX} = 30MHz ($1/(t_{IS1} + t_{CKO1})$)**
- **Functional superset of PLS105/105A**
- **Field-programmable (Ti-W fusible link) See note below**
- **16 input variables**
- **8 output functions**
- **64 transition terms**
- **8-bit State Register**
- **8-bit Output Register**
- **2 transition Complement Array terms**
- **Multiple clocks***
- **Programmable Asynchronous Initialization or $\overline{\text{Output Enable}}$**
- **Power-on preset of all registers to "1"**
- **"On-chip" diagnostic test mode features for access to state and output registers**
- **950mW power dissipation (typical)**
- **TTL compatible**
- **J-K or S-R flip-flop functions**
- **Automatic "Hold" states**
- **3-State outputs**
- **Factory programmed option available**

PIN CONFIGURATION



For LLCC pin assignments see JEDEC Standard 21

APPLICATIONS

- **Interface protocols**
- **Sequence detectors**
- **Peripheral controllers**
- **Timing generators**
- **Sequential circuits**
- **Elevator controllers**
- **Security locking systems**
- **Counters**
- **Shift registers**

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-Pin Ceramic DIP 600mil-wide	PLUS405/BXA
28-Pin Ceramic Leadless Chip Carrier	PLUS405/B3A
28-Pin Ceramic Flat Pack	PLUS405/BYA

* Refer to AC Specifications for clock and operating frequencies when using multiple clocks.

NOTE: The standard to use verify function circuitry is not available for Military product. To use pattern verification must be accomplished by functional testing only.

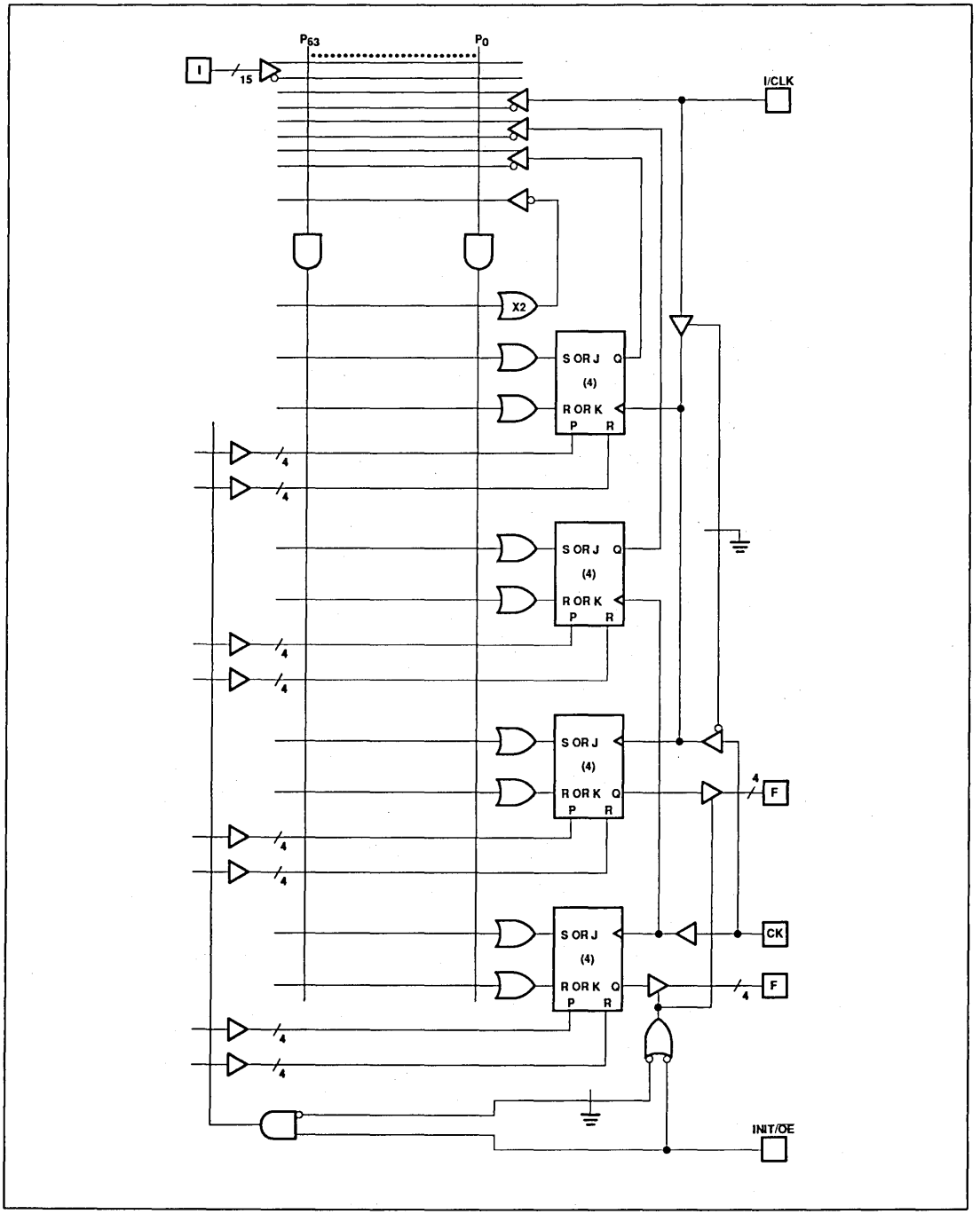
Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CLK1	**Clock:** The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers. Pin 1 only clocks P_{0-3} and F_{0-3} if Pin 4 is also being used as a clock.	Active-High (H)
2, 3, 5 - 9, 26 - 27 20 - 22	I_0 - I_4, I_7, I_6, I_8 - I_9 I_{13} - I_{15}	**Logic Inputs:** The 12 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence. True and complement signals are generated via use of "H" and "L".	Active-High/Low (H/L)
4	I_5/CLK2	**Logic Input/Clock:** A user programmable function:	
		• **Logic Input**: A 13th external logic input to the AND array, as above.	Active-High/Low (H/L)
		• **Clock**: A 2nd clock for the State Registers P_{4-7} and Output Registers F_{4-7}, as above. Note that input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using Pin 4 as a Clock.	Active-High (H)
23	I_{12}	**Logic/Diagnostic Input:** A 14th external logic input to the AND array, as above, when exercising standard TTL levels. When I_{12} is held at +10V, device outputs F_0 - F_7 reflect the contents of State Register bits P_0 - P_7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
24	I_{11}	**Logic/Diagnostic Input:** A 15th external logic input to the AND array, as above, when exercising standard TTL levels. When I_{11} is held at +10V, device outputs F_0 - F_7 become direct inputs for State Register bits P_0 - P_7; a Low-to-High transition on the appropriate clock line loads the values on pins F_0 - F_7 into the State Register bits P_0 - P_7. The contents of each Output Register remains unaltered.	Active-High/Low (H/L)
25	I_{10}	**Logic/Diagnostic Input:** A 16th external logic input to the AND array, as above, when exercising standard TTL levels. When I_{10} is held at +10V, device outputs F_0 - F_7 become direct inputs for Output Register bits Q_0 - Q_7; a Low-to-High transition on the appropriate clock line loads the values on pins F_0 - F_7 into the Output Register bits Q_0 - Q_7. The contents of each State Register remains unaltered.	Active-High/Low (H/L)
10 - 13 15 - 18	F_0 - F_7	**Logic Outputs/Diagnostic Outputs/Diagnostic Inputs**: Eight device outputs which normally reflect the contents of Output Register Bits Q_0 - Q_7, when enabled. When I_{12} is held at +10V, F_0 - F_7 = (P_0 - P_7). When I_{11} is held at +10V, F_0 - F_7 become inputs to State Register bits P_0 - P_7. When I_{10} is held at +10V, F_0 - F_7 become inputs to Output Register bits Q_0 - Q_7.	Active-High (H)
19	INIT/$\overline{OE}$	**Initialization or $\overline{\text{Output Enable}}$ Input:** **A user-programmable function:**	
		• **Initialization**: Provides an asynchronous preset to logic "1" or reset to logic "0" of all State and Output Register bits, determined individually for each register bit through user programming. INIT overrides Clock, and when held High, clocking is inhibited and F_0 - F_7 are in their initialization state. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after INIT goes Low. See timing definition for t_{VCK} and t_{NVCK}.	Active-High (H)
		• **$\overline{\text{Output Enable}}$**: Provides an output enable function to buffers F_0 - F_7 from the Output Registers.	Active-Low (L)

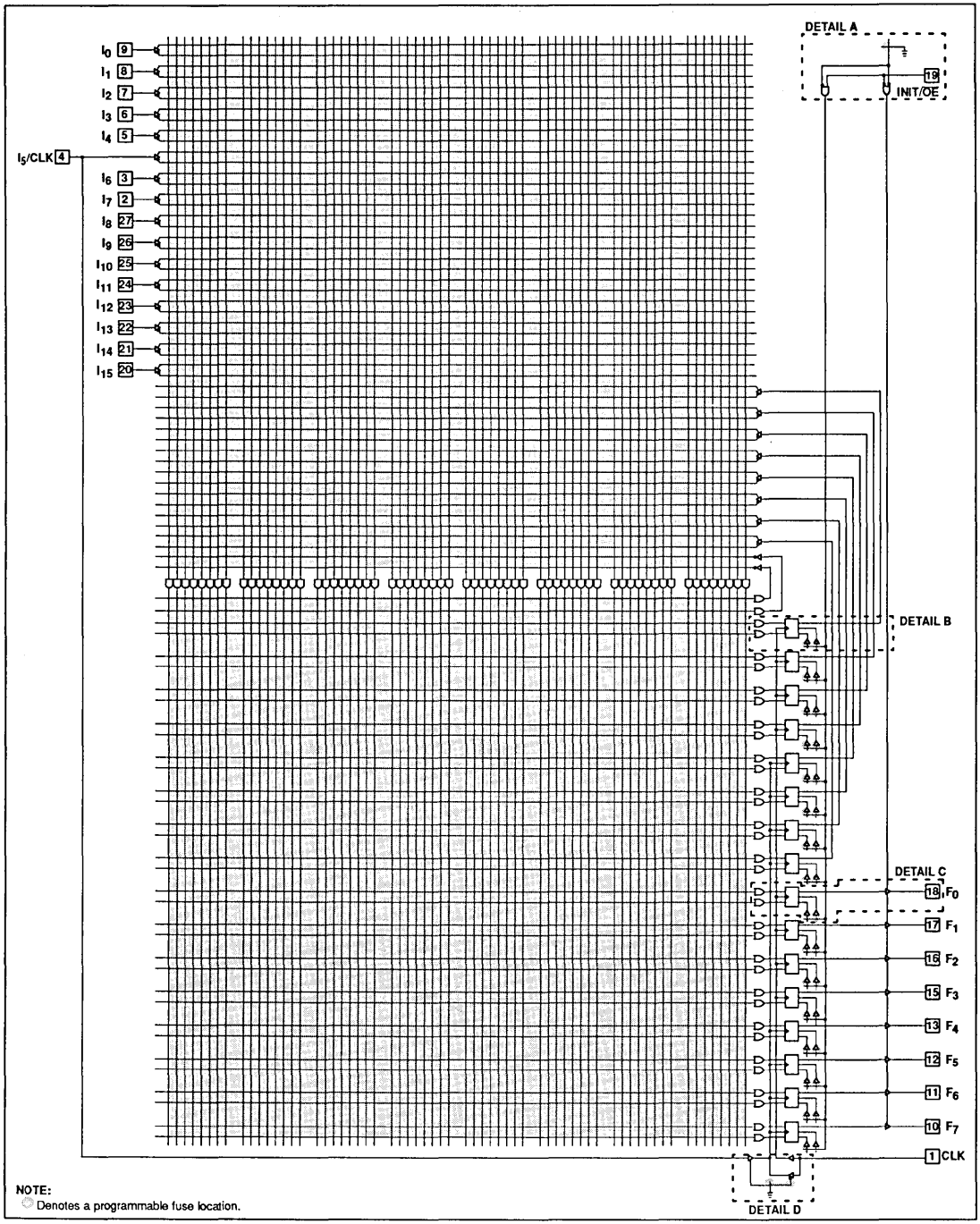
Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

FUNCTIONAL DIAGRAM



Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

FPLS LOGIC DIAGRAM



NOTE:
Denotes a programmable fuse location.

Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{STG}	Storage temperature range	-65	+150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}[9]	High level Input voltage	2.0			V
V_{IL}[9]	Low level Input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High level Output current			-2	mA
I_{OL}	Low level Output current			9.6	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

SYMBOL	PARAMETER[3]	TEST CONDITIONS[3]	LIMITS[3]			UNIT
			Min	Typ[2]	Max	
V_{IC}	Input Clamp voltage[4]	V_{CC} = Min, I_{IN} = Max		-0.8	-1.2	V
V_{OH}	High Level Output voltage	V_{CC} = Min, I_{OH} = Max	2.4			V
V_{OL}	Low Level Output voltage	V_{CC} = Min, I_{OL} = Max		0.35	0.5	V
I_{IH}	High Level Input current	V_{IN} = V_{CC} = Max		<1	25	µA
I_{IH1}	High Level Input current (Pin 1 only)	V_{IN} = V_{CC} = Max			50	µA
I_{IL}	Low Level Input current	V_{IN} = 0.45V, V_{CC} = Max		-10	-100	µA
I_{IL}	Low (CK input) Level Input current	V_{IN} = 0.45V, V_{CC} = Max		-50	-150	µA
I_{OHZ}	Off-State Output current High level	V_{CC} = Max, V_{OUT} 5.5V		1	40	µA
I_{OLZ}	Off-State Output current Low level	V_{CC} = Max, V_{OUT} 0.45V		-1	-40	µA
I_{OS}	Short circuit[4,5]	V_{CC} = Max, V_{OUT} = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current[6]	V_{CC} = Max		190	225	mA
C_{IN}	Input Capacitance[7]	V_{CC} = Nom, V_{IN} = 2.0V		8	13	pF
C_{OUT}	Output Capacitance[7]	V_{CC} = Nom, V_{OUT} = 2.0V		10	15	pF

Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[2]	Max	
Pulse Width							
t_{CKH1}	Clock High; CLK1 (Pin 1)	CK-	CK+	10	8		ns
t_{CKL1}	Clock Low; CLK1 (Pin 1)	CK+	CK-	10	8		ns
t_{CKP1}	CLK1 Period (without Complement Array)	Output±	Input±	33	24		ns
t_{CKH2}	Clock High: CLK2 (Pin 4)	CK-	CK+	10	8		ns
t_{CKL2}	Clock Low; CLK2 (Pin 4)	CK+	CK-	10	8		ns
t_{CKP2}	CLK2 Period (without Complement Array)	Output+	Input±	30	25		ns
t_{CKP3}	CLK1 Period (with Complement Array)	CK+	CK+	40	32		ns
t_{CKP4}	CLK2 Period (with Complement Array)[11]	Output±	Input±	40	35		ns
t_{INITH}	Initialization pulse	INIT+	INIT-	15	10		ns
Setup Time[8]							
t_{IS1}	Input	CK+	Input±	18	12		ns
t_{IS2}	Input (through Complement Array)	CK+	Input±	25	20		ns
t_{VS}	Power-on preset[10]	CK-	V_{CC}+	0	-10		ns
t_{VCK}	Clock resume (after initialization)	CK-	INIT-	0	-5		ns
t_{NVCK}	Clock lockout (before initialization)	INIT-	CK-	15	5		ns
Hold Time							
t_{IH}	Input	Input±	CK+	0	-5		ns
Propagation Delay							
t_{CKO1}	Clock1 (Pin 1)	Output±	CK1+		10	15	ns
t_{CKO2}	Clock2 (Pin 4)	Output±	CK2+		12	15	ns
t_{OE}	Output Enable	Output-	OE-		12	15	ns
t_{OD}	Output Disable[8]	Output+	OE+		12	15	ns
t_{INIT}	Initialization	Output+	INIT+		15	20	ns
t_{PPR}	Power-on preset[10]	Output+	V_{CC}+		0	10	ns
Max. Frequency of Operation							
f_{MAX1}	CLK1; (without Complement Array)					30.0	MHz
f_{MAX3}	CLK1; (with Complement Array)					25.0	MHz

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Duration of short circuit should not exceed 1 second.
6. Measured with the INIT/$\overline{OE}$ input grounded, all other inputs ≥ 4.5V and the outputs open.
7. C_{IN} and C_{OUT} is guaranteed but not measured.
8. $C_L = 5pF$; $V_T = V_{OL} + 0.5V$.
9. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Testing of these values requires special equipment.
10. These parameters are guaranteed, but not tested.
11. Not tested, but guaranteed through the testing of t_{IS2} and t_{CKO2}.

Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

TRUTH TABLE

V_{CC}	OPTION INIT	OPTION $\overline{OE}$	I_{10}	I_{11}	I_{12}	CK	J	K	Q_P	Q_F	F
	H		*	*	*	X	X	X	H/L	H/L	Q_F
	L		+10V	X	X	↑	X	X	Q_P	L	L^9
	L		+10V	X	X	↑	X	X	Q_P	H	H^9
	L		X	+10V	X	↑	X	X	L	Q_F	L^9
	L		X	+10V	X	↑	X	X	H	Q_F	H^9
	L		X	X	+10V	X	X	X	Q_P	Q_F	Q_P
	L		X	X	X	X	X	X	Q_P	Q_F	Q_F
		H	X	X	*	X	X	X	Q_P	Q_F	Hi-Z
		X	+10V	X	X	↑	X	X	Q_P	L	L^9
+5V		X	+10V	X	X	↑	X	X	Q_P	H	H^9
		X	X	+10V	X	↑	X	X	L	Q_F	L^9
		X	X	+10V	X	↑	X	X	H	Q_F	H^9
		L	X	X	+10V	X	X	X	Q_P	Q_F	Q_P
		L	X	X	X	X	X	X	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	L	Q_P	Q_F	Q_F
		L	X	X	X	↑	L	H	L	L	L
		L	X	X	X	↑	H	L	H	H	H
		L	X	X	X	↑	H	H	$\overline{Q_P}$	$\overline{Q_F}$	$\overline{Q_F}$
↑	X	X	X	X	X	X	X	X	X	X	H

NOTES:
1. Positive Logic:
   S/R (or J/K) = $T_0 + T_1 + T_2 + \ldots T_{63}$
   $T_n = (C_0, C_1)\ (I_0, I_1, I_2, \ldots)\ (P_0, P_1, \ldots P_7)$
2. Either Initialization (Active-High) or $\overline{\text{Output Enable}}$ (Active-Low) are available, but not both. The desired function is a user-programmable option.
3. ↑ denotes transition from Low-to-High level.
4. * = H/L/+10V.
5. X = Don't Care (≤ 5.5V)
6. H/L implies that either a High or a Low can occur, depending upon user-programmed selection (each State and Output Register individually programmable).
7. When using the F_n pins as inputs to the State and Output Registers in diagnostic mode, the F buffers are 3-Stated and the indicated levels on the output pins are forced by the user.

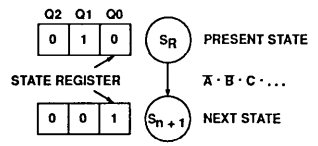
VIRGIN STATE

A factory-shipped virgin device contains all fusible links intact, such that:

1. INIT/$\overline{OE}$ option is set to INIT. In order to use the INIT function, the user must select either the PRESET or the RESET option for each flip-flop. Note that regardless of the user-programmed initialization, or even if the INIT function is not used, all registers are preset to "1" by the power-up procedure.
2. All transition terms are inactive (0).
3. All S/R (or J/K) flip-flop inputs are disabled (0).
4. The device can be clocked via a Test Array pre-programmed with a standard test pattern.

LOGIC FUNCTION

Typical State Transition:



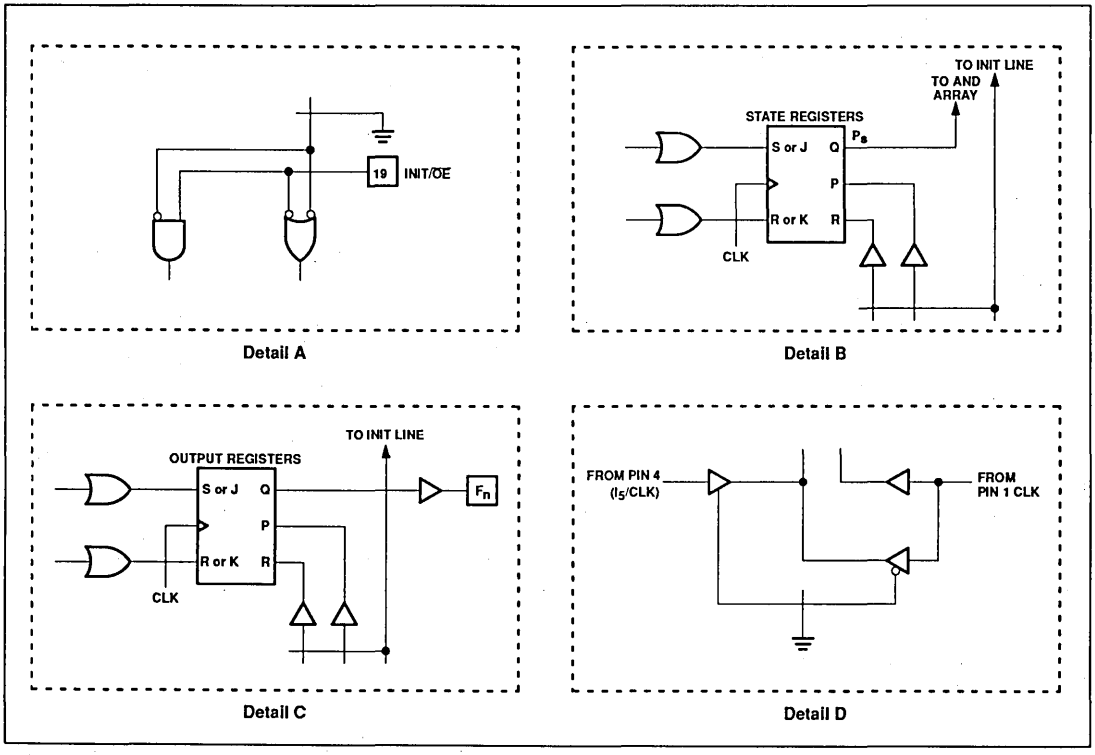
SET Q_0: $S_0 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$
$R_0 = 0$

RESET Q_1: $S_1 = 0$
$R_1 = (\overline{Q}_2 \cdot Q_1 \cdot \overline{Q}_0) \cdot \overline{A} \cdot \overline{B} \cdot C \ldots$

HOLD Q_2: $S_2 = 0$
$R_2 = 0$

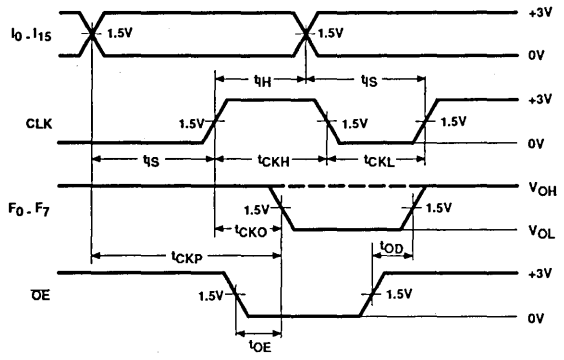
Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

DETAILS FOR REGISTERS FOR PLUS405

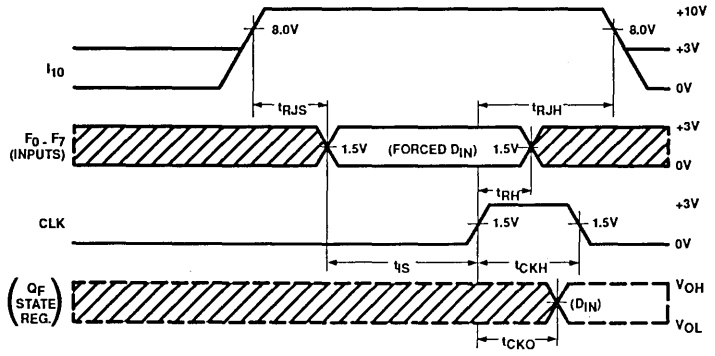


Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

TIMING DIAGRAMS



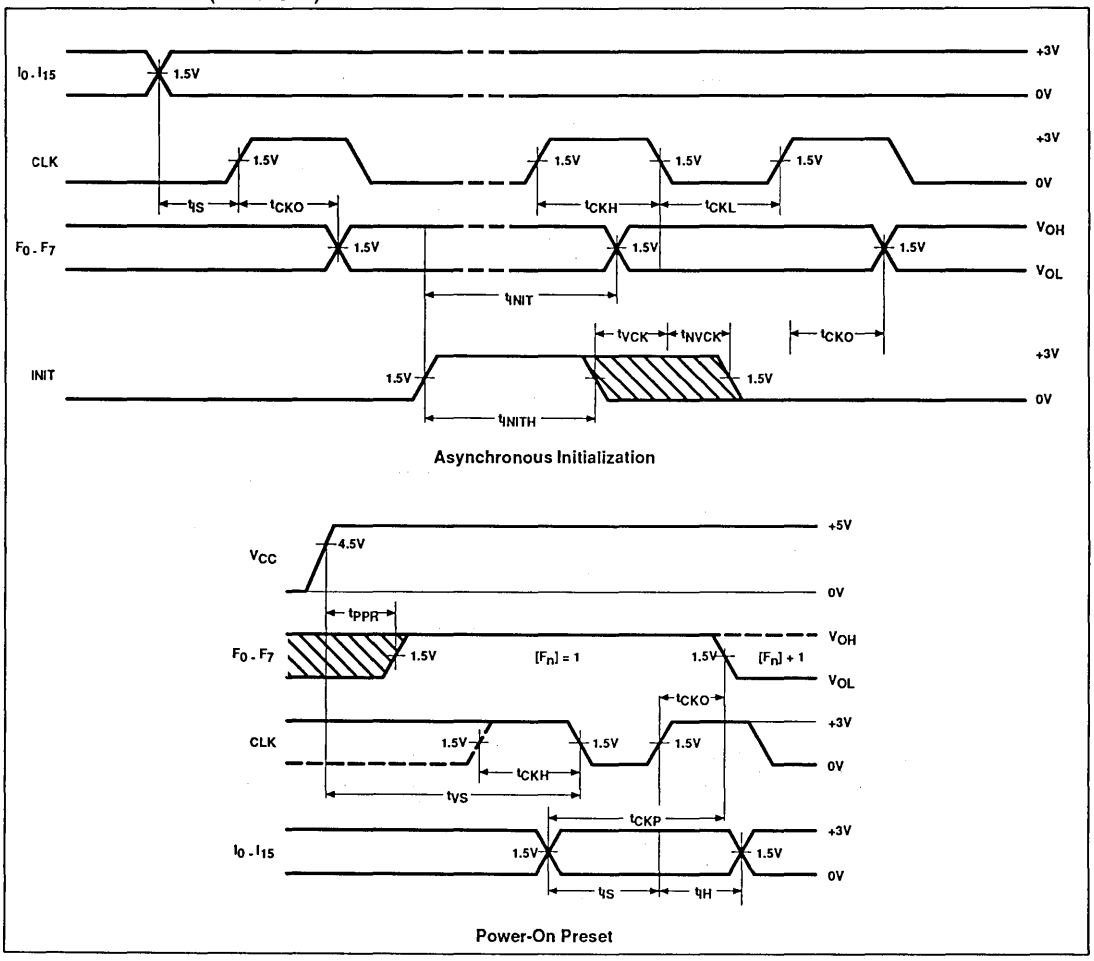
Sequential Mode



Diagnostic Mode - Output Register Input Jam

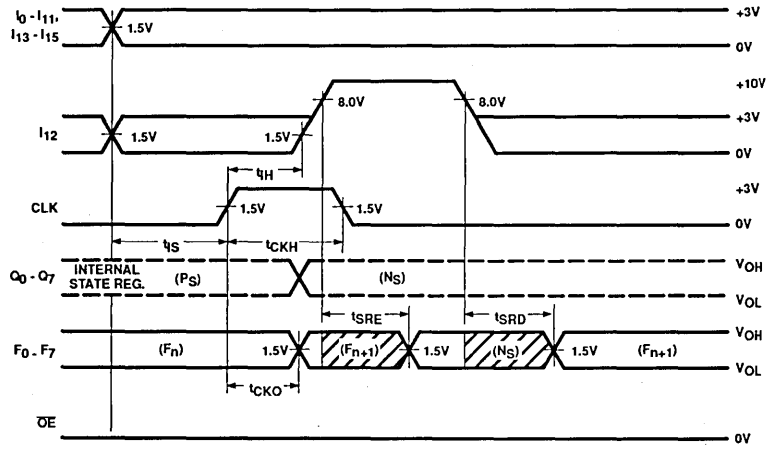
Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

TIMING DIAGRAMS (Continued)

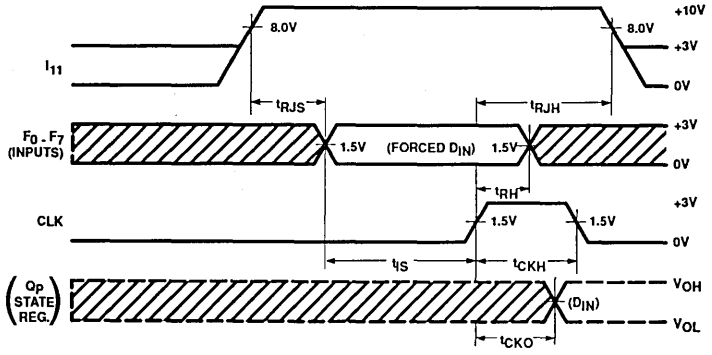


Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

TIMING DIAGRAMS (Continued)



Diagnostic Mode - State Register Outputs



Diagnostic Mode - State Register Input Jam

TIMING DEFINITIONS

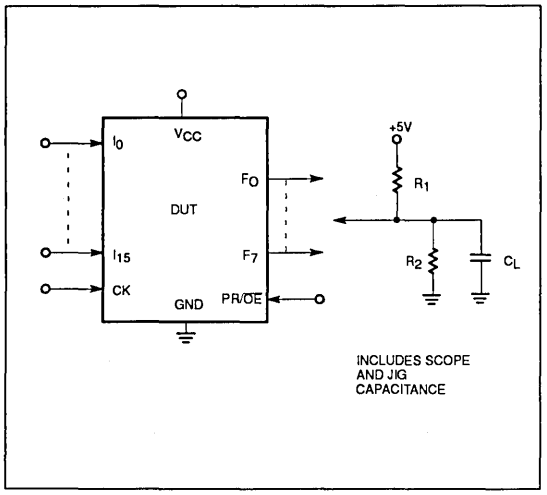
SYMBOL	PARAMETER
$t_{CKH12,13}$	Width of input clock pulse.
$t_{CKP12,13}$	Clock period - when not using Complement Array.
t_{IS1}	Required delay between beginning of valid input and positive transition of Clock.
$t_{CKO12,13}$	Delay between positive transition of Clock and when Outputs become valid (with INIT/$\overline{OE}$ Low).
t_{PPR}	Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
t_{IS2}	Required delay between beginning of valid Input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
t_{RJH}	Required delay between positive transition of Clock and end of inputs I_{11} or I_{10} transition to State and Output Register Input Jam Diagnostic Modes, respectively.
$f_{MAX12,13,14,15}$	Maximum operating frequency.

SYMBOL	PARAMETER
$t_{CKL12,13}$	Interval between clock pulses.
$t_{CKP14,15}$	Clock period - when using Complement Array.
t_{IH}	Required delay between positive transition of Clock and end of valid Input data.
t_{OE}	Delay between beginning of Output Enable Low and when Outputs become valid.
t_{SRE}	Delay between input I_{12} transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
t_{RJS}	Required delay between inputs I_{11} or I_{10} transition to State and Output Register Input Jam Diagnostic Modes, respectively, and when the output pins become available as inputs.
t_{NVCK}	Required delay between the negative transition of the clock and the negative transition of the Asynchronous Initialization to guarantee that the clock edge is not detected as a valid negative transition.

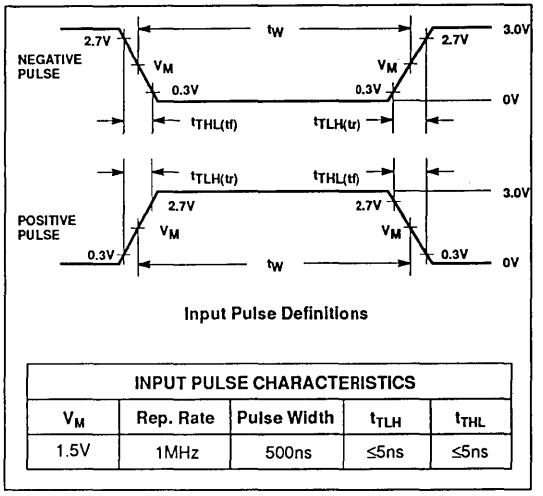
SYMBOL	PARAMETER
t_{INITH}	Width of initialization input pulse.
t_{VS}	Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
t_{OD}	Delay between beginning of Output Enable High and when Outputs are in the OFF-state.
t_{INIT}	Delay between positive transition of Initialization and when Outputs become valid.
t_{SRD}	Delay between input I_{12} transition to Logic mode and when the Outputs reflect the contents of the Output Register.
t_{RH}	Required delay between positive transition of Clock and end of valid Input data when jamming data into State or Output Registers in diagnostic mode.
t_{VCK}	Required delay between negative transition of Asynchronous Initialization and negative transition of Clock preceding first reliable clock pulse.

Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

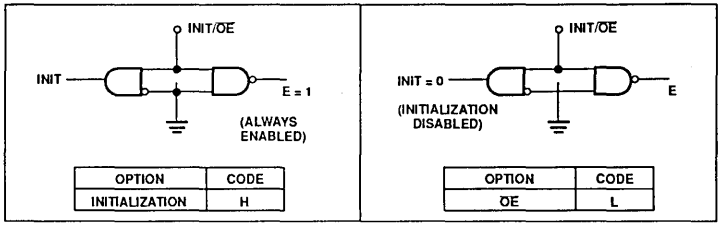
LOGIC PROGRAMMING

PLUS405 Logic designs can be generated using Signetics AMAZE design software or several other commercially available, JEDEC standard PLD design software packages. Boolean and/or state equation entry format is accepted.

PLUS405 logic designs can also be generated using the program table format detailed on the following page(s). This Program Table Entry format (PTE) is supported by the Signetics AMAZE PLD design software. AMAZE is available free of charge to qualified users.

To implement the desired logic functions, each logic variable (I, B, P, S, T, etc.) from the logic equations is assigned a symbol. TRUE, COMPLEMENT, PRESET, RESET, OUTPUT ENABLE, INACTIVE, etc., symbols are defined below.

INITIALIZATION/$\overline{OE}$ OPTION - (INIT/$\overline{OE}$)



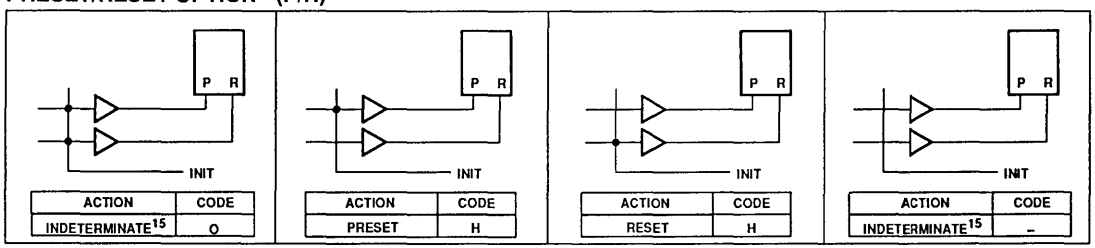
OPTION	CODE
INITIALIZATION	H

OPTION	CODE
OE	L

PROGRAMMING THE PLUS405:
The PLUS405 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (State and Output Register) at logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

PROGRAMMING VERIFICATION;
The fuse verify circuitry is not available for Military grade product. Fuse pattern verification must be accomplished by functional teting. Signetics can provide product programmed and functionally tested directly from the factory as an option. Contact your local Signetics sales representative or the Military Marketing Group for details.

PRESET/RESET OPTION - (P/R)



ACTION	CODE
INDETERMINATE[15]	0

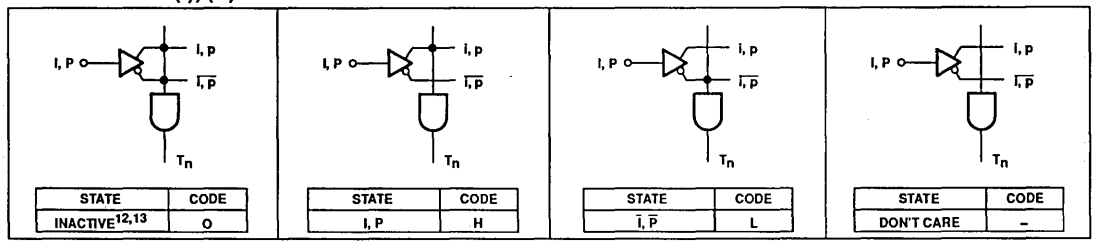
ACTION	CODE
PRESET	H

ACTION	CODE
RESET	H

ACTION	CODE
INDETERMINATE[15]	–

Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

"AND" ARRAY - (I), (P)



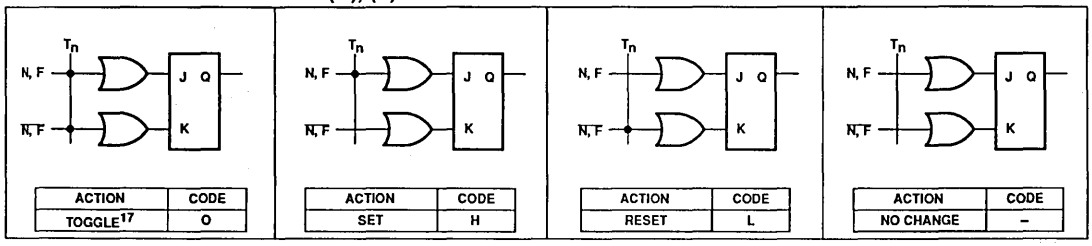
STATE	CODE
INACTIVE[12,13]	O

STATE	CODE
I, P	H

STATE	CODE
$\overline{I}$, $\overline{P}$	L

STATE	CODE
DON'T CARE	–

"OR" ARRAY - J-K FUNCTION - (N), (F)



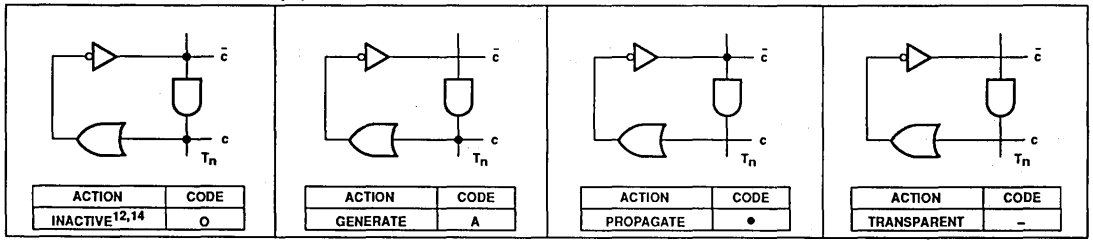
ACTION	CODE
TOGGLE[17]	O

ACTION	CODE
SET	H

ACTION	CODE
RESET	L

ACTION	CODE
NO CHANGE	–

"COMPLEMENT" ARRAY - (C)



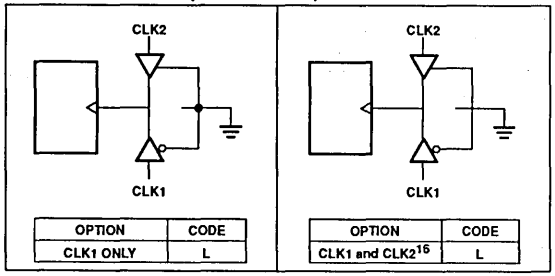
ACTION	CODE
INACTIVE[12,14]	O

ACTION	CODE
GENERATE	A

ACTION	CODE
PROPAGATE	•

ACTION	CODE
TRANSPARENT	–

CLOCK OPTION - (CLK1/CLK2)



OPTION	CODE
CLK1 ONLY	L

OPTION	CODE
CLK1 and CLK2[15]	L

NOTES:

12. This is the initial unprogrammed state of all links.
13. Any gate T_n will be unconditionally inhibited if any one of its I or P link pairs are left intact.
14. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n.
15. These states are not allowed when using PRESET/RESET option.
16. Input buffer I_5 must be deleted from the AND array (i.e., all fuse locations "Don't Care") when using second clock option.
17. A single product term cannot drive more than 8 registers by itself when used in TOGGLE mode.

Field-Programmable Logic Sequencer (16 × 64 × 8) PLUS405

PLUS405 PROGRAM TABLE

AND

INACTIVE	0	Im, Ps
I, P	H	
$\overline{I}$, $\overline{P}$	L	
DON'T CARE	-	

INACTIVE	0	Cn
GENERATE	A	
PROPAGATE	•	
TRANSPARENT	-	

OR

INACTIVE OR TOGGLE	0	Ns, Fr
SET	H	
RESET	L	
NO CHANGE	-	

OPTIONS

INIT	H	INIT/$\overline{OE}$
$\overline{OE}$	L	
CLK1 ONLY	L	CLK1/CLK2
CLK1 AND 2	H	

CUSTOMER NAME _____ SIGNETICS DEVICE # _____ CF (XXXX) _____ CUSTOMER SYMBOLIZED PART # _____

REV _____ DATE _____ PROGRAM TABLE _____

	AND																				OR												OPTIONS							
	CLOCK 1/2																				INITIALIZATION/OUTPUT ENABLE																		
	COMP. ARRAY		INPUT (Im)														PRESENT STATE (Ps)								NEXT STATE (Ns)								OUTPUT (Fr)							
	C1	C0	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	P7	P6	P5	P4	P3	P2	P1	P0	N7	N6	N5	N4	N3	N2	N1	N0	F7	F6	F5	F4	F3	F2	F1	F0
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PIN NO.			20	21	22	23	24	25	26	27	2	3	4	5	6	7	8	9																	10	11	12	13	15	16	17	18
PIN LABELS																																									

NOTES:
1. The FPLS is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the IN/E and H for the clock option, exists in the table, shown BLANK instead for clarity.
2. Unused Cn Im, and Ps bits are normally programmed Don't Care (—).
3. Unused Transition Terms can be left blank for future code modification, or programmed as (—) for maximum speed.

Signetics

Military Products

Section 8
Package Outlines

Please refer to the Packaging Information of the Introduction on page 15.

Signetics

Military Products

Section 9
Sales Offices, Representatives & Distributors

Sales Offices, Representatives & Distributors

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