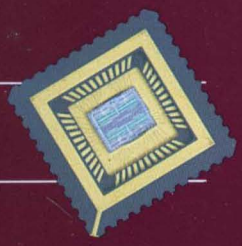

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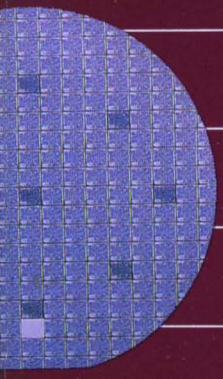

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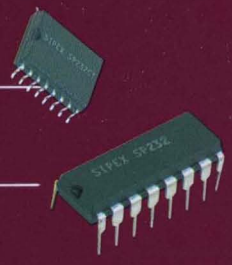

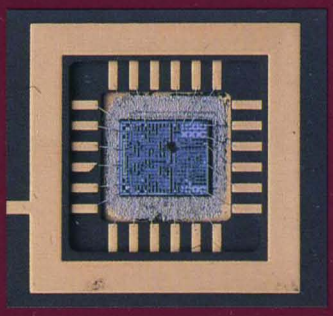

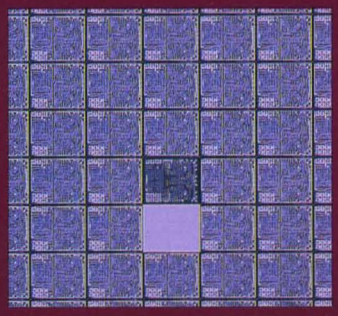

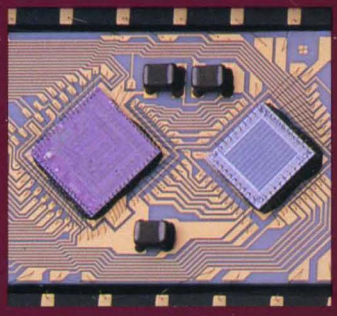

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Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SIPEX . . . EXCELLENCE IN SIGNAL PROCESSING

SIPEX is a manufacturing company that serves the analog signal processing market. The company produces signal conditioning, signal conversion and data acquisition system products utilizing both hybrid and monolithic technologies.

Excelling in the fields of high speed and high precision, SIPEX offers products of standard, semi-custom and full-custom design. SIPEX also produces and sells dielectrically isolated wafers produced to customer specifications.

SIPEX's broad product offerings and capabilities are the result of recent mergers between Hybrid Systems Corporation, Datalinear Corporation Barvon and Dielectric Semiconductor Inc. As a result of the mergers, SIPEX provides its customers with multiple solutions to its signal processing needs.

While the name SIPEX is new, the foundations of the company represent years of solid technological achievements. SIPEX, which stands for Signal Processing Excellence, is the summation of the strengths of our two operations.

- **East Coast,** in operation for over twenty years, a leader in technological advances and certified to MIL-STD-1772, produces standard and custom hybrid circuits and thin film substrates.
- **West Coast,** designs and manufactures linear IC's and dielectric isolation base wafers, supplying military and commercial markets with full custom, standard, and ASIC products.

Quality and reliability have long been inherent to our company, consequently the wafers, IC's and hybrids manufactured by SIPEX are used in many major military and space programs including AMRAAM, Sparrow Missile, MILSTAR, Trident and SICBM. Industrially, SIPEX serves the ATE, process control, medical, seismics, telecommunications and other related market areas.

A unified worldwide sales network provides easy access to our capabilities and applications engineers. We are committed not only to the most advanced signal processing products, but also to the highest level of customer service.

CERTIFIED TO MIL-STD-1772

In addition to the standard hybrid and monolithic products shown in this catalog, Sipex offers the following additional capabilities:

CUSTOM HYBRID CIRCUITS

In addition to having a complete line of standard products, Sipex Corporation also provides many complex application specific products to its customers.

Custom products include A/D converters, D/A converters, voltage to frequency converters, sample and holds, instrumentation amplifiers, OP amps, voltage references, multiplexers, modulators, filters, analog switches, bus interface, analog and digital interface, thin-film resistor networks, and thin-film substrates.

With state-of-the-art design and manufacturing equipment, Sipex Corporation is an industry leader in the manufacturing of custom hybrid components. Send your custom requirements to your Sipex representative or directly to the factory.

CLASS "S" PRODUCTION

Sipex's commitment to the highest achievable quality control and reliability is exemplified through Military/NASA standard Class "S" hybrids used in aerospace satellite and manned space flight applications. Sipex has dedicated a special program management office to control all Class "S" production. Our hybrids are being used in the space shuttle program, MILSTAR defense satellite, shuttle/centaur booster rocket, and various military classified defense satellites.

MIL-STD-1772

Sipex Corporation has been certified to produce Sipex Circuits which meet the requirements of MIL-STD-1772.

MIL-STD-1772 was established by the Defense Electronics Supply Center (DESC) to provide a standardized flow of fabrication processes and lines. It also provides for a standardization of Documentation and Testing.

Military Sipex Components purchased to MIL-STD-883 are now required to be manufactured and tested in a facility which is certified to MIL-STD-1772.

RADIATION TESTING

For the past several years, Sipex has been conducting in-house programs to study the effects of radiation on our converter products. Converter circuits have become an integral part of military and space programs and for these programs, radiation survivability is an essential factor. We have completed studies on precision reference sources, analog-to-digital and digital-to-analog converters using the facilities at the University of Lowell radiation laboratory. We have performed total exposure using CO-60 and fast neutron exposure using both an accelerator and a research reactor.

Sipex is willing and able to test for qualification any component which we manufacture and in addition, will be happy to quote on testing products from other manufacturers. Our experience testing and characterizing converter products makes us an ideal source for radiation testing.

DIELECTRIC ISOLATION TECHNOLOGY

TECHNOLOGY/PRODUCTS

Sipex offers a broad range of high performance linear, monolithic IC's which either require or benefit from the use of Dielectric Isolation (DI) technology. This technology offers several significant user benefits:

- Higher bandwidths and slew rates than are achievable with conventional IC technology.
- High temperature operation (up to 200°C).
- Radiation hardened parts.

While DI has long been known for its radiation hardening benefits, its features extend beyond just radiation hardening. DI allows high f_T, vertical NPN and PNP bipolar transistors to be fabricated on the same chip. The presence of the high speed, vertical PNP transistor allows the high bandwidths, slew rates and settling times as well as the excellent DC characteristics that are uniquely associated with DI OP Amp type products.

Sipex's technology extends beyond just high speed, complementary transistors. In addition to these transistors and other devices, the IC processes employ p channel and n channel JFET's MOS capacitors, sub-surface zeners and thin film Nichrome (NiCr) resistors. The NiCr resistors offer extremely low temperature coefficients and can be laser trimmed to achieve the ultimate in matching and precision. This library of devices offers users the best combination of speed and precision available on one chip today.

This DI technology can be accessed at one of four levels:

- Standard products
- Full custom
- Cell custom
- Array custom

FACILITIES

Sipex has a 31,000 sq. ft. building located in Milpitas, CA which houses a wafer fab, assembly and test operations, a design engineering staff, a full array of CAD/CAE equipment and other supporting staff and equipment. The wafer fab is Class 100 in the photo area and all work stations. The assembly line is MIL certified. Off-shore assembly houses have been selected and audited for supplying parts to cost sensitive operations.

Sipex also provides high quality dielectrically isolated silicon substrates to a broad spectrum of semiconductor manufacturers. Sipex provides unique structures in silicon that serve as a foundation for:

- High speed linear circuits
- High voltage switching arrays
- Opto-coupled photovoltaic devices
- Radiation resistant integrated circuits

Dielectric Isolation technology allows the fabrication of these product families because each active device area may be isolated in an individual tub region, separated from the other devices in the circuit. This eliminates parasitics that degrade circuit performance and improves reliability under conditions of extreme levels of ionizing radiation.

Sipex is actively involved in advanced processing techniques related to cost reduction of the material and improved island thickness control. In addition, research is currently underway to provide material's processing that may be applied to very high speed CMOS and BIMOS technologies.

In addition, Sipex provides services related to the deposition of polycrystalline silicon, wafer thinning and chemical etching for transducer and solar cell applications.

MILITARY PROGRAM PARTICIPATION

Sipex Corporation plays a vital part and is an expert in many major military and space programs, both in the United States and Europe. Some of the programs Sipex Corporation participates in are:

- SPACE SHUTTLE
- F-15
- F-16
- F-18
- STD MISSILE
- F-111
- B-1
- SEA SPARROW
- TOW-2
- MAVERICK
- MILSTAR
- EA6B/B-1
- SPARROW MISSILE
- PIVADS
- MIRAGE F1
- AMRAAM
- SPACE LAB
- TORNADO
- STING RAY
- JAS 38
- ALRM
- SPEARFISH
- HOT
- DM2A3 TORPEDO
- ROLAND
- LEOPARD I & II
- AIRBUS 310
- MAGIC
- MIRAGE 2000
- HARM MISSILE
- LARZAC & CFM 56
- TRIDENT
- SICBM

SALES, SHIPPING & SERVICE INFORMATION

ORDERING INFORMATION

Orders may be placed with either our regional sales offices, sales representatives or directly with sales headquarters. Addresses and telephone/FAX numbers are listed in the sales office directory.

International: Customers outside the United States are served by Sipex's subsidiaries; Sipex Systems GmbH and Sipex Systems U.K. Ltd; Sipex Systems S.A.R.L.; or international sales representatives located throughout Europe, the Far East, and Canada. All international orders may be placed with either our international sales offices, sales representatives or directly with International Sales Department at sales headquarters. Addresses and telephone/FAX numbers are listed in the sales office directory.

TERMS AND CONDITIONS OF SALE

Price and delivery information of any item in this catalog is available from our sales representatives or direct from the Company. Quotations are F.O.B. factory of origin, and are subject to change without notice. On all orders, payment is net 30 days following date of shipment.

APPLICATIONS ENGINEERING

Sipex maintains a support staff of technical sales engineers, both domestically and internationally, who are expert in specific areas of analog, digital, and microelectronics technology. Staff engineers provide further technical support, as needed, on advanced circuit designs or application problems.

SHIPPING INSTRUMENTS

Shipping will be via United Parcel Service or Parcel Post unless other instructions are indicated. For rush service, we will ship by Air Freight, Air Express or Air Parcel Post on request.

WARRANTY

Sipex warrants its products to be free from defects in material and workmanship for a period of one year from the date of shipment. This warranty shall not apply to any product which has been abused or misused physically or electrically or whose leads have been clipped or soldered. Sipex's sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective components. Sipex shall not be liable for consequential damages under any circumstances.

RETURNS

When returning material for repair or replacement, it is necessary first to contact Customer Service. Upon acceptance of the request, a return material authorization will be issued. We require a detailed description of the reason for the return; the date and purchase order number on which it was obtained, and the date of receipt.

SPECIFICATIONS

Sipex reserves the right to discontinue items and change specifications without notice.

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SIGNAL PROCESSING EXCELLENCE

APPLICATION NOTES

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Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DIGITIZING DYNAMIC SIGNALS

When using Analog/Digital Converters based on the successive approximation technique, careful attention must be paid to the dynamic behavior of the circuit in order to achieve the desired accuracy. This article shows how the desired accuracy can be maintained with rapidly changing dynamic signals.

INTRODUCTION

The block diagram in Figure 1 shows the typical configuration of a data acquisition system used to convert an analog value into a corresponding binary form. The analog signal, which is often non-electrical in nature (like pressure, temperature, pH-value, distance) is converted to an electrical voltage by a sensor or transducer. In many cases, this voltage has an amplitude of just a few millivolts and is often superimposed on a common mode voltage. The instrumentation amplifier suppresses the common mode voltage and amplifies the analog signal to a level which is useful for subsequent processing (e.g., 0 to +10 volts). Additional function blocks like low pass- or anti-aliasing-filters (to suppress noise and unwanted frequency bands) can be inserted between the instrumentation amplifier and the A/D Converter. After the conversion has been completed, the ADC will output a digital word which corresponds to the value of the analog input signal. Depending on the desired function of the circuit, the digital word can be further processed by a computer or microprocessor.

To test the performance of such a circuit (as shown in Figure 1), usually a variable voltage source is used as the input instead of the sensor or transducer. Provided that the instrumentation amplifier has a linear transfer function and the ADC meets its specifications (especially differential linearity), all possible bit combinations (e.g., 4096 for 12-bit resolution) can be produced at the output of the ADC by varying the input voltage source. But once a dynamically changing voltage source, like a function generator, is connected to the analog input to simulate the response of the transducer, substantial linearity errors and so-called "missing codes" can be observed. This can easily degrade the accuracy of the data acquisition system from 12 to 10 or 8 bits or less. The reasons for this performance degradation and how these errors can be eliminated will be described below.

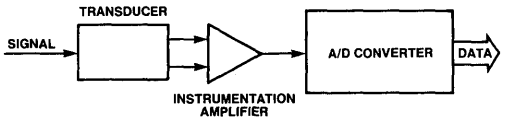


Figure 1. Block Diagram of a Data Acquisition System

CONVERSION PRINCIPLES

Several analog-to-digital conversion techniques have been developed which are tailored to the specific needs of different applications. Following is a short description of the three major techniques.

Integrating A/D Converters: Integrating or Dual-Slope ADCs were the first on the market. They consist of a charging capacitor, a current source, an analog comparator and a digital counter with clock. The conversion is done in two phases. During the first phase, the capacitor is charged with a current derived from the input voltage for a fixed amount of time. In the second phase, the counter is started and the capacitor is discharged with a constant current source. The comparator stops the counter as soon as the capacitor is completely discharged. The reading of the counter is directly proportional to the value of the input signal. The conversion of the input signal and the conversion time is directly dependent on the value of the input signal.

Integrating ADCs offer medium to high resolution at conversion speeds of 1 to 1000 samples per second. Their characteristics include high noise immunity, relatively simple design and low cost. Applications include digital voltmeters and acquisition of slow changing signals such as temperature. Special conversion techniques like Quad-Slope have been derived from the Dual-Slope principle for special applications such as very high precision voltmeters.

Flash A/D Converters: Offering the highest possible speed, Flash-converters are used in applications such as waveform recording and digitizing video signals. Sampling rates exceeding 100 MHz are no longer a talk of the future. This extremely high conversion speed is achieved with a single-step architecture. A reference voltage is applied to the top of a ladder of resistors with equal value. Each tab of the ladder is connected to one input of a voltage comparator, while the other input of each comparator is connected to the input voltage. For N bits of resolution, $2^N - 1$ resistors and comparators are required. This limits the resolution of currently available Flash-converters to 10 bits (requiring 1023 resistors and comparators). Each comparator compares the input voltage with the scaled reference voltage resulting in a "bar"-type output code. A digital encoder finally converts the linear "bar"-type code into a binary code.

Successive Approximation (SAR-type) A/D Converters: This type of ADC fills the gap between the high resolution/low speed integrating ADC and the extremely fast, low resolution Flash converter. SAR-type ADCs offer medium to high resolution with conversion speeds of 10,000 to 1,000,000 samples per second.

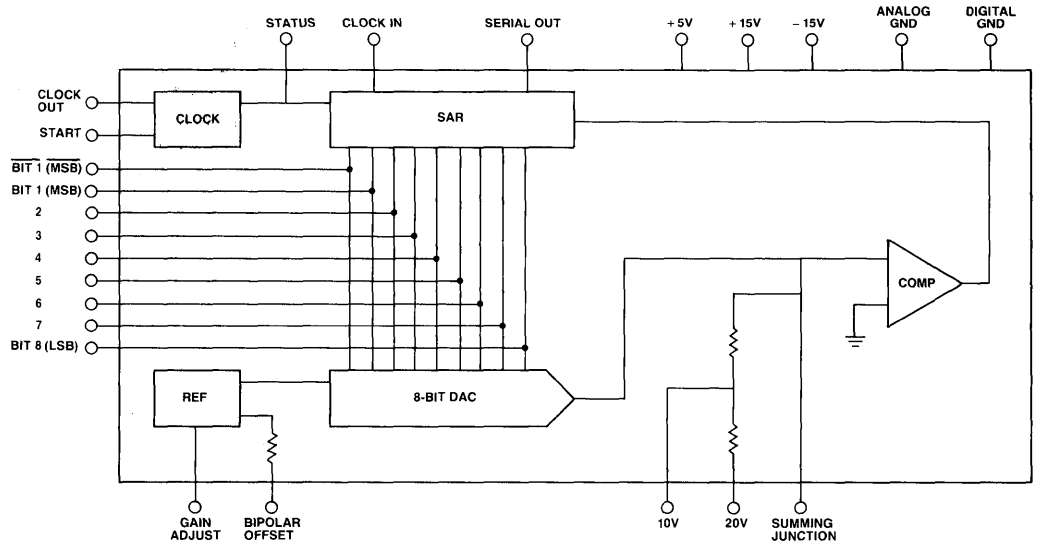


Figure 2. Functional Diagram of an A/D Converter with SAR

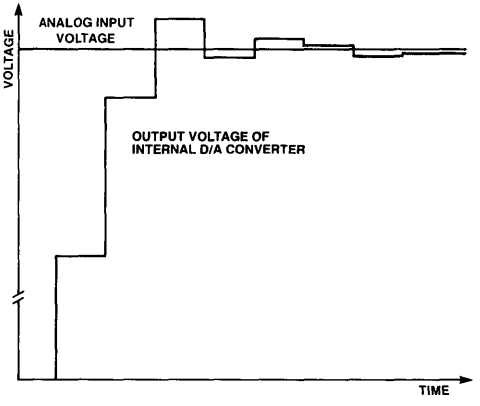


Figure 3. Internal Sequence of an A/D Conversion

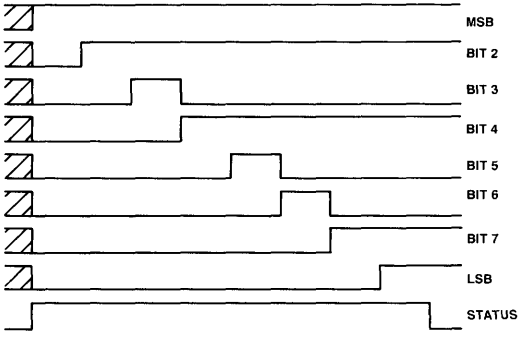


Figure 4. Timing Diagram

Figure 2 shows a block diagram of an 8-bit SAR-type ADC. The main building block is a Digital/Analog-Converter which determines the accuracy of the ADC. A comparator compares the output of the DAC with the analog input and provides a digital signal to the "Successive Approximation Register" (SAR). During the conversion time the SAR generates a digital code in such a manner that the output of the DAC equals the analog input signal. For N bits of resolution only N clock cycles are required, far less than that for the integrating converter. Some converters require one additional clock pulse at the beginning of the conversion cycle to reset the SAR. The SAR determines the digital code in the same way as an unknown weight is determined with a beam balance with the least number of decisions.

At the beginning of a conversion cycle, the MSB (Most Significant Bit) is switched on with all other bits switched off. After the output of the DAC has settled, the comparator decides whether the output voltage is greater or smaller than the input voltage and provides this information to the SAR. If the DAC output is smaller than the input voltage, the MSB remains switched on; otherwise it is reset to zero. The MSB of the final digital output is valid after the first clock cycle and may be read out (this is normally done for serial output). With the next clock pulse the second bit is switched on and based on the comparator's decision, is reset to zero or remains set. This process is repeated until the SAR has switched on all the remaining bits and latched the comparator's decisions. The sequence over time of the A/D conversion is shown in Figure 3. It can be clearly seen how the DAC's output voltage approaches the input signal during the conversion cycle. Figure 4 shows the corresponding timing diagram.

PERFORMANCE DEGRADATION

It is essential to monitor the effects of changes in the input signal during an analog-to-digital conversion for the different conversion techniques. The output code of an integrating ADC depends on the amount of charing current applied to the capacitor during the first phase of the conversion. A change in the input signal during the second phase will not affect the result. Flash converters take an instantaneous snapshot of the input signal, so the input signal doesn't really change during conversion. However, it must be determined at which point during the conversion time the data is latched from the comparator outputs into the digital encoder.

For SAR-type ADCs the output code may represent any of the voltages between the start and the end of the conversion. Therefore, it is extremely important to keep the input voltage constant once a conversion has been started. The following example shows why. At the beginning of a conversion the input voltage may be just a little bit higher than the value of the MSB. After the first clock cycle the MSB will remain set. If the input voltage decreases during conversion to a value lower than the MSB, the resulting code will be erroneous because the MSB remains switched on. Once a comparator has made a decision it cannot subsequently be changed. However, the successive approximation principle, by its nature, insures that the digital code approximates the actual value, so errors are corrected within a limited band. For that reason the remaining error will never be greater than the voltage change during a conversion and no totally erroneous codes will be generated. At least the magnitude of the error can be estimated that way.

When digitizing an analog waveform, the samples must be taken at precisely determined sampling intervals in order to be able to reconstruct the original signal. Even though some kind of error correction takes place during the conversion time, it cannot be said whether the digital code represents the input signal at the beginning or the end of the conversion time or somewhere in between.

When the analog input signal changes during the conversion time, not only will the output code be erroneous, but some of the codes might also disappear. Since these codes can't be produced with any input voltage, this reduces the effective resolution of the A/D Converter. It doesn't make economical sense to use a 12-bit ADC when only 10 or 8 bits of effective resolution are achieved. As a rule of thumb, the analog input signal should not change more than ½ LSB during the conversion time (which will produce a maximum linearity error of ½ LSB) to maintain specified performance. This is because an ADC with a specified integral linearity error of ½ LSB will not have any "missing codes" and the full resolution is available. If, however, the ADC itself has an integral linearity error of ½ LSB, each additional error, regardless how small it is, can lead to missing codes.

Figure 5a shows a computer program which can be used to simulate an ideal ADC when the input signal changes during conversion. The program reconstructs the function of an ADC by comparing the changing input signal with the output of the internal DAC and issuing a corresponding bit stream to the comparator. The program listing has been simplified for easier understanding and although it is written in HP 85 basic, it can run on any computer after adapting the print format (line 200).

In Figure 5b the appropriate printout of two program runs can be seen. Column 1 shows the number of the clock cycle (cycle 0 is start of conversion) while column 2 shows the actual input voltage. The voltage level here is expressed in LSBs for simplification, but can be converted to any other voltage level by multiplication with a constant factor. Column 3 shows the digital code which is applied to the DAC and therefore compared with the input voltage. The comparator's decision is shown in the next column while the last column shows the SAR output code after the decision. The printout in Figure 5b shows two 12-bit conversions with input voltages of 2047.66 and 2047.67 LSBs, respectively. In both cases, the input voltage changes at a rate of +4 LSBs per conversion. With an analog input of 2047.66 LSBs, the resulting code is 2047; if the input voltage is raised just 0.01 LSB at the beginning of the conversion, the resulting code is 2051. Thus, the three successive codes 2048, 2049 and 2050 cannot be generated if the input voltage changes at a rate of +4 LSBs during the conversion time. This means the effective resolution of the 12-bit converter has been reduced to 9 bits in this case.

```
10 ! R=RESOLUTION
20 ! V1=INPUT VOLTAGE (LSB)
30 ! D=VOLTAGE CHANGE PER CONVE
   RSION
40 ! D1=VOLTAGE CHANGE PER CLOC
   K-CYCLE
50 ! A(I)=BIT WEIGHTS
70 ! C1  = COMPARATOR DECISION
80 FOR I=1 TO R @ A(I)=2^(R-I)
   @ NEXT I   (ARRAY INITIALIZA
   TION)
90 D1=D/R
100 C=0
110 PRINT USING 200 ; 0,V1,0,0,0
120 FOR I=1 TO R
130 C=C+A(I)
140 C2=1
150 C1=C
160 V1=V1+D1
170 IF C>V1 THEN C=C-A(I) @ C2=0
180 PRINT USING 200 ; I,V1,C1,C2
   ,C
190 NEXT I
200 IMAGE 2D,X,6DZ.DD,2X,5D,2X,D
   ,2X,5D  ! (PRINT-FORMAT)
210 END
```

Figure 5A. Program Listing

```
RESOLUTION:        12 BITS
INITIAL VOLTAGE:   2047.67 LSB
CHANGE/CONVERS:    4 LSB

#1      #2          #3   #4     #5
--   ---------      ----  --   ----
 0    2047.67          0   0      0
 1    2048.00       2048   1   2048
 2    2048.34       3072   0   2048
 3    2048.67       2560   0   2048
 4    2049.00       2304   0   2048
 5    2049.34       2176   0   2048
 6    2049.67       2112   0   2048
 7    2050.00       2080   0   2048
 8    2050.34       2064   0   2048
 9    2050.67       2056   0   2048
10    2051.00       2052   0   2048
11    2051.34       2050   1   2050
12    2051.67       2051   1   2051
```

```
RESOLUTION:        12 BITS
INITIAL VOLTAGE:   2047.66 LSB
CHANGE/CONVERS:    4 LSB

#1      #2          #3   #4     #5
--   ---------      ----  --   ----
 0    2047.66          0   0      0
 1    2047.99       2048   0      0
 2    2048.33       1024   1   1024
 3    2048.66       1536   1   1536
 4    2048.99       1792   1   1792
 5    2049.33       1920   1   1920
 6    2049.66       1984   1   1984
 7    2049.99       2016   1   2016
 8    2050.33       2032   1   2032
 9    2050.66       2040   1   2040
10    2050.99       2044   1   2044
11    2051.33       2046   1   2046
12    2051.66       2047   1   2047
```

Figure 5B. Printout

The corresponding input signal frequency can be easily calculated if the conversion time is known. For a popular ADC like the industry standard HS 574, which has a maximum conversion time of 30 µ sec, the corresponding input frequency would have been 16 Hz in this case — pretty low for a reduction from 12 to 9 bits in resolution.

Taking the above mentioned rule of thumb that the input signal should not change more than ½ LSB during conversion time, the following formula can be used to calculate the maximum input frequency.

$$f_{max.} = \frac{1}{2 * Pi * 2^N * \text{conversion time}} \qquad (1)$$

(2^N = number of codes, e.g., 4096 for 12 bits of resolution)

Using this formula, the maximum usable input frequency for the popular HS 574 is limited to 1.3 Hz (!), which is much too low for most applications and would make the high throughput rate of more than 30,000 samples per second unattainable (according to signal theory, two samples per period is sufficient to reconstruct the original signal...).

The above formula is based on the maximum slew rate of the input signal which for sine waves occurs during the zero crossing. Sometimes a slightly different formula (2) is applied which uses the average slew rate of a sine wave instead of the maximum slew rate. But even using this formula, the HS 574 would be limited to input frequencies of 2 Hz.

$$f_{max.} = \frac{1}{4 * 2^N * \text{conversion time}} \qquad (2)$$

What are the implications to the user of this input signal limitation to 1.3 or 2.0 Hz? It simply means, that with input frequencies exceeding that limit, **the specified accuracy of an A/D-Converter cannot be achieved.** The appendix graphically shows the maximum input frequency as a function of conversion time and resolution for any given ADC.

TEST RESULTS

Because the quantitative measurement of the above mentioned errors is quite difficult, a special test set-up has been used to demonstrate the resulting effects and prove theory in practice. The experiment has been made with the HS 574 which is used for a wide range of industrial and military applications. The converter has been used in the 8-bit conversion mode which results in a conversion time of 15 μ sec. This has been done because the graphic resolution of the printer was limited to 256 dots (8 bits), but the results can be converted to any other resolution and conversion time.

The ADC has been selected for the smallest linearity error so that the results reflect the influence of the input signal slew rate instead of the ADC's linearity error. The sample used showed an integral linearity error of less than 0.1 LSB at 12-bit resolution which is about 5 times better than specified.

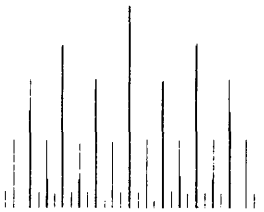


Figure 6A. HS 574 AK, 8-Bit Resolution, Signal Frequency 5000 Hz

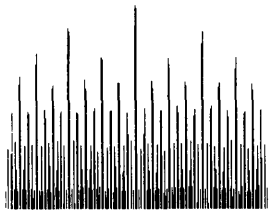


Figure 6B. HS 574AK, 8-Bit Resolution, Signal Frequency 1000 Hz

Figure 6C. HS 574AK, 8-Bit Resolution, Signal Frequency 41 Hz

In the test set-up a triangular waveform (which means a signal with a constant slew rate) was applied to the analog input of the ADC. The signal frequency was 41 Hz which is just the maximum value for an 8-bit converter running at 15 sec per conversion. The sampling frequency of the ADC was chosen so that it was asynchronous with the input signal. The amplitude of the triangular wave was made slightly larger than the input voltage range of the ADC so that the reversing points did not fall into the transfer curve of the ADC.

A large number of samples of the input signal were then taken (about 100,000) and the digital data was fed to a desktop computer for statistical analysis. Figure 6 shows the results of measurements at three different frequencies. The x-axis is scaled from 1 to 254 which represents each output code while the y-axis shows the density of each output code, i.e., how often the particular code occurred during all measurements. With a perfectly linear ADC, you'd expect every possible output code to occur as often as any other code (roughly 400 times for 100,000 measurements at 8-bit resolution). In Figure 6a, which shows the result of the test with a frequency of 41 Hz, it can be seen that this is almost true — the density of the codes in the output spectrum is about the same for each code.

If one of the codes is a so-called "missing code," it will show a density of zero. This can be seen in Figure 6b, where the input frequency has been raised to 1000 Hz. Here more than 50 codes are missing while the remaining codes appear with many different densities. The two codes in the middle of the transfer function (127 and 128) appear more than 1500 times, almost 4 times more than they should. This shows that not only has the resolution been degraded, but the remaining codes exhibit large linearity errors as well. Keep in mind that the same kind of graph would show up at an input frequency of 62.5 Hz (1/16th of 1000 Hz) if the ADC's resolution were 12 bits. Figure 6c shows the results for a frequency of 5000 Hz (or 310 Hz for 12-bit resolution). Only 50 codes remained in the output spectrum while none of the other codes occurred even once during the 100,000 samples that were taken.

HOW TO ELIMINATE THESE PROBLEMS

To obtain the full accuracy and resolution from your ADC, you must insure that the analog input signal does not change during the conversion time, i.e., the input signal must be frozen. This can be done with Sample/Hold (S/H) or Track/Hold (T/H) Amplifiers. (Both amplifier types are similar and can be used for that specific purpose, but only the expression Sample/Hold will be used hereafter.)

In most applications, the digital control input of the Sample/Hold can be driven directly from the STATUS- or EOC- (End of Conversion) line of the following A/D Converter. As long as no conversion is taking place, the Sample/Hold is in the sample mode and its output follows or tracks the input signal. In this mode the S/H functions just like an ordinary buffer amplifier with a gain of 1. As soon as a conversion has been started, this will be indicated by the STATUS-output of the ADC. This forces the S/H to switch from the sample mode to the hold mode, "freezing" the input voltage.

Sample/Hold amplifiers consist of three major building blocks: a capacitor, an analog switch and a buffer amplifier. In the sample mode the switch is closed and the input voltage appears across the capacitor. When entering the hold mode, the switch is opened and the previous input voltage is stored on the capacitor. The amplifier inside the S/H buffers the capacitor voltage and provides a low impedance output to the ADC. Some S/H amplifiers require an external hold

capacitor. This capacitor must be chosen very carefully, otherwise, it will memorize the previously stored voltage. This "memory" is caused by an effect called dielectric absorption. Therefore, only polystyrene or teflon capacitors are suitable for S/H applications because their dielectric absorption is fairly small.

When selecting an S/H amplifier one could be confused with all the data sheet specifications. Below is a short description of the major S/H specifications.

Acquisition Time: After switching from hold to sample mode, the S/H requires some time until the new input signal is acquired (the hold capacitor must be charged to the new voltage). The time which is required until the buffer output has settled within a certain error band to the new voltage is called acquisition time. After an analog-to-digital conversion has been completed, the next conversion cannot be initiated until the S/H has acquired a new input voltage. This delay is the S/H acquisition time.

Aperture Delay: The logic circuit inside the S/H requires some time to detect the S/H command and some time until the analog switch has fully opened. The sum of these times is the aperture delay. For high speed applications where it is important to have very precise timing, the S/H command can be advanced to compensate for this aperture delay.

Aperture Uncertainty: This time is the variation of the aperture delay from one sample to the next one; it is sometimes called aperture jitter. This time is roughly 100 times less than the aperture delay and it determines the maximum usable input frequency for S/H amplifiers.*

Hold Mode Settling Time: Every time the S/H switches from sample to hold, a glitch pulse can be seen at the output. The time required for the output to settle before the ADC's comparator makes the first (MSB) decision is the hold mode settling time.

Sample-to-Hold Offset: This offset or pedestal is caused by a charge transfer of the analog switch when switching from Sample to Hold mode. As long as the resulting offset is linear with input voltage, it will be noticeable only as a small gain change and can be trimmed out easily.

Droop Rate: Due to leakage and bias currents the hold capacitor cannot hold the stored voltage indefinitely and therefore, it will discharge. This discharge is specified as Droop Rate and it must be kept in mind that Droop Rate normally doubles for every 10°C rise in temperature.

* The maximum frequency can be calculated with the formulas (1) and (2). In the formulas conversion time has to be substituted with aperture jitter.

While the S/H eliminates many analog signal processing problems, it also has some drawbacks. Due to non-linearity of the Sample/Hold offset and other effects, the S/H will always add errors to the following ADC. If, for example, the S/H is specified for use in 12-bit linear systems, a S/H nonlinearity of 0.012% will be specified in the S/H data sheet, which equals ½ LSB at 12 bits. If you sum this error up with the ½ LSB linearity specification of the following ADC, the worst case linearity error will be 1 LSB which means that the **system accuracy** has been degraded to 11 bits. It also might be necessary to adjust the output offset of the S/H in addition to the offset adjustment of the ADC.

SINGLE PACKAGE SOLUTION

To overcome these disadvantages and still use the benefits of a S/H, Hybrid Systems has introduced the HS 9474, a 12-bit A/D Converter with built-in S/H amplifier. The ADC used in this device is the industry standard HS 574. All functions of the HS 574 such as microprocessor interface, software controlled 8- or 12-bit conversion and internal reference voltage are also available with the HS 9474. The Sample/Hold command input of the S/H is directly connected to the STATUS output of the ADC so that the S/H is automatically in the hold mode during conversion and is switched back into the sample mode as soon as the conversion has been completed.

The specifications of the HS 9474, such as linearity, temperature drift and conversion time are identical to those of the HS 574 but with the S/H amplifier included. This means the errors of the S/H do not add to the errors of the ADC; they are included in the ADC specifications. The required hold capacitor is also included in the HS 9474, eliminating the need for external components and the possibility of errors due to dielectric absorption of the capacitor.

Figure 7 shows the block diagram of the HS 9474. It is important to notice that the HS 9474 is pin compatible with the HS 574. This allows existing designs which use a S/H amplifier to be upgraded to the HS 9474 without any hardware or software modifications. Also, universal A/D interfaces can be equipped with the HS 574 or HS 9474 depending on the application. In all existing designs where a 574 is used with an external S/H amplifier, the 574 and the S/H can be replaced by a HS 9474 when a connection is made from the input to the output pin of the S/H layout. This not only reduces the cost for stock and incoming inspection (one component instead of 2-4), but also improves system accuracy and even maintains compatibility to the existing design.

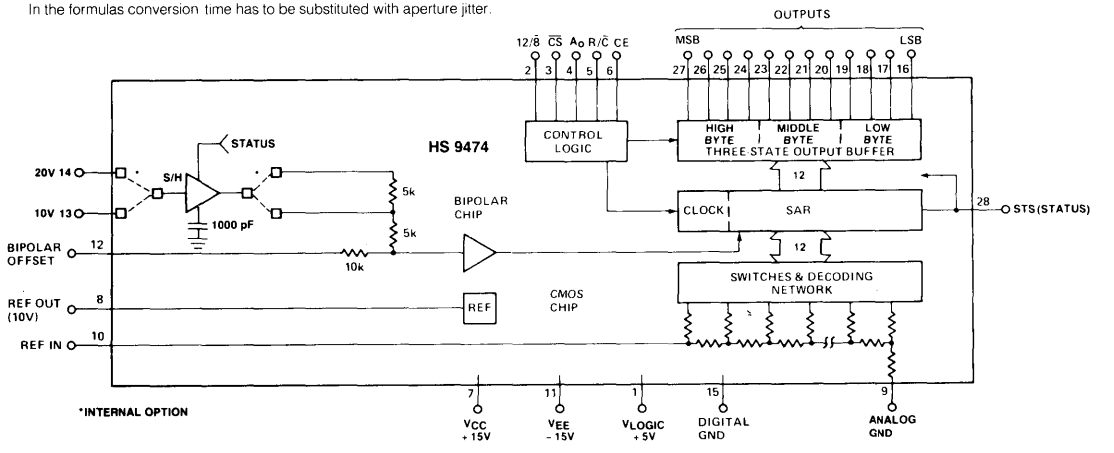


Figure 7. HS 9474 Functional Diagram

Attention must be paid to the acquisition time of the S/H amplifier. To acquire a new analog signal, a time span of 10 μ sec (max) is required between two consecutive conversions. Because the output data of the ADC must be read and stored in memory, this time span is available in almost any application. While the digital data is transferred, the S/H already acquires the new input signal. Unlike the HS 574, the input impedance of the HS 9474 is very high eliminating the need for additional buffer amplifiers. Due to the relatively low input impedance of the 574 (3 to 14k ohm), a buffer amplifier is required if the signal source doesn't have a very low output impedance.

BUILDING DATA ACQUISITION SYSTEMS WITH THE HS 9474

Due to the high input impedance of the HS 9474 only a single analog multiplexer is required to build a multichannel Data Acquisition System (DAS). The ON-resistance of the multiplexer can be neglected compared to the input impedance of the HS 9474. The schematic of such a DAS with eight single-ended inputs is shown in Figure 8. For differential measurements, as required when common mode voltages are superimposed on the input signal, the circuit can be expanded with a second multiplexer and an instrumentation amplifier as shown in Figure 9. The resistors R1 and R2 can be used to control the gain of the amplifier in a wide range. If it is required to change the gain from one channel to the next, small reed relays can be used to switch different resistors, one for each gain setting. But for more than two or three gain settings, the use of a digitally programmable gain amplifier is recommended. Such an amplifier is the HS 2020 which has fixed gains of 1, 2, 4, 8, 16, 32, 64 and 128. The gains can be programmed with a 3-bit binary code. Figure 10 shows the building blocks for a DAS with a very high dynamic range.

As an alternative to building a DAS with functional blocks, Hybrid Systems offers the HS 9410 series and the HS 9404/9408 series. These are complete DAS' as shown in Figures 8-10 packaged in one hybrid. The advantages of less board space, less inventory, simpler manufacturing and quickness to market may be beneficial to you.

INTERFACING THE HS 9474 TO AμP

A built-in microprocessor interface allows easy interfacing of the HS 9474 to both 8- and 16-bit microprocessor systems. The device can also be operated in a stand-alone mode. The converter provides an A_0 address input which is normally connected directly to the LSB of the address bus. In memory mapped applications two adjacent memory locations are allocated to the device and from a software point of view, the HS 9474 is treated like an ordinary random access memory. Start of a conversion is achieved by writing any data byte into one of the two corresponding addresses. Depending on which of the addresses was chosen, either an 8-bit or a 12-bit conversion is started.

The STATUS-output of the converter is set to a logic high level during conversion and returns back to a low level as soon as the conversion is completed. Once a conversion is started, there are several methods to detect the end-of-conversion and to read the data. For example, the STATUS-output can be used to cause a hardware interrupt by connecting the STATUS line to the IRQ input of the processor. An interrupt service routine then can be used to read the data.

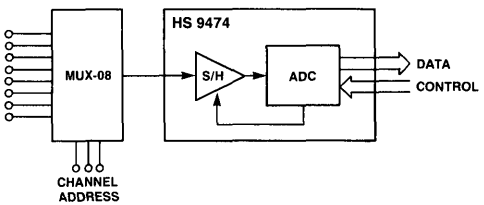


Figure 8. Block Diagram of an 8-Channel Data Acquisition System

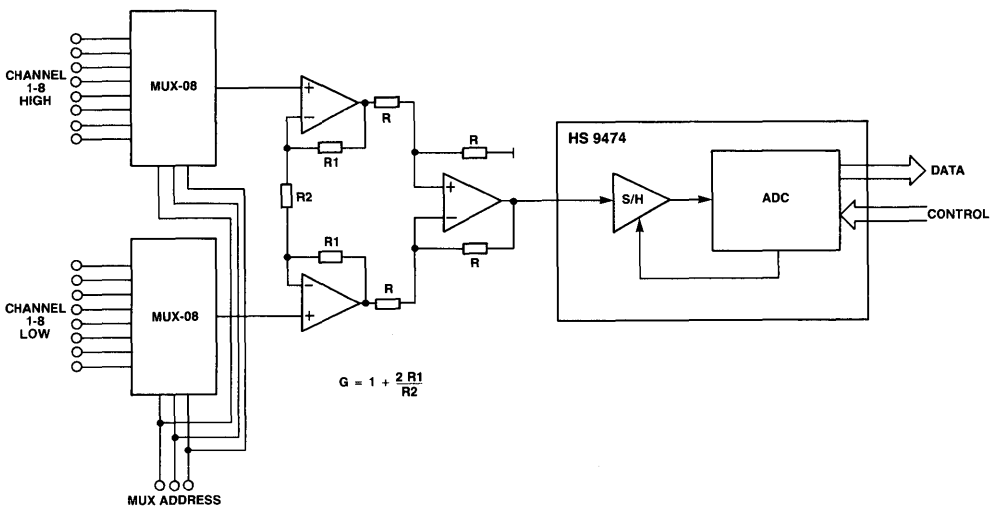


Figure 9. Data Acquisition System with 8 Differential Channels

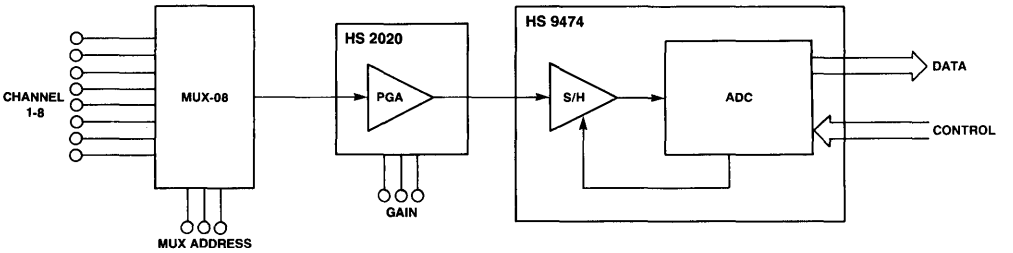


Figure 10. Data Acquisition System with Digitally Programmable Gain Amplifier

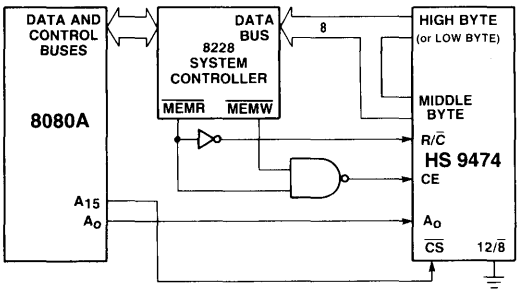
But in order to achieve the maximum conversion rate this method is not very practical because serving an interrupt requires many processor cycles (saving and restoring all register information). Another possibility is to connect the STATUS line to an input port and to read that port until conversion is completed. Also just a couple of NOP statements can be inserted in the software after the start command. The amount of the NOP commands must be chosen in accordance with the processor cycle time so that a minimum time gap of 30 μ sec is inserted between the start of conversion and the data read procedure. This method has the disadvantage that even if the converter operates at a higher speed (25 μ sec typical), the time gap must be 30 μ sec long to be within the maximum specification of the conversion time.

However, the best method to interface the HS 9474 to a processor is to suspend all processor operation during conversion. This can be done by connecting the STATUS-output to the WAIT- or HALT-input of the processor; in some cases little additional hardware such as gates or inverters is necessary. When writing the software, the data read instructions directly follow the conversion start command. As soon as a conversion is started, the processor stops operation and all bus and control lines are absolutely quiet. This greatly reduces the possibility of noise pick-up in the analog signal or the converter itself. As soon as the conversion is completed, the processor resumes operation and continues in the software to read the output data.

The data format can be chosen by means of the 12/8 input of the HS 9474. If this input is at logic high level, the data format is 12-bit parallel; if it is low, the data is available in two 8-bit bytes which are addressed using the A_0 line. One byte contains the upper 8 bits, while the other one contains the 4 remaining bits followed by 4 trailing zeros. The data format in the 8-bit mode is therefore left-justified.

Figures 11a and 11b show how to interface the HS 9474 to the popular microprocessors 8080A and 8048. For the 8080A no address decoding is shown; depending on system complexity an address decoder might be necessary to generate the Chip-Select signal.

The data outputs of the HS 9474 are able to drive one standard TTL load. For systems where this is not sufficient, an additional bus driver (e.g., 74LS245) must be placed between the data outputs and the bus. The output buffers inside the HS 9474 are built-in CMOS technology, so pull-up resistors are not required for CMOS processor systems. The data outputs are switched into high-impedance (tri-state) if Chip-Select or Chip-Enable are not valid or the STATUS-output is logic high.



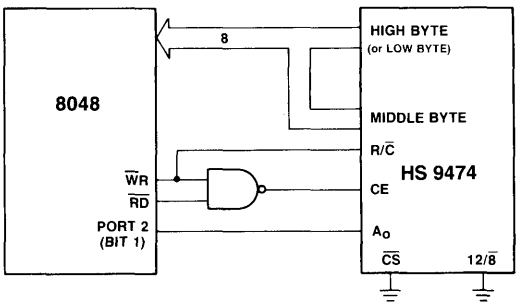


Figure 11A. Interfacing HS 9474 to 8080A μP (Top)

Figure 11B. Interfacing HS 9474 to 8048 μP (Bottom)

HELPFUL HINTS WHEN USING A/Ds

When using A/D converters, some design rules must be obeyed to achieve the desired accuracy. One should keep in mind that for 12-bit resolution and 10 volts full scale range, ½ LSB corresponds to just 1.22 mV. However, the comparator inside an ADC must be capable of making accurate decisions with much smaller voltages. In digital circuits the noise margin is in excess of a couple of hundred millivolts, but for analog circuits the noise margin is absolutely zero. Therefore, already small amounts of noise might have an effect on the ADC and this noise must be kept far away from such components.

Care must be taken when selecting the power supplies. In particular, switching power supplies often have high frequency noise in excess of 100 mV on their outputs. The ability of the ADC to suppress changes in the power supply voltage is specified as Power Supply Rejection Ratio, PSRR. But this specification only applies to DC changes such as long term drift of power supply voltages. With increasing frequency the suppression of variations in voltage decreases rapidly, so that high frequency noise is not suppressed at all. If possible, the analog supply voltages of an ADC ($\pm$ 15 volts) should be produced with linear regulated power supplies. Careful bypassing of all power supplies directly at the converter package is very important. A tantalum capacitor in parallel with a multi-layer ceramic capacitor should be used.

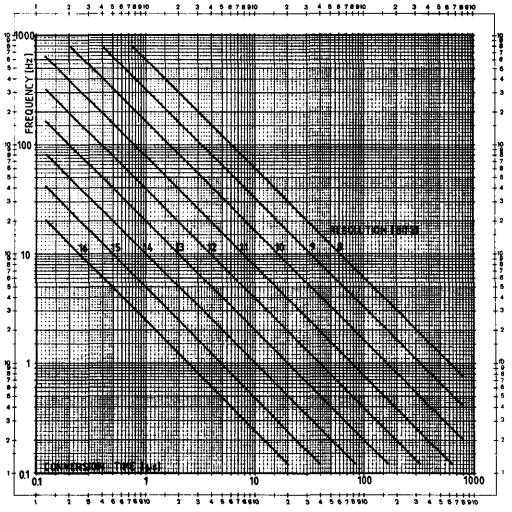
Correct layout of the ground lines is extremely important to the function of the ADC. To avoid ground loops, all ground lines of a system should be connected at one "star-point" which should be located as close to the ADC as possible. Generally, ground lines should be of very low impedance. Therefore, wide ground runs on the PC board should be used. If possible, a ground plane should be located directly underneath the converter package. This ground plane can also be used to connect analog and digital grounds. In some cases it might even be necessary to shield the converter package from the top.

However, the best protective measures are useless if the analog signal itself is superimposed with noise. In this case the input signal must be filtered and shielded cable should be used to connect the analog signal to the board.

If any problems persist while designing in a Hybrid Systems' A/D Converter, one should not hesitate to contact the factory for technical assistance. We know our product very well and our applications engineers will be able to assist in solving any problems you may have.

APPENDIX

Nomogram to determine the maximum input frequency versus resolution and conversion time of ADCs without S/H amplifiers.



Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

QUAD S/H SOLVES ACQUISITION PROBLEMS

1

As users of data acquistion systems become more sophisticated and their applications become more complex, the limited capabilities of simple systems become apparent. Two new quad sample/hold amplifiers from Hybrid Systems allow circuit designers to optimally address increasingly complex data conditioning and acquisition problems.

In a simple data acquisition system (DAS), the usual method of digitizing multiple inputs utilizes an input multiplexor (see Figure 1). This configuration utilizes a minimum of hardware to sequentially sample and digitize the multiple channels. The timing required is shown in Figure 1b. The time to sample any channel will consist of the sum of at least three delays. First is the acquisition time of the S/H, which is the amount of time required for a worst case input voltage swing to settle out to the required accuracy at the hold capacitor. Second would be the aperture delay time, the finite time required to actually switch the S/H into hold mode. Because this time represents a delay, it can be pipelined out of the total time by applying the "hold" command earlier. When pipelined, the next will be the hold-mode settling time, the delay while the output buffer of the S/H settles out from the hold-mode switching transition. Third is the specified conversion time of the A/D converter. A fifth time, that for the multiplexor to switch channels, is usually pipelined to occur while the S/H is in hold mode, again not affecting the total aggregate system sampling rate.

Assigning some typical numbers to these times gives an interesting view of the efficiency of such a system. Table 1 shows that for a fast A/D converter, the large acquisition time (7 μs) is the bottleneck limiting a 500 kHz A/D to a 102 kHz aggregate throughput rate. Even with a slower A/D converter this time can prove to be troublesome. Consider the design of a four-channel time division multiplexor for four telephone channels. A 25 μs A/D (40 kHz) proves too slow to sample the four channels at 8 kHz each if the prescribed 7 μs worst-case acquisition time is allowed.

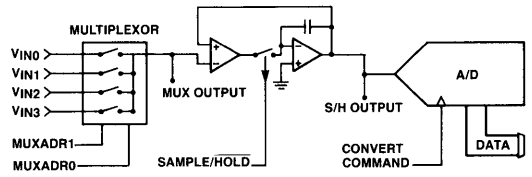
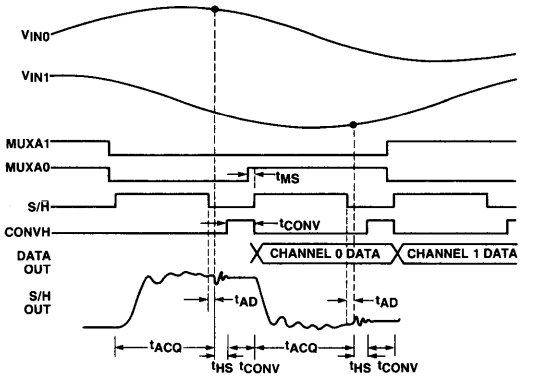


Figure 1A. Simple Sequential Four-Channel DAS



t_{ACQ} = ACQUISITION TIME
t_{HS} = HOLD MODE SETTLING TIME
t_{CONV} = A/D CONVERSION TIME
t_{AD} = APERTURE DELAY TIME
t_{MS} = MUX SWITCHING TIME
t_{CYCLE} = TIME REQUIRED TO DIGITIZE ALL FOUR CHANNELS

$t_{CYCLE} = (4)(t_{ACQ} + t_{HS} + t_{CONV})$

ASSUMING:
t_{ACQ} = 7 μs MAX
t_{HS} = 800 ns MAX
t_{CONV} = 2 μs MAX
t_{CYCLE} = 39.2 μs
∴ PER CHANNEL SAMPLING RATE = 25.5 kHz

*NOTE THAT t_{AD} AND t_{MS} HAVE BEEN PIPELINED FOR MAXIMUM SAMPLING RATE

Figure 1B. Timing

	Simple Sequential DAS	Simultaneous Sampling DAS	Pipelined Acquisition DAS
Maximum Aggregate Sampling Rate (Assuming 2 μ s A/D)	102.0 kHz	183.4 kHz	250 kHz
Maximum Per Channel Sampling Rate (2 μ s A/D, 4-Channels)	25.5 kHz	45.9 kHz	62.5 kHz
Maximum Aggregate Sampling Rate (25 μ s A/D)	30.5 kHz	35.1 kHz	37.0 kHz
Maximum Per Channel Sampling Rate (25 μ s A/D, 4-Channels)	7.6 kHz	8.8 kHz	9.3 kHz

Table 1. Maximum Data Throughput Rates for Four-Channel Data Acquisition Systems

Another characteristic of the simple DAS is the amount of stress that it applies to the S/H. The one S/H must be switched at the full conversion rate and with minimum sample-mode time to get maximum throughput. The required maximum slew rate in this configuration will be a full scale transition before adjacent conversions, even though each separate input signal must be antialias filtered to less than 1/4 of this rate (for a four-channel system). Because of the time multiplexing of the input to the sample/hold, even slowly changing signals will require maximum slew rate if one signal is near full scale and the next near negative full scale. Failure to observe maximum acquisition time specifications will lead to non-settling of the sample/hold independent of the input signal slew rate. Indeed, non-settling will show up as adjacent channel feedthrough or for worst-case situations as differential linearity aberrations near the major carry codes (for a successive approximation converter where the initial major-carry test is fooled by non-settling).

A final characteristic of the simple sequential DAS is the time delay between the samples of each channel. When time and phase relationships between the channels are important aspects of the system being monitored, these delays make the simple DAS unuseable. Consider the class of problem where multiple inputs are used to infer a multidimensional parameter of interest. A straightforward example is a robotic controller for a mechanical arm. Four channels are used to represent the x, y, z and rotational position of the arm. The instantaneous position of this arm would be very difficult to control during complex motions without simultaneous sampling of the four-dimensional vector.

Another example problem occurs during modal analysis, the testing of a structure's response to vibration. Multiple accelerometers are placed at a spacing determined by the expected maximum spatial frequency of the bending modes. A calibrated impact is applied to the structure and the resulting accelerations are sampled. From the multiple channels a two- or three-dimensional map of acceleration, velocity and displacement can be generated. Any time skew in the samples will badly distort the spatial relations between the sensors and thereby distort any two- or three-dimensional reconstruction. This technique is used with finite element analysis to verify earthquake survivability of skyscrapers and the structural stability of airplanes. Other three-dimensional reconstruction techniques are used in seismic data analysis for oil exploration and earthquake studies.

Another example of problems exists in an application where the spectra of two channels must be compared or correlated. The phase shifts between various channels are plotted versus input frequency in Figure 2. It can be shown that the time delay between the channels will apply a systematic error term of difference between the spectrums' mathematical descriptions. This shows up in the imaginary part of the spectrum as a linear slope.

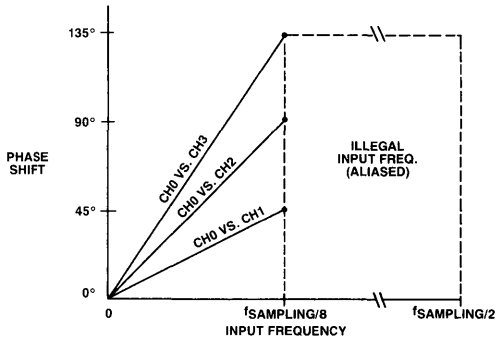
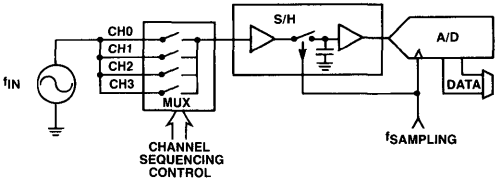


Figure 2. Phase Shift Between Channels Versus Input Frequency in Four-Channel Sequential Sampling DAS (shown below)



The optimal DAS architecture for these types of problems is one with a sample/hold for each channel with all channels simultaneously sampled, then converted sequentially. Figure 3 shows a simultaneous DAS architecture and timing. Notice that for an n-channel system only one acquisition time delay is required per n channels converted. A four-channel system using the same A/D converters as before yields aggregate throughputs of 183.4 kHz and 35.1 kHz, respectively (see Table 1.). Notice that the hypothetical telephone time division multiplexor is now feasible using a 25 μs A/D due to the throughput gain. Each input channel must be band limited to one quarter of the Nyquist frequency, which means that the maximum slew rates at each sample/hold will be one quarter of that in the simple sequential system. This implies that each channel will show less dynamic settling error. Finally, the samples will show time delays of less than 5 ns between each other, preserving the phase information between the channels.

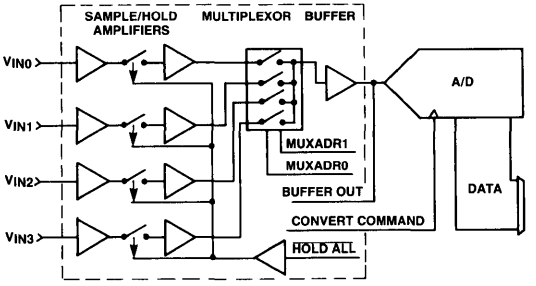
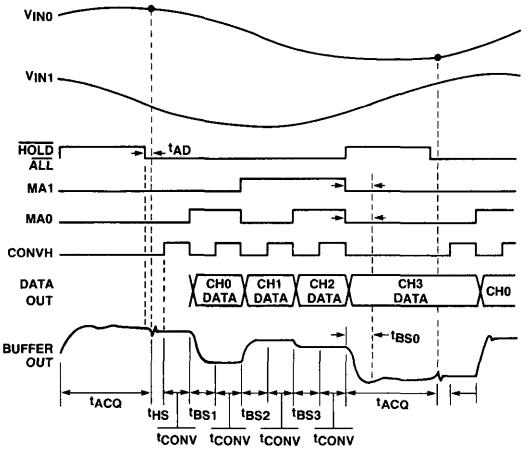


Figure 3A. Simultaneous Sampling DAS Using HS 9704



t_{BS} = MUX SWITCHING AND OUTPUT BUFFER SETTLING TIME

t_{CYCLE} = TIME REQUIRED TO DIGITIZE ALL FOUR CHANNELS

t_{CYCLE} = (1) (t_{ACQ} + t_{HS} + t_{CONV}) + (3) (t_{BS} + t_{CONV})

ASSUMING: t_{ACQ} = 7 μs MAX, t_{HS} = 800 ns MAX, t_{CONV} = 2 μs, t_{BS} = 2 μs MAX

t_{CYCLE} = 21.8 μs

∴ PER CHANNEL SAMPLING RATE = 45.87 kHz

*NOTE THAT t_{AD} AND t_{BS0} HAVE BEEN PIPELINED FOR MAXIMUM SAMPLING RATE

Figure 3B. Timing for Simultaneous Sampling DAS Using HS 9704

While the simultaneous sampling DAS increases throughput substantially, even more throughput can be obtained by pipelining the acquisition time entirely out of the total cycle time. A pipelined DAS and its timing is shown in Figure 4. After the pipeline is filled (11 μs for the example in Figure 4), the system can continuously convert samples at a 250 kHz rate (assuming a 2 μs A/D) or 37 kHz for the 40 kHz A/D (as in Table 1). Again the slew rate settling requirements upon the sample/holds are minimized, yielding better dynamic performance. The phase shift between channels is minimized, but still very significant. When maximum throughput is the design goal, a pipelined DAS makes the most sense.

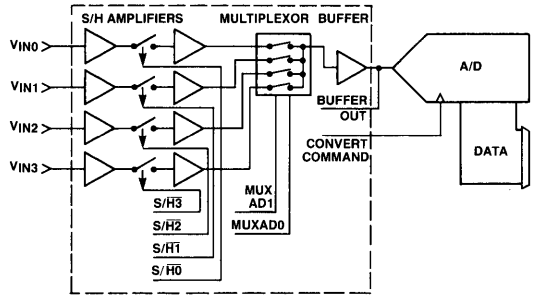
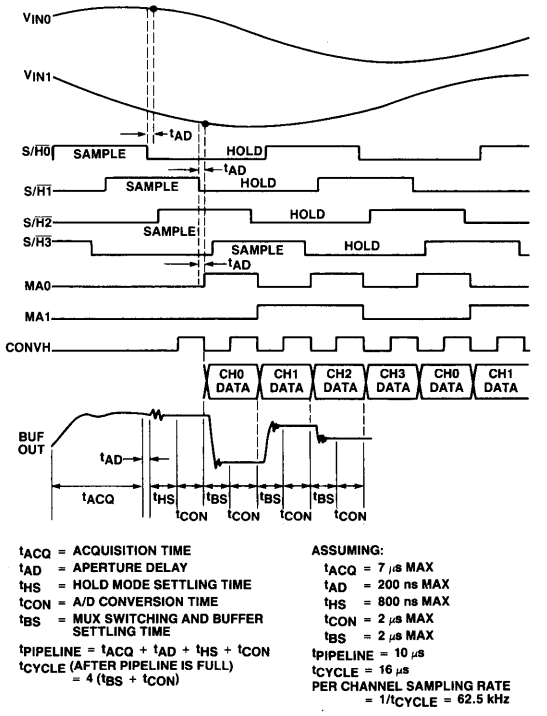


Figure 4A. Pipelined Acquisition DAS Using HS 9705



t_{ACQ} = ACQUISITION TIME
t_{AD} = APERTURE DELAY
t_{HS} = HOLD MODE SETTLING TIME
t_{CON} = A/D CONVERSION TIME
t_{BS} = MUX SWITCHING AND BUFFER SETTLING TIME
$t_{PIPELINE} = t_{ACQ} + t_{AD} + t_{HS} + t_{CON}$
t_{CYCLE} (AFTER PIPELINE IS FULL) $= 4(t_{BS} + t_{CON})$

ASSUMING:
t_{ACQ} = 7 μs MAX
t_{AD} = 200 ns MAX
t_{HS} = 800 ns MAX
t_{CON} = 2 μs MAX
t_{BS} = 2 μs MAX
$t_{PIPELINE}$ = 10 μs
t_{CYCLE} = 16 μs
PER CHANNEL SAMPLING RATE $= 1/t_{CYCLE}$ = 62.5 kHz

Figure 4B. Pipelined Sequential Data Acquisition System Using HS 9705

An interesting class of problem can be addressed by hardware identical to the pipelined system above. A fast "window grabber" system can be used to sample a limited number of points spaced much closer in time than the A/D conversion rate. For example, consider an eight-channel pipelined hardware system where each of the channels is connected to the same input. If the problem at hand involves analyzing eight points spaced 1 μs apart (to examine the impulse response of system, for instance), it is possible to stagger the hold commands to each channel by 1 μs to "grab" eight points with 1 μs spacing. The multiplexor is then used to route the samples to a slow A/D to sequentially convert them in non-real time.

In order to support the various applications mentioned above, Hybrid Systems has announced two different versions of quad multiplexed sample/holds. The HS 9704 is a binary encoded model. Each sample/hold can be uniquely addressed by a binary address for ease in μP interfacing. It also supplies an overriding "hold all" single control in order to simplify the design of simultaneous S/H systems. An implementation of a simultaneous sampling system is shown in Figure 5.

This synchronous circuit uses programmable counters to set various time delays. Converters of various speeds can be substituted by changing the programmed delays (possibly by use of dip switches) or by adjusting the master clock frequency.

The first programmable delay represents the sample-mode acquisition time of the S/H. A 7 μs acquisition time requires 56 clock periods of an 8 MHz clock. The most significant bit counter will output a terminal count when it counts to all ones. This occurs during count 1111 0000 = 240 Base 10. We use the leading edge of the 57th count to clear a flop and terminate the sample mode. Therefore, the preset data on the acquisition time counters is set to 240 − 57 = 183 Base 10 or 1011 0111 binary.

The next delay, the multiplex time, represents the amount of time each channel of held signal must be applied to the output buffer during each conversion. This time is equivalent to Tbs + Tcon, the output buffer settling time plus the A/D conversion time. For a per channel sampling rate of 8 kHz, we can allow up to 29.75 μs for this time. This is equivalent to 238 periods of an 8 MHz clock. In order to prevent terminal count glitching, we use up two clock periods to sequentially load and then enable the counters. Therefore, the multiplex time data inputs are set to 240 − 239 + 2 = 3 or 0000 0011 binary.

The fastest simultaneous system requires that the first buffer settling time be pipelined to occur during the acquisition time. However, each successive channel requires a completely symmetric sequence of control up to and including the nth channel. If we postulate symmetric timing for all four-channel conversions (in order to simplify the hardware), the beginning point of that symmetric cycle would occur before the end of the acquisition time. Specifically, it would occur Tbs − (Ths + Tad) before the end of the acquisition time. For Tbs = 2 μs, Ths = 800 ns and Tad = 200 ns, we require this symmetric cycle to start 1 μs before the hold mode is entered. Since we previously set the entrance to hold mode to occur after 56 counts, we need to decode 1 μs or 8 counts prior to entering hold mode. This must be done carefully to avoid glitching caused by asymmetric rise and fall times on the counter outputs. The magnitude comparator P = Q output could be used by synchronously clocking it into a flop at a cost of another flop and one clock period delay. The P > Q output goes low one count after the selected count but doesn't glitch. This output is used by applying 240 − 8 − 1 = 231 Base 10 or 1110 0111 binary at the symmetry start data inputs.

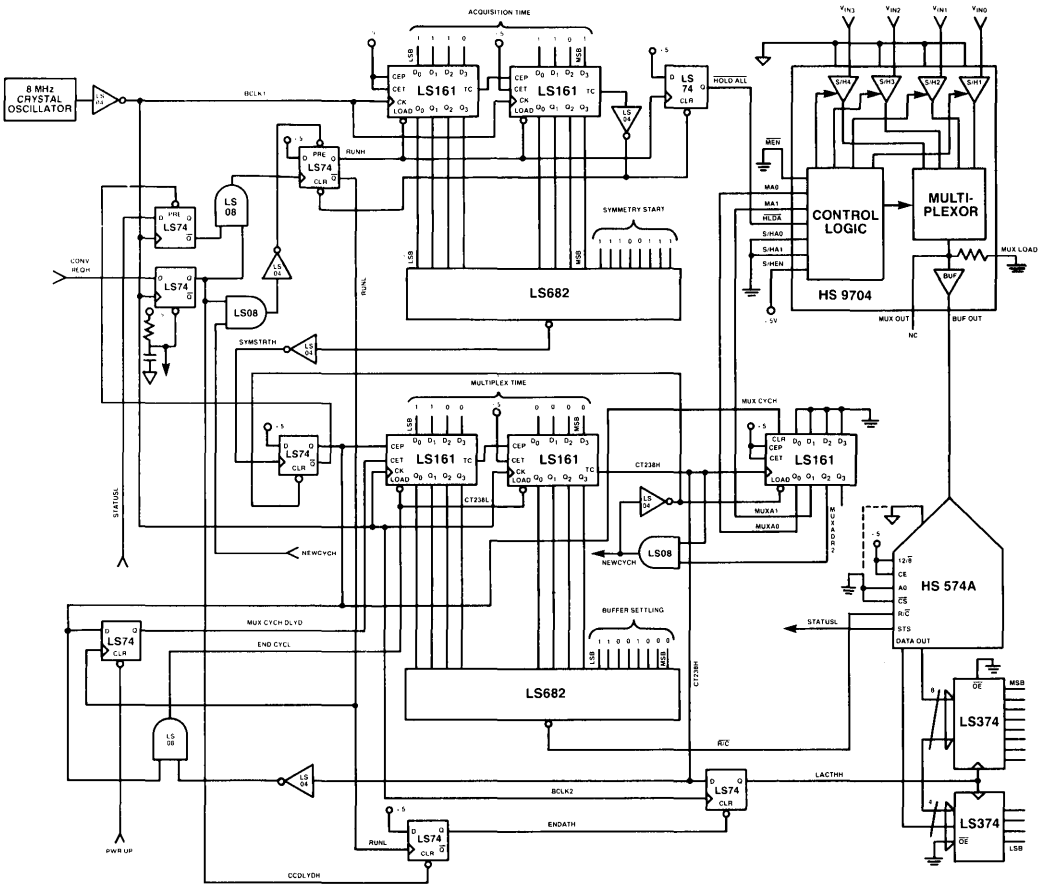


Figure 5. Four-Channel Time Division Multiplexing 12-Bit DAS Utilizing Simultaneous Sampling

The industry standard HS 574A A/D converter is an asynchronous device which requires a pulse to start. The simplified conversion time shown in Figure 3 must be further subdivided into a start pulse time, a true conversion time and a data latch time. By decoding one count of an 8 MHz clock we can supply a 125 ns start pulse (R/C*). The first pulse should occur Ths + Tad after entering hold mode. The next three pulses should occur Tbs after the multiplexor is switched. Because we initialize the multiplex time counter early, these two required timings can be generated by the same circuit, and the timing becomes symmetrical. The HS 9704 buffer settling time is 2 μs. Therefore, we set the buffer settling delay data inputs to decode 16 counts after the preset multiplex count of 3, where 16 + 3 = 19 Base 10 or 0001 0011 binary. Again, the P = Q output can glitch due to input rise/fall time differences. The 574 needs a minimum start pulse width of 50 nsec, so glitches don't start it; but at a cost of another flop the P = Q output could be synchronously clocked. This would require applying data to decode one clock earlier (data = 0001 0010).

The output data can be latched anytime between the end of the A/D conversion and the next R/C* (start) pulse. The simplest circuit latches data one clock after the multiplexor channel is switched. To insure that no false data is latched, this pulse is not enabled until after the first acquisition. Dropping the convert request level also disables output data and eventually reinitializes the logic.

The maximum true conversion time allowable runs from the rising edges of R/C* to the mux channel switch pulse (ct238h). Quantitatively this is equivalent to the multiplex time minus the buffer settling delay minus the R/C* pulse width, assuming that the multiplex switching and the data latching overlap for a small pipeline effect. In this example, the multiplex edge time is 237 counts, the buffer settling (Tbs) = 16 counts and R/C* = one count, so the maximum true conversion time at the A/D is 220 counts or 27.500 μs. This specification is met by the Hybrid Systems HS 574A, an industry standard 12-Bit A/D converter with 27 μs maximum conversion time over the military temperature range. The HS 9704/5 can be obtained in military temperature grades also, so that if 541s logic is used in the application circuit, the whole DAS should function over temperature.

The HS 9705 incorporates unencoded direct control of each sample/hold. This feature allows the sampling times of each channel to be staggered in order to support pipelined system applications. A simultaneous sampling system can still be implemented by tying S/H0 through S/H3 together externally, then pulsing them in the same manner as a "hold all" control. An implementation of a pipelined DAS is shown in Figure 6.

This application circuit takes advantage of the 16 μs total cycle time achievable with a sub-two μs converter like the HS 9520. This modulo 2 cycle time allows the 4-Bit binary counters to run open loop from clear using a 1 MHz clock. Again, the simple conversion time of Figure 4 must be subdivided into a start pulse time, a true conversion time, and a data latch time. The 8 MHz master clock allows the conversion time to be synchronously subdivided to decode these pulses.

In operation the begin h level is brought high and the counters start from clear on the next 8 MHz clock. From this starting point (run h = 1) until the time decoded by the '1s20 (7 μs here) will be the acquisition time for the first channel. This channel is then put in hold mode until the next cycle starts at 4 (Tbs + Tconv) = 16 μs.

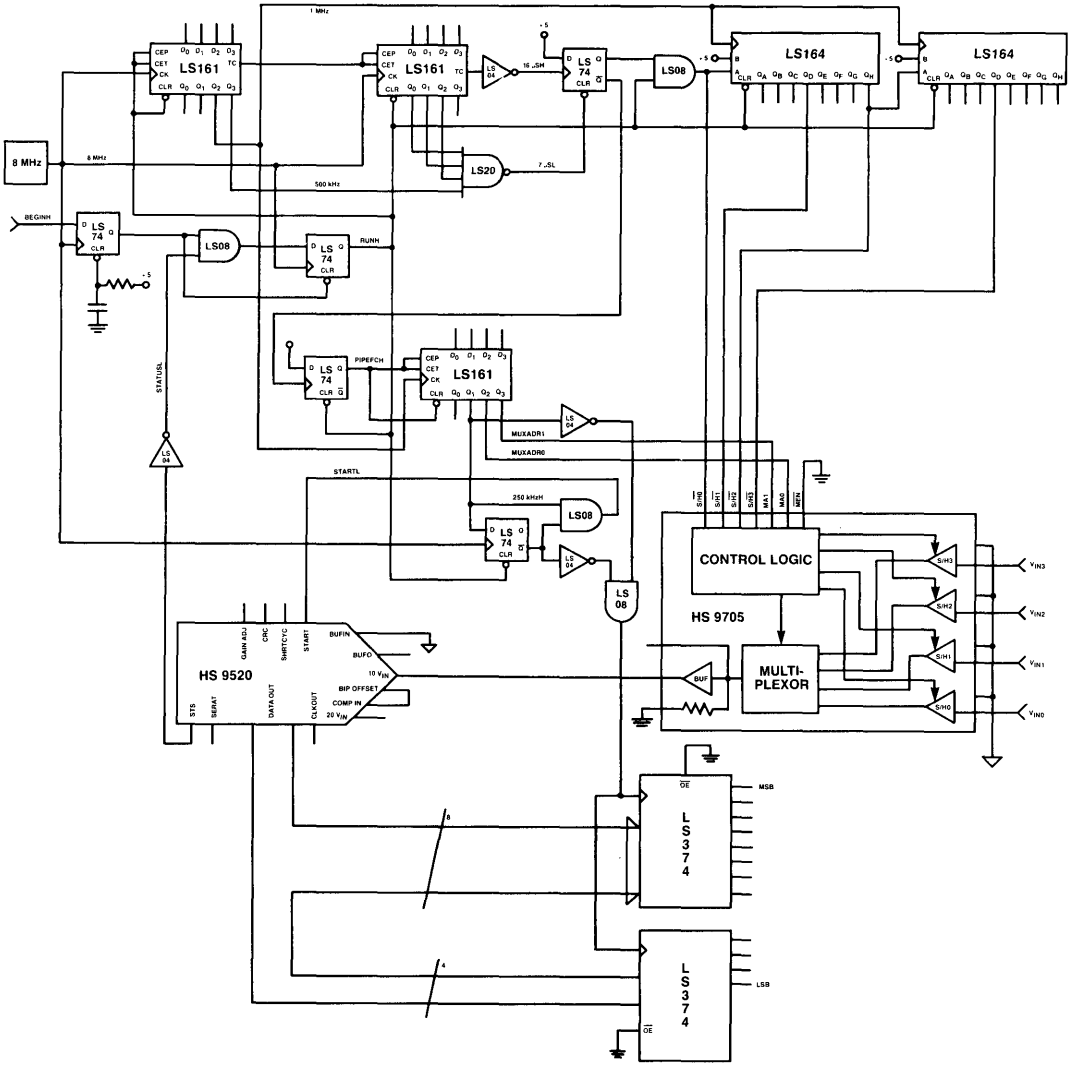


Figure 6. Pipelined Acquisition DAS for 250 kHz Throughput Using HS 9705

In general, the next channels must have identical timing on their S/Hn* lines, except that each must be delayed by (Tbs + Tconv), here equal to 4 μs. This can be accomplished with minimal hardware by simply delaying the original signal by 4 μs taps using LS164 shift registers. No end-of-cycle reset is necessary as the 4-Bit counters roll over at the 16th count.

The timing of Figure 4 shows that the optimum system would have its first conversion initiated at Tad + Ths after the end of the first acquisition time. This is 1 μs for Tad = 200 ns and Ths = 800 ns. For simple, symmetric hardware, this circuit initiates the first conversion at a Tbs delay (2 μs), which incurs a one-time 1 μs penalty in filling the pipeline. This is legal because the aperture delay is included in the Tbs specification on the data sheet. Note that a 200 ns aperture delay would otherwise become significant (a 10% longer (Tbs + Tad) delay would be required before each conversion if Tad isn't pipelined as in Figure 4).

The mux address counter gets enabled from clear after the first acquisition (at 7 μs). Two μs later the divide-by-four (250 kHzh) output goes high. This edge is delayed by almost 125 ns by the flip-flop and the two signals are gated to provide a start pulse to the HS 9520. At the falling edge of the start pulse the conversion begins and the status output goes high. Output data is valid after the status line goes low, 1.5 μs later.

The start pulse occurs during the first 125 ns of the "simple conversion time." The converter must complete its conversion within 1.875 μs, because at that point the multiplexor will be commanded to switch and the analog input will soon begin to change. Output data will be valid for 2.125 μs and can be latched anytime within this window. The simplest implementation is also the fastest and uses the inversion of 250 kHzh to latch data at 1.875 μs after the start of true conversion.

The HS 9704/5 quad multiplexed S/H's provide three of the major building blocks of a multichannel data acquisition system within one 24-pin double dip. The addition of an A/D of the required speed and control logic form a complete four-channel DAS, expandable in four-channel increments. The choice of control logic offered by the otherwise identical units allows for the design of sophisticated systems optimized for throughput or the required application. Making use of the internally trimmed offsets and pedestals and the temperature tracking allows the designer to construct unusual systems of high accuracy. "Window grabbers" require no extra external parts. The use of two parts and an external differential op-amp completes a two-channel true differentiator ($y(t) = x(nt) - x(nt-1)$). As A/D converter speeds continue to rise, the sophisticated system designer will increasingly turn to integrated subsystems such as these for system solutions.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

CMOS DACS
IMPORTANT CONSIDERATIONS ABOVE 12-BITS

1

BACKGROUND

High resolution data converters are now more than just a design curiosity in current circuit designs. In particular, with the price of digital to analog converters becoming more cost efficient designers are increasing system performance with little increase in parts cost. The new 16-bit CMOS DAC's are now selling for what used to be the price of 14-bit DAC's and 14-bit DAC's are now replacing 12-bit DAC's for more demanding applications. The evolution from large rack mounted DAC's to modules and now to hybrids and monolithic devices has been made possible by the optimum use of each technology. Modules could accommodate precision resistors and individual bit trims along with thermal blankets (ovens) to achieve the desired stability. However, modules have been limited in terms of circuit density and reliability. With the development of CMOS IC technology along with the maturation of deposited resistor technology, circuit designs have taken full advantage of these advances to the benefit of the user.

Hybrid Systems has been a leader in the design and production of high resolution hybrid and IC DAC's. Recognizing the benefits of both CMOS and resistor technology Hybrid Systems has introduced important and innovative products . . . many of these products were industry firsts and are listed below:

DAC370. Industry's first hybrid 18-bit MDAC linearity 0.0008% (16 bits) with input registers.

DAC377. Industry's first complete 18-bit DAC linearity 0.0008% with output amplifiers and reference.

DAC9331-16. Industry's first 16-bit MDAC with 0.0008% accuracy and guaranteed monotonic over temperature to 16-bits with internal latches.

DAC9377-16. 16-bit 0.0008% accurate complete DAC with voltage output and internal reference. Also available in 4 BCD.

HS 3140. Industry's first 14-bit MDAC linearity 0.003% (14-bits) from 0°C to 70°C (0° to +85°C, E version; −25°C to +85°C, B version).

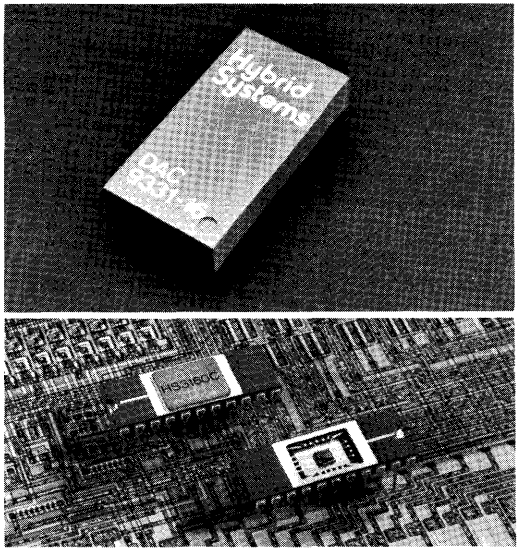
HS 3160. 16-bit monolothic MDAC, guaranteed monotonic to 0.003% (14-bits) from 0°C to +70°C (C version) and −25°C to +85°C for B version with MIL-STD-883 screening.

HS 3120. 12-bit MDAC, monolithic, double-buffered, μP compatible, super stable . . . 1ppm/°C Max.!! linearity drift, monotonic 0°C to 70°C.

HS 9338. 12-bit low cost, complete (0 to +10V, ±10V), μP compatible.

DAC9356. Low cost complete 12-bit DAC with lowest power . . . 175 mW, ±10V out DAC8O pinout.

DAC80. Industry standard low cost DAC voltage and current versions . . . no +5V required.



High resolution DAC's developed by Hybrid Systems include: DAC9331-16 (top) industry's first 0.0008% accurate Hybrid DAC and HS 3160 (bottom) 16-bit CMOS MDAC guaranteed monotonic to 14 bits (0.003%) from −25°C to +85°C.
Figure 1

DESIGN PROBLEMS

Problems and technical issues must be addressed by both the designer of the DAC and the user in applying the DAC within an application circuit. The device design problems and solutions are presented first. While it may seem to the user that the problems of the device designer are matters of little importance to the application, quite the contrary is the case. These issues are relevant in that they serve to enlighten the designer with nontrivial considerations in device selection and in great measure the selection of a vendor to supply these parts.

The most important issue in designing high resolution DAC's is the basic architecture, i.e. binary weighting versus others. The most common technique for building a D/A converter of n-bits is to use n-binary weighted switches to turn n-current or voltage sources ON or OFF, Figure 2. These switches are designed so that each switch or "bit" contributes twice as much to the D/A ouput as the preceding bit. This allows an nth-bit converter to generate $2^{(n-1)}$ output levels by turning ON the proper combination of bits.

DESCRIPTION OF KEY SPECIFICATIONS

MODEL	HS 3160
TYPE	4 Quadrant Multiplying
DIGITAL INPUTS	
Resolution	16-Bits
2-Quad. Unipolar Coding	Binary
4-Quad. Bipolar Coding	Offset Binary
Logic Compatibility	CMOS, TTL
Input Current	<1μA
REFERENCE INPUT	
Voltage Range	±25V (max), AC or DC
Input Impedance	6.5kΩ ± 50%
ANALOG OUTPUT	
Scale Factor	$150\mu A/V_{REF}$ ± 50%
Scale Factor Accuracy	±1%
Output Leakage	
@ +25°C	10nA (max)
@ +125°C	200nA (max)
Output Capacitance	
C_{out} 1, all inputs high	100 pF
C_{out} 1, all inputs low	50 pF
C_{out} 2, all inputs high	50 pF
C_{out} 2, all inputs low	100 pF
STATIC PERFORMANCE	
Integral Linearity	
HS 3160-3	±0.006% F.S.R. (typ) ±0.012% F.S.R. (max)
HS 3160-4	±0.003% F.S.R. (typ) ±0.006% F.S.R. (max)
Differential Linearity	
HS 3160-3	±0.006% F.S.R. (typ) ±0.012% F.S.R. (max)
HS 3160-4	±0.003% F.S.R. (typ) ±0.006% F.S.R. (max)
Monotonicity	
HS 3160-3	Guaranteed to 13-Bits
HS 3160-4	Guaranteed to 14-Bits
DYNAMIC PERFORMANCE	
Digital Small Signal Settling	1μS
Digital Full Scale Transition Settling	2μS
Reference Feedthrough Error (V_{REF} = 20Vpp)	
@ 1kHz	200μV
@ 10kHz	2mV
Reference Input Bandwidth	1MHz
STABILITY (Over specified temp. range)	
Scale Factor	4ppm/°C (typ)
Integral Linearity	0.5ppm F.S.R./°C (typ) 1ppm F.S.R./°C (max)
Differential Linearity	0.5ppm F.S.R./°C (typ) 1ppm F.S.R./°C (max)
Monotonicity Temp. Range	
HS 3160C-3/-4	0°C to +70°C
HS 3160B-3/-4	−25°C to +85°C
POWER SUPPLY (V_{DD})	
Nominal Voltage	+15V ±5%
Voltage Range	+8V to +18V
Current	2mA
Rejection Ratio	0.0005%/%
TEMPERATURE RANGE	
Operating HS 3160C-3/-4	0°C to +70°C
Operating HS 3160B-3/-4	−55°C to +125°C
Storage	−65°C to +150°C
SCREENING	
C-Models	0.4% AQL
B-Models	MIL-STD-883B
MECHANICAL	
Case Style	22 pin DIP, ceramic
PRICE (1-9)	
HS 3160C-3	
HS 3160C-4	
HS 3160B-3	
HS 3160B-4	

Output Capacitance
Important consideration for settling time and feedthrough.

Integral Linearity
Measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input combination.

Differential Linearity
The deviation of an output step from the theoretical value of 1 LSB for any adjacent input codes. ±0.006% Max is accuracy to 14 bits. The DAC9377-16 is guaranteed to 0.0015% (16 bits).

Stability of Linearity vs Offset
The missing specification. After the HS 3160 was characterized, it was found that this specification is $0.0325mV/mV_{OS}$. Because of this, external potentiometers can be eliminated.

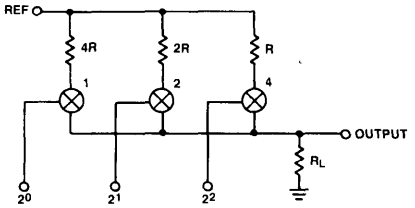
Reference Input BW
The reference can be an AC signal. The dynamics of this parameter are important in high speed signal processing.

Linearity TC
Impressive stability only obtained by the decoding techniques described.

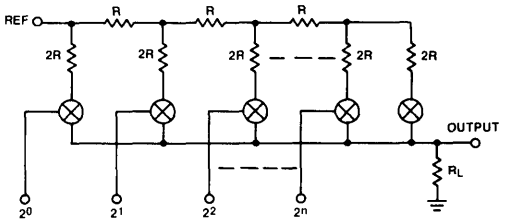
Monotonic Temperature Range
The temperature range over which the analog output increases or remains constant as the input digital code increases, but never decreases. This range of monotonicity is important in many servo or control systems.

Screening
0.4% AQL means that there will be no rejects in a sample lot of 100 pcs. All units have full burn-in at +85°C.

Price
Important key criteria in evaluating the price performance ratio.



Binary weighted current sources. Note resistor valves increase geometrically. This form taken directly becomes difficult to implement at high resolution.



R – 2R ladder network. By far the most basic approach in DAC construction.

Figure 2 Binary Weighted DAC – Circuit Configuration

Figure 3 illustrates graphically the binary bit weights. Since the most significant bit (MSB) contributes to 1/2 of the full scale output, bit 2 (MSB-1) contributes 1/4FS, bit three contributes 1/8FS etc. It follows that the worst errors occur at the major transitions of 1/2 scale, 1/4 scale etc. In bipolar modes where 1/2 scale is translated to 0, the greatest error in this case is at 0. Because of these conditions, the stability of the resistors and switch elements must be closely controlled. As an example, a 1% change in the MSB of a 10-bit converter will affect the output by 0.05% of full scale. On the other hand, a 1% change in the LSB of the same 10-bit converter affects the output by only 0.001% of full scale. To extend this discussion to 16-bits . . . and to maintain say 1/4LSB differential linearity the resistors have to be matched to 0.00015% (15 ppm) . . . and be kept to this match over time and temperature.

To overcome this basic drawback, Hybrid Systems has applied a decoding technique originally used in high speed "low glitch" DAC's. In 1979 Hybrid Systems introduced the first "low glitch" display DAC, DAC394, using a design approach that would reduce glitches. The design task at the time was to develop a DAC structure that would reduce the amount of switching currents that occur at the major transitions inherent in the R-2R approach commonly used.

Therefore, to reduce glitches (digital feedthrough) and to improve DAC performance . . . linearity and stability . . . the DAC is divided into two sections. This was the design approach used in implementing all of Hybrid Systems' high resolution DAC's. Figure 4 shows a 16-bit DAC with decoding of the top 4 MSB's.

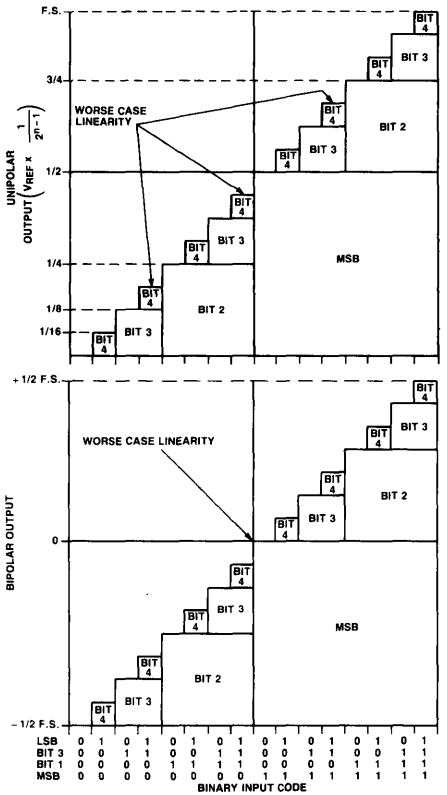
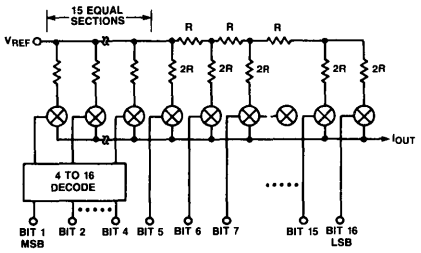


Figure 3 Binary Weighted DAC-Bit Weights



16-bit MDAC implemented by decoding top 4 MSB'S into 15 equal current sources followed by 12-bit R – 2R DAC

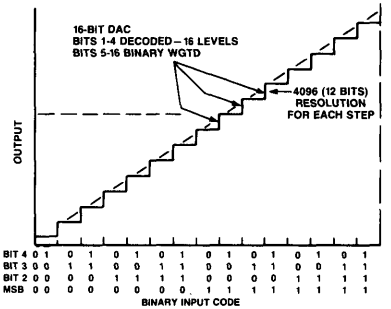


Figure 4 16-bit decoded DAC, top 4 bits decoded into 15 steps.

The lower order 12-bits which together only constitute 6.25% (4096/65536) of the total output current is implemented with a conventional R-2R current ladder. **However, instead of the upper 4-bits driving current sources with a binary weight of 1/2, 1/4, 1/8, and 1/16 the input lines are decoded into 15 logic lines which drive 15 equal current sources. Now, each of these equal sections . . . of the top 4 MSB's . . . has a weight of only 1/16th or 6.25% of the total output.** Therefore, as the incoming code on the 4 MSB's increment from 0 to 15, the equal current sources incrementally add 1/16th to the previous sum. As can be seen from the Truth Table 1, only 1 current source is switched ON for each successive major transition. Further it can be seen that all switching between any of the 16 major transitions involves either turning ON or OFF current sources . . . but never both in the same step. Using this technique greatly reduces the glitches produced by asymmetrical switching.

INPUT BINARY CODE				OUTPUT														
MSB	BIT 2	BIT 3	BIT 4	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

4 binary bits decoded into 15 LINES
TRUTH TABLE 1

In summary, by means of decoding, a high resolution DAC such as the HS 3160 can be made less sensitive to changes in individual bit switches. Further, differential linearity, and stability both over temperature and time are **8 times better** . . . (the MSB contributes 1/16 vs 1/2).

The HS 3160 is fabricated using a CMOS monolithic process in which the 4 MSB's are decoded. This requires 27 analog switches. 12 switches are used for the lower 12 bits.

By far the most important benefit of the decoding technique described here is the reduced V_{OS} sensitivity of the DAC. The segmented DAC is less prone to linearity variations due to the TC effects of V_{OS} in the output amplifier.

APPLICATION PROBLEMS

The benefits of the decoding process will become apparent to the user. DAC specifications can be analyzed relating to user benefits.

Temperature Stability

As discussed above, the decoding of the 4 MSB's (as in the HS 3160) improves parameters affecting DAC output by a factor of 8 over conventional R-2R techniques. Hybrid Systems' thin film resistor process yields resistor tracking stability in the order of 2ppm/°C typ., 6ppm/°C Max. This stability will yield (in the R-2R approach) linearity temperature coefficients of 1ppm/°C typ., 3 ppm/°C Max. However, in a decoded DAC we can divide these TC's by 8 . . . which yield linearity TC of 0.13ppm/°C, 1ppm/°C Max. In the case of the HS 3160, the specifications are conservatively rated at 0.5ppm/°C, 1ppm/°C Max. for both integral and differential linearity. Monotonicity is then guaranteed 0° to 75°C (C models) and −25°C to +85°C (B models).

Other high resolution DAC's from Hybrid Systems also feature impressive stability specifications due to the decoding process. Consider the DAC9331 (16-bit hybrid MDAC) with differential linearity TC of 0.5ppm/°C Max. Long term drift of linearity is specified at 3ppm FSR/1000 hrs. and scale factor TC is specified at 2ppm/°C FSR Max.

Output Capacitance

An undesirable specification of all CMOS DAC's is output capacitance. This is the capacitance effect of the FET bit switches and is present in all CMOS DAC's. The DAC equivalent circuit is represented in Figure 5. C_O is the output capacitance which is the distributed switch capacitance apparent at the output terminals (I_O terminals) to ground. The unwanted problems associated with this parameter are settling time and digital feedthrough; both will be discussed. However, because of the decoding technique previously described, Hybrid Systems' CMOS DAC's all exhibit industry's lowest value for this important parameter. In the decoding scheme, the binary weights are smaller (resistors are larger), so small FET switches can be used with resulting low capacitance. Basic R-2R DAC's require very large FET switches in the MSB's to reduce ON resistance thereby increasing C_O.

For example, Hybrid Systems' HS 3120 is a 12-bit CMOS DAC, the specified C_O of 25pF/50pF (shown with both conditions . . . switches OFF/ON) is the lowest capacitance C_O of any CMOS DAC available . . . in fact at least 5 times better. The specification indicates the expected values for C_O over all input codes. Hybrid Systems' HS 3140 and HS 3160 (14- and 16-bit MDAC's) have specified C_O of 50pF/100pF which is the lowest specified for this class of product.

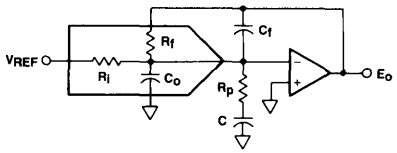


Figure 5 MDAC Equivalent Output Circuit

Settling Time

Settling time is directly affected by C_O. In Figure 5, C_O combines with R_f to add a pole to the open loop response, reducing bandwidth and causing excessive phaseshift—which could result in ringing and/or oscillation. A feedback capacitor, C_f, must be added to restore stability. Even with C_f there is still a zero-pole mismatch due to R_iC_O, which is code dependent. Mismatch is minimized when $R_iC_O = R_fC_f$. However, C_f must now be made larger to compensate for worst case R_iC_O; resulting in reduced bandwidth and increased settling time. With Hybrid Systems' 16-bit HS 3160 a small value of C_f can be used. Resistor R_p can be added; this will parallel R_i decreasing the effective resistance. If C_f is reduced, the bandwidth will be increased and settling time decreased. However, a system penalty for lowering C_f is to increase noise gain. The tradeoff is noise versus settling time. If R_p is added then a large value (1μF or greater) nonpolarized capacitor C_p should be added in series with R_p to eliminate DC drifts. If settling time is not important, eliminate R_p and C_p and adjust C_f to prevent overshoot.

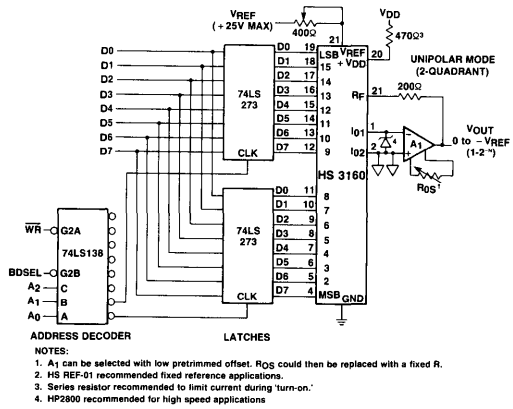
Digital Feedthrough

Digital feedthrough is never directly specified by manufacturers, however, the user can assume that this will generally be directly proportional to C_O. This parameter as applied to multiplying DAC's refers to the change in output with OV applied to the reference (analog input) and toggling the digital inputs at any worst case code. When using high resolution DAC's any feedthrough will affect system performance considering that 78μV is 1/2 LSB at 16 bits!

In the case where the DAC has on-board latches, measurements of feedthrough should be made with the reference set to full-scale and the data latched. Now toggling the input code any resultant output change is feedthrough. Feedthrough does occur even when DAC's have on-board latches. One can surmise that any feedthrough in latched DAC's is due first to capacitative coupling between CMOS cells where energy is coupled to the output in the form of spikes. Secondly, spikes can be coupled onto the output due to the capacitance of the package alone.

Hybrid Systems' HS 3120 with on-board latches has been measured for feedthrough characteristics by several users. Even though the specification for C_O is typically 4 times better (due to decoding) than equivalent devices, measurements confirm that feedthrough is an astounding 10 times better than others tested.

Most manufacturers now concede that there will be digital feedthrough even with one or two (double-buffering) layers of registers built into the device. The solution is to keep all digital input lines to the DAC as inactive as possible by use of external buffers. An example of this shown in Figure 6 where a rank of 74LS273's serve as separate latched buffers. Low power Schottky logic is recommended when external latches are used because of the uniform nature of the propogation delays between the rising and falling signal. This is not usually the case with other logic (or standard Schottky) devices. The latches should be as close to the DAC as possible and DAC input lines should be of equal length.



NOTES:
1. A_1 can be selected with low pretrimmed offset. R_{OS} could then be replaced with a fixed R.
2. HS REF-01 recommended fixed reference applications.
3. Series resistor recommended to limit current during 'turn-on.'
4. HP2800 recommended for high speed applications

Figure 6 Microprocessor Interface to HS 3160

Another suggestion to lower digital feedthrough is to clamp the MSB inputs to the DAC. As shown in Figure 7, resistors can be added to the MSB inputs to keep the logic "1" voltage as close to minimum as possible. Rather than allowing the TTL drive line to rise to +3.5 or +4.0 volts the lines can be kept at close to a minimum "1" or 2.4 volts. Pull down resistors are added from the inputs to ground. These resistors cause the driving element to source more current which lowers the DAC input voltage and source impedence. This impedance reduction will reduce noise pickup. Low power Schottky gates will source 400μA for a "1" output of +2.4 volts.

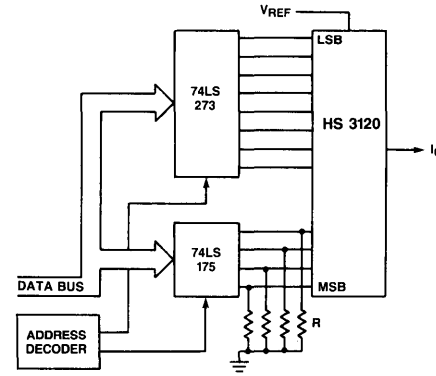


Figure 7 Clamp Resistors added to MSB Inputs

Finally, digital feedthrough can be reduced if strobe lines are optimized. In Figure 8 note that the data is strobed to the DAC on the ↓ positive going transition. In this case, the more desirable strobe to use would be Strobe B where the input pulse is not changing during the DAC transition. If Strobe B cannot be used, Strobe A should be made as narrow as possible to reduce energy presented to the capacitive feedthrough elements.

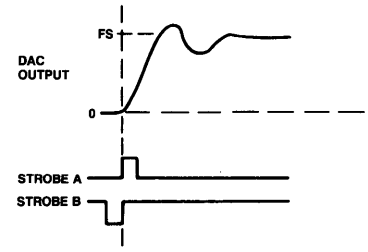


Figure 8 Strobe Input to DAC
STROBE A should be made narrow if used.
STROBE B recommended

Grounding

In addition to latched buffers, the designer must use the normal grounding and bypass techniques to further reduce unequal logic delays associated with external latches. If possible, a large ground plane and pin guarding should be used beneath and around the DAC and output amplifier, see Figure 9. With the ground as shown, the ground pin should be soldered directly to the ground plane. Further, in high speed applications, plastic or ceramic sockets should not be used.

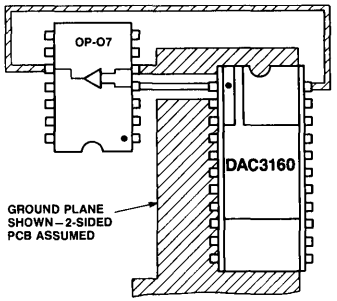
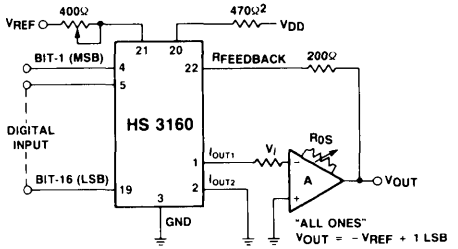


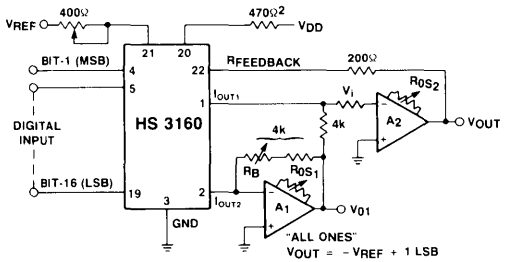
Figure 9 PCB Assembly Layout



Unipolar Transfer Characteristics

BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-N})$
100...001	$-V_{REF}(½+2^{-N})$
100...000	$-V_{REF}/2$
011...111	$-V_{REF}(½-2^{-N})$
000...001	$-V_{REF}(2^{-N})$
000...000	0

NOTES:
1. **To maintain specified HS 3160 linearity, the external amplifier (A) must be zeroed. Apply an ALL "ZEROS" digital input and adjust R_{OS} for V_{OUT} = 0 ±1mV.**
2. **Series resistor recommended to limit current during 'turn-on'.**
3. **R_{OS} may not be needed with many amplifiers.See discussion of offset.**



Bipolar Transfer Characteristics

OFFSET BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-(N-1)})$
100...001	$-V_{REF}(2^{-(N-1)})$
100...000	0
011...001	$V_{REF}(2^{-(N-1)})$
000...001	$V_{REF}(1-2^{-(N-1)})$
000...000	V_{REF}

NOTES:
1. **To maintain specified HS 3160 linearity, external amplifiers (A_1 and A_2) must be zeroed. With a digital input of 10...0 and V_{REF} set to zero:**
   a) Set R_{OS1} for V_{01} = 0
   b) Set R_{OS2} for V_{OUT} = 0
   c) Set V_{REF} to +10V and adjust R_B for V_{OUT} to be 0 Volts
2. **Series resistor recommended to limit current during 'turn-on.'**
3. **R_{OS} may not be needed with many amplifiers. See discussion of offset.**

Figure 10 Typical output connections unipolar (top), bipolar (bottom)

Ground placement associated with the output amplifier used to convert DAC output current to a voltage addressed to minimize system errors. Typical connections for unipolar and bipolar operation are shown in Figure 10. The amplifier input low (noninverting terminal) and analog ground must be connected directly at the DAC. If this is not done the effective resistance r_i (Figure 10) creates an undesired input to the amplifier resulting in loss of system accuracy. Consider the following:

r_i = Track resistance from DAC I_2 terminal to the amplifier input. Assume 100 milliohms.

I_2 = 2mA (typical full scale DAC output current)

$\therefore V_{in}+$ = Voltage apparent at amplifier input.

$= 2 \times 10^{-3} \times 100 \times 10^{-3} = 200\mu V$

At 16 bits 200 μV error results in an additional 1.31 LSB's error where 1 LSB at 16 bits is 153μV on the 10V range.

This example shows that ground returns at the output amplifier must be made with low impedance runs to reduce error created with unwanted IR voltages.

Power supplies must be properly bypassed to provide low impedance ac paths to ground. All power supplies used in the DAC system should be bypassed with at least 0.1μF (low frequency) and paralleled with 0.01μF ceramic type (high frequency). Ideally, a large ceramic capacitor should be located as close to the DAC as possible. With high resolution DAC's (above 12 bits) switching power supplies should be avoided and if possible accurate linear regulated supplies should be used.

Output Offset

In most applications, the output of the DAC is fed into an amplifier which converts the DAC's current output to voltage. A little known and not commonly discussed parameter is the linearity error associated with the offset voltage V_{OS} of the output amplifier. All CMOS DAC's must operate into a virtual ground; i.e. the summing junction of an op amp. Any amplifier offset will appear as a linearity error at the output which can be treated as LSB's of error.

Most all CMOS DAC's today are implemented using an R–2R ladder network. Consider the following analysis (see Figure 11):

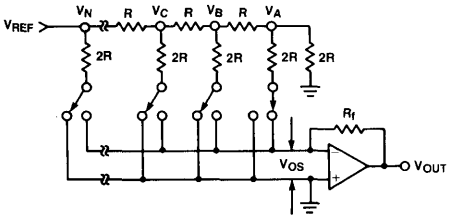


Figure 11 R–2R DAC with output amplifier

When: $V_{OS} = 0$

$V_{A..N} = V_{REF}/2^{(n-1)}$

where $V_A = V_B/2$

$V_B = V_C/2$ . . . etc.

For a 12-bit converter (R-2R type), where V_{REF} = 10V

V_A = 4.88mV, V_B = 9.77mV,

V_C = 19.5mV, etc.

However, when $V_{OS} = V_A$ then

(1) $V_{C1} = (V_{REF}/2^{n-1})\ 22/21 \approx V_C$

$$(2)\quad V_{B1} = \frac{\left(V_C\right)\left(\frac{6}{5}R\right)}{R + \frac{6}{5}R} > V_B$$

but for simplicity let $V_{B1} \approx V_B$ then

(3) $V_{A1} = V_{B1} \times 2R/(R+2R) > V_A$

(4) $V_{A1} = \frac{2}{3} V_B \equiv V_{OS}$

Where V_{A1} is the voltage at the LSB node. From (4) one can see that when the offset voltage V_{OS} is equal to V_{A1} then $I_1 = 0$. This results in a change in the linearity error of 1 LSB. In this case, it has been shown that:

(5) where $V_{OS} = 0$, an LSB goes to "1"

(6) $V_{OS} = V_{A1}$, an LSB goes to "0"

Or to put it another way; to change output linearity 1 LSB (i.e. changing 2.44mV) the corresponding V_{OS} change would have to be:

(7) $\Delta V_{OS} \rightarrow \frac{2}{3} V_B = \frac{2}{3} (9.76) = 6.5mV$

Now we have a 1 LSB change in linearity for 6.5mV change in V_{OS}. Therefore, it takes a 6.507mV change in V_{OS} to vary the output linearity 1 LSB (V_{REF} = 10V, 12-bit R – 2R type).

However, due to decoding (Figure 12), the basic R – 2R portion of the DAC yields a larger voltage at V_A and therefore the DAC is less prone to errors due to the amplifier's offset voltage.

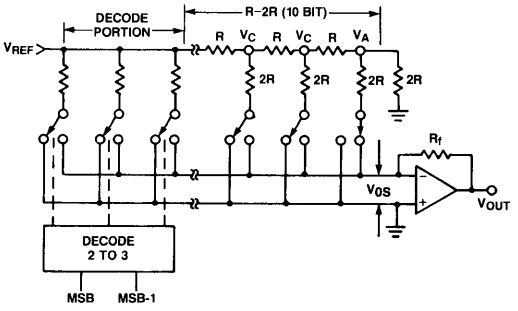


Figure 12 HS 3120 Decoded 12-bit DAC—2MSB's decoded followed by conventional 10-bit R–2R DAC

Hybrid Systems not only uses decoding (sometimes referred to as "segmenting") in the implementation of high resolution DAC's, but also binarily weights the LSB's. This is shown in Figure 13.

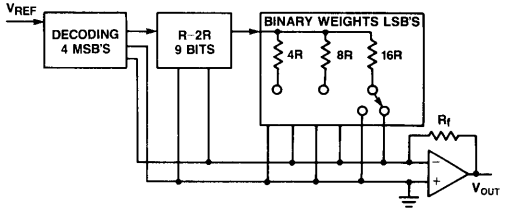
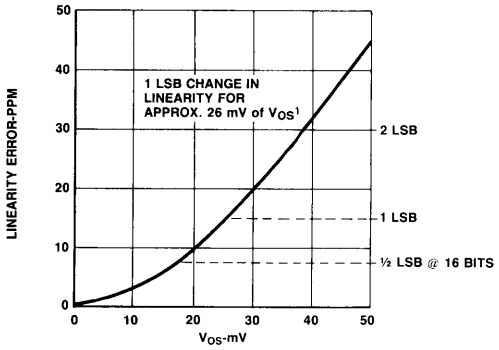


Figure 13 HS 3160 16-bit MDAC shown with implemented with decoder, R–2R, and binary weighting.

By doing this, it can be seen that a change in offset contributed by the output amplifier affects DAC linearity at a point "higher up" from the LSB switches. **This will yield a greater insensitivity to changes in V_{OS}.** Data taken on the HS 3160 (Figure 14) confirms these calculations. Table 2 compares high resolution DAC's with the method of decoding to illustrate this coefficient of sensitivity to amplifier offset.



1. Actual measurement of 26-27mV compares favorably with the calculated value of 28.5mV (Table 2).

Figure 14 HS 3160 Additional Linearity Error vs. Output- Amplifier Offset-Voltage

TABLE 2

TYPE	RESOLUTION (Bits)	DECODING	R – 2R (Bits)	BIN/ WGT	ΔV_{OS}/1 LSB ERROR
Gen. Pur.	12	N.A.	12		6.5mV
HS 3120	12	2 MSB's	10		26.0mV
Gen. Pur.	14	N.A.	14		1.63mV
HS 3140	14	4 MSB's	9	1 LSB	28.5mV
Gen. Pur.	16	N.A.	16		0.41mV
HS 3160	16	4 MSB's	9	3 LSB's	28.5mV
HS 9331-16	16	4 MSB's	12		3.56mV

From the above table one can see that for a 12-bit DAC the HS 3120 is 4 times less sensitive to V_{OS} than a standard R – 2R type. At 16 bits the HS 3160 and the DAC9331-16 are 69 and 9 times less sensitive than the standard schemes.

What this means to the user is that many types of low cost amplifiers can be used with decoded DAC's without the need to adjust offset.

Consider the following calculations, Table 3 of V_{OS}, for specific amplifers:

TABLE 3

AMPLIFIER	V_{OS} @25°C	TC	V_{OS} +25°C to +70°C
LF411	0.5mV	10μV/°C	0.95mV
LM301	7.5mV	30μV/°C	8.85mV
LM741	6mV	30μV/°C	7.35mV
HA 2525	10mV	30μV/°C	11.35
OP07	75μV*	0.25μV/°C	

*Drift specified at 1.0μV/Month Max.

Normally, CMOS DAC application notes will always show a potentiometer used to null out the amplifier's offset. *Note: always use the offset terminal to insert a nulling voltage—never inject a correction current into the summing junction.* The designer can readily see that with Hybrid Systems' high resolution DAC's the potentiometer can be eliminated saving PCB space and lowering system cost.

Finally, while this discussion has dealt with the issues of change in linearity with respect to ΔV_{OS} it should be pointed out that this should in no way be confused with initial accuracy which will still be present . . . but in many applications can be calibrated out.

Output Amplifier—Finite Gain Effects

The ideal model of an operational amplifier assumes infinite open-loop gain. This implies zero differential input voltage at all output levels. In reality, operational amplifiers exhibit open-loop gains ranging from 80 to 100dB (10^4 to 10^5 V/V). This results in finite measureable input voltage differentials. For example, in a typical DAC system with a full-scale output of 10 volts an amplifier having an open-loop gain of 100dB (10^5 V/V), the amplifier differential input voltage would be 100μV with respect to ground. This additional "error" voltage appearing at the input terminals can be treated as an additional offset and would effect linearity according to Table 2 above.

One can see that there are errors produced by "finite" amplifier gain. This can produce significant errors in high resolution 14- to 16-bit DAC's which might be justifiably ignored at the 12-bit level.

To maintain system accuracy when using high resolution DAC's, we recommend output amplifiers such as the OP07 or LF411 type which possess large, stable open-loop gain and reasonably low (but stable) offset voltages. For less demanding applications, the 741 or 301 type amplifier can be used provided the resultant errors are within acceptable limits and where cost is a consideration.

Reference Voltage Level

Performance of high resolution DAC's are optimized for a 10 volt reference level. However, it should be noted that as the magnitude of the reference is lowered, offset voltages, leakage currents and other higher order parasitics represent an increasing contribution to linearity and gain error. Typical linearity error versus reference voltage are shown in Figure 15.

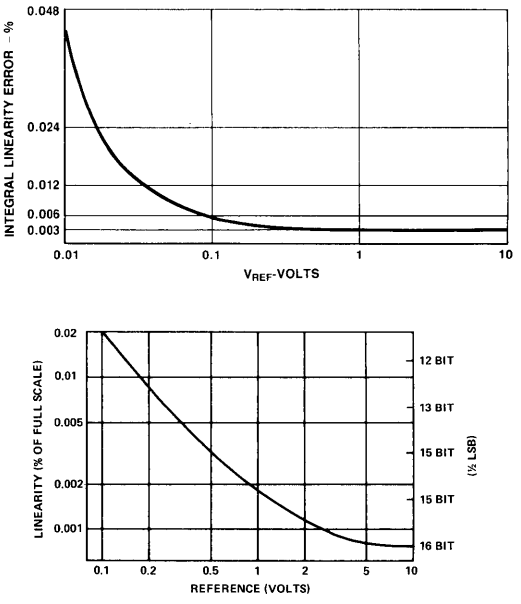


Figure 15 Linearity VS Reference Voltage, HS 3160 (top), DAC9331-16 (bottom)

LOW COST HIGH RESOLUTION DAC SYSTEMS

Discussion previously has focused on understanding high resolution DAC's from the combined perspectives of the DAC designers and the design engineer applying the DAC. The following application discussion will focus on component selection.

12-Bit DAC System

By using Hybrid Systems' HS 3120 and HS REF01 along with National's LF441A, a low power economical 12-bit DAC system can be realized.

HS REF01

This reference element is by now an industry standard. It is multisourced and available in four temperature grades—3, 10, 20, and 70ppm/°C. The 20ppm/°C plastic grade is generally available for $2.00 (100's)—even the 3ppm grade in a TO-99 is only $7.60 (100's approx.). The HS REF01 draws only 1mA quiescent current and can deliver at least 10mA to a load. Therefore, one HS REF01 can power several DAC's allowing the fullscale tempco of the entire system to be referenced to one source.

HS 3120

This popular 12-bit DAC has many design features that make it an ideal choice in this 12-bit system. The HS 3120 is a monolithic 12-bit MDAC with double buffered input registers sectioned into 3 segments (nibbles) of 4 bits each. Each section is individually addressable for easy interface with 4-, 8-, or 16-bit data busses. The control logic allows the designer to use the DAC in a "memory map" mode. The decoding discussed above results in very impressive differential and integral linearity guaranteed at 1ppm/°C maximum. Monotonicity is guaranteed 0°C to +70°C along with scale factor TC of 2ppm/°C max. Due to decoding, feedthrough is low and the effects of V_{OS} are also lower than conventional 12-bit DAC's.

LF441A/LF411A

Now, two low cost JFET input op amps are available from National Semiconductor The LF441A has low power consumption (supply current 150 μA), low noise, and low offset voltage (0.5 mV, Max). It has the same bandwidth, gain, slew rate, and pin out of a 741 at 1/10 the power. The LF411A has 3 MHz gain BW (Min), low noise, and low offset voltage (0.5 mV, Max).

These op amps are trimmed to reduce input offset voltage to 0.3 mV typical, 0.5 mV Max. Because of the decoding of the HS 3120 (Table 2), it takes 26mV of offset (V_{OS}) to yield a linearity error of 1 LSB, so pots are not necessary to keep within 12-bit linearity even over temperature. The temperature coefficient of input offset voltage is 7 μV/°C typical, 10° μV/°C Max.

For example:

Max. V_{OS}, 0°C to 70°C: 0.5mV + (10)(70μV) = 1.2mV

Typical V_{OS}, 0°C to 70°C: 0.3mV + (7)(70μV) = 0.82mV

Additional linearity error, due to V_{OS} and dV_{OS} (0/70°C)

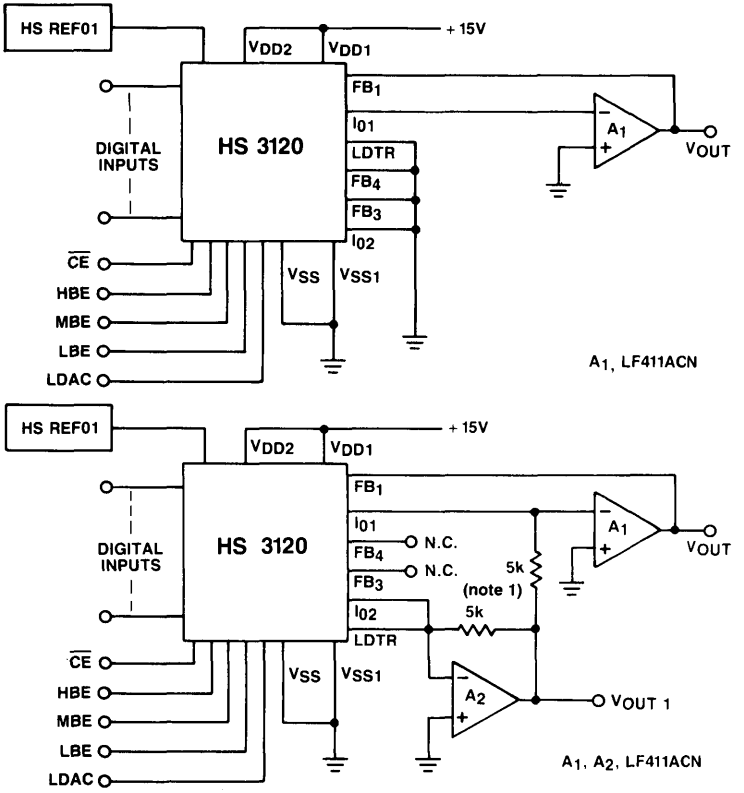
Maximum: 1.2 x 1/26 = 0.046 LSB's

Typical: 0.82 x 1/26 = 0.032 LSB's

Now include the specified 1ppm/°C differential linearity drift (700μV over 0°C to 70°C) and the system yields a total drift of linearity 0°C to 70°C of less than 1/3 LSB.

The HS 3120 with the LF441/LF411 requires no external trim pots which save PCB space and material cost. This system will provide monotonicity over a large temperature range.

The 12-bit DAC system implemented using these parts is shown in Figure 16. The cost in 100's for the unipolar system is $20.15 while the bipolar version is $24.05.



NOTE:
1. External resistors should be selected for good bipolar offset tempco and need only track well. Absolute TC or tolerance is not important. The internal 5K resistors can be used if 10ppm/°C drift is tolerable.

COST (POWER BUDGET)

UNIPOLAR: 0 to −10V CODING: SB, CSB				BIPOLAR: −10V to +10V CODING: OB, COB			
PART	Current Drain TYP	MAX	COST/100's	PART	Current Drain TYPE	MAX	COST/100's
HS REF01C	+1.0	+1.4	$ 2.00	LF441ACN	+ .15	+ .2	$ 2.40
LF441ACN	+ .15	+ .2	2.40		− .15	− .2	
	− .15	− .2		5K Resistors W.W.			1.50
HS 3120	+1.0	+2.5	15.75	Load Current, A2	+1.25	+2.0	
				Unipolar Parts	+2.15	+4.1	
					− .15	− .2	20.15
Total	+2.15	+4.1	$20.15	Total	+3.55	+6.3	$24.05
	− .15	− .2			−0.3	−0.4	

Figure 16 Low Cost 12-Bit DAC System

High Speed System

Fast settling times can be realized using the circuit in Figure 5. Three op amps are reviewed. The HA2525 is the fastest with 120V/μS slew rate and a gain BW of 20MHz. However, in low gain configuration, additional compensation is needed. So while this device is the fastest, system performance is limited by compensation required for G<3. The disadvantage is no short circuit protection and up to 10mV$_{OS}$ at 25°C. The LF357 is next best but requires trim pots. The LF411ACN is the least fast but requires no trim pots. Settling time and component values are shown in Table 4.

TABLE 4

OP AMP	R_i	C_{BW}	C_f	SETTLING TIME to 0.1%
HA2525	1K	5pF		1.8μsec.
LF357	1K		20pF	2.0μsec.
LF411ACN	1K			2.5μsec.

Note:
1. HA2525 uses a 'BW' capacitor on pin 8, therefore, no C_f is required. The LF411ACN has internal compensation and appears to operate well without the addition of C_f.
2. R_i and C_f are designations from Figure 5.

14-Bit DAC System

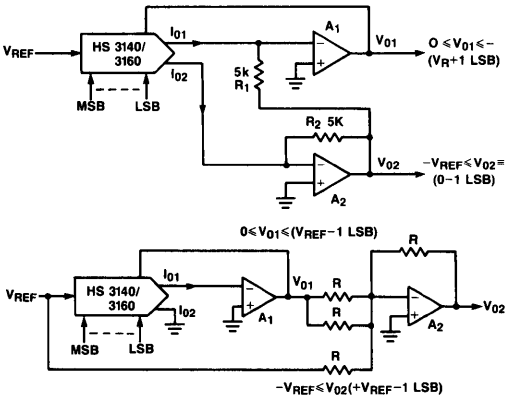
The 12-bit DAC system described above can be upgraded to 14 bits by using Hybrid Systems' HS 3140. The HS 3140 is a single chip DAC implemented using decoding and binary weighting. The improved DAC performance has been discussed above. Monotonicity is guaranteed from −25°C to +85°C and the specified stability of 1ppm/°C Max. is not matched by competitive devices. The diagram in Figure 10 can be used along with external input latches shown in Figure 6.

16-BIT DAC System

Once again, upgrading from 12 or 14 bits to 16 bits can be accomplished by using either the HS 3160 or HS 9331-16 Both DAC's use decoding for the MSB's along with an R−2R ladder, and binary weighting for the LSB's. This makes it possible to use the amplifiers previously discussed.

Bipolar Operation

Most application notes including this one show bipolar operation as indicated in Figure 17A. As noted earlier, R_1 and R_2 must and A_1 and A_2 must have low offset to eliminate the offset adjustment. If A_1 and A_2 are LF411A type, the system would have to deal with V_{OS} of 0.5mV Max. Using the LF412A then V_{OS} would be ±1mV. The user should realize that in bipolar operation all additional linearity errors double.



Top: Standard Bipolar arrangement
Bottom: Bipolar arrangement with A_2 scaled by V_{REF}

Figure 17 Bipolar operation

Considering an alternate configuration, Figure 17B, it can be seen that the errors need not be doubled as in Figure 17A. This is because I_{02} is not used. Linearity is only effected by A_1. Note in Figure 17 B, the R's must track for good V_{OS} and full-scale characteristics. A recommended resistor network is Hybrid Systems' HS R4100-5001-03 which has an absolute tolerance of ±1%, ratio match ±0.5%, and tracking TC of 2ppm/°C. In this configuration, only A_1 must be selected for low V_{OS} while A_2 can a more common type say LF412CN (99¢/100's) and is a dual op amp. For a multiple DAC system A_2 can be LF444CN which is a quad op amp.

PRECAUTIONS WHEN USING CMOS DAC'S

Most CMOS DAC's now on the market are the most well-protected CMOS devices ever produced. However, still observe the following precautions:

1. Do not allow digital inputs to float. Digital inputs that are routed off the PC card should have at least 1MΩ resistors pull-ups or pull-downs (or termination networks) to prevent accumulation of static charges when PC boards are disconnected from the system. CMOS DAC's should not be interfaced to TRI-state busses, even buffered (latched) DAC's, without pull-ups/downs, and/or terminations.
2. No CMOS DAC input/or output should go more than .5V negative. I_O terminals should be schottky-clamped to ground to prevent high-speed op amps from slewing negative on power up or certain input changes.
3. When V_{DD} is lost while the digital inputs are driven with "1"'s an SCR-like effect can occur with the input switches upon reapplication of V_{DD}. Add a 500Ω to 1 KΩ resistor in series with the V_{DD} line to current limit if this should occur.
4. In particularly noisy systems, where the possibility exists that the digital inputs can go below −.6V (due to the GND pin on the digital drivers spiking negative), it is a good idea to buffer the digital inputs with series resistors, say around 100KΩ. Input currents are in the nano amp range so large resistors are ok, and logic compatibility is maintained.
5. Use standard CMOS handling precautions.

ANALOG PROCESSING FOR DATA ACQUISITION

With the advent of low-cost, highly-accurate digital computation and control systems, more emphasis is being put on convenient ways to process analog information to the digital section. For those who are not familiar with analog signal processing, there is often more to it than meets the eye. Component idiosyncracies often become apparent when operating in the often imperfect analog world. When building the data acquisition function, potential problem areas include grounding, noise, layout, individual component errors and component interaction effects. Optimal system performance can only be obtained when the designer has carefully understood and minimized all possible error sources.

In an effort to make this task easier, Hybrid Systems now offers standard data acquisition components in cost-effective hybrid format. Incorporating such functions as multiplexing, sample-and-hold circuitry and analog-to-digital conversion into one or two dual in-line packages, many potential problem areas have been minimized.

Let's examine the Data Acquisition System and identify areas which may cause problems. Figure 1 shows a typical multichannel data acquisition system. It consists of an analog mutiplexer to select the desired analog input, an instrumentation amplifier (if required) to amplify the input signal and remove any unwanted common-mode signal, a sample-and-hold amplifier to "freeze" the input signal, and an analog-to-digital converter (A/D) to convert the sampled analog voltage into digital data.

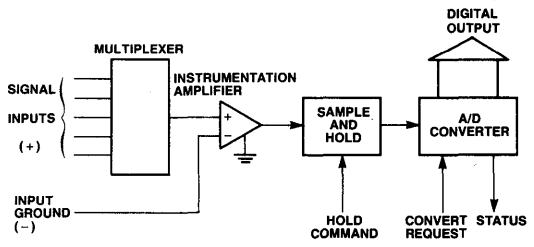


Figure 1. Typical Data Acquisition System

Multiplexing

The multiplexer is a cost-effective way to time share an A/D, as opposed to using one A/D per channel to be digitized. Multiplexers generally come in 4, 8 and 16 input configurations. Proper attention to multiplexer error sources can yield excellent performance, making the multiplexer a logical choice for DAS applications.

When considering a multiplexer, one needs to look at the internal timing which controls the switching from one channel to the next. Many multiplexers are designed to "break before make." This allows for delay between disconnection from the previous channel and connection to the next channel. Thus, assuring no input channels are ever momentarily short together, thereby causing an invalid output.

Many designers attempt to use an RC filter on each multiplexer input as an attempt at reducing grounding and noise problems. A typical set of values might be R_{in} = 100KΩ and C_{in} = 0.01μF. The problem here is that when the multiplexer is switched to a new channel, C_{out} charges by acquiring some of the charge in C_{in}, thus reducing its voltage by about 1% (see Figure 2).

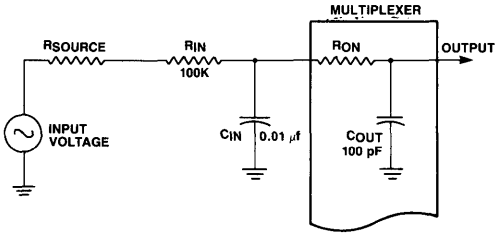


Figure 2. Input Decoupling Yields Poor Settling

While the voltage at C_{in} is within 1% of where it should be, this is the equivalent of up to 40 LSBs on a 12-bit system. Final system settling involves charging C_{in} and C_{out} through R_{in}, and this RC product is on the order of 1 millisecond. In summation, worst case analysis requires several milliseconds of settling time after multiplexer channel changes with this topology and the component values chosen.

If local RC decoupling is required at the multiplexer inputs, a better solution is to individually buffer each input at the multiplexer as shown in Figure 3. This method allows the use of very low frequency pole RC filters and yet presents a low source impedance to the multiplexer inputs for fast settling after input channel changes.

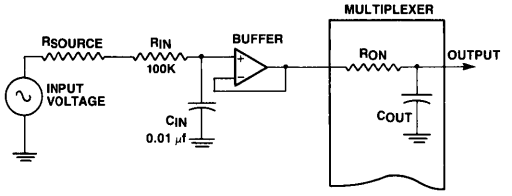


Figure 3. Op Amp Buffer on each Multiplexer Input Yields Improved Settling when RC Filter is Necessary

Another important consideration is the series resistance of the multiplexer (see Figure 4). Most analog multiplexers utilize a CMOS switch which exhibits an on resistance which may vary from 50 ohms to 2K ohms. When current flows through the multiplexer, a voltage difference will be created between the signal input and multiplexer output. In this case, a high input-impedance amplifier can be used to buffer the multiplexer outputs. I_{mux}, the current flowing through the R_{on} will be the summation of multiplexer leakage current and amplifier bias current. The offset voltage between the input signal source and multiplexer output is the product I_{mux} and R_{on} and R_{source}. A significant source of error at elevated temperature can be attributed to the multiplexer leakage current which doubles with every 10°C increase in ambient temperature. "BI-FET" type op amps should also be carefully looked at as input bias current, while quite low at room temperature, can become quite significant at elevated temperature.

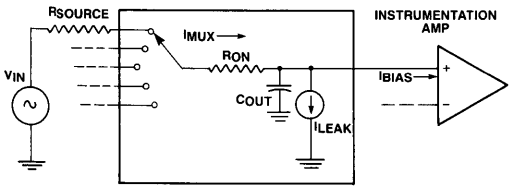


Figure 4. Simplified Multiplexer Model

Gain

Some data acquisition applications may require an instrumentation amplifier for further signal processing after multiplexing. The amplifier maintains a high impedance at both of its differential inputs, removes common-mode voltage, and amplifies the signal to match the voltage range of the A/D.

Gain setting can generally be set by either internal resistor networks or by externally applied resistors. Gain errors are often sources of inaccuracy in DC amplifiers, and are mostly due to mismatch in the individual resistor networks or external resistors when used. The highest accuracy and stability are obtained when all resistors reside in a common network.

For precision applications, Hybrid Systems offers a wide range of thin film resistor networks both in package and chip form. Utilizing advanced processing techniques, ratio tolerances can be held as low as 0.02% with resistor-to-resistor tracking of 2.5ppm/°C.

While one can speak of simple "offset error" equal to output voltage when V_{in} = 0V, it is usually more instructive to view the offset as a summation of input-referred and output-referred terms. The difference between these is that an input-referred offset, like the input signal, appears to be proportional to amplifier gain while output-referred offset appears as a constant added to the amplifier output signal. Therefore, input-referred offset typically become a problem when operating at higher gains. In addition, manufacturers may also specify voltage drift (μV/°C) as a combination of input- and output-related terms. A hypothetical example might be as follows:

V_{offs} = 2mV + (50V x GAIN)

V_{drift} = 30V/°C + (10V/°C x GAIN)

This amplifier has an input-referred offset of 50V, an input-referred drift of 10V/°C, an output-referred offset of 2mV, and an output-referred drift of 30V/°C.

Common-mode rejection ratio is also an important parameter of the instrumentation amplifier. An ideal differential input would respond only to the voltage that is common to both inputs. Although most manufacturers specify CMRR, the designer should consider two points.

1. CMRR is a function of frequency. Higher frequencies decrease the ability of the amplifier to reject common-mode signals.

2. The CMRR of the instrumentation amplifier may be effected by the circuitry around it. A "pseudo differential" setup in which all inputs share a common remote signal ground, can reject general differences between input signal ground and measurement system ground (Figure 5). It does not, however, possess individual differential input signal pairs. This can cause low CMRR particularly at high frequencies. This is because the sum of the source resistance, multiplexer channel resistance, and multiplexer output capacitance form an RC pole. This attenuates any common-mode signal on the + input. A truly differential approach (Figure 6), contains an RC pole in each input lead, preserving the common-mode balance. This does assume that the + input and – input source resistors are kept balanced.

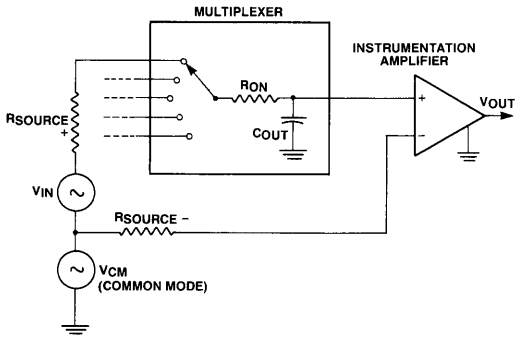


Figure 5. Pseudo-Differential Connection Degrades Common Mode Rejection

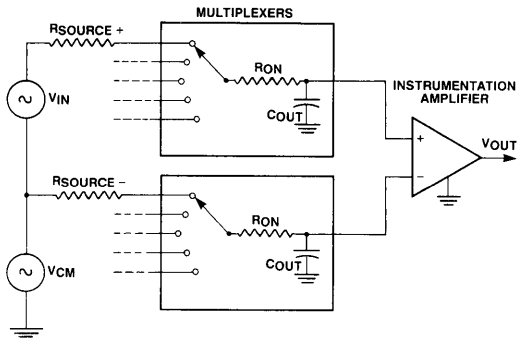


Figure 6. Balanced Differential Approach Preserves Common Mode Balance

Hybrid Systems' superior thin film technology guarantees exceptional stability of CMRR over wide ranges of both time and temperature.

A final consideration in the instrumentation amplifier area is settling time. Before the multiplexer switches to a new output signal, it is important the amplifier be allowed to settle acceptably close to it's final value. Settling time is gain dependent, generally increasing at higher gain ranges.

Sample-and-Holds

The sample-and-hold section of a data acquisition system can often be the most troublesome to utilize properly. Functionally, the sample-and-hold captures the input signal voltage, stores it on a high quality capacitor, and presents the A/D a stable voltage level during conversion. As simple as it appears, there are many subtle factors which can degrade the sample-and-hold performance. Errors can occur within the circuit itself, be caused by external interactions, or can be due to a combination of both.

To better understand potentials error sources, let's examine the sample-and-hold. A simplified circuit can be seen in Figures 7a and 7b. A high input impedance buffer amplifier is recommended for the input so the source is not loaded. It's output must be capable of driving enough current to charge the hold capacitor rapidly. A FET switch is usually utilized and controlled by a switch driver or level translator circuit interfaced with TTL inputs. Most hybrid sample-and-hold's use MOS type hold capacitors due to low leakage and low dielectric absorption. If an external hold cap is required, polystyrene, polypropylene, or teflon are recommended. A FET input amplifier with very low input bias current should be used to buffer the voltage of the hold capacitor.

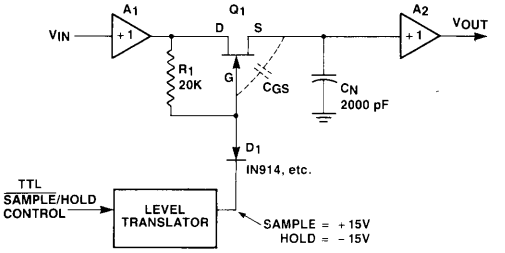


Figure 7a. Simplified Sample-and-Hold Circuit

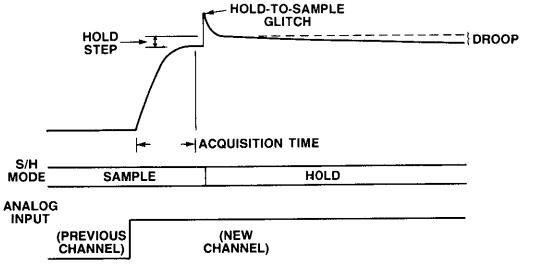


Figure 7b. Typical Sample-and-Hold Output Behavior

The first task for the sample-and-hold is the acquisition of the new input signal. The circuit is placed in the sample mode, and the new input voltage is made available. After a certain period of time allowed for amplifier slewing and settling, the output voltage will be sufficiently close to the input signal. This is known as acquisition time.

Be careful when considering acquisition time required. Many manufacturers only specify "typical" acquisition times for a 10V step. A bipolar 10V application could see a 20V swing at the input, causing a longer acquisition time. Acquisition time can also be a function of hold capacitor size. The larger the hold cap, the longer the acquisition time.

Sample-and-Holds (cont.)

After acquiring the input signal, the circuit is switched to the "hold" mode. The level translator develops a signal of −15V in the hold mode and +15V in the sample mode. When the circuit switches from the sample-to-hold mode, the voltage on the gate of the FET switch goes from V_{in} to −15V. The switch ceases conduction and freezes the input signal voltage on the hold capacitor. Observing the buffered capacitor voltage at V_{out} before and after transition to hold mode, reveals the capacitor voltage has shifted negative by approximately 20mV. This is due to a junction capacitance that exists between gate and source of the FET switch. This couples the negative going gate drive signal into the hold capacitor. This phenomenon is known as "hold step." Unfortunately, the hold step observed at the output is not constant, but is a function of analog input voltage. Figure 8 shows a graph of hold step versus analog input voltage in our simplified circuit.

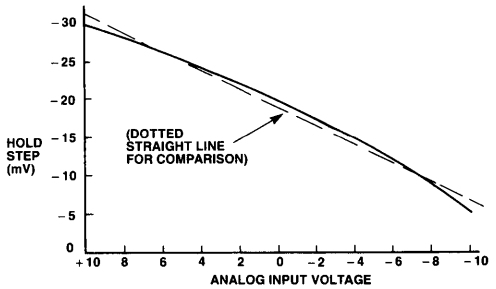
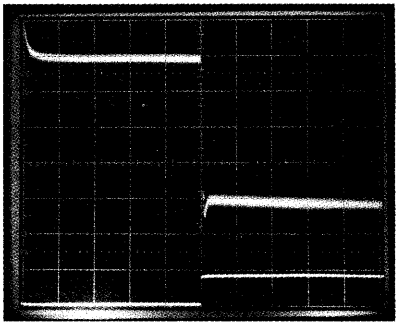


Figure 8. Hold Step vs. Input Voltage for Simplified Sample-and-Hold

Hybrid Systems has been able to overcome this problem with the HS 362K. By designing a proprietary sample-and-hold circuit, the hold step is small and well-controlled with respect to input voltage. An example of step size vs input voltage for the HS 362K and typical sample-and-hold circuits is shown in Figures 9-11.

V_{IN} = 0V
TOP = ANALOG OUT 2 mV/DIV, AC COUPLED
BOTTOM = SAMPLE/HOLD IN 5V/DIV
HORIZ. = 10 μsec/DIV

TYPICAL SAMPLE-AND-HOLD CIRCUIT



HYBRID SYSTEMS HS 362

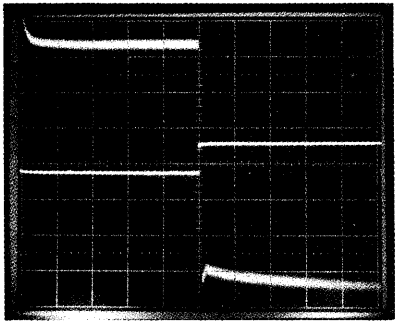
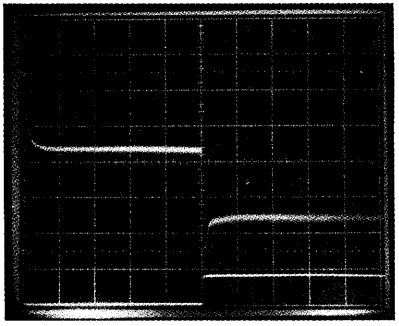


Figure 9. Sample Hold Step Size Performance

V_{IN} = +10V
TOP = ANALOG OUT 2 mV/DIV, AC COUPLED
BOTTOM = SAMPLE/HOLD IN 5V/DIV
HORIZ. = 10 μsec/DIV

TYPICAL SAMPLE-AND-HOLD CIRCUIT



HYBRID SYSTEMS HS 362

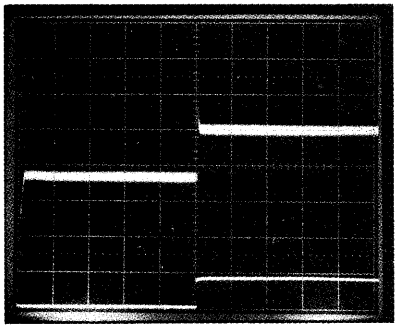


Figure 10. Typical Sample-and-Hold Circuit

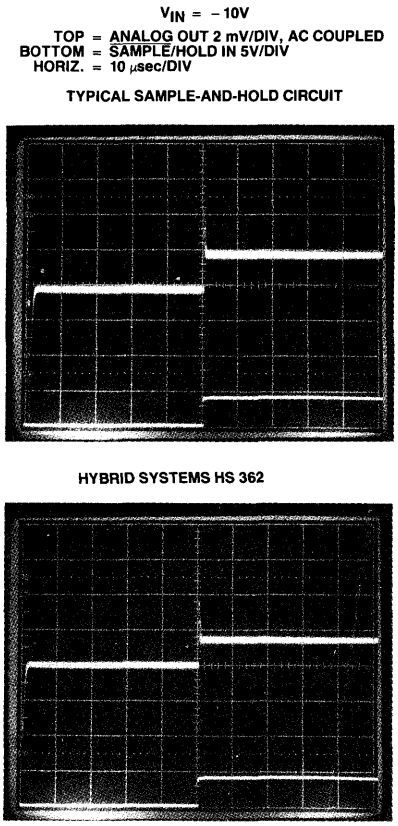


Figure 11. Typical Sample-and-Hold Circuit

Stray capacitance can also be a source of sample-and-hold error. It is possible to pick up unwanted signal from the input buffer amplifier through the circuit capacitance between source and drain of the FET switch. Coupling while in the hold mode is known as "feedthru." A worst case condition for feedthru occurs when an input signal near −full scale is sampled and the DAS input multiplexer then switches to a new signal at +full scale (or vice versa). To minimize feedthru errors, it's best not to switch input channels while the sample-and-hold is in the hold mode. Figure 13 gives examples of proper timing relationships.

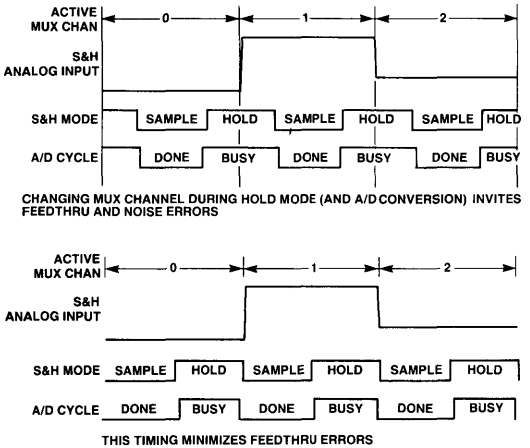


Figure 13. Changing Mux Channel During Hold Mode (and A/D Conversion) Invites Feedthru and Noise Errors

An additional potential problem area can be the sample-to-hold glitch. When the circuit is switched from the sample-to-hold mode, a glitch will appear on the output. It is important this glitch is allowed to settle out before the A/D conversion takes place. This can be especially troublesome in a system where the A/D EOC (end of conversion) status signal directly controls the mode of the sample-and-hold. The glitch must settle between the time the A/D starts conversion and the time it makes its first MSB decision. If this is a problem, the user can either use a separate logic signal-to-switch-to-hold mode sufficiently before initiation of the A/D conversion, or utilize a sample-and-hold with a fast settling glitch. Figure 12 shows an example of glitch performance of a typical sample-and-hold circuit vs the HS 362.

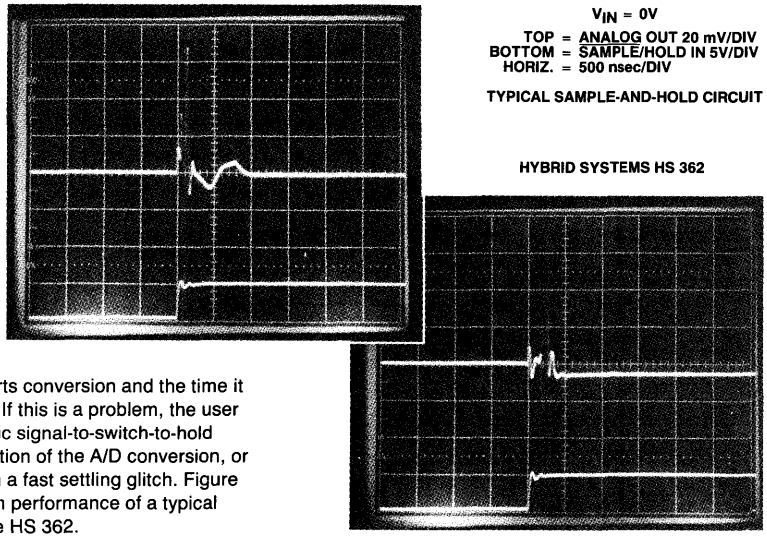


Figure 12. Sample-and-Hold Glitch

Analog-to-Digital Conversion

Now that the front-end system has been examined, the incorporation of the A/D will make the DAS complete. Here again, there are potential error sources both within the A/D itself, and from interaction with the other system components. Offset and gain errors in the A/D have the same effect as offset and gain errors elsewhere in the front end. The sum of the system errors may be "tweeked" out at a single point, but care must be taken to allow for enough adjustment range. Applications information may contain trim circuits which only have enough range to accommodate errors in the A/D alone.

The designer should carefully select an A/D converter which meets requirements for linearity error. This specification governs accuracy of the device and is not user adjustable. Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full-scale," with offset and gain adjusted to zero.

There is also a class of problems related to dynamic interactions between the A/D and its surrounding circuitry. Although the analog input node appears like a simple resistive load on the manufacturer's data sheet, the behavior of the actual physical circuit is often more complex. This is because, during the A/D cycle, various current sources (bits) are being switched in and out of the internal summing node to which the opposite side of this resistor is connected. These sudden voltage shifts couple through the A/D input resistor and upset the amplifier output of the previous stage. If the amplifier does not recover by the time the A/D makes its next bit decision, the conversion result will be erroneous (see Figure 14). A simple way to avoid this type of problem, is to be certain that the amplifier driving the A/D input has both sufficiently high bandwidth and low output impedance. The glitches induced at its output must settle out in less than the time between successive bit decisions ($\frac{T_{conv}}{\#\text{ of bits}}$). As a concrete example, an LM741 op amp is a poor choice to drive the analog input of an ADC85 A/D converter. The HS ADC85 is an industry standard 12-bit, 10 microsecond converter and allows about 830 nanoseconds ($\frac{10\mu sec}{12\text{-bits}}$) between successive bit decisions.

The speed of the LM741 is such that, if upset, its output will take perhaps 1 or 2 microseconds to return to normal, but this is obviously too long. A better choice for a buffer op amp is the LM310 which settles sufficiently after only a few hundered nanoseconds. For this reason, most ADC85's contain an internal uncommitted LM310 buffer amplifier which is intended to be used to drive the analog input node.

Similar dynamic problems can also occur at the A/D voltage reference input. Some converters exhibit dynamic load changes at this node, and the user must be certain that the integrity of the reference is maintained. A low output impedance, fast-settling buffer amplifier may also be required here.

A final point to consider for proper A/D operation is that of grounding. Figure 15 shows the most desirable method of grounding. Note the system uses separate analog and digital grounds and these are connected at only one point, near the A/D. In addition, the grounds for the sample-and-hold and instrumentation amplifier are also located close to the A/D ground.

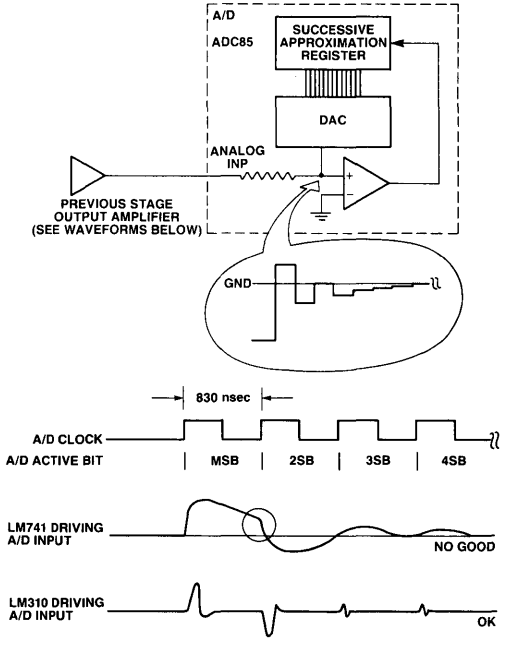


Figure 14. Dynamic Voltage Shifts can Couple Back Thru Input Resistor and Upset Amplifier Output of Previous Stage. The Amplifier Driving the Analog Input must Settle Back between Succesive Bit Cycles.

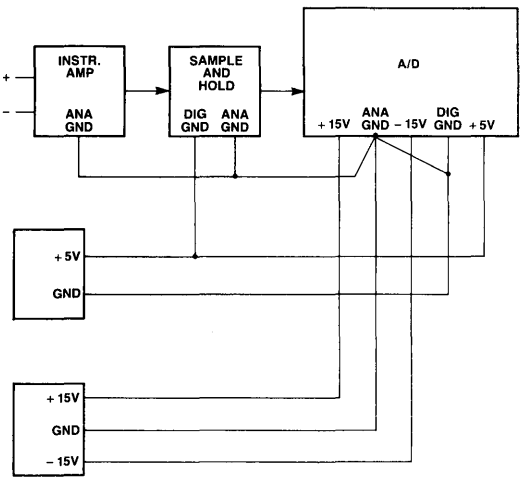


Figure 15. Proper Grounding Technique

SP1000 ANALOG ARRAY PRODUCTS

	TRANSISTOR COUNT	BOND PADS	TILES	VOLTAGE V_{CEO}	F_T NPN	F_T PNP	RESISTOR MATERIAL	MAX Ω	MAX CAP	FEATURES	PAGE
SP1104	444	24	16	20V 35V	1.0 GHz	0.6 GHz	NiCr	800K Ω	134 pF	100 mA TRANSISTORS	37
SP1204	448	40	16	20V 35V	1.0 GHz	0.6 GHz	NiCr	800K Ω	135 pF	P-JFETs	41
SP2107	780	54	20	20V 35V	1.0 GHz	0.6 GHz	NiCr	1200K Ω	336 pF	100 mA TRANSISTORS	45

Shaded area indicates new product since publication of 1988 Catalog

	Page
SP1000 General Description	35
SP1000 Component Descriptions	49
SP1000 Macro Cells	55

GENERAL DESCRIPTION

GENERAL DESCRIPTION

The SP1000 family is a high density, high performance semi-custom family of array products suitable for the implementation of analog ASIC functions. Using the pre-diffused transistors on the array, a variety of analog components such as op amps, comparators, references, and current buffers can be integrated into a system on a monolithic IC. This allows the user to save space, weight, and power while improving the performance and reliability of the circuit and reducing the unit cost.

The SP1000 family of products are personalized for each user's specific application by defining the thin film resistor layer, the two aluminum interconnect layers and the via layer which interconnects the two levels of aluminum.

While arrays in the SP1000 family vary in size and component count to allow the user to define a circuit which is best suited to his specific application, the core tile layout is consistent within the family. This allows functional macro cells to be developed and repeated within a circuit, or transported to another base array. Users may access the Sipex library of cells or develop their own using the individual components and SPICE models provided. The availability of a large number of tiles on each array permits the integration of many complete analog functions on a single monolithic ASIC.

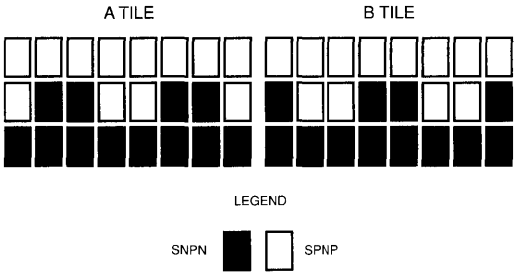
Using the support tools offered by Sipex, a user can take full control of the circuit design from concept through layout. Kit parts of the components and macrocells in the Sipex library are available for evaluation and breadboard analysis. The Sipex DESMAN 1100 design manual offers a complete tutorial on design, simulation, and layout of an SP1000 array product using commonly available design systems. SPICE models are provided with the DESMAN 1100. Mylar layout worksheets and GDS II database tapes are available to support the layout. Sipex also offers training sessions and conducts design consultations prior to creating masks from the layout.

Integration, which is performed by Sipex, consists of design rule and layout versus schematic continuity checks, mask manufacture, and fabrication of first silicon. Functional circuits, packaged and tested at room temperature are delivered to the customer to evaluate the design. An acceptable design can be rapidly moved into production with the addition of production probe and test programs.

ARRAY STRUCTURE

Each pre-diffused analog array contains linear bipolar transistors as well as numerous other components commonly used to implement high performance analog functions. The SP1000 family of arrays is configured around a tile architecture where each tile contains 24 1x geometry transistors.

TILES



High Gain, high bandwidth complimentary vertical NPN & PNP transistors coupled with precision thin film resistors and capacitors make the SP1000 family ideally suited for implementing cost effective ASIC solutions to high speed and high precision analog signal conditioning and signal processing applications.

The SP1000 family is fabricated with Sipex's Dielectric Isolation (DI) process. DI eliminates most of the parasitics which commonly plague IC designs. Consequently, translation of discrete breadboard designs into a working monolithic silicon chip is greatly simplified.

TECHNOLOGY

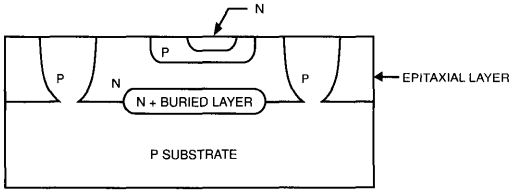
The SP1000 Analog Array family is fabricated using Sipex's dielectrically isolated (DI) complementary vertical NPN/PNP bipolar process. Enhanced precision is achieved through the utilization of on-chip low temperature coefficient thin film resistors. Stable buried zener diodes, pinch resistors and MOS capacitor structures are also available on each chip. In addition, some arrays have high current transistors, P-JFETs, or other components.

The DI technology used on the SP1000 family is a key product feature which offers users both ease of design and high performance. DI serves to eliminate the four layer parasitic device structures which most often plague analog array designers and users. DI technology also allows the easy

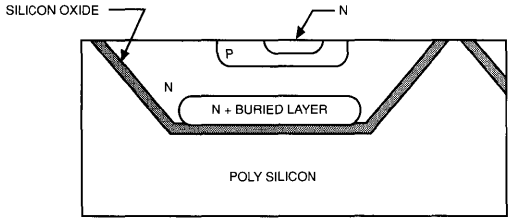
inclusion of high performance (i.e. high β f_T, Ic, etc....), full function complementary vertical NPN & PNP transistors on the array. The availability of both these transistor types on the SP1000 family not only simplifies designs, but also leads to significantly enhanced performance.

All monolithic integrated circuits are made up of individual circuit elements (i.e. transistors, resistors, diodes, etc.) fabricated in a common silicon substrate. Since this substrate can support current flow, it is necessary to electrically isolate each individual circuit element from the substrate.

Conventional semiconductor processes create the required electrical isolation by utilizing a reverse biased P-N junction placed electrically between the individual circuit element and the common substrate. Physically, this is realized by fabricating the circuit element within an N-type island that has been diffused into the P-type substrate. This type of electrical isolation is referred to as Junction Isolation or JI.



With a DI process, the reverse biased P-N junction is replaced by a high-quality, high field strength (Breakdown >800 Volts) silicon dioxide dielectric layer. Physically, this is realized by fabricating the circuit elements in individual silicon islands that are surrounded by silicon dioxide.



The process steps by which the DI islands are formed in the silicon substrate involves a combination of crystallographic preferential etching, oxidation, thick poly-silicon deposition and grinding and polishing.

BENEFITS

Compared to JI arrays, DI offers users of the SP1000 family several key advantages:

- The elimination of all parasitic 4-layer paths. These paths are prone to latch-up which can cause catastrophic damage to an IC.
- Elimination of isolation junction leakage currents. This is especially beneficial for applications that are required to work at high temperature.
- Significant reduction in the parasitic capacitance due to the isolation element. This can be especially beneficial in high speed designs.
- Availability of full function high performance (i.e. high bandwidth, high gain and high useable current) complementary NPN & PNP transistors.
- Simplified design and modeling since most of the parasitics unique to conventional IC's are eliminated.

PROCESS OPTIONS

Maximum operating voltage is a key requirement in most applications. For an analog ASIC application the maximum possible voltage is ultimately limited by the breakdown voltage of the transistors. The lowest breakdown voltage is usually V_{CEO} and process application capability is specified by this parameter. The V_{CEO} is determined by a combination of starting silicon resistivity and transistor geometries (i.e. spacings). Higher starting silicon resistivity gives higher V_{CEO}, but at the expense of slightly higher transistor parasitics (mainly R_C) which will ultimately limit circuit performance.

The SP1000 arrays are available in two process options: 20 Volt and 35 Volt processes. V_{CEO}'s of 35 Volts and 20 Volts are achieved through control of substrate resistivity. The 20 Volt V_{CEO} process offers somewhat lower parasitics, and therefore, higher speed. This is the preferred process for high speed applications, if maximum voltages can be held below 20 Volts.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

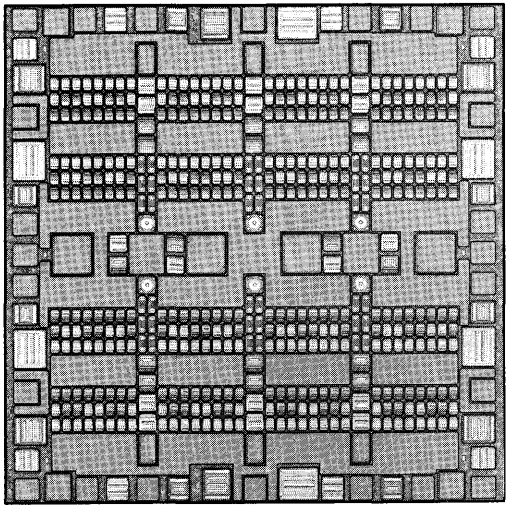
SP1104

HIGH PERFORMANCE ANALOG ARRAY

DESCRIPTION

The SP1104 is a high density, high performance analog array containing 444 linear bipolar transistors. Twelve high current transistors capable of driving up to 100 mA each directly off the IC are available as well as numerous other components commonly used to implement high performance analog functions. The SP1104 is a member of Sipex's SP1000 family of analog arrays which is configured around a standard tile of 24 1x geometry transistors.

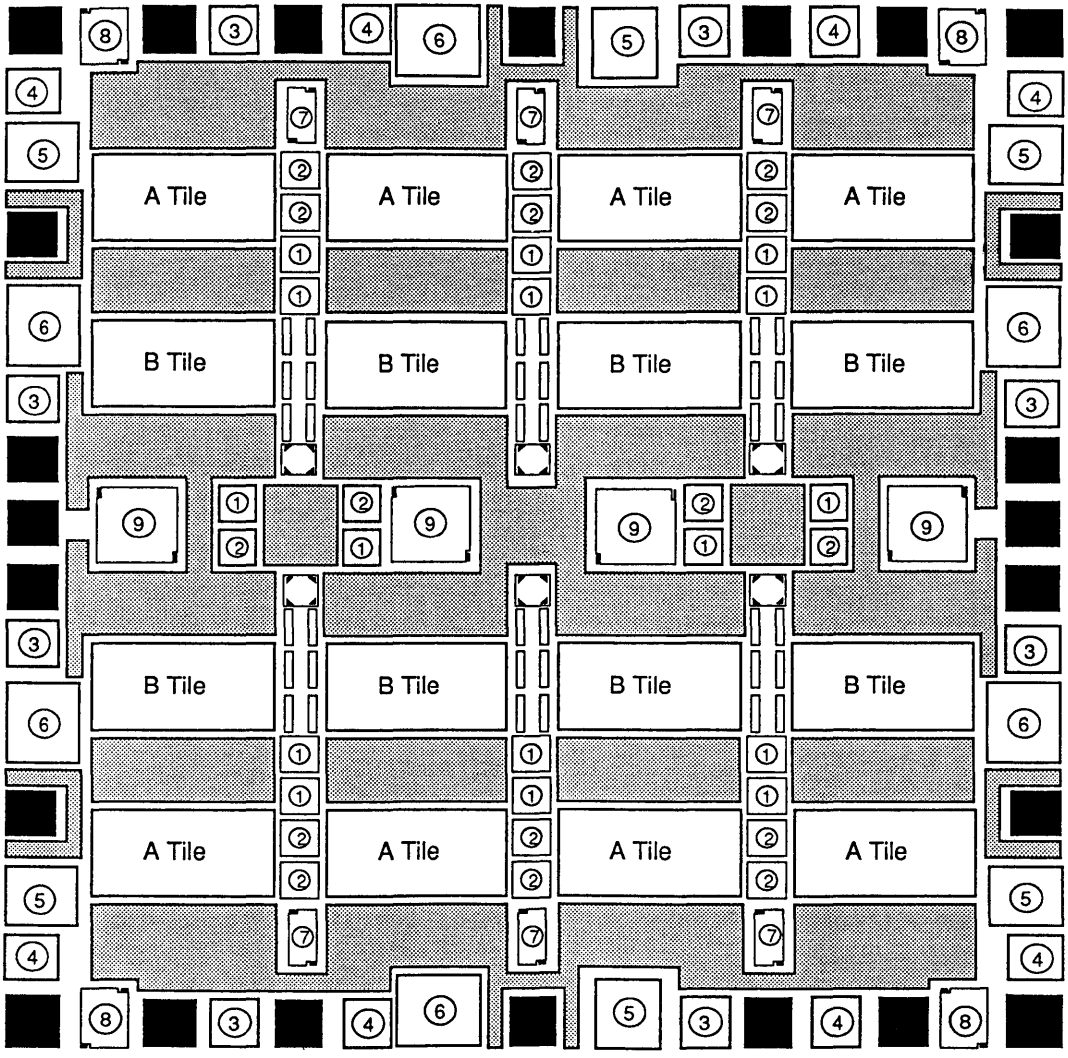
High gain, high bandwidth complementary vertical NPN & PNP transistors coupled with precision thin film resistors make the SP1104 ideally suited for implementing cost effective ASIC solutions to high speed, high precision analog signal conditioning and signal processing applications.



FEATURES

- Dielectric Isolation (DI) for Minimum Parasitics and Optimum Latch-up Free Performance
- 35 Volt or 20 Volt Operation
- 16 Tile Array Structure
- 222 Vertical NPN Transistors; $\beta \approx 200$, $f_T \approx 1000$ MHz
- 222 Vertical PNP Transistors; $\beta \approx 150$, $f_T \approx 600$ MHz
- High Output Drive Capability, up to 100 mA per output stage
- Precision Low Tc Thin Film Resistors; TC = 100 ppm/°C or TC = 300 ppm/°C
- Laser Trimming for Enhanced Precision; Matching to 0.02%
- Dual Layer Aluminum Metalization
- Tile Based Architecture Supported by a Macro Cell Library

SP-1104



Bond Pad

Nichrome Clear Field Area

Pinch Resistor

Buried Zener

① DBNPN

② DBPNP

③ MNPN

④ MPNP

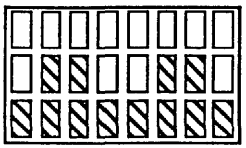
⑤ HNPN

⑥ HPNP

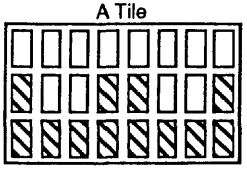
⑦ 5 pF Capacitor

⑧ 8 pF Capacitor

⑨ 18 pF Capacitor



A Tile



B Tile

SPNP

SNPN

SP1104 COMPONENT COUNT SUMMARY

DESCRIPTION	COUNT
Tiles:	
A Type	8
B Type	8
Transistors:	
SNPN	192
SPNP	192
DBNPN	16
DBPNP	16
MNPN	8
MPNP	8
HNPN	6
HPNP	6
Thin Film Resistors:	
Clear Field Area	5700 sq. mil (Total 800 KΩ Possible)
Pinch Resistors	36
Capacitors:	
5 pF (max)	6
8 pF (max)	4
18 pF (max)	4
Buried Zener Diodes	6
Bond Pads	24
Die Dimensions	143 mils x 140 mils

ARCHITECTURE & ORGANIZATION

The organization and complexity of the SP1104 array makes it ideally suited for integrating complete analog system functions on a single silicon chip. The SP1104 employs a tile based architecture where each tile has been configured (sized) so that it can contain a complete analog function. Pre-defined macro functions which fit these tiles are available and can be used to implement analog systems thus eliminating the tedious task of transistor level design. Using this approach also reduces both the manpower and elapsed time required to complete a design, while increasing the probability of first time success.

Each tile on the SP1104 consists of 12 SNPN & 12 SPNP transistors arranged in a 3 x 8 matrix. There are both A type & B type tiles. The only difference between the two tile types is that the locations of the SNPN & SPNP transistors in the middle row of the tile are reversed. As a result, A type tiles have two NPN Quads & one PNP Quad while the B type tiles have two PNP Quads and one NPN Quad. This feature simplifies many types of layouts.

The SP1104 is organized as a 4 x 4 matrix of tiles. The top and bottom rows have A type tiles, and the two middle rows contain the B type tiles. Above and below each tile is a clear field area which is reserved for user defined thin film resistors. Interspersed between the tiles and around the periphery of the array are the various other components available on the array.

To accommodate rapid layout, all SP1104 components are positioned on a 15μ grid. Within the clear field area there is 5μ sub grid for thin-film resistor layout. The SP1104 is symmetric about the two perpendicular center lines of the array. There are additional symmetries within the tiles themselves as well as between adjacent tiles which facilitate replication of structures to speed design and layout.

The dimensions of the SP1104 are 140 mils x 143 mils.

PROCESS OPTIONS

Maximum operating voltage is usually a key requirement in most applications. For an analog ASIC application the maximum possible voltage is ultimately limited by the breakdown voltage of the transistors. The lowest breakdown voltage is usually V_{CEO} and process application capability is specified by this parameter. The V_{CEO} is determined by a combination of starting silicon resistivity and transistor geometries (i.e. spacings). Higher starting silicon resistivity gives higher V_{CEO}, but at the expense of slightly higher transistor parasitics (mainly R_C) which will ultimately limit circuit performance.

The SP1104 array is available in two process options: 20 Volt and 35 Volt processes. By controlling substrate resistivity, V_{CEO}'s of 35 Volts & 20 Volts are achieved. The 20 Volt V_{CEO} process offers somewhat lower parasitics, and therefore, higher speed. This is the preferred process for high speed applications, if maximum voltages can be held below 20 Volts.

MACRO CELLS

Design time, cost and risk can be reduced significantly by designing with proven macro cells rather than at the transistor device level. A library of macro cells has been developed to support SP1104 user designs. Additional macros will be added to the library as they become available. Before starting your design, consult your local SIPEX sales office or the factory to obtain the latest update on available macro cells.

SP1104 MACRO CELL LIBRARY

CELL NAME	DESCRIPTION	# OF TILES
MXRB01	1.5V Voltage Reference	0.5
MXRB02	2.5V Voltage Reference	1
MXRB03	2.5V Voltage Reference a ±0.5 mA Current Reference	1
MXRB05	5.0V Voltage Reference	1
MXRB10	10.0V Voltage Reference	1
MXOP01	General Purpose Wideband Op Amp	1
MXOP02	Wideband, Medium Drive Op Amp	2
MXOP03	Precision High Bandwidth Op Amp	2
MXTA01	Transimpedance Amplifier	2+
MXCM01	General Purpose Comparator	1

SUPPORT PRODUCTS & SERVICES

- Commercially Available P-SPICE or Equivalent Simulators (Purchased Directly From the Vendor)
- Design Manual (DESMAN 1100)
- Mylar Layout Worksheets
- GDS II Database Tape for Workstations Based Layouts
- A Family of Proven Macro Cells (Circuit Schematics and Net Lists are Available in the Design Manual)
- Transistor Level and Macro Cell Kit Parts to Support Evaluation and Breadboarding (If Required)
- Application Assistance and Training by Sipex Personnel

SP1204

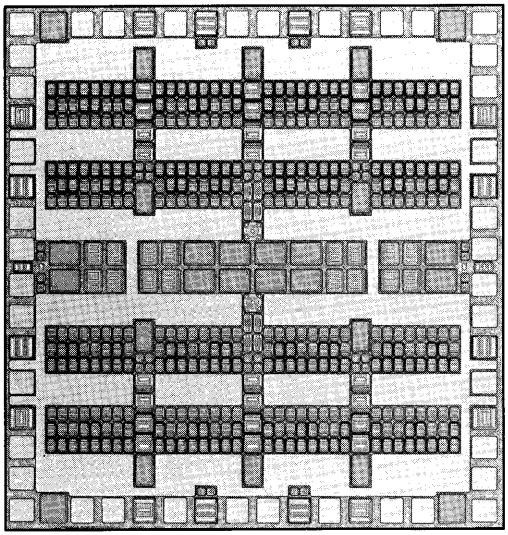
HIGH I/O ANALOG ARRAY WITH JFETS

DESCRIPTION

The SP1204 is a high density, high performance analog array containing 428 linear bipolar transistors and 16 P-channel JFET transistors as well as numerous other components commonly used to implement high performance analog functions. The SP1204 is a member of Sipex's SP1000 family of analog arrays which is configured around a standard tile of 24 1x geometry transistors.

High gain, high bandwidth complementary vertical NPN & PNP transistors coupled with precision thin film resistors make the SP1204 ideally suited for implementing cost effective ASIC solutions to high speed, high precision analog signal conditioning and signal processing applications.

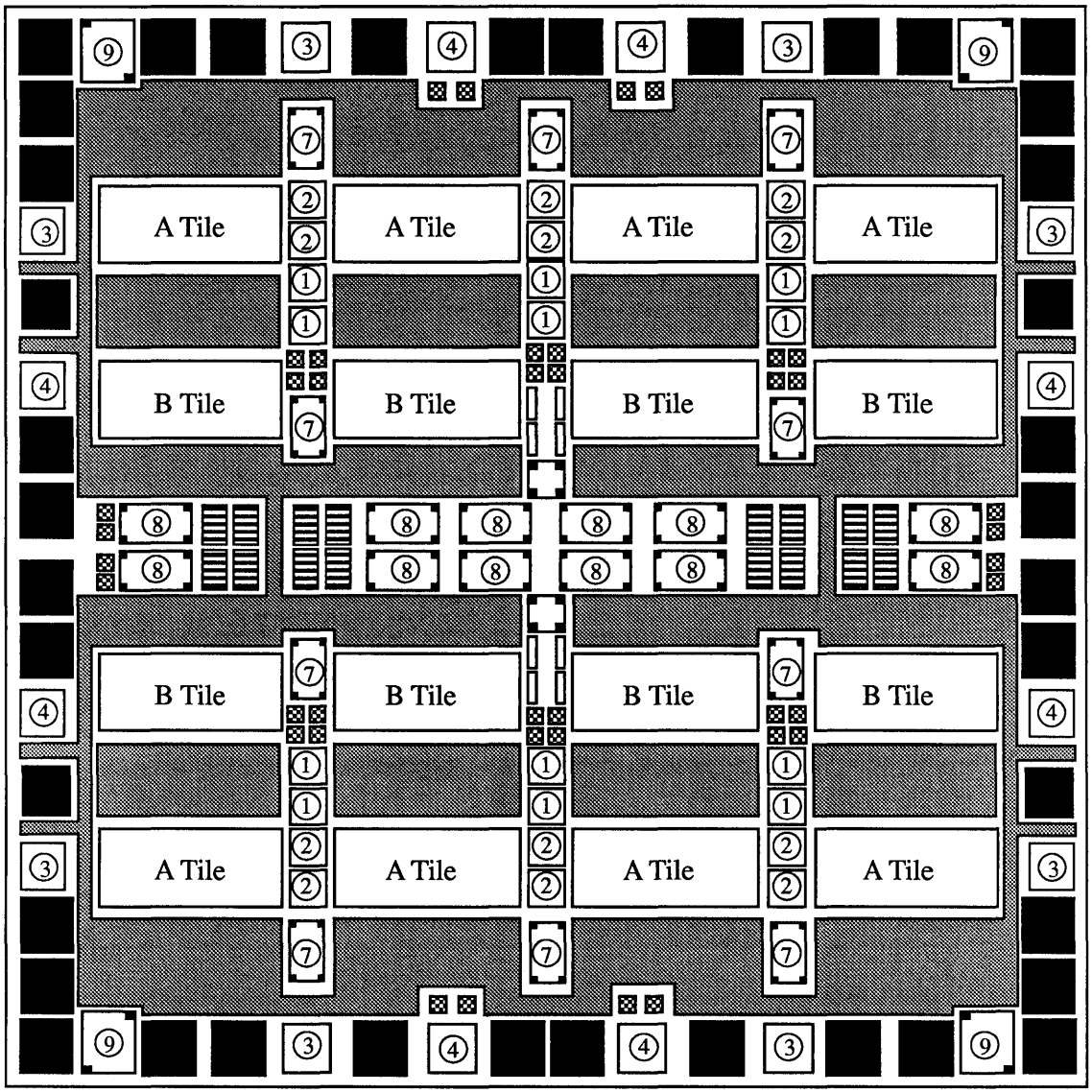
The availability of 16 P-channel JFETs makes the SP1204 particularly suited for those applications where extremely low input bias currents are required. These JFETs can also be used as switches.



FEATURES

- Dielectric Isolation (DI) for Minimum Parasitics and Optimum Latch-up Free Performance
- 35 Volt Operation
- 16 Tile Array Structure
- 216 Vertical NPN Transistors; $\beta \approx 200$, $f_T \approx 1000$ MHz
- 216 Vertical PNP Transistors; $\beta \approx 150$, $f_T \approx 600$ MHz
- 40 Bond Pads for High I/O Circuits
- 16 P-channel JFETS
- Precision Low TC Thin Film Resistors; TC = 100 ppm/°C or TC = 300 ppm/°C
- Laser Trimming for Enhanced Precision; Matching to 0.02%
- Dual Layer Aluminum Metalization
- Tile Based Architecture Supported by a Macro Cell Library

SP - 1204



Bond Pad

Buried Zener

Nichrome Clear Field Area

N+ /P+ Diode

P-JFET

Pinch Resistor

1 DBNPN

2 DBPNP

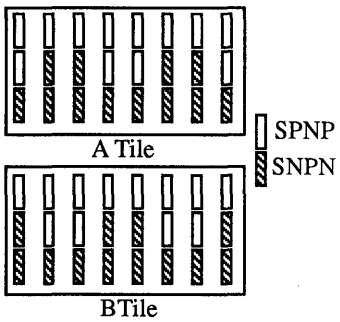
3 MNPN

4 MPNP

7 4.5pF Capacitor

8 6pF Capacitor

9 7pF Capacitor



SP1204 COMPONENT COUNT SUMMARY

DESCRIPTION	COUNT
Tiles:	
A Type	8
B Type	8
Transistors:	
SNPN	192
SPNP	192
DBNPN	16
DBPNP	16
MNPN	8
MPNP	8
HNPN	0
HPNP	0
P-JFET	16
Thin Film Resistors:	
Clear Field Area	5700 sq. mil (Total 800 KΩ Possible)
Pinch Resistors	8
Capacitors:	
4.5 pF (max)	10
6 pF (max)	12
7 pF (max)	4
Diodes:	
Buried Zener	2
N+/P+ Diodes	40
Bond Pads	40
Die Dimensions	146 mils x 140 mils

ARCHITECTURE & ORGANIZATION

The organization and complexity of the SP1204 array makes it ideally suited for integrating complete analog system functions on a single silicon chip. The SP1204 employs a tile based architecture where each tile has been configured (sized) so that it can contain a complete analog function. Pre-defined macro functions which fit these tiles are available and can be used to implement analog systems thus eliminating the tedious task of transistor level design. Using this approach also reduces both the manpower and elapsed time required to complete a design, while increasing the probability of first time success.

Each tile on the SP1204 consists of 12 SNPN & 12 SPNP transistors arranged in a 3 x 8 matrix. There are both A type & B type tiles. The only difference between the two tile types is that the locations of the SNPN & SPNP transistors in the middle row of the tile are reversed. As a result, A type tiles have two NPN Quads & one PNP Quad while the B type tiles have two PNP Quads and one NPN Quad. This feature simplifies many types of layouts.

The SP1204 is organized as a 4 x 4 matrix of tiles. The top and bottom rows have A type tiles while the two middle rows contain the B type tiles. Sixteen P-JFETs, arranged in quads, lie across the center of the die. The P-JFETs are only available with the 35 Volt process. (These areas are inactive when using the 20 Volt process).

Above and below each tile is a clear field area which is reserved for user defined thin film resistors. Interspersed between the tiles and around the periphery of the array are the various components available on the array.

To accommodate rapid layout, all SP1204 components are positioned on a 15μ grid. Within the clear field area there is a 5μ sub grid for thin-film resistor layout. The SP1204 is symmetric about the two perpendicular center lines of the array. There are additional symmetries within the tiles themselves as well as between adjacent tiles.

The dimensions of the SP1204 are 140 mils x 146 mils.

PROCESS OPTIONS

Maximum operating voltage is usually a key requirement in most applications. For an analog ASIC application the maximum possible voltage is ultimately limited by the breakdown voltage of the transistors. The lowest breakdown voltage is usually V_{CEO} and process application capability is specified by this parameter. The V_{CEO} is determined by a combination of starting silicon resistivity and transistor geometries (i.e. spacings). Higher starting silicon resistivity gives higher V_{CEO}, but at the expense of slightly higher transistor parasitics (mainly R_C) which will ultimately limit circuit performance.

The SP1204 array is available in two process options: 20 Volt and 35 Volt processes. By controlling substrate resistivity, V_{CEO}'s of 35 Volts & 20 Volts are achieved. The 20 Volt V_{CEO} process offers somewhat lower parasitics, and therefore, higher speed. This is the preferred process for high speed applications, if maximum voltages can be held below 20 Volts.

MACRO CELLS

Design time, cost and risk can be reduced significantly by designing with proven macro cells rather than at the transistor device level. A library of macro cells has been developed to support SP1204 user designs. Additional macros will be added to the library as they become available. Before starting your design, consult your local SIPEX sales office or the factory to obtain the latest update on available macro cells.

SP1204 MACRO CELL LIBRARY

CELL NAME	DESCRIPTION	# OF TILES
MXRB01	1.5V Voltage Reference	0.5
MXRB02	2.5V Voltage Reference	1
MXRB03	2.5V Voltage Reference a ±0.5 mA Current Reference	1
MXRB05	5.0V Voltage Reference	1
MXRB10	10.0V Voltage Reference	1
MXOP01	General Purpose Wideband Op Amp	1
MXOP02	Wideband, Medium Drive Op Amp	2
MXOP03	Precision High Bandwidth Op Amp	2
MXCM01	General Purpose Comparator	1

SUPPORT PRODUCTS & SERVICES

- Commercially Available P-SPICE or Equivalent Simulators (Purchased Directly From the Vendor)
- Design Manual (DESMAN 1100)
- Mylar Layout Worksheets
- GDS II Database Tape for Workstations Based Layouts
- A Family of Proven Macro Cells (Circuit Schematics and Net Lists are Available in the Design Manual)
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- Application Assistance and Training by Sipex Personnel

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP2107

SYSTEM LEVEL ANALOG ARRAY

2

DESCRIPTION

The SP2107 is a high density, high performance analog array containing 780 linear bipolar transistors. Twenty-four high current transistors capable of driving up to 100 mA each directly off the IC are available as well as numerous other components commonly used to implement high performance analog functions. The SP2107 is a member of Sipex's SP2000 family of analog arrays which is configured around a standard tile of 32 1x geometry transistors.

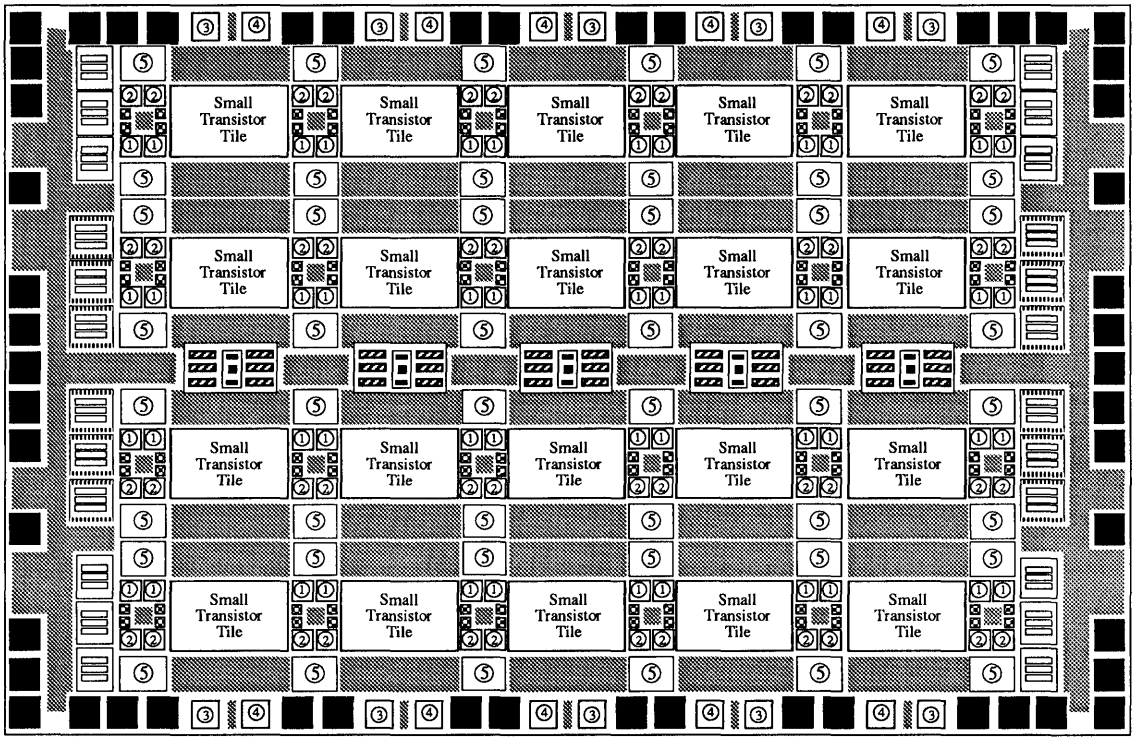
High gain, high bandwidth complementary vertical NPN & PNP transistors coupled with precision thin film resistors make the SP2107 ideally suited for implementing cost effective ASIC solutions to high speed, high precision analog signal conditioning and signal processing applications.

PRELIMINARY DATA

FEATURES

- Dielectric Isolation (DI) for Minimum Parasitics and Optimum Latch-up Free Performance
- 35 Volt or 20 Volt Operation
- 20 Tile Array Structure
- 320 Vertical NPN Transistors; $\beta \approx 200$, $f_T \approx 1000$ MHz
- 320 Vertical PNP Transistors; $\beta \approx 150$, $f_T \approx 600$ MHz
- High Output Drive Capability, up to 100 mA per output stage
- Precision Low TC Thin Film Resistors; TC = 100 ppm/°C or TC = 300 ppm/°C
- Laser Trimming for Enhanced Precision; Matching to 0.02%
- Dual Layer Aluminum Metalization
- Tile Based Architecture Supported by a Macro Cell Library

SP - 2107



Bond Pad

Buried Zener

Nichrome Clear Field Area

HPNP

HNPN

N+ /P+ Diode

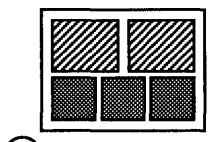
Pinch Resistor

1 DBNPN

2 DBPNP

3 MNPN

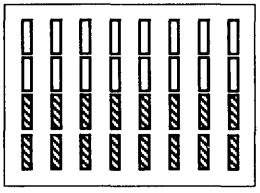
4 MPNP



5 Capacitor Block

2 pF

1 pF



SPNP

SNPN

Small Transistor Tile

SP2107 COMPONENT COUNT SUMMARY

DESCRIPTION	COUNT
Tiles:	20
Transistors:	
SNPN	320
SPNP	320
DBNPN	48
DBPNP	48
MNPN	10
MPNP	10
HNPN	12
HPNP	12
Thin Film Resistors:	
Clear Field Area	10,000 sq. mils. (Total 1200 KΩ Possible)
Pinch Resistors	30
Capacitors:	
1 pF (max)	144
2 pF (max)	96 (Total 336 pF Possible)
Diodes:	
Buried Zener	5
N+/P+ Diodes	96
Bond Pads	54
Die Dimensions	159 mils x 236 mils

ARCHITECTURE & ORGANIZATION

The organization and complexity of the SP2107 array makes it ideally suited for integrating complete analog system functions on a single silicon chip. The SP2107 employs a tile based architecture where each tile has been configured (sized) so that it can contain a complete high performance analog function. Pre-defined macro functions which fit these tiles are available and can be used to implement analog systems thus eliminating the tedious task of transistor level design. Using this approach also reduces both the manpower and elapsed time required to complete a design, while increasing the probability of first time success.

Each tile on the SP2107 consists of 16 SNPN & 16 SPNP transistors arranged in a 4 x 8 matrix. The symmetry of the array of transistors, capacitors and thin film area facilitates placement of macrocells within a tile. This feature simplifies many types of layouts.

The SP2107 is organized as a 4 x 5 matrix of tiles. This structure is ideal for complex quad systems or 5 channel systems of medium complexity. All tiles are identical to allow easy replication of multi-channel systems. Above and below each tile is a clear field area which is reserved for user defined thin film resistors. Interspersed between the tiles and around the periphery of the array are the various other components available on the array.

To accommodate rapid layout, all SP2107 components are positioned on a 15μ grid. Within the clear field area there is 5μ sub grid for thin-film resistor layout. The SP2107 is symmetric about the two perpendicular center lines of the array. There are additional symmetries within the tiles themselves as well as between adjacent tiles which facilitate replication of structures to speed design and layout.

The dimensions of the SP2107 are 236 mils x 159 mils.

PROCESS OPTIONS

Maximum operating voltage is usually a key requirement in most applications. For an analog ASIC application the maximum possible voltage is ultimately limited by the breakdown voltage of the transistors. The lowest breakdown voltage is usually V_{CEO} and process application capability is specified by this parameter. The V_{CEO} is determined by a combination of starting silicon resistivity and transistor geometries (i.e. spacings). Higher starting silicon resistivity gives higher V_{CEO}, but at the expense of slightly higher transistor parasitics (mainly R_C) which will ultimately limit circuit performance.

The SP2107 array is available in two process options: 20 Volt and 35 Volt processes. By controlling substrate resistivity, V_{CEO}'s of 35 Volts & 20 Volts are achieved. The 20 Volt V_{CEO} process offers somewhat lower parasitics, and therefore, higher speed. This is the preferred process for high speed applications, if maximum voltages can be held below 20 Volts.

MACRO CELLS

Design time, cost and risk can be reduced significantly by designing with proven macro cells rather than at the transistor device level. A library of macro cells has been developed to support SP2107 user designs. Additional macros will be added to the library as they become available. The macrocells for the SP1000 products are not usable on the SP2000 series arrays. Before starting your design, consult your local SIPEX sales office or the factory to obtain the latest update on available macro cells.

SUPPORT PRODUCTS & SERVICES

- Commercially Available P-SPICE or Equivalent Simulators (Purchased Directly From the Vendor)
- Design Manual (DESMAN 1100)
- Mylar Layout Worksheets
- GDS II Database Tape for Workstations Based Layouts
- A Family of Proven Macro Cells (Circuit Schematics and Net Lists are Available in the Design Manual)
- Transistor Level and Macro Cell Kit Parts to Support Evaluation and Breadboarding (If Required)
- Application Assistance and Training by Sipex Personnel

SP2107 MACRO CELL LIBRARY

CELL NAME	DESCRIPTION	# OF TILES
Operational Amplifiers		
OPA-01	General Purpose	<1
OPA-02	General Purpose w/Class A/B	1
OPA-03	Precision Op Amp, Low IB	1.5
OPA-05	General Purpose Clamped Output	1
Transimpedance Amplifier		
TZA-01	Wide Bandwidth	2
Comparators		
CMP-01	Wide Band, Single Supply	1
CMP-02	Wide Band, Dual Supply	1
CMP-04	2-Input Window Comparator	1
Multipliers		
MLT-01	2 Quadrant, Current Output	2
MLT-02	4 Quadrant, Current Output	2
MLT-03	4 Quadrant, Voltage Output	2
MLT-04	4 Quadrant, Digital, I Output	2
Sample and Hold Amplifiers		
SHA-01	Voltage Output S/H	3
Full Wave Rectifier		
FWR-01	General Purpose, +I Out	1
FWR-02	General Purpose, -I Out	1
General Bias Circuit		
BAS-01	Low TC Current Bias	1-2

COMPONENT DESCRIPTIONS

COMPONENT DESCRIPTIONS

Device level components available for use on the SP1000 arrays include both NPN and PNP transistors, thin-film resistors, pinch resistors, capacitors and buried zener diodes. Both nominal and worst case (i.e. process and temperature extremes) SPICE model parameters are available for all of these components.

To meet the range of performance requirements (I.e. drive, noise, ratios, etc.) typically required in analog ASIC applications, the SP1000 arrays contain several different complementary geometry bipolar transistors.

SNPN/SPNP

These transistors are the minimum geometry 1 x devices available on the array with drawn emitter dimensions of 10µ x 38µ. These devices offer excellent performance with a useable current range of 0.1 µA to 1 mA. These minimum geometry transistors have been designed to support a broad range of applications and are the workhorse transistors on the SP1000 array family.

	SNPN	SPNP
SP1104	192	192
SP1204	192	192

DBNPN/DBPNP

These transistors are 4 x geometry devices with a double base contact stripe for low base resistance (R_B). Low base resistance is a key requirement in low noise designs. The higher drive capability inherent in these 4 x devices makes them ideal for driving high slew rate nodes or for driving directly off the chip.

	DBNPN	DBPNP
SP1104	16	16
SP1204	16	16

MNPN/MPNP

These transistors are intended primarily as pre-drivers for the higher current HNPN/HPNP devices. Their emitter areas are 0.2 x those of the "H" devices. They have both double base and double collector stripe contacts for low R_B & low R_C. In addition to being used as a pre-driver for the "H" devices, these devices can be used to directly drive outputs or internal nodes requiring high slew rates.

	MNPN	MPNP
SP1104	8	8
SP1204	8	8

HNPN/HPNP

These transistors are large geometry devices intended to drive large currents (i.e. up to 100 mA) directly off the chip. The HNPN is a 20 x device and the HPNP is a 30 x device. Both the HNPN and HPNP devices have double base and double collector stripe contacts for low R_B and low R_C. They also have triple emitter stripe contacts.

	HNPN	HPNP
SP1104	6	6
SP1204	0	0

THIN FILM RESISTORS

Thin film nichrome metal resistors are the principal type of application resistor used on the SP1000 array. Each resistor is user defined by specifying both the resistor length & width (i.e. R=p(w/l)). For resistors which require trimming, the minimum width is 10µ. Trimmable resistors must be a minimum of 50µ wide. On chip resistor matching can be improved by utilizing larger than minimum widths. Thin film resistors are defined in the clear field areas available on the array. For the SP1000 family the maximum resistance utilizing 175Ω/ nichrome is approximately 800 KΩ's.

	MAX RESISTANCE
SP1104	800 KΩ
SP1204	800 KΩ

PINCH RESISTORS

Pinch resistors are high value resistors with very poor accuracy. Their principal attribute is the very small chip area they consume. They are useful in applications such as start-up and bleeder circuits that require neither absolute nor relative accuracy. The breakdown voltage of these devices is under 8.0 Volts. To achieve larger breakdowns, multiple resistors can be connected in series.

	QTY
SP1104	36
SP1204	8

CAPACITORS

Capacitors on the SP1000 arrays are of the MOS type (i.e. aluminum - silicon dioxide - N+ silicon). This structure has the advantage of virtually no voltage or temperature dependence. There are three different capacitor sizes on each array with maximum values ranging from 4.5 pF to 18 pF. Any capacitor may be programmed to a lower value by decreasing the area of the top aluminum plate.

	QTY CAPS	LARGEST CAP	TOTAL VALUE
SP1104	14	18 pF	134 pF
SP1204	26	7 pF	135 pF

BURIED ZENER DIODE

Buried zener diodes are N+/P+ junctions with zener breakdown occurring below the silicon surface. This eliminates surface effects and makes the device an extremely stable element. The diode has a single anode contact (P+) and four cathode (N+) contacts. The latter permits Kelvin connections of the zener diode.

	QTY
SP1104	6
SP1204	2

P-JFET TRANSISTORS

These transistors are intended for applications requiring extremely low input bias or leakage currents (e.g. sample & hold functions). They are typically used as quads, and they are arranged as four quads spread across the center of the array. These devices are only available on the 35 volt SP1204 array.

	20V	35V
SP1104	0	0
SP1204	0	16

N+/P+ DIODES

These diodes have breakdowns less than a V_{EBO} and can be used to protect emitter base junctions from damage from excess reverse voltage.

	QTY
SP1104	0
SP1204	40

ABSOLUTE MAXIMUM RATINGS - 20 VOLT PROCESS

V_{CEO} ..... 20 Volts
V_{EBO} ..... 6.5 Volts
Storage Temperature Range ..... $-65°C < T_A < 150°C$
Maximum Operating Junction Temperature ..... 150°C

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS
SNPN						
Gain	β	Typical I_C = 1 mA		200		
Bandwidth	f_T	Typical I_C = 2 mA, V_{CE} = 5V		990	1000	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-05		5	mA
Early Voltage	V_A	$V_A = R_O * I_C$		110		V
SPNP						
Gain	β	Typical I_C = 1 mA		150		
Bandwidth	f_T	Typical I_C = 2 mA, V_{CE} = 5V		660	700	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-05		4	mA
Early Voltage	V_A	$V_A = R_O * I_C$		110		V
DBNPN						
Gain	β	Typical I_C = 1 mA		175		
Bandwidth	f_T	Typical I_C = 5 mA, V_{CE} = 5V		825	950	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-05		20	mA
Early Voltage	V_A	$V_A = R_O * I_C$		100		V
DBPNP						
Gain	β	Typical I_C = 1 mA		160		
Bandwidth	f_T	Typical I_C = 5 mA, V_{CE} = 5V		380	500	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-05		20	mA
Early Voltage	V_A	$V_A = R_O * I_C$		50		V
MNPN						
Gain	β	Typical I_C = 1 mA		180		
Bandwidth	f_T	Typical I_C = 10 mA, V_{CE} = 5V		850	900	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-04		30	mA
Early Voltage	V_A	$V_A = R_O * I_C$		100		V
MPNP						
Gain	β	Typical I_C = 1 mA		150		
Bandwidth	f_T	Typical I_C = 10 mA, V_{CE} = 5V		580	620	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-04		30	mA
Early Voltage	V_A	$V_A = R_O * I_C$		50		V
HNPN						
Gain	β	Typical I_C = 1 mA		190		
Bandwidth	f_T	Typical I_C = 25 mA, V_{CE} = 10V		750	850	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	1		100	mA
Early Voltage	V_A	$V_A = R_O * I_C$		100		V
HPNP						
Gain	β	Typical I_C = 1 mA		150		
Bandwidth	f_T	Typical I_C = 25 mA, V_{CE} = 10V		375	450	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	1		100	mA
Early Voltage	V_A	$V_A = R_O * I_C$		50		V

*Unless otherwise noted, specifications apply for T_A = 25°C

ABSOLUTE MAXIMUM RATINGS - 35 VOLT PROCESS

V_{CEO} ..... 35 Volts
V_{EBO} ..... 6.5 Volts
Storage Temperature Range ..... $-65°C < T_A < 150°C$
Maximum Operating Junction Temperature ..... 150°C

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS
SNPN						
Gain	β	Typical I_C = 1 mA		200		
Bandwidth	f_T	Typical I_C = 2 mA, V_{CE} = 5V		900	950	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-05		5	mA
Early Voltage	V_A	$V_A = R_O * I_C$		110		V
SPNP						
Gain	β	Typical I_C = 1 mA		140		
Bandwidth	f_T	Typical I_C = 2 mA, V_{CE} = 5V		490	500	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-05		4	mA
Early Voltage	V_A	$V_A = R_O * I_C$		100		V
DBNPN						
Gain	β	Typical I_C = 1 mA		180		
Bandwidth	f_T	Typical I_C = 5 mA, V_{CE} = 5V		750	950	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-05		20	mA
Early Voltage	V_A	$V_A = R_O * I_C$		100		V
DBPNP						
Gain	β	Typical I_C = 1 mA		140		
Bandwidth	f_T	Typical I_C = 5 mA, V_{CE} = 5V		380	500	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-05		20	mA
Early Voltage	V_A	$V_A = R_O * I_C$		50		V
MNPN						
Gain	β	Typical I_C = 1 mA		140		
Bandwidth	f_T	Typical I_C = 10 mA, V_{CE} = 5V		850	900	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-04		30	mA
Early Voltage	V_A	$V_A = R_O * I_C$		100		V
MPNP						
Gain	β	Typical I_C = 1 mA		150		
Bandwidth	f_T	Typical I_C = 10 mA, V_{CE} = 5V		400	450	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	5E-04		30	mA
Early Voltage	V_A	$V_A = R_O * I_C$		50		V
HNPN						
Gain	β	Typical I_C = 1 mA		190		
Bandwidth	f_T	Typical I_C = 25 mA, V_{CE} = 10V		700	850	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	1		100	mA
Early Voltage	V_A	$V_A = R_O * I_C$		100		V
HPNP						
Gain	β	Typical I_C = 1 mA		150		
Bandwidth	f_T	Typical I_C = 25 mA, V_{CE} = 10V		350	450	MHz
Current Range	I_C Range	@ β = 0.7 β (max)	1		100	mA
Early Voltage	V_A	$V_A = R_O * I_C$		50		V
P-JFET						
Gain	β			9		µA/V
Current	I_{DSS}			93		µA
Threshold	V_{TP}	Typical I_C = 1 mA		1.1		V
Lambda	L_{AM}			0.044		V^{-1}

*Unless otherwise noted, specifications apply for T_A = 25°C

ABSOLUTE MAXIMUM RATINGS

V_{CEO} ..... 20V or 35V
V_{EBO} 6.5V
Storage Temperature Range ..... $-65°C \leq T_A \leq 150°C$
Maximum Operating Junction Temperature ..... 150°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, specifications apply for $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
NICHROME RESISTOR (I)						
Sheet Resistivity	ρ		140	175	210	Ω/sq.
Temp. Coefficient	Δ R/(R•Δ T)	((((R1-R2)/(R1+R2)/2))/(T1-T2))•1E+6		100	150	ppm/°C
Voltage Coefficient	Δ R/(R•Δ T)	((((R1-R2)/(R1+R2)/2))/(V1-V2))•1E+6		0		ppm/V
Parasitic Capacitance	C	Resistor Body and End Caps		4E-5		pF/μ^2
Matching	Δ R/R	Identical Geometry, (((R1-R2)/(R1+R2)/2))•100 Resistor Width = 25 microns		0.1		%
NICHROME RESISTOR (II)						
Sheet Resistivity	ρ		140	175	210	Ω/sq.
Temp. Coefficient	Δ R/(R•Δ T)	((((R1-R2)/(R1+R2)/2))/(T1-T2))•1E+6		300	350	ppm/°C
Voltage Coefficient	Δ R/(R•Δ T)	((((R1-R2)/(R1+R2)/2))/(V1-V2))•1E+6		0		ppm/V
Parasitic Capacitance	C	Resistor Body and End Caps		4E-5		pF/μ^2
Matching	Δ R/R	Identical Geometry, (((R1-R2)/(R1+R2)/2))•100 Resistor Width = 25 microns		0.1		%
CAPACITOR						
Capacitance	C		0.27	0.31	0.25	fF/μ^2
Matching	Δ C/C	(((C1-C2)/(C1+C2)/2))•100	-5		+5	%
Voltage Coefficient	Δ C/Δ V	(C1-C2)/(V1-V2)		0		fF/V
Temp. Coefficient	Δ C/(C•Δ T)	((((C1-C2)/(C1+C2)/2))/(T1-T2))		-5E-7		$(°C)^{-1}$
PINCH RESISTOR						
Resistance	R		15	35	70	KΩ
Temp. Coefficient	Δ R/(R•Δ T)	((((R1-R2)/(R1+R2)/2))/(T1-T2))•1E+6		4900		ppm/°C
Matching	Δ R/R	(((R1-R2)/(R1+R2)/2))•100	-20		+20	%
BURIED ZENER						
Zener Voltage	V_Z	I_Z - 500 μA	5.3	5.5	5.7	Volts
Temp. Coefficient	$\Delta V_Z/\Delta T$	Kelvin Configuration		1.6		mV/°C

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MACRO CELL DESCRIPTION

The datasheets in this section describe the currently available macro cells for the SP1000 family of arrays. Except as noted all macro cells can be implemented on any of the arrays in this family. The parameters presented are for the 35 Volt process. Variations for the 20 Volt process are indicated in the notes for each cell as required.

Cell Name	Description	Page
MBRB01	1.25V Voltage Reference	
MBRB02	2.5V Voltage Reference	
MBRB05	5.0V Voltage Reference	
MBRB10	10.0V Voltage Reference	
MBOP01	General Purpose Wideband Op-Amp	
MBOP02	High Output Current, Wideband Op-Amp	
MBOP03	High Performance Op-Amp	
MBTA01	Transimpedance Amplifier	
MBCM01	High Speed Comparator	

1.25V VOLTAGE REFERENCE
SP1000 FAMILY — 35 VOLT PROCESS

DESCRIPTION

The MBRB01 is a voltage reference macro cell featuring a 1.25 Volt output. It is useable with any SP1000 family array product fabricated on Sipex's 35 Volt process. The basic reference element is a "BAND-GAP" with first order temperature compensation. To achieve optimum temperature performance, the MBRB01 employs NiCr thin film resistors with appropriate matching to minimize temperature effects.

Key features of the MBRB01 are its low output voltage (1.25 Volts), and the very simple circuit design which results in low component usage. It is ideally suited for low voltage applications. The low component usage, half a tile, makes it especially attractive in very dense designs where component count is stretched to the limit. The simple design does, however, result in higher Temperature Coefficients (i.e. 400 ppm/°C max) than other macro cell references in the SP1000 library.

Applications for the MBRB01 include setting threshold levels and establishing reference currents and bias levels.

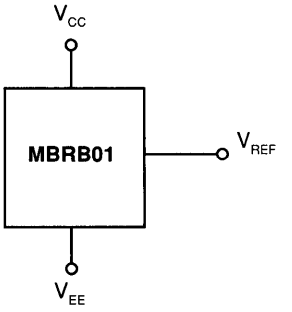
FEATURES

- Low Voltage Operation — Stable With Supply Voltages as Low as 4 Volts
- Extremely Low Component Usage (1/2 Tile)

APPLICATIONS

- General Purpose Reference
- Setting Threshold Levels
- Establishing Supply Voltage Independent Bias Levels

BLOCK DIAGRAM



V_{CC} POSITIVE POWER SUPPLY
V_{EE} NEGATIVE POWER SUPPLY
V_{REF} REFERENCE VOLTAGE OUTPUT

COMPONENT COUNT SUMMARY

COMPONENT TYPE	USAGE			
	SIGNAL PATH		BIAS CIRCUITS	
	A TILES	B TILES	A TILES	B TILES
Tiles (#)	1/2			
Transistors:				
SNPN	6			
SPNP	6			
DBNPN	0			
DBPNP	0			
MNPN	0			
MPNP	0			
HNPN	0			
HPNP	0			
Resistors:				
Nichrome (KΩ)	27.4			
Pinch (#)	6			
Capacitors:				
5 pF (max)	1			
8 pF (max)	0			
18 pF (max)	0			
Buried Zener Diodes	0			

MBRB01 — 1.25V VOLTAGE REFERENCE

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} 35V
Operating Temperature Range ..... $-55°C \leq T_A \leq 125°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq 150°C$

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, specifications apply for V_{EE} = 0V, V_{CC} = 15V, $0°C \leq T_A \leq 70°C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Current, Sinking	$+I_{OUT}$				1	mA
Output Current, Sourcing	$-I_{OUT}$				1	mA
Output Voltage	V_O	T_A = 25°C		1.25		V
V_O Temperature Coefficient	TCV_O	T_A = 25°C, $(\Delta V_O/V_O)/\Delta T$		100	400	ppm/°C
POWER SUPPLY						
Operating Supply Voltage	V_{SUPPLY}	V_{CC} - V_{EE}	4		35	V
Quiescent Current	I_{SUPPLY}	V_{CC} = 15V, I_{OUT} = 0		2		mA
V_O Load Regulation	$\Delta V_O/\Delta I_O$			3	10	mV/MA
V_O Line Regulation	$\Delta V_O/\Delta V_S$	$V_S = V_{CC} - V_{EE}$		5	20	mV/V

Note: Design limits account for process and temperature variations and should be used for worst case design analysis.

2.5V VOLTAGE REFERENCE
SP1000 FAMILY — 35 VOLT PROCESS

DESCRIPTION

The MBRB02 is a voltage reference macro cell featuring a 2.5 Volt output. It is useable with any SP1000 family array product fabricated on Sipex's 35 Volt process. The basic reference element is a "BAND-GAP" with first order temperature compensation. To achieve optimum temperature performance, the MBRB02 employs NiCr resistors with appropriate matching to minimize temperature effects.

The MBRB02 is one tile and is designed for low temperature drift (i.e. 55 ppm/°C typical). The design of MBRB02 is identical to the MBRB05 with the exception of different resistor scaling in the output which is required for 2.5V. The MBRB02 can be used with supply voltages as low as 7 Volts, operates over the full mil-temperature range, and can source 5 mA of output current.

Applications for the MBRB02 include setting threshold levels and establishing reference currents and bias levels, etc.

This macro cell has only been simulated and is not available as a kit part.

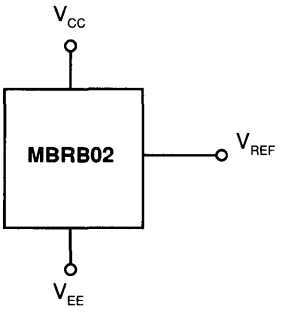
FEATURES

- Both Output Voltage and Temperature Coefficient Can Be Laser Trimmed for Improved Accuracy and Reduced Temperature Drift
- Low Temperature Drift (50 ppm/°C Untrimmed)
- Low Quiescent Current (0.5 mA)
- Moderate Component Count (1 Tile)

APPLICATIONS

- General Purpose Reference
- Setting Threshold Levels
- Establishing Supply Voltage Independent Bias Levels
- Establishing Reference Current

BLOCK DIAGRAM



V_{CC} POSITIVE POWER SUPPLY
V_{EE} NEGATIVE POWER SUPPLY
V_{REF} REFERENCE VOLTAGE OUTPUT

COMPONENT COUNT SUMMARY

COMPONENT TYPE	USAGE			
	SIGNAL PATH		BIAS CIRCUITS	
	A TILES	B TILES	A TILES	B TILES
Tiles (#)		1		
Transistors:				
SNPN		12		
SPNP		4		
DBNPN		0		
DBPNP		0		
MNPN		0		
MPNP		0		
HNPN		0		
HPNP		0		
Resistors:				
Nichrome (KΩ)		16		
Pinch (#)		5		
Capacitors:				
5 pF (max)		0		
8 pF (max)		1		
18 pF (max)		0		
Buried Zener Diodes		0		

MBRB02 — 2.5V VOLTAGE REFERENCE

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} 35V
Operating Temperature Range ..... -55°C ≤ T_A ≤ 125°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ 150°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, specifications apply for V_{EE} = 0V, V_{CC} = 15V, 55°C ≤ T_A ≤ 125°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Current, Sinking	$+I_{OUT}$			0.25		mA
Output Current, Sourcing	$-I_{OUT}$			5		mA
Output Voltage	V_O	T_A = 25°C		2.5		V
V_O Temperature Coefficient	TCV_O	@T_A = 25°C		50	150	ppm/°C
POWER SUPPLY						
Operating Supply Voltage	V_{SUPPLY}	V_{CC} - V_{EE}	7		35	V
V_O Line Regulation	$\Delta V_O/\Delta V_S$			5	20	mV/V
Quiescent Current	I_{SUPPLY}	V_{CC} = 15V, I_{OUT} = 0		0.5		mA
V_O Load Regulation	$\Delta V_O/\Delta I_O$			1	10	mV/mA

Note: Design limits account for process and temperature variations and should be used for worst case design analysis.

5.0V VOLTAGE REFERENCE
SP1000 FAMILY — 35 VOLT PROCESS

DESCRIPTION

The MBRB05 is a voltage reference macro cell featuring a 5.0 Volt output. It is useable with any SP1000 family array product fabricated on Sipex's 35 Volt process. The basic reference element is a "BAND-GAP" with first order temperature compensation. To achieve optimum temperature performance, the MBRB05 employs NiCr resistors with appropriate matching to minimize temperature effects.

The MBRB05 fits in one tile and is designed for low temperature drift (i.e. 50 ppm/°C typical). The MBRB05 can be trimmed both for output voltage and reduced temperature coefficient; operates over the full mil-temperature range; and can source 5 mA of output current.

Applications for the MBRB05 include setting threshold levels, establishing reference currents and bias levels.

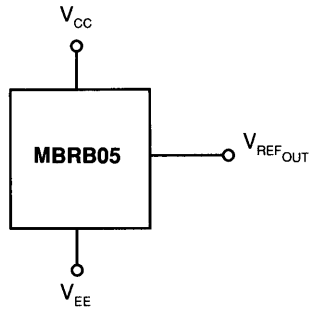
FEATURES

- Both Output Voltage and Temperature Coefficient Can Be Laser Trimmed for Improved Accuracy and Reduced Temperature Drift
- Low Temperature Drift (50 ppm/°C Untrimmed)
- Low Quiescent Current (0.5 mA)
- Moderate Component Count (1 Tile)

APPLICATIONS

- General Purpose Reference
- Setting Threshold Levels
- Establishing Supply Voltage Independent Bias Levels
- Establishing Reference Currents

BLOCK DIAGRAM



COMPONENT COUNT SUMMARY

COMPONENT TYPE	USAGE			
	SIGNAL PATH		BIAS CIRCUITS	
	A TILES	B TILES	A TILES	B TILES
Tiles (#)		1		
Transistors:				
SNPN		12		
SPNP		4		
DBNPN		0		
DBPNP		0		
MNPN		0		
MPNP		0		
HNPN		0		
HPNP		0		
Resistors:				
Nichrome (KΩ)		25.1		
Pinch (#)		5		
Capacitors:				
5 pF (max)		0		
8 pF (max)		1		
18 pF (max)		0		
Buried Zener Diodes		0		

MBRB05 — 5.0V VOLTAGE REFERENCE

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} 35V
Operating Temperature Range ..... $0°C \leq T_A \leq 70°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq 150°C$

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, specifications apply for V_{EE} = 0V, V_{CC} = 12V, $55°C \leq T_A \leq 125°C$.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Current, Sinking	$+I_{OUT}$			0.25		mA
Output Current, Sourcing	$-I_{OUT}$			5		mA
Output Voltage	V_O	T_A = 25°C	4.7	5.0	5.3	V
V_O Temperature Coefficient	TCV_O	T_A = 25°C		50	150	ppm/°C
POWER SUPPLY						
Operating Supply Voltage	V_{SUPPLY}	V_{CC} - V_{EE}	8*		35	V
Quiescent Current	I_{SUPPLY}	V_{CC} = 15V, I_{OUT} = 0		0.5		mA
V_O Load Regulation	$\Delta V_O/\Delta I_O$			1	6*	mV/mA
V_O Line Regulation	$\Delta V_O/\Delta V_S$			5	20	mV/V

Note: Design limits account for process and temperature variations and should be used for worst case design analysis.

*Variations for 20V process

— Operating Supply Voltage V_S = 8V min
— V_O Load Regulation $\Delta V_O/\Delta I_O$ = 5 mV/mA max

10.0V VOLTAGE REFERENCE
SP1000 FAMILY — 35 VOLT PROCESS

DESCRIPTION

The MBRB10 is a voltage reference macro cell featuring a 10 Volt output. It is useable with any SP1000 family array product fabricated on Sipex's 35 Volt process. The basic reference element is a "BAND-GAP" with first order temperature compensation. To achieve optimum temperature performance, the MBRB10 employs NiCr resistors with appropriate matching to minimize temperature effects.

The MBRB10 fits in one tile and is designed for low temperature drift (i.e. 50 ppm/°C). The design of the MBRB10 is identical to the MBRB05, with the exception of the different resistors scaling in the output which is required to achieve 10 volts. The MBRB10 can be trimmed, both for output voltage and reduced temperature coefficient; operates over the full mil-temperature range; and can source 5 mA of output current.

Applications for the MBRB10 include setting threshold levels and establishing reference currents and bias levels, etc.

This macro cell has only been simulated and is not available as a kit part.

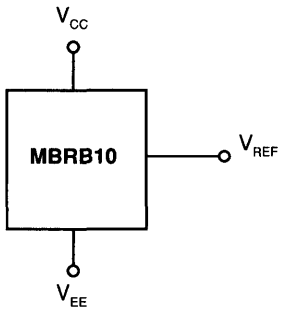
FEATURES

- Both Output Voltage and Temperature Coefficient Can Be Laser Trimmed for Improved Accuracy and Reduced Temperature Drift
- Low Temperature Drift (50 ppm/°C Untrimmed)
- Low Quiescent Current (0.5 mA)
- Moderate Component Count (1 Tile)

APPLICATIONS

- General Purpose Reference
- Setting Threshold Levels
- Establishing Supply Voltage Independent Bias Levels
- Establishing Reference Currents

BLOCK DIAGRAM



V_{CC} POSITIVE POWER SUPPLY
V_{EE} NEGATIVE POWER SUPPLY
V_{REF} REFERENCE VOLTAGE OUTPUT

COMPONENT COUNT SUMMARY

COMPONENT TYPE	USAGE			
	SIGNAL PATH		BIAS CIRCUITS	
	A TILES	B TILES	A TILES	B TILES
Tiles (#)		1		
Transistors:				
SNPN		12		
SPNP		4		
DBNPN		0		
DBPNP		0		
MNPN		0		
MPNP		0		
HNPN		0		
HPNP		0		
Resistors:				
Nichrome (KΩ)		41.4		
Pinch (#)		5		
Capacitors:				
5 pF (max)		0		
8 pF (max)		1		
18 pF (max)		0		
Buried Zener Diodes		0		

MBRB10 — 10.0V VOLTAGE REFERENCE

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} 35V
Operating Temperature Range ..... $0°C \leq T_A \leq 70°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq 150°C$

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, specifications apply for V_{EE} = 0V, V_{CC} = 15V, T_A = 25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Current, Sinking	$+I_{OUT}$			0.25		mA
Output Current, Sourcing	$-I_{OUT}$			5		mA
Output Voltage	V_O	T_A = 25°C		10		V
V_O Temperature Coefficient	TCV_O	T_A = 25°C		50	150	ppm/°C
POWER SUPPLY						
Operating Supply Voltage	V_{SUPPLY}	V_{CC} - V_{EE}	14		35	V
V_O Load Regulation	$\Delta V_O/\Delta I_O$			1	10	mV/mA
V_O Line Regulation	$\Delta V_O/\Delta V_S$			5	20	mV/V
Quiescent Current	I_{SUPPLY}	V_{CC} = 15V, I_{OUT} = 0		0.5		mA

Note: Design limits account for process and temperature variations and should be used for worst case design analysis.

GENERAL PURPOSE WIDEBAND OP-AMP
SP1000 FAMILY — 35 VOLT PROCESS

DESCRIPTION

The MBOP01 is a general purpose op-amp macro cell useable with any SP1000 family array product implemented on Sipex's 35 Volt process. Although it is the lowest performance op-amp in the SP1000 family library, the MBOP01 offers considerable higher performance than typical, off-the-shelf, general purpose op-amps.

The MBOP01 design employs base current cancellation techniques in order to optimize DC performance. Key features include low initial offset voltage (<1 mV), high bandwidth (25 MHz), and unity gain stable operation.

The MBOP01 has a very low component usage for an op-amp — one tile for signal path and bias circuitry. Bandwidth and slew-rate of the MBOP01 can be enhanced by increasing the operating current levels. This is accomplished by connecting the appropriate R_{SET} resistor between the I_{SET} pin and V_{EE}.

For SP1000 family general purpose op-amp applications, the low component count of the MBOP01 always makes it the preferred macro if its performance is adequate for the application.

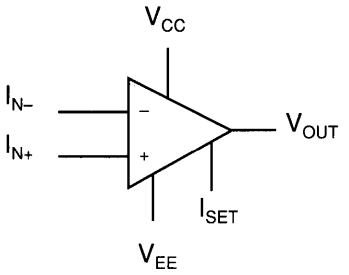
FEATURES

- Low Offset Voltage (0.5 mV Typical)
- Internally Compensated for Stable Operation at Unity Gain
- 25 MHz Unity Gain Bandwidth
- 10 V/µsec Slew Rate
- Power/Bandwidth Programmable

APPLICATIONS

- General Purpose Op-Amp Applications Internal to the Array

BLOCK DIAGRAM



V_{CC}	POSITIVE POWER SUPPLY
V_{EE}	NEGATIVE POWER SUPPLY
I_{N-}	INVERTING INPUT
I_{N+}	NON-INVERTING INPUT
I_{SET}	CIRCUIT BIAS CURRENT SETTING
V_{REF}	REFERENCE VOLTAGE OUTPUT

COMPONENT COUNT SUMMARY

COMPONENT TYPE	USAGE			
	SIGNAL PATH		BIAS CIRCUITS	
	A TILES	B TILES	A TILES	B TILES
Tiles (#)		1		
Transistors:				
SNPN		11		
SPNP		10		
DBNPN		2		
DBPNP		0		
MNPN		0		
MPNP		0		
HNPN		0		
HPNP		0		
Resistors:				
Nichrome (KΩ)		28		
Pinch (#)		6		
Capacitors:				
5 pF (max)		0		
8 pF (max)		0		
18 pF (max)		1		
Buried Zener Diodes		1		

MBOP01 — GENERAL PURPOSE WIDEBAND OP-AMP

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} 35V
Differential Input Voltage, V_D 7V
Input Voltage Range ..... V_{EE} -0.3V to V_{CC} +0.3V
Storage Temperature Range ..... -65°C ≤ T_A ≤ 150°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, specifications apply for T_A = 25°C, R_{SET} = 10 KΩ, V_{CC} = +15V, V_{EE} = -15V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			0.5	5	mV
Temp Coef. of Input Offset Voltage	TC_{VOS}			10		µV/°C
Input Offset Current	I_{OS}			200		nA
Input Bias Current	I_B			.5	1	µA
TRANSFER CHARACTERISTICS						
Common Mode Range	V_{CM}		V_{EE}+3.5		V_{CC}-3.5	V
Common Mode Rejection Ratio	CMRR		80	90		dB
Open Loop Gain	A_V	R_L = 10K to GND	60	72		dB
Phase Margin	PM	C_L = 1 pF, R_L = 10K		60		Deg
Gain Bandwidth Product	GBWP	C_L = 1 pF, R_L = 10K		25		MHz
OUTPUT CHARACTERISTICS						
Output Sink Current	I_{OUT}			0.4		mA
Output Source Current	I_{OUT}			5		mA
Peak Positive Output Voltage	V_O+	R_L = 100K to GND		V_{CC}-2V		V
Peak Negative Output Voltage	V_O-	R_L = 100K to GND		V_{EE}+2		V
TRANSIENT RESPONSE						
Slew Rate Rising	SR+	C_L = 1 pF, R_L = 10K	5	10		V/µS
Slew Rate Falling	SR-	C_L = 1 pF, R_L = 10K	5	10		V/µS
POWER SUPPLY						
Supply Voltage Range	V_{SUPPLY}	V_{CC} - V_{EE}	10		35	V
Supply Current	I_{SUPPLY}	R_{SET} = 10K		1.6		mA
Power Supply Rejection Ratio	PSRR		80	90		dB

Note: Design limits account for process and temperature variations and should be used for worst case design analysis.

HIGH OUTPUT CURRENT, WIDEBAND OP-AMP
SP1000 FAMILY — 35 VOLT PROCESS

DESCRIPTION

The MBOP02 is a general purpose op-amp macro cell useable with any SP1000 family array product implemented on Sipex's 35 Volt process. The MBOP02 is identical in design to the MBOP01 with the exception of its improved class AB emitter follower output stage.

Compared to the MBOP01 design, the MBOP02 offers higher open loop gain, symmetrical 10 V/µsec slew rates, and higher output current source and sink capability. The MBOP02 does, however, have higher component usage and draws slightly higher power than the MBOP01.

Layout of the MBOP02 can be accomplished in one tile, including the bias circuitry. Bandwidth and slew rate of the MBOP02 can be enhanced by increasing the operating current levels. This is accomplished by connecting the appropriate R_{SET} resistor between the I_{SET} pin and V_{EE}.

This macro cell has only been simulated and is not available as a kit part.

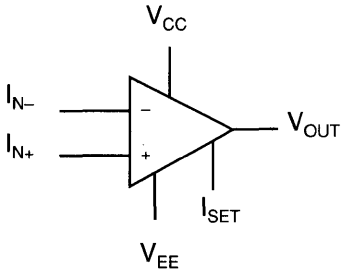
FEATURES

- Low Offset Voltage (0.5 mV Typical)
- Internally Compensated for Stable Operation at Unity Gain
- 25 MHz Unity Gain Bandwidth
- Symmetrical 10 V/µsec Slew Rate
- 20 mA Output Current Source & Sink Capability

APPLICATIONS

- General Purpose Op-Amp
- High Output Current Applications

BLOCK DIAGRAM



V_{CC}	POSITIVE POWER SUPPLY
V_{EE}	NEGATIVE POWER SUPPLY
I_{N-}	INVERTING INPUT
I_{N+}	NON-INVERTING INPUT
I_{SET}	CIRCUIT BIAS CURRENT SETTING
V_{OUT}	OUTPUT

COMPONENT COUNT SUMMARY

COMPONENT TYPE	USAGE			
	SIGNAL PATH		BIAS CIRCUITS	
	A TILES	B TILES	A TILES	B TILES
Tiles (#)		1		
Transistors:				
SNPN		12		
SPNP		12		
DBNPN		4		
DBPNP		1		
MNPN		1		
MPNP		1		
HNPN		0		
HPNP		0		
Resistors:				
Nichrome (KΩ)		28		
Pinch (#)		6		
Capacitors:				
5 pF (max)		0		
8 pF (max)		0		
18 pF (max)		1		
Buried Zener Diodes		1		

MBOP02 — HIGH OUTPUT CURRENT, WIDEBAND OP-AMP

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} 35V
Differential Input Voltage 7V
Input Voltage Range ..... V_{EE} -0.3V to V_{CC} +0.3V
Storage Temperature Range ..... -65°C ≤ T_A ≤ 150°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, specifications apply for T_A = 25°C, R_{SET} = 10 KΩ, V_{CC} = +15V, V_{EE} = -15V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			.5	5	mV
Temp Coef. of Input Offset Voltage	TC_{VOS}			10		µV/°C
Input Offset Current	I_{OS}			200		nA
Input Bias Current	I_B			.5	1	µA
TRANSFER CHARACTERISTICS						
Common Mode Range	V_{CM}		V_{EE}+3.5		V_{CC}-3.5	V
Common Mode Rejection Ratio	CMRR		80	90		dB
Open Loop Gain	A_V	R_L = 10K to GND	80	92		dB
Phase Margin	PM	C_L = 1 pF, R_L = 10K		60		Deg
Gain Bandwidth Product	GBWP	C_L = 1 pF, R_L = 10K		25		MHz
OUTPUT CHARACTERISTICS						
Output Sink Current	I_{OUT}			20		mA
Output Source Current	I_{OUT}			20		mA
Peak Positive Output Voltage	V_O+	R_L = 100K to GND		V_{CC}-3.5		V
Peak Negative Output Voltage	V_O-	R_L = 100K to GND		V_{EE}+4		V
TRANSIENT RESPONSE						
Slew Rate Rising	SR+	C_L = 1 pF, R_L = 10K	5	10		V/µS
Slew Rate Falling	SR-	C_L = 1 pF, R_L = 10K	5	10		V/µS
POWER SUPPLY						
Supply Voltage Range	V_{SUPPLY}	V_{CC} - V_{EE}	10		20	V
Supply Current	I_{SUPPLY}	R_{SET} = 10K		2.5		mA
Power Supply Rejection Ratio	PSRR		80	90		dB

Note: Design limits account for process and temperature variations and should be used for worst case design analysis.

HIGH PERFORMANCE OP-AMP
SP1000 FAMILY — 35 VOLT PROCESS

DESCRIPTION

The MBOP03 is a high performance single gain stage Op-Amp useable with any SP1000 family product implemented with Sipex's 35 Volt process. The design employs both input bias current and HOB cancellation to simultaneously achieve superior DC and AC characteristics.

The MBOP03 is the highest precision Op-Amp in the SP1000 macro cell library. As with the other op-amps in the library, bandwidth and slew rate of the MBOP03 can be enhanced by increasing the operating current level. This is accomplished by connecting the appropriate R_{SET} resistor between the I_{SET} pin and V_{EE}.

Key performance characteristics of the MBOP03 include high open loop gain, low input offset current, high bandwidth, a symmetrical slew rate of 10 V/µsec and unity gain stable operation. The MBOP03 is designed to allow laser trimming of the offset voltage. V_{OS} of 100 µ volts is achievable.

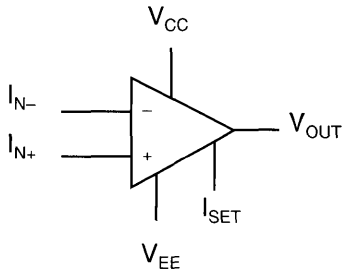
FEATURES

- Trimmable Offset Voltage (Down to V_{OS} ≤100 µV)
- High Open Loop Gain (A_{VOL} = 120 dB Typical)
- High Slew Rate (10 V/µsec Typical)
- Compensated for Unity Gain Stable Operation
- 50 MHz Gain Bandwidth

APPLICATIONS

- Precision Op-Amp Usage

BLOCK DIAGRAM



V_{CC}	POSITIVE POWER SUPPLY
V_{EE}	NEGATIVE POWER SUPPLY
I_{N-}	INVERTING INPUT
I_{N+}	NON-INVERTING INPUT
I_{SET}	CIRCUIT BIAS CURRENT SETTING
V_{OUT}	OUTPUT

COMPONENT COUNT SUMMARY

COMPONENT TYPE	USAGE			
	SIGNAL PATH		BIAS CIRCUITS	
	A TILES	B TILES	A TILES	B TILES
Tiles (#)	1	1		1/2
Transistors:				
SNPN	12	12		2
SPNP	11	6		8
DBNPN	1	0		1
DBPNP	1	0		0
MNPN	1	0		0
MPNP	1	0		0
HNPN	0	0		0
HPNP	0	0		0
Resistors:				
Nichrome (KΩ)	19	12		
Pinch (#)	0	0		6
Capacitors:				
5 pF (max)	0	0		0
8 pF (max)	1	0		0
18 pF (max)	0	0		0
Buried Zener Diodes	0	0		1

MBOP03 — HIGH PERFORMANCE OP-AMP

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} 35V
Differential Input Voltage 7V
Input Voltage Range ..... V_{EE} -0.3V to V_{CC} +0.3V
Storage Temperature Range ..... -65°C ≤ T_A ≤ 150°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, specifications apply for T_A = 25°C, R_{SET} = 18 KΩ, V_{CC} = +15V, V_{EE} = 15V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}	Untrimmed		1	5	mV
Temp Coef. of Input Offset Voltage	TC_{VOS}			10		µV/°C
Input Offset Current	I_{OS}			10	50	nA
Input Bias Current	I_B			50	200	nA
TRANSFER CHARACTERISTICS						
Common Mode Range	V_{CM}		V_{EE}+4		V_{CC}-4	V
Common Mode Rejection Ratio	CMRR		70	110		dB
Open Loop Gain	A_{VOL}	R_L = 10K to GND		120		dB
Phase Margin	PM	C_L = 1 pF, R_L = 10K		60		Deg
Gain Bandwidth Product	GBWP	C_L = 1 pF, R_L = 10K		15*		MHz
OUTPUT CHARACTERISTICS						
Output Source Current	I_{OUT}		5	20		mA
Output Sink Current	I_{OUT}		5	20		mA
Peak Positive Output Voltage	V_O+	R_L = 100K to GND		V_{CC}-4		V
Peak Negative Output Voltage	V_O-	R_L = 100K to GND		V_{EE}+4		V
TRANSIENT RESPONSE						
Slew Rate Rising	SR+	C_L = 1 pF, R_L = 10K		10		V/µS
Slew Rate Falling	SR-	C_L = 1 pF, R_L = 10K		10		V/µS
POWER SUPPLY						
Supply Current	I_{SUPPLY}	R_{SET} = 18K, No Load		2.5		mA
Power Supply Rejection Ratio	PSRR		80	90		dB
Supply Voltage Range	V_{SUPPLY}	V_{CC} - V_{EE}	10		35	V

Note: Design limits account for process and temperature variations and should be used for worst case design analysis.

*Variations for 20 V process

— Gain Bandwidth Product GBWP = 20 MHz max

TRANSIMPEDANCE AMPLIFIER
SP1000 FAMILY — 35 VOLT PROCESS

DESCRIPTION

The MBTA01 is a transimpedance amplifier macro cell useable on the SP1104 array implemented with Sipex's 35 Volt process. The MBTA01 utilizes 2 tiles as well as HNPN and HPNP devices which allow it to supply high output currents (100 mA).

As a current to voltage transimpedance amplifier, the MBTA01 exhibits relatively flat gain vs. frequency performance as well as excellent slew rate and settling characteristics. Since slew rate is a function of the voltage difference at the input terminals, a more exponential type settling characteristic is achieved. As a result, overshoot and settling time, compared to conventional op-amps, is greatly reduced. The MBTA01 also exhibits excellent phase margin and stability.

The MBTA01 employs current mode feedback to achieve its relatively large bandwidth. A 1 KΩ feedback resistor connected between V_{OUT} and IN+ is required for proper operation. The bias current, power consumption, slew rate, and bandwidth can be programmed by connecting the appropriate R_{SET} resistor between I_{SET} and GND.

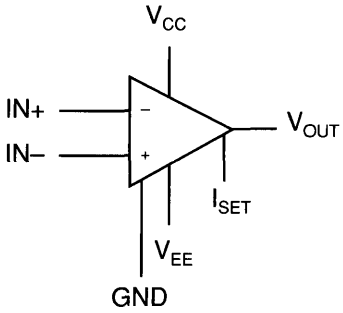
FEATURES

- 100 V/mA Transimpedance
- Very High Slew Rate (400 V/µsec)
- High Output Current Drive (±100 mA)
- Fast Settling (70 nsec to 1%)
- 10 MHz 3 dB Bandwidth

APPLICATIONS

- High Speed Current to Voltage Conversion
- Video Amplifier
- Precision Buffer
- Automatic Test Equipment
- Pulse Amplifier

BLOCK DIAGRAM



V_{CC}	POSITIVE POWER SUPPLY
V_{EE}	NEGATIVE POWER SUPPLY
IN+	INPUT (POSITIVE)
IN–	INPUT (NEGATIVE)
V_{OUT}	OUTPUT
I_{SET}	CURRENT SET
GND	GROUND

COMPONENT COUNT SUMMARY

COMPONENT TYPE	USAGE			
	SIGNAL PATH		BIAS CIRCUITS	
	A TILES	B TILES	A TILES	B TILES
Tiles (#)	1		1	
Transistors:				
SNPN	11		9	
SPNP	11		11	
DBNPN	2		2	
DBPNP	2		2	
MNPN	1		0	
MPNP	1		0	
HNPN	0		0	
HPNP	11		0	
Resistors:				
Nichrome (KΩ)	57.8		22.6	
Pinch (#)	0		0	
Capacitors:				
5 pF (max)	2		0	
8 pF (max)	0		0	
18 pF (max)	0		0	
Buried Zener Diodes	0		0	

MBTA01 — TRANSIMPEDANCE AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} 35V
Operating Temperature Range ..... 0°C ≤ T_A ≤ 70°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ 150°C
Input Voltage ..... ±5V
Peak Output Current ..... Output Limited
Inverting Input Current ..... ±5 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, specifications apply for T_A = 25°C, R_{SET} = 24.8 KΩ, V_{CC} = +15V, V_{EE} = -15V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Bias Current	$+I_B$			1		µA
Input Bias Current	$-I_B$			20		µA
TRANSFER CHARACTERISTICS						
Bandwidth (3 dB)	BW	R_L = 1KΩ, A_V = 1, R_F = 1K		10		MHz
Common Mode Rejection Ratio	CMRR			60		dB
Open Loop Gain	A_V			40		dB
Transimpedance	R_{OL}	R_L = 1KΩ		100		V/mA
Phase Margin	VP	f = 10 MHz, C_L = 50 pf		80		Deg
OUTPUT CHARACTERISTICS						
Output Source Current	I_{OUT}			100		mA
Output Sink Current	I_{OUT}			100		mA
Output Voltage Swing	V_O	R_L = 1 KΩ	V_{EE}+5		V_{CC}-5	V
TRANSIENT RESPONSE						
Slew Rate	S_R	C_L = 200 pF, R_L = 1 KΩ		400		V/µs
Rise Time	T_R	R_L = 150Ω, A_V = 1, R_F = 1K		35		ns
Fall Time	T_F	R_L = 150Ω, A_V = 1, R_F = 1K		35		ns
1% Settling Time	T_S	R_L = 150Ω, A_V = 1, R_F = 1K (Note 1)		70		ns
Propagation Delay	T_P	R_L = 150Ω, A_V = 1, R_F = 1K		20		ns
POWER SUPPLY						
Quiescent Current	I_{SUPPLY}	I_{OUT} = 0		11		mA
Power Supply Rejection Ratio	PSRR			75		dB
Supply Voltage Range	V_{SUPPLY}	V_{CC} - V_{EE}	12		35	V

Notes: 1. 10% to 1% of final value.
2. Design limits account for process and temperature variations and should be used for worst case design analysis.
3. Note this macro cell is not available on the SP1204 array.

HIGH SPEED COMPARATOR
SP1000 FAMILY — 35 VOLT PROCESS

DESCRIPTION

The MBCM01 is an efficient (less than one tile) quasi-TTL output comparator useable on any SP1000 family product implemented with Sipex's 35 Volt process. The output stage is current limited. Power dissipation and response time can be programmed by adjusting the bias current.

Because of its moderate gain, the MBCM01 is very stable and exhibits excellent AC performance. It is intended for applications with moderate signal levels and can be used in high speed applications (i.e. 30 nsec response time).

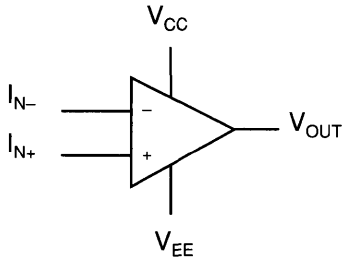
FEATURES

- Single or Dual Supply Operation
- Fast Response Time (30 nsec Typical)
- Very Low Component Usage (Less Than 1 Tile)
- Low Power Dissipation
- High CMRR (90 dB Typical)
- High PSRR (96 dB Typical)

APPLICATIONS

- A/D Conversion
- Threshold/Level Detection

BLOCK DIAGRAM



V_{CC} POSITIVE POWER SUPPLY
V_{EE} NEGATIVE POWER SUPPLY
I_{N-} INVERTING INPUT
I_{N+} NON-INVERTING INPUT
V_{REF} REFERENCE VOLTAGE OUTPUT

COMPONENT COUNT SUMMARY

COMPONENT TYPE	USAGE			
	SIGNAL PATH		BIAS CIRCUITS	
	A TILES	B TILES	A TILES	B TILES
Tiles (#)		1		
Transistors:				
SNPN		12		
SPNP		6		
DBNPN		0		
DBPNP		0		
MNPN		1		
MPNP		0		
HNPN		0		
HPNP		0		
Resistors:				
Nichrome (KΩ)		22		
Pinch (#)		4		
Capacitors:				
5 pF (max)		0		
8 pF (max)		0		
18 pF (max)		0		
Buried Zener Diodes		1		

MBCM01 — HIGH SPEED COMPARATOR

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} 35V
Maximum Differential Input Voltage
Operating Temperature Range ..... $0°C \leq T_A \leq 70°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq 150°C$

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, specifications apply for $0°C \leq T_A \leq 70°C$, V_{CC} = +15V, V_{EE} = 0V.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage	V_{OS}			5	20	mV
Input Bias Current	I_B			1.5		µA
TRANSFER CHARACTERISTICS						
Gain				60		dB
Common Mode Range	V_{CM}		V_{EE}+3		V_{CC}-3	V
Common Mode Rejection Ratio	CMRR		70	90		dB
OUTPUT CHARACTERISTICS						
Output Source Current	$-I_{OUT}$			2		mA
Output Sink Current	$+I_{OUT}$			2		mA
Output Low Voltage	V_{OL}	$+I_{OUT}$ = 1 mA		650		mV
High Output Voltage	V_{OH}			3.75		V
TRANSIENT RESPONSE						
Propagation Delay	T_D			30		nS
POWER SUPPLY						
Supply Current	I_{SUPPLY}	V_{CC} = 15V, I_{OUT} = 0		2		mA
Power Supply Rejection Ratio	PSRR		70	96		dB
Supply Voltage Range	V_{SUPPLY}	V_{CC} - V_{EE}	8		35	V
Max Output Voltage Swing	V_O			5		V

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RS232 LINE DRIVERS/RECEIVERS

MODEL	NO. OF RS232 DRIVERS	NO. OF RS232 RECEIVERS	LOW POWER SHUTDOWN	POWER SUPPLY VOLTAGE	PACKAGE	PAGE
SP230	5	0	Yes	+5V	20-Pin SD	77
SP231	2	2	No	+5V & +7.5V to 13.2V	14-Pin SD	77
SP232	2	2	No	+5V	16-Pin SD	77
SP233	2	2	No	+5V	20-Pin SD	77
SP234	4	0	No	+5V	16-Pin SD	77
SP235	5	5	Yes	+5V	24-Pin DD	77
SP236	4	3	Yes	+5V	24-Pin DD	77
SP237	5	3	No	+5V	24-Pin DD	77
SP238	4	4	No	+5V	24-Pin DD	77
SP239	3	5	Yes	+5V & +7.5V to 13.2V	24-Pin DD	77
SP241	4	5	Yes	+5V	28-Pin DD	77

RS232/422 LINE DRIVERS/RECEIVERS

MODEL	NO. OF RS232 DRIVERS	NO. OF RS422 DRIVERS	NO. OF RS232 RECEIVERS	NO. OF RS422 RECEIVERS	PACKAGE	PAGE
SP301	2	2	2	2	24-Pin SD	89
SP302	4	2	4	2	24-Pin SD	89

Shaded area indicates new product since publication of 1988 catalog

+5V POWERED RS232 DRIVERS/RECEIVERS

FEATURES/BENEFITS

- Operates from Single 5V Power Supply (+5V and +12V - SP231 and SP239)
- Meets All RS232C and V.28 Specifications
- Multiple Drivers and Receivers
- Onboard DC-DC Converters
- ±9V Output Swing with +5V Supply
- Low Power Shutdown ≤1 µA
- 3-State TTL/CMOS Receiver Outputs
- ±30V Receiver Input Levels
- Low Power CMOS: 5 mA Operation

APPLICATIONS

- Computers
- Peripherals
- Modems
- Printers
- Instruments

DESCRIPTION

The SP230 family of RS232 line drivers/receivers from Sipex Corporation provides a variety of configurations to fit most communication needs, especially those applications where ±12V is not available. The SP230 and SP236 feature a low power shutdown mode which reduces power dissipation to less than 5 µW. This is particularly beneficial in battery powered systems. The SP233 and SP235 use no external components and are particularly useful in applications where printed circuit board space is critical.

All of the SP230 family, except SP231 and SP239, include two charge pump voltage converters which allow them to operate from a single +5V supply. These converters convert the +5V input power to the ±10V needed to generate the RS232 output levels. The SP231 and SP239 are designed to operate from a +5V and +12V supplies with the use of an internal +12V to -12V charge pump voltage converter.

Both the drivers and receivers meet all EIA RS232C and CCITT V.28 specifications.

SELECTION TABLE

Part Number	Power Supply Voltage	No. of RS232 Drivers	No. of RS232 Receivers	External Components	Low Power Shutdown	TTL 3-State	No. of Pins
SP230	+5V	5	0	4 Capacitors	Yes	No	20
SP231	+5V & +7.5V to 13.2V	2	2	2 Capacitors	No	No	14
SP232	+5V	2	2	4 Capacitors	No	No	16
SP233	+5V	2	2	None	No	No	20
SP234	+5V	4	0	4 Capacitors	No	No	16
SP235	+5V	5	5	None	Yes	Yes	24
SP236	+5V	4	3	4 Capacitors	Yes	Yes	24
SP237	+5V	5	3	4 Capactiors	No	No	24
SP238	+5V	4	4	4 Capacitors	No	No	24
SP239	+5V & +12V	3	5	2 Capacitors	No	Yes	24
SP241	+5V	4	5	4 Capacitors	Yes	Yes	28

SP230-241

+5V Powered RS232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS*

V_{CC} . . . . . +6V
V+ . . . . . (VCC -0.3V) to +13.2V
V- . . . . . -13.2V
Input Voltages
T_{IN} . . . . . -0.3 to (VCC +0.3V)
R_{IN} . . . . . ±30V
Output Voltages
T_{OUT} . . . . . (V+, +0.3V) to (V-, -0.3V)
R_{OUT} . . . . . -0.3V to (VCC +0.3V)

Short Circuit Duration
T_{OUT} . . . . . Continous
Power Dissipation
CERDIP . . . . . 675 mW
(derate 9.5 m W/ °C above +70° C)
Plastic Dip . . . . . 375 mW
(derate 7 m W/ °C above +70° C)
Small Outline . . . . . 375 mW
(derate 7 m W/ °C above +70° C)

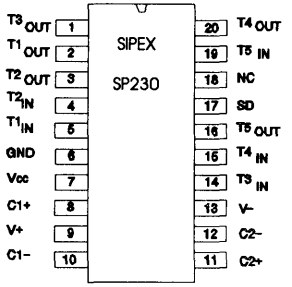
* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

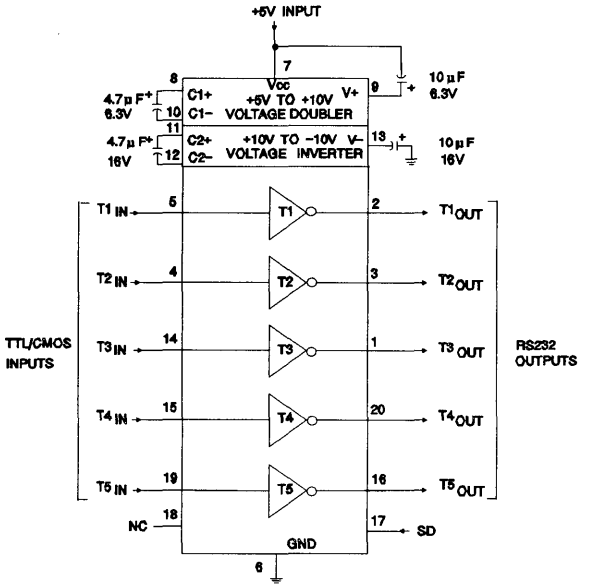
ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±10%, V+ = 7.5V to 13.2V (SP231 only) & V+ =12V ±10% (SP239 Only), T_A = Operating Temp. Range, unless otherwise noted

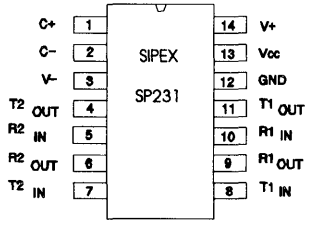
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3 K Ω to Ground	±5	±9		Volts
V cc Power Supply Current	No load, T_A = +25° C		5	10	mA
V+ Power Supply Current	No load, V+ = 12V SP231 & SP239 only		5	10	mA
Shutdown Supply Current	T_A = +25° C		1	10	μA
Input Logic Threshold Low	T_{IN}			0.8	Volts
Input Logic Threshold High	T_{IN}	2.0			Volts
Logic Pullup Current	T_{IN} = 0V		15	200	μA
RS232 Input Voltage Range		-30		+30	Volts
RS232 Input Threshold Low	V_{CC} = 5V, T_A = +25° C	0.8	1.2		Volts
RS232 Input Threshold High	V_{CC} = 5V, T_A = +25° C		1.7	2.4	Volts
RS232 Input Hysteresis	V_{CC} = 5V	0.2	0.5	1.0	Volts
RS232 Input Resistance	T_A = +25° C	3	5	7	K ohms
TLL/CMOS Output Voltage Low	I_{out} = 3.2mA			0.4	Volts
TLL/CMOS Output Voltage High	I_{out} = -1.0mA	3.5			Volts
TLL/CMOS Output Leakage Current	$\overline{EN}$ = V_{CC}, 0 V ≤ R_{out} ≤ V_{CC}		0.05	±10	μA
Output Enable Time	SP235, SP236, SP239		400		nS
Output Disable Time	SP235, SP236, SP239		250		nS
Propagation Delay	RS232 to TTL		0.5		μS
Instantaneous Slew Rate	C_L = 10 pF, R_L = 3-7 K Ω T_A = +25° C			30	V/μS
Transition Region Slew Rate	R_L = 3K Ω, C_L = 2500 pF Measured from +3V to -3V or -3V to +3V		3		V/μS
Output Resistance	V_{CC}= V+ = V- =0V, V_{OUT} = ±2V	300			Ohms
RS232 Output Short Circuit Current			±10		mA

SP230 Typical Operating Circuit

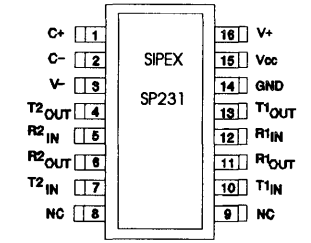




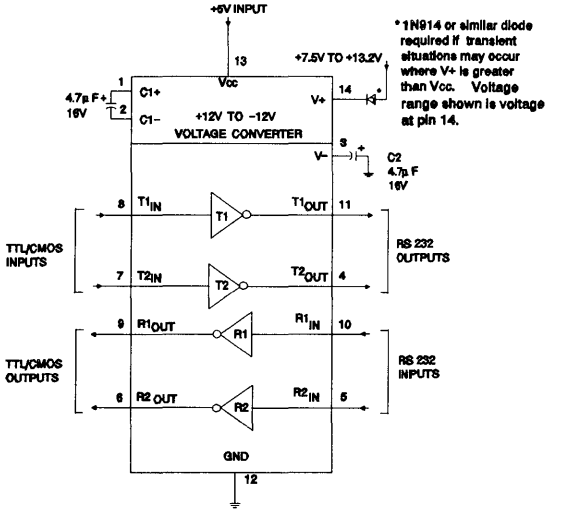
SP231 Typical Operating Circuit



14 Lead Plastic DIP



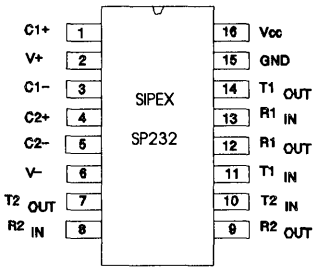
16 Lead Small Outline

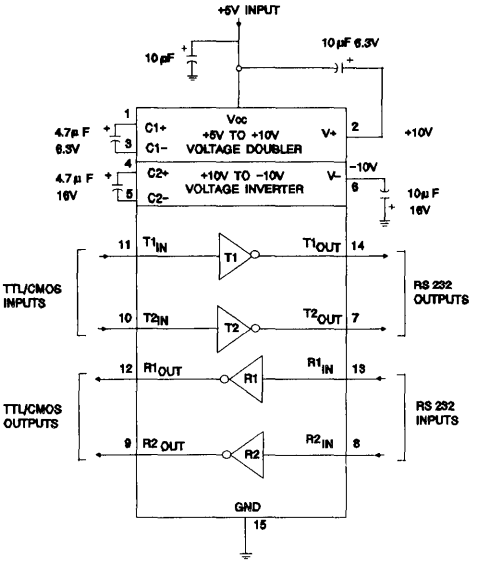


SP230-SP241

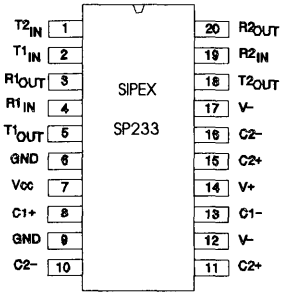
+5V Powered RS232 Drivers/Receivers

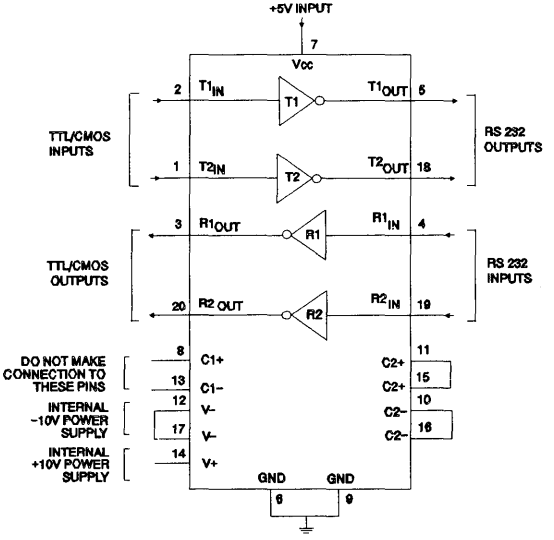
SP232 Typical Operating Circuit



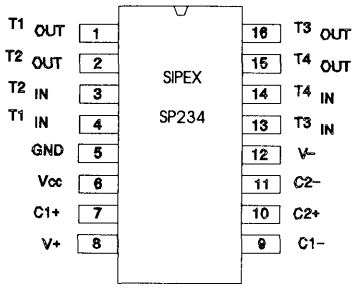


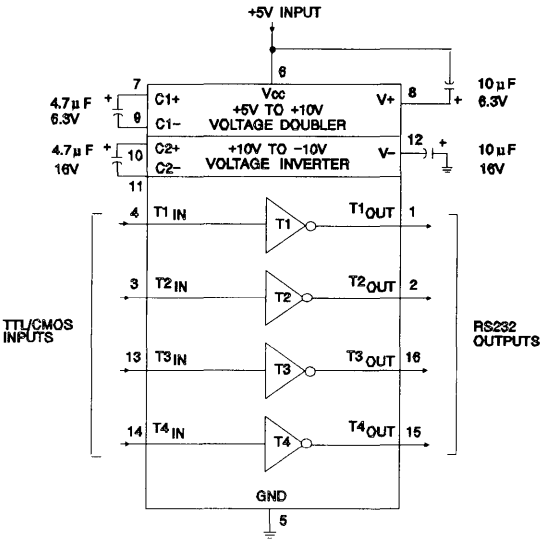
SP233 Typical Operating Circuit



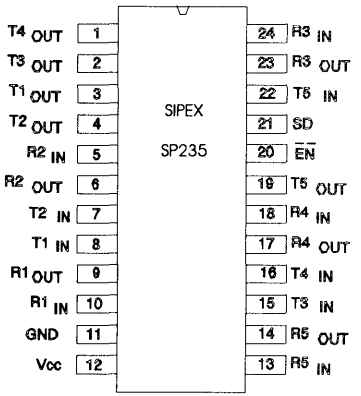


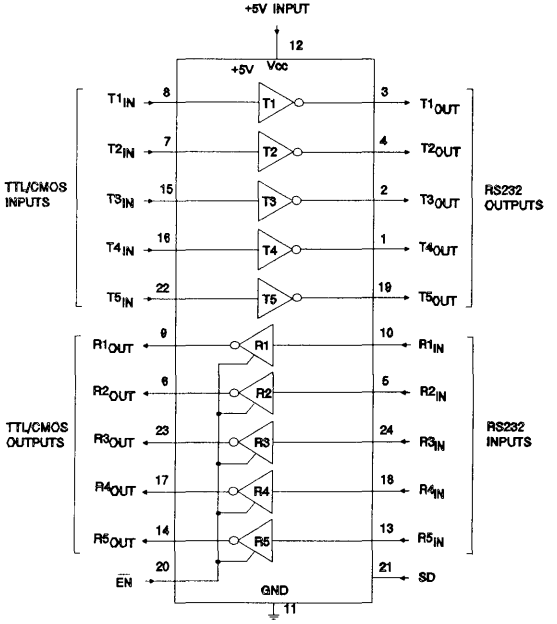
SP234 Typical Operating Circuit



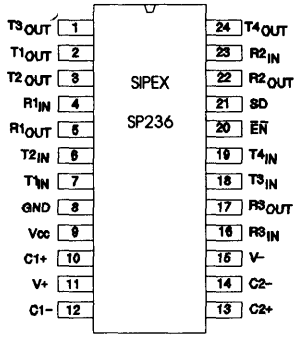


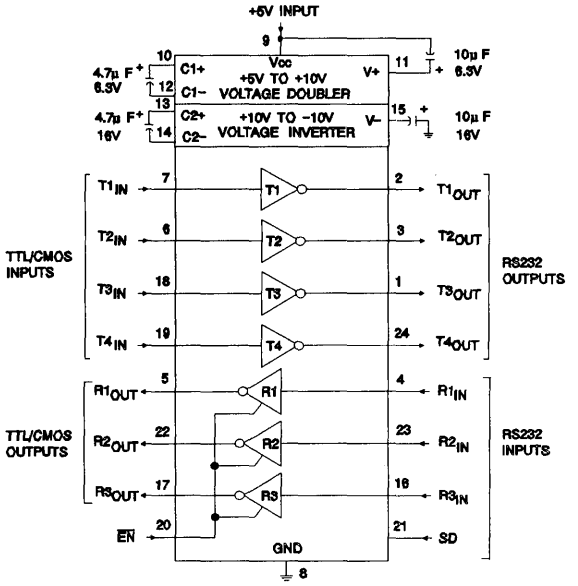
SP235 Typical Operating Circuit



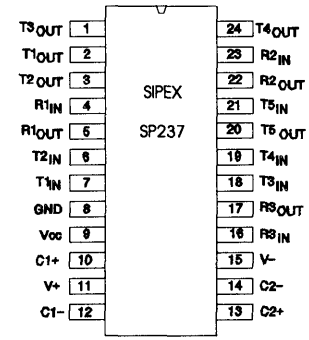


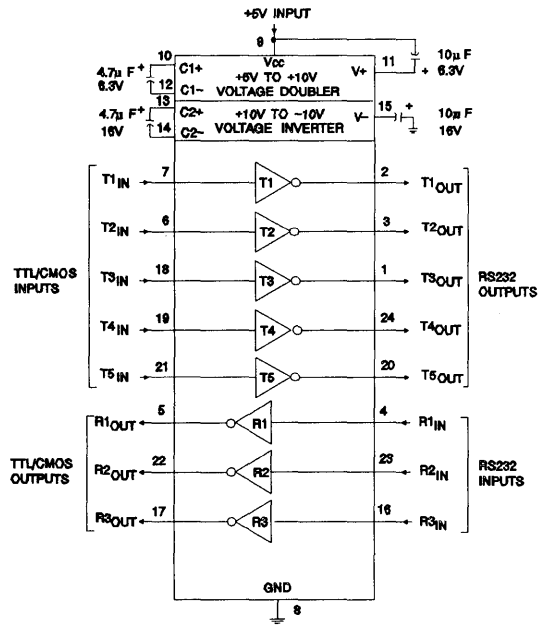
SP236 Typical Operating Circuit



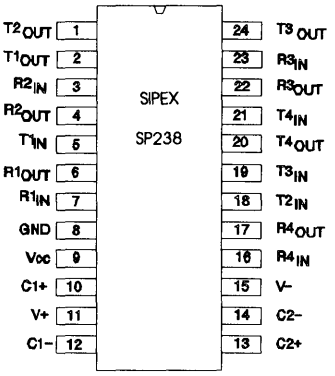


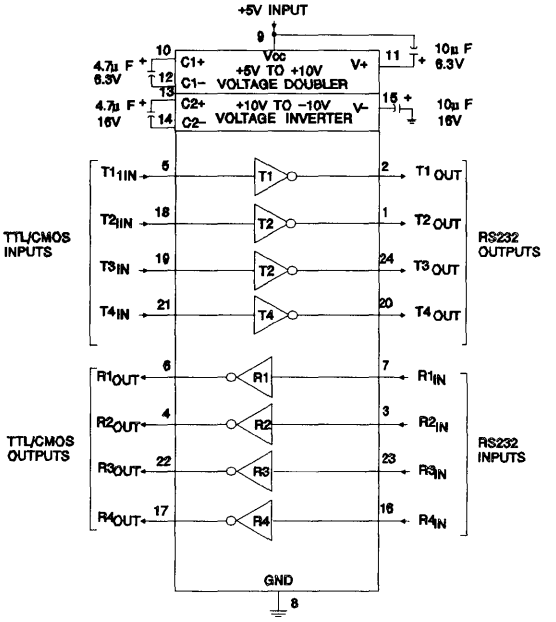
SP237 Typical Operating Circuit



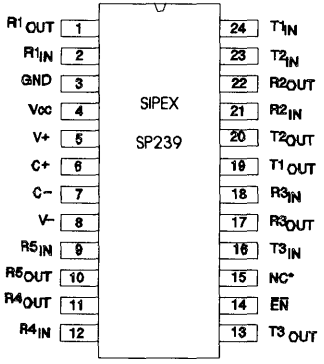


SP238 Typical Operating Circuit

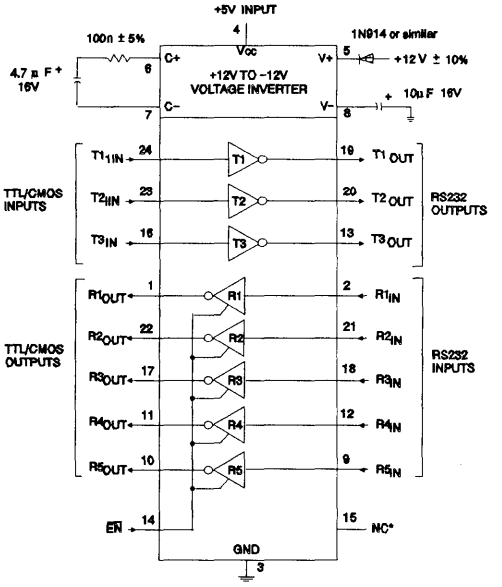




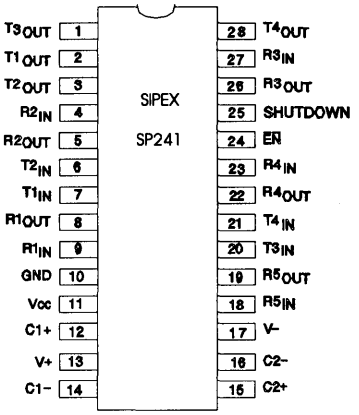
SP239 Typical Operating Circuit

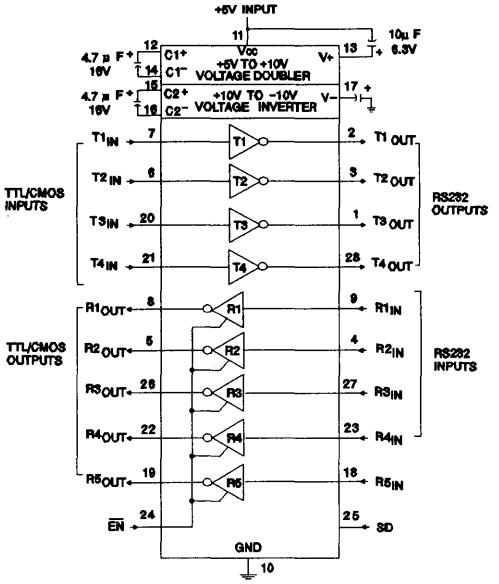


*NC – No Connection



SP241 Typical Operating Circuit

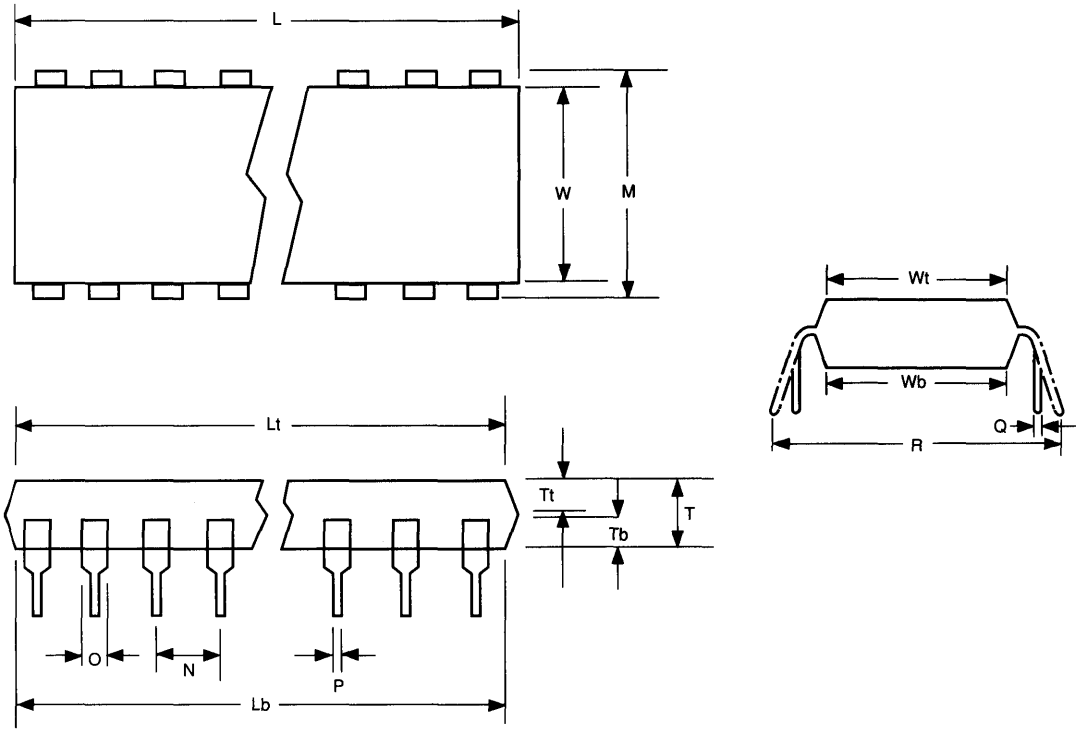




PART	TEMP. RANGE	PACKAGE	PART	TEMP. RANGE	PACKAGE	PART	TEMP. RANGE	PACKAGE
SP230			**SP231**			**SP232**		
SP230CP	0°C to +70°C	20 Lead Plastic DIP	SP231CP	0°C to +70°C	14 Lead Plastic DIP	SP232CP	0°C to +70°C	16 Lead Plastic DIP
SP230CT	0°C to +70°C	20 Lead Small Outline	SP231CT	0°C to +70°C	16 Lead Small Outline	SP232CT	0°C to +70°C	16 Lead Small Outline
SP230CX	0°C to +70°C	Dice	SP231CX	0°C to +70°C	Dice	SP232CX	0°C to +70°C	Dice
SP230EP	-40°C to +85°C	20 Lead Plastic DIP	SP231EP	-40°C to +85°C	14 Lead Plastic DIP	SP232EP	-40°C to +85°C	16 Lead Plastic DIP
SP230ET	-40°C to +85°C	20 Lead Small Outline	SP231ET	-40°C to +85°C	16 Lead Small Outline	SP232ED	-40°C to +85°C	16 Lead CERDIP
SP230ED	-40°C to +85°C	20 Lead CERDIP	SP231ED	-40°C to +85°C	14 Lead CERDIP	SP232ET	-40°C to +85°C	16 Lead Small Outline
			SP231MD	-55°C to +125°C	14 Lead CERDIP	SP232MD	-55°C to +125°C	16 Lead CERDIP
SP233			**SP234**			**SP235**		
SP233CP	0°C to +70°C	20 Lead Plastic DIP	SP234CP	0°C to +70°C	16 Lead Plastic DIP	SP235CP	0°C to +70°C	24 Lead Plastic DIP*
SP233EP	-40°C to +85°C	20 Lead Plastic DIP	SP234CT	0°C to +70°C	16 Lead Small Outline	SP235EP	-40°C to +85°C	24 Lead Plastic DIP*
			SP234CX	0°C to +70°C	Dice	SP235EC	-40°C to +85°C	24 Lead Ceramic*
			SP234EP	-40°C to +85°C	16 Lead Plastic DIP			
			SP234ET	-40°C to +85°C	16 Lead Small Outline			
			SP234ED	-40°C to +85°C	16 Lead CERDIP			
			SP234MD	-55°C to +125°C	16 Lead CERDIP			
SP236			**SP237**			**SP238**		
SP236CS	0°C to +70°C	24 Lead Plastic DIP	SP237CS	0°C to +70°C	24 Lead Plastic DIP	SP238CS	0°C to +70°C	24 Lead Plastic DIP
SP236CT	0°C to +70°C	24 Lead Small Outline	SP237CT	0°C to +70°C	24 Lead Small Outline	SP238CT	0°C to +70°C	24 Lead Small Outline
SP236CX	0°C to +70°C	Dice	SP237CX	0°C to +70°C	Dice	SP238CX	0°C to +70°C	Dice
SP236ES	-40°C to +85°C	24 Lead Plastic DIP	SP237ES	-40°C to +85°C	24 Lead Plastic DIP	SP238ES	-40°C to +85°C	24 Lead Plastic DIP
SP236ET	-40°C to +85°C	24 Lead Small Outline	SP237ET	-40°C to +85°C	24 Lead Small Outline	SP238ET	-40°C to +85°C	24 Lead Small Outline
SP236ER	-40°C to +85°C	24 Lead CERDIP	SP237ER	-40°C to +85°C	24 Lead CERDIP	SP238ER	-40°C to +85°C	24 Lead CERDIP
SP236MR	-55°C to +125°C	24 Lead CERDIP				SP238MR	-55°C to +125°C	24 Lead CERDIP
SP239			**SP241**					
SP239CS	0°C to +70°C	24 Lead Plastic DIP	SP241CT	0°C to +70°C	24 Lead Small Outline			
SP239CT	0°C to +70°C	24 Lead Small Outline	SP241ET	-40°C to +85°C	24 Lead Small Outline			
SP239CX	0°C to +70°C	Dice						
SP239ES	-40°C to +85°C	24 Lead Plastic DIP						
SP239ET	-40°C to +85°C	24 Lead Small Outline						
SP239ER	-40°C to +85°C	24 Lead CERDIP						
SP239MR	-55°C to +125°C	24 Lead CERDIP						

* = 0.600" package, all other packages are 0.300" wide.

PLASTIC DIP PACKAGE OUTLINE



PLASTIC DIP PACKAGE DIMENSIONS (300 MIL)

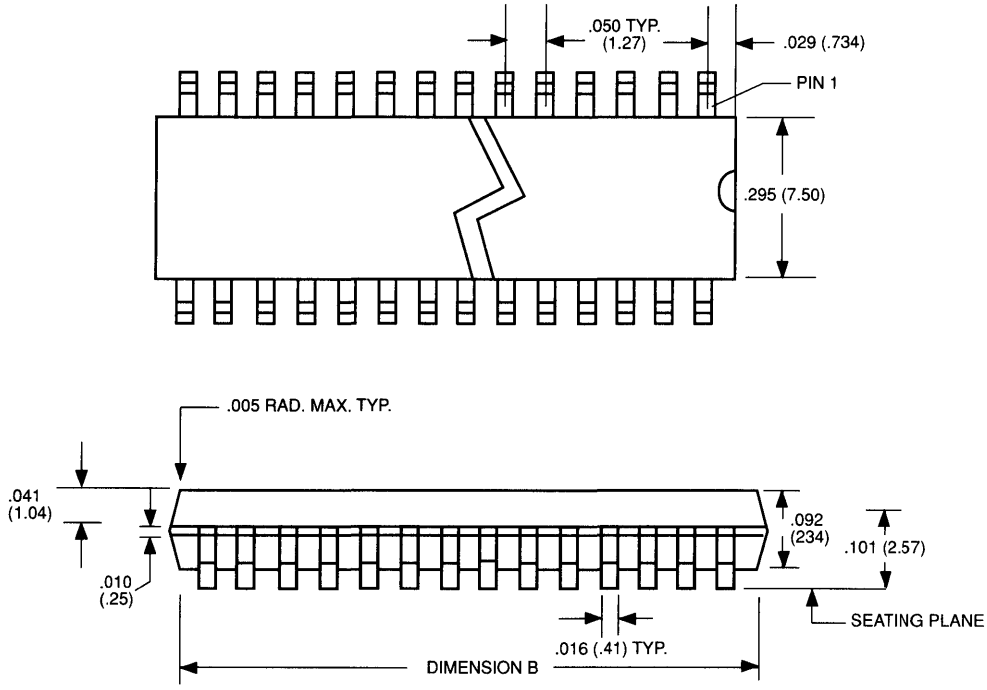
LEAD TYPE	14	16	20	24 SKINNY DIP	24 DOUBLE DIP
W	250	250	260	260	540
Wt	235	235	245	243	525
Wb	235	235	245	243	525
L	750	750	1024	1240	1254
Lt	739	739	1009	1225	1244
Lb	739	739	1009	1225	1244
T	132	132	132	130	150
Tt	61	61	61	60	70
Tb	61	61	61	60	70
M	300-325	300-325	310-325	310-325	600-625
N	100±2	100±2	100±2	100±2	100±2
O	60±2	60±2	60±2	60±2	60±2
P	18±2	18±2	18±2	18±2	18±2
Q	10±.3	10±.3	10±.3	10±.3	10±.3
R	350±25	350±25	350±25	350±25	650±25

NOTE

Package Dimension Tolerance for:

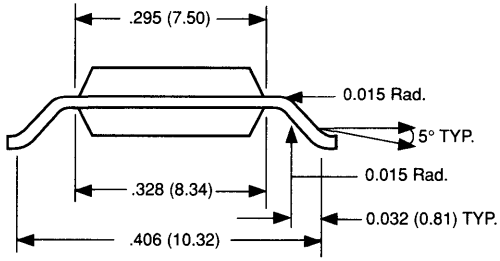
1. Length (L) = ±4 mils
2. Width (W) = ±2 mils
3. Thickness (T) = ±2 mils

SOIC PACKAGE OUTLINE



NOTE

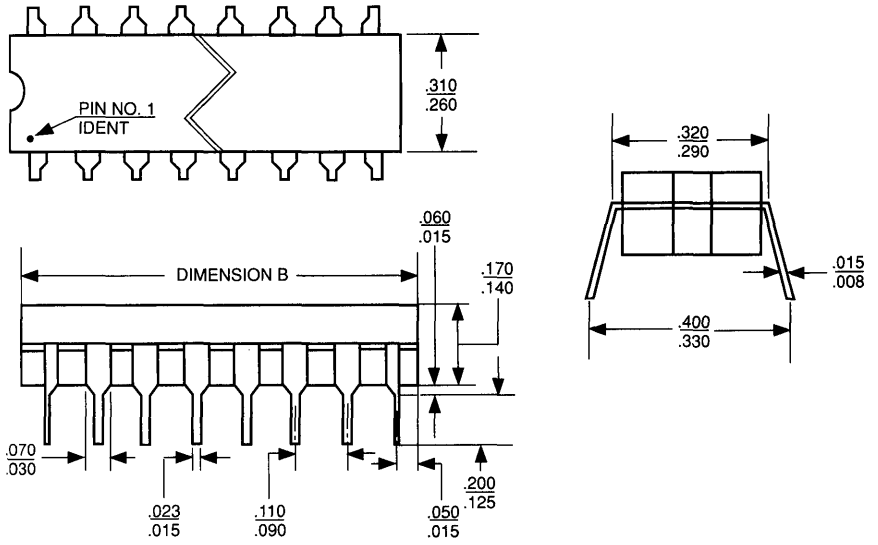
1. TOLERANCE UNLESS OTHERWISE SPECIFIED .xxx = ±.002"



SOIC PACKAGE DIMENSION

PACKAGE TYPE	DIMENSION B
16 Lead	0.409
20 Lead	0.509
24 Lead	0.609
28 Lead	0.709

CERDIP PACKAGE OUTLINE



CERDIP PACKAGE DIMENSION

PACKAGE TYPE	DIMENSION B
16 Lead	0.785
18 Lead	0.960
20 Lead	1.06
24 Lead	1.28

RS232/RS422 DRIVERS/RECEIVERS

FEATURES/BENEFITS

- RS232 and RS422 in One Chip
- Loopback for Self-testing
- Mode Selectable
- Short Circuit Protection
- Excellent Noise Immunity
- Tri-state Driver Outputs
- Low Power BiCMOS Technology
- ±15V Receiver Input Levels
- Small 0.3" Wide 24-Pin DIP Package

APPLICATIONS

- DTE - DCE Interface
- Packet Switching
- Local Area Networks
- Data Concentration
- Data Multiplexers
- Integrated Services Digital Network (ISDN)

DESCRIPTION

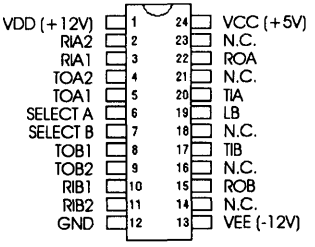
The SP301 and SP302 are single chip products containing both line drivers and receivers. They provide an interface between TTL level signals and Electronic Industries Associations Interface standard signals. They can be configured for either the single-ended interface Standard RS232 or the differential interface Standard RS422 modes of operation - or a combination of both. Each device has four different combinations of RS232 and/or RS422 drivers and receivers. The combination is selected by the logic inputs on the two selected pins - SEL A and SEL B. The SP301 and SP302 fully meet the requirements of the EIA standards when properly configured in the application circuits.

The RS232 line drivers convert TTL input levels into inverted RS232 output signals. The RS422 line drivers convert TTL input levels into RS422 differential output signals. The RS422 line driver output feature high source and sink current capability. All the line drivers are internally protected against short circuits on their outputs.

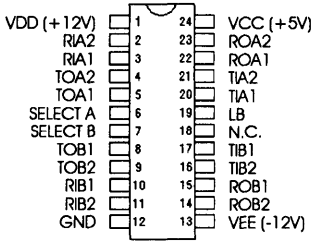
The RS232 receivers convert the EIA RS232 input signal into inverted TTL output logic levels. The RS422 line receivers convert the EIA RS422 differential input signals into non-inverted TTL output logic levels. The SP301 and SP302 receivers offer excellent noise immunity.

PIN CONFIGURATION

SP301



SP302



PARTS NUMBERING

Part Number	Package	Operating Temperature Range	RS232 Channels	RS422 Channels
SP301CS	Plastic	0°C to 70°C	2	2
SP301MR	Ceramic	-55°C to +125°C	2	2
SP301MR/883	Ceramic	-55°C to +125°C	2	2
SP302CS	Plastic	0°C to 70°C	4	2
SP302MR	Ceramic	-55°C to +125°C	4	2
SP302MR/883	Ceramic	-55°C to +125°C	4	2

Parts with suffix "/883" are processed in strict compliance with MIL-STD-883.

Filtering at the receiver eliminates any response to high frequency noise pulse. Input pulses with width of less than 1 mirco-second are completely ignored. The RS232 receiver circuit also employs voltage hysteresis. This helps eliminate spurious output transitions that might result from low amplitude noise voltages during slower speed signal transitions.

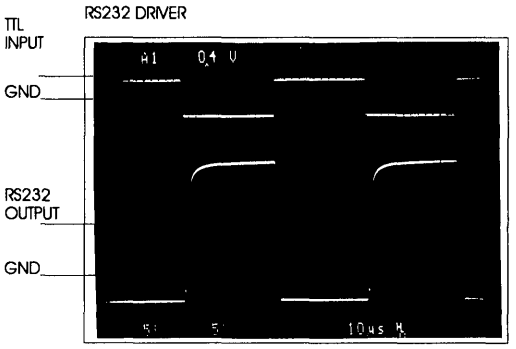
A loopback mode allows the driver outputs to be put into a tri-state (high impedance) level on the external line. Additionally, the driver outputs are internally switched to their associated receiver inputs. The internal switching provides a non-inverting signal path from the driver TTL inputs to the receiver TTL outputs.

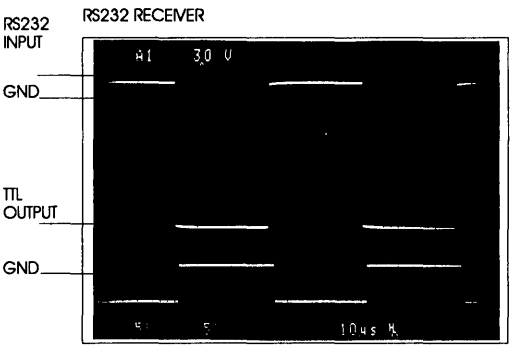
The controlling system can then perform a diagnostic self-tes of its RS232/RS422 transimit/receive circuitry at speeds up tc 3000 baud per second (BPS). This mode is enabled by providing a logic "0" on the LB pin.

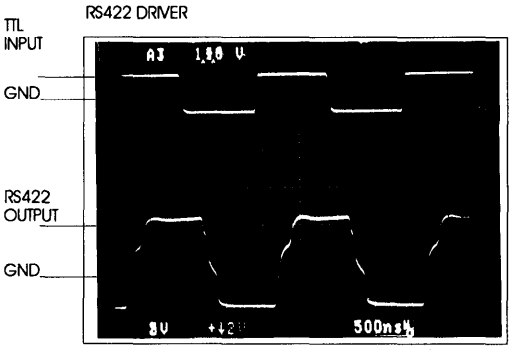
The SP301 and SP302 are manufactured using a BiCMOS process to provide low power operation.

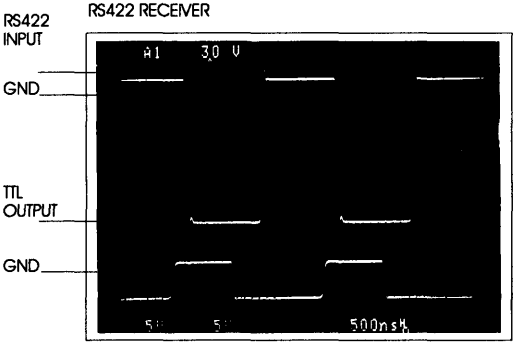
Both parts are available in 24 pin 0.300" DIP packages Plastic-packaged parts are available for operation over the commercial temperature range of 0° C to 70° C. Ceramic-packaged parts are available for operation over the military temperature range of -55° C to +125° C.

TYPICAL PERFORMANCE CURVES









ELECTRICAL CHARACTERISTICS RS232 & RS422 DRIVERS/RECEIVERS

V_{CC} = +5V ±5%, V_{DD} = +12V ±10%, V_{EE} = -12V ±10% unless otherwise specified
T_A = Operating Temperature Range unless otherwise specified

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
RS232 DRIVER					
TTL Input Level					
V_{IL}				0.8	Volts
V_{IH}		2.0			Volts
High Level Output Voltage	R_L = +3K Ohms V_{in} + =0.8V	6.0			Volts
Low Level Output Voltage	R_L = +3K Ohms V_{in} + = +2.0V			- 6.0	Volts
Short Circuit Protection Current	V_{out} = 0V			±20	mA
Output Voltage	R_L = 3K, V_{EE} = -12V @ Loop Back Mode	- 1.0		- 3.0	Volts
Slew Rate	C_L = 15pF, R_L = +3K Ohms			30	V/μS
	C_L = 15pF, R_L = +3K Ohms				
Transition Time	V_{out} from +3V to -3V or -3V to +3V			5	μS
Transmission Rate				20	KHz
RS232 RECEIVER					
Input Voltage Range		- 15		+15	Volts
Input High Threshold Voltage	Positive Going	+1.75		+2.5	Volts
Input Low Threshold Voltage	Negative Going	+0.75		+1.35	Volts
High Level Input Current	V_{in} = +15V	2.2		5.0	mA
Low Level Input Current	V_{in} = -15V	- 2.2		- 5.0	mA
Input Impedance	C_L < 2500pF	3		7	K Ohms
TTL Output Level					
V_{OL}	V_{CC} = +4.75V, I_{out} = +1.6mA			0.4	Volts
V_{OH}	V_{CC} = +4.75V, I_{out} = + - 0.5mA	2.4			Volts
Receiving Rate				20	KHZ
RS422 DRIVER					
TTL Input Level					
V_{IL}				0.8	Volts
V_{IH}		2.0			Volts
High Level Ouput Voltage	I_{OH} = - 20mA	2.75		6.0	Volts
Low Level Output Voltage	I_{OL} = +20mA			1.0	Volts
Differential Output Voltage	R_L = 100 Ohm	±2			Volts
	R_L = Infinity			±6	Volts
Short Circuit Output Current	Note 1			±100	mA
Output Current, Power Off	- 0.25V < Vo < V6			±500	μA
Transition Time	From 10% to 90% of steady state R_L = 100 Ohms, C_L = 15pF			400	nS
Transmission Rate				500	KHz
RS422 RECEIVER					
Common Mode Voltage Range	Note 2			± 7	Volts
Differential Input Voltage	Note 2			±15	Volts
Differential Input Threshold Voltage		- 0.2		+0.2	Volts
Input Voltage Hysteresis	V_{cm} = 0V	30			mV
Input Current	V_{in} = +15V			+5.0	mA
	V_{in} = - 15V			- 5.0	mA
Input Resistance	- 7V < Vcm <7V	3			K Ohms
Logic Output Level					
V_{OL}	V_{CC} = +4.75V, I_{out} = +1.6mA			0.4	Volts
V_{OH}	V_{CC} = +4.75V, I_{out} = - 0.5mA	2.4			Volts
Receiving Rate				500	KHz
Short Circuit Output Current	V_{out} = 0V			±100	mA
Power Supply Current					
I_{DD}	Note 3		7	12	mA
I_{CC}	Note 3		5	7	mA
I_{EE}	Note 3		11	15	mA

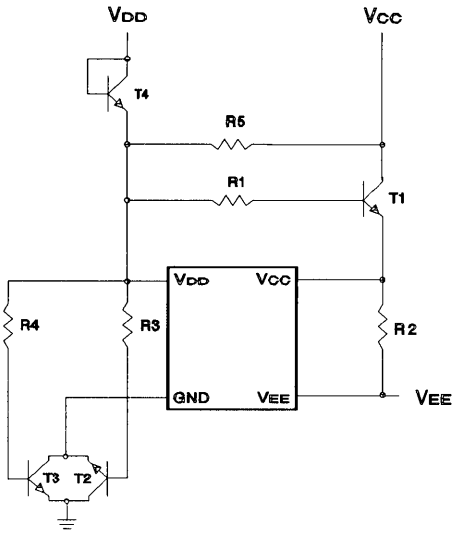
Note 1: Only one output drive pin per package will be shorted at any time.

Note 2: This is an absolute maximum rating, normal operating levels will have V_I < 5V.

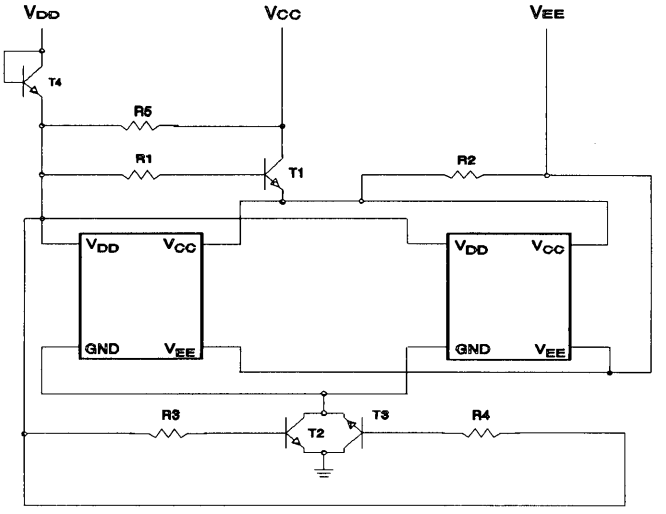
Note 3: Outputs unloaded; Inputs tied to GND; T_A= +25° C; V_{IL} = OV.

SUGGESTED APPLICATIONS CIRCUITS

Single SP30X



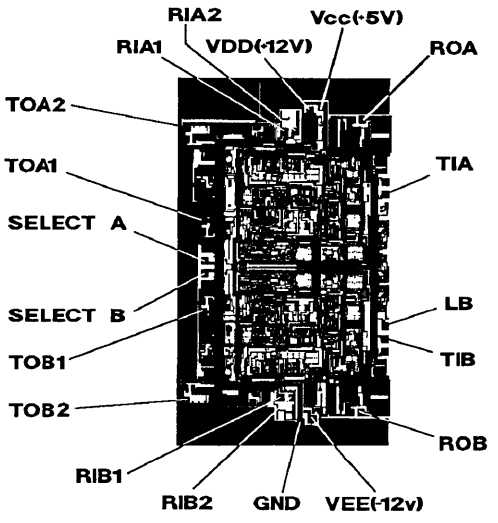
Multiple SP30X



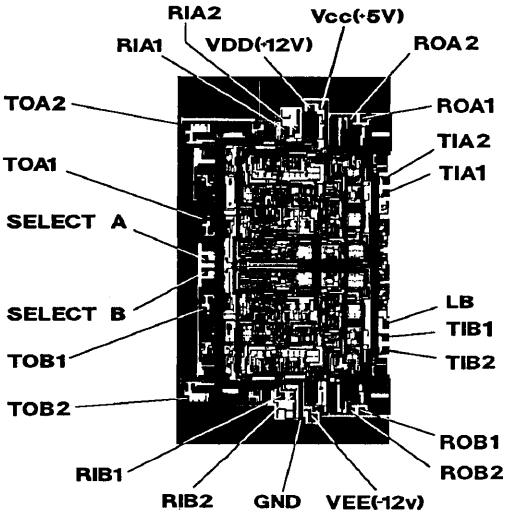
R1=R2=R3=R4= 3.3K Ohms
R5= 15K Ohms
T1=T2=T3=T4= 2N2222A

DIE CHARACTERISTICS

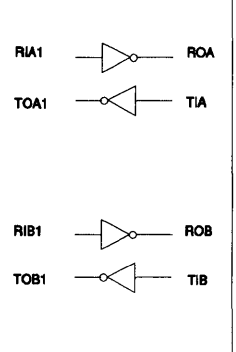
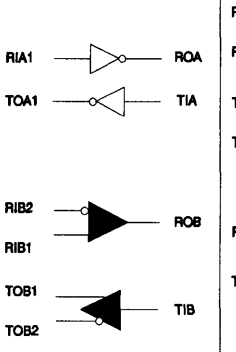
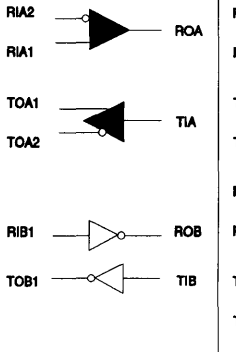
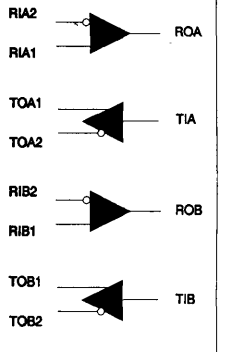
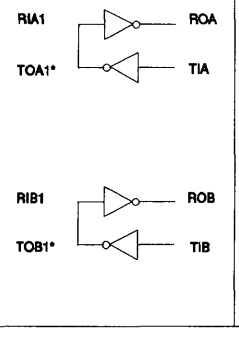
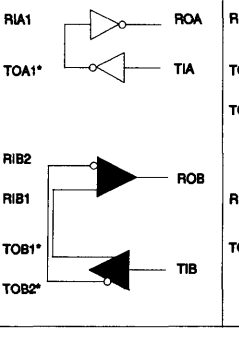
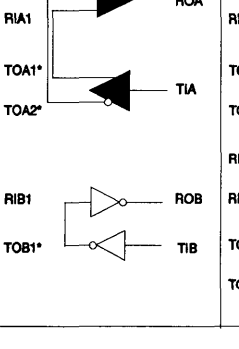
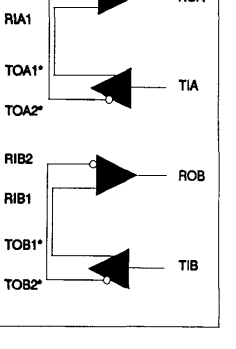
SP301
164.41 X 271.44 Mils



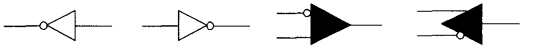
SP302
164.41 X 271.44 Mils



CONTROL LOGIC CONFIGURATION SP301

SELECT PIN	LOGIC VALUE	LOGIC VALUE	LOGIC VALUE	LOGIC VALUE
SEL A SEL B	0 0	0 1	1 0	1 1
NON-LOOPBACK (LB=1)				
LOOPBACK (LB=0)				

SYMBOL DEFINITIONS



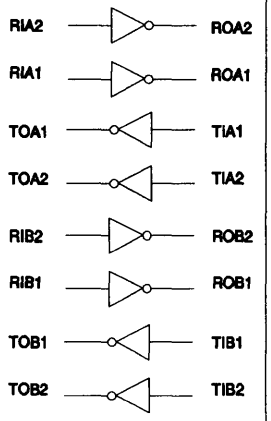
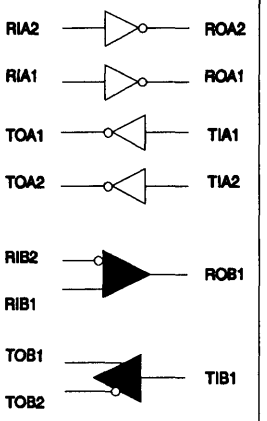
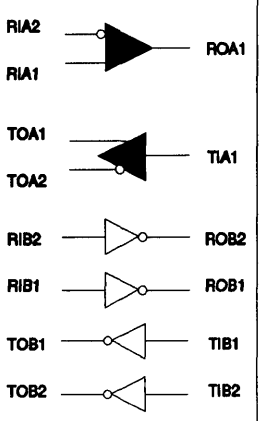
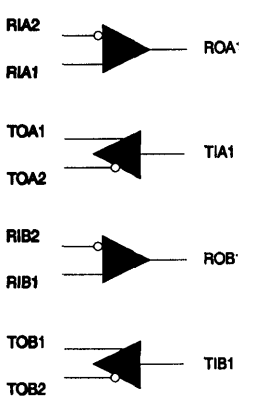
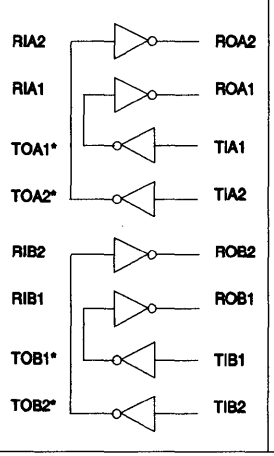
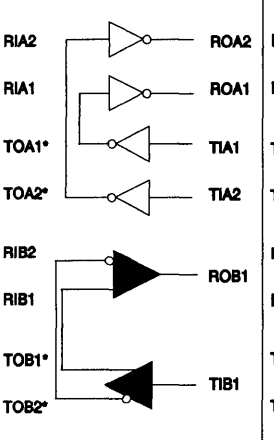
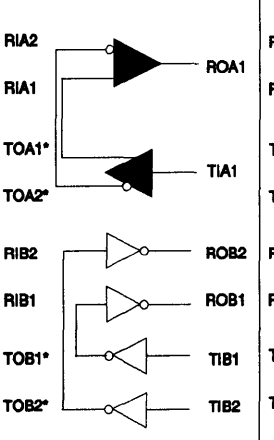
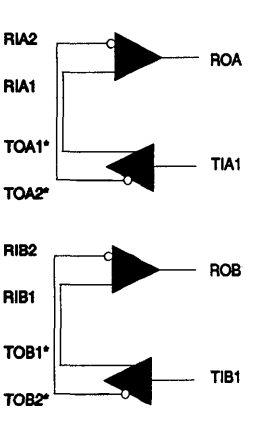
RS232 Driver
*Tri-State Output

RS232 Receiver

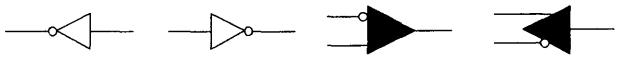
RS422 Receiver

RS422 Driver

CONTROL LOGIC CONFIGURATION SP302

SELECT PIN	LOGIC VALUE	LOGIC VALUE	LOGIC VALUE	LOGIC VALUE
SEL A SEL B	0 0	0 1	1 0	1 1
NON-LOOPBACK (LB=1)				
LOOPBACK (LB=0)				

SYMBOL DEFINITIONS



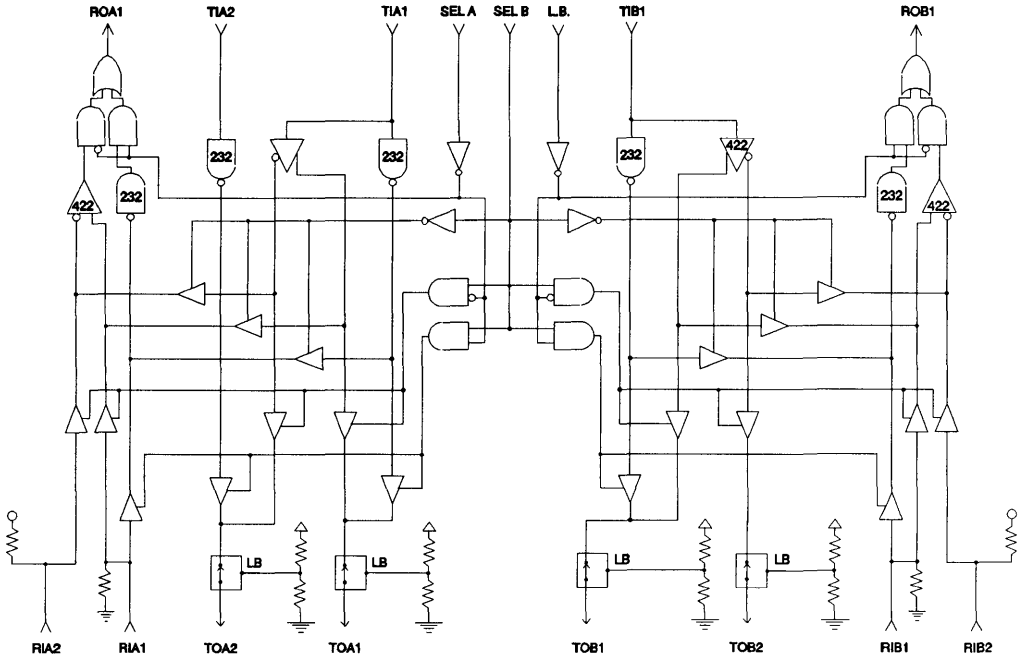
RS232 Driver
*Tri-State Output

RS232 Receiver

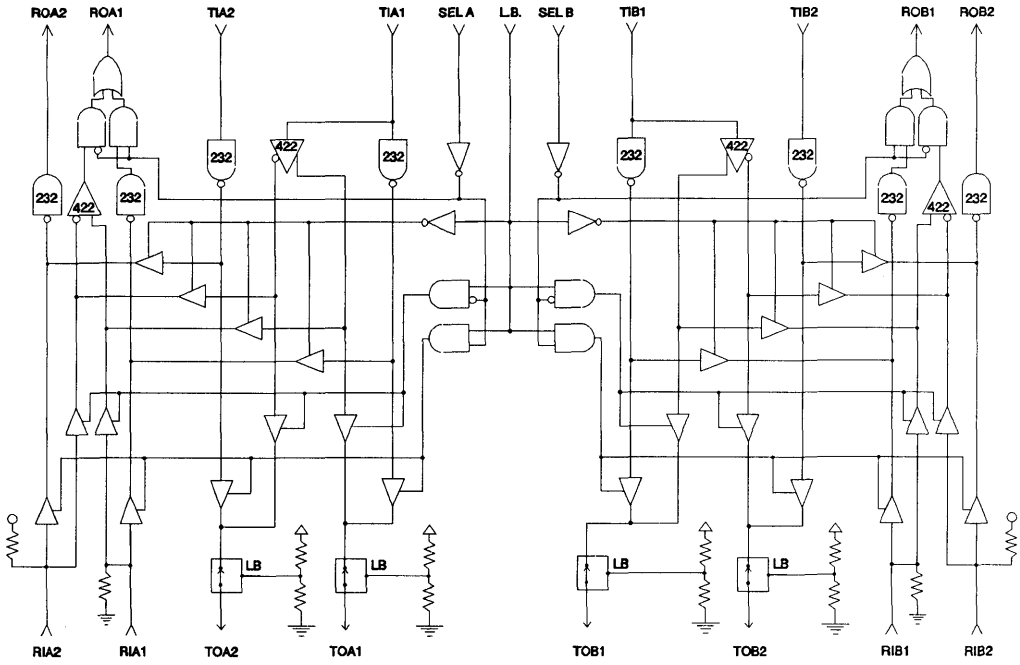
RS422 Receiver

RS422 Driver

SCHEMATIC OF SP301



SCHEMATIC OF SP302

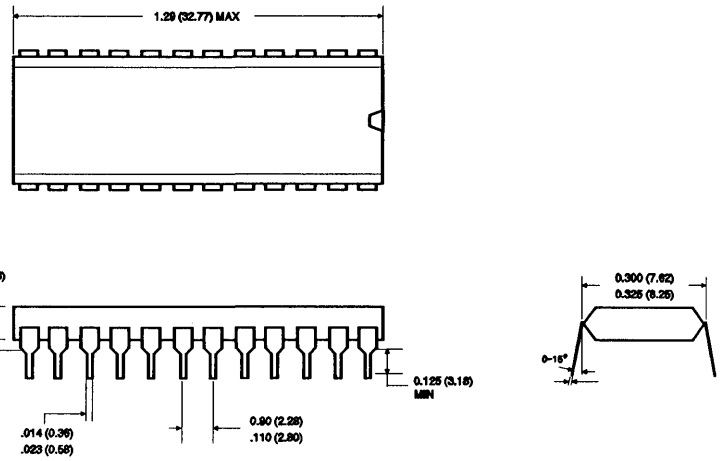


POWER SUPPLY SYMBOLS

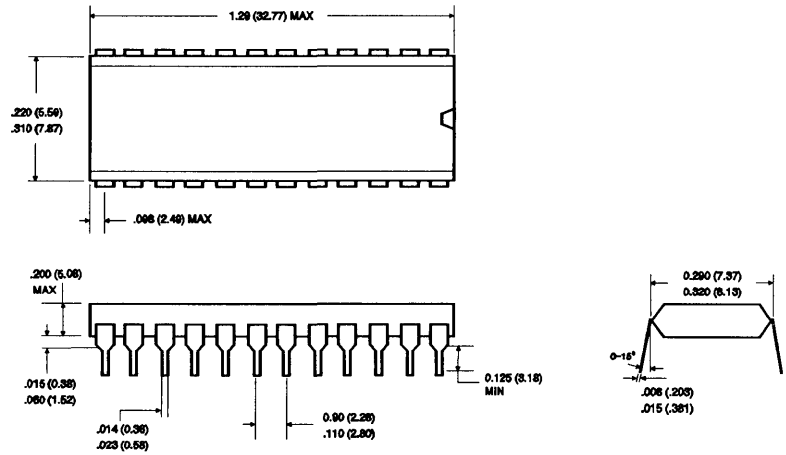
= V_{CC} = V_{EE} = GND

PACKAGE OUTLINES

24-PIN PLASTIC DIP



24-PIN CERAMIC DIP



HIGH SPEED OPERATIONAL AMPLIFIERS

MODEL	-55°C TO +125°C	0°C TO +75°C	SLEW RATE (V/µs)	GAIN BANDWIDTH PRODUCT (MHz)	BIAS CURRENT (nA)	OPEN LOOP GAIN (V/V)	MINIMUM STABLE GAIN	PAGE
SP111	X	X	2	2	0.0008			99
SP2400	X	X	30	40	50	150,000	1	107
SP2500	X		30	12	100	30,000	1	111
SP2502	X		30	12	125	25,000	1	111
SP2505		X	30	12	125	25,000	1	111
SP2510	X		65	12	100	15,000	1	117
SP2512	X		60	12	125	15,000	1	117
SP2515		X	60	12	125	15,000	1	117
SP2520	X		120	20	100	15,000	3	123
SP2522	X		120	20	125	15,000	3	123
SP2525		X	120	20	125	15,000	3	123
SP2539	X	X	600	600	5,000	30,000	1	129
SP2540	X	X	400	400	5,000	30,000	1	131
SP2541	X	X	280	40	6,000	10,000	1	133
SP2600	X		7	12	1	150,000	1	135
SP2602	X		7	12	15	150,000	1	135
SP2605		X	7	12	5	150,000	1	135
SP2620	X		35	100	1	150,000	5	141
SP2622	X		35	100	5	150,000	5	141
SP2625		X	35	100	5	150,000	5	141
HS4010	X	X	1,000	70	0.1		1	147
SP5190	X		150	200	5,000	30,000	1	155
SP5195		X	150	200	5,000	30,000	1	155
SP9610	X	X	2,500	100	5,000			159

PROGRAMMABLE GAIN AMPLIFIERS

MODEL	GAIN RANGES	MAXIMUM GAIN ERROR	INPUT BIAS CURRENT	OUTPUT SETTLING (To 0.1%)	SMALL SIGNAL BANDWIDTH (G = 1)	PACKAGE	PAGE
HS2020	1,2,4,8,16, 32,64,128 digitally programmed	±0.005 to ±0.2 depending on range	±200 pA	G = 1, 5.2 µsec max G = 128, 70 µsec max	5 MHz	18-Pin DIP	105

Shaded area indicates new product since publication of 1988 Catalog

PRECISION OPERATIONAL AMPLIFIER

FEATURES/BENEFITS

- Low Noise
- Low Input Bias Current
- Low Input Offset Voltage
- Low Drift
- High Common-Mode Rejection
- High Open-Loop Gain

Preliminary Specification

APPLICATIONS

- Medical Instrumentation
- Process Control Equipment
- Sensors
- Robotics
- Test Equipment
- Instrumentation
- Avionics
- Data Acquisition

DESCRIPTION

The SP111 and SP121 are precision monolithic operational amplifiers with outstanding performance characteristics that allow their use in even the most demanding instrumentation applications.

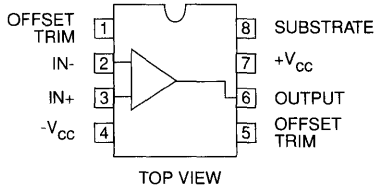
Designed completely with vertical transistor structures and dielectric isolation along with the use of Sipex' special SiFET® field effect transistors, the SP111/121 can provide superior performance in even the harshest of environments. This construction provides a latch-free performance in a radiation environment. Radiation tolerance is significantly improved over designs utilizing junction isolation, trench isolation, or lateral transistors in dielectric isolation.

Precision performance characteristics such as low input bias current, low input offset voltage, low input noise current, minimal drift, high open-loop gain, high common-mode rejection ratio, and high power supply rejection ratio exceed those of other field effect transistor technology amplifiers.

Improved performance in existing designs is easily obtained due to the industry standard 741 pin configuration.

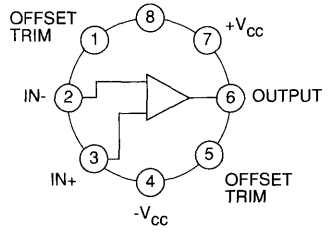
4

CONNECTION DIAGRAMS



TOP VIEW

SUBSTRATE AND CASE



PARTS NUMBERING

Part Number	Package	Operating Range
SP111AIH	TO-99 CAN	-25°C to +85°C
SP111AMH	TO-99 CAN	-55°C to +125°C
SP111AMH/883*	TO-99 CAN	-55°C to +125°C
SP111BIH	TO-99 CAN	-25°C to +85°C
SP121BCH	TO-99 CAN	0°C to +70°C
SP121ACP	8-PIN PLASTIC DIP	0°C to +70°C

* Processed in compliance with MIL-STD-883

ABSOLUTE MAXIMUM RATINGS[1]

Voltage between $+V_{CC}$ and $-V_{CC}$ Terminals 33V
Differential Input Voltage 33V
Input Voltage Range ..... ±16.5V
Output Short Circuit Duration ..... Continuous
Maximum Junction Temperature ..... +175°C
Maximum Storage Temperature Range ..... -65°C < T_A < +150°C

ELECTRICAL CHARACTERISTICS

$+V_{CC}$ = +15V, $-V_{CC}$ = -15V, and pin 8 connected to ground unless otherwise specified.

			SP111AIH			SP111AMH SP111AMH/883			
PARAMETERS	**CONDITIONS**	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Offset Voltage	V_{CM} = 0 Vdc	25°C		±100	±500		±100	±500	µV
		Full		±220	±1000		±300	±1500	µV
Average Offset Voltage Drift		Full		±2	±5		±2	±5	µV/°C
Bias Current	V_{CM} = 0 Vdc	25°C		±0.8	±2		±0.8	±2	pA
		Full		±50	±250		±820	±4100	pA
Offset Current	V_{CM} = 0 Vdc	25°C		±0.5	±1.5		±0.5	±1.5	pA
		Full		±30	±200		±510	±3100	pA
Differential Impedance		25°C		10^{13} II 1			10^{13} II 1		ΩII pF
Common Mode Impedance		25°C		10^{14} II 3			10^{14} II 3		ΩII pF
Common Mode Range		25°C	±10	±11		±10	±11		V
		Full	±10	±11		±10	±11		V
Input Noise Voltage Density									
f_O = 10 Hz		25°C		40	80		40	80	nV/√Hz
f_O = 100 Hz		25°C		15	40		15	40	nV/√Hz
f_O = 1 Hz		25°C		10	15		10	15	nV/√Hz
f_O = 10 kHz		25°C		9			9		nV/√Hz
f_O = 10 Hz to 10 kHz		25°C		0.7	1.2		0.7	1.2	μV_{RMS}
f_O = 0.1 Hz to 10 Hz		25°C		1.6	3.3		1.6	3.3	μV_{p-p}
Input Noise Current Density									
f_O = 0.1 Hz to 10 kHz		25°C		9.5	15		9.5	15	fA_{p-p}
f_O = 0.1 Hz thru 20 kHz		25°C		0.5	0.8		0.5	0.8	fA/√Hz
Large Signal Voltage Gain	$R_L \geq 2$ kΩ	25°C	114	125		114	125		dB
		Full	110	120		110	120		dB
Common Mode Rejection	V_{IN} = ±10 Vdc	25°C	90	110		90	110		dB
Ratio		Full	86	100		86	100		dB
Minimum Stable Gain		Full	1			1			
Gain-Bandwidth Product		25°C		2			2		MHz
Output Voltage Swing	$R_L \geq 2$ kΩ	25°C	±11	±12		±11	±12		V
		Full	±10.5	±11		±11	±11.5		V
Output Current	V_O = ±10 Vdc	25°C	±5.5	±10		±5.5	±10		mA
		Full	±5.25	±10		±5.25	±10		mA
Short Circuit Current	V_O = 0 Vdc	Full	10	40		10	40		mA
Output Resistance	DC, Open-loop	25°C		100			100		Ω
Full Power Bandwidth	$20V_{p-p}$, R_L = 2 kΩ	25°C	16	32		16	32		kHz
Slew Rate	V_O = ±10V, R_L = 2 kΩ	25°C	1	5		1	5		V/µsec
Settling Time	A_V = -1, R_L = 2 kΩ								
10V to 0.1%		25°C		6			6		µsec
10V to 0.01%		25°C		10			10		µsec
Overload Recovery[2]	A_V = -1								
50% Overdrive		25°C		5	3.5		5		µsec
Supply Current	I_O = 0 mADC	25°C		2.5	3.5		2.5	3.5	mA
		Full		2.5			2.5	3.5	mA
Power Supply Rejection Ratio	V_{CC} = ±10V to ±16.5V	25°C	90	110		90	110		dB
		Full	86	100		86	100		dB

ELECTRICAL CHARACTERISTICS

$+V_{CC}$ = +15V, $-V_{CC}$ = -15V, and pin 8 connected to ground unless otherwise specified.

			SP111BIH			
PARAMETERS	**CONDITIONS**	**TEMP**	**MIN**	**TYP**	**MAX**	**UNITS**
Offset Voltage	V_{CM} = 0 Vdc	25°C		±50	±250	µV
		Full		±110	±500	µV
Average Offset Voltage Drift		Full		±0.5	±1.5	µV/°C
Bias Current	V_{CM} = 0 Vdc	25°C		±0.5	±1	pA
		Full		±30	±130	pA
Offset Current	V_{CM} = 0 Vdc	25°C		±0.25	±0.75	pA
		Full		±15	±100	pA
Differential Impedance		25°C		10^{13} ll 1		Ωll pF
Common Mode Impedance		25°C		10^{14} ll 3		Ωll pF
Common Mode Range		25°C	±10	±11		V
		Full	±10	±11		V
Input Noise Voltage Density						
f_O = 10 Hz		25°C		30	60	nV/√Hz
f_O = 100 Hz		25°C		12	30	nV/√Hz
f_O = 1 kHz		25°C		9	12	nV/√Hz
f_O = 10 kHz		25°C		8		nV/√Hz
f_O = 10 Hz to 10 kHz		25°C		0.6	1.0	μV_{RMS}
f_O = 0.1 Hz to 10 Hz		25°C		1.2	2.5	μV_{p-p}
Input Noise Current Density						
f_O = 0.1 Hz to 10 kHz		25°C		7.5	12	fA_{p-p}
f_O = 0.1 Hz thru 20 kHz		25°C		0.4	0.6	fA/√Hz
Large Signal Voltage Gain	$R_L \geq 2$ kΩ	25°C	115	125		dB
		Full	114	120		dB
Common Mode Rejection Ratio	V_{IN} = ±10 Vdc	25°C	100	110		dB
		Full	90	100		dB
Minimum Stable Gain		Full	1			dB
Gain-Bandwidth Product		25°C		2		MHz
Output Voltage Swing	$R_L \geq 2$ kΩ	25°C	±11	±12		V
		Full	±11	±11.5		V
Output Current	V_O = ±10 Vdc	25°C	±5.5	±10		mA
		Full	±5.25	±10		mA
Short Circuit Current	V_O = 0 Vdc	Full	10	40		mA
Output Resistance	DC, Open-loop	25°C		100		Ω
Full Power Bandwidth	$20V_{p-p}$, R_L = 2 kΩ	25°C	16	32		kHz
Slew Rate	V_O = ±10V, R_L = 2 kΩ	25°C	1	5		V/µsec
Settling Time	A_V = -1, R_L = 2 kΩ					
10V to 0.1%		25°C		6		µsec
10V to 0.01%		25°C		10		µsec
Overload Recovery[2]						
50% Overdrive		25°C		6		µsec
Supply Current	Quiescent Current with I_O = 0 mADC	25°C		2.5	3.5	mA
		Full		2.5	3.5	mA
Power Supply Rejection Ratio	V_{CC} = ±10V to ±16.5V	25°C	100	110		dB
		Full	90	100		dB

ELECTRICAL CHARACTERISTICS

$+V_{CC}$ = +15V, $-V_{CC}$ = -15V, and pin 8 connected to ground unless otherwise specified.

			SP121BCH			SP121ACP			
PARAMETERS	**CONDITIONS**	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Offset Voltage	V_{CM} = 0 Vdc	25°C		±0.5	±2		±0.5	±3	mV
		Full		±1	±3		±1	±5	mV
Average Offset Voltage Drift		Full		±3	±10		±3	±10	µV/°C
Bias Current	V_{CM} = 0 Vdc	25°C		±1	±5		±1	±10	pA
		Full		±23	±115		±23	±250	pA
Offset Current	V_{CM} = 0 Vdc	25°C		±0.7	±4		±0.7	±8	pA
		Full		±16	±100		±16	±200	pA
Differential Impedance		25°C		10^{13} II 1			10^{13} II 1		ΩII pF
Common Mode Impedance		25°C		10^{14} II 3			10^{14} II 3		ΩII pF
Common Mode Range		25°C	±10	±11		±10	±11		V
		Full	±10	±11		±10	±11		V
Input Noise Voltage Density									
f_O = 10 Hz		25°C		40			50		nV/√Hz
f_O = 100 Hz		25°C		15			18		nV/√Hz
f_O = 1 kHz		25°C		10			12		nV/√Hz
f_O = 10 kHz		25°C		9			10		nV/√Hz
f_O = 10 Hz to 10 kHz		25°C		0.7			0.8		μV_{RMS}
f_O = 0.1 Hz to 10 Hz		25°C		1.6			2		μV_{p-p}
Input Noise Current Density									
f_O = 0.1 Hz to 10 kHz		25°C		15			21		fA_{p-p}
f_O = 0.1 Hz thru 20 kHz		25°C		0.8			1.1		fA/√Hz
Large Signal Voltage Gain	$R_L \geq 2$ kΩ	25°C	110	120		106	114		dB
		Full	106	116		100	110		dB
Common Mode Rejection	V_{IN} = ±10 Vdc	25°C	86	104		82	110		dB
Ratio		Full	82	98		80	96		dB
Minimum Stable Gain		Full	1			1			
Gain-Bandwidth Product		25°C		2			2		MHz
Output Voltage Swing	$R_L \geq 2$ kΩ	25°C	±11	±12		±11	±12		V
		Full	±10.5	±11		±10.5	±11		V
Output Current	V_O = ±10 Vdc	25°C	±5.5	±10		±5.5	±10		mA
		Full	±5.25	±10		±5.25	±10		mA
Short Circuit Current	V_O = 0 Vdc	Full	10	40		10	40		mA
Output Resistance	DC, Open-loop	25°C		100			100		Ω
Full Power Bandwidth	$20V_{p-p}$, R_L = 2 kΩ	25°C		32			32		kHz
Slew Rate	V_O = ±10V, R_L = 2 kΩ	25°C		5			5		V/µsec
Settling Time	A_V = -1, R_L = 2 kΩ								
10V to 0.1%		25°C		6			6		µsec
10V to 0.01%		25°C		10			10		µsec
Overload Recovery[2]	A_V = -1								
50% Overdrive		25°C		5			5		µsec
Supply Current	I_O = 0 mADC	25°C		2.5	4		2.5	4.5	mA
		Full		2.5	4.5		2.5	5.0	mA
Power Supply Rejection Ratio	V_{CC} = ±10V to	25°C	86	104		86	104		dB
	±16.5V	Full	82	94		82	94		dB

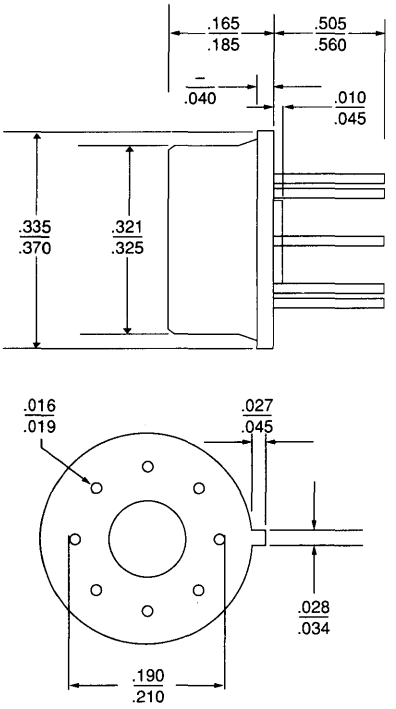
NOTES

The following notes apply to the Electrical Characteristics and Absolute Maximum Ratings Tables:

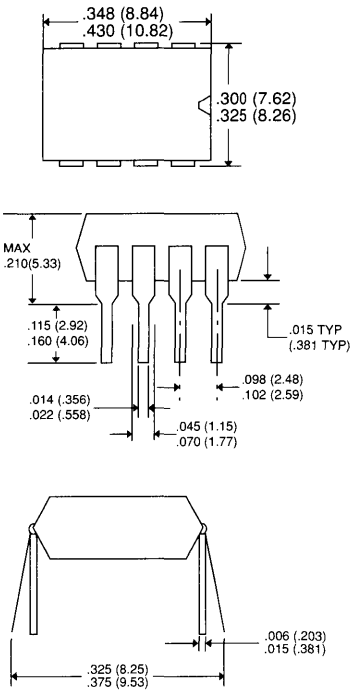
1. Absolute maximum ratings represent the values beyond which the part may be damaged. Functional operation at these values is not necessarily implied.
2. Overload recovery is defined as the time required for the output to resume linear operation after reaching saturation due to a 50% input overdrive.

PACKAGE OUTLINES

8 PIN TO -99 METAL CAN



8 PIN PLASTIC DIP



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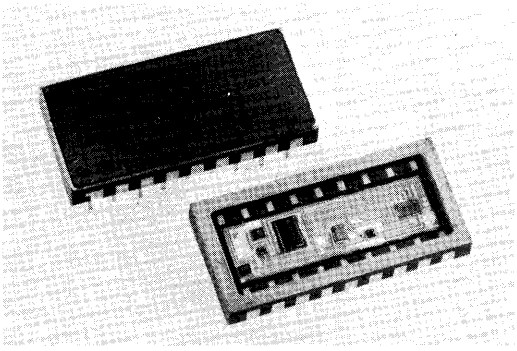
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS 2020
Programmable Gain Amplifier

FEATURES

- **Digitally Programmable 1 to 128**
- **Gain Nonlinearity 0.002%**
- **Gain Accuracy 0.002%**
- **Full Power Bandwidth 100 kHz**
- **Low Offset Drift: < 5 μV/°C**
- **MIL-STD-883 Rev. C, Level B Screening Available**



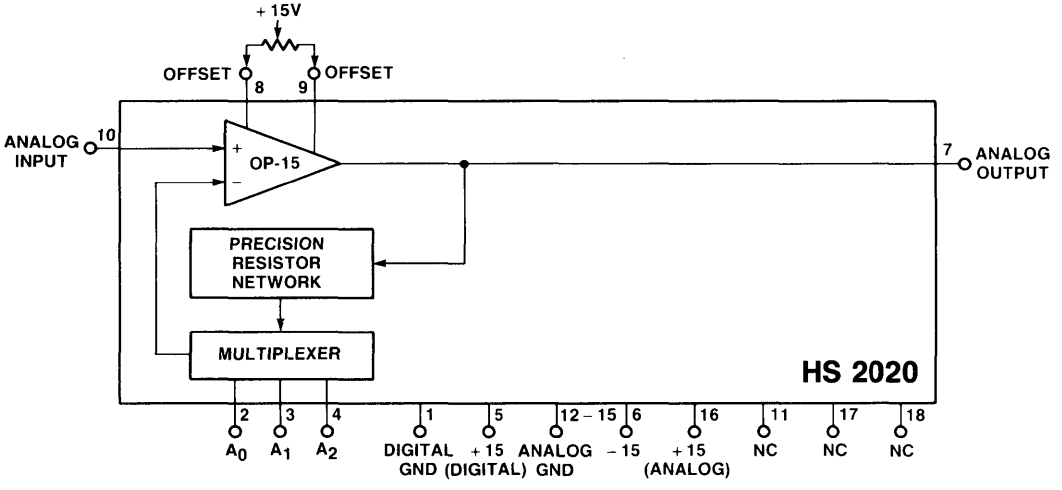
APPLICATIONS

- **Autoranging A/D**
- **μP Data Acquisition**
- **A/D Input Amplifier**
- **Sample and Hold Buffer**

DESCRIPTION

The HS 2020 is a precision hybrid amplifier that features high speed low offset performance in addition to being user programmable for gains from 1 to 128. A gain range from 1 to 128 can be achieved from binary (TTL) inputs to the HS 2020 in 8 steps. This gives the user a dynamic range of 19 bits with analog input steps from ±20 mV to ±10V. The HS 2020 uses the precision JFET OP-15 amplifier along with a laser trimmed stable nichrome thin film resistor network. The HS 2020 features very low 100 μV offset voltage which yields much less than ½ LSB in a 12 bit ADC. The excellent performance over temperature (−55°C to +125°C) is achieved by combining a proven circuit configuration with the benefits of state-of-the-art hybrid manufacturing to achieve low cost, small size, and high reliability. The HS 2020 is available in 2 versions. The HS 2020C is specified over a temperature range of 0°C to +70°C. The HS 2020B is specified from −55°C to +125°C and is fully screened and tested to MIL-STD-883 Rev. C, Level B requirements.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C, supply voltage ±15VDC, unless otherwise specified)

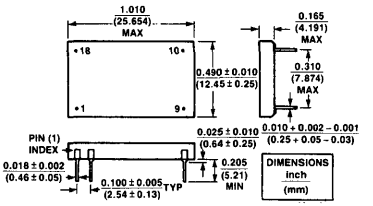
GAIN (Non-Inverting)	
Fixed Settings	1,2,4,8,16,32,64,128
Gain Nonlinearity (% FSR)	
G = 1	0.005% max (0.002% typ)
G = 8	0.006% max (0.002% typ)
G = 32	0.007% max (0.003% typ)
G = 64	0.008% max (0.003% typ)
G = 128	0.008% max (0.003% typ)
Gain Accuracy	
Initial (+25°C)	
G = 1	0.005% max (0.003% typ)
G = 128	0.2% max (0.1% typ)
VS Temperature	
(−25°C to +85°C)	
G = 1	0.008% max (0.003% typ)
G = 128	0.24% max (0.1% typ)
(−55°C to +125°C)	
G = 1	0.01% max (0.004% typ)
G = 128	0.4% max (0.2% typ)
ANALOG INPUT	
Input Impedance	$10^9\Omega$
Input Voltage Range	±12VDC
VOLTAGE OFFSET, Referred to Input	
Initial (@ +25°C)	
Adjustable to Zero	
G = 1	0.5mV max
G = 128	0.5mV max (0.1mV typ)
VS Temperature	
(−55°C to +125°C)	
G = 1	2mV max
G = 128	2mV max (0.5mV typ)
INPUT CURRENT	
Input Bias Current	±200pA max (±40pA typ)
VS Temperature	
(−55°C to +125°C)	±19nA max (±2.7nA typ)
NOISE	
Voltage Noise, RTI	
0.1 Hz to 10 Hz	
G = 1	4μV p-p
G = 128	4μV p-p
10 Hz to 1 MHz	
G = 1	200μV p-p
Current Noise	
0.1 Hz to 10 Hz	
G = 1	0.26pA p-p
G = 128	0.26pA p-p
10 Hz to 10 kHz	
G = 1	4pA p-p
LOGIC INPUT (TTL)[1]	
Logic "1"	+2.0V min
Logic "0"	0.8V min
Input Current	20μA max
Switching Time	0.7μSec
OUTPUT CHARACTERISTICS	
Output Range	±10V min (±12V typ)
Output Current	±5mA max
DYNAMIC RESPONSE	
Small Signal BW (G = 1)	5 MHz
Full Power BW	100 kHz
Slew Rate (G = 1)	15V/μSec
Output Settling (to 0.1%)	
G = 1	5.2μSec max (4μSec typ)
G = 16	8μSec max (5μSec typ)
G = 128	70μSec max (40μSec typ)
TEMPERATURE	
Operating	
-B	−55°C to +125°C
-C	0°C to +70°C
Storage	−65°C to +150°C
POWER SUPPLY	
Power Supply Range	±18V max (±15V typ)
Current	+16mA, −8mA
MBTF	260,000 hrs

NOTE:
1. Digital inputs should not exceed +8V. Logic supply at pin 5 must be at least +5V to maintain logic levels.

MECHANICAL

Case Style — Ceramic Pkg, Metal Lid

Case Dimensions

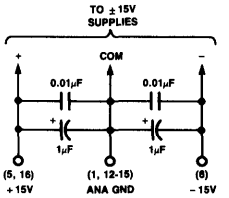


PIN ASSIGNMENTS

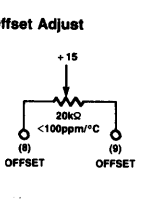
PIN	FUNCTION	PIN	FUNCTION
1	DIGITAL GND	18	NC
2	A_0	17	NC
3	A_1	16	+15 (ANALOG)
4	A_2	15	ANALOG GND
5	+15 (DIGITAL)	14	ANALOG GND
6	−15	13	ANALOG GND
7	ANALOG OUTPUT	12	ANALOG GND
8	OFFSET	11	NC
9	OFFSET	10	ANALOG INPUT

APPLICATIONS INFORMATION

RECOMMENDED POWER SUPPLY BYPASS CIRCUIT



OPTIONAL OFFSET AND GAIN ADJUSTMENTS



NOTE:
1. Analog ground shown connected to digital ground. User may elect to segregate these in a system application.

GAIN CODES AND SETTLING TIMES

GAIN	DIGITAL CODE A_2	A_1	A_0	OUTPUT SETTLING TIME* (±0.1% 20V Step)
1	0	0	0	4μSec
2	0	0	1	4μSec
4	0	1	0	4μSec
8	0	1	1	4μSec
16	1	0	0	5μSec
32	1	0	1	11μSec
64	1	1	0	20μSec
128	1	1	1	40μSec

*For each gain value the magnitude of the input step was chosen to make the output step 20V.

GAIN ACCURACIES

GAIN	ACCURACY (%)					
	25°C		−25°C to +85°C		−55°C to +125°C	
	TYPICAL	MAX	TYPICAL	MAX	TYPICAL	MAX
1	0.002	0.005	0.003	0.008	0.004	0.010
2	0.005	0.015	0.005	0.020	0.008	0.020
4	0.005	0.015	0.005	0.024	0.015	0.040
8	0.010	0.020	0.015	0.048	0.020	0.080
16	0.020	0.030	0.020	0.048	0.025	0.080
32	0.020	0.040	0.020	0.060	0.040	0.100
64	0.040	0.100	0.040	0.180	0.100	0.300
128	0.100	0.200	0.100	0.240	0.200	0.400

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 2020C	Programmable Gain Amplifier 0°C to +70°C
HS 2020B	Programmable Gain Amplifier Per MIL-STD-883 Rev. C, Level B −55°C to +125°C

Specifications subject to change without notice.

PRAM FOUR CHANNEL PROGRAMMABLE AMPLIFIER

PRELIMINARY INFORMATION

FEATURES

- Programmability
- Low Offset Voltage
- High Slew Rate
- Wide Bandwidth
- High Gain
- Low Crosstalk
- High Input Impedance

APPLICATIONS

- Signal Selection/Multiplexing
- Op Amp Gain
- Comparator Level Control
- Filter Programming
- Oscillator Frequency Control

DESCRIPTION

The SP2400 is a unique four channel high speed programmable monolithic amplifier. Utilizing four input amplifier channels, any channel (or none) may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth, and power bandwidth performance. External compensation is not required at closed loop gains of greater than 10.

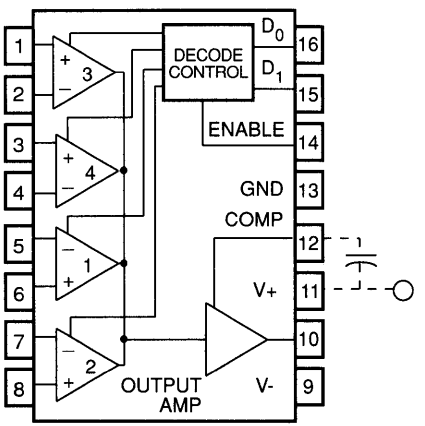
Programmability coupled with 2 mV offset voltage and 5 nA offset current makes the SP2400 outstanding for signal conditioning circuits. Each channel can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This ability makes the SP2400 ideal for multiplexing, signal selection, mathematical function designs, active filters, and data acquisition applications.

The SP2400 is available in a 16 pin dual-in-line package and specified from 0°C to +70°C for commercial or -55°C to +125°C for military applications.

4

CONNECTION DIAGRAM

TOP VIEW



PARTS NUMBERING

Part Number	Package	Operating Range
SPI-2400-2	Ceramic Dip	-55°C to +125°C
SP2400/883	Ceramic Dip	-55°C to +125°C*
SPI-2404-4	Ceramic Dip	-25°C to +85°C
SPI-2404-5	Ceramic Dip	0°C to +70°C

* Processed in compliance with MIL-STD-883

TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V- Terminals 45.0V
Differential Input Voltage ..... $\pm V_{Supply}$
Digital Input Voltage ..... -0.76V to +10.0V
Output Current ..... Short Circuit Protected
($I_{SC} \leq \pm 33$ mA)
Internal Power Dissipation (Note 13) ..... 300 mW
Operating Temperature Range ..... $-55°C \leq T_A \leq +125°C$ (SP2400)
$-25°C \leq T_A \leq +85°C$ (SP2404)
$0°C \leq T_A \leq +75°C$ (SP2405)
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

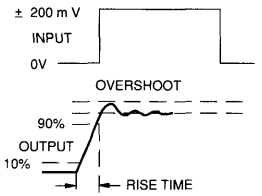
Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.
Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$. Limits apply to each of the four channels, when addressed.

		SP2400/SP2404 LIMITS			SP2405 LIMITS			
PARAMETERS	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
Offset Voltage	+25°C		1	2		1	2	mV
	Full			2			2	mV
Bias Current (Note 12)	+25°C		50	200		50	250	nA
	Full			400			500	nA
Offset Current (Note 12)	+25°C		5	50		5	50	nA
	Full			100			100	nA
Input Resistance (Note 12)	+25°C		30			30		MΩ
Common Mode Range	Full	±9.0			±9.0			V
Large Signal Voltage Gain (Notes 1,5)	+25°C	50K	300K		50K	300K		V/V
	Full	25K			25K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Note 3,14)	+25°C	20	40		20	40		MHz
(Note 4,14)	+25°C	4	8		4	8		MHz
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current	+25°C	±10	±20		10	20		mA
Full Power Bandwidth (Notes 3,5,14)	+25°C	300	475		300	475		kHz
(Notes 4,5,14)	+25°C	100	200		100	200		kHz
Rise Time (Notes 4,6)	+25°C		20	45		20	50	ns
Overshoot (Notes 4,6)	+25°C		5	40		25	40	%
Slew Rate (Notes 3,7)	+25°C	20	30		20	30		V/µs
(Notes 4,7)	+25°C	6	8		6	8		V/µs
Settling Time (Notes 4,7,8,14)	+25°C		1.5	2.5		1.5	2.5	µs
Digital Input Current (V_{IN} = 0V)	Full		1	1.5		1	1.5	mA
Digital Input Current (V_{IN} = +5.0V)	Full		5			5		nA
Output Delay (Note 9,14)	+25°C		100	250		100	250	ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90		74	90		dB

NOTES

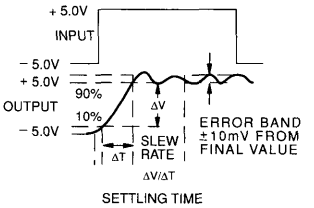
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 5$ Vdc
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2k\Omega$, $C_L = 50$ pF.
4. $A_V = +1$, $C_{COMP} = 15$ pF, $R_L = 2k\Omega$, $C_L = 50$ pF.
5. $V_{OUT} = 20$V peak to peak.
6. $V_{OUT} = 200$ mV peak to peak.
7. $V_{OUT} = 10.0$V peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10$ Vdc.
11. $V_{SUPP} = \pm 10$ Vdc to ± 20 Vdc.
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3 mW/°C above 105°C.
14. Guaranteed but not tested.

TRANSIENT RESPONSE

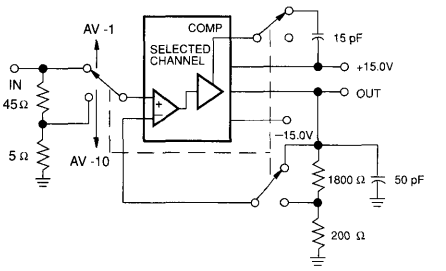


NOTE: Measured on both positive and negative transitions.

SLEW RATE AND SETTLING

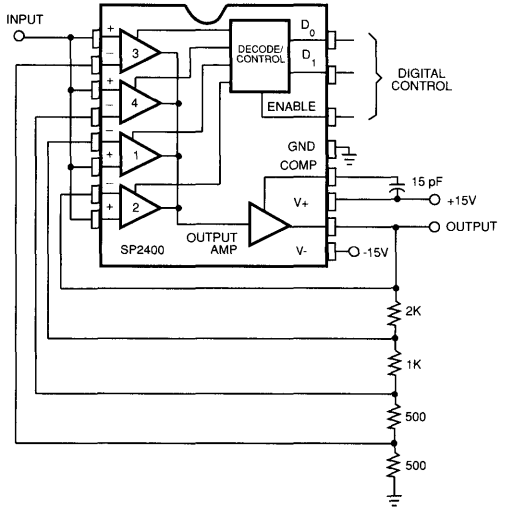


SLEW RATE AND TRANSIENT RESPONSE

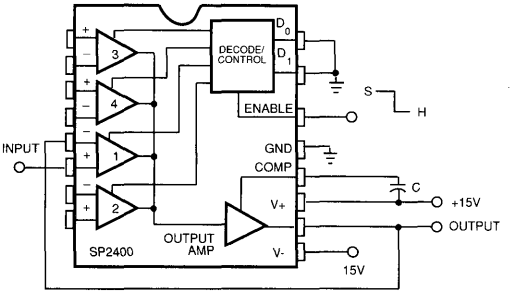


TYPICAL APPLICATIONS

AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN



SAMPLE AND HOLD



Sample charging rate = $\frac{I_1}{C}$ V/sec.

Hold drift rate = $\frac{I_2}{C}$ V/sec.

Switch pedestal error = $\frac{Q}{C}$ Volts.

$I_1 \approx 150 \times 10^{-6}$ A

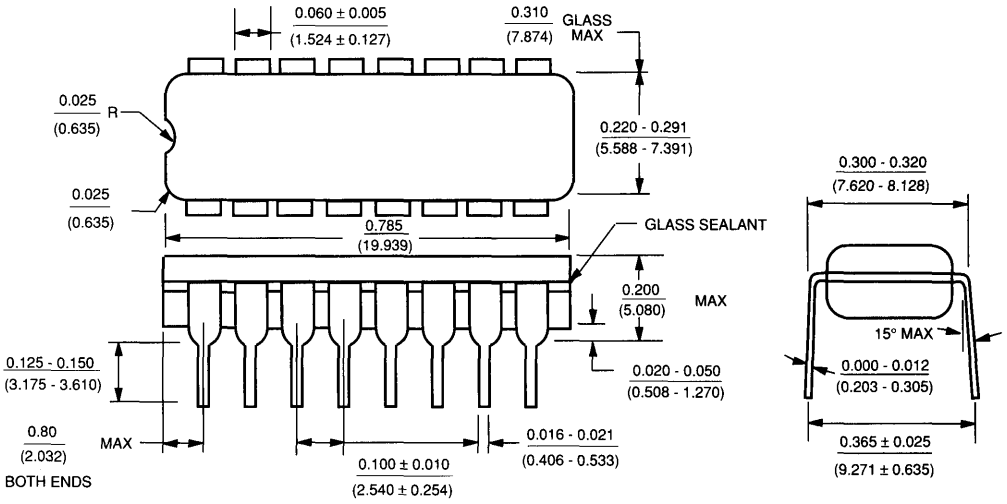
$I_2 \approx 200 \times 10^{-9}$ A @ +25°C

$\approx 600 \times 10^{-9}$ A @ -55°C

$\approx 100 \times 10^{-9}$ A @ +125°C

$Q \approx 2 \times 10^{-12}$ Coul

16 LEAD CERAMIC DIP PACKAGE OUTLINE



SP-2500/02/05

Precision, High Slew Rate Operational Amplifiers

Features

- 30 V/μS Slew Rate
- 10 nA Offset Current
- 330 nS Settling Time To 0.1%
- 500 KHz Full Power Bandwidth
- 12 MHz Typical Gain Bandwidth
- 20 MΩ Minimum Input Impedance
- Internally Compensated

Applications

- Video Amplifiers
- Pulse Amplifiers
- Signal Generators
- High Speed Sample-and-Hold Amplifiers

Description

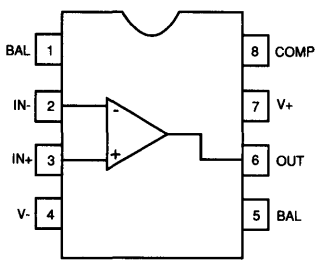
The SP-2500/02/05 operational amplifiers are fast settling, low offset voltage and current,and high slew rate operational amplifiers Their wide bandwidth and high input impedance combined with internal compensation make them excellant choices in high frequency signal conditioning applications.

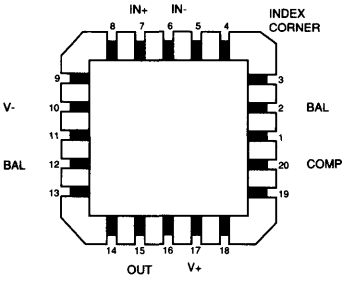
These devices are designed to allow additional compensation and offset trimming. A 100KΩ trim potentiometer is recommended for use between the balance pins (the wiper should be connected to V+).

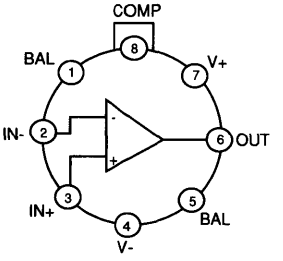
The SP-2502 and SP-2505 are the relaxed specification military temperature range and the commercial temperature range of the SP-2500.

All versions are available in metal can and ceramic mini DIP packages as well as in die form. LCC packaged versions are also available.

Connection Diagrams







SP-2500/02/05

Precision, High Slew Rate Operational Amplifiers

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±15.0V	SP-2500	$-55^oC \le T_A \le 125^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current , I_p	50mA		

Electrical Characteristics: $V^+ = +15V$, $V^- = -15V$, $T_A=25^oC$ unless otherwise specified in "Conditions".

SP-2500

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			2	5	mV
		$-55°C \le T_A \le 125°C$			8	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55°C \le T_A \le 125°C$; average		20		µV/°C
Bias Current	I_B			100	200	nA
		$-55°C \le T_A \le 125°C$			400	nA
Offset Current	I_{OS}			10	25	nA
		$-55°C \le T_A \le 125°C$			50	nA
Input Impedance	Z_{in}	Guaranteed by Design	25	50		MΩ
Common Mode Range	V_{cm}	$-55°C \le T_A \le 125°C$	±10.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm10V$	20K	30K		V/V
		$-55°C \le T_A \le 125°C$, $R_L = 2K\Omega$, $V_O = \pm10V$	15K			V/V
Common Mode Rejection Ratio	CMRR	$-55°C \le T_A \le 125°C$, $V_{cm} = \pm10V$	80	90		dB
Unity Gain Bandwidth Product	GBW	$A_V > 10$		12		MHz
Output Characteristics						
Output Voltage Swing	V_O	$-55°C \le T_A \le 125°C$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm10V$	±10	±20		mA
Full Power Bandwidth	FPBW	$V_O = \pm10V$, FPBW= (SR) $(2\pi V_p)^{-1}$	350	500		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$		25	50	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$		25	40	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$	25	30		V/ S
Settling Time to 0.1%	t_S	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$		0.33		S
Power Supply						
Supply Current	I_S			4	6	mA
Power Supply Rejection Ratio	PSRR	$-55°C \le T_A \le 125°C$, $\Delta V_s = \pm5V$	80	90		dB

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±15.0V	SP-2502	$-55^oC \le T_A \le 125^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current , I_p	50mA		

Electrical Characteristics: $V^+ = +15V$, $V^- = -15V$, $T_A=25^oC$ unless otherwise specified in "Conditions".

SP-2502

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			4	8	mV
		$-55^oC \le T_A \le 125^oC$			10	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^oC \le T_A \le 125^oC$; average		20		µV/°C
Bias Current	I_B			125	250	nA
		$-55^oC \le T_A \le 125^oC$			500	nA
Offset Current	I_{OS}			20	50	nA
		$-55^oC \le T_A \le 125^oC$			100	nA
Input Impedance	Z_{in}	Guaranteed by Design	25	50		MΩ
Common Mode Range	V_{cm}	$-55^oC \le T_A \le 125^oC$	±10.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm10V$	15K	25K		V/V
		$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$, $V_O = \pm10V$	10K			V/V
Common Mode Rejection Ratio	CMRR	$-55^oC \le T_A \le 125^oC$, $V_{cm} = \pm10V$	74	90		dB
Unity Gain Bandwidth Product	GBW	$A_V > 10$		12		MHz
Output Characteristics						
Output Voltage Swing	V_O	$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm10V$	±10	±20		mA
Full Power Bandwidth	FPBW	$V_O = \pm10V$, FPBW= (SR) ($2\pi V_p)^{-1}$	300	500		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$		25	50	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$		25	50	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$	20	30		V/ S
Settling Time to 0.1%	t_S	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$		0.33		S
Power Supply						
Supply Current	I_S			4	6	mA
Power Supply Rejection Ratio	PSRR	$-55^oC \le T_A \le 125^oC$, $\Delta V_s = \pm5V$	74	90		dB

SP-2500/02/05

Precision, High Slew Rate Operational Amplifiers

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±15.0V	SP-2505	$0\ ^oC \le T_A \le 75^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current , I_p	50mA		

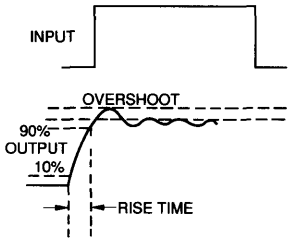
Electrical Characteristics:

$V^+ = +15V$, $V^- = -15V$, $T_A = 25^oC$ unless otherwise specified in "Conditions".

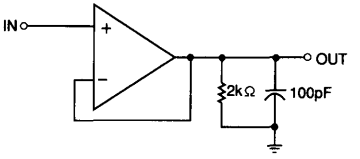
SP-2505

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			4	8	mV
		$0\ ^oC \le T_A \le 75^oC$			10	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$0\ ^oC \le T_A \le 75^oC$; average		20		µV/°C
Bias Current	I_B			125	250	nA
		$0\ ^oC \le T_A \le 75^oC$			500	nA
Offset Current	I_{OS}			20	50	nA
		$0\ ^oC \le T_A \le 75^oC$			100	nA
Input Impedance	Z_{in}	Guaranteed by Design	25	50		MΩ
Common Mode Range	V_{cm}	$0\ ^oC \le T_A \le 75^oC$	±10.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm 10V$	15K	25K		V/V
		$0\ ^oC \le T_A \le 75^oC$, $R_L = 2K\Omega$, $V_O = \pm 10V$	10K			V/V
Common Mode Rejection Ratio	CMRR	$0\ ^oC \le T_A \le 75^oC$, $V_{cm} = \pm 10V$	74	90		dB
Unity Gain Bandwidth Product	GBW	$A_V > 10$		12		MHz
Output Characteristics						
Output Voltage Swing	V_O	$0\ ^oC \le T_A \le 75^oC$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm 10V$	±10	±20		mA
Full Power Bandwidth	FPBW	$V_O = \pm 10V$, $FPBW = (SR)\ (2\pi\ V_p)^{-1}$	300	500		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 200mV$		25	50	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 200mV$		25	50	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 5V$	20	30		V/ S
Settling Time to 0.1%	t_S	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 5V$		0.33		S
Power Supply						
Supply Current	I_S			4	6	mA
Power Supply Rejection Ratio	PSRR	$0\ ^oC \le T_A \le 75^oC$, $\Delta V_s = \pm 5V$	74	90		dB

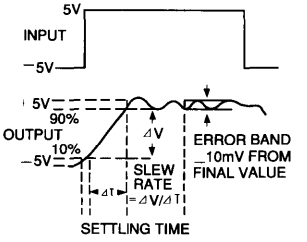
A.C. Performance



Transient Response



A.C. Test Circuit



Slew Rate/Settling Time

Ordering Information

When ordering the SP-2500/02/05, specify the package and screening according to the following :

SP 2 - 2500 - 2

Prefix: SP (SIPEX)

Generic Part #

PACKAGE :

SCREENING

1 - 14 pin ceramic DIP	-2 : -55 °C to 125 °C
2 - Metal Can	-4 : -25 °C to 85 °C
3 - 8 Pin Plastic DIP	-5 : 0 °C to 75 °C
4 - 20 Pin LCC	-6 : 25 °C 100% D.C. Probe
7 - 8-Pin CERDIP	(Dice Only)
0 - DICE	/883 : -55 °C to 125 °C
	Full Mil Processing

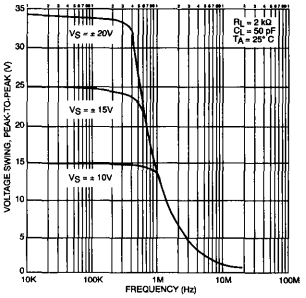
NOTES: 1. Not all package types and screening option combinations are available. Consult local sales office or factory for availability information.

2. Consult factory for special package or screening requirements.

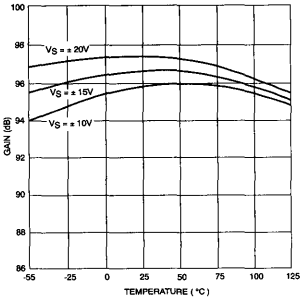
3. Consult factory for 883 revision C compliant data sheet.

4. Consult factory for package mechanical dimensions.

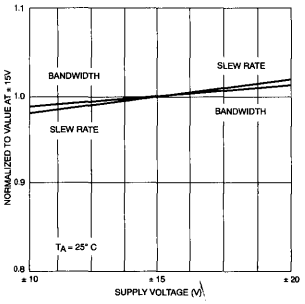
OUTPUT VOLTAGE SWING vs. FREQUENCY



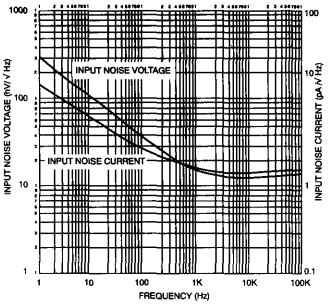
OPEN-LOOP VOLTAGE GAIN vs. TEMPERATURE



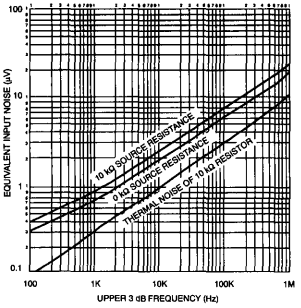
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



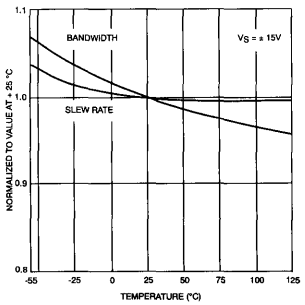
INPUT NOISE DENSITY vs. FREQUENCY



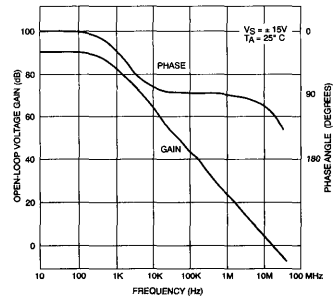
BROADBAND NOISE CHARACTERISTICS



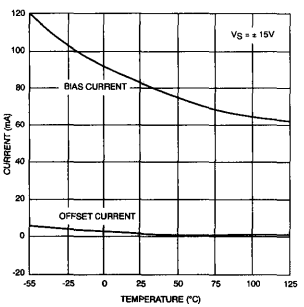
NORMALIZED AC PARAMETERS vs. TEMPERATURE



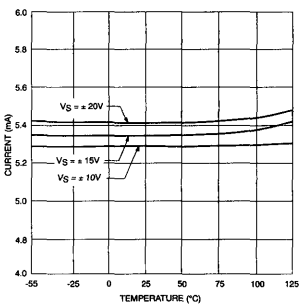
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



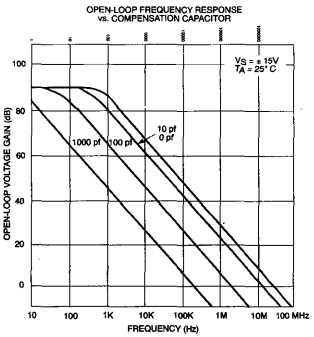
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



POWER SUPPLY CURRENT vs. TEMPERATURE



OPEN-LOOP FREQUENCY RESPONSE
vs. COMPENSATION CAPACITOR



Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP-2510/12/15

High Slew Rate Operational Amplifiers

Features

- 65 V/μS Slew Rate
- 250 nS Settling Time to 0.1%
- 1 MHz Full Power Bandwidth
- 12 MHz Gain Bandwidth
- 100 MΩ Input Impedance
- Internally Compensated

Applications

- Video Amplifiers
- Pulse Amplifiers
- Signal Generators
- High Speed Sample-and-Hold Amplifiers

Description

The SP-2510/12/15 operational amplifiers are optimally compensated for bandwidth, slew rate, and settling time. These characteristics make these devices the preferred candidates for high accuracy and high frequency analog signal processing applications.

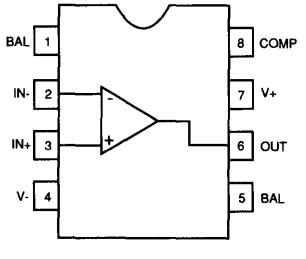
These devices are designed to allow additional compensation and offset trimming. A 100KΩ trim potentiometer is recommended for use between the balance pins (the wiper should be connected to V+).

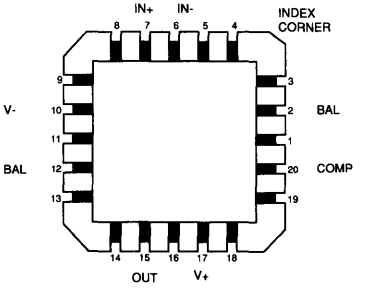
The SP-2512 and SP-2515 are the relaxed specification military temperature range and the commercial temperature range of the SP-2510.

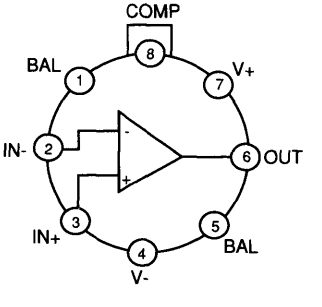
All versions are available in metal can, ceramic mini DIP packages, and in die form. The SP-2510 is also available in ceramic LCC packages.

4

Connection Diagrams







SP-2510/12/15

High Slew Rate Operational Amplifiers

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±15.0V	SP-2510	$-55^oC \le T_A \le 125^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current , I_p	50mA		

Electrical Characteristics:

$V^+ = +15V$, $V^- = -15V$, $T_A=25^oC$ unless otherwise specified in "Conditions".

SP-2510

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			4	8	mV
		$-55^oC \le T_A \le 125^oC$			11	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^oC \le T_A \le 125^oC$; average		20		µV/°C
Bias Current	I_B			100	200	nA
		$-55^oC \le T_A \le 125^oC$			400	nA
Offset Current	I_{OS}			10	25	nA
		$-55^oC \le T_A \le 125^oC$			50	nA
Input Impedance	Z_{in}	Guaranteed by Design	50	100		MΩ
Common Mode Range	V_{cm}	$-55^oC \le T_A \le 125^oC$	±10.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm10V$	10K	15K		V/V
		$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$, $V_O = \pm10V$	7.5K			V/V
Common Mode Rejection Ratio	CMRR	$-55^oC \le T_A \le 125^oC$, $V_{cm} = \pm10V$	80	90		dB
Unity Gain Bandwidth Product	GBW	$A_V > 10$		12		MHz
Output Characteristics						
Output Voltage Swing	V_O	$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm10V$	±10	±20		mA
Full Power Bandwidth	FPBW	$V_O = \pm10V$, $FPBW = (SR)\,(2\pi V_p)^{-1}$	750	1000		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$		25	50	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$		25	40	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$	50	65		V/ S
Settling Time to 0.1%	t_S	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$		0.25		S
Power Supply						
Supply Current	I_S			4	6	mA
Power Supply Rejection Ratio	PSRR	$-55^oC \le T_A \le 125^oC$	80	90		dB

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±15.0V	SP-2512	$-55^oC \le T_A \le 125^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current , I_p	50mA		

Electrical Characteristics:

$V^+ = +15V$, $V^- = -15V$, $T_A=25^oC$ unless otherwise specified in "Conditions".

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SP-2512

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			5	10	mV
		$-55^oC \le T_A \le 125^oC$			14	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^oC \le T_A \le 125^oC$; average		25		µV/°C
Bias Current	I_B			125	250	nA
		$-55^oC \le T_A \le 125^oC$			500	nA
Offset Current	I_{OS}			20	50	nA
		$-55^oC \le T_A \le 125^oC$			100	nA
Input Impedance	Z_{in}	Guaranteed by Design	40	100		MΩ
Common Mode Range	V_{cm}	$-55^oC \le T_A \le 125^oC$	±10.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm10V$	7.5K	15K		V/V
		$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$, $V_O = \pm10V$	5K			V/V
Common Mode Rejection Ratio	CMRR	$-55^oC \le T_A \le 125^oC$, $V_{cm} = \pm10V$	74	90		dB
Unity Gain Bandwidth Product	GBW	$A_V > 10$		12		MHz
Output Characteristics						
Output Voltage Swing	V_O	$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm10V$	±10	±20		mA
Full Power Bandwidth	FPBW	$V_O = \pm10V$, FPBW= (SR) $(2\pi V_p)^{-1}$	600	1000		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$		25	50	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$		25	50	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$	40	60		V/ S
Settling Time to 0.1%	t_S	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$		0.25		S
Power Supply						
Supply Current	I_S			4	6	mA
Power Supply Rejection Ratio	PSRR	$-55^oC \le T_A \le 125^oC$	74	90		dB

SP-2510/12/15

High Slew Rate Operational Amplifiers

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±15.0V	SP-2515	$0\ ^oC \le T_A \le 75^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current , I_p	50mA		

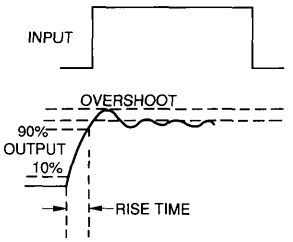
Electrical Characteristics:

$V^+ = +15V$, $V^- = -15V$, $T_A = 25^oC$ unless otherwise specified in "Conditions".

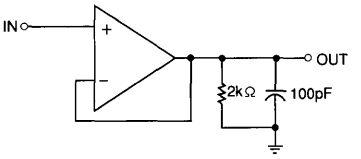
SP-2515

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			5	10	mV
		$0\ ^oC \le T_A \le 75\ ^oC$			14	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$0\ ^oC \le T_A \le 75\ ^oC$; average		30		µV/°C
Bias Current	I_B			125	250	nA
		$0\ ^oC \le T_A \le 75\ ^oC$			500	nA
Offset Current	I_{OS}			20	50	nA
		$0\ ^oC \le T_A \le 75\ ^oC$			100	nA
Input Impedance	Z_{in}	Guaranteed by Design	40	100		MΩ
Common Mode Range	V_{cm}	$0\ ^oC \le T_A \le 75\ ^oC$	±10.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm 10V$	7.5K	15K		V/V
		$0\ ^oC \le T_A \le 75\ ^oC$, $R_L = 2K\Omega$, $V_O = \pm 10V$	5K			V/V
Common Mode Rejection Ratio	CMRR	$0\ ^oC \le T_A \le 75\ ^oC$, $V_{cm} = \pm 10V$	74	90		dB
Unity Gain Bandwidth Product	GBW	$A_V > 10$		12		MHz
Output Characteristics						
Output Voltage Swing	V_O	$0\ ^oC \le T_A \le 75\ ^oC$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm 10V$	±10	±20		mA
Full Power Bandwidth	FPBW	$V_O = \pm 10V$, $FPBW = (SR)\ (2\pi\ V_p)^{-1}$	600	1000		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 200mV$		25	50	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 200mV$		25	50	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 5V$	40	60		V/ S
Settling Time to 0.1%	t_S	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 5V$		0.25		S
Power Supply						
Supply Current	I_S			4	6	mA
Power Supply Rejection Ratio	PSRR	$0\ ^oC \le T_A \le 75\ ^oC$	74	90		dB

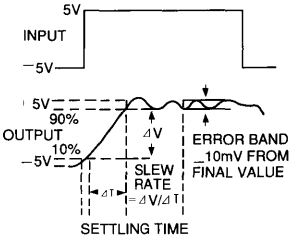
A.C. Performance



Transient Response



A.C. Test Circuit



Slew Rate/Settling Time

Ordering Information

When ordering the SP-2510/12/15, specify the package and screening according to the following :

SP 2 - 2510 - 2

Prefix: SP (SIPEX) — Generic Part # — PACKAGE : — SCREENING

PACKAGE :	SCREENING	
1 - 14 pin ceramic DIP	-2 :	-55 °C to 125 °C
2 - Metal Can	-4 :	-25 °C to 85 °C
3 - 8 Pin Plastic DIP	-5 :	0 °C to 75 °C
4 - 20 Pin LCC	-6 :	25 °C 100% D.C. Probe (Dice Only)
7 - 8-Pin CERDIP		
0 - DICE	/883 :	-55 °C to 125 °C Full Mil Processing

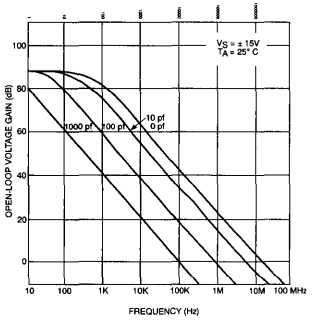
NOTES: 1. Not all package types and screening option combinations are available. Consult local sales office or factory for availability information.

2. Consult factory for special package or screening requirements.

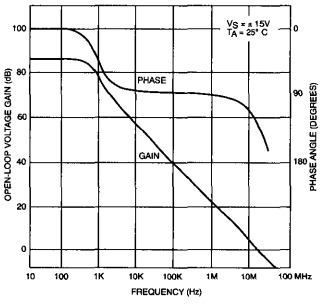
3. Consult factory for 883 revision C compliant data sheet.

4. Consult factory for package mechanical dimensions.

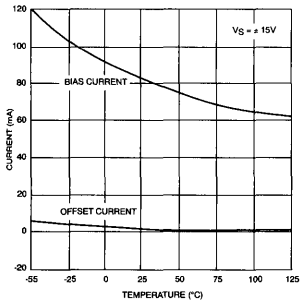
OPEN-LOOP FREQUENCY RESPONSE vs. COMPENSATION CAPACITOR



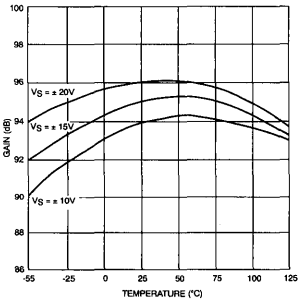
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



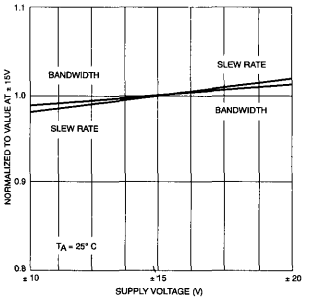
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



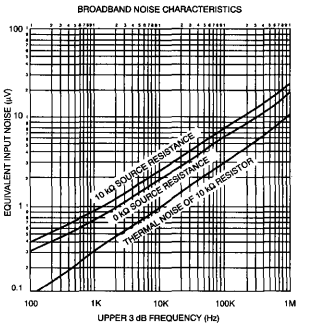
OPEN-LOOP VOLTAGE GAIN vs. TEMPERATURE



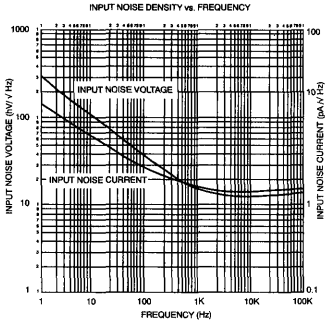
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



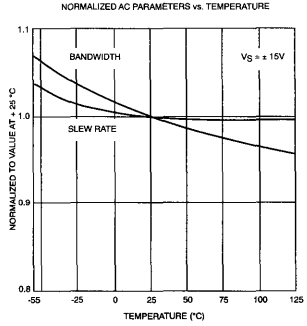
BROADBAND NOISE CHARACTERISTICS



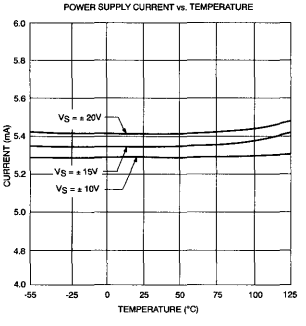
INPUT NOISE DENSITY vs. FREQUENCY



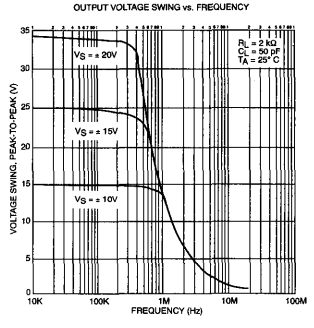
NORMALIZED AC PARAMETERS vs. TEMPERATURE



POWER SUPPLY CURRENT vs. TEMPERATURE



OUTPUT VOLTAGE SWING vs. FREQUENCY



Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP-2520/22/25

Uncompensated, High Slew Rate Operational Amplifiers

Features

- 120 V/µS Slew Rate
- 200 nS Settling Time to 0.1%
- 2.0 MHz Full Power Bandwidth
- 20 MHz Gain Bandwidth

Applications

- Video Amplifiers
- Pulse Amplifiers
- Signal Generators
- High Speed Sample-and-Hold Amplifiers

Description

The SP-2520/22/25 are high slew rate, wide bandwidth operational amplifiers which are stable at closed loop gains of 3 or greater without external compensation. These devices also exhibit fast settling times, high input impedance, and low input offset currents. These characteristics combine to make the SP-2520/22/25 prime candidates for high frequency analog processing applications.

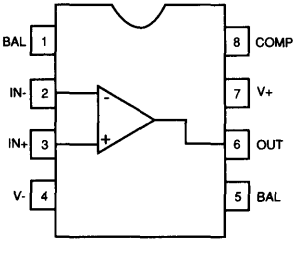
These amplifiers provide the designer with the ability to tailor its transfer characteristics through compensation. Offsets can be trimmed by connecting a nulling potentiometer between its balance pins, and connecting the wiper to the positive supply, V^+. A 200KΩ potentiometer is recommended.

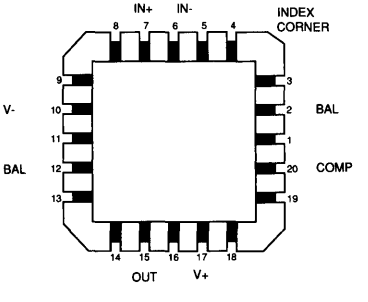
The SP-2522 and SP-2525 are the relaxed specification military temperature range and the commercial temperature range of the SP-2520.

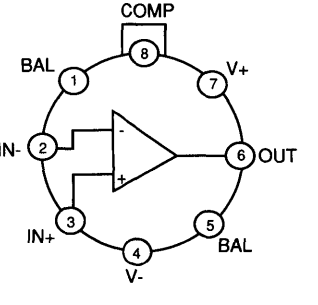
All versions are available in metal can, ceramic mini DIP packages, and in die form. The SP-2520 is also available in ceramic LCC packages.

4

Connection Diagrams







SP-2520/22/25

Uncompensated, High Slew Rate Operational Amplifiers

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±15.0V	SP-2520	$-55^oC \le T_A \le 125^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current , I_p	50mA		

Electrical Characteristics:

$V^+ = +15V$, $V^- = -15V$, $T_A = 25^oC$ unless otherwise specified in "Conditions".

SP-2520

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			4	8	mV
		$-55^oC \le T_A \le 125^oC$			11	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^oC \le T_A \le 125^oC$; average		20		µV/°C
Bias Current	I_B			100	200	nA
		$-55^oC \le T_A \le 125^oC$			400	nA
Offset Current	I_{OS}			10	25	nA
		$-55^oC \le T_A \le 125^oC$			50	nA
Input Impedance	Z_{in}	Guaranteed by Design	50	100		MΩ
Common Mode Range	V_{cm}	$-55^oC \le T_A \le 125^oC$	±10.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm 10V$	10K	15K		V/V
		$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$, $V_O = \pm 10V$	7.5K			V/V
Common Mode Rejection Ratio	CMRR	$-55^oC \le T_A \le 125^oC$, $V_{cm} = \pm 10V$	80	90		dB
Gain Bandwidth Product	GBW	$A_V > 10$, Guaranteed by Design	10	20		MHz
Output Characteristics						
Output Voltage Swing	V_O	$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm 10V$	±10	±20		mA
Full Power Bandwidth	FPBW	$V_O = \pm 10V$, FPBW= (SR) $(2\pi V_p)^{-1}$	1500	2000		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 200mV$, $A_V = 3$		25	50	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 200mV$, $A_V = 3$		25	40	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 5V$, $A_V = 3$	±100	120		V/ S
Settling Time to 0.1%	t_S	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 5V$, $A_V = 3$		0.20		µS
Power Supply						
Supply Current	I_S			4	6	mA
Power Supply Rejection Ratio	PSRR	$-55^oC \le T_A \le 125^oC$, $\Delta V_s = \pm 5V$	80	90		dB

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±15.0V	SP-2522	$-55^oC \le T_A \le 125^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current , I_p	50mA		

Electrical Characteristics:

$V^+ = +15V$, $V^- = -15V$, $T_A=25^oC$ unless otherwise specified in "Conditions".

SP-2522

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			5	10	mV
		$-55^oC \le T_A \le 125^oC$			14	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^oC \le T_A \le 125^oC$; average		25		µV/°C
Bias Current	I_B			125	250	nA
		$-55^oC \le T_A \le 125^oC$			500	nA
Offset Current	I_{OS}			20	50	nA
		$-55^oC \le T_A \le 125^oC$			100	nA
Input Impedance	Z_{in}	Guaranteed by Design	40	100		MΩ
Common Mode Range	V_{cm}	$-55^oC \le T_A \le 125^oC$	±10.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm10V$	7.5K	15K		V/V
		$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$, $V_O = \pm10V$	5K			V/V
Common Mode Rejection Ratio	CMRR	$-55^oC \le T_A \le 125^oC$, $V_{cm} = \pm10V$	74	90		dB
Gain Bandwidth Product	GBW	$A_V > 10$, Guaranteed by Design	10	20		MHz
Output Characteristics						
Output Voltage Swing	V_O	$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm10V$	±10	±20		mA
Full Power Bandwidth	FPBW	$V_O = \pm10V$, FPBW= (SR) ($2\pi V_p)^{-1}$	1200	1600		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$, $A_V = 3$		25	50	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$, $A_V = 3$		25	50	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$, $A_V = 3$	±80	120		V/ S
Settling Time to 0.1%	t_S	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$, $A_V = 3$		0.20		µS
Power Supply						
Supply Current	I_S			4	6	mA
Power Supply Rejection Ratio	PSRR	$-55^oC \le T_A \le 125^oC$, $\Delta V_s = \pm5V$	74	90		dB

SP-2520/22/25

Uncompensated, High Slew Rate Operational Amplifiers

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±15.0V	SP-2525	$0\,^oC \le T_A \le 75^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current , I_p	50mA		

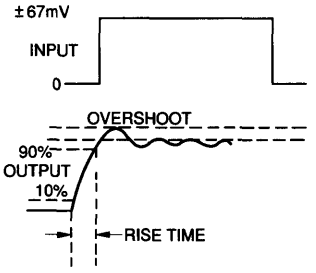
Electrical Characteristics:

$V^+ = +15V$, $V^- = -15V$, $T_A = 25^oC$ unless otherwise specified in "Conditions".

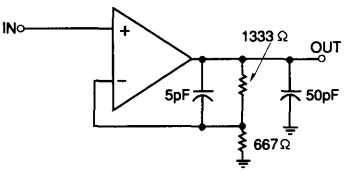
SP-2525

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Chars.						
Offset Voltage	V_{OS}			5	10	mV
		$0\,^oC \le T_A \le 75^oC$			14	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$0\,^oC \le T_A \le 75^oC$; average		30		µV/°C
Bias Current	I_B			125	250	nA
		$0\,^oC \le T_A \le 75^oC$			500	nA
Offset Current	I_{OS}			20	50	nA
		$0\,^oC \le T_A \le 75^oC$			100	nA
Input Impedance	Z_{in}	Guaranteed by Design	40	100		MΩ
Common Mode Range	V_{cm}	$0\,^oC \le T_A \le 75^oC$	±10.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm 10V$	7.5K	15K		V/V
		$0\,^oC \le T_A \le 75^oC$, $R_L = 2K\Omega$, $V_O = \pm 10V$	5K			V/V
Common Mode Rejection Ratio	CMRR	$0\,^oC \le T_A \le 75^oC$, $V_{cm} = \pm 10V$	74	90		dB
Gain Bandwidth Product	GBW	$A_V > 10$, Guaranteed by Design	10	20		MHz
Output Characteristics						
Output Voltage Swing	V_O	$0\,^oC \le T_A \le 75^oC$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm 10V$	±10	±20		mA
Full Power Bandwidth	FPBW	$V_O = \pm 10V$, $FPBW = (SR)\,(2\pi V_p)^{-1}$	1200	1600		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 200mV$, $A_V = 3$		25	50	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 200mV$, $A_V = 3$		25	50	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 5V$, $A_V = 3$	±80	120		V/S
Settling Time to 0.1%	t_S	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm 5V$, $A_V = 3$		0.20		µS
Power Supply						
Supply Current	I_S			4	6	mA
Power Supply Rejection Ratio	PSRR	$0\,^oC \le T_A \le 75^oC$, $\Delta V_s = \pm 5V$	74	90		dB

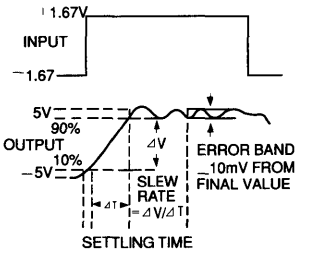
A.C. Performance



Transient Response



A.C. Test Circuit



Slew Rate/Settling Time

Ordering Information

When ordering the SP-2520/22/25, specify the package and screening according to the following :

SP 2 - 2520 - 2

Prefix: SP (SIPEX)

Generic Part #

PACKAGE :

SCREENING

1 - 14 pin ceramic DIP	-2 : -55 °C to 125 °C
2 - Metal Can	-4 : -25 °C to 85 °C
3 - 8 Pin Plastic DIP	-5 : 0 °C to 75 °C
4 - 20 Pin LCC	-6 : 25 °C 100% D.C. Probe
7 - 8-Pin CERDIP	(Dice Only)
0 - DICE	/883 : -55 °C to 125 °C
	Full Mil Processing

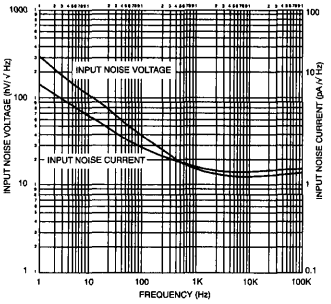
NOTES:1. Not all package types and screening option combinations are available. Consult local sales office or factory for availability information.

2. Consult factory for special package or screening requirements.

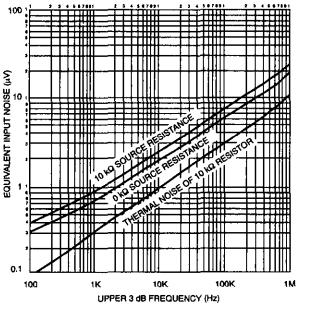
3. Consult factory for 883 revision C compliant data sheet.

4. Consult factory for package mechanical dimensions.

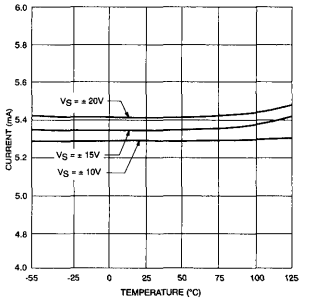
INPUT NOISE DENSITY vs. FREQUENCY



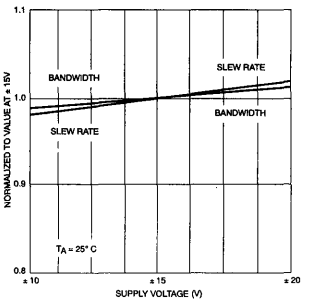
BROADBAND NOISE CHARACTERISTICS



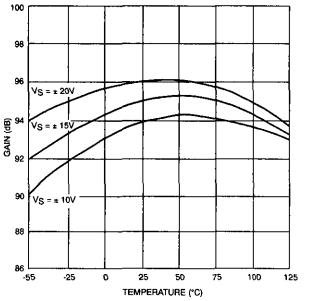
POWER SUPPLY CURRENT vs. TEMPERATURE



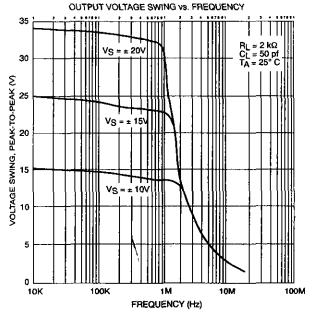
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



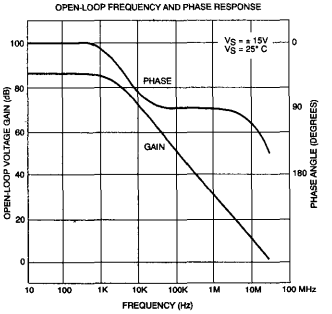
OPEN-LOOP VOLTAGE GAIN vs. TEMPERATURE



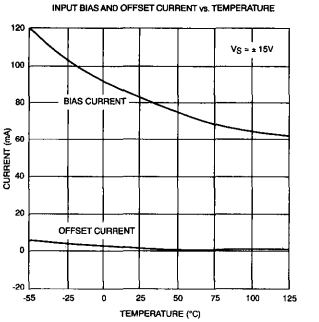
OUTPUT VOLTAGE SWING vs. FREQUENCY



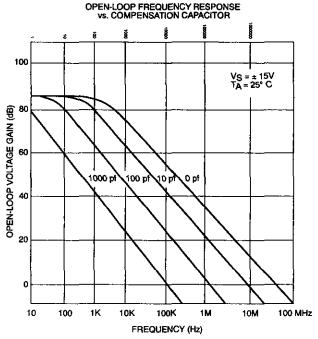
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



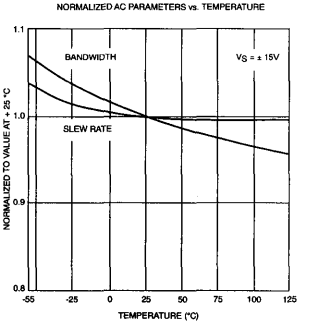
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



OPEN-LOOP FREQUENCY RESPONSE vs. COMPENSATION CAPACITOR



NORMALIZED AC PARAMETERS vs. TEMPERATURE



VERY HIGH SLEW RATE WIDEBAND OPERATIONAL AMPLIFIERS

FEATURES

- Very High Slew Rate 600V/µs
- Open Loop Gain 15 kV/V
- Wide Gain-Bandwidth 600 MHz
- Power Bandwidth 9.5 MHz
- Low Offset Voltage 3 mV
- Input Voltage Noise 6 nV/√Hz
- Output Voltage Swing ±10V

PRELIMINARY SPECIFICATION

APPLICATIONS

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

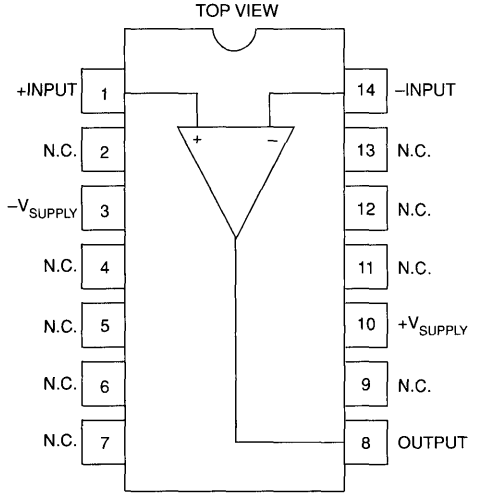
DESCRIPTION

The SP2539 represents the ultimate in high slew rate wideband, monolithic, operational amplifiers. It has been designed and constructed with Sipex high frequency Bipolar dielectric isolation process and features dynamic parameters never before available from a truly differential device.

With a 600 V/µs slew rate and a 600 MHz gain-band-width-product, the SP2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full ±10V swing coupled with outstanding A.C. parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

The SP2539 is available in the 14 pin ceramic and epoxy packages, as well as a 20 pin LCC package. The SP2539-2 denotes -55°C to ±125°C operation while the SP2539-5 operates over the 0°C to ±75°C range.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

Voltage between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current ..... 50 mA (Peak)
Internal Power Dissipation[2] ..... 870 mW (Cerdip)

Operating Temperature Range:
(SP2539-2) ..... $-55°C \le T_A \le +125°C$
(SP2539-5) ..... $0°C \le T_A \le +75°C$
Maximum Storage Temperature Range .... $-65°C \le T_A < +150°C$

ELECTRICAL CHARACTERISTICS

$V_{SUPPLY} = \pm 15$ Volts, $R_L = 1$ Kohms, unless otherwise specified.

			SP2539-2 -55°C to +125°C			SP2539-5 0°C to +75°C			
PARAMETERS	**CONDITIONS**	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT CHARACTERISTICS									
Offset Voltage		25°C		8	10		8	15	mV
		Full		13	15			20	mV
Average Offset Voltage Drift		Full		20			20		µV/°C
Bias Current		25°C		5	20		5	20	µA
		Full			25			25	µA
Offset Current		25°C		1	6		1	6	µA
		Full			8			8	µA
Input Resistance		25°C		10			10		Kohms
Input Capacitance		25°C		1.0			1.0		pF
Common Mode Range		Full	±10			±10			V
Input Noise Voltage (f = 1 kHz, $R_g = 0\Omega$)		25°C		6			6		nV/√Hz
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$R_L = 1$ KΩ, $V_O = \pm 10V$	25°C	10K	15K		10K	15K		V/V
		Full	5K			5K			V/V
Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	Full	60			60			dB
Gain Bandwidth Product	$V_O = 90$ mV $A_V = 10$	25°C		600			600		MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 1$ KΩ, $V_O = \pm 10V$	Full	±10			±10			V
Output Current	$R_L = 1$ KΩ, $V_O = \pm 10V$	25°C	10			10			mA
Output Resistance		25°C		30			30		Ohms
Full Power Bandwidth Full power bandwidth guaranteed based on slew rate measurement using FPBW= Slew Rate/2π Vpeak.	$R_L = 1$ KΩ, $V_O = \pm 10V$	25°C	8.7	9.5		8.7	9.5		MHz
TRANSIENT RESPONSE	Refer to Test Ckts Section of data sheet								
Rise Time		25°C		7			7		nS
Overshoot		25°C		15			15		%
Slew Rate		25°C	550	600		550	600		V/µs
Settling Time: 10V Step to 0.1%		25°C		200			200		nS
POWER REQUIREMENTS									
Supply Current		Full		20	25		20	25	mA
Power Supply Rejection Ratio[3]		Full	60			60			dB

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7 mV/°C for operation at ambient temperatures above +75°C. Heat sinking required at temperatures above +75°C. $T_{JA} = 115°C/W$; $T_{JC} = 35°C/W$. Thermalloy model 6007 heat sink recommended.
3. $V_{SUPPLY} = \pm 5$ Vdc to ±15 Vdc.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP2540

WIDEBAND, FAST SETTLING OPERATIONAL AMPLIFIERS

FEATURES

- Very High Slew Rate 400V/µs
- Open Loop Gain 200 ns
- Wide Gain-Bandwidth 400 MHz
- Power Bandwidth 6 MHz
- Low Offset Voltage 8 mV
- Input Voltage Noise 6 nV/√Hz
- Output Voltage Swing ±10V
- Monolithic Bipolar Construction

PRELIMINARY SPECIFICATION

APPLICATIONS

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

DESCRIPTION

The SP2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance in circuits where closed loop gain is 10 or greater. Additionally, the SP2540 has a drive capability of ±10V into a 1 Kohm load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

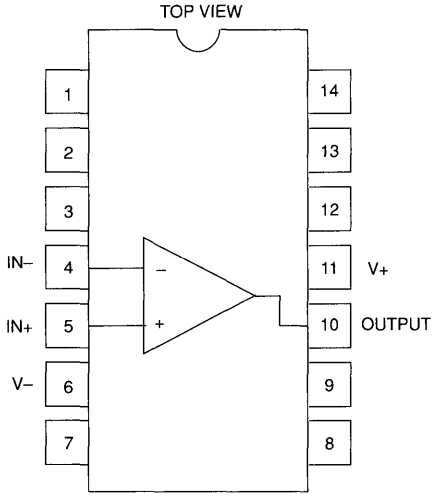
A 400V/µs slew rate ensures high performance in video and pulse amplification circuits, while the 400 MHz gain-band-width-product is ideally suited for wideband signal amplification. A settling time of 200 ns also makes the SP2540 an excellent selection for high speed Data Acquisition Systems.

The SP2540-2 is specified over the -55°C to ±125°C range while the SP2540-5 is specified from 0°C to +75°C.

The SP2540 is available in 14 pin ceramic and epoxy packages, as well as a 20 pin LCC package.

4

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

Voltage between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current ..... 50 mA (Peak)
Internal Power Dissipation[2] ..... 870 mW (Cerdip)

Operating Temperature Range:
(SP2540-2) ..... $-55°C \le T_A \le +125°C$
(SP2540-5) ..... $0°C \le T_A \le +75°C$
Maximum Storage Temperature Range .... $-65°C \le T_A < +150°C$

ELECTRICAL CHARACTERISTICS

$V_{SUPPLY} = \pm 15$ Volts, $R_L = 1$ Kohms, unless otherwise specified.

			SP2540-2 -55°C to +125°C			SP2540-5 0°C to +75°C			
PARAMETERS	**CONDITIONS**	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT CHARACTERISTICS									
Offset Voltage		25°C		8	10		8	15	mV
		Full		13	15			20	mV
Average Offset Voltage Drift		Full		20			20		µV/°C
Bias Current		25°C		5	20		5	20	µA
		Full			25			25	µA
Offset Current		25°C		1	6		1	6	µA
		Full			8			8	µA
Input Resistance		25°C		10			10		Kohms
Input Capacitance		25°C		1.0			1.0		pF
Common Mode Range		Full	±10			±10			V
Input Noise Voltage (f = 1 kHz, $R_g = 0\Omega$)		25°C		6			6		nV/√Hz
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$R_L = 1\ K\Omega$, $V_O = \pm 10V$	25°C	10K	15K		10K	15K		V/V
		Full	5K			5K			V/V
Common Mode Rejection Ratio	$V_{CM} = \pm 10V$	Full	60			60			dB
Gain Bandwidth Product	$V_O = 90$ mV, $A_V = 10$	25°C		400			400		MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 1\ K\Omega$, $V_O = \pm 10V$	Full	±10			±10			V
Output Current	$R_L = 1\ K\Omega$, $V_O = \pm 10V$	25°C	10			10			mA
Output Resistance		25°C		30			30		Ohms
Full Power Bandwidth	$R_L = 1\ K\Omega$, $V_O = \pm 10V$	25°C	5.5	6		5.5	6		MHz
Full power bandwidth guaranteed based on slew rate measurement using FPBW= Slew Rate/2π Vpeak.									
TRANSIENT RESPONSE	Refer to Test Ckts Section of data sheet								
Rise Time		25°C		14			14		nS
Overshoot		25°C		5			5		%
Slew Rate		25°C	350	400		350	400		V/µs
Settling Time:									
10V Step to 0.1%		25°C		200			200		nS
POWER REQUIREMENTS									
Supply Current		Full		20	25		20	25	mA
Power Supply Rejection Ratio[3]		Full	60			60			dB

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7 mV/°C for operation at ambient temperatures above +75°C. Heat sinking required at temperatures above +75°C. $T_{JA} = 115°C/W$; $T_{JC} = 35°C/W$. Thermalloy model 6007 heat sink recommended.
3. $V_{SUPPLY} = \pm 5$ Vdc to ±15 Vdc.

SP-2541

Wideband, Fast Settling, Unity Gain Stable Operational Amplifiers

PRELIMINARY

Features

- 40 MHz Unity Gain Bandwidth
- 280 V/μS Slew Rate
- 90 nS Settling Time
- 4 MHz Power Bandwidth
- Unity Gain Stable
- Internally Compensated

Applications

- Video Amplifiers
- Pulse Amplifiers
- High Speed Sample-and-Hold Amplifiers
- D/A Output Buffers
- A/D Input Buffers

Description

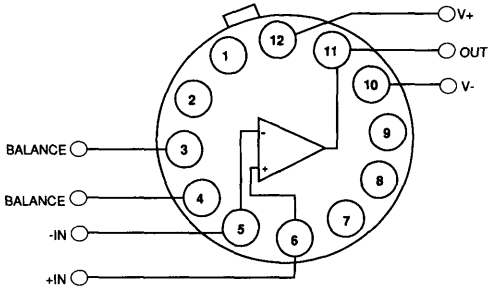
The SP-2541 is a monolithic operational amplifier which is unity gain stable at 40 MHz. The SP-2541 is internally compensated for ease of application, and offers quick settling time and high slew rate to complement its wide bandwidth.

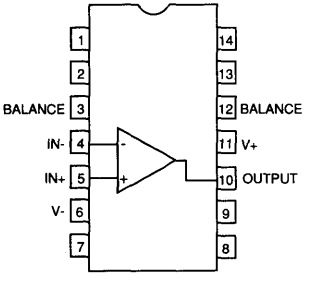
The SP-2541 can be offset trimmed using a 5KΩ trim potentiometer between the balance pins and by connecting the wiper to the positive supply, V^+.

The SP-2541 is available as a full military temperature range version (SP-2541-2) or as a lower cost version specified over the commercial temperature range (SP-2541-5).

These devices are available in metal can, ceramic DIP packages, or in die form.

Connection Diagrams





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Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP-2600/02/05

Wideband, Precision Operational Amplifiers

Features

- 12 MHz Unity Gain Bandwidth Product
- 500 MΩ Input Impedance
- 500 μV Input Offset Voltage
- 150K V/V Open Loop Voltage Gain

Applications

- Video Amplifiers
- Pulse Amplifiers
- High Speed, Precision Comparators
- DAC Buffers
- High Speed Sample-and-Hold Amplifiers

Description

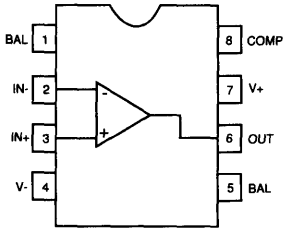
The SP-2600/02/05 are internally compensated, bipolar operational amplifiers. Their wide bandwidth and high input impedance combine with low offset current to make them excellant candidates for high-gain amplification of analog signals; specifically signals comprised of high frequencies.

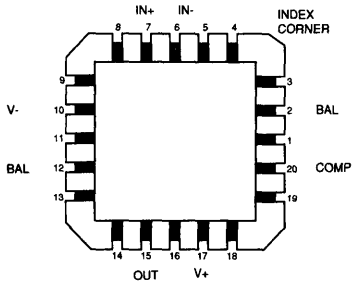
This operational amplifier provides the designer with the opportunity to supplement the compensation (pin 8) where the application requires it. Offsets can also be trimmed by attaching an external nulling potentiometer between the balance pins (pins 1 and 5) and by connecting the wiper to the positive supply, V^+. A 100KΩ potentiometer is recommended.

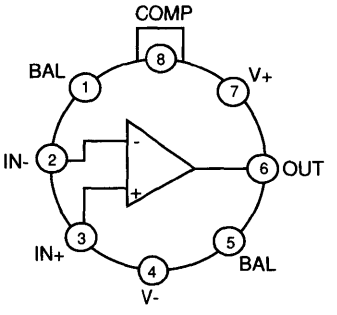
The SP-2600 and SP-2602 are offered as military (-55°C to 125°C) versions; both are available in metal can, ceramic mini DIP and LCC packages as well as in die form. The SP-2605 is offered in plastic, ceramic mini DIP, and metal can packages as well as in die forms.

4

Connection Diagrams







SP-2600/02/05

Wideband, Precision Operational Amplifiers

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	45.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±12.0V	SP-2600	$-55^oC \le T_A \le 125^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current	Full Short Circuit Protection		

Electrical Characteristics: $V^+ = +15V$, $V^- = -15V$, $T_A=25^oC$ unless otherwise specified in "Conditions".

SP-2600

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			0.5	4	mV
		$-55^oC \le T_A \le 125^oC$		2	6	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^oC \le T_A \le 125^oC$; average		5		µV/°C
Bias Current	I_B			1	10	nA
		$-55^oC \le T_A \le 125^oC$		10	30	nA
Offset Current	I_{OS}			1	10	nA
		$-55^oC \le T_A \le 125^oC$		5	30	nA
Input Impedance	Z_{in}	Guaranteed by Design	100	500		MΩ
Common Mode Range	V_{cm}	$-55^oC \le T_A \le 125^oC$	±11.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm10V$	100K	150K		V/V
		$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$, $V_O = \pm10V$	70K			V/V
Common Mode Rejection Ratio	CMRR	$-55^oC \le T_A \le 125^oC$, $V_{cm} = \pm10V$	80	100		dB
Unity Gain Bandwidth Product	GBW	$V_{OL} < 90mV$		12		MHz
Output Characteristics						
Output Voltage Swing	V_O	$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm10V$	±15	±22		mA
Full Power Bandwidth	FPBW	$V_O = \pm10V$, FPBW= (SR) $(2\pi V_p)^{-1}$	50	75		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm200mV$		30	60	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm200mV$		25	40	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm5V$	±4	±7		V/µS
Settling Time	t_S	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm5V$		1.5		S
Power Supply						
Supply Current	I_S			3.0	3.7	mA
Power Supply Rejection Ratio	PSRR	$-55^oC \le T_A \le 125^oC$, $\Delta V_s = \pm5V$	80	90		dB

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	45.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±12.0V	SP-2602	$-55^oC \le T_A \le 125^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current	Full Short Circuit Protection		

Electrical Characteristics: $V^+ = +15V, V^- = -15V$, $T_A = 25^oC$ unless otherwise specified in "Conditions".

SP-2602

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			3	5	mV
		$-55^oC \le T_A \le 125^oC$			7	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^oC \le T_A \le 125^oC$; average		5		µV/°C
Bias Current	I_B			15	25	nA
		$-55^oC \le T_A \le 125^oC$			60	nA
Offset Current	I_{OS}			5	25	nA
		$-55^oC \le T_A \le 125^oC$			60	nA
Input Impedance	Z_{in}	Guaranteed by Design	40	300		MΩ
Common Mode Range	V_{cm}	$-55^oC \le T_A \le 125^oC$	±11.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm 10V$	80K	150K		V/V
		$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$, $V_O = \pm 10V$	60K			V/V
Common Mode Rejection Ratio	CMRR	$-55^oC \le T_A \le 125^oC$, $V_{cm} = \pm 10V$	74	100		dB
Unity Gain Bandwidth Product	GBW	$V_{OI} < 90mV$		12		MHz
Output Characteristics						
Output Voltage Swing	V_O	$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm 10V$	±10	±18		mA
Full Power Bandwidth	FPBW	$V_O = \pm 10V$, $FPBW = (SR)\,(2\pi V_p)^{-1}$	50	75		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm 200mV$		30	60	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm 200mV$		25	40	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm 5V$	±4	±7		V/µS
Settling Time	t_S	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm 5V$		1.5		S
Power Supply						
Supply Current	I_S			3.0	4.0	mA
Power Supply Rejection Ratio	PSRR	$-55^oC \le T_A \le 125^oC$, $\Delta V_s = \pm 5V$	74	90		dB

SP-2600/02/05

Wideband, Precision Operational Amplifiers

Absolute Maximum Ratings

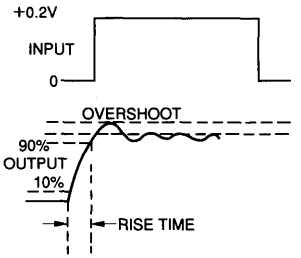
Voltage Between V^+ and V^- Terminals	45.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±12.0V	SP-2605	$0\ ^oC \le T_A \le 75^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current	Full Short Circuit Protection		

Electrical Characteristics: $V^+ = +15V$, $V^- = -15V$, $T_A=25^oC$ unless otherwise specified in "Conditions".

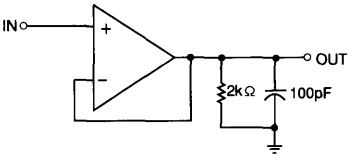
SP-2605

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			3	5	mV
		$0°C \le T_A \le 75°C$			7	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$0°C \le T_A \le 75°C$; average		5		µV/°C
Bias Current	I_B			5	25	nA
		$0°C \le T_A \le 75°C$			40	nA
Offset Current	I_{OS}			5	25	nA
		$0°C \le T_A \le 75°C$			40	nA
Input Impedance	Z_{in}	Guaranteed by Design	40	300		MΩ
Common Mode Range	V_{cm}	$0°C \le T_A \le 75°C$	±11.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm10V$	80K	150K		V/V
		$0°C \le T_A \le 75°C$, $R_L = 2K\Omega$, $V_O = \pm10V$	60K			V/V
Common Mode Rejection Ratio	CMRR	$0°C \le T_A \le 75°C$, $V_{cm} = \pm10V$	74	100		dB
Unity Gain Bandwidth Product	GBW	$V_{Ot} < 90mV$		12		MHz
Output Characteristics						
Output Voltage Swing	V_O	$0°C \le T_A \le 75°C$, $R_L = 2K\Omega$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm10V$	±10	±18		mA
Full Power Bandwidth	FPBW	$V_O = \pm10V$, FPBW= (SR) $(2\pi V_p)^{-1}$	50	75		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm200mV$		30	60	nS
Overshoot	γ	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm200mV$		25	40	%
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm5V$	±4	±7		V/µS
Settling Time	t_S	$R_L = 2K\Omega$, $C_L = 100pF$, $V_O = \pm5V$		1.5		S
Power Supply						
Supply Current	I_S			3.0	4.0	mA
Power Supply Rejection Ratio	PSRR	$0°C \le T_A \le 75°C$, $\Delta V_s = \pm5V$	74	90		dB

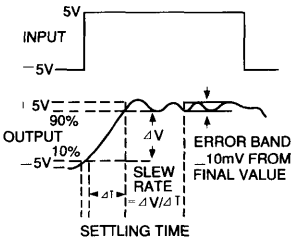
A.C. Performance



Transient Response



A.C. Test Circuit



Slew Rate/Settling Time

Ordering Information

When ordering the SP-2600/02/05, specify the package and screening according to the following :

SP 2 - 2600 - 2

Prefix: SP (SIPEX)

Generic Part #

PACKAGE :

SCREENING

1 - 14 pin ceramic DIP	-2 : -55 °C to 125 °C
2 - Metal Can	-4 : -25 °C to 85 °C
3 - 8 Pin Plastic DIP	-5 : 0 °C to 75 °C
4 - 20 Pin LCC	-6 : 25 °C 100% D.C. Probe (Dice Only)
7 - 8-Pin CERDIP	/883 : -55 °C to 125 °C Full Mil Processing
0 - DICE	

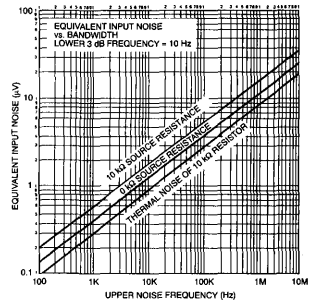
NOTES: 1. Not all package types and screening option combinations are available. Consult local sales office or factory for availability information.

2. Consult factory for special package or screening requirements.

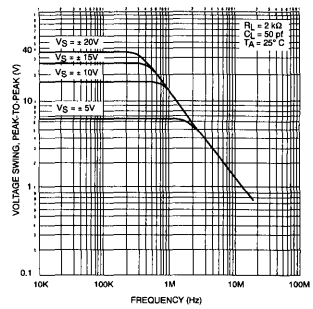
3. Consult factory for 883 revision C compliant data sheet.

4. Consult factory for package mechanical dimensions.

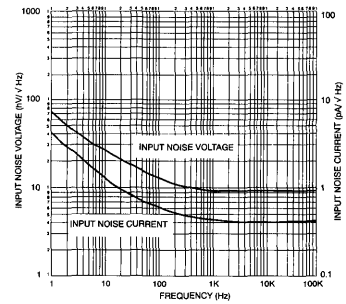
BROADBAND NOISE CHARACTERISTICS



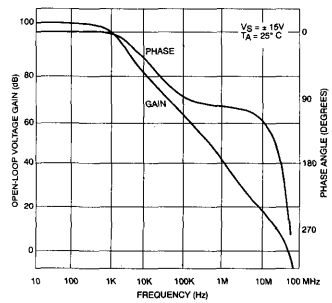
OUTPUT VOLTAGE SWING vs. FREQUENCY



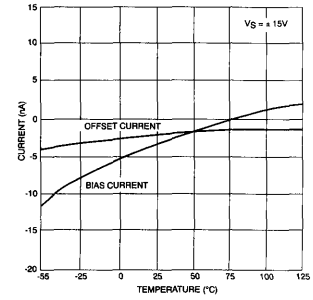
INPUT NOISE DENSITY vs. FREQUENCY



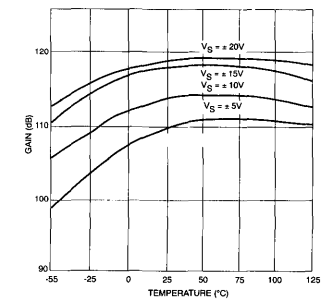
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



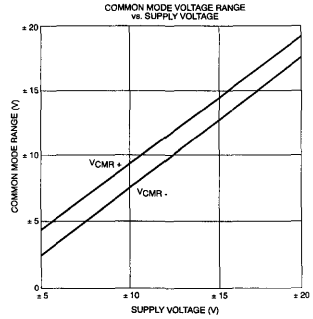
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



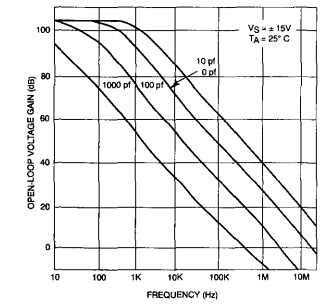
OPEN-LOOP VOLTAGE GAIN vs. TEMPERATURE



COMMON MODE VOLTAGE RANGE
vs. SUPPLY VOLTAGE



OPEN-LOOP FREQUENCY RESPONSE
vs. COMPENSATION CAPACITORS



SP-2620/22/25

Very Wideband, Uncompensated Operational Amplifiers

Features

- 100 MHz Gain Bandwidth Product (A_V = 5)
- 500 MΩ Input Impedance
- 500 μV Input Offset Voltage
- 150K V/V Open Loop Voltage Gain

Applications

- Video Amplifiers
- Pulse Amplifiers
- High Speed Comparators
- Low Distortion Oscillators
- High-Q Active Filters

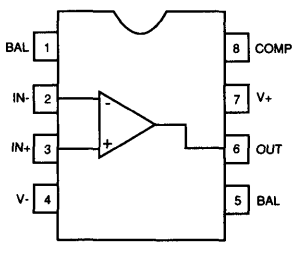
Description

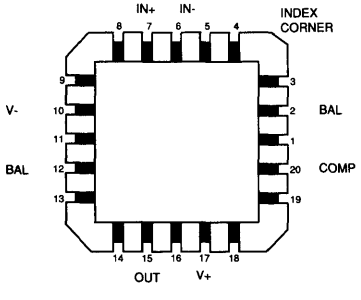
The SP-2620/22/25 are uncompensated, wide bandwidth operational amplifiers. They are stable for gains of five (5) or greater. In addtion to their wide bandwidth, the SP-2620/22/25 offer the advantages of high input impedance, low input bias, input offset currents, low input offset voltage, and short circuit protection. These characteristics combined with the option for complete control of the amplifier's compensation to make it a superior amplifier for high frequency analog signal applications.

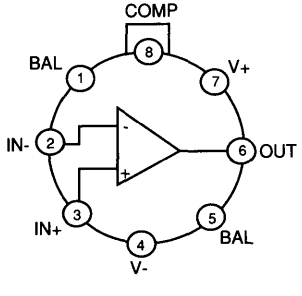
These amplifiers provide the designer with the ability to tailor its transfer characteristics through compensation. Offsets can also be trimmed by connecting a nulling potentiometer between its balance pins, and connecting the wiper to the positive supply, V+. A 100KΩ potentiometer is recommended.

The SP-2620 and the SP-2622 are offered in military (-55°C to 125°C) versions: both are available in metal can, ceramic mini DIP, and LCC packages as well as in die form. The SP-2625 is offered in plastic, ceramic mini DIP, and metal can packages as well as in die form.

Connection Diagrams







SP-2620/22/25

Very Wideband, Uncompensated Operational Amplifiers

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	45.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±12.0V	SP-2620	$-55^oC \le T_A \le 125^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current	Full Short Circuit Protection		

Electrical Characteristics: $V^+ = +15V$, $V^- = -15V$, $T_A=25^oC$ unless otherwise specified in "Conditions".

SP-2620

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			0.5	4	mV
		$-55^oC \le T_A \le 125^oC$			6	mV
Bias Current	I_B			1	15	nA
		$-55^oC \le T_A \le 125^oC$		10	35	nA
Offset Current	I_{OS}			1	15	nA
		$-55^oC \le T_A \le 125^oC$		5	35	nA
Input Impedance	Z_{in}	Guaranteed by Design	65	500		MΩ
Common Mode Range	V_{cm}	$-55^oC \le T_A \le 125^oC$	±11.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm10V$, $C_L = 50pF$	100K	150K		V/V
		$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm10V$	70K			V/V
Common Mode Rejection Ratio	CMRR	$-55^oC \le T_A \le 125^oC$, $V_{cm} = \pm10V$	80	100		dB
Gain Bandwidth Product	GBW	$V_{OI} < 90mV$, $R_L = 2K\Omega$, $C_L = 50pF$, $A_V = 40dB$		100		MHz
Output Characteristics						
Output Voltage Swing	V_O	$-55^oC \le T_A \le 125^oC$, $R_L = 2K\Omega$, $C_L = 50pF$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm10V$	±15	±22		mA
Full Power Bandwidth	FPBW	$V_O = \pm10V$, $FPBW = (SR)(2\pi V_p)^{-1}$, $R_L = 2K\Omega$, $C_L = 50pF$	400	600		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$, $A_V = 40dB$		17	45	nS
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$, $A_V = 40dB$	±25	±35		V/μS
Power Supply						
Supply Current	I_S			3.0	4.0	mA
Power Supply Rejection Ratio	PSRR	$-55^oC \le T_A \le 125^oC$, $\Delta V_s = \pm5V$	80	90		dB

Absolute Maximum Ratings

Voltage Between V^+ and V^- Terminals	45.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±12.0V	SP-2622	$-55^oC \le T_A \le 125^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current	Full Short Circuit Protection		

Electrical Characteristics: $V^+ = +15V$, $V^- = -15V$, $T_A=25^oC$ unless otherwise specified in "Conditions".

SP-2622

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			3	5	mV
		$-55°C \le T_A \le 125°C$			7	mV
Bias Current	I_B			5	25	nA
		$-55°C \le T_A \le 125°C$			60	nA
Offset Current	I_{OS}			5	25	nA
		$-55°C \le T_A \le 125°C$			60	nA
Input Impedance	Z_{in}	Guaranteed by Design	40	300		MΩ
Common Mode Range	V_{cm}	$-55°C \le T_A \le 125°C$	±11.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm10V$, $C_L = 50pF$	80K	150K		V/V
		$-55°C \le T_A \le 125°C$, $R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm10V$	60K			V/V
Common Mode Rejection Ratio	CMRR	$-55°C \le T_A \le 125°C$, $V_{cm} = \pm10V$	74	100		dB
Gain Bandwidth Product	GBW	$V_{OI} < 90mV$, $R_L = 2K\Omega$, $C_L = 50pF$, $A_V = 40dB$		100		MHz
Output Characteristics						
Output Voltage Swing	V_O	$-55°C \le T_A \le 125°C$, $R_L = 2K\Omega$, $C_L = 50pF$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm10V$	±10	±18		mA
Full Power Bandwidth	FPBW	$V_O = \pm10V$, $FPBW = (SR)(2\pi V_p)^{-1}$, $R_L = 2K\Omega$, $C_L = 50pF$	320	600		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm200mV$, $A_V = 40dB$		17	45	nS
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$, $A_V = 40dB$	±20	±35		V/μS
Power Supply						
Supply Current	I_S			3.0	4.0	mA
Power Supply Rejection Ratio	PSRR	$-55°C \le T_A \le 125°C$, $\Delta V_s = \pm5V$	74	90		dB

SP-2620/22/25

Very Wideband, Uncompensated Operational Amplifiers

Absolute Maximum Ratings

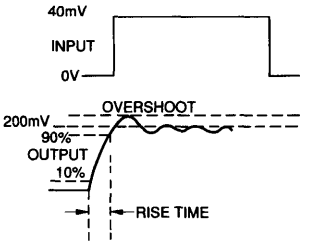
Voltage Between V^+ and V^- Terminals	45.0V	Operating Temperature Range	
Differential Input Voltage, V_d	±12.0V	SP-2625	$0\,^oC \le T_A \le 75^oC$
Internal Power Dissipation , P_d	300mV	Storage Temperature Range	$-65^oC \le T_A \le 150^oC$
Peak Output Current	Full Short Circuit Protection		

Electrical Characteristics: $V^+ = +15V$, $V^- = -15V$, $T_A=25^oC$ unless otherwise specified in "Conditions".

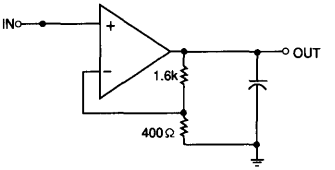
SP-2625

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Characteristics						
Offset Voltage	V_{OS}			3	5	mV
		$0\,^oC \le T_A \le 75^oC$			7	mV
Bias Current	I_B			5	25	nA
		$0\,^oC \le T_A \le 75^oC$			40	nA
Offset Current	I_{OS}			5	25	nA
		$0\,^oC \le T_A \le 75^oC$			40	nA
Input Impedance	Z_{in}	Guaranteed by Design	40	300		MΩ
Common Mode Range	V_{cm}	$0\,^oC \le T_A \le 75^oC$	±11.0			V
Transfer Characteristics						
Large Signal Voltage Gain	Av_{OL}	$R_L = 2K\Omega$, $V_O = \pm10V$, $C_L = 50pF$	80K	150K		V/V
		$0\,^oC \le T_A \le 75^oC$, $R_L = 2K\Omega$, $V_O = \pm10V$, $C_L = 50pF$	70K			V/V
Common Mode Rejection Ratio	CMRR	$0\,^oC \le T_A \le 75^oC$, $V_{cm} = \pm10V$	74	100		dB
Gain Bandwidth Product	GBW	$V_{Ot} < 90mV$, $C_L = 50pF$, $R_L = 2K\Omega$, $A_V = 40dB$		100		MHz
Output Characteristics						
Output Voltage Swing	V_O	$0\,^oC \le T_A \le 75^oC$, $R_L = 2K\Omega$, $C_L = 50pF$	±10.0	±12.0		V
Output Current	I_{OUT}	$V_O = \pm10V$	±10	±18		mA
Full Power Bandwidth	FPBW	$V_O = \pm10V$, $FPBW=(SR)(2\pi V_p)^{-1}$, $C_L=50pF$, $R_L=2K\Omega$	320	600		KHz
Transient Response						
Rise Time	t_R	$R_L = 2K\Omega$, $C_L = 50pF$, $A_V = 5$		17	45	nS
Slew Rate	SR	$R_L = 2K\Omega$, $C_L = 50pF$, $V_O = \pm5V$, $A_V = 5$	±20	±35		V/µS
Power Supply						
Supply Current	I_S			3.0	4.0	mA
Power Supply Rejection Ratio	PSRR	$0\,^oC \le T_A \le 75^oC$, $\Delta V_s = \pm5V$	74	90		dB

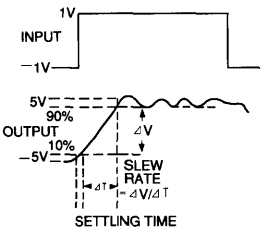
A.C. Performance



Transient Response



A.C. Test Circuit



Slew Rate/Settling Time

Ordering Information

When ordering the SP-2620/22/25, specify the package and screening according to the following :

SP 2 - 2620 - 2

Prefix: SP (SIPEX) — Generic Part # — PACKAGE : — SCREENING

PACKAGE :	SCREENING	
1 - 14 pin ceramic DIP	-2 :	-55 °C to 125 °C
2 - Metal Can	-4 :	-25 °C to 85 °C
3 - 8 Pin Plastic DIP	-5 :	0 °C to 75 °C
4 - 20 Pin LCC	-6 :	25 °C 100% D.C. Probe (Dice Only)
7 - 8-Pin CERDIP		
0 - DICE	/883 :	-55 °C to 125 °C Full Mil Processing

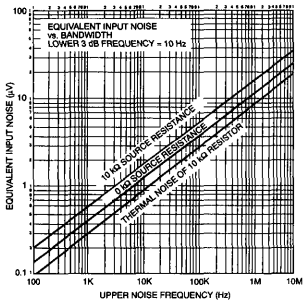
NOTES: 1. Not all package types and screening option combinations are available. Consult local sales office or factory for availability information.

2. Consult factory for special package or screening requirements.

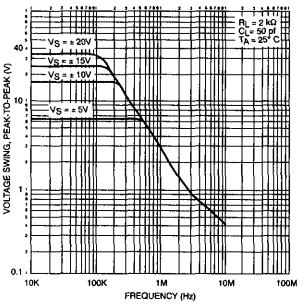
3. Consult factory for 883 revision C compliant data sheet.

4. Consult factory for package mechanical dimensions.

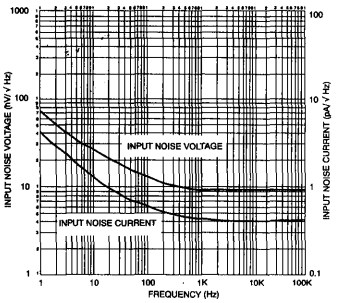
BROADBAND NOISE CHARACTERISTICS



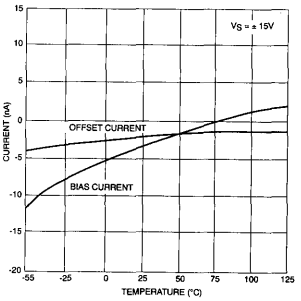
OUTPUT VOLTAGE SWING vs. FREQUENCY



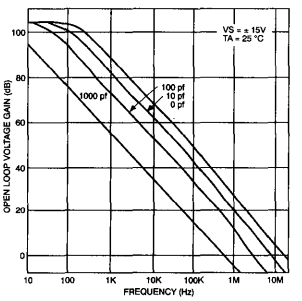
INPUT NOISE DENSITY vs. FREQUENCY



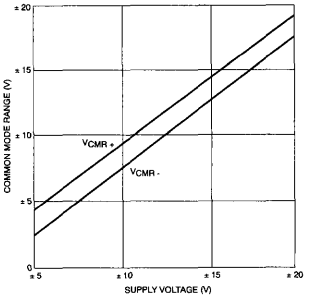
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



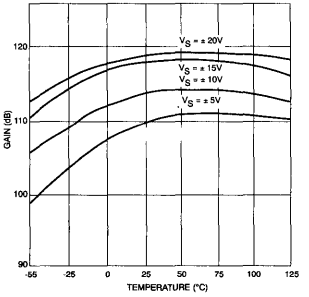
OPEN-LOOP FREQUENCY RESPONSE vs. COMPENSATION CAPACITOR



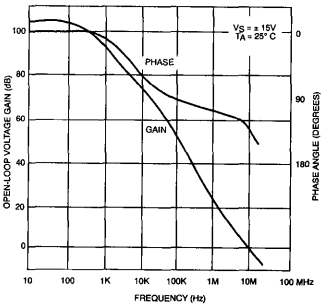
COMMON MODE VOLTAGE RANGE vs. SUPPLY VOLTAGE



OPEN-LOOP VOLTAGE GAIN vs. TEMPERATURE



OPEN-LOOP FREQUENCY AND PHASE RESPONSE



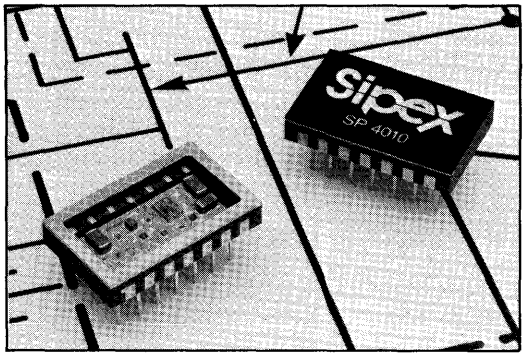
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP4010

WIDE BANDWIDTH, HIGH ACCURACY, HIGH SPEED BUFFER

FEATURES

- Bandwidth: 60 MHz
- High slew rate: 1000V/μsec min
- Low offset and drift: 1mV/10μV/°C
- FET input
- 16-bit linearity @ ± 10VDC; 1kΩ load
- Voltage gain of 1 ±0.002%
- Settling time: 100nsec to 0.005% (5V step)
  200nsec to 0.005% (20V step)

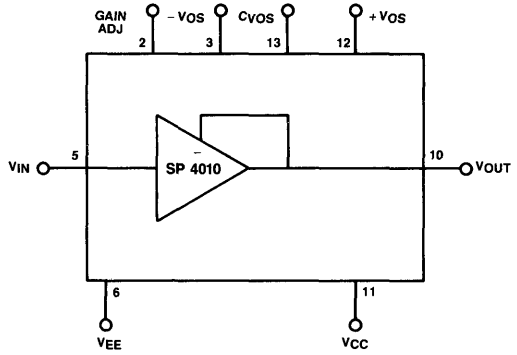


DESCRIPTION

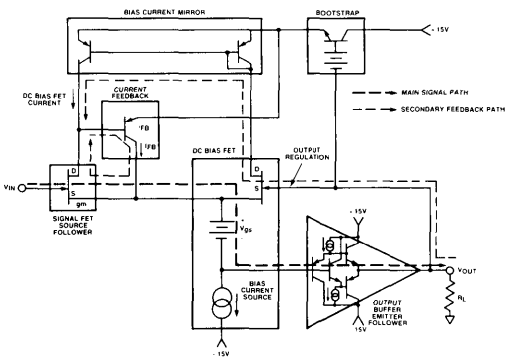
The SP4010 is a high accuracy, high speed, FET input buffer providing up to ±50 mA of continuous current at frequencies from DC to 60 MHz. High linearity, low offset, and excellent stability make it an ideal candidate for a high impedance input buffer for high resolution A/D converters. With a slew rate of 1000V/μsec, good phase linearity and low distortion, the SP4010 is also well suited for a variety of video and high speed data acquisition applications.

The SP4010 is specified for operation from 0°C to +70°C for commercial grade and −55°C to +125°C for military grades.

FUNCTIONAL DIAGRAM



SIMPLIFIED SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

MODEL	SP 4010C	SP 4010B
Supply Voltage	±18V	±18V
Input Voltage	V_{SUPPLY}	V_{SUPPLY}
Power Dissipation	1 Watt	1 Watt
Continuous Output Current	50mA	50mA
Peak Output Current	100mA	100mA
Operating Temperature Range	0°C to +70°C	−55°C to +125°C
Operating Junction Temperature	150°C	150°C
Case to Junction Thermal Resistance	20°C/Watt	20°C/Watt
Storage Temperature	−65°C to +125°C	−65°C to +150°C

DC ELECTRICAL CHARACTERISTICS

(Typical @ +25C, V_{CC} = +15VDC, VEE = −15 VDC unless otherwise specified)

MODEL	SP 4010C	SP 4010B
Input Bias Current[1]	100pA	100pA
Input Impedance	1GΩ	1GΩ
Input Capacitance	5pF	5pF
Output Offset Voltage[2]	±1mV typ. ±2mV max	±1mV typ. ±2mV max
Offset Voltage T_C	±10μV/°C	±10μV/°C typ ±50μV/°C max
Output Impedance	±0.1Ω	±0.1Ω typ. ±0.5Ω max
Output Voltage Swing (1kΩ Load)	V_{CC} −4.5V to V_{EE} +4V	V_{CC} −4.5V to V_{EE} +4V
Output Current	±25mA @ V_{OUT} = ±10V	±25mA@ V_{OUT}= ±10V ±50mA @ V_{OUT} = ±5V
Supply Current (Quiescent)	10mA	10mA typ, 14mA max
Power Consumption (Quiescent)	300mW	300mW
PSRR	0.001%/%	0.001%/%
Gain (1K Load)[2]	1±0.002% typ. ±0.02% max	1±0.002% typ. ±0.02% max
±10V Linearity Error (>1K Load)	±0.0005% typ. ±0.002% max	0.0005% typ. ±0.002% max

AC ELECTRICAL CHARACTERISTICS

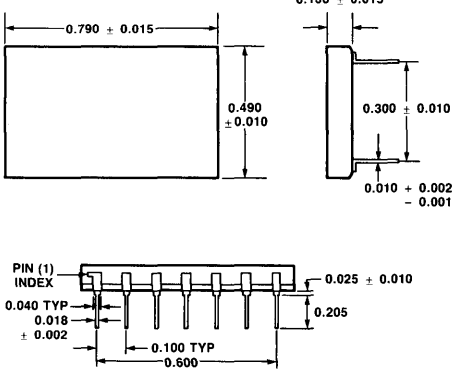
(Typical @ +25 C, V_{CC} = +15VDC, V_{EE} = 15VDC unless otherwise specified)

MODEL	SP 4010C	SP 4010B
Slew Rate	±1000V/μsec	±1000V/μsec min
Bandwidth	60 MHz	60 MHz
Harmonic Distortion Ω @10 kHz ($20V_{p-p}$, 1KΩLoad) @1 MHz ($10V_{p-p}$, 1KΩLoad) @10 MHz ($5V_{p-p}$, 1KΩLoad)	 −100dB typ, −90dB max −80dB −60dB	 −100dB typ, −90dB max −80dB −60dB
Settling Time (to 0.005%, ±20V Step) 1KΩLoad	200nS typ, 300nS max	200nS typ, 300nS max
Settling Time (to 0.005%, ±5V Step) 1KΩ Load	100nS typ, 200nS max	100nS typ, 200nS max
Noise Voltage Density	20nV/Hz	20nV/Hz

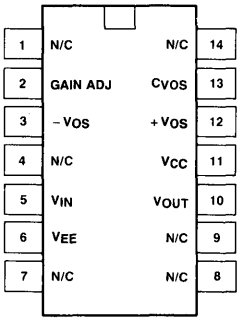
NOTES
1. Independent of input voltage if allowable swing is not exceeded.
2. Adjustable to zero. See gain/offset adjust procedure.

PACKAGE OUTLINE

Dimensions In Inches



PIN ASSIGNMENTS



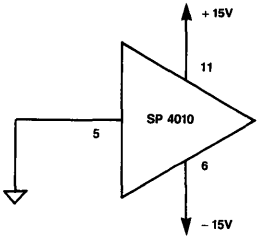
TOP VIEW

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	N/C	14	N/C
2	GAIN ADJ	13	C_{VOS}
3	$-V_{OS}$	12	$+V_{OS}$
4	N/C	11	V_{CC}
5	V_{IN}	10	V_{OUT}
6	V_{EE}	9	N/C
7	N/C	8	N/C

INTERNAL ACTIVE DEVICE	COUNT
Bipolar Transistors	41
JFET	2
DIODES	5

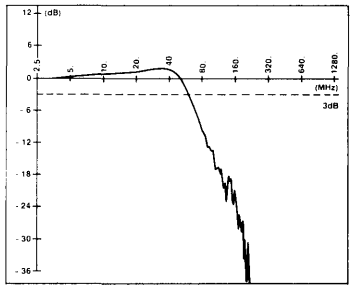
BURN IN SCHEMATIC



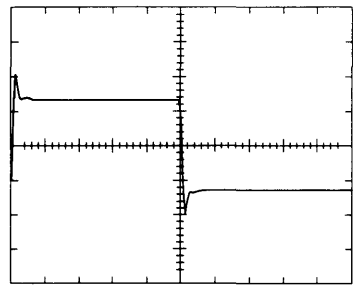
ORDERING INFORMATION

MODEL	TEMP RANGE	SCREENING
SP 4010B	−55°C to +125°C	MIL-STD-883C
SP 4010C	0°C to 70°C	—

TYPICAL PERFORMANCE CHARACTERISTICS

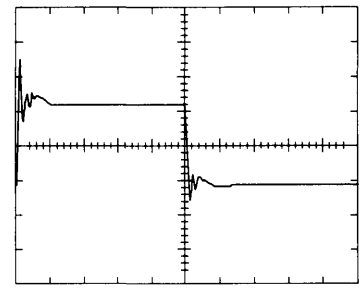


Small Signal Bandwidth



V = 50mV/DIV
H = 100nS/DIV

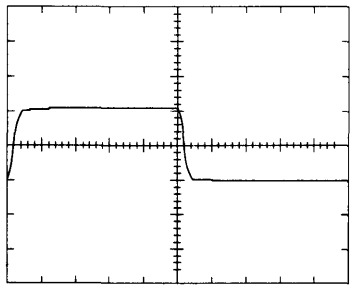
Small Signal Settling Into 100Ω Load



V = 2V/DIV
H = 100nS/DIV

5V Settling Into 1KΩ Load

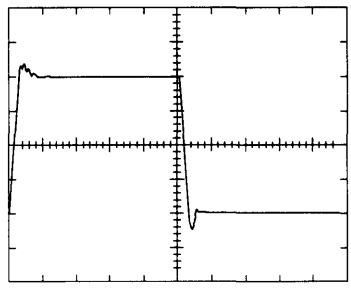
4



V = 5V/DIV
H = 100nS/DIV

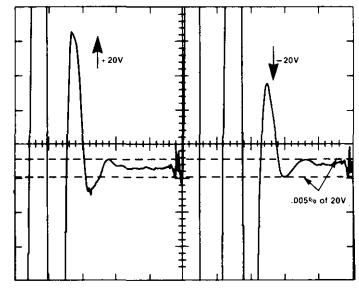
10V Settling Into 1KΩ

The Generator slew rate was purposely limited to 250V/μS to illustrate large signal non-slew settling.



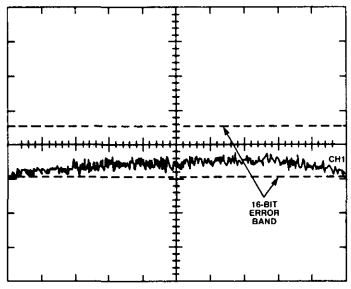
V = 5V/DIV
H = 100nS/DIV

20V Settling Into 1KΩ Load



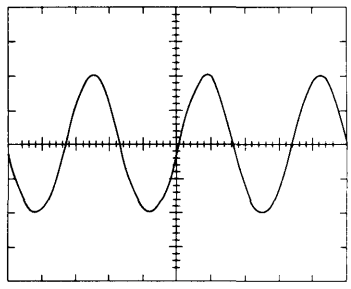
V = 2mV/DIV
H = 100nS/DIV

20V, 0.005% Settling Time Into 1KΩ Load



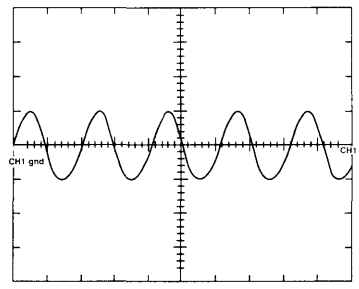
V = 200μV/DIV (V_{out} − V_{in})
H = 2V/DIV (V_{in})

$20V_{p-p}$ Linearity Error With 1KΩ Load



V = 50V/DIV
H = 50nS/DIV

5MHz, 20V Sinewave Into 1KΩ Load



V = 5V/DIV
H = 50nS/DIV

10MHz, 10V Sinewave Into 1KΩ Load

SUPPLY BYPASSING

Power supply bypassing is necessary to prevent oscillation with the SP 4010 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within ¼" to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1μF in parallel; adding a 4.7μF solid tantalum capacitor will help in troublesome instances.

RECOMMENDED LAYOUT PRECAUTIONS

RF/video printed circuit board layout rules should be followed when using the SP 4010 since it will provide power gain to frequencies over 60 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal lid of the device since it is electrically isolated from internal circuitry. Alternatively, the lid should be connected to the output to minimize input capacitance.

The gain adjust pot and the offset adjust pot should be mounted within one inch of the SP 4010. An etch guard ring should be laid around the gain and offset adjust circuitry and tied to the output to prevent dynamic deterioration from stray capacitance. (See Figure 1).

GAIN AND OFFSET ADJUSTMENTS

In most system applications there will be no need to adjust the gain and offset of the SP 4010 separately. The system gain and offset adjustments could be used instead. However, it is not recommended that the gain and offset adjustment pots connected to the SP 4010 be used to compensate system gain and offset errors.

Figure 1 shows the recommended gain and offset adjustment circuit.

IMPORTANT: The lead length on the gain and offset adjustment circuit should be kept short (within one inch) to avoid oscillation or deterioration of dynamic performance.

The DVM must have both inputs floating. A hand held DVM with 100μV or finer resolution may be used for this measurement.

For very critical adjustments a 5 minute warmup is recommended for the SP 4010.

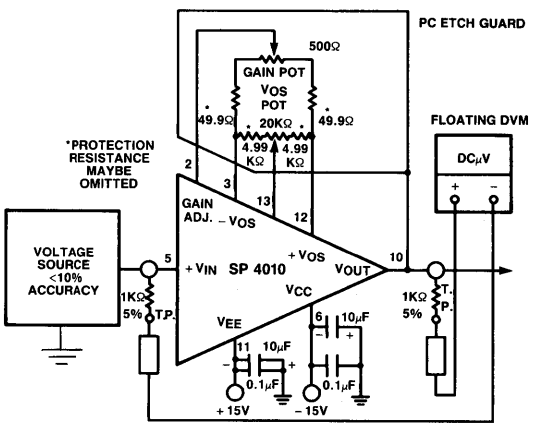


Figure 1. Gain and Offset Adjustment

GAIN ADJUSTMENT

The gain adjustment should be done before the offset adjustment to avoid the effect that the gain pot has on the offset voltage.

The gain adjustment also affects the output resistance of the SP 4010. The output resistance will be closest to zero ohms when the gain is closest to one.

The gain pot is adjusted while plus full scale and minus full scale voltages (as defined by the user's system) are applied to the SP 4010 by an external voltage source or by the previous stage in the system. This applied voltage needs to be only 10% accurate because the floating DVM is measuring gain error directly. The gain error has been compensated when the floating DVM reads the same value for plus full scale and minus full scale input voltages. The input voltage applied to the SP 4010 can be a manually controlled DC voltage or a slow 2 to 10 second period full scale square wave.

OFFSET ADJUSTMENT

After the gain has been adjusted, the remaining error is eliminated by the offset adjustment. The input voltage applied to the SP 4010 should be zero volts. The offset pot is adjusted until the floating DVM reads zero volts.

CAPACITIVE LOADING

Two considerations must be taken into account when driving capacitive loads. These are frequency stability and charge current magnitude.

For some values of load capacitance (>50pf) it may be necessary to isolate the capacitive load with a resistor from 1Ω to 10Ω to reduce ringing or oscillation tendency. The desired step response can be obtained with the right resistor value for each application. (See Figure 2)

The charge current magnitude must be controlled not to exceed the maximum rated output current for the SP 4010. If the maximum output current is exceeded, the output stage will saturate during a transient and will take long to recover.

The charge current into the capacitor is established by

$$I_{C\ load} = C_{load} \times \frac{dv}{dt}$$

The charge current can be limited by controlling the slew rate of the signals driving the SP 4010, by reducing the amount of capacitive loading or by adding resistance in series with the capacitive load.

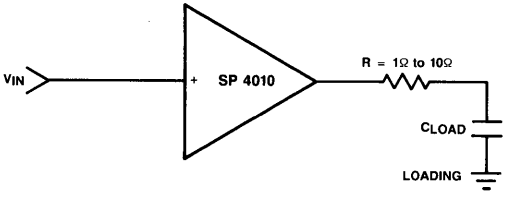


Figure 2. Capacitive Loading

SP 4010 THEORY OF OPERATION

A source follower is a unity gain amplifier that uses field effect transitors in the main signal path. The input is applied at the FET gate, while the output is taken from the FET source. The typical source follower has the advantage of very high input impedance and high speed, but its voltage range, accuracy, linearity and drive capability are poor.

The SP 4010 employs a proprietary architecture that has all the high input impedance and speed of a source follower, as well as the full voltage range, accuracy, linearity and drive capability of a unity gain closed loop op amp.

The SP 4010 is divided into the following circuit blocks: (See simplified schematic on page 1.)

Signal FET Source Follower
Output Buffer Emitter Follower
DC Bias FET and Load Regulation
Bias Current Mirror
Current Feedback Loop (Common Emitter)
Bootstrap

The primary voltage signal path is from the input through the source follower to the emitter follower buffer to the output. The Signal FET Source Follower operates at the channel current set by the Bias FET. The Signal FET source drives the output buffer emitter follower directly through a Vgs shift that cancels its own Vgs.

With matched FET's running at the same ID and Vds, it follows that the offset from gate to gate (or V_{IN} to V_{OUT}) of the FET's is zero.

The Bias Current Mirror and the current feedback common emitter loop adjust the signal FET current until it's matched to the Bias FET current. A residual ID mismatch error remains due to finite gain in the current feedback loop and mirror gain error.

The signal FET is lightly loaded at its source by the finite impedance of the bias current source, output buffer and boot-strapped bias FET current. The current feedback loop is responsible for linearization of the signal FET source voltage under these load currents. The output impedance of the signal FET source is divided by the current gain of the loop.

The DC Bias FET provides not only DC Bias, but also load regulation for the output buffer emitter follower. Any offsets presented by the output buffer simply appear as a minor shift in the Vgs which is common to both FET's and does not affect V_{OUT} vs. V_{IN}.

Any signal dependent variation in the output buffer emitter follower offset as caused by a load resistor or its inherent linearity error, gets transformed into a current by the gm of the Bias FET. This signal flows as a current through the mirror and the current loop forces an equal change in the signal FET current that transforms into an equal and opposite Vgs change with the matched gm of the signal FET.

It is important to note here that the load regulation signal flows through the Bias FET and Mirror once into the current loop without recirculation through the Bias FET.

V_{OUT}/V_{IN} variations on the output buffer emitter follower simply cause a small variation in the operating point of the FET's that is rejected by the CMRR of the FET's.

DC CHARACTERIZATION METHOD

The DC characterization of offset voltage, gain error, linearity, output resistance and output swing under load is done with the test system shown in Figure 3. This test approach was chosen because of it's immunity from source or DVM induced errors.
The SP 4010 unity gain buffer is a 4 terminal device where signal is concerned. There are two power pins, an input pin and an output pin. A signal voltage may be applied with respect to ground or with respect to the supplies which are firmly defined with respect to ground. So, except for a signal inversion, it is the same to drive the input with respect to the supplies as it is to drive both supplies with respect to the input.

The latter was chosen and the input of the SP 4010 was grounded so that the supplies may be driven by the DC source DAC 08. This scheme allows direct measurement of all errors with the HP 3456A DVM, using its more sensitive scales without the resolution and accuracy sacrifice presented by the ±20V range. The accuracy of the signal source is also very non-critical. The DAC 08 is more than adequate to measure 18-bit linearity on the SP 4010 because the DAC 08 output does not appear in the error signal.

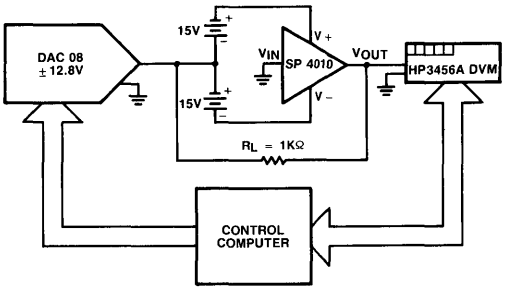


Figure 3. DC Test System

One last point that should be addressed is the distinction between Power Supply rejection ratio and the measurements carried out by this system. Note that while the two 15V "Battery" supplies are being moved with respect to the input pin, each supply is a constant well regulated and bypassed 15V. A power supply rejection ratio test is done by changing the magnitude of the supply voltage individually or by the same amount.

AC CHARACTERIZATION METHOD
STEP RESPONSE

The AC characterization of step response settling time uses the same measurement philosophy as the DC characterization method. The test system is reconfigured by computer control into the test setup shown in Figure 4.

The DAC 08 now controls the amplitude of the square wave that the HI 201HS switches generate. Careful layout and bypassing of all supplies are essential to generate a square wave free of ringing. Any slow droop or amplitude inaccuracy in the square wave is effectively rejected by this measurement method.

The settling error is directly amplified by clamping amplifier and measured on the oscilloscope. As before, there is no need to cancel out the input square wave. The TEKTRONIX 2430 oscilloscope provides hard copy thru a HP 2225A Printer (see Page 3).

FREQUENCY RESPONSE

The frequency response characterization was done with the test system outlined in Figure 5. This test method yields good consistent accurate results with commonly available lab equipment. A small signal (250mV) square wave is fed to the device under test to produce a step response at the output. This square wave must be free of ringing and must have a rise time (= 2nS) that is faster than that of the device under test.

One transition (positive or negative) is captured at the output of the SP 4010, by the TEK 2430 digital storage oscilloscope. The step response is differentiated in the HP 9826 Computer to produce the impulse response. A Fast Fourier Transform is performed on the impulse response to obtain the frequency response. The magnitude of the frequency response is displayed on the CRT and hard copy may be obtained on the printer or plotter. See Page 3 for a copy of the printout.

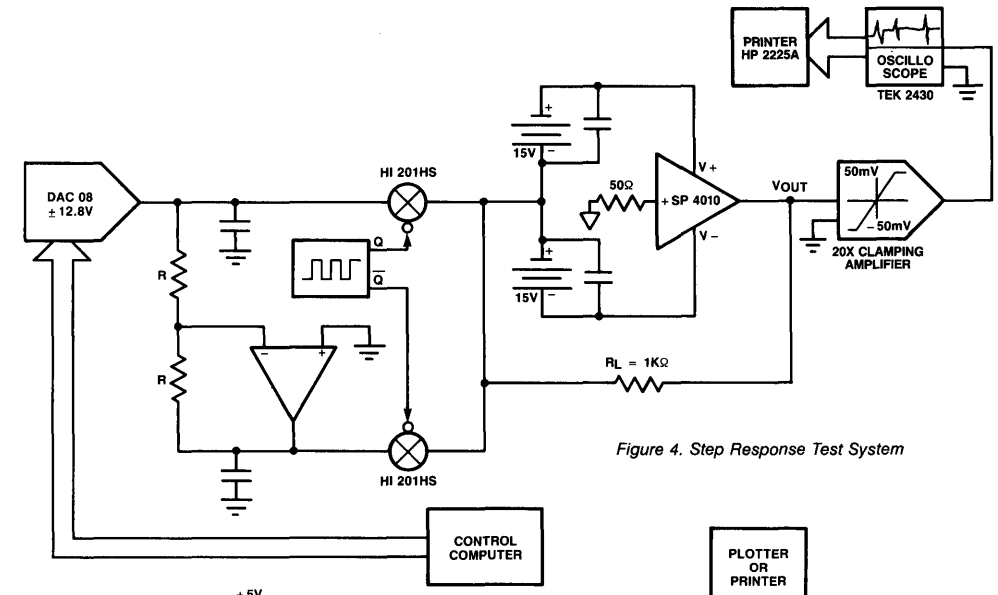


Figure 4. Step Response Test System

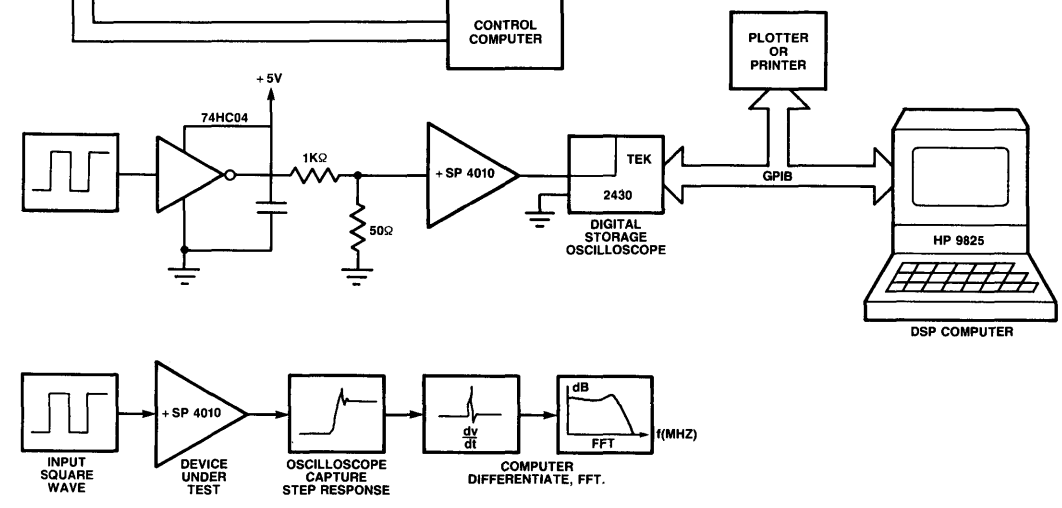
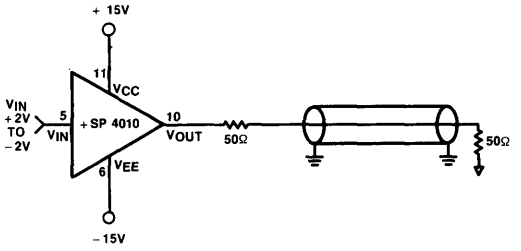
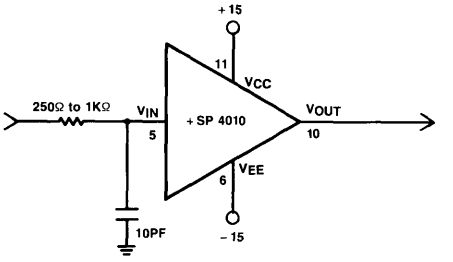


Figure 5. Frequency Response Test System

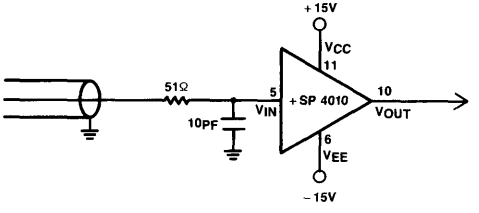
APPLICATION CIRCUITS



PRECISION CABLE DRIVER

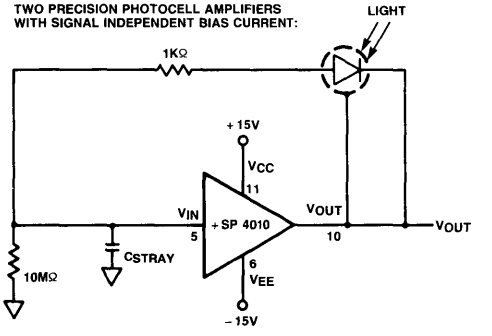


OPTIMIZE FOR LARGE SIGNAL SETTLING



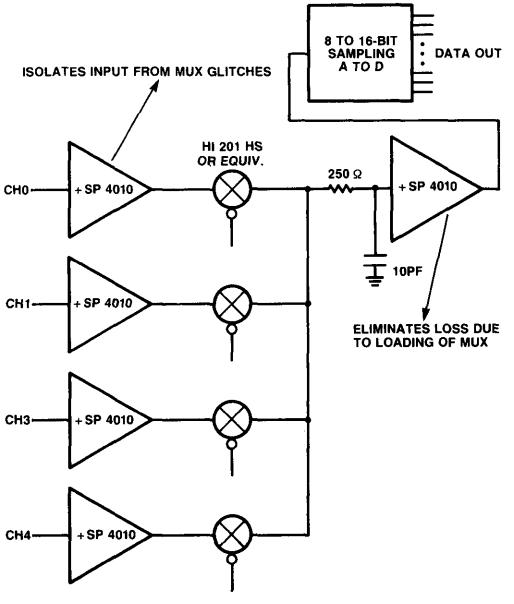
UNTERMINATED CABLE BUFFER

TWO PRECISION PHOTOCELL AMPLIFIERS WITH SIGNAL INDEPENDENT BIAS CURRENT:

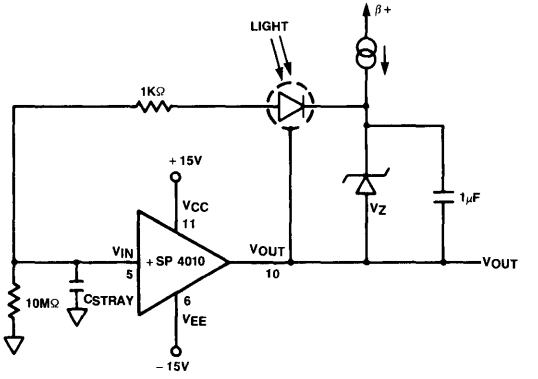


FAST 10MΩ TRANS RESISTANCE AMPLIFIER FOR PHOTO DIODE DETECTOR

$$BW = \frac{1}{2\pi \times 10M\Omega \times C_{STRAY}}$$



VERY HIGH SPEED BUFFERED DAS FOR MAGNETIC RESONANCE IMAGING ON CAT SCANNER APPLICATIONS

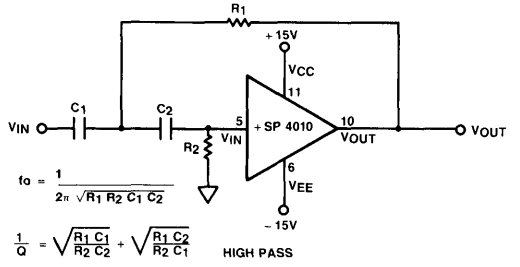


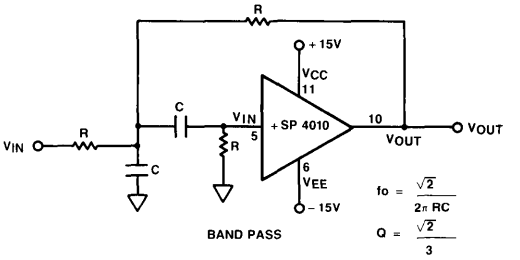
FAST 10MΩTRANS RESISTANCE AMPLIFIER FOR REVERSE BIASED PHOTO DIODE DETECTOR

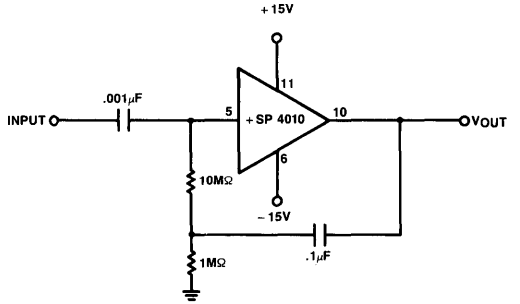
$$BW = \frac{1}{2\pi \times 10M\Omega \times C_{STRAY}}$$

APPLICATION CIRCUITS

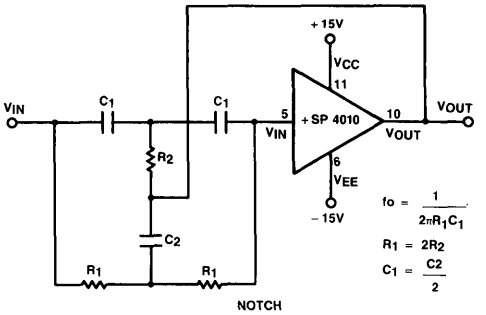
Low Distortion Active Filters

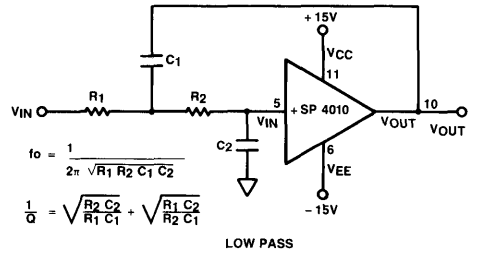


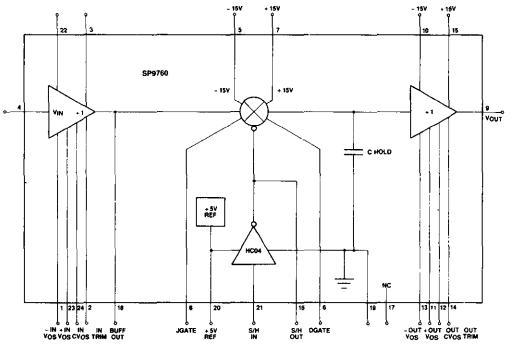




NOTE: REFER TO "RECOMMENDED LAYOUT PRECAUTIONS" FOR ALL APPLICATIONS CIRCUITS







PRECISION HIGH SPEED SAMPLE AND HOLD SP9760

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP5190/SP5195

WIDEBAND, FAST SETTLING OPERATIONAL AMPLIFIERS

FEATURES

- Fast Settling Time 70 ns
- Very High Slew Rate 200 V/µs
- Wide Gain-Bandwidth 150 MHz
- Power Bandwidth 6.5 MHz
- Low Offset Voltage 3 mV
- Input Voltage Noise 6 nV/√Hz
- Monolithic Bipolar Construction

PRELIMINARY SPECIFICATION

APPLICATIONS

- Fast, Precise D/A Converters
- High Speed Sample-Hold Circuits
- Pulse and Video Amplifiers
- Wideband Amplifiers
- Replace Costly Hybrids

DESCRIPTION

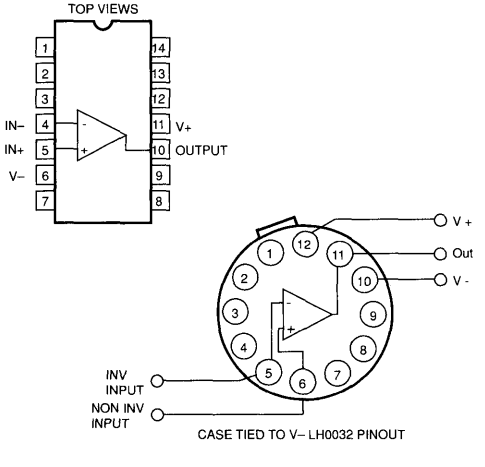
SP5190/SP5195 are monolithic operational amplifiers featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with dielectric isolation, these devices are capable of delivering an unparalleled 200V/µs slew rate with a settling time of 70 ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains ≥5 without the need for external compensation. Other outstanding SP5190/95 features are 150 MHz gain-bandwidth-product and 6.5 MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 3 mV offset voltage and 6.0 nV input voltage noise (at 1 kHz).

With 200 V/µs slew rate and 70 ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. 150 MHz gain-bandwidth-product, 6.5 MHz power bandwidth, and 6 mV offset voltage make SP5190/5195 ideally suited for a variety of pulse and wideband video amplifier applications.

The SP5190/5195 are available in metal can (TO-5), 20 pin LCC, and 14 pin ceramic packages.

At temperatures above +75°C, a heat sink is required for SP5190. (See note 2). SP5190 is specified over the -55°C to +125°C range while SP5195 is specified from 0°C to +75°C.

CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS[1]

Voltage between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current ..... 50 mA (Peak)
Internal Power Dissipation[2] ..... 870 mW (Cerdip); 1W (TO-8) Free Air

Operating Temperature Range:
(SP5190) ..... $-55°C \le T_A \le +125°C$
(SP5195) ..... $0°C \le T_A \le +75°C$
Maximum Storage Temperature Range .... $-65°C \le T_A < +150°C$

ELECTRICAL CHARACTERISTICS

$V_{SUPPLY} = \pm 15$ Volts, $R_L = 200$ ohms, unless otherwise specified.

			SP5190 -55°C to +125°C			SP5195 0°C to +75°C			
PARAMETERS	**CONDITIONS**	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT CHARACTERISTICS									
Offset Voltage		25°C		3.0	5.0		3.0	6	mV
		Full			10.0			10.0	mV
Average Offset Voltage Drift		Full		20			20		µV/°C
Bias Current		25°C		5	15		5	15	µA
		Full			20			20	µA
Offset Current		25°C		1	4		1	4	µA
		Full			6			6	µA
Input Resistance		25°C		10			10		Kohms
Input Capacitance		25°C		1.0			1.0		pF
Common Mode Range		Full	±5			±5			V
Input Noise Voltage (f = 1 kHz, $R_g = 0\Omega$)		25°C		6			6		nV/√Hz
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain	$R_L = 200\Omega$, $C_L<10$ pF, $V_O = \pm 5V$	25°C	15K	30K		10K	30K		V/V
		Full	5K			5K			V/V
Common Mode Rejection Ratio	$V_{CM} = \pm 5V$	Full	74			74			dB
Gain Bandwidth Product	$V_O = 90$ mV, $A_V = 10$	25°C		150			150		MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	$R_L = 200\Omega$, $C_L<10$ pF, $V_O = \pm 5V$	Full	±5	±8		±5	±8		V
Output Current	$R_L = 200\Omega$, $C_L<10$ pF, $V_O = \pm 5V$	25°C	25	30		25	30		mA
Output Resistance		25°C		30			30		Ohms
Full Power Bandwidth Full power bandwidth guaranteed based on slew rate measurement using FPBW= Slew Rate/2π Vpeak.	$R_L = 200\Omega$, $C_L<10$ pF, $V_O = \pm 5V$	25°C	5	6.5		5	6.5		MHz

ELECTRICAL CHARACTERISTICS (cont'd)

V_{SUPPLY} = ±15 Volts, R_L = 200 ohms, unless otherwise specified.

			SP5190 -55°C to +125°C			SP5195 0°C to +75°C			
PARAMETERS	**CONDITIONS**	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
TRANSIENT RESPONSE	Refer to Test Ckts Section of data sheet								
Rise Time		25°C		13	18		13	18	nS
Overshoot		25°C		8			8		%
Slew Rate		25°C	160	200		160	200		V/µs
Settling Time:									
5V Step to 0.1%		25°C		70			70		nS
5V Step to 0.01%		25°C		100			100		nS
2.5V Step to 0.1%		25°C		50			50		nS
2.5V Step to 0.01%		25°C		80			80		nS
POWER REQUIREMENTS									
Supply Current		Full		19	28		19	28	mA
Power Supply Rejection Ratio[3]		Full	70	90		70	90		dB

4

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7 mV/°C for operation at ambient temperatures above +75°C. Heat sinking required at temperatures above +75°C. T_{JA} = 115°C/W; T_{JC} = 35°C/W. Thermalloy model 6007 heat sink recommended.
3. V_{SUPPLY} = ±5 Vdc to ±15 Vdc.

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Wide Bandwidth Fast Settling Time Operation Amplifier

FEATURES

- Ultrastable Unity Gain Bandwidth (100MHz)
- 20nS Settling Time to 0.1%
- Superior DC Performance
- Offset Voltage ±0.3mV
- Bias Current 2µA
- ±16mA Supply Currents

APPLICATIONS

- Driving Flash Converters
- High-Speed DAC's
- Radar, IF Processors
- Photodiode Preamps
- ATE/Pulse Generators
- Imaging/Display Drivers

DESCRIPTION

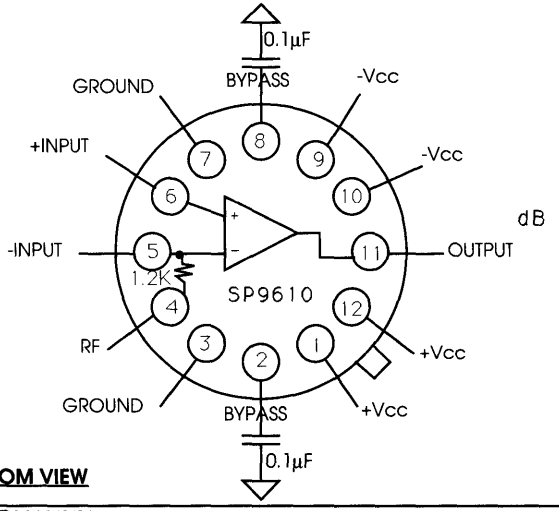
The SP9610 is a fast-settling, wide-bandwidth DC-coupled transimpedance operational amplifier which combines superior DC specifications and exceptional dynamic performance. This combination provides remarkable versatility for high-speed designers.

Thin-film technology and innovative design techniques help assure stable operation over the complete operating temperature range. Input offset voltage temperature drift is typically 5µV/°C; input bias current drift is typically 70nA/°C.

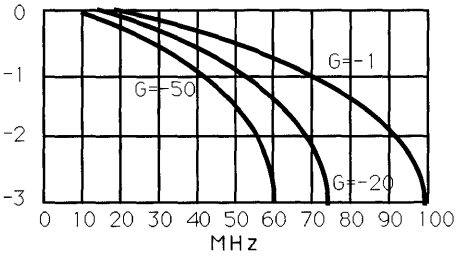
A unique internal architecture keeps the SP9610 inherently stable over its complete gain range and assures wide bandwidth at various gain settings. With G= -1, 3dB bandwidth is 100MHz; with G= -20, 3dB bandwidth is an incredible 75MHz. Slew rate, rise time, fall time, and settling time are also independent of gain.

The design of the SP9610 makes it easy to apply. The unit is internally compensated and needs no external components. An internal 1.2k feedback resistor is available to the user by connecting Pin 4 to output Pin 11. Pins 2 and 8 are bypass pins and should be connected to ground through 0.1µF ceramic capacitors; effective decoupling of the power supplies is also important for proper operation.

Three temperature ranges are available. The SP9610C is guaranteed over a case temperature of 0°C to +70°C; the SP9610T is for a range of -55°C to +125°C, and the SP9610T/B is MIL-STD-883C screened over a temperature range of -55°C to +125°C.



BOTTOM VIEW



SP9610 INVERTING GAIN

SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS ($\pm V = \pm 15$; $A_V = -10$; $R_{IN} = 1200\Omega$, $R_F = 1.2K\Omega$, no R_{LOAD})

PARAMETER (CONDITIONS)	SP9610 TYPICAL @ +25°C	SP9610C MIN/MAX @ 0°C	SP9610C MIN/MAX @ +25°C	SP9610C MIN/MAX @ +70°C	SP9610T,T/B MIN/MAX @ -55°C	SP9610T,T/B MIN/MAX @ +25°C	SP9610T,T/B MIN/MAX @ +125°C	UNITS
Offset Voltage	±0.3		±1.0			±1.0		mV
Offset Voltage T_C	±5							uV/°C
Input Bias Current								
Inverting	±5		±15			±15		uA
Non-Inverting	±15		±50			±50		uA
Input Bias Current T_C								
Inverting	±70							nA/°C
Non-Inverting	±30							nA/°C
Inverting Impedance	20							Ω
Non-Inverting								
Impedance	200k							Ω
Capacitance	4							pF
Common-Mode Input	±5		±5			±5		V
Internal Feedback Resistor (R_F)	1200		1190/1210			1190/1210		Ω
R_F Temperature Coefficient								
Common-Mode Rejection Ratio (CMRR)	>50		≥35			≥35		dB
CMRR (R_F-1500Ω;R_{IN}=150Ω;ΔV_S=5V)	>60							dB
Common-Mode Sensitivity (CMS)								
Referred to Input (ΔV_S=5V)								
-CMS	3		8			8		uA/V
+CMS	3		8			8		uA/V
$CMS_{VOLTAGE}$	62		≥50			≥50		dB
Output Impedance (DC to 100kHz)	0.05							Ω
Output voltage swing (R_{LOAD}=200Ω)	±10		≥±9			≥±9		V
Output Current (continuous)	±50		≥±50			≥±50		mA
Open Loop Transimpedance Gain(200Ω)	4.8		3.0			3.0		MΩ
Supply Current	16		20			20		mA
Power Consumption	480		600			600		mW
Power Supply Rejection Ratio (PSRR)	>50		≥35			≥35		dB
PSRR(R_F=1500Ω;R_{IN}=150Ω;ΔV_S=10V)	>60							dB
Power Supply Sensitivity (PSS)								
Referred to Input (ΔV_S=10V)								
$PSS_{VOLTAGE}$	68		50			50		dB
-PSS	3		8			8		uA/V
+PSS	3		8			8		uA/V

AC ELECTRICAL CHARACTERISTICS ($\pm V = 15V$; $A_V = -10$; R_{IN}=120Ω, R_F=1.2KΩ, R_{LOAD}=200Ω)

PARAMETER(CONDITIONS)	SP9610 TYPICAL @+25°C	SP9610C MIN/MAX @ -25°C	SP9610C MIN/MAX @ +25°C	SP9610C MIN/MAX @ +85°C	SP9610T,T/B MIN/MAX @ -55°C	SP9610T,T/B MIN/MAX @ +25°C	SP9610T,T/B MIN/MAX @ +125°C	UNITS
Bandwidth (-3dB V_{OUT}=100mV p-p)G=-10	>100							MHz
Amplitude of Peaking								
DC to 60MHz	0							dB
>60MHz	0							dB
Phase Nonlinearity (DC to 45MHz)	1							°
Rise (Fall) Time (V_{OUT}=±2.5V Step)	<5							ns
Slew Rate (V_{OUT}=10V Step)	≥3							V/ns
Settling Time to 0.1% (G=-10;5V output step)	20							ns
Settling Time to 0.02% (G=-10;5V output)	30							ns
Overshoot Amplitude (V_{OUT}=5V Output)	<1							%
Propagation Delay	4.8							ns
Total Harmonic Distortion (Freq=20MHz								
Output Voltage=2V p-p)	55							dB
Input Noise (R_{LOAD}=100Ω)								
Voltage (5MHz to 150MHz)	0.7							nV/√HZ
Current (5MHz to 150MHz)	23							pA/√HS

Sipex Corporation

APPLYING THE SP9610 OP AMP

In applying the SP9610 op amp, there are certain precautions which must be observed to protect the unit from damage.:

1. Shorting either power supply input pin (Pin 10 or 12) to the output (Pin 11) will destroy the device.
2. Shorting the output (Pin 11) to ground will destroy the device; no internal protection is provided.

The noninverting input of the SP9610 Operational Amplifier is a high impedance. This requires that it be driven from a low-impedance source, or connected to ground. Driving this input from a high impedance detracts from the wide bandwidth performance; connecting it to ground avoids the possibility of closed-loop ac peaking.

Because the internal biasing network of the SP9610 is connected to the +V and -V supply pins, it is important that these pins have adequate decoupling. Nominal supply voltages for the SP9610 are ±15V, but this can be reduced to a lower limit of ±12V without serious degradation of high-speed performance. When ± 12V supplies are used, output voltage swings from the amplifier must be reduced to 7 volts.

Bypass Pins 2 and 8 should be decoupled to ground through 0.1µF capacitors to maintain stability on the bias network.

Feedback resistor R_F is internal to the SP9610 and has been precisely adjusted to allow the widest possible range of operating conditions. While it is possible to use an external feedback resistor for the device, the user is urged to avoid the temptation to "tune" performance with this technique because it will inevitably detract from ac performace.

A massive low-impedance ground plane is essential for optimum performance from the SP9610 because it provides a moderate level of shielding and helps reduce the effects of distributed capacitance.

But the benefits of a large ground plane can be diminished if components are grounded at multiple points on the ground plane. Single-point grounding is *always* preferred for high-speed circuits to avoid the possibility of voltage differentials which might result from multiple grounds.

The best high-frequency performance is obtained from the SP9610 when total output capacitance is minimized. Realistically, this is not always possible; but performance can be improved with a 5-30Ω resistor in series with the output as shown in Figure 1.

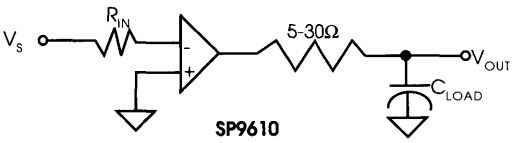


Figure 1.

Isolation provided by the series resistor makes it possible for the SP9610 to drive loads well outside its design limits, but at some loss of speed. Isolating the capacitance load from the output of the amplifier is particularly useful when driving flash A/D converters.

The power supplies for the SP9610 must be decoupled effectively to obtain maximum performance from the device. Recommended choices are a 0.1µF ceramic capacitor and a 10µF tantalum capacitor in parallel on each supply. These connections show up in Figures 2 and 3 which illustrate the connections for inverting and noninverting operations, respectively. Decoupling components should always be connected as closely as possible to the amplifier's voltage supply pins.

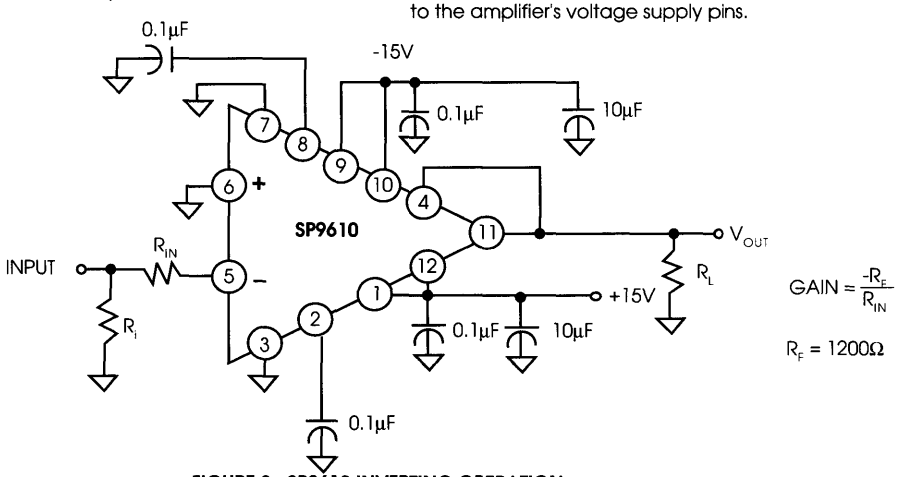


FIGURE 2. SP9610 INVERTING OPERATION

If the expected output voltage swings are small, it is possible to operate the output stages from ±5V supplies; this will reduce power dissipation and junction temperatures on the output transistors. For this, the ±5V and ±15V supplies must be decoupled seperately.

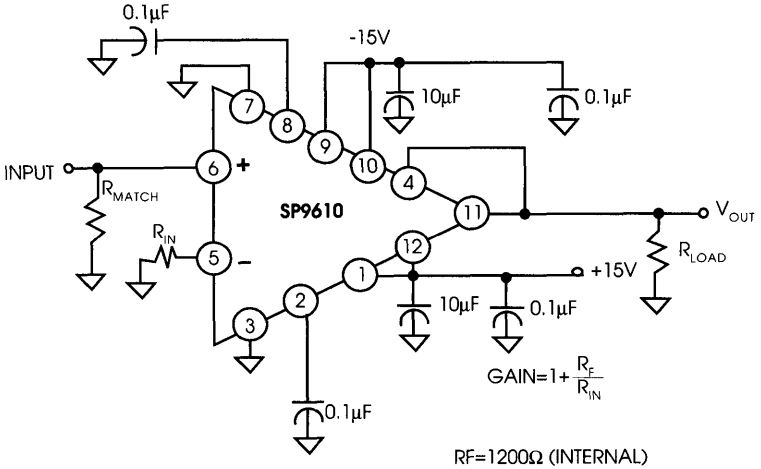


FIGURE 3. SP9610 NONINVERTING OPERATION

As shown in Figures 2 and 3, bypass pins 2 and 8 should be decoupled individually with a 0.1µF capacitor in series to ground. Without this decoupling, power supply and common-mode rejection ratios (PSRR and CMRR) may be degraded. In some applications, the lack of this decoupling may show up as very high-frequency "ringing" on the output. R_{MATCH} in Figures 2 and 3 is used to match the output impedance of the driving source.

SP9610 POWER DISSIPATION

Quiescent power supply currents for the SP9610 are ±16mA. Supply currents this low allow the unit to be operated over a wide temperature range without damage. For high-temperature operation and long-term stability, however, the user is urged to use a heat sink. Two acceptable models for TO-8 packages are the Thermalloy 2240 and the IERC Up-TO8-48CB.

VOLTAGE REFERENCES

MODEL	OUTPUT VOLTAGE RANGE	OUTPUT VOLTAGE TEMPCO	TEMPERATURE RANGE	PACKAGE	PAGE
HS2700	+10V, -10V	±3 to ±10 ppm/°C	-25°C to +85°C -55°C to +125°C	14-Pin SD	165

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

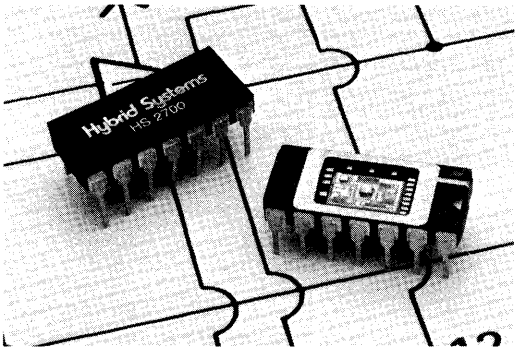
HS2700 SERIES

PRECISION +10V, −10V, ±10V REFERENCES

FEATURES

- High accuracy: 10.000 volts, ±2.5mV
- Low temperature coefficient: 3 ppm/°C
- 14-pin ceramic side brazed package
- Performance guaranteed −55°C to +125°C
- AD2700 Series pin out compatibility

MODEL	OUTPUT
HS2700	+10.000V
HS2701	−10.000V
HS2702	±10.000V



5

DESCRIPTION

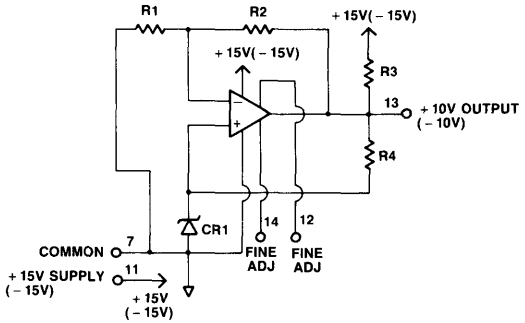
The HS2700 Series offers a complete line of precision +10V, −10V, and ±10V references. All models can be processed to MIL-STD-883C or commercial/industrial standards. The HS2700 Series combines precision laser trimmed nichrome resistors with premimum grade gain and reference components for ultra-stable overall performance. Versions with tempcos as low as ±3 ppm/°C are available.

The HS2700 is a +10 volt reference with 10mA output drive capability making it suitable for use with high accuracy bipolar D/A converters or as a general positive system reference.

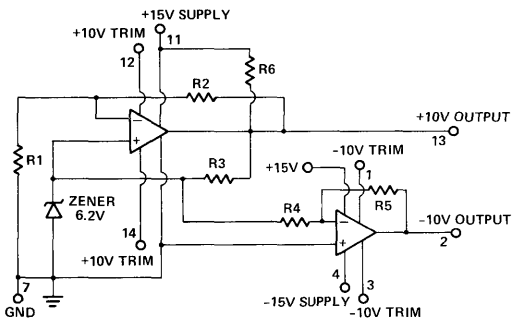
The HS2701 is a negative 10 volt reference designed to interface with CMOS D/A and A/D converters. For systems requiring a dual tracking reference, the HS2702 offers both positive and negative precision 10 volt outputs in a single package. Both are often used with the HS5210 Series 12-Bit A/D converters which require −10V external references for high accuracy over a wide temperature range.

Commercial "J" and "L" grades offer −25°C to +85°C operation while "S" and "U" grades operate from −55°C to +125°C. Screening to MIL-STD-883C is available.

FUNCTIONAL DIAGRAMS



HS2700 (2701)



HS2702

SPECIFICATIONS

(Maximum or minimum @E_{IN} ±15V @ +25°C, R_L = 2kΩ unless otherwise noted.)

MODEL	HS 2700JD	HS 2700LD	HS 2700SD	HS 2700UD
ABSOLUTE MAX RATINGS				
Input Voltage (for applicable supply)	±20V	*	*	*
Power Dissipation @ +25°C				
HS 2700, 01	300mW	*	*	*
HS 2702	450mW	*	*	*
Operating Temperature Range	−25°C to +85°C	*	−55°C to +125°C	***
Storage Temperature Range	−65°C to +150°C	*	*	*
Lead Temperature (soldering, 10s)	+300°C	*	*	*
Short Circuit Protection (to GND)	Continuous	*	*	*
OUTPUT VOLTAGE ERROR @ +25°C				
HS 2700 (10.000V)	±0.005V	±0.0025V	*	**
HS 2701 (−10.000V)	±0.005V	±0.0025V	*	**
HS 2702 (±10.000V)	±0.005V	±0.0025V	*	**
OUTPUT CURRENT[1]				
@ +25°C	±10mA	*	*	*
(V_{IN} = ±13 to ±18V) over op. temp. range	±5mA	+5mA, −2mA	**	**
OUTPUT VOLTAGE ERROR (T_{min} to T_{max})[2]				
HS 2700, 01	10ppm/°C ±11.0mV	3ppm/°C ±4.3mV	** ±8mV	** ±5.5mV
HS 2702	10ppm/°C ±11.0mV	5ppm/°C ±5.5mV	** ±10.0mV	3ppm/°C ±5.5mV
LINE REGULATION				
V_{IN} = ±13.5 to ±16.5V	300μV/V	*	*	*
LOAD REGULATION				
0 to +10mA				
HS 2700	50μV/mA	*	*	*
HS 2701	200μV/mA	*	*	*
HS 2702	50μV/mA	*	*	*
OUTPUT RESISTANCE	0.05Ω	*	*	*
INPUT VOLTAGE, OPERATING	±13V to ±18V	*	*	*
QUIESCENT CURRENT				
HS 2700, 01	±14mA	*	*	*
HS 2702	+17mA, −4mA	*	*	*
NOISE				
(0.1 to 10Hz)	50μV p-p typ	*	*	*
OFFSET ADJUST RANGE				
(See Diagrams)	±20mV min	*	*	*
OFFSET ADJUST TEMP DRIFT EFFECT	±4μV/°C per mV of Adjust typ	*	*	*
PACKAGE	14-Pin Ceramic DIP			

NOTES:

*Same as "JD" grade performance. **Same as "LD" grade performance. ***Same as "SD" grade performance.

1. Specified with resistive load to common.

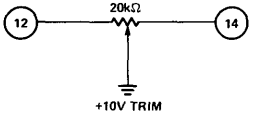
2. Output voltage error as a function of temperature is determined using the box method. Each unit is tested at T_{min}, T_{max} and +25°C. At each temperature V_{OUT} must fall within the rectangular area bounded by the minimum and maximum temperature and whose maximum V_{OUT} is equal to V_{OUT} nominal plus or minus the maximum +25°C error plus the maximum drift error from +25°C. The box limits are noted below the drift values used to calculate the box.

Specifications subject to change without notice.

APPLICATIONS INFORMATION

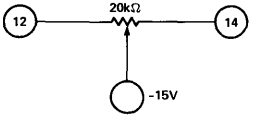
OPTIONAL ADJUSTMENTS

HS 2700



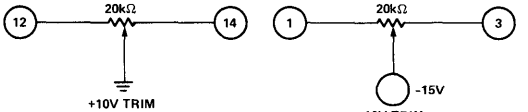
Trim range is 15mV (min)

HS 2701



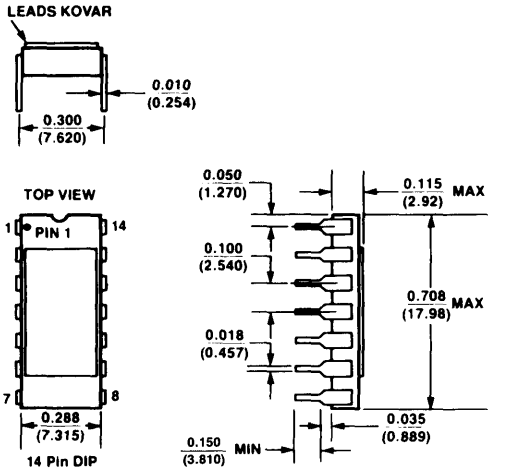
Trim range is 15mV (min)

HS 2702



1. Trim range is 20mV (min.)
2. Trim +10V output first.
3. Trim -10V output last.

PACKAGE DIMENSIONS

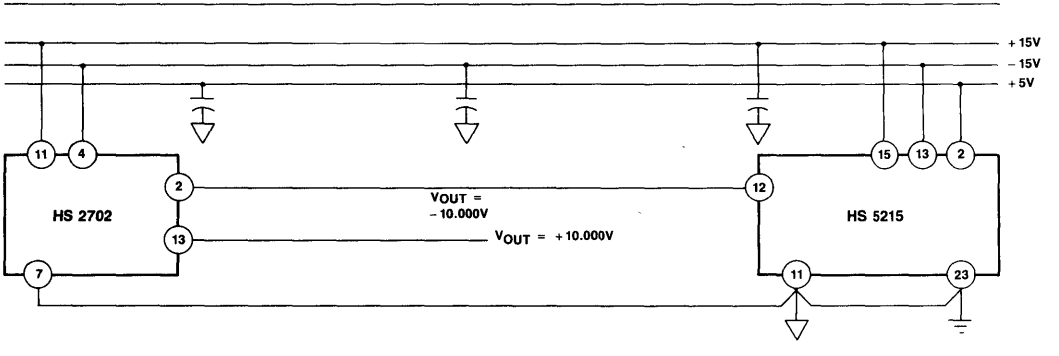


PIN OUT, HS 2702

1	-10V fine adj.
2	-10V OUT
3	-10V fine adj.
4	-15V
5	N/C
6	N/C
7	GND
8	N/C
9	N/C
10	T.P.
11	+15V
12	+10V fine adj.
13	+10V OUT
14	+10V fine adj.

PIN OUT, HS 2700, 2701

1	N/C
2	N/C
3	N/C
4	N/C
5	N/C
6	N/C
7	GND
8	N/C
9	N/C
10	N/C
11	+15V or (-15V)
12	V_{out} fine adj.
13	V_{out}
14	V_{out} fine adj.



Using HS 2702 Reference with the Fast, High Accuracy HS 5215 — 12-Bit ADC

ORDERING INFORMATION

MODEL	OUTPUT VOLTAGE ERROR	STABILITY	OPERATING TEMPERATURE RANGE	SCREENING
HS 2700JD	±0.005V	10 ppm/°C	−25°C to +85°C	—
HS 2700LD	±0.0025V	3 ppm/°C	−25°C to +85°C	—
HS 2700SD/883	±0.005V	3 ppm/°C	−55°C to +125°C	MIL-STD-883C
HS 2700UD/883	±0.0025V	3 ppm/°C	−55°C to +125°C	MIL-STD-883C
HS 2701JD	±0.005V	10 ppm/°C	−25°C to +85°C	—
HS 2701LD	±0.0025V	3 ppm/°C	−25°C to +85°C	—
HS 2701SD/883	±0.005V	3 ppm/°C	−55°C to +125°C	MIL-STD-883C
HS 2701UD/883	±0.0025V	3 ppm/°C	−55°C to +125°C	MIL-STD-883C
HS 2702JD	±0.005V	10 ppm/°C	−25°C to +85°C	—
HS 2702LD	±0.0025V	5 ppm/°C	−25°C to +85°C	—
HS 2702SD/883	±0.005V	5 ppm/°C	−55°C to +125°C	MIL-STD-883C
HS 2700UD/883	±0.0025V	3 ppm/°C	−55°C to +125°C	MIL-STD-883C

SAMPLE/HOLD AMPLIFIERS

SAMPLE/HOLD AMPLIFIERS

MODEL	ACCURATE TO	ACQUISITION (TIME) (μsec)	APERTURE UNCERTAINTY (nsec)	DROOP RATE (μV/msec)	POWER CONSUMPTION (mW)	PACKAGE	PAGE
HS9704/05 (QUAD S/H)	12 bits	4	5	20	750	24-Pin DD	177
HS346	12 bits	2	6	500	795	14-Pin SD	171
SP5330	12 bits	0.5	0.1	10	555	14-Pin SD	173
HS9720	12 bits	0.2	0.05	500	730	24-Pin DD	187
SP9730	12 bits	0.1	0.05	5	1000	24-Pin DD	193
HS9716	16 bits	10	0.7	10	300	14-Pin DD	181
SP9760	16 bits	0.3				24-Pin DD	197

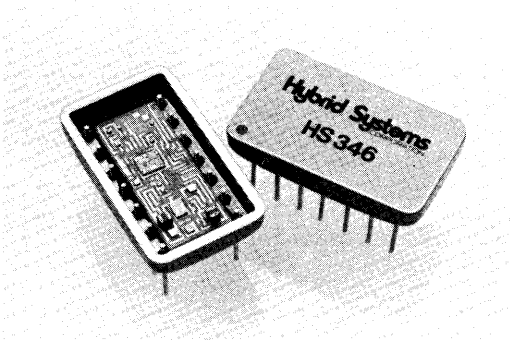
Shaded area indicates new product since publication of 1988 Catalog

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS 346
High Speed Sample/Hold

FEATURES

- **Acquisition Time, 2.0 μs**
- **Linearity 0.01%**
- **Low Droop 0.5 mV/ms**
- **Internal Hold Capacitor**
- **−55°C to +125°C Operation**
- **Small Size, 14 pin DIP**



DESCRIPTION

The HS 346 is a high speed, high accuracy sample/hold amplifier in a 14 pin DIP. It is pretrimmed to a max of 0.02% gain error with a low sample to hold offset of less than 4mV. The HS 346 is specially built for military applications in the −55°C to +125°C temperature range and features precision laser trimmed thin film resistors, carefully selected active chips and is processed to the requirements of MIL-STD-883 Rev. C, Level B (HS 346B). HS 346 is a superior replacement of the MN346. Product highlights include:

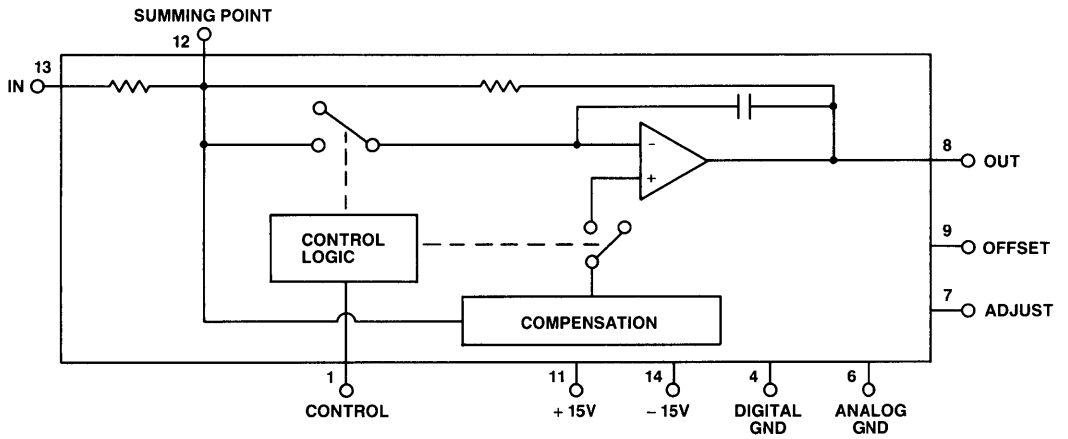
LOW GAIN ERROR — the gain of the HS 346 is laser-trimmed to an accuracy of ±0.02% max at room temperature. It will stay within ±0.05% max over the full −55°C to +125°C temperature range.

FAST SIGNAL ACQUISITION — a small internal holding capacitor is combined with a high slew rate output amplifier for a fast signal acquisition time of 2 μs max.

HIGH-REL PROCESSING — HS 346 is specified for the full −55°C to +125°C temperature range and is processed according to the requirements of MIL-STD-883 Rev. C, Level B.

6

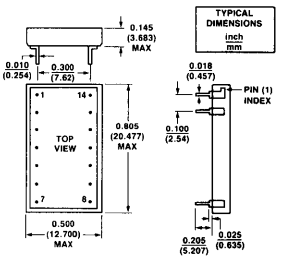
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C, rated supply unless otherwise noted)

MODEL	HS 346
SAMPLE/HOLD CHARACTERISTICS	
Acquisition Time	
to 0.01%, 10V step	1.0μs (typ), 2.0μs (max)
to 0.01%, 20V step	1.6μs (typ), 2.5μs (max)
Aperture Delay	60ns (max)
Aperture Uncertainty	6ns
Settling Time ($10V_{pp}$, Sample Mode)	2.0μs (max)
Droop Rate[1]	
@ +25°C	0.5mV/ms (max)
@ +125°C[2]	200mV/ms (typ), 700mV/ms (max)
Sample to Hold Offset	2mV (typ), 4mV (max)
@ −55°C to +125°C[2]	10mV (typ), 20mV (max)
Feedthrough (Hold Mode)	
@ 1 kHz	0.02% (max)
TRANSFER CHARACTERISTICS	
Gain	−1.00
Gain Accuracy	
@ −55°C to +125°C[2]	±0.05% (max)
Full Power Bandwidth	1.4 MHz
Output Slew Rate	50 V/μs
ANALOG INPUT CHARACTERISTICS	
Voltage Range	±10V
Absolute Max Input Voltage	±V supply
Offset Voltage[3]	±3mV (max)
−55°C to +125°C[2]	±6mV (typ), ±20mV (max)
DIGITAL INPUT CHARACTERISTICS	
Input Voltage	
Hold Mode	<+0.8 Volt
Sample Mode[4]	>+2.0 Volt
Input Current "0"	50μA (max)
Input Current "1"	1.0μA (max)
POWER REQUIREMENTS	
Supply Voltage[5]	±15V, ±3%
Supply Currents $+V_S$	28mA
Supply Currents $-V_S$	−25mA
PSRR (both supplies)	0.001%/V
Consumption	795mW (max)
TEMPERATURE RANGE	
Operating	
HS 346C	0°C to +70°C
HS 346B	−55°C to +125°C
Storage	−65°C to +150°C
MECHANICAL	
Case Style	14 pin DIP



Pin 1 is marked by a dot on the top of the package.

PIN	FUNCTION
1	DIGITAL INPUT
2	N/C
3	N/C
4	DIGITAL GND
5	N/C
6	ANALOG GND
7	OFFSET ADJUST
8	ANALOG OUTPUT
9	OFFSET ADJUST
10	N/C
11	+15V
12	SUMMING POINT
13	ANALOG INPUT
14	−15V

NOTES:
1. The output droop in hold mode doubles every 10°C temperature rise.
2. For HS 346B version only.
3. Can be adjusted to zero.
4. Maximum digital input voltage is 5.5 Volt.
5. Maximum output swing is 4 Volts less than the supply voltage.

APPLICATION NOTES

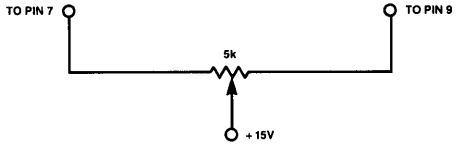
POWER SUPPLY BYPASS

For optimum performance, the +15V and −15V supplies should be bypassed to ground with a 0.01μF ceramic capacitor as close to the pins as possible.

GROUNDING

Analog ground and digital ground are not connected internally. They must be tied together as close to the package as possible.

OFFSET ADJUST

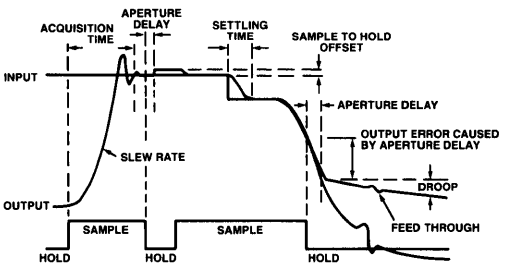


Connect the input (pin 13) to ground and adjust the output to read zero volt, while HS 346 is in sample mode (pin 1 at +5V).

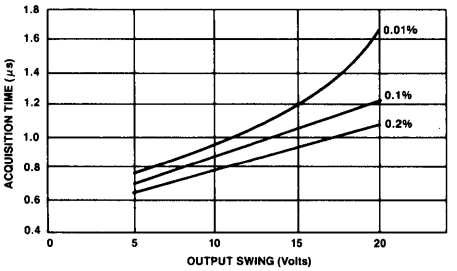
GAIN ERROR/SAMPLE TO HOLD OFFSET ERROR

These errors are intrinsic with the HS 346 and cannot be adjusted directly at the unit. However, since the HS 346 is most likely used in front of an ADC, the system's gain error and sample to hold error can be adjusted using the trim circuitry of the ADC.

TIMING DIAGRAM (not to scale)



HS 346 ACQUISITION TIME vs OUTPUT SWING



ORDERING INFORMATION

MODEL	DESCRIPTION
HS 346C	High Speed S/H, Commercial
HS 346B	High Speed S/H, MIL-STD-883 Rev. C, Level B

Specifications subject to change without notice.

SP5330

VERY HIGH SPEED PRECISION MONOLITHIC SAMPLE AND HOLD AMPLIFIERS

FEATURES

- Very Fast Acquisition — 350 ns (0.1%), 500 ns (0.01%)
- Low Droop Rate — 0.01 μV/μs
- Very Low Offset — 0.2 mV
- Power Bandwidth — 90 V/μs
- Wide Supply Range — ±11V to ±18V
- Internal Hold Capacitor
- Fully Differential Input
- TTL/CMOS Compatible

PRELIMINARY SPECIFICATION

APPLICATIONS

- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto-Zero Circuits
- Peak Detectors

DESCRIPTION

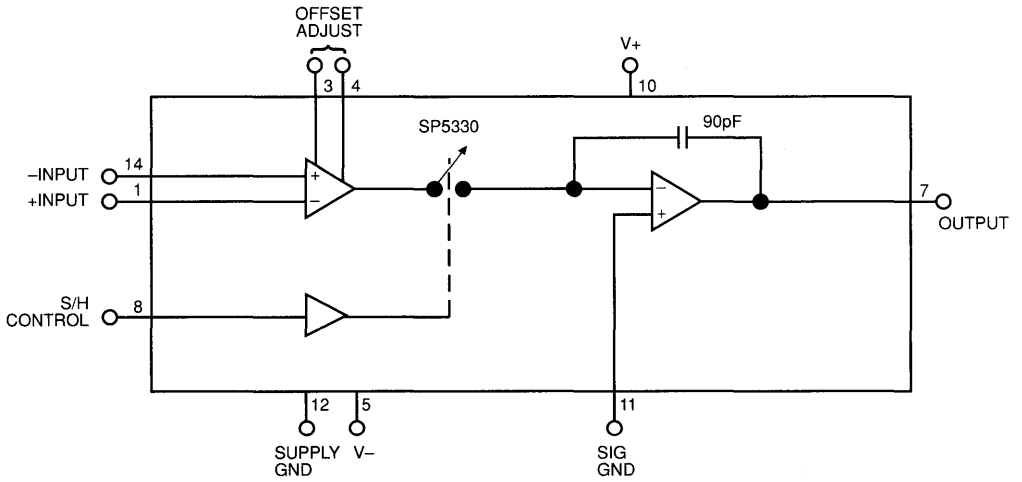
The SP5330 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes Sipex isolation process to achieve a 500 ns acquisition time to 12-bit accuracy and a droop rate of 0.01 μV/μs. The circuit consists of an input transconductance amplifier capable of producing large amounts of changing current, a low leakage analog switch, and an integrating output stage which includes a 90 pF hold capacitor.

The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of V_{in}.

The SP5330 will operate at reduced supply voltages (to ±11V) with a reduced signal range. This monolithic device is available in a ceramic 14-pin DIP. The MIL-STD-883 data sheet for this device is available on request.

6

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

Voltage between V+ and PWR/SIG GND 20V
Voltage between V- and PWR/SIG GND ..... -20V
Voltage between PWR GND and SIG GND ..... ±2.0V
Differential Input Voltage ..... ±24V
Voltage between S/H Control and PWR/SIG GND .....8V, -6V
Output Current, continuous[2] ..... ±17 mA
Total Power Dissipation 1.33W
Derate 13.3 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise specified) V_{SUPPLY} = ±15V ±3%; Digital Input (Pin 8): V_{IL} = +0.8V (sample): V_{IH} = +2.0V (hold); SIG GND = PWR GND.

			SP5330 -2, -4			SP5330 -5			
PARAMETERS	**CONDITIONS**	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT CHARACTERISTICS									
Input Voltage Range		Full	±10			±10			V
Input Resistance		25°C	5	15		5	15		MΩ
Derived from computer simulation only; not tested.									
Input Capacitance		25°C		3			3		pF
Offset Voltage		25°C		0.2			0.2		mV
		Full			2.0			1.5	mV
Offset Voltage T.C.		Full		1	10		1	10	µV/°C
Bias Current		25°C		±20			±20		nA
		Full			±500			±300	nA
Offset Current		25°C		20			20		nA
		Full			500			300	nA
Common Mode Range		Full	±10			±10			V
CMMR	V_{CM} = ±10 Vdc	Full	86	188		86	100		dB
TRANSFER CHARACTERISTICS									
Gain, DC		Full	$2X10^6$	$2X10^7$		$2X10^6$	$2X10^7$		V/V
Gain Bandwidth Product	V_O = 200 mV_{p-p}; R_L = 2K: C_L = 50 pF	25°C		4.5			4.5		MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing		Full	±10			±10			V
Output Current		Full	±10			±10			mA
Full Power Bandwidth		25°C		1.6			1.6		MHz
Full power bandwidth guaranteed based on slew rate measurement using FPBW= Slew Rate/2π Vpeak.									
Output Resistance									
(Hold Mode)		25°C		0.2			0.2		Ω
(Sample Mode)		25°C		10^{-5}	0.001		10^{-5}	0.001	Ω
Total Output Noise, DC to 4.0 MHz									
Sample		25°C		230			230		µV RMS
Hold		25°C		190			190		µV RMS
TRANSIENT RESPONSE									
Rise Time	V_O = 200 mV_{p-p}; R_L = 2K: C_L = 50 pF	25°C		70			70		nS
Overshoot	V_O = 200 mV_{p-p}; R_L = 2K: C_L = 50 pF	25°C		10			10		%
Slew Rate	V_O = 20V Step; R_L = 2K: C_L = 50 pF	25°C		90			90		V/µs

ELECTRICAL CHARACTERISTICS (cont'd)

Test conditions (unless otherwise specified) V_{SUPPLY} = ±15V ±3%; Digital Input (Pin 8): V_{IL} = +0.8V (sample): V_{IH} = +2.0V (hold); SIG GND = PWR GND.

			SP5330 -2, -4			SP5330 -5			
PARAMETERS	**CONDITIONS**	**TEMP**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT CHARACTERISTICS									
Input Voltage (High), V_{IH}		Full	2.0			2.0			V
Input Voltage (Low), V_{IL}		Full			0.8			0.8	V
Input Current (V_{IL} = 0V)		Full		10	40		10	40	µA
Input Current (V_{IH} = +5V)		Full		10	40		10	40	µA
SAMPLE/HOLD CHARACTERISTICS									
Acquisition Time:									
(0.1%)		25°C		350			350		nS
		Full			500			500	nS
(0.01%)		25°C		500			500		nS
		Full			900			900	nS
Aperture Time		25°C		20			20		nS
Derived from computer simulation only; not tested.									
Effective Aperture Delay Time (See Glossary)		25°C	-50	-25	0	-50	-25	0	nS
Aperture Uncertainty		25°C		0.1			0.1		nS
Droop Rate[3]		25°C		0.01			0.01		µV/µs
		Full			100			10	µV/µs
Hold Step Error	V_{IN} = 0V; V_{IH} = +3.5V; t_r = 20 ns (V_{IL} to V_{IH})	25°C		0.5			0.5		mV
Hold Mode Settling Time (0.01%)		25°C		100	200		100	200	ns
Hold Mode Feedthrough $20V_{p-p}$, 100 kHz		Full		-88			-88		dB
POWER REQUIREMENTS									
Positive Supply Current		Full		18	22		18	24	mA
Negative Supply Current		Full		19	23		19	23	mA
Power Supply Rejection V+, V-[4]		Full	86	100		86	100		dB

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below ±17 mA.
3. This parameter is measured at ambient temperature extremes in a high speed test environment. Consequently, steady state heating effects from internal power dissipation are not included.
4. Based on a three volt delta in each supply, i.e. 15V = ±1.5 Vdc.

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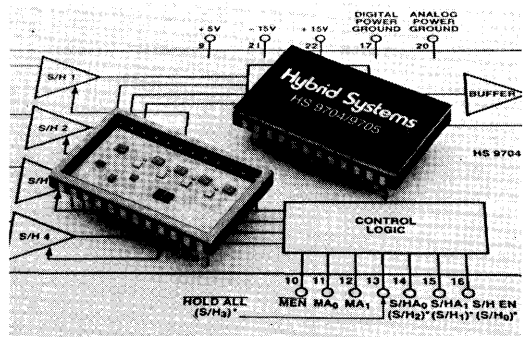
12-BIT ACCURATE QUAD SAMPLE/HOLD FOR SIMULTANEOUS/SEQUENTIAL SAMPLING

FEATURES

- Simultaneous sampling
- Sequential sampling
- Four complete 12-bit S/Hs with MUX, internal capacitors, control logic and buffered output in single 24-pin DIP
- Internally trimmed offsets and S/H step
- Control logic allows independent handling of MUX and S/Hs



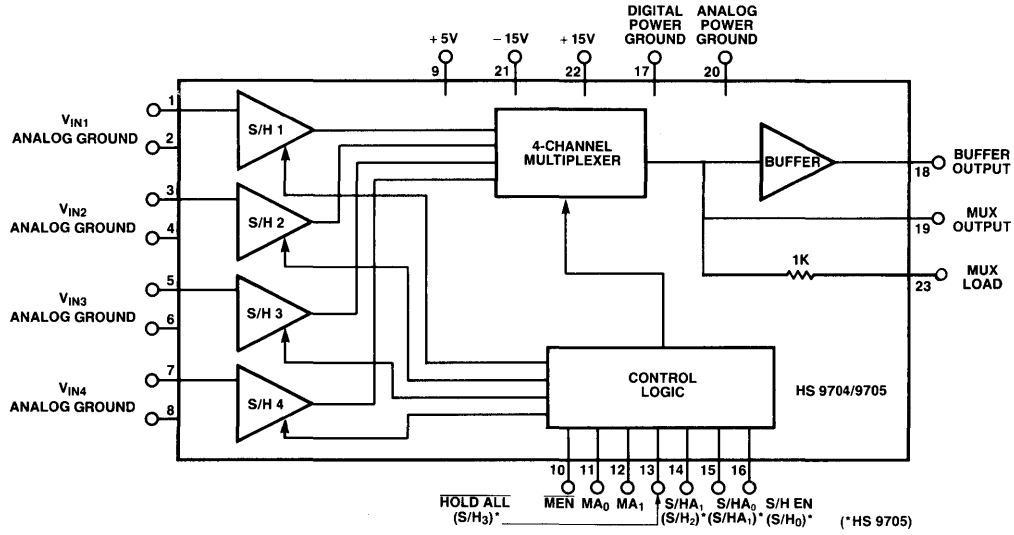
DESCRIPTION

The HS9704/9705 consists of four complete 12-bit sample and holds with internal hold capacitors, MUX, control logic and a buffered output in a single 24-pin DIP. The HS9704 control logic allows simultaneous holding of all four S/Hs or holding of one at a time. The HS9705 allows the flexibility to hold any combination of S/Hs at any time. Simultaneous sampling allows the user to take a snapshot of up to four input signals, freezing their values in a 5 nanosecond aperture uncertainty across all channels. An analog ground pin is available at each sample and hold input to make it convenient for shielding the analog input signals. The HS9704/9705 is particularly suited for use with the HS574 A/D, the HSADC85 and the HS5200 series.

The HS9704/9705 is packaged in a 24-pin DIP and is specified for operation from 0°C to +70°C for commercial grades and from −55°C to +125°C for military grades. Full screening to MIL-STD-883 Rev. C, Levels B or S, is available.

6

FUNCTIONAL DIAGRAM



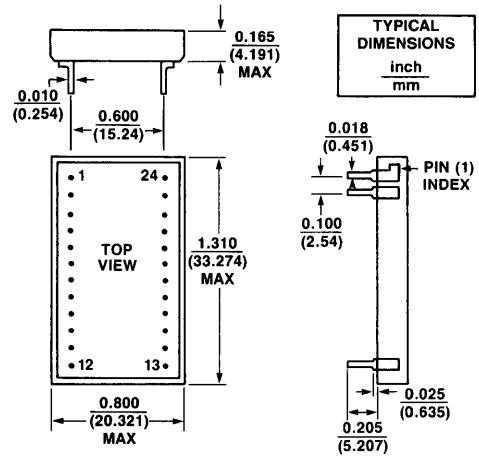
SPECIFICATIONS

(Typical @ +25°C and nominal supply voltages, unless otherwise noted)

MODEL	HS 9704/HS 9705
DYNAMIC CHARACTERISTICS	
Acquisition Time to 0.01%, 20V step	4 μ sec typ, 7 μ sec (max)
Aperture Delay	200 nsec
Aperture Delay Variation between Channels	5 nsec
Aperture Uncertainty	200 psec
Settling Time (Hold Mode, to 0.01%)	800 nsec
Output Settling* (10V step, to 0.01%)	1 μsec typ, 3 μsec max
Droop Rate	
@ +25°C	35 V/msec
@ +125°C	2 mV/msec
Sample to Hold Offset (Pedestal)	±1 mV typ, ±2.5 mV max
Feedthrough (Hold Mode)	
@ 1 kHz	−80 dB
Power Supply Rejection Ratio	60 dB (+15V), 80 dB (−15V)
Crosstalk (Channel to Channel)	−80 dB max
TRANSFER CHARACTERISTICS	
Gain	+1
Full Power Bandwidth	500 kHz
Slew Rate	13V/ μs
DC Gain Linearity (Sample Mode)	0.015% typ, 0.035% max
ANALOG INPUT/OUTPUT CHARACTERISTICS	
Voltage Range	±10V min
Absolute Max Input Voltage	±V supply
Offset Voltage Matching between S/Hs	±0.3 mV typ, ±1 mV max
Offset Over Temperature Range	±2 mV typ, ±5 mV max
Input Bias Current	50 nA max, 100 nA @ +125°C
Input Impedance	10^{10}
Buffered Output Resistance	0.05Ω typ, 0.2Ω max
DIGITAL INPUT CHARACTERISTICS	
Input Voltage	
Low	<+0.8 volt
High	>+2.4 volt
Input Current	
Leakage	±1 μ A
POWER REQUIREMENTS	
Supply Voltage Range	±15V, ±1V +5V, ±0.5V
Current Drain	
+15V	37 mA typ, 46 mA max
−15V	37 mA typ, 46 mA max
+5V	5 mA typ, 8 mA max
Power Dissipation	1W typ, 1.5W max
TEMPERATURE RANGE	
Operating	
C	0°C to +70°C
B	−55°C to +125°C
Storage	−65°C to +150°C
MECHANICAL	
Case Style	24-pin ceramic DIP

*Includes switching of MUX and settling of output buffer.

PACKAGE OUTLINE



Pin 1 is marked by a dot on the top of the package.

PIN-OUT FOR HS 9704 (* - HS 9705)

PIN	FUNCTION	PIN	FUNCTION
1	V_{IN_0}	24	NC
2	ANALOG GROUND	23	MUX LOAD**
3	V_{IN_1}	22	+15V
4	ANALOG GROUND	21	−15V
5	V_{IN_2}	20	ANALOG POWER GROUND
6	ANALOG GROUND	19	MUX OUT
7	V_{IN_3}	18	BUFFER OUT
8	ANALOG GROUND	17	DIGITAL POWER GROUND
9	+5V	16	S/HEN (S/H0)*
10	MEN	15	S/HA0 (S/H1)*
11	MA0	14	S/HA1 (S/H2)*
12	MA1	13	HOLD ALL (S/H3)*

Note: NC — No Internal Connection

**MUX LOAD must be grounded for proper operation.

ABSOLUTE MAXIMUM RATINGS (Referenced to GND)

(Exceeding any *one* of these parameters may cause permanent damage to the unit)

Analog Input Voltage . . . . . ±15V

Logic Input Voltage . . . . . −0.5V to +5V supply

Output Buffer Short Circuit Duration . . . . . indefinite

Output Mux Short Circuit Duration . . . . . indefinite @ 20 mA max

Supply Voltages
- ±15V . . . . . ±18V max
- +5V . . . . . −0.5V to +7V

Temperature Soldering Duration . . . . . 10 sec @ 300°C

Storage Temperature Range . . . . . −65°C to +150°C

APPLICATIONS INFORMATION

(Ref. Application Note — QUAD S/H Solves Acquisition Problems)

CONTROL FUNCTIONS

All control functions are described in Tables 1, 2, and 3.

MEN	MA0	MA1	V_{OUT}
H	X	X	X
L	L	L	S/H0
L	H	L	S/H1
L	L	H	S/H2
L	H	H	S/H3

Table 1. MUX Truth Table (HS 9704/9705)

S/HEN	HOLD ALL	S/HA0	S/HA1	FUNCTION
X	L	X	X	ALL HOLD
L	H	L	L	ONLY S/H0 HOLD
L	H	H	L	ONLY S/H1 HOLD
L	H	L	H	ONLY S/H2 HOLD
L	H	H	H	ONLY S/H3 HOLD
H	H	X	X	ALL TRACK

Table 2. S/H Truth Table (HS 9704)

S/H0	S/H1	S/H2	S/H3	FUNCTION
L	X	X	X	S/H0 Hold
X	L	X	X	S/H1 Hold
X	X	L	X	S/H2 Hold
X	X	X	L	S/H3 Hold
Can hold any combination of S/H's at any time				

Table 3. S/H Truth Table (HS 9705)

NOTES:
1. L indicates logic LOW 2. X indicates don't care.

S/H STEP

The S/H step (also known as the sample-to-hold offset) depends on the input voltage. We have internally trimmed the step to be less than 1 mV for a grounded input. With the internally trimmed offset matching, this makes the offsets in both track and hold mode negligible across all channels for a 12-bit system. The S/H step with +10V input is +3.5 mV and with −10V input is −3.5 mV and it is linear over the ±10V range.

This S/H step on the HS 9705 is also dependent on the S/H control lines. To improve the S/H step, pull up each S/H control line to the +5V supply through a 1K resistor.

INPUT EXPANSION

The HS 9704/05 can be easily expanded to more channels by connecting two or more devices in parallel. Also two (or multiples thereof) of the 9704/05s can be configured in a differential mode using an additional instrumentation amplifier.

Single-Ended Mode: Since the output of the analog multiplexer inside the HS 9704/05 can be disabled using the MEN input (pin 10), the output of another multiplexer can be fed into the input of the buffer amplifier. Figure 1 shows how to connect two HS 9704/05s in parallel to achieve eight input channels.

The MUX OUTPUT pins of both devices are tied together, and because the output buffer amplifiers of both devices remain connected to the multiplexer outputs there will be two independant outputs, tracking each other within a few millivolts. Only one MUX LOAD should be grounded to avoid overloading the S/H. One of them might be used to drive the following circuit (like an A/D converter) while the other one can be used for test and measurement purposes. Normally when a probe is connected to the buffer output, it's capacitance and lead length will have some influence on the measured signal, like ringing, overshoot etc. If the other buffer output is used for measurements, the probe will have no influence on the signal which goes to the ADC.

MUX TRUTH TABLE

MEN	MA0	MA1	V_{OUT}
H	L	L	V0
H	H	L	V1
H	L	H	V2
H	H	H	V3
L	L	L	V4
L	H	L	V5
L	L	H	V6
L	H	H	V7

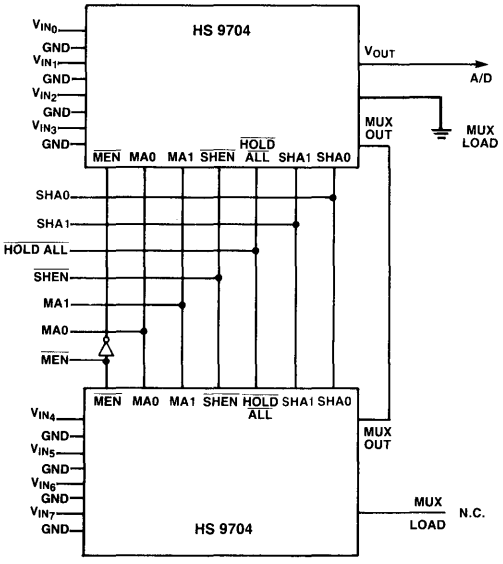


Figure 1. Single-Ended Mode

APPLICATIONS INFORMATION (continued)

INPUT EXPANSION (continued)

Differential Mode: Four differential channels can be held simultaneously, if two HS 9704/05s are connected using an additional instrumentation amplifier as shown in Figure 2. Another solution to that problem could be to use four instrumentation amplifiers in front of one Quad S/H, but this will require 16 instead of 4 precisely matching resistors and offset adjustment has to be made for four amplifiers instead of one. As in the single-ended mode more channels can be achieved by simply adding more Quad S/Hs in parallel. Four of them will be required for eight differential channels, six for 12 channels and so on.

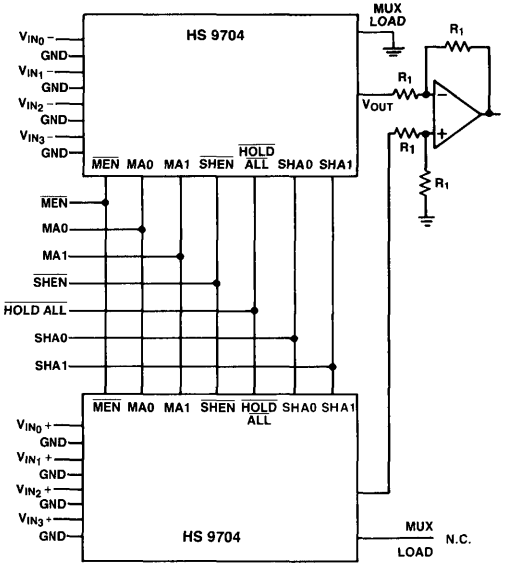
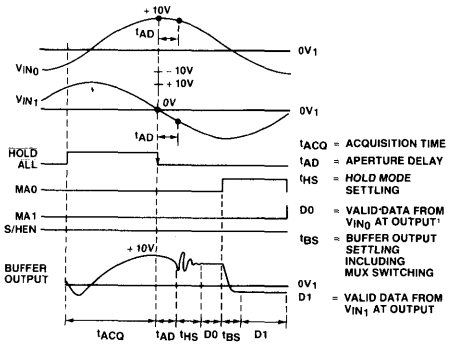


Figure 2. Differential Mode

TIMING DIAGRAMS



NOTES:
1. NOTE THAT BECAUSE THE OUTPUT SETTLING IS FASTER THAN THE ACQUISITION TIME THERE EXISTS NO OUTPUT SETTLING TIME IF THE OUTPUT HAS NOT BEEN MULTIPLEXED FROM ANOTHER CHANNEL.
2. FOR SIMULTANEOUS SAMPLING USING HS 9705 (UNDECODED) S/H0-S/H3 WOULD BE EXTERNALLY TIED TOGETHER AND PULSED AS HOLD ALL.
3. TIMING NOT DRAWN TO SCALE (FOR CLARITY). SEE SPECIFICATIONS FOR TRUE SCALE.

Figure 3. Timing Diagram of Simultaneous Sampling (HS 9704)[2]

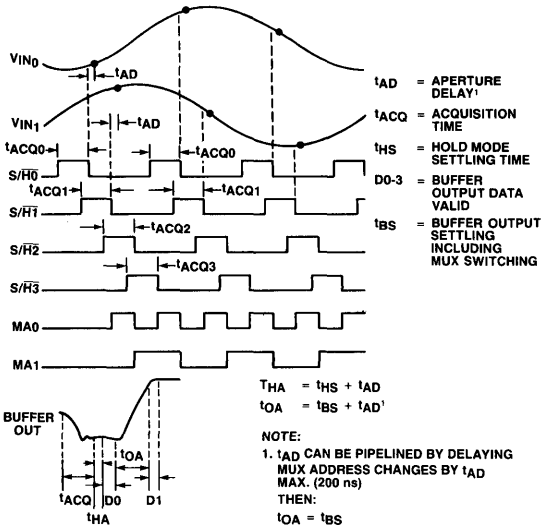
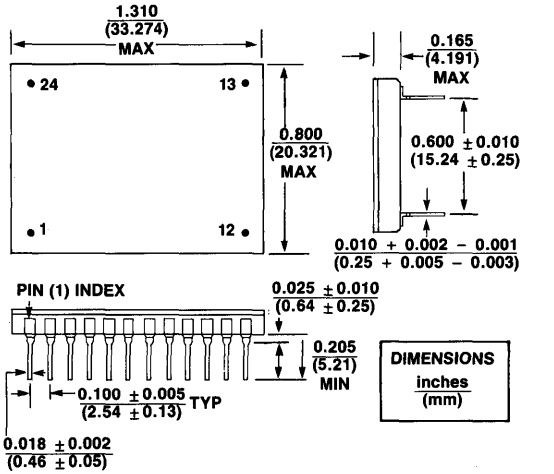


Figure 4. Pipelined Acquisition Sequential Sampling Using HS 9705.

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE
HS 9704B	QUAD S/H, MIL-STD-883 Rev. C	−55°C to +125°C
HS 9705B	QUAD S/H, MIL-STD-883 Rev. C (Hold any combination)	−55°C to +125°C
HS 9704C	QUAD S/H	0°C to +70°C
HS 9705C	QUAD S/H (Hold any combination)	0°C to +70°C

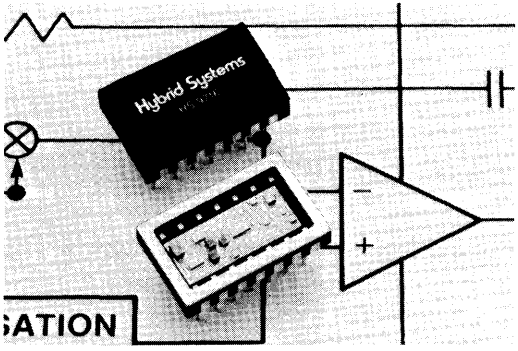


HS9716/HS9714

16/14-BIT ACCURATE SAMPLE/HOLD AMPLIFIER

FEATURES

- Dielectric absorption compensation to ½ LSB at 16-bits
- Droop rate of 0.05μV/μsec at +25°C
- Acquisition time of 10μsec max to 0.0008% of 20V (8μsec max to 0.003%)
- Hold mode feedthrough of −98 dB min (20 Vp-p, 20 kHz Signal)
- Pin-for-pin compatible with AD389



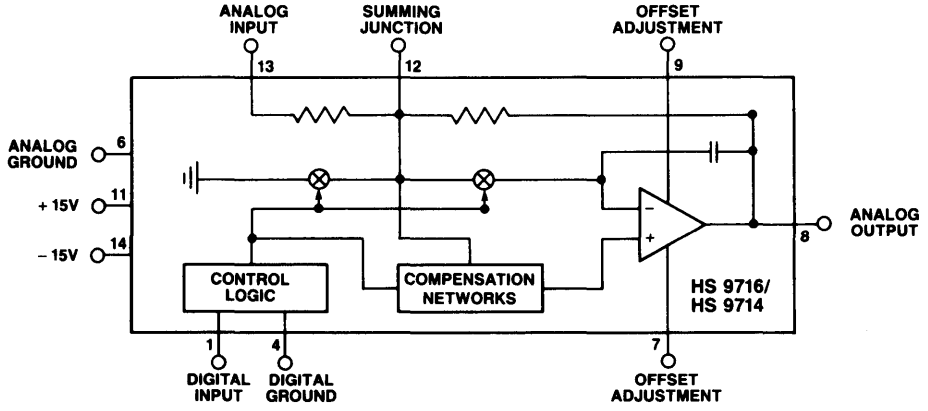
DESCRIPTION

The HS9716 is a high accuracy sample/hold amplifier designed for use in high resolution data acquisition applications. Compensation networks include dielectric absorption compensation to ½ LSB at 16 bits making the HS9716 suitable for use with true 16-bit A/D converters such as the HS9516. The HS9714 is suitable for use with 16-bit A/D converters with 14-bit accuracy such as the HS9576.

The HS9716/HS9714 comes complete with an internal hold capacitor and is available for use over the 0°C to 70°C temperature range and the −55°C to +125°C military temperature range. Full screening to MIL-STD-883C is available.

6

FUNCTIONAL DIAGRAM



SPECIFICATIONS

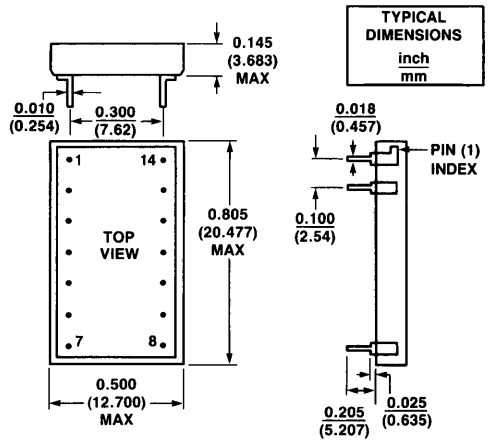
(Typical @ +25°C and nominal power supply voltages unless otherwise noted)

MODEL	HS 9716K	HS 9716TB	HS 9714K	HS 9714TB
ANALOG INPUT				
Voltage Range	±10V min	*	*	*
Overvoltage, No Damage	±15V max	*	*	*
Input Impedance	10K Ω	*	*	*
DIGITAL INPUT				
Track Mode, Logic "1"	2 to 5.5V	*	*	*
Hold Mode, Logic "0"	0 to 0.8V	*	*	*
Logic "1" Current	5μA max	*	*	*
Logic "0" Current	5μA max	*	*	*
ANALOG OUTPUT				
Voltage	±10V min	*	*	*
Current	2 mA min	*	*	*
Short Circuit Current	25 mA max	*	*	*
Impedance	0.1 Ω @ 1 kHz 12 Ω @ 1 MHz	*	*	*
DC ACCURACY/STABILITY				
Gain	−1.00 V/V	*	*	*
Gain Error	±0.02% max	*	±0.03% max	±0.03% max
Gain Nonlinearity (±10V Output Track)	±0.0005%	*	±0.001%	±0.001%
Gain Drift	5 ppm/°C max	*	*	*
Offset[1]	±30 mV max	*	*	*
Output Offset @ T_{min}, T_{max} (Track)	±1 mV	*	*	*
TRACK (SAMPLE) MODE DYNAMICS				
Frequency Response				
Small Signal (−3 dB)	1 MHz min	*	*	*
Full Power Bandwidth	0.2 MHz	*	*	*
Slew Rate	10V/μsec	*	*	*
Noise in Track Mode, DC to 1.0 MHz	50μVrms	*	50μVrms	50μVrms
TRACK (SAMPLE)-TO-HOLD SWITCHING				
Aperture Delay	30 nsec	*	*	*
Aperture Uncertainty	100 psec	*	*	*
Offset Step (Pedestal)	±2 mV	*	*	*
Switching Transient				
Amplitude	50 mV	*	*	*
Settling to 1 mV	0.5μsec	*	*	*
Settling to 0.3 mV	1μsec max	*	*	*
Dielectric Absorption	7.5μV/V max	*	15μV/V max	15μV/V max
HOLD MODE DYNAMICS				
Droop Rate	0.05μV/μsec max	*	0.1μV/μsec max	0.1μV/μsec max
Droop Rate at T_{max}	10μV/μsec max	*	*	*
Feedthrough Rejection				
(20 Vp-p @ 20 kHz)	98 dB min	*	90 dB min	90 dB min
(20 Vp-p @ 200 kHz)	90 dB min	*	86 dB min	86 dB min
Noise in Hold	25 μVrms	*	*	*
HOLD-TO-TRACK (SAMPLE) DYNAMICS				
Acquisition Time to ±0.0008% of 20V	5μsec typ, 10μsec max	*	N/A	N/A
Acquisition Time to ±0.003% of 20V	4μsec typ7.5μsec max	*	*	*
POWER REQUIREMENTS				
Nominal Voltages for Rated Performance	±15V (±3%)[2]	*	*	*
Supply Current				
$+V_S$	10 mA, 25 mA max	*	*	*
$-V_S$	10 mA, 23 mA max	*	*	*
Power Dissipation	300 mW, 720 mW max	*	*	*
Power Supply Rejection	100μV/V max	*	*	*
TEMPERATURE RANGE				
Operating	0°C to +70°C	−55°C to +125°C	0°C to +70°C	−55°C to +125°C
Storage	−40°C to +85°C	−65°C to +155°C	−40°C to +85°C	−65°C to +155°C
PACKAGE				
14-Pin Single DIP Ceramic				
Junction to Air, θ_{JA} (free air)	35°C/W	*		
Junction to Case, θ_{JC}	10°C/W	*		

NOTES:

1. Adjustable to zero.
2. ±5V to ±18V operating for operating to derated performance.
3. *Same as 9716K specification

PACKAGE OUTLINE



Pin 1 is marked by a dot on the top of the package.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	DIGITAL INPUT	14	−15V
2	NC	13	ANALOG INPUT
3	NC	12	SUMMING JUNCTION
4	DIGITAL GROUND	11	+15V
5	NC	10	NC
6	ANALOG GROUND	9	OFFSET ADJUSTMENT
7	OFFSET ADJUSTMENT	8	ANALOG OUTPUT

NC — No internal connection

ABSOLUTE MAXIMUM RATINGS

(Referenced to Grnd)
(Exceeding any one of these parameter may cause permanent damage to the unit.)

Voltage Between $+V_S$ and $-V_S$ Terminals 36V
Input Voltage . . . . . Actual Supply Voltage
Digital Input Voltage . . . . . −0.5V to +5.5V
Output Current, Continuous . . . . . ±40 mA
Internal Power Dissipation . . . . . 1000 mW
Storage Temperature Range . . . . . −65°C to +150°C
Output Short-Circuit Duration . . . . . Indefinite
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

OPERATING INSTRUCTIONS

OFFSET ADJUST

In most data acquisition systems only one offset adjustment is made. Usually, the offset adjust of the ADC is used to cancel all other accumulated system offsets. The offset of the HS 9716/9714 can be nulled by means of a 5kΩ to 25kΩ potentiometer between pins 7, 9, and 11. If the offset of the HS 9716/9714 is not adjusted, then connect pins 7 and 9 to pin 14, the negative supply. Otherwise, the high impedance of the null pin together with parasitic capacitances can cause tail effects.

SAMPLE/HOLD CONTROL

A TTL logic "1" applied to pin 1 switches the HS 9716/9714 into the track (sample) mode. In this mode, the device acts as an amplifier which exhibits normal operational amplifier behavior. Application of a logic "0" to pin 1 switches the HS 9716/9714 into the hold mode, with the output voltage held constant at the value present when the hold command is given.

INSTALLATION

GROUNDING

The HS 9716 is a true 16-Bit performance sample/hold amplifier. Grounding of this component, as with any 16-Bit component, must be done with care for full performance. The analog ground (pin 6) is isolated from the digital ground (pin 4) in order to allow for isolation of digital and signal path ground currents. A low noise grounding circuit is shown in Figure 1. Notice that the logic grounds return to the +5V supply on a wire separate from the wire providing a logic return for the A/D converter. Also notice that only analog grounds directly in the signal path are joined together with the A/D converter analog ground. The result of this is that the signal path ground remains quiet to <1LSB (150μV) and full performance is obtained.

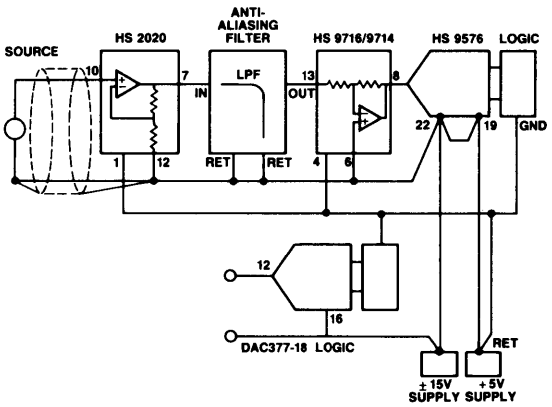


Figure 1. Basic Grounding Practice

DECOUPLING

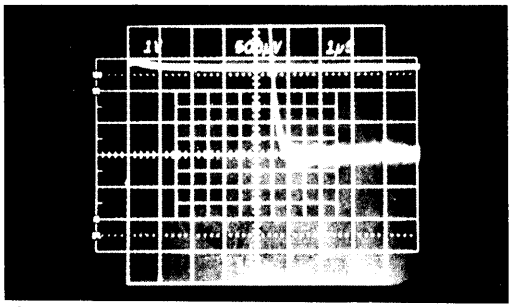
Internal 0.01μF power supply bypass capacitors are included in the HS 9716/9714 to maintain device stability. If the supply voltages contain excessive high frequency noise, additional external high frequency capacitors may be necessary to maintain low noise performance.

DISCUSSION OF SPECIFICATIONS

TERMINOLOGY

Sample/Hold Amplifier is actually a more common name for what really is a track/hold (T/H) amplifier. A true S/H amplifier normally spends most of its time in the hold mode. When commanded to the sample mode, it will take a very fast sample and immediately go back into the hold mode. A true T/H amplifier can track the input indefinitely and it can be in the hold mode indefinitely. In practice, most S/H amplifiers manufactured today are actually T/H amplifiers. This is why the HS 9716/9714 data sheet specifies track (sample) in many places.

Acquisition Time is the time required by the device to "switch" from the hold mode to the track (sample) mode. This time is measured between the application of a "track" command and the point at which the output has settled to within a specified error band. This time includes the switch delay time, slewing time and settling time for a given output voltage change.



Acquisition Time of a Worst Case 20V Step (Plus to Minus Input)
Top trace shows hold command going high in the second horizontal division. Lower trace shows output settling to a 500 μ V/div. scale.

Switching Transient Settling (Hold Mode Settling) is the time required for the device to stabilize in the hold mode to within specified limits of its final value after the hold mode signal has been given.

Aperture Delay is the time lag between the application of the "hold" command and the instant the output stops tracking the input. It consists primarily of the propagation delay of the switch driver. Since it is a known quantity, the "hold" command can be advanced to account for this delay.

Aperture Uncertainty (Jitter) is the variation in the aperture delay from sample to sample. This time uncertainty produces a voltage uncertainty proportional to the input slew rate.

Offset Step (Pedestal) is a track (sample)-to-hold offset that results from unequal charge transfers when the device is switched into the hold mode.

Feedthrough is the amount of analog input signal that is coupled through to the analog output while the circuit is in the hold mode. It is usually expressed as a ratio in dB's. Since feedthrough increases with frequency, it should be specified at a given frequency.

Droop Rate is the rate of change in output voltage over time while in the hold mode. The droop rate will determine how long a signal can be accurately held before it changes more than 1 LSB. This, in turn, determines the maximum conversion time that an A/D converter can have to be used with a particular S/H.

Full Power Bandwidth is the frequency at which a full scale input/output sine wave becomes slew rate limited to −3 dB.

Small Signal Bandwidth is the maximum analog signal frequency that can be tracked before the gain is reduced by 3 dB. This assumes the signal amplitude is small enough so as not to be slew rate limited.

Dielectric Absorption is the long term polarization of the dielectric material in the hold capacitor. This polarization changes the electric field strength in the capacitor producing a long term voltage error or "memory."

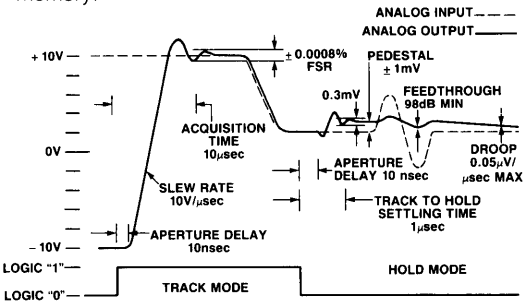


Figure 2. Pictoral Showing Various S/H Characteristics

KEY SPECIFICATIONS DETERMINING 16-BIT ACCURACY

The key specifications of the HS 9716 which support its accuracy to 16 bits are listed below.

1. Gain Nonlinearity — For a ±10V output range, gain nonlinearity is ±0.0005% which is less than ½ LSB at 16 bits (0.0008%).

2. Noise in Track Mode — For a noise bandwidth between DC and 1 MHz, the noise is specified at 20 μ V rms. Since ½ LSB at 16 bits is 150 μ V (FSR = 20V), the noise level is well below that required for 16-Bit accuracy.

3. Droop — The droop rate is specified at 0.05 μ V/ μ sec max. For a 150 μ V change (½ LSB, 16 bits, FSR = 20V), this S/H can accurately hold a signal for 3000 μ sec, or 3 milliseconds. This makes it ideal for use with 16-Bit integrating A/Ds. The droop rate at +125°C is specified at 10 μ V/ μ sec max. Thus, for a 150 μ V change (½ LSB at 16 bits), the HS 9716 can accurately hold a signal for 15 μ sec at +125°C.

4. Dielectric Absorption — This is specified at 7.5 μ V/V max. For a 20V input change which must be stored by the hold capacitor, the change in the stored voltage will be 150 μ V max, or ½ LSB at 16 bits.

5. Acquisition Time — This is specified as 10 μ sec max settling to ±0.0008% of 20V, or ½ LSB at 16 bits.

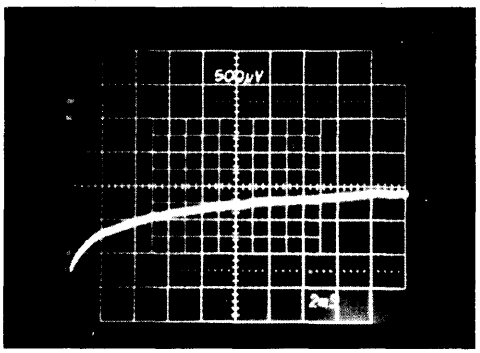
6. Feedthrough — Feedthrough rejection is specified at 98 dB min for a 20V p-p, 20 kHz input signal. This means that the hold mode output will move no more than 98 dB less than the input. For a ±10V input, this is ±125 μ V which is less than ±½ LSB at 16 bits.

DISCUSSION OF DIELECTRIC ABSORPTION

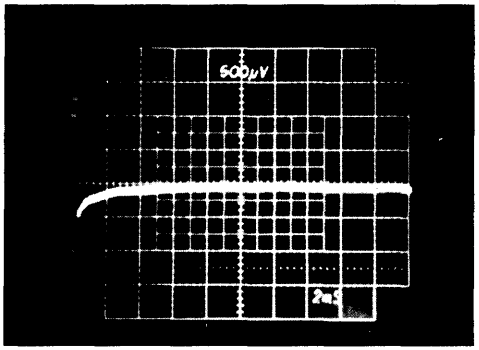
Dielectric absorption (D.A.) is often the biggest error source in a sample and hold or track/hold amplifier. D.A. is caused by either the rotation of polar molecules in a polar dielectric such as tantalum pentoxide, producing an error as big as 8%, or it is caused by slight distortions in the electron fields of molecules in a non-polar dielectric such as polystyrene, producing errors only as big as 0.04%.

Worst case dielectric absorption can be measured with a standard test. This test involves charging a capacitor for a period longer than T_{Max} (50ms), discharging it for a period shorter than T_{Min} (100 μs) and observing the open circuit voltage for a period longer than T_{Max} (50ms). This assures that all of the molecules in the dielectric are completely polarized before the charge on the capacitor plates is removed with enough speed that the polarizations are not neutralized. Obviously, if the application involves sample and hold times which are less extreme, then the dielectric absorption error will be less severe.

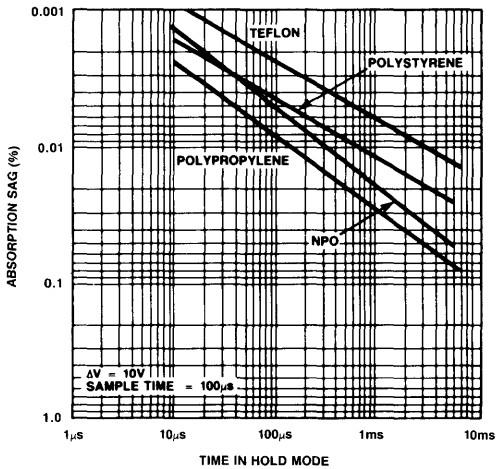
These molecular distortions and polarizations exhibit multiple exponential decays which may be modeled by adding series R-C networks in parallel with the hold capacitor with time constants ranging from 100 microseconds to 50 milliseconds. In the HS 9716/14, these multiple time constants are carefully matched and compensated to below 0.00075%/0.0015%. As can be seen in the absorption sag/sample time graph, even teflon capacitors exhibit absorption errors as large as 0.01% for a 10 microsecond sample time. Thus the HS 9716 is a substantial improvement from conventional sample and hold or track/hold amplifiers using the lowest dielectric absorbtion capacitors available. The two different hold mode oscilloscope photographs show how the HS 9716 hold capacitor dielectric absorption behaves without and with the compensation circuit connected.



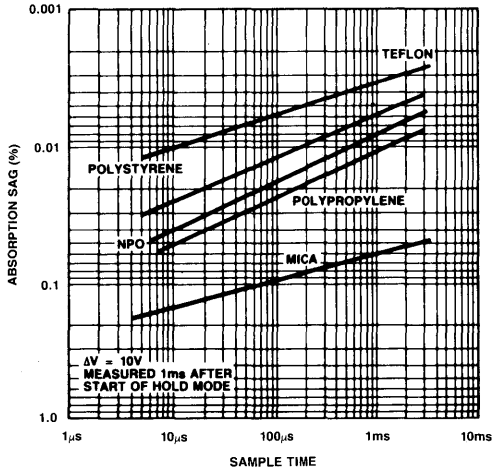
Hold Mode Dielectric Absorption Sag For 5μsec Sample Period Without Dielectric Absorption Compensation



Hold Mode Dielectric Absorption Sag For 5μsec Sample Period With Dielectric Absorption Compensation



Capacitor Dielectric Absorption



Capacitor Dielectric Absorption

APPLICATIONS

DIGITIZING DYNAMIC SIGNALS

Sample/hold amplifiers are normally used in front of A/D converters to hold the input voltage constant during conversion. Digitizing errors will result if the analog input signal varies by more than ½ LSB during conversion. In the case of the HS 9576, a 16-Bit A/D with a conversion time of 15 μ sec to 14 bits, this results in a low input frequency which can be accurately digitized as explained below:

For a sine wave input, its maximum rate of change is calculated as $2\pi Af$ where f = frequency and A = amplitude. If one allows a ½ LSB change (0.6mV) during conversion for a ± 10V input swing to the A/D converter, the maximum rate of change limit would be 0.6mV/15 μsec, or 0.04mV/ μsec. Thus, the maximum sine wave input frequency that can be accurately digitized is calculated as:

$$0.04mV/\mu sec = 2\pi Af$$

For a ± 10V input sine wave, this frequency limit is 0.63 Hz.

Expressed differently, the full scale bandwidth of the HS 9576 is slew rate limited to 0.63 Hz. By using a S/H, such as the HS 9716/9714 in front of the A/D (ref. Fig. 1), this bandwidth can be significantly increased. The S/H will "freeze" an input signal that is changing too rapidly for the A/D alone to handle and hold it constant while the A/D performs a conversion. A S/H can accurately "freeze" signals moving as fast as ½ LSB during its aperture uncertainty of 100 psec. Thus, for use with the HS 9576 to 14-Bit accuracy, the maximum rate of change limit would be 0.6mV (½ LSB, 14 bits, ± 10V swing) during 100 psec, or 6V/ μ sec, which is within the slew limit of the HS 9716/9714 (10V/ μsec). Thus, the maximum full scale input frequency that can be accurately digitized is calculated as:

$$6V/\mu sec = 2\pi Af$$

For a ± 10V full scale input, this frequency limit is 95 kHz. Expressed differently, the slew rate limited full scale bandwidth of the HS 9576 has now been increased to 95 kHz with the use of the HS 9716/9714 S/H.

Throughput and the Nyquist criteria are other factors which will determine the highest input signal frequency that can be sampled. For the combination of the HS 9576 and the HS 9716/9714, the throughput is related to the sum of the conversion time of the A/D (15 μ sec), the acquisition time of the S/H (5 μ sec) and the hold mode (switching transient) settling time of the S/H (1 μ sec). The total of 21 μ sec represents a throughput of 47.6 kHz. Based on the Nyquist criteria of sampling more than twice per cycle, the highest input signal frequency that can be accurately digitized is slightly less than 23.8 kHz.

OVERSAMPLING/UNDERSAMPLING

Oversampling is a technique where, for example, two samples are averaged to provide twice the resolution at half the bandwidth. The HS 9716 is well suited for this since its low noise of 20 μ V rms produces a dynamic range of 7.14 V rms (rms equivalent of 20 Vp-p sine wave) divided by 20 μ V rms, or 110 dB. This is equivalent to 18 bits of resolution.

Undersampling is a bandpass technique where one can sample a frequency higher than the Nyquist frequency. This is accomplished by bandpass filtering the input so that the bandwidth is less than the Nyquist frequency. The HS 9716 is well suited for this due to its large small signal bandwidth (1 MHz) and low aperture uncertainty (100 psec).

ORDERING INFORMATION

MODEL	DIELECTRIC ABSORPTION	TEMPERATURE RANGE
HS 9716K	7.5 μV/V	0°C to +70°C
HS 9714K	15 μV/V	0°C to +70°C
HS 9716TB	7.5 μV/V	−55°C to +125°C
HS 9714TB	15 μV/V	−55°C to +125°C

Specifications subject to change without notice.

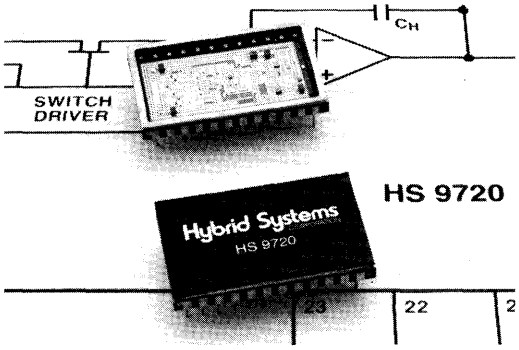
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

NOT RECOMMENDED FOR NEW DESIGNS SEE SP9730

HIGH SPEED, 12-BIT ACCURATE, SAMPLE/HOLD AMPLIFIER

FEATURES

- Pin-for-pin replacement for THA-05203, SHM-4860, TP-4860, MN376 and HTC-0300
- Hold mode feedthrough of −80 dB (20 Vp-p, 2.5 MHz)
- Maximum power dissipation 790 mW



DESCRIPTION

The HS9720 is a high speed sample/hold amplifier designed for use with 12-bit A/D converters. The maximum acquisition time of 200 nsec is specified to ±0.01% of 10V. The HS9720 is a complete sample/hold circuit containing a precision hold capacitor and a MOSFET switching driver. The HS9720 is particularly suited for use with high speed, 12-bit A/D converters.

The HS9720 is packaged in a 24-pin DIP and is specified for operation from 0°C to +70°C for commercial grades, and −55°C to +125°C for military grades. Full screening to MIL-STD-883C is available.

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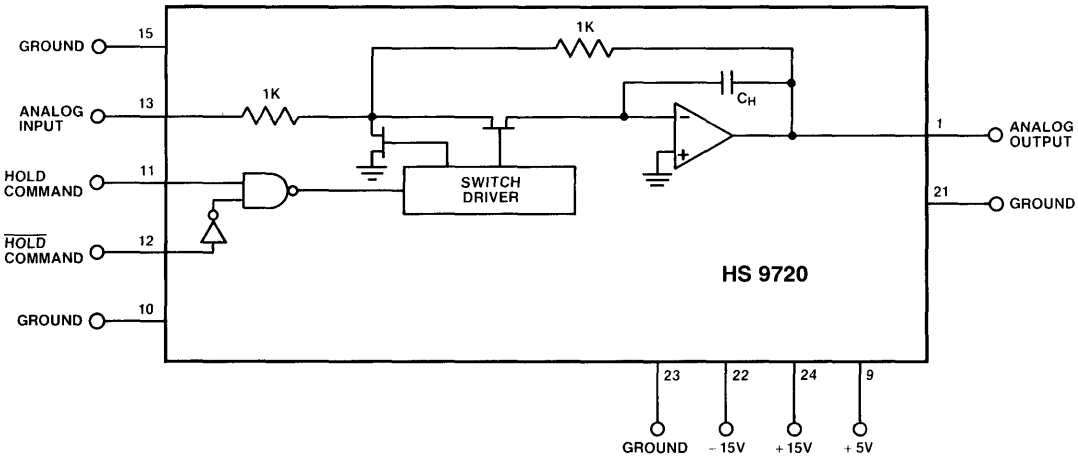
FUNCTIONAL DIAGRAM



SPECIFICATIONS

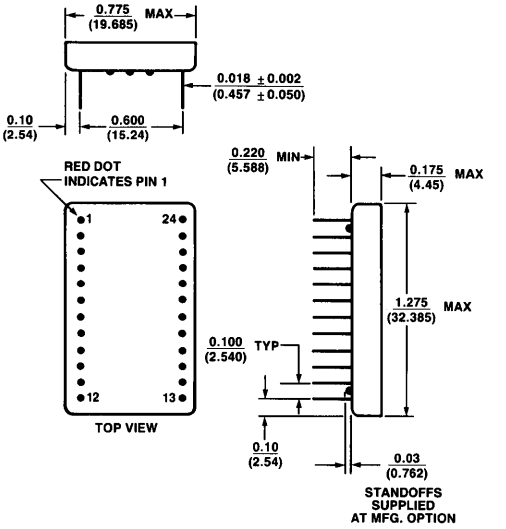
(Typical @ +25°C and nominal power supply voltages unless otherwise noted)

MODEL	HS 9720K	HS 9720TB
ANALOG INPUT		
Voltage Range	±11.5V typ, ±10.25V min	*
Input Impedance	1KΩ	*
DIGITAL INPUT[1]		
Logic "1"	+2V min to +5V max	*
Logic "0"	0V min to +0.8V max	*
Loading[2]	1 TTL Load	*
ANALOG OUTPUT		
Voltage	±11.5V typ, ±10.25V min	*
Current	±20 mA	*
Impedance	0.5Ω	*
Maximum Capacitive Load	200 pF	*
DC ACCURACY/STABILITY		
Gain	−1.00 V/V	*
Gain Error	±0.01% typ, ±0.1% max	*
Gain Nonlinearity	±0.005% typ, ±0.01% of FS max	*
Gain Drift	±1 ppm/°C typ, ±5 ppm/°C max	*
Offset	±0.5 mV, ±5 mV max	*
Offset Drift	±5 mV typ, ±20 mV max over full temperature range	*
TRACK (SAMPLE) MODE DYNAMICS		
Frequency Response		
Small Signal (−3 dB)	13 MHz typ, 8 MHz min	*
Full Power Bandwidth	3.5 MHz typ, 2.4 MHz min	*
Slew Rate	170V/μsec typ, 150V/μsec min	*
Noise in Track Mode		
DC to 5 MHz	90 μV rms	*
DC to 1 MHz	40 μV rms	*
DC to 0.1 MHz	13 μV rms	*
TRACK (SAMPLE)-TO-HOLD SWITCHING		
Aperture Delay[5]	6 nsec, 10 nsec max	*
Aperture Uncertainty	±50 psec	*
Offset Step (Pedestal)	±0.5 mV typ, ±10 mV max	*
Offset Step (Pedestal) Drift	±4 ppm of FSR/°C	*
Switching Transient		
Settling to ±10 mV (±0.1% FS)	40 nsec	*
Settling to ±1 mV (±0.01% FS)	60 nsec, 100 nsec max	*
Amplitude	180 mVp-p	*
HOLD MODE DYNAMICS		
Droop Rate	±0.5 μV/μsec, ±5 μV/μsec max	*
Droop Rate at T_{max}	±1.2 mV/μsec max	*
Feedthrough Rejection (20 Vp-p @ 2.5 MHz)	−90 dB typ, −80 dB min	*
HOLD-TO-TRACK (SAMPLE) DYNAMICS		
Acquisition Time to ±0.01% of 10V (±1 mV)	160 nsec, 200 nsec max	*
Acquisition Time to ±0.1% FS of 10V (±10 mV)	100 nsec, 170 nsec max	*
Acquisition Time to ±1% FS of 10V (±100 mV)	90 nsec	*
Acquisition Time to ±1.0% FS of 1V (+100 mV)	75 nsec	*
POWER REQUIREMENTS		
Nominal Voltages for Rated Performance	±15V (±3%)	*
	+5V (±5%)	*
Supply Current		
+15V	25 mA max	*
−15V	−25 mA max	*
+5V	+8 mA max	*
Power Dissipation	790 mW max	*
Power Supply Rejection	±0.5 mV/V	*
TEMPERATURE RANGE		
Operating	0°C to +70°C	−55°C to +125°C
Storage	−40°C to +85°C	−65°C to +155°C
PACKAGE		
24-Pin Double DIP		

NOTES:

1. Logic "1" to pin 12 or logic "0" to pin 11 will put the HS 9720 into the track (sample) mode.
2. One TTL load is defined as sinking 40 μA with a logic "1" applied and sourcing 1.6 mA with a logic "0" applied.
3. Manufacturer's option.
4. Lid is internally grounded.
5. From HOLD command pin 11.
6. FSR = 20 Volt Full Scale Range, FS = 10 Volt Full Scale.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	ANALOG OUTPUT	24	+15V
2	NC	23	GROUND
3	NC	22	−15V
4	NC	21	GROUND
5	NC	20	NC
6	NC	19	NC
7	NC	18	NC
8	NC	17	NC
9	+5V	16	NC
10	GROUND	15	GROUND
11	HOLD COMMAND	14	NC
12	$\overline{\text{HOLD}}$ COMMAND	13	ANALOG INPUT

NC — No internal connection.

ABSOLUTE MAXIMUM RATINGS

(Referenced to ground. Exceeding any one of these parameters may cause permanent damage to the unit.)

Voltage Between + 15V and − 15V Terminals	36V
Analog Input Voltage	Actual Supply Voltage
Digital Input Voltage	− 0.5V to + 5.5V
Output Current, Continuous	± 50 mA
Storage Temperature Range	− 65°C to + 150°C
Output Short-Circuit to Ground	Indefinitely
Lead Temperature (Soldering, 10 secs.)	+ 300°C

OPERATING INSTRUCTIONS

Sample/Hold Control

A TTL logic "0" applied to pin 11 (or a logic "1" applied to pin 12) will put the HS 9720 into the track (sample) mode. In this mode, the device acts as an amplifier which exhibits normal operational behavior. Application of a logic "1" to pin 11 (or a logic "0" applied to pin 12) will put the HS 9720 into the hold mode, with the output voltage held constant at the value present when the hold command is given.

INSTALLATION

Grounding

The HS 9720 is a high speed, 12-Bit accurate sample/hold amplifier. Grounding of this component must be done with care for full performance. The HS 9720 has four ground pins (pins 10, 15, 21, and 23). All must be tied together and connected to system analog ground as close to the package as possible. It is preferable to have a large analog ground plane beneath the HS 9720 and have all four ground pins soldered directly to it. Pin 10 is particularly noise sensitive because the fast switching currents from the switch drivers are grounded to this pin. Therefore, most digital ground currents will be routed through pin 10. Care must be taken to insure that no ground potentials exist between pin 10 and the other ground pins. Therefore, pin 10 must be tied to the analog and not the digital ground system.

DECOUPLING

Internal 0.01 μF power supply bypass capacitors are included in the HS 9720 to maintain device stability. If the supply voltages contain excessive high frequency noise, additional external high frequency capacitors may be necessary to maintain low noise performance.

OUTPUT LOADING

A capacitive load more than 50 pf will result in degrading acquisition time. Capacitive loads more than 250 pf will result in a continuous oscillation. The specified load resistor is 500Ω min. Lower value loads can be driven if the input/output range is lowered and the load current does not exceed ± 20 mA.

KEY SPECIFICATIONS DETERMINING 12-BIT ACCURACY

The key specifications of the HS 9720 which support its accuracy to 12 bits are listed below.

1. Gain Nonlinearity — For a ± 10V output range, gain nonlinearity is ± 0.01% max which is less than ½ LSB at 12 bits (0.012%).

2. Noise in Track Mode — For a noise bandwidth between DC and 5 MHz, the noise is specified at 90 μV rms. Since ½ LSB at 12 bits is 2.4 mV (FSR = 20V), the noise level is well below that required for 12-Bit accuracy.

3. Droop — The droop rate is specified at ± 5 μV/ μsec max. For a 2.4 mV change (½ LSB, 12 bits, FSR = 20V), this S/H can accurately hold a signal for 480 μsec. The droop rate at + 125°C is specified at 1.2 mV/ μsec max. Thus, for a 2.4 mV change, the HS 9720 can accurately hold a signal for 2 μsec at + 125°C.

4. Acquisition Time — This is specified at 200 nsec max settling to ± 0.01% of 10V, or ½ LSB at 12 bits.

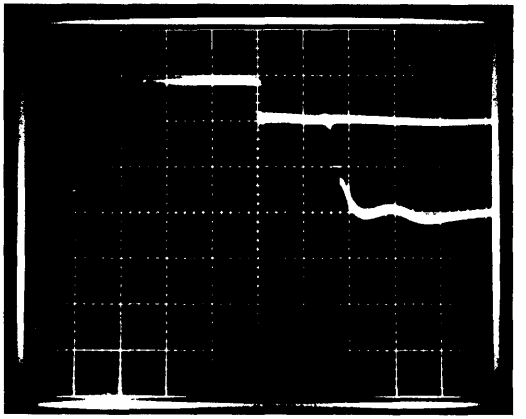
5. Feedthrough — Feedthrough rejection is specified at − 90 dB typ, − 80 dB min for a 20 Vp-p, 2.5 MHz input signal. This means that the hold mode will move no more than − 80 dB less than the input. For a ± 10V input, this is less than ½ LSB at 12 bits.

DISCUSSION OF SPECIFICATIONS

TERMINOLOGY

Sample/Hold Amplifier is actually a more common name for what really is a track/hold (T/H) amplifier. A true S/H amplifier normally spends most of its time in the hold mode. When commanded to the sample mode, it will take a very fast sample and immediately go back into the hold mode. A true T/H amplifier can track the input indefinitely and it can be in the hold mode indefinitely. In practice, most S/H amplifiers manufactured today are actually T/H amplifiers. This is why the HS 9720 data sheet specifies track (sample) in many places.

Acquisition Time is the time required by the device to "switch" from the hold mode to the track (sample) mode. This time is measured between the application of a "track" command and the point at which the output has settled to within a specified error band. This time includes the switch delay time, slewing time and settling time for a given output voltage change.



Acquisition Time of a + 10V Input Step

Top trace shows hold command going low in the middle of the photo. Lower trace shows output settling to a 2 mV/div. vertical scale. Horizontal scale is 100 nsec/div.

Switching Transient Settling (Hold Mode Settling) is the time required for the device to stabilize in the hold mode to within specified limits of its final value after the hold mode signal has been given.

Aperture Delay is the time lag between the application of the "hold" command and the instant the output stops tracking the input. It consists primarily of the propagation delay of the switch driver. Since it is a known quantity, the "hold" command can be advanced to account for this delay.

Aperture Uncertainty (Jitter) is the variation in the aperture delay from sample to sample. This time uncertainty produces a voltage uncertainty proportional to the input slew rate.

Offset Step (Pedestal) is a track (sample)-to-hold offset that results from unequal charge transfers when the device is switched into the hold mode.

Feedthrough is the amount of analog input signal that is coupled through to the analog output while the circuit is in the hold mode. It is usually expressed as a ratio in dB's. Since feedthrough increases with frequency, it should be specified at a given frequency.

Droop Rate is the rate of change in output voltage over time while in the hold mode. The droop rate will determine how long a signal can be accurately held before it changes more than 1 LSB. This, in turn, determines the maximum conversion time that an A/D converter can have to be used with a particular S/H.

Full Power Bandwidth is the frequency at which a full scale input/output sine wave becomes slew rate limited to −3 dB.

Small Signal Bandwidth is the maximum analog signal frequency that can be tracked before the gain is reduced by 3 dB. This assumes the signal amplitude is small enough so as not to be slew rate limited.

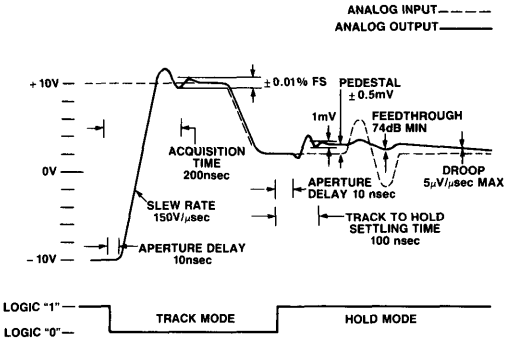


Figure 1. Pictoral Showing Various S/H Characteristics

APPLICATIONS

DIGITIZING DYNAMIC SIGNALS

Sample/hold amplifiers are normally used in front of A/D converters to hold the input voltage constant during conversion. Digitizing errors will result if the analog input signal varies by more than ½ LSB during conversion. In the case of the HS 9548, a 12-Bit A/D with a conversion time of 500 nsec to 12 bits, this results in a low input frequency which can be accurately digitized as explained below:

For a sine wave input, its maximum rate of change is calculated as 2π Af where f = frequency and A = amplitude. If one allows a ½ LSB change (2.4mV) during conversion for a ± 10V input swing to the A/D converter, the maximum rate of change limit would be 2.4mV/2 μsec, or 1.2mV/ μsec. Thus, the maximum sine wave input frequency that can be accurately digitized is calculated as:

$$1.2\text{mV}/\,\mu\text{sec} = 2\pi\,\text{Af}$$

For a ± 10V input sine wave, this frequency limit is 19 Hz.

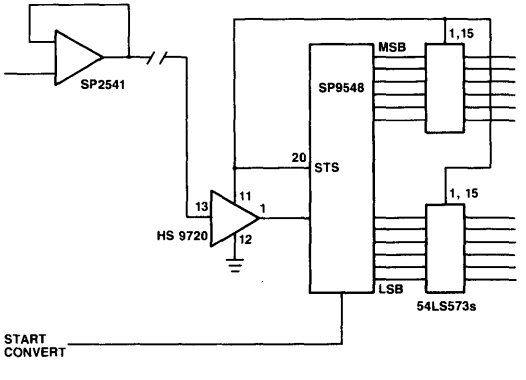
Expressed differently, the full scale bandwidth of the A/D is slew rate limited to 19 Hz. By using a S/H, such as the HS 9720 in front of the A/D , this bandwidth can be significantly increased. The S/H will "freeze" an input signal that is changing too rapidly for the A/D alone to handle and hold it constant while the A/D performs a conversion. A S/H can accurately "freeze" signals moving as fast as ½ LSB during its aperture uncertainty of 50 psec. Thus, the maximum rate of change limit would be 2.4mV (½ LSB, 12 bits, ± 10V swing) during 50 psec, or 48V/μ sec, which is within the slew limit of the HS 9720 (150V/μ sec min). Thus, the maximum full scale input frequency that can be accurately digitized is calculated as:

$$48V/\mu \text{ sec} = 2\pi Af$$

For a ± 10V full scale input, this frequency limit is 760 kHz. Expressed differently, the slew rate limited full scale bandwidth has now been increased to 760 kHz with the use of the HS 9720.

Throughput and the Nyquist criteria are other factors which will determine the highest input signal frequency that can be sampled. For the combination of 2μ sec ADC and the HS 9720, the throughput is related to the sum of the conversion time of the A/D (2 μ sec), the acquisition time of the S/H (0.2 μ sec) and the hold mode (switching transient) settling time of the S/H (0.1 μ sec). The total of 2.3μ sec represents a throughput of 434 kHz. Based on the Nyquist criteria of sampling more than twice per cycle, the highest input signal frequency that can be accurately digitized is slightly less than 217 kHz.

TYPICAL APPLICATION



Two importantly overlooked parameters are output impedance and settling time. The A/D is the S.A.R. type which means a current is injected into a comparator mode. This has a result of "dragging" the analog input to a new and distored value. The S/H must recover the signal to the original value before the comparator makes it's decision. For a 1.5μsec conversion this is 115 nanoseconds. The HS 9720 settles within a 100 nanoseconds, allowing it to be used with fast S.A.R. type A/Ds. Output impedance is also important because the input impedance of the A/D is relatively low (10kΩ). With a low output impedance of 0.5Ωmax, this allows for very little distortion due to the HS 9720, and an adequate drive capability.

TRACK/HOLD COMMAND

There are two hold commands for the HS 9720, the HOLD AND $\overline{\text{HOLD}}$. To use the HOLD command, tie $\overline{\text{HOLD}}$ (pin 12) to a TTL logic 0. To generate a track command apply TTL logic 0 to HOLD (pin 11). In this mode, the HS 9720 will effectively be an op-amp in the − 1 gain mode. A TTL logic 1 will put the HS 9720 into the hold command.

To incorporate the $\overline{\text{HOLD}}$ (pin 12), tie the HOLD (pin 11) to a TTL logic 1. A TTL logic 1 will put the HS 9720 into the track mode, a TTL logic 0 will put the HS 9720 into the hold mode. In using the $\overline{\text{HOLD}}$ command, there will be an additional delay of 4 nsec (typ), 12 nsec (max). This will increase aperture delay to 22 nsec (max), but will have no effect on settling time, acquisition time, gain, etc.

DRIVING THE INPUT OF THE HS 9720

The input resistance of the HS 9720 is a 1kΩ(typical) load. If driven by a weak source a loss of accuracy can occur due to the relatively low input impedance of the HS 9720. This is especially true, if the source is driving a long cable with a high capacitive load. A high speed, low output resistance op-amp should be used to drive the HS 9720 (such as the SP2541) to increase system performance and accuracy.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	MIL PROCESSING
HS 9720K	0°C to + 70°C	—
HS 9720TB	− 55°C to + 125°C	883C

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VERY HIGH SPEED 12-BIT ACCURATE, S/H AMPLIFIER

FEATURES

- 120 ηsec Acquisition Time to .01% for 5V
  200 ηsec Acquisition Time to .005% for 20V
- -94 dB Feedthrough Rejection Ratio (20V Step)
- Low Aperture Uncertainty of 50 psec rms
- Excellent Linearity: ±.005% for ±5V Range
  ±.001% for ±10V Range
- Low Droop Rate: ±5V/sec
- Low Distortion: -90 dB (5V p-p @ 100 kHz)

APPLICATIONS

- Wideband, High Speed Data Acquisition Systems
- Electronic Counter Measures
- Radar
- Deglitching Circuits
- Peak Detectors
- Telecommunications
- ATE

DESCRIPTION

The SP9730 is an ultra fast 12 bit linear sample-and-hold, featuring an acquisition time of 200 ηsec and 150 ηsec for 20V and 10V signal step respectively. The ultimate combination of speed, accuracy and stability is evidenced by low aperture uncertainty of 50 psec rms, 12 bit linearity, 30 MHz small signal bandwidth and maximum pedestal of ±5 mV.

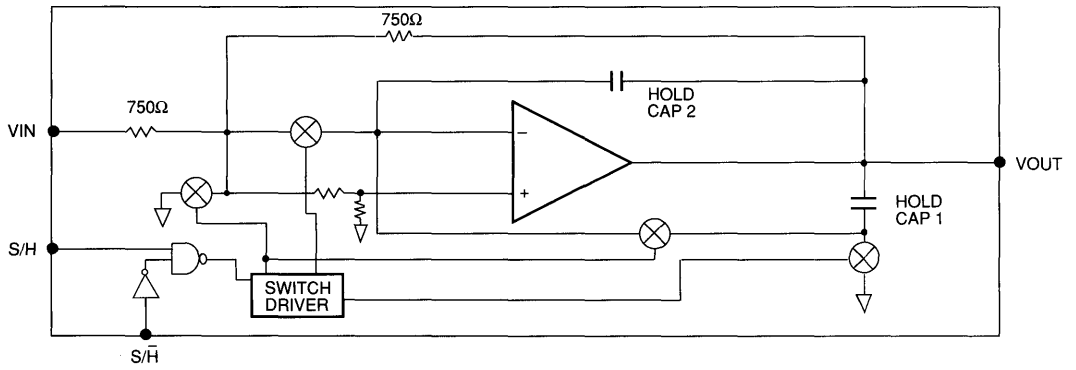
PRELIMINARY INFORMATION

The SP9730 accepts bipolar ±10V input signal, dissipates 1W and is available in the 24 pin dual-in-line package. The superior attributes of the SP9730 make it an ideal candidate to use in conjunction with a high speed 12-bit A/D in a multiplexed data acquisition applications such as guidance and control or ATE and signal processing systems such as ECM or Radar.

Two temperature ranges are available. The SP9730C is guaranteed over a case temperature of 0°C to +70°C; the SP9730B is MIL-STD-883C screened over a temperature range of -55°C to +125°C.

6

FUNCTIONAL DIAGRAM



(Typical @ +25°C and ±15V power supply voltages unless otherwise noted)		
PARAMETER	**SP9730C**	**SP9730B**
ANALOG INPUT		
Input Voltage	±10V	*
Input Bias Current	100 pA	*
Input Impedance	750Ω	*
DIGITAL INPUT		
Logic "0"	0V min, .8V max	*
Logic "1"	2V min, +5V max	*
ANALOG OUTPUT		
Voltage	±10V	
Current	±2 mA @ ±10V Swing	
TRANSFER CHARACTERISTICS		
Gain	-1	*
Gain Error	.01%	*
Offset Error	±5 mV (max)	*
Dielectric Absorption	.0005%	*
Linearity		
20V Range	±.001%	*
10V Range	±.005%	*
SAMPLE MODE DYNAMICS		
Frequency Response		
Small Signal (-3 dB)	16 MHz	*
Full Power BW (20V p-p)	8 MHz	*
Slew Rate	200V/µsec	*
Distortion		
5V p-p @ 100 kHz	80 dB	*
HOLD MODE DYNAMICS		
Droop Rate	50 (100 max) µV/µsec	*
Feedthrough Rejection 20V step	-80 dB	*
SAMPLE TO HOLD SWITCHING		
Aperture Delay	6 nsec	
Aperture Uncertainty	±50 psec RMS	*
Pedestal	±5 mV max	*
HOLD-TO-SAMPLE-DYNAMICS		
Acquisition Time		
20V Step to .005%	200 nsec	*
10V Step to .005%	150 nsec	*
5V Step to .01%	120 nsec	*
POWER REQUIREMENTS		
Nominal Voltages for Rated Performance		
+Analog	+15V	*
-Analog	-15V	*
Digital	+5V	*
Power Dissipation	1.0W	*
TEMPERATURE RANGE		
Operating	0°C to 70°C	-55°C to +125°C
Storage	-40°C to +85°C	-65°C to +155°C
PACKAGE	24 Pin Double DIP	

*Same as SP9730C

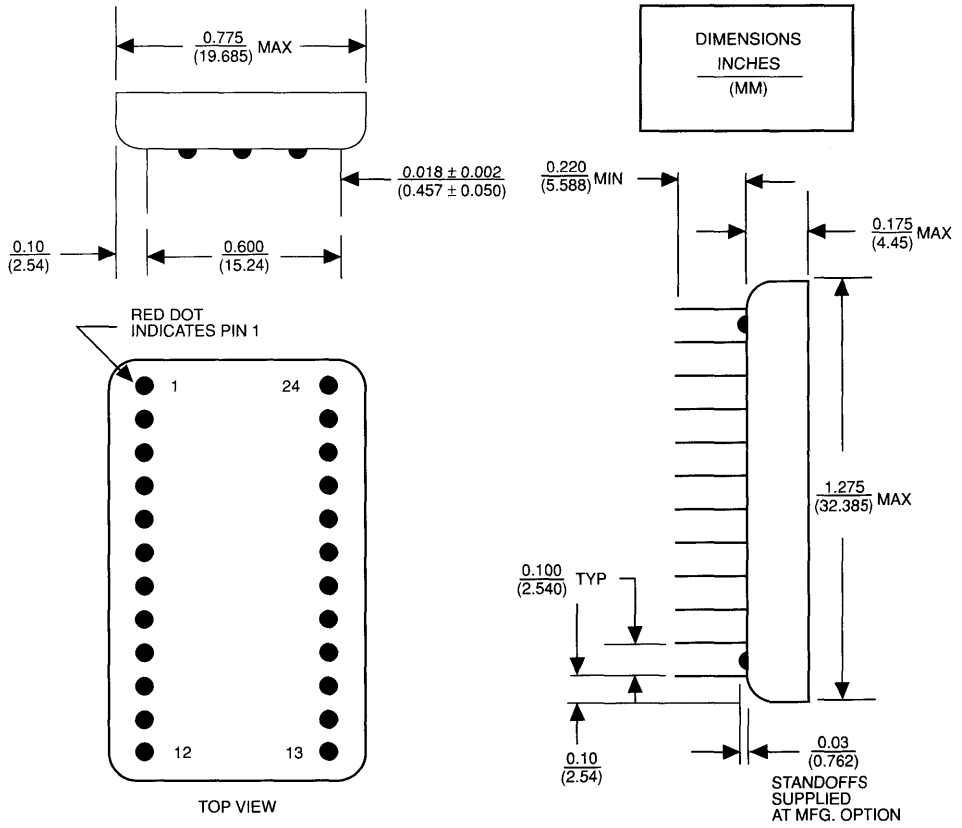
PIN ASSIGNMENTS

PIN	FUNCTION
1	Analog Output
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	NC
9	+5V Supply
10	Ground
11	Hold Command
12	$\overline{\text{Hold}}$ Command
13	Analog Input
14	NC
15	Ground
16	NC
17	NC
18	NC
19	NC
20	NC
21	Ground
22	-15V Supply
23	Ground
24	+15V Supply

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	SCREENING
SP9730C	0°C to 70°C	—
SP9730B	-55°C to +125°C	MIL-STD-883

PACKAGE OUTLINE



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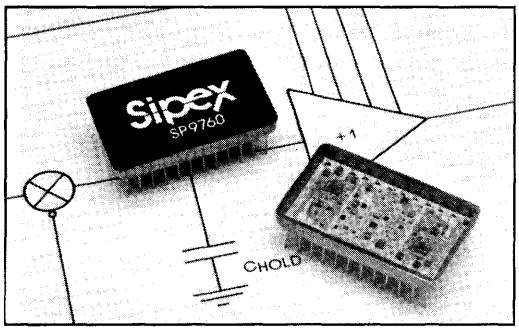
ULTRA HIGH SPEED 16-BIT ACCURATE, TRACK & HOLD AMPLIFIER

FEATURES

- 350 ηsec Acquisition Time to .005% for 20V step
  250 ηsec Acquisition Time to .005% for 10V step
- -94 dB Feedthrough Rejection Ratio (20V step)
- Low Aperture Uncertainty of 75 ρsec rms
- Excellent Linearity: ±.0005% for ±5V range
  ±.001% for ±10V range
- Low droop rate: 1V/sec
- Low distortion: -90 dB (5V p-p @ 100 kHz)
  -88 dB (20V p-p @ 10 kHz)



DESCRIPTION

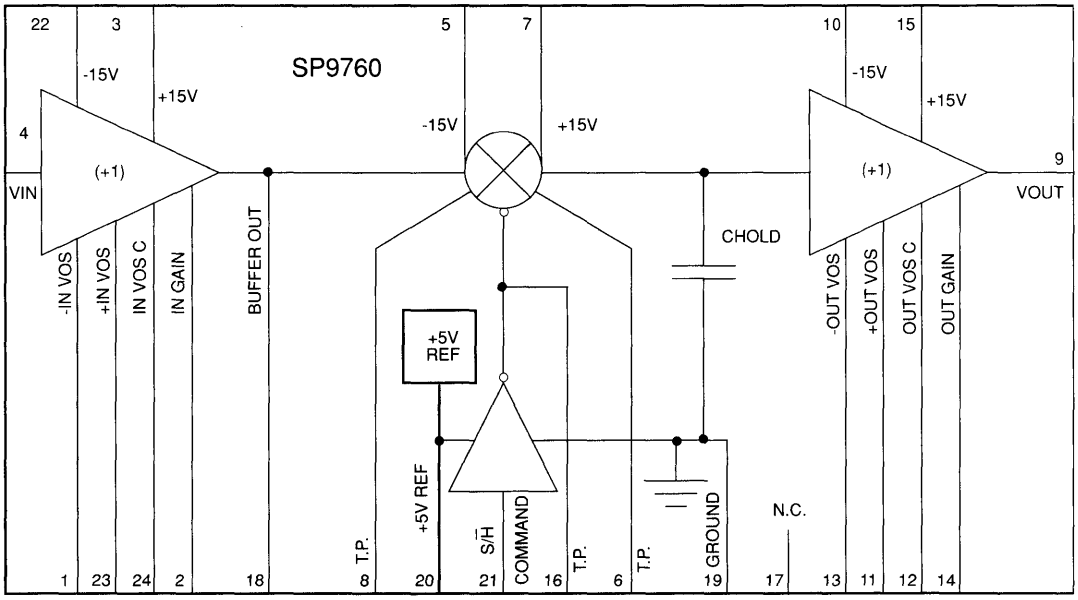
The SP9760 is an ultra fast 16 bit linear sample-and-hold, featuring an acquisition time of 250 ηsec and 350 ηsec for 20V and 10V signal step respectively. The ultimate combination of speed, accuracy and stability is evidenced by low aperture uncertainty of 75 ρsec rms, 16 bit linearity, 30 MHz small signal bandwidth and maximum pedestal of ±1mV. Two proprietary Dielectric-Isolation-based ASICs are utilized in the design of the SP9760 to achieve true 16 bit performance at specified conversion rates.

The SP9760 accepts bipolar ±10V input signal, dissipates 825 mW and is available in the 24 pin dual-in-line package. The superior attributes of the SP9760 make it an ideal candidate to use in conjunction with a high speed14 to 16 bit ADC's in multiplexed data acquisition applications such as audio digitizing, ATE, industrial data acquisition and signal processing such as magnetic resonance imaging and radar.

Two temperature ranges are available. The SP9760C is guaranteed over a case temperature of 0°C to +70°C; the SP9760B is MIL-STD-883C screened over a temperature range of -55°C to +125°C.

6

FUNCTIONAL DIAGRAM



SPECIFICATIONS

	SP9760C 0°C to 70°C			SP9760B (PRELIMINARY) -55°C to +125°C			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG INPUT							
Input Voltage	±10			±10			V
Input Bias Current		100			100		pA
Input Impedance		100			100		MΩ
DIGITAL INPUT							
Logic "0"	0		0.8	0		0.8	V
Logic "1"	2.0		5.0	2.0		5.0	V
ANALOG OUTPUT							
Voltage	±10			±10			V
Current		20			20		mA
Impedance		.1			.1		Ω
Capacitive Load[1]							
SAMPLE MODE DC TRANSFER CHARACTERISTICS							
Offset Error		±1	±5		±5	±20	mV
Offset Drift		±20			±50	±200	µV/°C
Gain		+1			+1		
Gain Error		±.03	±.1		±.05	±.2	%FSR
Gain Drift		±2	±20		±2	±20	ppm/°C
Linearity							
20V Range		.001	.002		.001	.002	%FSR
10V Range		.0005			.0005		%FSR
SAMPLE MODE DYNAMICS							
Frequency Response							
Small Signal (-3 dB)		30			20		MHz
Full Power (20V p-p)		2			1		MHz
(10V p-p)		4			2		MHz
Slew Rate	75	120		40	60		V/µsec
Acquisition Time							
±20V Step to .0015%		350	500		600	700	nsec
±10V Step to .0015%		250			450		nsec
±5V Step to .01%		200			375		nsec
Distortion							
5V p-p @ 100 kHz		-90			-80		dB
20V p-p @ 10 kHz		-88			-78		dB
HOLD MODE DYNAMICS							
Pedestal Offset Error		±0.2	±1.0		±2	±5	mV
Pedestal Offset Drift		±30			±20	±50	µV/°C
Pedestal Gain Error		±.002			±.005	±.01	%FSR
Pedestal Linearity		±.0005	±.002		±.0005	±.002	%FSR
Droop Rate		±1	±100		±150	±1000	µV/µS
Feedthrough Rejection[2, 5]		-103	-90		-103	-90	dB
Dielectric Absorption[2]		.0005			.001		%FSR
Aperture Delay		30			30		nsec
Aperture Uncertainty		75			75		ps RMS
Sample to Hold Settling[3]		150			150		nsec
Noise[4]		300			300		µV RMS

SPECIFICATIONS

	SP9760C 0°C to 70°C			SP9760B (PRELIMINARY) -55°C to +125°C			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
POWER REQUIREMENTS							
Nominal Voltage							
$+V_S$		+15			+15		V
$-V_S$		-15			-15		V
Supply Current							
$+V_S$		31			31		mA
$-V_S$		24			24		mA
Power Dissipation		825			825		mW
Power Supply Rejection		100			100		µV/V
TEMPERATURE RANGE							
Operating		0 to +70			-55 to +125		°C
Storage		-40 to +85			-65 to +150		°C
ABSOLUTE MAXIMUM RATINGS							
$\pm V_S$			16			16	V
Analog Input	$-V_S$		$+V_S$	$-V_S$		$+V_S$	V
Digital Input	-1		+6	-1		+6	V
Junction Temp			150				°C
Θ_{JC}			30.3				°C/Watt

NOTES

1. $C_{load} < {}^{Iload}/(\partial V_{out}/\partial I_{out})$. See recommendations on capacitive loading.
2. ±20V Step
3. To ±0.005%
4. DC to 30 MHz
5. Feedthrough rejection tested at 25°C.

6

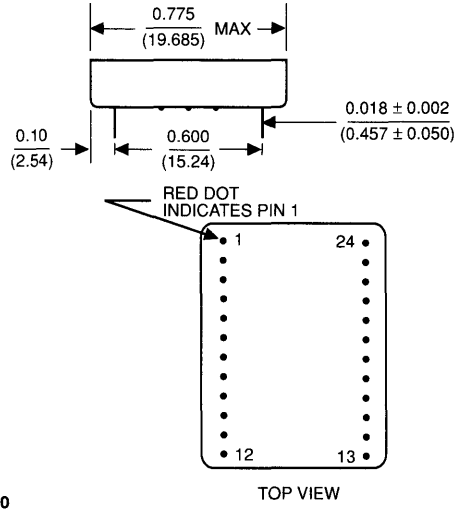
PIN ASSIGNMENTS

PIN	FUNCTION
1	-In V_{os}
2	In Gain
3	+15V
4	V_{in}
5	-15V
6	TP
7	+15V
8	TP
9	V_{out}
10	-15V
11	+Out V_{os}
12	Out V_{os} C
13	-Out V_{os}
14	Out Gain
15	+15V
16	TP
17	NC
18	Buffer Out
19	Ground
20	+5V Ref
21	S/$\overline{H}$ In
22	-15V
23	+In V_{os}
24	In V_{os} C

ORDERING INFORMATION

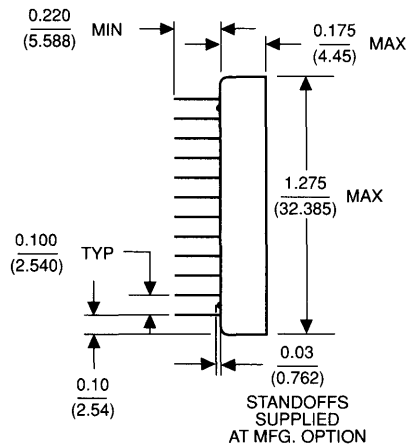
MODEL	TEMPERATURE RANGE	DESCRIPTION
SP9760C	0°C to 70°C	—
SP9760B	-55°C to +125°C	MIL-STD-883

PACKAGE OUTLINE

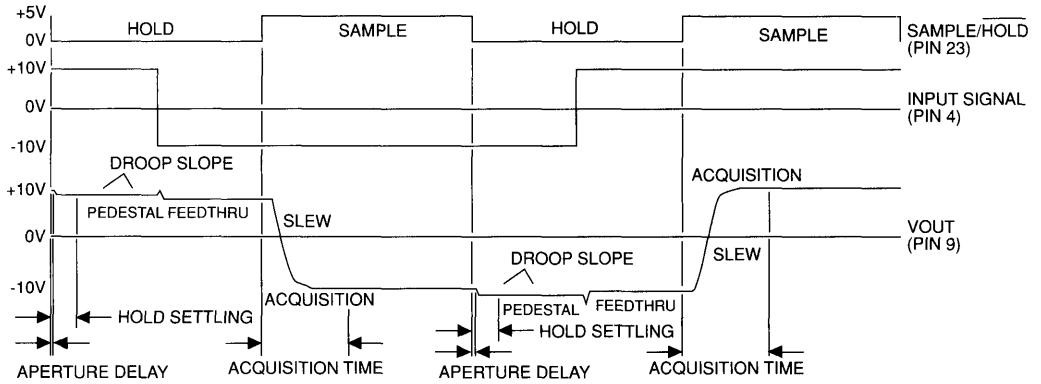


FUNCTIONAL PIN DESCRIPTIONS

Pins 1, 23, 24	Input Offset Trim: Trim pot connection for external offset trim of input buffer.
Pins 11, 12, 13	Output Offset Trim: Trim pot connection for external offset trim of output buffer.
Pin 2	Input Gain Trim: Trim pot wiper connection for external gain trim of input buffer.
Pin 14	Output Gain Trim: Trim pot wiper connection for external gain trim of output buffer.
Pin 4	Analog Input: High impedance signal input to first buffer.
Pin 9	Analog Output: Low impedance output of S/H amplifier.
Pin 21	S/$\overline{H}$ In: Logic control of sample mode (high) and hold mode (low).
Pin 20	+5V Ref Out: Internal reference generated with 78L05.
Pin 19	GND: Only ground pin.
Pin 3	+15V Input Supply: Input buffer positive supply.
Pin 22	-15V Input Supply: Input buffer negative supply.
Pin 15	+15V Output Supply: Output buffer positive supply.
Pin 10	-15V Output Supply: Output buffer negative supply.
Pin 7	+15V Gate Drive Supply: Analog switch positive supply.
Pin 5	-15V Gate Drive Supply: Analog switch negative supply.
Pin 18	Buffer Out: Output of input buffer.
Pin 16	TP: Factory test point.
Pin 8	TP: Factory test point.
Pin 6	TP: Factory test point.
Pin 17	No Connect.



TIMING DIAGRAM



TIMING

The timing diagram illustrates the critical timing points for the SP9760. This is illustrated by sending the SP9760 into hold and back to sample on both positive and negative going signals. The key points on the timing diagram are defined below.

Aperture Delay - the difference in time between when the hold signal is given and the SHA holds the input signal.

Hold Settling - the time it takes the SHA to settle to the held signal.

Pedestal - the difference in voltage between sample and hold for the same input voltage.

Droop Rate - the rate at which the held signal changes (droops) due to leakage of charge off the hold capacitor.

Feedthru - the extent to which a signal on the input of the SHA, during hold mode, will change the signal being held.

Slew Rate - the rate at which the sample and hold amplifier changes to the new signal being sampled.

Acquisition Time - the time it takes the sample-and-hold to settle and fully acquire a new signal. This time is dependent on input voltage change and accuracy required.

SUPPLY BYPASSING

Power supply bypassing is necessary to prevent oscillation with the SP9760 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within 1/4" to 1/2" of the device package) to a ground plane. Capacitors should be 0.1 µF in parallel (for each supply pin) with a 10 µF solid tantalum capacitor for each supply voltage.

RECOMMENDED LAYOUT PRECAUTIONS

RF/video printed circuit board layout rules should be followed when using the SP9760 since it will provide power gain to frequencies over 30 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors.

The optional gain adjust pots and the offset adjust pots should be mounted within one inch of the SP9760. An etch guard ring should be laid around the gain and offset adjust circuitry and tied to the output of each buffer to prevent dynamic deterioration from stray capacitance. (See Figure 1.)

GAIN AND OFFSET ADJUSTMENTS

In most system applications there will be no need to adjust the gain and offset of the SP9760 separately. The system gain and offset adjustments should be used instead. However, it is not recommended that the gain and offset adjustment pots connected to the SP9760 be used to compensate system gain and offset errors.

Figure 1 shows the recommended gain and offset adjustment circuit. The gain and offset adjustments should be repeated for each buffer.

IMPORTANT: The lead length on the gain and offset adjustment circuit should be kept short (within one inch) to avoid oscillation or deterioration of dynamic performance.

The DVM must have both inputs floating. A hand held DVM with 100 µV or finer resolution may be used for this measurement.

For very critical adjustments a 5 minute warmup is recommended for the SP9760.

GAIN ADJUSTMENT

The gain adjustment should be done before the offset adjustment to avoid the effect that the gain pot has on the offset voltage.

The gain adjustment also affects the output resistance of the SP9760 buffers. The output resistance will be closest to zero ohms when the gain is closest to one.

The gain pot is adjusted in sample mode while plus full scale and minus full scale voltages (as defined by the user's system) are applied to the SP9760 by an external voltage source or by the previous stage in the system. This applied voltage needs to be only 10% accurate because the floating DVM is measuring gain error directly. The

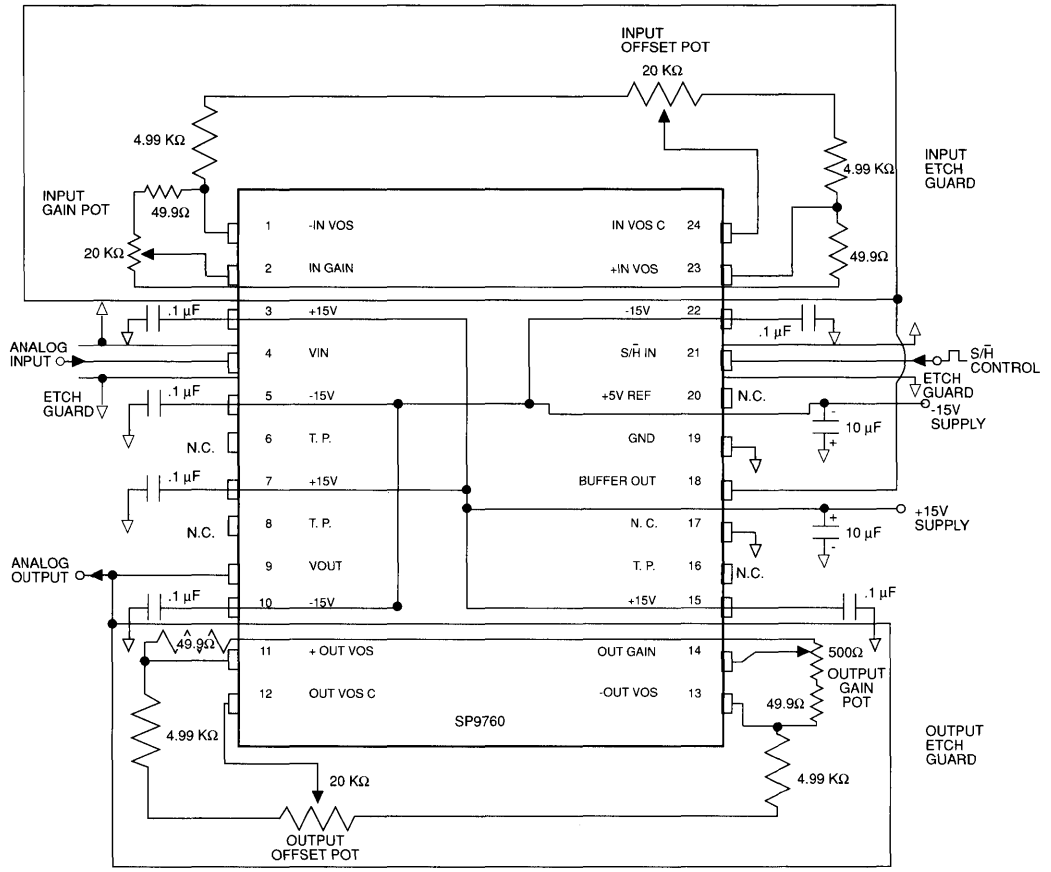


FIGURE 1
SUGGESTED TOPOLOGY AND RELATIVE PLACEMENT OF COMPONENTS

gain error has been compensated when the floating DVM reads the same value for plus full scale and minus full scale input voltages. The input voltage applied to the SP9760 can be a manually controlled DC voltage or a slow 2 to 10 second period full scale square wave.

OFFSET ADJUSTMENT

After the gain has been adjusted, the remaining error is eliminated by the offset adjustment. The input voltage applied to the SP9760 should be zero volts. The offset pot is adjusted until the floating DVM reads zero volts.

CAPACITIVE LOADING

Two considerations must be taken into account when driving capacitive loads. These are frequency stability and charge current magnitude.

For some values of load capacitance (>50 pf) it may be necessary to isolate the capacitive load with a resistor from 1Ω to 10Ω to reduce ringing or oscillation tendency. The desired step response can be obtained with the right resistor value for each application. (See Figure 2.)

The charge current magnitude must be controlled not to exceed the maximum rated output current for the SP9760. If the maximum output current is exceeded, the output stage will saturate during a transient and will take longer to recover.

The charge current into the capacitor is established by

$$I_{C\ load} = C_{load} \times \frac{dv}{dt}$$

The charge current can be limited by controlling the slew rate of the signals driving the SP9760, by reducing the amount of capacitive loading or by adding resistance in series with the capacitive load.

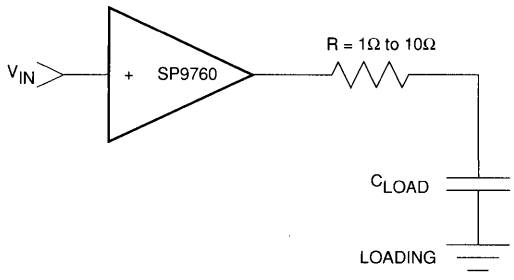


FIGURE 2
CAPACITIVE LOADING

APPLICATIONS

The SP9760 is suited for data acquisition and signal processing applications with high speed 14 and 16-bit analog-to-digital converters. In figure 3 the SP9760 is connected to an SP9588 14-bit 2 µsec analog-to-digital converter. The figure shows everything required for these two parts to work together, in a 0 to +10V unipolar mode. As can be seen in graph 1 with an input signal of 120 kHz at 0 dB the signal-to-noise + distortion ratio is 70 dB.

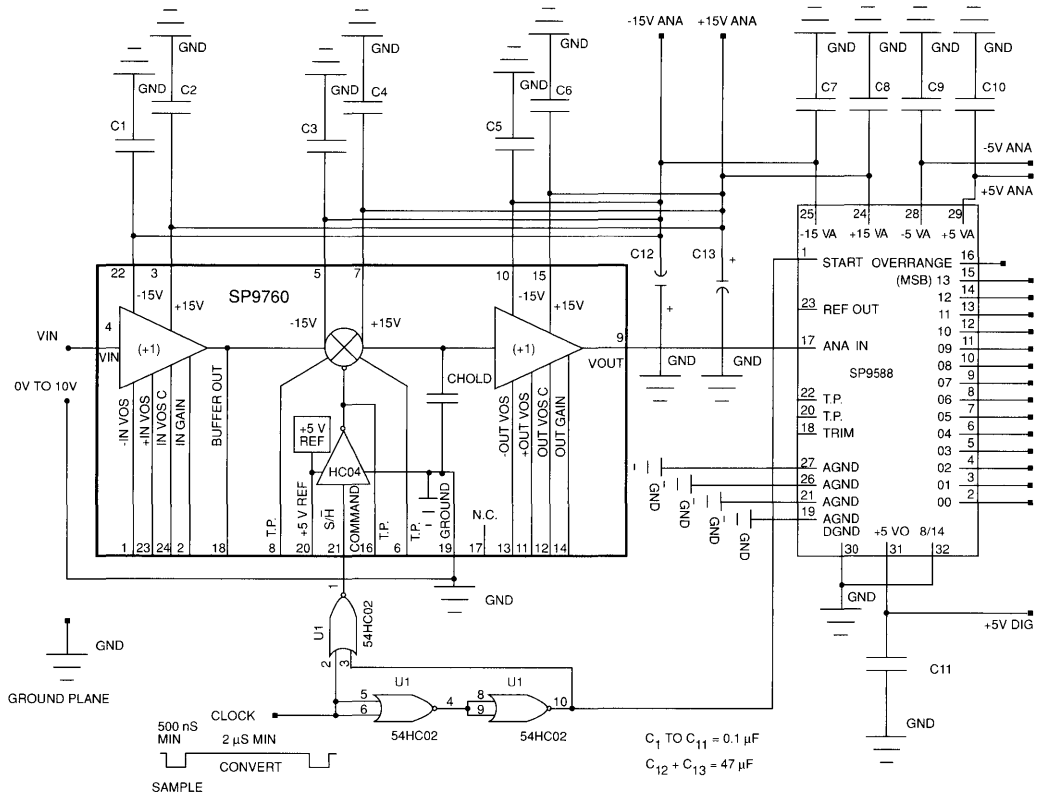
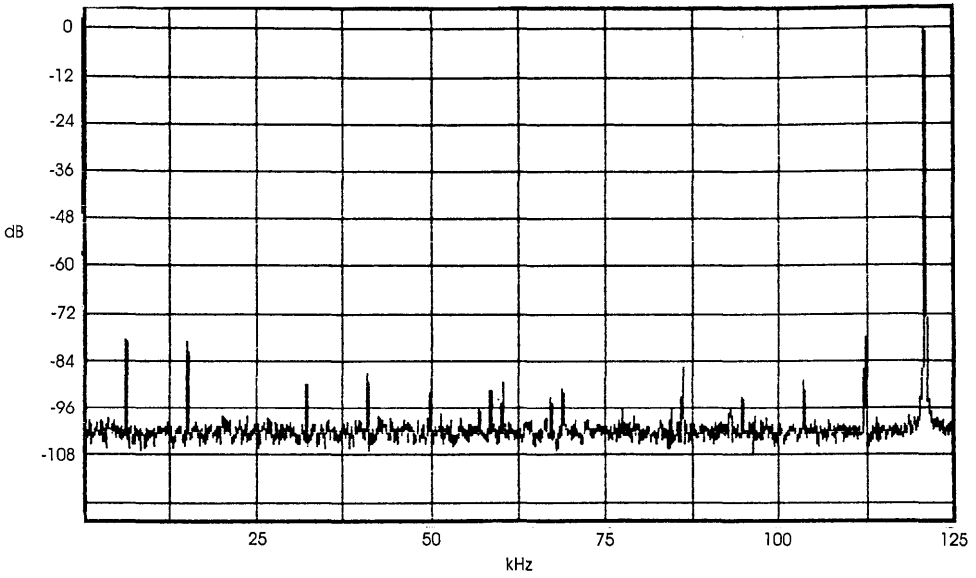


FIGURE 3
0V TO 10V UNIPOLAR DATA ACQUISITION SYSTEM

Sampling Rate = 250 kHz
Input Frequency = 120 kHz
Input Amplitude = 10 Volts p-p (0 dB)
Noise Floor < -100 dB
Maximum Harmonic < -72 dB



SIGNAL-TO-NOISE + DISTORTION RATIO
SINAD = 69.36 dB

Graph 1

The SP9760 and SP9588 can be used in the bipolar mode and be AC coupled for AC signal processing applications. In figure 4 the complete schematic is given for ±5V input range and AC coupling.

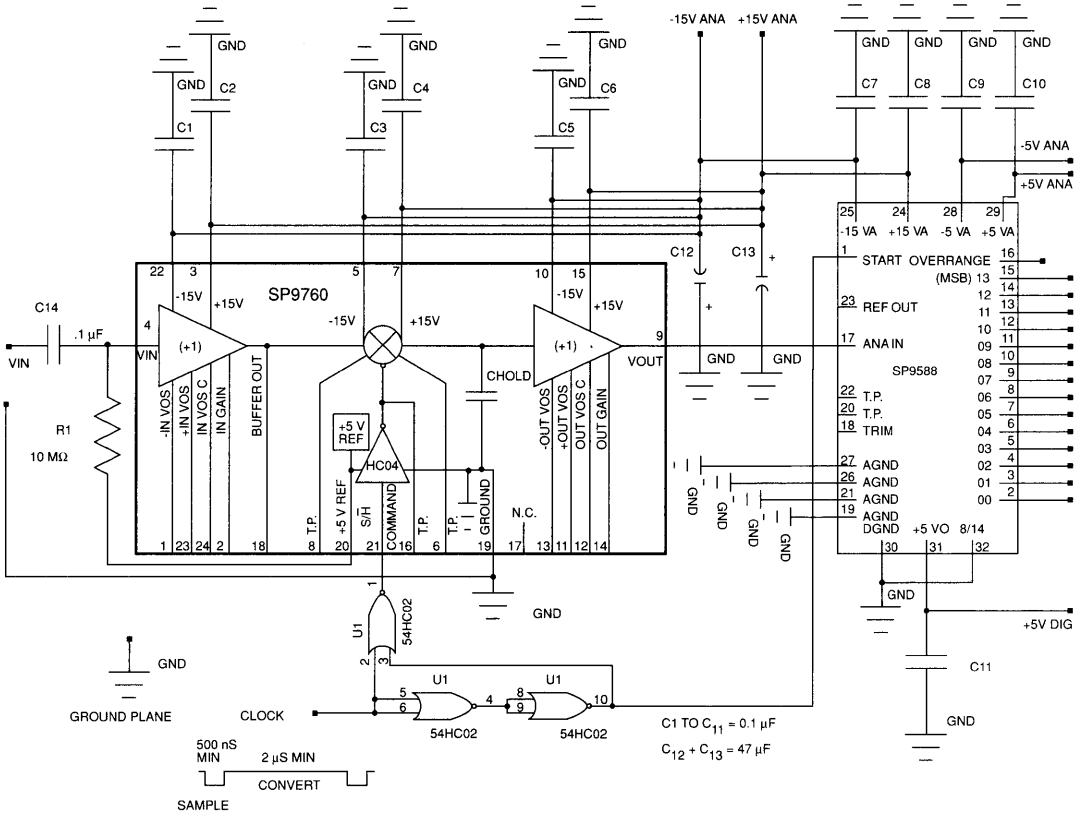


FIGURE 4
-5V TO +5V AC COUPLED BIPOLAR DATA ACQUISITION SYSTEM

The SP9760 and SP9588 can be used in conjunction with a multiplexer for multi-channel data acquisition systems. The configuration seen in figure 5 will handle eight input channels providing a total throughput of 100 kHz per channel.

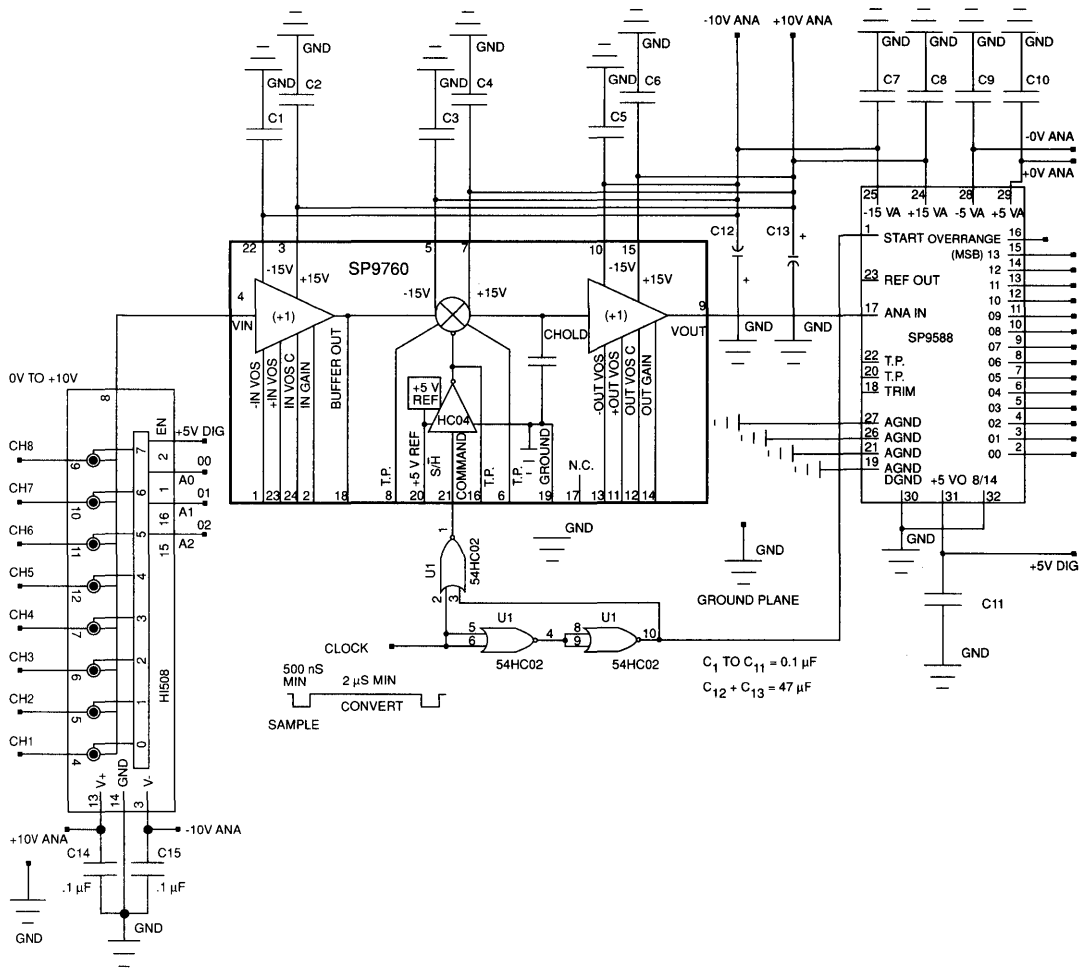


FIGURE 5
0V TO +10V UNIPOLAR DATA ACQUISITION SYSTEM WITH 8 CHANNELS AND 100 KHz THROUGHPUT

The internal buffer amplifier on the SP9760 can be used to implement a multi-order anti-aliasing filter for signal processing applications. (See Figure 6.) The formula for calculating the frequency and Q of the filter are:

$$F_o = \frac{1}{2\pi\sqrt{R_1 R_2 C_{14} C_{15}}}$$

$$\frac{1}{Q} = \sqrt{\frac{R_1 C_{15}}{R_2 C_{14}}} + \sqrt{\frac{R_2 C_{15}}{R_1 C_{15}}}$$

in this case F_o = 100 kHz Q = .5

$R_1 = R_2 = 1k\Omega$ $C_{14} = C_{15}$ = 1600 pF

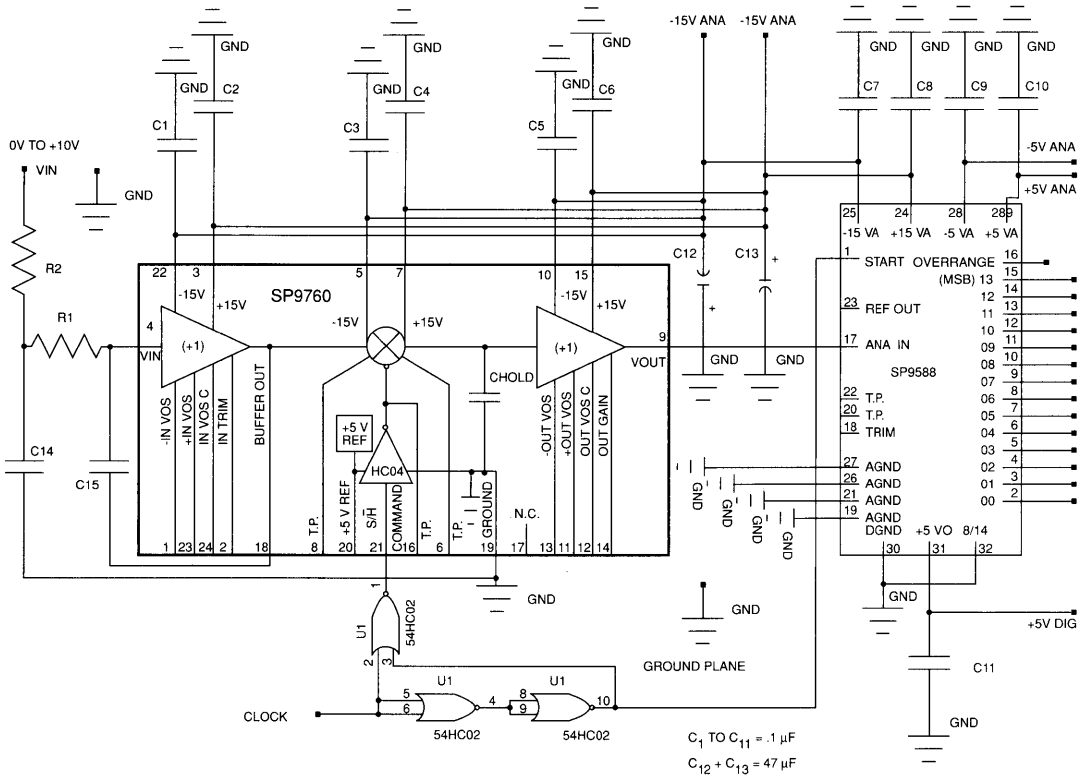


FIGURE 6
0V TO +10V UNIPOLAR DATA ACQUISITION SYSTEM WITH SECOND ORDER ANTI-ALIASING FILTER

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DIGITAL TO ANALOG CONVERTERS

MODEL	RESOLUTION	SETTLING TIME	INPUT LATCHES	INTERNAL REFERENCE	I_{OUT} OR V_{OUT}	POWER CONSUMPTION (mW)	PACKAGE	PAGE
DAC336-8	8 bits	4 µsec	Yes	Yes	V	150	16-Pin SD	225
DAC337	8 bits	5 µsec	No	Yes	V	285	14-Pin SD	231
HS3020	8 bits	3 µsec	Yes	Yes	V	680	18-Pin SD	255
DAC337	10 bits	5 µsec	No	Yes	V	285	16-Pin SD	231
DAC347-10	10 bits	20 µsec	No	Yes	V	225	18-Pin SD	237
DAC87	12 bits	4 µsec	No	Yes	V	450	24-Pin DD	211
DAC87A	12 bits	6 µsec	Yes	Optional	V	360	24-Pin DD	217
DAC331-12	12 bits	3 µsec	No	No	I	30	18-Pin SD	223
DAC336-12	12 bits	5 µsec	Yes	Yes	V	300	24-Pin DD	227
DAC338	12 bits	2.5 µsec	Yes	Yes	V	450	28-Pin DD	233
DAC347-12	12 bits	20 µsec	No	Yes	V	225	18-Pin SD	237
DAC349-12	12 bits	15 µsec	No	Optional	V	300	24-Pin DD	239
DAC356	12 bits	5 µsec	No	Yes	V	75	18-Pin SD	243
HS3120	12 bits	2 µsec	Yes	No	I	40	28-Pin DD	257
HS3860	12 bits	3 µsec	Yes	Optional	V	675	24-Pin DD	269
HS7541A	12 bits	2 µsec	No	No	I	30	18-Pin SD	273
HS7584 QUAD	12 bits	2 µsec	Yes	No	I	20	40-Pin DD	279
HS9338	12 bits	2.5 µsec	Yes	Yes	V	450	28-Pin DD	305
HS9342 QUAD	12 bits	2 µsec	Yes	Optional	V	750	28-Pin DD	309
SP9344 QUAD	12 bits	15 µsec	Yes	No	V	600	28-Pin DD	313
DAC9349-12	12 bits	15 µsec	No	Optional	V	300	24-Pin DD	317
DAC9356	12 bits	25 µsec	No	Yes	V	200	24-Pin DD	319
HS9393/94	12 bits	50/1000 nsec	No	Yes	I/V	495/900	24-Pin DD	351
HS33806	12 bits	2.5 µsec	Yes	No	V	405	28-Pin DD	359
HS3140	14 bits	2 µsec	No	No	I	30	20-Pin SD	261
DAC331-14	14 bits	3 µsec	No	No	I	30	24-Pin DD	223
DAC9331-14	14 bits	3 µsec	No	No	I	30	24-Pin DD	299
SP1148	16 bits	20 µsec	Yes	Yes	V	500	32-Pin TD	251
HS3160	16 bits	2 µsec	No	No	I	30	22-Pin SD	263
SP9316	16 bits	2 µsec	Yes	No	I	60	24-Pin DD	291
DAC9331-16	16 bits	2 µsec	Yes	No	I	60	24-Pin DD	299
HS9371	16 bits	5 µsec	Yes	No	I	45	28-Pin DD	321
HS9372	16 bits	1 µsec	Yes	No	I	50	24-Pin DD	329
DAC9377	16 bits	20 µsec	Yes	Yes	V	450	24-Pin DD	335
HS9378	16 bits	16 µsec	Yes	Yes	V	425	28-Pin DD	339
HS9390	16 bits	75 nsec	Yes	Yes	I	900	32-Pin DD	355
DAC370-18	18 bits	2 µsec	Yes	No	I	60	28-Pin DD	245
DAC377-18	18 bits	20 µsec	Yes	Yes	V	400	28-Pin DD	247
SP9380	18 bits	50 µsec	Yes	Yes	V	600	32-Pin TD	345
DAC349-3D	3 DEC	15 µsec	No	Optional	V	300	24-Pin DD	239
DAC9349-3D	3 DEC	15 µsec	No	Optional	V	300	24-Pin DD	317
DAC9377-4D	4 DEC	20 µsec	Yes	No	V	450	24-Pin DD	335

Shaded area indicates new product since publication of 1988 Catalog

SP DAC87

COMPLETE MONOLITHIC 12-BIT D/A CONVERTER

FEATURES

- Single Chip Construction
- On-Board Output Amplifier
- Low Power Dissipation: 300 mW
- Monotonicity Guaranteed Over Temperature
- Guaranteed for Operation With ±12V Supplies
- Buried Zener Reference
- ±1/2 LSB Max Nonlinearity

PRODUCT DESCRIPTION

The SP DAC87 is a 12-bit digital-to-analog converter with both a high stability voltage reference and output amplifier combined on a single monolithic chip.

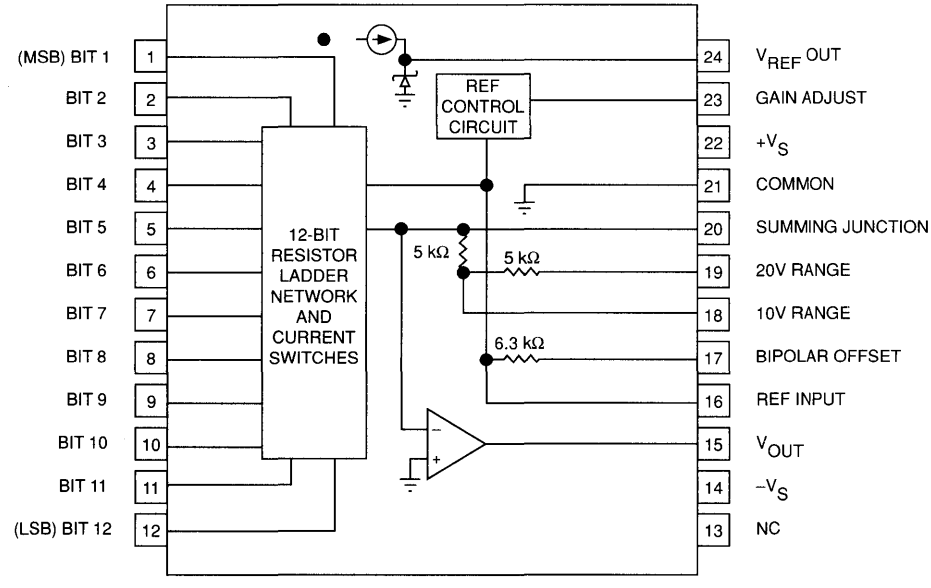
Innovative circuit design reduces the total power consumption to 300 mW which not only improves reliability but also improves long term stability.

The SP DAC87 incorporates a fully differential, non-saturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise, high stability, subsurface Zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete Zener references.

The SP DAC87 is available in a hermetically sealed ceramic package and is specified for -55°C to +125°C temperature operation. MIL-STD-883 processing is available.

7

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to Power Ground ..... 0V to +18V
$-V_S$ to Power Ground ..... 0V to -18V
Digital Input (Pins 1 to 12) to Power Ground ..... -1.0V to +7V
Ref In to Reference Ground ..... ±12V
Bipolar Offset to Reference Ground ..... ±12V
10V Span R to Reference Ground ..... ±12V
20V Span R to Reference Ground ..... ±24V
Ref Out ..... Indefinite Short to Power Ground or $+V_S$

(T_A = +25°C, rated power supplies unless otherwise noted.)

MODEL SP DAC87	MIN	TYP	MAX	UNITS
DIGITAL INPUT				
Binary - CBI			12	Bits
Logic Levels (TTL Compatible)				
V_{IH} (Logic "1")	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)			250	µA
I_{IH} (V_{IL} = 0.8V)			100	µA
TRANSFER CHARACTERISTICS ACCURACY				
Linearity Error @ +25°			±1/2	LSB[1]
T_A @ T_{min} to T_{max}		±1/2	±3/4	LSB
Differential Linearity Error @ +25°C			±3/4	LSB
T_A @ T_{min} to T_{max}			±1	LSB
Gain Error[2]		±0.1	±0.2	%FSR[3]
Offset Error[2]		±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed Monotonicity	-55		+125	°C
DRIFT (T_{min} to T_{max})				
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±30	ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]				
Unipolar		±0.18	±0.3	% of FSR
Bipolar		±0.14	±0.24	% of FSR
Gain				
Including Internal Reference			±20	ppm of FSR/°C
Excluding Internal Reference			±10	ppm of FSR/°C
Unipolar Offset			±3	ppm of FSR/°C
Bipolar Offset			±10	ppm of FSR/°C
CONVERSION SPEED				
Settling Time to ±0.01% of FSR for FSR change (2 kΩ||500 pF load)				
with 10 kΩ Feedback		3	4	µs
with 5 kΩ Feedback		2	3	µs
For LSB Change		1		µs
Slew Rate	10			V/µs

(T_A = +25°C, rated power supplies unless otherwise noted.)

MODEL SP DAC87	MIN	TYP	MAX	UNITS
ANALOG OUTPUT				
Ranges - CBI		±2.5, ±5, ±10 +5, +10		V
Output Current	±5			mA
Output Impedance (dc)		0.05		Ω
Short Circuit Current			40	mA
Internal Reference Voltage (V_R)	+6.23	+6.3	+6.37	V
Output Impedance		1.5		Ω
Max External Current[6]			+2.5	mA
Tempco of Drift			±10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY				
±15V ±10%, 5V supply when applicable			±0.002	% of FSR/% V_S
±12V ±5%			±0.002	% of FSR/% V_S
POWER SUPPLY REQUIREMENTS				
Rated Voltages		±15		V
Range				
Analog Supplies	±11.4[7]		±16.5	V
Logic Supplies	+4.5		+5.5	V
Supply Drain				
+12, +15V		5	10	mA
-12, -15V		14	20	mA
TEMPERATURE RANGE				
Specification	-55		+125	°C
Operating	-55		+125	°C
Storage	-65		+150	°C

NOTES

1. Least Significant Bit.
2. Adjustable to zero with external trim potentiometer.
3. FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V range.
4. Gain and offset errors adjusted to zero at +25°C.
5. C_F = 0, see Figure 1.
6. Maximum with no degradation of specifications, must be a constant load.
7. A minimum of ±12.3V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

DIGITAL INPUT CODES

The SP DAC87 accepts complementary digital input code in binary (CBI) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, COB or CTC.

DIGITAL INPUT		ANALOG OUTPUT		
MSB	LSB	CSB COMPL. STRAIGHT BINARY	COB COMPL. OFFSET BINARY	CTC* COMPL. TWO'S COMPL.
000000000000		+Full Scale	+ Full Scale	-1 LSB
011111111111		+1/2 Full Scale	Zero	-Full Scale
100000000000		Mid-Scale	-1 LSB	+Full Scale
111111111111		Zero	-Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table I. Digital Input Codes

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it cannot be corrected. Linearity error is specified over its entire temperature range. This means that the analog output will not vary by more than its maximum specification, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1 LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2 LSB means that the output voltage step sizes can range from 1/2 LSB to 1 1/2 LSB when the input changes from one adjacent input state to the next.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain drift is established by: 1) testing the end point differences for each SP DAC87 model at the lowest operating temperature, +25°C and the highest operating temperature; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input.

Voltage Output. Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0 1 1 1 . . . 11 to 1 0 0 0 . . . 0 0), the point at which the worst case settling time occurs. The settling time characteristic depends on the compensation capacitor selected, the optimum value is 25 pF as shown in Figure 1.

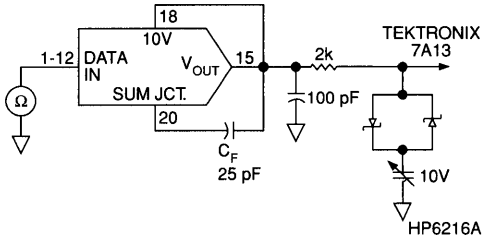


FIGURE 1
SETTLING TIME CIRCUIT

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to ±1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5 mA. An external buffer amplifier is recommended if this reference will result in gain variations. All gain adjustments should be made under constant load conditions.

USING THE SP DAC87

POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams. These capacitors (1 μF electrolytic recommended) should be located close to the SP DAC87. Electrolytic capacitors, if used, should be paralleled with 0.01 μF ceramic capacitors for optimum high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams and adjusted as described below. TCR of the potentiometers should be 100 ppm/°C or less. The 3.9 MΩ and 10 MΩ resistors (20% carbon or better) should be located close to the SP DAC87 to prevent noise pickup. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 2 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01 μF ceramic capacitor should be connected from this pin to common to prevent noise pickup.

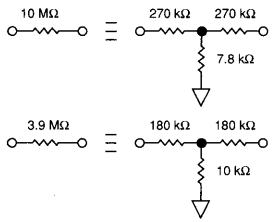


FIGURE 2
EQUIVALENT RESISTANCES

Offset Adjustment. For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is -10V. See Table II for corresponding codes.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages.

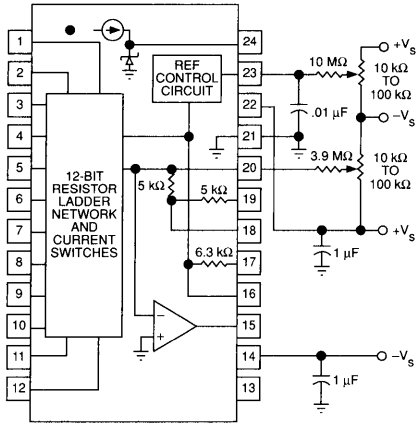


FIGURE 3
EXTERNAL ADJUSTMENT AND VOLTAGE SUPPLY CONNECTION DIAGRAM

DIGITAL INPUT		ANALOG OUTPUT	
12 BIT RESOLUTION		VOLTAGE*	
MSB	LSB	0 to +10V	±10V
000000000000		+9.9976V	+9.9951V
011111111111		+5.0000V	0.0000V
100000000000		+4.9976V	4.88 mV
111111111111		0.0000V	-10.0000V
1 LSB		2.44 mV	-0.0049V

* To obtain values for other binary ranges 0 to +5V range: divide 0 to +10 values by 2; ±5V range: divide ±10V range values by 2; ±2.5V range: divide ±10V range values by 4.

Table II. Digital Input/Analog Output

VOLTAGE RANGES

Internal scaling resistors provided in the SP DAC87 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 4).

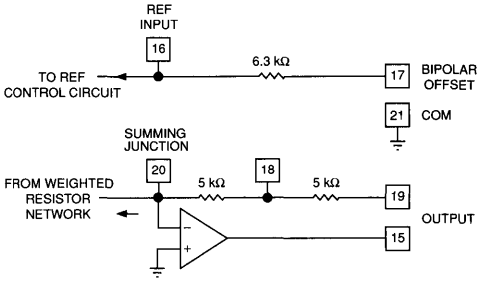


FIGURE 4
OUTPUT AMPLIFIER VOLTAGE RANGE
SCALING CIRCUIT

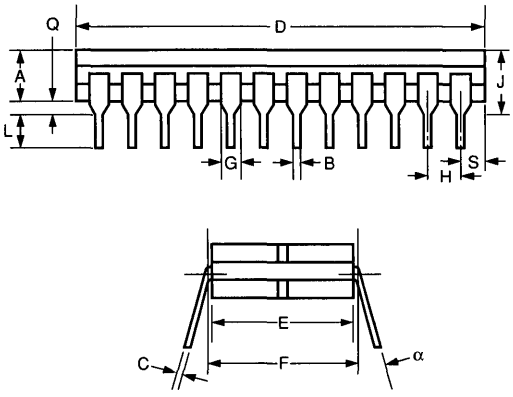
Gain and offset drift are minimized in the SP DAC87 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 4 microseconds for a 10 kΩ feedback resistor; 3 microseconds for a 5 kΩ feedback resistor when using the compensation capacitor shown in Figure 1.

OUTPUT RANGE	DIGITAL INPUT CODES	CONNECT PIN 15 TO	CONNECT PIN 17 TO	CONNECT PIN 19 TO	CONNECT PIN 16 TO
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

Table III. Output Voltage Range Connections

ORDERING INFORMATION

MODEL	LINEARITY ERROR	TEMPERATURE RANGE	SCREENING
SP DAC87-CBI-V/B	±1/2 LSB	-55°C to +125°C	MIL-STD-883C



SYMBOL	INCHES
A	.180
B	.018
C	.012
D	1.27
E	.535
F	.615
G	.070
H	.110
J	.225
L	.150
Q	.045
S	.090
α	15°

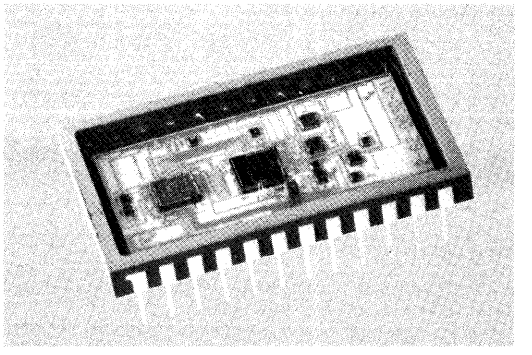
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

NOT RECOMMENDED FOR NEW DESIGNS SEE SP DAC87

COMPLETE 0.006% LINEAR DAC

FEATURES

- True 14-bit (±0.006%) linearity
- Superior replacement for DAC80/85/87, MN3850 and DAC335
- Input register
- Specified over −55°C to +125°C
- Low power: 360mW
- +5V supply not required



DESCRIPTION

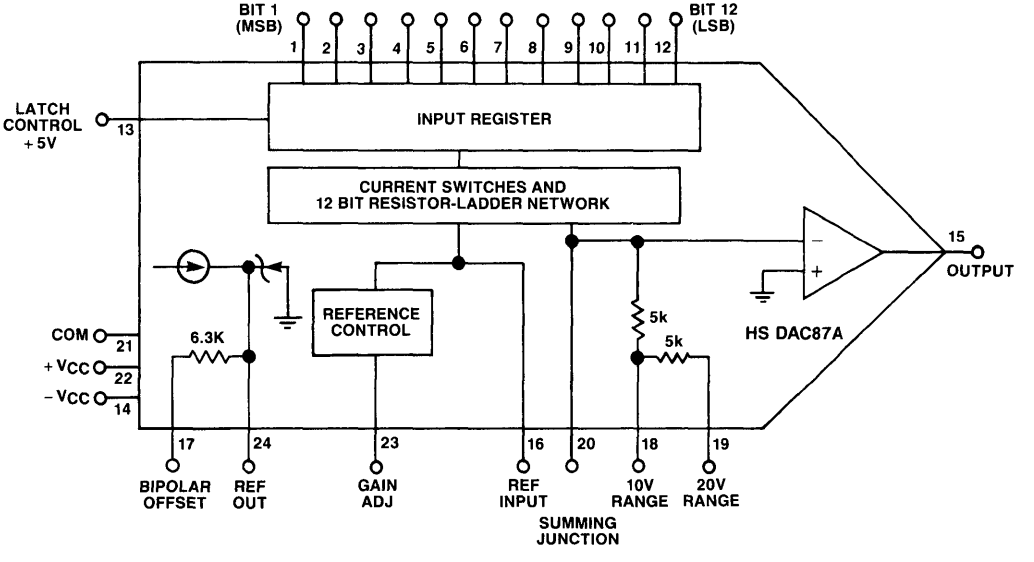
The HSDAC87A series is industry's most accurate complete 12-bit DAC. The DAC87A series is pin compatible with the popular DAC87 but also contains an input storage register. The DAC87A is specified with several linearity grades rated over the full MIL temperature range −55°C to +125°C.

The DAC87A achieves its superior linearity rating resulting from the use of a high precision 18-bit decoded switch set. This high precision switch is a proprietary monolithic CMOS circuit that when used with a low TC thin film network combine to provide the user with an ultra-stable 12-bit DAC.

The DAC87A series is pin compatible with the popular DAC87 DAC. An input register is incorporated within the CMOS switch circuit. The latch control for the input register is connected to pin 13. Pin 13 can be connected to +5V or left open and the HSDAC87A will function as a DAC87. In addition pin 13 can be used to 'latch' data into the input registers, see Figure 3.

7

FUNCTIONAL DIAGRAM



SPECIFICATIONS

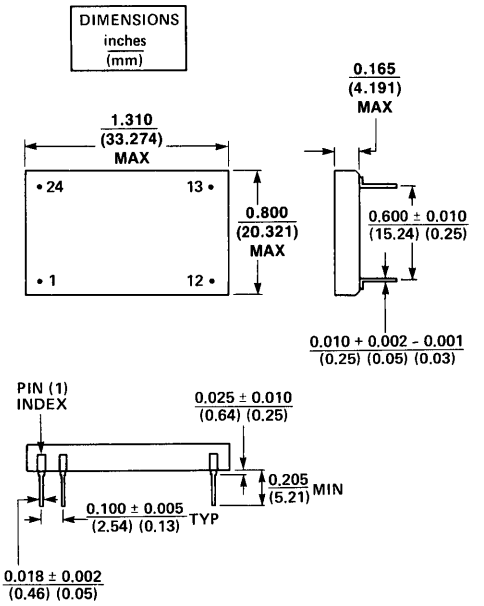
(Typical @ +25°C and nominal power supplies unless otherwise noted)

MODEL	HS DAC87A		
DIGITAL INPUT			
Resolution	12 Bits		
Coding	Complementary Binary/ Complementary Offset Binary		
Data Inputs[1,2]			
Logical "1" (at +1μA)	+2.4V min, $+V_{CC}$ max		
Logical "0" (at −1μA)	−0.5V min, +0.8V max		
Latch Control	TTL Compatible, Level Triggered		
LINEARITY/ACCURACY (Max)[3]			
Model	DAC 87AS	DAC 87AT	DAC 87AU
Integral Linearity[4]			
+25°C	±¾ LSB	±½ LSB	±¼ LSB
−55°C to +125°C	±¾ LSB	±½ LSB	±¼ LSB
Differential Linearity			
+25°C	±¾ LSB	±⅔ LSB	±⅓ LSB
−55°C to +125°C	±1 LSB	±⅔ LSB	±⅓ LSB
Monotonic Range	−55°C to +125°C		
Gain Error (FSR)[5]			
+25°C	0.1%	0.1%	0.07%
−55°C to +125°C	0.25%	0.25%	0.22%
Unipolar Offset			
+25°C	←——— ±0.1% FSR ———→		
−55°C to +125°C	←——— ±0.13% FSR ———→		
Bipolar Offset			
+25°C	←——— ±0.10% FSR ———→		
−55°C to +125°C	←——— ±0.12% FSR ———→		
DRIFT			
Total Bipolar Drift	±15ppm/°C max		
Gain, including REF	±15ppm/°C max		
Offset			
Unipolar	±3ppm/°C		
Bipolar	±10ppm/°C		
CONVERSION SPEED			
Settling Time			
For FSR change with			
10kΩ feedback, 20V swing	10μs max		
5kΩ feedback, 10V swing	6μs typ		
For 1 LSB Change	1.5μs typ, 3μs max		
Slew Rate	10V/μs, 5V/μs min		
ANALOG OUTPUT			
Ranges	±2.5, ±5V, ±10V, 0 to +5V, 0 to +10V		
Current	±5mA min		
Output Impedance	0.05Ω typ		
Short Circuit Duration	Indefinite to Common		
INTERNAL REFERENCE VOLTAGE	6.3V ±5% max		
Drift	±5ppm/°C		
Ext Current	±200μA max		
POWER SUPPLY			
Power Supply Requirements			
Rated Voltage	±15V, ±18V max		
Rated Operation (max)	±12.5V to ±16.5V		
Supply Drain			
+15V Supply	15mA, 25mA max		
−15V Supply	9mA, 20mA max		
Power Supply Sensitivity	±0.001% FSR/%V_S		
Power Consumption	360mW typ, 525W max		
TEMPERATURE RANGE			
Operating	−55°C to +125°C		
Storage	−65°C to +150°C		

NOTES:

1. Data inputs must not be applied without $\pm V_{CC}$ first applied. 2. Unused data inputs must be grounded. 3. Fractions expressed to 2 decimals. 4. For this product, integral linearity is measured as the arithmetic mean value of the magnitudes of the greatest positive and negative deviations from the theoretical value (after gain and offset adjustment) for any given input combination. 5. FSR: Full Scale Range.

PACKAGE OUTLINE



Pin 1 is marked by a dot on the top of the package.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	24	REF OUT (6.3V)
2	BIT 2	23	GAIN ADJUST
3	BIT 3	22	+15V SUPPLY
4	BIT 4	21	GROUND
5	BIT 5	20	SUMMING JUNCTION
6	BIT 6	19	20V RANGE
7	BIT 7	18	10V RANGE
8	BIT 8	17	BIPOLAR OFFSET
9	BIT 9	16	REF INPUT
10	BIT 10	15	V_{OUT}
11	BIT 11	14	−15V SUPPLY
12	BIT 12 (LSB)	13	LATCH CONTROL[1,2]

NOTES:

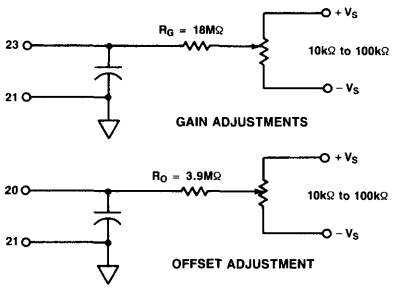
1. When +5V is applied to pin 13 (or left open), as is the case with DAC 87 the input register is transparent; i.e., data enters DAC normally. To use the input register see Figure 3.
2. Latch control is level triggered.

CAUTION: ESD (Electro-Static-Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed.

APPLICATIONS INFORMATION

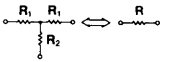
EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed using the circuitry shown in Figure 1. The potentiometers should have a TCR of 100 ppm/°C or less and all resistors should be located as close to the HS DAC87A as possible.



NOTES:

1. Series high value R's can be transformed into a 'T' network:



where: $R_1 = R/X$, $R_2 = R_1 (X-2)$

For the above values this becomes:

1) R_G = 18MΩ, X = 100
   Then, R_1 = 180kΩ and R_2 = 1.84kΩ
2) R_O = 3.9MΩ, X = 10
   Then R_1 = 390kΩ and R_2 = 47kΩ (approx.)

2. For users with other pin compatible DAC87 types, the following chart should be considered:

GAIN RESISTOR R_G	OFFSET RESISTOR R_O	DAC87A ADJUSTMENT RANGE GAIN	OFFSET
10MΩ	3.9MΩ	0.6%	0.2%
18MΩ	3.9MΩ	0.4%	0.2%
18MΩ	1.8MΩ	0.4%	0.4%
33MΩ	3.9MΩ	0.2%	0.2%
45MΩ	30MΩ	0.15%	0.02%

Figure 1. Gain And Offset Connection

ADJUSTMENT PROCEDURE

A voltmeter capable of 1/10 LSB resolution and accuracy is required (244 μV for a 0 to + 10V, 12-bit DAC). The accuracy of the converter subsequent to calibration is directly dependent upon the accuracy of the voltmeter.

The offset adjustment should be made first followed by the gain adjustment.

Offset Adjustment: Connect the voltmeter to the HS DAC87A output (pin 15).
Unipolar operation: Strobe an input code (all 1's) that will result in an output of zero. Adjust the offset until the converter is within ± 1/10 LSB of zero.
Bipolar operation: Strobe an input code that will result in minus full scale (all 1's). Adjust the output to within ± 1/10 LSB's.
Gain Adjustment: Strobe an input code that will result in positive full scale output (all 0's). Adjust gain until the HS DAC87A output reads nominal full scale *minus* 1 LSB to within ± 1/10 LSB.

OUTPUT RANGE	CONNECT PIN 15 TO	CONNECT PIN 17 TO	CONNECT PIN 19 TO	CONNECT PIN 16 TO
± 10V	19	20	15	24
± 5V	18	20	N.C.	24
± 2.5V	18	20	20	24
0 to + 10V	18	21	N.C.	24
0 to + 5V	18	21	20	24

Table 1. Output Range Connections

INPUT LATCH

The HS DAC87A incorporates input buffering and decoding to achieve up to 14-bit linearity (Figure 2). This input buffer's propagation time can introduce a skewing of the digital data reaching the bit switches.

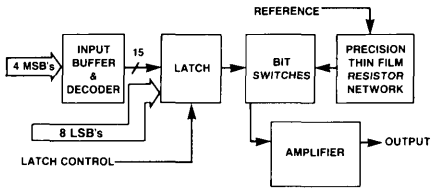
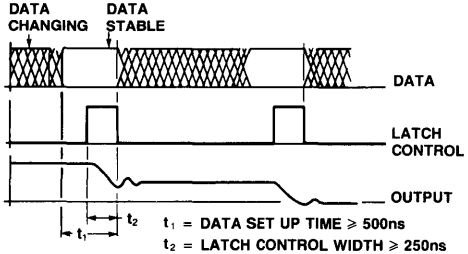


Figure 2. HS DAC87A Block Diagram

The skewing results in the bit switches not operating synchronously with each data change, producing an increase in the settling time (1 to 2 microseconds) and output "glitches." The dynamic performance of the HS DAC87A is greatly improved by using internal latches. The latches are located after the input buffer circuits and just before the bit switches. When strobed the latches present a data change to the bit switches in a synchronous manner. The latches should be closed while the input data is changing and propagating through the buffers. After the digital data has settled the latch is loaded and the "new" data is transferred to the switches synchronously. The latch is then closed and is ready for the next data update. See latch control timing Figure 3.



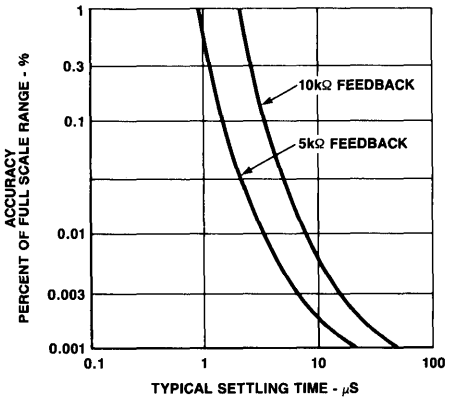
LATCH STROBE INPUT	LATCH CONTROL[1] PIN 13	FUNCTION
0	−0.5V to +0.8V	DATA LATCHED (HELD)
1	+2.4V to +V_{CC}	DATA CHANGING (TRANSFER)

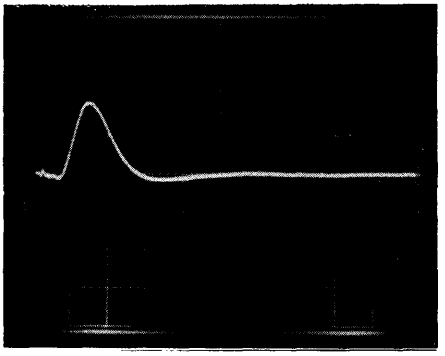
1. TTL Compatible, level triggered.

Figure 3. Latch Control Timing

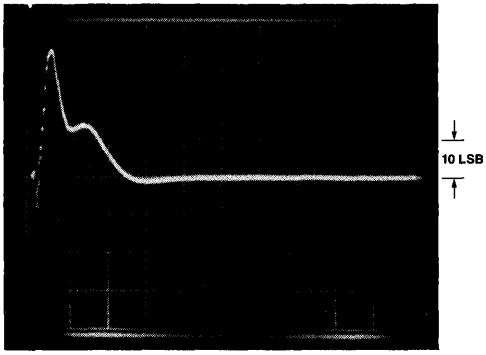
SETTLING TIME

Output Range: ± 10V, 1 LSB = 4.88mV, Code Transition: 011111111111 to 100000000000

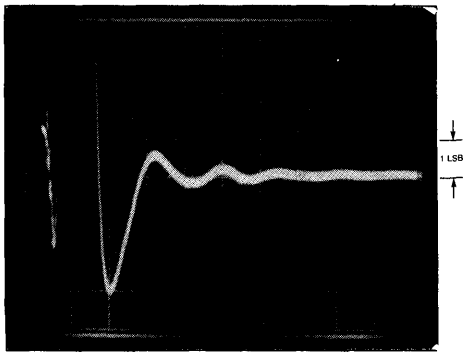




4b. Data *latched.*
Scale: Vertical 10 LSB/DIV, Horizontal 0.5 s/cm.
Note that with latch the "glitch area" is reduced by a factor of 2, as compared to Fig. 4a.



4a. Data *not latched.*
Scale: Vertical 10 LSB/DIV, Horizontal 0.5 s/cm.
See improved performance using latches, Fig. 4b.



4c. Small Scale Settling.
Scale: Vertical 5mV/cm (approx. 1 LSB),
Horizontal 1μs/cm.
4c is basically an expanded version of 4b.

Figure 4. Major Transition Settling Time Measurements

Settling time for each HS DAC87A model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 4).

Three settling times are specified to ± 0.01% of full scale range (FSR); two maximum full scale range changes of 20V, 10V and one for a 1 LSB change. The 1 LSB change is measured at the major carry (0111...11 to 1000...00), *the point at which the worst case settling time occurs.*

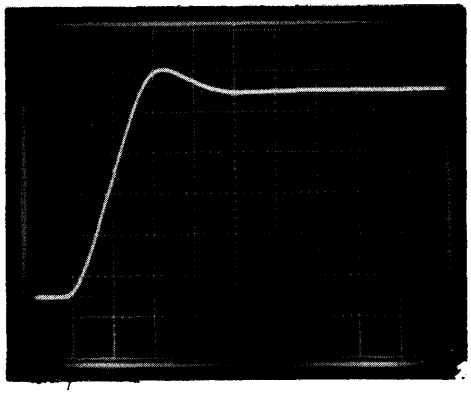


Figure 5. Full Scale Slew Rate (Right)
Output Range: 0 to + 10V
Code Transition: 000000000000 to 111111111111
Data Latched: Yes
Vertical Scale: 2V/cm
Horizontal Scale: 0.5μs/cm.

APPLICATIONS INFORMATION (continued)

POWER SUPPLY CONSIDERATION

Power supplies used for the HS DAC87A should be selected for low noise operation. In particular they should be free of high frequency noise. It is important to remember that 2.44mV is 1 LSB for a 10 volt input.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 1μF tantalum type in parallel with 0.1μF disc ceramic type, see Fig. 6.

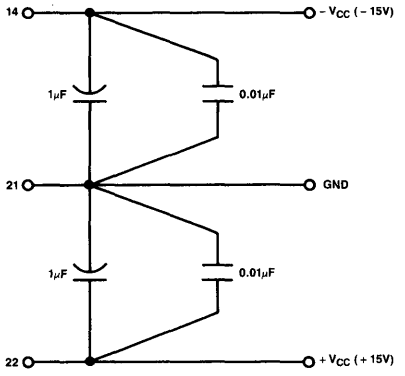
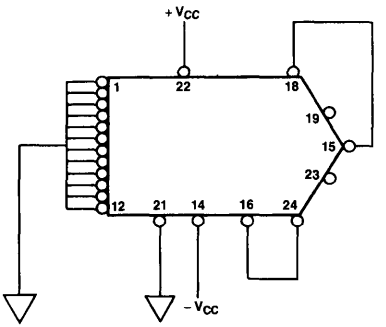


Figure 6. Recommended Power Supply Bypass

POWER BURN-IN

All 'B' HS DAC87A devices are burned in for 168 hours at +125°C in accordance with MIL-STD-883 Method 1015. Those DAC's not designated 'B' are burned-in for 48 hours at +85°C. The burn-in circuit is shown in Figure 7.



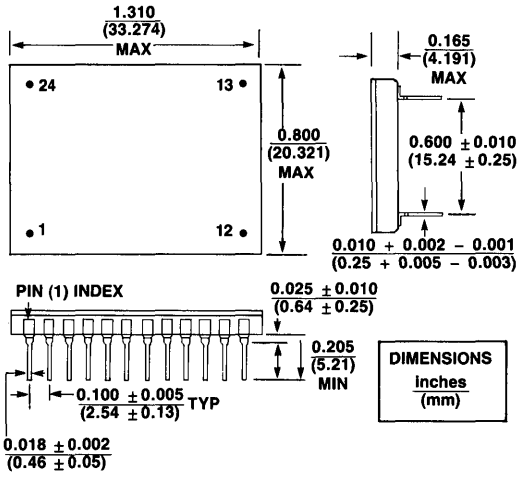
NOTE: Bypass each supply with a 1μF tantalum and a 0.01μF ceramic to Common.

Figure 7. Burn In Circuit

7

TRANSFER CHARACTERISTICS

HS DAC87A DIGITAL INPUT CODE	BIPOLAR OUTPUT VOLTAGE RANGES			UNIPOLAR OUTPUT VOLTAGE RANGES	
LSB MSB	±2.5V	±5V	±10V	0 to +5V	0 to +10V
000000000000	+2.4988V	+4.9976V	+9.9951V	+4.9988V	+9.9976V
011111111111	0.0000V	0.0000V	0.0000V	+2.5V	+5.0000V
10000000000	-0.0012V	-0.0024V	-0.0049V	+2.4988V	+4.9976V
111111111111	-2.5V	-5V	-10.0000V	0.0000V	0.0000V
1 LSB VALUE	1.22mV	2.44mV	4.88mV	1.22mV	2.44mV



ORDERING GUIDE

MODEL	MAXIMUM INTEGRAL LINEARITY ERROR (T_{Min} to T_{Max})	MAXIMUM DIFFERENTIAL LINEARITY ERROR (T_{Min} to T_{Max})	MAXIMUM GAIN ERROR 25°C	MAXIMUM GAIN ERROR (T_{Min} to T_{Max})	SCREENING
DAC87AS/B	± ¾ LSB	± 1 LSB	0.2%	0.25%	883 Rev. C
DAC87AT/B	± ½ LSB	± ⅔ LSB	0.1%	0.25%	883 Rev. C
DAC87AU/B	± ¼ LSB	± ⅓ LSB	0.07%	0.22%	883 Rev. C

Specifications subject to change without notice.

NOTICE: DAC335 USERS

The HS DAC87A is pin compatible with the Hybrid Systems DAC335 except that users must change the gain and offset resistors as indicated in this data sheet.

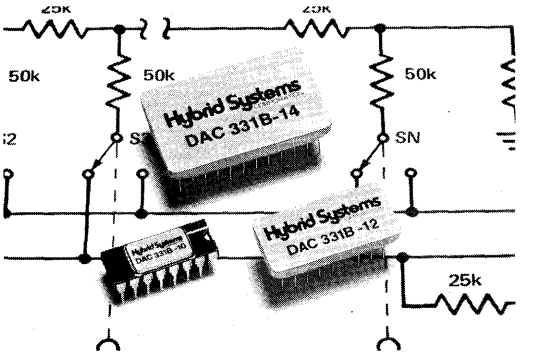
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC331

12 & 14 BIT MULTIPLYING DACs

FEATURES

- Accuracy/resolution to 14-bits
- 2 and 4-quadrant multiplication
- −55°C to +125°C operation
- Ladders and feedback resistors trimmed to ±5% absolute
- Low power
- Single power supply



DESCRIPTION

The DAC331 Series includes 12 and 14-bit multiplying digital-to-analog (DAC) converters. Linearity error of ±½ LSB maximum is standard for all models. All models are capable of both 2-quadrant (unipolar) and 4-quadrant (bipolar) multiplication and 2-quadrant division. Models are available in commercial/industrial grade ("C" versions) for 0 to +70°C operation. "B" versions are processed to the requirements of MIL-STD-883 Rev. C, Level B and are specified for use over a wide, −55°C to +125°C, temperature range.

Ultra-stable R/2R thin-film resistor ladder networks are trimmed to 25K/50KΩ absolute. Each DAC331 includes a 25KΩ feedback resistor (for use with external op amp) that closely tracks the R/2R ladder. Linearity tempco is a low ±2 ppm/°C FSR. Gain tempcos are for 12-and 14-bit models.

Each DAC331 Series converter operates from a single, +5V power supply. Power consumed is less than 30 mW. All models are TTL/DTL and CMOS compatible.

Uses for DAC331 Series converters include digital attenuation of AC and DC voltages, digital gain control, and stroke generators for CRT graphics displays. DAC331's low power is well suited to battery powered equipment applications.

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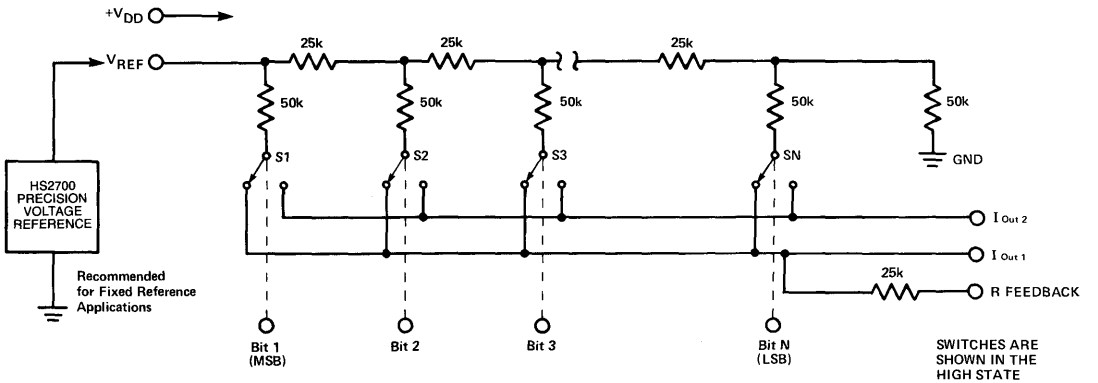
FUNCTIONAL DIAGRAM



SPECIFICATIONS

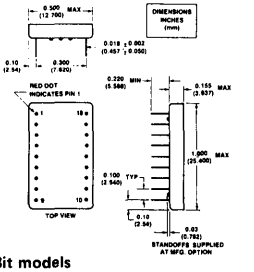
(Typical @ +25°C unless otherwise noted; Using V_{DD} nominal power supply, V_{REF} = +10V)

SERIES	DAC331
TYPE	Multiplying, Current Output
DIGITAL INPUT	
Resolution:	
-12 models	12 Bits
-14 models	14 Bits
2-Quad. Unipolar Coding	Binary
4-Quad. Bipolar Coding	Offset Binary
Logic Compatibility	DTL, TTL, 5V CMOS
Logic Thresholds[1]	V_{IH}=3.0V (min), V_{IL}=1.0V (max)
Input Leakage Current	±1μA (max) @ 0V≤V_{IN}≤V_{DD}
REFERENCE INPUT	
Voltage Range	±25V (max)
Input Impedance	25KΩ ± 1% (nom)[2]
ANALOG OUTPUT	
Gain Accuracy[3]	40μA/V ± 0.1% F.S.R.,typ; ±1.0% F.S.R., max
Offset[4]	50μV (max)
Small Signal 3 dB Bandwidth	600 kHz (min)
Output Capacitance	
C_{out_1}	100pF (max) all inputs high
C_{out_2}	65pF (max) all inputs high
C_{out_1}	65pF (max) all inputs low
C_{out_2}	100pF (max) all inputs low
STATIC PERFORMANCE	
Integral Linearity (all models)	±½ LSB (max)
Differential Linearity (all models)	±½LSB, typ; ±1LSB, max
DYNAMIC PERFORMANCE	
Major Code Transition Settling to ± 0.05% 12 and 14 Bit models	3.0μS (max)
Reference Feedthrough Error (V_{REF} = 20Vpp @ 10 kHz)	10mVpp
STABILITY[4] (Over Specified Temp. Range)	
Scale Factor[5] 12 and 14 Bit models	±3ppm/°C F.S.R. (max)
Linearity (all models)	±3ppm/°C F.S.R. (max)
Differential Linearity (all models)	±2ppm/°C F.S.R. (max)
POWER SUPPLY (V_{DD})[6]	
Voltage Range @ Current	+5V (nom); +4.75V to +10V @ < 1mA
Rejection Ratio	0.005%/% (max)
Total Dissipation (inputs at GND)	30mW (max)
TEMPERATURE RANGE	
Specified:	
-C Versions	0°C to +70°C
-B Versions	-55°C to +125°C
Operating (all models)	-55°C to +125°C
Storage (all models)	-65°C to +150°C
MECHANICAL	
Case Style	metal

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. Power supply should come up before, or at the same time, as the digital input supply.

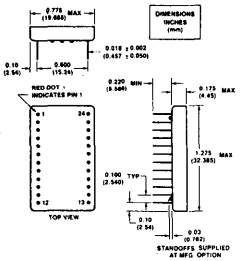
18- & 24-Pin Case Envelope Dimensions

12-Bit models



PIN	FUNCTION	PIN	FUNCTION
1	I OUT 1	18	R FEEDBACK
2	I OUT 2	17	V REF
3	GND	16	+V_{DD}
4	Bit 1 (MSB)	15	Bit 12 (LSB)
5	Bit 2	14	Bit 11
6	Bit 3	13	Bit 10
7	Bit 4	12	Bit 9
8	Bit 5	11	Bit 8
9	Bit 6	10	Bit 7

14-Bit models



PIN	FUNCTION	PIN	FUNCTION
1	R FEEDBACK	24	V_{REF}
2	I OUT 2	23	+V_{DD}
3	I OUT 1	22	BIT 5
4	N.C.	21	BIT 6
5	BIT 1 (MSB)	20	BIT 7
6	BIT 2	19	BIT 8
7	BIT 3	18	BIT 9
8	BIT 4	17	BIT 10
9	N.C.	16	BIT 11
10	N.C.	15	BIT 12
11	N.C.	14	BIT 13
12	GROUND	13	BIT 14 (LSB)

Note: N.C. means no connection

NOTES:

1. The switching threshold is typically $V_{DD}/2$.
2. 10K Ω input impedance available. Consult factory.
3. Using internal feedback resistor.
4. Using the internal $R_{feedback}$ with nulled external amplifier in a constant 25°C ambient. (Offset doubles every 10°C).
5. The DAC331 Series is designed to be used only in those applications where the current output is virtual ground; i.e., the summing junction of an op amp in the inverting mode. The internal feedback resistor (R Feedback) must be used to achieve temperature tracking.
6. The power supply voltage must not exceed + 10V.
7. In case of discrepancy between package shown in photograph and package outline dimension, the mechanical outline is correct.

ORDERING INFORMATION

MODEL NUMBER	DESCRIPTION
DAC331C-12-1	Comm, 12-Bit, +5V Operation
DAC331B-12-1	Mil, 12-Bit, +5V Operation
DAC331C-14-1	Comm, 14-Bit, +5V Operation
DAC331B-14-1	Mil, 14-Bit, +5V Operation

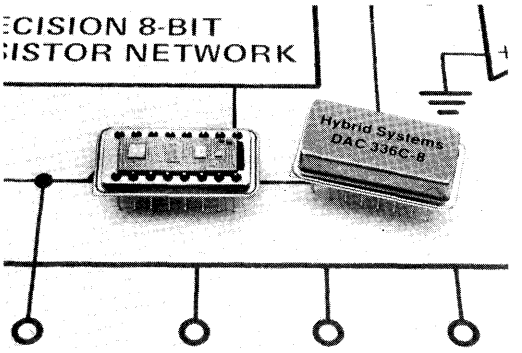
"C" models are commercially processed.
"B" models are processed to MIL-STD-883 Rev. C, Level B.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC336-8
8-Bit Storage Register DACs

FEATURES

- **Input Storage Register**
- **Compact and Complete**
  Contains reference, ladder network, switches output amplifier, and input storage register in a 16-pin package
- **Adjustment-Free**
- **Accurate to ±1/8 LSB (typ)**
- **Very Low Power . . . 150mW (typ)**
- **-55° C To +125° C Operation**



DESCRIPTION

The DAC336-8 includes a precision voltage reference, resistor ladder network, switches, output amplifier, and the input storage register. The reduced need for external circuitry lowers cost and improves reliability in microcomputer based process control and other applications.

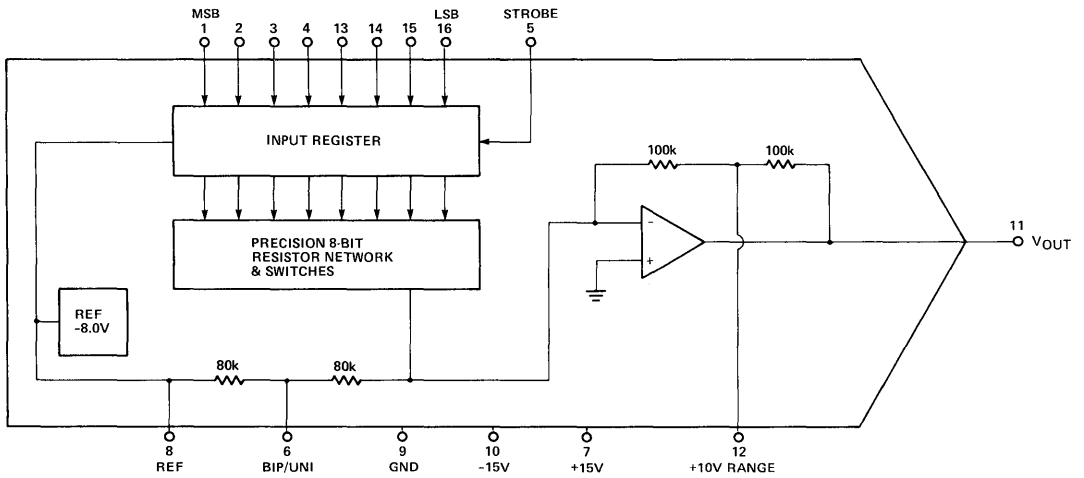
There is no need to add external adjustment potentiometers or expensive capacitors to the DAC336-8. It is factory pre-trimmed to ±0.05%...four times the accuracy normally associated with 8-Bit DACs. And simple pin jumpering allows a choice of four voltage range outputs: 0 to +10V, 0 to −10V, ±5V, ±10V.

The STROBE input (Pin 5) controls the data flow to the DAC336-8 latches (storage register). When the STROBE is low, data in the register is held. When the STROBE is high, the input register is "transparent" and the analog output follows the digital input.

The heart of the DAC336-8 is a laser-trimmed low drift thin-film nichrome resistor network. Low power consumption, typically 150 mW, is featured in the design. DAC336-8 will accept TTL, DTL, and 5V CMOS logic levels and will deliver a minimum of 5 mA @ ± 10V output.

The features, accuracy, simplicity, and quality built into DAC336-8 are a result of Hybrid Systems' many years of experience in the converter field. Two DAC336-8 models are available: DAC336C-8 for commercial/industrial uses; DAC336B-8 where MIL-STD-883 Rev. C, Level B processing is required.

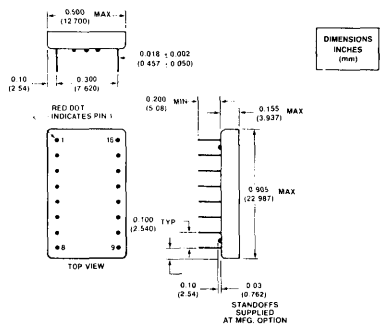
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C and nominal supplies unless otherwise noted)

MODEL	DAC336-8
TYPE	Latched, Fixed Reference, Voltage Output
RESOLUTION	8 Bits
DIGITAL INPUTS	
Logic Compatibility[1]	TTL/DTL, CMOS
Input Current	1 μA (max)
Input Codes	
Unipolar Positive	Complementary Binary
Unipolar Negative	Binary
Bipolar	Complementary Offset Binary
Strobe Width[2]	140nS (min)
Data Set Up Time[3]	50nS (min)
ANALOG OUTPUT	
Scale Factor (Gain)[4]	±0.05% FSR, ±0.2% FSR (max)
Initial Offset[4]	±0.05% FSR, ±0.2% FSR (max)
Output Ranges[5]	
Unipolar	0 to -10V, 0 to +10V
Bipolar	±5V, ±10V
Output Current Capability	5mA (min)
Output Impedance	⩽1Ω
REFERENCE[6]	Internal -8.0 VDC
STATIC PERFORMANCE	
Integral Linearity	± ⅛LSB (typ), ± ½LSB (max)
Differential Linearity	±½LSB typ; ±1 LSB (max)
DYNAMIC PERFORMANCE	
Settling Time to 0.2% FSR[7]	
For a 1 LSB Change	4μS (max)
Slew Rate	0.5V/μS
STABILITY	
Differential Linearity	
0°C to +70°C	±15 ppm of FSR/°C, ±25 ppm of FSR/°C (max)
-55°C to +125°C	±15 ppm of FSR/°C
Scale Factor (Gain)	
0°C to +70°C	±20 ppm of FSR/°C, ±30 ppm of FSR/°C (max)
-55°C to +125°C	±20 ppm of FSR/°C
Offset	
0°C to +70°C	±20 ppm of FSR/°C, ±30 ppm of FSR/°C (max)
-55°C to +125°C	±20 ppm of FSR/°C
Total Transfer Accuracy[8]	
0°C to +70°C	±30 ppm of FSR/°C, ±50 ppm of FSR/°C (max)
-55°C to +125°C	±50 ppm of FSR/°C
POWER SUPPLY[9]	
Requirements	
+15V	+11.0V to +18.0V @ 3.5mA, 6mA (max)
-15V	-11.0V to -18.0V @ 6.5mA, 12mA (max)
Rejection Ratio	
+15V	0.005% FSR/%Vs (max)
-15V	0.005% FSR/%Vs (max)
TEMPERATURE RANGE	
Operating	-55°C to +125°C B Version
Storage	0°C to +70°C C Version
MECHANICAL	
Case Style	Metal



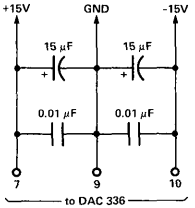
Pin Assignments

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	BIT 1 (MSB)	16	BIT 8 (LSB)
2	BIT 2	15	BIT 7
3	BIT 3	14	BIT 6
4	BIT 4	13	BIT 5
5	STROBE	12	+10V RANGE
6	BIPOLAR OFFSET	11	OUTPUT
7	+15V	10	-15V
8	REF OUT	9	GND

NOTES:
1. 5V CMOS, 2.5V (nom.) threshold.
   Logic 1 > 3.5V (min).
   Logic 0 < 0.8V (max).
2. Strobe input load is 2 CMOS inputs.
3. Time data must be stable before Strobe goes to "0".
4. Initially pre-trimmed, no adjustment necessary.
5. User pin programmable, see Gain Scaling Table.
6. User accessible, 5 mA (min).
7. Worst case for 20V range is 45 μ s, and 25 μ s for 10V range.
8. Includes gain, zero, and linearity errors.
9. Supply voltages must be at least 2.5V above maximum output voltage.
10. In case of discrepancy between package shown in photograph and package outline dimension, the mechanical outline is correct.

APPLICATIONS INFORMATION

RECOMMENDED POWER SUPPLY BYPASS CIRCUIT



STROBE LOGIC

STROBE	FUNCTION
0	data latched (held)
1	data changing (transfer)

TRANSFER CHARACTERISTICS

Digital Input Code	Analog Output			
	Unipolar		Bipolar	
	+10V	-10V	±10V	±5V
0 0 0 0 0 0 0 0	+9.961	0.000	+10.000	+5.000
0 0 0 0 0 0 0 1	+9.922	-0.039	+9.922	+4.961
0 1 1 1 1 1 1 1	+5.000	-4.961	+0.078	+0.039
1 0 0 0 0 0 0 0	+4.961	-5.000	0.000	0.000
1 1 1 1 1 1 1 0	+0.039	-9.922	-9.843	-4.922
1 1 1 1 1 1 1 1	0.000	-9.961	-9.921	4.961

GAIN SCALING TABLE

OUTPUT VOLTAGE RANGE	CONNECT PIN 6 TO	CONNECT PIN 11 TO	CODING
0 to + 10V	8	12	Comp. Bin
0 to - 10V	Gnd	12	Bin
±5V	NC	12	Comp. Off. Bin.
±10V	NC	NC	Comp. Off. Bin.
Note: NC means no connection			

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below – 0.5 volts. Power supply should come up before, or at the same time, as the digital input supply.

ORDERING INFORMATION

MODEL	APPLICATION
DAC336C-8	Commercial/Industrial
DAC336B-8	Per Mil-STD-883 Rev. C, Level B

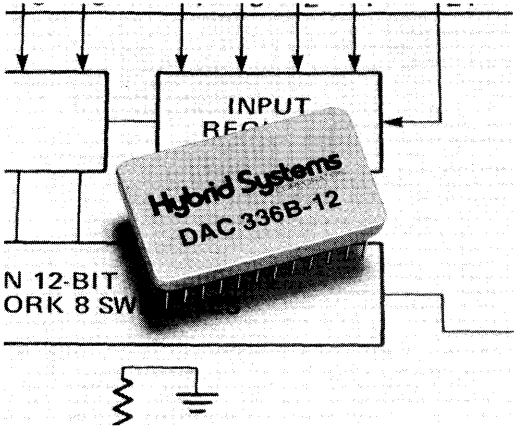
Specifications subject to change without notice.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC336-12
12-Bit Storage Register DACs

FEATURES

- **Input Storage Register**
- **Compact and Complete**
  Contains reference, ladder network, switches, output amplifier, and input storage register in a 24 pin DIP style package.
- **Very Low Power . . . 300mW typical**
- **Operates -55°C to +125°C**
- **MIL or Comm./Indust. Processing**



DESCRIPTION

DAC336-12 models are easy to use because they're so complete. They're ideal for microprocessor applications. Each DAC336-12 operates reference, ladder network, switches, output amplifier and input register on just 300 mW, typical; and all in a 24 pin package.

DAC336-12's input register is both 8-Bit bus and 12-Bit bus compatible. Strobe input pins 23 and 24 can be operated independently to enter 8 bits and 4 bits of data respectively or both pins can be operated simultaneously when operating from 12 bit or larger data bus. Data is held in the register when the Strobe inputs are low. When Strobe inputs are high, the input register is "transparent" and the analog output follows the digital inputs.

At the heart of the DAC336-12 is a laser-trimmed, low drift, thin-film nichrome network. The units accept TTL/DTL and 5V CMOS logic levels and deliver a minimum of 5 mA at ± 10V out. Simple pin jumpering allows the user output choices of either ± 10V or 0 to + 10V.

Two DAC336-12 models are available: DAC336C-12 for commercial/industrial uses; DAC336B-12 where MIL-STD-883 Rev. C, Level B processing is required.

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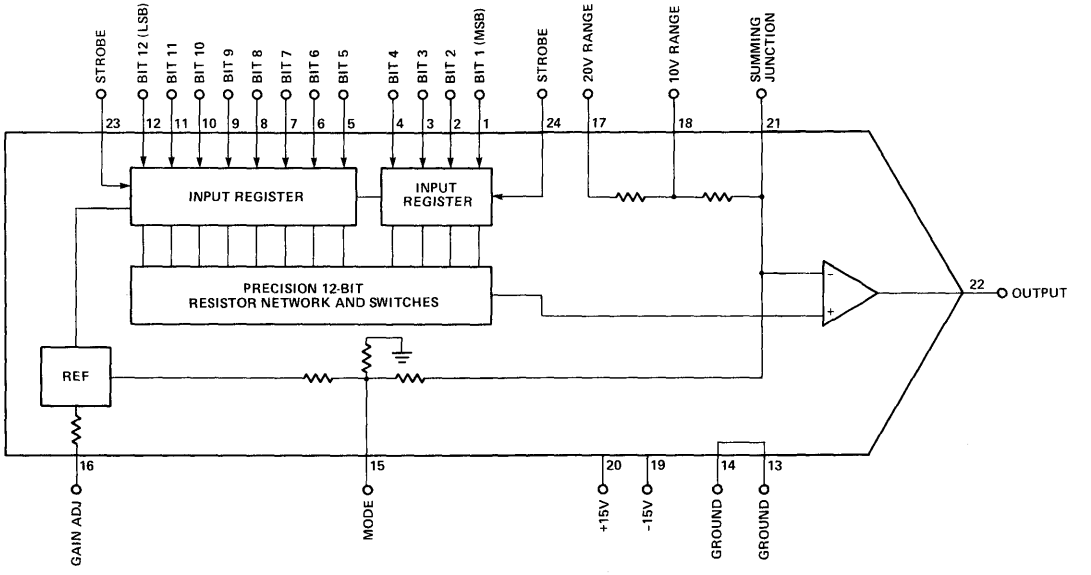
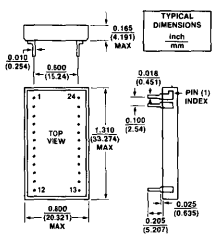
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C and nominal power supply voltages unless otherwise noted)

SERIES	DAC336-12
TYPE	Latched, Fixed Ref., Volt. Output
RESOLUTION	12 Bits
DIGITAL INPUTS	
Logic Compatibility[1]	TTL, DTL, CMOS
Input Current	1 μA (max)
Coding	
Unipolar	Binary
Bipolar	Offset Binary
Strobe Width[2]	140nS (min)
Data Set Up Time[3]	50nS (min)
ANALOG OUTPUT	
Scale Factor[4]	±0.2% F.S.R. (max)
Initial Offset[4]	±0.2% F.S.R. (max)
Output Ranges[5]	0 to +10V, ±10V
Output Current Capability	5mA (min)
Output Impedance	0.2Ω
REFERENCE	Internal
STATIC PERFORMANCE	
Integral Linearity (best straight line)	±0.03% F.S.R. (max)
Differential Linearity	±1 LSB (max)
DYNAMIC PERFORMANCE	
Maximum Settling Time	
10V Change	5μS
20V Change	10μS
Slew Rate	10V/μS
STABILITY	
Differential Linearity	
0 to +70°C	±2ppm/°C of F.S.R. (max)
-55°C to +125°C	±5ppm/°C of F.S.R. (max)
Scale Factor (Gain)	
0 to +70°C	±20ppm/°C of F.S.R. (max)
-55°C to +125°C	±30ppm/°C of F.S.R. (max)
Offset	
0 to +70°C	±20ppm/°C of F.S.R. (max)
-55°C to +125°C	±30ppm/°C of F.S.R. (max)
Total Transfer Accuracy[6]	
0 to +70°C	30ppm/°C
-55°C to +125°C	40ppm/°C
POWER SUPPLY[7]	
Requirements	
+15V	+11.0V to +18.0V @ 10mA (max)
-15V	-11.0V to -18.0V @ 25mA (max)
Rejection Ratio	0.001%/%V_S
TEMPERATURE RANGE	
Operating	-55°C to +125°C B version
Storage	0°C to +70°C C version
MECHANICAL	
Case Style	24-pin ceramic



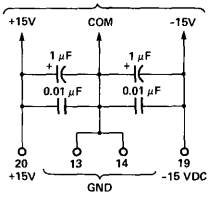
Pin 1 is marked by a dot on the top of the package.

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	24	STROBE BIT 1-4
2	BIT 2	23	STROBE BIT 5-12
3	BIT 3	22	OUTPUT
4	BIT 4	21	SUMMING JUNCTION
5	BIT 5	20	+ 15 V
6	BIT 6	19	- 15 V
7	BIT 7	18	10 V RANGE
8	BIT 8	17	20 V RANGE
9	BIT 9	16	GAIN ADJUST
10	BIT 10	15	MODE
11	BIT 11	14	GROUND
12	BIT 12(LSB)	13	GROUND

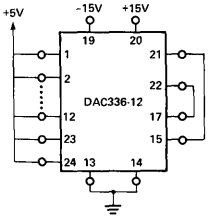
NOTES:
1. 5V CMOS, 2.5V (nom.) threshold. Logic 1 > 3.5V (min), Logic 0 < 0.8V (max).
2. Strobe input load is 2 CMOS inputs.
3. Time data must be stable before Strobe goes to "0".
4. Adjustable to zero...see APPLICATIONS INFORMATION.
5. Pin programmable...see APPLICATIONS INFORMATION.
6. Includes gain, zero, and linearity errors.
7. Supply voltages must be at least 3.5V above maximum output voltage.
8. In case of discrepancy between package shown in photograph and package outline dimension, the mechanical outline is correct.

APPLICATIONS INFORMATION

RECOMMENDED POWER SUPPLY BYPASS CIRCUIT



RECOMMENDED BURN-IN CIRCUIT
(Standard for MIL-STD-883 Models)



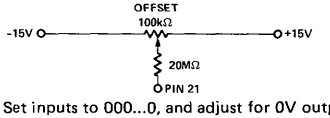
GAIN SCALING

Output Voltage Range	Connect Pin 15 to	Connect Pin 22 to
0 to +10V	Gnd	18
±10V	21	17

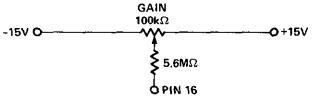
STROBE LOGIC

Strobe	Function
0	data latched (held)
1	data changing (transfer)

OPTIONAL ADJUSTMENTS*



Unipolar - Set inputs to 000...0, and adjust for 0V output.
Bipolar - Set inputs to 000...0, and adjust for -10V output.



Unipolar - Set inputs to 111...1, and adjust for +10V output.
Bipolar - Same as above.

*Allow for swing of ±0.5% minimum.

TRANSFER CHARACTERISTICS

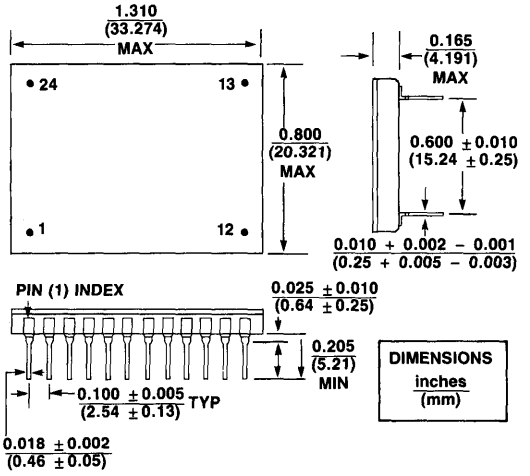
DIGITAL	UNIPOLAR		BIPOLAR	
INPUT CODE	OUTPUT WEIGHTING	OUTPUT VOLTAGE	OUTPUT WEIGHTING	OUTPUT VOLTAGE
1 1 1 . . . 1	(F.S. -1 LSB)	+9.9975V	(F.S. -1 LSB)	+9.995V
1 0 0 . . . 0	F.S./2	+5.000V	ZERO	0 Volts
0 0 0 . . . 0	ZERO	0 Volts	-F.S.	-10.000V

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. Power supply should come up before, or at the same time, as the digital input supply.

ORDERING INFORMATION

MODEL	PROCESSING
DAC336C-12	Commercial/Industrial
DAC336B-12	Per MIL-STD-883 Rev. C, Level B

Specifications subject to change without notice.


1.310
(33.274)
MAX
0.165
(4.191)
MAX
• 24
13 •
0.800
(20.321)
MAX
0.600 ±0.010
(15.24 ±0.25)
• 1
12 •
0.010 + 0.002 − 0.001
(0.25 + 0.005 − 0.003)
PIN (1) INDEX
0.025 ±0.010
(0.64 ±0.25)
0.205
(5.21)
MIN
0.100 ±0.005
(2.54 ±0.13) TYP
0.018 ±0.002
(0.46 ±0.05)
DIMENSIONS
inches
(mm)

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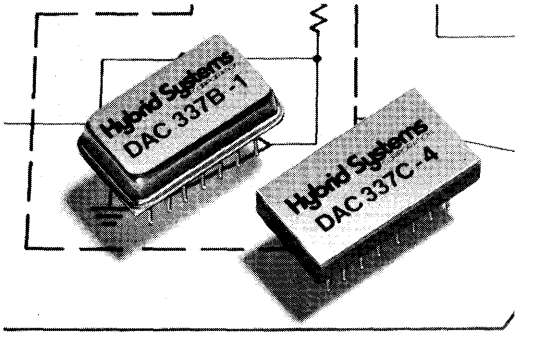
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC337
Adjustment-Free, 8 & 10-Bit DACs

FEATURES

- **8 and 10 Bit Versions**
- **No Zero Or Gain Adjusts**
- **±½LSB Linearity**
- **Internal Reference and Output Amplifier**
- **MIL-STD-883 or Comm./Indust. Processing**
- **Low Power**



DESCRIPTION

The DAC337 Series digital-to-analog converters are designed for completely adjustment-free operation.

The word "simplicity" best characterizes the DAC337 Series. All models are housed in hermetically-sealed DIP style packages and operate on ±15V power supplies. Each model incorporates a precision reference, highly stable thin-film nichrome resistor network, output amplifier, and switches. ±½ LSB linearity is achieved without the use of external zero and gain adjustment circuits.

Both the 8- and 10-Bit versions are offered with the choice of four output voltage ranges: 0 to +10, 0 to −10 (*unipolar*) and ±5, ±10 (bipolar).

Hybrid Systems offers two grades of processing: commercial/industrial (Option C) and MIL-STD-883 Rev. C, Level B (Option B).

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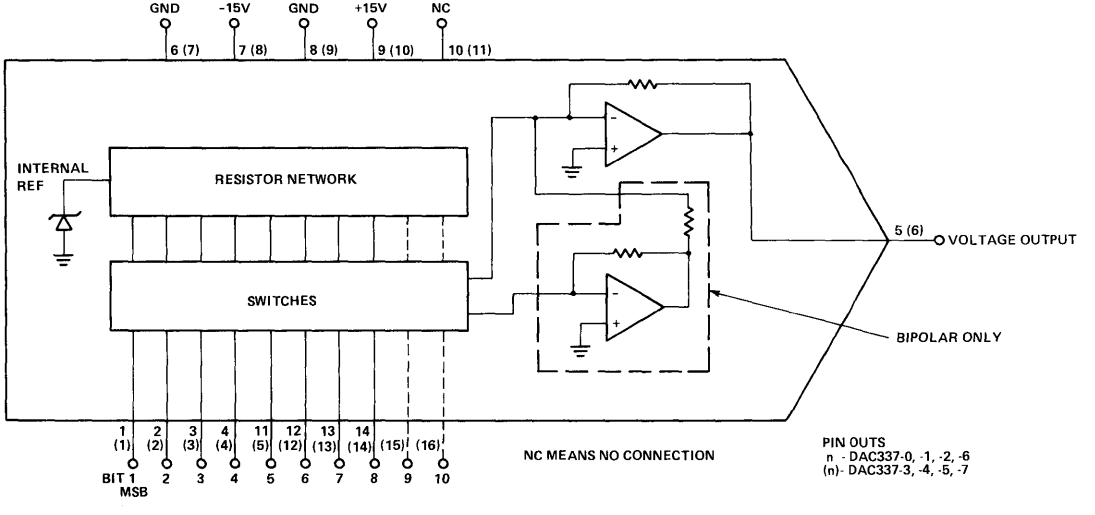
FUNCTIONAL DIAGRAM

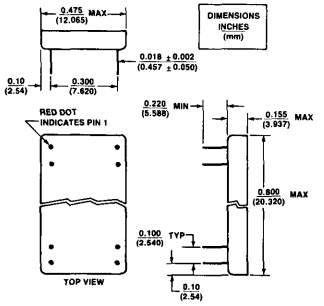


SPECIFICATIONS

(Typical for all models @ +25°C and nominal power supplies unless otherwise noted)

SERIES	DAC337
TYPE	Fixed Ref., Volt, Output
DIGITAL INPUT	
Resolution	
DAC337-0, -1, -2, -6	8 Bits
DAC337-3, -4, -5, -7	10 Bits
Coding	
DAC337-0, -3	Complementary Binary
DAC337-1, -4, -6, -7	Offset Binary
DAC337-2, -5	Binary
Logic Compatibility	TTL, DTL, CMOS (from 5.0V Supply) V_{IH}=2.4V (typ), 3.5V (min) V_{IL}=0.8V (max)
ANALOG OUTPUT	
Voltage	
DAC337-0, -3	0 to -10V @ -5mA
DAC337-1, -4	±5V @ ±5mA
DAC337-2, -5	0 to +10V @ +5mA
DAC337-6, -7	±10V @ ±5mA
Impedance	≤0.1Ω
REFERENCE	Internal
STATIC PERFORMANCE	
Integral Linearity	±½ LSB, max
Differential Linearity	±½ LSB, typ; ±1 LSB, max
DYNAMIC PERFORMANCE	
Settling Time to ½ lsb for F.S.R. Change	
DAC337-0, -1, -2, -3, -4, -5	20μS
DAC337-6, -7	40μS
For 1 lsb change	5μS, typ; 10μS, max
Slew Rate	0.5V/μS
STABILITY (T_{MIN} to T_{MAX})	
Accuracy	
DAC337-0, -1, -2, -6	1 LSB
DAC337-3, -4, -5, -7	4 LSB
Linearity	±½ LSB, max
Offset	±1 LSB, max
POWER SUPPLY	
Voltage @ Current	+15V ± 20% @ +6mA, max -15V ± 20% @ -13mA, max
Power Supply Rejection Ratio	+15V Supply, 0.1% F.S.R./Volt -15V Supply, 0.2% F.S.R./Volt
TEMPERATURE RANGE	
Operating	
"C" models	0 to +70°C
"B" models	-55°C to +125°C
Storage	-65°C to +150°C
MECHANICAL	
Case Style	Metal or ceramic at manufacturer's option.
Case Envelope Dimensions	

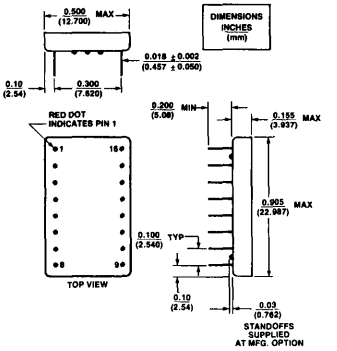
DAC337-0, -1, -2, -6



PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	14	BIT 8 (LSB)
2	BIT 2	13	BIT 7
3	BIT 3	12	BIT 6
4	BIT 4	11	BIT 5
5	OUTPUT	10	N.C.
6	GND	9	+15V
7	-15V	8	GND

NOTE: N.C. MEANS NO CONNECTION

DAC337-3, -4, -5, -7

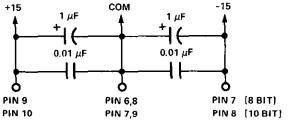


PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	16	BIT 10 (LSB)
2	BIT 2	15	BIT 9
3	BIT 3	14	BIT 8
4	BIT 4	13	BIT 7
5	BIT 5	12	BIT 6
6	OUTPUT	11	N.C.
7	GND	10	+15V
8	-15V	9	GND

NOTE: N.C. MEANS NO CONNECTION

APPLICATIONS INFORMATION

RECOMMENDED POWER SUPPLY BY-PASS CIRCUIT



TRANSFER CHARACTERISTICS

DAC337	TRANSFER CHARACTERISTICS ANALOG OUTPUT							
INPUT PINS	337-0	-1	-2	-6	-3	-4	-5	-7
11111111	0V	+5V	+9.961	+10V				
10000000	-4.961V	+0.040V	+5V	+0.080V				
01111111	-5V	0	+4.961	0V				
00000000	-9.961V	-4.961V	0V	-9.921V				
1111111111					0V	+5V	+9.990V	+10V
1000000000					-4.990V	+0.010V	+5V	+0.020V
0111111111					-5V	0V	+4.990V	0V
0000000000					-9.990V	-4.990V	0V	-9.980V

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the supply voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

Specifications subject to change without notice.

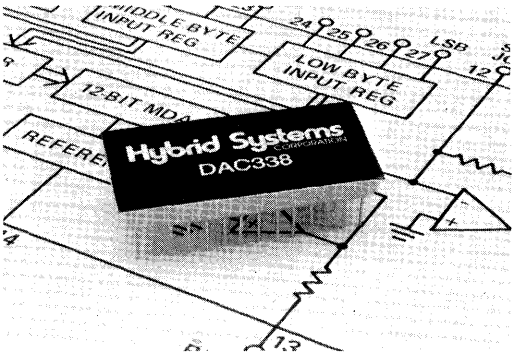
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC338

COMPLETE μP COMPATIBLE 12-BIT DAC

FEATURES

- Output ranges: 0 to +10V, ±10V,
- Coding: binary; offset binary
- Linearity: ±0.01%
- Settling time: 2.5 μS
- μP compatible
- 28-pin package
- CMOS, TTL compatible
- Double buffered inputs



DESCRIPTION

DAC338 is a μP compatible, complete 12-bit double buffered digital-to-analog converter. To enhance application flexibility, the data input registers have been configured as 3 independent, 4-bit bytes. This enables the user to directly interface to 4, 8, and 12-bit data buses. DAC338 comes complete with interface control logic. The three separate byte enable inputs latch data from the bus into the appropriate primary data latches. The LDAC input transfers data from the primary latches to the DAC register. In addition to these input functions are two chip select inputs and a read/write input allowing direct memory-map configurations. All input controls are static to allow hardwired configurations. The DAC338 is packaged in a hermetically sealed package and is rated −55°C to +125°C. The B-models of the DAC338 are fully screened and tested to MIL-STD-883C.

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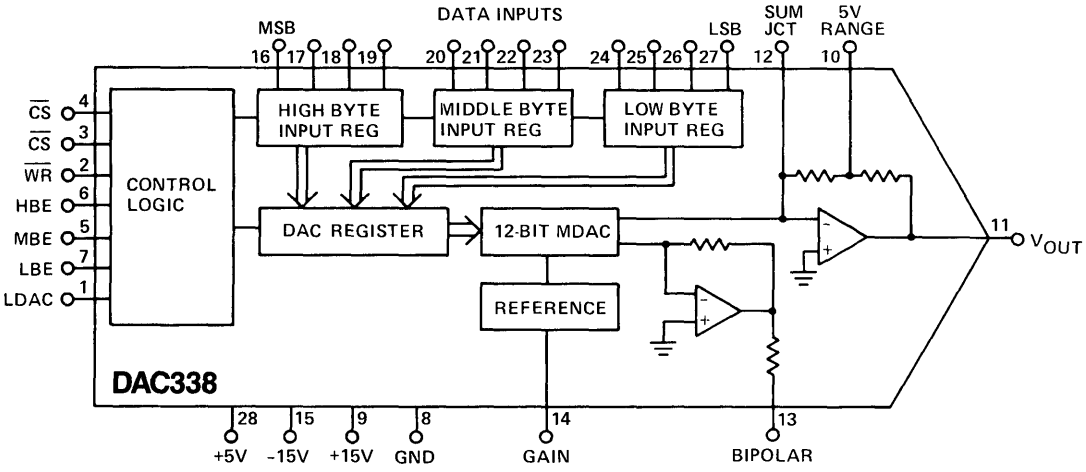
FUNCTIONAL DIAGRAM



SPECIFICTIONS

(Typical @25°C unless otherwise noted. Power supply voltages: +15V, −15V, +5V, (±5%))

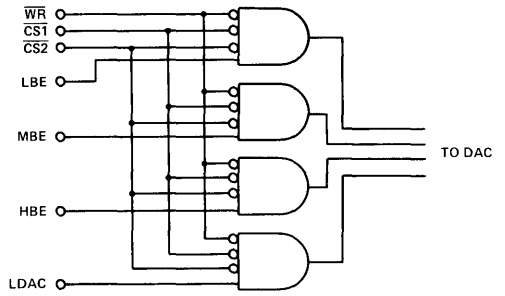
MODEL	DAC338-2	DAC338-0
DIGITAL INPUT		
Resolution	12 Bit	*
Unipolar Code	Binary	*
Bipolar Code	Offset Binary	*
Logic Compatibility[1]	CMOS, TTL	*
Control Logic Inputs		
I_{IH} @V_{IH} = 2.4V	20 μA	*
I_{IL} @V_{IL} = 0.4V	−0.36mA	*
Data Input Current[5]	±1 μA	*
ANALOG OUTPUT		
Scale Factor Accuracy[2]	±0.1% FSR	*
Initial Offset[2]		
Bipolar	±0.1% FSR max	*
Unipolar	±0.05% FSR max	*
Voltage Range[2]		
Bipolar	±10V,	*
Unipolar	0 to +10V	*
STATIC PERFORMANCE		
Integral Linearity[3]	±0.015% FSR max	±0.050% FSR max
Differential Linearity	±0.024 FSR max	±0.097% FSR max
Monotonicity	12 Bits	10 Bits
DYNAMIC PERFORMANCE		
Full Scale Transition		
Settling Time	5 μS max	*
	2.5 μS max	*
Full Scale Transition		
Slew Rate	10V/μS min	*
Delay to Analog Output		
From Bits Input[4]	220nS	*
From LDAC	220nS	*
From CS[4] or WE[4]	225nS	*
STABILITY		
Scale Factor	20ppm FSR	*
Integral Linearity	1ppm FSR max	*
Differential Linearity	1ppm FSR max	*
Offset Drift		
Bipolar	10ppm/°C	*
Unipolar	5ppm/°C	*
Monotonicity Temperature Range	0°C to +70°C	*
±15V POWER SUPPLY		
+15V Supply Current	12mA	*
−15V Supply Current	10mA	*
PSRR	0.005%/%	*
+5V POWER SUPPLY		
+5V Supply Current	24mA	*
TEMPERATURE RANGE		
Operating	−55°C to +125°C	*
Storage	−65°C to +155°C	*
MECHANICAL		
Case Style	Metal	*

NOTES: 1. Control inputs are TTL and 5V CMOS only; data inputs are fully CMOS and TTL compatible. 2. See APPLICATION NOTES for adjustment procedures. 3. Specified as "Best Straight Line". 4. Operating the unit with the DAC Register transparent may result in output "glitches" due to logic skewing with the unit. 5. Digital Input Voltage must not exceed supply voltage or go below −0.5V. "0" 0.8V; 2.4V "1" V_{DD}.

*Same as DAC338-2.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts.

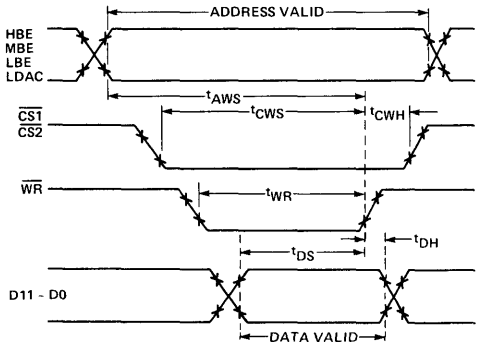
CONTROL LOGIC FUNCTIONAL DIAGRAM



TRUTH TABLE

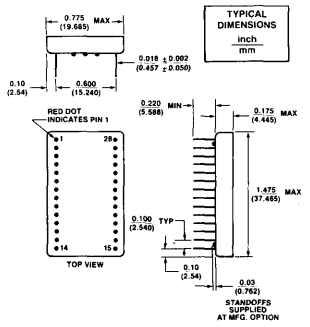
DAC338 CONTROL INPUTS							DAC338 OPERATION
$\overline{WR}$	$\overline{CS1}$	$\overline{CS2}$	LBE	MBE	HBE	LDAC	
1 X X	X 1 X	X X 1	X	X	X	X	Device not selected Output reflects previously loaded data
0	0	0	1	0	0	0	Write data into low byte data register
0	0	0	0	1	0	0	Write data into middle byte data register
0	0	0	0	0	1	0	Write data into high byte data register
0	0	0	0	0	0	1	Load DAC register with data in low byte middle byte and high byte data registers
0	0	0	1	1	1	0	Write data simultaneous into all data registers
0	0	0	1	1	1	1	Write data directly into DAC register

TIMING DIAGRAM



t_{DS} : Data setup time, 250 nsec
t_{DH} : Data hold time, 20 nsec
t_{WR} : Write pulse width, 350 nsec
t_{CWS} : Chip select to write setup time, 375 nsec
t_{CWH} : Chip select to write hold time, 0 nsec
t_{AWS} : Address to write setup time, 250 nsec

PACKAGE OUTLINE



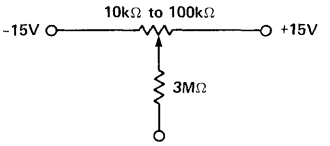
PIN DIAGRAM

PIN	FUNCTION
1	LDAC, LOADS DAC REGISTER AND CHANGES OUTPUT
2	$\overline{WR}$, WRITE INPUT, ACTIVATES ALL CONTROLS
3	$\overline{CS2}$, CHIP SELECT INPUT 2
4	$\overline{CS1}$, CHIP SELECT INPUT 1
5	MBE, MIDDLE BYTE ENABLE, D4 TO D7
6	HBE, HIGH BYTE ENABLE, D8 TO D11
7	LBE, LOW BYTE ENABLE, D0 TO D3
8	GND, GROUND, ANALOG AND DIGITAL GROUND CONNECTED INTERNALLY
9	V_{CC}, +15V SUPPLY
10	RANGE, 5V OUTPUT RANGE INPUT
11	V_{OUT}, DAC VOLTAGE OUTPUT
12	SUMJCT, SUMMING JUNCTION OF OUTPUT OPAMP
13	BIPOLAR, CONNECTED TO SUMJCT FOR BIPOLAR OUTPUT RANGE
14	GAIN, INPUT TO ADJUST FULL SCALE OUTPUT VOLTAGE
15	V_{EE}, -15V SUPPLY
16	D11, DATA INPUT, WEIGHT 2^{-1}, MSB
17	D10, DATA INPUT, WEIGHT 2^{-2}
18	D9, DATA INPUT, WEIGHT 2^{-3}
19	D8, DATA INPUT, WEIGHT 2^{-4}
20	D7, DATA INPUT, WEIGHT 2^{-5}
21	D6, DATA INPUT, WEIGHT 2^{-6}
22	D5, DATA INPUT, WEIGHT 2^{-7}
23	D4, DATA INPUT, WEIGHT 2^{-8}
24	D3, DATA INPUT, WEIGHT 2^{-9}
25	D2, DATA INPUT, WEIGHT 2^{-10}
26	D1, DATA INPUT, WEIGHT 2^{-11}
27	D0, DATA INPUT, WEIGHT 2^{-12}, LSB
28	V_{DD}, +5V SUPPLY, CONTROL LOGIC

OUTPUT CONNECTIONS

RANGE	OUTPUT	CONNECT PIN 12	CONNECT PIN 10	CONNECT PIN 13
0 to +10V	PIN 11	OPEN	OPEN	OPEN
-10V to +10V	PIN 11	PIN 13	OPEN	PIN 12

OUTPUT OFFSET ADJUST

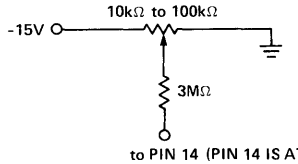


to PIN 12 (PIN 12 IS AT VIRTUAL GROUND)

RANGE: ±0.25% F.S.

Adjust for V_{out} = 0.000 Volt at input code 00 . . . 0 for unipolar operation or at input code 10 . . . 0 for bipolar operation.

OUTPUT GAIN ADJUST



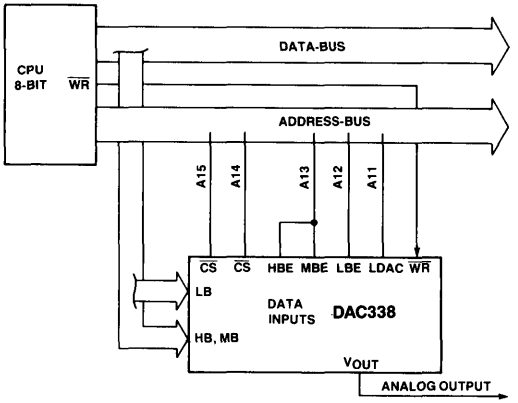
to PIN 14 (PIN 14 IS AT -6.4 VOLTS)

RANGE: ±0.5%

Adjust for V_{out} = +9.9976 Volt at input code 11 . . . 1 (4.9988 Volt on 0-5V range) or for V_{out} = -10.000 Volt at input code 00 . . . 0 (-5.0000 Volt on ±5V range) if set up for bipolar operation.

APPLICATIONS INFORMATION

INTERFACING THE DAC338 TO AN 8-BIT PROCESSOR USING NO EXTERNAL COMPONENTS

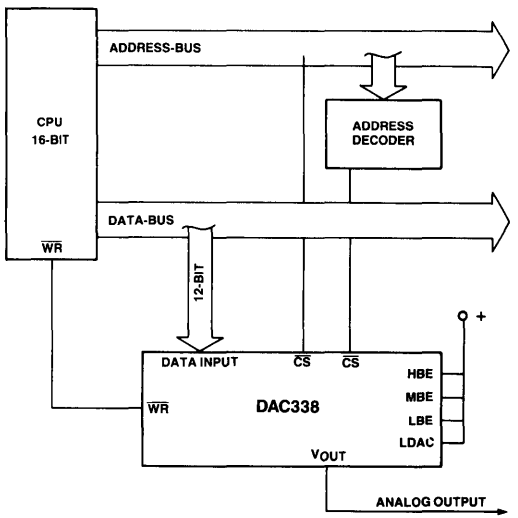


This mode of operation requires 13k bytes of unused addresses. No additional address decoder is necessary. The two chip-select inputs together with the byte-enable and load-DAC inputs are used to control all functions of the DAC. Through selecting the address-lines the user can vary the addresses used to control the DAC. In the above figure the control signals have the following address-configurations (hex):

HBE, MBE	2000
LBE	1000
LDAC	0800

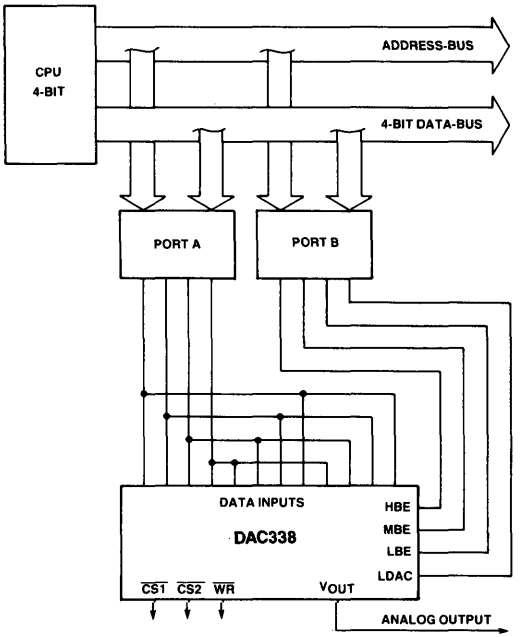
The LDAC input shold not be tied together to the LBE input to ensure correct data transfer between the DAC registers.

INTERFACING THE DAC338 TO A 16-BIT MICROPROCESSOR



Interfacing the DAC338 to a 16-Bit microprocessor is quite easy, because no multiplexing of the data inputs is necessary. An address decoder and the second chip-select input is used to select the DAC.

INTERFACING THE DAC338 to a 4-BIT MICROPROCESSOR USING 4-BIT I/O-PORTS



This figure shows how to operate the DAC338 with two 4-Bit ports. The chip-selects are tied to ground allowing continuous operation; they can be used for operating more DAC's at the same port. In the first step data should appear at the port A outputs; in the second step the control flags should appear on port B.

ORDERING INFORMATION

MODEL	DESCRIPTION
DAC338B-12-2	µP DAC, 0.01% Linearity, 883C
DAC338B-12-0	µP DAC, 0.05% Linearity, 883C

Specifications subject to change without notice.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC347

LOW POWER, WIDE TEMPERATURE RANGE DACs

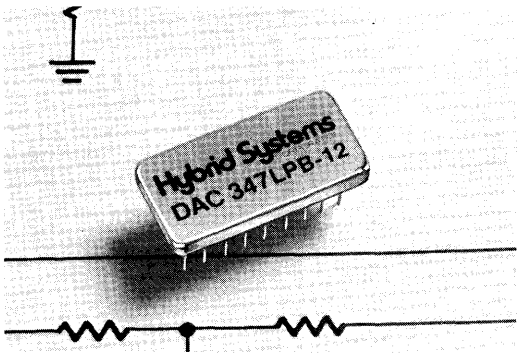
FEATURES

- 10- and 12-bit models
- Very low power: less than 300 mW
- Wide operating temperature range: −55°C to +125°C
- MIL-STD-883 Rev. C, Level B or commercial processing
- 18 pin hermetic package

DESCRIPTION

This Series is specifically designed and tested for low power operation. The models feature low total power dissipation of less than 300 mW. Each unit incorporates a pretrimmed output amplifier and a low power internal reference.

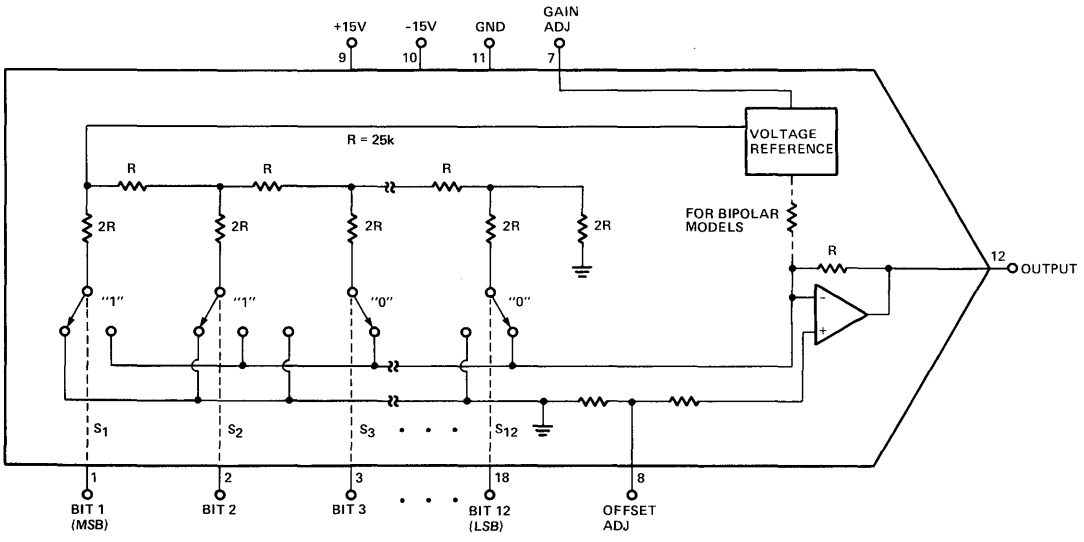
The DAC347 Series are high performance, general purpose, digital-to-analog converters utilizing matched CMOS current switches and ultra stable thin-film nichrome resistor networks. All DAC347 Series models provide optimum stability in performance over the full −55°C to +125°C temperature range.



Unipolar models use complementary binary coding and bipolar models use complementary offset binary coding. Each DAC347 Series converter comes packaged in a hermetically-sealed 18-pin package, ideal for applications where maximum performance in minimum space is required.

7

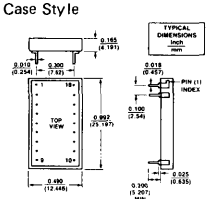
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C using nominal supplies unless otherwise noted).

SERIES	DAC347
TYPE	Fixed Ref, Volt Output
DIGITAL INPUT	
Resolution	
-10 option	10-bits
-12 option	12-bits
Coding Unipolar	Comp. Binary
Bipolar	Comp. Offset Binary
Logic Compatibility[1]	DTL, TTL, CMOS V_{IH}=2.4V (min), V_{IL}=0.8V (max) $I_{IH}=I_{IL}=1\mu A$ (max)
ANALOG OUTPUT[2]	
Voltage Output	
-U option	0 to +10V
-B option	±5V
-G option	±10V
Impedance	0.1Ω
Current	±5mA
REFERENCE	Internal
STATIC PERFORMANCE	
Integral Linearity	±½LSB (max)
Differential Linearity	±½LSB ±1LSB (max)
End Point Accuracy	±0.1%
DYNAMIC PERFORMANCE	
Settling Time for a Worst Case Digital Change	
-10 models (to ±0.05%)	20μS (max)
-12 models (to ±0.05%)	20μS (max)
-25°C TO +85°C OPERATION	
Change in Accuracy[3]	
-10 models	±0.15% F.S.R.
-12 models	±0.1% F.S.R.
Differential Linearity	
-10 models	±0.1% F.S.R.
-12 models	±0.025% F.S.R.
Linearity Error	
-10 models	±0.05% F.S.R.
-12 models	±0.0125% F.S.R.
-55°C TO +125°C OPERATION	
Change in Accuracy	
-10 models	±0.7% F.S.R.
-12 models	±0.35% F.S.R.
Differential Linearity	
-10 models	±0.1% F.S.R.
-12 models	±0.05% F.S.R.
Linearity Error	
-10 models	±0.05% F.S.R.
-12 models	±0.025% F.S.R.
POWER REQUIREMENTS	
Power Supply	+15V, ±3% @ 6mA (typ), 9mA (max) -15V, ±3% @ 9mA (typ), 12mA (max)
Power Supply Rejection Ratio	0.001%/% (typ), 0.002%/% (max)
ENVIRONMENTAL	
Operating Temperature Range	-55°C to +125°C B Versions 0°C to 70°C C Versions
MECHANICAL	
Case Style	18 pin ceramic

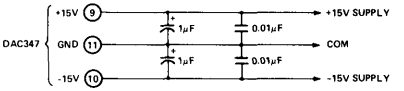


PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	18	BIT 12 (LSB)
2	BIT 2	17	BIT 11
3	BIT 3	16	BIT 10
4	BIT 4	15	BIT 9
5	BIT 5	14	BIT 8
6	BIT 6	13	BIT 7
7	GAIN ADJ	12	OUTPUT
8	OFFSET ADJ	11	GND
9	+15V	10	-15V

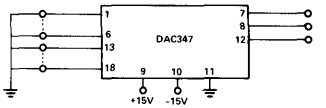
NOTES:
1. Logic input should not exceed +5.5V or be below −0.3V.
2. Full scale range and offset voltage are externally adjustable.
3. Includes effects of scale factor, zero and linearity.
4. In case of discrepancy between package shown in photograph and package outline dimension, the mechanical outline is correct.

APPLICATIONS INFORMATION

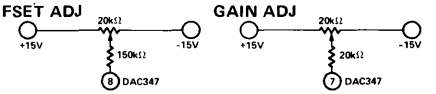
RECOMMENDED POWER SUPPLY BYPASS CIRCUIT



RECOMMENDED BURN-IN CIRCUIT
(Standard for MIL-STD-883 models)



OPTIONAL OFFSET AND GAIN ADJUSTMENTS



Calibration Prodedures

Unipolar models
1. Apply a 111...1 input code and set the OFFSET ADJUST potentiometer for 0 volt output.
2. Apply a 000...0 input code and set the GAIN ADJUST potentiometer for desired full scale output.

Bipolar models
1. Apply a 0111...1 input code and set the OFFSET ADJUST potentiometer for 0 volt output.
2. Apply a 000...0 input code and set the GAIN ADJUST potentiometer for desired (+) full scale output.

TRANSFER CHARACTERISTICS

UNIPOLAR, -U MODELS (0 to +10V OUTPUT)													
Complementary Binary Input Code												Analog Output	
MSB	2	3	4	5	6	7	8	9	10	11	LSB	Weighting	Voltage
1	1	1	1	1	1	1	1	1	1	1	1	Zero	+0.000V
1	1	1	1	1	1	1	1	1	1	1	0	+1 LSB	+0.0024V
0	1	1	1	1	1	1	1	1	1	1	1	+½ F.S.	+5.000V
0	0	0	0	0	0	0	0	0	0	0	0	+F.S. -1 LSB	+9.9976V

BIPOLAR, -B MODELS (±5V OUTPUT)													
Complementary Offset Binary Input Code												Analog Output	
MSB	2	3	4	5	6	7	8	9	10	11	LSB	Weighting	Voltage
1	1	1	1	1	1	1	1	1	1	1	1	-F.S.	-5.000V
1	0	0	0	0	0	0	0	0	0	0	0	-1 LSB	-0.0024V
0	1	1	1	1	1	1	1	1	1	1	1	Zero	+0.000V
0	0	0	0	0	0	0	0	0	0	0	0	+F.S. -1 LSB	+4.9976V

BIPOLAR, -G MODELS (±10V OUTPUT)													
Complementary Offset Binary Input Code												Analog Output	
MSB	2	3	4	5	6	7	8	9	10	11	LSB	Weighting	Voltage
1	1	1	1	1	1	1	1	1	1	1	1	-F.S.	-10.000V
1	0	0	0	0	0	0	0	0	0	0	0	-1 LSB	-0.0048V
0	1	1	1	1	1	1	1	1	1	1	1	Zero	+0.000V
0	0	0	0	0	0	0	0	0	0	0	0	+F.S. -1 LSB	+9.9951V

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts.

ORDERING INFORMATION

MODEL	DESCRIPTION
DAC347LPB-10-G	MIL, 10-Bit, ±10V
DAC347LPB-12-G	MIL, 12-Bit, ±10V
DAC347LPB-10-B	MIL, 10-Bit, ±5V
DAC347LPB-12-B	MIL, 12-Bit, ±5V
DAC347LPB-10-U	MIL, 10-Bit, 0 to +10V
DAC347LPB-12-U	MIL, 12-Bit, 0 to +10V
DAC347LPC-10-G	Comm, 10-Bit, ±10V
DAC347LPC-12-G	Comm, 12-Bit, ±10V
DAC347LPC-10-B	Comm, 10-Bit, ±5V
DAC347LPC-12-B	Comm, 12-Bit, ±5V
DAC347LPC-10-U	Comm, 10-Bit, 0 to +10V
DAC347LPC-12-U	Comm, 12-Bit, 0 to +10V

LPC models are commercially processed.
LPB models are processed to MIL-STD-883 Rev. C, Level B.

Specifications subject to change without notice.

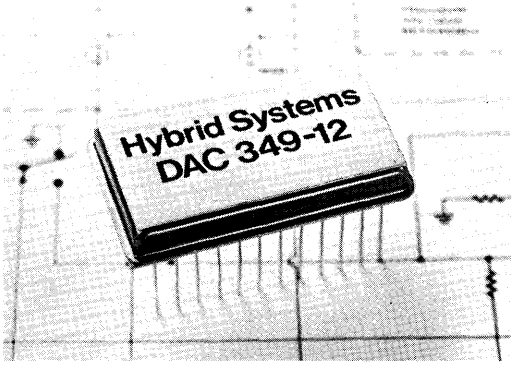
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC349

LOW POWER, 12-BIT, CMOS DACs

FEATURES

- 12-bits binary or 3-decades BDC
- Low power: 300mW
- Commercial, industrial and MIL-STD-883 models
- 5 pin selectable output ranges



DESCRIPTION

The DAC349 Series are versatile, low power 12-bit D/A converters that are intended for fixed reference applications. These units combine a novel CMOS switching technique with a precision, ultra-stable thin-film ladder to achieve accurate conversion with low power drain; improved reliability and near-instantaneous warmup are major advantages of reduced power consumption. All models include an internal precision reference and a gain-selectable output amplifier.

The DAC349 Series offers a choice of either 12-bit binary coding (-12 models) or 3 decade BCD coding (-3D models).

By external pin jumpering, the binary models can be connected for unipolar output ranges of 0 to −5V or 0 to −10V and for offset binary coded bipolar outputs of ±2.5V, ±5V and ±10V. For ratiometric applications, the units operate from an external fixed DC reference of −10V ±10%.

Both binary and BCD models are available in commercial/industrial and MIL-STD-883 Rev. C, Level B versions. The DAC349B is specified over a temperature range of −55°C to +125°C. Both versions operate −55°C to +125°C.

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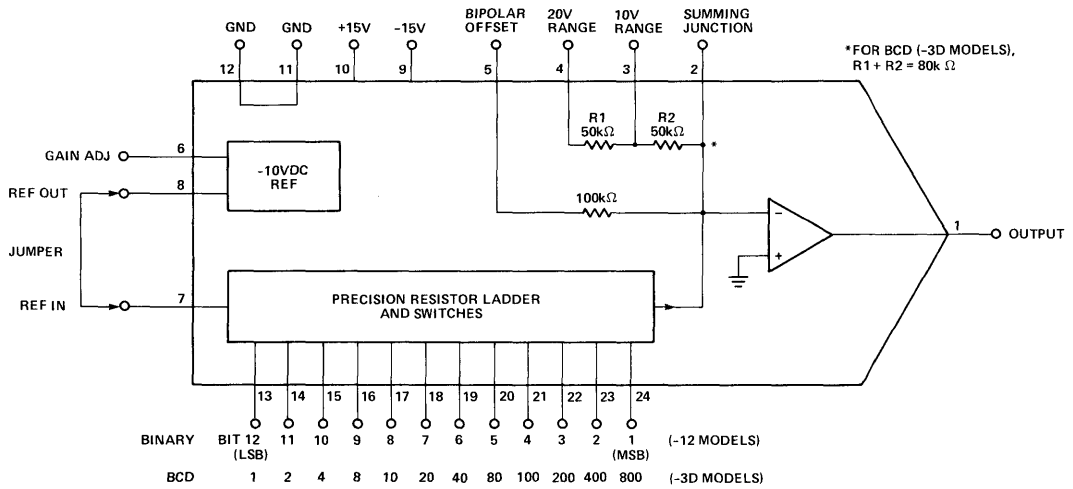
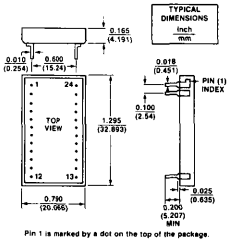
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C and nominal power supplies unless otherwise noted)

SERIES	DAC349
TYPE	Fixed Reference, Voltage Output
DIGITAL INPUT	
Resolution	12 Bits Binary (-12) or 3 Decades BCD (-3D)
Unipolar Coding	Binary or BCD
Bipolar Coding	Offset Binary
Logic Levels	
Binary	V_{IH}=2.4V min, V_{IL}=0.8V max
BCD	V_{IH}=3.5V min, V_{IL}=1.5V max
Input Current	±1μA max
ANALOG OUTPUT	
Voltage Range	0 to -5V, 0 to -10 ±2.5V, ±5V, ±10V
Current Compliance	±5mA (min)
Impedance	≤0.1
Scale Factor[1]	±0.1% of F.S.R. (max)
Unipolar Offset[1]	±0.2% of F.S.R. (max)
Bipolar Offset[1]	±0.1% of F.S.R. (max)
REFERENCE	
Internal[2]	-10VDC
External (D.C. only)	-10VDC ±10% @ 1mA
STATIC PERFORMANCE	
Linearity	±½ LSB (max)
Differential Linearity	±1 LSB (max)
DYNAMIC PERFORMANCE	
Settling Time	15μS (max)
Slew Rate	1V/μS
STABILITY	
Accuracy vs Temp.[3]	30ppm/°C (max)
Linearity vs Temp.	5ppm/°C (max)
Differential Linearity vs Temp.	2ppm/°C (max)
POWER SUPPLY	
Voltage @ Current	+15V @ 5mA (nom): 10mA (max) +13V to +18V; -15V @ 15mA (nom): 20mA (max) -13V to -18V
Rejection Ratio	0.005%/%
Power Consumption	375mW (max)
TEMPERATURE RANGE	
Specified	
DAC349C	-25°C to +85°C
DAC349B	-55°C to +125°C
Operating, All models	-55°C to +125°C
Storage, All models	-65°C to +150°C
MECHANICAL	
Case Style	Ceramic



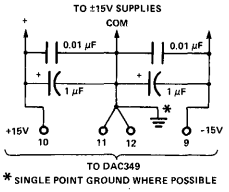
PIN NO.	FUNCTION	PIN NO.	FUNCTION BINARY	FUNCTION BCD
1	OUTPUT	24	BIT 1 (MSB)	800
2	SUMMING JCT	23	BIT 2	400
3	10V RANGE	22	BIT 3	200
4	20V RANGE	21	BIT 4	100
5	BIPOLAR OFFSET	20	BIT 5	80
6	GAIN ADJ	19	BIT 6	40
7	REF IN	18	BIT 7	20
8	REF OUT	17	BIT 8	10
9	-15V	16	BIT 9	8
10	+15V	15	BIT 10	4
11	GND	14	BIT 11	2
12	GND	13	BIT 12(LSB)	1

NOTES:
1. Offset and gain are externally adjustable. See APPLICATIONS INFORMATION.
2. For specified overall performance, external loading of the reference output (Pin 8) must not exceed 1.0 mA.
3. Total effect of linearity, offset and gain tempco's on the transfer characteristics of the unit.
4. In case of discrepancy between package shown in photograph and package outline dimension, the mechanical outline is correct.

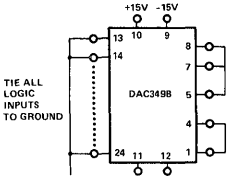
Specifications subject to change without notice.

APPLICATIONS INFORMATION

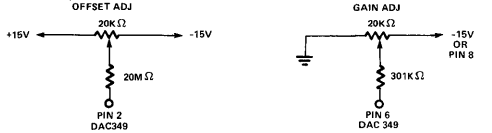
RECOMMENDED POWER SUPPLY BYPASS CIRCUIT



RECOMMENDED BURN-IN CIRCUIT (Standard for MIL-STD-883 Models)



OPTIONAL ADJUSTMENTS



Binary Unipolar Operation:
1. Apply a 0 0 0 . . . 0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 1 1 1 . . . 1 input code and set the GAIN ADJ pot for -(F.S. - 1 LSB).

Binary Bipolar Operation:
1. Apply a 1 0 0 . . . 0 input code and set the OFFSET ADJ pot for a zero output.
2. Apply a 1 1 1 . . . 1 input code and set the GAIN ADJ pot for -(F.S. - 1 LSB).

BCD Unipolar Operation:
1. Apply a 0 0 0 . . . 0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply 1001 1001 1001 input and set the GAIN ADJ pot for -9.990V.

RANGE SCALING*

Output Voltage Range	Jumper These Pins	Connect Pin 5 to Pin	Coding
0 to -5V	1 & 3, 2 & 4	11	Binary
0 to -10V	1 & 3	11	
0 to -9.99V	1 & 4	**	BCD
±2.5V	1 & 3 2 & 4	7	Offset Binary
±5V	1 & 3	7	
±10V	1 & 4	7	

*Pin 7 must be connected to either the internal reference (Pin 8) or to an external -10VDC reference source.
**No connection on BCD (-3D) models.

TRANSFER CHARACTERISTICS

Binary Unipolar Operation

Digital Input	Analog Output
1 1 1 . . . 1	-(F.S. -1 LSB)
1 0 0 . . . 0	-F.S./2
0 0 0 . . . 0	0V

BCD Unipolar Operation

Digital Input	Analog Output
1001 1001 1001	-9.99
0101 0000 0000	-5.00
0000 0000 0000	0V

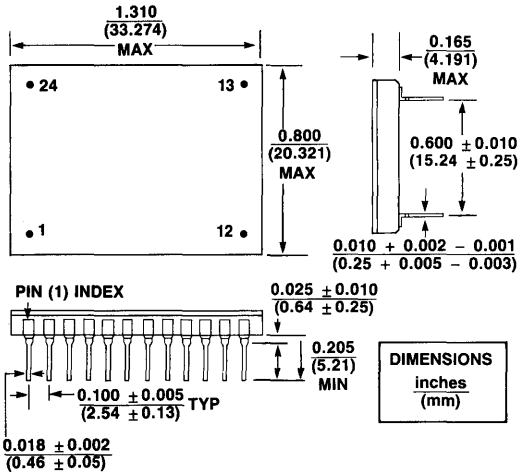
Binary Bipolar Operation

Digital Input	Analog Output
1 1 1 . . . 1	-(F.S. -1 LSB)
1 0 0 . . . 0	0V
0 0 0 . . . 0	+F.S.

ORDERING INFORMATION

MODEL	DESCRIPTION
DAC349C-12	Comm, 12-Bit, -25°C to +85°C
DAC349C-3D	Comm, 3-Decade, -25°C to +85°C
DAC349B-12	MIL, 12-Bit, -55°C to +125°C
DAC349B-3D	MIL, 3-Decade, -55°C to +125°C

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts.


1.310
(33.274)
MAX
• 24
13 •
• 1
12 •
0.800
(20.321)
MAX
0.165
(4.191)
MAX
0.600 ±0.010
(15.24 ±0.25)
0.010 + 0.002 − 0.001
(0.25 + 0.005 − 0.003)
PIN (1) INDEX
0.025 ±0.010
(0.64 ±0.25)
0.205
(5.21)
MIN
0.100 ±0.005
(2.54 ±0.13) TYP
0.018 ±0.002
(0.46 ±0.05)
DIMENSIONS
inches
(mm)

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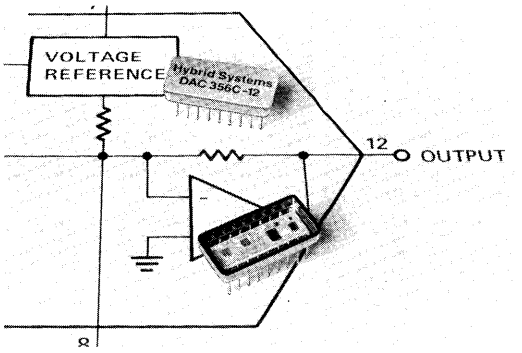
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC356

ULTRA-LOW POWER 12-BIT IC DACs

FEATURES

- Low power: 75mW versions
- −55°C to +125°C operation
- MIL-STD-883 or commercial processing
- Internal reference and output amplifier
- Hermetic 18-pin package



DESCRIPTION

Only DAC356 Series 12-bit digital-to-analog converters (DACs) offer minimum power consumption of available low cost DACs with internal references and output amplifiers. DAC356LP-12 operates switches, ladder network, internal reference and output amplifier on just 75mW typical, 90mW maximum. Each DAC is hermetically sealed in a compact 18-pin, single DIP width package.

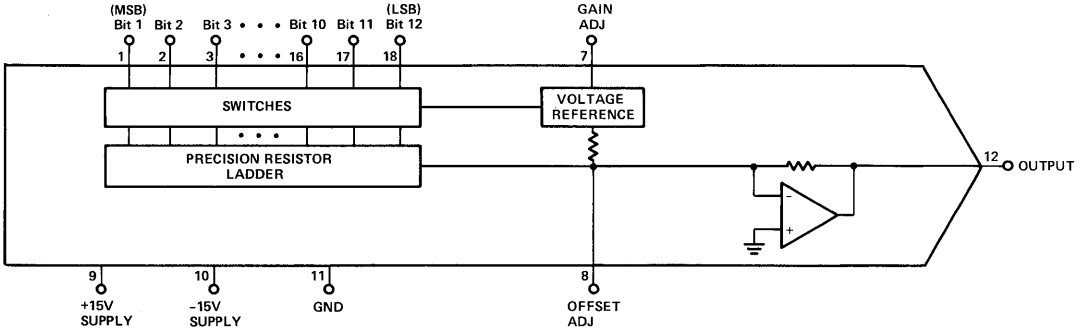
Low power operation is accomplished using matched CMOS current switches. All models are factory trimmed to ±0.1% of full scale range (FSR) and may be further adjusted to an accuracy of ±0.02% or better (see APPLICATIONS INFORMATION).

The DAC356 Series uses complementary offset binary coding and delivers an output of ±10V @5mA (consult factory for other ranges). Input logic is DTL, TTL, and CMOS compatible. Settling time for 1 LSB change to ±0.02% FSR is 5μS; a full scale change settles in 50μS. Gain drift is ±30ppm/°C FSR. Operation is from ±13 to ±18 volt power supplies (±15V nominal). The DAC356 is an ultra low power version of the DAC346 and DAC347.

DAC356 Series models are of particular advantage in systems that incorporate large numbers of DACs...where the accumulated power consumption can be significant. DAC356 Series allows minimum power supply size and expense. Related heat removal requirements are also diminished. And DAC356 Series' wide tolerance on power supply voltages (versus ±3% tolerance usual for higher power drain units) further eases supply needs. In systems applications of large or small DAC quantities, DAC356 Series' units offer increased reliability and wider operating temperature range.

7

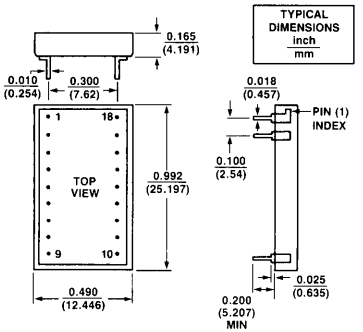
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C and nominal supplies unless otherwise noted)

SERIES	DAC356
TYPE	Fixed Ref, Volt Output
DIGITAL INPUT	
Resolution	12-Bits
Coding	Complementary Offset Binary
Logic Compatibility[1]	V_{IH}= 2.4V min, V_{IL}= 0.8V max
Input Current	±1μA max
ANALOG OUTPUT[2]	
Voltage @ Current	±10 Volts @ ±5mA
Impedance	0.1Ω
Initial Accuracy[3]	±0.1% F.S.R.
Output Protection	Short Circuit to GND (Continuous)
REFERENCE	Internal
STATIC PERFORMANCE	
Integral Linearity	±0.012% F.S.R. max
Differential Linearity	±½LSB typ, ±1LSB max
End Point Accuracy	±0.1% max
DYNAMIC PERFORMANCE	
Settling Time for 1 LSB Change to ±0.02% F.S.R.	5μS
Settling Time for Full Scale Change to ±0.02% F.S.R.	50μS
STABILITY	
Gain	±30ppm/°C F.S.R. (max)
Offset	±10ppm/°C F.S.R. (max)
Differential Linearity	±5ppm/°C F.S.R. (max)
POWER REQUIREMENTS	
+15V Supply Voltage	+13 to +18 Volts
+15V Supply Current	2.5mA, typ; 3.0mA, max
-15V Supply Voltage	-13 to -18 Volts
-15V Supply Current	2.5mA, typ; 3.0mA, max
Rejection Ratio	0.002%/% max
TEMPERATURE RANGE	
Operating	-55°C to +125°C B Version 0°C to 70°C C Version
MECHANICAL	
Case Style	Metal



Pin 1 is marked by a dot on the top of the package.

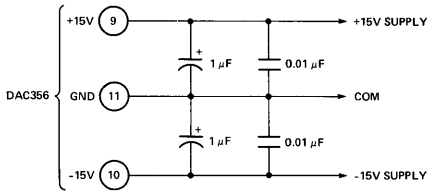
Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	18	BIT 12 (LSB)
2	BIT 2	17	BIT 11
3	BIT 3	16	BIT 10
4	BIT 4	15	BIT 9
5	BIT 5	14	BIT 8
6	BIT 6	13	BIT 7
7	GAIN ADJ	12	OUTPUT
8	OFFSET ADJ	11	GND
9	+15V	10	-15V

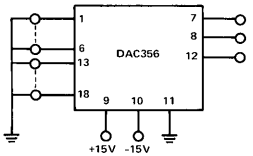
NOTES:
1. Logic input should not exceed +15.0V or be below -0.3V.
2. Full scale range and offset voltage are externally adjustable. See APPLICATIONS INFORMATION.
3. Can be adjusted to ±0.02% F.S.R. or better. See OPTIONAL OFFSET AND GAIN ADJUSTMENTS in APPLICATIONS INFORMATION.

APPLICATIONS INFORMATION

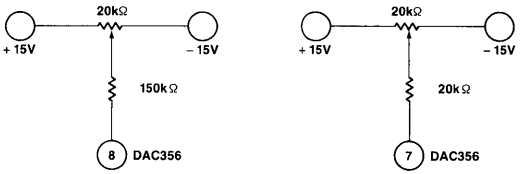
RECOMMENDED POWER SUPPLY BYPASS CIRCUIT



RECOMMENDED BURN-IN CIRCUIT
(Standard for MIL-STD-883 models)



OPTIONAL OFFSET AND GAIN ADJUSTMENT CIRCUITS



Quick Calibration Procedure

1. Apply a 0 1 1 . . . 1 1 1 input code and set the OFFSET ADJ pot for zero output.
2. Apply a 1 1 1 . . . 1 1 1 input code and set the GAIN ADJ pot for -F.S. output.

TRANSFER CHARACTERISTICS

Complementary Offset Binary Input Code												Analog Output	
MSB	2	3	4	5	6	7	8	9	10	11	LSB	Weighting	Voltage
1	1	1	1	1	1	1	1	1	1	1	1	-F.S	-10.000V
1	0	0	0	0	0	0	0	0	0	0	0	-1 LSB	-0.0048V
0	1	1	1	1	1	1	1	1	1	1	1	ZERO	+0.000V
0	0	0	0	0	0	0	0	0	0	0	0	+F.S. -1LSB	+9.9952V

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the supply voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

ORDERING INFORMATION

MODEL	DESCRIPTION
DAC356LPC-12	Comm, Ultra-Low Power, 12-Bits
DAC356LPB-12	MIL, Ultra-Low Power, 12-Bits

C models are commercially processed.
B models are processed to MIL-STD-883 Rev. C, Level B.

Specifications subject to change without notice.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC370-18

18-BIT STORAGE REGISTER, MDAC

FEATURES

- True 16-bit (0.0008%) linearity
- Two chip construction
- Input registers
- Low power
- Hermetic 28-pin DIP
- 2- and 4-quadrant multiplication
- Single-supply operation
- Available with MIL-STD-883 screening and testing

DESCRIPTION

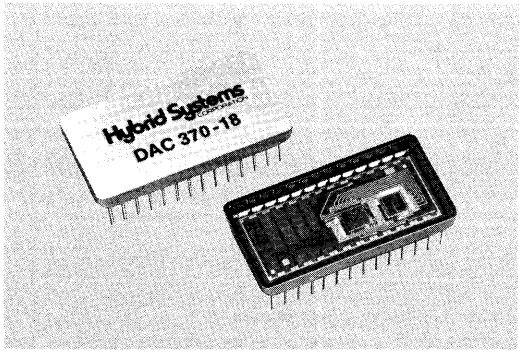
The DAC370-18 is a true 16-bit linear D/A converter manufactured with the most advanced proprietary monolithic devices[1] and proven packaging technique. A single, unique monolithic chip contains switches, storage registers and other electronics for high resolution and low linearity error. A second, passive chip provides all the resistors needed for this multiplying D/A. Input storage registers are in two 8- and one 2-bit segments with independent latching — a system that is compatible with most microprocessor data bus interfaces. Combining 2-and 4-quadrant multiplying capability, TTL/DTL and CMOS compatibility, low power consumption and operation from a single supply, the DAC370-18 offers exceptional performance/cost ratio.

Outstanding features include:

True 16-Bit Linearity — 16-bit (0.0008%) linearity with 18-bit resolution is now a reality. No other microcircuit converter does better.

Low Power — CMOS proprietary monolithic devices in a unique circuit configuration yield extremely low power (60 mW max).

Two-Chip Construction — The most advanced monolithic device, combined with our own resistor network is all that is needed in this converter. Fully automatic wire-bonding makes the most consistently superior assembly available.

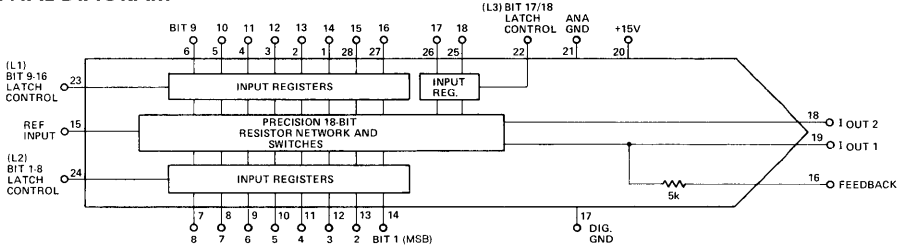


Input Storage Registers — Designed as two 8-bit and one 2-bit segments, the input registers provide data storage when latched, but are "transparent" when unlatched. Data conversion can now be performed continuously **or** from stored data.

Reliability — Our 28-pin hermetically-sealed package offers the utmost in reliability microelectronic converter products. Combined with our proprietary monolithic device and automatic wirebonding, we've made the DAC370-18 the most reliable high resolution device to date. Reliability is further enhanced by batch-processed, precision laser-trimmed resistor networks fabricated in our own facility. Networks are functionally trimmed and glass passivated to assure reliability under adverse environmental conditions. DAC370-18 converters are available fully screened and tested to MIL-STD-883C.

Advanced designs, proven processes and continuous monitoring during all production operations by our quality control organization are combined with rigorous AQL screening to provide the most reliable converter possible.

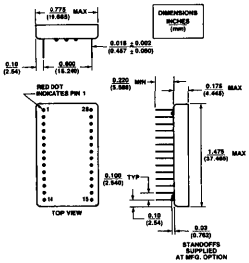
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C and nominal power supply, V_{REF} = +10V, unipolar unless otherwise noted)

MODEL	DAC370-18
TYPE	Multiplying, latched inputs
DIGITAL INPUT	
Resolution	18 bits
2-Quad. Unipolar Coding	Binary
4-Quad. Bipolar Coding	Offset binary
Logic Compatibility	DTL, TTL, CMOS V_{IH} > 2.4V min V_{IL} < 0.8V max
Input Leakage Current	±1μA max, 0.4V > V_{LOGIC} > 3.2V
Strobe Width	250 ns min
Data Set-Up Time[1]	500 ns min
REFERENCE INPUT	
Voltage Range	±25V max
Input Impedance	5K
ANALOG OUTPUT	
Gain Accuracy[2]	0.1% typ, 0.2% max
Offset[3] (Unipolar)	5Cμ V max
Small Signal 3 dB Bandwidth	1 MHz
Output Capacitance C_{OUT1}	90 pF
C_{OUT2}	70 pF
STATIC PERFORMANCE	
Integral Linearity (best straight line)	±0.0008% typ, ±0.0015% max
Differential Linearity (monotonic to 16-Bits)	±0.0004% typ, ±0.0015% max
DYNAMIC PERFORMANCE	
Major Code Transition Settling to 0.01% FSR (strobed)	2μ s
Reference Feedthrough Error (V_{REF} = 20 Vpp @ 10 kHz)	2 mVp-p
STABILITY[3,5] (Over Specified Temp. Range)	
Scale Factor[4]	2 ppm/°C FSR typ, 6 ppm/°C max
Linearity	1 ppm/°C FSR max
Differential Linearity	1 ppm/°C FSR max
Linearity	±0.0115% max @ +125°C ±0.0095% max @ −55°C
Differential Linearity	±0.0115% max @ +125°C ±0.0095% max @ −55°C
POWER SUPPLY (V_{DD})	
Voltage Range @ Current	+15V nom; +11.5V to +15.5V @ 1.5 mA
Rejection Ratio (14.0V-16.0V)	0.002%/% max
Power Dissipation (inputs @ GND, V_{REF} = 0)	60 mW max
TEMPERATURE RANGE	
Operating — B Option	−55°C to +125°C
Operating — C Option	0°C to +85°C
Storage	−65°C to +150°C
MECHANICAL	
Case Style	28-pin double-DIP metal
Case Dimensions	

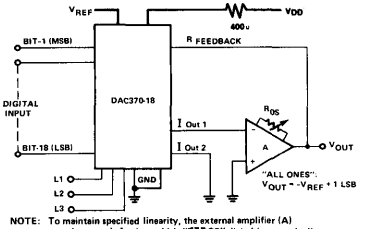


PIN	FUNCTION	PIN	FUNCTION
1	BIT 14	28	BIT 15
2	BIT 13	27	BIT 16
3	BIT 12	26	BIT 17
4	BIT 11	25	BIT 18
5	BIT 10	24	2^{-1}–2^{-8} LATCH
6	BIT 9	23	2^{-9}–2^{-16} LATCH
7	BIT 8	22	2^{-17}, 2^{-18} LATCH
8	BIT 7	21	ANA GND
9	BIT 6	20	+15V
10	BIT 5	19	I_{out} 1
11	BIT 4	18	I_{out} 2
12	BIT 3	17	DIG GND
13	BIT 2	16	FEEDBACK
14	BIT 1	15	REF INPUT

NOTES:
1. Time data must be stable before Strobe goes to "1".
2. Using internal feedback resistor.
3. Using the internal $R_{feedback}$ with nulled external amplifier in a constant 25°C ambient. (Offset doubles every 10°C.)
4. The DAC370-18 is designed to be used only in those applications where the current output is virtual ground; i.e., the summing junction of an op amp in the inverting mode. The internal feedback resistor (R Feedback) must be used to achieve temperature tracking. See APPLICATIONS INFORMATION for recommended circuit configurations.
5. For further information on long term drift, refer to HS 377 Application Notes, page 140.

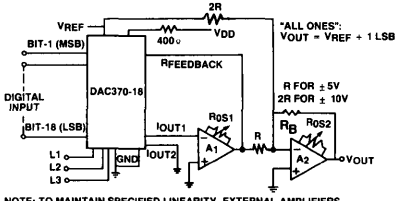
APPLICATIONS INFORMATION

UNIPOLAR OPERATION (2-Quadrant Multiplication)



NOTE: To maintain specified linearity, the external amplifier (A) must be zeroed. Apply an ALL "ZEROS" digital input and adjust R_{OS} for V_{OUT} = 0 ±1mV.

BIPOLAR OPERATION (4-Quadrant Multiplication)



NOTE: TO MAINTAIN SPECIFIED LINEARITY, EXTERNAL AMPLIFIERS (A_1 AND A_2) MUST BE ZEROED. WITH A DIGITAL INPUT OF 10...0 AND V_{REF} SET TO ZERO:
a) SET R_{OS1} FOR V_{O1} = 0
b) SET R_{OS2} FOR V_{OUT} = 0
c) SET V_{REF} TO +10V AND ADJUST R_B FOR V_{OUT} TO BE 0 VOLTS.

UNIPOLAR OPERATION
Transfer Characteristics

BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-N})$
100...001	$-V_{REF}(½+2^{-N})$
100...000	$\frac{-V_{REF}}{2}$
011...111	$-V_{REF}(½-2^{-N})$
000...001	$-V_{REF}(2^{-N})$
000...000	0

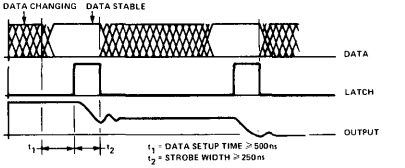
BIPOLAR OPERATION
Transfer Characteristics

OFFSET BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-(N-1)})$
100...001	$-V_{REF}(2^{-(N-1)})$
100...000	0
011...111	$V_{REF}(2^{-(N-1)})$
000...001	$V_{REF}(1-2^{-(N-1)})$
000...000	V_{REF}

STROBE LOGIC

Strobe	Function
0	data latched (held)
1	data changing (transfer)

TIMING DIAGRAM



PRECAUTIONARY NOTE:
In order to realize the ultimate resolution which this unit is capable of delivering, several precautions must be taken.
(1) Amplifiers must be balanced so the summing junction is as close to zero volts as can be achieved. Usually less than 100μ V.
(2) Amplifiers must have a large enough open loop gain to be consistent with the required linearity. To obtain optimum performance this should be in excess of 10^5V/V or 100 dB.
(3) All grounds should be of low resistance.
(4) Reference should be as high as possible to minimize errors due to offset at outputs.
(5) To maintain accuracy over temperature amplifiers should have low bias current and offset voltage temperature coefficients.
(6) For optimum performance refer to APPLICATIONS INFORMATION in front of catalog.
(7) Tie unused inputs to ground.
(8) Do not apply digital inputs before V_{DD} supply.
(9) Unused inputs must be grounded.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts.

ORDERING INFORMATION

MODEL NUMBER	DESCRIPTION
DAC370B-18	18-Bit MDAC, +15V Operation, MIL
DAC370C-18	18-Bit MDAC, +15V Operation, COMM

Specifications subject to change without notice.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC377-18 SERIES

COMPLETE BUFFERED 18-BIT DAC

FEATURES

- True 16-bit (0.0008%) linearity
- Complete with internal reference, input storage registers, output amplifier
- Low power
- Hermetic 28-pin DIP
- Available with MIL-STD-883 screening and testing

DESCRIPTION

The DAC377-18 is a complete 18-bit D/A converter with true 16-bit linearity. Complete with storage registers, internal reference and output amplifier, DAC377-18 provides the user with exceptional performance and self-contained operation. Input storage resisters are in two 8-bit and one 2-bit segments with independent latching — a system compatible with most microprocessor data bus interfaces. A single proprietary[1] monolithic chip contains switches, storage registers and other electronics for high resolution and low linearity error.

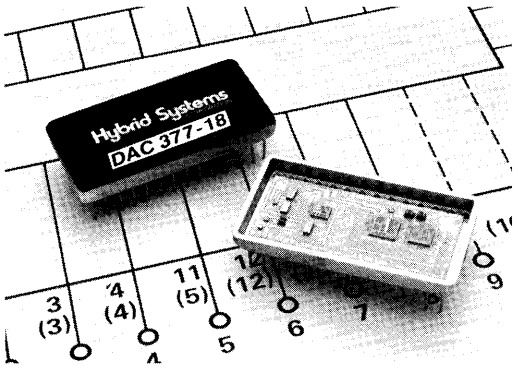
Outstanding features include:

True 16-Bit Linearity — 16-bit (±0.0008%) linearity with 18-bit resolution is unequaled. No other microcircuit converter does better.

Low Power — CMOS proprietary monolithic devices in a unique circuit configuration yield the lowest power dissipation (450 mW typ) of any complete 18-bit converter available.

Complete — No external components are required for 18-bit conversion.

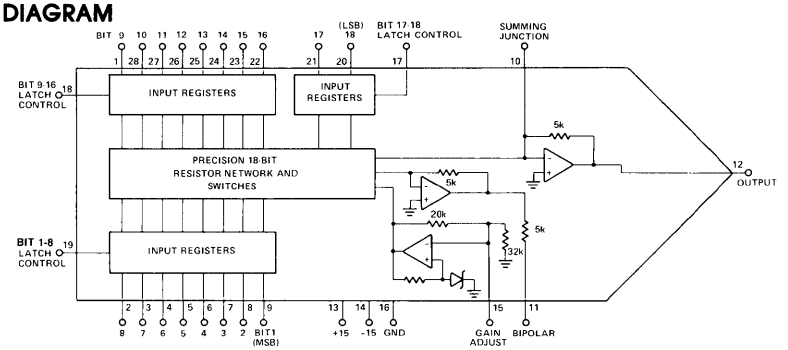
Input Storage Registers — Designed as two 8-bit and one 2-bit segments, the input storage registers provide data storage when latched, but are "transparent" when unlatched, allowing data conversion to be performed continuously **or** from stored data.



Reliability — Our 28 pin hermetically-sealed package performs reliably in adverse environments. Together with our own proprietary monolithic device and automatic wirebonding, DAC377-18 is one of the most reliable high resolution devices to date. Batch-processed precision thin-film resistor networks fabricated in our own facility are functionally laser-trimmed and glass passivated to assure proven performance in the toughest environments. Continuously monitored during assembly and test, each production lot is screened 100% to assure reliable performance to all specifications. DAC377B-18 models are fully screened and tested to MIL-STD-883 Rev. C, Levels B or S.

Advanced designs, proven processes and continuous monitoring during all production operations by our quality control organization are combined with rigorous AQL screening to provide the most dependable converter possible.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25° C nominal power supply, no load, unless otherwise noted)

MODEL	DAC377-18
TYPE	Latched Inputs, Voltage Output
DIGITAL INPUT	
Resolution	18-Bits
Unipolar Coding	Binary
Bipolar Coding	Offset Binary
Logic Compatibility[1]	DTL, TTL, CMOS
Input Leakage Current	±1μA (max), 0.4V>V_{LOGIC}>3.2V
Latch Control Width	250hS (min)
Data Set-up Time[2]	500nS (min)
Data Hold Time[3]	0nS (min)
ANALOG OUTPUT	
Scale Factor[4]	±0.15% F.S.R. (max)
Initial Offset[4]	
Unipolar	±0.05% F.S.R. (max)
Bipolar	±0.05% F.S.R. (max)
Voltage Range	
Unipolar	0 to +10V
Bipolar	±10V
Current Compliance	±5 mA
Output Impedance	< 1Ω
Noise	
PP-noise (wideband)	0.0005% F.S.R.
REFERENCE	
Internal[5]	
STATIC PERFORMANCE	
Integral Linearity[6]	±0.0008% F.S.R. (typ) ±0.0015% F.S.R. (max)
Differential Linearity[7]	±0.0004% F.S.R. (typ) ±0.0015% F.S.R. (max)
Monotonicity	Guaranteed to 16-bits
DYNAMIC PERFORMANCE	
Major Code Transition Settling to 0.006% F.S.R. (strobed)	20μS
Slew Rate	0.20 v/μS
STABILITY (Over Specified Temp. Range)	
Scale Factor	2ppm/°C F.S.R. (typ), 8ppm/°C (max)
Linearity	1ppm/°C F.S.R. (max)
Differential Linearity	1ppm/°C F.S.R. (max)
Linearity	±0.0115% max @ +125°C ±0.095% max @ −55°C
Differential Linearity	±0.0115% max @ +125°C ±0.095% max @ −55°C
Offset Drift	
Unipolar	1ppm/°C F.S.R.
Bipolar	5ppm/°C F.S.R.
POWER SUPPLY	
Requirements	+15V ±5% @ 15mA (max) −15V ±5% @ 25mA (max)
Rejection Ratio	0.001%/%
Power Dissipation	400mW (typ), 600mW (max)
TEMPERATURE RANGE	
Operating - B option	−55°C to +125°C
Operating - C option	0°C to +70°C
Storage	−65° to +150°C
MECHANICAL	
Case Style	28-pin hermetic double-DIP

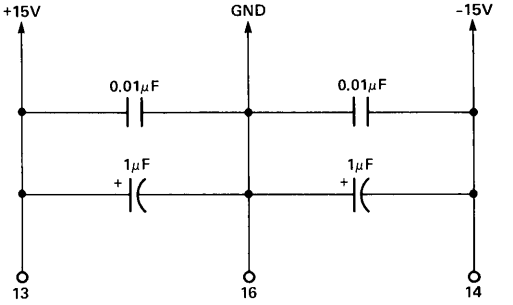
NOTES:

1. Digital Input voltage must not exceed supply voltage, or go below -0.5V. "0"<0.8 volts, "1">2.4 volts.
2. Time, data must be stable after Latch Control goes to "1".
3. Time, data must be stable after Latch Control goes to "0".
4. See APPLICATIONS INFORMATION for calibration procedure.
5. See APPLICATION NOTES.
6. Integral Linearity, for this product, is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input combination.
7. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.

CAUTION:
UNUSED INPUTS MUST BE GROUNDED!

APPLICATIONS INFORMATION

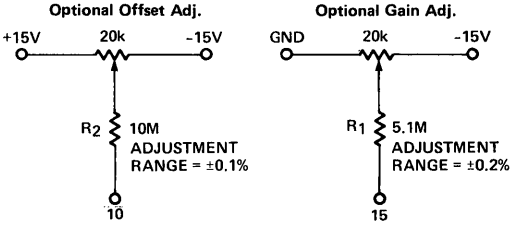
RECOMMENDED BYPASS CIRCUIT



PIN CONNECTIONS

1. UNIPOLAR OUTPUT: Ground pin 11
   BIPOLAR OUTPUT: Connect pin 11 to pin 10
2. Unused bit pins should be grounded. If bits 17 and 18 are not used, the latch control (pin 17) must be tied to either +5V or to +15V

OPTIONAL GAIN & OFFSET ADJUSTMENT CIRCUIT



Values of R_1 & R_2 can be changed to increase or decrease the sensitivity of the adjustment. This adjustment should not be greater than ±1% around the nominal value for best performance.

CALIBRATION PROCEDURE
(for optional external Gain & Offset adjustment

Unipolar operation:

1. Apply a 0 0 0 . . . 0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 1 1 1 . . . 1 input code and set the GAIN ADJ pot for F.S. -1 LSB.

Bipolar operation:

1. Apply a 100 . . . 0 input code and set the OFFSET ADJ pot for OV output
2. Apply a 000 . . . 0 input code and set the GAIN ADJ pot for -F.S.

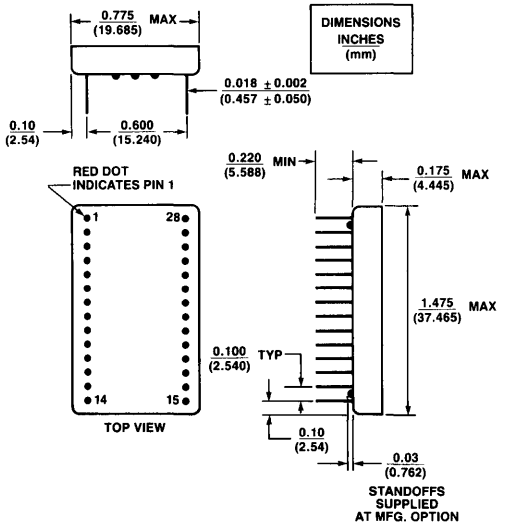
TRANSFER CHARACTERISTICS

Unipolar Operation

BINARY INPUT	ANALOG OUTPUT
1 1 1...1 1 1	+F.S. −1 LSB
1 0 0...0 0 0	+F.S./2
0 1 1...1 1 1	+F.S./2 −1 LSB
0 0 0...0 0 0	0V

Bipolar Operation

BINARY INPUT	ANALOG OUTPUT
1 1 1...1 1 1	+F.S. −1 LSB
1 0 0...0 0 0	0V
0 1 1...1 1 1	−1 LSB
0 0 0...0 0 0	−F.S.

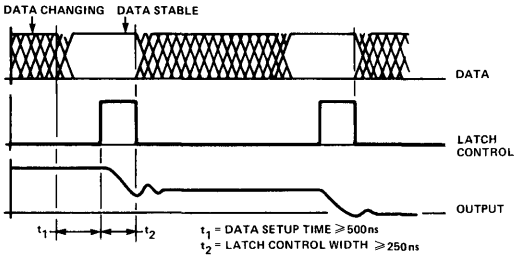


PIN	FUNCTION	PIN	FUNCTION
1	BIT 9	28	BIT 10
2	BIT 8	27	BIT 11
3	BIT 7	26	BIT 12
4	BIT 6	25	BIT 13
5	BIT 5	24	BIT 14
6	BIT 4	23	BIT 15
7	BIT 3	22	BIT 16
8	BIT 2	21	BIT 17
9	BIT 1, MSB	20	BIT 18, LSB
10	SUMMING JCT	19	2^{-1}-2^{-8} LATCH
11	BIPOLAR	18	2^{-9}-2^{-16} LATCH
12	OUTPUT	17	2^{-17}-2^{-18} LATCH
13	+15	16	GND
14	−15	15	GAIN ADJUST

TIMING DIAGRAM

LATCH CONTROL

Latch Strobe Input	Function
0	data latched (held)
1	data changing (transfer)



When loading the DAC from an 8-bit computer bus, optimum dynamic response will be obtained when the MSB segment is loaded first, followed by the LSB segments. This sequence allows the MSB's to settle while loading the LSB's.

Note that this loading sequence is necessary only when the processor cycle time is longer than the DAC settling time. If the processor cycle time is shorter than the DAC settling time, the bits may be loaded in any sequence.

APPLICATION NOTES

INTERNAL REFERENCE (NOTE 4)

Buffered bootstrap design of the reference voltage is totally internal. A temperature compensated -6.2 volt planar-zener diode minimizes temperature drift. The voltage can be monitored with a high impedance digital voltmeter at pin 15 (GAIN ADJUST).

OUTPUT NOISE

Noticeable amounts of noise at both low and high input levels can be prevented through output noise filtering. Care must be taken in choosing an output filter network that will not slow down the operating speed beyond what is desired.

ADDITIONAL RECOMMENDATIONS

1. For optimum performance, DAC377-18 should be allowed sufficient warmup time (5 min).
2. Due to the small bit weight (38μV), noise becomes a noticeable factor; if sockets are used, gold-plated ones are recommended to minimize contact resistance.
3. When changing output/gain range, a resistor (connected between pins 10 and 12) with a temperature coefficient between 0 and 10 ppm/°C is required to keep the DAC377-18 within guaranteed specifications.
4. Power supplies should come up before, or at the same time as the digital input supply.

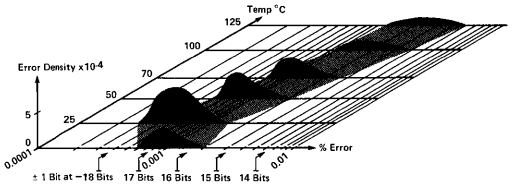
SETTLING TIME

The DAC377-18 incorporates input buffering circuits whose propagation time introduces a skewing of the digital data reaching the bit switches. The skewing results in the bit switches not operating synchronously with each data change, producing an increase in the settling time (1 to 2 microseconds) and large "glitches". The dynamic performance of the DAC377-18 can be greatly improved by using the internal latches which are available on these units. The latches are located after the input buffer circuits and just before the bit switches. When correctly strobed the latches present a data change to the bit switches in a synchronous manner. The latches should be closed while the input data is changing and propagating through the buffers. After the digital data has settled the latch is loaded and the "new" data is transfered to the switches snychronously. The latch is then closed and is ready for the next data update.

LINEARITY VS TEMPERATURE

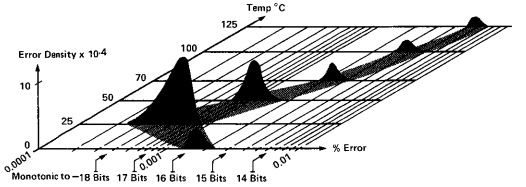
The plots below show the distribution of the maximum error of a unit in a typical lot of DAC377-18's.

INTEGRAL



Integral Linearity is a measurement of the deviation of the DAC377-18 transfer function from a straight line through the end points. It is expressed in the number of bits as well as the percent error.

DIFFERENTIAL



Differential Linearity is a measurement of the maximum deviation of any one LSB step change in the transfer function of the DAC377-18 from its ideal weight (38μV). It is expressed in terms of the number of bits as well as the percent error.

LONGTERM DRIFT

Long-term drift of the DAC's transfer function, after initial trim of offset and gain, is composed of several factors which are discussed below.

a. Offset Drift. For maximum performance, the offset should be zeroed after at least one hour of operation. Then the offset drift will be typically 2.5μV for the first 1000 hrs and 1μV per 1000 hrs thereafter.

b. Reference Voltage Drift. The intrinsic long-term drift of the breakdown voltage of the temperature compensated zener-diode in the reference voltage circuitry will cause a gain error at the output of the DAC. The drift that will occur is typically less than 1mV per year. A correction of this drift error can be made using the gain adjustment circuitry.

c. Output Amplifier Gain Change. Any noticeable gain change will be caused by a drift of the internal feedback resistor relative to the DAC's network impedance. This can contribute 10ppm F.S.R./1000 hrs, which can be corrected using the gain adjustment circuitry.

d. Linearity Drift. Due to the unique circuitry used in the DAC network, effects of resistor accuracy drift on linearity are greatly reduced. Typical differential linearity drift is less than 3ppm/1000 hrs.

IMPORTANT NOTICE TO THE USER: When measuring the stability of the DAC377-18, care should be taken so that the drift of the measurement instruments can be separated from the drift factors mentioned above, and the measurements are taken at identical temperatures.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the supply voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

ORDERING INFORMATION

MODEL	DESCRIPTION
DAC377B-18	18-Bit Complete DAC, MIL-STD-883 Screening
DAC377C-18	18-Bit Complete DAC, Commercial

Specifications subject to change without notice.

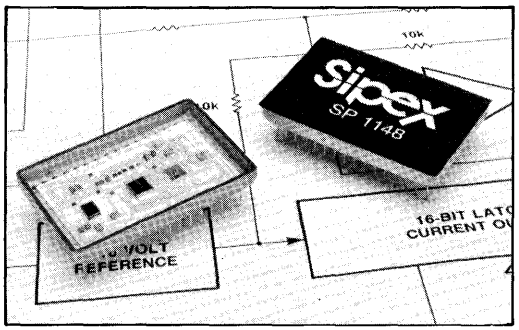
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP1148

16-Bit D/A Converter
μP Controlled Gain & Offset

FEATURES
- 16-Bit Linearity
- Low Power
- Software Programmable Gain and Offset
- On Chip Latches, Reference & Output Voltage Amplifier

APPLICATIONS
- Automatic Test Equipment
- Scientific Instrumentation
- Beam Positioners

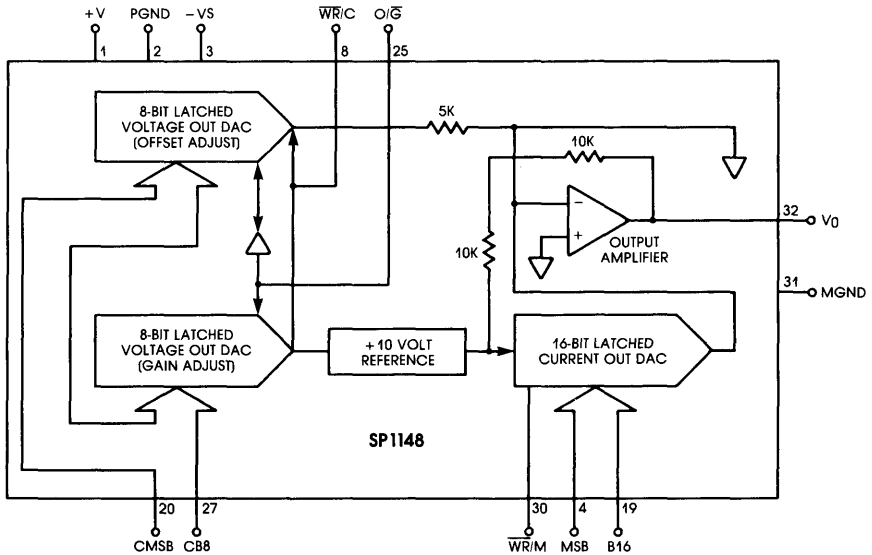


DESCRIPTION
The SP1148 is a 16-bit, latched input Digital to Analog converter. Two internal 8-bit latched input DAC's allow direct offset and gain adjustment via microprocessor interface. An 18-bit precision CMOS switch and a laser-trimmed thin-film resistor network are used to provide 16-bit accuracy and excellent temperature stability.

The correction DAC's inputs are separate from the main DAC's. The main (16-bit) DAC is loaded as a 16-bit word. The gain correction DAC's inputs are multiplexed with the offset DAC's 8-bit inputs. This allows for a separate 8-bit bus interface with the correction DAC's — common in applications such as automatic test equipment.

7

FUNCTIONAL DIAGRAM



OFFSET AND GAIN CALIBRATION

Initial offset and gain error can be adjusted to zero using the two internal 8-bit calibration DAC's. There are three control lines used in the calibration sequence: $\overline{WR}$/M is the write line for the MAIN (16-bit) DAC—the latches are transparent when the write line is low and latched when the write line goes high; $\overline{WR}$/C is the write line for the correction DAC's and operates the same as $\overline{WR}$/M; O/$\overline{G}$ selects between the offset correction DAC and the gain correction DAC—a high level on this pin selects the offset DAC and a low level selects the gain DAC. Offset and Gain calibrations are performed as follows:

1. With $\overline{WR}$/M low, set the digital inputs of the MAIN DAC to "000...00" (in unipolar mode) or "100...00" (in bipolar mode).
2. Set $\overline{WR}$/M high to latch the digital input into the Main DAC.
3. With $\overline{WR}$/C low and O/$\overline{G}$ high, adjust the digital inputs of the offset correction DAC until the Main DAC's output voltage (pin V_O) is as close to 0.000000 volts as possible. Note that incrementing the digital input produces a more negative voltage output.
4. Set $\overline{WR}$/C high to latch the digital input into the offset correction DAC.
5. With $\overline{WR}$/M low, set the digital input of the Main DAC to "111...11".
6. Set $\overline{WR}$/M high to latch the digital input into the Main DAC.
7. With $\overline{WR}$/C low and O/$\overline{G}$ low, adjust the digital inputs of the gain correction DAC until the Main DAC's output voltage (pin V_O) is as close as possible to the positive full-scale voltage shown below in Table 2. Note that incrementing the digital input produces a more negative voltage output.
8. Set $\overline{WR}$/C high to latch the digital input into the gain correction DAC.
9. Calibration is complete. Set $\overline{WR}$/M low and begin/resume normal digital-to-analog conversion via the Main DAC.

OUTPUT VOLTAGE RANGE	POSITIVE FULL-SCALE VOLTAGE
0 to +5 volts	+4.999924 volts
0 to +10 volts	+9.999847 volts
±5 volts	+4.999847 volts
±10 volts	+9.999695 volts

Table 2. Gain Calibration

GROUNDING AND GUARDING

The current from the measurement ground pin (MGND) is constant, independent of digital input, for ease of making measurements. This is the high quality ground for the SP1148. It should be connected to the high quality ground in the application. Power ground (PGND) should be connected to measurement ground (MGND) at the measurement point.

8-BIT MICROPROCESSOR INTERFACE

The SP1148 can easily be operated with an 8-bit bus by the addition of an octal latch. The 16-bit Main DAC is loaded from the 8-bit bus as two 8-bit bytes. Figure 2 shows the configuration when using a 74HC573 latch.

The eight most significant bits are latched into the 74HC573 by setting the "latch enable" control line low. The eight least significant bits are then placed on the bus. Now all sixteen bits can be simultaneously latched into the Main DAC by setting $\overline{WR}$/M high.

The offset and gain correction DAC's are calibrated as they were for 16-bit microprocessor applications. See the "OFFSET AND GAIN CALIBRATION" section of this data sheet.

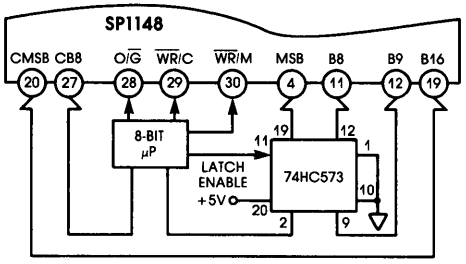


Figure 2. Connections For 8-Bit Bus Interface

AUTOMATIC TESTING OF 12-BIT ADC's AND DAC's

The SP1148 can be used as a reference DAC to automatically test the integral and differential linearity of 12-bit ADC's and DAC's. An ideal reference DAC should be an order of magnitude more accurate than the devices to be tested. The SP1148 is sixteen times more accurate than the devices to be tested and therefore can be considered ideal. The general test procedures for ADC's and DAC's are shown below. Before actual testing proceeds, calibrate the offset and gain of the SP1148 (see "OFFSET AND GAIN CALIBRATION" section of this data sheet).

ADC TESTING (refer to Figures 3 & 4)

The differential nonlinearity of ADC's is the difference between the actual code widths of the analog input vs. the ideal, one LSB code widths of a perfect converter. A code width is the range of analog input voltage which produces the desired digital output word.

A code width can be measured by determining the analog input voltage at which the transition occurs from the code under test to its next lower digital output code and then differencing that analog value with the same determined for the transition from the code undertest to its next higher digital output code.

Virtually all converters exhibit a degree of noise. This will necessitate an averaging technique to determine the analog input value for a code transition where a reduction in analog input voltage produces a majority of the lower digital code decisions and analog input increase produces a majority of the higher digital code decisions.

Begin testing by calibrating the offset and gain of the ADC under test per the manufacturer's instructions. Set the digital inputs of the reference DAC to the nominal value of the desired transition edge (produces an analog input to the device under test that is either ½ LSB below or ½ LSB above the ideal analog input for the code test). Increment or decrement this digital input until the Device Under Test (D.U.T.) outputs the digital code below the transition 50% of the time and the digital code above the transition 50% of the time. Record this digital input and repeat the procedure for the next transition of the nominal code to be measured. Compare this second digital input with the recorded input. The difference between these two digital values is the width of the code being measured. A perfect code width is 16 counts of the reference DAC. Each count more, or less than 16, corresponds to a differential linearity error of 1/16 LSB for the D.U.T. The arithmetic average of the two digital input values is the center of the code being tested. Each count of difference between this actual code center and the ideal, nominal code center represents an integral linearity error of 1/16 LSB.

SPECIFICATIONS

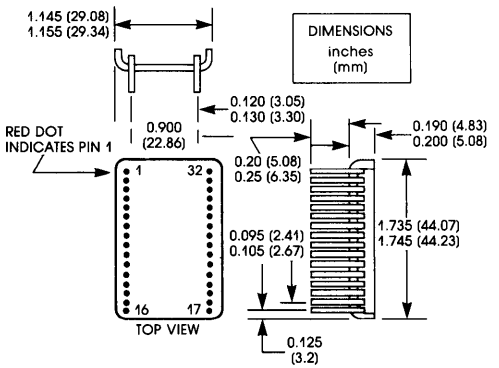
(Typical @25°C and rated supplies unless otherwise specified.)

MODEL	SP1148C	SP1148B
RESOLUTION	16-Bits	•
ACCURACY		
Integral Nonlinearity	±0.0076% FSR	•
Differential Nonlinearity	±0.00076% FSR	•
Monotonic (16-Bits)	Guaranteed	•
Offset	Adj. to Zero (±¼ LSB)	•
Gain	Adj. to Full Scale (±¼ LSB)	•
STABILITY		
Differential Nonlinearity	±1ppm/°C max	•
Bipolar Offset	±6ppm/°C max	•
Gain (Includes Int. Ref.)	±10ppm/°C max	•
DYNAMIC PERFORMANCE		
Settling Time to 0.00076%		
Voltage, Full-Scale Step	20µs	•
Voltage, LSB Step	3µs	•
DIGITAL INPUT CODES	(5 Volt CMOS/TTL)	•
Main DAC		
Unipolar	Binary (BIN)	•
Bipolar	Offset Binary (OBN)	•
Correction DAC's	Binary (BIN)	•
ANALOG OUTPUT		
Voltage	±10V	•
Noise (100kHz BW)	60µV rms	•
POWER REQUIREMENTS		
Voltage		
Rated Performance	±15V (±5%)	•
Operating	±12.5V to ±17V	•
Supply Current Drain	20mA max	•
Total Power @V_S = 15V	500mW max	•
POWER SUPPLY SENSITIVITY		
Offset	±10ppm/V	•
Gain	±10ppm/V	•
OFFSET ADJUSTMENT		
Range	±0.05% FSR	•
Resolution (@±10V)	¼ LSB	•
GAIN ADJUSTMENT		
Range		
Unipolar/Bipolar	±0.1%	•
Resolution		
Unipolar/Bipolar	½ LSB	•
TEMPERATURE RANGE		
Operating Temperature	0°C to +70°C	−55°C to +125°C
Storage Temperature	−40°C to +100°C	−65°C to +120°C

*Specifications same as SP1148C.

Specifications subject to change without notice.

PACKAGE OUTLINE



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	+V_S	9	B6	17	B14	25	CB6
2	PGND	10	B7	18	B15	26	CB7
3	−V_S	11	B8	19	B16	27	CB8
4	MSB	12	B9	20	CMSB	28	O/$\overline{G}$
5	B2	13	B10	21	CB2	29	$\overline{WR}$/C
6	B3	14	B11	22	CB3	30	$\overline{WR}$/M
7	B4	15	B12	23	CB4	31	MGND
8	B5	16	B13	24	CB5	32	Vo

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	SCREENING
SP1148C	0°C to 70°C	—
SP1148B	−55°C to +125°C	MIL-STD-883C

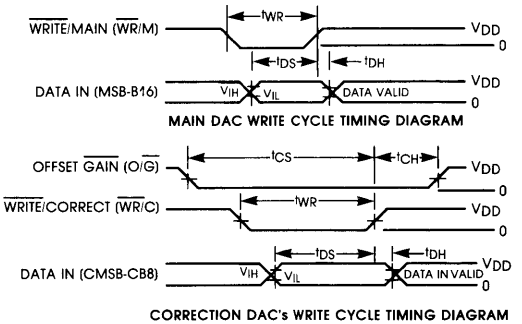
APPLICATIONS INFORMATION

TIMING DIAGRAM

The timing requirements for the SP1148 is shown in Table 1. The timing diagrams for the MAIN 16-bit DAC and the 8-bit Correction DAC's are shown in Figure 1. The three control lines operate as follows: $\overline{WR}$/M is the write line for the main DAC. The latches are transparent when the write line is low, and latched when the write line goes high. $\overline{WR}$/C is the write line for the correction DAC's. Operation is the same as above. O/$\overline{G}$ selects between the offset correction DAC and the gain correction DAC. A high level on this pin selects the offset DAC. A low level selects the gain DAC.

SYMBOL	PARAMETER	REQUIREMENT
Main DAC		
t_{DS}	Data Setup Time	140ns min
t_{DH}	Data Hold Time	120ns min
t_{WR}	Write Pulse Width	250ns min
Correction DAC's		
t_{CS}	O/$\overline{G}$ to Write Setup Time	200ns min
t_{CH}	O/$\overline{G}$ to Write Hold Time	20ns min
t_{DS}	Data Valid to Write Setup Time	110ns min
t_{DH}	Data Valid to Write Hold	0ns min
t_{WR}	Write Pulse Width	100ns min

Table 1. Timing Requirements



NOTES:
1. All input signal rise and fall times measured from 10% to 90% of V_{DD} x V_{DD} = +5V, $t_R = t_F$ = 20ns.
2. Timing measurement reference level is ($V_{IH} + V_{IL}$)/2.

Figure 1. SP1148 Timing Diagrams

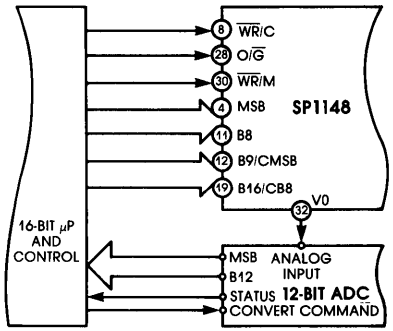


Figure 3. ADC Testing

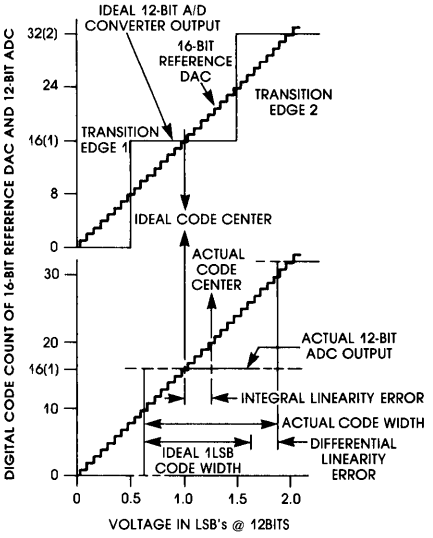


Figure 4. 12-Bit ADC Linearity Testing

DAC TESTING (refer to Figure 5)

To test 12-bit DAC's begin with offset and gain calibration of the DAC under test per the manufacturer's instructions. Set the digital inputs of the reference DAC and the D.U.T. to the desired code. Latch this digital input into the reference DAC. The DAC's outputs are differenced and amplified by an instrumentation amplifier. The voltage error between the DAC's is the integral linearity error. Now null the meter and then increment or decrement the digital input to the D.U.T. only, by one LSB. The meter reading will correspond to the code width of the new digital input word. The deviation of this voltage from the ideal value of one LSB is the differential linearity of the D.U.T.

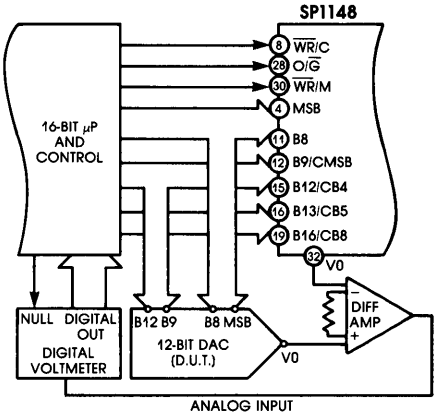


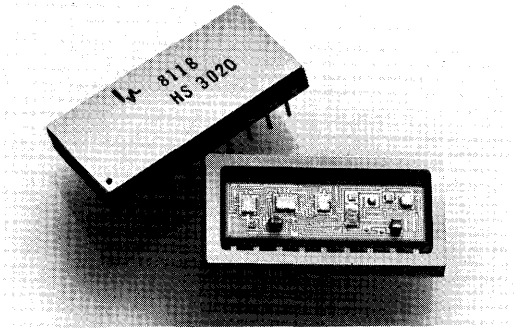
Figure 5. DAC Testing

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS 3020
8-Bit DAC with Input Registers

FEATURES

- ± 1/2 LSB Linearity
  ± 1 LSB Absolute Accuracy
- 4 Output Ranges
- Internal References and Output Amplifier
- Pin Compatible with MN 3020
- Input Register
- MIL-STD-883 Rev. C Processing Available



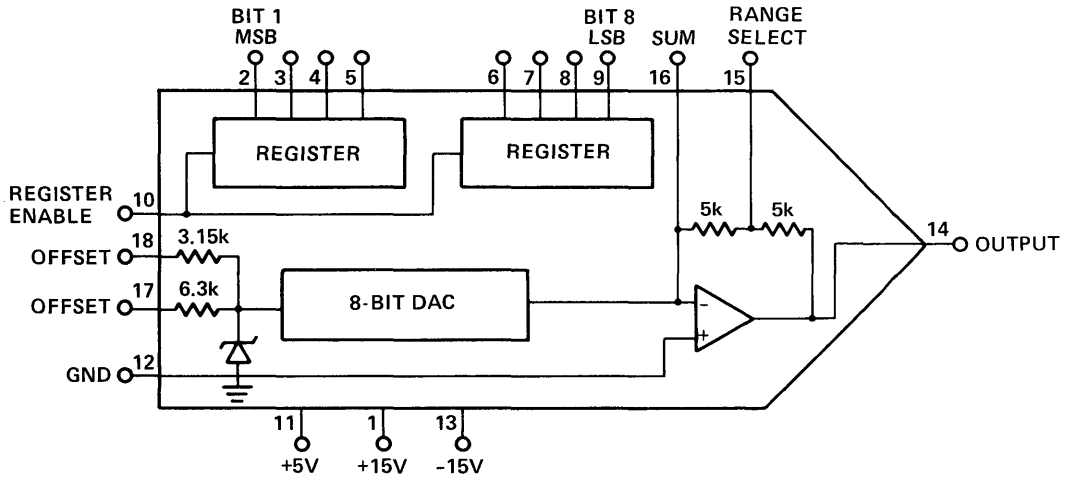
DESCRIPTION

The HS 3020 is an 8-Bit Digital-to-Analog Converter. It contains an internal reference, an input register and an output amplifier. It is packaged in a ceramic 18-pin DIP which is hermetically-sealed. The HS 3020's hybrid construction utilizes a precision network, a low drift reference, an input register and a fast settling output amplifier.

Hybrid Systems guarantees linearity and accuracy not only at room temperature but also at the extremes of the operating range of −55°C to +125°C.

7

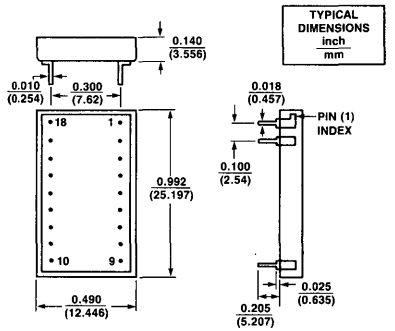
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C and nominal power supplies unless otherwise noted)

MODEL	HS 3020
TYPE	D/A Converter
DIGITAL INPUT	
Resolution	8 Bits
Coding	Straight Binary/Offset Binary
Logic Levels (Data Inputs)	
Logic "1" (at 30μA)	+2V min, +5.5V max
Logic "0" (at -.6mA)	-0.5V D.C. min, +0.7V max
Register Enable Logic	
Logic "1" (at 40μA)	+2V min, +5.5V max
Logic "0" (at -.8mA)	-0.5V min, +0.7V max
Pulse Width	60nSec min
Setup Time	40nSec min
ACCURACY	
Linearity Error	
0°C to +70°C	±1/4 LSB typ ±1/2 LSB max
-55°C to +125°C	±1/2 LSB max
Monotonicity	Guaranteed Over Temperature
Absolute Accuracy Error	
0°C to +70°C	±1/2 LSB typ ±1 LSB max
-55°C to +125°C	±1 LSB max
Unipolar Offset Error	
-55°C to +125°C	±1 LSB max
Bipolar Offset Error	
-55°C to +125°C	±1 LSB max
Offset Drift[1]	
Unipolar + Range	±2ppm of F.S.R./°C typ
Unipolar - Range	±10ppm of F.S.R./°C typ
Bipola Ranges	±10ppm of F.S.R./°C typ
Gain Drift[1]	±15ppm/°C typ
CONVERSION SPEED	
Settling Time (10V change to ±1/2 LSB)	3.0μs max
Output Slew Rate	20V/μs typ
ANALOG OUTPUTS	
Output Impedance	0.05Ω typ
Output Current	±5mA min
Short Circuit Duration	Indefinite to Common
POWER SUPPLIES	
Power Supply Range	
+15V	+14V to +18V
-15V	-14V to -18V
+5V	+4.75V to +5.25V
Power Supply Rejection	
+15V	±0.03% F.S.R./%Vs
-15V	±0.01% F.S.R./%Vs
Current Drain (Output Unloaded)	
+15V	20mA max
-15V	-13mA max
+5V	37mA max
Power Consumption	680mW
Package Outline	



Pin 1 is marked by a dot on the top of the package.

NOTE

1. Over specified operating temperature range

PIN DESIGNATIONS

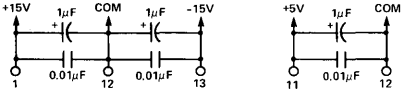
PIN	FUNCTION	PIN	FUNCTION
1	+15V	18	Unipolar Offset
2	Bit 1 (MSB)	17	Bipolar Offset
3	Bit 2	16	Summing Junction
4	Bit 3	15	Range Select
5	Bit 4	14	Analog Output
6	Bit 5	13	-15V
7	Bit 6	12	Ground
8	Bit 7	11	+5V Supply
9	Bit 8	10	Register Enable

OUTPUT RANGE CONNECTIONS

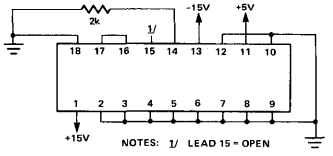
DIGITAL INPUT	ANALOG OUTPUT (DC VOLTS)			
	UNIPOLAR	UNIPOLAR	BIPOLAR	BIPOLAR
MSB LSB	POSITIVE	NEGATIVE	±5	±10
00000000	0.000	-9.961	-5.000	-10.000
00000001	+0.039	-9.922	-4.961	- 9.922
01111111	+4.961	-5.000	-0.039	- 0.078
10000000	+5.000	-4.961	-0.000	0.000
11111110	+9.922	-0.039	+4.922	+ 9.844
11111111	+9.961	0.000	+4.961	+ 9.922
CONNECT	14 to 15	14 to 15	14 to 15	
PIN TO PIN	17 to GND	16 to 18	16 to 17	16 to 17
	18 to GND	17 to GND	18 to GND	18 to GND

APPLICATIONS INFORMATION

RECOMMENDED POWER SUPPLY BY-PASS CIRCUIT



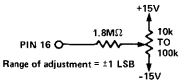
BURN-IN AND LIFE TEST CIRCUIT



OPTIONAL OFFSET ADJUSTMENT

A constant offset voltage can be added to or subtracted from the output of the HS 3020 for the purpose of increasing accuracy at and around a particular output level.

Connect the offset potentiometer as shown; apply the desired input code, adjust the offset potentiometer until the desired output level is achieved.



REGISTER ENABLE

When the Register Enable (Pin 10) is high (hold mode) the digital data in the input register will be latched, and when the Register Enable is low (track mode), the converter's output will follow its input. In order to latch new digital data into the register, the Register Enable must go low for a minimum of 60nSec and digital input data must be valid for a minimum of 40 nSec prior to Register Enable going high again.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 3020B	MIL, 8 BIT D/A, -55° to +125°C
HS 3020C	COMM, 8 BIT D/A, 0° to +70°C

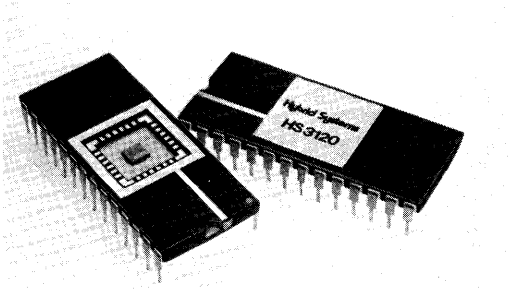
Specifications subject to change without notice.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS 3120
Double Buffered 12-Bit MDAC

FEATURES

- **Monolithic Construction**
- **12 Bit Resolution**
- **0.01% Non-Linearity**
- **μP Compatible**
- **4-Quadrant Multiplication**
- **Latch-up Protected**



DESCRIPTION

The HS 3120 is a precision monolithic 12-bit multiplying DAC with internal two-stage input storage registers for easy interfacing with microprocessor busses. It is packaged in a 28-pin DIP to give high I/O design flexibility.

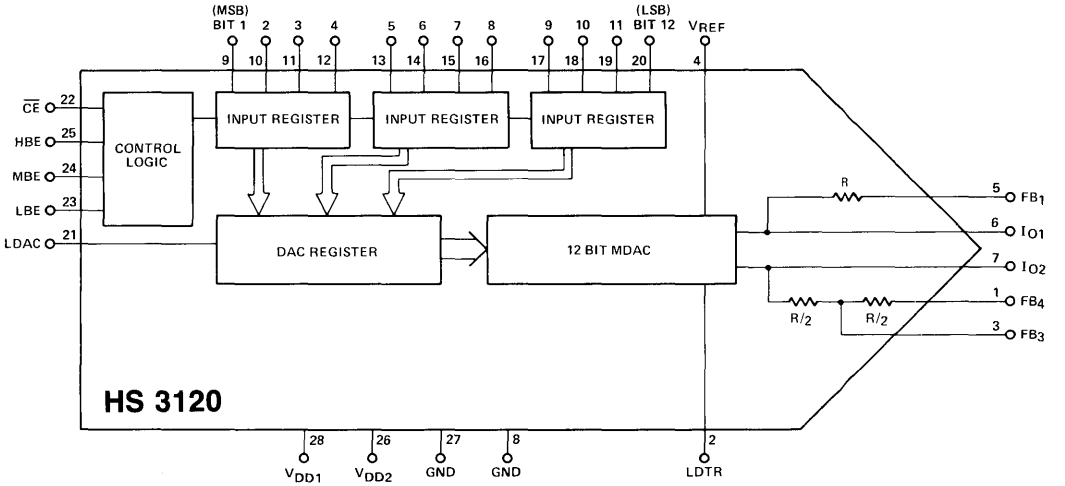
DOUBLE BUFFERED – The input registers are sectioned into 3 segments of 4 bits each, all individually addressable. The DAC-register, following the input registers, is a parallel 12-bit register for holding the DAC data while the input registers are updated. Only the data held in the DAC register determines the analog output value of the converter.

MICRO PROCESSOR COMPATIBLE – The HS 3120 has been designed for great flexibility in connecting to bus-oriented systems. The 12 data inputs are organized into 3 independent addressable 4-bit input registers such that the HS 3120 can be connected to either a 4, 8 or 16-bit data bus. The control logic of the HS 3120 includes chip enable and latch enable inputs for flexible memory mapping. All controls are level-triggered to allow static or dynamic operation.

VERSATILE OUTPUTS – A total of 5 output lines are provided by the HS 3120 to allow unipolar and bipolar output connection with a minimum of external components. The feedback resistor is internal. The resistor ladder network termination is externally available, thus eliminating an external resistor for the 1 LSB offset in bipolar mode.

MONOLITHIC CMOS CONSTRUCTION – The HS 3120 is a one-chip CMOS circuit with a resistor ladder network designed for 0.01% linearity without laser trimming. Small chip size and high manufacturing yields result in greatly reduced cost.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

(Typical @ 25°C, nominal power supply, V_{REF} = +10V, unipolar unless otherwise noted).

MODEL	HS 3120-2	HS 3120-0
TYPE	**MULTIPLYING, DOUBLE BUFFERED INPUTS**	*
DIGITAL INPUT		
Resolution	12-Bits	*
2-Quad. Unipolar Coding	Binary[1], Comp. Binary[1]	*
4-Quad. Bipolar Coding	Offset Binary	*
Logic Compatibility[2]	CMOS, TTL	*
Input Current	±1 μA (max)	*
Data Set-up Time[3]	250nS (min)	*
Strobe Width[3]	250nS (min)	*
Data Hold Time[3]	0nS (min)	*
REFERENCE INPUT		
Voltage Range	±25V (max)	*
Input Impedance	8kΩ ±50%	*
ANALOG OUTPUT		
Scale Factor	125μA/V_{Ref} ±50%	*
Scale Factor Accuracy[4]	±0.4%	*
Output Leakage[5]		
@ 25°C	<10nA (max)	*
@ 125°C	<200nA (max)	*
Output Capacitance		
$C_{OUT\ 1}$, all inputs high	80pF	*
$C_{OUT\ 1}$, all inputs low	40pF	*
$C_{OUT\ 2}$, all inputs high	40pF	*
$C_{OUT\ 2}$, all inputs low	80pF	*
STATIC PERFORMANCE		
Integral Linearity	±0.015% F.S.R. (max)	±0.05 % F.S.R. (max)
Differential Linearity	±0.024% F.S.R. (max)	±0.097% F.S.R. (max)
Monotonicity	Guaranteed to 12 bits	Guaranteed to 10 bits
Monotonicity Temp. Range		
C-Models	0°C to +70°C	*
B-Models	-55°C to +125°C	*
DYNAMIC PERFORMANCE		
Digital Small Signal Settling	1.0μsec	*
Full Scale Transition Settling to 0.01% (strobed)	2.0μsec	*
Reference Feedthrough Error (V_{Ref} = 20V_{pp})		
@ 1kHz	<1mV	*
@ 10kHz	2mV	*
Delay to output		
from Bits input	100nS[6]	*
from $\overline{LDAC}$	200nS[6]	*
from $\overline{CE}$	120nS[6]	*
STABILITY (Over Specified Temp. Range)		
Scale Factor[4]	2 ppm F.S.R./°C (max)	*
Integral Linearity	0.2 ppm F.S.R./°C (max)	*
Differential Linearity	0.2 ppm F.S.R./°C (max)	*
Monotonicity Temp. Range		
C-Option	0°C to +70°C	*
B-Option	-55°C to +125°C	*
POWER SUPPLY (V_{DD})		
Operating Voltage (specifications guaranteed)	+15V ±5%	*
Maximum Voltage Range	+5V to 16V	*
Current	2.5mA (max)	*
Rejection Ratio	0.002%/% (max)	*
TEMPERATURE RANGE		
Operating C-Option	0°C to +70°C	*
Operating B-Option	-55°C to +125°C	*
Storage	-65°C to +150°C	*
MECHANICAL		
Case Style	28-pin double DIP	*
C-Option	plastic or ceramic	*
B-Option	ceramic	*

NOTES:

* Same as HS 3120-2

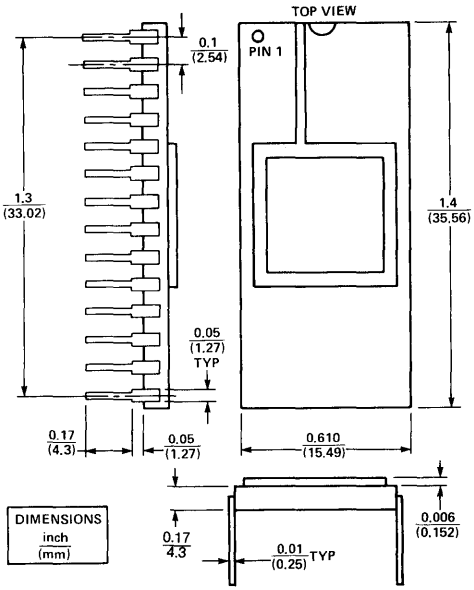
1. The input coding is complementary binary if I_{O2} is used.
2. Digital input voltage must not exceed supply voltage or go below -0.5V. "0" <0.8V, 2.4V < "1" ≤V_{DD}.
3. All strobes are level triggered. See TIMING DIAGRAM.
4. Using the internal feedback resistor and an external opamp.
5. The output leakage current will create an offset voltage at the external opamps output. It doubles every 10°C temperature increase.
6. Delay times are twice the amount shown at T_A = +125°C

PIN ASSIGNMENTS

PIN	FUNCTION
1	FB_4, Feedback Bipolar Operation
2	LDTR, Ladder Termination
3	FB_3, Feedback Bipolar Operation
4	V_{REF}, Reference Voltage Input
5	FB_1, Feedback, Unipolar/Bipolar
6	I_{O1}, Current out into virtual ground
7	I_{O2}, Current out-complement of I_{O1}
8	V_{SS}, Ground, Analog and DAC Register
9	Bit 1, MSB
10	Bit 2
11	Bit 3
12	Bit 4
13	Bit 5
14	Bit 6
15	Bit 7
16	Bit 8
17	Bit 9
18	Bit 10
19	Bit 11
20	Bit 12
21	LDAC, Transfers data from input to DAC register
22	$\overline{CE}$, Chip Enable, active low
23	LBE, Bit 12 to Bit 9 Enable
24	MBE, Bit 8 to Bit 5 Enable
25	HBE, Bit 4 to Bit 1 Enable
26	V_{DD2}, Supply Analog and DAC Register
27	V_{SS1}, Ground input latches
28	V_{DD1}, Supply input latches

NOTE: Pins 8 and 27 and pins 26 and 28 must be connected externally.

MECHANICAL



CONNECTIONS

Unipolar Operation: Connect I_{O1} and FB_1 as shown in diagram. Tie I_{O2} (Pin 7), FB_3 (Pin 3), FB_4, (Pin 1) all to Ground (Pin 8)

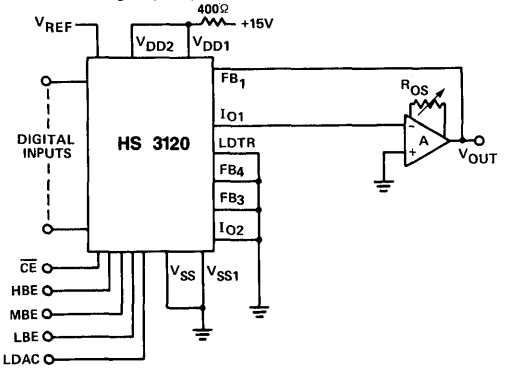
Bipolar Operation: Connect I_{O1}, I_{O2}, FB_1, FB_3, FB_4 as shown in diagram. Tie LDTR to I_{O2}

Grounding: Connect all GRD to system analog ground and tie this to digital ground.

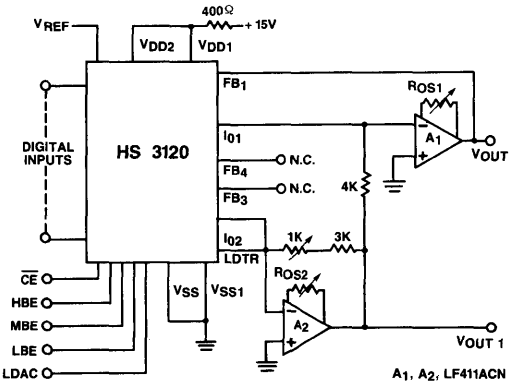
NOTE: All unused input pins must be grounded.

APPLICATIONS INFORMATION

Connection Diagram, Unipolar Operation



Connection Diagram, Bipolar Operation



Connection Diagram, Bipolar Operation (for applications where *bipolar offset temperature drift* (≈ 10 ppm/°C) is not critical)

NOTE: To maintain specified linearity, external amplifiers must be zeroed. This is best done with V_{REF} set to zero and,
Unipolar: load the DAC register with all bits at zero and adjust R_{OS} for V_{OUT} = OV

Bipolar: load the DAC register with 10 . . .0 (MSB =1) and set R_{OS2} for $V_{OUT\,1}$ = OV. Then set R_{OS1} for

TRANSFER FUNCTION (N=12)

BINARY INPUT	UNIPOLAR OUTPUT	BIPOLAR OUTPUT
111 . . . 111	$-V_{REF}\,(1 - 2^{-N})$	$-V_{REF}\,(1 - 2^{-(N-1)})$
100 . . . 001	$-V_{REF}\,(1/2 + 2^{-N})$	$-V_{REF}\,(2^{-(N-1)})$
100 . . . 000	$\frac{-V_{REF}}{2}$	0
011 . . . 111	$-V_{REF}\,(1/2 - 2^{-N})$	$V_{REF}\,(2^{-(N-1)})$
000 . . . 000	0	V_{REF}

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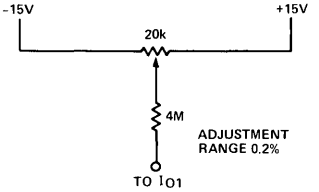
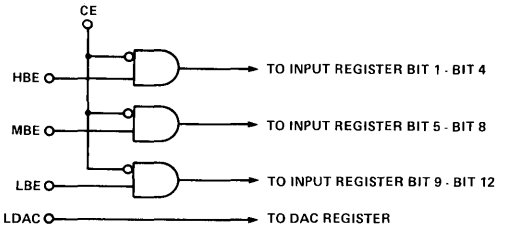
BIPOLAR OFFSET ADJUST (external)



NOTE: External opamps have to be zeroed before the bipolar offset adjust circuit is connected.

CONTROL LOGIC

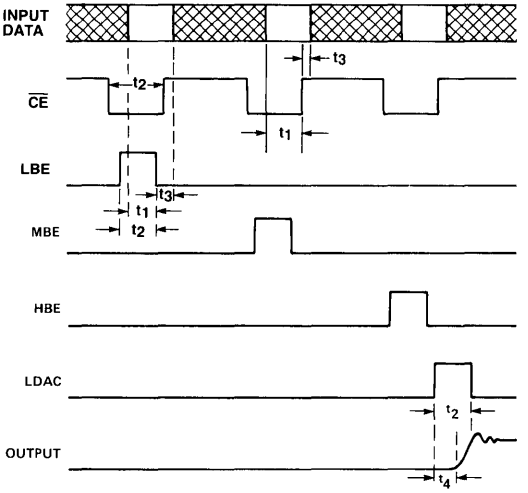


NOTE: The transfer from input register to DAC register can be performed without Enabling Chip.

STROBE LOGIC

Strobe	Function
0	data latched (held)
1	data changing (transfer)

TIMING DIAGRAM



TIME AXIS NOT TO SCALE. ALL STROBES ARE LEVEL TRIGGERED.

t_1: Data Setup Time. Time data must be stable before strobe (byte enable/LDAC) goes to "0", t_1 (min) = 250 nsec.

t_2: Strobe Width. t_2 (min) = 250 nsec. (CE, LBE, MBE, HBE, LDAC).

t_3: Hold Time. Time data must be stable after strobe goes to "0", t_3 = 0 nsec.

t_4: Delay from LDAC to Output. t_4 = 200 nsec.

NOTE: Minimum common active time for $\overline{CE}$ and any byte enable is 250 nsec.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 3120C-0	Double Buffered 12-Bit MDAC, Commercial
HS 3120C-2	Double Buffered 12-Bit MDAC, Commercial
HS 3120B-0	Double Buffered 12-Bit MDAC, MIL-STD-883C
HS 3120B-2	Double Buffered 12-Bit MDAC, MIL-STD-883C

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the supply voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

Specifications subject to change without notice.

1990

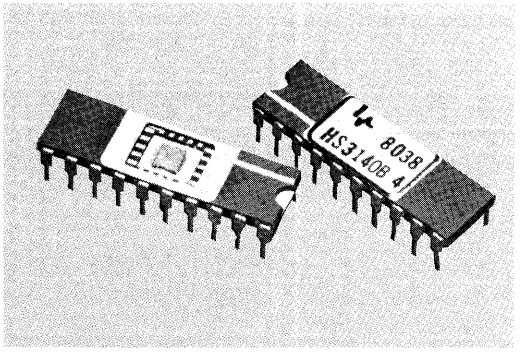
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS3140

MONOLITHIC 14-BIT MDAC

FEATURES

- Monolithic CMOS circuit
- On-chip resistors
- Linearity ±0.004%
- Monotonic over temperature
- Latch-up protected
- Small size, 20 pin DIP
- Pin compatible to DAC-HA14B
- Commercial and MIL-STD-883 processing



DESCRIPTION

The HS3140 is a 14-bit CMOS multiplying D/A converter integrated in a single monolithic chip. It represents a major advance in the field of monolithic converter technology, extending resolution and linearity to 14 bits and 0.003%. The HS3140 accepts AC or DC reference voltages, multiplies in all four quadrants, has latch-up protection, and is packaged in a hermetic 20 pin DIP. Outstanding features of the HS3140 include:

14-Bit Performance — HS3140 offers a 0.003% integral linearity and a 0.003% differential linearity and is monotonic over the entire specified operating temperature range. The excellent differential linearity is achieved by using a unique bit decoding technique. The transfer function is actually divided into 16 segments (determined by bits 1 to 4), each consisting of 1024 discrete voltage levels (determined by bits 5 to 14). Bits 1 to 4 are digitally decoded into 15 control signals, driving 15 equal current sources, rather than 4 binarily weighted sources; thus, reducing the matching accuracy requirement on the resistors and CMOS switches.

Monolithic Construction — HS3140 is a single chip CMOS circuit using advanced design and manufacturing techniques. It is the industry's first monolithic digital-to-analog converter offering 14-bit resolution and a linearity of 0.003%.

Processing — The HS3140 is offered in two versions. The -C version is commercially processed for applications in the 0°C to 70°C range. The -B version operates in the −55°C to +125°C temperature range and is processed and screened to the requirements of MIL-M-38510 and MIL-STD-883C.

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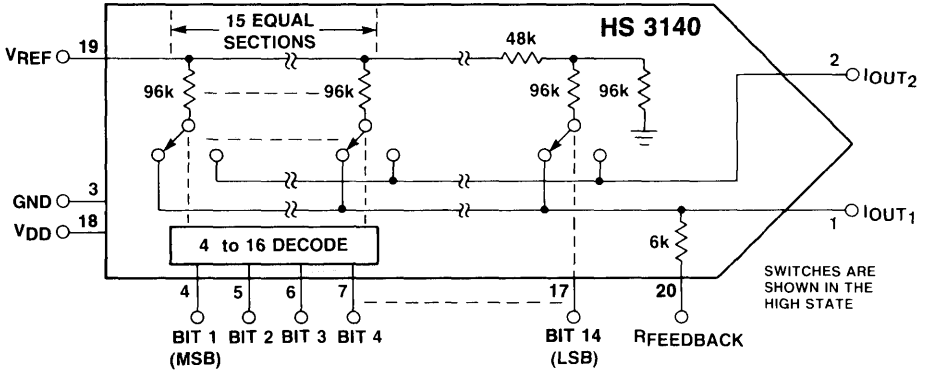
FUNCTIONAL DIAGRAM



SPECIFICATIONS

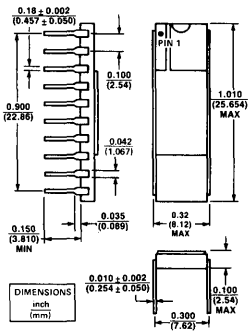
(Typical @ +25°C, nominal power supply, V_{REF} = +10V, unipolar unless otherwise noted)

MODEL	HS 3140
TYPE	**4 QUADRANT MULTIPLYING**
DIGITAL INPUTS	
Resolution	14-Bits
2-Quad. Unipolar Coding	Binary
4-Quad. Bipolar Coding	Offset Binary
Logic Compatibility[1]	CMOS, TTL
Input Current	<1μA
REFERENCE INPUT[2]	
Voltage Range	±25V (max), AC or DC
Input Impedance	6.5kΩ ± 50%
ANALOG OUTPUT	
Scale Factor	150μA/V_{REF} ± 50%
Scale Factor Accuracy [3, 4]	±1% max
Output Leakage	
@ +25°C	10nA (max)
@ +125°C	200nA (max)
Output Capacitance	
C_{out} 1, all inputs high	100 pF
C_{out} 1, all inputs low	50 pF
C_{out} 2, all inputs high	50 pF
C_{out} 2, all inputs low	100 pF
STATIC PERFORMANCE	
Integral Linearity [5]	
HS 3140-3	±0.007% F.S.R. (typ)
	±0.012% F.S.R. (max)
HS 3140-4	±0.003% F.S.R. (typ)
	±0.006% F.S.R. (max)
Differential Linearity[6]	
HS 3140-3	±0.006% F.S.R. (typ)
	±0.012% F.S.R. (max)
HS 3140-4	±0.003% F.S.R. (typ)
	±0.006% F.S.R. (max)
Monotonicity	
HS 3140-3	Guaranteed to 13-Bits
HS 3140-4	Guaranteed to 14-Bits
DYNAMIC PERFORMANCE	
Digital Small Signal Settling	1μS
Digital Full Scale	
Transition Settling	2μS
Reference Feedthrough	
Error (V_{REF} = 20V_{PP})	
@ 1kHz	200μV
@ 10kHz	2mV
STABILITY (Over specified Temp. Range)	
Scale Factor[3]	4ppm/°C (typ)
Integral Linearity	0.5ppm F.S.R./°C (typ)
	1ppm F.S.R./°C (max)
Differential Linearity	0.5ppm F.S.R./°C (typ)
	1ppm F.S.R./°C (max)
Monotonicity Temp. Range	
HS 3140C-3/-4	0°C to +70°C
HS 3140B-3/-4	−25°C to +85°C
POWER SUPPLY (V_{DD})[7]	
Nominal Voltage	+15V ±5%
Maximum Voltage Range	+11V to +18V
Current	2mA
Rejection Ratio	.005%/%
TEMPERATURE RANGE	
Operating HS 3140C-3/-4	0°C to +70°C
Operating HS 3140B-3/-4	−55°C to +125°C
Storage	−65°C to +150°C
MECHANICAL	
Case Style	20 pin DIP, ceramic

NOTES

1. -0.5V< "0" < +0.8V, 2.4V < "1" ≤ V_{DD}, Worst Case.
2. We recommend our HS REF 01 or R675B-1 for fixed reference application.
3. Using the internal feedback resistor and an external Opamp.
4. The Scale Factor can be adjusted externally by variable resistors in series with the reference input and/or in series to the internal feedback resistor (See APPLICATIONS INFORMATION).
5. Integral Linearity is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input combination.
6. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
7. A 400Ω resistor should be added in series with V_{DD} and by-passed by a 0.1μf capacitor.

Case Dimensions

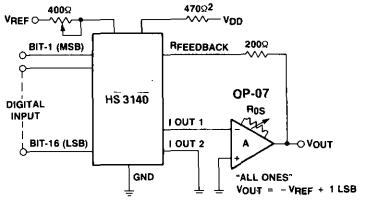


Pin Assignments

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT 1, $I_{OUT\,1}$	20	R FEEDBACK
2	OUTPUT 2, $I_{OUT\,2}$	19	V_{REF}
3	GND	18	$+V_{DD}$
4	BIT 1 (MSB)	17	BIT 14
5	BIT 2	16	BIT 13
6	BIT 3	15	BIT 12
7	BIT 4	14	BIT 11
8	BIT 5	13	BIT 10
9	BIT 6	12	BIT 9
10	BIT 7	11	BIT 8

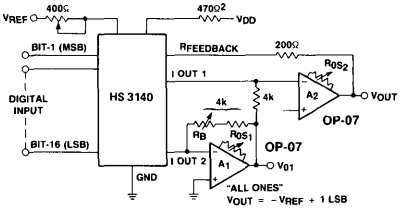
APPLICATIONS INFORMATION

UNIPOLAR OPERATION (2-Quadrant Multiplication)



NOTES:
1. To maintain specified HS 3140 linearity, the external amplifier (A) must be zeroed.
   Apply an ALL "ZEROS" digital input and adjust R_{OS} for V_{OUT} = 0 ±1mV.
2. Series resistor recommended to limit current during 'turn-on'.

BIPOLAR OPERATION (4-Quadrant Multiplication)



NOTES:
1. To maintain specified HS 3140 linearity, external amplifiers (A_1 and A_2) must be zeroed. With a digital input of 10...0 and V_{REF} set to zero:
   a) Set R_{OS1} for V_{01} = 0
   b) Set R_{OS2} for V_{OUT} = 0
   c) Set V_{REF} to +10V and adjust R_B for V_{OUT} to be 0 Volts
2. Series resistor recommended to limit current during 'turn-on'.

UNIPOLAR OPERATION
Transfer Characteristics

BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-N})$
100...001	$-V_{REF}(1/2+2^{-N})$
100...000	$-V_{REF}/2$
011...111	$-V_{REF}(1/2-2^{-N})$
000...001	$-V_{REF}(2^{-N})$
000...000	0

BIPOLAR OPERATION
Transfer Characteristics

OFFSET BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-(N-1)})$
100...001	$-V_{REF}(2^{-(N-1)})$
100...000	0
011...001	$V_{REF}(2^{-(N-1)})$
000...001	$V_{REF}(1-2^{-(N-1)})$
000...000	V_{REF}

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 3140C-3	14-Bit MDAC, 0.006% Lin. Commercial
HS 3140C-4	14-Bit MDAC, 0.003% Lin. Commercial
HS 3140B-3	14-Bit MDAC, 0.006% Lin. MIL-STD-883C
HS 3140B-4	14-Bit MDAC, 0.003% Lin. MIL-STD-883C

Specifications subject to change without notice.

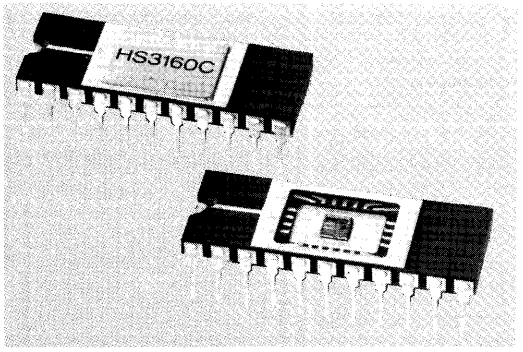
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS3160

MONOLITHIC 16-BIT MDAC

FEATURES

- Monolithic CMOS circuit
- Linearity ±0.003%
- Linearity TC 1.0ppm/°C max
- Latch-up protected
- Small size: 22 pin ceramic DIP
- Commercial and MIL-STD-883 Rev. C processing
- Single power supply: +15VDC
- Low power: 30mW



DESCRIPTION

The HS3160 is a 16-bit CMOS multiplying D/A converter integrated in a single monolithic chip. It represents a major advance in the field of monolithic converter technology, extending resolution to 16 bits and with linearity to 14 bits and 0.003%. The HS3160 accepts AC or DC reference voltages, multiplies in all four quadrants, has latch-up protection, and is packaged in a hermetic 22 pin DIP. Outstanding features of the HS3160 include:

14-Bit Linearity — HS3160 offers a 0.003% integral linearity and a 0.003% differential linearity and is monotonic over the entire specified operating temperature range. The excellent differential linearity is achieved by using a unique bit decoding technique. The transfer function is actually divided into 16 segments (determined by bits 1 to 4), each consisting of 4096 discrete voltage levels (determined by bits 5 to 16). Bits 1 to 4 are digitally decoded into 15 control signals, driving 15 equal current sources, rather than 4 binarily weighted sources; thus, reducing the matching accuracy requirement on the resistors and CMOS switches.

Monolithic Construction — HS3160 is a single chip CMOS circuit using advanced design and manufacturing techniques.

Processing — The HS3160 is offered in two versions. The -C version is commercially processed for applications in the 0°C to 70°C range. The -B version operates in the −55°C to +125°C temperature range and is processed and screened to the requirements of MIL-M-38510 and MIL-STD-883C.

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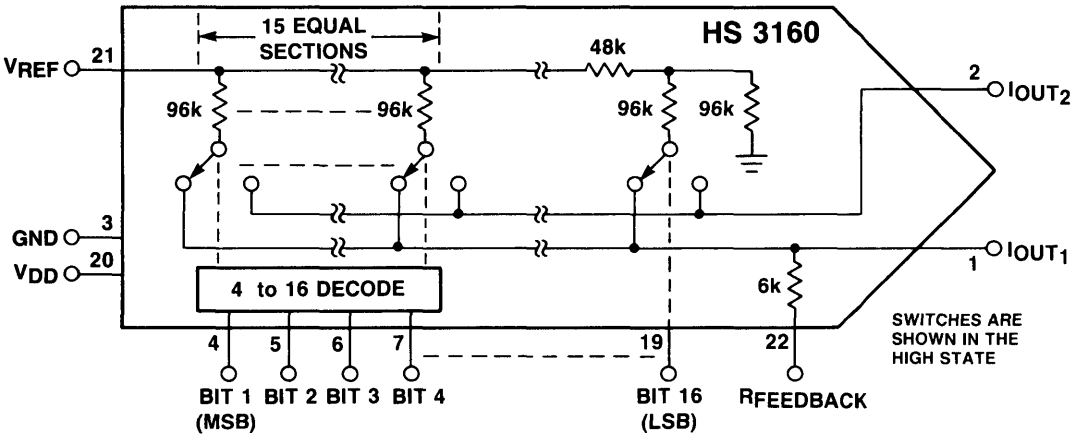
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C, nominal power supply, V_{REF} = +10V, unipolar unless otherwise noted)

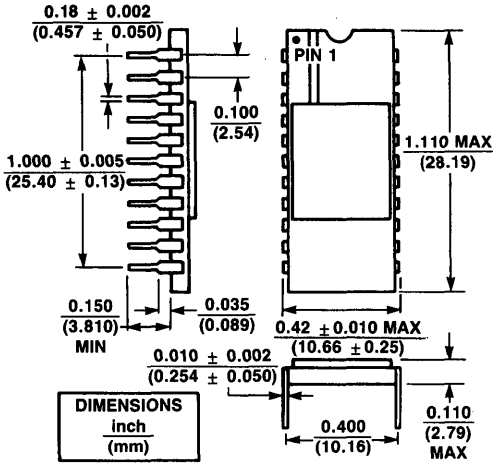
MODEL	HS 3160
TYPE	4 Quadrant Multiplying
DIGITAL INPUTS	
Resolution	16-Bits
2-Quad. Unipolar Coding	Binary
4-Quad. Bipolar Coding	Offset Binary
Logic Compatibility[1]	CMOS, TTL
Input Current	<1μA
REFERENCE INPUT[2]	
Voltage Range	±25V (max), AC or DC
Input Impedance	6.5kΩ ± 50%
ANALOG OUTPUT[7]	
Scale Factor	150μA/V_{REF} ± 50%
Scale Factor Accuracy[3,4]	±1% (max)
Output Leakage	
@ +25°C	10nA (max)
@ +125°C	200nA (max)
Output Capacitance	
C_{out} 1, all inputs high	100 pF
C_{out} 1, all inputs low	50 pF
C_{out} 2, all inputs high	50 pF
C_{out} 2, all inputs low	100 pF
STATIC PERFORMANCE	
Integral Linearity[5]	
HS 3160-3	±0.006% F.S.R. (typ)
	±0.012% F.S.R. (max)
HS 3160-4	±0.003% F.S.R. (typ)
	±0.006% F.S.R. (max)
Differential Linearity[6]	
HS 3160-3	±0.006% F.S.R. (typ)
	±0.012% F.S.R. (max)
HS 3160-4	±0.003% F.S.R. (typ)
	±0.006% F.S.R. (max)
Monotonicity	
HS 3160-3	Guaranteed to 13-Bits
HS 3160-4	Guaranteed to 14-Bits
DYNAMIC PERFORMANCE	
Digital Small Signal Settling	1μS
Digital Full Scale	
Transition Settling	2μS
Reference Feedthrough Error	
(V_{REF} = 20Vpp)	
@ 1kHz	200μV
@ 10kHz	2mV
Reference Input Bandwidth	1MHz
STABILITY (Over specified temp. range)	
Scale Factor[3]	4ppm/°C (typ)
Integral Linearity	0.5ppm F.S.R./°C (typ)
	1ppm F.S.R./°C (max)
Differential Linearity	0.5ppm F.S.R./°C (typ)
	1ppm F.S.R./°C (max)
Monotonicity Temp. Range	
HS 3160C-3/-4	0°C to +70°C
HS 3160B-3/-4	−25°C to +85°C
POWER SUPPLY (V_{DD})[8]	
Nominal Voltage	+15V ±5%
Voltage Range	+8V to +18V
Current	2mA
Rejection Ratio	0.005% F.S.R./%V
TEMPERATURE RANGE	
Operating HS 3160C-3/-4	0°C to +70°C
Operating HS 3160B-3/-4	−55°C to +125°C
Storage	−65°C to +150°C
MECHANICAL	
Case Style	22 pin DIP, ceramic

NOTES

1. −0.5V < "0" < +0.8V, 2.4V < "1" ≤ V_{DD}, Worst Case.
2. We recommend our HS REF 01 or R675B-1 for fixed reference application.
3. Using the internal feedback resistor and an external Opamp.
4. The Scale Factor can be adjusted externally by variable resistors in series with the reference input and/or in series to the internal feedback resistor (See APPLICATIONS INFORMATION).
5. Integral Linearity is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input combination.
6. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
7. The HS 3160 has been used successfully with OP-07, OP-27 and LF441A. For high speed application HA2525, LF411ACN and OP-01 are recommended.
8. Use series 470Ω resistor to limit startup current — See applications schematics.

CAUTION: ESD (Electro-Static-Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed.

CASE DIMENSIONS



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT 1, $I_{OUT\,1}$	22	R FEEDBACK
2	OUTPUT 2, $I_{OUT\,2}$	21	V_{REF}
3	GND	20	V_{DD}
4	BIT 1 (MSB)	19	BIT 16 (LSB)
5	BIT 2	18	BIT 15
6	BIT 3	17	BIT 14
7	BIT 4	16	BIT 13
8	BIT 5	15	BIT 12
9	BIT 6	14	BIT 11
10	BIT 7	13	BIT 10
11	BIT 8	12	BIT 9

PRINCIPLES OF OPERATION

The HS 3160 achieves true 14 bit accuracy coupled with 16 bit resolution by using a decoded or segmented DAC scheme to implement this function. The following is a brief description of this approach.

The most common technique for building a D/A converter of n bits is to use n switches to turn n current or voltage sources on or off. The n switches and n sources are designed so that each switch or bit contributes twice as much to the D/A converter's output as the preceding bit. This technique is commonly known as binary weighting and allows an n-bit converter to generate 2^n output levels by turning on the proper combination of bits.

In such binary-weighted converter, the switch with the smallest contribution (the LSB) accounts for only 2^{-n} of the converter's full-scale value. Similarly, the switch with the largest contribution (the MSB) accounts for 2^{-1} or half of the converter's full-scale output. Thus it is easy to see that a given percent change in the MSB will have a greater effect on the converter's output than would a similar percent change in the LSB. For example, a 1% change in the LSB of a 10 bit converter would only affect the output by 0.001% of full-scale. A 1% change in the MSB of the same converter would affect the output by 0.5% of F.S.R.

In order to overcome the problem which results from the large weighting of the MSB, the two MSB's can be decoded to three equally weighted sources. Table 1 shows that all combinations of the two MSB's of a converter result in four output levels. So by replacing the two MSB's with three bits equally weighted at ¼ full-scale and decoding the two MSB digital inputs into three lines which drive the equally weighted bits. The same functional performance can be obtained. Thus by replacing the two MSB switches of a conventional converter with three switches properly decoded, the contribution of any switch is reduced from ½ to ¼. This reduction in sensitivity also reduces the accuracy required of any switch for a given overall converter accuracy.

Table 1. Contribution of the two MSB's

2^{-1}(MSB)	2^{-2}	Output
0	0	0
0	1	¼ Full-Scale
1	0	½ Full-Scale
1	1	¾ Full-Scale

With the decoded converter described above, a 1% change in any of the converter's switches will affect the output by no more than 0.25% of full-scale as compared to 0.5% for a conventional converter. In other words the conventional d-a converter can be made less sensitive to the quality of it's individual bits by decoding.

In the HS 3160 the first four MSB's are decoded into 16 levels which drive 15 equally weighted current sources. The sensitivity of each switch on the output is reduced by a factor of 8. Each of the 15 sources contributes 6.25% output change rather than an MSB change of 50% for the common approach.

Following the decoded section of the DAC a standard binary weighted R-2R approach is used. This divides each of the 16 levels (or 6.25% of F.S.) into 4096 discrete levels (the 12 LSB's).

OUTPUT CAPACITANCE

The HS 3160 has very low output capacitance (C_O). This is specified both with all switches ON and all switches OFF. Output capacitance varies from 50pf to 100pf over all input codes. This low capacitance is due in part to the decoding technique used. Smaller switches are used with resulting less capacitance. Three important system characteristics are affected by C_O and ΔC_O; namely digital feedthrough, settling time, and bandwidth. The DAC output equivalent circuit can be represented as shown in Figure 1.

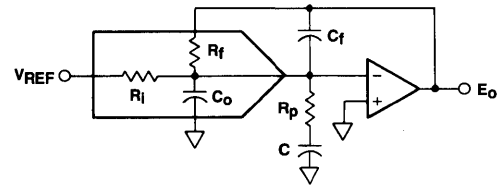


Figure 1. HS 3160 Equivalent Output Circuit

Digital feedthrough is the change in analog output due to the toggling conditions on the converter input data lines when the analog input V_{REF} is at 0V. The HS 3160 has very low C_O and therefore will yield low digital feedthrough. Inputs to the HS 3160 can be buffered. This input latch with microprocessor control is shown in Figure 5.

Settling time is directly affected by C_O. In Figure 1, C_O combines with R_f to add a pole to the open loop response, reducing bandwidth and causing excessive phase shift — which could result in ringing and/or oscillation. A feedback capacitor, C_f must be added to restore stability. Even with C_f, there is still a zero-pole mismatch due to R_iC_O which is code dependent. This code dependent mismatch is minimized when $C_OR_i = R_fC_f$. However C_f must now be made larger to compensate for worst case ΔR_iC_O — resulting in reduced bandwidth and increased settling time. With the HS 3160 small values for C_f must be used. Resistor R_p can be added, this will parrallel R_i decreasing the effective resistance. If C_f is reduced the bandwidth will be increased and settling time decreased. However a system penalty for lowering C_f is to increase noise gain. The tradeoff is noise vs. settling time. If R_p is added then a large value (1mF or greater) non-polarized capacitor C_p should be added in series with R_p to eliminate any DC drifts. If settling time is not important, eliminate R_p and C_p, and adjust C_f to prevent overshoot.

OUTPUT OFFSET

In most applications, the output of DAC is fed into an amplifier to convert the DAC's current output to voltage. A little known and not commonly discussed parameter is the linearity error versus offset voltage of the output amplifier. All CMOS DAC's must operate into a virtual ground, i.e., the summing junction of an op amp. Any amplifier's offset from the amplifier will appear as an error at the output (which can be related to LSB's of error).

Most all CMOS DAC's currently available are implemented using an R-2R ladder network. The formula for nonlinearity is typically $0.67mV/mV_{OS}$ (not derived here). However the HS 3160 has a coefficient of only $0.065mV/mV_{OS}$!! This is due to the decoding technique described earlier. CMOS DAC applications notes (including this one) always show a potentiometer used to null out the amplifier's offset. If an amplifier is chosen having 'pretrimmed' offset it may be possible to eliminate this component. Consider the following calculations:

1. Using LF441A amplifier (low power — 741 pinout)
2. Specified offset: 0.5mV max
3. Temperature coefficient of input offset: 10μV/°C max

V_{OS} max (0°C to 70°C) = 0.5mV + (70μV)10 = 1.2mV
Additional nonlinearity (max) = 1.2mV × 0.065mV/mV
= 78μV (½LSB @ 16 Bits!)
Where: 78μV ≅ ½LSB @ 16 Bits (10V range)

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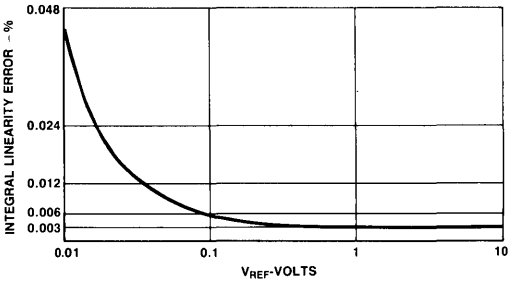
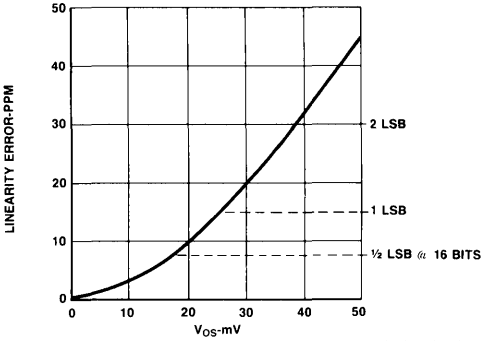
CHARACTERISTIC CURVES

(Typical @ +25°C, V_{DD} = +15VDC, V_{REF} = +10VDC, unless otherwise noted.)

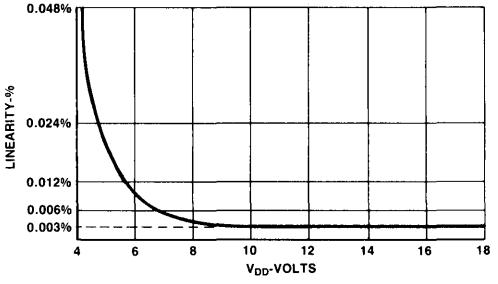


Integral Linearity Error vs. Reference Voltage

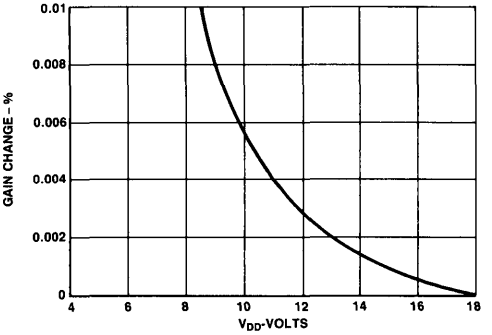


Additional Linearity Error vs. Output-Amplifier Offset-Voltage

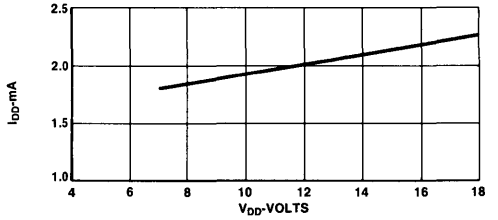
(V_{REF} = + 10V)



Linearity vs. Supply Voltage

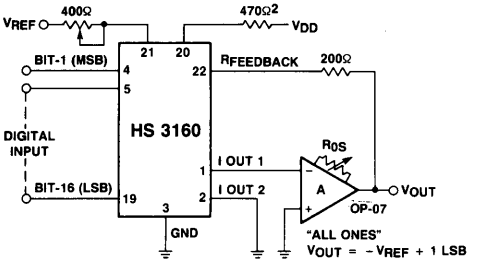


Gain Change vs. Supply Voltage



Power Supply Current vs. Voltage

APPLICATIONS INFORMATION

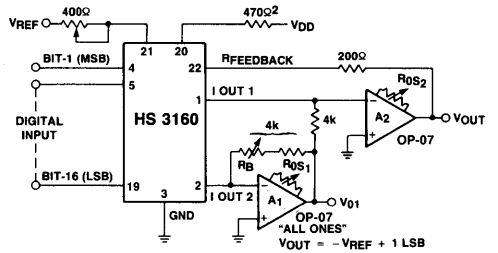


NOTES:
1. To maintain specified HS 3160 linearity, the external amplifier (A) must be zeroed.
   Apply an ALL "ZEROS" digital input and adjust R_{OS} for V_{OUT} = 0 ±1mV.
2. Series resistor recommmended to limit current during 'turn-on'.

Transfer Characteristics

BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-N})$
100...001	$-V_{REF}(½+2^{-N})$
100...000	$-V_{REF}/2$
011...111	$-V_{REF}(½-2^{-N})$
000...001	$-V_{REF}(2^{-N})$
000...000	0

Figure 2. Unipolar Operation (2-Quadrant Multiplication)

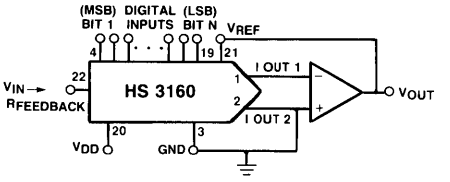


NOTES:
1. To maintain specified HS 3160 linearity, external amplifiers (A_1 and A_2) must be zeroed. With a digital input of 10...0 and V_{REF} set to zero:
   a) Set R_{OS1} for V_{O1} = 0
   b) Set R_{OS2} for V_{OUT} = 0
   c) Set V_{REF} to +10V and adjust R_B for V_{OUT} to be 0 Volts
2. Series resistor recommended to limit current during 'turn-on.'

Transfer Characteristics

OFFSET BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-(N-1)})$
100...001	$-V_{REF}(2^{-(N-1)})$
100...000	0
011...001	$V_{REF}(2^{-(N-1)})$
000...001	$V_{REF}(1-2^{-(N-1)})$
000...000	V_{REF}

Figure 3. Bipolar Operation (4-Quadrant Multiplication)

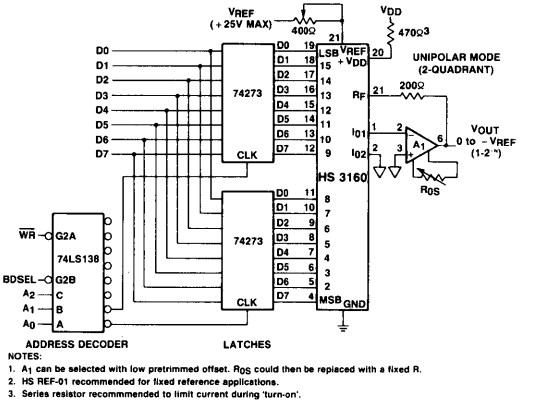


Via the above configuration, the HS 3160 can be used to divide an analog signal by a digital code (i.e, for digitally controlled gain). The transfer function is given as:

$$V_{OUT} = \frac{-V_{IN}}{\frac{\text{Bit 1}}{2^1} + \frac{\text{Bit 2}}{2^2} + \frac{\text{Bit 3}}{2^3} + \ldots + \frac{\text{Bit N}}{2^N}}$$

where the value of each bit is 0 or 1. Division by all "0"s is undefined and causes the op amp to saturate.

Figure 4. Analog/Digital Division



NOTES:
1. A_1 can be selected with low pretrimmed offset. R_{OS} could then be replaced with a fixed R.
2. HS REF-01 recommended for fixed reference applications.
3. Series resistor recommmended to limit current during 'turn-on'.

Figure 5. Microprocessor Interface to HS 3160

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APPLICATIONS INFORMATION

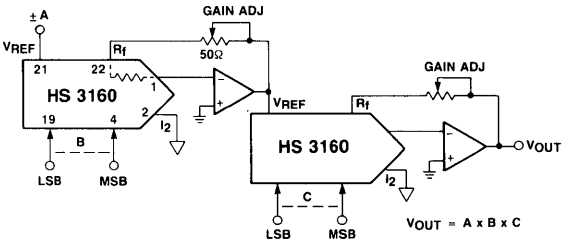


Figure 6. Cascade Multiplication

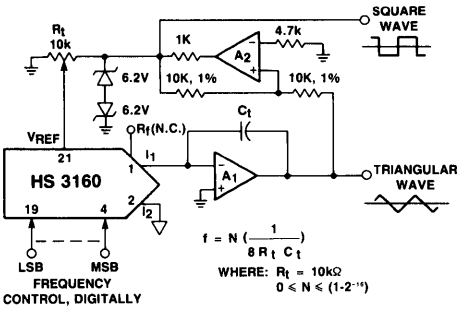


Figure 7. Programmable Function Generator

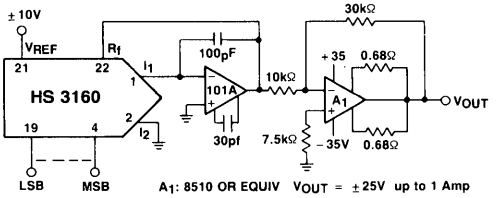


Figure 8. DAC Controlled Power Output

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

ORDERING INFORMATION

MODEL	LINEARITY RESOLUTION	LINEARITY ERROR (MAX)	MONOTONIC RANGE	TEMP RANGE	SCREENING
HS 3160C-3	16 BITS	0.012%	0°C to +70°C	0°C to +70°C	—
HS 3160C-4	16 BITS	0.006%	0°C to +70°C	0°C to+ 70°C	—
HS 3160B-3	16 BITS	0.012%	−25°C to +85°C	−55°C to +125°C	883C
HS 3160B-4	16 BITS	0.006%	−25°C to +85°C	−55°C to +125°C	883C

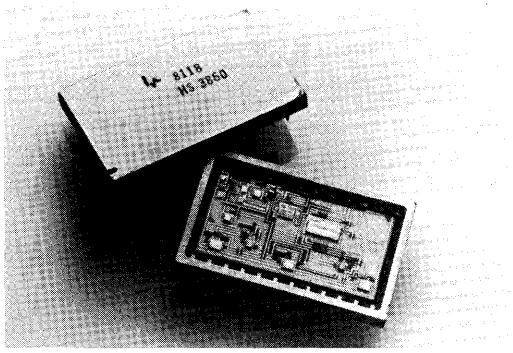
Specifications subject to change without notice.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS 3860
12-Bit DAC with Input Registers

FEATURES

- ±1/2 LSB Linearity
- ±0.3% Absolute Accuracy Over Temperature
- 7μSec Settling Time
- Input Registers
- MIL-STD-883 Screening Available (B Models)



DESCRIPTION

The HS 3860 is a 12-Bit digital-to-analog converter packaged in a hermetically sealed, 24 pin double-width, dual-in-line package.

The D/A is constructed using hybrid microcircuit technology and includes a precision thin-film network, laser-trimmed to produce a high linearity, high accuracy converter, stable over a wide temperature range. Errors in linearity and accuracy are specified at room temperature as well as operating temperature extremes for both MIL and Commercial products.

The HS 3860 includes an internal, precision reference supply, a fast output amplifier for minimum settling time, and input registers for easier microprocessor interface.

MIL-STD-883 Rev. C, Level B screening and processing is available in the "B" grade device. Operating temperature range for the HS 3860B is −55°C to +125°C.

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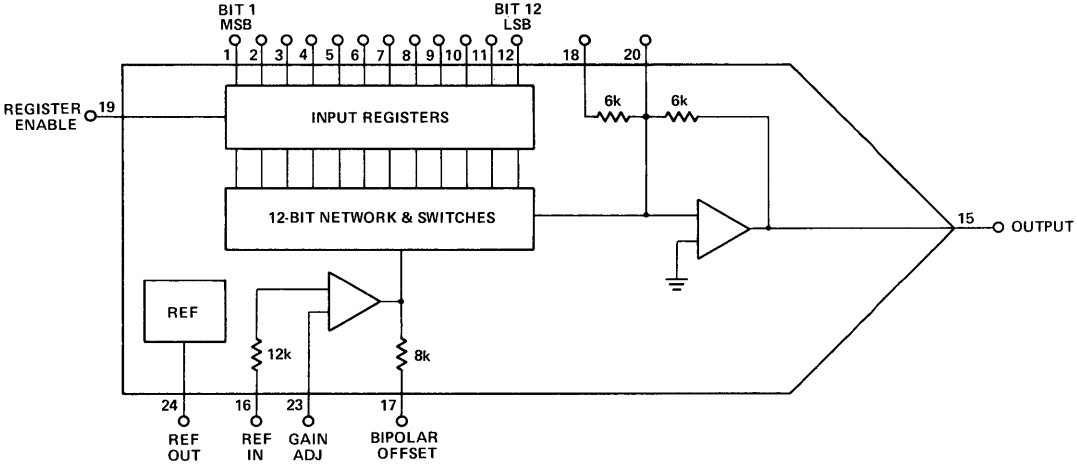
FUNCTIONAL DIAGRAM



SPECIFICATIONS

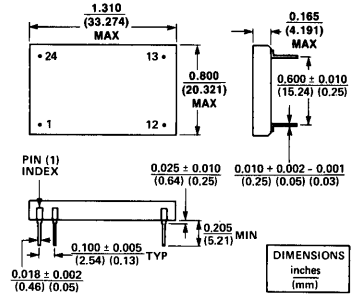
(Typical for all models @ +25°C and nominal power supplies unless otherwise noted)

MODEL	HS 3860
TYPE	Digital to Analog Converter
DIGITAL INPUTS	
Resolution	12 bits
Coding	Complementary Binary/ Offset Binary
Logic Levels (Data Inputs)	
Logic "1" (30μA max)	+2V min, +5.5V max
Logic "0" (-0.6mA max)	-0.5V min, +0.7V max
Register Enable Logic[1]	
Logic "1" (60μA max)	+2V min, +5.5V max
Logic "0" (-1.2mA max)	-0.5V min, +0.7V max
Pulse Width	60nS min
Set up Time	40nS min
ANALOG OUTPUT	
Output Voltage Ranges	0 to +10; ±5; ±10
Output Impedance	0.05Ω typ
Output Current	±5mA
Short Circuit Duration	Indefinite to Common
ACCURACY	
Linearity Error[2, 3]	
0°C to +70°C	±1/4 LSB typ; ±1/2 LSB max
-55°C to +125°C	±1/2 LSB max
Monotonicity	Guaranteed Over Temperature
Full Scale Absolute Error[4, 5]	
+25°C	±0.05% F.S.R. typ; ±0.1% F.S.R. max
-55°C to +125°C[6]	±0.15% F.S.R. typ; ±0.3% F.S.R. max
Zero Error[4, 5]	
25°C	±0.025% F.S.R. typ; ±0.05% F.S.R. max
-55°C to 125°C[6]	±0.05% F.S.R. typ; ±0.1% F.S.R. max
Gain Error	±0.1%
Gain Drift	±10ppm/°C
CONVERSION SPEED	
Settling Time	
20V Step	5μS typ; 7μS max
10V Step	3μS typ; 5μS max
Output Slew Rate	20 volts/μS typ
REFERENCE OUTPUT	
Voltage	6.3 volts ±5%
Tempco	±10ppm/°C
Load Current	100μA max
POWER SUPPLIES	
Power Supply Range	
+15V Supply	+14V to +18V
-15V Supply	-14V to -18V
+5V Supply	+4V to +7V
Power Supply Rejection	
+15V (from +14.55 to +15.45V)	-0.01% F.S.R./% typ; ±0.04% F.S.R./% max
-15V (from -14.55 to -15.45V)	±0.001% F.S.R./% typ; ±0.004% F.S.R./%max
Current Drain	
+15V Supply	25mA max
-15V Supply	25mA max
+5V Supply	50mA max
Power Consumption	675mW typ, 1000mA max
MECHANICAL	
Case Style	24 Pin DIP, Ceramic

NOTES

1. The analog output follows the digital input when Register Enable is a logic "0". The analog output is constant when the Register Enable is a logic "1".
2. Hybrid Systems guarantees and tests maximum Linearity Error at the extremes of the operating temperature and at room temperature. ±1/2 LSB Linearity Error guarantees monotonicity and differential linearity of ±1 LSB.
3. One LSB is 0.024% F.S.R. for a 12 bit DAC.
4. F.S.R. is Full Scale Range. For the ±10V output range the F.S.R. is 20 volts and 1 LSB is 4.88mV.
5. Absolute Accuracy Error includes linearity, gain, offset and all other errors and is specified without the use of adjustments.
6. Commercial Models are specified over a temperature range of 0°C to +70°C.

Package Outline

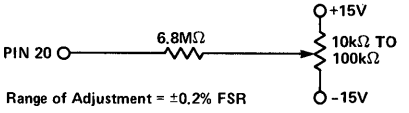


Pin Designations

PIN	FUNCTION	PIN	FUNCTION
1	Bit 1	24	REF OUT
2	Bit 2	23	-Full Scale Adjust (Gain Adj)
3	Bit 3	22	+15V
4	Bit 4	21	Common
5	Bit 5	20	Summing Junction
6	Bit 6	19	Register Enable
7	Bit 7	18	10V Range
8	Bit 8	17	Bipolar Offset
9	Bit 9	16	REF IN
10	Bit 10	15	Analog Output
11	Bit 11	14	-15V
12	Bit 12	13	+5V

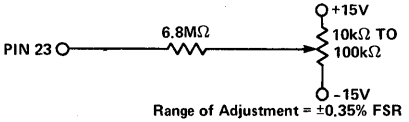
APPLICATIONS INFORMATION

FULL SCALE ADJUSTMENT



Connect the full scale potentiometer as shown and apply all "0's" to the digital inputs. Adjust the potentiometer until the analog output is equal to the maximum positive voltage for the chosen output range as shown in the table.

ZERO (-FULL SCALE) ADJUSTMENT



Connect the zero (-full scale) potentiometer as shown and apply all "1's" to the digital inputs. Adjust the potentiometer until the analog output is equal to zero volts for unipolar output ranges and -full scale voltage for bipolar output ranges.

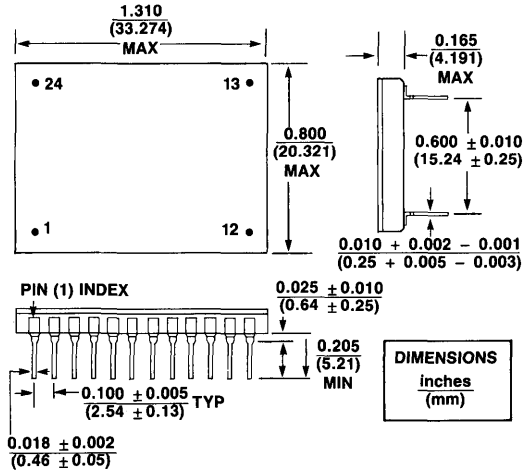
INPUT LOGIC CODING AND OUTPUT RANGE SELECTION

DIGITAL INPUT MSB LSB	ANALOG OUTPUT 0 to +10V	±5V	±10V
0000 0000 0000	+9.9976V	+4.9976V	+9.9951V
0000 0000 0001	+9.9951V	+4.9951V	+9.9902V
0111 1111 1111	+5.0000V	0.0000V	0.0000V
1000 0000 0000	+4.9976V	-0.0024V	-0.0049V
1111 1111 1110	+0.0024V	-4.9976V	-9.9951V
1111 1111 1111	0.0000V	-5.0000V	-10.0000V
CONNECT	24 to 16	24 to 16	24 to 16
PIN TO PIN	17 to 21	17 to 20	17 to 20
	15 to 18	15 to 18	

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 3860B	MIL, 12 Bit D/A
HS 3860C	COMM, 12 Bit D/A

Specifications subject to change without notice.


1.310
(33.274)
MAX
• 24
13 •
• 1
12 •
0.800
(20.321)
MAX
0.165
(4.191)
MAX
0.600 ±0.010
(15.24 ±0.25)
0.010 + 0.002 − 0.001
(0.25 + 0.005 − 0.003)
PIN (1) INDEX
0.025 ±0.010
(0.64 ±0.25)
0.205
(5.21)
MIN
0.100 ±0.005
(2.54 ±0.13) TYP
0.018 ±0.002
(0.46 ±0.05)
DIMENSIONS
inches
(mm)

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Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS-7541A

CMOS 12 Bit Multiplying DAC

Features

- Improved Accuracy and Ruggedness Over The 7541
- 12 Bit Endpoint Linearity (± 1/2 LSB)
- Improved Gain Error: ± 1 LSB (No User Adjustment Required)
- Low Gain Tempco (5 ppm/°C Max)
- 2 and 4 Quadrant Multiplication
- Superior Power Supply Rejection.
- Low Feedthrough Error and Digital Charge Injection.
- Low Power Consumption.
- TTL/CMOS Compatible
- All Data Input Pins Designed To withstand 200IV ESD
- Direct Replacement for AD 7541 and AD 7541 A.

Applications

- Programmable Amplifiers
- Function Generators
- Digitally Controlled Attenuators
- Digitally Controlled Power Supplies
- Digital Filters
- Digital/Synchro Conversion
- Ratiometric A/D Conversion
- CRT Graphics Generator

Description

The HS-7541A is a 12-Bit, 4 quadrant multiplying digital-to-analog converter contained in a single high density monolithic CMOS chip. It is manufactured using an advanced oxide isolated, silicon-gate, monolithic CMOS technology.

The HS-7541A features circuitry designed to protect data inputs against damage from 2001 volt electrostatic discharge.

The HS-7541A consists of a highly stable thin-film R-2R ladder network and twelve NMOS current switches on a monolithic chip. The thin-film resistors are laser trimmed to provide true 12 Bit linearity and excellent absolute linearity. The NMOS switches are temperature compensating and their "ON" resistances are binarily scaled so that the voltage drop across each switch is identical. This is essential in maintaining the accuracy of the binarily weighted current division performed by the ladder network. The internal feedback resistor used in the output current-to-voltage conversion operation is matched to the R-2R ladder.

The HS-7541A is a superior pin-compatible replacement for the industry standard 7541 and the AD7541A. Available in standard Epoxy and CERDIP packages, the HS-7541A is compatible with automatic insertion equipment. The improved performance of the HS-7541A permits upgrading existing designs with greater ruggedness and accuracy. Tight linearity and gain error specifications may permit reduced system parts count by eliminating trimming circuitry.

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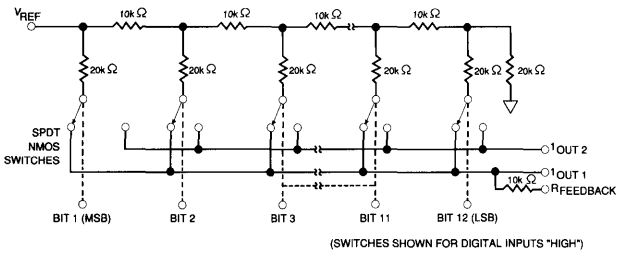
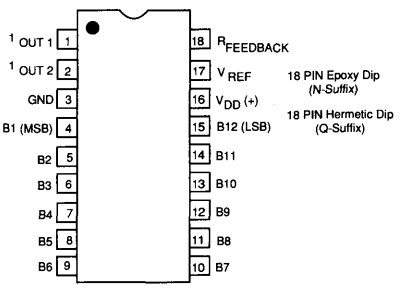
Functional Diagram



(SWITCHES SHOWN FOR DIGITAL INPUTS "HIGH")

Pin Connections



HS-7541A

CMOS 12-Bit Multiplying DAC

Absolute Maximum Ratings

(T_A=+25°C, unless otherwise noted)

V_{DD} (to GND)	+17V
V_{REF}(to GND)	±25V
V_{RFB}(to GND)	±25V
Digital Input Voltage Range	V_{DD} to GND
Output Voltage (Pin 1, Pin 2)	-0.3V, to V_{DD}
Power Dissipation (Package)	450mW
Derate Above +75°C	6mW/°C

Operating Temperature Range (T_A = Full)		
Commerical	(KN ,LN GRADES)	0° C to 70°C
Industrial	(BQ, CQ GRADES)	-25°C to +85°C
Military	(TQ, UQ GRADES)	-55°C to +125°C
Dice Junction Temperature		+150°C
Storage Temperature		-65°C to +150°C
Lead Temperature (Soldering, 60 Sec)		+300°C

Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
Use proper ESD handling procedures

Electrical Characteristics:

V_{DD} =+15V, V_{REF} = +10V,V_{OUT1} = V_{OUT2} = 0V; T_A = Full unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
STATIC ACCURACY						
Resolution	N		12			Bits
Nonlinearity	INL				± 1/2	LSB
Differential NonLinearity	DNL	HS-7541A - KN/BQ/TQ			± 1/2	LSB
		HS-7541A - JN/AQ/SQ			± 1	LSB
Gain Error	G_{FSE}	Using Internal Feedback Resistor				
		HS-7541A - KN/BQ/TQ				
		T_A = 25°C			1	LSB
		T_A = Full			2	LSB
		HS-7541A - JN/AQ/SQ				
		T_A = 25°C			2	LSB
		T_A = Full			3	LSB
GAIN TEMPCO (Δ Gain/Δ Temp.)	TC_{GFS}			± 2	± 5	PPM/°C
Power Supply Rejection Ratio (Δ Gain/ Δ V_{DD})	PSRR	T_A = 25°C, Δ V_{DD} = ±5%			±0.001	%/%
		T_A = Full, ΔV_{DD} = ±5%			±0.002	%/%
Output Leakage Current	I_{LKG}	For I_{OUT1} Digital Inputs = V_{IL}				
		HS-7541A - KN/BQ/TQ				
		T_A = 25°C			5	NA
		T_A = Full			10	NA
		HS-7541A - JN/AQ/SQ				
		T_A = 25°C			5	NA
		T_A = Full			100	NA
Zero Scale Error	I_{ZSE}	V_{REF}=+10V, all digital inputs=0V				
		HS-7541A - KN/BQ/TQ				
		T_A=25°C		0.002		LSB
		T_A=Full		0.01		LSB
		HS-7541A- JN/AQ/SQ				
		T_A=°25C		0.002		LSB
		T_A=Full		0.05		LSB

Electrical Characteristics:

V_{DD} =+15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V; T_A = Full unless otherwise noted.

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Reference Input						
Input Resistance	R_{PEF}		7	11	15	kΩ
Input Resistance Tempco (Δ R/ΔT)	TC R-REF			50		ppm/°C
Power Supply						
Supply Current	I_{DD}	Digital Inputs = V_{IL} OR V_{IH} Digital Inputs = 0V or V_{DD}		 100	2 μ A	ma
Digital Input						
Digital Input High	V_{IH}		2.4			V
Digital Input Low	V_{IL}				0.8	V
Input Leakage Current	I_{IL}	T_A = 25°C T_A = Full		±1	 ±1	NA μA
Input Capacitance	C_{IN}	V_{IN} = 0V			8	PF
Dynamic Performance						
Propagation Delay	T_{PD}	I_{OUT} LOAD = 100Ω, C_{EXT} = 13 PF, Measured Fom Digital Input Change to 90% Of Final Analog Output, T_A = 25°C		100	150	NS
Output Current Settling Time	T_S	To ± 1/2 LSB, T_A = 25°C Extrapolated Measurement		0.6	1	μS
Feedthrough Error (V_{REF} to I_{OUT})	FT	V_{REF} = 20 V_{PP} @ f = 10 kHz All Digital Inputs Low TA = 25°C		2	5	mV_{P-P}
Digital To Analog Glitch Energy	Q	V_{REF} = 0V, All Digital Inputs = 0V To V_{DD} Or V_{DD} To 0V, T_A = 25°C		700	1000	NVS
Analog Outputs						
Output Capacitance	C_{OUT1} C_{OUT2}	Digital Inputs = V_{IH} Digital Inputs = V_{IL} Digital Inputs = V_{IH} Digital Inputs = V_{IL}		85 30 30 85	120 50 50 120	PF PF PF PF

7

Circuit Description

General

The HS7541A is a 12-bit multiplying D/A converter consisting of a highly stable, silicon-chrome thin film R-2R resistor ladder network and twelve pairs of NMOS current steering switches on a monolithic chip. Most applications require the addition of a voltage or current reference and an output operational amplifier.

A simplified circuit of the HS754A1 is shown in Figure 1. The R-2R inverted ladder binarily divides the input currents that are switched between $I_{OUT\,1}$ and $I_{OUT\,2}$ bus lines. This switching allows a constant current to be maintained in each ladder leg independent of the input code.

The twelve output current-steering switches are in series with the R-2R resistor ladder, and therefore, can introduce bit errors. It is essential then, that the switch "ON" resistance be binarily scaled so that the voltage drop across each switch remains constant. If, for example, switch 1 of Figure 1 was designed with an "ON" resistance of 10 ohms, switch 2 for 20 ohms, etc., then with a 10 volt reference input, the current through switch 1 is 0.5mA, switch 2 is 0.25mA, etc., a constant 5mV drop will then be maintained across each switch.

To further insure accuracy across the full temperature range, permanently "ON" MOS switches are included in series with the feedback resistor and the R2-R ladder's terminating resistor. These series switches are equivalently scaled to two times switch 1 (MSB) and to switch 12 (LSB) respectively to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection) V_{DD} must be present to turn "ON" these series switches.

2001 ESD Protection

In the design of the HS-7541A's data inputs, 2001 V ESD resistance has been incorporated through careful layout and the inclusion of input protection circuitry.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for all digital inputs LOW and HIGH respectively. The reference current is switched to $I_{OUT\,2}$ when all inputs are LOW and $I_{OUT\,1}$ when inputs are HIGH. The $I_{LEAKAGE}$ current source is the combination of surface and junction leakages to the substrate; the 1/4096 current source represents the constant 1-bit current drain through the ladder terminating resistor. The output capacitance is dependent upon the digital input code, and is therefore varied between the low and high values.

Output Impedance

The output resistance, as in the case of the output capacitance,varies with the digital input code. The resistance, looking back into the $I_{OUT\,1}$ terminal, may be anywhere between 10kΩ (the feedback resistor alone when all digital inputs are low) and 7.5kΩ (the feedback resistor in parallel with approximately 30kΩ of the R-2R ladder network resistance when any single bit logic is high). Static accuracy and dynamic performance will be affected by these variations.

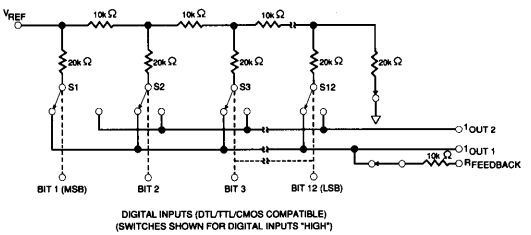


FIGURE 1: Simplified DAC Circuit

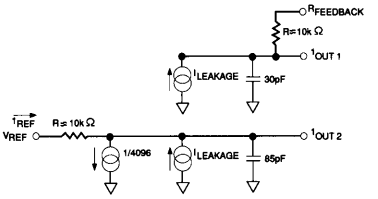


FIGURE 2: HS-7541A Equivalent Circuit (All Inputs Low)

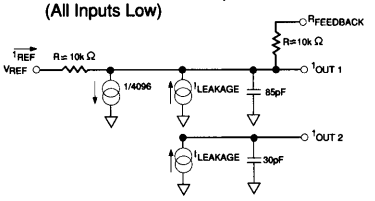


FIGURE 3: HS-7541A Equivlalent Circuit (All Inputs High)

Application Information

Unipolar Operation

The connections required for digital unipolar operation are shown in Figure 4. The reference voltage V_{REF} may be either positive or negative. The 2kΩ potentiometer in the V_{REF} line and the 1kΩ resistor in the feedback loop are optional and are only needed when the gain error must be trimmed to less than 0.3% F.S.R. They should track each other to better than 0.1%, but don't have to track 7541's internal network resistors.

As shown in Figure 4 the DAC current output is typically connected to an external OP-AMP with it's non-inverting input tied to ground. The amplifier selected should have a low input bias current and low drift over temperature. To maintain specified HS7541 linearity, the amplifiers input offset voltage should be nulled to less than ±200μV (o.1LSB). Table 1 shows the code table for unipolar operation.

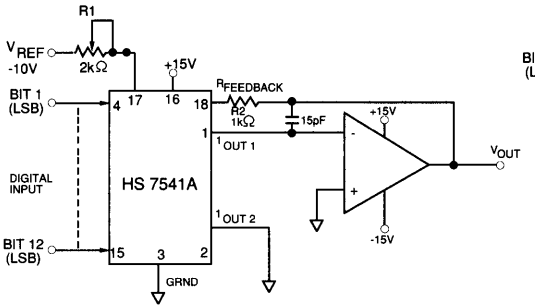


FIGURE 4: Unipolar Operation

Bipolar Operation

The connections required for bipolar operation are shown in Figure 5. The digital input is offset binary coded and produces an output according to the code table shown in Table 2.

As in the case of unipolar operation the gain trim resistors can be omitted in applications that do not require minimum gain error. Amplifier considerations of low input bias current, low drift and offset nulling are also applicable for bipolar operation.

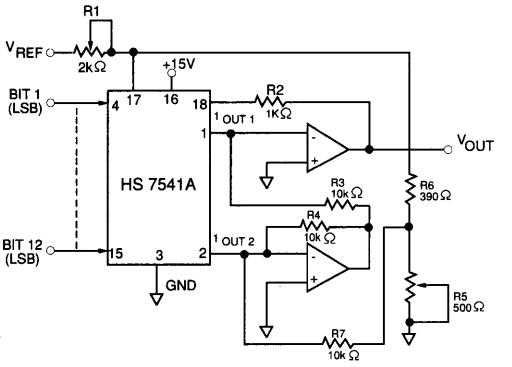


FIGURE 5: Bipolar Operation

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	-0.99975 V_{REF}
1 0 0 0 0 0 0 0 0 0 0 0	-0.50000V V_{REF}
0 1 1 1 1 1 1 1 1 1 1 1	-0.49975 V_{REF}
0 0 0 0 0 0 0 0 0 0 0 0	0

TABLE 1: Unipolar Operation Code Table

DITGITAL INPUT	NOMINAL ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1 1 1	-0.99951 V_{REF}
1 0 0 0 0 0 0 0 0 0 0 0	-0.00049V V_{REF}
0 1 1 1 1 1 1 1 1 1 1 1	+0.50000 V_{REF}
0 0 0 0 0 0 0 0 0 0 0 0	+1.00000 V_{REF}

TABLE 2: Bipolar Operation Code Table

HS-7541A

CMOS 12-BIT Multiplying DAC

Ordering Information

PART #	PACKAGE	T_A-TEMP RANGE (°C)	RELATIVE ACCURACY (LSB's)	GAIN ERROR (LSB's)
HS-7541A JN	20-Pin Epoxy Dip	0 to 70	± 1/2	± 3
HS-7541A KN	20-Pin Epoxy Dip	0 to 70	± 1/2	± 2
HS-7541A AQ	20-Pin Hermetic Cerdip	-25 to 85	± 1/2	± 3
HS-7541A BQ	20-Pin Hermetic Cerdip	-25 to 85	± 1/2	± 2
HS-541A SQ	20-Pin Hermetic Cerdip	-55 to 125	± 1/2	± 3
HS-541A TQ	20-Pin Hermetic Cerdip	-55 to125	± 1/2	± 2
HS-7541A SQ/883	20-Pin Hermetic Cerdip	-55 to125	+1/2	± 3
HS-7541A TQ/883	20-Pin Hermetic Cerdip	-55 to125	± 1/2	± 2

NOTES: 1) Consult Factory For 883 Data Sheet
2) Package Designations: Suffix N-Plastic Dip, Suffix Q-Hermetic Dip. For package mechanical dimensions, call DataLinear at (408) 945-9080.

CROSS REFERENCE INFORMATION

ADI Part No.	DataLinear Part No.
AD 7541A JN	HS 7541A JN
AD 7541A KN	HS 7541A KN
AD 7541A AD	HS 7541A AQ
AD 7541A BD	HS 7541A BQ
AD 7541A SD	HS 7541A SQ
AD 7541A TD	HS 7541A TQ
AD 7541A SD/883	HS 7541A SQ/883
AD 7528A TD/883	HS 7541A TQ/883

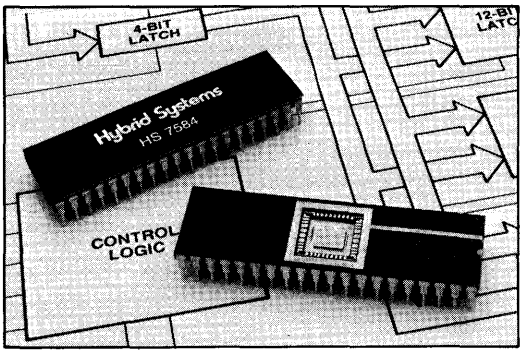
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS 7584

Quad 12-Bit MDAC

FEATURES

- Four 12-Bit DACs on a Single Monolithic Chip
- Independent V_{REF} Input For Each DAC
- Low Power CMOS (5 mW)
- Single +5V Operation
- Double Buffered Input Structure for μP Interface
- Available in 40-Pin DIP or 44-Pin LCC/PLCC



DESCRIPTION

The HS 7584 contains four CMOS current output D/A converters on a single monolithic chip. All four DACs provide 4-quadrant multiplication with a separate reference input and feedback resistor for each DAC. Monolithic construction ensures excellent matching and tracking between all four DACs.

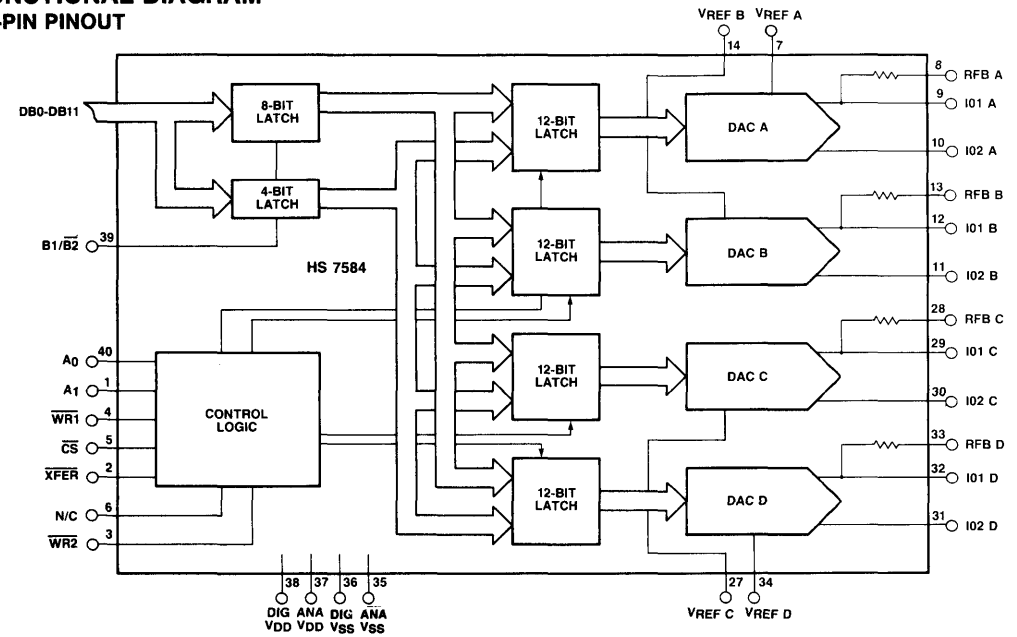
The double buffered input structure is designed to accept 12-Bit parallel data or 8-Bit/4-Bit data allowing easy microprocessor interface. All four DACs may be simultaneoulsy updated using a single $\overline{XFER}$ command.

The HS 7584 is packaged in a 40-Pin DIP as well as a 44-Pin LCC and PLCC and operates from a +5V power supply. Processing to MIL-STD-883B, Rev C is available.

7

FUNCTIONAL DIAGRAM

40-PIN PINOUT



SPECIFICATIONS

(Typical @25°C with $V_{DD} = V_{SS} = +5V$, $V_{REF} = +10V$ unless otherwise noted.)

MODEL	HS 7584	
PACKAGE	**DIP/LCC**	**PDIP/PLCC**
DIGITAL INPUTS		
Resolution	12-Bits	*
V_{IH} Logic Level	2.4V min	*
V_{IL} Logic Level	0.8V max	*
I_{IN} Input Current	1μA typ, 4μA max	*
2 Quad, Unipolar Coding	Straight Binary	*
4 Quad, Bipolar Coding	Offset Binary	*
REFERENCE INPUT		
Input Resistance	5kΩmin, 10kΩtyp, 15kΩmax	*
STATIC PERFORMANCE		
Integral Linearity	0.006% FSR typ, 0.012% FSR max	*
Differential Linearity	0.006% FSR typ, 0.024% FSR max	*
Monotonicity	12-Bits	*
DYNAMIC PERFORMANCE		
Output Current Settling Time	2μ sec typ, 3μ sec max	*
Data Set-Up Time	100 nsec min	*
Data Hold Time	0 nsec min	*
Write Pulse Width	100 nsec min	*
ANALOG OUTPUT		
Scale Factor	$100\mu A/V_{REF}$	*
Scale Factor Accuracy	±0.0488% typ, 0.0976% max	±0.15% max
I_O Leakage	1 nA typ, 10 nA max	*
Output Capacitance	80 pF typ	*
STABILITY		
Scale Factor	1 ppm/°C typ, 2 ppm/°C max	10 ppm/°C
Integral Linearity	0.5 ppm/°C typ, 1 ppm/°C max	*
Differential Linearity	0.5 ppm/°C typ, 1 ppm/°C max	*
Input Impedance	−400 ppm/°C typ	*
I_{OUT} Leakage (T_{MIN}-T_{MAX})	100 nA typ, 200 nA max	*
Scale Factor Tracking (DAC to DAC)	2 ppm/°C typ, 4 ppm/°C max	*
POWER REQUIREMENTS		
Operating Voltage	+5V ±5%	*
Supply Current		
V_{IN} = 0 or 5V	0.5 mA typ, 1 mA max	*
V_{IN} = 0.8V or 2.0V	5 mA typ, 10 mA max	*
Power Supply Rejection Ratio	0.0005%/%typ, .002%/% max	0.0025%/%
Power Dissipation		
V_{IN} = 0 or 5V	2.5 mW typ, 5.0 mW max	*
V_{IN} = 0.8V or 2.0V	25 mW typ, 50 mW max	*

*Specifcations same as HS 7584-DIP/LCC

ABSOLUTE MAXIMUM RATINGS

V_{DD} 7V
V_{SS} . . . . . ±0.4V
V_{REF} A,B,C,D . . . . . ±20V
RFB A,B,C,D . . . . . ±20V
Digital Input Voltage . . . . . −0.3V to 5.5V
V_{PIN} 9,10,11,12,29,30,31,32 . . . . . ±0.4V
ANGND to DGND . . . . . ±0.4V
Power Dissipation (Any Package)
To +75°C . . . . . 450 mW
Derates above +75°C . . . . . 6 mW/°C
Operating Temperature Range
Commercial . . . . . 0 to +70°C
Extended . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

PIN ASSIGNMENTS (DIP, PDIP)

PIN	FUNCTION	DESCRIPTION
1	A1	Address Line 1
2	$\overline{XFER}$	Transfer, Updates all DAC's
3	$\overline{WR2}$	Write Input, Active Low, Gates Transfer Fuction
4	$\overline{WR1}$	Write Input, Active Low, Gates DAC Selection
5	$\overline{CS}$	Chip Select Input, Active Low
6	N/C	No Connection
7	$V_{REF\ A}$	Voltage Reference Input to DAC A
8	RFB A	Reference Feedback Resistor of DAC A
9	IO1 A	Current Output to Virtual Ground
10	IO2 A	Current Output – Complement of IO1 A
11	IO2 B	Current Output – Complement of IO2 B
12	IO1 B	Current Output to Virtual Ground
13	RFB B	Reference Feedback Resistor of DAC B
14	$V_{REF\ B}$	Voltage Reference Input to DAC B
15	DB11	Data Bit 11 (MSB)
16	DB10	Data Bit 10
17	DB9	Data Bit 9
18	DB8	Data Bit 8
19	DB7	Data Bit 7
20	DB6	Data Bit 6
21	DB5	Data Bit 5
22	DB4	Data Bit 4
23	DB3	Data Bit 3
24	DB2	Data Bit 2
25	DB1	Data Bit 1
26	DB0	Data Bit 0 (LSB)
27	$V_{REF\ C}$	Voltage Reference Input to DAC C
28	RFB C	Reference Feedback Resistor of DAC C
29	IO1 C	Current Output to Virtual Ground
30	IO2 C	Current Output – Complement of IO1 C
31	IO2 D	Current Output – Complement of IO1 D
32	IO1 D	Current Output to Virtual Ground
33	RFB D	Reference Feedback Resistor of DAC D
34	$V_{REF\ D}$	Voltage Reference Input to DAC D
35	AV_{SS}	Analog Ground
36	DV_{SS}	Digital Ground
37	AV_{DD}	Analog Supply
38	DV_{DD}	Digital Supply
39	B1/$\overline{B2}$	Byte 1/Byte 2, Selects Data Input Format 8-Bit/4-Bit or 12-Bit Parallel
40	A0	Address Line 2

PIN ASSIGNMENTS (LCC, PLCC)

PIN	FUNCTION	DESCRIPTION
1	A1	Address Line 1
2	$\overline{XFER}$	Transfer, Updates all DAC's
3	$\overline{WR2}$	Write Input, Active Low, Gates Transfer Fuction
4	$\overline{WR1}$	Write Input, Active Low, Gates DAC Selection
5	$\overline{CS}$	Chip Select Input, Active Low
6	N/C	No Connection
7	$V_{REF\ A}$	Voltage Reference Input to DAC A
8	RFB A	Reference Feedback Resistor of DAC A
9	IO1 A	Current Output to Virtual Ground
10	IO2 AF	Current Output (Forcing) } Complement of IO1 A
11	IO2 AS	Current Output (Sensing) } Complement of IO1 A
12	IO2 BS	Current Output (Sensing) } Complement of IO2 B
13	IO2 BF	Current Output (Forcing) } Complement of IO2 B
14	IO1 B	Current Output to Virtual Ground
15	RFB B	Reference Feedback Resistor of DAC B
16	$V_{REF\ B}$	Voltage Reference Input to DAC B
17	DB11	Data Bit 11 (MSB)
18	DB10	Data Bit 10
19	DB9	Data Bit 9
20	DB8	Data Bit 8
21	DB7	Data Bit 7
22	DB6	Data Bit 6
23	DB5	Data Bit 5
24	DB4	Data Bit 4
25	DB3	Data Bit 3
26	DB2	Data Bit 2
27	DB1	Data Bit 1
28	DB0	Data Bit 0 (LSB)
29	$V_{REF\ C}$	Voltage Reference Input to DAC C
30	RFB C	Reference Feedback Resistor of DAC C
31	IO1 C	Current Output to Virtual Ground
32	IO2 CF	Current Output (Forcing) } Complement of IO1 C
33	IO2 CS	Current Output (Sensing) } Complement of IO1 C
34	IO2 DS	Current Output (Sensing) } Complement of IO1 D
35	IO2 DF	Current Output (Forcing) } Complement of IO1 D
36	IO1 D	Current Output to Virtual Ground
37	RFB D	Reference Feedback Resistor of DAC D
38	$V_{REF\ D}$	Voltage Reference Input to DAC D
39	AV_{SS}	Analog Ground
40	DV_{SS}	Digital Ground
41	AV_{DD}	Analog Supply
42	DV_{DD}	Digital Supply
43	B1/$\overline{B2}$	Byte 1/Byte 2, Selects Data Input Format 8-Bit/4-Bit or 12-Bit Parallel
44	A0	Address Line 2

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APPLICATIONS INFORMATION

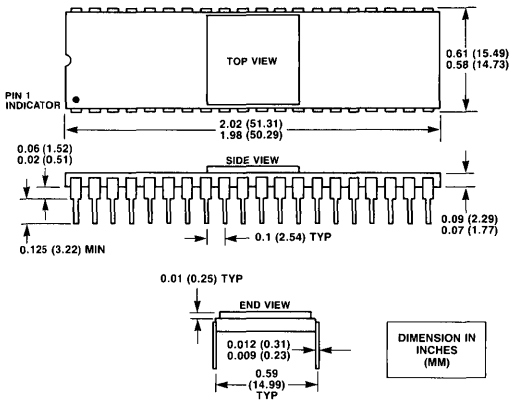
THEORY OF OPERATION

The HS 7584 is a quad MDAC designed to provide maximum flexibility. Each current output DAC provides 4-quadrant multiplication for unipolar and bipolar output and has an individual reference input and feedback resistor. The monolithic HS 7584 gives a designer four DAC's with excellent matching and tracking which accept separate AC or DC signals. The quad MDAC is therefore ideal for those applications where multiple digital to analog conversion roles are required in a small package with optimum thermal and gain error matching characteristics.

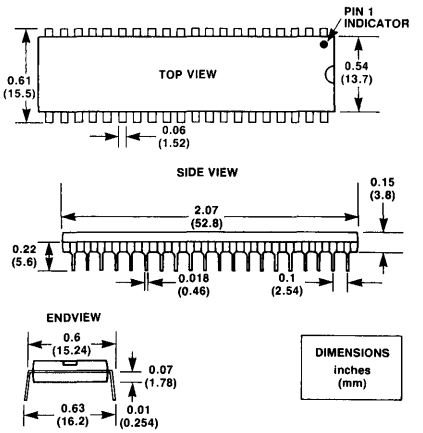
Maximum flexibility has also been applied to the microprocessor compatible control inputs. A double buffered input structure allows simple interface to many microprocessors without the need for external latches. The first buffer has been split to accept 12-Bit parallel data or 8-Bit/4-Bit data allowing direct interface to 8- or 12-Bit bus structures. A separate control line "B1/B2" allows the four MDAC's to be selectively connected to an 8- and a 12-Bit bus without the need for rewiring.

The monolithic CMOS construction results in very low system level power requirements with a total dissipation of 2mW. The very low power requirement contributes to the excellent thermal and gain error matching between the four DAC's.

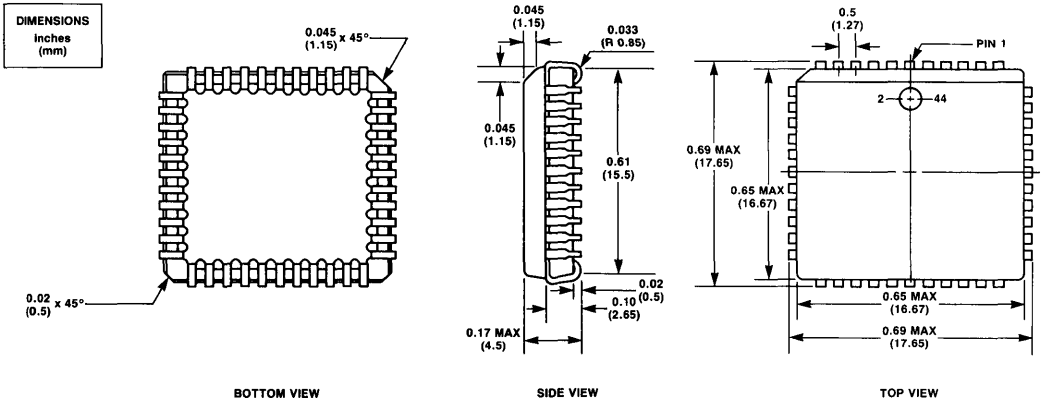
PACKAGE OUTLINE (DIP)



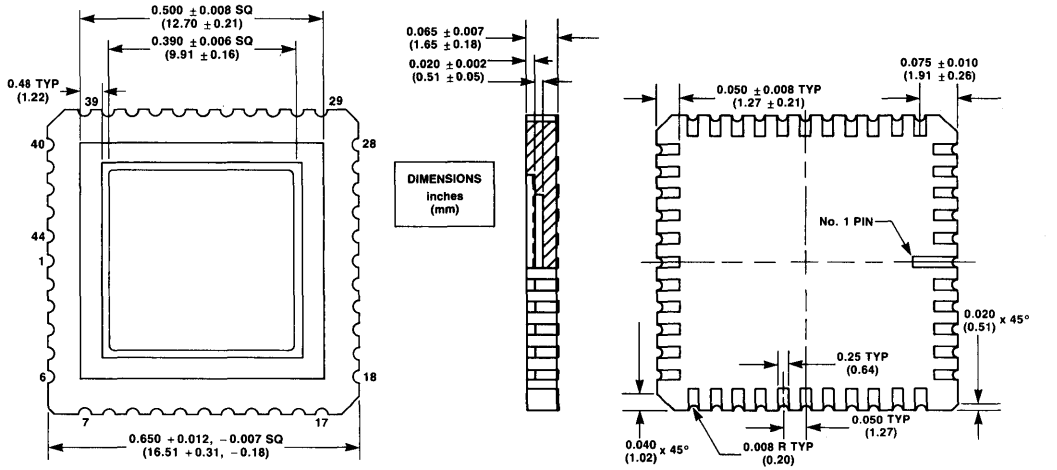
PACKAGE OUTLINE (PDIP)



PACKAGE OUTLINE (PLCC)



PACKAGE OUTLINE (LCC)



HS 7584 CONTROL INPUTS

A_0	A_1	$\overline{CS}$	$\overline{WR1}$	B1/$\overline{B2}$	$\overline{WR2}$	$\overline{XFER}$	HS 7584 OPERATION DESCRIPTION
0	0	0	0	1	1	1	Address DAC A register and loads data (register only)
1	0	0	0	1	1	1	Address DAC B register and loads data (register only)
0	1	0	0	1	1	1	Address DAC C register and loads data (register only)
1	1	0	0	1	1	1	Address DAC D register and loads data (register only)
X	X	X	X	X	0	0	Transfers data from first registers to all DAC's
X	X	1	X	X	X	X	No updated information
X	X	X	1	X	X	X	No updated information

HS 7584 Truth Table 12-Bit Parallel Load

HS 7584 CONTROL INPUTS

A_0	A_1	$\overline{CS}$	$\overline{WR1}$	B1/$\overline{B2}$	$\overline{WR2}$	$\overline{XFER}$	HS 7584 OPERATION DESCRIPTION
0	0	0	0	1	1	1	Address DAC A register and loads data (register only)
0	0	0	0	0	1	1	Address DAC A register and updates lower 4 Bits
1	0	0	0	1	1	1	Address DAC B register and loads data (register only)
1	0	0	0	0	1	1	Address DAC B register and updates lower 4 Bits
0	1	0	0	1	1	1	Address DAC C register and loads data (register only)
0	1	0	0	0	1	1	Address DAC C register and updates lower 4 Bits
1	1	0	0	1	1	1	Address DAC D register and loads data (register only)
1	1	0	0	0	1	1	Address DAC D register and updates lower 4 Bits
X	X	X	X	X	0	0	Transfers data from first registers to all DAC's
X	X	1	X	X	X	X	No updated information
X	X	X	1	X	X	X	No updated information

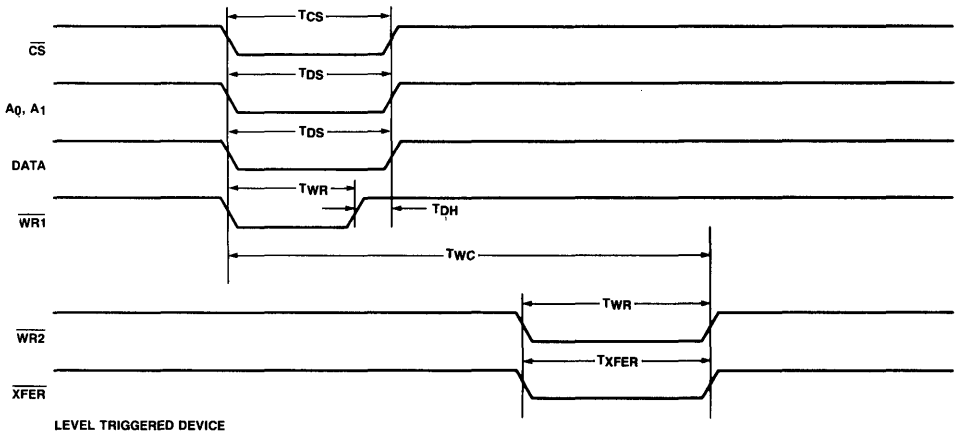
HS 7584 Truth Table 12-Bit Parallel Load

CONTROL FUNCTIONS

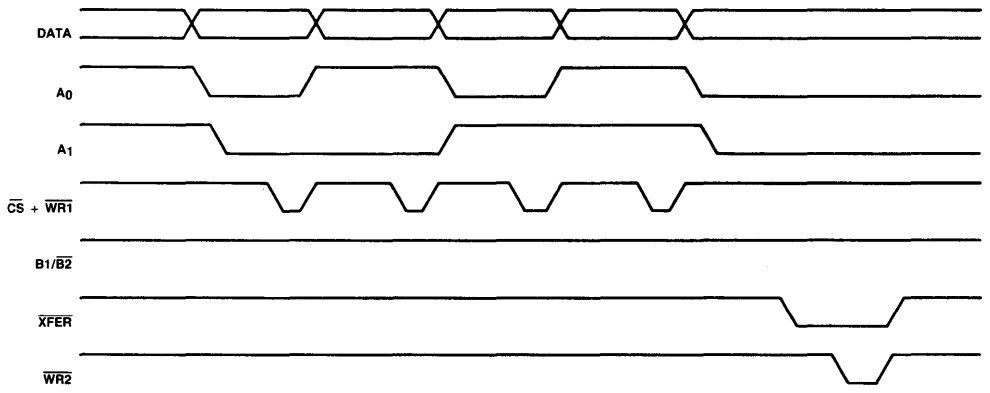
PIN	FUNCTION
A_0	Address 0 for DAC selection
A_1	Address 1 for DAC selection
$\overline{CS}$	Enables DAC input and A_0, A_1 (along with $\overline{WR1}$) for writing (Active low)
$\overline{WR1}$	Enables A_0, A_1 (along with $\overline{CS}$), active low, gated with $\overline{CS}$
B1/$\overline{B2}$	Selects high and low bytes. In 12-Bit mode, B1/$\overline{B2}$ tied high; In 8-Bit mode, a 12-Bit word is loaded into first register when B1/$\overline{B2}$ is high, and a 4-Bit word is updated to the lower bits when B1/$\overline{B2}$ is low.
$\overline{WR2}$	Gated with $\overline{XFER}$, used to load all DAC's simultaneously (Active low)
$\overline{XFER}$	Gated with $\overline{WR2}$, used to load all DAC's simultaneously (Active low)

TIMING CHARACTERISTICS

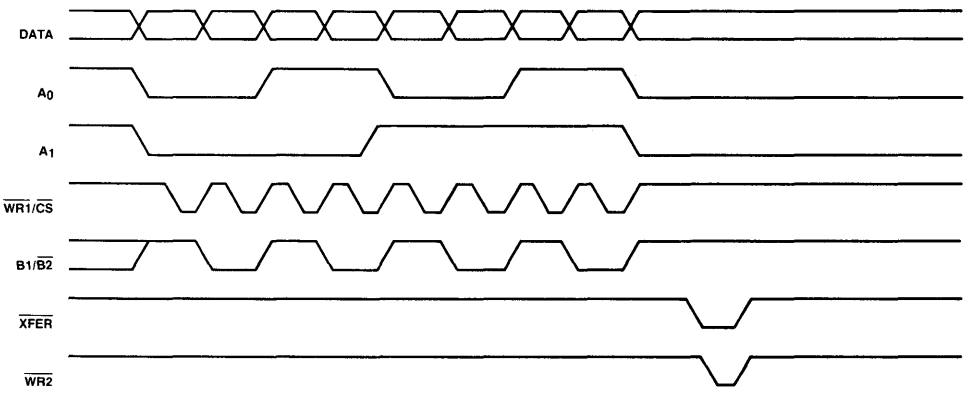
PARAMETER	LIMIT AT T_A = +25°C	LIMIT AT −55°C to +125°C	UNITS	
T_{DS}	100 min	125 min	ns	Data Set Up Time (To rising edge of $\overline{WR1}$ command)
T_{DH}	0 min	0 min	ns	Data Hold Time
T_{WR}	100 min	120 min	ns	Write Pulse Width
T_{CS}	100 min	125 min	ns	Chip Select Width
T_{XFER}	100 min	120 min	ns	Transfer Pulse Width
T_{WC}	200 min	245 min	ns	Total Write Command



Write Cycle Timing Diagram

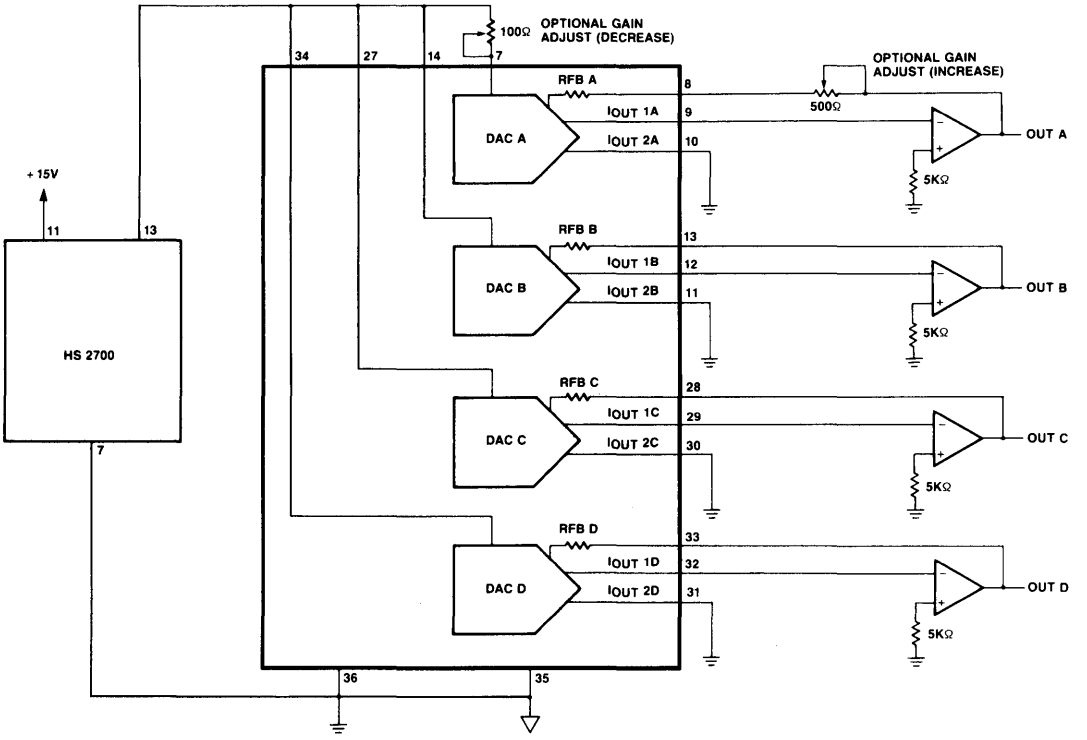


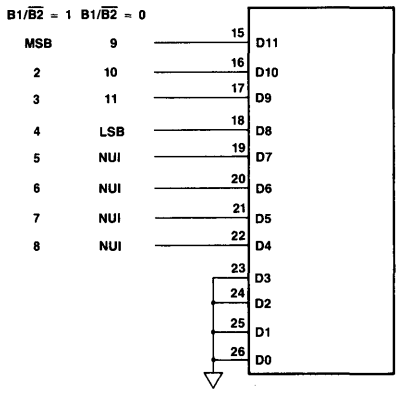
Typical Interface with a 12-Bit Data Bus



Typical Interface with an 8-Bit Data Bus

UNIPOLAR OPERATION





NUI = No Updated information. During the second load cycle, the information on pins 15 thru 18 will be loaded into the lower bits of the first register; information on pins 19 through 22 will not be recognized. Note: Upper 8 bits should be loaded first, then lower bits.

8-Bit Bus Configuration

OFFSET AND GAIN ADJUSTMENT

Offset Adjust. Since the maximum output leakage is 200nA (over temperature range) the offset voltage, due to the DAC, would be ± 1.4mV. This, plus any offset's due to the op-amp, could be nulled out by the offset adjust circuit given by the op-amp manufacturer. The 5KΩ resistor, from the positive summing junction to ground, reduces offset voltages due to bias currents of the op-amp. They may be eliminated if cost factors out ways offset demands.

Gain Adjust. The circuit may be modified which would lead the user to adjusting gain. A 100 Ohm trimpot in series between the reference and reference input would allow for a 0 to − 1.4% adjustment range in gain. A 500 Ohm trimpot in series with the feedback resistor to output of the op-amp would allow for a 0 to + 7% adjustment range.

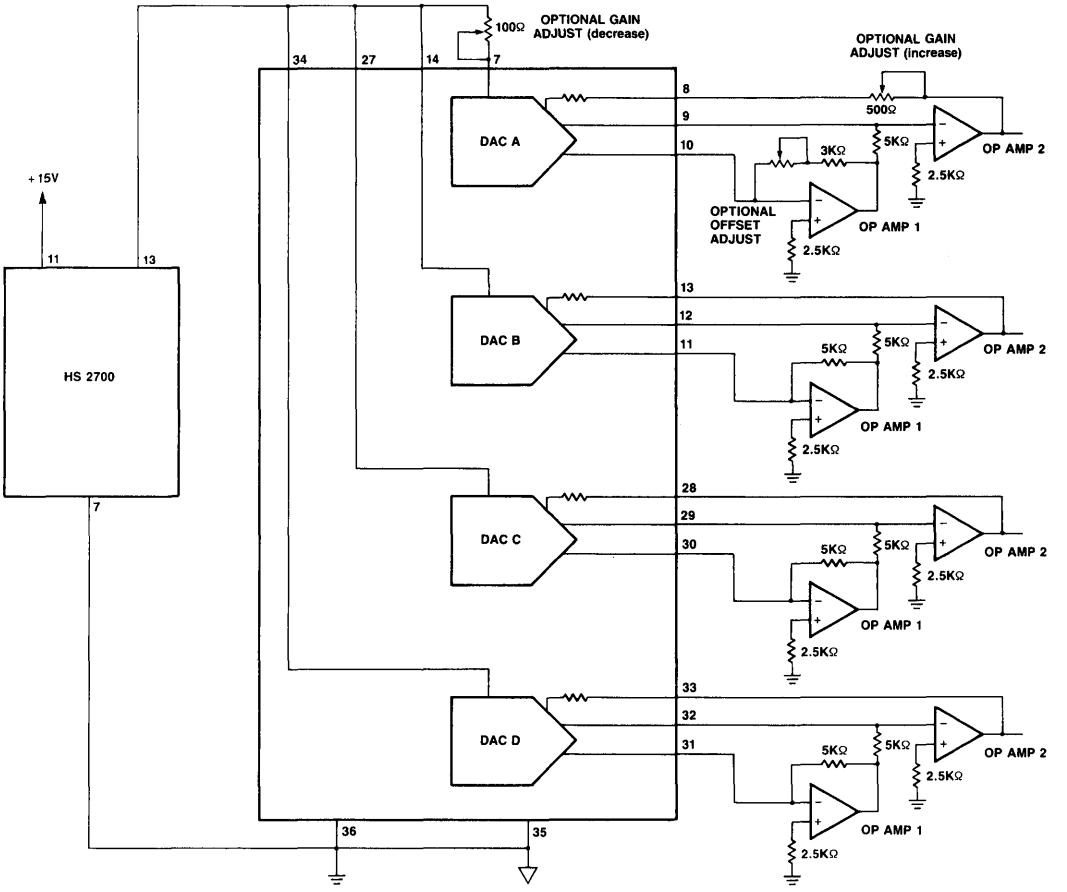
Note: Trimpots reduce stability coefficients given in specifications and should be used only in cases where the specified end point accuracy is not sufficient.

Coding: Straight Binary

INPUT MSB LSB	OUTPUT
0000 0000 0000	0
0000 0000 0001	1 LSB
0111 1111 1111	$-V_{REF}/2$ − 1 LSB
1000 0000 0000	$-V_{REF}/2$
1000 0000 0001	$-V_{REF}/2$ + 1 LSB
1111 1111 1111	$-V_{REF}$ + 1 LSB

$$1\ LSB = \frac{-V_{REF}}{2^{12}}$$

BIPOLAR OPERATION



OFFSET AND GAIN ADJUSTMENT

Offset Adjust. The resistor in feedback loop of the first op-amp can be a 3KΩ resistor in series with a 5KΩ trimpot. This will give enough adjustment range to match the absolute tolerance of the DAC's resistors. Apply a 1 MSB and all 0's code and adjust for 0.000 Volts.

Gain Adjust. The circuit may be modified which would allow the user to adjust gain. 100 Ohm trimpots in series between the reference and reference input would allow for a 0 to −1.4% adjustment range. A 500 Ohm trimpot in series with the feedback resistor of the second op-amp would allow for a 0 to +7% adjustment range.

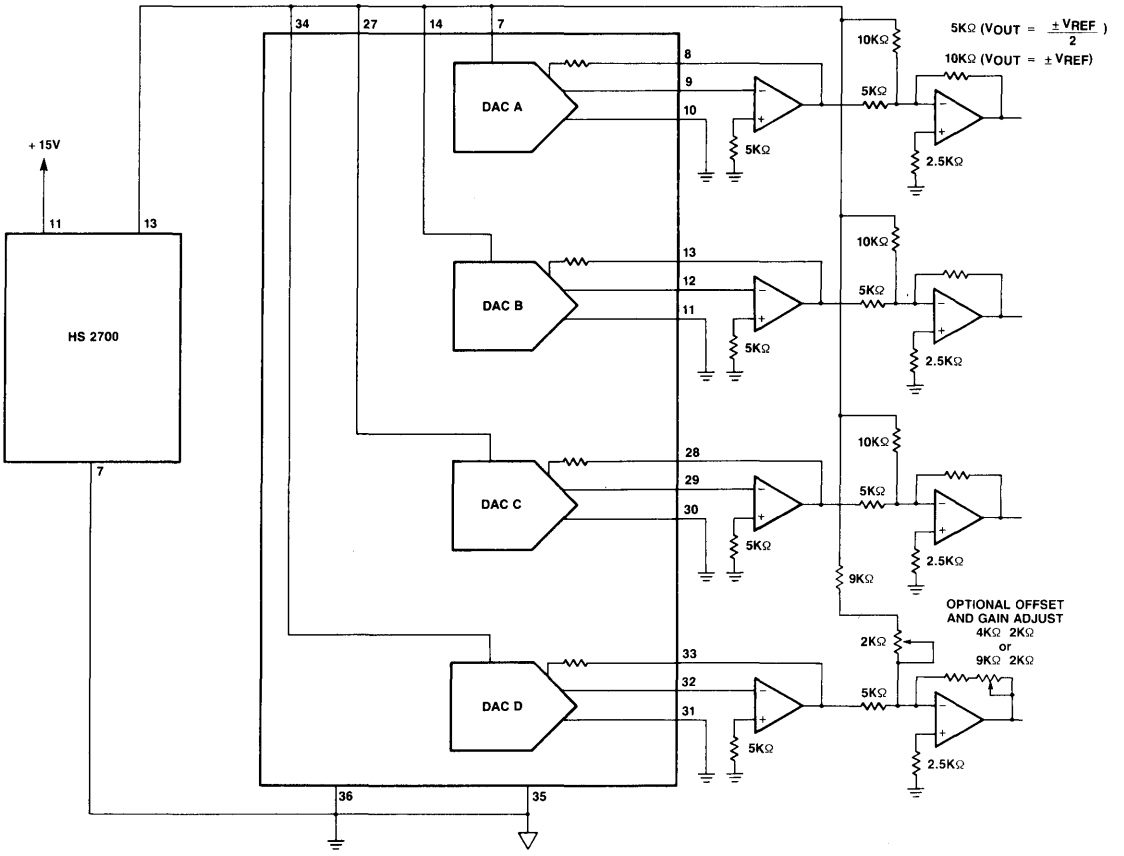
Note: Trimpots reduce stability coefficients given in specifications and should be used only in cases where the specified end point accuracy is critical.

Coding: Complementary Binary

INPUT MSB LSB	OUTPUT
0000 0000 0000	V_{REF}
0000 0000 0001	V_{REF} − 1 LSB
0111 1111 1111	0 − 1 LSB
1000 0000 0000	0
1000 0000 0001	0 + 1 LSB
1111 1111 1111	$-V_{REF}$ − 1 LSB

$$1\ LSB = \frac{V_{REF}}{2^{12}}$$

BIPOLAR OPERATION



OFFSET AND GAIN ADJUSTMENT

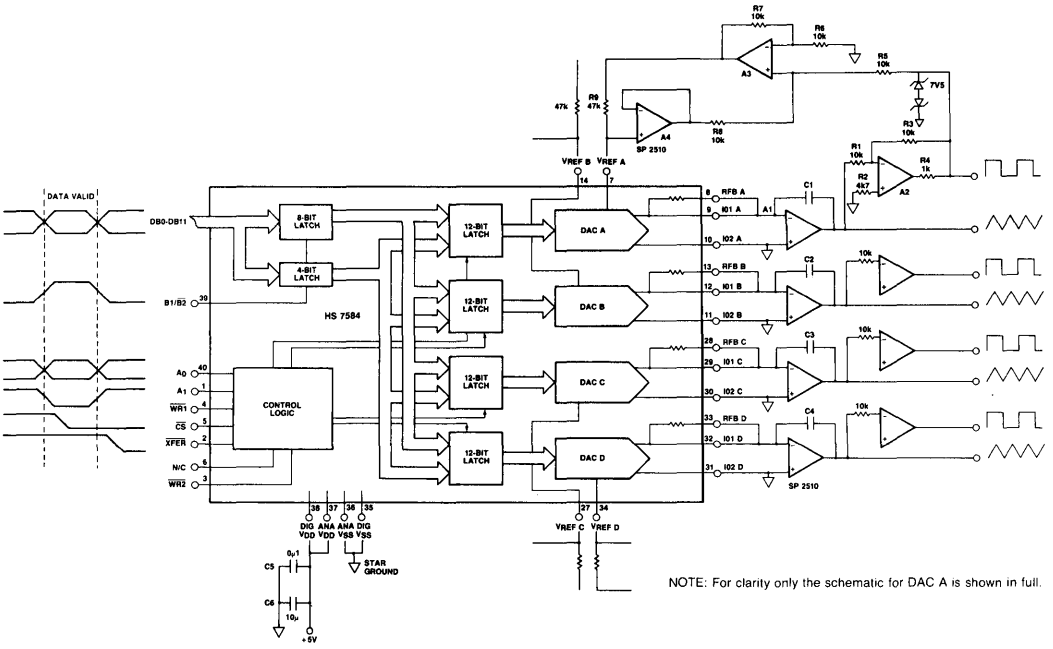
Offset Adjust. The resistor from V_{REF} to the negative summing junction of the second op-amp can be a 9KΩ resistor in series with a 2KΩ trimpot. This will give a ±10% adjustment range. Apply a 1000 0000 0000 code and adjust for 0.000 Volts.

Gain Adjust. Gain adjust should be performed after offset adjust and is done by utilizing a trimpot in the feedback loop of the second op-amp. Apply all ones digital input code and adjust for $+V_{REF} - 1$ LSB. A 4.0KΩ resistor in series with 2KΩ trimpot will adjust out any errors, for $\pm V_{REF}/2$, or a 9KΩ resistor in series with a 2KΩ trimpot for $\pm V_{REF}$.

Note: Trimpots reduce stability coefficients given in specifications and sould be used only in cases where the specified end point accuracy is not sufficient.

Coding: Straight Binary

INPUT	OUTPUT	
MSB LSB	10KΩ FEEDBACK	5KΩ FEEDBACK
0000 0000 0000	$-V_{REF}$	$-V_{REF}/2$
0000 0000 0001	$-V_{REF} + 1$ LSB	$-V_{REF}/2 + 1$ LSB
0111 1111 1111	0 − 1 LSB	0 − 1 LSB
1000 0000 0000	0	0
1111 1111 1111	$+V_{REF} - 1$ LSB	$+V_{REF}/2 + 1$ LSB
	$1\text{ LSB} = \frac{2\,V_{REF}}{2^{12}}$	$1\text{ LSB} = \frac{V_{REF}}{2^{12}}$



TRIANGLE/SQUAREWAVE GENERATOR

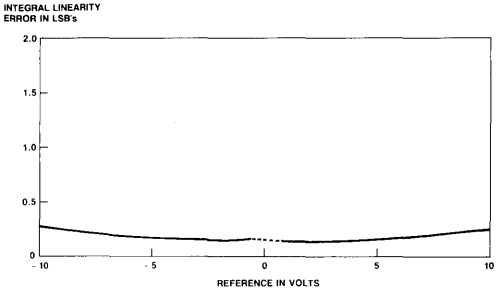
TRIANGLE/SQUAREWAVE GENERATOR

A programmable triangle/squarewave generator can easily be implemented utilizing the HS 7584, providing micropressor control of multiple signal sources.

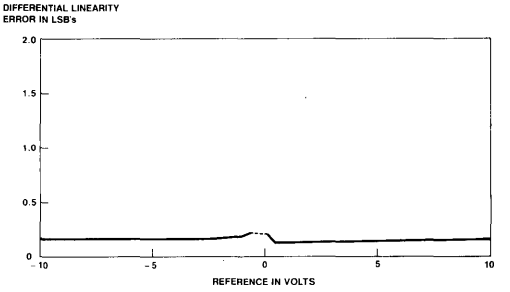
The outputs are derived from an 8-Bit or 12-Bit source determined by the state of B1/$\overline{B2}$. In a 12-Bit system this control line should be tied high. The digitally controlled integrator has a frequency determined by:

$$f = \frac{\text{Digital Input}}{4\,RC}$$

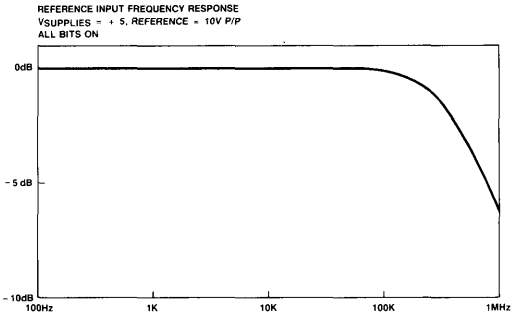
C is the value of C_1 to C_4 and R is the resistance of the DAC. With the four DACs on a single chip the resistance matching is excellent resulting in very stable timing relationships at the generator outputs. The output of the comparator A_2 determines whether the constant current source provided by A_3 and A_4 is positive or negative. The system performance is determined by the selection of the amplifiers A_1, A_2, A_3 and A_4. For good high frequency performance the SP 2510 has been used. The SP 2510 has a slew rate of 65V/ μs and settles to 0.1% of the final output in 0.25 μs.



Integral Linearity Error Vs. Reference Voltage
Typical Results For 5V Supply



Differential Linearity Error Vs. Reference Voltage
Typical Results For 5V Supply



7

ORDERING INFORMATION

MODEL	DESCRIPTION	TEMPERATURE RANGE	PACKAGE	SCREENING
HS 7584C	12-Bit Quad DAC	0 to +70°C	40 Pin DIP	—
HS 7584C/LCC	12-Bit Quad DAC	0 to +70°C	44 Pin LCC	—
HS 7584B	12-Bit Quad DAC	−55°C to +125°C	40 Pin DIP	MIL-STD-883C
HS 7584B/LCC	12-Bit Quad DAC	−55°C to +125°C	44 Pin LCC	MIL-STD-883C
HS 7584C/PLCC	12-Bit Quad DAC	0 to +70°C	44 Pin PLCC	—
HS 7584C/PDIP	12-Bit Quad DAC	0 to +70°C	40 Pin PDIP	—

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Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP9316

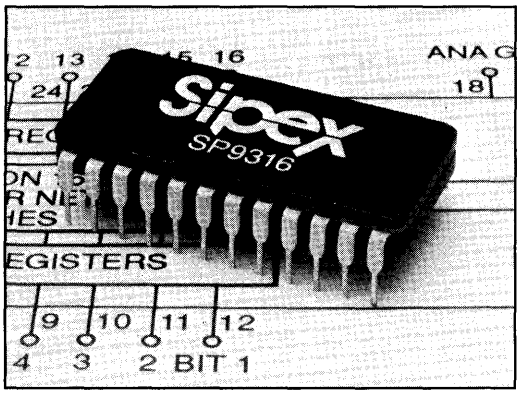
16-BIT MONOLITHIC MDAC

FEATURES

- Monolithic Construction
- Low Power (60 mW)
- Input Registers
- Single Supply Operation
- Low Cost

DESCRIPTION

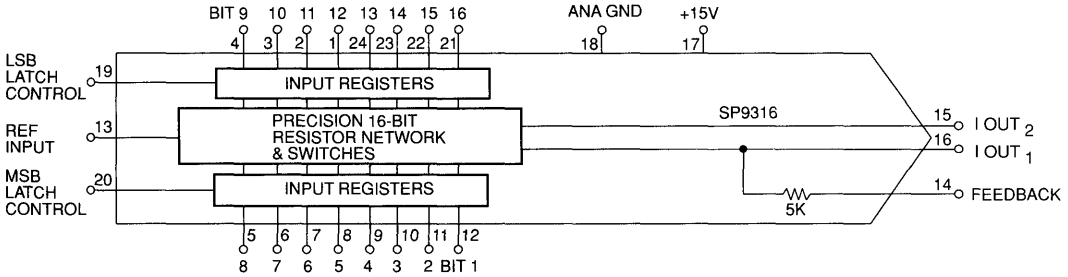
The SP9316 is a 16-bit, monolithic CMOS, multiplying digital-to-analog converter with two 8-bit input registers for direct microprocessor interface. The SP9316 offers two and four quadrant multiplying capability with TTL/DTL and CMOS logic compatibility. Operating from a single +15V supply, power consumption is less than 60 mW. Its high accuracy and monotonicity is achieved without laser trimming through the use of a highly accurate, low TCR thin film resistor process. A unique digital decoding technique of the 4 MSB's results in excellent linearity and stability over time and temperature.



Packaged in a hermetic 24-pin ceramic or molded plastic. The SP9316 is specified for operation from 0°C to 70°C for commercial grades and -55°C to +125°C for military grades.

7

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @25°C, nominal power supply, VREF=10V, Unipolar unless otherwise noted)

MODEL	SP9316C-4			SP9316C-5			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUT							
Resolution	16			*			Bits
2-Quad Unipolar Coding		Binary			*		
4-Quad Bipolar Coding		Offset Binary			*		
Input High Voltage	2.4		V_{DD}				V
Input Low Voltage	-0.3		0.8				V
Input Current[1]		±1	±10				µA
Input Capacitance[2]			8				pf
REFERENCE INPUT							
Voltage Range		±25			*		V
Input Impedance	2.5	5k	7.5		*		KΩ
ANALOG OUTPUT							
Offset Error[3]			50			*	µV
Gain Accuracy[4]		0.1	0.2		*		%FSR
Small Signal 3 dB Bandwidth		1			*		MHz
Output Capacitance Cout1		90			*		pf
Cout2		70			*		pf
STATIC PERFORMANCE							
Integral Linearity[5]			±0.006			±0.003	%FSR
Differential Linearity			±0.006			±0.003	%FSR
SWITCHING CHARACTERISTICS							
Strobe Width	80	60					nsec
Data Set-Up Time	80	70					nsec
Data Hold Time	40	20					nsec
STABILITY[4]							
Gain[6]		±1	±4			*	ppm/°C
Offset			+1			*	ppm/°C
Integral Nonlinearity		0.1	±1			*	ppm/°C
Monotonicity Guaranteed	14			15			Bits
LONG TERM STABILITY							
Differential Nonlinearity		1			*		ppm/°C
Offset		±0.5			*		ppm/°C
Gain		±1			*		ppm/°C
POWER SUPPLY							
Voltage Range VDD	+5	+15	+16				V
Rejection Ratio (14-16V)		±0.0001	±0.002			*	%/%
Power Dissipation			60			*	mW
Supply Current IDD		2	4				mA
IDD		0.2	1				mA
TEMPERATURE RANGE							
Operating (7)	0		70	*		*	°C
Storage	-55		85	*		*	°C

NOTES

1. Logic inputs are MOS gates. I in typical is less than 1 nA @ 25°C.
2. Guaranteed by design not production tested.
3. Unipolar: Using the Internal Rfeedback with nulled external amplifier in a constant 25°C ambient (offset doubles every 10°C).
4. Using internal feedback resistor.
5. Integral Linearity, for this product, is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input combination.

   Differential Linearity is the deviation of an ouput step from the theoretical value of 1 LSB for any two adjacent digital input codes.
6. The SP9316 series is designed to be used only in those applications where the current output is virtual ground; i.e. the summing junction of an op-amp in the inverting mode. The internal feedback resistor must be used to achieve temperature tracking. See applications information for recommended circuit configurations.
7. For military temperature range devices, please consult factory.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are subject to sample testing only.
VDD = +15V, VREF = 10V

MODEL	SP9316C-4			SP9316C-5			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
PROPAGATION DELAY[1]		300			*		nsec
CURRENT SETTLING TIME							
Major Code Settling to:							
0.01% FSR (strobed)		2			*		µsec
0.00076% FSR (strobed)		3			*		µsec
OUTPUT CAPACITANCE							
CI01 Digital Inputs VIH		170					pf
CI02 Digital Inputs VIH		30					pf
CI03 Digital Inputs VIL		80					pf
CI04 Digital Inputs VIL		100					pf
GLITCH ENERGY[2]		250			*		nVsec
MULTIPLYING FEEDTHROUGH ERROR							
At I01		3[3]			*		mV p-p
		0.3[4]			*		mV p-p

NOTES

1. I01 load R = 100Ω, (ext 13 pf; all data inputs 0V to VDD or VDD to 0V. From 50% digital input change to 90% of final analog output.
2. VREF = 0V, DAC Register Alternately loaded with all 0's and 1's.
3. VREF = 20 Vpp, f = 10 kHz sine wave.
4. VFEF = 20 Vpp, f = 1 kHz sine wave.

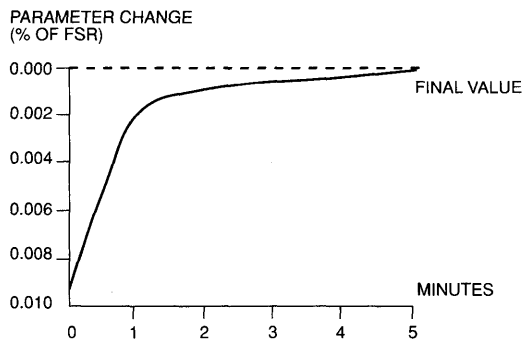


FIGURE 1
WARM UP DRIFT

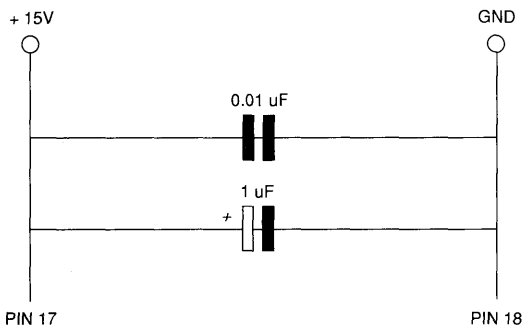


FIGURE 2
RECOMMENDED BYPASS CIRCUIT

PIN ASSIGNMENTS

PIN	FUNCTION
1	Bit 12
2	Bit 11
3	Bit 10
4	Bit 9
5	Bit 8
6	Bit 7
7	Bit 6
8	Bit 5
9	Bit 4
10	Bit 3
11	Bit 2
12	Bit 1 (MSB)
13	Ref In
14	R feedback
15	I out 2
16	I out 1
17	+15V
18	Analog GND
19	LSB Latch
20	MSB Latch
21	Bit 16 (LSB)
22	Bit 15
23	Bit 14
24	Bit 13

ABSOLUTE MAXIMUM RATINGS

(TA = 25°C unless otherwise noted)

VDD to GND	-0.3V, +17V
Digital Input Voltage to GND	-0.3V, VDD +0.3V
VREF or VRFB to GND	±25V
Output Voltage (PIN 15, PIN 16)	-0.3V, VDD +0.3V
Power Dissipation (Any Package) to +75°C	450 mW
Derates above 75°C by	6 mW/°C
Dice Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C

CAUTION

1. Do not apply voltages higher than VDD or less than GND potential on any terminal other than VREF or RFB.
2. The digital inputs are diode clamp protected against ESD damage. However, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all time until ready to use.
3. Use proper anti-static handling procedures.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied.

APPLICATIONS INFORMATION

THEORY OF OPERATION

The SP9316 can be configured for unipolar voltage operation (2-quadrant Multiplication) and bipolar voltage operation (4-quadrant Multiplication). Coding is binary and offset binary respectively. In bipolar operation both the reference signal and the number represented by the digital input applied to the MDAC may be either positive or negative polarity.

Individual latch controls are provided for the high and low bytes which may be tied together for single 16-bit word update. The data is latched with the strobe at logic 0. The latches are level triggered and can be made transparent. However, use of the latches is recommended in most applications as they significantly reduce data bit skew to low glitch performance.

STROBE	FUNCTION
0	Data Latched (held)
1	Data Changing (transfer)

Table 1

UNIPOLAR OPERATION
Transfer Characteristics

BINARY INPUT	ANALOG OUPUT
111 . . . 111	$-V_{REF}(1-2^{-N})$
100 . . . 001	$-V_{REF}(1/2+2^{-N})$
100 . . . 000	$-V_{REF}/2$
011 . . . 111	$-V_{REF}(1/2-2^{-N})$
000 . . . 001	$-V_{REF}(2^{-N})$
000 . . . 000	0

BIPOLAR OPERATION
Transfer Characteristics

OFFSET BINARY INPUT	ANALOG OUTPUT
111 . . . 111	$-V_{REF}(1-2^{-(N-1)})$
100 . . . 001	$-V_{REF}(2^{-(N-1)})$
100 . . . 000	0
011 . . . 111	$V_{REF}(2^{-(N-1)})$
000 . . . 001	$V_{REF}(1-2^{-(N-1)})$
000 . . . 000	V_{REF}

TIMING INFORMATION

Figure one details the SP9316 timing. If a transparent latch is required the latch control can be tied to logic 1.

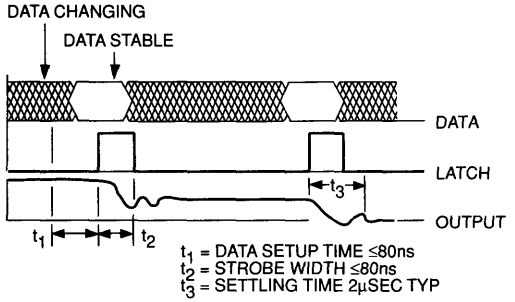


FIGURE 3
TIMING DIAGRAM

UNIPOLAR OPERATION

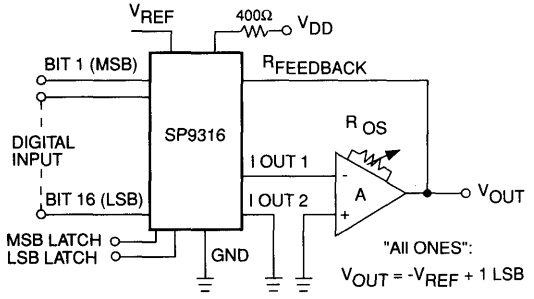


FIGURE 4

NOTE: To maintain specified linearity, the external amplifier (A) must be zeroed. Apply on ALL "ZEROES" digital input and adjust R_{OS} for $V_{OUT} = 0 \pm 1$ mV.

BIPOLAR OPERATION

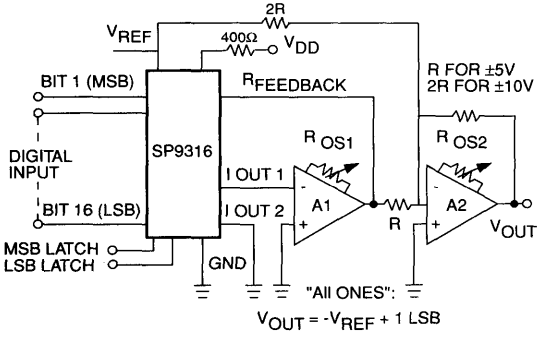


FIGURE 5

NOTE: To maintain specified linearity, external amplifiers (A_1 and A_2) must be zeroed. With a digital input of 10 . . . 0 and V_{REF} set to zero:

a) Set R_{OS1} for $V_{01} = 0$
b) Set R_{OS2} for $V_{OUT} = 0$
c) Set V_{REF} to +10V and adjust R_B for V_{OUT} to be 0 volts.

AMPLIFIER SELECTION

The SP9316 allows the engineer to design the optimum voltage output 16-bit digital-to-analog system for each application. Selection of the correct operational amplifier is critical to the success of the design.

To obtain the optimum linearity performance, the amplifiers must have an open loop gain in excess of 100 000 or 100 dB. The SP2600 series op-amps may be considered for specific applications as the requirement is met with a specification of 150 000.

Care should be taken to ensure that the summing junction is as close to analog ground as can be achieved. Most applications demand that this offset is kept to below 100μV.

To maintain accuracy over temperature, amplifiers should have low bias currents and offset voltage temperature coefficients.

In bipolar applications, attention must be paid to the choice of resistors R and 2R (see figure 5). As the analog voltage output increases from zero to full-scale, the power dissipated by the feedback resistor increases and the resistor heats up. This causes a small change in the resistance value which could lead to an alteration to the transfer function and which may be seen as integral linearity errors.

The resistor network has been designed using ultra-stable thin-film nichrome. It is important that the external resistors come as close as possible to meeting the stringent temperature coefficient displayed by the DAC internal resistances. Resistors with a temperature coefficient of 10ppm/°C or better should be used.

LAYOUT, GROUNDING AND GUARDING

16-bit system performance can be maintained with attention paid to the layout, grounding and guarding techniques employed.

All grounds should be of as low resistance as the layout allows. Analog and digital grounds should be individually star-pointed and tied together as close as possible to the measurement point.

Good layout techniques dictate that high speed digital inputs should be kept separate from low level analog outputs.

The DAC output and op-amps inputs are high impedance and so are sensitive to interference from the digital input lines. Careful pinout design of the SP9316 has reduced this problem to a minimum but guarding of these points should be considered. Figures six and seven detail the low impedance guard track layout.

7

LONG TERM DRIFT

All stability measurements require great attention to detail. When measuring the stability of the SP9316 great care should be taken to ensure that the drift of the measurement instruments can be separated from the device drift and that all measurements are taken at identical temperatures.

The long term drift of a SP9316 voltage output system transfer function, after initial op-amp trim, will largely be determined by the choice of the external components.

For minimum offset error the op-amps should be trimmed after one hour of continuous operation. The SP9316 contribution to the offset drift after that time will be ±0.1ppm/°C per 1000 hours.

The long term gain drift error contribution of the SP9316 is ±1 ppm/°C per 1000 hours. Also to be considered is the temperature coefficients of the external resistors, the op-amp drift specifications and the stability of the reference. The HS2700 LD with a stability of 3ppm/°C is recommended.

The unique SP9316 network results in an exceptionally low linearity drfit with time. Typical differential linearity drift is 0.1ppm/°C.

UNIPOLAR

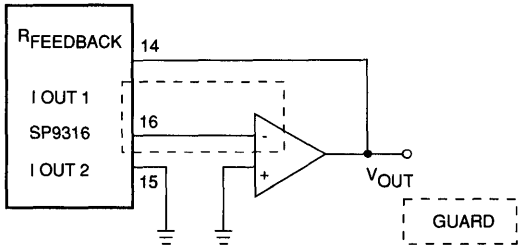


FIGURE 6

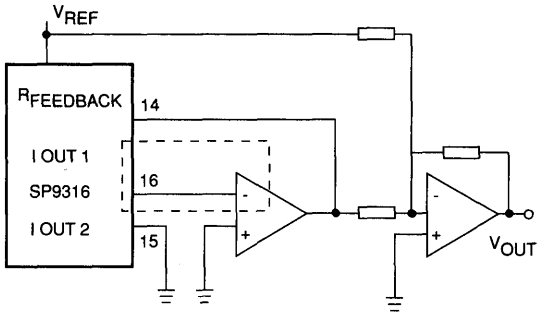


FIGURE 7

DIGITAL CONTROL LOW PASS FILTER

The SP9316 multiplying DAC can be used to construct active filters which display very low noise and distortion characteristics. Low pass filters can be built to give the engineer control over center frequency, gain and Q-factor. The SP9316 is an ideal high resolution element for this application.

Figure eight shows a low pass filter designed to be independent of the resistance of the SP9316 DAC network by using it as a programmable gain element. The filter characteristic is given by:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R3}{R1}\left(\frac{1}{1+j\ w\ \frac{R3\ R4\ C}{R2\ D}}\right)$$

where D is the binary code applied to the DAC and C is the value of the capacitor.

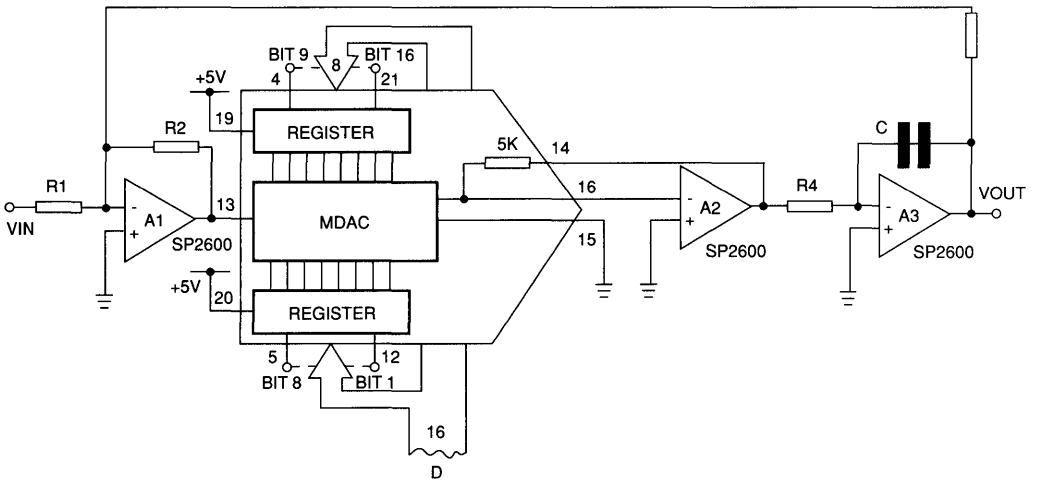


FIGURE 8
DIGITALLY CONTROLLED LOW PASS FILTER

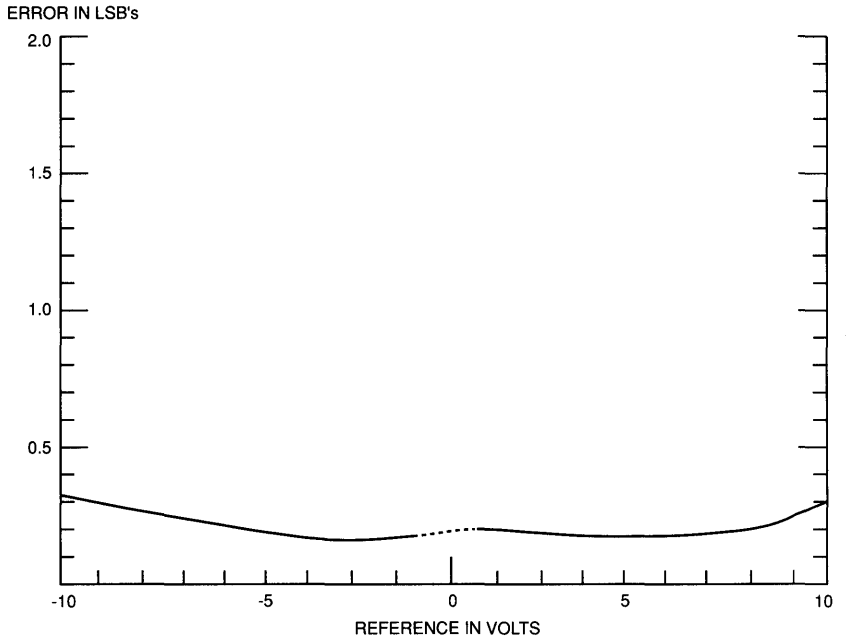
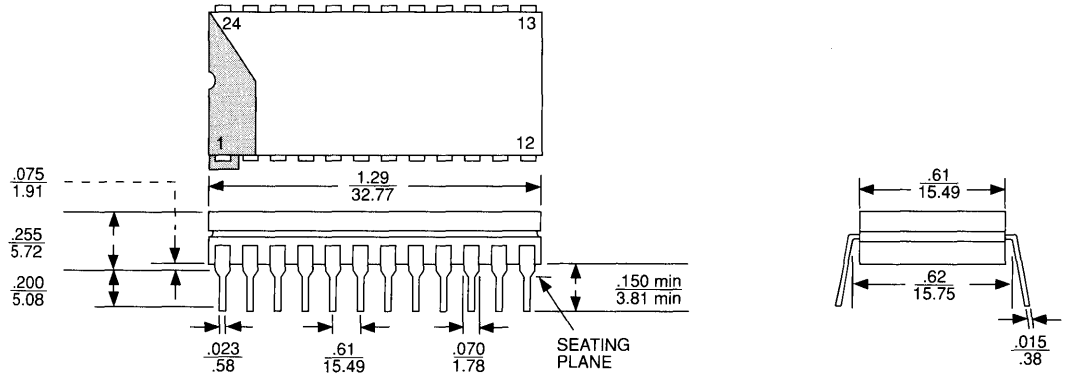


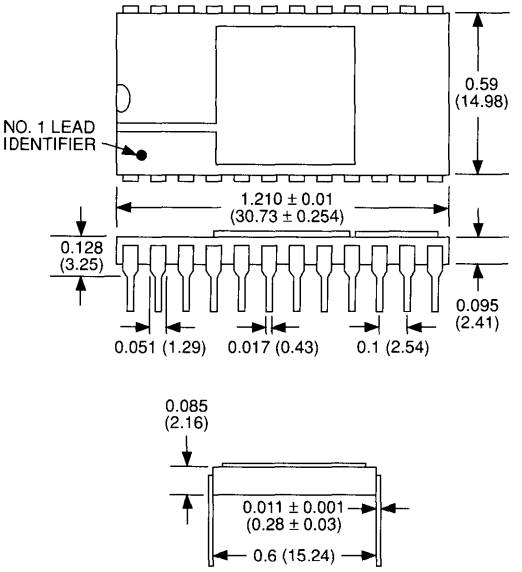
FIGURE 9
SP9316 LATCHED MDAC
INTEGRAL LINEARITY ERROR VS. PERFORMANCE VOLTAGE
TYPICAL RESULTS @ +25°C AND NOMINAL +15V

PACKAGE OUTLINE

24 PIN CERDIP



24 PIN SIDE BRAZE



NOTES

1. In lieu of cerdip package Sipex reserves the right to ship side braze packaged parts.
2. All dimensions max unless otherwise noted.

ORDERING INFORMATION

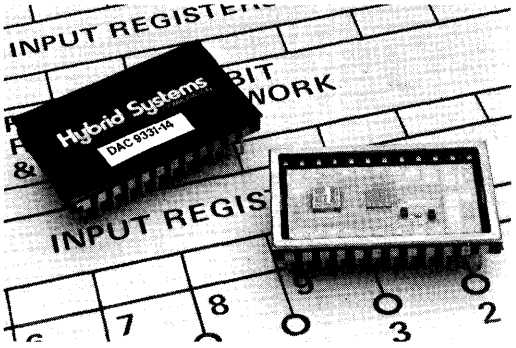
MODEL NUMBER	DESCRIPTION	TEMPERATURE RANGE	SCREENING
SP9316C-4	14-Bit Linearity MDAC	0°C to 70°C	—
SP9316C-5	15-Bit Linearity MDAC	0°C to 70°C	—

DAC9331-14

14-BIT MULTIPLYING DAC

FEATURES

- 14-bit resolution and accuracy
- 2 and 4-quadrant multiplication
- Precision laser trimmed ladder
- Low power
- Single power supply operation
- Reliable



DESCRIPTION

The DAC9331-14 is a low cost 14-bit multiplying digital-to-analog converter packaged in a unique 24-pin double DIP. Capable of 2 and 4-quadrant multiplication, the unit is TTL/DTL and CMOS compatible with power consumption less than 30mW. Power supply options include +5V (-1) or +15V (-2). Outstanding features of the DAC9331-14 include:

True 14-Bit Performance — Up to 14-bit resolution and accuracy over the 0 to 70°C operating range.

2 And 4-Quadrant Multiplication — Reference input range to ±25 volts.

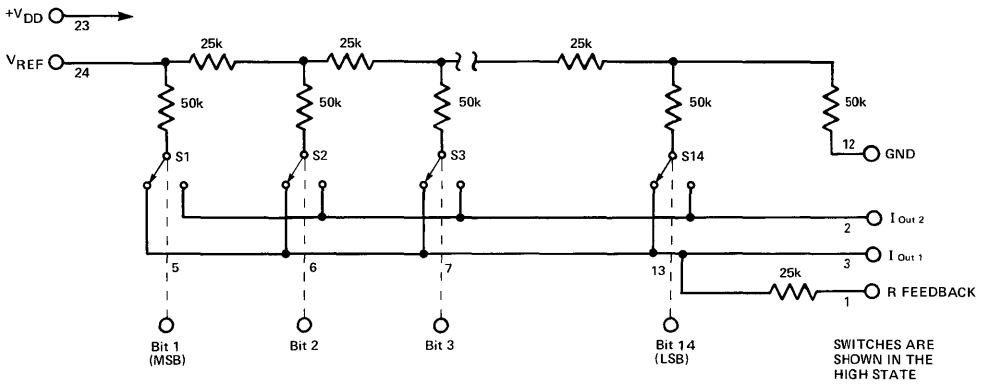
Low Power — CMOS technology provides less than 30mW total power dissipation — a real battery saver.

Reliability Plus — Packaged in a unique enclosure which has undergone extensive environmental testing during its development, the DAC9331-14 is continuously monitored during all assembly and test operations by our quality control organization.

Reliability is enhanced by batch-processed, precision laser-trimmed resistor networks fabricated in our own facility. Similar to monolothic circuits, the networks are processed and functionally trimmed to assure consistent performance. Networks are glass passivated to assure reliability under adverse environmental conditions.

7

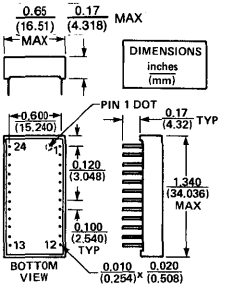
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C and nominal power supply, V_{REF} = +10V, unless otherwise noted)

MODEL	DAC9331-14
TYPE	Multiplying
DIGITAL INPUT	
Resolution	14-Bits
2-Quad, Unipolar Coding	Binary
4-Quad, Bipolar Coding	Offset Binary
Logic Compatibility	DTL, TTL, CMOS
Logic Thresholds	V_{IH}=3.5V (min), V_{IL}=1.0V(max)[1]
Input Leakage Current	±1μA (max)
REFERENCE INPUT	
Voltage Range	±25V (max)
Input Impedance	25kΩ
ANALOG OUTPUT	
Gain Accuracy[2]	0.1%
Offset[3]	50μV (max)
Output Leakage	40nA (max)
Small Signal	
3dB Bandwidth	600kHz (min)
Output Capacitance	
C_{out1}	100pF (max) all inputs high
C_{out2}	30pF (max) all inputs high
C_{out1}	30pF (max) all inputs low
C_{out2}	100pF (max) all inputs low
STATIC PERFORMANCE	
Integral Linearity[4]	±½LSB (max)
Differential Linearity	±½LSB (typ), ±1LSB (max)
DYNAMIC PERFORMANCE	
Major Carry Transition Settling to ±0.05%	3.0μS (max)
Reference Feedthrough Error (Vref=20Vpp @ 10kHz)	10mVpp
STABILITY[3] (Over Specified Temp. Range)	
Scale Factor[5]	±3ppm/°C F.S.R. (max)
Linearity	±3ppm/°C F.S.R. (max)
Differential Linearity	±2ppm/°C F.S.R. (max)
POWER SUPPLY (V_{DD})[6]	
Voltage Range @ Current	
-1 Option	+5V (nom); +4.75V to +7V @ <1mA
-2 Option	+15V (nom); +11.5V to +15,5V @ 2mA
Rejection Ratio	0.005%/% (typ), 0.007%/% (max)
Total Dissipation (inputs at GND)	30mW (max)
TEMPERATURE RANGE	
Operating	0°C to +70°C
Storage	0°C to +85°C
MECHANICAL	
Case Style	24-pin double-DIP
Case Dimensions	



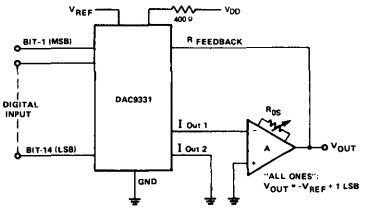
PIN	FUNCTION	PIN	FUNCTION
1	R FEEDBACK	24	V_{REF}
2	I_{OUT} 2	23	+V_{DD}
3	I_{OUT} 1	22	BIT 5
4	N.C.	21	BIT 6
5	BIT 1 (MSB)	20	BIT 7
6	BIT 2	19	BIT 8
7	BIT 3	18	BIT 9
8	BIT 4	17	BIT 10
9	N.C.	16	BIT 11
10	N.C.	15	BIT 12
11	N.C.	14	BIT 13
12	GROUND	13	BIT 14 (LSB)

Note: N.C. means no connection

NOTES:
1. The switching threshold is typically $V_{DD}/2$ for -1 models and $V_{DD}/6$ for -2 models. The logic input must never exceed $V_{DD}/3$ for -2 models.
2. Using internal feedback resistor.
3. Using the internal $R_{feedback}$ with nulled external amplifier in a constant 25°C ambient. (Offset doubles every 10°C).
4. Best straight line method of test.
5. The DAC9331-14 Series is designed to be used only in those applications where the current output is virtual ground; i.e., the summing junction of an op amp in the inverting mode. The internal feedback resistor (R Feedback) must be used to achieve temperature tracking. See APPLICATIONS INFORMATION for recommended circuit configurations.
6. The power supply voltage must not exceed +10V for the -1 versions or +15,5V for the -2 versions.

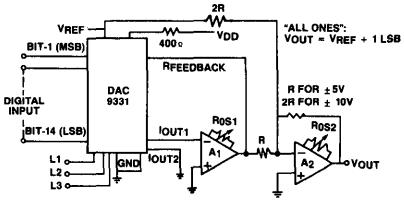
APPLICATIONS INFORMATION

UNIPOLAR OPERATION (2-Quadrant Multiplication)



NOTE: To maintain specified DAC9331 linearity, the external amplifier (A) must be zeroed. Apply an ALL "ZEROS" digital input and adjust R_{OS} for V_{OUT} = 0 ±1mV.

BIPOLAR OPERATION (4-Quadrant Multiplication)



NOTE: TO MAINTAIN SPECIFIED LINEARITY, EXTERNAL AMPLIFIERS (A_1 AND A_2) MUST BE ZEROED. WITH A DIGITAL INPUT OF 10...0 AND V_{REF} SET TO ZERO:
a) SET R_{OS1} FOR V_{01} = 0
b) SET R_{OS2} FOR V_{OUT} = 0
c) SET V_{REF} TO +10V AND ADJUST R_B FOR V_{OUT} TO BE 0 VOLTS.

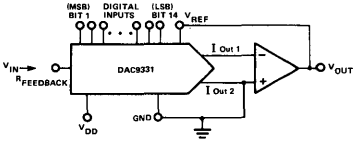
UNIPOLAR OPERATION
Transfer Characteristics

BINARY INPUT	ANALOG OUTPUT
111···111	$-V_{REF}(1-2^{-N})$
100···001	$-V_{REF}(1/2+2^{-N})$
100···000	$\frac{-V_{REF}}{2}$
011···111	$-V_{REF}(1/2-2^{-N})$
000···001	$-V_{REF}(2^{-N})$
000···000	0

BIPOLAR OPERATION
Transfer Characteristics

OFFSET BINARY INPUT	ANALOG OUTPUT
111···111	$-V_{REF}(1-2^{-(N-1)})$
100···001	$-V_{REF}(2^{-(N-1)})$
100···000	0
011···111	$V_{REF}(2^{-(N-1)})$
000···001	$V_{REF}(1-2^{-(N-1)})$
000···000	V_{REF}

ANALOG/DIGITAL DIVISION



Via the above configuration, the DAC331 can be used to divide an analog signal by a digital code (i.e., for digitally controlled gain). The transfer function is given as

$$V_{OUT} = \frac{-V_{IN}}{\frac{\text{Bit 1}}{2^1} + \frac{\text{Bit 2}}{2^2} + \frac{\text{Bit 3}}{2^3} + \cdots + \frac{\text{Bit 14}}{2^{14}}}$$

where the value of each bit is 0 or 1. Division by all "0"s is undefined and causes the op amp to saturate.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts.

ORDERING INFORMATION

MODEL NUMBER	DESCRIPTION
DAC9331-14-1	14-Bit MDAC, +5V Operation
DAC9331-14-2	14-Bit MDAC, +15V Operation

Specifications subject to change without notice.

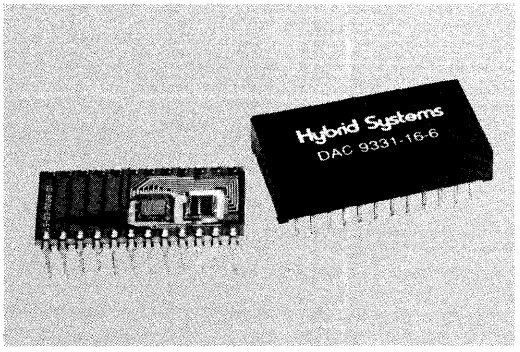
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC9331-16 Series

14, 15, and 16-Bit Linearity, Latched MDAC's

FEATURES

- **Up to 16-Bit Linearity**
- **Two Chip Construction**
- **Input Registers**
- **Low Power**
- **Ceramic 24-Pin DIP**
- **2 and 4-quadrant Multiplication**
- **Single-Supply Operation**
- **Low-Cost**



DESCRIPTION

The DAC9331-16 Series are true 16-Bit D/A converters manufactured with advanced proprietary monolithic devices and proven performance packaging technique. A single, unique monolithic chip contains switches, storage registers and other electronics for high resolution and low linearity error. A second, passive chip provides all the needed resistors for these multiplying D/A's. Input storage registers are in two 8-Bit segments with independent latching — a system that is compatible with microprocessor data bus interfaces. It's a truly "byte-sized" D/A input system. Combining 2- and 4-quadrant multiplying capability, TTL/DTL and CMOS compatibility; low power consumption (less than 60 mW) and operation from a single supply, the DAC9331-16 Series offers exceptional performance/cost ratio. Outstanding features include:

True 16-Bit Linearity — 16-Bit (0.0008%) linearity with 16-Bit resolution is now a reality. No other microcircuit converter does better. 14- and 15-Bit linearity versions available at lower cost.

Low Power — CMOS proprietary monolithic devices[1] in a unique circuit configuration[1] yield the lowest power of any 16-Bit converter available.

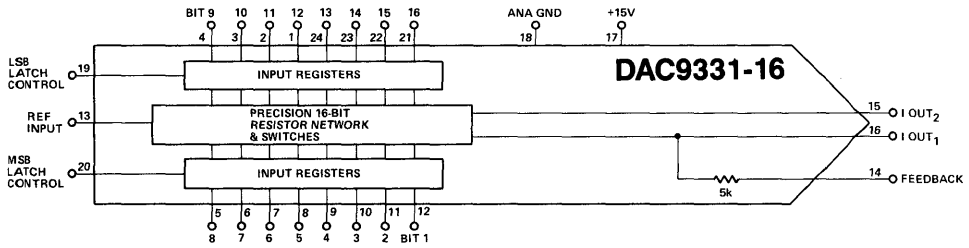
Two-Chip Construction — An advanced monolithic device, combined with our own resistor networks are all that's needed in this converter. Automatic wirebonding makes the most consistently superior assembly available.

Input Storage Registers — Designed as two 8-Bit segments, the input registers provide data storage when latched, or "transparent" registers when unlatched. Data conversion can now be performed continuously *or* from stored data — "byte-sized" input segments provide compatibility with most data bus lines.

Reliability — A proven performer, the DAC9331-16 is packaged in a 24-pin ceramic double DIP for the utmost in reliability. Combined with our proprietary monolithic switches and automatic wirebonding, we've made the DAC9331-16 Series the most reliable industrial converter to date. Reliability is further enhanced by batch-processed, precision laser-trimmed resistor networks fabricated in our own facility. Networks are functionally trimmed and glass passivated to assure reliability under adverse environmental conditions.

Advanced designs, proven processes and continuous monitoring during all production operations by our quality control organization are combined with rigorous AQL screening to provide the most dependable, low cost D/A converter possible.

FUNCTIONAL DIAGRAM

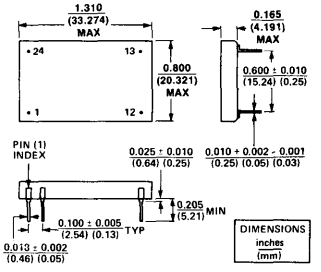


SPECIFICATIONS

(Typical @ +25°C and nominal power supply, V_{REF} = +10V, unipolar unless otherwise noted)

MODEL	DAC9331-16 -6 -5 -4		
TYPE	Multiplying, Latched Inputs		
DIGITAL INPUT			
Resolution	16-Bits		
2-Quad. Unipolar Coding	Binary		
4-Quad. Bipolar Coding	Offset Binary		
Logic Compatibility[1]	DTL, TTL, CMOS		
Input Leakage Current	±1μA (max): 0.4V>V_{LOGIC}>3.2V		
Strobe Width	250nS (min)		
Data Set-up Time[2]	500nS (min)		
REFERENCE INPUT			
Voltage Range	±25V (max)		
Input Impedance	5KΩ		
ANALOG OUTPUT			
Gain Accuracy[3]	0.1%		
Offset (unipolar)[4]	50μV (max)		
Small Signal 3dB Bandwidth	1 MHz		
Output Capacitance			
C_{out_1}	90pF		
C_{out_2}	70pF		
STATIC PERFORMANCE			
Integral Linearity (max)	±0.001%	±0.002%	±0.003%
Differential Linearity (max)	±0.0015%	±0.003%	±0.006%
Monotonicity Guaranteed	16 bits	15 bits	14 bits
DYNAMIC PERFORMANCE			
Major Code Transition Settling to 0.01% F.S.R. (strobed)	2μS		
Reference Feedthrough Error (Vref=20Vpp @ 10kHz)	2mVp-p		
STABILITY[3] (Over Specified Temp. Range)			
Scale Factor[5]	2ppm/°C F.S.R. (typ), 6ppm/°C (max) 6ppm/°C (max)		
Linearity	0.5ppm/°C F.S.R. (max)		
Differential Linearity	0.5ppm/°C F.S.R. (max)		
Linearity Over Time[5]	3ppm F.S.R./1000 hrs.		
POWER SUPPLY(V_{DD})			
Voltage Range @ Current	+15V (nom); +11.5V to +15.5V @ 1.5mA		
Rejection Ratio (14V-16V)	±0.002%/% (max)		
Power Dissipation (inputs at GND, V_{ref}=0)	60mW (max)		
TEMPERATURE RANGE			
Operating	0°C to +70°C		
Storage	-55°C to +85°C		
MECHANICAL			
Case Style	24-pin double-DIP		
Case Dimensions			

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12	24	BIT 13
2	BIT 11	23	BIT 14
3	BIT 10	22	BIT 15
4	BIT 9	21	BIT 16
5	BIT 8	20	MSB LATCH
6	BIT 7	19	LSB LATCH
7	BIT 6	18	ANA GND
8	BIT 5	17	+15V
9	BIT 4	16	I OUT 1
10	BIT 3	15	I OUT 2
11	BIT 2	14	$R_{FEEDBACK}$
12	BIT 1	13	REF IN

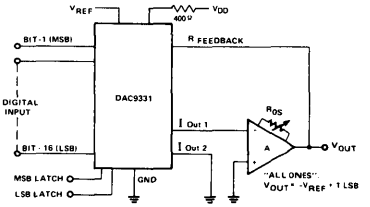


NOTES:

1. V_{IH}=2.4V (min); V_{IL}=0.8V (max) Inputs not to exceed -0.5V to +V_{DD}.
2. Time data must be stable before Strobe goes to "0".
3. Using internal feedback resistor.
4. Using the internal $R_{feedback}$ with nulled external amplifier in a constant 25°C ambient. (Offset doubles every 10°C).
5. The DAC9331-16 Series is designed to be used only in those applications where the current output is virtual ground; i.e., the summing junction of an op amp in the inverting mode. The internal feedback resistor (R Feedback) must be used to achieve temperature tracking. See APPLICATIONS INFORMATION for recommended circuit configurations.
6. For further information on long term drift refer to HS 9377 Application Notes.

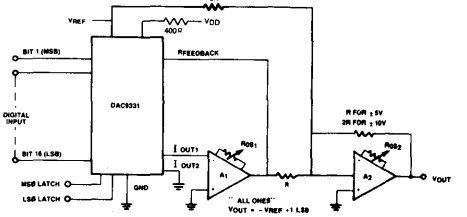
APPLICATIONS INFORMATION

UNIPOLAR OPERATION (2-Quadrant Multiplication)



NOTE: To maintain specified DAC9331 linearity, the external amplifier (A) must be zeroed. Apply an ALL "ZEROS" digital input and adjust R_{OS} for V_{OUT} = 0 ±1mV.

BIPOLAR OPERATION (4-Quadrant Multiplication)



NOTE: To maintain specified DAC9331 linearity, external amplifiers (A_1 and A_2) must be zeroed. With a digital input of 10...0 and V_{REF} set to zero:
a) Set R_{OS1} for V_{01} = 0
b) Set R_{OS2} for V_{OUT} = 0
c) Set V_{REF} to +10V and adjust R_B for V_{OUT} to be 0 Volts.

UNIPOLAR OPERATION
Transfer Characteristics

BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-N})$
100...001	$-V_{REF}(½+2^{-N})$
100...000	$-\frac{V_{REF}}{2}$
011...111	$-V_{REF}(½-2^{-N})$
000...001	$-V_{REF}(2^{-N})$
000...000	0

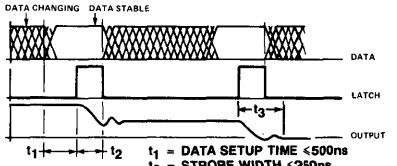
BIPOLAR OPERATION
Transfer Characteristics

OFFSET BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF}(1-2^{-(N-1)})$
100...001	$-V_{REF}(2^{-(N-1)})$
100...000	0
011...111	$V_{REF}(2^{-(N-1)})$
000...001	$V_{REF}(1-2^{-(N-1)})$
000...000	V_{REF}

STROBE LOGIC

Strobe	Function
0	data latched (held)
1	data changing (transfer)

TIMING DIAGRAM



t_1 = DATA SETUP TIME <500ns
t_2 = STROBE WIDTH <250ns
t_3 = SETTLING TIME 2μSEC TYP

PRECAUTIONARY NOTES:

In order to realize the ultimate resolution which this unit is capable of delivering, several precautions must be taken.

1. Amplifiers must be balanced so the summing junction is as close to zero volts as can be achieved. Usually less than 100μV.
2. Amplifiers must have a large enough open loop gain to be consistent with the required linearity. To obtain optimum performance this should be in excess of 10^5V/V or 100dB.
3. All grounds should be of low resistance.
4. Reference should be as high as possible to minimize errors due to offset at outputs.
5. To maintain accuracy over temperature amplifiers should have low bias current and offset voltage temperature coefficients.

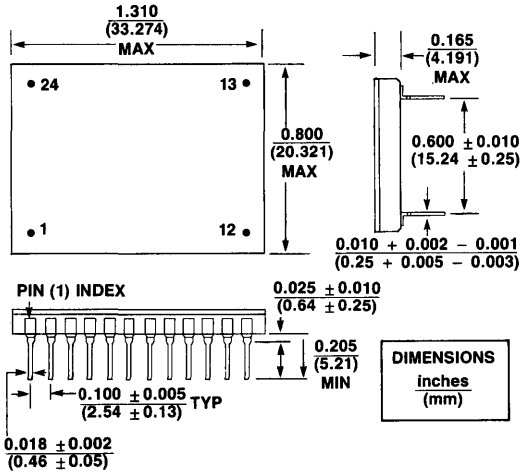
ORDERING INFORMATION

MODEL NUMBER	DESCRIPTION
DAC9331-16-4	14-BIT Linearity MDAC
DAC9331-16-5	15-BIT Linearity MDAC
DAC9331-16-6	16-BIT Linearity MDAC

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts.

Specifications subject to change without notice.

BULLETIN DAC9331-16 SERIES/4-88/Printed in U.S.A.


1.310
(33.274)
MAX
0.165
(4.191)
MAX
24
13
1
12
0.800
(20.321)
MAX
0.600 ±0.010
(15.24 ±0.25)
0.010 + 0.002 − 0.001
(0.25 + 0.005 − 0.003)
PIN (1) INDEX
0.025 ±0.010
(0.64 ±0.25)
0.205
(5.21)
MIN
0.100 ±0.005
(2.54 ±0.13) TYP
0.018 ±0.002
(0.46 ±0.05)
DIMENSIONS
inches
(mm)

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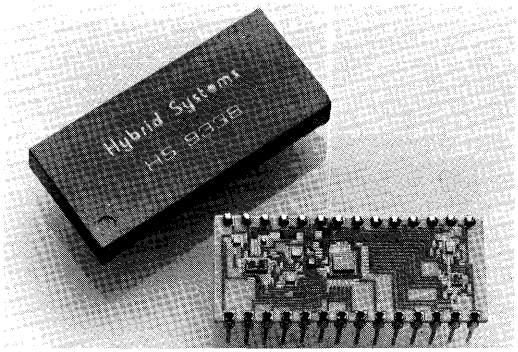
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9338

COMPLETE μP COMPATIBLE 12-BIT DAC

FEATURES

- Output ranges: 0 to +10V, ±10V,
- Coding: binary; offset binary
- Linearity: ±0.01%
- Settling time: 2.5μS
- μP compatible
- 28-pin package
- CMOS, TTL compatible
- Double buffered inputs

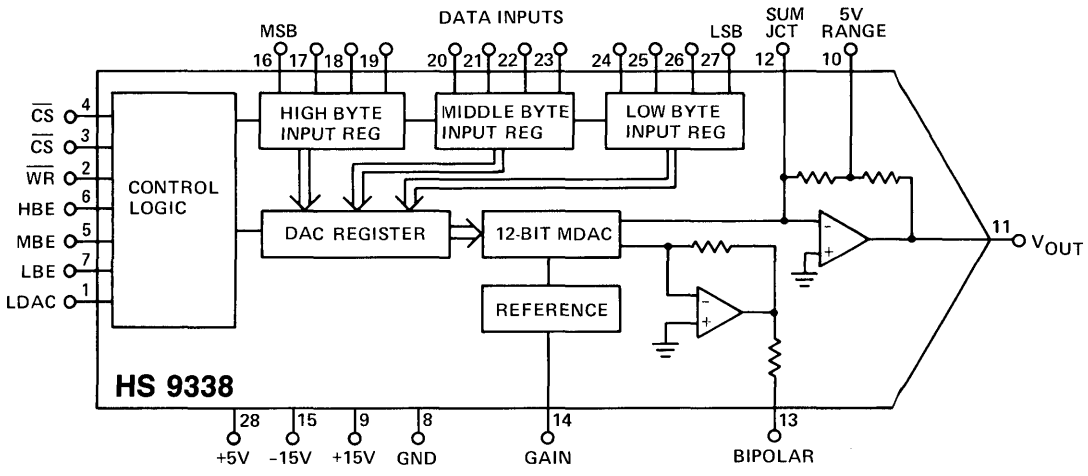


DESCRIPTION

HS9338 is a μP compatible, complete 12-bit double buffered digital-to-analog converter. To enhance application flexibility, the data input registers have been configured as 3 independent, 4-bit bytes. This enables the user to directly interface to 4, 8, and 12-bit data buses. HS9338 comes complete with interface control logic. The three separate byte enable inputs latch data from the bus into the appropriate primary data latches. The LDAC input transfers data from the primary latches to the DAC register. In addition to these input functions are two chip select inputs and a read/write input allowing direct memory-map configurations. All input controls are static to allow hardwired configurations.

7

FUNCTIONAL DIAGRAM



SPECIFICTIONS

(Typical @25°C unless otherwise noted. Power supply voltages: +15V, −15V, +5V, (±5%))

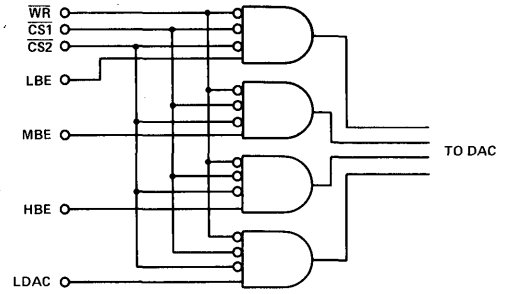
MODEL	HS 9338-2	HS 9338-0
DIGITAL INPUT		
Resolution	12 Bit	*
Unipolar Code	Binary	*
Bipolar Code	Offset Binary	*
Logic Compatibility[1]	CMOS, TTL	*
Control Logic Inputs		
I_{IH} @V_{IH} = 2.4V	20μA	*
I_{IL} @V_{IL} = 0.4V	−0.36mA	*
Data Input Current[5]	±1μA	*
ANALOG OUTPUT		
Scale Factor Accuracy[2]	±0.1% FSR	*
Initial Offset[2]		
Bipolar	±0.1% FSR max	*
Unipolar	±0.05% FSR max	*
Voltage Range[2]		
Bipolar	±10V,	*
Unipolar	0 to +10V	*
STATIC PERFORMANCE		
Integral Linearity[3]	±0.015% FSR max	±0.050% FSR max
Differential Linearity	±0.024 FSR max	±0.097% FSR max
Monotonicity	12 Bits	10 Bits
DYNAMIC PERFORMANCE		
Full Scale Transition		
Settling Time	5μS max	*
	2.5μS max	*
Full Scale Transition		
Slew Rate	10V/μS min	*
Delay to Analog Output		
From Bits Input[4]	220nS	*
From LDAC	220nS	*
From CS[4] or WE[4]	225nS	*
STABILITY		
Scale Factor	20ppm FSR	*
Integral Linearity	1ppm FSR max	*
Differential Linearity	1ppm FSR max	*
Offset Drift		
Bipolar	10ppm/°C	*
Unipolar	5ppm/°C	*
Monotonicity Temperature Range	0°C to +70°C	*
±15V POWER SUPPLY		
+15V Supply Current	12mA	*
−15V Supply Current	10mA	*
PSRR	0.005%/%	*
+5V POWER SUPPLY		
+5V Supply Current	24mA	*
TEMPERATURE RANGE		
Operating	−55°C to +125°C	*
Storage	−65°C to +155°C	*
MECHANICAL		
Case Style	Plastic	*

NOTES: 1. Control inputs are TTL and 5V CMOS only; data inputs are fully CMOS and TTL compatible. 2. See APPLICATION NOTES for adjustment procedures. 3. Specified as "Best Straight Line". 4. Operating the unit with the DAC Register transparent may result in output "glitches" due to logic skewing with the unit. 5. Digital Input Voltage must not exceed supply voltage or go below −0.5V. "0" 0.8V; 2.4V "1" V_{DD}.

*Same as HS 9338-2.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts.

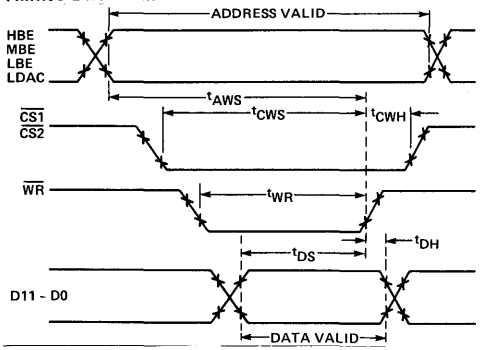
CONTROL LOGIC FUNCTIONAL DIAGRAM



TRUTH TABLE

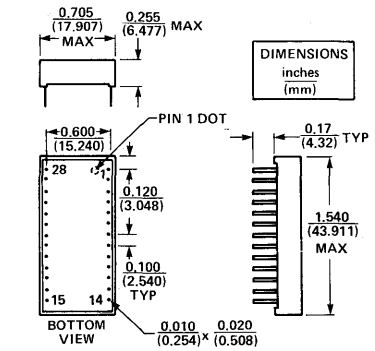
HS 9338 CONTROL INPUTS							HS 9338 OPERATION
WR	CS1	CS2	LBE	MBE	HBE	LDAC	
1 X X	X 1 X	X X 1	X	X	X	X	Device not selected Output reflects previously loaded data
0	0	0	1	0	0	0	Write data into low byte data register
0	0	0	0	1	0	0	Write data into middle byte data register
0	0	0	0	0	1	0	Write data into high byte data register
0	0	0	0	0	0	1	Load DAC register with data in low byte middle byte and high byte data registers
0	0	0	1	1	1	0	Write data simultaneous into all data registers
0	0	0	1	1	1	1	Write data directly into DAC register

TIMING DIAGRAM



t_{DS} : Data setup time, 250 nsec
t_{DH} : Data hold time, 20 nsec
t_{WR} : Write pulse width, 350 nsec
t_{CWS} : Chip select to write setup time, 375 nsec
t_{CWH} : Chip select to write hold time, 0 nsec
t_{AWS} : Address to write setup time, 250 nsec

PACKAGE OUTLINE



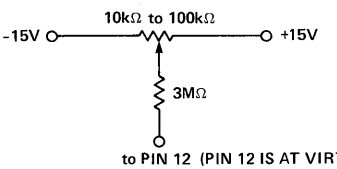
PIN DIAGRAM

PIN	FUNCTION
1	LDAC, LOADS DAC REGISTER AND CHANGES OUTPUT
2	$\overline{WR}$, WRITE INPUT, ACTIVATES ALL CONTROLS
3	$\overline{CS2}$, CHIP SELECT INPUT 2
4	$\overline{CS1}$, CHIP SELECT INPUT 1
5	MBE, MIDDLE BYTE ENABLE, D4 TO D7
6	HBE, HIGH BYTE ENABLE, D8 TO D11
7	LBE, LOW BYTE ENABLE, D0 TO D3
8	GND, GROUND, ANALOG AND DIGITAL GROUND CONNECTED INTERNALLY
9	V_{CC}, +15V SUPPLY
10	RANGE, 5V OUTPUT RANGE INPUT
11	V_{OUT}, DAC VOLTAGE OUTPUT
12	SUMJCT, SUMMING JUNCTION OF OUTPUT OPAMP
13	BIPOLAR, CONNECTED TO SUMJCT FOR BIPOLAR OUTPUT RANGE
14	GAIN, INPUT TO ADJUST FULL SCALE OUTPUT VOLTAGE
15	V_{EE}, -15V SUPPLY
16	D11, DATA INPUT, WEIGHT 2^{-1}, MSB
17	D10, DATA INPUT, WEIGHT 2^{-2}
18	D9, DATA INPUT, WEIGHT 2^{-3}
19	D8, DATA INPUT, WEIGHT 2^{-4}
20	D7, DATA INPUT, WEIGHT 2^{-5}
21	D6, DATA INPUT, WEIGHT 2^{-6}
22	D5, DATA INPUT, WEIGHT 2^{-7}
23	D4, DATA INPUT, WEIGHT 2^{-8}
24	D3, DATA INPUT, WEIGHT 2^{-9}
25	D2, DATA INPUT, WEIGHT 2^{-10}
26	D1, DATA INPUT, WEIGHT 2^{-11}
27	D0, DATA INPUT, WEIGHT 2^{-12}, LSB
28	V_{DD}, +5V SUPPLY, CONTROL LOGIC

OUTPUT CONNECTIONS

RANGE	OUTPUT	CONNECT PIN 12	CONNECT PIN 10	CONNECT PIN 13
0 to +10V	PIN 11	OPEN	OPEN	OPEN
−10V to +10V	PIN 11	PIN 13	OPEN	PIN 12
−5V to +5V	PIN 11	PIN 13	PIN 12	PIN 12

OUTPUT OFFSET ADJUST

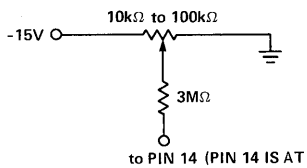


to PIN 12 (PIN 12 IS AT VIRTUAL GROUND)

RANGE: ±0.25% F.S.

Adjust for V_{out} = 0.000 Volt at input code 00 . . . 0 for unipolar operation or at input code 10 . . . 0 for bipolar operation.

OUTPUT GAIN ADJUST



to PIN 14 (PIN 14 IS AT -6.4 VOLTS)

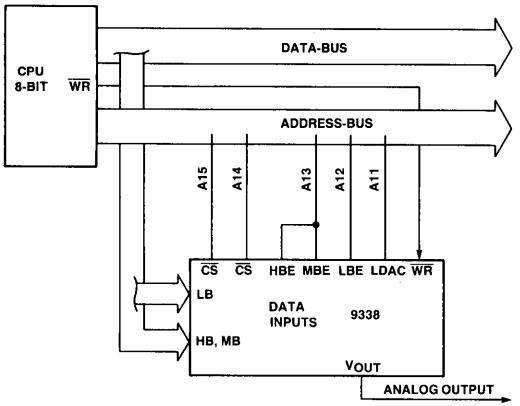
RANGE: ±0.5%

Adjust for V_{out} = +9.9976 Volt at input code 11 . . . 1 (4.9988 Volt on 0-5V range) or for V_{out} = -10.000 Volt at input code 00 . . . 0 (-5.0000 Volt on ±5V range) if set up for bipolar operation.

7

APPLICATIONS INFORMATION

INTERFACING THE HS9338 TO AN 8-BIT PROCESSOR USING NO EXTERNAL COMPONENTS

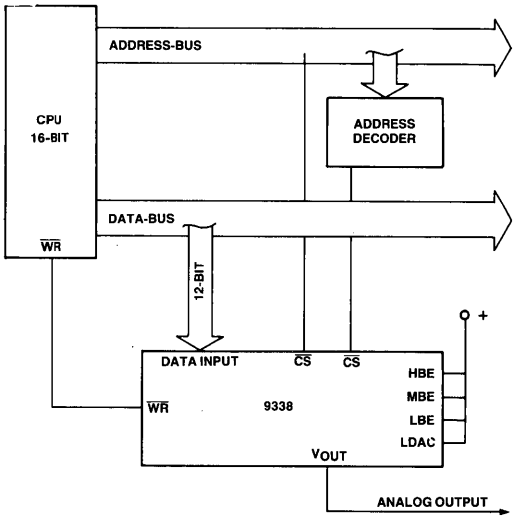


This mode of operation requires 13k bytes of unused addresses. No additional address decoder is necessary. The two chip-select input together with the byte-enable and load-DAC inputs are used to control all functions of the DAC. Through selecting the address-lines the user can vary the addresses used to control the DAC. In the above figure the control signals have the following address-configurations (hex):

HBE, MBE	2000
LBE	1000
LDAC	0800

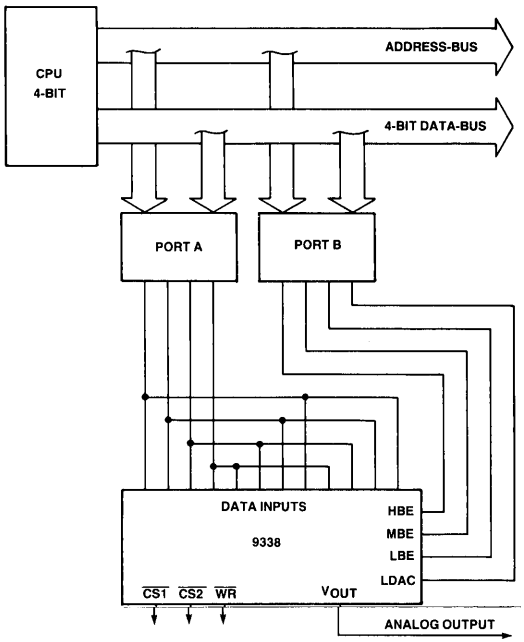
The LDAC input should not be tied together to the LBE input to ensure correct data transfer between the DAC registers.

INTERFACING THE HS9338 TO A 16-BIT MICROPROCESSOR



Interfacing the HS9338 to a 16-Bit microprocessor is quite easy, because no multiplexing of the data inputs is necessary. An address decoder and the second chip-select input is used to select the DAC.

INTERFACING THE HS9338 to a 4-BIT MICROPROCESSOR USING 4-BIT I/O-PORTS



This figure shows how to operate the HS 9338 with two 4-Bit ports. The chip-selects are tied to ground allowing continuous operation; they can be used for operating more DAC's at the same port. In the first step data should appear at the port A outputs; in the second step the control flags should appear on port B.

PRODUCT SCREENING AND QUALIFICATION

Products cataloged as Class B are fully screened in accordance with Method 5004 of MIL-STD-883, Class B.

Hybrid Systems is equipped to perform qualification and quality conformance testing of its products to the Class B requirements of MIL-STD-883, Method 5005. Processing to applicable Class S requirements is available where the higher confidence level is required.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 9338-2	μP DAC, 0.01% Linearity
HS 9338-0	μP DAC, 0.05% Linearity

Specifications subject to change without notice.

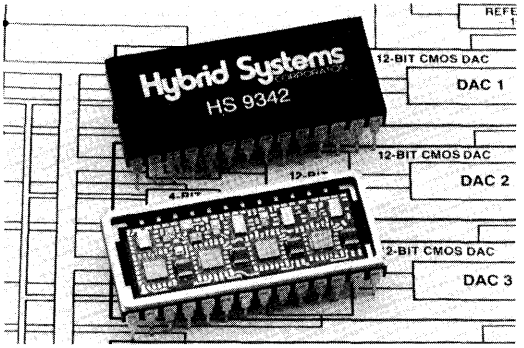
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9342

12-BIT, SPACE SAVING QUAD DAC

FEATURES

- Four 12-bit DAC's in a single package
- Low power: 750 mW typ, 1.12W max
- Double buffered input structure for μP interface
- 5μsec max voltage output settling to 0.012% for a 10V step
- Accepts internal or external voltage reference



DESCRIPTION

The HS9342 consists of four complete 12-bit digital-to-analog converters with a bipolar voltage output and reference circuit in a single 28-pin hybrid package. The design features latched monolithic 12-bit CMOS DACs, which provides low power and high reliability. The HS9342 is ideally suited for applications where board space is at a premium.

The HS9342 is packaged in a 28-pin DIP and is specified for operation from 0°C to 70°C for commercial grades and −55°C to +125°C for military grades. Full screening to MIL-STD-883C is available.

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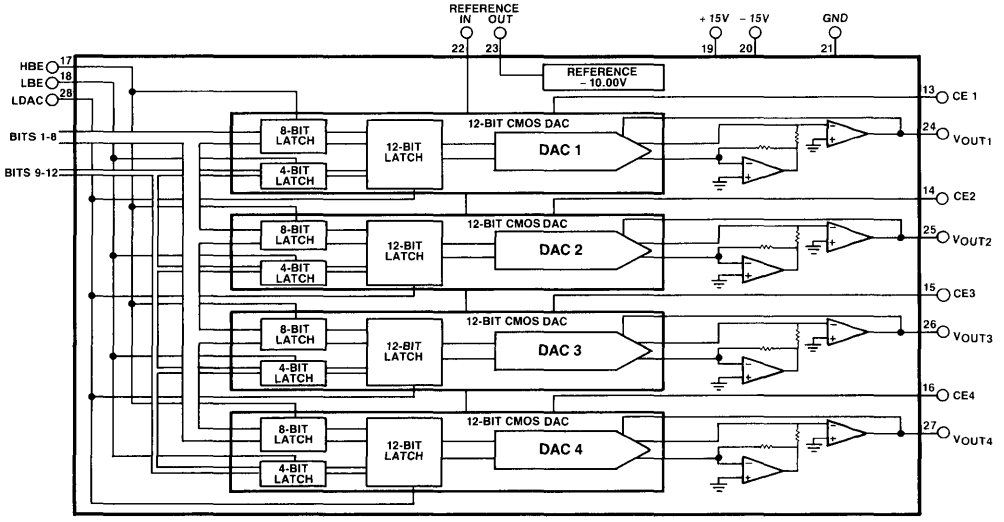
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C with V_{DD} = +15V, V_{EE} = −15V unless otherwise noted)

MODEL	HS 9342
DIGITAL INPUTS	
Resolution	12-Bits
V_{IH} Logic Level[1]	2.4V min
V_{IL} Logic Level[1]	0.8V max
I_{IN} Input Current (0V V_{IN} V_{DD})	1.0 μA typ, 4.0 μA max
Data Set-Up Time[2]	250 nsec min
Strobe Width[3]	250 nsec min
Data Hold Time	0 nsec min
Four-Quadrant Coding	Offset Binary
VOLTAGE REFERENCE INPUT	
Input Voltage Range	±10V
Input Impedance	1.2 KΩ min, 2.5 KΩ nom, 3.8 KΩ max
VOLTAGE REFERENCE OUTPUT (REF OUT connected to REF IN)	
Output Voltage Error	±10 mV max
Noise Voltage (peak-to-peak wide band)	100 μV typ, 200 μV max
Total Available Current (T_{min} to T_{max}) (I_{REF} + I_{EXT})	15 mA min, 20 mA max
Voltage Drift (T_{min} to T_{max})[4]	5 ppm/°C typ, 8 ppm/°C max
Current (Available for External Use)	12 mA max
STATIC DAC PERFORMANCE	
Integral Linearity[5]	±¼ LSB typ, ±½ LSB max
Differential Linearity	±¼ LSB typ, ±1 LSB max
Bipolar Zero Error	±1 LSB typ, ±2 LSB max
Gain Error	±2 LSB typ, ±4 LSB max
Gain Error Matching	±3 LSB typ
DYNAMIC PERFORMANCE	
Small Signal Settling (to 0.012%)	2.0 μsec
Full Scale Settling (to 0.012%)	5.0 μsec
Slew Rate	8V/μsec min, 12V/μsec typ
LDAC to Output Delay	300 nsec
DRIFT (T_{min} to T_{max})	
Gain	10 ppm/°C typ, 15 ppm/°C max
Bipolar Zero	3 ppm/°C typ, 5 ppm/°C max
Integral Linearity	0.5 ppm/°C typ, 1 ppm/°C max
Differential Linearity	0.5 ppm/°C typ, 1 ppm/°C max
POWER SUPPLY	
V_{DD}	+13.5V to +16.5V
V_{EE}	−13.5V to −16.5V
I_{DD} @ V_{DD} = +15V ±5%[6]	20 mA typ, 35 mA max
I_{EE} @ V_{EE} = −15V ±5%[6]	25 mA typ, 35 mA max
I_{DD} @ V_{DD} = +15V ±5%[7]	20 mA typ, 35 mA max
I_{EE} @ V_{EE} = −15V ±5%[7]	22 mA typ, 30 mA max
Power Supply Rejection	V_{DD} 0.002%/% typ V_{EE} 0.001%/% typ
POWER DISSIPATION	
	675 mW typ, 900 mW max[6] 530 mW typ, 825 mW max[7]
TEMPERATURE RANGE	
Operating	
C-Model	0°C to 70°C
B-Model	−55°C to +125°C
Storage	−65°C to +150°C
PACKAGE	
28-Pin Ceramic	
9342B	Case A
9342C	Case A
θ_{JA}	30°C/W

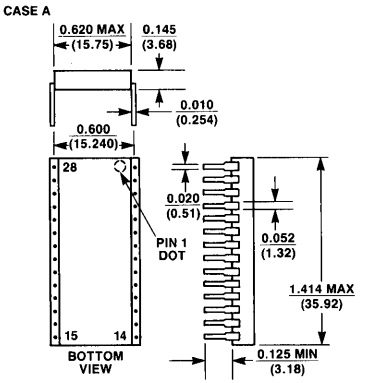
NOTES:
1. Digital inputs must never exceed V_{DD} or go below −0.3V.
2. Data must be stable before strobe (HBE, LBE, LDAC) goes to 0.
3. CE, LBE, HBE, LDAC. (All strobes are level triggered.)
4. The error band is defined graphically in terms of a box (voltage vertically, temperature horizontally) whose diagonals extend from 25°C to T_{max} and 25°C to T_{min}, with a slope equal to the stated temperature coefficient.
5. Integral linearity, for this product, is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value of any combination.
6. Utilizing internal voltage reference.
7. Applying external voltage reference to REF IN.

ABSOLUTE MAXIMUM RATINGS (Referenced to GND)

(Exceeding any *one* of these parameters may cause permanent damage to the unit)

V_{DD}	−0.3V to +18V
V_{EE}	+0.3V to −18V
V_{IN} (Bits 1-12, LBE, HBE, $\overline{CE}_{1-4}$)	−0.3V to (V_{DD} + 0.3V)
$V_{REF\ IN}$	±20V
DAC Outputs	Infinite short to GND
Reference Output	Infinite short to GND
Temperature Soldering Duration	10 sec @ 300°C
Power Dissipation	1800 mW

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	15	$\overline{CE}3$
2	BIT 2	16	$\overline{CE}4$
3	BIT 3	17	HBE
4	BIT 4	18	LBE
5	BIT 5	19	+15V
6	BIT 6	20	−15V
7	BIT 7	21	GND
8	BIT 8	22	REF IN
9	BIT 9	23	REF OUT
10	BIT 10	24	V_{OUT1}
11	BIT 11	25	V_{OUT2}
12	BIT 12 (LSB)	26	V_{OUT3}
13	$\overline{CE}1$	27	V_{OUT4}
14	$\overline{CE}2$	28	LDAC

APPLICATIONS INFORMATION

The HS 9342 has been designed for maximum flexibility in connecting to bus oriented systems. The HS 9342 is designed to accept 12-bit parallel data or 8-bit/4-bit data formatted by control pins CE1-CE4, HBE, LBE, and LDAC. The input registers are double buffered allowing any primary register to be updated independently of the others. Loading of any given primary register is accomplished by bringing the appropriate chip enable low, HBE and LBE high. All four DAC outputs are simultaneously updated by a single LDAC command.

CONTROL FUNCTIONS

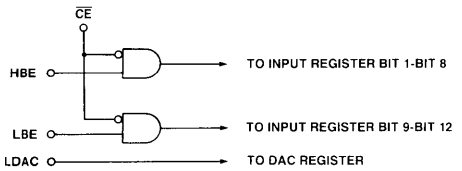
PIN	DEFINITION	FUNCTION
$\overline{CEX}$	Chip Enable X	Enables the primary register of DACX for loading data in conjunction with the HBE and/or LBE function.
HBE	High Byte Enable	Enables the 8 MSBs to be loaded into the primary register of the DACs selected by $\overline{CEX}$.
LBE	Low Byte Enable	Enables the 4 LSBs to be loaded into the primary register of the DACs selected by $\overline{CEX}$.
LDAC	Load DAC	Loads all data in all four DACs, from the primary to secondary registers and updates all DAC outputs.

HS 9342 TRUTH TABLE

$\overline{CE1}$	$\overline{CE2}$	$\overline{CE3}$	$\overline{CE4}$	HBE	LBE	LDAC	DESCRIPTION
0	1	1	1	1	1	0	Enables 1st rank of DAC1
1	0	1	1	1	1	0	Enables 1st rank of DAC2
1	1	0	1	1	1	0	Enables 1st rank of DAC3
1	1	1	0	1	1	0	Enables 1st rank of DAC4
X	X	X	X	X	X	1	Load DACs 1-4 secondary register from primary registers.

NOTE:
By enabling HBE, LBE and LDAC, all latches become transparent on selected DACs.

CONTROL LOGIC

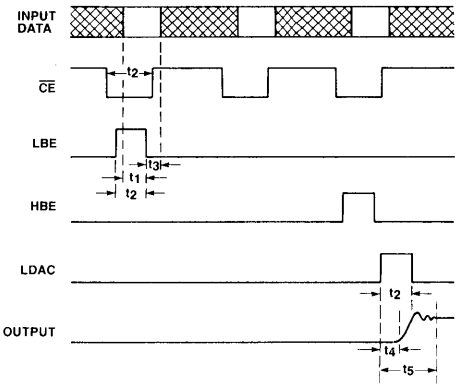


NOTE:
The transfer from input register to DAC register can be performed without Enabling Chip.

STROBE LOGIC

STROBE	FUNCTION
0	Data Latched (Held)
1	Data Changing (Transfer)

TIMING DIAGRAM



TIME AXIS NOT TO SCALE. ALL STROBES ARE LEVEL TRIGGERED.
t_1: Data Setup Time. Time data must be stable before strobe (byte enable/LDAC) goes to "0", t_1 (min) = 250 nsec.
t_2: Strobe Width. t_2 (min) = 250 nsec. (CE, LBE, HBE, LDAC).
t_3: Hold Time. Time data must be stable after strobe goes to "0", t_3 = 0 nsec.
t_4: Delay from LDAC to Output. t_4 = 300 nsec
t_5: Settling Time. 5μ sec (typical).

NOTE:
Minimum common active time for $\overline{CE}$ and any byte enable is 250 nsec.

TRANSFER CHARACTERISTICS

DIGITAL INPUT CODE			ANALOG OUTPUT VOLTAGE	
0000	0000	0000	− 10.000V	− FULL SCALE
0100	0000	0000	− 5.000V	− 1/2 SCALE
1000	0000	0000	0.000V	ZERO
1000	0000	0001	+ 4.88 mV	+ 1 LSB
1100	0000	0000	+ 5.000V	+ 1/2 SCALE
1111	1111	1111	+ 9.9951V	+ FULL SCALE-1 LSB

REFERENCE CIRCUITRY

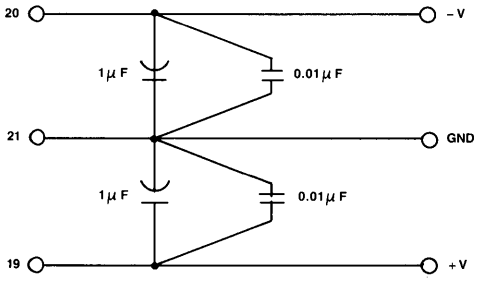
The HS 9342 is supplied with a precision internal − 10V reference, trimmed to within ± 5 millivolts. The reference is available for external use and can supply up to 8 mA of output current. In normal operation, the REF OUT (Pin 23) is connected to REF IN (Pin 22)[1]. The REF OUT is then fully loaded. If a system reference is available, an external reference may be used. It is recommended if an external reference is used, it supplies a minimum of 8 milliamps of current.

1. The reference is then fully loaded.

APPLICATIONS INFORMATION (continued)

POWER SUPPLY CONSIDERATION

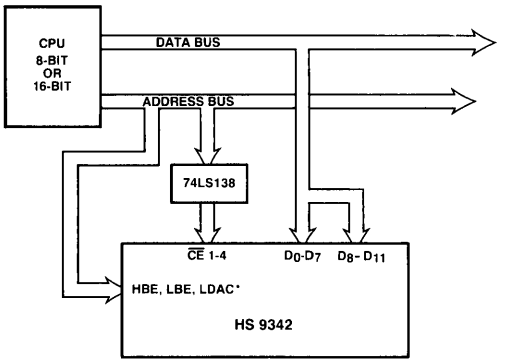
Power supplies used for the HS 9342 should be selected for low noise operation. In particular, they should be free of high frequency noise. Decoupling capacitors are recommended on all power supply pins located as close to the unit as possible. Suitable decoupling capacitors are 1 μ F tantulum type in parallel with 0.1 μ F disc ceramic type.



Recommended Power Supply Bypass

MICROPROCESSOR INTERFACE

The HS 9342 control logic is easily interfaced to most common microprocessors. Due to the 8-Bit/4-Bit input architecture, no external latches are required for interface to 8- or 16-bit bus structures.



For 8-Bit Data Bus, HBE and LBE addressed separately as high byte and low byte. For 16-Bit Data Bus, HBE and LBE are tied together and addressed as one word.

HS 9342 8- or 16-Bit Bus Interface

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below – 0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	DESCRIPTION
HS 9342C	0°C to 70°C	12-Bit, QUAD DAC
HS 9342B	– 55°C to + 125°C	12-Bit, QUAD DAC 883C

Specifications subject to change without notice.

SP9344

12-BIT QUAD DAC

FEATURES

- Four 12-bit DACs in a Single Package
- Low Power (600 mW)
- Double Buffered Inputs
- Voltage Output

PRELIMINARY INFORMATION

DESCRIPTION

The SP9344 is a QUAD 12-bit digital-to-analog converter with a bipolar voltage output in a single 28-pin dual-in-line package. The design is based on a proprietary latched 12-bit DAC chip keeping chip count to a minimum. The SP9344 features a double buffered input structure for each DAC allowing easy microprocessor interface. Each DAC is independently addressable allowing a versatile control architecture. All four DACs may be simultaneously updated using a single XFER command. Featuring 15 µsec settling time and ±1/2 LSB accuracy the SP9344 is ideally suited for applications where multiple DACs are required and board space is at a premium. Typical applications include ATE, process controllers, robotics, and instrumentation.

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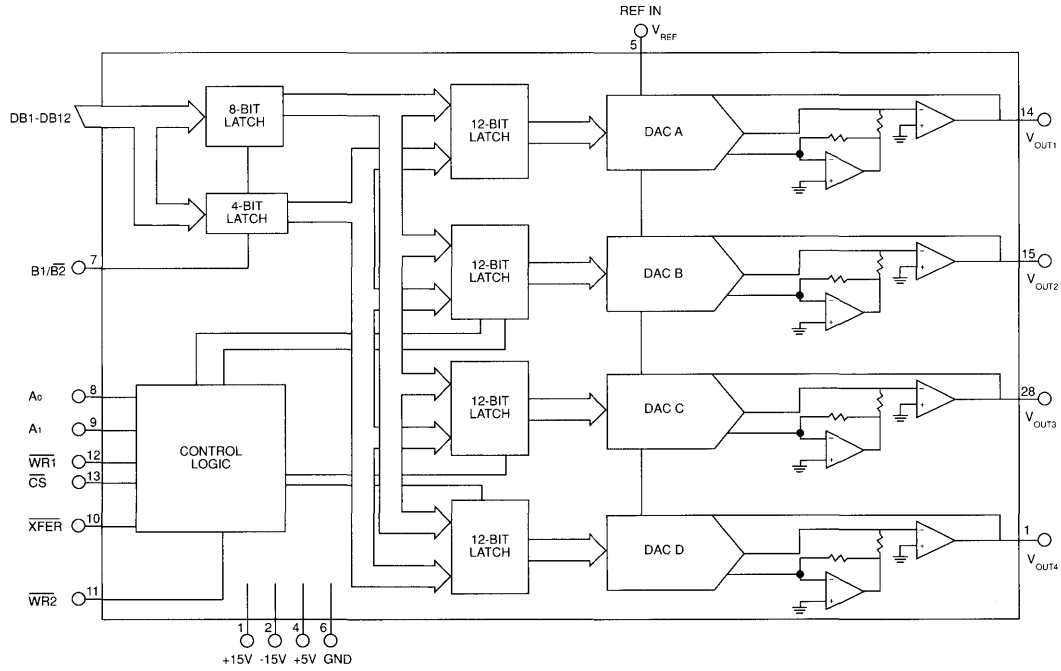
FUNCTIONAL DIAGRAM



(Typical @ 25°C and Nominal Power Supplies)

MODEL	SP9344C	SP9344B
DIGITAL INPUTS		
Resolution	12-Bits	*
VIH Logic	2.4V min	*
VIL Logic	0.8V max	*
4 Quad, Bipolar Coding	Complementary Binary	*
REFERENCE INPUT		
Voltage Range	±10V	*
Input Resistance	5 KΩ min, 10 KΩ typ, 15 KΩ max	*
SWITCHING CHARACTERISTICS		
Strobe Width	120 nsec min	*
Data Set-up Time	125 nsec min	*
Data Hold Time	0 nsec min	*
ANALOG OUTPUT		
Gain	±3 LSB max	±2 LSB max
Initial Offset Bipolar	±2 LSB max	±1 LSB max
Voltage Range Bipolar	±10V	*
Output Impedance	TBD	*
STATIC PERFORMANCE		
Integral Linearity	±0.5 LSB typ, ±1 LSB max	*
Differential Linearity	±0.5 LSB typ, ±1 LSB max	*
Monotonicity (t_{min} to t_{max})	12-bits	*
DYNAMIC PERFORMANCE		
Settling Time		
Small Signal to 0.012%	5 µsec	*
Full Scale to 0.012%	15 µsec	*
Slew Rate	TBD	*
STABILITY (t_{min} to t_{max})		
Gain	15 ppm/°C	*
Bipolar Zero	15 ppm/°C	*
Integral Linearity	±1ppm/ °C max	*
Differential Linearity	±1ppm/°C max	*
POWER REQUIREMENTS		
V_{DD}	+15V	*
V_{EE}	-15V	*
V_{Logic}	+5V	*
I_{DD}	15 mA typ, 18 mA max	*
I_{EE}	25 mA typ, 28 mA max	*
I_{Logic}	0.1 mA typ, 0.2 mA max	*
Power Dissipation	600 mW typ, 690 mW max	*
Power Supply Rejection	±0.004%/% max	*
TEMPERATURE RANGE		
Operating		
C Models	0°C to 70°C	
B Models		-55°C to +125°C
Storage	-60°C to +150°C	

PIN ASSIGNMENTS

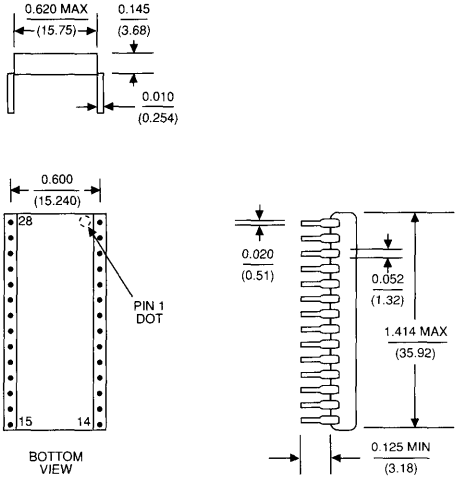
PIN	FUNCTION	DESCRIPTION
1	V_{OUT} 4	Voltage Output DAC 4
2	V_{EE}	-15V Supply
3	V_{DD}	+15V Supply
4	V_{logic}	+5V Supply
5	REF IN	Reference Input
6	GND	Ground
7	B1/$\overline{B2}$	Byte 1/Byte 2, Selects Data Input Format
8	A0	Address for DAC Selection
9	A1	Address for DAC Selection
10	$\overline{XFER}$	Transfer, Updates all DACs
11	$\overline{WR2}$	Write Input, Gates XFER Function
12	$\overline{WR1}$	Write Input, Gates DAC Selection
13	$\overline{CS}$	Enables DAC Input for Writing
14	V_{OUT} 1	Voltage Output DAC 1
15	V_{OUT} 2	Voltage Output DAC 2
16	DB 12	Data Bit 12
17	DB 11	Data Bit 11
18	DB 10	Data Bit 10
19	DB 9	Data Bit 9
20	DB 8	Data Bit 8
21	DB 7	Data Bit 7
22	DB 6	Data Bit 6
23	DB 5	Data Bit 5
24	DB 4	Data Bit 4
25	DB 3	Data Bit 3
26	DB 2	Data Bit 2
27	DB 1	Data Bit 1
28	V_{OUT} 3	Voltage Output DAC 3

CODING: COMPLEMENTARY BINARY

INPUT			OUTPUT
MSB		LSB	
0000	0000	0000	V_{REF}
0000	0000	0001	V_{REF} - 1 LSB
0111	1111	1111	0 - 1 LSB
1000	0000	0000	0
1000	0000	0001	0 + 1 LSB
1111	1111	1111	$-V_{REF}$ + 1 LSB

$$1\ LSB = \frac{V_{REF}}{2^{12}}$$

PACKAGE OUTLINE



ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	SCREENING
SP9344C	0°C to 70°C	—
SP9344B	-55°C to +125°C	MIL-STD-883C

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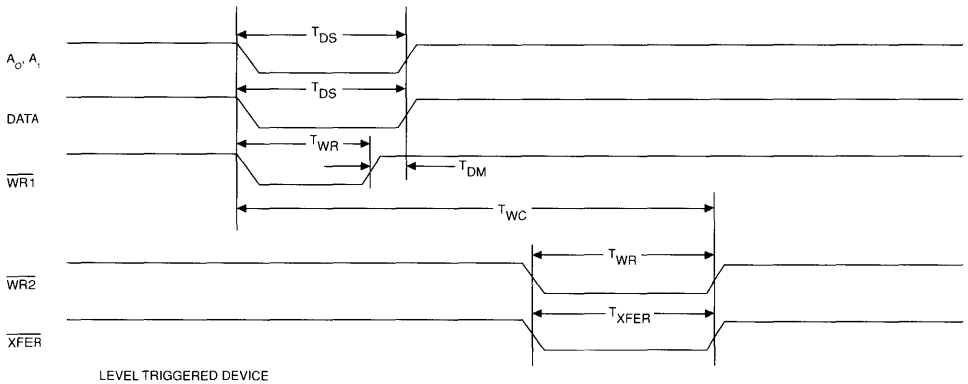
CONTROL FUNCTIONS

PIN	FUNCTION
A_0	Address 0 for DAC Selection
A_1	Address 1 for DAC Selection
$\overline{WR1}$	Enables A_0, A_1 (Along With $\overline{CS}$), Active Low, Gated With $\overline{CS}$
B1/$\overline{B2}$	Selects high and low bytes. In 12-bit mode, B1/$\overline{B2}$ tied high. In 8-bit mode, a 12-bit word is loaded into first register when B1/$\overline{B2}$ is high, and a 4-bit word is updated to the lower bits when B1/$\overline{B2}$ is low.
$\overline{WR2}$	Gated with $\overline{XFER}$, used to load all DACs simultaneously (Active Low)
$\overline{XFER}$	Gated with $\overline{WR2}$, used to load all DACs simultaneously (Active Low)

TIMING CHARACTERISTICS

PARAMETER	LIMIT AT T_A = +25°C	LIMIT AT -55°C TO +125°C	UNITS	
T_{DS}	100 min	125 min	ns	Data Set Up Time (To rising edge of $\overline{WR1}$ command)
T_{DH}	0 min	0 min	ns	Data Hold Time
T_{WR}	100 min	120 min	ns	Write Pulse Width
T_{XFER}	100 min	120 min	ns	Transfer Pulse Width
T_{WC}	200 min	245 min	ns	Total Write Command



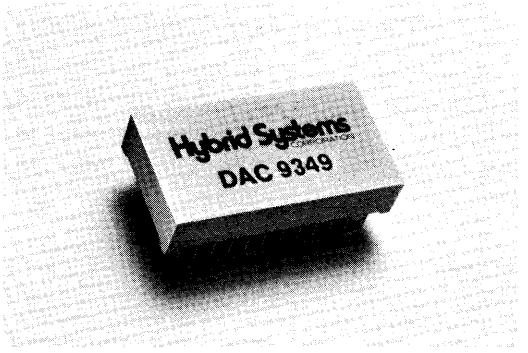
WRITE CYCLE TIMING DIAGRAM

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC9349
Complete 12-Bit CMOS DAC

FEATURES

- **12-Bit Binary or 3-Decade BCD Coding**
- **±2.5V, ±5V, ±10V, 0 to -5V, 0 to -10V Output Ranges**
- **Complete**
- **Low Power**
- **Low Cost**
- **Reliable**



DESCRIPTION

The DAC9349 is a versatile, economically-priced complete 12-Bit D/A converter intended for use in fixed reference applications. The unit combines CMOS switches, precision laser-trimmed ladder, internal precision reference and gain-selectable output amplifier in a unique, low-cost 24-pin double DIP[1]. An external fixed reference of −10V ±10% may be used for ratiometric applications. Features of the DAC9349 include:

Choice of Coding — Units can be supplied in either 12-Bit binary (−12 models) or 3 decade BCD coding (−3D models).

Pin Selectable Output Ranges — External pin jumpers provide unipolar output ranges of 0 to −5V or 0 to −10V (binary models), or ±2.5V, ±5V and ±10V for (offset binary coded) bipolar outputs.

Completeness — No additional external components are required for a 12-Bit D/A conversion.

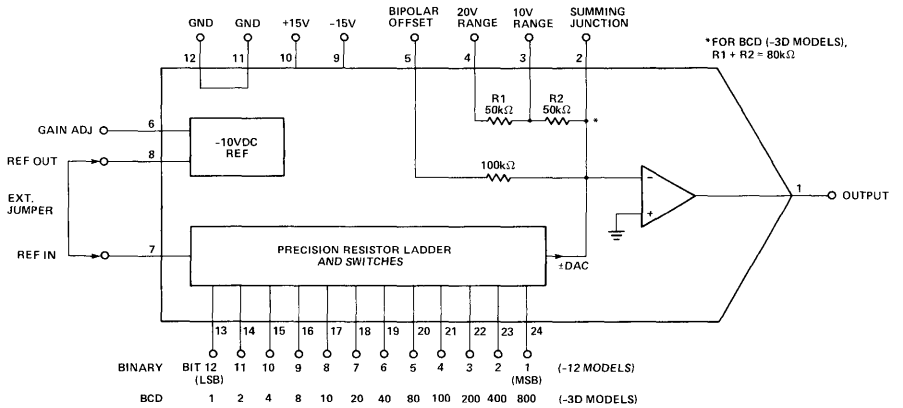
Good Dynamic Performance — Reduced settling time and higher slew rate compared to many 12-Bit converters.

Reliability — Like other converters in the commercial product line, the DAC9349 is offered in a unique package which has undergone the same extensive environmental testing to assure its reliability.

Reliability is enhanced by batch-processed, precision laser-trimmed resistor networks fabricated in our own facility. Similar to monolithic circuits, the networks are processed and functionally trimmed to assure consistent performance. Networks are glass passivated to assure reliability under adverse environmental conditions.

1. U.S. Patent Pending

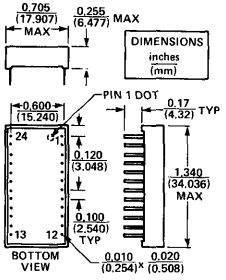
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ 25°C Using Internal Reference and V_{DD} =±15V unless noted)

MODEL	DAC9349
TYPE	Fixed Reference, Voltage Out
DIGITAL INPUT	
Resolution	12 Bits
Coding	
Unipolar	Binary; 3 DEC. BCD
Bipolar	Offset Binary
Logic Levels (Threshold)	V_{IL}=1.0V max V_{IH}=3.5V min
ANALOG OUTPUT	
Scale Factor[1]	0.1% F.S.R. max
Initial Offset[1]	
Unipolar	±0.2% F.S.R. max
Bipolar	±0.1% F.S.R. max
Voltage Range[2]	
Unipolar	0 to -5V, 0 to -10V
Bipolar	±2.5V, ±5V, ±10V
Current Compliance	±10mA typ ±5mA min
Output Impedance	0.1 Ω max
REFERENCE	
Internal[3]	-10VDC
External (D.C. Only)	-10VDC ±10% @ 1mA
STATIC PERFORMANCE	
Linearity	±1/2 LSB max
Differential Linearity	1 LSB max
DYNAMIC PERFORMANCE	
Settling Time (worst case)	15µs max
Slew Rate	1V/µs
STABILITY	
(Over Specified Temperature Range)	
Linearity	5ppm/°C max
Differential Linearity	2ppm/°C max
Transfer Characteristics[4]	30ppm/°C max
POWER SUPPLY	
Requirements	+15V @ 5mA typ 10mA max -15V @ 15mA typ 20mA max
Rejection Ratio	0.005%/% max
TEMPERATURE	
Operating	0°C to +70°
Storage	0°C to +85°C
MECHANICAL	
Case Style	24-pin Double-DIP
Case Dimensions	



PIN NO.	FUNCTION	PIN NO.	FUNCTION BINARY	FUNCTION BCD
1	OUTPUT	24	BIT 1 (MSB)	800
2	SUMMING JCT	23	BIT 2	400
3	10V RANGE	22	BIT 3	200
4	20V RANGE	21	BIT 4	100
5	BIPOLAR OFFSET	20	BIT 5	80
6	GAIN ADJ	19	BIT 6	40
7	REF IN	18	BIT 7	20
8	REF OUT	17	BIT 8	10
9	-15V	16	BIT 9	8
10	+15V	15	BIT 10	4
11	GND	14	BIT 11	2
12	GND	13	BIT 12(LSB)	1

NOTES:

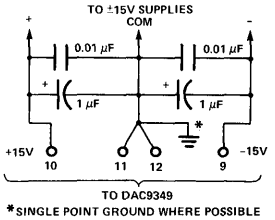
[1] Or 10mV max, whichever is greater. Externally adjustable (see Figure 3).

[2] The -3D models have a 3-decade BCD format with a unipolar FS output range of 0 to -9.99V.

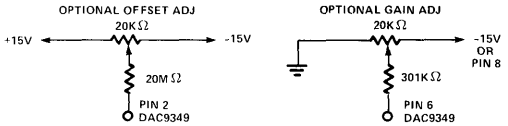
[3] For specified overall performance, external loading of the reference output (Pin 8) must not exceed 1.0mA.

[4] Total effect of linearity, offset and gain temperature coefficients on the transfer characteristic of the unit.

APPLICATIONS INFORMATION



OPTIONAL GAIN AND OFFSET ADJUSTMENT CIRCUIT



CALIBRATION PROCEDURE
(for optional external Gain & Offset adjustment)

Unipolar operation:
1. Apply a 0 0 0 . . . 0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 1 1 1 . . . 1 input code and set the GAIN ADJ pot for -(F.S. -1LSB).

Bipolar operation:
1. Apply a 0 0 0 . . . 0 input code and set the OFFSET ADJ pot for a +F.S. output.
2. Apply a 1 1 1 . . . 1 input code and set the GAIN ADJ pot for -(F.S. -1LBS).

BCD Unipolar operation:
1. Apply a 0 0 0 . . . 0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply 1001 1001 1001 input and set the GAIN ADJ pot for -9.990V.

TRANSFER CHARACTERISTICS

Unipolar Operation

Digital Input	Analog Output
1 1 1 . . . 1	-(F.S. -1 LSB)
1 0 0 . . . 0	-F.S./2
0 0 0 . . . 0	0V

Bipolar Operation

Digital Input	Analog Output
1 1 1 . . . 1	-(F.S. -1 LSB)
1 0 0 . . . 0	0V
0 0 0 . . . 0	+F.S.

BCD Unipolar Operation

Digital Input	Analog Output
1001 1001 1001	-9.99
0101 0000 0000	-5.00
0000 0000 0000	0V

OUTPUT RANGE SCALING**

Output Voltage Range	Jumper These Pins	Connect Pin 5 to Pin	Coding
0 to -5V	1&3, 2&4	11	Binary
0 to -10V	1 & 3	11	
0 to -9.99V	1 & 4	*	BCD
±2.5V	1 & 3 2 & 4	7	Offset Binary
±5V	1 & 3	7	
±10V	1 & 4	7	

*No Connection on BCD (-3D) Models.

****Pin 7 must be connected to either the internal reference (Pin 8) or to an external -10VDC reference source.**

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts.

ORDERING INFORMATION

MODEL	DESCRIPTION
DAC9349-12	Complete, 12-Bit Binary DAC
DAC9349-3D	Complete, 3-Decade BCD DAC

Specifications subject to change without notice.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC9356

COMPLETE LOW-POWER 12-BIT DAC

FEATURES

- Low cost
- Complete
- Low power
- DAC80 compatibility
- Reliable

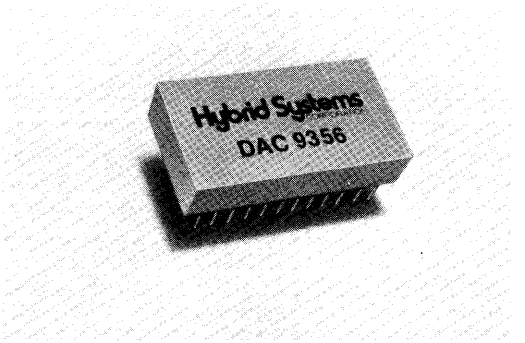
DESCRIPTION

The DAC9356 is a unique, low-cost, 12-bit DAC packaged in a 24 pin double DIP. As supplied, the unit provides an output of ±10 volts at 5mA; 25μS settling time for a full scale change; and ±30ppm/°C gain drift. The addition of an external resistor permits ±5 volt output with no loss in current capability — other ranges can be provided in OEM quantities. Matched CMOS current switches provide the lowest static power consumption of available technologies, while the ±20% supply tolerance is a significant advantage over similar devices which may demand ±3% or better. Outstanding features of the DAC9356 are:

Completeness — No external components are required for a 12-bit D-A conversion function. The DAC9356 includes the switches, temperature compensated reference, precision ladder network and output amplifier in the same package. Nothing else is needed.

Low Power Consumption — 175mW at ±15 volts. Accumulated power, power supply size and expense, and system heat removal are significantly reduced — and no +5 volt logic supply is required.

Pin-Out Similarity with DAC80 — For ±10 volt output, the DAC9356 replaces the DAC80. DAC9356 is similar to other more expensive, higher power units as well.

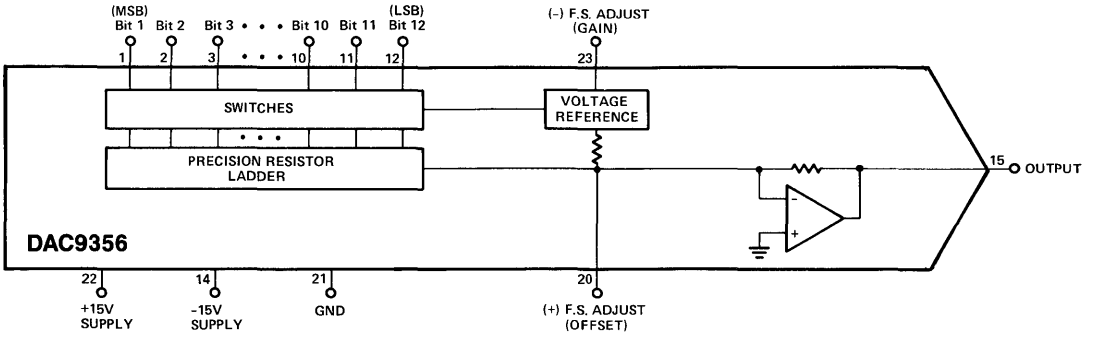


Reliability Plus — Packaged in a unique enclosure which has undergone extensive environmental testing during its development, the DAC9356 is continuously monitored during all assembly and test operations by our quality control organization.

Reliability is enhanced by batch-processed, precision laser-trimmed resistor networks fabricated in our own facility. Similar to monolithic circuits, the networks are processed and functionally trimmed to assure consistent performance. Networks are glass passivated to assure reliability under adverse environmental conditions.

Because of its low cost, low power, completeness and reliability, the DAC9356 is your best choice for systems which employ several DACs. With the advantages of large supply tolerance and lack of external components or adjustments, the DAC9356 is the most cost-effective converter product available.

FUNCTIONAL DIAGRAM



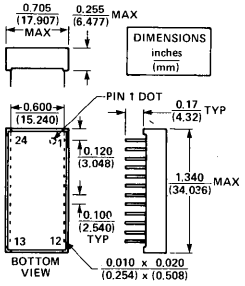
SPECIFICATIONS

(Typical @ +25°C and nominal power supplies unless otherwise noted)

MODEL	DAC9356
DIGITAL INPUT	
Resolution	12-Bits
Coding	Complementary Offset Binary
Logic Compatibility[1]	CMOS 2.0V threshold (nominal) V_{IH}>3.0V (min), V_{IL}<0.8V (max)
Input Current	±1μA (max): 0.4V>V_{LOGIC}>3.0V
ANALOG OUTPUT[2]	
Voltage @ Current[3]	±10 Volts @ ±5mA
Impedance	<0.1Ω
Initial Accuracy[4]	±0.1% F.S.R.
Protection	Continuous Short Circuit to Ground
REFERENCE	Internal; Temp. Compensated
STATIC PERFORMANCE	
Integral Linearity (best straight line)	±0.02% (max)
Differential Linearity	±½ LSB (typ), ±1 LSB (max)
DYNAMIC PERFORMANCE	
Settling Time, 10V Change to ±0.02% F.S.R.	25μSec
Slew Rate	0.6V/μsec
STABILITY	
Gain	±30ppm/°C F.S.R.
Offset	±10ppm/°C F.S.R.
Differential Linearity	±5ppm/°C F.S.R.
POWER REQUIREMENTS*	
Positive Supply Voltage	+11.5 to +18 volts (max)
+15V Supply Current	2.5mA (typ), 3.5mA (max)
Negative Supply Voltage	-11.5 to -18 volts (max)
-15V Supply Current	11mA (typ), 15.0mA (max)
Rejection Ratio	0.05%/% (typ), 0.08%/% (max)

*Supply voltage must exceed maximum converter output voltage by not less than 3 volts.

ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	0°C to +85°C
MECHANICAL	
Case Style	24 pin double-DIP
Case Dimensions	



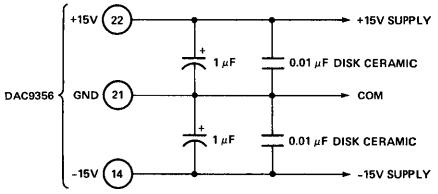
PIN	FUNCTION	PIN	FUNCTION
1	BIT-1 (MSB)	24	N.C.
2	BIT-2	23	(-) F.S. ADJ
3	BIT-3	22	+15VDC
4	BIT-4	21	GND
5	BIT-5	20	(+) F.S. ADJ
6	BIT-6	19	N.C.
7	BIT-7	18	N.C.
8	BIT-8	17	N.C.
9	BIT-9	16	N.C.
10	BIT-10	15	OUTPUT
11	BIT-11	14	-15VDC
12	BIT-12 (LSB)	13	N.C.

NOTES:

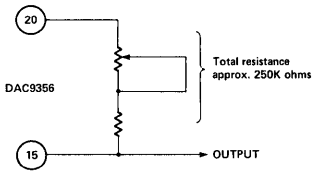
1. Logic input should not exceed +15 volts or be below -0.3V.
2. Full Scale range and offset voltage externally adjustable. See APPLICATIONS INFORMATION.
3. Can be supplied in unipolar ranges for OEM quantities. Consult factory.
4. Can be adjusted to ±0.02% F.S.R. or better. See OPTIONAL ADJUSTMENT CIRCUITS.

APPLICATIONS INFORMATION

OPTIONAL BYPASS CIRCUIT

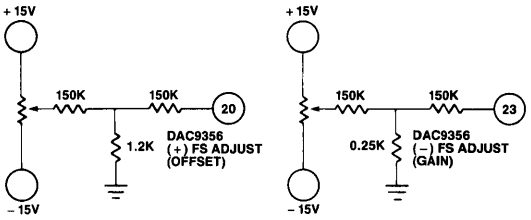


OPTIONAL* ±5 VOLT (OUTPUT) CONNECTION



*TC of external resistors must be between 0 and +50ppm/°C to maintain drift performance.

OPTIONAL ADJUSTMENT CIRCUITS



CALIBRATION PROCEDURES

1. Apply 000 ... 000 input code and set +F.S. ADJUST potentiometer for +F.S. -1 LSB output.
2. Apply 111 ... 111 input code and set -F.S. ADJUST potentiometer for -F.S. output.

TRANSFER CHARACTERISTICS

Complementary Offset Binary Input Code												Analog Output	
MSB	2	3	4	5	6	7	8	9	10	11	LSB	Weighting	Voltage
1	1	1	1	1	1	1	1	1	1	1	1	-F.S.	-10.000V
1	0	0	0	0	0	0	0	0	0	0	0	-1 LSB	-0.0048V
0	1	1	1	1	1	1	1	1	1	1	1	Zero	+0.000V
0	0	0	0	0	0	0	0	0	0	0	0	+F.S. -1 LSB	+9.9951V

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts.

ORDERING INFORMATION

MODEL	DESCRIPTION
DAC9356	Complete 12-Bit D/A Converter

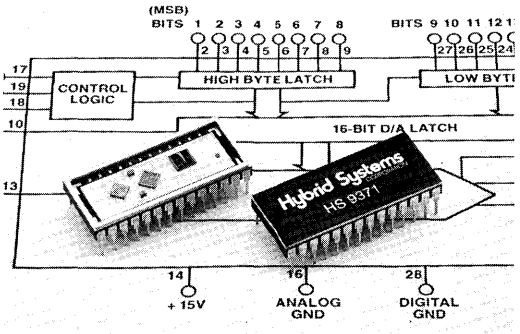
Specifications subject to change without notice.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

μP COMPATIBLE, CURRENT OUTPUT, 16-BIT MDAC

FEATURES

- Monotonic to 16-bits over the military and commercial temperature ranges
- Low power consumption, 45 mW max.
- Double buffered input
- Proprietary semicustom gate array signficantly reduces digital feedthrough
- Pinout permits 16 digital input lines to be connected to an 8-bit data bus without crossing bus lines



DESCRIPTION

The HS9371 is a current output, 16-bit multiplying D/A converter with 16-bit monotonicity guaranteed over the commercial and military temperature ranges. Complete with dual storage registers, the HS9371 Series easily interfaces with either 8-bit or 16-bit bus structures, eliminating the need for external latches.

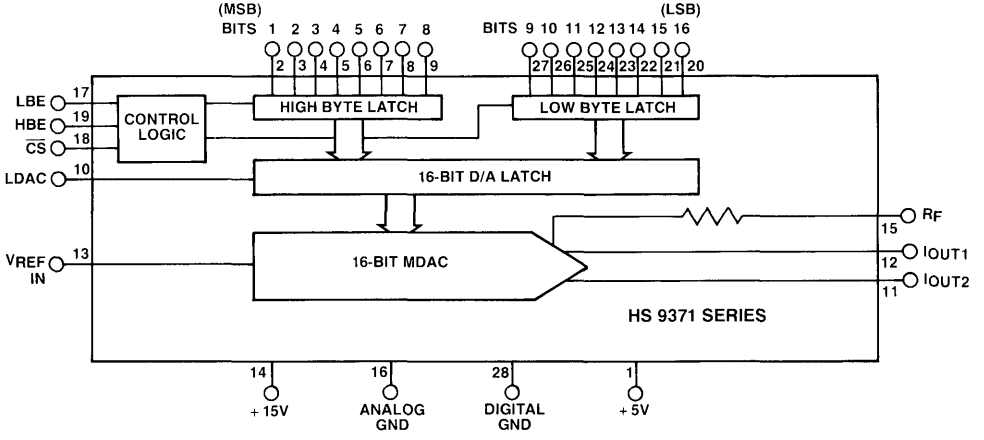
A proprietary semicustom gate array is used to significantly reduce digital feedthrough while internal decoupling capacitors reduce the effect of power supply perturbations.

The HS9371 has dual 8-bit input registers for direct interface to 8- or 16-bit bus structures. The pinout of the HS9371 allows the user with an 8-bit bus to run only 8 traces directly underneath the hybrid to connect to the 16-bit input register.

The HS9371 is available for either commercial (+0°C to +70°C) or military (−55°C to +125°C) applications. Screening to MIL-STD-883C is available.

7

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C unless otherwise specified)

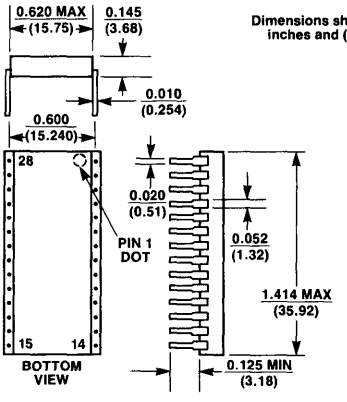
MODEL	HS 9371K	HS 9371J	HS 9371TB	HS 9371SB
DIGITAL INPUT				
Resolution	16-bits	*	*	*
Coding	Straight/Offset Binary	*	*	*
Logic Compatibility	TTL, LSTTL, CMOS			
V_{IL} (max)[5]	0.8V	*	*	*
V_{IH} (min)[5]	2.4V	*	*	*
Input Current	10 μ A max	*	*	*
Latch Control Minimum Pulse Width	100 nsec	*	*	*
Data Set-Up Time	100 nsec min[1]	*	*	*
Data Hold Time	0 nsec	*	*	*
ANALOG OUTPUT				
Gain Accuracy	±0.1% F.S.R. typ, ±0.2% max[2]	*	*	*
Initial Offset Error	±0.0005% max[2]	*	*	*
Current Range				
Unipolar	0 to +2 mA	*	*	*
Bipolar	±1 mA	*	*	*
Noise				
p-p noise (0.1 Hz to 100 Hz)	50 μ V	*	*	*
Output Capacitance	80 pF	*	*	*
REFERENCE INPUT				
Input Impedance	5K Ω	*	*	*
STATIC PERFORMANCE				
Integral Linearity Error[3]	±0.0015% max	±0.003% max	±0.0015% max	±0.003% max
Differential Linearity Error[4]	±0.0015% max	±0.003% max	±0.0015% max	±0.003% max
Monotonicity Guaranteed to:	16-bits	15-bits	16-bits	15-bits
DYNAMIC PERFORMANCE				
Major Carry Transition Settling to 0.0015% F.S.R.	1 μ sec[6]	*	*	*
Full Scale Transition Settling to 0.0015% F.S.R.	5 μ sec[6]	*	*	*
Reference Feedthrough Attenuation[8]	100 dB @ 100 Hz sine wave	*	*	*
	80 dB @ 1 kHz sine wave	*	*	*
Glitch Energy[8]	3 nV-sec	*	*	*
STABILITY				
Gain Drift	6 ppm/°C max	*	*	*
Offset Drift				
Unipolar	1 ppm/°C max	*	*	*
Bipolar	2 ppm/°C max	*	*	*
Linearity Drift	1 ppm/°C max	*	*	*
POWER SUPPLY				
Current	V_{LOGIC}, all bit inputs			
	0 or +5V		+2.5V	
+15V supply	1 mA typ, 3 mA max		1 mA typ, 3 mA max	
+5V supply	0.1 μ A typ, 1 μ A max		12 mA typ, 20 mA max	
Power Dissipation[7]	45 mW max, V_{LOGIC} = 0 or +5V, all bit inputs 150 mW max, V_{LOGIC} = +2.5V, all bit inputs			
Rejection Ratio	±0.0006% FS/% typ	*	*	*
	±0.002% FS/% max	*	*	*
TEMPERATURE RANGE				
Operating	0°C to +70°C	0°C to +70°C	−55°C to +125°C	−55°C to +125°C
Storage	−25°C to +85°C	−25°C to +85°C	−65°C to +150°C	−65°C to +150°C
PACKAGE				
28-pin, double DIP				

NOTES:

1. −55°C to +125°C.
2. Adjustable to zero.
3. Integral Linearity is measured per best straight line method.
4. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
5. Voltages at the digital inputs may not go below 0 volts or exceed +5V.
6. 50 Ω load.
7. To minimize power consumption, add 2KΩ pull-up resistors to the digital inputs when driving with TTL.
8. Lid of Case should be grounded to analog ground for optimum performance.

*Specifications same as 9371K.

PACKAGE OUTLINE



PIN ASSIGNMENTS

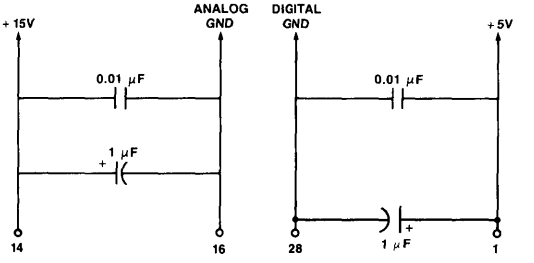
PIN	FUNCTION	PIN	FUNCTION
1	+5V	28	DIGITAL GND
2	BIT 1 (MSB)	27	BIT 9
3	BIT 2	26	BIT 10
4	BIT 3	25	BIT 11
5	BIT 4	24	BIT 12
6	BIT 5	23	BIT 13
7	BIT 6	22	BIT 14
8	BIT 7	21	BIT 15
9	BIT 8	20	BIT 16
10	LDAC	19	HBE
11	I_{OUT2}	18	$\overline{CS}$
12	I_{OUT1}	17	LBE
13	V_{REF}	16	ANALOG GND
14	+15V	15	R_F

ABSOLUTE MAXIMUM RATINGS (HS 9371)

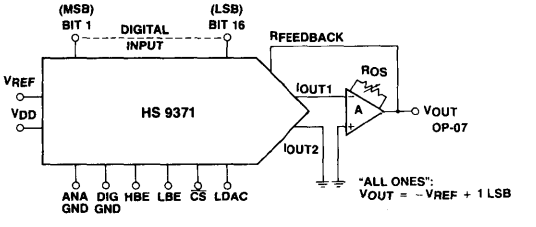
+15V Supply (+V_{DD}) to Analog GND . . . +17V
+5V Supply (+V_{CC}) to Digital GND . . . . +7V
Analog GND to Digital GND . . . . . ±0.5V
Digital Input Voltage to Digital GND . . . . . +V_{CC} + 0.3V max
Digital GND −0.3V min
$V_{REF\,IN}$ to Analog GND . . . . . ±25V
Output Voltage (Pins 11, 12) . . . . . Analog GND ±0.1V
Power Dissipation of Package
(Case A) . . . . . 1.4W @ +85°C
(Case B) . . . . . 1.5W @ +125°C
Lead Temperature, Soldering
(Case A) . . . . . 300°C, 5 sec
(Case B) . . . . . 300°C, 10 sec

APPLICATION INFORMATION

RECOMMENDED BYPASS CIRCUIT

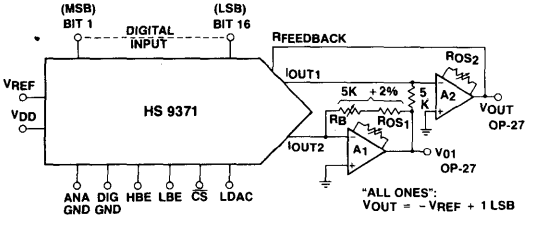


UNIPOLAR OPERATION *(2-Quadrant Multiplication)*



NOTE: To maintain specified HS 9371 linearity, the external amplifier (A) must be zeroed. Apply an ALL "ZEROS" digital input and adjust R_{OS} for V_{OUT} = 0 ± 1 mV.

BIPOLAR OPERATION *(4-Quadrant Multiplication)*



NOTE: To maintain specified HS 9371 linearity, external amplifiers (A_1 and A_2) must be zeroed. With a digital input of 10...0 and V_{REF} set to zero:
a) Set R_{OS1} for V_{01} = 0 ± 1 mV
b) Set R_{OS2} for V_{OUT} = 0 ± 1 mV
c) Set V_{REF} to +10V and adjust R_B for V_{OUT} to be 0 volts.

TRANSFER CHARACTERISTICS

UNIPOLAR OPERATION

BINARY INPUT	ANALOG OUTPUT
111...111	+F.S. − 1 LSB
100...000	+F.S./2
011...111	+F.S./2 − 1 LSB
000...000	0V

BIPOLAR OPERATION

BINARY INPUT	ANALOG OUTPUT
111...111	+F.S. − 1 LSB
100...000	0V
011...111	−1 LSB
000...000	−F.S.

MICROPROCESSOR INTERFACE CONSIDERATIONS

General

The HS 9371 is easily interfaced to either an 8-bit or 16-bit microprocessor. First, a signal to select (or address) the HS 9371 must be generated. Then the input data must be written (or latched) to the DAC and after settling, the analog output is valid.

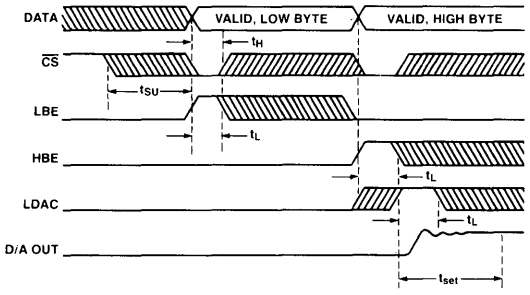
The bus interface logic consists of three independently addressable registers in two buffers. The first buffer consists of two 8-bit registers which can be loaded directly from an 8- or 16-bit microprocessor bus. Once the complete 16-bit word has been assembled in the first buffer, it can be loaded into the second buffer for conversion.

The required selection signal, $\overline{CS}$, is easily derived in most systems. Usually a base address is decoded and this active low signal is used for $\overline{CS}$. The active high signal for the low byte enable (LBE) and high byte enable (HBE) loads the two 8-bit registers into the first buffer while the LDAC signal loads the second buffer for conversion. The double-buffered input eliminates the generation of spurious analog output values.

MEMORY MAPPED INTERFACE TO 8-BIT μP

Figure 1 shows the timing sequence for operating the HS 9371 with an 8-bit μP bus and Figure 2 shows a general interface. Note that the pinout of the HS 9371 allows the user to run only 8 traces directly underneath the hybrid to connect to the two 8-bit input registers in the first buffer.

The HS 9371 is addressed by the chip select ($\overline{CS}$) signal going low for a minimum of 100 nsec. Since t_{su}, the minimum time required for the input data to be valid before $\overline{CS}$, LBE, or HBE are active, is 0 ns minimum, the $\overline{CS}$ signal can go low simultaneously with data. The low byte enable (LBE) signal going high loads the 8 LSBs into the lower register of the first buffer. After a minimum latch time of 100 nsec, the LBE signal going low latches the data in the lower register. A similar control signal and timing sequence is used to load the 8 MSBs into the upper register of the first buffer (HBE). The load DAC (LDAC) signal going high loads the full 16-bits of data from the first buffer into the second buffer and the D/A for conversion. A minimum latch time of 100 nsec is required for the LDAC signal. The analog output then changes to the new value within the specified settling time. Table 1 is a truth table for the control inputs.



t_{SU}	Setup time required for input data to be valid before $\overline{CS}$, LBE or HBE going active	0 nsec min
t_H	Hold time for $\overline{CS}$ to stay low	100 nsec min
t_L	Latch time for LBE, HBE, and LDAC	100 nsec min
t_{SET}	Settling time from LDAC going active to valid output	
	– 0.0015% F.S.R., all zeros to all ones	5 μ sec typ
	– 0.0015% F.S.R., midscale LSB transition	1 μ sec typ

Figure 1. Timing Diagram for Interface to 8-Bit μP Bus

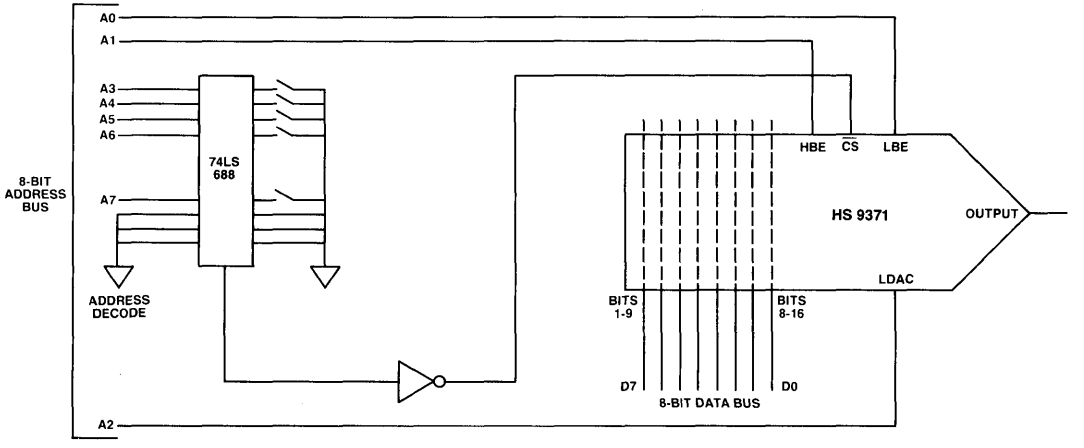


Figure 2. Block Diagram of HS 9371 Interfaced to 8-Bit μP

A_7-A_3 ($\overline{CS}$)	A_2 (LDAC)	A_1 (HBE)	A_0 (LBE)	OPERATION
Defined by switches to give low signal to $\overline{CS}$ when 9371 is addressed	0	0	0	All data latched
	0	0	1	Data into low byte of 1st buffer, all others latched
	0	1	0	Data into high byte of 1st buffer, all others latched
	0	1	1	Invalid address
	1	0	0	Data into 2nd buffer (16 bits) and D/A, 1st buffer latched
	1	0	1	Invalid address
	1	1	0	Invalid address
	1	1	1	Data directly to D/A from bus, latches transparent

Table 1. Truth Table – Control Inputs (References Figure 2)

MEMORY MAPPED INTERFACE TO 16-BIT μP

Figure 3 shows the timing sequence for operating the HS 9371 with a 16-bit μP bus and Figure 4 shows a general interface. Table 2 is a truth table for the control inputs. Note that the control inputs are simplified since the HBE and LBE signals can be connected together.

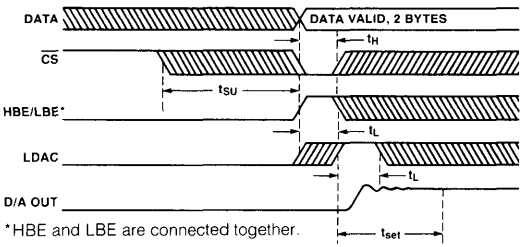


Figure 3. Timing Diagram for Interface to 16-Bit μP Bus

A_{15}-A_2 (CS)	A_1 (LDAC)	A_0 (HBE, LBE)	OPERATION
Defined by switches to give low signal to $\overline{CS}$ when 9371 is addressed	0	0	Data latched
	0	1	Data into 1st buffer, 2nd buffer latched
	1	0	Data into 2nd buffer, 1st buffer latched
	1	1	Data directly to D/A, latches transparent

Table 2. Truth Table – Control Inputs (References Figure 4)

POWER SUPPLY CONSIDERATIONS

Power supplies used for the HS 9371 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output voltage may result with noisy power sources. It is important to remember that 0.03 μA is 1 LSB for a 2 mA output. This translates to 156 μV for a 10 volt output range when converting to voltage.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10 μF tantalum type in parallel with 0.01 μF disc ceramic type.

ADDITIONAL RECOMMENDATIONS

1. For optimum performance, HS 9371 should be allowed sufficient warmup time (5 min.).
2. Due to the small bit weight (0.03 μA), noise becomes a noticeable factor; therefore, high quality sockets are recommended (if sockets are used) to minimize contact resistance.
3. No digital input should be left floating as the unit will draw excessive current. Unused digital inputs must be tied to a voltage potential between 0V and +5V.

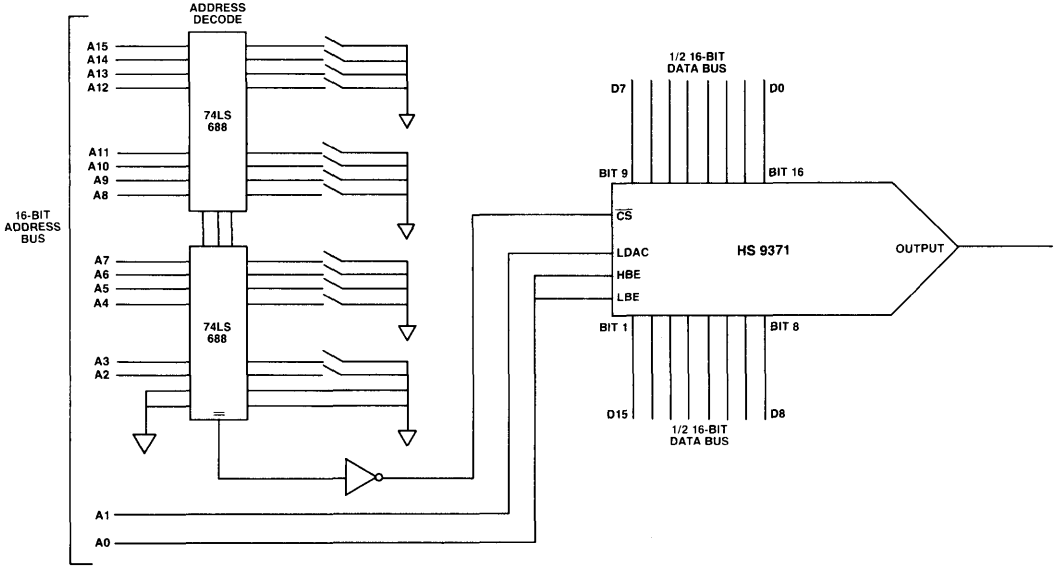


Figure 4. Block Diagram of HS 9371 Interfaced to 16-Bit μP

4. If optimum transient and glitch energy performance are required, electrically connect the lid (Case B) to pin 16.
5. If the D/A is driven from a non-buffered or heavily loaded bus, best linearity is obtained by adding 2K Ω pullups to the digital bit inputs.

CONTROL LOGIC

Figure 5 details the control logic function. Note that the LDAC signal is independent of the $\overline{CS}$ signal. All the latches are level controlled as opposed to edge triggered. This allows each of the latches to be operated in a transparent mode by tying the latch control input to a fixed logic "1" level. Since all 3 latches are independent of one another, the sequence of loading the 8 MSBs and the 8 LSBs is reversible.

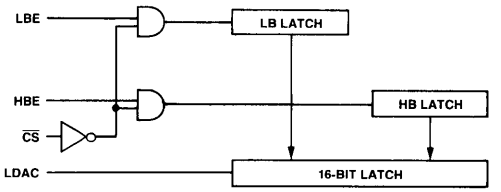


Figure 5. Control Logic Function

LAYOUT CONSIDERATIONS

Due to the small bit weight (0.03 μA for 1 LSB) special attention must be paid to the layout of the PC-board. To avoid capacitive coupling from digital lines to the hybrid substrate, a ground-plane should be placed directly under the converter package on the component side. This ground-plane can be directly connected to pin 16 of the HS 9371. All digital lines should run on the soldering side of the PC-board.

The pin assignment of the HS 9371 has been arranged so that the 16 digital inputs can be connected to an 8-bit data bus without crossing of bus lines (see Figure 2).

In general, analog and digital lines should be separated as far as possible and should not run in parallel. If analog and digital lines must cross, they should be at right angles to minimize coupling capacitance. The ground connection to the converter should be made using a wide, low resistive run to minimize voltage drop. Analog and digital ground lines must be connected at only one point, preferably directly at the converter package.

TERMINOLOGY

Major Carry Transition Settling: The total elapsed time between the application of a new input code and the point at which the analog output has settled to within a specified error band. The HS 9371 specifies settling to within 0.0015% FSR. For a major carry transition, the change is when the digital input goes from a "0" and all "1's" to a "1" and all "0's" or vice versa.

Full Scale Transition Settling: The same as major carry transition settling with the exception that the change is a full scale change. For the HS 9371, the change is from I_{OUT1} = 0 to I_{OUT1} = 2 mA or vice versa.

Monotonicity: A monotonic DAC means that the analog output does not decrease as the input is increased or vice versa. The relevant specification is over what temperature range and to what accuracy monotonicity is guaranteed.

A PRECISION SENSE-AND-CONTROL ROBOTICS SYSTEM

A counting A/D converter can be configured as a sense-and-control servo system for robotics applications. Figure 6 illustrates a bus-interfaced system which can:

1. Use the precision 16-Bit accurate HS 9371 as a D/A to provide a control voltage to a positioning device such as a motor or a speed controller such as a voltage to frequency converter.
2. Provide a tracking A/D function which allows a digital readout of position information.
3. Provide an infinite duration no-droop hold function for V_{SENSE}, under microprocessor control.

As shown, the system can traverse its entire output range of 0 to − 10V at approximately 10 Hz, which covers the entire 65,536 digital input (output) codes. This allows 1.5 μs for each successive count, or a clock rate to CCK of 667 kHz.

CIRCUIT OPERATION

A standard counting type A/D converter compares the output of a D/A converter to an external input signal and causes an N bit counter to move the N bit D/A inputs such that the D/A output converges to the external input signal. When the two signals are equal, the counter counts up and down on each successive clock, with the D/A output dithering on either side of the input by 1 LSB weight or less. The counter outputs are then a binary representation of the input (sense) voltage and the output (control) voltage.

This circuit has modified and expanded upon the basic configuration to provide a useable voltage output from the D/A (rather than the current output) and allow an easily scaled input voltage while being able to distinguish 16-Bit voltage difference levels (156 μV) at a 10V signal range).

ANALOG INS AND OUTS

The D/A-counter-comparator loop has been described. The HS OP-27 is used to convert the D/A output current to a 0 to − 10V signal. A comparator preamp is necessary at the 16-Bit level to ensure an adequate overdrive to a monolithic comparator because the response time of existing monolithic devices is inadequate for a 1.5 μs loop time. (Remember that all parts of the servo loop must settle to a 16-Bit level during each clock cycle; luckily the system moves by 1 LSB each cycle, so the voltage excursion is small.) A CA3127 monolithic transistor array is used for the differential pair and the output buffer devices.

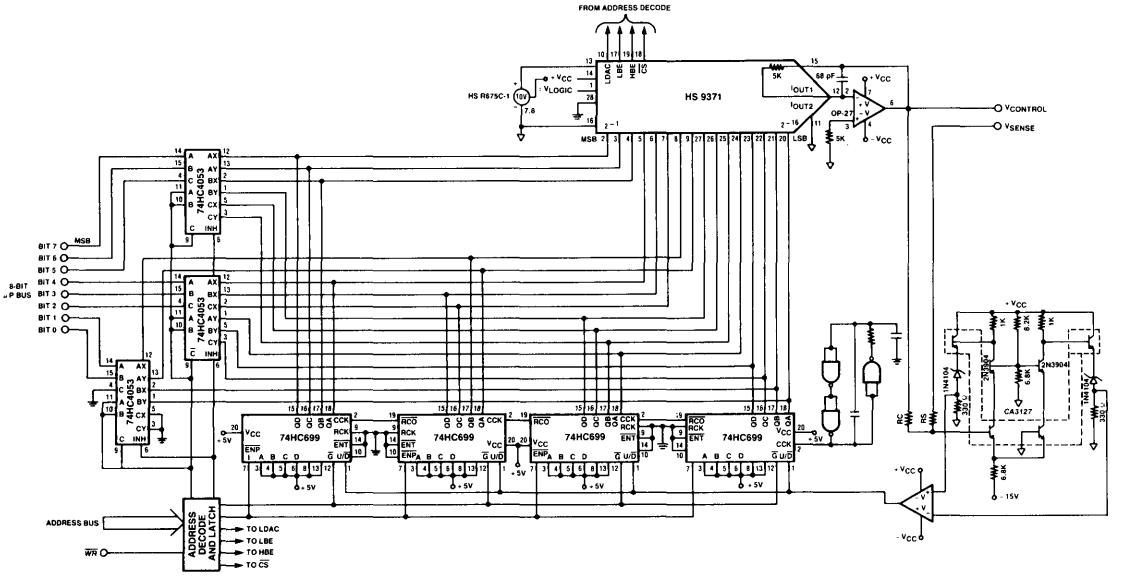


Figure 6. Bus Programmable Sense and Control Servo Loop for Precision Robotics Applications

The 1N4104 zener diodes provide a level shift of the preamp output to 3.3V to keep the signals within the common mode range of ±5V comparators such as the LT1016 and the LM360. The 2N3904 cascode devices may not be necessary in lower speed systems; a comparator such as the LM 319 or LM311 may also be used in less critical applications. The 1K gain setting resistors may be adjusted to trim offset voltage if the comparator has no such trim. The preamp is configured for a gain of 40, yielding an LSB output weight of (153 μV)*(40) = 6.1 mV to the comparator input.

Resistors RC and RS are used to compare $V_{CONTROL}$ and V_{SENSE}. With a positive 10V reference to the D/A converter (an HS R675C-1 is used for low noise and good transient response), a −10V full scale output is generated for $V_{CONTROL}$. This allows a 0V to positive V for V_{SENSE}, where

$$\frac{\max V_{CONTROL}}{RC} = \frac{\max V_{SENSE}}{RS}$$

is the constraint so that the input and output ranges match. If a 0V to negative V range is required, a negative reference such as the HS R675-3 can be used. A multiplexer (2:1 analog mux with low Ron) can be used to switch between negative and positive references at the V_{SENSE} zero crossing if a bipolar range is required.

DIGITAL UPS AND DOWNS

The comparator output must be a TTL or CMOS compatible signal which drives the UP/DOWN inputs of the counters. The four 4-Bit synchronous counters are cascaded to yield 16 binary outputs. Cascading results in a maximum rollover delay (for "HC" logic) of about 60-80 ns, which is small compared to the 1.5 μs minimum clock period. The $\overline{ENP}$ enable input is used to stop the count sequence for the "hold" function, while gate input $\overline{G}$ makes the outputs high impedance to allow the bus to load the D/A directly. If the system goes to the low or high end of the scale, the counter will roll over to the other end. If this is a problem (a linear versus rotary system), the ripple carry out $\overline{RCO}$ of the most significant counter can be exclusively NORed (XNOR) with the comparator output to cause the counter to toggle between its endpoint and 1 LSB away from the endpoint.

The bus interface uses 74HC4053s as a bidirectional 2:1 multiplexer with tri-state capability. The bus can load data into the D/A to force a specific control voltage. The bus interface in the HS 9371 can latch this data and act as a direct open-loop controller from the data bus with $\overline{ENP}$ high. If $\overline{ENP}$ is low, the 74HC4053s can be used to read the digital signal on the counter outputs in two 8-Bit bytes with the system in "track" mode. (If a two-byte read takes longer than one clock cycle, the tracking operation should be halted during READ to prevent erroneous data from being read.) To disconnect the bus from the servo system, make INH low. If both the counter and the bus can be tri-state, use pullup or pulldown resistors on the D/A inputs to prevent them from floating.

The address decode logic will be different for different processors and systems. It must be tailored to mate the address with the proper output signal polarity needed to drive the D/A interface signals and counter logic.

FINAL FEEDBACK

As with any highly sensitive analog circuit, care must be taken with circuit layout, power supply decoupling and ground paths. Keep clock signals away from analog signals, use analog ground plane underneath sensitive areas (especially the preamp and comparator) and minimize capacitive coupling between the comparator output and inputs. This coupling can cause oscillation which will preclude circuit operation. To prevent a linearity error due to ground resistance, route I_{OUT2} of the HS 9371 to the main analog ground via a separate trace from other low-level grounds. Connect analog and digital grounds at only one point, preferably near the D/A. Keep connections from the D/A to the preamp and comparator as short as possible. Follow decoupling procedures as described elsewhere in this data sheet.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the supply voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for techincal assistance.

LONG TERM DRIFT

Long-term drift of the DAC's transfer function, after initial trim of offset and gain, is composed of several factors which are discussed below.

a. Offset Drift. For maximum performance, the offset should be zeroed after at least one hour of operation. Then the offset drift will be typically 200 V for the first 1000 hrs; and 100 V per 1000 hrs thereafter.

b. Reference Voltage Drift. The intrinsic long-term drift of the breakdown voltage of the temperature compensated zener-diode in the reference voltage circuitry will cause a gain error at the output of the DAC. The drift that will occur is typically less than 1mV per year. A correction of this drift error can be made using the gain adjustment circuitry.

c. Output Amplifier Gain Change. Any noticeable gain change will be caused by a drift of the internal feedback resistor relative to the DAC's network impedance. This can contribute 10ppm F.S.R./1000 hrs, which can be corrected using the gain circuitry.

d. Linearity Drift. Due to the unique circuitry used in the DAC network, effects of resistor accuracy drift on linearity are greatly reduced. Typical differential linearity drift is less than 3ppm F.S.R./1000 hrs.

ORDERING INFORMATION

MODEL	MONOTONICITY (over temp.)	TEMPERATURE RANGE	SCREENING
HS 9371K	16 bits min	0°C to +70°C	—
HS 9371J	15 bits min	0°C to +70°C	—
HS 9371TB	16 bits min	−55°C to +125°C	MIL-STD-883C
HS 9371SB	15 bits min	−55°C to +125°C	MIL-STD-883C

Specifications subject to change without notice.

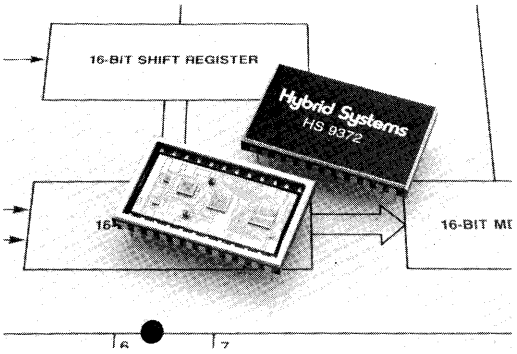
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9372

SERIAL INPUT, 16-BIT DAC

FEATURES

- Serial input
- Monotonic to 16-bits
- Asynchronous clear input
- Low power



DESCRIPTION

The HS9372 is a serial input, 16-bit, current output multiplying D/A converter with 16-bit monotonicity guaranteed over the commercial and military temperature ranges. A proprietary semi-custom gate array is used to significantly reduce digital feedthrough while internal decoupling capacitors reduce the effect of power supply perturbations.

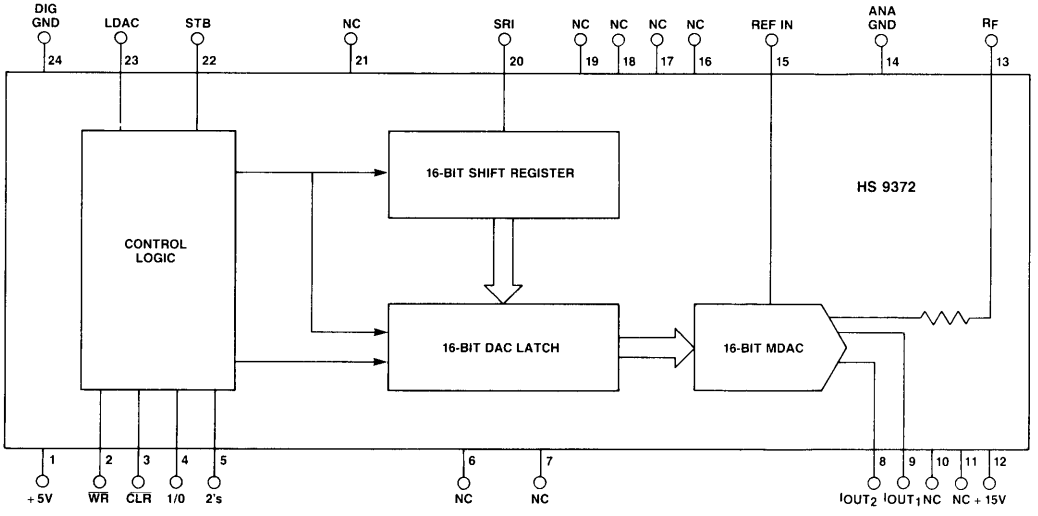
The data is clocked in serially (MSB first) to a shift register and then the 16-bit digital word is loaded into the DAC latch for conversion to analog out. Both unipolar and bipolar operation can be configured; in bipolar mode the input can be either offset binary coding or 2's complement coding.

A CLEAR input is provided for the asynchronous setting of the DAC latch to either all "0's" or "1" (MSB) and all "0's" depending on the user's choice.

The HS9372 is available for either commercial (0°C to +70°C) or military (−55°C to +125°C) applications. Screening to MIL-STD-883 Rev. C, Levels B or S is available.

7

FUNCTIONAL DIAGRAM

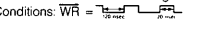


SPECIFICATIONS

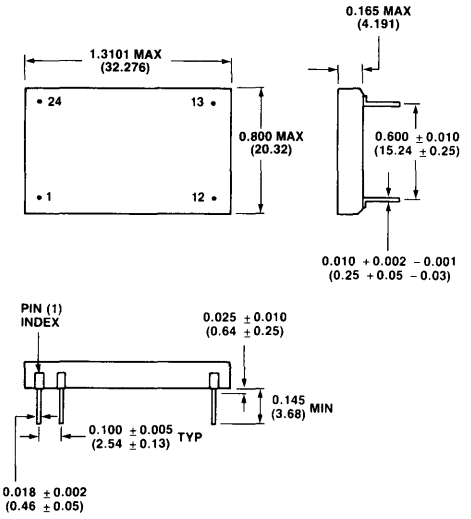
(Typical @ +25°C unless otherwise specified)

MODEL	HS 9372K	HS 9372J	HS 9372TB	HS 9372SB
DIGITAL INPUT				
Resolution	16-bits, Serial MSB first	*	*	*
Coding	Straight/Offset Binary/ 2's Complement[1]	*	*	*
Logic Compatibility	TTL, LSTTL, CMOS			
V_{IL} (max)[2]	0.8V	*	*	*
V_{IH} (min)[2]	2.4V	*	*	*
Input Current	10 μA max	*	*	*
SWITCHING CHARACTERISTICS[3]				
t_{WR} ($\overline{WR}$ pulse width)	120 nsec min	*	*	*
t_{AW} (STB and LDAC valid to end of $\overline{WR}$)	120 nsec min	*	*	*
t_{DW} (DATA valid to end of $\overline{WR}$)	120 nsec min	*	*	*
t_{DH} (DATA hold time)	0 nsec min	*	*	*
t_{AH} (STB and LDAC hold time)	0 nsec min	*	*	*
t_{WCL} ($\overline{CLR}$ pulse width)	200 nsec min	*	*	*
ANALOG OUTPUT				
Gain Accuracy	±0.1% F.S.R. typ, ±0.2% max[4]	*	*	*
Initial Offset Error	50 μV max[4,5]	*	*	*
Current Range				
Unipolar	0 to +2 mA	*	*	*
Bipolar	±1 mA	*	*	*
Noise				
p-p noise (0.1 Hz to 100 Hz)	50 μV p-p	*	*	*
Output Capacitance	80 pF	*	*	*
REFERENCE INPUT				
Input Impedance	5KΩ	*	*	*
STATIC PERFORMANCE				
Integral Linearity Error[6]	±0.0015% max	±0.003% max	±0.0015% max	±0.003% max
Differential Linearity Error	±0.0015% max	±0.003% max	±0.0015% max	±0.003% max
Monotonicity Guaranteed to: (over temperature)	16-bits	15-bits	16-bits	15-bits
DYNAMIC PERFORMANCE				
Major Carry Transition Settling to 0.0015% F.S.R.	1 μsec[7]	*	*	*
Full Scale Transition Settling to 0.0015% F.S.R.	5 μsec[7]	*	*	*
Reference Feedthrough Attenuation[8]	100 dB @ 100 Hz sine wave	*	*	*
	80 dB @ 1 kHz sine wave	*	*	*
Glitch Energy[8]	3 nV-sec	*	*	*
STABILITY				
Gain Drift	8 ppm/°C max	*	*	*
Offset Drift				
Unipolar	1 ppm/°C max	*	*	*
Bipolar	2 ppm/°C max	*	*	*
Linearity Drift	1 ppm/°C max	*	*	*
POWER SUPPLY				
Current				
+15V	1 mA max	*	*	*
+5V				
Static Consumption	50 μA max	*	*	*
Dynamic Consumption[9]	7 mA max	*	*	*
Power Dissipation				
Static	15.25 mW max	*	*	*
Dynamic	50 mW max	*	*	*
PSRR	±0.0006% FS/% typ ±0.002% FS/% max			
TEMPERATURE RANGE				
Operating	0°C to +70°C	*	−55°C to +125°C	*
Storage	−25°C to +85°C	*	−65°C to +150°C	*
PACKAGE				
24-pin, double DIP				

NOTES:

1. The coding is determined by the logic level on the 2's pin (see further).
2. Voltages at the digital inputs may not go below 0 volts or exceed +5V.
3. −55°C to +125°C.
4. Adjustable to zero.
5. Using the internal R_F with nulled external amplifier in a constant 25°C ambient.
6. Integral Linearity is measured per best straight line method.
7. 50 Ω load.
8. Lid of Case B units should be grounded to analog ground for optimum performance.
9. Conditions: $\overline{WR}$ = 

PACKAGE OUTLINE



Pin 1 is marked by a dot on the top of the package.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	24	DIGITAL GND
2	$\overline{WR}$	23	LDAC
3	$\overline{CLR}$	22	STB
4	1/0	21	NC
5	2's	20	SRI
6	NC	19	NC
7	NC	18	NC
8	I OUT 2	17	NC
9	I OUT 1	16	NC
10	NC	15	REF IN
11	NC	14	ANALOG GND
12	+15V	13	RF

NC — No internal connection.

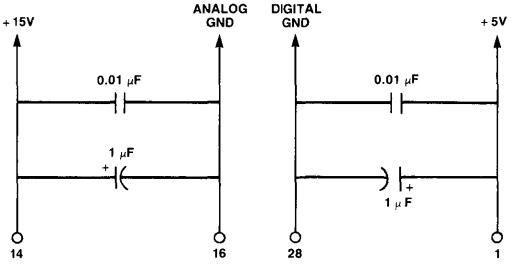
ABSOLUTE MAXIMUM RATINGS (HS 9372)

+15V Supply (+V_{DD}) to Analog GND . . . +17V
+5V Supply (−V_{CC}) to Digital GND . . . . +7V
Analog GND to Digital GND . . . . . ±0.5V
Digital Input Voltage to Digital GND . . . . . +V_{CC} + 0.3V max
Digital GND −0.3V min
$V_{REF\ IN}$ to Analog GND . . . . . ±25V
Output Voltage (Pins 8,9) . . . . . Analog GND ±0.1V
Power Dissipation of Package
(Case A) . . . . . 1.4W @ +85°C
(Case B) . . . . . 1.5W @ +125°C
Lead Temperature, Soldering
(Case A) . . . . . 300°C, 5 sec
(Case B) . . . . . 300°C, 10 sec

7

APPLICATION INFORMATION

RECOMMENDED BYPASS CIRCUIT



THEORY OF OPERATION

If the HS 9372 is to operate in unipolar mode or in bipolar mode with OFFSET BINARY coding, the 2's pin must be connected to 0 Volts. In bipolar mode with 2's COMPLEMENT coding, the 2's pin must be tied to +5 Volts.

The STB and LDAC pins address the shift register and the DAC latch respectively. When the shift register is addressed (LDAC = "0", STB = "1"), serial data appearing at the SRI pin will be clocked in on the falling edge of $\overline{WR}$. When the shift register is full, the DAC latch is addressed (STB = "0", LDAC = "1") and data will be transferred in by bringing $\overline{WR}$ momentarily low.

Using 1/0 pin in conjunction with the $\overline{CLR}$ pin, the DAC output can be set asynchronously to 0 Volts in both unipolar and bipolar mode (offset binary or 2's complement code). This occurs by bringing $\overline{CLR}$ low. Table 1 indicates how to connect 1/0 pin in the different cases.

MODE	CODING	1/0 PIN
Unipolar	Straight Binary (2's = "0")	"0"
Bipolar	Offset Binary (2's = "0")	"1"
Bipolar	2's Complement (2's = "1")	"0"

Table 1

This feature allows an easy system initialization and simplifies the DAC calibration (see "Unipolar Operation" and "Bipolar Operation" paragraphs).

Table 2 is a truth table for the logic control inputs.

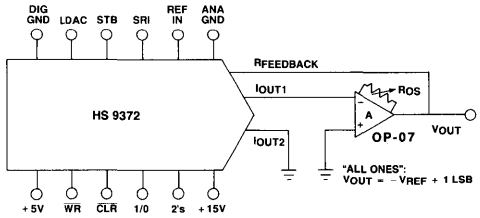
CONTROL INPUTS				OPERATION
$\overline{CLR}$	$\overline{WR}$	STB	LDAC	
0	X	X	X	Clear DAC latch to 00...00 if 1/0 is Dig Gnd 10...00 if 1/0 is +5V (asynchronous operation)
1	1	X	X	Device not selected, output
1	X	0	0	reflects previously loaded data
1	⌐[1]	1	0	Strobe data into the shift register
1	⌐	0	1	Load data into the DAC latch[2]
1	⌐	1	1	Invalid address

Table 2. Truth Table — Control Inputs

NOTES:

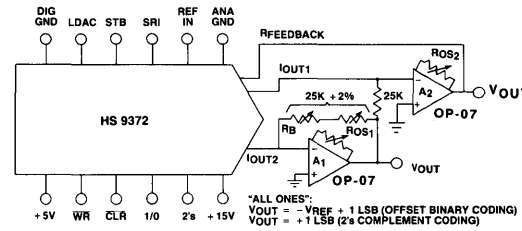
1. ⌐ = edge sensitive (falling edge)
   ⌐ = level sensitive (low)
2. If 2's = "1", data is loaded in 2's complement coding for the bipolar mode. If 2's = "0", data is loaded in offset binary coding for the bipolar mode and in direct binary coding for the unipolar mode.

UNIPOLAR OPERATION *(2's = "0")*



NOTE: To maintain specified HS 9372 linearity, the external amplifier (A) must be zeroed. This operation is easily performed without having to serially load an "all 0's" code: set $\overline{CLR}$ and 1/0 to logic level "0" and adjust R_{OS} for $V_{OUT} = 0 \pm 1$ mV.

BIPOLAR OPERATION *(4-Quadrant Multiplication)*



NOTE: To maintain specified HS 9372 linearity, external amplifiers (A_1 and A_2) must be zeroed. For offset binary coding (2's = "0"), set $\overline{CLR}$ = "0" and 1/0 = "1" and then follow steps A & B below. For two's complement coding (2's = "1"), set $\overline{CLR}$ and 1/0 = "0" and then follow steps A & B below.

a) With REF IN = 0, set R_{OS1} for $V_{O1} = 0 \pm 1$ mV and R_{OS2} for $V_{OUT} = 0 \pm 1$ mV.

b) Set REF IN to +10V and adjust R_B for V_{OUT} to be 0 volts.

TRANSFER CHARACTERISTICS

UNIPOLAR OPERATION

BINARY INPUT	ANALOG OUTPUT
1 1 1...1 1 1	+F.S. −1 LSB
1 0 0...0 0 0	+F.S./2
0 1 1...1 1 1	+F.S./2 −1 LSB
0 0 0...0 0 0	0V

BIPOLAR OPERATION

OFFSET BINARY INPUT	ANALOG OUTPUT
1 1 1...1 1 1	+F.S. −1 LSB
1 0 0...0 0 0	0V
0 1 1...1 1 1	−1 LSB
0 0 0...0 0 0	−F.S.

BIPOLAR OPERATION

2's COMPLEMENT INPUT	ANALOG OUTPUT
0 1 1...1 1 1	+F.S. −1 LSB
0 0 0...0 0 0	0V
1 1 1...1 1 1	−1 LSB
1 0 0...0 0 0	−FS

TIMING INFORMATION

Figure 1 is the timing diagram for loading the shift register. Figure 2 is the timing diagram for loading the DAC latch. Figure 3 is a global timing diagram for the complete operation of the HS 9372.

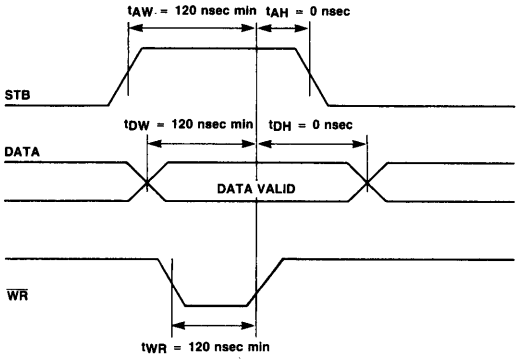


Figure 1. Loading the Shift Register (LDAC = "0") through the SRI Pin. Write Cycle #1 to 16.

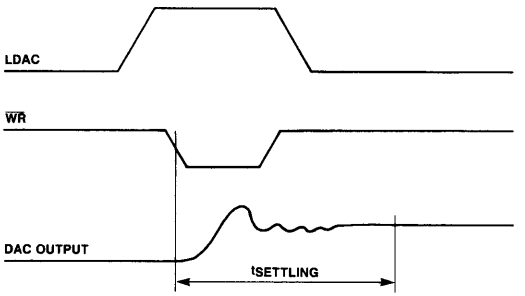


Figure 2. Loading the DAC Latch (STB = "0") from the Shift Register. Write Cycle #17.

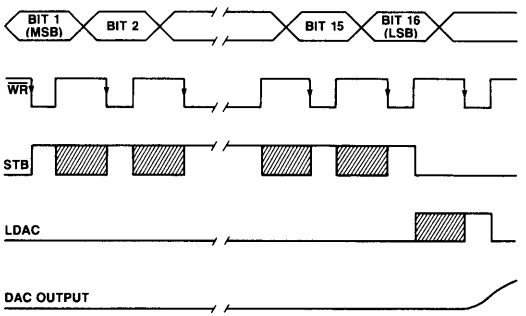


Figure 3. Global Timing for Complete Operation of the HS 9372.

MICROPROCESSOR INTERFACE

The timing information described earlier is fully compatible with the timing of several microprocessors (Intel, Zilog, etc.) without the addition of any external components. Figure 4 is a general example of interfacing the HS 9372 to an 8-bit μP. It is followed by a routine example.

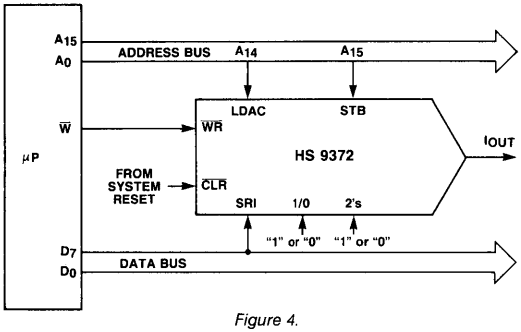


Figure 4.

ROUTINE SOFTWARE PROGRAM

Assumptions:

1. The first byte of data is at memory address 0000.
2. The second byte of data is a memory address 0001.
3. A = accumulator of the μP.
4. B = general register of the μP.
5. 4000 is the address of the DAC latch ($A_{14} = 1$; $A_{15} = 0$)
6. 8000 is the address of the shift register ($A_{14} = 0$; $A_{15} = 1$)

LOAD the value 8 in register B.
LOAD in the accumulator A of the μP the content of memory address 0000.
JUMP to SHIFT (SHIFT is the *subroutine* which allows the loading of data in the input register).
LOAD the value 8 in register B.
LOAD in A the second byte of data which is at memory address 0001.
JUMP to SHIFT.
WRITE at the address 4000 (a memory write instruction at the address 4000 loads the data in the DAC latch).
END.

SHIFT WRITE at the address 8000 (a memory write instruction at the address 8000 loads the data bit by bit in the shift register).
ROTATE LEFT the content of A.
DECREMENT B.
If B $\neq$ 0, GOTO SHIFT.
RETURN from subroutine.

POWER SUPPLY CONSIDERATIONS

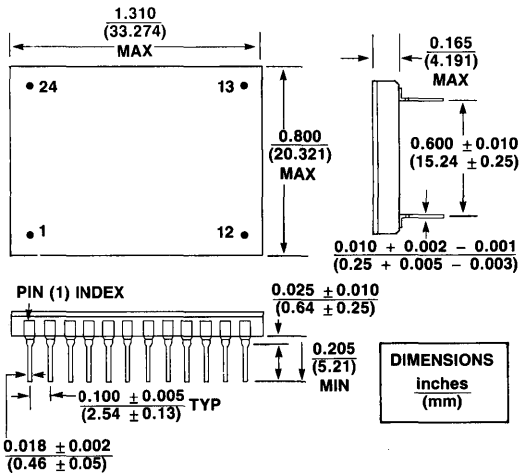
Power supplies used for the HS 9372 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output voltage may result with noisy power sources. It is important to remember that 0.03 μA is 1 LSB for a 2 mA output. This translates to 156 μV for a 10 volt output range when converting to voltage.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10 μF tantalum type in parallel with 0.01 μF disc ceramic type.

LAYOUT CONSIDERATIONS

Due to the small bit weight (0.03 μA for 1 LSB) special attention must be paid to the layout of the PC-board. To avoid capacitive coupling from digital lines to the hybrid substrate, a ground-plane should be placed directly under the converter package on the component side. This ground-plane can be directly connected to pin 14 of the HS 9372. All digital lines should run on the soldering side of the PC-board.

In general, analog and digital lines should be separated as far as possible and should not run in parallel. If analog and digital lines must cross, they should be at right angles to minimize coupling capacitance. The ground connection to the converter should be made using a wide, low resistive run to minimize voltage drop. Analog and digital ground lines must be connected at only one point, preferably directly at the converter package.



LONG TERM DRIFT

Long-term drift of the DAC's transfer function, after initial trim of offset and gain, is composed of several factors which are discussed below.

a. Offset Drift. For maximum performance, the offset should be zeroed after at least one hour of operation. Then the offset drift will be typically 200 μV for the first 1000 hrs; and 100 μV per 1000 hrs thereafter.

b. Reference Voltage Drift. The intrinsic long-term drift of the breakdown voltage of the temperature compensated zener-diode in the reference voltage circuitry will cause a gain error at the output of the DAC. The drift that will occur is typically less than 1mV per year. A correction of this drift error can be made using the gain adjustment circuitry.

c. Output Amplifier Gain Change. Any noticeable gain change will be caused by a drift of the internal feedback resistor relative to the DAC's network impedance. This can contribute 10ppm F.S.R./1000 hrs, which can be corrected using the gain circuitry.

d. Linearity Drift. Due to the unique circuitry used in the DAC network, effects of resistor accuracy drift on linearity are greatly reduced. Typical differential linearity drift is less than 3ppm F.S.R./1000 hrs.

ORDERING INFORMATION

MODEL	MONOTONICITY (over temp.)	TEMPERATURE RANGE	SCREENING
HS 9372K	16 bits min	0°C to +70°C	—
HS 9372J	15 bits min	0°C to +70°C	—
HS 9372TB	16 bits min	−55°C to +125°C	MIL-STD-883C
HS 9372SB	15 bits min	−55°C to +125°C	MIL-STD-883C

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

DAC9377-SERIES

COMPLETE BUFFERED 16-BIT DAC

FEATURES

- True 16-bit (0.0008%) linearity
- μP compatible
- Complete
- 24-pin package
- Low power — 450mW
- Low cost
- Binary or BCD code

DESCRIPTION

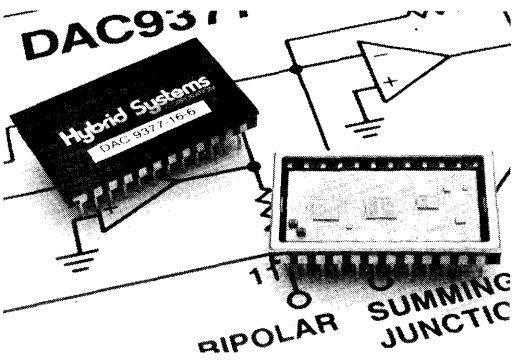
The DAC9377-16 is a complete, voltage output, 16-bit D/A converter with true 16-bit linearity. Complete with storage registers, internal reference and output amplifier, DAC9377-16 provides the user with exceptional performance and self-contained operation. The input storage register is composed of 16 parallel latches — a system compatible with 16-bit data bus interfaces. A single proprietary monolithic chip contains switches, storage registers and other electronics for high resolution and low linearity error. TTL and CMOS compatibility combined with low power dissipation in a ceramic 24-pin DIP, makes the DAC9377-16 unsurpassed in a high resolution data conversion device.

True 16-Bit Linearity — 16-bit (±0.0008%) linearity in a 24-pin DIP is unequaled. No other microcircuit converter does better. Additional versions with 15-and 14-bit linearity are also available.

Low Power — CMOS proprietary monolithic devices in a unique circuit configuration yield the lowest power dissipation (450 mW typ.) of any complete 16-bit converter available.

Complete — No external components are required for 16-bit conversion.

Input Storage Registers — Designed in one 16-bit segment, the input storage register provides data storage when latched, but is "transparent" when unlatched. The latch control is level-triggered for either static or dynamic operation.

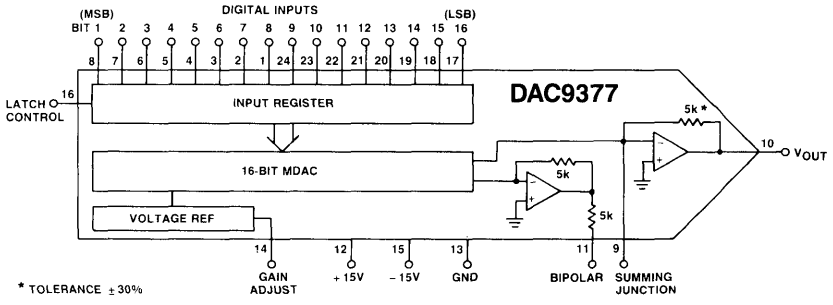


Reliability — A proven performer, the DAC9377-16 is packaged in a 24-pin ceramic DIP for the utmost in reliability. Combined with our proprietary monolithic device and automatic wirebonding, we've made the DAC9377-16 the most reliable device to date. Reliability is further enhanced by batch-processed, precision laser-trimmed resistor networks fabricated in our own facility. Networks are functionally trimmed and glass passivated to assure reliability under adverse environmental conditions.

Advanced designs, proven processes and continuous monitoring during all production operations by our quality control organization are combined with rigorous AQL screening to provide the most dependable, low cost D/A converter possible.

7

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C unipolar operation and nominal power supply, no load)

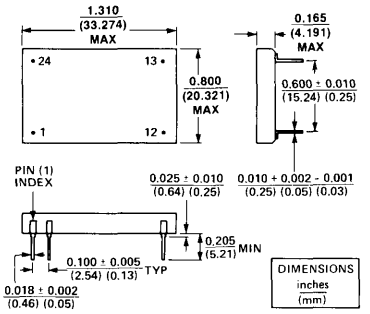
MODEL	DAC9377-16-6	DAC9377-16-5	DAC9377-16-4	DAC9377-4D
TYPE	Latched Inputs	*	*	*
DIGITAL INPUT				
Resolution	16-Bits	*	*	*
Unipolar Coding	Binary	*	*	BCD
Bipolar Coding	Offset Binary	*	*	N.A.
Logic Compatibility[1]	TTL, CMOS	*	*	*
Input Leakage Current	±1μA (max) 0.4V>V_{LOGIC}>3.2V	*	*	*
Latch Control Width	250nS (min)	*	*	*
Data Set-up Time[2]	500nS (*min*)	*	*	*
Data Hold Time[3]	0nS (min)	*	*	*
ANALOG OUTPUT				
Scale Factor[4]	0.1% F.S.R. (typ)	*	*	*
Initial Offset[4]	0.15% F.S.R. (*max*)			
Unipolar	±0.05% F.S.R. (max)	*	*	*
Bipolar	±0.10% F.S.R. (max)	*	*	N.A.
Voltage Range				
Unipolar	0 to +10V	*	*	*
Bipolar	±10V	*	*	N.A.
Current Compliance	±5mA	*	*	*
Output Impedance	<0.1Ω	*	*	*
Noise				
PP-noise (wideband)	±0.0005% F.S.R.	*	*	*
REFERENCE				
Voltage	−10V (internal)	*	*	*
Drift	5ppm/°C	*	*	*
Stability	1mV/yr	*	*	*
STATIC PERFORMANCE				
Integral Linearity[6]	±0.0008% F.S.R. (typ)	±0.0015% F.S.R. (typ)	±0.0015% F.S.R. (typ)	±0.002% F.S.R. (typ)
	±0.0015% F.S.R. (max)	±0.002% F.S.R. (max)	±0.003% F.S.R. (max)	±0.005% F.S.R. (max)
Differential Linearity[7]	±0.0004% F.S.R. (typ)	±0.0008% F.S.R. (typ)	±0.0015% F.S.R. (typ)	±0.005% F.S.R. (typ)
	±0.0015% F.S.R. (max)	±0.003% F.S.R. (max)	±0.006% F.S.R. (max)	±0.01% F.S.R. (max)
Monotonicity	Guaranteed to 16-bits	Guaranteed to 15-bits	Guaranteed to 14-bits	
DYNAMIC PERFORMANCE				
Major Carry Transition Settling to 0.006% F.S.R. (strobed)	20μS	*	*	*
Slew Rate	0.20V/μS	*	*	*
STABILITY[5] (Over Specified Temp. Range)				
Gain	8ppm/°C F.S.R. (max)	*	*	*
Linearity	1ppm/°C F.S.R. (max)	*	*	5ppm/°C
Differential Linearity	1ppm/°C F.S.R. (max)	*	*	5ppm/°C
Offset Drift				
Unipolar	3ppm/°C F.S.R.	*	*	*
Bipolar	5ppm/°C F.S.R.	*	*	*
POWER SUPPLY				
Requirements	+15V ±5% @ 15mA (max)	*	*	*
	−15V ±5% @ 20mA (max)	*	*	*
Rejection Ratio	0.003%/% (max)	*	*	*
Power Dissipation	450mW, 600mW max	*	*	*
TEMPERATURE RANGE				
Operating	0°C to +70°C	*	*	*
Storage	−25°C to +85°C	*	*	*
MECHANICAL				
Case Style	24 pin, double-DIP			
Case Dimensions				

NOTES:

* Same as DAC9377-16-6

1. Digital input voltage must not exceed supply voltage or go below −0.5V;
2. Time, data must be stable before latch control goes to "0".
3. Time, data must be stable after latch control goes to "0".
4. See APPLICATIONS INFORMATION for calibration procedure.
5. See APPLICATIONS NOTES.
6. Integral Linearity, for this product, is measured as the arithmetic mean value of the magnitudes of the greatest positive deviation and the greatest negative deviation from the theoretical value for any given input combination.
7. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.

Package Outline



Pin Connections

Unipolar Output: Ground pin 11 (No Connection for BCD)

Bipolar Output: Connect pin 11 to pin 9 (Binary Only)

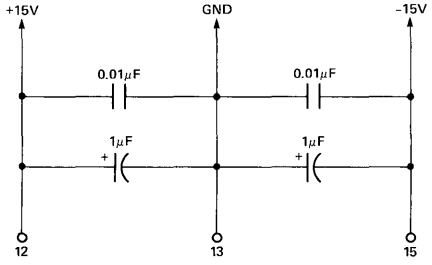
PIN DESIGNATIONS

PIN	FUNCTION		PIN	FUNCTION	
	Binary	BCD		Binary	BCD
1	2^{-8}	(100)	24	2^{-9}	(80)
2	2^{-7}	(200)	23	2^{-10}	(40)
3	2^{-6}	(400)	22	2^{-11}	(20)
4	2^{-5}	(800)	21	2^{-12}	(10)
5	2^{-4}	(1000)	20	2^{-13}	(8)
6	2^{-3}	(2000)	19	2^{-14}	(4)
7	2^{-2}	(4000)	18	2^{-15}	(2)
8	2^{-1}	(8000)	17	2^{-16}	(1)
9	SUMMING JUNCTION		16	LATCH CONTROL	
10	OUT		15	−15V	
11	BIPOLAR	N/C	14	GAIN ADJUST	
12	+15V		13	GND	

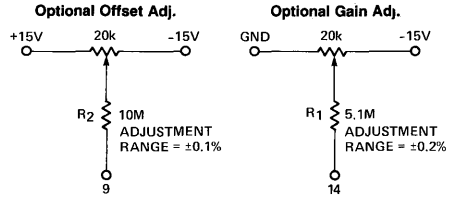
Note on BCD pin 11 must have no connection.

APPLICATIONS INFORMATION

RECOMMENDED BYPASS CIRCUIT



OPTIONAL GAIN & OFFSET ADJUSTMENT CIRCUIT



Values of R_1 & R_2 can be changed to increase or decrease the sensitivity of the adjustment. This adjustment should not be greater than ±1% around the nominal value for best performance.

CALIBRATION PROCEDURE
(for optional external Gain & Offset adjustment)

Unipolar operation:
1. Apply a 0 0 0 . . . 0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 1 1 1 . . . 1 input code and set the GAIN ADJ pot for F.S. − 1 LSB.

Bipolar operation:
1. Apply a 1 0 0 . . . 0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 0 0 0 . . . 0 input code and set the GAIN ADJ pot for − F.S.

TRANSFER CHARACTERISTICS

Unipolar Operation

BINARY INPUT	ANALOG OUTPUT
111...111	+F.S. −1 LSB
100...000	+F.S./2
011...111	+F.S./2 −1 LSB
000...000	0V

Bipolar Operation

BINARY INPUT	ANALOG OUTPUT
111...111	+F.S. −1 LSB
100...000	0V
011...111	−1 LSB
000...000	−F.S.

BCD Operation

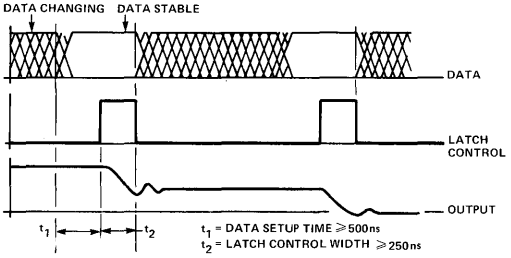
BCD INPUT	VOLTAGE OUTPUT
9 9 9 9	9.999 Volts
5 0 0 0	5.000 Volts
2 5 0 0	2.500 Volts
0 0 0 0	0.000 Volts

APPLICATION NOTES

TIMING DIAGRAM

LATCH CONTROL

Latch Strobe Input	Function
0	data latched (held)
1	data changing (transfer)



INTERNAL REFERENCE (NOTE4)

Buffered bootstrap design of the reference voltage is totally internal. A temperature compensated −6.2 volt planar-zener diode minimizes temperature drift. The voltage can be monitored with a high impedance digital voltmeter at pin 14 (GAIN ADJUST).

SETTLING TIME

The DAC9377-16 incorporates input buffering circuits whose propagation time introduces a skewing of the digital data reaching the bit switches. The skewing results in the bit switches not operating synchronously with each data change, producing an increase in the settling time (1 to 2 microseconds) and large "glitches". The dynamic performance of the DAC9377-16 can be greatly improved by using the internal latches which are available on these units. The latches are located after the input buffer circuits and just before the bit switches. When correctly strobed the latches present a data change to the bit switches in a synchronous manner. The latches should be closed while the input data is changing and propagating through the buffers. After the digital data has settled the latch is loaded and the "new" data is transferred to the switches synchronously. The latch is then closed and is ready for the next data update.

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APPLICATION NOTES

OUTPUT NOISE

Noticeable amounts of noise at both low and high input levels can be prevented through output noise filtering. Care must be taken in choosing an output filter network that will not slow down the operating speed beyond what is desired.

ADDITIONAL RECOMMENDATIONS

1. For optimum performance, DAC9377-16 should be allowed sufficient warmup time (5 min).
2. Due to the small bit weight (152μV), noise becomes a noticeable factor; therefore, high quality sockets are recommended, if sockets are used, to minimize contact resistance.
3. When changing output/gain range, a resistor (connected between pins 9 and 10) with a temperature coefficient between 0 and 10ppm/°C, is required to keep the DAC9377-16 within guaranteed specifications.
4. No digital input should be left floating as the unit will draw excessive current.
5. Power supplys should be applied before or at the same times as the digital input supply.

LONG TERM DRIFT

Long-term drift of the DAC's transfer function, after initial trim of offset and gain, is composed of several factors which are discussed below.

a. Offset Drift. For maximum performance, the offset should be zeroed after at least one hour of operation. Then the offset drift will be typically 200μV for the first 1000 hrs; and 100μV per 1000 hrs thereafter.

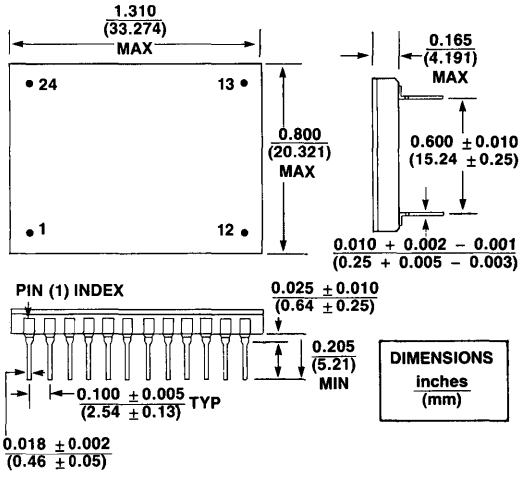
b. Reference Voltage Drift. The intrinsic long-term drift of the breakdown voltage of the temperature compensated zener-diode in the reference voltage circuitry will cause a gain error at the output of the DAC. The drift that will occur is typically less than 1mV per year. A correction of this drift error can be made using the gain adjustment circuitry.

c. Output Amplifier Gain Change. Any noticeable gain change will be caused by a drift of the internal feedback resistor relative to the DAC's network impedance. This can contribute 10ppm F.S.R./1000 hrs, which can be corrected using the gain circuitry.

d. Linearity Drift. Due to the unique circuitry used in the DAC network, effects of resistor accuracy drift on linearity are greatly reduced. Typical differential linearity drift is less than 3ppm F.S.R./1000 hrs.

IMPORTANT NOTICE TO THE USER: When measuring the stability of the DAC9377-16, care should be taken so that the drift of the measurement instruments can be separated from the drift factors mentioned above and the measurements are taken at identical temperatures.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.



ORDERING INFORMATION

MODEL	DESCRIPTION
DAC9377-16-6	16-Bit DAC with 16-bit linearity
DAC9377-16-5	16-Bit DAC with 15-bit linearity
DAC9377-16-4	16-Bit DAC with 14-bit linearity
DAC9377-4D	16-Bit 4 Decade BCD

Specifications subject to change without notice.

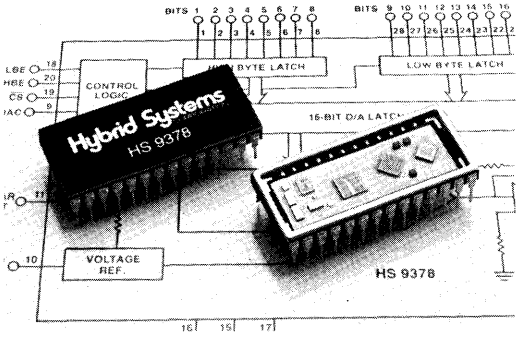
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9378 SERIES

μP COMPATIBLE, 16-BIT DAC

FEATURES

- Monotonic to 16-bits at 25°C
- Double buffered input
- Proprietary semicustom gate array significantly reduces digital feedthrough
- Pinout permits 16 digital input lines to be connected to an 8-bit data bus without crossing bus lines



DESCRIPTION

The HS9378 is a complete voltage output, 16-bit D/A converter with 16-bit monotonicity guaranteed at room temperature. Complete with dual storage registers, internal reference and an output amplifier, the HS9378 series easily interfaces with either 8-bit or 16-bit bus structures, eliminating the need for external latches.

A proprietary semicustom gate array is used to significantly reduce digital feedthrough while internal decoupling capacitors reduce the effect of power supply perturbations.

The HS9378 has dual 8-bit input registers for direct interface to 8- or 16-bit bus structures. The pinout of the HS9378 allows the user with an 8-bit bus to run only 8 traces directly underneath the hybrid to connect to the 16-bit input register.

The HS9378 is available for either commercial (+0°C to +70°C) or military (−55°C to +125°C) applications. Screening to MIL-STD-883 Rev. C, Levels B or S, is available.

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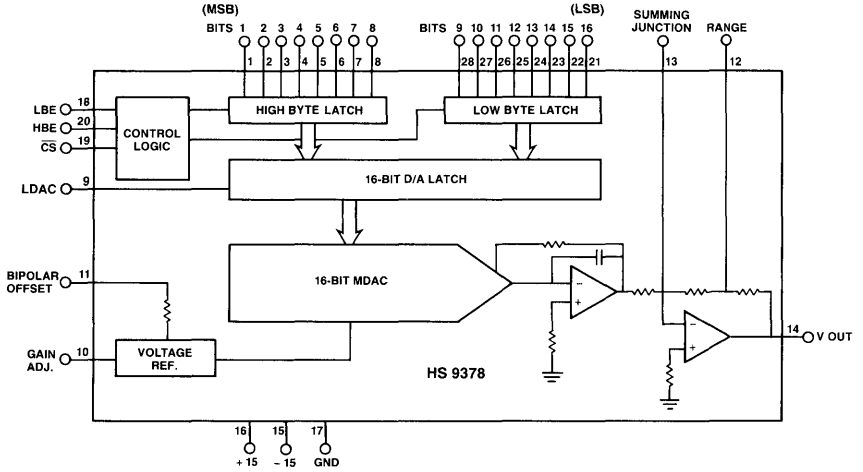
FUNCTIONAL DIAGRAM



SPECIFICATIONS

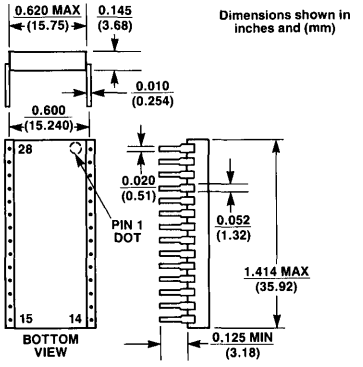
(Typical @ +25°C unless otherwise specified)

MODEL	HS 9378C	HS 9378TB	HS 9378SB
DIGITAL INPUT			
Resolution	16-bits	•	•
Coding	*Straight/Offset* Binary	•	•
Logic Compatibility	TTL, LSTTL, CMOS		
V_{IL} (max)[6]	0.8V	•	•
V_{IH} (min)[6]	2.4V		
Input Current	10 μA max	•	•
Latch Control Minimum Pulse Width	100 nsec	•	•
Data Set-Up Time	100 nsec min[1]	•	•
Data Hold Time	0 nsec	•	•
ANALOG OUTPUT			
Scale Factor Error	±0.20% F.S.R. max[2]	•	•
Initial Offset			
Unipolar	±0.15% F.S.R. max[2]	±0.05% F.S.R. max[2]	±0.05% F.S.R. max[2]
Bipolar	±0.15% F.S.R. max[2]	±0.05% F.S.R. max[2]	±0.05% F.S.R. max[2]
Voltage Range			
Unipolar	0 to +10V	•	•
Bipolar	±5V, ±10V	•	•
Current Compliance[5]	5 mA	•	•
Output Impedance	1Ω max	•	•
Noise p-p noise (0.1 Hz to 100 Hz)	50 μV	•	•
STATIC PERFORMANCE			
Integral Linearity Error[3]	0.0008% typ 0.0015% max	0.0008% typ 0.0015% max	0.0015% typ 0.003% max
Differential Linearity Error[4]	0.0015% max	•	0.003% max
Monotonicity Guaranteed to:			
(room temperature)	16 bits	16 bits	15 bits
(over temperature)	15 bits	15 bits	14 bits
Glitch Energy[7]	3 nV-sec	•	•
DYNAMIC PERFORMANCE			
Major Carry Transition Settling to 0.0015% F.S.R.	16 μsec	•	•
Slew Rate	1.7 v/μsec	•	•
Full Scale Transition Settling to 0.0015% F.S.R.	22 μsec	•	•
STABILITY			
Gain	10 ppm/°C max	10 ppm/°C max	15 ppm/°C max
Linearity Drift	1 ppm/°C max	•	•
Offset Drift			
Unipolar	5 ppm/°C max	2 ppm/°C	5 ppm/°C
Bipolar	10 ppm/°C max	5 ppm/°C	10 ppm/°C
POWER SUPPLY			
Requirements	+15V, ±5% @ 26.3 mA max	•	•
	−15V, ±5% @ 10.3 mA max	•	•
Rejection Ratio	±0.0006% FS/% V_{CC} typ, ±0.002% FS/% V_{CC} max	•	•
Power Dissipation	425 mW typ, 550 mW max	•	•
TEMPERATURE RANGE			
Operating			
C-model	+0°C to +70°C		
B-model	−55°C to +125°C		
Storage			
C-model	−25°C to +85°C		
B-model	−65°C to +150°C		
PACKAGE			
28-pin, double DIP			

NOTES:

1. −55°C to +125°C.
2. Adjustable to zero.
3. Integral Linearity is measured per end point definition.
4. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
5. Analog output is fully protected against infinite duration short circuit to ground.
6. Voltages at the digital inputs may not go below 0 volts or exceed +5V.
7. For minimum glitch, lid of Case B units should be grounded.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	28	BIT 9
2	BIT 2	27	BIT 10
3	BIT 3	26	BIT 11
4	BIT 4	25	BIT 12
5	BIT 5	24	BIT 13
6	BIT 6	23	BIT 14
7	BIT 7	22	BIT 15
8	BIT 8	21	BIT 16 (LSB)
9	LDAC	20	HBE
10	GAIN ADJ	19	$\overline{CS}$
11	BIPOLAR OFFSET	18	LBE
12	RANGE	17	GND
13	SUM JCT	16	+15V
14	V_{out}	15	−15V

ABSOLUTE MAXIMUM RATINGS (HS 9378)

+15V Supply (+V_{DD}) to GND ..... +17V

−15V Supply (−V_{DD}) to GND ..... −22V

Digital Input Voltage to GND 6.5V

Analog Input Voltage to GND

Pins 10, 12 ..... ±V_{DD}

Pin 11 ..... +V_{DD} max, −9V min

Pin 13 ..... ±0.1V

V_{OUT} ..... Indefinite short to GND

Package Power Dissipation

(Case A) ..... 1.4W @ +85°C

(Case B) ..... 1.5W @ +125°C

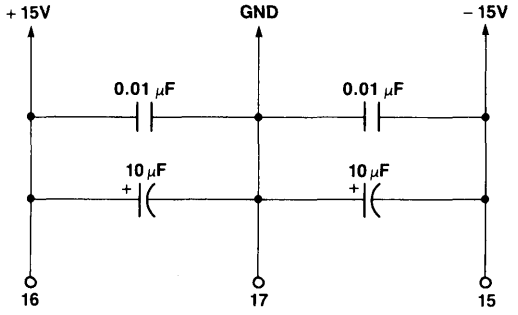
Lead Temperature, Soldering

(Case A) ..... 300°C, 5 sec

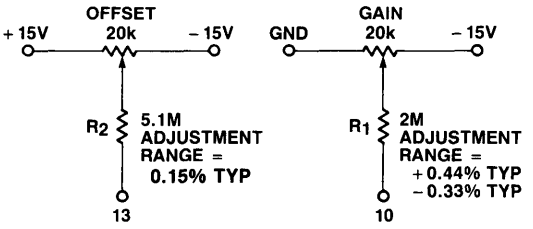
(Case B) ..... 300°C, 10 sec

APPLICATIONS INFORMATION

RECOMMENDED BYPASS CIRCUIT



OPTIONAL OFFSET & GAIN ADJUSTMENT CIRCUIT



Values of R_1 & R_2 can be changed to increase or decrease the sensitivity of the adjustment. (This adjustment should not be greater than ±1% around the nominal value for best performance.) Decreasing the R_1/R_2 value increases the range of adjustment.

CALIBRATION PROCEDURE
(for optional external Gain & Offset adjustment)

Unipolar operation:

1. Apply a 0 0 0...0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 1 1 1...1 input code and set the GAIN ADJ pot for F.S. − 1 LSB.

Bipolar operation:

1. Apply a 1 0 0...0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 0 0 0...0 input code and set the GAIN ADJ pot for − F.S.

TRANSFER CHARACTERISTICS

UNIPOLAR OPERATION

BINARY INPUT	ANALOG OUTPUT
1 1 1...1 1 1	+F.S. − 1 LSB
1 0 0...0 0 0	+F.S./2
0 1 1...1 1 1	+F.S./2 − 1 LSB
0 0 0...0 0 0	0V

BIPOLAR OPERATION

BINARY INPUT	ANALOG OUTPUT
1 1 1...1 1 1	+F.S. − 1 LSB
1 0 0...0 0 0	0V
0 1 1...1 1 1	− 1 LSB
0 0 0...0 0 0	−F.S.

MICROPROCESSOR INTERFACE CONSIDERATIONS

General

The HS 9378 is easily interfaced to either an 8-bit or 16-bit microprocessor. First, a signal to select (or address) the HS 9378 must be generated. Then the input data must be written (or latched) to the DAC and after settling, the analog output is valid.

The bus interface logic consists of three independently addressable registers in two buffers. The first buffer consists of two 8-bit registers which can be loaded directly from an 8- or 16-bit microprocessor bus. Once the complete 16-bit word has been assembled in the first buffer, it can be loaded into the second buffer for conversion.

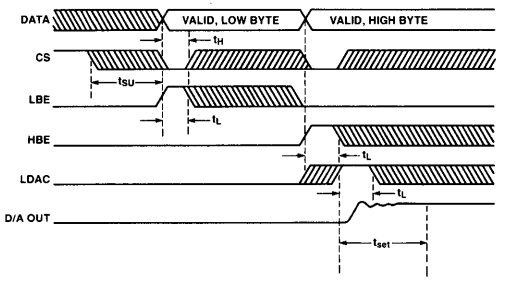
The required selection signal, $\overline{CS}$, is easily derived in most systems. Usually a base address is decoded and this active low signal is used for $\overline{CS}$. The active high signal for the low byte enable (LBE) and high byte enable (HBE) loads the two 8-bit registers into the first buffer while the LDAC signal loads the second buffer for conversion. The double-buffered input eliminates the generation of spurious analog output values.

MEMORY MAPPED INTERFACE TO 8-BIT μP

Figure 1 shows the timing sequence for operating the HS 9378 with an 8-bit μP bus and Figure 2 shows a general interface. Note that the pinout of the HS 9378 allows the user to run only 8 traces directly underneath the hybrid to connect to the two 8-bit input registers in the first buffer.

The HS 9378 is addressed by the chip select ($\overline{CS}$) signal going low for a minimum of 100 nsec. Since t_{SU}, the minimum time required for the input data to be valid before $\overline{CS}$, LBE, or HBE are active, is 0 ns minimum, the $\overline{CS}$ signal can go low simultaneously with data. The low byte enable (LBE) signal going high loads the 8 LSBs into the lower register of the first buffer. After a minimum latch time of 100 nsec, the LBE signal going low latches the data in the lower register. A similar control signal and timing sequence is used to load the 8 MSBs into the upper register of the first buffer (HBE). The load DAC (LDAC) signal going high loads the full 16-bits of data from the first buffer into the second buffer and the D/A for conversion. A minimum latch time of 100 nsec is required for the LDAC signal. The analog output then changes to the new value within the specified settling time. Table 1 is a truth table for the control inputs.

8-BIT BUS INTERFACE



t_{SU}	Setup time required for input data to be valid before $\overline{CS}$, LBE or HBE going active	0 nsec min
t_H	Hold time for $\overline{CS}$ to stay low	100 nsec min
t_L	Latch time for LBE, HBE, and LDAC	100 nsec min
t_{SET}	Settling time from LDAC going active to valid output	
	0.0015% F.S.R., all zeros to all ones	22 μ sec typ
	0.0015% F.S.R., midscale LSB transition	16 μ sec typ

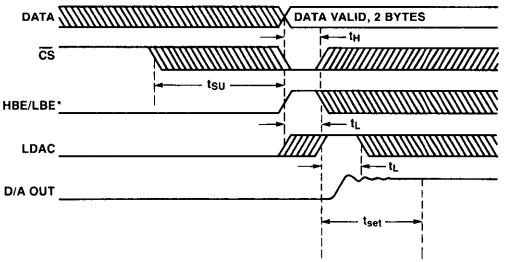
Figure 1. Timing Diagram for Interface to 8-Bit μP Bus

A_7-A_3 ($\overline{CS}$)	A_2 (LDAC)	A_1 (HBE)	A_0 (LBE)	OPERATION
Defined by switches to give low signal to $\overline{CS}$ when 9378 is addressed	0	0	0	All data latched
	0	0	1	Data into low byte of 1st buffer, all others latched
	0	1	0	Data into high byte of 1st buffer, all others latched
	0	1	1	Invalid address
	1	0	0	Data into 2nd buffer (16 bits) and D/A, 1st buffer latched
	1	0	1	Invalid address
	1	1	0	Invalid address
	1	1	1	Data directly to D/A from bus, latches transparent

Table 1. Truth Table — Control Inputs (References Figure 2)

MEMORY MAPPED INTERFACE TO 16-BIT μP

Figure 3 shows the timing sequence for operating the HS 9378 with a 16-bit μP bus and Figure 4 shows a general interface. Table 2 is a truth table for the control inputs. Note that the control inputs are simplified since the HBE and LBE signals can be connected together.



*HBE and LBE are connected together.

Figure 3. Timing Diagram for Interface to 16-Bit μP Bus

A_{15}-A_2 ($\overline{CS}$)	A_1 (LDAC)	A_0 (HBE, LBE)	OPERATION
Defined by switches to give low signal to $\overline{CS}$ when 9378 is addressed	0	0	Data latched
	0	1	Data into 1st buffer, 2nd buffer latched
	1	0	Data into 2nd buffer, 1st buffer latched
	1	1	Data directly to D/A, latches transparent

Table 2. Truth Table — Control Inputs (References Figure 4)

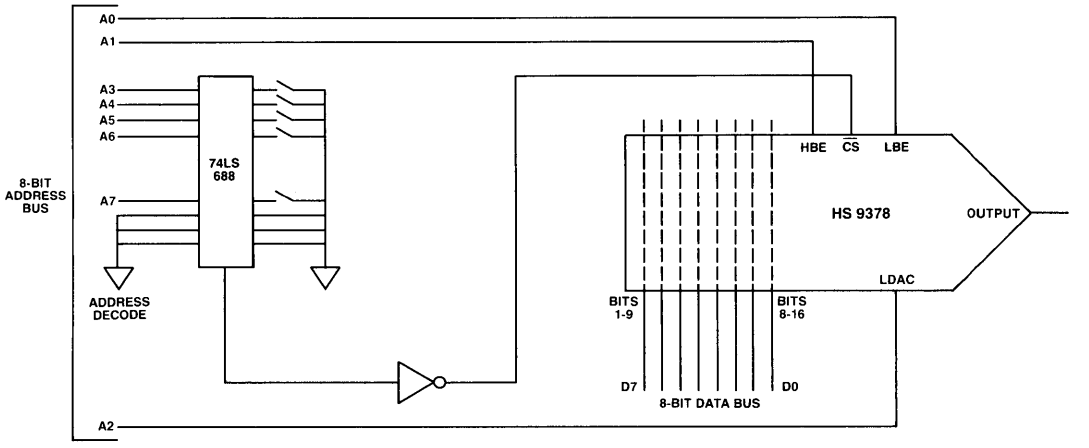


Figure 2. Block Diagram of HS 9378 Interfaced to 8-Bit μP

APPLICATIONS INFORMATION (continued)

MEMORY MAPPED INTERFACE TO 16-BIT μP (continued)

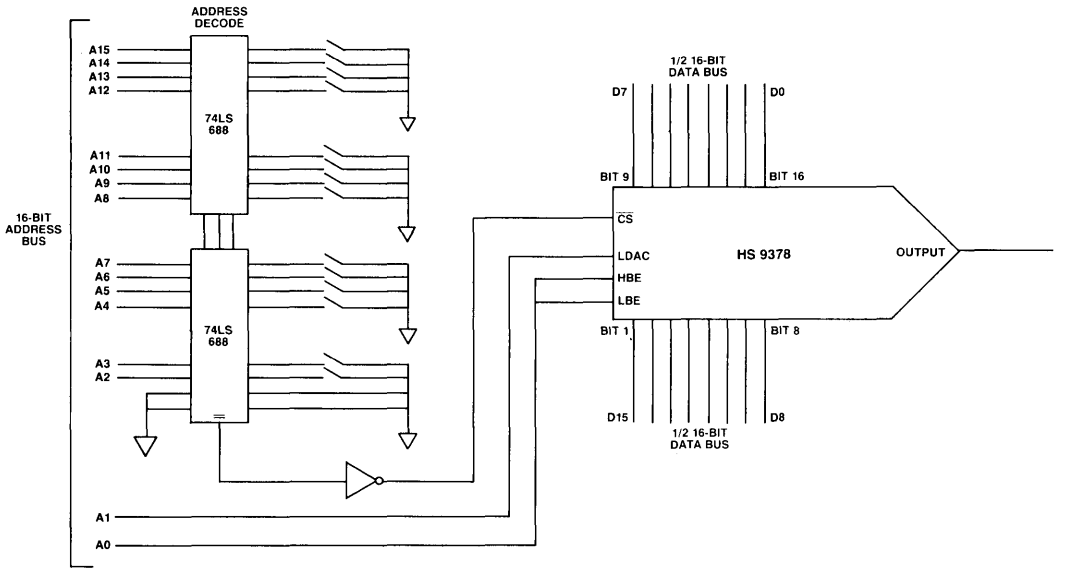


Figure 4. Block Diagram of HS 9378 Interfaced to 16-Bit μP

POWER SUPPLY CONSIDERATIONS

Power supplies used for the HS 9378 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output voltage may result with noisy power sources. It is important to remember that 156 μV is 1 LSB for a 10 volt output.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10 μF tantalum type in parallel with 0.01 μF disc ceramic type.

ADDITIONAL RECOMMENDATIONS

1. For optimum performance, HS 9378 should be allowed sufficient warmup time (5 min.).
2. Due to the small bit weight (156 μV), noise becomes a noticeable factor; therefore, high quality sockets are recommended (if sockets are used) to minimize contact resistance.
3. No digital input should be left floating as the unit will draw excessive current. Unused digital inputs must be tied to a voltage potential of 0V or +5V.
4. If optimum transient and glitch energy performance are required, electrically connect the lid (Case B) to pin 17.
5. If the D/A is driven from a non-buffered or heavily loaded bus, best linearity is obtained by adding 2kΩ pullups to the digital bit inputs.

CONTROL LOGIC

Figure 5 details the control logic function. Note that the LDAC signal is independent of the $\overline{CS}$ signal. All the latches are level controlled as opposed to edge triggered. This allows each of the latches to be operated in a transparent mode by tying the latch control input to a fixed logic "1" level. Since all 3 latches are independent of one another, the sequence of loading the 8 MSBs and the 8 LSBs is reversible.

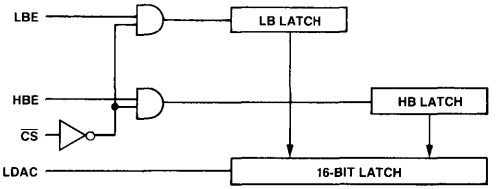


Figure 5. Control Logic Function

LAYOUT CONSIDERATIONS

Due to the small bit weight (156 μV for 1 LSB) special attention must be paid to the layout of the PC-board. To avoid capacitive coupling from digital lines to the hybrid substrate, a ground-plane should be placed directly under the converter package on the component side. This ground-plane can be directly connected to pin 17 of the HS 9378. All digital lines should run on the soldering side of the PC-board.

APPLICATIONS INFORMATION (continued)

The pin assignment of the HS 9378 has been arranged so that the 16 digital inputs can be connected to an 8-bit data bus without crossing of bus lines (see Figure 2). In systems with 16-bit data buses, capacitive coupling of the data bus to the HS 9378 can be further reduced by not routing any of the digital lines under the package (see Figure 4).

In general, analog and digital lines should be separated as far as possible and should not run in parallel. If analog and digital lines must cross, they should be at right angles to minimize coupling capacitance. The ground connection to the converter should be made using a wide, low resistive run to minimize voltage drop. If your system distinguishes between analog and digital ground lines, they must be connected at only one point, preferably directly at the converter package. If the connection cannot be made at the package, only the analog ground should be connected to the HS 9378.

TERMINOLOGY

Major Carry Transition Settling: The total elapsed time between the application of a new input code and the point at which the analog output has settled to within a specified error band. The HS 9378 specifies settling to within 0.0015% FSR. For a major carry transition, the change is when the MSB just turns on or off; i.e., when the digital input goes from a "0" and all "1's" to a "1" and all "0's" or vice versa.

Full Scale Transition Settling: The same as major carry transition settling with the exception that the change is a full scale change. For the HS 9378, the change is $-10V$ to $+10V$, or 20V.

Monotonicity: A monotonic DAC means that the analog output does not decrease as the input is increased or vice versa. The relevant specification is over what temperature range and to what accuracy monotonicity is guaranteed.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below -0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

OUTPUT VOLTAGE RANGE

The HS 9378 can be configured for 3 output ranges: $\pm 10V$, $\pm 5V$ and 0 to 10V. (If unipolar operation is desired, the 20V range is not possible since the output amplifiers saturate at approximately 13V.) Range connections are given in the following chart:

OUTPUT RANGE	PIN 12	PIN 11
$\pm 10V$	Open	Connect to Pin 13
$\pm 5V$	Connect to Pin 14	Connect to Pin 13
0 to 10V	Connect to Pin 14	Connect to Pin 17

LONG TERM DRIFT

Long-term drift of the DAC's transfer function, after initial trim of offset and gain, is composed of several factors which are discussed below.

a. Offset Drift. For maximum performance, the offset should be zeroed after at least one hour of operation. Then the offset drift will be typically 200 μV for the first 1000 hrs; and 100μ V per 1000 hrs thereafter.

b. Reference Voltage Drift. The intrinsic long-term drift of the breakdown voltage of the temperature compensated zener-diode in the reference voltage circuitry will cause a gain error at the output of the DAC. The drift that will occur is typically less than 1mV per year. A correction of this drift error can be made using the gain adjustment circuitry.

c. Output Amplifier Gain Change. Any noticeable gain change will be caused by a drift of the internal feedback resistor relative to the DAC's network impedance. This can contribute 10ppm F.S.R./1000 hrs, which can be corrected using the gain circuitry.

d. Linearity Drift. Due to the unique circuitry used in the DAC network, effects of resistor accuracy drift on linearity are greatly reduced. Typical differential linearity drift is less than 3ppm F.S.R./1000 hrs.

ORDERING INFORMATION

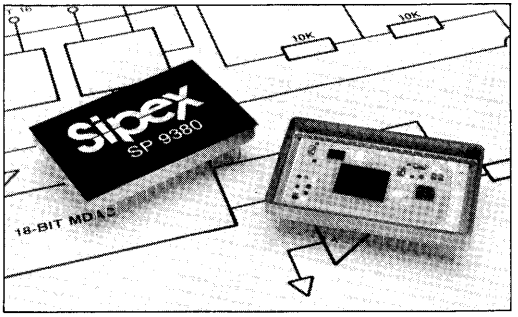
MODEL	MONOTONICITY (over temp.)	TEMPERATURE RANGE	SCREENING
HS 9378C	15 bits	0°C to +70°C	—
HS 9378TB	15 bits	−55°C to +125°C	MIL-STD-883C
HS 9378SB	14 bits	−55°C to +125°C	MIL-STD-883C

NOTE: Contact factory for serial input version or for voltage MDAC version.

Complete Buffered 18-Bit DAC

FEATURES

- Complete 18-Bit DAC Including an Internal Reference and an Output Amplifier
- Input Latches Assist in Microprocessor Interface
- Low Nonlinearity:
  - ±½ LSB 18-Bit Differential
  - ±½ LSB 18-Bit Integral
- 18-Bit Monotonicity
- Low Power: 600 mW Typ
- High Stability Over Time and Temperature



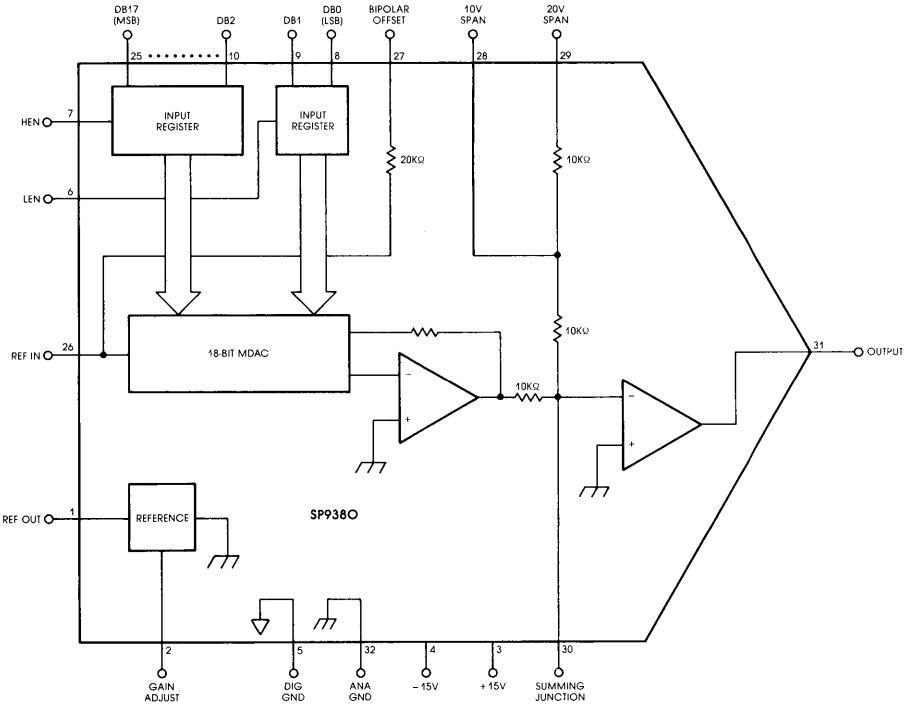
DESCRIPTION

The Sipex SP9380 is a complete voltage output DAC offering 18-bit resolution (1 part in 262,144) and true 18-bit accuracy in a component size hybrid package. The SP9380 comes complete with input latches, an internal reference and a very low noise output amplifier. The analog output ranges are pin programmable for 0 to +5V, 0 to +10V, ±5V and ±10V.

Using decoding techniques and ultrastable resistor technology, the SP9380 exhibits maximum nonlinearities of ±0.5 LSB (differential and integral) and high stability over time and temperature. The power dissipation is 600mW typical.

The device is available for either commercial (0°C to +70°C) or military (−55°C to +125°C) applications in a 32 pin triple DIP.

FUNCTIONAL DIAGRAM



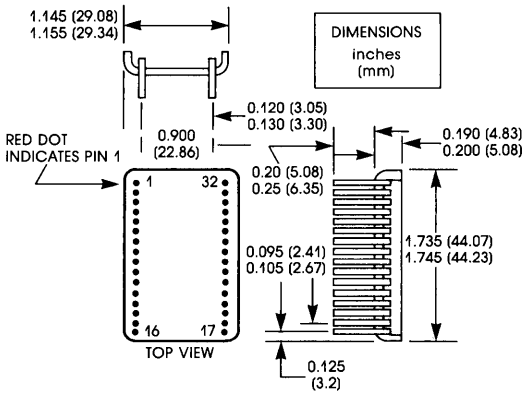
SPECIFICATIONS

(Typical @25°C and rated supplies.)

MODEL	SP938O-18	SP938O-16
RESOLUTION	18-Bits	*
DIGITAL INPUTS		
Unipolar Coding	Binary	*
Bipolar Coding	Offset Binary	*
Logic	TTL CMOS	*
Compatibility[1]		
Input Leakage Current[2]	±1.0μA	*
Data Setup[3]	150 nsec	*
Latch Width	170 nsec	*
Data Hold[4]	100 nsec	*
ACCURACY		
Differential Nonlinearity	±0.0002% FSR typ, ±0.0004% FSR max	±0.0008% FSR typ, ±0.0016% FSR max
Integral Nonlinearity	±0.0002% FSR typ, ±0.0004% FSR max	±0.0010% FSR typ ±0.0016% FSR max
Monotonicity	18-Bits	18-Bits
INITIAL ERRORS		
Gain	±0.01% typ, ±0.10% max	*
Offset		
Unipolar	±0.01% typ, ±0.05% max	*
Bipolar	±0.01% typ, ±0.05% max	*
STABILITY (ppm/°C)		
Differential Nonlinearity	±0.1 typ, 0.4 max	*
Integral Nonlinearity	±0.2 typ, ±0.4 max	*
Gain	±3 typ, ±7 max	*
Offset		
Unipolar	±0.1 typ, ±0.5 max	*
Bipolar	±1 typ, ±4 max	*
STABILITY LONG TERM		
Differential Linearity	16ppm/168 hrs. @125°C	*
	1ppm/1000 hrs. @25°C	*
Gain	15ppm/1000 hrs @25°C	*
Offset	15ppm/1000 hrs. @25°C	*
WARM-UP TIME	10 minutes	*
DYNAMIC PERFORMANCE		
Analog Settling Time (½ LSB)		
10 Volt Step	30μsec	*
20 Volt Step	50μsec	*
LSB Change	8μsec	*
Slew Rate	2V/μsec	*
Major Carry Transition Settling to 0.006% FSR Strobed	10μs	*
REFERENCE		
Voltage	+10V (internal)	*
Drift	5ppm/°C	*
Stability	1mV/year	*
ANALOG OUTPUT		
Voltage	+5V, +10V, ±5V, ±10V	
Noise (Wideband)	0.0004% FSR p-p	
POWER SUPPLY REQUIREMENTS		
+15V DC (±5%)	30mA max	*
−15V DC (±5%)	20mA max	*
Power Dissipation	600mW	*
Supply Rejection	±0.0001%/%	*
TEMPERATURE RANGE		
Operating	−55 to +125°C	*
Storage	−65 to +150°C	*
PACKAGE	32 Pin Metal	

NOTES: 1. Digital input voltage must not exceed supply voltage or go below 0.5V. 2. $V_{IL} \leq 0.4$, $V_{HL} \geq 3.2$.
3. Time that data must be stable before latch control goes to 0. 4. Time that data must be stable after latch control goes to 0.

PACKAGE OUTLINE



PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	REF OUT	32	ANA GND
2	GAIN ADJUST	31	OUTPUT
3	+15V	30	SUMMING JUNCTION
4	−15V	29	20V SPAN
5	DIG GND	28	10V SPAN
6	LEN	27	BIPOLAR OFFSET
7	HEN	26	REF IN
8	DB0 (LSB)	25	DB17 (MSB)
9	DB1	24	DB16
10	DB2	23	DB15
11	DB3	22	DB14
12	DB4	21	DB13
13	DB5	20	DB12
14	DB6	19	DB11
15	DB7	18	DB10
16	DB8	17	DB9

OPERATING INSTRUCTIONS

POWER SUPPLY AND GROUNDING CONSIDERATIONS

Clearly, the management of IR drops, power supply noise, thermal stability and environmental noise become critical issues when designing an 18-bit system. To optimize the absolute accuracy of a high resolution system, the following rules of thumb have to be followed:

1. Selection of low noise operation power supplies.
2. Proper decoupling of the supplies at the DAC using a 10μF ceramic disk capacitor.
3. Usage of the "holy point" grounding technique.
4. "Kelvin-sensed-output" connection of the DAC at the load.

Figure 1 illustrates the use of these rules to hook-up the SP9380.

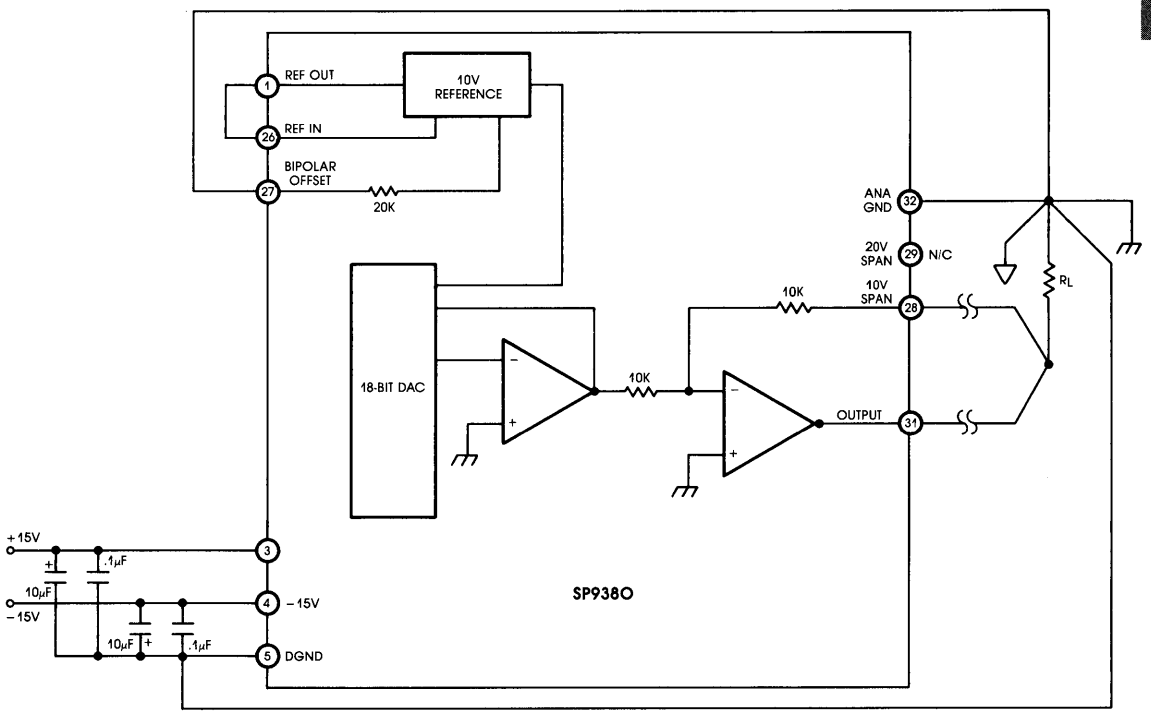


Figure 1. Typical Hook-Up Diagram with "Holy Point" Ground and "Kelvin-Sensed" Load (Unipolar 10V)

The "holy point" grounding technique consists of choosing a ground reference point where ground returns of different systems' components are connecting. Separate ground returns are provided to minimize the current flow in the path from sensitive points to the system "holy" point. For example, supply currents do not flow in the same return path with an analog signal, or logic-gate return currents are not summed into the return from a precision reference.

The Kelvin sense capability of the SP9380 allows driving heavy loads and long lines without the usual accompanying gain errors. By sensing at the load, as described in Figure 1, the load current will pass through the amplifier's output and the ground, but not through the sense lines. The potential gain errors which would be induced by that load current are, therefore, minimized.

REFERENCE

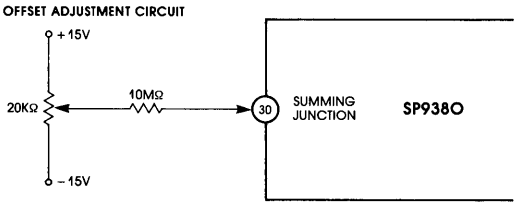
The SP9380 comes with a zener reference circuit showing low drift over time and temperature. By strapping Pin 1 (REF OUT) and Pin 26 (REF IN), the SP9380 will be properly biased from the internal reference. The reference output is used to adjust the total gain of the DAC (see further paragraph). In systems where several components need to track the same reference, an external 10V reference can be supplied through Pin 26, leaving Pin 1 open.

ANALOG OUTPUT RANGES

The SP9380 is pin programmable to provide four different analog voltage outputs. Table 1 gives the connections to realize to obtain them.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Initial offset and gain errors can be adjusted to zero by using external potentiometers as shown in Figure 2.



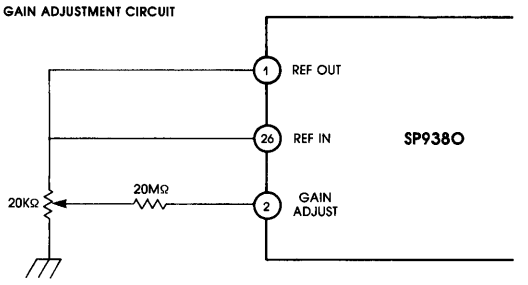


Figure 2. Gain and Offset Adjust Circuits

The potentiometers selected should be good quality Cermet type. Multi-turn potentiometers with 20 turns and 100ppm/°C temperature coefficients are adequate. The 20 the 10M Ohm (20% carbon or better) should be as close to the unit as possible to avoid noise pick-up. If it is not convenient to use such high value resistors, an equivalent "T" network can substitute them as shown in Figure 3.

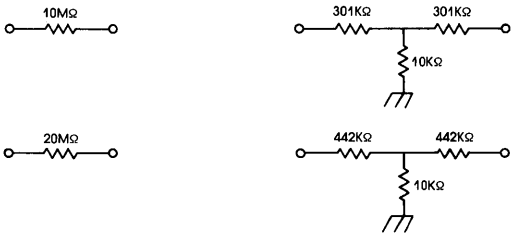


Figure 3. Equivalent Resistances

The procedure for the adjustments is as follows:

UNIPOLAR MODE:

1. Apply a digital input of all "0's".
2. Adjust the offset potentiometer until a 0.000000V output is obtained.
3. Apply a digital input of all "1's".
4. Adjust the gain potentiometer until plus full scale output is obtained (see Table 2 for exact value).

	CONNECT PIN			
OUTPUT RANGE	**27 (BIPOLAR OFFSET) to**	**28 (10V SPAN) to**	**29 20V SPAN to**	**30 (SUMMING JUNCTION) to**
0 to +5V	END	31 (OUTPUT)	30 (SUMMING JUNCTION)	29 20V SPAN
0 to +10V	END	31 (OUTPUT)	N/C	N/C
±5V	30 (SUMMING JUNCTION)	31 (OUTPUT)	N/C	27 (BIPOLAR OFFSET)
±10V	30 (SUMMING JUNCTION)	N/C	31 (OUTPUT)	27 (BIPOLAR OFFSET)

N/C = NOT CONNECTED

Table 1. Output Range Selection

BIPOLAR MODE:

1. Apply a digital input of "1" and all "0's".
2. Adjust the offset potentiometer until a 0.000000V output is obtained.
3. Apply a digital input of all "1's".
4. Adjust the gain potentiometer until plus full scale output is obtained (see Table 2 for exact value).

		Code 000...00	Code 111...11	
Unipolar	+5V	0.000000V	+4.999981V	
	+10V	0.000000V	+9.999962V	
		Code 100...00	**Code 111...11**	**Code 000...00**
Bipolar	±5V	0.000000V	+4.999962V	− 5.000000V
	±10V	0.000000V	+9.999924V	−10.000000V

Table 2. Full-Scale and Offset Calibration Voltages

Refer to Figures 4 and 5 for the relationship of offset and gain adjustments to unipolar and bipolar hooked-up SP9380's.

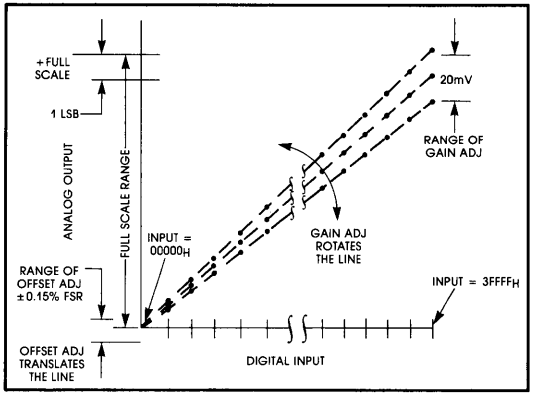


Figure 4. Relationship of Offset and Gain Adjustments in Unipolar Mode

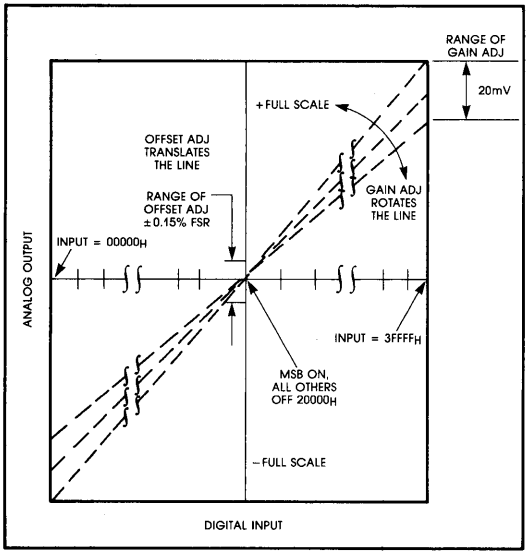
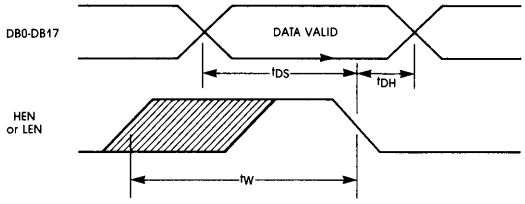


Figure 5. Relationships of Offset and Gain Adjustments in Bipolar Mode

TIMING DIAGRAM

Timing requirements for loading a digital input word in the latches of the SP9380 are shown in Figure 6. The HEN line controls the 16 MSB's while LEN commands the two last LSB's. The latches are transparent when the control lines are HIGH. When they are activated LOW, the data present at the inputs is held in the latch and the corresponding analog voltage is seen at the output.



t_{DS} = DATA SET-UP TIME = 150 ns min
t_{DH} = DATA HOLD TIME = 100 ns min
t_W = LEN or HEN PULSE WIDTH = 170 ns min

Figure 6. SP9380 Timing Diagram

APPLICATIONS

IBM* PC INTERFACE

Figure 7 illustrates a typical IBM personal computer interface which uses three 8-bit external latches and two decoders. The HCT374 latches are connected to the data bus of the PC (D0-D7). The HCT688 defines a base address for the SP9380, while the HCT138 enables each latch including the SP9380's internal latch. This decoding scheme allows the computer to load digital words to the SP9380 when I/O write operations are performed. In the example of Figure 7, the base address is 1C0 hexadecimal. Table 3 lists the address position occupied by each latch.

I/O Address	Selected Latch	Data Bits
Base Address	Low Byte	DB0-DB7
Base Address +1	Mid Byte	DB8-DB15
Base Address +2	High Byte	DB16, DB17
Base Address +3	SP9380 Latch	DB0-DB17

Table 3. IBM Interface Address Locations

*IBM is a trademark of International Business Machine.

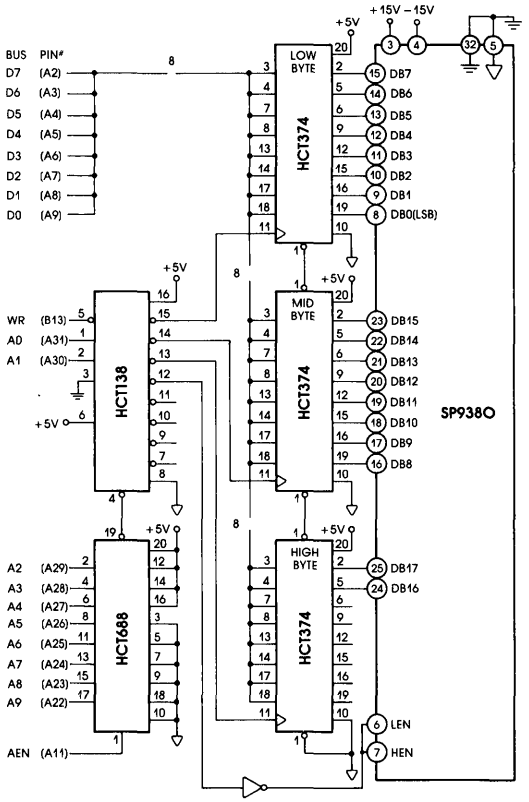


Figure 7. IBM PC Interface

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	SCREENING
SP9380C-18	0°C to 70°C	—
SP9380C-16	0°C to 70°C	—
SP9380B-18	–55°C to +125°C	MIL-STD-883C
SP9380B-16	–55°C to +125°C	MIL-STD-883C

HS9393/9394

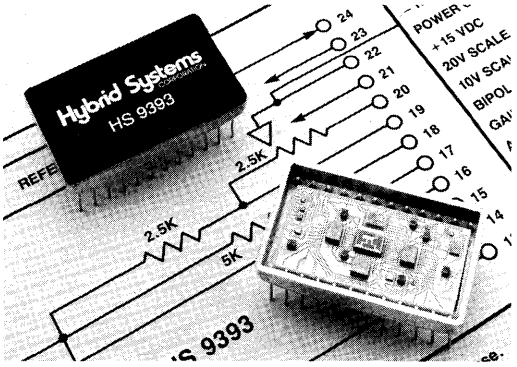
12-BIT ULTRA HIGH SPEED, VOLTAGE or CURRENT OUTPUT D/A CONVERTER

FEATURES

- HS9393 — 50nsec settling time (4mA step to ±½ LSB)
  HS9394 — 1μsec maximum voltage output settling time
- Monotonicity guaranteed over temperature
- Current output (HS9393)

DESCRIPTION

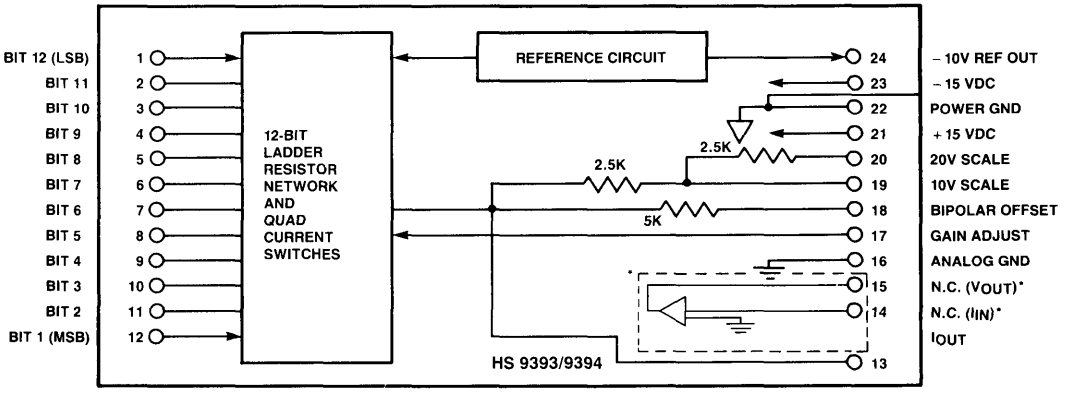
The HS9393 is a very high speed, current output 12-bit DAC and the HS9394 is a high speed, voltage output DAC. The HS9393 can settle a 4mA step to ±0.01% FSR in 50nsec (typ) while the HS9394 can settle a ±FS input change in 1μsec (max). Integral linearity is ±½ LSB max while monotonicity is guaranteed over the operating temperature range. The HS9393/9394 combines a proprietary high speed, dielectrically isolated current switch, a specially designed nichrome resistor network and a buffered reference circuit.



The HS9393/9394 is packaged in a 24-pin ceramic DIP and is offered for commercial (0°C to +70°C) and military (−55°C to +125°C) applications with MIL-STD-883C processing.

7

FUNCTIONAL DIAGRAM



Analog ground and power ground must be externally connected to each other. Power ground is connected to case.

*REFERS TO HS 9394

SPECIFICATIONS

(Typical at +25°C, ±15V unless otherwise noted)

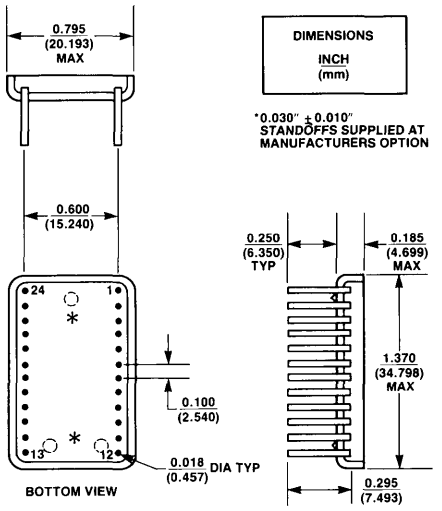
HS 9393				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0		+5.5	volts
Logic "0"	0		+0.8	volts
Logic Loading[1]			1	TTL load
Logic Coding				
Unipolar Range		Straight Binary		
Bipolar Range		Offset Binary		
ANALOG OUTPUT				
Output Range				
Unipolar		0 to 4		mA
Bipolar		±2		mA
Compliance Voltage	±0.6			volts
Output Resistance				
Unipolar		1.5		KΩ
Bipolar		1.2		KΩ
STATIC PERFORMANCE				
Integral Linearity Error				
+25°C		±¼	±½	LSB
0 to +70°C (9393C)		±½		LSB
−55 to +125°C (9393B)		±½		LSB
Differential Linearity Error		±½	±1	LSB
Guaranteed Monotonicity				
9393C	0		+70	°C
9393B	−55		+125	°C
Gain Error[2,3]		±0.1	±1	%
Offset Error[2]				
Unipolar (000...000)		±½	±1	LSB
Bipolar (100...000)		±½	±2	LSB
STABILITY				
Offset Drift				
Unipolar		±0.5	±1	ppm of FSR/°C
Bipolar		±3	±10	ppm of FSR/°C
Gain Drift		±7	±20	ppm/°C
Reference Drift		±5	±15	ppm/°C
Warm-up Time to ±1 LSB		30		seconds
DYNAMIC CHARACTERISTICS				
Settling Time (4 mA step to ±½ LSB)		50	100	nsec
Glitch Energy		0.6		mA-ns
REFERENCE				
Voltage		−10.00		V
Accuracy		±1		%
External Load			2	mA
POWER SUPPLIES				
Accuracy		±2		%
Current Drain				
+15V supply		±30	±35	mA
−15V supply		−13	−18	mA
Power Consumption		650	800	mW
Power Supply Rejection Ratio		±0.001	±0.0024	%/FSR/%V_S
TEMPERATURE RANGE				
Operating				
9393C	0		+70	°C
9393B	−55		+125	°C

HS 9394				
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0		+5.5	volts
Logic "0"	0		+0.8	volts
Logic Loading[1]			1	TTL load
Logic Coding				
Unipolar Range		Straight Binary		
Bipolar Range		Offset Binary		
ANALOG OUTPUT				
Output Range				
Unipolar		0 to −5, 0 to −10		volts
Bipolar		±2.5, ±5, ±10		volts
Compliance Current	±5			mA
Output Resistance		0.05		Ω
STATIC PERFORMANCE				
Integral Linearity Error				
+25°C		±¼	±½	LSB
0 to +70°C (9394C)		±½		LSB
−55 to +125°C (9394B)		±½		LSB
Differential Linearity Error		±½	±1	LSB
Guaranteed Monotonicity				
9394C	0		+70	°C
9394B	−55		+125	°C
Gain Error[2,3]		±0.1	±1	%
Offset Error[2]				
Unipolar (000...000)		±2	±4	LSB
Bipolar (100...000)		±½	±2	LSB
STABILITY				
Offset Drift				
Unipolar		±3	±15	ppm of FSR/°C
Bipolar		±10	±25	ppm of FSR/°C
Gain Drift		±10	±20	ppm/°C
Reference Drift		±5	±15	ppm/°C
Warm-up Time to ±1 LSB		30		seconds
DYNAMIC CHARACTERISTICS				
Settling Time (10V step to ±½ LSB)			1000	nsec
Slew Rate		50		V/μsec
Small Scale Signal Settling (1 LSB Change)		100		nsec
Glitch Energy		2500		mV-ns
REFERENCE				
Voltage		−10.00		V
Accuracy		±1		%
External Load			2	mA
POWER SUPPLIES				
Accuracy		±2		%
Current Drain				
+15V supply		+40	+46	mA
−15V supply		−20	−26	mA
Power Consumption		900	1000	mW
Power Supply Rejection Ratio		±0.001	±0.0024	%/FSR/%V_S
TEMPERATURE RANGE				
Operating				
9394C	0		+70	°C
9394B	−55		+125	°C

NOTES:

1. 1 TTL load is defined as sinking 40μA with a logic "1" and sourcing 1.6 mA with a logic "0" applied.
2. Gain and offset errors can be adjusted to zero using external trim potentiometers.
3. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output current span from the 000...000 to the 111...111 output.

PACKAGE OUTLINE



ABSOLUTE MAXIMUM RATINGS

+ 15 Volts Supply (Pin 21) . . . . . + 18 volts

– 15 Volts Supply (Pin 23) . . . . . – 18 volts

Digital Input Voltage (Pins 1-12) . . . . . 0 to + 7 volts

Output Short Circuit Duration
- Current Output . . . . . continuous to ground
- Reference Output (Pin 24) . . . . . 2 seconds

Storage Temperature (both models) . . . . . – 65°C to + 150°C

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	24	– 10V REF OUT
2	BIT 11	23	– 15V
3	BIT 10	22	POWER GROUND
4	BIT 9	21	+ 15V
5	BIT 8	20	20V SCALE
6	BIT 7	19	10V SCALE
7	BIT 6	18	BIPOLAR OFFSET
8	BIT 5	17	GAIN ADJUST
9	BIT 4	16	ANALOG GROUND
10	BIT 3	15	N.C. (V_{OUT})*
11	BIT 2	14	N.C. (I_{IN})*
12	BIT 1 (MSB)	13	I_{OUT}

NOTES:
*Refers to HS 9394
N.C. — No Internal Connection

APPLICATIONS INFORMATION

POWER SUPPLIES AND GROUNDS

High speed systems require extra care in power distribution to obtain optimum performance. It is recommended that 1 μF tantalum capacitors be added externally between each supply input and analog ground. The power ground (pin 22), which is internally connected to the case, must be externally connected to system analog ground to minimize ground loop errors.

OUTPUT RANGE SELECTION (HS 9393)

OUTPUT		PIN PROGRAMMING
OUTPUT RANGE	OUTPUT PIN	JUMPER PIN 18 TO
0 to + 4 mA	Pin 13	—
± 2 mA	Pin 13	Pin 24

OUTPUT RANGE SELECTION (HS 9394)

OUTPUT		PIN PROGRAMMING			
OUTPUT RANGE	OUTPUT PIN	JUMPER PIN 14 TO	JUMPER PIN 18 TO	JUMPER PIN 19 TO	JUMPER PIN 20 TO
0 to – 5V	Pin 15	Pin 13	Pin 16 (Ground)	Pin 15	Pin 13
0 to – 10V	Pin 15	Pin 13	Pin 16 (Ground)	Pin 15	—
± 2.5V	Pin 15	Pin 13	Pin 24	Pin 15	Pin 13
± 5V	Pin 15	Pin 13	Pin 24	Pin 15	—
± 10V	Pin 15	Pin 13	Pin 24	—	Pin 15

LOGIC INPUTS

Logic inputs are standard TTL/DTL compatible. Unused bits, if any, should be grounded since an "open" bit input line represents a logic "1". However, opening the bit lines should not be used to generate a logic "1" due to the possibilities of noise pickup. Table 1 shows the coding for the HS 9393. Note that 1 LSB equals 0.98μ A. Table 2 shows the coding for the HS 9394.

ANALOG OUTPUT	DIGITAL INPUT	
CURRENT	UNIPOLAR BINARY	BIPOLAR OFFSET BINARY
– FS	N/A	000...000
– ½ FS	N/A	010...000
– 1 LSB	N/A	011...111
0	000...000	100...000
+ 1 LSB	000...001	100...001
+ ½ FS	100...000	110...000
+ FS – 1 LSB	111...111	111...111

Table 1. Input Coding/Output Value for HS 9393

ANALOG OUTPUT	DIGITAL INPUT	
VOLTAGE	UNIPOLAR BINARY	BIPOLAR OFFSET BINARY
+FS	N/A	000...000
+½ FS	N/A	010...000
+1 LSB	N/A	011...111
0	000...000	100...000
−1 LSB	000...001	100...001
−½ FS	100...000	110...000
−FS +1 LSB	111...111	111...111

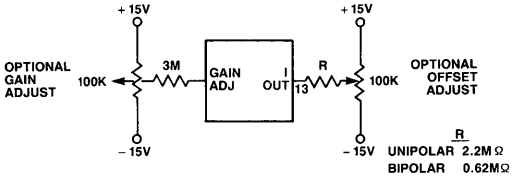
Table 2. Input Coding/Output Value for HS 9394

DYNAMIC CHARACTERISTICS

To optimize settling time and to make the settling time independent of the digital driver characteristics, 2.2 KΩ 1/8 Watt pull-up resistors are recommended at all logic inputs.

OPTIONAL TRIM PROCEDURES

Offset and gain errors are trimmed at the factory to within the limits listed in the specifications table. These initial errors may be trimmed to zero using external potentiometers as shown in Figure 1. Adjustments should be made after sufficient time for warm-up (5 minutes) and, to avoid interaction, offset should be adjusted before gain. The fixed resistors should be located close to the connecting pins to reduce noise and the potentiometers should have a tempco of 100 ppm/°C or less to minimize drift with temperature.



Offset Adjustment: Set the digital input code to 000...000 and adjust the offset trim potentiometer for zero output current (unipolar) or minus full scale output current (bipolar).

Gain Adjustment: Set the digital input code to 111...111 and adjust the gain trim potentiometer for plus full scale minus 1 LSB output current.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts.

ORDERING INFORMATION

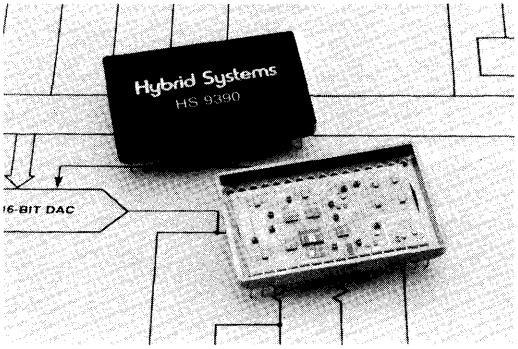
MODEL	TEMPERATURE RANGE	DESCRIPTION
HS 9393C	0°C to +70°C	Current Output DAC
HS 9393B	−55°C to +125°C	Current Output DAC, 883C Screening
HS 9394C	0°C to +70°C	Voltage Output DAC
HS 9394B	−55°C to +125°C	Voltage Output DAC, 883C Screening

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

16-BIT ULTRA HIGH SPEED, LOW GLITCH D/A CONVERTER

FEATURES

- 75nsec settling time (4mA step to ±0.006%)
- Segmented switching architecture reduces glitch area to 140% FSR-nsec



DESCRIPTION

The HS9390 is a very high speed, current output 16-bit DAC that can settle a 4mA step to ±0.006% in 75 nsec. A segmented switching architecture for the top 3 bits reduces switching glitches, making the HS9390 suitable for high resolution video display applications. Proprietary high speed, dielectrically isolated current swtiches provide the HS9390 with its key specifications.

The HS9390 is packaged in a 32-pin metal triple DIP and is offered for commercial (0°C to +70°C) and military (−55°C to +125°C) applications with processing available in full compliance with MIL-STD-883C.

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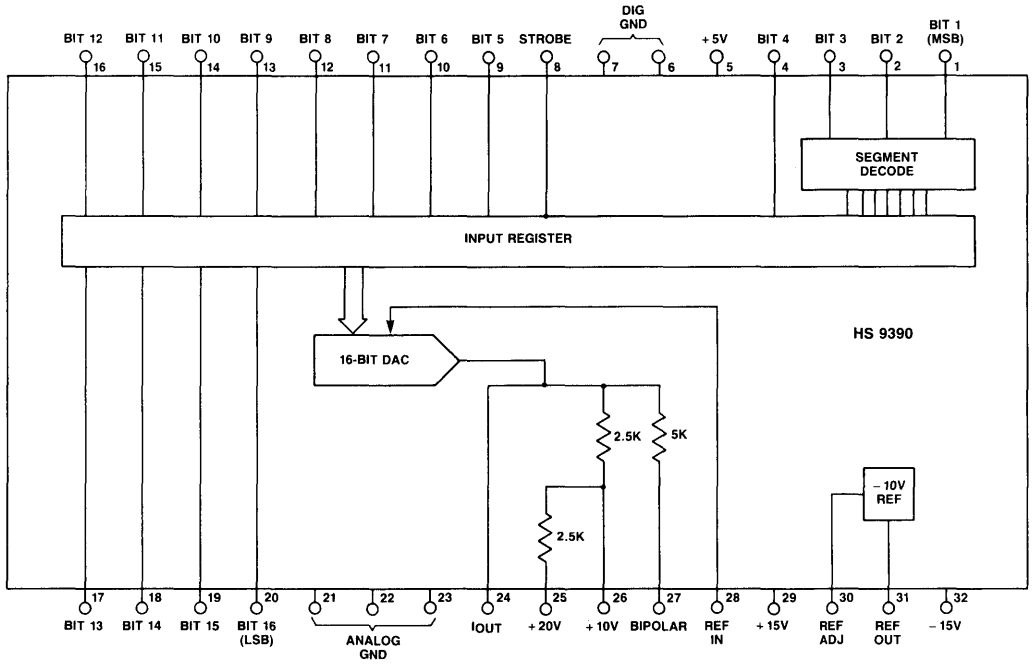
FUNCTIONAL DIAGRAM



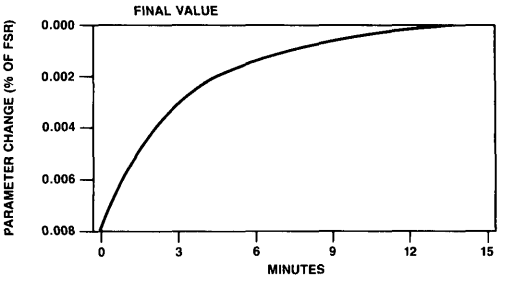
SPECIFICATIONS

(Typical at +25°C, ±15V unless otherwise noted)

	HS 9390			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUTS				
Logic Levels				
Logic "1"	+2.0		+5.5	volts
Logic "0"	0		+0.8	volts
Logic Loading			1	TTL load
Logic Coding				
Unipolar Range	Straight Binary			
Bipolar Range	Offset Binary			
ANALOG OUTPUT				
Output Range				
Unipolar		0 to 4		mA
Bipolar		±2		mA
Compliance Voltage			±1.0	volts
Output Impedance				
Unipolar		1.2K		ohms
Bipolar		1.2K		ohms
STATIC PERFORMANCE				
Integral Linearity				
+25°C		±0.003	±0.006	%FSR
0 to +50°C		±0.006	±0.007	%FSR
Differential Linearity				
+25°C	monotonic to 14 bits			
0 to +50°C	monotonic to 13 bits			
Gain Error[2,3]		±0.1	±1.0	%FSR
Offset Error[2]				
Unipolar (000...000)		±0.05	±0.1	%FSR
Bipolar (100...000)		±0.1	±0.2	%FSR
STABILITY				
Linearity Drift		±1	±2	ppm/°C
Offset Drift				
Unipolar		±1	±2	ppm/°C
Bipolar		±3	±10	ppm/°C
Gain Drift		±5	±10	ppm/°C
Reference Drift		±5	±10	ppm/°C
Warm-up Time	See Figure			
DYNAMIC CHARACTERISTICS				
Settling Time				
to ±0.006% FSR		75	150	nsec
Glitch Energy		0.8		nV-sec
Data Set-up Time (t_1)	70			nsec
Strobe Pulse Width (t_2)	20			nsec
Data Transfer on Positive Edge of Strobe				
REFERENCE				
Voltage	−10.1	−10.0	−9.9	volts
External Current		2		mA
POWER SUPPLIES				
Accuracy		±0.1	±2	%
Current Drain				
+15V Supply		20	25	mA
−15V Supply		15	20	mA
+5V Supply		80	100	mA
Power Consumption		900	1200	mW
Supply Rejection				
+15V Supply		±0.001	±0.002	%/%
−15V Supply		±0.0005	±0.001	%/%
+5V Supply		±0.001	±0.002	%/%
TEMPERATURE RANGE				
Operating				
9390C	0		+70	°C
9390B	−55		+125	°C

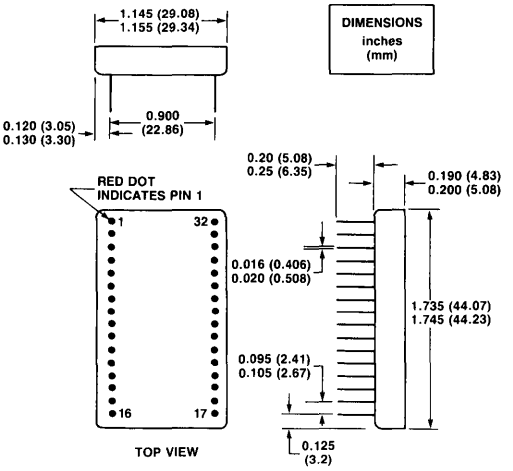
NOTES:

1. Gain and offset errors can be adjusted to zero using external trim potentiometers.
2. Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output current span from the 000...000 to the 111...111 output.



Warm-up Drift of HS 9390

PACKAGE OUTLINE



ABSOLUTE MAXIMUM RATINGS

+15 Volts Supply (Pin 29) ..... +18 volts

−15 Volts Supply (Pin 32) ..... −18 volts

+5 Volts Supply (pin 5) ..... +7 Volts

Digital Input Voltage (Pins 1-4, 9-20) ..... 0 to +7 volts

Output Short Circuit Duration
- Current Output ..... continuous to ground
- Reference Output (Pin 31) ..... 2 seconds

Storage Temperature (both models) ..... −65°C to +150°C

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	32	−15V
2	BIT 2	31	REF OUT
3	BIT 3	30	REF ADJUST
4	BIT 4	29	+15V
5	+5V	28	REF INPUT
6	DIG GND	27	BIPOLAR
7	DIG GND	26	10V SCALE
8	STROBE	25	20V SCALE
9	BIT 5	24	I_{OUT}
10	BIT 6	23	ANALOG GND
11	BIT 7	22	ANALOG GND
12	BIT 8	21	ANALOG GND
13	BIT 9	20	BIT 16
14	BIT 10	19	BIT 15
15	BIT 11	18	BIT 14
16	BIT 12	17	BIT 13

APPLICATIONS INFORMATION

POWER SUPPLIES AND GROUNDS

High speed systems require extra care in power distribution to obtain optimum performance. It is recommended that 1 μF tantalum capacitors be added externally between each supply input and analog ground. The power ground (pin 22) must be externally connected to system analog ground to minimize ground loop errors.

OUTPUT RANGE SELECTION (HS 9390)

OUTPUT		PIN PROGRAMMING
OUTPUT RANGE	OUTPUT PIN	JUMPER PIN 27 TO
0 to +4 mA	Pin 24	Pin 23
±2 mA	Pin 24	Pin 28

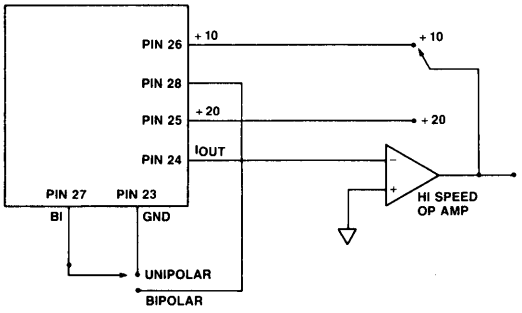
LOGIC INPUTS

Logic inputs are standard TTL/DTL compatible. Unused bits, if any, should be grounded since an "open" bit input line represents a logic "1". However, opening the bit lines should not be used to generate a logic "1" due to the possibilities of noise pickup. Table 1 shows the coding for the HS 9390. Note that 1 LSB equals 0.06 μA.

ANALOG OUTPUT	DIGITAL INPUT	
CURRENT	UNIPOLAR BINARY	BIPOLAR OFFSET BINARY
−FS	N/A	000...000
−½ FS	N/A	010...000
−1 LSB	N/A	011...111
0	000...000	100...000
+1 LSB	000...001	100...001
+½ FS	100...000	110...000
+FS −1 LSB	111...111	111...111

Table 1. Input Coding/Output Value for HS 9390

CONNECTION FOR EXTERNAL AMPLIFIER



OPTIONAL TRIM PROCEDURES

Offset and gain errors are trimmed at the factory to within the limits listed in the specifications table. These initial errors may be trimmed to zero using external potentiometers as shown in Figure 1. Adjustments should be made after sufficient time for warm-up (5 minutes) and, to avoid interaction, offset should be adjusted before gain. The fixed resistors should be located close to the connecting pins to reduce noise and the potentiometers should have a tempco of 100 ppm/°C or less to minimize drift with temperature.

Offset Adjustment: Set the digital input code to 000...000 and adjust the offset trim potentiometer for zero output current (unipolar) or minus full scale output current (bipolar).

Gain Adjustment: Set the digital input code to 111...111 and adjust the gain trim potentiometer for plus full scale minus 1 LSB output current.

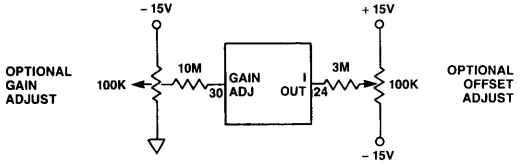
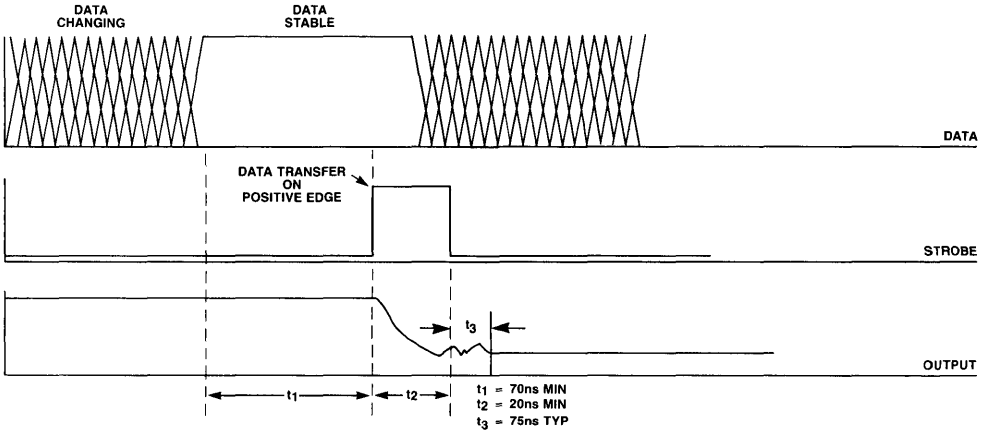


Figure 1.

STROBE TIMING



CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	DESCRIPTION
HS 9390C	0°C to +70°C	Current Output DAC
HS 9390B	−55°C to +125°C	Current Output DAC, 883C Screening

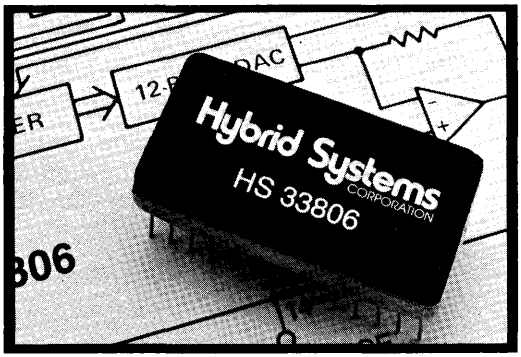
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS33806

MULTIPLYING, VOLTAGE OUTPUT, μP COMPATIBLE 12-BIT DAC

FEATURES

- 2- and 4-quadrant multiplying
- Coding: binary; offset binary
- Linearity: ±0.01%
- Settling time: 2.5μS
- μP compatible
- 28-pin package
- CMOS, TTL compatible
- Double buffered inputs



DESCRIPTION

HS33806 is a μP compatible, complete 12-bit double buffered digital-to-analog converter. To enhance application flexibility, the data input registers have been configured as 3 independent, 4-bit bytes. This enables the user to directly interface to 4, 8, and 12-bit data buses. HS33806 comes complete with interface control logic. The three separate byte enable inputs latch data from the bus into the appropriate primary data latches. The LDAC input transfers data from the primary latches to the DAC register. In addition to these input functions are two chip select inputs and a read/write input allowing direct memory-map configurations. All input controls are static to allow hardwired configurations. The HS33806 is packaged in a hermetically sealed package and is rated −55°C to +125°C. Units are fully screened and processed to MIL-STD-883 requirements.

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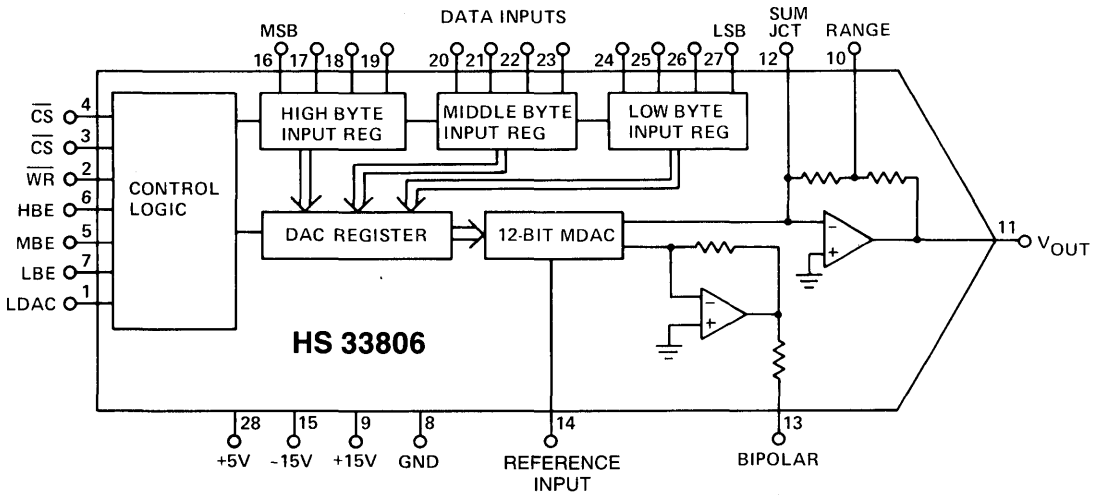
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C unless otherwise noted. Power supply voltages: +15V, −15V, +5V (±5%), Reference −10.0V)

MODEL	HS 33806
DIGITAL INPUT	
Resolution	12 Bit
Unipolar Code	Binary
Bipolar Code	Offset Binary
Logic Compatibility[1,5]	CMOS, TTL
Control Logic Inputs	
I_H @ V_{IH} = 2.4V	20μA
I_{IL} @ V_{IL} = 0.4V	-0.36mA
Data Input Current[5]	±1μA
REFERENCE INPUT	
Max Input Voltage	±25V
Input Impedance	8kΩ ±50%
Reference Feedthrough (V_{REF} = 20 V_{pp})	
@ 1 kHz	<1 mV
@ 10 kHz	2 mV
Bandwidth	
Small Signal	500 kHz
Full Power	200 kHz
ANALOG OUTPUT	
Scale Factor Accuracy	±0.1% F.S.R.
Initial Offset[2]	
Bipolar	10 mV Max
Unipolar	10 mV Max
Voltage Range[2]	
Bipolar	±V_{REF}, ±V_{REF}/2
Unipolar	0 to −V_{REF}, 0 to −V_{REF}/2
STATIC PERFORMANCE	
Integral Linearity[3]	±0.015% F.S.R. Max
Differential Linearity	±0.024% F.S.R. Max
Monotonicity	12 Bits
DYNAMIC PERFORMANCE	
Full Scale Transition Settling Time	5μS (max) 2.5μS (typ)
Full Scale Transition Slew Rate	10V/μS (min)
Delay to Analog Output	
From Bits Input[4]	220nS
From LDAC	220nS
From CS[4] or WE[4]	225nS
STABILITY	
Scale Factor	2 ppm F.S.R.
Integral Linearity	1 ppm F.S.R. Max
Differential Linearity	1 ppm F.S.R. Max
Offset Drift	
Bipolar	100 μV/°C
Unipolar	100 μV/°C
Monotonicity Temperature Range	−55°C to +125°C
±15V POWER SUPPLY	
+15V Supply Current	12mA
-15V Supply Current	7 mA
PSRR	0.005%/%
+5V POWER SUPPLY	
+5V Supply Current	24mA
TEMPERATURE RANGE	
Operating	−55°C to +125°C
Storage	−65°C to +150°C
MECHANICAL	
Case Style	Case B

NOTES

1. Control inputs are TTL and 5V CMOS only; data inputs are fully CMOS and TTL compatible.
2. See APPLICATION NOTES for adjustment procedures.
3. Specified as "Best-Straight Line".
4. Operating the unit with the DAC Register transparent may result in output "glitches" due to logic skewing with the unit.
5. Digital Input voltage must not exceed supply voltage or go below -0.5V. "0" < 0.8V; 2.4V < "1" < V_{DD}.

APPLICATIONS INFORMATION

TRANSFER CHARACTERISTICS

UNIPOLAR OPERATION, PIN 11 OPEN

BINARY INPUT	ANALOG OUTPUT	BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF} \cdot \frac{4095}{4096}$	011...111	$-V_{REF} \cdot \frac{2047}{4096}$
100...001	$-V_{REF} \cdot \frac{2049}{4096}$	000...001	$-V_{REF} \cdot \frac{1}{4096}$
100...000	$-V_{REF} \cdot \frac{2048}{4096}$	000...000	0

Formula: $V_{OUT} = -V_{REF} \cdot \frac{N}{4096}$ where N represents the code applied to the DAC

UNIPOLAR OPERATION, PIN 11 CONNECTED TO PIN 10

BINARY INPUT	ANALOG OUTPUT	BINARY INPUT	ANALOG OUTPUT
111...111	$-\frac{1}{2} V_{REF} \cdot \frac{4095}{4096}$	011...111	$-\frac{1}{2} V_{REF} \cdot \frac{2047}{4096}$
100...001	$-\frac{1}{2} V_{REF} \cdot \frac{2049}{4096}$	000...001	$-\frac{1}{2} V_{REF} \cdot \frac{1}{4096}$
100...000	$-\frac{1}{2} V_{REF}$	000...000	0

Formula: $V_{OUT} = -\frac{1}{2} V_{REF} \cdot \frac{N}{4096}$ where N represents the code applied to the DAC

BIPOLAR OPERATION, PIN 11 OPEN

OFFSET BINARY INPUT	ANALOG OUTPUT	OFFSET BINARY INPUT	ANALOG OUTPUT
111...111	$-V_{REF} \cdot \frac{2047}{2048}$	011...111	$+V_{REF} \cdot \frac{1}{2048}$
100...001	$-V_{REF} \cdot \frac{1}{2048}$	000...001	$+V_{REF} \cdot \frac{2047}{2048}$
100...000	0	000...000	$+V_{REF}$

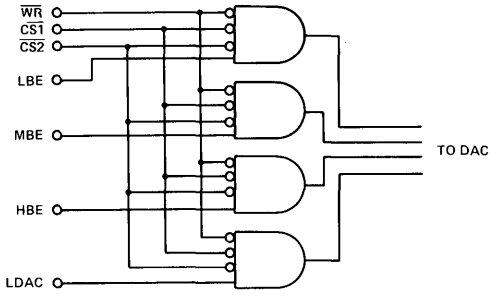
Formula: $V_{OUT} = -V_{REF} \cdot \frac{(N-2048)}{2048}$ where N represents the code applied to the DAC

BIPOLAR OPERATION, PIN 11 CONNECTED TO PIN 10

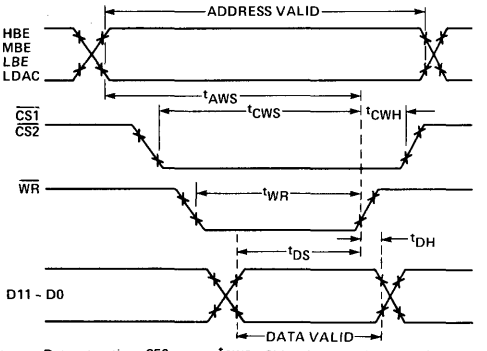
OFFSET BINARY INPUT	ANALOG OUTPUT	OFFSET BINARY INPUT	ANALOG OUTPUT
111...111	$-\frac{1}{2} V_{REF} \cdot \frac{2047}{2048}$	011...111	$+\frac{1}{2} V_{REF} \cdot \frac{1}{2048}$
100...001	$-\frac{1}{2} V_{REF} \cdot \frac{1}{2048}$	000...001	$+\frac{1}{2} V_{REF} \cdot \frac{2047}{2048}$
100...000	0	000...000	$+\frac{1}{2} V_{REF}$

Formula: $V_{OUT} = -\frac{1}{2} V_{REF} \cdot \frac{(N-2048)}{2048}$ where N represents the code applied to the DAC

CONTROL LOGIC FUNCTIONAL DIAGRAM



TIMING DIAGRAM



t_{DS} : Data setup time, 250 nsec
t_{DH} : Data hold time, 20 nsec
t_{WR} : Write pulse width, 300 nsec
t_{CWS} : Chip select to write setup time, 300 nsec
t_{CWH} : Chip select to write hold time, 0 nsec
t_{AWS} : Address to write setup time, 250 nsec

TRUTH TABLE

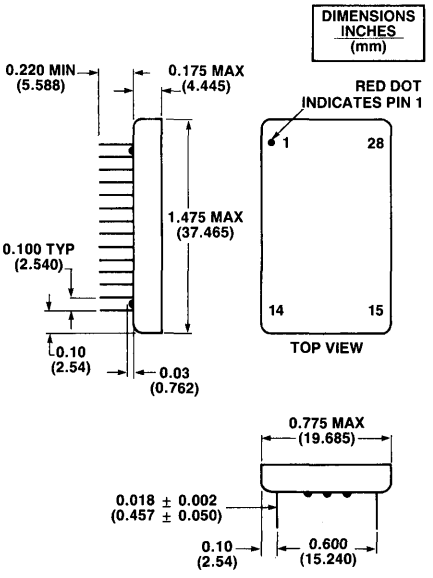
HS 9338 CONTROL INPUTS							HS 9338 OPERATION
$\overline{WR}$	$\overline{CS1}$	$\overline{CS2}$	LBE	MBE	HBE	LDAC	
1 X X	X 1 X	X X 1	X	X	X	X	Device not selected Output reflects previously loaded data
0	0	0	1	0	0	0	Write data into low byte data register
0	0	0	0	1	0	0	Write data into middle byte data register
0	0	0	0	0	1	0	Write data into high byte data register
0	0	0	0	0	0	1	Load DAC register with data in low byte middle byte and high byte data registers
0	0	0	1	1	1	0	Write data simultaneous into all data registers
0	0	0	1	1	1	1	Write data directly into DAC register

PIN DIAGRAM

PIN	FUNCTION
1	LDAC, LOADS DAC REGISTER AND CHANGES OUTPUT
2	$\overline{WR}$, WRITE INPUT, ACTIVATES ALL CONTROLS
3	$\overline{CS2}$, CHIP SELECT INPUT 2
4	$\overline{CS1}$, CHIP SELECT INPUT 1
5	MBE, MIDDLE BYTE ENABLE, D4 TO D7
6	HBE, HIGH BYTE ENABLE, D8 TO D11
7	LBE, LOW BYTE ENABLE, D0 TO D3
8	GND, GROUND, ANALOG AND DIGITAL GROUND CONNECTED INTERNALLY
9	V_{CC}, +15V SUPPLY
10	OUTPUT RANGE
11	V_{OUT}, DAC VOLTAGE OUTPUT
12	SUMJCT, SUMMING JUNCTION OF OUTPUT OPAMP
13	BIPOLAR, CONNECTED TO SUMJCT FOR BIPOLAR OUTPUT RANGE
14	REFERENCE INPUT
15	V_{EE}, -15V SUPPLY
16	D11, DATA INPUT, WEIGHT 2^{-1}, MSB
17	D10, DATA INPUT, WEIGHT 2^{-2}
18	D9, DATA INPUT, WEIGHT 2^{-3}
19	D8, DATA INPUT, WEIGHT 2^{-4}
20	D7, DATA INPUT, WEIGHT 2^{-5}
21	D6, DATA INPUT, WEIGHT 2^{-6}
22	D5, DATA INPUT, WEIGHT 2^{-7}
23	D4, DATA INPUT, WEIGHT 2^{-8}
24	D3, DATA INPUT, WEIGHT 2^{-9}
25	D2, DATA INPUT, WEIGHT 2^{-10}
26	D1, DATA INPUT, WEIGHT 2^{-11}
27	D0, DATA INPUT, WEIGHT 2^{-12}, LSB
28	V_{DD}, +5V SUPPLY, CONTROL LOGIC

PACKAGE OUTLINE

CASE B

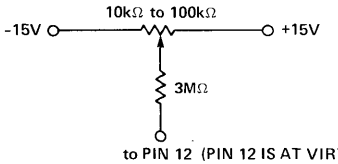


Ceramic or metal package at manufacturer's option.

OUTPUT CONNECTIONS

RANGE	OUTPUT	CONNECT PIN 12	CONNECT PIN 10	CONNECT PIN 13
0 to $-V_{REF}$	PIN 11	OPEN	OPEN	OPEN
0 to $-V_{REF}/2$	PIN 11	OPEN	PIN 11	OPEN
$+V_{REF}$ to $-V_{REF}$	PIN 11	PIN 13	OPEN	PIN 12
$+V_{REF}/2$ to $+V_{REF}/2$	PIN 11	PIN 13	PIN 11	PIN 12

OUTPUT OFFSET ADJUST (OPTIONAL)



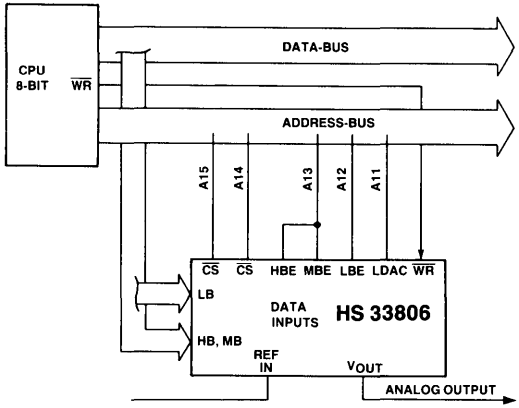
to PIN 12 (PIN 12 IS AT VIRTUAL GROUND)

RANGE: ±25 mV typ
Adjust for V_{out} = 0.000 Volt at input code 00 . . . 0 for unipolar operation or at input code 10 . . . 0 for bipolar operation.

SCALE FACTOR ADJUST: Scale factor is factory trimmed to 0.1% typ. Adjust external reference voltage if initial accuracy is not sufficient.

APPLICATIONS INFORMATION

INTERFACING THE HS 33806 TO AN 8-BIT PROCESSOR USING NO EXTERNAL COMPONENTS

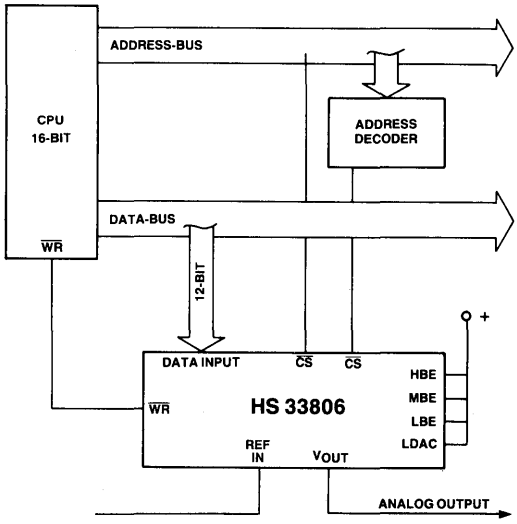


This mode of operation requires 13k bytes of unused addresses. No additional address decoder is necessary. The two chip-select inputs together with the byte-enable and load-DAC inputs are used to control all functions of the DAC. Through selecting the address-lines the user can vary the addresses used to control the DAC. In the above figure the control signals have the following address-configurations (hex):

HBE, MBE	2000
LBE	1000
LDAC	0800

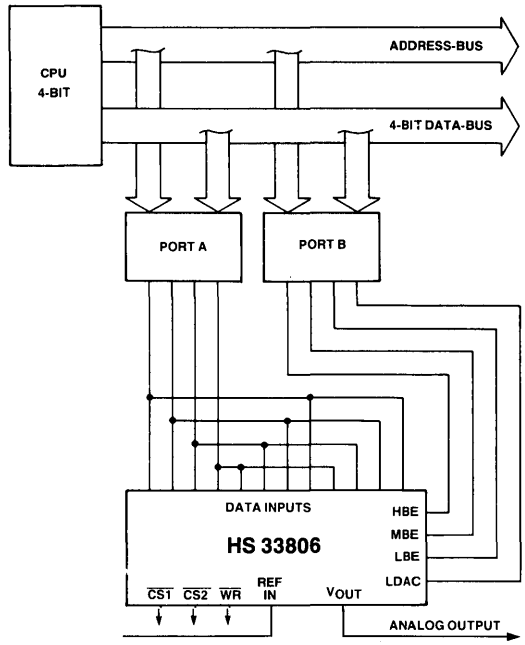
The LDAC input shold not be tied together to the LBE input to ensure correct data transfer between the DAC registers.

INTERFACING THE HS 33806 TO A 16-BIT MICROPROCESSOR



Interfacing the HS 33806 to a 16-Bit microprocessor is quite easy, because no multiplexing of the data inputs is necessary. An address decoder and the second chip-select input is used to select the DAC.

INTERFACING THE HS 33806 to a 4-BIT MICROPROCESSOR USING 4-BIT I/O-PORTS



This figure shows how to operate the HS 33806 with two 4-Bit ports. The chip-selects are tied to ground allowing continuous operation; they can be used for operating more DAC's at the same port. In the first step data should appear at the port A outputs; in the second step the control flags should appear on port B.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 33806	μP MDAC, Voltage Output, MIL-STD-883 Screening

Specifications subject to change without notice.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the supply voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for techincal assistance.

FLASH A/D SUBSYSTEMS

MODEL	RESOLUTION	SAMPLING RATE	BUFFER AMPLIFIER	REFERENCE	POWER DISSIPATION	PACKAGE	PAGE
HS1068	8 bit	20 MHz	Yes	Yes	1.75W	24-Pin DD	365
SP1070	8 bit	25 MHz	Yes	Yes	1W	28-Pin DD	377
SP1072	8 bit	20 MHz	Yes	Yes	3.0W	42-Pin	388
SP1078	8 bit	50 MHz	Yes	Yes	0.6W	24-Pin DD	399

Shaded area indicates new product since publication of 1988 Catalog

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS1068

FLASH PLUS 8-BIT 20 MSPS A/D CONVERTER

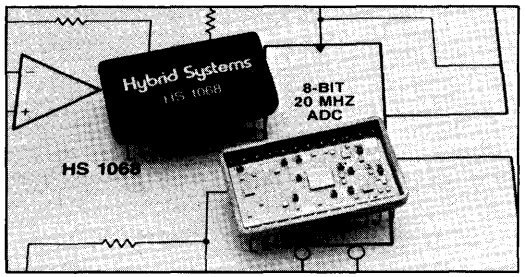
FEATURES

- Complete analog front-end and ADC in a single package
- 20 MHz sampling rate
- Pin strappable unipolar or bipolar input ranges
- Offset and gain adjust pins
- Three-state output

DESCRIPTION

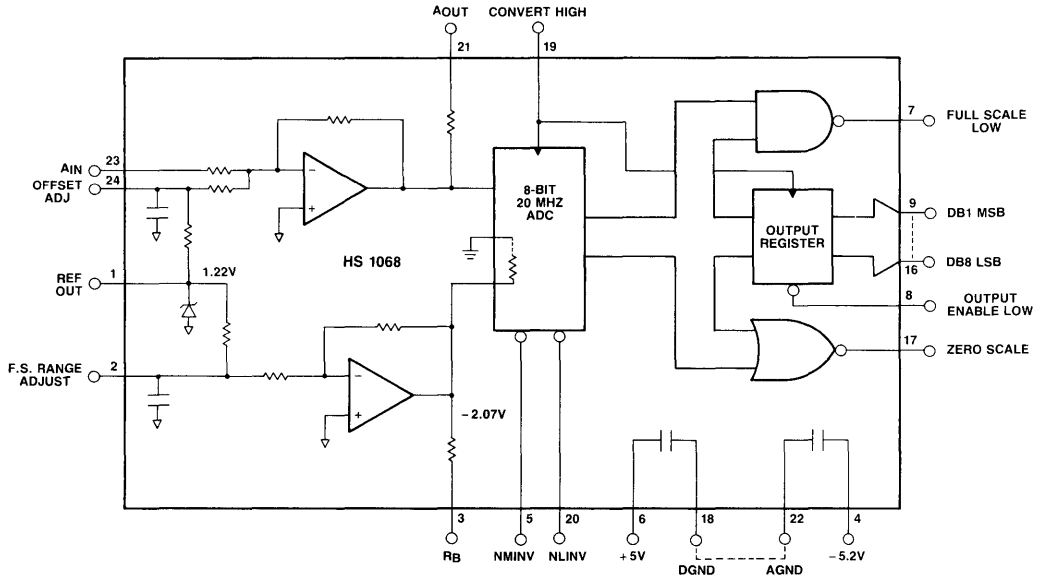
The HS1068 is a complete FLASH ANALOG to DIGITAL CONVERTER that combines all circuitry required to convert high speed analog signals into 8-bit digital data at a rate of 20 mega samples per second. The HS1068 is completely self contained providing an 8-bit, 20 MHz, flash A/D; a wideband analog input amplifier; precision voltage reference and three-state outputs in a single 24-pin package.

Combining all analog support circuitry with the A/D converter offers significant savings of board space; along with component, assembly and design costs.



Designed to meet demanding military applications, the HS1068 is housed in a hermetic 24-pin DIP and operates with guaranteed performance over the full −55°C to +125°C case operating temperature range. Processing in compliance with MIL-STD-883C is available.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage	V_{CC}	7.0	V
	V_{EE}	−7.0	V
Digital Input Voltage	$V_{IN}(D)$	5.5	V
Analog Input Voltage	$V_{IN}(A)$	±5.5	V
Reference Voltage Span	—	2.2	V
Applied Output Voltage	—	5.5	V
Junction Temperature	T_J	150	°C
Operating Case Temperature	T_C	140	°C
Storage Temperature	T_{STG}	−65 to +150	°C

*Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEMPERATURE RANGE						UNITS
		0°C to +70°C			−55°C to +125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Digital Supply Voltage	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
Analog Supply Voltage	V_{EE}	−4.9	−5.2	−5.5	−4.9	−5.2	−5.5	V
Analog Ground	AGND	−0.1	0	+0.1	−0.1	0	+0.1	V
Analog Input, Range ADJ and OFFSET ADJ Open	$V_{IN}(A)$	−0.5		+0.5	±0.5		+0.5	V
Digital Input Voltage, HIGH	$V_{IN}(D)$	2.0			2.0			V
Digital Input Voltage, LOW				0.8			0.8	V
Applied Output Voltage	V_o			V_{CC}			V_{CC}	V
CONV Pulse Width, LOW	t_{PWL}	18			18			nS
CONV Pulse Width, HIGH	t_{PWH}	22			22			nS
Clock Frequency, Max	f_{CLK}	20			20			MHz
Operating Ambient Temperature	T_A	0		70				°C
Operating Case Temperature	T_C				−55		+125	°C

PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution	N				8.0			8.0	Bits
Integral Linearity Error	E_{LI}	DC, Best Straight Line					±0.35		LSB
Differential Linearity Error	E_{DI}	DC					±0.25		LSB
Signal-to-Noise Ratio[1] RMS Signal/RMS Noise + Distortion	SNR	1.123 MHz Input		47			47		dB
		2.234 MHz Input		46			46		dB
		4.456 MHz Input		43			43		dB
Differential Phase	DP	F_S = 4 x NTSC Carrier		1			1		Degree
Differential Gain	DC	F_S = 4 x NTSC Carrier		2			2		%
Aperture Error	E_{AP}			±60			±60		pS
Code Size	CS		25		175	25		175	%
Full Power Bandwidth	BW	No Spurious Code	7	13		5	13		MHz
Input Amplifier Bandwidth	ABW	Freq −3 dB		20			20		MHz
Settling Time (to 0.4%)	t_S	Full Scale Transition		45			45		nS
Amplifier Overshoot	O_S			1			1		%
Overload Recovery	t_{REC}	±100 mV Overdrive		5			5		nS
Input Amplifier Noise		10 MHz Bandwidth[2]		125			125		μVRMS
Range AMP Bandwidth			100			100			kHz
Range AMP Settling		One Volt Step at R_{BOT}		14	50		14	50	μSec

SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Conversion Rate	F_S	V_{CC}, V_{EE} = MIN	20			20			MHz
Sampling Time Offset	t_{STO}	V_{CC}, V_{EE} = MIN	0	10	10	0	10	10	nS
Digital Output Delay	t_D	V_{CC} = MIN	15		28	15		28	nS
Digital Output Enable	t_{PZL}	V_{CC} = MIN		20			20		nS
Digital Output Disable	t_{PHZ}	V_{CC} = MIN		15			15		nS
Full Scale Flag	t_{CFSL}	V_{CC} = MIN		25			25		nS
Zero Scale Flag	t_{CZSH}	V_{CC} = MIN		29			29		nS
CONV Pulse Width, LOW	t_{PWL}	V_{CC} = MIN	18			18			nS
CONV Pulse Width, HIGH	t_{PWH}	V_{CC} = MIN	22			22			nS

INPUTS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Current, Logic LOW	I_{IL}	NMINV, NLINV			−0.6			−0.6	mA
		OE			−0.4			−0.4	mA
		CONV			−0.8			−0.8	mA
Input Current, Logic HIGH	I_{IH}	NMINV, NLINV			50			50	μA
		OE			20			20	μA
		CONV			70			70	μA
Input Voltage, Logic LOW	V_{IL}				0.8			0.8	V
Input Voltage, Logic HIGH	V_{IH}		2.0			2.0			V
Analog Input Resistance	R_{IN}			1K	1.05K		1K	1.05K	Ω
Analog Input Capacitance	C_{IN}			3			3		pF
Input Offset Current	I_B	$I_B = V_{OS} \div$ 1K Ohm			±4			±4	μA
Gain Error	E_G			±0.4			±0.4		%
Bipolar Offset Error	V_{OS}	Offset Open		±1			±1		LSB
Unipolar Offset Error	V_{OS}	Offset ADJ = GND		±1			±1		LSB
Bipolar Offset Error Tempco	T_{CB}	LSB's/°C Case temp rise		+0.05			+0.05		LSB/°C
Unipolar Offset Error Tempco	T_{CU}	LSB's/°C Case temp rise		+0.05			+0.05		LSB/°C

DIGITAL OUTPUTS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Leakage Current, Logic LOW	I_{LOL}				−20			−20	μA
Output Leakage Current, Logic HIGH	I_{LOH}				20			20	μA
Output Voltage, Logic LOW	V_{OL}	I_{OL} = 12 mA[3]		0.25	0.4		0.25	0.4	V
Output Voltage, Logic HIGH	V_{OH}	I_{OH} = −1 mA[3]	2.4	3.4		2.4	3.4		V
Short Circuit Output Current	I_{OS}	V_{CC} = MAX, Output HIGH	−30		−130	−30		−130	mA
Output Capacitance	C_{OUT}								

REFERENCE

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Reference Voltage	V_{REF}	V_{REF} OUT		1.224		1.19	1.224	1.26	V
Reference Current, Sourced	I_{REF}	600Ω, V_{REF} to GND			2.0			2.0	mA
R_{BOT} Adjustment Range	R_{ADJ}	Recommended Range[4]		±0.2			±0.2		V

8

POWER SUPPLIES

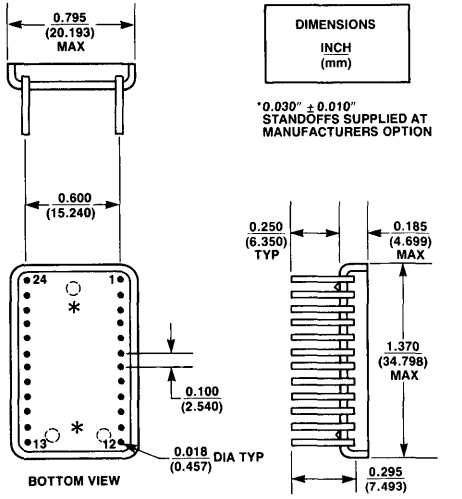
PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Digital Supply Current	I_{CC}	V_{CC} = MAX, Static[5]		101			110		mA
Digital Supply Current	I_{CC}	V_{CC} = MAX, Dynamic[6]		117			125		mA
Analog Supply Current	I_{EE}	V_{EE} = MAX, Static[5]		207			207		mA
Power Dissipation	P_D	V_{CC} = MAX, V_{EE} = MAX Static[5]		1.67			1.75		W
Power Dissipation	P_D	V_{CC} = MAX, V_{EE} = MAX Dynamic[6]		1.75			1.826		W

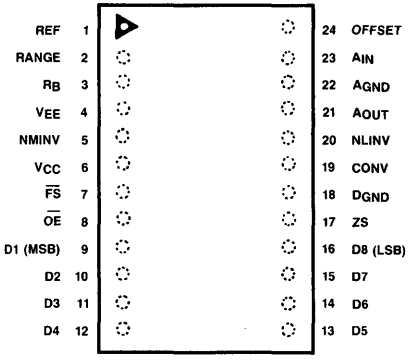
NOTES:
1. SNR = Signal/Noise + Distortion, f_{SAMPLE} = 20 MHz.
2. Referred to input (AV = −2).
3. To minimize power dissipation within the HS 1068, it is better to load the device with a minimal (1LSTTL) load.
4. Operation is possible down to R_{BOT} = −1.1V with reduced dynamic performance specifications.
5. DC input, Output Codes = All low, 1 LSTTL load.
6. 1.1 MHz FS Input, 1 LSTTL load.
7. Specifications subject to change without notice.

PIN ASSIGNMENTS

PIN	SYMBOL	FUNCTION
1	REF	+1.22V Reference Output
2	RANGE	Gain adjust Input, Adjusts −2.0V REF Nominal @Flash
3	R_B	Test Point, −2.0V Nominal @Flash
4	V_{EE}	Negative Supply Voltage, −5.2V
5	NMINV	Not Most Significant Bit Invert
6	V_{CC}	Positive Supply Voltage, +5.0V
7	FS	Full Scale Low, Overflow Detector
8	OE	Output Enable, "High" Tristates Output Data Line
9	D1(MSB)	Data Bit 1
10	D2	Data Bit 2
11	D3	Data Bit 3
12	D4	Data Bit 4
13	D5	Data Bit 5
14	D6	Data Bit 6
15	D7	Data Bit 7
16	D8(LSB)	Data Bit 8
17	ZS	Zero Scale, Underflow Detector
18	DGND	Digital Ground
19	CONV	Convert
20	NLINV	Not Least Significant Bits Invert
21	A_{OUT}	Test Point (Amplifier Output, Flash Input)
22	AGND	Analog Ground
23	A_{IN}	Analog Signal Input
24	OFFSET	Offset Adjust

PACKAGE OUTLINE





APPLICATIONS INFORMATION

THEORY OF OPERATION

The HS 1068 consists of four circuit blocks: the input buffer amplifier, voltage reference, flash converter and digital output logic. Analog and digital grounds are separated to provide flexibility in system grounding and decoupling.

The input amplifier has been designed to be compatible with baseband video signals. The input range is 1 Volt p-p, with pin strap selectable offsets to accommodate 0 to 1 Volt unipolar or ±0.5 Volt bipolar ranges. Typical sources can directly drive the 1 kOhm input impedance, or external resistors to ground can be used to terminate 75 or 50 Ohm cabling. The gain is set to −2 to provide 0 to −2 Volts to the flash converter. A resistor isolated (470 Ohm) analog output test point is available for debugging or for use in application circuits. Settling time is optimized at the factory by an internal variable capacitor.

An internal +1.22 Volt bandgap voltage reference is used to derive a −2.07 Volt nominal reference which drives the flash resistor ladder. The +1.22 Volt reference is capable of sourcing up to 2 mA to drive external application circuits. A resistor isolated (470 Ohms) negative reference output (Rbot) is also available for use in application circuits. These two outputs can be used with external trimpots to obtain calibration of system offset and gain with good power supply rejection. In this case the trimpot ends would go to the two references and the wiper brought through a resistor to the offset or range adjust pins. The HS 1068 is factory trimmed for offset and gain after 15 minute warmup under still room temperature air conditions.

The gain of the converter is set by trimming the reference voltage at the bottom of the flash resistor ladder. This is equivalent to trimming the full scale range at the flash. A maximum adjustment range of ±0.2 Volts is recommended which corresponds to a ±10% gain change. The unit will operate under reduced dynamic performance specifications with the reference as low as 1.5V, corresponding to a gain increase of 33%. Gain decreases can easily be obtained by using a resistive divider at the analog input pin (see Analog Input section).

The A/D is an 8-bit fully parallel flash converter capable of digitizing at rates above 20 MSPS. A single convert (CONV) signal controls the conversion operation. The flash itself consists of 255 sampling comparators, encoding logic and a latched output register. On the rising edge of the CONV signal, the comparators are latched and on the falling edge, the 255 to 8 encoding is performed. The 8 bit value is transferred to a flash-internal data register on the next rising edge. At the third rising edge the data is latched into the output register. The zero scale and full scale flags will be valid before this third rising edge, to allow over and underflow conditions to be detected simultaneously with the suspect data. This register also improves output fanout capability while providing a high-impedance disable function at the outputs. Data is latched into the output register regardless of whether the output is enabled or disabled.

POWER SUPPLIES

The HS 1068 requires two power supply voltages: V_{CC} at +5.0 Volts and V_{EE} at −5.2 Volts nominal. The return path for I_{EE} is through A_{GND}. The return path for most of I_{CC} is D_{GND}. A small amount of I_{CC} is internally separately routed from the V_{CC} pin to the analog operational amplifiers. A_{GND} and D_{GND} are not internally connected. In normal operation they would be tied together at one point underneath the converter. In systems with unusually noisy digital grounds, some resistive isolation between A_{GND} and D_{GND} may be necessary. In this case a small (0.1 μF) decoupling capacitor may be necessary from V_{CC} to A_{GND} to keep the V_{CC} noise from the op-amps. The voltage differential between A_{GND} and D_{GND} should be less than ±0.5V. An alternate method of isolation would involve keeping the A_{GND} and D_{GND} tied together under the converter and using small resistors in series with ferrite beads to isolate the converter's D_{GND} from noise-generating bus drivers. These resistors cannot be too large as they will degrade the noise margin at the non-isolated TTL inputs.

NAME	FUNCTION	VALUE	PIN
V_{CC}	Positive Power Supply	+5.0V	6
V_{EE}	Negative Power Supply	−5.2V	4
A_{GND}	Analog Ground	0.0V	22
D_{GND}	Digital Ground	0.0V	18

ANALOG INPUT

The HS 1068 has a nominal input impedance of 1K Ohm and an input voltage range of 1 Volt p-p. The HS 1068 can accept either unipolar 0 to 1V or bipolar ±0.5V. Both the input impedance and input voltage range may be changed for operation in other modes. The values of two external input resistors can determine the input impedance and voltage range of the device. Suggested values for various input impedances and voltage ranges are shown in Table 1.

For input voltage ranges and input impedances not covered by the Input Resistor Selection Table, the following formulas may be used to calculate series input resistor R1 and shunt resistor R2 (used to form an input "T" attenuator).

$$R2 = \frac{1}{\frac{VR}{Z_{IN}} - \frac{1}{1000}}$$

$$R1 = Z_{IN} - \frac{1000\ R2}{R2 + 1000}$$

where VR is the desired input voltage range of the board, Z_{IN} is the desired input impedance of the board, and the constant value 1000 is the input resistor R_{IN} (internal).

NAME	FUNCTION	VALUE	PIN
A_{IN}	Analog Input Voltage	See Text	23

CONTROL INPUTS

Two control inputs are provided for changing the format of the output data. When NMINV is tied to logic "0" the most significant bit of the output data is inverted. When the NLINV is tied to logic "0" the seven least significant bits of the output data are inverted. By using these DC controls, the output data can be read in binary, inverted binary, two's complement or inverted two's complement formats. Output data versus input voltage and control input state is illustrated in Table 2.

NAME	FUNCTION	VALUE	PIN
NMINV	Not Most Significant Bits Invert	TTL	5
NLINV	Not Least Significant Bits Invert	TTL	20

REFERENCE

The HS 1068 includes circuitry for generating the negative voltage necessary for the flash converter. Two reference voltages are made available for application circuits. The actual bandgap reference (+1.22 Volts) is brought out directly. The fullscale reference at the bottom of the flash resistor ladder is brought out through a 470 Ohm isolation resistor. If external trimpots are to be used to trim out system errors, these pins provide tracking sources exhibiting good power supply rejection for that purpose.

NAME	FUNCTION	VALUE	PIN
REF	Reference Output	1.22V	1
R_{BOT}	Negative REF	−2.07V	3

CONVERT

The HS 1068 samples within 10 nS of the rising edge of the "CONV" signal. Data is latched into the flash data resigter on the next rising edge, then into the output register on the next rising edge. Note that there are minimum width requirements on the waveshape of the CONV signal. If these requirements are met, sampling frequencies higher than 20 MHz can be obtained. However, the performance specifications are only tested with a squarewave 20 MHz convert clock and therefore are only guaranteed under these conditions.

NAME	FUNCTION	VALUE	PIN
CONV	A/D Clock Input	TTL	19

DATA OUTPUTS

The outputs of the HS 1068 are LSTTL compatible and are capable of driving ten STTL loads to 50 LSTTL loads. The outputs can be put into the high impedance state by use of the output enable (low) control pin. A TTL low will enable the outputs. Note that the zeroscale and fullscale flags are unaffected by outenlow.

NAME	FUNCTION	VALUE	PIN
D1 (MSB)	Most Significant Data Bit	TTL	9
D2		TTL	10
D3		TTL	11
D4		TTL	12
D5		TTL	13
D6		TTL	14
D7		TTL	15
D8 (LSB)	Least Significant Data Bit	TTL	16

CALIBRATION

The HS 1068 is trimmed after warmup at room temperature with still air. Operation in different ambient temperatures or different airflows may require offset voltage adjustment if absolute DC accuracy is important. The offset adjust pin is used for this purpose, as well as for choosing the unipolar/bipolar range of the converter. The recommended factory-trimmed bipolar range is obtained by leaving this pin "open" (NC). The factory trimmed unipolar range is obtained by shorting this pin to ground.

The Thevenin model of this pin consists of 600 Ohms in series with a +0.6 Volt voltage source. When shorted to ground 1mA flows through this pin. Note also that this 1mA "uses up" 1mA of the current which would be available for application circuit use out the V_{REF} pin. V_{REF} loading should be kept under 1mA when the converter is used in unipolar mode. When adjusting offset in the unipolar mode it is necessary to construct a circuit which can sink 1mA to some delta voltage around ground. A simple circuit would use a trimpot connected as a rheostat to obtain 1600 Ohms nominal between the offset pin and −2.07V (R_{BOT}) (Figure 1). A rheostat connection depends upon absolute resistor stability over temperature for its' temperature stability. Moreover, with 1mA through it the trimpot will incur self-heating errors. A more elegant circuit would use less current in a resistor ratio with an opamp buffer as shown in Figure 2.

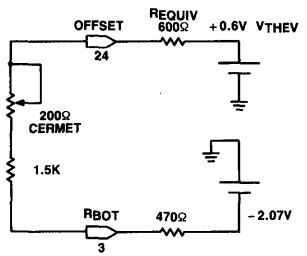


Figure 1. Unipolar Mode — External Offset Adjustment

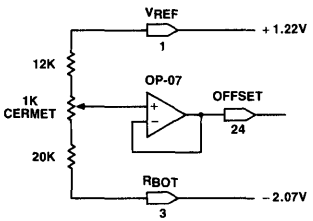


Figure 2. Unipolar Mode — Stable External Offset Adjustment

The bipolar mode offset adjust requires a source sitting close to +0.6 Volts with fairly high impedance. A ±30mV range at the amplifier output requires a ±18mV change into the Thevenin network implying ±30μA currents. A 5K Ohm potentiometer from +V_{REF} (1.22V) to ground can be used with a 20K Ohm resistor from wiper to offset pin to provide ±30μA into 0.6 Volts for a 30mV offset adjust range when in bipolar mode. This loads the +V_{REF} by only 0.25mA while using a resistor ratio for better temperature stability. If the range at the potentiometer

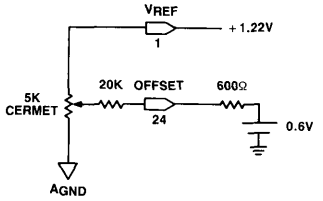


Figure 3. Bipolar Mode — External Offset Adjustment

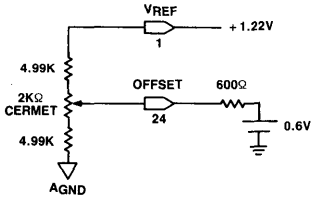


Figure 4. Bipolar Mode — Stable External Offset Adjustment

wiper was limited to ±20mV by pad resistors at each end, the 10K series resistor can be eliminated entirely for true ratiometric operation (see Figures 3 & 4).

The HS 1068 has been laser trimmed under typical conditions for a quantization range of 0.992 Volts p-p. In unipolar mode, for example, input voltages below +2mV output code "0" and input voltages above +0.994 Volts output code "255". System gain may be recalibrated at the converter by use of the range adjust pin. The recommended adjustment range should not exceed ±10%. In practice, power dissipation considerations make it more practical to use this pin solely for gain increases, as this tends to reduce the power dissipated in the flash resistor ladder. Gain reduction can be accomplished over a wide range by use of resistor padding at the input.

The Thevenin model of the range adjust pin is 933 Ohms to +1.035V nominal. This point drives an inverting gain of two amplifier which supplies the −2.07V reference (at up to 40 mA) to the bottom of the flash resistor ladder. Thus converter gain is adjusted by directly adjusting the full scale range of the flash itself. A gain increase of 10% can be obtained by loading down the voltage at the range adjust pin by 10%. A simple 1 to 10% gain increase control could consist of a 8.6k Ohm resistor in series with a 100k rheostat-connected trimpot to ground (Figure 5). This adjustment rapidly becomes less sensitive as the rheostat approaches zero Ohms. A more elegant approach is shown in Figure 6.

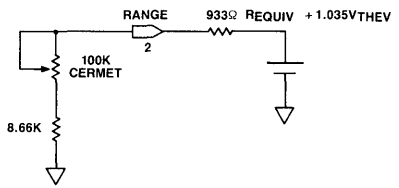


Figure 5. +1 to +10% External Gain Increase Circuit

A negatively offset input range is available for an input range of −1.0V to zero volts. This can be accomplished by tying the REF OUT pin to the OFFSET ADJ pin.

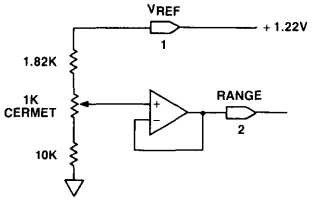


Figure 6. +8% to −1% External Gain Adjust Circuit

NAME	FUNCTION	VALUE	PIN
Range	Gain Adjustment		2
Offset	Offset Adjustment		24

ZERO AND FULLSCALE FLAGS

The endpoint codes of well behaved converters are of indeterminate width — that is they remain "clipped" for large values of out-of-range input voltage. The zero and fullscale flags are separate TTL signals to indicate that the input voltage is within/outside of the quantization range of the converter. They can be used to flag input protection circuitry when out-of-range values are applied, or as start or stop flags to begin processes after input-value conditions are met. They are gated from data within the pipeline of the converter, so that generally they will be valid before the data is valid. This allows an external decision to be made based on these flags before the data enters the rest of the user's system.

When the flash converter is running in the binary mode (and assuming unipolar offsets) the zero scale flag will detect the presence of zero or less than zero Volts at the input to the HS 1068 (all zeroes on the internal data bus). Similarly the fullscale flag corresponds to voltages of 0.994 Volts or greater at the input in binary mode (all ones on the internal data bus). When the flash converter is run in any of its other three possible coding formats, the meanings of these flags will change accordingly. The first one to consider is complementary binary (NMINV, NLIMV = low). In this mode the flags' meanings are interchanged. "Zeroscale" becomes active (high) at 0.994 Volts or greater and "Fullscale" becomes active (low) with inputs more negative than 2mV.

Note that "Fullscale" is an LSTTL output, while the "Zeroscale" is an LSTTL open collector gate with an internal 1.1KΩ pull up resistor.

AOUT

The AOUT pin is primarily used as a testpoint in calibrating the HS 1068. It supplies an inverted gain of two version of the input signal, exhibiting the offsetting necessary for unipolar or bipolar operation. A 470 Ohm isolation resistor protects the internal amplifier from ground shorts. Note that a −50mV nominal offset will be found here even in unipolar mode. It is added in at the input amplifier to compensate for offsets in the flash resistor ladder. This output can be buffered, even into a virtual ground, with minimal effect on the digitized signal.

Input Voltage Range										
Z_{IN}	1V		2V		4V		5V		10V	
	R1	R2	R1	R2	R1	R2	R1	R2	R1	R2
50	0	52.3	24.9	24.3	37.4	12.7	40.2	10	45.3	4.99
75	0	80.6	37.4	39.2	56.2	19.1	60.4	15.4	68.1	7.5
93	0	102	46.4	48.7	69.8	23.7	75	19.1	84.5	9.31
1k	0	open	499	1k	750	332	806	249	909	110

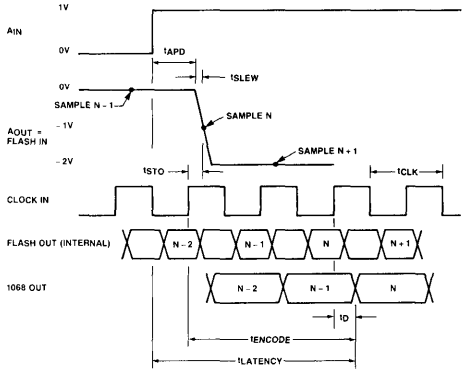
Table 1. Input Resistor Selection Table (Values in Ohms)

Input Voltage Code Center In Unipolar Mode	Binary		Two's Complement	
	True	Inverted	True	Inverted
	NMINV-1 NLINV-1	0 0	0 1	1 0
0.0000	00000000	11111111	10000000	01111111
+0.0039	00000001	11111110	10000001	01111110
*	*	*	*	*
*	*	*	*	*
*	*	*	*	*
+0.4960	01111111	10000000	11111111	00000000
+0.5000	10000000	01111111	00000000	11111111
*	*	*	*	*
*	*	*	*	*
*	*	*	*	*
+0.9920	11111110	00000001	01111110	10000001
+0.9960	11111111	00000000	01111111	10000000

Table 2. Output Coding Table[1]

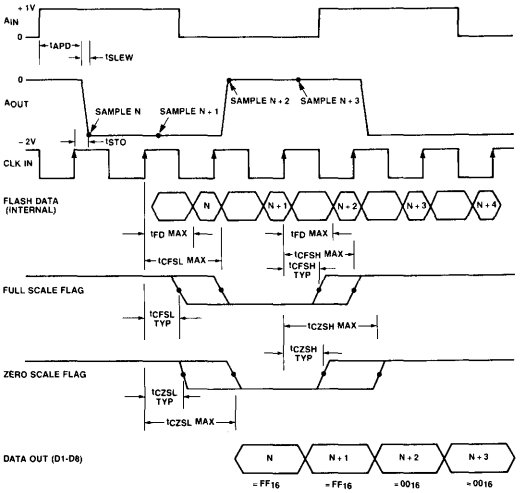
Note: 1. Input voltages are at code centers and buffer amplifier offset voltage is nulled.

TIMING DIAGRAMS



tAPD = AMPLIFIER PROPAGATION DELAY = 30 nS TYP
tSLEW = AMPLIFIER SLEWING TIME = 5 nS TYP
tSTO = SAMPLING TIME OFFSET = 0 TO 10 nS (10 nS TYP)
tD = DIGITAL OUTPUT DELAY = 15 nS TYP
tCLK = ONE CONVERT CLOCK CYCLE = 50 nS (FOR 20 MHZ SAMPLING)
tLATENCY = 2(tCLK) + tD - tSTO + tAPD + tSLEW = 140 nS (TYPICAL CONDITIONS)
TYPICAL CONDITIONS: ROOM AIR 24°C
VCC, VEE = NOMINAL
tCASE = 60°C
1 LSTTL LOAD

Figure 7. Output Data Timing Diagram



tFD MAX = INTERNAL FLASH DATA DELAY, MAX = 35 nS MAX
tCFSL = CLOCK TO/FULL SCALE FLAG ASSERTED (LOW) = 25 nS TYPICALLY
tCZSH = CLOCK TO ZERO SCALE FLAG ASSERTED (HIGH) = 29 nS TYPICALLY
tOVFSL = OVERVOLTAGE IN TO /FS = LOW = 100 nS TYP
tUVZSH = UNDERVOLTAGE TO ZS = HIGH = 105 nS TYP

TYPICAL CONDITION: ROOM AIR 24°C, 20 MHZ tCLK
VCC, VEE = NOM
tCASE = 60°C
1 LSTTL LOAD

Figure 8. Zero Scale/Full Scale Flags Timing Diagram

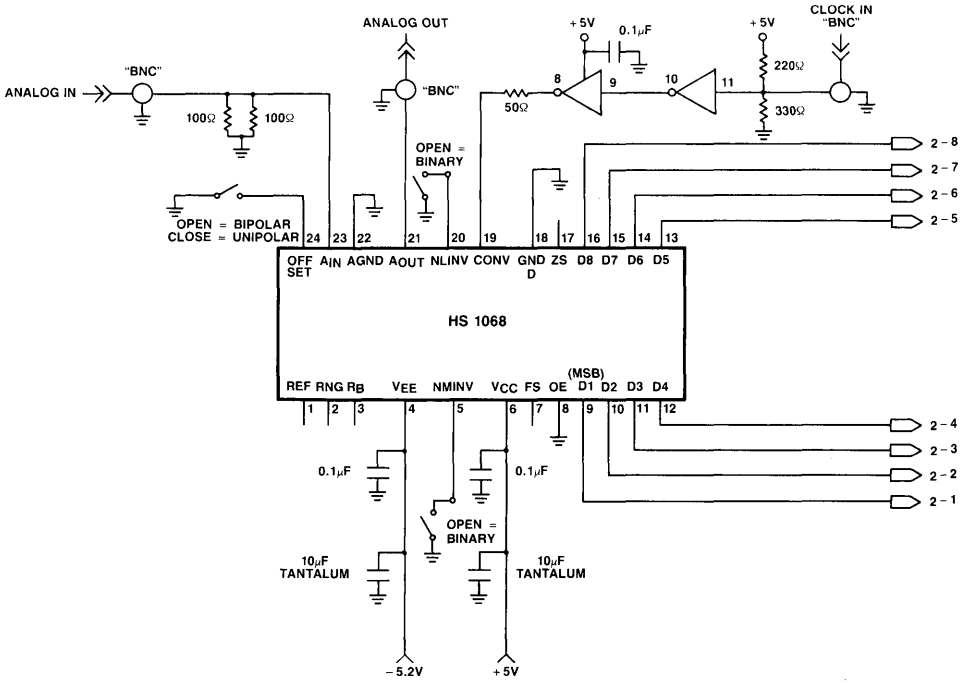


Figure 9. HS 1068 Connection Diagram

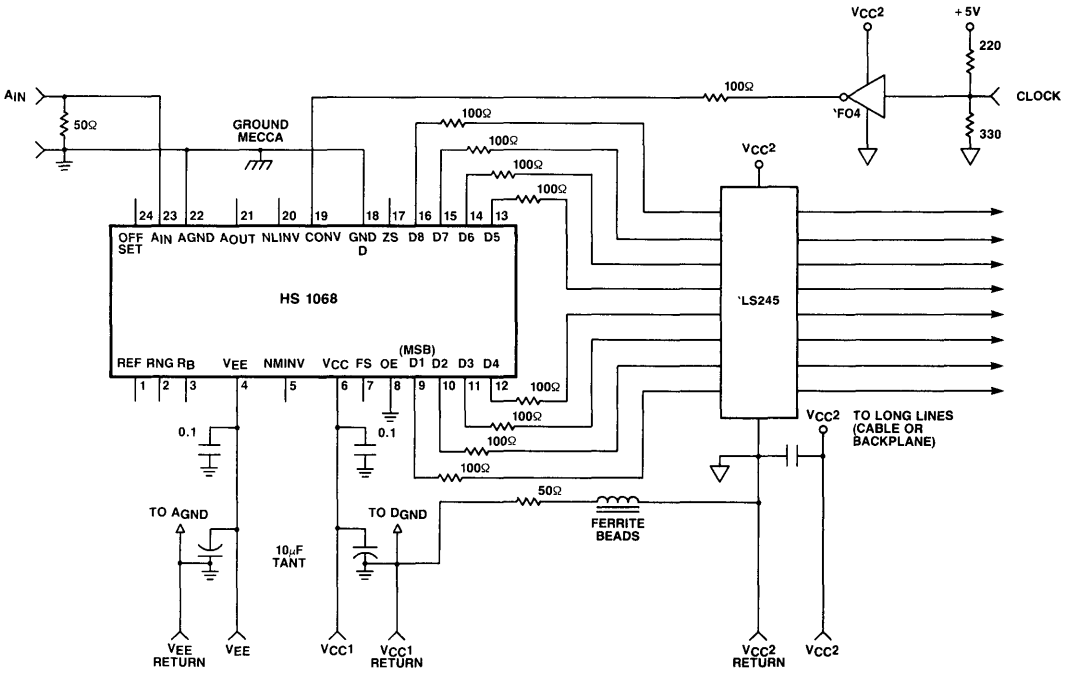


Figure 10. Isolating Digital Ground Noise From Converter Using RL Isolation at Digital Grounds (100Ω Resistors Used to Series Terminate Long Runs)

DYNAMIC TESTING OF THE HS 1068

The HS 1068 has been designed to minimize the dynamic distortions normally found in high speed digitizers. Its excellent dynamic performance is due to the low aperture jitter in the flash converter and the wide gain-bandwidth of the input amplifier. Dynamic distortion tests can be compared to the Total Harmonic Distortion, Noise and Intermodulation Distortion measurements usually made on audio information-carrying channels.

The dynamic tests done at Hybrid Systems utilize a low distortion oscillator, passive filters to insure signal purity, a 20-25 MS/sec fifo buffer and a computer. A flat-topped pulse generator is also used, without filtering, to measure settling times.

The SNR test is the primary measurement of signal fidelity. As performed at Hybrid, the test sequence involves running the converter under typical still room air conditions at 20 MS/s and grabbing a buffer of 4k points length. The data is multiplied by a Von Hann window, then a 4k point FFT is computed. The resulting spectrum is very carefully measured. The fundamental frequency is first identified, then the rms "Voltage" of the entire window-smeared fundamental section of the spectrum is computed. This section of the spectrum is then "notched out" by manually setting these frequency bins to zero. The rms sum of the rest of the spectrum is then computed and is designated the "noise". Note that any distortions or spurious signals (i.e. oscillations or power supply beats etc.) will be included as "noise". A linear spectrum approximating the Fourier Integral is the result of an FFT. Any non-harmonic component in the data will faithfully be reproduced, without the ambiguity associated with a Fourier Series expansion, which assumes a signal may be completely described by its harmonics.

Sampling theory can be used to derive the SNR of an ideal converter, one whose only error is due to the quantization of the numbers describing each point. The result is the well known formula:

SNR (rms sig to rms "noise") = 6.02 x N + 1.76 dB
where N = number of bits in quantized number

In this formula the 1.76 dB applies for all practical cases where the quantization noise will be uncorrelated (white) with respect to the input signal. (This number approaches zero as the input signal approaches DC compared to the sampling frequency — in so-called "coarse quantization").

Figure 11 shows the excellent agreement between theory and the SNR algorithm when ideal computer-generated data is measured. Remember that 49.92 dB SNR is the ideal number for an 8 bit converter with no linearity errors and is due to the quantization noise alone. If a converter were to exhibit ½ LSB of linearity errors, its SNR would be expected to show 3 dB less SNR. At 1 LSB of linearity error, 6 dB less SNR is expected. The HS 1068 under typical conditions exhibits ½ LSB linearity at up to 1.1 MHz (Figure 12) inputs and is still showing 1 LSB error at 4.0 MHz fullscale inputs. For less than fullscale input levels or when cooled, the HS 1068 can exhibit lower total linearity errors.

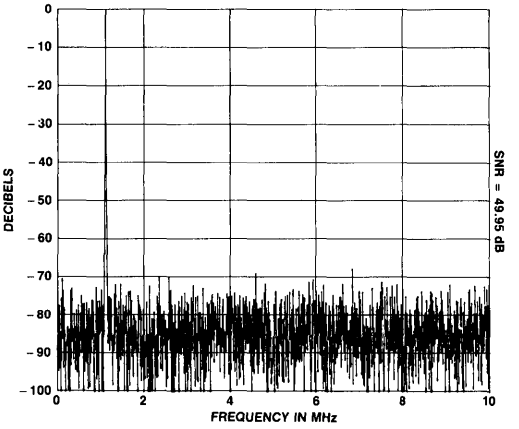


Figure 11. FFT of Ideal 8-Bit Converter

The SNR vs. Input Level graph (Figure 14) points out one of the design compromises at the input buffer. Fullscale high frequency signals generate some (up to 1.25%) harmonic distortion when the buffer is internally compensated for settling time optimization.

The converter power bandwidth is defined separately from the −3 dB frequency of the input amplifier. Power bandwidth here means the frequency at which a full scale input sinewave causes spurious codes. As such it is related to a slew rate, above which the differential delay through the flash comparators can cause a gross encoding error. At room temperature conditions, the power bandwidth is typically 13 MHz, well above the normal Nyquist bandlimit for 20 MS/sec encoding. Spurious codes are detected by measuring the variance in 10 SNR measurements, representing 40,960 samples. A variance of 0.1 dB or more indicates that a spurious code was present. (Some variance will always occur due to the random start points of the sampled sine waves — typically sigma squared equals 0.01 dB or less.)

The beat frequency test is another powerful dynamic test technique, and is used at Hybrid Systems to measure settling times, as well as a graphical tool for "seeing" spurious codes (Figure 15). A stable frequency oscillator is set to a small delta frequency over the sampling rate. The resulting output data "walks through" the input wave with very small time steps. The frequency is picked to produce one full cycle of this beat frequency in one buffer (4k points) of data. Settling times may be measured very accurately because the very low aperture jitter of the flash converter ensures the accuracy of the resulting "walked through" data points.

Histogram testing is a useful tool to evaluate the dynamic differential linearity of a video speed converter. A filtered sine wave is applied to the converter and 10 buffers of 4k points are stored. The number of occurences of each code is then determined, and this histogram is compared with an ideal quantized sine wave of the same gain and offset. The ratio of the real number of occurences to the ideal number of occurences yields an effective code width for each code. The ideal code width (one) is subtracted from this ratio to yield the dynamic differential linearity error as shown in Figures 16 thru 18. The excellent dynamic perfor-

mance of this part shows up as near ideal dynamic differential linearity, even as the input frequency approaches and exceeds the Nyquist bandlimit. Other flash converters must utilize internal grey scale encoders to limit the extent of dynamic differential linearity errors at frequencies as low as one half the Nyquist bandlimit — and still cannot guarantee no missing codes at these frequencies — caveat emptor!

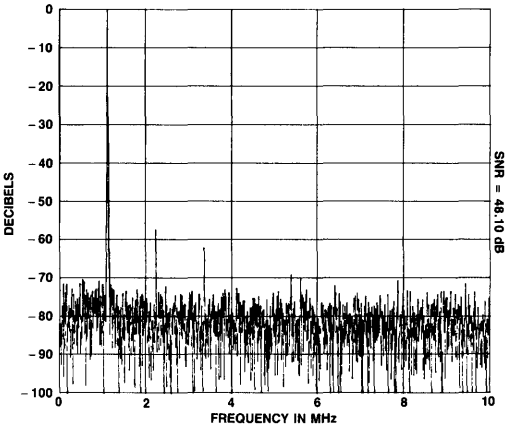


Figure 12. FFT of HS 1068, F_{IN} = 1.123 MHz, F_{SAMPLE} = 20 MHz

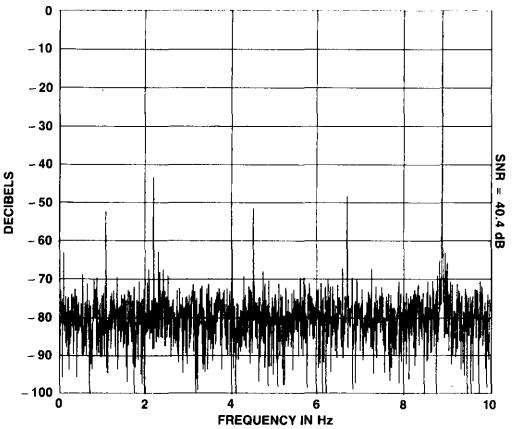


Figure 13. FFT of HS 1068, F_{IN} = 8.9 MHz, F_S = 20 MHz

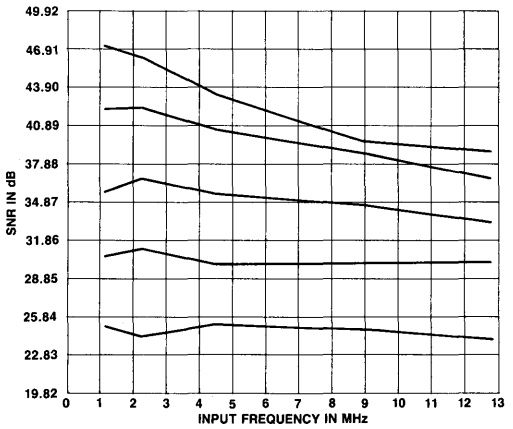


Figure 14. HS 1068 SNR Vs. Frequency Showing 0 to – 24 dB Input Levels, F_S = 20 MHz

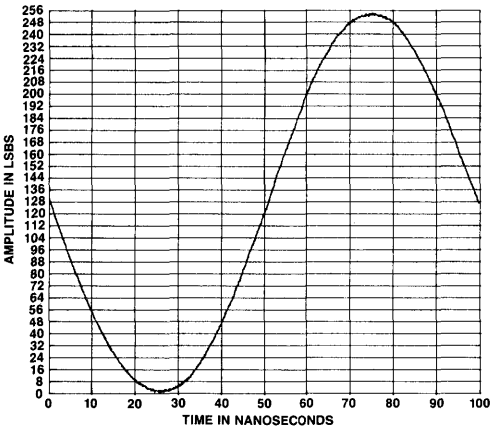


Figure 15. HS 1068 Beat Frequency Test F_{IN} = 10 + MHz, F_S = 20 MHz

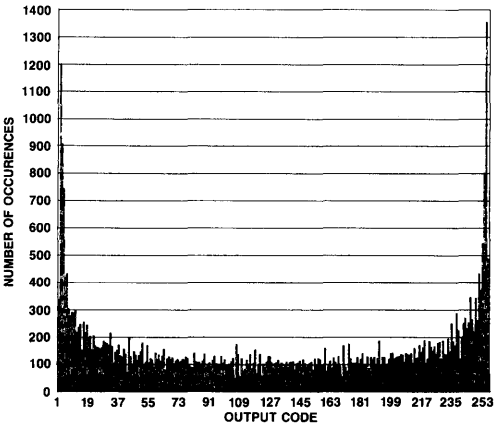


Figure 16. Histogram of HS 1068, F_{IN} = 8.9 MHz, F_S = 20 MHz

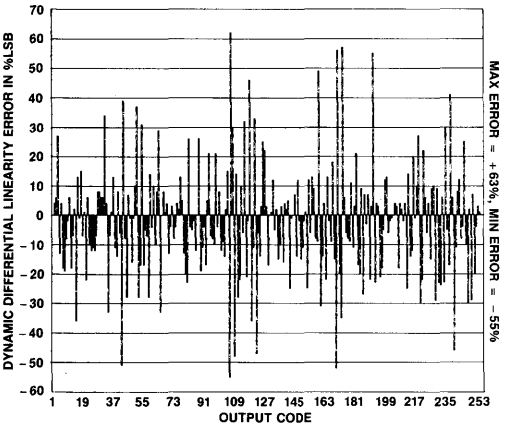


Figure 17. HS 1068 Dynamic Differential Linearity Error, F_{IN} = 8.9 MHz, F_S = 20 MHz

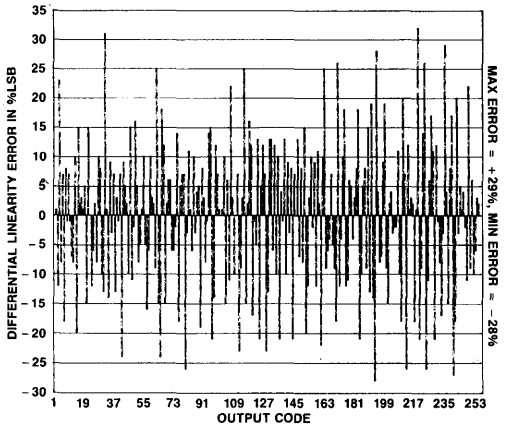


Figure 18. HS 168 Dynamic Differential Linearity Error Low Frequency Input, $F_S = 20$ MHz

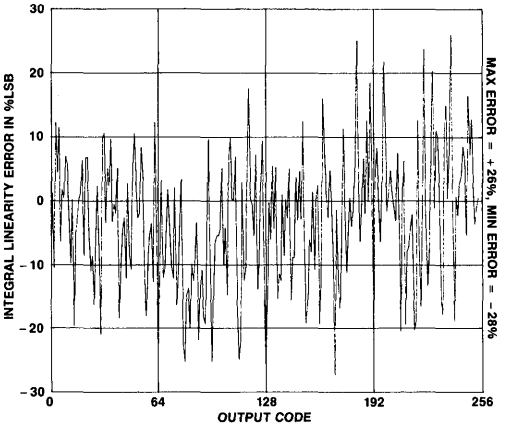


Figure 19. HS 168 Dynamic Integral Linearity Error Low Freuency Input, $F_S = 20$ MHz

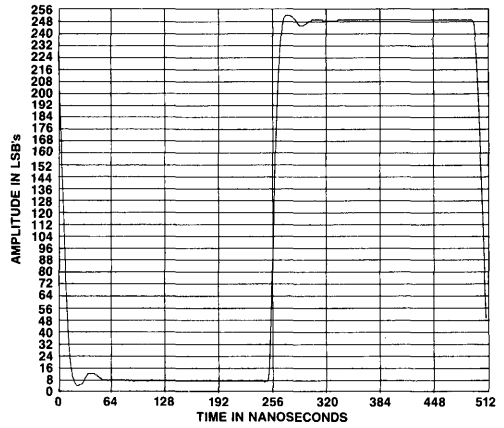


Figure 20. HS 1068 Beat Frequency Input Amplifier Settling Time $F_{IN} = 2+$ MHz, $F_S = 20$ MHz

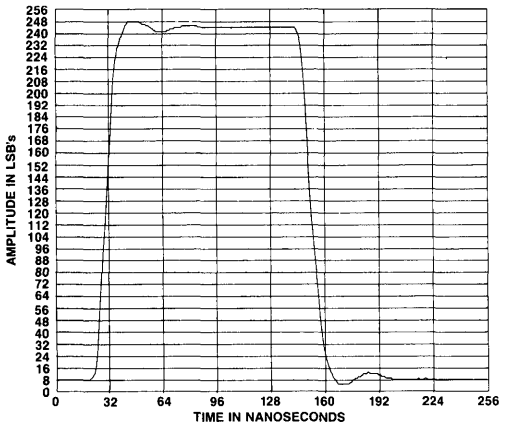


Figure 21. HS 1068 Beat Frequency Input Amplifier Settling Time $F_{IN} = 4+$ MHz, $F_S = 20$ MHz

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	DESCRIPTION
HS 1068C	−0°C to +70°C	8-Bit, 20 MHz ADC
HS 1068B	−55°C to +125°C	8-Bit, 20 MHz ADC, MIL-STD-883C Screening

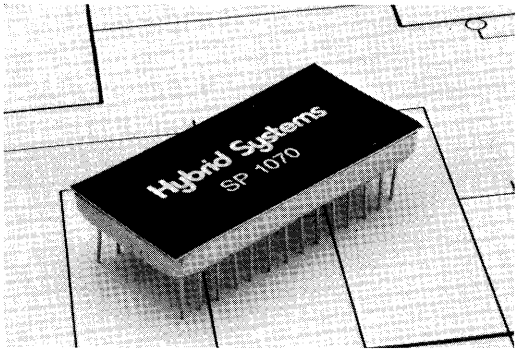
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP1070

8-BIT 25 MSPS A/D CONVERTER

FEATURES

- Complete analog front-end and 25MHz ADC in a single package
- Low power consumption, 1W
- DC stabilized input amplifier
- Pin selectable RS170/RS343 gains

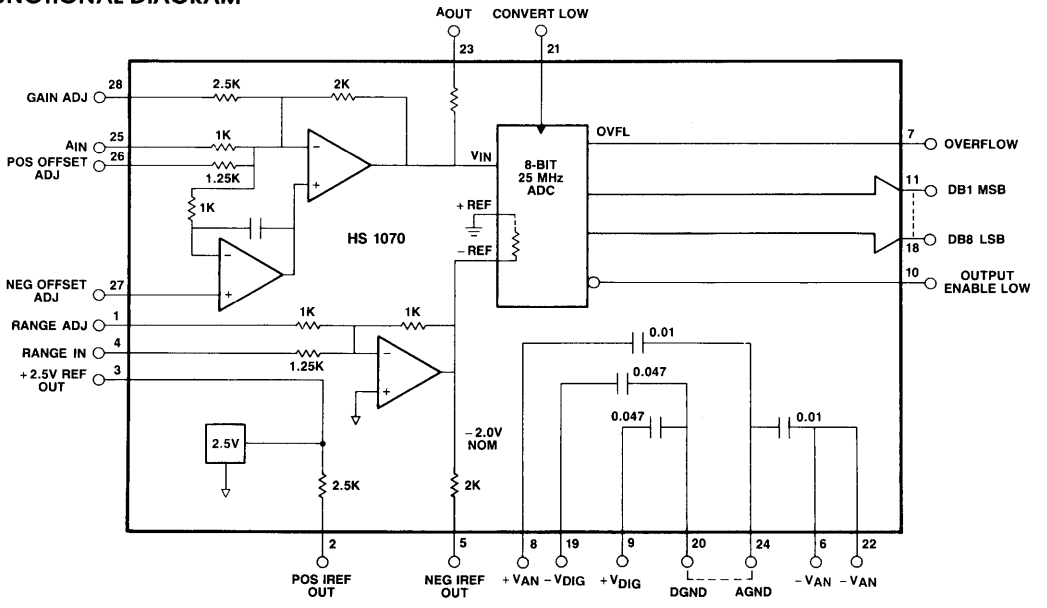


DESCRIPTION

The SP1070 is a complete flash analog to digital converter that includes all the circuitry necessary to convert video frequency analog signals into 8-bit digital data at rates up to 25 mega samples per second. The SP1070 is completely self contained providing a low power, 8-bit, 25MHz, flash A/D; a DC-stabilized wideband input amplifier; overload protection/recovery circuitry and 2.5 volt boot-strapped reference in a single 28-pin package.

The combination of all this circuitry into a single hermetic 28-pin DIP offers significant savings in board space; It also saves on component, assembly and design costs, while offereing tremendous flexibility in application circuits. Operation over the full military temperature range (−55°C to +125°C) and full compliance with MIL-STD-883C is available.

FUNCTIONAL DIAGRAM



8

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage	V_{CC}	7.0	V
	$+V_A$	17.5	V
	V_{EE}	−7.0	V
	$-V_A$	−17.5	V
Digital Input Voltage	$V_{IN}(D)$	5.5	V
Analog Input Voltage	$V_{IN}(A)$	±5.5	V
Reference Voltage Span	$(A_{GND} - V_{pin\ 5})$	2.2	V
Applied Output Voltage	—	5.5	V
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEMPERATURE RANGE						UNITS
		0°C to +70°C			−55°C to +125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Digital Supply Voltage (Positive)	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
Analog Supply Voltage (Positive)	$+V_A$	4.75	5.0	15.0	4.75	5.0	15.0	V
Digital Supply Voltage (Negative)	V_{EE}	−3.0	−5.0	−6.0	−3.0	−5.0	−6.0	V
Analog Supply Voltage (Negative)	$-V_A$	−4.75	−5.0	−15.0	−4.75	−5.0	−15.0	V
Analog Ground	(AGND-DGND)	−0.1	0	+0.1	−0.1	0	+0.1	V
Analog Input, Range ADJ and OFFSET ADJ Open	$V_{IN}(A)$	0.0		+1.0	0.0		+1.0	V
Digital Input Voltage, HIGH	$V_{IN}(D)$	2.0			2.0			V
Digital Input Voltage, LOW				0.8			0.8	V
Applied Output Voltage	V_o	0.0		V_{CC}	0.0		V_{CC}	V
CONV Pulse Width, LOW	t_{PWL}	15			15			nS
CONV Pulse Width, HIGH	t_{PWH}	5			5			nS
Clock Frequency, Max	f_{CLK}	25			25			MHz
Operating Ambient Temperature	T_A	0		70				°C
Operating Case Temperature	T_C				−55		+125	°C

PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS (F_{Sample} = 20 MHz)	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution	N				8.0			8.0	Bits
Integral Linearity Error	E_{LI}	DC, Best Straight Line		±0.5	±1.0		±0.5	±1.0	LSB
Differential Linearity Error	E_{DI}	DC		±0.4	±0.85		±0.4	±0.75	LSB
RMS Signal/RMS Noise + Distortion	SNR	1.123 MHz Input	45	47		44	47		dB
		2.234 MHz Input	44	45		43	45		dB
		4.456 MHz Input	38	40		36	40		dB
Differential Phase	DP	F_S = 4 x NTSC Carrier		1			1		Degree
Differential Gain	DC	F_S = 4 x NTSC Carrier		1			1		%
Aperture Error	E_{AP}	Apeture Jitter		±300			±300		pS
Full Power Bandwidth	BW	No Missing Code	4	6		4	6		MHz
Input Amplifier Full Power Bandwidth	ABW	Freq −3 dB		20			20		MHz
Settling Time (to 0.1%)	t_S	Full Scale Transition		60	100		60	150	nS
Amplifier Overshoot	O_S			0			0		%
Overload Recovery	t_{REC}	±500 mV Overdrive		10			10		nS
Input Amplifier Noise		10 MHz Bandwidth[2]		200			200		μVRMS
Range AMP Bandwidth			5	8		5	8		MHz
Range AMP Settling		One Volt Step at R_{BOT}		0.5	1.0		0.5	1.0	μSec

SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Conversion Rate	F_S	V_{CC}, V_{EE} = MIN	25	30		20	25	30	MHz
Sampling Time Offset	t_{STO}	V_{CC}, V_{EE} = MIN	0	10		0	10		nS
Digital Output Delay	t_D	V_{CC} = MIN	15	19		15	19		nS
Digital Output Enable	t_{PZL}	V_{CC} = MIN		20			20		nS
Digital Output Disable	t_{PHZ}	V_{CC} = MIN		15			15		nS
Overflow	t_{OVF}	V_{CC} = MIN		20			20		nS
CONV Pulse Width, LOW	t_{PWL}	V_{CC} = MIN	15			15			nS
CONV Pulse Width, HIGH	t_{PWH}	V_{CC} = MIN	5			5			nS

INPUTS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Current, Logic LOW	I_{IL}								
		OE @0.4V		−0.1	−0.4		−0.1	−0.8	mA
		CONV @0.4V		−0.1	−0.4		−0.1	−0.8	mA
Input Current, Logic HIGH	I_{IH}	OE @2.7V			20			40	μA
		CONV		0	100		0	100	μA
Input Voltage, Logic LOW	V_{IL}				0.8			0.8	V
Input Voltage, Logic HIGH	V_{IH}		2.0			2.0			V
Analog Input Resistance	R_{IN}		0.99K	1K	1.01K	0.99K	1K	1.01K	
Analog Input Capacitance	C_{IN}			3			3		pF
Input Offset Current	I_B	$I_B = V_{OS}$/1K Ohm		0.1			0.1		mA
Gain Error	E_G			±0.1			±0.1		%
Bipolar Offset Error				±0.5			±0.1		LSB
Unipolar Offset Error				±0.5			±0.1		LSB
Bipolar Offset Error Tempco	T_{CB}	LSB's/°C Case temp rise		±0.01			+0.005		LSB/°C
Unipolar Offset Error Tempco	T_{CU}	LSB's/°C Case temp rise		±0.01			+0.005		LSB/°C

DIGITAL OUTPUTS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Leakage Current, Logic LOW	I_{LOL}	V_O = 0.4V (3-State)			−50			−50	μA
Output Leakage Current, Logic HIGH	I_{LOH}	V_O = 2.4V (3-State)			50			50	μA
Output Voltage, Logic LOW	V_{OL}	I_{OL} = 4 mA		0.35	0.4		0.35	0.4	V
Output Voltage, Logic HIGH	V_{OH}	I_{OH} = −0.4mA	2.4	3.0		2.4	3.0		V
Short Circuit Output Current	I_{OS}	V_{CC} = MAX, Output HIGH, 1 sec		35			35		mA
Output Capacitance	C_{OUT}	(3-State)		9			9		pF

REFERENCE

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Reference Voltage	V_{REF}	V_{REF} OUT	2.49	2.500	2.51	2.48	2.500	2.52	V
Reference Current, Sourced	I_{REF}	V_{REF} to GND	8			8			mA
Reference Adjustment Range	R_{ADJ}	Recommended Range[4]	−1.0		−2.0	−1.0		−2.0	V

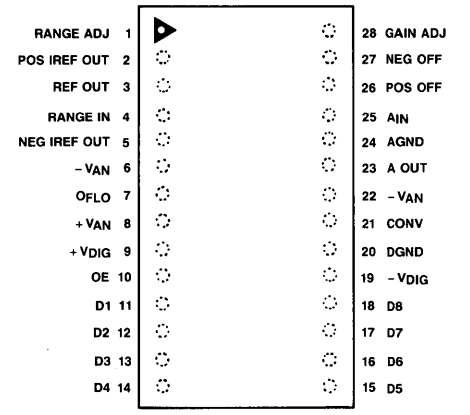
POWER SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Positive Digital Supply Current	I_{CC}	V_{DIG} = 5.0V		114			114		mA
		V_{DIG} = 5.5V					123		mA
Negative Digital Supply Current	I_{EE}	$-V_{DIG}$ = 5.0V		10			10		mA
		$-V_{DIG}$ = 6.0V		10			10		mA
Positive Analog Supply Current	$+I_{AN}$	$+V_{AN}$ = 5.0V		26			26		mA
		$+V_{AN}$ = 5.5V					26.5		mA
Negative Analog Supply Current	$-I_{AN}$	$-V_{AN}$ = 5.0V		43			43		mA
		$-V_{AN}$ = 5.5V					43.5		mA
Power Dissipation		V_{DIG} = V_{AN} = Nominal		0.965			0.965		W
Fs = 20 MHz		$-V_{DIG}$ = $-V_{AN}$ = 10% High					1.117		W

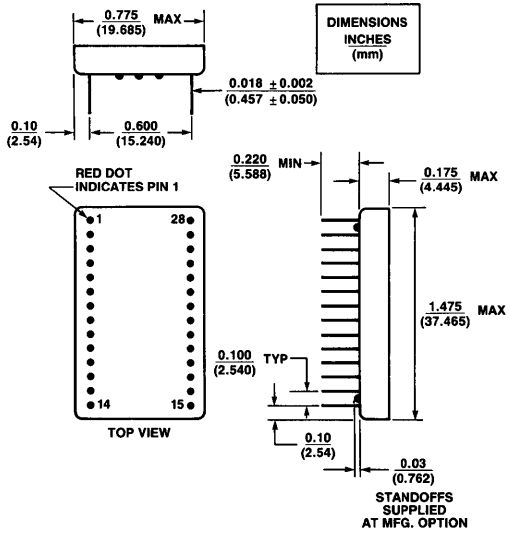
PIN ASSIGNMENTS

PIN	SYMBOL	FUNCTION
1	RANGE ADJ	Range Adjust
2	POS I_{REF} OUT	Isolated Reference Out, Positive, 2.5V
3	REF OUT	Reference Out, 2.5V
4	RANGE IN	Full Scale Range Adjust
5	NEG I_{REF} OUT	Isolated Reference Out, Negative, 2.05V
6	$-V_{AN}$	Negative Analog Supply Voltage
7	O_{FLO}	Overflow Detector, Active High
8	$+V_{AN}$	Positive Analog Supply Voltage
9	$+V_{DIG}$	Positive Digial Supply Voltage, +5V
10	OE	Output Enable Low
11	D1	Data Bit 1
12	D2	Data Bit 2
13	D3	Data Bit 3
14	D4	Data Bit 4
15	D5	Data Bit 5
16	D6	Data Bit 6
17	D7	Data Bit 7
18	D8	Data Bit 8
19	$-V_{DIG}$	Negative Digital Supply Voltage
20	D_{GND}	Digital Ground
21	CONV	Convert Low
22	$-V_{AN}$	Negative Analog Supply Voltage
23	A_{OUT}	Test Point (Amplifier Output, Flash Input)
24	A_{GND}	Analog Ground
25	A_{IN}	Analog Signal Input
26	POS OFF	Positive Offset Adjust
27	NEG OFF	Negative Offset Adjust
28	GAIN ADJ	Gain Adjust

PIN ASSIGNMENTS



PACKAGE OUTLINE



ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	DESCRIPTION
SP 1070C	−0°C to +70°C	8-Bit, 25 MHz ADC
SP 1070B	−55°C to +125°C	8-Bit, 25 MHz ADC, MIL-STD-883C Screening

THEORY OF OPERATION

The SP 1070 consists of four circuit blocks: the input amplifier, the fullscale range amplifier, the 2.5 Volt reference, and the flash converter and its control logic. The analog and digital grounds are separated to provide flexibility in system grounding and decoupling. The additional isolation of the amplifier supplies from the flash supplies allows a wide range of supply voltages or decoupling schemes to be utilized.

The input amplifier is a DC stabilized feedforward design which overcomes the DC drift and warmup problems of a single stage design. It features two summing inputs which may be pin strapped together for 0.714 Volt (RS343) fullscale or used separately for 1 Volt (RS170) or 2.5 Volt fullscale nominal levels. A third summing input can provide a 1.25 Volt input range. Any of these pins which are not used as signal inputs may be used as offset adjustment points. Unused inputs should be left unconnected to maintain maximum amplifier bandwidth.

Typical sources can drive the 714-to-2.5K Ohm input impedance. External resistors to ground can be used to terminate 50 or 75 Ohm cabling. Higher input fullscale voltages can be applied by constructing an external "Tee" attenuator of the desired impedance.

The feedforward configuration provides two modes of adjusting system offset. Offset voltages may be applied to any of the unused summing inputs or to the amplifier non-inverting terminal at NEG OFF ADJ. Note that the operation of these two points is complementary — a positive voltage on a summing input will offset the amplfier output negatively, while the same voltage on the NEG OFF ADJ pin will force the amplfier in the positive direction. The NEG OFF ADJ pin is a high impedance point and is therefore preferred for use with trimpots or E2POTS. An external current output DAC can be used with any of the summing inputs to provide a current mode (high speed) programmable amplifier offset. The positive offset adjust pin can be used for this purpose when either of the video standard gains is chosen, and requires a DAC voltage compliance of only 1.25 Volts for a full-scale offset change (+1mA).

When the 1 Volt range is chosen, the normal factory trimmed ranges may be chosen by:

a) 0 to 1V — ground NEG OFF ADJ, POS OFF ADJ = unconnected
b) −0.5 to +0.5 — ground NEG OFF ADJ, connect POS IREF to GAIN ADJ
c) −1 to 0V — ground NEG OFF ADJ, connect VREF to GAIN ADJ

A resistor isolated (500 Ohm) analog output testpoint is brought out for debugging or application circuit use. Note that it will show any offsets necessary for proper operation over the −25mV to −2.025V (nominal) input range at the flash input. Amplifier settling time is optimized at the factory by an internal variable capacitor.

The 2.5 Volt reference is a fixed positive reference used to generate tracking outputs for pin strap offset and gain options. V_{REF} is normally tied to the inverting range amplifier input to generate the −2.025V nominal reference to the bottom of the flash resistor ladder. User adjustment of system gain is normally done at the range amplifier adjust input. The V_{REF} output is buffered and up to 8mA is available for use in application circuits. The second output, POS I_{REF}, provides a 2.5K Ohm series resistor to generate 1mA nominal into a virtual ground. This pin is especially useful for supplying a reference current to an external DAC for programmable gains or offsets.

The range amplifier is an inverting amplifier with a power buffer used to generate the large currents needed to drive the flash resistor ladder. It directly sets the fullscale range at the flash converter. Any gain adjustment should be done here at the range adjust pin (normally grounded for factory laser trimmed nominal gains). The settling time to 0.1% of this amplifier is less than 1 s. By use of an external current mode DAC, the fullscale range of the converter may be updated very quickly, during one horizontal flyback interval, for example. A DAC drawing 0 to 1mA from the RANGE ADJ pin can program an effective two-to-one gain increase at the expense of some loss of differential linearity at the highest gains. Gain decreases are best accomplished by attenuating at the input.

The input amplifier, range amplifier and reference all share the isolated supplies $+V_{AN}$ and $-V_{AN}$. For minimal power dissipation the best choice for these supplies is +5V, −5.2V, but any values up to ±15V are possible, allowing the system designer to choose the "cleanest" supplies available. The flash converter requires +5V nominal and a negative supply of −3 to −6 Volts (−5 Volts nominal if tied to $-V_{AN}$) at V_{CC} and V_{EE} pins respectively. Only 53mA of current is necessary from a single −5.2 Volt supply when V_{EE} is tied to $-V_{AN}$.

The flash converter requires a TTL convert clock from DC to 25 MHz. The outputs are enabled when OUT EN is at TTL low. The OVERFLOW output is not three-stateable, and is not affected by the OUT EN control.

OUTPUT CODING OF SP 1070

The SP 1070 outputs are in complement binary form. The table below gives the input voltage at pin 25 for both 0 to 1V fullscale operation (pins 26, 28 open) and for ±0.5V fullscale (pin 3 to pin 28). For a negative input voltage range (−1 to 0V) tie pin 3 to pin 26. Operation at other ranges will be similar to the complement binary and offset complement binary ranges shown. Binary coding requires external inverters at outputs.

+Unipolar	Bipolar (V_{IN} at Code Centers)	−Unipolar	Code Output	Overflow Output
−0.0039	−0.5039	−1.0039	1111 1111	1
0.0000	−0.5000	−1.0000	1111 1111	0
+0.0039	−0.4960	−0.9960	1111 1110	0
+0.4960	−0.0039	−0.5039	0111 1111	0
+0.5000	0.0000	−0.5000	1000 0000	0
+0.992	+0.4920	−0.0080	0000 0001	0
+0.996	+0.4960	−0.0039	0000 0000	0
+1.000*	+0.5000*	0.0000*	0000 0000*	0*

*Denotes underflow not detected at overflow output

CALIBRATION

The SP 1070 is laser trimmed for unipoar and bipolar gains and offsets utilizing the 1 Volt fullscale range input (pin 25). The other input resistors are passively trimmed to correctly ratio the input resistor at pin 25. Normal room temperature operation will require no external trimming. Offset and gain errors arising from earlier stages of the system, or the utilization of the programmable gain and offset pins for more sophisticated applications may require external gain or offset trimming. Pins 2 and 3 provide positive voltages and pin 5 provides a negative reference voltage which exhibit excellent power supply rejection and should be used to drive any external trimpots or current mode D/A converters used for trimming.

One simple offset adjustment circuit is shown below. This circuit utilizes the internal resistors at pins 2 and 5 to minimize the ratio drift that external resistors will exhibit. No input pins are "used up" by this circuit, allowing it to be used for all unipolar input ranges. Note that the resistor at pin 2 will show some variation from the absolute 2.5K Ohm value shown, as it has been laser trimmed when connected to pin 28 for bipolar offset adjustment. This circuit uses pin 28 and thus cannot easily be used to trim bipolar mode offset — the circuit of Figure 2 will trim both unipolar and bipolar offsets. Note that now pin 28 is "used up", and is unavailable for use in setting the fullscale input range, as in the ±0.357 Volt fullscale input range. Figure 3 shows a circuit which does not need pin 28 and allows independent adjustment of unipolar and bipolar offsets. Unipolar offset should be adjusted first, as this trimpot will affect both unipolar and bipolar offsets. Note that for bipolar operation only, pin 27 can be grounded and the 200 Ohm trimpot is unnecessary.

The gain of the SP 1070 is adjusted by sinking or sourcing current into the RANGE ADJ (pin 1). This operation will cause the −2.05 Volts at the flash converter reference to change, thus directly setting the fullscale range. The voltage at NEG I_{REF} (pin 5) will change correspondingly. When NEG I_{REF} is used to drive external offset adjustment rimpots in fixed gain applications the gain should be adjusted as early in the trim procedure as possible. This will minimize the interaction between the gain and offset trims.

Note that external trim circuits which use the NEG I_{REF} pin to set the reference of a multiplying DAC (such as a DAC-08) will exhibit a very useful feature: the offset can be set to any percentage of fullscale which is desired, than as the gain is changed over the allowed 2 to 1 range, the offset will track accordingly.

Some useful, although complex to analyze, circuits can be used for gain increases. For example, after tying pin 3 to pin 4 for normal operation, pin 5 can be tied to pin 1 for a 25% gain increase (−1.52 Volts fullscale at the flash). If an external resistor is added, as in Figure 4, infinitely adjustable gains of 0 to 10% can be achieved, although temperature stability will be determined by the temperature stability of the ratio of external to internal resistors.

Gain reduction (setting the flash reference more negative than the −2.05V nominal) is discouraged, as the range amplifier headroom from the NEG V_{AN} supply is limited at minimum NEG V_{AN} values. The reference voltage at the flash can safely be brought to −2.2 Volts only if the NEG V_{AN} supply is more negative than −4.9 Volts. Gain reduction is easily done by resistor padding at the inputs or by choice of an appropriate input pin.

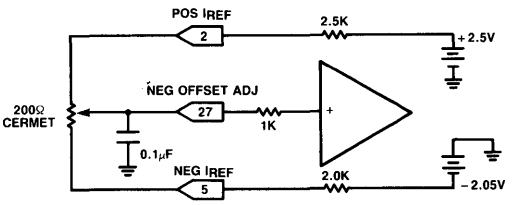


Figure 1. Simple Unipolar Range Offset Adjustment Circuit

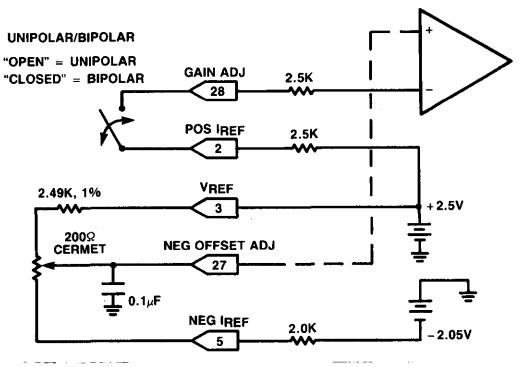


Figure 2. Unipolar/Bipolar Range Offset Adjustment Circuit

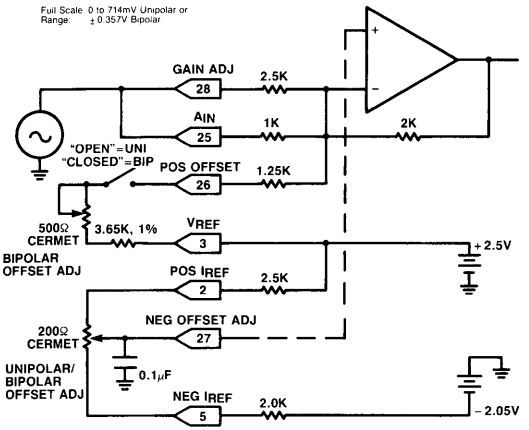


Figure 3. Offset Adjustment Circuit for Bipolar Range When Pin 28 is Used in Pin Strapped Gain Selection

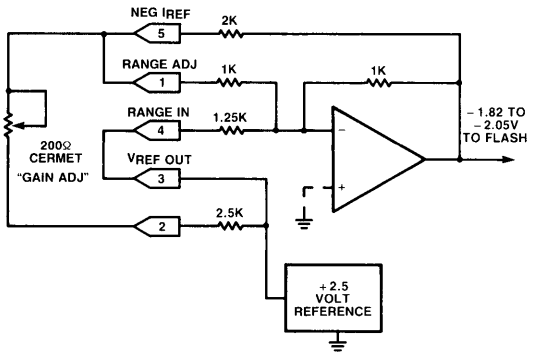
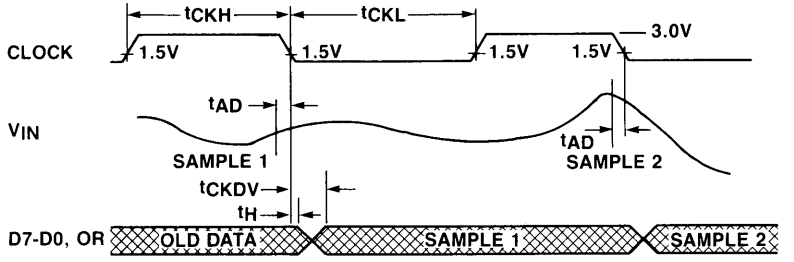
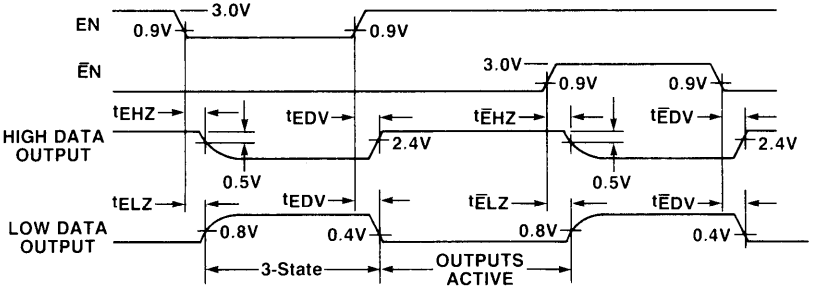


Figure 4. Gain Adjustment Circuit for 0 to 10% Gain Increase

System Timing Diagrams

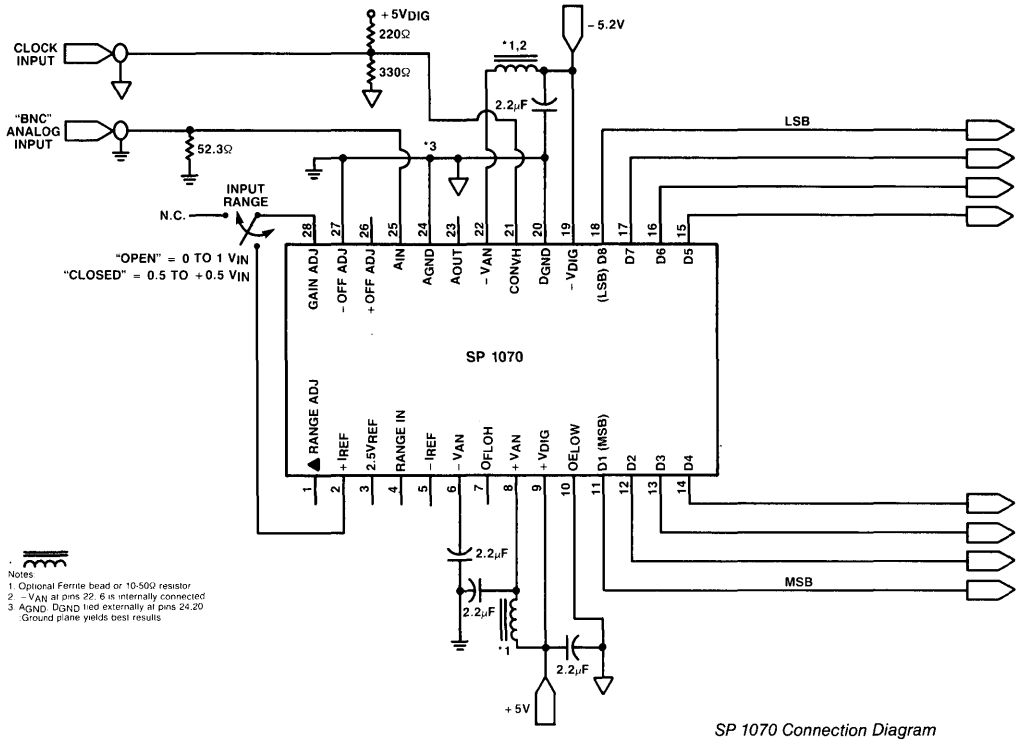


tCKDV and tH measured at output levels of 0.8 and 2.4 volts.



TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = +5.0V, V_{EE} = 5.2V. See System Timing Diagram.)

Parameter	Symbol	Min	Typ	Max	Unit
INPUTS					
Min Clock Pulse Width — High	t_{CKH}	—	5.0	—	ns
Min Clock Pulse Width — Low	t_{CKL}	—	15	—	ns
Max Clock Rise, Fall Time	$t_{R,F}$	—	100	—	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	—	19	—	ns
Aperture Delay	t_{AD}	—	4.0	—	ns
Hold Time	t_H	—	6.0	—	na
Data High to 3-State from Enable Low*	t_{EHZ}	—	27	—	ns
Data Low to 3-State from Enable Low*	t_{ELZ}	—	18	—	ns
Data High to 3-State from Enable High*	t_{EHZ}	—	32	—	ns
Data Low to 3-State from Enable High*	t_{ELZ}	—	18	—	ns
Valid Data from Enable High (Pin 20 = 0V)*	t_{EDV}	—	15	—	ns
Valid Data from Enable Low (Pin 19 = 5.0V)*	t_{EDV}	—	16	—	ns
Output Transition Time* (10%-90%)	t_{tr}	—	8.0	—	ns



SP 1070 Connection Diagram
Minimal Power Dissipation Application Circuit

DYNAMIC TESTING OF THE SP 1070

The SP 1070 has been designed and characterized upon a high speed dynamic test system developed at Hybrid Systems. It's wide bandwidth amplifier and Gray scale encoded flash converter provide excellent dynamic performance at sampling frequencies to 25 MHz.

All dynamic performance characteristics as well as all DC trimming and linearity specifications are 100% tested at a sample rate of 20 MHz. Note that the DC linearity specifications become even better as the sample rate is lowered. SP 1070 "B" grade parts are tested at 20 MHz over the full military temperature range. The parts are also characterized here at room temperature at 25 MHz.

Figures (A) and (B) shown an FFT and a signal-to-noise + distortion number at each frequency input. Any harmonics of the fundamental which show in the graphs are due to integral nonlinearity in either the input amplifier or the flash converter transfer curve. Any noise in the hybrid or any dynamic differential linearity errors will raise the noise floor of the graph above that generated by 8-Bit quantization noise floor of an ideal converter. Note that higher order harmonics will alias back down into the FFT spectrums shown. The SNR number as defined here represents a figure of merit representing the total dynamic error of the converter. Integral non-linearity will usually be the error which limits this number, as any harmonic spectral lines will rapidly degrade this number. However, this method of measurement insures that all potential sources of "spectral noise" have been accounted for, including potential oscillations of the reference, sub-harmonics of the clock frequency due to crosstalk, code dependent ground currents or any other error not related to absolute gain or offset. A SINAD of 47.1 dB at 1.12 MHz can be converted to 7.53 effective bits. The dominant error source is the two harmonic lines evident in the graph. Thus the integral linearity error at 1.12 MHz input can be seen to be better than 1/2 LSB.

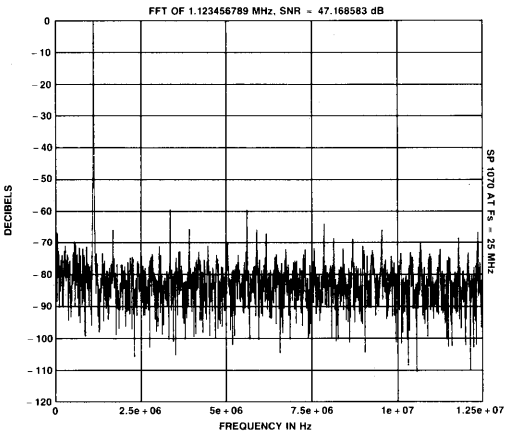
At 4.45 MHz input the FFT plot shows significant lines, aliased by the sampling process, at the second, third, fifth, seventh and ninth harmonics. While none of these harmonics are greater than 50 dB below the fundamental, the rms sum of these lines is primarily responsible for the SNR decrease from the ideal 49.96 dB to the 41.6 dB shown. The 4K point FFT's done here at Hybrid Systems are four times the length of those done by many manufacturers. This results in a plotted quantization noise floor 12 dB below that of other manufacturer's graphs. The advantage is that the cause of any SNR decrease can be identified — here the integral linearity of the amplifier/flash combination can be identified as the limiting factor to the SNR number. It can be said with confidence that no "spurious codes" or extremes in differential linearity error have raised the noise floor and limited the SNR measurement. Note that shorter length FFT's with the resulting raised plotted noise floor might not show these lines at all — they could be "buried" in the noise floor, and no such judgment would be possible.

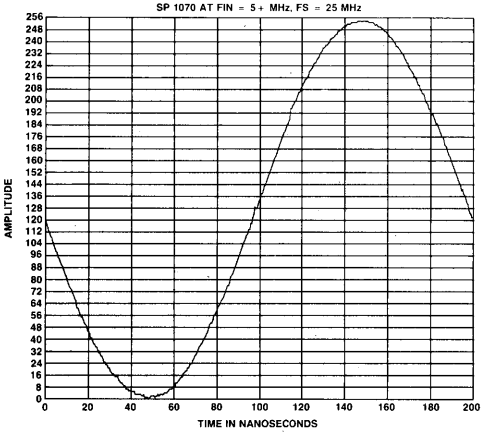
In addition, the SNR number as measured here at Hybrid is actually the average of 10 SNR computations. If a non-Gray scaled flash is run near its power bandwidth limit, a finite probability exists that the converter can "make a mistake" in assigning a binary number to a voltage which was rapidly changing. This "mistake" would show up on an FFT as the raised noise floor, as described above. By measuring the variation in the 10 SNRs which are averaged, it is possible to detect this kind of spurious code. The Gray scaled flash converters used in the SP 1070 do not exhibit this type of catastrophic error. Some degradation with increasing input slew rate is unavoidable — it can only be helped by the use of an extremely fast sample/hold in front of the analog input. However, the use of an internal Gray scale as a minimum distance code will have a useful effect upon the severity of any errors: even when the comparator determining the MSB is in error, the binary number which is output will be only a few LSB's away from the correct code. Thus the relative accuracy of the SP 1070 will be seen to degrade with increasing slew rate in a gradual and graceful manner — no "sparkle codes" will show up in the reconstructed video output, and at most the output will exhibit a dither-like noise, which the eye would average out if displayed upon a screen. The new problem is how to accurately specify the dynamic performance of such a device.

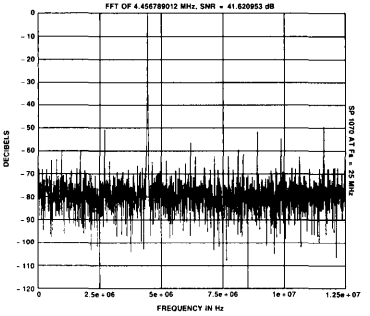
The dynamic testing and specifications of this part were designed to give a true indication of its performance. A new specification, dynamic differential linearity, is used to quantify the degradation in accuracy inherent in flash converters as the input signal slew rate is increased. It can be shown from histogram testing of Gray scale error-corrected flash converters, that the first DC specification which begins to get worse as input signal slew rate increases is the width of each code. Normally the code widths are measured with a DC voltage reference and are shown in units of differential linearity error, which is the difference, in fractional LSB's, of each code width from the ideal code width. Dynamic differential linearity error is a measure of the width of each code when a pure sine wave of known frequency and amplitude (and hence one of defined maximum slew rate) is applied to the flash converter.

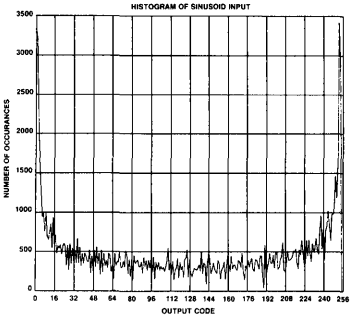
Histograms of pure sine waves are used to compute the code widths. Figure (C) shows the reconstruction of a sine wave of just over 5 MHz applied to the input of an SP 1070. Thirty buffers of 4K points each of these sine waves are stored, then used to generate the histogram of Figure (D). A curve fitting algorithm is then run to compute the "best fit ideal sinusoidal histogram" of Figure (E). The ideal histogram is used to calculate the number of times each code should have occurred. The number of actual occurrences of each code is ratioed to this ideal number. Codes which occurred fewer times than expected exhibited small code widths. The difference between the actual and the expected code widths can be normalized into units of differential linearity error in fractional LSB's. A plot of this "dynamic differential linearity error" is shown in Figures (F) and (G). The first was run with an extremely low frequency input, the second at 5+ MHz, and both were run at a sampling frequency of 25 MHz. An error of −1 LSB would indicate a missing code. Operation at lower sampling frequencies will yield even better dynamic differential linearity than the plots at 25 MHz show.

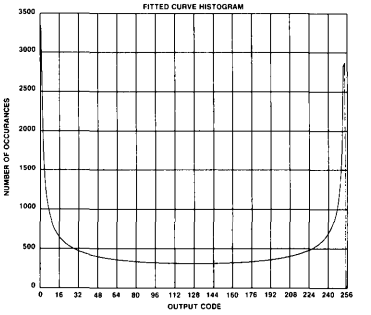
The specifications show an "input power bandwidth" number. This number is not related to the amplifier frequency response — typically the amplifier is only 2 dB down at 20 MHz fullscale inputs. What this number is meant to indicate is that for signals exhibiting slew rates equivalent to the slew rate of a fullscale input of this frequency (or lower), the code widths are guranteed to be greater than zero — no missing codes. Signals of greater slew rate may begin to show the effects of the Gray scale error minimization — appearing slightly noisy, especially near major transitions. If the application requires absolute fidelity in the reconstruction of fullscale signals of comparable slew rates, the use of a properly timed sample/hold in front of the analog input is recommended. An example would be where a system was attempting to demodulate a fullscale 10 MHz intermediate frequency. Note that most bandwidth limited signals, such as broadcast quality video, or signals limited by an external anti-aliasing filter, exhibit only small amounts of high frequency energy, and that 1/2 scale inputs at twice the 6 MHz input power bandwidth exhibit the same slew rate as fullscale inputs at 6 MHz, and are thus subject to only minimal degradation.

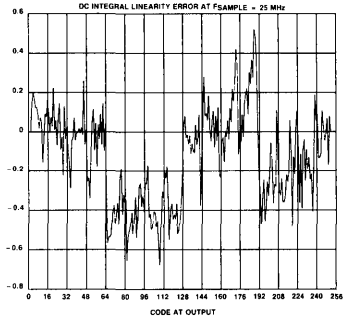


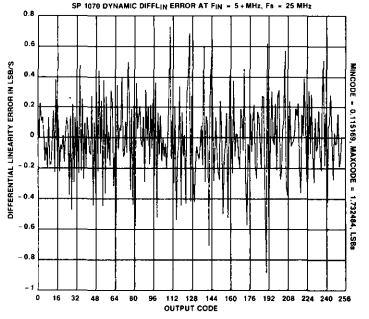


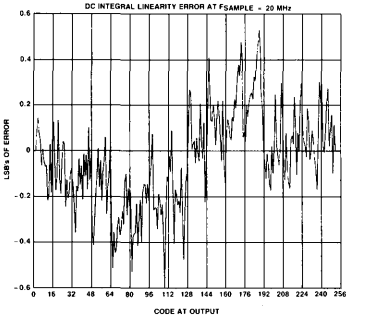

FFT OF 4.456789012 MHz, SNR = 41.620953 dB
DECIBELS
SP 1070 AT Fs = 25 MHz
FREQUENCY IN Hz

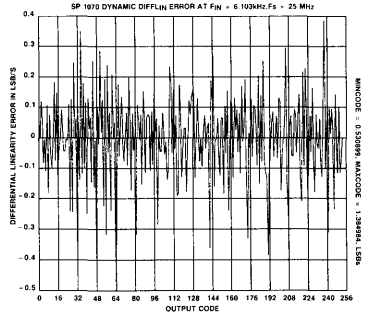

HISTOGRAM OF SINUSOID INPUT
NUMBER OF OCCURANCES
OUTPUT CODE

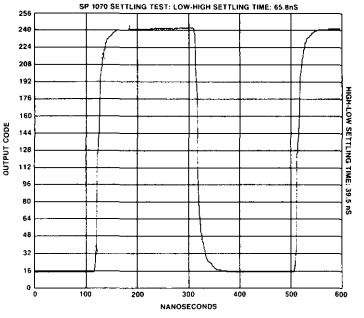

FITTED CURVE HISTOGRAM
NUMBER OF OCCURANCES
OUTPUT CODE


DC INTEGRAL LINEARITY ERROR AT FSAMPLE = 25 MHz
LSB's OF ERROR
CODE AT OUTPUT


SP 1070 DYNAMIC DIFFLIN ERROR AT FIN = 5 MHz, Fs = 25 MHz
DIFFERENTIAL LINEARITY ERROR IN LSB'S
MINCODE = 0.115169, MAXCODE = 1.732464 LSBs
OUTPUT CODE


DC INTEGRAL LINEARITY ERROR AT FSAMPLE = 20 MHz
LSB's OF ERROR
CODE AT OUTPUT


SP 1070 DYNAMIC DIFFLIN ERROR AT FIN = 6.103kHz,Fs = 25 MHz
DIFFERENTIAL LINEARITY ERROR IN LSB'S
MINCODE = 0.530096, MAXCODE = 1.394974 LSBs
OUTPUT CODE


SP 1070 SETTLING TEST: LOW-HIGH SETTLING TIME: 65.6nS
OUTPUT CODE
HIGH-LOW SETTLING TIME: 39.5 nS
NANOSECONDS

DUAL CHANNEL 8-BIT 25 MSPS A/D CONVERTER

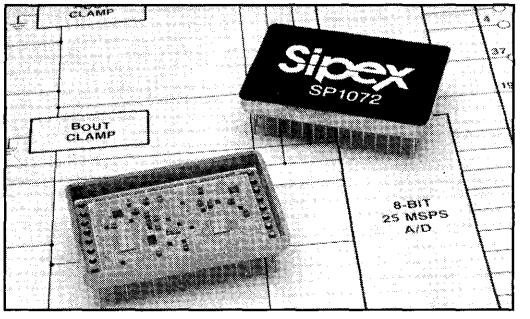
FEATURES

- Two 8-Bit 25 MHz Flash A/Ds in a Single Package
- Separate Input Buffer Amplifier and High Speed Limiter for Each Channel
- Internal Precision Voltage Reference

DESCRIPTION

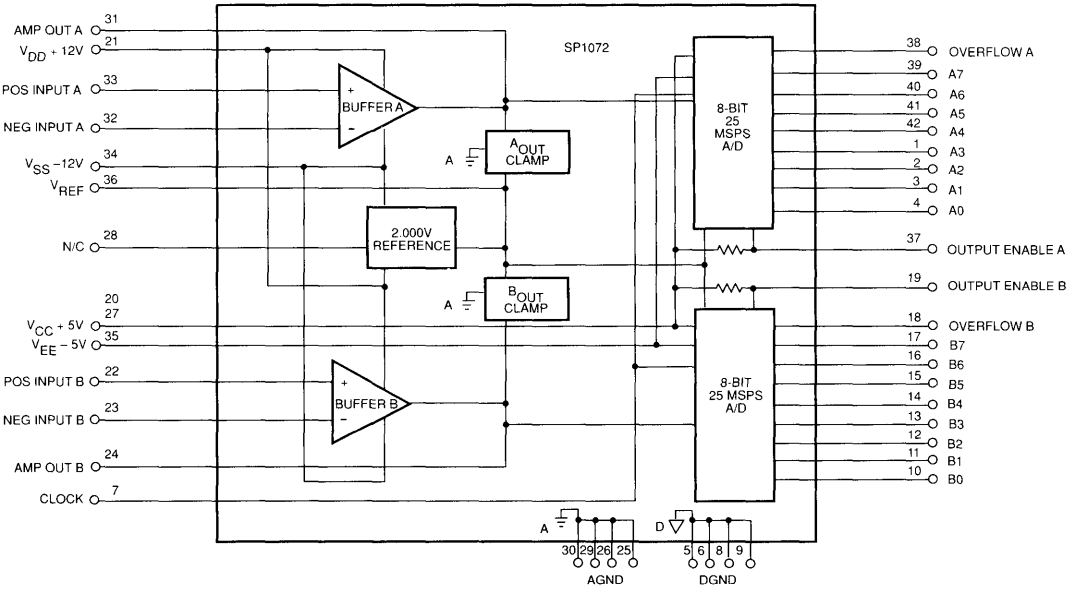
The SP1072 is a dual channel 8-Bit Flash A/D Converter with a common reference and clock input. Each channel has its own 25 MHz flash converter, input amplifier and high speed input limiter. The limiter protects the input of the flash converter from positive and negative overrange conditions. The input amplifier provides a low impedance source to the input of the flash and can be configured for different gains. Each converter has internal coding to minimize spurious codes thereby increasing the accuracy of the output code.

A precision voltage reference is common to both channels. The SP1072 is manufactured using low power bi-polar flash A/D's, and as a result, power consumption varies very little with increasing clock frequencies.



The SP1072 offers a significant savings in board space and analog design effort. Careful layout provides maximum interchannel isolation (-54 dB) while sampling time offset between channels is kept to a minimum (1 nsec). Packaged in a hermetic 42 pin package, operation over the full military temperature range (-55°C to +125°C) with full compliance to MIL-STD-883C is available.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage	V_{DD}	+15	V
	V_{SS}	-15	V
	V_{CC}	+7	V
	V_{EE}	-7	V
Digital Input Voltage	$V_{IN}(D)$	+7	V
Analog Input Voltage	$V_{IN}(A)$	±6	V
Junction Temperature	T_J	+150	°C
Operating Case Temperature	T_C	+135	°C
Storage Temperature	T_{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEMPERATURE RANGE -55°C to +125°C			UNITS
		MIN	TYP	MAX	
Supply Voltage	V_{DD}	+8	+12	+15	V
	V_{SS}	-8	-12	-15	V
	V_{CC}	+4.75	+5	+5.25	V
	V_{EE}	-3	-5	-6	V
Digital Input Voltage, HIGH	$V_{IN}(D)$	2.0			V
Digital Input Voltage, LOW				0.8	V
CONV Pulse Width, LOW	t_{PWL}	15			ns
CONV Pulse Width, HIGH	t_{PWH}	5			ns
Clock Frequency, Max	f_{CLK}			25	MHz
Operating Ambient Temperature	T_A	-55		+125	°C
Operating Case Temperature	T_C	-55		+125	°C

PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE -55°C to +125°C			UNITS
			MIN	TYP	MAX	
Resolution	N				8	Bits
Integral Linearity Error	E_{LI}	DC, Best Straight Line			±1	LSB
Differential Linearity Error	E_{DI}	DC			±1	LSB
No Missing Codes	NMC		8			Bits
RMS Signal/RMS Noise[1]	SNR	1.123 MHz Input	39.8	46		dB
+ Distortion		9.678 MHz Input		33		dB
Differential Phase	DP	F_S = 4 x NTSC Carrier		1		Degree
Differential Gain	DC	F_S = 4 x NTSC Carrier		1		%
Aperture Delay	E_{AP}			4		ns
Full Power Bandwidth	BW	No Spurious Code	7	11		MHz
Input Amplifier Bandwidth[2]	ABW	8 MHz	-3		0	dB
Settling Time (to 0.4%)	I_S	Full Scale Transition		50		ns
Delay Time (CH1-CH2)				1		ns
Overload Recovery	I_{REC}	±100 mV Overdrive		20		ns
Input Amplifier Noise		10 MHz Bandwidth		8.8		nV/√Hz
Cross Channel Isolation				-54		dB

SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE -55°C TO +125°C			UNITS
			MIN	TYP	MAX	
Maximum Conversion Rate	F_S	V_{CC}, V_{EE} = MIN	25			MHz
Sampling Time Offset	t_{STO}	V_{CC}, V_{EE} = MIN		4.0	8.5	ns
Digital Output Delay	t_D	V_{CC} = MIN		19		ns
Digital Output Enable	t_{PZL}	V_{CC} = MIN		27		ns
Digital Output Disable	t_{PHZ}	V_{CC} = MIN		18		ns
Full Scale Flag	t_{CFSL}	V_{CC} = MIN		19		ns
CONV Pulse Width, LOW	t_{PWL}	V_{CC} = MIN	15	20		ns
CONV Pulse Width, HIGH	t_{PWH}	V_{CC} = MIN	5	20		ns

INPUTS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE -55°C TO +125°C			UNITS
			MIN	TYP	MAX	
Input Current, Logic LOW	I_{IL}					
		OE	-400	-100		µA
		CONV	-800	-160		µA
Input Current, Logic HIGH	I_{IH}					A
		OE		-400	-100	µA
		CONV	-200	-40		µA
Input Voltage, Logic LOW	V_{IL}				0.8	V
Input Voltage, Logic HIGH	V_{IH}		2.0			V
Analog Input Capacitance	C_{IN}					
Inverting Input				1.0		pf
Non-Inverting Input				1.0		pf
Offset Voltage	V_{OFF}				13	mV
Offset Voltage Drift	V_{OFF} TC			20		V/°C
Bias Current				8	25	µA
Offset Current					8	µA
Open Loop Gain				5000		V/V
CMRR			60			dB
Gain Bandwidth Product				400		MHz

DIGITAL OUTPUTS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Leakage Current	I_{LEAK}	Output High Z	-50		+50	µA
Output Voltage, Logic LOW	V_{OL}	I_{OL} = 4 mA			0.4	V
Output Voltage, Logic HIGH	V_{OH}	I_{OH} = 100 µA	2.4			V

REFERENCE

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE -55°C TO +125°C			UNITS
			MIN	TYP	MAX	
Reference Voltage	V_{REF}	V_{REF} OUT	1.992	2.0	2.008	V
Reference Current, Sourced					2.0	mA

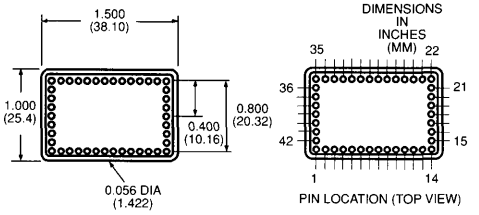
POWER SUPPLIES

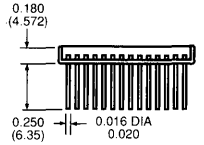
PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE -55°C TO +125°C			UNITS
			MIN	TYP	MAX	
Supply Current	I_{DD}[3]	+12V		80	110	mA
	I_{SS}[3]	-12V		-40	-90	mA
	I_{CC}	+5V		225	250	mA
	I_{EE}	-5V		-20	-40	mA
Power Dissipation	P_D	V_{CC} = MAX, V_{EE} = MAX Dynamic		2.6	3.8	W

NOTES

1. SNR = Signal/Noise + Distortion, f_{SAMPLE} = 20 MHz.
2. Internal amplifier connected with R_{IN} = 604Ω, R_F = 1.21 KΩ, R_{NG} = 97.6Ω.
3. For ±5V operation contact the factory.

PACKAGE OUTLINE





ODERING INFORMATION

MODEL	TEMPERATURE RANGE	DESCRIPTION
SP1072B	-55°C to +125°C	Dual 8-Bit, 25 MHz ADC MIL-STD-883C Screening

PIN ASSIGNMENTS

PIN	SYMBOL	FUNCTION
1	A3	Data Bit 3 Flash A
2	A2	Data Bit 2 Flash A
3	A1	Data Bit 1 Flash A
4	A0	Data Bit 0 Flash A
5	DGND	Digital Ground
6	DGND	Digital Ground
7	CLOCK	Clock Input
8	DGND	Digital Ground
9	DGND	Digital Ground
10	B0	Data Bit 0 Flash B
11	B1	Data Bit 1 Flash B
12	B2	Data Bit 2 Flash B
13	B3	Data Bit 3 Flash B
14	B4	Data Bit 4 Flash B
15	B5	Data Bit 5 Flash B
16	B6	Data Bit 6 Flash B
17	B7	Data Bit 7 Flash B
18	OVERFLOW B	Overflow Flash B
19	OUTPUT ENABLE B	Output Enable Flash B
20	V_{CC}	Positive Supply +5V
21	V_{DD}	Positive Supply +12V
22	POS INPUT B	Positive Input Buffer Amp B
23	NEG INPUT B	Negative Input Buffer Amp B
24	AMP OUT B	Buffer Amp B Output
25	AGND	Analog Ground
26	AGND	Analog Ground
27	V_{CC}	Positive Supply +5V
28	N/C	No Connect
29	AGND	Analog Ground
30	AGND	Analog Ground
31	AMP OUT A	Buffer Amp A Output
32	NEG INPUT A	Negative Input Buffer Amp A
33	POS INPUT A	Positive Input Buffer Amp A
34	V_{SS}	Negative Supply -12V
35	V_{EE}	Negative Supply -5V
36	V_{REF}	Voltage Reference Output
37	OUTPUT ENABLE A	Output Enable Flash A
38	OVERFLOW A	Overflow Flash A
39	A7	Data Bit 7 Flash A
40	A6	Data Bit 6 Flash A
41	A5	Data Bit 5 Flash A
42	A4	Data Bit 4 Flash A

APPLICATIONS INFORMATION

THEORY OF OPERATION

ANALOG INPUTS

The input amplifiers are uncommitted op amps, and inverting or non-inverting connections may be used. The recommended Feedback resistance is from 1K to 2K ohms. The minimum noise gain should be 10 for optimum response. The amplifier output must go from nominal voltages of 0 Volts for the low end of the scale and +2 Volts for full scale. See figure 1 below.

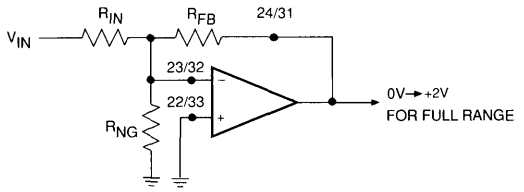


FIGURE 1

$$\frac{R_{FB}}{R_{IN}} = \frac{2\,V}{FSR\ Volts} \quad \text{i.e. if } R_{FB} = 1\ K\Omega \text{ \& FSR} = 1\ V \text{ then } \frac{R_{FB}}{R_{IN}} = 2, R_{IN} = .5\ K\Omega$$

$$R_{NG_{MAX}} = \frac{1}{\frac{9}{R_{FB}} - \frac{1}{R_{IN}}} \quad \text{i.e. if } R_{FB} = 1\ K\Omega \text{ \& } R_{IN} = .5\ K\Omega \text{ then } R_{NG_{MAX}} = 142.8\Omega$$

A bipolar input can be accommodated by using another amplifier in conjunction with the internal reference. This is accomplished by placing a voltage equal to half scale on the negative input of the input amplifier (pin 23 or pin 32). In the example below the reference voltage (+2V) is shifted to -10 Volts and then attenuated by a factor of 10 to -1V, which is one-half of full scale. This is accomplished by amplifying the reference by -5 and attenuating the output by 10 which is makes the attenuation resistor 10 times the R_{FB}. This resistor should be high impedence to minimize its effect on the input amplifier, furthermore, the offsetting amplifier should be selected for good DC stability over temperature.

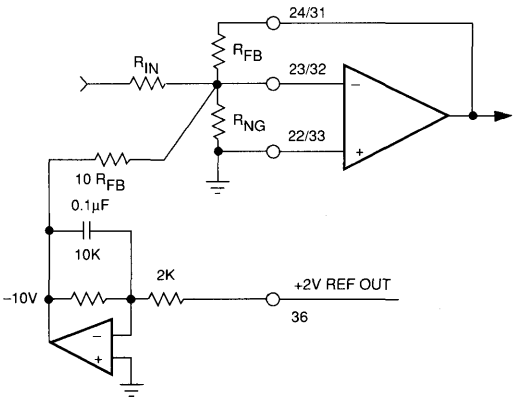


FIGURE 2
TYPICAL BIPOLAR CONNECTIONS

CLOCKS

The clock input can easily be increased from the 20 MHz frequency that is used for dynamic testing of the hybrid. Although higher clock frequencies have been used, 25 MHz should be used as a practical limit. The circuitry layout considerations are extensive at 20 MHz and become even more critical at higher clock frequencies. When the clock frequency is raised the di/dt noise present on the 5 Volt supplies increase and become more difficult to filter. The clock input is TTL compatible and since the clock is common to both channels it appears as two parallel TTL gates. The analog input is digitized just prior to the falling edge of the clock signal and is latched from the same falling edge to the next rising edge of the clock input signal.

ENABLE INPUTS

Enable inputs are TTL compatible and cause the data outputs of the flash to change from a high impedance to an active state when brought to a logic "1" level. These inputs only control the output data latches and do not disable the overrange output pins. Although these inputs do not reduce the power consumed by the flash converters, they also don't cause spurious output codes when toggled. The enable pins are resistively coupled to a logic level "1" in order to provide a known operating condition in the event of these pins becoming intermittent or left unconnected.

POWER SUPPLIES

Power supplies will consist of both analog and digital supplies. V_{DD}(+12V) and V_{SS}(-12V) will be considered as the analog supplies while V_{CC}(+5V) and V_{SS}(-5V) will be referred to as the digital supplies. Each supply should be bypassed with both a 10µF tantalum and a 0.1µF multi-layer ceramic capacitor to their respective grounds. The ceramic capacitor should be as close to the pins of the hybrid as possible. The values and the quantities of the bypass capacitors can be increased so long as they provide low inductance characteristics for a wide range of frequencies.

GROUNDING

Grounding has a large impact on the performance of flash converters since they have a high conversion rate and a 1/2LSB is less than 4 mV. Steps have been taken in the design of this device to make sure that the series ground impedance for the references is less than 200 mΩ for all frequencies up to 30 MHz. This is one example of how sensitive the grounds and the supplies can be to either series resistance or inductance. The device has both analog and digital ground pins available to the user. It is recommended that these grounds be tied together in order to provide a "MECCA Ground." The user may want to keep the grounds separated. It should be noted that the case of the hybrid is connected to the analog ground.

CALIBRATION

The SP1072 can be easily calibrated for offset and gain errors. This calibration is accomplished by external potentiometers set up in conjunction with the resistors used to set up the uncommitted internal amplifier (see Analog Inputs). The SP1072 connection diagram below shows all connections to make the SP1072 function including offset and gain calibration circuitry.

The gain error is adjusted through use of a potentiometer in series with R_{IN}. The potentiometer should be chosen so that it is less than 10% of R_{IN}, futhermore, R_{IN} should be adjusted downward by one-half the value of the potentiometer in order to provide both positive and negative trim range.

The offset error is trimmed by placing a small voltage on the positive terminal of the input amplifier (pin 22 or pin 33), by using a divider in conjunction with a potentiometer. A bipolar voltage is developed by using a 50 KΩ potentiometer between the ±12V supplies. This voltage is then attenuated by a factor of 500 to develop a small offsetting voltage to null the offset error of the amplifier. Furthermore, a .01µF capacitor should be added on the positive terminal for bypassing. See figure 3.

An example of the bipolar connection is shown on channel two of the SP1072 connection diagram. The bipolar offset is accomplished by placing a potentiometer in series with the reference voltage which is 10% of the input resistor to the offset amplifier. The resistor should be decreased by one-half the value of the potentiometer similar to the gain trim. See figure 4.

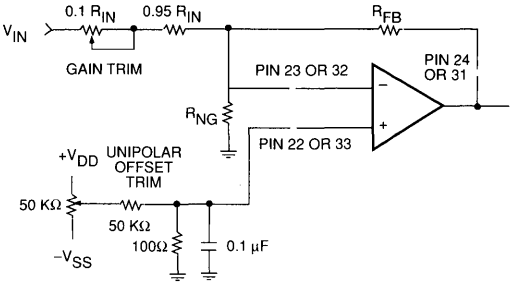


FIGURE 3
SP1072 GAIN TRIM AND UNIPOLAR OFFSET TRIM

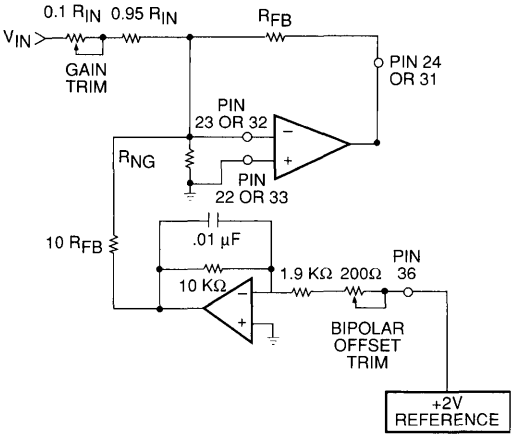
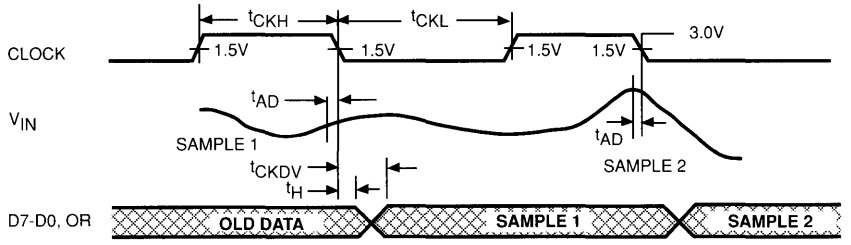


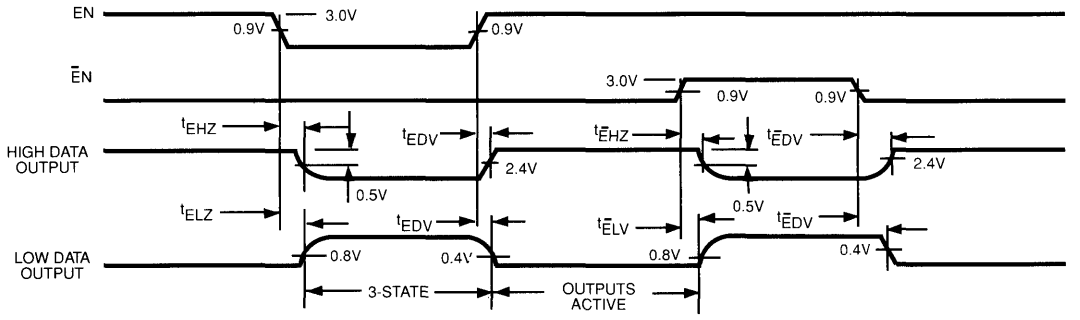
FIGURE 4
SP1072 GAIN TRIM AND BIPOLAR OFFSET TRIM

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = +5.0V, V_{EE} = 5.2V. See System Timing Diagram.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
INPUTS					
Min Clock Pulse Width — High	t_{CKH}	5	20	—	ns
Min Clock Pulse Width — Low	t_{CKL}	15	20	—	ns
Max Clock Rise, Fall Time	$t_{R,F}$	—	100	—	ns
Clock Frequency	t_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	—	19	—	ns
Aperture Delay	t_{AD}	—	4.0	—	ns
Hold Time	t_H	—	6.0	—	ns
Data High to 3-State from Enable Low	t_{EHZ}	—	27	—	ns
Data Low to 3-State from Enable Low	t_{ELZ}	—	18	—	ns
Data High to 3-State from Enable High	t_{EHZ}	—	32	—	ns
Data Low to 3-State from Enable High	t_{ELZ}	—	18	—	ns
Valid Data from Enable High (Pin 20 = 0V)	t_{EDV}	—	15	—	ns
Valid Data from Enable Low (Pin 19 = 5.0V)	t_{EDV}	—	16	—	ns
Output Transition Time (10%-90%)	t_{tr}	—	8.0	—	ns



t_{CKDV} and t_H measured at output levels of 0.8 and 2.4 volts.



SYSTEM TIMING DIAGRAMS

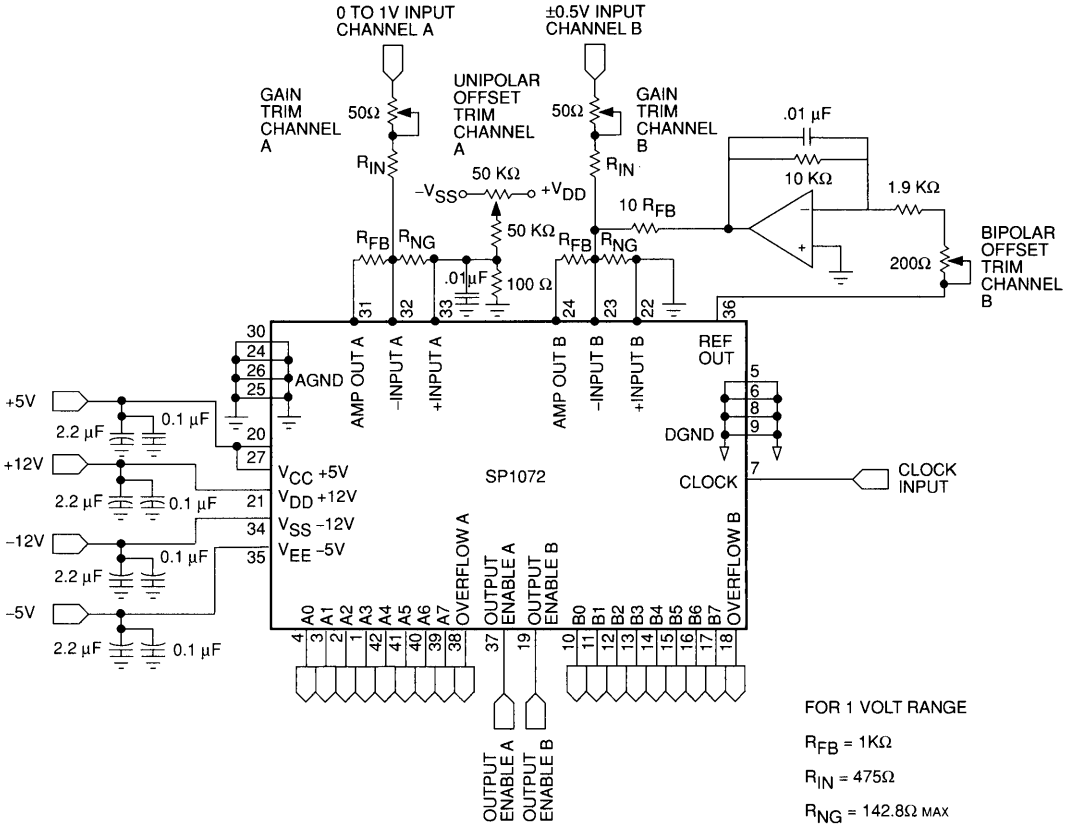


FIGURE 5
SP1072 CONNECTION DIAGRAM
CHANNEL A 0 TO 1V INPUT
CHANNEL B ±0.5V INPUT

DYNAMIC TESTING OF THE SP1072

The SP1072 has been designed and characterized upon a high speed dynamic test system. Its wide bandwidth amplifier and Gray scale encoded flash converter provide excellent dynamic performance at sampling frequencies to 25 MHz.

All dynamic performance characteristics as well as all DC trimming and linearity specifications are 100% tested at a sample rate of 20 MHz. Note that the DC linearity specifications become even better as the sample rate is lowered. SP1072 "B" grade parts are tested at 20 MHz over the full military temperature range. The parts are also characterized here at room temperature at 25 MHz.

Graphs 1 and 2 show an FFT and a signal-to-noise + distortion number at each frequency input. Any harmonics of the fundamental which show in the graphs are due to integral nonlinearity in either the input amplifier or the flash converter transfer curve. Any noise in the hybrid or any dynamic differential linearity errors will raise the noise floor of the graph above that generated by 8-Bit quantization noise floor of an ideal converter. Note that higher order harmonics will alias back down into the FFT spectrums shown. The SNR number as defined here represents a figure of merit representing the total dynamic error of the converter. Integral non-linearity will usually be the error which limits this number, as any harmonic spectral lines will rapidly degrade this number. However, this method of measurement insures that all potential sources of "spectral noise" have been accounted for, incuding potential oscillations of the reference, sub-harmonics of the clock frequency due to crosstalk, code dependent ground currents or any other error not related to absolute gain or offset. A SINAD of 47.1 dB at 1.12 MHz can be converted to 7.53 effective bits. The dominant error source is the two harmonic lines evident in the graph. Thus the integral linearity error at 1.12 MHz input can be seen to be better than 1/2 LSB.

At 4.45 MHz input the FFT plot shows significant lines, aliased by the sampling process, at the second, third, fifth, seventh and ninth harmonics. While none of these harmonics are greater than 50 dB below the fundamental, the rms sum of these lines is primarily responsible for the SNR decrease from the ideal 49.96 dB to the 41.6 dB shown. The 4K point FFT's done here at Sipex are four times the length of tho se done by many manufacturers. This results in a plotted quantization noise floor 12 dB below that of other manufacturer's graphs. The advantage is that the cause of any SNR decrease can be identified — here the integral linearity of the amplifier/flash combination can be identified as the limiting factor to the SNR number. It can be said with confidence that no "spurious codes" or extremes in differential linearity error have raised the noise floor and limited the SNR measurement. Note that shorter length FFT's with the resulting raised plotted noise floor might not show these lines at all — they could be "buried" in the noise floor, and no such judgment would be possible.

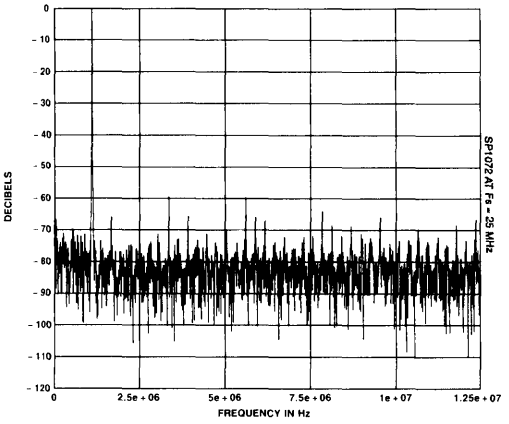
In addition, the SNR number as measured is actually the average of 10 SNR computations. If a non-Gray scaled flash is run near its power bandwidth limit, a finite probability exists that the converter can "make a mistake" in assigning a binary number to a voltage which was rapidly changing. This "mistake" would show up on an FFT as the raised noise floor, as described above. By measuring the variation in the 10 SNRs which are averaged, it is possible to detect this kind of spurious code. The Gray scaled flash converters used in the SP1072 do not exhibit this type of catastrophic error. Some degradation with increasing input slew rate is unavoidable — it can only be helped by the use of an extremely fast sample/hold in front of the analog input. However, the use of an internal Gray scale as a minimum distance code will have a useful effect upon the severity of any errors; even when the comparator determining the MSB is in error, the binary number which is output will be only a few LSB's away from the correct code. Thus the relative accuracy of the SP1072 will be seen to degrade with increasing slew rate in a gradual and graceful manner — no "sparkle codes" will show up in the reconstructed video output, and at most the output will exhibit a dither-like noise, which the eye would average out if displayed upon a screen. The new problem is how to accurately specify the dynamic performance of such a device.

The dynamic testing and specifications of this part were designed to give a true indication of its performance. Dynamic differential linearity is used to quantify the degradation in accuracy inherent in flash converters as the input signal slew rate is increased. It can be shown from histogram testing of Gray scale error-corrected flash converters, that the first DC specification which begins to get worse as input signal slew rate increases is the width of each code. Normally the code widths are measured with a DC voltage reference and are shown in units of differential linearity error, which is the difference, in fractional LSB's, of each code width from the ideal code width. Dynamic differential linearity error is a measure of the width of each code when a pure sine wave of known frequency and amplitude (and hence one of defined maximum slew rate) is applied to the flash converter.

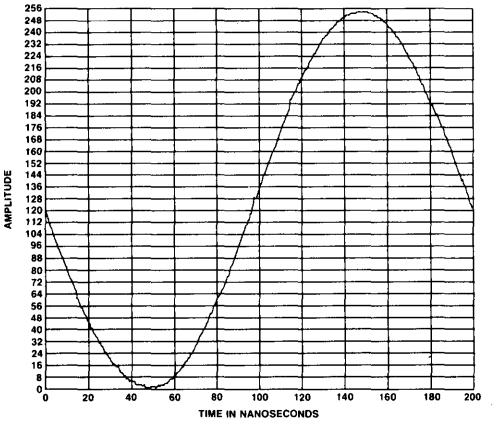
Histograms of pure sine waves are used to compute the code widths. Graph 3 shows the reconstruction of a sine wave of just over 5 MHz applied to the input of an SP1072. Thirty buffers of 4K points each of these sine waves are stored, then used to generate the histogram of Graph 4. A curve fitting algorithm is then run to compute the "best fit ideal sinusoidal histogram" of Graph 5. The ideal histogram is used to calculate the number of times each code should have occurred. The number of actual occurrences of each code is ratioed to this ideal number. Codes which occurred fewer times than expected exhibited small code widths. The difference between the actual and the expected code

widths can be normalized into units of differential linearity error in fractional LSB's. A plot of this "dynamic differential linearity error" is shown in Graphs 7 and 9. Graph 9 was run with an extremely low frequency input, Graph 7 at 5 + MHz, and both were run at a sampling frequency of 25 MHz. An error of -1 LSB would indicate a missing code. Operation at lower sampling frequencies will yield even better dynamic differential linearity than the plots at 25 MHz show.

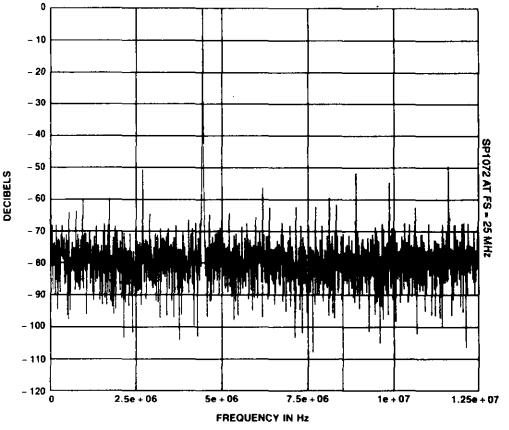
The specifications show an "input power bandwidth" number. This number is not related to the amplifier frequency response — typically the amplifier is only 2 dB down at 20 MHz fullscale inputs. What this number is meant to indicate is that for signals exhibiting slew rates equivalent to the slew rate of a fullscale input of this frequency (or lower), the code widths are guranteed to be greater than zero — no missing codes. Signals of greater slew rate may begin to show the effects of the Gray scale error minimization — appearing slightly noisy, especially near major transitions. If the application requires absolute fidelity in the reconstruction of fullscale signals of comparable slew rates, the use of a properly timed sample/hold in front of the analog input is recommended. An example would be where a system was attempting to demodulate a fullscale 10 MHz intermediate frequency. Note that most bandwidth limited signals, such as broadcast quality video, or signals limited by an external antialiasing filter, exhibit only small amounts of high frequency energy, and that 1/2 scale inputs at twice the 6 MHz input power bandwidth exhibit the same slew rate as fullscale inputs at 6 MHz, and are thus subject to only minimal degradation.



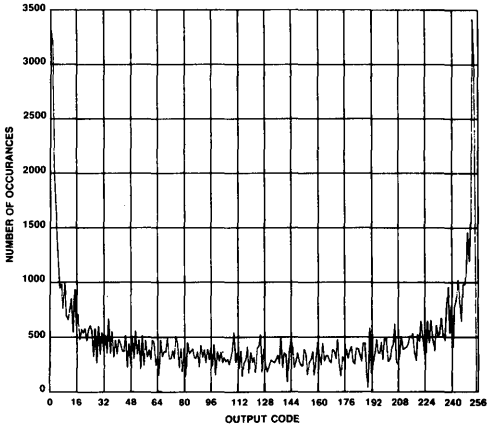
Graph 1. FFT of 1.23456789 MHz, SNR = 47.168583 dB



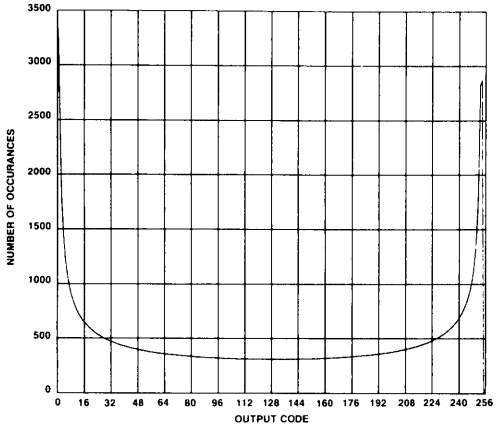
Graph 2. FFT of 4.456789012 MHz, SNR = 41.620953 dB



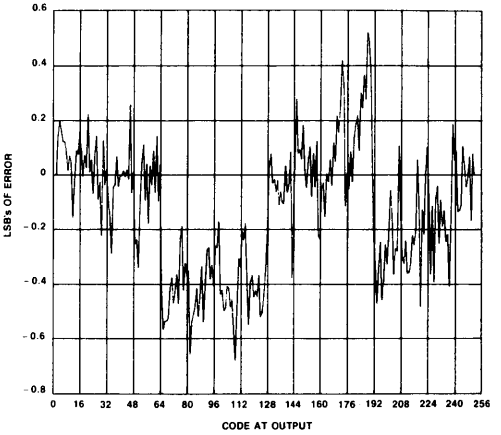
Graph 3. SP1072 at F_{in} = 5+ MHz, FS = 25 MHz



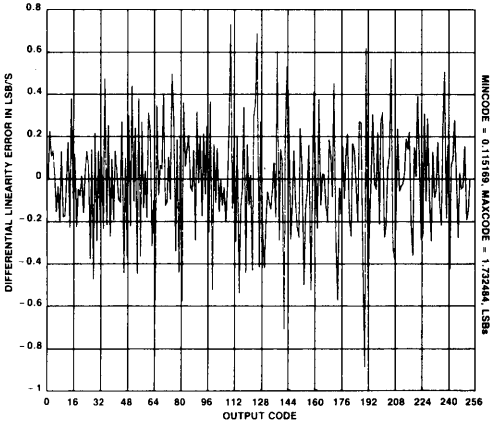
Graph 4. Histogram of Sinusoid Input



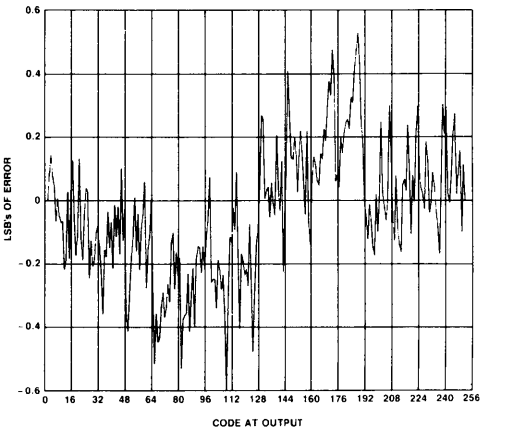
Graph 5. Fitted Curve Histogram



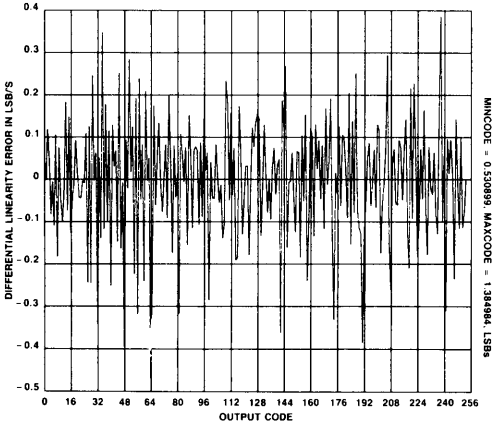
Graph 6. Dc Integral Linearity Error at F_{Sample} = 25 MHz



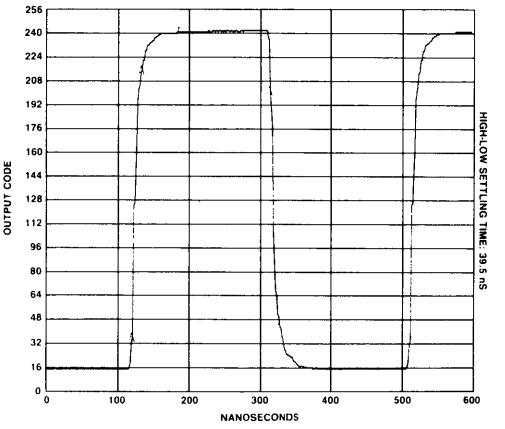
Graph 7. SP1072 Dynamic $Diffl_{in}$ Error at F_{in} = 5+ MHz, Fs = 25 MHz



Graph 8. Dc Integral Linearity Error at F_{Sample} = 20 MHz



Graph 9. SP1072 Dynamic $Diffl_{in}$ Error at F_{in} = 6.103 kHz, Fs = 25 MHz



Graph 10. SP1072 Settling Test: Low-High Settling Time: 65.8 ns

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Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

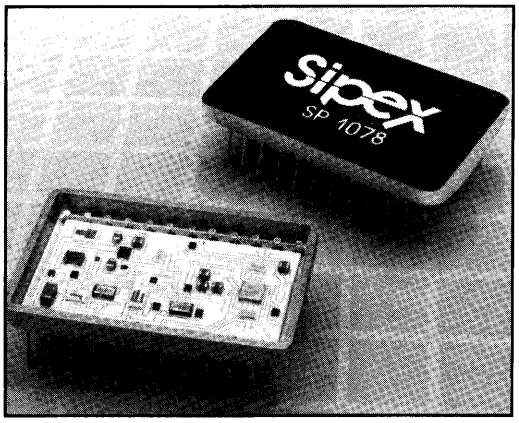
8-BIT 50 MSPS A/D CONVERTER

FEATURES

- Complete Analog Front-end and ADC in a single package
- DC to 50 MHz sampling rate
- Selectable amplifier modes and input ranges
- Precision 2.5 volt reference for external applications
- Summing node available for external offset/gain adjustment
- Three-state TTL outputs
- Minimal 15ns latency
- Binary or two's complement coding
- Half the power at twice the sampling rate of competing parts.

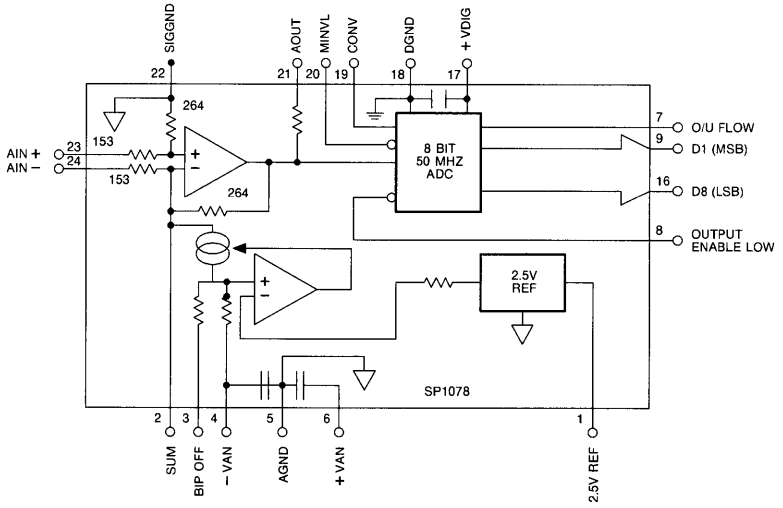
DESCRIPTION

The SP1078 is a complete flash analog to digital conversion subsystem capable of converting high speed analog signals into 8-bit digital words at up to 50 megasamples per second. It contains a wide-band current feedback amplifier, a precision 2.5 volt reference, and a 50 msps flash converter featuring 3 stateable series-terminated TTL outputs and an out-of-range indicator. The input amplifier may be run in the inverting, non-inverting or differential modes. Pin strap selection provides a choice of unipolar or bipolar input range, independent of the amplifier mode. The circuit draws less than 570 mW from +5, -5.2 volt supplies.



The combination of support circuitry and converter within one 24-pin package offers significant savings of board space. Other benefits include savings in component, assembly and design costs.

Designed to meet military applications, the SP 1078 is housed in a hermetic 24-pin double DIP and operates with guaranteed performance over the full -55°C to +125°C temperature range. Processing in compliance with MIL-STD-883C is available.



SP1078C and SP1078B SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage:	V_{CC}	7.0	V
	$+V_{AN}$	7.0	V
	$-V_{AN}$	-7.0	V
Vdifference	$V_{CC} - (+V_{AN})$	+/-0.5	V
Gdifference	$A_{GND} - D_{GND}$	+/-1.0	V
Digital Vin	$V_{IN}(D)$	5.5	V
	$V_{IN}(D)$	-0.6	V
Analog Vin	V(Ain)	+Van + 0.6	V
		-Van - 0.6	V
Junction Temp	Tj	150	°C
Storage Temp	Ts	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS:

PARAMETER	SYMBOL	TEMPERATURE RANGE						UNITS
		TYP 25°C	SP1078C 0° to 70°C MIN	SP1078C 0° to 70°C MAX	TYP 25°C	SP1078B -55° to 125°C MIN	SP1078B -55° to 125°C MAX	
Digital Supply Voltage	V_{CC}	5.0	4.75	5.25	5.0	4.75	5.25	V
Positive Analog Supply	$+V_{AN}$	5.0	4.75	5.25	5.0	4.75	5.25	V
Negative Analog Supply	-Van	-5.2	-4.9	-5.5	-5.2	-4.9	-5.5	V
Gdifference	$(A_{GD} - D_{GD})$	0.0			0.0			V
Analog Range	A_{IN}	1.0			1.0			V_{P-P}
Conv Pulse LOW	t_{PWL}	50%	8	—	50%	8	—	nS
Conv Pulse HI	t_{PWH}	50%	8	—	50%	8	—	nS
Clock Freq	f_{CLK}	—	0	50	—	0	40	MHz
Ambient Temp	t_{AMB}	25	0	70	25	—	—	°C
Case Temp	t_{CASE}	25	—	—	25	-55	125	°C

PERFORMANCE CHARACTERISTICS:

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			TYP 25°C	0°C to 70°C MIN	0°C to 70°C MAX	TYP 25°C	-55°C to 125°C MIN	-55°C to 125°C MAX	
Resolution	N	(F_S = 20 MHz)			8			8	Bits
Integral Linearity Error	E_{LI}	DC, Best St. Line	+/-0.6	—	+/-1.0	+/-0.6	—	+/-1.0	LSB
Differential Linearity Error	E_{LD}	DC	+/-0.4	—	+/-0.75	+/-0.35	—	+/-0.6	LSB
Dynamic Differential Error	E_{DD}	5 MHz Input	+/-0.6	—	—	+/-0.5	—	—	LSB
	E_{DD}	8.1 MHz Input	+.95, -.8	—	No Missing	+/-0.6	—	No Missing	LSB
Signal-to-Noise + Distortion	SINAD	1.123 MHz	47	44	—	47	44	—	dBc
		2.234 MHz	46	—	—	46	—	—	dBc
		4.456 MHz	45	—	—	45	—	—	dBc
		8.1 MHz	43	39	—	43	40	—	dBc
		(F_S = 50 MHz)							
Differential Linearity Error	E_{LD}	DC	+/-0.5	—	—	+/-0.4	—	—	LSB
Dynamic Differential Error	E_{DD}	5 MHz Input	+/-0.75	—	—	+/-0.6	—	—	LSB
	E_{DD}	10 MHz Input	No Missing	—	—	No Missing	—	—	LSB
Signal-to-Noise + Distortion	SINAD	1.123 MHz	46	—	—	46	—	—	dBc
		2.234 MHz	45	—	—	45	—	—	dBc
		4.456 MHz	44	—	—	44	—	—	dBc
		9.768 MHz	39	—	—	40	—	—	dBc
Aperture Jitter	E_{AP}		50			50			pS
Full Power Bandwidth	BW	No Spurious Code	10	10	—	12	8	—	MHz
Ampifier F.P. Bandwidth	ABW	Freq -3 dB	50	—	—	50	—	—	MHz
Settling Time	t_S	FS Xisition	18	—	—	18	—	—	nS
Rise/Fall	t_R	FS Xisition	4	—	—	4	—	—	nS
Overload Recovery	t_{REC}	100% Overdrive	5	—	—	5	—	—	nS
Input Noise	AN	10 MHz Bandwidth	125	—	—	125	—	—	µVRMS

SWITCHING CHARACTERISTICS:

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			TYP 25°C	SP1078C 0°C to 70°C MIN	SP1078C 0°C to 70°C MAX	TYP 25°C	SP1078B -55°C to 125°C MIN	SP1078B -55°C to 125°C MAX	
Fsample	F_S	$V_{CC} = V_{EE} = MIN$	60	50	—	60	40	—	MHz
Sampling Time Offset	t_{STO}	$V_{CC} = V_{EE} = MIN$	2	—	—	2	—	—	nS
Digital Delay	t_D	$V_{CC} = V_{EE} = MIN$	15	—	18	15	—	18	nS
Digital Hold	t_H	$V_{CC} = V_{EE} = MIN$	7	6	—	7	6	—	nS
Digital Enable	t_{PZL} t_{PZH}	$V_{CC} = V_{EE} = MIN$ $V_{CC} = V_{EE} = MIN$	18 23	— —	24 29	18 23	— —	24 29	nS nS
Digital Disable	t_{PLZ} t_{PHZ}	$V_{CC} = V_{EE} = MIN$ $V_{CC} = V_{EE} = MIN$	10 18	— —	16 24	10 18	— —	16 24	nS nS
CONV LOW	t_{PWL}	$V_{CC} = V_{EE} = MIN$	—	8	—	—	8	—	nS
CONV HIGH	t_{PWH}	$V_{CC} = V_{EE} = MIN$	—	8	—	—	8	—	nS

INPUTS:

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			TYP 25°C	0°C to 70°C MIN	0°C to 70°C MAX	TYP 25°C	-55°C to 125°C MIN	-55°C to 125°C MAX	
Input Current, Logic LOW (*Note 1)	I_{IL}	OEL = 0.4V	—	—	-0.4	—	—	-0.4	mA
		MINVL = 0.4V	-1.3	—	-1.5	-1.3	—	--1.5	mA
		CONV = 0.4V	—	—	-0.4	—	—	-0.4	mA
Input Current, Logic HIGH	I_{IH}	OEL = 2.7V	—	—	20	—	—	20	μA
		MINVL = Vdig	0	—	0	0	—	0	μA
		MINVL = 2.7V	-0.4	—	-0.6	-0.4	—	-0.6	mA
		CONV = 2.7V	—	—	100	—	—	100	μA
Clock Input Resistance	R_{INC}	CONV	4	—	—	4	—	—	kOhm
Input Voltage, Logic LOW	V_{IL}	OEL, MINVL	—	0	0.8	—	0	0.8	V
		CONV	—	0	0.8	—	0	0.8	V
Input Voltage, Logic HIGH	V_{IN}	OEL, MINVL	—	2.0	V_{DIG}	—	2.0	V_{DIG}	V
		CONV	—	2.0	2.7	—	2.0	2.7	V
Analog Input Resistance	R_{IN}	A_{IN}^+	417	—	—	417	—	—	Ohms
		A_{IN}^-	153	—	—	153	—	—	Ohms
Analog Input Capacitance	C_{IN}	A_{IN}^+, A_{IN}^-	3	—	—	3	—	—	pF
Gain Error	E_G	Endpoints	+/-0.2	—	—	+/-0.1	—	—	%
Offset Error	E_{OU}	Unipolar	+/-0.5	—	—	+/-0.4	—	—	LSB
	E_{OB}	Bipolar	+/-0.6	—	—	+/-0.5	—	—	LSB
Offset Tempco	T_{CU}	Unipolar	+/-0.015	—	—	+/-0.007	—		LSB/°C
	T_{CB}	Bipolar	+/-0.015	—	—	+/-0.007	—		LSB/°C

*Note 1: MINVL is internally tied to V_{DIG} through a 5 kOhm nominal resistor and can be left unconnected for binary coded operation or tied to ground for 2's complement operation.

DIGITAL OUTPUTS:

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			TYP 25°C	0°C to 70°C MIN	0°C to 70°C MAX	TYP 25°C	-55°C to 125°C MIN	-55°C to 125°C MAX	
Output Leakage Current, Logic LOW	I_{LOL}	$V_O = 0.4V$	—	—	-30	—	—	-30	μA
Output Leakage Current, Logic HIGH	I_{LOH}	$V_O = 2.4V$	—	—	30	—	—	30	μA
Output Voltage, Logic LOW	V_{OL}	$I_{OL} = 1$ mA	0.4	—	0.45	0.4	—	0.45	V
Output Voltage, Logic HIGH	V_{OH}	$I_{OH} = -.4$ mA	—	2.6	—	—	2.6	—	V

REFERENCE:

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			TYP 25°C	0°C to 70°C MIN	0°C to 70°C MAX	TYP 25°C	-55°C to 125°C MIN	-55°C to 125°C MAX	
Reference Voltage	V_{REF}		2.500	2.49	2.51	2.500	2.49	2.51	V
Reference Current	I_{REF}	Sourced	2	2	—	2	2	—	mA

POWER SUPPLIES:

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			TYP 25°C	0°C to 70°C MIN	0°C to 70°C MAX	TYP 25°C	-55°C to 125°C MIN	-55°C to 125°C MAX	
V_{DIG} Current	I_{DIG}	V_{DIG} = MAX	30	—	—	30	—	—	mA
$+V_{AN}$ Current	$+I_{AN}$	$+V_{AN}$ = MAX	56	—	—	56	—	—	mA
$-V_{AN}$ Current	$-I_{AN}$	$-V_{AN}$ = MAX	20	—	—	20	—	—	mA
Power Dissipation	P_D	MAX Supplies, (F_S = 50 MHz)	561	—	—	561	—	—	mW

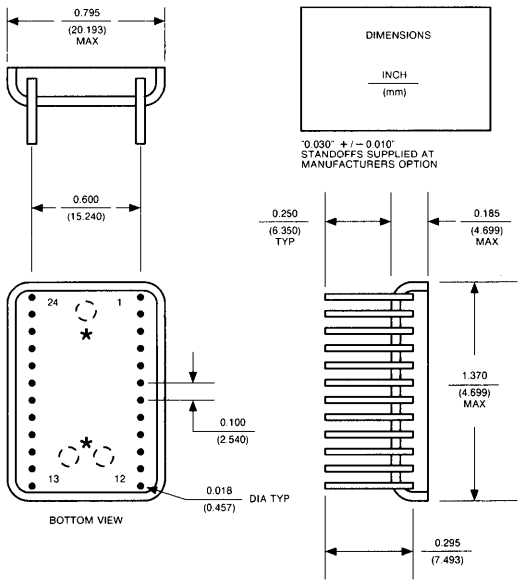
MISCELLANEOUS:

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE						UNITS
			TYP 25°C	0°C to 70°C MIN	0°C to 70°C MAX	TYP 25°C	-55°C to 125°C MIN	-55°C to 125°C MAX	
Input Voltage Range	$V_{IN}+$	$A_{IN}+$ = Input, $A_{IN}-$ = A_{GND}, Bipoff = n.c.					0 to 1		V
		Bipoff = $-V_{AN}$					-.5 to +.5		V
	$V_{IN}-$	$A_{IN}+$ = A_{GND}, $A_{IN}-$ = Input, Bipoff = n.c.					0 to -1		V
		Bipoff = $-V_{AN}$					+.5 to -.5		V
Output Coding		MINVL = HIGH (or n.c.)					Binary		
		MINVL = LOW (or D_{GND})					2's complement		

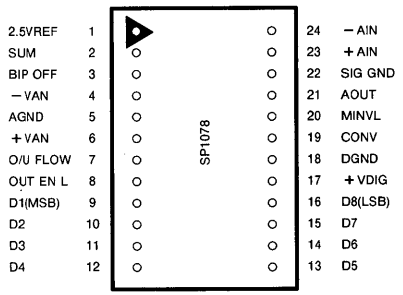
PIN ASSIGNMENTS

PIN	SYMBOL	FUNCTION
1	2.5Vref	Reference Voltage Output
2	SUM	Amplifier Summing Junction
3	BIPOFF	Strap to -Van for Bipolar Inputs
4	-VAN	-5.2 Volt Analog Supply
5	AGND	Analog and Signal Ground
6	+VAN	+5 Volt Analog Supply
7	O/UFLOW	Out-of-range TTL Output
8	OEL	Output Enable Low
9	D1	MSB TTL Data Output
10	D2	TTL Data Output
11	D3	TTL Data Output
12	D4	TTL Data Output
13	D5	TTL Data Output
14	D6	TTL Data Output
15	D7	TTL Data Output
16	D8	LSB TTL Data Output
17	+VDIG	+5 Volt Digital Supply
18	DGND	Digital Ground
19	CONV	Convert Command to Flash
20	MINVL	MSB Invert Low
21	AOUT	Amplifier Output, Resistor Isolated
22	SIGGND	Signal Ground, internally tied to AGND
23	+AIN	Positive Signal Analog Input
24	-AIN	Negative Signal Analog Input

PACKAGE OUTLINE



PIN DESCRIPTION



ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	DESCRIPTION
SP1078C	0°C to + 70°C	8-Bit, 50 MHz ADC
SP1078B	-55°C to + 125°C	8-Bit, 50 MHz ADC, MIL-STD-883C Screening

APPLICATIONS INFORMATION

THEORY OF OPERATION

The SP1078 consists of four circuit blocks: the input amplifier, the flash converter, the precision 2.5 Volt reference and an amplifier offsetting circuit used to pin-strap select either unipolar or bipolar input voltage ranges.

The analog and digital grounds are internally tied through 100 Ohms on the flash converter, but are brought out separately to provide flexibility in system grounding and decoupling. The +5 Volt nominal analog and digital supplies are brought out separately, although they may not exceed one diode drop of voltage difference during operation. In most applications these supplies are tied together or generated from a common supply. The power supplies may be "brought up" in any order and supplies may be connected and disconnected without any known latchup modes. If the potential difference between +Van and +Vdig exceeds one diode drop, the current through the internal diode should be limited to less than 100 mA, or the two supplies tied externally through power diodes.

The input amplifier is a wideband transimpedance amplifier with application resistors configured such that it may be used in the inverting, non-inverting or differential modes. The inverting input (Sum, pin 2) has been brought out to enable non-standard offset and gain configurations. Due to the nature of trans-z amplifiers, this is a low impedance point, capable of sinking and sourcing current. Connecting a resistor from Sum to Ain- (or Agnd if Ain- is grounded) will increase the amplifier gain with only minor change of offset. A resistor from Sum to Vref at pin 1 can be used to decrease the offset at the amplifier output.

The Ain+ non-inverting input pin exhibits a resistance of 417 Ohms, nominal. One Volt fullscale sources need to be able to supply 2.4 mA of current to this pin. An external 56 Ohm resistor to ground will provide termination for a 50 Ohm system. The Ain- inverting input pin exhibits 153 Ohms to virtual ground, when +Ain is grounded. If the input is applied here in the inverting amplifier mode, the source should be capable of 6.5 mA of sink current in 0 to -1 Volt unipolar range, or ± 3.3. mA for the +0.5 to -.5 V range. An external 75 Ohm resistor to Agnd will terminate a 50 Ohm system.

The Signal ground at pin 22 has been internally connected to Agnd at pin 5 in order to minimize ground noise during 50 Msps operation. It should be externally connected to Agnd at pin 5 and any external termination resistors. The amplifier output is available through an internal 450 Ohm nominal resistor at Aout, pin 21. This point will also exhibit the offset induced into the amplifier by the unipolar/bipolar range offset choice. A 50 Ohm resistor to ground will provide a 10 to 1 attenuated replica of the amplifier output suitable for viewing on an oscilloscope, without affecting the amplifier performance.

The flash converter initiates a new conversion at the rising edge of the clock at Conv, pin 19. Old data is held for 7 to 8 ns at the flash outputs, and the new data has settled typically 15 ns from this edge. No internal pipelining is used in the flash conversion process — a single clock edge will generate correct data. The clock input has been designed to be able to use low-level ac coupled signals, or low level dc coupled signals centered about 1.5 Volts. The clock amplitude should not exceed 2.5 Volts peak to peak. If a full TTL level clock is to be used, a small series termination resistor can be used to both series-terminate the clock trace transmission line and to limit the voltage swing at the clock input pin.

The converter control line at MINVL, pin 20, is used to invert the polarity of the msb data at the flash output. An internal 5 kOhm resistor pulls this line up to +Vdig. If this line is externally tied to a logic "low", the msb will be inverted yielding 2's complement coded data. This trace internally shields the CONV signal from analog circuitry. In order to minimize crosstalk it is desirable to connect this pin to a low impedance source, such as +Vdig or Dgnd. The output high impedance control, OEL at pin 8, is used to enable the digital outputs, including the over/underflow flag. Outputs are enabled when this line is at a logic "low".

The digital outputs consist of 8 data lines plus an over/underflow indicator. This O/UFLOW, pin 7, is at a TTL "low" when data has been clocked through the flash converter representing a valid code between 0 and 225. If the analog input was below the voltage representing a valid 0 code, this indicator will be at a TTL "high", indicating a true "underflow" condition. If the analog input was above the voltage representing a valid 255 code, this indicator will be at a TTL "high", indicating a true overflow condition. The output data will clip at the 255 code when in overflow, or at zero when in underflow. Both data and O/UFLOW become valid simultaneously after a rising CONV edge.

The nine digital outputs all are series-terminated internally with 47 Ohm resistors. These terminators limit the rise and fall times of the digital signals which results in less noise generation and lower crosstalk. Any capacitive loading upon these lines will degrade the digital data settling times. In applications where capacitive loads such as a large tri-state bus or cables must be driven, an external bus driver or latch, such as a 74F374 is recommended. Note that Advanced CMOS loads may require pullup resistors or the use of the TTL compatible (74ACTxxx) series at the SP1078 output pins.

The precision 2.5 Volt reference is used internally to set the full scale range of the voltages at the flash converter inputs and to generate a precision current pulled out of the input amplifier inverting input. This current produces an offsetting voltage at the amplifier output. When BipOff (pin 3) is unconnected, the current pulled generates enough offset voltage to guarantee that +1.95 mV at the Ain+ pin will make the flash converter toggle between codes hex 00 and hex 01. When BipOff is pin strapped to -Van (pin 4), the current pulled generates an amplifier offset voltage such that +1.95 mV at the +Ain pin will make the flash converter toggle between codes hex 80 and hex 81 (assuming that MINVL is a high and binary coding is chosen). The 2.5 Volt reference is available at pin 1 and can source up to 2 mA for use in external application circuits.

The low power dissipation of the circuit minimizes any case temperature rise at room temperature operation (around 5°C). The temperature-dependant errors are small — typically the offset moves less than 1.5 lsbs over the -55 to +125°C range. Absolute accuracy of the part will be best after a 1 minute warmup, but the warmup drift is typically much less than 0.2 lsb, and will be negligible for most applications.

CALIBRATION

The SP1078 is a laser trimmed for unipolar and bipolar offset and gain from both the positive and negative inputs. The transimpedance amplifier summing junction has been brought out to facilitate applications requiring non-standard offsets and gains. If system gain and offset is to be calibrated at the converter, external circuitry can sink or source current from this pin.

The offsetting circuitry within the SP1078 depends upon sinking a precision current across the amplifier feedback resistor. Gains can easily be increased by paralleling the internal resistor at the AIN- pin with a resistor from the SUM pin. Because the value of the feedback resistor remains unchanged, the offset at the amplifier output will remain essentially unchanged and will not interact with this type of gain trim. Similarly, an external resistance can be added in series with the resistor at the AIN- pin for a gain reduction. This idea can be used to generate an external gain trim of roughly ± 6% which can be used in either the inverting or non-inverting amplifier mode, and which will have only secondary effects upon the offset of the amplifier. This circuit is shown in figure 1.

Offset adjustments can make use of the summing junction, or in either unipolar mode of operation, current can be sunk or sourced from the BipOff pin. In the inverting mode, the voltage of AIN+ could alternately be adjusted, and in the non-inverting mode the voltage at AIN- could be trimmed. One circuit which can raise and lower the effective gain, as well as increase or decrease the required offset for unipolar operation is shown in figure two. The gain trim will reflect the ratio drift of the trimpot over temperature, while the offset trim will depend upon the absolute drift of the offset resistors (shunted by the stable 540 Ohm internal resistor).

The amplifier resistors have been designed to support use as a differential input amplifier, and common mode rejection is laser trimmed to support this feature. No use of the summing junction should be made in this mode, as any impedance from this point will degrade the common mode rejection of the amplifier. A circuit for ± 0.5 volt p-p differential signals showing balanced 75 Ohm termination is illustrated in figure 3. The input impedance of 417 Ohms at the AIN+ terminal is shunted by 90.9 Ohms to achieve 75 Ohm impedance to ground. The 153 Ohms at AIN- is shunted by 147 Ohms to produce 75 Ohms at the second input. If the source is not floating, it may be necessary to ground the shield only at the source end. The high capacitance between the two signal wires limits the useful bandwidth of such a system to less than 20 MHz, but excellent magnetic and electric noise rejection make such a system very useful for low to moderate frequency signals in a noisy environment.

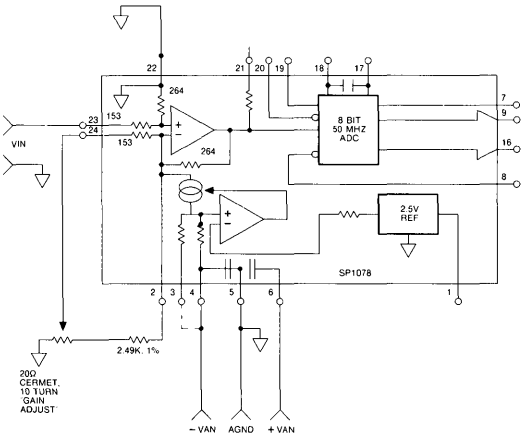


FIGURE 1
UNIVERSAL GAIN ADJUST CIRCUIT CAPABLE OF ± 6% ADJUSTMENT WITH LITTLE EFFECT ON AMPLIFIER OFFSET

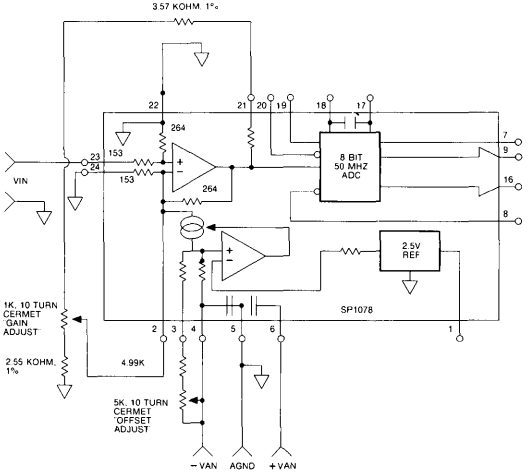


FIGURE 2
OFFSET AND GAIN TRIM FOR POSITIVE UNIPOLAR INPUT APPLICATIONS: ± 1% GAIN AND OFFSET TRIM RANGE, MINIMUM

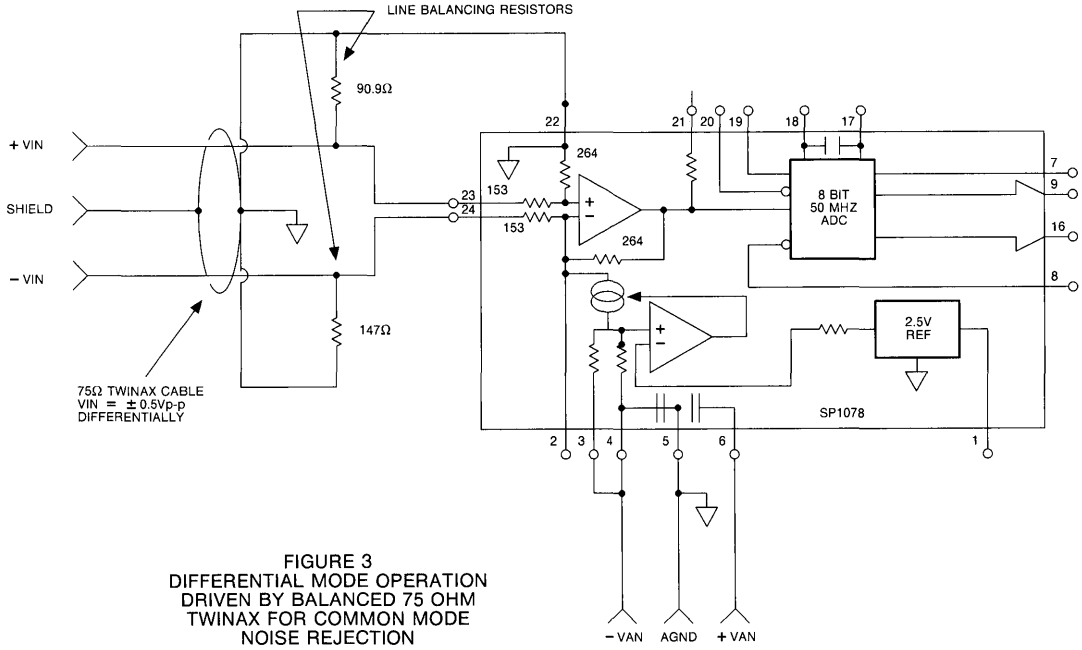
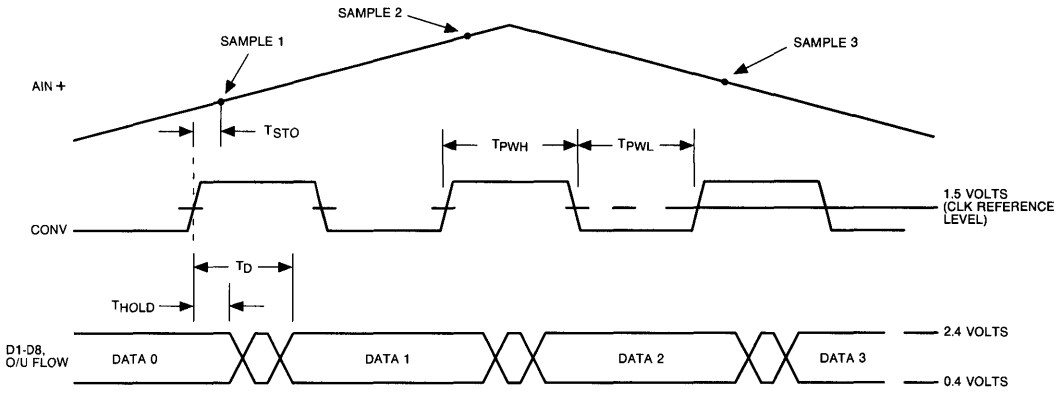


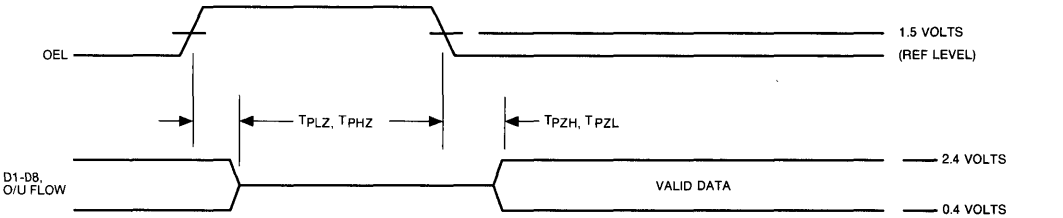
FIGURE 3
DIFFERENTIAL MODE OPERATION
DRIVEN BY BALANCED 75 OHM
TWINAX FOR COMMON MODE
NOISE REJECTION

Output Coding of SP1078

Input Voltage at Code Centers		Output Code		O/UFLOW
Ain+ = Signal Ain– = Agnd BipOff = n.c.	Ain+ = Signal Ain– = Agnd BipOff = –Van	MINVL = n.c. (or = +Vdig)	MINVL = "low" (or = Dgnd)	
–0.0039	–0.5039	0000 0000	1000 0000	1
0.0000	–0.5000	0000 0000	1000 0000	0
+0.0039	–0.4961	0000 0001	1000 0001	0
+0.4961	–0.0039	0111 1111	1111 1111	0
+0.5000	0.0000	1000 0000	0000 0000	0
+0.5039	+0.0039	1000 0001	0000 0001	0
+0.9922	+0.4922	1111 1110	0111 1110	0
+0.9961	+0.4961	1111 1111	0111 1111	0
+1.0000	+0.5000	1111 1111	0111 1111	1
Ain– = Signal Ain+ = Agnd BipOff = n.c.	Ain– = Signal Ain+ = Agnd BipOff = –Van	MINVL = n.c. (or = +Vdig)	MINVL = "low" (or = Dgnd)	
+0.0039	+0.5039	0000 0000	1000 0000	1
0.0000	+0.5000	0000 0000	1000 0000	0
–0.0039	+0.4961	0000 0001	1000 0001	0
–0.4961	+0.0039	0111 1111	1111 1111	0
–0.5000	0.0000	1000 0000	0000 0000	0
–0.5039	–0.0039	1000 0001	0000 0001	0
–0.9922	–0.4922	1111 1110	0111 1110	0
–0.9961	–0.4961	1111 1111	0111 1111	0
–1.0000	–0.5000	1111 1111	0111 1111	1



DATA TIMING DIAGRAM



HIGH IMPEDANCE OUTPUT TIMING

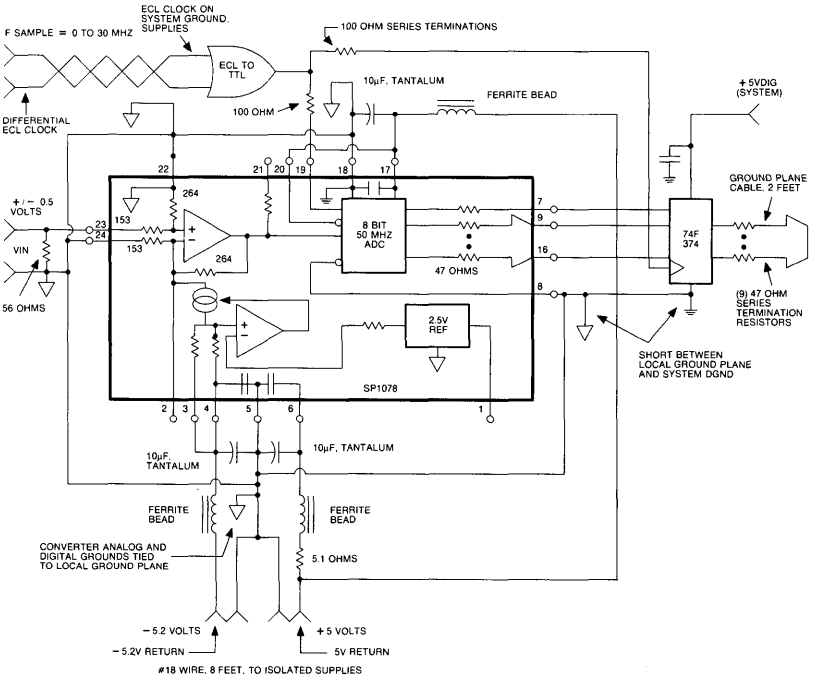


FIGURE 4
BIPOLAR INPUT, NON-INVERTING CIRCUIT
FOR OPERATION UP TO FSAMPLE = 30 MHZ

DYNAMIC PERFORMANCE OF THE SP1078

The SP1078 can be considered a major breakthrough in terms of the quality of the dynamic performance at such low power dissipation. The transimpedance input amplifier offers superb linearity and low distortion combined with excellent settling performance. The flash converter holds its differential and integral linearity up to 10 MHz fullscale inputs at sampling rates up to 50 MHz. This combination provides an excellent solution for high resolution video digitizing, pulse height measurement systems or even for direct downsampling applications from a 10.7 MHz i.f. system. The small signal bandwidth at the flash converter is roughly 20 MHz, and signals of less than fullscale amplitude can be recovered out to that frequency range.

The SNR test is the primary measurement of signal fidelity. As performed, the test sequence involves running the converter under typical still room air conditions at 50 MS/s and grabbing a buffer of 4k points length. The data is multiplied by a Von Hann window, then a 4k point FFT is computed. The resulting spectrum is very carefully measured. The fundamental frequency is first identified, then the rms "Voltage" of the entire window-smeared fundamental section of the spectrum is computed. This section of the spectrum is then "notched out" by manually setting these frequency bins to zero. The rms sum of the rest of the spectrum is then computed and is designated the "noise". Note that any distortions or spurious signals (i.e. oscillations or power supply beats etc.) will be included as "noise". A linear spectrum approximating the Fourier Integral is the result of an FFT. Any non-harmonic component in the data will faithfully be reproduced, without the ambiguity associated with a Fourier series expansion, which assumes a signal may be completely described by its harmonics.

Sampling theory can be used to derive the SNR of an ideal converter, one whose only error is due to the quantization of the numbers describing each point. The result is the well known formula:

SNR (rms sig to rms "noise") = 6.02 × N + 1.76 dB

where N = number of bits in quantized number

In this formula the 1.76 dB applies for all practical cases where the quantization noise will be uncorrelated (white) with respect to the input signal. (This number approaches zero as the input signal approaches DC compared to the sampling frequency — in so-called "coarse quantization").

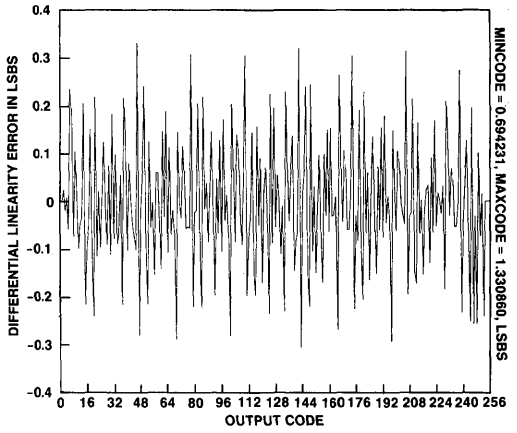
The beat frequency test is another powerful dynamic test technique, and is used to measure settling times, as well as a graphical tool for "seeing" spurious codes. A stable frequency oscillator is set to a small delta frequency over the sampling rate. The resulting output data "walks through" the input wave with very small time steps. The frequency is picked to produce one full cycle of this beat frequency in one buffer (4k points) of data. Settling times may be measured very accurately because the very low aperture jitter of the flash converter ensures the accuracy of the resulting "walked through" data points.

Histogram testing is a useful tool to evaluate the dynamic differential linearity of a video speed converter. A filtered sine wave is applied to the converter and 10 buffers of 4k points are stored. The number of occurrences of each code is then determined, and this histogram is compared with an ideal quantized sine wave of the same gain and offset. The ratio of the real number of occurrences to the ideal number of occurrences yields an effective code width for each code. The ideal code width (one) is subtracted from this ratio to yield the dynamic differential linearity error.

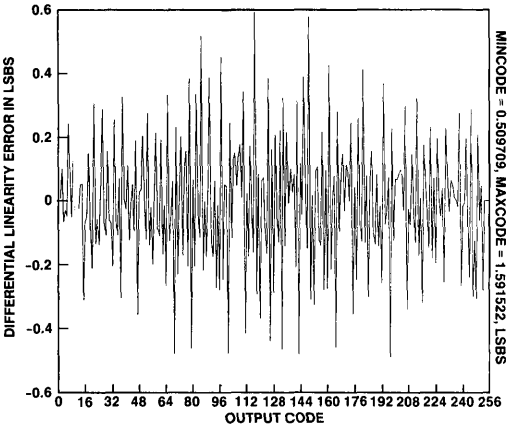
The circuit used to measure the dynamic performance of the SP1078 at sampling rates up to 30 MHz is shown in figure 4. The test computer is at the far end of 2 feet of ground planed cable, and its noisy digital ground must not be allowed into the signal path. A differential ECL clock is generated from a crystal the computer. The clock is converted to TTL levels with extremely low jitter a few inches from the DUT. Two 74F374's are used to latch the output data and drive the cable. Both a local digital ground plane, referenced to the computer ground, and 47 Ohm output series termination resistors are used on the DUT card to minimize ground noise generation and digital noise radiation. The digital supplies on this section of the circuit are common with the computer.

A programmable voltage supply is used to generate two voltages for use on the DUT. A +5 Volt nominal supply and a -5.2 Volt nominal supply are referenced together at a local ground plane at the DUT. The single +5 Volt supply is further isolated by ferrite beads and a small series resistor into an "Analog" and a "Digital" supply, with separate decoupling capacitors. The use of a single supply requires that the converter digital ground be tied to the converter analog ground. This is not a large problem due to the internal 47 Ohm series termination resistors and the low switching currents drawn by this flash converter. At 30 MHz and below the local DUT ground plane can be tied at one point to the system digital ground without much signal degradation. This assures a full noise margin on the output TTL lines. The same rising edge used to generate new data can be used to latch old output data, thus removing any ground noise that a second clock might generate. SIGGND and AGND at the hybrid should always be tied together to the local ground plane to assure a low impedance path from the hybrid substrate to ground.

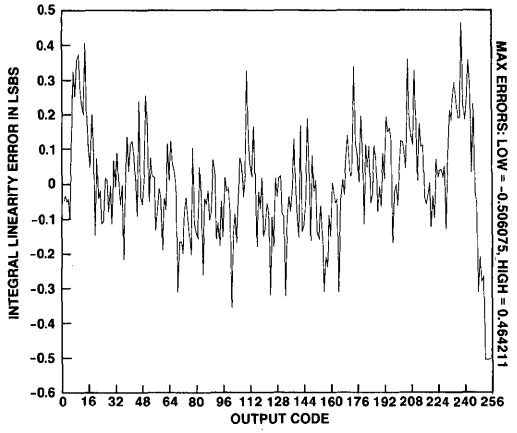
At 20 MHz sampling rates, the performance of this circuit is exhibited in the graphs 1 - 6. Differential linearity at low frequency inputs exhibits less than ± 0.35 lsbs of error, rising to less than ± 0.6 lsbs at Nyquist frequency inputs. The best fit straight line integral linearity is typically ± 0.5 lsb. This is reflected in the excellent 47.7 dBc of Sig-to-Noise-and-Distortion (abbreviated as SNR on the graphs) at 1.123 MHz fullscale input and an incredible 45.1 dB at near Nyquist fullscale input. The 45.1 dBc includes the increased digital noise due to driving the cable with the rapidly changing digital data representing the 9.678 MHz input.



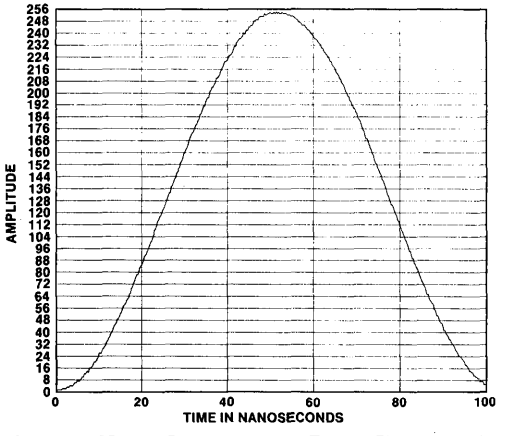
Graph 1. SP1078 Difflin Error at Fin = 48.8 kHz, Fs = 20 MHz



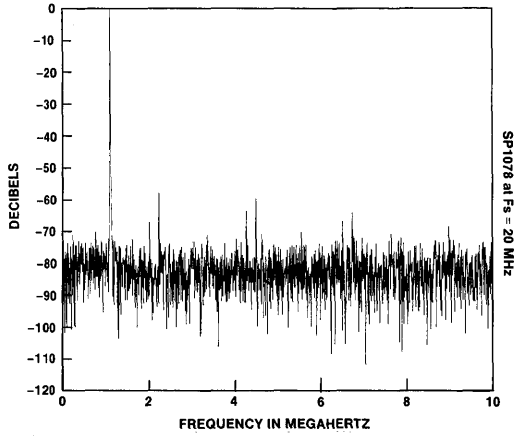
Graph 2. Dynamic DiffLin Error at Fin = 10-MHz, Fs = 20 MHz



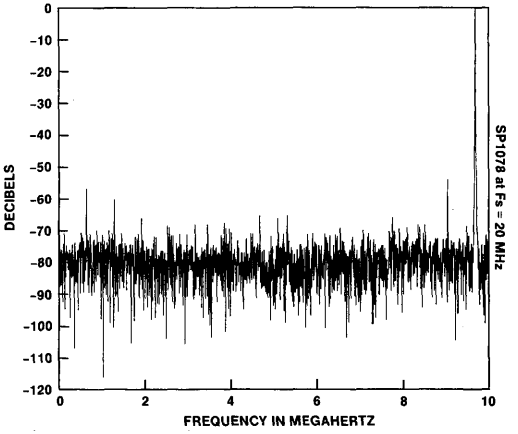
Graph 3. SP1078 Integral Linearity Error at Fin = 48.82 kHz, Fs = 20 MHz



Graph 4. SP1078 Beat Frequency Test at Fin = 10+MHz, Fs = 20 MHz



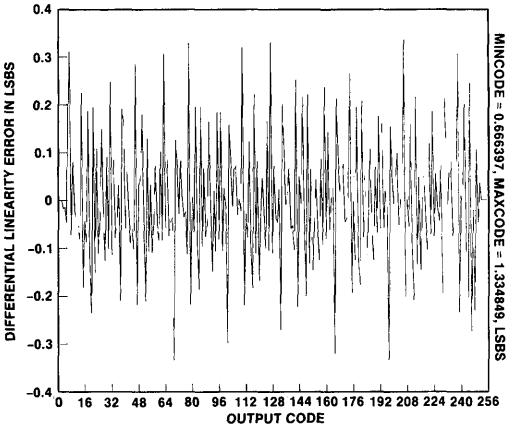
Graph 5. FFT of 1.1234567 MHz, SNR = 47.789730 dB



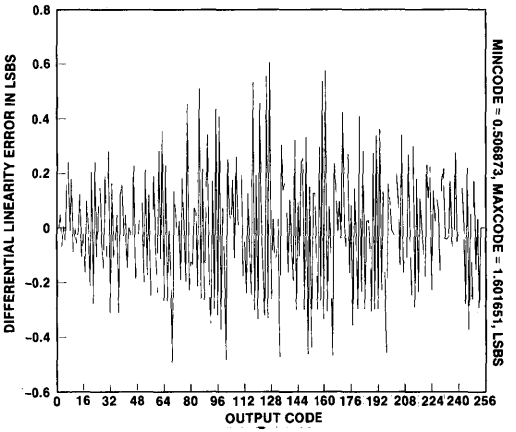
Graph 6. FFT of 9.678901 MHz, SNR = 45.168835 dB

At 30 MHz sampling rates the circuit shows little change.

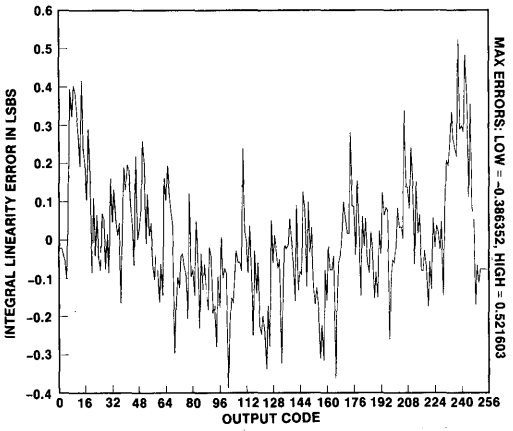
Graphs 7 through 11 illustrate this performance. Low frequency differential errors are less than ± 0.35 lsbs, while 10 MHz inputs yield ± 0.6 lsbs. Integral linearity shows ± 0.52 lsbs of error, and SNR's of 47.5 and 45.0 are virtually the same.



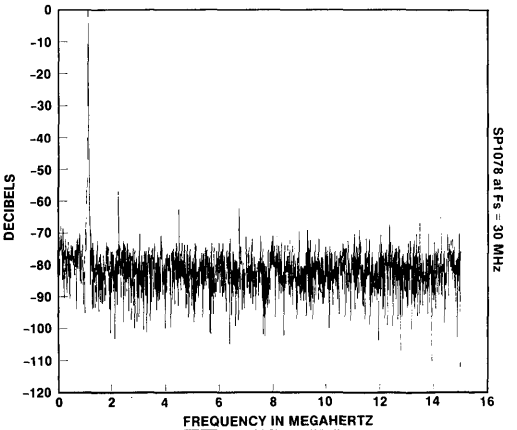
Graph 7. SP1078 Difflin Error at Fin = 7.324 kHz, Fs = 30 MHz



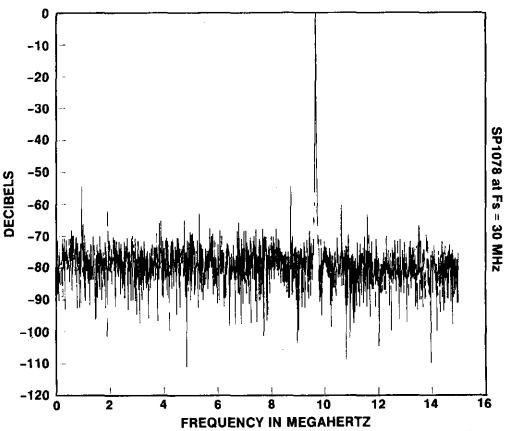
Graph 8. Dynamic DiffLin Error at Fin = 10–MHz, Fs = 30 MHz



Graph 9. SP1078 Integral Linearity Error at Fin = 7.324 kHz, Fs = 30 MHz



Graph 10. FFT of 1.1234567 MHz, SNR = 47.580505 dB



Graph 11. FFT of 9.678901 MHz, SNR = 45.049816 dB

In order to measure the performance of 40 to 50 MHz sampling rates, (on a tester only capable of 30 MHz operation) the DUT card needed to be modified. A TTL clock equal to 1/2 of the Fsample clock was generated at the computer. It was used to latch "every other" digital word at the converter output — a hardware "decimate-by-two" function. Because any high harmonic will be aliased back into the output data, no loss of generality is incurred in the SNR or other measuring algorithms, although the frequency axis on the FFT graphs only extends to 1/2 of the decimated rate (i.e. to 10 MHz after decimating the 40 MHz data down to a 20 MHz data rate).

While the latching of the data occurred at no higher rates than at previous tests, the termination of the clock itself and its jittery timing after propagating down the cable increased the digital ground noise significantly. It was found necessary to isolate this noisy system ground from the DUT for best performance. The braid from the DUT ground plane to the local digital ground plane was replaced by twenty Ohms in series with a 20 MHz ferrite bead. Note that 20 Ohms is near the practical limit as values much higher will "use up" all the noise margin for TTL logic "lows", and "spurious-looking" codes will corrupt the digital data.

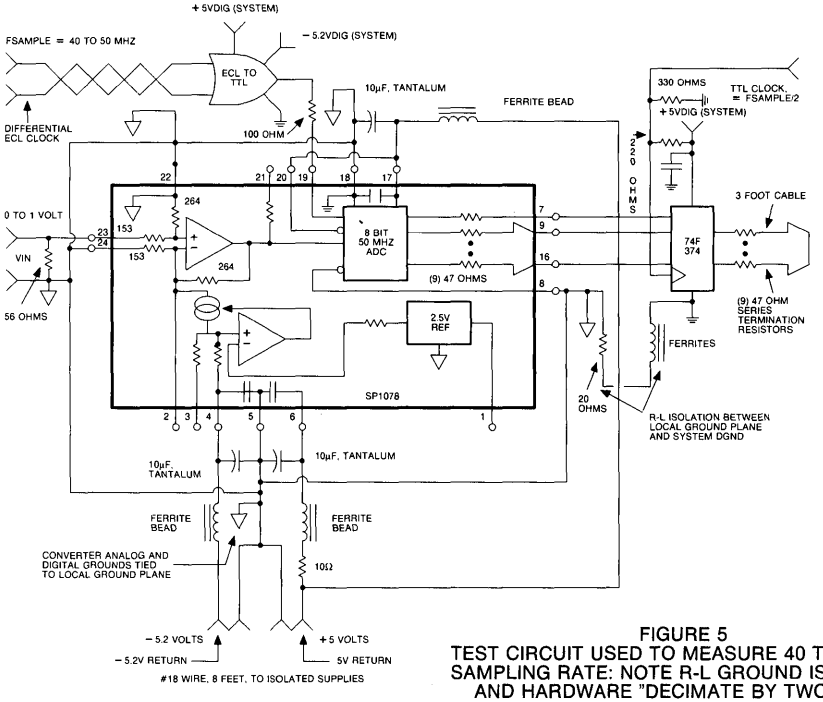
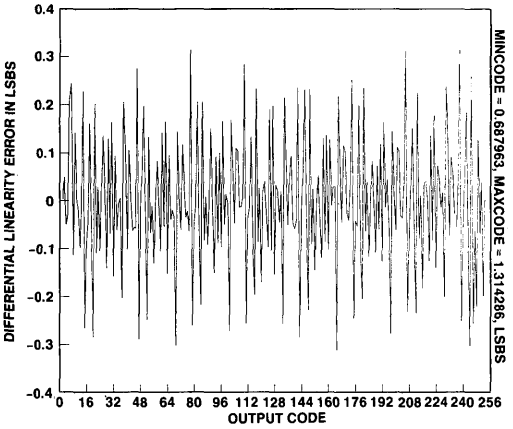
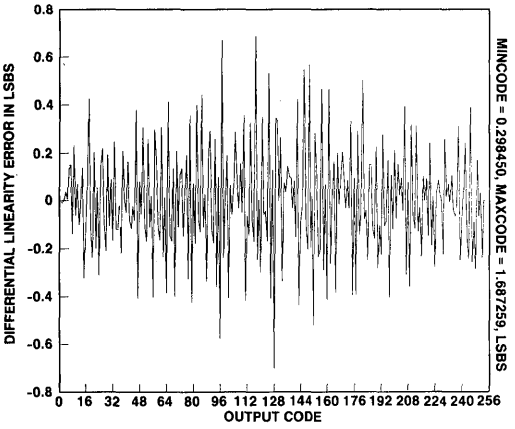


FIGURE 5
TEST CIRCUIT USED TO MEASURE 40 TO 50 MHZ SAMPLING RATE: NOTE R-L GROUND ISOLATION, AND HARDWARE "DECIMATE BY TWO" USED TO MINIMIZE GROUND NOISE GENERATION AND COUPLING (ECL CLOCK ON SYSTEM DGND PLANE)

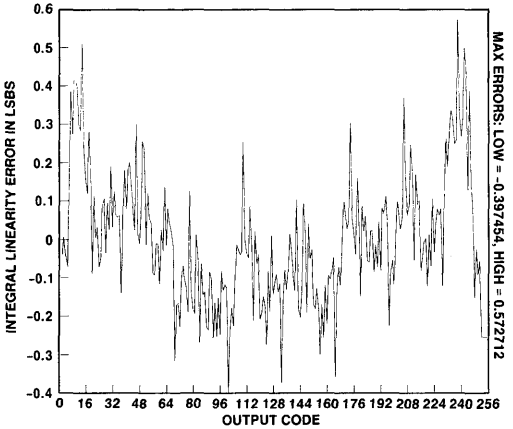
The higher frequency clock now was also generating more noise on the DUT digital supply. Increased isolation resistors were inserted between +Van and +Vdig at the DUT. Figure 5 shows the test circuit. To illustrate the use of the unipolar mode selection, these tests were run at a unipolar input voltage range of 0 to +1 Volt, (BIPOFF = n.c.). The tests were repeated at 40 MHz sampling rates. The results appear in graphs 12 - 17. DC differential linearity actually improved to ± 0.33 lsbs. Differential error at 10 MHz in is near ± 0.7 lsbs. Low frequency integral linearity error is within ± 0.6 lsbs. SNR at 1.123 MHz stayed at 47.8 dBc, while at 9.678 MHz it degraded marginally to 44.9 dBc. The settling time test graph shows two features of interest. The first is the well behaved 18 ns settling time of the amplifier. The second point is the presence of spurious codes during the digitization of the fast-slewing edge of the square-wave input. Because the amplifier is cable of 4 ns rise times, the slew rate must be limited before the input to the SP1078 in applications where no spurious codes can be allowed. Note that in pulse height measurement applications, the flash converter is typically not strobed until the pulse has settled at the output of the amplifier.



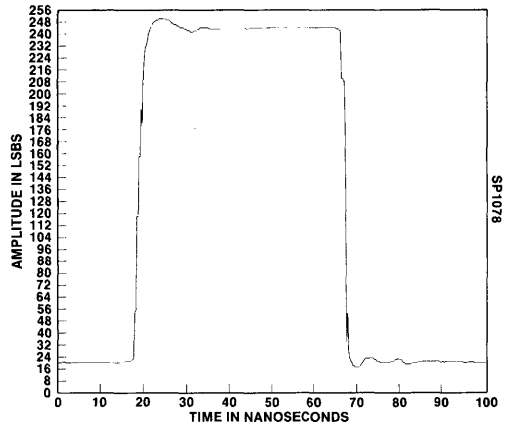
Graph 12. SP1078 Difflin Error at Fin = 48.82 kHz, Fs = 40 MHz



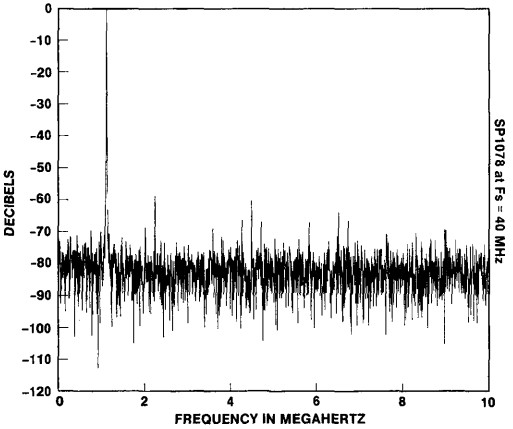
Graph 13. Dynamic DiffLin Error at Fin = 10-MHz, Fs = 40 MHz



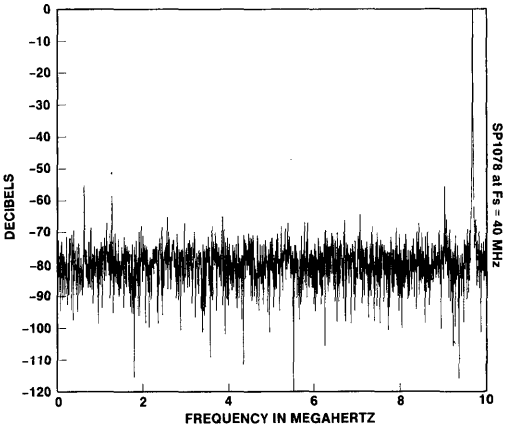
Graph 14. SP1078 Integral Linearity Error at Fin = 48.82 kHz, Fs = 40 MHz



Graph 15. Beat Frequency Settling Time Test Fin = 10+MHz, Fs = 40 MHz

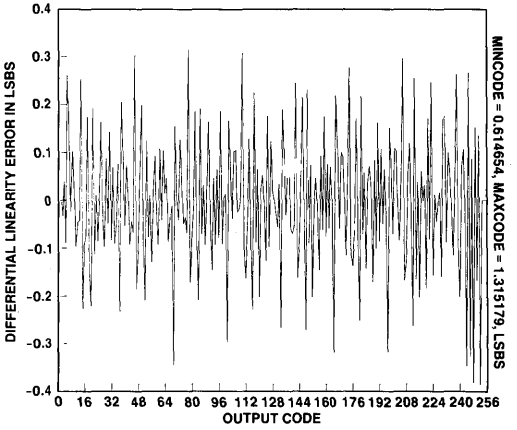


Graph 16. FFT of 1.1234567 MHz, SNR = 47.823864 dB

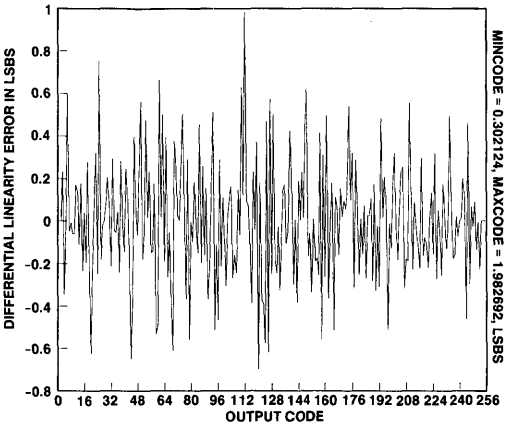


Graph 17. FFT of 9.678901 MHz, SNR = 44.940491 dB

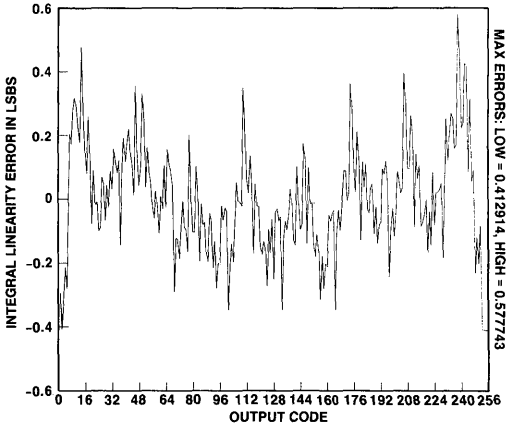
The tests were repeated at 50 MHz sampling frequency. The graphs 18 - 25 show excellent dynamic performance at this rate. Low frequency differential error is better than ± 0.35 lsbs. At a 10 MHz input frequency, the dynamic differential error is less than +1.0, -0.8 lsb. Integral linearity error is still ± 0.6 lsb. SNR at 1.123 MHz degraded slightly to 46.4 dBc, and second harmonic distortion limits the SNR at 9.678 MHz to 41.1 dBc. To demonstrate the true 12 MHz spurious-free fullscale power bandwidth, a plot of the SNR at 12.123 MHz input displays 37.5 dBc, dominated by second and third harmonic distortion components. The variance between 10 SNR measurements was less than 0.1 dB, revealing the absence of spurious codes. The beat frequency plot of a 12.5 MHz fullscale input shows no spurious codes at this slew rate and no dynamic differential linearity aberrations. The settling time plot of a 12.5 MHz square wave provides finer detail of the amplifier's 18 ns settling time. Again the spurious codes generated at digitization of the fast-slewing edges are apparent.



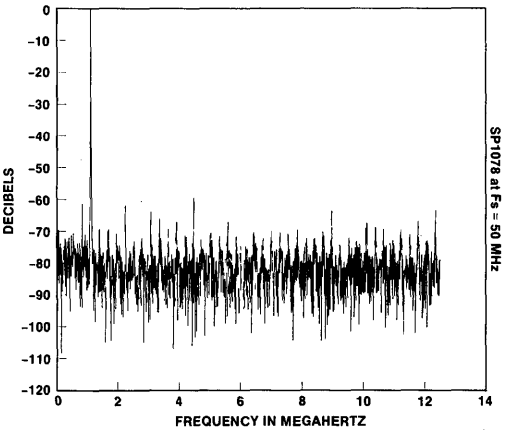
Graph 18. SP1078 Difflin Error at Fin = 6.1 kHz, Fs = 50 MHz



Graph 19. Dynamic DiffLin Error at Fin = 10-MHz, Fs = 50 MHz

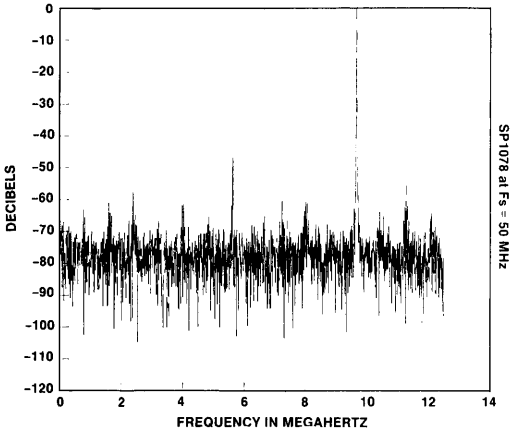


Graph 20. SP1078 Integral Linearity Error at Fin = 6.1 kHz, Fs = 50 MHz

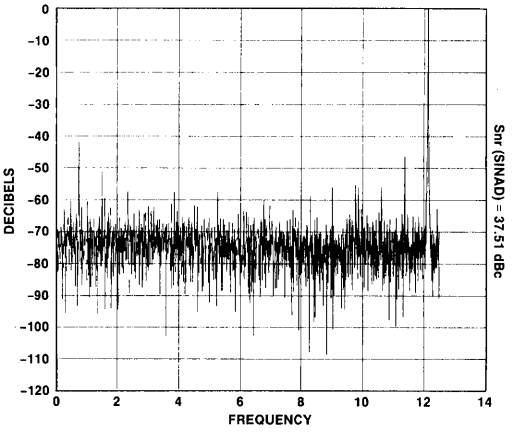


Graph 21. FFT of 1.123456 MHz, SNR = 46.430019 dB

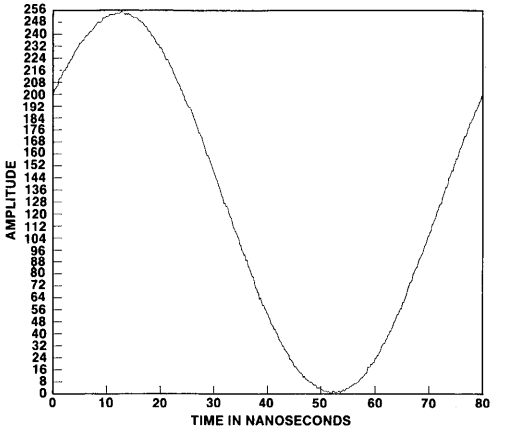
Attempts to run at 60 MHz were unsuccessful until system timing and isolation were again modified. Timing was adjusted by shorting the 100 Ohm series termination at the converter CONV pin, to satisfy the output data settling time at the 74F374. Ground isolation was brought up to 24 Ohms to limit ground noise coupling (at further expense to TTL noise margin). The duty cycle of the 16.6 ns 60 MHz clock pulse violated the minimum 8 ns Tpwl, and thus this mode of operation is not recommended for customer use over temperature. The resulting data shows that the converter is capable of operation at 60 MHz if the system is carefully tweaked. DC difflin error was within ± 0.4 lsbs, while dynamic difflin at 10 MHz input showed one almost-missing code and one of width greater than 1 lsb. DC integral linearity error was within ± 0.8 lsbs and SNR's of 43.2 and 40.0 dBc at 1.123 and 9.678 MHz displayed variances of less than 0.1 dB, attesting to no-spurious-code operation. The beat frequency test displays the no-spurious-code behavior, although the widening of some codes reveals the onset of dynamic differential linearity aberrations.



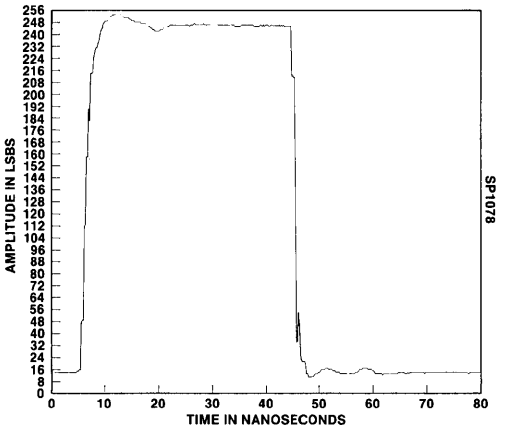
Graph 22. FFT of 9.678 MHz, SNR = 41.191879 dB



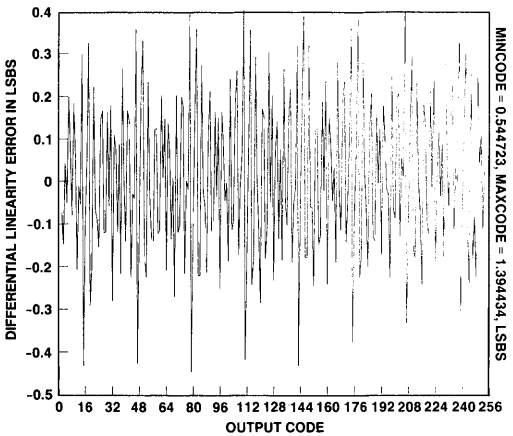
Graph 23. FFT of 12.123 MHz Fin, Fs = 50 MHz Decimated by Two



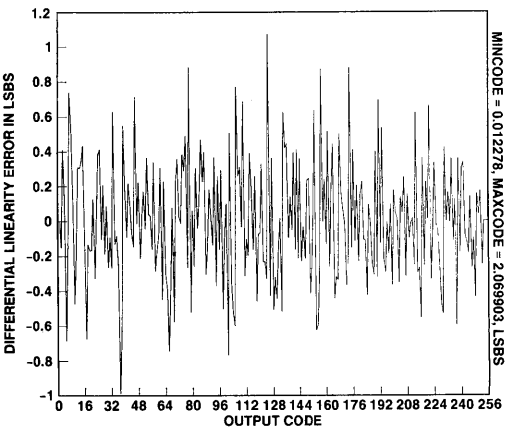
Graph 24. SP1078 Beat Frequency Test at Fin = 12.5+MHz, Fs = 50 MHz



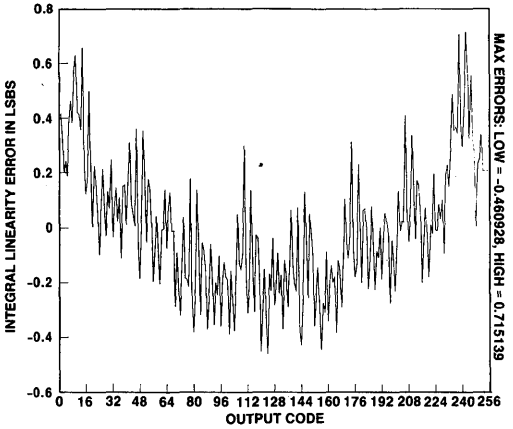
Graph 25. Beat Frequency Settling Time Test Fin = 12.5+MHz, Fs = 50 MHz



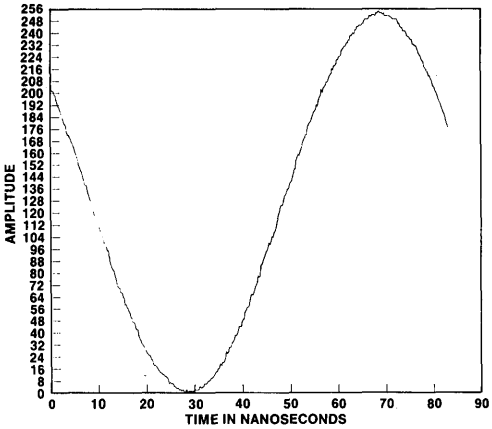
Graph 26. SP1078 Difflin Error at Fin = 7.324 kHz, Fs = 60 MHz



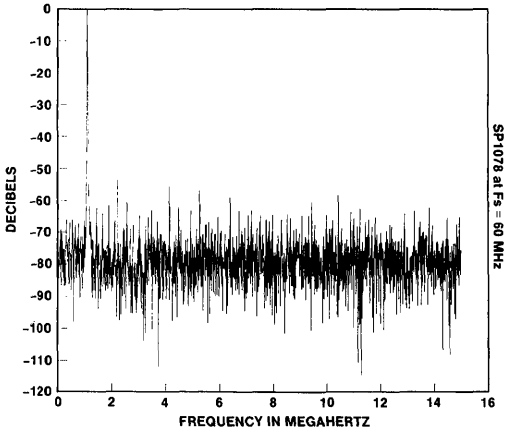
Graph 27. Dynamic DiffLin Error at Fin = 10-MHz, Fs = 60 MHz



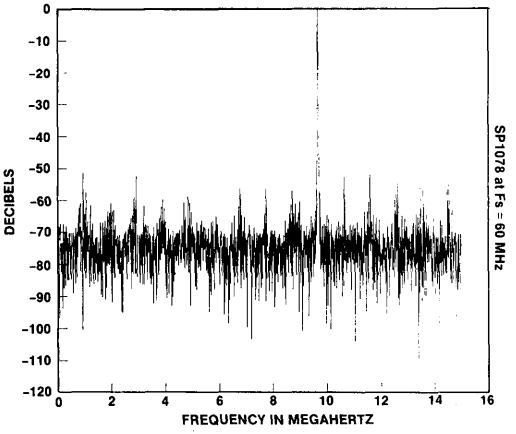
Graph 28. SP1078 Integral Linearity Error at Fin = 7.324 kHz, Fs = 60 MHz



Graph 29. SP1078 Beat Frequency Test at Fin = 12+MHz, Fs = 60 MHz



Graph 30. FFT of 1.1234567 MHz, SNR = 43.288948 dB



Graph 31. FFT of 9.678901 MHz, SNR = 40.006523 dB

The dynamic performance of this part is unrivaled by any circuit dissipating less than 1.5 Watts, and represents a new standard for signal purity while eliminating the thermal management headaches associated with high power circuits.

ANALOG-TO-DIGITAL CONVERTERS

MODEL	RESOLUTION	CONVERSION SPEED (µsec)	µP COMPATIBLE	INTERNAL CLOCK	INPUT RANGES	POWER CONSUMPTION (mW)	PACKAGE	PAGE
ADC541/542	8 bits	2.5	No	Yes	6 ranges	650	24-Pin DD	427
HS ADC82	8 bits	2.5	No	Yes	6 ranges	650	24-Pin DD	417
HS5131	8 bits	2.5	No	No	±5V	680	18-Pin SD	451
HS5150	8 bits	2.5	Yes	No	7 ranges	680	24-Pin DD	453
HS ADC85	12 bits	10	No	Yes	5 ranges	1320 max	32-Pin TD	421
HS5210	12 bits	13	No	No	4 ranges	785	24-Pin DD	457
HS5251	12 bits	175	No	No	±5V	56	24-Pin DD	463
HS574A	12 bits	25	Yes	Yes	4 ranges	150	28-Pin DD	431
SP674A	12 bits	15	Yes	Yes	4 ranges	150	28-Pin DD	441
SP9548	12 bits	0.5	No	Yes	0 to +5V	1700	32-Pin TD	471
SP9550	12 bits	0.2	No	Yes	0 to +5V	1700	32-Pin TD	477
SP9588	14 bits	2	No	Yes	0 to -10V	2100	32-Pin TD	487
HS9516	16 bits	100	No	Yes	6 ranges	1200	32-Pin TD	467
HS9576	16 bits	15	No	Yes	6 ranges	1000	32-Pin TD	481

Shaded area indicates new product since publication of 1988 Catalog

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS ADC82

FAST 8-BIT ADC

FEATURES

- 2.8 µS Conversion Time
- Low Power . . . 650 mW
- Completely Self Contained
- Fully Compatible with ADC82 AG
- Low Cost

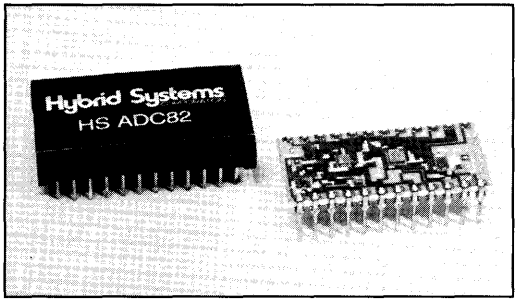
DESCRIPTION

The HS ADC82 is a fast, low power, hybrid IC analog-to-digital converter (ADC). It features 8-Bit resolution and accuracy with 2.8 µsec maximum conversion time. The inputs can be pin-programmed for 0 to +5V, 0 to +10V, 0 to +20V and ±2.5V, ±5V and ±10V. All digital inputs and outputs are TTL compatible. The outputs are provided in either parallel or serial format. HS ADC82 is completely self-contained with internal clock, reference, comparator, successive approximation register and a monolithic 8-Bit DAC.

Outstanding features include:

No External Adjustments — HS ADC82 is pre-trimmed for 8-Bit accuracy to eliminate external adjustments. However, HS ADC82 provides offset and gain adjust pins to obtain even greater accuracy.

Low Power — HS ADC82 is designed for minimum power consumption. The reference circuitry and resistor values were chosen for lowest possible currents, to avoid excessive dissipation and heat spots within the hybrid circuitry.



Pin-to-Pin Compatibility — The HS ADC82 is a superior replacement for the BURR-BROWN ADC82 AG. Reduced power consumption and a new packaging technique offer increased reliability and reduced cost.

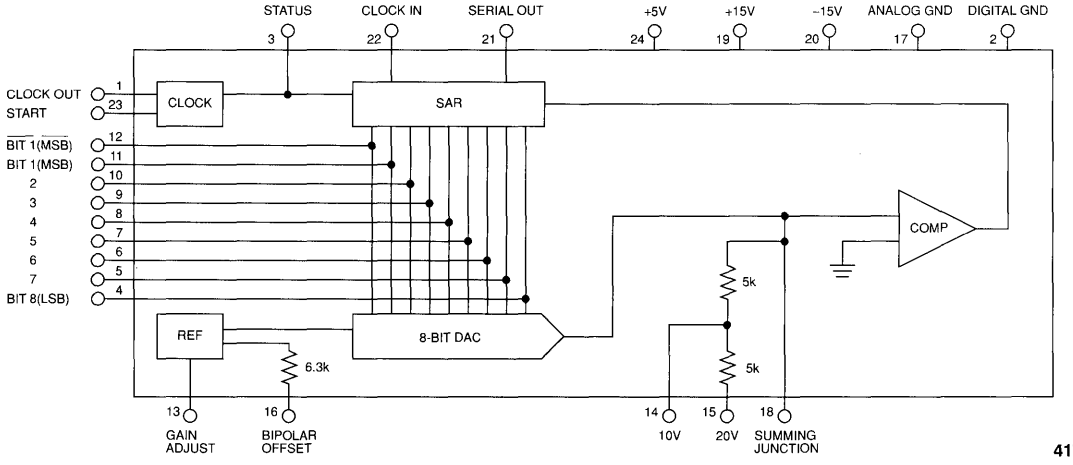
Reliability Plus — Our unique 24-pin double DIP[1] is a proven performer, offering the utmost in reliable packaging for our 9000 Series converter products.

Reliability is enhanced by batch-processed, precision laser-trimmed resistor networks fabricated in our own facility. Similar to monolithic circuits, the networks are processed and functionally trimmed to assure consistent performance. Networks are glass passivated to assure reliability under adverse environmental conditions.

1. U.S. Patent Pending

9

FUNCTIONAL DIAGRAM



SPECIFICATIONS

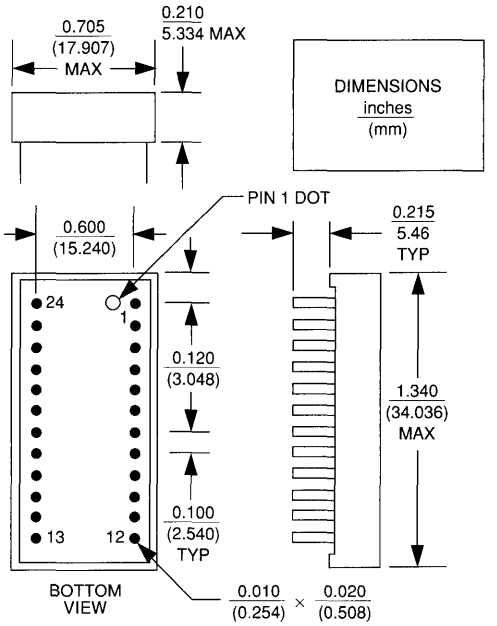
(Typical @ +25°C and nominal power supply unless otherwise noted)

MODEL	HS ADC82
RESOLUTION	8-Bits
TYPE	Successive Approximation
ANALOG INPUT	
Unipolar	0 to +5V, 0 to +10V, 0 to +20V
Bipolar	±2.5V, ±5.0V, ±10V
Impedance	500Ω/Volt
DIGITAL INPUT	
Start Command[1]	Positive Pulse 50 nS (min), TTL
Logic Loading	1 TTL Load
Clock Input	1 TTL Load
DIGITAL OUTPUT	
Data Coding	
Parallel, Unipolar	Complementary Binary
Parallel, Bipolar	Complementary Offset Binary Complementary 2's Complement
Serial Coding	NRZ, Complementary Binary Complementary Offset Binary
Data Output Drive Capability	3 TTL Loads Logic "1" > 2.4V, "0" < 0.4V
Status Output Driver Capability	2 TTL Loads Logic "1" During Conversion
Clock Output Frequency	2.85 MHz
CONVERSION TIME[2]	2.8 µS (max)
ACCURACY	
Quantization	±1/2 LSB
Linearity	±0.2% F.S.R. (max)
Gain Error[3]	±0.1%
Offset Error,[3] Unipolar and Bipolar	±0.05% F.S.R.
No Missing Codes Temp. Range	0°C to 70°C
Total Accuracy Error[4]	±1 LSB (max)
STABILITY (Over Specified Temp. Range)	
Linearity	±20 ppm of F.S.R./°C (max)
Gain	±40 ppm/°C (max)
Offset	
Unipolar	±20 ppm of F.S.R./°C (max)
Bipolar	±35 ppm of F.S.R./°C (max)
Monotonicity	Guaranteed
POWER SUPPLY	
Requirements	
+15V ±3%	24 mA max
-15V ±3%	12 mA max
+5V ±5%	105 mA max
Rejection Ratio	
+15V	±0.05%/% max
-15V +5V	0.01%/% max
Total Power Consumption	650 mW, 1W max
TEMPERATURE RANGE	
Specified, Operating[5]	0°C to 70°C
Storage	-55°C to +85°C
MECHANICAL	
Case Style	24 Pin Double DIP

NOTES

1. Starting edge resets register, trailing edge starts conversion.
2. Conversion time with internal clock.
3. Can be adjusted to zero using external trim circuitry. See APPLICATIONS INFORMATION.
4. Gain and offset error adjusted to zero.
5. Specify Hybrid Systems Model ADC542 for operating temperature range of -55°C to +125°C.
6. Use trailing edge of clock to strobe serial output.

CASE DIMENSIONS

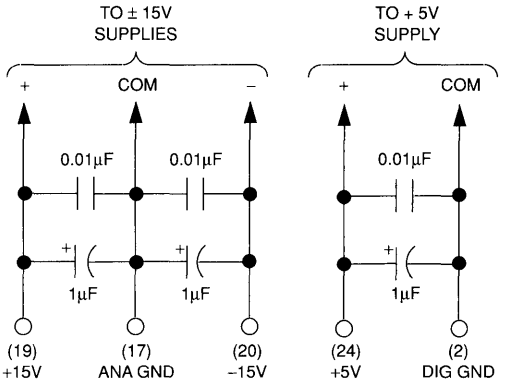


PIN DESIGNATIONS

PIN	FUNCTION
1	CLOCK OUT
2	DIGITAL GND
3	STATUS
4	BIT 8 (LSB)
5	BIT 7
6	BIT 6
7	BIT 5
8	BIT 4
9	BIT 3
10	BIT 2
11	BIT 1 (MSB)
12	$\overline{\text{BIT 1 (MSB)}}$
13	GAIN ADJUST
14	10V INPUT
15	20V INPUT
16	BIPOLAR OFFSET
17	ANALOG GND
18	SUMMING JCT
19	+15V
20	-15V
21	SERIAL OUT
22	CLOCK IN
23	START
24	+5V

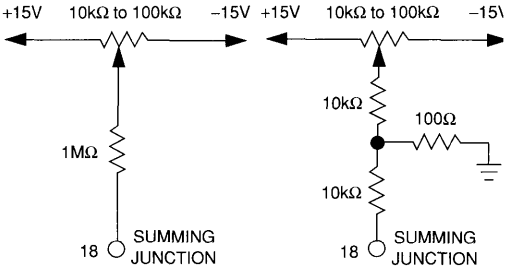
APPLICATIONS INFORMATION

RECOMMENDED POWER SUPPLY BYPASS CIRCUIT



OPTIONAL OFFSET AND GAIN ADJUSTMENTS

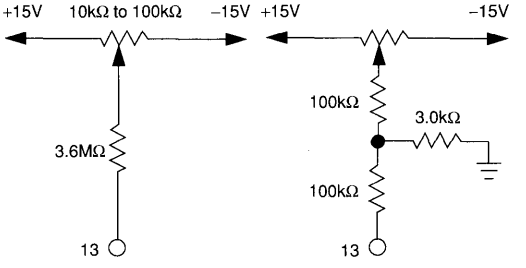
Offset Adjust



Two Methods Offering a ±1% Swing

Unipolar: Apply a +1/2 LSB analog input and set the potentiometer for a digital output that alternates between 111 ... 1 and 111 ... 0.
Bipolar: No adjustments necessary.

Gain Adjust



Two Methods Offering a ±1% Swing

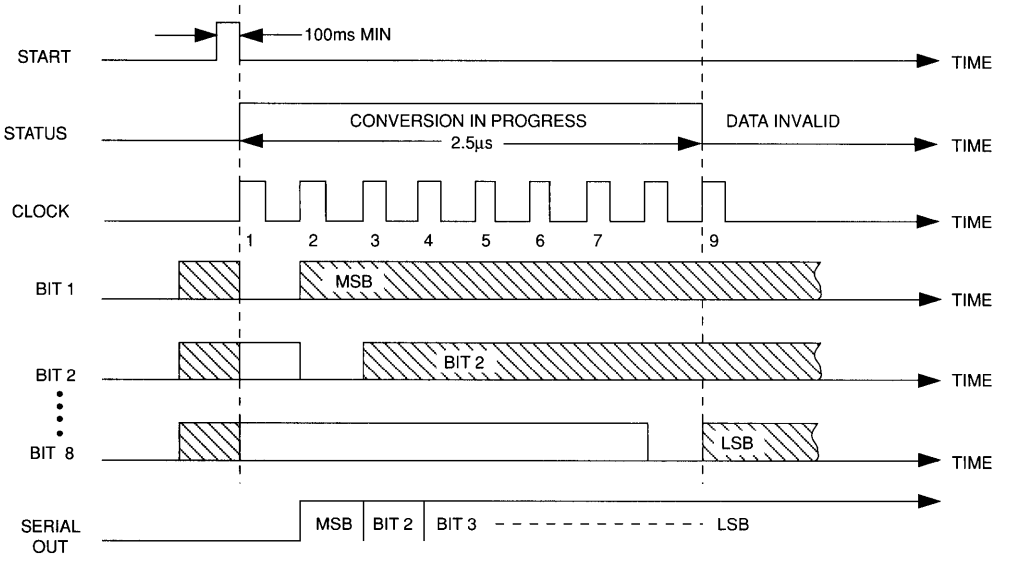
Unipolar & Bipolar: Apply a +(F.S. -3/2 LSB) analog input and set the potentiometer for a digital output that alternates between 000 ... 0 and 000 ... 1.

INPUT VOLTAGES, TRANSITION VALUES, LSB VALUES AND CODE DEFINITIONS

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE						
ANALOG INPUT VOLTAGE RANGES	DEFINED AS	±10V	±5V	±2.5V	0 to +10V	0 to -5V	0 to +20V
CODE DESIGNATION		COB or CTC	COB or CTC	COB or CTC	CSB	CSB	CSB
ONE LEAST SIGNIFICANT BIT (LSB)	FSR 2^n n = 8	20V 2^n 78.13 mV	10V 2^n 39.06 mV	5V 2^n 19.53 mV	10V 2^n 39.06 mV	5V 2^n 19.53 mV	20V 2^n 78.13 mV
TRANSITION VALUES MSB LSB							
000 . . . 00ϕ	+FULL SCALE	+10V -1 1/2 LSB	+5V -1 1/2 LSB	+2.5V -1 1/2 LSB	+10V -1 1/2 LSB	+5V -1 1/2 LSB	+20V -1 1/2 LSB
ϕϕϕ . . . ϕϕϕ	MID SCALE	-1/2 LSB	-1/2 LSB	-1/2 LSB	+5V -1/2 LSB	+2.5V -1/2 LSB	+10V -1/2 LSB
111 . . . 11ϕ	-FULL SCALE	-10V -1/2 LSB	-5V -1/2 LSB	-2.5V -1/2 LSB	0 + 1/2 LSB	0 + 1/2 LSB	0 + 1/2 LSB

The voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting the output bits indicated as ϕ will change from "1" to "0" or from "0" to "1" as the input voltage passes through the level indicated.

TIMING DIAGRAM



INPUT SELECTION

INPUT VOLT. RANGE	PIN CONNECTIONS	INPUT PIN
0 to +5V	16 to 17 & 15 to 18	
±2.5V	16 to 18 & 15 to 18	14
0 to +10V	16 to 17	
±5V	16 to 18	14
0 to +20V	16 to 17	
±10V	16 to 18	14

ORDERING INFORMATION

MODEL	DESCRIPTION
HS ADC82	8-Bit ADC, Commercial

Specifications subject to change without notice.

HS ADC85

12-BIT, 10 μS HYBRID ADC

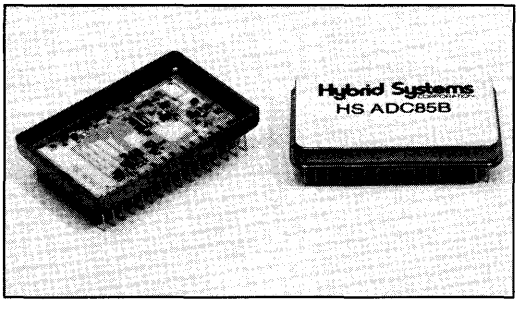
FEATURES

- -55°C to +125°C Operation
- MIL-STD-883 Processing
- 10 μS Conversion Time
- Low Power, 1.32W (max)
- Replacement for ADC85/84 and ADC-HX12B/HZ12B

DESCRIPTION

The HS ADC85 is specifically designed to replace the ADC581, ADC85/84 and ADC-HX12B/HZ12B. Complete with internal clock, reference and input buffer amplifier, the HS ADC85 can also be used with an external clock for synchronization (see EXTERNAL CLOCK section under APPLICATIONS INFORMATION). Conversion speeds of 10 μs for 12-Bit operation, and 8 μs for 10-Bit operation allows the HS ADC85 to be used in a wide range of applications. Short cycle and internal clock rate may also be externally adjusted to provide faster conversion speeds at lower resolutions. Gain and offset can be externally trimmed to zero, providing full scale accuracy of ±0.012% ±1/2 LSB. Data is obtainable in both parallel and serial form with corresponding clock and status signals. Digital input and output signals are DTL/TTL compatible. Other features include:

Low Power — A 33% reduction in power dissipation allows the HS ADC85 to operate reliably at high temperatures without failure due to excessive package heating. Total power consumed is only 1.32W maximum.



Selectable Input Ranges — Input scaling resistors allow the selection of input ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V.

Reliability — Packaged in a 32-pin hermetically sealed case, and utilizing advanced devices and laser-trimmed thin-film resistors, the HS ADC85 is one of the most reliable analog-to-digital converters to date. Specified over the -55°C temperature range, it has a low linearity drift specification of only ±2 ppm/°C maximum. All "B" versions of the HS ADC85 series are fully screened and tested to MIL-STD-883 Rev. C, Level B requirements.

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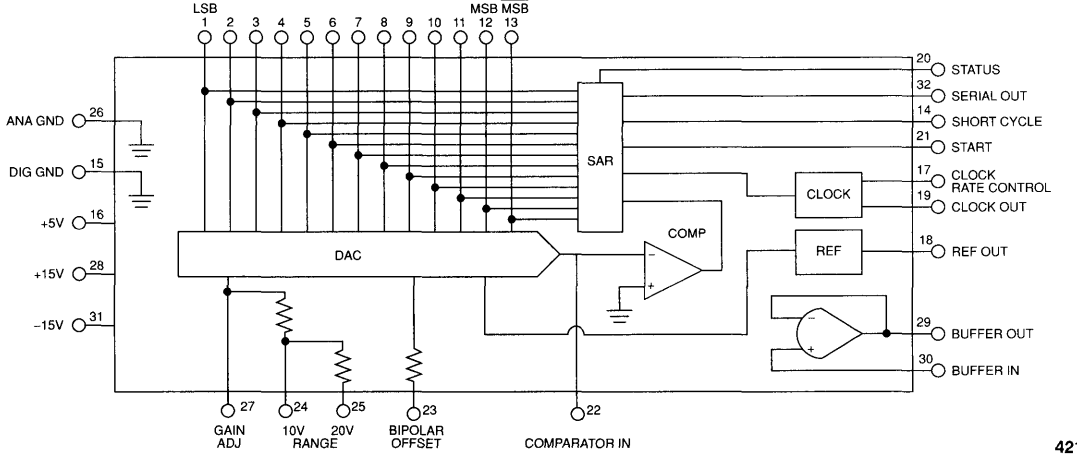
FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C and rated power supply unless otherwise noted)

SERIES	HS ADC85
TYPE	**Successive Approximation**
RESOLUTION	12-Bits
ANALOG INPUTS	
Bipolar Ranges	±2.5V, ±5V, ±10V
Unipolar Ranges	0 to +5V, 0 to +10V
Impedance (Direct Input)	300Ω/Volt
Buffer Amplifier	
Impedance	100 MΩ (min)
Bias Current	50 nA
Settling Time[1]	2 µS
DIGITAL INPUTS[2]	
Start	Positive Pulse 50 nS Wide (min), Trailing Edge ("1" to "0") Initiates Conversion[3]
Logic Loading	1 TTL Load
External Clock	Optional[4]
DIGITAL OUTPUTS[2]	
Parallel Data	
Output Codes	
Unipolar	Comp. Straight Bin.
Bipolar	Comp. Offset Bin., Comp. Two's Comp.
Output Drive	2 TTL Loads (min)
Serial (Non Return to Zero) Data	
Output Codes	Comp. Straight Bin., Comp. Offset Bin.
Output Drive	2 TTL Loads (min)
Status	Logic "1" During Conversion
Status Output Drive	2 TTL Loads (min)
Clock Out[4]	
Output Drive	2 TTL Loads (min)
Frequency	1.4 MHz
REFERENCE	Internal +6.2V ±5%
Ref Out	200 µA Maximum with no Degradation of Specs
Drift	±10 ppm/°C (max)
CONVERSION TIME/THROUGHPUT RATE	8.8 µS, Typ; 10 µS, max/100 kHz
ACCURACY @ 25°C	
Quantization	±1/2 LSB
Linearity	±0.012% of F.S.R. (max)
Offset[5]	
Unipolar	±0.05% of F.S.R.
Bipolar	±0.1% of F.S.R. (max)
Gain[5]	±0.1% of F.S.R.
Monotonicity	No Missing Codes
STABILITY	
Linearity	
-25°C to +85°C	±1 ppm/°C; ±2 ppm/°C, (max)
-55°C to +125°C	±2 ppm/°C, (max)
Scale Factor (Gain)	
-25°C to +85°C	±8 ppm/°C; ±15 ppm/°C, (max)
-55°C to +125°C	±20 ppm/°C, (max)
Offset (Unipolar)	
-25°C to +85°C	±2 ppm/°C; ±3 ppm/°C, (max)
-55°C to +125°C	±3 ppm/°C, (max)
Offset (Bipolar)	
-25°C to +85°C	±4 ppm/°C; ±7 ppm/°C, (max)
-55°C to +125°C	±12 ppm/°C, (max)
Total Transfer Accuracy	
-25°C to +85°C	±10 ppm/°C; ±20 ppm/°C, (max)
-55°C to +125°C	±30 ppm/°C, (max)

SPECIFICATIONS

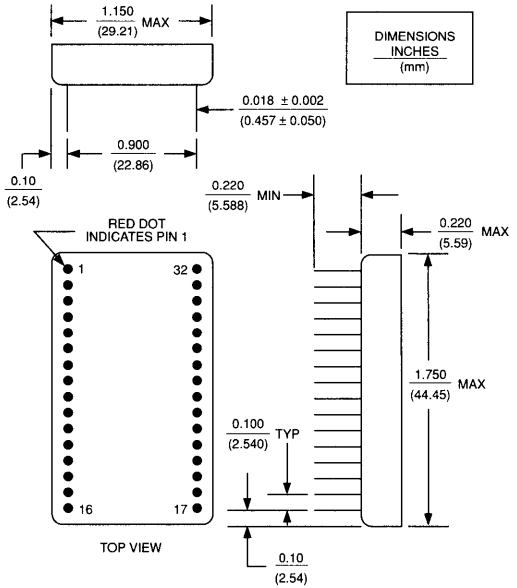
(Typical @ +25°C and rated power supply unless otherwise noted)

SERIES	HS ADC85
POWER SUPPLY	
Requirements	
+15V, Rated	+14.25 to +15.75V @ 28 mA (max)
-15V, Rated	-14.25V to +15.75V @ 30 mA (max)
+5V, Rated	+4.75V to +5.25V @ 91 mA (max)
Rejection Ratio	
+15V Supply	±0.005% F.S.R./% Vs
-15V Supply	±0.002% F.S.R./% Vs
+5V Supply	±0.002% F.S.R./% Vs
Power Consumption	1.32W (max)
TEMPERATURE	
Operating	-55°C to +125°C B Version 0°C to 70°C C Version
MECHANICAL	
Case Style	32-Pin Hermetic Metal

NOTES

1. For 20V step to 0.01%, Settling Time adds to Conversion Time when buffer is connected to input.
2. DTL/TTL compatible, i.e. logic "0" = 0.8V max, logic "1" = 2.0V min., for inputs and, for digital outputs, logic "0" = +0.4V max. and logic "1" = 2.4V min.
3. See TIMING DIAGRAM under APPLICATIONS INFORMATION.
4. HS ADC85 can accept external clock. See TIMING DIAGRAM under APPLICATIONS INFORMATION.
5. Externally adjustable, see OPTIONAL OFFSET AND GAIN ADJUSTMENTS under APPLICATIONS INFORMATION.

CASE ENVELOPE DIMENSIONS



PIN ASSIGNMENTS

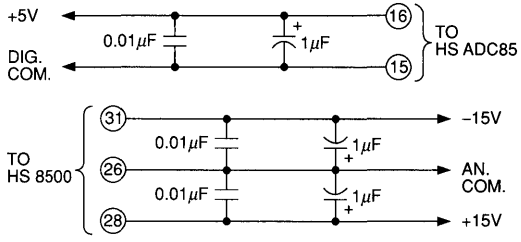
PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 (LSB)	32	SERIAL OUT
2	BIT 11	31	-15V
3	BIT 10	30	BUFFER IN
4	BIT 9	29	BUFFER OUT
5	BIT 8	28	+15V
6	BIT 7	27	GAIN ADJ.
7	BIT 6	26	ANALOG GND.*
8	BIT 5	25	20V RANGE
9	BIT 4	24	10V RANGE
10	BIT 3	23	BIPOLAR OFFSET
11	BIT 2	22	COMPARATOR IN
12	BIT 1 (MSB)	21	START
13	$\overline{\text{BIT 1 (MSB)}}$	20	STATUS
14	SHORT CYCLE	19	CLOCK OUT
15	DIGITAL GND.*	18	REF OUT
16	+5V	17	CLOCK RATE CONTROL**

* DIGITAL GND (Pin 15), and ANALOG GND (Pin 26), should be tied together as close to the unit as possible. If these grounds must be run separately, use a wide conductor pattern, and a non-polarized 0.01 µF to 0.1 µF bypass capacitor between the two.

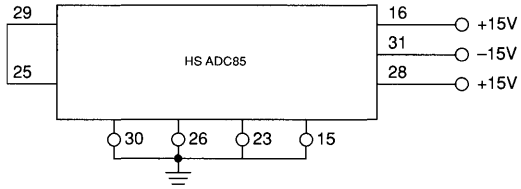
** See APPLICATIONS INFORMATION for connections.

APPLICATIONS INFORMATION

RECOMMENDED POWER SUPPLY BYPASS CIRCUIT



RECOMMENDED BURN-IN CIRCUIT (Standard for MIL-STD-883 Versions)

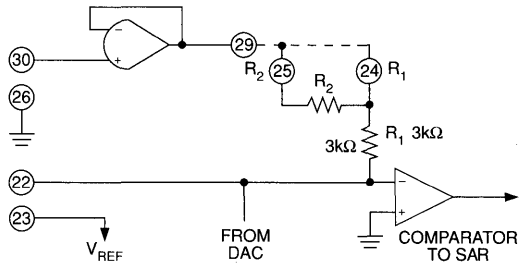


INPUT RANGE SCALING

To maximize signal resolution using the HS ADC85, the analog input should be scaled as close to the maximum input signal range as possible. The analog input can be connected through an internal buffer amp (pin 30) or directly to the converter (pin 24 or 25). Be sure to ground pin 30 if the internal buffer amp is not used. Use the table below for the necessary pin jumping for various input scales.

INPUT SIGNAL RANGE	OUTPUT CODE	BUFFERED OR DIRECT INPUT		BUFF. INPUT ONLY	DIR. INPUT ONLY
		PIN 23 TO PIN	PIN 25 TO	PIN 29 TO PIN	INPUT TO PIN
±10V	COB, CTC	22	INPUT	25	25
±5V	COB, CTC	22	OPEN	24	24
±2.5V	COB, CTC	22	PIN 22	24	24
0 TO +5V	CSB	26	PIN 22	24	24
0 TO +10V	CSB	26	OPEN	24	24

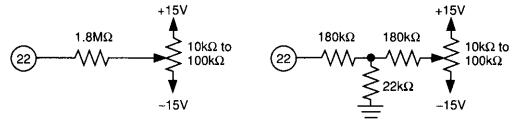
Note: COB is Complementary Offset Binary Coding
CTC is Complementary Two's Complement Coding
CSB is Complementary Straight Binary Coding



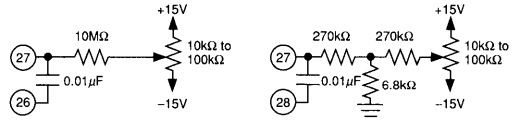
OPTIONAL OFFSET AND GAIN ADJUSTMENTS

External GAIN and OFFSET trim potentiometers may be used to adjust HS ADC85 Series gain and offset errors. A multiturn potentiometer with 100 ppm/°C or better TCR of any value from 10 kΩ to 100 kΩ is suggested. Typical optional adjustment circuits offering adjustment ranges of 0.4% and 0.6% of Full Scale respectively for OFFSET and GAIN are shown below.

OFFSET ADJUST



GAIN ADJUST



CALIBRATION PROCEDURE (For CSB Unipolar and COB Bipolar Codes)

Unipolar

1. Apply a +1/2 LSB analog input and adjust the OFFSET ADJ. potentiometer (pin 22) for a digital output that alternates between 111 . . . 11 and 111 . . . 10.
2. Apply a (FS -3/2 LSB) analog input and set the GAIN ADJ. potentiometer (pin 27) for a digital output that alternates between 000 . . . 01 and 000 . . . 00.

Bipolar

1. Apply a (-FS +1/2 LSB) analog input and adjust the OFFSET ADJ. potentiometer (pin 22) for a digital output that alternates between 111 . . . 11 and 111 . . . 10.
2. Apply a (FS -3/2 LSB) analog input and adjust the GAIN ADJ. potentiometer (pin 27) for a digital output that alternates between 000 . . . 01 and 000 . . . 00.

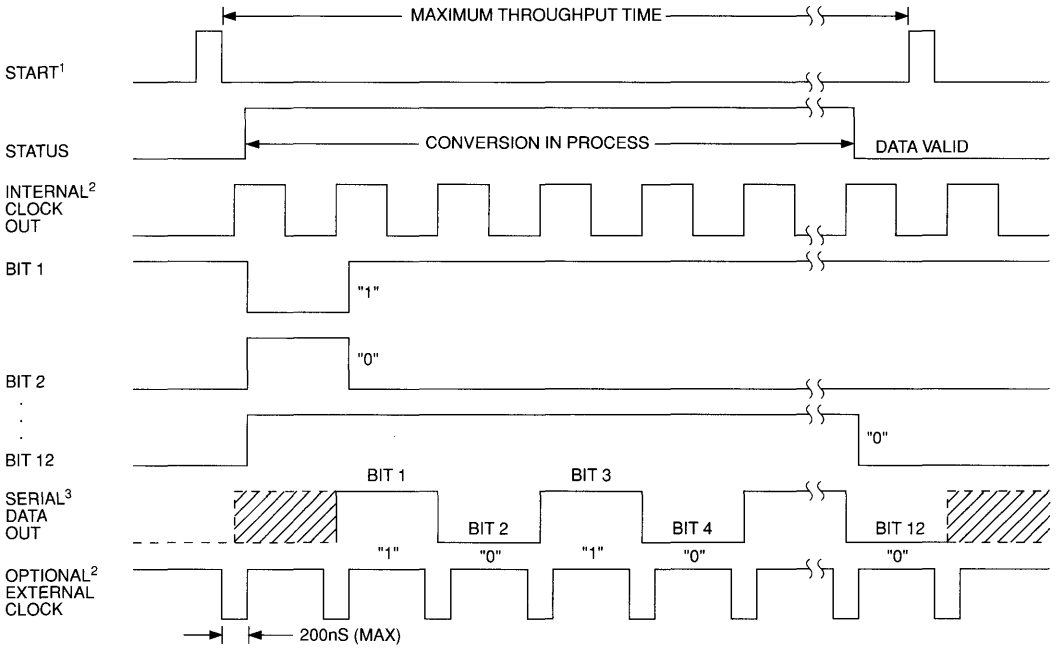
TRANSFER CHARACTERISTICS

UNIPOLAR[1] INPUT VOLTAGE RANGES		DIGITAL OUTPUT CODE	BIPOLAR[2] INPUT VOLTAGE RANGES		
0 to +5V	0 to +10V	MSB LSB	±2.5V	±5V	±10V
4.9982	9.9963	0000000000ϕ	2.498V	4.9963V	9.9927V
2.4994	4.9988	ϕϕϕϕϕϕϕϕϕϕ	0.0006V	+0.00122V	-0.00488V
0.006	+0.00122	1111111111ϕ	-2.4994V	-2.4988V	-9.9976V

NOTES

1. CSB (Complementary Straight Binary) Coding is shown for Unipolar Input Ranges.
2. COB (Complementary Offset Binary) Coding is shown for Bipolar Input Ranges. Use MSB (pin 13) in place of MSB (pin 12) for CTC coding. One LSB = (FSR)/4096.
3. The voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting the output bits indicated as ϕ will change from "1" to "0" or from "0" to "1" as the input voltage passes through the level indicated.

TIMING DIAGRAM



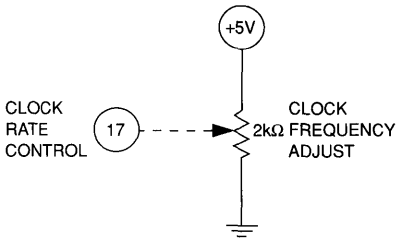
NOTES:

1. CONVERSION IS INITIATED BY THE TRAILING EDGE OF THE START INPUT. THE PULSE MUST HAVE A MINIMUM DURATION OF 50nS AND MUST REMAIN LOW DURING A CONVERSION.
2. WHEN USING AN EXTERNAL CLOCK TO SPEED UP CONVERSIONS, PERFORMANCE WILL BE DECREASED AND LINEARITY ERROR CAN BE GREATER THAN ±1/2 LSB.
3. USE TRAILING EDGE OF CLOCK TO STROBE SERIAL OUTPUT.

CLOCK RATE CONTROL

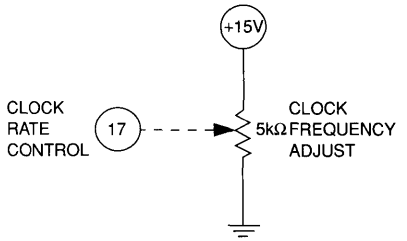
Higher conversion speed may be obtained by connecting the CLOCK RATE CONTROL to an external multi-turn trim potentiometer with a TCR of ±100 ppm/°C or less. Configurations for 8, 10 and 12 bit resolution are shown below. If these alternate adjustments are used, delete the connections for pin 17 shown in the table for SHORT CYCLE connections.

12 BIT RESOLUTION



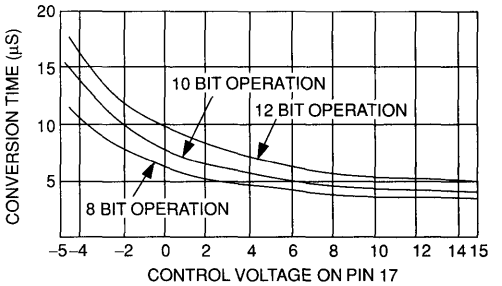
RANGE OF ADJUSTMENT IS 10μs TO 6.8μs

8 OR 10 BIT RESOLUTION



RANGE OF ADJUSTMENT IS TYPICALLY 7.5μs TO 4.0μs FOR 10 BIT AND 6.5μs TO 3.5μs FOR 8 BIT RESOLUTIONS.

CONVERSION TIME VS. CLOCK RATE CONTROL VOLTAGE



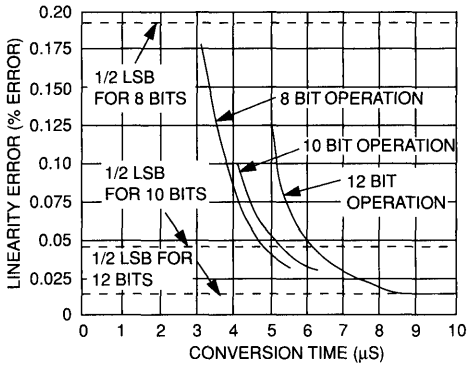
SHORT CYCLING

For applications where lower bit resolution can be tolerated, connecting the "short cycle" input, pin 14, as shown in the following table, will result in shorter conversion time.

CONVERSION TIME VS. BIT RESOLUTION

Resolution (Bits)	12	10	8
Maximum Conversion Time (μS) (1)	10	8	4
Maximum Nonlinearity at 25°C (% of F.S.R.)	0.012	0.048	0.20
Connect Pin 17 to (2)	Pin 15	Pin 16	Pin 28
Connect Pin 14 to	Pin 16	Pin 2	Pin 4

LINEARITY ERROR VS. CONVERSION TIME



EXTERNAL CLOCK

The HS ADC85 has an internal clock and is able to accept external clocks if synchronism with other system elements is required. Connect the external clock to start (pin 21); the start triggering pulse shown in the timing diagram is not used. A negative going pulse having a width of 100 to 200 nS must be used to accomplish external clocking. A total of 13 pulses are necessary to perform conversion; the falling edge of the following pulse will initiate a new conversion.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS ADC85C	Commercial
HS ADC85B	Per MIL-STD-883 Rev. C, Level B

Specifications subject to change without notice.

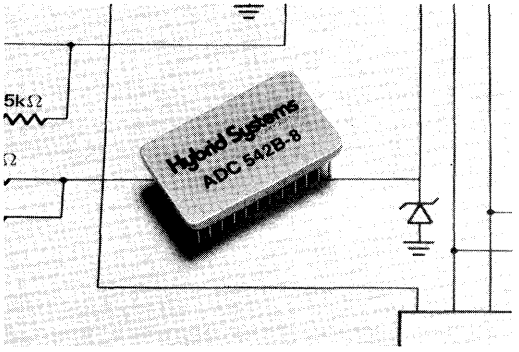
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

ADC541/542

8-BIT, WIDE TEMPERATURE, 2.5μS ADCs

FEATURES

- 2.5μS conversion time
- Low power: 650mW
- Wide temperature range models: −55°C to +125°C operation
- MIL-STD-883 or commercial/industrial processing
- Plug-in replacements for ADC82



DESCRIPTION

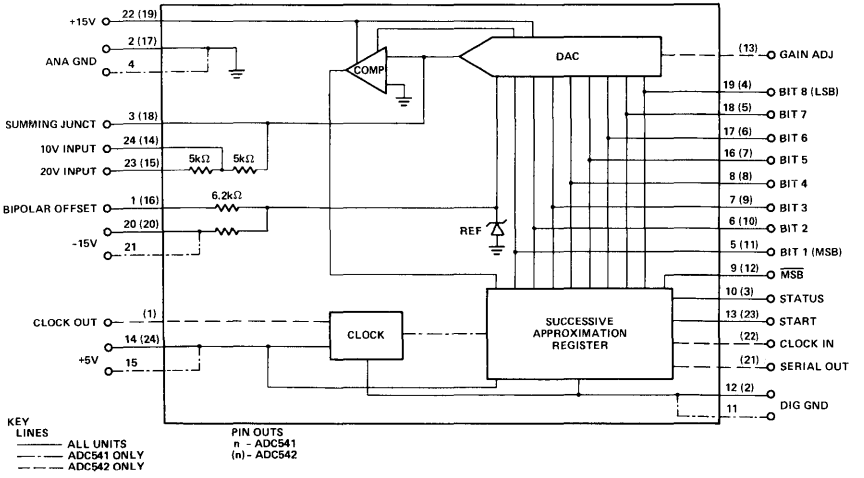
The ADC541/542 Series are fast, low power, hybrid IC analog-to-digital converters (ADCs). The series features 8-bit resolution and accuracy with 2.5μS typical conversion time. The low power drain of 650 mW is from standard ±15 VDC and +5 VDC power supplies. All models are hermetically-sealed in 24-pin DIP style packages and are complete with precision thin-film DAC, clock, comparator, reference and successive approximation register.

The ADC541C-8 and ADC542C-8 are processed to commercial/industrial standards and operate −25°C to +85°C. ADC541B-8 and ADC542B-8 are processed to MIL-STD-883 Rev. C, Level B requirements, and operate −55°C to +125°C. In addition, the ADC542 versions are plug-in replacements for the ADC82.

All models can be externally pin-connected for 3 unipolar and 3 bipolar input ranges. Output coding in the bipolar mode is user selectable as either offset binary or 2's complement. ADC541/542 feature an overall temperature coefficient of ±45 ppm/°C and long-term stability of 0.1%/year.

ADC541/542 models provide systems designers with greater flexibility, savings in space and weight, and the ultimate in reliability. Their compact size, 8-bit resolution, accuracy and extensive self-contained features are particularly well suited to microprocessor applications.

FUNCTIONAL DIAGRAM

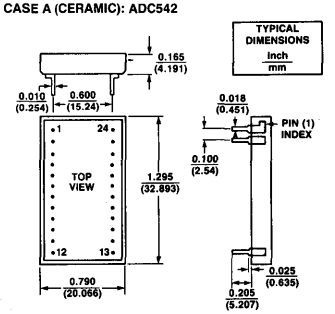


SPECIFICATIONS

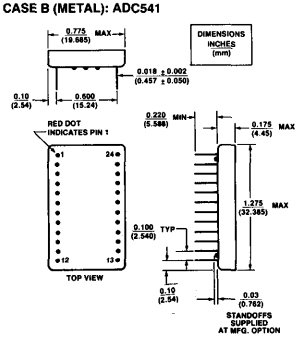
(Typical @ +25°C and nominal power supplies unless otherwise noted)

SERIES	**ADC541/542**
RESOLUTION	8-Bits
TYPE	*Successive Approximation*
ANALOG INPUT	
Unipolar	0 to +5V, 0 to +10V, 0 to +20V
Bipolar	±2.5V, ±5V, ±10V
Impedance	500Ω/Volt
DIGITAL INPUTS	
Start Command Pulse Input	100nS wide, min. Logic "1" > +2.0V; Logic "0" < +0.8V
Logic Loading	2 TTL Loads
Clock In (ADC542 only)	2 TTL Loads
DIGITAL OUTPUTS	
Data Coding, ADC541	Parallel Outputs Only
Unipolar	Binary
Bipolar	2's Complement, Offset Binary
Data Coding, ADC542	Parallel and Serial Outputs
Unipolar	Complementary Binary
Bipolar	Complementary Offset Binary, Complementary 2's Complement
Data Output Drive Capability	3 TTL Loads Logic "1" > +2.4V Logic "0" < 0.4V
Status Output Drive Capability	2 TTL Loads, Logic "1" during conversion
Clock Out (ADC542 only)	
Frequency	2.85 MHz
REFERENCE	Internal
CONVERSION TIME/ THROUGHPUT RATE	2.5μS, typ; 2.8μS max/400 kHz
ACCURACY	
Quantization	±½ LSB max
Linearity	±0.2% of F.S.R. max
Offset, Unipolar and Bipolar[1]	±0.2% of F.S.R. max
Gain[1]	±0.2% of F.S.R. max
STABILITY	
Over Specified Temperature Range	
Linearity	±10ppm/°C
Gain	±40ppm/°C
Offset	±10ppm/°C
Transfer Accuracy[2]	±45ppm/°C
Long Term	±0.1%/year @ +25°C
POWER SUPPLY	
Requirements	
+15V ±3%	20mA max
-15V ±3%	12mA max
+5V ±5%	105mA max
Rejection Ratio	0.05%/% (+15V); 0.01%/% (-15V)
Power Consumption	1W max
TEMPERATURE RANGE	
Specified	
ADC541C/542C	0° to 70°C
ADC541B/542B	-55°C to +125°C
Storage, All Models	-65°C to +150°C
MECHANICAL	
Case Style	Case A (ceramic): ADC542
Case Envelope Dimensions	Case B (metal): ADC541

CASE A (CERAMIC): ADC542



CASE B (METAL): ADC541



Pin Assignments

ADC541

PIN	FUNCTION	PIN	FUNCTION
1	BIPOLAR OFFSET	24	+10V INPUT
2	ANALOG GND	23	+20V INPUT
3	SUMMING JCT.	22	+15V
4	ANALOG GND	21	-15V
5	BIT 1 (MSB)	20	-15V
6	BIT 2	19	BIT 8 (LSB)
7	BIT 3	18	BIT 7
8	BIT 4	17	BIT 6
9	BIT 1 (MSB)	16	BIT 5
10	STATUS	15	+5V
11	DIGITAL GND	14	+5V
12	DIGITAL GND	13	START

ADC542

PIN	FUNCTION	PIN	FUNCTION
1	CLOCK OUT	24	+5V
2	DIGITAL GND	23	START
3	STATUS	22	CLOCK IN
4	Bit 8 (LSB)	21	SERIAL OUT
5	Bit 7	20	-15V
6	Bit 6	19	+15V
7	Bit 5	18	SUMMING JCT
8	Bit 4	17	ANALOG GND
9	Bit 3	16	BIPOLAR OFFSET
10	Bit 2	15	20V INPUT
11	Bit 1 (MSB)	14	10V INPUT
12	Bit 1 (MSB)	13	GAIN ADJUST

NOTES

1. Initial offset and gain errors are externally adjustable. See APPLICATIONS INFORMATION.
2. Includes effects of Linearity, offset, and gain errors.

ORDERING INFORMATION

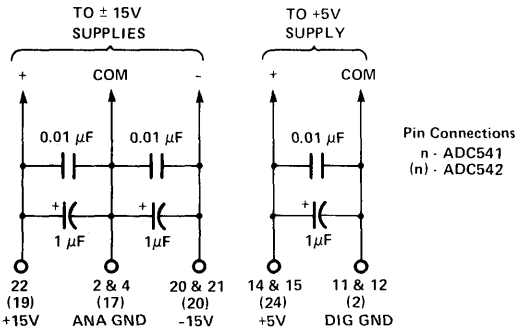
MODEL	DESCRIPTION
ADC541C-8	Commercial/Industrial Process
ADC541B-8	MIL-STD-883 Rev. C, Level B Process
ADC542C-8	Commercial/Industrial Process; ADC82 Pin Out Compat.
ADC542B-8	MIL-STD-883 Rev. C, Level B Process; ADC82 Pin Out Compat.

Specifications subject to change without notice.

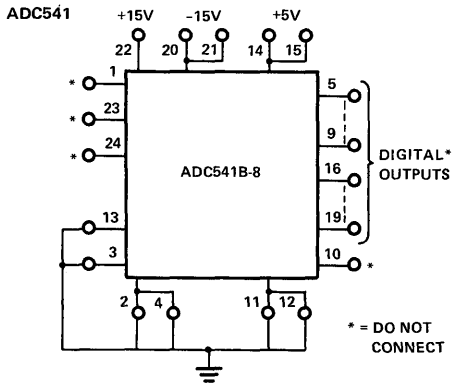
Pin 1 is marked by a dot on the top of the package.

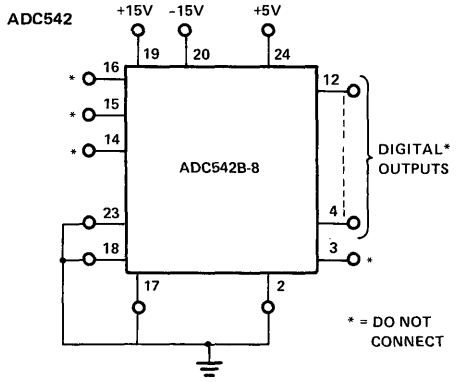
APPLICATIONS INFORMATION

RECOMMENDED POWER SUPPLY BYPASS CIRCUIT

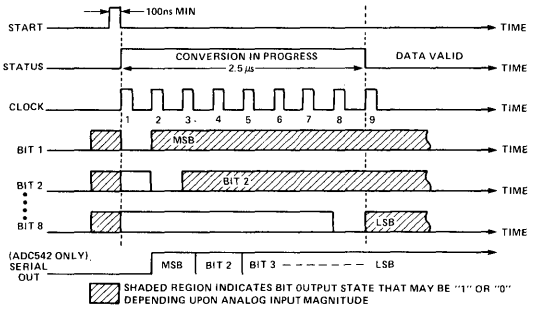


RECOMMENDED BURN-IN CIRCUITS
(Standard for MIL-STD-883 Versions)





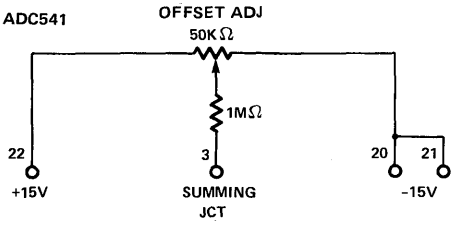
TIMING DIAGRAM



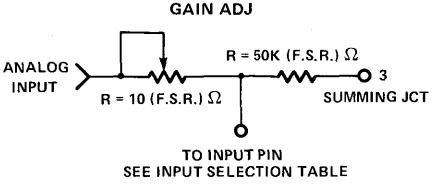
INPUT SELECTION

INPUT VOLT. RANGE	ADC541 PIN CONNECTIONS	ADC541 INPUT PIN	ADC542 PIN CONNECTIONS	ADC542 INPUT PIN
0 to +5V	23 to 3 & 1 to 2	24	16 to 17 & 15 to 18	14
±2.5V	23 to 3 & 1 to 3		16 to 18 & 15 to 18	
0 to +10V	1 to 2	24	16 to 17	14
±5V	1 to 3		16 to 18	
0 to +20V	1 to 2	23	16 to 17	15
±10V	1 to 3		16 to 18	

OPTIONAL ADJUSTMENTS



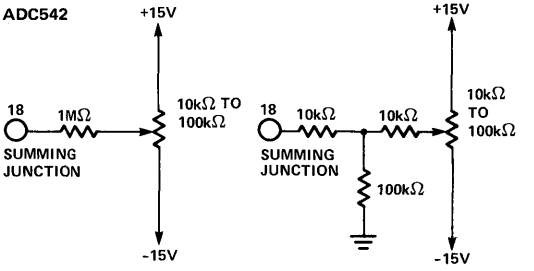
Unipolar: Apply a +½LSB analog input and set the potentiometer for a digital output that alternates between 000...0 and 000...1.
Bipolar: The bipolar offset is factory calibrated and requires no external adjustment.



Unipolar & Bipolar: Apply a +(F.S. -3/2LSB) analog input and set the potentiometer for a digital output that alternates between 111...0 and 111...1.

OPTIONAL ADJUSTMENTS (continued)

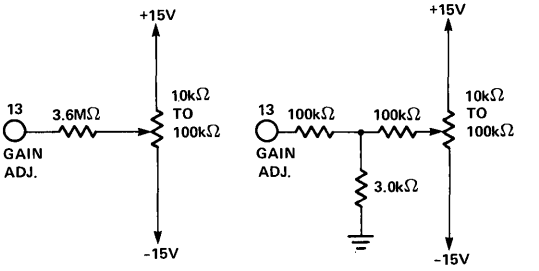
OFFSET ADJ



Two Methods Offering A ±1% Swing.

Unipolar: Apply a +½LSB analog input and set the potentiometer for a digital output that alternates between 111...1 and 111...0.
Bipolar: No adjustments necessary.

GAIN A



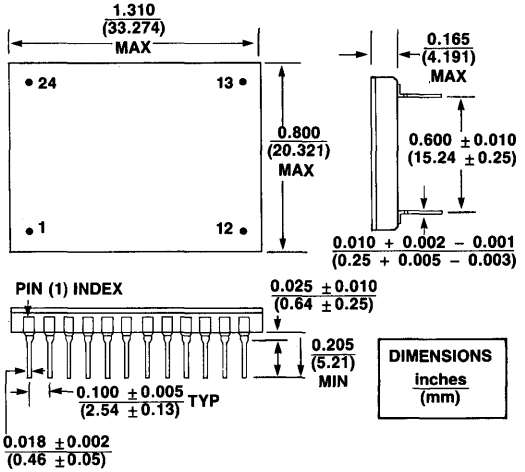
Two Methods Offering A ±1% Swing.

Unipolar & Bipolar: Apply a +(F.S. -3/2LSB) analog input and set the potentiometer for a digital output that alternates between 000...0 and 000...1.

INPUT VOLTAGES, TRANSITION VALUES, LSB VALUES AND CODE DEFINITIONS

BINARY (BIN) OUTPUT	INPUT VOLTAGE RANGE						
ANALOG INPUT VOLTAGE RANGES	DEFINED AS	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
CODE DEISGNATION		COB or CTC	COB or CTC	COB or CTC	CSB	CSB	CSB
ONE LEAST SIGNIFICANT BIT (LSB)	$\frac{FSR}{2^n}$ n=8	$\frac{20V}{2^n}$ 78.13 mV	$\frac{10V}{2^n}$ 39.06 mV	$\frac{5V}{2^n}$ 19.53 mV	$\frac{10V}{2^n}$ 39.06 mV	$\frac{5V}{2^n}$ 19.53 mV	$\frac{20V}{2^n}$ 78.13 mV
TRANSITION VALUES 541 542 MSB LSB MSB LSB							
111...11ø 000...000	+FULL SCALE	+10V – 1½LSB	+5V – 1½LSB	+2.5V – 1½LSB	+10V – 1½LSB	+5V – 1½LSB	+20V – 1½LSB
øøø...øøø øøø...øøø	MID SCALE	– ½LSB	– ½LSB	– ½LSB	+5V – ½LSB	+2.5V – ½LSB	+10V – ½LSB
000...000 111...11ø	–FULL SCALE	–10V + ½LSB	–5V + ½LSB	–2.5V + ½LSB	0 + ½LSB	0 + ½LSB	0 + ½LSB

NOTES:
1. Codings shown for ADC541 are Binary and Offset Binary. Use MSB for 2's Complement Coding.
2. Codings shwon for ADC542 are Complementary Binary and Complementary Offset Binary. Use MSB for Complementary 2's Complement Coding.
3. One LSB = FSR/256.
4. The voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting the output bits indicated as ø will change from "1" to "0" or from "0" to "1" as the input voltage passes through the level indicated.

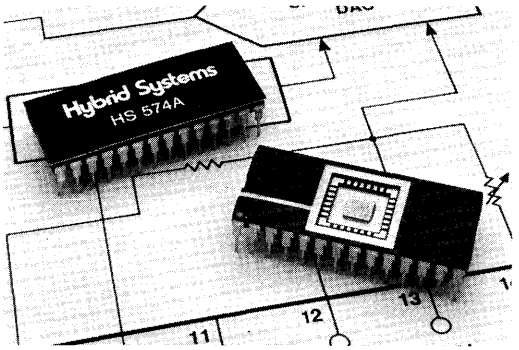


Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

COMPLETE 12-BIT, 25μSEC A/D CONVERTER WITH μP INTERFACE

FEATURES

- Complete 12-bit A/D converter with sample-hold, reference, clock, and three state outputs
- Low power dissipation: 150mW max
- 12-bit linearity over temperature
- Fast conversion time: 25μSec max
- Monolithic construction



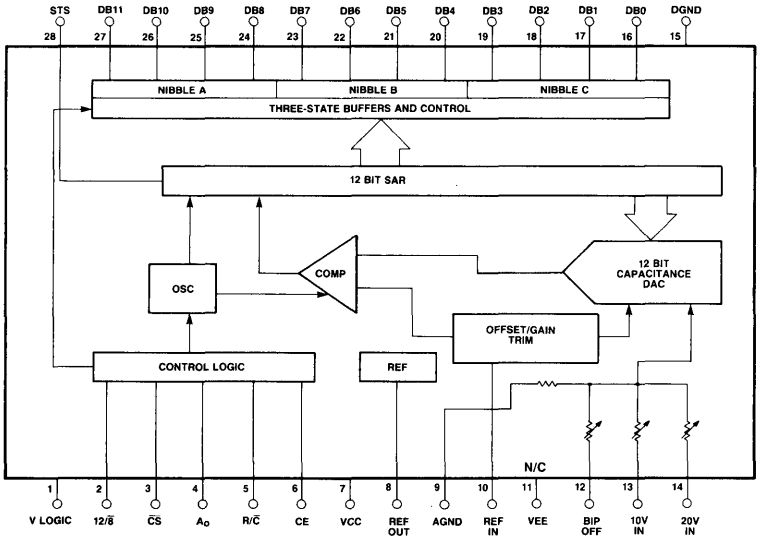
DESCRIPTION

The HS574A is a complete 12-bit successive-approximation A/D converter with three-state output buffers for direct interface to 8-, 12- or 16-bit microprocessor buses. The device is integrated on a single die and includes an internal reference, clock and a sample-hold.

The HS574A has standard bipolar and unipolar input ranges of 10V and 20V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy. Power requirements are +5V and +12V to +15V with a maximum dissipation of 150mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative supply is not required. Conversion time of 25μSec (max) is also featured.

The HS574A is available in 9 product grades. The HS574AJ, AK and AL are specified over a 0°C to +70°C temperature range; the HS574AA, AB and AC: −40°C to +85°C; and the HS574AS, AT and AU: −55°C to +125°C. Processing in accordance with MIL-STD-883C is also available.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

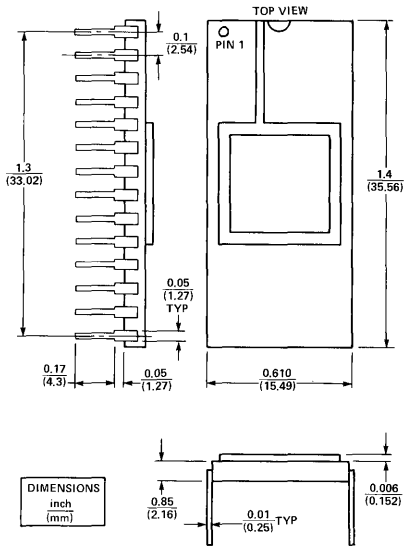
(Typical @ +25°C with V_{CC} = +15V, V_{EE} = 0V, V_{LOGIC} = +5V unless otherwise specified)

MODEL	HS 574AJ	HS 574AK	HS 574AL	HS 574AS	HS 574AT	HS 574AU
RESOLUTION (max)	12 Bits	*	*	*	*	*
TYPE	Successive Approximation	*	*	*	*	*
ANALOG INPUTS						
Input Ranges						
Bipolar	±5V, ±10V	*	*	*	*	*
Unipolar	0 to +10V, 0 to +20V	*	*	*	*	*
Input Impedance						
10 Volt Span	3.75kΩ min, 6.25kΩ max	*	*	*	*	*
20 Volt Span	15kΩ min, 25kΩ max	*	*	*	*	*
DIGITAL INPUTS						
Logic Inputs						
CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$						
Logic 1	+2.4V min, +5.5V max	*	*	*	*	*
Logic 0	−0.3V min, +0.8V max	*	*	*	*	*
Current						
−0.3V to 5.5V Input	±0.1μA typ, ±50μA max	*	*	*	*	*
0 to 5.5V Input	±5μA max	*	*	*	*	*
Capacitance	5pF	*	*	*	*	*
Control Input, 12/$\overline{8}$	Hardwire to V_{LOGIC} or DIG COM	*	*	*	*	*
DIGITAL OUTPUTS						
Logic Outputs						
DB_{11}-DB_0, STS						
Logic 0	+0.4V max, I_{SINK} ≤1.6mA	*	*	*	*	*
Logic 1	+2.4V min, I_{SOURCE} ≤ 500μA	*	*	*	*	*
Leakage (High Z State)	±40μA max (Data Bits Only)	*	*	*	*	*
Capacitance	5pF	*	*	*	*	*
Parallel Data						
Output Codes						
Unipolar	Positive True Binary	*	*	*	*	*
Bipolar	Positive True Offset Binary	*	*	*	*	*
REFERENCE						
Internal	10.00 ±0.1 Volts max	*	*	*	*	*
Output Current[1]	2mA	*	*	*	*	*
CONVERSION TIME						
12-bit	13μSec min, 25μSec max	*	*	*	*	*
8-bit	10μSec min, 19μSec max	*	*	*	*	*
ACCURACY						
Linearity Error @25°C	±1 LSB	±½ LSB	±½ LSB	±1 LSB	±½ LSB	±½ LSB
(t_{min} to t_{max})	±1 LSB	±½ LSB	±½ LSB	±1 LSB	±½ LSB	±½ LSB
Differential Linearity Error[2] @25°C	11 Bits	12 Bits	12 Bits	11 Bits	12 Bits	12 Bits
(t_{min} to t_{max})	11 Bits	12 Bits	12 Bits	11 Bits	12 Bits	12 Bits
Offset[3]						
Unipolar	±2 LSB	*	*	*	*	*
Bipolar	±10 LSB	±4 LSB	±4 LSB	±10 LSB	±4 LSB	±4 LSB
Full Scale Calibration Error (% of FSR)						
Fixed 50Ω resistor from REF OUT to REF IN	0.3%	*	*	*	*	*
No Adjustment at +25°C t_{min} to t_{max}	0.5%	0.4%	0.35%	0.8%	0.6%	0.4%
With Adjustment at +25°C t_{min} to t_{max}	0.22%	0.12%	0.05%	0.5%	0.25%	0.12%
STABILITY						
Unipolar Offset (ppm/°C max)						
0°C to +70°C	±10	±5	±5			
−55°C to +125°C				±5	±2.5	±2.5
Bipolar Offset (ppm/°C max)						
0°C to +70°C	±10	±5	±5			
−55°C to +125°C				±10	±5	±2.5
Gain (Scale Factor)(ppm/°C max)						
0°C to +70°C	±50	±27	±10			
−55°C to +125°C				±50	±25	±12.5
POWER SUPPLY						
V_{LOGIC}	+4.5 to +5.5 Volts @ 3mA	*	*	*	*	*
V_{CC}	+11.4 to +16.5 Volts @ 9mA	*	*	*	*	*
Power Dissipation	110mW typ, 150mW max	*	*	*	*	*
POWER SUPPLY REJECTION						
Max. change in full scale calibration						
+13.5V ≤ V_{CC} ≤ +16.5V or +11.4V ≤ V_{CC} ≤ 12.6V	±2 LSB	±1 LSB	±1 LSB	±2 LSB	±1 LSB	±1 LSB
+4.5V ≤ V_{LOGIC} ≤ +5.5V	±½ LSB	*	*	*	*	*
TEMPERATURE RANGE						
Operating	0°C to +70°C	*	*	−55°C to +125°C	**	**
Storage	−25°C to +85°C	*	*	−65°C to +150°C	**	**

NOTES: 1. Available for external loads. External load should not change during conversion. When supplying an external load and operating on a +12V supply, a buffer amplifier must be provided for the reference output. 2. Minimum resolution for which no missing codes are guaranteed. 3. Externally adjustable to zero. See applications information.

*Specifications same as HS 574AJ. **Specifications same as HS 574AS.

PACKAGE OUTLINE



NOTE: See ordering information for Leadless Chip Carrier & CERDIP package outline. Sipex reserves the right to ship CERDIP in lieu of ceramic package.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	V_{LOGIC}	28	STS
2	12/8	27	DB_{11} (MSB)
3	CS	26	DB_{10}
4	A_0	25	DB_9
5	R/C	24	DB_8
6	CE	23	DB_7
7	V_{CC}	22	DB_6
8	REF OUT	21	DB_5
9	ANA GND(AC)	20	DB_4
10	REF IN	19	DB_3
11	N/C*	18	DB_2
12	BIP OFF	17	DB_1
13	$10V_{IN}$	16	DB_0 (LSB)
14	$20V_{IN}$	15	DIGITAL GND

*This pin is not connected inside the device so it can be tied to −15V, ground, or left floating.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common . . . . . 0 to +16.5V
V_{LOGIC} to Digital Common . . . . . 0 to +7V
Analog Common to Digital Common . . . . . ±1V
Control Inputs (CE, CS, A_0, 12/8, R/C) to Digital Common . . . . . −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common . . . . . ±16.5V
$20V_{IN}$ to Analog Common . . . . . ±24V
REF OUT . . . . . Indefinite short to common
Momentary short to V_{CC}
Power Dissipation 1000mW
Lead Temperature, Soldering . . . . . 300°C, 10Sec
J/C . . . . . 45°C/W
MTBF-25°C Ground Base . . . . . 2.915 million hours
MTBF-125°C Missile Launch . . . . . 10.16 thousand hours

CONVERT MODE TIMING CHARACTERISTICS

Typical @25°C, V_{CC} = +15V or +10V, V_{LOGIC} = +5V, V_{EE} = 0V, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS[1]	MIN	MAX	UNITS
t_{DSC} STS Delay from CE			200	ns
t_{HEC} CE Pulse Width		50		ns
t_{SSC} CS to CE Setup		50		ns
t_{HSC} CS Low during CE High		50		ns
t_{SRC} R/C to CE Setup		50		ns
t_{HRC} R/C Low during CE High		50		ns
t_{SAC} A_0 to CE Setup		0		ns
t_{HAC} A_0 Valid during CE High		50		ns
t_C Conversion Time				
12-Bit Cycle	T_{min} to T_{max}	13	25	µs
8-Bit Cycle	T_{min} to T_{max}	10	19	µs

NOTE: 1. Time is measured from 50% level of digital transitions. Tested with a 100pF and 3kΩ load for high impedance to drive and tested with 10pF and 3KΩ load for drive to high impedance.

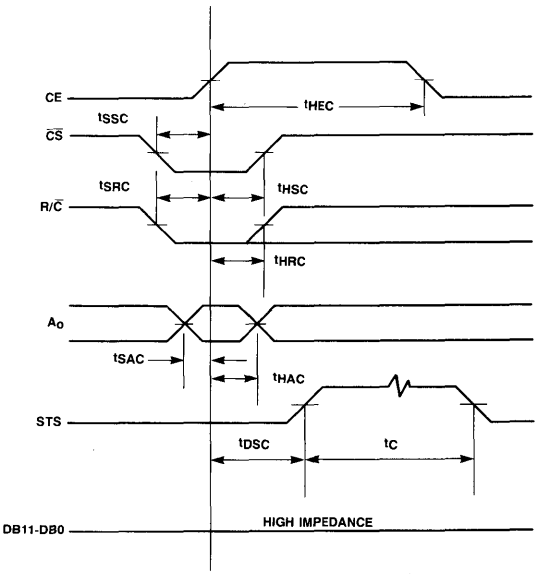


Figure 1. Convert Mode Timing Diagram

READ MODE TIMING CHARACTERISTICS

Typical @25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = 0V, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS
t_{DD} Access Time from CE			150	ns
t_{HD} Data Valid After CE Low	25			ns
t_{HL} Output Float Delay			150	ns
t_{SSR} CS to CE Setup	50	0		ns
t_{SRR} R/C to CE Setup	0	0		ns
t_{SAR} A_0 to CE Setup	50			ns
t_{HRS} CS Valid After CE Low	0	0		ns
t_{HRR} R/C High After CE Low	0	50		ns
t_{HAR} A_0 Valid After CE Low	50			ns
t_{HS} STS Delay After Data Valid	300		1000	ns

9

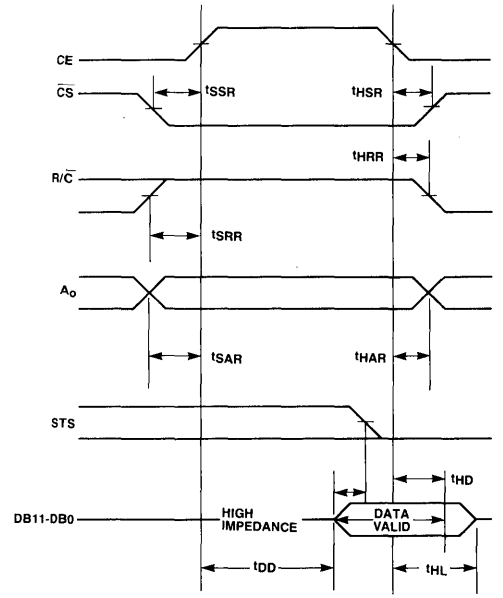


Figure 2. Read Mode Timing Diagram

STAND-ALONE MODE TIMING CHARACTERISTICS

Typical @25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = 0V, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL} Low R/C Pulse Width	50			ns
t_{DS} STS Delay from R/C			200	ns
t_{HDR} Data Valid After R/C Low	25			ns
t_{HS} STS Delay After Data Valid	300		1000	ns
t_{HRH} High R/C Pulse Width	150			ns
t_{DDR} Data Access Time			150	ns

SAMPLE AND HOLD

Acquisition Time[1]	1.8	2.9	4.0	μs
Aperture Uncertainty Time[1]		20		ns

NOTE: 1. Parameter is guaranteed by design and sampled characterization data.

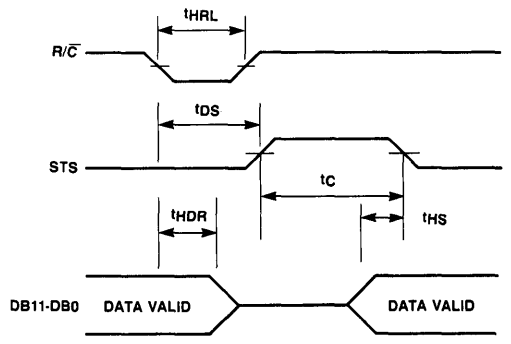


Figure 3. Low Pulse For R/C — Outputs Enabled After Conversion

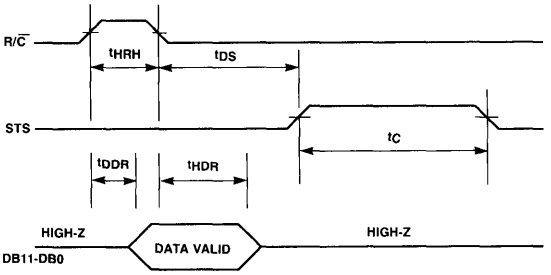


Figure 4. High Pulse For R/C — Outputs Enabled While R/C is High, Otherwise High Impedance

CIRCUIT OPERATION

The HS 574A is a complete 12-bit analog-to-digital converter which consists of a single chip version of the industry standard 574. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive-approximation register (SAR), sample and hold, clock, output buffers and control circuitry to make it possible to use the HS 574A with few external components.

When the control section of the HS 574A initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HS 574A 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to be greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±½ LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2mA to an external load in addition to that required to drive the reference input resistor (1mA) and offset resistor (1mA) when operating with ±15V supplies. If the HS 574A is used with ±12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the HS 574A reference must remain constant during conversion.

The sample and hold is a default function by virtue of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although there is no sample and hold circuit in the classical sense, the sampling nature of the capacitive DAC makes the HS 574A appear to have a built in sample and hold. This sample and hold action substantially increases the signal bandwidth of the HS 574A over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HS 574A is disconnected from the user's sample and hold. This prevents transients occuring during conversion from being inflicted upon the attached sample and hold buffer. All other 574/674 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

Furthermore, the isolation of the input after the acquisition time in the HS 574A allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HS 574A acts as any other 574 device because the internal S/H is transparent. The sample/hold function in the HS 574A is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

The operation of the S/H function is internal to the HS 574A and is controlled through the normal R/C control line (refer to Figure 5.) When the R/C line makes a negative transition, the HS 574A starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as t_{ACQ}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

During t_{ACQ}, the equivalent circuit of the HS 574A input is as shown in Figure 6 (the time constant of the input is independent of which input level is used). This CDAC capacitance must be charged up to the input voltage during t_{ACQ}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12 bits of accuracy during t_{ACQ}. The excess time left during t_{ACQ} allows the user's buffer amp to settle after being switched to the CDAC load.

Note that because the sample is taken relative to the R/C transition, t_{ACQ} is also the traditional "aperture delay" of this internal sample and hold.

Since t_{ACQ} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in t_{ACQ} = 2.9 μsecs $\pm$ 1.1 μsecs between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the HS 574A.

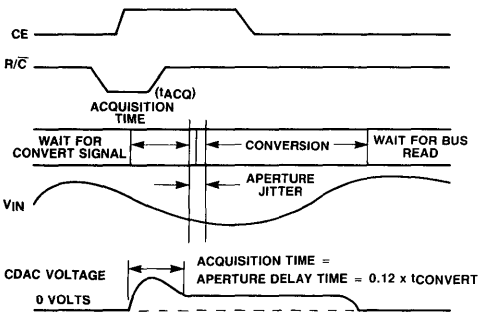


Figure 5. Sample and Hold Function

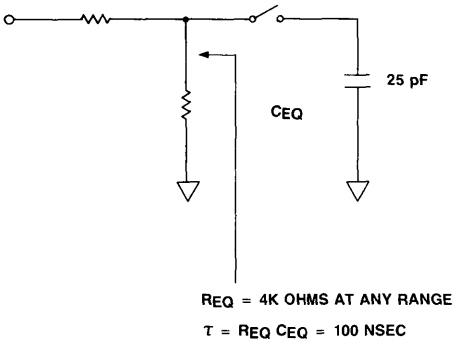


Figure 6. Equivalent HS 574A Input Circuit

APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time the actual sample is taken — i.e. the "aperture jitter" or t_{AJ}. The HS 574A has a nominal aperture jitter of 20 nsecs between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (See Figure 7). The magnitude of this change for a sine wave can be calculated:

Assume a sinusoidal signal, maximum slew rate, $S_R = 2\pi f V_P$ (V_P = peak voltage, f = frequency of sine wave). For an N-bit converter to maintain $\pm$ ½ LSB accuracy:

$V_{ERR} \leq V_{FS}/2^{N+1}$ (where V_{ERR} is the allowable error voltage and V_{FS} is the full scale voltage).

From Figure 10:

$S_R = \Delta V/\Delta T = 2\pi f V_P$

Let $\Delta V = V_{ERR}$, $V_P = V_{IN}/2$ and $\Delta T = t_{AJ}$ (the time during which unwanted voltage change occurs)

The above conditions then yield:

$V_{FS}/2^{N+1} \geq \pi f V_{IN} t_{AJ}$ or $f_{MAX} \leq V_{FS}/(\pi V_{IN} t_{AJ})2^{N+1}$

For the HS 574A, t_{AJ} = 20 nsec; therefore,

$f_{MAX} \leq$ 2kHz

For higher frequency signal inputs, an external sample and hold is recommended.

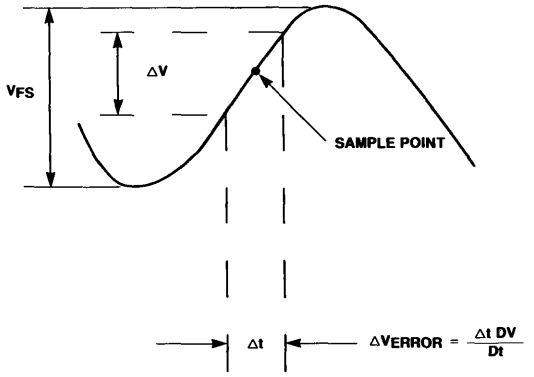


Figure 7. Aperture Uncertainty

TYPICAL INTERFACE CIRCUIT

The HS 574A is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figures 8 and 9. The two typical interface circuits are for operating the HS 574A in either a unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few considerations concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead. If this is not possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HS 574A must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to its respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 μF tantalum and a 0.1 μ F ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HS 574A is being used to upgrade an already existing design.

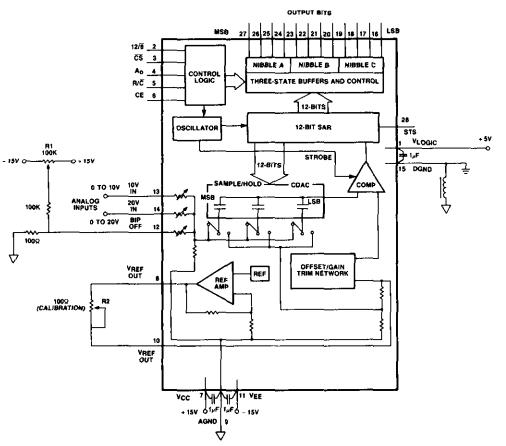


Figure 8. Unipolar Input Connections

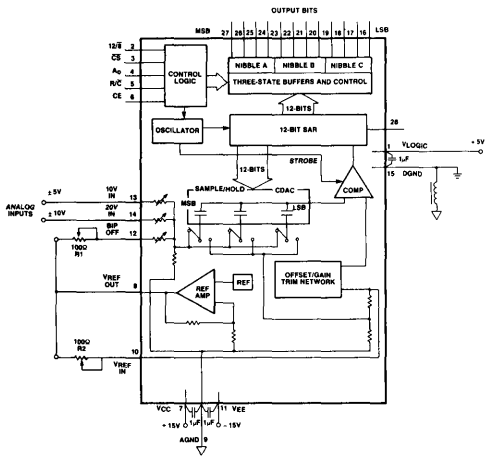


Figure 9. Bipolar Input Connections

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accomodate the ground currents present with this device.

The analog ground current is approximately 6mADC while the digital ground is 3mADC. The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HS 574A may be operated by a μP or in the stand-alone mode. The part has four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 8, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +½ LSB or +1.22mV for the 10V range and +2.44mV for the 20V range should be applied to the HS 574A. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1½ LSB below the nominal full scale which is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0V to 10V range or to pin 14 for the 0V to 20V range.

BIPOLAR

The gain and offset errors listed in the specifications may be adjusted to zero using the potentiometers R1 and R2 (See Figure 9). If adjustment is not needed, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5V range or to pin 14 for a ±10V range. First apply a DC input voltage ½ LSB above negative full scale which is −4.9988V for the ±5V range or −9.9976V for the ±10V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1½ LSB below positive full scale which is +4.9963V for the ±5V range or +9.9927V for the ±10V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

The 100Ω potentiometer R2 provides gain adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (for and LSB of 2.5mV) or 20.48 (for an LSB of 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then to provide gain adjust for the 10.24 range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 1000Ω potentiometer in series with pin 14.

CONTROLLING THE HS 574A

The HS 574A can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/C input pin. Full μP control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 followed by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/8, CS, A_0, R/C and CE. The use of these inputs in controlling the converter's operations is shown in Table 1, and the internal control logic is shown in a simplified schematic in Figure 10.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/C. The other controls must be tied to known states as follows: CE and 12/8 are wired high, A_0 and CS are wired low. The output data arrives in words of 12-bits each. The limits on R/C duty cycle are shown in Figures 3 and 4. It may have duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/C is high unless STS is also high, indicating a conversion is in progress.

CONVERSION LENGTH

A conversion start transition latches the state of A_0 as shown in Figure 10 and Table 1. The latched state determines if the conversion stops with 8-bits (A_0 high) or continues for 12-bits (A_0 low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". A_0 is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

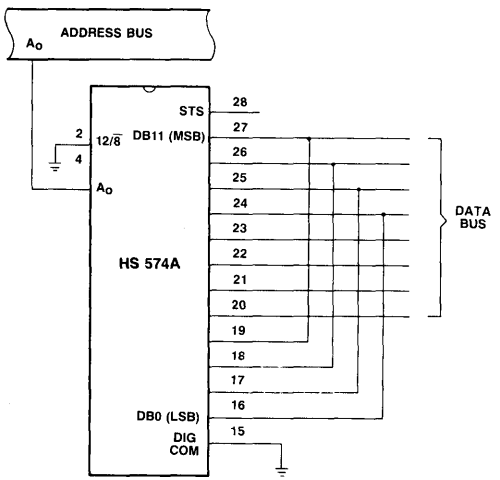


Figure 10. Interfacing the HS 574A to an 8-Bit Data Bus

CONVERSION START

A conversion may be initated by a logic transition on any of the three inputs: CE, CS, R/C, as shown in Table 1. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if A_0 changes state after a conversion begins, an additional Start Convert command will latch the new state of A_0 and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

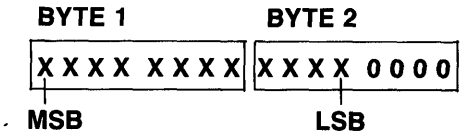
READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/C is high, STS is low, CE is high and CS is low. The data lines become active in response to the four conditions and output data according to the conditions of 12/8 and A_0. The timing diagram for this process is shown in Figure 2. When 12/8 is high, all 12 data outputs become active simultaneously and the A_0 input is ignored. This is for easy interface to a 12 or 16 bit data bus. The 12/8 input is usually tied high or low, although it is TTL/CMOS compatible.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 Bit Conversion
↑	0	0	X	1	Initiate 8 Bit Conversion
1	↓	0	X	0	Initiate 12 Bit Conversion
1	↓	0	X	1	Initiate 8 Bit Conversion
1	0	↓	X	0	Initiate 12 Bit Conversion
1	0	↓	X	1	Initiate 8 Bit Conversion
1	0	1	1	X	Enable 12 Bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Table 1. Truth Table for the HS 574 Control Inputs

When 12/8 is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 10. The A_0 control can be connected to the least significant bit of the data bus in order to store the output data into two consecutive memory locations. When A_0 is pulled low, the 8 MSB's are enabled only. When A_0 is high, the 4 MSB's are disabled, bits 4 through 7 are forced to a zero and the four LSB's are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

A_0 may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 10 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is complete and STS is low. If earlier access is needed, the read can begin no later than the addition of times t_{DD} and t_{HS} before STS goes low.

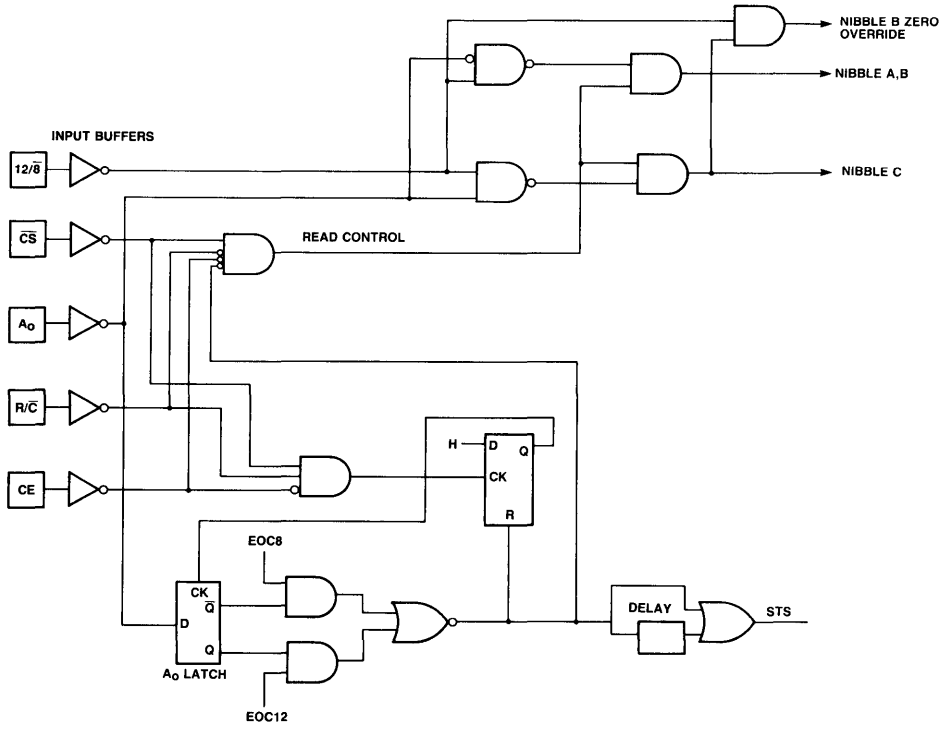


Figure 11. HS 574A Control Logic

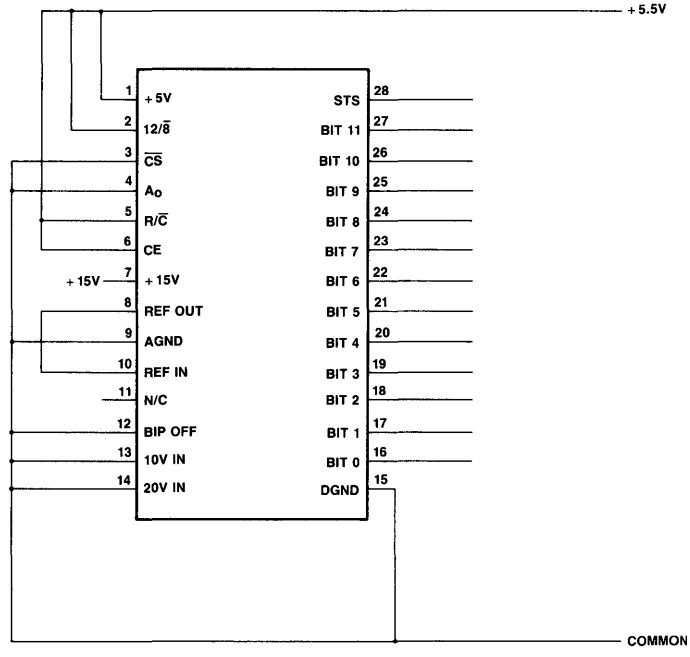


Figure 12. Burn-In Schematic

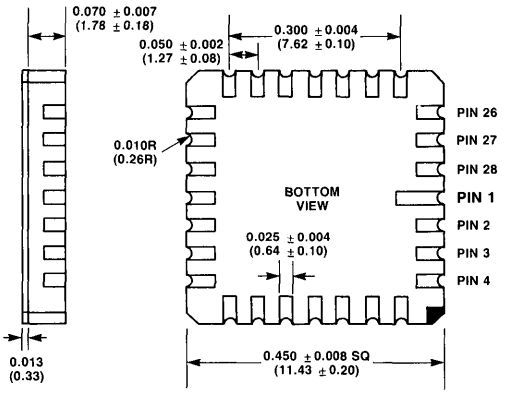
ORDERING INFORMATION

MODEL NUMBER	RESOLUTION NO MISSING CODES (T_{min} to T_{max})	LINEARITY ERROR	MAX FULL SCALE T.C. (ppm/°C)	TEMP. RANGE	MIL SCREENING
HS 574AJ	11 Bits	±1 LSB	50.0	0°C to +70°C	—
HS 574AK	12 Bits	±½ LSB	27.0	0°C to +70°C	—
HS 574AL	12 Bits	±½ LSB	10.0	0°C to +70°C	—
HS 574AA[1]	11 Bits	±½ LSB	50.0	−40°C to +85°C	—
HS 574AB[1]	12 Bits	±½ LSB	27.0	−40°C to +85°C	—
HS 574AC[1]	12 Bits	±½ LSB	10.0	−40°C to +85°C	—
HS 574AS	11 Bits	±1 LSB	50.0	−55°C to +125°C	—
HS 574AT	12 Bits	±½ LSB	25.0	−55°C to +125°C	—
HS 574AU	12 Bits	±½ LSB	12.5	−55°C to +125°C	—
HS 574S/B	11 Bits	±1 LSB	50.0	−55°C to +125°C	MIL-STD-883C
HS 574AT/B	12 Bits	±½ LSB	25.0	−55°C to +125°C	MIL-STD-883C
HS 574AU/B	12 Bits	±½ LSB	12.5	−55°C to +125°C	MIL-STD-883C

NOTE: 1.Electrical specifications for AA, AB, and AC grades are the same as AJ, AK, and AL models, respectively with the exception of extended operating temperature range performance from −40°C to +85°C.

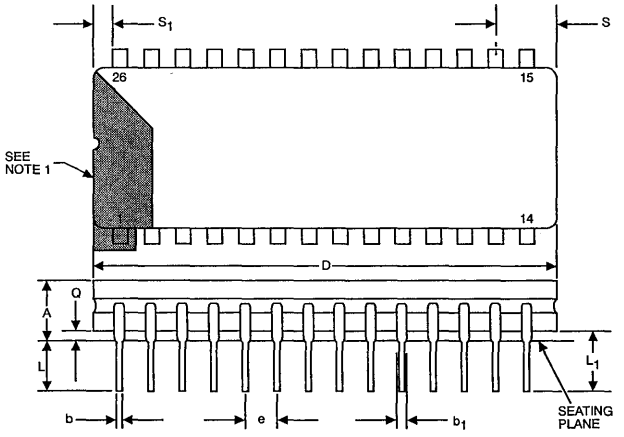
PACKAGE OUTLINE

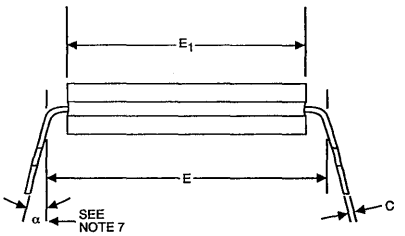
28 Pin Leadless Chip Carrier



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.225		5.72	
b	0.014	0.026	0.36	0.66	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.018	0.20	0.46	7
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015		0.38		3
S		0.100		2.54	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	

NOTE: To order Leadless Chip Carrier version add /LCC suffix to model number.

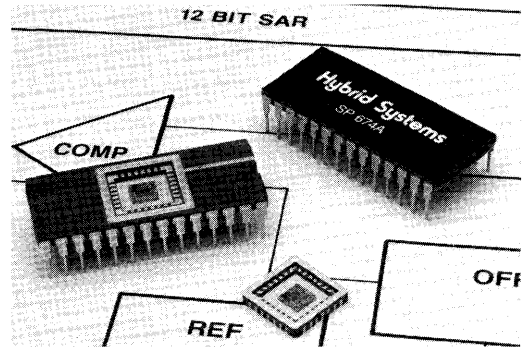




COMPLETE 12-BIT, 15μSEC A/D CONVERTER WITH μP INTERFACE

FEATURES

- Complete 12-bit A/D converter with sample-hold, reference, clock, and three-state outputs
- Low power dissipation: 150mW max
- 12-bit linearity over temperature
- Fast conversion time: 15μsec max
- Monolithic construction



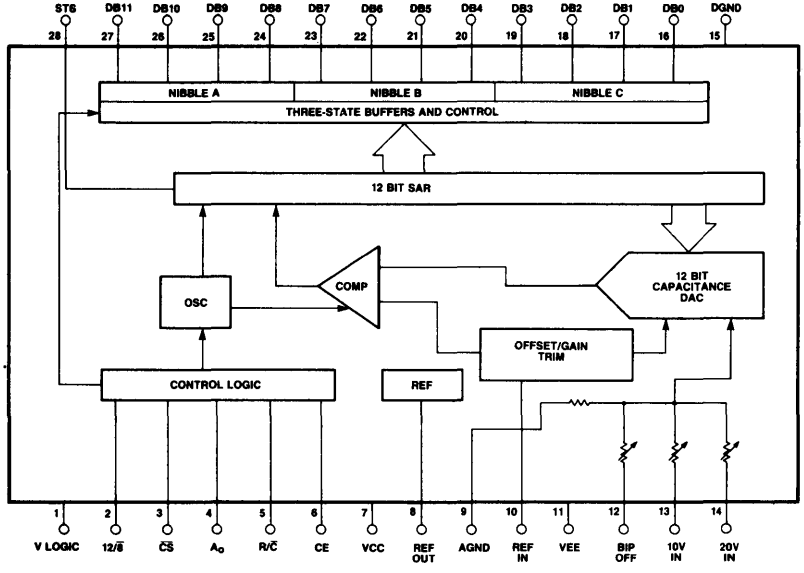
DESCRIPTION

The SP674A is a complete 12-bit successive-approximation A/D converter with three-state output buffers for direct interface to 8-, 12- or 16-bit microprocessor buses. The device is integrated on a single die and includes an internal reference, clock and a sample-hold.

The SP674A has standard bipolar and unipolar input ranges of 10V and 20V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy. Power requirements are +5V and +12V to +15V with a maximum dissipation of 150mW at the specified voltages. Power consumption is about five times lower than currently available devices, and a negative supply is not required. Conversion time of 15μsec max is also featured.

The SP674A is available in 9 product grades. The SP674AJ, AK and AL are specified over a 0°C to +70°C temperature range; the SP674AA, AB and AC: −40°C to +85°C; and the SP674AS, AT and AU: −55°C to +125°C. Processing in accordance with MIL-STD-883C is also available.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

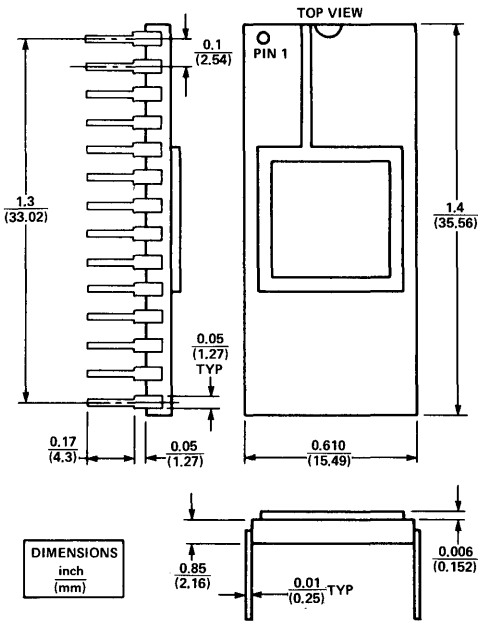
(Typical @ +25°C with V_{CC} = +15V, V_{EE} = 0V, V_{LOGIC} = +5V unless otherwise specified)

MODEL	SP 674AJ	SP 674AK	SP 674AL	SP 674AS	SP 674AT	SP 674AU
RESOLUTION (max)	12 Bits	*	*	*	*	*
TYPE	Successive Approximation	*	*	*	*	*
ANALOG INPUTS						
Input Ranges						
Bipolar	±5V, ±10V	*	*	*	*	*
Unipolar	0 to +10V, 0 to +20V	*	*	*	*	*
Input Impedance						
10 Volt Span	3.75kΩ min, 6.25kΩ max	*	*	*	*	*
20 Volt Span	15kΩ min, 25kΩ max	*	*	*	*	*
DIGITAL INPUTS						
Logic Inputs						
CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$						
Logic 1	+2.4V min, +5.5V max	*	*	*	*	*
Logic 0	−0.5V min, +0.8V max	*	*	*	*	*
Current						
0 to 5.5V Input	±50μA max	*	*	*	*	*
Capacitance	5pF	*	*	*	*	*
DIGITAL OUTPUTS						
Logic Outputs						
DB_{11}-DB_0, STS						
Logic 0	+0.4V max, I_{SINK} 1.6mA	*	*	*	*	*
Logic 1	+2.4V min, I_{SOURCE} 500 μA	*	*	*	*	*
Leakage (High Z State)	±40μA max (Data Bits Only)	*	*	*	*	*
Capacitance	5pF	*	*	*	*	*
Parallel Data						
Output Codes						
Unipolar	Positive True Binary	*	*	*	*	*
Bipolar	Positive True Offset Binary	*	*	*	*	*
REFERENCE						
Internal	10.00 ±0.1 Volts max	*	*	*	*	*
Output Current[1]	2mA	*	*	*	*	*
CONVERSION TIME						
12 Bit	9μSec min, 15μSec max	*	*	*	*	*
8 Bit	6μSec min, 10μSec max	*	*	*	*	*
ACCURACY						
Linearity Error @25°C, max	±1 LSB	±½ LSB	±½ LSB	±1 LSB	±½ LSB	±½ LSB
(t_{min} to t_{max}), max	±1 LSB	±½ LSB	±½ LSB	±1 LSB	±½ LSB	±½ LSB
Differential Linearity Error[2] @25°C, min	11 Bits	12 Bits	12 Bits	11 Bits	12 Bits	12 Bits
(t_{min} to t_{max}), min	11 Bits	12 Bits	12 Bits	11 Bits	12 Bits	12 Bits
Offset[3]						
Unipolar, max	±2 LSB	*	*	*	*	*
Bipolar, max	±10 LSB	±4 LSB	±4 LSB	±10 LSB	±4 LSB	±4 LSB
Full Scale Calibration Error (±% of FSR), max						
Fixed 50 resistor from REF OUT to REF IN	0.3%	*	*	*	*	*
No Adjustment at +25°C t_{min} to t_{max}	0.5%	0.4%	0.35%	0.8%	0.6%	0.4%
With Adjustment at +25°C t_{min} to t_{max}	0.22%	0.12%	0.05%	0.5%	0.25%	0.12%
STABILITY						
Unipolar Offset (ppm/°C max)						
0°C to +70°C	±10	±5	±5			
−55°C to +125°C				±5	±2.5	±2.5
Bipolar Offset (ppm/°C max)						
0°C to +70°C	±10	±5	±5			
−55°C to +125°C				±10	±5	±2.5
Gain (Scale Factor)(ppm/°C max)						
0°C to +70°C	±50	±27	±10			
−55°C to +125°C				±50	±25	±12.5
POWER SUPPLY						
V_{LOGIC}	+4.5 to +5.5 Volts @ 3mA	*	*	*	*	*
V_{CC}	+11.4 to +16.5 Volts @ 9mA	*	*	*	*	*
Power Dissipation	110mW typ, 150mW max	*	*	*	*	*
POWER SUPPLY REJECTION						
Max. change in full scale calibration						
+13.5V ≤ V_{CC} ≤ +16.5V or +11.4V ≤ V_{CC} ≤ 12.6V	±2 LSB	±1 LSB	±1 LSB	±2 LSB	±1 LSB	±1 LSB
+4.5V ≤ V_{LOGIC} ≤ +5.5V	±½ LSB	*	*	*	*	*
TEMPERATURE RANGE						
Operating	0°C to +70°C	*	*	−55°C to +125°C	**	**
Storage	−25°C to +85°C	*	*	−65°C to +150°C	**	**

NOTES: 1. Available for external loads. External load should not change during conversion. When supplying an external load and operating on a +12V supply, a buffer amplifier must be provided for the reference output. 2. Minimum resolution for which no missing codes are guaranteed. 3. Externally adjustable to zero. See applications information.

*Specifications same as SP 674AJ. **Specifications same as SP 674AS.

PACKAGE OUTLINE



NOTE: See ordering information for Leadless Chip Carrier & CERDIP package outline. Sipex reserves the right to ship CERDIP in lieu of ceramic package.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	V_{LOGIC}	28	STS
2	12/8	27	DB_{11} (MSB)
3	CS	26	DB_{10}
4	A_0	25	DB_9
5	R/C	24	DB_8
6	CE	23	DB_7
7	V_{CC}	22	DB_6
8	REF OUT	21	DB_5
9	ANA GND(AC)	20	DB_4
10	REF IN	19	DB_3
11	N/C*	18	DB_2
12	BIP OFF	17	DB_1
13	$10V_{IN}$	16	DB_0 (LSB)
14	$20V_{IN}$	15	DIGITAL GND

*This pin is not connected to the device; V_{EE} is generated internally.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common . . . . . 0 to + 16.5V
V_{LOGIC} to Digital Common . . . . . 0 to + 7V
Analog Common to Digital Common . . . . . − 0.5 to + 1V
Control Inputs (CE, CS, A_0, 12/8, R/C) to Digital Common . . . . . − 0.5V to V_{LOGIC} + 0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common . . . . . ± 16.5V
$20V_{IN}$ to Analog Common . . . . . ± 24V
REF OUT . . . . . Indefinite short to common
Momentary short to V_{CC}
Power Dissipation 1000mW
Lead Temperature, Soldering . . . . . 300°C, 10Sec

CONVERT MODE TIMING CHARACTERISTICS

Typical @25°C, V_{CC} = + 15V or + 10V, V_{LOGIC} = + 5V, V_{EE} = 0V, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS[1]	MIN	MAX	UNITS
t_{DSC} STS Delay from CE			200	ns
t_{HEC} CE Pulse Width		50		ns
t_{SSC} CS to CE Setup		50		ns
t_{HSC} CS Low during CE High		50		ns
t_{SRC} R/C to CE Setup		50		ns
t_{HRC} R/C Low during CE High		50		ns
t_{SAC} A_0 to CE Setup		0		ns
t_{HAC} A_0 Valid during CE High		50		ns
t_C Conversion Time				
12-Bit Cycle	T_{min} to T_{max}	9	15	µs
8-Bit Cycle	T_{min} to T_{max}	6	10	µs

NOTE: 1. Time is measured from 50% level of digital transitions. Tested with a 100pF and 3k Ω load for high impedance to drive and tested with 10pF and 3KΩ load for drive to high impedance.

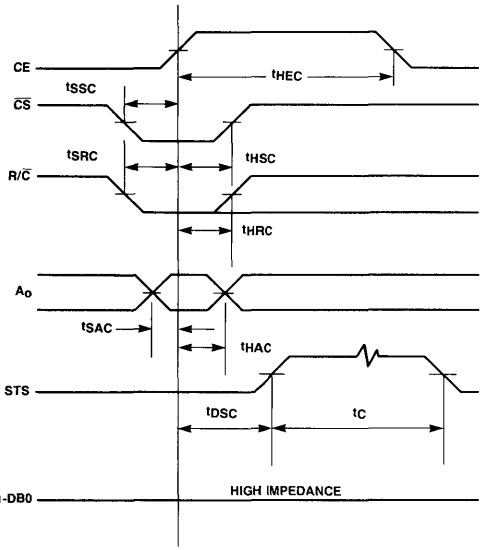


Figure 1. Convert Mode Timing Diagram

READ MODE TIMING CHARACTERISTICS

Typical @25°C, V_{CC} = + 15V or + 12V, V_{LOGIC} = + 5V, V_{EE} = 0V, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS
t_{DD} Access Time from CE			150	ns
t_{HD} Data Valid After CE Low	25			ns
t_{HL} Output Float Delay			150	ns
t_{SSR} CS to CE Setup	50	0		ns
t_{SRR} R/C to CE Setup	0	0		ns
t_{SAR} A_0 to CE Setup	50			ns
t_{HRS} CS Valid After CE Low	0	0		ns
t_{HRR} R/C High After CE Low	0	0		ns
t_{HAR} A_0 Valid After CE Low	50			ns
t_{HS} STS Delay After Data Valid	100		600	ns

9

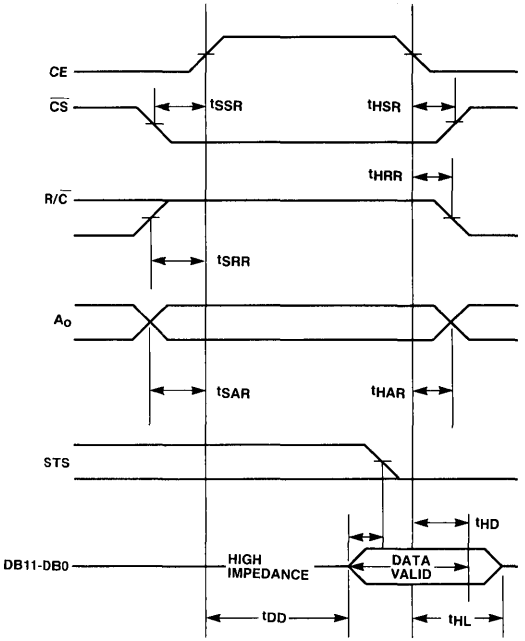


Figure 2. Read Mode Timing Diagram

STAND-ALONE MODE TIMING CHARACTERISTICS

Typical @25°C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = 0V, unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL} Low R/C Pulse Width	50			ns
t_{DS} STS Delay from R/C			200	ns
t_{HDR} Data Valid After R/C Low	25			ns
t_{HS} STS Delay After Data Valid	100		600	ns
t_{HRH} High R/C Pulse Width	150			ns
t_{DDR} Data Access Time			150	ns

SAMPLE AND HOLD

Acquisition Time[1]	1.0	1.4	1.8	μs
Aperture Uncertainty Time[1]		20		ns

NOTE: 1. Parameter is guaranteed by design and sampled characterization data.

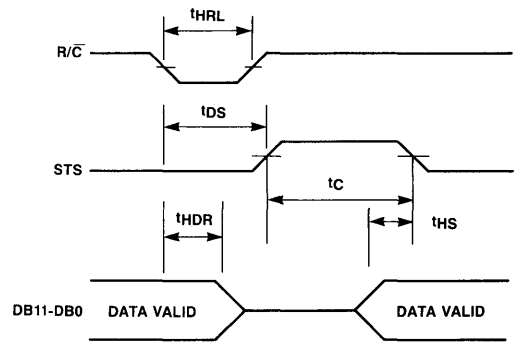


Figure 3. Low Pulse For R/C — Outputs Enabled After Conversion

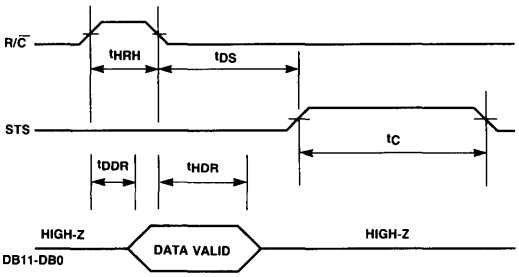


Figure 4. High Pulse For R/C — Outputs Enabled While R/C is High, Otherwise High Impedance

CIRCUIT OPERATION

The SP 674A is a complete 12-bit analog-to-digital converter which consists of a single chip version of the industry standard 674. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive-approximation register (SAR), sample and hold, clock, output buffers and control circuitry to make it possible to use the SP 674A with few external components.

When the control section of the SP 674A initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re-started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal SP 674A 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to be greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ± ½ LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ± 1% and can supply up to 2mA to an external load in addition to that required to drive the reference input resistor (1mA) and offset resistor (1mA) when operating with ± 15V supplies. If the SP 674A is used with ± 12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the SP 674A reference must remain constant during conversion.

The sample and hold is a default function by virtue of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although there is no sample and hold circuit in the classical sense, the sampling nature of the capacitive DAC makes the SP 674A appear to have a built in sample and hold. This sample and hold action substantially increases the signal bandwidth of the SP 674A over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the SP 674A is disconnected from the user's sample and hold. This prevents transients occuring during conversion from being inflicted upon the attached sample and hold buffer. All other 674 circuits will cause a transient load current on the sample and hold which will upset the buffer output and may add error to the conversion itself.

Furthermore, the isolation of the input after the acquisition time in the SP 674A allows the user an opportunity to release the hold on an external sample and hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the SP 674A acts as any other 674 device because the internal S/H is transparent. The sample/hold function in the SP 674A is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

The operation of the S/H function is internal to the SP 674A and is controlled through the normal R/C control line (refer to Figure 5.) When the R/C line makes a negative transition, the SP 674A starts the timing of the sampling and conversion. The first 2 clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as t_{ACQ}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

During t_{ACQ}, the equivalent circuit of the SP 674A input is as shown in Figure 6 (the time constant of the input is independent of which input level is used). This CDAC capacitance must be charged up to the input voltage during t_{ACQ}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12 bits of accuracy during t_{ACQ}. The excess time left during t_{ACQ} allows the user's buffer amp to settle after being switched to the CDAC load.

Note that because the sample is taken relative to the R/C transition, t_{ACQ} is also the traditional "aperture delay" of this internal sample and hold.

Since t_{ACQ} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in t_{ACQ} = 1.4 μsecs $\pm$0.4 μsecs between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the SP 674A.

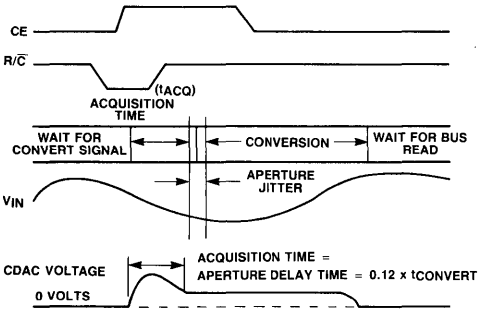


Figure 5. Sample and Hold Function

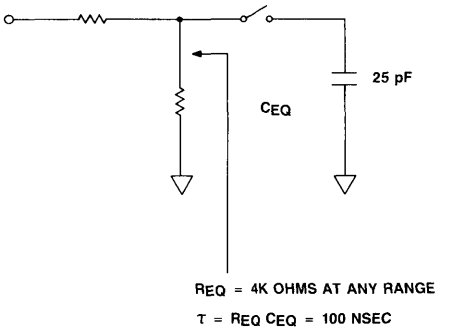


Figure 6. Equivalent SP 674A Input Circuit

APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample and hold is the uncertainty in the time the actual sample is taken — i.e. the "aperture jitter" or t_{AJ}. The SP 674A has a nominal aperture jitter of 20 nsecs between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point (See Figure 7). The magnitude of this change for a sine wave can be calculated:

Assume a sinusoidal signal, maximum slew rate, $S_R = 2\pi f V_P$ (V_P = peak voltage, f = frequency of sine wave). For an N-bit converter to maintain $\pm$ ½ LSB accuracy:

$V_{ERR} \leq V_{FS}/2^{N+1}$ (where V_{ERR} is the allowable error voltage and V_{FS} is the full scale voltage).

From Figure 7:

$S_R = \Delta V/\Delta T = 2\pi f V_P$

Let $\Delta V = V_{ERR}$, $V_P = V_{IN}/2$ and $\Delta T = t_{AJ}$ (the time during which unwanted voltage change occurs)

The above conditions then yield:

$V_{FS}/2^{N+1} \leq \pi f V_{IN} t_{AJ}$ or $f_{MAX} \leq V_{FS}/(\pi V_{IN} t_{AJ})2^{N+1}$

For the SP 674A, t_{AJ} = 20 nsec; therefore,

$f_{MAX} \leq 2$kHz

For higher frequency signal inputs, an external sample and hold is recommended.

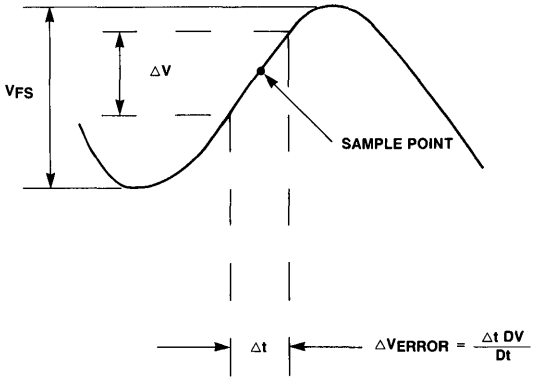


Figure 7. Aperture Uncertainty

TYPICAL INTERFACE CIRCUIT

The SP 674A is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in Figures 8 and 9. The two typical interface circuits are for operating the SP 674A in either a unipolar or bipolar input mode. Further information is given in the following sections on these connections, but first a few considerations concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead. If this is not possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the SP 674A must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to its respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 μF tantalum and a 0.1 μF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the SP 674A is being used to upgrade an already existing design.

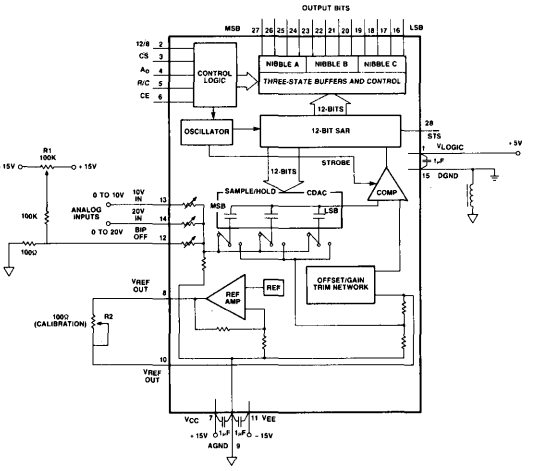


Figure 8. Unipolar Input Connections

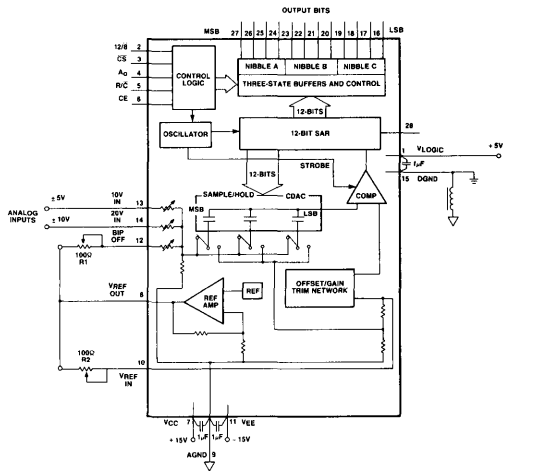


Figure 9. Bipolar Input Connections

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accomodate the ground currents present with this device.

The analog ground current is approximately 6mADC while the digital ground is 3mADC. The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The SP 674A may be operated by a μP or in the stand-alone mode. The part has four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to Figure 8, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +½ LSB or +1.22mV for the 10V range and +2.44mV for the 20V range should be applied to the SP 674A. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1½ LSB below the nominal full scale which is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R1 with a 50Ω, 1% metal film resister and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0V to 10V range or to pin 14 for the 0V to 20V range.

BIPOLAR

The gain and offset errors listed in the specifications may be adjusted to zero using the potentiometers R1 and R2 (See Figure 9). If adjustment is not needed, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5V range or to pin 14 for a ±10V range. First apply a DC input voltage ½ LSB above negative full scale which is −4.9988V for the ±5V range or −9.9976V for the ±10V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1½ LSB below positive full scale which is +4.9963V for the ±5V range or +9.9927V for the ±10V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

The 100Ω potentiometer R2 provides gain adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (for and LSB of 2.5mV) or 20.48 (for an LSB of 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then to provide gain adjust for the 10.24 range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 1000 potentiometer in series with pin 14.

CONTROLLING THE SP 674A

The SP 674A can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/C input pin. Full μP control consists of selecting an 8- or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 followed by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/8, CS, A_0, R/C and CE. The use of these inputs in controlling the converter's operations is shown in Table 1, and the internal control logic is shown in a simplified schematic in Figure 10.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/C. The other controls must be tied to known states as follows: CE and 12/8 are wired high, A_0 and CS are wired low. The output data arrives in words of 12-bits each. The limits on R/C duty cycle are shown in Figures 3 and 4. It may have duty cycle within and including the extremes shown in the specifications on the pages. In general, data may be read when R/C is high unless STS is also high, indicating a conversion is in progress.

CONVERSION LENGTH

A conversion start transition latches the state of A_0 as shown in Figure 10 and Table 1. The latched state determines if the conversion stops with 8-bits (A_0 high) or continues for 12-bits (A_0 low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic "1". A_0 is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

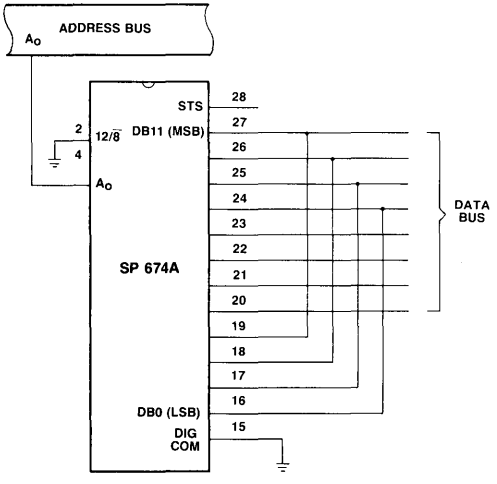


Figure 10. Interfacing the SP 674A to an 8-Bit Data Bus

CONVERSION START

A conversion may be initated by a logic transition on any of the three inputs: CE, CS, R/C, as shown in Table 1. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if A_0 changes state after a conversion begins, an additional Start Convert command will latch the new state of A_0 and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

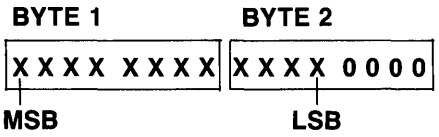
READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/C is high, STS is low, CE is high and CS is low. The data lines become active in response to the four conditions and output data according to the conditions of 12/8 and A_0. The timing diagram for this process is shown in Figure 2. When 12/8 is high, all 12 data outputs become active simultaneously and the A_0 input is ignored. This is for easy interface to a 12 or 16 bit data bus. The 12/8 input is usually tied high or low, although it is TTL/CMOS compatible.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 Bit Conversion
↑	0	0	X	1	Initiate 8 Bit Conversion
1	↓	0	X	0	Initiate 12 Bit Conversion
1	↓	0	X	1	Initiate 8 Bit Conversion
1	0	↓	X	0	Initiate 12 Bit Conversion
1	0	↓	X	1	Initiate 8 Bit Conversion
1	0	1	1	X	Enable 12 Bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Table 1. Truth Table for the SP 674A Control Inputs

When 12/8 is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in Figure 10. The A_0 control can be connected to the least significant bit of the data bus in order to store the output data into two consecutive memory locations. Whn A_0 is pulled low, the 8 MSB's are enabled only. When A_0 is high, the 4 MSB's are disabled, bits 4 through 7 are forced to a zero and the four LSB's are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

A_0 may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in Figure 10 will never be enabled at the same time.

In Figure 2, it can be seen that a read operation usually begins after the conversion is complete and STS is low. If earlier access is needed, the read can begin no later than the addition of times t_{DD} and t_{HS} before STS goes low.

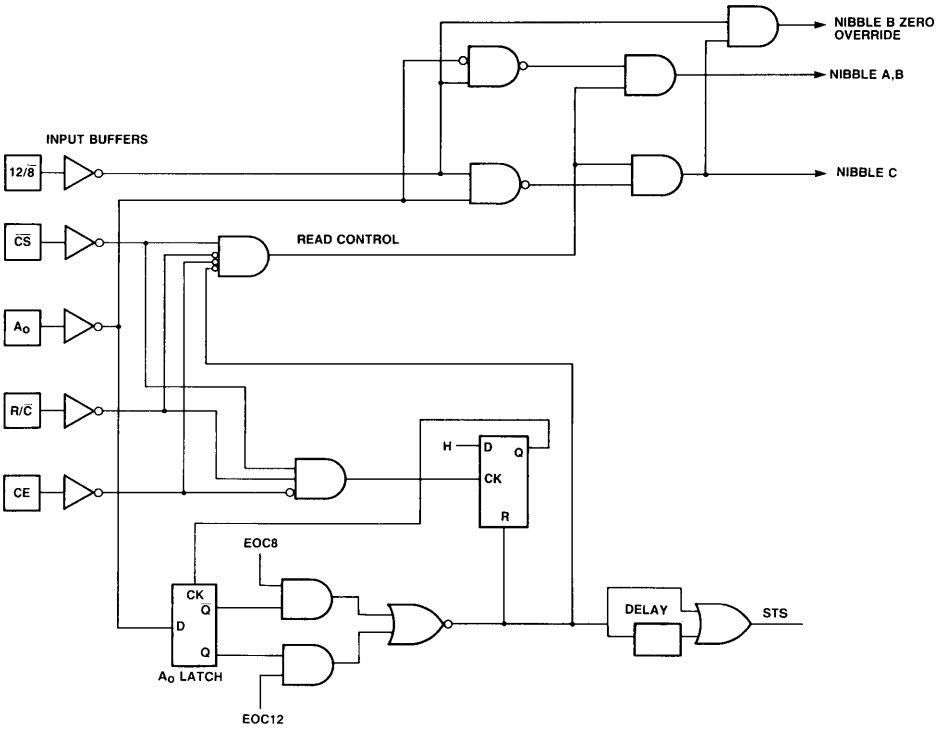


Figure 11. SP 674A Control Logic

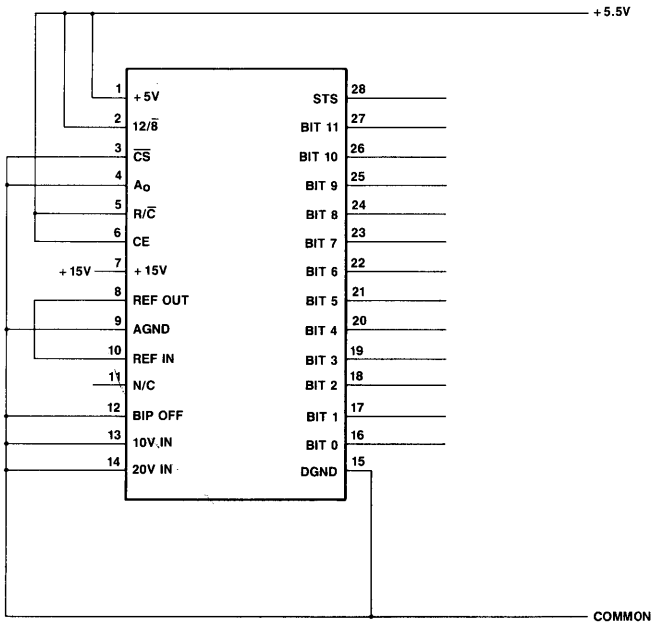


Figure 12. Burn-In Schematic

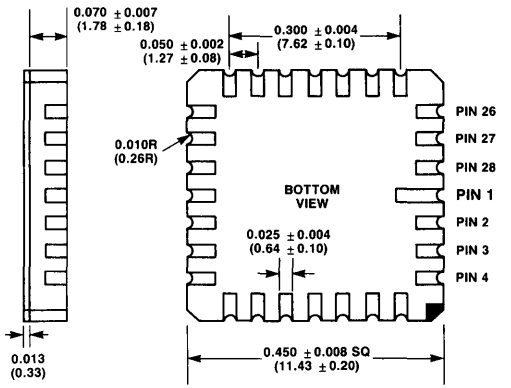
ORDERING INFORMATION

MODEL NUMBER	RESOLUTION NO MISSING CODES (T_{min} to T_{max})	LINEARITY ERROR	MAX FULL SCALE T.C. (ppm/°C)	TEMP. RANGE	MIL SCREENING
SP 674AJ	11 Bits	±1 LSB	50.0	0°C to +70°C	—
SP 674AK	12 Bits	±½ LSB	27.0	0°C to +70°C	—
SP 674AL	12 Bits	±½ LSB	10.0	0°C to +70°C	—
SP 674AA[1]	11 Bits	±1 LSB	50.0	−40°C to +85°C	—
SP 674AB[1]	12 Bits	±½ LSB	27.0	−40°C to +85°C	—
SP 674AC[1]	12 Bits	±½ LSB	10.0	−40°C to +85°C	—
SP 674AS	11 Bits	±1 LSB	50.0	−55°C to +125°C	—
SP 674AT	12 Bits	±½ LSB	25.0	−55°C to +125°C	—
SP 674AU	12 Bits	±½ LSB	12.5	−55°C to +125°C	—
SP 674AS/B	11 Bits	±1 LSB	50.0	−55°C to +125°C	MIL-STD-883C
SP 674AT/B	12 Bits	±½ LSB	25.0	−55°C to +125°C	MIL-STD-883C
SP 674AU/B	12 Bits	±½ LSB	12.5	−55°C to +125°C	MIL-STD-883C

NOTE: 1.Electrical specifications for AA, AB, and AC grades are the same as AJ, AK, and AL models, respectively with the exception of extended operating temperature range performance from −40°C to +85°C.

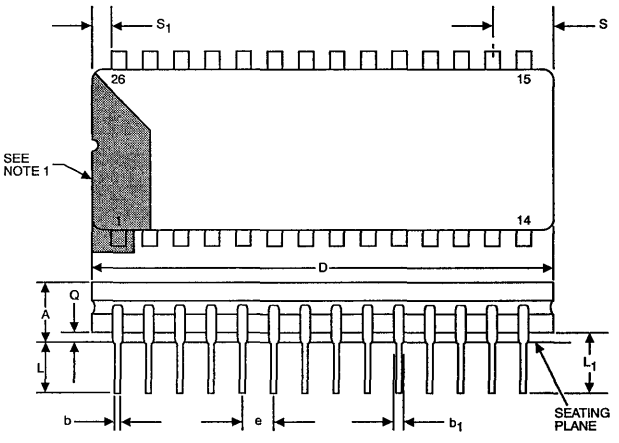
PACKAGE OUTLINE

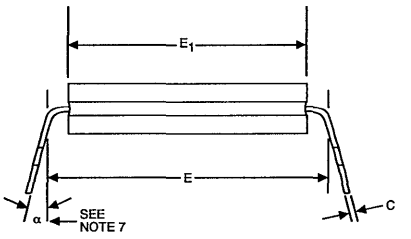
28 Pin Leadless Chip Carrier



NOTE: To order Leadless Chip Carrier version add /LCC suffix to model number.

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A		0.225		5.72	
b	0.014	0.026	0.36	0.66	7
b_1	0.030	0.070	0.76	1.78	2, 7
c	0.008	0.018	0.20	0.46	7
D		1.490		37.85	4
E	0.500	0.610	12.70	15.49	4
E_1	0.590	0.620	14.99	15.75	6
e	0.090	0.110	2.29	2.79	8
L	0.125	0.200	3.18	5.08	
L_1	0.150		3.81		
Q	0.015		0.38		3
S		0.100		2.54	5
S_1	0.005		0.13		5
α	0°	15°	0°	15°	



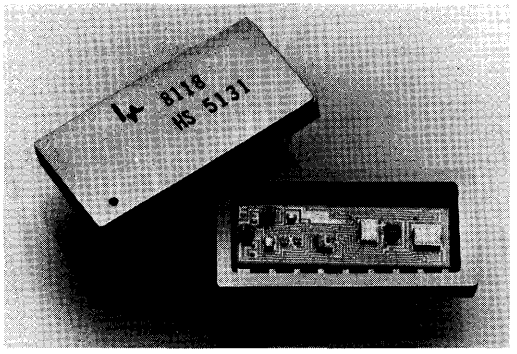


Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS 5131
8-Bit, 2.5μS ADC

FEATURES

- **2.5μS Conversion Time**
- **Low Power . . . 680mW Typical**
- **Small 18-Pin DIP**
- **Replacement for MN5131**
- **Adjustment Free**
- **±½LSB Linearity**
- **Guaranteed Monotonic**



DESCRIPTION

The HS 5131 is a fast, low-power 8-Bit successive approximation A/D converter with both parallel and serial output capability. It is designed as a replacement unit for the MN5131 and maintains ±2 LSB accuracy over the full temperature range. Conversion speed is 2.5 μ s, maximum.

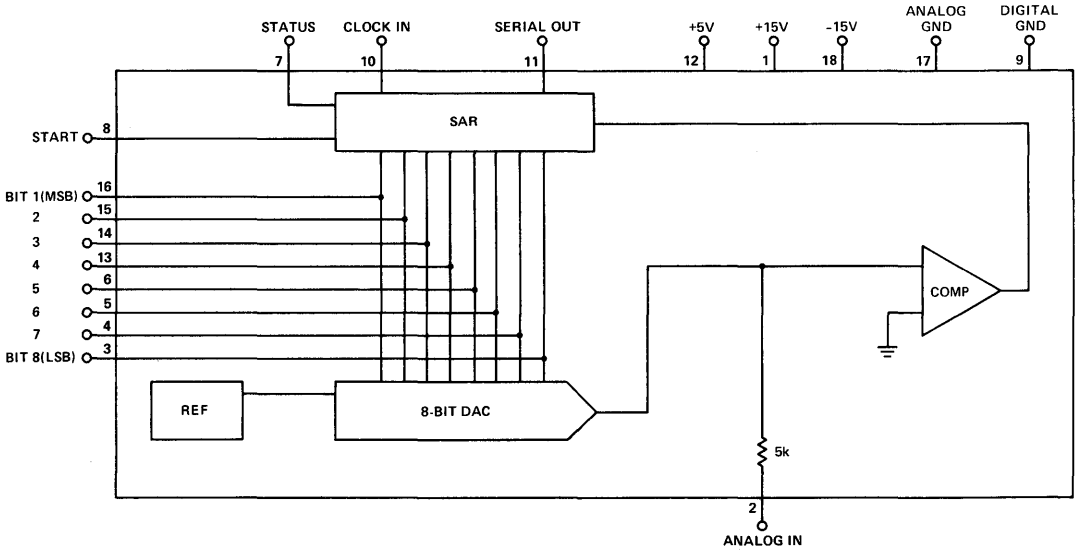
Analog input range of the HS 5131 is ±5V and input circuits are DTL/TTL compatible.

The HS 5131 is housed in a hermetically-sealed 18-pin side brazed ceramic package and incorporates precision, laser-trimmed resistors for excellent long-term stability.

Monotonicity of the HS 5131 is guaranteed over the specified temperature range.

All "B" versions of the HS 5131 are fully screened and tested to MIL-STD-883 Rev. C, Level B requirements to assure highest reliability in severe environments.

FUNCTIONAL DIAGRAM



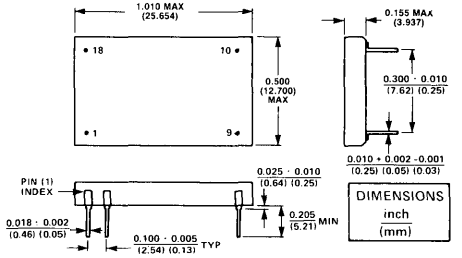
9

SPECIFICATIONS

(Typical @ +25° C and nominal power supplies unless otherwise noted)

MODEL	**HS 5131**
TYPE	Successive Approximation
RESOLUTION	8 Bits
ANALOG INPUT	
Range	-5V to +5V
Impedance	5kΩ
DIGITAL INPUT	
Logic 1	+2.0V min
Logic 0	+0.4V max
Clock	1 TTL Load max
Pulse Width, High	25nS min
Pulse Width, Low	50nS min
Frequency	3.2 MHz max
Start, High	2 TLL Loads max
Start, Low	1 TTL Load max
DIGITAL OUTPUTS	
Logic 1	2.4V min
Logic 0	0.4V max
Fan-out High	11 TTL Loads min
Fan-out Low	5 TTL Loads min
Coding	Offset Binary
Serial Output	NRZ
ACCURACY	
Linearity[1]	±1/2 LSB max
Absolute Accuracy[2]	±1 LSB max
Absolute Accuracy[1]	±2 LSB max
Bipolar Offset	1 LSB max
Bipolar Offset[1]	2 LSB max
Conversion Time	2.5μS max
POWER SUPPLY	
Requirements	
+15V (nominal) ±3%	@ 21mA max
-15V (nominal) ±3%	@ -10mA max
+5V (nominal) ±5%	4.75 to 5.25V @ 100mA max
Rejection Ratios	
+15V Supply	±0.05%/% max
-15V Supply	±0.01%/% max
Total Power Consumption	965mW max
TEMPERATURE RANGE	
Operating[1]	
C Versions	0°C to 70°C
B Versions	-55°C to +125°C
Storage	-65°C to +150°C
MECHANICAL	
Case Style	18 Pin DIP, ceramic

Case Dimensions



Pin Designations

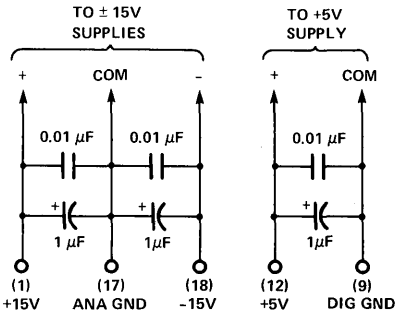
PIN	FUNCTION	PIN	FUNCTION
1	+15V	18	-15V
2	Analog In	17	Analog Gnd
3	Bit 8	16	Bit 1
4	Bit 7	15	Bit 2
5	Bit 6	14	Bit 3
6	Bit 5	13	Bit 4
7	Status	12	+5V
8	Start	11	Serial Out
9	Digital Gnd	10	Clock In

NOTES

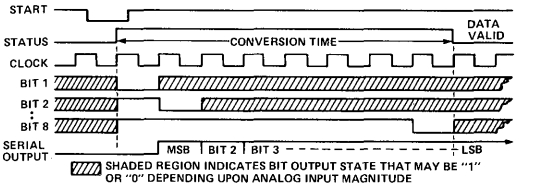
1. Specification applies for operation over the temperature range.
2. Absolute accuracy includes all errors due to gain, offset and non-linearity.

APPLICATIONS INFORMATION

RECOMMENDED POWER SUPPLY BYPASS CIRCUIT



TIMING DIAGRAM



NOTES:

1. For continuous operation connect start (Pin 8) to status (Pin 7).
2. Reset the converter by holding the start 'low' during a low to high transition of the clock. The start must be low for a minimum of 20nS prior to the clock transition. After the start is again set high the conversion will begin on the next low to high transition of the clock. The start may be set low at any time during a conversion to reset and begin again.
3. At the end of conversion the status will remain low until the converter is reset. The parallel data is valid for the entire time the status is low.
4. The serial output is non-return to zero.
5. For the user's design flexibility, digital and analog grounds are brought out separately and must be externally connected. For optimum results, this external connection should be made as close to the converter as is possible.

TRANSFER CHARACTERISTICS

ANALOG INPUT	DIGITAL OUTPUT MSB							LSB
-4.961	0	0	0	0	0	0	0	0
-0.039	0	1	1	1	1	1	1	0
0.000	0	0	0	0	0	0	0	0
4.922	1	1	1	1	1	1	0	0
4.961	1	1	1	1	1	1	1	0

*The voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting the output bits indicated as 0 will change from "1" to "0" or from "0" to "1" as the input voltage passes through the level indicated.

ORDERING INFORMATION

MODEL NUMBER	DESCRIPTION
HS5131C	8-Bit ADC, Commercial
HS 5131B	8-Bit ADC, MIL

Specifications subject to change without notice.

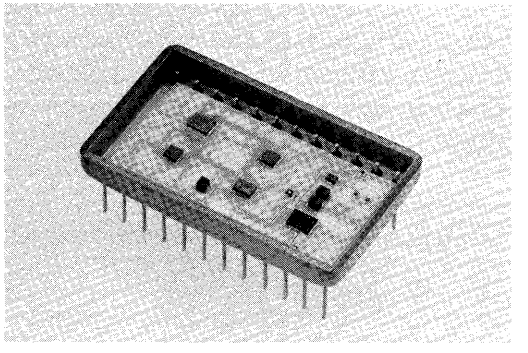
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS 5150

High Speed 8-Bit ADC with μP Interface

FEATURES

- **2.5μsec Conversion Time**
- **Three State Outputs**
- **Full MIL Operation**
  −55°C to +125°C
- **7 User-Selectable Input Ranges**
- **Adjustment Free −**
  No Gain or Offset Adjustments Necessary

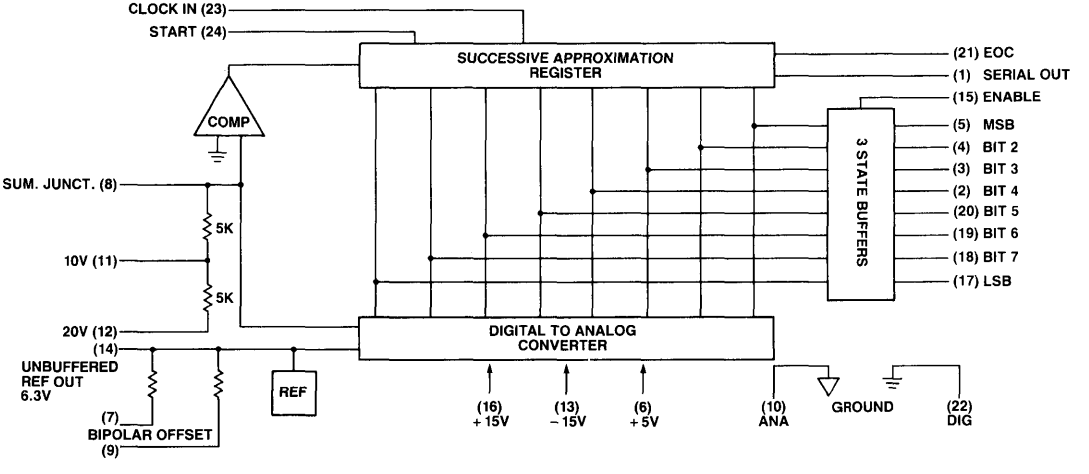


DESCRIPTION

The HS 5150 is a complete, 8-bit, successive approximation analog to digital converter with three-state output buffers for direct interface to microprocessor buses. The ADC converts in 2.5 μ sec (max), and features ± ½ LSB linearity with no missing codes guaranteed over an operating temperature of −55°C to +125°C. The HS 5150 incorporates highly stable thin-film resistor networks enabling adjustment free operation. No external gain or offset adjusting potentiometers are required for ±1 LSB absolute accuracy. The inputs can be pin programmed for 0 to +5V, 0 to +10V, ±2.5V, ±5V, ±10V, 0 to −5V, and 0 to −10V.

Three state output buffers enable interface to a variety of 8-bit microprocessors. In memory mapped applications, the ADC resembles a RAM location with 2.5 μ sec access time. The HS 5150 is available with MIL-STD-883 Rev. C, Levels B or S screening for military/aerospace applications.

FUNCTIONAL DIAGRAM



9

SPECIFICATIONS

(Typical @ +25°C with ±15V and +5V, unless otherwise specified)

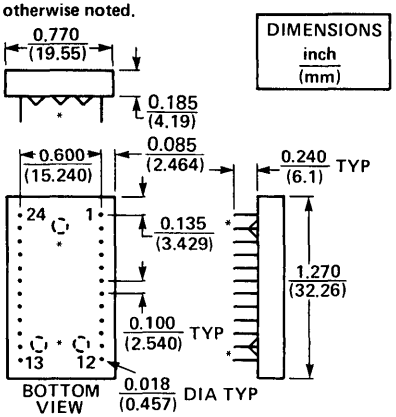
SERIES	HS 5150
TYPE	Successive Approximation
RESOLUTION	8-Bits
ANALOG INPUTS	
Input Voltage Range	7 Input Ranges
Input Impedance	2.5/5/10 KΩ
DIGITAL INPUTS	
Logic "0" (Except Enable)	0.8V max
Logic "1" (Except Enable)	2.0V min
Loading (Note 1)	1 TTL Load
Logic "0" Enable (Outputs "ON")	1.5V max
Logic "1" Enable (Outputs "OFF")	3.5V min
Loading	0.1 μA max
Clock Pulse Width	46 nsec min
Start Pulse Width	50 nsec min
DIGITAL OUTPUTS	
Parallel Outputs	
Output Current "0" and "1"	1.6 mA min
Logic "1"	2.4V min
Logic "0"	0.4V max
Serial and EOC Output Fanout[1]	5 TTL Loads
Delay from Enable Pulse to Data Valid	85 nsec typ
	120 nsec max
REFERENCE, INTERNAL	
Voltage	6.3V ±5%
Drift	25 ppm/°C
Output Current	200 μA max
CONVERSION TIME[2]	2.5 μ sec max
ACCURACY	
Absolute Accuracy[3]	±1/2 LSB typ ±1 LSB max
Absolute Accuracy (−55°C to +125°C)	±2 LSB max
Zero Error	±1/4 LSB typ ±1/2 LSB max
−55°C to +125°C	±1/2 LSB typ ±1 LSB max
Linearity (−55°C to +125°C)	±1/4 LSB typ ±1/2 LSB max
No Missing Codes (−55°C to +125°C)	Guaranteed
POWER SUPPLY	
Requirements	
+15	+14.5V to +15.5V @ 20 mA max
−15	−14.5V to +15.5V @ −13 mA max
+5	+4.75V to +5.25V @ 101 mA max
Rejection Ratio	
+15	±0.03% FSR/% Supply
−15	±0.01% FSR/% Supply
Power Consumption	680 mW typ
	1000 mW max
TEMPERATURE	
Operating	
C- Model	0°C to 70°C
B- Model	−55°C to +125°C
Storage	−65°C to +150°C

NOTES:

1. A TTL Load is defined as 40 μA at Logic "1" and 1.6 mA at Logic "0".
2. Conversion time of 2.5 μ sec corresponds to an external clock frequency of 3.6 MHz.
3. Absolute Accuracy includes all errors gain, zero and linearity.

PACKAGE OUTLINE

Case Dimensions max unless otherwise noted.



*0.030 (0.76) ±0.010 (0.25) STANDOFFS, SUPPLIED AT MANUFACTURERS OPTION.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	SERIAL OUT	13	−15V
2	BIT 4	14	V_{REF} OUT (6.3V)
3	BIT 3	15	DATA ENABLE
4	BIT 2	16	+15V
5	BIT 1 (MSB)	17	BIT 8 (LSB)
6	+5V	18	BIT 7
7	BIPOLAR OFFSET	19	BIT 6
8	SUMMING JUNCTION	20	BIT 5
9	BIPOLAR OFFSET	21	EOC
10	ANALOG GND	22	DIGITAL GND
11	10V INPUT	23	CLOCK
12	20V INPUT	24	START

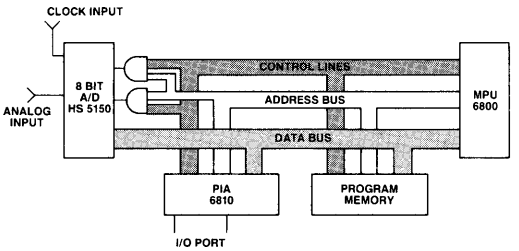
ABSOLUTE MAXIMUM RATINGS

+15V Suppy . . . . . −0.5V to +18V
−15V Supply . . . . . +0.5V to −18V
5V Supply . . . . . −0.5V to +7V
Analog Input . . . . . ±20V
Digital Inputs . . . . . −0.5V to +5.5V

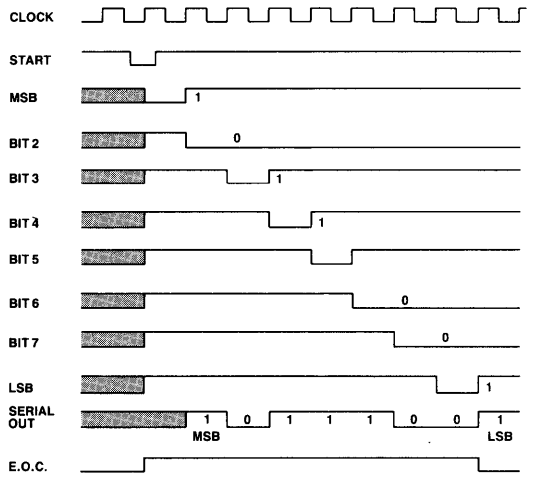
APPLICATIONS INFORMATION

The three state outputs of the HS 5150 make interfacing to data busses of minicomputers very easy. A typical application would consist of using the HS 5150 in the basic 6800 microprocessor system as shown in the block diagram below.

In this application, the HS 5150 is treated as a memory location and is addressed by using the extended addressing mode. Just two instructions are needed to acquire the desired information. First, the HS 5150 receives a start command by the use of a STORE instruction, and then a LOAD or arithmetic instruction is used to obtain the digital information by addressing the HS 5150 as a memory location. Since the HS 5150 converts in 2.5 μ sec, there is no delay waiting for the information to be valid. Several HS 5150s may be incorporated in one system by changing the address of the enable signal. The HS 5150 may be used in a similar manner with other microprocessors.



TIMING DIAGRAM



NOTES:

1. Shaded area represents indeterminate logic level.
2. Code shown represents an analog input of +7.226 volts for the 0 to +10 volts range.
3. The converter will reset on the first rising edge of the clock after the start command has gone low. Conversion will begin on the first rising edge of the clock after the start has returned high.
4. The start has to be low for a minimum of 50 nSec prior to the edge of the clock.
5. The EOC will go low approximately 45 nSec prior to Bit 8 (LSB) being valid.
6. For continuous conversion connect the EOC to the start command.

TRANSFER CHARACTERISTICS

DIGITAL OUTPUT		ANALOG INPUT RANGE						
MSB	LSB	0 to +5	0 to +10	±2.5	±5	±10	0 to −5	0 to −10
0000	0000	0	0	−2.500	−5.000	−10.000	−4.981	−9.961
0000	0001	+0.019	+0.039	−2.481	−4.961	−9.922	−4.961	−9.922
0111	1111	+2.481	+4.961	−0.019	−0.039	−0.078	−2.500	−5.000
1000	0000	+2.500	+5.000	0	0	0	−2.481	−4.961
1111	1110	+4.961	+9.922	+2.461	−4.922	−9.844	−0.019	−0.039
1111	1111	+4.981	+9.961	+2.481	+4.961	+9.922	0	0
Input Impedance		2.5K	5K	2.5K	5K	10K	2.5K	5K
Connect Input to Pin		11	11	11	11	12	11	11
Connect Pin 8 to Pin		12	Open	12 & 9	9	9	12,7 & 9	9,7
Connect Pin 10 to Pin		7 & 9	7 & 9	7	7	7	NC	NC

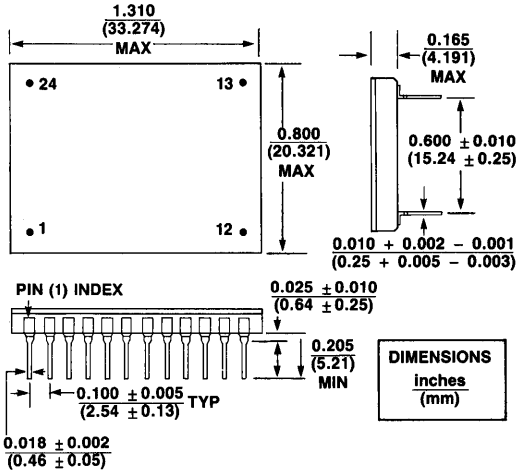
*Voltages given are theoretical values for the transitions indicated. Ideally, the digital output will change as the input voltage passes through the voltage level indicated.

APPLICATIONS INFORMATION (continued)

OPERATION

Data Enable — The data enable line controls the state of the parallel outputs. For a high impedance output (outputs in the off state) the Data Enable line must be at a logic "1" level. For the data to be available on the outputs, the Data Enable line must be at a logic "0" level. Data will be available 120 nsec (max) after the Data Enable goes low.

Grounds — To obtain optimum performance analog and digital grounds are not connected internally and must be tied together as close to the unit as possible. If these grounds must run separately, a non-polarized 0.01 μF capacitor should be connected between Pins 10 and 22. The power supplies should be decoupled with a tantalum or electrolytic type capacitor located as close to the HS 5150 as possible. For optimum performance, a 1 μF paralleled by a 0.01 μF ceramic capacitor should be connected between analog ground and the ±15 volt supplies and between digital ground and the +5 volt supply.



Analog Input — Since the HS 5150 is a high speed converter, the signal source must have a low output impedance at high frequencies to allow for fast changes in the current sinking and sourcing to the analog input. A suitable amplifier would be the Harris HA2525 operational amplifier or a high speed sample and hold amplifier such as Hybrid Systems' HS 346.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 5150C	COMM., 8-BIT, ADC
HS 5150B	MIL., 8-BIT, ADC

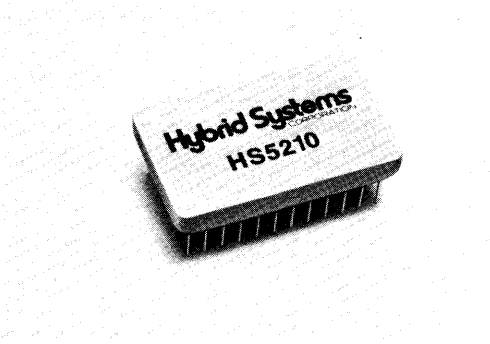
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS5210 SERIES

12-BIT ADJUSTMENT FREE ADCs

FEATURES

- 12-bit conversion in 10μS typ; 13μS max
- Adjustment-free, ±0.0125% linearity
- Low power: 670 mW typ
- Wide operating temperature range: −55°C to +125°C
- Small size: 24-pin, metal-to-metal, hermetic package
- Full MIL-STD-883 Rev. C, Levels B or S, or commercial processing



DESCRIPTION

HS5210 Series are extremely fast 12-bit succesive approximation A/D converters providing both parallel and serial output. All models have a maximum conversion time of 13μS which allows full accuracy with a 1 MHz clock.

HS5210 Series hybrid microcircuit converters are housed in hermetically-sealed 24-pin dual-in-line packages. Miniature size, low power consumption and adjustment free operation are product features. The HS5210 Series provides the user with the best possible performance in systems requiring maximum reliability in the smallest space. All converters are completely laser-trimmed, adjustment free, and incorporate highly stable thin-film resistor networks which provide long-term maintenance free operation.

HS5210 Series ADCs are available in four input voltage ranges: 0 to −10 volts (HS5210/13), ±5 volts (HS5211/14), ±10 volts (HS5212/15), and 0 to +10 volts (HS5216). For each of these input ranges, the user has the option of specifying a model complete with an internal reference or for improved absolute accuracy, models which require an external reference.

In all cases ±½ LSB linearity is guaranteed over the entire operating temperature range.

All models of the HS5210 Series may be procured for operation over the −55°C to +125°C military temperature range ("B" models) with the same operating characteristics as the commercial 0°C to +70°C range. In addition, full military temperature range models are available processed to MIL-STD-883 Rev. C, Levels B or S.

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HS 5210 SERIES SUCCESSIVE APPROXIMATION 12-BIT A/D Converters

ABSOLUTE MAXIMUM RATINGS:

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Positive Supply	+18 Volts
Negative Supply	-18 Volts
Logic Supply	+7 Volts
Analog Input	±25 Volts
Digital Outputs	0 to Logic Supply
Digital Inputs	-0.5 to +5.5 Volts
Reference Supply (Models HS5213, 14, 15)	-15 Volts

SPECIFICATIONS (T_A=25°C, Voltages ±15, +5 Unless otherwise stated)

PERFORMANCE (NOTE 1):

INPUT RANGE	INPUT IMPEDANCE	HIGH PERFORMANCE (Internal Reference)	HIGH ACCURACY (Ext. Ref.= -10.000V)	
0 to -10V	3.6k	HS5210	HS5213	
+5V to -5V	3.6k	HS5211	HS5214	
+10V to -10V	7.2k	HS5212	HS5215	
0 to +10V	3.3k	HS5216		
		MAX.	MAX.	UNITS
Resolution		12	12	Bits
Linearity (25°C)		±½	±½	LSB
Zero Error		1	1	LSB
t_{min} to t_{max}		±3/4	±3/4	LSB
Absolute Accuracy (25°C) (Note 2)		2	2	LSB
Absolute Accuracy (-55°C to +125°C) (Note 2)		±.4	±.1	%
Conversion Time		13	13	µSec
Power Supply Requirements				
Current Drain +15 Volt Supply		16	10	mA
Current Drain -15 Volt Supply		28	28	mA
Current Drain + 5 Volt Supply (Note 5)		50	50	mA
Current Drain @ Reference Input			2	mA
Power Supply Rejection				
±15 Volts (Note 3)		±0.002	±0.002	%F.S.R./%Supply
+ 5 Volts		±0.001	±0.001	%F.S.R./%Supply
Power Consumption		910	825	mW

LOGIC RATINGS

	MIN.	TYP.	MAX.	UNITS
Input Logic Commands				
Logic "0"			0.7	Volts
Logic "1"	2.0			Volts
Loading		0.5		TTL Load
Clock Input Pulse Width				
Logic "0"	180			nSec
Logic "1"	100			nSec
Output Logic				
Logic "0"		0.15	0.4	Volts
Logic "1"	2.4	3.6		Volts
Serial Output				NRZ
Parallel Output (See Timing Diagram)				
Fanout-High	8			TTL Load
Fanout-Low	2			TTL Load

LOGIC CODING

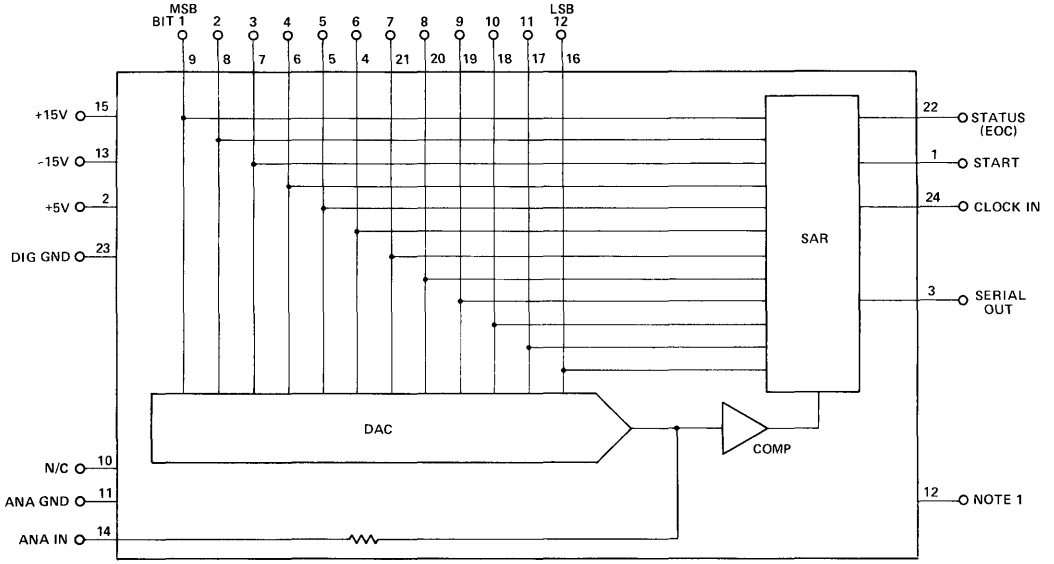
HS5210/5213	HS5211/5214	HS5212/5215	HS5216	MSB LSB
0.0000V	+5.0000V	+10.0000V	+10.0000V	0000 0000 0000
- 0.0024V	+4.9976V	+ 9.9951V	+ 9.9976V	0000 0000 000Ø*
- 4.9976V	+0.0024V	+ 0.0049V	+ 5.0024V	0111 1111 111Ø*
- 5.0000V	0.0000V	0.0000V	+ 5.0000V	ØØØØ ØØØØ ØØØØ*
- 5.0024V	-0.0024V	- 0.0049V	+ 4.9976V	1000 0000 000Ø*
- 9.9976V	-4.9976V	- 9.9951V	+ 0.0024V	1111 1111 111Ø*
-10.0000V	-5.0000V	-10.0000V	0.0000V	1111 1111 1111

The voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting the output bits indicated as Ø will change from "1" to "0" or from "0" to "1" as the input voltage passes through the level indicated

EXAMPLE:
With an HS 5210/13 (0 to - 10V range), the transition from an output 0000 0000 0000 to 0000 0000 0001 will ideally occur at an analog voltage of - 0.0024V and the transition from 1111 1111 1110 to 1111 1111 1111 will occur with an analog voltage of - 9.9976.

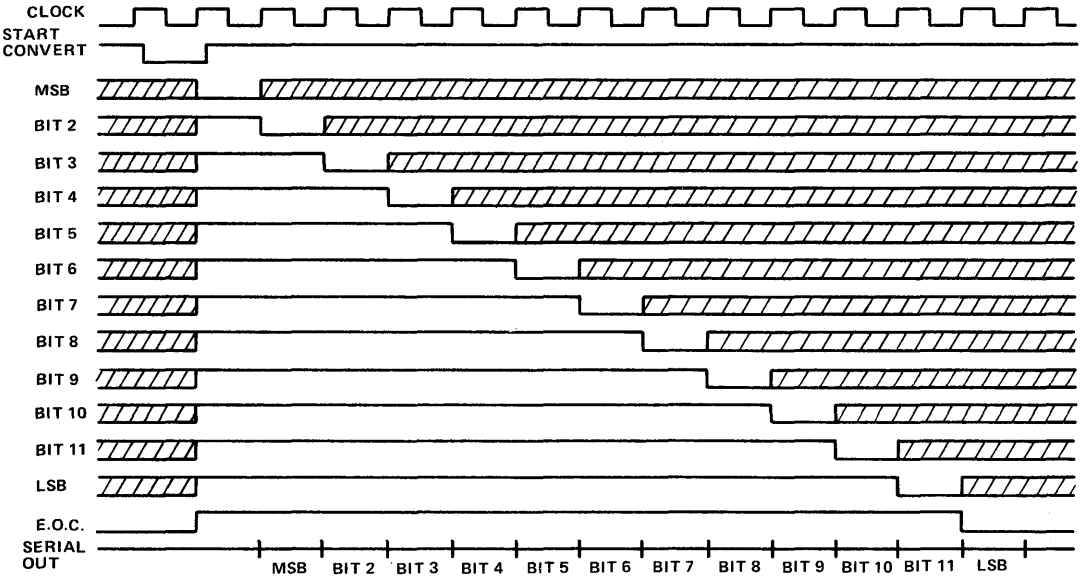
NOTE 1. Parts can be tested to meet MIL-38510/120. Consult factory.
NOTE 2. Absolute accuracy includes all errors, gain, zero, and linearity. No missing codes guaranteed over temperature.
NOTE 3. For proper operation ± 15V power supplies tolerance should not be greater than ± 5%.
NOTE 4. FSR is the abbreviation for "Full Scale Range" and is equal to the peak-to-peak output voltage, *i.e., 10V for ± 5V range.*
NOTE 5. Model HS 5216 + 5V current is 57 mA max.
NOTE 6. In case of discrepancy between package shown in photograph and package outline dimension, the mechanical outline is correct.

FUNCTIONAL DIAGRAM



NOTE 1. N/C for internal reference models. -10V ref input for external reference models.

TIMING DIAGRAM

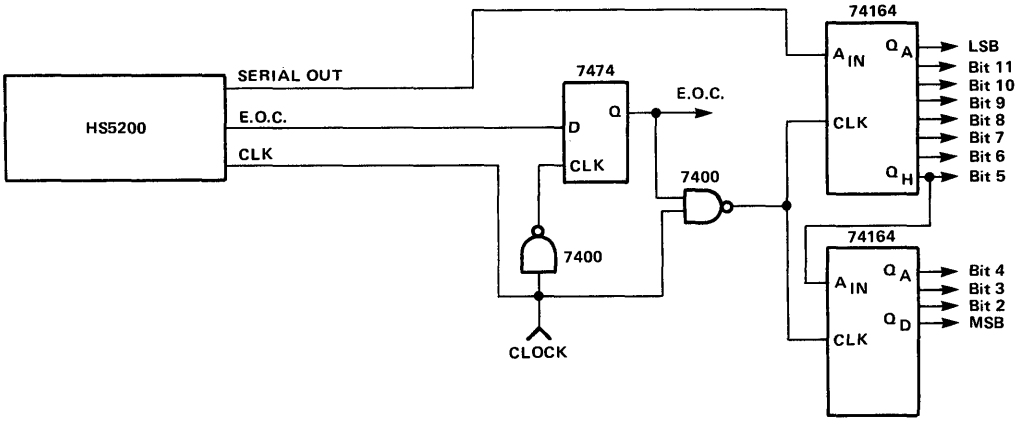


NOTES:

1. Shaded areas shown for parallel data outputs denote bit states determined by successive approximation of analog input.
2. For continuous operation connect start convert (Pin 1) to end of conversion (Pin 22).
3. Reset the converter by holding the start 'low' during a low to high transition of the clock. The start must be low for a minimum of 25 nSec prior to the clock transition. After the start is again set high the conversion will begin on the next low to high transition of the clock. The start may be set low at any time during a conversion to reset and begin again.
4. At the end of conversion the E.O.C. will remain low until the converter is reset. The parallel data is valid for the entire time the E.O.C. is low.
5. The serial output is non-return to zero.
6. For the user's design flexibility, digital and analog grounds are brought out separately and must be externally connected. For optimum results, this external connection should be made as close to the converter as is possible.

APPLICATIONS INFORMATION

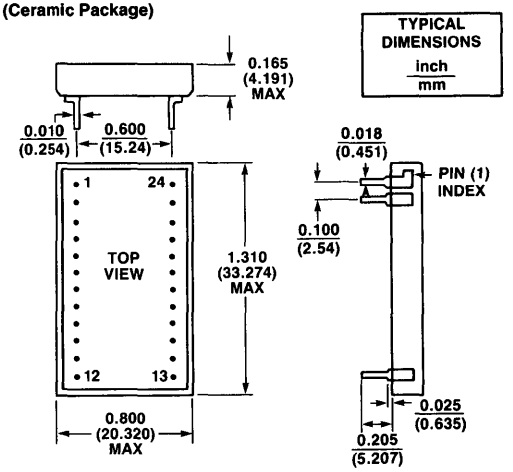
SERIAL TO PARALLEL CONVERSION



PIN DESIGNATIONS

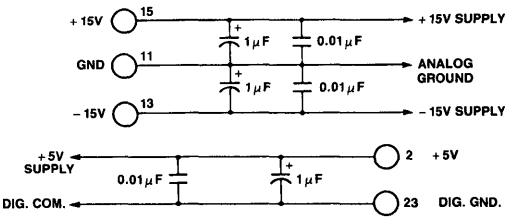
PIN NO.	FUNCTION	PIN NO.	FUNCTION
Pin 1	Start	Pin 24	Clock Input
Pin 2	+5V	Pin 23	DIG GND
Pin 3	Serial Out	Pin 22	E.O.C. (end of conversion)
Pin 4	Bit 6	Pin 21	Bit 7
Pin 5	Bit 5	Pin 20	Bit 8
Pin 6	Bit 4	Pin 19	Bit 9
Pin 7	Bit 3	Pin 18	Bit 10
Pin 8	Bit 2	Pin 17	Bit 11
Pin 9	MSB	Pin 16	LSB
Pin 10	No connection	Pin 15	+15V
Pin 11	Analog Ground	Pin 14	Analog in
Pin 12	N/C (int.ref.models) -V ref in (ext.ref.models)	Pin 13	-15V

MECHANICAL
(Ceramic Package)



Pin 1 is marked by a dot on the top of the package.

RECOMMENDED POWER SUPPLY BYPASS CIRCUITS

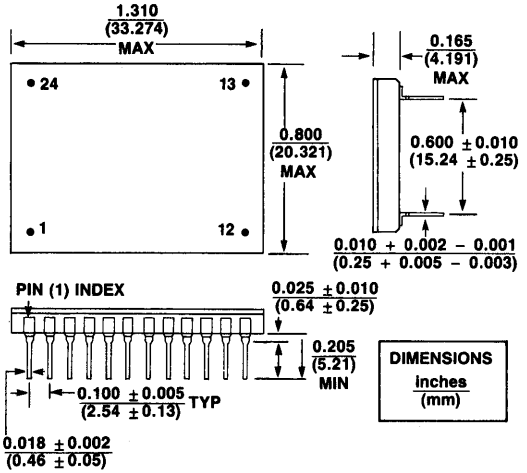


ORDERING INFORMATION

Model	Description
HS52XXC	Comm., 12-Bits, 13μS
HS52XXB	MIL, 12-Bits, 13μS

Model Selection Number

Specifications subject to change without notice.


1.310
(33.274)
MAX
• 24
13 •
• 1
12 •
0.800
(20.321)
MAX
0.165
(4.191)
MAX
0.600 ±0.010
(15.24 ±0.25)
0.010 + 0.002 − 0.001
(0.25 + 0.005 − 0.003)
PIN (1) INDEX
0.025 ±0.010
(0.64 ±0.25)
0.205
(5.21)
MIN
0.100 ±0.005
(2.54 ±0.13) TYP
0.018 ±0.002
(0.46 ±0.05)
DIMENSIONS
inches
(mm)

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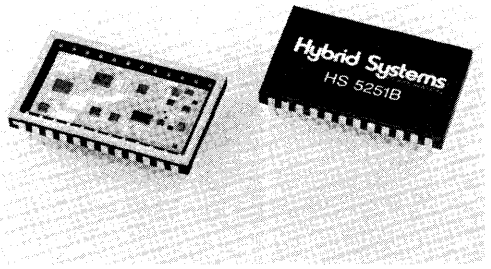
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS5251

12-BIT LOW POWER CMOS ADC

FEATURES

- Low power: 80mW
- Low standby power: 10nW
- Adjustment-free, ±0.0125% linearity
- Small size: 24-pin DIP
  Full Mil operation −55°C to +125°C
- Full MIL-STD-883, Class B or commercial processing
- Improved replacement for MN5251
- No missing codes: 0°C to +70°C



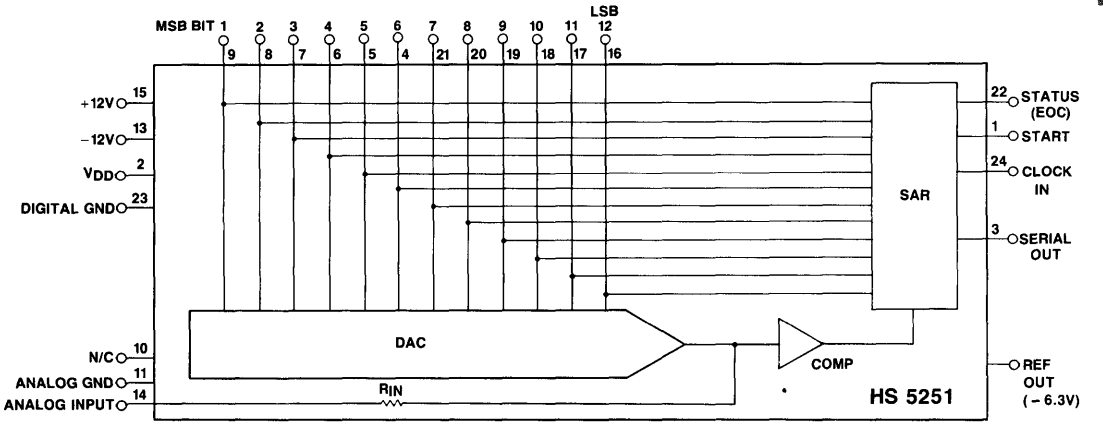
DESCRIPTION

The HS5251 Series is a complete adjustment free successive approximation type ADC requiring a low 80mW of power. The ADC provides digital output in both parallel or serial form. The HS5251 is packaged in a hermetically-sealed dual-in-line package and has the pinout of the popular HS5200 family of ADC's.

Miniature size, ultra low power consumption and adjustment free operation are product features. The HS5251 provides the user with the best possible performance in systems requiring maximum reliability in the smallest space. All converters are completely laser-trimmed, adjustment free, and incorporate highly stable thin-film resistor networks which provide long term maintenance free operation. Linearity of ±½ LSB is guaranteed over the entire operating temperature range.

All models of the HS5251 may be procured for operation over the −55°C to +125°C military temperature range ("B" models) with the same operating characteristics as the commercial 0°C to +70°C range. In addition, full military temperature range models are available screened to MIL-STD-883 Rev. C, Level B and are processed in accordance with the Method 5008.1.

FUNCTIONAL DIAGRAM



9

SPECIFICATIONS

(Typical @ +25°C with ±12V, and V_{DD} = +5V, unless otherwise specified)

SERIES	**HS 5251**
TYPE	Successive Approximation
RESOLUTION	12 Bits
ANALOG INPUTS	
Bipolar Range	±5V
Impedance	50kΩ
DIGITAL INPUTS (CMOS Compatible)	
Logic Level	
Logic 1	3.5V min, V_{DD} = +5V 8.4V min, V_{DD} = +12V
Logic 0	1.5 max, V_{DD} = +5V 3.5 max, V_{DD} = +12V
Loading	
Input Current	10pA
Input Capacitance	5pF
Pulse Width (Start)	750ns min, V_{DD} = +5V 250ns min, V_{DD} = +12V
Clock Input	
Frequency	71kHz max
Pulse Width	600ns min, V_{DD} = +5V 300ns min, V_{DD} = +12V
Rise/Fall Time	15μs max, V_{DD} = +5V 4μs max, V_{DD} = +12V
DIGITAL OUTPUTS	
Parallel Data	
Output Codes	
Unipolar	Complementary Binary
Bipolar	Complementary Offset Binary
Logic Levels	
Logic 1	4.95V min, V_{DD} = +5V 11.95V min, V_{DD} = +12V
Logic 0	0.01V max, V_{DD} = +5V 0.05V max, V_{DD} = +12V
Output Drive	
Logic 1	0.2mA min, V_{DD} = +5V, V_{OH} = 2.5V 0.3mA min, V_{DD} = +12V, V_{OH} = 11V
Logic 0	0.1mA min, V_{DD} = +5V, V_{OH} = 0.4V 1.0mA min, V_{DD} = +12V, V_{OH} = 1.5V
Serial Output	NRZ (see coding)

REFERENCE, INTERNAL	
Voltage	−6.3V ±5%
Drift	±15ppm/°C
Output Current	10μA max
CONVERSION TIME/ THROUGHPUT RATE	175μs max/5.7kHz
ACCURACY	
Linearity, +25°C	±0.012% max
Over Temperature (Tmin to Tmax)	
C-Model	±0.012% max
B-Model	±0.024% max
Differential Linearity	½ LSB
Monotonicity[5]	No Missing Codes
Absolute Accuracy[2] +25°C	±0.05% FSR, ±0.1% FSR max
Over Temperature (Tmin to Tmax)	
C-Model	±0.2% FSR, ±0.5% FSR max
B-Model	±0.3% FSR, ±0.6% FSR max
Zero Error, +25°C	±0.01% FSR, .1% max
Over Temperature (Tmin to Tmax)	
C-Model	±0.04% FSR, ±0.1% FSR max
B-Model	±0.05% FSR, ±0.1% FSR max
Gain Error	±0.05% FSR, .1% max
Gain TC	±20% ppm/°C
POWER SUPPLY	
Requirements	
+12V, rated	+11.64V to +12.36V, @ 3.5mA max
−12V, rated	−11.64V to −12.36V, @ −2.7mA max
V_{DD}[1] (+5V nominal)	+4.75 to +12.36, @ 1.0mA
Rejection Ratio	
+12V	±0.003% FSR/%
−12V	±0.03% FSR/%
V_{DD} (+5V nominal)	±0.0003% FSR/%
Power	56mW, 80mW max
TEMPERATURE	
Operating	
C-Model	0° to +70°C
B-Model	−55°C to +125°C
Storage	−65°C to +150°C

NOTES:
1. V_{DD} logic is CMOS compatible. It can vary between +5V and +12V as indicated.
2. Absolute accuracy includes all errors, gain, zero, and linearity.
3. For proper operation ±12V power supplies tolerance should not be greater than ±3%.
4. FSR is the abbreviation for "Full Scale Range" and is equal to the peak to peak output voltage, i.e. 10V for ±5V range.
5. No missing codes 0°C to +70°C

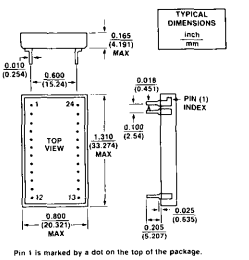
PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	START	24	CLOCK INPUT
2	V_{DD} (+5V)	23	DIGITAL GND
3	SERIAL OUT	22	STATUS (EOC)
4	BIT 6	21	BIT 7
5	BIT 5	20	BIT 8
6	BIT 4	19	BIT 9
7	BIT 3	18	BIT 10
8	BIT 2	17	BIT 11
9	BIT 1, MSB	16	BIT 12, LSB
10	N/C	15	+12V
11	ANALOG GROUND	14	ANALOG INPUT
12	REF OUT	13	−12V

ABSOLUTE MAXIMUM RATINGS

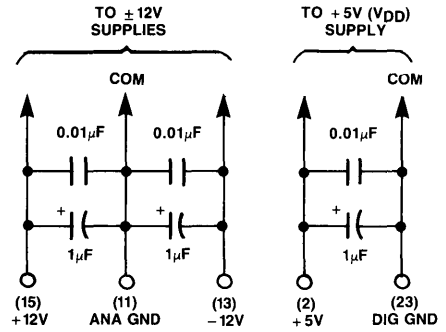
+12V Supply to Digital Common ..... +18V
−12V Supply to Digital Common ..... −18V
V_{DD} to Digital Common ..... −0.5V to +16V
Analog Input to Analog Common ..... ±25V
Digital Inputs to Digital Common ..... −0.5V to +V_{DD}

PACKAGE OUTLINE



APPLICATIONS INFORMATION

RECOMMENDED POWER SUPPLY BYPASS CIRCUIT

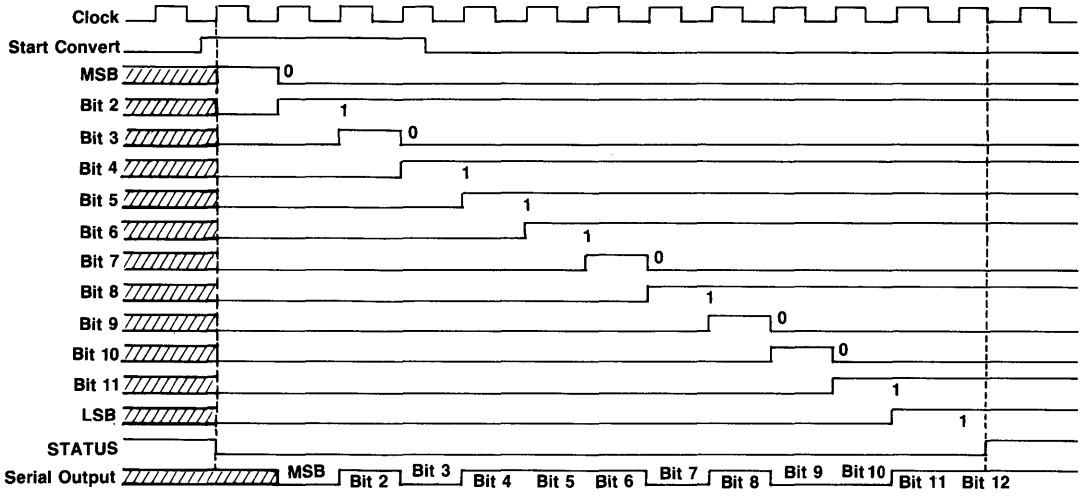


TRANSFER CHARACTERISTICS

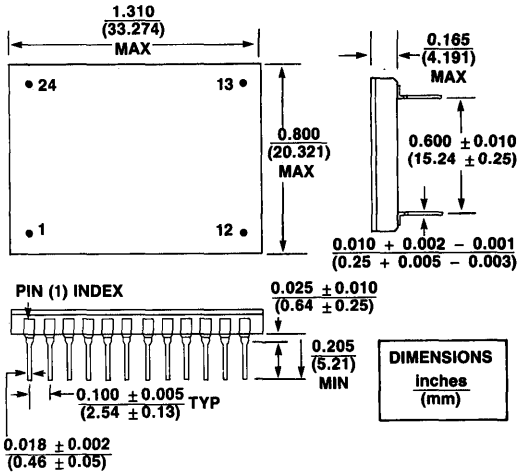
DIGITAL OUTPUT CODE MSB LSB	BIPOLAR INPUT VOLTAGE RANGE
000000000000	+4.9976
100000000000	0.0000V
111111111110*	−4.9976V

*The voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting the output bits indicated as 0 will change from "1" to "0" or from "0" to "1" as the input voltage passes through the level indicated.

TIMING DIAGRAM



NOTES:
1. Shaded areas shown for parallel data outputs denote bit states determined by successive approximation of analog input.
2. For continuous operation connect START (Pin 1) to STATUS (Pin 22)
3. Reset the converter by holding the start high during a low to high transition of the clock. The start must be high for a minimum of 300 nSec prior to the clock transition. The conversion will begin on the next low to high transition of the clock. The start may be set high at any time during a conversion to reset and begin again.
4. At the end of conversion, the E.O.C. will remain high until the converter is reset. The parallel data is valid for the entire time the E.O.C. is high.
5. The serial output is non-return to zero.
6. For the user's design flexibility, digital and analog grounds are brought out separately and must be externally connected. For optimum results, this external connection should be made as close to the converter as is possible.



CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 5251C-12	Comm., 12-Bits, Low Power ADC
HS 5251B-12	MIL, 12-Bits, Low Power ADC

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9516

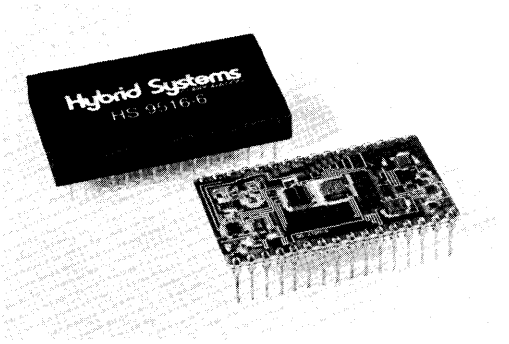
COMPLETE 0.0008% ACCURATE (16-BIT) ADC

FEATURES

- True 16-bit (±0.0008%) linearity error
- Full 16-bit resolution (1 part in 65,536)
- No missing codes (16-bits) 0°C to +70°C
- Six user selectable input ranges
- Completely self-contained
- Parallel data output
- Low full scale drift 10ppm/°C (max)

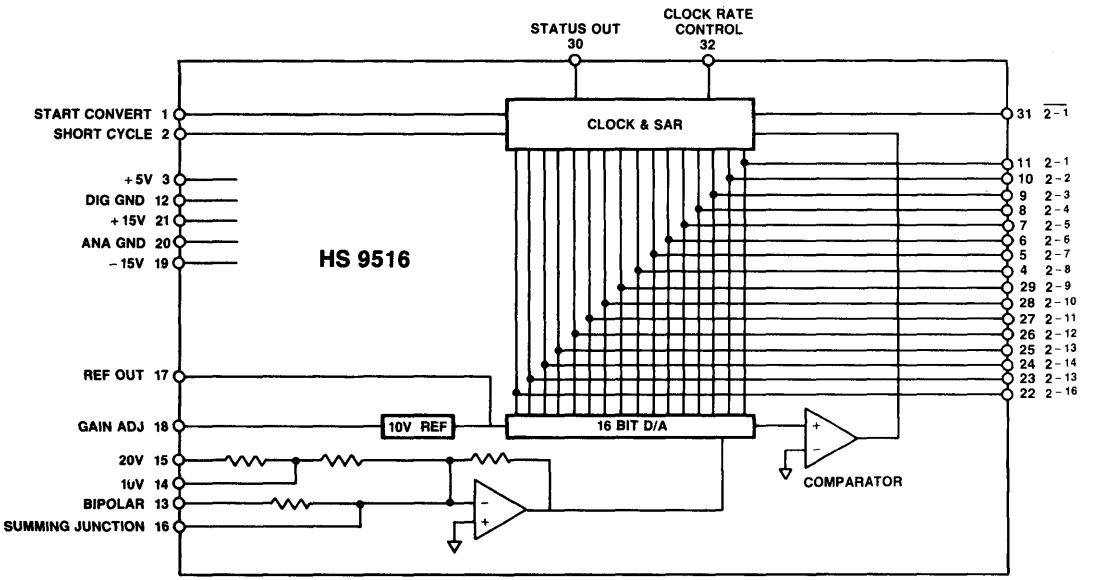
DESCRIPTION

The HS9516 is a 16-bit successive approximation analog to digital converter in a 32 pin triple DIP package. The 9516 is completely self-contained with clock, reference, comparator, successive approximation register and low power 16-bit DAC. It converts in 100 microseconds on 0 to +5V, 0 to +10V, 0 to +20V, ±2.5V, ±5V and ±10V input ranges. Output data is available in parallel binary and 2's complement formats. Short cycle and internal clock rate control may be externally adjusted to provide less conversion time at lower resolutions.



The HS9516 is available with 14-bit (±0.003% FSR), 15-bit (±0.0015% FSR) or 16-bit (±0.0008% FSR) nonlinearity. The B versions are fully screened and tested to MIL-STD-883C and are packaged in a hermetic 32-pin DIP.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

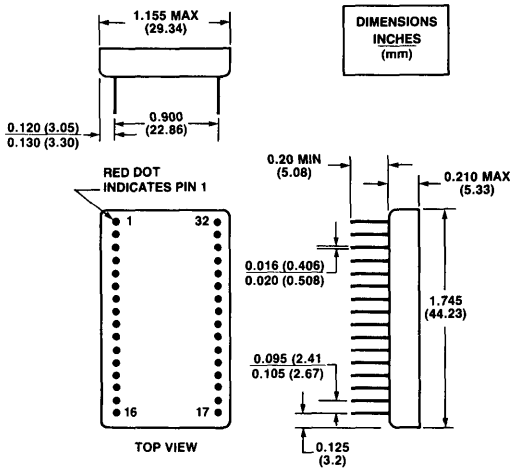
(Typical @ +25°C and nominal supply voltages)

MODEL	HS9516C-6	HS9516C-5	HS9516C-4	HS9516B-6	HS9516B-5	HS9516B-4
ANALOG INPUT						
Nominal Input Voltage Ranges	5V, 10V, 20V, ±2.5V, ±5V, ±10V	*	*	*	*	*
Absolute Max Input Voltage	±25V	*	*	*	*	*
Input Impedance	2.5KΩ on 5V ranges, 5KΩ on 10V ranges, 10KΩ on 20V ranges	*	*	*	*	*
Input Circuitry Settling Time	20μsec for full rated accuracy after FSR analog change	*	*	*	*	*
DIGITAL OUTPUTS						
Data Coding						
Unipolar	16-bits binary	*	*	*	*	*
Bipolar	Offset binary, 2's complement	*	*	*	*	*
Status Output	'H' = conversion in process; goes low 50nsec before LSB is stable	*	*	*	*	*
Logic '1' Voltage	2.4V min to 5V	*	*	*	*	*
Logic '0' Voltage	0V min to 0.4V max	*	*	*	*	*
Max Loading	2 std TTL loads, each output	*	*	*	*	*
DIGITAL INPUTS						
Start Convert	Positive pulse, 50nsec min width, initiates conversion on trailing edge. Must remain low during conversion.	*	*	*	*	*
Short Cycle	'H' enables conversion. Must be tied to logic supply for 16-bit conversion and to bit N + 1 for N bit conversion.	*	*	*	*	*
Logic '1' Voltage	2V min to 5.5V max	*	*	*	*	*
Logic '0' Voltage	−0.5V min to 0.8V max	*	*	*	*	*
Loading	1 LPTTL load max each input	*	*	*	*	*
POWER REQUIREMENTS						
+15V Supply Range	+15V ±10%	*	*	*	*	*
+15V Supply Current	30mA max	*	*	*	*	*
−15V Supply Range	−15V ±10%	*	*	*	*	*
−15V Supply Current	30mA max	*	*	*	*	*
+5V Supply Range	+5V ±10%	*	*	*	*	*
+5V Supply Current	60mA max	*	*	*	*	*
Total Power Dissipation	1.2W max	*	*	*	*	*
REFERENCE OUTPUT						
Voltage	+10V ±10%	*	*	*	*	*
Output Resistance	0.1Ω	*	*	*	*	*
Max Loading	±1mA	*	*	*	*	*
ACCURACY						
Quantization	±½ LSB	*	*	*	*	*
Scale Factor Error	±0.1% max[1]	*	*	*	*	*
Zero Error (Unipolar or Bipolar)	±0.1% FSR max[1]	*	*	*	*	*
Differential Linearity Error						
(% of FSR, max)	±0.0015	±0.003	±0.006	±0.0015	±0.003	±0.006
No Missing Codes[2]	16 bits	15 bits	14 bits	14 bits	**	**
Integral Linearity Error						
(% of FSR, max)	±0.0008 typ	±0.0015	±0.003	±0.0008 typ	±0.0015	±0.003
	±0.0015 max	±0.003	±0.006	±0.0015 max	±0.003	±0.006
Noise (2σp-p. RTI)	⅓ LSB	*	*	*	*	*
CONVERSION TIME[2]	100μsec max	*	*	*	*	*
STABILITY						
Scale Factor Tempco	±10ppm/°C max	*	*	*	*	*
Zero Tempco						
Unipolar	±2ppm FSR/°C	*	*	*	*	*
Bipolar	±5ppm FSR/°C	*	*	*	*	*
Integral Linearity Tempco	±1ppm FSR/°C max	*	*	*	*	*
Differential Linearity	±0.5ppm FSR/°C max	*	*	*	*	*
Change in Absolute Accuracy with Change in Power Supply Voltages						
+15V	0.002%/% ΔV_S max	*	*	*	*	*
−15V	0.002%/% ΔV_S max	*	*	*	*	*
+5V	0.002%/% ΔV_S max	*	*	*	*	*
ENVIRONMENTAL LIMITS						
Operating Temp Range	0°C to +70°C	*	*	−55°C to +125°C	**	**
Storage Temp Range	−55°C to +85°C	*	*	−65°C to +150°C	**	**
PACKAGE	Case A	*	*	Case A	**	**

NOTES: 1. Adjustable to zero. 2. Over full operating temperature range.

*Specifications same as HS 9516C-6. **Specifications same as HS 9516B-6.

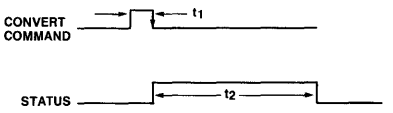
PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	START CONVERT	32	CLOCK RATE CONTROL
2	SHORT CYCLE	31	$\overline{2^{-1}}$
3	+5V	30	STATUS OUT
4	2^{-8}	29	2^{-9}
5	2^{-7}	28	2^{-10}
6	2^{-6}	27	2^{-11}
7	2^{-5}	26	2^{-12}
8	2^{-4}	25	2^{-13}
9	2^{-3}	24	2^{-14}
10	2^{-2}	23	2^{-15}
11	2^{-1} (MSB)	22	2^{-16} (LSB)
12	DIG GND	21	+15V
13	BIPOLAR	20	ANA GND
14	10V INPUT	19	−15V
15	20V INPUT	18	GAIN ADJ
16	SUMMING JUNCTION	17	REF OUT

TIMING



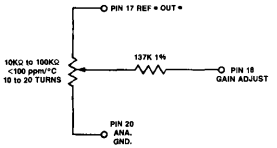
$t_1 \geq$ 50nsec CONVERT COMMAND MUST STAY LOW
$t_2 \leq$ 100μsec

PIN 2 CONNECTS TO	16-BIT	15-BIT	14-BIT	13-BIT	12-BIT
	+5V	Pin 22	Pin 23	Pin 24	Pin 25

SHORT CYCLE CONNECTIONS

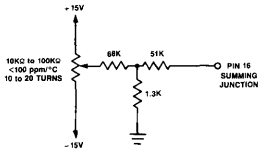
APPLICATIONS INFORMATION

OPTIONAL OFFSET AND GAIN ADJUSTMENTS



GAIN ADJUST CIRCUIT MIN ADJUST RANGE = ±0.2% FSR

Unipolar & Bipolar: Apply +F.S. −3/2 LSB analog input and set the potentiometer for a digital output that alternates between 111...1 and 111...0.



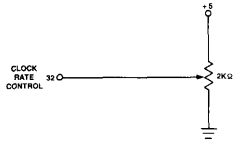
OFFSET ADJUST CIRCUIT MIN ADJUST RANGE = +0.2% FSR

Unipolar: Apply +½ LSB analog input and set potentiometer for a digital output that alternates between 000...0 and 000...1.
Bipolar: Apply +½ LSB and set potentiometer for a digital output that alternates between 1000...0 and 1000...1.

CONNECTIONS FOR VARIOUS INPUT RANGES

INPUT RANGE	ANALOG IN TO PIN	CONNECT PIN 13 TO	NOTES
−2.5V to +2.5V	14	17	Connect pins 15 + 16
−5V to +5V	14	17	
−10V to +10V	15	17	
0V to 5V	14	20	Connect pins 15 + 16
0V to 10V	14	20	
0V to 20V	15	20	

CLOCK RATE CONTROL



ADJUSTMENT RANGE IS 50μsec to 200μsec at 16-BIT RESOLUTION

The HS 9516 clock rate is set by the factory for a conversion time of 100μsec, i.e. Pin 32 left open. For higher or lower clock rates, connect Pin 32 to a multi-turn potentiometer as shown above.

GROUNDING AND POWER SUPPLY DECOUPLING

Connect Analog GND to Digital GND at package pins. If not possible, connect 1μf* tantalum capacitor in parallel with a 0.1μf ceramic capacitor between Analog GND and Digital GND pins. Decouple +15V and −15V supplies to Analog GND and +5V supply to Digital GND at package pins with 1μf tantalum and 0.1μf ceramic capacitors.

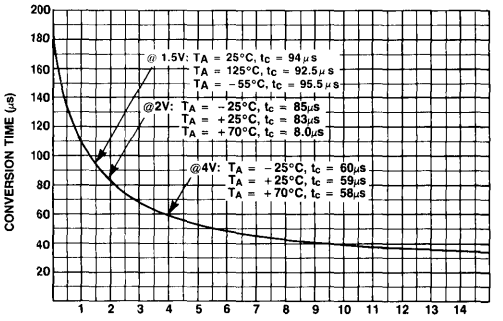
*Non-polarized

TRANSFER CHARACTERISTICS

	BIPOLAR INPUT VOLTAGE RANGE			UNIPOLAR INPUT VOLTAGE RANGE		
MSB LSB	±2.5	±5V	±10V	0 to 5V	0 to 10V	0 to 20V
111111111111110[3]	2.49989V	5.99977V	9.99954V	4.99989V	9.99977V	19.99954V
0000000000000000	−0.038mV	−0.076mV	−0.153mV	2.49996V	4.99992V	9.99985V
0000000000000000	−2.49992V	−4.99992V	−9.99985V	−0.038mV	−0.076mV	−0.153mA

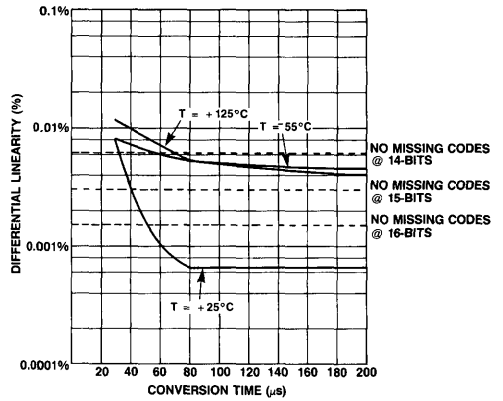
NOTES:
1. Codings shown are binary and offset binary. Use $\overline{MSB}$ for 2's complement coding. 2. One LSB = FSR/2^{16} 3. The voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting the output bits indicated as 0 will change from "1" to "0" or from "0" to "1" as the input voltage passes through the level indicated.

TYPICAL CHARACTERISTIC CURVES

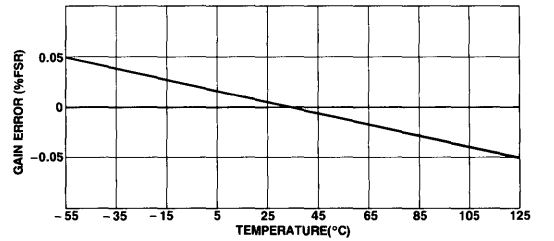


CONVERSION TIME VS. CONTROL VOLTAGE, T_A = +25°C

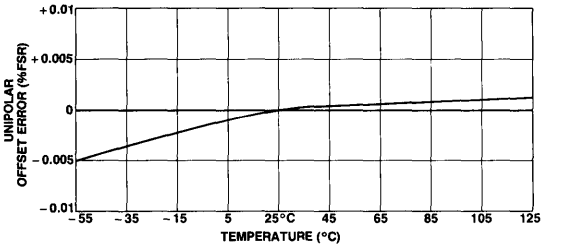
NOTE: CONVERSION TIME WILL BE 100μsec MAX IF VOLTAGE TO PIN 32 IS 'OPEN', AND TYPICALLY 200μsec IF PIN 32 IS AT 0V (GROUND).



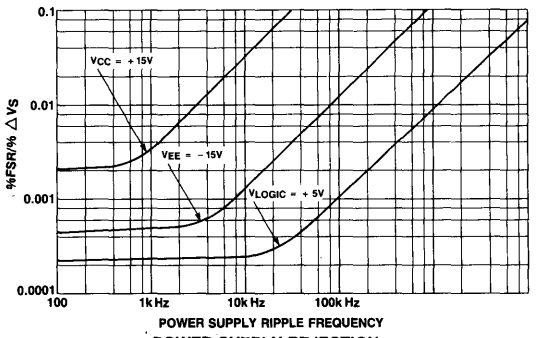
HS 9516-6 DIFFERENTIAL LINEARITY VS. CONVERSION TIME



GAIN DRIFT VS. TEMPERATURE



OFFSET DRIFT VS. TEMPERATURE



POWER SUPPLY REJECTION

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 9516C-6	16-Bit ADC with ±0.001% Integral Linearity, 0°C to 70°C
HS 9516C-5	16-Bit ADC with ±0.0015% Integral Linearity, 0°C to 70°C
HS 9516C-4	16-Bit ADC with ±0.003% Integral Linearity, 0°C to 70°C
HS 9516B-6	16-Bit ADC with ±0.001% Integral Linearity, −55°C to +125°C
HS 9516B-5	16-Bit ADC with ±0.0015% Integral Linearity, −55°C to +125°C
HS 9516B-4	16-Bit ADC with ±0.003% Integral Linearity, −55°C to +125°C

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

NOT RECOMMENDED FOR NEW DESIGNS SEE SP9550

SP9548

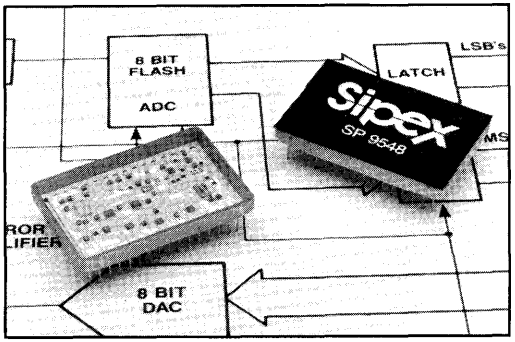
2 MHz, MULTIPASS™ 12-BIT A/D CONVERTER

DESCRIPTION

The SP9548 is a 12-bit, 500 nanosecond, analog-to-digital converter employing the SIPEX state-of-the-art Multipass™ subranging Flash technology while consuming much less than 2 Watts. The subranging Multipass process is optimized for low power operation by multiplexing a single 8-bit Flashe for each of the two ranges to yield a final resolution of 12 bits

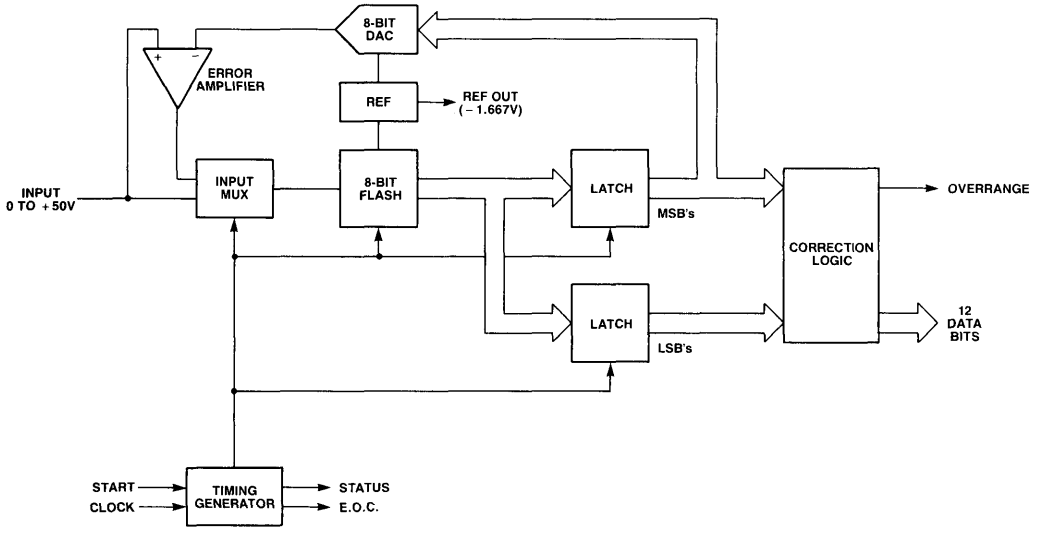
The SP9548 can be used in either a single or continuous mode. In the single mode, a START command initiates the conversion on the next CLOCK cycle. Total conversion can is completed in 500 nanoseconds...in synch with the clock.

In the continuous mode, the SP9548 can operate at a 2 MHz sampling rate and can be interfaced with the HS9720 Sample/Hold Amplifier. The SP9548 provides a control signal to the HS9720 permitting the S/H to begin tracking as soon as the Flash has latched the subrange data. This results in no conversion time degradation for the SP9548/HS9720 pair...the sampling time remains 2 MHz.



The SP9548 input range, 0 to +5V, has been optimized for high speed applications such as radar, sonar and video digitization, and high speed data acquisition systems. The SP9548 is ideal in all applications that require 12-bit performance at high speed with low power consumption.

FUNCTIONAL DIAGRAM



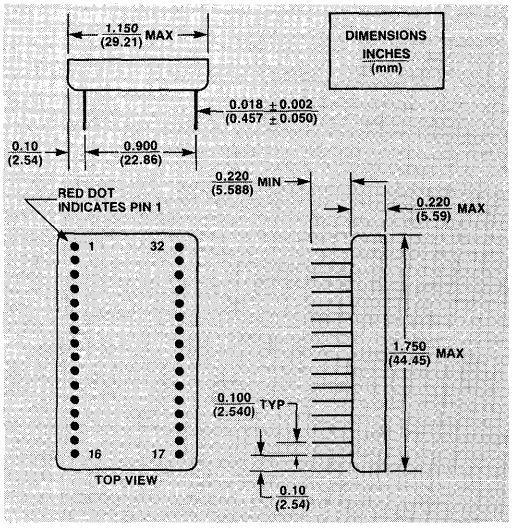
9

SPECIFICATIONS

(Typical @25°C and nominal supply voltages unless otherwise specified.)

MODEL	SP 9548
RESOLUTION	12-Bits
ANALOG INPUTS	
Input Voltage Range	0 to +5V
Input Impedance	1kΩ
DIGITAL INPUTS	
Logic Levels: Logic "1"	2.4V min
Logic "0"	0.4V max
Logic Loading	1 TTL Load
ACCURACY	
Integral Linearity	
@25°C	±½ LSB
0°C to +70°C	±1 LSB
Differential Linearity	
@25°C	±½ LSB
0°C to +70°C	±1 LSB
No Missing Codes	Guaranteed
Offset Error	0.1% of FSR typ, 0.3% max
Gain Error	0.2% of FSR typ, 0.5% max
DYNAMIC PERFORMANCE	
Conversion Time	500nsec
STABILITY	
Integral Linearity Tempco	10 ppm/°C
Differential Linearity Tempco	2 ppm/°C
Unipolar Offset Error Drift	5 ppm/°C
Gain Error Drift	40 ppm/°C
DIGITAL OUTPUTS	
Output Coding (Straight Binary)	See Table
Output Drive Capability	4 TTL Loads
REFERENCE	
Voltage	-1.67V nom
External Current	5mA
POWER SUPPLY REQUIREMENTS	
Current @nominal Voltage	
+15V (±10%)	20mA
-15V (±10%)	20mA
+5V Digital (±10%)	100mA
+5V Analog (±1%)	50mA
-5V (±1%)	50mA
Dissipation	1.6W typ, 2.0W max
PACKAGE	
Triple DIP — Metal	32-Pin

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	CLOCK	32	START
2	STATUS	31	+5V DIGITAL
3	EOC	30	DIGITAL GND
4	BIT 12 (LSB)	29	+5V ANALOG
5	BIT 11	28	-5V
6	BIT 10	27	ANALOG GND
7	BIT 9	26	ANALOG GND
8	BIT 8	25	-15V
9	BIT 7	24	+15V
10	BIT 6	23	REF OUT
11	BIT 5	22	TEST POINT
12	BIT 4	21	NC
13	BIT 3	20	TEST POINT
14	BIT 2	19	NC
15	BIT 1 (MSB)	18	TRIM
16	OVERRANGE	17	ANALOG INPUT

THEORY OF OPERATION

INTERFACE INFORMATION

The SP 9548 is designed primarily for high speed applications that require a sampling rate of up to 2 MHz. It should be noted that the SP 9548 will also operate at slower rates than 2 MHz with no degradation in performance. The rate of conversion is set by the CLOCK signal that is applied to it. For ideal operation the CLOCK signal should be a square wave at twice the desired sampling rate...it takes two clock cycles for a total conversion.

The input stage has been designed for fast settling so as to function in a data acquisition environment with S/H amplifiers and multiplexers. As such, the input signal should be driven by a low impedance source sufficient to drive the 1K ohm input impedance at 12-bit accuracy. Most S/H amplifiers and fast operational amplifiers are adequate.

CONVERSION PROCESS

As shown in the block diagram, the input analog signal is attenuated and switched, via the input multiplexer (INPUT MUX) to the input of the 8-BIT FLASH ADC. The FLASH converter also receives a reference voltage (REF) of 1.667 volts. The input signal is compared to this reference in the conversion process by the FLASH converter and the resulting digital 8-bit word, which represents the most significant bits (MSB), is internally latched for further processing by both the 8-bit DAC and the CORRECTION LOGIC.

The above sequence is refered to as the "first pass" or "input" conversion. The resulting 8-bit word is sent to an 8-bit DAC which is trimmed to better than 12-bit accuracy. The DAC output is then directly subtracted from the input signal to determine the "error" or "second pass" input signal to be converted by the Flash.

The "second pass" occurs when the INPUT MUX switches the ERROR AMPLIFIER output to the input of the FLASH converter. The result of this conversion process is a digital word which represents the least significant bits (LSB). This digital output is also latched for processing by the CORRECTION LOGIC.

INPUT VOLTAGE	BINARY BITS OR	1	2	3	4	5	6	7	8	9	10	11	12	HEX CODE
0.00000		0	0	0	0	0	0	0	0	0	0	0	0	0 0 0 0
0.00122		0	0	0	0	0	0	0	0	0	0	0	1	0 0 0 1
2.49878		0	1	1	1	1	1	1	1	1	1	1	1	0 7 F F
2.50000		1	0	0	0	0	0	0	0	0	0	0	0	0 8 0 0
2.50122		1	0	0	0	0	0	0	0	0	0	0	1	0 8 0 1
4.99878		1	1	1	1	1	1	1	1	1	1	1	1	0 F F F
5.00000	1	0	0	0	0	0	0	0	0	0	0	0	0	1 0 0 0
5.00122	1	0	0	0	0	0	0	0	0	0	0	0	1	1 0 0 1
5.29175	1	0	0	0	0	1	1	1	0	1	1	1	1	1 0 E F
5.83%	Overrange													

SP 9548 Coding Table @5 Volt Full Scale

The CORRECTION LOGIC accepts the 8 MSB's and the 8 LSB's and combines them by an improved, unique algorithm using digital addition. The result is a 12-bit digital word which accurately represents the analog input. The CORRECTION LOGIC also provides an overrange (O.R.) bit to indicate that the input has exceeded full scale. The output coding is straight binary. Refer to Coding Table.

The entire conversion process is controlled by the TIMING GENERATOR which requires requires a square wave CLOCK at twice the sampling speed i.e., the clock should be 4 MHz for 2 MHz operation. This is not to be confused with the Nyquist Criterion...2 MHz sampling can only convert input signals up to 1 MHz. The SP 9548 requires two such clock cycles (4 MHz) for a complete (2 MHz) sampling cycle or (500nsec) conversion.

SINGLE CONVERSION MODE

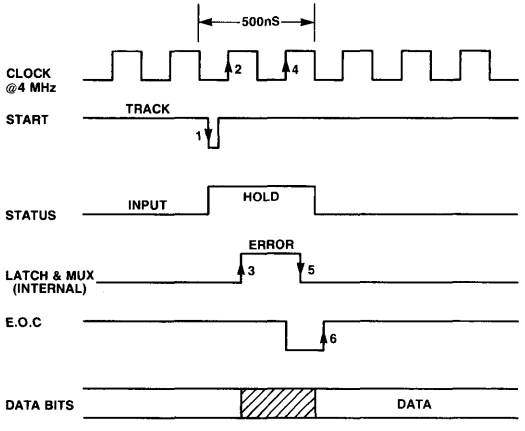
The single conversion mode is shown on the TIMING GENERATOR timing diagram. The timing sequence shown reflects the nominal minimum conversion time required...the START pulse is applied just before the rising edge of the clock. If the START pulse is applied immediately after the rising edge of the clock, the process will not begin until the next clock cycle.

If the START pulse is applied asynchronously then the conversion time will vary with the relationship of the START pulse to the clock...in any case the resulting data will still be accurate even though the conversion time may be varying from 350nsec to 850nsec.

Referring to the timing diagram, the process is as follows:

1. Negative going START pulse (50nsec min) is applied to the SP 9548 initiating conversion. In this mode the STATUS signal can be used to control a S/H amplifier as shown.
2. The rising edge of the next CLOCK cycle causes the FLASH to perform a conversion to determine the MSB's.
3. The FLASH data is latched for the DAC and accordingly the INPUT MUX is switched to the ERROR AMPLIFIER connecting it to the FLASH converter.
4. On the next CLOCK cycle, positive edge, the FLASH converts the error to determine the LSB's.
5. The FLASH data is latched for the CORRECTION LOGIC.
6. The positive edge of the E.O.C. (end of conversion) signal can be used to externally latch the valid data to the outside world. Note, that the data is not valid during the conversion process as indicated by the STATUS signal.

Note, that if the START pulse stays negative for more than two clock pulses a second conversion process will commence. If this happens the STATUS signal will stay high until that conversion is completed. In fact, if the START pulse is kept low...the SP 9548 will be in the continuous mode of operation.



SP 9548 Timing Diagram: Single Conversion Mode

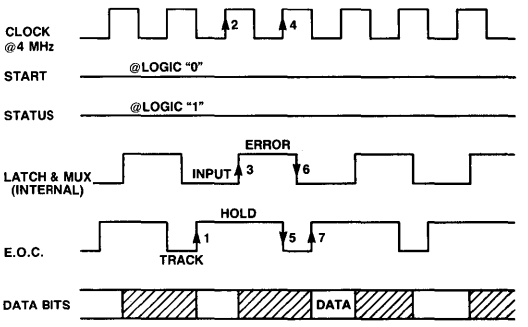
CONTINUOUS CONVERSION MODE

The SP 9548 will be in the continuous conversion mode as long as the START signal is kept low. This mode is used to follow high speed input signals and is capable of up to a 1 MHz (Nyquist Limit) input signal at a 2 MHz sampling rate by simply applying a 4 MHz CLOCK to the SP 9548. Since the STATUS signal will remain high during this mode, the E.O.C. signal should be used to control an input S/H amplifier. Also, by using the E.O.C. signal the maximum conversion rate will not be affected by the addition of the S/H process. Of course, the S/H amplifier should be of the high speed variety such as the HS 9720.

Referring to the timing diagram, the process is as follows:

1. The positive edge of the E.O.C. signal causes the external S/H, HS 9720 or equivalent, to hold the input signal.
2. The rising edge of the next CLOCK cycle causes the FLASH to perform a conversion to determine the MSB's.
3. The FLASH data is latched for the DAC and accordingly the INPUT MUX is switched to the ERROR AMPLIFIER connecting it to the FLASH converter.
4. On the next CLOCK cycle, positive edge, the FLASH converts the error to determine the LSB's.
5. The negative edge of the E.O.C. causes the S/H amplifier to track the input signal in preparation for the next conversion cycle.
6. The FLASH data is latched for the CORRECTION LOGIC.
7. The positive edge of the E.O.C. (end of conversion) signal can be used to externally latch the valid data to the outside world. Note, that the data is not valid during the conversion process as indicated by the STATUS signal.

The process is repeated continuously as shown in the timing diagram. The STATUS signal remains high as long as the START pulse remains low and the SP 9548 is in the continuous conversion mode.

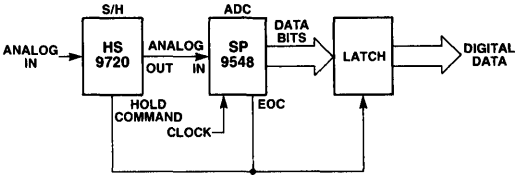


SP 9548 Timing Diagram: Continuous Conversion Mode

TYPICAL APPLICATIONS

The application block diagram illustrates a typical system using the SP 9548 with an external S/H amplifier such as the HS 9720 and an external latch for the data bits. Note that the E.O.C. signal from the SP 9548 can be used for both the hold command and the latch strobe.

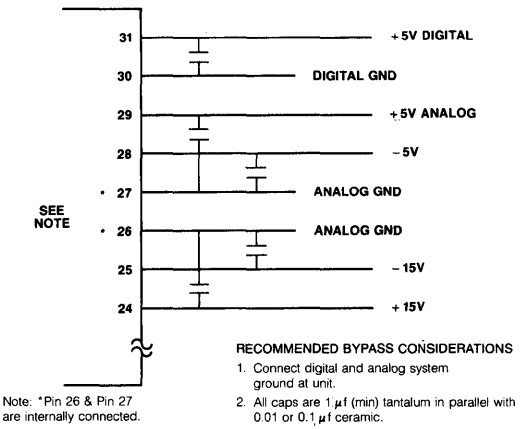
The SP 9548 can be used directly without a S/H amplifier to take a quick snapshot of a slow moving input signal. The maximum input frequency that can be followed without a S/H amplifier is approximately 20 kHz which allows for the conversion of audio band signals.



Typical Application: SP 9548 Continuous Mode With External S/H Amplifier & External Latch

POWER SUPPLY CONNECTIONS

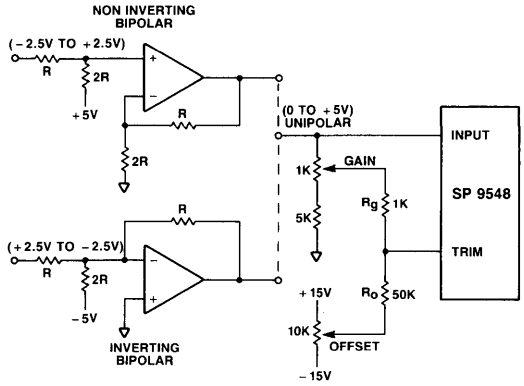
As shown in the Power Supply Connection diagram, 5 pairs of capacitors are recommended for bypassing the power supplies at the SP 9548. Also note that it is recommended to externally connect the analog and digital grounds at the SP 9548. Also, the analog and digital +5V supplies should be separate for optimum performance.



SP 9548 Power Supply Connections

TRIM ADJUSTMENTS

The SP 9548 can be externally trimmed for gain and offset as shown in the block diagram. To change the sensitivity of the gain trim, increase or decrease the value of R_g (1K ohm). To change the sensitivity of the offset trim, increase or decrease the value of R_O (50k ohm). The interaction of the gain and offset trim is minimal; some readjustment may have to be made if one or the other trim is extreme.



To change sensitivity of GAIN Trim increase/decrease R_g.
To change sensitivity of OFFSET Trim increase/decrease R_O.

SP 9548 Fine Trim Adjustments

BIPOLAR OPERATION

Since the SP 9548 is a unipolar A/D converter, bipolar operation can only be obtained by level shifting the input signal. The FINE TRIM block diagram illustrates this process for either inverting or non-inverting operation using a suitable Operational Amplifier. The value of R should be carefully selected for speed and accuracy. The GAIN and OFFSET adjustments can be used to trim the final input range as previously described.

SUMMARY

The SP 9548 has been designed to simplify high speed conversion and operate at reasonably low power levels. The subranging technique and correction logic have been optimized to provide the accuracy. With this in mind, the SP 9548 is a reasonable solution to most high speed data conversion problems.

ORDERING INFORMATION

MODEL	OPERATING TEMPERATURE RANGE	SCREENING
SP 9548C	0 to +70°C	—

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Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP9550

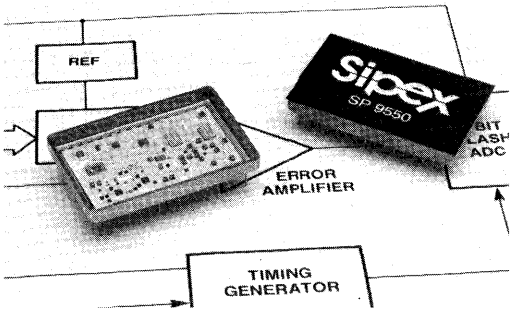
5 MHz, MULTIPASS™ 12-BIT A/D CONVERTER

DESCRIPTION

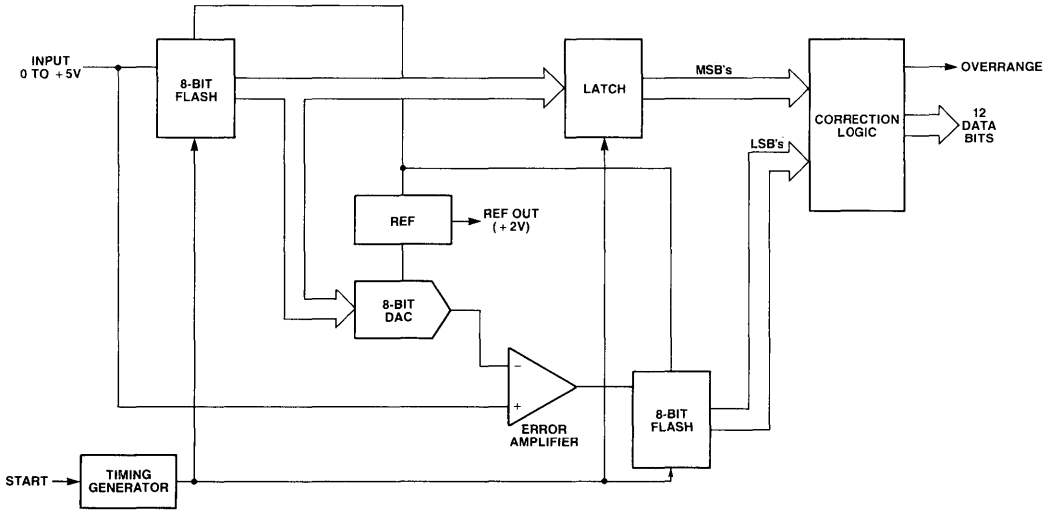
The SP9550 is a 12-bit, 200 nanosecond, analog-to-digital converter employing the SIPEX state-of-the-art Multipass™ subranging Flash technology. The subranging Multipass process is optimized for high accuracy operation by using two 8-bit Flashes in a feed-forward error correction scheme to yield a final resolution of 12 bits while consuming less than 2.5 watts.

The SP9550 can be used in either a single or continuous mode. In the single mode, a START command initiates the conversion on its rising edge and completes the conversion on its falling edge. Total conversion can be completed in less than 200 nanoseconds. By repeating the START command every 200 nanoseconds, the SP9588 will operate in a continuous mode at a maximum of 5 MHz.

The SP9550 input range, 0 to +5V, has been optimized for high accuracy applications such as radar, sonar and video digitization, and high speed data acquisition systems. The SP9550 is ideal in all applications that require 12-bit performance at relatively high speed with moderately low power consumption.



FUNCTIONAL DIAGRAM



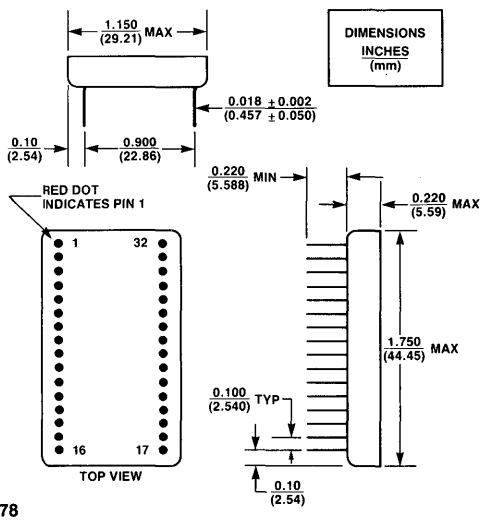
9

SPECIFICATIONS

(Typical @25°C and nominal supply voltages unless otherwise specified.)

MODEL	SP 9550
RESOLUTION	12-Bits
ANALOG INPUTS	
Input Voltage Range	0 to +5V
Input Impedance	1kΩ
DIGITAL INPUTS	
Logic Levels: Logic "1"	2.4V min
Logic "0"	0.4V max
Logic Loading	1 TTL Load
ACCURACY	
Integral Linearity	
@25°C	±½ LSB
0°C to +70°C	±1 LSB
Differential Linearity	
@25°C	±½ LSB
0°C to +70°C	±1 LSB
No Missing Codes	Guaranteed
Offset Error	0.2% of FSR typ, 0.5% max
Gain Error	0.2% of FSR typ, 0.5% max
DYNAMIC PERFORMANCE	
Conversion Time	200nsec
STABILITY	
Integral Linearity Tempco	10 ppm/°C
Differential Linearity Tempco	2 ppm/°C
Unipolar Offset Error Drift	5 ppm/°C
Gain Error Drift	40 ppm/°C
DIGITAL OUTPUTS	
Output Coding (Straight Binary)	See Table
Output Drive Capability	4 TTL Loads
REFERENCE	
Voltage	+2.0V nom
External Current	5mA
POWER SUPPLY REQUIREMENTS	
Current @nominal Voltage	
+15V (±10%)	15mA
−15V (±10%)	15mA
+5V Digital (±10%)	225mA
+5V Analog (±1%)	125mA
−5V (±1%)	75mA
Dissipation	2.4W typ, 2.7W max
PACKAGE	
Triple DIP — Metal	32-Pin

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	START (CLOCK)	32	NC
2	NC*	31	+5V DIGITAL
3	NC*	30	DIGITAL GND
4	BIT 12 (LSB)	29	+5V ANALOG
5	BIT 11	28	−5V
6	BIT 10	27	ANALOG GND
7	BIT 9	26	ANALOG GND
8	BIT 8	25	−15V
9	BIT 7	24	+15V
10	BIT 6	23	REF OUT
11	BIT 5	22	TEST POINT
12	BIT 4	21	NC
13	BIT 3	20	TEST POINT
14	BIT 2	19	NC
15	BIT 1 (MSB)	18	TRIM
16	OVERRANGE	17	ANALOG INPUT

*Internally connected to ground.

THEORY OF OPERATION

INTERFACE INFORMATION

The SP 9550 is designed primarily for high speed applications that require a conversion time as low as 200 nanoseconds (185ns min). Of course, the SP 9550 will operate at slower conversion times with no degradation. The rate of conversion is set by the START signal that is applied to it. The rising edge of the START signal initiates the conversion process and the falling edge of the START signal completes the process.

The input stage has been designed for fast settling so as to function in a data acquisition environment with S/H amplifiers and multiplexers. As such, the input signal should be driven by a low impedance source sufficient to drive the 1K ohm input impedance at 12-bit accuracy. Most S/H amplifiers and fast operational amplifiers are adequate...but some thought must be given to their selection.

CONVERSION PROCESS

As shown in the block diagram, the input analog signal is directed to the input of the first 8-BIT FLASH ADC. The FLASH converter also receives a reference voltage (REF) of 2.0 volts. The input signal is compared to this reference in the conversion process by the FLASH converter and the resulting digital 8-bit word, which represents the most significant bits (MSB), is internally latched for further processing by both the 8-bit DAC and the CORRECTION LOGIC.

The above sequence is refered to as the "first pass" or "input" conversion. The resulting 8-bit word is sent to an 8-bit DAC which is trimmed to better than 12-bit accuracy. The DAC output is then directly subtracted from the input signal to determine the "error" or "second pass" input signal to be converted by the Flash.

The "second pass" occurs when the ERROR AMPLIFIER output is directed to the input of the second FLASH converter. The result of this conversion process is a digital word which represents the least significant bits (LSB). This digital output is now ready for further processing by the CORRECTION LOGIC.

INPUT VOLTAGE	BINARY BITS OR	1	2	3	4	5	6	7	8	9	10	11	12	HEX CODE
0.00000		0	0	0	0	0	0	0	0	0	0	0	0	0 0 0 0
0.00122		0	0	0	0	0	0	0	0	0	0	0	1	0 0 0 1
2.49878		0	1	1	1	1	1	1	1	1	1	1	1	0 7 F F
2.50000		1	0	0	0	0	0	0	0	0	0	0	0	0 8 0 0
2.50122		1	0	0	0	0	0	0	0	0	0	0	1	0 8 0 1
4.99878		1	1	1	1	1	1	1	1	1	1	1	1	0 F F F
5.00000	1	0	0	0	0	0	0	0	0	0	0	0	0	1 0 0 0
5.00122	1	0	0	0	0	0	0	0	0	0	0	0	1	1 0 0 1
5.29175	1	0	0	0	0	1	1	1	0	1	1	1	1	1 0 E F
5.83%	Overrange													

SP 9550 Coding Table @5 Volt Full Scale

The CORRECTION LOGIC accepts the 8 MSB's and the 8 LSB's and combines them by an improved, unique algorithm using digital addition. The result is a 12-bit digital word which accurately represents the analog input. The CORRECTION LOGIC also provides an overrange (O.R.) bit to indicate that the input has exceeded full scale. The output coding is straight binary. Refer to Coding Table.

The entire conversion process is controlled by the TIMING GENERATOR which only requires a START signal as previously described. The falling edge of the START signal indicates that the digital data is ready.

SINGLE CONVERSION MODE

The single conversion mode is shown on the TIMING GENERATOR timing diagram. The timing sequence shown reflects the nominal minimum conversion time required.

Referring to the timing diagram, the process is as follows:

1. The rising edge of the START signal causes the first FLASH to perform a conversion to determine the MSB's. Old data from the previous conversion remains intact.
2. The falling edge of the START signal causes the second FLASH to perform a conversion to determine the LSB's. New data will be valid 50 nanoseconds later.

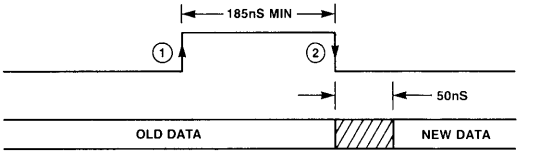
CONTINUOUS CONVERSION MODE

The SP 9550 will be in the continuous conversion mode as long as the START signal is repeated. This mode is used to follow high speed input signals and is capable of a 5 MHz converting rate. However, an external S/H amplifier is required...the time necessary for the S/H amplifier to acquire and settle must be taken into consideration.

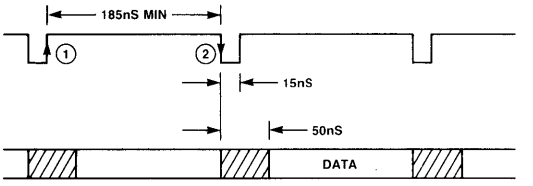
Referring to the timing diagram, the process is as follows:

1. The rising edge of the START signal causes the first FLASH to perform a conversion to determine the MSB's. Old data from the previous conversion reamins intact.
2. The falling edge of the START signal causes the second FLASH to perform a conversion to determine the LSB's. New data will be valid 50 nanoseconds later.

The process is repeated continuously as shown in the timing diagram. When operating at the maximum rate of 5 MHz, the START signal should be high for only 185 nanoseconds and low for 15 nanoseconds. When using an external S/H amplifier, the START signal should be high for the full 200 nanoseconds and low for the time required for the S/H amplfier to acquire and settle. The resulting conversion rate will be proportional to the total time required for both the S/H amplifier and the SP 9550.



SINGLE CONVERSION



5 MHZ CONVERSION

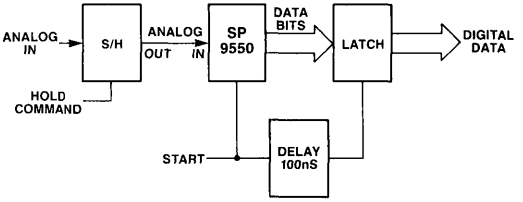
SP 9550 Timing Diagram

TYPICAL APPLICATIONS

The application block diagram illustrates a typical system using the SP 9550 with an external S/H amplifier and an external latch for the data bits. Since the data is valid 50 nanoseconds after the falling edge of the START signal, the START signal needs to be de-

layed by more than 50 nanoseconds if it is to be used as the strobe for the latch.

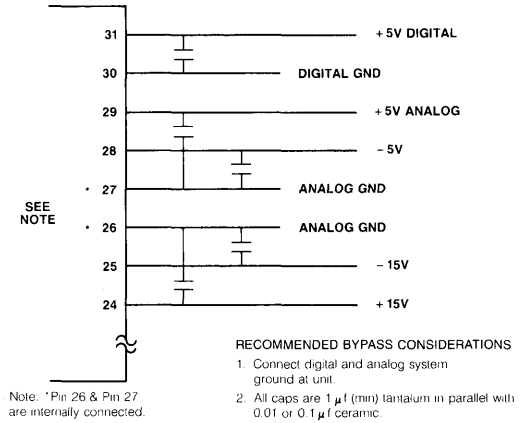
The SP 9550 can be used directly without a S/H amplifier to take a quick snapshot of a slow moving input signal. The maximum input frequency that can be followed without a S/H amplifier is approximately 20 kHz which allows for the conversion of audio band signals.



Typical Application: SP 9550 With External S/H Amplifier & External Latch

POWER SUPPLY CONNECTIONS

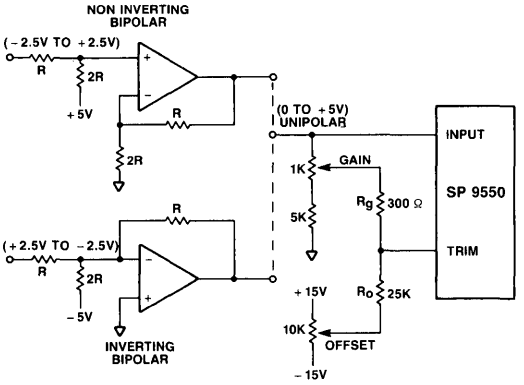
As shown in the Power Supply Connection diagram, 5 pairs of capacitors are recommended for bypassing the power supplies at the SP 9550. Also note that it is recommended to externally connect the analog and digital grounds at the SP 9550. Also, the analog and digital +5V supplies should be separate for optimum performance.



SP 9550 Power Supply Connections

TRIM ADJUSTMENTS

The SP 9550 can be externally trimmed for gain and offset as shown in the block diagram. To change the sensitivity of the gain trim, increase or decrease the value of R_g (300 ohm). To change the sensitivity of the offset trim, increase or decrease the value of R_O (25k ohm). The interaction of the gain and offset trim is minimal; some readjustment may have to be made if one or the other trim is extreme.



To change sensitivity of GAIN Trim increase/decrease R_g.
To change sensitivity of OFFSET Trim increase/decrease R_O.

SP 9550 Fine Trim Adjustments

BIPOLAR OPERATION

Since the SP 9550 is a unipolar A/D converter, bipolar operation can only be obtained by level shifting the input signal. The FINE TRIM block diagram illustrates this process for either inverting or non-inverting operation using a suitable Operational Amplifier. The value of R should be carefully selected for speed and accuracy. The GAIN and OFFSET adjustments can be used to trim the final input range as previously described.

SUMMARY

The SP 9550 has been designed to simplify high speed conversion and operate at reasonable power levels. The subranging technique and correction logic have been optimized to provide the accuracy. With this in mind, the SP 9550 is a realistic solution to most high speed data conversion problems.

ORDERING INFORMATION

MODEL	OPERATING TEMPERATURE RANGE	SCREENING
SP 9550C	0 to +70°C	—
SP 9550B	-55°C to +125°C	MIL-STD-883C

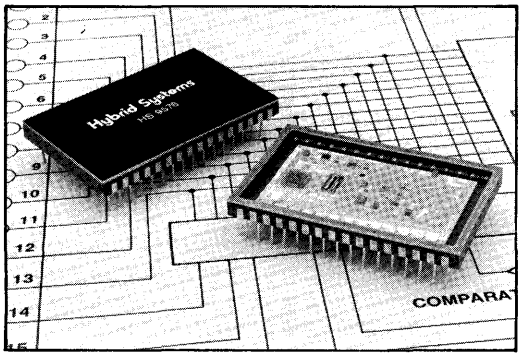
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9576

HIGH SPEED, LOW COST 16-BIT A/D

FEATURES

- Complete 16-bit ADC with internal reference and clock
- Linearity error ±0.003% max
- Fast conversion time: 15μSec max
- Pin for pin compatible with BB ADC 76 and AD 376

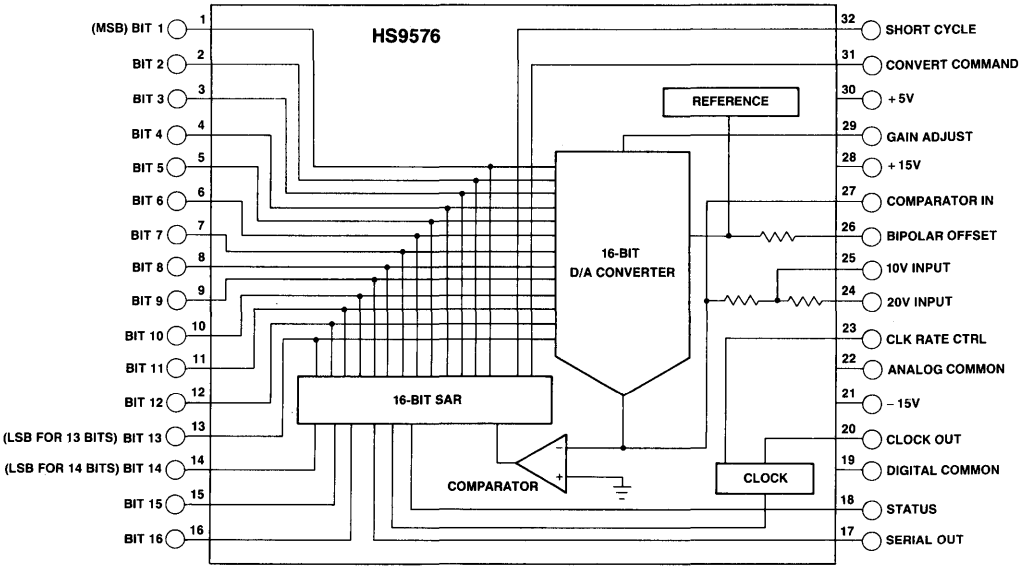


DESCRIPTION

The HS9576 is a low cost, 16-bit successive approximation A/D converter. The converter is complete with internal reference, short cycling capabilities and thin-film scaling resistors which allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V and 0 to +20V. Integral non-linearity is specified at ±0.003% of FSR maximum while no missing codes to 14 bits is guaranteed over the full operating temperature range. Conversion time is 15μsec maximum for 14 bits with the option for faster conversion times to resolutions less than 14 bits. Power consumption is specified at 1W typical.

The HS9576 is a versatile building block for high-accuracy, high-speed systems. When used with the HS9716 sample (track)/hold, a high-speed acquisition system is formed which can digitize signals at a rate of 50,000 conversions per second. The HS9576 is available for operation over the commercial (0°C to +70°C) temperature range or −55°C to +125°C with full MIL-STD-883C screening.

FUNCTIONAL DIAGRAM



9

SPECIFICATIONS

(Typical @ +25°C and nominal power supplies unless otherwise specified)

MODEL	HS 9576J	HS 9576K	HS 9576S/B	HS 9576T/B
RESOLUTION	16 bits	*	*	*
ANALOG INPUTS				
Voltage Range				
Bipolar	±2.5, ±5, ±10V	*	*	*
Unipolar	0 to +5, +10, +20V	*	*	*
Impedance	2.5KΩ on 5V ranges	*	*	*
	5KΩ on 10V ranges	*	*	*
	10KΩ on 20V ranges	*	*	*
DIGITAL INPUTS[1]				
Convert Command	Positive pulse 50 nsec wide (min) trailing edge initiates conversion			
Logic Loading	1 LSTTL load	*	*	*
DIGITAL OUTPUTS[1]				
(All Codes Complementary)				
Output Codes[2]				
Unipolar	CSB	*	*	*
Bipolar	COB, CTC[3]	*		
Output Drive	8 LSTTL loads	*	*	*
Status	Logic "1" during conversion			
Status Output Drive	8 LSTTL loads max	*	*	*
Internal Clock[4]				
Clock Output Drive	4 LSTTL loads max	*	*	*
Frequency	933 kHz	*	*	*
TRANSFER CHARACTERISTICS				
Integral Linearity Error[5]	±0.006% of FSR max	±0.003% of FSR max	±0.006% of FSR max	±0.003% of FSR max
Differential Linearity Error	±0.003% of FSR typ	*	*	*
Gain Error[6]	±0.05% typ; ±0.2% max	*	*	*
Offset Error[6]				
Unipolar	±0.05% of FSR typ; ±0.1% of FSR max	*	*	*
Bipolar	±0.05% of FSR typ; ±0.2% of FSR max	*	*	*
3σNoise at Transitions (pk-pk)	0.001% of FSR typ; 0.003% of FSR max	*	*	*
CONVERSION TIME[4]				
12-Bits	13 μsec max	*	*	*
14-Bits	15 μsec max	*	*	*
16-Bits	17 μsec max	*	*	*
POWER REQUIREMENTS				
Power Consumption	1000 mW typ; 1100 mW max	*	*	*
Rated Voltage, Analog	±15V (±0.5V max)	*	*	*
Rated Voltage, Digital	+5V (±0.25V max)	*	*	*
Supply Drain				
+15Vdc	+23 mA max	*	*	*
−15Vdc	−38 mA max	*	*	*
+5Vdc	+37 mA max	*	*	*
Power Supply Sensitivity	0.001% of FSR/%ΔV_S (all supplies)	*	*	*
WARM-UP TIME	3 minutes	*	*	*
DRIFT				
Gain	±15 ppm/°C max	*	*	*
Offset				
Unipolar	±4 ppm of FSR/°C max	±2 ppm of FSR/°C max	±4 ppm of FSR/°C max	±2 ppm of FSR/°C
Bipolar	±10 ppm of FSR/°C max	*	*	*
Linearity	±3 ppm of FSR/°C max	±2 ppm of FSR/°C max	±3 ppm of FSR/°C max	±2 ppm of FSR/°C
Guaranteed No Missing Codes[7]				
Temperature Range	13 Bits (0°C to +70°C)	14 Bits (0°C to +70°C)	13 Bits (−55°C to +125°C)	14 Bits (−55°C to +125°C)
TEMPERATURE RANGE				
Operating Temperature Range	0°C to +70°C	*	−55°C to +125°C	*
Storage Temperature Range	−55°C to +85°C	*	−65°C to +150°C	*

NOTES:

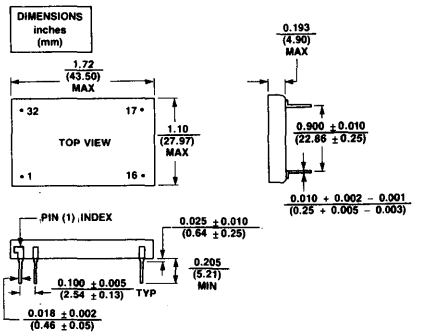
1. Logic "0" = 0.8V max, Logic "1" = 2.0V min for inputs. For digital outputs Logic "0" = +0.4V max, Logic "1" = 2.4V min. 2. CSB — Complementary Straight Binary. COB — Complementary Offset Binary. CTC — Complementary Two's Complement. 3. TCB coding obtained by inverting MSB (Pin 1). Valid for parallel output data only. 4. With CLK RATE CTRL (Pin 23) left open. 5. End Point Definition. 6. Adjustable to zero. 7. A missing code is defined as less than 0.2 LSB wide.

*Specifications same as HS 9576J.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	32	SHORT CYCLE
2	BIT 2	31	CONVERT COMMAND
3	BIT 3	30	+5V
4	BIT 4	29	GAIN ADJUST
5	BIT 5	28	+15V
6	BIT 6	27	COMPARATOR IN
7	BIT 7	26	BIPOLAR OFFSET
8	BIT 8	25	10V INPUT
9	BIT 9	24	20V INPUT
10	BIT 10	23	CLOCK RATE CONTROL
11	BIT 11	22	ANALOG GROUND
12	BIT 12	21	−15V
13	BIT 13 (LSB FOR 13 BITS)	20	CLOCK OUT
14	BIT 14 (LSB FOR 14 BITS)	19	DIGITAL GROUND
15	BIT 15	18	STATUS
16	BIT 16	17	SERIAL OUT

PACKAGE OUTLINE



Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0 to +10V	0 to +5V	0 to +20V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	FSR 2^n	20V 2^n	10V 2^n	5V 2^n	10V 2^n	5V 2^n	20V 2^n
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV	4.88mV
	n = 13	2.44mV	1.22mV	610μV	1.22mV	610μV	2.44mV
	n = 14	1.22mV	610μV	305μV	610μV	305μV	1.22mV
	n = 15	610μV	305μV	152μV	305μV	152μV	610μV
Transition Values MSB LSB							
000...000[4]	+ Full Scale	+ 10V – 3/2LSB	+ 5V – 3/2LSB	+ 2.5V – 3/2LSB	+ 10V – 3/2LSB	+ 5V – 3/2LSB	+ 20V – 3/2LSB
011...111	Mid Scale	0 – 1/2LSB	0 – 1/2LSB	0 – 1/2LSB	+ 5V – 1/2LSB	+ 2.5V – 1/2LSB	+ 10V – 1/2LSB
111...110	– Full Scale	– 10V + 1/2LSB	– 5V + 1/2LSB	– 2.5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

1. Complementary Offset Binary.
2. Complementary Two's Complement — obtained by inverting the most significant bit. MSB (pin 1).
3. Complementary Straight Binary.
4. Voltages given are the nominal value for transition to the code specified.

Table 1. Input Voltages, Transition Values, LSB Values, and Code Definitions

INSTALLATION

GROUNDING AND LAYOUT PRECAUTIONS

Due to the small bit weight (610 μV for 1 LSB, 14 bit, 10V range) special attention must be paid to the layout of the PC board. To avoid capacitive coupling from digital lines to the hybrid substrate, a ground-plane should be placed directly under the converter package on the component side. This ground plane can be directly connected to pin 22 of the HS 9576. All digital lines should run on the soldering side of the PC board.

In general, analog and digital lines should be separated as far as possible and should not run in parallel. If analog and digital lines must cross, they should be at right angles to minimize coupling capacitance. The ground connection to the converter should be made using a wide, low resistive run to minimize voltage drop. Analog and digital ground lines must be connected at only one point, preferably directly at the converter package. For the HS 9576, pin 19 (digital ground) and pin 22 (analog ground) should be tied together as close as possible to the converter.

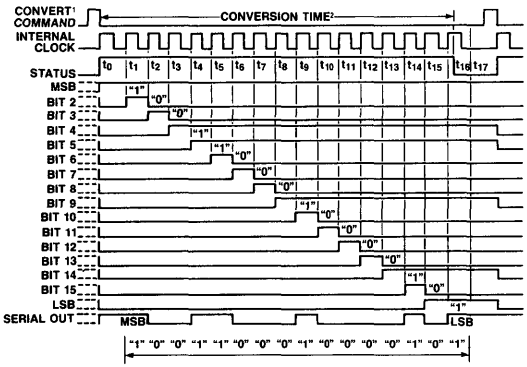
POWER SUPPLY DECOUPLING

Internal 0.01 μF power supply bypass capacitors are included in the HS 9576 to maintain device stability. If the supply voltages contain excessive high frequency noise, additional external high frequency capacitors may be necessary to maintain low noise performance.

OPERATING INSTRUCTIONS

TIMING

The timing diagram is shown in Figure 1. A conversion is initiated by the "trailing edge" of the CONVERT COMMAND. Simultaneous to a CONVERT COMMAND signal, the STATUS flag goes high indicating a conversion is in progress and removing the inhibit applied to the gated clock. The conversion is accomplished by successively comparing the analog input to the feedback DAC output, one bit at a time (MSB first, LSB last). After the LSB decision is made, there is a 30 nsec delay period before the STATUS flag goes low indicating that the conversion is complete and that the output data is valid. Incorporation of this 30 nsec delay guarantees that the digital data is valid at the logic "1" to "0" transition of the STATUS flag, allowing parallel data transfer to be initiated by the trailing edge of the STATUS signal. Resetting the STATUS flag to logic "0" restores the gated clock inhibit signal forcing the clock output to the logic "0" state. The clock remains low until the next conversion is initiated.



NOTES:
1. THE CONVERT COMMAND PULSE WIDTH IS 50ns MIN. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND. IF A NEW CONVERT COMMAND HAPPENS DURING CONVERSION, ALL THE LOGIC OF THE A/D IS RESET AND A NEW CONVERSION BEGINS.
2. 15μs FOR 14 BITS.

*Figure 1. Timing Diagram (Output Code 1001100010000101)**

*Note that all codes are complementary coded. Thus, the output code in Figure 1 represents an analog input whose positive true digital equivalent is 0110011101111010.

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OPTIONAL OFFSET ADJUST

The unipolar offset or bipolar zero error may be trimmed to zero (optional) using an external trim potentiometer connected to the HS 9576 as shown in Figures 2 or 3.

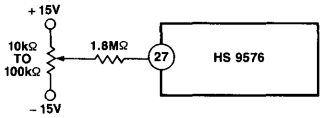


Figure 2. Unipolar Offset or Bipolar Zero Adjustment Circuit (± 0.4% FSR)

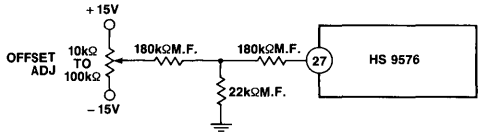


Figure 3. Low Tempco Adjustment Circuit

The adjustment circuit shown in Figure 2 consists of a 100 ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 1.8MΩ resistor to pin 27. In this case a carbon composition resistor is adequate: if we assume that its tempco is - 1200 ppm/°C and that the adjustment range required is no more than 16 LSB14 (0.1% of FS), it contributes only 1.17 ppm/°C of tempco (0.001 × 1200). The low tempco adjustment circuit in Figure 3 contributes negligible tempco if metal film resistors (tempco <100 ppm/°C) are used.

With both circuits the fixed resistor connected to pin 27 should be located close to the converter to keep the pin connection runs short. Offset or zero should be adjusted after warm-up and before gain (see below) to prevent interaction of the two adjustments. Offset or zero is adjusted with the analog input near zero volts. Refer to Table 1 for the appropriate values.

OPTIONAL GAIN ADJUST

The gain error may be trimmed to zero (optional) using an external offset trim potentiometer connected to the HS 9576 as shown in Figure 4.

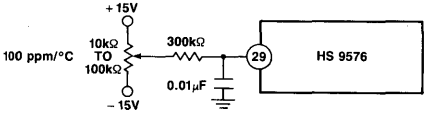


Figure 4. Gain Adjustment Circuit (± 0.2% FSR)

The gain adjustment circuit shown in Figure 4 consists of a 100 ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 300 KΩ resistor to pin 29. Gain should be adjusted after warm-up and after unipolar offset or bipolar zero (see above) to prevent interaction of the two adjustments. Gain is adjusted with the analog input near the most positive end of the analog range. Refer to Table 1 for the appropriate values.

OPTIONAL CONVERSION TIME ADJUST

Short Cycle: A SHORT CYCLE input, pin 32, permits the timing cycle shown in Figure 1 to be terminated after any number of desired bits has been converted. For instance, when 14-bit resolution is desired, pin 32 is connected to bit 15 (output pin 15). The conversion cycle will then terminate and the STATUS flag reset after the bit 14 decision has been made. SHORT CYCLE connections and associated conversion times are summarized in Table 2 below for a 933 kHz clock.

Resolution Bits	(%FSR)	Max Conversion Time (μs)	Connect SHORT CYCLE Pin 32* to Pin:
16	0.0015	17.1	N/C (open)
15	0.003	16.1	16
14	0.006	15.0	15
13	0.012	13.9	14
12	0.024	12.9	13
10	0.100	10.7	11

*Pin 32 cannot be connected to +5V.

Table 2. Short Cycle Connections

Clock Rate Adjust: The HS 9576 may be operated at faster or slower conversion times by connecting the CLOCK RATE CONTROL, pin 23, to an external multiturn trim potentiometer with a TCR of ± 100 ppm/°C or less as shown in Figure 5. The conversion time is trimmed to 17μsec (16-bits) at the factory with CLK RATE CTRL open. The typical conversion time versus the clock rate control voltage is shown in Figure 6. The nonlinearity errors will vary with speed as shown in Figure 7.

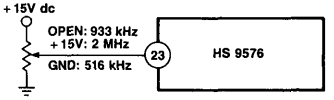


Figure 5. Optional Clock Rate Control Circuit

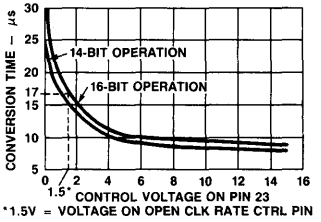


Figure 6. Conversion Time Vs. Clock Rate Control Voltage

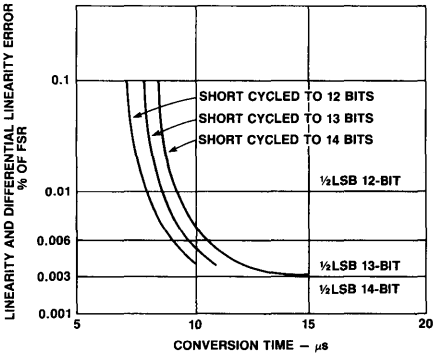


Figure 7. HS 9576 Nonlinearity Vs. Conversion Time

EXTERNAL CLOCK

An external clock may be connected to the CONVERT COMMAND input (pin 31); the CONVERT COMMAND of Figure 1 is not used in this case. The external clock must consist of negative going pulses 100 to 200 nsec wide and must be at a lower frequency than the internal clock. The result is that each falling edge of the external clock turns on the internal clock for a single cycle, completing a conversion in 16 clock cycles.

The converter begins to convert when the external clock is started and will provide a continuous string of conversions with each conversion starting on the first falling edge of the external clock after the STATUS output has gone low, signaling the end of the previous conversion. When continously converting in this manner, the STATUS output goes low for one external clock period following the completion of each conversion. Figure 8 shows continuous conversion using an external clock.

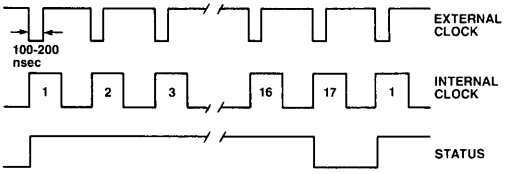


Figure 8. Continuous Conversion Using External Clock

PARALLEL DIGITAL OUTPUT DATA

Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Complementary two's complement may be obtained by inverting MSB (pin 1). Table 1 shows the LSB, transition values and code definitions for each possible analog input signal range for 12-15 bits of resolution. The output data is CMOS compatible and the drive capability is 8 LSTTL loads. If long digital lines have to be driven, external output buffers are recommended.

SERIAL DIGITAL OUTPUT DATA

Serial data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. It is CMOS compatible and has a drive capability of 8 LSTTL loads. At the first low to high transition of the A/D clock, serial out is set to "1" (See Figure 1). The digital word becomes available (bit by bit MSB first) 30nS maximum after the low to high transitions of the clock (Figure 9).

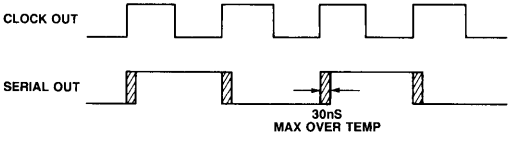


Figure 9. Serial Data to Clock Relationship

INPUT SCALING

The HS 9576 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table 3.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Input Signal To Pin
±10V	COB or CTC*	27	Input Sig.	24
±5V	COB or CTC*	27	Open	25
±2.5V	COB or CTC*	27	Pin 27	25
0 to +5V	CSB	22	Pin 27	25
0 to +10V	CSB	22	Open	25
0 to +20V	CSB	22	Input Sig.	24

*Obtained by inverting MSB (pin 1). Parallel output data only.

Table 3. HS 9576 Input Scaling Connections

CONNECTIONS AND CALIBRATION PROCEDURE

(14-Bit Resolution Example)

Figures 10 and 11 show the different analog and power connections required for unipolar 0 to 10V and bipolar −10V to +10V input range operation.

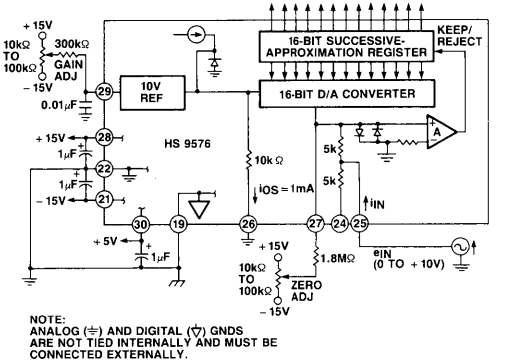


Figure 10. Analog and Power Connections for Unipolar 0 to +10V Input Range

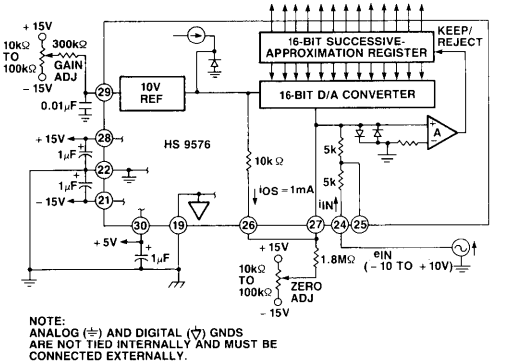


Figure 11. Analog and Power Connections for Bipolar +10V to +10V Input Range

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 10 & 11, are used for device calibration. To prevent interaction of these two adjustments, unipolar offset or bipolar zero is always adjusted first and then gain.

CALIBRATION FOR 0 TO +10V RANGE

Set analog input to +1 LSB_{14} = 0.00061V. Adjust ZERO for digital output = 11111111111110. ZERO is now adjusted. Set analog input to +FS − 2 LSB_{14} = 9.99878V. Adjust GAIN for 00000000000001 digital output code; GAIN is now calibrated. Half scale calibration check: set analog input to +5V; digital output code should be 01111111111111.

CALIBRATION FOR −10V TO +10V RANGE

(Complementary Offset Binary Code)

Set analog input to 0.00000V; adjust ZERO for 01111111111111 digital output code. Set analog input to 9.99756V (+FS − 2 LSB_{14}); adjust GAIN for 00000000000001 digital output code.

OTHER RANGES

Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5 V and −5V to +5V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively, as indicated in Table 1.

Unipolar offset or bipolar zero and full-scale calibrations can be accomplished to a precision of ± ½ LSB using the static adjustment procedure described above.

SAMPLE/HOLD REQUIREMENTS FOR THE HS 9576

Sample/hold amplifiers are normally used in front of A/D converters to hold the input voltage constant during conversion. Digitizing errors will result if the analog input signal varies by more than ½ LSB during conversion. In the case of the HS 9576, a 16-Bit A/D with a conversion time of 15 μsec to 14 bits, this results in a low input frequency which can be accurately digitized as explained below:

For a sine wave input, its maximum rate of change is calculated as 2 πAf where f = frequency and A = amplitude. If one allows a ½ LSB change (0.6mV) during conversion for a ± 10V input swing to the A/D converter, the maximum rate of change limit would be 0.6mV/15 μsec, or 0.04mV/ μsec. Thus, the maximum sine wave input frequency that can be accurately digitized is calculated as:

$$0.04\text{mV}/\ \mu\text{sec} = 2\ \pi\text{Af}$$

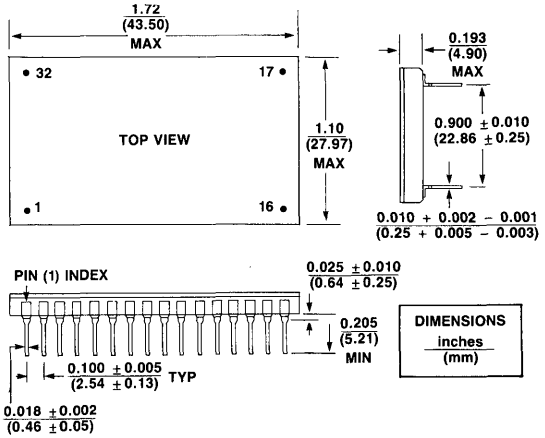
For a ± 10V input sine wave, this frequency limit is 0.63 Hz.

Expressed differently, the full scale bandwidth of the HS 9576 is slew rate limited to 0.63 Hz. By using a S/H, such as the HS 9716/9714 in front of the A/D this bandwidth can be significantly increased. The S/H will "freeze" an input signal that is changing too rapidly for the A/D alone to handle and hold it constant while the A/D performs a conversion. A S/H can accurately "freeze" signals moving as fast as ½ LSB during its aperture uncertainty (100 psec for the HS 9716/9714). Thus, for use with the HS 9576 to 14-Bit accuracy, the maximum rate of change limit would be 0.6mV (½ LSB, 14 bits, ± 10V swing) during 100 psec, or 6V/ μsec, which is the slew rate of the HS 9716/9714. Thus, the maximum full scale input frequency that can be accurately digitized is calculated as:

$$6\text{V}/\ \mu\text{sec} = 2\ \pi\text{Af}$$

For a ± 10V full scale input, this frequency limit is 95 kHz. Expressed differently, the slew rate limited full scale bandwidth of the HS 9576 has now been increased to 95 kHz with the use of the HS 9716/9714 S/H.

Throughput and the Nyquist criteria are other factors which will determine the highest input signal frequency that can be sampled. For the combination of the HS 9576 and the HS 9716/9714, the throughput is related to the sum of the conversion time of the A/D (15 μsec), the acquisition time of the S/H (5 μsec) and the hold mode (switching transient) settling time of the S/H (1 μsec). The total of 21 μsec represents a throughput of 47.6 kHz. Based on the Nyquist criteria of sampling more than twice per cycle, the highest input signal frequency that can be accurately digitized is slightly less than 23.8 kHz.



ORDERING INFORMATION

MODEL	MAX LINEARITY ERROR	TEMPERATURE RANGE	SCREENING
HS 9576J	±0.006% FSR	0°C to +70°C	—
HS 9576K	±0.003% FSR	0°C to +70°C	—
HS 9576S/B	±0.006% FSR	−55°C to +125°C	MIL-STD-883C
HS 9576T/B	±0.003% FSR	−55°C to +125°C	MIL-STD-883C

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP9588

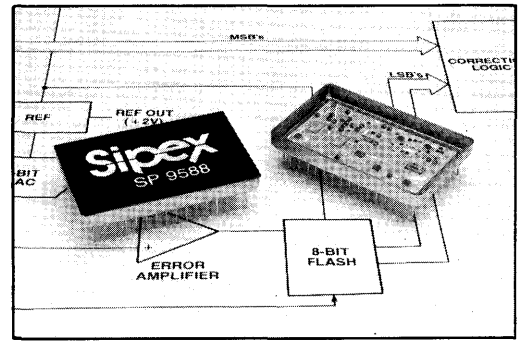
500 kHz, MULTIPASS™ 14-BIT A/D CONVERTER

DESCRIPTION

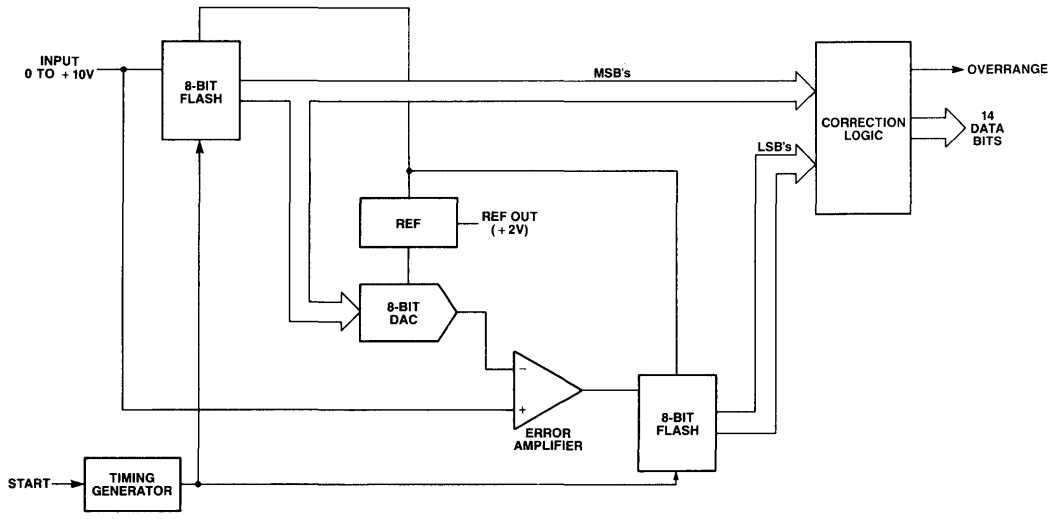
The SP9588 is a 14-bit, 2.0 microsecond, analog-to-digital converter employing the SIPEX state-of-the-art Multipass™ subranging Flash technology. The subranging Multipass process is optimized for high accuracy operation by using two 8-bit Flashes in a feed-forward error correction scheme to yield a final resolution of 14 bits while consuming less than 3 watts.

The SP9588 can be used in either a single or continuous mode. In the single mode, a START command initiates the conversion on its rising edge and completes the conversion on its falling edge. Total conversion can be completed in less than 2.0 microseconds. By repeating the START command every 2.0 microseconds, the SP9588 will operate in a continuous mode at a maximum of 500 kHz.

The SP9588 input range, 0 to +10V, has been optimized for high accuracy applications such as high speed, high accuracy data acquisition systems. The SP9588 is ideal in all applications that require 14-bit performance at relatively high speed with moderately low power consumption.



FUNCTIONAL DIAGRAM



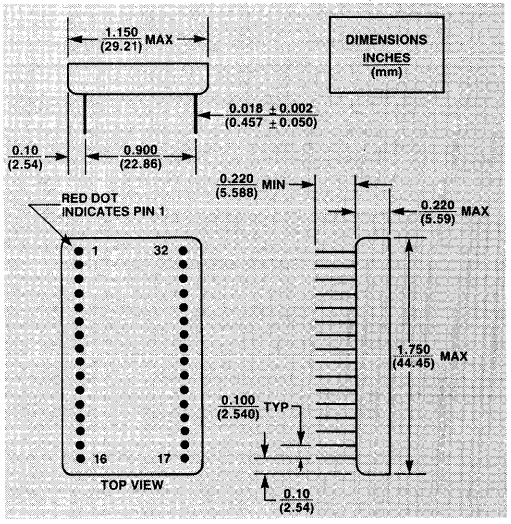
9

SPECIFICATIONS

(Typical @25°C and nominal supply voltages unless otherwise specified.)

MODEL	SP 9588
RESOLUTION	14-Bits
ANALOG INPUTS	
Input Voltage Range	0 to +10V
Input Impedance	5kΩ
DIGITAL INPUTS	
Logic Levels: Logic "1"	2.4V min
Logic "0"	0.4V max
Logic Loading	1 TTL Load
ACCURACY	
Integral Linearity @25°C	±1 LSB max
Differential Linearity @25°C	±½ LSB
No Missing Codes 0 to 70°C	Guaranteed
Offset Error	0.1% of FSR typ, 0.3% max
Gain Error	0.1% of FSR typ, 0.5% max
DYNAMIC PERFORMANCE	
Conversion Time	2.0μ sec
STABILITY	
Integral Linearity Tempco	2.5 ppm/°C
Differential Linearity Tempco	2 ppm/°C
Unipolar Offset Error Drift	1 ppm/°C
Gain Error Drift	25 ppm/°C
DIGITAL OUTPUTS	
Output Coding (Straight Binary)	See Table
Output Drive Capability	3 TTL Loads
REFERENCE	
Voltage	+2.0V nom
External Current	5mA
POWER SUPPLY REQUIREMENTS	
Current @nominal Voltage	
+15V (±10%)	25mA
−15V (±10%)	25mA
+5V Digital (±10%)	300mA
+5V Analog (±1%)	30mA
−5V (±1%)	30mA
Dissipation	2.5W typ, 3.0W max
PACKAGE	
Triple DIP — Metal	32-Pin

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	START (CLOCK)	32	8/14 SELECT
2	BIT 14 (LSB)	31	+5V DIGITAL
3	BIT 13	30	DIGITAL GND*
4	BIT 12	29	+5V ANALOG
5	BIT 11	28	−5V
6	BIT 10	27	ANALOG GND
7	BIT 9	26	ANALOG GND
8	BIT 8	25	−15V
9	BIT 7	24	+15V
10	BIT 6	23	REF OUT
11	BIT 5	22	TEST POINT
12	BIT 4	21	ANALOG GND
13	BIT 3	20	TEST POINT
14	BIT 2	19	ANALOG GND
15	BIT 1 (MSB)	18	TRIM
16	OVERRANGE	17	ANALOG INPUT

*Internally connected to case.

THEORY OF OPERATION

INTERFACE INFORMATION

The SP 9588 is designed primarily for high accuracy applications that require a conversion time as low as 2.0 microseconds. The SP 9588 will also operate at slower conversion times with no degradation. The rate of conversion is set by the START signal that is applied to it. The rising edge of the START signal initiates the conversion process and the falling edge of the START signal completes the process.

The input stage has been designed for fast settling so as to function in a data acquisition environment with S/H amplifiers and multiplexers. As such, the input signal should be driven by a low impedance source sufficient to drive the 5K ohm input impedance at 14-bit accuracy. This requires a careful selection of appropriate S/H amplifiers and fast operational amplifiers.

CONVERSION PROCESS

As shown in the block diagram, the input analog signal is directed to the input of the first 8-BIT FLASH ADC. The FLASH converter also receives a reference voltage (REF) of 2.0 volts. The input signal is compared to this reference in the conversion process by the FLASH converter and the resulting digital 8-bit word, which represents the most significant bits (MSB), is generated for further processing by both the 8-bit DAC and the CORRECTION LOGIC.

The above sequence is refered to as the "first pass" or "input" conversion. The resulting 8-bit word is sent to an 8-bit DAC which is trimmed to better than 14-bit accuracy. The DAC output is then directly subtracted from the input signal to determine the "error" or "second pass" signal to be converted by the Flash.

The "second pass" occurs when the ERROR AMPLIFIER output is directed to the input of the second FLASH converter. The result of this conversion process is a digital word which represents the least significant bits (LSB). This digital output is now ready for further processing by the CORRECTION LOGIC.

The CORRECTION LOGIC accepts the 8 MSB's and the 8 LSB's and combines them by an improved, unique algorithm using digital addition. The result is a 14-bit digital word which accurately represents the analog input. The CORRECTION LOGIC also provides an overrange (O.R.) bit to indicate that the input has exceeded full scale. The output coding is straight binary. Refer to Coding Table.

The entire conversion process is controlled by the TIMING GENERATOR which only requires a START signal as previously described. The falling edge of the START signal indicates that the digital data is ready.

SINGLE CONVERSION MODE

The single conversion mode is shown on the TIMING GENERATOR timing diagram. The timing sequence shown reflects the nominal minimum conversion time required.

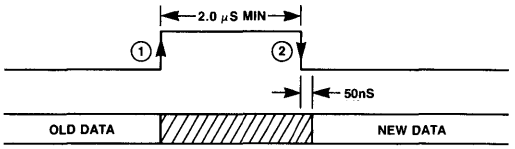
Referring to the timing diagram, the process is as follows:

1. The rising edge of the START signal causes the first FLASH to perform a conversion to determine the MSB's. Old data from the previous conversion is no longer valid.
2. The falling edge of the START signal causes the second FLASH to perform a conversion to determine the LSB's. New data will be valid 50 nanoseconds later.

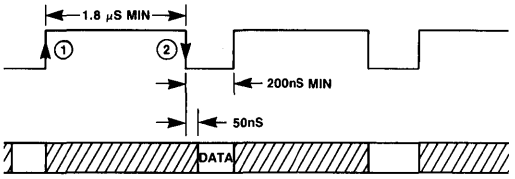
CONTINUOUS CONVERSION MODE

The SP 9588 will be in the continuous conversion mode as long as the START signal is repeated. This mode is used to follow high speed input signals and is capable of a 500 kHz converting rate. However, an external S/H amplifier is required...the time necessary for the S/H amplifier to acquire and settle must be taken into consideration. If the S/H amplifier requires 500 nanoseconds then the throughput rate is 400 kHz.

Referring to the timing diagram, the process is as follows:



SINGLE CONVERSION



CONTINUOUS CONVERSION

SP 9588 Timing Diagram

1. The rising edge of the START signal causes the first FLASH to perform a conversion to determine the MSB's. Old data from the previous conversion is no longer valid.
2. The falling edge of the START signal causes the second FLASH to perform a conversion to determine the LSB's. New data will be valid 50 nanoseconds later.

The process is repeated continuously as shown in the timing diagram. When operating at the maximum rate of 500 kHz, the START signal should be high for only 1.8 microseconds and low for 0.2 microseconds. When using an external S/H amplifier, the START signal should be high for the full 2.0 microseconds and low for the time required for the S/H amplfier to acquire and settle. The resulting conversion rate will be proportional to the total time required for both the S/H amplifier and the SP 9588.

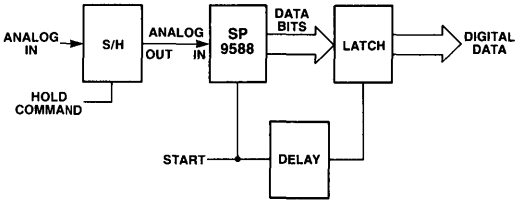
INPUT VOLTAGE	BINARY BITS OR	1	2	3	4	5	6	7	8	9	10	11	12	13	14	HEX CODE
0.00000		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0 0 0 0
0.00061		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0 0 0 1
4.99939		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1 F F F
5.00000		1	0	0	0	0	0	0	0	0	0	0	0	0	0	2 0 0 0
5.00061		1	0	0	0	0	0	0	0	0	0	0	0	0	1	2 0 0 1
9.99939		1	1	1	1	1	1	1	1	1	1	1	1	1	1	3 F F F
10.00000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4 0 0 0
10.00061	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	4 0 0 1
10.11658	1	0	0	0	0	0	0	1	0	1	1	1	1	1	1	4 0 B F
1.17%	Overrange															

SP 9588 Coding Table @10 Volt Full Scale

TYPICAL APPLICATIONS

The application block diagram illustrates a typical system using the SP 9588 with an external S/H amplifier and an external latch for the data bits. Since the data is valid 50 nanoseconds after the falling edge of the START signal, the START signal needs to be delayed by more than 50 nanoseconds if it is to be used as the strobe for the latch.

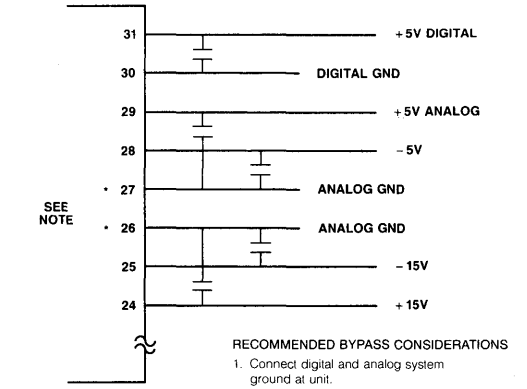
The SP 9588 can be used directly without a S/H amplifier to take a quick snapshot of a slow moving input signal. The maximum input frequency that can be followed without a S/H amplifier is approximately 300 Hz.



Typical Application: SP 9588 With External S/H Amplifier & External Latch

POWER SUPPLY CONNECTIONS

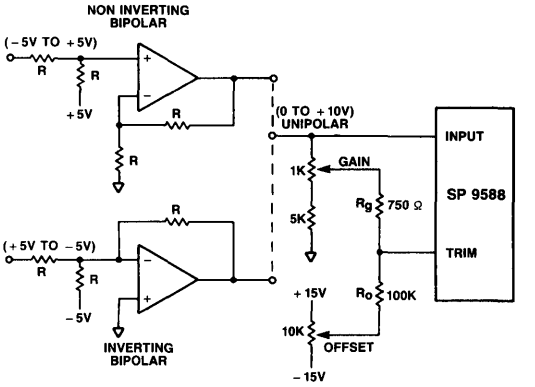
As shown in the Power Supply Connection diagram, 5 pairs of capacitors are recommended for bypassing the power supplies at the SP 9588. Also note that it is recommended to externally connect the analog and digital grounds at the SP 9588. Also, the analog and digital +5V supplies should be separate for optimum performance.



SP 9588 Power Supply Connections

TRIM ADJUSTMENTS

The SP 9588 can be externally trimmed for gain and offset as shown in the block diagram. To change the sensitivity of the gain trim, increase or decrease the value of R_g (750 ohm). To change the sensitivity of the offset trim, increase or decrease the value of R_O (100k ohm). The interaction of the gain and offset trim is minimal; some readjustment may have to be made if one or the other trim is extreme.

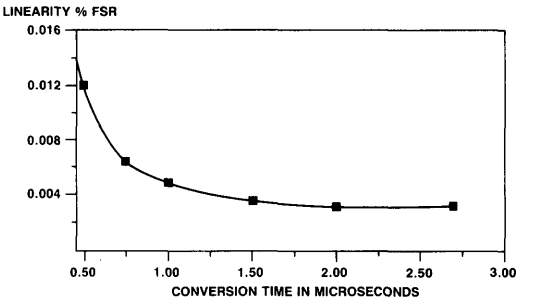


To change sensitivity of GAIN Trim increase/decrease R_g.
To change sensitivity of OFFSET Trim increase/decrease R_O.

SP 9588 Fine Trim Adjustments

BIPOLAR OPERATION

Since the SP 9588 is a unipolar A/D converter, bipolar operation can only be obtained by level shifting the input signal. The FINE TRIM block diagram illustrates this process for either inverting or non-inverting operation using a suitable Operational Amplifier. The value of R should be carefully selected for speed and accuracy. The GAIN and OFFSET adjustments can be used to trim the final input range as previously described.



SP 9588 Linearity Vs. Conversion Time

SUMMARY

The SP 9588 has been designed to simplify high speed, high accuracy conversion and operate at reasonable power levels. The subranging technique and correction logic have been optimized to provide the high accuracy. With this in mind, the SP 9588 is then the solution to most high speed, high accuracy data conversion problems.

ORDERING INFORMATION

MODEL	OPERATING TEMPERATURE RANGE	SCREENING
SP 9588C	0 to +70°C	—
SP 9588B	-55°C to +125°C	MIL-STD-883C

SAMPLING A/D CONVERTERS

MODEL	RESOLUTION	THROUGHPUT	µP COMPATIBLE	POWER CONSUMPTION (mW)	PACKAGE	PAGE
HS9474	12 bits	37 kHz	Yes	300	28-Pin DD	493
SP9560	12 bits	10 MHz	Yes	3500	46-Pin	513
SP9478	14 bits	500 kHz	Yes	3000	32-Pin TD	509
HS9476	16 bits	50 kHz	Yes	1520	32-Pin TD	501

Shaded area indicates new product since publication of 1988 catalog

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9474

37kHz SAMPLING, 12-BIT A/D CONVERTER

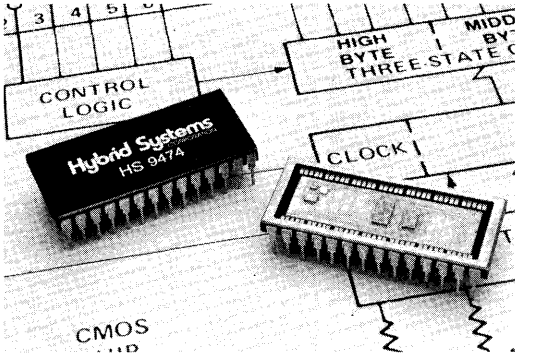
FEATURES

- Complete 12-bit A/D converter with reference, clock and three state outputs
- Internal sample-and-hold amplifier
- Internal hold capacitor
- Pin compatible with industry standard 574
- 37kHz throughput
- Low power: 390mW

DESCRIPTION

The HS9474 is a complete HS574 A/D converter with internal sample-hold amplifier. Requiring no external sample-hold connections, the HS9474 is pin for pin compatible with the industry standard 574. It is specifically designed for systems applications where the sample-hold is an integral part of the conversion process. Incorporation of the sample-hold into the same circuit with the A/D converter reduces real estate, parts count, design time, and component interaction errors.

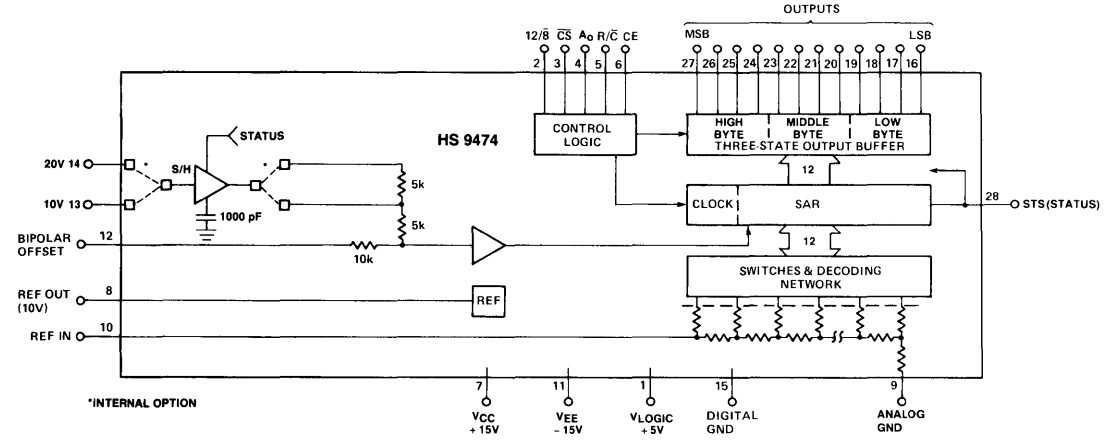
The sample-hold has a 7μsec acquisition time to 0.01% for a full 10V input change. A 1000 pF hold



capacitor is included in the circuit. Input voltage ranges available are ±5V or 0 to +10V for the -1 model and ±10V for the -2 model.

The HS9474 is offered in a hermetically-sealed ceramic package for use over a wide temperature range and for MIL-STD-883 Rev. C requirements.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V, V_{EE} = −15V, V_{LOGIC} = +5V unless otherwise specified)

MODEL	HS 9474J	HS 9474K	HS 9474S	HS 9474T
RESOLUTION (max)	12 Bits	*	*	*
TYPE	Successive Approximation	*	*	*
ANALOG INPUTS				
Input Ranges				
−1***	±5V, 0 to +10V	*	*	*
−2	±10V	*	*	*
Input Impedance	$10^{10}\Omega$			
DIGITAL INPUTS				
Logic Inputs				
CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$				
Logic 1	+2.4V min, +5.5V max	*	*	*
Logic 0	−0.5V min, +0.8V max	*	*	*
Current	±5μA max	*	*	*
Capacitance	5pF	*	*	*
Minimum Start Pulse				
CE-Positive	50nsec	*	*	*
$\overline{CS}$-Negative	50nsec	*	*	*
R/$\overline{C}$-Negative	50nsec	*	*	*
DIGITAL OUTPUTS				
Logic Outputs				
DB_{11}-DB_0, STS				
Logic 0	+0.4V max, I_{SINK} ≤1.6mA	*	*	*
Logic 1	+2.4V min, I_{SOURCE} ≤500μA	*	*	*
Leakage (High Z State)	±5μA max (Data Bits Only)	*	*	*
Capacitance	5pF	*	*	*
Parallel Data				
Output Codes				
Unipolar	Positive True Binary	*	*	*
Bipolar	Positive True Offset Binary	*	*	*
REFERENCE				
Internal	10.00 ±0.1 Volts max	*	*	*
Output Current	1.5mA****	*	*	*
CONVERSION TIME	18μsec (25μsec max)	*	*	*
ACQUISITION TIME	7μsec (10μsec max)	*	*	*
ACCURACY				
Linearity (% of F.S.R. max)	±0.025	±0.012	±0.025	±0.012
Monotonicity (Bits)[2]				
No Missing Codes	11	12	11	12
Offset[3]				
Unipolar (% of F.S.R. max)	±0.05	*	*	*
Bipolar (% of F.S.R. max)	±0.25	±0.1	±0.25	±0.1
Gain[3, 4] (% fo F.S.R. max)	±0.3	*	*	*
STABILITY				
Linearity (ppm/°C max)				
0°C to +70°C	±0.5	*	±0.5	**
−55°C to +125°C			±0.5	**
Unipolar Offset (ppm/°C max)				
0°C to +70°C	±10	±5		
−55°C to +125°C			±10	±5
Bipolar Offset (ppm/°C max)				
0°C to +70°C	±15	±10		
−55°C to +125°C			±15	±10
Gain (Scale Factor)(ppm/°C max)				
0°C to +70°C	±50	±27		
−55°C to +125°C			±50	±25
POWER SUPPLY				
V_{LOGIC}	+4.5 to +5.5 Volts @ 3mA max	*	*	*
V_{CC}	+13.5 to +16.5 Volts @ 12.5mA typ, 17mA max	*	*	*
V_{EE}	−13.5 to −16.5 Volts @ 8mA max	*	*	*
Power Dissipation	390mW max	*	*	*
Rejection[5]				
V_{LOGIC}	±0.002%/%	*	*	*
V_{CC}, V_{EE}	±0.005%/%	*	*	*
TEMPERATURE RANGE				
Operating	0°C to +70°C	*	−55°C to +125°C	
Storage	−25°C to +85°C	*	−65°C to +150°C	

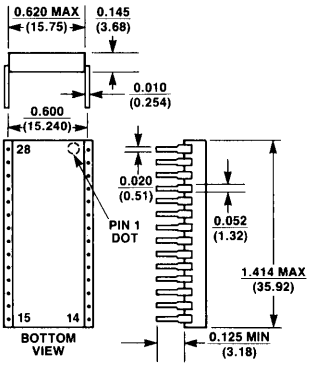
NOTES:

1. Conversion time shown for a complete 12 bit conversion. 2. T_{min} to T_{max}. 3. Externally adjustable to zero. See application information. 4. Connect 50Ω between REF OUT and REF IN initial gain and offset adjustable to zero. 5. Maximum change over rated supply range.

*Specifications same as HS 9474J. **Specifications same as HS 9474S.

***Input range selected at factory. ****Recommend buffer for external use.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	V_{LOGIC}	28	STS
2	12/$\overline{8}$	27	DB_{11}(MSB)
3	$\overline{CS}$	26	DB_{10}
4	A_0	25	DB_9
5	R/$\overline{C}$	24	DB_8
6	CE	23	DB_7
7	V_{CC}	22	DB_6
8	REF OUT	21	DB_5
9	ANA GND(AC)	20	DB_4
10	REF IN	19	DB_3
11	V_{EE}	18	DB_2
12	BIP OFF	17	DB_1
13*	$10V_{IN}$ (−1)	16	DB_0(LSB)
14*	$20V_{IN}$ (−2)	15	DIGITAL GND

*Input not selected at factory will not be connected.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, V_{IN}) to Analog Common ..... ±16.5V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Power Dissipation 1000mW
Lead Temperature, Soldering ..... 300°C, 10sec

CONTROL FUNCTIONS

The HS 9474 contains all control functions necessary to provide for complete microprocessor interface and also 'stand alone' operation including continuous conversions. All control functions are defined in Table 1 and Table 2.

Function	Definition	Function
CE	Chip Enable	1. Typically used as clock synchronization with µP. 2. Must be high (1) for a conversion to start. 3. Must be high (1) to read data on the output. 4. ⌐ transition may be used to initiate conversion.
$\overline{CS}$	Chip Select	1. Typically the address pin when used with µP. 2. Must be low (0) for a conversion to start or read data at the output. 3. ¬ transition may be used to initiate conversion.
R/$\overline{C}$	Read/Convert	1. ¬ initiate conversion 2. ⌐ initiate read
A_0	Address	1. Selects conversion mode. 12 Bits if low (0). 8 Bits if high (1). 2. In read mode A_0 selects the output format. If low (0) then 8 MSB's (high and middle byte) or if high (1) then only low byte and trailing zeros.
12/$\overline{8}$	Output Format	1. Must be hard wired. 2. Normal 12 Bit format if high (1). 3. 8-Bit format as set by A_0 if low (0).

Table 1. Defining the Control Functions

CONTROL INPUTS					HS 9474 OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	¬	X	0	Initiates 12-Bit Conversion
1	0	¬	X	1	Initiates 8-Bit Conversion
⌐	0	0	X	0	Initiates 12-Bit Conversion
⌐	0	0	X	1	Initiates 8-Bit Conversion
1	¬	0	X	0	Initiates 12-Bit Conversion
1	¬	0	X	1	Initiates 8-Bit Conversion
1	0	⌐	Pin 1	X	Enables 12-Bit Parallel Output
1	0	⌐	Pin 15	0	Enables 8 MSB's
1	0	⌐	Pin 15	1	Enables 4 LSB's and 4 Trailing Zeros

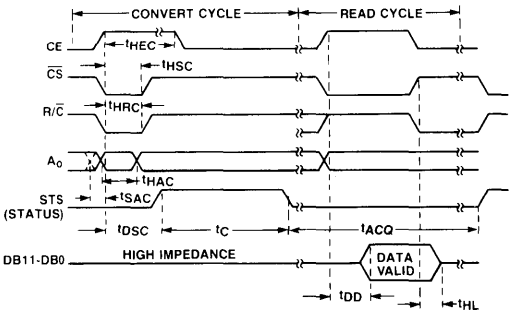
NOTES: 1. 1 indicates logic HIGH.
2. 0 indicates logic LOW.
3. X indicates don't care.
4. ⌐ indicates operation commences on low to high transition.
5. MSB → XXXX (High Byte) XXXX (Middle Byte) XXXX (Low Byte) ← LSB
6. Not a common use of this function.
7. When using the HS 9474 in the 8-bit bus mode with 12-bit resolution, the high byte must be externally hard wired to the low byte.

10

TIMING

The timing diagrams are shown in Fig. 1. Note that to start a conversion CS, CE, and R/C must have an overlap time of 50ns minimum. CS and R/C may be advanced or delayed if needed (by the application) but no specifications are given for this — only the coincidence of 50ns must be met. Typically R/C is used to initiate a conversion — however other lines may be used. See truth table (Table 2).

In the READ mode **note the access time t_{DD} is 75ns typ, 150ns max. This means that an entire conversion can be completed and read in 20 μs typ, 25 μs max** including setup, conversion time and access time.



CONVERT CYCLE

SYMBOL	PARAMETER	
t_{ACQ}	Acquisition Time	7 μs typ, 10 min
t_{HEC}	CE Pulse Width	50ns min
t_{HSC}	CS LOW during CE high	50ns min
t_{HRC}	R/C LOW during CE high	50ns min
t_{HAC}	A_0 valid during CE high	50ns min
t_{SAC}	Maximum A_0 delay from CE. Set up as shown (negative time wrt* CE) not needed	0ns max
t_{DSC}	STS delay from CE	200ns max
t_C	Conversion time	
	8 Bit cycle	13 μs typ, 19 μs max
	12 Bit cycle	20 μs typ, 25 μs max

CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, CS, R/C, as shown in Table 1. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if A_0 changes state after a conversion begins, an additional Start Convert command will latch the new state of A_0 and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

READ CYCLE

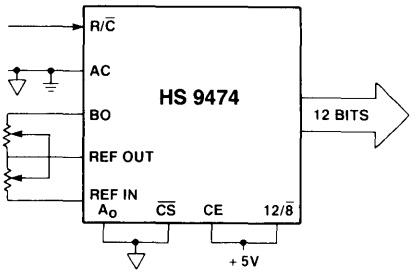
t_{DD}	Access time from CE high	75ns typ, 150ns max
t_{HL}	Output Float Delay	150ns max

*wrt = With Respect To.

Figure 1. HS 9474 Interface Timing

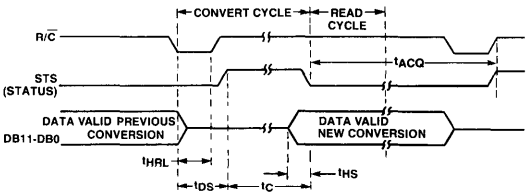
STAND-ALONE OPERATION

The HS 9474 can be used in a 'stand-alone' mode in systems having dedicated input ports. Connections and timing for this mode are shown in Fig. 2.



NOTE: HS 9474 wired for 12-Bit conversion

R/C NEGATIVE PULSE



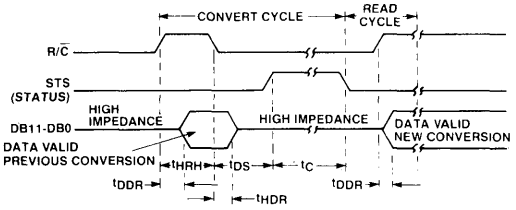
CONVERT CYCLE

SYMBOL	PARAMETER	
t_{HRL}	Low R/C Pulse Width	50ns min
t_{DS}	STS Delay from R/C	200ns max
t_C	Conversion Time	25 μs max
t_{HS}	Data valid after STS low	70ns max
t_{ACQ}	Acquisition Time	7 μs typ
		10μs max

READ CYCLE

1. Data always in 'read' mode except during a conversion in which data lines revert to high impedance.
2. Output always valid after conversion is complete

R/C POSITIVE PULSE



CONVERT CYCLE

SYMBOL	PARAMETER	
t_{HDR}	Valid Data (Previous Conversion) after R/C low	25ns min
t_{HRH}	High R/C Pulse Width	150ns min
t_{DS}	STS Delay from R/C	200ns max
t_{DDR}	Data Access Time	150ns max
t_C	Conversion Time	25 μs max

READ CYCLE

1. Converter output remains in high impedance state after conversion (STS goes low) until R/C goes high (to 'read' data).

Figure 2. HS 9474 Stand-Alone Operation
Top: Using negative R/C pulse
Bottom: Using positive R/C pulse

CONTINUOUS CONVERSION

Requirements for self triggered-continuous conversions are popular applications for an analog to digital converter, see Fig. 3.

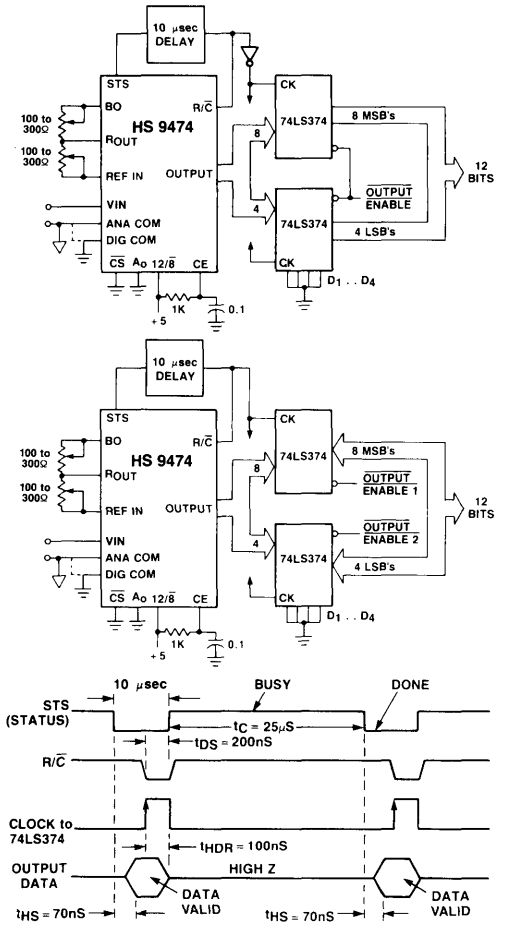


Figure 3. Continuous Conversion
Top: DATA BUS 12 Bits or greater
Bottom: DATA BUS 8 Bits

$\overline{CS}$ and A_0 are tied low (0) while 12/$\overline{8}$ is tied high (1) to select the converter and enable a 12-Bit conversion. Note A_0 is 'don't care' in the truth table.

CE is connected to a 1KΩ and 0.1 μF integrator as shown, this ensures an initial conversion on power up. CE will see a rising edge which will initiate a conversion ($\overline{CS}$ = 0, R/$\overline{C}$ = 0). The RC network will then integrate the initial 1 at the output of the first inverter causing a delay in the R/$\overline{C}$ command. After the first conversion, continuous conversions are caused by delaying the STATUS (STS) into R/$\overline{C}$. After the conversion is complete the output data lines come out of tri-state approximately 70ns after STS goes low (DONE). Data will remain valid (from previous conversion) 100ns after the new R/$\overline{C}$ command which allows for the positive edge triggered data to be loaded into the external buffer (75LS374 or equivalent).

Using the R-C network as shown, 1.5 μs is allowed between conversions. Shorter times can be used but a longer time will cause long rise and fall of the R/$\overline{C}$ line and the clock input to the buffer. The setup time for the latch shown is 20ns and the hold time is 0ns.

The user may access the octal latches asynchronously by means of the $\overline{OUTPUT\ ENABLE}$ (CONTROL OUTPUT) line. The data will always be valid,for a 12-bit conversion. Using this method, data will always be current and the STATUS bit need not be tested for valid data.

USING THE A_0 LINE

The state of the A_0 line at the start of a conversion places the HS 9474 in either a full 12-bit conversion or in an 8-bit 'short cycle' mode. During a READ at the end of a conversion the A_0 line is used to the format of the data as follows:

1. Prior to Conversion

	MODE
$A_0 = 1$	Short cycle 8-bit conversion
$A_0 = 0$	Full 12-bit conversion

2. After Conversion (READ)

$A_0 = 1$	Data = Low Byte (LSB) followed by zeros
$A_0 = 0$	Data = High Byte (MSB's) followed by middle and low byte.

In a μP application the A_0 line can be considered a pair of $\overline{WR}$ locations as follows:

1. Prior to Conversion (WRITE)

	MODE
$\overline{WR} = 0$ in low address ($A_0 = 0$)	Full 12-bit conversion
$\overline{WR} = 0$ in high address ($A_0 = 1$)	Short cycle 8-bit conversion

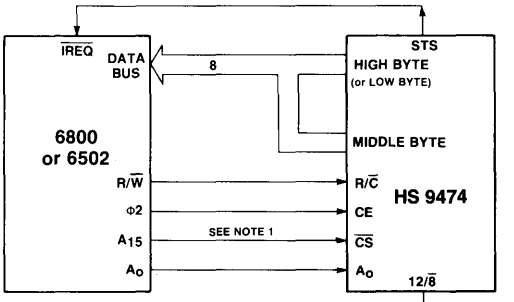
2. After Conversion (READ)

$\overline{WR} = 1$ in either address ($A_0 = X$)	Full 12-bit word with 12/$\overline{8}$ = 1
$\overline{WR} = 1$ in high address ($A_0 = 1$)	LSB's & zeros when 12/$\overline{8}$ = 0
$\overline{WR} = 1$ in low address ($A_0 = 0$)	8 MSB's only when 12/$\overline{8}$ = 0

INTERFACING THE HS 9474 WITH 8-BIT MICROPROCESSORS

The HS 9474 which has 12-bit data can be used directly with popular 8-bit microprocessors. The data however, must be multiplexed by setting the output mode select 12/$\overline{8}$ pin to GND.

In the first case, a 6800 (or 6502) is used. See Figure 4.



Note 1. Decoding may be needed for a large system.

Figure 4. Interfacing the HS 9474 and a 6800 μP

The STATUS (STS) is tied directly to $\overline{IREQ}$ which is the interrupt line. When STS goes to 0 (at the end of a conversion) the 6800 may either service the interrupt or be timed for 25 μs (since this $\overline{IREQ}$ is software maskable) the time required for a conversion.

Figure 5 shows the 8080A μP as interfaced with the HS 9474. In this case, a 8228 controller is shown with gates to generate needed signals.

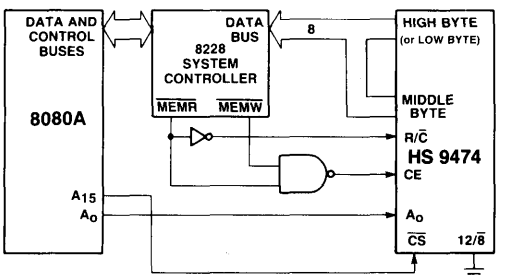


Figure 5. Interfacing the HS 9474 and 8080A μP

Figure 6 shows the HS 9474 connected with a 8048 μP. A single NAND gate is used to generate CE.

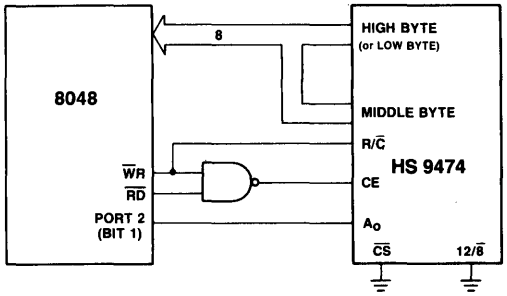


Figure 6. Interfacing the HS 9474 and a 8048 μP

A summary of μP types and connections is in Table 3.

MICRO-PROCESSOR	HS 9474 CONTROL INPUTS			
	CE	R/C	CS	A_0
8080 MEMORY MAPPED I/O PROGRAMMED I/O	(MEMW • MEMR) (I/OW • I/OR)	(MEMR) (I/OR)	DECODED ADDRESS	A_0
6800	ϕ_2	R/W	DECODED ADDRESS	A_0
6502	ϕ_2	R/W	DECODED ADDRESS	A_0
Z80 MEMORY MAPPED I/O	(RD • WR)	(RD)	DECODED ADDRESS WITH MREQ	A_0
PROGRAMMED I/O	(RD • WR)	(RD)	DECODED ADDRESS WITH IOR	A_0
8048	(RD • WR)	(RD)	PORT 2_{0-3}*	PORT 2_{0-3}*

*Port 2, Lines 0-3 can be used as a 4-Bit address bus. System address decoding requirements vary from no hardware to a fully latched 12-Bit address, depending on system complexity.

Table 3. Summary of HS 9474 Control Inputs with Various Microprocessors

ENABLING DATA IN 8-BIT MODE

To operate the HS 9474 in a 12-bit conversion mode with an 8-bit data bus, use the basic configuration shown in Figure 7. The A_0 control can be connected to the least significant bit of the data bus in order to store the output data into two consecutive memory locations. When A_0 is pulled low, only the 8 MSB's are enabled. When A_0 is high, the 4 MSB's are disabled, bits 4 through 7 are forced to a zero and the 4 LSB's are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1. A_0 may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between two data bytes. This assures that the outputs which are strapped together in Figure 7 will never be enabled at the same time.

ZERO AND GAIN CONNECTIONS

The HS 9474 is normally used with external zero and gain calibration potentiometers. However, if maximum accuracy is not required, they may be omitted. If no trims are used, the gain calibration will be within approximately $\pm$2LSB zero offset error, and $\pm$12LSB maximum full scale error. See Figure 8 for connection with no trims. If gain and zero adjustment potentiometers are used, they should be connected as shown in Figure 9. The zero control has a range of about $\pm$20LSB, and the gain control has a range of about $\pm$13LSB.

Proper gain and zero calibration requires great care and the use of extremely sensitive and accurate instruments. The voltage source used as a signal input must be very stable. It also should be capable of being set to within 1/10LSB at both ends of its range.

The HS 9474's zero and gain adjustments are independent of each other if the zero (or offset) adjustment is made first.

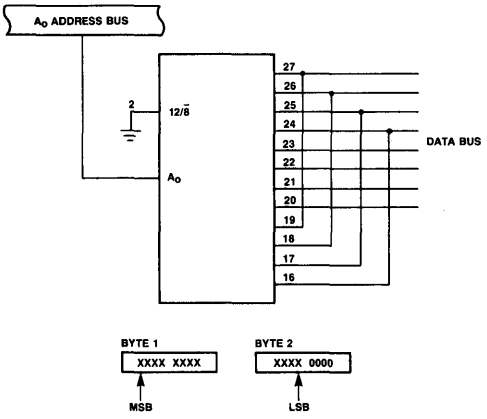
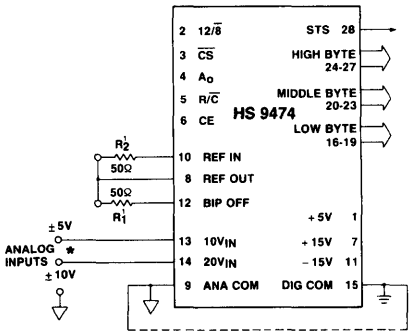
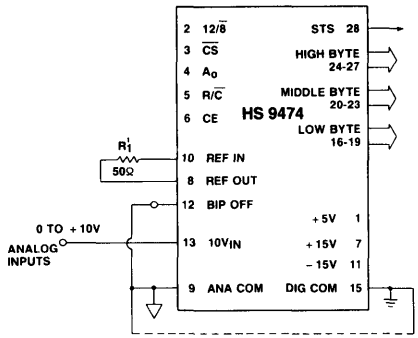


Figure 7. Enabling Data in 8-Bit Mode



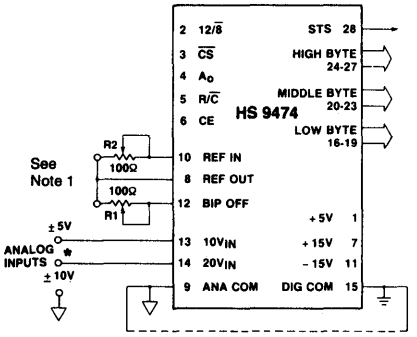
1. 50Ω ± 1% metal film

Figure 8a. No Trim Biplor Input Connections



1. 50Ω ± 1% metal film

Figure 8b. No Trim Unipolar Input Connections

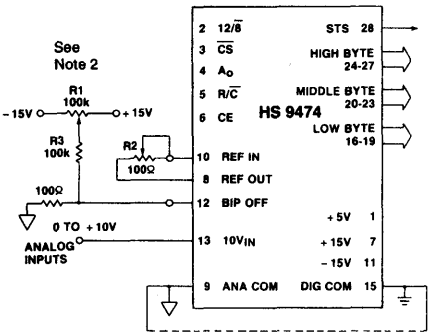


1. To increase adjustment range:
   a) Change R1 and R2 to 300 .
   b) Add series resistor 100Ω to ±5V input and 200Ω to ±10V input.

*Selected at factory.

**May be changd to 300Ω for greater adjustment capability.

Figure 9a. Bipolar Input Connections with Trim Adjustment



2. To increase adjustment range:
   a) Change R3 to 33kΩ, and R2 to 300
   b) Add series resistor 100Ω to ±5V input and 200Ω to ±10V input.

Figure 9b. Unipolar Input Connections with Trim Adjustment

ZERO ADJUSTMENT PROCEDURE

1. For unipolar ranges:
   a) Set input voltage precisely to +½LSB.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001.
2. For bipolar ranges:
   a) Set input voltage precisely to ½LSB above — F.S.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001

GAIN ADJUSTMENT PROCEDURE

1. Set input voltage precisely to ½LSB less than 'all bits on' value. Note that this is 1½LSB less than nominal full scale.
2. Adjust gain control until converter is switching from 111111111110 to 111111111111.

Table 4 summarizes the zero and gain adjustment procedure, and shows the proper input test voltages used in calibrating the HS 9474.

Table 4. Calibration Data

Input Voltage Range	Adjustment	Input Voltage	Adjust input to point where converter is just on the verge of switching between the two codes shown.[1]
-1 Model	ZERO	1.22mV	0000 0000 000Ø
0 to +10V	GAIN	9.9963V	1111 1111 111Ø
-1 Model	ZERO	-4.9988V	0000 0000 000Ø
±5V	GAIN	4.9963V	1111 1111 111Ø
-2 Model	ZERO	-9.9976V	0000 0000 000Ø
±10V	GAIN	9.9927V	1111 1111 111Ø

[1]Codes shown are natural binary for unipolar input ranges and offset binary for bipolar ranges.
Ø = a transition between logic "1" and logic "0".

POWER SUPPLY CONSIDERATION

Power supplies used for the HS 9474 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output codes may result with noisy power sources. It is important to remember that 2.44mV is 1LSB for a 10 volt input.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10 μF tantalum type in parallel with 0.1 μF disc ceramic type.

GROUNDING CONSIDERATIONS

The analog common at pin 9 is the ground reference point for the internal reference and is thus the high quality ground for the HS 9474; it should be connected directly to the analog reference point of the system. In order to achieve all of the high accuracy performance available from the HS 9474 in an environment of high digital noise content, it is recommended that the analog and digital commons be connected together at the package. In some situations, the digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred. If digital common contains high frequency noise beyond 200mV, this noise may feed through the converter, so that some caution will be required.

It is also important in the layout, to carefully consider the placement of digital lines. It is recommended that digital lines not be run directly under the 9474. For optimum system performance, if space permits, a ground plane is advised under the 9474. This should be connected to a digital ground. Finally, in packaging the assembled 9474, the designer should also try to minimize any capacitive coupling that might occur at the top to the device.

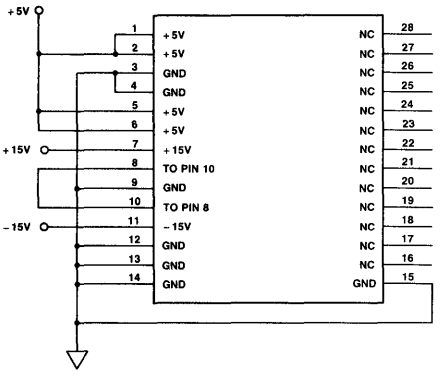


Figure 10. Burn-In Schematic

ORDERING INFORMATION

MODEL NUMBER	RESOLUTION MONOTONICITY	INPUT RANGE(S)	TEMPERATURE RANGE	SCREENING
HS 9474J-1	11 Bits	±5V, 0 to +10V	0° to +70°C	
HS 9474J-2	11 Bits	±10V	0° to +70°C	
HS 9474K-1	12 Bits	±5V, 0 to +10V	0° to +70°C	
HS 9474K-2	12 Bits	±10V	0° to +70°C	
HS 9474S/B-1	11 Bits	±5V, 0 to +10V	−55°C to +125°C	883 Rev. C, Level B
HS 9474S/B-2	11 Bits	±10V	−55°C to +125°C	883 Rev. C, Level B
HS 9474T/B-1	12 Bits	±5V, 0 to +10V	−55°C to +125°C	883 Rev. C, Level B
HS 9474T/B-2	12 Bits	±10	−55°C to +125°C	883 Rev. C, Level B

Specifications subject to change without notice.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9476

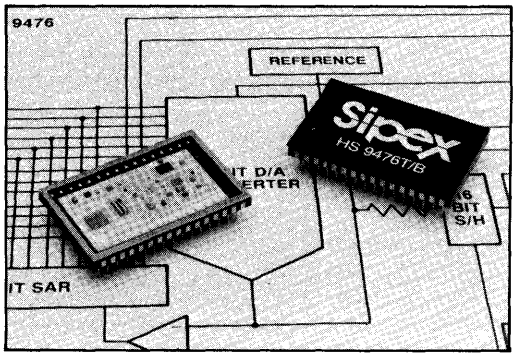
16-BIT SAMPLING A/D CONVERTER

FEATURES

- 16-bit ADC with internal 16-bit sample and hold amplifier
- 50kHz system throughput
- Pin for pin compatible with HS9576, BB ADC 76, AD 376

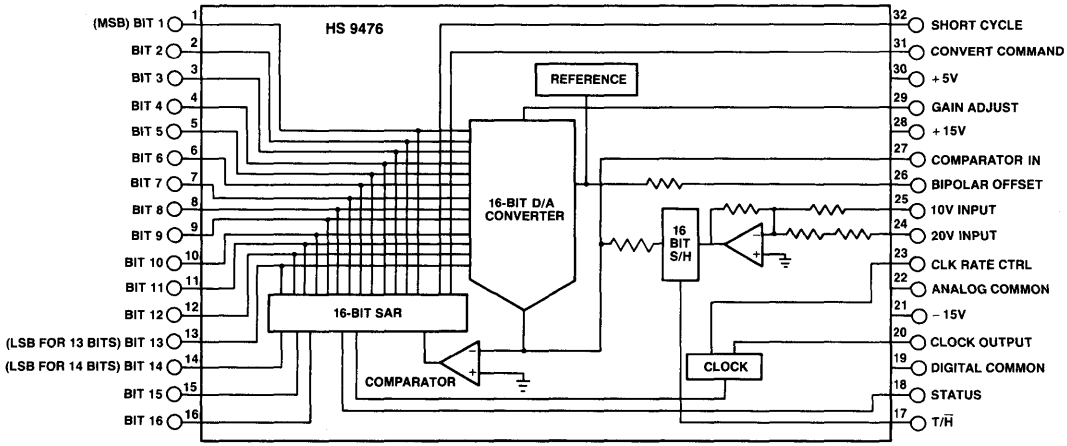
DESCRIPTION

Combining a 16-bit ADC and sample and hold amplifier (S/H) in a single 32 pin DIP, the HS9476 is a high accuracy sampling ADC capable of throughput rates up to 50kHz. Based on the HS9716, 16-bit 4μsec S/H and HS9576 16-bit 15μsec ADC the HS9476 is a pin compatible upgrade for the industry standard ADC 76/376 pin out. The S/H section has been specifically designed to match the requirements of the ADC for optimal performance. By integrating the S/H into the same package as the ADC, designers can avoid poor performance due to ground loops, signal coupling, and digital noise introduced when separate S/H and A/D converters are interconnected.



The HS9476 allows analog input ranges of ±5V, ±10V, 0 to +10V, and 0 to +20V. Integral nonlinearity is specified at ±0.003% of FSR maximum, while no missing codes is guaranteed for the full operating temperature range. The HS9476 is available for operation over the commercial (0°C to 70°C) temperature range or −55°C to +125°C with full MIL-STD-883C screening.

FUNCTIONAL DIAGRAM



10

SPECIFICATIONS

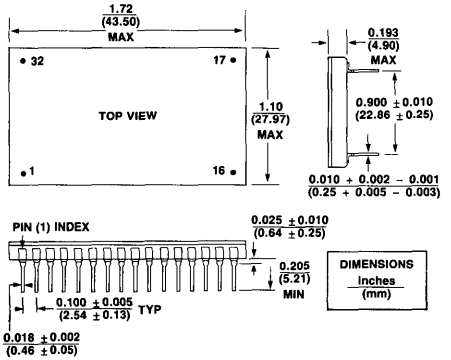
(Typical @ +25°C and nominal power supplies unless otherwise specified)

MODEL	HS 9476J	HS 9476K	HS 9476S/B	HS 9476T/B
RESOLUTION	16 bits	*	*	**
ANALOG INPUTS				
Voltage Range				
Bipolar	±5V, ±10V	*	*	**
Unipolar	0 to +10V, 0 to +20V	*	*	**
Overvoltage, No Damage				
10V Range	±15V max	*	*	**
20V Range	±30V max	*	*	**
Impedance				
10V Range	10kΩ	*	*	**
20V Range	20kΩ	*	*	**
DIGITAL INPUTS[1]				
Convert Command (Pin 31)	Positive pulse 50 nsec wide, trailing edge initiates conversion	*	*	**
Logic Loading	1 LSTTL load	*	*	**
T/H Command (Pin 17)	TRACK MODE, Logic "1"	*	*	**
	HOLD MODE, Logic "0"	*	*	**
DIGITAL OUTPUTS[1] (All Codes Complementary)				
Output Codes[2]				
Unipolar	CSB	*	*	**
Bipolar	COB, CTC	*	*	**
Output Drive	8 LSTTL loads	*	*	**
Status	Logic "1" during conversion	*	*	**
Status Output Drive	8 LSTTL loads	*	*	**
Internal Clock[3]				
Clock Output Drive	4 LSTTL loads	*	*	**
Frequency	933 kHz	*	*	**
TRANSFER CHARACTERISTICS				
Integral Linearity Error	0.006% of FSR max	0.003% of FSR max	0.006% of FSR max	0.003% of FSR max
Differential Linearity Error	0.003% of FSR typ, 0.006% of FSR max	*	*	**
Gain Error[4]	±0.05% typ; ±0.2% max	*	*	**
Offset Error[4]				
Unipolar	±0.05% of FSR typ, ±0.2% of FSR max	*	*	**
Bipolar	±0.05% of FSR typ, ±0.2% of FSR max	*	*	**
3σ Noise at Transitions (pk-pk)	0.003% of FSR max	*	*	**
DRIFT				
Gain	±20 ppm/°C max	*	*	**
Offset				
Unipolar	±5 ppm/°C of FSR max	*	*	**
Bipolar	±15 ppm/°C of FSR max	*	*	**
Linearity	±3 ppm/°C of FSR max	±2 ppm/°C of FSR max	±3ppm/°C of FSR max	±2ppm/°C of FSR max
Guaranteed No Missing Codes[5]	13 bits (0°C to 70°C)	14 bits (0°C to 70°C)	13 bits (−55°C to 125°C)	14 bits (−55°C to 125°C)
THROUGHPUT[6]				
Sampling Rate				
14-Bit Resolution	50 kHz typ, 47.6 kHz min	*	*	**
16-Bit Resolution	45.4 kHz typ, 43.4 kHz min	*	*	**
ADC CHARACTERISTICS				
Conversion Time[3] (t_{CONV})				
12-Bits	13μ sec max	*	*	**
14-Bits	15μ sec max	*	*	**
16-Bits	17μ sec max	*	*	**
SAMPLE/HOLD CHARACTERISTICS				
Track (Sample) Mode Dynamics				
Frequency Response				
Small Signal (−3 dB)	1 MHz	*	*	**
Full Signal Bandwidth	0.2 MHz	*	*	**
Slew Rate	6V/μsec	*	*	**
Noise in Track Mode, DC to 1.0 MHz	50μV rms	*	*	**
Hold Mode Dynamics				
Droop Rate	0.1μV/μsec max	*	*	**
Droop Rate at T_{max}	10μV/μsec max	*	*	**
Feedthrough Rejection				
(20Vp-p @ 20 kHz)	90 dB min	*	*	**
(20Vp-p @ 200 kHz)	86 dB min	*	*	**
Track (Sample)-To-Hold Switching				
Aperture Delay	30 nsec	*	*	**
Aperture Uncertainty	100 psec	*	*	**
Offset Step (Pedestal)	±2mV max	*	*	**
Switching Transient				
Amplitude	50mV	*	*	**
Settling to 1mV	0.5μsec	*	*	**
Settling to 0.3mV (t_{TH})	1μsec max	*	*	**
Hold-To-Track (Sample) Dynamics Acquisition Time to ±0.003% (20V Step) (t_{ACQ})	4μsec typ, 5μsec max	*	*	**
POWER REQUIREMENTS				
Power Consumption	1520 mW max	*	*	**
Rated Voltage, Analog	±15V (±0.5V max)	*	*	**
Rated Voltage, Digital	+5V (±0.5V max)	*	*	**
Supply Current				
+15V	+38 mA max	*	*	**
−15V	−51 mA max	*	*	**
+5V	+37 mA max	*	*	**
Power Supply Rejection	0.001%/% (all supplies)	*	*	**
Warm-Up Time	1 minute	*	*	**
TEMPERATURE RANGE				
Operating	0°C to +70°C	*	−55°C to +125°C	**
Storage	−25°C to +85°C	*	−65°C to +150°C	**
PACKAGE				
32 Pin				

NOTES:

1. Logic "0" = 0.8V max, Logic "1" = 2.0V min for inputs. For digital outputs Logic "0" = +0.4V max, Logic "1" = 2.4V min. **2.** CSB — Complementary Straight Binary. COB — Complementary Offset Binary. CTC — Complementary Two's Complement. **3.** With CLK RATE CTRL (Pin 23) left open. **4.** Adjustable to zero. **5.** A missing code is defined as less than 0.2 LSB wide. **6.** Throughput Rate = $1/(t_{ACQ} + t_{TH} + t_{CONV})$. *Specifications same as HS 9476J. **Specifications same as HS 9476S.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	32	SHORT CYCLE
2	BIT 2	31	CONVERT COMMAND
3	BIT 3	30	+5V
4	BIT 4	29	GAIN ADJUST
5	BIT 5	28	+15V
6	BIT 6	27	COMPARATOR IN
7	BIT 7	26	BIPOLAR OFFSET
8	BIT 8	25	10V INPUT
9	BIT 9	24	20V INPUT
10	BIT 10	23	CLOCK RATE CONTROL
11	BIT 11	22	ANALOG GROUND
12	BIT 12	21	−15V
13	BIT 13 (LSB FOR 13 BITS)	20	CLOCK OUT
14	BIT 14 (LSB FOR 14 BITS)	19	DIGITAL GROUND
15	BIT 15	18	STATUS
16	BIT 16	17	T/$\overline{H}$

Analog Input Voltage Range	Defined As:	±10V	±5V	0 to +10V	0 to +20V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	FSR 2^n	20V 2^n	10V 2^n	10V 2^n	20V 2^n
	n = 12	4.88mV	2.44mV	2.44mV	4.88mV
	n = 13	2.44mV	1.22mV	1.22mV	2.44mV
	n = 14	1.22mV	610μV	610μV	1.22mV
	n = 15	610μV	305μV	305μV	610μV
Transition Values MSB LSB					
000...000[4]	+ Full Scale	+ 10V − 3/2LSB	+ 5V − 3/2LSB	+ 10V − 3/2LSB	+ 20V − 3/2LSB
011...111	Mid Scale	0 − 1/2LSB	0 − 1/2LSB	+ 5V − 1/2LSB	+ 10V − 1/2LSB
111...110	− Full Scale	− 10V + 1/2LSB	− 5V + 1/2LSB	0 + 1/2LSB	0 + 1/2LSB

1. Complementary Offset Binary.
2. Complementary Two's Complement — obtained by inverting the most significant bit. MSB (pin 1).
3. Complementary Straight Binary.
4. Voltages given are the nominal value for transition to the code specified.

Table 1. Input Voltages, Transition Values, LSB Values, and Code Definitions

INSTALLATION

GROUNDING AND LAYOUT PRECAUTIONS

Due to the small bit weight (610 μV for 1 LSB, 14 bit, 10V range) special attention must be paid to the layout of the PC board. To avoid capacitive coupling from digital lines to the hybrid substrate, a ground-plane should be placed directly under the converter package on the component side. This ground plane can be directly connected to pin 22 of the HS 9476. All digital lines should run on the soldering side of the PC board.

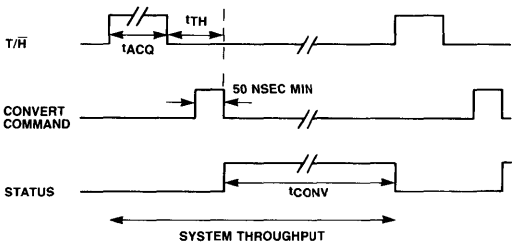
In general, analog and digital lines should be separated as far as possible and should not run in parallel. If analog and digital lines must cross, they should be at right angles to minimize coupling capacitance. The ground connection to the converter should be made using a wide, low resistive run to minimize voltage drop. Analog and digital ground lines must be connected at only one point, preferably directly at the converter package. For the HS 9476, pin 19 (digital ground) and pin 22 (analog ground) should be tied together as close as possible to the converter.

POWER SUPPLY DECOUPLING

Internal 0.01 μF power supply bypass capacitors are included in the HS 9476 to maintain device stability. If the supply voltages contain excessive high frequency noise, additional external high frequency capacitors may be necessary to maintain low noise performance.

OPERATING INSTRUCTIONS

The HS 9476 tracks an analog input signal when the T/$\overline{H}$ command is high. When entering the hold mode (T/$\overline{H}$ goes low), time must be given to the sample-hold amplifier for settling in the hold mode. Hence, the A/D conversion, initiated by the falling edge of the CONVERT COMMAND cannot begin immediately after the T/$\overline{H}$ command is low: a 1 μsec delay must be added to account for the hold mode settling as shown in the system timing diagram of Figure 1.

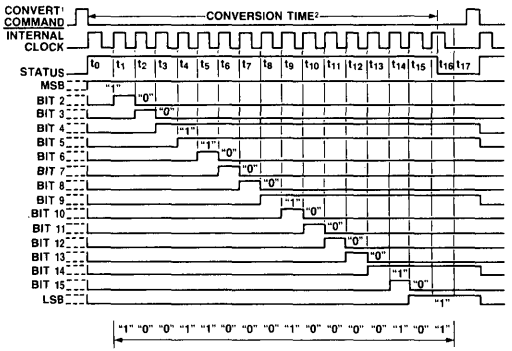


tACQ = SAMPLE-HOLD ACQUISITION TIME — 4μSEC TYP, 5μSEC MAX
tTH = SAMPLE-HOLD HOLD MODE SETTLING TIME — 1μSEC MAX
tCONV = A/D CONVERSION TIME — 14-BITS RESOLUTION — 15 SEC MAX
16 BITS RESOLUTION — 17μSEC MAX
SYSTEM THROUGHPUT = 14-BITS — 20μSEC TYP, 21μSEC MAX
16-BITS — 22μSEC TYP, 23μSEC MAX

Figure 1. System Timing Diagram

Simultaneous to a CONVERT COMMAND signal, the STATUS flag goes high indicating a conversion is in progress and removing the inhibit applied to the gated clock. The conversion is accomplished by successively comparing the analog input to the feedback DAC output, one bit at a time (MSB first, LSB last). After the LSB decision is made, there is a 30 nsec delay period before the STATUS flag goes low indicating that the conversion is complete and that the output data is valid. Incorporation of this 30 nsec delay guarantees that the digital data is valid at the logic "1" to "0" transition of the STATUS flag, allowing parallel data transfer to be initiated by the trailing edge of the STATUS signal. Resetting the STATUS flag to logic "0" restores the gated clock inhibit signal forcing the clock output to the logic "0" state. The clock remains low until the next conversion is initiated.

Figure 2 shows the detailed timing for the A/D converter of the HS 9476.



NOTES:
1. THE CONVERT COMMAND PULSE WIDTH IS 50nS MIN. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND. IF A NEW CONVERT COMMAND HAPPENS DURING CONVERSION, ALL THE LOGIC OF THE A/D IS RESET AND A NEW CONVERSION BEGINS.
2. 15μs FOR 14 BITS.

*Figure 2. A/D Timing Diagram (Output Code 1001100010000101)**

*All codes are complementary coded. Thus, the output code in Figure 2 represents an analog input whose positive true digital equivalent is 0110011101111010.

APPLICATIONS CIRCUIT

The purpose of this paragraph is to describe circuit examples for the implementation of the timing described earlier in Figure 1.

Figure 3 shows the circuit and the associated timing. The idea is to generate the T/$\overline{H}$ command from the CONVERT COMMAND signal and the STATUS flag.

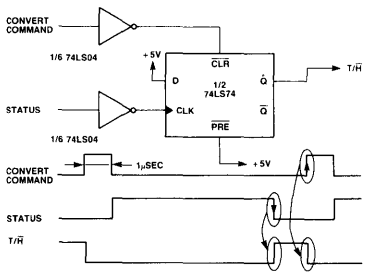


Figure 3. Generation of the T/$\overline{H}$ Command from CONVERT COMMAND and STATUS

The rising edge of the CONVERT COMMAND makes the T/$\overline{H}$ command going low (hold mode). The falling edge of the STATUS flag makes the sample-hold going back in track mode (T/$\overline{H}$ = "1").

To obtain the maximum throughput (HS 9476 short cycled to 14 bits), the CONVERT COMMAND should be a 50 kHz signal. Figure 4 shows how to obtain it from a 500 kHz clock. Slowing down this frequency reduces the throughput rate, which is given by fclock/10.

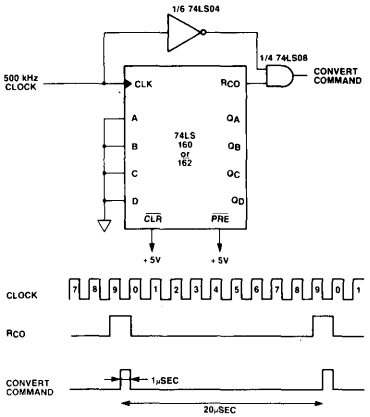


Figure 4. Generation of the CONVERT COMMAND

Using the schematics of Figure 3 and Figure 4 for applying the HS 9476 necessitates only 4 ICs: 74LS08, 74LS04, 74LS74 and 74LS160.

OPTIONAL UNIPOLAR OFFSET OR BIPOLAR ZERO ADJUST

The unipolar offset or bipolar zero error may be trimmed to zero (optional) using an external trim potentiometer connected to the HS 9476 as shown in Figures 5 or 6.

The adjustment circuit shown in Figure 5 consists of a 100 ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 1.8MΩresistor to pin 27. In this case a carbon composition resistor is adequate: if we assume that its tempco is −1200 ppm/°C and that the adjustment range required is no more than 16 LSB_{14} (0.1% FS), it contributes for only 1.17 ppm/°C of tempco (0.001 x 1200). The low tempco adjustment circuit in Figure 6 contributes for negligible tempco if metal film resistors (tempco <100 ppm/°C) are used.

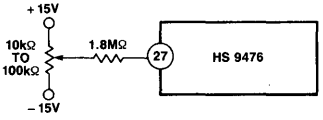


Figure 5. Unipolar Offset or Bipolar Zero Adjustment Circuit (±0.4% FSR)

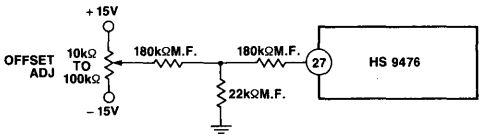


Figure 6. Low Tempco Adjustment Circuit

With both circuits the fixed resistor connected to pin 27 should be located close to the converter to keep the pin connection runs short. Offset or zero should be adjusted after warm-up and before gain (see below) to prevent interaction of the two adjustments. Offset or zero is adjusted with the analog input near zero volt. Refer to Table 1 for the appropriate values.

OPTIONAL GAIN ADJUST

The gain error may be trimmed to zero (optional) using an external offset trim potentiometer connected to the HS 9476 as shown in Figure 7.

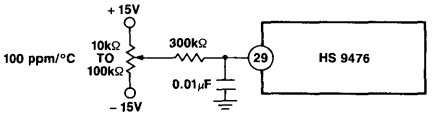


Figure 7. Gain Adjustment Circuit (± 0.2% FSR)

The gain adjustment circuit shown in Figure 7 consists of a 100 ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 300 K Ω resistor to pin 29. Gain should be adjusted after warm-up and after unipolar offset or bipolar zero (see above) to prevent interaction of the two adjustments. Gain is adjusted with the analog input near the most positive end of the analog range. Refer to Table 1 for the appropriate values.

OPTIONAL CONVERSION TIME ADJUST

Short Cycle: A SHORT CYCLE input, pin 32, permits the A/D timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted. For instance, when 14-bit resolution is desired, pin 32 is connected to bit 15 (output pin 15). The conversion cycle will then terminate and the STATUS flag reset after the bit 14 decision has been made. SHORT CYCLE connections and associated conversion times are summarized in Table 2 below for a 933 kHz clock.

Resolution Bits	(%FSR)	Max Conversion Time (μs)	Connect SHORT CYCLE Pin 32* to Pin:
16	0.0015	17.1	N/C (open)
15	0.003	16.1	16
14	0.006	15.0	15
13	0.012	13.9	14
12	0.024	12.9	13
10	0.100	10.7	11

*Pin 32 cannot be connected to +5V

Table 2. Short Cycle Connections

Clock Rate Adjust: The A/D of the HS 9476 may be operated at faster or slower conversion times by connecting the CLOCK RATE CONTROL, pin 23, to an external multiturn trim potentiometer with a TCR of ± 100 ppm/°C or less as shown in Figure 8. The conversion time is trimmed to 17μsec (16-bits) at the factory with CLK RATE CTRL open. The typical conversion time versus the clock rate control voltage is shown in Figure 9. The nonlinearity errors will vary with speed as shown in Figure 10.

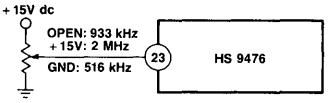


Figure 8. Optional Clock Rate Control Circuit

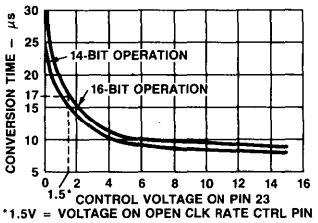


Figure 9. Conversion Time Vs. Clock Rate Control Voltage

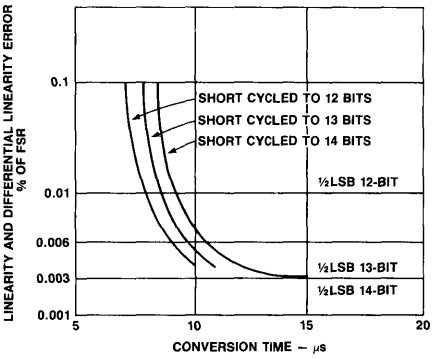


Figure 10. HS 9476 Nonlinearity Vs. Conversion Time

DIGITAL OUTPUT DATA

Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Complementary two's complement may be obtained by inverting MSB (pin 1). Table 1 shows the LSB, transition values and code definitions for each possible analog input signal range for 12-15 bits of resolution. The output data is CMOS compatible and the drive capability is 8 LSTTL loads. If long digital lines have to be driven, external output buffers are recommended.

INPUT SCALING

The HS 9476 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table 3.

Input Signal Range	Output Code	Connect Pin 26 To Pin	Connect Pin 24 To	Connect Pin 25 To
± 10V	COB or CTC*	27	Input Sig.	Pin 22
± 5V	COB or CTC*	27	Pin 22	Input Sig.
0 to +10V	CSB	22	Pin 22	Input Sig.
0 to +20V	CSB	22	Input Sig.	Pin 22

*Obtained by inverting MSB (pin 1)

NOTE: The unused analog input is grounded to reduce noise pickup.

Table 3. HS 9476 Input Scaling Connections

CONNECTIONS AND CALIBRATION PROCEDURE
(14-Bit Resolution Example)

Figures 11a and 11b show the different analog and power connections required for unipolar 0 to 10V and bipolar −10V to +10V input range operation.

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figure 11, are used for device calibration. To prevent interaction of these two adjustments, unipolar offset or bipolar zero is always adjusted first and then gain.

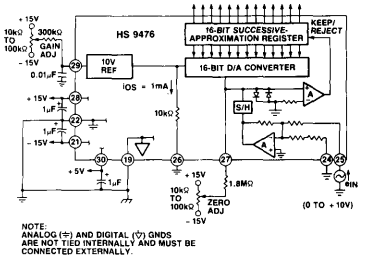


Figure 11a. Analog and Power Connections for Unipolar 0 to +10V Input Range

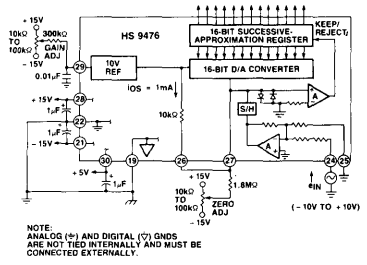


Figure 11b. Analog and Power Connections for Bipolar −10V to +10V Input Range

CALIBRATION FOR 0 TO +10V RANGE

Set analog input to $+1\ LSB_{14}$ = 0.00061V. Adjust ZERO for digital output = 11111111111110. ZERO is now adjusted. Set analog input to $+FS - 2\ LSB_{14}$ = 9.99878V. Adjust GAIN for 00000000000001 digital output code; GAIN is now calibrated. Half scale calibration check: set analog input to +5V; digital output code should be 01111111111111.

CALIBRATION FOR −10V TO +10V RANGE
(Complementary Offset Binary Code)

Set analog input to 0.00000V; adjust ZERO for 01111111111111 digital output code. Set analog input to 9.99756V ($+FS - 2\ LSB_{14}$); adjust GAIN for 00000000000001 digital output code.

OTHER RANGES

Coding relationships and calibration points for 0 to +20V and −5V to +5V ranges can be found by doubling and halving respectively the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, as indicated in Table 1.

Unipolar offset or bipolar zero and full-scale calibrations can be accomplished to a precision of ±½ LSB using the static adjustment procedure described above.

DISCUSSION OF SPECIFICATIONS

SYSTEM SPECIFICATIONS

The actual conversion errors that are associated with the HS 9476 are combinations of analog errors due to the sample-hold amplifier and the A/D.

Figure 12 shows the ideal HS 9476 transfer characteristics.

All the system specifications include the errors introduced by both the sample-hold amplifier and the A/D converter. The offset error is a shift (left or right) of the ideal transfer characteristics. Gain error is an error in the slope of the transfer function. Both these errors can be trimmed externally as explained earlier. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristics from a zero input voltage (which calls for an "all 1's" digital output) to a point which is defined as a full scale **(END POINT definition).** Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size. If the differential linearity is too negative, a code can be missing. The HS 9476K and T/B are specified as having no missing codes at the 14 bit level for the commercial and military temperature ranges.

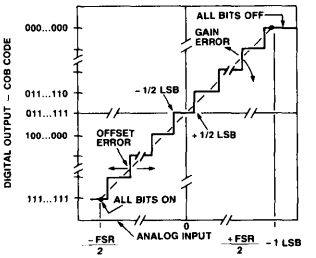


Figure 12. Ideal HS 9476 Transfer Characteristics (Bipolar Mode)

SAMPLE/HOLD SPECIFICATIONS

Acquisition Time is the time required by the sample/hold amplifier to "switch" from the hold mode to the track (sample) mode. This time is measured between the application of a "track" command and the point at which the output has settled to within a specified error band. This time includes the switch delay time, slewing time and settling time for a given output voltage change.

Switching Transient Settling (Hold Mode Settling) is the time required for the device to stabilize in the hold mode to within specified limits of its final value after the hold mode signal has been given.

Aperture Delay is the time lag between the application of the "hold" command and the instant the output stops tracking the input. It consists primarily of the propagation delay of the switch driver. Since it is a known quantity, the "hold" command can be advanced to account for this delay.

Offset Step (Pedestal) is a track (sample)-to-hold offset that results from unequal charge transfers when the device is switched into the hold mode.

Aperture Uncertainty (Jitter) is the variation in the aperture delay from sample to sample. This time uncertainty produces a voltage uncertainty proportional to the input slew rate.

Feedthrough is the amount of analog input signal that is coupled through to the analog output while the circuit is in the hold mode. It is usually expressed in dB's. Since feedthrough increases with frequency, it should be specified at a given frequency.

Droop Rate is the rate of change in output voltage over time while in the hold mode. The droop rate will determine how long a signal can be accurately held before it changes more than 1 LSB. This, in turn, determines the maximum conversion time that an A/D converter can have to be used with a particular S/H.

Full Power Bandwidth is the frequency at which a full scale input/output sine wave becomes slew rate limited to −3 dB.

Small Signal Bandwidth is the maximum analog signal frequency that can be tracked before the gain is reduced by 3 dB. This assumes the signal amplitude is small enough so as not to be slew rate limited.

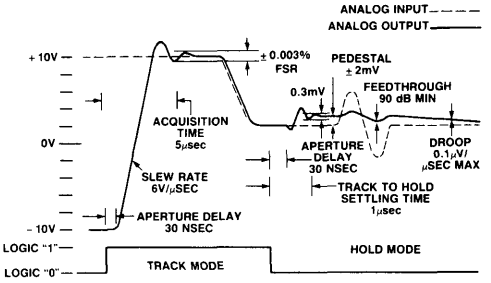


Figure 13. Illustration of the Main S/H Characteristics

DYNAMIC PERFORMANCE

The system specifications discussed earlier describe the DC performance of the HS 9476. For digital signal processing oriented applications, however, the response of the sampling A to D converter to AC signals must be known.

At Hybrid Systems, two different kinds of dynamic testing can be performed on the device:

1. Signal-to-Noise Ratio (SNR) test
2. Histogram test

These tests are discussed in the following paragraphs. They have been performed on devices **short cycled to 14 bits (in order to get a 50kHz throughput rate)** and configured in bipolar 10V mode.

The SNR test is the primary measurement of signal fidelity: distortion of an input sinewave due to Integral Linearity errors is quantified by this test. More precisely a finite time sequence of sampled data from a spectrally pure sine wave input is computed by the tester into a frequency spectrum using a Fast Fourier Transform algorithm. From this frequency domain representation of the output data, the effect of Integral Non-Linearity may be measured: harmonics of the input sine wave caused by Integral Linearity errors are aliased into the baseband spectrum. The magnitude of the fundamental's spectral lines (the signal) is summed, then divided by the sum of the remaining spectral lines (the noise). The logarithm of this number, multiplied by 20 provides the SNR expressed in decibels. For an ideal converter, it can be shown that:

$$SNR = 6.02 \times N + 1.76dB$$

(N = number of bits of the converter)

For a 14 bit converter, the SNR should be 86dB for all frequencies below the Nyquist rate (25kHz for the HS 9476). If the linearity error is ±½LSB, a SNR of 3dB less is expected.

Figure 14 to 16 show the SNR results of the HS 9476 for full scale input frequency of 2.345, 12.345, 23.456kHz respectively. This shows the very slow degradation of the SNR with the input frequency.

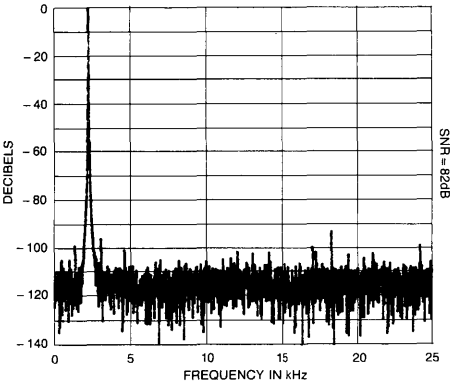


Figure 14. FFT of the HS 9476, Fin = 2.234kHz, Fsample = 50kHz

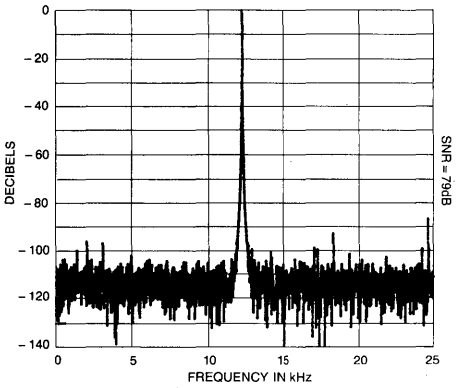


Figure 15. FFT of the HS 9476, Fin = 12.234kHz, Fsample = 50kHz

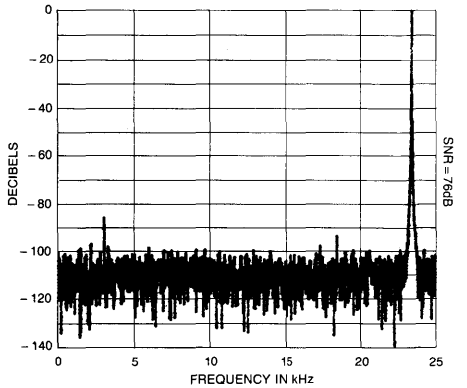


Figure 16. FFT of the HS 9476, Fin = 23.234kHz, Fsample = 50kHz

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The HS 9476 will exhibit an improvement in SNR when less than full scale input signal is applied. Figure 17 illustrates that improvement.

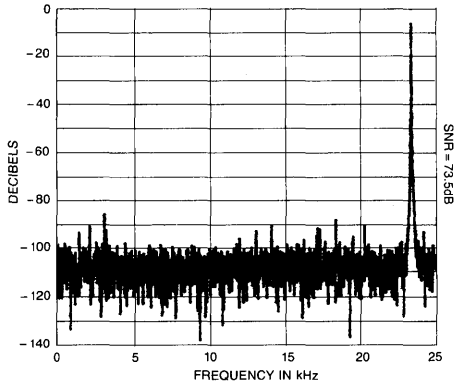


Figure 17. FFT of the HS 9476, Fin = 23.346kHz, Fsample = 50kHz, – 6dB input levels

Histogram testing is used to evaluate the dynamic differential linearity of a converter. A sine wave is applied to the converter and a finite number of sampled data is taken and stored by the tester. The number of occurences of each code is then determined, and this histogram is compared with an ideal quantized sine wave of same gain and offset. The ratio of the real number of occurences to the ideal number yields an effective code width for each code. Figure 18 shows the good dynamic differential linearity of the HS 9476 even when the input signal approaches the Nyquist bandlimit.

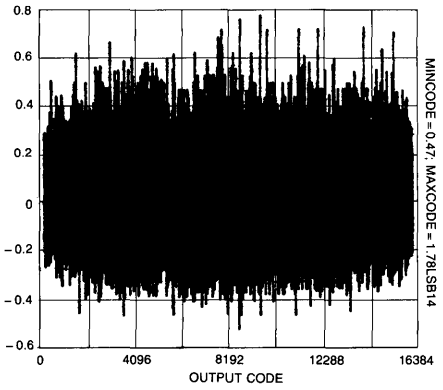


Figure 18. HS 9476 Dynamic Differential Linearity, Fin = 23.456kHz, Fsample = 50kHz

ORDERING INFORMATION

MODEL	MAX LINEARITY ERROR	TEMPERATURE RANGE	SCREENING
HS 9476K	±0.003% FSR	0°C to +70°C	—
HS 9476J	±0.006% FSR	0°C to +70°C	—
HS 9476T/B	±0.003% FSR	–55°C to +125C	MIL-STD-883
HS 9476S/B	±0.006% FSR	–55°C to 125°C	MIL-STD-883

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP9478

14-BIT, 400 kHz SAMPLING A/D CONVERTER

FEATURES

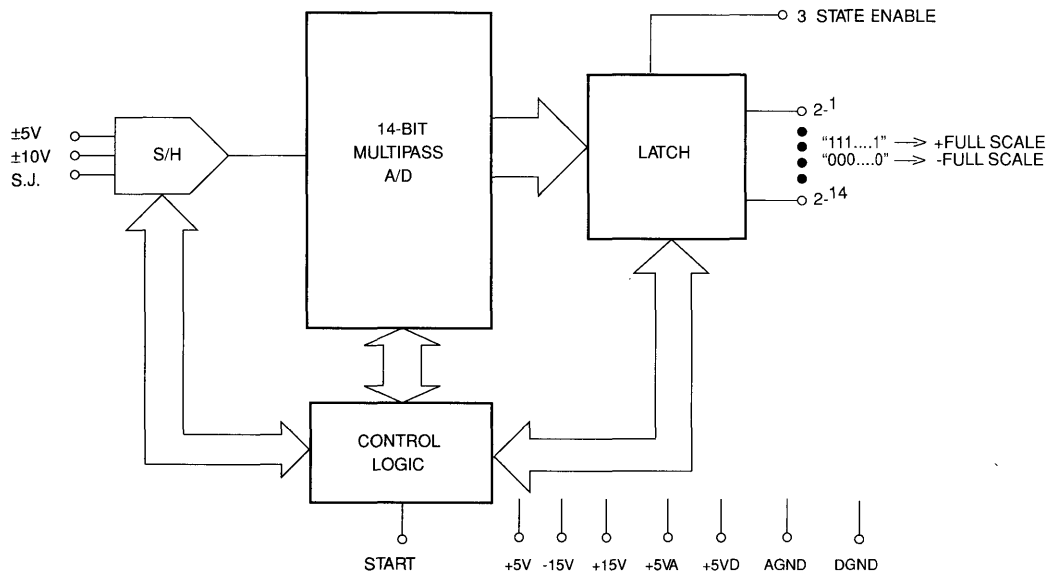
- 400 kHz Throughput
- Internal Sample-Hold
- Three State Output
- 0.003% FSR Accuracy

DESCRIPTION

The SP9478 is a high speed, 14-Bit A/D which combines a high speed sample hold and A/D in a single package. The A/D section utilizes the Multipass process, combining two 8-Bit flash converters in a feed-forward error correction scheme to yield resolution of 14-Bits. The sample-hold section has been specifically designed to match the requirements of the ADC for optimal performance. The SP9478 provides user selectable input ranges of ±2.5V, ±5V and ±10V. Three state outputs provide easy interface to microprocessor bus structures. Packaged in a 32 pin dual in-line package the SP9478 is available for -55° C to +125° C operation with MIL-STD-883C screening.

PRELIMINARY INFORMATION

FUNCTIONAL DIAGRAM



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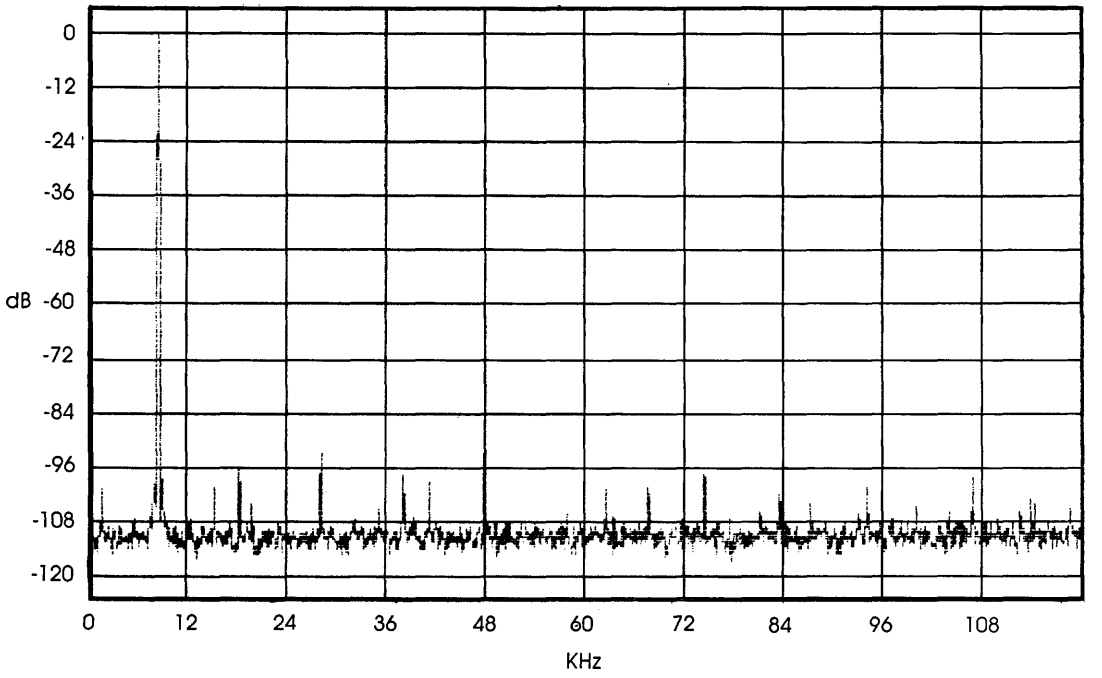
SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Typical @25°C and Nominal Supply Voltages unless otherwise noted)					
PARAMETERS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG INPUTS Voltage Range		 -10 -5 -2.5		 +10 +5 +2.5	 Volts Volts Volts
DIGITAL INPUTS Logic Levels Logic Loading	 Logic 1 Logic 0	 2.4	 1	 0.4	 Volts Volts TTL Load
STATIC PERFORMANCE Integral Linearity Differential Linearity No Missing Codes			 ±1 ±1/2	 ±1 14	 LSB LSB Bits
CONVERSION & THROUGHPUT Throughput A/D Conversion Time S/H Acquisition Time			 400 1.5 1.0		 kHz µsec µsec
STABILITY Integral Linearity Tempco Differential Linearity Tempco Offset Error Drift Gain Error Drift			 2 2 5 25		 ppm/°C ppm/°C ppm/°C ppm/°C
DIGITAL OUTPUTS Coding Output Drive			 3		 Straight Binary TTL Loads
DYNAMIC PERFORMANCE Signal to Noise + Distortion Fin=10 kHz Fin=100 kHz	 Input = 0 dB Input = -20 dB		 80 55		 dB dB
POWER SUPPLY REQUIREMENTS +15V -15V +5V Digital +5V Analog -5V Dissipation			 45 45 175 85 25 2.75		 mA mA mA mA mA W

PIN ASSIGNMENTS

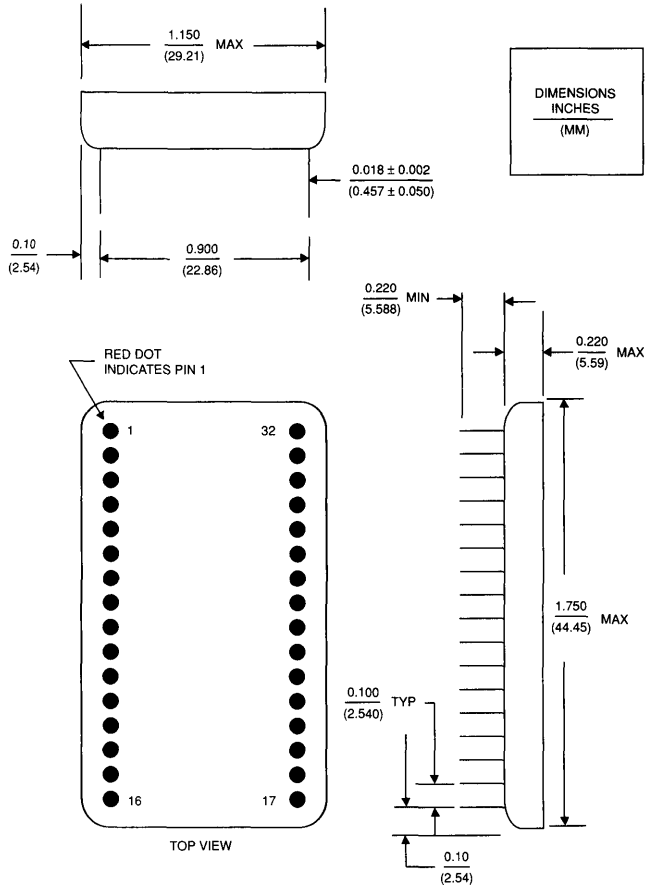
PIN	FUNCTION
1	Analog Ground
2	Analog Ground
3	+5V Analog
4	–5V Analog
5	+5V Digital
6	Digital Ground
7	Digital Ground
8	Start Convert
9	Output Enable (High)
10	Bit 14 (LSB)
11	Bit 13
12	Bit 12
13	Bit 11
14	Bit 10
15	Bit 9
16	Bit 8

PIN	FUNCTION
17	Bit 7
18	Bit 6
19	Bit 5
20	Bit 4
21	Bit 3
22	Bit 2
23	Bit 1 (MSB)
24	Analog Ground
25	–15V
26	+15V
27	NC
28	Analog Ground
29	Digital Ground
30	Summing Junction
31	±10V
32	±5V

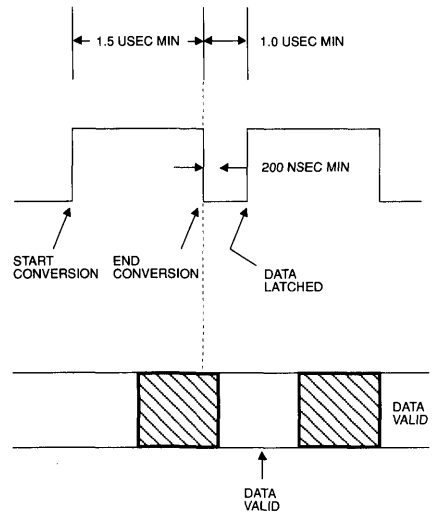


Graph 1. SINAD = 79.84 dB

PACKAGE OUTLINE



TIMING DIAGRAM



Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP9560

12-BIT 10 MHz SAMPLING A/D CONVERTER

FEATURES

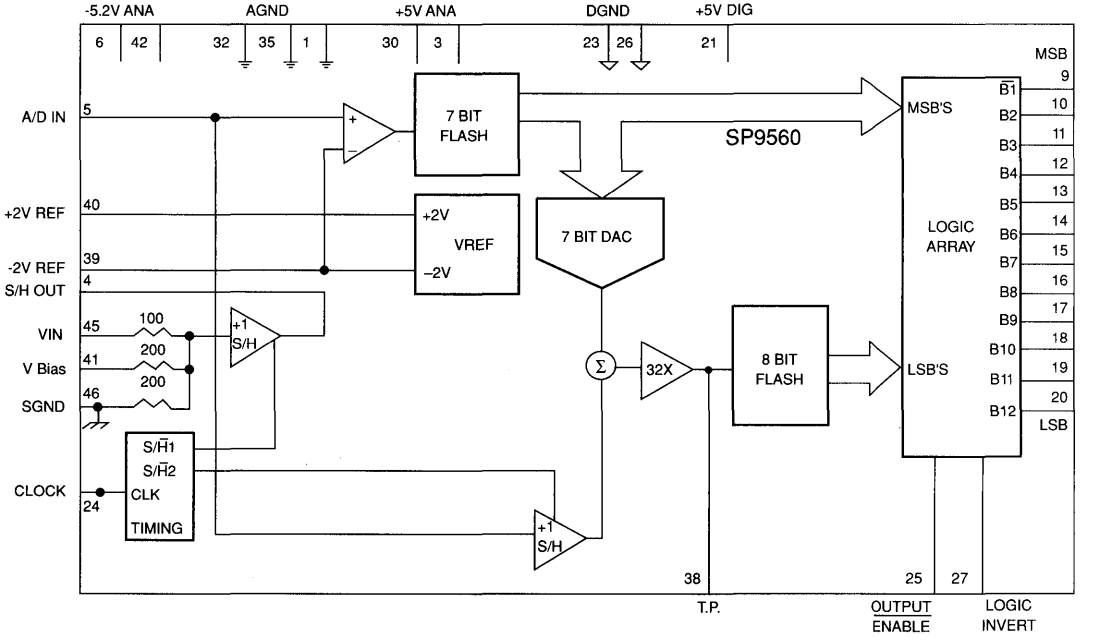
- 10 MHz Sampling Rate
- Complete with SHA and Reference
- High Signal/Noise Ratio: 69 dB
- High SINAD Ratio: 68 dB
- Low Harmonic Distortion: -72 dB
- Low Power Consumption: 3.6W
- 0°C to +70°C and -55°C to +125°C

PRELIMINARY INFORMATION

DESCRIPTION

The SP9560 is a 10 MHz sample rate, 12-Bit Analog-to-Digital converter which includes all components necessary to digitize an incoming analog signal. The SP9560 includes a 12-Bit A/D Converter, a sample and hold amplifier, an on-board reference and all of the control logic necessary for complete functionality. The SP9560 has very low power consumption of 3.6 Watts, can digitize signals up to 10 MHz, and has excellent Signal to Noise + Distortion performance of 68 dB with total harmonic distortion of -72 dB. The SP9560 uses two's complement or inverted two's complement coding and is designed to function over the military temperature range of -55°C to +125°C. All this is packaged in a 46-pin dual in-line package, and will be available with MIL-STD-883C screening.

FUNCTIONAL DIAGRAM



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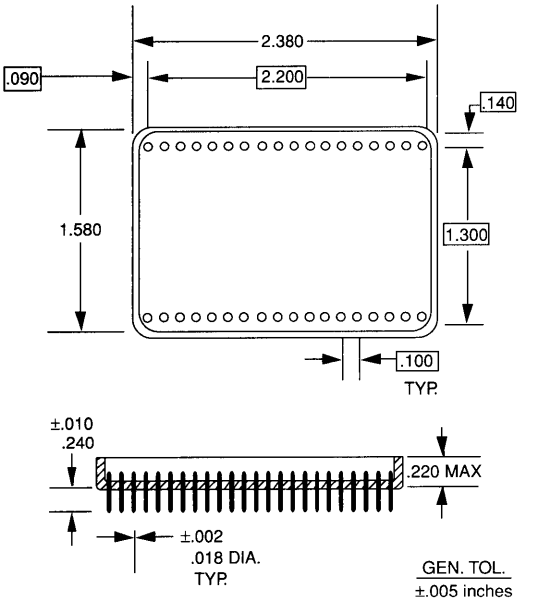
SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (Typical @ 25°C and Nominal Supply Voltages unless otherwise noted)					
PARAMETERS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG INPUTS					
Voltage Range			±1.0V		Volts
DIGITAL INPUTS					
Logic Levels	Logic 1	2.4			Volts
	Logic 0			0.5	Volts
Logic Loading			1		TTL Load
STATIC PERFORMANCE					
Differential Linearity			±0.5		LSB
Integral Linearity			±0.5		LSB
No Missing Codes					Bits
Gain Error			±0.75		%FSR
Offset Error			±0.75		%FSR
DYNAMIC PERFORMANCE					
Signal to Noise Ratio	(10 MHz clock)				
Fin=100 kHz			69		dB
Fin=4.99 MHz			69		dB
Signal to Noise + Distortion	(10 MHz clock)				
Fin=100 kHz			68		dB
Fin=4.99 MHz			64		dB
Total Harmonic Distortion	(10 MHz clock)				
Fin=100 kHz	-0.5 dB		-72		dB
Fin=4.99 kHz	-0.5 dB		-68		dB
Dynamic Differential Linearity	(10 MHz clock)		±0.5		LSB
A.C. PARAMETERS					
Throughput			10		MHz
S/H Aperture Delay			5		nsec
S/H Aperture Time			1		nsec
S/H Aperture Jitter			10		psec RMS
DIGITAL OUTPUTS					
Coding					Two's Complement Inverted 2's Comp
Output Drive			2		TTL Loads
POWER SUPPLY REQUIREMENTS					
PSRR			±0.01		%/%
+5V Digital			193		mA
+5V Analog			350		mA
-5.2V Analog			280		mA
Dissipation			3.6		W

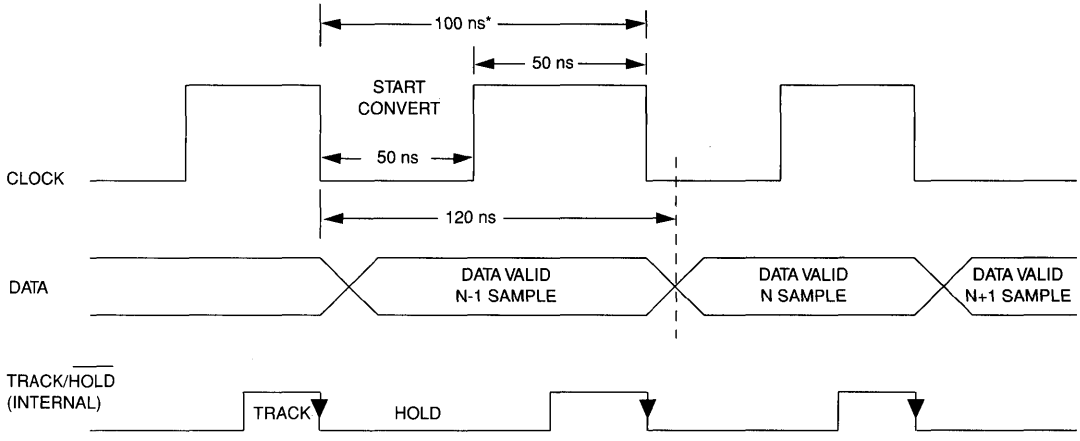
PIN ASSIGNMENTS

PIN	FUNCTION
1	AGND
2	N.C.
3	+5V Analog
4	S/H Out
5	A/D In
6	-5V Analog
7	N.C.
8	N.C.
9	Bit 1 $\overline{D11}$ (MSB)
10	Bit 2 D10
11	Bit 3 D9
12	Bit 4 D8
13	Bit 5 D7
14	Bit 6 D6
15	Bit 7 D5
16	Bit 8 D4
17	Bit 9 D3
18	Bit 10 D2
19	Bit 11 D1
20	Bit 12 D0
21	+5V Digital
22	N.C.
23	DGND
24	Clock
25	Output $\overline{\text{Enable}}$
26	DGND
27	Logic Invert
28	N.C.
29	N.C.
30	+5 VA
31	N.C.
32	AGND
33	N.C.
34	N.C.
35	AGND
36	N.C.
37	N.C.
38	Test Point
39	-2V Ref
40	+2V Ref
41	V Bias
42	-5.2V Analog
43	N.C.
44	N.C.
45	Vin
46	SGND

PACKAGE OUTLINE



TIMING DIAGRAM



*DUTY CYCLE MUST BE 50%

DATA-ACQUISITION SYSTEMS

MODEL	RESOLUTION (BITS)	CHANNELS		S/H ACQUISITION TIME (µs)	A/D CONVERSION TIME (µs)	IA GAIN RANGE	MAXIMUM THROUGHPUT	POWER CONSUMPTION (mW)	PACKAGE	PAGE
		NO. OF INPUTS	TYPE OF INPUTS							
HS9404/08	12	4/8	DI/SE	6	25	1-100	35 kHz	950	40-Pin DD	529
HS9410	12	8	SE	6	25	N/A	25 kHz	600	28-Pin DD	535
HS9414	12	4	DI	6	25	1-500	25 kHz	980	40-Pin DD	543
SP9415	12	8	SE	1	12	N/A	75 kHz	1100	28-Pin DD	555
HS9403	12	8/16	DI/SE	9	10	1-1000	50 kHz	1500	62-Pin	523
HS362	12	8/16	DI/SE	7	N/A	N/A	N/A	1000	32-Pin TD	519
SP9462/63	12	8/16	DI/SE	5	25	1-100	45 kHz	1000	68-Pin	563
SP9480	16	8	SE	13	20	N/A	25 kHz	1200	32-Pin TD	567
SP9488	16	8/16	DI/SE	3	16	1	50 kHz	1400	62-Pin	575

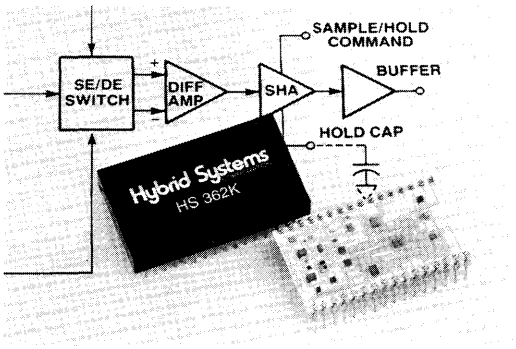
Shaded area indicates new product since publication of 1988 Catalog

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

16-CHANNEL MULTIPLEXER WITH PRECISION SAMPLE-AND-HOLD

FEATURES

- 16SE or 8DIF inputs switchable mode control
- High speed: 7μSec acquisition time to 0.01%
- Complete front end for 12-bit DAS
- Protected multiplexer inputs



DESCRIPTION

The HS362 is a complete 12-bit data acquisition system front end network. The HS362 contains two 8-channel multiplexers and a precision sample and hold that can be user configured to accept either 8 differential inputs or 16 single-ended inputs.

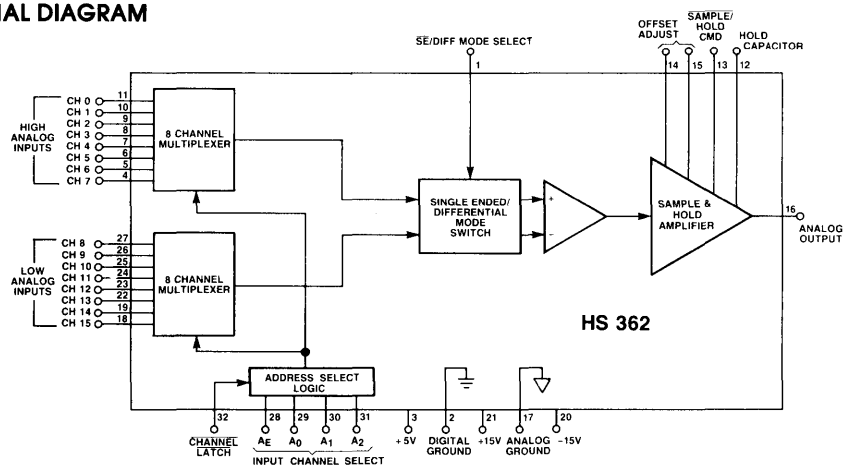
The sample and hold amplifier is designed to work in conjunction with most ADC's by connecting the 'status' output of the ADC to the SAMPLE/HOLD control input of the HS362. The 'convert' command to the ADC will switch the HS362 into 'hold' mode during conversion. An output buffer is provided so that the user can connect the HS362 directly to the unbuffered analog input of most 12-bit successive approximation type ADC's.

When the HS362 is used with a 12-bit, 25-microsecond ADC such as the HS574, system throughput rate is 30kHz for full 12-bit precision.

PRODUCT HIGHLIGHTS

1. The 16-input channels can be user configured for either single-ended or differential operation. The mode select switching is LSTTL compatible for greater system flexibility.
2. The HS362 when used with a 12-bit ADC such as the HS574 forms a complete, high speed, μP compatible data acquisition system.
3. Channel select addressing is combined with a latch control to facilitate interface to μP busses.
4. A precision hold capacitor is provided with each HS362.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

(Typical @ +25°C and nominal power supplies unless otherwise specified)

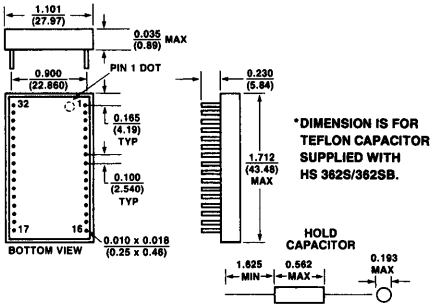
MODEL	HS 362K	HS 362S/HS 362SB[1]
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential	*
Voltage Range[6]	±10V	*
Bias Current, per Channel	±50nA max	*
Impedance		
ON Channel	$10^{10}\Omega$ || 100pF	*
OFF Channel	$10^{10}\Omega$ || 10pF	*
Fault Current	20mA, Internally limited	*
CMR		
Differential Mode @1kHz, $20V_{p-p}$	70dB min (80dB typ)	*
MUX Crosstalk		
Any OFF Channel to any ON Channel @1kHz, $20V_{p-p}$	−80dB max (−90dB typ)	*
Offset, Channel to Channel	±500μV max	*
ACCURACY		
Offset Error, T_{Min} to T_{Max}	±4mV max	*
Gain Error, T_{Min} to T_{Max}	±0.02% FSR max	*
Linearity Error		
@25°C	±0.01% max	±0.005% max
T_{Min} to T_{Max}	±0.015% max	±0.01% max
Noise Error		
@25°C	$1mV_{p-p}$, 0.1 to 1MHz max	*
T_{Min} to T_{Max}	$2mV_{p-p}$, 0.1 to 1MHz max	*
DRIFT (T_{Min} to T_{Max})		
Gain	±4ppm/°C max	±2ppm/°C max
Offset, ±10V Range	±4ppm/°C max	*
DIGITAL INPUT[2]		
INPUT CHANNEL SELECT	4-Bit Binary, CHANNEL ADDRESS	*
	1LS TTL Load	*
$\overline{\text{CHANNEL LATCH}}$	"1" = Latch Transparent	*
	"0" = Latched	*
	8LS TTL Loads	*
$\overline{\text{SE}}$/DIFF	"0" = Single-ended Mode	*
	"1" = Differential Mode	*
	2LS TTL Loads	*
$\overline{\text{SAMPLE}}$/HOLD	"0" = Sample	*
	"1" = Hold	*
	High Impedance Input[3]	*
	V_{TH} = +1.4V	*
SAMPLE AND HOLD DYNAMICS		
Acquisition Time, for 20V Step to ±0.01% of Final Value[4]	7μsec, 10μsec max	*
SAMPLE TO HOLD Step	6mV	*
Settling Time, Hold Mode to ±1mV of Final Value	600nsec	*
Feedthrough @1kHz	−70dB, −60dB max	*
Droop Rate	0.02mV/ms, 1mV/ms max	*
Aperture Delay	225nsec	*
Aperture Uncertainty	10nsec	*
POWER SUPPLY REQUIREMENTS[5]		
Rated Voltage/Current	+15V, ±5% @ 40mA max	30mA max
	−15V, ±5% @ 20mA max	30mA max
	+5V, ±5% @ 25mA max	20mA max
Total Power	775mW (typ) 1.0 Watt max	500mW typ, 1W max
TEMPERATURE RANGE		
Operation	0 to 70°C	−55°C to +125°C
Storage	−25°C to +85°C	−55°C to +150°C

NOTES:

1. The HS 362SB is processed and screened to the requirements of MIL-STD-883C, Rev C, Level B.
2. One LS TTL load is defined as: $I_{IL} = -0.36mA$ max @$V_{IL} = 20\mu A$ max @$V_{IH} = 2.7V$.
3. Less than 1 LSTTL load.
4. For optimum acquisition time performance the analog input should be buffered with a low output impedance.
5. The power supplies should be sequenced in this order: +15V, −15V, +5V to avoid latch-up.
6. Input voltage is limited to $V_{DD} - 4$ volts maximum, or 11 volts for a 15 volt supply.

*Specifications same as HS 362K.

PACKAGE OUTLINE



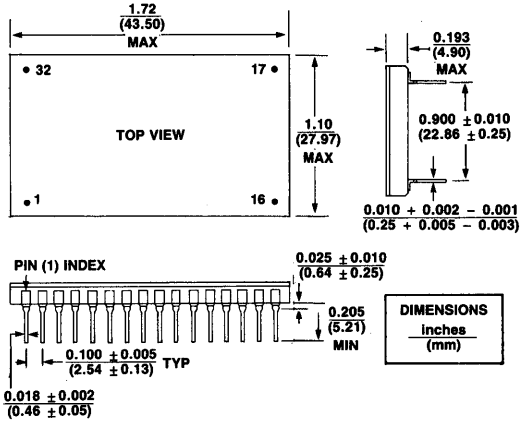
PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	$\overline{\text{SE}}$/DIFF MODE SELECT	32	$\overline{\text{CHANNEL LATCH}}$
2	DIGITAL GROUND	31	INPUT CHANNEL ADDRESS, BIT A_2
3	+5V	30	INPUT CHANNEL ADDRESS, BIT A_1
4	ANALOG INPUT, CHANNEL 7	29	INPUT CHANNEL ADDRESS, BIT A_0
5	ANALOG INPUT, CHANNEL 6	28	INPUT CHANNEL ADDRESS, BIT A_E
6	ANALOG INPUT, CHANNEL 5	27	ANALOG INPUT, CHANNEL 8
7	ANALOG INPUT, CHANNEL 4	26	ANALOG INPUT, CHANNEL 9
8	ANALOG INPUT, CHANNEL 3	25	ANALOG INPUT, CHANNEL 10
9	ANALOG INPUT, CHANNEL 2	24	ANALOG INPUT, CHANNEL 11
10	ANALOG INPUT, CHANNEL 1	23	ANALOG INPUT, CHANNEL 12
11	ANALOG INPUT, CHANNEL 0	22	ANALOG INPUT, CHANNEL 13
12	HOLD CAPACITOR	21	+15V
13	$\overline{\text{SAMPLE}}$/HOLD COMMAND	20	−15V
14	OFFSET ADJUST	19	ANALOG INPUT, CHANNEL 14
15	OFFSET ADJUST	18	ANALOG INPUT, CHANNEL 15
16	ANALOG OUTPUT	17	ANALOG GROUND

ABSOLUTE MAXIMUM RATING

+V, Digital Supply ..... +5.5V
+V, Analog Supply* ..... +16V
−V, Analog Supply ..... −16V
V_{IN}, Signal ..... ±V, Analog Supply
V_{IN}, Digital ..... 0 to +V, Digital Supply
A_{GND} to D_{GND} ..... ±1V

* +V Analog Supply must remain ≥ +V Digital Supply



APPLICATIONS INFORMATION

INPUTS

The HS 362 has two 8-channel multiplexers as input elements. The output of these multiplexers are connected via analog switches to a differential amplifier. One unique feature of the HS 362 is that the internal analog switches can be controlled externally by a digital signal that configures the multiplexer output between single-ended and differential modes. This feature allows the user to select either of these input configuration modes without external hard-wire interconnections. See Table 1.

$\overline{SE}$/DIFF MODE SELECT (PIN 1)	TTL LOGIC INPUT	MUX CONFIGURATION
	0	Single-ended, 16-channels
	1	Differential, 8-channels

Table 1. $\overline{SE}$/DIFF Mode Select Truth Table

MULTIPLEXER ADDRESSING

Multiplexer channels are addressed by means of a level-triggered latch. A logic '1' applied to $\overline{CHANNEL\ LATCH}$ causes the address signals to feed directly to the multiplexer to select the desired input channel. The address information is held in the address select logic when a '0' is applied to the $\overline{CHANNEL\ LATCH}$ input. Input channel addressing is defined in Table 2. Although the fastest mode of operation involves changing the channel address during the A/D conversion while the sample-and-hold amplifier is in the 'hold' mode, this is not the recommended mode of operation. Latch control logic is shown in Table 3.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table 2. Input Channel Addressing Truth Table

$\overline{CHANNEL\ LATCH}$ INPUTS (PIN 32)	TTL LOGIC INPUT	INPUT ADDRESS
	1	Address Passes To MUX
	0	Address Latched

Table 3. $\overline{CHANNEL\ LATCH}$ Truth Table

SAMPLE-AND-HOLD

The sample-and-hold circuitry of the HS 362 is an improvement over other designs. Specifically, it offers a smaller hold step, faster acquisition and hold mode settling times, and lower noise in hold mode to improve system performance. A logic "1" on the $\overline{SAMPLE}$/HOLD command input causes the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally, the $\overline{SAMPLE}$/HOLD command is connected to the ADC status output which is at logic "1" during conversions and logic "0" between conversions. For slowly changing inputs, throughput speed may be increased by grounding the $\overline{SAMPLE}$/HOLD command input and eliminating the hold capacitor.

A 2000 pf polystyrene hold capacitor is provided with each HS 362K. A 2000 pf teflon hold capacitor is provided with each HS 362S and HS 362SB. Use of this external hold capacitor ensures optimum performance with respect to sample-to-hold step size and dielectric absorption effects. Smaller hold capacitors may be used for somewhat faster acquisition times with some penalty paid in a larger sample-to-hold step (see Figs. 1 and 2).

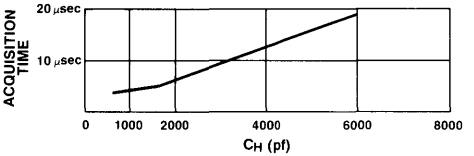


Figure 1. Acquisition Time Vs. Hold Cap (20V Step to .01%)

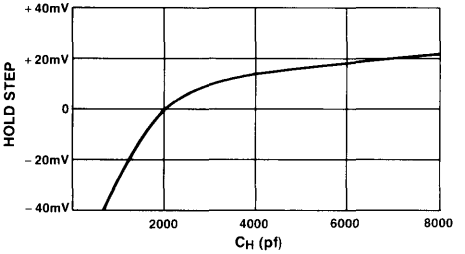


Figure 2. Typical Hold Step Vs. Hold Cap

The hold capacitor is connected between pins 12 and 17. If an alternate capacitor is used, the designer must consider the errors that will be introduced.
CAUTION: Polystyrene capacitors will be damaged if subjected to temperatures above +85°C.

OFFSET ADJUSTMENT

When the HS 362 is used with an ADC, normally the system offset is adjusted at the ADC. However, an offset adjustment for the HS 362 is provided. Refer to Figure 3 for offset adjustment connections.

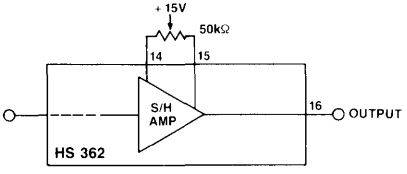


Figure 3. HS 362 Offset Voltage Adjustment

ADC INTERFACE

The HS 362 is designed to be coupled with a precision ADC forming a complete data acquisition system (DAS). This generalized connection is shown in Fig. 4.

APPLICATIONS INFORMATION (Continued)

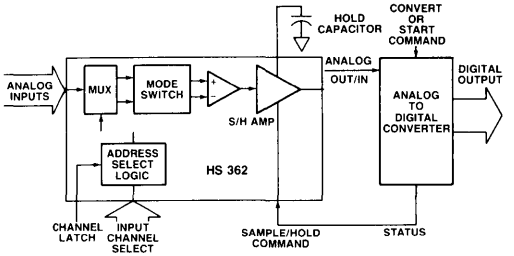
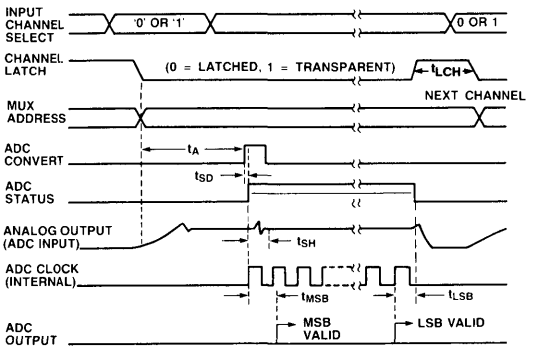


Figure 4. Data Acquisition

Timing of the DAS system (Fig. 4) is shown in Fig. 5. This configuration assumes the following important considerations:

1. Input channel is not changed during a conversion.
2. The MSB decision should not occur until after the S/H amplifier has settled in HOLD mode (t_{SH}).
3. The LSB decision must be made prior to STATUS going low ($t_{LSB} \geq 0$).

The S/H amplifier transient during the sample-to-hold transition is shown in Figure 6.



SYMBOL	PARAMETER	
t_A =	Acquisition time, includes MUX and sample/hold amplifier settling	7μs typ, 10μs max
t_{SH} =	Sample to Hold settling	600ns typ
t_C =	Conversion time	depends on ADC
t_{MSB} =	MSB delay from STATUS	$\geq t_{SH}$
t_{SD} =	Delay of STATUS from ADC CONV	depends on ADC
t_{LSB} =	Time from LSB decision to STATUS low	≤ 0
t_{LCH} =	Minimum pulse width	20 nanoseconds (min, room)
Data set up time for t_{LCH}		20 nanoseconds (min, room)

NOTES:
1. Input address shown is recommended to be 'latched' during A/D conversion cycle.
2. The MSB decision should not occur until after the S/H amplifier has settled in HOLD mode (t_{SH}).
3. LSB decision must be made prior to STATUS going low ($t_{LSB} \geq 0$).

Figure 5. Data Acquisition System Timing

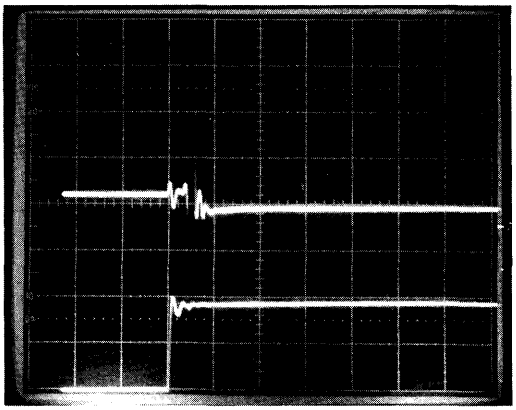


Figure 6. Sample-to-Hold Step (Top), HOLD Command (Bottom) Scale: 20mV/div, vertical; 500 ns/div, horizontal

POWER SUPPLY CONSIDERATIONS

Analog and digital ground lines should be separated to prevent induced spurious signals being introduced into the system. Analog and digital grounds are not connected internally to the HS 362. These must be connected externally by the user. The choice of an optimum 'star' point is an important consideration in the system layout. Grounds should be arranged to avoid loops and to minimize the coupling of voltage drop to sensitive analog sections. A suggested grounding approach is shown in Fig. 7.

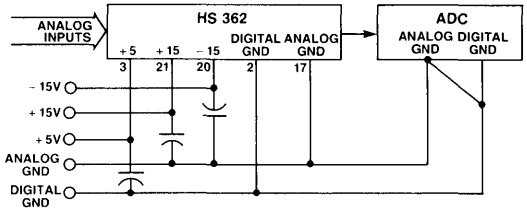


Figure 7. Power Supply and Grounding Connections

In this example the system ground has been chosen to be located at the ADC for optimum performance. Should the grounds be connected at a different point in the system then back-to-back diodes (1N914 or equivalent) are recommended to prevent potential variations between the grounds from exceeding ±1 volt. The HS 362 will function properly with as much as ±200mV between grounds.

Power leads should be bypassed to ground as shown in Fig. 7. Either 1μf tantalum or 0.1μf ceramic capacitors are recommended.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	DESCRIPTION
HS 362K	0 to 70°C	Precision 16-channel
HS 362S	−55°C to +125°C	data acquisition system
HS 362SB*	−55°C to +125°C	analog input section.

*Processed to MIL-STD-883C.

Specifications subject to change without notice.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

HS9403

16-CHANNEL, 12-BIT DATA ACQUISITION SYSTEM

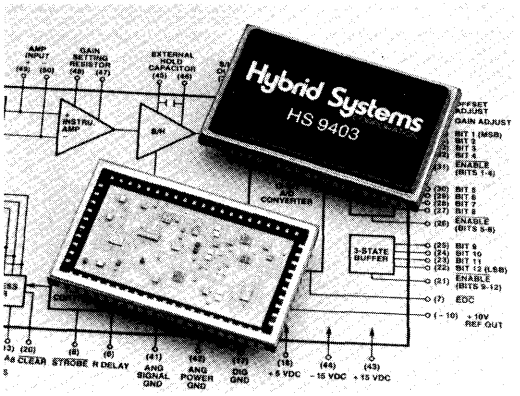
FEATURES

- Multiplexer, instrumentation amp, S/H, A/D and control logic in a 62-pin package
- Three state output buffer
- Instrumentation amp with selectable gain ranging 1 to 1000
- Single-ended (−16) and differential (−8) inputs
- 50 kHz minimum throughput

DESCRIPTION

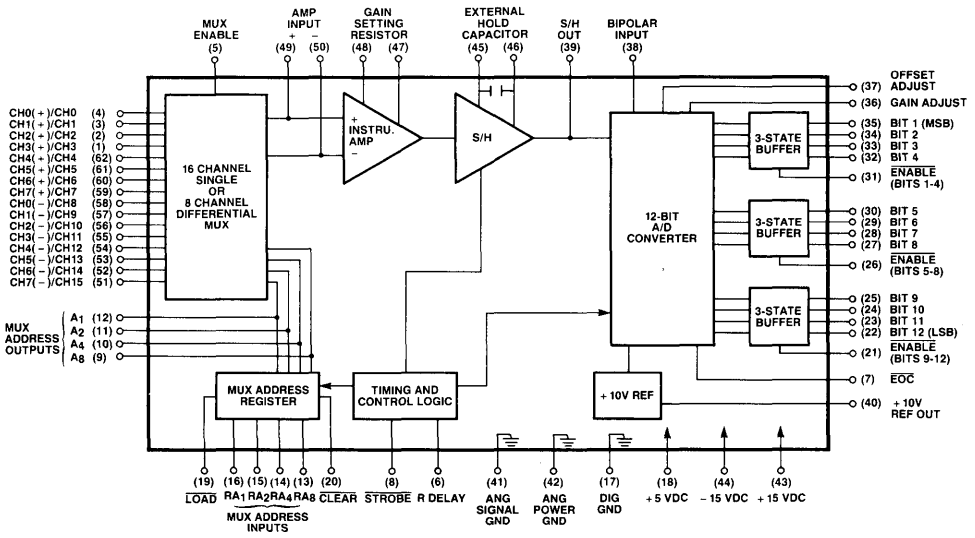
The HS9403-8 and 9403-16 provide complete 12-bit data acquisition functionality in a single, 62-pin package. The 9403 includes 8- or 16-channel multiplexing, a programmable gain instrumentation amplifier, sample-hold circuit, 10V buffered reference, 12-bit 10μsec A/D and three-state output buffers.

The 9403 is flexible enough to accept full scale input ranges from ± 10 mV to ± 10V. Three-state output buffers allow output data to be accessed in any combination of three 4-bit bytes. Expansion to 32 single-ended or 16 differential inputs can be achieved with the addition of only 2 ICs.



The 9403 is packaged in a 62-pin, hermetically-sealed, ceramic package. Temperature ranges available are 0°C to 70°C for commercial versions and −55°C to 125°C with MIL-STD-883C screening for military grades.

FUNCTIONAL DIAGRAM



11

SPECIFICATIONS

(Typical @ +25°C and nominal power supplies unless otherwise specified)

ANALOG INPUTS	HS 9403
Number of Input Channels	
HS 9403-8	8 Differential
HS 9403-16	16 Single-Ended
Input Voltage Range[1]	
Unipolar	0 to +10V
Bipolar	±10V
Common Mode Voltage Range	±11V min
CMRR	
G = 1 (1 kHz)	74 dB
G = 1000 (60 Hz)	110 dB
Input Bias Current	±50 pA typ
Bias Current Drift	Doubles every 10°C
Input Offset Current	±25 pA typ, ±100 pA max
Offset Current Drift	Doubles every 10°C
Input Offset Voltage	±2 mV
Offset Voltage Drift	(20 + 7G)μV/°C
Voltage Noise (RTI)[2]	
G = 1	150 μV (RMS)[3]
G = 1000	1.6 μV (RMS)[3]
Input Resistance	10^{12}
Input Capacitance	
OFF Channel	10 pF
ON Channel 9403-8	50 pF
9403-16	100 pF

DIGITAL INPUTS	
Logic Levels	
Logic "1"	+2V min, +5.3V max
Logic "0"	−0.3V min, +0.8V max
Logic Loading	
Logic "1"	20 μA
Logic "0"	-0.2 mA

STATIC PERFORMANCE[4]	
No Missing Codes	Guaranteed over operating temperature range
Integral Linearity Error	±¼ LSB typ, ±½ LSB max
Differential Linearity Error	±¼ LSB typ, ±½ LSB max
Unipolar Offset Error[5]	±0.025% FSR typ, ±0.1% FSR[6] max
Bipolar Zero Error[5]	±0.025% FSR typ, ±0.1% FSR[6] max
Gain Error[5]	±0.025% typ, ±0.2% max

+10V REFERENCE	
Output Voltage	+10.000V ±10 mV
Output Voltage Drift	±3 ppm/°C typ, ±8 ppm/°C max

DYNAMIC PERFORMANCE	
Throughput Rate	50 kHz min
S/H Acquisition Time[7]	9 μsec typ, 10 μsec max
A/D Conversion Time	10 μsec max
Aperture Delay	25 nsec typ
Sample-Hold Droop	0.1 μV/μsec
Feedthrough (@ 1 kHz)[8]	±0.01% max
MUX Crosstalk (@ 1 kHz)	−80 dB min
Strobe Command Pulse Width	40 nsec min
Setup Time Digital Inputs to Strobe[9]	50 nsec min
Hold Time Digital Inputs from Strobe[9]	50 nsec max
$\overline{\text{ENABLE}}$	
Tri State to Valid	40 nsec max
Valid to Tri State	30 nsec max

DRIFT CHARACTERISTICS[10]	
Integral Linearity	±1 ppm/°C typ, ±2 ppm/°C max
Differential Linearity	±1 ppm/°C typ, ±2 ppm/°C max
Unipolar Offset	±3 ppm/°C typ, ±7 ppm/°C max
Bipolar Zero	±3 ppm/°C typ, ±10 ppm/°C max
Gain	±8 ppm/°C typ. ±20 ppm/°C max

DIGITAL OUTPUTS	
Logic Levels	
Logic "1"	2.4V min
Logic "0"	0.4V max
Logic Coding	
Unipolar Ranges	Straight binary
Bipolar Ranges	Offset binary
Fanout	5 TTL Loads

POWER SUPPLIES	
Power Supply Range	
±15V	±14.5V to ±15.5V
+5V	+4.5V to +5.5V
Current Drains	
+15V	55 mA typ, 55 mA max
−15V	68 mA typ, 60 mA max
+5V	32 mA typ, 45 mA max
Power Dissipation	1.4W typ, 2.0W max
P.S.R.R. for 3 supplies	0.005%/% max
P.S.R.R. (+10V ref)	0.01%/% max

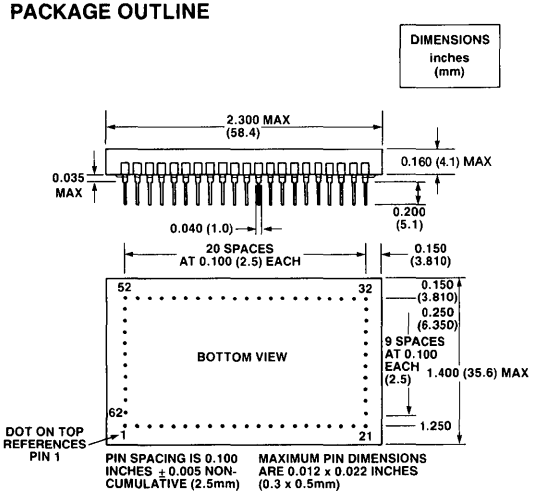
TEMPERATURE RANGE	
Operating C-Option	0°C to +70°C
Operating B-Option	−55°C to +125°C
Storage	−65°C to +150°C

ABSOLUTE MAXIMUM RATINGS	
$+V_{CC}$	−0.5V to +18V
$-V_{CC}$	+0.5V to −18V
V_{DD}	−0.3 to +7V
Analog Input Channels	±35V
Digital Inputs	−0.3 to V_{DD} +0.3V

NOTES:

1. For unity gain.
2. Referred to input.
3. Measured at output of S/H.
4. Specifications refer to entire system from MUX input to A/D output with instrumentation amplifier G = 1.
5. Initial offset and gain errors are adjustable to zero with optional external potentiometers.
6. FSR = full scale range. Unipolar FSR = 10V, Bipolar FSR = 20V. For a 12-bit system, 1 LSB = 0.024% FSR.
7. Includes MUX switching and settling time, instrumentation amp unity gain settling time and S/H acquisition time. Specified for 10V step settling to 0.01% FSR.
8. Measured at S/H output with S/H in hold mode.
9. Includes MUX address, MUX enable, clear and load inputs.
10. Unipolar 10V FSR is the basis for parts per million specifications.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN NO.	FUNCTION HS 9403-16	FUNCTION HS 9403-8
1	CH3 IN	CH3(+)IN
2	CH2 IN	CH2(+)IN
3	CH1 IN	CH1(+)IN
4	CH0 IN	CH0(+)IN
5	MUX ENABLE	
6	R DELAY	
7	$\overline{EOC}$	
8	$\overline{STROBE}$	
9	A8	
10	A4 MUX ADDRESS OUT	
11	A2	
12	A1	
13	RA8	
14	RA4 MUX ADDRESS IN	
15	RA2	
16	RA1	
17	DIGITAL GROUND	
18	+5V	
19	$\overline{LOAD}$ ENABLE	
20	$\overline{CLEAR}$ ENABLE	
21	$\overline{ENABLE}$ (BITS 9-12)	
22	BIT 12 OUT (LSB)	
23	BIT 11 OUT	
24	BIT 10 OUT	
25	BIT 9 OUT	
26	$\overline{ENABLE}$ (BITS 5-8)	
27	BIT 8 OUT	
28	BIT 7 OUT	
29	BIT 6 OUT	
30	BIT 5 OUT	
31	$\overline{ENABLE}$ (BITS 1-4)	
32	BIT 4 OUT	
33	BIT 3 OUT	
34	BIT 2 OUT	
35	BIT 1 OUT (MSB)	
36	GAIN ADJ	
37	OFFSET ADJ	
38	BIPOLAR INPUT	
39	SAMPLE/HOLD OUT	
40	+10V REFERENCE OUT	
41	ANALOG SIGNAL GROUND	
42	ANALOG POWER GROUND	
43	+15V	
44	−15V	
45	EXTERNAL HOLD CAP HIGH	
46	EXTERNAL HOLD CAP LOW	
47	R GAIN LOW	
48	R GAIN HIGH	
49	INSTRU. AMP (+) INPUT	
50	INSTRU. AMP (−) INPUT	
51	CH15 IN	CH7(−)IN
52	CH14 IN	CH6(−)IN
53	CH13 IN	CH5(−)IN
54	CH12 IN	CH4(−)IN
55	CH11 IN	CH3(−)IN
56	CH10 IN	CH2(−)IN
57	CH9 IN	CH1(−)IN
58	CH8 IN	CH0(−)IN
59	CH7 IN	CH7(+)IN
60	CH6 IN	CH6(+)IN
61	CH5 IN	CH5(+)IN
62	CH4 IN	CH4(+)IN

DIGITAL PIN FUNCTIONS

FUNCTION	PIN NO.	LOGIC STATE	DESCRIPTION
MUX ENABLE	5	"0"	Disables internal MUX
		"1"	Enables internal MUX
$\overline{EOC}$	7	"0"	Signal acquisition cycle in progress
		"1"	A/D conversion in progress
		"1" to "0"	Conversion complete
$\overline{STROBE}$	8	"1" to "0"	Initiates acquisition and conversion of analog signal
MUX ADDRESS OUT	9-12		Output of MUX address register. Straight binary coding
MUX ADDRESS IN	13-16		Selects MUX for random address mode. Straight binary coding
$\overline{LOAD}$	19	"0"	Random address mode initiated on falling edge of $\overline{STROBE}$
		"1"	Sequential address mode
$\overline{CLEAR}$	20	"0"	Forces MUX address to CH0 on next falling edge of $\overline{STROBE}$ regardless of $\overline{LOAD}$ and MUX address inputs
$\overline{ENABLE}$ (BITS 9-12)	21	"0"	Enables three-state outputs bits 9-12
		"1"	Disables three-state outputs bits 9-12
$\overline{ENABLE}$ (BITS 5-8)	26	"0"	Enables three-state outputs bits 5-8
		"1"	Disables three-state outputs bits 5-8
$\overline{ENABLE}$ (BITS 1-4)	31	"0"	Enables three-state outputs outputs bits 1-4
		"1"	Disables three-state outputs bits 1-4

ANALOG PIN FUNCTIONS

FUNCTION	PIN NO.	DESCRIPTION
R DELAY	6	Connect external resistor to lengthen S/H acquisition time when instrumentation AMP is set for high gain (for normal operation, R DELAY tied to +5V).
GAIN ADJUST	36	External gain adjust (optional)
OFFSET ADJUST	37	External offset adjust (optional)
BIPOLAR INPUT	38	For unipolar operation (0 to +10V), connect to pin 39 (S/H OUT). For Bipolar operation (±10V), connect to pin 40 (+10V REF OUT)
S/H OUTPUT	39	Sample-Hold output
+10V REF OUT	40	Buffered +10V reference output
EXTERNAL HOLD CAPACITOR	45, 46	Add external polypropylene, polystyrene or teflon hold capacitor to improve S/H droop rate (optional)
R GAIN	47, 48	Optional gain selection point. R = 20k/(G − 1). Leave open for G = 1
INSTRUMENTATION AMP INPUTS	49, 50	Use when adding additional external multiplexers for expanded single-ended or differential operation (see Applications Information). Connect pin 50 to analog common for HS 9403-16

APPLICATIONS INFORMATION

NOTES:

1. Input channels are protected to 20V beyond power supplies.
2. To improve sample-hold droop rate, an external hold capacitor may be connected between external hold cap pins 45 and 46. Polypropylene or teflon capacitors are recommended for best results. Acquisition time must be increased accordingly.
3. $\text{R GAIN } (\Omega) = \dfrac{20{,}000}{(\text{GAIN} - 1)}$ $(\pm 0.1\%$ typical)
4. To increase acquisition time allotment, connect a resistor from R DELAY (pin 6) to +5V (pin 18).

$$\text{R DELAY } (\Omega) = \frac{\text{AMP settling time}}{10^{-9}} - 9\text{K (see Table 1)}$$

INPUT RANGE	GAIN	R GAIN (R)	AMP SETTLING TIME	R DELAY	THROUGHPUT	SYSTEM ACCURACY
±10V	1	None	9 μsec	None	55.5 kHz	0.009%
±5V	2	20.0k	9 μsec	None	55.5 kHz	0.009%
±2.5V	4	6.667k	9 μsec	None	55.5 kHz	0.009%
±1V	10	2.222k	9 μsec	None	55.5 kHz	0.009%
±200 mV	50	408.2	16 μsec	7K	40.0 kHz	0.010%
±100 mV	100	202.0	30 μsec	21K	25.6 kHz	0.011%
± 50 mV	200	100.5	60 μsec	51K	14.5 kHz	0.016%
± 20 mV	500	40.08	144 μsec	135K	6.5 kHz	0.035%
± 10 mV	1000	20.02	288 μsec	279K	3.3 kHz	0.069%

Table 1. Input Range Parameters

MUX CHANNEL ADDRESSING

The HS 9403-8 and HS 9403-16 are capable of having their input multiplexer channels either randomly or sequentially addressed.

ADDRESS MODE	MUX ENABLE	$\overline{\text{LOAD}}$	$\overline{\text{CLEAR}}$	ADDRESS INPUTS	ADDRESS OUTPUTS	$\overline{\text{STROBE}}$
Random	1	0	1	Next channel	On channel	"1" to "0"
Sequential	1	1	1	Don't care	On channel	"1" to "0"
Free-Running Sequential	1	1	1	Don't care	On channel	"1" to "0"

Table 2.

RANDOM ADDRESS

Set $\overline{\text{LOAD}}$ (pin 19) to LOGIC "0". The next falling edge of $\overline{\text{STROBE}}$ will load the MUX channel address present on pin 13 to pin 16. Address inputs must be stable 50 nsec before and after falling edge of $\overline{\text{STROBE}}$ pulse.

TRIGGERED SEQUENTIAL ADDRESS

Set $\overline{\text{LOAD}}$ (pin 19) and $\overline{\text{CLEAR}}$ (pin 20) to LOGIC "1". Applying a falling edge trigger pulse to $\overline{\text{STROBE}}$ (pin 8). This negative transition causes the contents of the address counter to increment by one followed by a sample-hold acquisition and A/D conversion. Changing digital data appearing at the address inputs will not affect the HS 9403 when it is in the sequential address mode.

FREE-RUNNING SEQUENTIAL ADDRESS

Set $\overline{\text{LOAD}}$ (pin 19) and $\overline{\text{CLEAR}}$ (pin 20) to LOGIC "1" Connect $\overline{\text{EOC}}$ (pin 7) and $\overline{\text{STROBE}}$ (pin 8) together. The falling edge of $\overline{\text{EOC}}$ will increment channel address. When the $\overline{\text{EOC}}$ goes low, the digital output data is valid for the previous channel for approximately 10 sec while the multiplexer is switching channels and the S/H is acquiring the new signal.

VALID OUTPUT

During the conversion ($\overline{\text{EOC}}$ high), the output of the A/D is changing during the successive approximation sequence. If the outputs are connected to a Data Bus, the enable inputs (pins 21, 26 and 31) must be held high to prevent invalid data from reaching the bus. If data is to be read immediately after conversion is completed, connect $\overline{\text{EOC}}$ to $\overline{\text{ENABLE}}$ (bits 1-4), $\overline{\text{ENABLE}}$ (bits 5-8) and $\overline{\text{ENABLE}}$ (bits 9-12), pins 21, 26 and 31. This will tri-state the outputs during conversion and enable them during the acquisition period.

ADDRESS INPUTS				MUX ENABLE	CHANNEL SELECTED	
A8	A4	A2	A1			
X	X	X	X	0	None	
0	0	0	0	1	0	
0	0	0	1	1	1	
0	0	1	0	1	2	
0	0	1	1	1	3	
0	1	0	0	1	4	
0	1	0	1	1	5	
0	1	1	0	1	6	
0	1	1	1	1	7	HS 9403-8
1	0	0	0	1	8	
1	0	0	1	1	9	
1	0	1	0	1	10	
1	0	1	1	1	11	
1	1	0	0	1	12	
1	1	0	1	1	13	
1	1	1	0	1	14	
1	1	1	1	1	15	HS 9403-16

Table 3. MUX Channel Addressing

APPLICATIONS INFORMATION (continued)

INPUT EXPANSION

The HS 9403 can be easily expanded to 32 single-ended channels or 16 differential channels. When extending channel capacity, the multiplexer settling time must be extended through the use of R DELAY (pin 6).

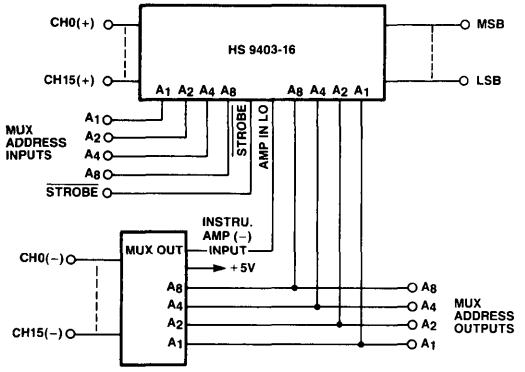


Figure 2. 16-Channel Differential Input Expansion

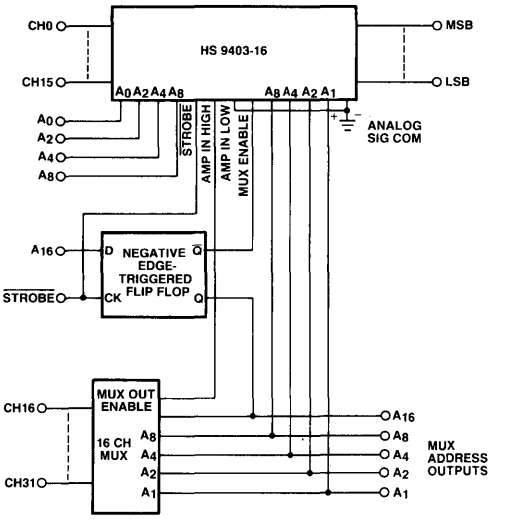


Figure 3. 32-Channel Single-Ended Input Expansion

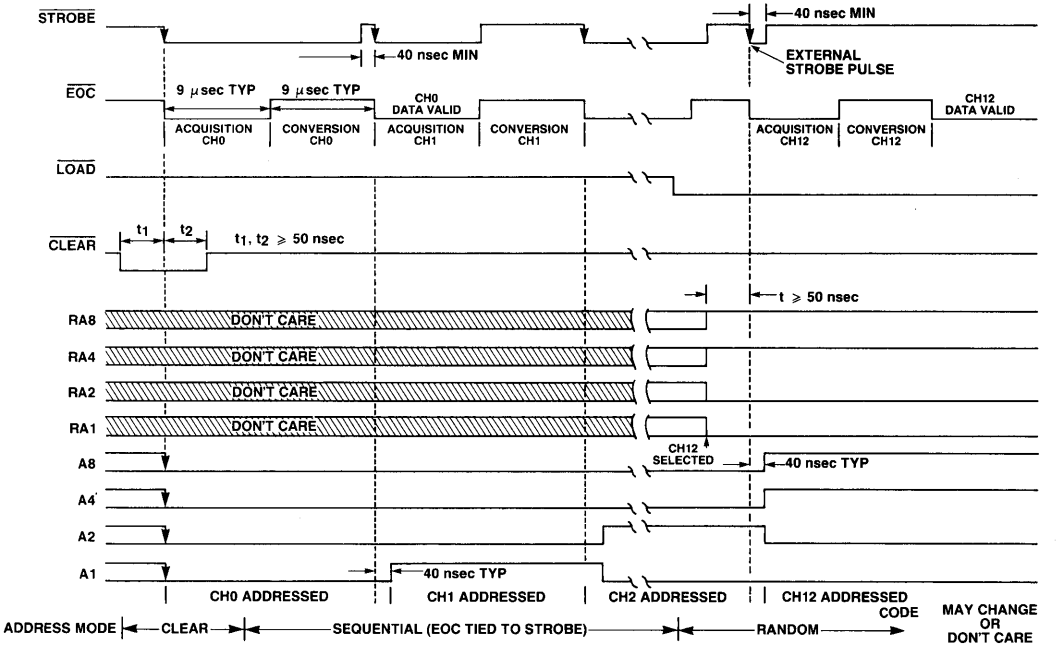
ORDERING INFORMATION

MODEL NUMBER	TEMPERATURE RANGE	DESCRIPTION
HS 9403C-8	0°C to +70°C	8 differential input, 12-bit, data acqusition system (DAS)
HS 9403C-16	0°C to +70°C	16 single-ended input, 12-bit, DAS
HS 9403B-8	-55°C to +125°C	8 differential input, 12-bit, DAS MIL-STD-883C
HS 9403B-16	-55°C to +125°C	16 single-ended input, 12-bit, DAS MIL-STD-883C
HS 9403C-16 FP	0°C to +70°C	16 single-ended input in flat pack
HS 9403B-16 FP	-55°C to +125°C	16 single-ended input, in flat pack, MIL-STD-883C

Specifications subject to change without notice

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below – volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

TIMING DIAGRAM



OFFSET AND GAIN ADJUST CONNECTIONS

The HS 9403 offset and gain adjustments may be made by connecting two 20K trim potentiometers as shown below:

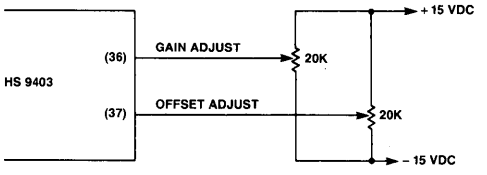


Figure 1. Offset and Gain Adjust Connections

Offset Adjustment — Connect the OFFSET potentiometer as shown above and apply an analog input voltage equivalent to +½ LSB if operating in a unipolar mode or −FS +½ LSB if operating in a bipolar mode. While performing repeated conversions, adjust the offset potentiometer down until all output bits are "0". Then adjust up until the LSB just turns to a "1"

Gain Adjust — Connect the gain potentiometer as shown and apply an analog input voltage equivalent to +FS −1½ LSB. While performing repeated conversions, adjust the gain potentiometer up until all the output bits are "1". Then adjust down until the LSB just turns to "0".

NOTE:
Since the offset adjustments effects the gain of the system, offset voltage must be adjusted first.

DIGITAL OUTPUT CODING

	UNIPOLAR 0 to +10V	0 to +5V	STRAIGHT BINARY		
+FS −1 LSB	+ 9.9976	+4.9988	1111	1111	1111
+½ FS	+ 5.0000	+2.5000	1000	0000	0000
+1 LSB	+ 0.0024	+0.0012	0000	0000	0001
ZERO	0.0000	0.0000	0000	0000	0000
	BIPOLAR ±10V	**±5V**	**OFFSET BINARY**		
+FS −1 LSB	+ 9.9951	+4.9976	1111	1111	1111
+½ FS	+ 5.0000	+2.5000	1100	0000	0000
+1 LSB	+ 0.0049	+0.0024	1000	0000	0001
ZERO	0.0000	0.0000	1000	0000	0000
−FS +1 LSB	− 9.9951	−4.9976	0000	0000	0001
−FS	−10.000	−5.0000	0000	0000	0000

GROUNDING CONSIDERATIONS

The HS 9403 brings out separate pins for analog power ground, analog signal grounds, and digital ground. All three should be connected together as close to the unit as possible and connected to system analog ground. If the ground pins cannot be connected directly at the package, wide low resistive ground lines should be used and a non-polarized capacitor (0.1 to 1 μF) should be connected between analog and digital ground directly at the package.

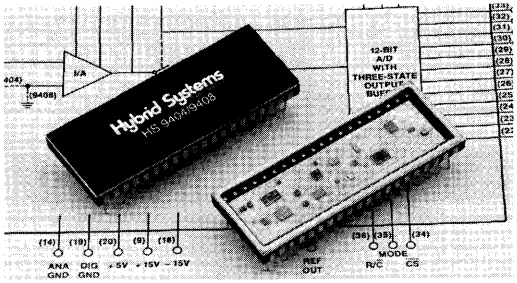
Internal 0.01 μF ceramic decoupling capacitors are used in the device. However, it is advisable to add a 1 μF or 10 μF tantalum capacitor to each power supply pin from the central ground point to minimize power supply noise problems.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

8-CHANNEL, 12-BIT DATA ACQUISITION SYSTEM (DAS)

FEATURES

- Complete 12-bit DAS
  - 8-channel multiplexer
  - Instrumentation amp with programmable gain
  - Sample/hold circuit
  - 12-bit A/D
  - 3-state output buffer
- 40 pin DIP
- 35 kHz throughput
- Low power



DESCRIPTION

The HS9404 and HS9408 are compact, single-package solutions to multichannel acquisition applications. These units are complete data acquisition systems which include input multiplexing, instrumentation amplifier with programmable gain, sample and hold circuit, 12-bit A/D converter, and control logic. Accuracy and linearity are specified for the complete system from analog input to digital output. The need for ordinary component specifications such as instrumentation amp linearity, gain accuracy, and sample-hold pedestal error are eliminated, as they are guaranteed in system specifications.

The HS9404 offers four differential inputs while the HS9408 provides eight single-ended inputs. Both devices feature overvoltage input protection (to ±35V) and the instrumentation amp provides gain ranges of 1 to 100*. The gain range is selected through the use of a single external resistor and allows a variable input range of ± 100 mV to ± 10V.

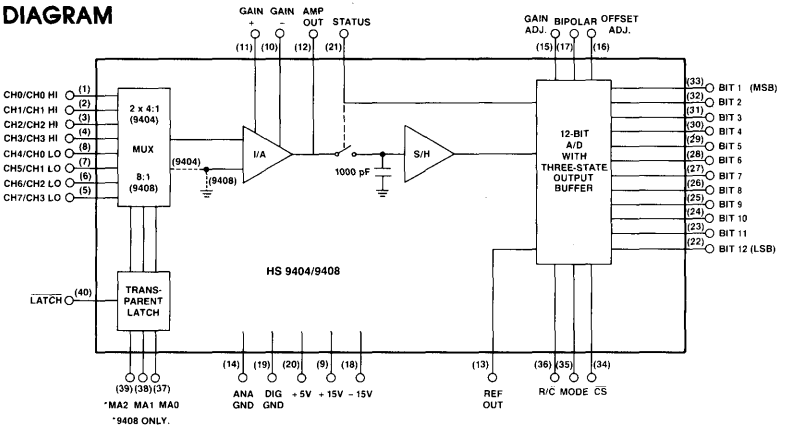
Expansion to seven differential or fifteen single-ended inputs is easily accomplished with two additional ICs.

Total system linearity is specified as ± ½ LSB at 25°C and ± ¾ LSB is guaranteed over the military operating temperature range. System throughput rates of up to 35 kHz can be achieved, while a three-state output buffer permits easy interface with a microprocessor bus.

The HS9404 and HS9408 operate from ± 15V and +5V with a total power dissipation of 655 mW and 650 mW respectively. Both models are offered in 40-pin ceramic packages and are specified for operation from 0°C to 70°C for commercial grades and −55°C to +125°C with MIL-STD-883 Rev. C, Levels B or S screening for military grades.

*Gain can be set to higher values but operation to 12-bit accuracy is not guaranteed.

FUNCTIONAL DIAGRAM



11

SPECIFICATIONS

(Typical @ +25°C and nominal power supplies unless otherwise specified)

ANALOG INPUTS

Number of Inputs	
HS 9404	4 Differential
HS 9408	8 Single-Ended
Input Voltage Range[3]	
Unipolar	0 to +10V
Bipolar	±10V or ±5V[1]
Common Mode Voltage Range	±10V
CMRR[2]	
G = 1 @ 200 Hz, Vcm = 20 Vpp	90 dB
Input Bias Current	
+25°C	±15 nA typ, ±100 nA max
−55°C to +125°C	±200 nA (max)
Input Resistance	$10^{12}\Omega$ typ
Input Capacitance	
OFF Channel	5 pF
ON Channel 9404	10 pF
9408	10 pF
Gain Equation (A_V)	$\frac{20K}{R_G} + 1$

DIGITAL INPUTS (t_{MIN} to t_{MAX})

Logic Levels (R/C, MODE, CS)	
Logic "1"	2.4V min
Logic "0"	0.8V max
Logic Loading	1 LSTTL load max

STATIC PERFORMANCE[3]

Integral Nonlinearity[5] (K)	±½ LSB over temperature
(T)	±¾ LSB over temperature
(S,J)	± 1 LSB over temperature
Differential Nonlinearity (T,K)	±1 LSB over temperature
(S,J)	±2 LSB over temperature
No Missing Codes (T,K)	12 bits over temperature
(S,J)	11 bits over temperature
Unipolar Offset Error[3,4]	±0.05% max
Bipolar Minus Full Scale Error[3,4]	±0.05% typ, ±0.1% max
Gain Error[4]	±0.1% typ, ±0.3% max
Channel to Channel Offset Voltage	1 mV max

DYNAMIC PERFORMANCE

Throughput Rate:	
Gain = 1	35 kHz
Gain = 10	28 kHz
Gain = 100	15 kHz
System Acquisition Time (20V step, 0.01%) to A/D Input	3.5 μ sec typ, 10 μ sec max[3]
A/D Conversion Time	20 μ sec typ, 25 μ sec max
S/H Feedthrough Attenuation	90 dB
MUX Crosstalk Attenuation (off isolation)	68 dB
t Settling, MUX IN to AMP OUT (0.01%)	
Gain = 1	2.5 μ sec
Gain = 10	10 μ sec
Gain = 100	40 μ sec
Slew Rate, AMP OUT	13V/μsec
Adjacent Channel Coupling Error[7] (V_{IN} = 20 Vp-p sine wave)	−78 dB @ 40 kHz −90 dB @ 0.5 kHz

DRIFT CHARACTERISTICS

Integral Nonlinearity	±2 ppm/°C
Differential Nonlinearity	±2 ppm/°C
Unipolar Offset[6]	±10 ppm/°C
Bipolar Zero[6]	±10 ppm/°C
Gain[6]	±25 ppm/°C

DIGITAL OUTPUTS

Logic Levels	
Logic "1"	2.4V min
Logic "0"	0.4V max
Leakage	±5 μA max
Logic Coding	
Unipolar Range	Straight binary
Bipolar Range	Offset binary

POWER SUPPLIES

Power Supply Range	±15V, ±5% 5V, ±5%	
PSRR (all supplies)	0.002%/% typ, 0.005%/% max	
Current Drain	HS 9404	HS 9408
+15V	27 mA	22 mA
−15V	15 mA	18 mA
+5V	5 mA	10 mA
Power Dissipation	655 mW	650 mW

TEMPERATURE RANGE

Operating (J,K)	0°C to +70°C
Operating (S,T)	−55°C to +125°C
Storage	−65°C to +150°C

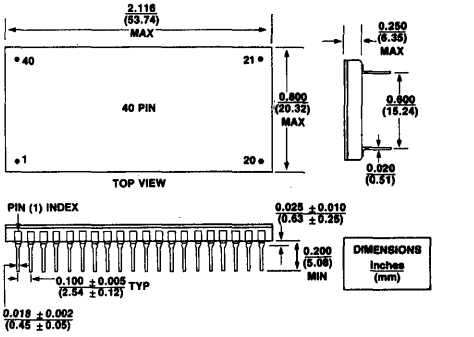
PACKAGE

Weight	15 grams

NOTES:

1. Input range selected at factory.
2. HS 9404 only.
3. Unity gain configured.
4. Adjustable to zero; see application notes.
5. End point definition.
6. Gain and offset drift specifications as stated in data sheet are maximum (average) limits over the given temperature range, tested at temperature end points.
7. For best performance above 1 kHz, connect package lid to analog ground.

PACKAGE OUTLINE



NOTE: Initial commercial offerings will be in ceramic with future offerings in plastic.

PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	CH0/CH0 HI	40	$\overline{\text{LATCH}}$
2	CH1/CH1 HI	39	MA2*
3	CH2/CH2 HI	38	MA1
4	CH3/CH3 HI	37	MA0
5	CH7/CH3 LO	36	R/$\overline{\text{C}}$
6	CH6/CH2 LO	35	MODE
7	CH5/CH1 LO	34	$\overline{\text{CS}}$
8	CH4/CH0 LO	33	BIT 1 (MSB)
9	+15V	32	BIT 2
10	GAIN (−)	31	BIT 3
11	GAIN (+)	30	BIT 4
12	AMP OUT	29	BIT 5
13	REF OUT	28	BIT 6
14	ANALOG GND	27	BIT 7
15	GAIN ADJ	26	BIT 8
16	OFFSET ADJ	25	BIT 9
17	BIPOLAR	24	BIT 10
18	−15V	23	BIT 11
19	DIGITAL GND	22	BIT 12 (LSB)
20	+5V	21	STATUS

*HS 9408 only.

ABSOLUTE MAXIMUM RATINGS (HS 9404/HS 9408)

+15V (+V_{DD})	+16.5V
−15V (−V_{DD})	−16.5V
+5V (+V_{CC})	+7V
Analog GND to Digital GND	±0.5V
Digital Inputs to Digital GND	+5.5V max −0.5V min
Analog Inputs to Analog GND	
Pins 1 through 8	±35V
Pins 10, 11, 15, 16, 17	±V_{DD}
Amp Out to Analog or Digital GND	Indefinite short circuit
REF OUT to Analog or Digital GND to ±V_{DD}	Indefinite short circuit 100 ms short circuit
Voltage on Digital Ouputs in Tri-State Mode	+V_{CC} +0.5V max −0.5V min
Lead Temperature, Soldering	300°C, 10 sec

APPLICATIONS INFORMATION

CONTROL FUNCTIONS

The HS 9404/HS 9408 contains control functions necessary to provide for microprocessor interface. All control functions are defined in Tables 1, 2, and 3.

FUNCTION	DEFINITION	FUNCTION
R/$\overline{C}$	Read/Convert	1. ↓ initiates conversion 2. High (1) initiates read along with $\overline{CS}$ low
$\overline{CS}$	Chip Select	1. High (1) disconnects data bus 2. Low (0) connects data bus, must be low for conversion to start
$\overline{Latch}$	Latch	1. High (1) transparent 2. Low (0) MUX address latched
MA0 MA1 MA2*	Multiplexer Address	Select Channels (see MUX Logic Table 3)
MODE	$\overline{12\text{-bit}}$/8-bit	1. High (1) indicates 8-bit conversion 2. Low (0) indicates 12-bit conversion

*HS 9408 only.

Table 1. Defining the Control Functions

CONTROL INPUTS R/$\overline{C}$	CONTROL INPUTS $\overline{CS}$	OPERATION
↓	0	Initiates conversion
1	1	Output goes to high impedance state
1	0	Initiates read

Table 2. Truth Table — Control Inputs

MUX ADDRESS INPUTS MA2*	MA1	MA0	CHANNEL SELECTED HS 9404	HS 9408
0	0	0	CH0 HI/CH0 LOW	CH0
0	0	1	CH1 HI/CH1 LOW	CH1
0	1	0	CH2 HI/CH2 LOW	CH2
0	1	1	CH3 HI/CH3 LOW	CH3
1	0	0	—	CH4
1	0	1	—	CH5
1	1	0	—	CH6
1	1	1	—	CH7

NOTES:
*Applies to HS 9408 only. $\overline{Latch}$ high allows MUX address to MUX.
$\overline{Latch}$ low latches the address present during low edge and keeps that channel selected.

Table 3. Truth Table — Multiplexer Address

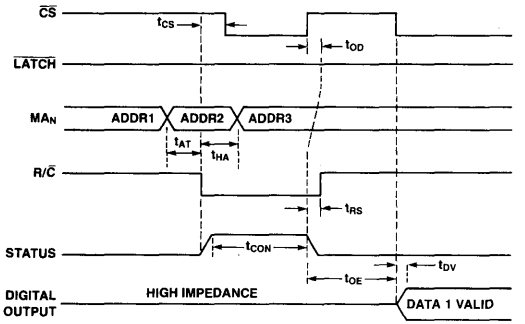
TIMING

The timing diagram in Figure 1 shows how the HS 9404/HS 9408 works when controlled by a microprocessor. The normal sequence of events is as follows:

1. The input signal is acquired by the MUX, AMP and S/H (track mode) after the MUX address is changed.
2. A conversion is initiated by the R/$\overline{C}$ control line going to logic "0". Concurrent with this event, the status line goes to logic "1" to indicate the A/D is "busy". When the A/D is "busy", the S/H is in the hold mode.
3. The A/D indicates completion of the conversion by returning the status line to logic "0".
4. Data is placed on the output bus when the R/C control line is set to logic "1" and when the CS line is set to logic "0".

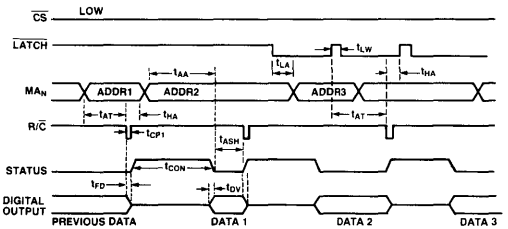
Reference Figure 1 for timing constraints of various operations.

Figure 2 shows the timing requirements for stand-alone operation. The major difference between stand-alone and bus compatible operation is the use of the $\overline{CS}$ control line. Since stand-alone operation does not require the output data to arrive at a specified time, the $\overline{CS}$ line is kept at logic "0". This presents output data immediately after conversion is complete. Reference Figure 2 for timing constraints of various operations.



t_{CS} – CHIP SELECT DELAY TIME – 100 nsec MAX.
t_{OD} – OUTPUT DISABLE DELAY AFTER ↓ OF STATUS – 35 nsec MAX.
t_{AT} – TOTAL ACQUISITION TIME OF MUX, AMP, S/H (TRACK MODE) – SEE SPECIFICATIONS.
t_{HA} – S/H HOLD APERTURE TIME – 500 nsec. (MINIMUM TIME BEFORE SWITCHING MUX ADDRESS)
t_{RS} – READ SETUP TIME – 0 nsec MIN.
t_{OE} – OUTPUT ENABLE SETUP TIME – 0 nsec MIN.
t_{DV} – DATA VALID TIME – 250 nsec.
t_{CON} – CONVERSION TIME OF A/D – 25 μsec (12 BITS) MAX, 19 μsec (8 BITS) MAX

Figure 1. Timing for Bus Compatible DAS



t_{AT} – TOTAL ACQUISITION TIME OF MUX, AMP, S/H (TRACK MODE) – THIS IS THE TIME FROM CHANGING THE ADDRESS TO STARTING A NEW CONVERSION. SEE SPECIFICATIONS.
t_{CP1} – NEGATIVE CONVERT PULSE WIDTH – 50 nsec MIN., 1 μsec MAX.
t_{FD} – OUTPUT FLOAT DELAY TIME – 150 nsec.
t_{CON} – CONVERSION TIME OF A/D – 25 μsec MAX.
t_{HA} – S/H HOLD APERTURE TIME – 500 nsec.
t_{AA} – MUX AND AMP ACQUISITION TIME – SEE SPECIFICATIONS.
t_{ASH} – S/H ACQUISITION TIME – 7 μsec TYP., 10 μsec. MAX..
t_{DV} – DATA VALID TIME – 1000 nsec MAX, 250 nsec MIN.
t_{LA} – $\overline{LATCH}$ TO ADDRESS CHANGE TIME – 30 nsec.
t_{LW} – LATCH PULSE WIDTH – 80 nsec MIN.

Figure 2. Timing for Stand-Alone Operation

OFFSET AND GAIN CONNECTIONS

The DAS is normally used with external offset and gain calibration potentiometers. However, if maximum accuracy is not required, they may be omitted. The offset control has a range of about ±20 LSB, and the gain control has a range of about ±13 LSB.

Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate instruments. The voltage source used as a signal input must be very stable. It also should be capable of being set to within 1/10 LSB at both ends of its range.

The DAS's offset and gain adjustments are independent of each other if the offset adjustment is made first. To minimize transition noise at the gain and offset pins, a 1 μF decoupling capacitor should be connected as shown on the diagram of Figure 3.

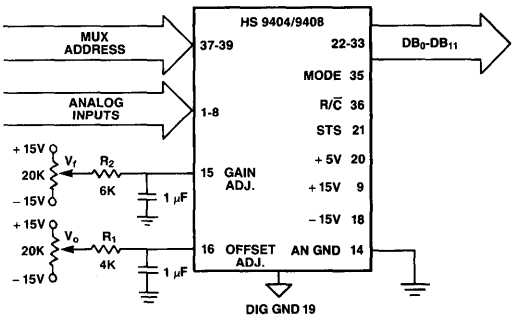


Figure 3. Gain and Offset Input Connections

OFFSET ADJUSTMENT PROCEDURE

1. For unipolar ranges:
   a) Set input voltage precisely to + 1/2 LSB.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001.
2. For bipolar ranges:
   a) Set input voltage precisely to 1/2 LSB above −FS.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001.

GAIN ADJUSTMENT PROCEDURE

1. Set input voltage precisely to 1/2 LSB less than "all bits on" value. Note that this is 1-1/2 LSB less than nominal full scale.
2. Adjust gain control until converter is switching from 111111111110 to 111111111111.

GAIN ADJUSTMENT PROCEDURE (continued)

Table 4 summarizes the offset and gain adjustment procedure and shows the proper input test voltages used in calibrating the DAS.

Input Voltage Range	Adjustment	Input Voltage	Adjust input to point where converter is just on the verge of switching between the two codes shown.[1]
0 to +10V	OFFSET	1.22mV	0000 0000 000Ø
	GAIN	9.9963V	1111 1111 111Ø
±5V	OFFSET	−4.9988V	0000 0000 000Ø
	GAIN	4.9963V	1111 1111 111Ø
±10V	OFFSET	−9.9976V	0000 0000 000Ø
	GAIN	9.9927V	1111 1111 111Ø

[1]Codes shown are natural binary for unipolar input ranges and offset binary for bipolar ranges.
Ø = transition between logic "1" and logic "0".

Table 4. Calibration Data

Note: For bipolar operation, OFFSET adjust sets −full scale (or all zeros out code), not 0V in (midscale code).

The offset and gain adjustments at pins 16 and 15 only affect the A/D converter. The offset adjustment as shown should have enough range to compensate for any internal errors. If the internal amplifier is used at greater than unity gain, a gain adjustment should be added to the R_G circuit of the instrumentation amplifier. Note: If the gain and offset pins are not being used, they should be left floating.

GROUNDING CONSIDERATIONS

To insure maximum accuracy, the HS 9404/HS 9408s have a separate analog and digital ground; these two grounds must be routed properly to prevent DC and transient errors.

DC errors can be caused by current flowing through a run resistance between the system ground reference and the DAS ground reference. (One mA through 2.5Ω will cause an LSB of error.) The best way to prevent this type of error is to connect the digital and analog grounds very close to the HS 9404 or HS 9408 and use this point as the system ground. This can be done as a so-called "star ground" as shown in Figure 5a or as shown in Figure 5b. In Figure 5a, the single common ground reference insures no ground current or ground loop errors. The circuit of Figure 5b sends all digital currents to the digital supply reference thereby preventing any digital current flow through a common ground supply return.

APPLICATIONS INFORMATION (continued)

GROUNDING CONSIDERATIONS (continued)

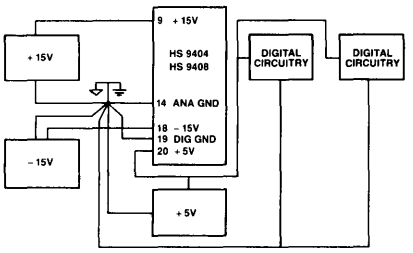


Figure 5a.

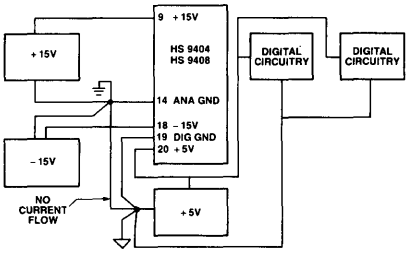


Figure 5b.

Since all ground currents are returned to their respective power supplies, no current flows through the connection between analog and digital ground; this causes both ground points to be at the same potential. If possible, a ground plane should be placed underneath the package to reduce noise pickup. If this is not the case, do not run any digital lines underneath the package. The HS 9404/9408 Series has been layed out such that the analog section is on pins 1 through 20 and the digital section is on pins 21 through 40. To get 12-bit accuracy, the PC board should adhere to the same general layout rules.

To minimize transient-caused errors, decoupling capacitors are recommended between all supplies and their respective grounds. The HS 9404 and HS 9408 have three 0.01 μF ceramic bypass capacitors inside, so an external 10 μF for each supply should be all that is required.

INSTRUMENTATION AMPLIFIER & ANALOG FRONT END

The HS 9404 has a full instrumentation amplifier with high impedance differential inputs and resistor programmable gain. The output of the amplifier is available for driving other analog circuitry or accessing the signal after amplification. Be aware that any loading in excess of 2 K ohms in parallel with 10 pF will adversely affect output voltage swing and settling time.

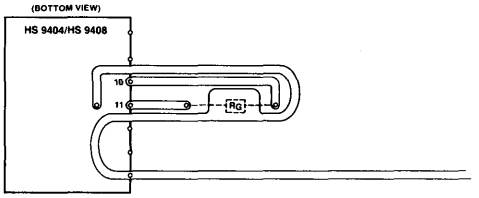
The formulas for calculating gain and the gain resistor are as follows:

$$A_V = \frac{20K}{R_G} + 1 \qquad R_G = \frac{20K}{A_V - 1}$$

Some typical values are as follows:

GAIN	1	5	10	50	100
R_G	infinite	5.000 K Ω	2.222 K Ω	408.2 Ω	202.0 Ω

Special care must be exercised when operating at high gains (>20) to avoid coupling error signals into the relatively high impedance GAIN (−) and GAIN (+) pins. The gain set resistor should be placed as close to the HS 9404/9408 package as possible and the connections should be guarded with a quiet, low impedance signal trace such as analog ground, REF OUT, +15V or AMP OUT. The use of a ground plane is preferred. To minimize gain errors due to temperature, a low drift (low temperature coefficient of resistance) resistor should be used for R_G with a TCR < 25 ppm/°C over the required temperature range.



Reference output current capability decreases as temperature increases. If REF OUT must supply more than ±1 mA above 70°C, an external current buffer is recommended.

If the circuit is to be used at or near its maximum throughput rate, care must be used to prevent dynamic errors due to source impedance at the multiplexer inputs. If a low-pass anti-alias filter is used at the analog inputs (Figure 6a), it is suggested that a buffer be used (Figure 6b) to eliminate charge-transfer errors between C_{FILTER} and $C_{MUX,AMP}$ (Figure 6c).

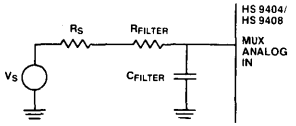


Figure 6a. (not recommended)

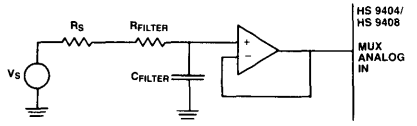


Figure 6b. (recommended)

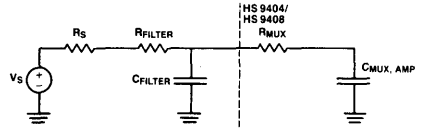


Figure 6c. (equivalent circuit of 6a)

The multiplexer used on the military processed devices is made with dielectrically isolated CMOS analog switches. They can withstand a continuous voltage of 10 volts greater than either supply and transient spikes of several hundred volts. This can eliminate the need for complex protection. The commercial devices use a multiplexer which can withstand voltages no greater than $V_{SUPPLY}{}^{4}$. Thus, for commercial devices, make sure that power is applied to the device before or at the same time analog voltages appear at the MUX. This will save the device from destruction.

APPLICATIONS INFORMATION (continued)

UNIPOLAR/BIPOLAR CONFIGURATION

The HS 9404/HS 9408 - 2 are 20 volt range units which must be operated in bipolar configuration to give a ± 10V input signal range (for unity gain amplification). The HS 9404/HS 9408 - 1 are 10 volt range units which can be operated in unipolar or bipolar modes.

To connect for bipolar operation, short pin 17 to pin 13. For unipolar operation, short pin 17 to analog ground.

Noise performance is improved in bipolar mode if pin 17 is decoupled to analog ground with a 0.01 μF ceramic capacitor. (This value may be inadequate at + 125°C, causing the reference to oscillate.)

INPUT EXPANSION

The DAS is configured with either an 8-channel single-ended or 4-channel differential input. This was done to optimize package size and cost. In the event the user wishes to increase the number of input channels, examples of input expansion are shown in Figures 7a and 7b.

ADDR2	ADDR1	ADDR0	CHANNEL OUT
0	0	0	NONE
0	0	1	±IN1
0	1	0	±IN2
0	1	1	±IN3
1	0	0	±IN4
1	0	1	±IN5
1	1	0	±IN6
1	1	1	±IN7

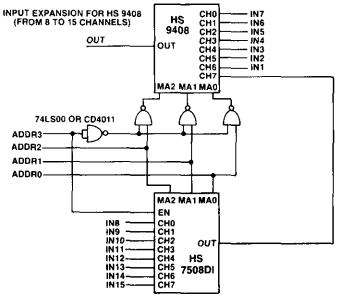


Figure 7a

ADDR3	2	1	0	CHANNEL OUT
0	0	0	0	NONE
0	0	0	1	IN1
0	0	1	0	IN2
0	0	1	1	IN3
0	1	0	0	IN4
0	1	0	1	IN5
0	1	1	0	IN6
0	1	1	1	IN7
1	0	0	0	IN8
1	0	0	1	IN9
1	0	1	0	IN10
1	0	1	1	IN11
1	1	0	0	IN12
1	1	0	1	IN13
1	1	1	0	IN14
1	1	1	1	IN15

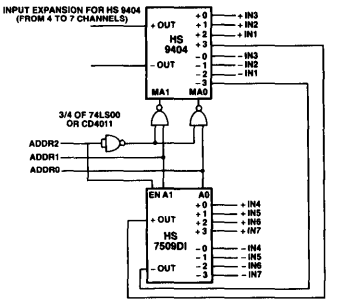
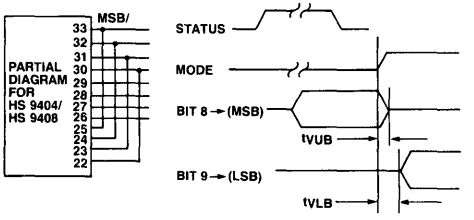


Figure 7b

To allow the HS 9404/9408 to be used with an 8-bit bus, Figure 8 should be utilized.



tVUB = TIME FOR UPPER BITS TO GO TO HIGH IMPEDANCE – 125ns
tVLB = TIME FOR LOWER BITS TO REACH VALID STATE – 250ns

Figure 8. 8-Bit Bus Read Mode — 12-Bit Conversion

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Devices should never be plugged in under power and the PC board the device is in should be handled with caution. Unused digital inputs should never exceed the logic supply by 0.5 volts or go below ground by 0.5 volts. Thus, when powering up these devices, all supplys should come on at the same time. If not, a logic "1" on an unpowered device can destroy the digital inputs.

ORDERING INFORMATION

MODEL NUMBER	INTEGRAL LINEARITY	INPUT RANGE(S)	TEMPERATURE RANGE	SCREENING
HS 940X-J1	± 1 LSB	± 5V, 0 to + 10V	0°C to + 70°C	
HS 940X-J2	± 1 LSB	± 10V	0°C to + 70°C	
HS 940X-K1	± ½ LSB	± 5V, 0 to + 10V	0°C to + 70°C	
HS 940X-K2	± ½ LSB	± 10V	0°C to + 70°C	
HS 940X-S/B-1	± 1 LSB	± 5V, 0 to + 10V	– 55°C to + 125°C	883 Rev. C
HS 940X-S/B-2	± 1 LSB	± 10V	– 55°C to + 125°C	883 Rev. C
HS 940X-T/B-1	± ½ LSB	± 5V, 0 to + 10V	– 55°C to + 125°C	883 Rev. C
HS 940X-T/B-2	± ½ LSB	± 10V	– 55°C to + 125°C	883 Rev. C

NOTES:
1. HS 940X

Specifications subject to change without notice.

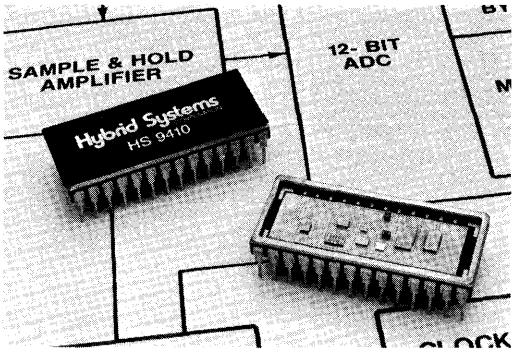
MODEL SUFFIX	INPUT CHANNELS
4	4 DI
8	8 SE

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

8 CHANNEL, 12-BIT DATA ACQUISITION SYSTEM WITH μP INTERFACE

FEATURES

- Complete 8 channel, 12-bit data acquisition system with MUX, S/H, REF, clock and three-state outputs
- Full 8- or 16-bit microprocessor bus interface
- Guaranteed linearity over temperature
- High throughput rate: 25kHz
- Hermetic 28-pin ceramic or low cost epoxy DIP
- Low Power: 400mW



DESCRIPTION

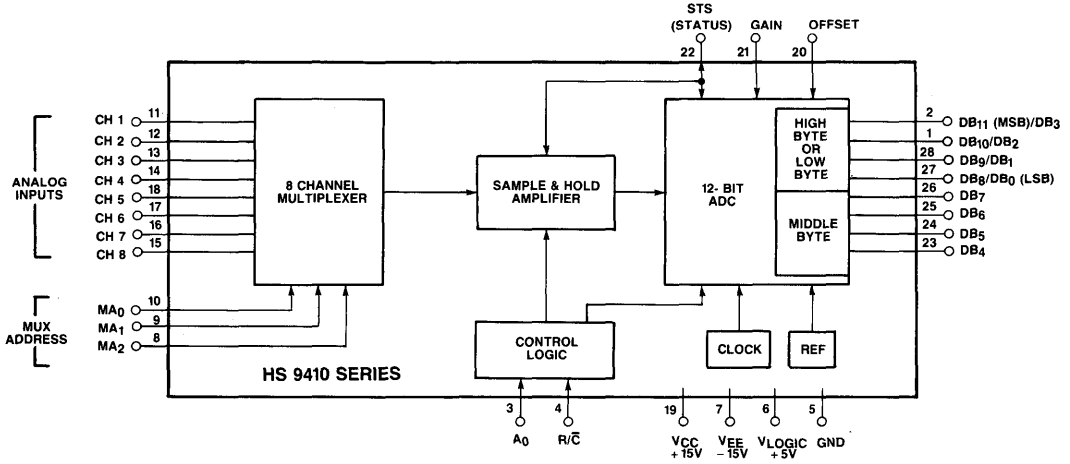
The HS9410 Series is a complete 8 channel, microprocessor compatible, 12-bit data acquisition system with all the interface logic to connect directly to 8- or 16-bit microprocessor buses. It is contained in a 28-pin DIP and includes an 8 channel multiplexer, a sample-and-hold amplifier, and a 12-bit A/D converter along with the control logic needed to perform a complete data acquisition function. System throughput rate is 25kHz for full rated accuracy.

The analog-to-digital converter section contains the HS574 12-bit ADC. The HS9410 Series is offered in a hermetically-sealed package for use over a wide temperature range and for MIL-STD-883 requirements.

The HS9410 Series operates from ±15V* and +5V with a total power consumption of 400mW. To take advantage of the 28-pin package the user must specify an input range of 0 to +10V, ±5V or ±10V when ordering. Four basic product grades are available; J and K models are specified over a temperature range of 0°C to +70°C while the S and T models are specified over an extended temperature range of −55°C to +125°C. Full screening to MIL-STD-883C and processing in accordance with Method 5008.1 is available with models specified as "B."

* ±12V operation possible; consult factory for further information.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V, V_{EE} = −15V, V_{LOGIC} = +5V, unless otherwise specified.)

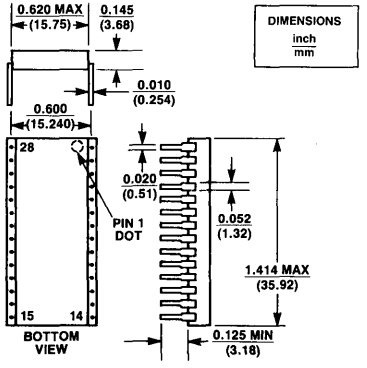
MODEL	HS 941XJ	HS 941XK	HS 941XS	HS 941XT
TRANSFER CHARACTERISTICS				
Resolution	12-Bits	•	•	•
Number of Channels	8 Single-Ended	•	•	•
Throughput Rate	25 kHz	•	•	•
ANALOG INPUTS				
Input Ranges[1] (Specified as a suffix in the model number. See Ordering Guide.)				
HS 9410	0 to +10V	•	•	•
HS 9411	±5V	•	•	•
HS 9412	±10V	•	•	•
Input Bias Current per Channel				
I_{IB} 25°C	±10nA	•	•	•
−55°C to +125°C			±250nA max	•
Input Impedance				
ON Channel	10^{10} Ω|| 100pf	•	•	•
OFF Channel	10^{10} Ω|| 10pf	•	•	•
DIGITAL INPUTS				
Logic Inputs				
R/C, A_0				
V_{IH} min	+2.4V	•	•	•
V_{IH} max	+5.5V	•	•	•
V_{IL} max	+0.8V	•	•	•
V_{IL} min	−0.5V	•	•	•
I_{IL} max	±5μA max	•	•	•
I_{IH} max	±5μA max	•	•	•
Multiplexer Inputs				
V_{IL} max	+0.8V	•	•	•
V_{IH} min	+2.4V	•	+4.0V[2]	+4.0V[2]
Input Capacitance (All Digital Inputs)	5pF typ	•	•	•
Minimum Start Pulse				
R/C-Negative	50ns	•	•	•
SIGNAL DYNAMICS				
Conversion Time				
12-Bit Conversion	25μs max	•	•	•
8-Bit Conversion	19μs max	•	•	•
DIGITAL OUTPUTS				
Logic Outputs				
DB_{11}-DB_0, STS				
Logic 0	+0.4V max, $I_{OL} \leq 1.6$mA	•	•	•
Logic 1	+2.4V min, $I_{OH} \leq 0.5$mA	•	•	•
Leakage (High Z State)	±5μA typ (DB_{11}-DB_0 only)	•	•	•
Capacitance	5pF typ	•	•	•
Output Code Configuration				
Unipolar	Positive True Binary	•	•	•
Bipolar	*Positive True Offset Binary*	•	•	•
POWER SUPPLY				
V_{LOGIC}	+4.5 to +5.5 Volts @ 11mA max	•	•	•
V_{CC}	+13.5 to +16.5 Volts @ 16mA max	•	•	•
V_{EE}	−13.5 to −16.5 Volts @ 7mA max	•	•	•
Power Dissipation	400mW max	•	700mW typ, 1W max	700mW typ, 1W max
Rejection[3]				
V_{LOGIC}	0.002%/% typ, 0.005%/% max	•	•	•
V_{CC}	0.002%/% typ, 0.005%/% max	•	•	•
V_{EE}	0.002%/% typ, 0.005%/% max	•	•	•
ACCURACY				
Linearity Error (% of F.S.R. max)	±0.025	±0.012	±0.025	±0.012
Offset[4]		•	•	•
Unipolar (% of F.S.R. max)	±0.05			
Bipolar (% of F.S.R. max)	±0.25	±0.1	±0.25	±0.1
Gain[4] (% to F.S.R. max)	±0.3	•	•	•
STABILITY				
Linearity (ppm/°C max)	±0.5	±0.5	±2.5	±2.5
Unipolar Offset (ppm/°C max)	±10	±5	±25	±20
Bipolar Offset (ppm/°C max)	±25	±20	±25	±20
Gain (Scale Factor)(ppm/°C max)	±50	±20	±50	±25
TEMPERATURE RANGE				
Operating	0° to +70°C	•	−55°C to +125°C	−55°C to +125°C
Storage	−25°C to +85°C	•	−65°C to +150°C	−55°C to +125°C

NOTES:
1. For J and K models, positive analog input voltage should not exceed V_{CC} − 4 volts. Exceeding V_{CC} − 4 volts can cause an OFF channel to be turned ON. Negative input voltages and input voltages for S and T models may go to supply voltages. Input voltages exceeding these values will not result in permanent damage as long as the absolute maximum ratings are not exceeded. 2. 1K pullup to +5V recommended for MA_0-MA_2 when driven by TTL. 3. Maximum change over rated supply voltage. 4. Externally adjustable to zero. See Applications Information.

*Specifications same as HS 9410J.

PACKAGE OUTLINE

Dimensions shown in inches and (mm).



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	DB_{10}/DB_2	28	DB_9/DB_1
2	DB_{11}(MSB)/DB_3	27	DB_8/DB_0
3	A_0	26	DB_7
4	R/$\overline{C}$	25	DB_6
5	GROUND	24	DB_5
6	V_{LOGIC}	23	DB_4
7	V_{EE}	22	STS(STATUS)
8	MUX ADDRESS A_2	21	GAIN
9	MUX ADDRESS A_1	20	OFFSET
10	MUX ADDRESS A_0	19	V_{CC}
11	INPUT CH 1	18	INPUT CH 5
12	INPUT CH 2	17	INPUT CH 6
13	INPUT CH 3	16	INPUT CH 7
14	INPUT CH 4	15	INPUT CH 8

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Common GND . . . . . 0 to + 16.5V
V_{EE} to Common GND . . . . . 0 to − 16.5V
V_{LOGIC} to Common GND . . . . . 0 to + 7V
Control Inputs (A_0, R/C) to
Common GND . . . . . − 0.5V to V_{LOGIC} + 0.5V
Power Dissipation 1.3W
Lead Temperature, Soldering . . . . . 300°C, 10Sec
Maximum Input Voltage . . . . . V_{CC} + 20V
Minimum Input Voltage . . . . . V_{EE} − 20V
Analog Input Maximum Current 25mA

CONTROL FUNCTIONS

The HS 9410 Series contains control functions necessary to provide for microprocessor interface. All control functions are defined in Tables 1, 2, and 3.

Function	Definition	Function
R/$\overline{C}$	Read/Convert	1. ↓ initiates conversion. 2. Low (0) disconnects data bus. 3. High (1) initiates read.
A_0	Device Address	1. Selects conversion mode. 12-bits if low (0), 8-bits if high (1) when R/$\overline{C}$ ↓. 2. In read mode A_0 selects the output format. If low (0) then 8 MSB's (high and middle byte) or if high (1) then only low byte and trailing zeroes.
MA_0 MA_1 MA_2	Multiplexer Address	Select Channels 1-8 (see MUX Logic Table 3)

Table 1. Defining the Control Functions

Control Inputs		Operation
R/$\overline{C}$	A_0	
↓	0	Initiates 12-bit conversion
↓	1	Initiates 8-bit conversion
1	0	Enables 8 MSB's (high byte)
1	1	Enables 4 LSB's (low byte) and 4 trailing zeros
0	X	Output data (DB) goes to high impedance state.

Table 2. Truth Table—Control Inputs

Mux Address Inputs			Channel Selected
A_2	A_1	A_0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

NOTES:
1. 1 indicates logic HIGH.
2. 0 indicates logic LOW.
3. X indicates don't care.
4. ↓ indicates operation commences on high to low transition.
5. MSB → XXXX (High Byte) XXXX (Middle Byte)
6. XXXX (Low Byte) ← LSB

Table 3. Truth Table—Multiplexer Address

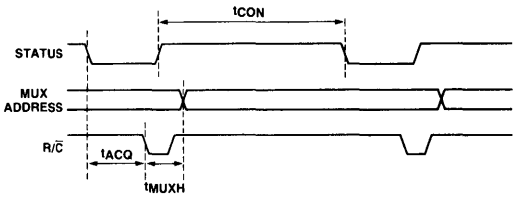
APPLICATIONS INFORMATION

TIMING

The timing diagrams are shown in Figures 1 through 6. Figures 1 and 2 show how the multiplexer addressing is related to the convert cycle, while Figures 3 and 4 show the timing sequence to start either a 12- or an 8-bit conversion. Figures 5 and 6 show how to read the multiplexed data from the internal register in the HS 9410.

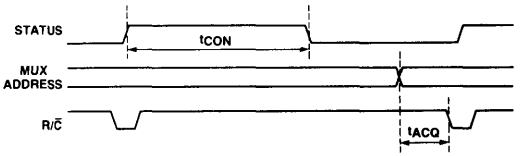
Figures 1 and 2

The multiplexer address can be changed either during or after a conversion, but care must be taken not to change the address within 1 microsecond after the convert command to insure that the sample/hold will not start to acquire the signal of the new channel. After the multiplexer address has been changed, you must allow the sample/hold at least 10 microseconds **in sample mode** to acquire the new input signal.



t_{MUXH}	Multiplexer address hold time after convert command	1μs min
t_{ACQ}	Minimum time between conversions (S/H acquisition time)	10μs min
t_{CON}	Conversion time for -12 bit resolution	25μs max
	- 8 bit resolution	19μs max

Figure 1. Timing Diagram 8/12-Bit Conversion, MUX Address Changes During Conversion

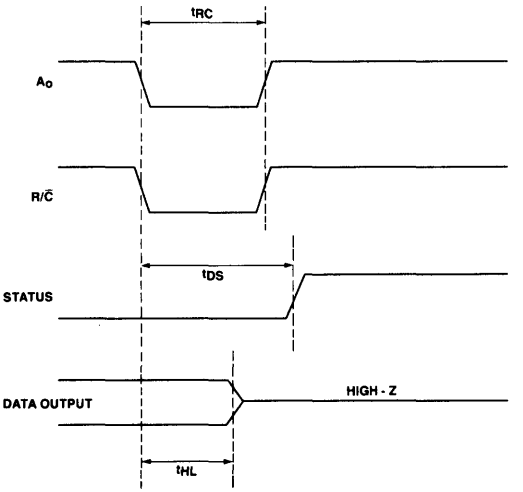


t_{ACQ}	Minimum time between MUX address change and convert command	10μs min
t_{CON}	Conversion time - Specifications, see Figure 1	

Figure 2. Timing Diagram 8/12-Bit Conversion, MUX Address Changes Between Conversions

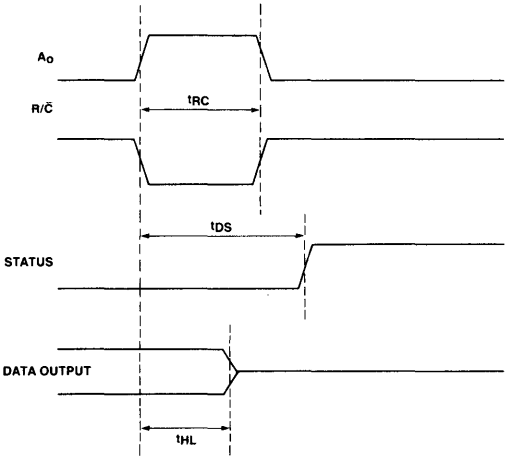
Figures 3 and 4

Figures 3 and 4 show how to start a convert cycle. The logic level of the A_0 line determines whether a 12- or 8-bit conversion will be initiated. If A_0 is low during the start convert command, a 12 bit conversion will be started; if A_0 is high, an 8-bit conversion will occur. The A_0 line has to be setup when the R/$\overline{C}$ line goes to logic '0' and must remain in the desired level for at least 150 ns. The R/$\overline{C}$ line is used both to start a conversion and to read the output data. If R/$\overline{C}$ is going low a conversion is initiated. This is indicated by the STATUS line going high. A second start convert command during a conversion will be ignored. The R/$\overline{C}$ pulse must have a minimum width of 150 ns. For optimum performance the rising edge of the R/$\overline{C}$ pulse should not occur during a conversion if the conversion has been in progress for more than 1.5 microseconds, i.e., the negative R/C pulse should be either shorter than 1.5 microseconds or longer than the conversion time.



t_{RC}	R/C pulse width, A_0 pulse width (Note 1)	50 ns min
t_{DS}	Status delay from R/$\overline{C}$	200 ns max
t_{HL}	Output float delay	150 ns max

Figure 3. Timing Diagram to Start a 12-Bit Conversion

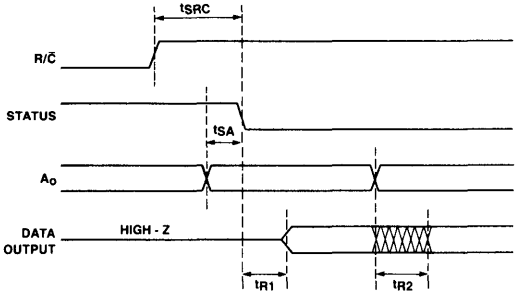


t_{RC}	R/C pulse width, A_0 pulse width (Note 1)	50 ns min
t_{DS}	Status delay from R/$\overline{C}$	200 ns max
t_{HL}	Output float delay	150 ns max

Figure 4. Timing Diagram to Start an 8-Bit Conversion

Figures 5 and 6

If a conversion is in progress the data output lines are disabled and in the high-impedance state. Data can be enabled by bringing the R/$\overline{C}$ line high after a conversion is complete (this is indicated by the STATUS line going low; Fig. 6). If R/$\overline{C}$ has been returned high during a conversion the data outputs will be enabled automatically after STATUS goes low (Fig. 5). The A_0 line is used to address either the 8 upper data bits or the 4 lower data bits followed by 4 trailing zeros. If an 8-bit conversion has been performed the lower 4 bits will always be '0'. After an 8-bit conversion, it is not necessary to read the lower 4 bits prior to starting a new conversion. Note that A_0 only controls the address of the two data bytes while the high impedance state of the output buffers is controlled by the R/$\overline{C}$ and STATUS line. The output buffers will not return to the high impedance state when A_0 is changed to address the second data byte.



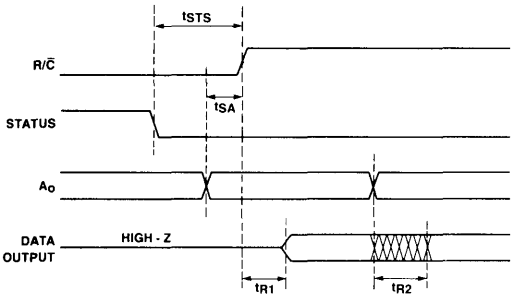
t_{SRC}	R/C set-up time prior to status going low	0 ns min
t_{SA}	A_0 set-up time prior to status going low (Note 2)	100 ns min
t_{R1}	Access time, 1st data byte (from status)	125 ns max
t_{R2}	Access time, 2nd data byte (from A_0)	225 ns max

Figure 5. Timing Diagram Read Cycle, R/$\overline{C}$ Going High During Conversion

NOTES:

1. For optimum performance the positive edge of the R/C pulse should not occur during a conversion if the conversion has been started for more than 4.5 microseconds. The negative R/C pulse should be longer than the 4.5 microseconds before STATUS goes high.

2. If the set-up time for A_0 cannot be met, the access time for the first data byte will be increased. In that case the first data byte will become valid 225 ns max after the change of the A_0 line.



t_{STS}	Status going low prior to R/C going high	0 ns min
t_{SA}	A_0 set-up time prior to R/C going high (Note 2)	100 ns min
t_{R1}	Access time, 1st data byte (from R/C)	125 ns max
t_{R2}	Access time, 2nd data byte (from A_0)	225 ns max

Figure 6. Timing Diagram Read Cycle, R/$\overline{C}$ Going High After Conversion

USING THE A_0 LINE

The state of A_0 at the start of a conversion places the DAS in either a full 12-bit conversion or in an 8-bit 'short cycle' mode. During a READ at the end of a conversion A_0 is used to format the data as follows:

1. Prior to Conversion (WRITE)

	MODE
$A_0 = 1$	Short cycle 8-bit conversion
$A_0 = 0$	Full 12-bit conversion

2. After Conversion (READ)

$A_0 = 1$	Data = Low Byte (LSB) followed by zeros
$A_0 = 0$	Data = High Byte (MSB's) followed by middle byte.

In a μP application A_0 can be considered a pair of $\overline{W/R}$ locations as follows:

1. Prior to Conversion (WRITE)

	MODE
$\overline{W/R} = 0$ in low address ($A_0 = 0$)	Full 12-bit conversion
$\overline{W/R} = 0$ in high address ($A_0 = 1$)	Short cycle 8-bit conversion

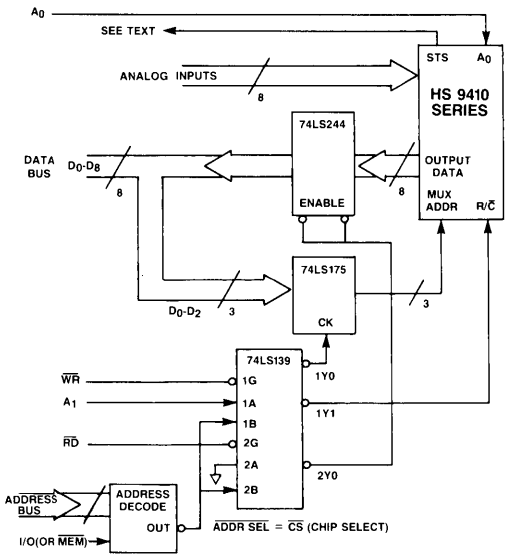
2. After Conversion (READ)

$\overline{W/R} = 1$ in high address ($A_0 = 1$)	LSB's & zeros
$\overline{W/R} = 1$ in low address ($A_0 = 0$)	8 MSB's only

MICROPROCESSOR INTERFACE

The HS 9410 Series DAS can be interfaced with most popular 8-bit microprocessors. The DAS may be either positioned in a memory location (memory map) or as an I/O device. In the case of memory mapping, the DAS acts as a static RAM where READ and WRITE instructions are given to the selected address. When the DAS is connected as an I/O device, the I/O enable can be substituted for the $\overline{MEMR}$ or $\overline{MEMW}$ command. Figure 7 shows a typical scheme to implement this interface.

STS is not used in this example; the μP must read data 30μs after conversion starts. This delay can be generated with NOP or other instructions inserted between the WRITE and READ functions. The STS line can also be used to cause the processor to WAIT or HALT or can be used as an interrupt line such as IREQ (in the case of 6800 or 6502).



					HS 9410 Function	
A_0	A_1	WR	RD	ADDR SEL	Read/Write	Operation
X	0	⌐¯_	1	0	WRITE	MUX ADDRESS
0	1	⌐¯_	1	0	WRITE	START 12-BIT CONV.
1	1	⌐¯_	1	0	WRITE	START 8-BIT CONV.
0	X	1	0	0	READ	HIGH BYTE (8 MSB's)
1	X	1	0	0	READ	LOW BYTE (4 LSB's)

NOTES:

1. 1 indicates logic HIGH. 2. 0 indicates logic LOW. 3. X indicates don't care.
4. ⌐¯_ indicates operation commences on low to high transition.
5. _¯⌐ indicates operation commences on high to low transition.

Figure 7. Interfacing the HS 9410 Series

INPUT EXPANSION

The DAS is configured with an 8 channel high level multiplexer input. This was done to optimize package size (28 pin DIP) and cost. In the event the user wishes to increase the number of input channels, a double rank MUX input is recommended (series connected). This typical configuration is shown in Figure 8.

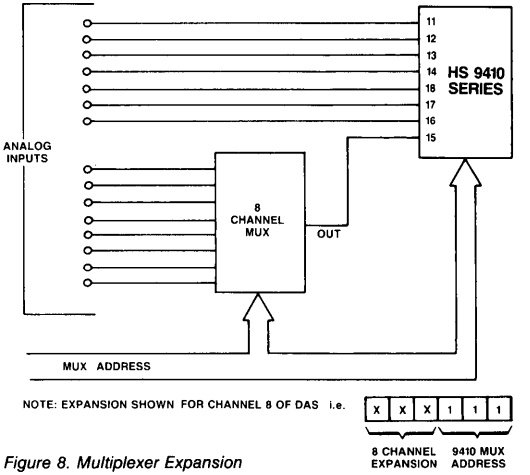


Figure 8. Multiplexer Expansion

ZERO AND GAIN CONNECTIONS

The DAS is normally used with external zero and gain calibration potentiometers. However, if maximum accuracy is not required, they may be omitted. The zero control has a range of about $\pm$20LSB, and the gain control has a range of about $\pm$13LSB.

Proper gain and zero calibration requires great care and the use of extremely sensitive and accurate instruments. The voltage source used as a signal input must be very stable. It also should be capable of being set to within 1/10LSB at both ends of its range.

The DAS's zero and gain adjustments are independent of each other if the zero (or offset) adjustment is made first.

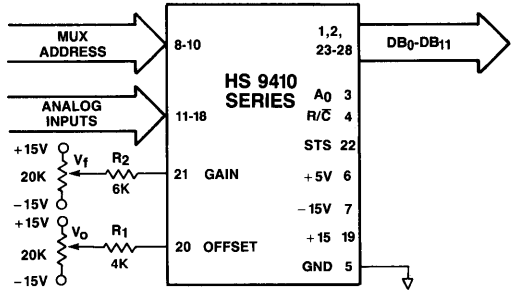


Figure 9. Gain and Offset Input Connections

ZERO ADJUSTMENT PROCEDURE

1. For unipolar ranges:
   a) Set input voltage precisely to + ½LSB.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001.
2. For bipolar ranges:
   a) Set input voltage precisely to ½LSB above – F.S.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001
3. When offset adjust is not used, tie pin 20 to ground.

GAIN ADJUSTMENT PROCEDURE

1. Set input voltage precisely to ½LSB less than 'all bits on' value. Note that this is 1½LSB less than nominal full scale.
2. Adjust gain control until converter is switching from 111111111110 to 111111111111.
3. When gain adjust is not used, tie pin 21 to ground.

Table 4 summarizes the zero and gain adjustment procedure, and shows the proper input test voltages used in calibrating the DAS.

Input Voltage Range	Adjustment	Input Voltage	Adjust input to point where converter is just on the verge of switching between the two codes shown.[1]
0 to + 10V	ZERO	1.22mV	0000 0000 000Ø
	GAIN	9.9963V	1111 1111 111Ø
± 5V	ZERO	– 4.9988V	0000 0000 000Ø
	GAIN	4.9963V	1111 1111 111Ø
± 10V	ZERO	– 9.9976V	0000 0000 000Ø
	GAIN	9.9927V	1111 1111 111Ø

[1]Codes shown are natural binary for unipolar input ranges and offset binary for bipolar ranges.

Ø = transition between a logic 0 and a logic 1 state. All gain, offset and linearity measurements are performed using the transition test method.

Table 4. Calibration Data

POWER SUPPLY CONSIDERATION

Power supplies used for the DAS should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output codes may result with noisy power sources. It is important to remember that 2.44mV is 1LSB for a 10 volt input.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10μF tantalum type in parallel with 0.1μF disc ceramic type.

GROUNDING CONSIDERATIONS

The common at pin 5 is the ground reference point for the internal reference and is thus the high quality ground for the DAS. In order to achieve all of the high accuracy performance available from the DAS in an environment of high digital noise content, care should be taken when handling analog and digital grounds, as follows. Where analog and digital grounds are run separately on the PCB, these should be connected together at the package (pin 5). However, if the grounds are connected separately in the system for other reasons, then only the analog ground should be connected at the package to pin 5. If digital common contains high frequency noise beyond 200mV, this noise may feed through the converter, so that some caution will be required.

It is also important in the layout to carefully consider the placement of digital lines. It is recommended that digital lines not be run directly under the DAS. For optimum system performance, if space permits, a ground plane is advised under the DAS. This should be connected to a digital ground. In packaging the assembled DAS, the designer should also try to minimize any capacitive coupling that might occur at the top to the device. Parallel runs between analog and digital signals should be avoided. A star system ground is the most preferred layout method. See Figure 10.

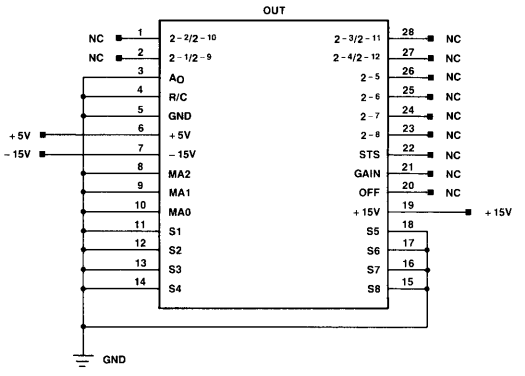


Figure 10. HS 9410 Burn-In Schematic

ORDERING INFORMATION

Model Number[1]	Input Range	System Accuracy (% FSR)	Full Scale T.C. (ppm/°C)	Temp. Range	MIL Screening
HS 94XXJ	SEE NOTE 1	±0.025	50.0	0°C to +70°C	—
HS 94XXK		±0.012	20.0	0°C to +70°C	—
HS 94XXS		±0.025	50.0	−55°C to +125°C	—
HS 94XXT		±0.012	25.0	−55°C to +125°C	—
HS 94XXS/B		±0.025	50.0	−55°C to +125°C	883C
HS 94XXT/B		±0.012	25.0	−55°C to +125°C	883C

NOTES:

1. HS 94XX

MODEL SUFFIX	INPUT RANGE
10	0 to +10V
11	±5V
12	±10V

Add letter suffix as required above.

Specifications subject to change without notice.

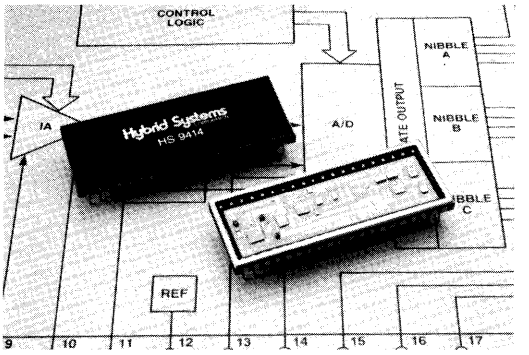
CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SOFTWARE PROGRAMMABLE, 12-BIT, DATA ACQUISITION SYSTEM (DAS)

FEATURES

- MUX, inst. amp, S/H, A/D in a compact 40-pin DIP
- Software programmable gain instrumentation amplifier (SPGIA)
- Input and output offset adjust
- 126 dB dynamic range

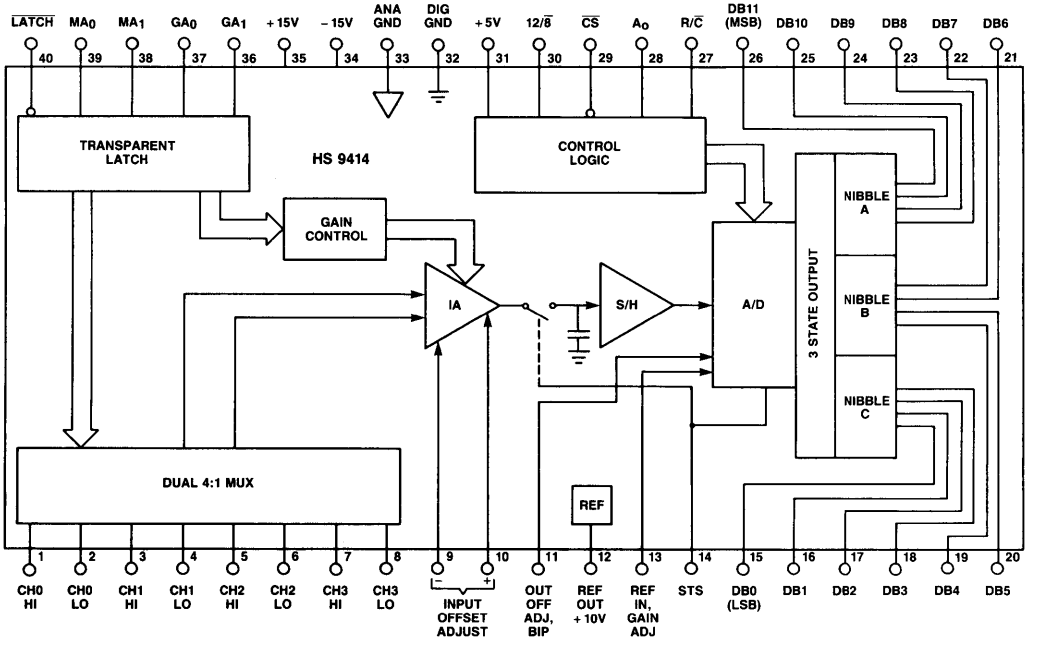


DESCRIPTION

The HS9414 provides complete 12-bit data acquisition functionality in a 40-pin DIP. The HS9414 includes a 4-channel differential input multiplexer, a software programmable instrumentation amplifier, a sample and hold circuit and the HS574A, 12-bit, 25μsec A/D converter. Specifications are guaranteed for the complete system instead of for each individual component.

The HS9414 is offered in a ceramic package for commercial (0°C to +70°C) and military (−55°C to +125°C) applications with processing available in full compliance with MIL-STD-883C.

FUNCTIONAL DIAGRAM



11

SPECIFICATIONS

(Typical @ +25°C, V_{CC} = +15V, V_{EE} = −15V, V_{LOGIC} = +5V unless otherwise specified)

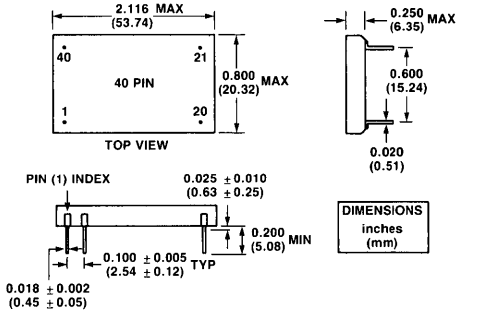
MODEL	HS 9414
ANALOG INPUTS	
Number of Inputs	4 Differential
Input Voltage Range (G = 1)[1]	
Unipolar (−1)	0 to +10V or ±5V
Bipolar (−2)	±10V
Common Mode Voltage Range	$\pm(11 - \frac{\lvert V_{IN}\ Diff\rvert \times Gain}{2})$
Differential Mode Voltage Range	$\pm(\frac{2(10 - \lvert CMV\rvert)}{Gain})$
Input Offset Voltage (Unipolar)[3]	
G = 1	±0.5 LSB
G = 10	±100 μV
G = 100	±50 μV, 250 μV max
G = 500	±50 μV, 250 μV max
Input CH to CH Offset Voltage	2 μV
CMRR	
G = 1	−80 dB typ, −76 dB max
G = 10	−100 dB typ, −90 dB max
G = 100, G = 500	−120 dB typ
Input Dynamic Range	126 dB
Input Bias Current	60 nA
Input Resistance	1 GΩ
Input Capacitance	25 pF
Input Offset Current	60 nA
Input Noise Voltage	2 μV RMS, 10 μV p-p @G = 500
DIGITAL INPUTS	
Logic Inputs	
$\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$	
Logic "1"	+2.0V min, +5.5V max
Logic "0"	−0.5V min, +0.8V max
Current	±50 A max
Capacitance	5 pF
Control Input, 12/$\overline{8}$	Hardwire to V_{LOGIC} or DIG COM
Minimum Start Pulse	
$\overline{CS}$-Negative	120 nsec
R/$\overline{C}$-Negative	120 nsec
LATCH	33 nsec
Data Set-Up Time	
MA0, MA1, GA0, GA1	33 nsec
Fan-Out	1 TTL Load
SIGNAL DYNAMICS	
A/D Conversion Time	25 μsec typ, 30 μsec max
System Throughput Rate[2]	
G = 1,10 (0.01% Settling Accuracy)	28.6 kHz max
G = 100 (0.015% Settling Accuracy)	17 kHz max
G = 500 (0.02% Settling Accuracy)	10 kHz typ
Gain Switching Time and IA Settling Time	
G = 1,10	10 μsec typ
G = 100	50 μsec typ
G = 500	90 μsec typ
Amplifier Bandwidth (−3 dB)	
G = 1	3 mHz
G = 10	2.5 mHz
G = 100	100 kHz
G = 500	20 kHz
S/H Acquisition Time to 0.01%	10 μsec max
S/H Aperture Jitter	50 psec typ
S/H Feedthrough	76 dB
Crosstalk (V_{IN} = 20V p-p sine wave)	−78 dB @40 kHz −90 dB @0.5 kHz
ACCURACY	
Integral Linearity	
HS 9414C (0°C to +70°C)	±½ LSB max
HS 9414B (0°C to +70°C)	±½ LSB max
(t_{MIN} to t_{MAX})	±1 LSB max
Differential Linearity	
HS 9414C (0°C to +70°C)	±¼ LSB typ, ±1 LSB max
HS 9414B (0°C to +70°C)	±¼ LSB typ, ±1 LSB max
(t_{MIN} to t_{MAX})	±¼ LSB typ, ±1 LSB max
No Missing Codes	
12-Bits	0°C to 70°C
11-Bits	−55°C to +125°C
Total Gain Error @G = 1[3] @other gains referred to G = 1	0.1% typ, 0.3% max
G = 10	0.02% typ, 0.1% max
G = 100	0.03% typ, 0.1% max
G = 500	0.05% typ
Bipolar Offset[3]	±1 LSB typ, ±3 LSB max
t_{MIN} to t_{MAX}	15 LSB max
DRIFT	
Integral Nonlinearity	±2 ppm/°C
Differential Nonlinearity	±2 ppm/°C
Unipolar Output Offset	±10 ppm/°C
Bipolar Output Offset	±10 ppm/°C
Gain Tempco G = 1	±25 ppm/°C
REFERENCE	
Output Voltage	10.00V nominal, ±0.1V max
Tempco	±30 ppm/°C typ, ±50 ppm/°C max
Output Current	1.5 mA

MODEL	HS 9414
POWER REQUIREMENTS	
Power Supply Range	±15V, ±5%
PSSR (All Supplies) %FSR/% Supply	0.002%/% typ, 0.005%/% max
Current Drain	
+15V	22 mA typ, 27 mA max
−15V	10 mA typ, 15 mA max
+5V	2 mA typ, 5 mA max
Power Dissipation	490 mW typ, 655 mW max
TEMPERATURE RANGE	
Operating	
9414C	−0°C to +70°C
9414B	−55°C to +125°C
Storage	−65°C to +165°C

NOTES:

1. Input range selected at factory.
   HS 9414C-1 = 0 to +10V or ±5V input
   HS 9414C-2 = ±10V input
   HS 9414B-1 = 0 to +10V or ±5V input
   HS 9414B-2 = ±10V input
2. Assumes pipelining — signal is applied to I.A., acquired by sample/hold and converted by A/D.
3. Externally adjustable to zero. See Applications Information.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	CH0 HI	40	$\overline{LATCH}$
2	CH0 LO	39	MA0
3	CH1 HI	38	MA1
4	CH1 LO	37	GA0
5	CH2 HI	36	GA0
6	CH2 LO	35	V_{CC} (+15V)
7	CH3 HI	34	V_{EE} (−15V)
8	CH3 LO	33	Analog GND
9	Input Offset Adjust −	32	Digital GND
10	Input Offset Adjust +	31	V_{LOGIC} (+5V)
11	Output Offset Adjust, Bipolar	30	12/$\overline{8}$
12	Ref Out (+10V)	29	$\overline{CS}$
13	Ref In, Gain Adjust	28	A_0
14	Status	27	R/$\overline{C}$
15	DB0 (LSB)	26	DB11 (MSB)
16	DB1	25	DB10
17	DB2	24	DB9
18	DB3	23	DB8
19	DB4	22	DB7
20	DB5	21	DB6

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$, $\overline{LATCH}$, MA0, MA1, GA0, GA1) to Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, CH0-CH3) to Analog Common ..... ±16.5V
Input Offset Adjust Pins 9, 10 ..... V_{CC} ±1V
REF OUT to Analog or Digital GND ..... Indefinite short circuit to ±V_{DD} ..... 100 ms short circuit
Voltage on Digital Outputs in Tri-State Mode ..... +V_{CC} +0.5V max
Lead Temperature, Soldering ..... 300°C, 10 sec

APPLICATIONS INFORMATION

A/D CONTROL FUNCTIONS

The HS 9414 contains all control functions necessary to provide for complete microprocessor interface and also 'stand alone' operation including continuous conversions. All A/D control functions are defined in Table 1 and Table 2.

FUNCTION	DEFINITION	FUNCTION
$\overline{CS}$	Chip Select	1. Typically the address pin when used with µP. 2. Must be low (0) for a conversion to start or read data at the output. 3. ↓ transition may be used to initiate conversion.
R/$\overline{C}$	Read/$\overline{Convert}$	1. ↓ initiate conversion 2. ↓ initiate read
A_0	Address	1. Selects conversion mode. 12 Bits if low (0). 8 Bits if high (1). 2. In read mode A_0 selects the output format. If low (0) then 8 MSB's (high and middle byte) or if high (1) then only low byte and trailing zeros.
12/$\overline{8}$	Output Format	1. May be hard wired. 2. Normal 12-Bit format if high (1). 3. 8-Bit format as set by A_0 if low (0).

Table 1. Defining A/D Control Functions

CONTROL INPUTS				HS 9414 OPERATION
CS	R/C	12/8	A_0	
1	X	X	X	No Operation
0	↓	X	0	Initiates 12-Bit Conversion
0	↓	X	1	Initiates 8-Bit Conversion
↓	0	X	0	Initiates 12-Bit Conversion
↓	0	X	1	Initiates 8-Bit Conversion
0	↓	Pin 31	X	Enables 12-Bit Parallel Output
0	↓	Pin 32	0	Enables 8 MSB's
0	↓	Pin 32	1	Enables 4 LSB's and 4 Trailing Zeros
↓	1	Pin 31	X	Enables 12 Bit Parallel Output
↓	1	Pin 32	0	Enables 8 MSB's
↓	1	Pin 32	1	Enables 4 LSB's & 4 Trailing Zero's

NOTES: 1. 1 indicates logic HIGH.
2. 0 indicates logic LOW.
3. X indicates don't care.
4. ↓ indicates operation commences on low to high transition.
5. MSB → XXXX (High Byte) XXXX (Middle Byte) XXXX (Low Byte) ← LSB
6. Not a common use of this function.

Table 2. HS 9414 A/D Section Truth Table

SPGIA CONTROL FUNCTIONS

The HS 9414 has a 4-Bit transparent latch that selects input MUX channel as well as Gain. The SPGIA control functions are defined in Table 3.

NAME	DEFINITION	FUNCTION
LATCH	MUX, Gain, Clock	1. ↓ Update input MUX & Gain 2. ↑ Hold input MUX & Gain 3. High (1) is hold mode 4. Low (0) is transparent mode
MA1, MA0	MUX Address	Select Input MUX Channel MA0 MA1 CH 0 0 0 0 1 1 1 0 2 1 1 3
GA1, GA0	Gain Address	Select Gain GA1 GA0 Gain 0 0 0(x1) 0 1 1(x10) 1 0 2(x100) 1 1 3(x500)

Table 3. Defining the SPGIA Control Functions

TIMING

The timing diagrams are shown in Figure 1. Note that to start a conversion $\overline{CS}$, and R/$\overline{C}$ must have an overlap time of 120 nS minimum. $\overline{CS}$ and R/$\overline{C}$ may be advanced or delayed if needed (by the application) but no specifications are given for this — only the coincidence of 120 nS must be met. Typically R/$\overline{C}$ is used to initiate a conversion — however other lines may be used. See truth table (Table 2).

In the READ mode **note the access time t_{DD} is 125 nS typ, 150 nS max. This means that an entire conversion can be completed and read in 25.3 µS typ, 30.35 µS max** including setup, conversion time and access time.

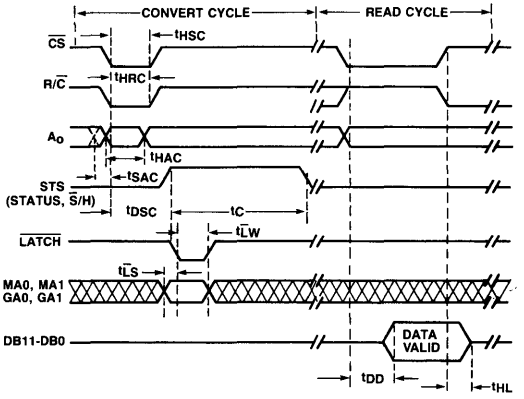


Figure 1a. HS 9414 Interface Timing

CONVERT CYCLE

SYMBOL	PARAMETER	
t_{HSC}	$\overline{CS}$ Pulse Width	120 nS min
t_{HRC}	R/$\overline{C}$ LOW during $\overline{CS}$ LOW	120 nS min
t_{HAC}	A_0 valid during $\overline{CS}$ LOW	120 nS min
t_{SAC}	Maximum A_0 delay from $\overline{CS}$ Set up as shown (negative time wrt* $\overline{CS}$) not needed	60 nS max
t_{DSC}	STS delay from $\overline{CS}$	150 nS min
t_C	Conversion time	
	8 Bit cycle	15 μS typ, 25 μS max
	12 Bit cycle	25 μS typ, 30 μS max
t_{LS}	$\overline{LATCH}$ Setup Time	33 nS min
t_{LW}	$\overline{LATCH}$ Pulse Width	33 nS min

NOTE: No setup for $\overline{CS}$, R/$\overline{C}$ or A_0 is required. The only condition that must be satisfied is 120 nS coincidence, as shown. R/$\overline{C}$, or $\overline{CS}$, can be advanced or delayed as needed as long as this condition is met. Should A_0 be delayed (t_{SAC} 60 nS) then this must be added to $\overline{CS}$ and R/$\overline{C}$. This condition not shown above.

READ CYCLE

t_{DD}	Access time from $\overline{CS}$ LOW	125 nS typ, 150 nS max
t_{HL}	Output Float Delay	150 nS max

*wrt = With Respect To.

Figure 1b. HS 9414 Interface Timing

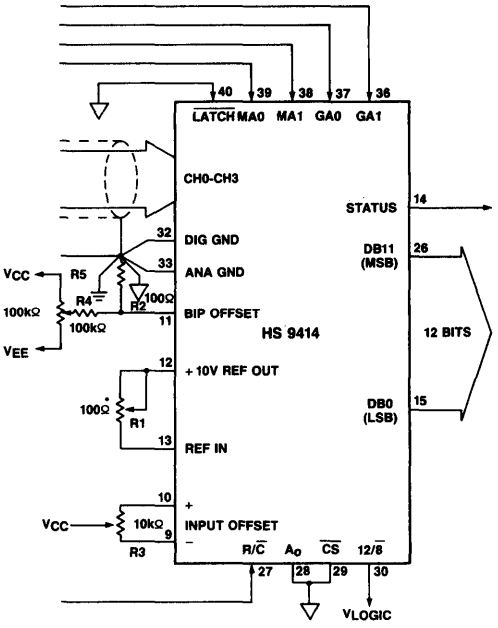


Figure 2b. Unipolar Stand-Alone Connections with Offset and Gain Adjustments

STAND-ALONE OPERATION

The HS 9414 can be used in a 'stand-alone' mode. Connections and timing for this mode are shown in Figure 2.

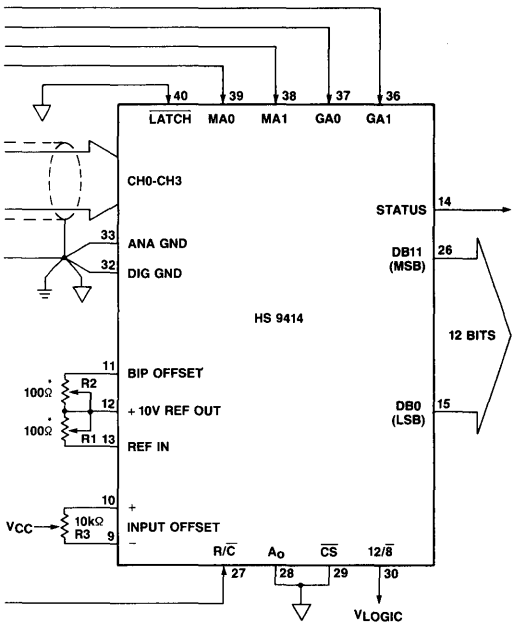


Figure 2a. Bipolar Stand-Alone Connections with Offset and Gain Adjustments

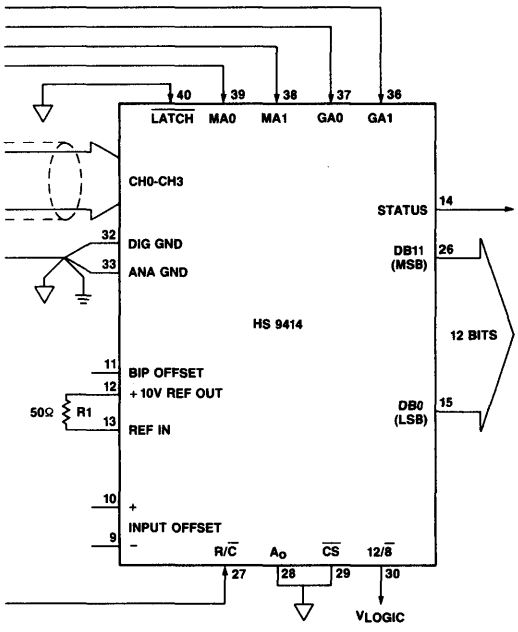


Figure 2c. No Trim Unipolar Connections

*Trimpots can be 300Ω for greater range adjustments.

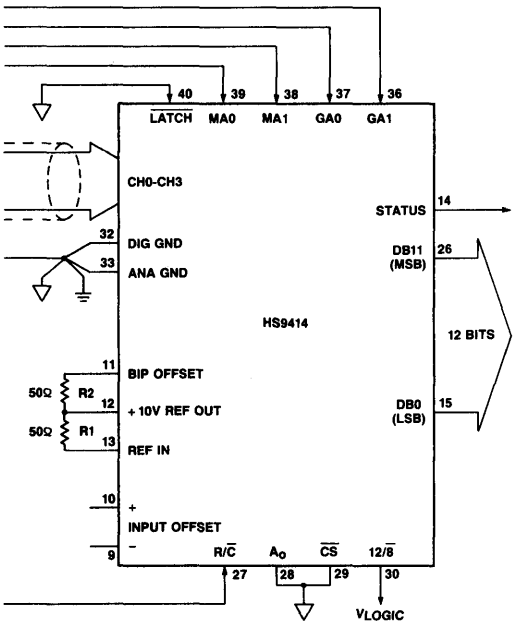
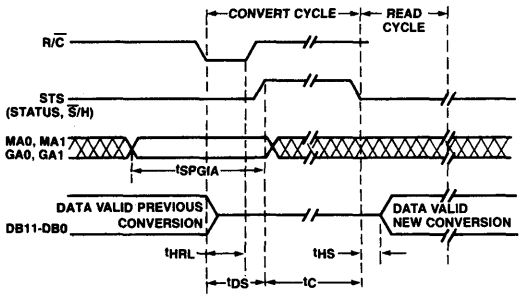


Figure 2d. No Trim Bipolar Connections

R/C NEGATIVE PULSE



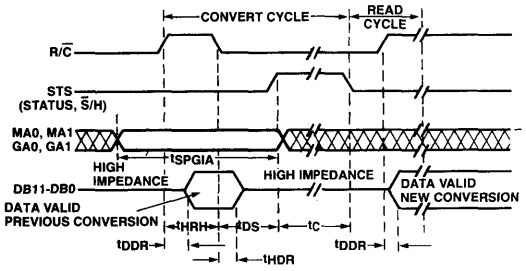
CONVERT CYCLE

SYMBOL	PARAMETER	
t_{HRL}	Low R/C Pulse Width	100 nS min
t_{DS}	STS Delay from R/C	200 nS max
t_C	Conversion Time	30 μS max
t_{HS}	Data valid after STS low	70 nS max
t_{SPGIA}	Software programmable gain instrumentation amplifier and S/H settling time after input MUX, gain or input signal change	

READ CYCLE

1. Data always in read mode except during a conversion in which data lines revert to high impedance or when R/C goes low (0).
2. Output always valid after conversion is complete.

R/C POSITIVE PULSE



CONVERT CYCLE

SYMBOL	PARAMETER	
t_{HDR}	Valid Data (Previous Conversion) after R/C low	100 nS min
t_{HRH}	High R/C Pulse Width	90 nS min
t_{DS}	STS Delay from R/C	200 nS max
t_{DDR}	Data Access Time	150 nS max
t_C	Conversion Time	30 μS max
t_{SPGIA}	Software programmable gain instrumentation amplifier and S/H settling time after input MUX, gain or input signal change	

READ CYCLE

1. Converter output remains in high impedance state after conversion (STS goes low) until R/C goes high (to read data).

Figure 3. HS 9414 Stand-Alone Operation
Top: Using Negative R/C Pulse
Bottom: Using Positive R/C Pulse

INCREASING THROUGHPUT

To minimize added set-up delay, overlapping the multiplexer channels can significantly improve throughput. The technique involved is the same as normal operation; however, instead of waiting for the A/D to complete a conversion before selecting a new multiplexer channel, the new channel is selected at the start of the A/D conversion. By doing this, the A/D digitizes the analog voltage that is held in the sample and hold and the new multiplexer channel's voltage can start to settle through the multiplexer and intrumentation amplifier. An added 25 μS (A/D conversion time) can be saved from the front end settling time required by preselecting the new channel. After the A/D is finished converting, the sample and hold will switch back to sample to acquire the newly selected channel's voltage and the process repeated.

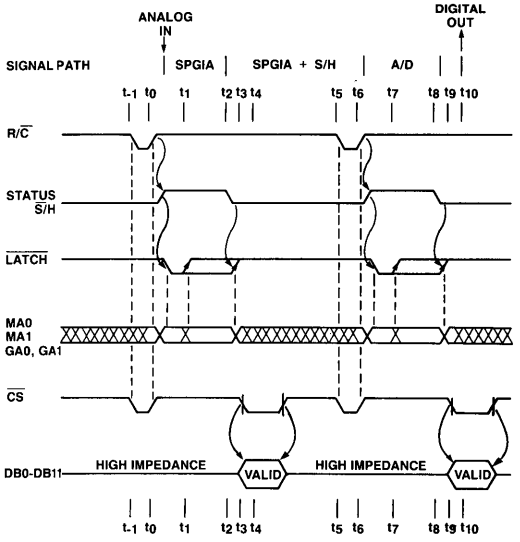


Figure 4. HS 9414 Pipeline Timing for Highest Throughput

t_{-1}-t_0 R/$\overline{C}$ pulse starts new conversion and sample and hold goes to hold mode.

t_0-t_2 New SPGIA gain, new input MUX channel and new input signal while the A/D is converting.

t_3-t_6 Sample and hold samples the new input signal.

t_3-t_4 A/D data from the last signal is retrieved.

t_5-t_6 R/$\overline{C}$ starts conversion of the new input signal.

t_6 Sample and hold holds the new signal.

t_6-t_7 Next SPGIA gain, next input MUX channel and next input signal.

t_7-t_9 The new signal is converted.

t_{10} The new signal digital data is retrieved.

NOTE: Pipeline delay from t_0 to t_{10}
Throughput is $1/t_6$ to Hz
SPGIA settling time from t_0 to t_6
S/H acquisition time from t_2 to t_6

USING THE A_0 LINE

The state of the A_0 line at the start of a conversion places the HS 9414 in either a full 12-Bit conversion or in an 8-Bit 'short cycle' mode. During a READ at the end of a conversion the A_0 line is used to format the data as follows:

1. Prior to Conversion

	MODE
$A_0 = 1$	Short cycle 8-Bit conversion
$A_0 = 0$	Full 12-Bit conversion

2. After Conversion (READ)

$A_0 = 1$	Data = Low Byte (LSB) followed by zeros
$A_0 = 0$	Data = High Byte (MSB's) followed by middle and low byte.

In a μP application the A_0 line can be considered a pair of $\overline{WR}$ locations as follows:

1. Prior to Conversion (WRITE)

	MODE
$\overline{WR} = 0$ in low address ($A_0 = 0$)	Full 12-Bit conversion
$\overline{WR} = 0$ in high address ($A_0 = 1$)	Short cycle 8-Bit conversion

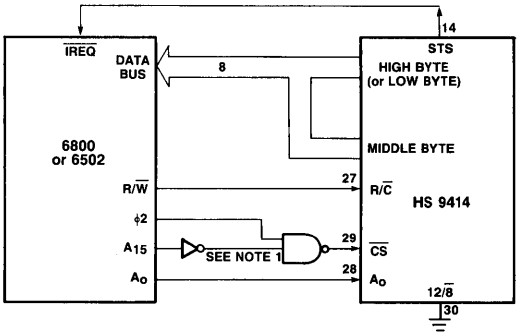
2. After Conversion (READ)

$\overline{WR} = 1$ in either address ($A_0 = X$)	Full 12-Bit word with $12/\overline{8} = 1$
$\overline{WR} = 1$ in high address ($A_0 = 1$)	LSB's & zeros when $12/\overline{8} = 0$
$\overline{WR} = 1$ in low address ($A_0 = 0$)	8 MSB's only when $12/\overline{8} = 0$

INTERFACING THE HS 9414 WITH 8-BIT MICROPROCESSORS

The HS 9414 which has 12-Bit data can be used directly with popular 8-Bit microprocessors. The data however, must be multiplexed by setting the output mode select 12/$\overline{8}$ pin to GND.

In the first case, a 6800 (or 6502) is used. See Figure 5.



NOTE 1. Decoding may be needed for a large system.

Figure 5. Interfacing the HS 9414 and a 6800 μP

The STATUS (STS) is tied directly to IREQ which is the interrupt line. When STS goes to 0 (at the end of a conversion) the 6800 may either service the interrupt or be timed for 30 μS (since this IREQ is software maskable) the time required for a conversion.

Figure 6 shows the 8080A μP as interfaced with the HS 9414. In this case, a 8228 controller is shown with gates to generate needed signals.

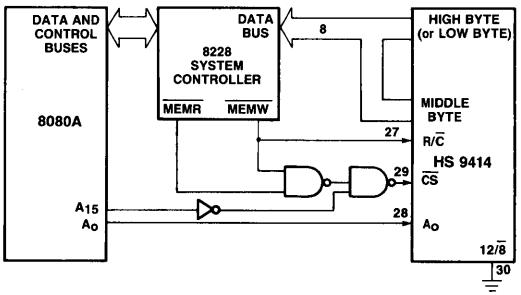


Figure 6. Interfacing the HS 9414 and 8080A μP

Figure 7 shows the HS 9414 connected with a 8048 μP. A single AND gate is used to generate $\overline{CS}$.

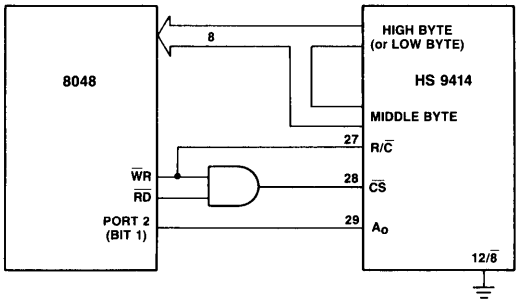


Figure 7. Interfacing the HS 9414 with a 8048 μP.

A summary of μP types and connections is in Table 4.

MICRO-PROCESSOR	HS 9414CONTROL INPUTS		
	R/C	CS	A_0
8080 MEMORY MAPPED I/O PROGRAMMED I/O	$\overline{(MEMR)}$ $\overline{(I/OR)}$	DECODED ADDRESS	A_0
6800	R/$\overline{W}$	DECODED ADDRESS	A_0
6502	R/$\overline{W}$	DECODED ADDRESS	A_0
Z80 MEMORY MAPPED I/O	$\overline{(RD)}$	DECODED ADDRESS WITH MREQ	A_0
PROGRAMMED I/O	$\overline{(RD)}$	DECODED ADDRESS WITH IOR	A_0
8048	$\overline{(RD)}$	PORT 2_{0-3}*	PORT 2_{0-3}*

*Port 2, Lines 0-3 can be used as a 4-Bit address bus. System address decoding requirements vary from no hardware to a fully latched 12-Bit address, depending on system complexity.

Table 4. Summary of HS 9414 Control Inputs with Various Microprocessors

ENABLING DATA IN 8-BIT OUTPUT MODE

For an 8-bit system Figures 5, 6 and 7 show no direct connection of the low bytes. Hybrid Systems has provided internal multiplexing prior to the output tri-state drivers of the MSB's and LSB's. During the READ cycle when $A_0 = 0$ the 8 MSB's are enabled and appear on pins 19-26. When $A_0 = 1$ the LSB's are multiplexed onto pins 23-26, pins 20-23 to "0", and pins 15-18 float (High Z). The LSB's may be hardwired directly to the MSB's (23-26) with no loss in system performance but this will decrease the system versatility.

A recap of the output data in an 8-bit system is as follows:

CONDITIONS

1. 12/$\overline{8}$ (pin 2) grounded or at "0"
2. READ cycle.

	OUTPUT		
A_0 State	23-26 (High)	19-22 (Middle)	15-18 (Low)
0	MSB Data (Bits 1-4)	Middle Bit Data (Bits 5-8)	Float (High Z)
1	LSB Data (Bits 9-12)	0's	Float (High Z)

USING THE $\overline{LATCH}$ LINE

The $\overline{LATCH}$ line controls the internal 4-Bit transparent latch that holds the input MUX channel number (MA0, MA1) and the gain selection word (GA0, GA1). A low (0) on this line updates this latch and a high (1) holds the new word.

If the system where the HS 9414 is being used already has fully implemented output ports, then the $\overline{LATCH}$ line may be hardwired low so that an output port may control the timing of the input MUX and SPGIA gain directly. (See Figure 8).

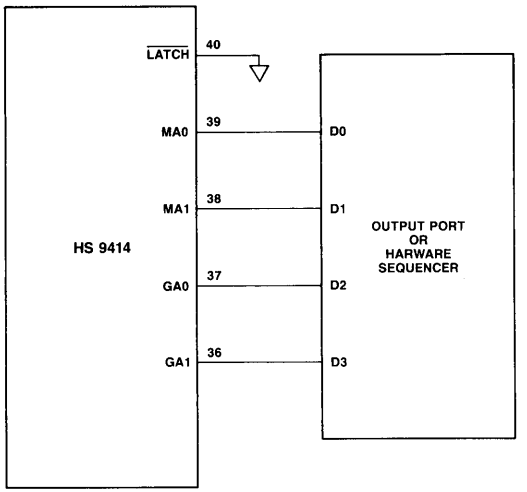


Figure 8.

If the system does not have available output ports for the input MUX channel and gain selection, then 4-Bits from the system data bus can be directly tied to the MA0, MA1, GA0 and GA1 lines. Port address control decoding circuitry is connected to the $\overline{LATCH}$ line so that the 4-Bit data is grabbed from the system bus at the proper time. (See Figure 9).

11

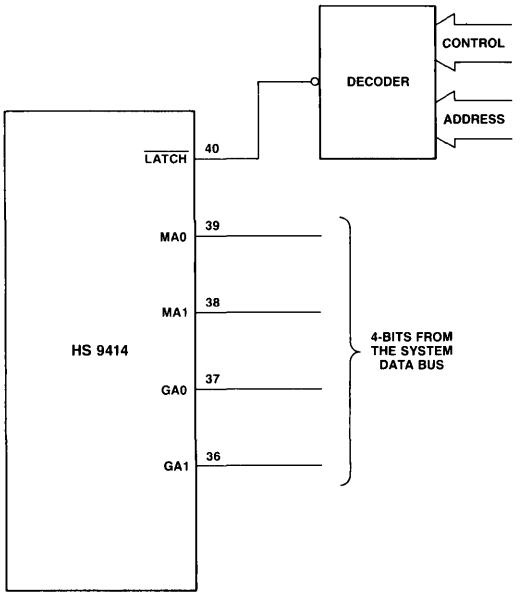


Figure 9.

OUTPUT OFFSET AND GAIN ADJUSTMENT AT GAIN = 1

The output offset and gain adjustments are used to calibrate the A/D section at a gain of one. The HS 9414 is normally used with external zero and gain calibration potentiometers. However, if maximum accuracy is not required, they may be omitted. If no trims are used, the gain of one calibration will be within approximately ±2 LSB zero offset error, and ± 12 LSB maximum full scale error. See Figure 2c & 2d for connection with no trims. If gain and zero adjustment potentiometers are used, they should be connected as shown in Figure 2a & 2b. The zero control has a range of about ±20 LSB, and the gain control has a range of about ± 13 LSB.

Proper gain and zero calibration requires great care and the use of extremely sensitive and accurate instruments. The voltage source used as a signal input must be very stable. It also should be capable of being set to within 1/10 LSB at both ends of its range.

The HS 9414's zero and gain adjustments are independent of each other if the zero (or offset) adjustment is made first.

SPGIA INPUT OFFSET ADJUSTMENT AT HIGH GAIN

The HS 9414 provides input offset adjustment to allow calibration of input offset errors to less than 5 μV (< ½ LSB @G = 500) at high gains. The initial offset error before calibration is typically less than 50 μV or 250 μV maximum at G = 500. This input offset error may be adequate in some applications, and input offset adjustment may be omitted. See Figure 2 for the various adjustment options.

Proper use of the input and output offset adjustment pots results in an offset free system regardless of SPGIA gain setting or input channel. This can be achieved by calibrating the A/D section output offset and gain adjustments first and the input offset second. After the input offset is adjusted at G = 500 the output offset at G = 1 may need a minor adjustment.

A/D CALIBRATION

1. Center input offset pot if used.
2. Set SPGIA gain to one.
3. Tie channel LO to analog ground (Pin 33) and apply the input voltage standard between HI and LO of that channel.
4. Make sure that the voltage standard is grounded externally only at the input channel LO.

ZERO ADJUSTMENT PROCEDURE

1. For unipolar ranges:
   a) Set input voltage precisely to + ½ LSB.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001.
2. For bipolar ranges:
   a) Set input voltage precisely to ½ LSB above −F.S.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001

GAIN ADJUSTMENT PROCEDURE

1. Set input voltage precisely to ½ LSB less than "all bits on" ideal value. Note that this is 1½ LSB less than nominal full scale.
2. Adjust gain control until converter is switching from 111111111110 to 111111111111.

Table 5 summarizes the zero and gain adjustment procedure, and shows the proper input test voltages used in calibrating the HS 9414.

SPGIA OFFSET CALIBRATION PROCEDURE

1. Calibrate the A/D section first.
2. Set the SPGIA gain to 500.
   a) Apply ½ LSB to the input channel via a 500:1 attenuator as shown in Figure 10 or via the external front end circuitry. ½ LSB at gain of 500 is 4.8 μV for 20V range units (HS 9414X-2) and 2.4 μV for 10V range units (HS 9414X-1).
   b) Unipolar configuration:
   Adjust input offset pot until converter is switching from 000000000000 to 000000000001
   c) Bipolar configuration:
   Adjust input offset pot until converter is switching from 100000000000 to 1000000000001

Voltage Range	Adjustment	Ideal Input Voltage Value				Adjust input to point where converter is just on the verge of switching between the two codes shown.[1]
		GAIN = 1	GAIN = 10	GAIN = 100	GAIN = 500	
0 to +10V	ZERO	1.22mV	0.122mV	12.2μV	2.4μV	000000000000
	GAIN	9.9963V	0.99963V	99.963mV	19.9926mV	111111111110
±5V	ZERO	−4.9988V	−0.49988V	−49.988mV	9.9976mV	000000000000
	GAIN	4.9963V	0.49963V	49.963mV	−9.9926mV	111111111110
±10V	ZERO	−9.9976V	−0.9976V	−99.976mV	−19.9952mV	000000000000
	GAIN	9.9927V	0.99927V	99.927mV	19.99859mV	111111111110

NOTE 1. Codes shown are natural binary for unipolar input ranges and offset binary for bipolar ranges.
The term "0" is the transition between a logic 0 and a logic 1 state.

Table 5. Calibration Data

POWER SUPPLY CONSIDERATION

Power supplies used for the HS 9414 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output codes may result with noisy power sources. It is important to remember that 5 μV is 1 LSB for a 10 volt range, at a gain of 500.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10 μF tantalum type in parallel with 0.1 μF disc ceramic type.

GROUNDING CONSIDERATIONS

To insure maximum accuracy, the HS 9414 has a separate analog and digital ground; these two grounds must be routed properly to prevent DC and transient errors.

DC errors can be caused by current flowing through a run resistance between the system ground reference and the DAS ground reference. (One mA through 2.5Ω will cause an LSB of error.) The best way to prevent this type of error is to connect the digital and analog grounds very close to the HS 9414 and use this point as the system ground. This can be done as a so-called "star ground" as shown in Figure 11. The single common ground reference insures no ground current or ground loop errors.

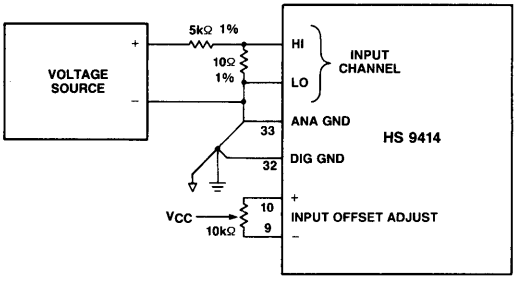


Figure 10. Suggested SPGIA Input Offset Calibration Circuit

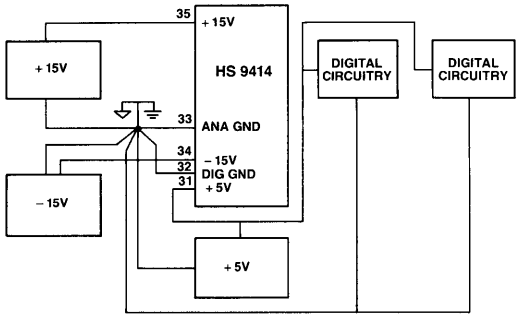


Figure 11.

ANALOG FRONT END

If the circuit is to be used at or near its maximum throughput rate, care must be used to prevent dynamic errors due to source impedance at the multiplexer inputs. If a low-pass anti-alias filter is used at the analog inputs (Figure 12a), it is suggested that a buffer be used (Figure 12b) to eliminate charge-transfer errors between C_{FILTER} and $C_{MUX,AMP}$ (Figure 12c).

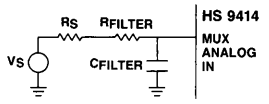


Figure 12a. (Not Recommended)

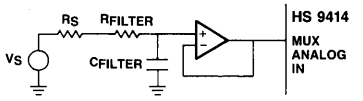


Figure 12b. (Recommended)

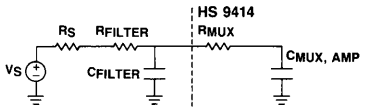


Figure 12c. (Equivalent Circuit of 12a)

The HI and LOW inputs for each channel are adjacent to each other in the package. This simplifies layout of closely spaced HI and LO lines and eases connection of shielded and twisted pairs for each channel. (See Figure 13). These wiring consideration are particularly important at high SPGIA gain settings. The close proximity and similarity of the HI and LO conductors also reduces thermoelectric errors due to Seebeck effect.

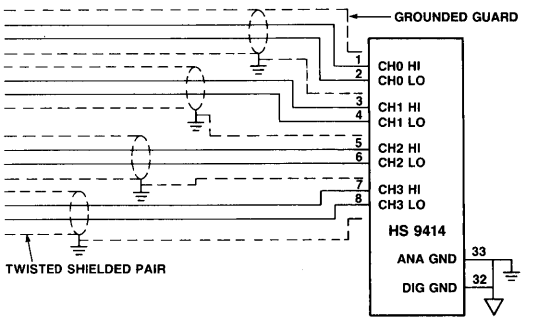


Figure 13. Recommended Input Wiring Layout

DYNAMIC PERFORMANCE CONSIDERATIONS

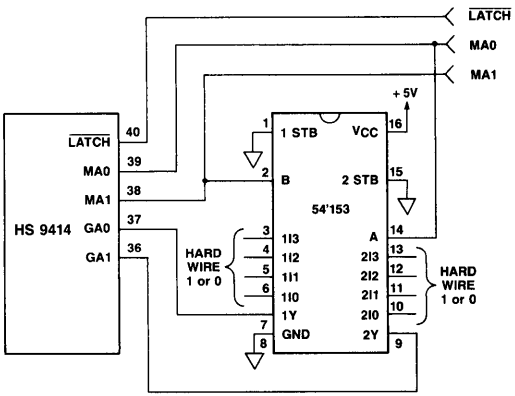
The analog signal path in the HS 9414 has a characteristic settling time for each gain setting. If maximum accuracy is desired, enough settling time for each gain setting must be allowed. If not, each new conversion may have vestigial amounts of signal from the previous conversion. This phenomenon also manifests itself as poor crosstalk performance among successively converted channels or input signals.

Coherent noise coupling and input MUX crosstalk is more detrimental at certain time slots of the DAS pipeline (Figure 4) than others. System coherent noise spikes and adjacent channel dynamic swings will affect the signal that is being converted more severely if they happen in the last 1 to 10 μs before the status line goes high.

When switching the SPGIA to a higher gain it is important to make sure that the input MUX is not switched to the new low level signal later than the gain. Momentary saturation may occur while the signal presented to SPGIA is still high level and the new gain is high.

FIXED GAIN ASSIGNMENT FOR EACH INPUT CHANNEL

The HS 9414 has four input channels and four independent gains. Any input channel can be software or hardware programmed for any gain in any sequence of DAS conversions. However, in some applications it suffices to preassign a fixed gain for each channel. This reduces the number of SPGIA control bits from four (MA0, MA1, GA0, GA1) to two (MA0, MA1). Figure 14 shows an implementation of this configuration using a dual 4-input multiplexer.



EXAMPLE:

2I0, 1I0 = 1,1 CH0 HAS GAIN OF 500
2I1, 1I1 = 0,0 CH1 HAS GAIN OF 1
2I2, 1I2 = 1,0 CH2 HAS GAIN OF 100
2I3, 1I3 = 0,1 CH3 HAS GAIN OF 10

INPUT CHANNEL	ASSIGNED GAIN AT:
CH0	2I0, 1I0
CH1	2I1, 1I1
CH2	2I2, 1I2
CH3	2I3, 1I3

Figure 14. Input Channel Assigned Gain

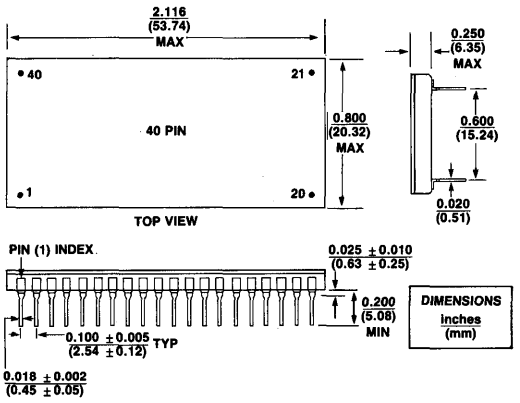
UNIPOLAR/BIPOLAR CONFIGURATION

The HS 9414-2 units are 20 volt range units which must be operated in bipolar configuration to give a ± 10V input signal range (for unity gain amplification). The HS 9414-1 units are 10 volt range units which can be operated in unipolar or bipolar modes. Refer to Figure 2 for various configurations.

INPUT EXPANSION

The DAS is configured with a 4-channel differential input. In the event the user wishes to increase the number of input channels, examples of input expansion are shown in Figure 15.

ADDR2	ADDR1	ADDR0	ACTIVE CHANNEL
0	0	0	NONE
0	0	1	±IN1
0	1	0	±IN2
0	1	1	±IN3
1	0	0	±IN4
1	0	1	±IN5
1	1	0	±IN6
1	1	1	±IN7



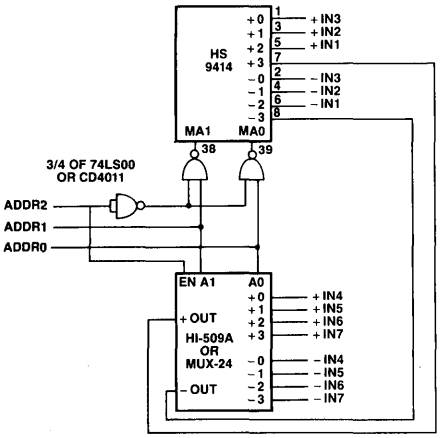


Figure 15. Input Expansion for HS 9414 (From 4 to 7 Channels)

ORDERING INFORMATION

MODEL NUMBER	INPUT RANGE	TEMPERATURE RANGE	SCREENING
HS 9414C-1	10V	0°C to +70°C	—
HS 9414C-2	20V	0°C to +70°C	—
HS 9414B-1	10V	−55°C to +125°C	883C
HS 9414B-2	20V	−55°C to +125°C	883C

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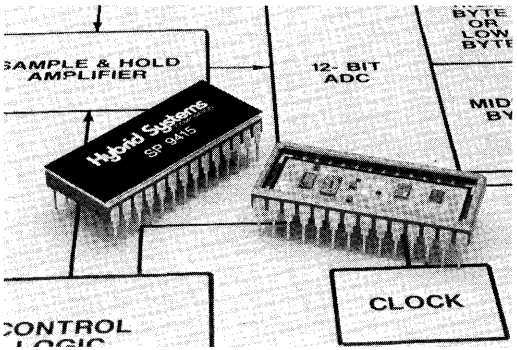
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP9415 SERIES

8-CHANNEL, 12-BIT, 75kHz DATA ACQUISITION SYSTEM

FEATURES

- Multiplexer, sample-and-hold, A/D in a compact 28-pin DIP
- Input overvoltage protection
- 75 kHz system throughput
- Three state output buffer
- Pin for pin compatible with HS9410 Series

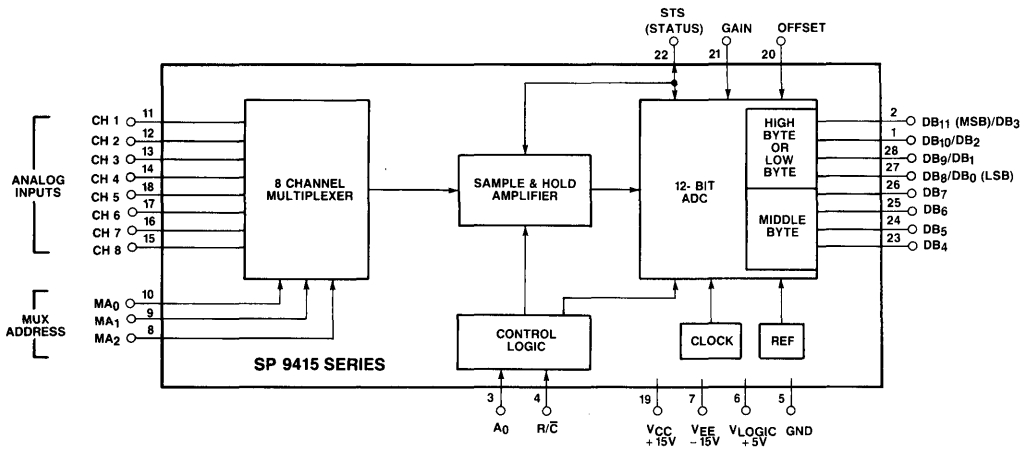


DESCRIPTION

The SP9415 Series is a complete 8-channel, microprocessor compatible, 12-bit data acquisition system with all the interface logic to connect directly to 8-or 16-bit microprocessor buses. Packaged in a ceramic, 28-pin DIP, the SP9415 Series includes an 8-channel multiplexer, 1 microsecond sample-and-hold-amplifier and a 15 microsecond, 12-bit A/D converter. Pin for pin compatible with the popular HS9410 Series, the SP9415 Series offers faster acquisition time, A/D conversion time and system throughput.

To take advantage of the 28-pin package the user must specify an input range of 0 to +10V, ±5V or ±10V when ordering. Four basic product grades are available; J and K models are specified over a temperature range of 0°C to +70°C while the S and T models are specified over an extended temperature range of −55°C to +125°C. Full screening to MIL-STD-883C is available.

FUNCTIONAL DIAGRAM



11

SPECIFICATIONS

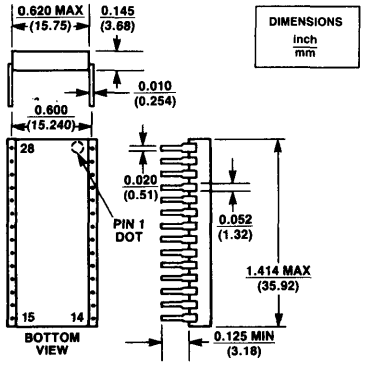
(Typical @ +25°C with V_{CC} = +15V, V_{EE} = −15V, V_{LOGIC} = +5V, unless otherwise specified.)

MODEL	SP 941XJ	SP 941XK	SP 941XS	SP 941XT
TRANSFER CHARACTERISTICS				
Resolution	12-Bits	*	*	*
Number of Channels	8 Single-Ended	*	*	*
Throughput Rate	75 kHz typ, 60 kHz min	*	*	*
ANALOG INPUTS				
Input Ranges[1] (Specified as a suffix in the model number. See Ordering Guide.)				
SP 9415	0 to +10V	*	*	*
SP 9416	±5V	*	*	*
SP 9417	±10V	*	*	*
Input Bias Current per Channel				
I_{IB} 25°C	±10nA	*	*	*
−55°C to +125°C			±250nA max	*
Input Impedance				
ON Channel	5MΩ ‖ 25pf	*	*	*
OFF Channel	5MΩ ‖ 5pf	*	*	*
DIGITAL INPUTS				
Logic Inputs				
R/C, A_0				
V_{IH}	+2.4V min	*	*	*
V_{IH}	+5.5V max	*	*	*
V_{IL}	+0.8V max	*	*	*
V_{IL}	−0.5V min	*	*	*
I_{IL}	±5μA max	*	*	*
I_{IH}	±5μA max	*	*	*
Multiplexer Inputs				
V_{IL}	+0.8V max	*	*	*
V_{IH}	+4.0V max[2]	*	*	*
Input Capacitance (All Digital Inputs)	5pF typ	*	*	*
Minimum Start Pulse				
R/C-Negative	50ns	*	*	*
SIGNAL DYNAMICS				
Acquisition Time (20V STep)				
0.1%	0.8μsec typ, 1.2μsec max	*	*	*
0.01%	1.0μsec typ, 1.5μsec max	*	*	*
Conversion Time				
12-Bit Conversion	12μs typ, 15μs max	*	*	*
8-Bit Conversion	8μs typ, 12μs max	*	*	*
DIGITAL OUTPUTS				
Logic Outputs				
DB_{11}-DB_0, STS				
Logic 0	+0.4V max, I_{OL} = 1.6mA	*	*	*
Logic 1	+2.4V min, I_{OH} = 0.5mA	*	*	*
Leakage (High Z State)	±5μA typ (DB_{11}-DB_0 only)	*	*	*
Capacitance	5pF typ	*	*	*
Output Code Configuration				
Unipolar	Positive True Binary	*	*	*
Bipolar	Positive True Offset Binary	*	*	*
POWER SUPPLY				
V_{LOGIC}	+4.5 to +5.5 Volts @ 5mA max	*	*	*
V_{CC}	+13.5 to +16.5 Volts @ 25mA max	*	*	*
V_{EE}	−13.5 to −16.5 Volts @ 10mA max	*	*	*
Power Dissipation	550mW max	*	*	*
Rejection[3]				
V_{LOGIC}	0.002%/% typ, 0.005%/% max	*	*	*
V_{CC}	0.002%/% typ, 0.005%/% max	*	*	*
V_{EE}	0.002%/% typ, 0.005%/% max	*	*	*
ACCURACY				
Linearity Error (% of F.S.R. max)	±0.025	±0.012	±0.025	±0.012
Offset[4]				
Unipolar (% of F.S.R.)	±0.05 typ, ±0.1 max	*	*	*
Bipolar (% of F.S.R. max)	±0.25	±0.1	±0.25	±0.1
Gain[4] (% to F.S.R. max)	±0.3	*	*	*
STABILITY				
Linearity (ppm/°C max)	±0.5	±0.5	±2.5	±2.5
Unipolar Offset (ppm/°C max)	±10	±5	±25	±20
Bipolar Offset (ppm/°C max)	±25	±20	±25	±20
Gain (Scale Factor)(ppm/°C max)	±50	±20	±50	±25
TEMPERATURE RANGE				
Operating	0° to +70°C	*	−55°C to +125°C	−55°C to +125°C
Storage	−25°C to +85°C	*	−65°C to +150°C	−55°C to +125°C

NOTES:
1. All models input may exceed supply voltages up to 70V_{pp} without permanent damage to device. 2. 1K pullup to +5V recommended for MA_0-MA_2 when driven by TTL. 3. Maximum change over rated supply voltage. 4. Externally adjustable to zero. See Applications Information.

*Specifications same as SP 9415J.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	DB_{10}/DB_2	28	DB_9/DB_1
2	DB_{11}(MSB)/DB_3	27	DB_8/DB_0
3	A_0	26	DB_7
4	R/C	25	DB_6
5	GROUND	24	DB_5
6	V_{LOGIC}	23	DB_4
7	V_{EE}	22	STS(STATUS)
8	MUX ADDRESS A_2	21	GAIN
9	MUX ADDRESS A_1	20	OFFSET
10	MUX ADDRESS A_0	19	V_{CC}
11	INPUT CH 1	18	INPUT CH 5
12	INPUT CH 2	17	INPUT CH 6
13	INPUT CH 3	16	INPUT CH 7
14	INPUT CH 4	15	INPUT CH 8

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Common GND . . . . . 0 to + 16.5V
V_{EE} to Common GND . . . . . 0 to − 16.5V
V_{LOGIC} to Common GND . . . . . 0 to + 7V
Control Inputs (A_0, R/C) to
Common GND . . . . . − 0.5V to V_{LOGIC} + 0.5V
Power Dissipation 1.6W
Lead Temperature, Soldering . . . . . 300°C, 10Sec
Maximum Input Voltage . . . . . V_{CC} + 20V
Minimum Input Voltage . . . . . V_{EE} − 20V
Analog Input Maximum Current 25mA

CONTROL FUNCTIONS

The SP 9415 Series contains control functions necessary to provide for microprocessor interface. All control functions are defined in Tables 1, 2, and 3.

Function	Definition	Function
R/$\overline{C}$	Read/Convert	1. ↯ initiates conversion. 2. Low (0) disconnects data bus. 3. High (1) initiates read.
A_0	Device Address	1. Selects conversion mode. 12-bits if low (0), 8-bits if high (1) when R/$\overline{C}$ ↯. 2. In read mode A_0 selects the output format. If low (0) then 8 MSB's (high and middle byte) or if high (1) then only low byte and trailing zeroes.
MA_0 MA_1 MA_2	Multiplexer Address	Select Channels 1-8 (see MUX Logic Table 3)

Table 1. Defining the Control Functions

Control Inputs		Operation
R/C	A_0	
↯	0	Initiates 12-bit conversion
↯	1	Initiates 8-bit conversion
1	0	Enables 8 MSB's (high byte)
1	1	Enables 4 LSB's (low byte) and 4 trailing zeros
0	X	Output data (DB) goes to high impedance state.

Table 2. Truth Table—Control Inputs

Mux Address Inputs			Channel Selected
A_2	A_1	A_0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

NOTES:
1. 1 indicates logic HIGH.
2. 0 indicates logic LOW.
3. X indicates don't care.
4. ↯ indicates operation commences on high to low transition.
5. MSB → XXXX (High Byte) XXXX (Middle Byte)
6. XXXX (Low Byte) ← LSB

Table 3. Truth Table—Multiplexer Address

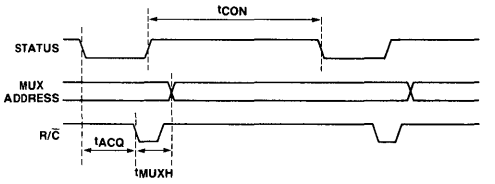
APPLICATIONS INFORMATION

TIMING

The timing diagrams are shown in Figures 1 through 6. Figures 1 and 2 show how the multiplexer addressing is related to the convert cycle, while Figures 3 and 4 show the timing sequence to start either a 12- or an 8-bit conversion. Figures 5 and 6 show how to read the multiplexed data from the internal register in the SP 9415.

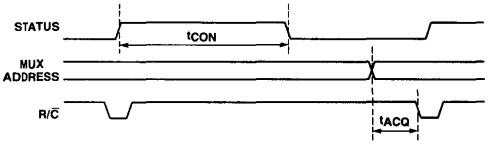
Figures 1 and 2

The multiplexer address can be changed either during or after a conversion, but care must be taken not to change the address within 1 microsecond after the convert command to insure that the sample/hold will not start to acquire the signal of the new channel. After the multiplexer address has been changed, you must allow the sample/hold at least 1.5 microseconds **in sample mode** to acquire the new input signal.



t_{MUXH}	Multiplexer address hold time after convert command	1μs min
t_{ACQ}	Minimum time between conversions (S/H acquisition time)	1.5μs min
t_{CON}	Conversion time for -12 bit resolution	15μs max
	- 8 bit resolution	12μs max

Figure 1. Timing Diagram 8/12-Bit Conversion, MUX Address Changes During Conversion

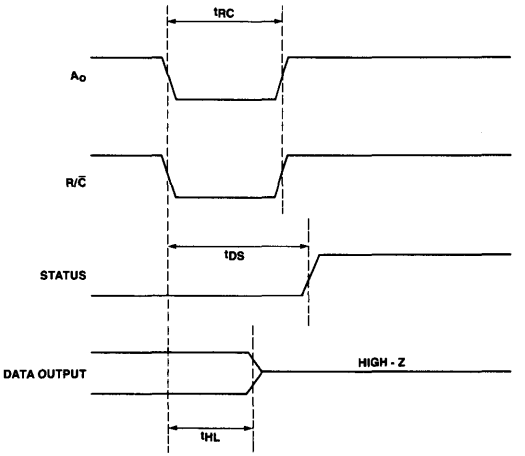


t_{ACQ}	Minimum time between MUX address change and convert command	1.5μs min
t_{CON}	Conversion time - Specification, see Figure 1	

Figure 2. Timing Diagram 8/12-Bit Conversion, MUX Address Changes Between Conversions

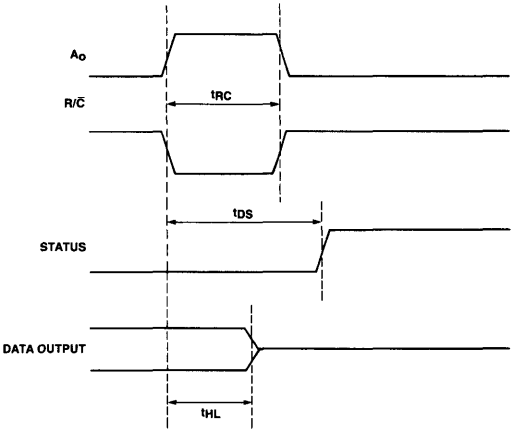
Figures 3 and 4

Figures 3 and 4 show how to start a convert cycle. The logic level of the A_0 line determines whether a 12- or 8-bit conversion will be initiated. If A_0 is low during the start convert command, a 12 bit conversion will be started; if A_0 is high, an 8-bit conversion will occur. The A_0 line has to be setup when the R/C line goes to logic '0' and must remain in the desired level for at least 50 ns. The R/C line is used both to start a conversion and to read the output data. If R/C is going low a conversion is initiated. This is indicated by the STATUS line going high. A second start convert command during a conversion will be ignored. The R/C pulse must have a minimum width of 50 ns. For optimum performance the rising edge of the R/C pulse should not occur during a conversion if the conversion has been in progress for more than 1 microsecond, i.e., the negative R/C pulse should be either shorter than 1 microsecond or longer than the conversion time.



t_{RC}	R/C pulse width, A_0 pulse width (Note 1)	50 ns min
t_{DS}	Status delay from R/C	200 ns max
t_{HL}	Output float delay	25 ns min

Figure 3. Timing Diagram to Start a 12-Bit Conversion

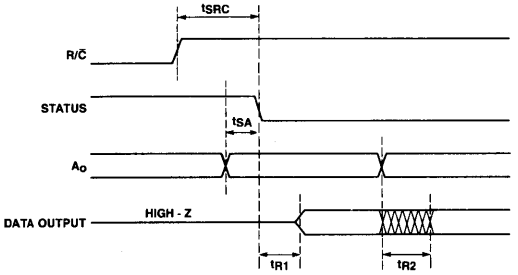


t_{RC}	R/C pulse width, A_0 pulse width (Note 1)	50 ns min
t_{DS}	Status delay from R/C	200 ns max
t_{HL}	Output float delay	25 ns min

Figure 4. Timing Diagram to Start an 8-Bit Conversion

Figures 5 and 6

If a conversion is in progress the data output lines are disabled and in the high-impedance state. Data can be enabled by bringing the R/C line high after a conversion is complete (this is indicated by the STATUS line going low; Fig. 6). If R/C has been returned high during a conversion the data outputs will be enabled automatically after STATUS goes low (Fig. 5). The A_0 line is used to address either the 8 upper data bits or the 4 lower data bits followed by 4 trailing zeros. If an 8-bit conversion has been performed the lower 4 bits will always be '0'. After an 8-bit conversion, it is not necessary to read the lower 4 bits prior to starting a new conversion. Note that A_0 only controls the address of the two data bytes while the high impedance state of the output buffers is controlled by the R/C and STATUS line. The output buffers will not return to the high impedance state when A_0 is changed to address the second data byte.

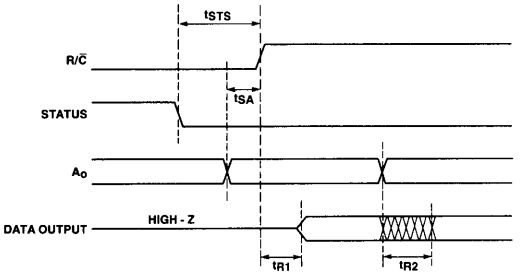


t_{SRC}	R/C set-up time prior to status going low	0 ns min
t_{SA}	A_0 set-up time prior to status going low (Note 2)	50 ns min
t_{R1}	Access time, 1st data byte (from status)	125 ns max
t_{R2}	Access time, 2nd data byte (from A_0)	225 ns max

Figure 5. Timing Diagram Read Cycle, R/C Going High During Conversion

NOTES:

1. For optimum performance the positive edge of the R/C pulse should occur during a conversion if the conversion has been started for more than 4.5 microseconds. The negative R/C pulse should be longer than 4.5 microseconds before the STATUS goes high.
2. If the set-up time for A_0 cannot be met, the access time for the first data byte will be increased. In that case the first data byte will become valid 225 ns max after the change of the A_0 line.



t_{STS}	Status going low prior to R/C going high	0 ns min
t_{SA}	A_0 set-up time prior to R/C going high (Note 2)	50 ns min
t_{R1}	Access time, 1st data byte (from R/C)	125 ns max
t_{R2}	Access time, 2nd data byte (from A_0)	225 ns max

Figure 6. Timing Diagram Read Cycle, R/C Going High After Conversion

USING THE A_0 LINE

The state of A_0 at the start of a conversion places the DAS in either a full 12-bit conversion or in an 8-bit 'short cycle' mode. During a READ at the end of a conversion A_0 is used to format the data as follows:

1. Prior to Conversion (WRITE)

	MODE
$A_0 = 1$	Short cycle 8-bit conversion
$A_0 = 0$	Full 12-bit conversion

2. After Conversion (READ)

$A_0 = 1$	Data = Low Byte (LSB) followed by zeros
$A_0 = 0$	Data = High Byte (MSB's) followed by middle byte.

In a μP application A_0 can be considered a pair of W/R locations as follows:

1. Prior to Conversion (WRITE)

	MODE
$\overline{W/R} = 0$ in low address ($A_0 = 0$)	Full 12-bit conversion
$\overline{W/R} = 0$ in high address ($A_0 = 1$)	Short cycle 8-bit conversion

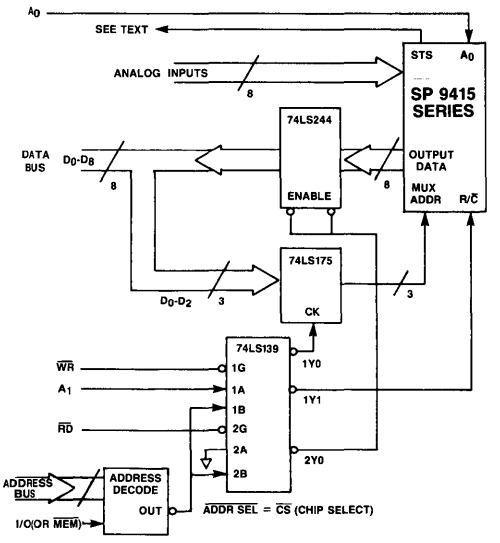
2. After Conversion (READ)

$\overline{W/R} = 1$ in high address ($A_0 = 1$)	LSB's & zeros
$\overline{W/R} = 1$ in low address ($A_0 = 0$)	8 MSB's only

MICROPROCESSOR INTERFACE

The SP 9415 Series DAS can be interfaced with most popular 8-bit microprocessors. The DAS may be either positioned in a memory location (memory map) or as an I/O device. In the case of memory mapping, the DAS acts as a static RAM where READ and WRITE instructions are given to the selected address. When the DAS is connected as an I/O device, the I/O enable can be substituted for the MEMR or MEMW command. Figure 7 shows a typical scheme to implement this interface.

STS is not used in this example; the μP must read data 15μs after conversion starts. This delay can be generated with NOP or other instructions inserted between the WRITE and READ functions. The STS line can also be used to cause the processor to WAIT or HALT or can be used as an interrupt line such as IREQ (in the case of 6800 or 6502).



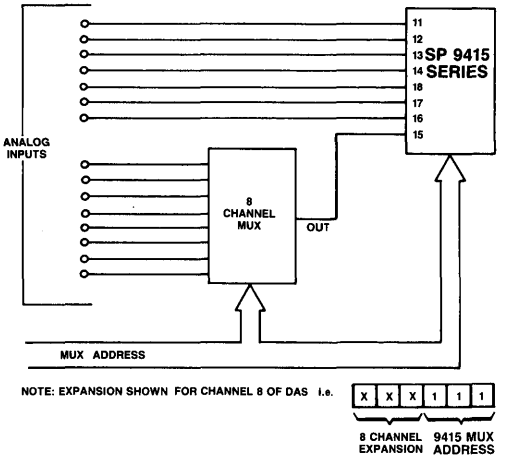
A_0	A_1	WR	RD	ADDR SEL	SP 9415 FUNCTION Read/Write	Operation
X	0	↑↓	1	0	WRITE	MUX ADDRESS
0	1	↓↑	1	0	WRITE	START 12-BIT CONV.
1	1	↓↑	1	0	WRITE	START 8-BIT CONV.
0	X	1	0	0	READ	HIGH BYTE (8 MSB's)
1	X	1	0	0	READ	LOW BYTE (4 LSB's)

NOTE:

1. 1 indicates logic HIGH.
2. 0 indicates logic LOW.
3. X indicates don't care.
4. ↓ indicates operation commences on low to high transition.
5. ↑ indicates operation commences on high to low transition.

INPUT EXPANSION

The DAS is configured with an 8 channel high level multiplexer input. This was done to optimize package size (28 pin DIP) and cost. In the event the user wishes to increase the number of input channels, a double rank MUX input is recommended (series connected). This typical configuration is shown in Figure 8.

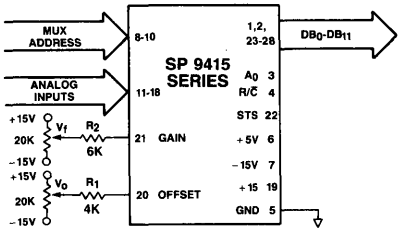


ZERO AND GAIN CONNECTIONS

The DAS is normally used with external zero and gain calibration potentiometers. However, if maximum accuracy is not required, they may be omitted. The zero control has a range of about ± 20LSB, and the gain control has a range of about ± 13LSB.

Proper gain and zero calibration requires great care and the use of extremely sensitive and accurate instruments. The voltage source used as a signal input must be very stable. It also should be capable of being set to within 1/10LSB at both ends of its range.

The DAS's zero and gain adjustments are independent of each other if the zero (or offset) adjustment is made first.



ZERO ADJUSTMENT PROCEDURE

1. For unipolar ranges:
   a) Set input voltage precisely to +½LSB.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001.
2. For bipolar ranges:
   a) Set input voltage precisely to ½LSB above – F.S.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001
3. When zero adjust is not performed pin 20 should be a no connect.

GAIN ADJUSTMENT PROCEDURE

1. Set input voltage precisely to ½LSB less than 'all bits on' value. Note that this is 1½LSB less than nominal full scale.
2. Adjust gain control until converter is switching from 111111111110 to 111111111111.
3. When gain adjust is not performed pin 20 should be a no connect.

Table 4 summarizes the zero and gain adjustment procedure, and shows the proper input test voltages used in calibrating the DAS.

Input Voltage Range	Adjustment	Input Voltage	Adjust input to point where converter is just on the verge of switching between the two codes shown.[1]
0 to +10V	ZERO	1.22mV	0000 0000 000Ø
	GAIN	9.9963V	1111 1111 111Ø
±5V	ZERO	–4.9988V	0000 0000 000Ø
	GAIN	4.9963V	1111 1111 111Ø
±10V	ZERO	–9.9976V	0000 0000 000Ø
	GAIN	9.9927V	1111 1111 111Ø

[1]Codes shown are natural binary for unipolar input ranges and offset binary for bipolar ranges.

Ø = transition between logic "1" and logic "0" state. All gain, offset and linearity measurements are performed using the transition test method.

Table 4. Calibration Data

POWER SUPPLY CONSIDERATION

Power supplies used for the DAS should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output codes may result with noisy power sources. It is important to remember that 2.44mV is 1LSB for a 10 volt input.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10μF tantalum type in parallel with 0.1μF disc ceramic type.

GROUNDING CONSIDERATIONS

The common at pin 5 is the ground reference point for the internal reference and is thus the high quality ground for the DAS. In order to achieve all of the high accuracy performance available from the DAS in an environment of high digital noise content, care should be taken when handling analog and digital grounds, as follows. Where analog and digital grounds are run separately on the PCB, these should be connected together at the package (pin 5). However, if the grounds are connected separately in the system for other reasons, then only the analog ground should be connected at the package to pin 5. If digital common contains high frequency noise beyond 200mV, this noise may feed through the converter, so that some caution will be required.

It is also important in the layout to carefully consider the placement of digital lines. It is recommended that digital lines not be run directly under the DAS. For optimum system performance, if space permits, a ground plane is advised under the DAS. This should be connected to a digital ground. Finally, in packaging the assembled DAS, the designer should also try to minimize any capacitive coupling that might occur at the top to the device.

ORDERING INFORMATION

Model Number[1]	Input Range	System Accuracy (% FSR)	Full Scale T.C. (ppm/°C)	Temp. Range	MIL Screening
SP 94XXJ	SEE NOTE 1	±0.025	50.0	0°C to +70°C	–
SP 94XXK		±0.012	20.0	0°C to +70°C	–
SP 94XXS		±0.025	50.0	−55°C to +125°C	–
SP 94XXT		±0.012	25.0	−55°C to +125°C	–
SP 94XXS/B		±0.025	50.0	−55°C to +125°C	883C
SP 94XXT/B		±0.012	25.0	−55°C to +125°C	883C

NOTES:

1. SP 94XX

MODEL SUFFIX	INPUT RANGE
15	0 to +10V
16	±5V
17	±10V

Add letter suffix as required above.

Specifications subject to change without notice.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance. Unused analog input channels should be tied to ground. If the gain and offset circuitry is not used, pins 20 and 21 should be floating with no "antenna" type runs attached, and if possible be surrounded by a ground plane. Unused digital inputs should be tied to ground 0V to +5V.

Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP9462
SP9463

12-BIT DATA ACQUISITION SYSTEM

FEATURES

- Complete 12-Bit Data Acquisition System
- Guaranteed No Missing Codes over Temperature
- Three State Output
- 33 kHz Throughput Rate
- Selectable Gains of 1, 10 and 100
- Small Pin Grid Array Package
- Low Power: 500 mW

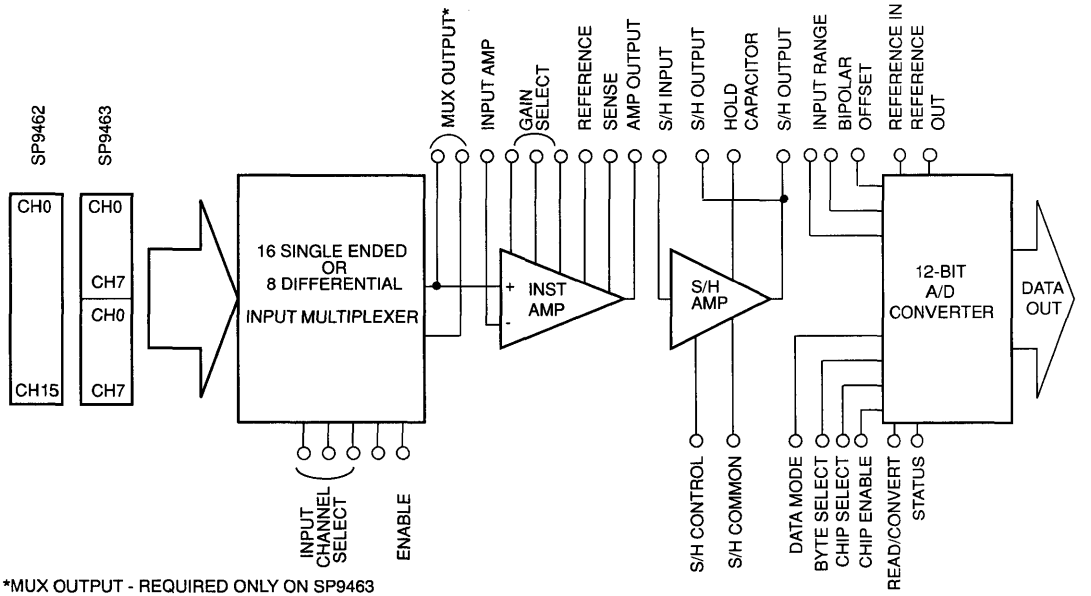
DESCRIPTION

The SP9462 and SP9463 are complete data acquisition systems in a 68 pin grade array package. The SP9462 includes a 16 channel input multiplexer, selectable gain instrumentation amplifier, sample and hold amplifier, a 12-Bit Analog to Digital Converter, and 3-state output buffers. The SP9463 is the 8 differential input channel device equivalent to the SP9462. The SP9462 and SP9463 will accept unipolar or bipolar voltage inputs of 0 to +10V, ±5V and ±10V. The instrumentation amplifier can be selected for gains of 1, 10 and 100 by pin-strapping pins. The

PRELIMINARY INFORMATION

SP9462 and SP9463 are available in three temperature ranges: 0 to +70°C, -25 to +85°C and -55 to +125°C, with MIL-STD-883C screening available.

FUNCTIONAL DIAGRAM



*MUX OUTPUT - REQUIRED ONLY ON SP9463

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SPECIFICATIONS

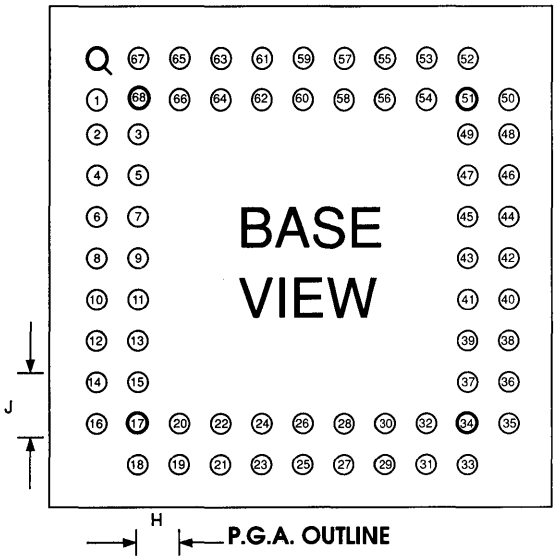
ELECTRICAL CHARACTERISTICS (Typical @25°C and Nominal Supply Voltages unless otherwise noted)					
PARAMETERS	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
ANALOG INPUTS					
Voltage Range			±5,±10,0 to +10		Volts
CMRR		80	85		dB
Crosstalk			-85	-80	dB
Feedthrough			-85	-80	dB
Offset[1]			30	100	µVolts
DIGITAL INPUTS					
Logic Levels	Logic 1	2.4			Volts
	Logic 0		0.4		Volts
Logic Loading			1		TTL Load
ACCURACY					
Integral Linearity				±0.012 (±0.024)*	% of FSR
Differential Linearity				±0.012 (±0.024)*	% of FSR
No Missing Codes				12	Bits
Gain Error (G=1)			0.7		%
Gain Error (G=100)			0.9		%
Unipolar Offset Error			16		mV
Bipolar Offset Error			50		mV
Droop Rate			50	500	µV/ms
CONVERSION & THROUGHPUT					
Throughput (Serial Mode)				45	µsec
A/D Conversion Time			20	25	µsec
S/H Acquisition Time			5		µsec
S/H Aperture Delay			50		nsec
S/H Aperture Jitter			2		nsec
STABILITY					
Unipolar Offset Tempco				15 (20)*	ppm/°C
Bipolar Offset Tempco				25 (30)*	ppm/°C
Gain Error Drift				35 (60)*	ppm/°C
DIGITAL OUTPUTS					
Coding					Straight Binary
Output Drive					TTL Loads
POWER SUPPLY REQUIREMENTS					
+15V			20	27	mA
-15V			10	18	mA
+5V Digital			10	14	mA
Dissipation			500	750	mW
TEMPERATURE RANGE					
J,K		0		70	°C
A,B		-25		+85	°C
R,S		-55		+125	°C

NOTES

*Spec in parenthesis is for J, A and R grades.

1. Gain = 1, all inputs grounded.

PACKAGE OUTLINE



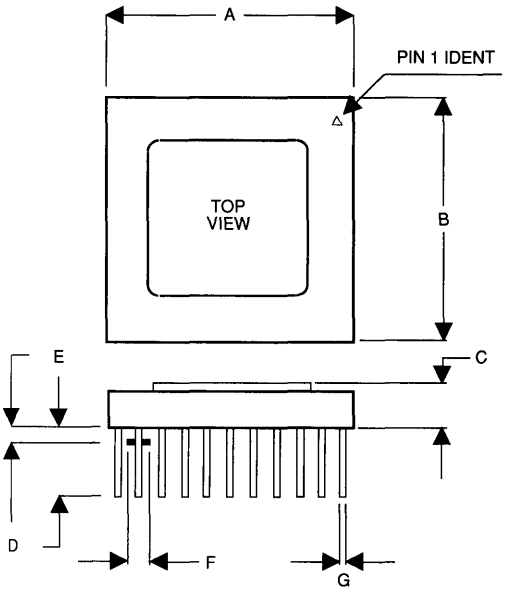
PIN ASSIGNMENTS

PIN	FUNCTION
1	Amp Out
2	Amp Ref
3	+15V (1)
4	–15V (1)
5	+5V
6	Status
7	D11
8	D10
9	D9
10	D8
11	D7
12	D6
13	D5
14	D4
15	D3
16	D2
17	D1
18	D0
19	ADC DCOM
20	-15V (2)
21	ADC In (20V)
22	ADC In (10V)
23	Bipolar Offset
24	Ref In
25	ACOM (2)
26	Ref Out
27	+15V (2)
28	$\overline{CE}$
29	R/C
30	$\overline{Data}$ Mode
31	$\overline{CS}$
32	Byte Select
33	S/H Control
34	S/H Common

PIN	FUNCTION
35	S/H Out
36	Hold Cap
37	S/H Out
38	NC
39	S/H In
40	CH7 (CH7+)*
41	CH6 (CH6+)*
42	CH5 (CH5+)*
43	CH4 (CH4+)*
44	CH3 (CH3+)*
45	CH2 (CH2+)*
46	CH1 (CH1+)*
47	CH0 (CH0+)*
48	Mux Enable
49	Mux Address 0
50	Mux Address 1
51	Mux Address 2
52	Mux Address 3 (NC)*
53	ACOM (1)
54	CH8 (CH0-)*
55	CH9 (CH1-)*
56	CH10 (CH2-)*
57	CH11 (CH3-)*
58	CH12 (CH4-)*
59	CH13 (CH5-)*
60	CH14 (CH6-)*
61	CH15 (CH7-)*
62	RG (Gain Range)
63	G10
64	G100
65	Mux Out+/Amp In+
66	Amp In-
67	NC (Mux Out-)*
68	Amp Sense

*Applicable to the SP9463

P.G.A. MECHANICAL OUTLINE



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.087	1.109	27.610	28.169
B	1.087	1.109	27.610	28.169
C	.115	.140	2.921	3.556
D	.162	.198	4.115	5.029
E	.045	.055	1.143	1.397
F	.045	.055	1.143	1.397
G	.016	.020	.406	.508
H	.100 BASIC		2.540 BASIC	
J	.100 BASIC		2.540 BASIC	

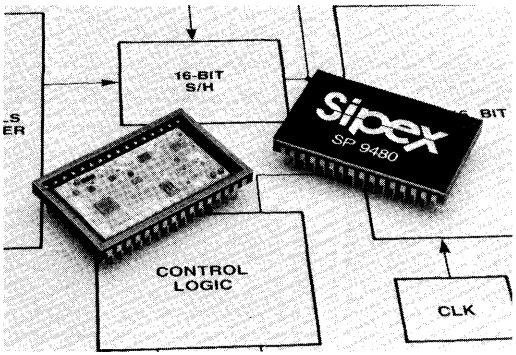
Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP9480 SERIES

8 CHANNEL, 16-BIT DATA ACQUISITION SYSTEM WITH μP INTERFACE

FEATURES

- Complete 8 channel, 16-bit data acquisition system with MUX, S/H, REF, clock and three-state outputs
- Full 8- or 16-bit microprocessor bus interface
- Guaranteed no missing codes 14-bit over temperature
- Hermetic 32-pin ceramic
- Low power: 1.2W

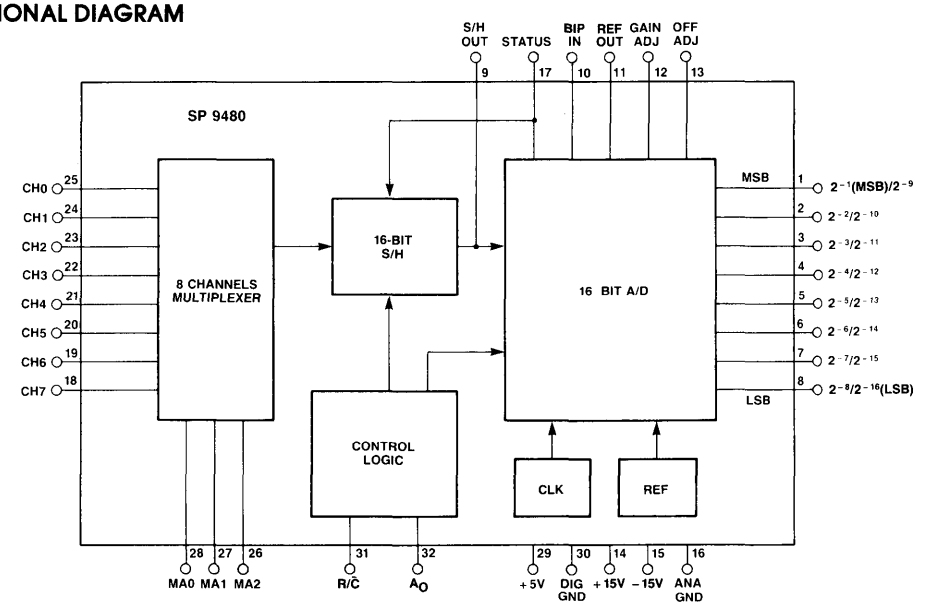


DESCRIPTION

The SP9480 Series is a complete 8 channel, microprocessor compatible, 16-bit data acquisition system with all the interface logic to connect directly to 8- or 16-bit microprocessor buses. Contained in a 32-pin DIP it includes an 8 channel multiplexer, sample-and-hold amplifier, and a 16-bit A/D converter along with the control logic needed to perform a complete data acquisition function. System throughput rate is 25kHz for full rated accuracy, output data is multiplexed and read as two bytes after conversion.

The SP9480 Series is offered in a hermetically-sealed 32-pin package and operates from ±15V and +5V with a total power consumption of 1200mW. Four basic product grades are available; J and K models are specified over a temperature range of 0°C to +70°C while the S/B and T/B models are specified over an extended temperature range of −55°C to +125°C. Full screening to MIL-STD-883C is available with models specified as "B."

FUNCTIONAL DIAGRAM



11

SPECIFICATIONS

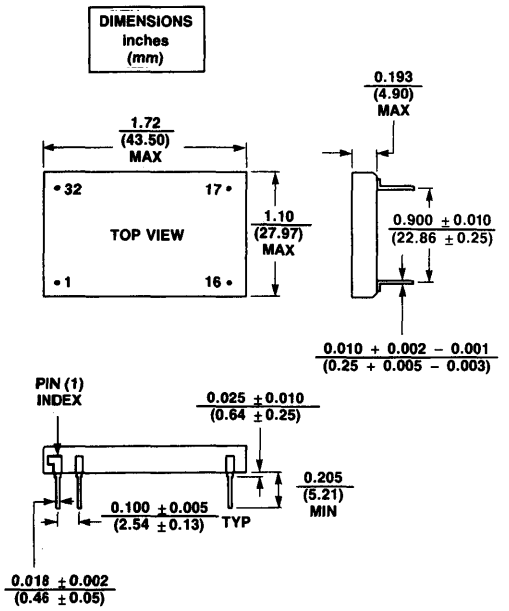
(Typical @ +25°C and nominal power supplies unless otherwise specified)

MODEL	SP 9480J	SP 9480K	SP 9480S/B	SP 9480T/B
RESOLUTION	16 Bits	*	*	**
ANALOG INPUTS				
Number of Channels	8 Single-Ended	*	*	**
Input Voltage Ranges				
Unipolar	0 to 10V	*	*	**
Bipolar	±10V			
Input Bias Current	70nA	*	*	**
Input Offset Current	30nA	*	*	**
Input Offset Voltage	2mV max	*	*	**
Input Voltage Noise (RTI)[1]	125μ VRMS[2]	*	*	**
Input Resistance	5MΩ	*	*	**
Input Capacitance				
OFF Channel	5pF	*	*	**
ON Channel	10pF	*	*	**
DIGITAL INPUTS				
$R/\overline{C}$, A_0				
Logic "1"	+2.0V min, +5.5V max	*	*	**
Logic "0"	0V min, +0.8V max	*	*	**
Logic Loading	1 LSTTL max	*	*	**
MA0, MA1, MA2				
Logic "1"	2.4V min	*	+4.0V min[3]	**
Logic "0"	0.8V max	*	*	**
Input Capacitance (All Digital Inputs)	5pF	*	*	**
DIGITAL OUTPUTS				
Logic Levels				
Logic "1"	+2.4V min	*	*	**
Logic "0"	+0.4V max	*	*	**
Leakage (High Z)	±1μA typ	*	*	**
Capacitance	4pF	*	*	**
Output Codes[4]				
Unipolar	TSB	*	*	**
Bipolar	TOB	*	*	**
Drive Capability	8 LSTTL	*	*	**
Status				
Logic "1" During A/D Conversion				
Drive Capability	2 LSTTL	*	*	**
STATIC PERFORMANCE[5]				
Integral Linearity Error[6]	±0.006% of FSR max	±0.003% of FSR max	±0.006% of FSR max	±0.003% of FSR max
Differential Linearity Error	±0.003% of FSR typ	*	*	**
	±0.006% of FSR max	*	*	**
Gain Error[7]	±0.05% typ	*	*	**
	±0.2% max	*	*	**
Unipolar Offset Error[7]	±0.05% of FSR typ	*	*	**
	±0.2% of FSR max	*	*	**
Bipolar Zero Error[7]	±0.05% of FSR typ	*	*	**
	±0.2% of FSR max	*	*	**
DYNAMIC PERFORMANCE				
A/D Conversion Time	20μs typ, 25μs max	*	*	**
Acquisition Time[8]	13μs min, 15μs max	*	*	**
Throughput Rate	25 kHz min	*	*	**
MUX Crosstalk ($20V_{p-p}$, 1kHz)	85dB	*	*	**
S/H Aperture Delay	25ns	*	*	**
S/H Droop Rate at 25°C	0.025μV/μs	*	*	**
S/H Droop Rate at Tmax	8.5μV/μs	*	*	**
Feedthrough[9] ($20V_{p-p}$, 1kHz)	120dB min	*	*	**
DRIFT CHARACTERISTICS				
Linearity	±3ppm/°C of FSR max	±2ppm/°C of FSR max	±3ppm/°C of FSR max	±2ppm/°C of FSR max
Guaranteed No Missing Codes	13 Bits (0 to +70°C)	14 Bits (0 to +70°C)	13 Bits (−55°C to +125°C)	14 Bits (−55°C to +125°C)
Gain	±20ppm/°C max	*	*	**
Offset				
Unipolar	±5ppm/°C of FSR max	*	*	**
Bipolar	±15ppm/°C of FSR max	*	*	**
+10V REFERENCE				
Output Current	2.5mA	*	*	**
Output Voltage	+10V ±10mV	*	*	**
POWER REQUIREMENTS				
Power Consumption	1.2W typ, 1.3W max	*	*	**
Rated Voltage Analog	±15V (±0.5V max)	*	*	**
Rated Voltage, Digital	+5V (±0.5V max)	*	*	**
Supply Current				
+15V	35mA max	*	*	**
−15V	39mA max	*	*	**
+5V	38mA max	*	*	**
Power Supply Rejection	0.001%/% (All Supplies)	*	*	**
Warm-Up Time	1 minute	*	*	**
TEMPERATURE RANGE				
Operating	0°C to +70°C	*	−55°C to +125°C	**
Storage	−25°C to +85°C	*	−65°C to +150°C	**

NOTES: 1. Referred to input. 2. Measured at the output of the sample/hold. 3. 1KΩ pullup to +5V recommended for MA0-MA2 when driven by TTL. 4. TSB = True Straight Binary; TOB = True Offset Binary. 5. Specifications refer to entire system from MUX input to A/D outputs. 6. End point definition. 7. Adjustable to zero. 8. Includes MUX switching and settling time and S/H acquisition time. 9. Measured at the output of the S/H with S/H in hold mode.

*Specifications same as SP 9480J. **Specifications same as HS 9476S/B.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	2^{-1}(MSB)/2^{-9}	17	STATUS
2	$2^{-2}/2^{-10}$	18	CH7
3	$2^{-3}/2^{-11}$	19	CH6
4	$2^{-4}/2^{-12}$	20	CH5
5	$2^{-5}/2^{-13}$	21	CH4
6	$2^{-6}/2^{-14}$	22	CH3
7	$2^{-7}/2^{-15}$	23	CH2
8	$2^{-8}/2^{-16}$(LSB)	24	CH1
9	S/H OUT	25	CH0
10	BIP IN	26	MA2
11	REF OUT	27	MA1
12	GAIN ADJ	28	MA0
13	OFF ADJ	29	+5V
14	+15V	30	DIG GND
15	−15V	31	R/$\overline{C}$
16	ANA GND	32	A_0

APPLICATIONS INFORMATION

INPUT RANGES

Two input ranges are selectable on the SP 9480:
— Unipolar 10V is obtained by connecting "S/H OUT" (pin 9) to "BIP IN" (pin 10).
— Bipolar 20V is obtained by connecting "BIP IN" (pin 10) to "REF OUT" (pin 11).

CONTROL FUNCTIONS

The SP 9480 Series contains control functions necessary to provide for microprocessor interface. All control functions are defined in Tables 1, 2, and 3.

Function	Definition	Function
R/$\overline{C}$	Read/Convert	1. ↓ initiates conversion. 2. Low (0) disconnects data bus. 3. High (1) initiates read.
A_0	Address	In read mode A_0 selects the byte to be read. If low (0) then the high byte (MSB's) is selected, if high (1) the low byte (LSB's) is selected.
MA_0 MA_1 MA_2	Multiplexer Address	Select Channels (CH0-CH7) (see MUX Logic Table 3)

Table 1. Defining the Control Functions

Control Inputs		Operation
R/$\overline{C}$	A_0	
↓	X	Initiates 16-bit conversion
1	0	Enables 8 MSB's (high byte)
1	1	Enables 8 LSB's (low byte)
0	X	Output data goes to high impedance state.

Table 2. Truth Table—Control Inputs

Mux Address Inputs			Channel Selected
MA_2	MA_1	MA_0	
0	0	0	CH0
0	0	1	CH1
0	1	0	CH2
0	1	1	CH3
1	0	0	CH4
1	0	1	CH5
1	1	0	CH6
1	1	1	CH7

NOTES:
1. 1 indicates logic HIGH.
2. 0 indicates logic LOW.
3. X indicates don't care.
4. ↓ indicates operation commences on high to low transition.

Table 3. Truth Table—Multiplexer Address

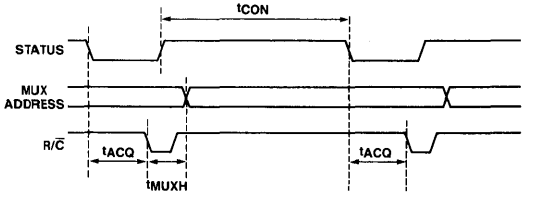
TIMING

The timing diagrams are shown in Figures 1 through 5. Figures 1 and 2 show how the multiplexer addressing is related to the conversion cycle while Figure 3 shows the timing reference to start a 16-Bit conversion. Figures 4 and 5 show how to read the multiplexed data from the SP 9480's internal register.

Figures 1 and 2

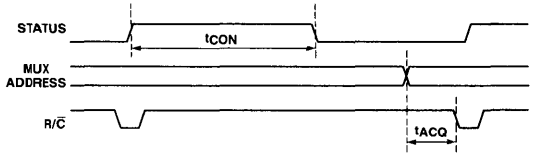
The multiplexer address can be changed either during (Figure 1) or after (Figure 2) a conversion. To improve the feedthrough performance of the device, the multiplexer is disabled during conversion. The consequence is that the sample/hold amplifier must stay in

sample mode at least 13 microseconds after the conversion is over to acquire the new input signal, **EVEN** if the multiplexer address has been changed during conversion. In other words, *"pipelining"* to increase throughput is not possible.



t_{MUXH}	Multiplexer address hold time after convert command	100ns min
t_{ACQ}	Minimum time between conversions (S/H acquisition time)	13μs min
t_{CON}	Conversion time for 16-Bit resolution J,K-Models	25μs max
	S,T-Models	25μs max

Figure 1. Timing Diagram 16-Bit Conversion, MUX Address Changes During Conversion

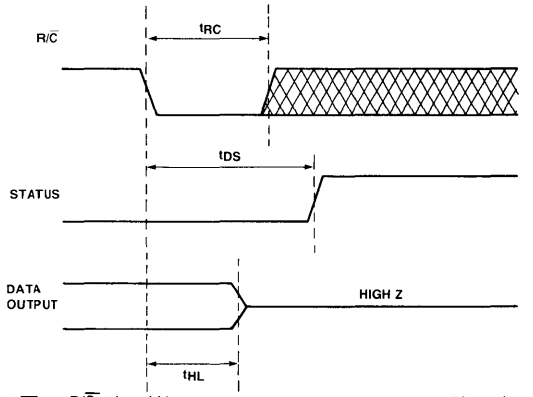


t_{ACQ}	Minimum time between MUX address change and convert command	13μs min
t_{CON}	Conversion time - Specifications, see Figure 1	

Figure 2. Timing Diagram 16-Bit Conversion, MUX Address Changes Between Conversions

Figure 3

Figure 3 shows how to start a conversion cycle. The R/$\overline{C}$ line is used both to start a conversion and to read the output data. If R/$\overline{C}$ is going low a conversion is initiated. This is indicated by the STATUS line going high. During a conversion R/$\overline{C}$ can stay low or go high again. The R/$\overline{C}$ pulse must have a minimum width of 50ns. For optimum performance the rising edge of the R/$\overline{C}$ pulse should not occur during a conversion if the conversion has been in progress for more than 1.5 microseconds, i.e., the negative R/$\overline{C}$ pulse should be either shorter than 1.5 microseconds or longer than the conversion time.

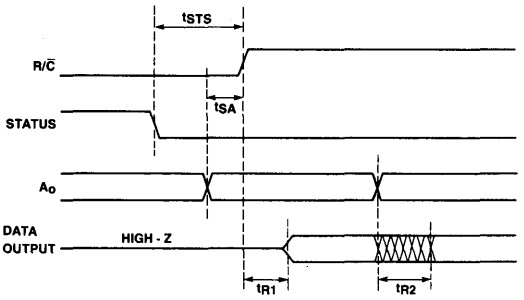


$t_{R\overline{C}}$	R/$\overline{C}$ pulse width	50 ns min
t_{DS}	STATUS delay from R/$\overline{C}$	30 ns max
t_{HL}	Output float delay	50 ns max

Figure 3. Timing Diagram to Start a 16-Bit Conversion

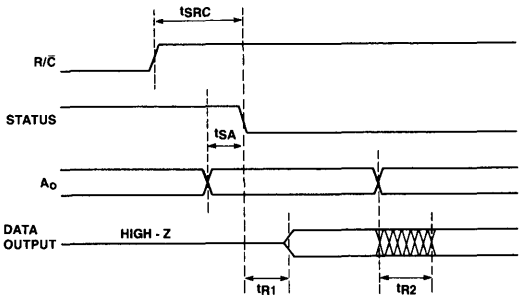
Figures 4 and 5

If a conversion is in progress the data output lines are disabled and in the high impedance state. Data can be enabled by bringing the R/$\overline{C}$ line high after a conversion is complete. This is indicated by the STATUS line going low (see Figure 4). If R/$\overline{C}$ has been returned high during a conversion the data outputs will be enabled automatically after STATUS goes low (Figure 5). The Ao line is used to address either the 8 upper data bits or the lower data bits. Note that Ao only controls the address of the two data bytes while the high impedance state of the output buffers is controlled by the R/$\overline{C}$ and STATUS line. The output buffers will not return to the high impedance state when Ao is changed to address the second data byte.



t_{STS}	STATUS going low prior to R/$\overline{C}$ going high	0 ns min
t_{SA}	Ao set-up time prior to R/$\overline{C}$ going high	10 ns min
t_{R1}	Access time, 1st data byte (from R/$\overline{C}$)	30 ns max
t_{R2}	Access time, 2nd data byte (from Ao)	30 ns max

Figure 4. Timing Diagram Read Cycle, R/$\overline{C}$ Going High After Conversion

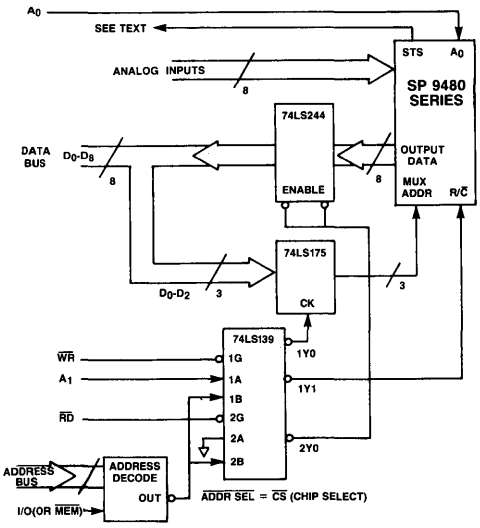


t_{SRC}	R/$\overline{C}$ set-up time prior to STATUS going low	0 ns min
t_{SA}	Ao set-up time prior to STATUS going low	10 ns min
t_{R1}	Access time, 1st data byte (from STATUS)	30 ns max
t_{R2}	Access time, 2nd data byte (from Ao)	30 ns max

Figure 5. Timing Diagram Read Cycle, R/$\overline{C}$ Going High During Conversion

MICROPROCESSOR INTERFACE

The SP 9480 Series DAS can be interfaced with most popular 8-Bit microprocessors. The DAS may be either positioned in a memory location (memory map) or as an I/O device. In the case of memory mapping, the DAS acts as a static RAM where READ and WRITE instructions are given to the selected address. When the DAS is connected as an I/O device, the I/O enable can be substituted for the MEMR or MEMW command. Figure 6 shows a typical scheme to implement this interface.



					SP 9480 Function	
A_0	A_1	$\overline{WR}$	$\overline{RD}$	ADDR SEL	Read/Write	Operation
X	0	⊓⊔	1	0	WRITE	MUX ADDRESS
X	1	⊓⊔	1	0	WRITE	START 16-BIT CONV.
0	X	1	0	0	READ	HIGH BYTE (8 MSB's)
1	X	1	0	0	READ	LOW BYTE (8 LSB's)

NOTE:

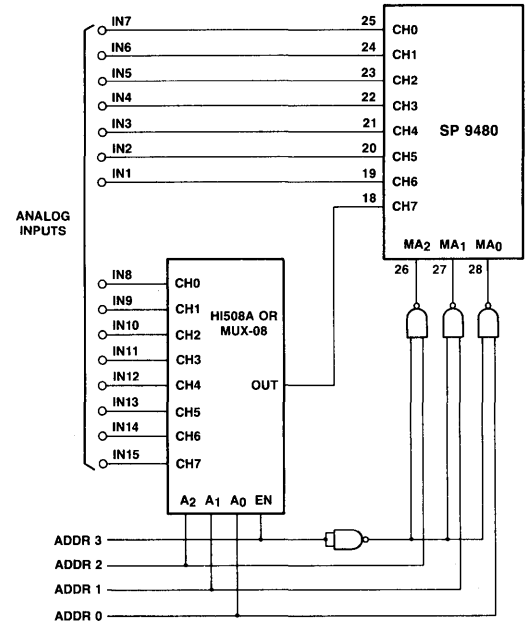
1. 1 indicates logic HIGH.
2. 0 indicates logic LOW.
3. X indicates don't care.
4. ⊓⊔ indicates operation commences on low to high transition.
5. ⊔⊓ indicates operation commences on high to low transition.

Figure 6. SP 9480 μP Interface

The STATUS line is not used in this example; the μP must read data 20μs typical after conversion starts. This delay can be generated with NOP or other instructions inserted between the WRITE and READ functions. The STATUS line can also be used to cause the processor to WAIT or HALT or can be used as an interrupt line such as IREQ (in the case of 6800 or 6502).

INPUT EXPANSION

The DAS contains a single 8 channel multiplexer. This was done to optimize package size (32 pin DIP) and cost. The expansion to 15 channels is possible by connecting an external multiplexer in *"series"* with the internal one. This typical configuration and its associated addresses are shown in Figure 7.



ADDR3	ADDR2	ADDR1	ADDR0	SELECTED INPUT
0	0	0	0	NONE
0	0	0	1	IN1
0	0	1	0	IN2
0	0	1	1	IN3
0	1	0	0	IN4
0	1	0	1	IN5
0	1	1	0	IN6
0	1	1	1	IN7
1	0	0	0	IN8
1	0	0	1	IN9
1	0	1	0	IN10
1	0	1	1	IN11
1	1	0	0	IN12
1	1	0	1	IN13
1	1	1	0	IN14
1	1	1	1	IN15

Figure 7. Multiplexer Expansion (15 Channels)

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OPTIONAL OFFSET ADJUST

The offset error may be trimmed to zero (optional) using an external offset trim potentiometer connected to the SP 9480 as shown in Figures 8 and 9.

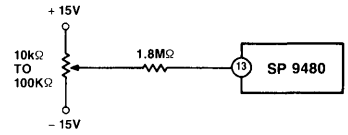

Figure 8. Offset Adjustment Circuit (± 0.4% FSR)

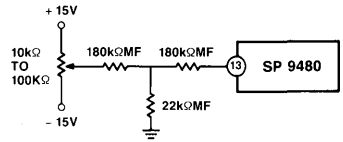

Figure 9. Low Tempco Offset Adjustment Circuit

The offset adjustment circuit shown in Figure 8 consists of a 100ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 1.8MΩ resistor to pin 13. In this case a carbon composition resistor is adequate: if we assume that its tempco is 1200ppm/°C and that the adjustment range required is no more than 16 LSB_{14} (0.1% of FSR), it contributes for only 1.17ppm/°C of offset tempco (0.001 x 1200). The low tempco adjustment circuit of Figure 9 contributes for negligible offset tempco if metal film resistors (tempco <100ppm/°C) are used.

With both circuits the fixed resistor connected to pin 13 should be located close to the converter to keep the pin connection runs short. Offset should be adjusted after warm-up and before gain (see below) to prevent interaction of the two adjustments. Offset is adjusted with the analog input near the most negative end of the analog range. Refer to Table 4 for the appropriate values.

OPTIONAL GAIN ADJUST

The gain error may be trimmed to zero (optional) using an external trim potentiometer connected to the SP 9480 as shown in Figure 10.

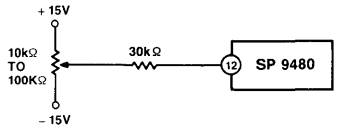

Figure 10. Gain Adjustment Circuit (± 0.3% FSR)

The gain adjustment circuit shown in Figure 10 consists of a 100ppm/°C potentiometer connected across the analog supply voltages with its slider connected through a 30kΩ resistor to pin 12. Gain should be adjusted after warm-up and after offset (see above) to prevent interaction of the two adjustments. Gain is adjusted with the analog input near the most positive end of the analog range. Refer to Table 4 for the appropriate values.

Input Voltage Range	Adjustment	Input Voltage	Adjust potentiometers to point where converter is just on the verge of switching between the two codes shown.*
0 to + 10V	OFFSET	0.0003V ($\frac{1}{2}LSB_{14}$)	000000000000 000000000001
	GAIN	9.9991V (10V - 3/2LSB_{14})	111111111110 111111111111
- 10V to + 10V	OFFSET	- 9.9994V (-10V + $\frac{1}{2}LSB_{14}$)	000000000000 000000000001
	GAIN	+ 9.9982V (10V - 3/2LSB_{14})	111111111110 111111111111

*Note: The codes shown are 14-bit codes. The adjustment will be 14-bit accurate.

Table 4. Calibration Data

POWER SUPPLY CONSIDERATIONS

Power supplies used for the SP 9480 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output codes may result with noisy power sources. It is important to remember that 610 μV is 1 LSB_{14} for a 10 volt range.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable capacitors are 10 μF tantalum types in parallel with 0.1 μF disc ceramic types.

GROUNDING CONSIDERATIONS

To ensure maximum accuracy, the SP 9480 has a separate analog and digital ground, which must be routed properly to prevent DC and transient errors. DC errors can be caused by current flowing through a run resistance between the system ground reference and the SP 9480 ground reference (1mA through 0.6Ω will cause an LSB_{14} of error). The best way to prevent this type of error is to connect the digital and analog grounds very close to the SP 9480 and use this point as the system ground. This can be done as a so-called "star ground" as shown in Figure 11. The single common ground reference ensures no ground current or ground loop errors.

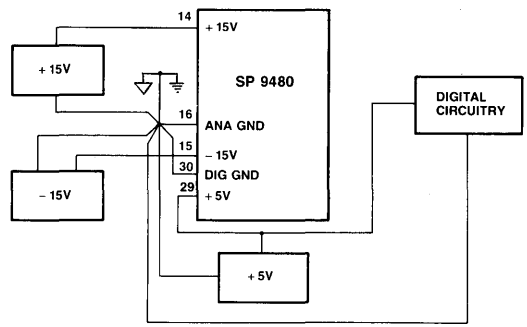

Figure 11. Grounding the SP 9480

DYNAMIC PERFORMANCE

The accuracy performance of the SP 9480 is specified statically. In certain applications, however, it can be important to know how well it digitizes "fast" moving signals.

Following the Nyquist theorem, the fastest signal the SP9480 can digitize is 12.5kHz (throughput/2) when **one** channel is used. If the eight channels are looked at successively, the maximum frequency of the input signal is 1.56kHz (12.5/8).

The most common way of characterizing a converter dynamically is performing a Signal to Noise Ratio (SNR) test, which quantifies Integral Linearity under dynamic conditions. In this test a finite time sequence of sampled data from a spectrally pure sine wave input is computed by the tester into a frequency spectrum using a Fast Fourier Transform algorithm. From this frequency domain representation of the output data, the effect of Integral Non-Linearity may be measured: harmonics of the input sine wave caused by I.L. errors are aliased into the baseband spectrum. The magnitude of the fundamental's spectral lines (the signal) is summed, then divided by the sum of the remaining spectral lines (the noise). The logarithm of this number multiplied by 20 provides the SNR expressed in decibels. For an ideal converter, it can be shown that:

$$SNR = 6.02 \times N + 1.76 \text{ dB}$$

(N = number of bits of the converter)

For a 14 bit converter the SNR should be 86dB. If the linearity error is ±1/2 LSB, a SNR of 3dB less is expected.

Figure 12 shows the behavior of the SP 9480 with a 1.123kHz sine wave input: the accuracy is 14 bits.

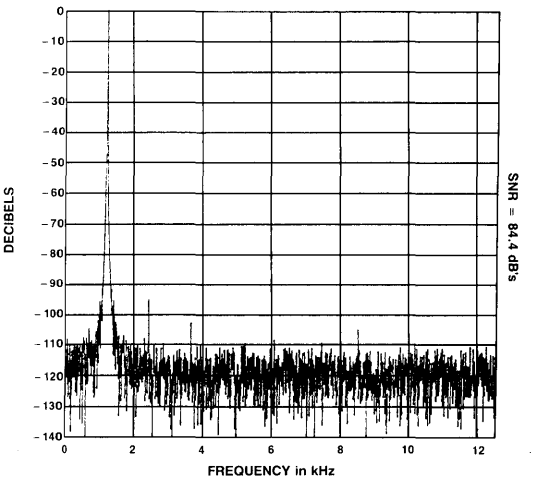

Figure 12. FFT of the SP9480, Fin = 1.123kHz, Fsample = 25kHz

ORDERING INFORMATION

MODEL	LINEARITY ERROR	TEMPERATURE RANGE	SCREENING
SP9480J	±0.006%	0°C to 70°C	—
SP9480K	±0.003%	0°C to 70°C	—
SP9480S/B	±0.006%	−55°C to +125°C	MIL-STD-883C
SP9480T/B	±0.003%	−55°C to +125°C	MIL-STD-883C

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Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

SP9488

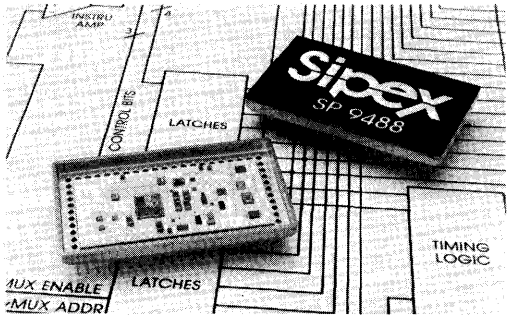
16-BIT
µP CONTROLLED DATA ACQUISITION SYSTEM

FEATURES

- Integral Linearity - 0.001% FSR
- Differential Linearity - 0.003% FSR
- High CMRR - 80 dB min.
- High Throughput - 50 kHz

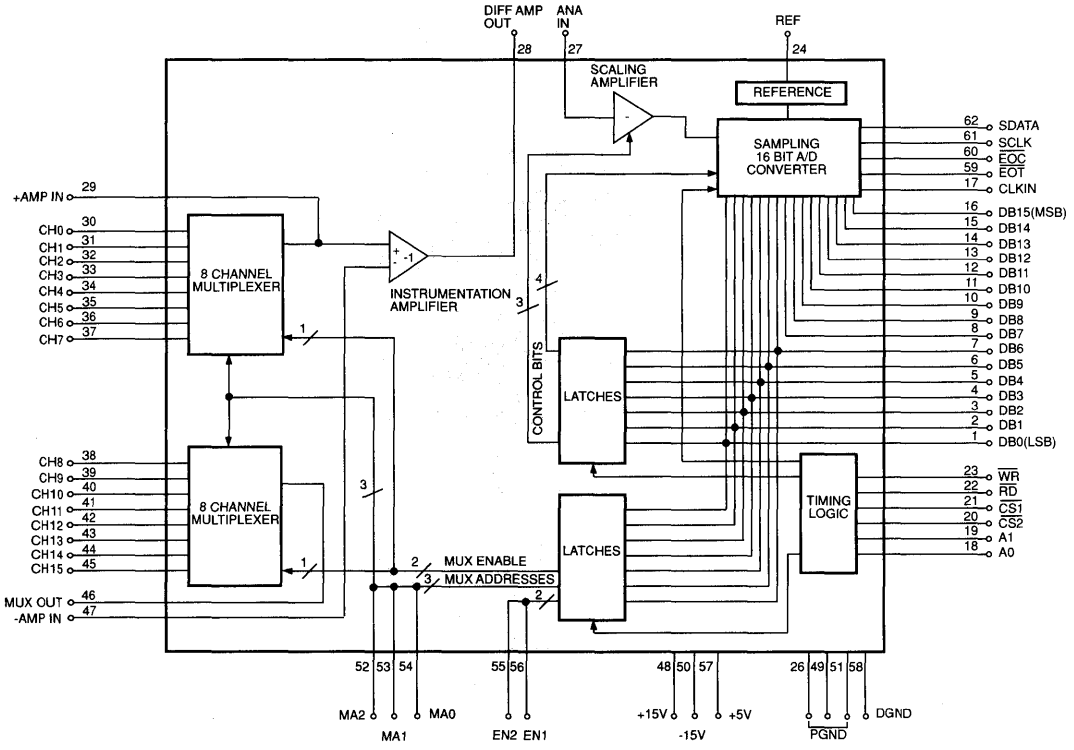
DESCRIPTION

The SP9488 provides complete 16-bit data acquisition functionality in a single 62 pin package. It includes user selected 8 differential or 16 single-ended input channel multiplexing, an instrumentation amplifier with gain of 1 and a self calibrating 16-bit sampling A/D converter. Different modes and ranges (bipolar 20V, 10V and 5V; unipolar 10V, 5V and 2.5V) are digitally selectable. The SP9488 is suited for intelligent (microprocessor based) applications. A "shared" 16-bit data bus reads the result of a conversion or the status word of the A/D, writes control bits to the A/D and selects a new input signal. The



SP9488 is offered in a 62 pin hermetically sealed package. Temperature ranges available are 0 to 70°C for commercial versions and -55 to +125°C with MIL-STD-883 Rev C screening for military grades.

FUNCTIONAL DIAGRAM



(Typical @ +25°C and nominal power supplies unless otherwise specified)

MODEL	SP9488C	SP9488B
ANALOG INPUTS		
Number of Channels	User selectable 16 SE or 8 DI	*
Input Voltage Range[1]		
Unipolar	0 to +2.5V, 0 to +5V, 0 to +10V	*
Bipolar	-10V to +10V, -5V to +5V, -2.5V to +2.5V	*
Common Mode Voltage	±11V min	*
CMRR (1 kHz, 20 Vp-p)	80 dB min	*
Multiplexer Crosstalk	80 dB typ	*
Inputs Bias Current	50 nA max	*
Input Offset Current	20 nA max	*
Input Offset Voltage	1 mV max	*
Input Impedance	11 GOhm	*
Full Power Bandwidth	25 kHz	*
DIGITAL INPUTS		
High Level Input Voltage	2.0V min	*
Low Level Input Voltage	0.8V max	*
Input Current	10 µA max	*
DIGITAL OUTPUTS		
High Level Output Voltage	3.75V min	*
Low Level Output Voltage	0.4V max	*
Tri-State Leakage Current	±10 µA max	*
Digital Output Pin Capacitance	9 pF typ	*
Output Coding		
Unipolar	Straight Binary	*
Bipolar	Offset Binary	*
Output Drive	8 LSTTL Loads	*
SWITCHING CHARACTERISTICS		
Refer to the "THEORY OF OPERATION" section for details.		
STATIC PERFORMANCE		
Integral Linearity Error[2]	±0.001% of FSR typ, ±0.002% of FSR max	*
Differential Linearity Error	±0.003% of FSR max	*
Gain Error[3]	±0.03% typ, ±0.1% max	*
Unipolar Offset Error[3]	±0.02% of FSR typ, ±0.05% max	*
Bipolar Offset Error[3]	±0.03% of FSR max, ±0.1% max	*
Noise	0.9 LSB 16 bit RMS typ	*
CONVERSION and THROUGHPUT		
Throughput[4]	50 kHz max	*
A/D Conversion Time[5]	16 µs typ	*
S/H Acquisition Time[5]	3 µs typ	*
Front End Acquisition Time[6]	15 µs typ	*
DRIFT CHARACTERISTICS		
Integral Linearity Error (t_{MIN}-t_{MAX})	±0.003% of FSR max	*
Differential Linearity (t_{MIN}-t_{MAX})	No Missing Codes 15-Bits	*
Gain	±15 ppm/°C max	*
Unipolar Offset	±5 ppm of FSR/°C max	*
Bipolar Offset	±10 ppm of FSR/°C max	*
POWER REQUIREMENTS[7]		
Current Drains		
+15V	50 mA max	*
-15V	40 mA max	*
+5V	10 mA max	*
Power Consumption	1.4W max	*
PSRR (All Supplies, Any Range and Mode)	0.001% of FSR/% of V_{supply} max	*
TEMPERATURE RANGE		
Operating	0°C to 70°C	-55°C to +125°C
Storage	-65°C to +150°C	*

NOTES

*Same as SP9488C

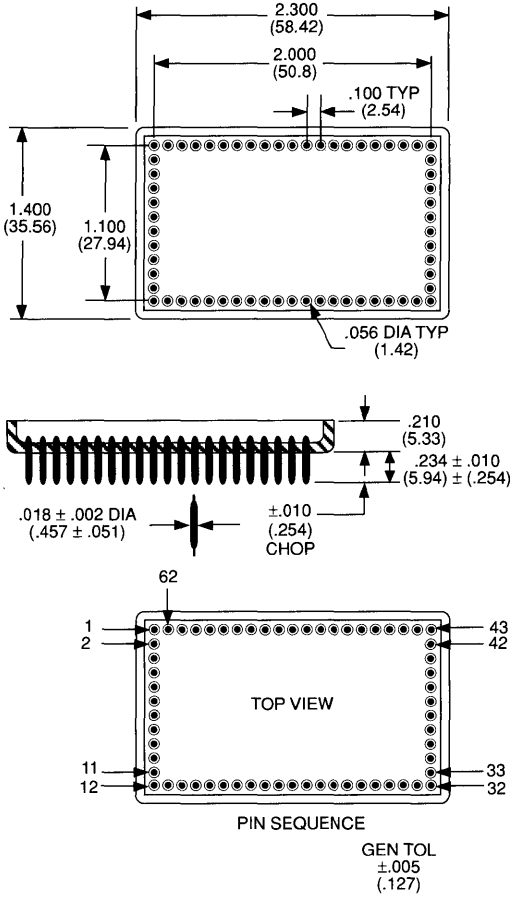
1. Digitally selectable by the user.
2. End point definition.
3. Specification valid for any selectable ranges. Assumption is made that Pins 27 and 28 are tied together.
4. Throughput specified when the pipeline technique is used to acquire the new input signal. A 4 MHz external clock and synchronous sampling are assumed to be used.
5. A 4 MHz external clock and synchronous sampling are assumed to be used. The conversion time is defined as the time between the falling edge on $\overline{WR}$ and the falling edge on $\overline{EOC}$.
6. Includes the settling time of the multiplexers, instrumentation amplifier and scaling amplifier.
7. The +5V supply should not be applied before the ±15V supply. Otherwise, latch up condition may occur.

PIN ASSIGNMENTS

PIN #	FUNCTION
1	DB0 (LSB)
2	DB1
3	DB2
4	DB3
5	DB4
6	DB5
7	DB6
8	DB7
9	DB8
10	DB9
11	DB10
12	DB11
13	DB12
14	DB13
15	DB14
16	DB15 (MSB)
17	CLK IN
18	A0
19	A1
20	$\overline{CS2}$
21	$\overline{CS1}$
22	$\overline{RD}$
23	$\overline{WR}$
24	REF
25	Reserved
26	PGND-2
27	ANA IN
28	DIFFAMP OUT
29	+AMP IN
30	CH0
31	CH1
32	CH2
33	CH3
34	CH4
35	CH5
36	CH6
37	CH7
38	CH8
39	CH9
40	CH10
41	CH11
42	CH12
43	CH13
44	CH14
45	CH15
46	MUX OUT
47	-AMP IN
48	+15V
49	PGND-1
50	-15V
51	PGND-3
52	MA2
53	MA1
54	MA0
55	EN2
56	EN1
57	+5V
58	DGND
59	$\overline{EOT}$
60	$\overline{EOC}$
61	SCLK
62	SDATA

PACKAGE OUTLINE

(DIMENSIONS IN INCHES (mm))



ABSOLUTE MAXIMUM RATINGS

+15V to PGND
(Positive Analog Supply) ..... +18V
-15V to PGND
(Negative Analog Supply) ..... -18V
+5V to DGND (Digital Supply) 5.8V
Analog Input Voltage ..... Analog Supplies +20V
Digital Input Voltage ..... Digital Supply

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	SCREENING
SP9488C	0°C to 70°C	—
SP9488B	-55°C to +125°C	MIL-STD-883C

PIN DESCRIPTION

The description given in this paragraph is not exhaustive: a more complete explanation of how to use the different pins is done in the "THEORY OF OPERATION" chapter.

A. Power Pins:

- +15V (pin 48): positive analog power supply. Nominally +15V.
- -15V (pin 50): negative analog power supply. Nominally -15V.
- PGND (pins 26, 49 and 51): analog ground reference. These three pins must be tied together close to the package.
- +5V (pin 57): positive digital supply. Nominally +5V.
- DGND (pin 58): digital ground reference.

B. Analog Pins:

1. Inputs:

- CH0 to CH15 (pins 30 to 45): analog inputs channels of the SP9488. They can be used individually as single-ended channels or in pair as differential inputs.
- +AMP IN and -AMP IN (pins 29 and 47): non-inverting and inverting inputs of the instrumentation amplifier. These pins used with MUX OUT (pin 46) permit the choice between single-ended and differential configuration for the input multiplexers of the SP9488.
- ANA IN (pin 27): A/D input of the SP9488. This signal generally comes from the DIFFAMP OUT pin (pin 28) and can be either a bipolar 20V, 10V or 5V, or a unipolar 10V, 5V or 2.5V following the mode and range selected digitally.

2. Outputs:

- MUX OUT (pin 46): output of one of the multiplexers of the SP9488. Used with +AMP IN and -AMP IN (pins 29 and 47), this pin permits the choice between single-ended and differential configuration for the input multiplexers of the SP9488.
- DIFFAMP OUT (pin 28): output of the instrumentation amplifier. This pin is generally tied to ANA IN (pin 27), unless a filter, a PGA, etc., is used between the output of the instrumentation amplifier and the A/D input.
- REF (pin 24): output of the internal reference of the sampling A/D (4.5V). A 0.47µF tantalum capacitor must be tied to this pin. This output can not be used for other purposes without being buffered.
- Pin 25: this pin is reserved for factory use. It must be left open for the correct operation of the SP9488.

C. Digital Pins:

1. Inputs:

- CLKIN (pin 17): all conversions and calibrations are timed from a master clock which can be either supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND (pin 58).
- A0, A1, $\overline{CS2}$, $\overline{CS1}$, $\overline{RD}$, $\overline{WR}$ (pins 18 to 23): control inputs for the proper management of the Data Bus (pins 1 to 16) of the SP9488.

2. Outputs:

- DB0 to DB15 (pins 1 to 16): bidirectional Data Bus. It can carry FROM the SP9488 the result of a conversion or a status word of the A/D. It can carry TO the SP9488 control bits to the A/D or a new input channel address. The bus is controlled by the input pins 18 to 23.
- SCLK (pin 61): serial clock. Used to synchronize the serial result of an A/D conversion coming from the SDATA pin (pin 62).
- SDATA (pin 62): serial output data. The result of an A/D conversion is presented bit by bit after each bit is determined by the successive approximation algorithm. Valid on the rising edge of SCLK (pin 61), data appears MSB first, LSB last.
- $\overline{EOC}$ (pin 60): this output indicates the end of a conversion or calibration cycle of the A/D. It is high during conversion and will fall to a low state upon completion of the conversion cycle indicating the data is valid at the output. Returns high on the first subsequent read or the start of a new conversion.
- $\overline{EOT}$ (pin 59): if low, it indicates that enough time has elapsed since the last conversion for the A/D to acquire the analog input signal.
- MA2, MA1, MA0, EN2 and EN1 (pins 52 to 56): multiplexer addresses pins. They are used for addressing external multiplexers when more than 16 single-ended or 8 differential input channels are desired.

THEORY OF OPERATION

The SP9488 includes complex circuitry. The description of its operation will be gradual, starting at a system level to finish with a detailed explanation, including timing informations.

A. System Description:

The SP9488 can be seen as a two part system:

- The "Signal Conditioning" section, including the multiplexers and the instrumentation amplifier.
- The "Converting" section, including the sampling A/D (plus an input amplifier).

The Data Bus (pins 1 to 16) is shared by both sections. The "Signal Conditioning" section uses it to get new channel addresses and the "Converting" section uses it to get control bits (like selection of the mode and range) or to give the external world the result of a conversion or a status report. The management of the bus between these two sections is insured by the control lines A0, A1, $\overline{CS2}$, $\overline{CS1}$, $\overline{RD}$ and $\overline{WR}$ (pins 18 to 23).

Table 1 gives a summary of the SP9488 functions, versus the logic levels on the control lines:

$\overline{CS1}$	$\overline{CS2}$	A0	A1	$\overline{WR}$	$\overline{RD}$	FUNCTION
1	1	X	X	X	X	No operation (Data Bus in tri-state)
1	0	X	X	↓	1	The external world selects a new input channel
0	1	X	1	↓	1	The external world writes control bits to the A/D
0	1	1	0	↓	1	The A/D starts a conversion
0	1	1	0	X	0	The external world reads the result of a conversion
0	1	0	0	1	0	The external world reads the status register of the A/D

Note: X means "do not care" (but do not leave pin open).
↓ means that the event occurs on a high to low transition.

Table 1. SP9488 Functions

B. "Signal Conditioning" Section Description:

1. Single-Ended or Differential Input Configuration:

The SP9488 contains two 8 single-ended channels multiplexers which can be configured in 1 16 single-ended channels or 8 differential channels multiplexer following the user's choice. Table 2 shows the connections to obtain one or the other input configuration.

2. Addressing the Multiplexers:

As mentioned earlier the multiplexer addressing is done through the shared Data Bus: the 7 LSB's (DB0 to DB6) are used to carry a new input channel address. Table 1 indicates that $\overline{CS1}$ and $\overline{RD}$ must be high and $\overline{CS2}$ low (the logic levels on A0 and A1 do not care) to select a new input channel. A high to low transition on the $\overline{WR}$ control line makes the new channel selection. Table 3 lists the selected channel as a function of the code on the Data Bus.

In Table 3, the value on DB5 and DB6 does not care. These two addresses are important only when a channel input expansion is desired.

Single-Ended Input Configuration:

DB6	DB5	DB4	DB3	DB2	DB1	DB0	SELECTED CHANNEL
X	X	0	1	0	0	0	CH0
X	X	0	1	0	0	1	CH1
X	X	0	1	0	1	0	CH2
X	X	0	1	0	1	1	CH3
X	X	0	1	1	0	0	CH4
X	X	0	1	1	0	1	CH5
X	X	0	1	1	1	0	CH6
X	X	0	1	1	1	1	CH7
X	X	1	0	0	0	0	CH8
X	X	1	0	0	0	1	CH9
X	X	1	0	0	1	0	CH10
X	X	1	0	0	1	1	CH11
X	X	1	0	1	0	0	CH12
X	X	1	0	1	0	1	CH13
X	X	1	0	1	1	0	CH14
X	X	1	0	1	1	1	CH15

Differential Input Configuration:

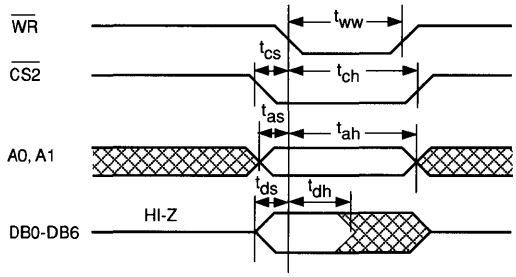
DB6	DB5	DB4	DB3	DB2	DB1	DB0	SELECTED DIFFERENTIAL CHANNELS
X	X	1	1	0	0	0	CH0/CH8
X	X	1	1	0	0	1	CH1/CH9
X	X	1	1	0	1	0	CH2/CH10
X	X	1	1	0	1	1	CH3/CH11
X	X	1	1	1	0	0	CH4/CH12
X	X	1	1	1	0	1	CH5/CH13
X	X	1	1	1	1	0	CH6/CH14
X	X	1	1	1	1	1	CH7/CH15

Table 3. Multiplexer Addressing in the SP9488

INPUT CONFIGURATION	CONNECT PIN 46 (MUX OUT) TO	CONNECT PIN 47 (-AMP IN) TO	CONNECT PIN 29 (+AMP IN) TO
16 Single-Ended Channels	Pin 29 (+AMP IN)	Pin 49 (PGND1)	Pin 46 (MUX OUT)
8 Differential Channels	Pin 47 (-AMP IN)	Pin 46 (MUX OUT)	Left Open

Table 2. Multiplexers Configuration for the SP9488

Figure 1 shows the Data Bus timing when used to address the multiplexers.



Note: $\overline{CS1}$ is high

-t_{ds} = t_{cs} = t_{as} = data and address set-up times = 20 ns min.
-t_{dh} = data hold time = 5 ns min.
-t_{ch} = t_{ah} address hold time = 40 ns min.
-t_{ww} = write width pulse = 40 ns min.

FIGURE 1
DATA BUS TIMING (MULTIPLEXER ADDRESSING)

3. Input Channel Expansion:

The SP9488 can be extended to 24 or 32 single-ended, or 16 differential input channels without the addition of any component. Figure 2a shows how to connect two external 8 channels single-ended multiplexers to get a 32 channels single-ended input system. Table 4a shows the associated addresses.

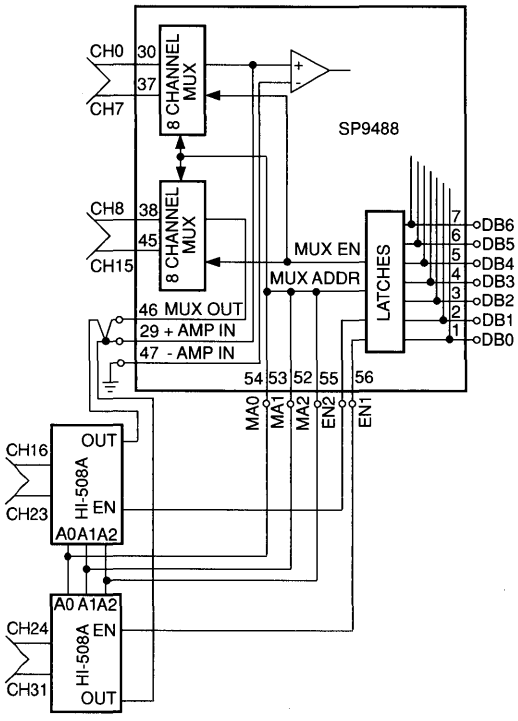


FIGURE 2a
INPUT EXPANSION OF THE SP9488
(32 SINGLE-ENDED CHANNELS)

DB6	DB5	DB4	DB3	DB2	DB1	DB0	SELECTED CHANNELS
0	0	0	1	*	*	*	CH0 to CH7
0	0	1	0	*	*	*	CH8 to CH15
0	1	0	0	*	*	*	CH16 to CH23
1	0	0	0	*	*	*	CH24 to CH31

Table 4a. Addresses for the Input Expansion of the SP9488 (32 Single-Ended Channels)

Figure 2b shows how to connect one external 16 channel single-ended multiplexer to get the same 32 single-ended expansion and table 4b indicates the associated addresses.

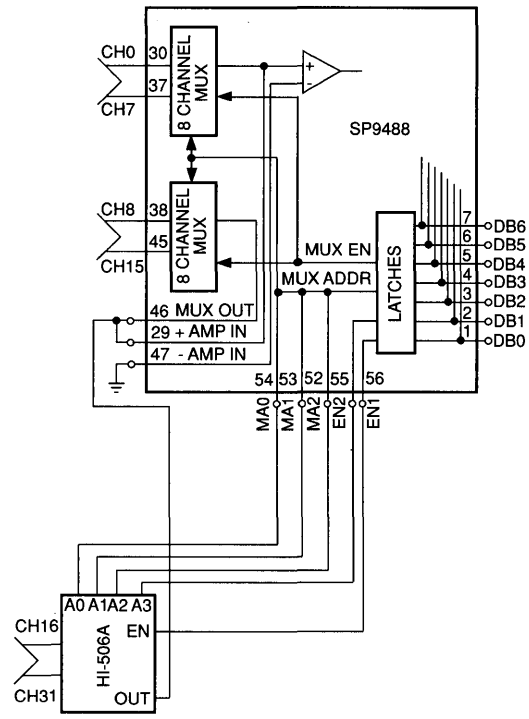


FIGURE 2b
INPUT EXPANSION OF THE SP9488
(32 SINGLE-ENDED CHANNELS)

DB6	DB5	DB4	DB3	DB2	DB1	DB0	SELECTED CHANNELS
0	0	0	1	*	*	*	CH0 to CH7
0	0	1	0	*	*	*	CH8 to CH15
1	*	0	0	*	*	*	CH16 to CH31

Table 4b. Addresses for the Input Expansion of the SP9488 (32 Single-Ended Channels)

Figure 2c shows how to connect 2 external 8 single-ended multiplexers to get a 16 differential input channels system. Table 4c indicates the associated addresses.

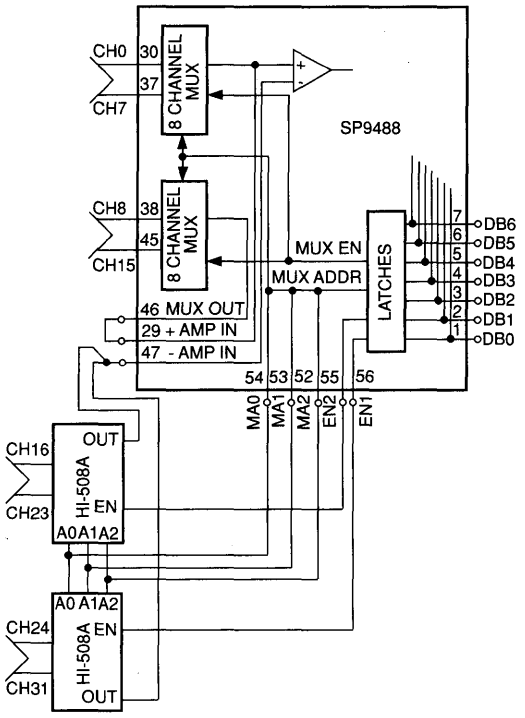


FIGURE 2c
INPUT EXPANSION OF THE SP9488
(16 DIFFERENTIAL CHANNELS)

DB6	DB5	DB4	DB3	DB2	DB1	DB0	SELECTED CHANNELS
0	1	0	1	*	*	*	CH0/CH16 to CH7/CH23
1	0	1	0	*	*	*	CH8/CH24 to CH15/CH31

Table 4c. Addresses for the Input Expansion of the SP9488 (16 Differential Channels)

Note: In Tables 4a, 4b, and 4c, only a range of selected channels is given: the value on DB0, DB1 and DB2 determines one channel.

C. "Converting" Section Description:

1. A/D Description:

The A/D used in the SP9488 is a 16-bit sampling A/D converter using the successive approximation algorithm. It uses a charge redistribution architecture that achieves high accuracy: the linearity, offsets and gains can be calibrated in different ways (see next paragraph). The A/D converter of the SP9488 comes complete with an internal reference. The modes and ranges are digitally programmable. However, the user has to supply a master clock (through the CLKIN pin) with a frequency between 100 kHz and 4 MHz. The relationship between the clock frequency and the conversion time is explained in paragraph 3c. Paragraph 3b explains how to initiate a conversion.

2. Set-up of the A/D Through the Data Bus:

As mentioned earlier, the mode and range of the A/D and the calibration modes are selected through the Data Bus. To be able to write control bits to the A/D, Table 1 shows that a high to low transition on the $\overline{WR}$ pin is necessary at the same time as $\overline{CS2}$, A1 and $\overline{RD}$ are high, $\overline{CS1}$ is low (the logic level on A0 does not care). The control bits are brought to the A/D by the DB0 to DB6 line (the same as the ones which carry the multiplexers addresses):

- DB3, DB4, DB5, DB6 carry the mode and range selection bits. Table 5 shows a truth table for these bits.

DB3	DB4	DB5	DB6	MODE AND RANGE SELECTED
1	0	1	1	Bipolar 20V
1	1	0	1	Bipolar 10V
1	1	1	0	Bipolar 5V
0	0	1	1	Unipolar 10V
0	1	0	1	Unipolar 5V
0	1	1	0	Unipolar 2.5V
X	0	0	0	Forbidden

Table 5. A/D Mode and Range Selection Bits

- DB1 sets the format of the conversion result (16-bit output code). When high, the output code can be read in one shot (16-bits); if low it can be read in two bytes available on pins DB0 to DB7, the eight most significant bits first.
- DB0 and DB2 are calibration bits. These two bits allow the user to choose between two different calibration procedures:

1. DB2: When this bit is brought high, all the internal logic of the A/D clears. When it returns low a full calibration begins, which takes 1,443,840 master clock cycles (360 ms with a 4 MHz clock) to complete. The same reset cycle can be obtained by performing a write operation with A0, $\overline{CS1}$, A1, low; $\overline{CS2}$ and $\overline{RD}$ high. The $\overline{EOC}$ output remains high throughout the reset operation and will fall upon completion. This mode of calibration is performed after a power-up or after the operating temperature of the SP9488 has changed.

2. DB0: When this bit is low, a calibration, termed "interleave" is initiated. Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. A calibration cycle is performed after 72,192 conversions. Practically this type of calibration extends the conversion time by 20 master clock periods. Other than reduced throughput, interleave is totally transparent to the user.

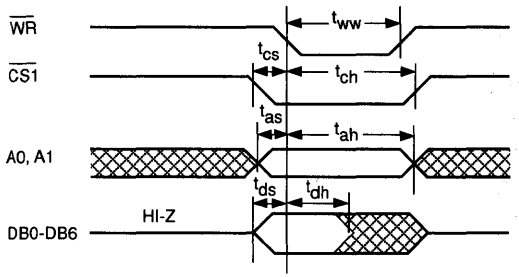
Table 6 summarizes the functions of DB0, and DB2 when used as control bits for the A/D of the SP9488.

DB0	DB2	FUNCTIONS
X	1	Full Reset Calibration
0	0	Initiate Interleave Calibration
1	0	Terminate Interleave Calibration

X means "do not care"

Table 6. Calibration Control Bits for the SP9488

The timing for writing control bits to the A/D is given at Figure 3.



Note: $\overline{CS2}$ is high

-t_{ds} = t_{cs} = t_{as} = data and address set-up times = 20 ns min.
-t_{dh} = data hold time = 5 ns min.
-t_{ch} = t_{ah} address hold time = 40 ns min.
-t_{ww} = write width pulse = 40 ns min.

FIGURE 3
DATA BUS TIMING (WRITING OF CONTROL BITS TO A/D)

Generally before starting a conversion, a set of bits must be written to the A/D in order to be sure that the conversion will be properly performed and to take advantage of the high accuracy of the SP9488. A calibration must be performed after the system is powered up.

3. Detailed Timing of the A/D:

a. Master Clock

The A/D of the SP9488 operates from a master clock which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the SP9488 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal. All calibration, conversion and throughput times directly scale to the master clock frequency. Thus, throughput can be precisely controlled and/or maximized using an external master clock. In contrast, the A/D's internal oscillator will vary from unit to unit and over temperature. Its tolerance gives rise to minimum and maximum conversion times and throughput rates. The SP9488 is specified for accurate operation with an external clock up to 4 MHz; its internal is specified at a minimum of 2 MHz.

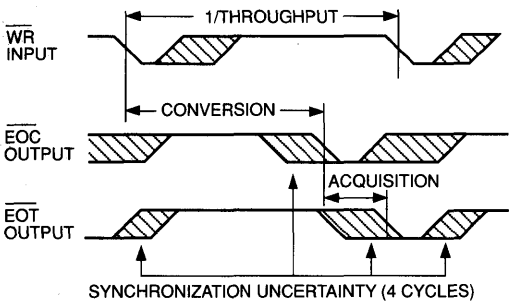
b. Initiation of Conversion

Table 1 indicates that a falling transition on the $\overline{WR}$ input with $\overline{CS1}$, A1 low and $\overline{CS2}$, A0, $\overline{RD}$ high will initiate a conversion. Under microprocessor control, it means that a "write" instruction to the base address of the SP9488's A/D (determined by $\overline{CS1}$, $\overline{CS2}$, A0 and A1) will initiate a conversion. A falling edge on the $\overline{WR}$ input puts the A/D sample-hold in the hold mode. The $\overline{WR}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50 ns. Upon completion of the conversion cycle, the sample-hold automatically returns to the track mode.

c. Conversion Time/System Throughput

Upon completion of a conversion cycle and returning to the track mode, the SP9488's A/D requires time to acquire the analog signal before another conversion can be initiated. The acquisition of the A/D is specified as six master clock cycles plus 2.25 µs. This adds to the conversion time to define the A/D and the SP9488's maximum throughput. The conversion time of the A/D, in turn, depends on the sampling, calibration and master clock conditions. There are basically two different sampling modes: the asynchronous and synchronous modes. Figure 4 shows their timing respectively, while Table 7 shows the conversion times and throughput rates associated with these two modes.

ASYNCHRONOUS SAMPLING



SYNCHRONOUS SAMPLING

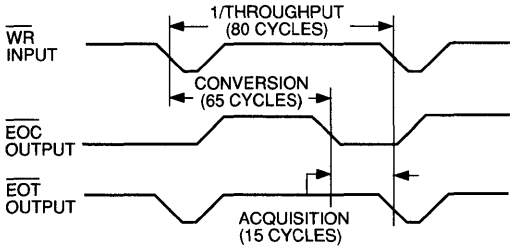


FIGURE 4
ASYNCHRONOUS AND SYNCHRONOUS SAMPLING OF SP9488'S (A/D)

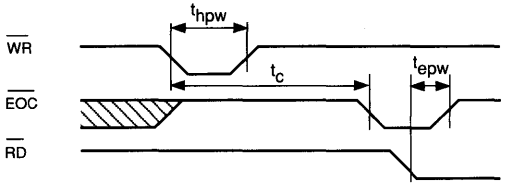
SAMPLING MODE	CONVERSION TIME	THROUGHPUT TIME
Asynchronous	65T min. 69T+235 ns max.	75T+2.25 µs max.
Synchronous	65T	80T

T=one master clock cycle

Table 7. Conversion and Throughput Times

The 4 cycles uncertainty that can be seen in the asynchronous mode are due to the fact that the sampling clock (on the $\overline{WR}$ pin) and the master clock are not synchronous. The maximum throughput is obtained by tying the $\overline{EOT}$ output to the $\overline{WR}$ input. In this case the master clock and the sampling clock are synchronous and the maximum throughput (50 kHz with a 4 MHz master clock) is achievable.

$\overline{EOC}$ is high during conversion. It will fall at the end of the conversion and will return high within four master clock cycles from the start of a read data operation or a conversion cycle. Figure 5 shows the conversion timing.



t_{hpw} = $\overline{WR}$ pulse width = $1/f_{CLK}$ + 50 ns min.; t_c max.
t_c = conversion time
t_{epw} = $\overline{EOC}$ pulse width = $4/f_{CLK}$ -20 ns.

FIGURE 5
CONVERSION TIMING

So far only the A/D has been taken in account in the evaluation of the throughput rate. In fact the total throughput of the system (SP9488) is not reduced by the presence of the multiplexers and the instrumentation amplifier, because of the pipeline technique for acquiring the analog signal. This technique selects a new channel immediately after the conversion of the former channel has started. So the acquisition of the "Signal Conditioning Section" is done while the conversion of the former channel is performed. Figure 6 illustrates the pipeline technique.

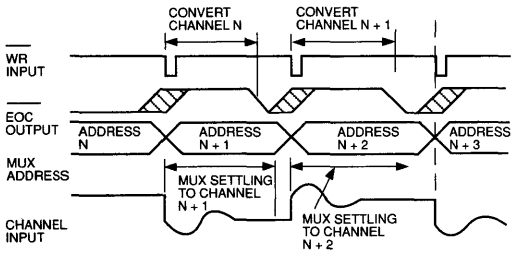
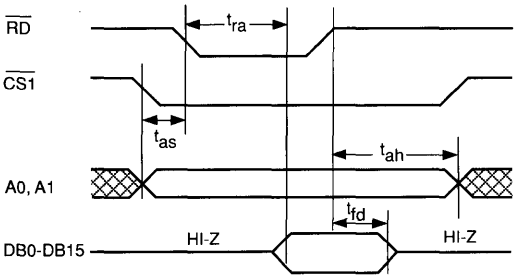


FIGURE 6
PIPELINED MUX INPUT CHANNELS

d. Reading of the Output Code

The result of a conversion can be read by strobing low the $\overline{RD}$ control input with $\overline{CS2}$, A0, high and $\overline{CS1}$, A1 low (the value on $\overline{WR}$ does not care). The data is read in one 16-bit word or two bytes following the control bits written to the A/D. Figure 7 shows a detailed timing of the reading cycle.



t_{as} = address set-up time = 20 ns min.
t_{ah} = address hold time = 50 ns min.
t_{ra} = $\overline{RD}$ low to data valid (access time) = 150 ns max.
t_{fd} = $\overline{RD}$ high to output HI-Z (output float delay) = 140 ns max.

FIGURE 7
DATA BUS TIMING (READING THE OUTPUT DATA OF THE SP9488)

The A/D of the SP9488 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in the SP9488 throughput. Enabling the tri-state outputs while a conversion is in process will not introduce errors. When TTL loads are utilized, the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the Data Bus of the SP9488 is therefore recommended.

e. Reading of the Status Word of the A/D

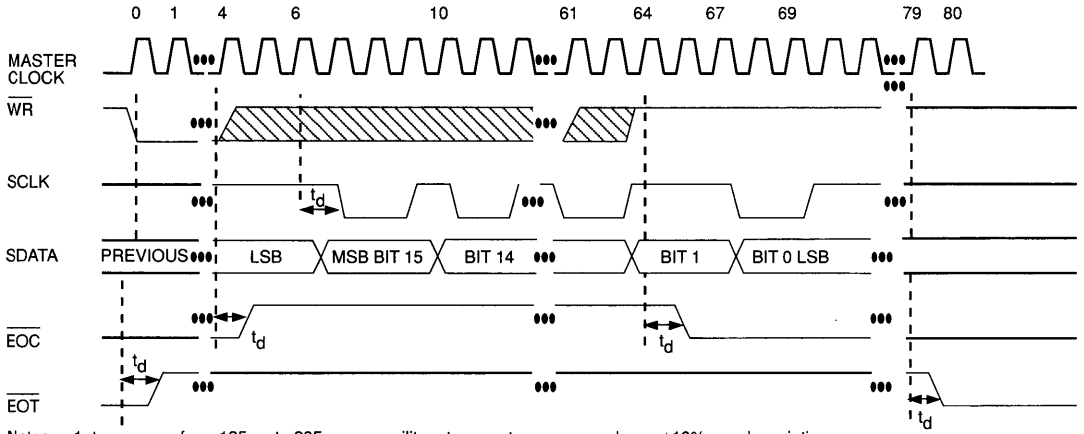
A status information byte can be read from the SP9488 when $\overline{RD}$ is strobed low while $\overline{CS1}$, A0, A1 are low, $\overline{CS2}$, and $\overline{WR}$ are high (see Table 1). The timing for reading the status byte is the same as reading the result of a conversion (figure 7). Table 8 defines all the status bits and their position on the Data Bus.

f. Serial Interface

The SP9488 presents also the result of a conversion serially (MSB first). It is available on the SDATA pin (pin 62) and to ease the interface with the external world, a serial clock, SCLK (pin 61) is provided. Figure 8 shows the general timing for the serial output.

PIN	STATUS	DEFINITION
DB0	$\overline{\text{End of conversion}}$	Falls upon completion of a conversion and returns high on the first subsequent read
DB1	Reserved	Reserved for factory use
DB2	Low byte/high byte	When data is to be read in an 8 bit format, indicates which byte will appear at the output next
DB3	$\overline{\text{End of track}}$	When low, indicates the input has been acquired to the A/D accuracy
DB4	Reserved	Reserved for factory use
DB5	Tracking	High when the A/D is tracking the input
DB6	Converting	High when the A/D is converting a held input
DB7	Calibrating	High when the A/D is in a calibration cycle

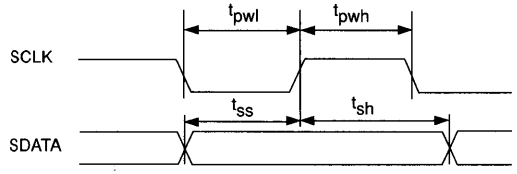
Table 8. Status Bit Definition



Notes: 1. t_d can vary from 135 ns to 235 ns over military temperature range and over ±10% supply variation.
2. For asynchronous mode, transitions of SCLK, SDATA, $\overline{\text{EOC}}$, $\overline{\text{EOT}}$ can shift by up to 4 clocks; e.g. the first high to low transition of SCLK may be on clock #6 to #9. The timing relationship between SCLK, SDATA, $\overline{\text{EOC}}$, and $\overline{\text{EOT}}$ is fixed.

FIGURE 8
SERIAL OUTPUT TIMING

Figure 8 shows that, just subsequent to each bit decision the serial clock (SCLK) will fall and return high once the bit information on SDATA has stabilized. Hence the rising edge of the SCLK output should be used to clock the data out of the SP9488. It can be seen too that the first bit of information is available after 8 master clock cycles (from the falling edge of $\overline{\text{WR}}$). Figure 9 specifies the timing for the SCLK and SDATA pin.



t_{pwl} = pulse width low = $2/f_{CLK}$ ns
t_{pwh} = pulse width high = $2/f_{CLK}$ ns
t_{ss} = SDATA to SCLK rising = $2/f_{CLK}$ -100 ns min.
t_{sh} = SCLK rising to SDATA = $2/f_{CLK}$ -100 ns min.

FIGURE 9
TIMING FOR THE SCLK AND SDATA OUTPUT PINS

APPLICATION INFORMATION

A. Power Supply and Grounding Considerations, Layout Precautions:

Power supplies for the SP9488 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output codes may result with noisy power supplies. It is important to remember that 310 μv is 1LSB15 bit for a 10 volt range. Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable capacitors are 10 μF tantalum types in parallel with 0.1 μF disc ceramic types.

To ensure maximum accuracy, the SP9488 has three different analog grounds separated from the digital ground, which must be routed properly to prevent DC and transient errors. DC errors can be caused by current flowing through a run resistance between the system ground reference (1 mA through 0.3 Ohm can cause 1LSB15 bit of error for a 10 volts range). The best way to prevent this type of error is to connect the digital and analog grounds very close to the SP9488 and use this point as the system ground. This can be done as a so-called "star-ground" as shown in Figure 10. The single common ground reference ensures no ground current or ground loop errors.

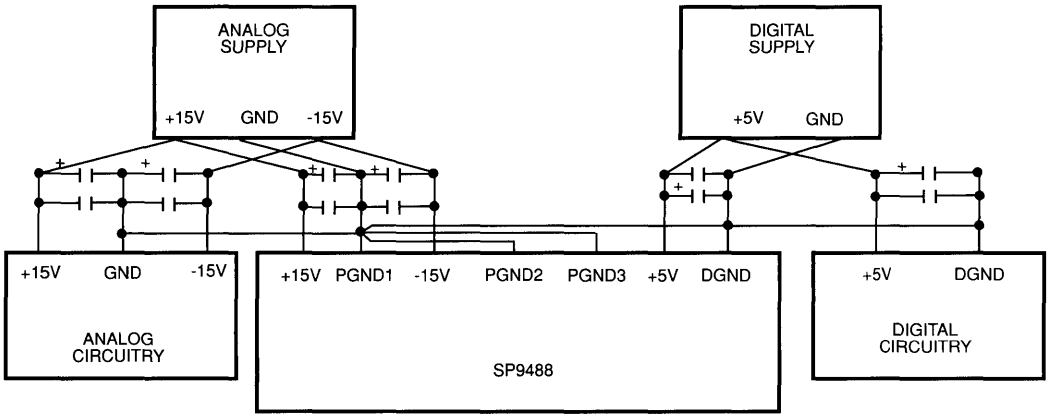


FIGURE 10
GROUNDING THE SP9488

The SP9488 has been laid out so that all the analog pins (24 to 51) and the digital pins (52 to 62 and 1 to 23) are together. This can simplify the design of a printed circuit board layout and make easier the separation of analog and digital signals. Figure 11 shows a suggested layout of the SP9488 and other circuitry.

B. Reference Capacitor:

As mentioned in the "pin description" paragraph, a 0.47 µF tantalum capacitor must be provided by the user at pin 24 (REF). This pin is the output of the 4.5V voltage reference used by the A/D of the SP9488. It can not be used for other purposes without being buffered.

C. Utilization of the SP9488 Under Static or Dynamic Input Signals:

The SP9488 has been designed to give the user the liberty of tailoring the "Signal Conditioning" section following his application. More precisely, there is no filtering element in the "Signal Conditioning" section, limiting the bandwidth of the input amplifiers; this gives maximum performance (fast settling time) when DC input signals are digitized. When wideband AC signals are digitized however, no filtering means that wideband noise is presented to the input of the A/D of the SP9488. Such noise is sampled at 50 kHz, and aliased back into the DC to 25 kHz band. The Signal-to-Noise measurement of the system can then be affected seriously. In this type of application, it is recommended that the user provides a filter between Pin 28 (DIFFAMPOUT) and Pin 27 (ANAIN) to limit the bandwidth of the input signal. A filter may even be needed for each input channel, depending on the application. Figure 12 shows the frequency response of the analog front end of the SP9488 when no filtering is processed (Pins 27 and 28 tied together).

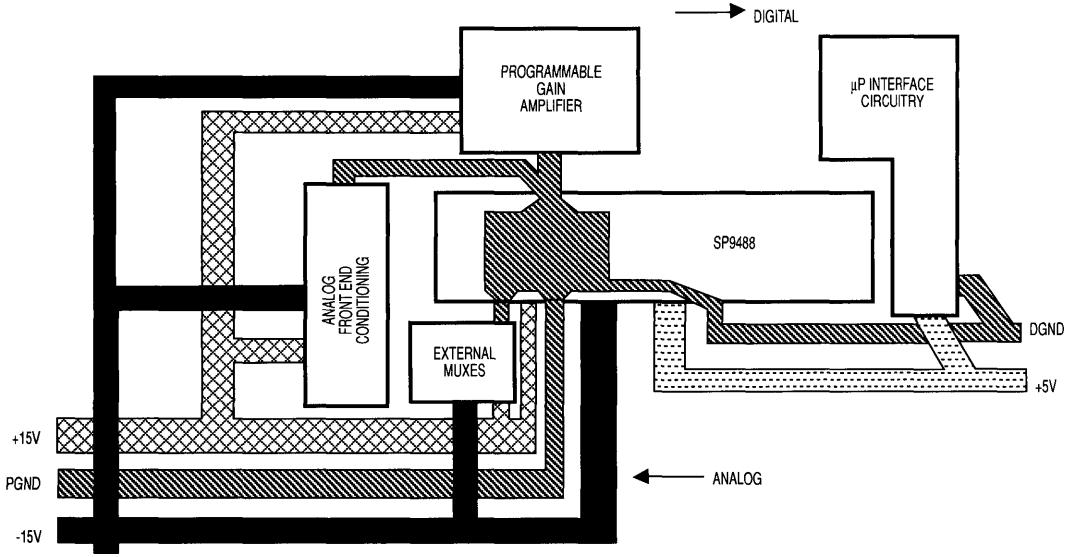


FIGURE 11
PCB LAYOUT FOR THE SP9488

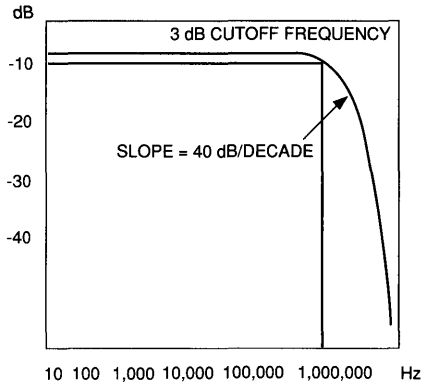


FIGURE 12
FREQUENCY RESPONSE OF THE SP9488
ANALOG FRONT END

D. General Interface of the SP9488 to a Microprocessor:

The interface of the SP9488 to a microprocessor involves several questions. First, write instructions must be executed by the processor to select new input channels, control the A/D or start a conversion. Read instructions have to be performed to inform the µP on the SP9488 status or receive the result of a conversion. When a conversion has been started, the processor has to wait for its end before reading valid conversion results. The SP9488 provides an output signal EOC which indicates when a conversion is in progress. This signal can be polled by reading it through an external tri-state buffer. The EOC can also generate an interrupt upon completion of conversion, if the processor has other tasks to perform (for instance selecting a new input channel). Another possible time-out method is to insert a sufficient number of "do-nothing" instructions to ensure that enough processor time has elapsed before reading the conversion result. Once established that the conversion is finished, the processor can get the result. For the SP9488 it can be read immediately by 8 or 16 bits µP, thanks to the user selected output format (two bytes or one 16 bit word).

The following paragraphs show the SP9488 interface to different families of microprocessors. For clarity, no linear hardware has been shown.

1. Intel:

The interface of the SP9488 to any INTEL processor is basically the same. It is the simplest too because INTEL processors have $\overline{RD}$ and $\overline{WR}$ output signals directly compatible with the $\overline{RD}$ and $\overline{WR}$ input signals of the SP9488. Figure 13 shows the interface to a 8088 µP. Writing data to the SP9488 consists in <MOV addr, AX> where AX is the register containing the data to be loaded, and addr the decoded address of the SP9488. The read instructions are <MOV AX, addr> type instructions.

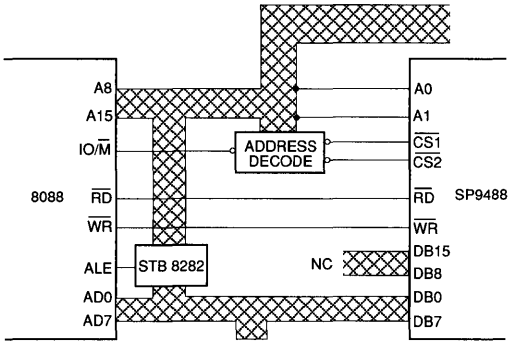


FIGURE 13
INTERFACE OF THE SP9488 TO AN INTEL µP

2. Motorola 8-Bit Non-Multiplexed Format (6800, 6500 Series):

Figure 14 shows this interface. Writing data to the SP9488 consists of <STAA,addr> instructions, where A is the accumulator (register) containing the data to be loaded and addr is the decoded address of the SP9488. The conversion result or the status word of the A/D is read by <LDAA,addr> type instructions: the data is then transferred from the SP9488 to the processor's accumulator.

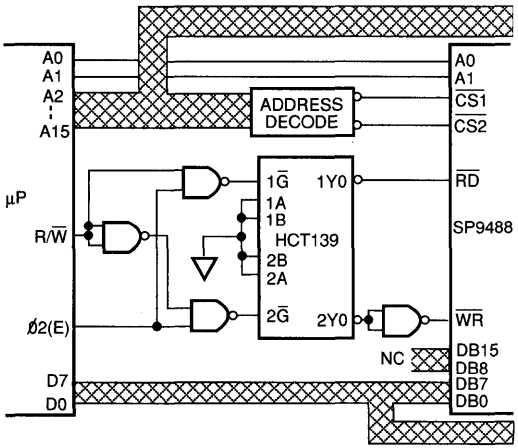


FIGURE 14
INTERFACE OF THE SP9488 TO A 6800 TYPE µP

3. Motorola 8-Bit Multiplexed Format (6801, 146805 Series):

The interface is very similar to the non-multiplexed format. Same type of instructions can be used to execute data transfers between the processor and the SP9488. Figure 15 shows how to demultiplex the data/address bus when the processor is used in expanded multiplexed mode. The rest of the interface is the same as Figure 14.

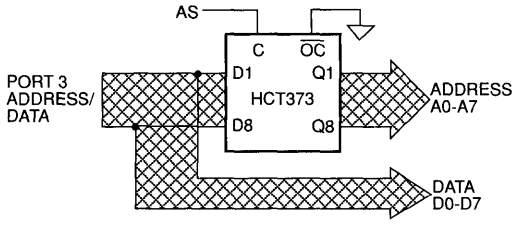


FIGURE 15
DEMULTIPLEXING THE ADDRESS/DATA BUS
OF A 6801 µP TYPE

4. Motorola 16-Bit Multiplexed Asynchronous Format (68000 Series):

A typical interface to the 68000 is shown in Figure 16. The extra logic gates are necessary to generate the $\overline{DTACK}$ signal of the 68000 when it writes to the SP9488 or reads the status word of the SP9488. If the processor tries to read the result of a conversion while the SP9488 is still converting, the read cycle will be stretched out over the entire conversion time by taking the $\overline{EOC}$ output of the SP9488 back into the $\overline{DTACK}$ input of the 68000. Writing data to the SP9488 consists of a <MOV.B Dn,addr> where Dn is the data register which contains the data to be loaded to the SP9488 and addr is the decoded address. Data is read from the SP9488 using a <MOV.B addr,Dn> instruction with the result of a conversion or a status report placed in the register Dn.

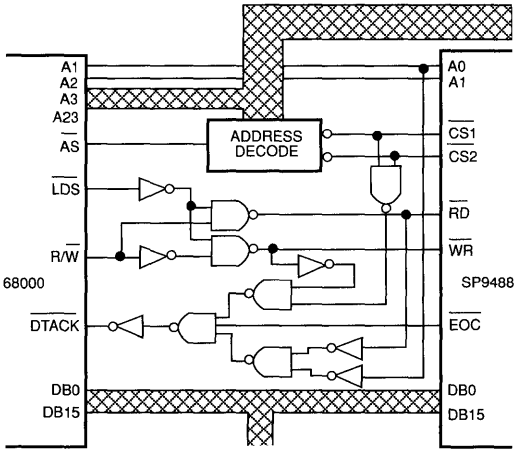


FIGURE 16
INTERFACE OF THE SP9488 TO A 68000 TYPE µP

E. Autocalibrated System:

The A/D of the SP9488 is self-calibrating: it means that when the opportunity is given to the device to perform a calibration, offset and gain errors due to it are negligible. Most of the offset and gain errors of the SP9488 are due to the front-end circuitry. These errors are actively trimmed at the factory to reduce them to a minimum. However, if the user desires it, there is an elegant way to reduce these errors to zero: the system autocalibration. Figure 17 shows a block diagram of the hardware configuration.

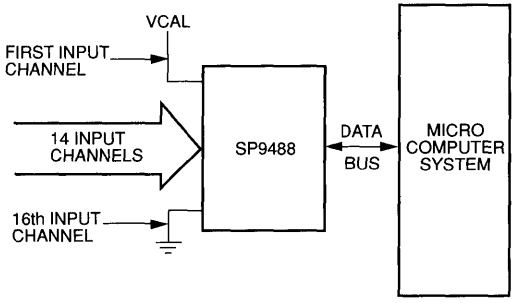


FIGURE 17
HARDWARE CONFIGURATION OF AN AUTOCALIBRATED
SYSTEM USING THE SP9488

The different steps for correcting offsets and gain errors are as follows:

1. Measure of ground (GND): it gives the offset system error.
2. Measure of a known voltage (VCAL): the following formula gives the system gain error (GE):

   GE = (ACVCAL - ACGND) / ICVCAL

   Where ACVCAL is the actual code measured for VCAL, ACGND is the actual code measured for GND, and ICVCAL is the ideal code for VCAL.
3. Storage of these numbers to correct future readings. The following formula gives the corrected code for any reading (CC):

   CC = (AC - ACGND) * GE

   Where AC is the actual code measured.

To apply this adjustment procedure, a stable and accurate VCAL is required.

SP9488 PERFORMANCE

A. Integral Linearity

Integral linearity is defined as the deviation of the transfer function from an ideal straight line through zero and full scale (End Point definition). Thanks to a unique calibration algorithm in SP9488's A/D and a fine design of the analog front end the integral linearity errors are kept below 0.001% of full scale typically.

Table 9 shows the integral linearity errors of a typical unit measured at the center code on both sides of each major 15 bit transition (bipolar 5V mode).

CODE-1 (OCTAL)	I.L. ERR (%)	CODE (OCTAL)	I.L. ERR (%)
1	0.0000	1	0.0000
2	-0.0000	2	0.0001
4	-0.0001	3	-0.0001
10	-0.0003	5	-0.0002
20	-0.0003	11	-0.0004
40	-0.0004	21	-0.0001
100	-0.0003	41	-0.0002
200	-0.0002	101	-0.0001
400	-0.0004	201	0.0001
1000	-0.0003	401	-0.0003
2000	-0.0002	1001	0.0001
4000	-0.0001	2001	0.0001
10000	-0.0002	4001	0.0002
20000	-0.0001	10001	0.0002
40000	-0.0009	20001	0.0003
60000	-0.0006	40001	-0.0008
70000	0.0004	60001	-0.0004
74000	-0.0000	70001	0.0007
76000	0.0001	74001	0.0002
77000	0.0003	76001	0.0003
77400	0.0001	77001	0.0006
77600	0.0003	77401	0.0002
77700	0.0004	77601	0.0005
77740	0.0004	77701	0.0006
77760	0.0003	77741	0.0007
77770	0.0003	77761	0.0005
77774	0.0002	77771	0.0002
77776	0.0001	77775	0.0000
		77777	0.0001

Table 9. Integral Linearity Error of a Typical Unit

B. Dynamic Performance:

The integral linearity is specified statically for the SP9488. This type of error under dynamic conditions is generally quantified by a Signal to Noise Ratio (SNR) test. In this test a finite time sequence of sampled data from a spectrally pure sine wave input is computed by the tester into a frequency spectrum using a Fast Fourier Transform algorithm. From this frequency domain representation of the output data, the effect of integral non-linearity may be measured: harmonics of the input sine wave caused by I.L. errors are aliased into the base band spectrum. The magnitude of the fundamental's spectral lines (the signal) is summed, then divided by the sum of the remaining spectral lines (the noise). The logarithm of this number multiplied by 20 provides the SNR expressed in decibels. For an ideal converter, it can be shown that:

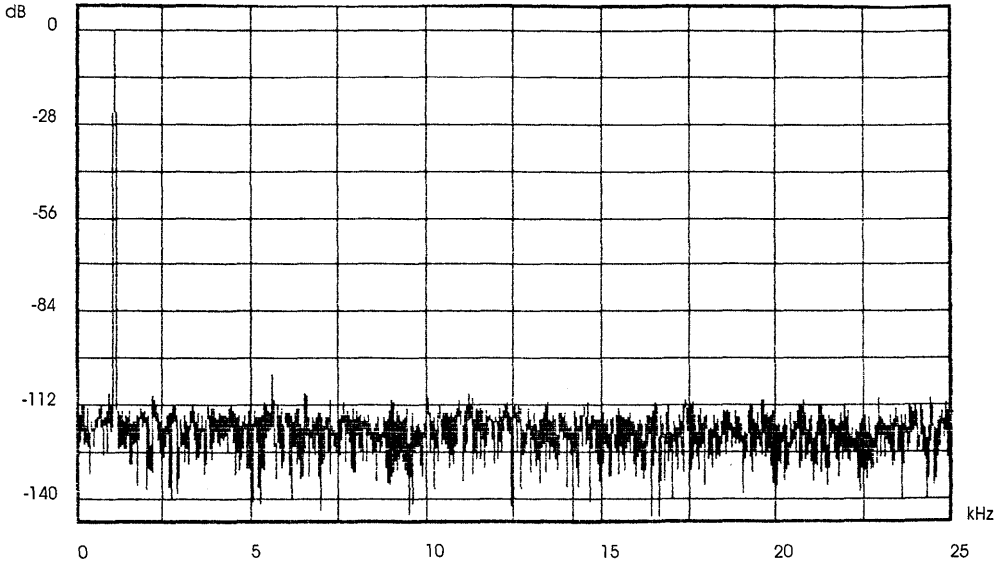
$$SNR = 6.02 \times N + 1.76 \text{ dB}$$

(N = number of bits of the converter)

Graph 1 shows the behavior of the SP9488 with a 1.123 kHz sine wave input: the accuracy is 14 bits.

C. Noise:

The result of each conversion performed by the SP9488 depends on the analog input level on the selected channel and the instantaneous value of noise sources in the data acquisition system. Because the SP9488's output is in digital form, any filtering of its noise must be performed in the digital domain and can be implemented in software with minimal overhead.



Graph 1. FFT of the SP9488, F_{IN} = 1.123 kHz, F_{Sample} = 50 kHz

An easy way of measuring the noise of the SP9488 is to plot an histogram of the codes obtained for a given DC input voltage. Figure 18 shows the histogram for the results of 5000 conversions performed by a SP9488 in bipolar 10V mode; the decimal code 49,152 was arbitrarily chosen and the analog input was set close to the code center.

SP9488 NOISE MEASUREMENT AT CODE 49,152

0	49,145
0	49,146
0	49,147
1	49,148
32	49,149
239	49,150
870	49,151
2595	49,152
1028	49,153
209	49,154
24	49,155
2	49,156
0	49,157
0	49,158
0	49,159

FIGURE 18
HISTOGRAM PLOT AT CODE 49,152 FOR THE SP9488

With a noiseless converter, code 49152 would always appear. The histogram shows a bell shape with all codes other than 49152 due to internal noise. From this histogram it is possible to extract the RMS value of the noise: in this case it is 0.9 LSB 16-bit RMS.

Noise in digital domain can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Oversampling spreads the noise over a wider frequency band (leading to a lower noise density in the desired bandwidth), then the averaging applies a low-pass filtering of the noise above the desired signal bandwidth.

In general, the SP9488's noise performance can be maximized in any application by always sampling at the maximum specified rate of 50 kHz and digitally filtering to the desired signal bandwidth.

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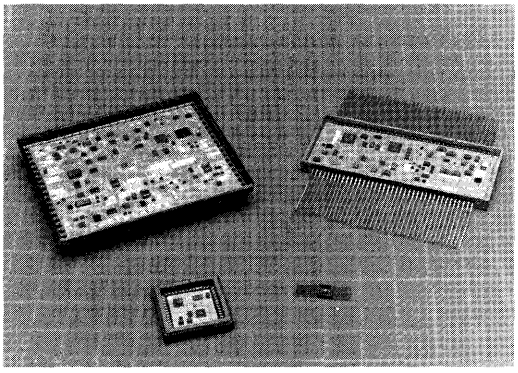
Sipex Corporation

SIGNAL PROCESSING EXCELLENCE

Custom Hybrid Products

FEATURES

- Extremely stable thin-film resistors
- Wide range of packages
- High density circuits using ASICs
- Short time to market
- Industrial, Military & Class S processing



APPLICATIONS

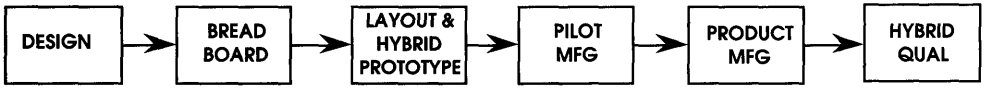
- Data Conversion Products
- Data Acquisition Systems
- Filters
- Mixed Analog/Digital Circuits
- Reactive Load Drivers

DESCRIPTION

As a fully certified 1772 hybrid facility, Sipex offers high quality processing on all custom designs. The same rigorous quality assurance program that is used on standard products is applied to each custom product to deliver product that meets the requirements of MIL-STD-883. With access to the Class S facilities and program management, we also process custom hybrids that are suitable for space applications.

The Custom Products Group offers full service from design through manufacturing, but is quite flexible allowing a customer to enter the system at the point that meets their needs. Some customers have design capability and only come to the Custom Products Group for full scale manufacturing or added capacity. Others come to us to take advantage of the proprietary Sipex technology (ASICs, high performance DACs and A/D products, or other analog products). Combining several technologies in a custom hybrid is often the most effective way to obtain the performance for a demanding application.

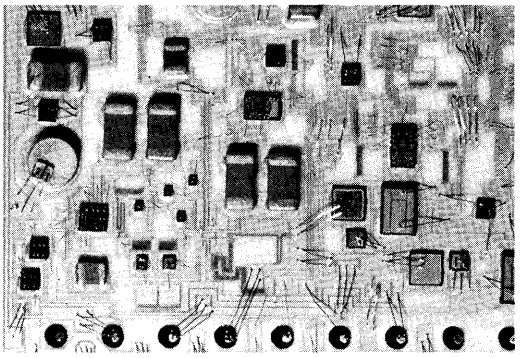
CUSTOM PRODUCT DEVELOPMENT CYCLE *



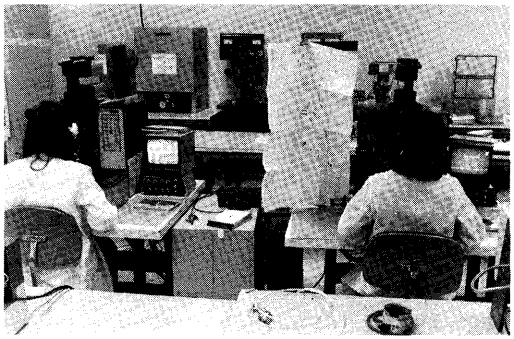
* This is a typical cycle. It can be taylored to meet customer requirements.

TECHNOLOGY

- Chip & Wire
- Thin-Film Substrates
- Thick-Film Substrates
- Thin-Film Chip Resistors
- Resistors on Ceramic
- Compatible with ASIC Components



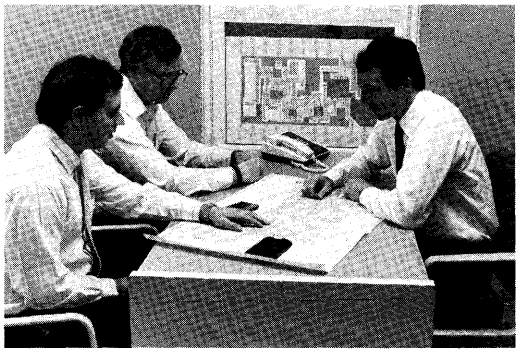
FACILITY



- 1772 Certified
- Typical output 10-20k units/week
- 20,000 Sq. Ft. Manufacturing Facility
- Class 10,000 + Class 100,000 Clean Rm
- Class 100 work areas
- Dedicated Class S area

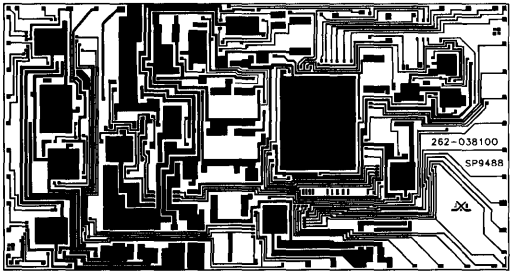
SERVICE

- Full Design Capability
- Analog Circuit Simulation
- Thermal Management Analysis
- Partnership with Customer
- Flexible Production Volumes
- Short Design & Production Cycles



SUBSTRATES

Circuits are manufactured using single-level thin-film and multi-level thick-film technologies. Thin-film substrates are alumina (10-25 mil thick) with gold traces (<0.02 Ω/square) for all conductor runs. Line widths and spacings down to 2 mils are possible. Thin-film resistors can also be built directly onto the substrate in order to reduce parasitic capacitance for high frequency applications or increase circuit density.



Specifications

Resistance Value	Typ Range 20Ω-500kΩ	Max Range 4.7Ω-10MΩ
Resistance Tolerance		
Absolute	±0.1%	±1%
1:1 Ratio	±0.02%	±0.05%
Temperature Coefficient		
Absolute	<10ppm/°C	< 50ppm/°C
1:1 Ratio (Tracking)	2.5ppm/°C	5ppm/°C
Stability		
+25°C Absolute	±0.05%/yr.	±0.1%/yr
1:1 Ratio	±0.005%/yr.	±0.01%/yr
+125°CAbsolute	±0.05%/1000hrs	±0.1%/1000hrs
1:1 Ratio	±0.005%/1000hrs	±0.01%/1000hrs

RESISTORS

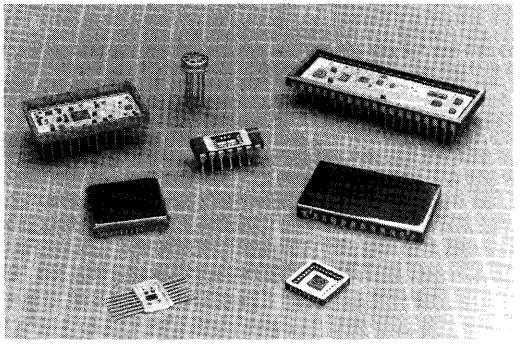
Sipex has full thin-film capability for the manufacture of high precision resistors. Using a stable Ni-chrome thin-film process on passivated silicon substrates we are able to provide a wide range of resistor values.

In addition to standard resistor products, Sipex is able to take advantage of in-house design, manufacture, and laser trim capabilities to provide custom resistor networks. Many resistors over a wide range of values can be combined on a custom network to deliver the ultimate in temperature tracking and component density.

PACKAGES

Packages are available in metal and ceramic. Sizes range from fractions of a square inch to over four square inches. Pin counts of over 100 are available. Most packages are hermetically sealed using an electric seam sealing process. Epoxy, solder, and glass seal packages are also available.

- Flat Pack
- DIP
- LCC
- J-lead
- TO-types
- Plug-in
- SLAM-packages
- Custom packs



DESIGN

A dedicated design engineer is assigned to each custom product. This engineer takes the customer requirements and translates them into a suitable design. He is responsible for the design, prototype, and early manufacturing runs of a product.

Design tools including analog simulation and a thermal analysis program are used to prepare a design. Schematic capture and layout are done using full capabilities of the Sipex CAD group. These include several workstations from CALMA, VIA, ViewLogic and Sun.

THERMAL MANAGEMENT

Thermal management is becoming a more important issue as circuit densities increase. Sipex has been aware of this problem and has developed tools to model heat flow within a hybrid. Conducting a thermal analysis is a routine part of the design of a custom product. The temperature rise of each active and resistive component is calculated, and predicted junction temperatures are compared to maximum ratings. This data is reviewed with the customer, and, if necessary, design or process changes are implemented to lower junction temperatures.

In addition to the thermal models, Sipex has a Hughes thermal mapping system. This can be used to measure the actual temperature of individual components within a hybrid.

COMPONENTS

Sipex has the ability to use most active and passive components available in chip form. This allows a designer to mix chip technologies (bipolar, CMOS, and others) and circuit functions (analog and digital) in a single integrated circuit. Freedom to combine such a wide range of components allows a Sipex custom hybrid to offer the highest performance in a single package.

In addition to standard products, one or more ASICs can be integrated in a hybrid to provide the ultimate in circuit density. For analog applications, Sipex offers a full line of compatible, semi-custom linear gate-arrays and full custom monolithic ICs from the Custom Monolithic Products Division. ASIC devices from other manufacturers can also be used in custom hybrids. Sipex has several foundry relationships to provide ASICs, or we can work with your ASIC supplier.

Passive components such as capacitors and resistors can also be integrated in a hybrid. Resistors are described in greater detail below. Capacitors smaller than 0.1uF can be easily handled in a custom hybrid. Larger caps can be integrated, but usually require special processing. Inductors are not well suited for integration within a hybrid and should be placed externally where possible. If inductors must be used in a hybrid their values should be made as small as possible.

CHIP MOUNT

Active and passive components are mounted on the substrate with electrically conductive epoxies. Eutectic mounting is available for high power applications and other special requirements. Non-conductive epoxies are also used to help secure large components such as capacitors to improve the reliability of the hybrids under stressful environmental conditions.

Most integrated circuits and other semiconductors available as single die can be mounted in a hybrid using these techniques. Passive components such as capacitors and resistors are also attached in this fashion.

WIRE-BONDING

Sipex typically uses 1 mil diameter gold wires with thermosonic bonding for all wires within a hybrid. Gold wirebonding from 0.70 to 2 mils is available for special needs. Thermal compression aluminum wire-bonding from 1 to 20 mils is also available.

ACTIVE LASER TRIM

Active laser trim allows Sipex to achieve high precision analog circuits. With the hybrid circuit powered up, a laser is used to trim resistors setting circuit parameters such as gain, offset, and phase to very high accuracies. This process is used to obtain 18-bit accuracy on several products. Manual systems

and automated LTX systems are used for this process.

ENVIRONMENTAL TESTING

The full range of environmental testing required for military product is available including: temperature cycling,fine and gross leak tests, constant acceleration, PIND test, thermal shock, x-ray, and others.

ELECTRICAL TESTING

Automated test equipment is available for testing an exceptionally wide range of parameters. HP, LTS, MassComp, and Tektronix equipment is used for test. Temperatures from -55°C to 125°C are available with Thermonics temperature forcing systems.

BURN-IN

Dynamic or static burn-in at 125°Cfor 168 hours is typical for Custom Products. 1000 hour life-tests are conducted as required. Other requirements can be reviewed.

PARTIAL EQUIPMENT LIST

Wire Bonders	--> K & S, Mech-el, Orthodyne
Chip Mount	--> Westbond
Seam Seal	--> Benchmark
Laser Trim	--> LTX and manual systems
Temp Forcing	--> Thermoncs
Test	--> HP, Analog Devices LTS, MassComp, Tektronix

SUMMARY

Sipex wants to be your partner in analog hybrid design. We have a wide range of technology and capability available to respond to yuor needs, and the special requirements of your design. Our engineers and program managers are specialists at listening to a customer's needs and translating those into a well designed and manufacturable product that is compatible with the Sipex operations and your specifications.

The individuals assigned to a custom product take personal responsibility for the success of that device and stay with it from the beginning through production. Open and interactive communication with the customer on all aspects of the program reduces the risk of misunderstandings in a custom design and allows Sipex to deliver the highest quality product to you on schedule.

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